Compal Confidential

Broadwell M/B Schematics Document

Intel ULV Processor with DDR3L

Date : 2015/04/14

Version 1.0

Project : Puccini (15")
ABW50

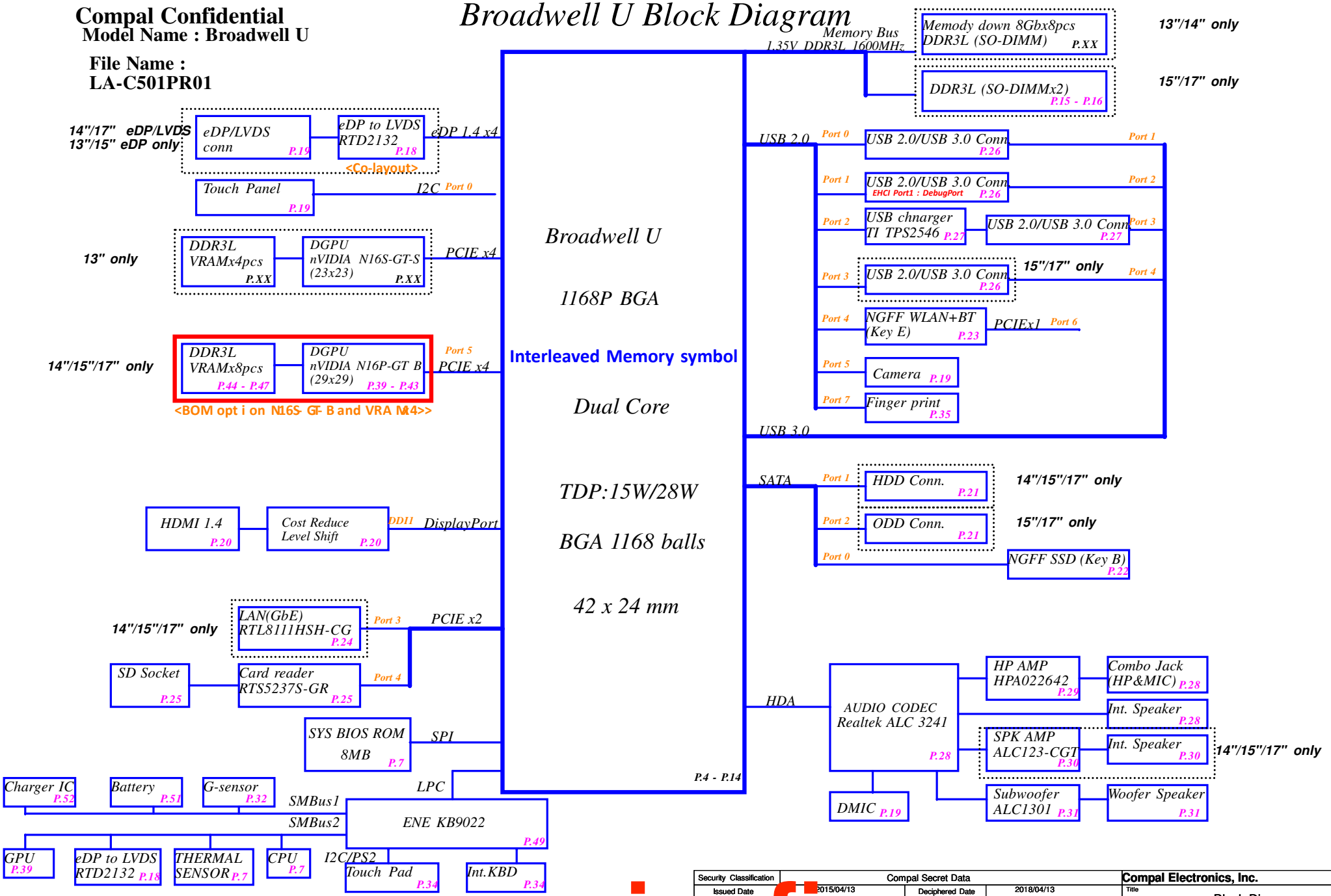
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-C501P	Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 1 of 63	

Compal Confidential
Model Name : Broadwell U

File Name :
LA-C501PR01

Broadwell U Block Diagram



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Title: Block Diagrams

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
+19VB	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VL_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)

short@ : short pad , don't pop.

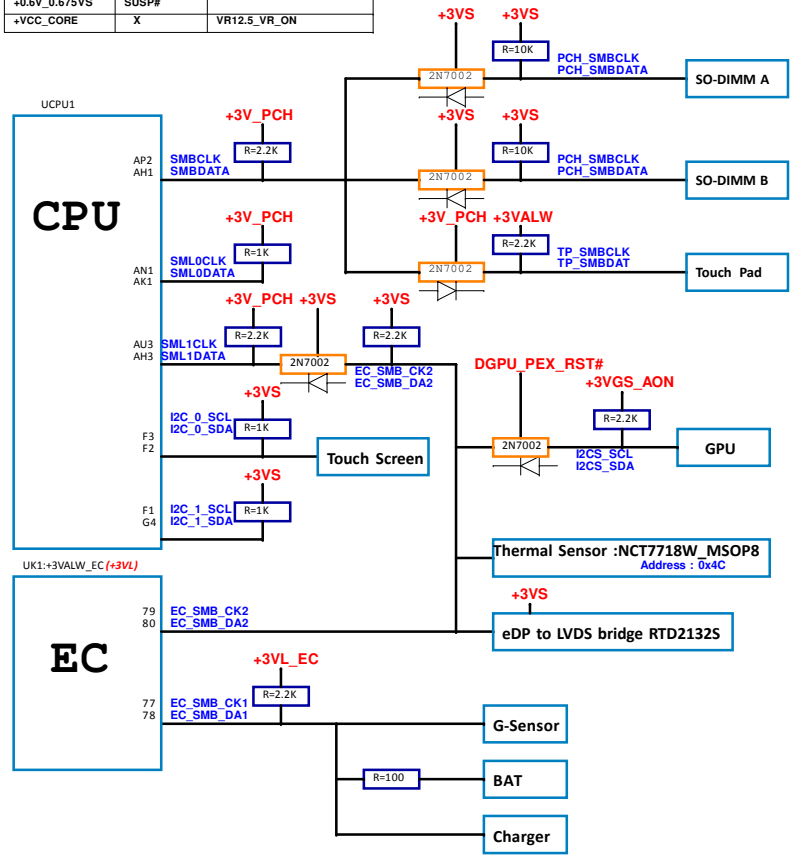
@EMI@,@ESD@,@RF@ : Reserve , don't pop.
RF@ : RF team request, must add.

EMI@ : EMI team request, must add.

ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.

DIS@ : GPU BOM conf i g



ZZZ

PCB
Part Number = DAZ1DO00100
PCB 1DO LA-C501P REV0 M/B 4

45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SOC_SMBCLK SOC_SMBDATA	+3VS	DIMMA	0xA0	TBC	TBC
		DIMMB	0xA4	TBC	TBC
	+3V_PCH	Touch Pad	0X2C	TBC	TBC
SOC_SML0CLK SOC_SML0DATA	+3V_PCH	NA	NA	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3VS	EC	0x1A 0X19	TBC	TBC
		DGPU	0X96	TBC	TBC
		Thermal Sensor	0x4C	TBC	TBC
		LVDS	0X94~97 0X6A 0X6B	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port 1	+3VLP_EC	BAT	0x14 0X15	TBC	TBC
		CHGR	0x12	TBC	TBC
		G-Sensor	0x29	TBC	TBC
SMBUS Port 2					

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C 0	+3VS	Touch Panel	0x20	TBC	TBC
I2C 1	+3VS	NA	TBC	TBC	TBC

CPU Memory down vender control table

CPU_GPIO50 SDRAM_ID4	CPU_GPIO49 SDRAM_ID3	CPU_GPIO48 SDRAM_ID2	CPU_GPIO47 SDRAM_ID1	Vender	MD size	Vender descipti on	Note	Project
0	0	0	0	X	X	X	SODIMMx2 (A,B)	15"/17"
0	0	0	1	X	X	X	SODIMMx1(A) No MDx16bitx4pcs (B)	13"
0	0	1	0	Micron	256x16	MT41K512M16TNA-125:E	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	0	1	1	Samsung	256x16	4B8G1646Q-MYK0	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	0	Hynix	256x16	H5TC8G63AMR-PBA	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	1	Micron	512x8	MT41K512M8RG-107:N	MDx8bitx8pcs (A) SODIMMx1(B)	14"
0	1	1	0	Samsung	512x8	K4B4G0846Q-HYK0	MDx8bitx8pcs (A) SODIMMx1(B)	14"
0	1	1	1	Hynix	512x8	H5TC4G83BFR-PBA	MDx8bitx8pcs (A) SODIMMx1(B)	14"

<USB2.0 port>

USB2.0 port	DESTINATION UMA	DESTINATION Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
2	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
3	USB 2.0/3.0(right side)	USB 2.0/3.0(right side)
4	WLAN/BT	WLAN/BT
5	Camera	Camera
6	X	X
7	FingerPrint	FingerPrint

<PCI-E,SATA,USB3.0>

Lane#	PCI-E	SATA	USB3.0	DESTINATION UMA	DESTINATION Dis
1			1	USB3.0	USB3.0
2			2	USB3.0	USB3.0
3	1		3	USB3.0	USB3.0
4	2		4	USB3.0	USB3.0
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4			Card reader(PCI-E)	Card reader(PCI-E)
7	5				GPU(DIS only)
8					GPU(DIS only)
9					GPU(DIS only)
10					GPU(DIS only)
11	6 L0		3	WLAN	WLAN
12	6 L1		2	ODD	ODD
13	6 L2		1	HDD	HDD
14	6 L3		0	SSD	SSD

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Title: Notes List

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UCPU1 5500@ I7-5500 SA000089A30

UCPU1 5200@ I5-5200 SA000089930

<HDMI>

UCPU1A BDW_ULT_DDR3L(Interleaved)

<20> PCH_DPB_N2 C54 DDI1_TXN0
<20> PCH_DPB_P2 C55 DDI1_TXP0
<20> PCH_DPB_N1 B58 DDI1_TXN1
<20> PCH_DPB_P1 C58 DDI1_TXP1
<20> PCH_DPB_N0 B55 DDI1_TXN2
<20> PCH_DPB_P0 A55 DDI1_TXP2
<20> PCH_DPB_N3 A57 DDI1_TXN3
<20> PCH_DPB_P3 B57 DDI1_TXP3

C51 DDI2_TXN0
C50 DDI2_TXP0
C53 DDI2_TXN1
B53 DDI2_TXP1
C49 DDI2_TXN2
B50 DDI2_TXP2
A53 DDI2_TXN3
B52 DDI2_TXP3

DDI EDP

EDP_TXN0 C45 EDP_CPU_LANE_N0_C <18>
EDP_TXP0 B46 EDP_CPU_LANE_P0_C <18>
EDP_TXN1 A47 EDP_CPU_LANE_N1_C <18>
EDP_TXP1 B47 EDP_CPU_LANE_P1_C <18>
EDP_TXN2 C47 EDP_CPU_LANE_N2_C <18>
EDP_TXP2 C46 EDP_CPU_LANE_P2_C <18>
EDP_TXN3 A49 EDP_CPU_LANE_N3_C <18>
EDP_TXP3 B49 EDP_CPU_LANE_P3_C <18>
EDP_AUXN A45 EDP_CPU_AUX#_C <18>
EDP_AUXP B45 EDP_CPU_AUX_C <18>
EDP_RCOMP D20 EDP_COMP
EDP_DISP_UTIL A43 T22 @

<eDP>

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BDW-ULT-DDR3L-IL_BGA1168
@

COMPENSATION PU FOR eDP
+VCCIOA_OUT
EDP_COMP 2 1 RC3
24.9_0402_1%

DG V2.0 PEG_COMP
Trace width=20mil and spacing=25mil
Max length=100mil

+3V_PCH
RC234 10K_0402_5%

+VCCIO_OUT
RC4 62_0402_5%

UCPU1B BDW_ULT_DDR3L(Interleaved)

PROC_DETECT# D61 PROC_DETECT
@T51 K61 CATERR
N62 PECI
<33> H_PECI

MISC

<33> PROCHOT# PROCHOT RC6 1 2 56_0402_5% H_PROCHOT#_R K63
PROCHOT

THERMAL

@ESD@ C295 10P_0402_50V8J

<6,11> +1.05VS_PG RC7 1 1K_0402_1% @ 2 H_CPUPWRGD_R C61
RC11 2 1 10K_0402_5%
PROCPWRGD

PWR

SM_RCOMP0 AU60 SM_RCOMP0
SM_RCOMP1 AV60 SM_RCOMP1
SM_RCOMP2 AU61 SM_RCOMP2
DDR3_DRAMRST# AV15 SM_DRAMRST
DDR_PG_CNTL AV61 SM_PG_CNTL1

DDR3L

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BDW-ULT-DDR3L-IL_BGA1168
@

JTAG

PRDY J62 XDP_PRDY# T58 @
PREQ K62 XDP_PREQ#
E60 XDP_TCK
PROC_TCK E61 XDP_TMS_CPU XDP_TCK <6>
PROC_TMS E59 XDP_TRST#_CPU
PROC_TRST F63 XDP_TDI_CPU XDP_TRST#_CPU <6>
PROC_TDI F62 XDP_TDO_CPU
PROC_TDO XDP_TDO_CPU <6>

BPM#0 J60 XDP_OBS0_R T80 @
BPM#1 H60 XDP_OBS1_R T79 @
BPM#2 H61 XDP_OBS2_R T52 @
BPM#3 H62 XDP_OBS3_R T53 @
BPM#4 K59 XDP_OBS4_R T54 @
BPM#5 H63 XDP_OBS5_R T55 @
BPM#6 K60 XDP_OBS6_R T56 @
BPM#7 J61 XDP_OBS7_R T57 @

@T86 XDP_TMS_CPU

+1.05VS_VCCST
XDP_TDI_CPU @RC12 2 1 51_0402_1%
XDP_PREQ# @RC13 2 1 51_0402_1%
XDP_TRST#_CPU
1 @ESD@ CC99 2 0.1U_0402_16V7K

DG V2.0 Trace width=12~15 mil
Max length=500mil

DDR3 COMPENSATION SIGNALS

200_0402_1% 2 1 RC18 SM_RCOMP0
120_0402_1% 2 1 RC19 SM_RCOMP1
100_0402_1% 2 1 RC20 SM_RCOMP2

+1.35V_VDDQ
RC308 470_0402_5%
DDR3_DRAMRST# DDR3_DRAMRST# <15,16>
@ESD@ CC88 0.1U_0402_16V7K

+1.35V_VDDQ
UC10
5 VCC NC 1
A 2 DDR_PG_CNTL
<15> SM_PG_CTRL 4 Y
GND 3
74AUP1G07GW_TSSOP5

+1.35V_VDDQ
@ESD@ CC130 0.1U_0402_16V7K

2015/02/13 ESD reserve for cocoa

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDI,MSIC,XDP

Size	Document Number	Rev
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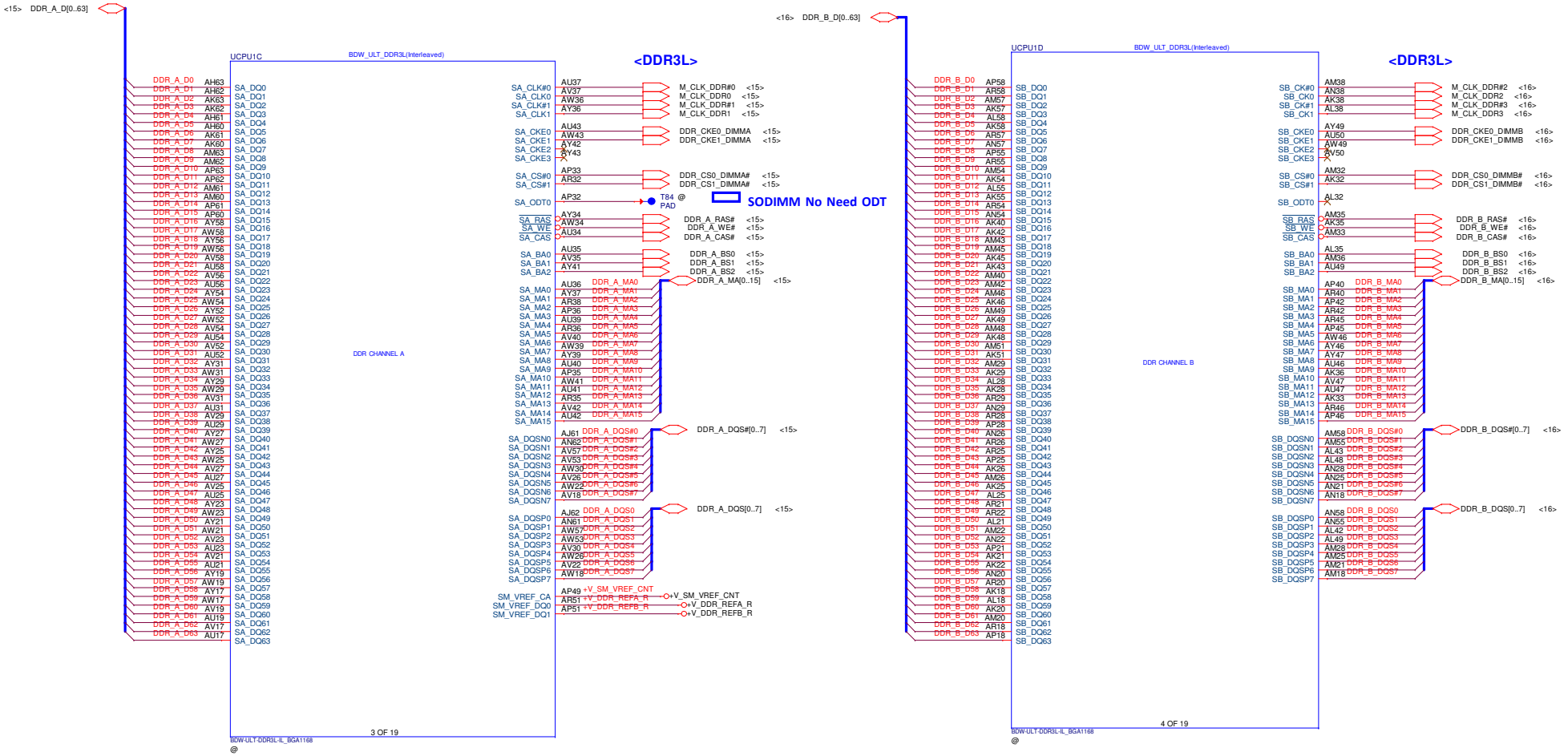
Interleaved Memory



Interleaved Memory

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: DDRIII			
Size: Custom	Document Number: LA-C501P		Rev: 1.0
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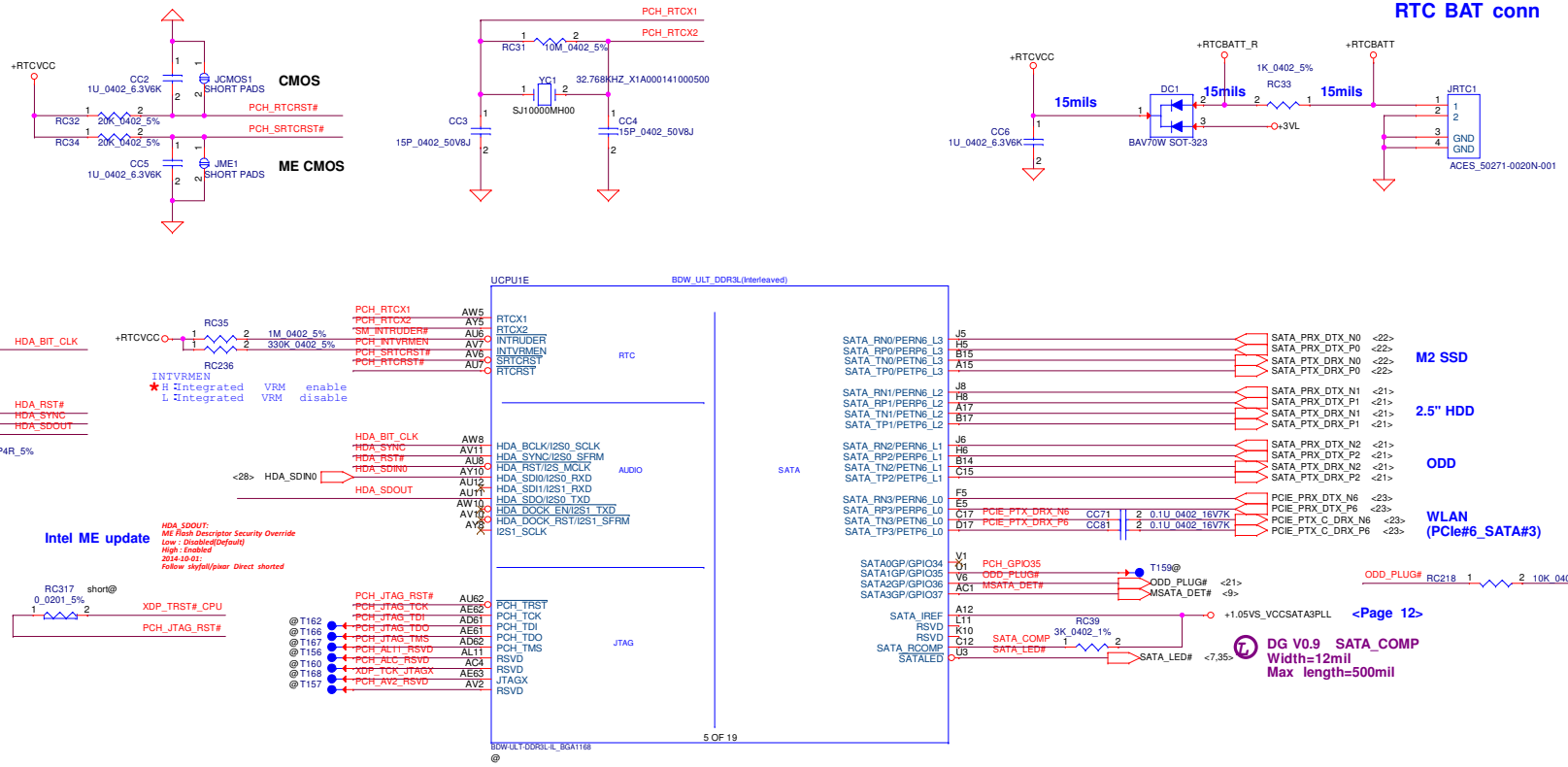
RTC BAT conn



Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: RTC,SATA,HDA,JTAG

Size	Document Number	Rev
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Intel #521772 : PCICLKRQ_Usage_Guidelines
Mapping
– Each PCIECLKRQn# needs to be routed to PCIE Port (n+1) – New to LPT-LP and what is not clear in EDS. Updated in LPT-LP EDS SU Rev1.5.1 (#508767).
– Each CLKOUT_PCIE[5:0] can be assigned to any PCIECLKRQn#

LAN(PCIe#3)

CardReader(PCIe#4)

GPU(PCIe#5)

WLAN(PCIe#6_SATA#3)

UCPU1F BDW_ULT_DDR3L(Interleaved)

CLOCK SIGNALS

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BDW-ULT-DDR3L-IL_BGA1168

UCPU1G BDW_ULT_DDR3L(Interleaved)

LPC SMBUS SPI C-LINK

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BDW-ULT-DDR3L-IL_BGA1168

<Page12>

<EC>

<XDP CLK reserve TP>

9/17 add RF solution

2014-09-29: Change GPU_CLKREQ# PU to +3VS on CPU side. Remove GPU side RG8

2014-09-29: Change USB_CR_PWREN to SMK0ALERT#

SPI ROM 8M

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESEC0F SO8W 8P

GD25B64BSIGR

CPU THERMAL SENSOR

Thermal sensor SMBus address -->100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)

NCT7718W_MSOP8
SA0000067P00

Thermal sensor SMBus address -->0111_100xb (0x78h)

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Title: CLK,SPI,SMB,LPC

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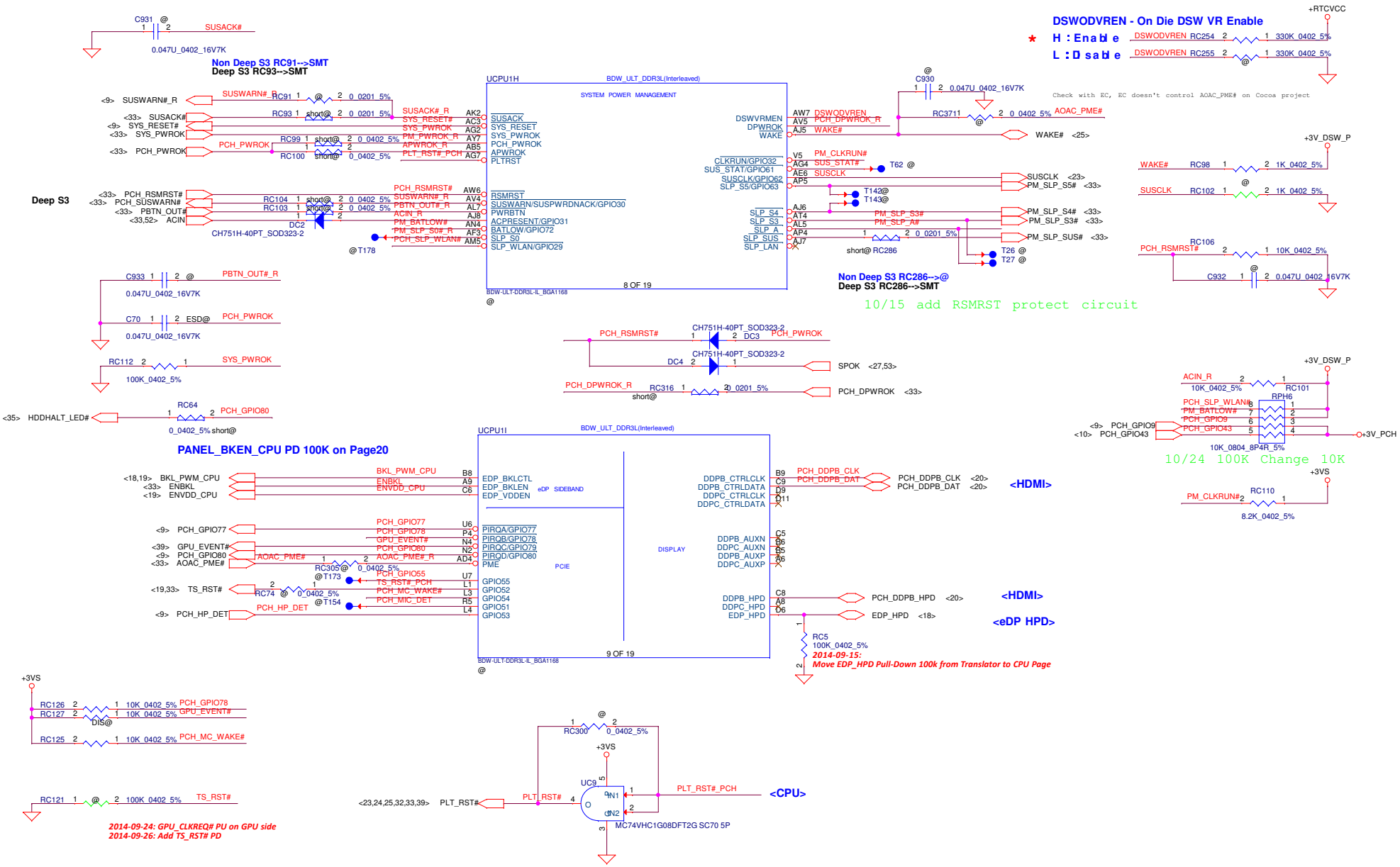

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: PM,GPIO,DDI			
Size: Custom	Document Number: LA-C501P		Rev: 1.0
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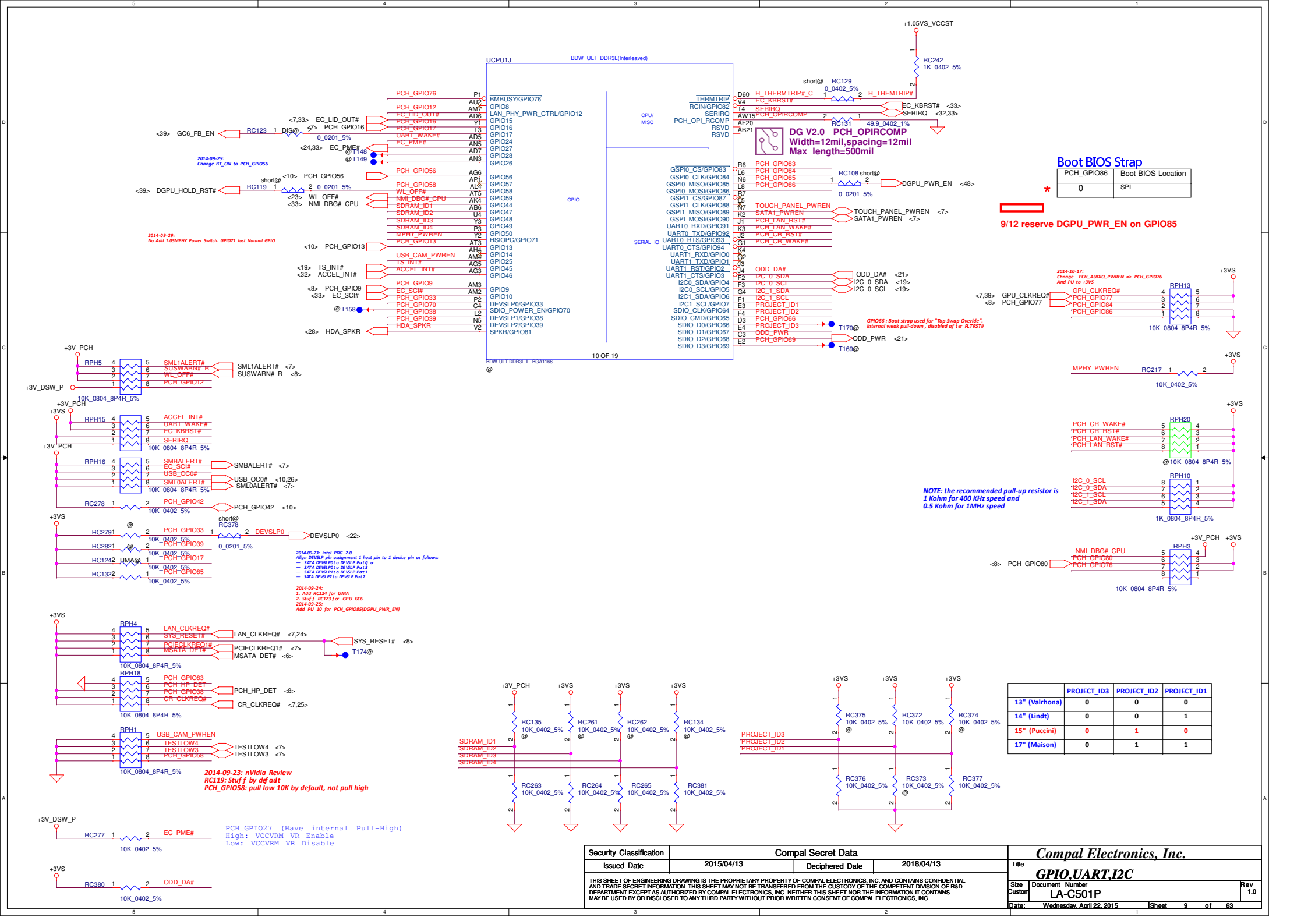

	PROJECT_ID3	PROJECT_ID2	PROJECT_ID1
13" (Valrhona)	0	0	0
14" (Lindt)	0	0	1
15" (Puccini)	0	1	0
17" (Maison)	0	1	1

Compal Electronics, Inc.

Title: GPIO,UART,I2C

Size: Custom | Document Number: LA-C501P | Rev: 1.0

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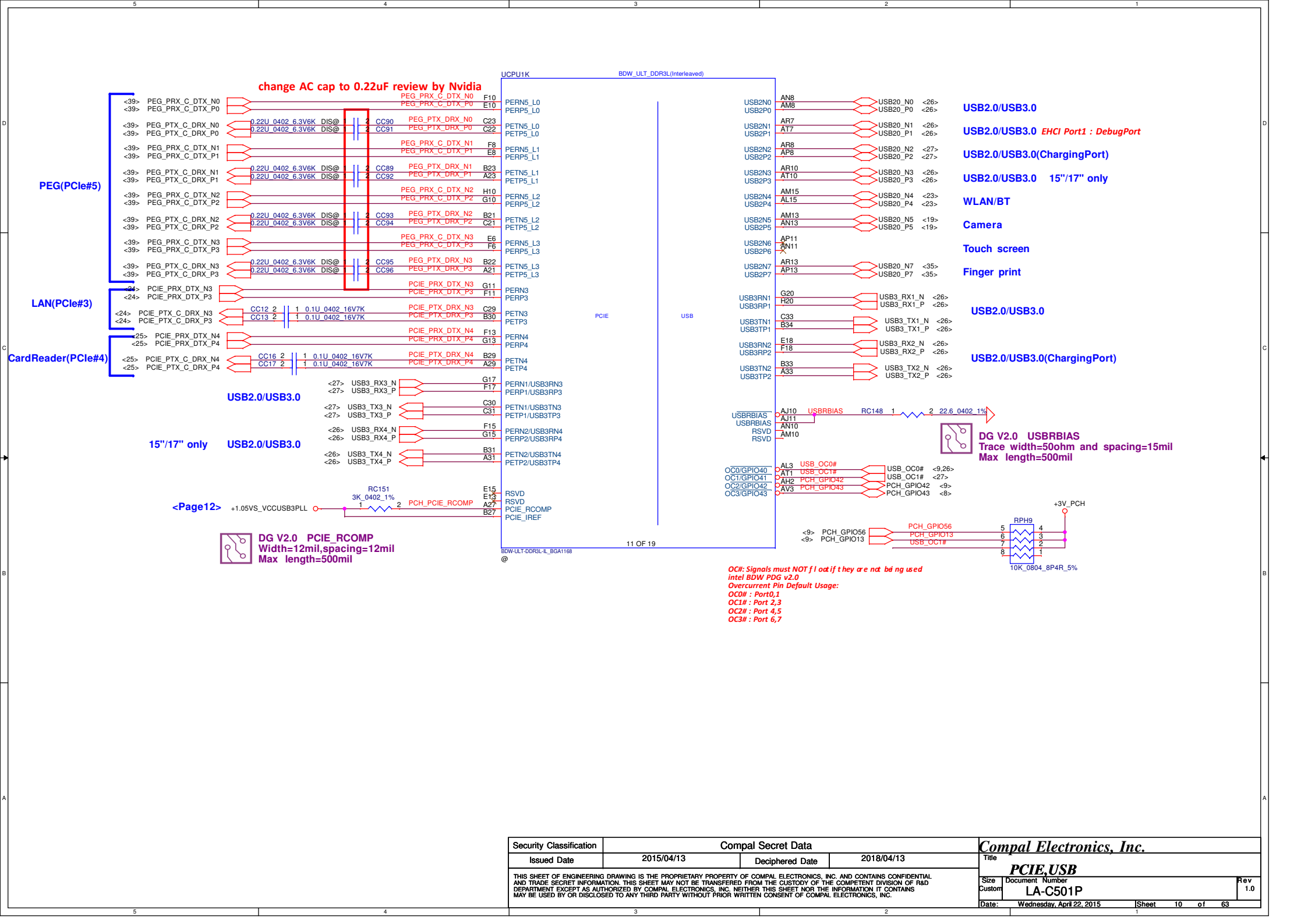

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: PCIE,USB

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+VCC_CORE@10000mA

SVID ALERT

<PWR VR12.6> <56> VR_SVID_ALRT# — RC1551 43_0402_1% — H_CPU_SVIDALRT#

+1.05VS_VCCST — RC154 75_0402_5% — H_CPU_SVIDALRT#

DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000~2000mil

SVID DATA

<PWR VR12.6> <56> VR_SVID_DAT — VR_SVID_DAT

+1.05VS_VCCST — RC156 130_0402_1% — VR_SVID_DAT

VCC_SENSE

<PWR VR12.6>

PH on power page

<56> VCCSENSE — VCCSENSE

<VR IV and CPU>
<EDP_COMP power rail>

+VCCIO_OUT
+VCCIOA_OUT

<56> VR_SVID_CLK — VR_SVID_CLK
VR_SVID_DAT

<56> VGATE — VGATE — RC87 short@ — <56> VR12.5_VR_ON — 0_0402_5%

<4,6> +1.05VS_PG — VR12.6PG_MCP

CPU_PWR_DEBUG

2014-09-23:
1.Follow intel VR12.6 and skyfall H5W
2.Remove UC8(74AUP1G07GW Buf f er) and RC288(10k)
3.Need to make sure VGATE is Pull-High 1.5kohm to VR_ON

+VCCIO_OUT — RC294 @ 0_0402_5% — +1.05VS

DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil

UCPU1L — BDW_ULT_DDR3L(Interleaved)

+1.35V_VDDQ — 2500mA

+VCC_CORE — 600mA

HSW ULT POWER

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BDW-ULT-DDR3L-IL_BGA1168

+1.05VS_VCCST — RC166 150_0402_5% — CPU_PWR_DEBUG — RC167 10K_0402_5%

+1.05VS — RC2231 short@ 0_0805_5% — +1.05VS_VCCST

CC71 22U_0805_6.3V6M — CC72 1U_0402_6.3V6K

+1.35V_VDDQ — CC20 2.2U_0402_6.3V6M — CC21 2.2U_0402_6.3V6M — CC22 2.2U_0402_6.3V6M — CC23 2.2U_0402_6.3V6M

<PV> Reserve CC24

+1.35V_VDDQ — CC24 330U_2V_D2_LESR9ME_EFSX_H1.9 — SGA20331E10

CC26 10U_0603_6.3V6M — CC27 10U_0603_6.3V6M — CC28 10U_0603_6.3V6M — CC29 10U_0603_6.3V6M — CC30 10U_0603_6.3V6M — CC31 10U_0603_6.3V6M

<Cocoa> Del reserve CC25 330u OSCON cap

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Power

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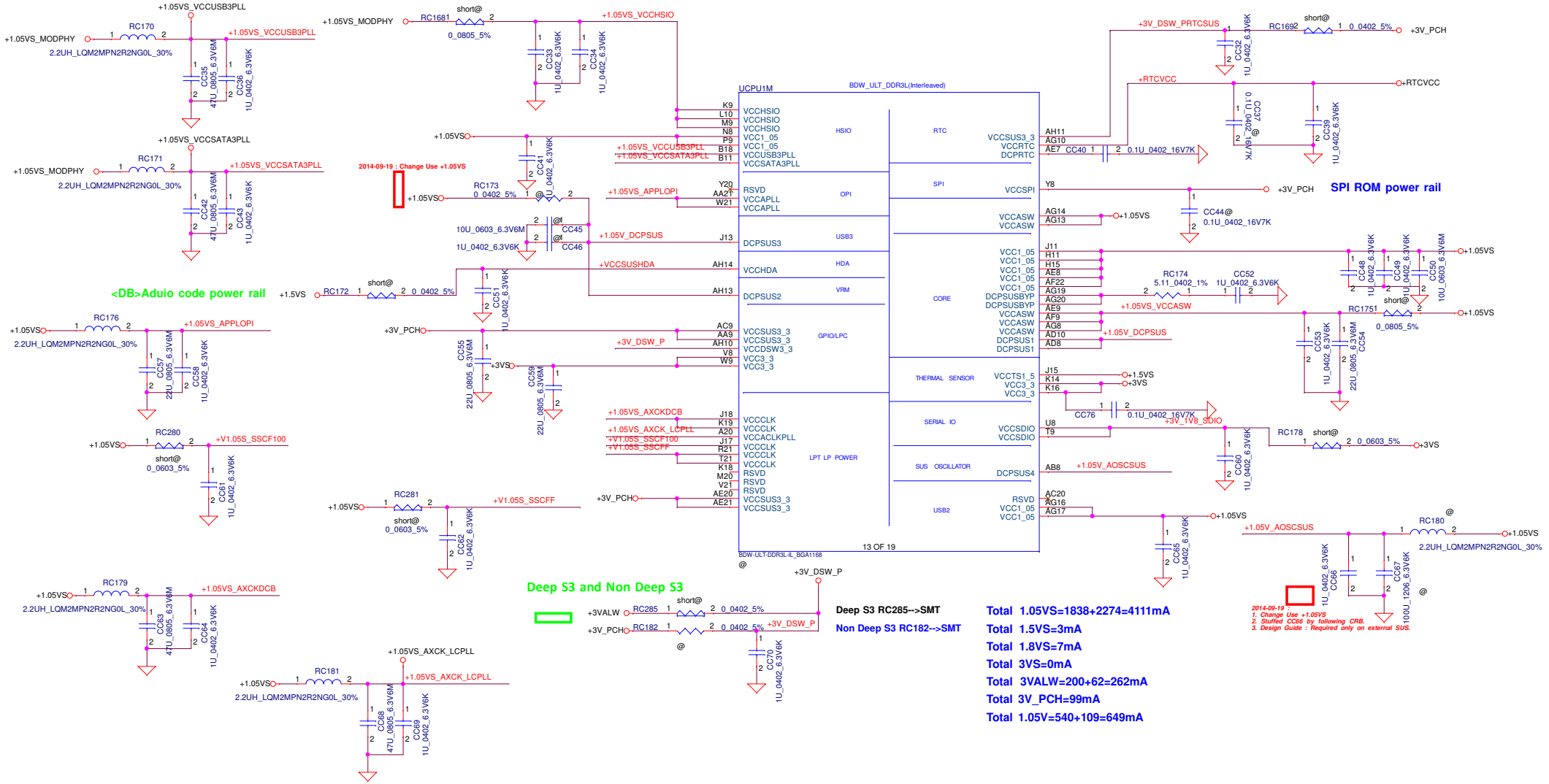

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **Power**

Size	Document Number	Rev
Custom	LA-C501P	1.0

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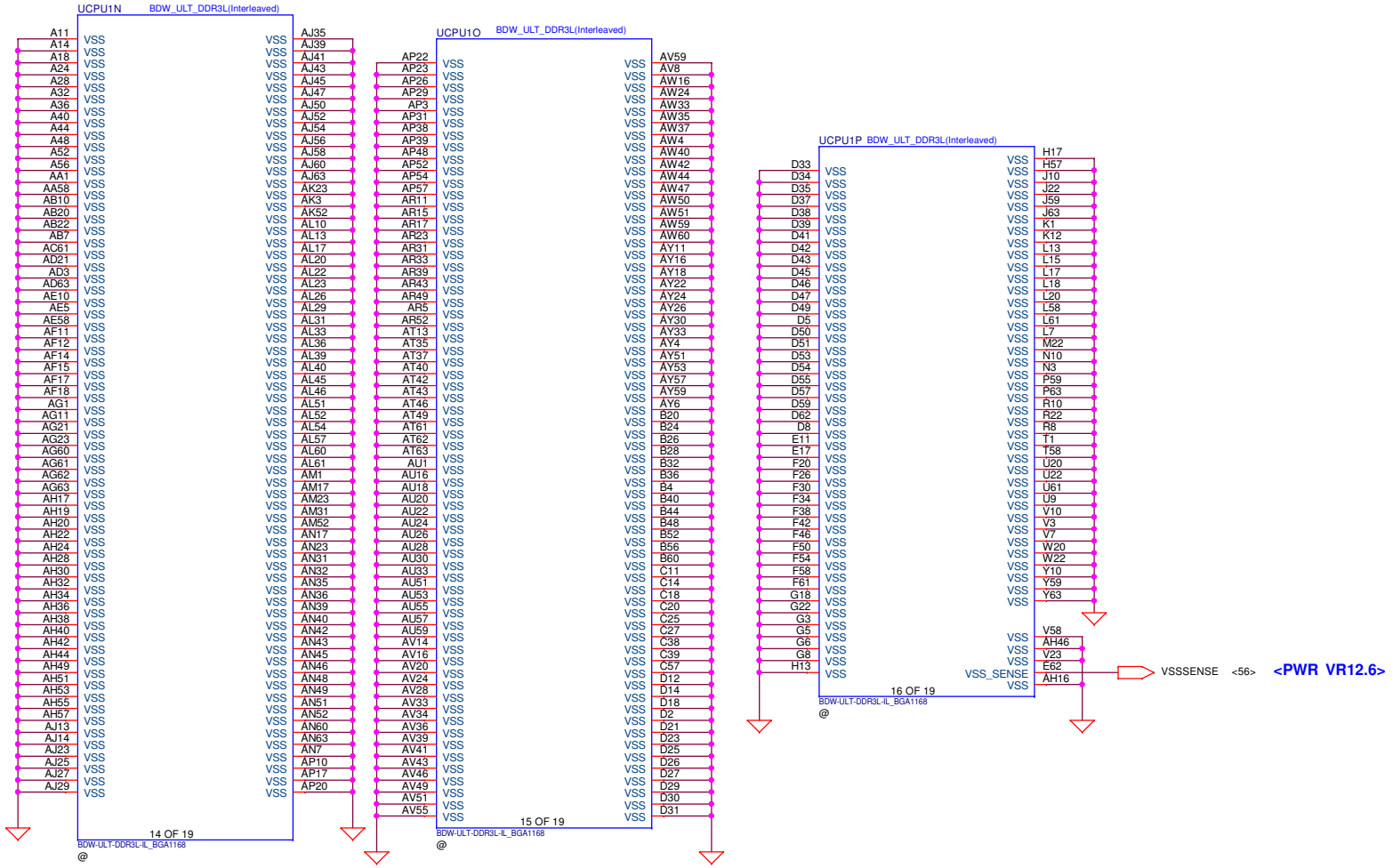

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: GND/VSSSEN

Size	Document Number	Rev
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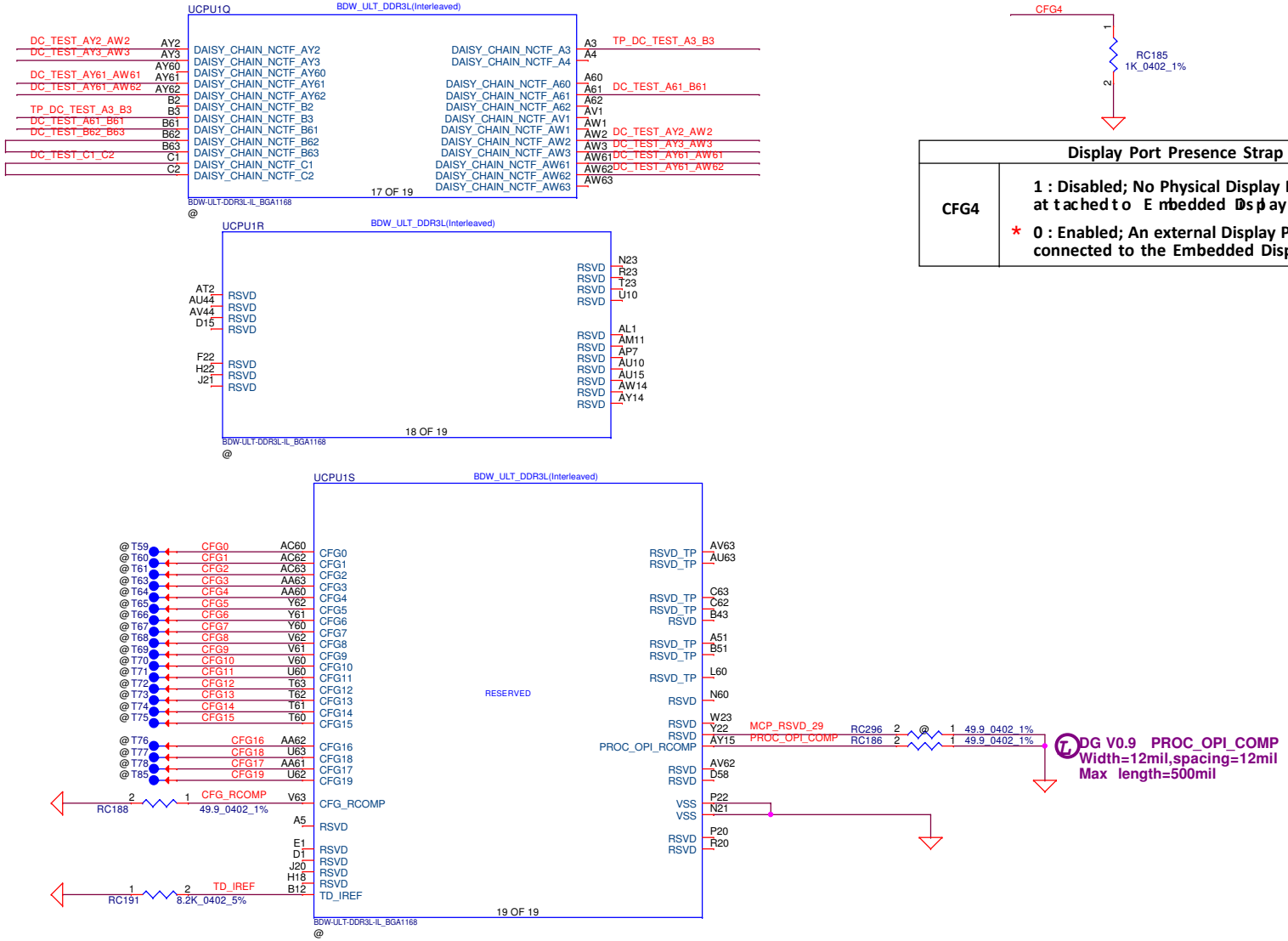

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Compal Electronics, Inc.

Title: RSVD/CFG

Size	Document Number	Rev
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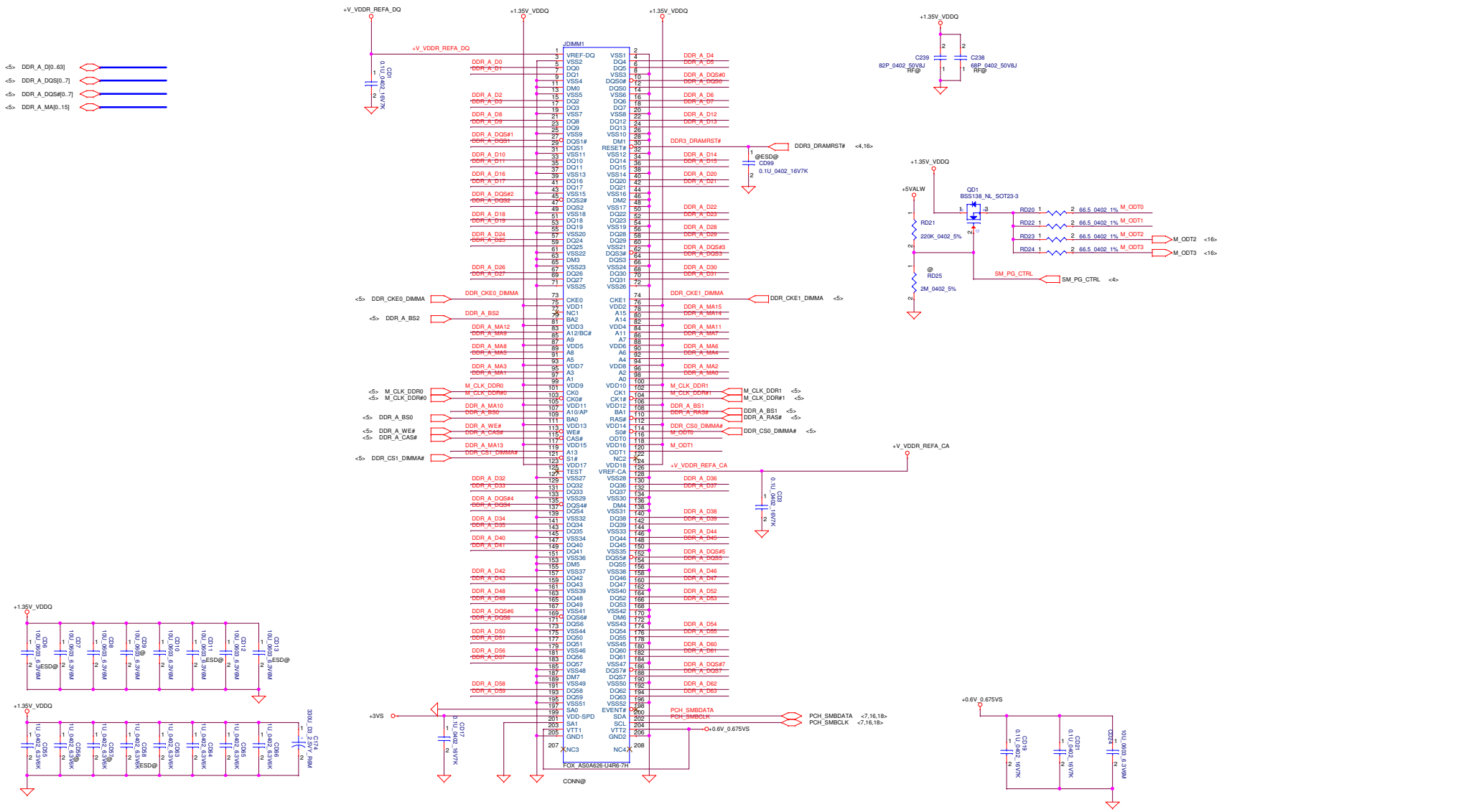

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: DDR3L DIMM0

Size	Document Number	Rev
	LA-C501P	1.0

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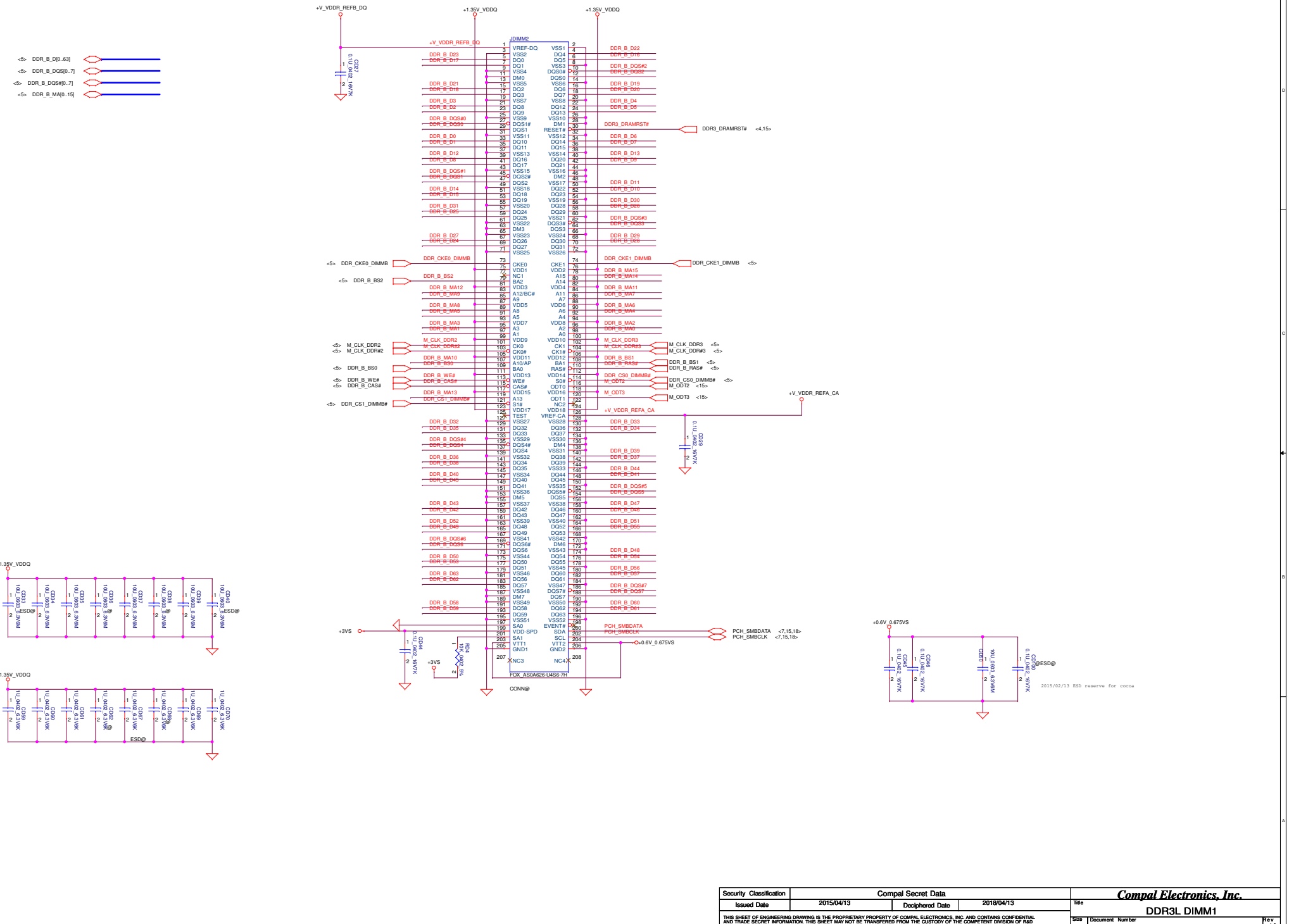

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: DDR3L DIMM1

Size	Document Number	Rev
	LA-C501P	1.0

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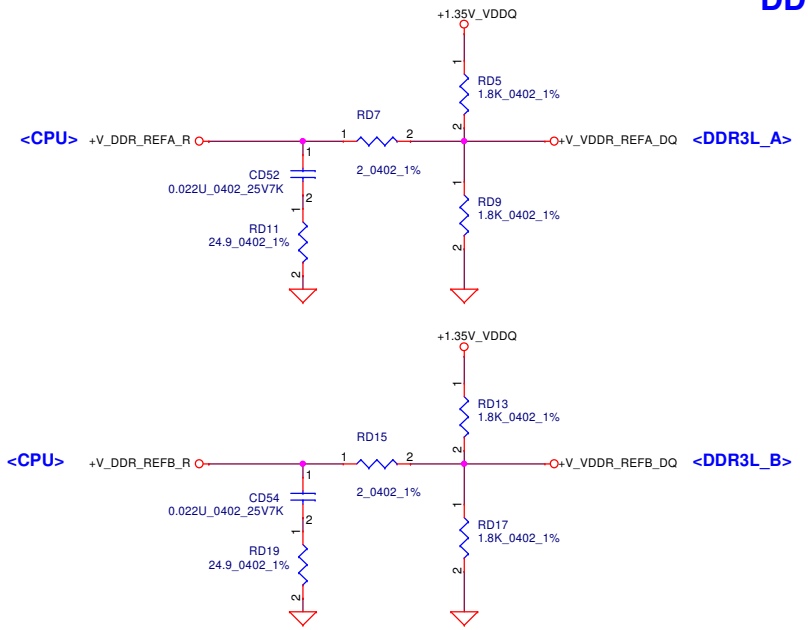
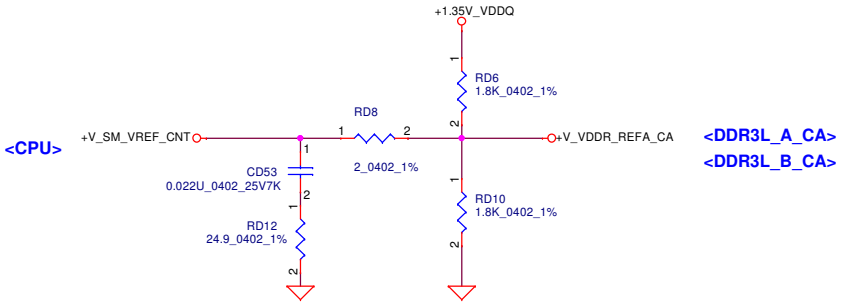
DDR3L VREF





Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: DDR3L VREF			
Size	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 17 of 63		

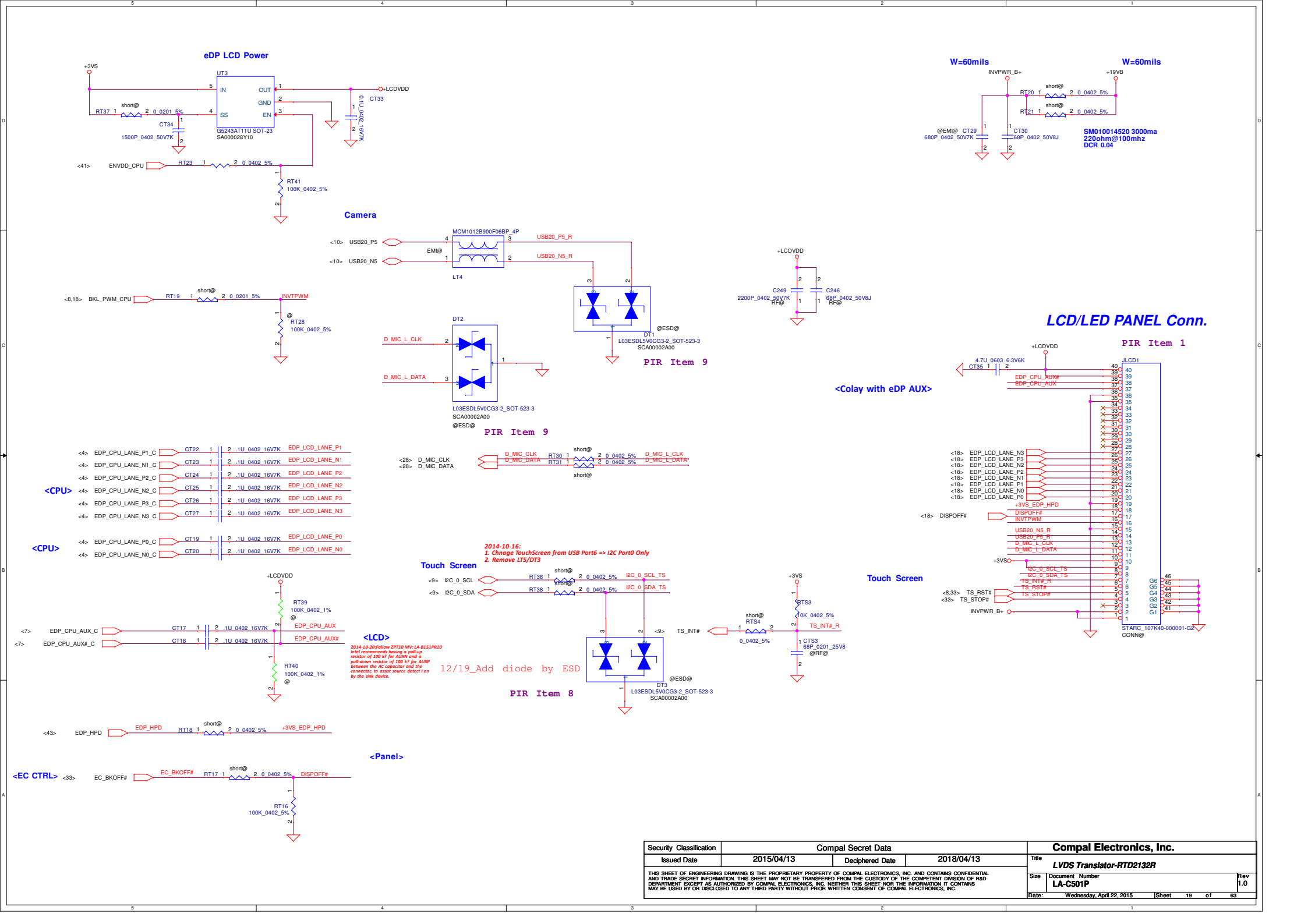
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: ***LVDS Translator-RTD2132R***

Size	Document Number	Rev
	LA-C501P	1.0

Date: Wednesday, April 22, 2015 | Sheet 18 of 63



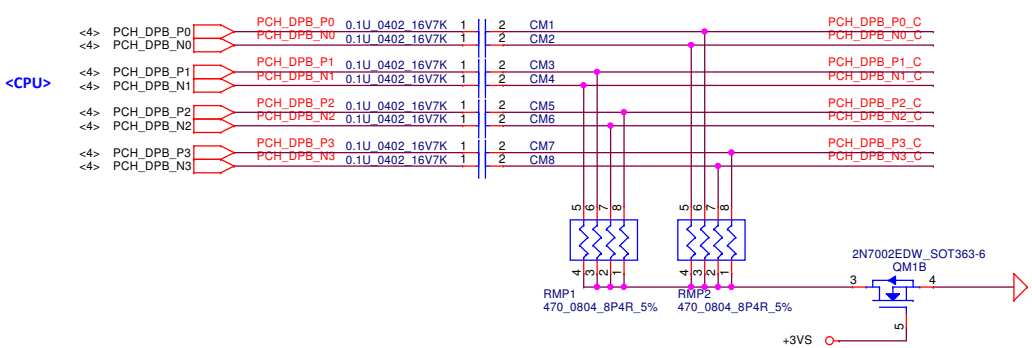
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

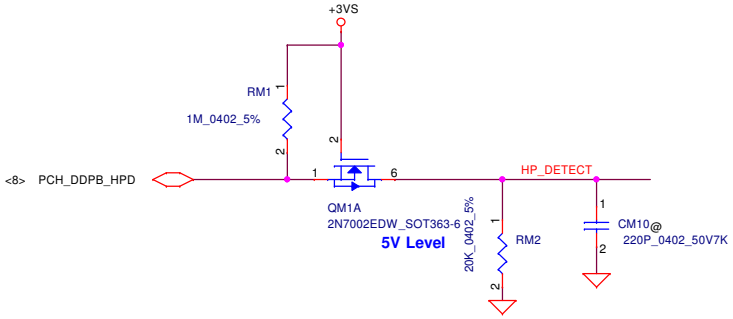
Compal Electronics, Inc.

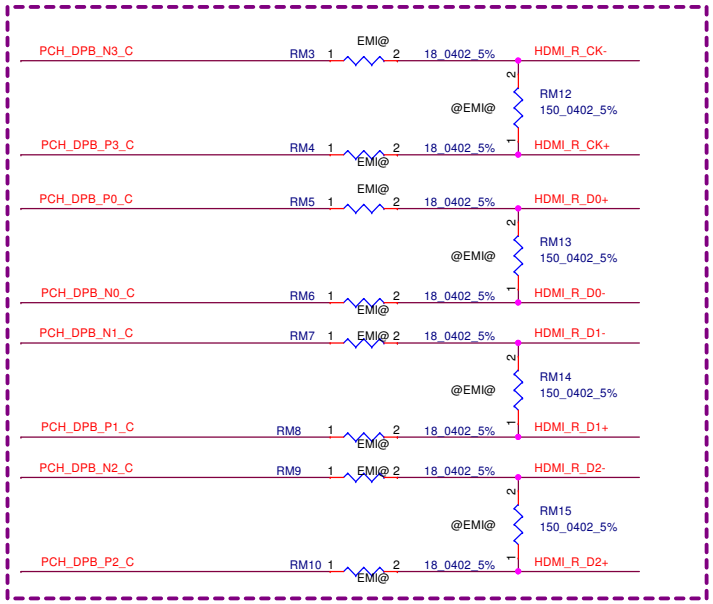
Title: *LVDS Translator-RTD2132R*

Size	Document Number	Rev
	LA-C501P	1.0

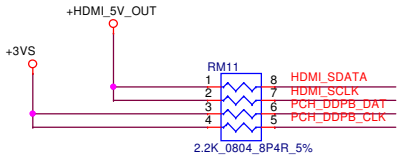
Date: Wednesday, April 22, 2015 | Sheet 19 of 63

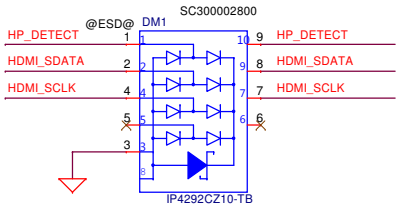


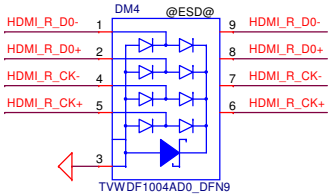


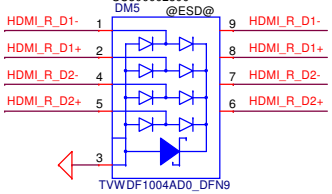


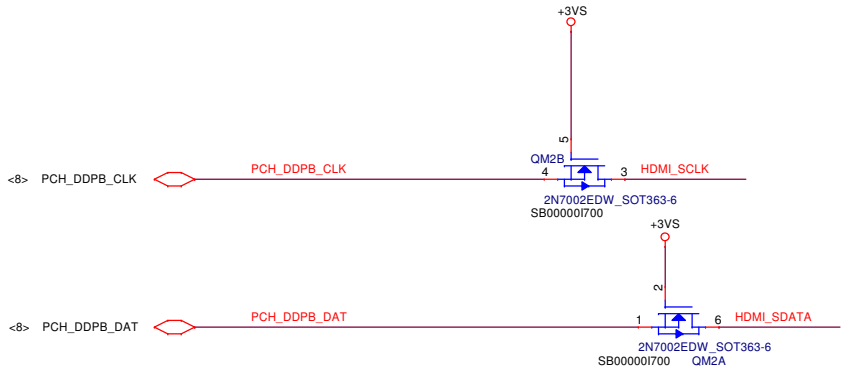
PIR Item 14

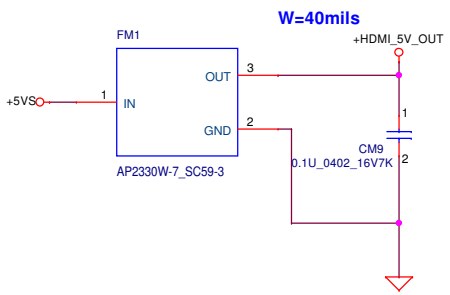




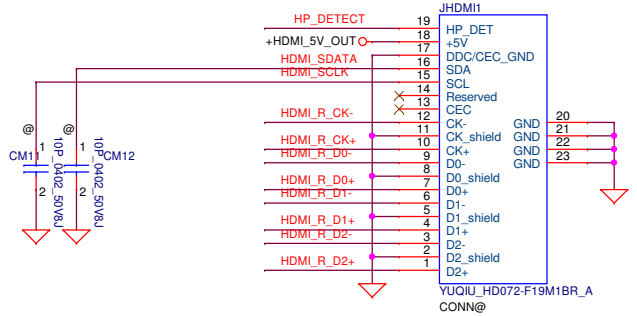








HDMI Conn.



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: HDMI_Conn/Level shift

Size	Document Number	Rev
	LA-C501P	1.0

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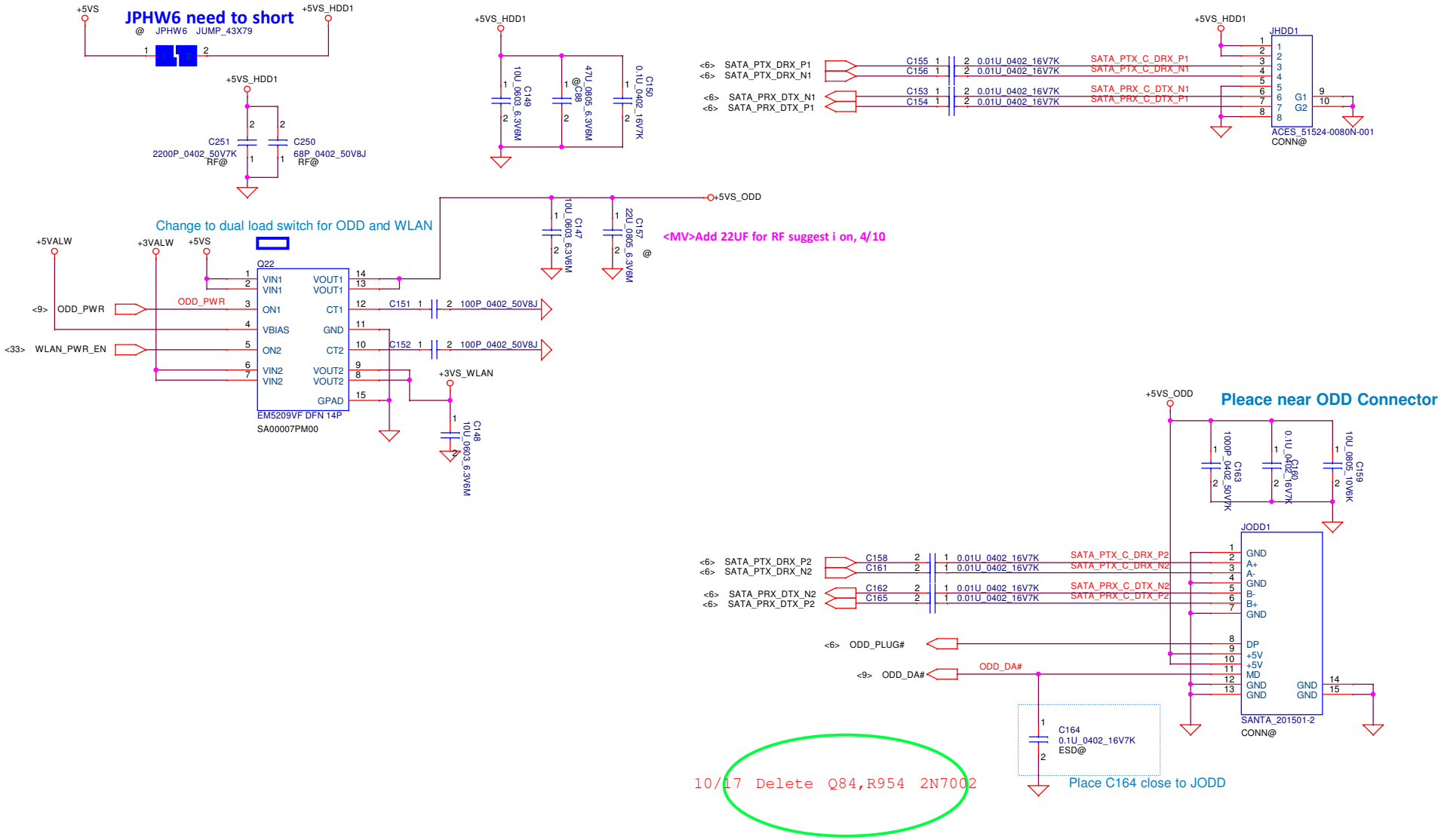


Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

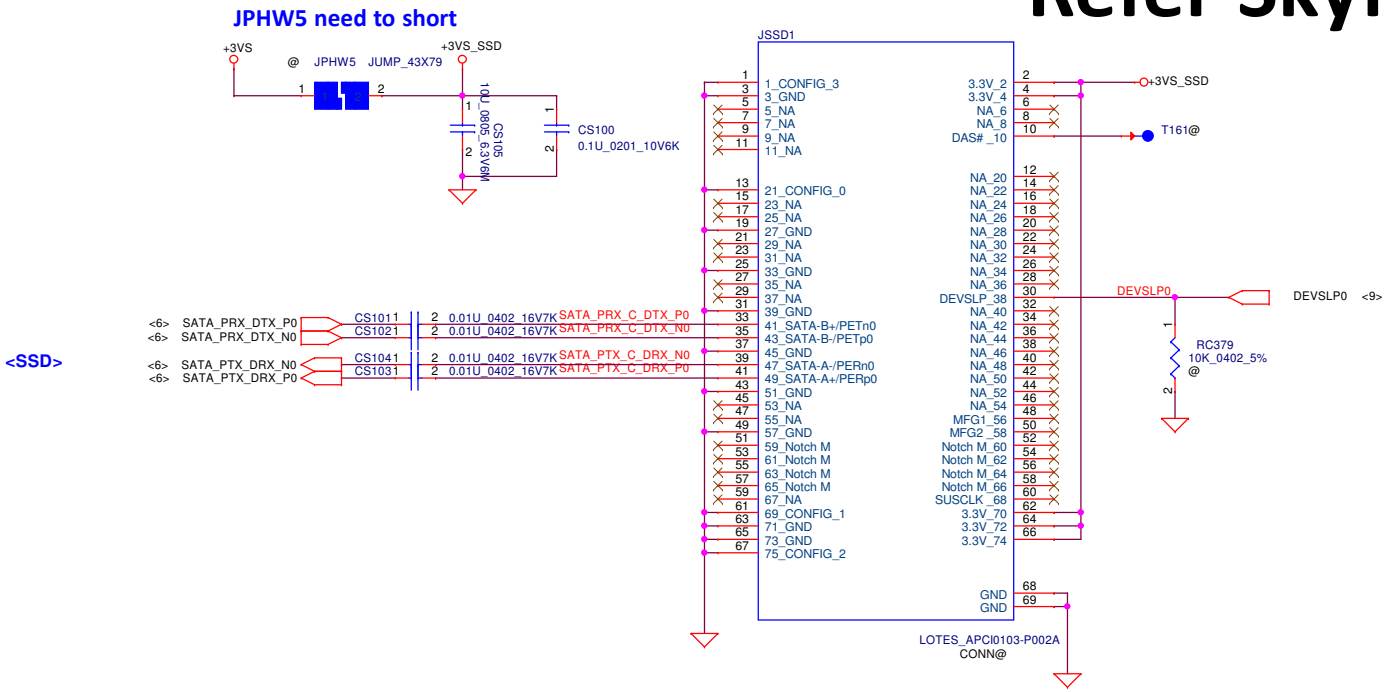
Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 21 of 63

Refer Skyfall test board



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

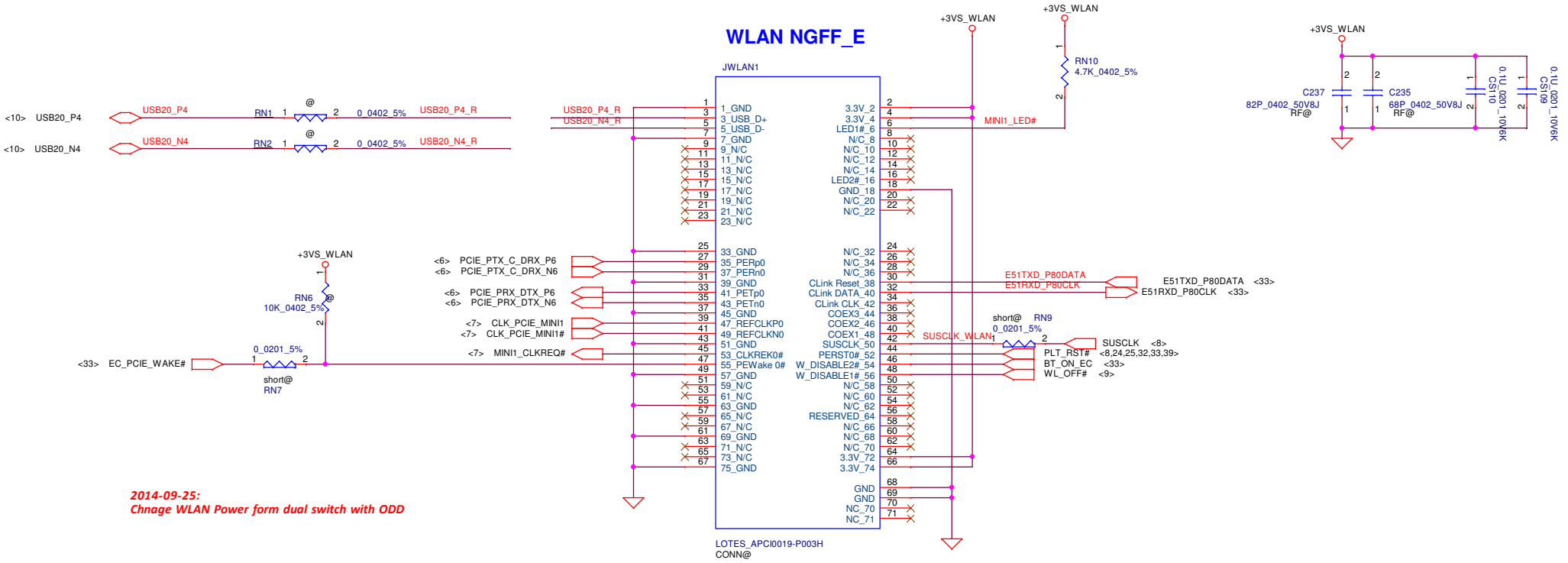
Compal Electronics, Inc.

Title: eDP to CRT

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 22 of 63

Refer Skyfall NGFF



2014-09-25:
Chnage WLAN Power form dual switch with ODD

WLAN
NGFF Key_E 67P P0.5 CH 0.32 H2.2 STD

Del +1.5VS_WLAN

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: WLAN			
Size	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 23 of 63		

JHW1 need to short

+LAN_VDD_3V3 Rising t i me need>0.5mS and <100mS

RTL8111HSH-CG=> Switching Regulator Only

Place Note :
CL12&CL13 close UL1 Pin 3,8
CL14 & CL15 close UL1_Pin22
CL26 & CL27 close UL1_Pin30

Place CL11~CL13 close UL1 Pin 3, 8 , 22

LL2, CL8, CL23 for 8161
CL8 & CL123 close LL2

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

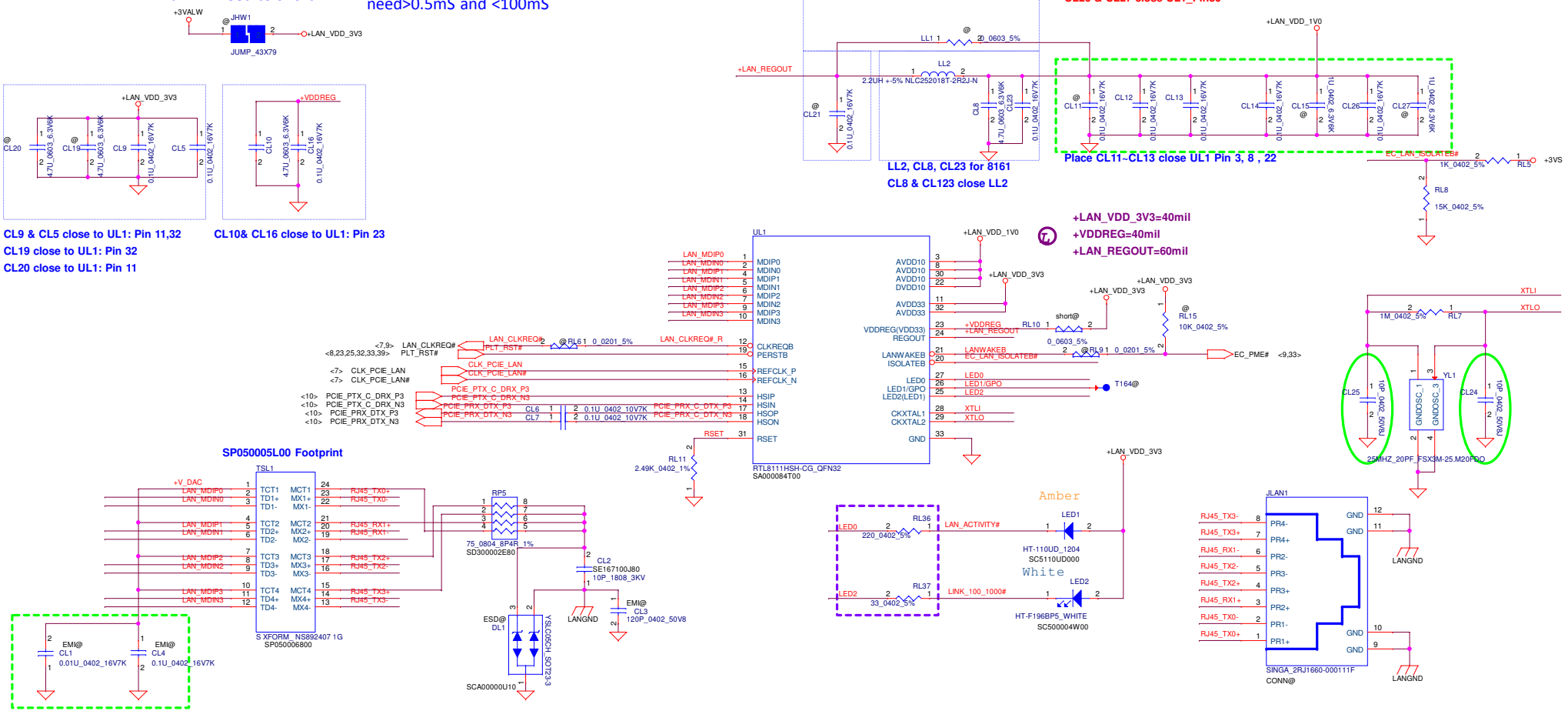
CL10& CL16 close to UL1: Pin 23

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

SP050005L00 Footprint

Amber

White



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

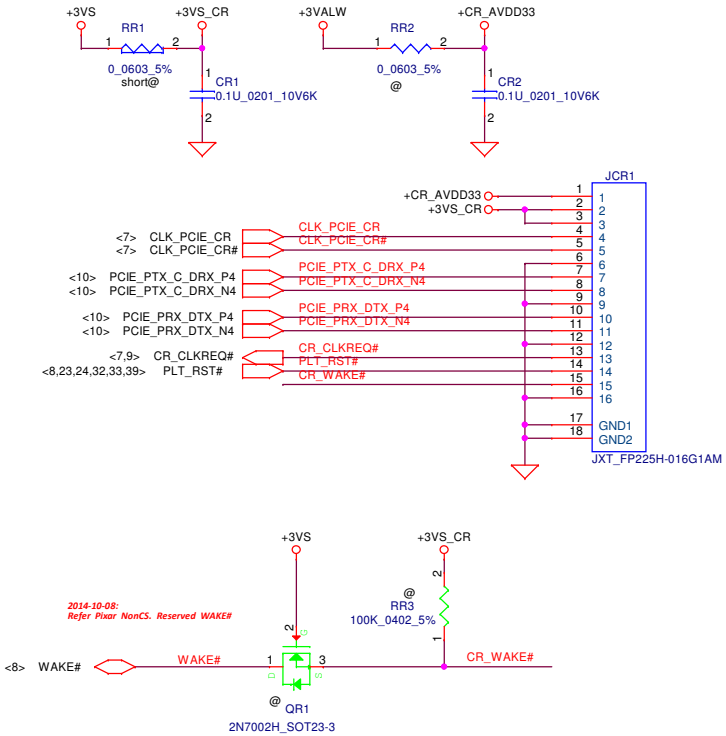
Compal Electronics, Inc.

Title: LAN 8111G

Size	Document Number	Rev
	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 24 of 63

CardReader on Suboard



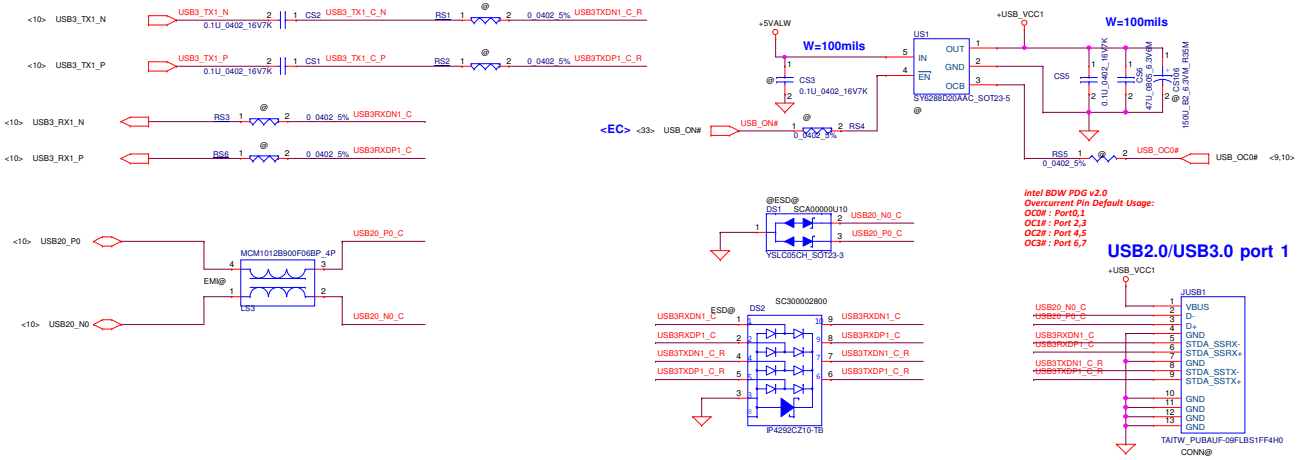
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

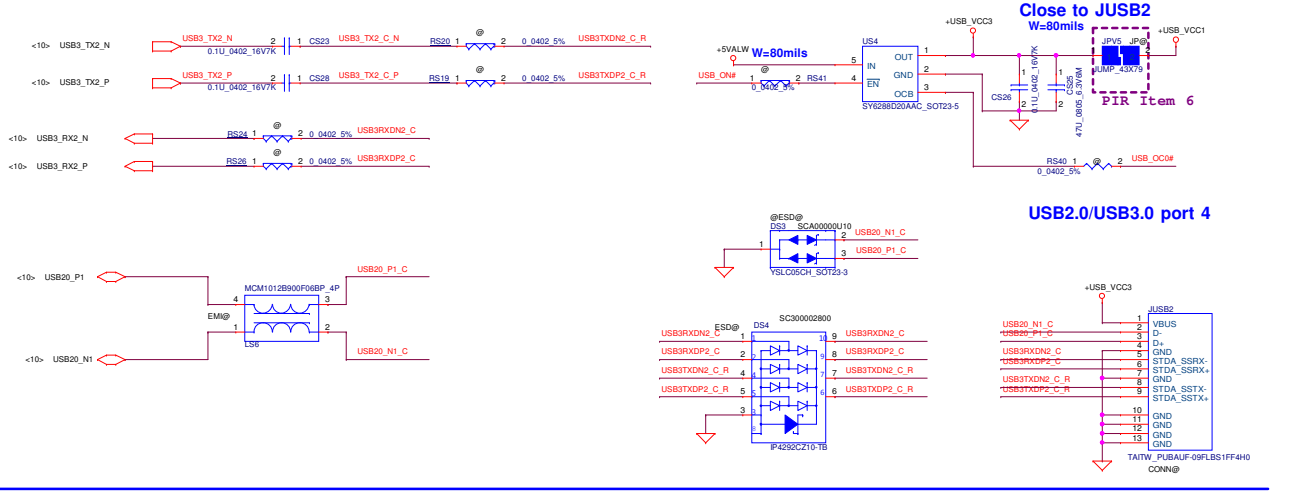
Title: **Card Reader_RTS5237S-CG**

Size	Document Number	Rev
	LA-C501P	1.0

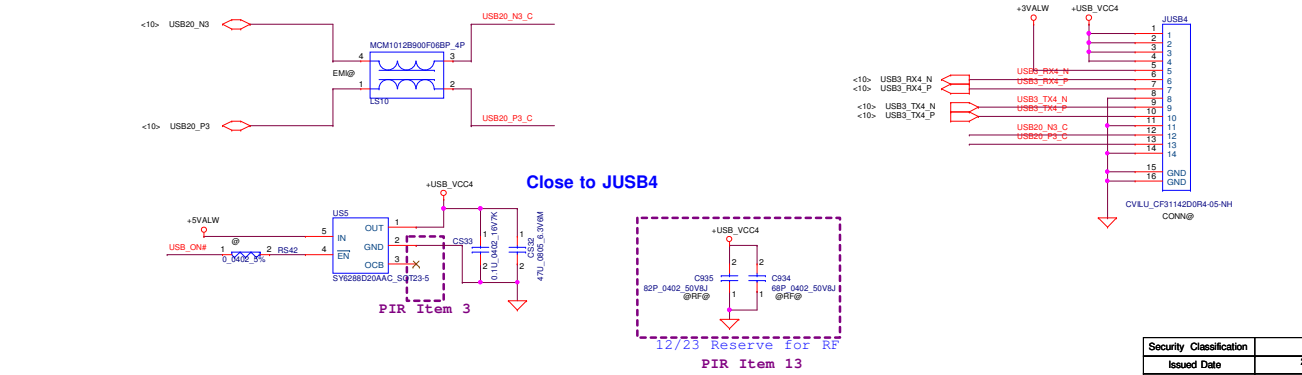
Date: Wednesday, April 22, 2015 | Sheet 25 of 63



EHCI Port1 : DebugPort



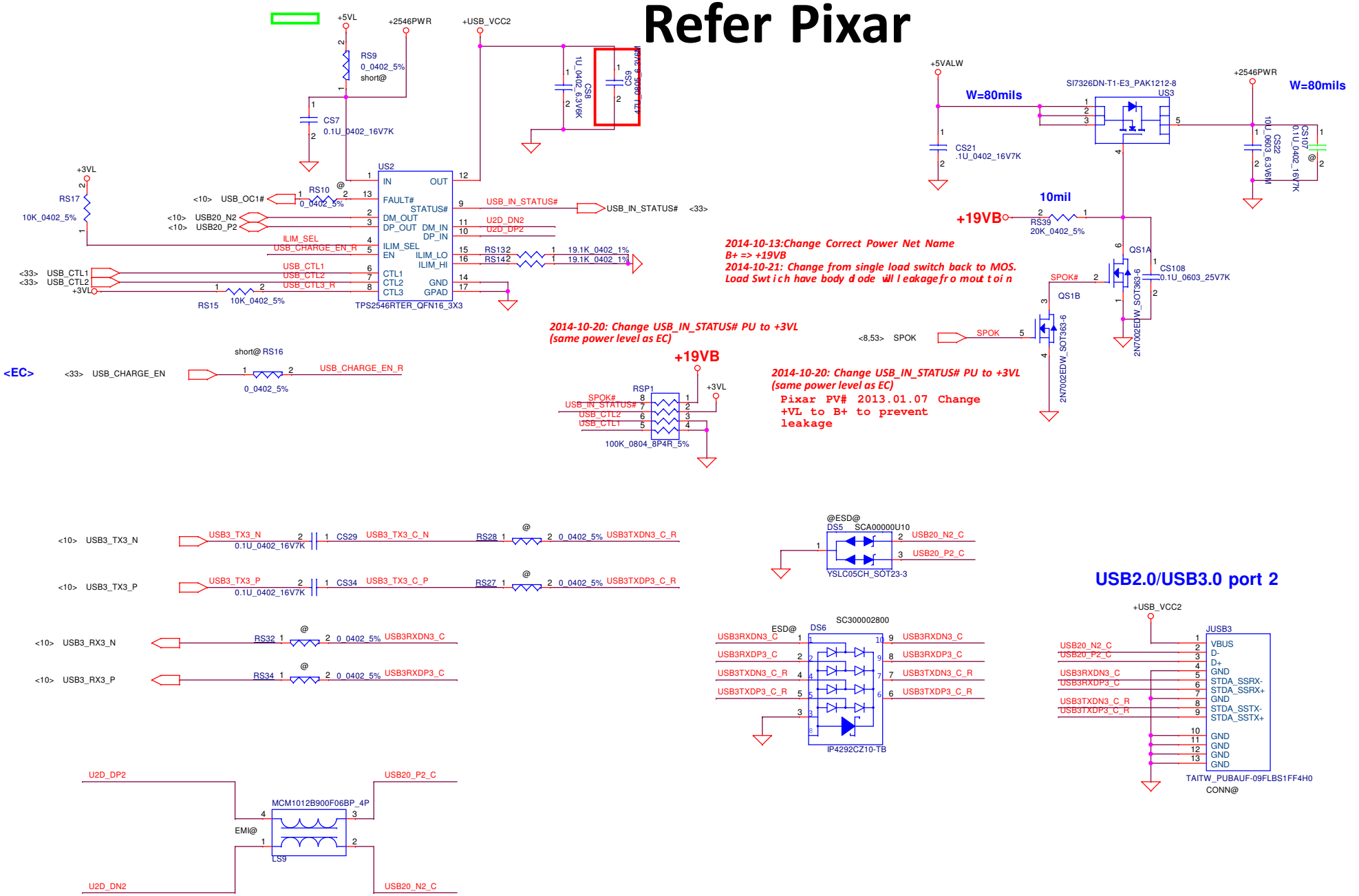
IO Suboard



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.	
Title	USB 3.0/2.0 conn
Size	Document Number: LA-C501P
Rev	1.0
Date:	Wednesday, April 22, 2015
Sheet	26 of 63

Refer Pixar



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/04/13	Deciphered Date 2018/04/13	Title: USB Charger
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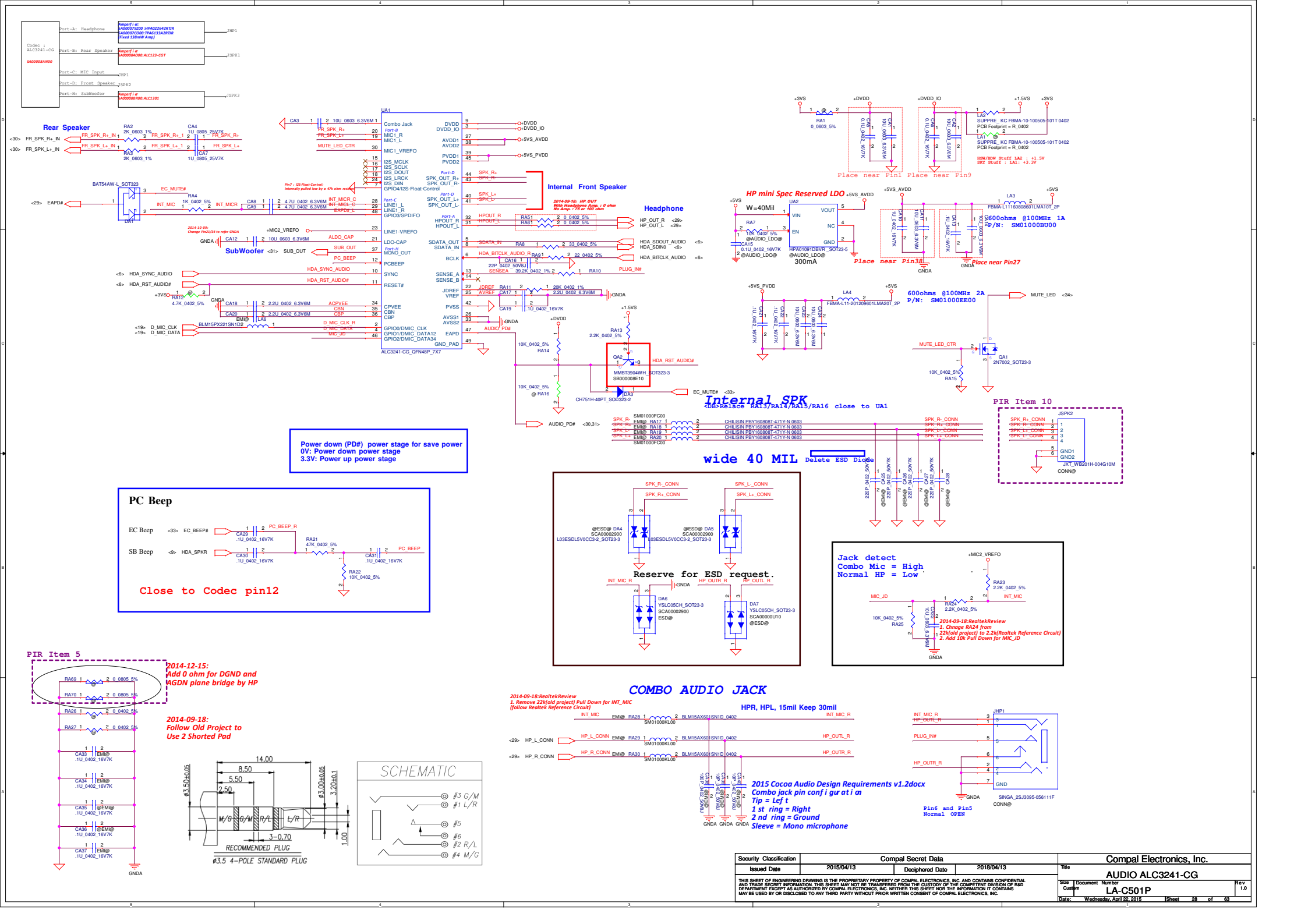
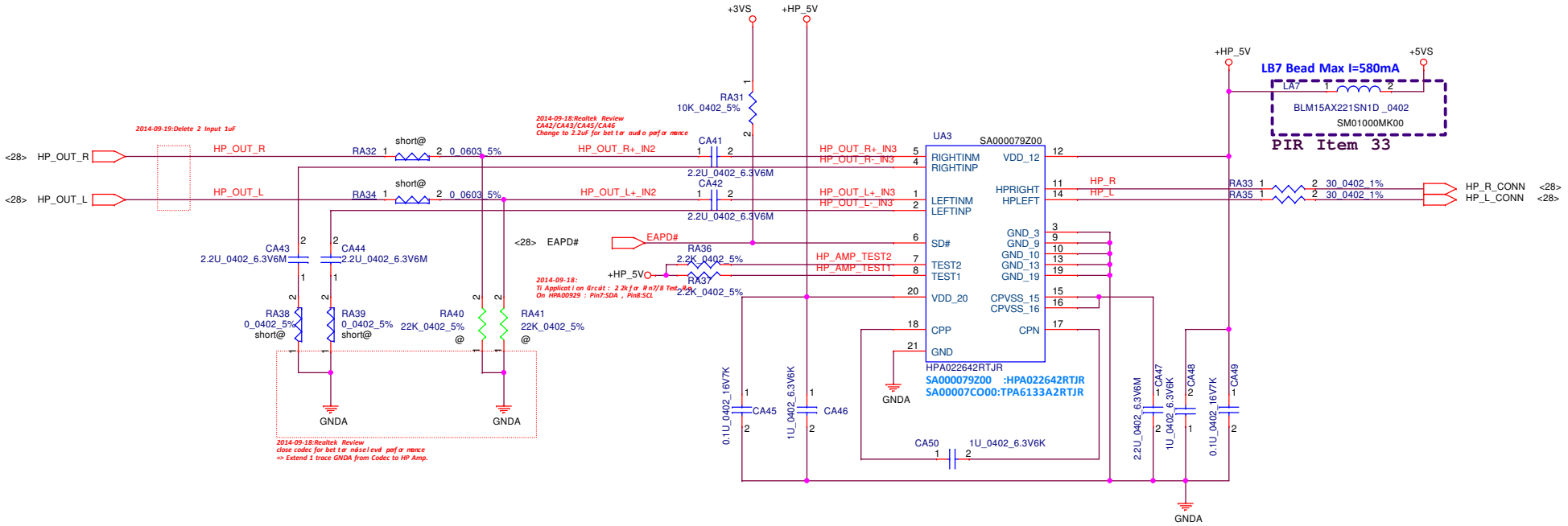
			Date: Wednesday, April 22, 2015; Sheet 27 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.	
Title	AUDIO ALC3241-CG
Size / Document Number	LA-C501P
Custom	Rev 1.0
Date: Wednesday, April 22, 2015	Sheet 28 of 63



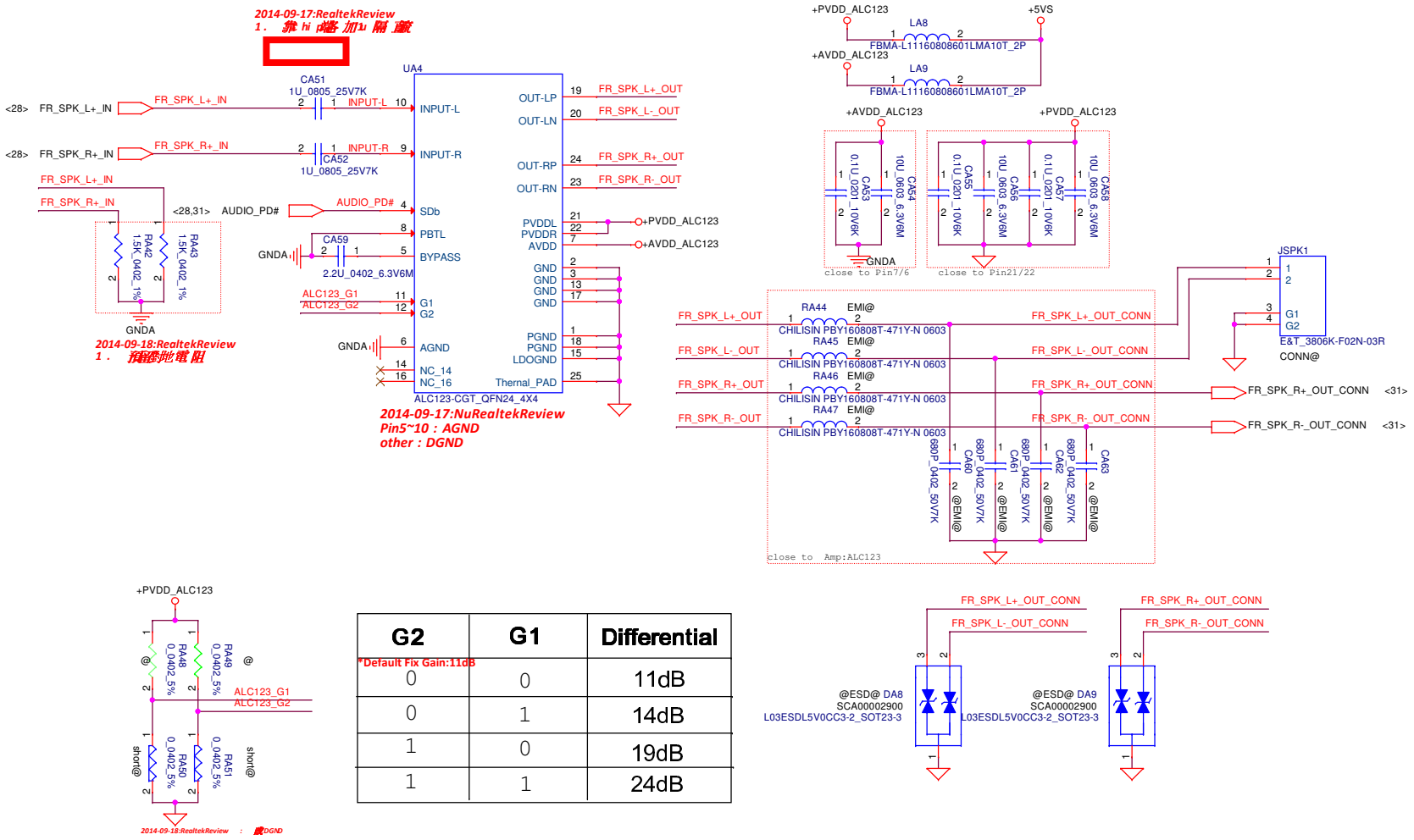
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: Audio HP Amp

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 29 of 63



G2	G1	Differential
*Default Fix Gain:11dB		
0	0	11dB
0	1	14dB
1	0	19dB
1	1	24dB

Compal Electronics, Inc.

Title: Audio Front Speaker Amp:ALC123-CGT

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 30 of 63

2014-10-13:Change Correct Power Net Name
B+ => +19VB +19VB : 9V~19.5V

2014-10-14:Realtek Review
Change all ALC1301 refer to DGND. Only Input Refer to AGND from Codec

2014-10-15:RealtekReview
1. Add RA65/RA66:10kohm for fine tune output speaker 4 W8ohm
2. Change CA64 from 1uF to 4.7uF

PIR Item 11

PIR Item 18

PIR Item 11

PIR Item 18

ALC1301-CGT_QFN48_6X6

2014-10-15:
Change CA69/70/81/83 from 1000pF to 10uF

+19VB

2014-10-15:
Change 2x220uF to 6x22uF
Need Realtek Confir m

Close to Pin44
Close to Pin2
Close to Pin41
Close to Pin35
Close to Pin30

Close to Amp Output

LB12 LB13 Bead Max I=2A

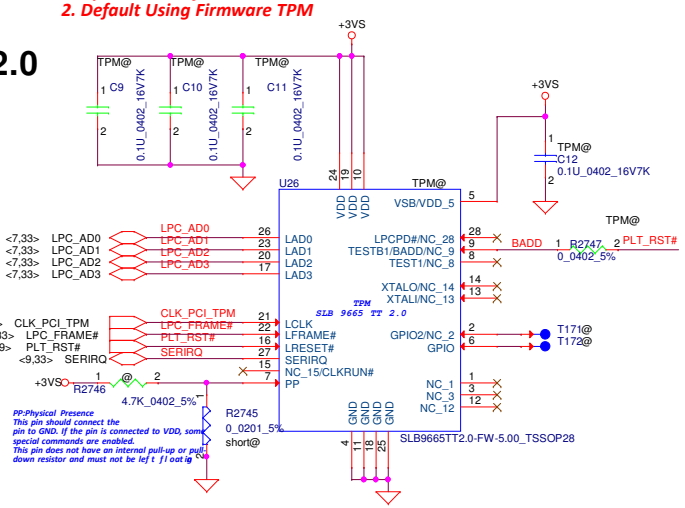
Rear Speaker

Gain	GAIN2	GAIN1	GAIN0	Min	Typ	Max	Unit
	1	1	1	31	32	33	dB
			0	25	26	27	
		0	1	19	20	21	
			0	17	18	19	
	0	1	1	11	12	13	
			0	9	10	11	
		0	1	5	6	7	
			0	-	0	-	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/04/13	Deciphered Date 2018/04/13	Title: Audio Subwoofer AMP : ALC1301-CGT
			Size: Custom; Document Number: LA-C501P; Rev: 1.0
			Date: Wednesday, April 22, 2015; Sheet 31 of 63

2014-10-14:
1. Upated Pin def i net o TP M2 0
2. Default Using Firmware TPM

TPM2.0

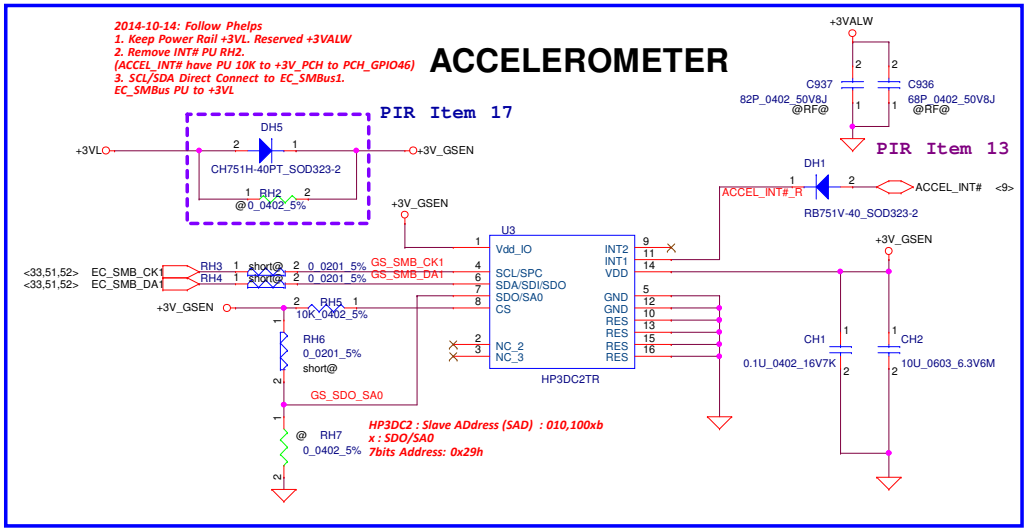


ACCELEROMETER

2014-10-14: Follow Phelps
1. Keep Power Rail +3VL. Reserved +3VALW
2. Remove INT# PU RH2.
(ACCEL_INT# have PU 10K to +3V_PCH to PCH_GPIO46)
3. SCL/SDA Direct Connect to EC_SMBus1.
EC_SMBus PU to +3VL

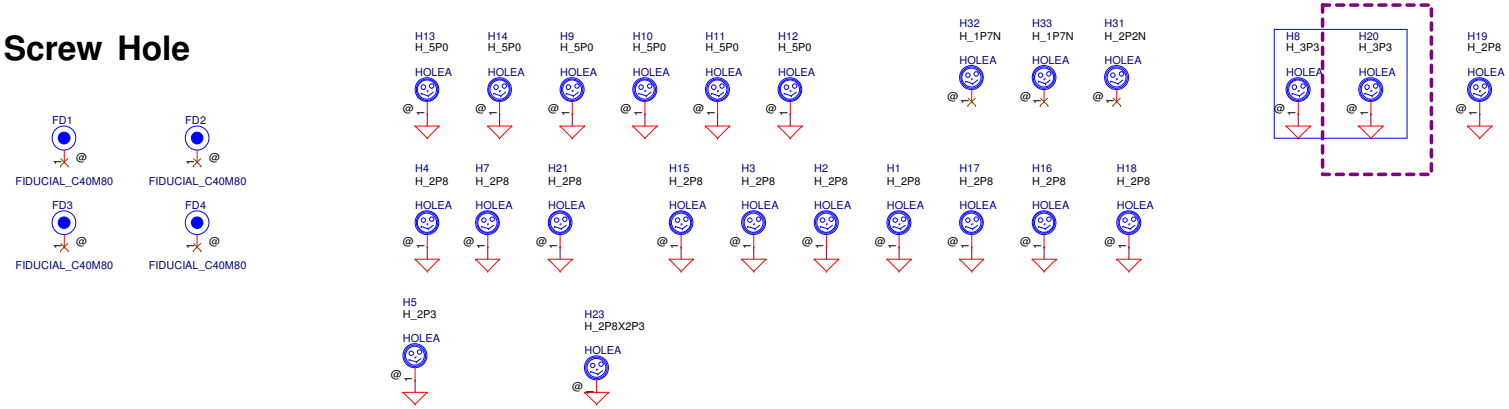
PIR Item 17

PIR Item 13



Screw Hole

PIR Item 2



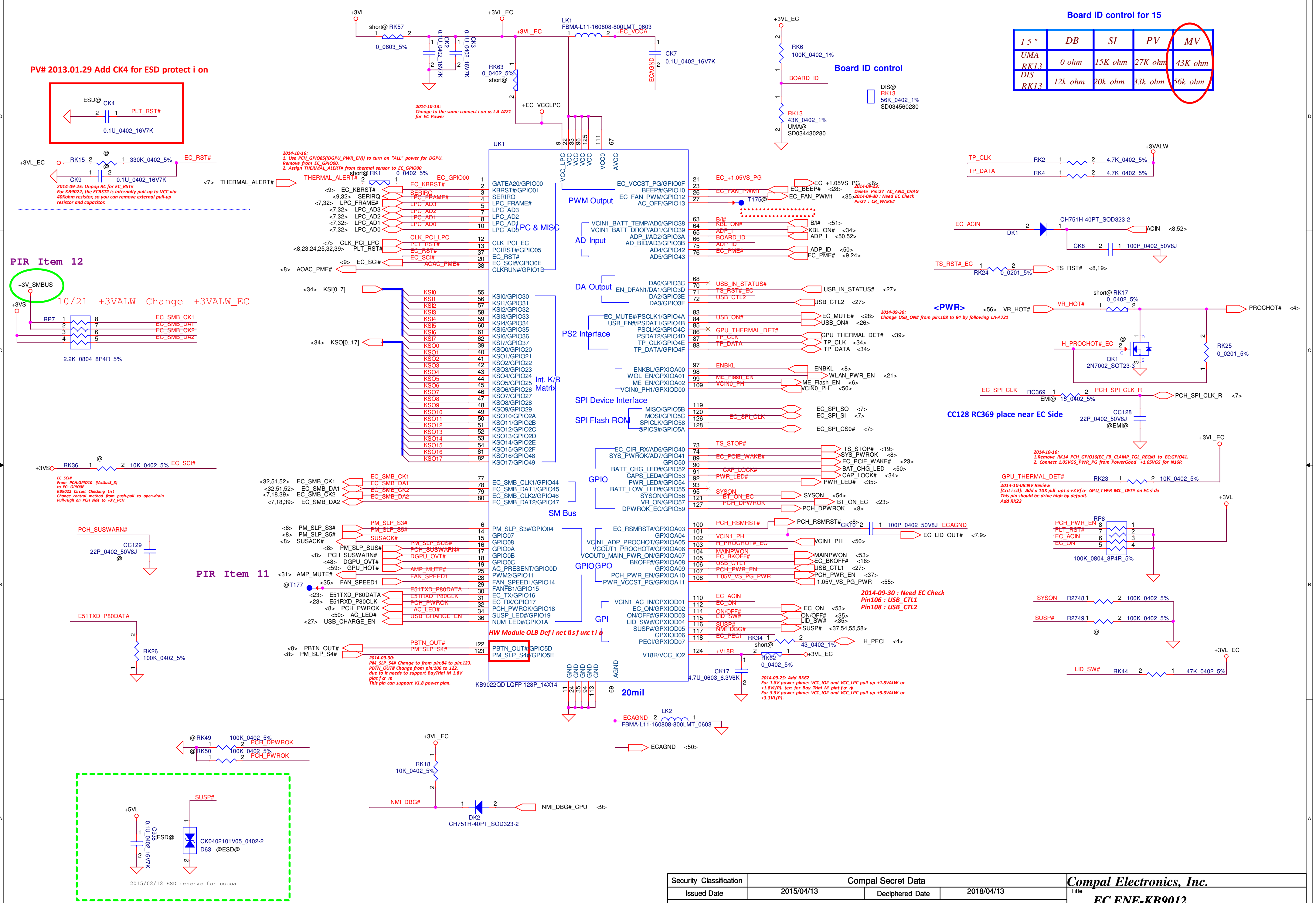
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: LED/14"Screw hole

Size	Document Number	Rev
	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 32 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

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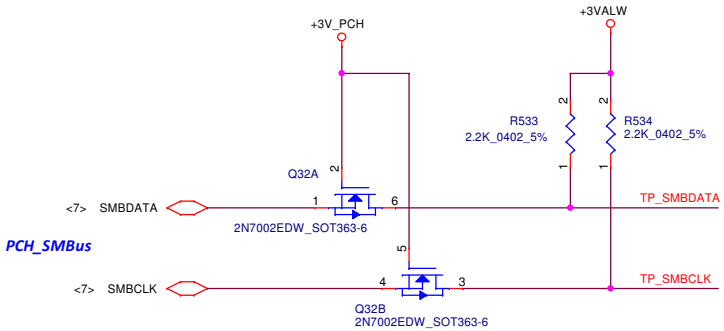
Compal Electronics, Inc.

Title: **EC ENE-KB9012**

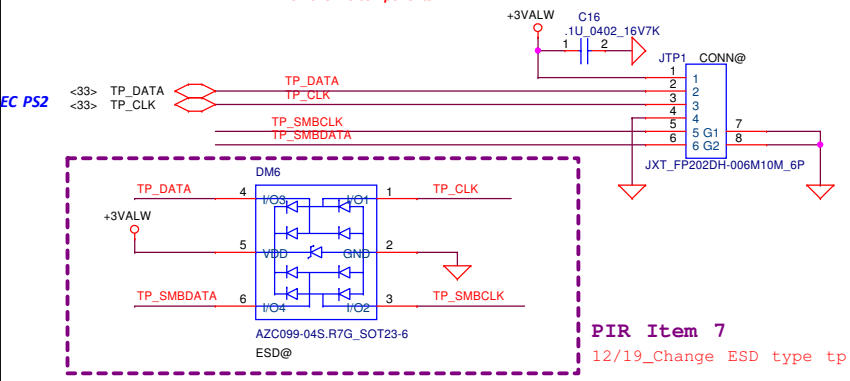
Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 33 of 63

Touch pad conn



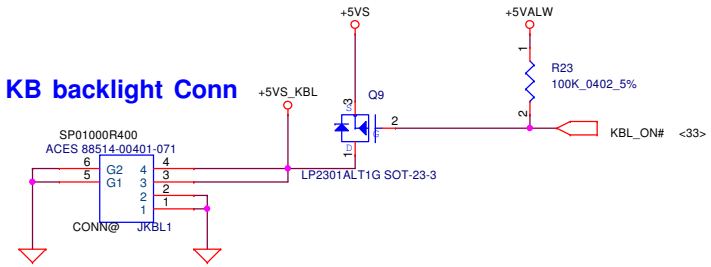
2014-10-14:
Confirm with Synaptics "Only" PS2+ SMBus" interface
Remove I2C components.



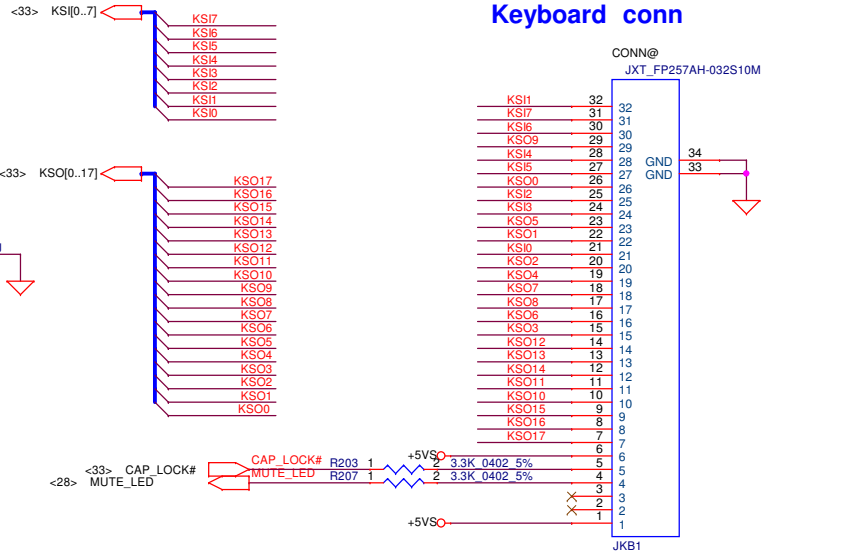
PIR Item 7

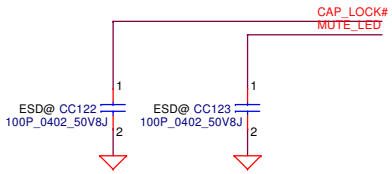
12/19_Change ESD type tp 6 pin

KB backlight Conn



Keyboard conn





Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: KB/TP

Size	Document Number	Rev
Custom	LA-C501P	1.0

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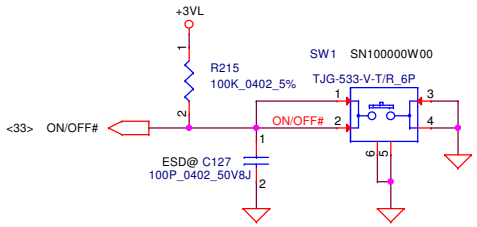
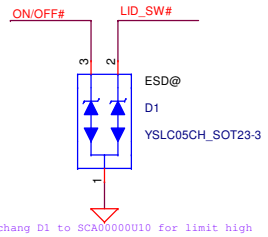
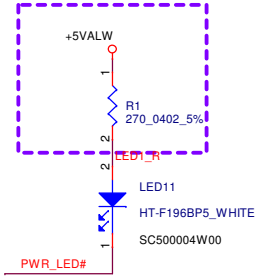
Powert Button Switch



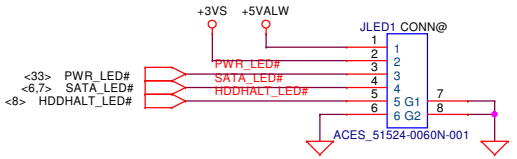
ESD Diode



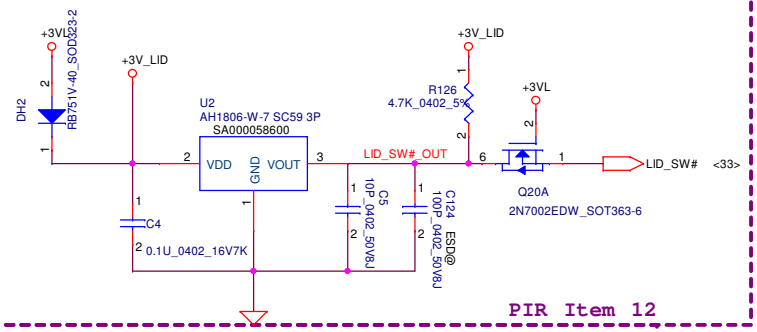
chang D1 to SCA00000U10 for limit high



to LED Board

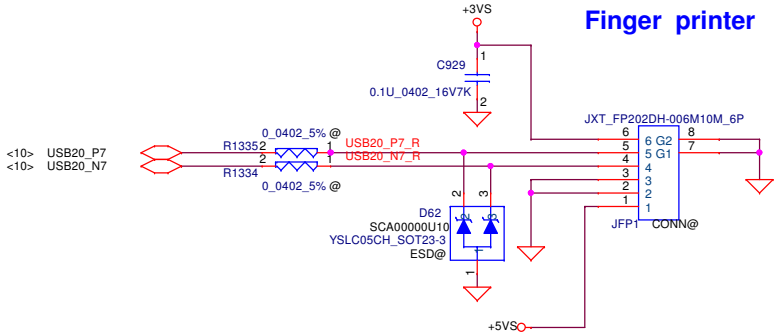


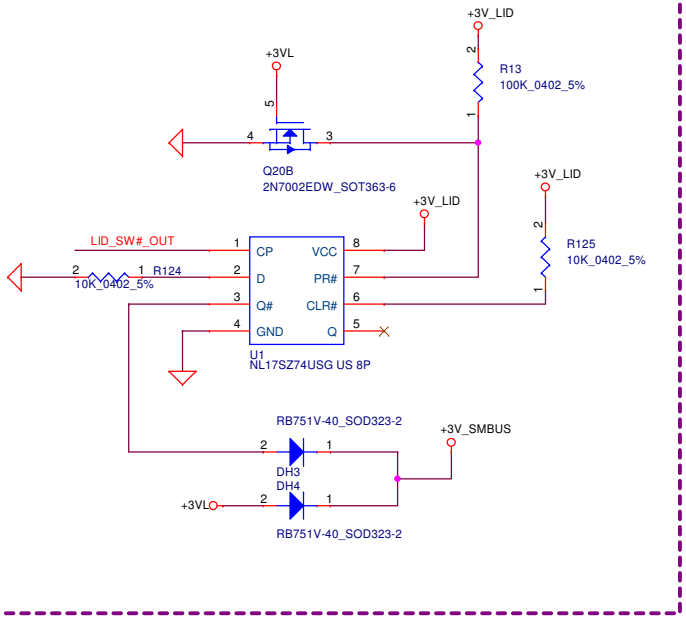
Lid Switch (Hall Effect Sensor)



PIR Item 12

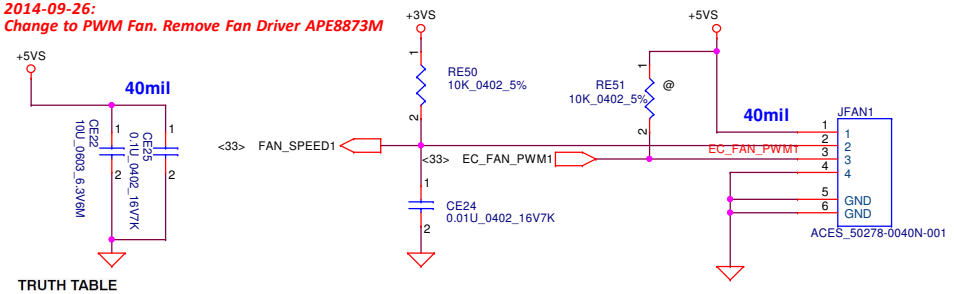
Finger printer





FAN conn

2014-09-26:
Change to PWM Fan. Remove Fan Driver APE8873M



TRUTH TABLE

Inputs				Outputs		
PR	CLR	CP	D	Q	Q̄	Operating Mode
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	↧	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low-to-High Transition
↧ = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT Inputs

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title	PWRBTN/FAN	
Size: Custom	Document Number: LA-C501P	Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 35 of 63	

Reserve for HW

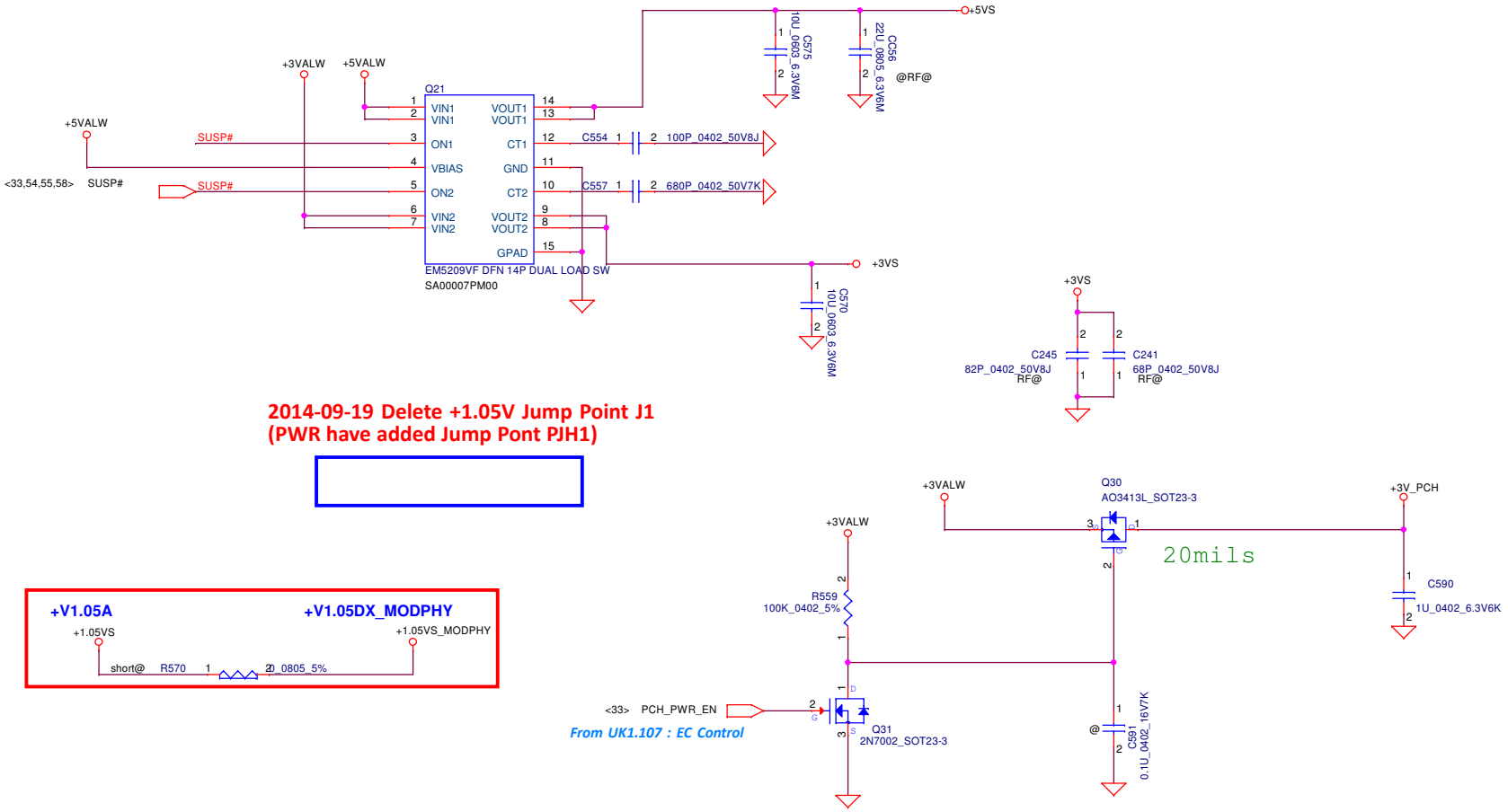
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **GCLK**

Size | Document Number: **LA-C501P** | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 36 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 37 of 63

Reserve for HW

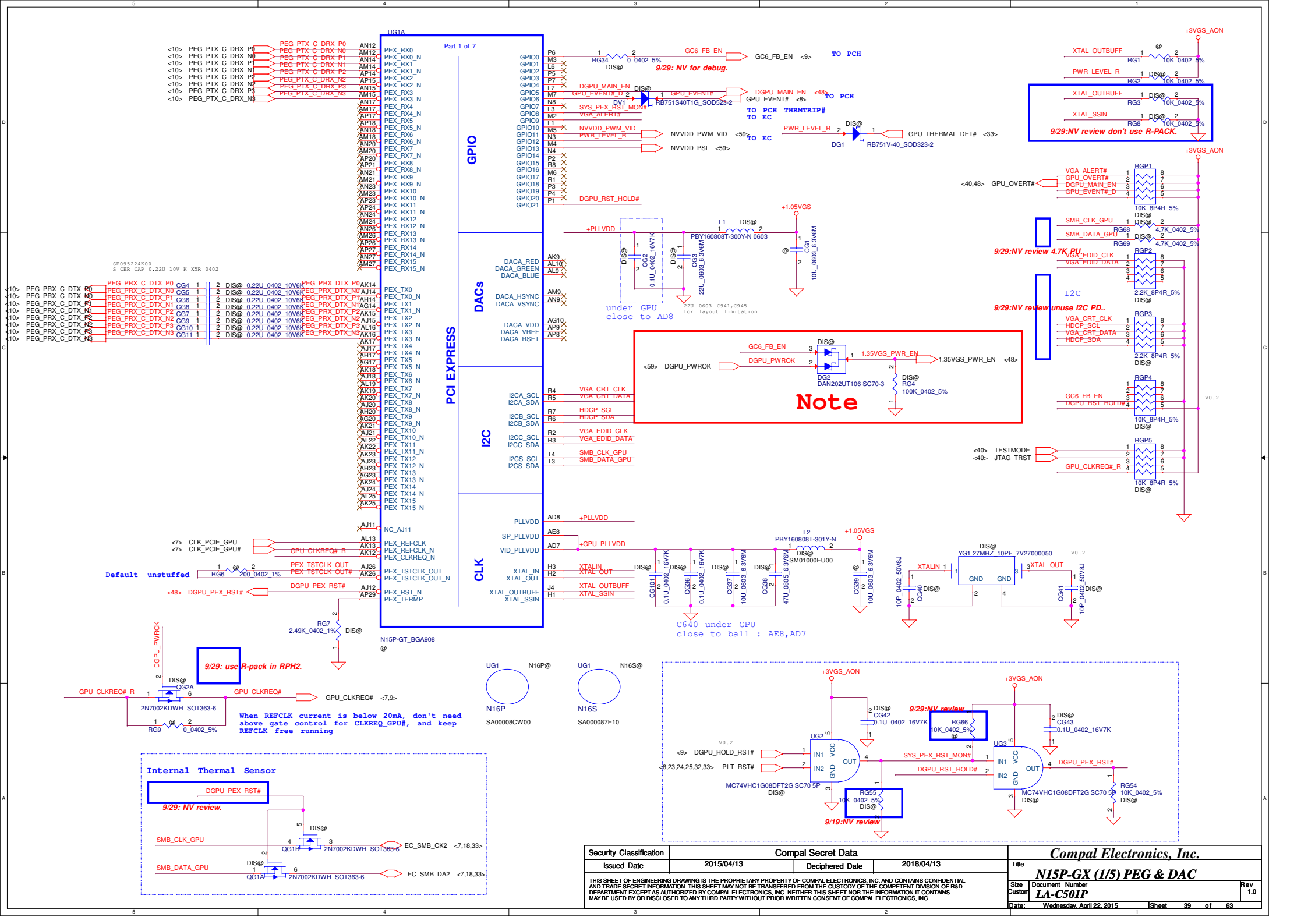
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **WAKE and RST-1**

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 | Sheet 38 of 63


UG1A
Part 1 of 7
PCI EXPRESS
GPIO
DACs
I2C
CLK
PEX_RX0
PEX_RX0_N
PEX_RX1
PEX_RX1_N
PEX_RX2
PEX_RX2_N
PEX_RX3
PEX_RX3_N
PEX_RX4
PEX_RX4_N
PEX_RX5
PEX_RX5_N
PEX_RX6
PEX_RX6_N
PEX_RX7
PEX_RX7_N
PEX_RX8
PEX_RX8_N
PEX_RX9
PEX_RX9_N
PEX_RX10
PEX_RX10_N
PEX_RX11
PEX_RX11_N
PEX_RX12
PEX_RX12_N
PEX_RX13
PEX_RX13_N
PEX_RX14
PEX_RX14_N
PEX_RX15
PEX_RX15_N
PEX_TX0
PEX_TX0_N
PEX_TX1
PEX_TX1_N
PEX_TX2
PEX_TX2_N
PEX_TX3
PEX_TX3_N
PEX_TX4
PEX_TX4_N
PEX_TX5
PEX_TX5_N
PEX_TX6
PEX_TX6_N
PEX_TX7
PEX_TX7_N
PEX_TX8
PEX_TX8_N
PEX_TX9
PEX_TX9_N
PEX_TX10
PEX_TX10_N
PEX_TX11
PEX_TX11_N
PEX_TX12
PEX_TX12_N
PEX_TX13
PEX_TX13_N
PEX_TX14
PEX_TX14_N
PEX_TX15
PEX_TX15_N
NC_AJ11
PEX_REFCLK
PEX_REFCLK_N
PEX_CLKREQ_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_RST_N
PEX_TERMP
N15P-GT_BGA908
@
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
GC6_FB_EN
DGPU_MAIN_EN
GPU_EVENT#_D
SYS_PEX_RST_MON#
VGA_ALERT#
NVVDD_PWM_VID
PWR_LEVEL_R
NVVDD_PSI
DGPU_RST_HOLD#
+PLLVDD
+GPU_PLLVDD
VGA_CRT_CLK
VGA_CRT_DATA
HDCP_SCL
HDCP_SDA
VGA_EDID_CLK
VGA_EDID_DATA
SMB_CLK_GPU
SMB_DATA_GPU
XTALIN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
PEG_PTX_C_DRX_P0
PEG_PTX_C_DRX_N0
PEG_PTX_C_DRX_P1
PEG_PTX_C_DRX_N1
PEG_PTX_C_DRX_P2
PEG_PTX_C_DRX_N2
PEG_PTX_C_DRX_P3
PEG_PTX_C_DRX_N3
PEG_PRX_C_DTX_P0
PEG_PRX_C_DTX_N0
PEG_PRX_C_DTX_P1
PEG_PRX_C_DTX_N1
PEG_PRX_C_DTX_P2
PEG_PRX_C_DTX_N2
PEG_PRX_C_DTX_P3
PEG_PRX_C_DTX_N3
SE095224K00
S CER CAP 0.22U 10V K X5R 0402
CLK_PCIE_GPU
CLK_PCIE_GPU#
GPU_CLKREQ#_R
DGPU_PEX_RST#
DGPU_PWROK
GPU_CLKREQ#
2N7002KDWH_SOT363-6
When REFCLK current is below 20mA, don't need above gate control for CLKREQ_GPU#, and keep REFCLK free running
9/29: use R-pack in RPH2.
9/29: NV for debug.
TO PCH
TO PCH THRMTRIP#
TO EC
GPU_THERMAL_DET#
RB751V-40_SOD323-2
RB751S40T1G_SOD523-2
9/29:NV review don't use R-PACK.
9/29:NV review 4.7K PU
9/29:NV review unuse I2C PD..
I2C
Note
GPU_OVERT#
TESTMODE
JTAG_TRST
GPU_CLKREQ#_R
1.35VGS_PWR_EN
DGPU_PWROK
DAN202UT106 SC70-3
PBY160808T-300Y-N 0603
PBY160808T-301Y-N
SM01000EU00
YG1 27MHZ 10PF 7V27000050
under GPU close to AD8
C640 under GPU close to ball : AE8,AD7
22U 0603 C941,C945 for layout limitation
Internal Thermal Sensor
9/29: NV review.
9/19:NV review
MC74VHC1G08DFT2G SC70 5P
EC_SMB_CK2
EC_SMB_DA2
N16P
SA00008CW00
N16S
SA000087E10
+3VGS_AON
+1.05VGS
Security Classification
Compal Secret Data
Issued Date
2015/04/13
Deciphered Date
2018/04/13
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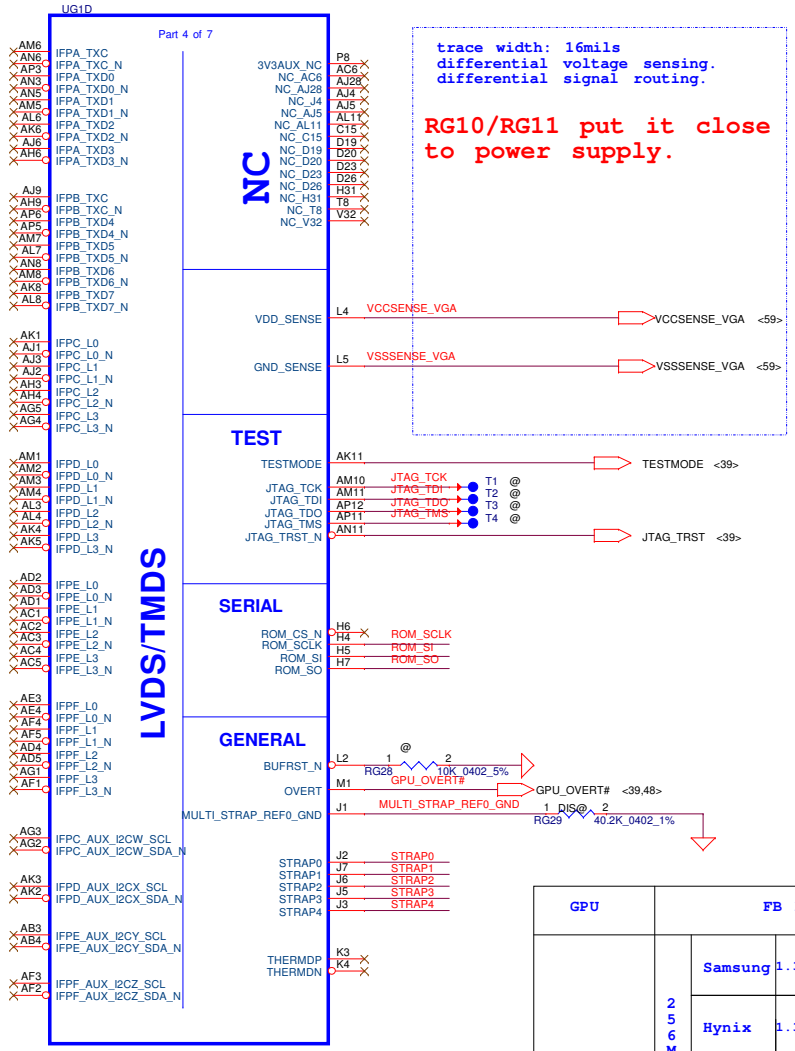
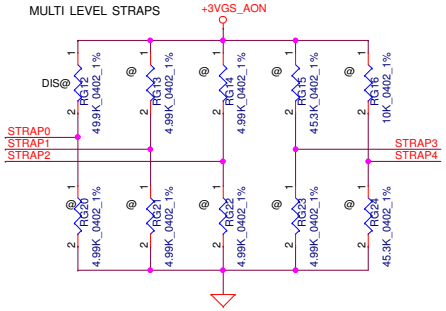
Compal Electronics, Inc.
Title
N15P-GX (1/5) PEG & DAC
Size
Custom
Document Number
LA-C501P
Rev
1.0
Date:
Wednesday, April 22, 2015
Sheet
39
of
63

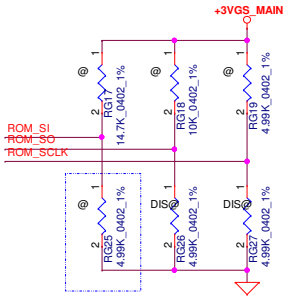


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS_MAIN	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	+3VGS_MAIN	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	+3VGS_MAIN	**DEVID_SEL**	**PCIE_CFG**	**SMB_ALT_ADDR**	VGA_DEVICE
STRAP0	Keep pull-up to 3V3_AON and pull-down to GND foot print and stuff 50K ohm pull-up				
STRAP1					
STRAP2	RESERVED				
STRAP3					
STRAP4					

SKU	Device ID	bit5 to bit0
N16P-GT		

Resistor Values	Pull-up to +3VGS_MAIN	Pull-down to Gnd
5K	1000 =8	0000 =0
10K	1001 =9	0001 =1
15K	1010 =A	0010 =2
20K	1011 =B	0011 =3
25K	1100 =C	0100 =4
30K	1101 =D	0101 =5
35K	1110 =E	0110 =6
45K	1111 =F	0111 =7

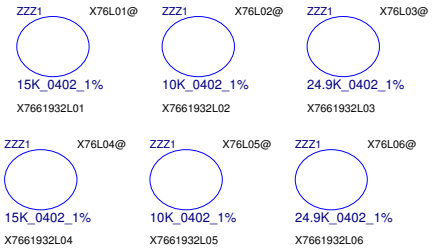




GPU	FB Memory DDR3L(1.35V)					RAM_CFG[3:0] (ROM_SI)	
N16P-GT, N16S-GT	256M x16	Samsung	1.35V	900MHz	K4W4G1646E-BC1A	0x1(PD 10K)	
		Hynix	1.35V	900MHz	H5TC4G63CFR-N0C	0x2(PD 15K)	
		Hynix	1.35V	900MHz	H5TC4G63AFR-11C	0x3(PD 20K)	
		Micron	1.35V	900MHz	MT41J256M16HA-093G:E DateCode_Min:1332	0x4(PD 24.9K)	V
		Samsung	1.35V	900MHz	K4W4G1646D-BC1A	0x5(PD 30.1K)	

Table 6. N16P-GT DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	N/A	Production candidate
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production candidate
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production candidate
		256Mx16	Single Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production candidate
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production candidate
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate



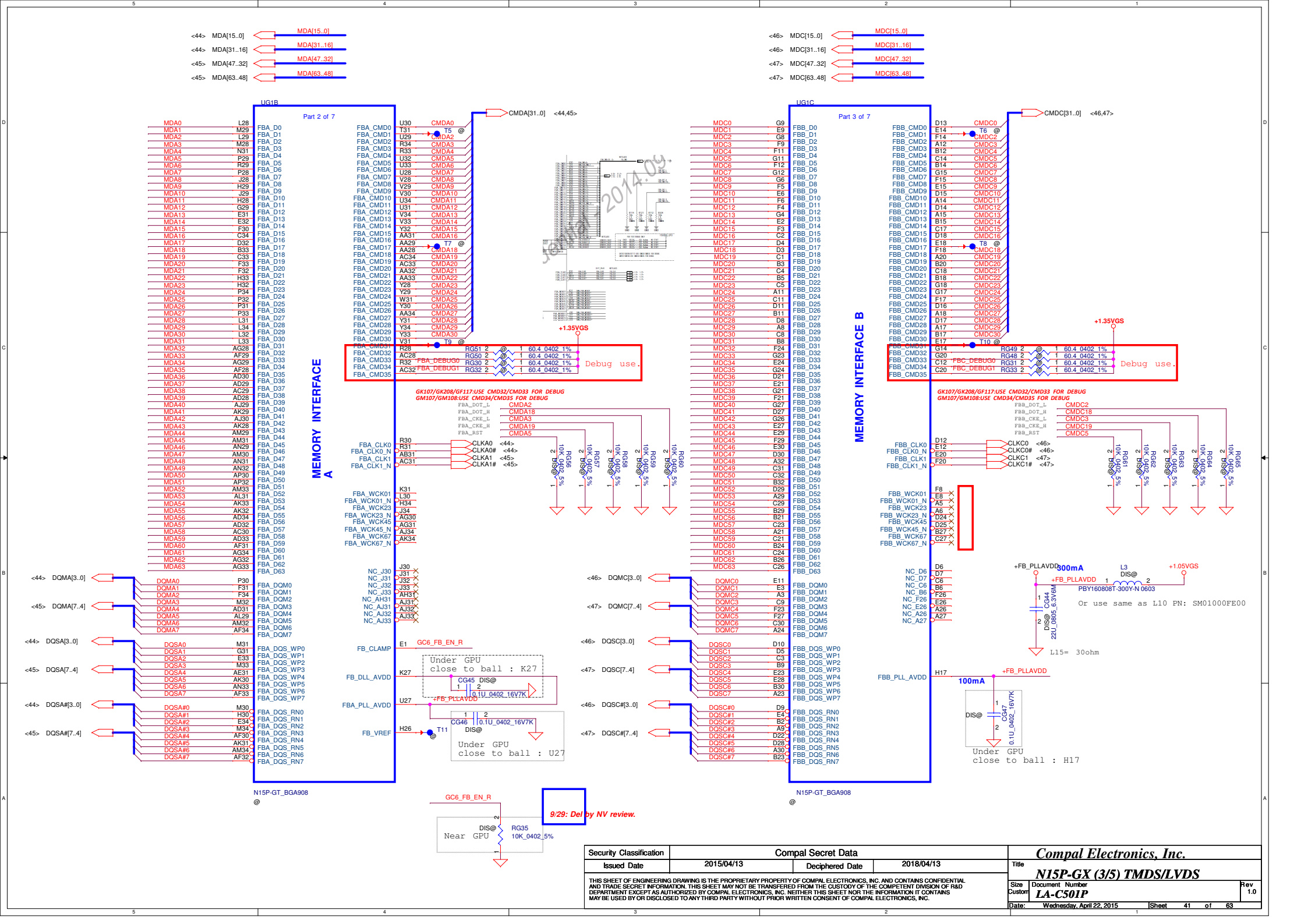
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: N15P-GX (2/5) TMDS/LVDS

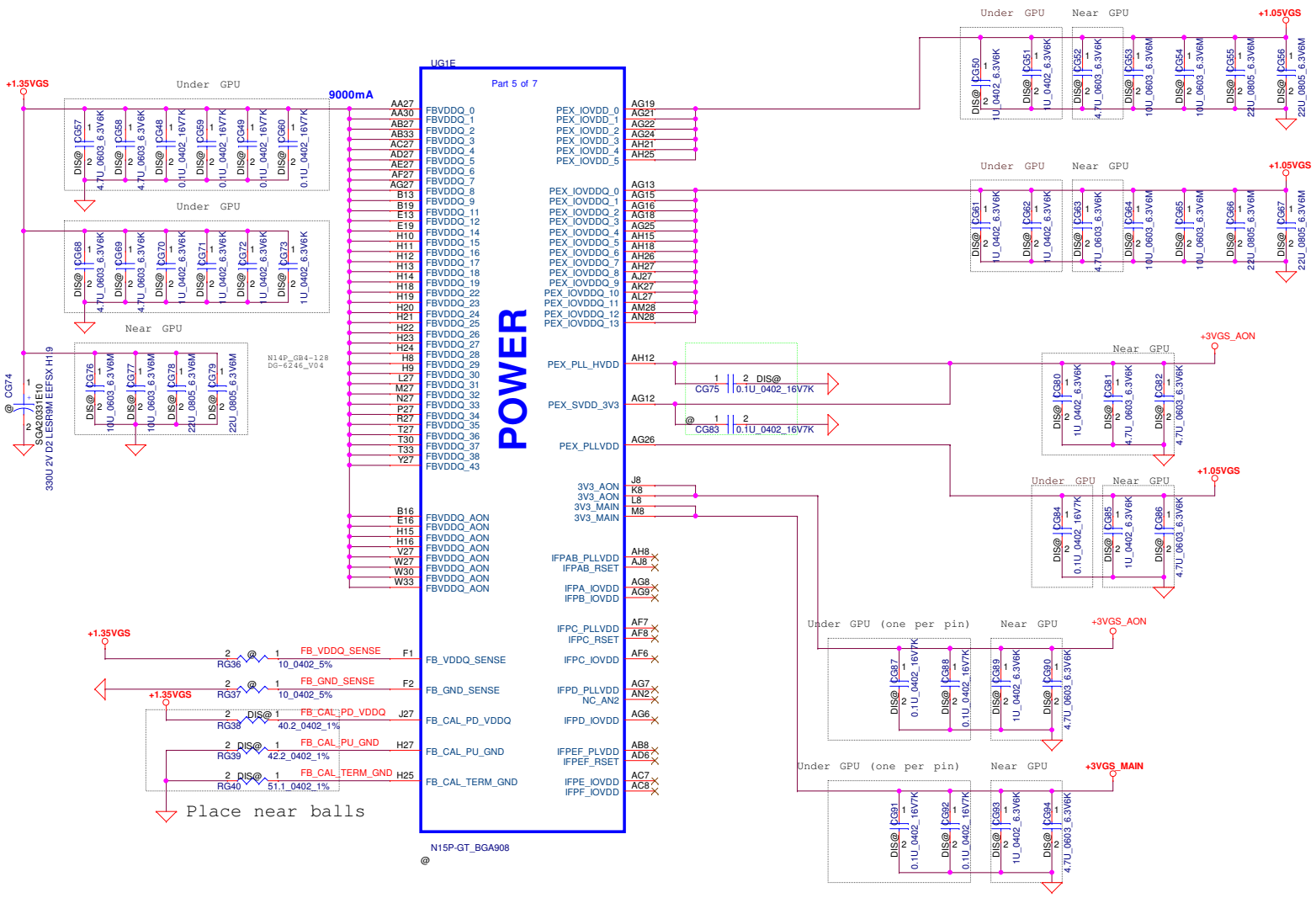
Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 40 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	N15P-GX (3/5) TMDS/LVDS		
Size: Custom	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 41 of 63		



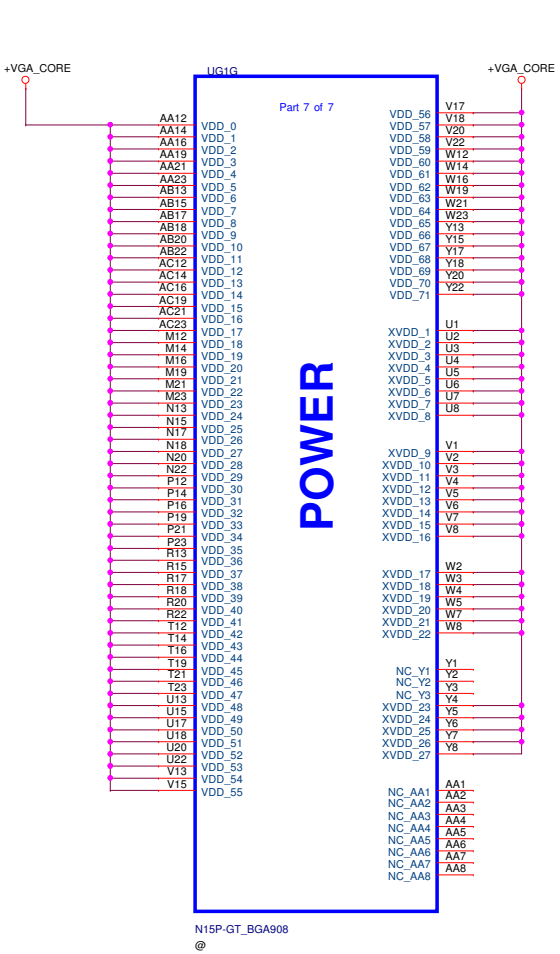
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

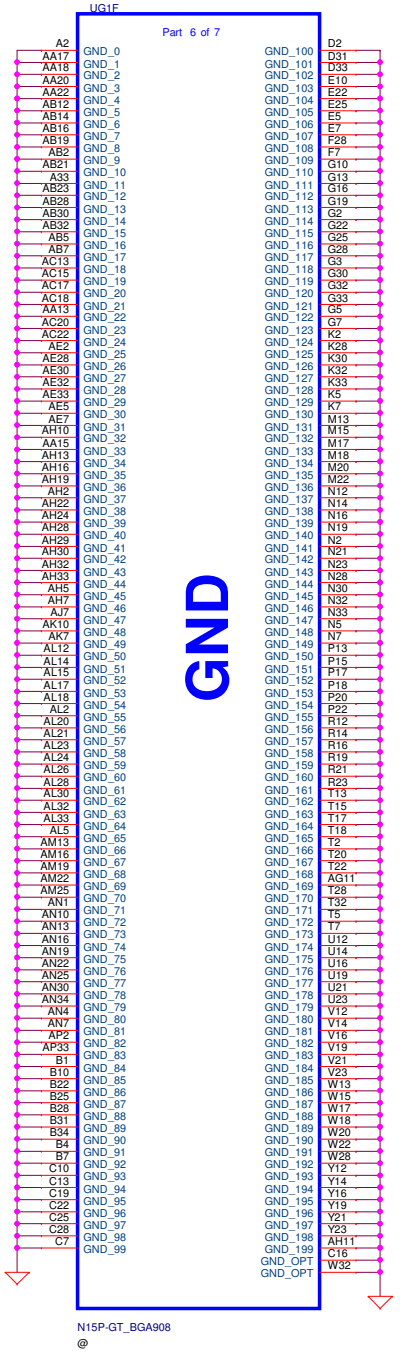
Compal Electronics, Inc.

Title: N15P-GX (4/5) POWER

Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 42 of 63





Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: N15P-GX (5/5) POWER/ GND

Size	Document Number	Rev
Custom	LA-C501P	1.0

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Memory Partition A - Lower 32 bits [31..0]

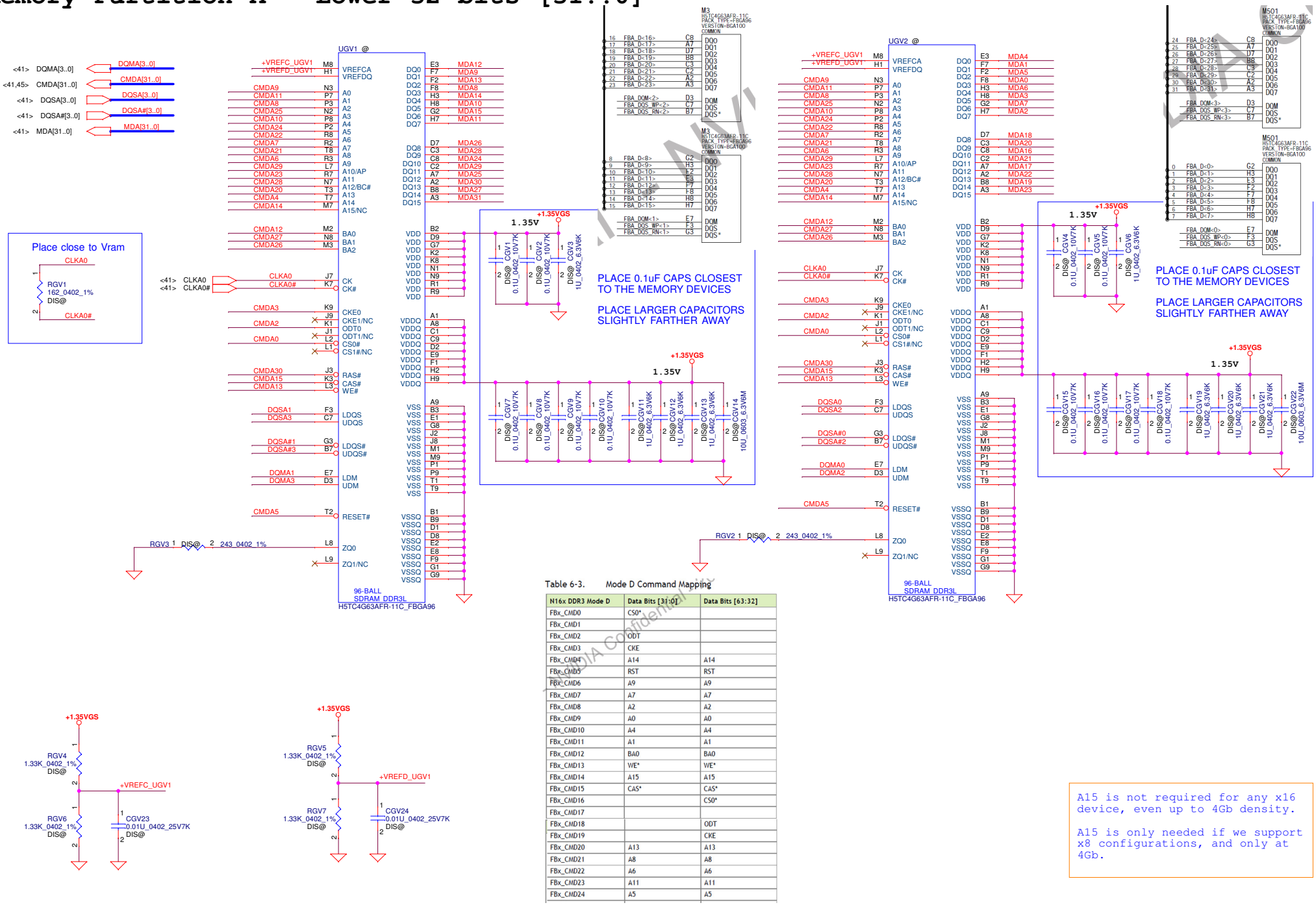


Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: VRAM_DDR3_A Lower			
Size: Custom	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 44 of 63		

Memory Partition A - Upper 32 bits [63..32]

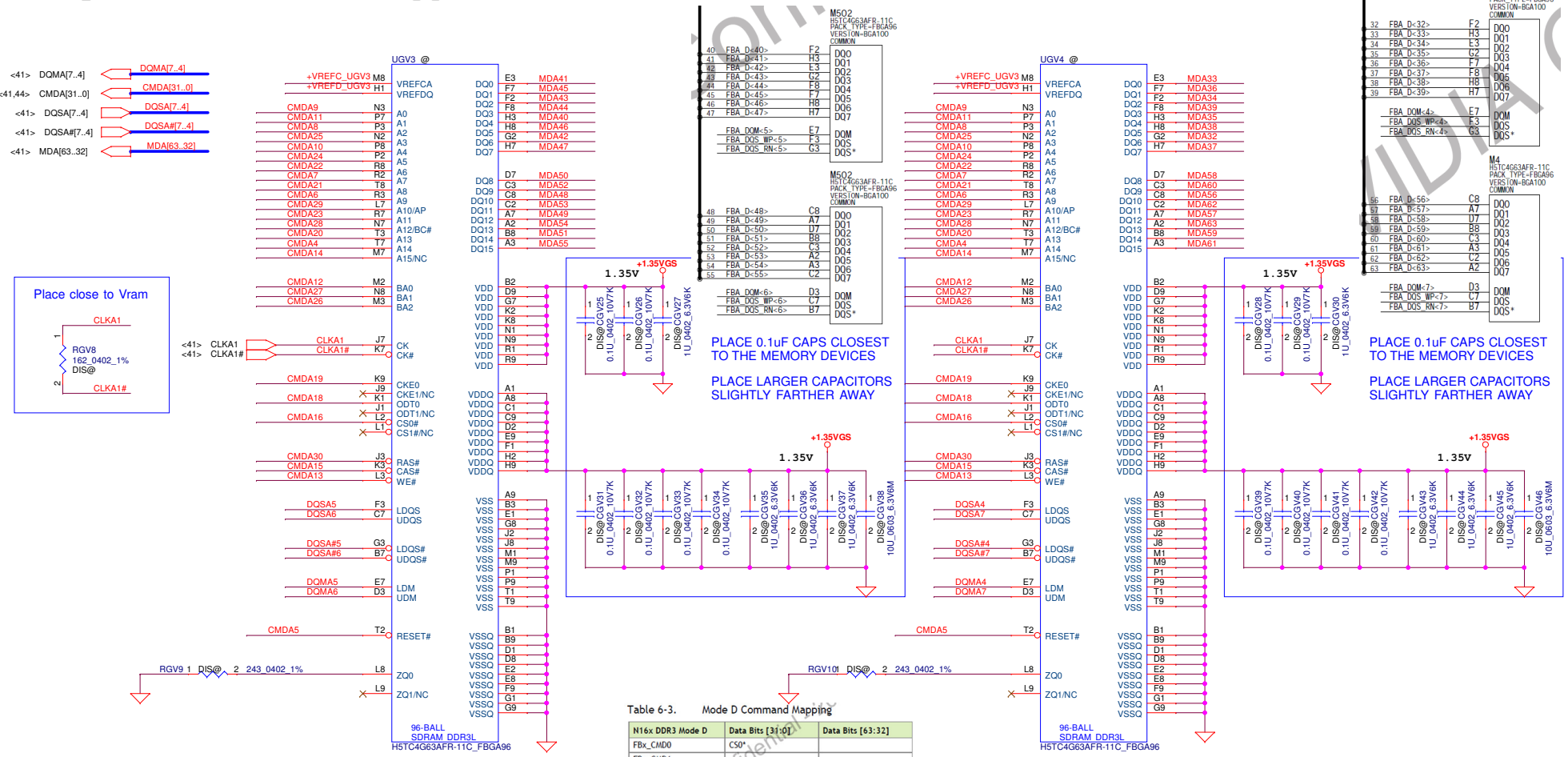


Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Compal Electronics, Inc.

Title: VRAM_DDR3_A Upper

Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 45 of 63

Memory Partition C - Lower 32 bits [31..0]

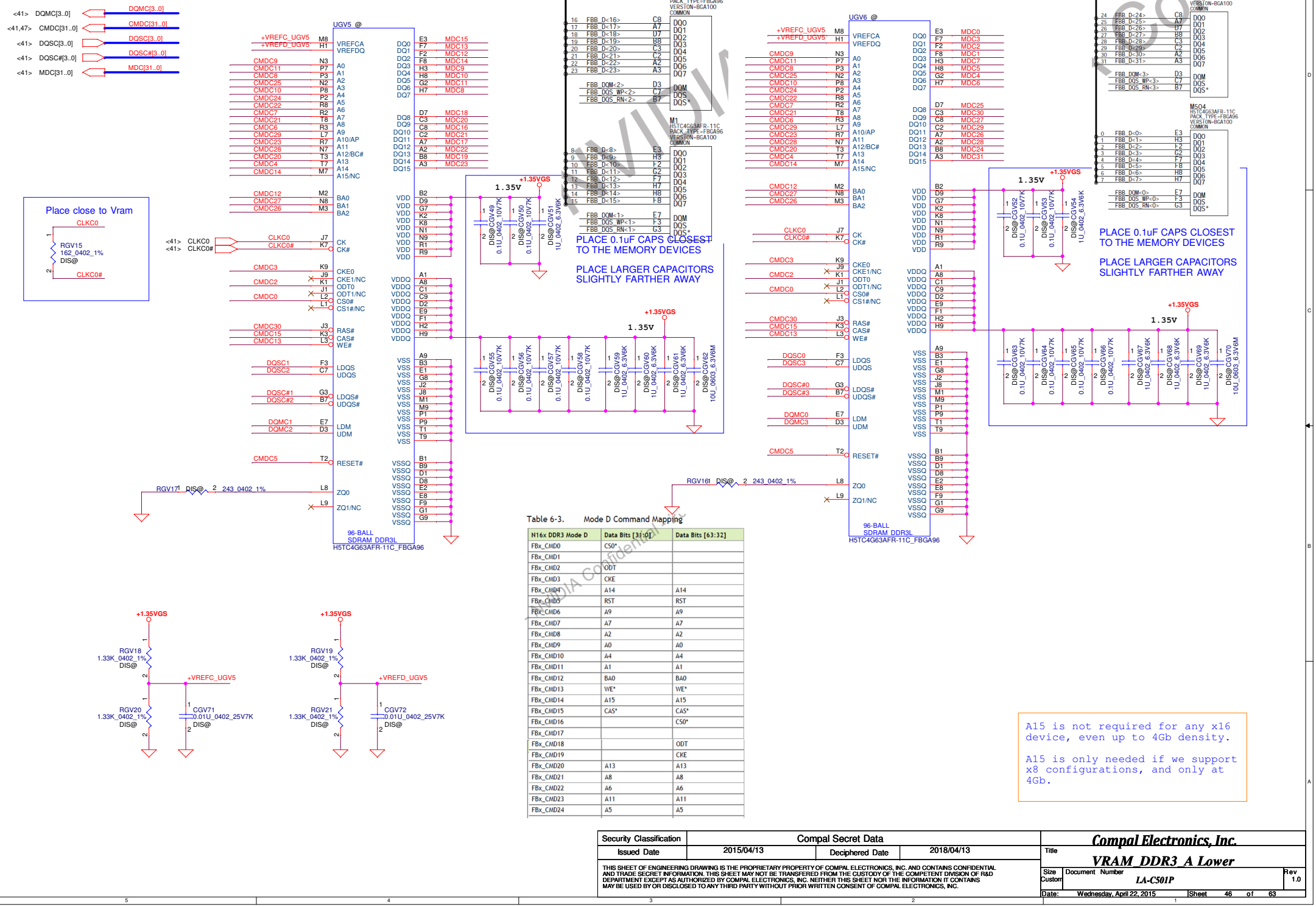


Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1	ODT	
FBx_CMD2	CKE	
FBx_CMD3		
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

Compal Electronics, Inc.

Title: VRAM_DDR3_A Lower

Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 46 of 63

Memory Partition C - Upper 32 bits [63..32]

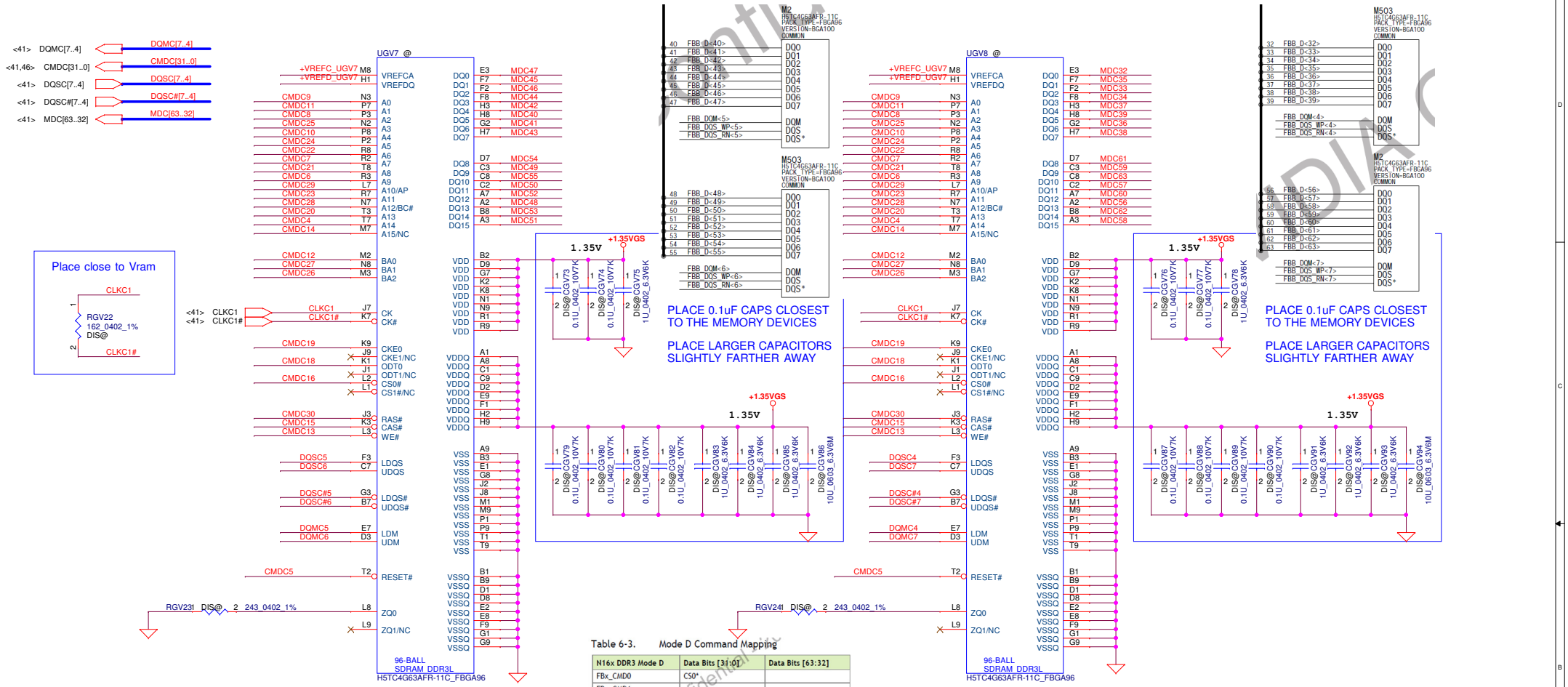


Table 6-3. Mode D Command Mapping

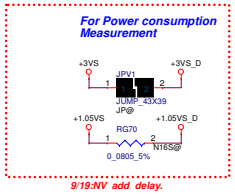
N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

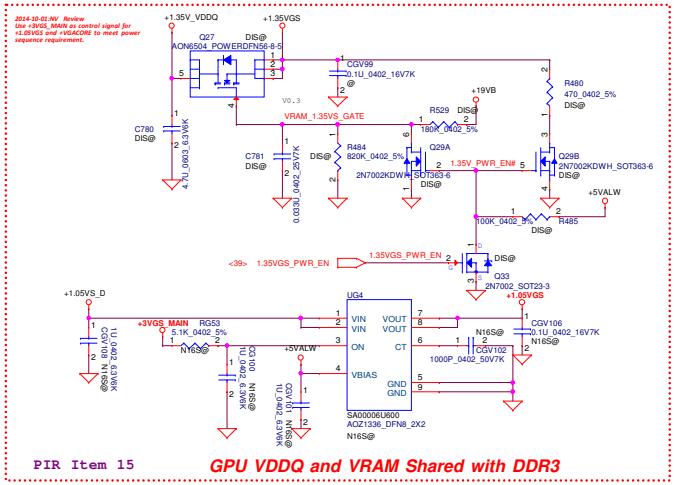
A15 is not required for any x16 device, even up to 4Gb density.

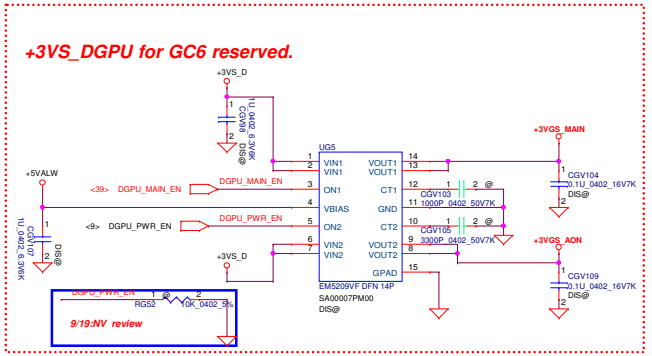
A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	VRAM_DDR3_A Upper		
Size	Document Number		Rev
Custom	LA-C501P		1.0
Date:	Wednesday, April 22, 2015	Sheet	47 of 63







3.10.2 Power Sequencing Recommendations

Power sequencing guidelines are provided relative to the ramping up of the main 3.3V system rail, which is the 3.3V input to the GPU.

3.10.2.1 Power-Up Sequence

The following condition is recommended:

3.3V → NVVDD/PEX_VDD → FBVDD/Q

- All GPU power rails must ramp up after 3.3V.
- FBVDD/Q should ramp up after both NVVDD and PEX_VDD are in regulation.

All other 3.3V power rails can ramp up with 3.3V, and all other 1.05V power rails can ramp up with PEX_VDD. Figure 3-6 shows an example of proper GPU power up sequence.

IFPx_VDD powered at 3.3V can ramp up with other 3.3V power rails. IFPy_VDD powered at 1.05V can ramp up with other 1.05V power rails. Figure 3-7 shows an example of proper GPU power up sequence.

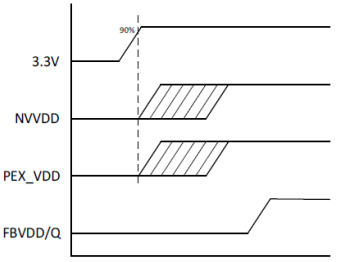


Figure 3-7. Example of Power-Up Sequencing Order

Note:

- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- Designs that support GC6 2.0 are required to meet all GC6 timing requirements. Refer to Section 18.3.2.3 for requirement details.
- PEX_VDD can ramp up before, after, or at the same time with NVVDD.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

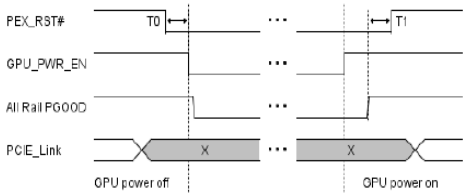


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

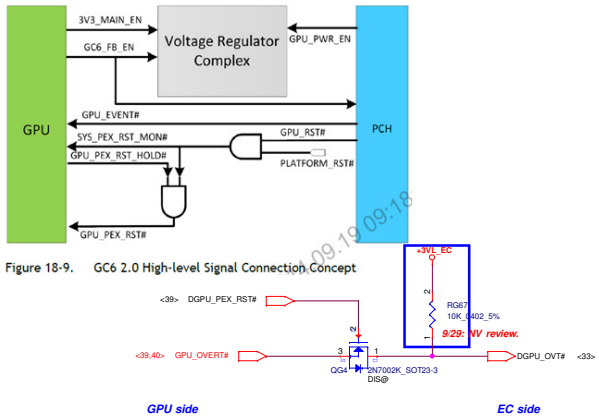


Figure 18-9. GC6 2.0 High-level Signal Connection Concept

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

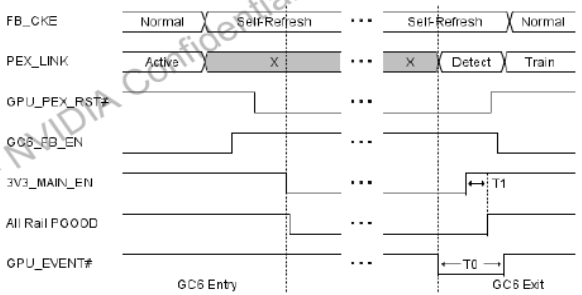


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

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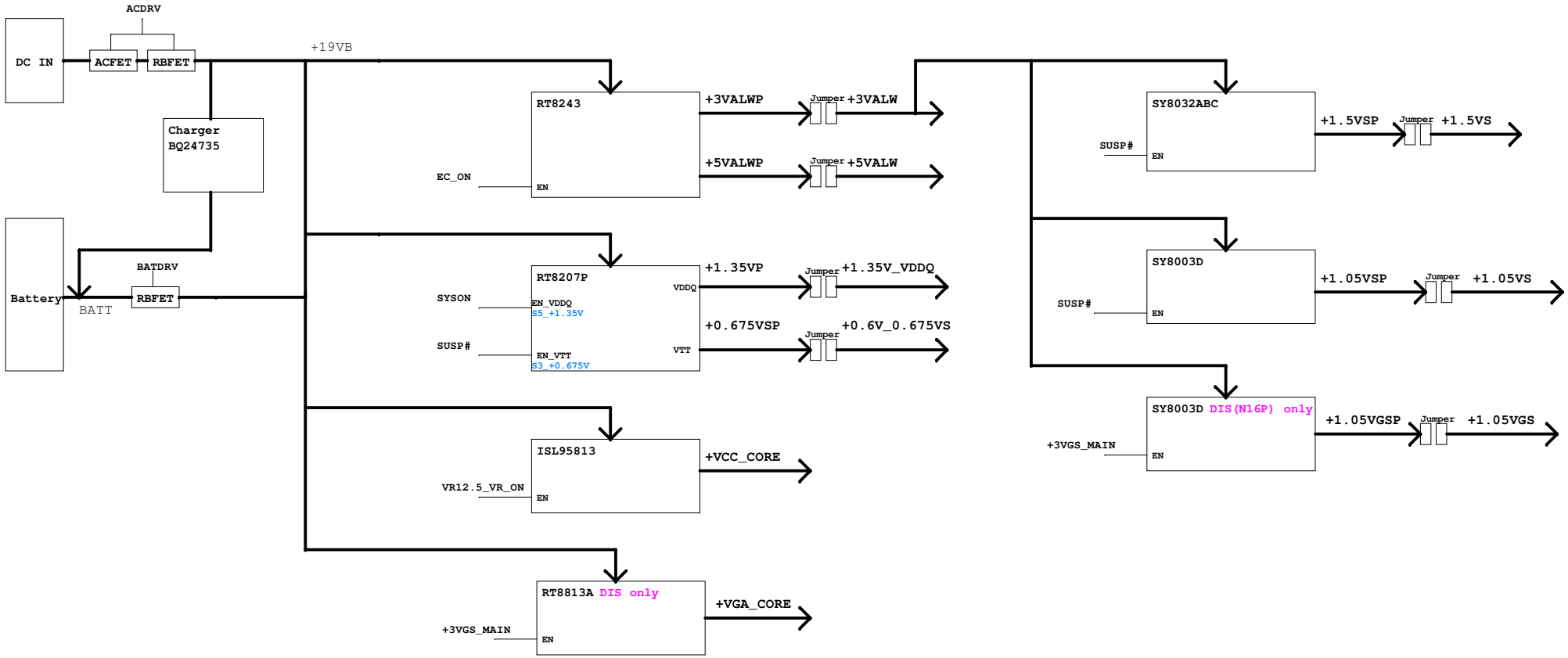
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title: N15P-GX DC-DC			
Size: Custom	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 48 of 63		



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Compal Electronics, Inc.

Title: ***Power Block Diagram***

Size	Document Number	Rev
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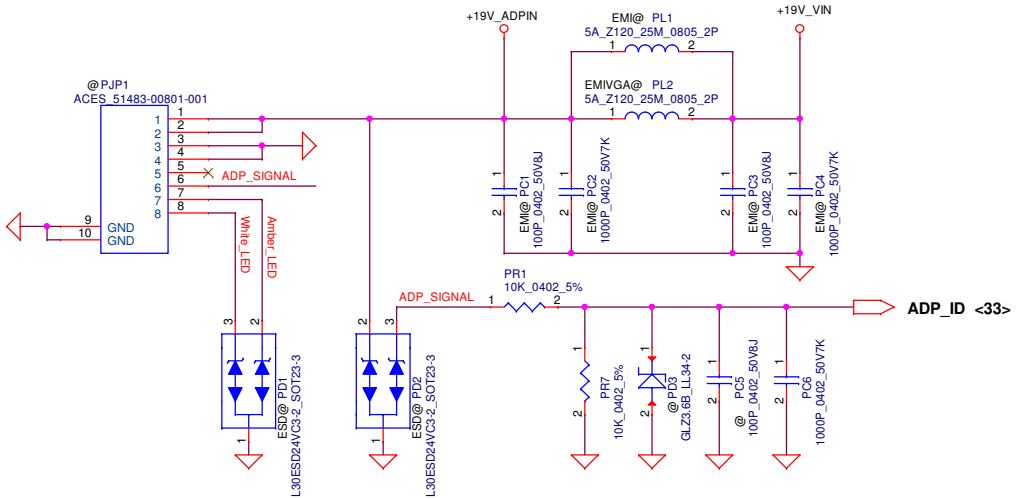
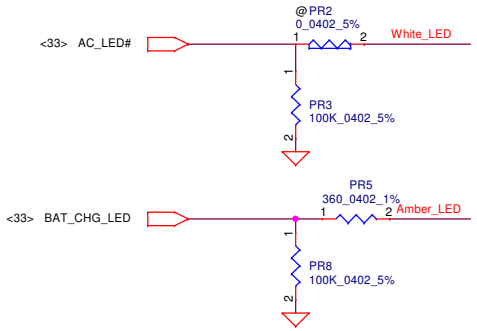
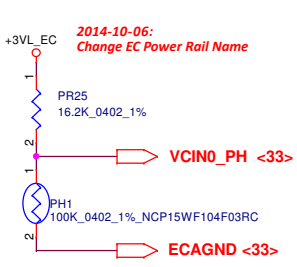
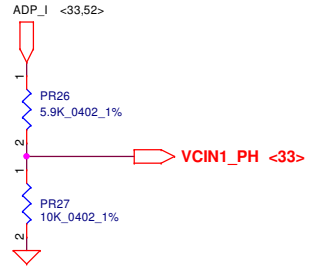






VCIN0_PH set ting
Trigger point = 1V (92C)
Recovery point = 2.02V (56C)



VCIN1_PH set ting
90W
Active: VCIN1_PH = 0.799V(123.86 W)
Resume : VCIN1_PH = 0.0.581V(90.07W)
65W
Active: VCIN1_PH = 0.599(92.86 W)
Resume : VCIN1_PH = 0.419(64.96W)
45W
Active: VCIN1_PH = 0.414(64.18 W)
Resume : VCIN1_PH = 0.289(44.8W)

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Issued Date	2014/10/09	Deciphered Date	2015/12/31

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Title	*DC Conn*	
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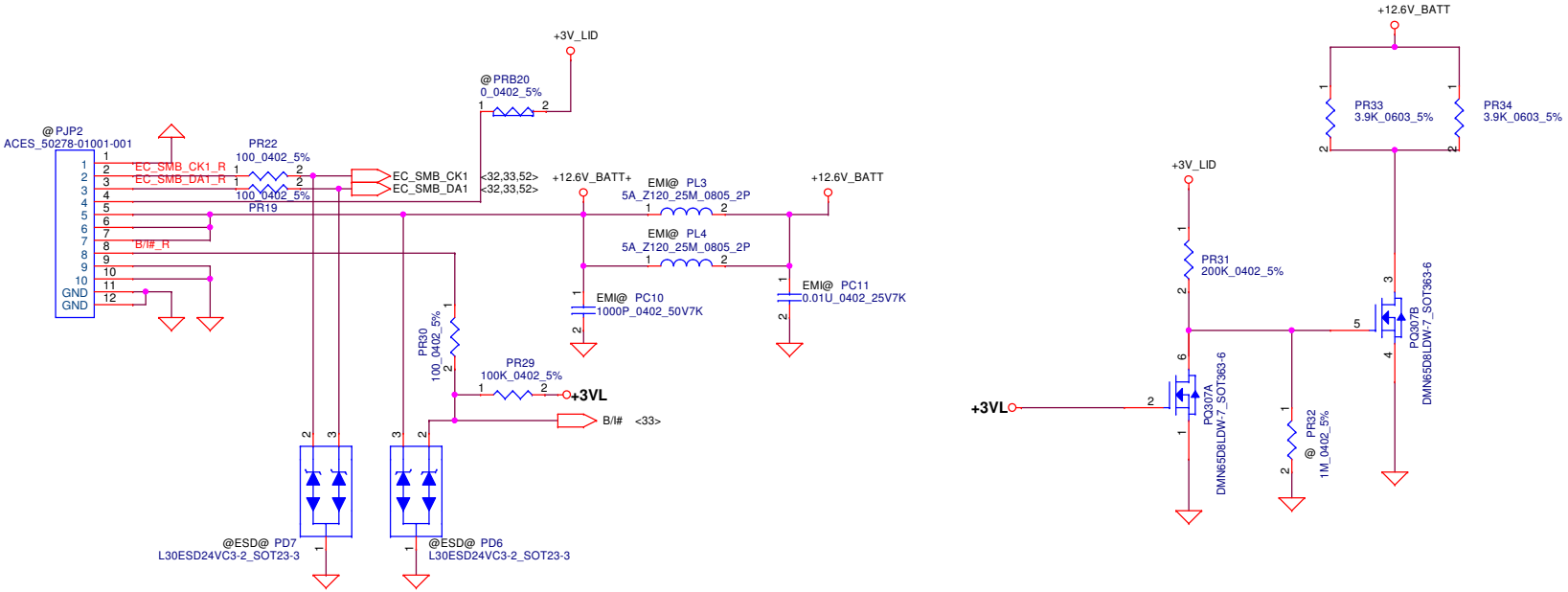
Date: Wednesday, April 22, 2015	Sheet 50 of 61	



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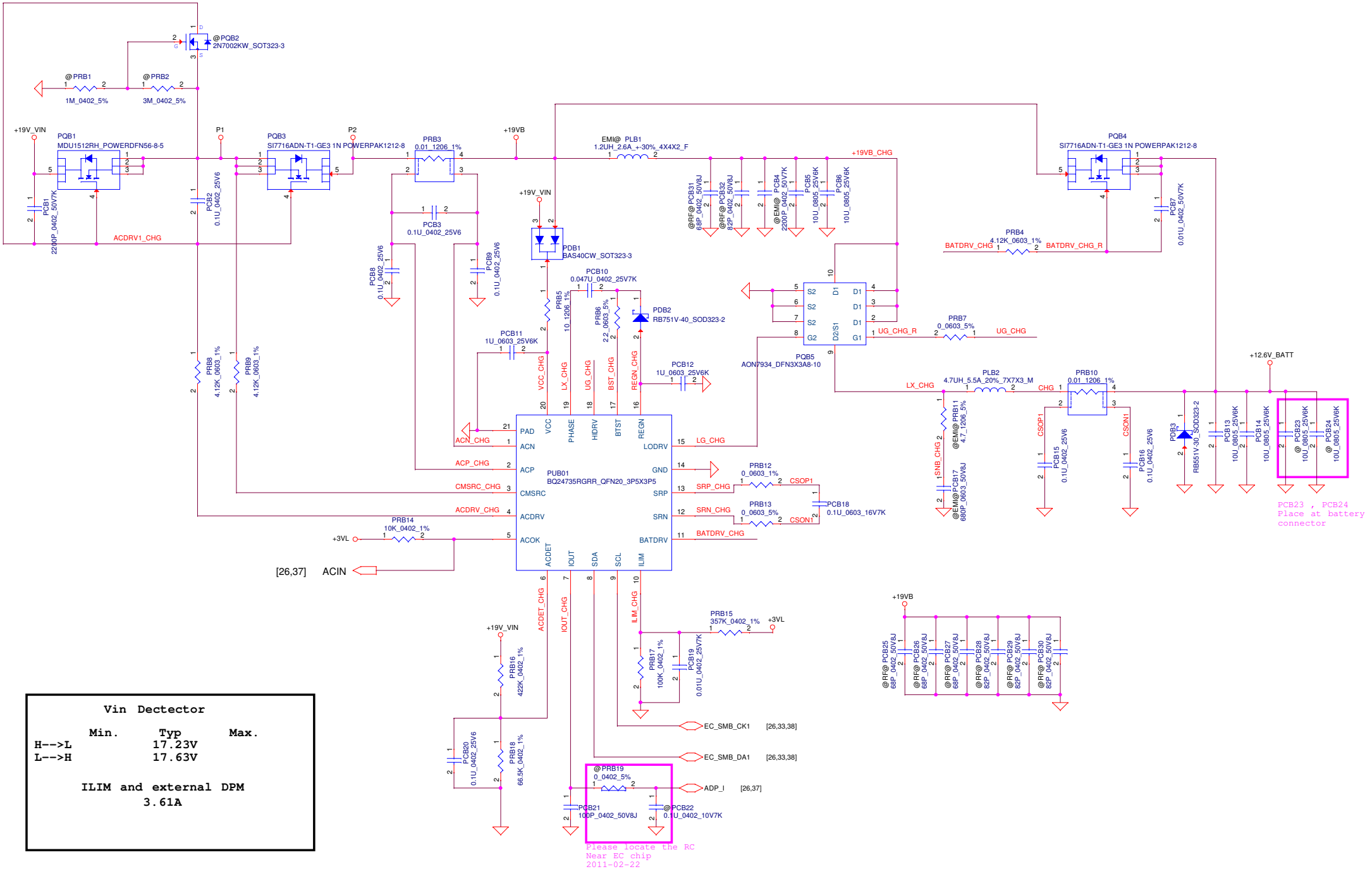
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-C501P** | Rev: 0.1

Date: Wednesday, April 22, 2015 | Sheet 51 of 61



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.61A

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Issued Date	2014/10/09	Deciphered Date	2015/12/31

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Title: *CHARGER*

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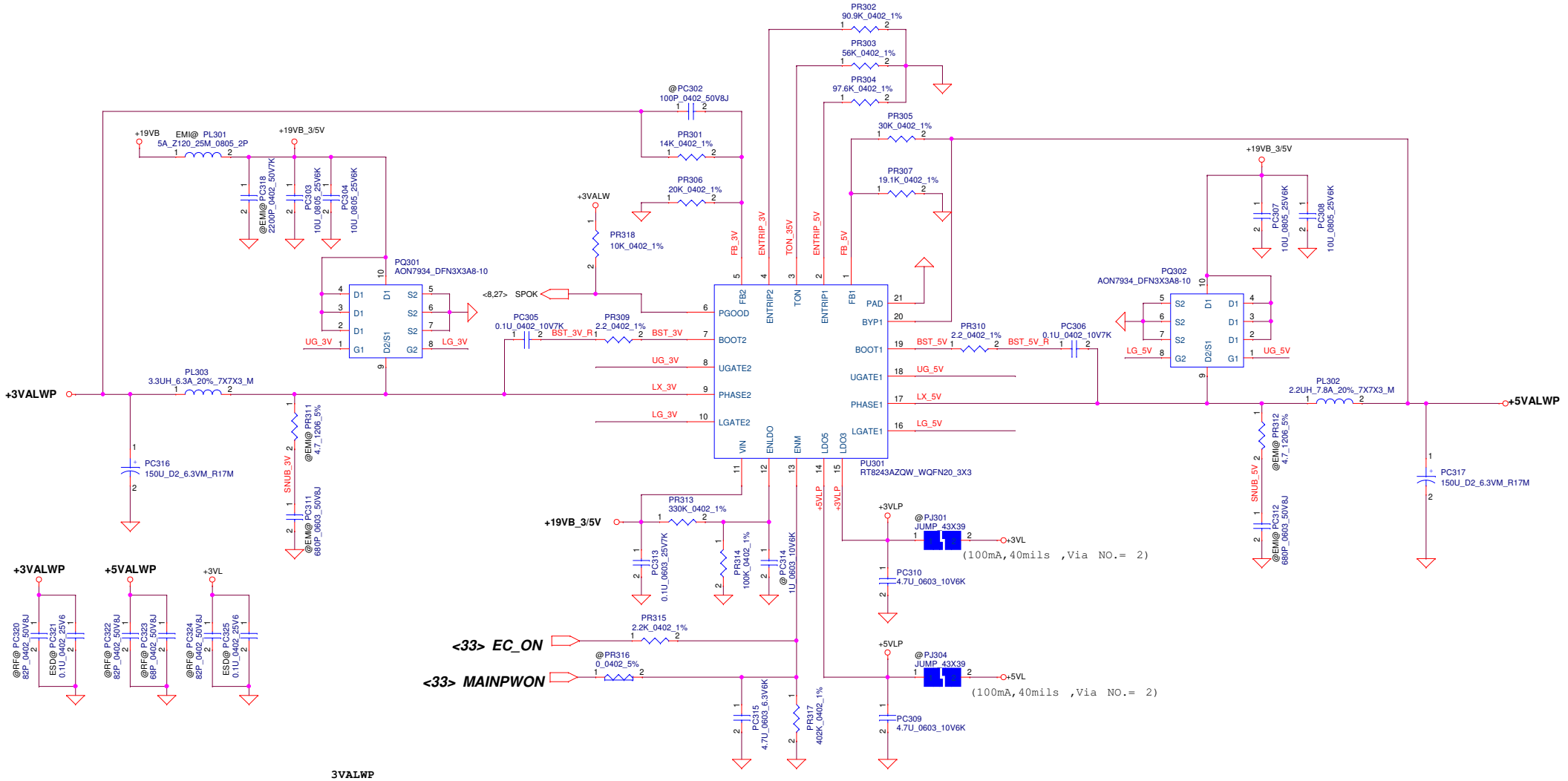

3VALWP
Fsw : 455kHz
ITDC : 5.6A
Ipeak : 7A
Iocp: 8.4A
OVP : 113%~120%

5VALWP
Fsw : 390kHz
ITDC : 6.4A
Ipeak : 8A
Iocp: 9.6A
OVP : 113%~120%

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

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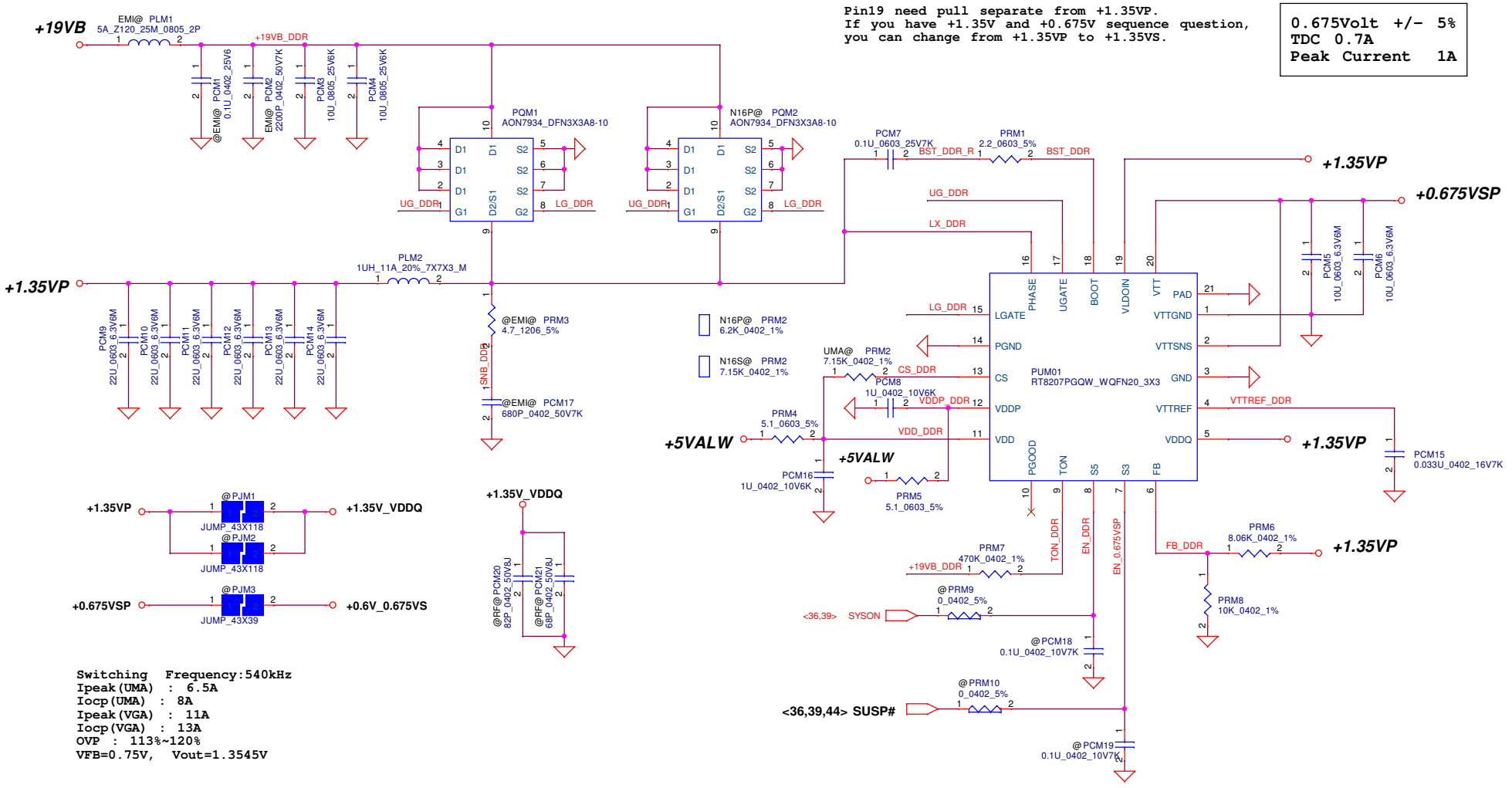
Title: *3VALW/5VALW*

Size	Document Number	Rev
Custom	LA-C501P	0.1

Date: | Sheet 53 of 61



Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Switching Frequency:540kHz
Ipeak(UMA) : 6.5A
Iocp(UMA) : 8A
Ipeak(VGA) : 11A
Iocp(VGA) : 13A
OVP : 113%~120%
VFB=0.75V, Vout=1.3545V

MOSFET: 3x3 DFN
H/S Rds(on): 12.4mohm(Typ), 15.8mohm(Max)
Idsm: 13A@Ta=25C, 7.8A@Ta=70C

L/S Rds(on): 9.4mohm(Typ), 11.6mohm(Max)
Idsm: 15A@Ta=25C, 9A@Ta=70C

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: 1.35V/0.675VS

Size	Document Number	Rev
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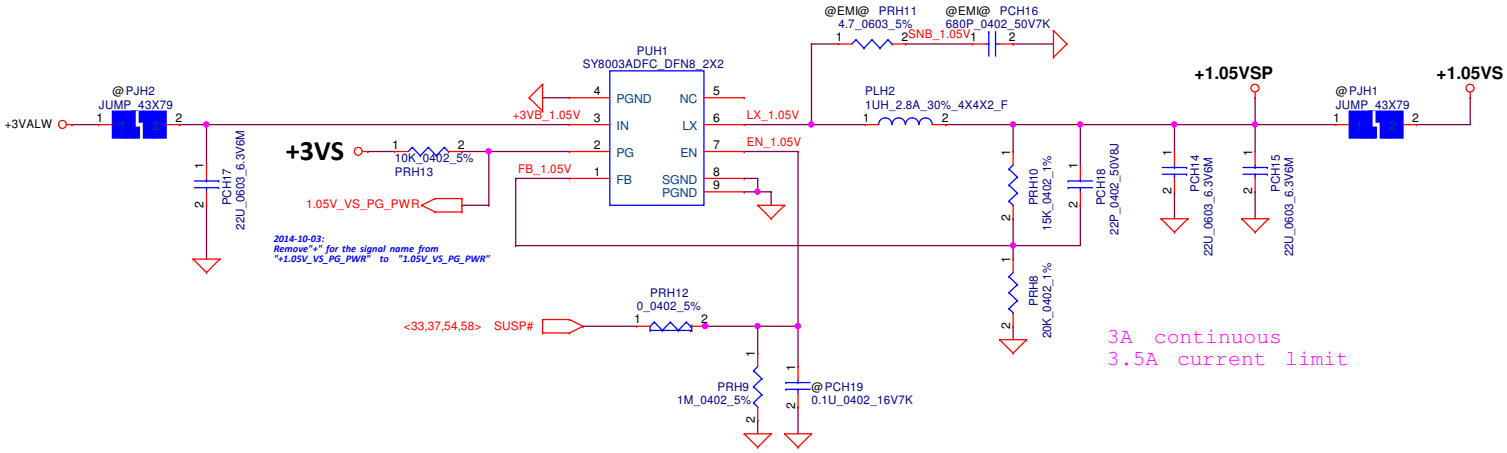

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Title	*1.05V*	
Size	Document Number: **LA-C501P**	Rev: 0.1
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Module model information:
ISL95813_V1A for IC module
ISL95813_V1B for SW module

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.15UH (Size:7*7*3)
Rdc=0.66mohm +-7%
Heat Rating Current=36A

ITDC=10A
ICCMAX=32A
OCP=38A
Fsw=700kHz

Follow intel guideline

+1.05VS_VCCST

PRZ1 130_0402_1%
PRZ2 54.9_0402_1%
PCZ1 1U_0402_6.3V6K

Note:
VR_SVID_ALRT#
Pull high on HW side

<11> VR_SVID_DAT
<11> VR_SVID_ALRT#
<11> VR_SVID_CLK
<11> VR12.5_VR_ON

+1.05VS_VCCST
@ PRZ22 1.5K_0402_1%
PRZ4 1.5K_0402_1%
<11> VGATE

PRZ3 90.9K_0402_1%

Note:
PRZ3=90.9K
=>ICCMAX=33A
Fsw=700kHz
ECO mode

PUZ1
ISL95813HRZ-T_QFN20_3X4

1	VR_ON	LGATE	16
2	PGOOD	PHASE	15
3	IMON	UGATE	14
4	VR_HOT#	BOOT	13
5	NTC	VCC	12
6	COMP	PRGM2	11
7	FB	ISUMP	10
8	RTN	ISUMN	9
17	PRGM1	SDA	18
		ALERT#	19
		SCLK	20
		PAD	21

PCZ7 1000P_0402_50V7K
PRZ6 110K_0402_1%
IMON_CPU
VR_HOT#
<33> VR_HOT#
PHZ1 470K_0402_5%_B25/50 4700K
PRZ10 3.83K_0402_1%
NTC_CPU
PRZ11 27.4K_0402_1%
PCZ9 47P_0402_50V8J
COMP_CPU

Note:
VR_HOT# Pull high on HW side

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PRZ5 0_0603_5%
PRZ7 2.2_0603_5%
PCZ8 0.22U_0603_16V7K
BST_CPU
BST_CPU_R
LG_CPU
LX_CPU
UG_CPU
PRGM2_CPU
PCZ11 0.1U_0402_25V6
+5VS

PRZ12 124K_0402_1%

Note:
PRZ12=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PQZ1 MDV1525URH_PDFN33-8-5
PQZ3 P6632BA_PDFN8-5

change to AON6794
(SB000017Q00)

+19VB_CPU
+19VB
EMI@ PLZ01 5A_Z120_25M_0805_2P
@EMI@ PLZ3 5A_Z120_25M_0805_2P

PCZ2 10U_0805_25V6K
PCZ3 10U_0805_25V6K
@RF@ PCZ23 68P_0402_50V8J
@RF@ PCZ24 2.2U_0402_25V6M
@EMI@ PCZ4 0.1U_0402_25V6
EMI@ PCZ5 2200P_0402_50V7K
@PCZ31 33U_D2_25M_R60M
@PCZ32 33U_25V_NC_6.3X4.5
PCZ33 33U_25V_NC_6.3X4.5

PLZ2 0.15UH_29A_+-20%_7X7X4_M
+VCC_CORE

@EMI@ PRZ8 4.7_1206_5%
@EMI@PCZ10 680P_0603_50V8J

ISUMP_CPU_R
ISUMN_CPU_R

PRZ9 3.65K_0603_1%
PRZ18 4.32K_0402_1%
PRZ19 11K_0402_1%
PHZ2 10K_0402_5%_B25/50 4250K
PCZ17 0.1U_0402_16V4Z

RC Match
PCZ16 0.01U_0402_25V7K

PRZ13 3.16K_0402_1%
PCZ13 6800P_0402_25V7K
PCZ12 33P_0402_50V8J
FB_CPU
@PRZ14 2K_0402_1%
@PRZ15 10_0402_1%
@ PCZ14 390P_0402_50V7K
@ PCZ15 330P_0402_50V7K
PRZ16 1.27K_0402_1%
Droop

PRZ17 4.99M_0402_1%

OCP Setting
PRZ20 280_0402_1%

<11> VCCSENSE
@PCZ18 330P_0402_50V7K
PCZ20 0.01U_0402_50V7K
@PCZ19 0.082U_0402_16V7K
<13> VSSSENSE

@PCZ21 4700P_0402_25V7K
@PRZ21 1.5K_0402_1%

Local sense put on HW site

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Issued Date	2014/10/09	Deciphered Date	2015/12/31

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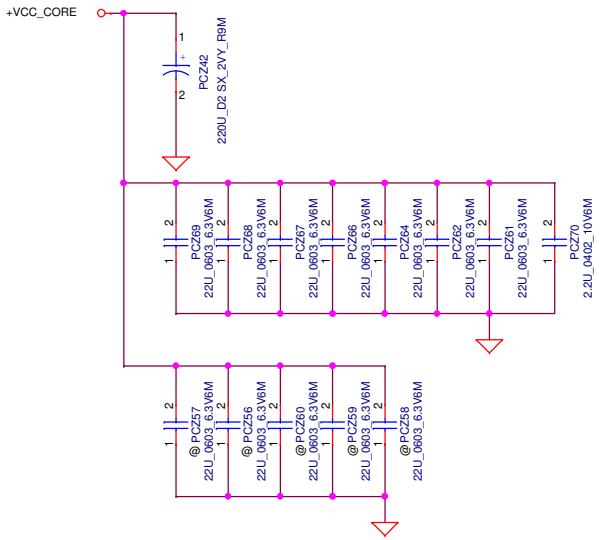
Title: VCC_CORE
Size: | Document Number: LA-C501P for CN30 | Rev: 0.1
Date: Wednesday, April 22, 2015 | Sheet 56 of 61



BDW-U 15W
220uF X 1
22uF X7
2.2uF X1

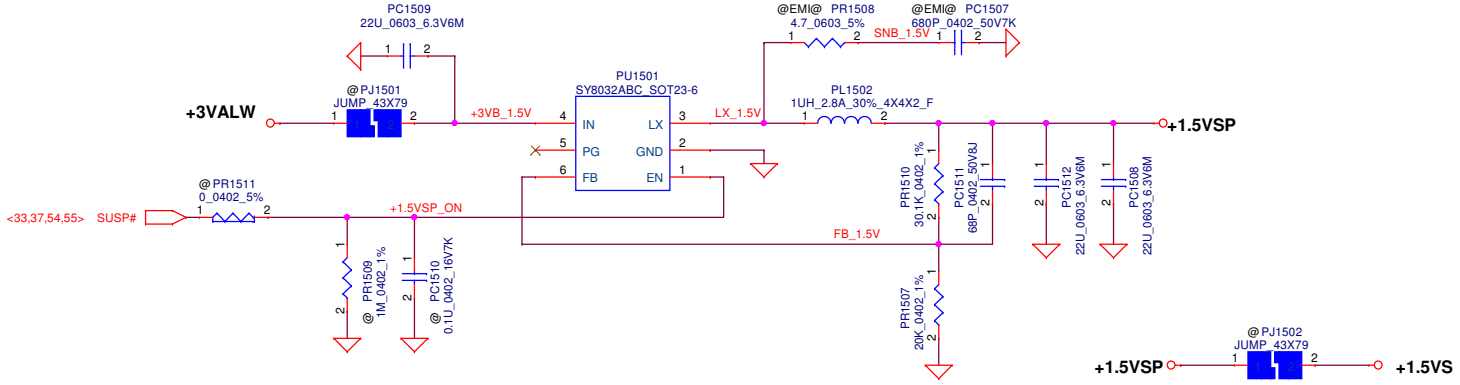
Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	LA-C501P For CN30	0.1

Date: | Sheet 57 of 61



continuous 2.5A

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

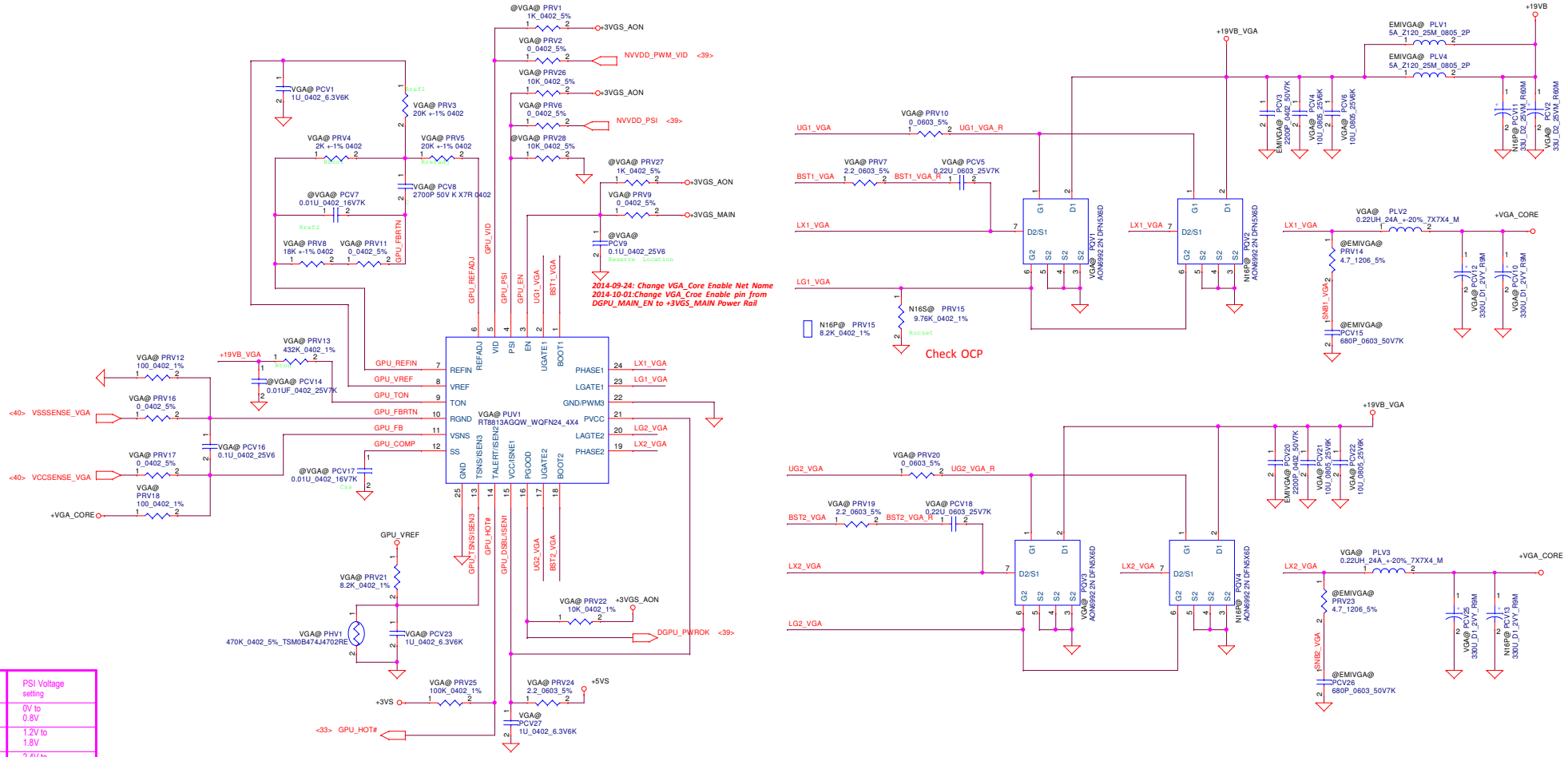
Compal Electronics, Inc.

Title	*1.5VS*	
Size	Document Number: LA-C501P	Rev: 0.1
Date: Wednesday, April 22, 2015	Sheet 58 of 61	

H-side MOS: AON6992
Rds(on):
4.3mohm@Vgs=10V
5.2mohm@Vgs=4.5V
Id :32A@Tc=100C

L-side MOS: AOS6992
Rds(on):
2mohm@Vgs=10V
2.2mohm@Vgs=4.5V
Id :66A@Tc=100C

Choke: 0.22UH (Size:7*7*3)
Rdc=0.98mohm +-5%
Heat Rating Current=28A



Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

1. VSNS Soft-Start time (Internal) is 0.7ms (PCV17 un-pop)
   Tss=(Css*Vrefin)/Iss+2.3ms
   =0.01U*0.9V/5uA+2.3ms=4.1ms (PCV17 pop)

2. Switching frequency setting:
   Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=353Khz

3. Thermal monitoring:
   (VGPU_VREF-VTSNS)/PRV21=VTSNS/Rth

	T_min	T_typical	T_max
PRV21=18.7K	99.16C	101.57C	103.94C
PRV21=13K	110.19C	112.75C	115.26C
PRV21=8.2K	125.15C	127.91C	130.62C

Switching Frequency : 353kHz
Ipeak(N16P-GT) : 70A
Iocp(N16P-GT) : 83A
Ipeak(N16-S-GT) : 50A
Iocp(N16S-GT): 61A

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Issued Date	2014/10/09	Deciphered Date	2015/12/31

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Title: **VGA_CORE**

Size	Document Number	Rev
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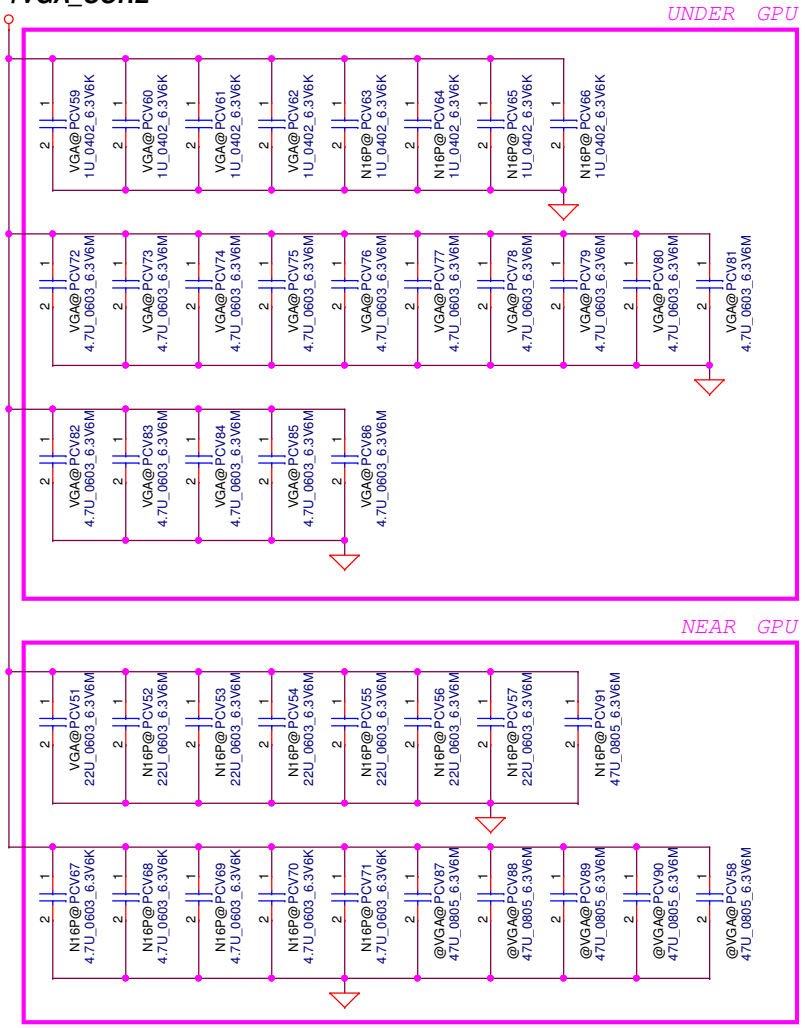
+VGA_CORE




```
N16S-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 3
47U 6.3V X5R 0805 (SE00000PL00) X 1
22U 6.3V X5R 0603 (SE00000M000) X 1
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
1U 6.3V X5R 0402 (SE000000K80) X 4

N16P-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 4
22U 6.3V X5R 0603 (SE00000M000) X 7
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
4.7U 6.3V X5R 0603 (SE107475K80) X 5
1U 6.3V X5R 0402 (SE000000K80) X 8
```

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

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Title: VGA CHIP DECOUPLING

Size	Document Number	Rev
B	LA-C501P	0.1

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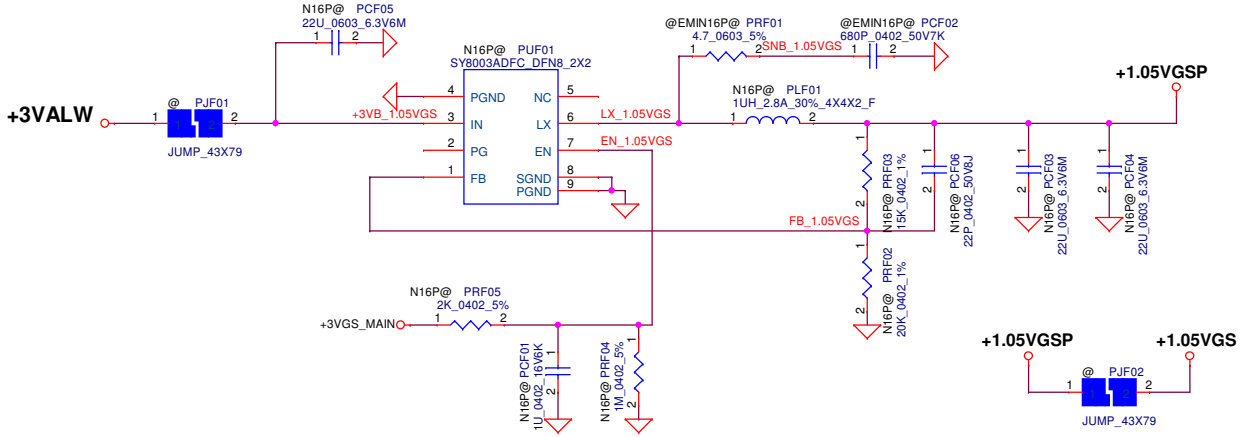
For Nvdia N16P-GT



3A continuous
3.5A current limit

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: 1.05VGS

Size: Custom | Document Number: LA-C501P | Rev: 0.1

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **PWR-PIR**

Size: Custom | Document Number: **<Doc>** | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 62 of 63

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME request	0.2	P19	Change eDP Connector(JLCD1) for ME	12/15	
2		Screw Hole	0.2	P32	Change H20 from 3.0 mm to 3.3 mm	12/15	
3		Sub USB Power Switch	0.2	P26	Change Power Switch US5 circuit	12/15	
4		ME Flash Circuit	0.2	P6	Add ME FLASH Circuit	12/15	
5		Audio GND Bridge circuit	0.2	P28	Add two Resistor for HP request	12/15	
6		Add JUMP on JUSB1 and JUSB2 Power	0.2	P26	Add JUMP JPV5	12/19	
7		ESD request	0.2	P34	Change Touch PAD Diode for ESD request	12/19	
8		ESD request	0.2	P19	Reserve Touch Screen Diode for ESD	12/19	
9		ESD request	0.2	P19	Change Camera and D-MIC Diode for ESD request	12/19	
10		Audio team Request	0.2	P28	Change JSPK2 Pin define	12/22	
11		Vendor Request	0.2	P31 P33	Change Subwoofer circuit	12/22	
12		Customer Request	0.2	P35 P33	Add Shipping Mode Circuit	12/22	
13		RF Request	0.2	P26 P32	Reserve 68P and 82P on +3VALW and +USB_VCC4	12/23	
14		ESD request	0.2	P20	Change HDMI EMI Solution	12/23	
15		HW Modify	0.2	P48	Change N16X 1.35V and 1.05V solution	12/25	
16		HW Modify	0.3	P48	Change N16X 1.35V and 1.05V solution	01/23	
17		HW Modify	1.0	P32	Add DH5 for storage Mode	04/02	
18		Vendor Request	1.0	P31	Change Subwoofer circuit	04/02	
19		HW Modify	1.0		Change 0 ohm to short pad. RC8,RC108,RC119,RC378, RT19,RT37,RA32,RA34, RA38,RA39,RA50,RA51, RT17 RT18,RTS4	04/13	

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