LCFC Confidential

Tiny6 GH470 MB Schematics Document
Intel Comlet Lake-S CPU+Comlet Lake-H PCH

2020-01-01

REV:1.0

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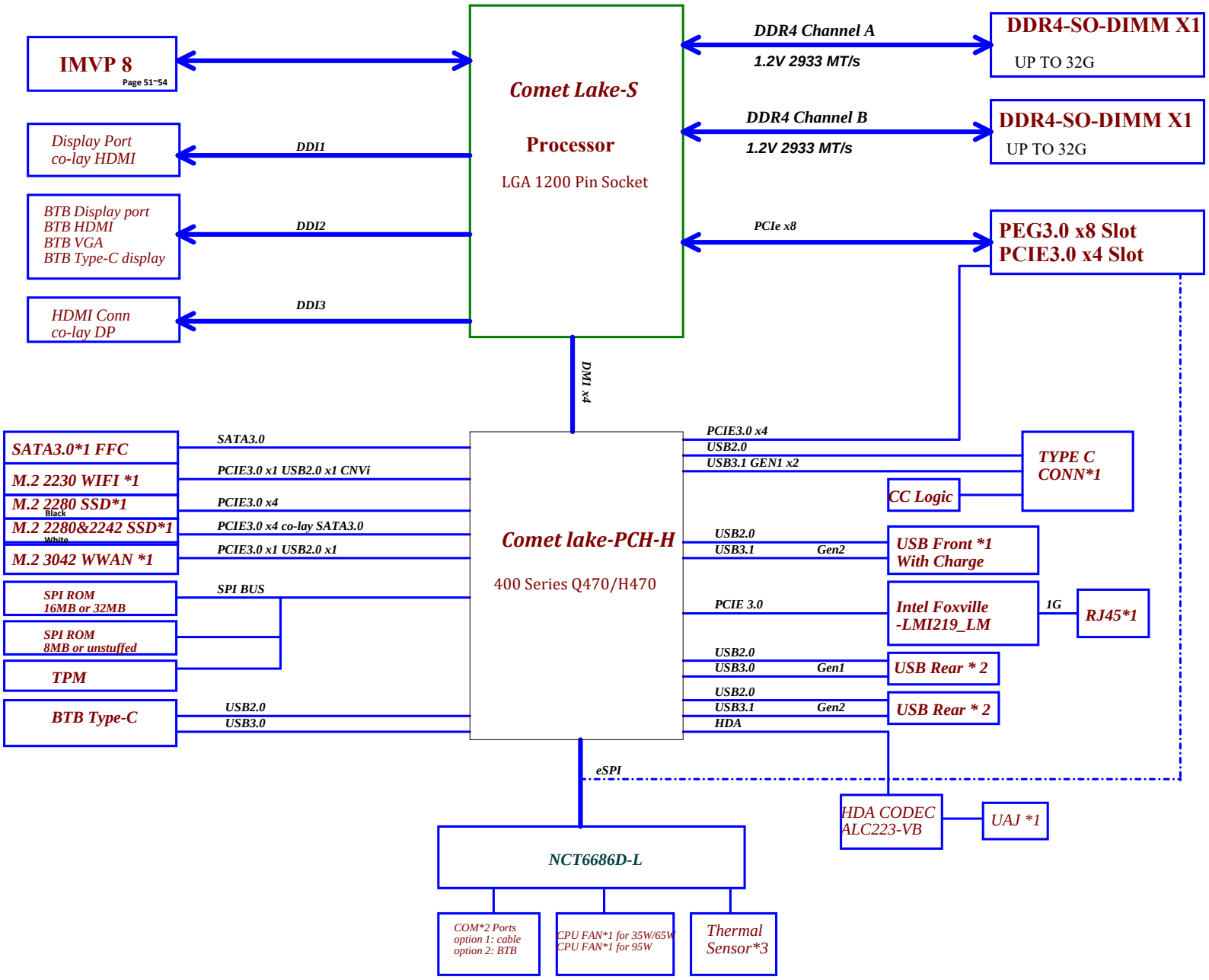
File Name : Tiny6 SVT

Board Number : NM-C901

PN : DA600017510



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Title	Block Diagram		
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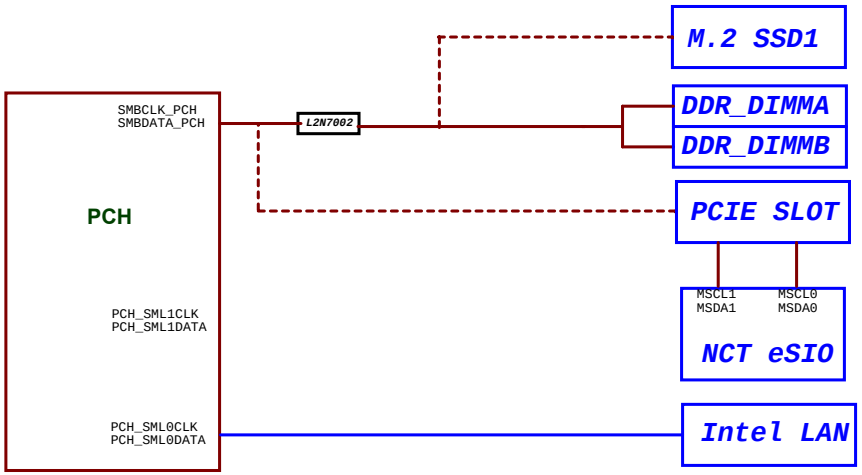
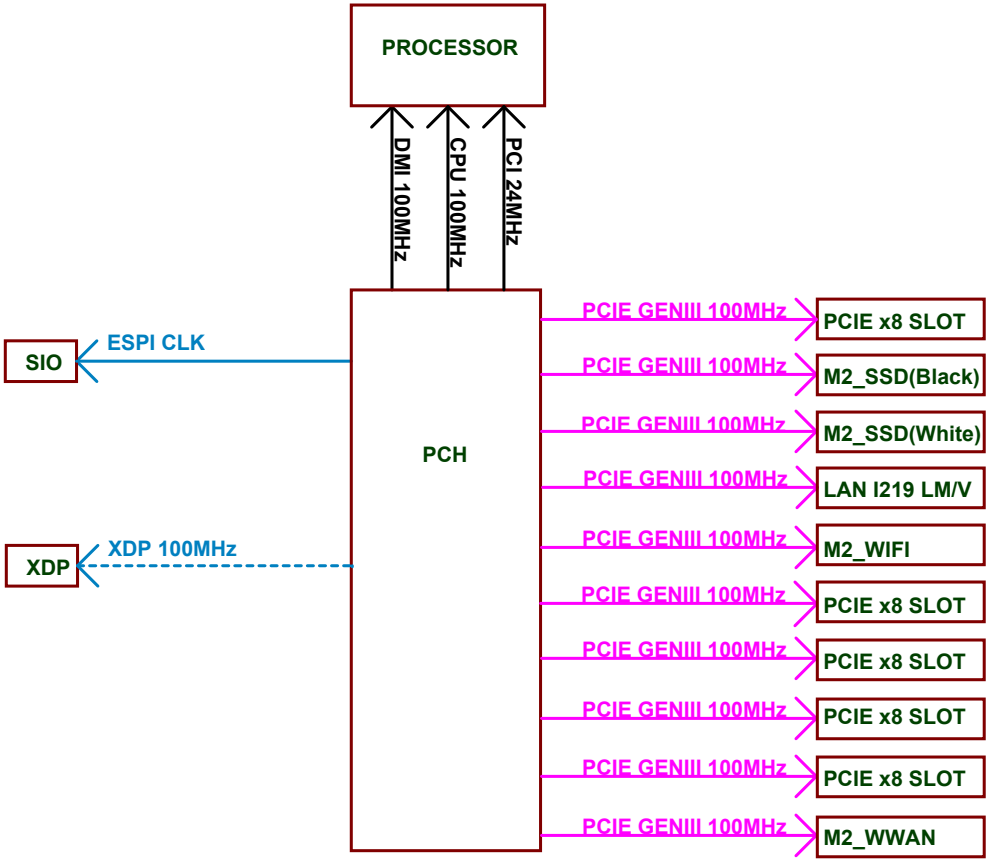
SMBUS Block Diagram

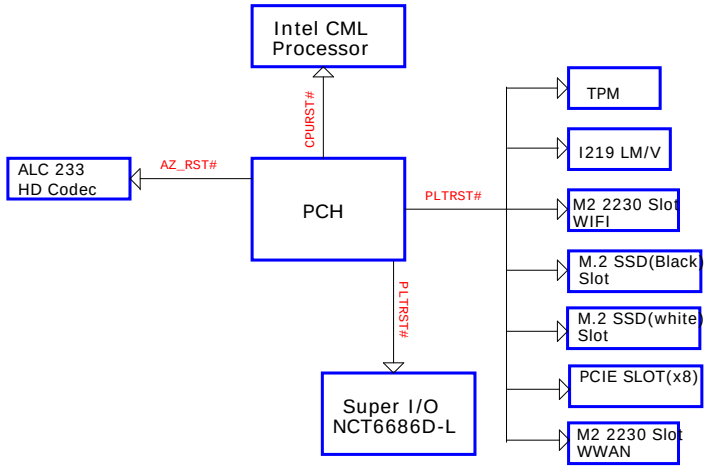


BOM Structure	BTO Item
@	Not stuff
Q490@	For Q490 SKU (M90Q,M80Q,NEC Q490,WS Tiny), 32M SPI ROM
H470@	For H470 SKU
DEBUG@	For NPI debug need
BMC@	For BMC part
DP1@	For 1st DP colay HDMI port, DP SKU part
DP2@	For 2nd DP colay HDMI port, DP SKU part
HDMI1@	For 1st DP colay HDMI port, HDMI SKU part
HDMI2@	For 2nd DP colay HDMI port, HDMI SKU part
EMC@	For EMC part
EMC_NS@	For EMC nu-stuff part
PCIEX8X4@	For PCIE X8/X4 part
SYSFAN@	For System FAN part£¬only reserved
MS@	For Modern Standby function
SSD2@	For M.2 SSD(Black) PCIE part, only M920X(Q370) need
M2_EXP@	For M.2 SSD(White) docking function need
ME@	For ME part
DOTLED@	For NEC DOT LED remove
HDMILOGO@	HDMI LOGO
BATTERY@	Battery cell
SPIROM@	For 45J SPI ROM

CLOCK MAP



RESET MAP



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Title	Notes List		
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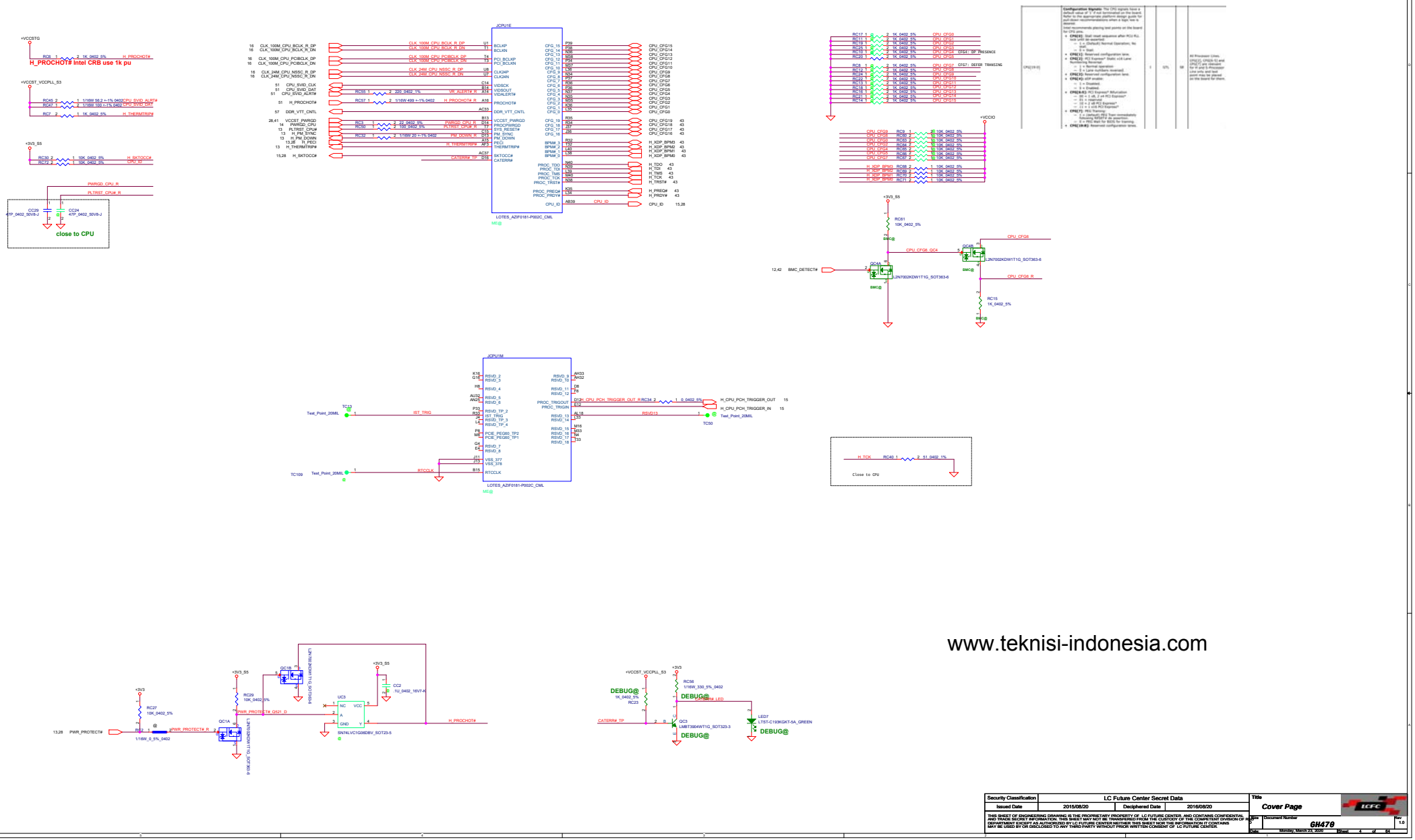

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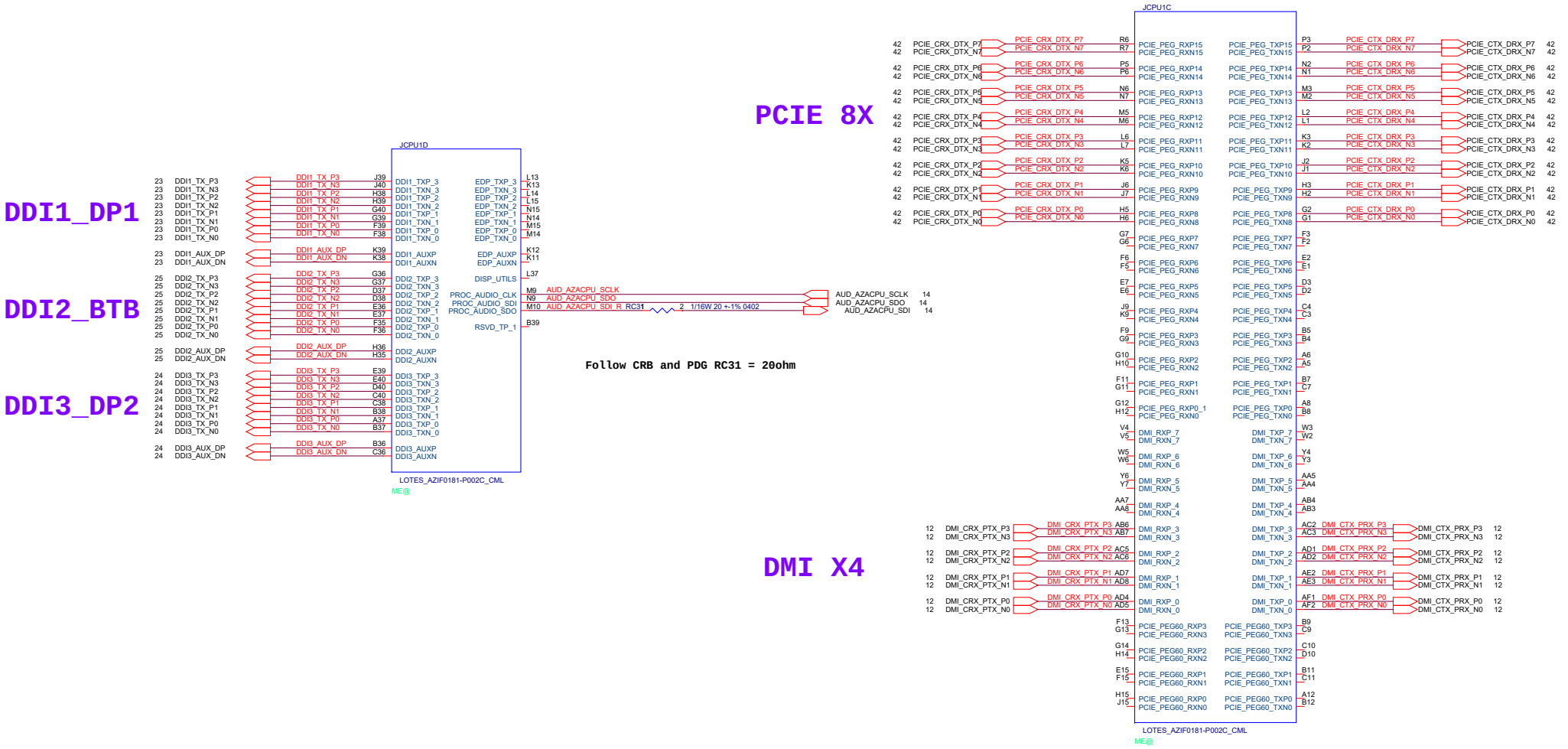

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Title: CPU (PEG,DMI,DDI,EDP)

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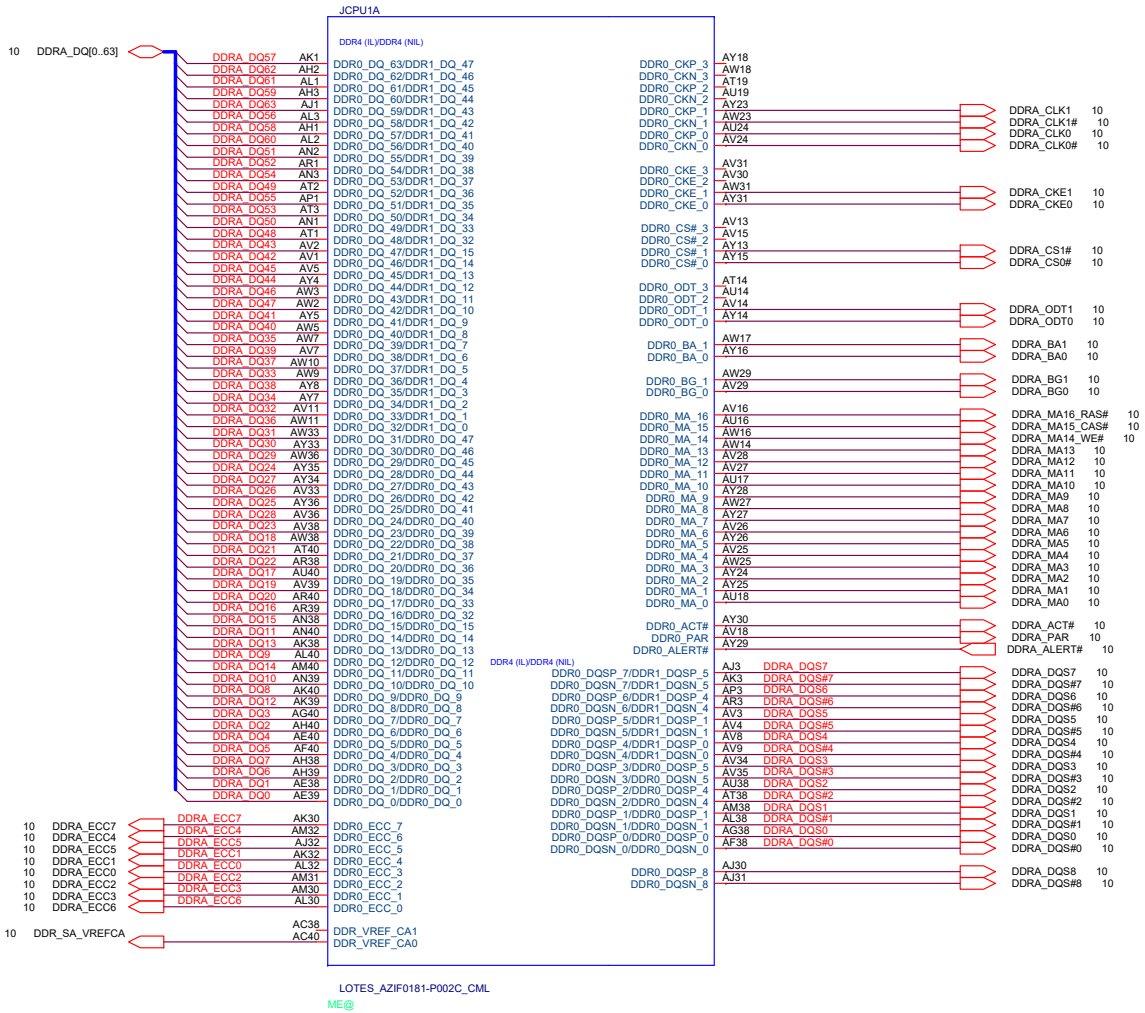
SO-DIMM DDR4 CHA



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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CPU (DDR4-CHA)

Size	Document Number	Rev
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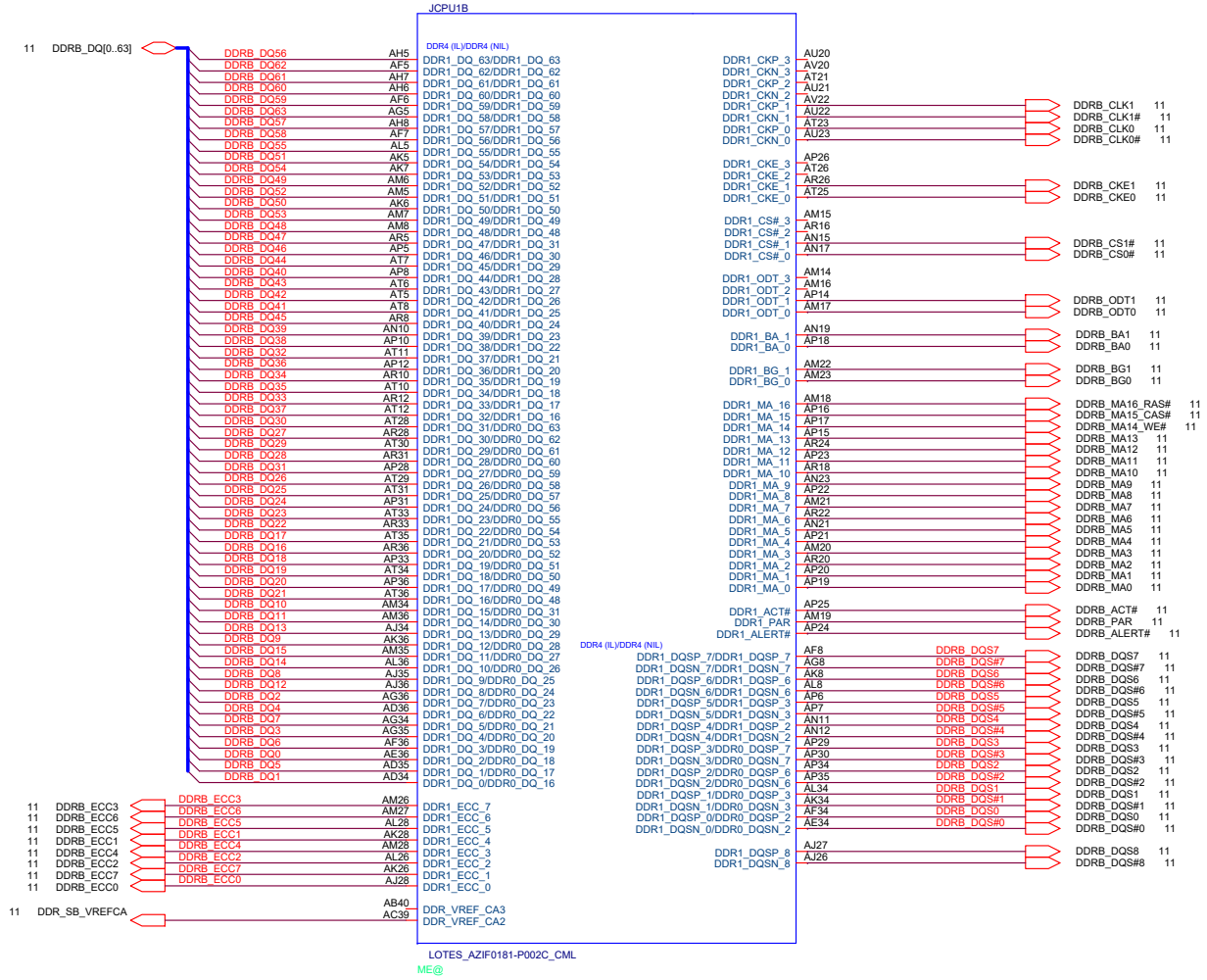
SO-DIMM DDR4 CHB



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Title: CPU (DDR4-CHB)

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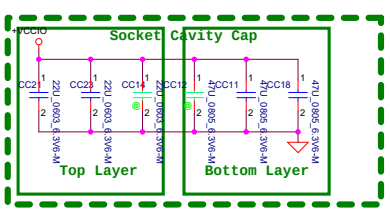

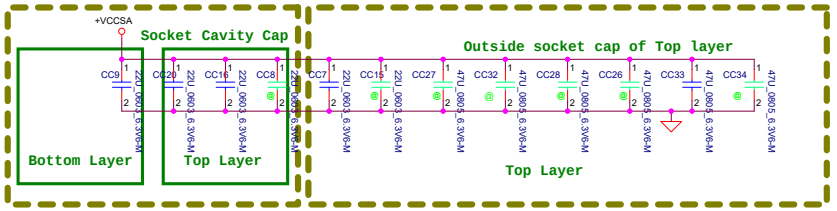

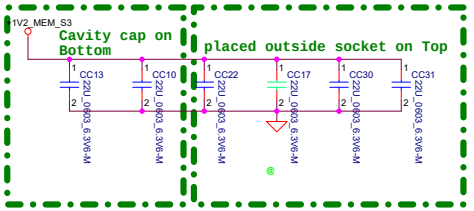

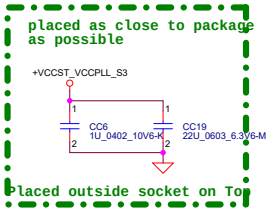

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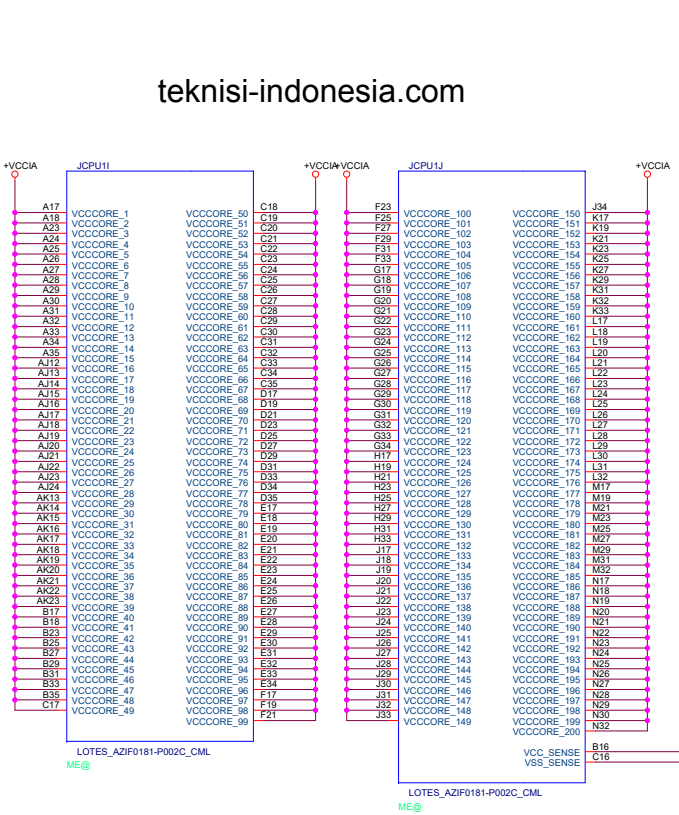

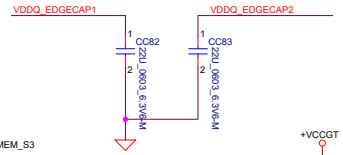

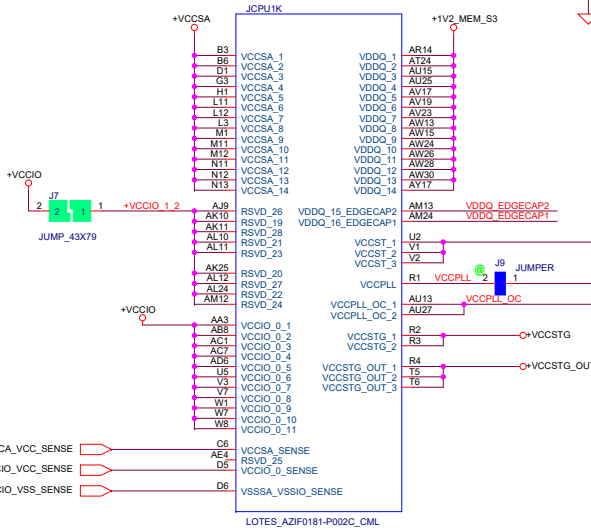

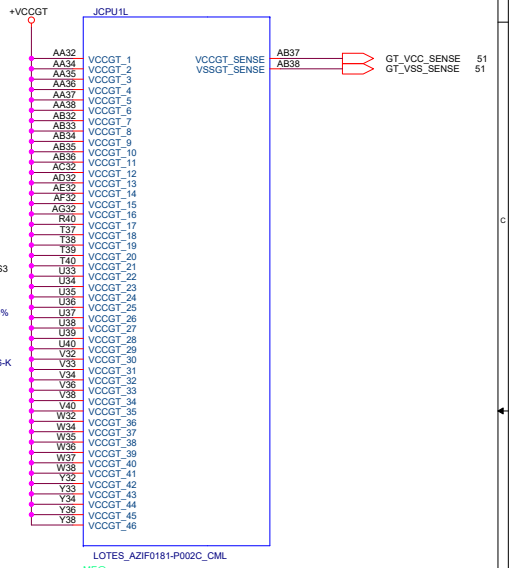

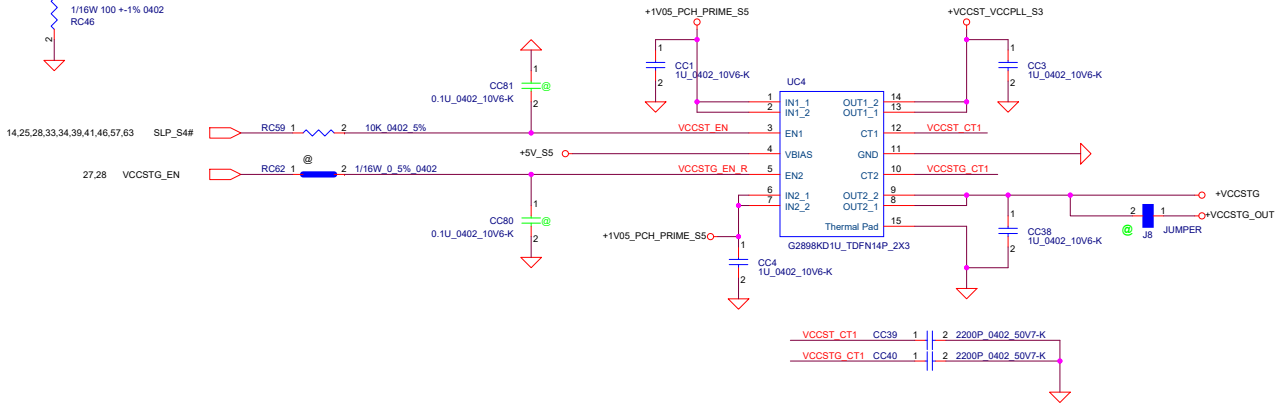

Table 50-3. Decoupling Requirements for CFL S Processor

Domain	Cavity cap	Outside socket cap	Topside/ Bottom side	Placement guideline and notes
Vcc	12x 22uF 0805		Top	
	6x 22uF 0603		Top	
		5x 22uF 0805	Top	
V_{CCGT}	8x 47uF 0805		Top	
		4x 47uF 0805	Top	
V_{CCSA}	4x 22uF 0603		Top	
		2x 22uF 0603	Top	
		4x 47uF 0805	Top	
V_{DDQ}		4x 22uF 0603	Top	
V_{CCIO}	5x 22uF 0603		Top	
	1x 22uF 0805		Top	
V_{CCST}	1x 22uF 0805		Top	Merged with VccPLL; VccST and VccSTG merged on package. Capacitors placed as close to package as possible
	1x 1uF 0402		Top	
V_{CCPLL_OC}	1x 1uF 0402		Top	

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Title: **CPU(CPU POWER)**

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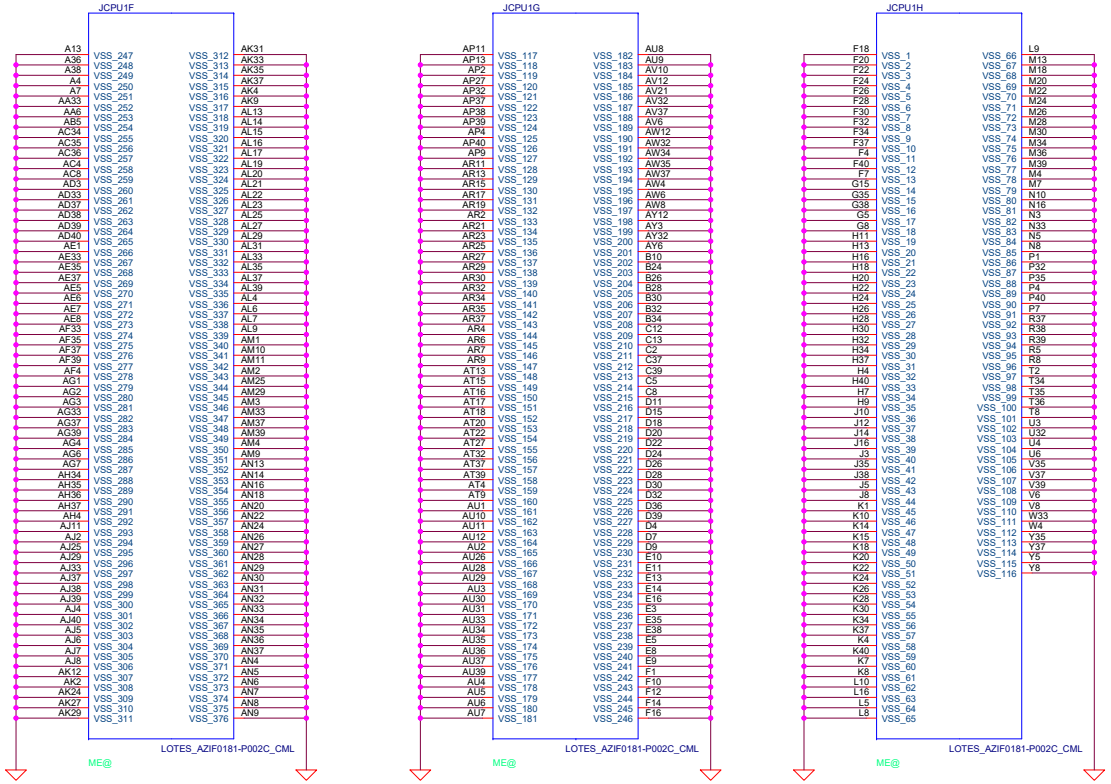

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Title	CPU(VSS)		
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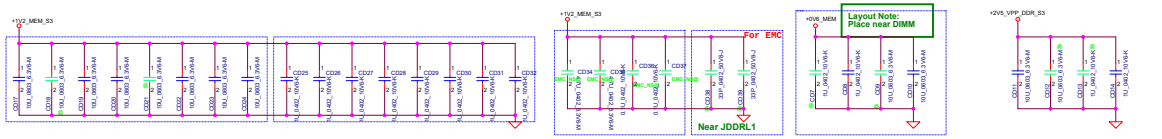
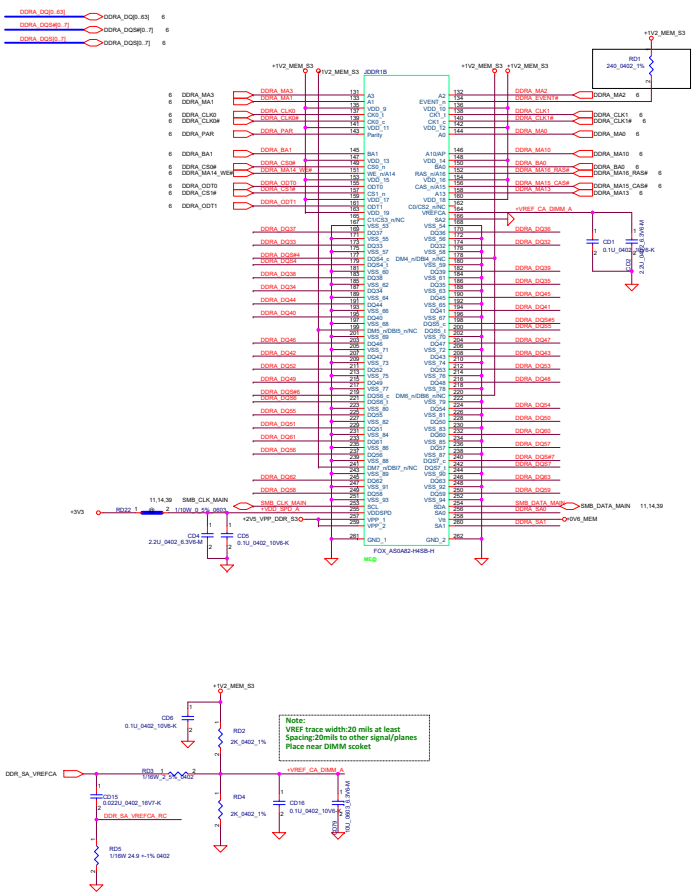
DDR4 SO-DIMM





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Title: DDR4 CHA SO-DIMM1

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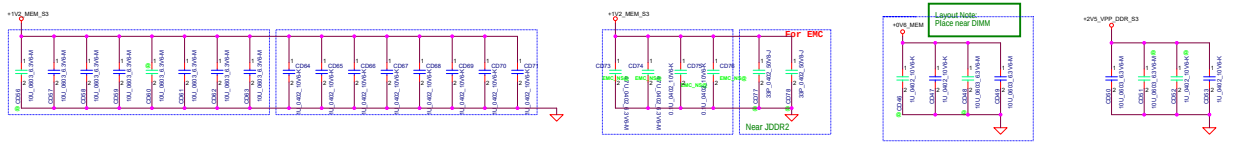

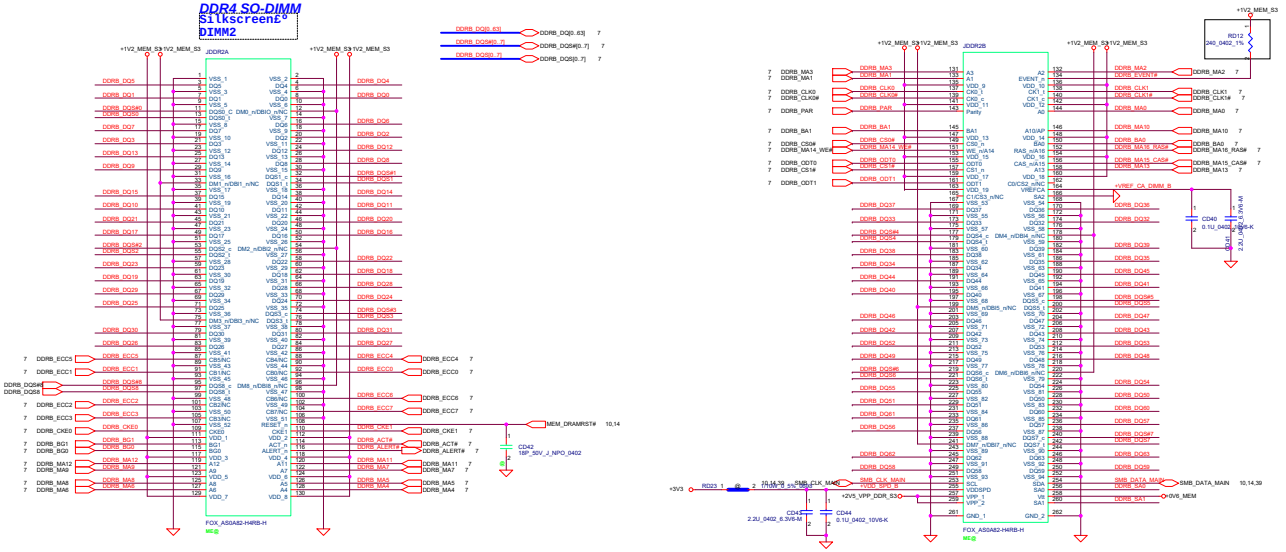

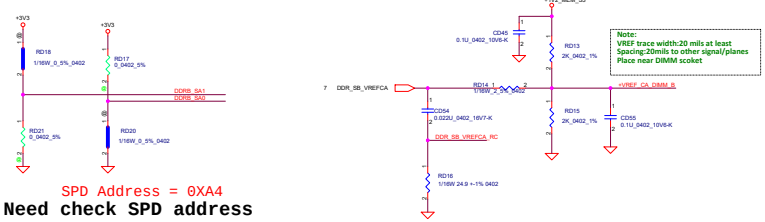

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Title: DDR4 CHB SO-DIMM2

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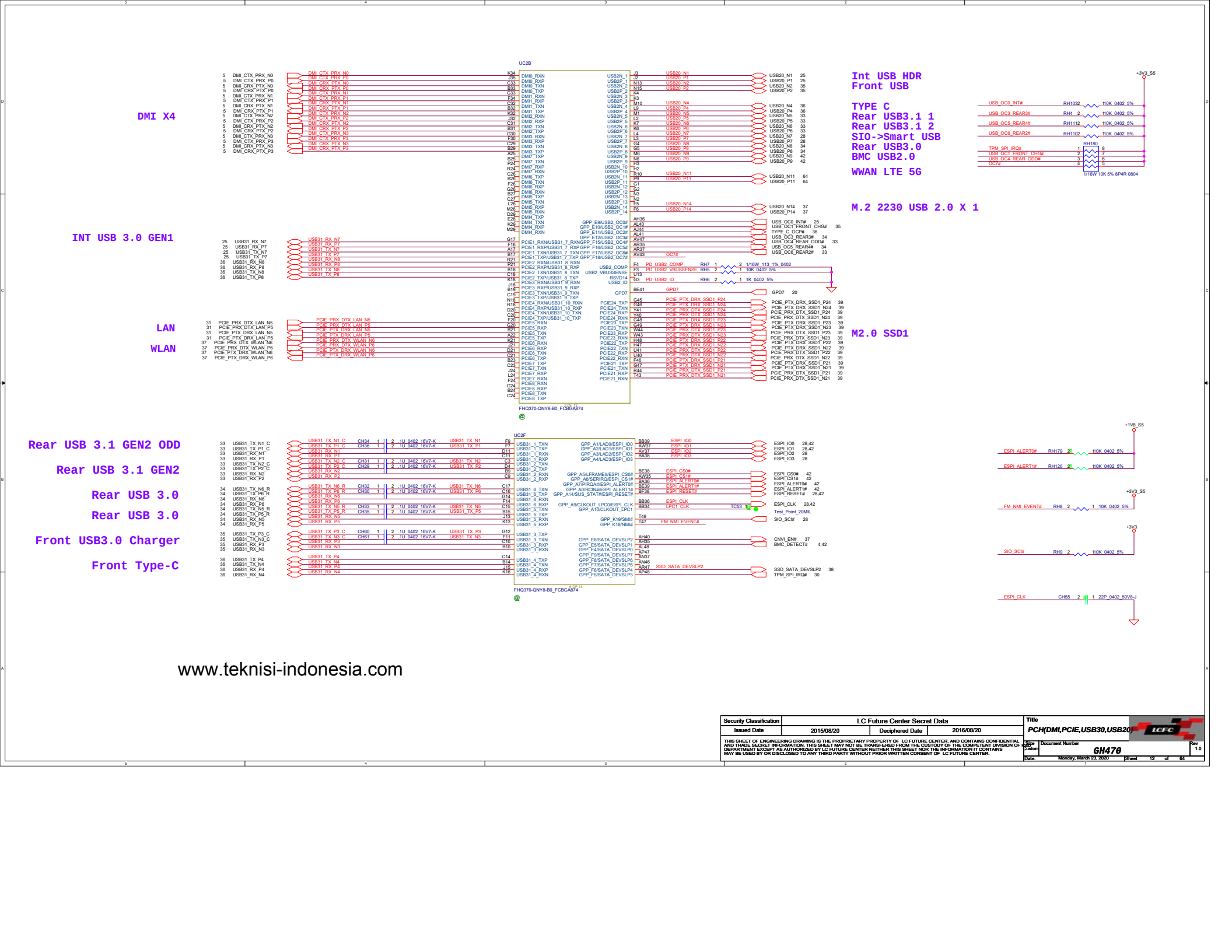

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Title	PCH(DMI,PCIE,USB30,USB20)		
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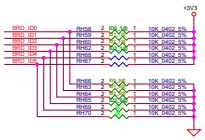

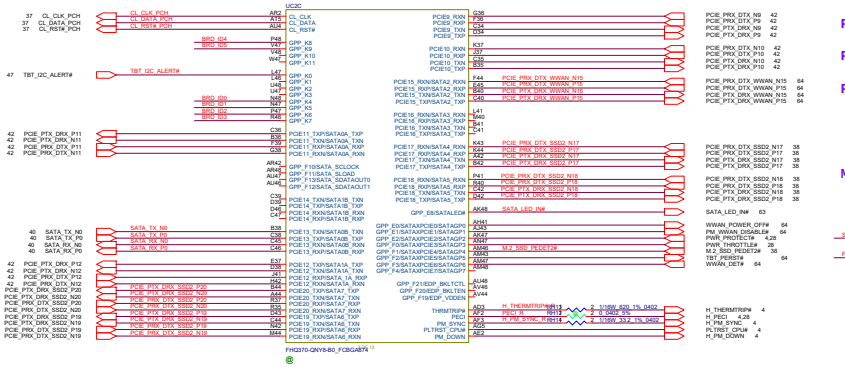

PCIEX4 for SLOT

PCIEX4 for SLOT

PCIEX4 for WWAN

PCIEX4 for SLOT

SATA FFC Cable

PCIEX4 for SLOT

M.2_2280_SSD#2 Black

M.2_2280_SSD#2 Black

Tiny6	PCH GPIO	Chipset	ME FW	GPP_K9	GPP_K8	GPP_K7	GPP_K6	GPP_K5	GPP_K4
	Board ID MAP			ID5	ID4	ID3	ID2	ID1	ID0
	P340 Workstation	Q470	Corp	1	1	0	0	0	0
	M90q LI	Q470	Corp	1	1	0	0	0	1
	M80q LI	Q470	Corp	1	1	0	0	1	0
	M80q LC	Q470	Corp	1	1	0	0	1	1
	M70q LI	H470	Consumer	1	1	0	1	0	0
	M70q LC	H470	Consumer	1	1	0	1	0	1
	NEC M80q	Q470	Corp	1	1	0	1	1	0
	NEC M70q	H470	Consumer	1	1	0	1	1	1
	Tiny H550Q consumer	H470	Consumer	1	1	1	0	0	0
	Tiny Server	W480	Corp	1	1	1	0	0	1
	Tiny AIO V70	H470	Consumer	1	1	1	0	1	0
	Tiny Amazon	H470	Consumer	1	1	1	0	1	1

Figure 3-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

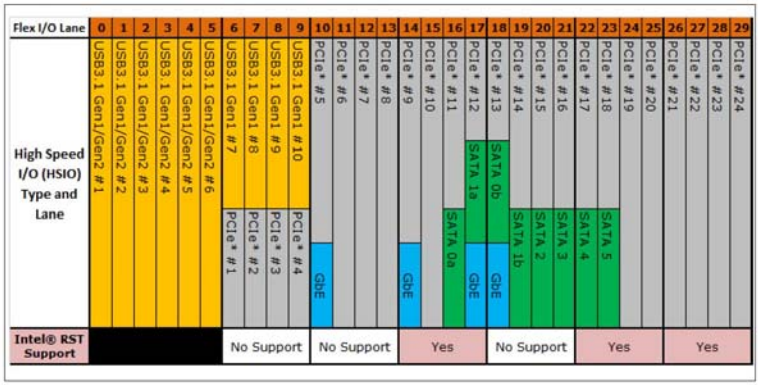

Table 4. Desktop PCH HSIO Details

Flex I/O Lane	SKU		
	Z490	H470	Q470
0	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)
1	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)
2	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)
3	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)
4	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1
5	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)/ USB 3.2 Gen 2x1 (10 Gb/s)
6	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)
7	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)	USB 3.2 Gen 1x1 (5 Gb/s)	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)
8	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)	PCIe	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)
9	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)	PCIe	PCIe;USB 3.2 Gen 1x1 (5 Gb/s)
10	PCIe*;GbE	PCIe*;GbE	PCIe*;GbE
11	PCIe*	PCIe*	PCIe*
12	PCIe*	PCIe*	PCIe*
13	PCIe*	PCIe*	PCIe*
14	PCIe*;GbE	PCIe*;GbE	PCIe*;GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*;SATA 0A	PCIe*;SATA 0A	PCIe*;SATA 0A
17	SATA 1A;PCIe*;GbE	SATA 1A;PCIe*;GbE	SATA 1A;PCIe*;GbE
18	SATA 0B;PCIe*;GbE	SATA 0B;PCIe*;GbE	SATA 0B;PCIe*;GbE
19	SATA 1B;PCIe*	SATA 1B;PCIe*	SATA 1B;PCIe*
20	SATA 2;PCIe*	SATA 2;PCIe*	SATA 2;PCIe*
21	SATA 3;PCIe*	SATA 3;PCIe*	SATA 3;PCIe*
22	SATA 4;PCIe*	SATA 4	SATA 4;PCIe*
23	SATA 5;PCIe*	SATA 5	SATA 5;PCIe*
24	PCIe*	PCIe*	PCIe*
25	PCIe*	PCIe*	PCIe*
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

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Title: PCH(PCIE,SATA,C LINK,GPIO)

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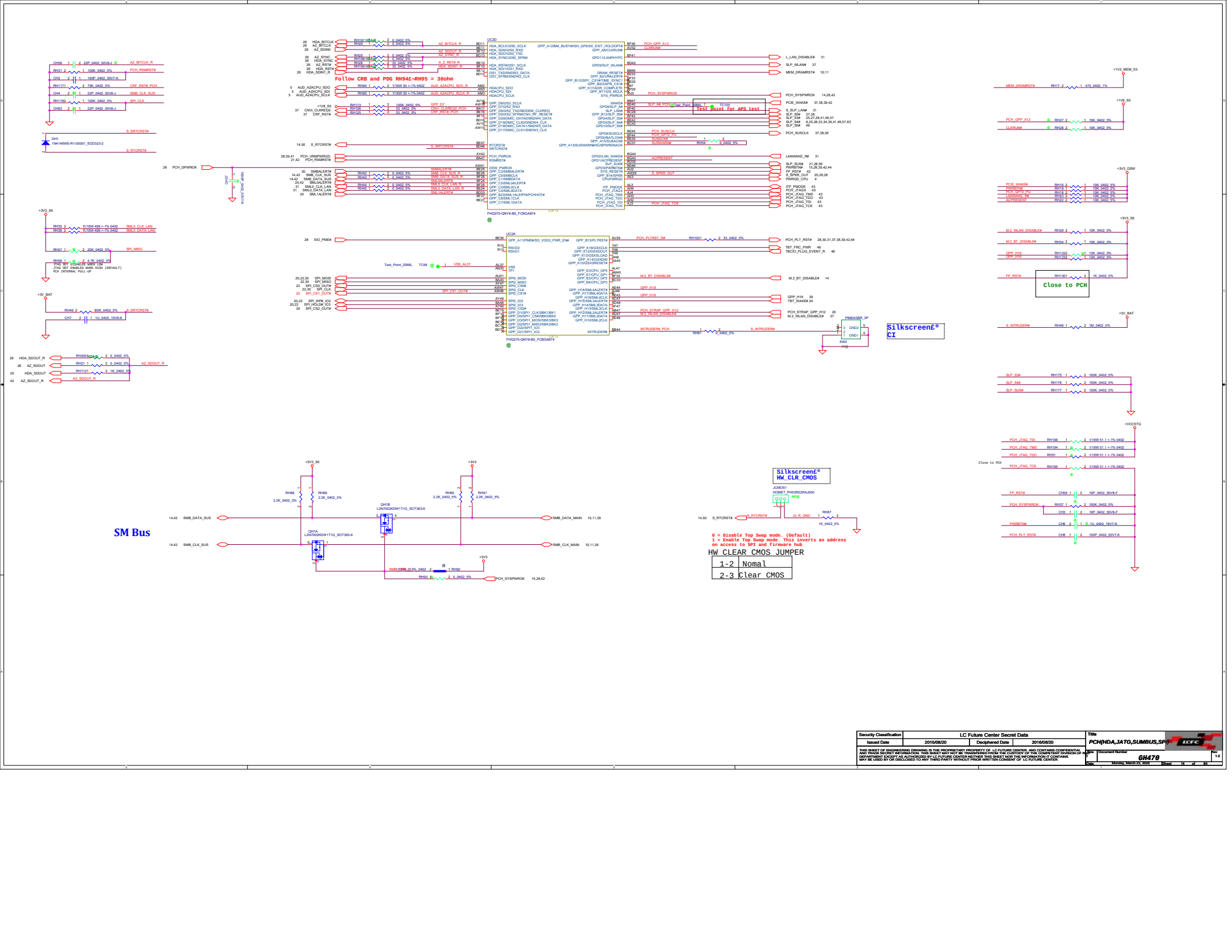

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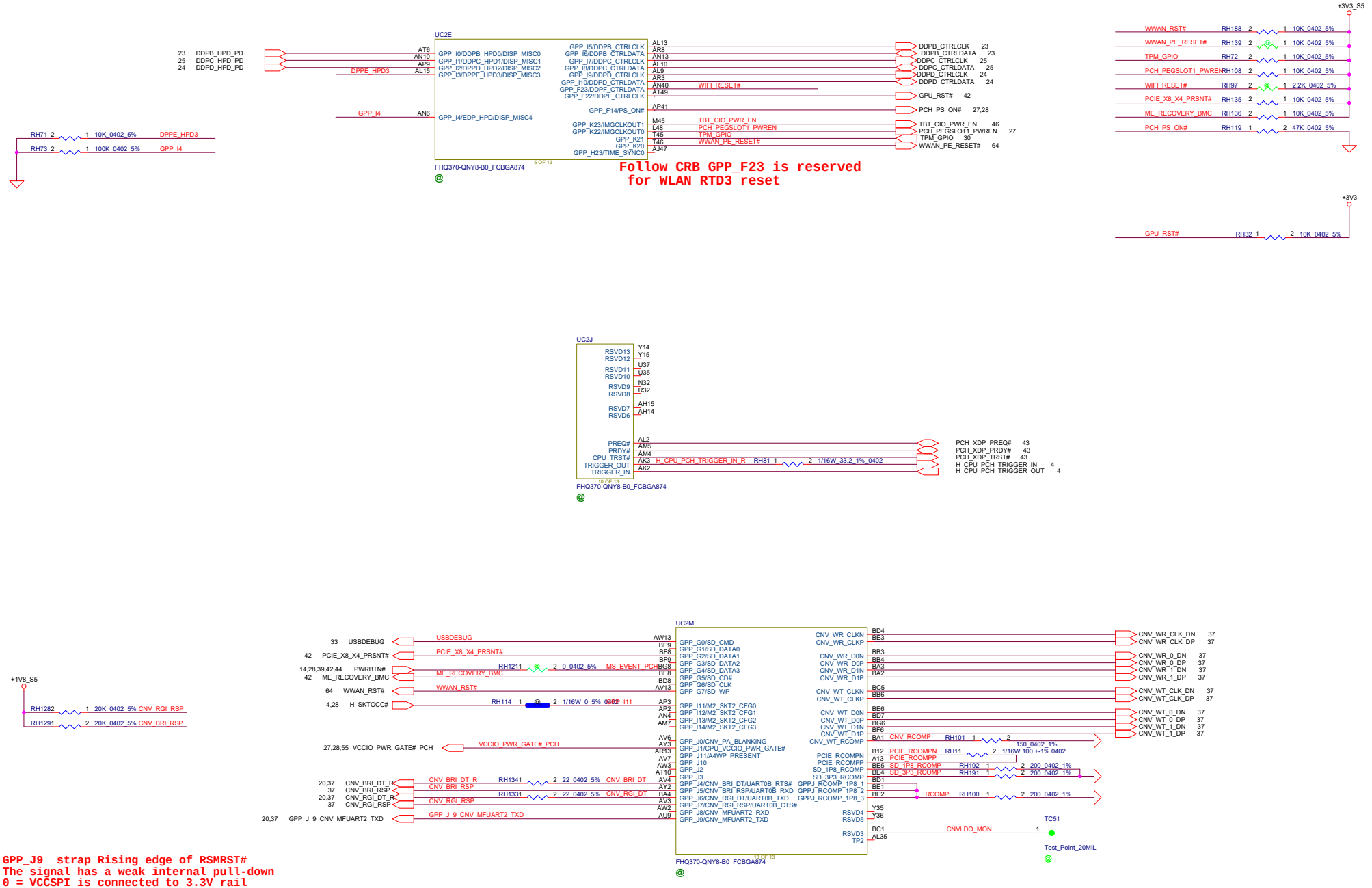

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Title: PCH(DDP,CNVi,XDP)

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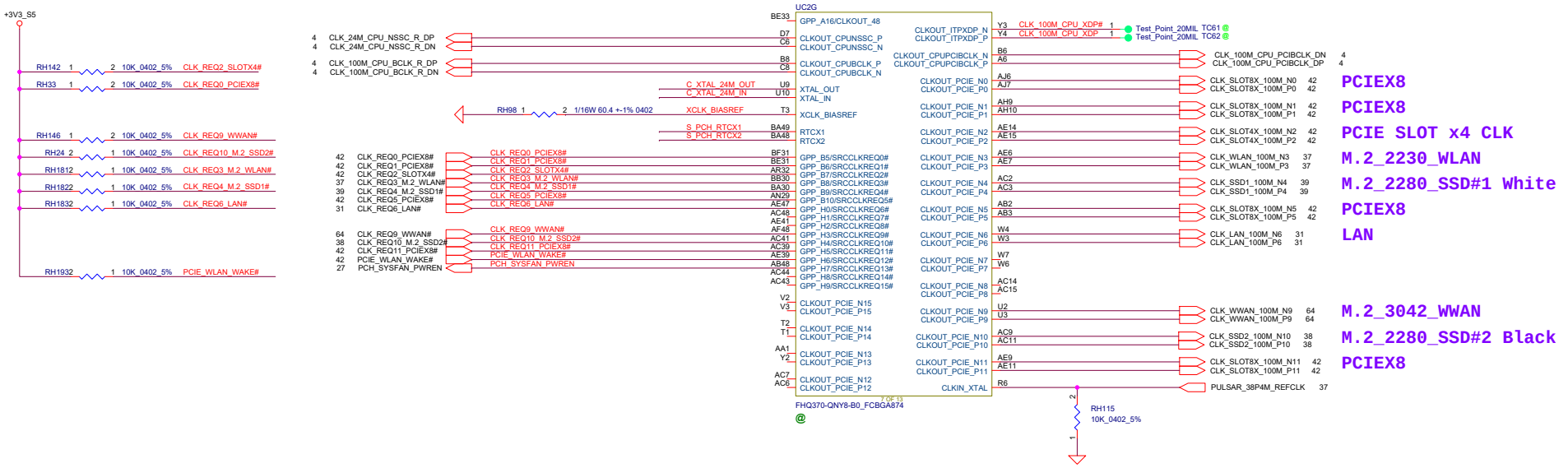
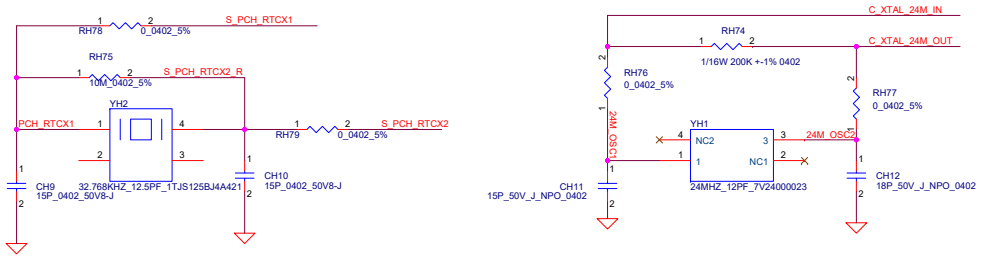
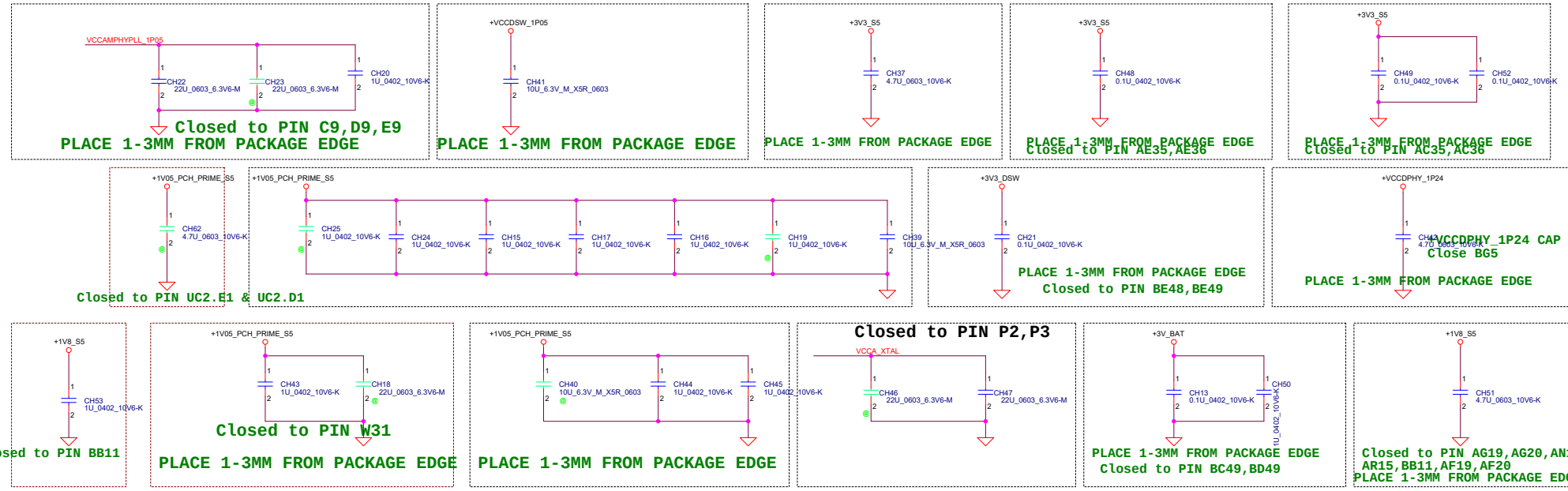


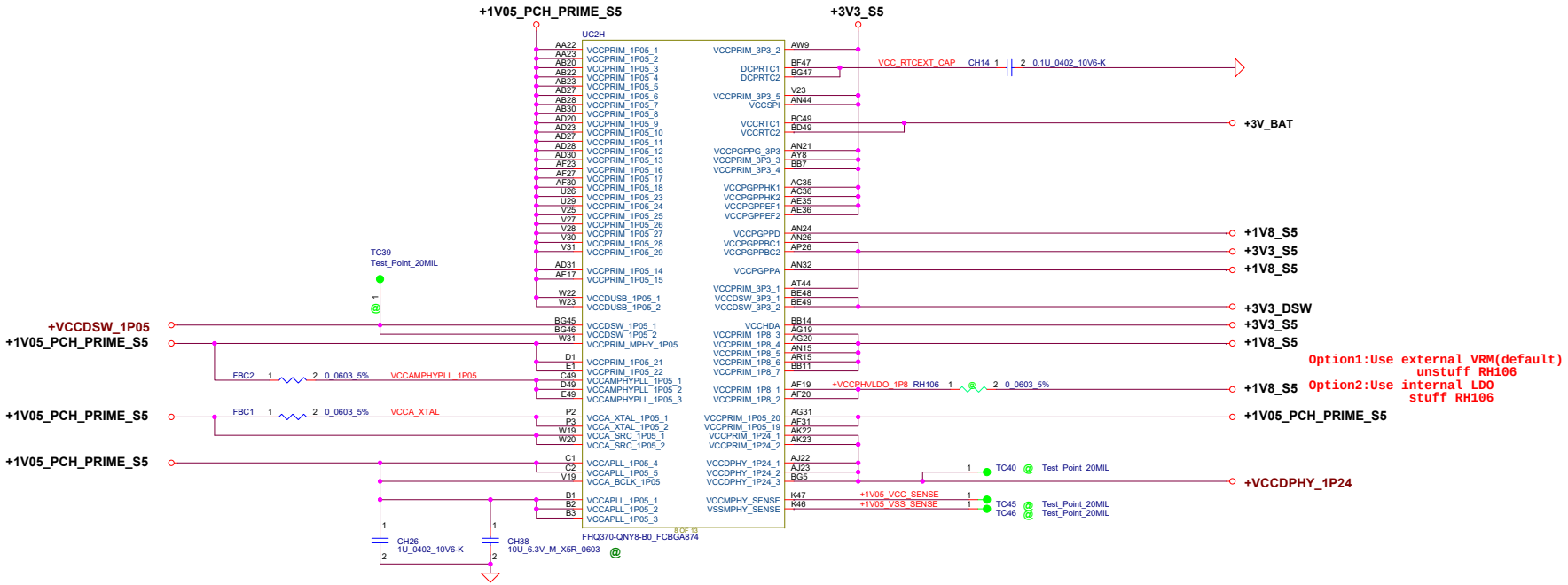


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PCH(CLK,REQ)		
Size C	Document Number GH470		Rev 1.0
Date: Monday, March 23, 2020	Sheet 16 of 64		

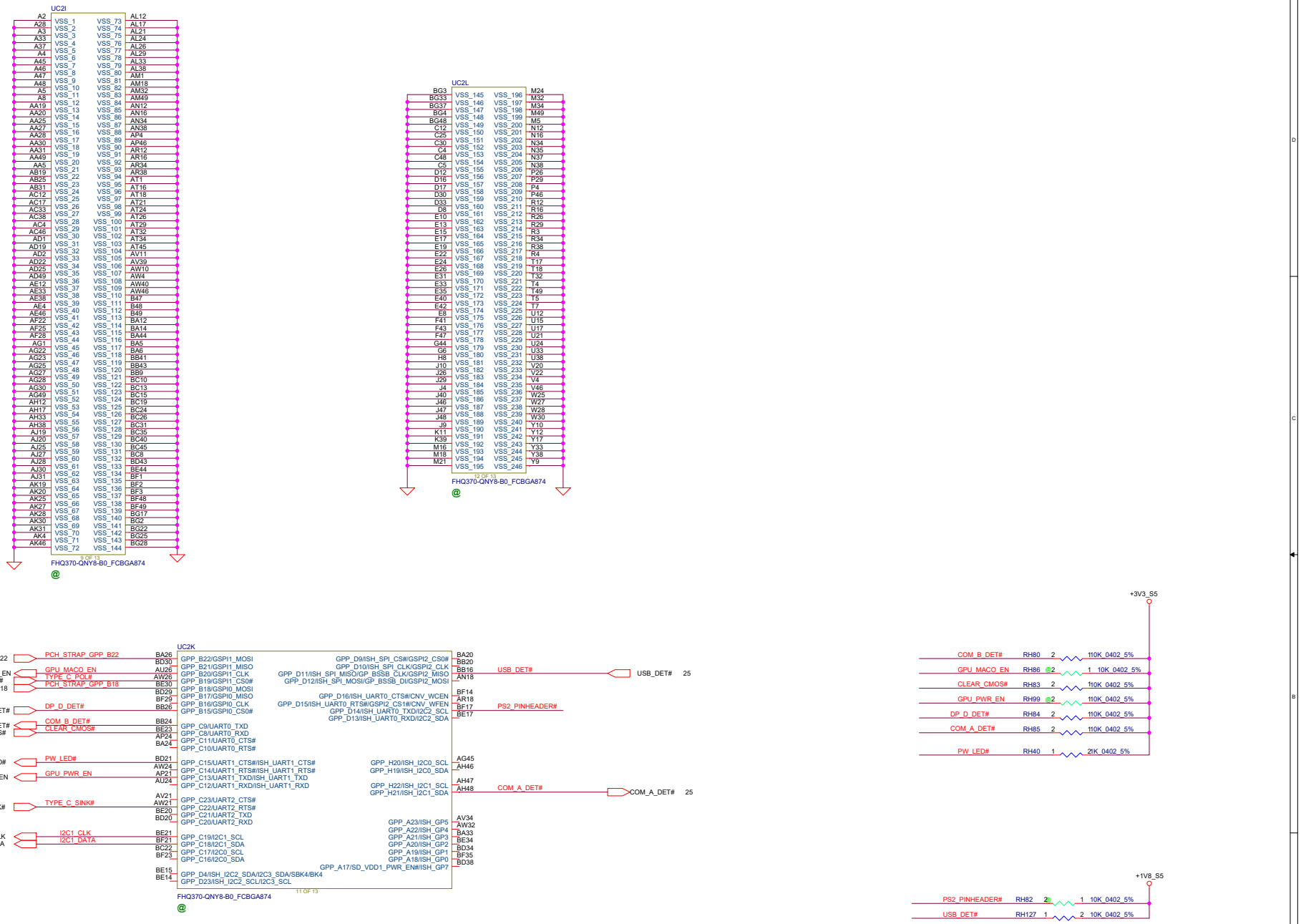
CAP FOLLOW CRB





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PCH(PCH POWER)		
Size C	Document Number GH470		Rev 1.0
Date: Monday, March 23, 2020	Sheet 17 of 64		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PCH(I2C,UART,VSS)

Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 18 of 64		

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

PCH(I2C,UART,VSS)

Size: B	Document Number: GH470	Rev: 1.0
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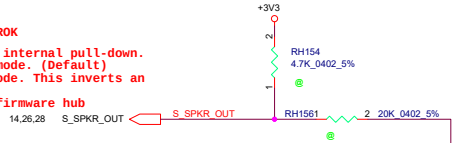
GPP_B14 SPKR

Rising edge of PCH_PWROK

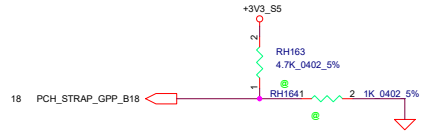
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode. This inverts an address
on access to SPI and firmware hub



GPP_B18

Rising edge of PCH_PWROK

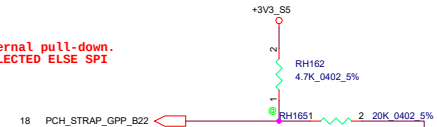
REBOOT (INTERNAL PD)
NO REBOOT
0: DISABLE (DEFAULT)
1: ENABLE



GPP_B22

Rising edge of PCH_PWROK

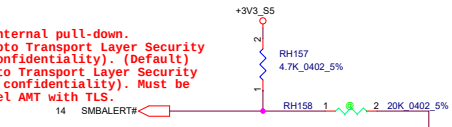
BOOT SELECT STRAP
This Signal has a weak internal pull-down.
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
0 = SPI
1 = LPC



GPP_C2

Rising edge of RSMRST#

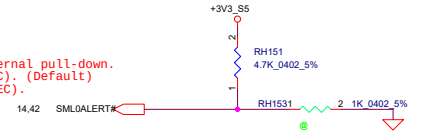
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.



GPP_C5

Rising edge of RSMRST#

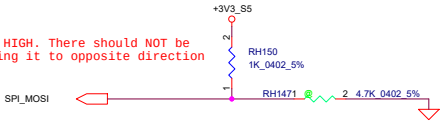
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).



SPI0_MOSI

Rising edge of RSMRST#

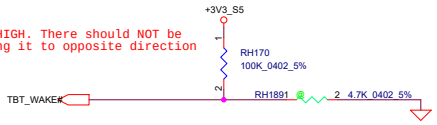
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



GPP_H15

Rising edge of RSMRST#

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



GPP_B23

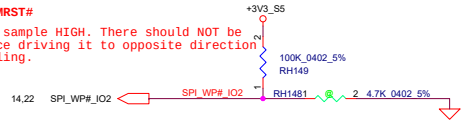
Rising edge of RSMRST#

GPP_B23 /SML1ALERT# /PCHHOT#
This signal has an internal pull-down.
0 = Disable DCI-OOB (Default)
1 = Enable DCI-OOB

SPI0_IO2

Rising edge of RSMRST#

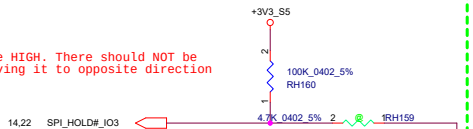
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_IO3

Rising edge of RSMRST#

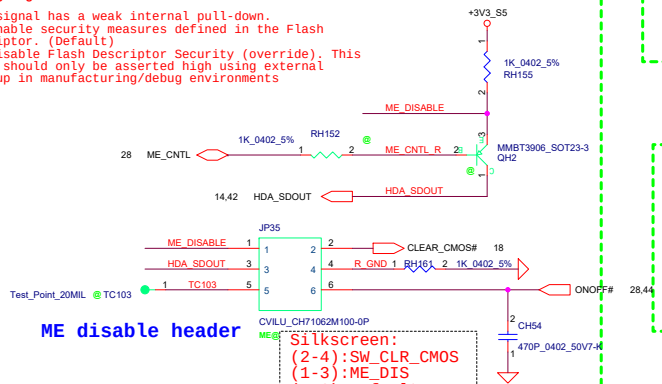
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



HDA_SDO

Rising edge of RSMRST#

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY



ME disable header

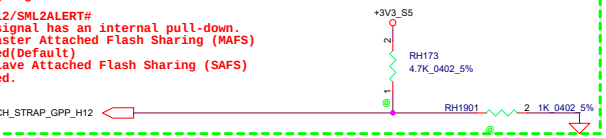
SW CLEAR CMOS

Silkscreen:
(2-4):SW_CLR_CMOS
(1-3):ME_DIS
(5-6):Default
(4-6):Power button

GPP_H12 /SML2ALERT#

Rising edge of RSMRST#

GPP_H12/SML2ALERT#
This signal has an internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled(Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.



GPP_J4 /CNV_BRI_DT /UART0_RTS#

Rising edge of RSMRST#

GPP_J4 /CNV_BRI_DT /UART0_RTS# strap Rising edge of RSMRST#
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO

Place Res close to JWLAN1

GPP_J6 /CNV_RGI_DT /UART0_TXD

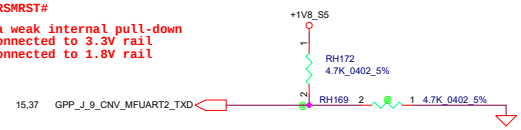
Rising edge of RSMRST#

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

Rising edge of RSMRST#

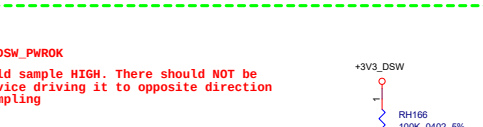
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail



GPD7

Rising edge of DSW_PWROK

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Strap pin		
Size: C	Document Number: GH470		Rev: 1.0
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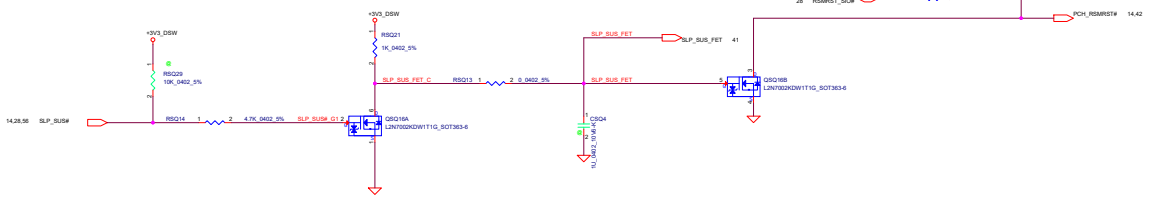
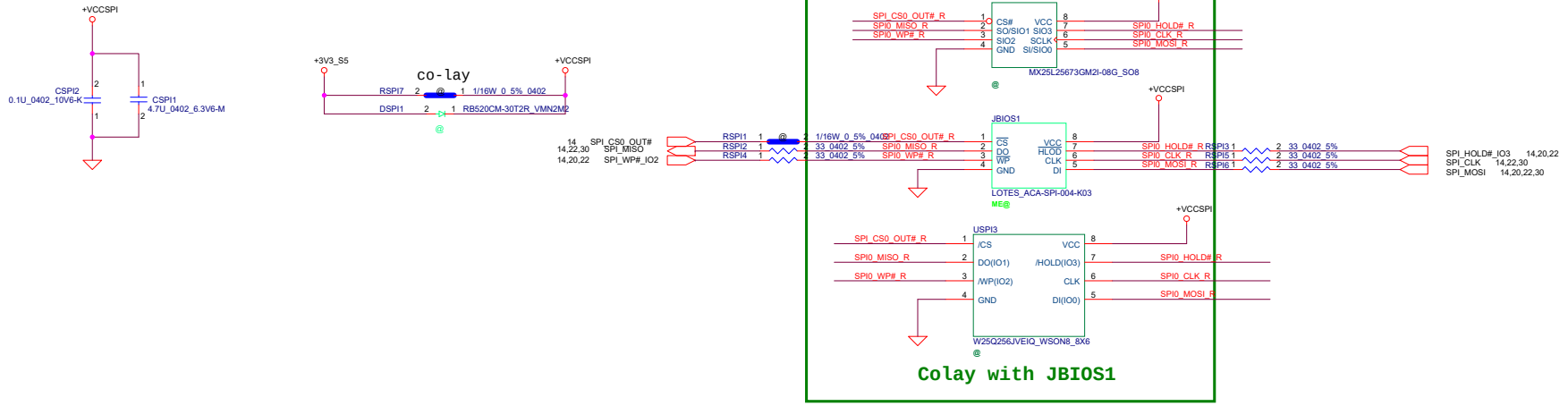
DSW CONTROL SIGNAL



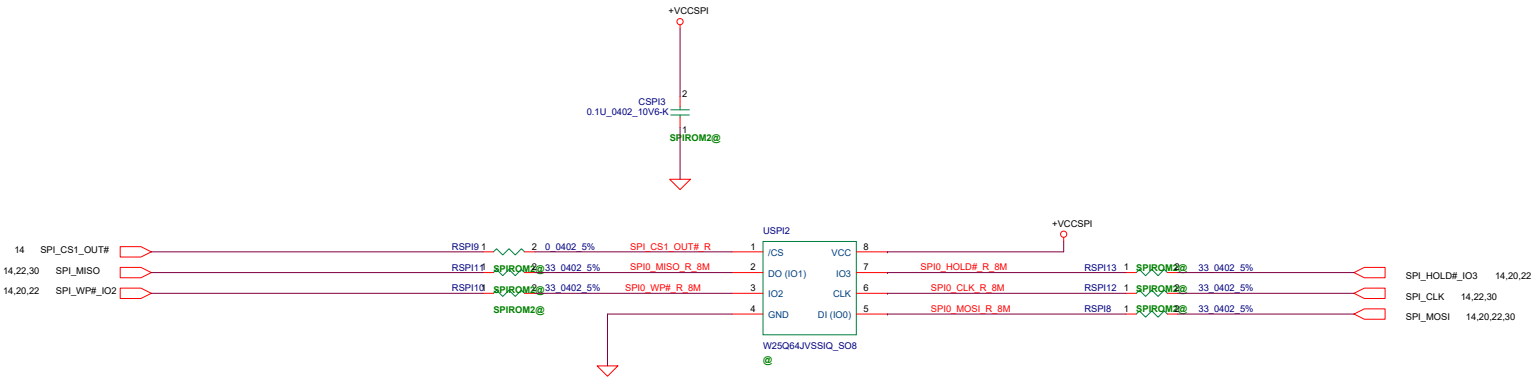
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	DSW		
Size C	Document Number GH470		Rev 1.0
Date: Monday, March 21, 2016	Sheet 21 of 64		

16M or 32M ROM



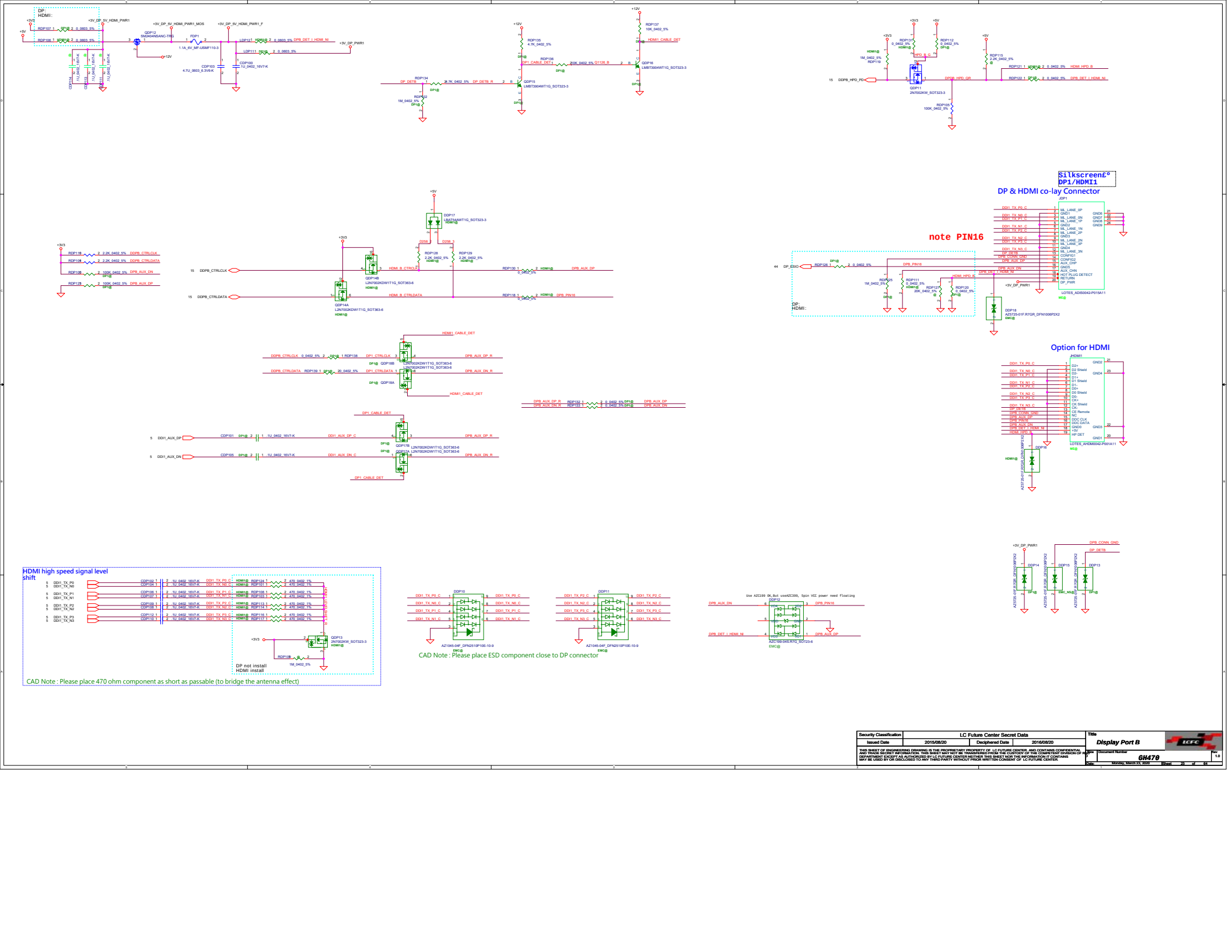
8M ROM



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: SPI ROM

Size: C	Document Number: GH470	Rev: 1.0
Date: Monday, March 23, 2020	Sheet 22 of 64	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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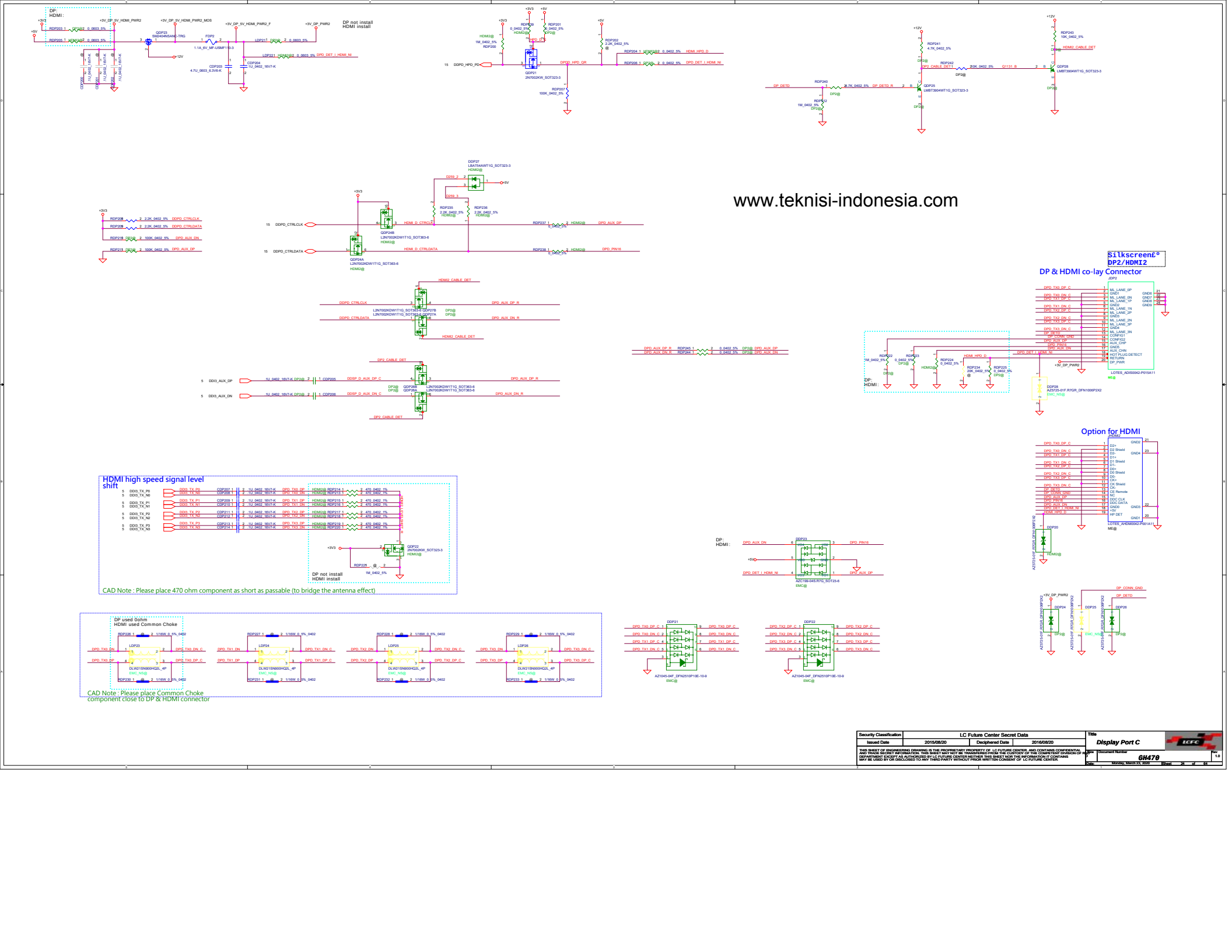
Title: Display Port B

Size: C | Document Number: GH470 | Rev: 1.0

Date: Monday, March 23, 2020 | Sheet 25 of 64



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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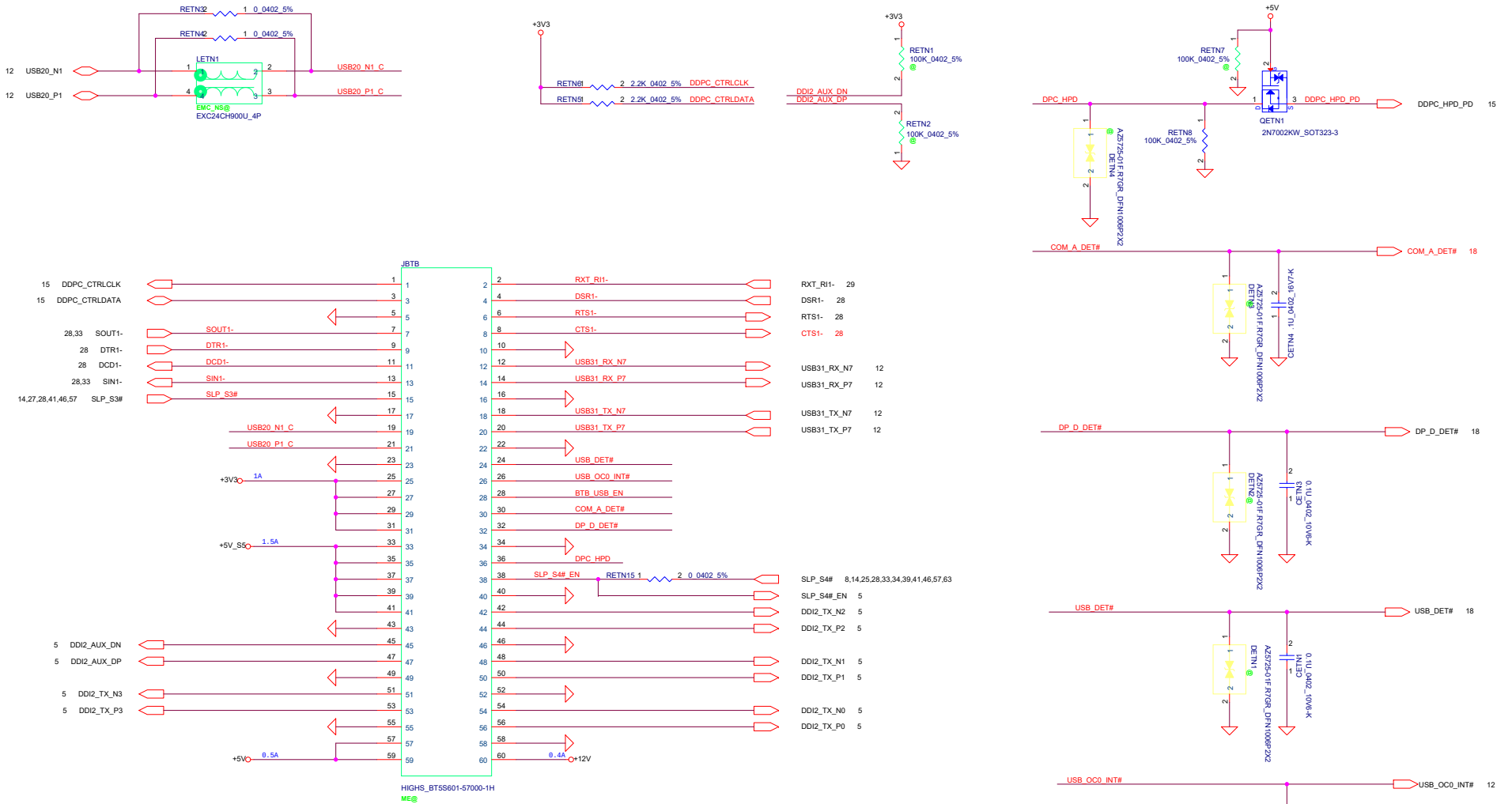
Title	Display Port C		
Size	Document Number		Rev
D	GH470		1.0
Date:	Monday, March 23, 2020	Sheet	25 of 64



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: BTB_USB3/USB2/DP/COM

Size	Document Number	Rev
C	GH470	1.0

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need change footprint and new PN

Supported iPhone/Nokia headset, Headphone, Line-In and Microphone through SW popup menu

ALC233-VA JD1 10K, JD2 39.2K, ALC233-VB JD1 100K, JD2 200K,

Place close to pin 1

Add this Filter to avoid other components/chips be influenced

Close to Pin 26

Close to Pin 40

FB1/FB2 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk

Silkscreen£° UAJ

Silkscreen£° SPKR

Audio Jack(COMBO) JA6341

ALC233-VB2-CG_MQFN48_6X6

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Near Audio jack

Near AVDD1 and AVDD2 power source input under Codec or near the Codec

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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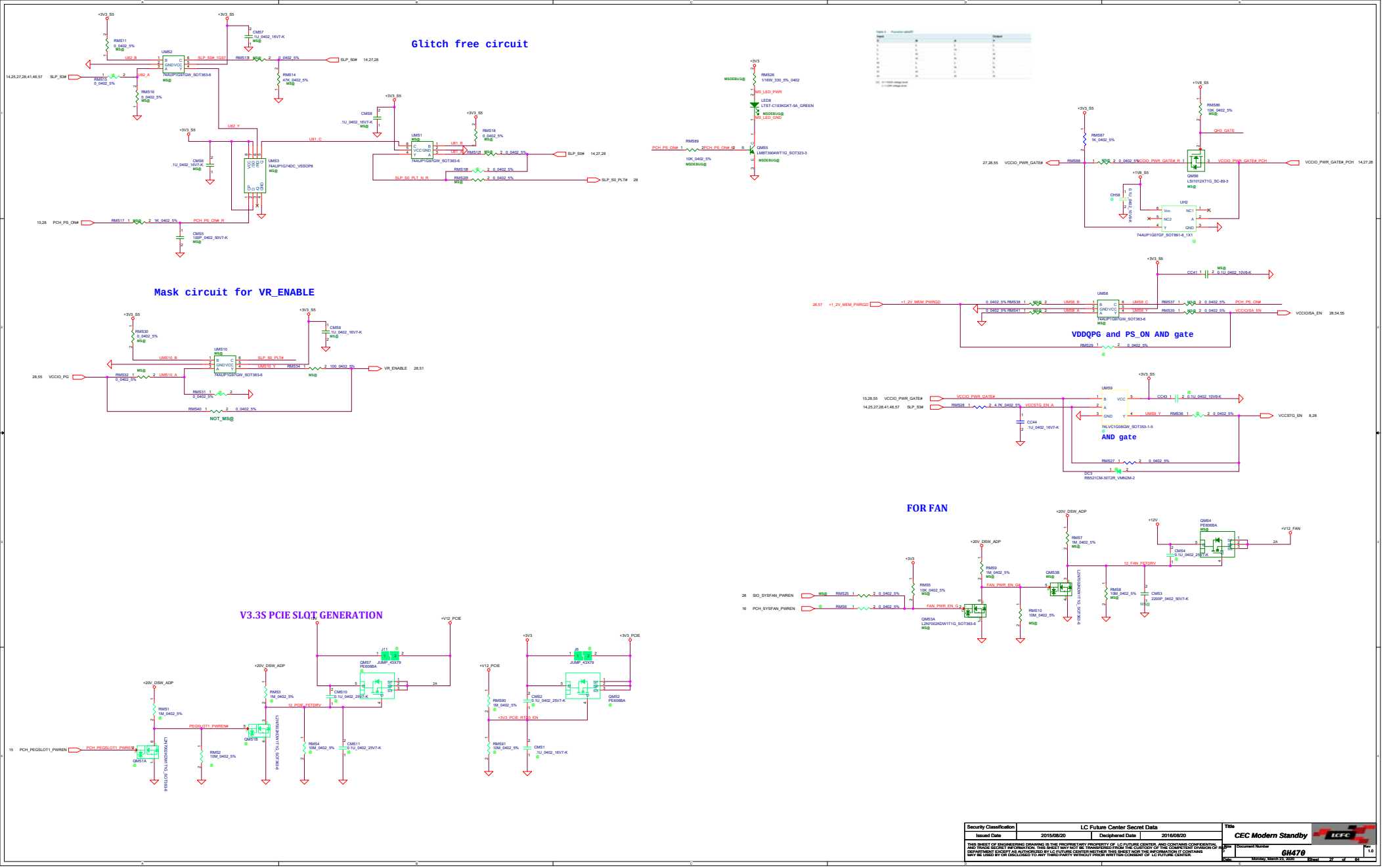
Title: Audio Codec - ALC233VB

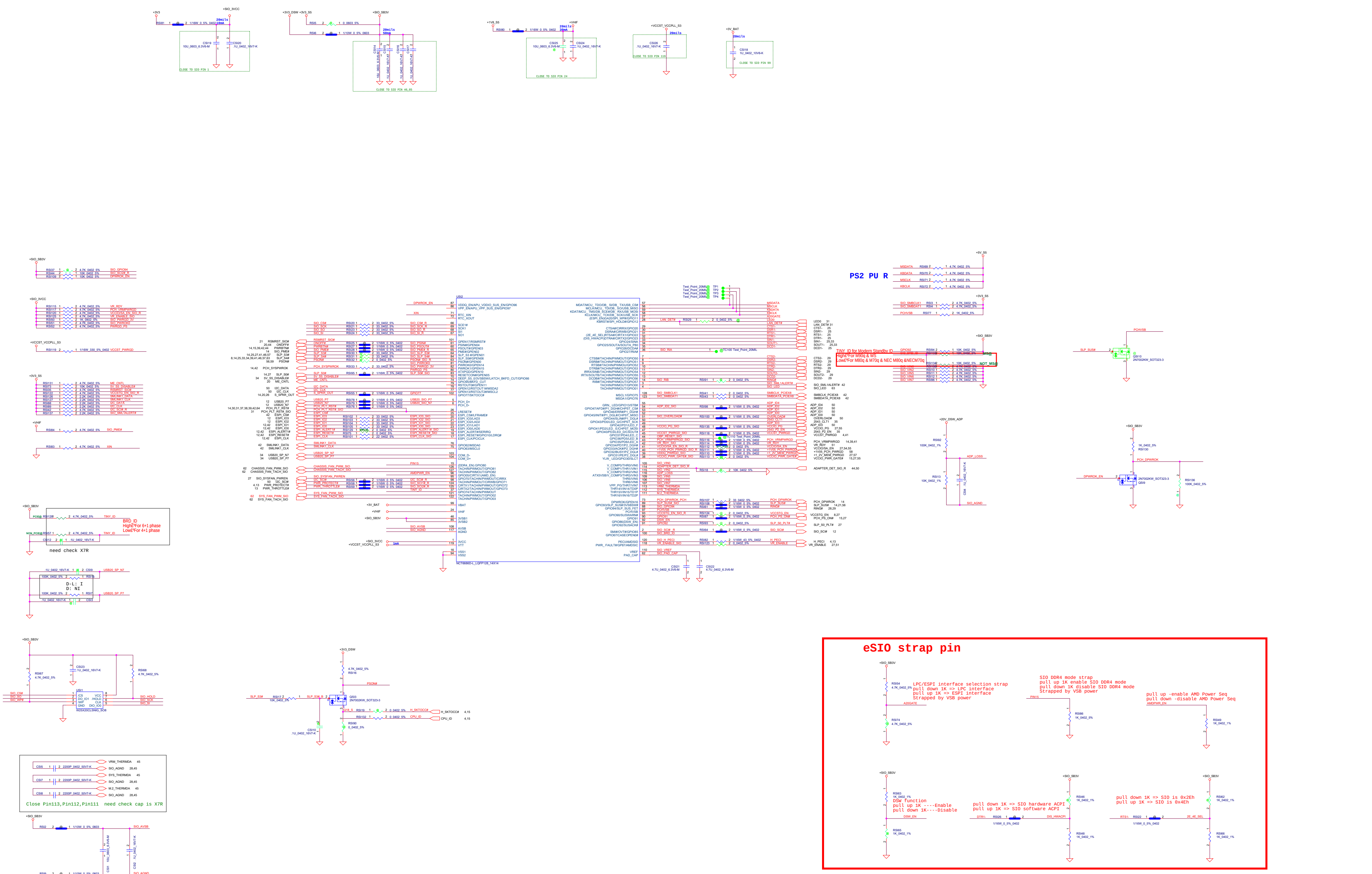
Size: C | Document Number: GH470 | Rev: 1.0

Date: Monday, March 28, 2016 | Sheet 26 of 64



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	CEC Modern Standby		
Size	Document Number		Rev
D	GH479		1.0
Date:	Monday, March 23, 2020	Sheet	27 of 64


PS2 PU R
eSIO strap pin
LPC/ESPI interface selection strap
pull down 1K => LPC interface
pull up 1K => ESPI interface
Strapped by VSB power
SIO DDR4 mode strap
pull up 1K enable SIO DDR4 mode
pull down 1K disable SIO DDR4 mode
Strapped by VSB power
pull up -enable AMD Power Seq
pull down -disable AMD Power Seq
DSW function
pull up 1K ----Enable
pull down 1K----Disable
pull down 1K => SIO hardware ACPI
pull up 1K => SIO software ACPI
pull down 1K => SIO is 0x2Eh
pull up 1K => SIO is 0x4Eh
BRD_ID
High for 6+1 phase
Low for 4+1 phase
need check X7R
Close Pin113,Pin112,Pin111 need check cap is X7R

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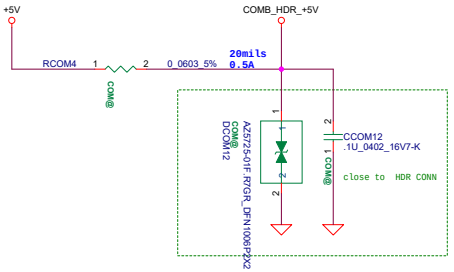
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

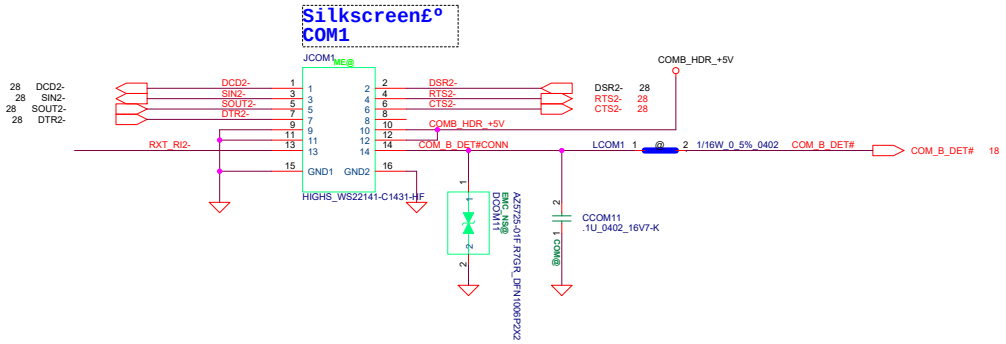
Title: SIO NCT6686D-L

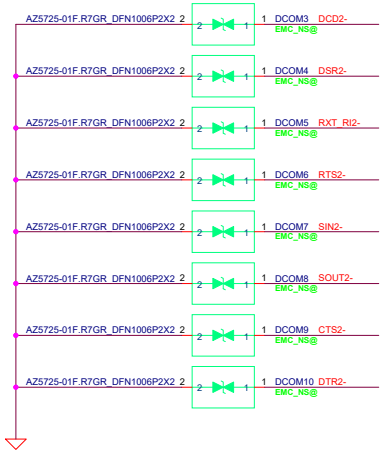
Document Number: GH470

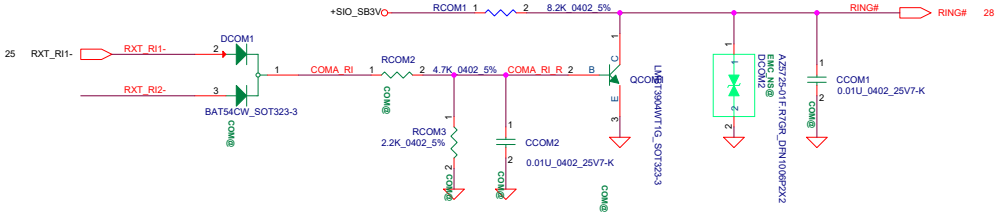
Rev: 1.0

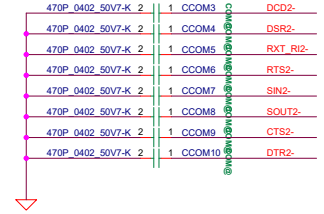
Date: Monday, March 23, 2020 Sheet 28 of 64





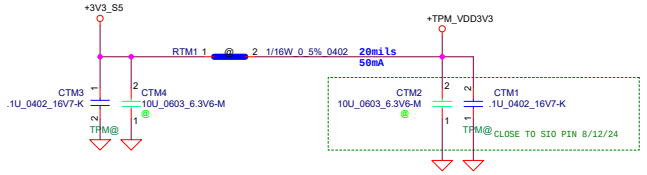




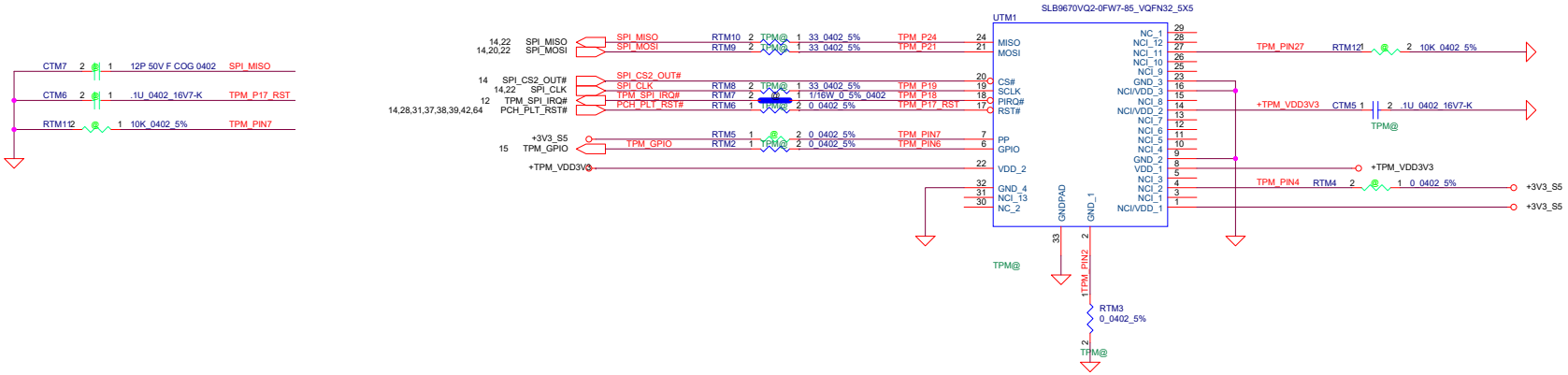


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	COM Port/ PS/2		
Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 29 of 64		



	RTM3	RTM2	
ST ST33HTPH2X32AHC4 (SPI)	V	X	
Nuvoton NPCT750LABYX(SPI)	X	V	Need confirm PN Nuvoton
Infineon SLB9670VQ2.0FW7.85 (SPI)	V	V	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: TPM - TCG 2.0

Size	Document Number	Rev
C	GH470	1.0

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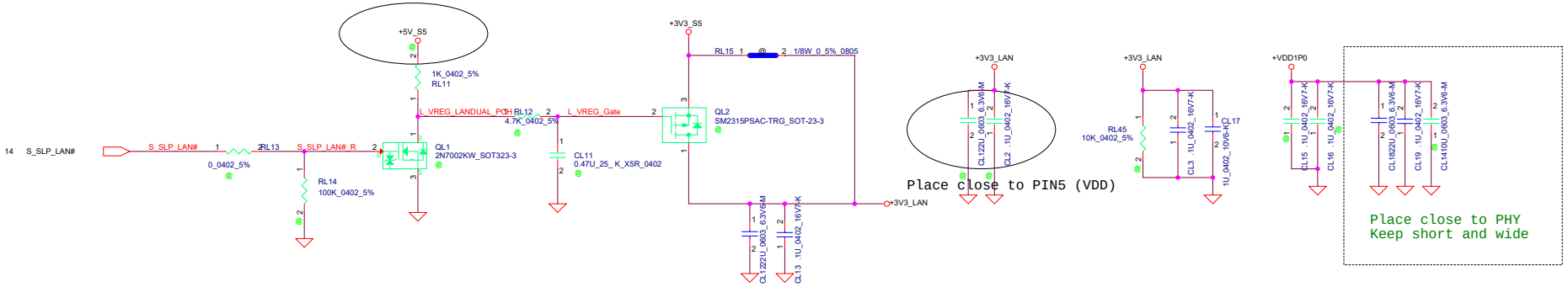
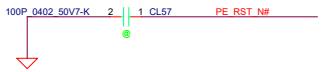
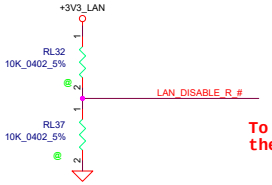
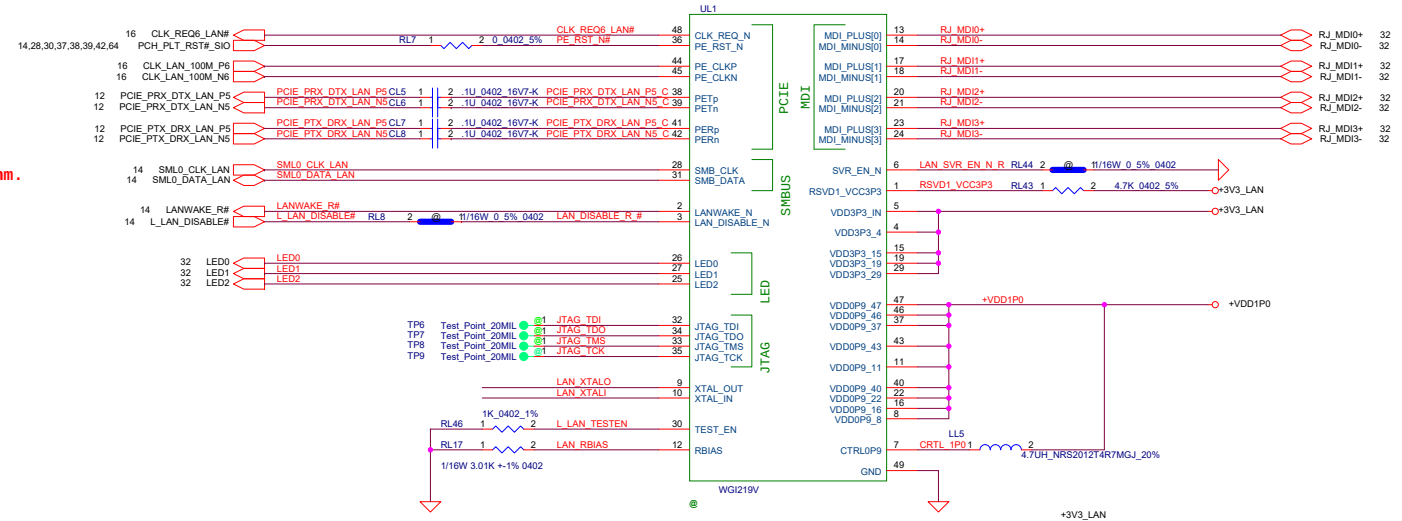
POWER DESIGN NOTE:
> +3.3V_LAN should always have power during all networking conditions
(S0, Sx, DeepSx states, WOL, etc.)

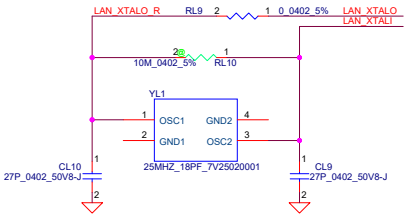




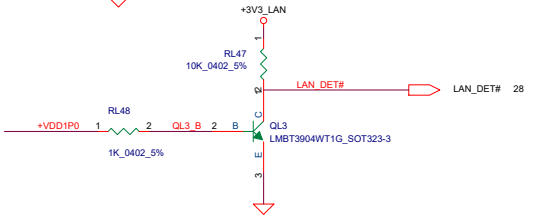


To support SMBUS 1MHz speed, the pull-up should be 499 ohm.





Change to SJ10000FZ00, S CRYSTAL 25MHZ 18PF +-30PPM 7V25020001



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	LAN - JacksonVille_i219LM		
Size C	Document Number GH470		Rev 1.0
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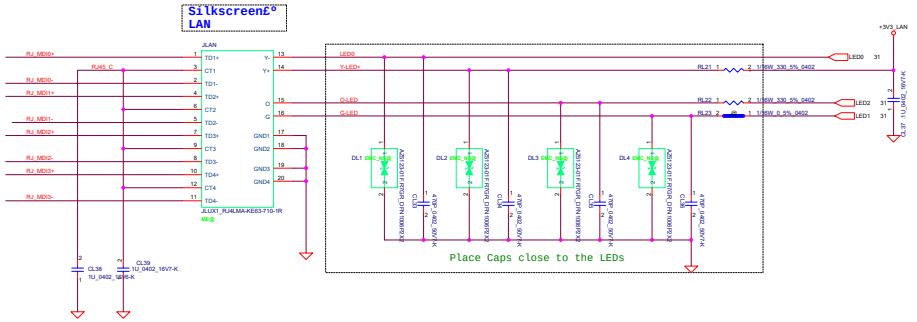
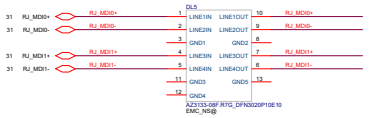
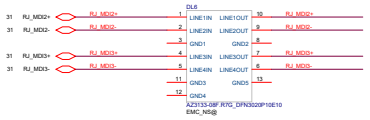
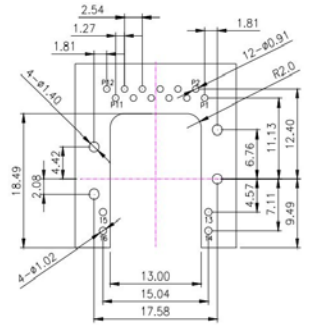
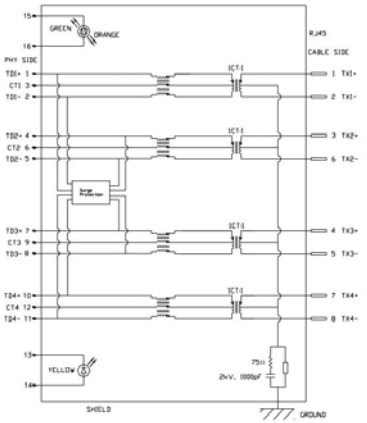




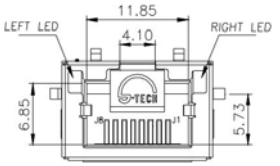




RECOMMENDED PCB LAYOUT
COMPONENT SIDE
ALL DIMENSION TOLERANCE ARE ±0.05mm
UNLESS OTHERWISE SPECIFIED



WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: RJ45

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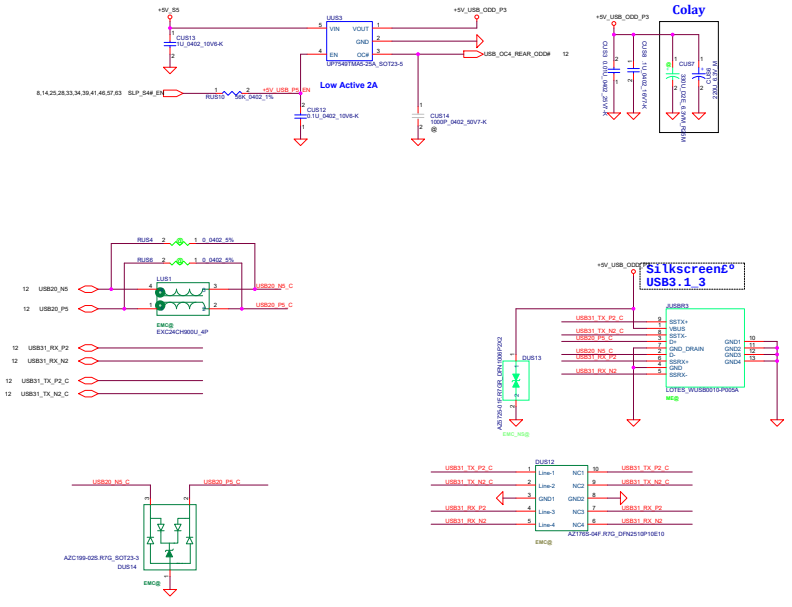
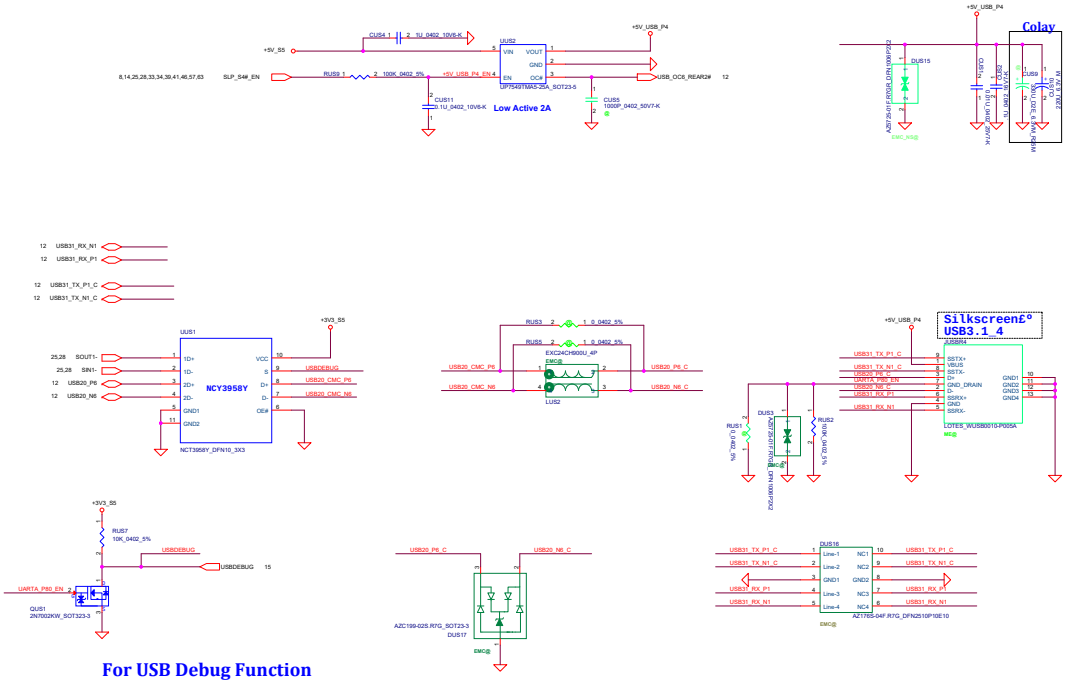
Rear Side USB ODD



Rear Side USB 3.1 GEN2
UART USB debug port



For USB Debug Function

USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UART_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to ID(+/-)
L	H	D(+/-) to 2D(+/-)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Rear USB3e ODD

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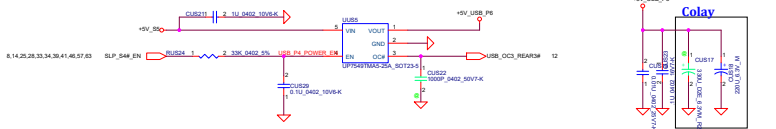
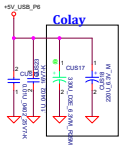
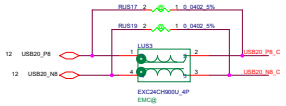
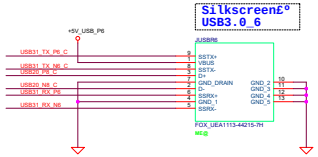
3 in 1 USB3 port

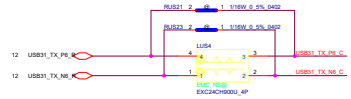


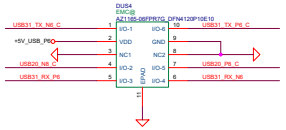
need change footprint



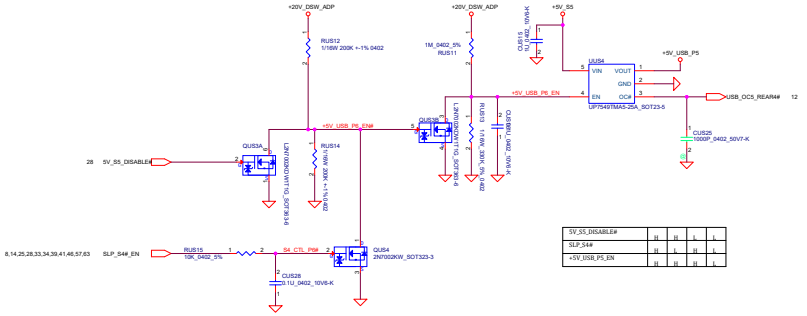




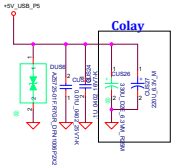


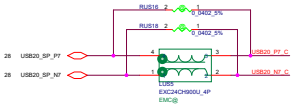


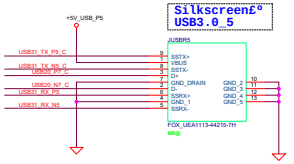
Smart power on USB

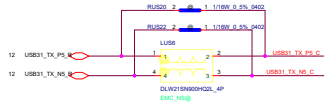


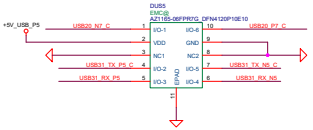
5V_S5_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P5_EN	H	H	H	L











Security Classification	LC Future Center Secret Data		
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Title: Rear USB3 x 2

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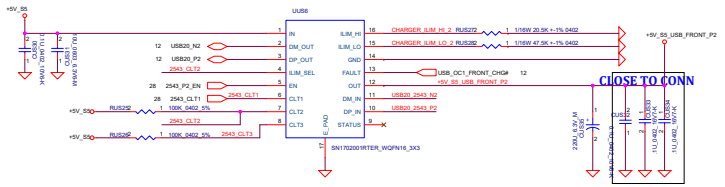
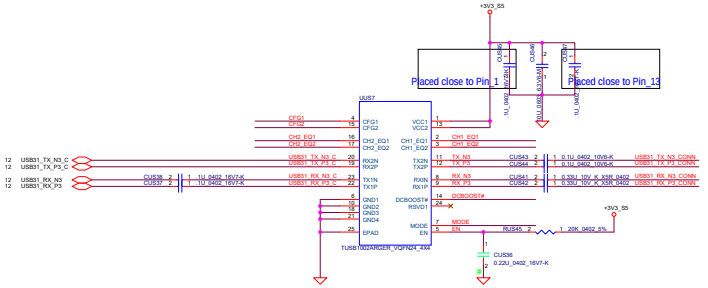
ILIM_HI	20.5K	2.5A
ILIM_LO	47.5K	1.1A

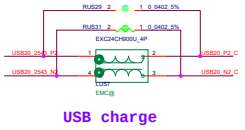
DCP	Tiny 53/54/55
CDP	Tiny 50 Tiny not support

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
						off
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{OS_FW} & ILIM_HI [1]	DCP load present [2]
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present [3]
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP [4]	ILIM_LO	off
1	1	1	1	CDP [4]	ILIM_HI	CDP load present [5]

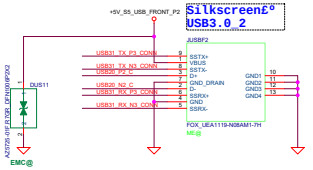
FRONT USB3.0 Charger

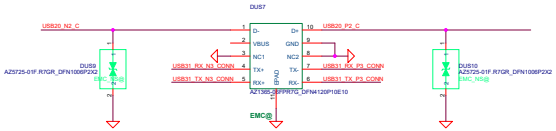


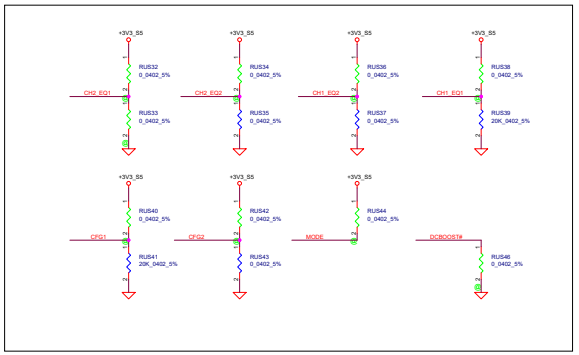




USB charge







CH2_EQ2 = 0

CH2_EQ1 = F

CH1_EQ2 = 0

CH1_EQ1 = R

CFG1 = R

CFG2 = 0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Front USB3 Charger x1		
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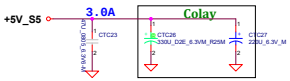

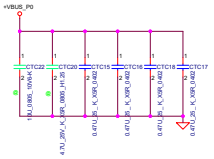

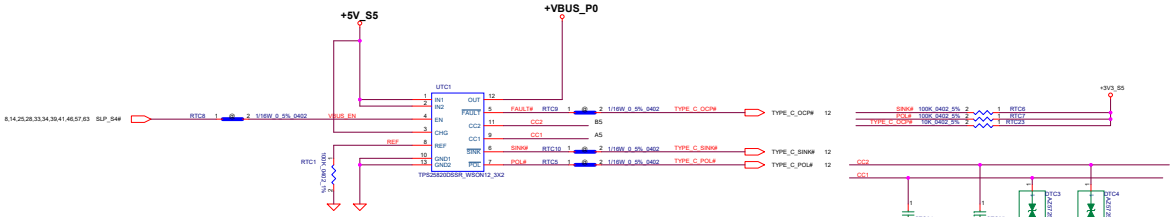

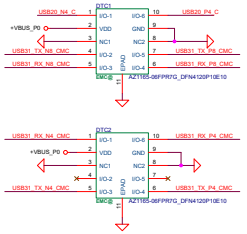

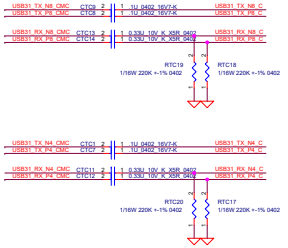

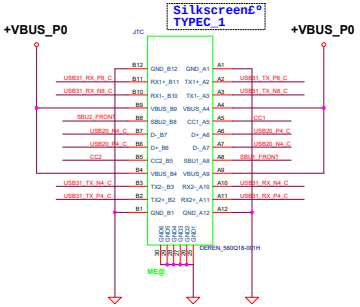

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Type-C RTS5449E		
Size	Document Number		Rev
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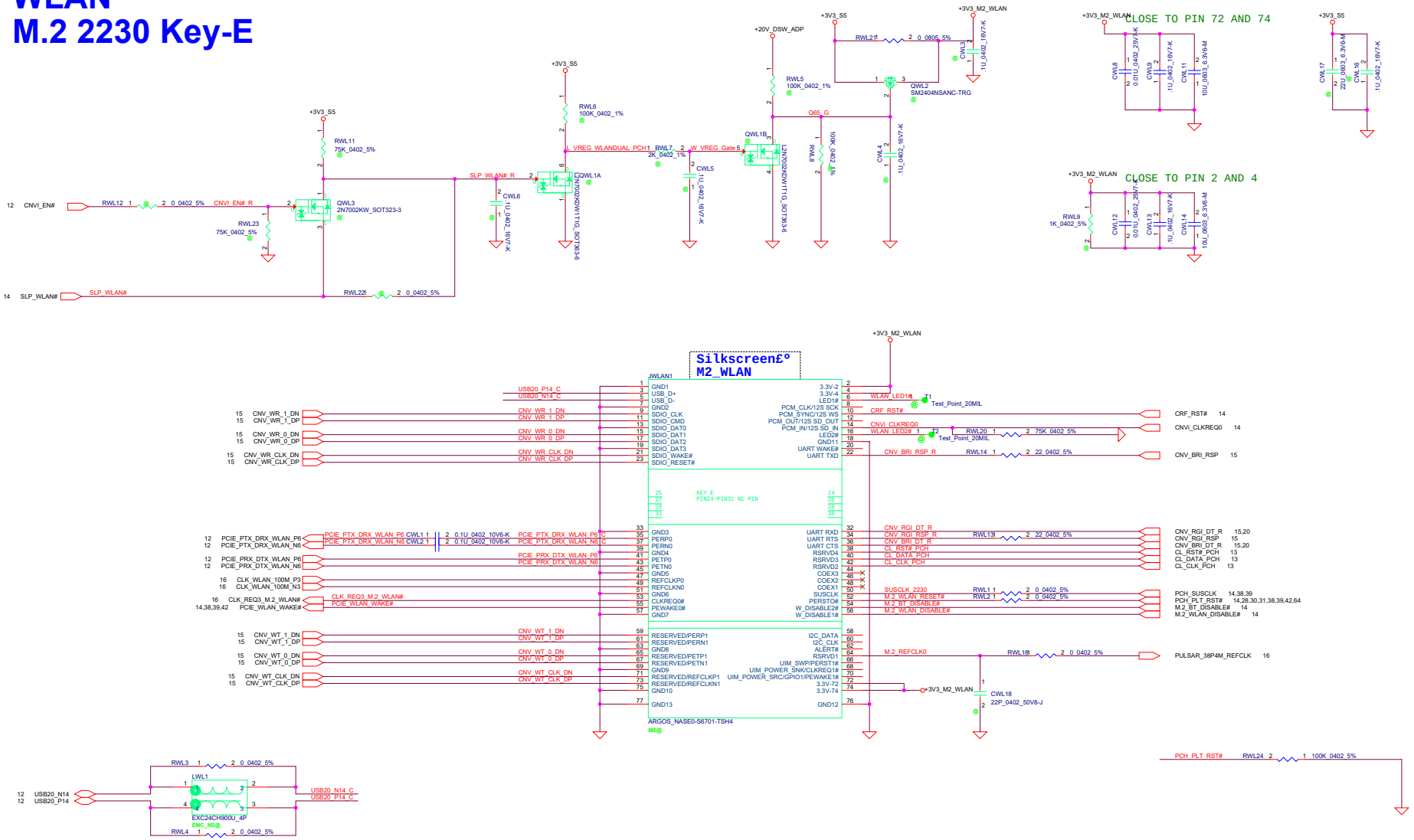
WLAN
M.2 2230 Key-E



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: M.2 2230-E WIFI/ BT/CNVI

Size: Custom | Document Number: GH470 | Rev: 1.0

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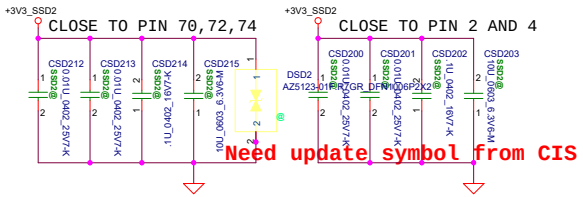
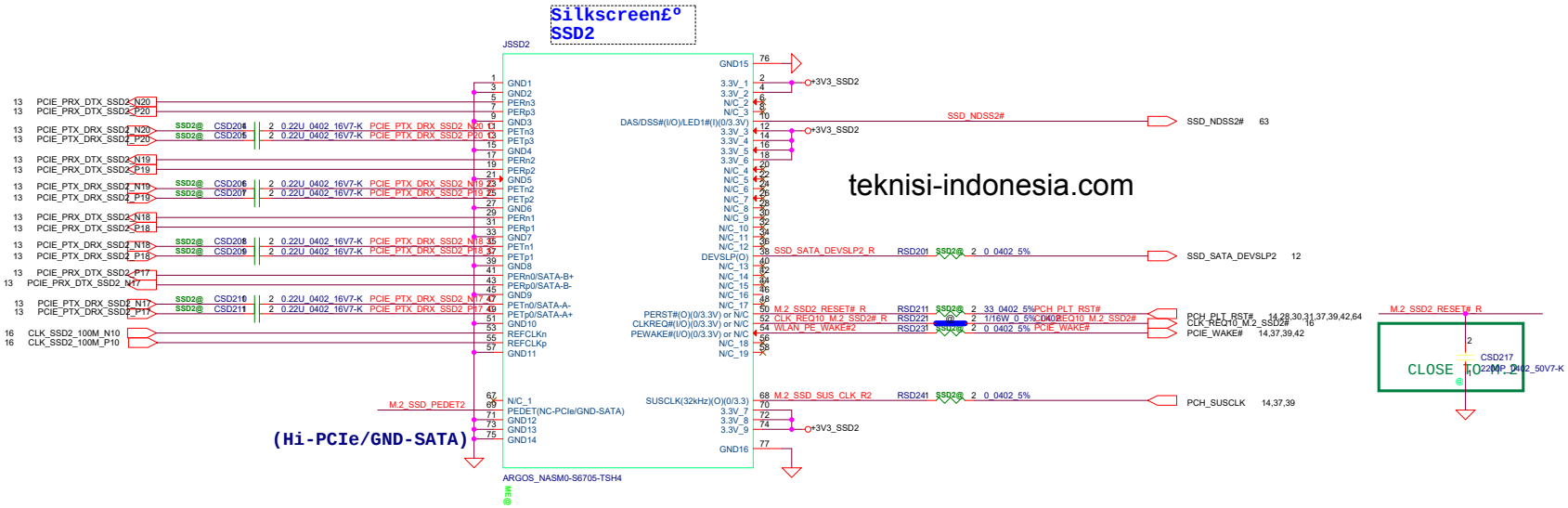
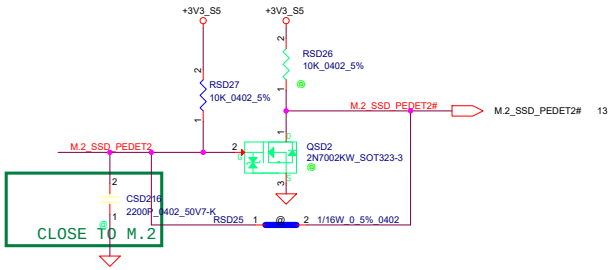
M.2 Connector SSD2#(Black)

JSSD3 on TOP Layer
JSSD2 on Bottom Layer







SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	M.2 2280-M SSD-2-BLACK		
Size	Document Number		Rev
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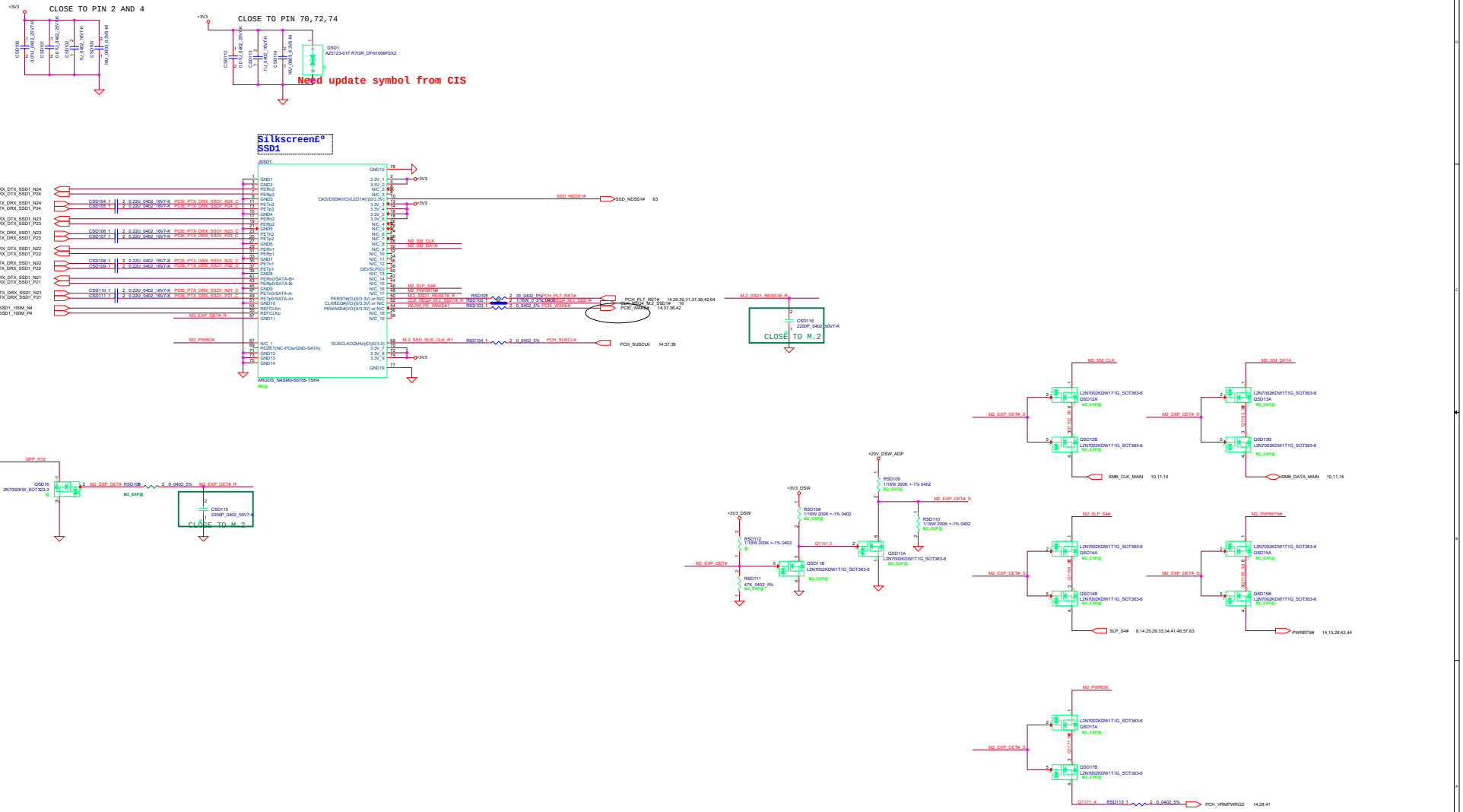
M.2 Connector SSD1#(WHITE)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	M.2 2280-M SSD-1-WHITE		
Size	Document Number		Rev
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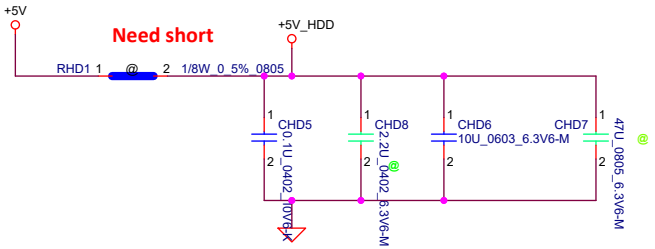

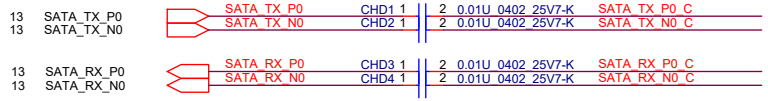

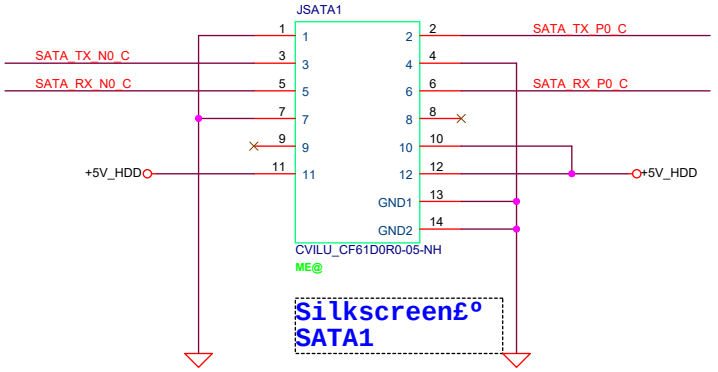

CAD NOTE : PLACE ALL CAPS WITHIN 0.5 INCH OF CONNECTOR

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Buzzer/Sata FFC**

Size: B	Document Number: GH470	Rev: 1.0
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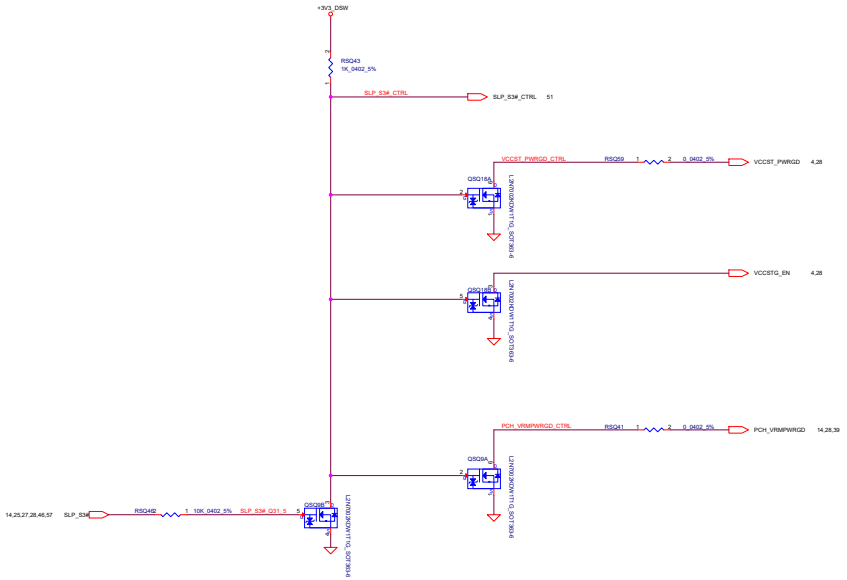
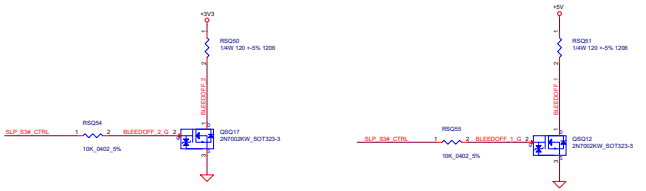
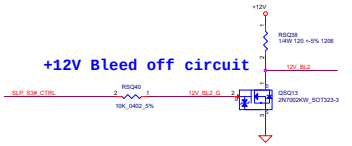
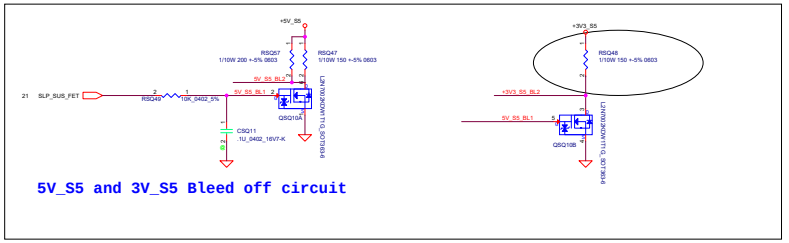


5V & 3.3V Bleed off circuit



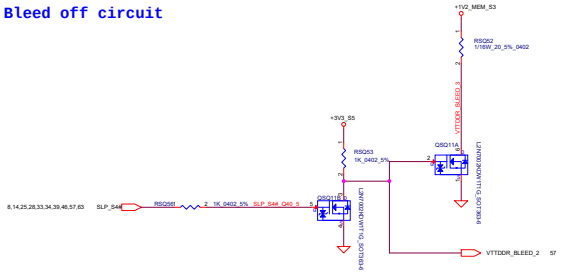
+12V Bleed off circuit





5V_S5 and 3V_S5 Bleed off circuit

+1V2_MEM Bleed off circuit



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWRGD & Bleed Off		
Size	Document Number		Rev
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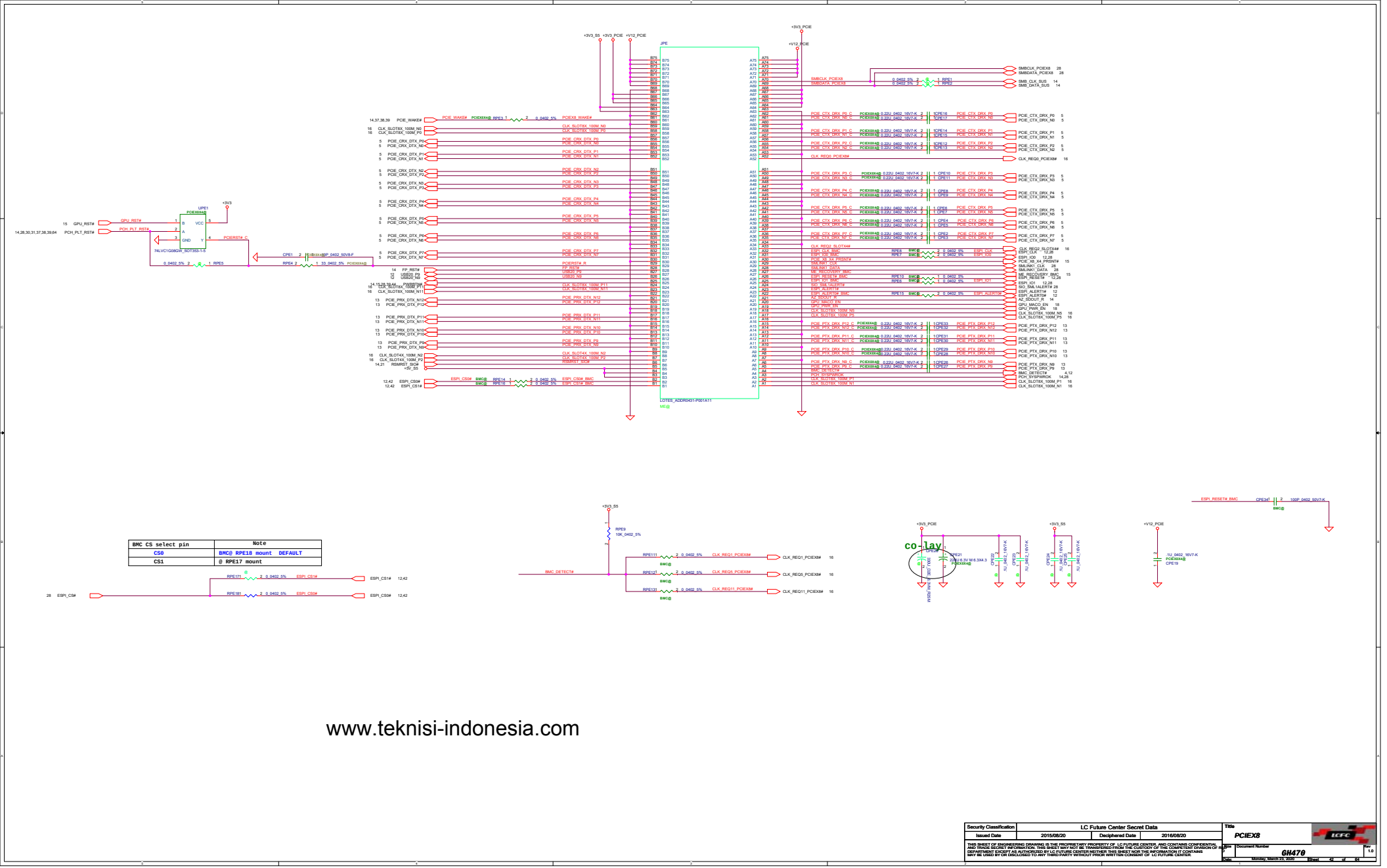
Date:	Monday, March 23, 2020	Sheet	41 of 64

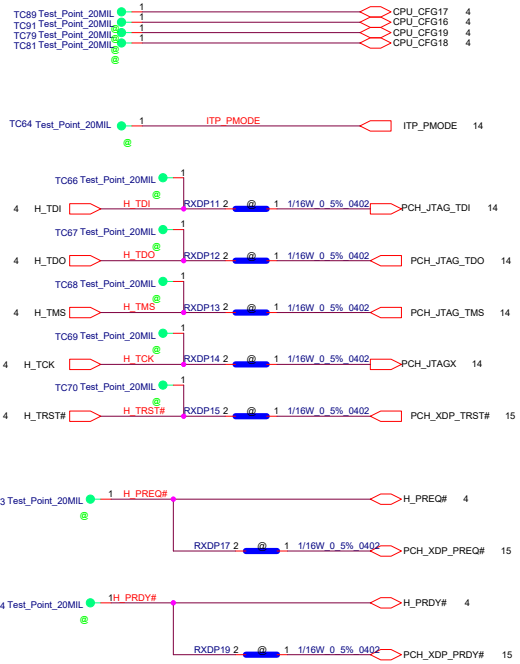


BMC CS select pin	Note
CS0	BMC@ RPE18 mount DEFAULT
CS1	@ RPE17 mount

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

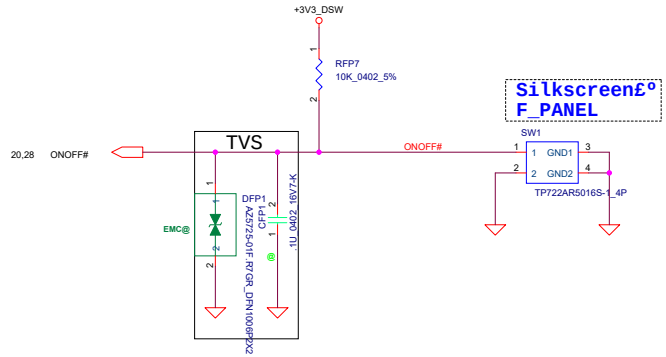
Title			
PCIEX8			
Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 42 of 64		

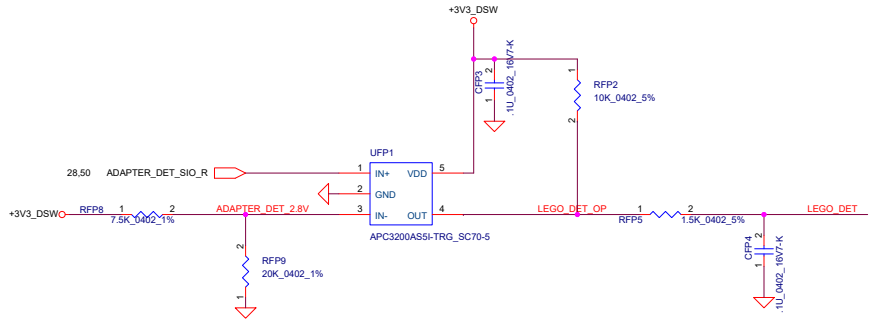
Intel XDP Debugging Connector

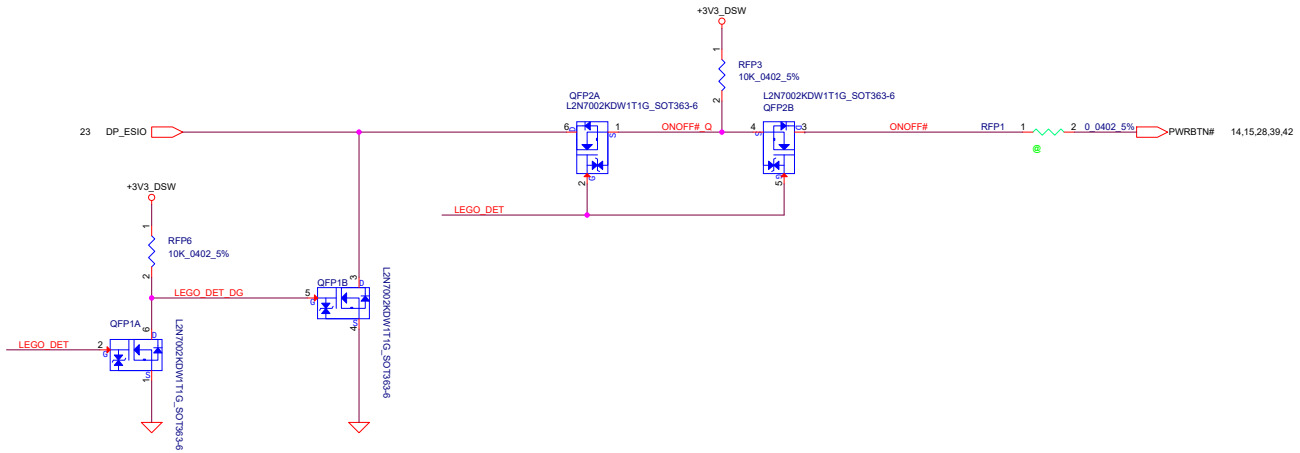


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: XDP			
Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 43 of 64		







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Button/ LED		
Size C	Document Number GH470		Rev 1.0
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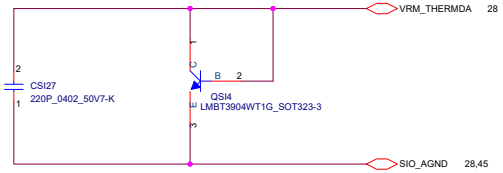
Temperature Sensing

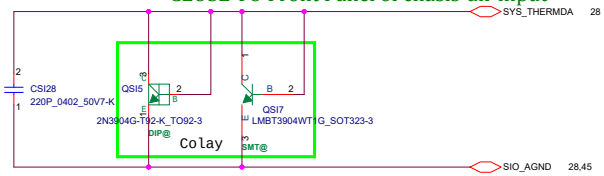
Current Mode

CLOSE TO VR MOSFET



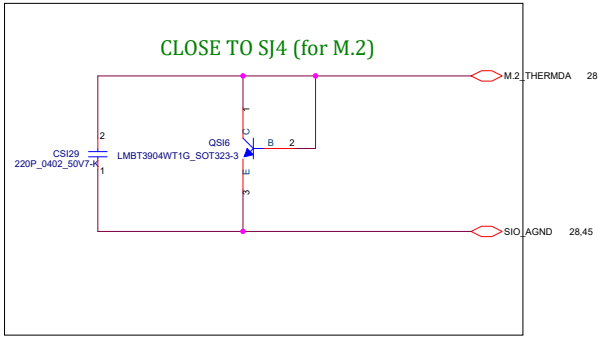
Silkscreen£º
THER_HD

CLOSE TO Front Panel of chasis-air input



CAD NOTE : Place MLCC Close to Thermal Diode

CLOSE TO SJ4 (for M.2)

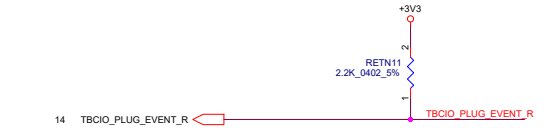


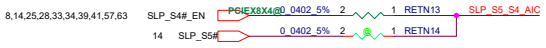
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

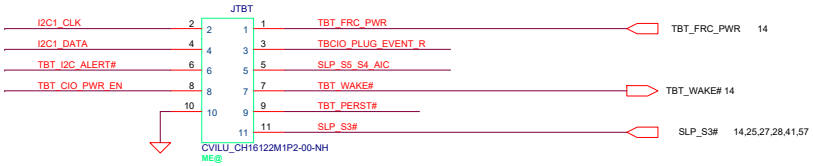
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: SM BUS/Thermal Sensing/TBT

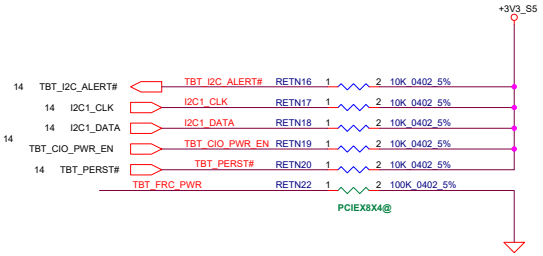
Size: C	Document Number: GH470	Rev: 1.0
Date: Monday, March 23, 2020	Sheet 45 of 64	







Silkscreen£º
TBT-HDR



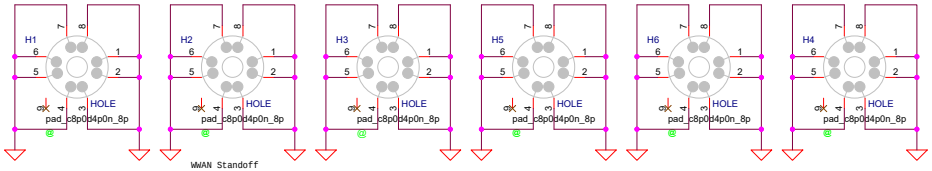
Title			
TBT-HDR			
Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 46 of 64		

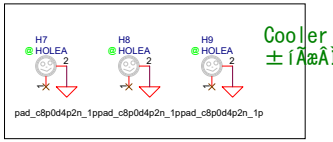
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

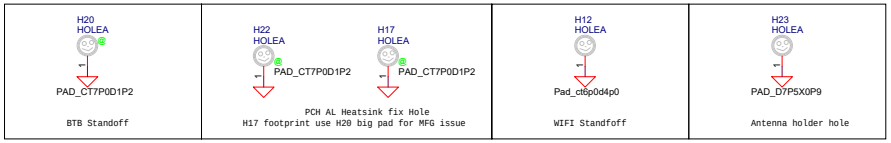
Title: *APS*

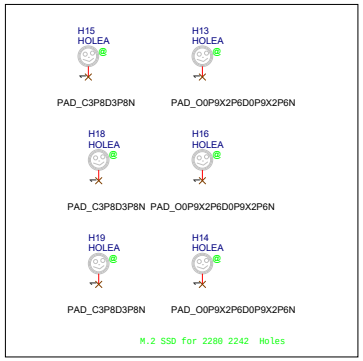
Size	Document Number	Rev
C	*GH470*	1.0

Date: Monday, March 23, 2020 | Sheet 47 of 64









ZZZ1
NM-C621
DA600016R10
PCB 1K6 NM-C621 REV1 M/B

ZZZ3
ROYALTY HDMI W/LOGO+HDCP
RO00000040J
ROYALTY HDMI W/LOGO+HDCP
HDMILOGO@

ZZZ4
Battery
GC02001Y500
BATT CR2032 3V 225MAH PA 5 0TG
BATTERY@

UC2
FH82H470 SRH14 A0 FCBGA 874P 09 !
SA0000AKN10
H470@

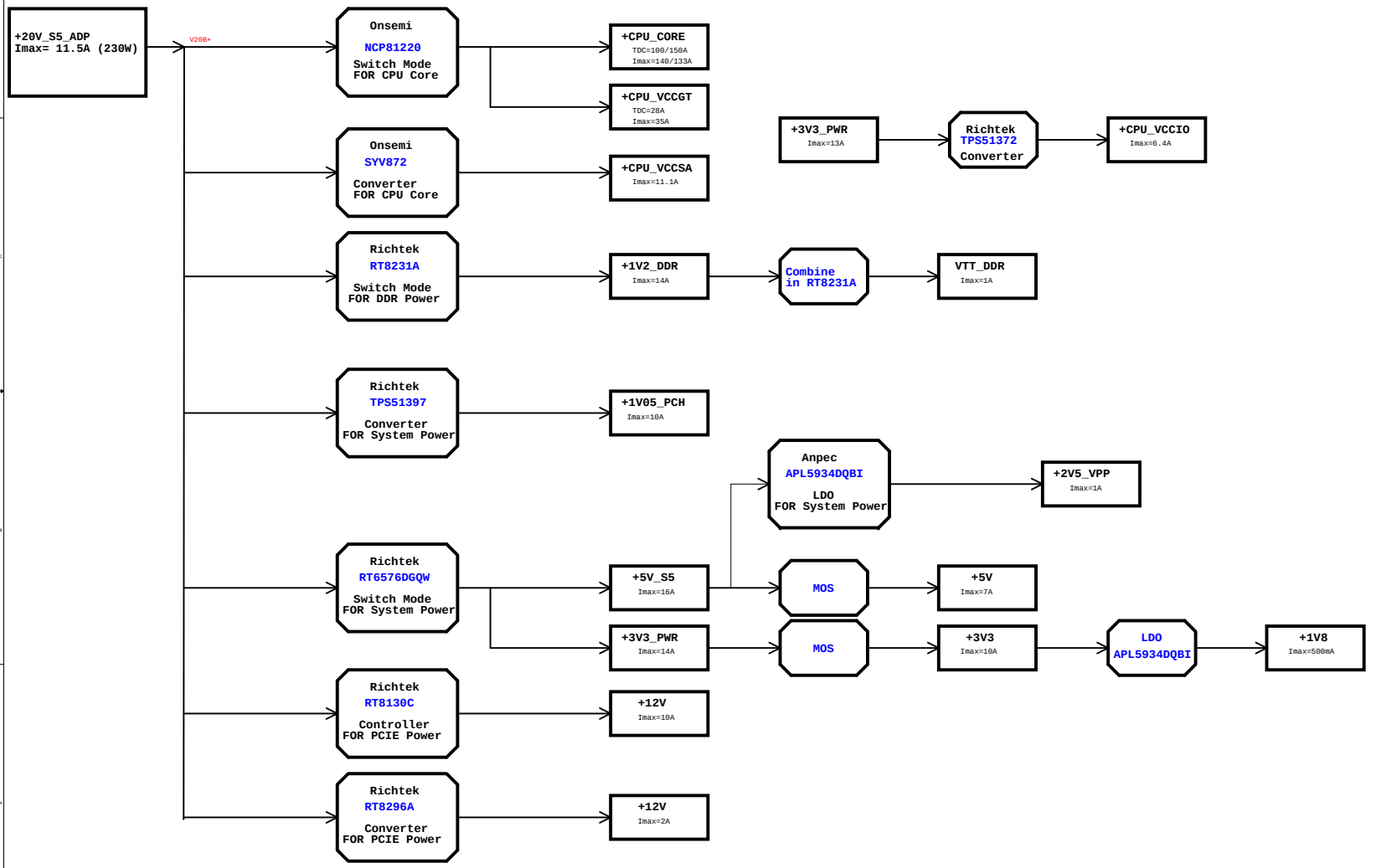
UC2
FH82Q470 SRH1A A0 FCBGA 874P 09 !
SA0000AKP10
Q470@

UL1
WGI219V
SA000072Z40
S IC WGI219V SLKJ5 A0 QFN LAN PHY 12 !
H470@

UL1
WGI219LM
SA000073040
S IC WGI219LM SLKJ3 A0 QFN 48P LAN PHY 12 !
Q470@

M80Q (32M)	**SOP8**	**43J** USPI1 MX25L25673GM2I-08G_SO8 SA00008J400 S IC FL256M MX25L25673GM2I-08G SOP 8P **SPIROM1@**
M70Q (16+8M)	**SOP8**	ZZZ2 WINBOND 16+8 X7649W090001 Tiny6 GH470 4+1 MB WINBOND 16+8 **SPIROM2@**

Title	Hole/PCB/Virtual symbol		
Size: C	Document Number: GH470		Rev: 1.0
Date: Monday, March 23, 2020	Sheet 48 of 64		

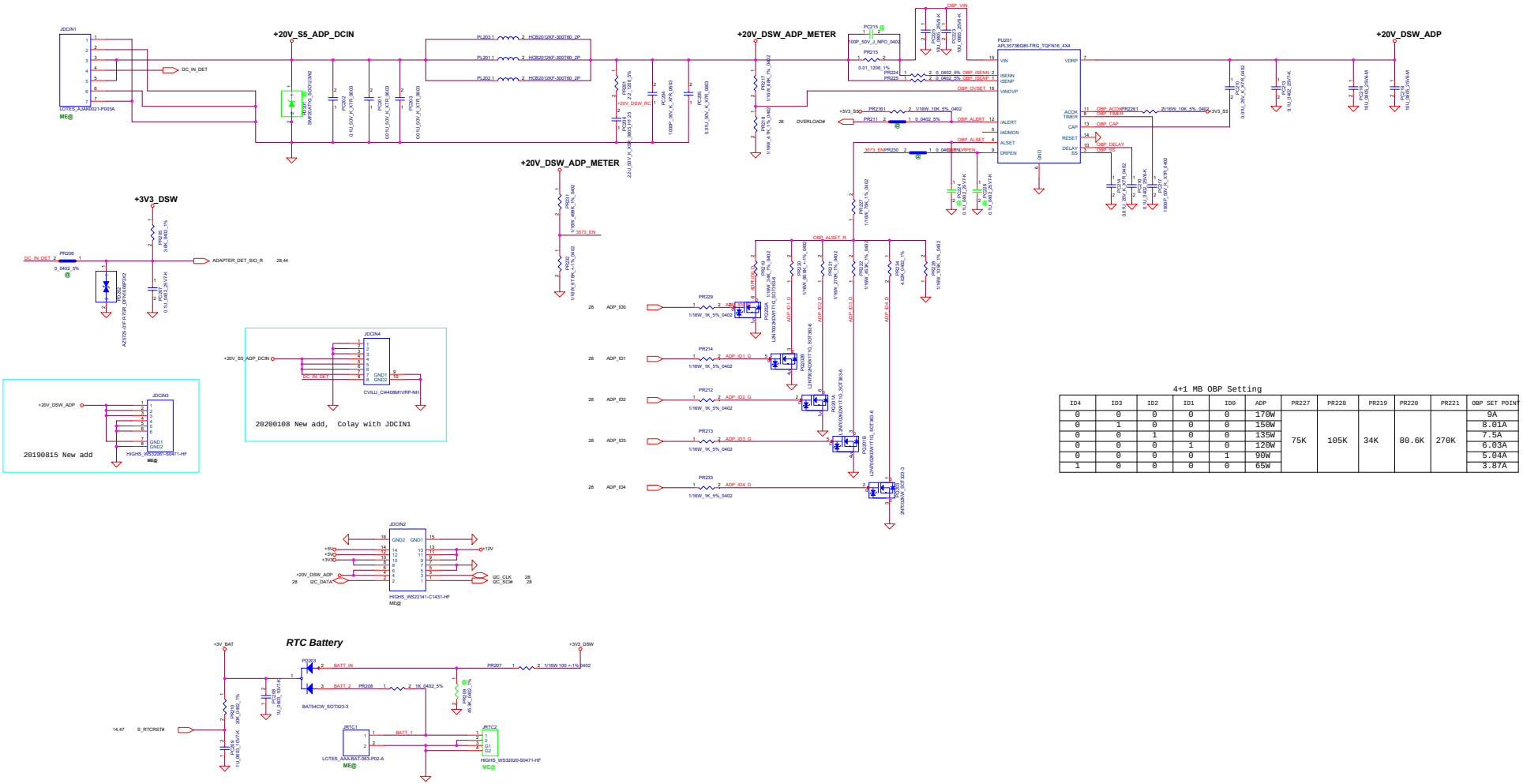


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: PWR-Power Diagram

Size: D | Document Number: G0498 | Rev: 0.1

Date: Monday, March 24, 2014 | Sheet 48 of 64



ID4	ID3	ID2	ID1	ID0	ADP	PR227	PR228	PR219	PR220	PR221	OBP SET POINT
0	0	0	0	0	170W						9A
0	1	0	0	0	150W						8.81A
0	0	1	0	0	135W	75K	105K	34K	80.6K	270K	7.5A
0	0	0	1	0	120W						6.63A
0	0	0	0	1	90W						5.04A
1	0	0	0	0	65W						3.87A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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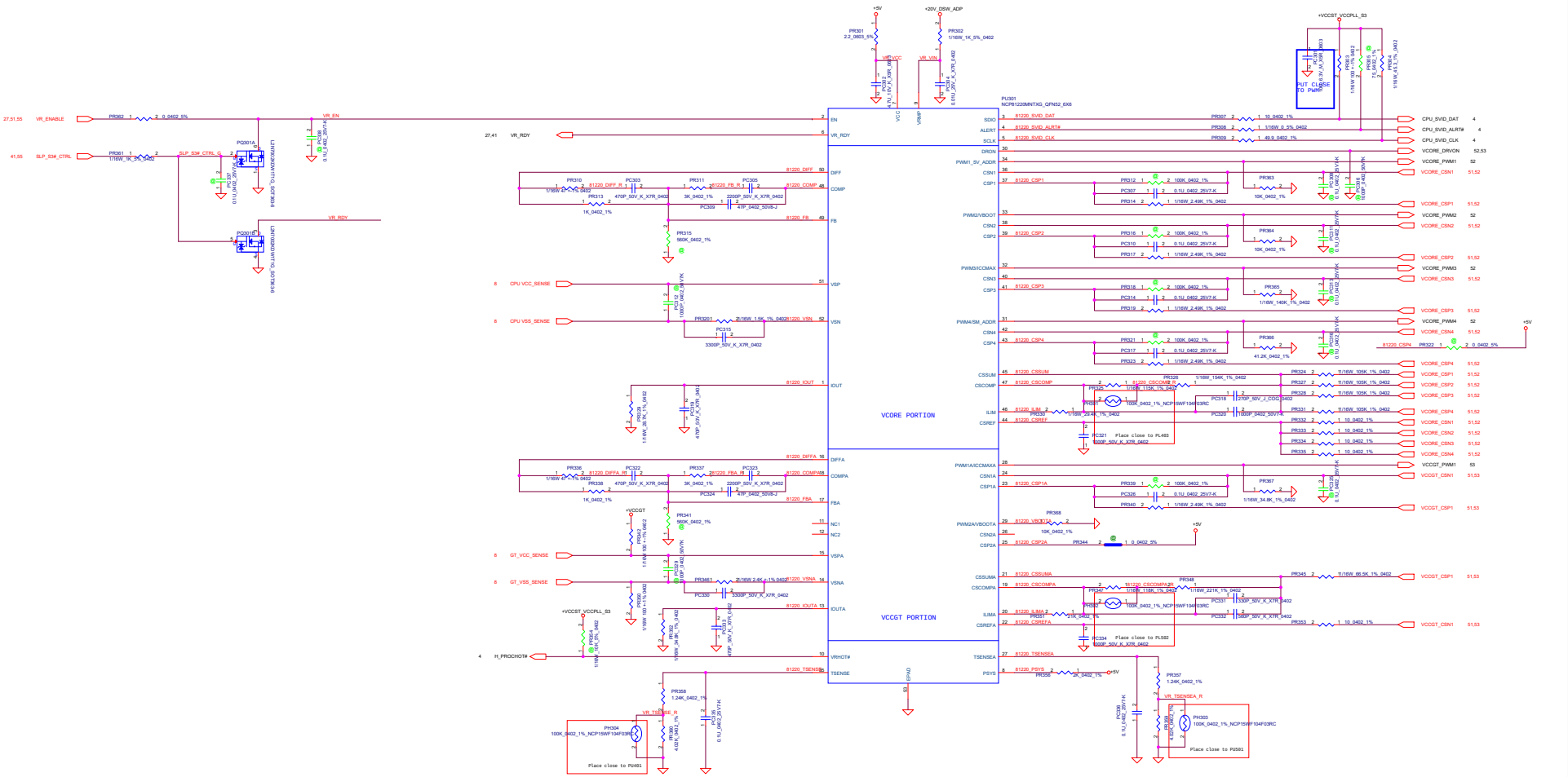
Title: PWR-DC_IN/ RTC Battery

Size: C | Document Number: G0498 | Rev: 0.1

Date: Monday, March 23, 2020 | Sheet 36 of 64



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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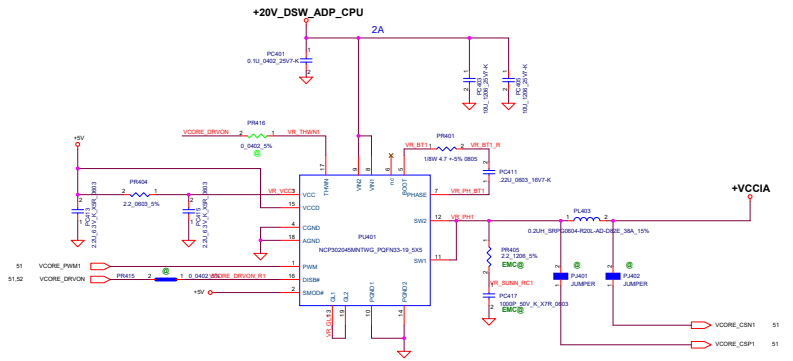
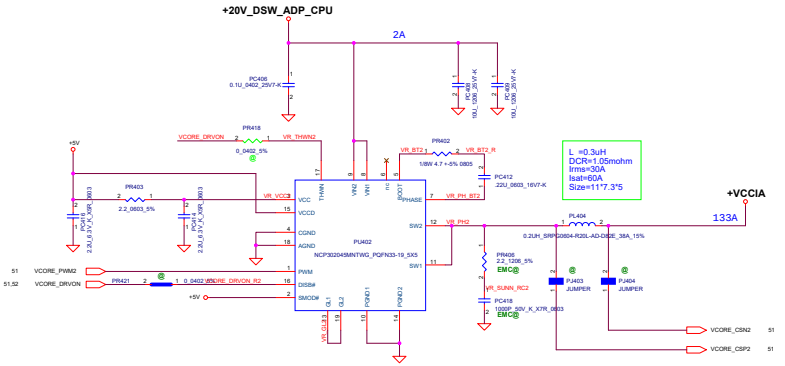
Title: PWR-IMVP8-ON_NCP81220

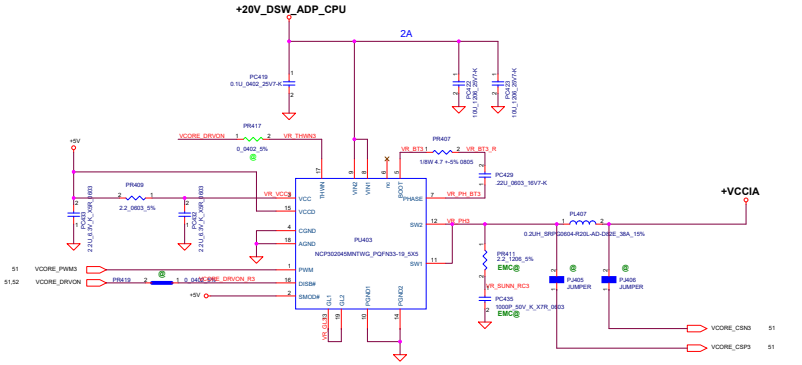
Size: C | Document Number: G0499 | Rev: 0.1

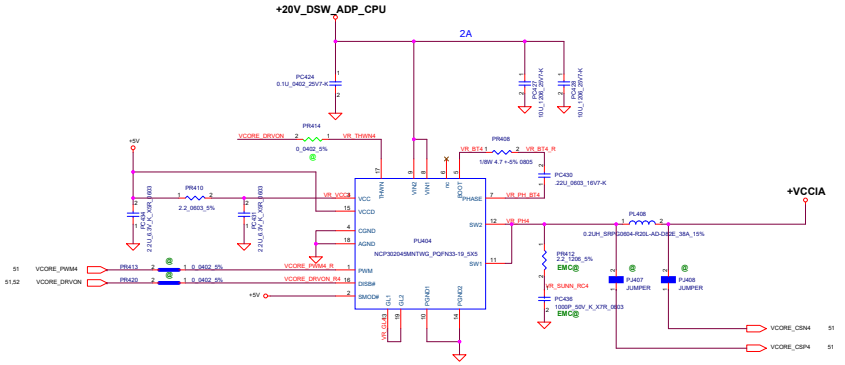
Date: Monday, March 23, 2020 | Sheet 51 of 64

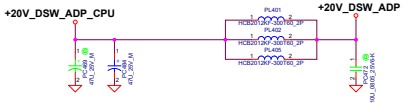


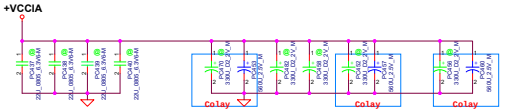


VID=0 V-1.52 V
Vboot=0V
DCR=1.05mohm
Irms=30A
LIR=33%
TDC/Iccmax=91/133A
OCP=150%~200%
OVP=Vout+200mV
UVP=Vout-300mV
Fsw=400KHz
Vin_Irms =9.7A
MLCC ripple current = 7.6A
Cin_CAP =187uF
Cout_CAP =2633uF

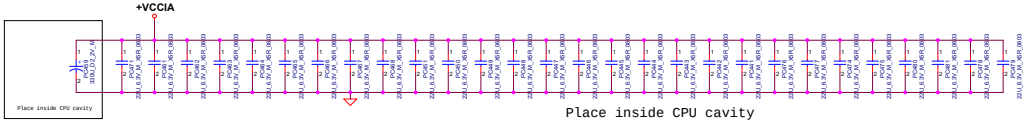








Place outside CPU cavity



Place inside CPU cavity

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Title: PWR-IMVP8-CPU_VCCIA

Size: C | Document Number: G0499 | Rev: 0.1

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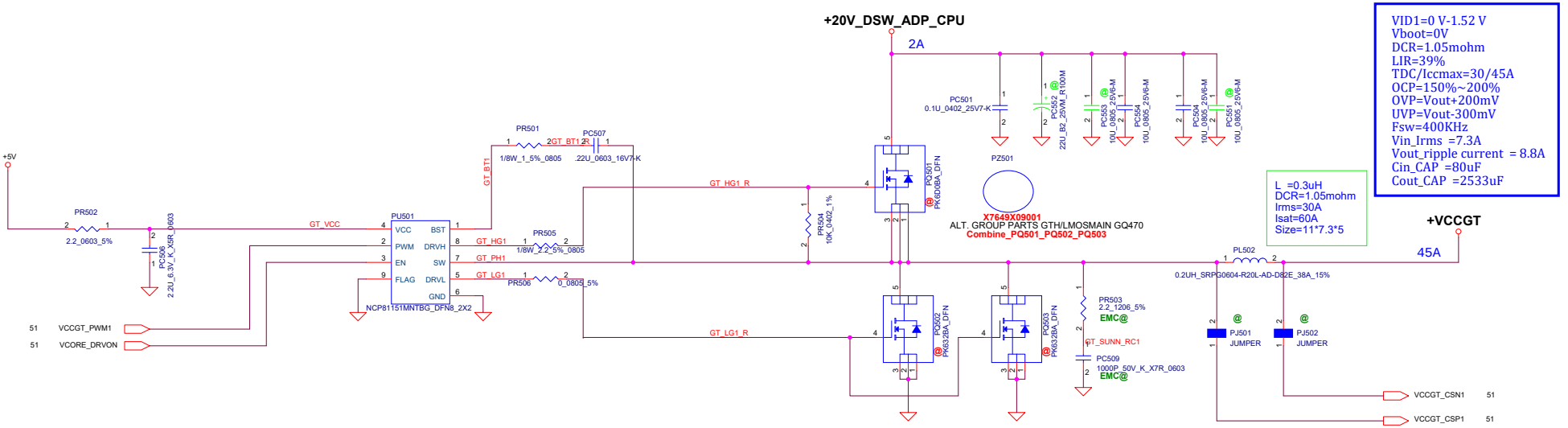

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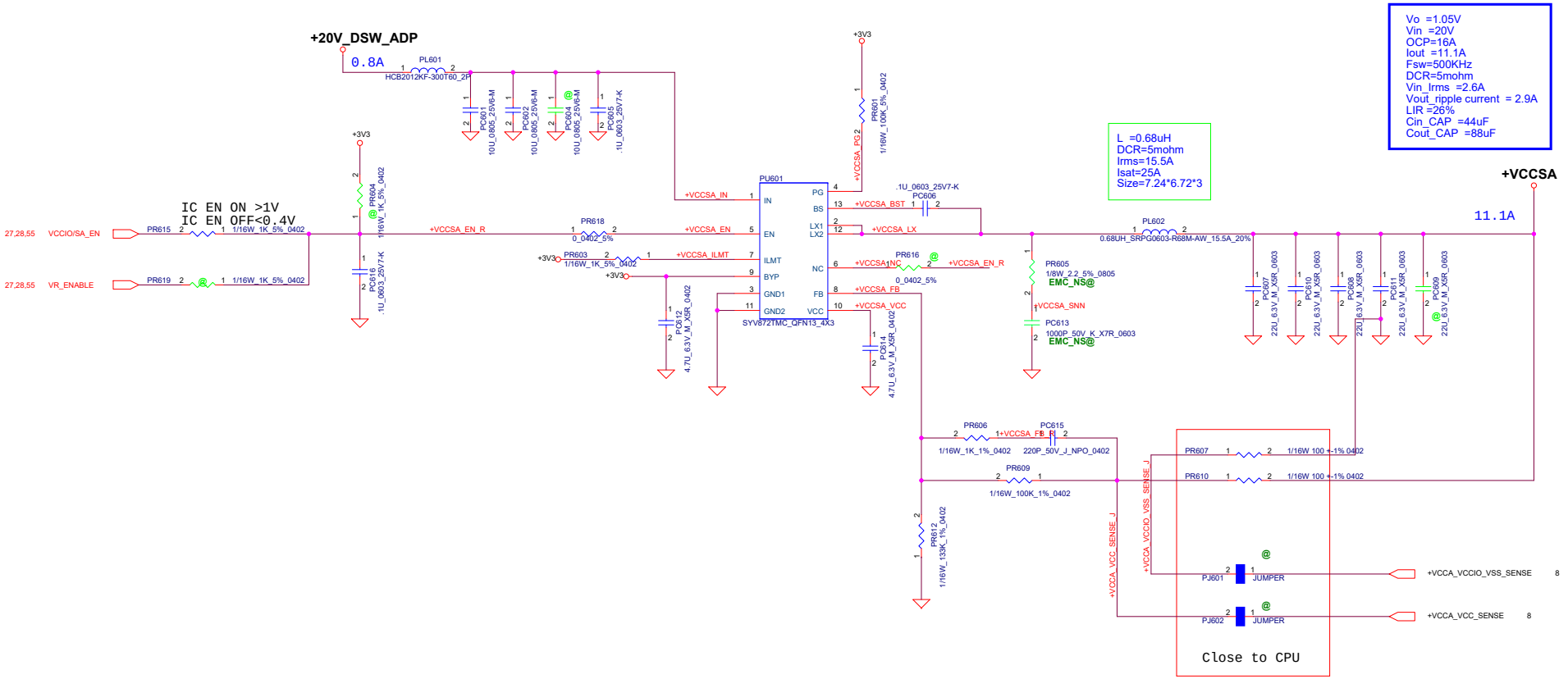
Title: PWR-IMVP8-VCCGT

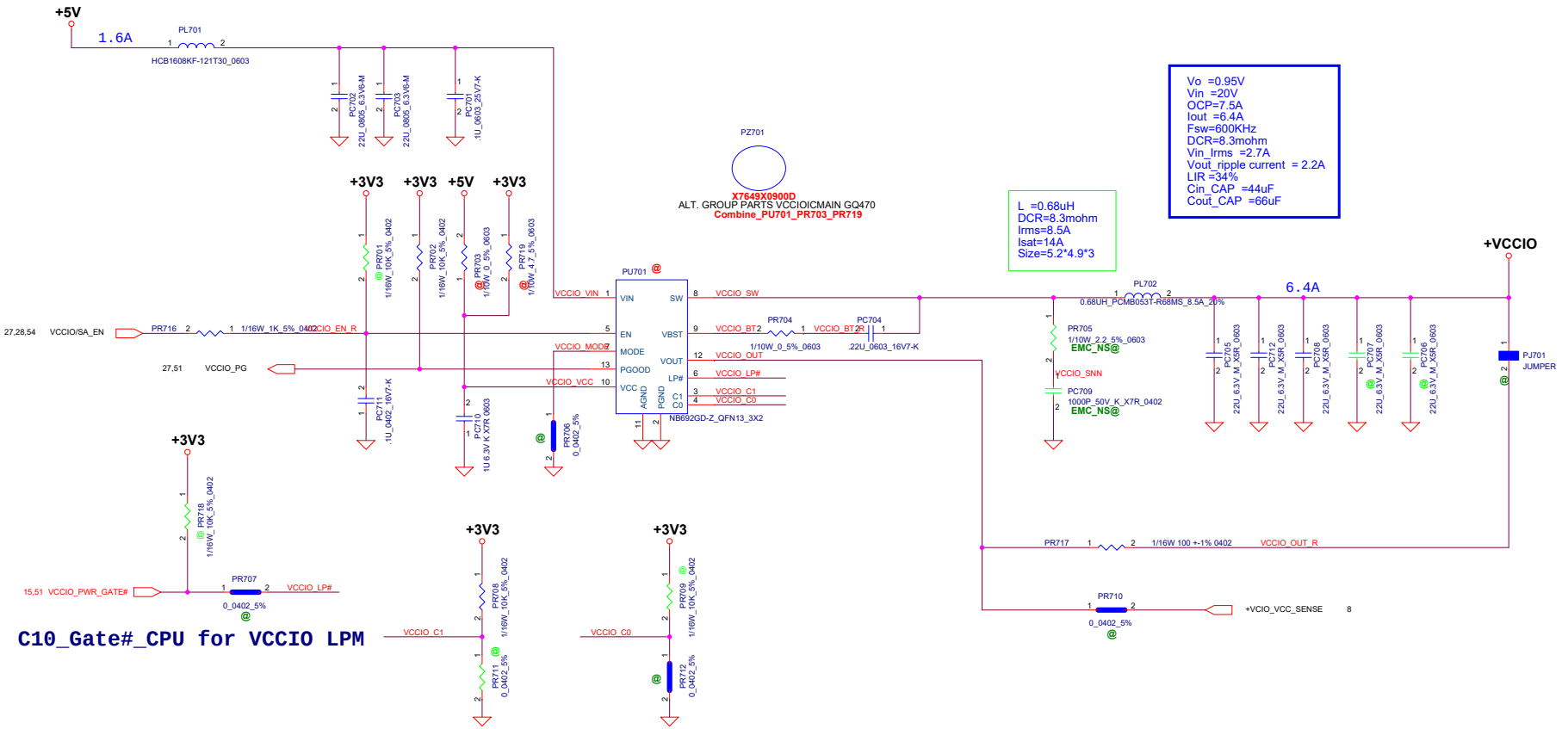
Size: C | Document Number: GQ490 | Rev: 0.1

Date: Monday, March 23, 2020 | Sheet 53 of 64



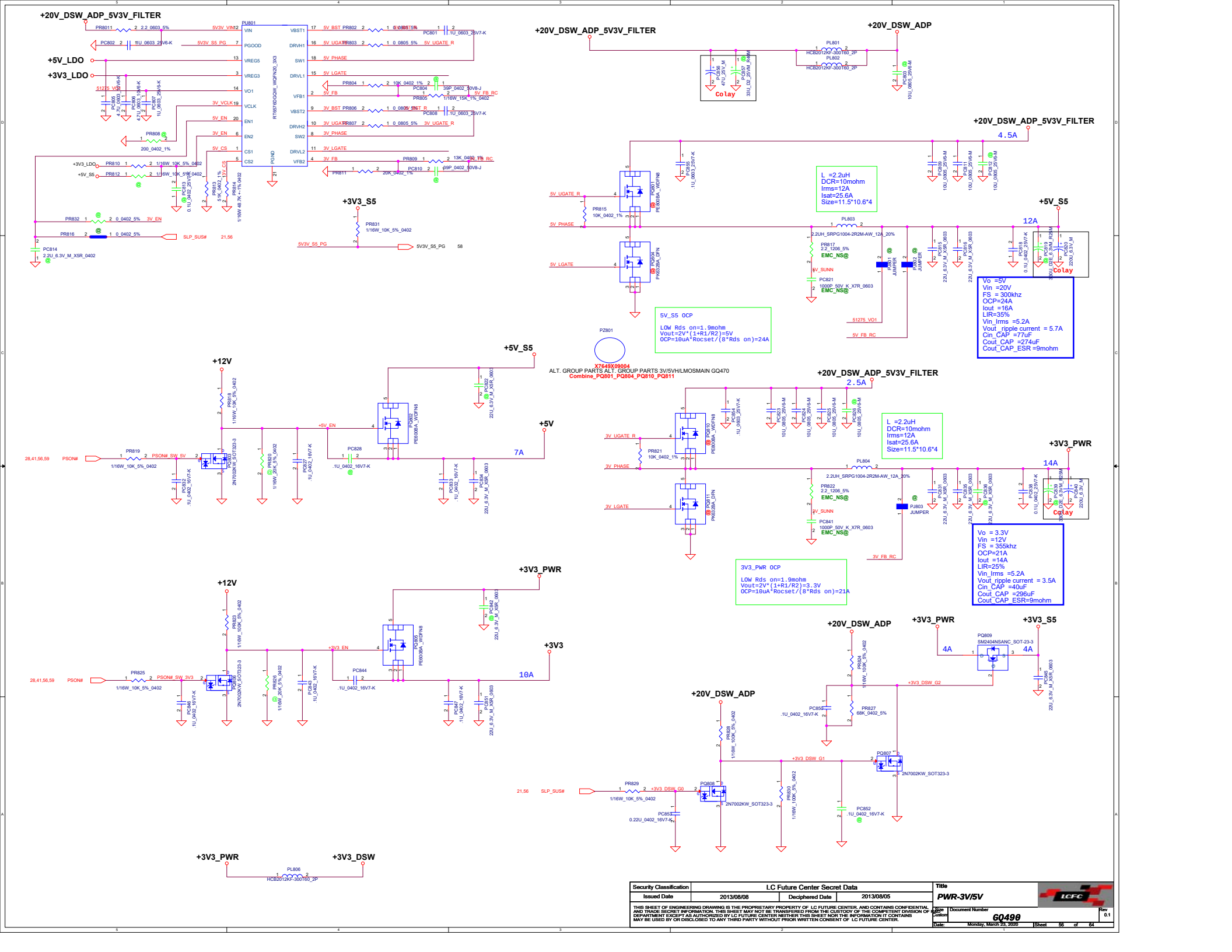
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	PWR-IMVP8-VCCSA		
Size C	Document Number GQ490		Rev 0.1
Date: Monday, March 23, 2020	Sheet 54 of 64		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	PWR-VCCIO		
Size	Document Number		Rev
C	GQ490		0.1
Date:	Monday, March 23, 2020	Sheet	55 of 64


+20V_DSW_ADP_5V3V_FILTER
PU801
RT6576BGQW_WDFN20_3X3
5V3V_VIN
5V3V_S5_PG
PGOOD
+5V_LDO
+3V3_LDO
VREG5
VREG3
VO1
3V_VCLK
VCLK
5V_EN
EN1
3V_EN
EN2
5V_CS
CS1
CS2
PGND
5V_BST
5V_UGATE
5V_PHASE
5V_LGATE
5V_FB
3V_BST
3V_UGATE
3V_PHASE
3V_LGATE
3V_FB
SLP_SUS#
+3V_LDO
+5V_S5
+3V3_S5
5V3V_S5_PG
+20V_DSW_ADP
Colay
+20V_DSW_ADP_5V3V_FILTER
4.5A
L =2.2uH
DCR=10mohm
Irms=12A
Isat=25.6A
Size=11.5*10.6*4
+5V_S5
12A
5V_S5 OCP
LOW Rds on=1.9mohm
Vout=2V*(1+R1/R2)=5V
OCP=10uA*Rocset/(8*Rds on)=24A
Vo =5V
Vin =20V
FS = 300khz
OCP=24A
Iout =16A
LIR=35%
Vin_Irms =5.2A
Vout_ripple current = 5.7A
Cin_CAP =77uF
Cout_CAP =274uF
Cout_CAP_ESR =9mohm
PZ801
X7649X09004
ALT. GROUP PARTS ALT. GROUP PARTS 3V/5VH/LMOSMAIN GQ470
Combine_PQ801_PQ804_PQ810_PQ811
+12V
+5V
7A
+20V_DSW_ADP_5V3V_FILTER
2.5A
+3V3_PWR
14A
3V_FB_RC
3V3_PWR OCP
LOW Rds on=1.9mohm
Vout=2V*(1+R1/R2)=3.3V
OCP=10uA*Rocset/(8*Rds on)=21A
Vo = 3.3V
Vin =12V
FS = 355khz
OCP=21A
Iout =14A
LIR=25%
Vin_Irms =5.2A
Vout_ripple current = 3.5A
Cin_CAP =40uF
Cout_CAP =296uF
Cout_CAP_ESR=9mohm
+3V3
10A
+20V_DSW_ADP
+3V3_PWR
+3V3_S5
4A
+3V3_DSW_G2
+3V3_DSW_G1
+3V3_DSW_G0
+3V3_DSW
PL806
HCB2012KF-300T60_2P
Security Classification
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Issued Date
2013/08/08
Deciphered Date
2013/08/05
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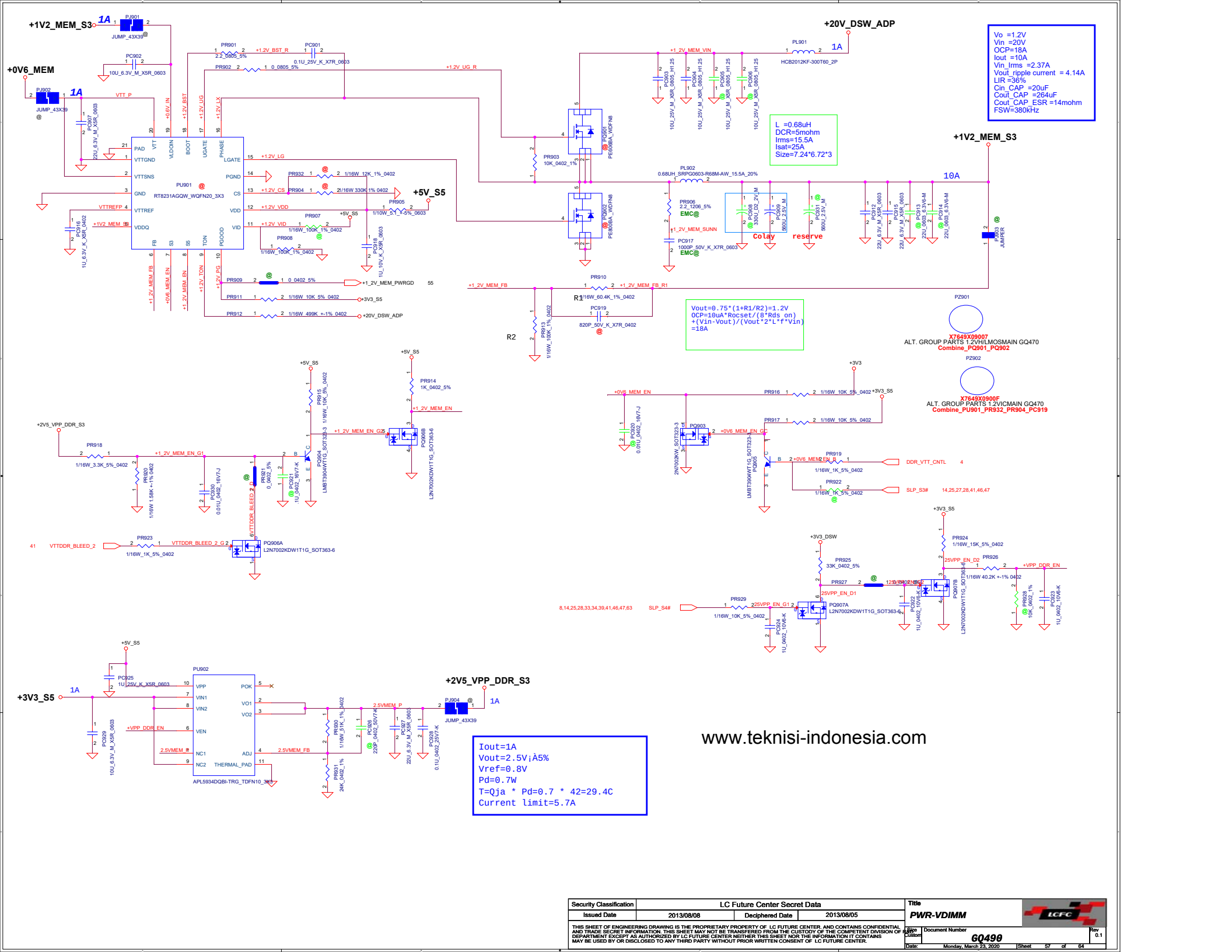

Security Classification	LC Future Center Secret Data		
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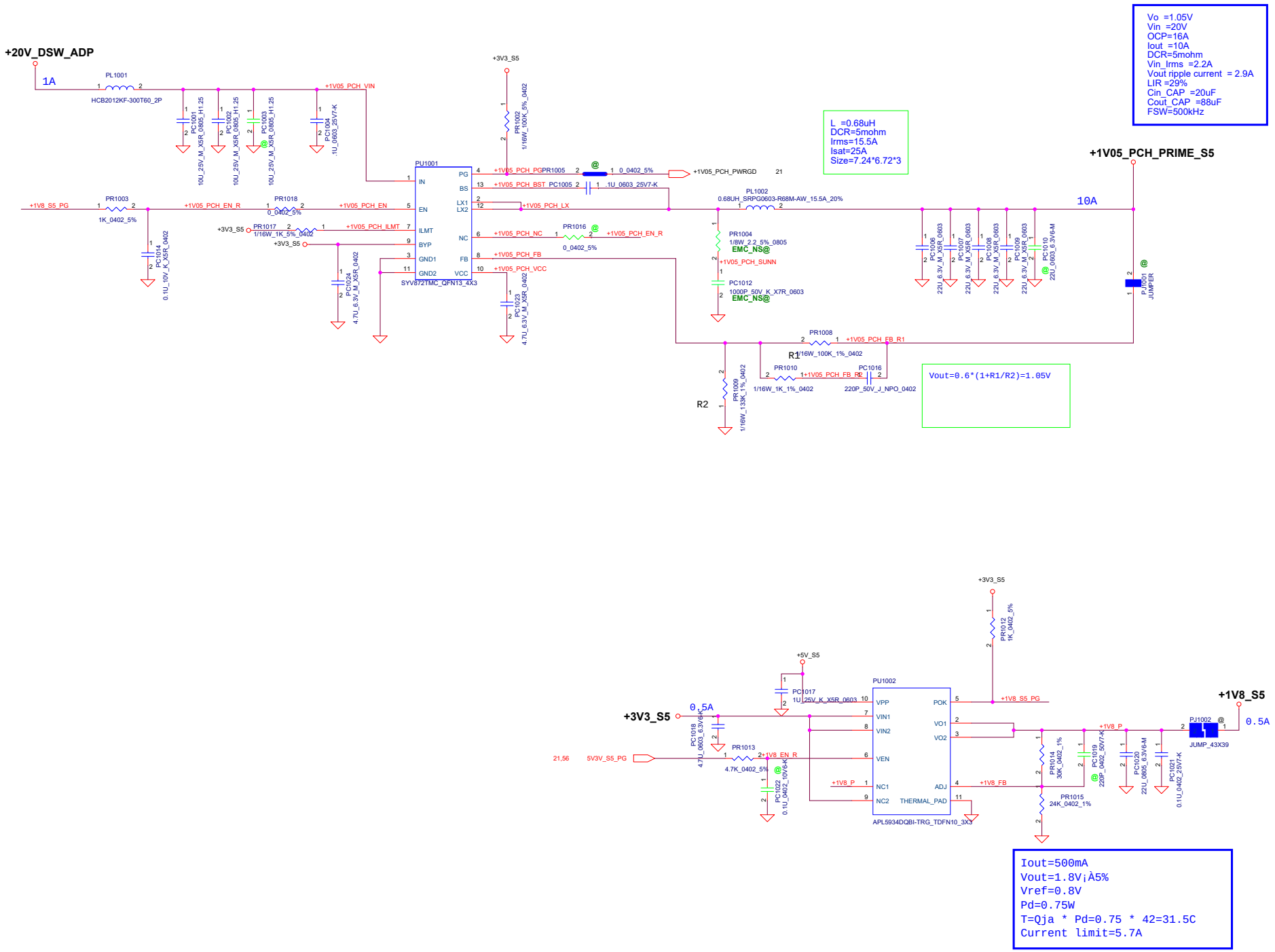
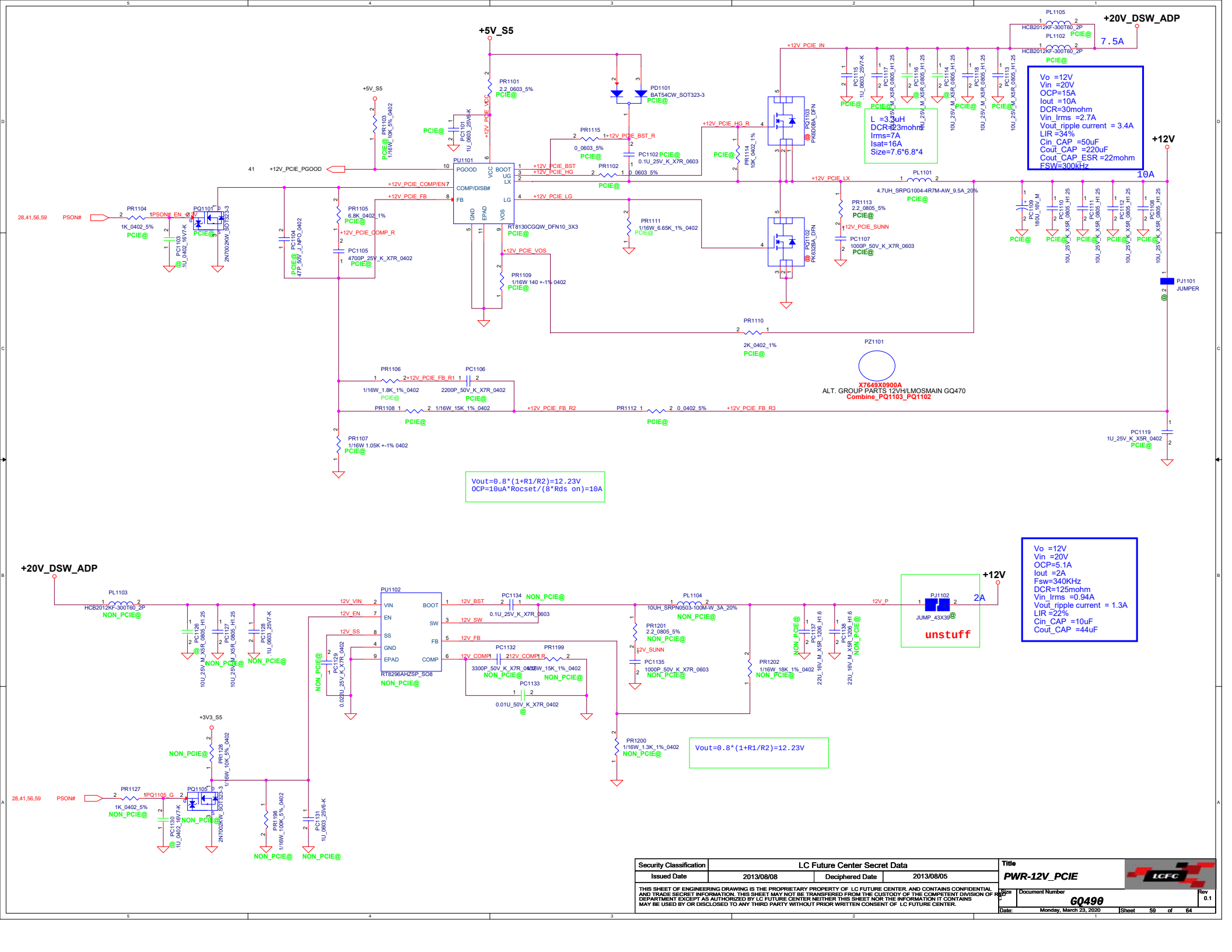
Title	PWR-VDIMM		
Size: Custom	Document Number: GQ490		Rev: 0.1
Date: Monday, March 23, 2020	Sheet 57 of 64		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	PWR-1V05_PCH/1V8_S5		
Size: C	Document Number: GQ490		Rev: 0.1
Date: Monday, March 23, 2020	Sheet 58 of 64		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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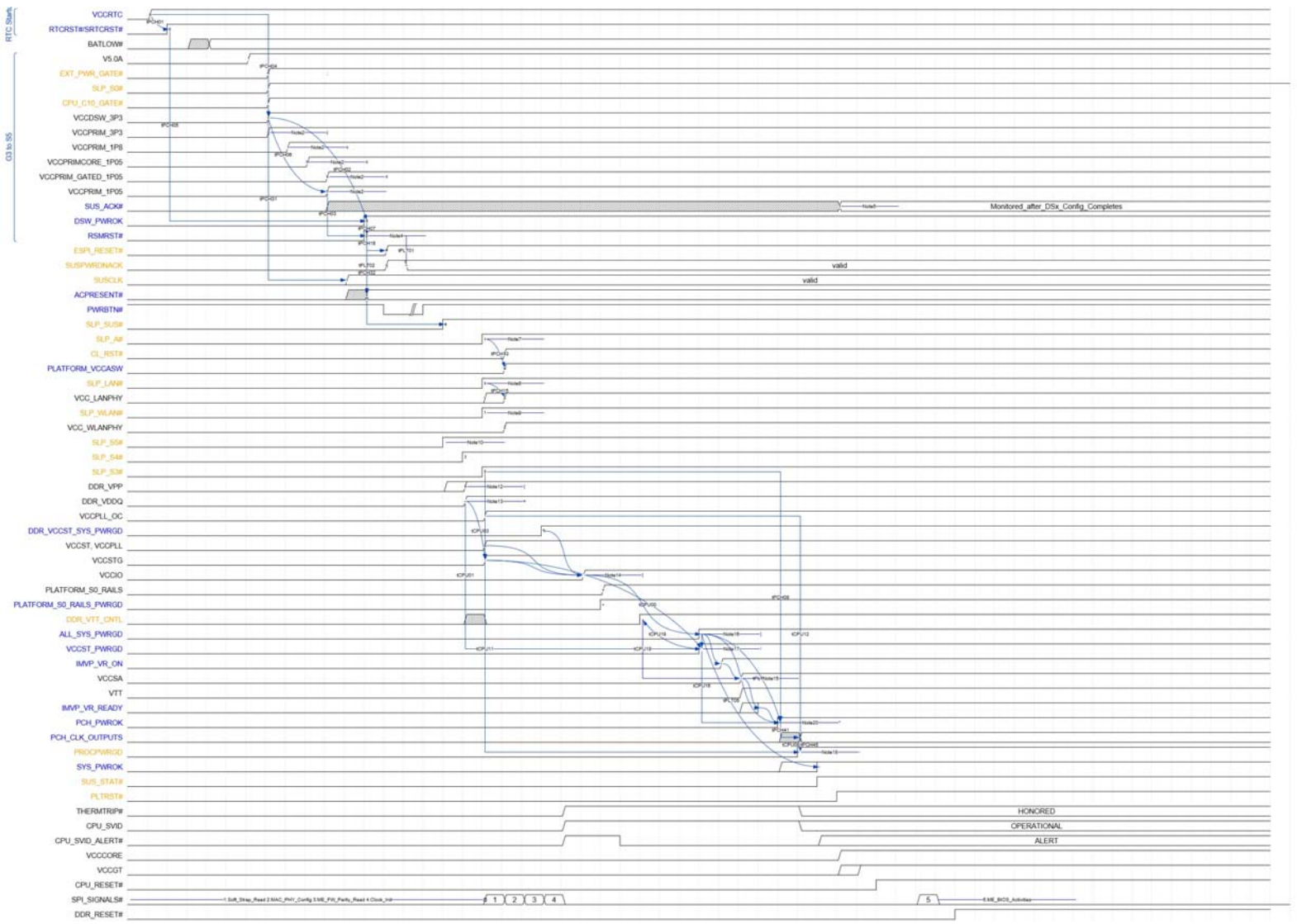
Title: PWR-12V_PCIE

Size: C | Document Number: GQ490 | Rev: 0.1

Date: Monday, March 23, 2020 | Sheet 59 of 64



with Deep Sx support

source	destination		G3	DEEP S5	S0
board	PCH	VBAT			
board	PCH	RTCRST#			
PSU	board	+5VSB_DSW			
board	PCH	+3VSB_DSW			
board	PCH	PCH_DPWROK			
PCH	SIO	PCH_SUSWARN#			
SIO	PCH	PCH_SUSACK#			
PCH	SIO	SLP_SUS#			
board	board	+5V_S5			
board	PCH	+3V3_S5			
board	PCH	+1V0_PCH			
SIO	PCH	RSMRST#			

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: POWER Sequence(G3-S0)

Size: Custom	Document Number: GH470		Rev: 1a
Date: Monday, March 28, 2016	Sheet 65 of 84		

GPIO	Power Well	Select In/Out	Select Native	Tiny6 Usage
GPP_A0	+1.8_S5	NATIVE	ESPI_ALERT1#	ESPI_ALERT1#
GPP_A1	+1.8_S5	NATIVE	ESPI_IO0	ESPI_IO0
GPP_A2	+1.8_S5	NATIVE	ESPI_IO1	ESPI_IO1
GPP_A3	+1.8_S5	NATIVE	ESPI_IO2	ESPI_IO2
GPP_A4	+1.8_S5	NATIVE	ESPI_IO3	ESPI_IO3
GPP_A5	+1.8_S5	NATIVE	ESPI_CS0#	ESPI_CS0#
GPP_A6	+1.8_S5	NATIVE	ESPI_CS1#	ESPI_CS1#
GPP_A7	+1.8_S5	NATIVE	ESPI_ALERT0#	ESPI_ALERT0#
GPP_A8	+1.8_S5	NATIVE	CLKRUN#	CLKRUN#
GPP_A9	+1.8_S5	NATIVE	ESPI_CLK	ESPI_CLK
GPP_A10	+1.8_S5	NATIVE		NC
GPP_A11	+1.8_S5	NATIVE	PME#	SIO_PME#
GPP_A12	+1.8_S5	NATIVE		NC
GPP_A13	+1.8_S5	NATIVE	SUSWARN#	SUSWARN#
GPP_A14	+1.8_S5	NATIVE	ESPI_RESET#	ESPI_RESET#
GPP_A15	+1.8_S5	NATIVE	SUSACK#	SUSACK#
GPP_A16	+1.8_S5	NATIVE		NC
GPP_A17	+1.8_S5	NATIVE		NC
GPP_A18	+1.8_S5	NATIVE		NC
GPP_A19	+1.8_S5	NATIVE		NC
GPP_A20	+1.8_S5	NATIVE		NC
GPP_A21	+1.8_S5	NATIVE		NC
GPP_A22	+1.8_S5	NATIVE		NC
GPP_A23	+1.8_S5	NATIVE		NC
GPP_B0	+3V3_S5	NATIVE		NC
GPP_B1	+3V3_S5	NATIVE		NC
GPP_B2	+3V3_S5	NATIVE		NC
GPP_B3	+3V3_S5	GPIO	GPP_B3	M.2_BT_DISABLE#
GPP_B4	+3V3_S5	NATIVE		NC
GPP_B5	+3V3_S5	NATIVE	SRCCLKREQ0#	CLK_REQ0_PCIEX8#
GPP_B6	+3V3_S5	NATIVE	SRCCLKREQ1#	CLK_REQ1_PCIEX8#
GPP_B7	+3V3_S5	NATIVE	SRCCLKREQ2#	CLK_REQ2_SLOTX4#
GPP_B8	+3V3_S5	NATIVE	SRCCLKREQ3#	CLK_REQ3_M.2_WLAN#
GPP_B9	+3V3_S5	NATIVE	SRCCLKREQ4#	CLK_REQ4_M.2_SSD1#
GPP_B10	+3V3_S5	NATIVE	SRCCLKREQ5#	CLK_REQ5_PCIEX8#
GPP_B11	+3V3_S5	NATIVE		NC
GPP_B12	+3V3_S5	NATIVE	SLP_S0#	SLP_S0#
GPP_B13	+3V3_S5	NATIVE	PLTRST#	PCH_PLT_RST#
GPP_B14	+3V3_S5	NATIVE	SPKR	S_SPKR_OUT
GPP_B15	+3V3_S5	GPI	GPP_B15	DP_D_DET#
GPP_B16	+3V3_S5	NATIVE		NC
GPP_B17	+3V3_S5	NATIVE		NC
GPP_B18	+3V3_S5	NATIVE	GSPIO_MOSI	PCH_STRAP_GPP_B18
GPP_B19	+3V3_S5	GPI	GPP_B19	TYPE_C_POL#
GPP_B20	+3V3_S5	GPO	GPP_B20	GPU_MACO_EN
GPP_B21	+3V3_S5	NATIVE		NC
GPP_B22	+3V3_S5	NATIVE	GSPI1_MOSI	PCH_STRAP_GPP_B22
GPP_B23	+3V3_S5	NATIVE	SML1ALERT#	SML1ALERT#
GPP_C0	+3V3_S5	NATIVE	SMBCLK	SMB_CLK_SUS
GPP_C1	+3V3_S5	NATIVE	SMBDATA	SMB_DATA_SUS
GPP_C2	+3V3_S5	NATIVE	SMBALERT#	SMBALERT#
GPP_C3	+3V3_S5	NATIVE	SML0CLK	SML0_CLK_LAN
GPP_C4	+3V3_S5	NATIVE	SML0DATA	SML0_DATA_LAN
GPP_C5	+3V3_S5	NATIVE	SML0ALERT#	SML0ALERT#0
GPP_C6	+3V3_S5	NATIVE		NC
GPP_C7	+3V3_S5	NATIVE		NC
GPP_C8	+3V3_S5	GPI	GPP_C8	CLEAR_CMOS#
GPP_C9	+3V3_S5	GPI	GPP_C9	COM_B_DET#
GPP_C10	+3V3_S5	NATIVE		NC
GPP_C11	+3V3_S5	NATIVE		NC
GPP_C12	+3V3_S5	NATIVE		NC
GPP_C13	+3V3_S5	GPO		GPU_PWR_EN
GPP_C14	+3V3_S5	NATIVE		NC
GPP_C15	+3V3_S5	GPO	GPP_C15	PW_LED#
GPP_C16	+3V3_S5	NATIVE		NC
GPP_C17	+3V3_S5	NATIVE		NC
GPP_C18	+3V3_S5	NATIVE	I2C1_SDA	I2C1_DATA
GPP_C19	+3V3_S5	NATIVE	I2C1_SCL	I2C1_CLK
GPP_C20	+3V3_S5	NATIVE		NC
GPP_C21	+3V3_S5	NATIVE		NC
GPP_C22	+3V3_S5	GPI	GPP_C22	TYPE_C_POL#
GPP_C23	+3V3_S5	NATIVE		NC

GPIO	Power Well	Select In/Out	Select Native	Tiny6 Usage
GPP_D0	+1.8_S5	NATIVE		NC
GPP_D1	+1.8_S5	NATIVE		NC
GPP_D2	+1.8_S5	NATIVE		NC
GPP_D3	+1.8_S5	NATIVE		NC
GPP_D4	+1.8_S5	NATIVE		NC
GPP_D5	+1.8_S5	NATIVE	CNV_RF_RESET#	CRF_RST#_PCH
GPP_D6	+1.8_S5	NATIVE	MODEM_CLKREQ	CNVI_CLKREQ0
GPP_D7	+1.8_S5	NATIVE		GPP_D7
GPP_D8	+1.8_S5	NATIVE		NC
GPP_D9	+1.8_S5	NATIVE		NC
GPP_D10	+1.8_S5	NATIVE		NC
GPP_D11	+1.8_S5	GPI		USB_DET#
GPP_D12	+1.8_S5	NATIVE		NC
GPP_D13	+1.8_S5	NATIVE		NC
GPP_D14	+1.8_S5	NATIVE		NC
GPP_D15	+1.8_S5	NATIVE		NC
GPP_D16	+1.8_S5	NATIVE		NC
GPP_D17	+1.8_S5	NATIVE		NC
GPP_D18	+1.8_S5	NATIVE		NC
GPP_D19	+1.8_S5	NATIVE		NC
GPP_D20	+1.8_S5	NATIVE		NC
GPP_D21	+1.8_S5	NATIVE		NC
GPP_D22	+1.8_S5	NATIVE		NC
GPP_D23	+1.8_S5	NATIVE		NC
GPP_E0	+3V3_S5	GPO	GPP_E0	WWAN_POWER_OFF#
GPP_E1	+3V3_S5	GPO	GPP_E1	PM_WWAN_DISABLE#
GPP_E2	+3V3_S5	GPI		PWR_PROTECT#
GPP_E3	+3V3_S5	NATIVE		NC
GPP_E4	+3V3_S5	NATIVE		NC
GPP_E5	+3V3_S5	GPI	GPP_E5	BMC_DETECT#
GPP_E6	+3V3_S5	GPO	GPP_E6	CNVI_EN#
GPP_E7	+3V3_S5	NATIVE		NC
GPP_E8	+3V3_S5	NATIVE	SATALED#	SATA_LED_IN#
GPP_E9	+3V3_S5	NATIVE	USB2_OC0#	USB_OC0_INT#
GPP_E10	+3V3_S5	NATIVE	USB2_OC1#	USB_OC1_FRONT_CHG#
GPP_E11	+3V3_S5	NATIVE	USB2_OC2#	TYPE_C_OCP#
GPP_E12	+3V3_S5	NATIVE	USB2_OC3#	USB_OC3_REAR3#
GPP_F0	+3V3_S5	GPI	GPP_F2	PWR_THROTTLE#
GPP_F1	+3V3_S5	GPI	GPP_F1	M.2_SSD_PEDET2#
GPP_F2	+3V3_S5	GPO		TBT_PERST#
GPP_F3	+3V3_S5	GPI	GPP_F3	WWAN_DET#
GPP_F4	+3V3_S5	NATIVE		NC
GPP_F5	+3V3_S5	NATIVE	GPP_F5	TPM_SPI_IRQ#
GPP_F6	+3V3_S5	NATIVE	SATA_DEVSLP4	SSD_SATA_DEVSLP2
GPP_F7	+3V3_S5	NATIVE		NC
GPP_F8	+3V3_S5	NATIVE		NC
GPP_F9	+3V3_S5	NATIVE		NC
GPP_F10	+3V3_S5	NATIVE		NC
GPP_F11	+3V3_S5	NATIVE		NC
GPP_F12	+3V3_S5	NATIVE		NC
GPP_F13	+3V3_S5	NATIVE		NC
GPP_F14	+3V3_S5	NATIVE	PS_ON#	PCH_PS_ON#
GPP_F15	+3V3_S5	NATIVE	USB2_OC4#	USB_OC4_REAR_ODD#
GPP_F16	+3V3_S5	NATIVE	USB2_OC5#	USB_OC5_REAR4#
GPP_F17	+3V3_S5	NATIVE	USB2_OC6#	USB_OC6_REAR2#
GPP_F18	+3V3_S5	NATIVE	USB2_OC7#	OC7#
GPP_F19	+3V3_S5	NATIVE		NC
GPP_F20	+3V3_S5	NATIVE		NC
GPP_F21	+3V3_S5	NATIVE		NC
GPP_F22	+3V3_S5	GPO	GPP_F22	GPU_RST#
GPP_F23	+3V3_S5	GPO	GPP_F23	GPP_F23

GPIO	Power Well	Select In/Out	Select Native	Tiny6 Usage
GPP_G0	+3V3_S5	GPI	GPP_G0	USBDEBUG
GPP_G1	+3V3_S5	NATIVE		NC
GPP_G2	+3V3_S5	GPI	GPP_G2	PCIE_X8_X4_PRSNT#
GPP_G3	+3V3_S5	NATIVE		NC
GPP_G4	+3V3_S5	GPI	GPP_G4	MS_EVENT_PCH
GPP_G5	+3V3_S5	GPO	GPP_G5	ME_RECOVERY_BMC
GPP_G6	+3V3_S5	NATIVE		NC
GPP_G7	+3V3_S5	GPO	GPP_G7	WWAN_RST#
GPP_H0	+3V3_S5	NATIVE	SRCCLKREQ6#	CLK_REQ6_LAN#
GPP_H1	+3V3_S5	NATIVE		NC
GPP_H2	+3V3_S5	NATIVE		NC
GPP_H3	+3V3_S5	NATIVE	SRCCLKREQ9#	CLK_REQ9_WWAN#
GPP_H4	+3V3_S5	NATIVE	SRCCLKREQ10#	CLK_REQ10_M.2_SSD2#
GPP_H5	+3V3_S5	NATIVE	SRCCLKREQ11#	CLK_REQ11_PCIEX8#
GPP_H6	+3V3_S5	GPI	GPP_H6	PCIE_WLAN_WAKE#
GPP_H7	+3V3_S5	GPO	GPP_H7	PCH_SYSFAN_PWREN
GPP_H8	+3V3_S5	NATIVE		NC
GPP_H9	+3V3_S5	NATIVE		NC
GPP_H10	+3V3_S5	GPO		NC
GPP_H11	+3V3_S5	GPO	GPP_H11	M.2_WLAN_DISABLE#
GPP_H12	+3V3_S5	NATIVE	SML2ALERT#	PCH_STRAP_GPP_H12
GPP_H13	+3V3_S5	NATIVE		NC
GPP_H14	+3V3_S5	NATIVE		NC
GPP_H15	+3V3_S5	NATIVE	SML3ALERT#	TBT_WAKE#
GPP_H16	+3V3_S5	GPI	GPP_H6	GPP_H16
GPP_H17	+3V3_S5	NATIVE		NC
GPP_H18	+3V3_S5	NATIVE		NC
GPP_H19	+3V3_S5	NATIVE		NC
GPP_H20	+3V3_S5	NATIVE		NC
GPP_H21	+3V3_S5	GPI		COM_A_DET#
GPP_H22	+3V3_S5	NATIVE		NC
GPP_H23	+3V3_S5	NATIVE		NC
GPP_I0	+3V3_S5	NATIVE	DDPB_HPD0	DDPB_HPD_PD
GPP_I1	+3V3_S5	NATIVE	DDPC_HPD1	DDPC_HPD_PD
GPP_I2	+3V3_S5	NATIVE	DDPD_HPD2	DDPD_HPD_PD
GPP_I3	+3V3_S5	NATIVE	DDPE_HPD3	DDPE_HPD3
GPP_I4	+3V3_S5	NATIVE	EDP_HPD	GPP_I4
GPP_I5	+3V3_S5	NATIVE	DDPB_CTRLCLK	DDPB_CTRLCLK
GPP_I6	+3V3_S5	NATIVE	DDPB_CTRLDATA	DDPB_CTRLDATA
GPP_I7	+3V3_S5	NATIVE	DDPC_CTRLCLK	DDPC_CTRLCLK
GPP_I8	+3V3_S5	NATIVE	DDPC_CTRLDATA	DDPC_CTRLDATA
GPP_I9	+3V3_S5	NATIVE	DDPD_CTRLCLK	DDPD_CTRLCLK
GPP_I10	+3V3_S5	NATIVE	DDPD_CTRLDATA	DDPD_CTRLDATA
GPP_I11	+3V3_S5	GPI		H_SKTOCC#
GPP_I12	+3V3_S5	NATIVE		NC
GPP_I13	+3V3_S5	NATIVE		NC
GPP_I14	+3V3_S5	NATIVE		NC
GPP_J0	+1.8_S5	NATIVE		NC
GPP_J1	+1.8_S5	NATIVE	CPU_C10_GATE#	VCCIO_PWR_GATE#
GPP_J2	+1.8_S5	NATIVE		NC
GPP_J3	+1.8_S5	NATIVE		NC
GPP_J4	+1.8_S5	NATIVE	CNV_BRI_DT	CNV_BRI_DT
GPP_J5	+1.8_S5	NATIVE	CNV_BRI_RSP	CNV_BRI_RSP
GPP_J6	+1.8_S5	NATIVE	CNV_RGI_DT	CNV_RGI_DT
GPP_J7	+1.8_S5	NATIVE	CNV_RGI_RSP	CNV_RGI_RSP
GPP_J8	+1.8_S5	NATIVE		NC
GPP_J9	+1.8_S5	NATIVE		GPP_J_9_CNV_MFUART2_TXD
GPP_J10	+1.8_S5	NATIVE		NC
GPP_J11	+1.8_S5	NATIVE		NC

GPIO	Power Well	Select In/Out	Select Native	Tiny6 Usage
GPP_K0	+3V3_S5	GPI	GPP_K0	TBT_I2C_ALERT#
GPP_K1	+3V3_S5	NATIVE		NC
GPP_K2	+3V3_S5	NATIVE		NC
GPP_K3	+3V3_S5	NATIVE		NC
GPP_K4	+3V3_S5	GPI		BRD_ID0
GPP_K5	+3V3_S5	GPI		BRD_ID1
GPP_K6	+3V3_S5	GPI		BRD_ID2
GPP_K7	+3V3_S5	GPI		BRD_ID3
GPP_K8	+3V3_S5	GPI		BRD_ID4
GPP_K9	+3V3_S5	GPI		BRD_ID5
GPP_K10	+3V3_S5	NATIVE		NC
GPP_K11	+3V3_S5	NATIVE		NC
GPP_K12	+3V3_S5	GPI	GPP_K12	TBCIO_PLUG_EVENT_R
GPP_K13	+3V3_S5	NATIVE		NC
GPP_K14	+3V3_S5	NATIVE		NC
GPP_K15	+3V3_S5	NATIVE		NC
GPP_K16	+3V3_S5	GPO	GPP_k16	TBT_FRC_PWR
GPP_K17	+3V3_S5	NATIVE		NC
GPP_K18	+3V3_S5	NATIVE	NMI#	FM_NMI_EVENT#
GPP_K19	+3V3_S5	NATIVE	SMI#	SIO_SCI#
GPP_K20	+3V3_S5	GPO		WWAN_PE_RESET#
GPP_K21	+3V3_S5	GPI	GPP_K21	TPM_GPIO (L: TPM stuffed)
GPP_K22	+3V3_S5	GPO	GPP_K23	PCH_PEGSLOT1_PWREN
GPP_K23	+3V3_S5	GPO	GPP_K23	TBT_CIO_PWR_EN
GPD0	+3V3_DSW	NATIVE	BATLOW#	PCH_GP72_PU
GPD1	+3V3_DSW	NATIVE	ACPRESENT	ACPRESENT
GPD2	+3V3_DSW	NATIVE	LAN_WAKE#	LANWAKE_R_N
GPD3	+3V3_DSW	NATIVE	PWRBTN#	PWRBTN#
GPD4	+3V3_DSW	NATIVE	SLP_S3#	SLP_S3#
GPD5	+3V3_DSW	NATIVE	SLP_S4#	SLP_S4#
GPD6	+3V3_DSW	NATIVE	SLP_A#	SLP_A#_PCH
GPD7	+3V3_DSW	NATIVE		GPD7
GPD8	+3V3_DSW	NATIVE	SUSCLK	PCH_SUSCLK
GPD9	+3V3_DSW	NATIVE	SLP_WLAN#	SLP_WLAN#
GPD10	+3V3_DSW	NATIVE	SLP_S5#	SLP_S5#
GPD11	+3V3_DSW	NATIVE	LANPHYPC	L_LAN_DISABLE#

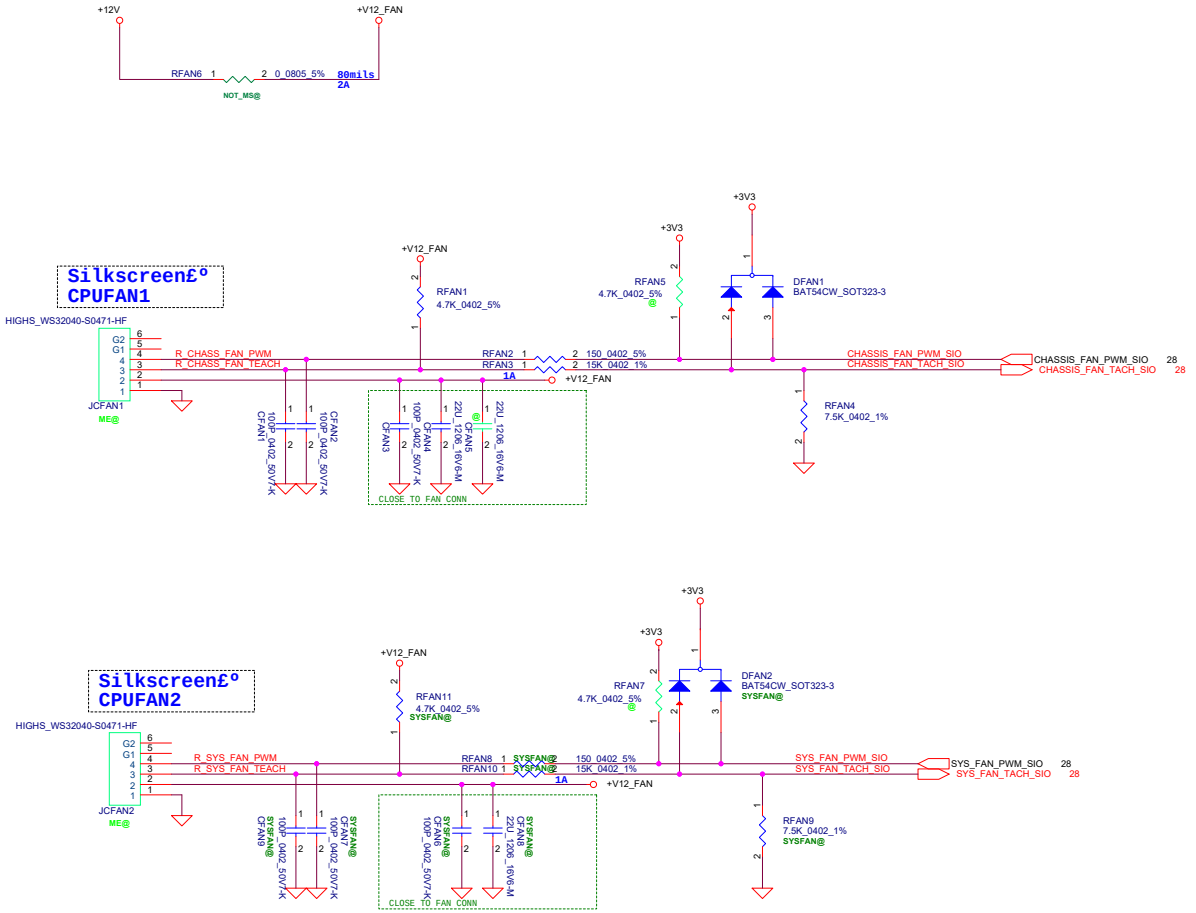
HSIO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	U3-G1/G2#1	U3-G1/G2#2	U3-G1/G2#3	U3-G1/G2#4	U3-G1/G2#5	U3-G1/G2#6	U3-G1#7	U3-G1#8	U3-G1#9	U3-G1#10	PCIe#5	PCIe#6	PCIe#7	PCIe#8	PCIe#9	PCIe#10	PCIe#11	PCIe#12	PCIe#13	PCIe#14	PCIe#15	PCIe#16	PCIe#17	PCIe#18	PCIe#19	PCIe#20	PCIe#21	PCIe#22	PCIe#23	PCIe#24
							PCIe #1	PCIe #2	PCIe #3	PCIe #4	GBE				GBE		SATA 0A	SATA 1A GBE	SATA 0B GBE	SATA #18	SATA #2	SATA #3	SATA #4	SATA #5	SATA #6	SATA #7				
Tiny6-Q470	USB3.1 GEN2	USB3.1 GEN2	USB3.1 GEN2	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	NA	NA	Gbe	PCIE	NA	NA	PCIE X4				SATA	NA	PCIE	NA	PCIE X4 RST				PCIE X4 RST			
Tiny6-H470	USB3.1 GEN2	USB3.1 GEN2	USB3.1 GEN2	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	USB3.1 GEN1	NA	NA	Gbe	PCIE	NA	NA	PCIE X4				SATA	NA	PCIE	NA	PCIE X4 RST				PCIE X4 RST			
	Type-A	Type-A	Type-A	Type-C	Type-A	Type-A	BT® Type-C	Type-C			LAN	WLAN			Riser card X4				SATA		WWAN		M.2 SSD2 Black				M.2 SSD1 White			

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPIO table

Size: C | Document Number: GH470 | Rev: 1.0

Date: Monday, March 23, 2020 | Sheet 61 of 64



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	FAN CTRL		
Size C	Document Number GH470		Rev 1.0
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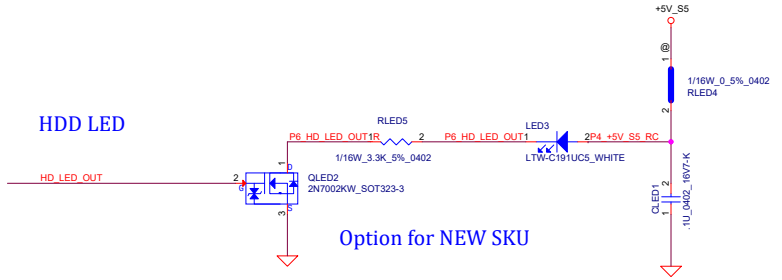
CONTROL PANEL / LED CIRCUITRY

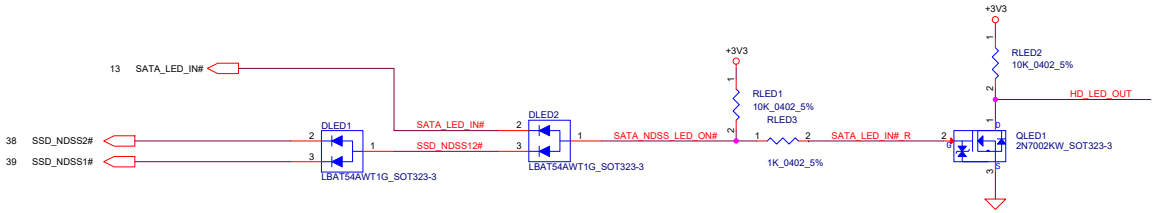


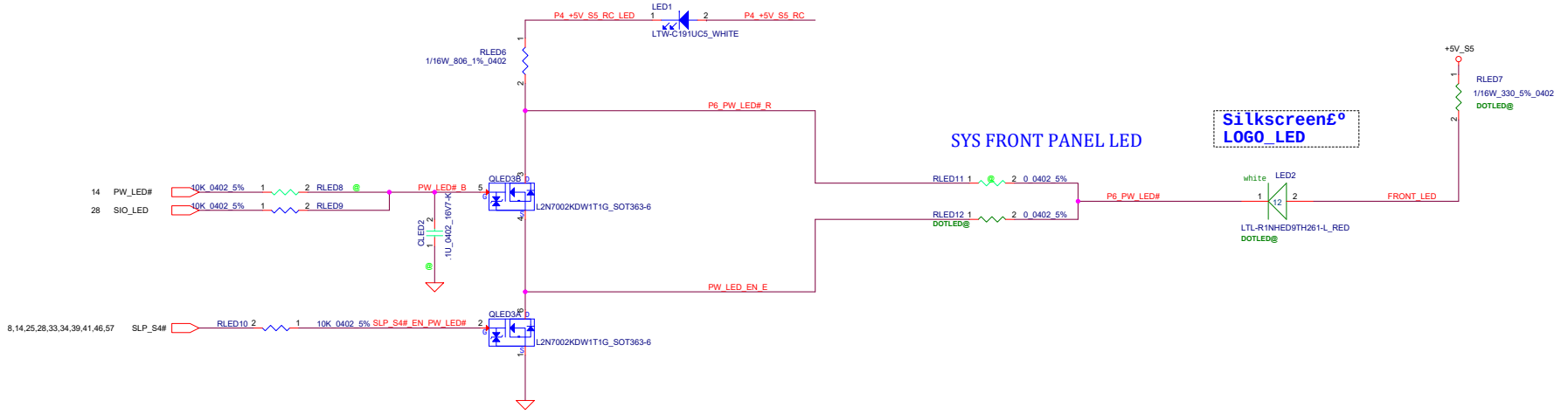
POWER BUTTON & LED

COLOR	Functoin
G	HDD

Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 330ohm = 5mA
5m * 3.2 V = 16 mW
0.1W (For Current limit R)

For NEC SKU:
Remove:
R765Q,Q42,R762
SW1
CR1
Install :
R779
SW1_
CR1_





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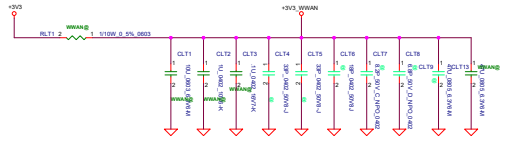
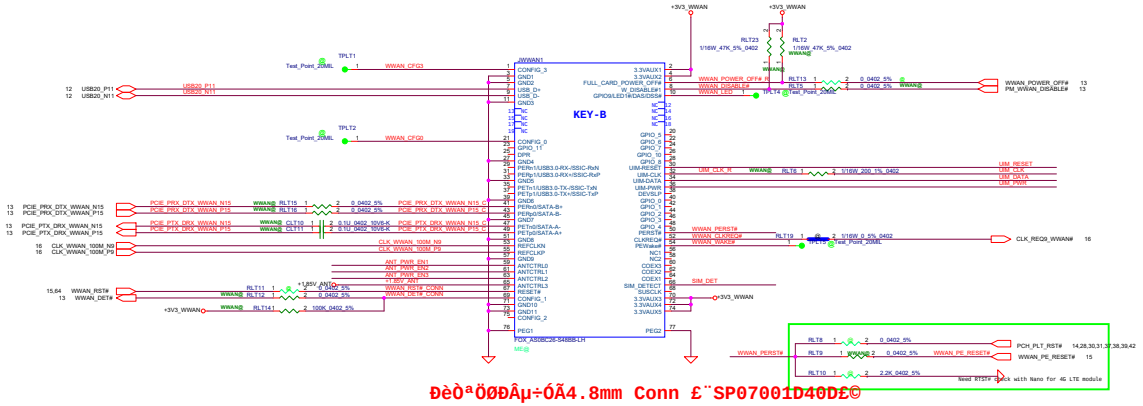
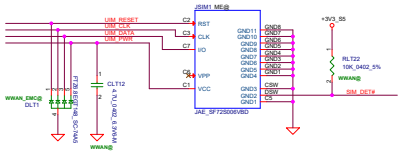
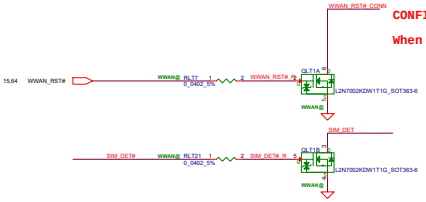
TYPE-B NGFF LTE CARD FOR WWAN

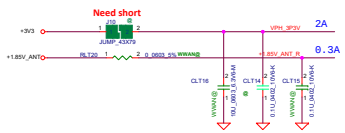


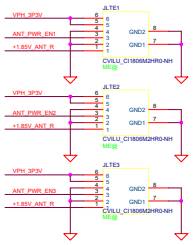


ÐèÒªÖØÐÂμ÷ÓÃ4.8mm Conn £¨SP07001D40D£©









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