MODEL NAME : *QBLB0*

PCB NO : *LA-8381P*

BOM P/N : *4319H631L01 (Samsung 1G)*
4319H631L02(Samsung 2G)
4319H631L03(Hynix 1G)
4319H631L04(Hynix 2G)

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Schematic Document

Specter MLK (Chief River)

Ivy Bridge(PGA) + Panther Point(standard)

DISCRETE VGA N13P-GT (optimus)

2011-10-26

Rev: X01

Highlight the short pad for 0 ohm

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Title: *Cover Page*

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 Sheet 1 of 63

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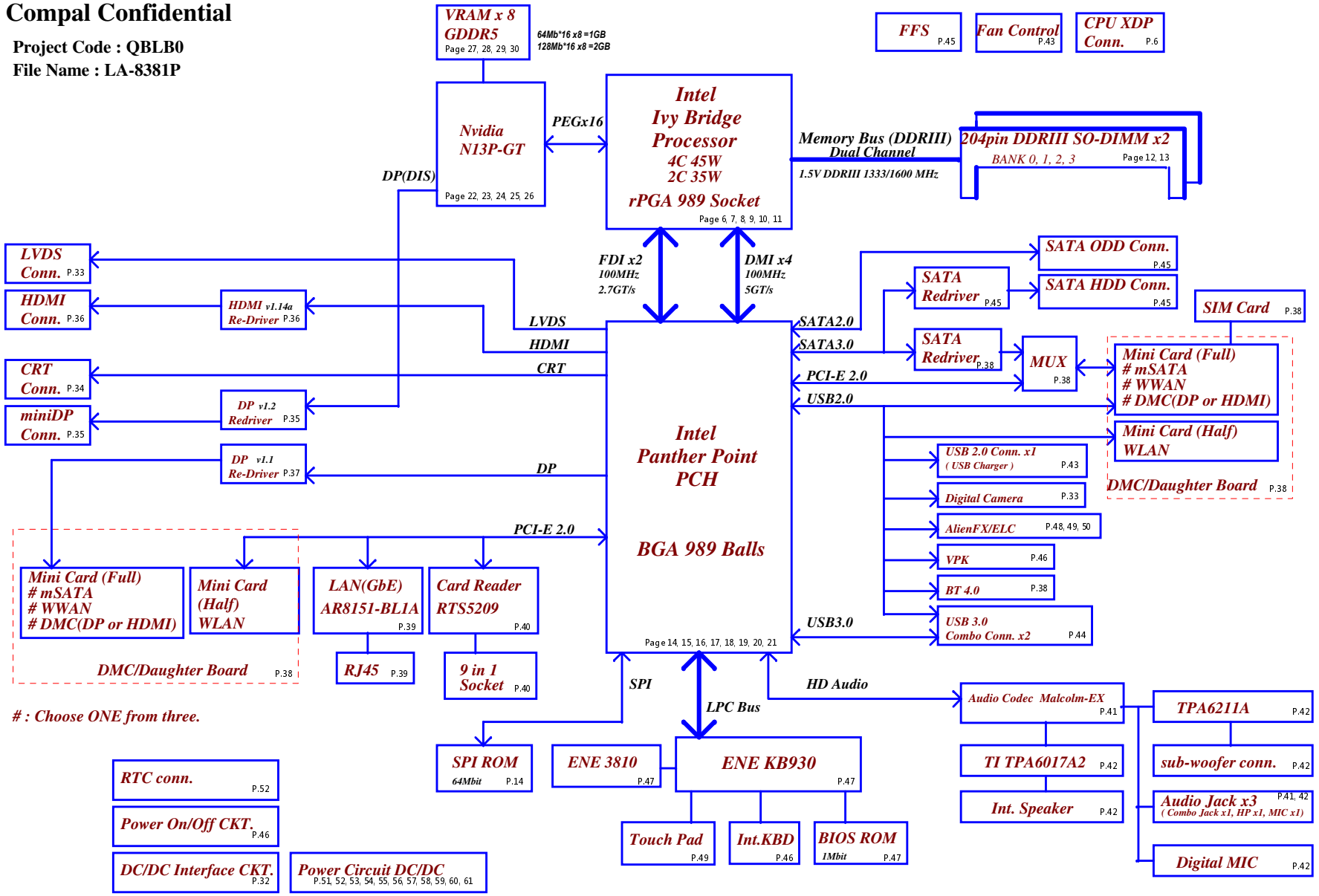
Project Code : QBLB0
File Name : LA-8381P



Security Classification	Compal Secret Data		
Issued Date	2011/02/23	Deciphered Date	2012/02/23

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Title: **Block Diagram**

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 2 of 63

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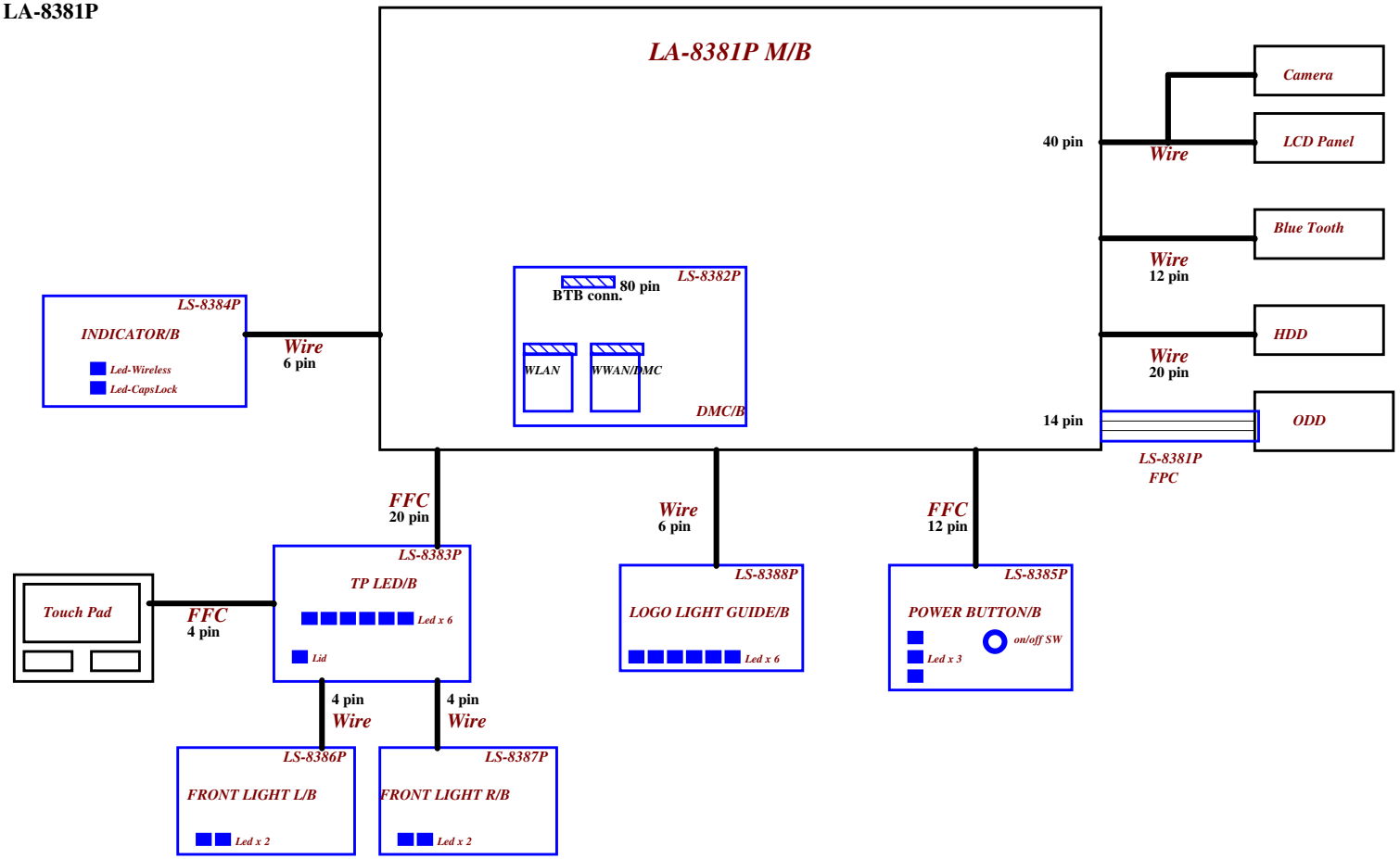
Project Code : QBLB0
File Name : LA-8381P



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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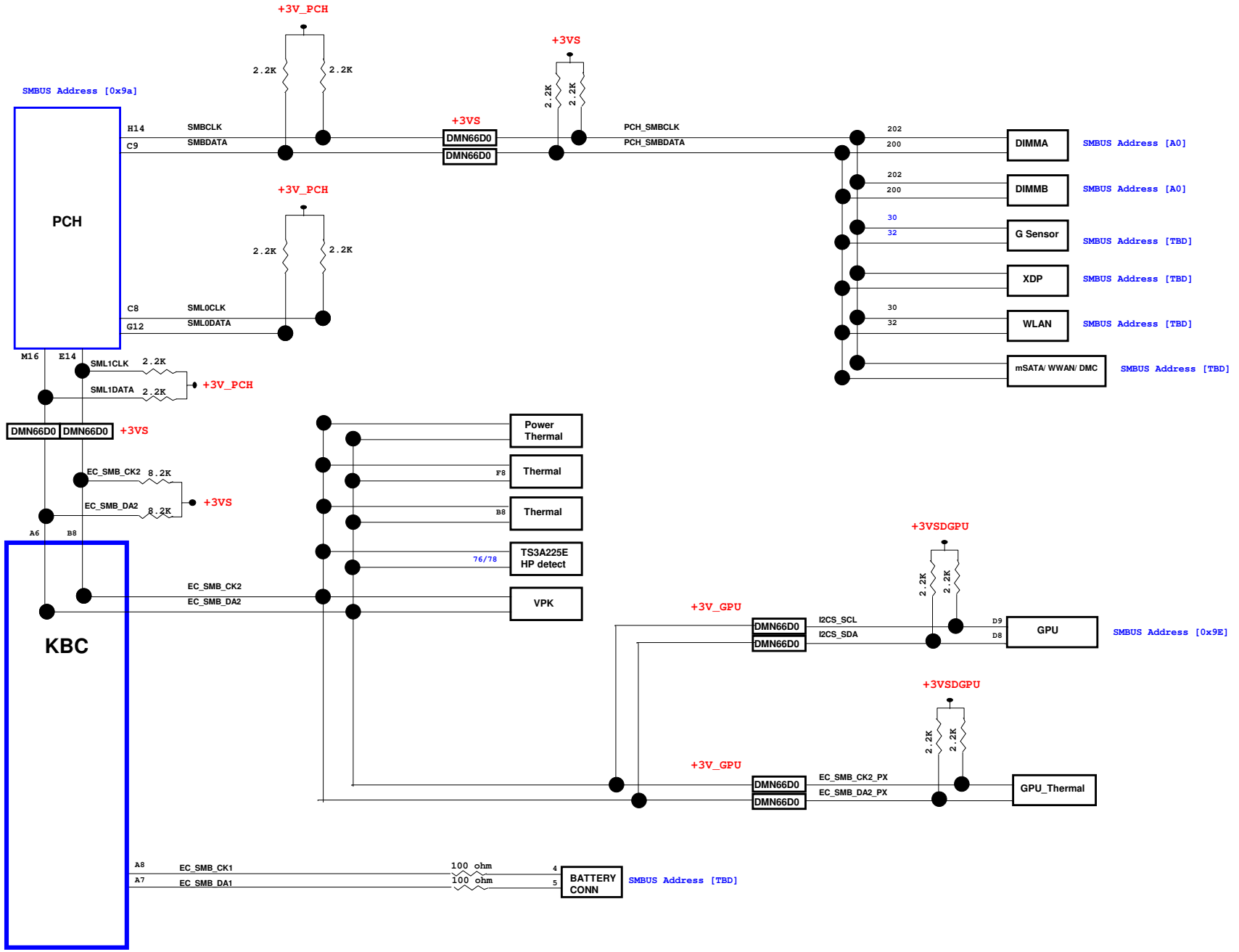
Title: **Block Diagram**

Size	Document Number	Rev
		1.0

Date: Thursday, January 12, 2012 | Sheet 3 of 63



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Title: **Block Diagram**

Size	Document Number	Rev
		1.0

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Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID Table for AD channel

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	Board ID	PCB Revision
0	0	0 V	0 V	0.155 V	0x00-0x0C	0	
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C	1	
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30	2	
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49	3	
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69	4	SSI_X00
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E	5	PT_X01
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB	6	ST_X02
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF	7	QT_A00

BOARD ID Table

SMBUS Control Table

	SOURCE	MINI1 (WLAN)	MINI2 (DMC)	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	XDP	Charger	HP detect
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V	V		V	V
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V			V		

Link

PCH	USB PORT#	DESTINATION
	0	JUSB2 (v3.0 Ext Right Side)
	1	JUSB3 (v3.0 Ext Right side)
	2	None
	3	None
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN/DMC)
	6	ELC 8051
	7	None
	8	Bluetooth
	9	JUSB1 (2.0 Ext Left Side)
	10	None
	11	None
	12	CAMERA
	13	VPK

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State \ power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.5V_CPU_VDDQ +VCCP = +1.05VS +VCC_CORE +VCC_GFXCORE_AXG +VCCSA +0.75VS +3VSDGPU +1.5VSDGPU +VGA_CORE
S0			
S3	ON	ON	ON
	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	10/100/1G LAN
	CLKOUT_PCIE2	MINI CARD-2 WWAN
	CLKOUT_PCIE3	MINI CARD-1 WLAN
	CLKOUT_PCIE4	CARD READER
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

FLEX CLOCKS	DESTINATION
CLKOUTFLEX0	None
CLKOUTFLEX1	None
CLKOUTFLEX2	None
CLKOUTFLEX3	None

Symbol Note :

: means Digital Ground

: means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	m-SATA
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

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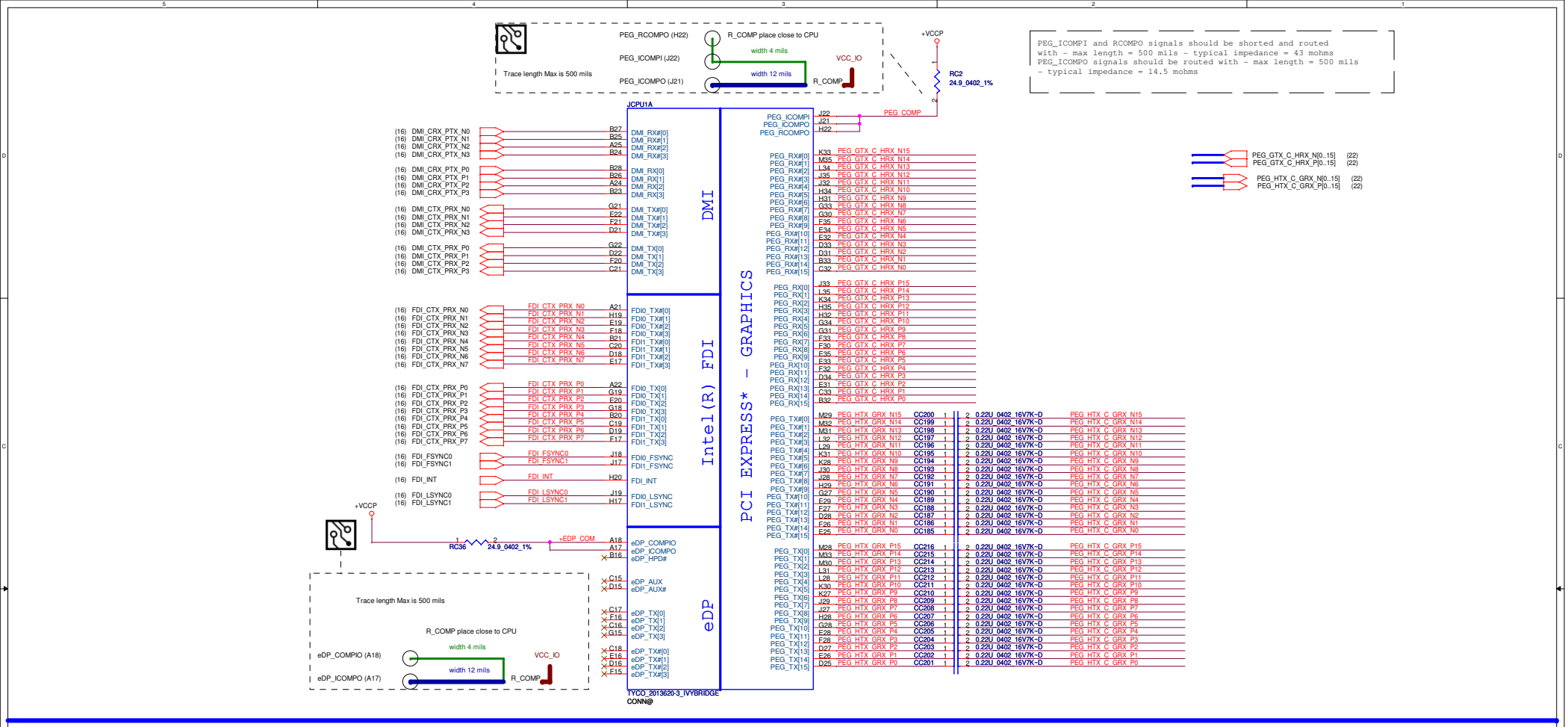
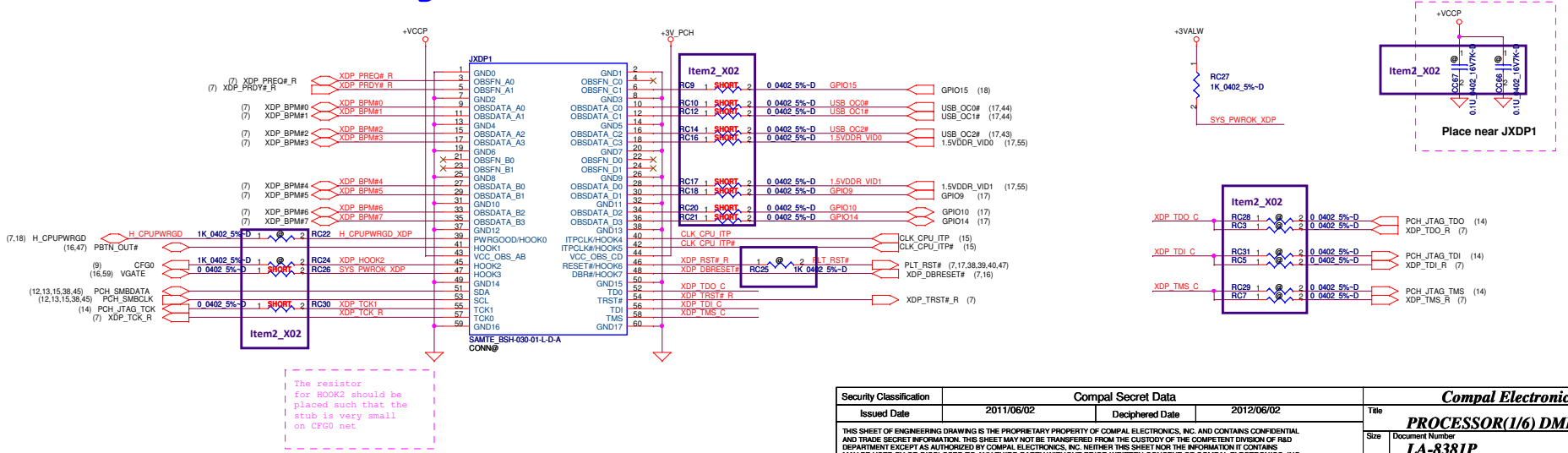
Title: Notes List
Size: Document Number: LA-8381P Rev: 1.0
Date: Thursday, January 12, 2012 Sheet 5 of 63



XDP Connector (Merged CPU-PCH)



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Compal Electronics, Inc.

Title: **PROCESSOR(1/6) DMI,FDI,PEG**

Size	Document Number	Rev
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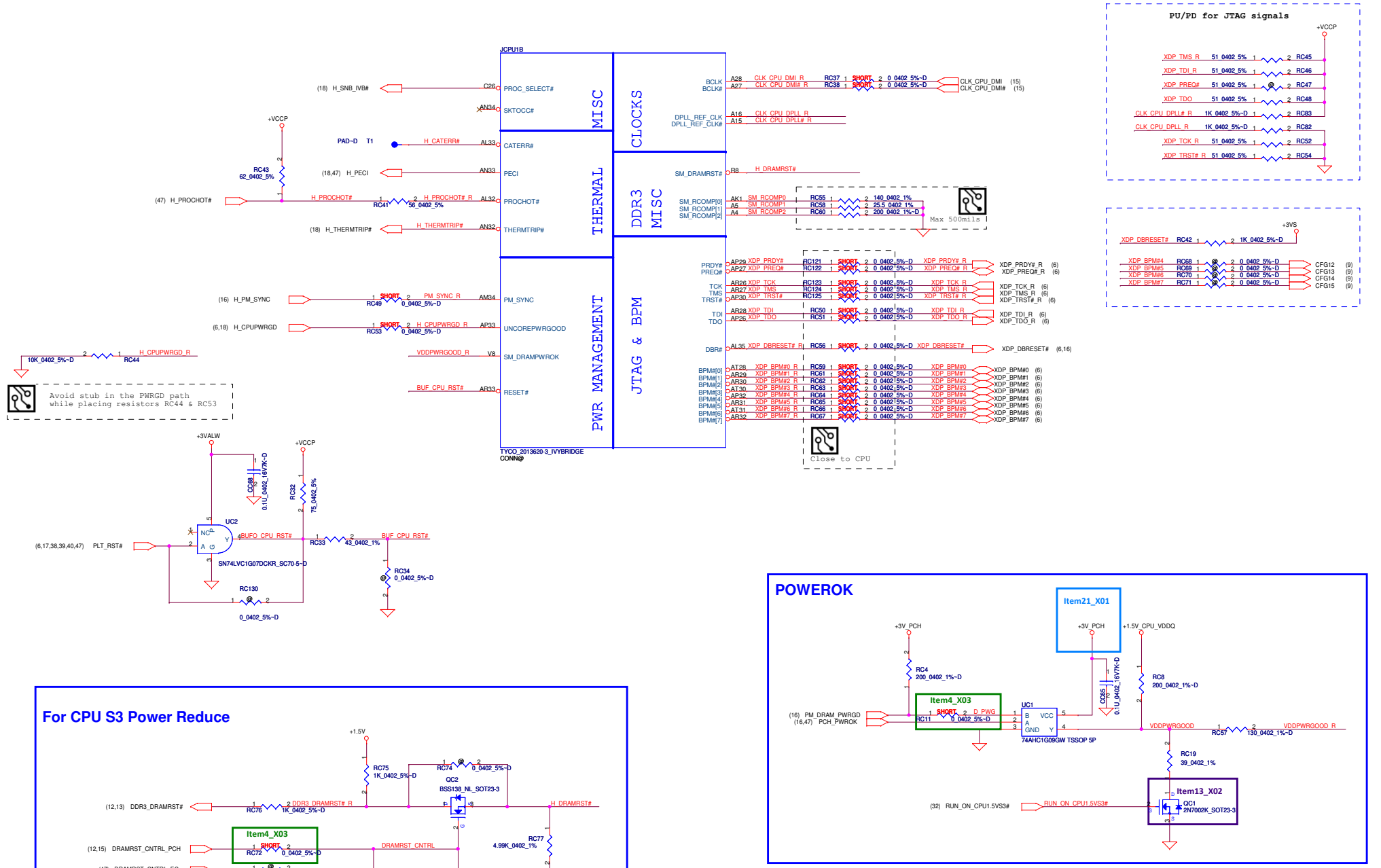
PM, XDP, CLK, S3 Reduce, PLTRST



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PROCESSOR(2/6) PM,XDP,CLK

Size	Document Number	Rev
	LA-8381P	1.0

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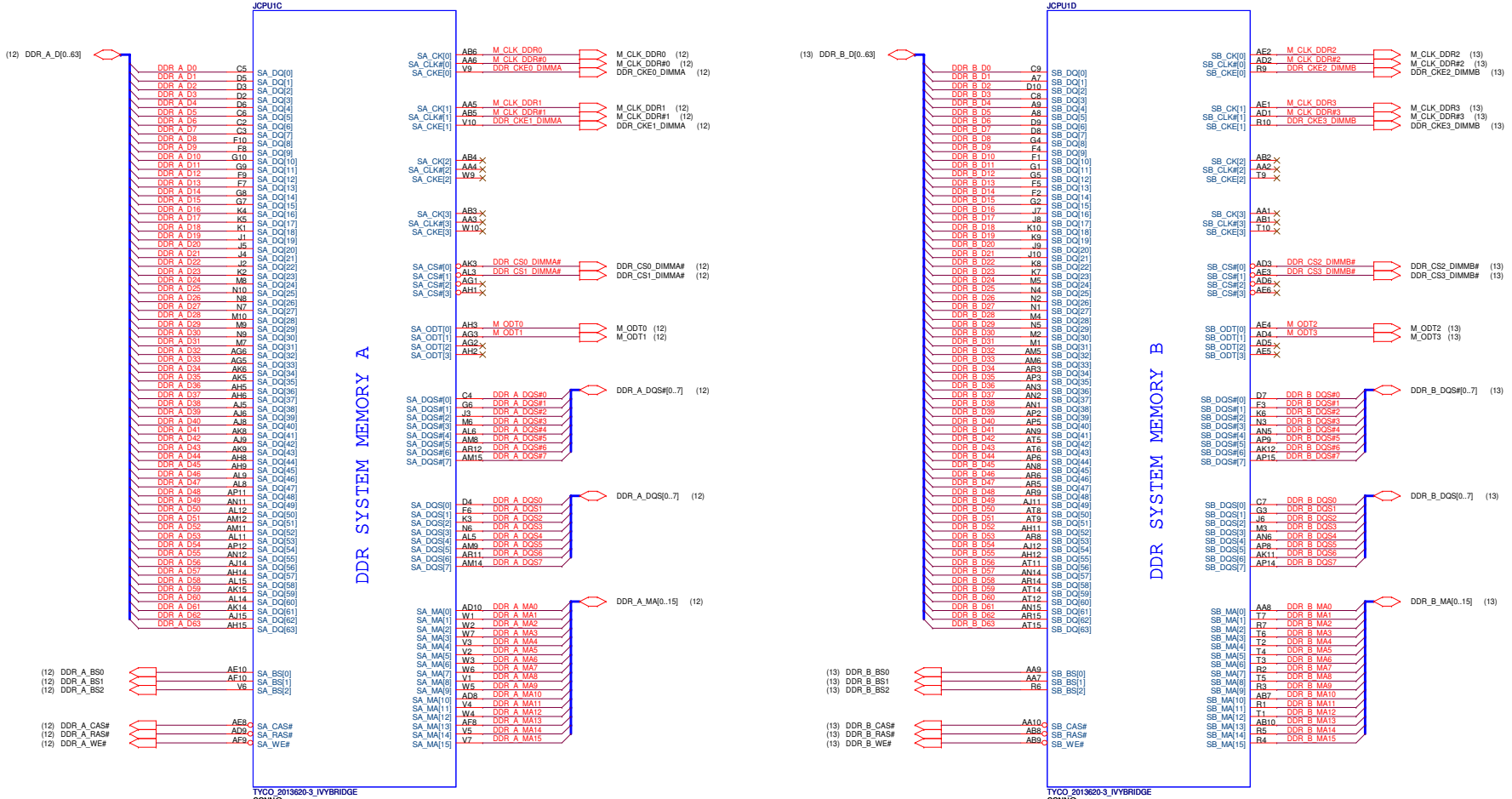

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PROCESSOR(3/6) DDRIII**

Size	Document Number	Rev
	LA-8381P	1.0

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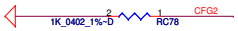
CFG Straps for Processor

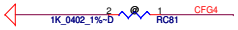


PEG Static Lane Reversal - CFG2 is for the 16x

CFG2

1:(Default) Normal Operation; Lane # definition matches socket pin map definition

* 0:Lane Reversed

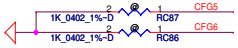


Display Port Presence Strap

CFG4

* 1 :Disabled; No Physical Display Port attached to Embedded Display Port

0 :Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps

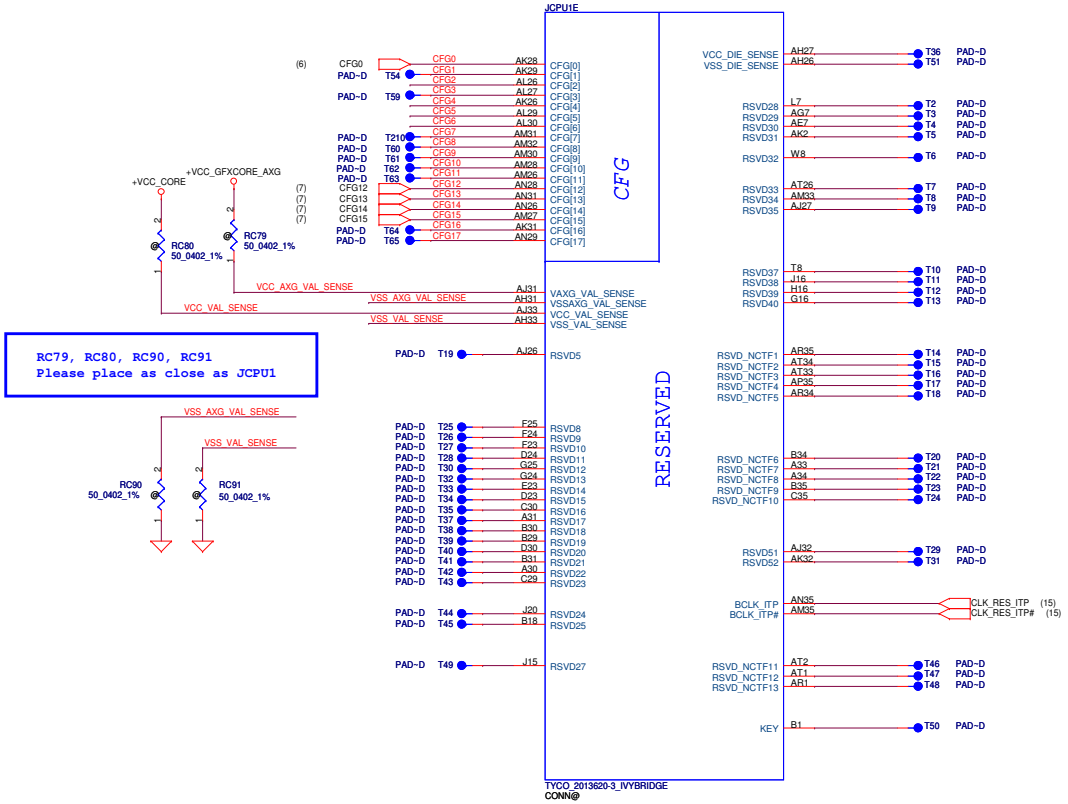
CFG[6:5]

*11:(Default) x16 - Device 1 functions 1 and 2 disabled

10:x8, 8 - Device 1 function 1 enabled ;function 2 disabled

01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Security Classification	Compal Secret Data		
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Title: PROCESSOR(4/6) RSVD,CFG

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POWER

JCPU1F

QC=94A
DC=53A

+VCC_CORE

CORE SUPPLY

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

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PEG AND DDR

+VCCP

8.5A

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 V10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12

VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11

VCCIO40 J23

+VCCSA

Socket Cavity Socket Edge

CC167 10U_0805_25V6K-D
CC168 10U_0805_25V6K-D
CC169 10U_0805_25V6K-D
CC170 10U_0805_25V6K-D
CC171 330U_D2_2VM_R6M-D

+1.8VS

Item4_X03

RC109 1 SHORT 2 0_0805_5%~D

+1.8VS_VCCPLL

Socket Edge

CC172 10U_0805_25V6K-D
CC174 1U_0402_6.3V6K-D
CC175 1U_0402_6.3V6K-D
CC176 330U_D2_2.5VM_R6M-D

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

+VCCP

Item3_X02

RC93 1 2 75_0402_5%
RC94 1 2 43_0402_1%
RC92 1 SHORT 2 0_0402_5%~D
RC96 1 SHORT 2 0_0402_5%~D
RC95 1 2 130_0402_1%~D

VR_SVID_ALRT# (59)
VR_SVID_CLK (59)
VR_SVID_DAT (59)
+VCCP

RC95 close to CPU

VIDALERT#
Connect one end of series-resistor 43±5% close to processor and pull-up to VCCIO through 75±5% on the other end of the series-resistor towards Intel MVP 7.

VIDSOUT:
Requires a pull-up to VCCIO through a pull-up resistor of 130 ±5% close to the processor, and a pull-up to VCCIO through a pull-up resistor of 130 ±5% close to Intel MVP 7.
VIDSCLK:
Required pull-up to VCCIO through 55 ±5% close to Intel IMVP 7.

18-mil witdh,and shoulde use differential routing with 7-milseparation. Signals must have equal trace length within 25 mils and are to be routed using external layer and GND referencing (no split plane referencing). VSS_SENSE, VCC_SENSE are to use 25-mils separation from any other signal or rail.

VCC_SENSE & VSS_SENSE:
xxxxxx
100- ±1% pull-down to GND near processor

SENSE LINES

+VCC_CORE

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

RC97 1 2 100_0402_1%~D
RC98 1 SHORT 2 0_0402_5%~D
RC99 1 SHORT 2 0_0402_5%~D
RC100 1 2 100_0402_1%~D

VCCSENSE (59)
VSSSENSE (59)

+VCCP

RC126 1 2 10_0402_1%~D

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10

RC129 1 2 10_0402_1%~D

VCCIO_SENSE (56)
VSSIO_SENSE (56)

Item3_X02

+1.5V

+1.5V_CPU_VDDQ

@ J8
PAD-OPEN 4x4m
J8 OPEN

Socket Edge

CC160 10U_0805_25V6K-D
CC161 10U_0805_25V6K-D
CC162 10U_0805_25V6K-D
CC163 10U_0805_25V6K-D
CC164 10U_0805_25V6K-D
CC165 10U_0805_25V6K-D
CC166 330U_D2_2VM_R6M~D

18-mil witdh,and shoulde use differential routing with 7-milseparation. Signals must have equal trace length within 25 mils and are to be routed using external layer and GND referencing (no split plane referencing). VSS_SENSE, VCC_SENSE are to use 25-mils separation from any other signal or rail.

+0.75VS

+V_SM_VREF

RC106 1 SHORT 2 0_0402_5%~D

Item3_X02

CC250 0.1U_0402_10V7K~D

1K_0402_5%~D RC112
1K_0402_5%~D RC116

+VCC_GFXCORE_AXG

VCC_AXG_SENSE RC131 1 2 100_0402_5%~D
VSS_AXG_SENSE RC132 1 2 100_0402_5%~D

POWER

+VCC_GFXCORE_AXG

JCPU1G

33A

VAXG1 AT24
VAXG2 AT23
VAXG3 AT21
VAXG4 AT20
VAXG5 AT18
VAXG6 AT17
VAXG7 AR24
VAXG8 AR23
VAXG9 AR21
VAXG10 AR20
VAXG11 AR18
VAXG12 AR17
VAXG13 AP24
VAXG14 AP23
VAXG15 AP21
VAXG16 AP20
VAXG17 AP18
VAXG18 AP17
VAXG19 AN24
VAXG20 AN23
VAXG21 AN21
VAXG22 AN20
VAXG23 AN18
VAXG24 AN17
VAXG25 AM24
VAXG26 AM23
VAXG27 AM21
VAXG28 AM20
VAXG29 AM18
VAXG30 AM17
VAXG31 AL24
VAXG32 AL23
VAXG33 AL21
VAXG34 AL20
VAXG35 AK24
VAXG36 AK23
VAXG37 AK21
VAXG38 AK20
VAXG39 AJ24
VAXG40 AJ23
VAXG41 AJ21
VAXG42 AJ20
VAXG43 AH24
VAXG44 AH23
VAXG45 AH21
VAXG46 AH20
VAXG47 AH18
VAXG48 AH17
VAXG49 AG24
VAXG50 AG23
VAXG51 AG21
VAXG52 AG20
VAXG53 AG18
VAXG54 AG17

GRAPHICS VAXG RAILS

SENSE LINES

VAXG_SENSE AK35 VCC_AXG_SENSE
VSSAXG_SENSE AK34 VSS_AXG_SENSE

VCC_AXG_SENSE (59)
VSS_AXG_SENSE (59)

+V_SM_VREF should have 10 mil trace width

VREF

SM_VREF AL1 +V_SM_VREF

SA_DIMM_VREFDQ B4 +V_DDR_REFA_R
SB_DIMM_VREFDQ D1 +V_DDR_REFB_R

+V_DDR_REFA_R (12)
+V_DDR_REFB_R (12)

10mil .Spacing is 10mil

DDR3 -1.5V RAILS

+1.5V_CPU_VDDQ

5A

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

+1.5V_CPU_VDDQ

CC182 2 1 0.1U_0402_10V7K~D
CC184 2 1 0.1U_0402_10V7K~D
CC181 2 1 0.1U_0402_10V7K~D
CC183 2 1 0.1U_0402_10V7K~D

+1.5V

SA RAIL

6A

+VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

VCCSA_SEL Voltage Selection Table

VID[0] Pin AE10	VID[1] Pin AG10	VCCSA Vout
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

1.8V RAIL

1.2A

+1.8VS_VCCPLL

TBD

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

MISC

VCCSA_SENSE H23 VCCSA_SENSE (57)

VCCSA_VID[0] C22 VCCSA_VID0
VCCSA_VID[1] C24 VCCSA_VID1

RC111 1 SHORT 2 0_0402_5%~D
RC108 1 SHORT 2 0_0402_5%~D

H_VCCSA_VID0 (57)
H_VCCSA_VID1 (57)

10mil .Spacing is 10mil

VCCIO_SEL A19 H_VCCP_SEL

RC88 1 SHORT 2 0_0402_5%~D

VCCP_PWRCTRL (56)

Item3_X02

Need PWR add new circuit on 1.05V(refer CRB)

TYCO_2013620-3_IVYBRIDGE
CONN@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

Size	Document Number	Rev
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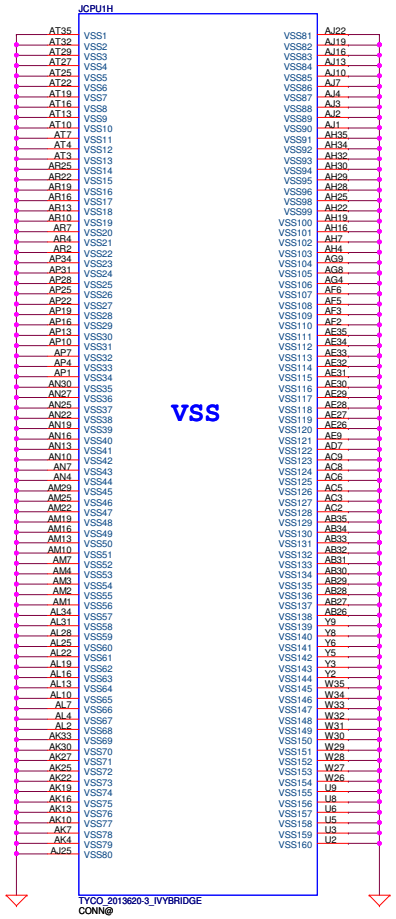

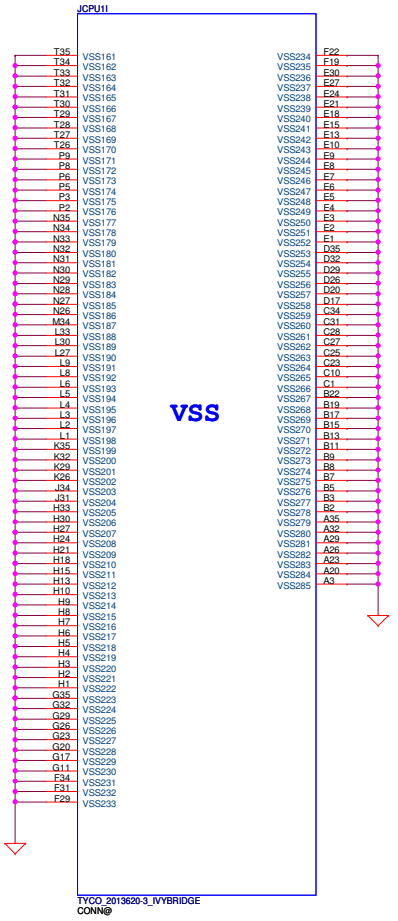

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PROCESSOR(6/6) PWR,VSS**

Size	Document Number	Rev
	LA-8381P	1.0

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(8) DDR_A_DQS#[0..7]
(8) DDR_A_DQS[0..7]
(8) DDR_A_D[0..63]
(8) DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

All VREF traces should have 10 mil trace width

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

JDIMM1
FOX_AS0A626-U2SN-7F
CONN@

M1
Item3 X02

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 12 of 63

(8) DDR_B_DQS#[0..7]
(8) DDR_B_DQS[0..7]
(8) DDR_B_D[0..63]
(8) DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

+V_DDR_REFB
+1.5V
JDIMM2

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

All VREF traces should have 10 mil trace width

DDR3_DRAMRST# (7,12)
DDR_CKE3_DIMMB (8)
M_CLK_DDR3 (8)
M_CLK_DDR#3 (8)
DDR_B_BS1 (8)
DDR_B_RAS# (8)
DDR_CS2_DIMMB# (8)
M_ODT2 (8)
M_ODT3 (8)
PCH_SMBDATA (6,12,15,38,45)
PCH_SMBCLK (6,12,15,38,45)

CONN@

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Layout Note:
Place near JDIMMB

Layout Note:
Place near JDIMMB.203,204

M1

RD11 SHORT 0_0402_5%~D
Item3_X02

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
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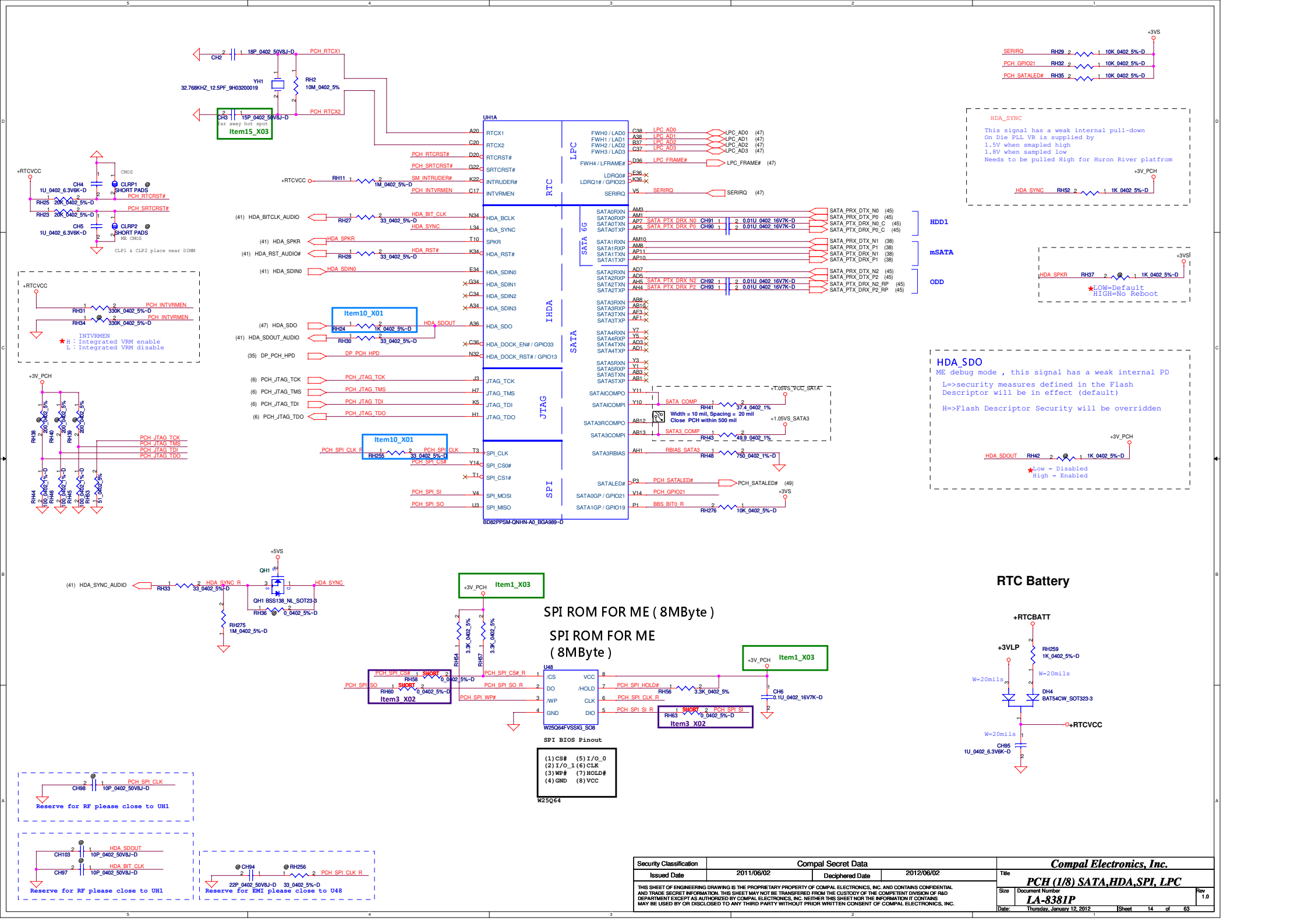
Date: Thursday, January 12, 2012 | Sheet 13 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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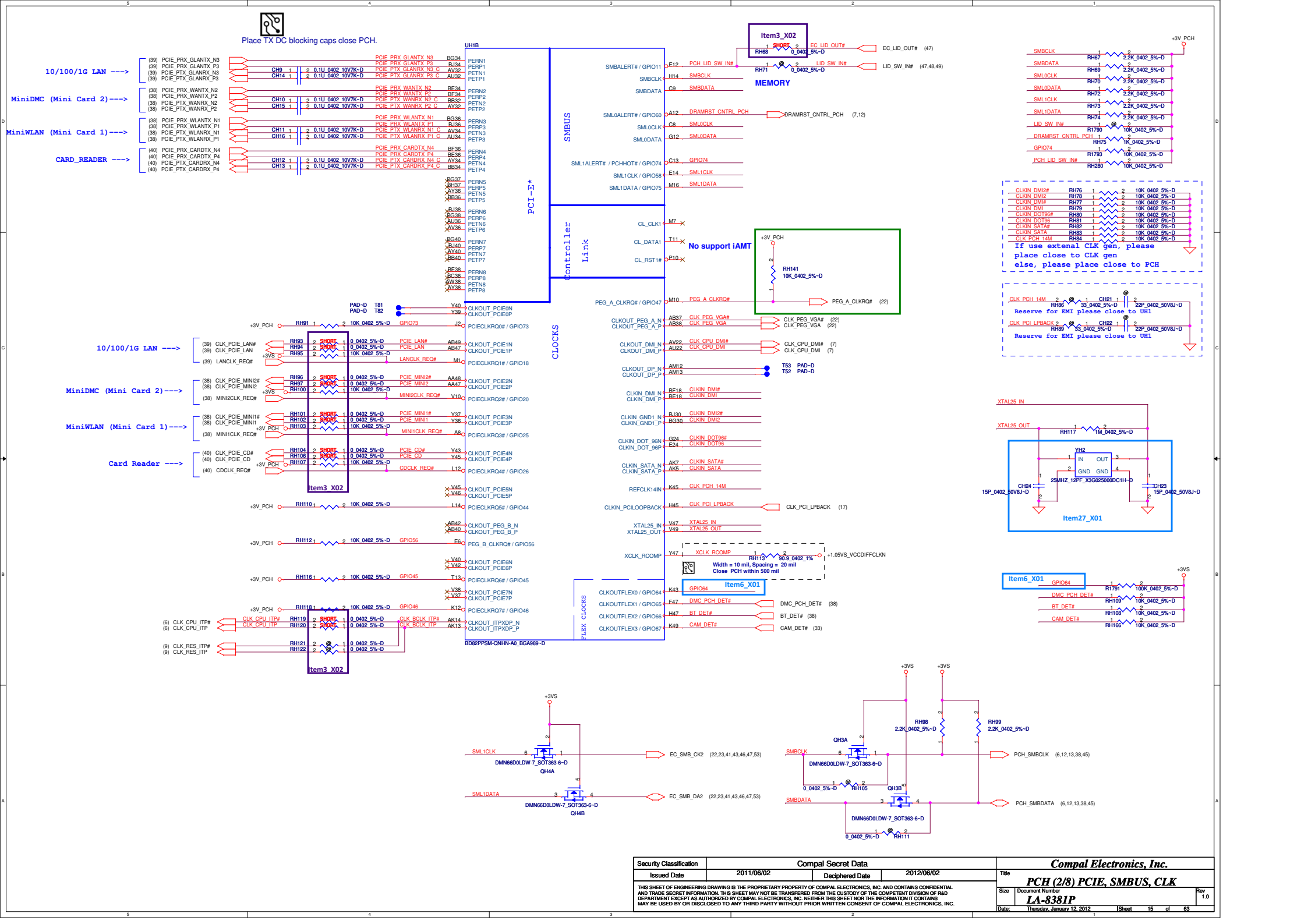
Compal Electronics, Inc.

Title: **PCH (1/8) SATA,HDA,SPI, LPC**

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 14 of 63



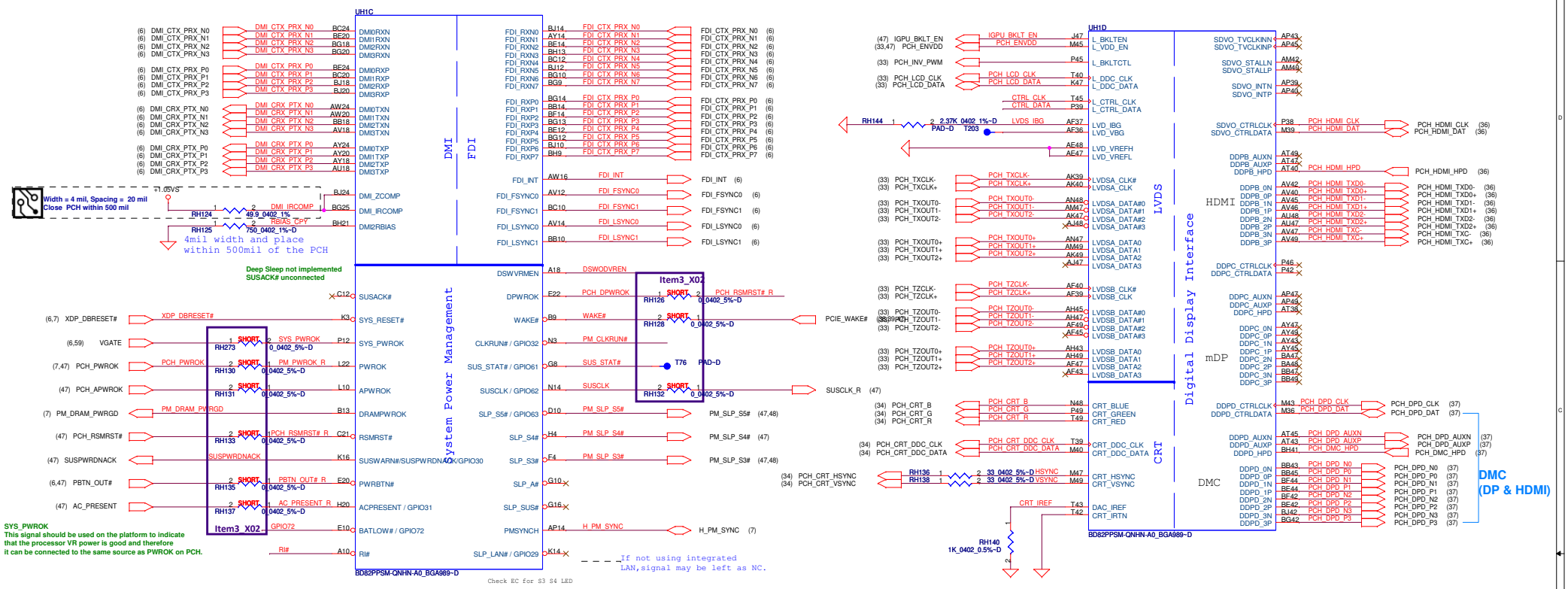
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 15 of 63



APWROK
This is a input signal to the PCH from power monitoring circuit to indicate that all Active Sleep Well (ASW) rails, i.e. Intel ME sub-system and LAN power rails are stable on the platform. Connect to ASW power rail monitoring circuit on motherboard. For platform not supporting Intel AMT it can be connected to PWROK. The ASW power must be stable for at least 1ms before platform logic asserts APWROK.

DPWROK
This is an input signal to the PCH from platform power monitoring logic to indicate that all power rails associated with the PCH Deep Sx well (DSW) are valid and stable. Connect to VccDSW3_3 power rail monitoring circuit on mother board for platforms that support Deep Sx state. This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state. The DSW rails must be stable for at least 10ms before DPWROK is asserted to PCH.

CRT_HSYNC and CRT_VSYNC resistor
33 ohm for Direct Connect
20 ohm for Dock Support
20 ohm for Switchable Graphics Device Down Topology
10 ohm for Switchable Graphics Dock Support

Put close PCH 500 mil

Reserve for RF please close to UH1

DSWODVREN - On Die DSW VR Enable
H : Enable
L : Disable

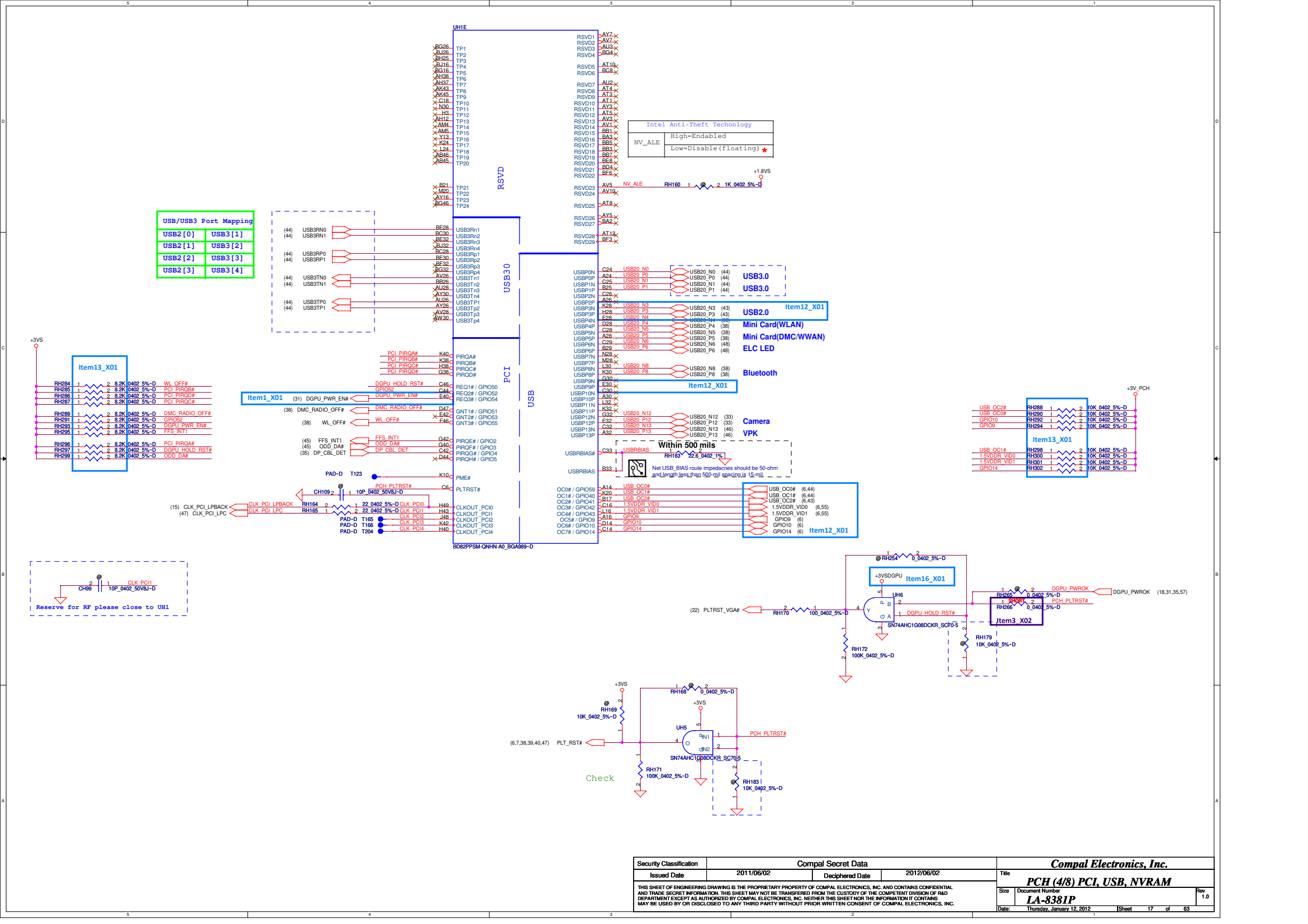
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 16 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

Size	Document Number	Rev
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Date: Thursday, January 12, 2012 | Sheet 17 of 63

High: CRT Plugged

+3VS
RH198 10K_0402_5%~D
CRT_DET
(34) CRT_DET#
QH5 2N7002K_SOT23-3
Item13_X02

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
+3V_PCH
PCH_GPIO28
RH229 8.2K_0402_5%~D
RH177 @ 1K_0402_5%~D

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)
+3VS
RH181 @ 1K_0402_5%~D PCH_GPIO37
RH182 10K_0402_5%~D PCH_GPIO37

UH1F

	CRT_DET	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40	ODD_EN#	ODD_EN# (45)
		A42	TACH1 / GPIO1	TACH5 / GPIO69	B41	GPIO69	T126 PAD~D
	GPIO6	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41		
(47)	EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40		
(47)	EC_SMI#	C10	GPIO8				
(38)	BT_RADIO_DIS#	C4	LAN_PHY_PWR_CTRL / GPIO12				
(6)	GPIO15	G2	GPIO15	A20GATE	P4	GATEA20	GATEA20 (47)
	GPIO16	U2	SATA4GP / GPIO16	PECI	AU16	PCH_PECI_R 1 @ 2 0_0402_5%~D RH175	H_PECI (7,47)
(17,31,35,57)	DGPU_PWROK	D40	TACH0 / GPIO17	RCIN#	P5	KB_RST#	KB_RST# (47)
	PCH_GPIO22	T5	SCLOCK / GPIO22	PROCPWRGD	AY11		H_CPUPWRGD (6,7)
		E8	GPIO24	THRMTRIP#	AY10	H_THERMTRIP#_C 1 2 390_0402_5% RH176	H_THERMTRIP# (7)
		E16	GPIO27	INIT3_3V#	T14	INIT3_3V# T127 PAD~D	
	PCH_GPIO28	P8	GPIO28	DF_TVS	AY1	NV_CLE	
(38)	BT_ON#	K1	STP_PCI# / GPIO34	TS_VSS1	AH8		
	GPIO35	K4	GPIO35	TS_VSS2	AK11		
(45)	ODD_DETECT#	V8	SATA2GP / GPIO36	TS_VSS3	AH10		
	PCH_GPIO37	M5	SATA3GP / GPIO37	TS_VSS4	AK10		
	DGPU_PRSNT#	N2	SLOAD / GPIO38	NC_1	P37		
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39				
(45)	FFS_INT2	V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2		
	GPIO49	V3	SATA5GP / GPIO49 / TEMP_ALERT#	VSS_NCTF_16	BG48		
(45)	HDD_DETECT#	D6	GPIO57	VSS_NCTF_17	BH3		
				VSS_NCTF_18	BH47		
		A4	VSS_NCTF_1	VSS_NCTF_19	BJ4		
		A44	VSS_NCTF_2	VSS_NCTF_20	BJ44		
		A45	VSS_NCTF_3	VSS_NCTF_21	BJ45		
		A46	VSS_NCTF_4	VSS_NCTF_22	BJ46		
		A5	VSS_NCTF_5	VSS_NCTF_23	BJ5		
		A6	VSS_NCTF_6	VSS_NCTF_24	BJ6		
		B3	VSS_NCTF_7	VSS_NCTF_25	C2		
		B47	VSS_NCTF_8	VSS_NCTF_26	C48		
		BD1	VSS_NCTF_9	VSS_NCTF_27	D1		
		BD49	VSS_NCTF_10	VSS_NCTF_28	D49		
		BE1	VSS_NCTF_11	VSS_NCTF_29	E1		
		BE49	VSS_NCTF_12	VSS_NCTF_30	E49		
		BF1	VSS_NCTF_13	VSS_NCTF_31	F1		
		BF49	VSS_NCTF_14	VSS_NCTF_32	F49		

GPIO
CPU/MISC
NCTF
BD82PPSM-QNHN-A0_BGA989~D

INIT3_3V
This signal has weak internal PU, can't pull low

DMI Termination Voltage

NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS
Weak internal PU,Do not pull low
RH161 2.2K_0402_5%~D
NV_CLE 1K_0402_5%~D RH162 H_SNB_IVB# (7)
CLOSE TO THE BRANCHING POINT
RH161 and RH162 Follow CRB FAB2 setting

+3V_PCH
HDD_DETECT# RH188 10K_0402_5%~D
EC_SMI# RH190 10K_0402_5%~D
BT_RADIO_DIS# RH279 10K_0402_5%~D
GPIO15 RH281 1K_0402_5%~D

+3VS
ODD_EN# RH187 10K_0402_5%~D
CRT_DET# RH192 @ 10K_0402_5%~D
ODD_DETECT# RH193 200K_0402_5%
GPIO16 RH274 10K_0402_5%~D
BT_ON# RH195 8.2K_0402_5%~D
KB_RST# RH196 10K_0402_5%~D
PCH_GPIO22 RH197 10K_0402_5%~D
GPIO35 RH257 @ 10K_0402_5%~D
GPIO49 RH258 10K_0402_5%~D
PCH_GPIO39 RH263 10K_0402_5%~D
GPIO6 RH271 10K_0402_5%~D
GATEA20 RH174 10K_0402_5%~D
EC_SCI# RH283 10K_0402_5%~D

For BIOS setting dGPU present
★ LOW - dGPU exist
+3VS
DGPU_PRSNT# RH262 @ 10K_0402_5%~D
DGPU_PRSNT# RH282 10K_0402_5%~D

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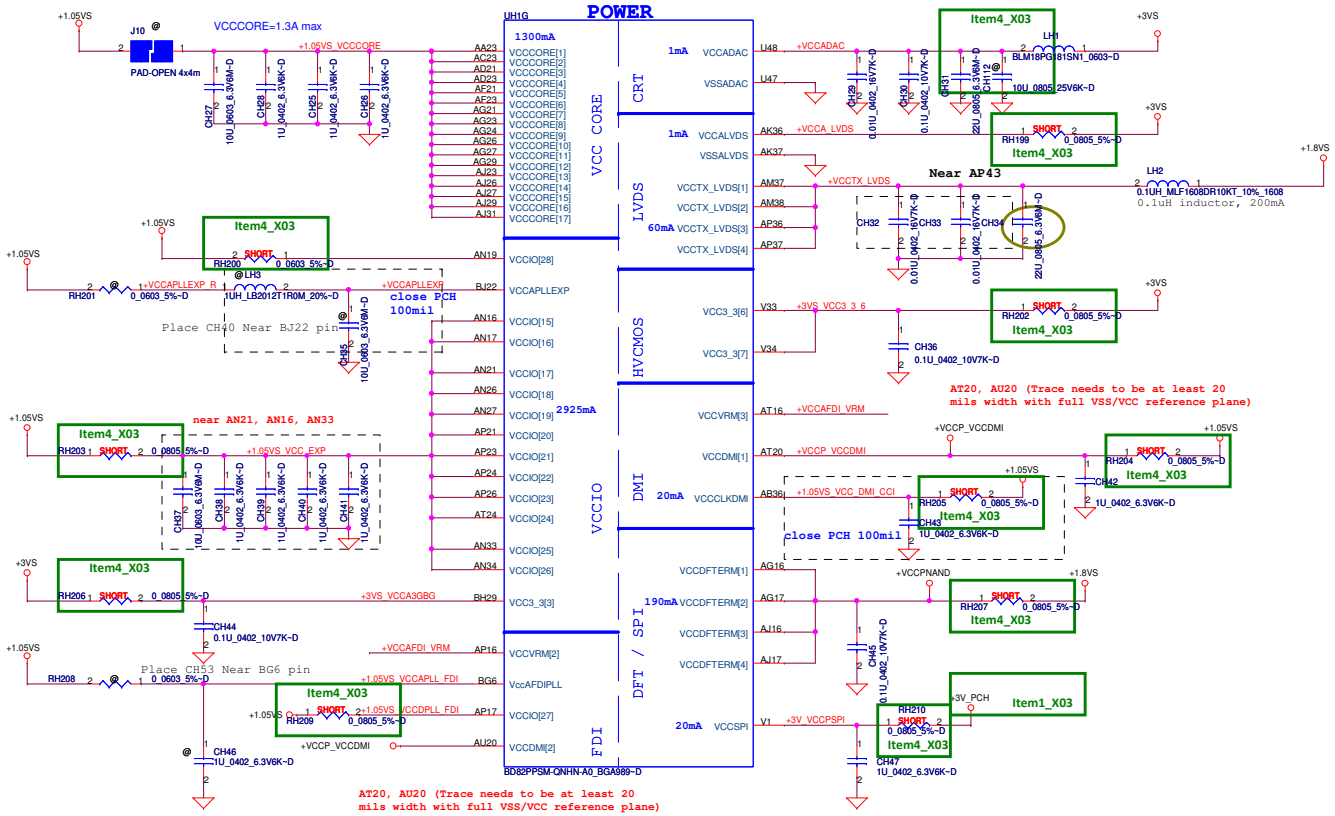
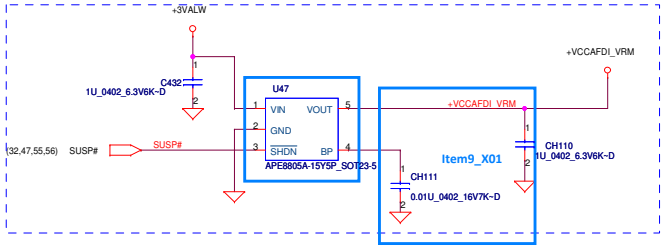
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.
Title: PCH (5/8) GPIO, CPU, MISC
Size: | Document Number: LA-8381P | Rev: 1.0
Date: Thursday, January 12, 2012 | Sheet 18 of 63

check power resistor package



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



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Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size | Document Number: LA-8381P | Rev: 1.0

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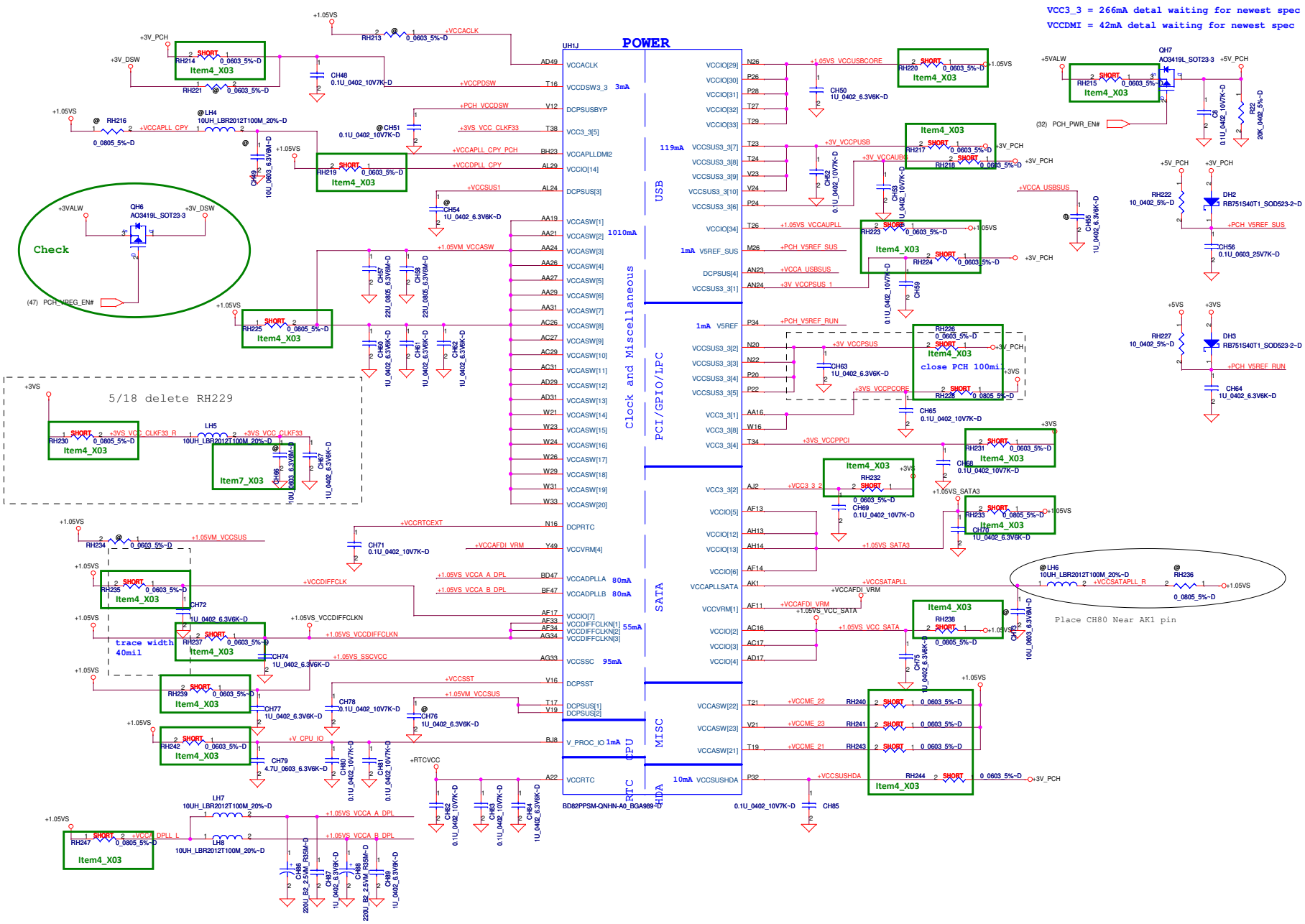


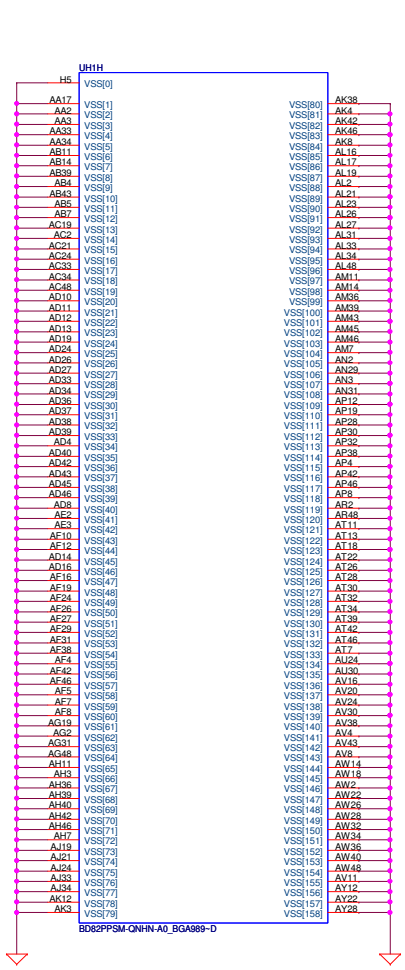
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

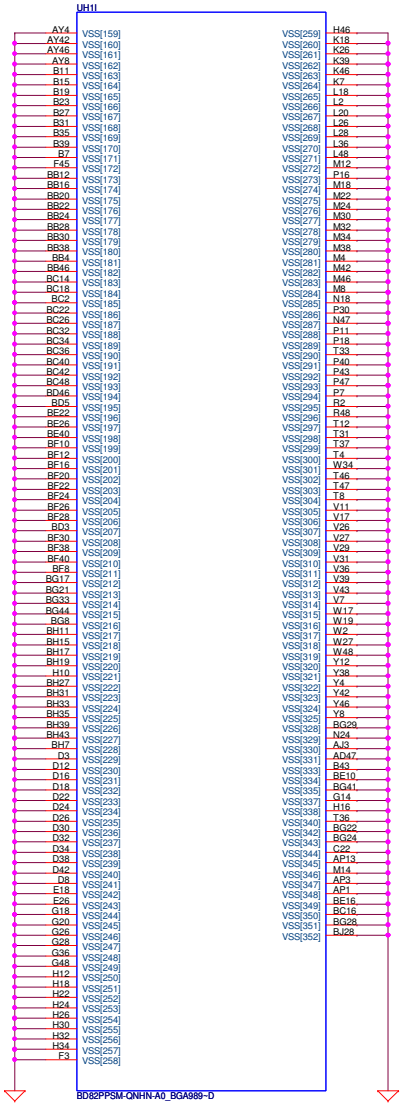
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size	Document Number	Rev
	LA-8381P	1.0

Date: Thursday, January 12, 2012 | Sheet 20 of 63





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Title: **PCH (8/8) VSS**

Size	Document Number	Rev
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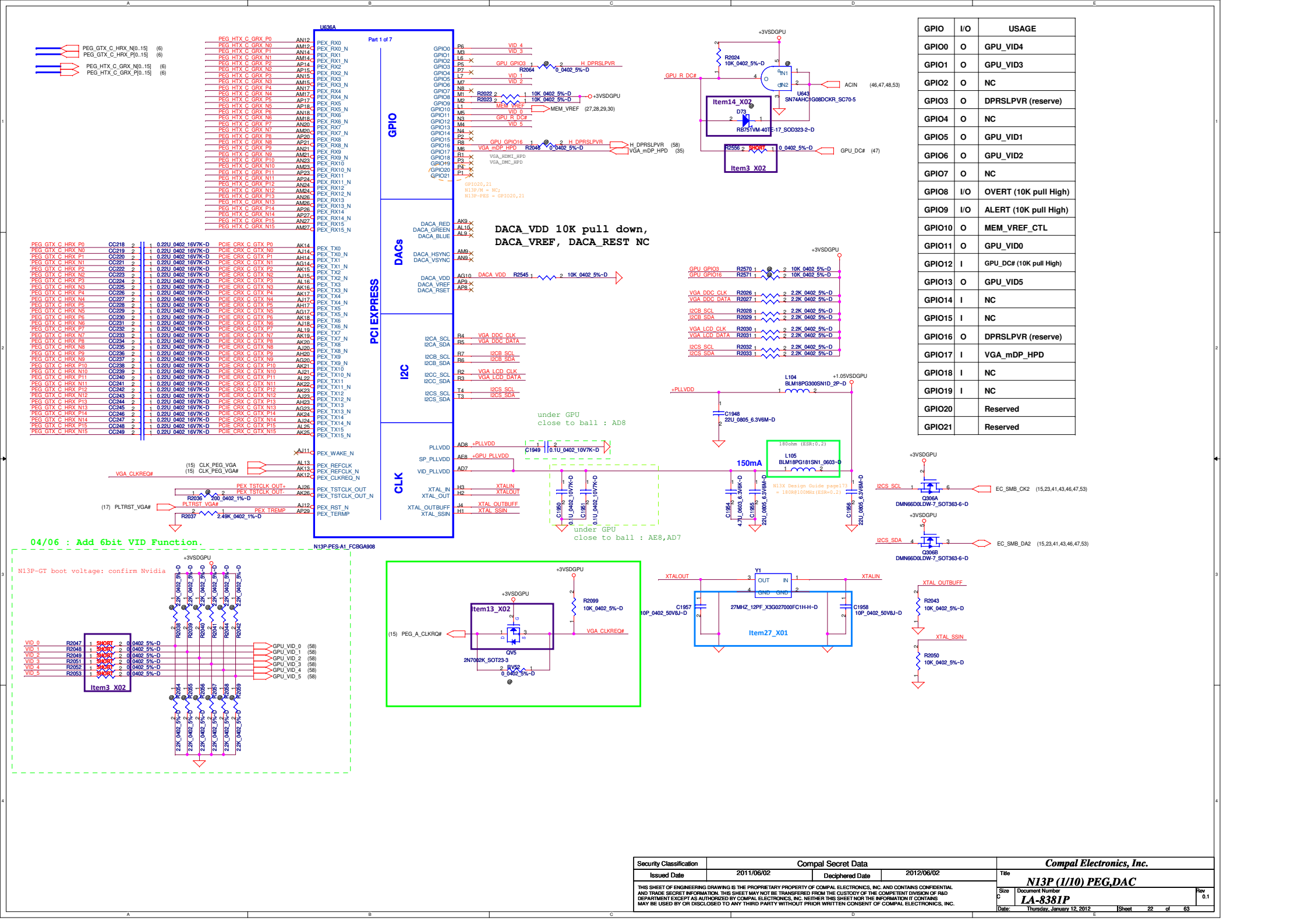

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	NC
GPIO3	O	DPRSLPVR (reserve)
GPIO4	O	NC
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	NC
GPIO8	I/O	OVERT (10K pull High)
GPIO9	I/O	ALERT (10K pull High)
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	GPU_DC# (10K pull High)
GPIO13	O	GPU_VID5
GPIO14	I	NC
GPIO15	I	NC
GPIO16	O	DPRSLPVR (reserve)
GPIO17	I	VGA_mDP_HPD
GPIO18	I	NC
GPIO19	I	NC
GPIO20		Reserved
GPIO21		Reserved

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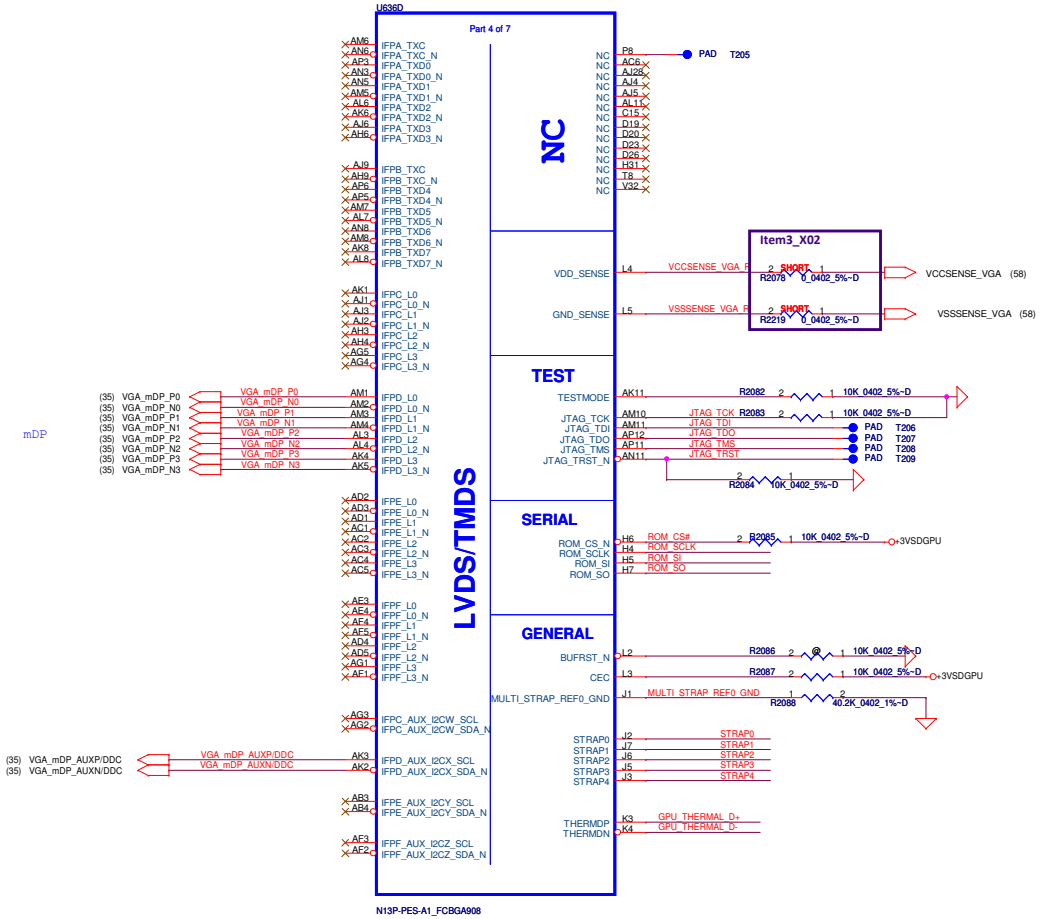
Compal Electronics, Inc.

Title: N13P (1/10) PEG,DAC

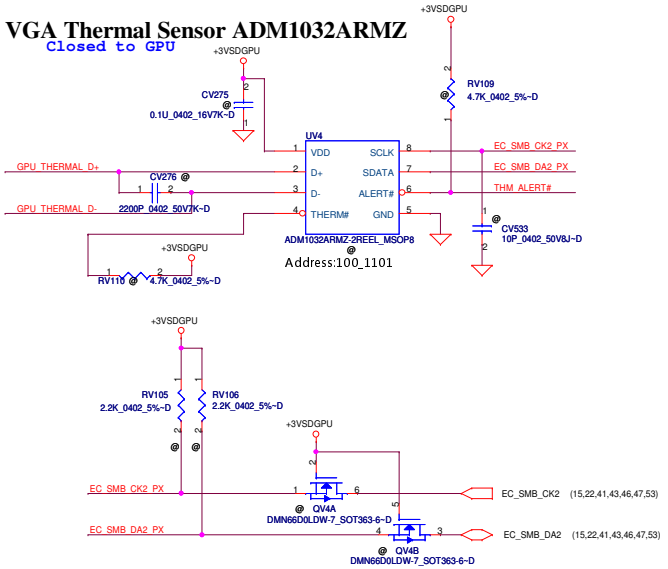
Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 Sheet 22 of 63

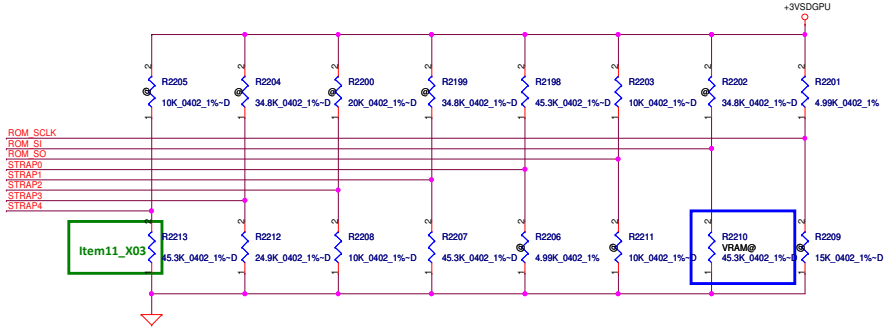


VGA Thermal Sensor ADM1032ARMZ

Closed to GPU



MULTI LEVEL STRAPS



For N13P-GT strap table

GPU	Frenq.	Memory Size	Memory Config	ROM_SCLK	ROM_SI	ROM_SO	STRAP0	STRAP1 (PCIe driving)	STRAP2 (ES PH20K)	STRAP3	STRAP4
N13P-GT	2500 MHz	64M* 16* 8 1GB	Samsung SA00003RS0L	PH 5K	PL 45.3K SD03445328L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	64M* 16* 8 1GB	Hynix SA00003WL0L	PH 5K	PL 34.8K SD03434828L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	128M* 16* 8 2GB	Samsung SA000048E0L	PH 5K	PL 30.1K SD03430128L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 MHz	128M* 16* 8 2GB	Hynix SA00004GD0L	PH 5K	PL 24.9K SD03424928L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K

Compal Electronics, Inc.

Title: N13P (2/10) mDP, Strapping

Size: C | Document Number: LA-8381P | Rev: 0.1

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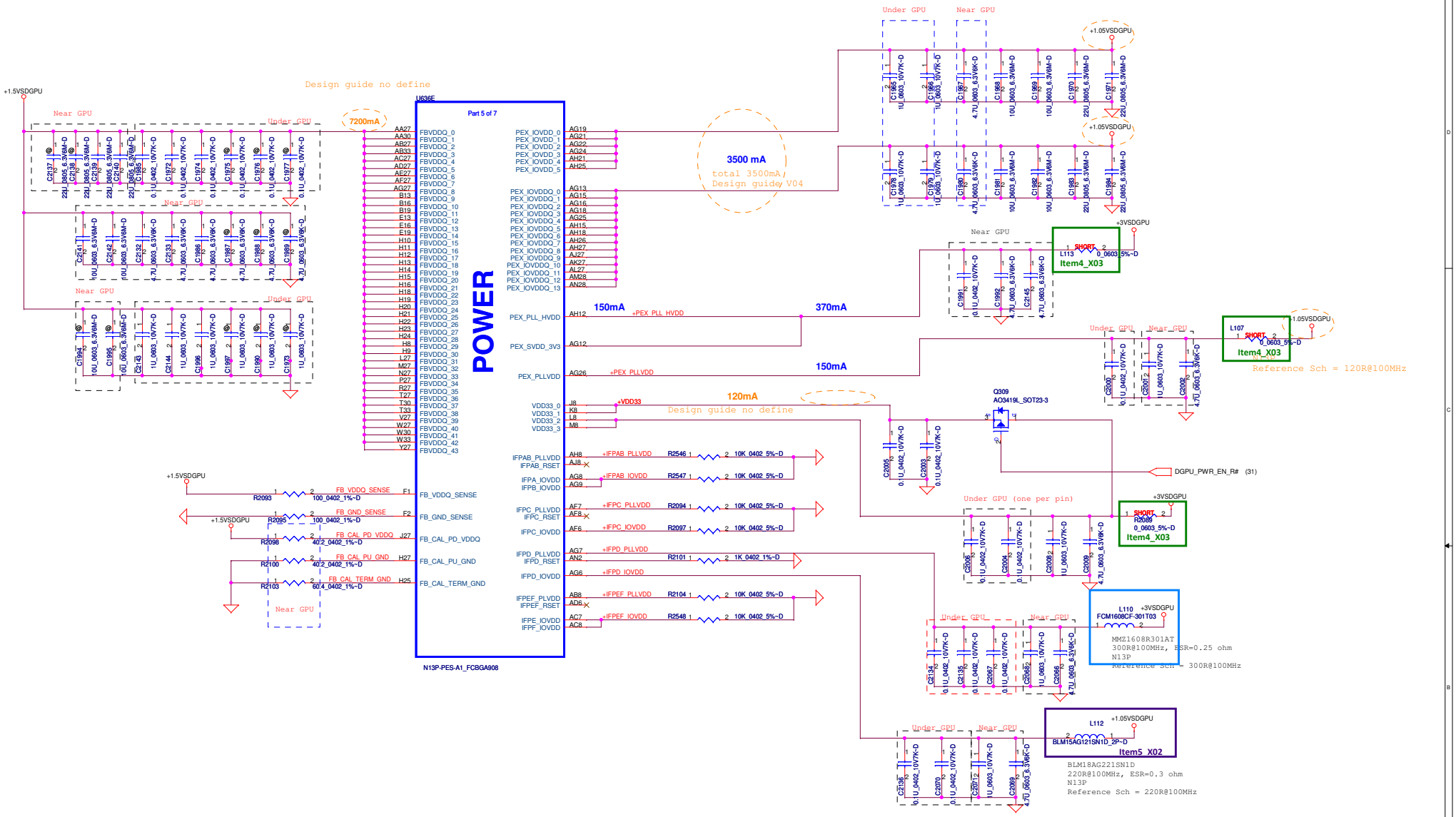

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Title: **N13P (3/10) POWER & GND**

Size	Document Number	Rev
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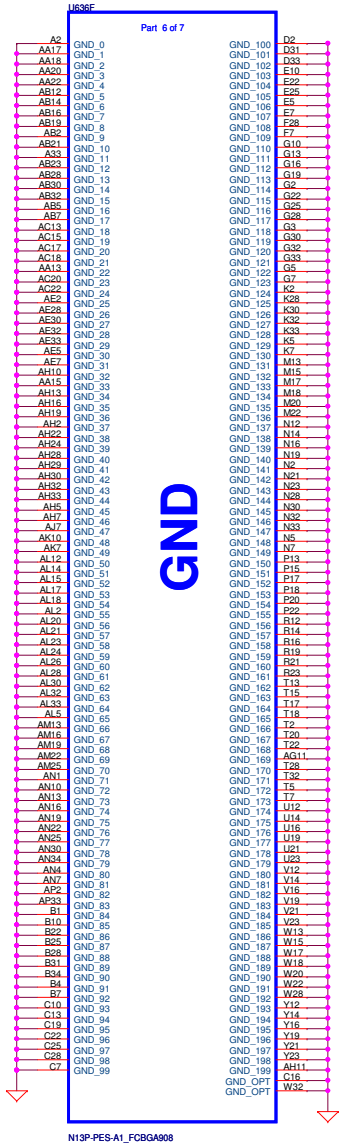
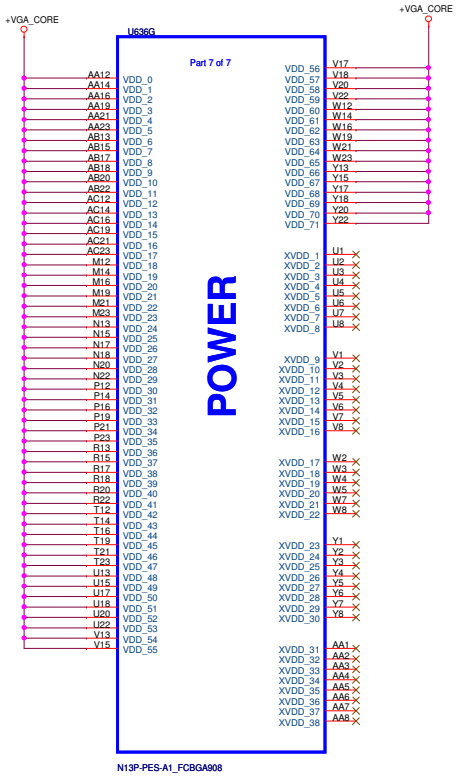
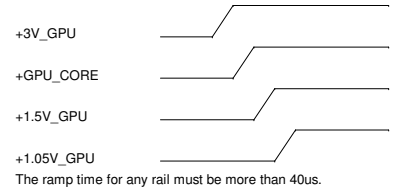




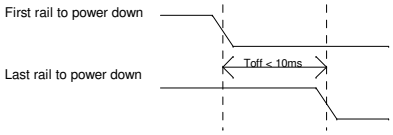
SEQUENCE

GPU Power Up Power Rail Sequence

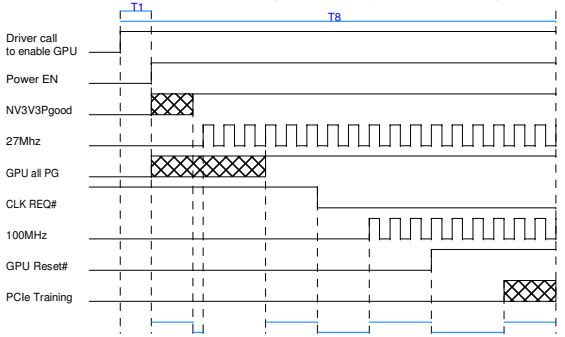


The ramp time for any rail must be more than 40us.

GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Up Sub-system Sequence

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Compal Electronics, Inc.			
Title: N13P (4/10) POWER & GND			
Size: C	Document Number: LA-8381P		Rev: 0.1
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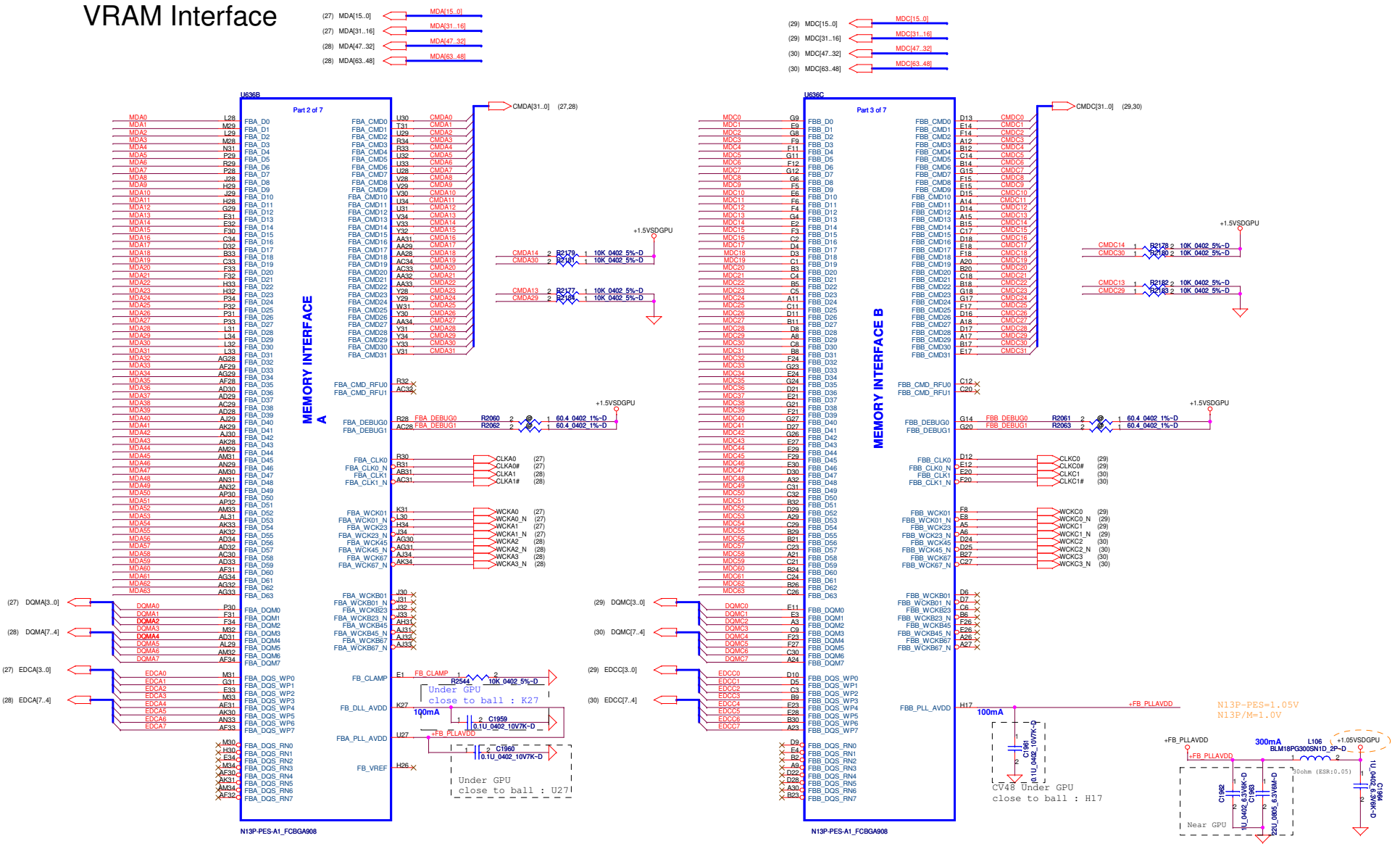
VRAM Interface



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Compal Electronics, Inc.			
Title: N13P (5/10) VRAM interface			
Size: C	Document Number: LA-8381P		Rev: 0.1
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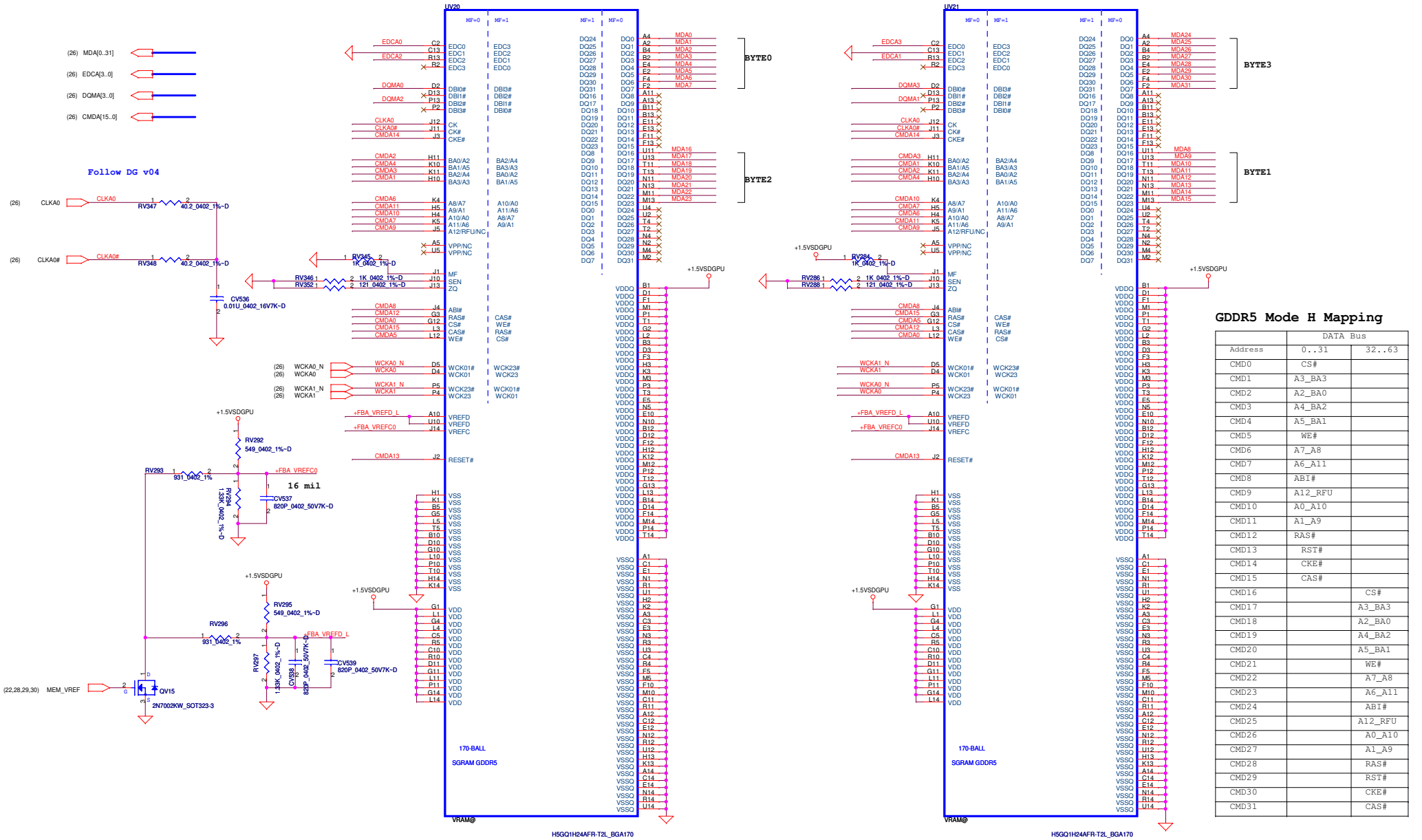
Memory Partition A - Lower 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Compal Electronics, Inc.

Title: N13P (6/10) VRAM A Lower

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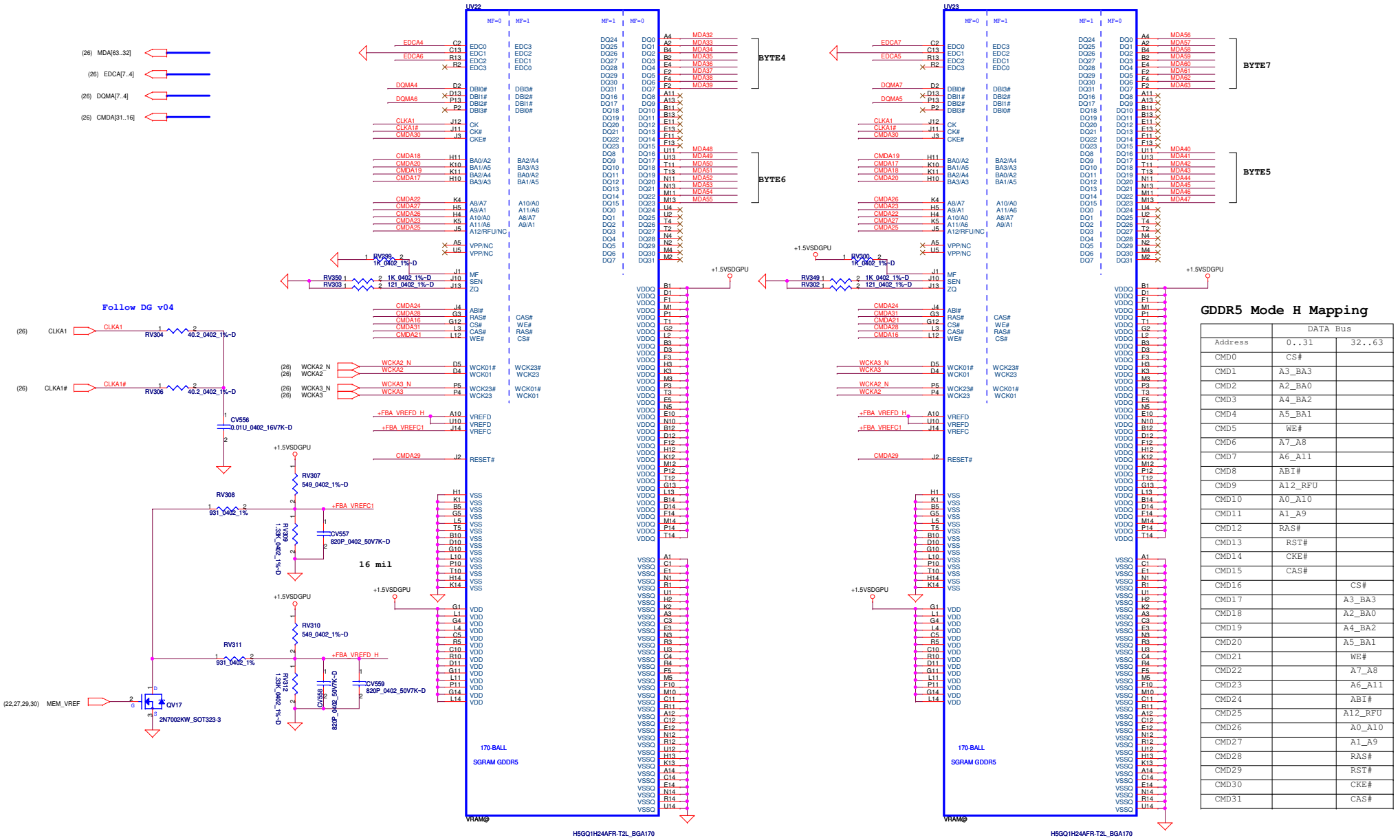
Memory Partition A - Upper 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **N13P (7/10) VRAM A Upper**

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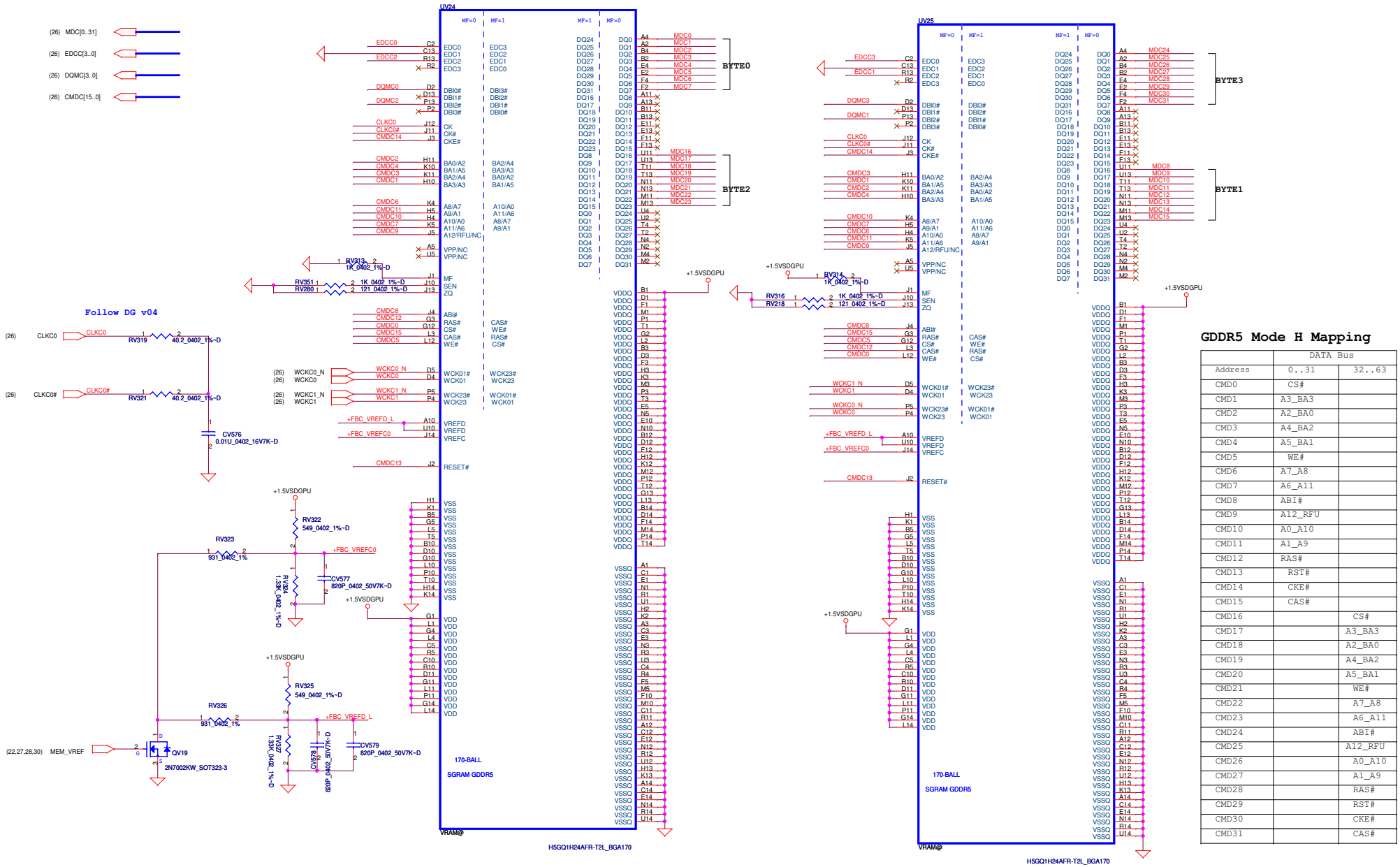
Memory Partition C - Lower 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Compal Electronics, Inc.

Title: N13P (8/10) VRAM B Lower

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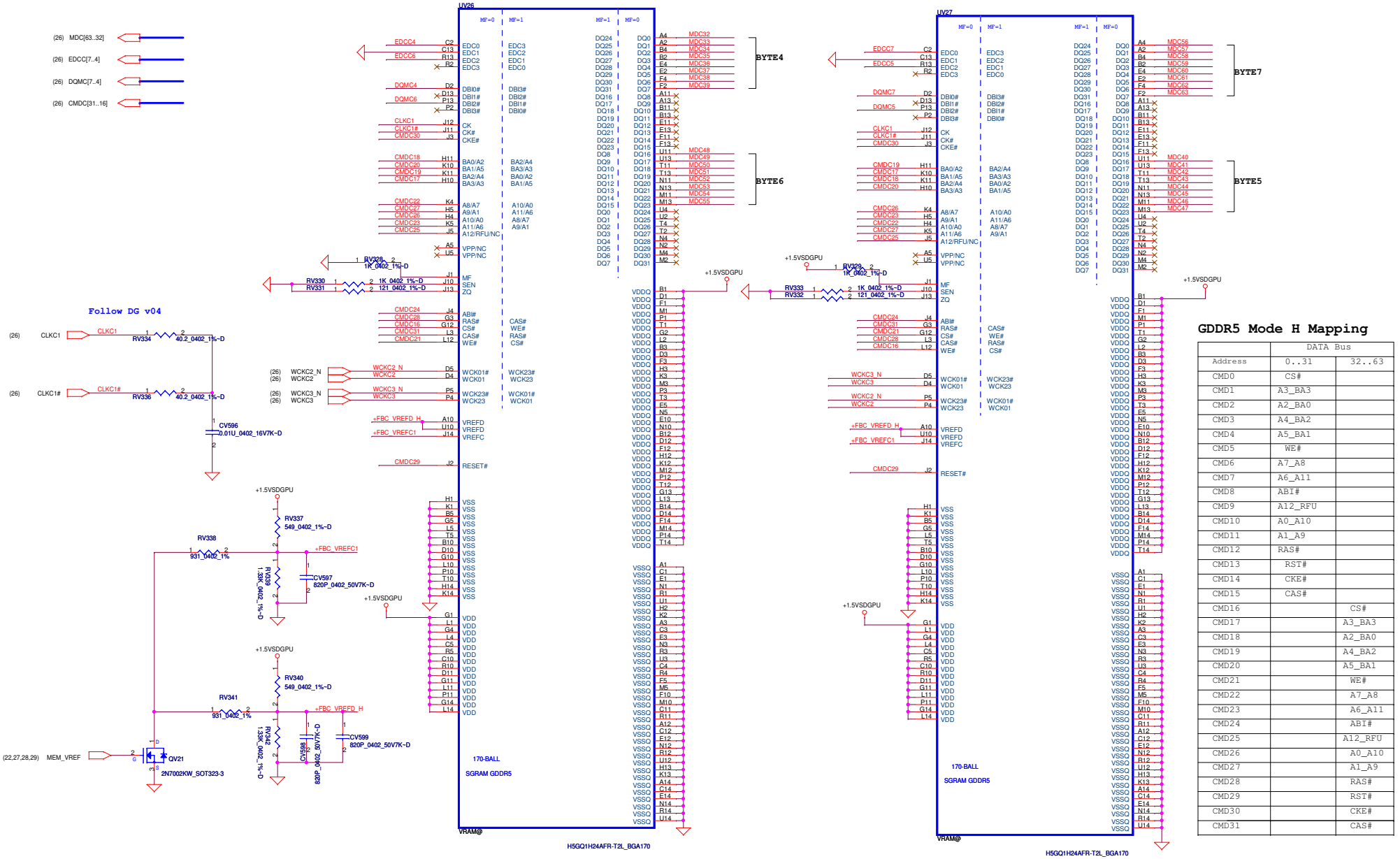
Memory Partition C - Upper 32 bits



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Compal Electronics, Inc.

Title: N13P (9/10) VRAM B Upper

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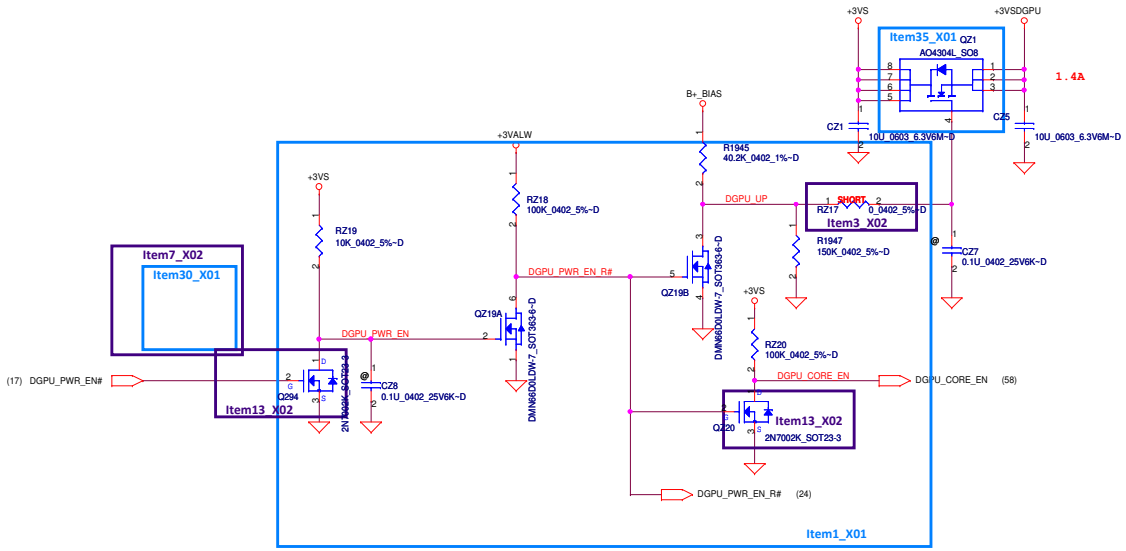
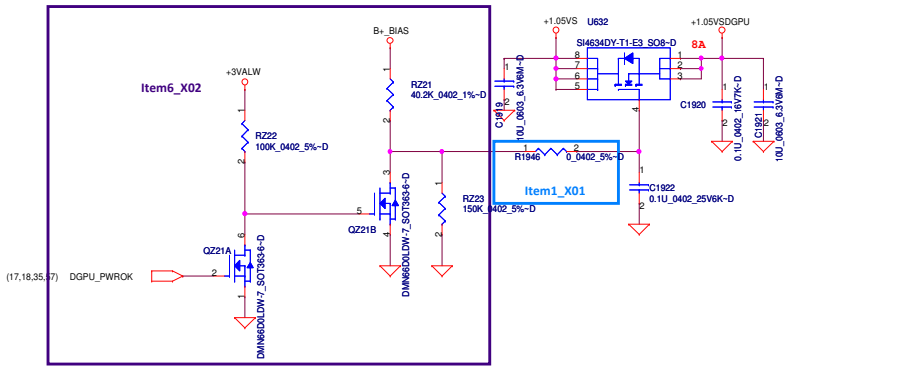
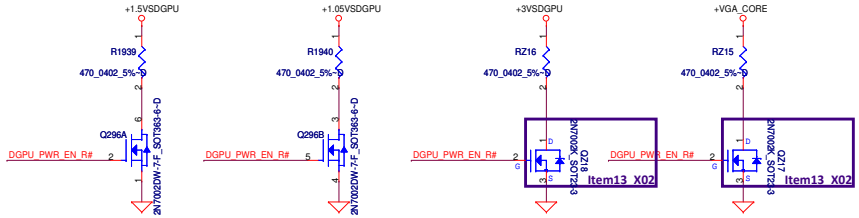
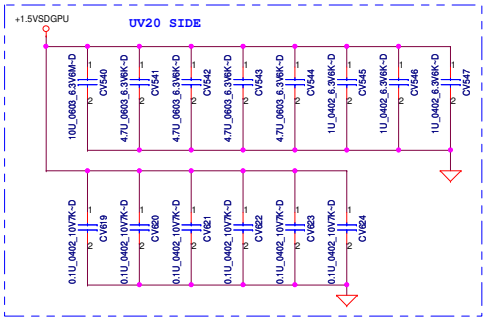
+3VS to +3VSDGPU

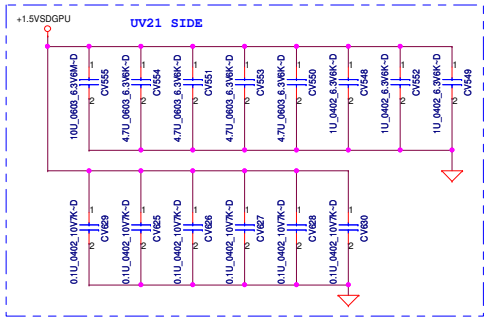
+1.05V to +1.05VSDGPU Transfer

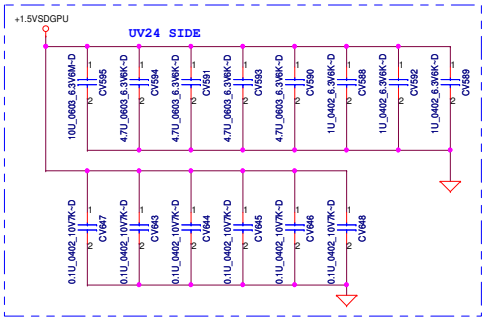


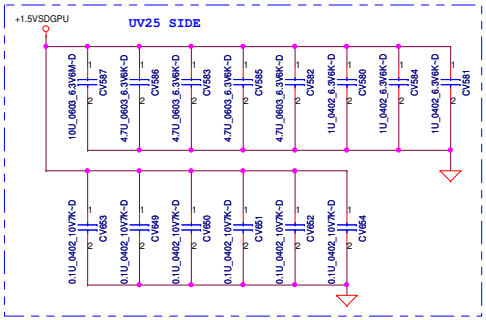


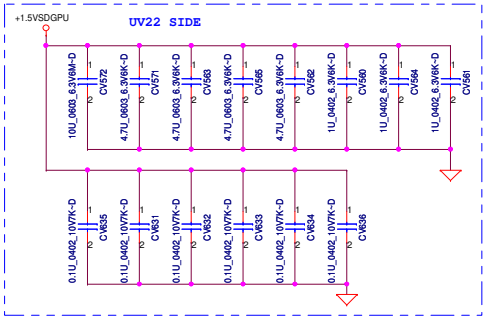


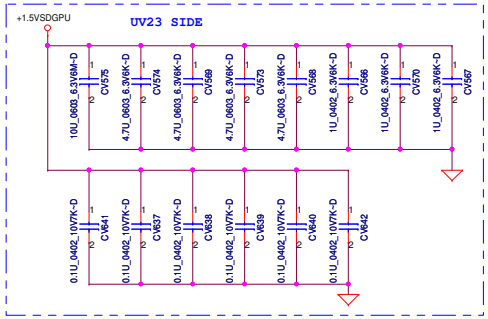


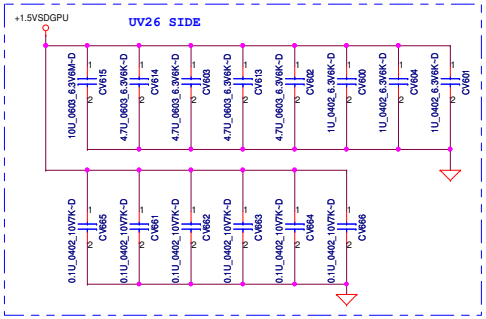


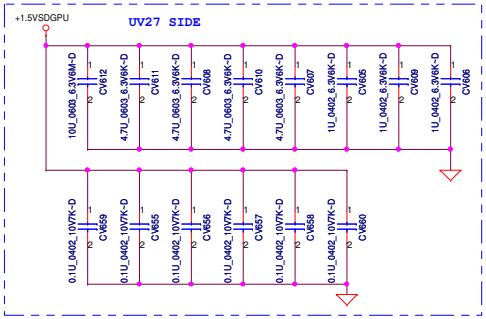












Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **N13P (10/10) DC/DC interface**

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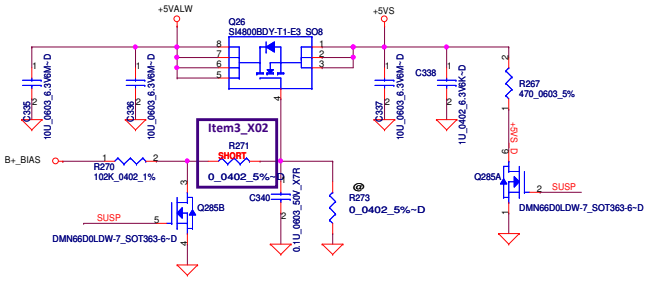
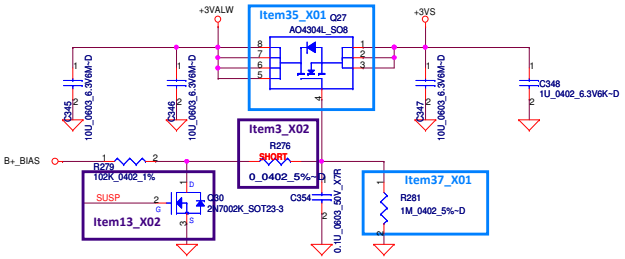
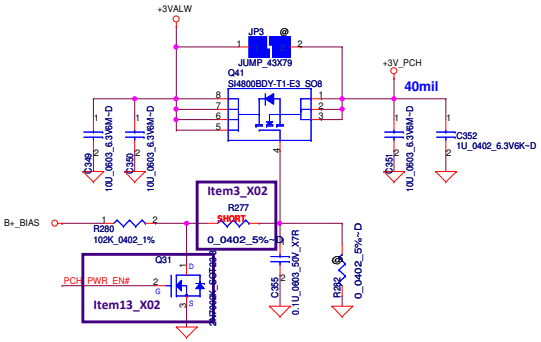
+5VALW to +5VS



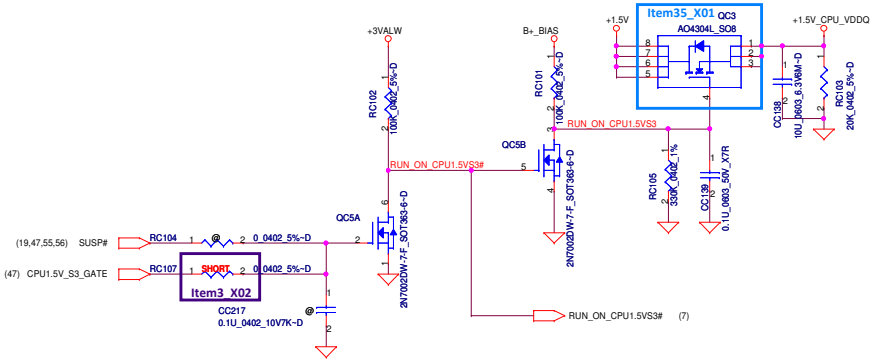
+3VALW to +3VS

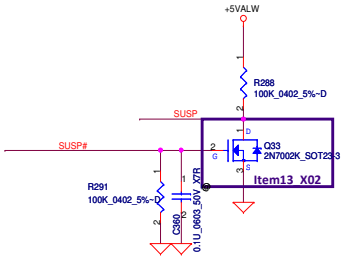


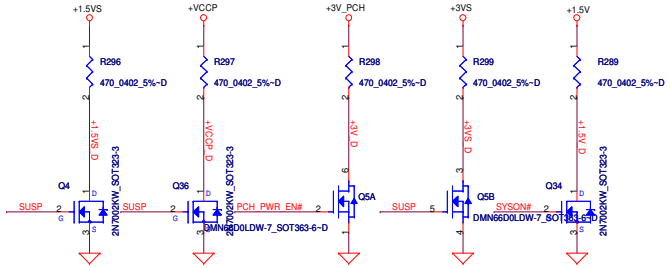
+3VALW to +3V_PCH

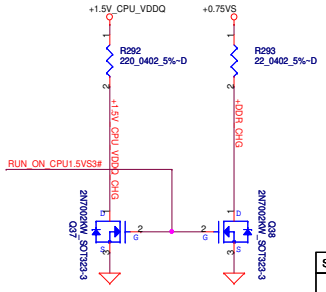


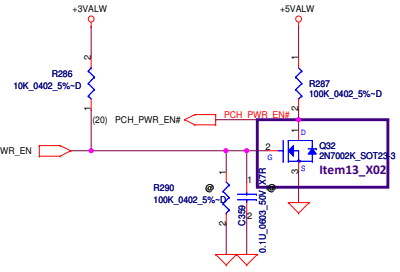
+1.5V to +1.5V_CPU_VDDQ

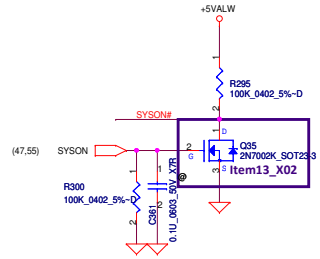












Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size	Document Number	Rev
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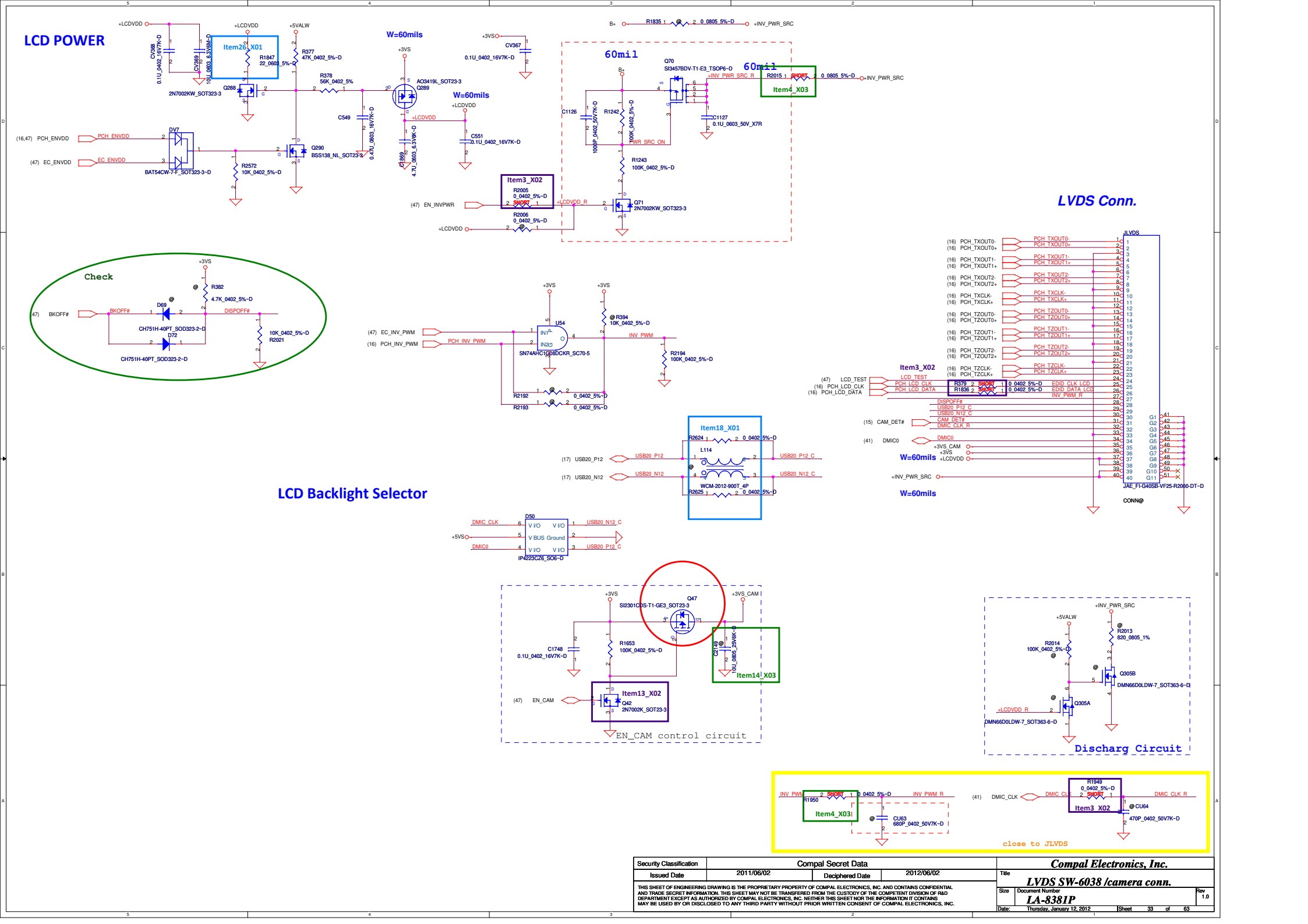

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **LVDS SW-6038 /camera conn.**

Size	Document Number	Rev
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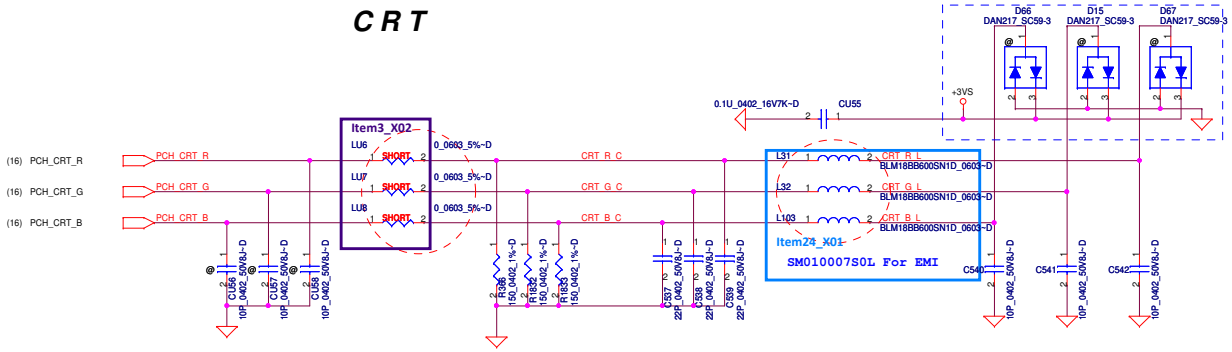
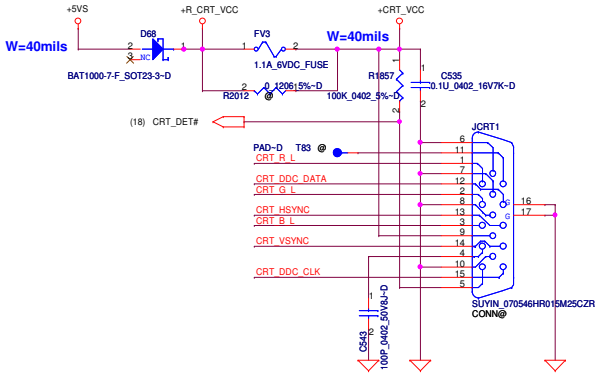
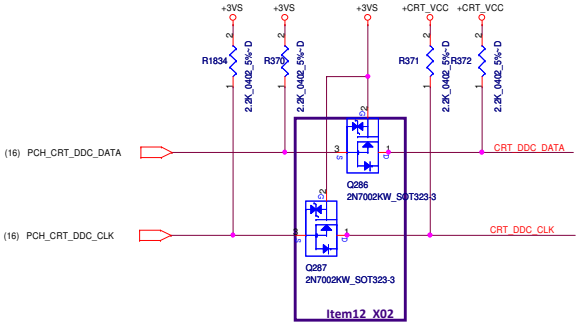
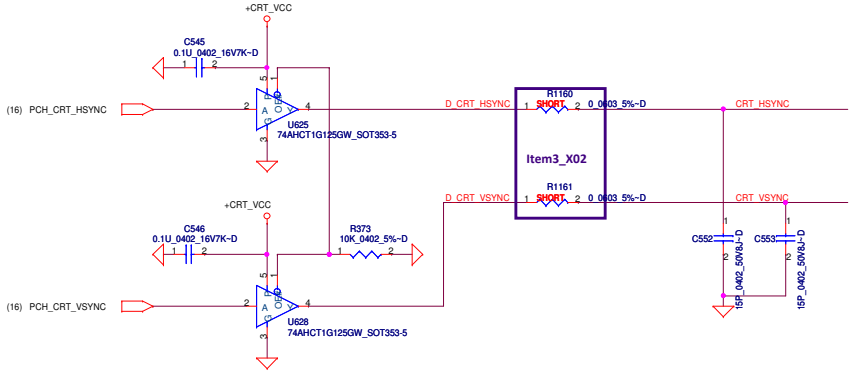
CRT









Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **VGA Conn.**

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X76 BOM option table

PARADE:	
U5 = SA00004ZM00	
C2018 = SE00000888L (2.2uF_0402)	
R2633 = SD02800008L	
Other = NC*	
TI:	
U5 = SA00004ZK0L	
C2018 = SE000000K8L (1uF_0402)	
R2641 = SD02800008L	
R2642 = SD02800008L	
Other = NC*	
PERICOM:	
U5 = SA00004ZN0L	
R2526 = SD02847018L (4.7K_0402)	
R2631 = SD02847018L (4.7K_0402)	
Other = NC*	

DP Redriver

Near to NV

DP Re-Driver config

Item4_X03

Item9_X02

Item19_X01

Item11_X02

Item29_X01

Co-lay

JMDP2

FOX_3V112M3-RH1HH7-7H

CONN@

Place close JDP1

RCLAMP0524P.TCT~D

PS8330BQFN48GTR-A0_QFN48_7X7

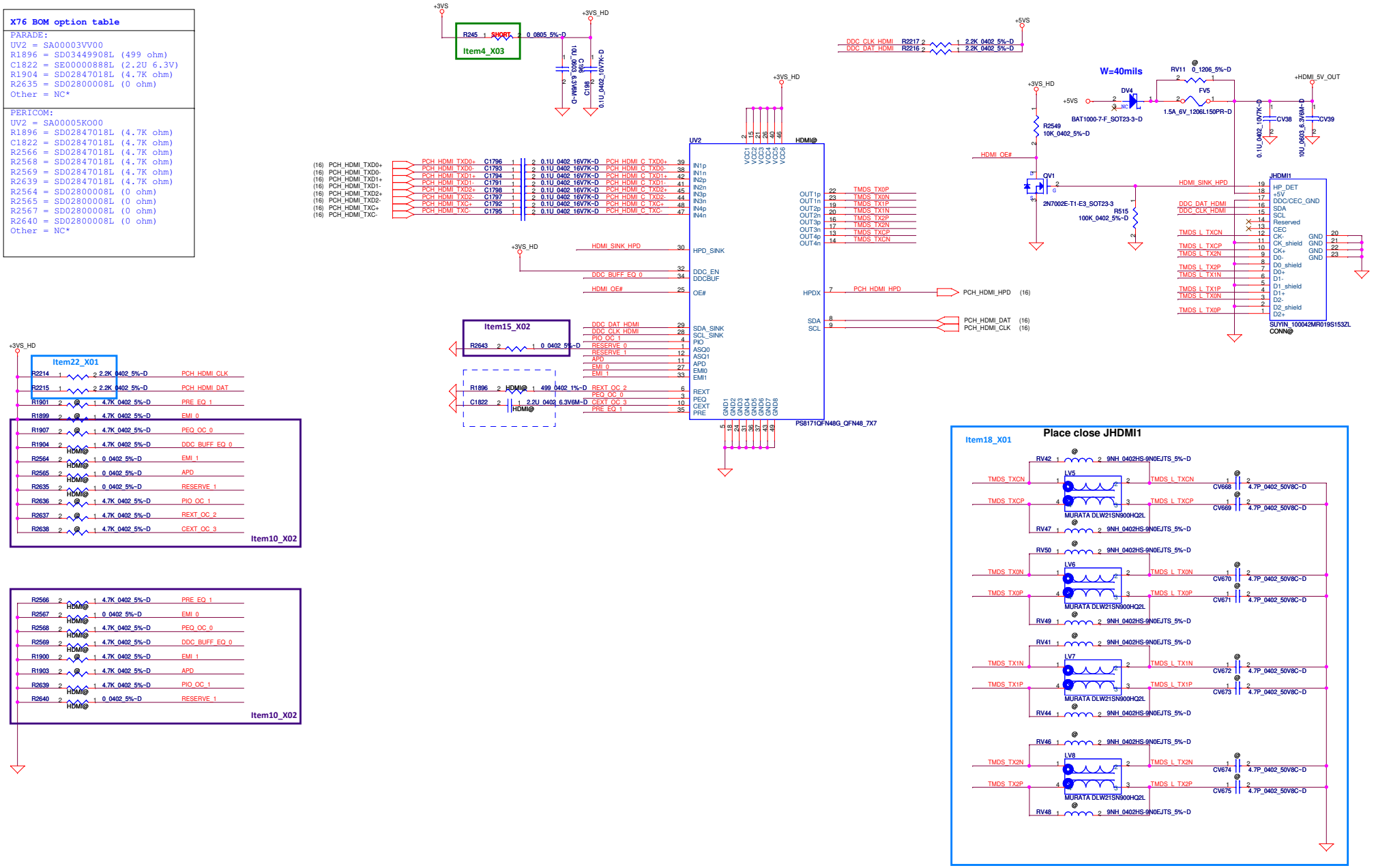
SN74AHC1G08DCKR_SC70-5

2N7002DW-7-F_SOT363-6-D

X76 BOM option table

PARADE:
UV2 = SA00003VV00
R1896 = SD03449908L (499 ohm)
C1822 = SE00000888L (2.2U 6.3V)
R1904 = SD02847018L (4.7K ohm)
R2635 = SD02800008L (0 ohm)
Other = NC*

PERICOM:
UV2 = SA00005KO00
R1896 = SD02847018L (4.7K ohm)
C1822 = SD02847018L (4.7K ohm)
R2566 = SD02847018L (4.7K ohm)
R2568 = SD02847018L (4.7K ohm)
R2569 = SD02847018L (4.7K ohm)
R2639 = SD02847018L (4.7K ohm)
R2564 = SD02800008L (0 ohm)
R2565 = SD02800008L (0 ohm)
R2567 = SD02800008L (0 ohm)
R2640 = SD02800008L (0 ohm)
Other = NC*



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **HDMI SW**

Size	Document Number	Rev
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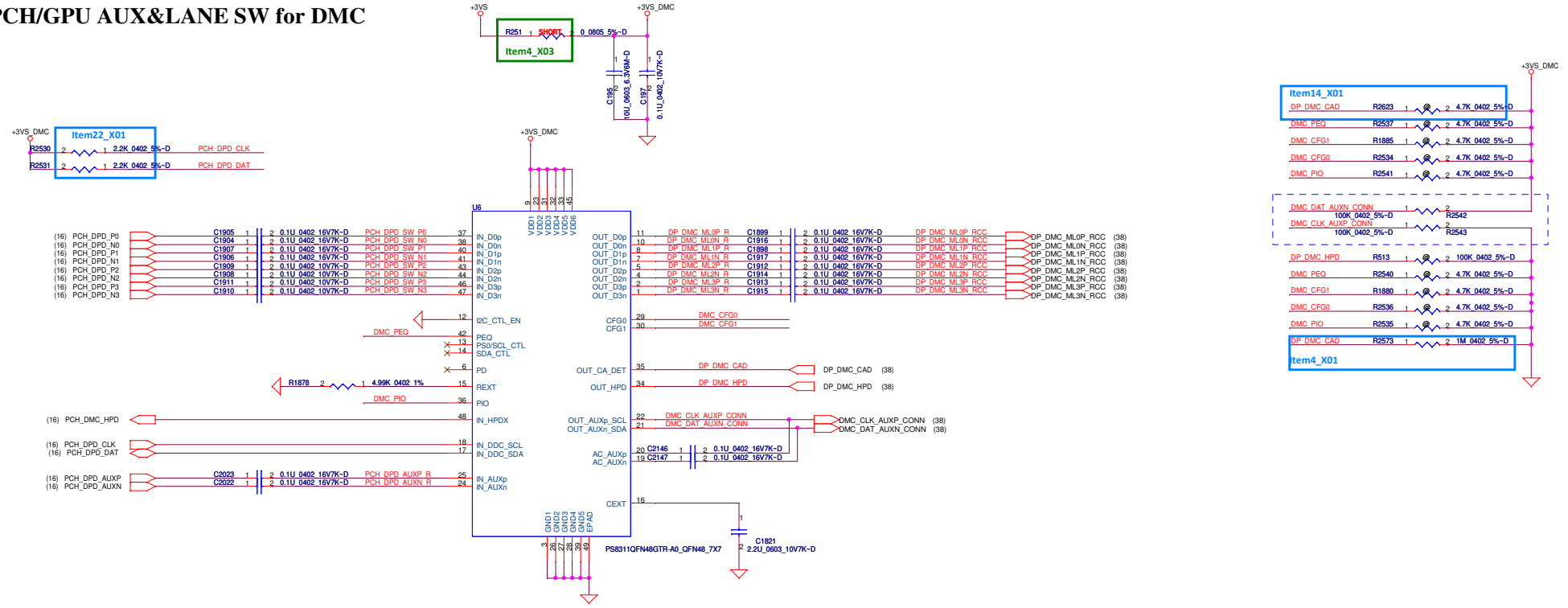
PCH/GPU AUX&LANE SW for DMC



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **DMC MUX/Redriver**

Size	Document Number	Rev
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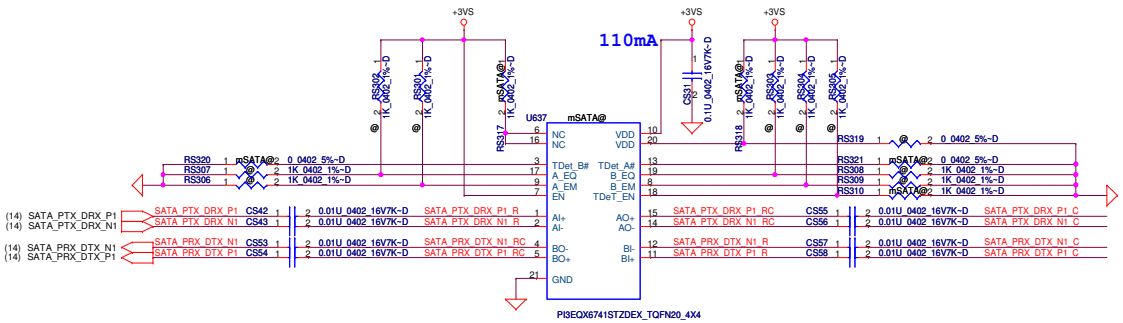
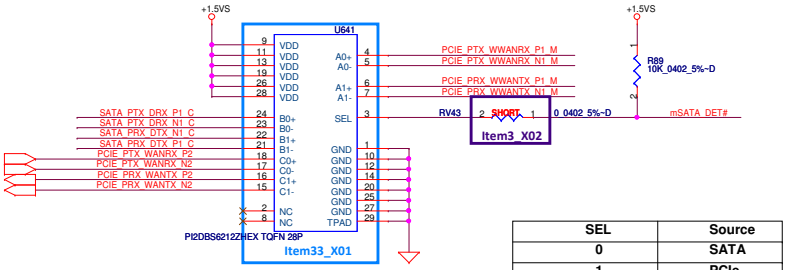
X76 BOM option table
PERICOM (PI3EQX6741): U637 = SA00004H100 RS318 = SD02800008L (0 ohm) Other = NC*
PARADE (PS8520B): U637 = SA00004WF00 RS317 = SD02800008L (0 ohm) RS320 = SD02800008L (0 ohm) RS321 = SD02800008L (0 ohm) Other = NC*
TI (SN75LVCP601RTJR): U637 = SA00003ZX0L RS310 = SD02800008L (0 ohm) RS318 = SD02800008L (0 ohm) RS320 = SD02800008L (0 ohm) RS321 = SD02800008L (0 ohm) Other = NC*

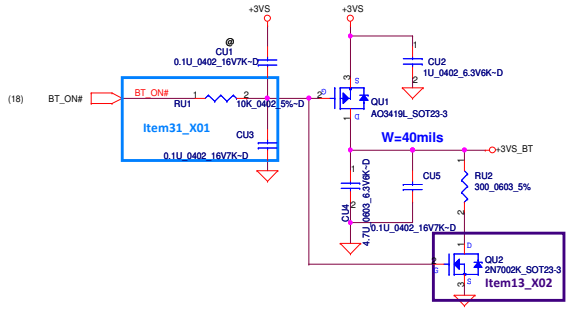
m-SATA ReDriver

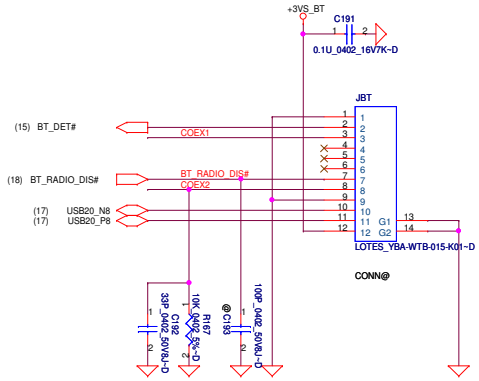




SEL	Source
0	SATA
1	PCIe

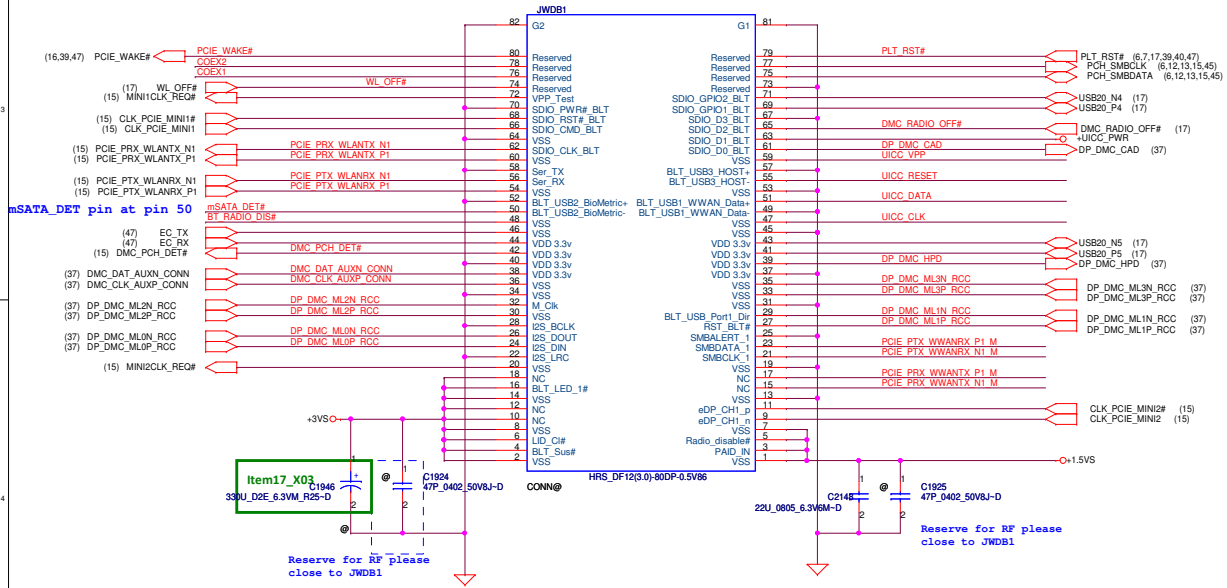
BlueTooth





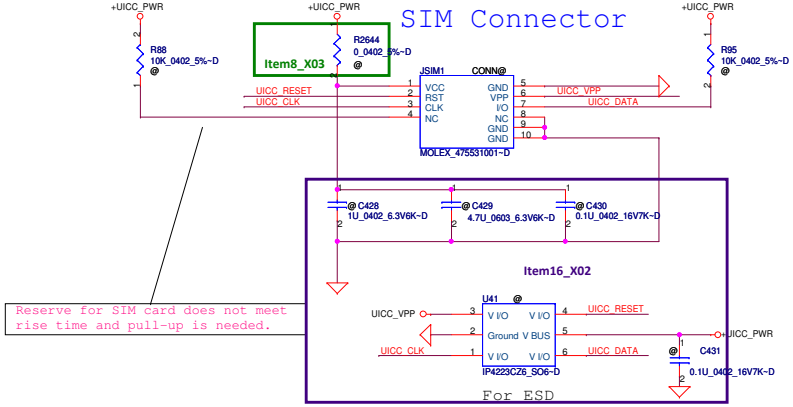
To DMC PCB connector

mSATA_DET pin at pin 50



SIM card board 4.7uF change to 1uF for Tiger detect issue.

SIM Connector



Reserve for SIM card does not meet rise time and pull-up is needed.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **Mini Card -WLAN / DMC / BT**

Size	Document Number	Rev
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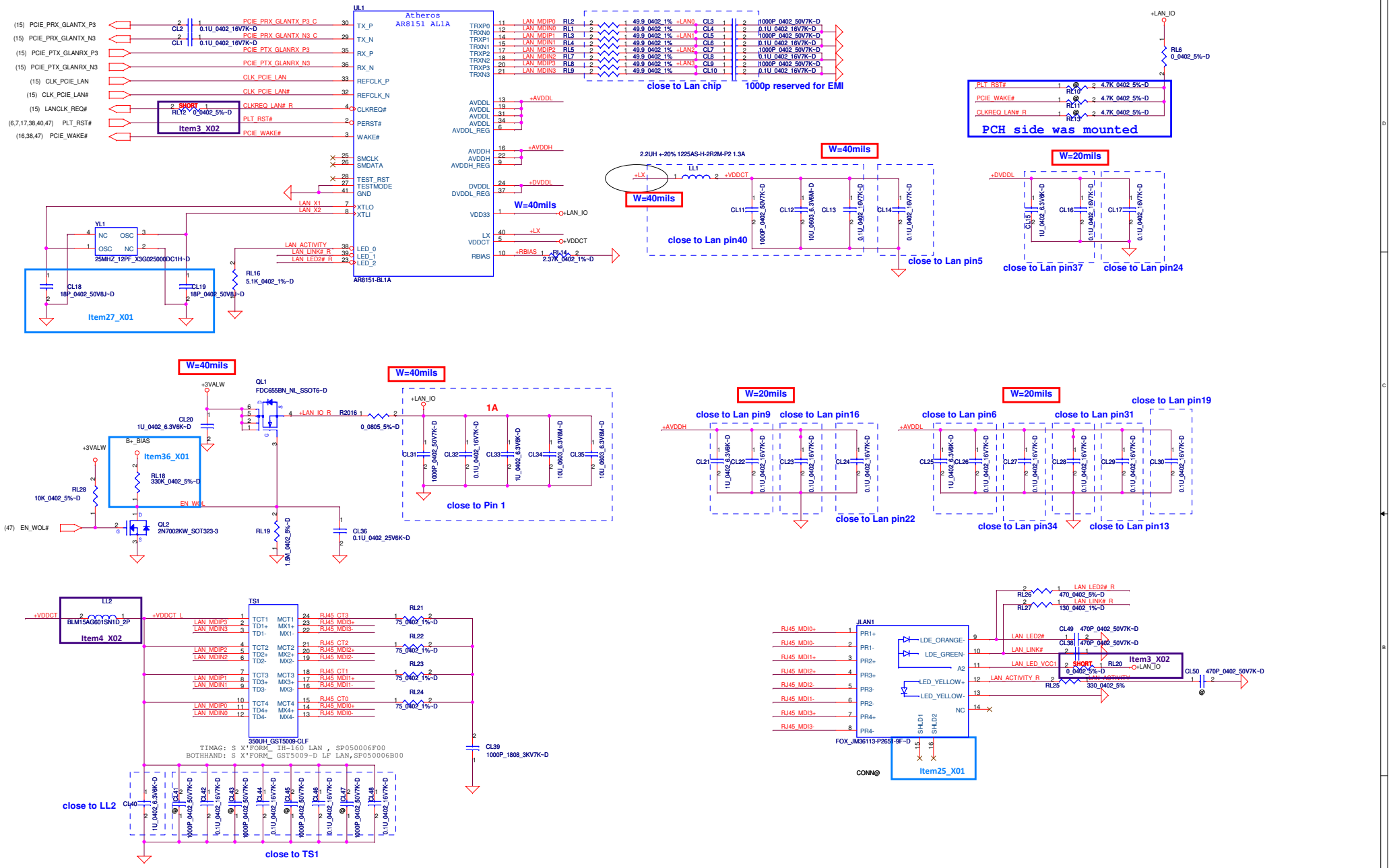

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: **GLAN AR8151 AL1A/ RJ45**

Size	Document Number	Rev
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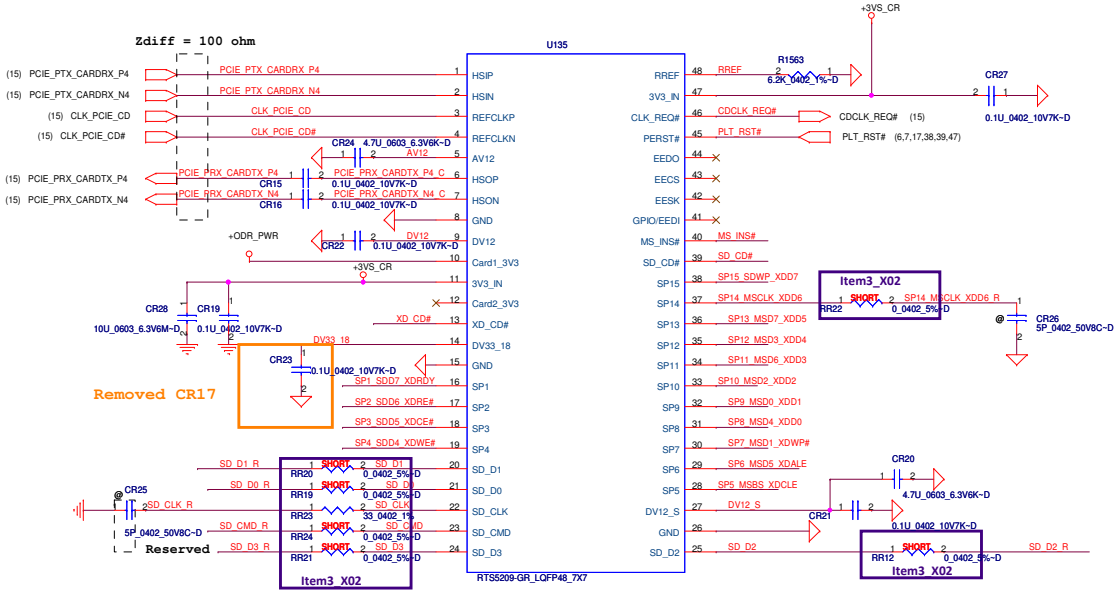
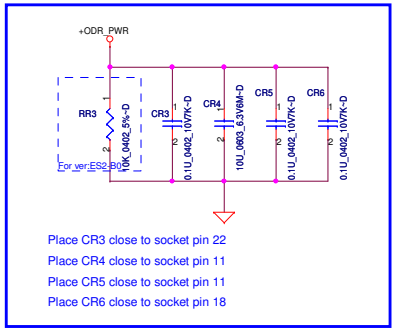
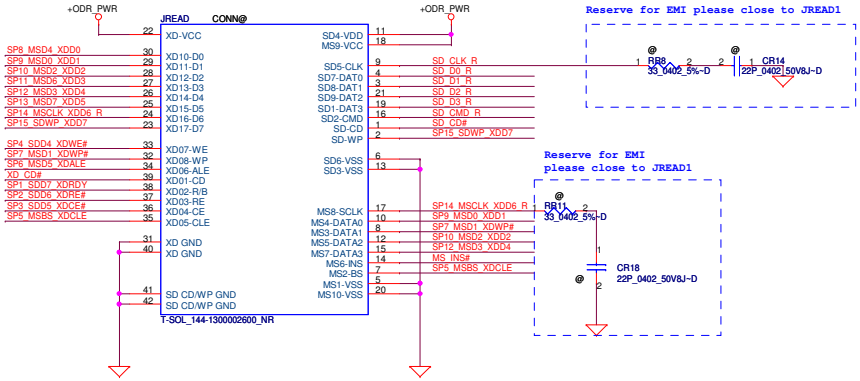
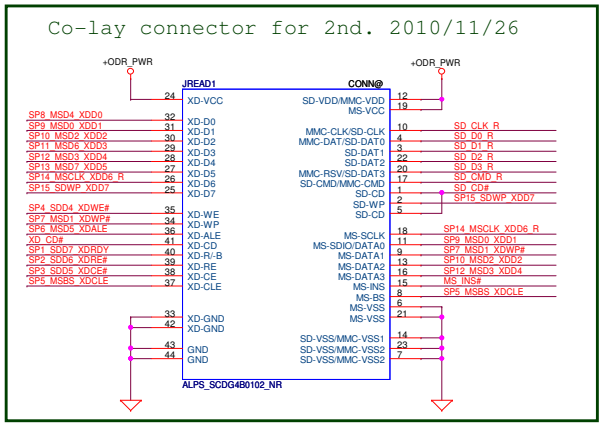
check IC support 9 in 1 function









Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: Card Reader RTS5209

Size	Document Number	Rev
	LA-8381P	1.0

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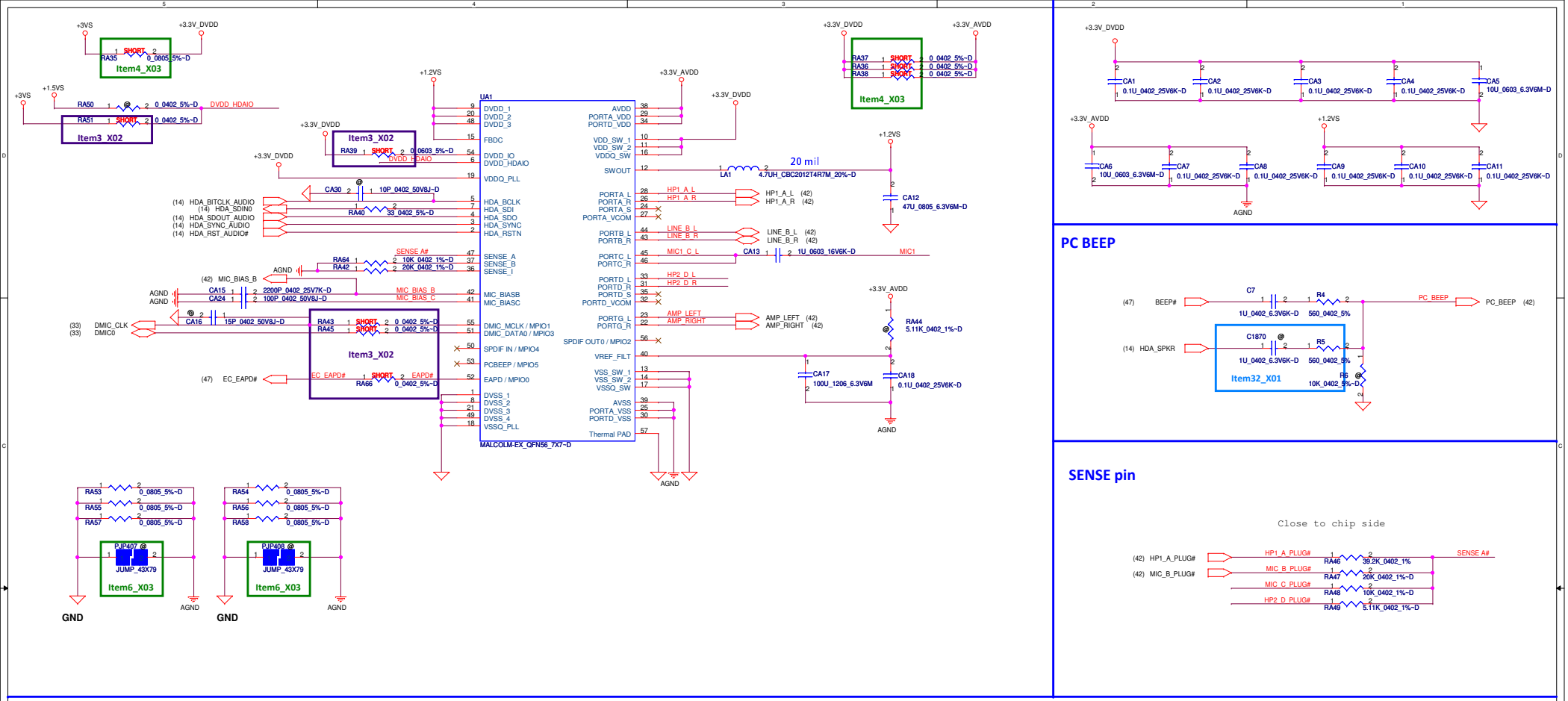

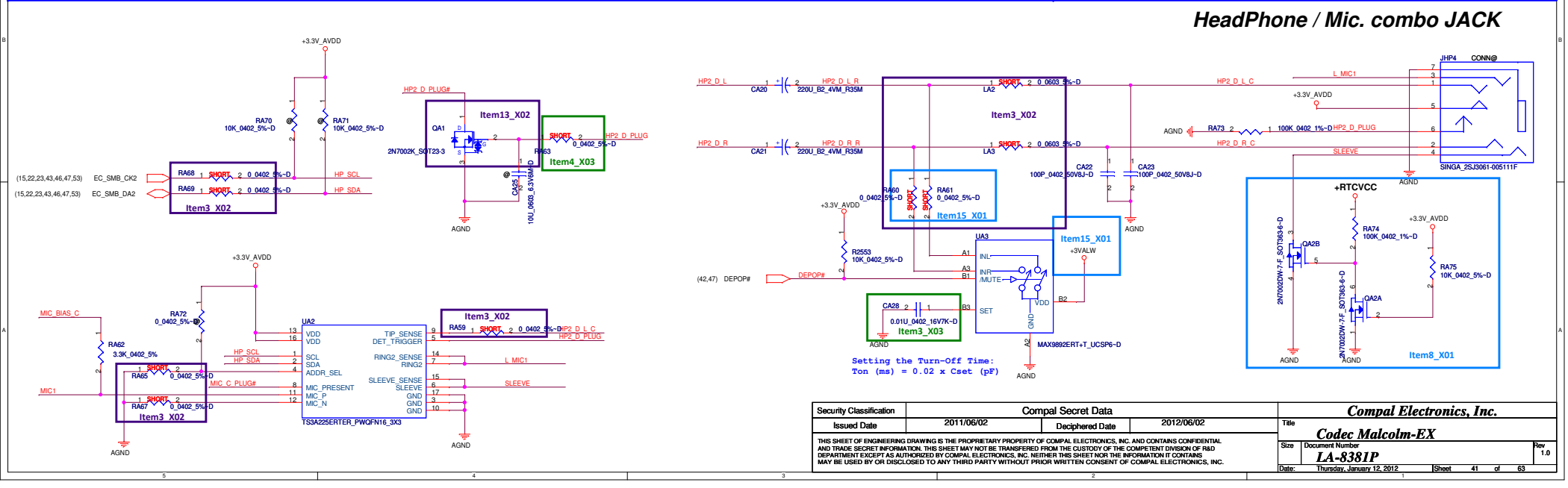

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **Codec Malcolm-EX**

Size	Document Number	Rev
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Line Out/HeadPhone

Mic. JACK

Int. Speaker Connector

Subwoofer support 3W

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

W=40mil

W=20mil

Item15_X01

Item3_X02

Item3_X03

Item12_X03

Item17_X01

Item10_X03

Item7_X01

Item1_X02

20mil

Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)

ANPEC
APA2031RI-TRG
SA00001R12

ANPEC
APA0714XAI-TRG
SA000059X00

either one option.

For ESD

Security Classification	Compal Secret Data
Issued Date	2011/06/02
Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: Amp TPA6017/subwoofer/ Audio Jack

Size	Document Number	Rev
	LA-8381P	1.0

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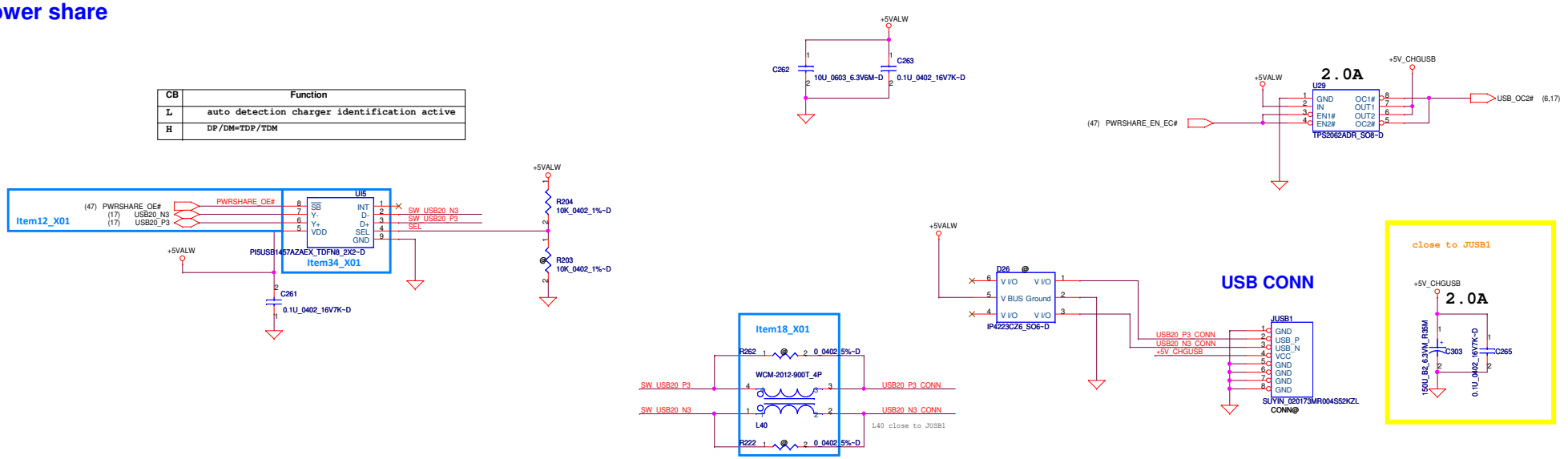
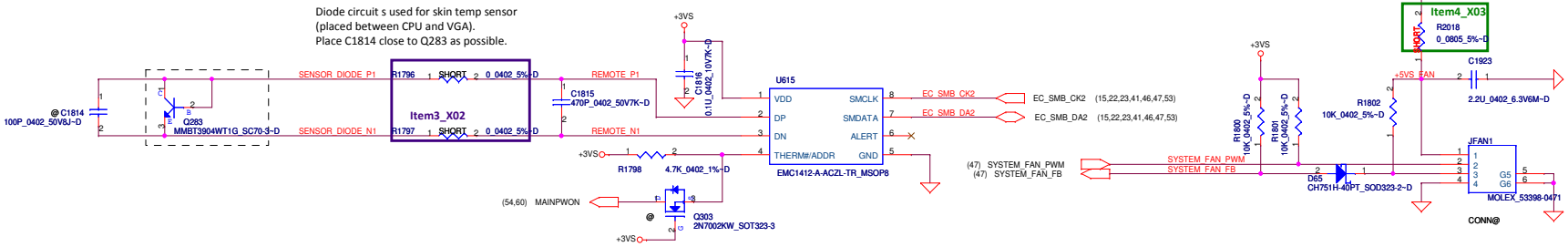
Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



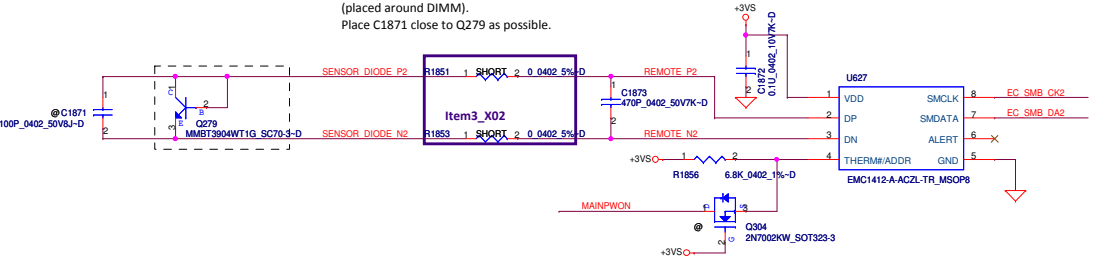
System Thermal Sensor 1

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.



System Thermal Sensor 2

Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C1871 close to Q279 as possible.



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: USB conn.

Size	Document Number	Rev
	LA-8381P	1.0

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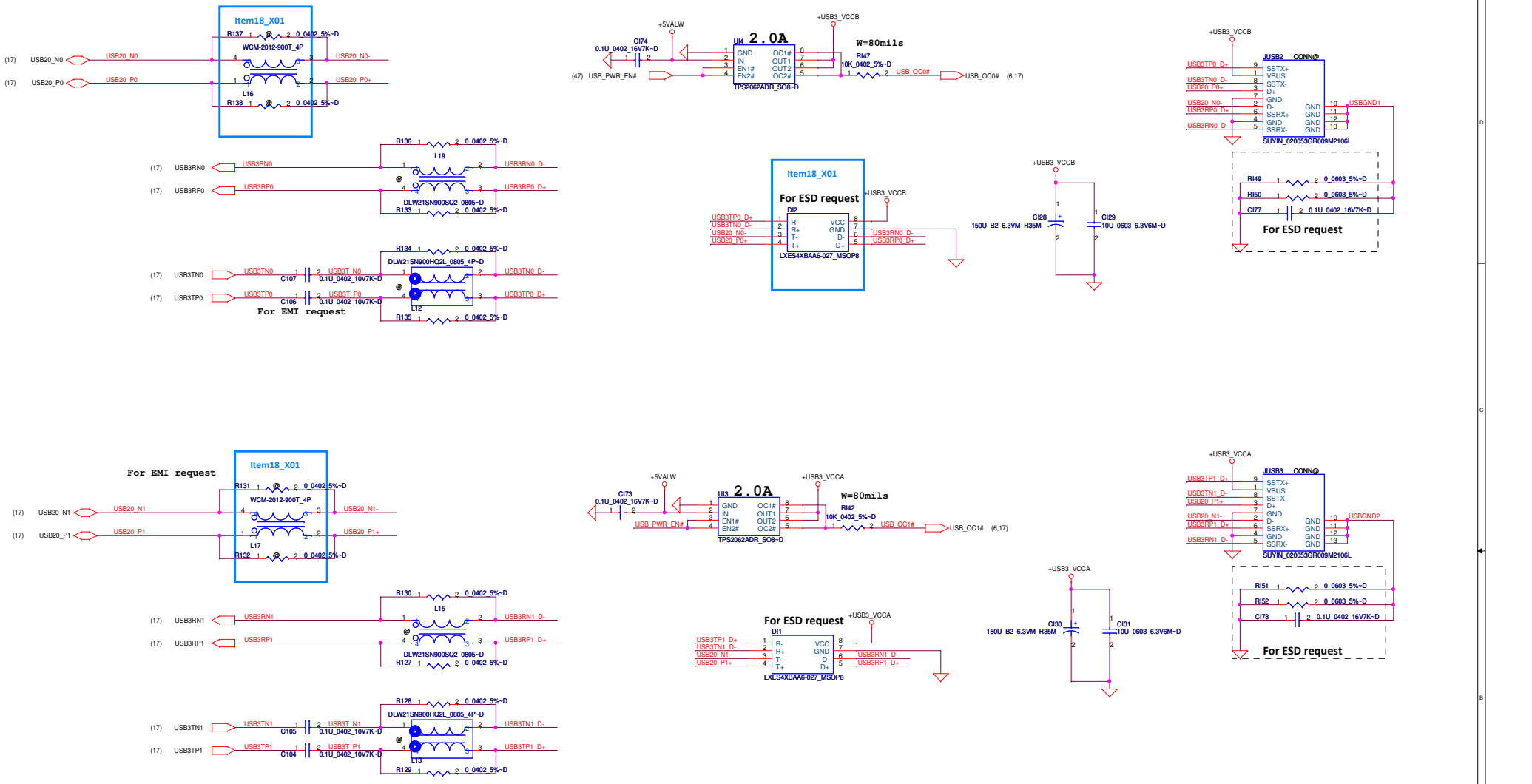

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: **USB conn.**

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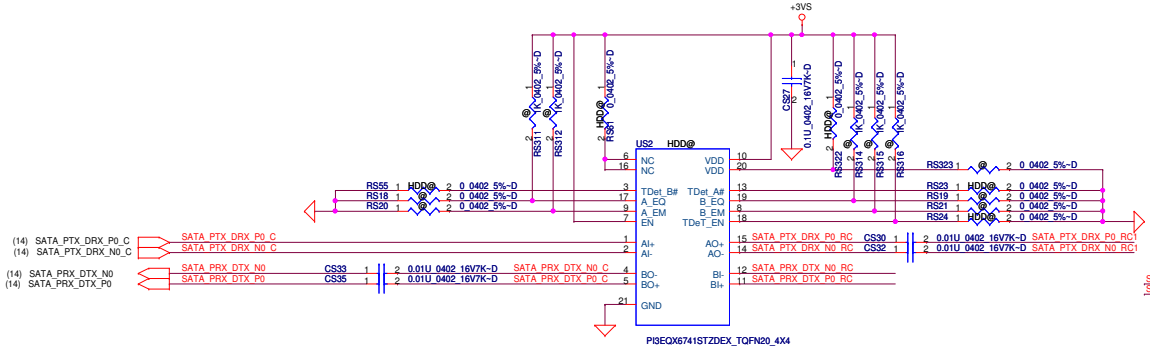
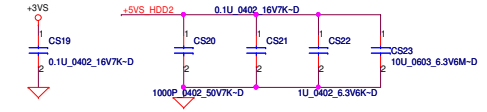
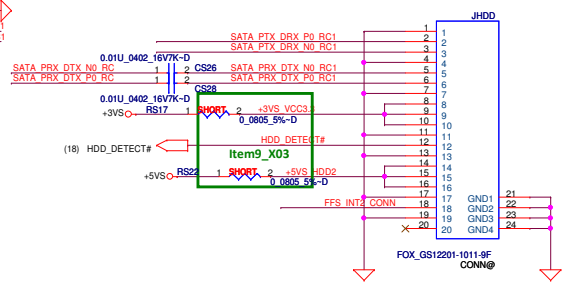
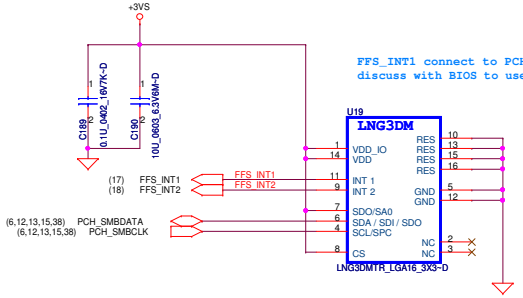
X76 BOM option table
PERICOM (PI3EQX6741): US2 = SA00004H100 RS322 = SD02800008L (0 ohm) Other = NC*
PARADE (PS8520B): US2 = SA00004WF00 RS23 = SD02800008L (0 ohm) RS55 = SD02800008L (0 ohm) RS61 = SD02800008L (0 ohm) Other = NC*
TI (SN75LVCP601RTJR): US2 = SA00003ZX0L RS23 = SD02800008L (0 ohm) RS24 = SD02800008L (0 ohm) RS55 = SD02800008L (0 ohm) RS322 = SD02800008L (0 ohm) Other = NC*



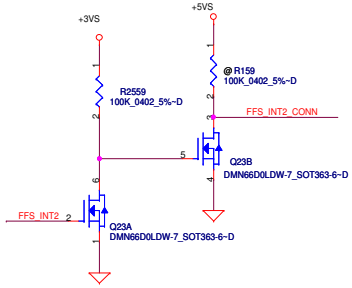




Free Fall Sensor

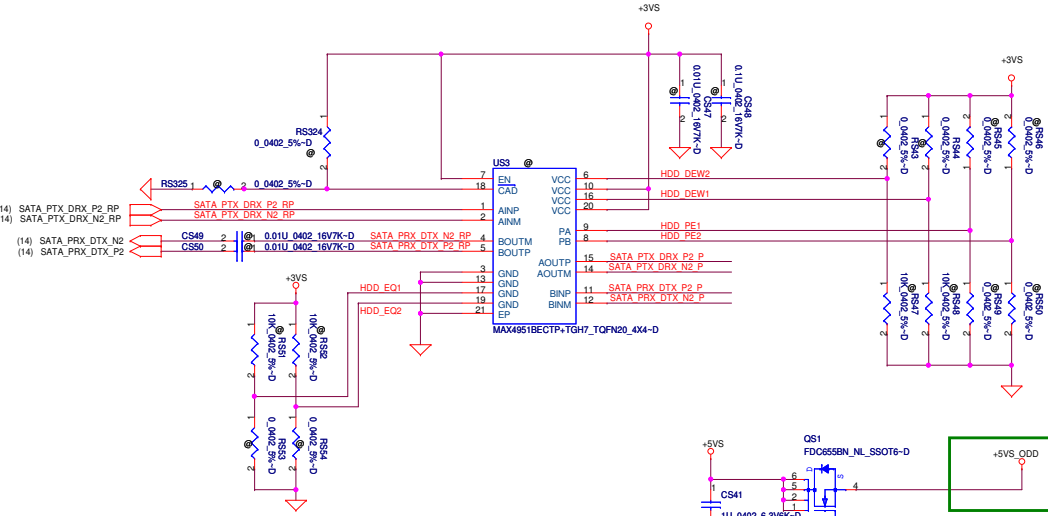


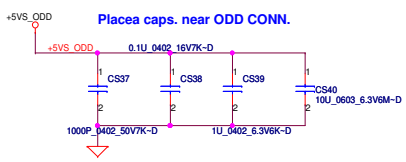
FFS_INT1 connect to PCH GPIO & EC discuss with BIOS to use which pin



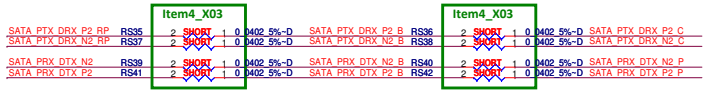
By Pass circuit

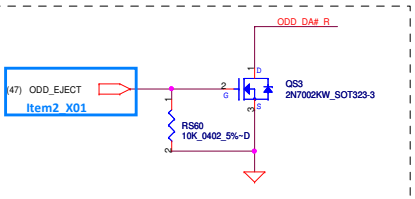
Item28_X01

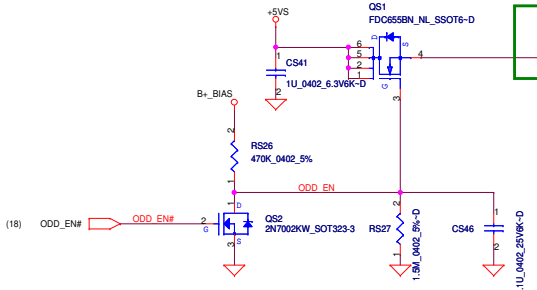


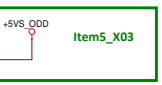


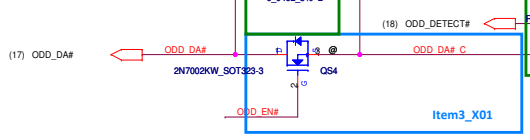
	MAXIM main	TI 2nd
P/N	SA00003LH1L	SA00003ZX0L
RS43 RS44	pop	depop
RS47 RS48	depop	pop
RS53 RS54	pop	depop



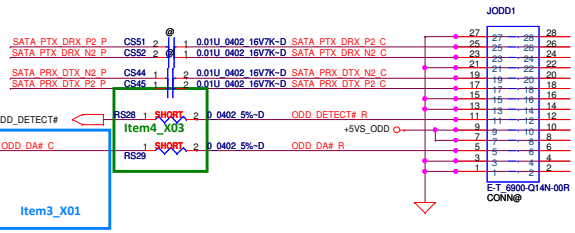








SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: FFS /HDD/ ODD Connector

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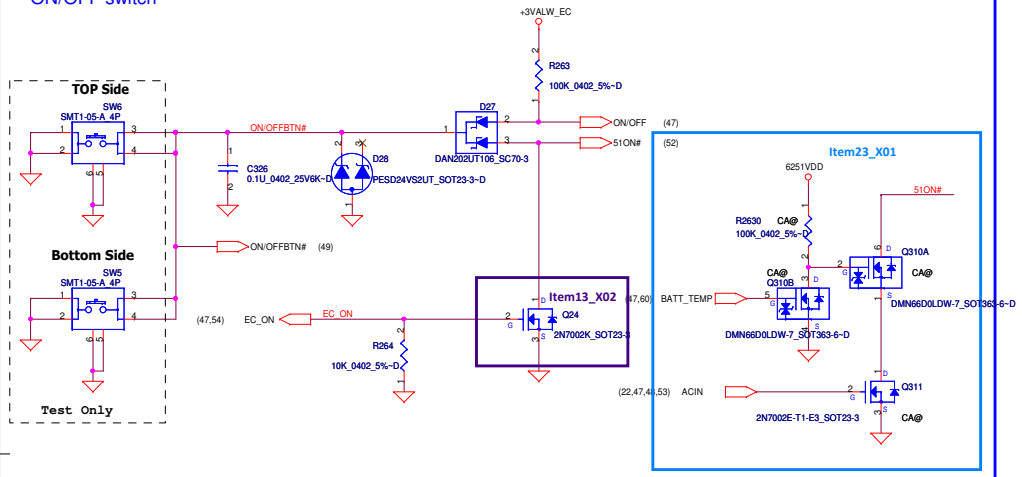
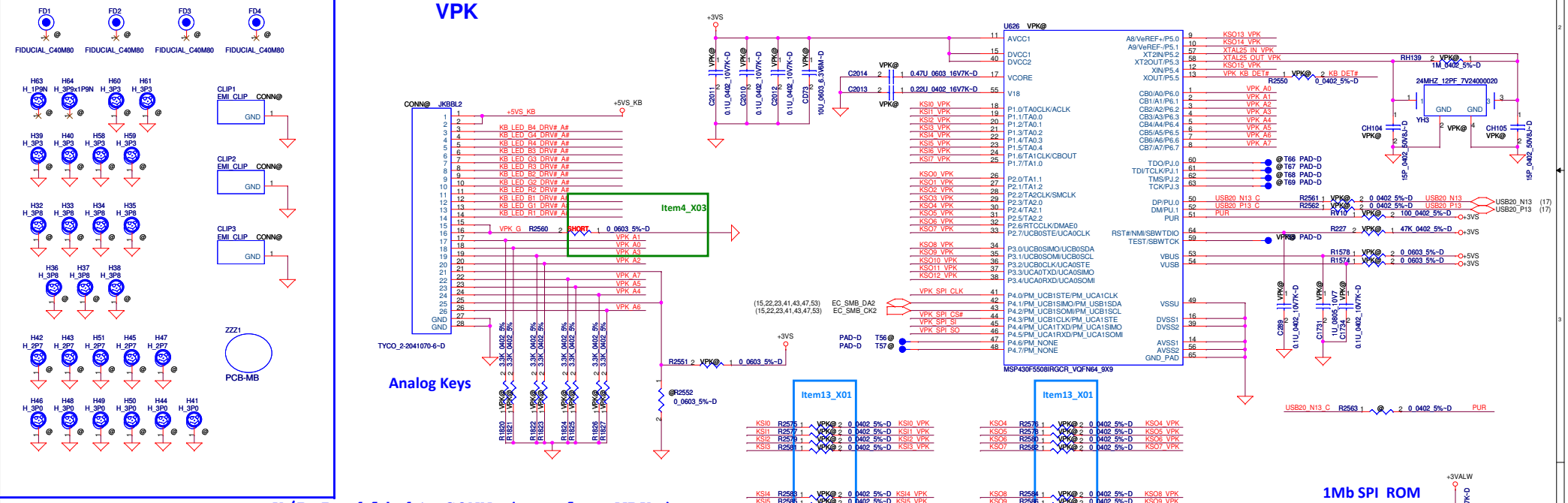
ON/OFF switch

Power Button

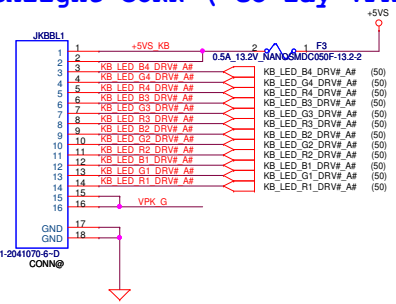


INT_KBD Conn.

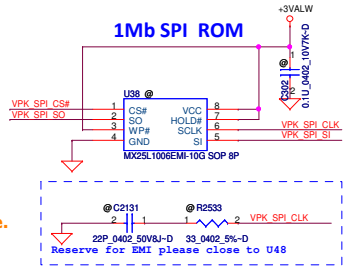
VPK



K/B Backlight CONN (co-lay VPK)



1Mb SPI ROM



8/17

1, Analog keys connector and F/P temporary use.
2, check pin assignment.
3, check VPK K/B layout.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PWRBTN/SCREWH/KB

Size	Document Number	Rev
	LA-8381P	1.0

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check GPIO table with BIOS team

+3VALW_EC

+3VALW

+3VLP

+3VALW_EC

L43 FBMA-L1_0603

+EC_VCCA

KSI[0..7]

KSO[0..16]

KSI[0..7] (46)

KSO[0..16] (46)

Item4_X03

10/1 ENE Recommand

R231 KSO1 47K_0402_5%~D

R232 KSO2 47K_0402_5%~D

R239 EC_SMI# 1K_0402_1%~D

R241 SPK_MUTE# 10K_0402_5%~D

R242 EC_ESB_CLK 4.7K_0402_5%~D

R243 EC_ESB_DAT 4.7K_0402_5%~D

R1952 LID_SW_IN# 10K_0402_5%~D

R2019 PCIE_WAKE#_R

R229 EC_SMB_CK1 2.2K_0402_5%~D

R230 EC_SMB_DA1 2.2K_0402_5%~D

R2574 KB_DET# 100K_0402_5%~D

Item8_X02

R216 0_0805_5%~D

R2538 SHORT 0_0402_5%~D

C277 C276 C278 C279 C280 0.1U_0402_16V7K~D

C281 1000P_0402_50V7K~D

C282 0.1U_0402_16V7K~D

ECAGND

C284 @22P_0402_50V8J~D

R226 @33_0402_5%~D

(17) CLK_PCI_LPC

R221 47K_0402_5%~D

(6,7,17,38,39,40) PLT_RST#

C285 0.1U_0402_16V7K~D

(18) EC_SCI#

(33) EN_CAM

U34

VCC VCC VCC VCC VCC VCC AVCC

LPC & MISC

(18) GATEA20

(18) KB_RST#

SERIRQ

(14) LPC_FRAME#

(14) LPC_AD3

(14) LPC_AD2

(14) LPC_AD1

(14) LPC_AD0

CLK_PCI_LPC

PLT_RST#

EC_SCI#

EN_CAM

GA20/GPIO00

KBRST#/GPIO01

SERIRQ#

LFRAME#

LAD3

LAD2

LAD1

LAD0

PCICLK

PCIRST#/GPIO05

ECRST#

SCI#/GPIO0E

CLKRUN#/GPIO1D

PWM Output

INVT_PWM/PWM1/GPIO0F

BEEP#/PWM2/GPIO10

FANPWM1/GPIO12

ACOFF/FANPWM2/GPIO13

BEEP# (41)

SYSTEM_FAN_PWM (43)

ACOFF (52,53)

AD Input

BATT_TEMP/AD0/GPIO38

BATT_OVP/AD1/GPIO39

ADP_I/AD2/GPIO3A

AD3/GPIO3B

AD4/GPIO42

SELIO2#/AD5/GPIO43

BATT_TEMP

ADP_I

AD_BID0

C286 100P_0402_50V8J~D

BATT_TEMP (46,60)

ADP_I (52,53)

DA Output

DAC_BRIG/DA0/GPIO3C

EN_DFAN1/DA1/GPIO3D

IREF/DA2/GPIO3E

DA3/GPIO3F

GPU_DC#

AC_SEL

IREF

CHGVADJ

GPU_DC# (22)

AC_SEL (52)

IREF (53)

CHGVADJ (53)

PS2 Interface

PSCLK1/GPIO4A

PSDAT1/GPIO4B

PSCLK2/GPIO4C

PSDAT2/GPIO4D

TP_CLK/PSCLK3/GPIO4E

TP_DATA/PSDAT3/GPIO4F

EC_MUTE#

PWRSHARE_EN_EC#

AC_PRESENT

H_PROCHOT#_EC

TP_CLK

TP_DATA

R228 SHORT 0_0402_5%~D

SPK_MUTE#

PWRSHARE_EN_EC# (43)

AC_PRESENT (16)

TP_CLK (49)

TP_DATA (49)

SPI Device Interface

SDICS#/GPXOA00

SDICLK/GPXOA01

SDIDO/GPXOA02

SDIDI/GPXID0

ODD_EJECT

EN_WOL#

HDA_SDO

LID_SW_IN#

ODD_EJECT (45)

EN_WOL# (39)

HDA_SDO (14)

LID_SW_IN# (15,48,49)

SPI Flash ROM

SPIDI/RD#

SPIDO/WR#

SPICLK/GPIO56

SPICS#

FRD#

R234 33_0402_5%~D FWR#

R_SPI_CLK R236 33_0402_5%~D SPI_CLK

R237 33_0402_5%~D SEL#

GPIO

CIR_RX/GPIO40

CIR_RLC_TX/GPIO41

FSTCHG/SELIO#/GPIO50

BATT_CHGI_LED#/GPIO52

CAPS_LED#/GPIO53

BATT_LOW_LED#/GPIO54

SUSP_LED#/GPIO55

SYSON/GPIO56

VR_ON/XCLK32K/GPIO57

AC_IN/GPIO59

PCH_VREG_EN#

EC_PECI

FSTCHG

BATT_CHG_LED#

CAPS_LED#

BATT_LOW_LED#

EN_INVPWR

SYSON

VR_ON

ACIN

PCH_VREG_EN# (20)

H_PECI (7,18)

R240 43_0402_1%

Please place R240 close to EC with in 750mil

C550 100P_0402_50V8J~D

GPO

EC_RSMRST#/GPXO03

EC_LID_OUT#/GPXO04

EC_ON/GPXO05

EC_SWI#/GPXO06

ICH_PWROK/GPXO06

BKOFF#/GPXO08

WL_OFF#/GPXO09

GPXO10

GPXO11

PCH_RSMRST#

EC_LID_OUT#

EC_ON

PCH_PWROK

BKOFF#

CPU1.5V_S3_GATE

PCH_APWROK

+VCCSA_PWRGD

PCH_RSMRST# (16)

EC_LID_OUT# (15)

EC_ON (46,54)

PCH_PWROK (7,16)

BKOFF# (33)

CPU1.5V_S3_GATE (32)

PCH_APWROK (16)

+VCCSA_PWRGD (57)

GPI

PM_SLP_S4#/GPXID1

ENBKL/GPXID2

GPXID3

GPXID4

GPXID5

GPXID6

GPXID7

PM_SLP_S4#

IGPU_BKLT_EN

EC_EAPD#

M_THERMAL#

SUSP#

PBTN_OUT#

PCIE_WAKE#

PM_SLP_S4# (16)

IGPU_BKLT_EN (16)

EC_EAPD# (41)

SUSP# (19,32,55,56)

PBTN_OUT# (6,16)

PCIE_WAKE# (16,38,39)

R1944 SHORT 0_0402_5%~D

V18R

+V18R

C283 4.7U_0603_6.3V6K~D

SM Bus

SCL1/GPIO44

SDA1/GPIO45

SCL2/GPIO46

SDA2/GPIO47

(60) EC_SMB_CK1

(60) EC_SMB_DA1

(15,22,23,41,43,46,53) EC_SMB_CK2

(15,22,23,41,43,46,53) EC_SMB_DA2

EC_SMB_CK1

EC_SMB_DA1

EC_SMB_CK2

EC_SMB_DA2

Int. K/B Matrix

KSI0/GPIO30

KSI1/GPIO31

KSI2/GPIO32

KSI3/GPIO33

KSI4/GPIO34

KSI5/GPIO35

KSI6/GPIO36

KSI7/GPIO37

KSO0/GPIO20

KSO1/GPIO21

KSO2/GPIO22

KSO3/GPIO23

KSO4/GPIO24

KSO5/GPIO25

KSO6/GPIO26

KSO7/GPIO27

KSO8/GPIO28

KSO9/GPIO29

KSO10/GPIO2A

KSO11/GPIO2B

KSO12/GPIO2C

KSO13/GPIO2D

KSO14/GPIO2E

KSO15/GPIO2F

KSO16/GPIO48

KSO17/GPIO49

(41,42) DEPOP#

DEPOP#

Item13_X01

Item3_X02

KSI0 R2599 SHORT 0_0402_5%~D KSI0_EC

KSI1 R2601 SHORT 0_0402_5%~D KSI1_EC

KSI2 R2603 SHORT 0_0402_5%~D KSI2_EC

KSI3 R2605 SHORT 0_0402_5%~D KSI3_EC

KSO4 R2600 SHORT 0_0402_5%~D KSO4_EC

KSO5 R2602 SHORT 0_0402_5%~D KSO5_EC

KSO6 R2604 SHORT 0_0402_5%~D KSO6_EC

KSO7 R2606 SHORT 0_0402_5%~D KSO7_EC

KSI4 R2607 SHORT 0_0402_5%~D KSI4_EC

KSI5 R2609 SHORT 0_0402_5%~D KSI5_EC

KSI6 R2611 SHORT 0_0402_5%~D KSI6_EC

KSI7 R2613 SHORT 0_0402_5%~D KSI7_EC

KSO8 R2608 SHORT 0_0402_5%~D KSO8_EC

KSO9 R2610 SHORT 0_0402_5%~D KSO9_EC

KSO10 R2612 SHORT 0_0402_5%~D KSO10_EC

KSO11 R2614 SHORT 0_0402_5%~D KSO11_EC

KSO0 R2615 SHORT 0_0402_5%~D KSO0_EC

KSO1 R2617 SHORT 0_0402_5%~D KSO1_EC

KSO2 R2619 SHORT 0_0402_5%~D KSO2_EC

KSO3 R2621 SHORT 0_0402_5%~D KSO3_EC

KSO12 R2616 SHORT 0_0402_5%~D KSO12_EC

KSO13 R2618 SHORT 0_0402_5%~D KSO13_EC

KSO14 R2620 SHORT 0_0402_5%~D KSO14_EC

KSO15 R2622 SHORT 0_0402_5%~D KSO15_EC

KSO16 R2537 SHORT 0_0402_5%~D KSO16_EC

Item2_X01

ODD_EJECT (45)

EN_WOL# (39)

HDA_SDO (14)

LID_SW_IN# (15,48,49)

Item2_X03

BKOFF# R217 10K_0402_5%~D

EC_SCI# R218 10K_0402_5%~D

M_THERMAL# R1943 10K_0402_5%~D

EC_SMB_CK2 R244 2.2K_0402_5%~D

EC_SMB_DA2 R247 2.2K_0402_5%~D

Item6_X01

Item8_X02

(16,48) PM_SLP_S3#

(16,48) PM_SLP_S5#

(18) EC_SMI#

(52) PS_ID

R249 SHORT 0_0402_5%~D PM_SLP_S3#_R

R250 SHORT 0_0402_5%~D PM_SLP_S5#_R

EC_SMI#

PS_ID

EC_ESB_CLK_R R252 SHORT 0_0402_5%~D EC_ESB_CLK_R

EC_ESB_DAT

(16) SUSPWRDNACK

(33) EC_INV_PWM

(43) SYSTEM_FAN_FB

(32) PCH_PWR_EN

(38) EC_TX

(38) EC_RX

(46) KB_DET#

(44) USB_PWR_EN#

SUSPWRDNACK

SYSTEM_FAN_FB

PCH_PWR_EN

EC_TX

EC_RX

ON/OFF

KB_DET#

USB_PWR_EN#

Item6_X01

PM_SLP_S3#/GPIO04

PM_SLP_S5#/GPIO07

EC_SMI#/GPIO08

LID_SW#/GPIO0A

SUSP#/GPIO0B

PBTN_OUT#/GPIO0C

EC_PME#/GPIO0D

EC_THERM#/GPIO11

FAN_SPEED1/FANFB1/GPIO14

FANFB2/GPIO15

EC_TX/GPIO16

EC_RX/GPIO17

ON_OFF/GPIO18

PWR_LED#/GPIO19

NUMLED#/GPIO1A

EC test PSID

XCLK1

XCLK0

(16) SUSCLK_R

Item3_X02

R253 SHORT 0_0402_5%~D

EC_CRY1 122

EC_CRY2 123

R1979 100K_0402_5%~D

C1947 20P_0402_50V8J~D

KB930QF A1 LQFP 128P

20mil

<BOM Structure>

L44 FBMA-L1_0603

ECAGND

GND GND GND GND AGND

11 24 35 34 113 69

Board ID

+3VALW_EC

Ra

R219 100K_0402_5%~D

AD_BID0

Item5_X01

Rb

R225 100K_0402_5%~D

C283 0.1U_0402_16V7K~D

Analog Board ID definition, Please see page 4.

+3VS

+5VS

Item11_X01

R2626 4.7K_0402_5%~D TP_CLK

R2627 4.7K_0402_5%~D TP_DATA

R223 4.7K_0402_5%~D

R224 4.7K_0402_5%~D

X1

EC_CRY1

EC_CRY2

32.768KHZ_12.5PF_9H03200019

C287 27P_0402_50V8J~D

C288 27P_0402_50V8J~D

R_SPI_CLK CH100 10P_0402_50V8J~D

EC_ESB_CLK_R CH101 10P_0402_50V8J~D

Reserve for RF please close to U34

(52,59) VR_HOT#

Item3_X02

R265 0_0402_5%~D

C1943 0.1U_0402_16V7K~D

U635

(7) H_PROCHOT#

H_PROCHOT#

H_PROCHOT#_EC

SN74LVC1G06DCKR_SC70-5

C1944 47P_0402_50V8J~D

R1999 100K_0402_5%~D

near POWER item

SPI ROM 128KB

+3VALW_EC

C297 0.1U_0402_16V7K~D

20mils

U36

VCC VSS W HOLD S C D O

MX25L1006EMI-10G SOP 8P

FSEL# R258 SHORT 0_0402_5%~D SPI_FSEL#

SPI_CLK R259 SHORT 0_0402_5%~D SPI_CLK_R

FWR# R260 SHORT 0_0402_5%~D SPI_FWR#

SPI_CLK_R R257 @ 33_0402_5%~D C296 @ 22P_0402_50V8J~D

Reserve for EMI please close to U36

SPI_SO R261 SHORT 0_0402_5%~D FRD#

SP07000F500 S SOCKET WIESON G6179-100000

8P SPIFLASH

WIESO_G6179-100000_8P

U620

EC_ESB_CLK

(53) CP_SEL

RST#

EC_ESB_DAT

(53) EMC_ALERT#

(52) Dyn_Turbo_Sel

Dyn Turbo Sel

(7) DRAMRST_CNTRL_EC

(16,33) PCH_ENVDD

ESB_CLK GPIO00 RST# ESB_DAT GPIO01 GPIO02 GPIO03 GPIO04 GPIO05 GPIO06 GPIO07/CAS_CLK GND

TEST_EN# GPIO08/CAS_DAT GPIO09 GPIO0A GPIO0B GPIO0C/PWM0 GPIO0D/PWM1 GPIO0E/PWM2 GPIO0F/PWM3 GPIO10/ESB_RUN# GPIO11/BaseAddOpt GND VCC

EC_ENVDD (33)

PWRSHARE_OE#

PWRSHARE_OE# (43)

WLES ON/OFF LED# (49)

EN_TPLED# (49)

LCD_TEST (33)

3V_F347_ON (48)

+3VALW_EC

60 mil

KC3810_QFN24_4X4

R248 47K_0402_5%~D

RST#

C292 0.1U_0402_16V7K~D

C294 0.1U_0402_16V7K~D

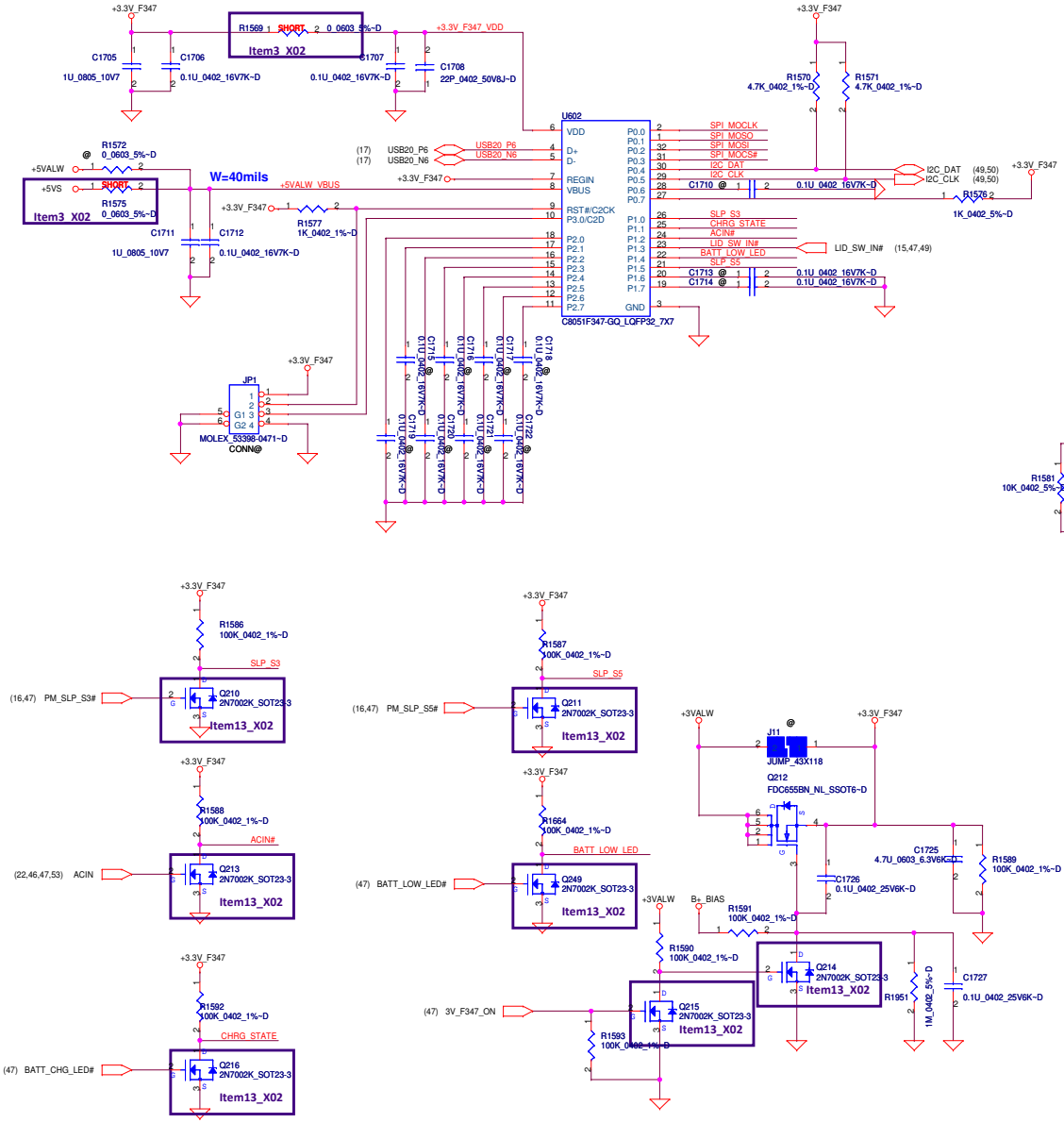
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: EC ENE-KB930/ ENE3810

Size: | Document Number: LA-8381P | Rev: 1.0

Date: Thursday, January 12, 2012 | Sheet 47 of 63



+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

AC mode battery full in S5:turn off ELC controller

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

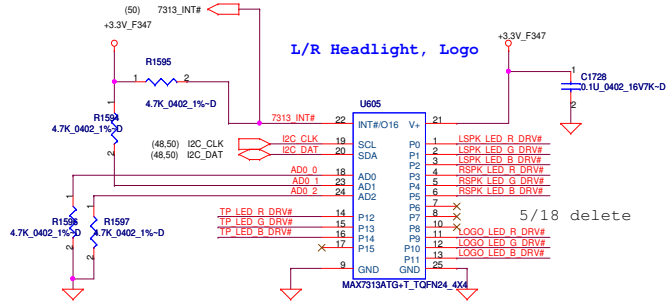
Compal Electronics, Inc.

Title: ELC (1)/STATUS CONN

Size	Document Number	Rev
	LA-8381P	1.0

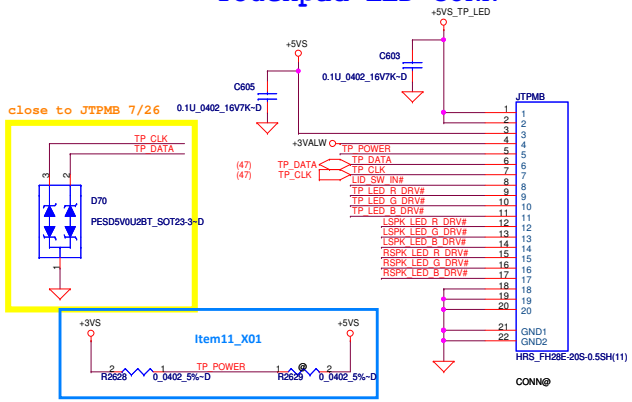
Date: Thursday, January 12, 2012 | Sheet 48 of 63

L/R Headlight, Logo

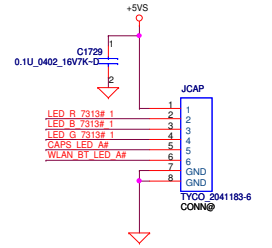


5/18 delete

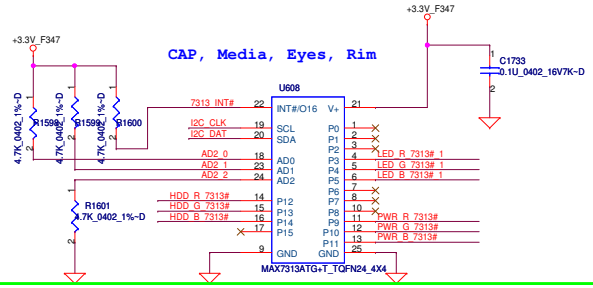
Touchpad LED CONN



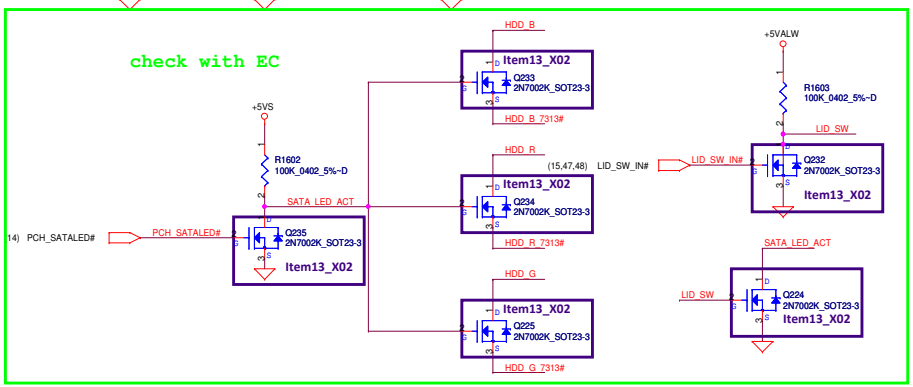
Indicator CONN

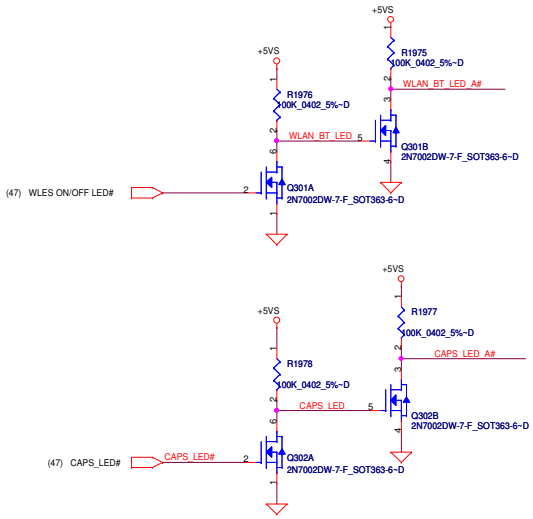


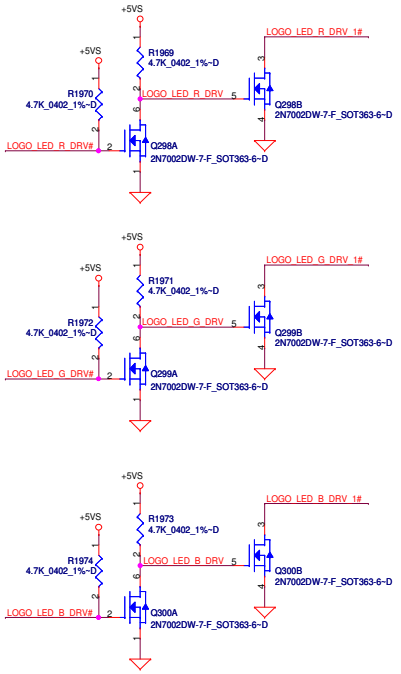
CAP, Media, Eyes, Rim



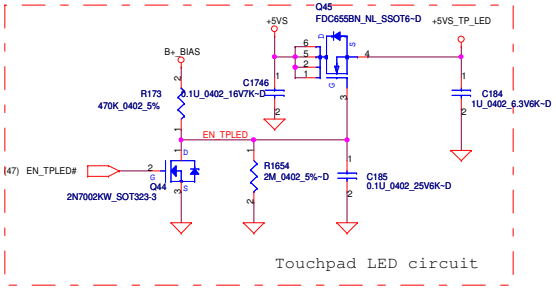
check with EC





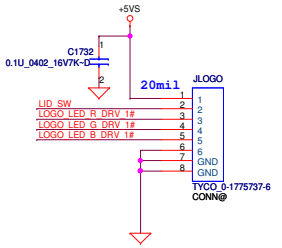


Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight , Logo, TP
U608	0	1	1	Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim

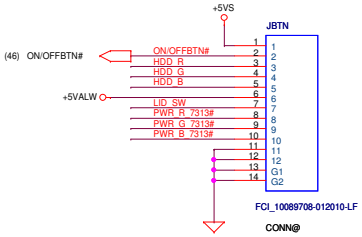


Touchpad LED circuit

LOGO Board CONN



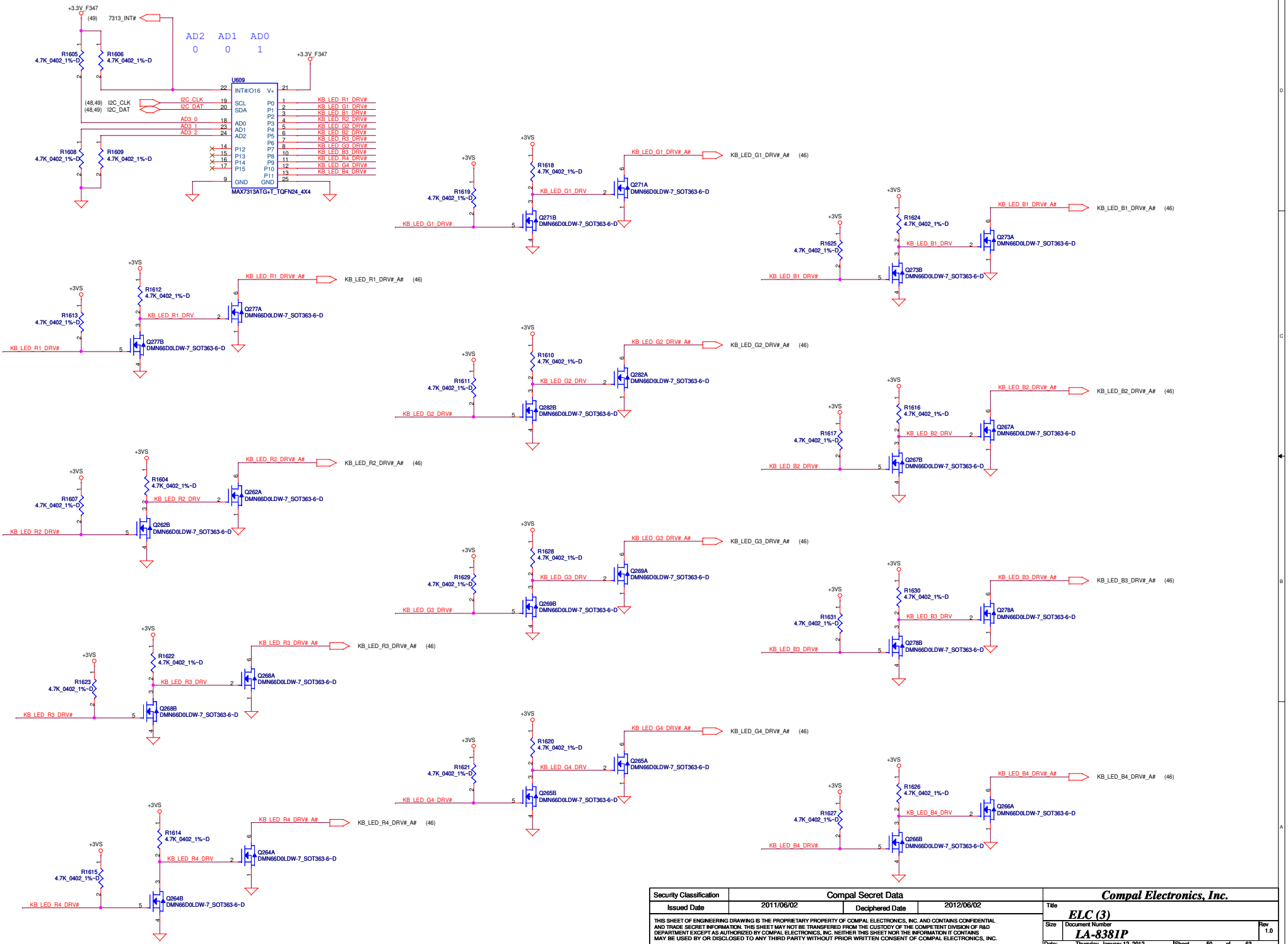
PWR BTN Board CONN



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: ELC (2)			
Size	Document Number: LA-8381P		Rev: 1.0
Date: Thursday, January 12, 2012	Sheet 49 of 63		

K/B Backlight



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

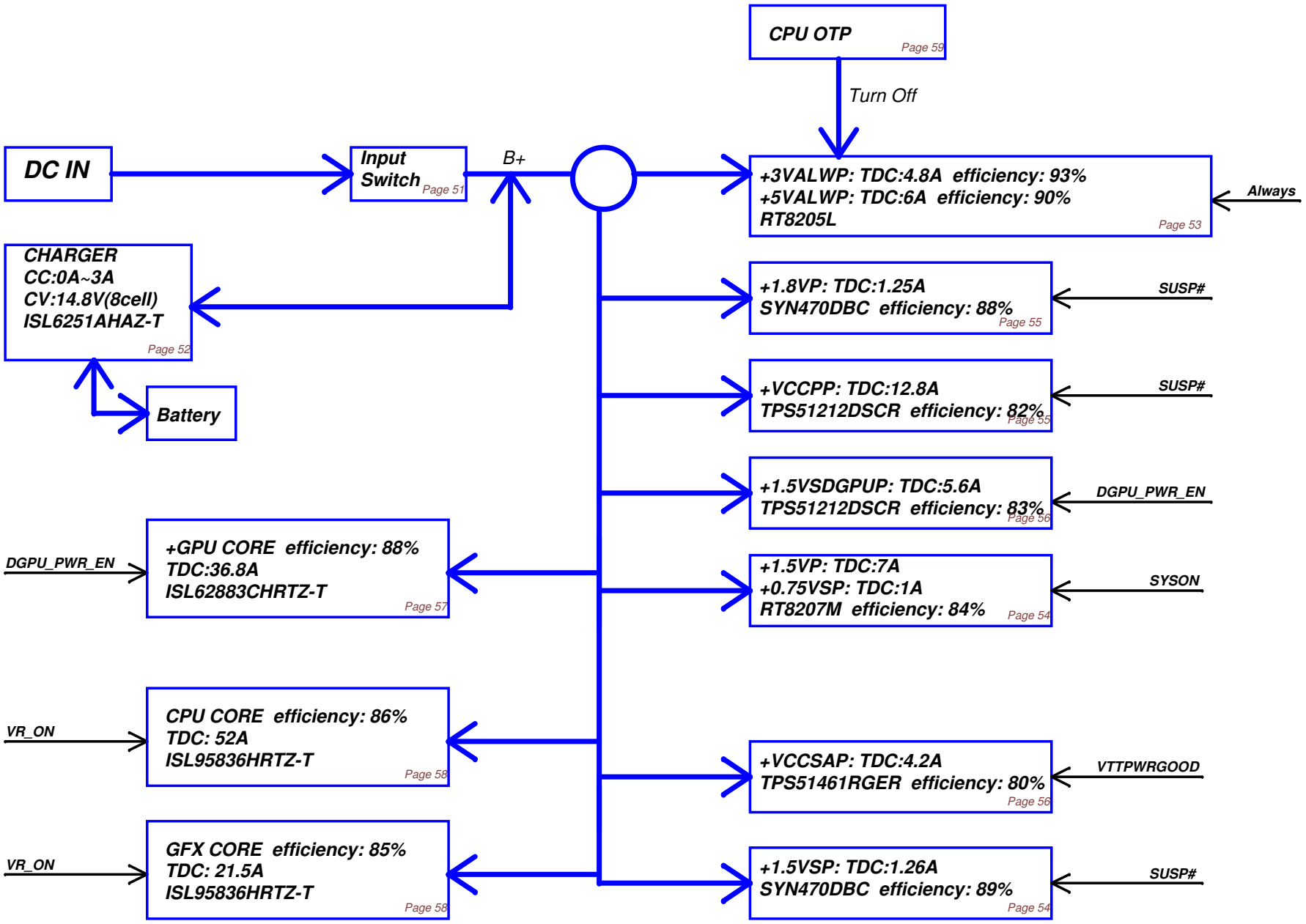
Compal Electronics, Inc.

Title: ELC (3)

Size	Document Number	Rev
	LA-8381P	1.0

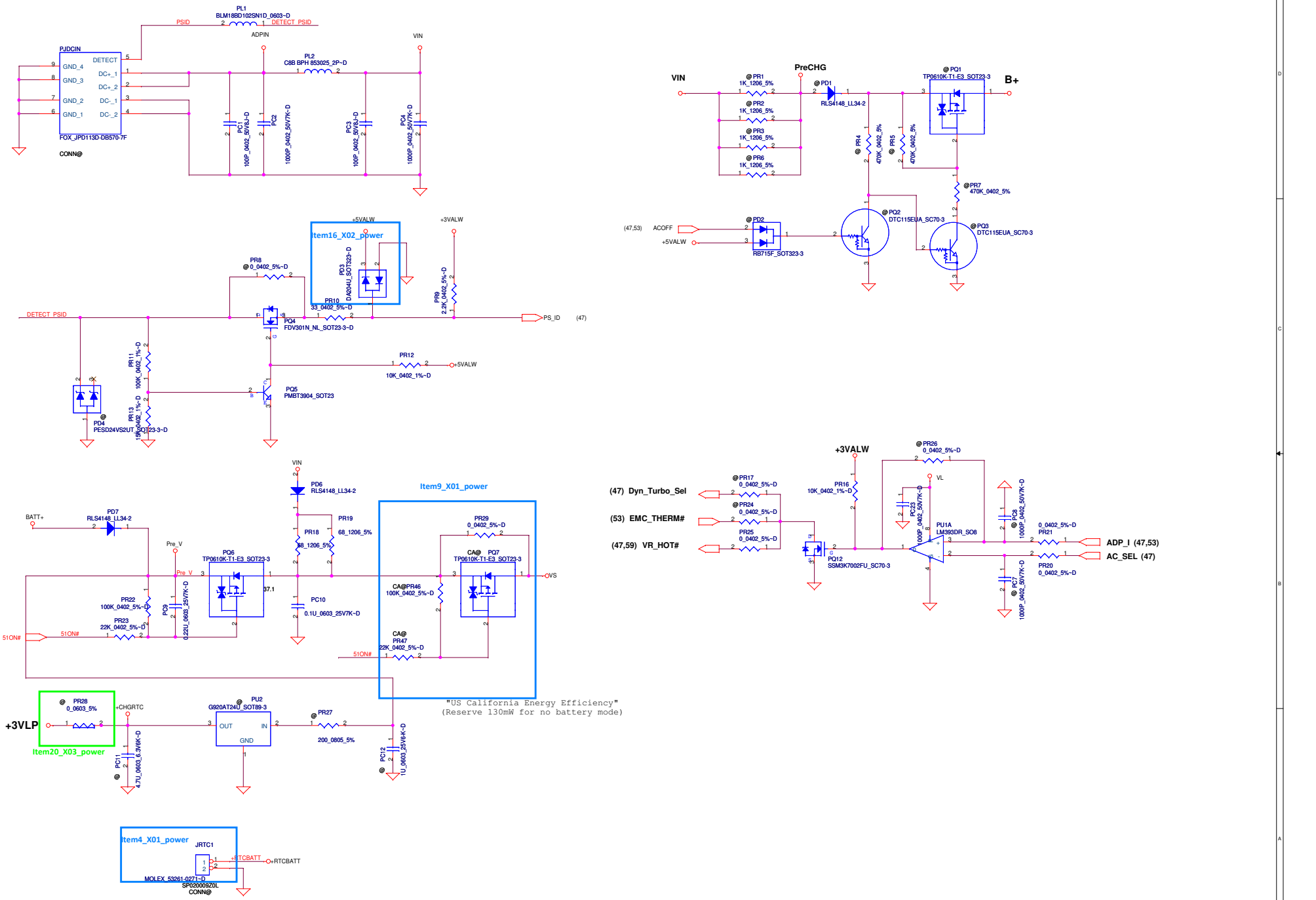
Date: Thursday, January 12, 2012 Sheet 50 of 63

Power block



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	POWER BLOCK DIAGRAM		
Size: Custom	Document Number: LA-6801P		Rev: 1.0
Date: Thursday, January 12, 2012	Sheet 51 of 63		



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 | Sheet 52 of 63

Iada=0~7.693A(150W/19.5V=7.693A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 6.92A

CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
Vaclim=2.39*((6.98K//152K)/((11.5K//152K)+(6.98K//152K)))

CC=3.3A

IREF=1*Icharge

IREF=0.25V~3.3V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

del 01/25
customer assent

slave address : 0101101
please placemnet near R-sense

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

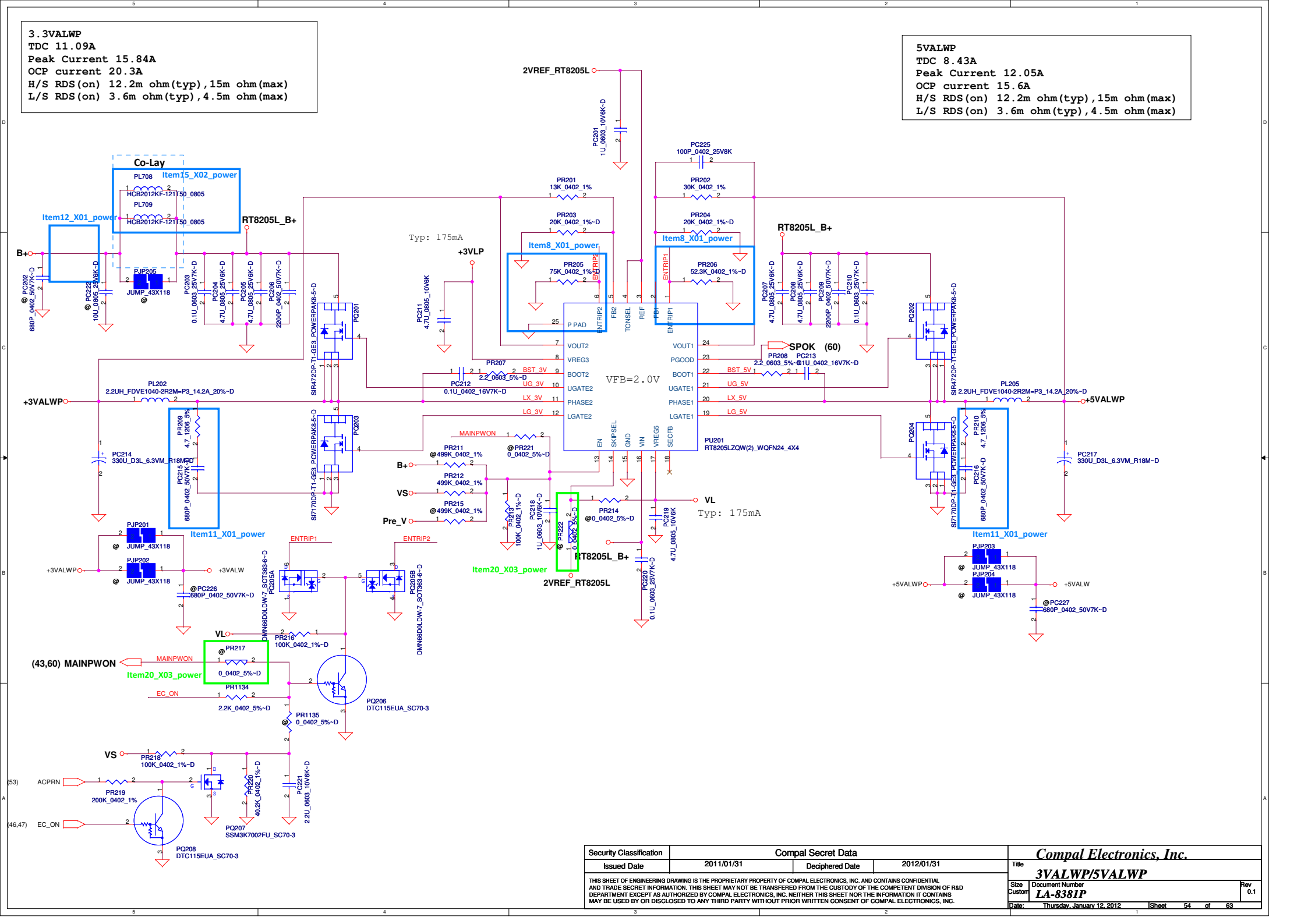
Title: PWR-CHARGER

Size: Custom | Document Number: LA-8381P | Rev: 1.0

Date: Thursday, January 12, 2012 | Sheet 53 of 63

3.3VALWP
TDC 11.09A
Peak Current 15.84A
OCP current 20.3A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 3.6m ohm(typ),4.5m ohm(max)

5VALWP
TDC 8.43A
Peak Current 12.05A
OCP current 15.6A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 3.6m ohm(typ),4.5m ohm(max)



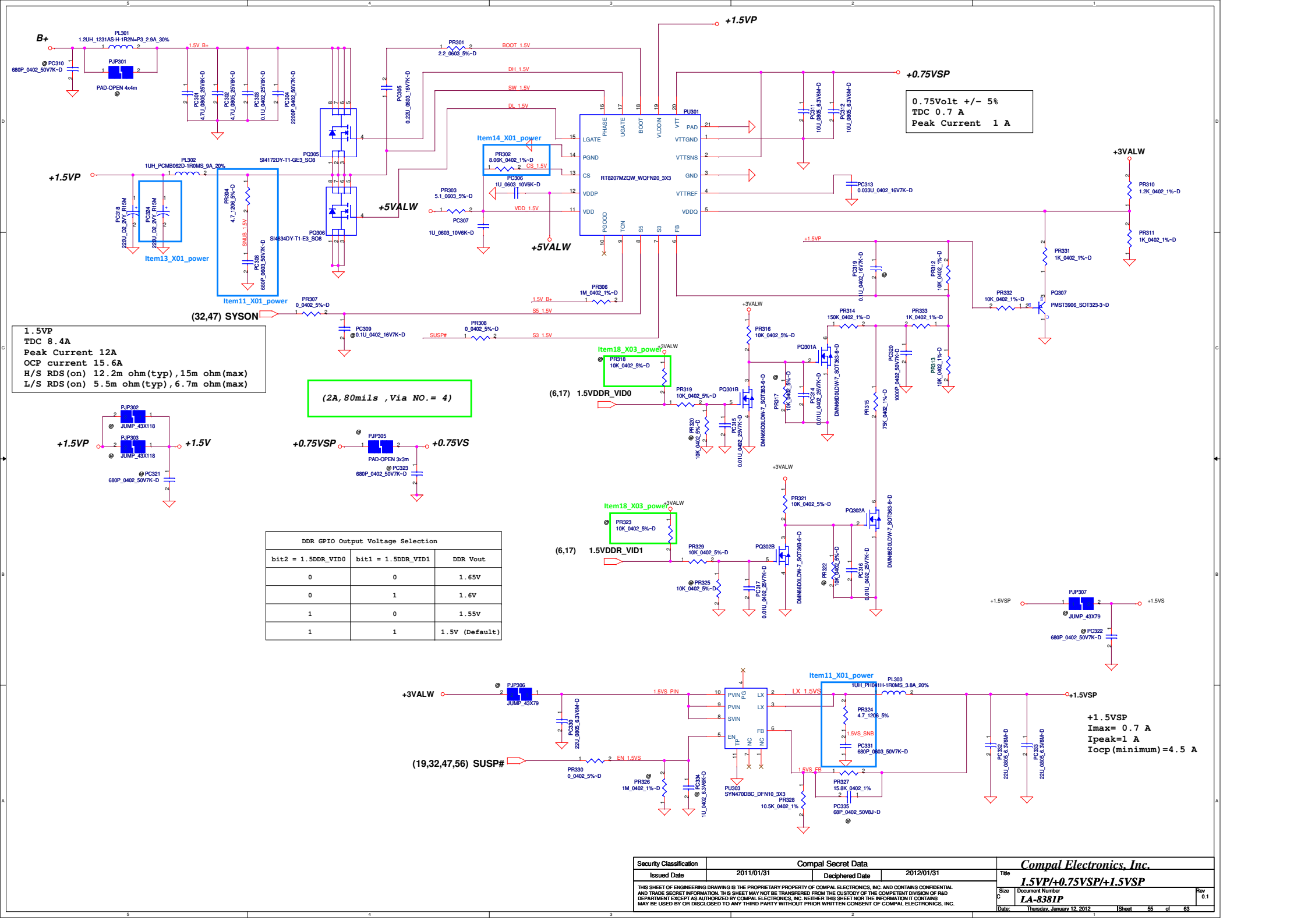
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA-8381P	0.1

Date: Thursday, January 12, 2012 Sheet 54 of 63



DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

Compal Electronics, Inc.

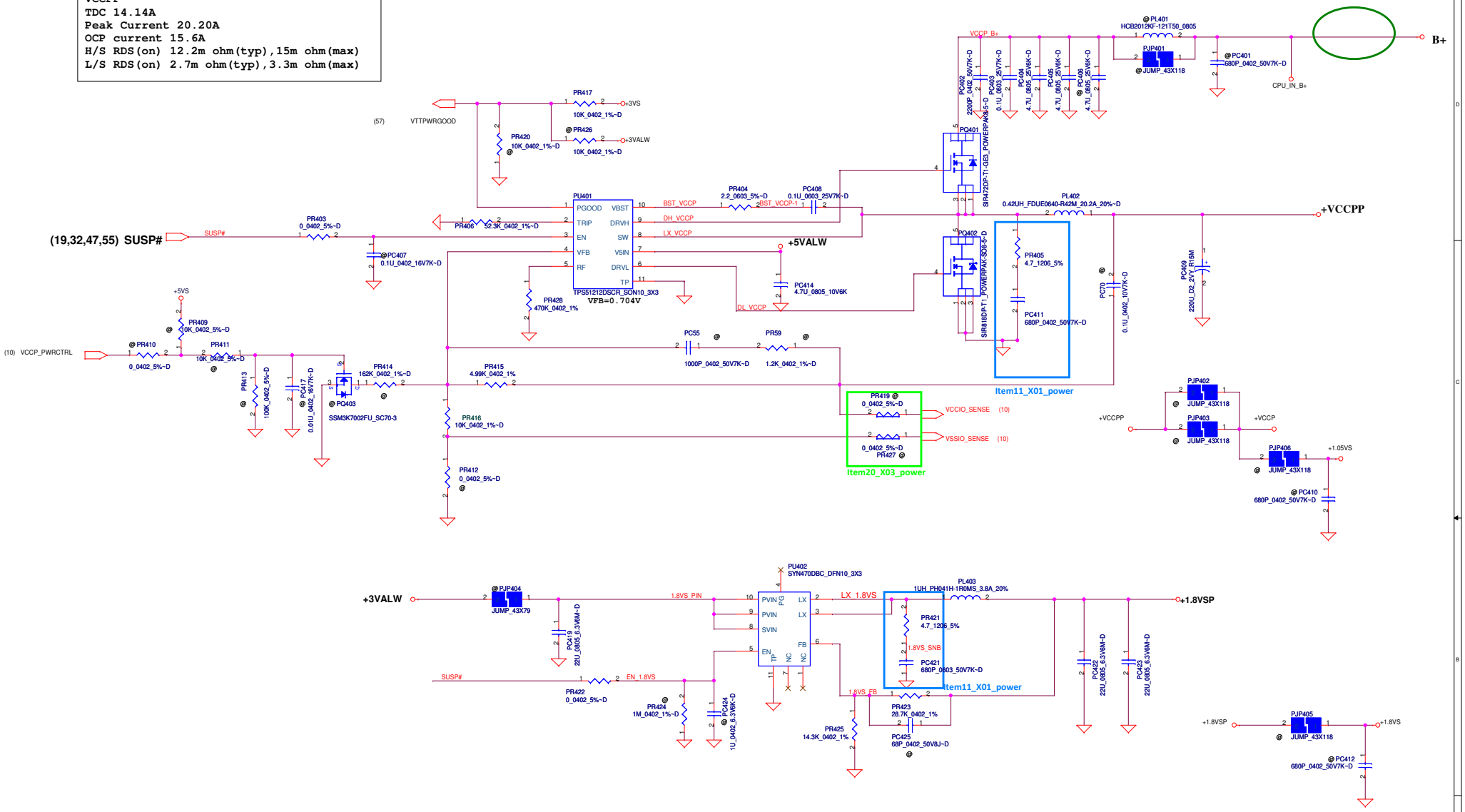
Title: 1.5VP/+0.75VSP/+1.5VSP

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 | Sheet 55 of 63

VCCPP
TDC 14.14A
Peak Current 20.20A
OCP current 15.6A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S RDS(on) 2.7m ohm(typ),3.3m ohm(max)

Due to remove VENTURA fun,
so delete PR401.



1.8VSP
TDC 1.08 A
Peak Current 1.55 A
OCP current 4.5 A

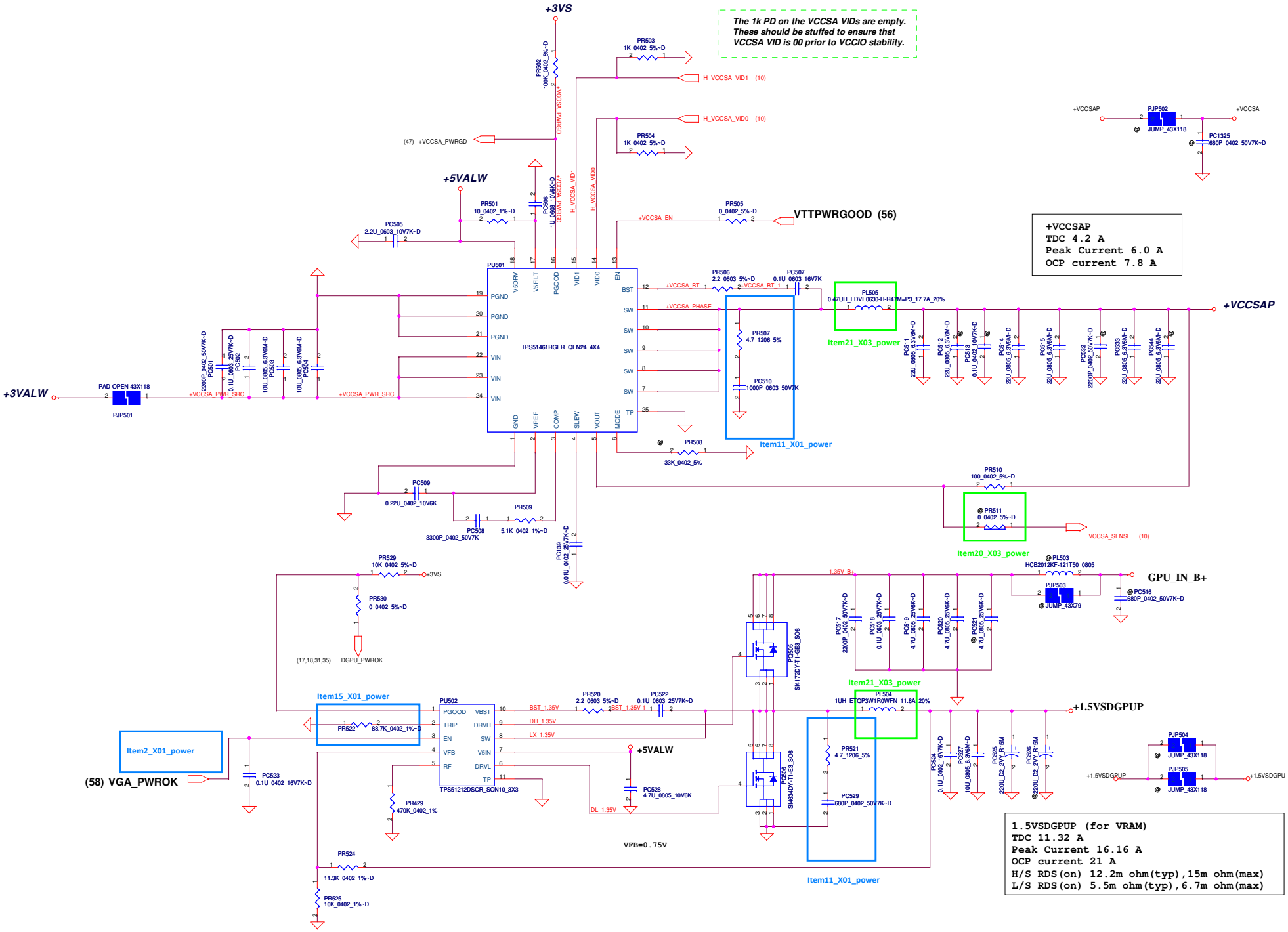
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR+VCCPP/+1.8VSP

Size	Document Number	Rev
C	LA-8381P	1.0

Date: Thursday, January 12, 2012 Sheet 56 of 63



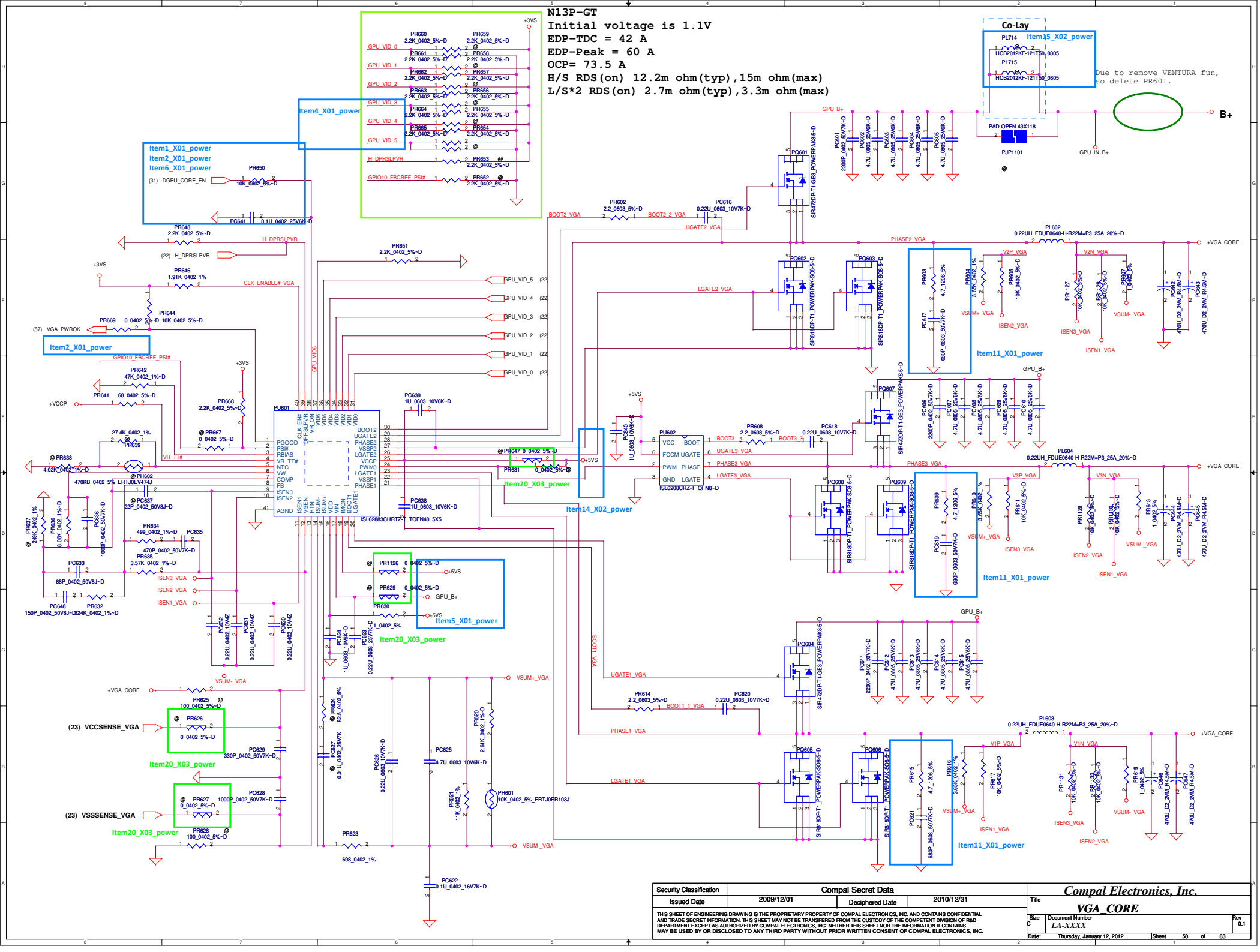
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.

Title: PWR-+VCCSAP/+1.5VSDGPUP

Size	Document Number	Rev
C	LA-8381P	0.1

Date: Thursday, January 12, 2012 | Sheet 57 of 63


N13P-GT
Initial voltage is 1.1V
EDP-TDC = 42 A
EDP-Peak = 60 A
OCP= 73.5 A
H/S RDS(on) 12.2m ohm(typ),15m ohm(max)
L/S*2 RDS(on) 2.7m ohm(typ),3.3m ohm(max)
Co-Lay
Due to remove VENTURA fun, so delete PR601.
B+
+VGA_CORE
PU601
ISL62883CHRTZ-T_TQFN40_5X5
PU602
ISL6208CRZ-T_QFN8-D
Item1_X01_power
Item2_X01_power
Item4_X01_power
Item5_X01_power
Item6_X01_power
Item11_X01_power
Item14_X02_power
Item15_X02_power
Item20_X03_power
(23) VCCSENSE_VGA
(23) VSSSENSE_VGA
Security Classification
Compal Secret Data
Issued Date
2009/12/01
Deciphered Date
2010/12/31
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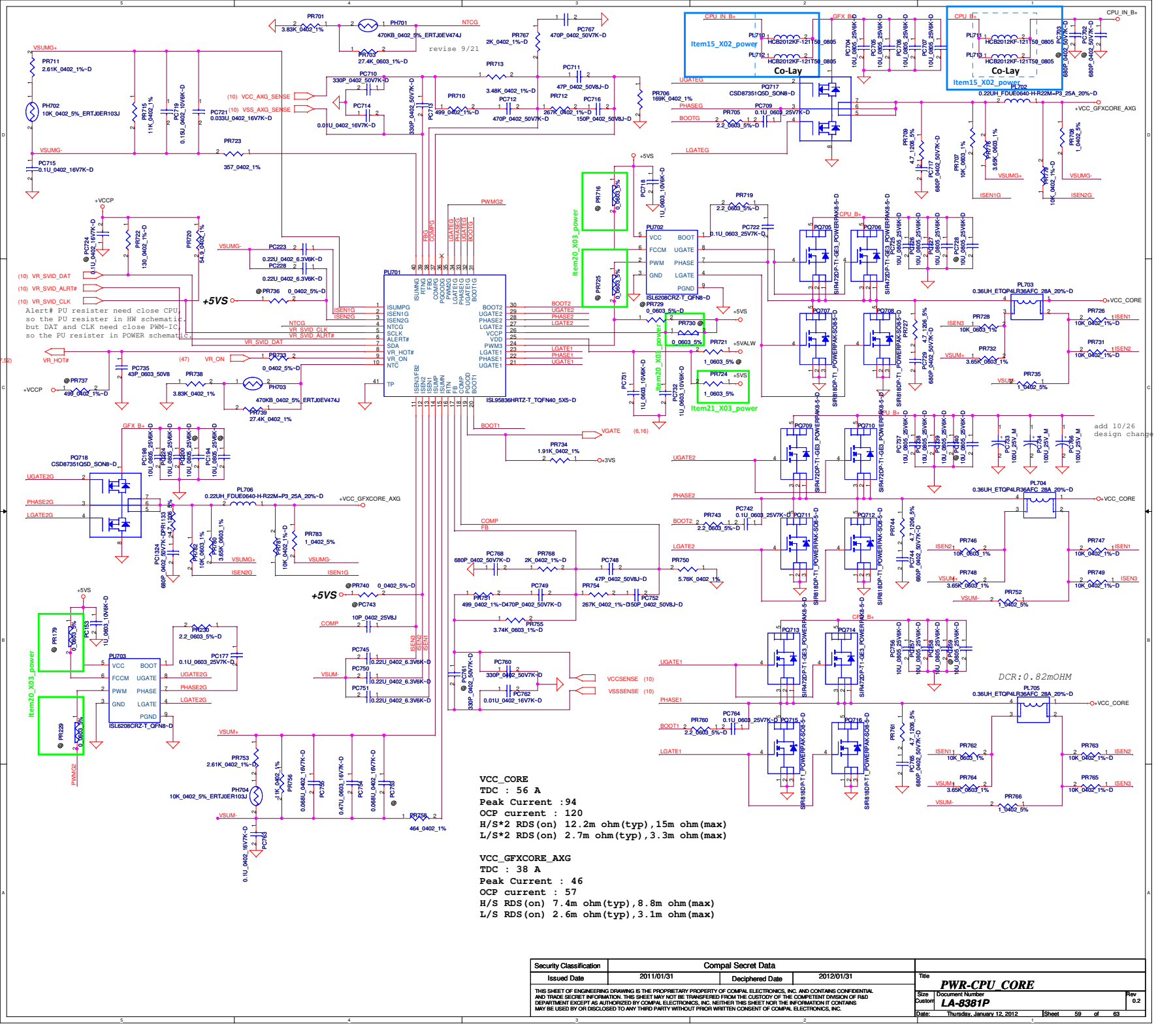
Compal Electronics, Inc.
Title
VGA_CORE
Size
C
Document Number
LA-XXXX
Rev
0.1
Date:
Thursday, January 12, 2012
Sheet
58
of
63



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

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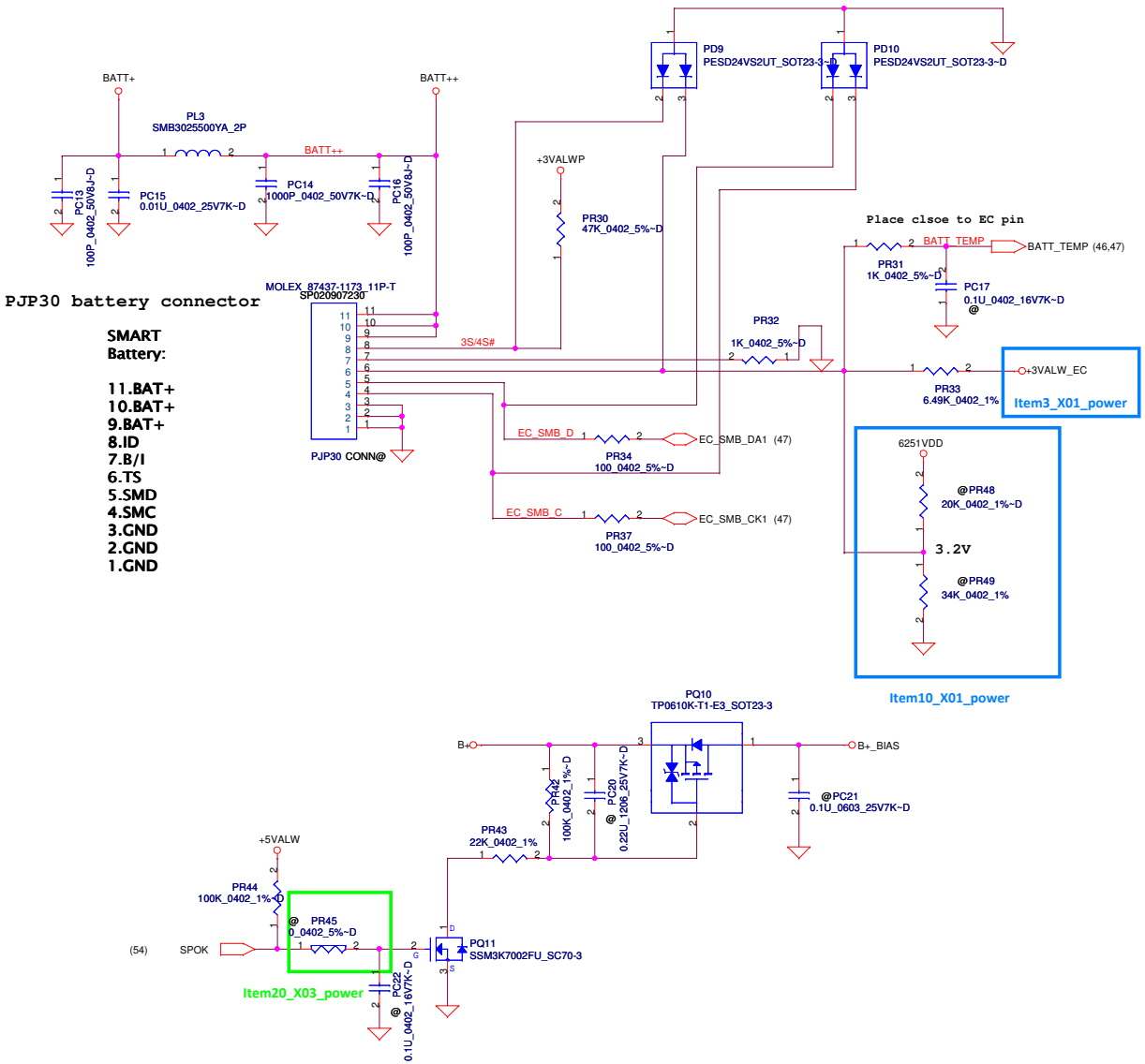
Title	PWR-CPU_CORE		
Size	Document Number		Rev
Custom	LA-8381P		0.2
Date:	Thursday, January 12, 2012	Sheet	59 of 63

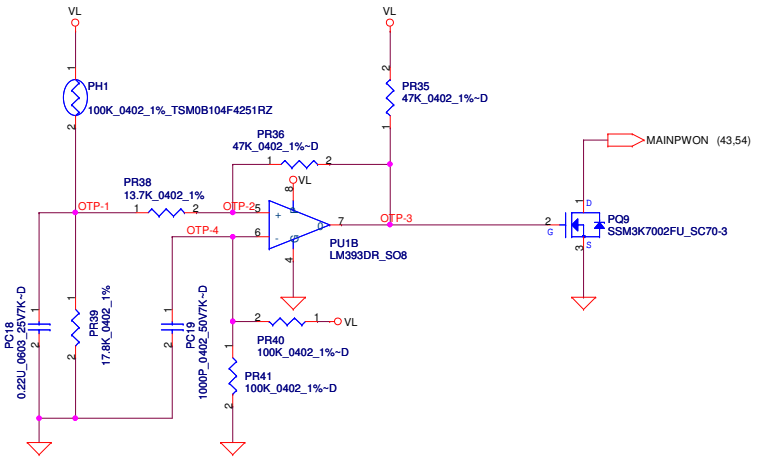


Battery Connect/OTP

PH1 under CPU botten side :

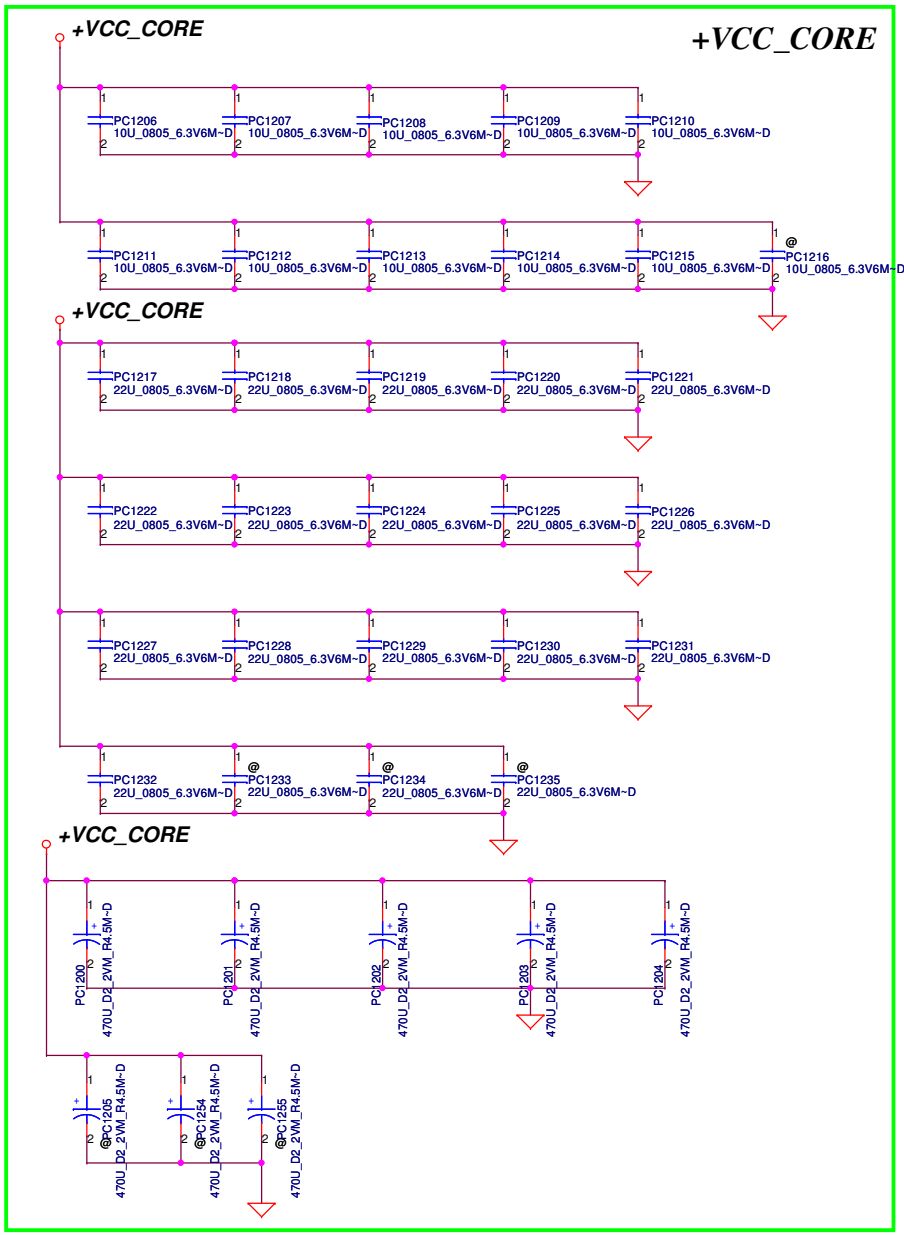
CPU thermal protection at 90 degree C

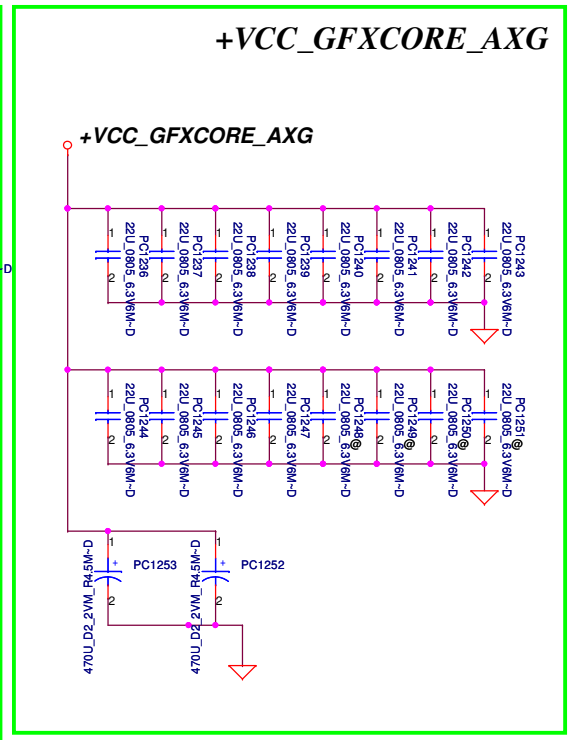
Recovery at 50 degree C

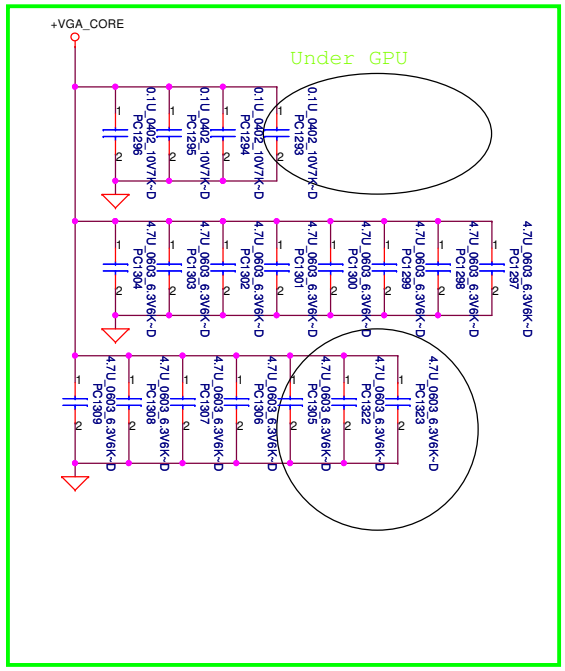


Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/01/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size: Custom	Document Number: LA-8381P		Rev: 0.1
Date: Thursday, January 12, 2012	Sheet 60 of 63		

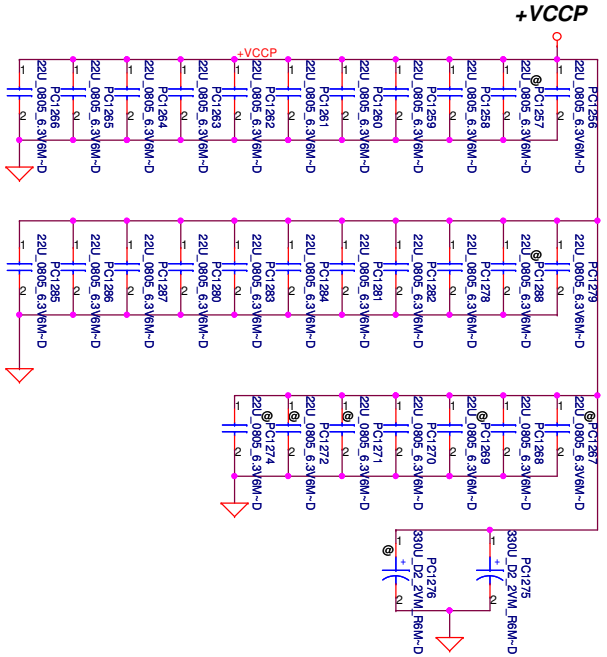


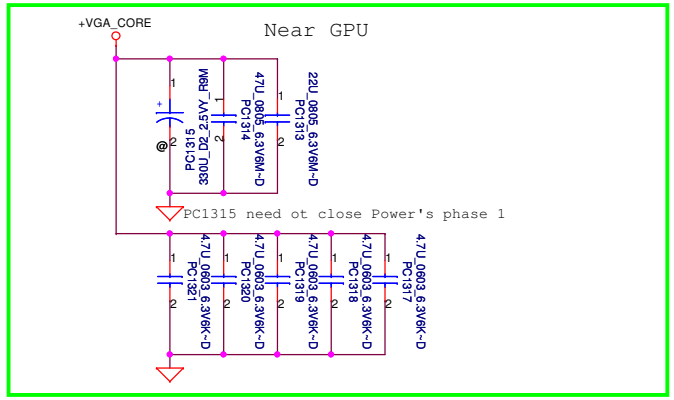




Below is 458544_CRV_PDDG_0.8 Table 5-6.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites





Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-8381P	0.1

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	61	PROCESSOR DECOUPLIN	11/09/9	COMPAL	Based on NVIDA check data to reduce VGA cap Q'ty	Remove PC1290~PC1293, PC1310,PC1312, PC1316.	0.1
2	55					Add PC1322, PC1323	0.1
3	58	+VGA_CORE	11/09/9	COMPAL	EE request	Add H_DPRSLPVR module port	0.1
4	51						
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Title: PWR-PIR

Size | Document Number | Rev 0.1

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Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: HW-PIR

Size	Document Number	Rev
		1.0

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