MS-7846

mATX
Ver: 1.0

Intel Sharkbay plamform H81 COLAY B85

CPU:

INTEL-Haswell LGA1150

System Chipset:

H81,B85,H87

Memory:

*DDRIII (1333/1666MHz) * 2 (Dual Channel)*

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL892 Colay 887

LAN-realtek8111G

SIO:NUVOTON 6779D

SPI ROM: 64 MB & 128MB

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 1*
*PCI Slot * 2*

Other:

*VGA*1*
*SATA2*2*
*SATA3*2*
*FRONT USB2.0 *4*
*FRONT USB3.0 *2*
*REAL USB2.0 *2*
*REAL USB3.0 *2*
*PS2*1*
*COM PORT*2 1F/1R*
*PRINT PORT*1 1R*

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Custom	Cover Sheet	1.0

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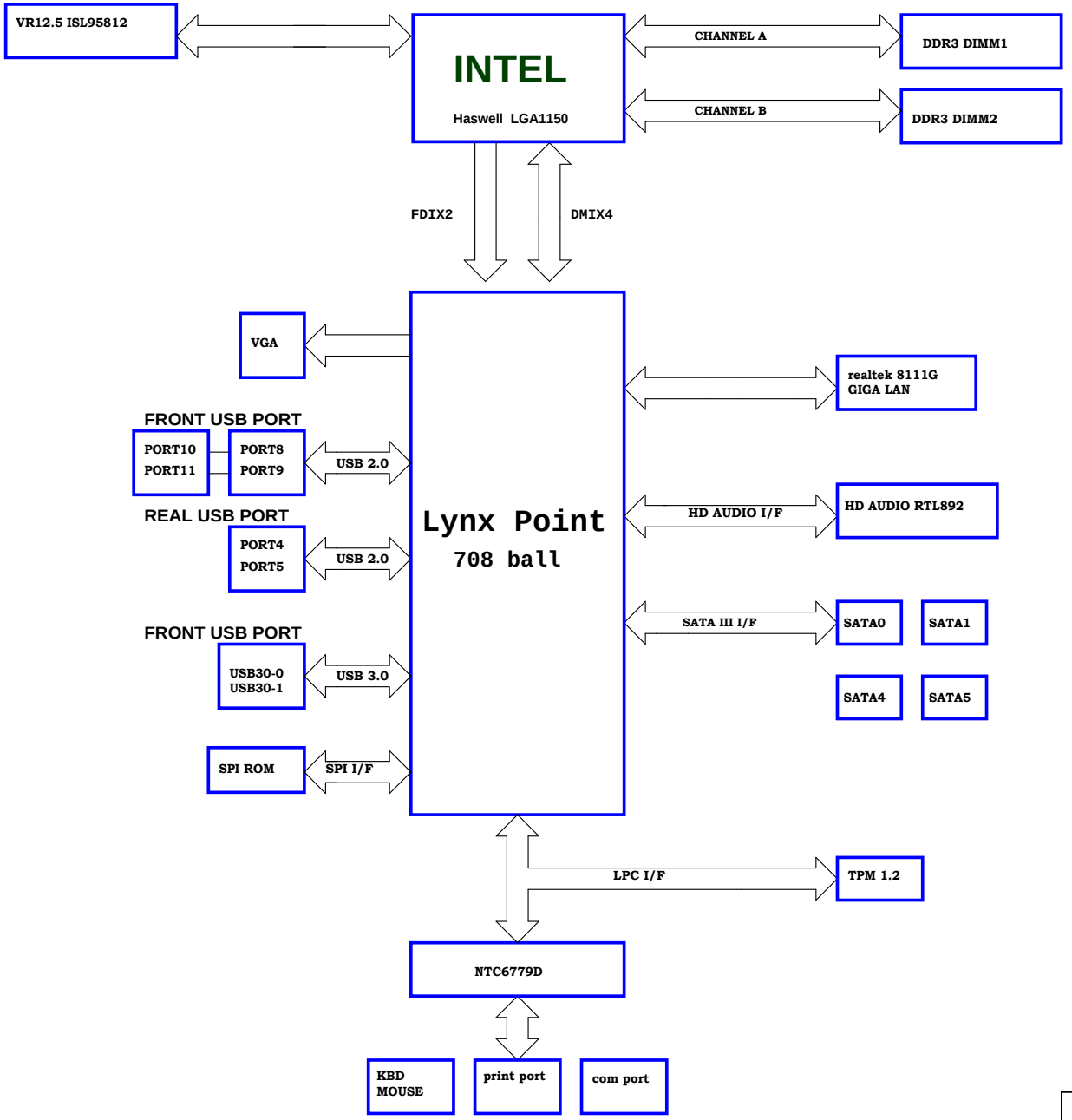
MS-7846 Block Diagram



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7846	
Size: Custom	Document Description: Block Diagram	Rev: 1.0
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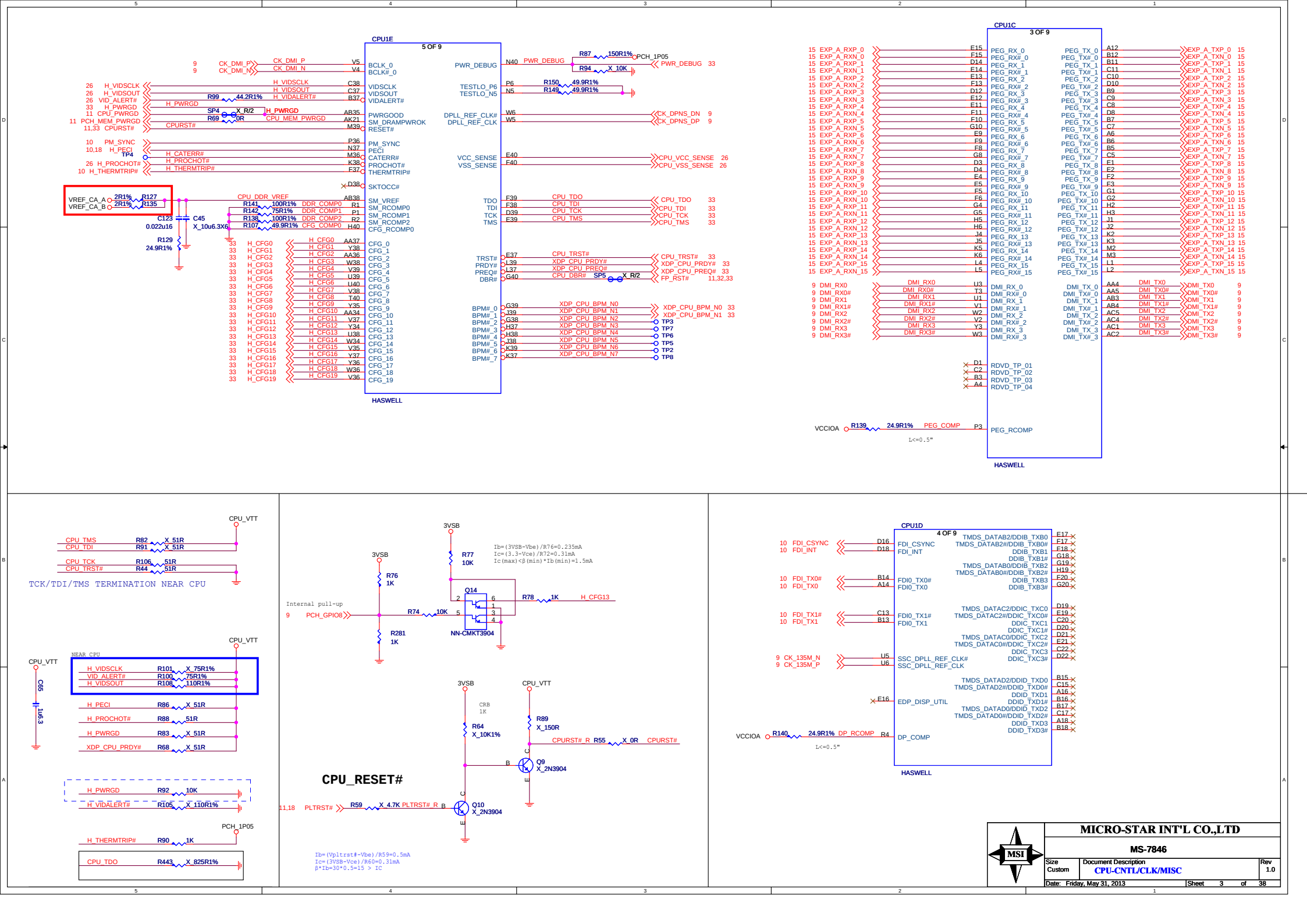
CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
HASWELL
CPU1D
4 OF 9
HASWELL
TCK/TDI/TMS TERMINATION NEAR CPU
CPU_RESET#
MICRO-STAR INT'L CO.,LTD
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CPU-CNTL/CLK/MISC
Size Custom
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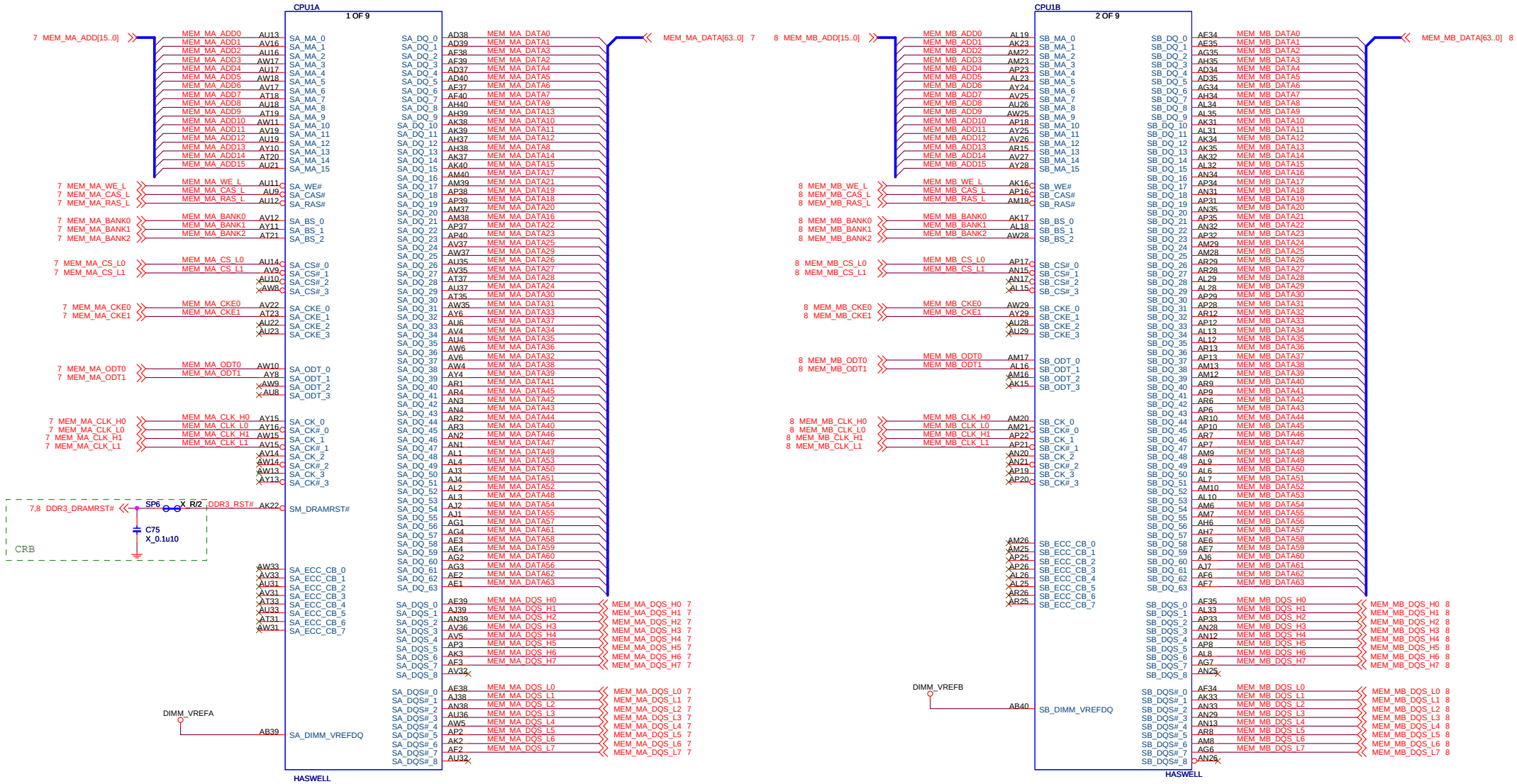

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-Memory	Rev: 1.0
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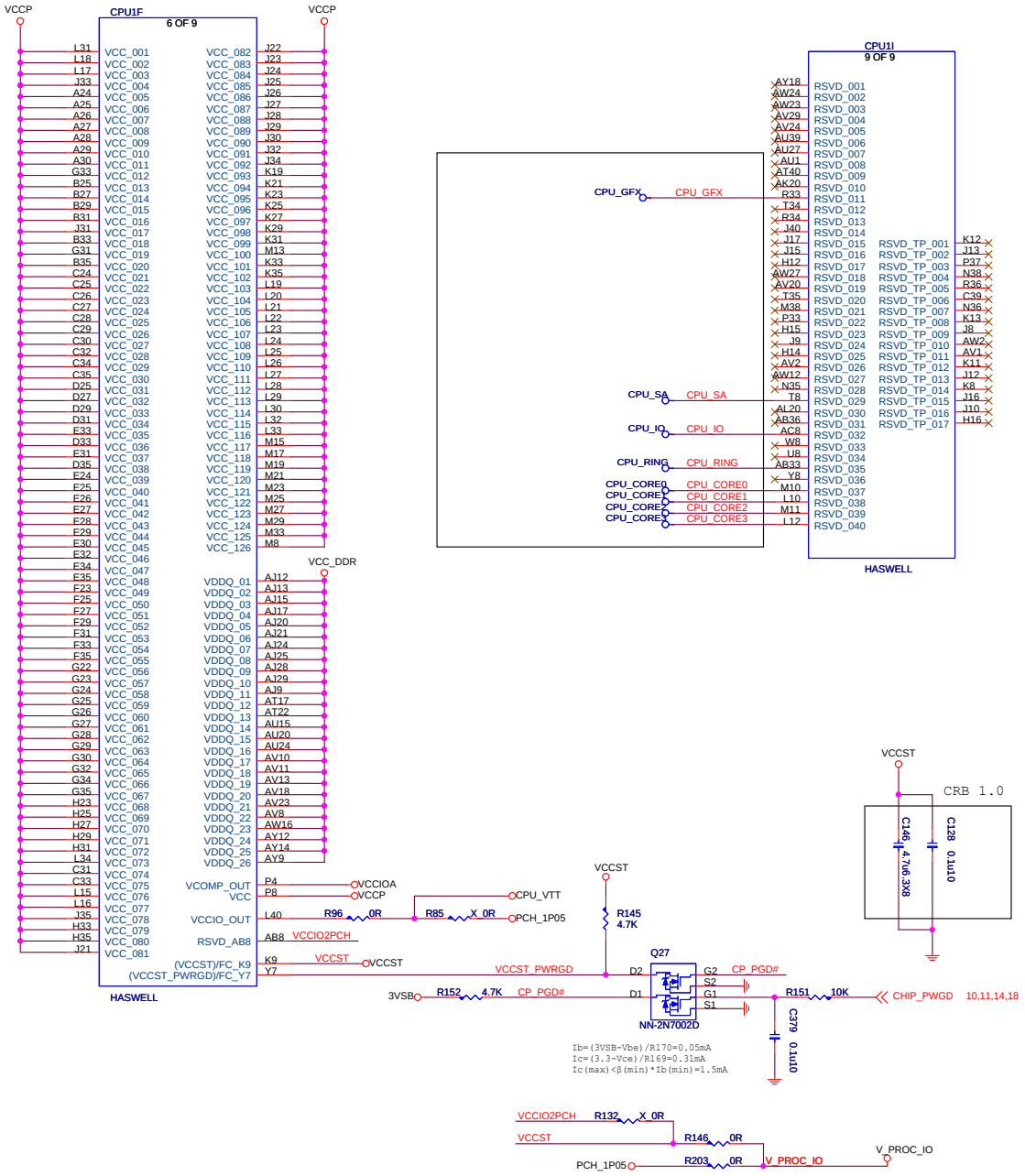
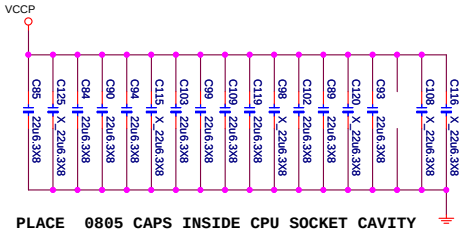
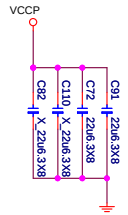


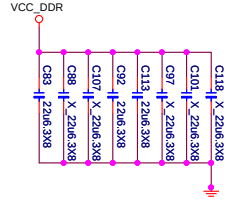
+CPU_VCCP-Decoupling



PLACE 0805 CAPS Near CPU SOCKET edge



+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS

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MS-7846		
Size: Custom	Document Description: CPU-Power	Rev: 1.0
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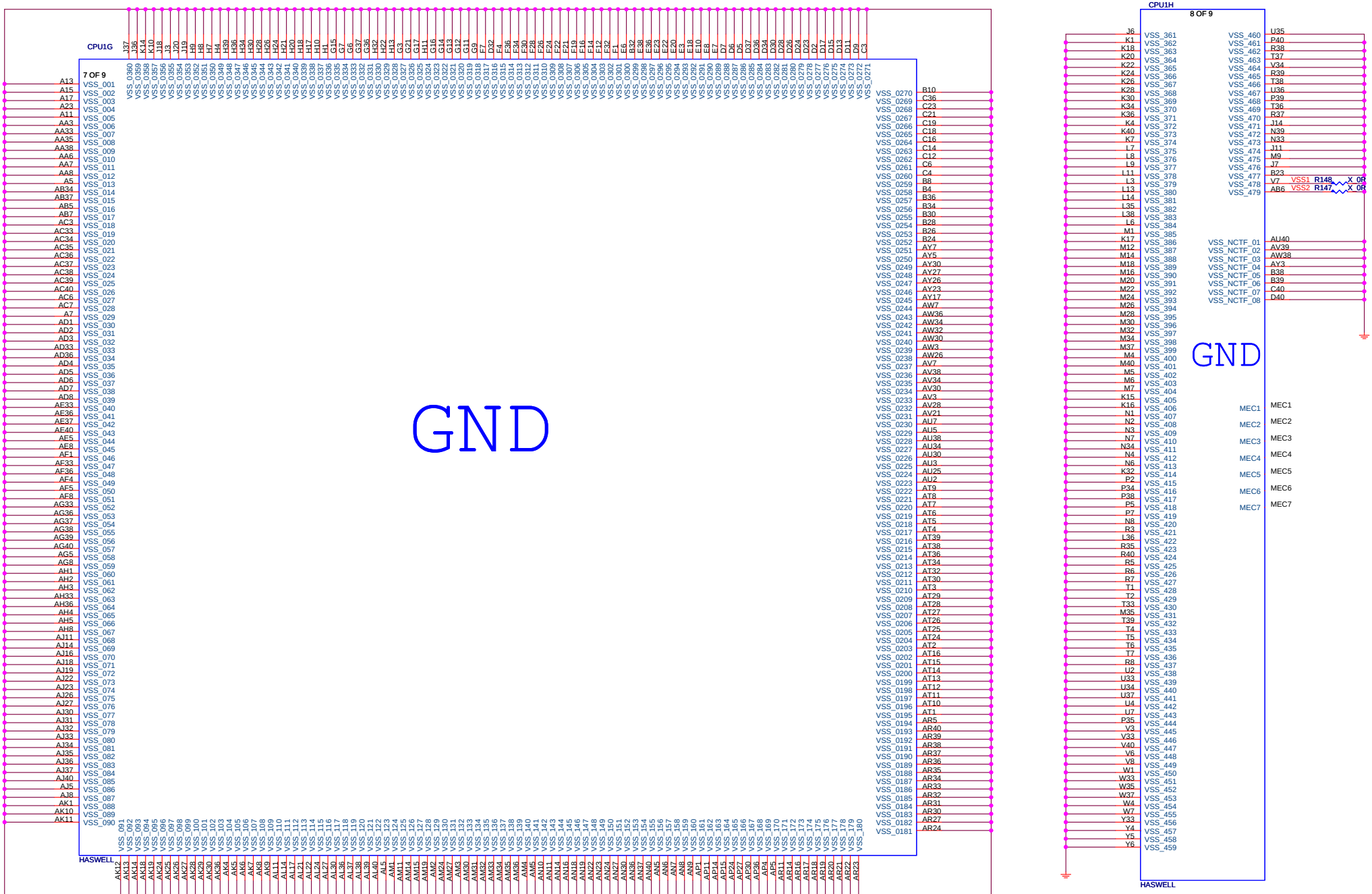

MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size: Custom	Document Description: CPU-GND	Rev: 1.0
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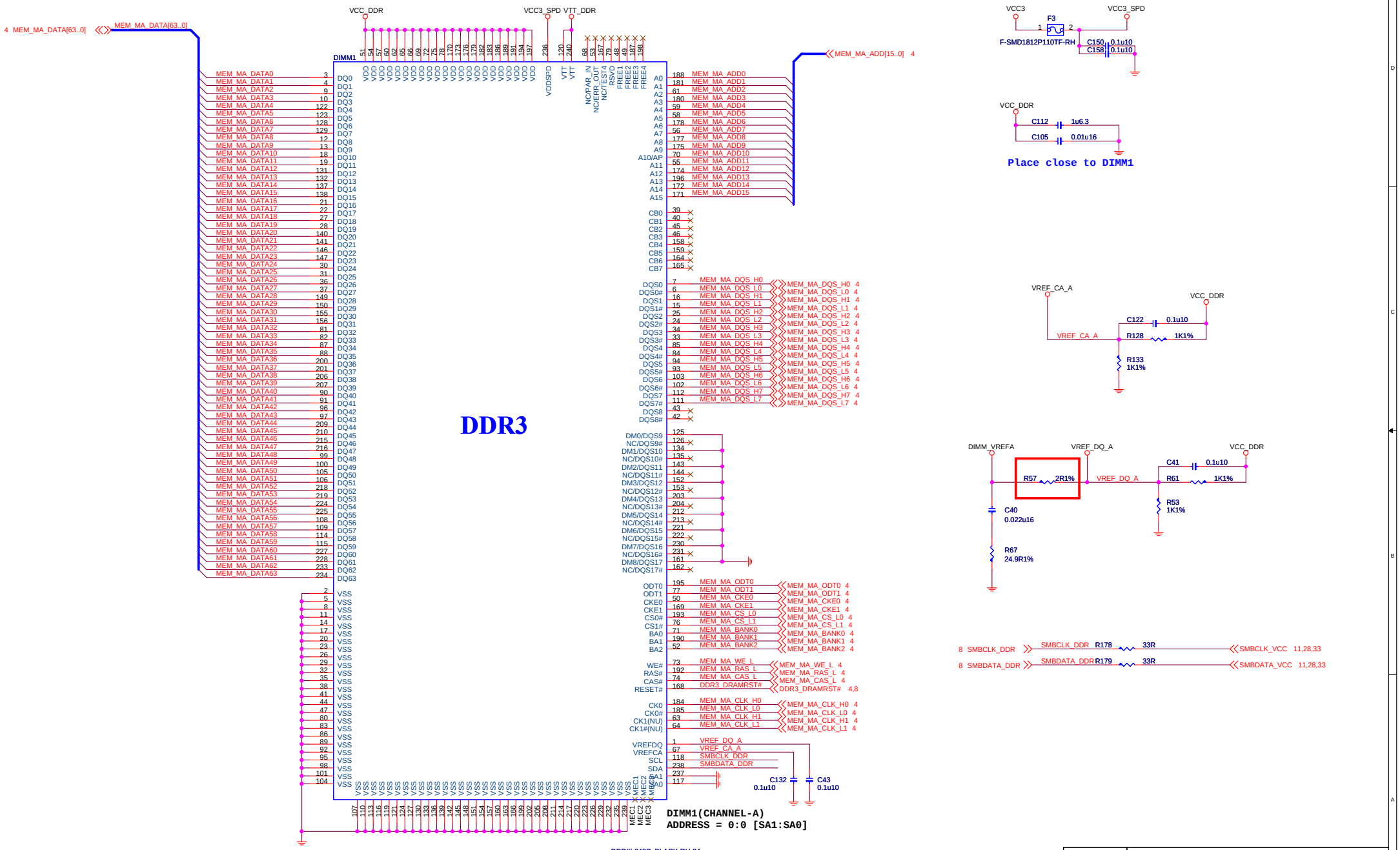

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2	Rev: 1.0
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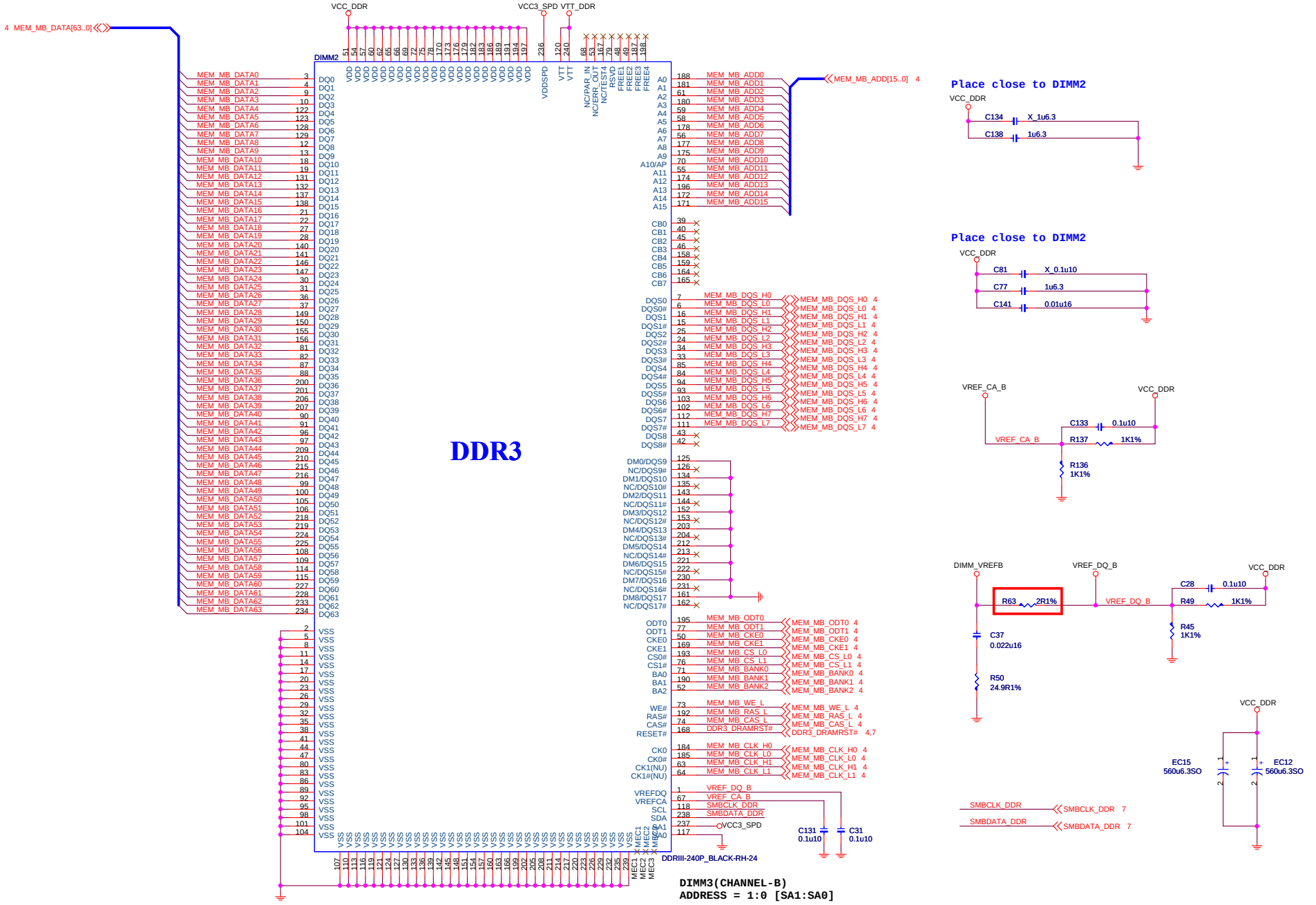
DDRIII DIMM_B0



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Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
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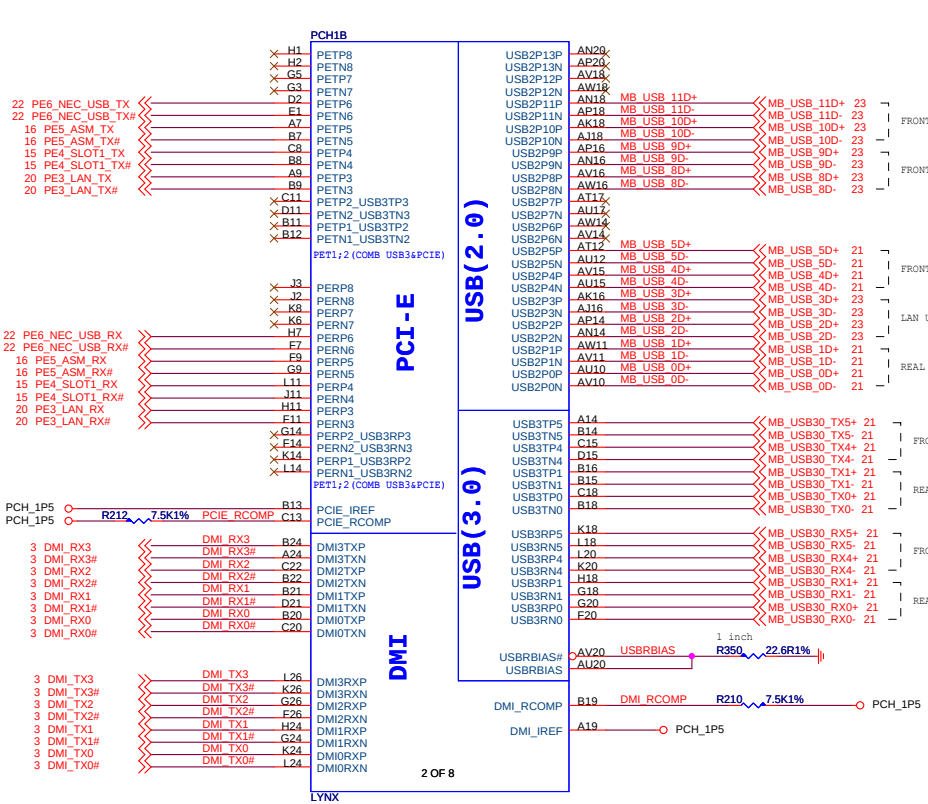
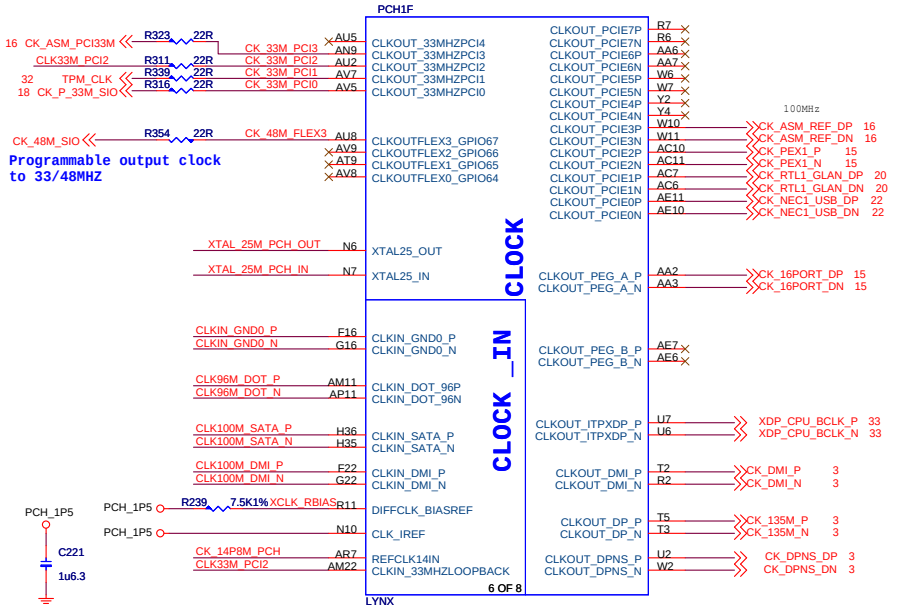
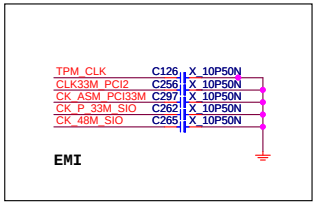
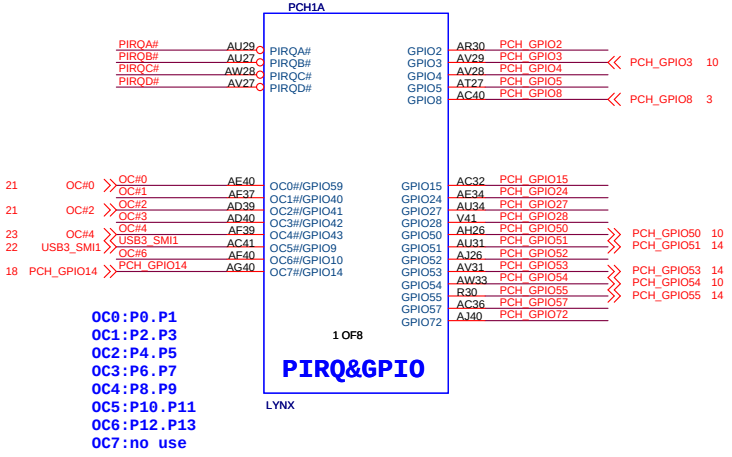
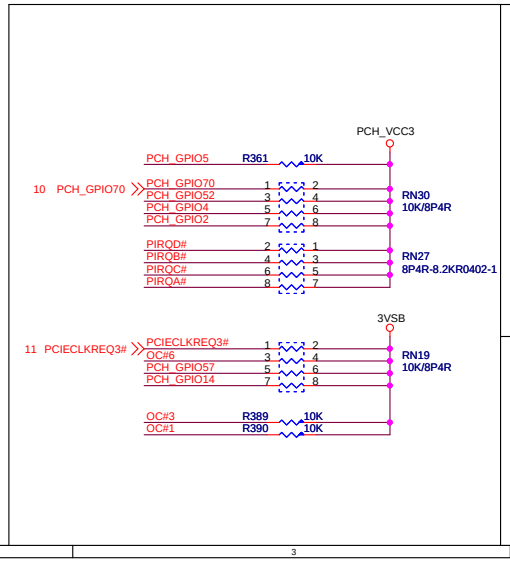
USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
Only USB 3.0 ports 1 and 2 are enabled.
pcie port7,8 NA

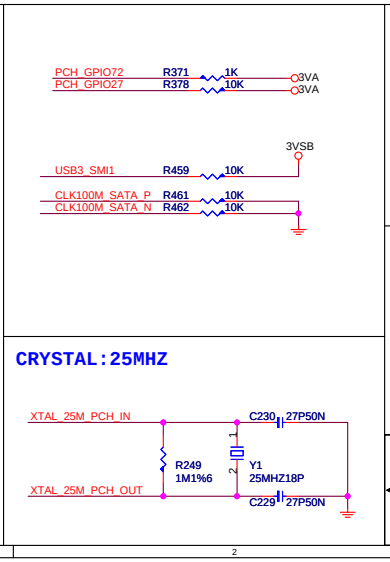


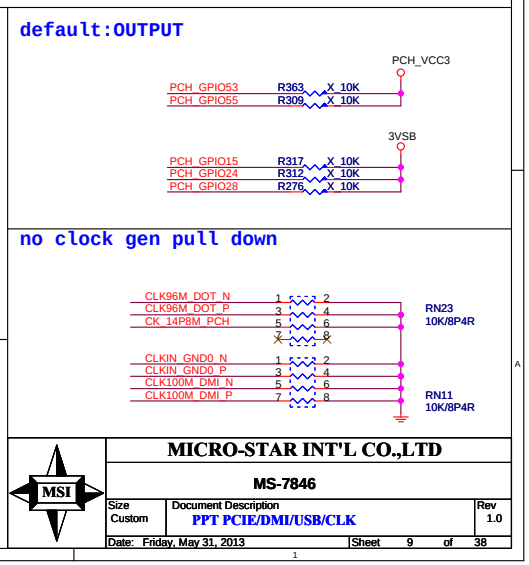












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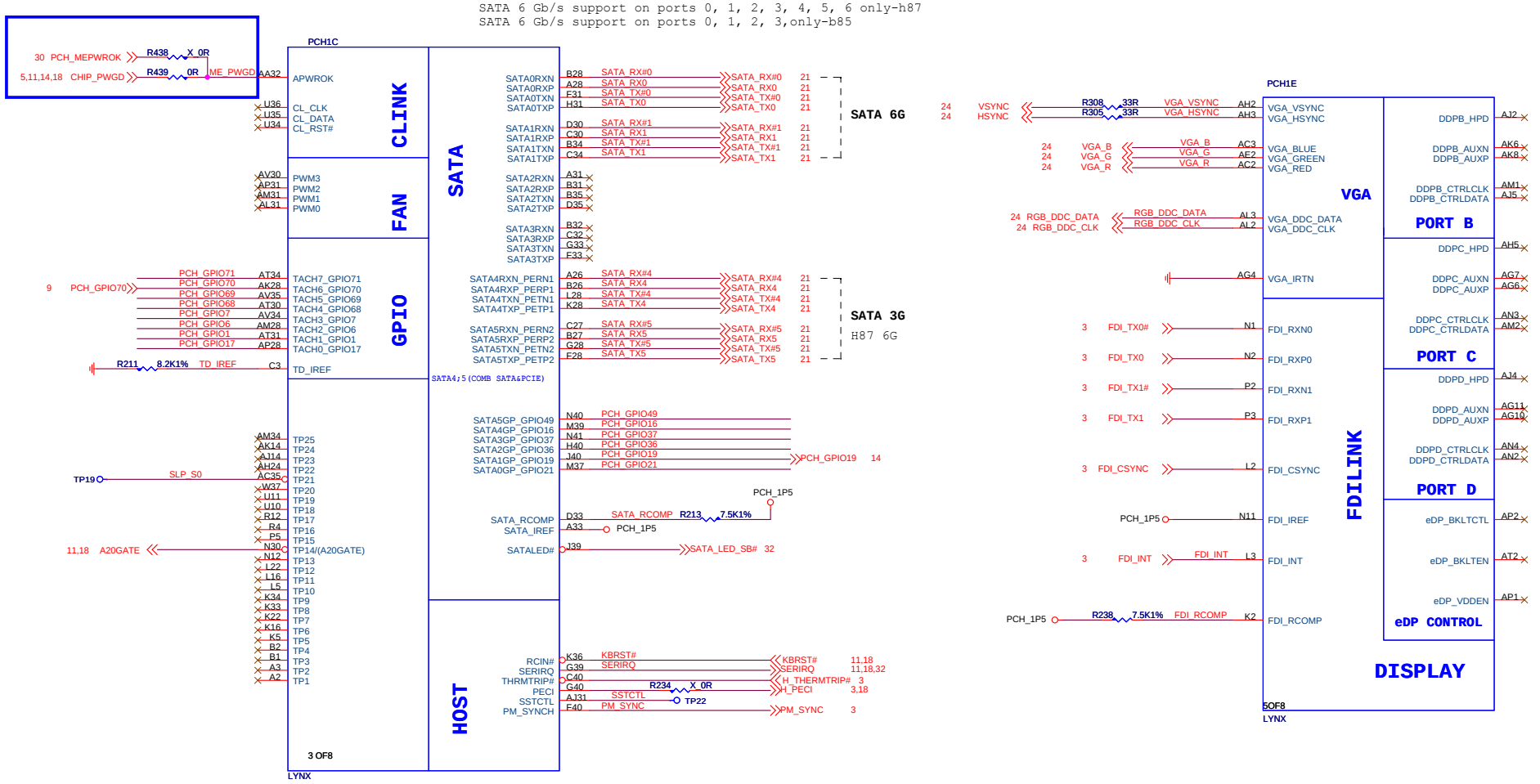
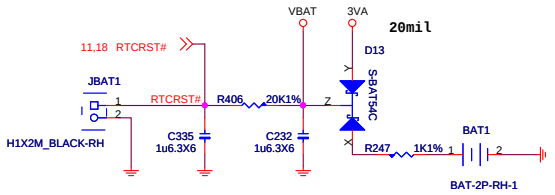
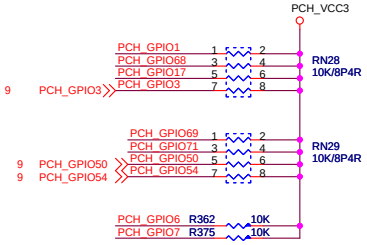
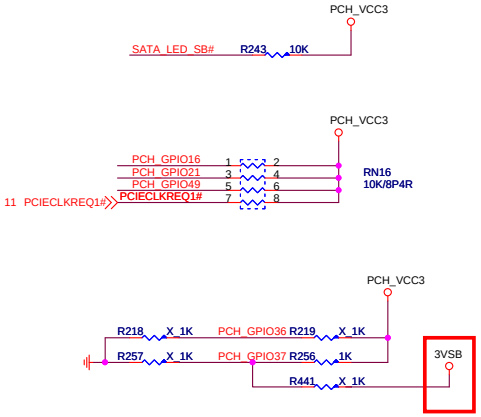
SATA 6 Gb/s support on ports 0 and 1 only.-h81
SATA 6 Gb/s support on ports 0, 1, 2, 3, 4, 5, 6 only-h87
SATA 6 Gb/s support on ports 0, 1, 2, 3,only-b85



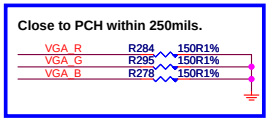
RTC and CLR_CMOS







Enable VGA(CTRLCLK/DATA Pull High)



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Size: Custom	Document Description: PPT SATA/HOST/FAN/GPIO/VGA
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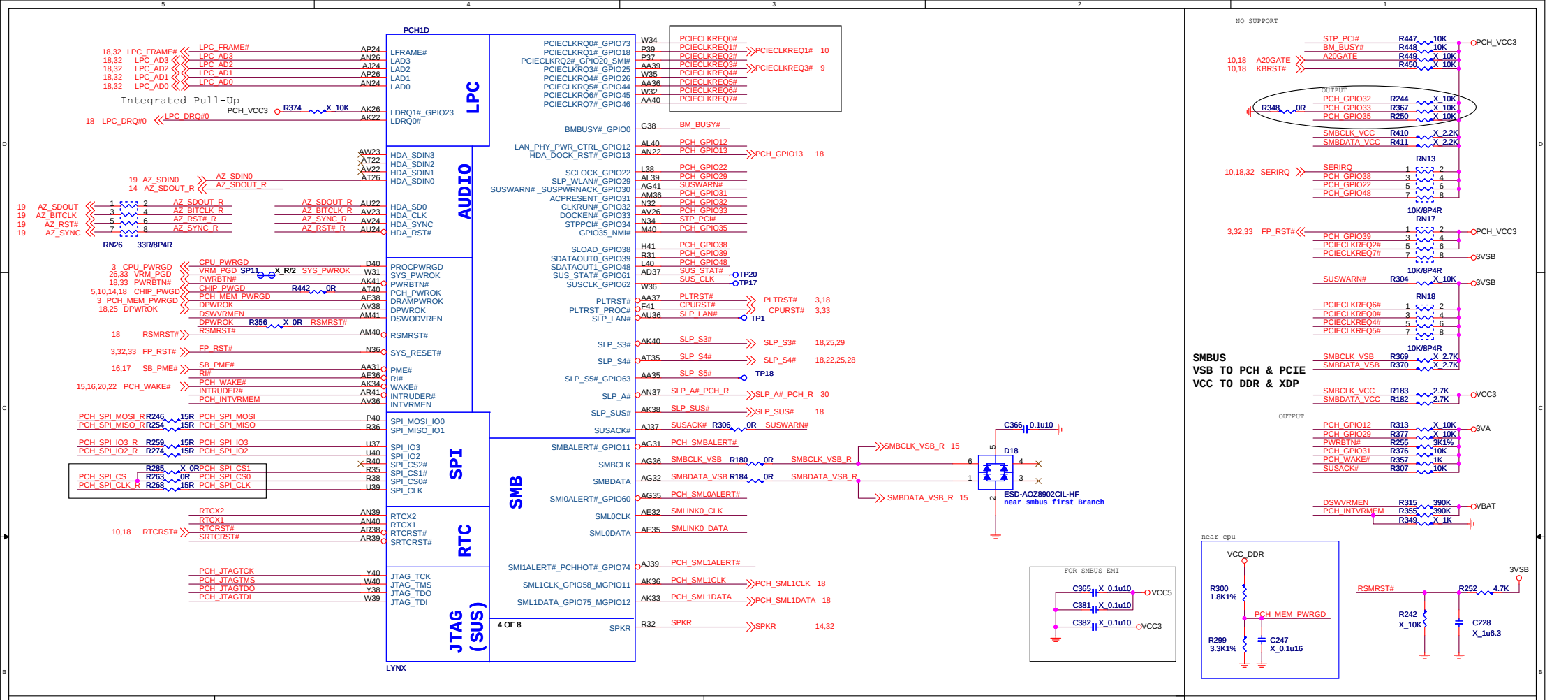

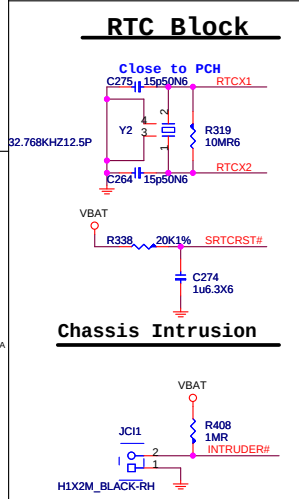

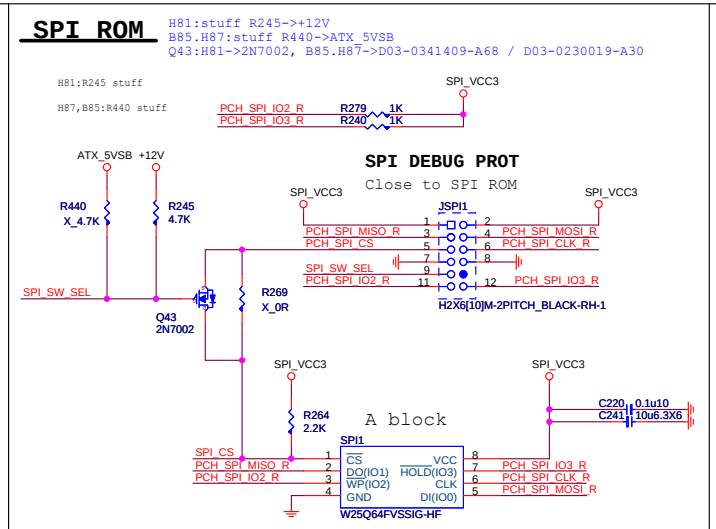

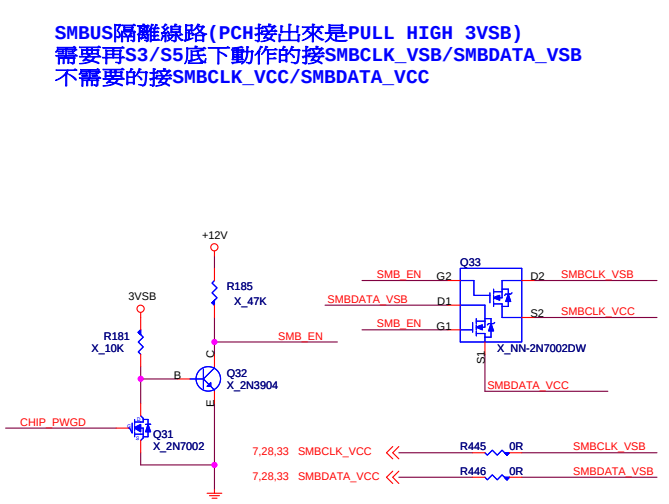

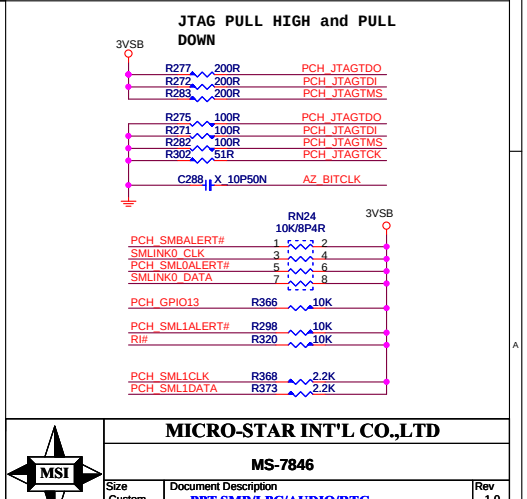

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Custom	PPT SMB/LPC/AUDIO/RTC	1.0

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VCC3 (PCH_VCC3) 0.21A

3VA 0.015A

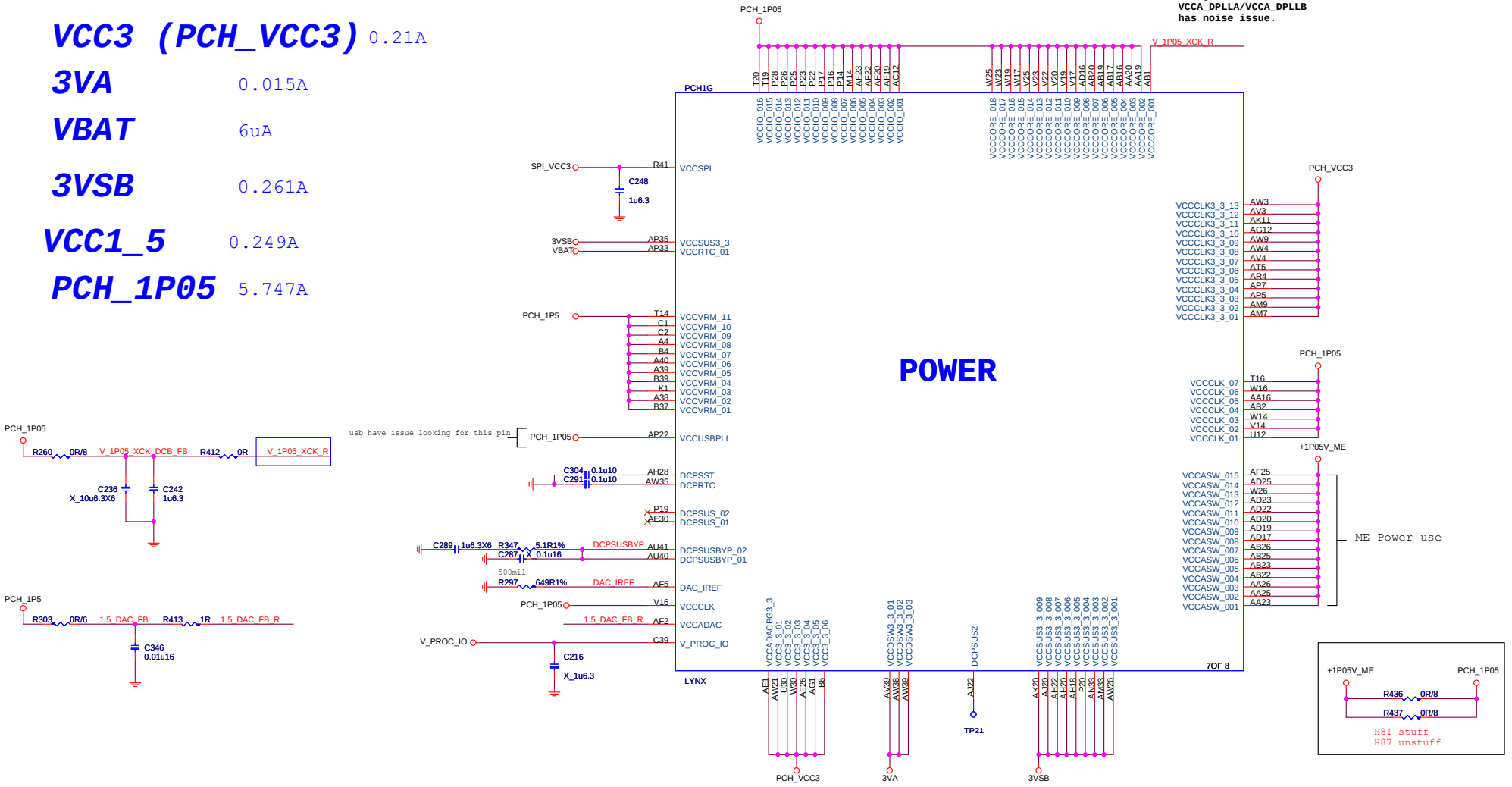
VBAT 6uA

3VSB 0.261A

VCC1_5 0.249A

PCH_1P05 5.747A

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

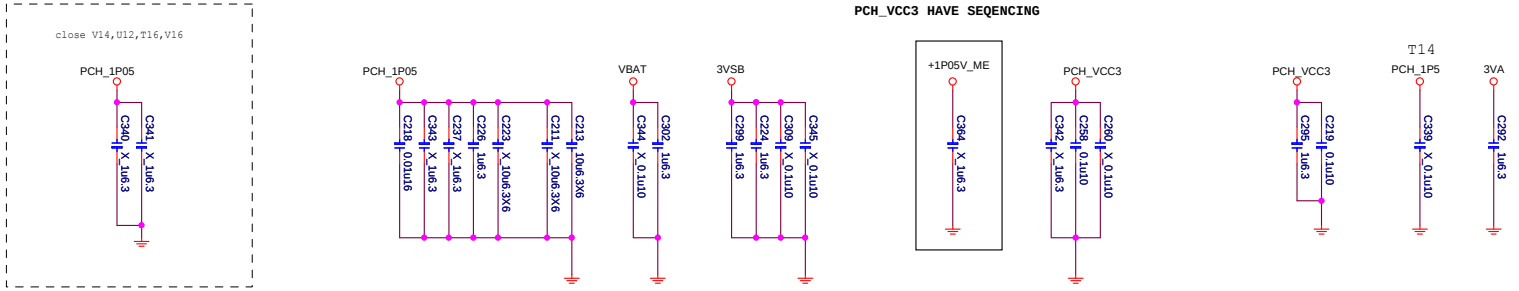


PCH decoupling cap

close V14,U12,T16,V16

PCH_VCC3 HAVE SEQENCING

T14



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Size: Custom	Document Description: LYNX -POWER PIN
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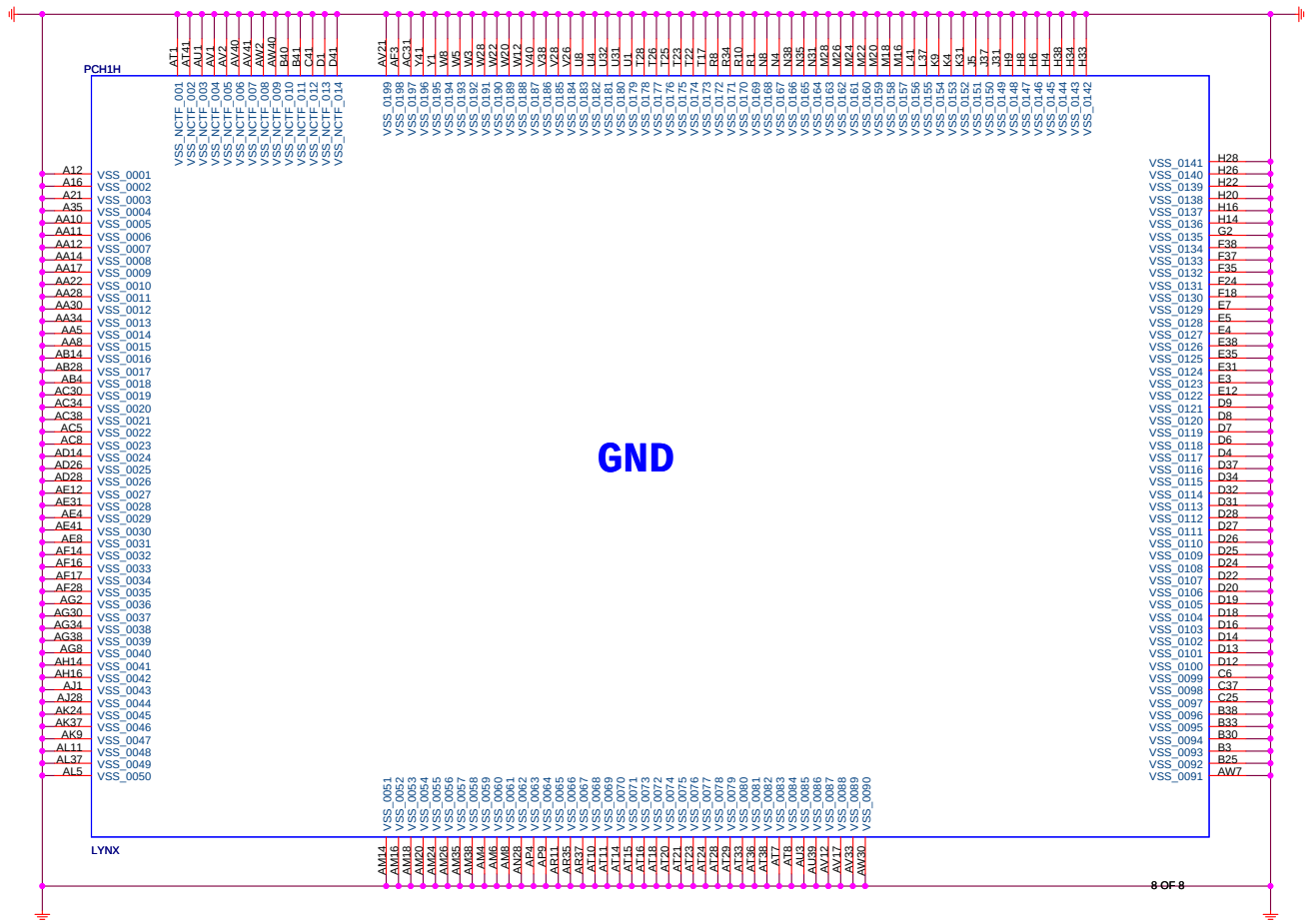

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Size: Custom	Document Description: PPT GND/NVRAM	Rev: 1.0
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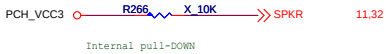
PCH Straps



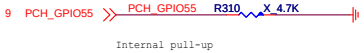
SPKR

Default Mode:

Internal weak Pull-down.

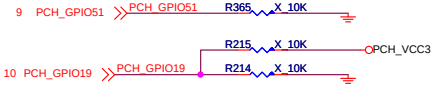
No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



GPIO55

Default Mode:
Internal pull-up.
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

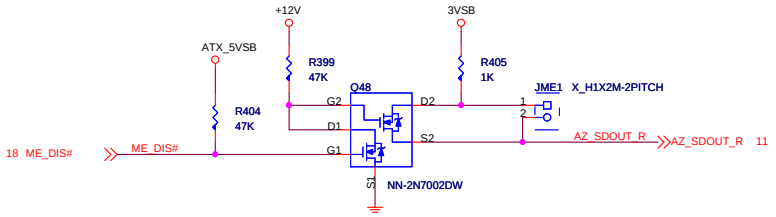


SATA1GP/GPIO19, GPIO51

Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

GPIO53

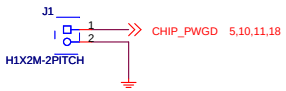
Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

Default:
Do not pull high.
Disable ME in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

For test cpu voltage



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Size: Custom	Document Description: PPT STRAPS	Rev: 1.0
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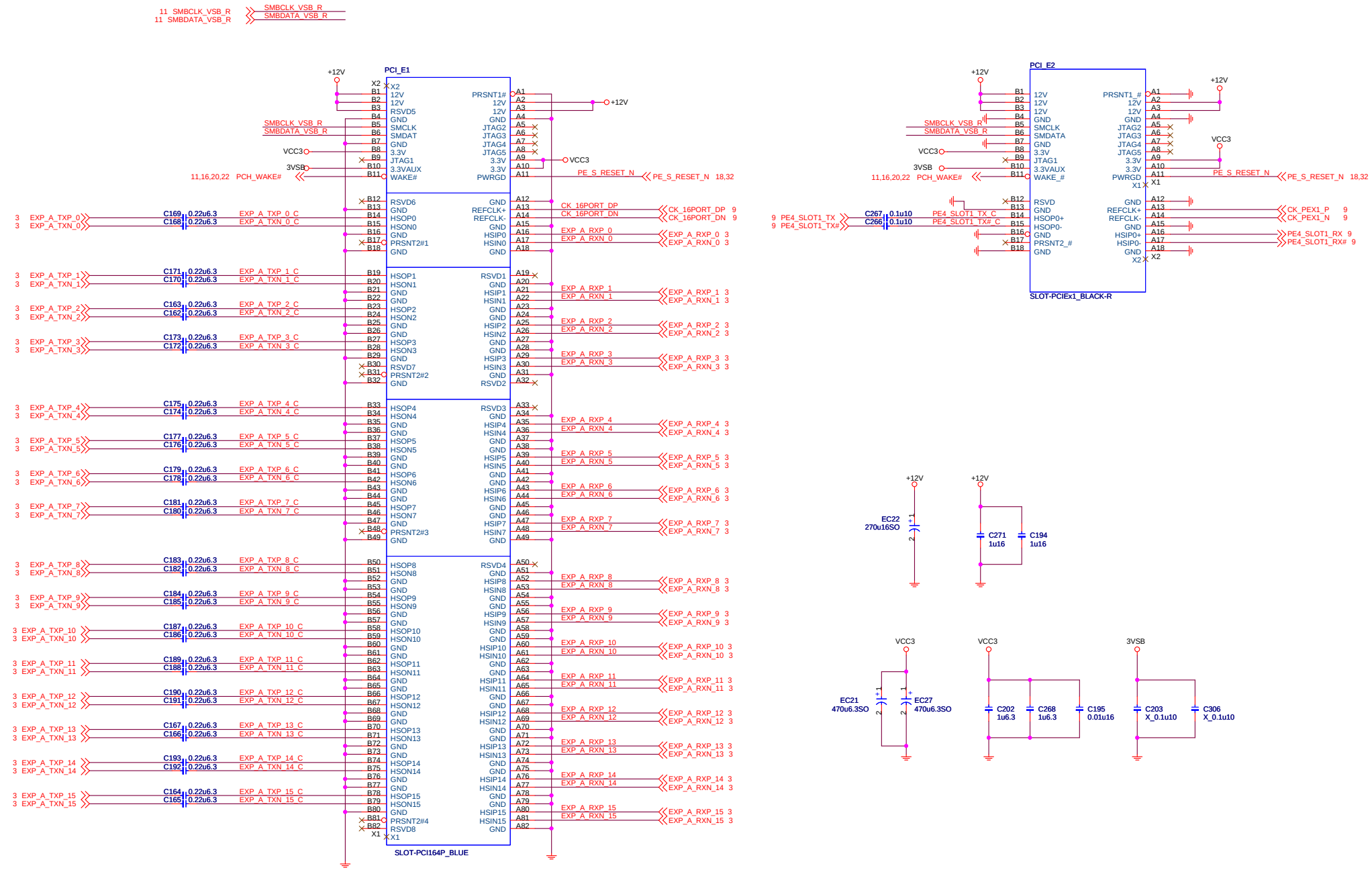

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIE1(X1) & PCIE2(X16) Slots	Rev: 1.0
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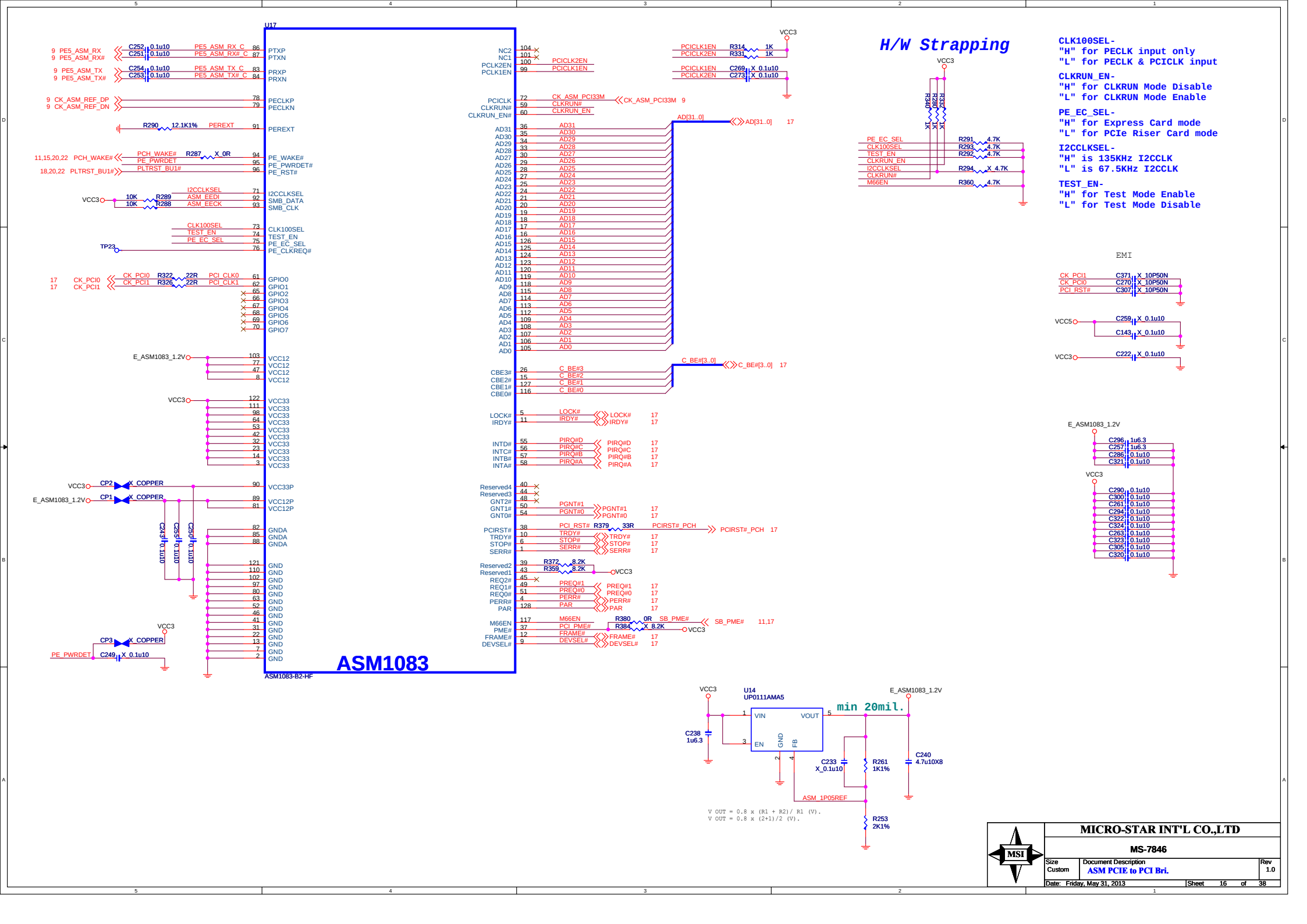
U17
ASM1083
ASM1083-B2-HF
H/W Strapping
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
EMI
min 20mil.
V OUT = 0.8 x (R1 + R2)/ R1 (V).
V OUT = 0.8 x (2+1)/2 (V).
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description ASM PCIE to PCI Bri.
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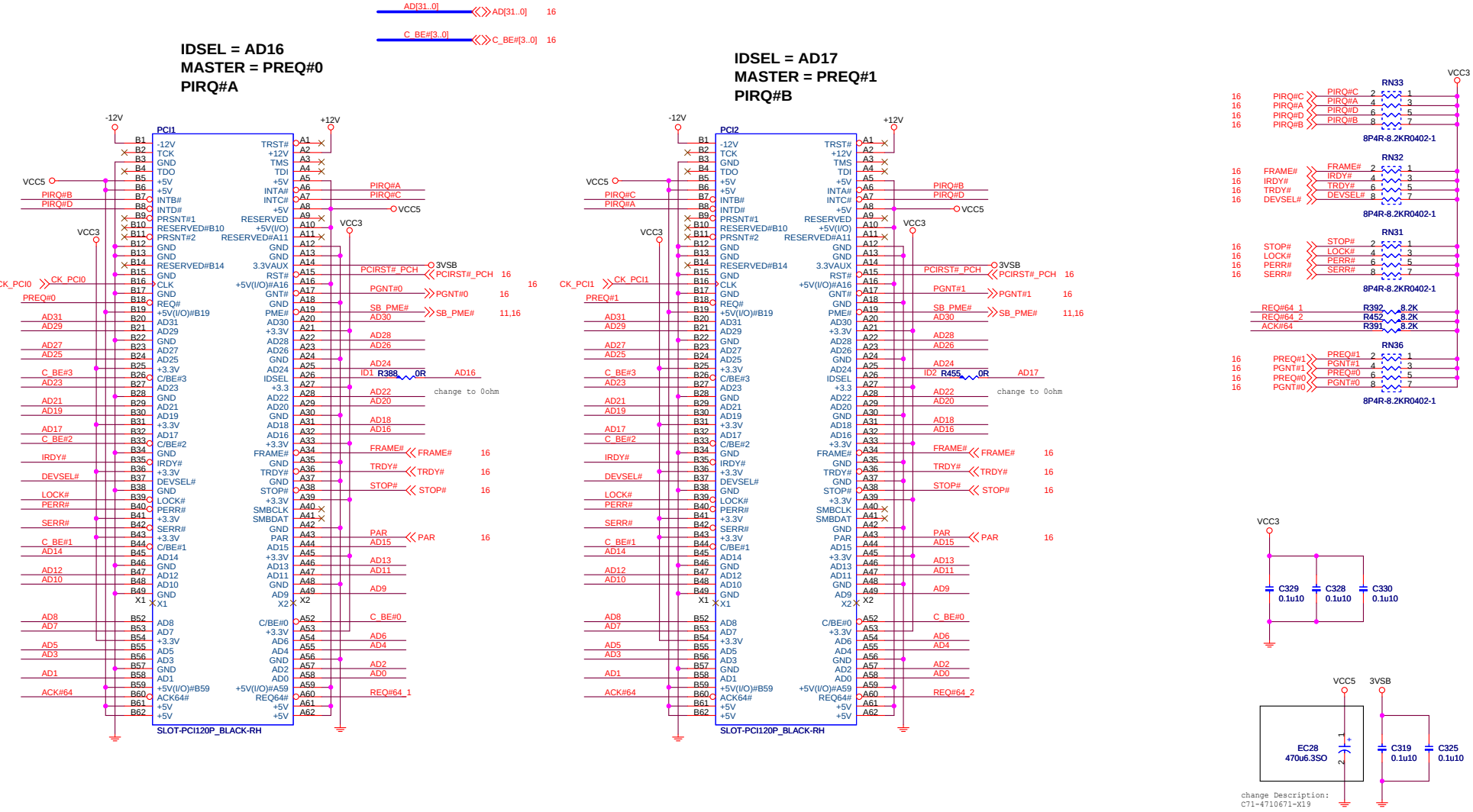

PCI slot (X2)	
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 5.2A
+5V	- 10A
+12V	- 1A

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都當GPIO
沒用的GPIO PIN 請PULL DOWN
FOR SIO POWER CONSUMPTION
GP73 BIOS要PO成WDT# FUNCTION

FOR BIOS USED
H81 0 0 0
B85 0 0 1
H87 0 1 0

GPIO013 from PCH

PCIE _SLOT_RESET_N
from SIO RESET_BUS2

Sio modify 12/24 Eric mail

GPIO 41, 46, 31 and 32 that
Support Wake-Up Function

PS2 Connector

Voltage Sensing

close to pin99

close to pin24,108

close to pin46,85

Thermal Resistor

(PIN31)RTSA#	0=2E	1=4E
(PIN32)DTRA#	0=24MHz	1=48MHz
(PIN34)SOUTA	0=Port80 Enable	1=PRT Enable
(PIN69)DSW_EN	0=Disable	1=Enable
(PIN9))(RTSB#)ORT80_EN	0=Disable	1=Enable
(PIN96)AMDPWR_EN	0=Disable	1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN	0=Disable	1=Enable

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Size: Custom | Document Description: 17 SIO-NTC6779D/PS2 | Rev: 1.0

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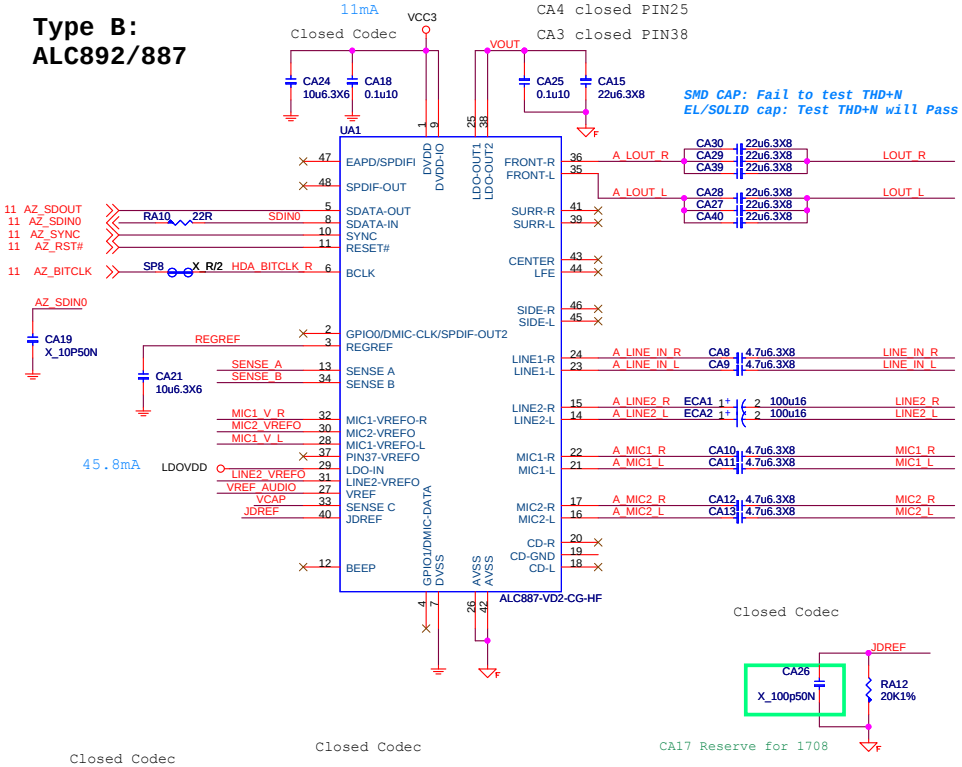
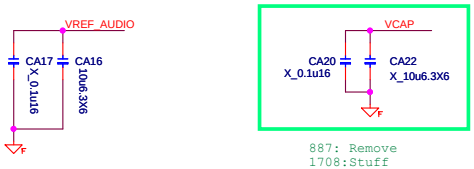
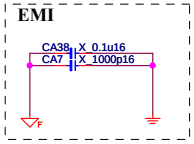
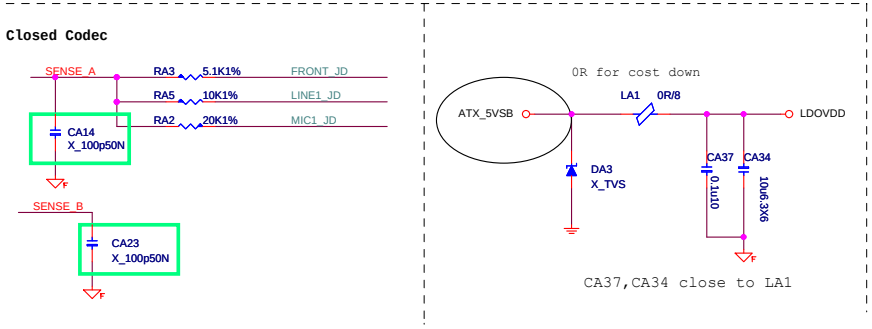
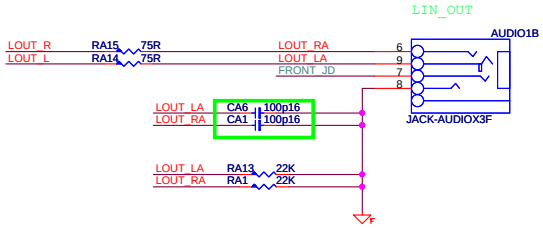
Type B: ALC892/887

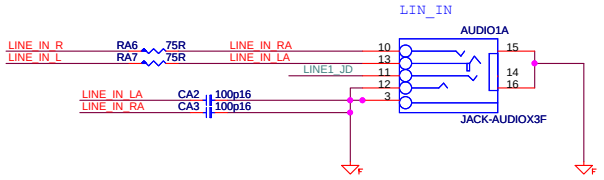


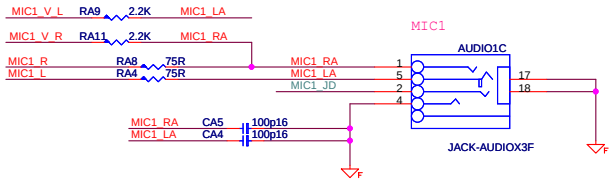


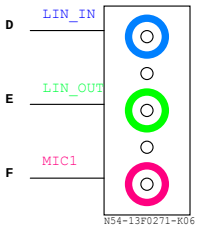


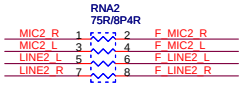


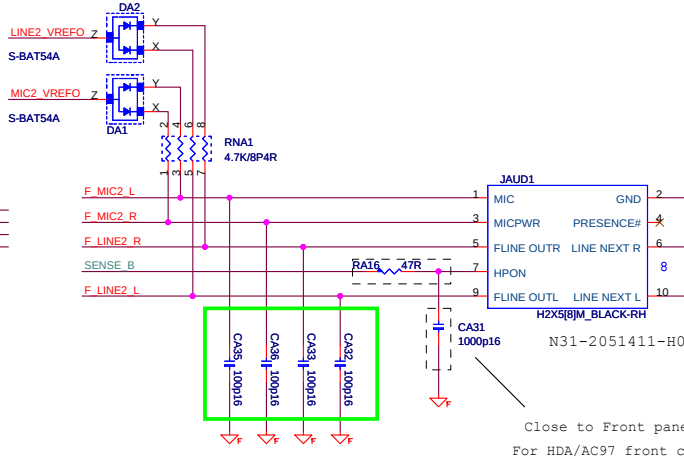












100pF Cap can change to TVS by PM request.

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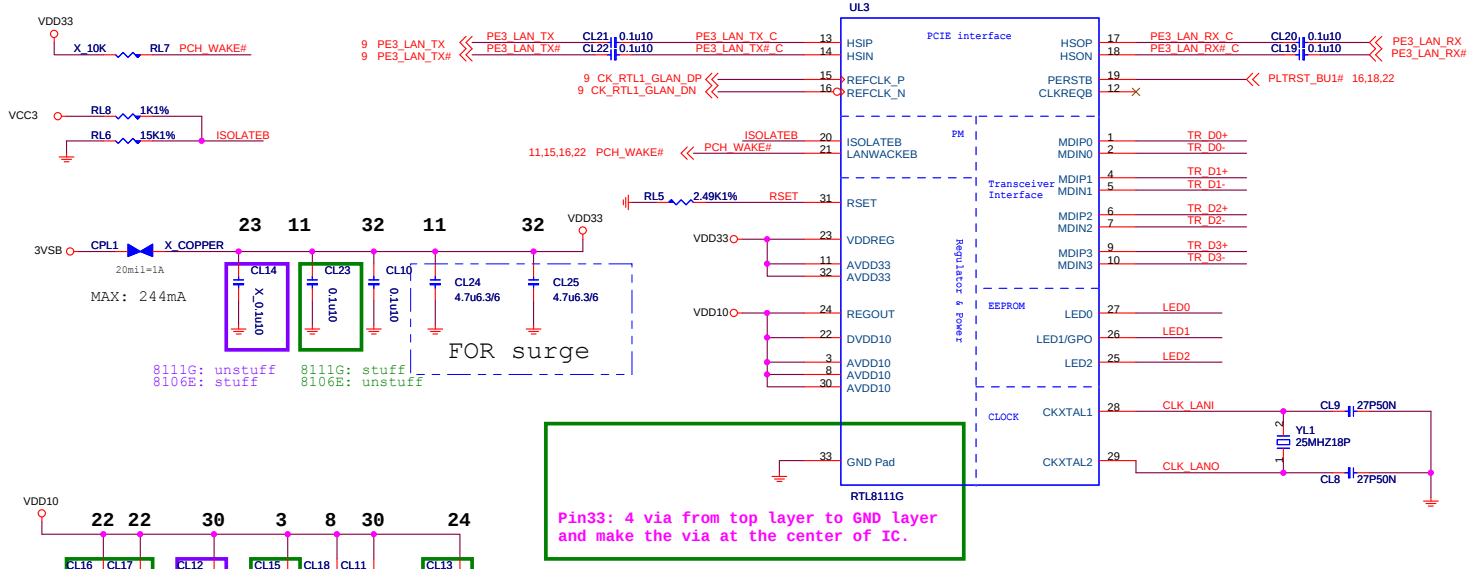
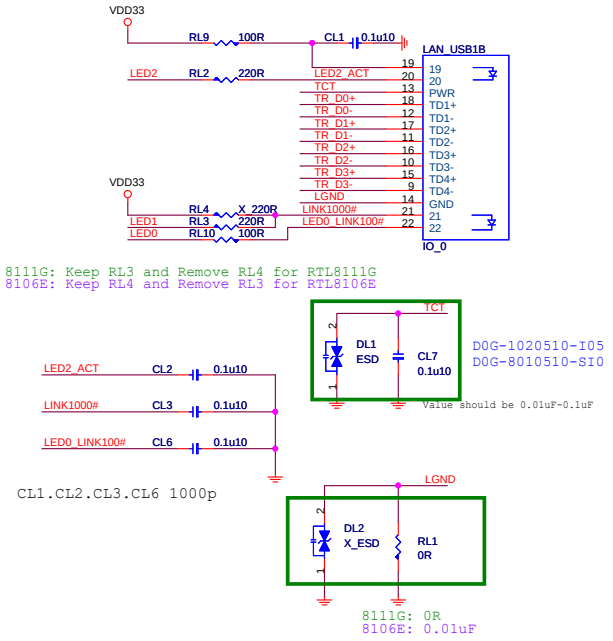
RTL8111G Giga LAN
RTL8106E 10/100M LAN

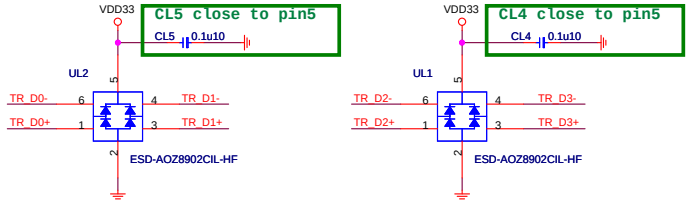


Icc10 average operating supply current from1.0V
At 1Gbps with heavy network traffic 300mA

LAN Connector



Reserve ESD Protect



MSI P/N : D0G-0200529-A68 、Vender P/N : AOZ8902CI
MSI P/N : D0G-0100619-I05 、Vender P/N : TVLST2304AD0

8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

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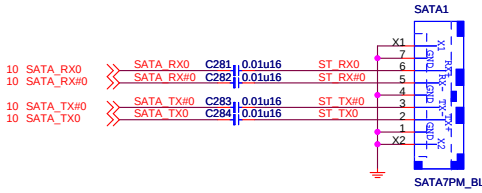
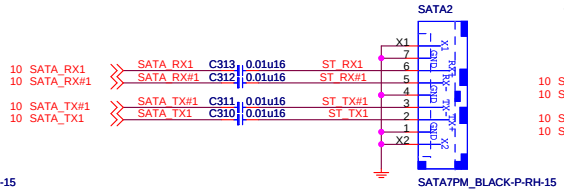
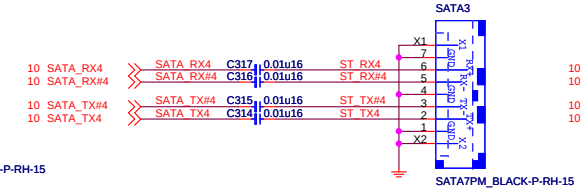
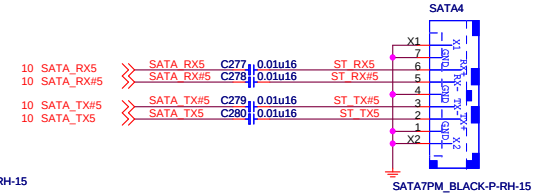
SATA 6G PORT 0,1

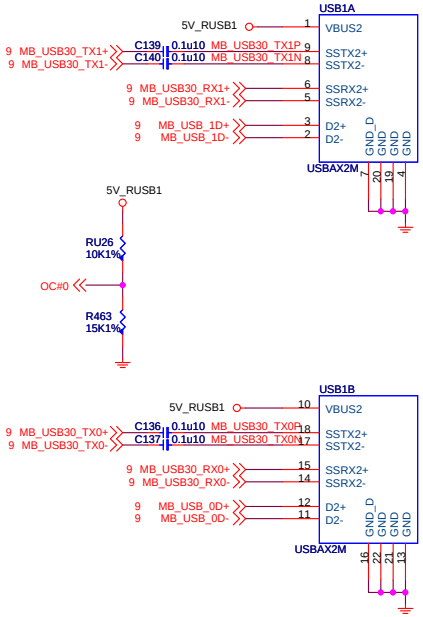


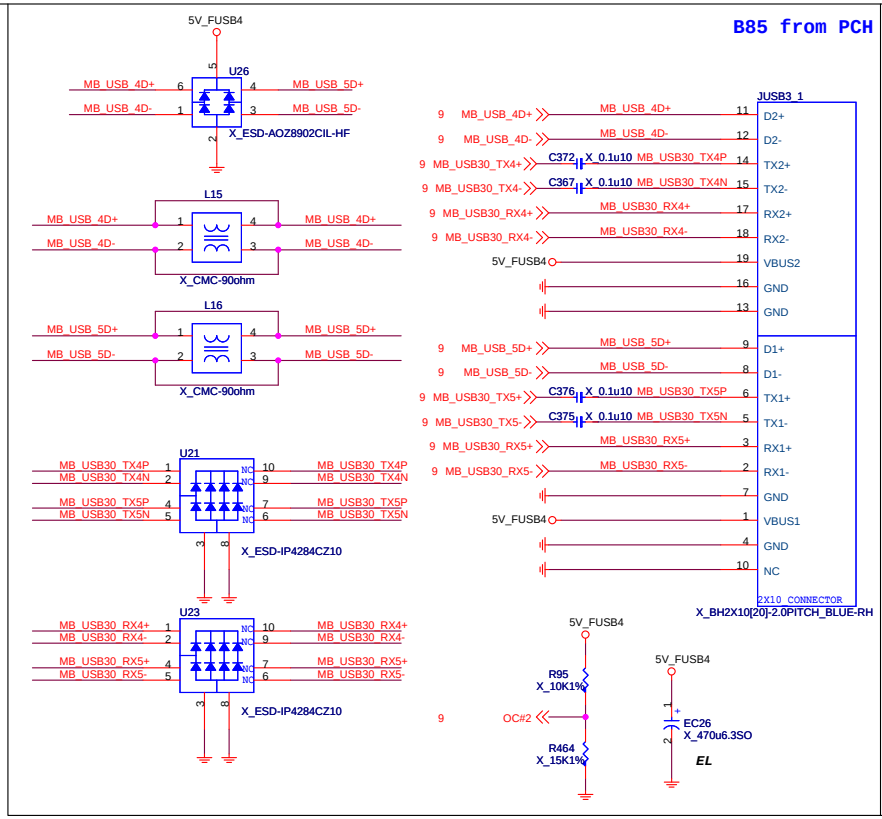


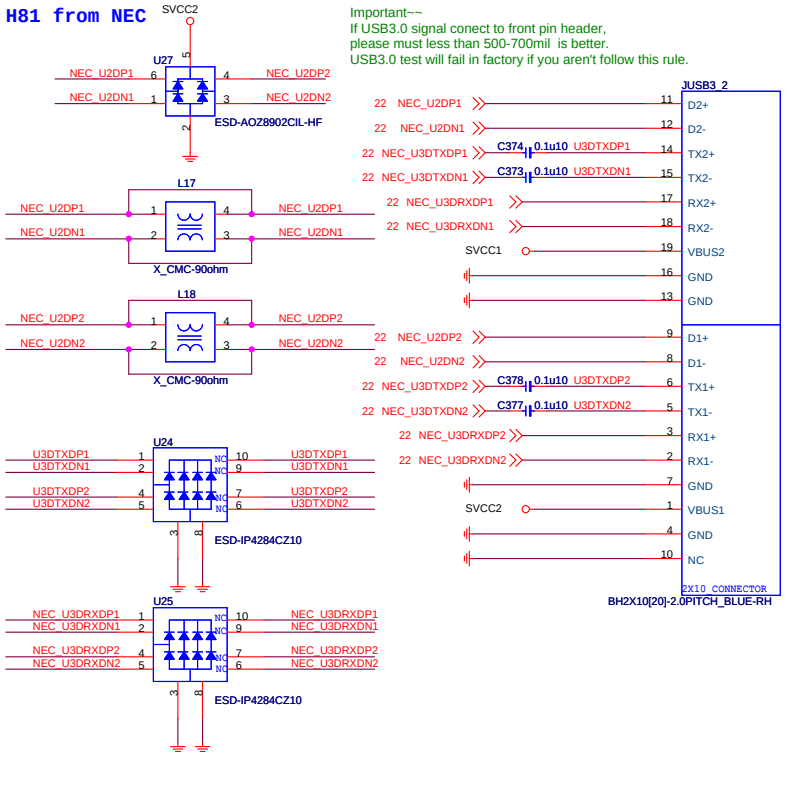
SATA 3G PORT 4,5

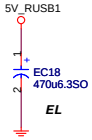


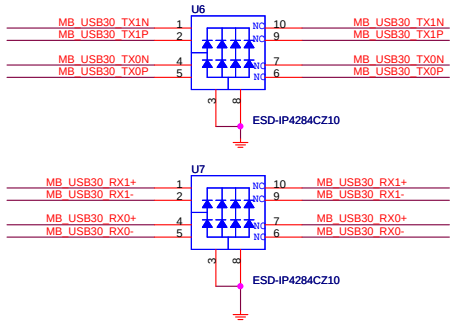


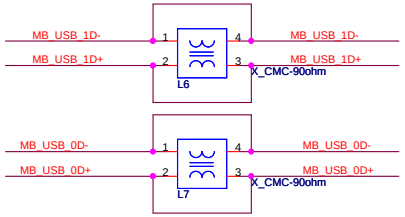


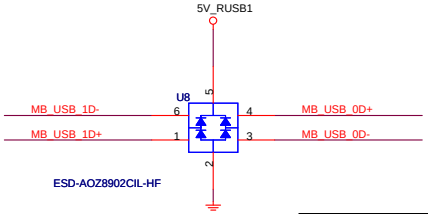












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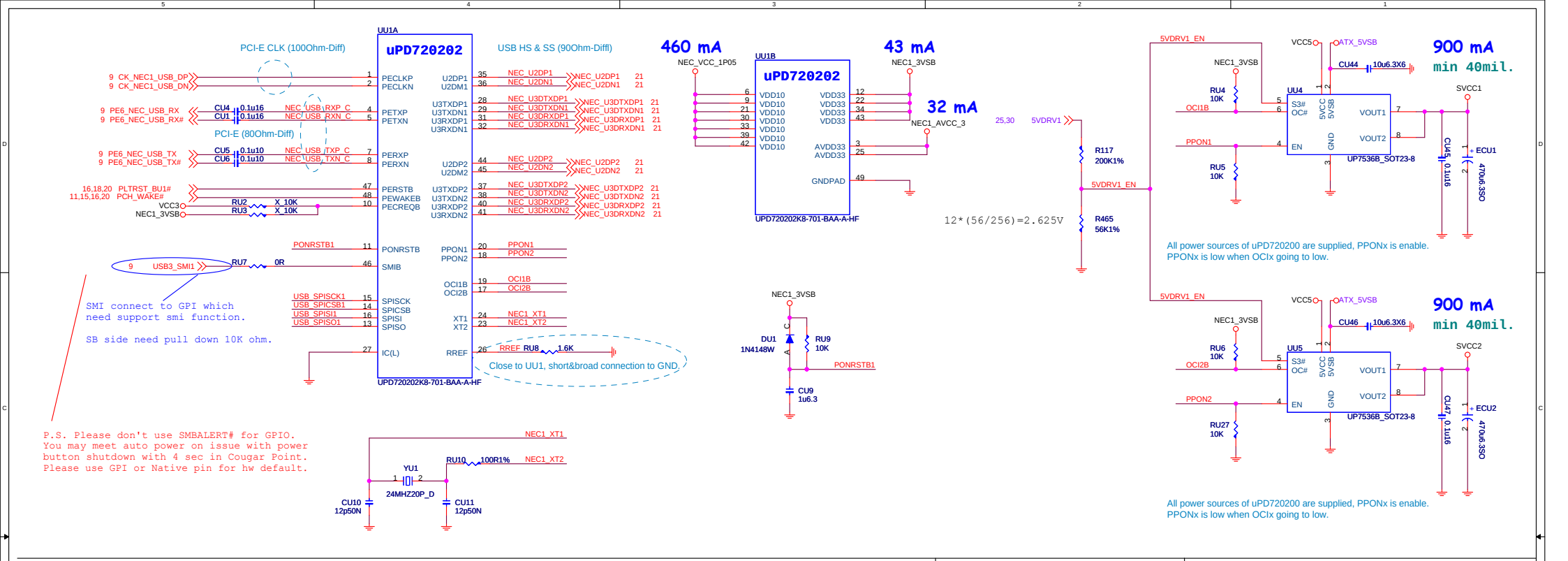
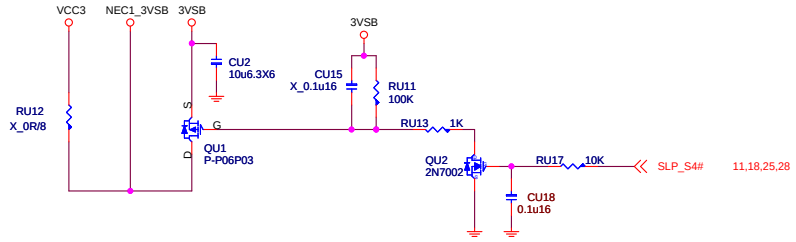
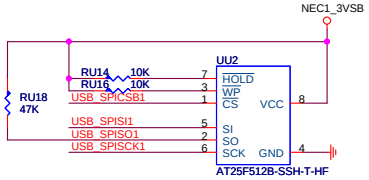


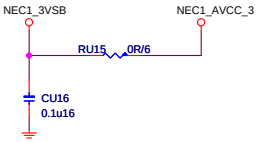
3V_Dual Circuit

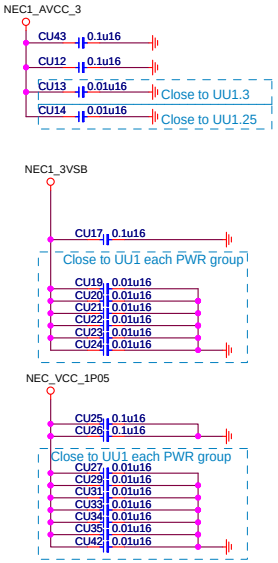


EEPROM

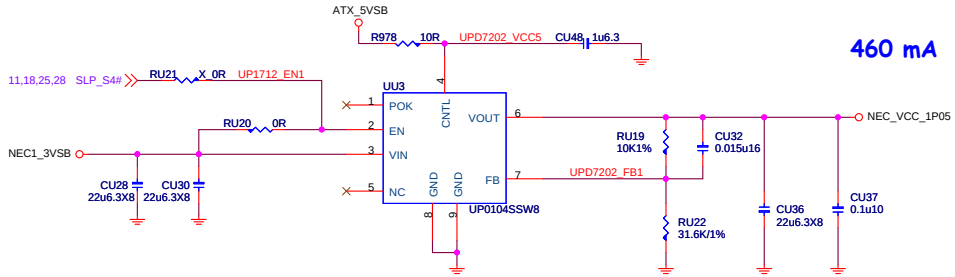


AVCC3 STB Power





uPD720200 core Power



MICRO-STAR INT'L CO.,LTD	
MS-7815	
Size: Custom	Document Description: Renesas µPD720202 USB3.0 2PORT
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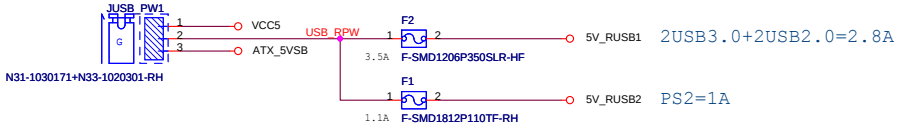
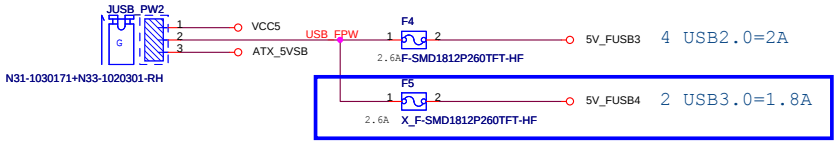
Type C: jumper +Fuse

PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



Near Front ==>



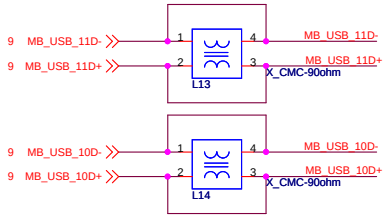
Default VCC5 (PIN1-2)

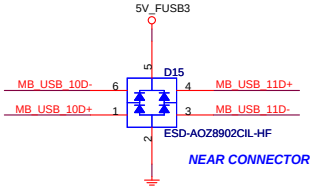
JUSB_PW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	
2-3	EUP Enable	Not support
	EUP Disable	support

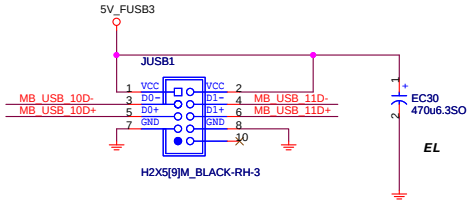
B85&H87 stuff F5

D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)
D08-2000200-P16 (Itrip=3.5A; 0.003ohm) MINISMD050

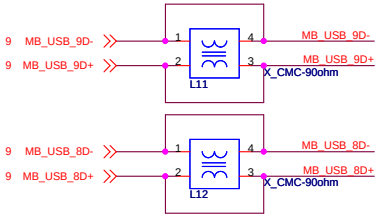
FRONT USB PORT 10,11

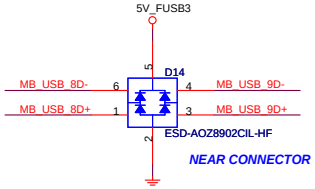


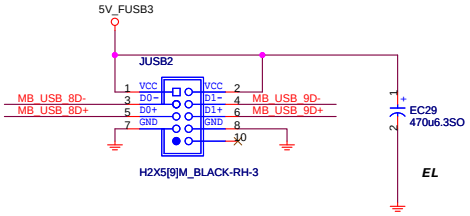




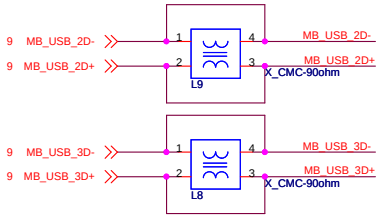
FRONT USB PORT 8,9

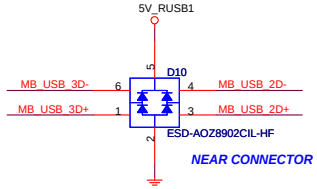


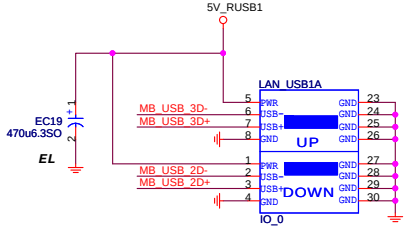


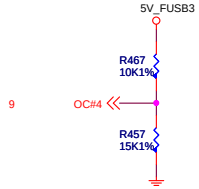


REAL USB PORT 12.13









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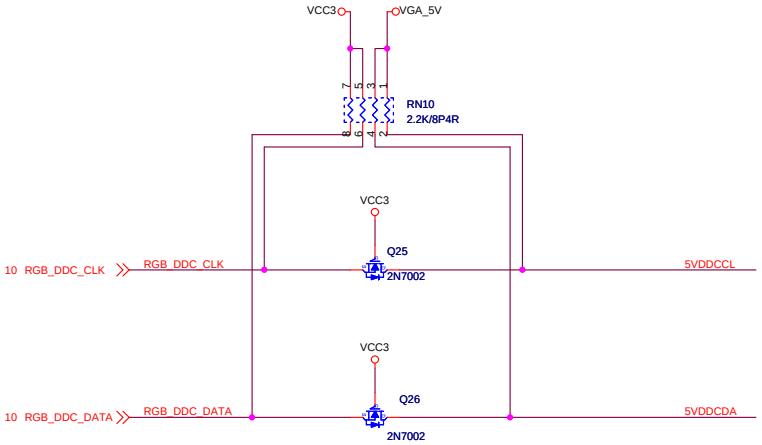
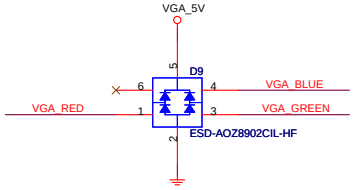
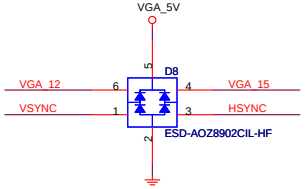
	MS-7846		
Size: Custom	Document Description: Rear I/O & USB2.0 Connector		Rev: 1.0
Date: Friday, May 31, 2013		Sheet 23 of 38	

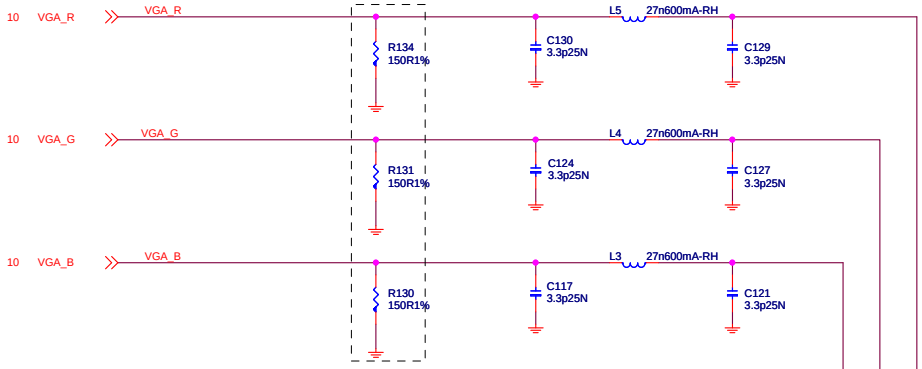
D-Sub

Level shift

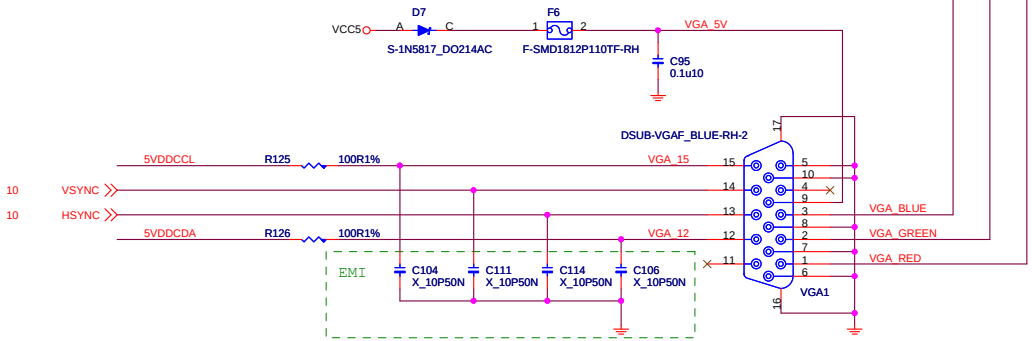








PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7846	
Size: Custom	Document Description: VGA Connector	Rev: 1.0
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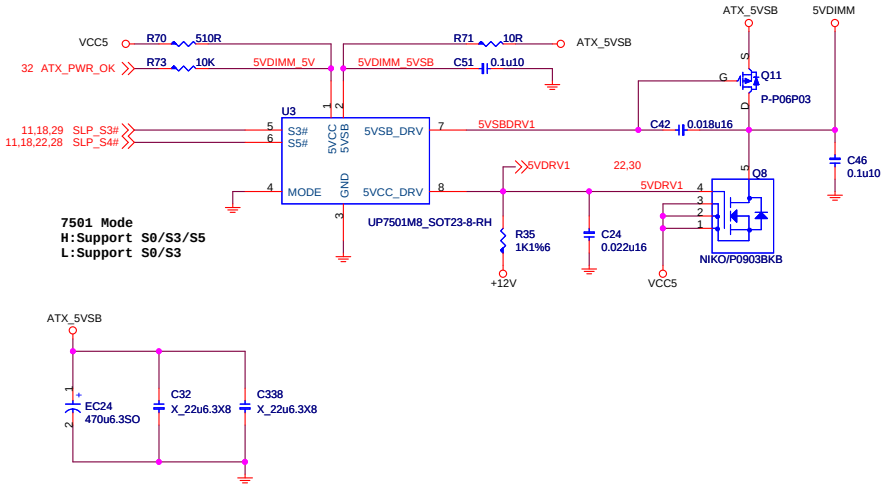
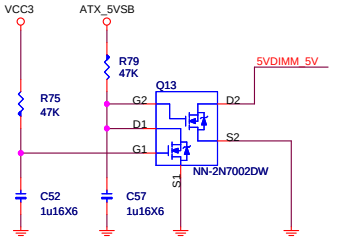
5VDIMM FOR DDR



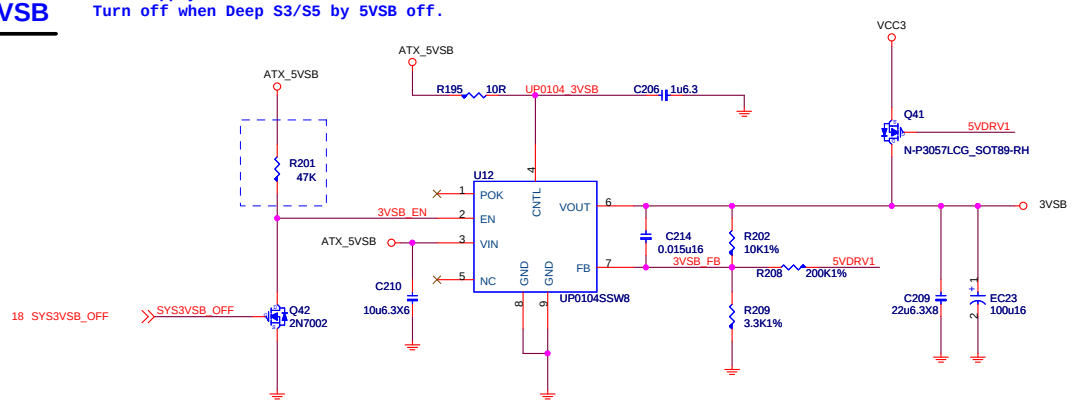
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



Patch coolermaster 700w power sequence

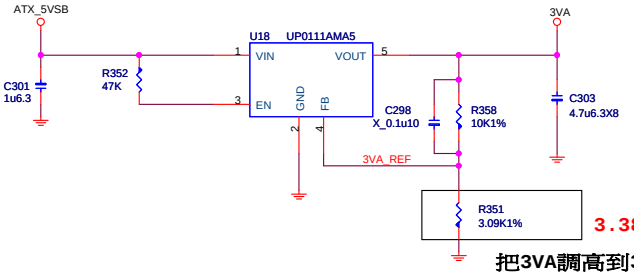
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.

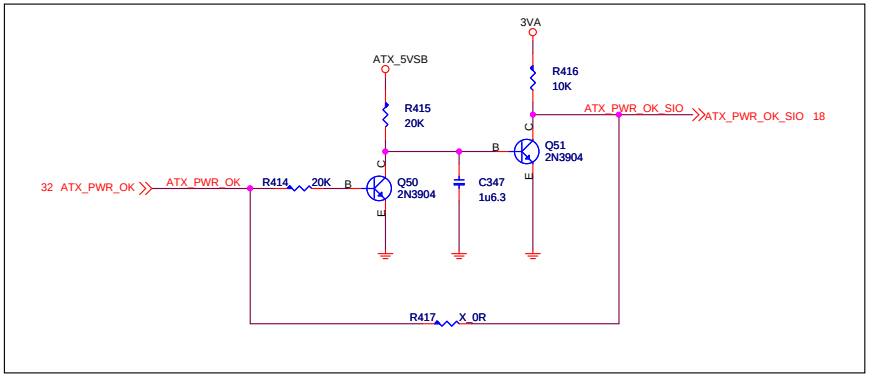


3VA

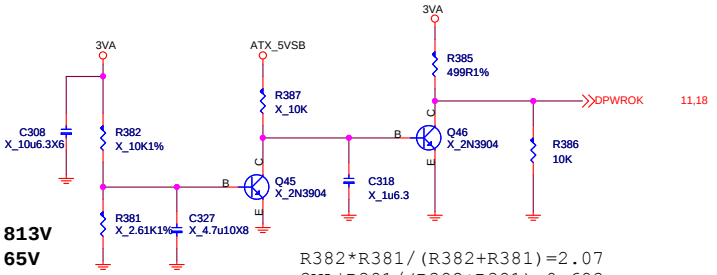
20mA



把3VA調高到3.389V



Sio modify 12/24 Eric mail



3.389V分壓=0.813V
2.71V分壓=0.65V

FOR DPWROK跟3VA的POWER DOWN的時序(S5-->G3)

R382*R381/(R382+R381)=2.07
3VA*R381/(R382+R381)=0.683
Ib=(0.683-VBE)/2.61=0.01265mA
Ic=(ATX_5VSB-Vce)/R387=0.48mA
Ic(max)<β(min)*Ib(min)=0.3795mA

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MS-7846

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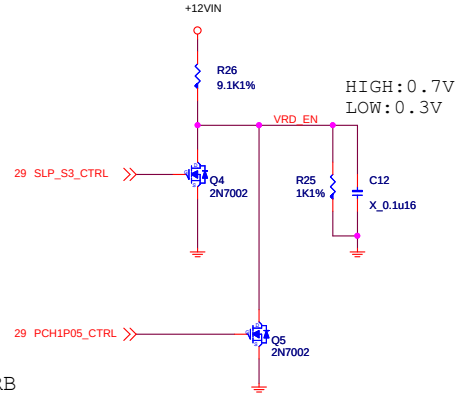
VCORE power on by s3 and 12v

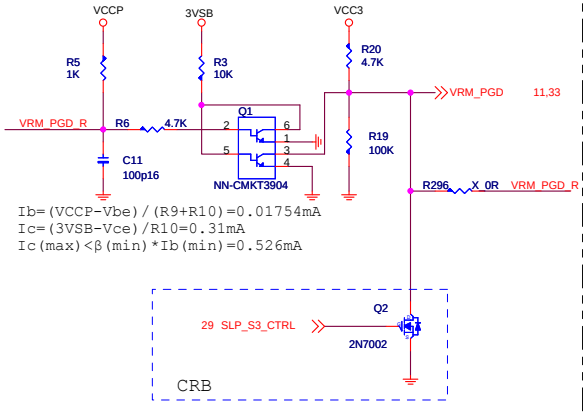


HIGH:0.7V
LOW:0.3V

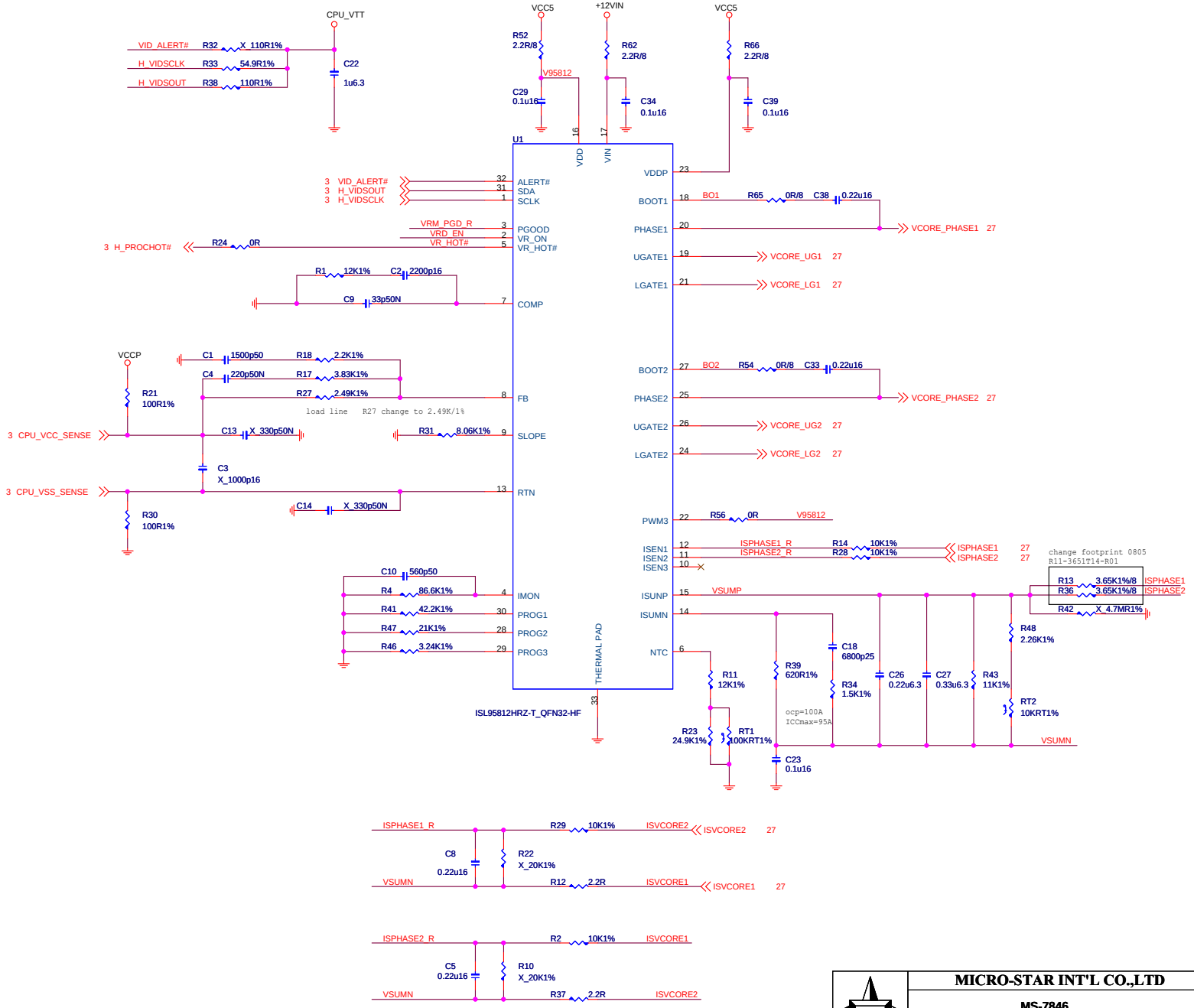
CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT



Ib=(VCCP-Vbe)/(R9+R10)=0.01754mA
Ic=(3VSB-Vce)/R10=0.31mA
Ic(max)<β(min)*Ib(min)=0.526mA



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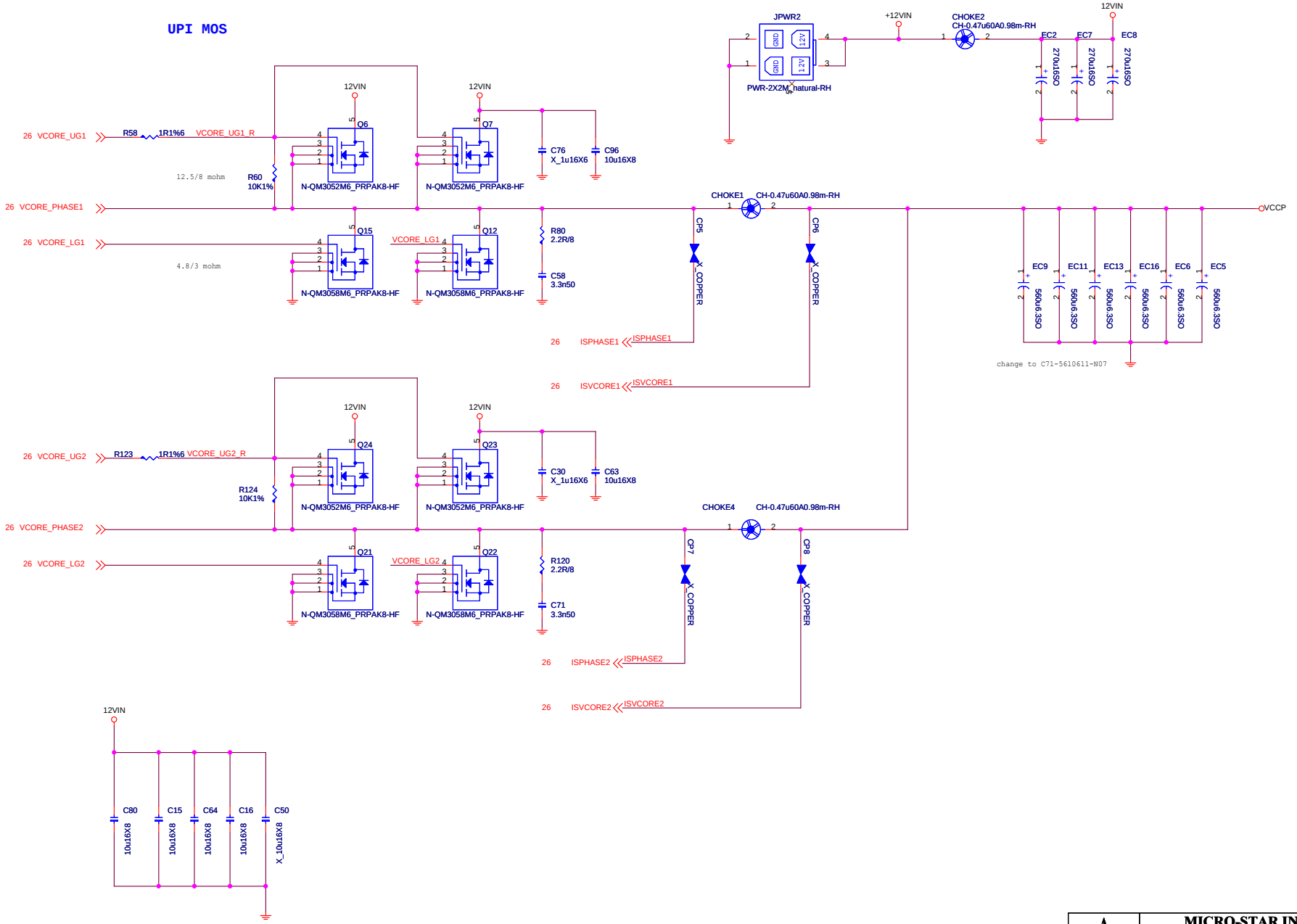
VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

Irms_input=17.5A

UPI MOS



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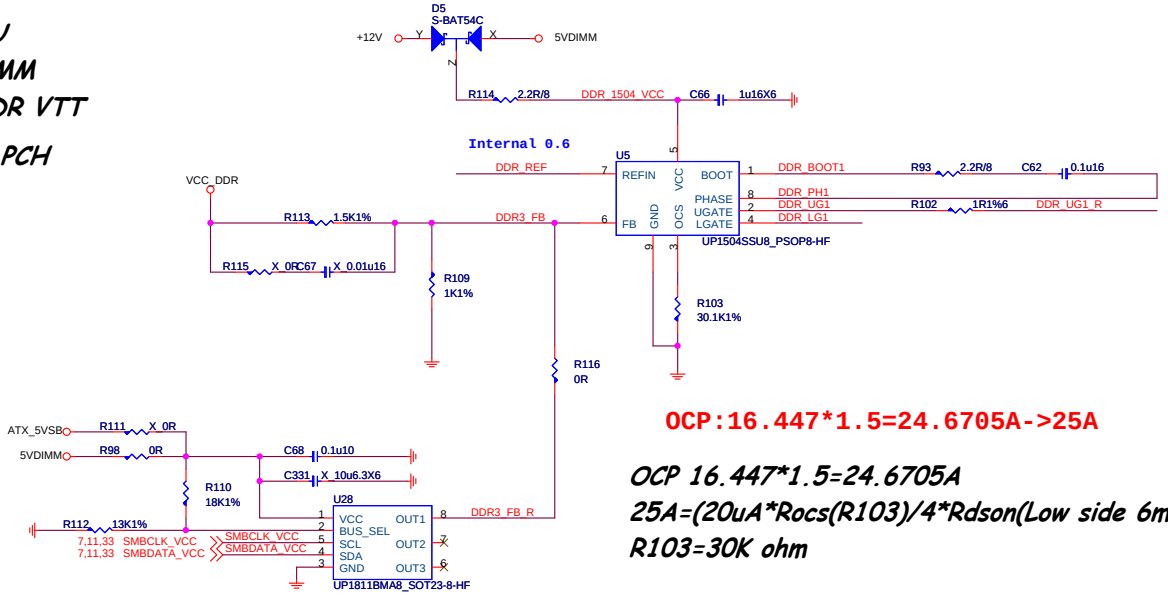
DDR Power:1.5V

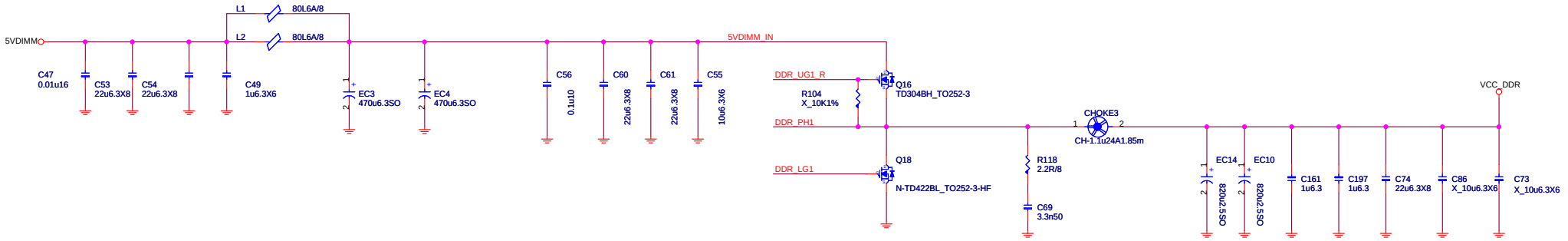
DDR3_1.5V 4.2A+6A+0.5A+5.747=16.447A

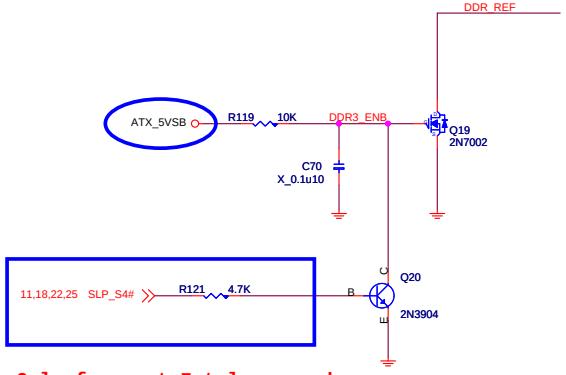
4.2A FOR CPU
6A FOR 2DIMM
0.5A FOR DDR VTT
5.747A FOR PCH



OCP:16.447*1.5=24.6705A->25A

*OCP 16.447*1.5=24.6705A*
*25A=(20uA*Rocs(R103)/4*Rdson(Low side 6mohm)*
R103=30K ohm



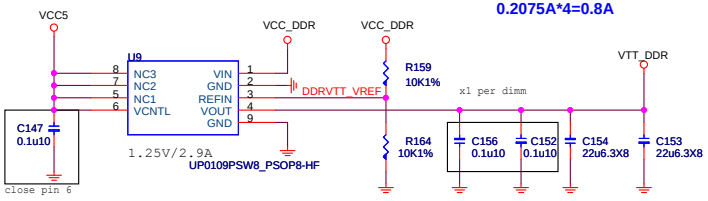


P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



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Custom	DDR Power -UP6103 1-Phase	1.0

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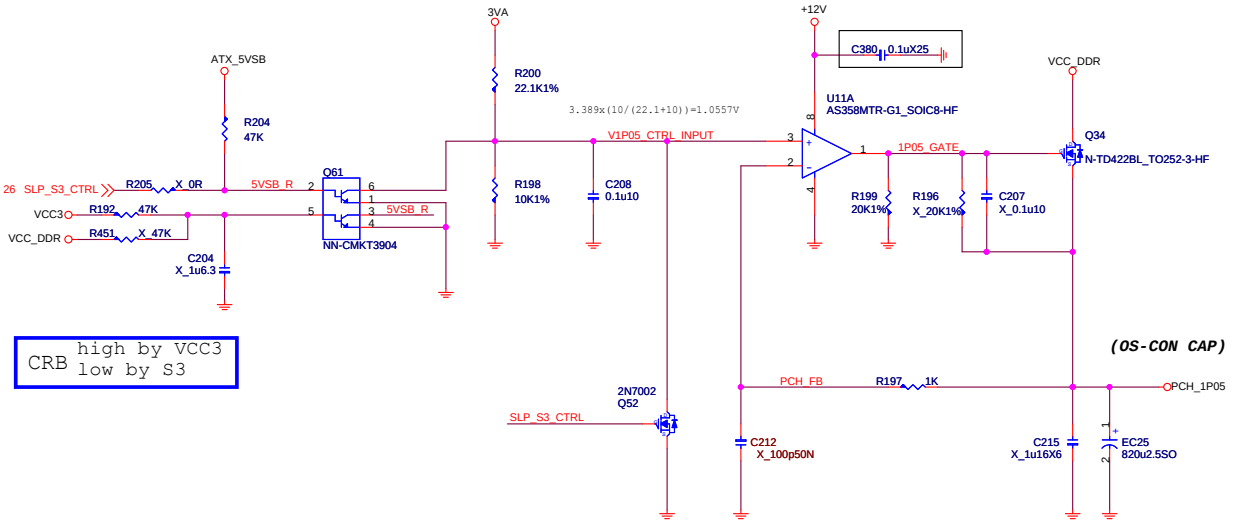
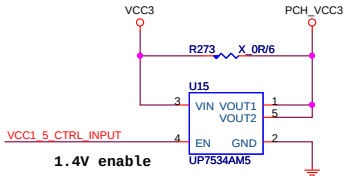
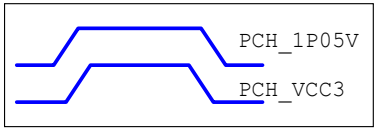
PCH Power:1.05V 5.747A

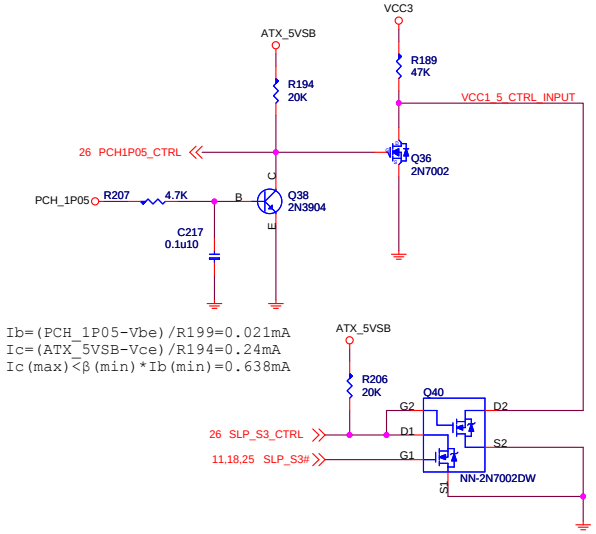


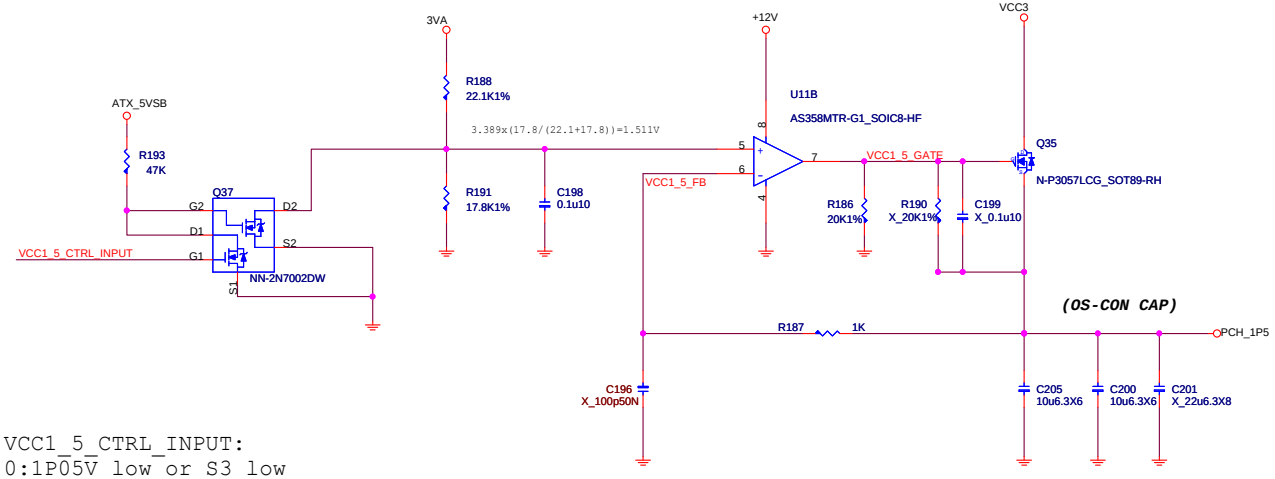
0.133A



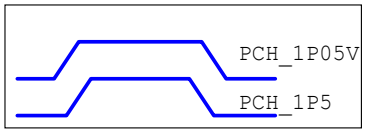


PCH Power:1.5V 0.183A





VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



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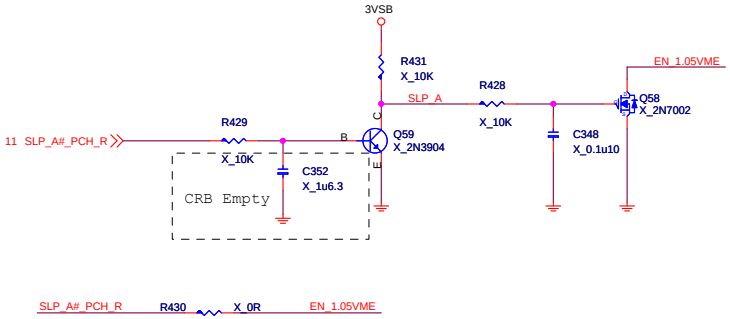
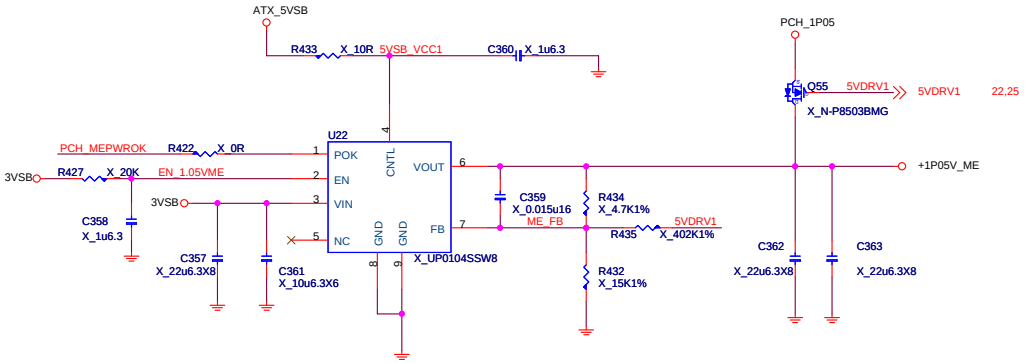
PCH ME Power:1.05V 0.670A

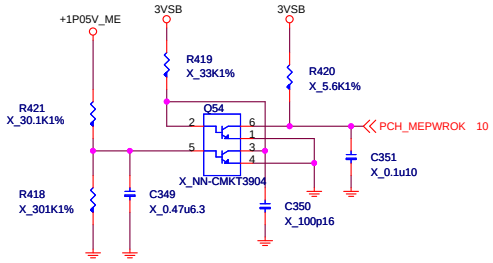
SLP_A

ME Power Control

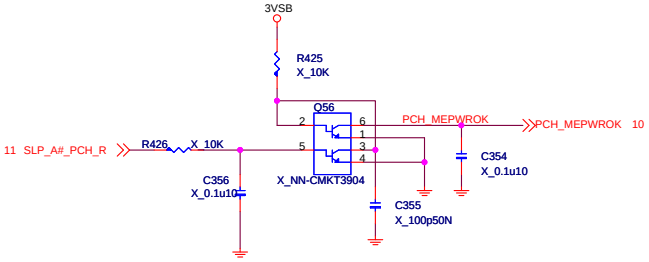




PCH_MEPWROK

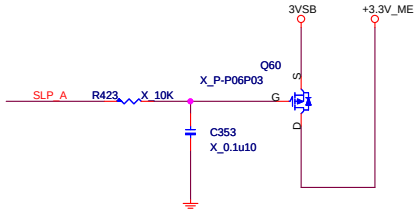


VccASW active to APWROK high 1ms

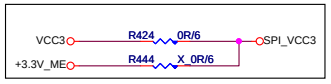


APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME



H81 stuff R424
B85 stuff R444

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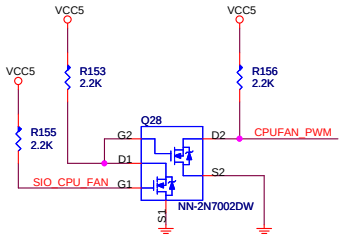
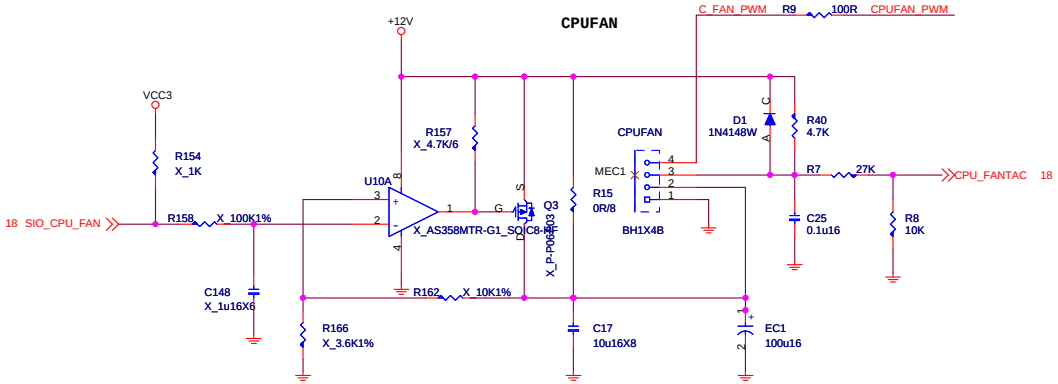
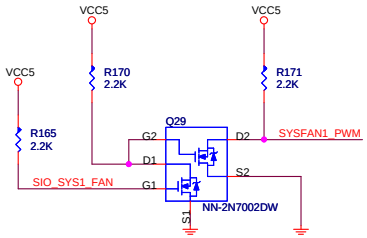
FAN-COUNTROL CIRCUIT

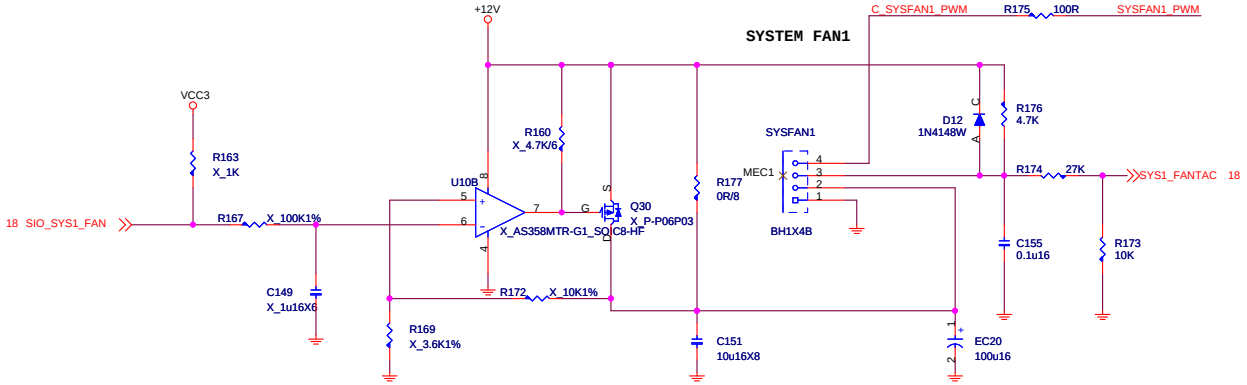


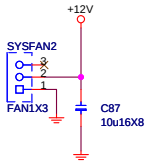
FAN TYPE E





FAN TYPE E





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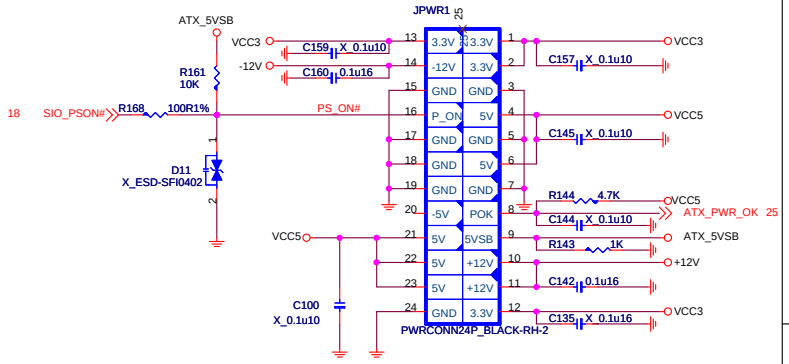
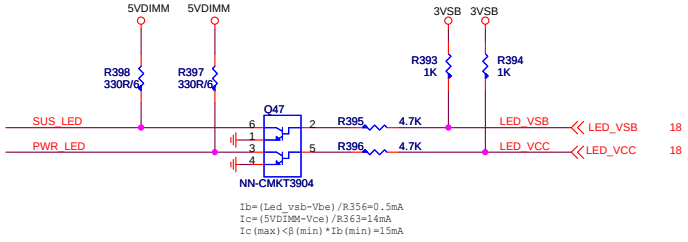
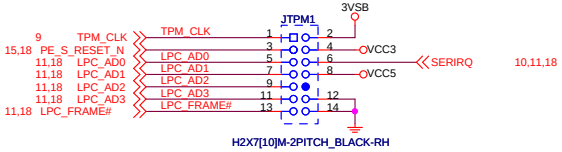
ATX_POWER_CONNECTOR



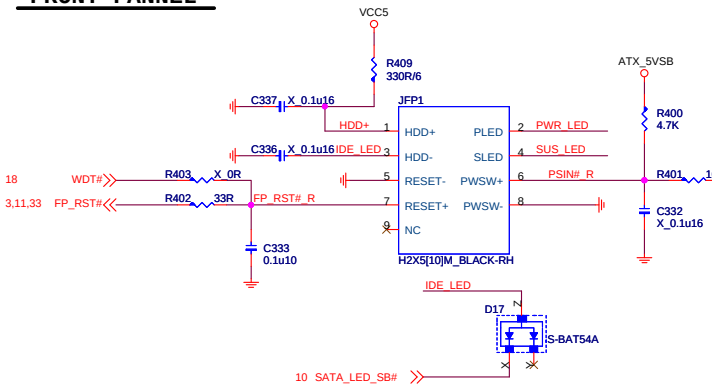
LED (for NV5533)



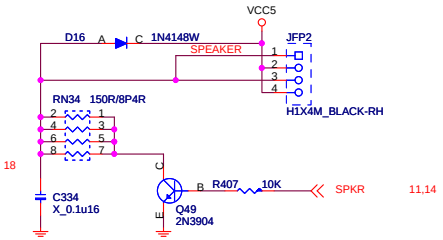
TPM/JLPC



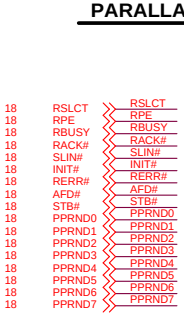
FRONT_PANNEL

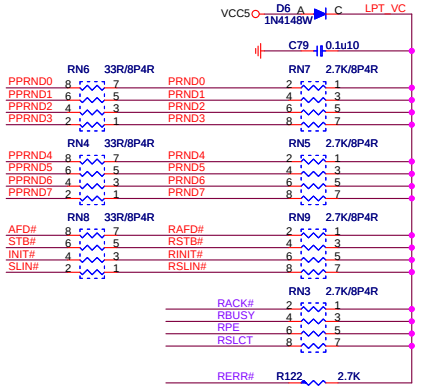


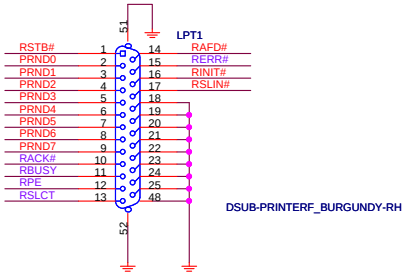
Speaker Pin Header

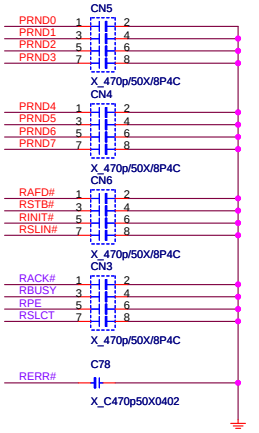


PARALLAL PORT









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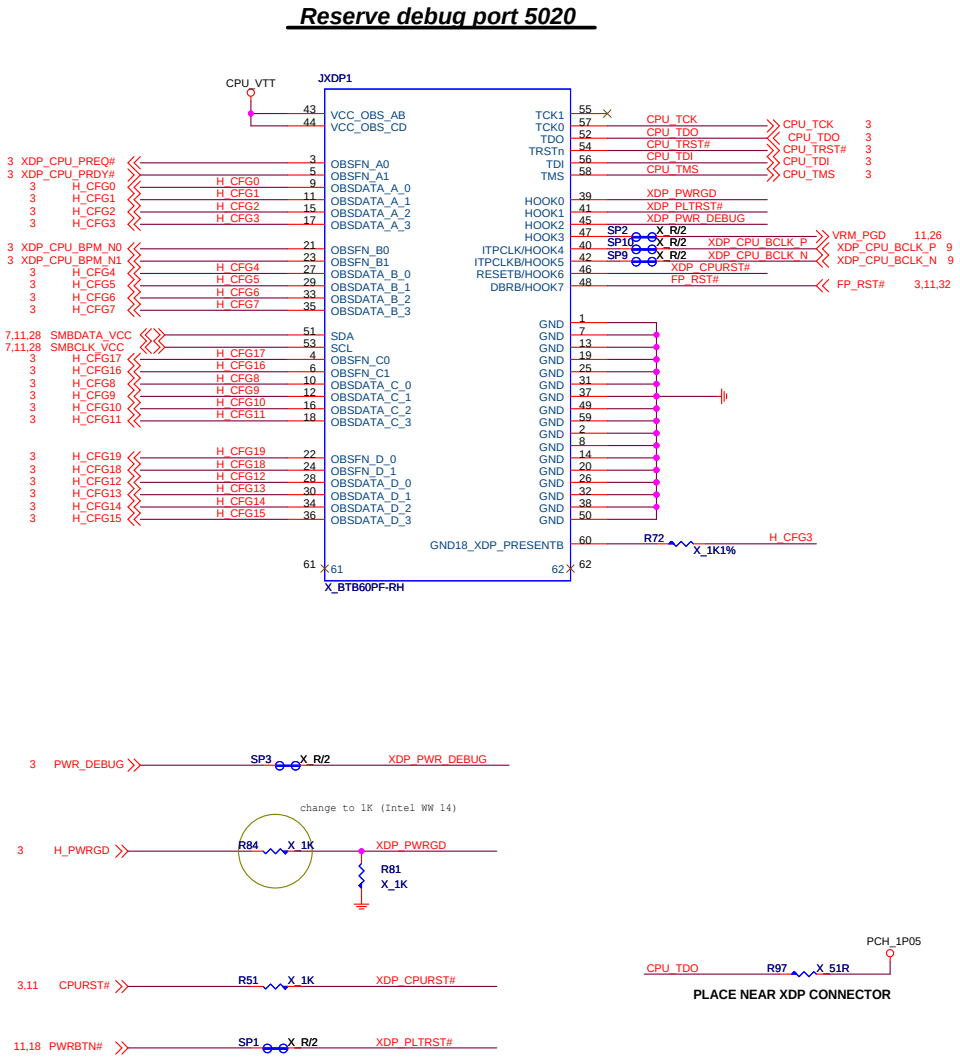

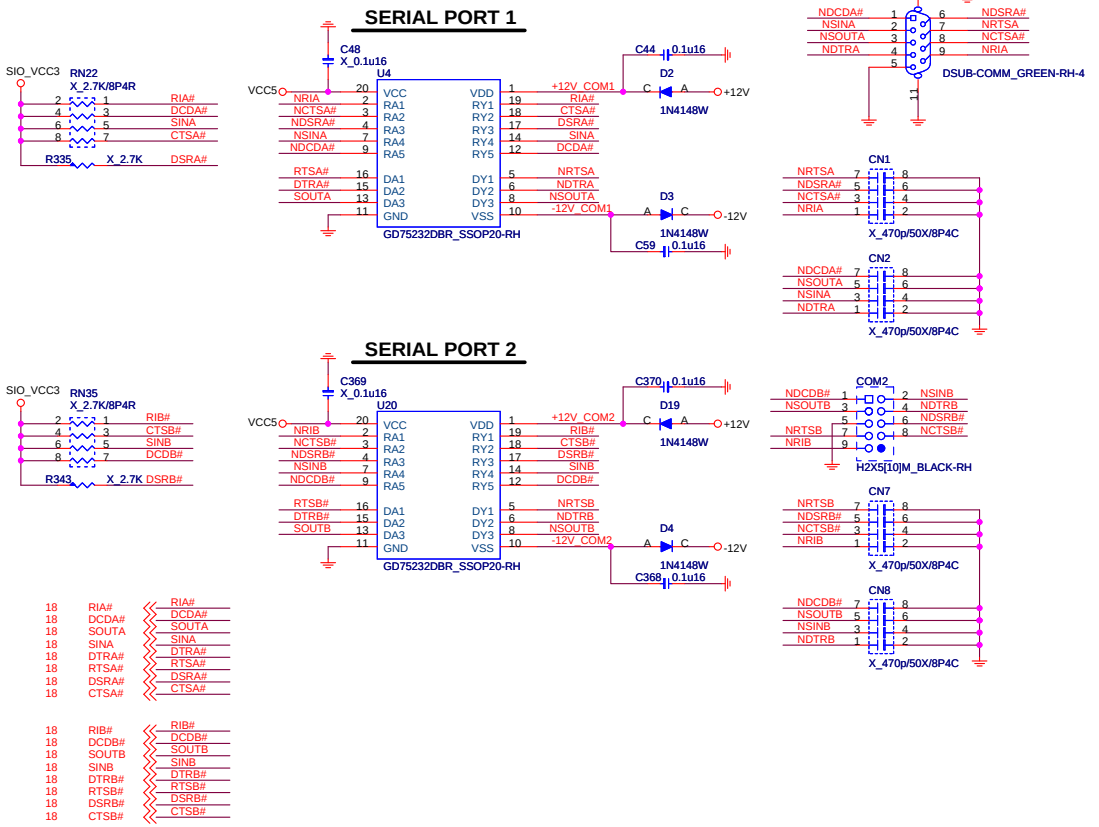

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SPI OPT.

SPI10
SPI 16M
X_W25Q128FVSIQ-HF

D1000
MOS
X_N-AO3414

CHIPSET OPT.

U1001
H87
X_H87 QS

U1002
B85
X_B85 QS

LABEL OPT.

LABEL100
H87
X_LABEL

LABEL101
B85
X_LABEL

MK1
G51-M1SPE13-Q13

LA3
AMI_BIOS LABLE
BIOS_LABLE

BAT1_X1
BAT-BCR2032P-RH

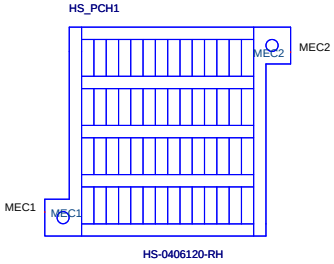
PCB1

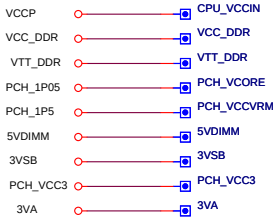
7846_10
PK0-0784610-G37
PK0-0784610-E48

CPU_H1
CPU
鍍座
CPU_H1

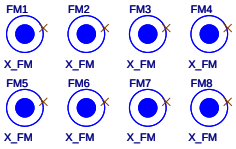
Simulation

PCH XDP PWRGD/RESET

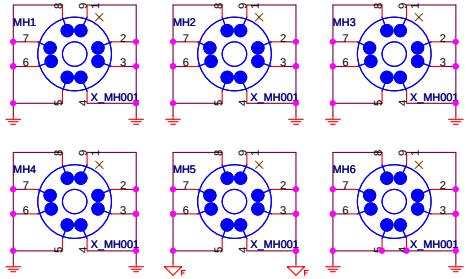




Optical Fiducial Marks-120



Mounting Holes



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