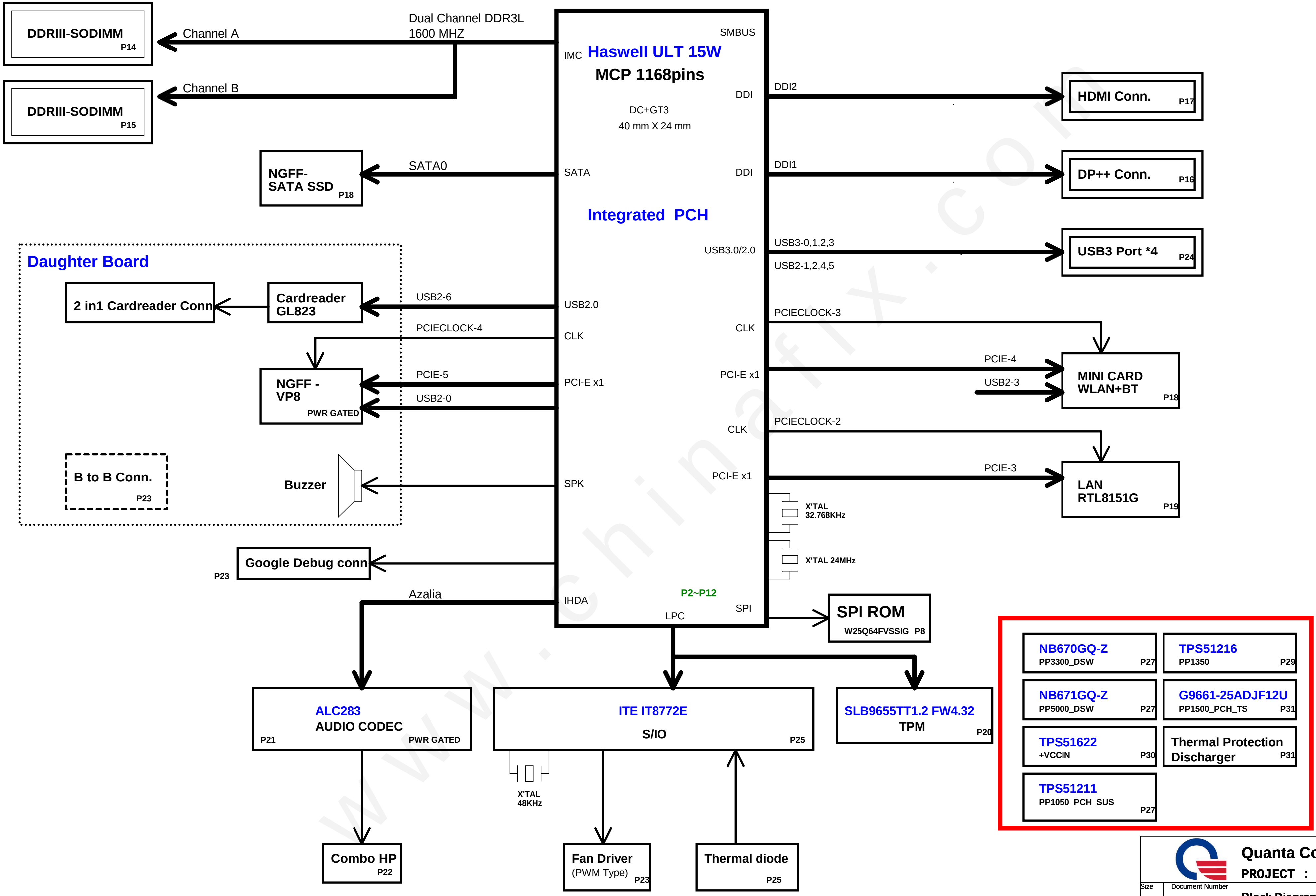
ZAKO/0W9 SHB ULT SYSTEM BLOCK DIAGRAM

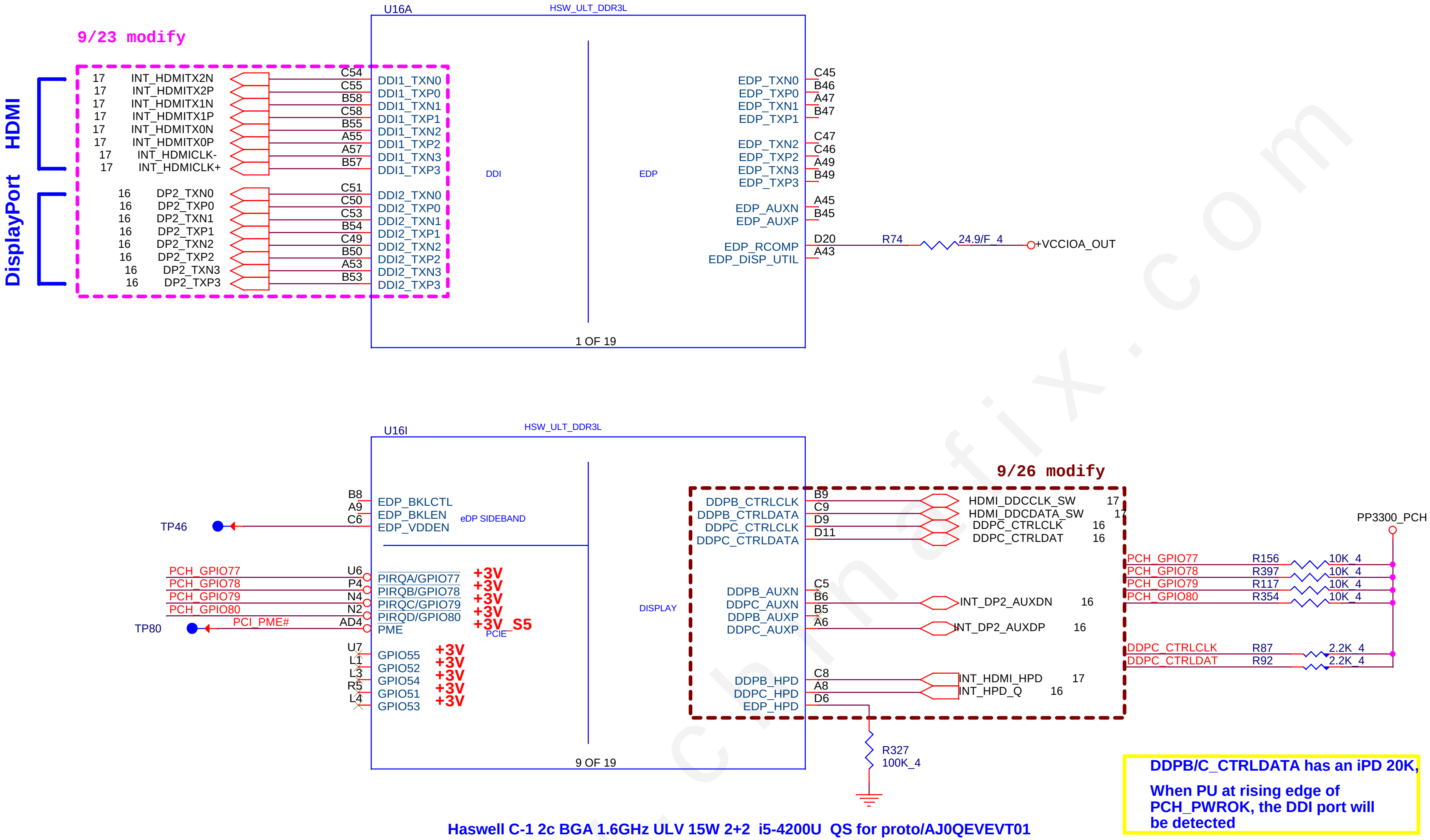


Quanta Computer Inc.

PROJECT : 0W9

Size	Document Number	Rev
	Block Diagram	3A
Date: Monday, February 17, 2014	Sheet 1 of 33	

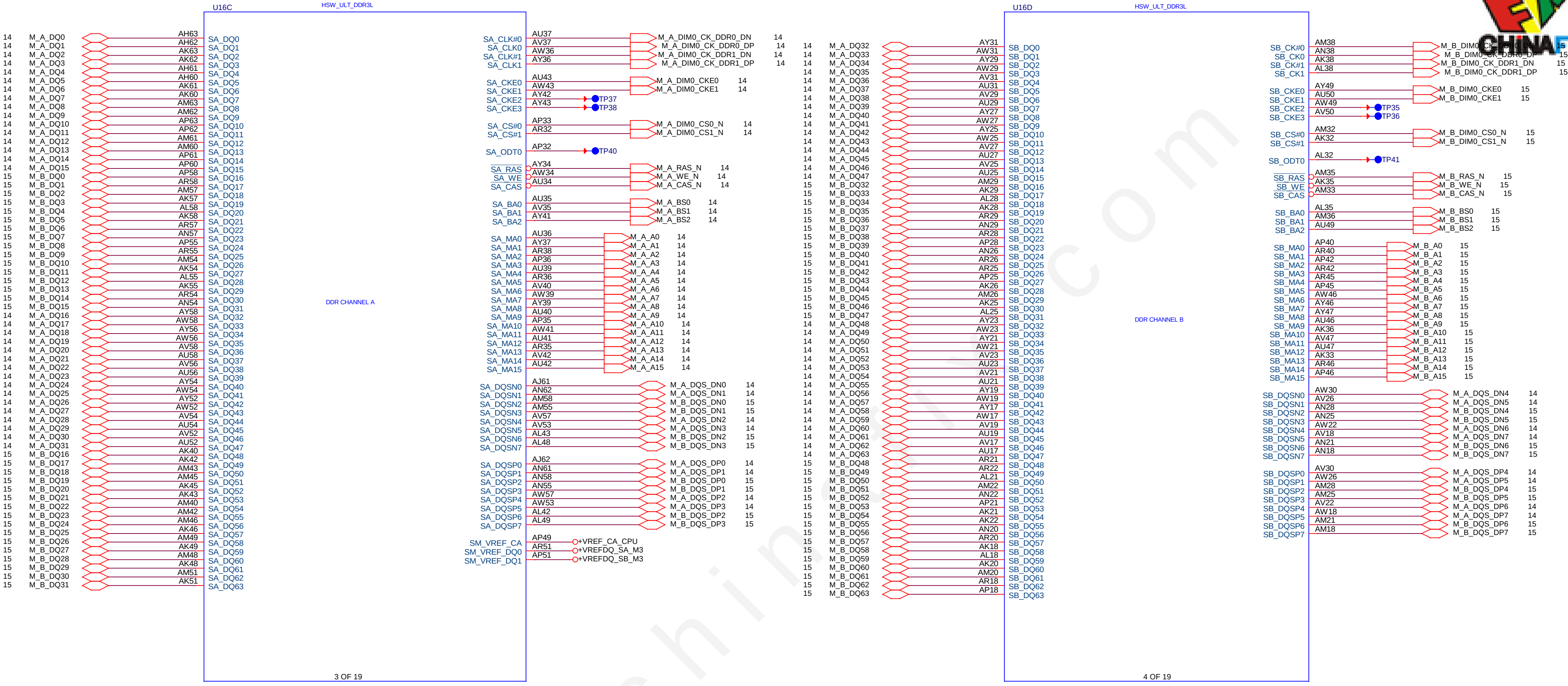
Haswell ULT (DISPLAY,eDP)



Quanta Computer Inc. PROJECT : 0W9		
Size	Document Number: Haswell 1/5 (DDI/eDP)	Rev 3A
Date: Monday, February 17, 2014	Sheet 2 of 33	

Haswell ULT (DDR3L)

Haswell Processor (DDR3L)



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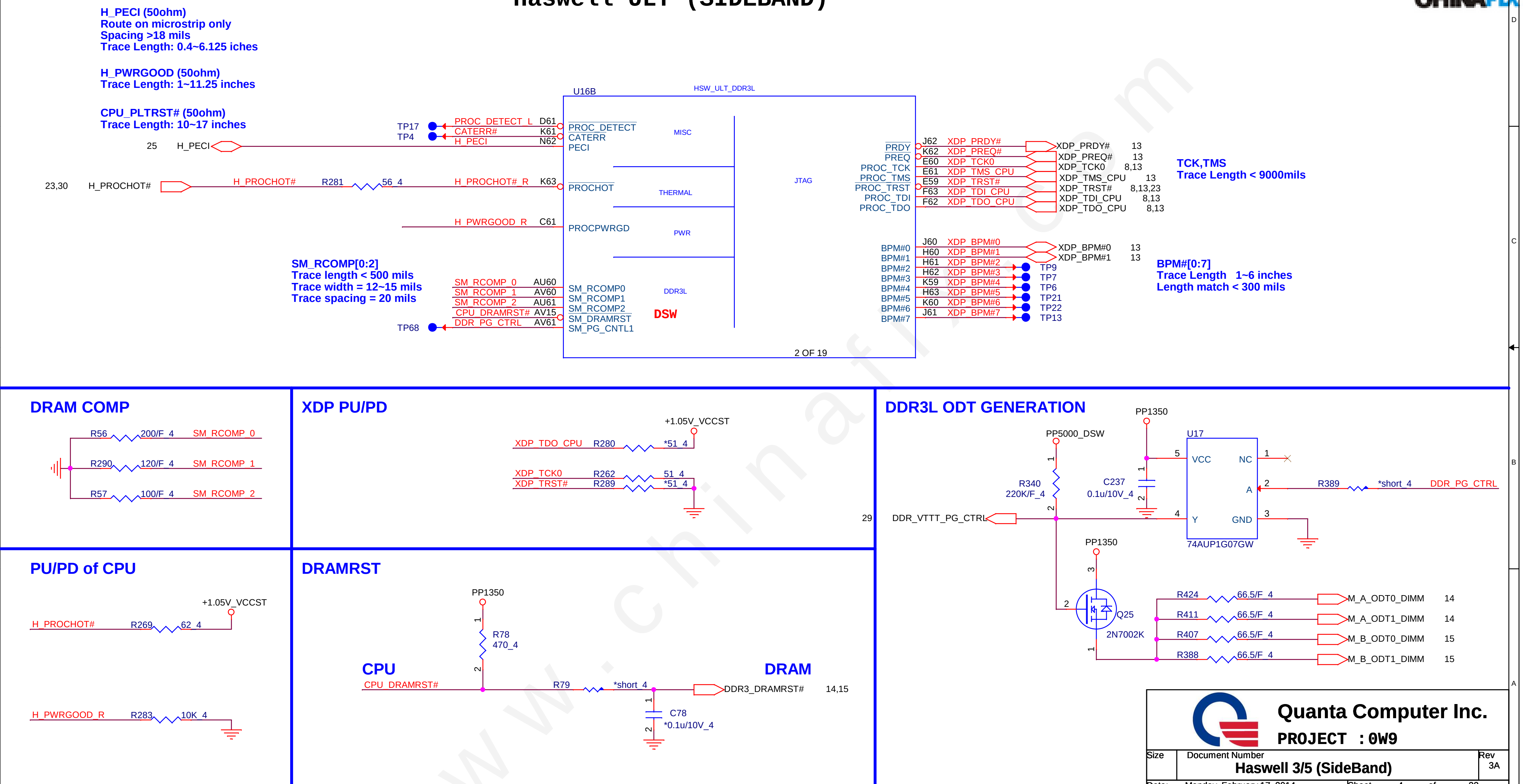
Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A
Date: Monday, February 17, 2014	Sheet 3 of 33	

Haswell ULT (SIDEBAND)



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PROJECT : 0W9

Size	Document Number	Rev
	Haswell 3/5 (SideBand)	3A

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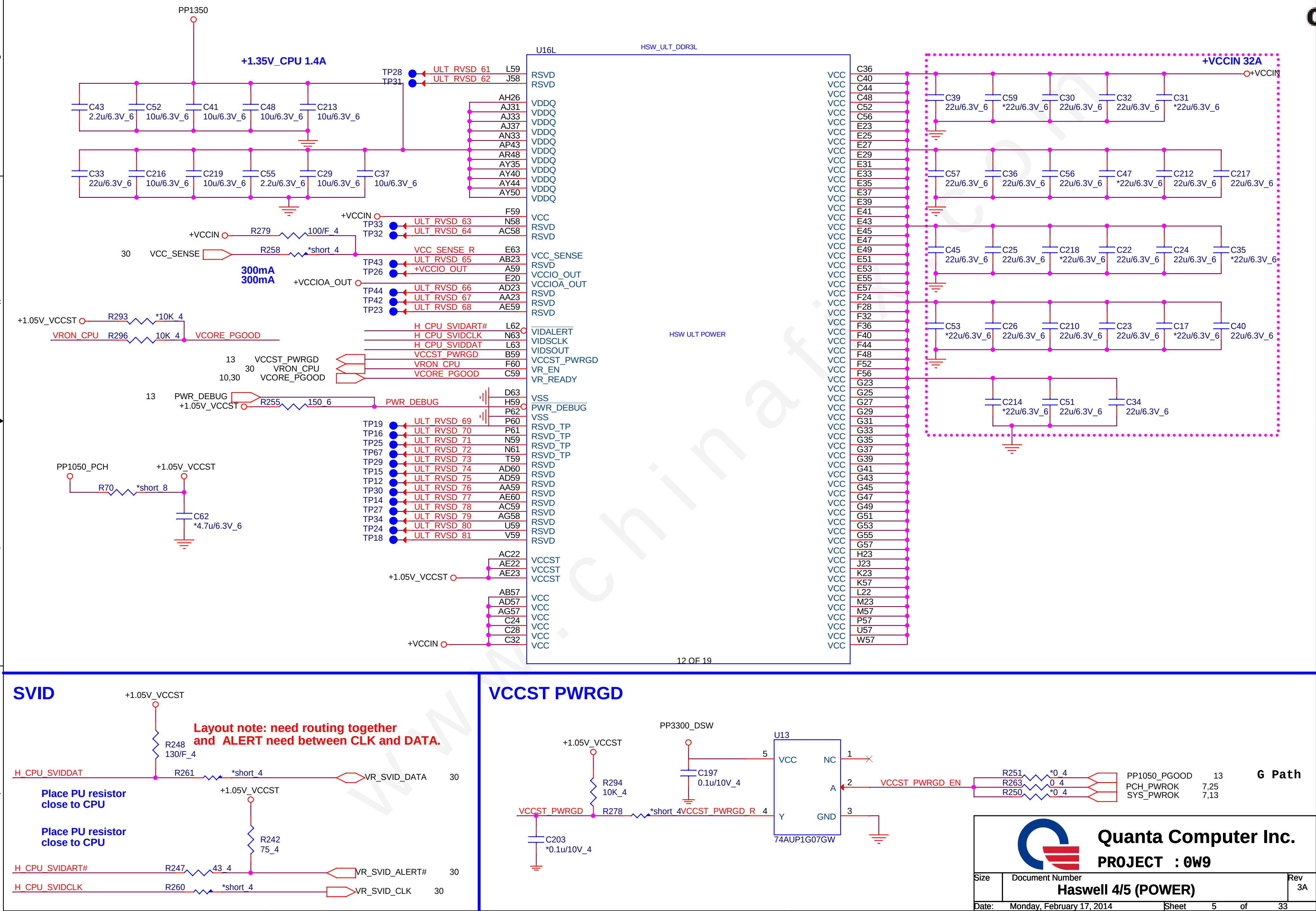
Haswell ULT (POWER)



Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A

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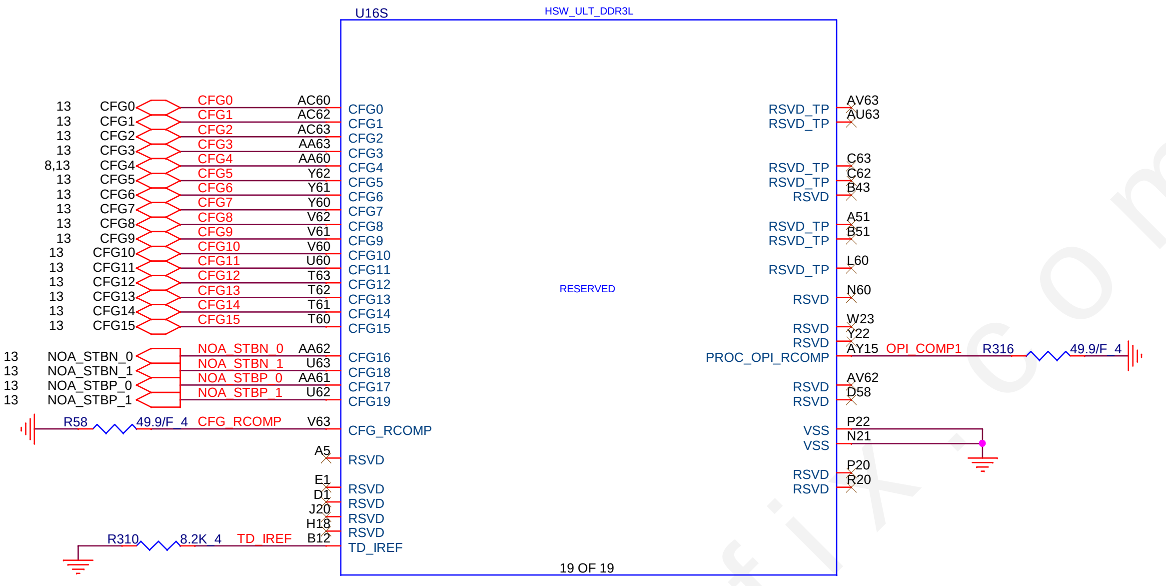
Date: Monday, February 17, 2014 Sheet 5 of 33

Haswell ULT (CFG,RSVD)



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R268 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R264 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R265 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R53 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R54 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R50 *1K_4

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Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
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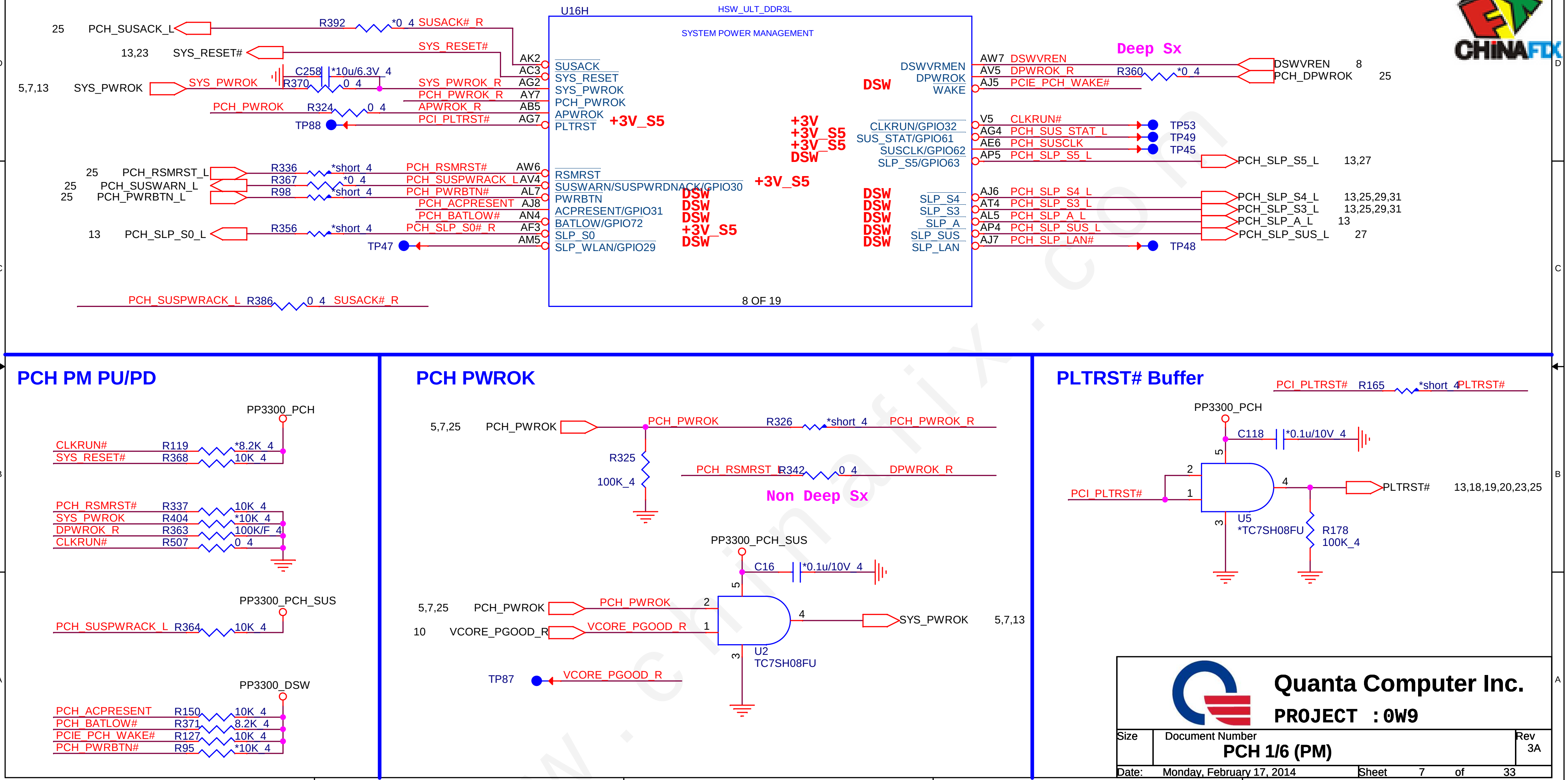
Haswell ULT PCH (PM)



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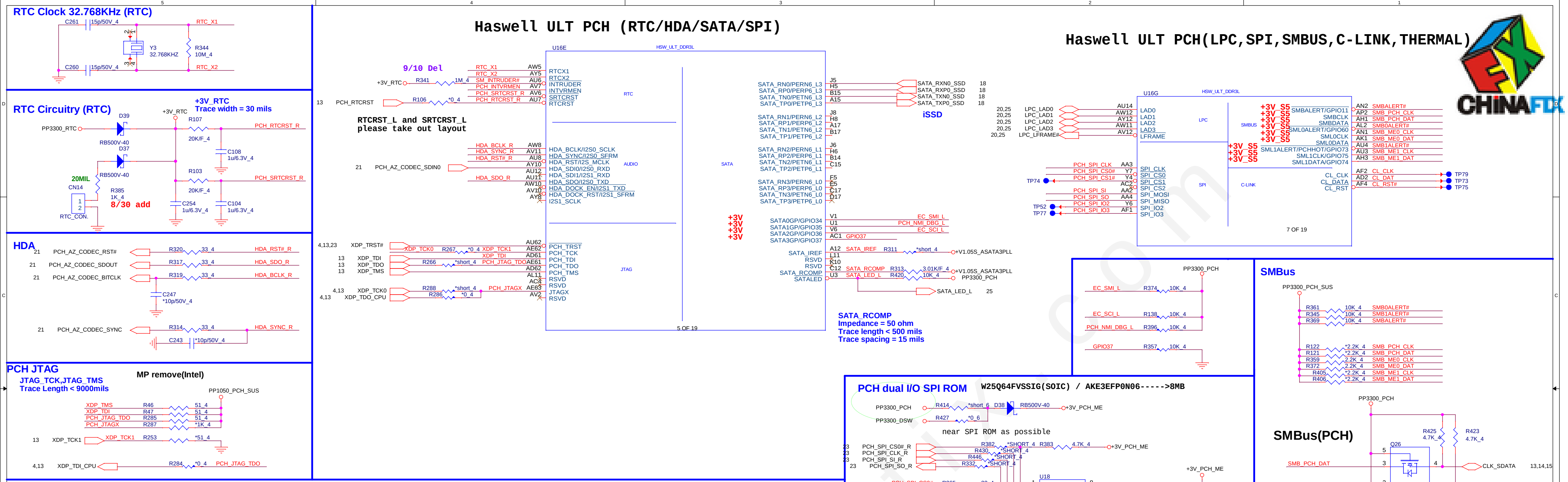
Size	Document Number	Rev
	PCH 1/6 (PM)	3A

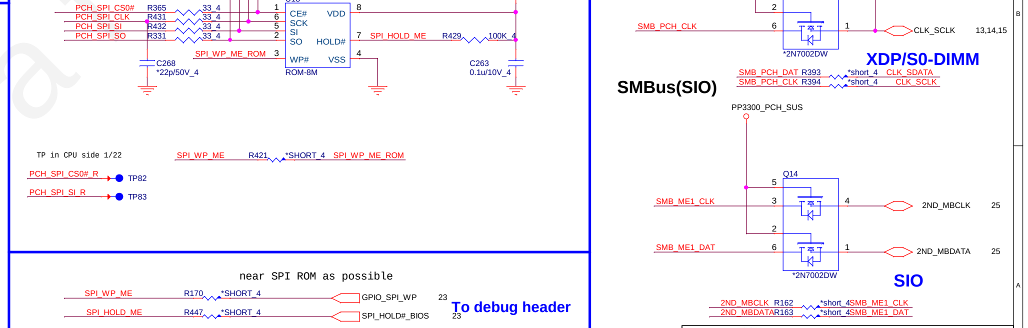
Date: Monday, February 17, 2014 Sheet 7 of 33



ULT Strapping Table

Note: R493 need stuff on MP.

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	PP3300_PCH R348 *1K_4 SPKR SPKR 10,21,23
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R318 *1K_4 PP3300_PCH
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R322 330K_4 PCH_INTVRMEN R321 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	10 GPIO66 PP3300_PCH R403 *1K_4 GPIO66 R375 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	10 GPIO86 PP3300_PCH R125 *1K_4 GPIO86 R146 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	10 GPIO15 PP3300_PCH_SUS R143 *8.2K_4 x86 stuff GPIO15 R130 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	6,13 CFG4 CFG4 R52 *1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	7 DSWVREN +3V_RTC R330 330K_4 DSWVREN R329 *330K_4



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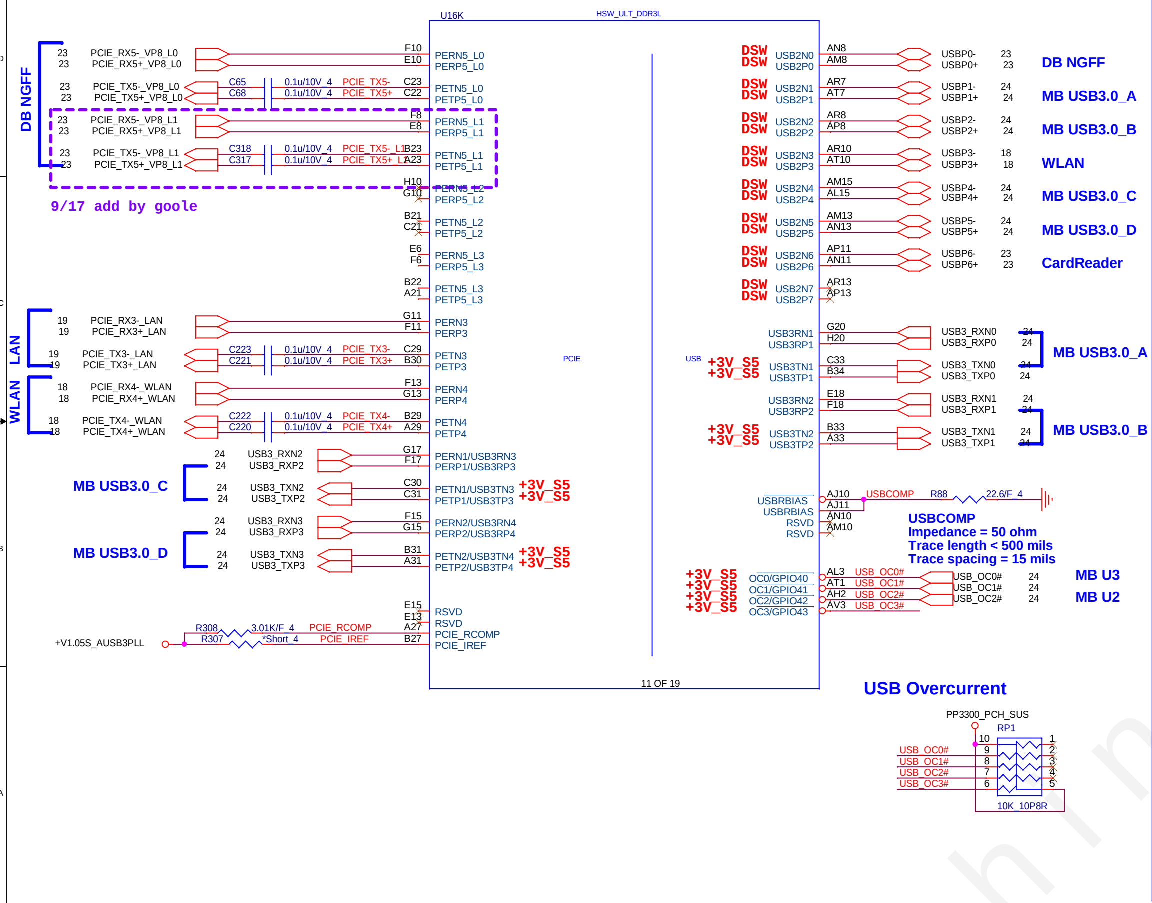
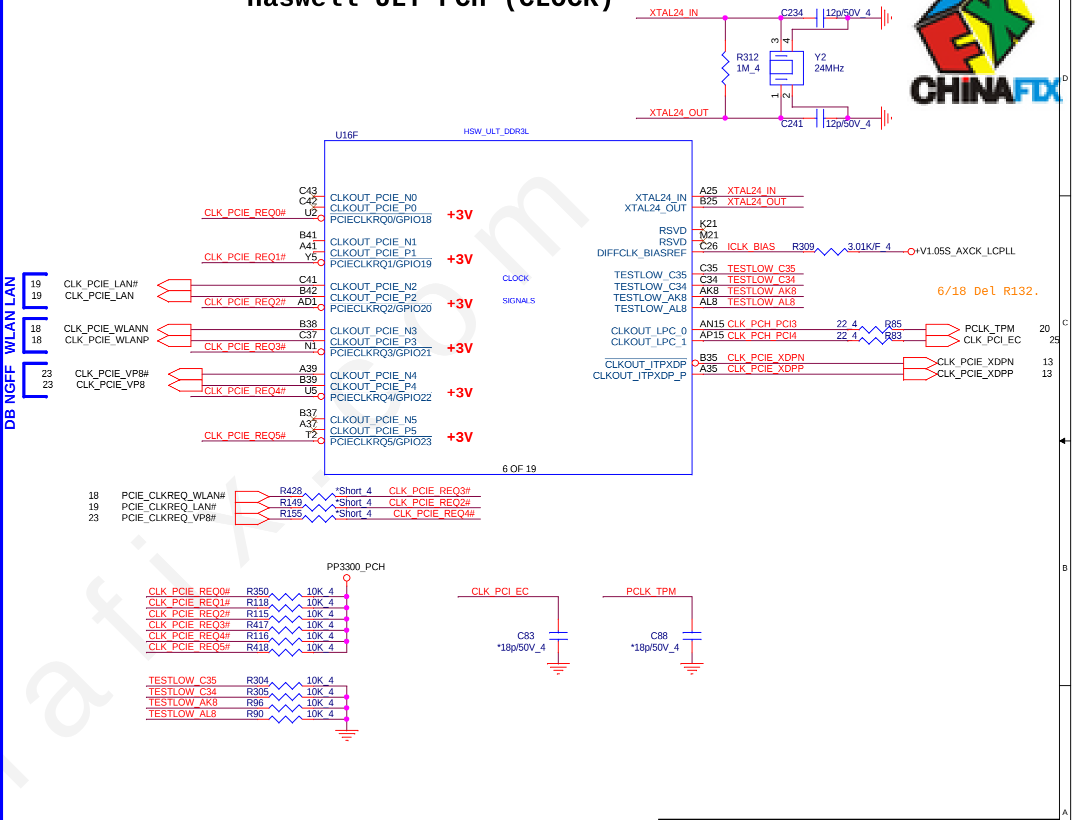
Document Number: PCH 2/6 (RTC/HDA/SATA/SPI)
Rev 3A
Date: Monday, February 17, 2014 Sheet 8 of 33

Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)



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PROJECT : 0W9		
Size	Document Number: PCH 3/6 (PCIE/USB/CLK)	Rev 3A
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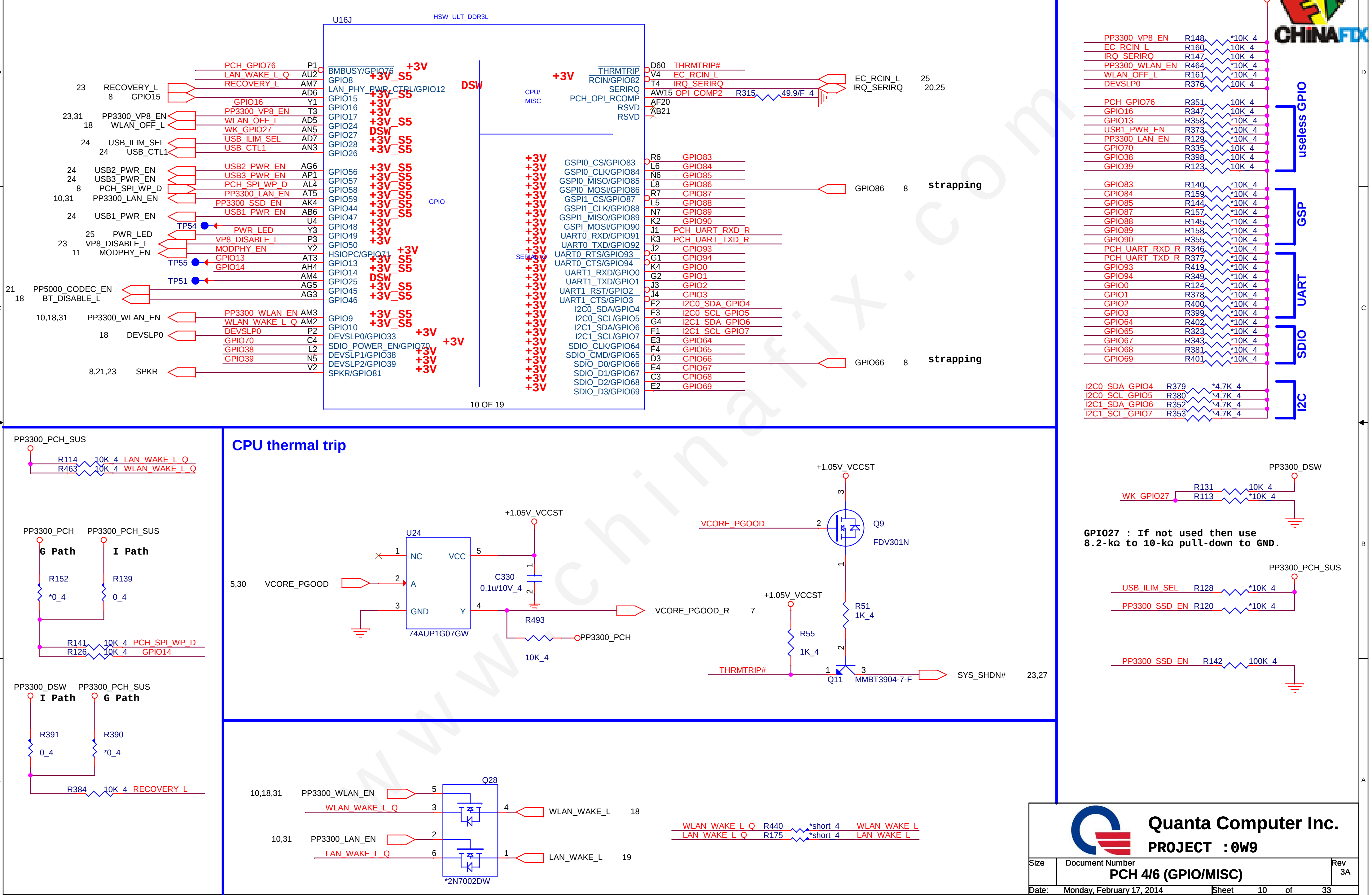
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)



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PROJECT : 0W9

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	3A

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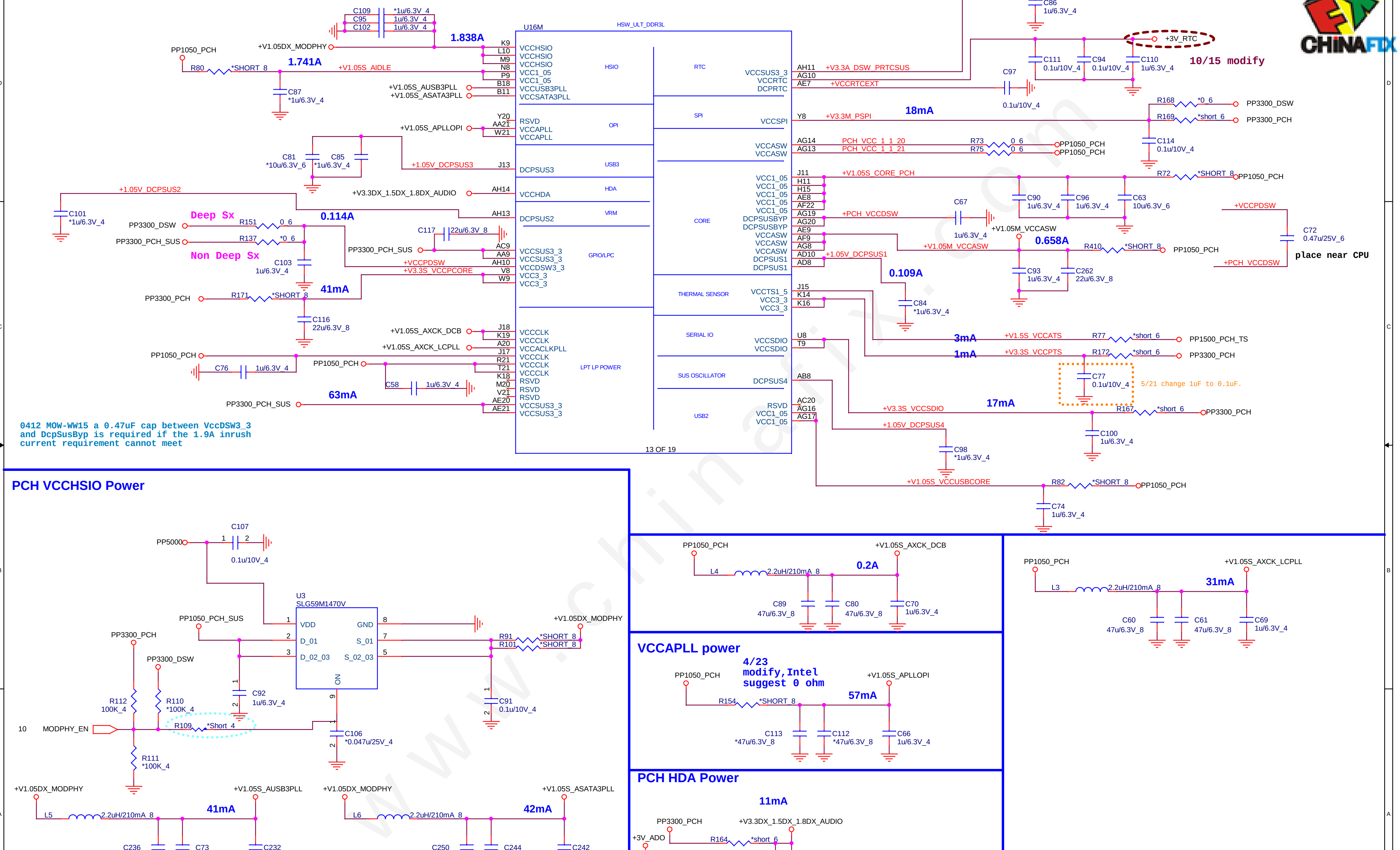
Haswell ULT PCH (Power)



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PROJECT : 0W9

Size	Document Number	Rev
	PCH 5/6 (POWER)	3A

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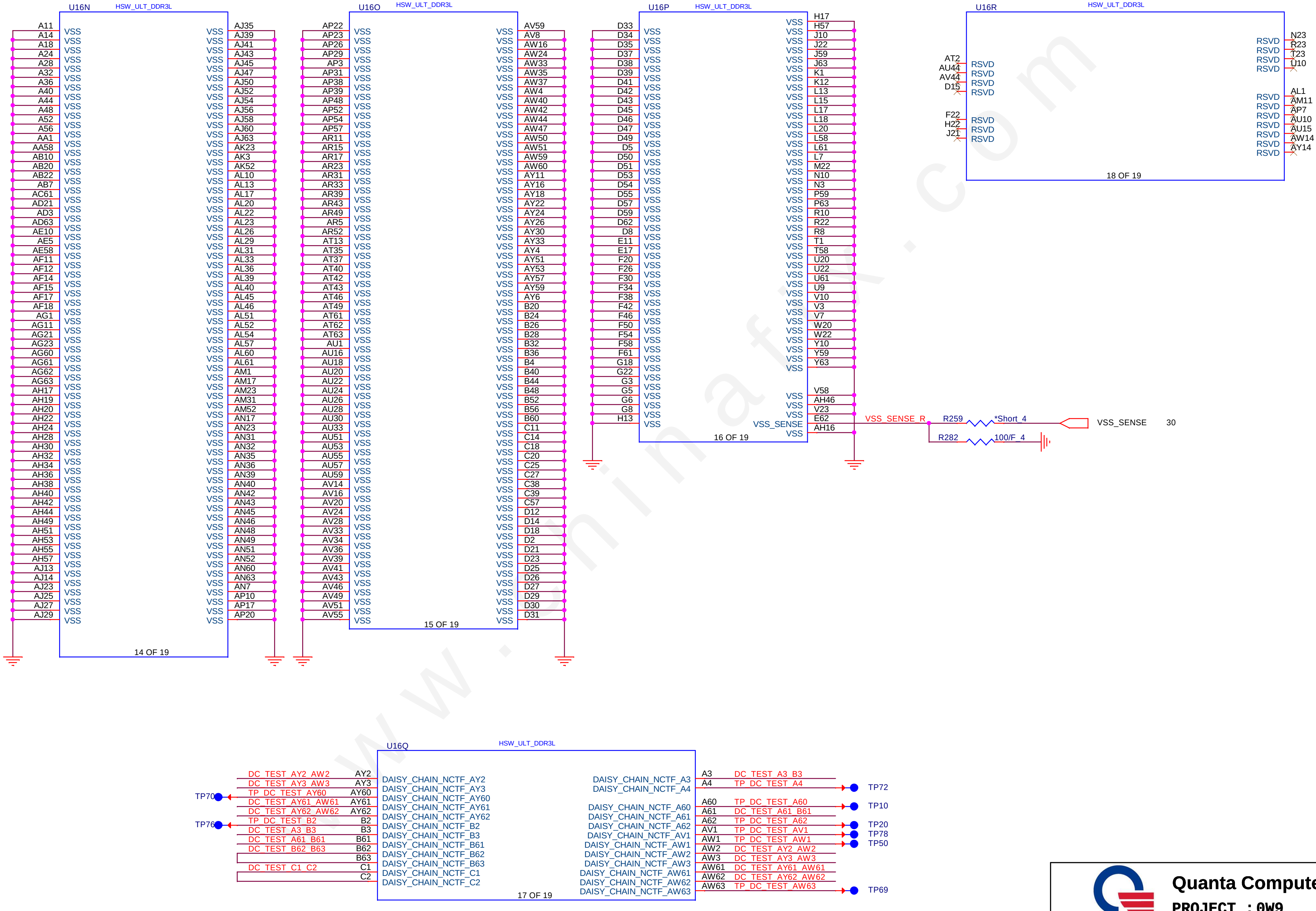
Haswell ULT (GND)



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Size	Document Number	Rev
	PCH 6/6 (GND)	3A

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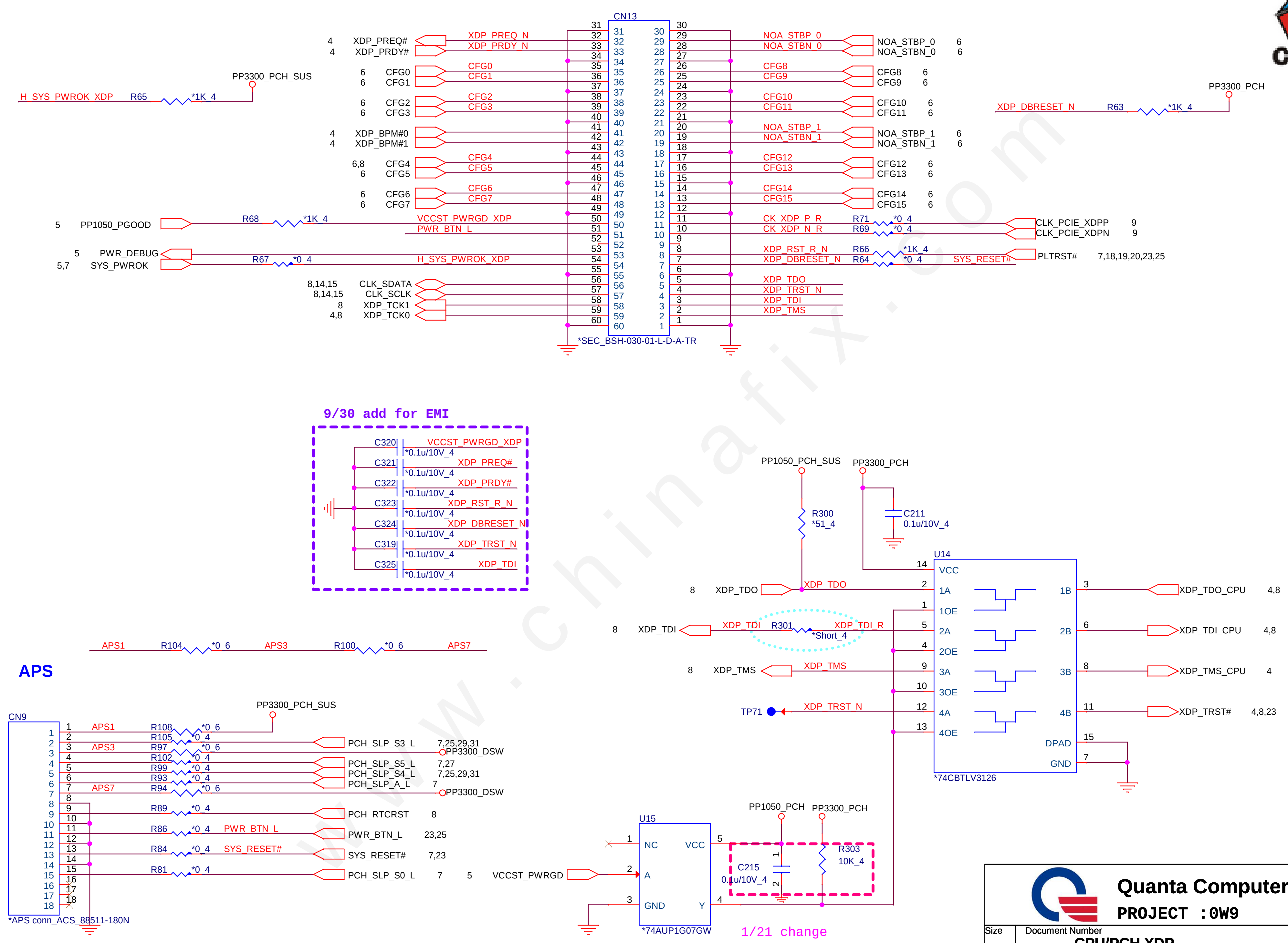
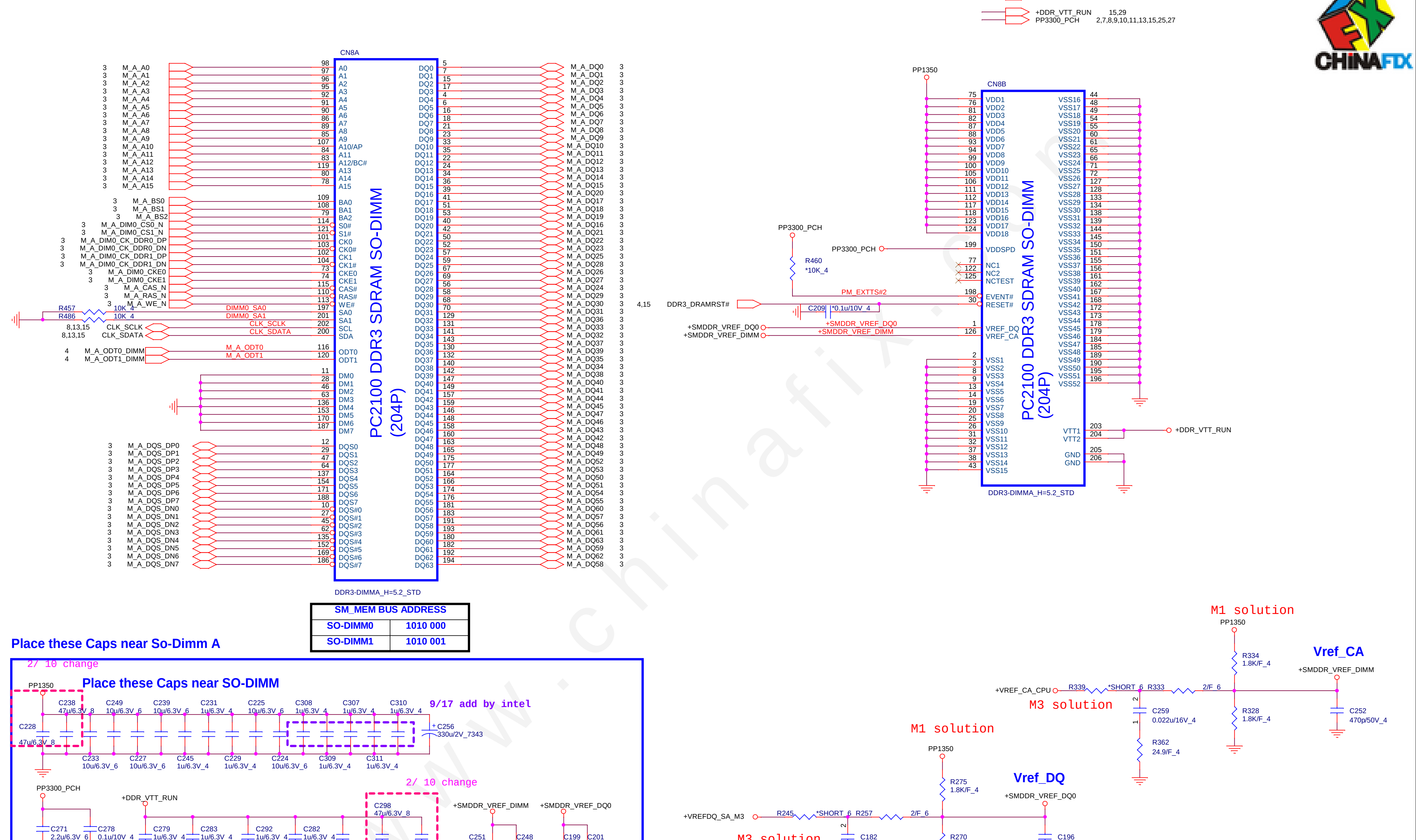

CN13
*SEC_BSH-030-01-L-D-A-TR
XDP_PREQ#
XDP_PRDY#
XDP_PREQ_N
XDP_PRDY_N
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7
XDP_BPM#0
XDP_BPM#1
CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15
NOA_STBP_0
NOA_STBN_0
NOA_STBP_1
NOA_STBN_1
PP3300_PCH_SUS
H_SYS_PWROK_XDP
R65 *1K_4
PP3300_PCH
XDP_DBRESET_N
R63 *1K_4
PP1050_PGOOD
R68 *1K_4
VCCST_PWRGD_XDP
PWR_BTN_L
PWR_DEBUG
SYS_PWROK
R67 *0_4
H_SYS_PWROK_XDP
CLK_SDATA
CLK_SCLK
XDP_TCK1
XDP_TCK0
CK_XDP_P_R
CK_XDP_N_R
R71 *0_4
R69 *0_4
CLK_PCIE_XDPP
CLK_PCIE_XDPN
XDP_RST_R_N
XDP_DBRESET_N
R66 *1K_4
R64 *0_4
SYS_RESET#
PLTRST#
7,18,19,20,23,25
XDP_TDO
XDP_TRST_N
XDP_TDI
XDP_TMS
9/30 add for EMI
C320 C321 C322 C323 C324 C319 C325
*0.1u/10V_4
VCCST_PWRGD_XDP
XDP_PREQ#
XDP_PRDY#
XDP_RST_R_N
XDP_DBRESET_N
XDP_TRST_N
XDP_TDI
PP1050_PCH_SUS
PP3300_PCH
R300 *51_4
C211 0.1u/10V_4
U14
*74CBTLV3126
VCC 1A 1OE 2A 2OE 3A 3OE 4A 4OE 1B 2B 3B 4B DPAD GND
XDP_TDO
XDP_TDI
R301 *Short_4
XDP_TDI_R
XDP_TMS
TP71
XDP_TRST_N
XDP_TDO_CPU 4,8
XDP_TDI_CPU 4,8
XDP_TMS_CPU 4
XDP_TRST# 4,8,23
APS1 R104 *0_6 APS3 R100 *0_6 APS7
APS
CN9
*APS conn_ACS_88511-180N
PP3300_PCH_SUS
R108 *0_6
R105 *0_4
R97 *0_6
R102 *0_4
R99 *0_4
R93 *0_4
R94 *0_6
R89 *0_4
R86 *0_4
R84 *0_4
R81 *0_4
PCH_SLP_S3_L 7,25,29,31
PP3300_DSW
PCH_SLP_S5_L 7,27
PCH_SLP_S4_L 7,25,29,31
PCH_SLP_A_L 7
PCH_RTCRST 8
PWR_BTN_L 23,25
SYS_RESET# 7,23
PCH_SLP_S0_L 7
VCCST_PWRGD
U15
*74AUP1G07GW
NC VCC A GND Y
PP1050_PCH
PP3300_PCH
C215 0.1u/10V_4
R303 10K_4
1/21 change

DDR3 DIMM-A



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

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Size	Document Number	Rev
	DDR3 SO-DIMM A	A1A

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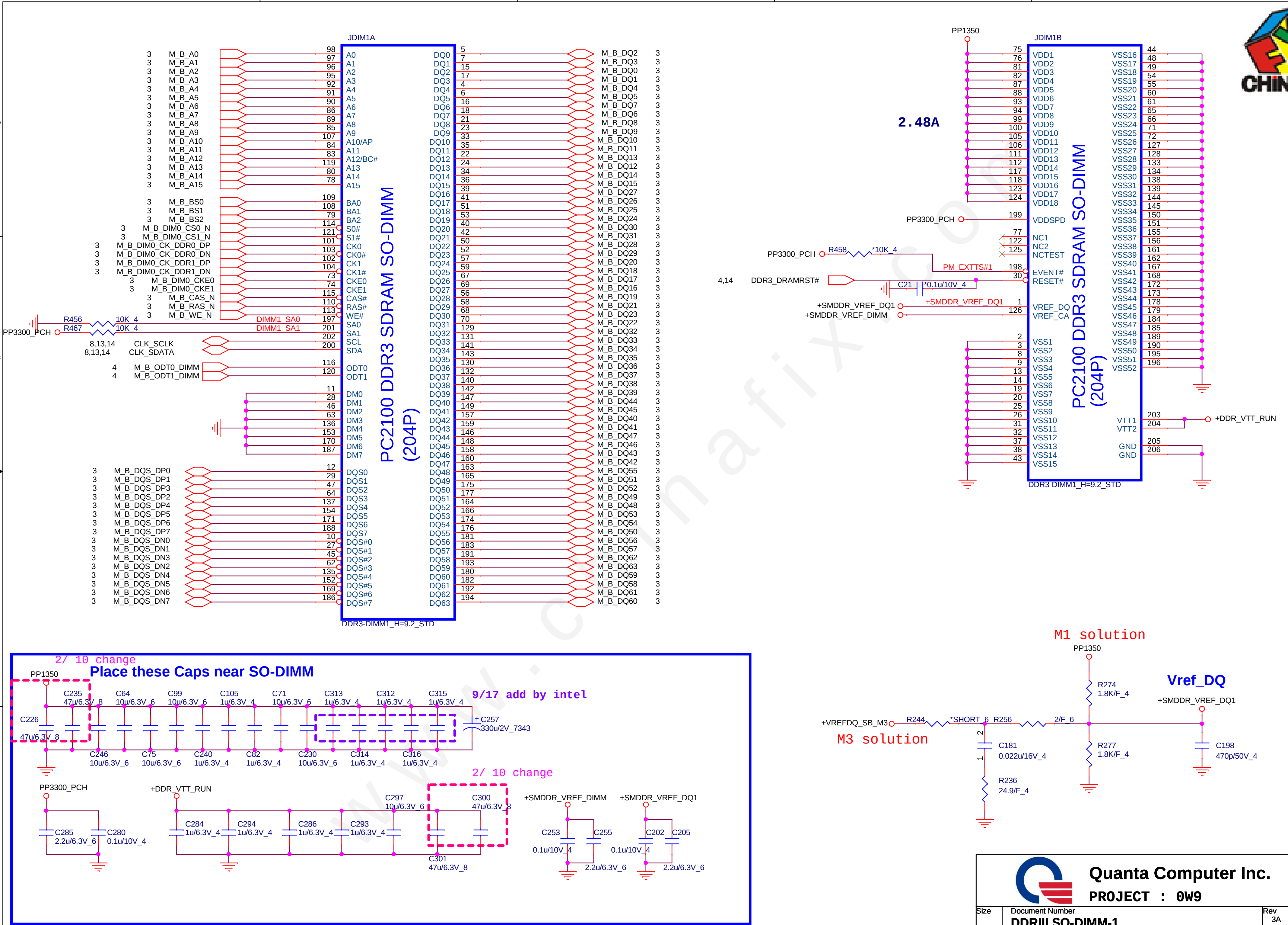

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Size	Document Number	Rev
	DDRIII SO-DIMM-1	3A

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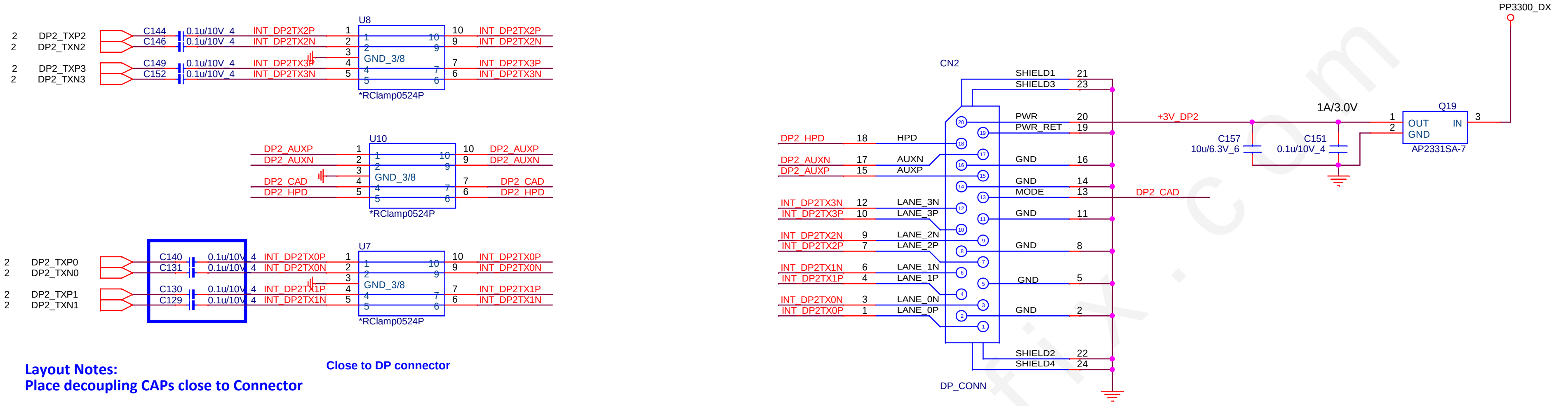
DisplayPort (DPP)

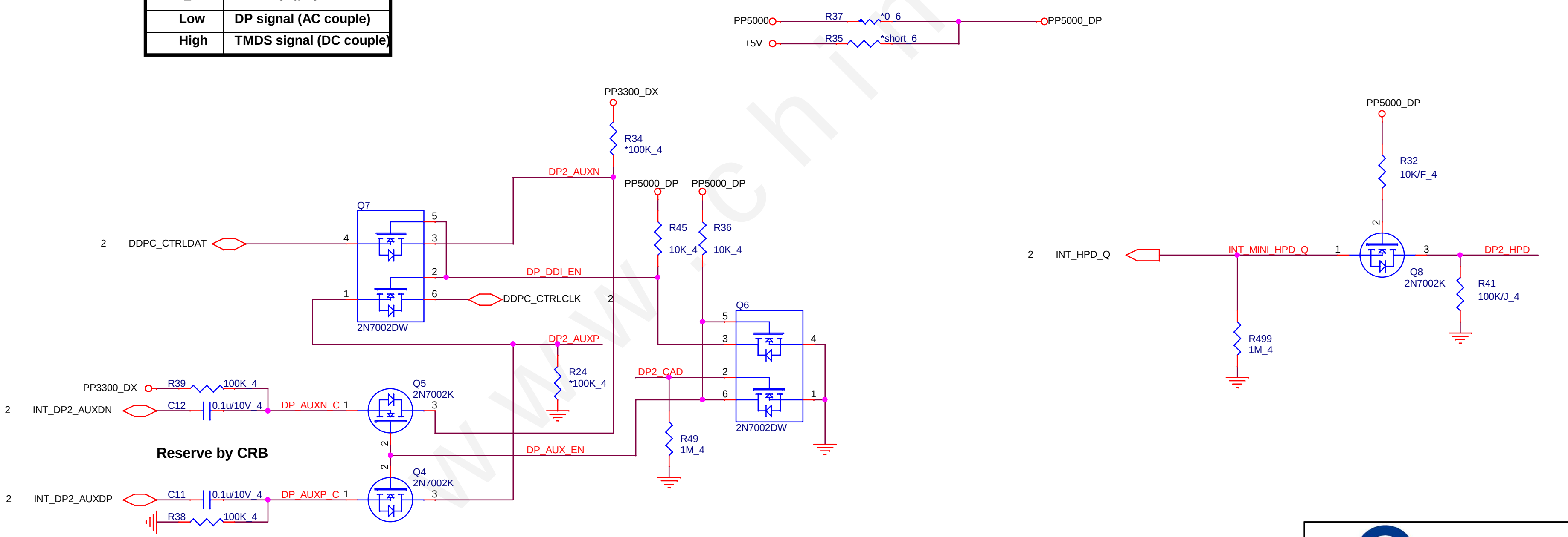


Layout Notes:
Place decoupling CAPs close to Connector

Close to DP connector

DP2 AUX (DPP)

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)



Reserve by CRB

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Size	Document Number	Rev
	DisplayPort	A1A

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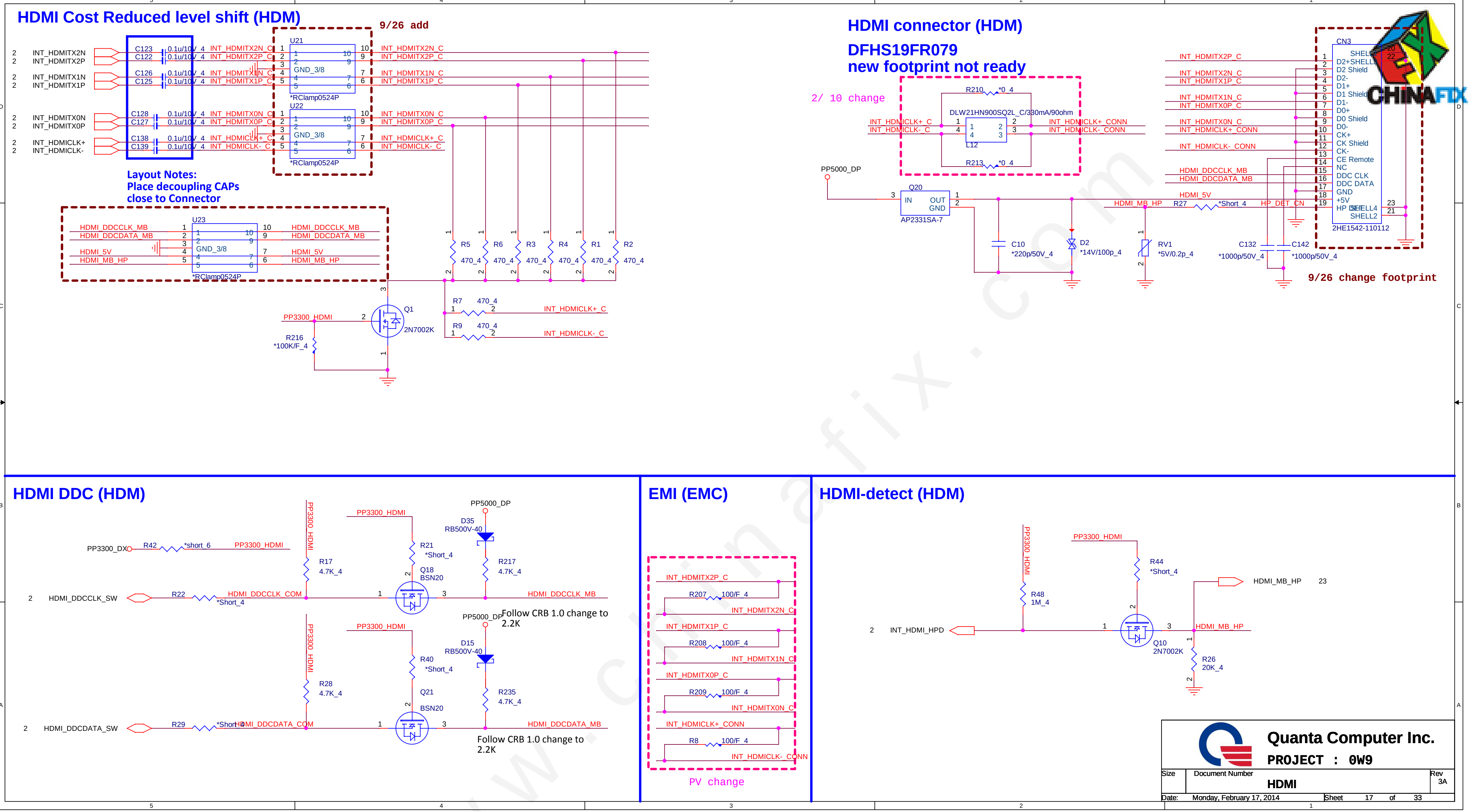
HDMI Cost Reduced level shift (HDM)
9/26 add
INT_HDMITX2N
INT_HDMITX2P
INT_HDMITX1N
INT_HDMITX1P
INT_HDMITX0N
INT_HDMITX0P
INT_HDMICLK+
INT_HDMICLK-
C123 C122 C126 C125 C128 C127 C138 C139
0.1u/10V_4
INT_HDMITX2N_C
INT_HDMITX2P_C
INT_HDMITX1N_C
INT_HDMITX1P_C
INT_HDMITX0N_C
INT_HDMITX0P_C
INT_HDMICLK+_C
INT_HDMICLK-_C
U21
U22
GND_3/8
*RClamp0524P
Layout Notes:
Place decoupling CAPs
close to Connector
U23
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HP
R5 R6 R3 R4 R1 R2
470_4
PP3300_HDMI
R216
*100K/F_4
Q1
2N7002K
R7
R9
HDMI connector (HDM)
DFHS19FR079
new footprint not ready
2/ 10 change
R210
*0_4
DLW21HN900SQ2L_C/330mA/90ohm
INT_HDMICLK+_CONN
INT_HDMICLK-_CONN
L12
R213
PP5000_DP
Q20
IN
OUT
GND
AP2331SA-7
C10
*220p/50V_4
D2
*14V/100p_4
R27
*Short_4
HP_DET_CN
RV1
*5V/0.2p_4
C132
*1000p/50V_4
C142
*1000p/50V_4
9/26 change footprint
CN3
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL4
SHELL2
2HE1542-110112
HDMI DDC (HDM)
PP3300_DX
R42
*short_6
HDMI_DDCCLK_SW
R22
*Short_4
HDMI_DDCCLK_COM
R17
4.7K_4
R21
*Short_4
Q18
BSN20
PP5000_DP
D35
RB500V-40
R217
4.7K_4
Follow CRB 1.0 change to 2.2K
HDMI_DDCDATA_SW
R29
*Short_4
HDMI_DDCDATA_COM
R28
4.7K_4
R40
*Short_4
Q21
BSN20
D15
RB500V-40
R235
4.7K_4
Follow CRB 1.0 change to 2.2K
EMI (EMC)
INT_HDMITX2P_C
R207
100/F_4
INT_HDMITX2N_C
INT_HDMITX1P_C
R208
100/F_4
INT_HDMITX1N_C
INT_HDMITX0P_C
R209
100/F_4
INT_HDMITX0N_C
INT_HDMICLK+_CONN
R8
100/F_4
INT_HDMICLK-_CONN
PV change
HDMI-detect (HDM)
PP3300_HDMI
R48
1M_4
R44
*Short_4
INT_HDMI_HPD
HDMI_MB_HP
Q10
2N7002K
R26
20K_4
Quanta Computer Inc.
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HDMI
Rev
3A
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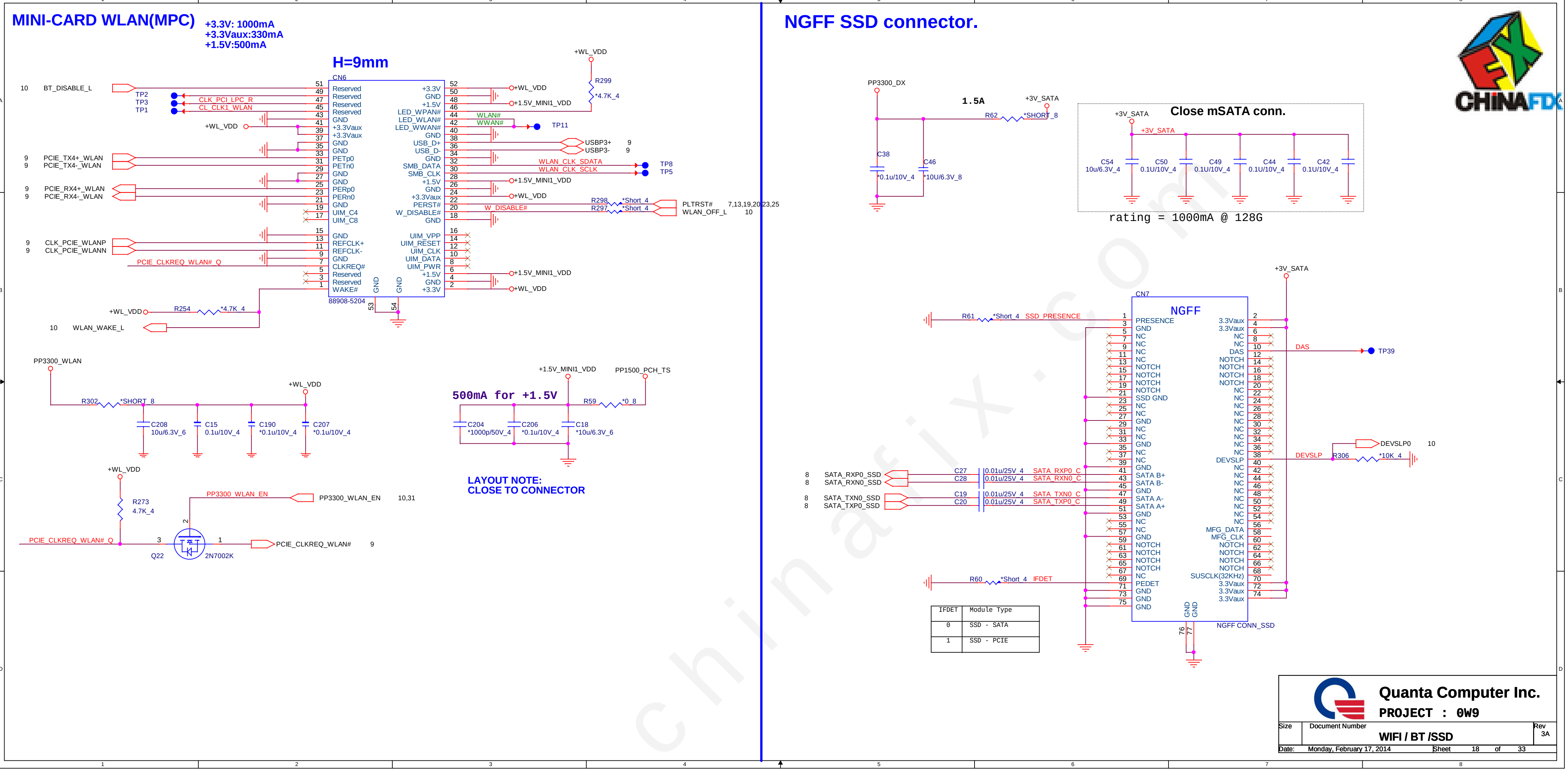

IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE

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Size	Document Number	Rev
	WIFI / BT /SSD	3A

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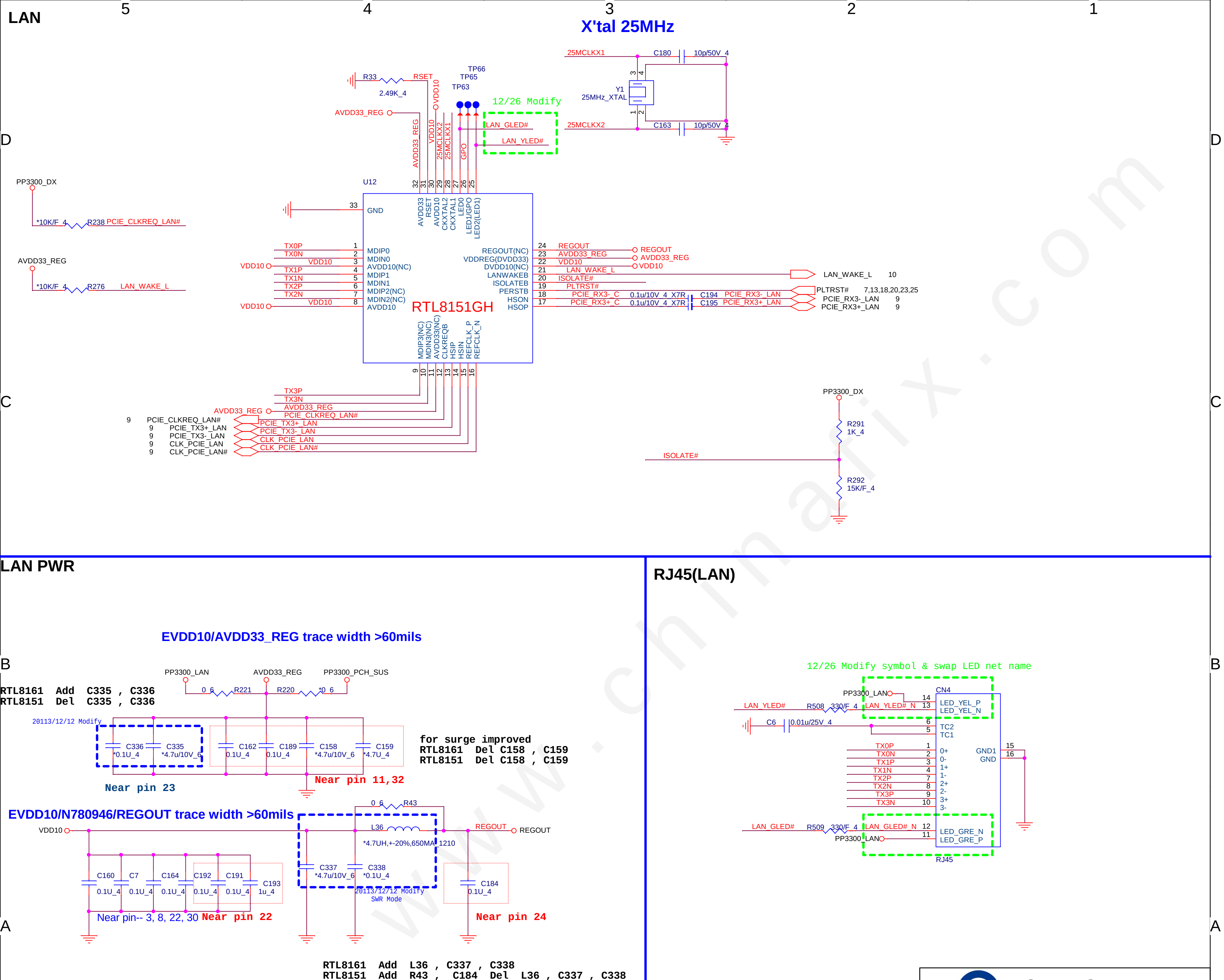

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Size	Document Number	Rev
	LAN (RTL8111G)	3B

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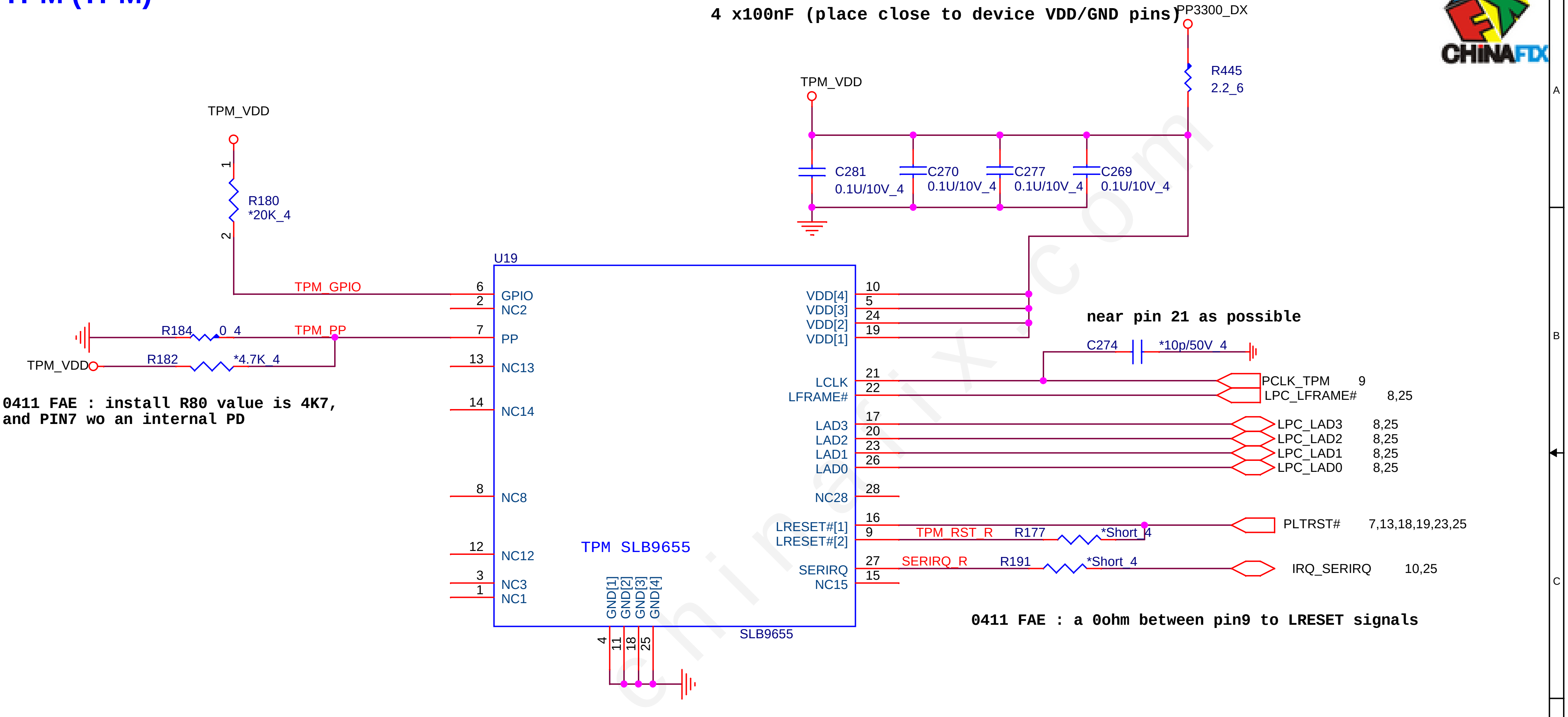
TPM (TPM)



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Size	Document Number	Rev
	TPM SLB9655 / LED	3A

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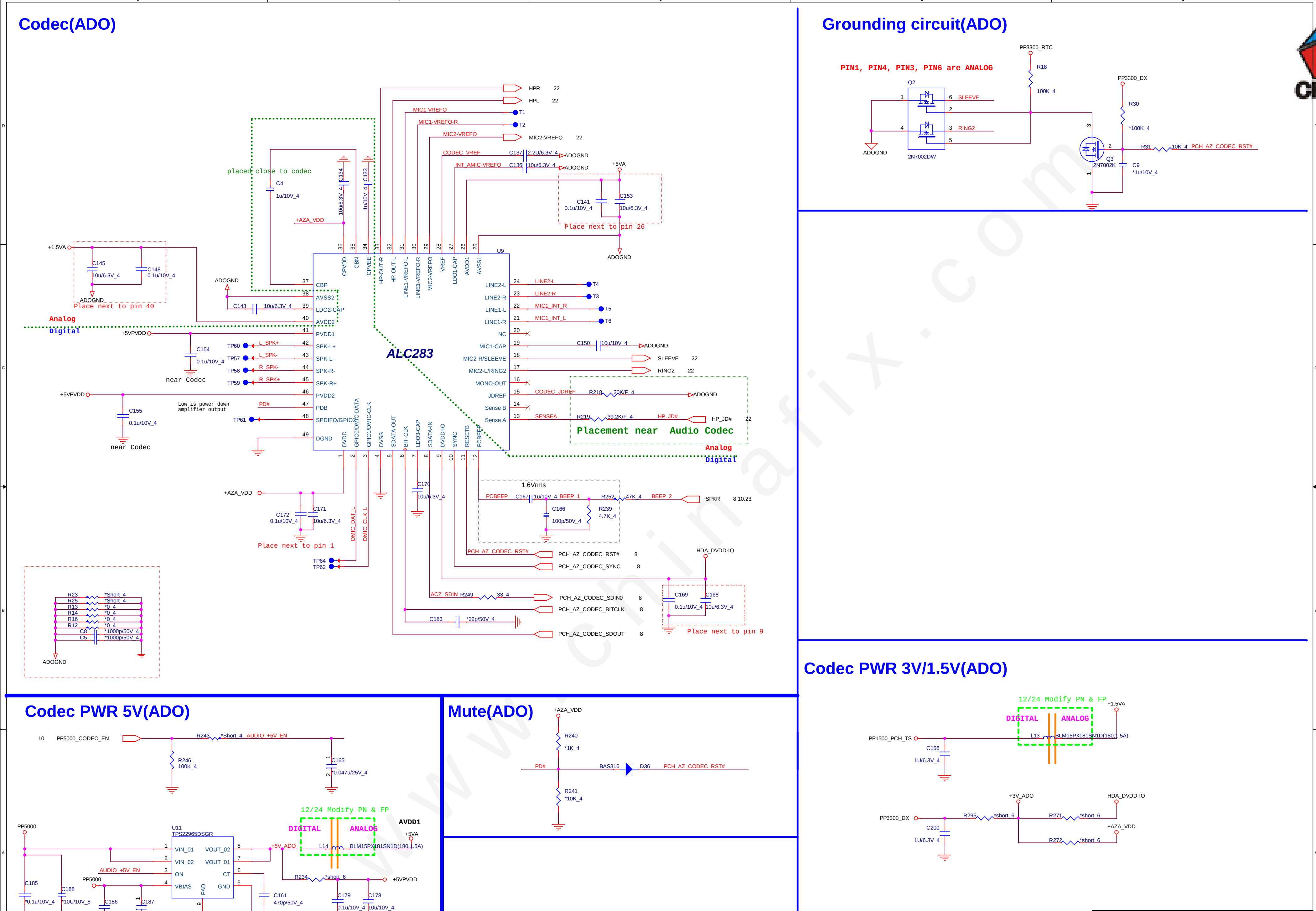

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Size	Document Number	Rev
	ALC283/HP/SPK	3A

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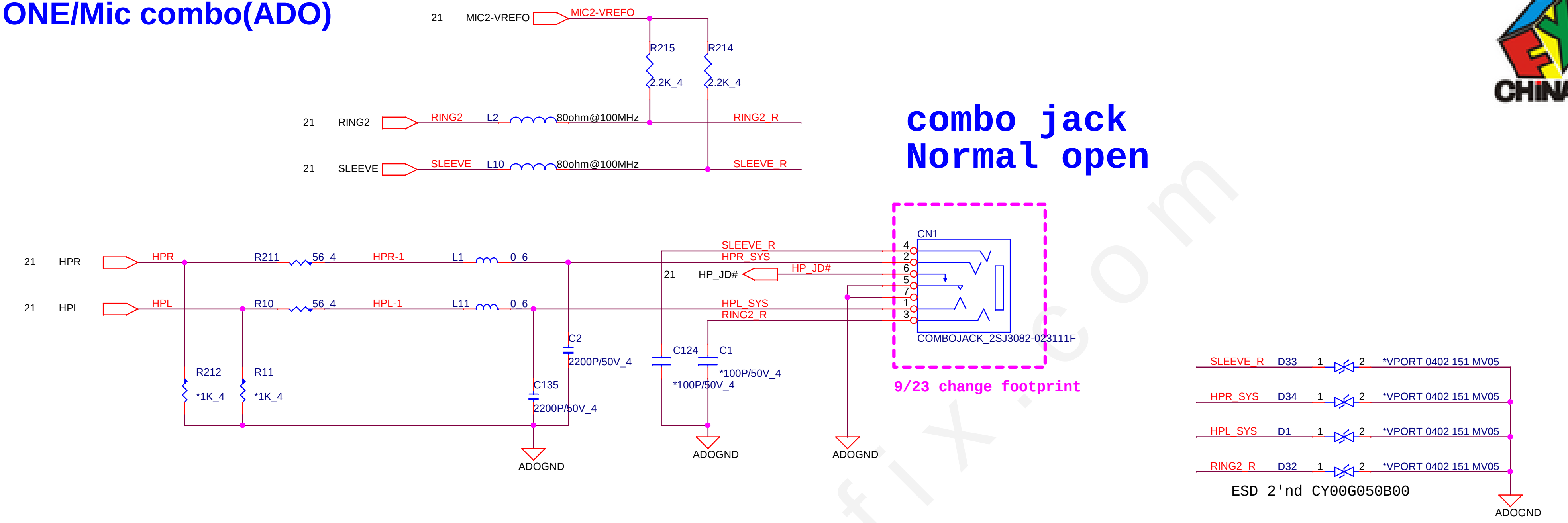
HEADPHONE/Mic combo(ADO)



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Size	Document Number	Rev
	Audio Headset SW	3A

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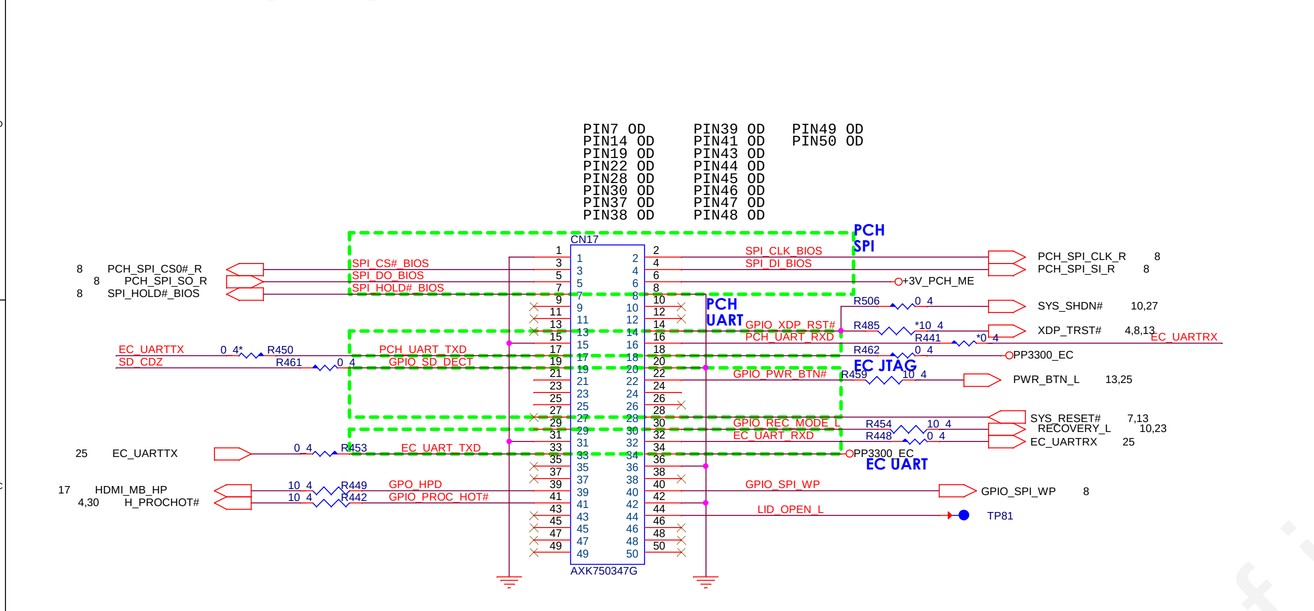
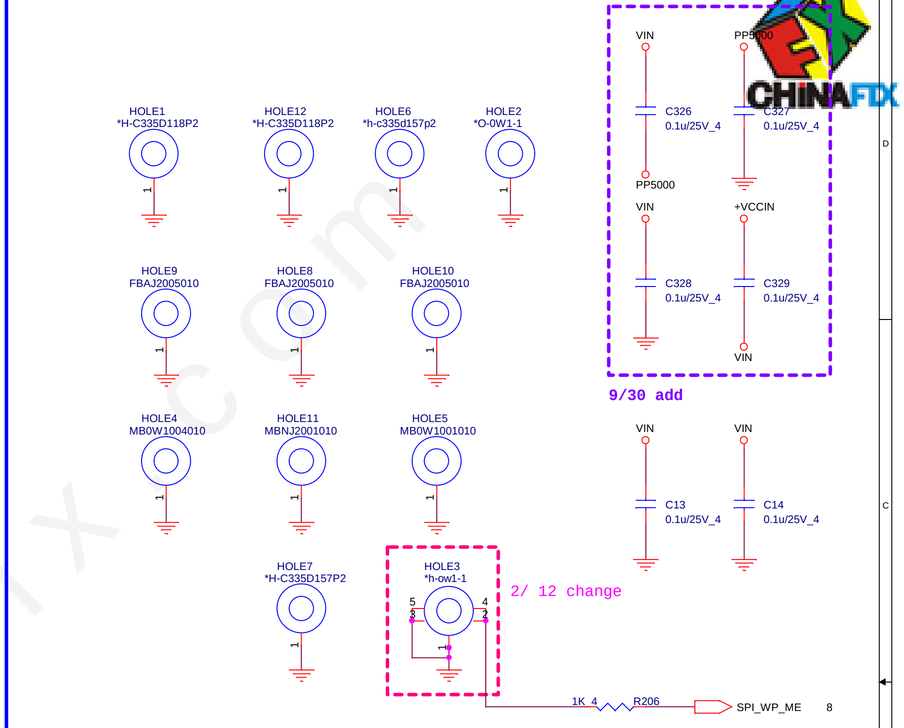
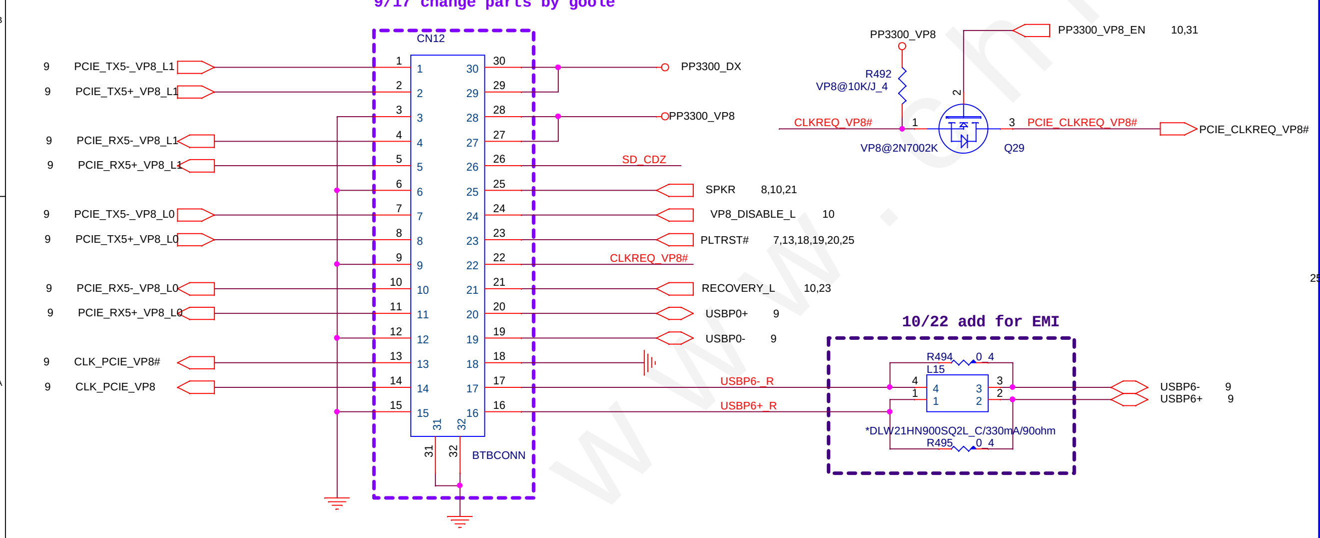
Debug Port(DBG)



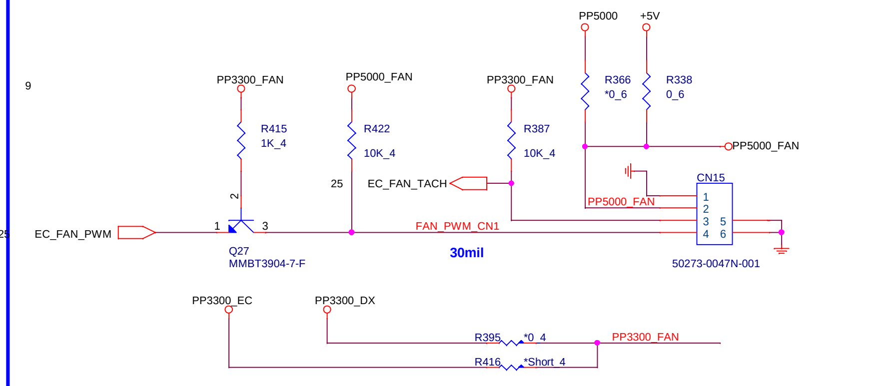
HOLE



B TO B



CPU FAN1 (THM)



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Size	Document Number	Rev
	FAN/Google Debug/HOLE	3A

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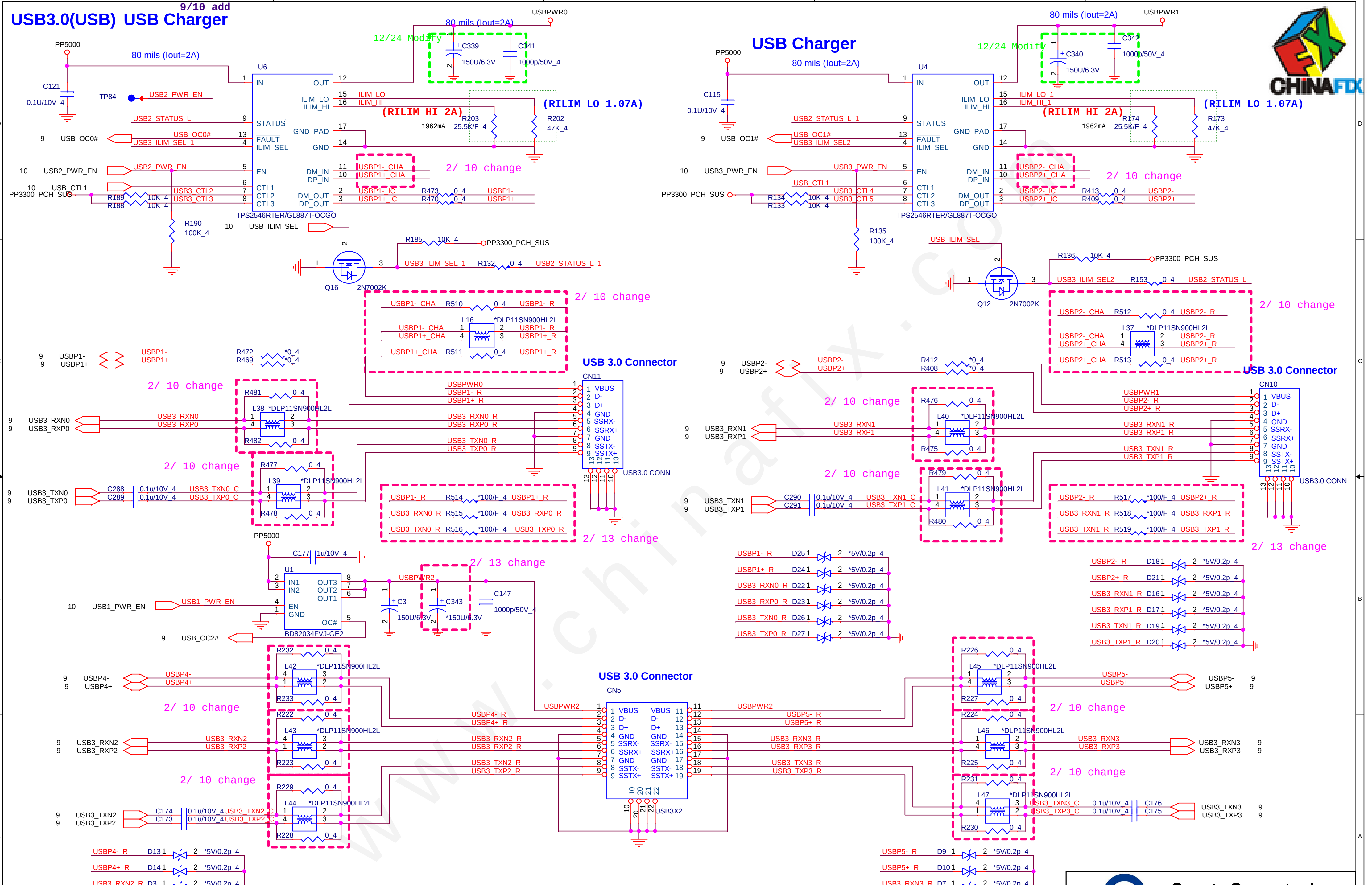

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Size	Document Number	Rev
	USB3	3A

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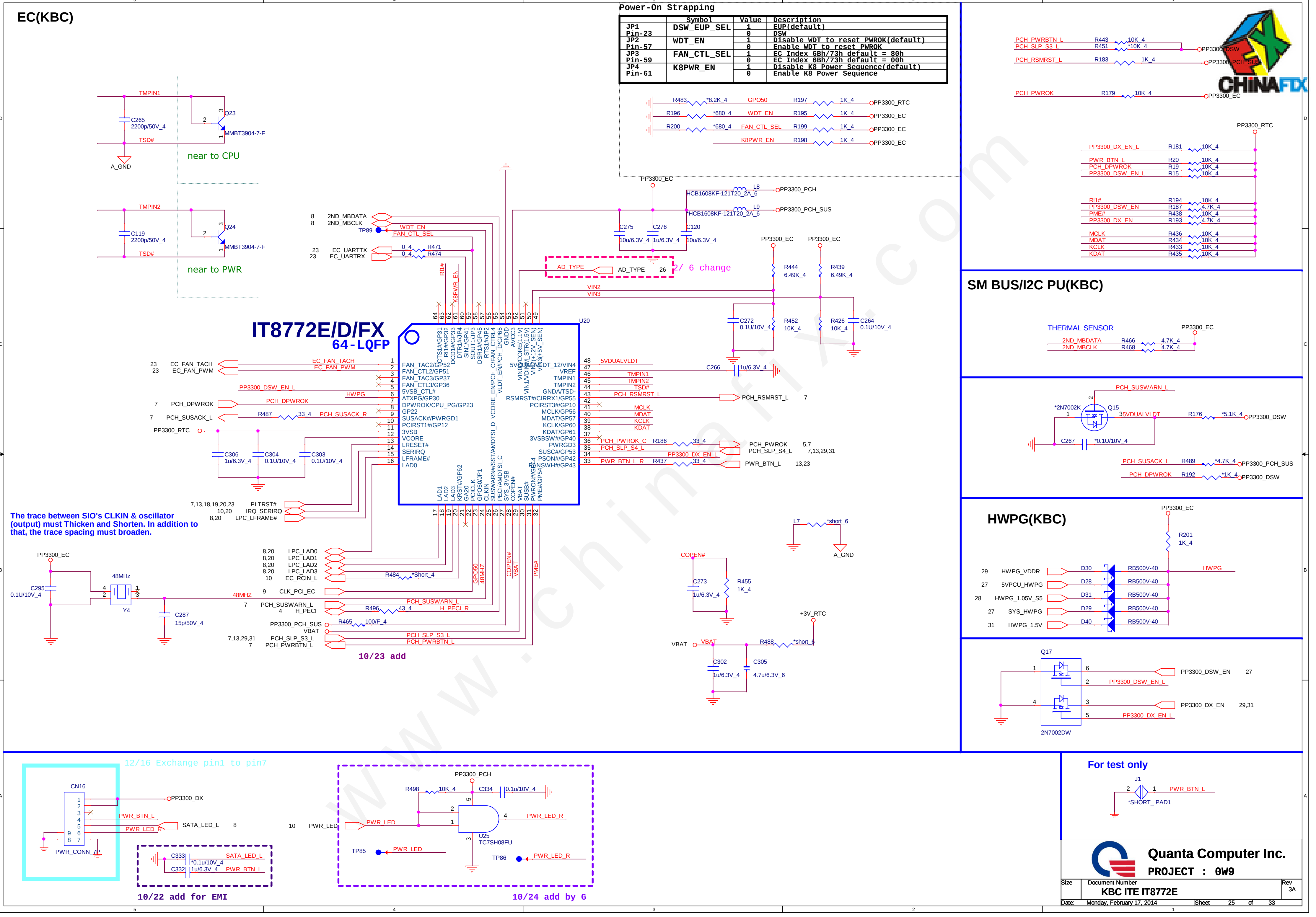
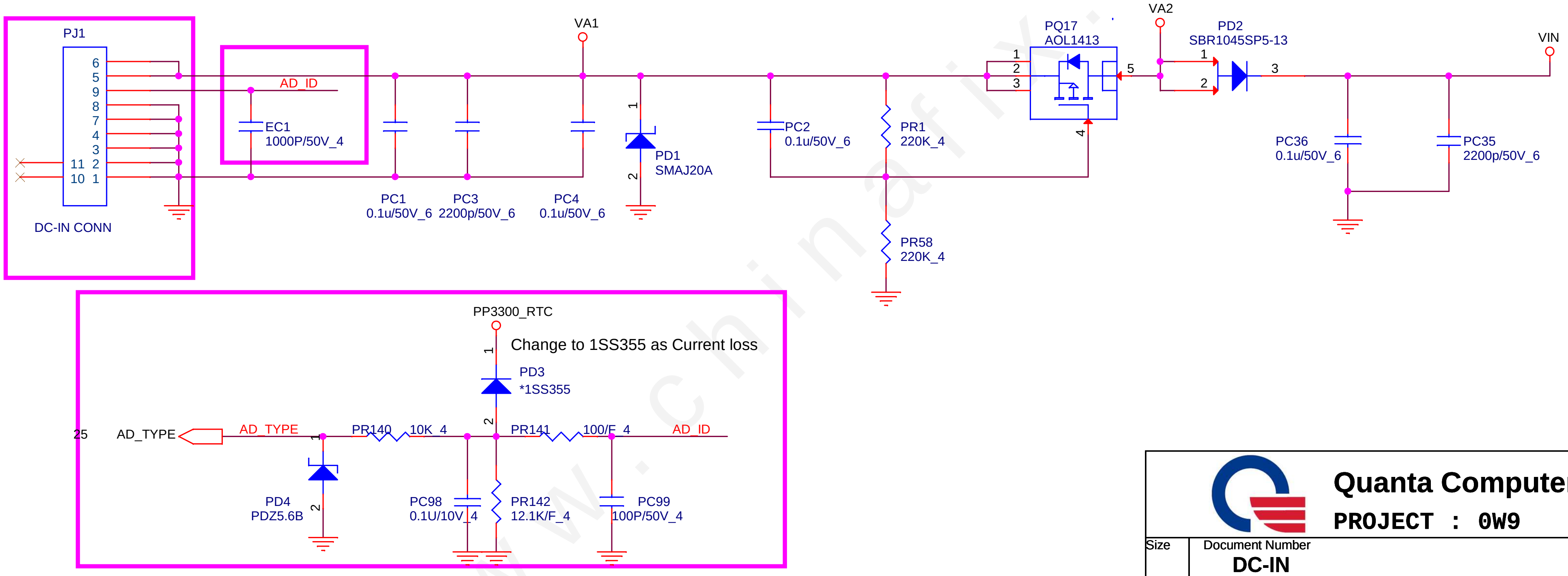
EC(KBC)



Power-On Strapping

	Symbol	Value	Description
JP1 Pin-23	DSW_EUP_SEL	1	EUP(default)
		0	DSW
JP2 Pin-57	WDT_EN	1	Disable WDT to reset PWROK(default)
		0	Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1	EC Index 6Bh/73h default = 80h
		0	EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1	Disable K8 Power Sequence(default)
		0	Enable K8 Power Sequence



Quanta Computer Inc.

PROJECT : 0W9

Size	Document Number	Rev
	DC-IN	3A

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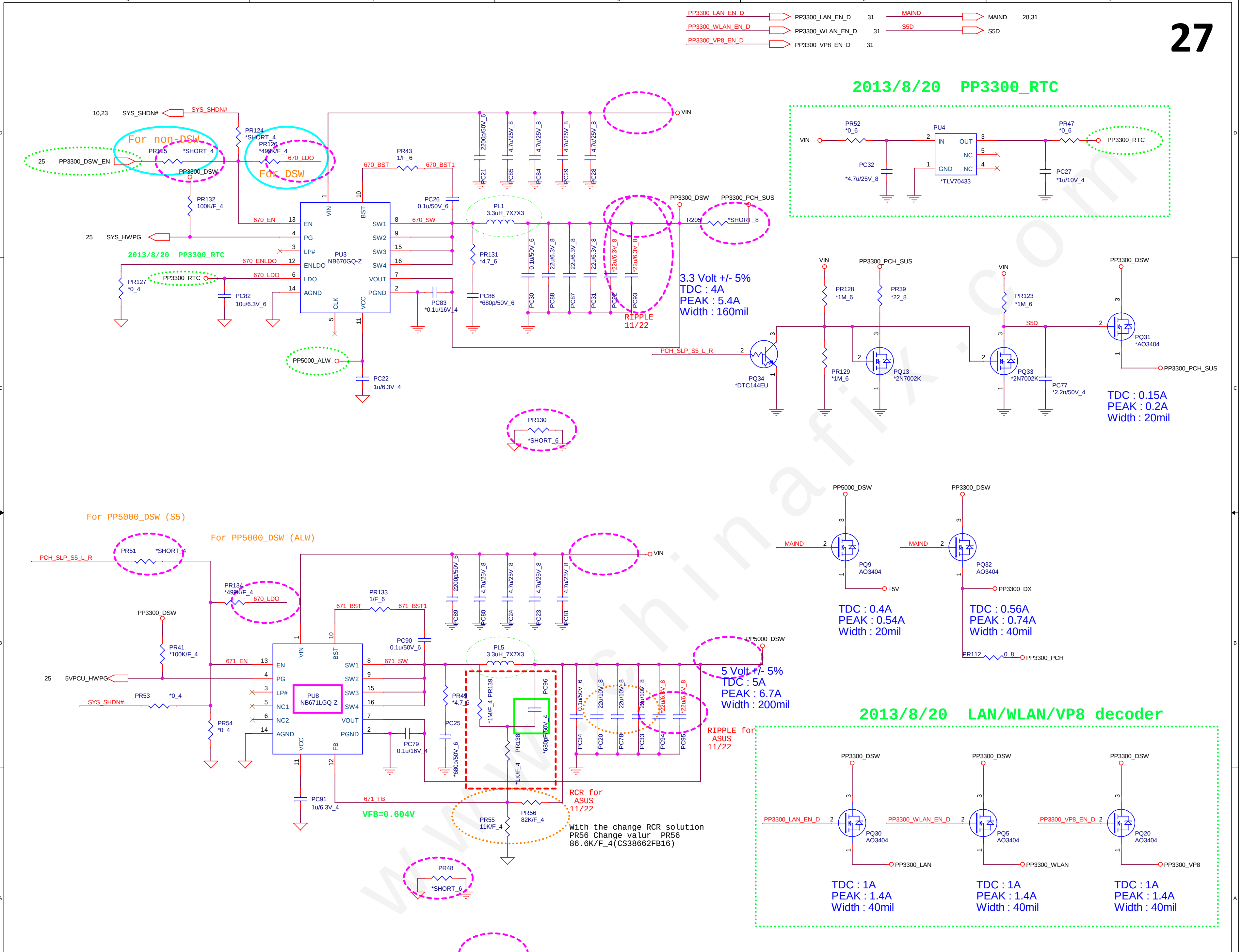
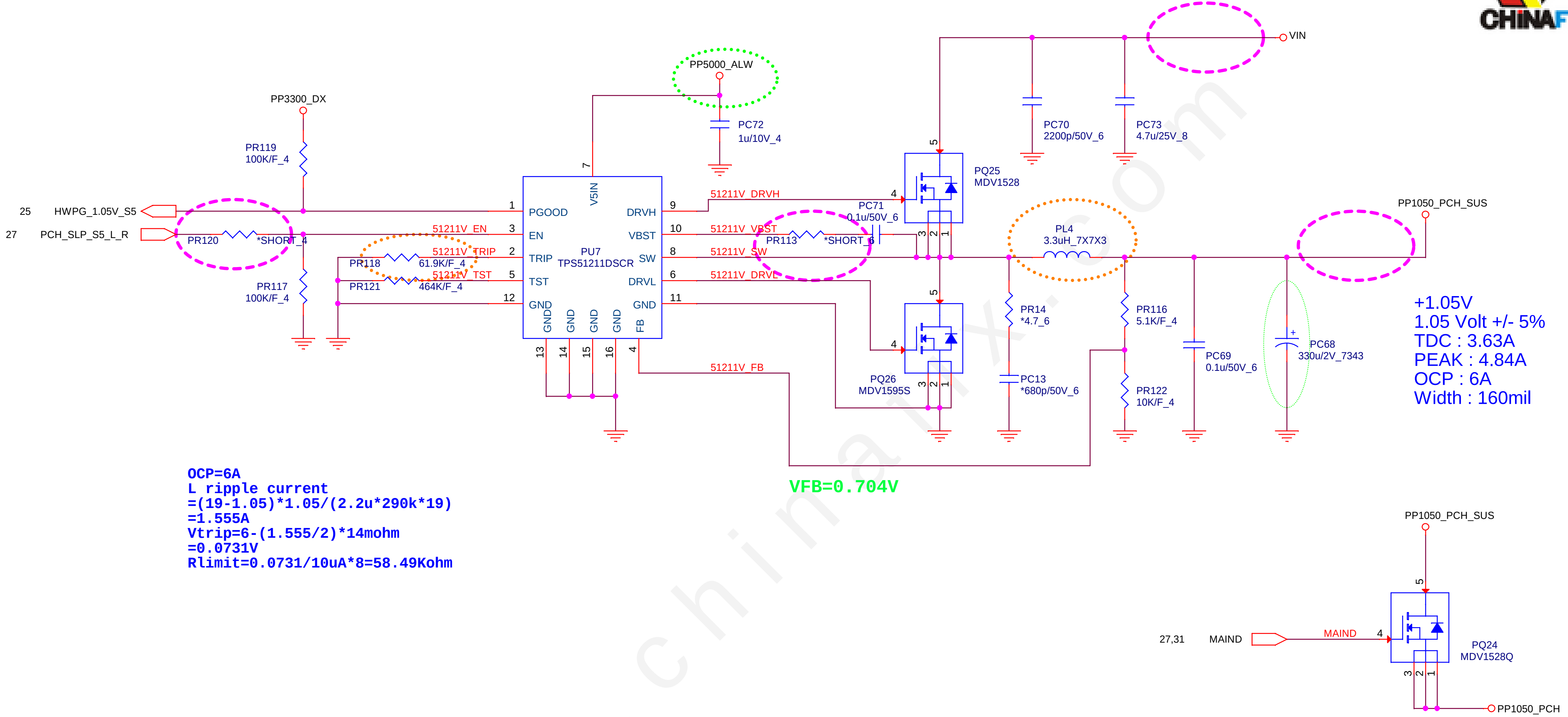


Quanta Computer Inc.	
PROJECT : 0W9	
Size	Document Number: SYSTEM 5V/3V (MPS670/671)
Rev	3A
Date:	Monday, February 17, 2014
Sheet	27 of 33



OCP=6A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=6-(1.555/2)*14mohm
=0.0731V
Rlimit=0.0731/10uA*8=58.49Kohm

+1.05V
1.05 Volt +/- 5%
TDC : 3.63A
PEAK : 4.84A
OCP : 6A
Width : 160mil

TDC : 2.08A
PEAK : 2.77A
Width : 100mil

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Size	Document Number	Rev
	+1.05V(TPS51211)	3A

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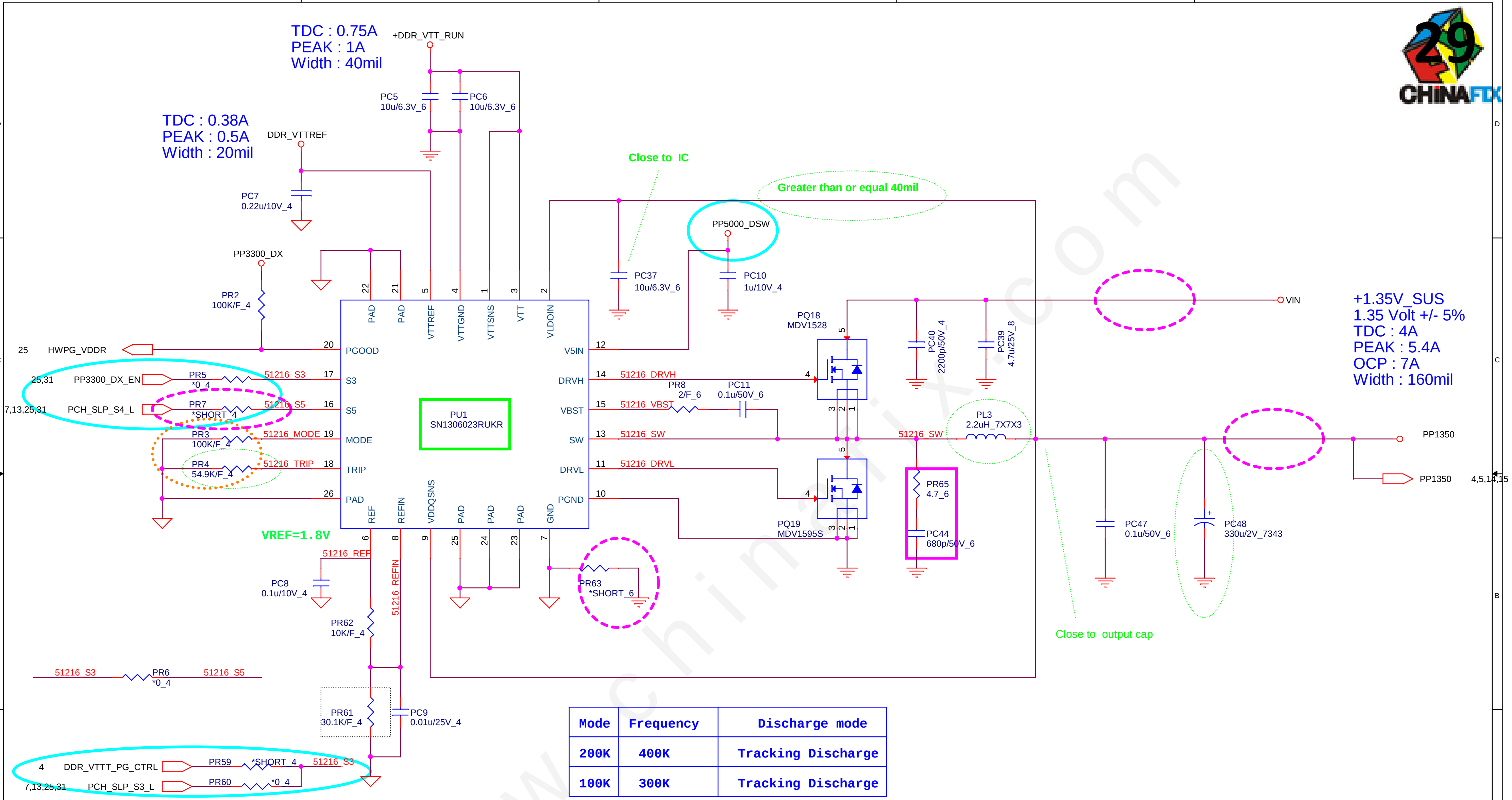

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=7A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=7-(1.425/2)*14mohm
=0.088V
Rlimit=0.088/10uA*8=70.42Kohm

DDR=1.35V
OCP=7A
PR102=10K/F_4
PR101=30.1K/F_4

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PROJECT : 0W9

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	3A
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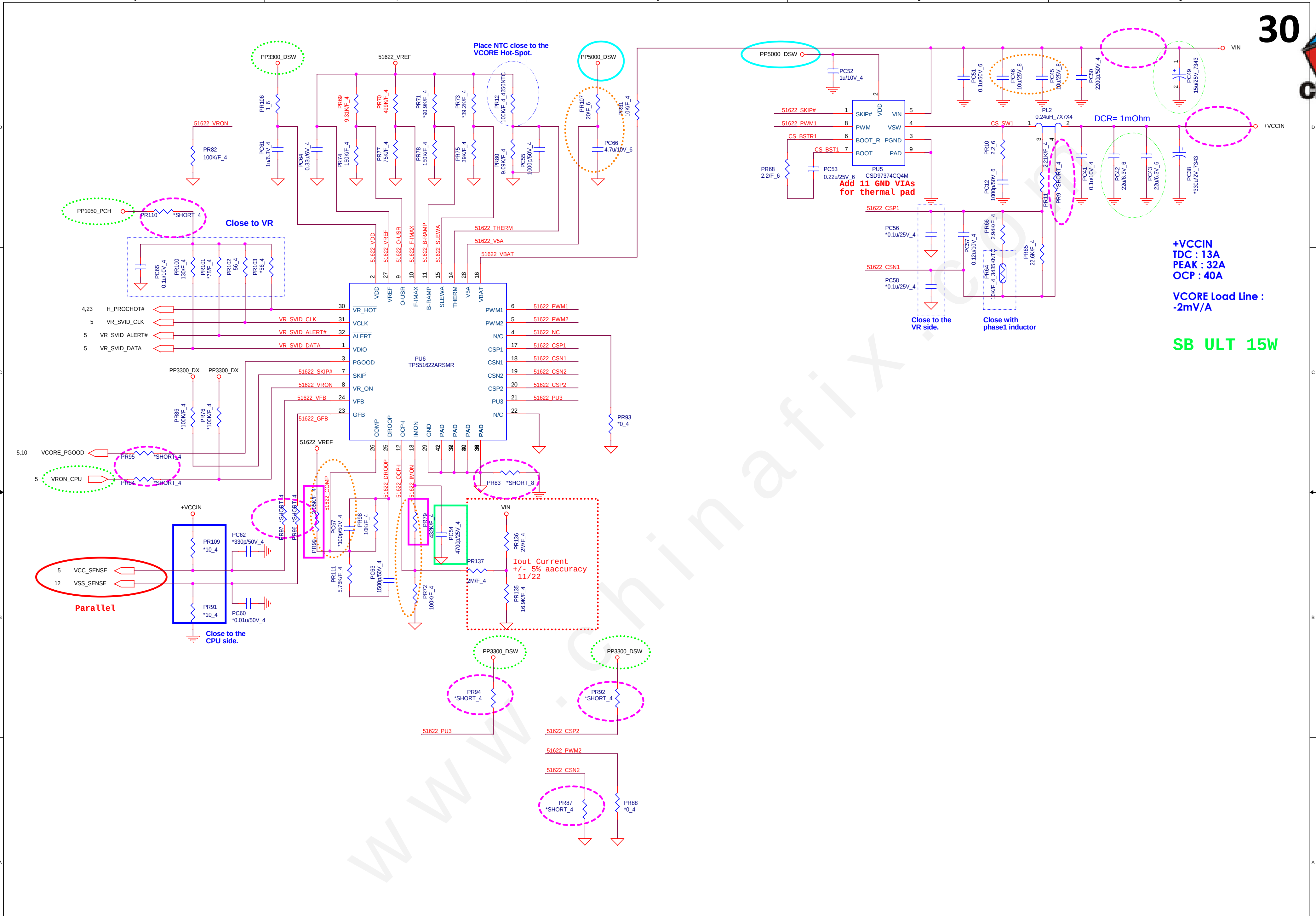

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PROJECT : 0W9

Size	Document Number	Rev
	+VCCIN(TPS51622)	3A

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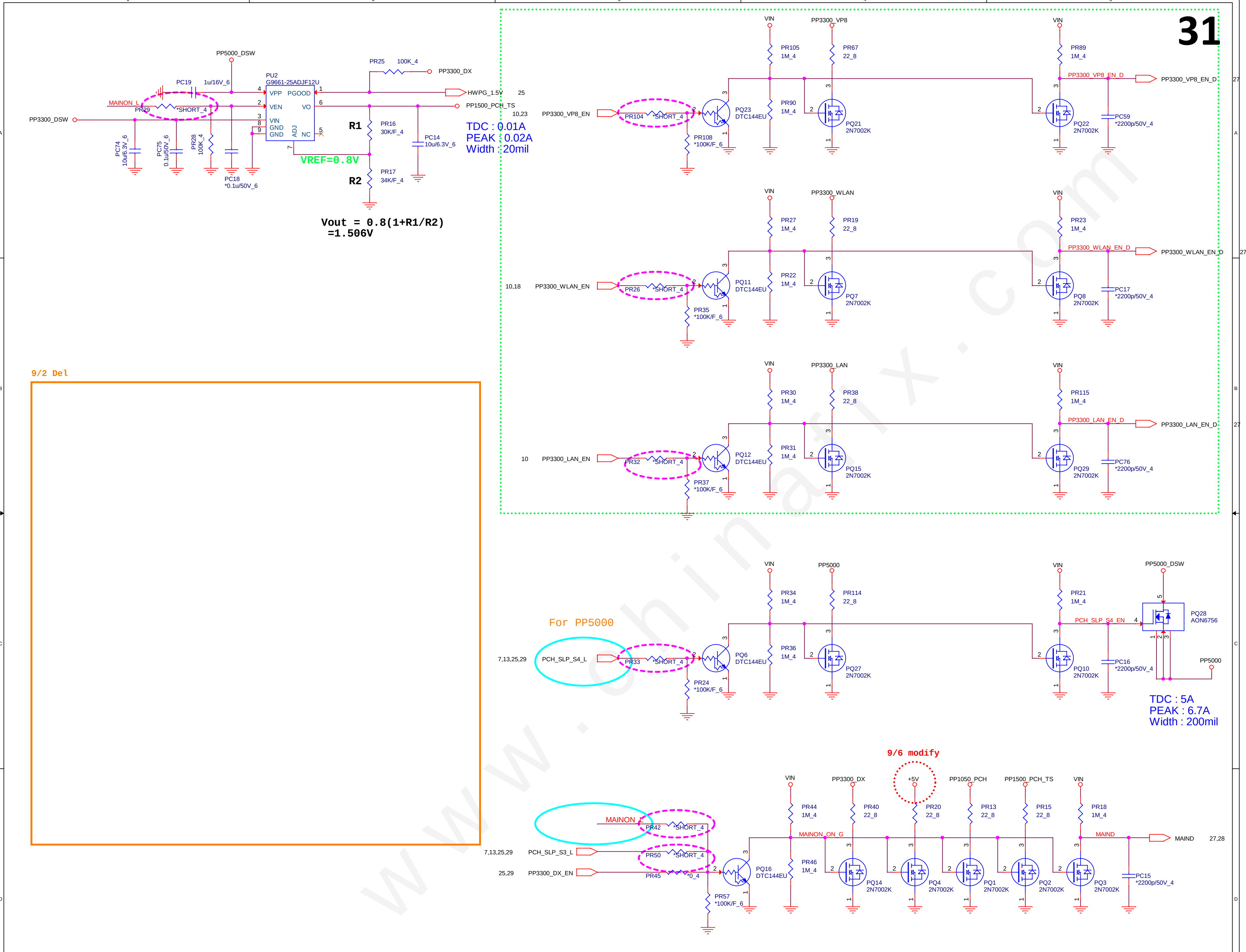

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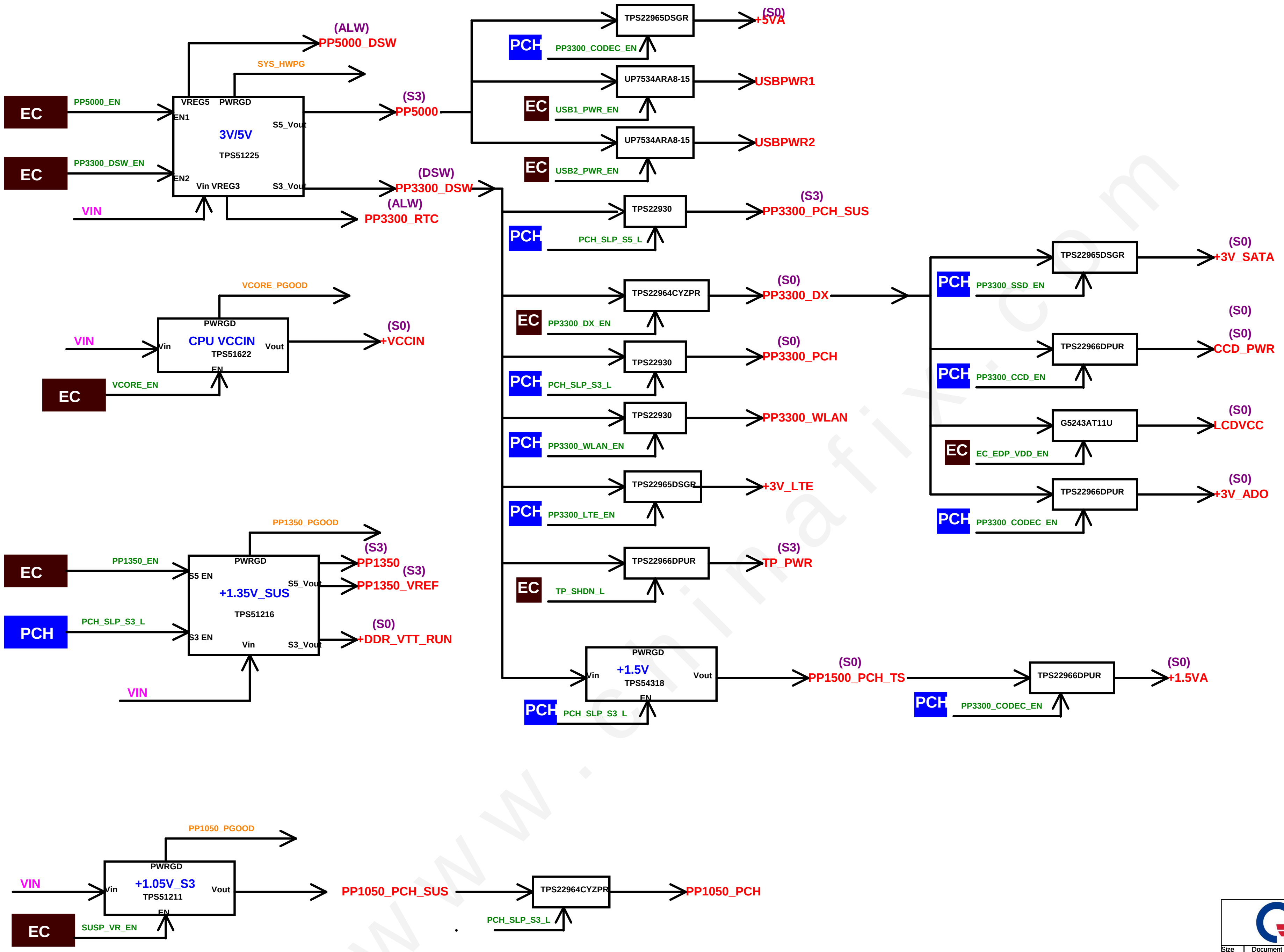
PROJECT : 0W9

Size	Document Number	Rev
	+1.5V/Thermal protect	3A

Date: Monday, February 17, 2014 Sheet 31 of 33



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PROJECT : 0W9

Size	Document Number	Rev
	ULT PWR CONTROL	3A

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