1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0001102890	ENGINEERING RELEASED	2011-04-07

J40I MLB

Thu Apr 7 18:48:24 2011

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67	74	VR - CPU VCORE & GPU CONTROLLER	J40I	11/23/2010
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DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8768	1	SCHEM,MLBI,J40I	SCH		
820-2993	1	PCBF,MLBI,J40I	MLB		
639-1558		PCBA,MLBI,J40I			
085-2372	1	DEV LIST,MLBI,J40I	DEV1		DEVELOPMENT_LIST

DRAWING
TITLE=SHORTSTACK
ABBREV=DRAWING

DRAWING TITLE: SCH,MLB,J40

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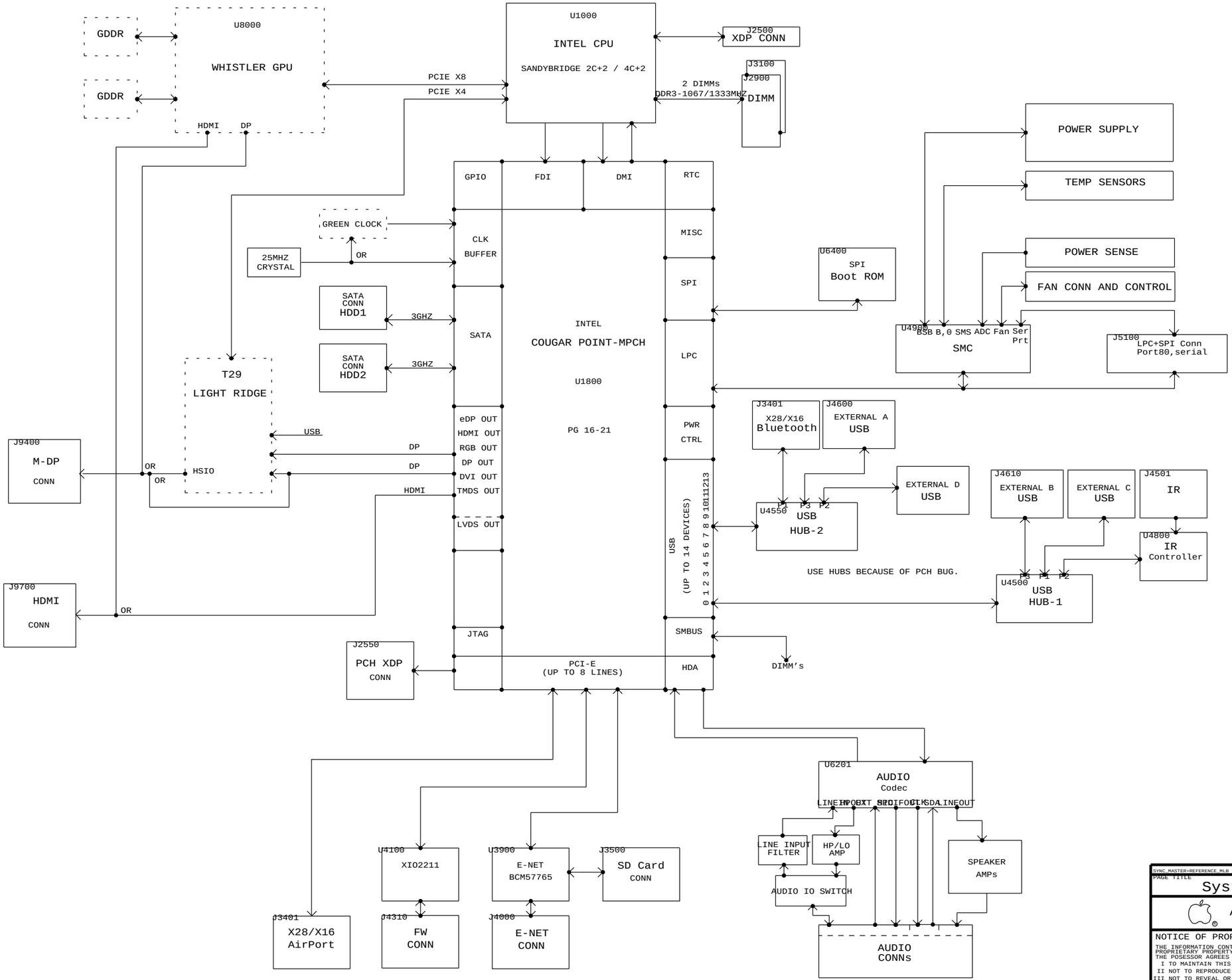

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PLATFORM CONTROL HUB (PCH)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3980	1	IC,PCH,COUGAR_POINT,QMZQ,SUPER SKU,BGA,ES1/B0	U1800	CRITICAL	COUGAR_POINT:B0
337S4022	1	IC,PCH,COUGAR_POINT,QXXX,SUPER SKU,BGA,QS/B1	U1800	CRITICAL	COUGAR_POINT:B1
337S4025	1	IC,PCH,COUGAR_POINT,QNJH,SUPER SKU,BGA,QS/B2	U1800	CRITICAL	COUGAR_POINT:B2
337S4029	1	IC,PCH,COUGAR_POINT,SLH9D,BD82HM65,BGA,PRQ/B2	U1800	CRITICAL	COUGAR_POINT:B2_PRQ_QLD
337S4087	1	IC,PCH,COUGAR_POINT,SLJ4P,BD82HM65,BGA,PRQ/B3	U1800	CRITICAL	COUGAR_POINT:B3_PRQ

PROGRAMMED PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341T0338	1	IC,EFI BOOTROM,J40	U6400	CRITICAL		BASE: 335S0770,335S0769
341T0335	1	IC,SMC,J40G	U4900	CRITICAL	SMC:J40G	BASE: 338S0895
341T0336	1	IC,SMC,J40I	U4900	CRITICAL	SMC:J40I	BASE: 338S0895
341T0337	1	IC,SMC,J40S	U4900	CRITICAL	SMC:J40S	BASE: 338S0895
341T0340	1	IC,IR CONTROLLER,J40	U4700	CRITICAL		BASE: 338S0375
341T0341	1	IC,ENET ROM J40	U3990	CRITICAL		BASE: 335S0539, 335S0663, OR 335S0800

NON-SCHEMATIC PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6838	1	LBL,SERIAL NUMBER	LBL		

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0286	128S0248	?	?	39UF CAP FROM SANYO AND CHEMI-CON
132S0099	132S0203	?	?	0.1UF CAP,X7R
138S0676	138S0691		?	22UF CAP FROM MURATA
138S0681	138S0638		?	10UF CAP FROM TAIYO YUDEN
152S0138	152S0694	?	?	INDUCTOR FROM VISHAY
152S1447	152S1269	?	?	INDUCTOR FROM CYNTEC
152S1282	152S1155	?	?	INDUCTOR FROM CYNTEC
152S1366	152S1289	?	?	INDUCTOR FROM TOKO
155S0641	155S0397	?	?	FERRITE FROM LAIRD
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
157S0058	157S0055		ALL	DELTA ALT TO TDK MAGNETICS
353S3196	353S3326	?	?	DIFFERENT TEMP RATING
371S0679	371S0652	?	?	PIN DIODE FROM NXP
376S0914	376S0881		?	SI7121DN AS ALTERNATE
376S0957	376S0999		?	DUAL FET FROM FAIRCHILD
376S0958	376S0953		?	DUAL FET FROM FAIRCHILD
376S1000	376S0960		?	DUAL FET FROM FAIRCHILD
376S0972	376S0612		?	FET FROM ROHM
376S0613	376S0859		?	OLDER DUAL FET FROM TOSHIBA
376S0855	376S0859		?	DUAL FET FROM DDS
376S0977	376S0859		?	DUAL FET FROM DDS
138S0703	138S0648		?	CAP FROM MURATA
197S0339	197S0179		?	OSC. FROM SITIME
376S0926	376S0610		?	DUAL FET FROM FAIRCHILD
376S0572	376S0659		?	FET FROM ALPHA OMEGA
377S0124	377S0057		?	VARISTOR FROM AMOTECH

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"G3" RAILS

ON WHEN UNIT HAS BATTERY POWER

BATTERY 3.3V G3

PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
OUT 27

DIODES 3.3V G3

PP3V3_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
OUT 17 18 21 27 91

"G3H" RAILS

ON WHEN UNIT HAS AC POWER

PSU 12V G3H

PP12V_G3H_PSU
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 51 72 91

PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM
OUT 41 51 60 65 72 78

PP12V_G3H_CPUDDR
MAKE_BASE=TRUE
VOLTAGE=12.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM
OUT 51 64 66 68 69 70

EG BOARDS ONLY.

PP12V_G3H_GPU
MAKE_BASE=TRUE
VOLTAGE=12.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM

LDO 5V G3H

PP5V_G3H
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
MAX_NECK_LENGTH=3 MM
OUT 45 47 61 65 91

VR 3.3V G3H

PP3V3_G3H
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 6 27 43 45 46 47 48 61 65 91

"S5" RAILS

STANDARD STANDBY STATE.

FET 5V S5

PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
MAX_NECK_LENGTH=3 MM
OUT 23 61

FET 3.3V S5

PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 17 18 19 20 21 23 24 25 27 28 59 61 62 78 89 91

FET 3.3V ENET

PP3V3_ENET
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 26 37 38 62 91

VR 1.2V ENET

PP1V2_ENET
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3 MM
OUT 37 38 91

PP3V3_G3H
DEVELOPMENT
R0600
200
1% 1/16W MF-LF 0402
ITS_PLUGGED_IN
NO_TEST=TRUE
LED0600
GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT

PP3V3_S4
PP3V3_G3H
DEVELOPMENT
R0602
200
1% 1/16W MF-LF 0402
ITS_ALIVE
NO_TEST=TRUE
LED0602
GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT

PP3V3_G3H
DEVELOPMENT
R0603
200
1% 1/16W MF-LF 0402
ITS_BREATHING
NO_TEST=TRUE
LED0603
GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT
ITS_BREATHING_Q
NO_TEST=TRUE

DEVELOPMENT
Q0603
SSM3K15FV
SOD-VESM-HF

SMC_SYS_LED

"S4" RAILS

ON IN RUN AND SLEEP

VR 5V S4

PP5V_S4
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 28 43 44 45 61 65 66 78 91

FET 3.3V S4

PP3V3_S4
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
MAX_NECK_LENGTH=3 MM
OUT 6 19 20 25 28 33 34 35 38 47 49 50 61 77 78 91

VR 1.5V S3

PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
OUT 28 30 31 32 61 66 72 91

VR 0.75V S3

PPDDRVREF_S3
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
OUT 33 66 91

PP3V3_S0
DEVELOPMENT
R0605
200
1% 1/16W MF-LF 0402
CATERR_LED_R
DEVELOPMENT
LED0605
RED 2X125-SM
CATERR_LED

DEVELOPMENT
R0615
100K
5% 1/16W MF-LF 0402

DEVELOPMENT
Q0605
DMB53D0UV
SOT-563
CATERR_R

DEVELOPMENT
R0616
20K
5% 1/16W MF-LF 0402
CPU_CATERR_L
CPU_CATERR_RL

DEVELOPMENT
Q0605
DMB53D0UV
SOT-563

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1.05V Rails

FET 5V S0

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 23 24 41 42 48 51 62 64 67 68 69 70 71 80 91

XW0700 SM 1 2
PP5V_S0_AUDIO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.508MM
MIN_NECK_WIDTH=0.208MM
MAX_NECK_LENGTH=3 MM
OUT 93

XW0701 SM 1 2
PP5V_S0_AUDIO_AMP
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3 MM
OUT 56

FET 3.3V S0

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 31 52 53 57 58 60 61 62 67 71 0 15 17 18 19 20 21 23 24 27 30 32 34 37 38 39 40 41 47 49 50 72 73 74 76 77 79 89 91

LDO 1.5V S0

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 17 21 23 39 53 71 72 91

VR 1.05V S0

PP1V05_S0_VCCIO
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 10 11 13 15 67 91

PP1V05_S0
OUT 24 46 50 62 70 76

PP1V05_S0_PCH
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
OUT 17 18 21 23 50

VR 1.8V S0

PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 15 18 21 23 26 71

PP1V8_S0_CPU_VCCPLL_R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
OUT 13 15

VR 0.75V S0

PP0V75_S0_DDRVTT
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 28 30 31 66 91

VR CPU-SA S0

PPVCCSA_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 13 16 50 64

VR CPU-CORE S0

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
MAX_NECK_LENGTH=3 MM
OUT 10 13 15 50 67 68 91

VR CPU-AXG S0 16 13 67 50

PPVAXG_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
MAX_NECK_LENGTH=3 MM
(IG BOARDS ONLY.)

FET 1.5V SW

PP1V5_VDDQ_CPU_R
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
OUT 50 61

PP1V5_VDDQ_CPU
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
OUT 11 13 16 28 31 32 50 62

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INTEL INTEGRATED GRAPHICS

FDI BUS.

10	IN	=FDI_DATA_P<7..0>	MAKE_BASE=TRUE	FDI_DATA_P<7..0>	OUT	18 81
10	IN	=FDI_DATA_N<7..0>	MAKE_BASE=TRUE	FDI_DATA_N<7..0>	OUT	18 81
10	OUT	=FDI_INT	MAKE_BASE=TRUE	FDI_INT	IN	18 81
10	OUT	=FDI_FSYNC<1..0>	MAKE_BASE=TRUE	FDI_FSYNC<1..0>	IN	18 81
10	OUT	=FDI_LSYNC<1..0>	MAKE_BASE=TRUE	FDI_LSYNC<1..0>	IN	18 81

NO PCIE TO EXTERNAL GRAPHICS

10	OUT	=PEG_D2R_N<7..0>	MAKE_BASE=TRUE	NC_PEG_D2RN<7..0>	91
10	OUT	=PEG_D2R_P<7..0>	MAKE_BASE=TRUE	NC_PEG_D2RP<7..0>	91
10	IN	=PEG_R2D_C_N<7..0>	MAKE_BASE=TRUE	NC_PEG_R2D_CN<7..0>	91
10	IN	=PEG_R2D_C_P<7..0>	MAKE_BASE=TRUE	NC_PEG_R2D_CP<7..0>	91
84 17	IN	PEG_CLK100M_N	MAKE_BASE=TRUE	NC_PEG_CLK100MN	91
84 17	IN	PEG_CLK100M_P	MAKE_BASE=TRUE	NC_PEG_CLK100MP	91

EXTERNAL DISPLAY PORT

18	BI	=IG_DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	DP_EXTA_DDC_CLK	BI	77 83
18	BI	=IG_DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	DP_EXTA_DDC_DATA	BI	77 83
18	BI	=IG_DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE	DP_EXTA_AUXCH_C_N	BI	77 83
18	BI	=IG_DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE	DP_EXTA_AUXCH_C_P	BI	77 83
18	OUT	=IG_DP_EXTA_HPD	MAKE_BASE=TRUE	DP_EXTA_HPD	IN	77 83
18	IN	=IG_DP_EXTA_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_EXTA_ML_C_N<3..0>	OUT	77 83
18	IN	=IG_DP_EXTA_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_EXTA_ML_C_P<3..0>	OUT	77 83

HDMI

18	BI	=IG_HDMI_LS_SCL	MAKE_BASE=TRUE	HDMI_LS_SCL	BI	79 83
18	BI	=IG_HDMI_LS_SDA	MAKE_BASE=TRUE	HDMI_LS_SDA	BI	79 83
18	OUT	=IG_HDMI_LS_HPD	MAKE_BASE=TRUE	HDMI_LS_HPD	IN	79 83
18	IN	=IG_HDMI_DATA_C_N<2..0>	MAKE_BASE=TRUE	HDMI_DATA_C_N<2..0>	OUT	79 83
18	IN	=IG_HDMI_DATA_C_P<2..0>	MAKE_BASE=TRUE	HDMI_DATA_C_P<2..0>	OUT	79 83
18	IN	=IG_HDMI_CLK_C_N	MAKE_BASE=TRUE	HDMI_CLK_C_N	OUT	79 83
18	IN	=IG_HDMI_CLK_C_P	MAKE_BASE=TRUE	HDMI_CLK_C_P	OUT	79 83

T29

PCIE

10	OUT	=PCIE_T29_D2R_N<3..0>	MAKE_BASE=TRUE	PCIE_T29_D2R_N<3..0>	IN	74 84
10	OUT	=PCIE_T29_D2R_P<3..0>	MAKE_BASE=TRUE	PCIE_T29_D2R_P<3..0>	IN	74 84
10	IN	=PCIE_T29_R2D_C_N<3..0>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_N<3..0>	OUT	74 84
10	IN	=PCIE_T29_R2D_C_P<3..0>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_P<3..0>	OUT	74 84

T29 DISPLAY PORT INPUT

18	BI	=IG_DP_T29SNK0_CTRL_CLK	MAKE_BASE=TRUE	DP_T29SNK0_CTRL_CLK	BI	74
18	BI	=IG_DP_T29SNK0_CTRL_DATA	MAKE_BASE=TRUE	DP_T29SNK0_CTRL_DATA	BI	74
18	BI	=IG_DP_T29SNK0_AUXCH_C_N	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_N	BI	74 83
18	BI	=IG_DP_T29SNK0_AUXCH_C_P	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_P	BI	74 83
18	OUT	=IG_DP_T29SNK0_HPD	MAKE_BASE=TRUE	DP_T29SNK0_HPD	IN	74 83
18	IN	=IG_DP_T29SNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_N<3..0>	OUT	74 83
18	IN	=IG_DP_T29SNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_P<3..0>	OUT	74 83

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC,T29,SLHAJ,FCBGA,15X15MM	U9000	CRITICAL	
335S0550	1	IC,EEPROM,SERIAL,SPI,4KX8,1.8V,MLP8,LF	U9090	CRITICAL	T29ROM:BLANK
341T0342	1	IC,CONF ROM,T29,J40I,S	U9090	CRITICAL	T29ROM:PROG_IS
341T0380	1	IC,CONF ROM,T29,J40G	U9090	CRITICAL	T29ROM:PROG_G
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0339	1	IC,PROGRMD,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3312	1	IC,CBTL04DP081A,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:NXP
353S3312	1	IC,CBTL04DP081A,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:BOTH
353S3055	1	IC,PI3VEDP212,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:PERICOM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3055	353S3312	T29DPMUX:BOTH	?	DP MUX FROM PERICOM

USED FOR T29 IC

ZT0840
STDOFF-4.0OD1.85H-SM

ZT0841
STDOFF-4.0OD1.85H-SM

SYNC_MASTER=J40S SYNC_DATE=12/30/2010

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CPU / NB HEATSINK MOUNTING HOLES / NUTS

ZT0960
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0961
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0962
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0966
STDOFF-4.5OD.98H-1.1-3.48-TH

ENCLOSURE MOUNTING POSTS

ZT0940
STDOFF-4.5OD10.75H-1.1-3.48-TH

ZT0941
STDOFF-4.5OD10.75H-1.1-3.48-TH

REAR I/O FENCE MOUNTING BOSS

ZT0910
4.0OD1.55H-M1.6X0.35-ST

ZT0911
4.0OD1.55H-M1.6X0.35-ST

ZT0912
4.0OD1.55H-M1.6X0.35-ST

ZT0913
4.0OD1.55H-M1.6X0.35-ST

ZT0914
4.0OD1.55H-M1.6X0.35-ST

SPEAKER BOSS

ZT0915
4.0OD1.55H-M1.6X0.35-ST

To be distributed after simulation

ZH0930 HOLE-VIA
ZH0931 HOLE-VIA
ZH0932 HOLE-VIA
ZH0933 HOLE-VIA
ZH0934 HOLE-VIA
ZH0935 HOLE-VIA
ZH0936 HOLE-VIA
ZH0937 HOLE-VIA
ZH0938 HOLE-VIA
ZH0940 HOLE-VIA
ZH0941 HOLE-VIA
ZH0942 HOLE-VIA
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ZH0953 HOLE-VIA
ZH0954 HOLE-VIA
ZH0955 HOLE-VIA
ZH0956 HOLE-VIA
ZH0957 HOLE-VIA
ZH0958 HOLE-VIA

Digital Ground

GND
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3 MM
VOLTAGE=0V
MAKE_BASE=TRUE

57 56 GND_AUDIO_SPKRAMP

POGO PINS FOR GROUNDING HEATPIPE ASSEMBLY.

ZP0900
POGO-2.0OD-3.6H-K86-K87

ZP0902
POGO-2.0OD-3.6H-K86-K87

ZP0901
POGO-2.0OD-3.6H-K86-K87

ZP0903
POGO-2.0OD-3.6H-K86-K87

ZP0907
POGO-2.0OD-3.6H-K86-K87

ZP0920
1.4DIA-SHORT-EMI-MLB-M97-M98

ZP0921
1.4DIA-SHORT-EMI-MLB-M97-M98

ZP0922
1.4DIA-SHORT-EMI-MLB-M97-M98

BLOWER SUPPORT POST.

ZT0970
STDOFF-3.04OD6.1H-1.3-1.9-TH1

DEVELOPMENT
J0900
SM-TP3P4X1P8-TOP

DEVELOPMENT
J0901
SM-TP3P4X1P8-TOP

PLACE ONE ON EACH SIDE OF BOARD IN EASILY ACCESSIBLE LOCATION. LABEL "GND".

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

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MECHANICAL, GROUND VIAS

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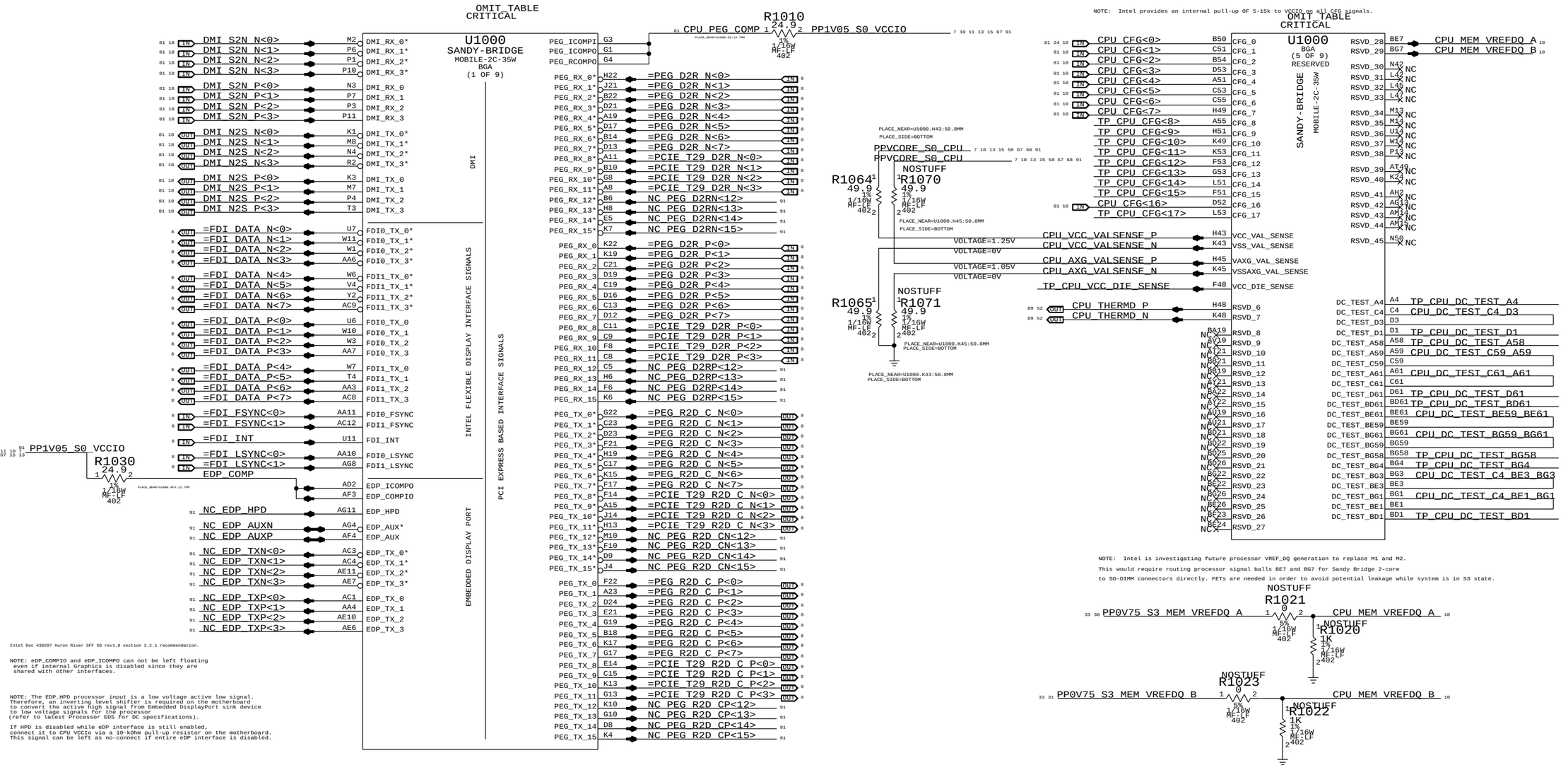

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4034	1	SNB,SR071,PRQ,J1,2.3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU:PRQ_2G3DC
337S4035	1	SNB,SR04A,PRQ,J1,2.5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU:PRQ_2G5DC
337S4036	1	SNB,SR041,PRQ,J1,2.7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU:PRQ_2G7DC

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CPU DMI/PEG/FDI/RSVD

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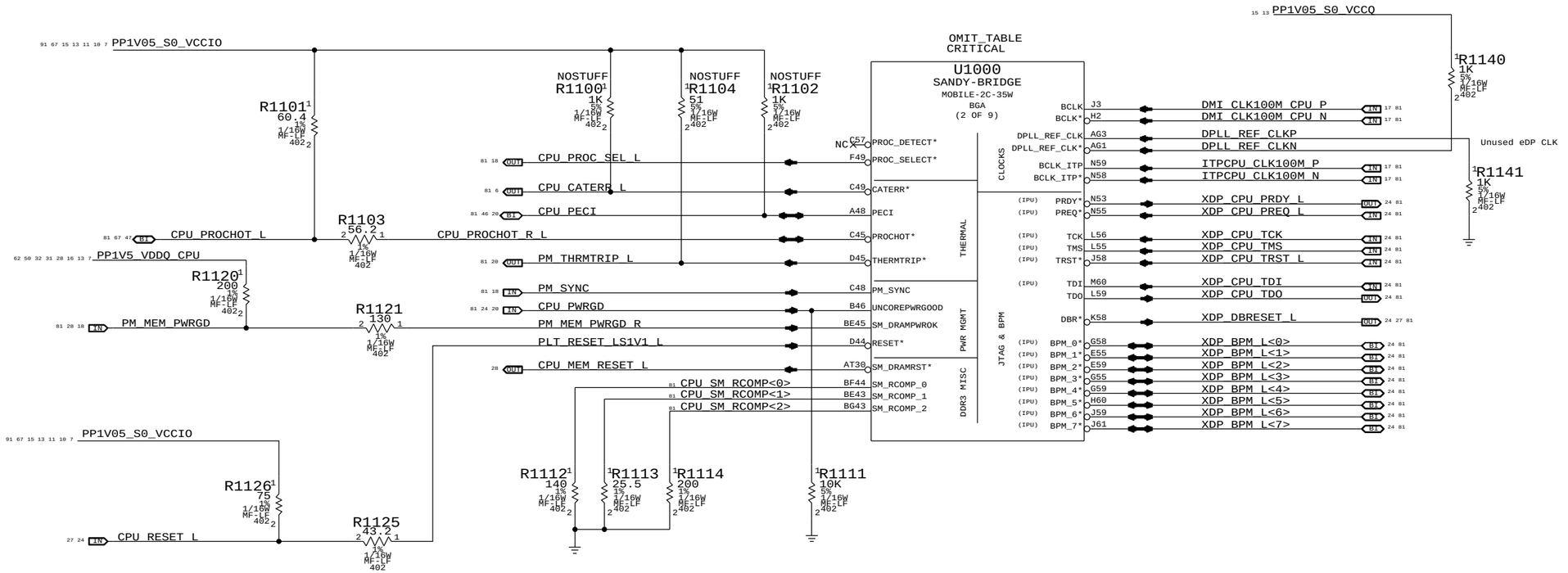

PAGE TITLE	CPU CLOCK/MISC/JTAG
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BGA
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SANDY-BRIDGE
MOBILE-2C-35W
MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	SA_CK_0	AU36	MEM_A_CLK_P<0>	82 29	30 82
MEM_A_DQ<1>	AJ6	SA_DQ_1	SA_CK_0*	AV36	MEM_A_CLK_N<0>	82 29	30 82
MEM_A_DQ<2>	AP11	SA_DQ_2	SA_CKE_0	AY26	MEM_A_CKE<0>		30 82
MEM_A_DQ<3>	AL6	SA_DQ_3					
MEM_A_DQ<4>	AJ10	SA_DQ_4	SA_CK_1	AT40	MEM_A_CLK_P<1>	82 29	30 82
MEM_A_DQ<5>	AJ8	SA_DQ_5	SA_CK_1*	AU40	MEM_A_CLK_N<1>	82 29	30 82
MEM_A_DQ<6>	AL8	SA_DQ_6	SA_CKE_1	BB26	MEM_A_CKE<1>		30 82
MEM_A_DQ<7>	AL7	SA_DQ_7					
MEM_A_DQ<8>	AR11	SA_DQ_8	SA_CS_0*	BB40	MEM_A_CS_L<0>		30 82
MEM_A_DQ<9>	AP6	SA_DQ_9	SA_CS_1*	BC41	MEM_A_CS_L<1>		30 82
MEM_A_DQ<10>	AU6	SA_DQ_10					
MEM_A_DQ<11>	AV9	SA_DQ_11	SA_ODT_0	AY40	MEM_A_ODT<0>		30 82
MEM_A_DQ<12>	AR6	SA_DQ_12	SA_ODT_1	BA41	MEM_A_ODT<1>		30 82
MEM_A_DQ<13>	AP8	SA_DQ_13					
MEM_A_DQ<14>	AT13	SA_DQ_14	SA_DQS_0*	AL11	MEM_A_DQS_N<0>	82 29	29 82
MEM_A_DQ<15>	AU13	SA_DQ_15	SA_DQS_1*	AR8	MEM_A_DQS_N<1>	82 29	29 82
MEM_A_DQ<16>	BC7	SA_DQ_16	SA_DQS_2*	AV11	MEM_A_DQS_N<2>	82 29	29 82
MEM_A_DQ<17>	BB7	SA_DQ_17	SA_DQS_3*	AT17	MEM_A_DQS_N<3>	82 29	29 82
MEM_A_DQ<18>	BA13	SA_DQ_18	SA_DQS_4*	AV45	MEM_A_DQS_N<4>	82 29	29 82
MEM_A_DQ<19>	BB11	SA_DQ_19	SA_DQS_5*	AY51	MEM_A_DQS_N<5>	82 29	29 82
MEM_A_DQ<20>	BA7	SA_DQ_20	SA_DQS_6*	AT55	MEM_A_DQS_N<6>	82 29	29 82
MEM_A_DQ<21>	BA9	SA_DQ_21	SA_DQS_7*	AK55	MEM_A_DQS_N<7>	82 29	29 82
MEM_A_DQ<22>	BB9	SA_DQ_22					
MEM_A_DQ<23>	AY13	SA_DQ_23	SA_DQS_0	AJ11	MEM_A_DQS_P<0>	82 29	29 82
MEM_A_DQ<24>	AV14	SA_DQ_24	SA_DQS_1	AR10	MEM_A_DQS_P<1>	82 29	29 82
MEM_A_DQ<25>	AR14	SA_DQ_25	SA_DQS_2	AY11	MEM_A_DQS_P<2>	82 29	29 82
MEM_A_DQ<26>	AY17	SA_DQ_26	SA_DQS_3	AU17	MEM_A_DQS_P<3>	82 29	29 82
MEM_A_DQ<27>	AR19	SA_DQ_27	SA_DQS_4	AW45	MEM_A_DQS_P<4>	82 29	29 82
MEM_A_DQ<28>	BA14	SA_DQ_28	SA_DQS_5	AV51	MEM_A_DQS_P<5>	82 29	29 82
MEM_A_DQ<29>	AU14	SA_DQ_29	SA_DQS_6	AT56	MEM_A_DQS_P<6>	82 29	29 82
MEM_A_DQ<30>	BB14	SA_DQ_30	SA_DQS_7	AK54	MEM_A_DQS_P<7>	82 29	29 82
MEM_A_DQ<31>	BB17	SA_DQ_31					
MEM_A_DQ<32>	BA45	SA_DQ_32	SA_MA_0	BG35	MEM_A_A<0>		30 82
MEM_A_DQ<33>	AR43	SA_DQ_33	SA_MA_1	BB34	MEM_A_A<1>		30 82
MEM_A_DQ<34>	AW48	SA_DQ_34	SA_MA_2	BE35	MEM_A_A<2>		30 82
MEM_A_DQ<35>	BC48	SA_DQ_35	SA_MA_3	BD35	MEM_A_A<3>		30 82
MEM_A_DQ<36>	BC45	SA_DQ_36	SA_MA_4	AT34	MEM_A_A<4>		30 82
MEM_A_DQ<37>	AR45	SA_DQ_37	SA_MA_5	AU34	MEM_A_A<5>		30 82
MEM_A_DQ<38>	AT48	SA_DQ_38	SA_MA_6	BB32	MEM_A_A<6>		30 82
MEM_A_DQ<39>	AY48	SA_DQ_39	SA_MA_7	AT32	MEM_A_A<7>		30 82
MEM_A_DQ<40>	BA49	SA_DQ_40	SA_MA_8	AY32	MEM_A_A<8>		30 82
MEM_A_DQ<41>	AV49	SA_DQ_41	SA_MA_9	AV32	MEM_A_A<9>		30 82
MEM_A_DQ<42>	BB51	SA_DQ_42	SA_MA_10	BE37	MEM_A_A<10>		30 82
MEM_A_DQ<43>	AY53	SA_DQ_43	SA_MA_11	BA30	MEM_A_A<11>		30 82
MEM_A_DQ<44>	BB49	SA_DQ_44	SA_MA_12	BC30	MEM_A_A<12>		30 82
MEM_A_DQ<45>	AU49	SA_DQ_45	SA_MA_13	AW41	MEM_A_A<13>		30 82
MEM_A_DQ<46>	BA53	SA_DQ_46	SA_MA_14	AY28	MEM_A_A<14>		30 82
MEM_A_DQ<47>	BB55	SA_DQ_47	SA_MA_15	AU26	MEM_A_A<15>		30 82
MEM_A_DQ<48>	BA55	SA_DQ_48					
MEM_A_DQ<49>	AV56	SA_DQ_49					
MEM_A_DQ<50>	AP50	SA_DQ_50					
MEM_A_DQ<51>	AP53	SA_DQ_51					
MEM_A_DQ<52>	AV54	SA_DQ_52					
MEM_A_DQ<53>	AT54	SA_DQ_53					
MEM_A_DQ<54>	AP56	SA_DQ_54					
MEM_A_DQ<55>	AP52	SA_DQ_55					
MEM_A_DQ<56>	AN57	SA_DQ_56					
MEM_A_DQ<57>	AN53	SA_DQ_57					
MEM_A_DQ<58>	AG56	SA_DQ_58					
MEM_A_DQ<59>	AG53	SA_DQ_59					
MEM_A_DQ<60>	AN55	SA_DQ_60					
MEM_A_DQ<61>	AN52	SA_DQ_61					
MEM_A_DQ<62>	AG55	SA_DQ_62					
MEM_A_DQ<63>	AK56	SA_DQ_63					
MEM_A_BA<0>	BD37	SA_BS_0					
MEM_A_BA<1>	BF36	SA_BS_1					
MEM_A_BA<2>	BA28	SA_BS_2					
MEM_A_CAS_L	BE39	SA_CAS*					
MEM_A_RAS_L	BD39	SA_RAS*					
MEM_A_WE_L	AT41	SA_WE*					

OMIT_TABLE
CRITICAL

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SANDY-BRIDGE
MOBILE-2C-35W
MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	SB_CK_0	BA34	MEM_B_CLK_P<0>	82 29	31 82
MEM_B_DQ<1>	AL1	SB_DQ_1	SB_CK_0*	AY34	MEM_B_CLK_N<0>	82 29	31 82
MEM_B_DQ<2>	AN3	SB_DQ_2	SB_CKE_0	AR22	MEM_B_CKE<0>		31 82
MEM_B_DQ<3>	AR4	SB_DQ_3					
MEM_B_DQ<4>	AK4	SB_DQ_4	SB_CK_1	BA36	MEM_B_CLK_P<1>	82 29	31 82
MEM_B_DQ<5>	AK3	SB_DQ_5	SB_CK_1*	BB36	MEM_B_CLK_N<1>	82 29	31 82
MEM_B_DQ<6>	AN4	SB_DQ_6	SB_CKE_1	BF27	MEM_B_CKE<1>		31 82
MEM_B_DQ<7>	AR1	SB_DQ_7					
MEM_B_DQ<8>	AU4	SB_DQ_8	SB_CS_0*	BE41	MEM_B_CS_L<0>		31 82
MEM_B_DQ<9>	AT2	SB_DQ_9	SB_CS_1*	BE47	MEM_B_CS_L<1>		31 82
MEM_B_DQ<10>	AV4	SB_DQ_10					
MEM_B_DQ<11>	BA4	SB_DQ_11	SB_ODT_0	AT43	MEM_B_ODT<0>		31 82
MEM_B_DQ<12>	AU3	SB_DQ_12	SB_ODT_1	BG47	MEM_B_ODT<1>		31 82
MEM_B_DQ<13>	AR3	SB_DQ_13					
MEM_B_DQ<14>	AY2	SB_DQ_14	SB_DQS_0*	AL3	MEM_B_DQS_N<0>	82 29	29 82
MEM_B_DQ<15>	BA3	SB_DQ_15	SB_DQS_1*	AV3	MEM_B_DQS_N<1>	82 29	29 82
MEM_B_DQ<16>	BE9	SB_DQ_16	SB_DQS_2*	BG11	MEM_B_DQS_N<2>	82 29	29 82
MEM_B_DQ<17>	BD9	SB_DQ_17	SB_DQS_3*	BD17	MEM_B_DQS_N<3>	82 29	29 82
MEM_B_DQ<18>	BD13	SB_DQ_18	SB_DQS_4*	BG51	MEM_B_DQS_N<4>	82 29	29 82
MEM_B_DQ<19>	BF12	SB_DQ_19	SB_DQS_5*	BA59	MEM_B_DQS_N<5>	82 29	29 82
MEM_B_DQ<20>	BF8	SB_DQ_20	SB_DQS_6*	AT60	MEM_B_DQS_N<6>	82 29	29 82
MEM_B_DQ<21>	BD10	SB_DQ_21	SB_DQS_7*	AK59	MEM_B_DQS_N<7>	82 29	29 82
MEM_B_DQ<22>	BD14	SB_DQ_22					
MEM_B_DQ<23>	BE13	SB_DQ_23	SB_DQS_0	AM2	MEM_B_DQS_P<0>	82 29	29 82
MEM_B_DQ<24>	BF16	SB_DQ_24	SB_DQS_1	AV1	MEM_B_DQS_P<1>	82 29	29 82
MEM_B_DQ<25>	BE17	SB_DQ_25	SB_DQS_2	BE11	MEM_B_DQS_P<2>	82 29	29 82
MEM_B_DQ<26>	BE18	SB_DQ_26	SB_DQS_3	BD18	MEM_B_DQS_P<3>	82 29	29 82
MEM_B_DQ<27>	BE21	SB_DQ_27	SB_DQS_4	BE51	MEM_B_DQS_P<4>	82 29	29 82
MEM_B_DQ<28>	BE14	SB_DQ_28	SB_DQS_5	BA61	MEM_B_DQS_P<5>	82 29	29 82
MEM_B_DQ<29>	BG14	SB_DQ_29	SB_DQS_6	AR59	MEM_B_DQS_P<6>	82 29	29 82
MEM_B_DQ<30>	BG18	SB_DQ_30	SB_DQS_7	AK61	MEM_B_DQS_P<7>	82 29	29 82
MEM_B_DQ<31>	BF19	SB_DQ_31					
MEM_B_DQ<32>	BD50	SB_DQ_32	SB_MA_0	BF32	MEM_B_A<0>		31 82
MEM_B_DQ<33>	BF48	SB_DQ_33	SB_MA_1	BE33	MEM_B_A<1>		31 82
MEM_B_DQ<34>	BD53	SB_DQ_34	SB_MA_2	BD33	MEM_B_A<2>		31 82
MEM_B_DQ<35>	BF52	SB_DQ_35	SB_MA_3	AU30	MEM_B_A<3>		31 82
MEM_B_DQ<36>	BD49	SB_DQ_36	SB_MA_4	BD30	MEM_B_A<4>		31 82
MEM_B_DQ<37>	BE49	SB_DQ_37	SB_MA_5	AV30	MEM_B_A<5>		31 82
MEM_B_DQ<38>	BD54	SB_DQ_38	SB_MA_6	BG30	MEM_B_A<6>		31 82
MEM_B_DQ<39>	BE53	SB_DQ_39	SB_MA_7	BD29	MEM_B_A<7>		31 82
MEM_B_DQ<40>	BF56	SB_DQ_40	SB_MA_8	BE30	MEM_B_A<8>		31 82
MEM_B_DQ<41>	BE57	SB_DQ_41	SB_MA_9	BE28	MEM_B_A<9>		31 82
MEM_B_DQ<42>	BC59	SB_DQ_42	SB_MA_10	BD43	MEM_B_A<10>		31 82
MEM_B_DQ<43>	AY60	SB_DQ_43	SB_MA_11	AT28	MEM_B_A<11>		31 82
MEM_B_DQ<44>	BE54	SB_DQ_44	SB_MA_12	AV28	MEM_B_A<12>		31 82
MEM_B_DQ<45>	BG54	SB_DQ_45	SB_MA_13	BD46	MEM_B_A<13>		31 82
MEM_B_DQ<46>	BA58	SB_DQ_46	SB_MA_14	AT26	MEM_B_A<14>		31 82
MEM_B_DQ<47>	AW59	SB_DQ_47	SB_MA_15	AU22	MEM_B_A<15>		31 82
MEM_B_DQ<48>	AW58	SB_DQ_48					
MEM_B_DQ<49>	AU58	SB_DQ_49					
MEM_B_DQ<50>	AN61	SB_DQ_50					
MEM_B_DQ<51>	AN59	SB_DQ_51					
MEM_B_DQ<52>	AU59	SB_DQ_52					
MEM_B_DQ<53>	AU61	SB_DQ_53					
MEM_B_DQ<54>	AN58	SB_DQ_54					
MEM_B_DQ<55>	AR58	SB_DQ_55					
MEM_B_DQ<56>	AK58	SB_DQ_56					
MEM_B_DQ<57>	AL58	SB_DQ_57					
MEM_B_DQ<58>	AG58	SB_DQ_58					
MEM_B_DQ<59>	AG59	SB_DQ_59					
MEM_B_DQ<60>	AM60	SB_DQ_60					
MEM_B_DQ<61>	AL59	SB_DQ_61					
MEM_B_DQ<62>	AF61	SB_DQ_62					
MEM_B_DQ<63>	AH60	SB_DQ_63					
MEM_B_BA<0>	BG39	SB_BS_0					
MEM_B_BA<1>	BD42	SB_BS_1					
MEM_B_BA<2>	AT22	SB_BS_2					
MEM_B_CAS_L	AV43	SB_CAS*					
MEM_B_RAS_L	BF40	SB_RAS*					
MEM_B_WE_L	BD45	SB_WE*					

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CPU DDR3 INTERFACES

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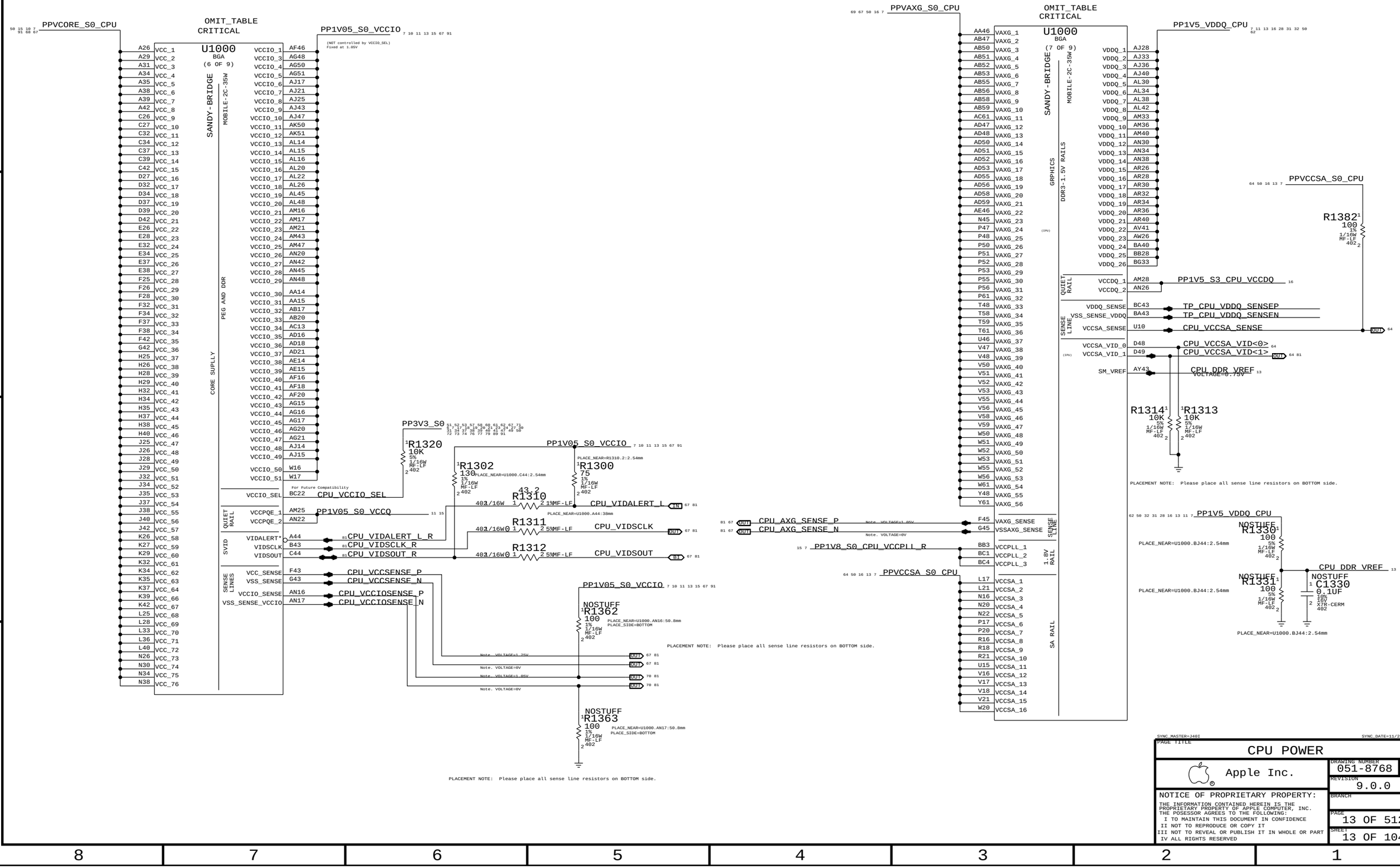

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CPU POWER

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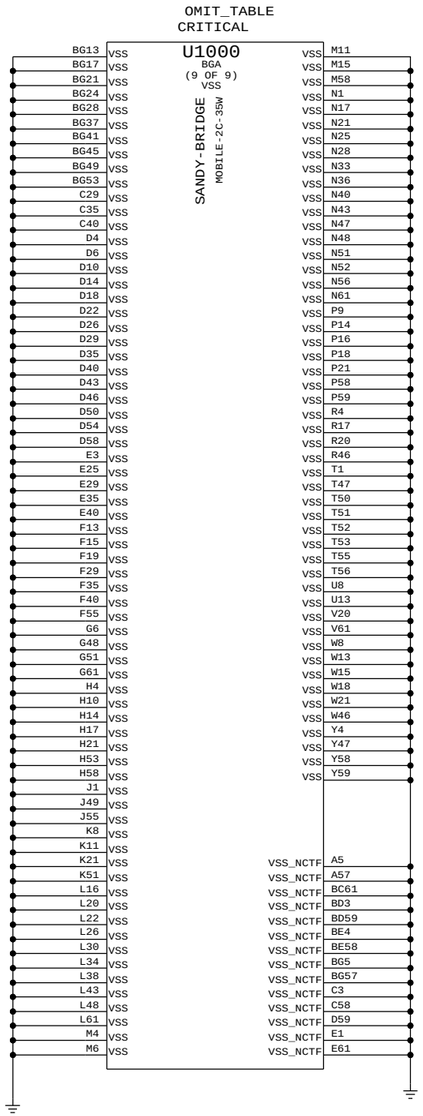

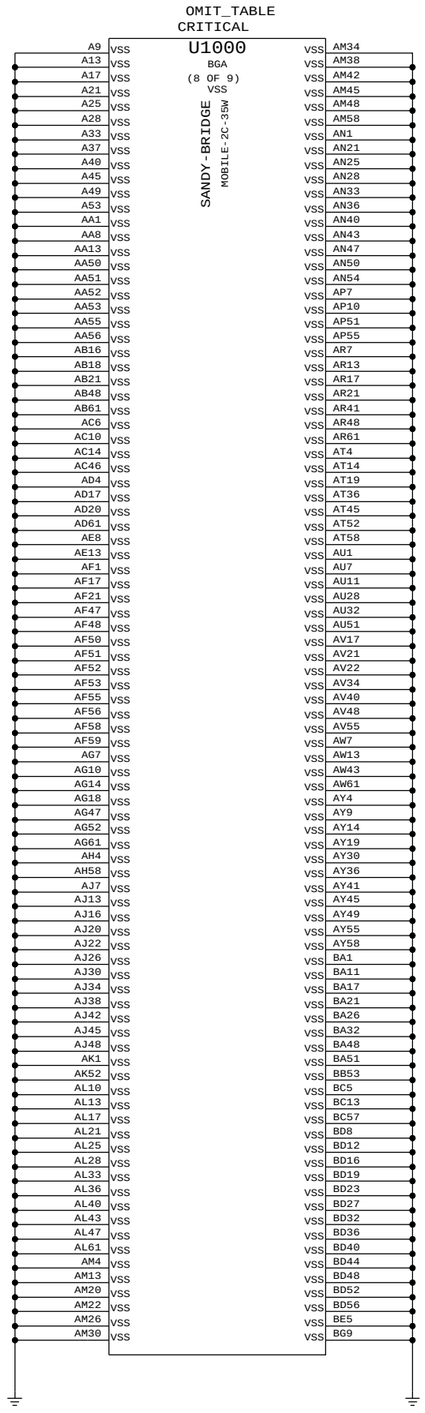

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CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

91 68 67 50 13 10 7 PPVCORE_S0_CPU

C1600 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1601 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1602 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1603 2.2UF 20% 6.3V CERM 402-LF
C1604 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1605 2.2UF 20% 6.3V CERM 402-LF
C1606 2.2UF 20% 6.3V CERM 402-LF
C1607 2.2UF 20% 6.3V CERM 402-LF
C1608 2.2UF 20% 6.3V CERM 402-LF
C1609 2.2UF 20% 6.3V CERM 402-LF
C1610 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1611 2.2UF 20% 6.3V CERM 402-LF
C1612 2.2UF 20% 6.3V CERM 402-LF
C1613 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1614 2.2UF 20% 6.3V CERM 402-LF
C1615 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1616 2.2UF 20% 6.3V CERM 402-LF
C1617 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1618 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1619 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1620 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1621 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1622 2.2UF 20% 6.3V CERM 402-LF
C1623 2.2UF 20% 6.3V CERM 402-LF
C1624 2.2UF 20% 6.3V CERM 402-LF

NOSTUFF C1625 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1626 2.2UF 20% 6.3V CERM 402-LF
C1627 2.2UF 20% 6.3V CERM 402-LF
C1628 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1629 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1630 2.2UF 20% 6.3V CERM 402-LF
C1631 2.2UF 20% 6.3V CERM 402-LF
C1632 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1633 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1634 2.2UF 20% 6.3V CERM 402-LF
C1635 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1636 2.2UF 20% 6.3V CERM 402-LF
C1637 2.2UF 20% 6.3V CERM 402-LF
C1638 2.2UF 20% 6.3V CERM 402-LF
C1639 2.2UF 20% 6.3V CERM 402-LF
C1640 2.2UF 20% 6.3V CERM 402-LF
C1641 2.2UF 20% 6.3V CERM 402-LF
C1642 2.2UF 20% 6.3V CERM 402-LF
C1643 2.2UF 20% 6.3V CERM 402-LF
C1644 2.2UF 20% 6.3V CERM 402-LF
C1645 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1646 2.2UF 20% 6.3V CERM 402-LF
C1647 2.2UF 20% 6.3V CERM 402-LF
C1648 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1649 2.2UF 20% 6.3V CERM 402-LF

C1650 2.2UF 20% 6.3V CERM 402-LF
C1651 2.2UF 20% 6.3V CERM 402-LF
C1652 2.2UF 20% 6.3V CERM 402-LF
C1653 2.2UF 20% 6.3V CERM 402-LF
C1654 2.2UF 20% 6.3V CERM 402-LF

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 22UF 20% 6.3V X5R-CERM1 0603
C1656 22UF 20% 6.3V X5R-CERM1 0603
C1657 22UF 20% 6.3V X5R-CERM1 0603
C1658 22UF 20% 6.3V X5R-CERM1 0603
C1659 22UF 20% 6.3V X5R-CERM1 0603
C1660 22UF 20% 6.3V X5R-CERM1 0603
C1661 22UF 20% 6.3V X5R-CERM1 0603
C1662 22UF 20% 6.3V X5R-CERM1 0603
C1663 22UF 20% 6.3V X5R-CERM1 0603
C1664 22UF 20% 6.3V X5R-CERM1 0603
C1665 22UF 20% 6.3V X5R-CERM1 0603
C1666 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 22UF 20% 6.3V X5R-CERM1 0603
C1668 22UF 20% 6.3V X5R-CERM1 0603
C1669 22UF 20% 6.3V X5R-CERM1 0603
C1670 22UF 20% 6.3V X5R-CERM1 0603
C1671 22UF 20% 6.3V X5R-CERM1 0603
C1672 22UF 20% 6.3V X5R-CERM1 0603
C1673 22UF 20% 6.3V X5R-CERM1 0603
C1674 22UF 20% 6.3V X5R-CERM1 0603
C1675 22UF 20% 6.3V X5R-CERM1 0603
C1676 22UF 20% 6.3V X5R-CERM1 0603
C1677 22UF 20% 6.3V X5R-CERM1 0603
C1678 22UF 20% 6.3V X5R-CERM1 0603
C1679 22UF 20% 6.3V X5R-CERM1 0603

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

13 11 10 7 91 67 PP1V05_S0_VCCIO

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

C1684 1UF 10% 10V X5R 402-1
C1685 1UF 10% 10V X5R 402-1
C1686 1UF 10% 10V X5R 402-1
C1687 1UF 10% 10V X5R 402-1
C1688 1UF 10% 10V X5R 402-1
C1689 1UF 10% 10V X5R 402-1
C1690 1UF 10% 10V X5R 402-1
C1691 1UF 10% 10V X5R 402-1
C1692 1UF 10% 10V X5R 402-1
C1693 1UF 10% 10V X5R 402-1
C1694 1UF 10% 10V X5R 402-1
C1695 1UF 10% 10V X5R 402-1
C1696 1UF 10% 10V X5R 402-1

C1697 1UF 10% 10V X5R 402-1
C1698 1UF 10% 10V X5R 402-1
C1699 1UF 10% 10V X5R 402-1
C169A 1UF 10% 10V X5R 402-1
C169B 1UF 10% 10V X5R 402-1
C169C 1UF 10% 10V X5R 402-1
C169D 1UF 10% 10V X5R 402-1
C169E 1UF 10% 10V X5R 402-1
C169F 1UF 10% 10V X5R 402-1
C161A 1UF 10% 10V X5R 402-1
C161B 1UF 10% 10V X5R 402-1
C161C 1UF 10% 10V X5R 402-1
C161D 1UF 10% 10V X5R 402-1

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V X5R 603
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

CRITICAL
R1601 0.010 1% 1/4W MF 0603

PP1V05_S0_VCCQ 11 13
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM

C167F 1UF 10% 10V X5R 402-1

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

71 26 23 21 18 7 PP1V8_S0

R1600 0 5% 1/16W MF-LF 402
PLACE_NEAR=U1000.A662:2.54 mm:NO_VIA

PP1V8_S0_CPU_VCCPLL_R 7 13

C160X 1UF 10% 10V X5R 402-1
C160Y 1UF 10% 10V X5R 402-1
PLACE_NEAR=U1000.A665:2.54 mm:NO_VIA

CRITICAL
C160Z 270UF 20% 2V TANT CASE-B4-SM
PLACE_NEAR=U1000.A661:5mm

CPU VCCPLL Low pass filter

SYNC_MASTER=J40I SYNC_DATE=11/23/2010

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

69 67 50 13 7 PPVAXG_S0_CPU

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402-1
C1701 1UF 10% 10V X5R 402-1
C1702 1UF 10% 10V X5R 402-1
C1703 1UF 10% 10V X5R 402-1
C1704 1UF 10% 10V X5R 402-1
C1705 1UF 10% 10V X5R 402-1
C1706 1UF 10% 10V X5R 402-1
C1707 1UF 10% 10V X5R 402-1
C1708 1UF 10% 10V X5R 402-1
C1709 1UF 10% 10V X5R 402-1
C1710 1UF 10% 10V X5R 402-1

C1770 10PF 5% 25V NPO 201
C1771 10PF 5% 25V NPO 201
C1772 10PF 5% 25V NPO 201
C1773 10PF 5% 25V NPO 201
C1774 10PF 5% 25V NPO 201
C1775 10PF 5% 25V NPO 201

PLACEMENT_NOTE (C1711-C1716):

C1711 10UF 20% 6.3V CERM-X5R 0402-1
C1712 10UF 20% 6.3V CERM-X5R 0402-1
C1713 10UF 20% 6.3V CERM-X5R 0402-1
C1714 10UF 20% 6.3V CERM-X5R 0402-1
C1715 10UF 20% 6.3V CERM-X5R 0402-1
C1716 10UF 20% 6.3V CERM-X5R 0402-1

C1776 10PF 5% 25V NPO 201
C1777 10PF 5% 25V NPO 201
C1778 10PF 5% 25V NPO 201
C1779 10PF 5% 25V NPO 201
C1780 10PF 5% 25V NPO 201
C1781 10PF 5% 25V NPO 201

PLACEMENT_NOTE (C1717-C1722):

C1717 22UF 20% 6.3V X5R-CERM1 0603
C1718 22UF 20% 6.3V X5R-CERM1 0603
C1719 22UF 20% 6.3V X5R-CERM1 0603
C1720 22UF 20% 6.3V X5R-CERM1 0603
C1721 22UF 20% 6.3V X5R-CERM1 0603
C1722 22UF 20% 6.3V X5R-CERM1 0603

C1782 10PF 5% 25V NPO 201
C1783 10PF 5% 25V NPO 201
C1784 10PF 5% 25V NPO 201
C1785 10PF 5% 25V NPO 201
C1786 10PF 5% 25V NPO 201
C1787 10PF 5% 25V NPO 201

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

62 50 32 31 28 13 11 7 PP1V5_VDDQ_CPU

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402-1
C1739 1UF 10% 10V X5R 402-1
C1740 1UF 10% 10V X5R 402-1
C1741 1UF 10% 10V X5R 402-1
C1742 1UF 10% 10V X5R 402-1
C1743 1UF 10% 10V X5R 402-1
C1744 1UF 10% 10V X5R 402-1
C1745 1UF 10% 10V X5R 402-1
C1746 1UF 10% 10V X5R 402-1
C1747 1UF 10% 10V X5R 402-1

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL
C1756 270UF 20% 2V TANT CASE-B4-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

CRITICAL
R1702 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 13

C1757 1UF 10% 10V X5R 402-1

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

64 50 13 7 PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402-1
C1759 1UF 10% 10V X5R 402-1
C1760 1UF 10% 10V X5R 402-1
C1761 1UF 10% 10V X5R 402-1
C1762 1UF 10% 10V X5R 402-1

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL
C1768 270UF 20% 2V TANT CASE-B4-SM

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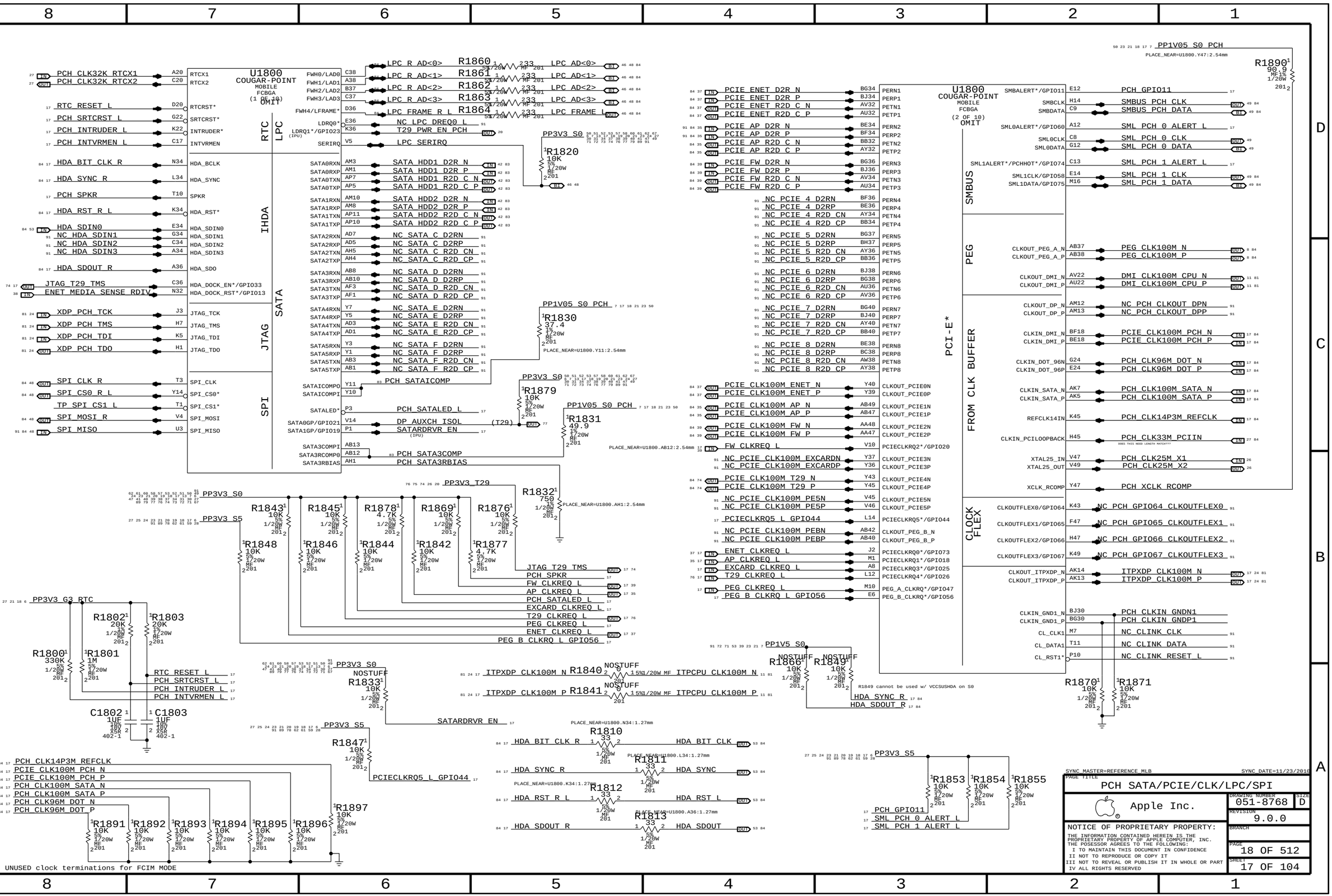
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MOBILE
FCBGA
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OMIT
RTC
LPC
IHDA
SATA
JTAG
SPI
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PCH CLK32K RTCX2
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
HDA BIT CLK R
HDA SYNC R
PCH SPKR
HDA RST R L
HDA SDIN0
NC HDA SDIN1
NC HDA SDIN2
NC HDA SDIN3
HDA SDOUT R
JTAG T29 TMS
ENET MEDIA SENSE RDIV
XDP PCH TCK
XDP PCH TMS
XDP PCH TDI
XDP PCH TDO
SPI CLK R
SPI CS0 R L
TP SPI CS1 L
SPI MOSI R
SPI MISO
LPC R AD<0>
LPC R AD<1>
LPC R AD<2>
LPC R AD<3>
LPC FRAME R L
NC LPC DREQ0 L
T29 PWR EN PCH
LPC SERIRQ
SATA HDD1 D2R N
SATA HDD1 D2R P
SATA HDD1 R2D C N
SATA HDD1 R2D C P
SATA HDD2 D2R N
SATA HDD2 D2R P
SATA HDD2 R2D C N
SATA HDD2 R2D C P
NC SATA C D2RN
NC SATA C D2RP
NC SATA C R2D CN
NC SATA C R2D CP
NC SATA D D2RN
NC SATA D D2RP
NC SATA D R2D CN
NC SATA D R2D CP
NC SATA E D2RN
NC SATA E D2RP
NC SATA E R2D CN
NC SATA E R2D CP
NC SATA F D2RN
NC SATA F D2RP
NC SATA F R2D CN
NC SATA F R2D CP
PCH SATAICOMP
PCH SATALED L
DP AUXCH ISOL
SATARDRVR EN
PCH SATA3COMP
PCH SATA3RBIAS
PP3V3 S0
PP1V05 S0 PCH
PP3V3 T29
PP3V3 S5
PP3V3 G3 RTC
PCIE ENET D2R N
PCIE ENET D2R P
PCIE ENET R2D C N
PCIE ENET R2D C P
PCIE AP D2R N
PCIE AP D2R P
PCIE AP R2D C N
PCIE AP R2D C P
PCIE FW D2R N
PCIE FW D2R P
PCIE FW R2D C N
PCIE FW R2D C P
NC PCIE 4 D2RN
NC PCIE 4 D2RP
NC PCIE 4 R2D CN
NC PCIE 4 R2D CP
NC PCIE 5 D2RN
NC PCIE 5 D2RP
NC PCIE 5 R2D CN
NC PCIE 5 R2D CP
NC PCIE 6 D2RN
NC PCIE 6 D2RP
NC PCIE 6 R2D CN
NC PCIE 6 R2D CP
NC PCIE 7 D2RN
NC PCIE 7 D2RP
NC PCIE 7 R2D CN
NC PCIE 7 R2D CP
NC PCIE 8 D2RN
NC PCIE 8 D2RP
NC PCIE 8 R2D CN
NC PCIE 8 R2D CP
PCIE CLK100M ENET N
PCIE CLK100M ENET P
PCIE CLK100M AP N
PCIE CLK100M AP P
PCIE CLK100M FW N
PCIE CLK100M FW P
FW CLKREQ L
NC PCIE CLK100M EXCARDN
NC PCIE CLK100M EXCARDP
PCIE CLK100M T29 N
PCIE CLK100M T29 P
NC PCIE CLK100M PE5N
NC PCIE CLK100M PE5P
PCIECLKRQ5 L GPIO44
NC PCIE CLK100M PEBN
NC PCIE CLK100M PEBP
ENET CLKREQ L
AP CLKREQ L
EXCARD CLKREQ L
T29 CLKREQ L
PEG CLKREQ L
PEG B CLKRQ L GPIO56
SMBUS
PEG
FROM CLK BUFFER
PCI-E*
CLOCK FLEX
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
PCH GPIO11
SMBUS PCH CLK
SMBUS PCH DATA
SML PCH 0 ALERT L
SML PCH 0 CLK
SML PCH 0 DATA
SML PCH 1 ALERT L
SML PCH 1 CLK
SML PCH 1 DATA
CLKOUT PEG A N
CLKOUT PEG A P
CLKOUT DMI N
CLKOUT DMI P
CLKOUT DP N
CLKOUT DP P
CLKIN DMI N
CLKIN DMI P
CLKIN DOT 96N
CLKIN DOT 96P
CLKIN SATA N
CLKIN SATA P
REFCLK14IN
CLKIN PCILOOPBACK
XTAL25 IN
XTAL25 OUT
XCLK RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT ITPXDP N
CLKOUT ITPXDP P
CLKIN GND1 N
CLKIN GND1 P
CL CLK1
CL DATA1
CL RST1*
PEG CLK100M N
PEG CLK100M P
DMI CLK100M CPU N
DMI CLK100M CPU P
NC PCH CLKOUT DPN
NC PCH CLKOUT DPP
PCIE CLK100M PCH N
PCIE CLK100M PCH P
PCH CLK96M DOT N
PCH CLK96M DOT P
PCH CLK100M SATA N
PCH CLK100M SATA P
PCH CLK14P3M REFCLK
PCH CLK33M PCIIN
PCH CLK25M X1
PCH CLK25M X2
PCH XCLK RCOMP
NC PCH GPIO64 CLKOUTFLEX0
NC PCH GPIO65 CLKOUTFLEX1
NC PCH GPIO66 CLKOUTFLEX2
NC PCH GPIO67 CLKOUTFLEX3
ITPXDP CLK100M N
ITPXDP CLK100M P
PCH CLKIN GNDN1
PCH CLKIN GNDP1
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NC CLINK RESET L
ITPXDP CLK100M N
ITPXDP CLK100M P
ITPCPU CLK100M N
ITPCPU CLK100M P
HDA BIT CLK R
HDA SYNC R
HDA RST R L
HDA SDOUT R
HDA BIT CLK
HDA SYNC
HDA RST L
HDA SDOUT
SATARDRVR EN
PCIECLKRQ5 L GPIO44
PCH GPIO11
SML PCH 0 ALERT L
SML PCH 1 ALERT L
R1849 cannot be used w/ VCCSUSHDA on S0
UNUSED clock terminations for FCIM MODE
SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2010
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PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER
051-8768
SIZE
D
REVISION
9.0.0
BRANCH
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17 OF 104
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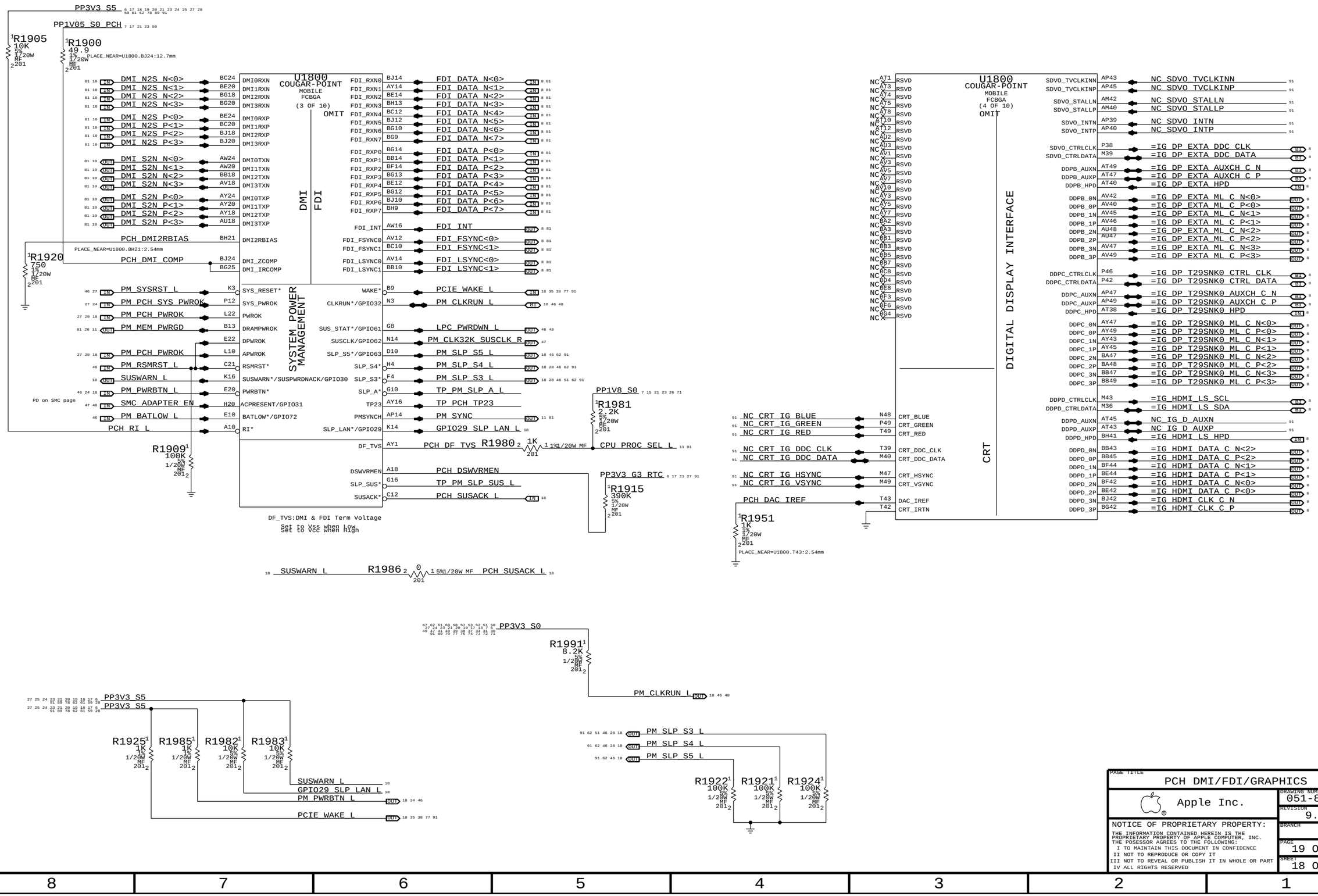
PP3V3_S5
PP1V05_S0_PCH
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201 PLACE_NEAR=U1800.BJ24:12.7mm
U1800
COUGAR-POINT
MOBILE
FCBGA
(3 OF 10)
OMIT
DMI
FDI
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
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DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI2RBIAS
R1920 750 1% 1/20W MF 201
PCH_DMI_COMP
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
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FDI_DATA_N<4>
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FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_INT
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_LSYNC<0>
FDI_LSYNC<1>
SYSTEM_POWER MANAGEMENT
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_MEM_PWRGD
PM_PCH_PWROK
PM_RSMRST_L
SUSWARN_L
PM_PWRBTN_L
PD on SMC page
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
TP_PCH_TP23
PM_SYNC
GPIO29_SLP_LAN_L
R1909 100K 5% 1/20W MF 201
PCH_DF_TVS
R1980 1K 1% 1/20W MF 201
CPU_PROC_SEL_L
PCH_DSWVRMEN
TP_PM_SLP_SUS_L
PCH_SUSACK_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when low
Set to Vcc when high
PP1V8_S0
R1981 2.2K 5% 1/20W MF 201
PP3V3_G3_RTC
R1915 390K 5% 1/20W MF 201
R1986 0 5% 1/20W MF
SUSWARN_L
PCH_SUSACK_L
PP3V3_S0
R1991 8.2K 5% 1/20W MF 201
PM_CLKRUN_L
PM_SLP_S3_L
PM_SLP_S4_L
PM_SLP_S5_L
R1922 100K 5% 1/20W MF 201
R1921 100K 5% 1/20W MF 201
R1924 100K 5% 1/20W MF 201
PP3V3_S5
R1925 1K 1% 1/20W MF 201
R1985 1K 1% 1/20W MF 201
R1982 10K 5% 1/20W MF 201
R1983 10K 5% 1/20W MF 201
SUSWARN_L
GPIO29_SLP_LAN_L
PM_PWRBTN_L
PCIE_WAKE_L
U1800
COUGAR-POINT
MOBILE
FCBGA
(4 OF 10)
OMIT
DIGITAL DISPLAY INTERFACE
CRT
NC_CRT_IG_BLUE
NC_CRT_IG_GREEN
NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC
PCH_DAC_IREF
R1951 1K 1% 1/20W MF 201 PLACE_NEAR=U1800.T43:2.54mm
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN
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NC_SDVO_TVCLKINP
NC_SDVO_STALLN
NC_SDVO_STALLP
NC_SDVO_INTN
NC_SDVO_INTP
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NC_IG_D_AUXP
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PAGE TITLE
PCH DMI/FDI/GRAPHICS
Apple Inc.
DRAWING NUMBER 051-8768
SIZE D
REVISION 9.0.0
BRANCH
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SHEET 18 OF 104
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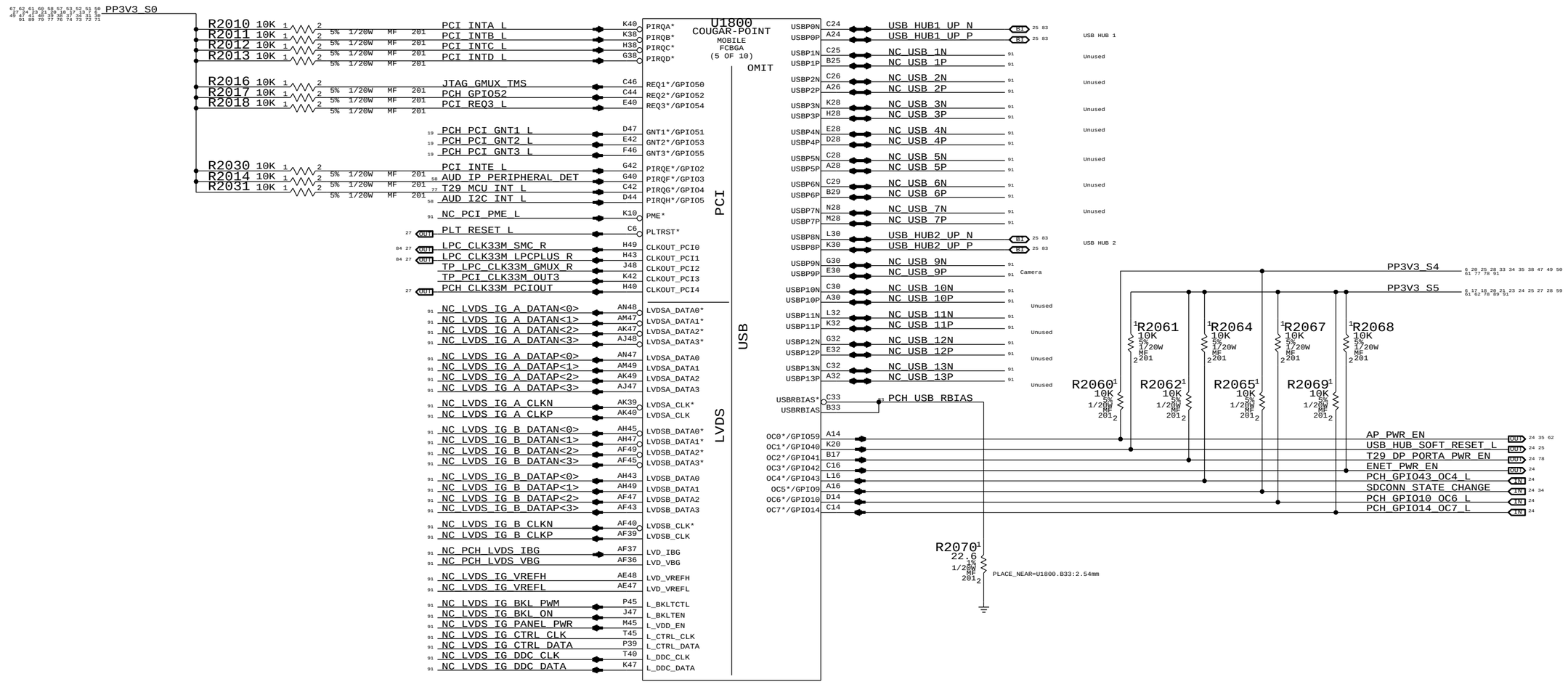

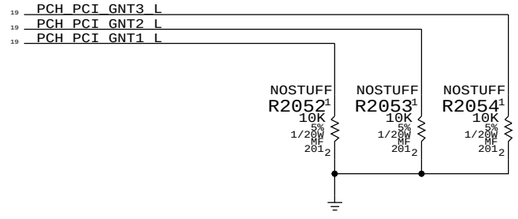

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PAGE TITLE: PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

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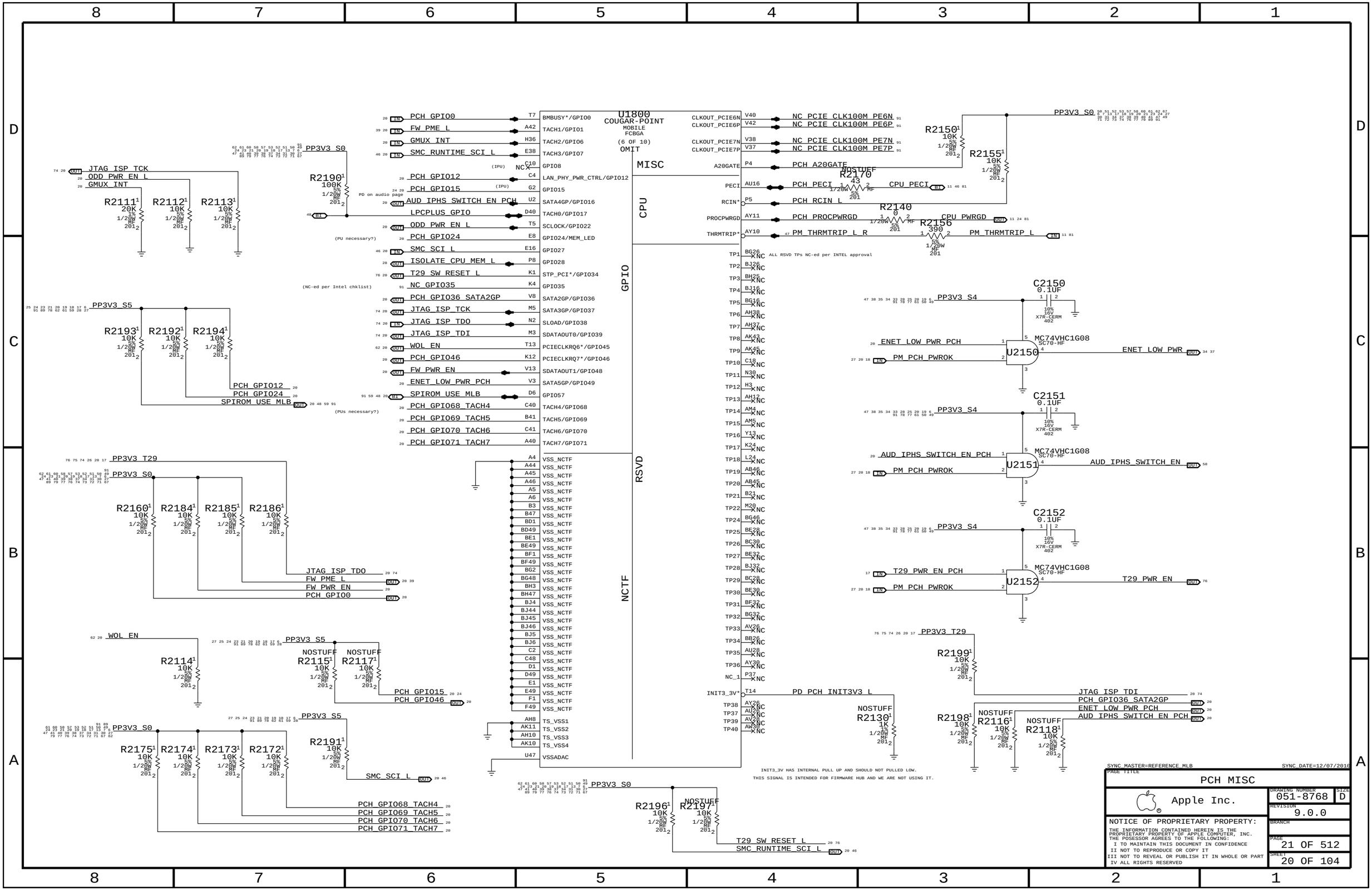
U1800
COUGAR-POINT
MOBILE
FCBGA
(6 OF 10)
OMIT
MISC
CPU
GPIO
RSVD
NCTF
PCH_GPIO0
FW_PME_L
GMUX_INT
SMC_RUNTIME_SCI_L
PCH_GPIO12
PCH_GPIO15
AUD_IPHS_SWITCH_EN_PCH
LPCPLUS_GPIO
ODD_PWR_EN_L
PCH_GPIO24
SMC_SCI_L
ISOLATE_CPU_MEM_L
T29_SW_RESET_L
NC_GPIO35
PCH_GPIO36_SATA2GP
JTAG_ISP_TCK
JTAG_ISP_TDO
JTAG_ISP_TDI
WOL_EN
PCH_GPIO46
FW_PWR_EN
ENET_LOW_PWR_PCH
SPIROM_USE_MLB
PCH_GPIO68_TACH4
PCH_GPIO69_TACH5
PCH_GPIO70_TACH6
PCH_GPIO71_TACH7
NC_PCIE_CLK100M_PE6N
NC_PCIE_CLK100M_PE6P
NC_PCIE_CLK100M_PE7N
NC_PCIE_CLK100M_PE7P
PCH_A20GATE
PCH_PECI
PCH_RCIN_L
PCH_PROCPWRGD
PM_THRMTRIP_L_R
PD_PCH_INIT3V3_L
ALL RSVD TPs NC-ed per INTEL approval
INIT3_3V HAS INTERNAL PULL UP AND SHOULD NOT PULLED LOW.
THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
R2190 100K
R2111 20K
R2112 10K
R2113 10K
R2193 10K
R2192 10K
R2194 10K
R2160 10K
R2184 10K
R2185 10K
R2186 10K
R2114 10K
R2115 NOSTUFF
R2117 10K
R2175 10K
R2174 10K
R2173 10K
R2172 10K
R2191 10K
R2150 10K
R2155 10K
R2170 43
R2140 0
R2156 390
R2199 10K
R2198 10K
R2116 NOSTUFF
R2118 10K
R2130 1K
R2196 10K
R2197 NOSTUFF
C2150 0.1UF
C2151 0.1UF
C2152 0.1UF
U2150 MC74VHC1G08
U2151 MC74VHC1G08
U2152 MC74VHC1G08
PP3V3_S0
PP3V3_S5
PP3V3_T29
PP3V3_S4
PM_PCH_PWROK
CPU_PECI
CPU_PWRGD
PM_THRMTRIP_L
ENET_LOW_PWR
AUD_IPHS_SWITCH_EN
T29_PWR_EN
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SYNC_DATE=12/07/2010
PAGE TITLE
PCH MISC
Apple Inc.
DRAWING NUMBER 051-8768
SIZE D
REVISION 9.0.0
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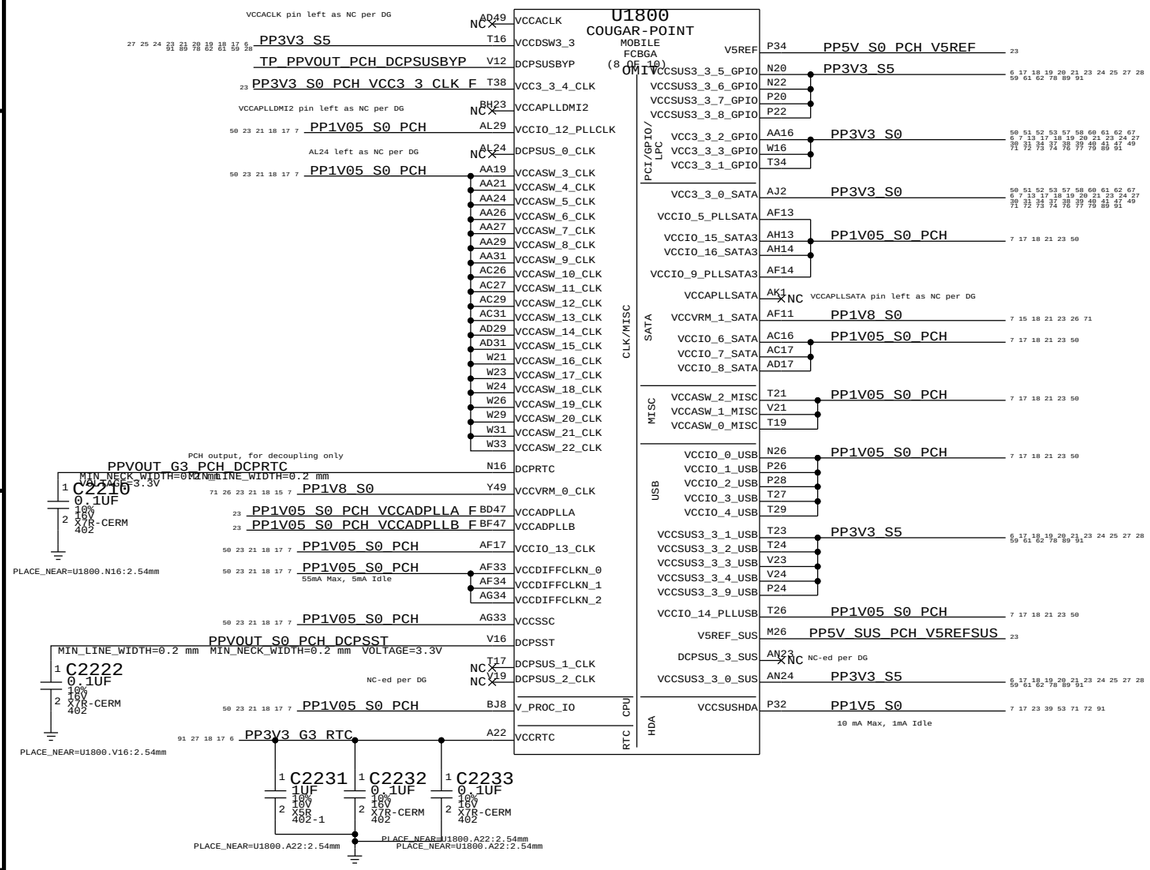

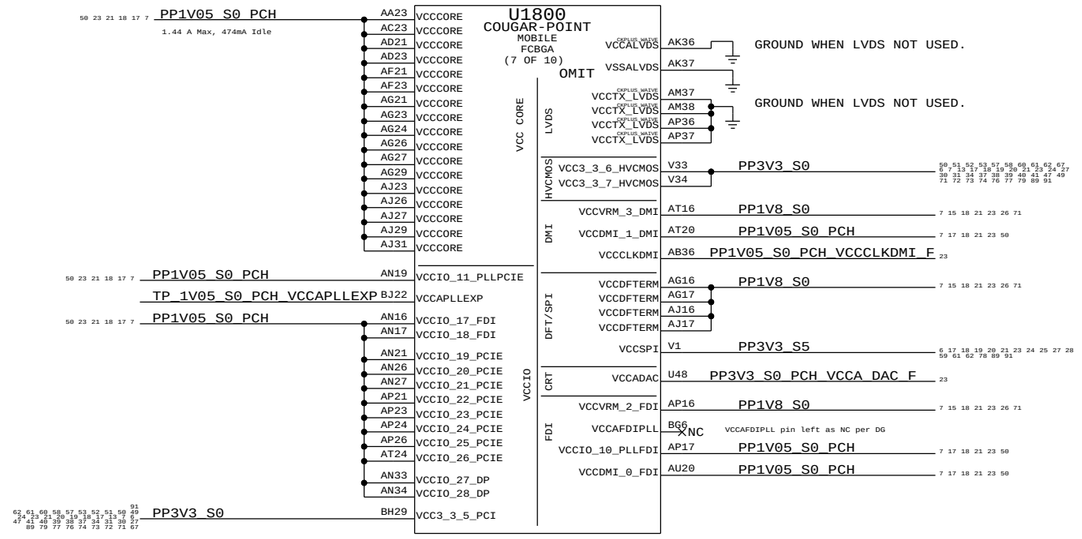

PAGE TITLE	PCH POWER
	Apple Inc.
DRAWING NUMBER	051-8768
SIZE	D
REVISION	9.0.0
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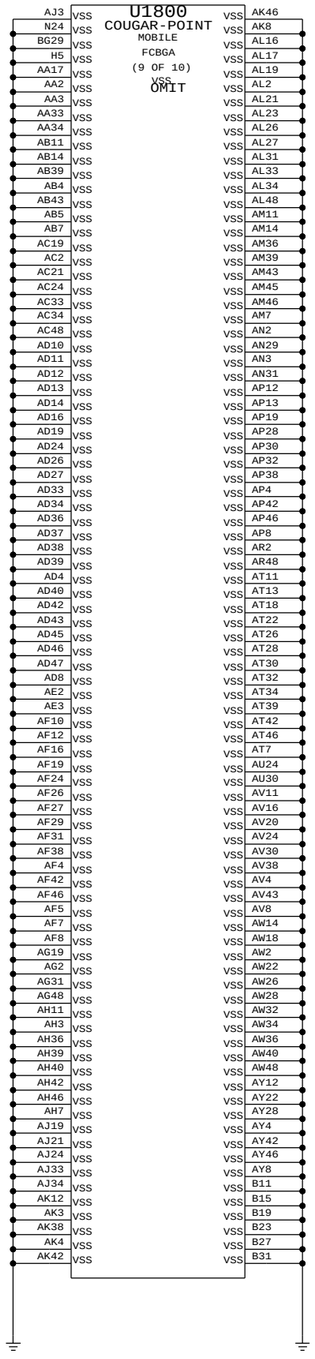

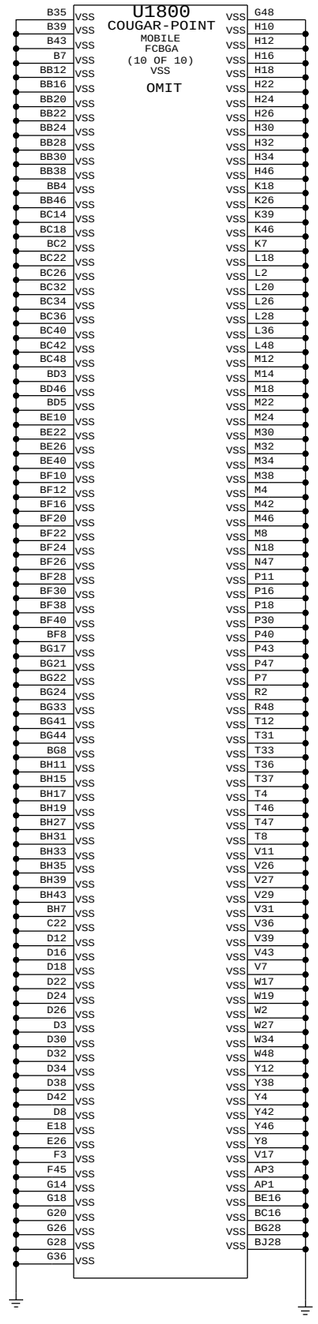

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Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

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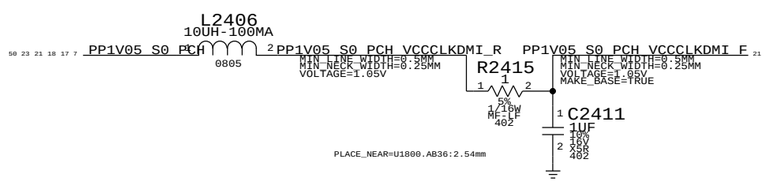

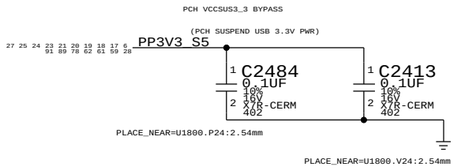

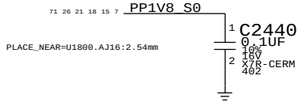

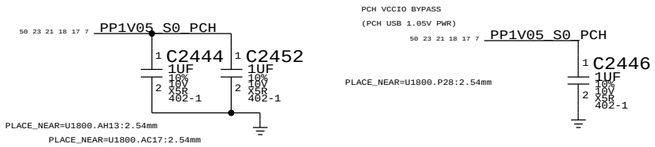

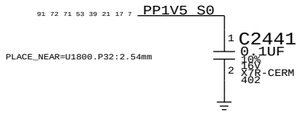

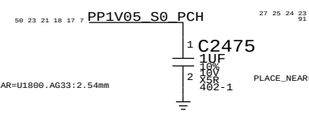

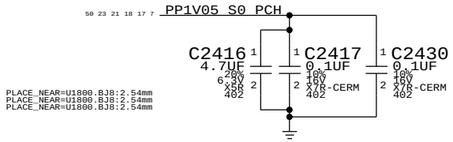

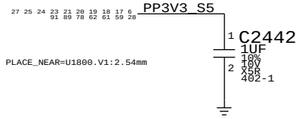

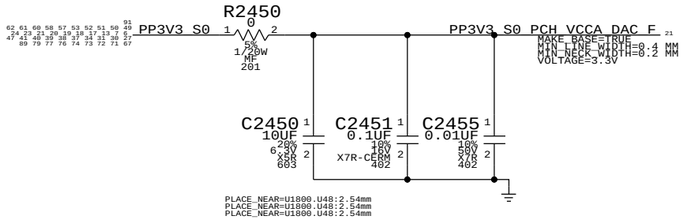

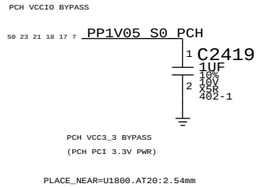

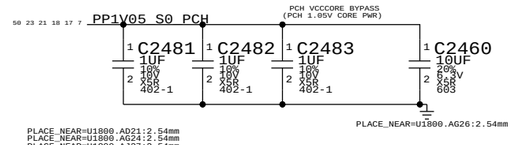

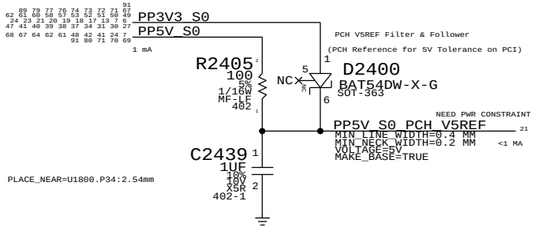

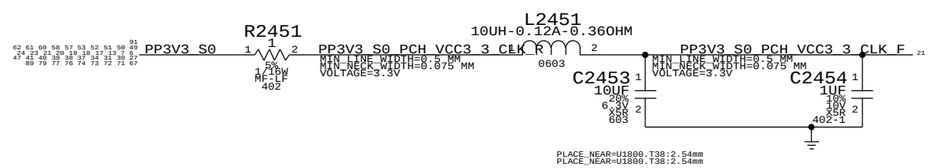

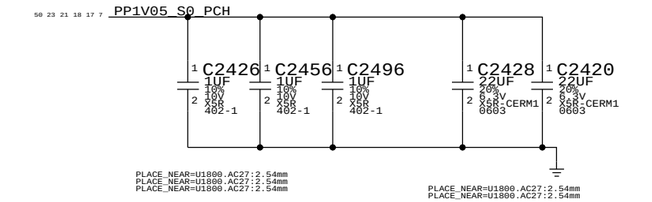

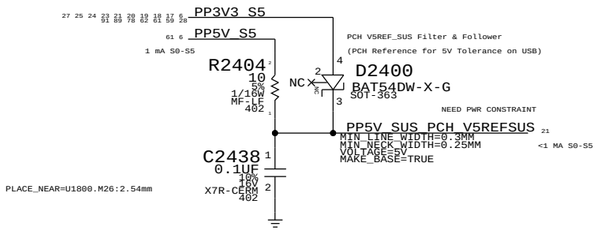

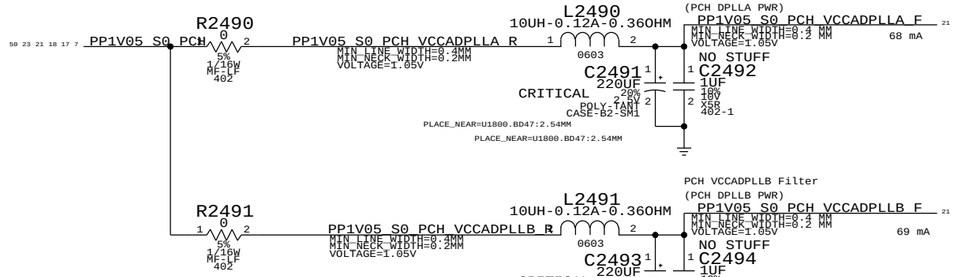

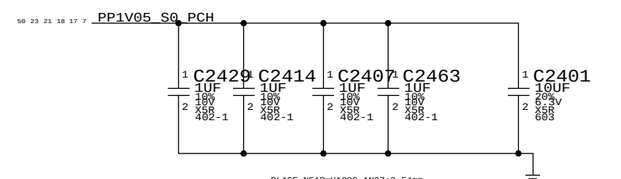

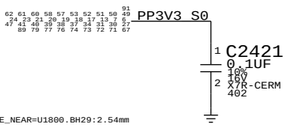

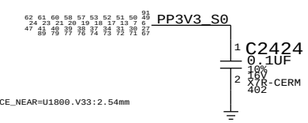

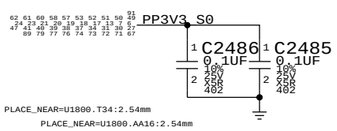

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PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

REVISION 9.0.0

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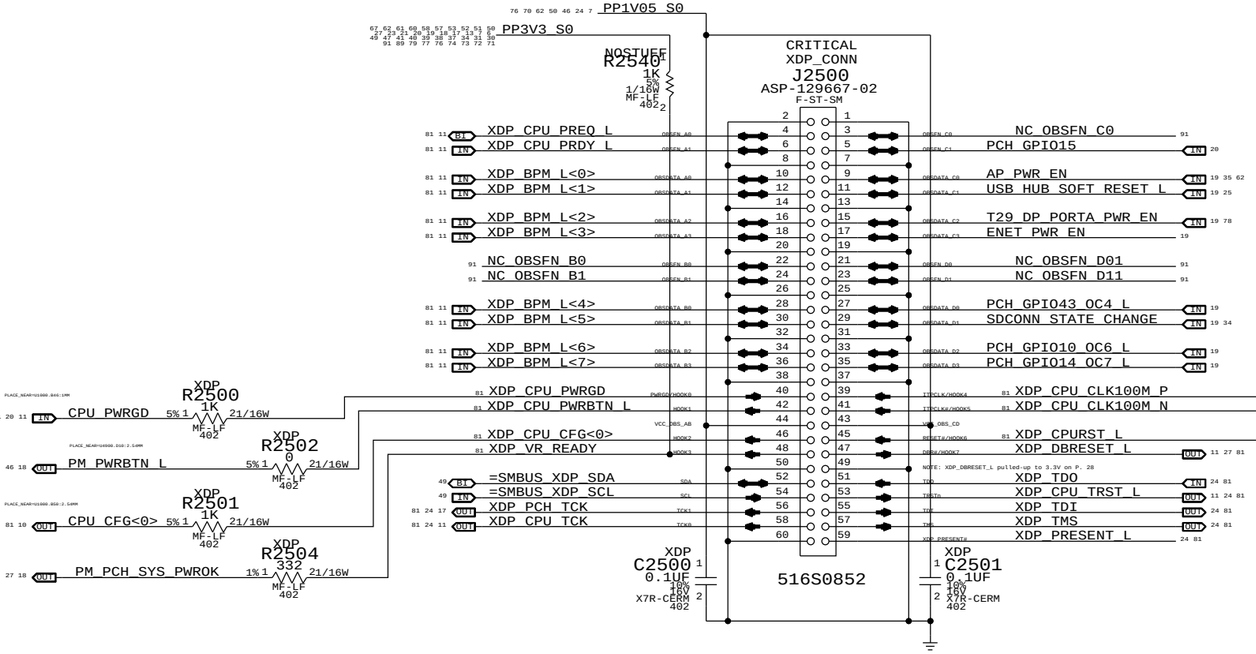
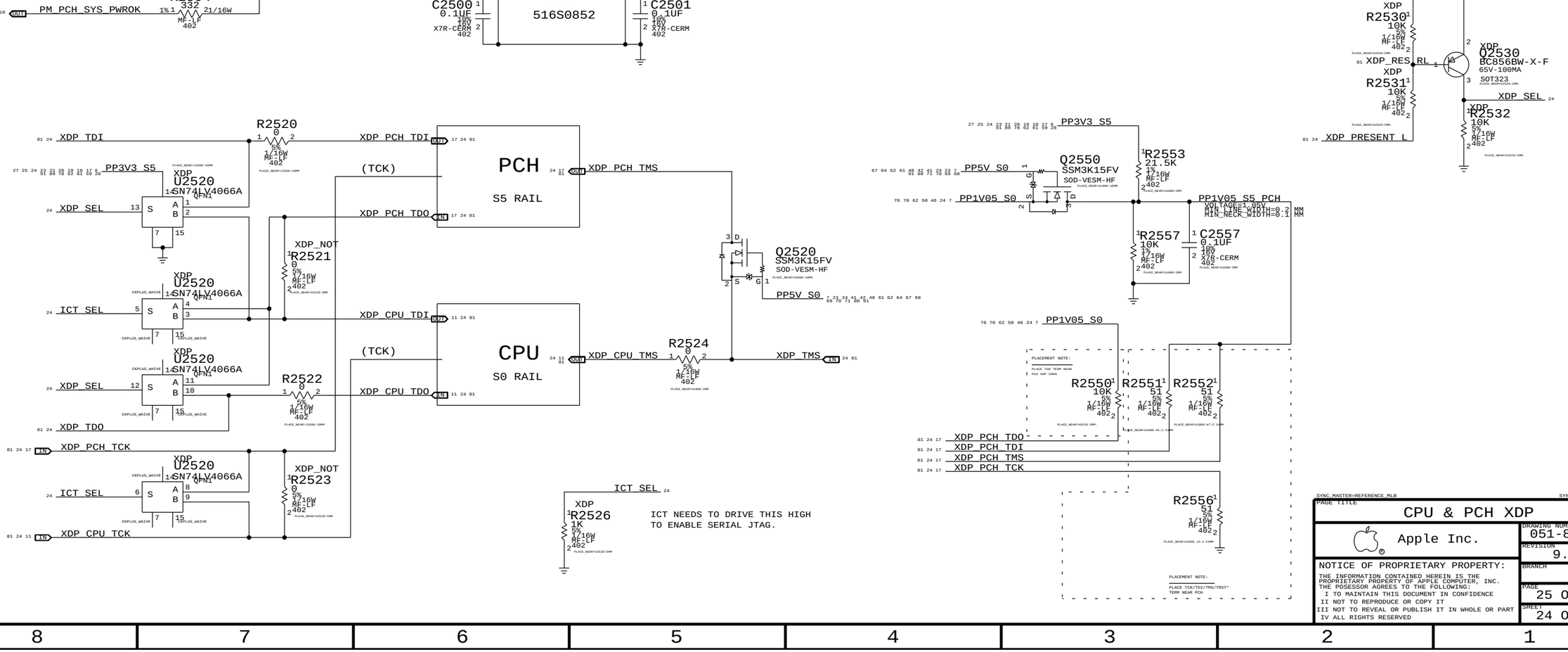
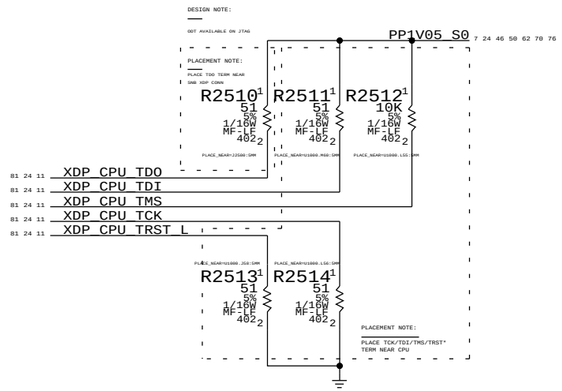
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0620 ADAPTER BOARD TO SUPPORT CPU, PCH DEBUGGING.







SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/30/2010

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

BRANCH:

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BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B

NONREM MEANS NOT CUSTOMER REMOVABLE.
THIS IS A DESIGNATION FOR SOFTWARE USE ONLY.

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2010

PAGE TITLE: USB HUBS

Apple Inc.

DRAWING NUMBER: 051-8768
SIZE: D
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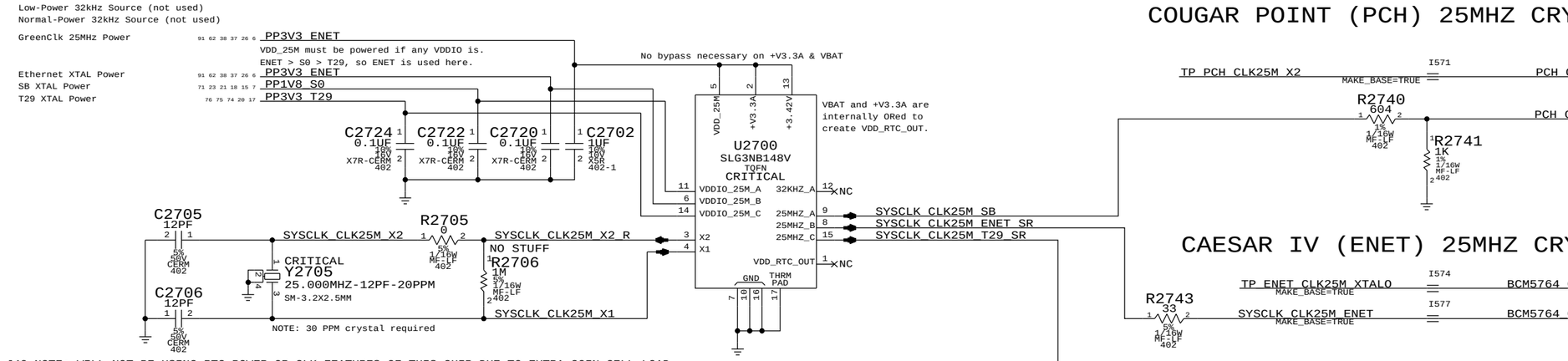
System 25MHz Clock Generator



GREEN CLK

SYNC_MASTER=J40S SYNC_DATE=11/23/2010

PAGE TITLE: CLOCKS, CRYSTALS

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

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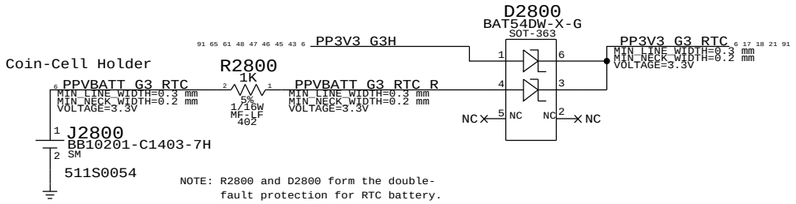
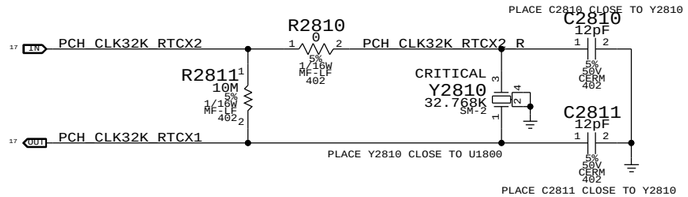
RTC Power Sources



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0062	1	BAT,COIN,LI/MAG,BR2032,3V,190MAH	BAT	CRITICAL	

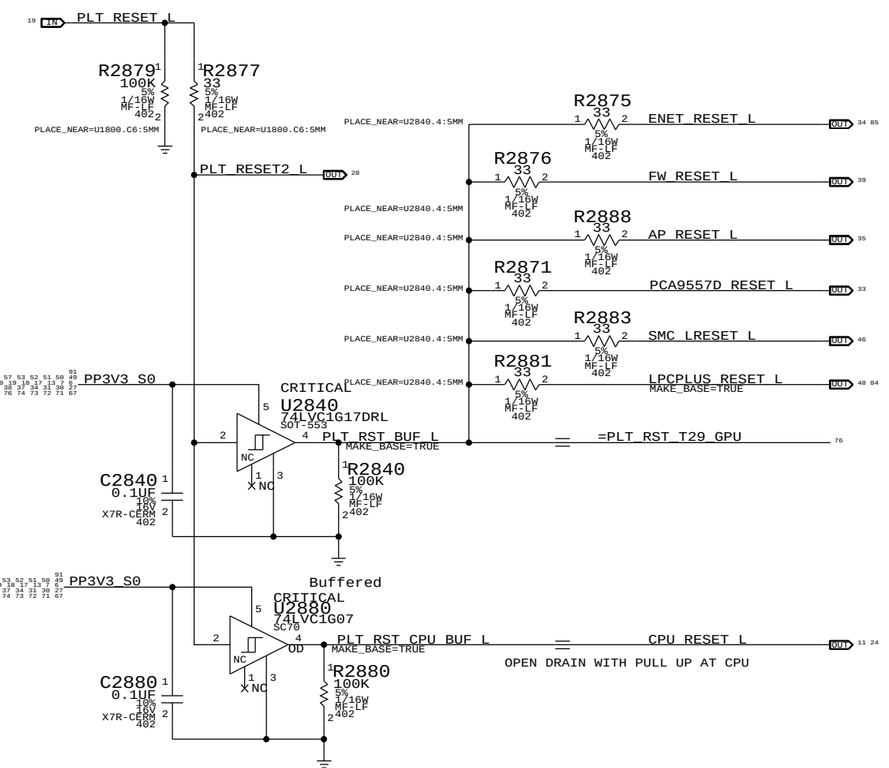
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0074	511S0054	?	?	BATTERY HOLDER WITHOUT ALIGNMENT PEGS

PCH RTC Crystal

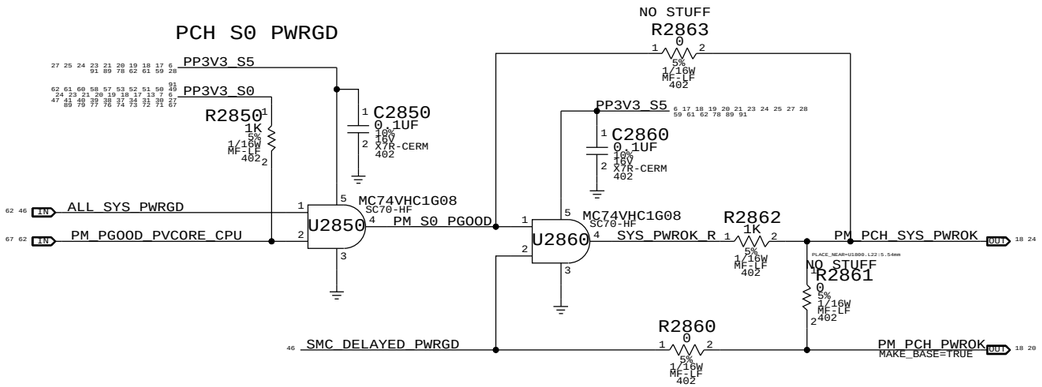


Platform Reset Connections

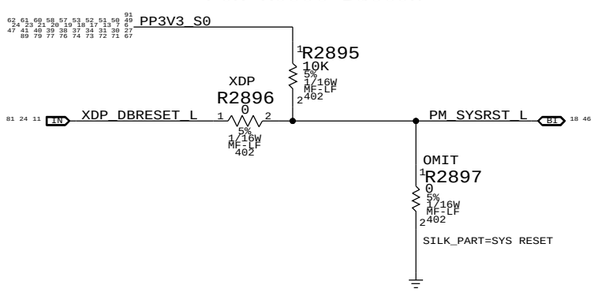
Unbuffered



PCH S0 PWRGD



PCH Reset Button



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/30/2011

PAGE TITLE

RTC SUPPORT, RESETS

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

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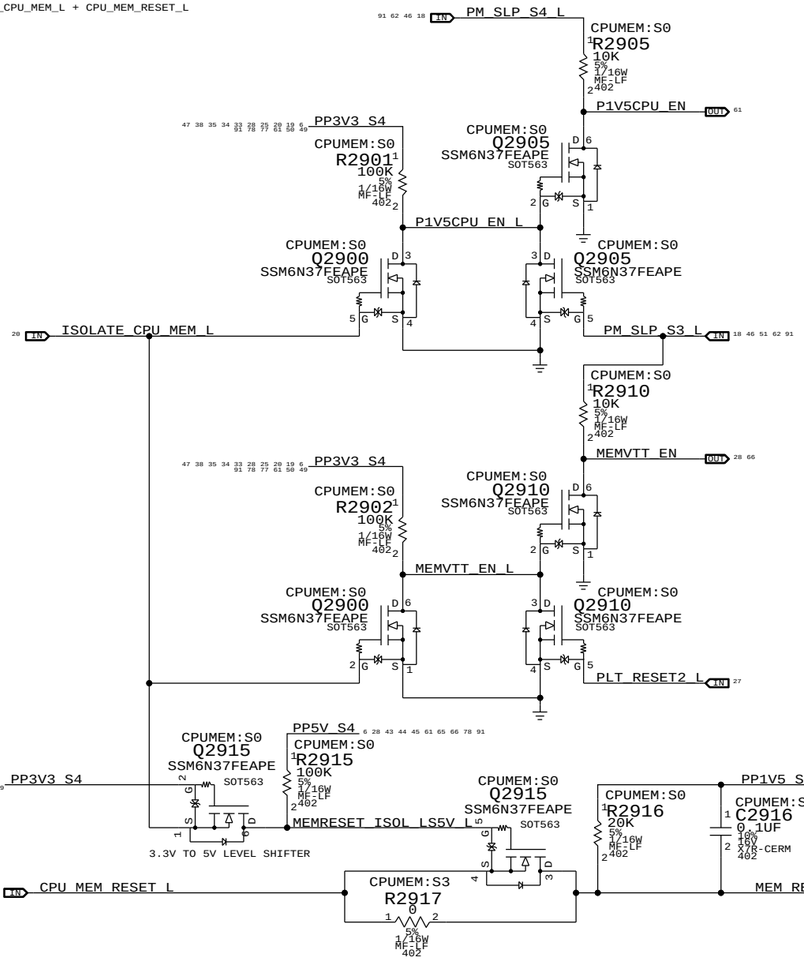
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well
as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN   = (ISOLATE_CPU_MEM_L + PLT_RST_L)   * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

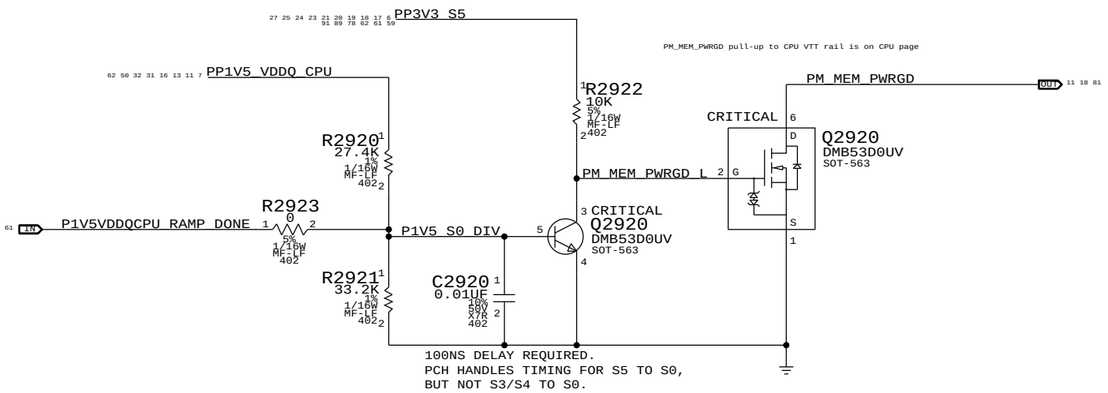


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	0	1
S3	3	0	0	0	1	X	0	0
	4	0	0	1	1	X	0	1
to	5	0	1	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

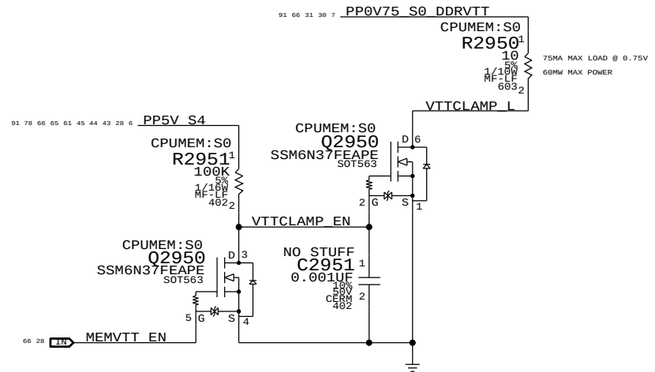
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE	CPU Memory S3 Support
Apple Inc.	DRAWING NUMBER 051-8768 · SIZE D
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Host Partition A 0 -> SO-DIMM A 0

SANDYBRIDGE CPU DOES NOT USE DATA MASK (DM) BITS.
PER PDG, TIE DM BITS TO GND.

MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	30
MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	30
	MAKE_BASE=TRUE	=MEM_A_DM<7>	30
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	30
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	30
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	30
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	30
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	30
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	30
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	30
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	30
	MAKE_BASE=TRUE		

Host Partition A 1 -> SO-DIMM A 1

MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	30
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	30
	MAKE_BASE=TRUE	=MEM_A_DM<6>	30
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	30
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	30
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	30
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	30
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	30
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	30
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	30
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	30
	MAKE_BASE=TRUE		

Host Partition A 2 -> SO-DIMM A 2

MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	30
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	30
	MAKE_BASE=TRUE	=MEM_A_DM<5>	30
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	30
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	30
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	30
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	30
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	30
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	30
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	30
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	30
	MAKE_BASE=TRUE		

Host Partition A 3 -> SO-DIMM A 3

MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	30
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	30
	MAKE_BASE=TRUE	=MEM_A_DM<4>	30
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	30
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	30
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	30
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	30
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	30
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	30
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	30
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	30
	MAKE_BASE=TRUE		

Host Partition A 4 -> SO-DIMM A 4

MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	30
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	30
	MAKE_BASE=TRUE	=MEM_A_DM<3>	30
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	30
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	30
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	30
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	30
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	30
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	30
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	30
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	30
	MAKE_BASE=TRUE		

Host Partition A 5 -> SO-DIMM A 5

MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	30
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	30
	MAKE_BASE=TRUE	=MEM_A_DM<2>	30
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	30
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	30
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	30
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	30
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	30
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	30
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	30
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	30
	MAKE_BASE=TRUE		

Host Partition A 6 -> SO-DIMM A 6

MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	30
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	30
	MAKE_BASE=TRUE	=MEM_A_DM<1>	30
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	30
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	30
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	30
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	30
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	30
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	30
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	30
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	30
	MAKE_BASE=TRUE		

Host Partition A 7 -> SO-DIMM A 7

MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	30
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	30
	MAKE_BASE=TRUE	=MEM_A_DM<0>	30
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	30
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	30
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	30
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	30
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	30
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	30
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	30
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	30

Host Partition B 0 -> SO-DIMM B 0

MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	31
MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	31
	MAKE_BASE=TRUE	=MEM_B_DM<7>	31
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	31
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	31
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	31
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	31
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	31
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	31
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	31
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	31
	MAKE_BASE=TRUE		

Host Partition B 1 -> SO-DIMM B 2

MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	31
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	31
	MAKE_BASE=TRUE	=MEM_B_DM<6>	31
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	31
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	31
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	31
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	31
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	31
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	31
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	31
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	31
	MAKE_BASE=TRUE		

Host Partition B 2 -> SO-DIMM B 3

MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	31
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	31
	MAKE_BASE=TRUE	=MEM_B_DM<5>	31
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	31
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	31
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	31
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	31
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	31
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	31
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	31
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	31
	MAKE_BASE=TRUE		

Host Partition B 3 -> SO-DIMM B 1

MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	31
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	31
	MAKE_BASE=TRUE	=MEM_B_DM<4>	31
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	31
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	31
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	31
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	31
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	31
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	31
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	31
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	31
	MAKE_BASE=TRUE		

Host Partition B 4 -> SO-DIMM B 4

MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	31
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	31
	MAKE_BASE=TRUE	=MEM_B_DM<3>	31
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	31
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	31
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	31
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	31
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	31
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	31
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	31
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	31
	MAKE_BASE=TRUE		

Host Partition B 5 -> SO-DIMM B 5

MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	31
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	31
	MAKE_BASE=TRUE	=MEM_B_DM<2>	31
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	31
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	31
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	31
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	31
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	31
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	31
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	31
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	31
	MAKE_BASE=TRUE		

Host Partition B 6 -> SO-DIMM B 6

MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	31
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	31
	MAKE_BASE=TRUE	=MEM_B_DM<1>	31
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	31
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	31
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	31
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	31
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	31
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	31
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	31
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	31
	MAKE_BASE=TRUE		

Host Partition B 7 -> SO-DIMM B 7

MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	31
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	31
	MAKE_BASE=TRUE	=MEM_B_DM<0>	31
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	31
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	31
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	31
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	31
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	31
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	31
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	31
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	31

SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2010

PAGE TITLE
SO-DIMM Pinswaps

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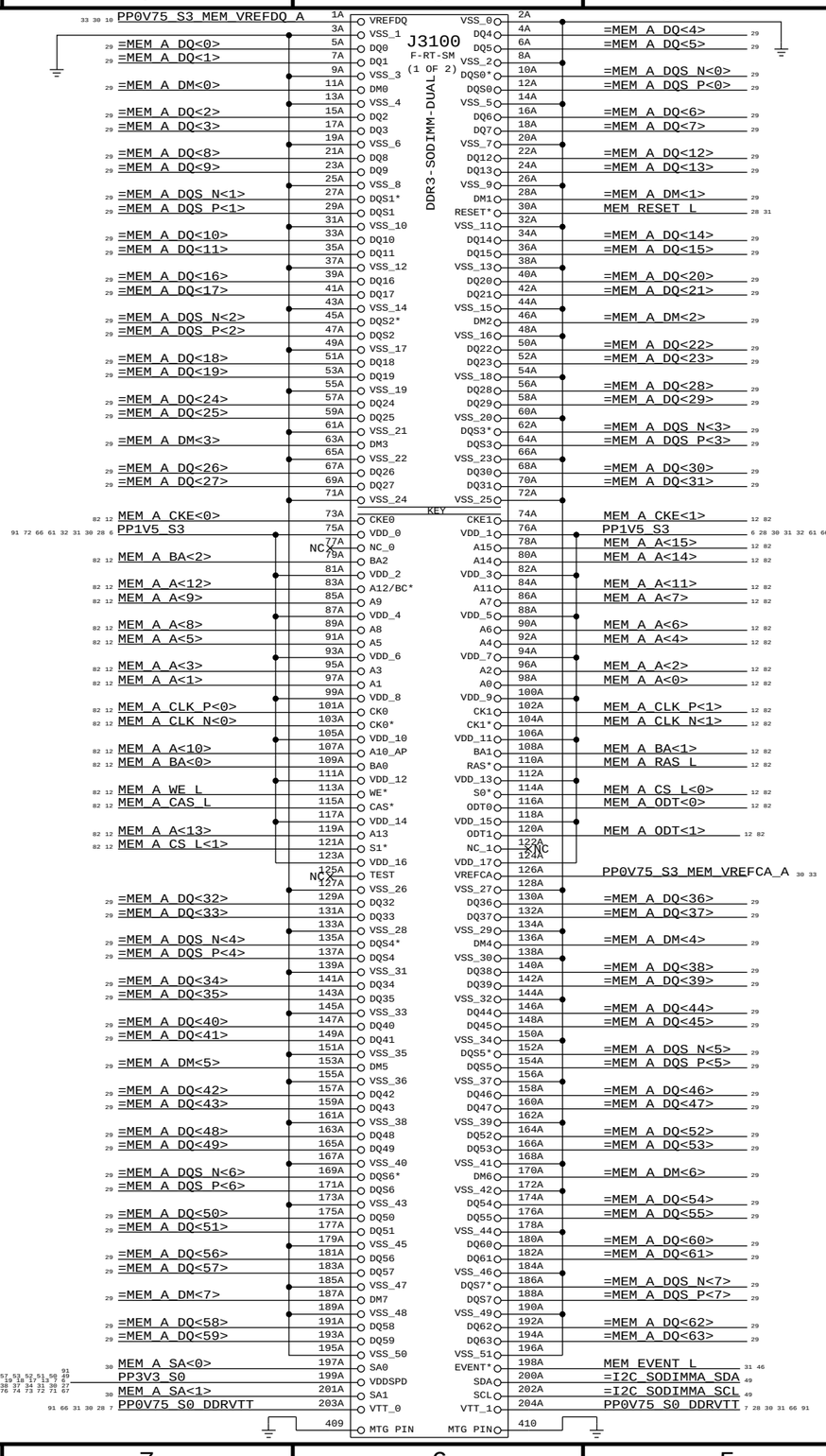
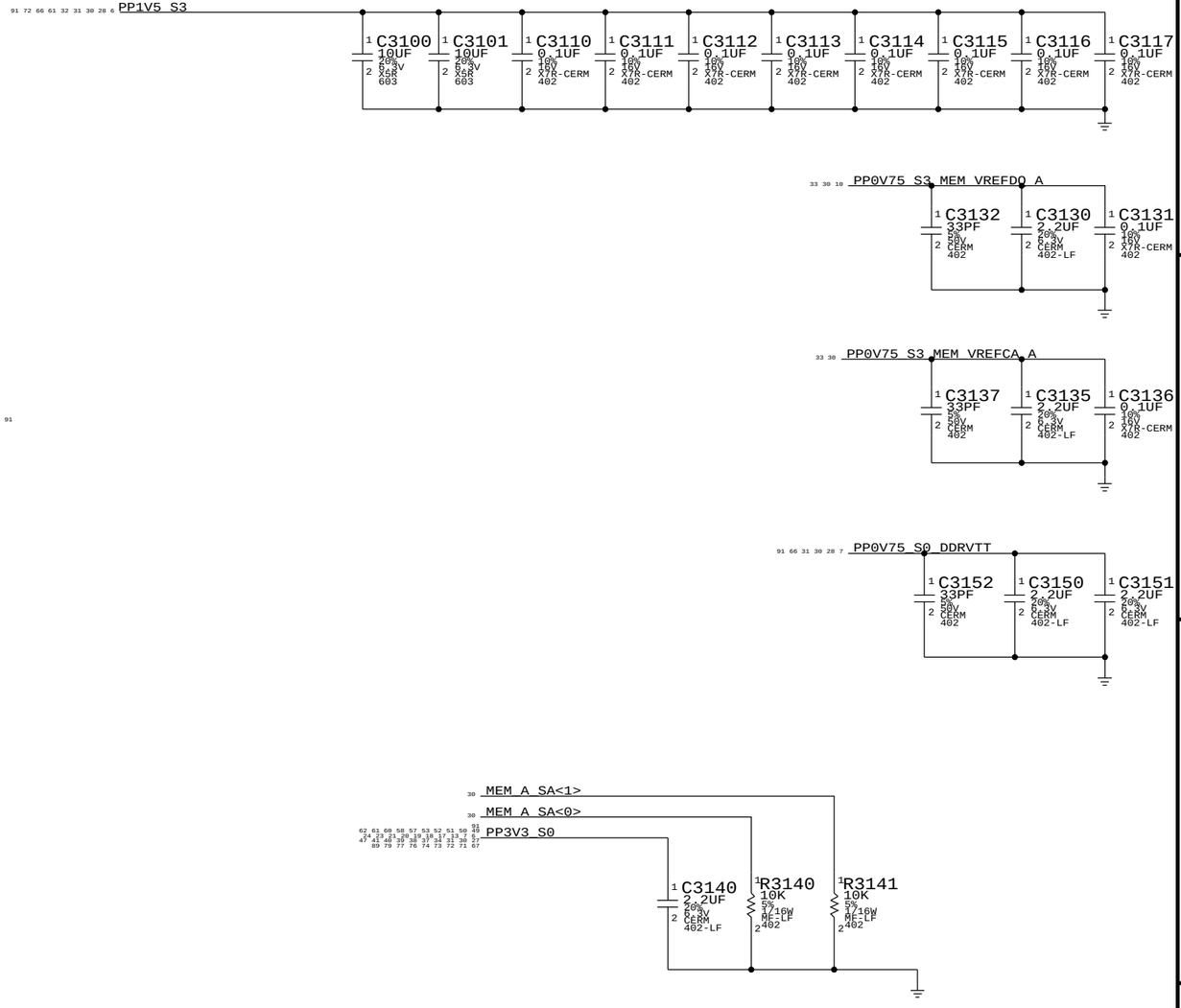


DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



516S0694

SPD ADDR=0xA0(WR)/0xA1(RD)

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

DDR3 SO-DIMM Connector A-1

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

REVISION 9.0.0

BRANCH

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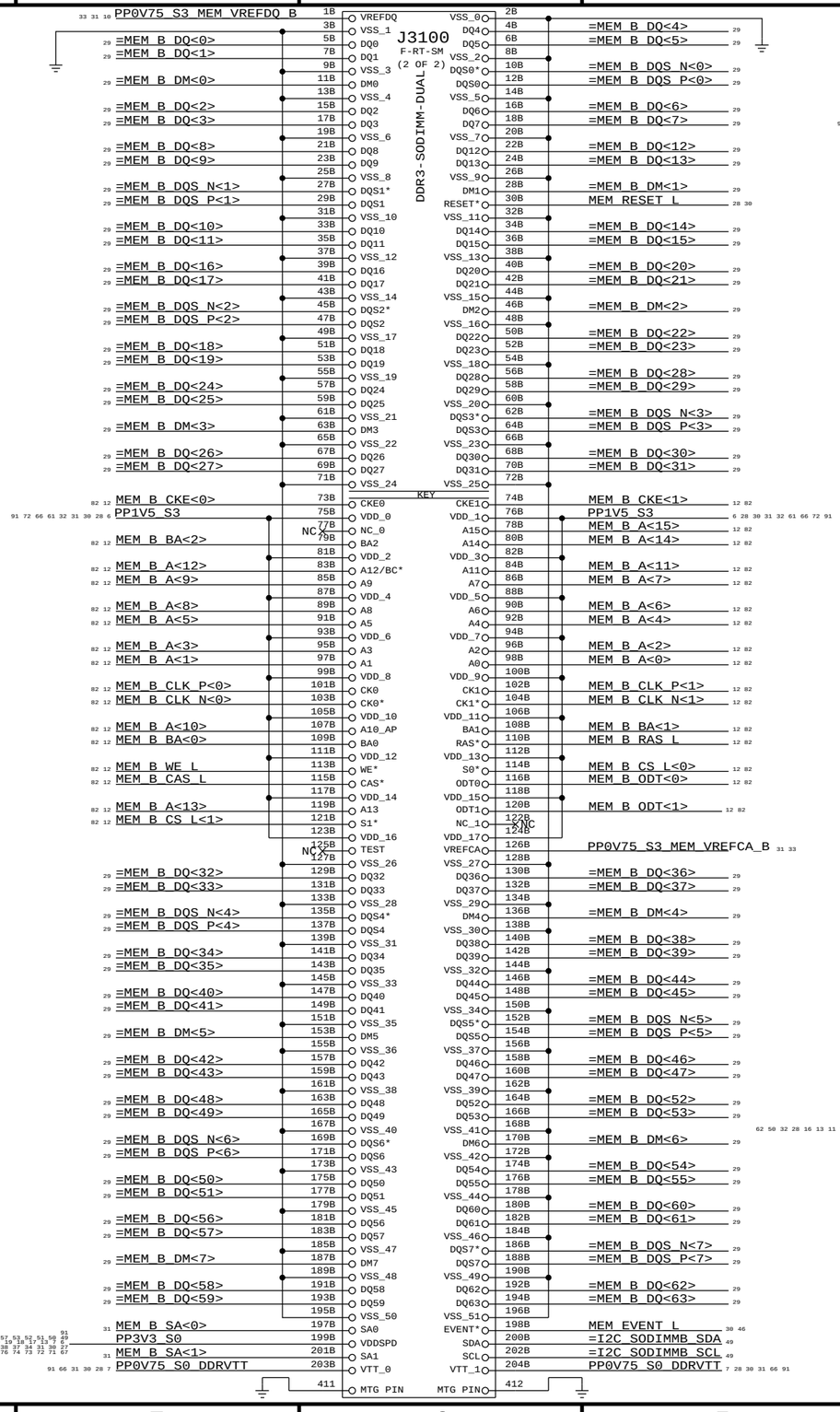
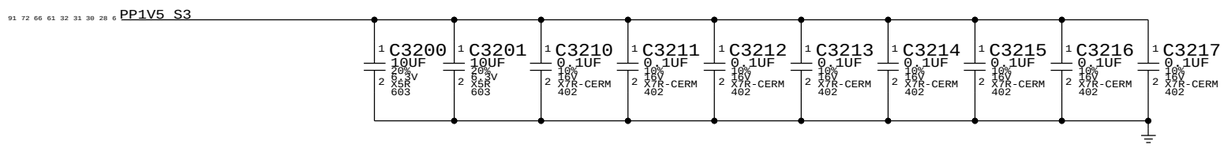
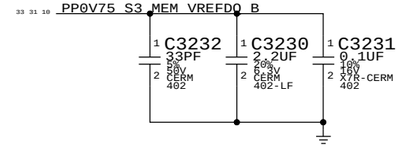
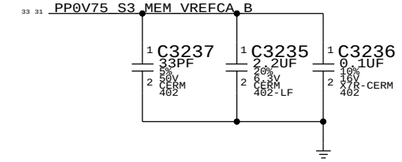
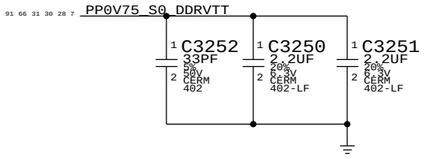


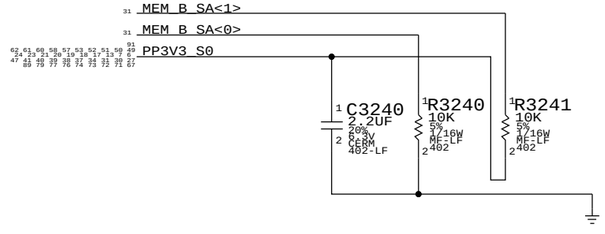
DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



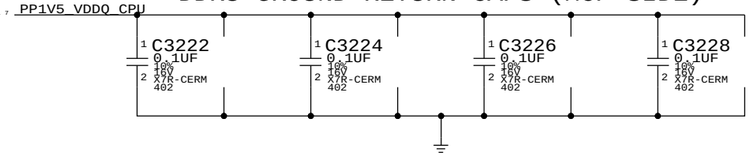








DDR3 GROUND RETURN CAPS (MCP SIDE)



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=12/01/2010

PAGE TITLE
DDR3 SO-DIMM Connector A-2

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D
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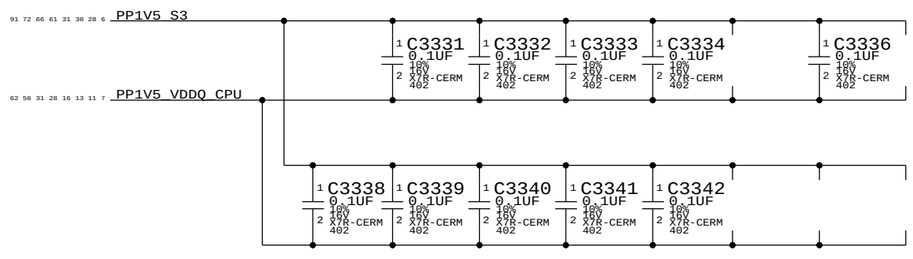

STICHING CAPS.

PLACE ACROSS PLANE SPLIT BETWEEN THESE RAIL
WHERE THE MEMORY ROUTES ARE.
EXTRAS CAN BE DELETED.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
DDR3 Support

Apple Inc.

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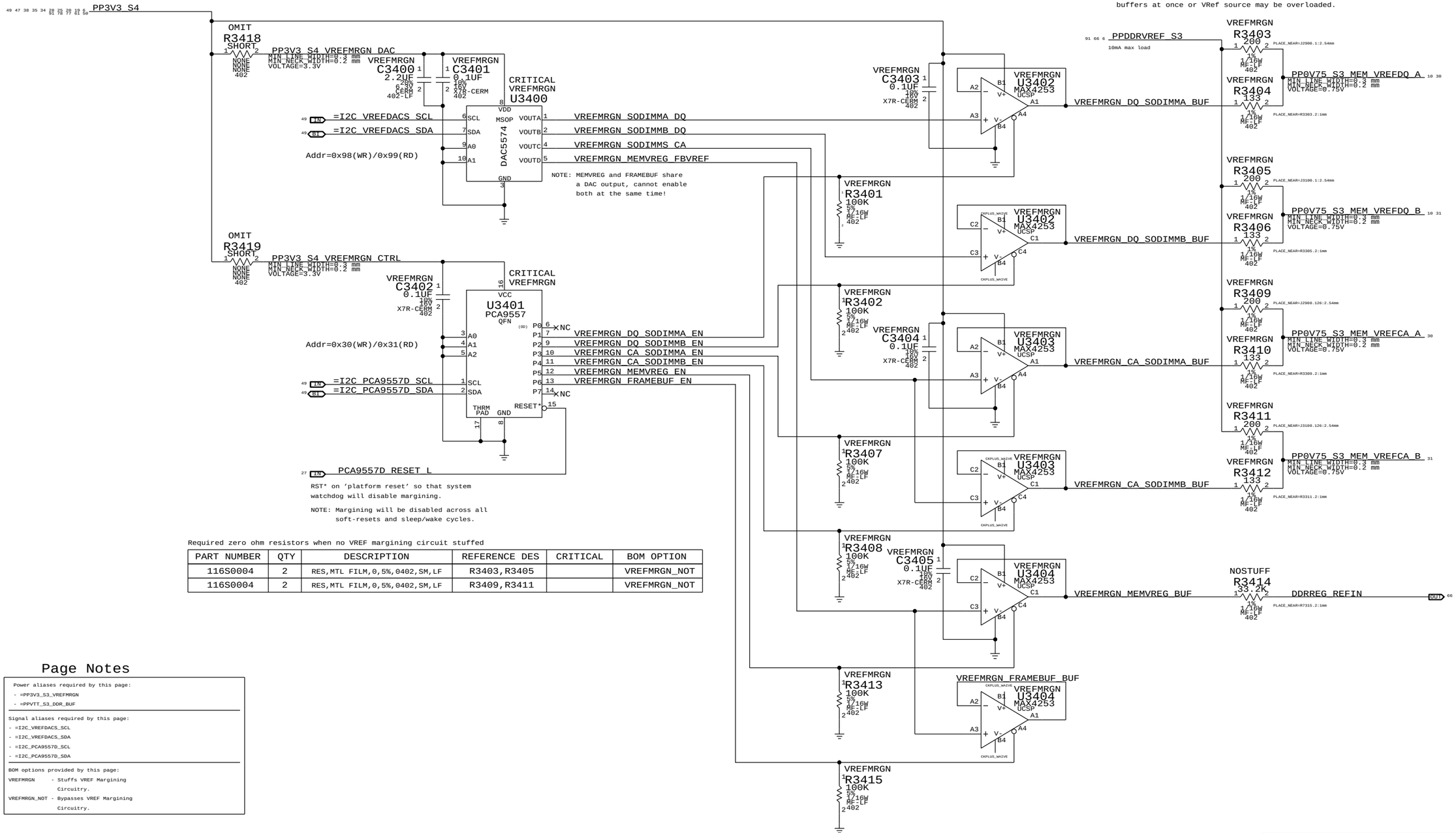

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- VREFMRGN - Stuffs VREF Margining Circuitry.
- VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2011

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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Caesar IV Support

EMI CAPS

PLACE NEXT TO J3500

NOSTUFF C3511 10PF 1 2 SDCONN_CMD_R 34 85
NOSTUFF C3512 10PF 1 2 SDCONN_DATA_R<0> 34 85
NOSTUFF C3513 10PF 1 2 SDCONN_DATA_R<1> 34 85
NOSTUFF C3514 10PF 1 2 SDCONN_DATA_R<2> 34 85
NOSTUFF C3515 10PF 1 2 SDCONN_DATA_R<3> 34 85
NOSTUFF C3516 10PF 1 2 SDCONN_DATA_R<4> 34 85
NOSTUFF C3517 10PF 1 2 SDCONN_DATA_R<5> 34 85
NOSTUFF C3518 10PF 1 2 SDCONN_DATA_R<6> 34 85
NOSTUFF C3519 10PF 1 2 SDCONN_DATA_R<7> 34 85
NOSTUFF C3520 10PF 1 2 SDCONN_WP 34 37 91
NOSTUFF C3521 10PF 1 2 SDCONN_DETECT 34 91

(All: 5% 50V CERM 402)

RESISTER ON FERRITE PADS!!

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	3	RES,ZERO OHM,0402	L3540,L3541,L3550	
152S1491	1	IND,WW,43NH,5%,100MA,0402	L3551	

TPS2065-1 HAS ACTIVE LOAD DISCHARGE SO R3505 IS NOSTUFF.

1.0A LIMIT

U3500 TPS2065-1 (DGN)
IN0 2, IN1 3, EN 4, GND 5, OC* 5, OUT0 6, OUT1 7, OUT2 8, THRM PAD 9
CRITICAL

67 62 61 60 59 57 53 52 51 50 24 23 21 20 19 18 17 13 7 6 49 47 41 40 39 38 37 31 30 27 91 89 79 77 76 74 73 72 71
PP3V3_S0 37 ENET_CR_PWREN

C3501 10UF 20% 6.3V X5R 603
C3500 0.1UF 10% 10V X7R-CERM 402
R3502 10K 5% 1/16W MF-LF 402
C3507 10UF 20% 6.3V X5R 603
C3505 0.1UF 10% 10V X7R-CERM 402
R3505 39.2K 1% 1/16W MF-LF 402 NOSTUFF

PU_SDCONN_OC_L

MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_SW_SD_PWR 91

RESISTER ON FERRITE PADS!!
PLACE AT SOURCE.

91 85 37 IN SDCONN_CLK — L3540 10NH-300MA 0402 — SDCONNF_CLK_FF — L3541 10NH-300MA 0402 — SDCONNF_CLK
C3542 NOSTUFF 15PF 5% 50V CERM 402
C3541 NOSTUFF 15PF 5% 50V CERM 402

RESISTER ON FERRITE PADS!!
PLACE AT CONNECTOR.

SDCONNF_CLK — L3550 13NH-430MA 0402 — SDCONN_CLK_FF — L3551 68NH-140MA 0402
C3551 NOSTUFF 15PF 5% 50V CERM 402
C3550 NOSTUFF 22PF 5% 50V CERM 402

SDCONN_CMD	R3555 10	SDCONN_CLK_R	85
SDCONN_DATA<0>	R3560 10	SDCONN_CMD_R	85 34
SDCONN_DATA<1>	R3561 10	SDCONN_DATA_R<0>	85 34
SDCONN_DATA<2>	R3562 10	SDCONN_DATA_R<1>	85 34
SDCONN_DATA<3>	R3563 10	SDCONN_DATA_R<2>	85 34
SDCONN_DATA<4>	R3564 10	SDCONN_DATA_R<3>	85 34
SDCONN_DATA<5>	R3565 10	SDCONN_DATA_R<4>	85 34
SDCONN_DATA<6>	R3566 10	SDCONN_DATA_R<5>	85 34
SDCONN_DATA<7>	R3567 10	SDCONN_DATA_R<6>	85 34
		SDCONN_DATA_R<7>	85 34
		SDCONN_DETECT	91 34 OUT
		SDCONN_WP	91 37 34 OUT

(All: 5% 1/16W MF-LF 402; 91 85 37 BI)

CRITICAL
J3500 SD-CARD-K40-K41 F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW (NC SWITCH)
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

516-0230

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

47 38 35 34 33 28 25 20 19 6 91 78 77 61 50 49 PP3V3_S4

C3530 1UF 10% 10V X5R 402-1

U3530 SLG4AP014V TDFN
VDD 1, LOW_PWR 2, RST_IN* 3, DET_IN (IPU) 6, GND 5, RST_OUT* 4, DET_CHNGD* 8, DET_OUT 7, THRM PAD 9
RST LOGIC, DLY, XOR, (OD)

37 28 IN ENET_LOW_PWR
85 27 IN ENET_RESET_L -> FROM PCH GPIO
R3511 0 5% 1/16W MF-LF 402
NOSTUFF R3510 10K 5% 1/10W MF-LF 402
SLG_ENET_RESET_L
SDCONN_DETECT_L
47 38 35 34 33 28 25 20 19 6 91 78 77 61 50 49 PP3V3_S4
R3530 100K 5% 1/10W MF-LF 402
Q3530 SSM3K15FV SOD-VESM-HF (D 3, G 1, S 2)
91 34 SDCONN_DETECT FROM SD CONN ->

SLG_ENET_RESET_R_L
R3514 0 5% 1/16W MF-LF 402
CIV_ENET_RESET_L OUT 37
NOSTUFF R3531 0 5% 1/16W MF-LF 402
SDCONN_STATE_CHANGE OUT 19 24 -> TO PCH GPIO
SDCONN_STATE_CHANGE_S1R
ENET_CR_DETECT_L OUT 37 -> TO ENET CHIP

*** Need to confirm with SW whether LATCH is required.
(SDCONN_STATE_RST_L will be required with LATCH)

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regradless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#

NOSTUFF R3512 0 5% 1/16W MF-LF 402

C3535 1UF 10% 10V X5R 402-1

U3535 SLG4AP014V TDFN
VDD 1, LOW_PWR 2, RST_IN* 3, DET_IN (IPU) 6, GND 5, RST_OUT* 4 NC, DET_CHNGD* 8, DET_OUT 7 NC, THRM PAD 9
RST LOGIC, DLY, XOR, (OD)

SDCONN_STATE_CHANGE_S2R
R3535 0 5% 1/16W MF-LF 402

WE WANT SDCONN_STATE_CHANGE TO WORK THE SAME IN S0 AS IN S3/4.
COPY CIRCUIT BUT TIE THE RST_IN* LOW.
WE CAN SWITCH BACK TO SINGLE PART WHEN THE PART IS CHANGED.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=12/03/2010

PAGE TITLE: SD CARD READER

Apple Inc.

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AIRPORT

PP3V3_WLAN 35 47 91

R3601 10K 5% 1/16W MF-LF 402

WHERE SHOULD THIS GO?

WLAN_THROTTLE_L 91

PCIE_WAKE_L 91 77 38 18 OUT

CRITICAL
J3601 500913-0302 F-ST-SM

RESET#
WAKE#
CLKREQ#

NC
NC

FLEX SIDE = 516S0573

516S0582

PCIE_AP_D2R_P OUT 17 84 91
PCIE_AP_D2R_N OUT 17 84 91

CRITICAL
L3601 90-OHM-100MA DLP11S

PCIE_CLK100M_AP_P IN 17 84
PCIE_CLK100M_AP_N IN 17 84

PLACE_NEAR=J3601.11:2.54 MM
PLACE_NEAR=J3601.15:5 MM

PCIE_CLK100M_AP_CONN_P 91 84
PCIE_CLK100M_AP_CONN_N 91 84

C3631 0.1UF 10% 16V X7R-CERM 402

C3630 0.1UF 10% 16V X7R-CERM 402

PCIE_AP_R2D_C_P IN 17 84
PCIE_AP_R2D_C_N IN 17 84

PLACE_NEAR=J3601.17:5 MM

PCIE_AP_R2D_P 91 84
PCIE_AP_R2D_N 91 84

USB_BT_CONN_P 91 83
USB_BT_CONN_N 91 83

PP3V3_S4_BT_F 6 19 20 25 28 33 34 35 38 47 49 50 61 77 78 91
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3632 0.01UF 10% 50V X7R 402

C3633 1UF 10% 10V X5R 402-1

CRITICAL
L3603 90-OHM DLP0NS

BLUETOOTH

USB_BT_P BI 25 83
USB_BT_N BI 25 83

PLACE_NEAR=J3601.27:2.54 MM

L3606 FERR-120-OHM-1.5A 0402

PP3V3_S4 6 19 20 25 28 33 34 35 38 47 49 50 61 77 78 91

PLACE_NEAR=J3601.27:2.54 MM

L3604 FERR-120-OHM-3A 0603

PP3V3_WLAN 91 47 35

PLACE_NEAR=J3601.27:2.54 MM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3622 0.01UF 10% 50V X7R 402

C3623 0.01UF 10% 50V X7R 402

C3624 1UF 10% 10V X5R 402-1

C3621 0.1UF 10% 16V X7R-CERM 402

C3620 10UF 10% 6.3V X5R-CERM 0805

ANTENNA CABLE CLIPS

CL3601 CLIP-ANT CLIP-SM-K40
CL3602 CLIP-ANT CLIP-SM-K40
CL3603 CLIP-ANT CLIP-SM-K40
CL3604 CLIP-ANT CLIP-SM-K40
CL3606 CLIP-ANT CLIP-SM-K40
CL3608 CLIP-ANT CLIP-SM-K40
CL3614 CLIP-ANT CLIP-SM-K40
CL3615 CLIP-ANT CLIP-SM-K40
CL3616 CLIP-ANT CLIP-SM-K40
CL3617 CLIP-ANT CLIP-SM-K40
CL3618 CLIP-ANT CLIP-SM-K40

806-0444

3.3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 mOhm @2.5V
LOADING	1.1 A (EDP)

PP3V3_WLAN_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL
Q3650 TPCP8102 23V1K-SM

C3650 0.1UF 10% 16V X7R-CERM 402

C3651 0.033UF 10% 16V X5R 402

R3650 33.2K 1% 1/16W MF-LF 402

P3V3WLAN_SS

PP3V3_S4 6 19 20 25 28 33 34 35 38 47 49 50 61 77 78 91
1.1 A PEAK
606 mA nominal max

R3651 10K 5% 1/16W MF-LF 402

PM_WLAN_EN_L IN 62

Supervisor & CLKREQ# Isolation

PP3V3_S4 6 19 20 25 28 33 34 35 38 47 49 50 61 77 78 91

C3640 0.1UF 10% 16V X7R-CERM 402

R3640 100K 5% 1/16W MF-LF 402

WF: Need pull-up?

R3653 232K 1% 1/16W MF-LF 402

R3654 100K 1% 1/16W MF-LF 402

CRITICAL
U3640 SLG4AP016V TDFN

P3V3WLAN_VMON
AP_RESET_CONN_L 91
AP_CLKREQ_L 91

SENSE 0.7V
RESET*
DLY
MR*
EN
OUT (OD)
IN
THRM PAD
GND

AP_RESET_L IN 27
AP_PWR_EN IN 19 24 62
AP_CLKREQ_L OUT 17

STANDOFFS FOR X28 CARD

SDF3600 STDOFF-3.85OD4.5H-1.3-TH 860-1277
SDF3601 STDOFF-3.85OD4.5H-1.3-TH 860-1277
SDF3602 STDOFF-3.85OD4.5H-1.3-TH 860-1277

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
WIRELESS,BT CONNECTOR

Apple Inc.

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PLACE ONE CAP NEAR EACH PINS 3 AND 4 OF T3801 AND T3802

ENET_CONN_CTAP

C3800 0.1UF 10% 16V X7R-CERM 402
C3801 0.1UF 10% 16V X7R-CERM 402
C3802 0.1UF 10% 16V X7R-CERM 402
C3803 0.1UF 10% 16V X7R-CERM 402

ETHERNET CONNECTOR

CRITICAL
T3801
SM
TLA-6T213HF

CRITICAL
T3802
SM
TLA-6T213HF

TX → RX

ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<3>
ENET_MDI_P<3>

ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_P<2>
ENET_CENTER_TAP<1>
ENET_CENTER_TAP<3>
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<0>
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_P<3>

CRITICAL
J3800
RJ45-J40
F-R-TH

ENET_MDI
TRAN_P0
TRAN_N0
TRAN_P1 *
TRAN_P2
TRAN_N2
TRAN_N1 *
TRAN_P3
TRAN_N3
SHIELD PINS

*SPLIT PAIR

514-0785

TRANSFORMERS SHOULD BE MIRRORED ON OPPOSITE SIDES OF BOARD.

D3800
RCLAMP0524P
SLP2510P8
NOSTUFF
CRITICAL

D3801
RCLAMP0524P
SLP2510P8
NOSTUFF
CRITICAL

D3800.1: PLACE_NEAR=T3800.2:4 MM
D3800.5: PLACE_NEAR=T3800.6:4 MM
D3801.1: PLACE_NEAR=T3800.8:4 MM
D3801.5: PLACE_NEAR=T3800.12:4 MM

R3800 75 1% 1/10W MF-LF 402
R3801 75 1% 1/10W MF-LF 402
R3802 75 1% 1/10W MF-LF 402
R3803 75 1% 1/10W MF-LF 402

ENET_CMODE_REF

CRITICAL
C3810 1000PF 10% 2KV CERM 1206

REQUIRES 1200V ISOLATION!

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
IF ENABLED: SR_VDD/SR_VDDP CONNECT TO PP3V3_ENET (ADD BYPASSING), LX CONNECTS TO INDUCTOR.
SPECIAL STAR ROUTING NEEDED ON THESE PINS. DECOUPLING ON PG 40.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

SEE CAPS ON NEXT PAGE FOR THESE PINS.

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

ENET_SR_LX
ENET_SR_VFB

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 16V X5R-CERM 0805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
MAKE_BASE=TRUE
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

PP3V3_S0
R3942 1K 5% 1/16W MF-LF 402 (Current Limiting Resistor)

C3950 0.1UF 10% 16V X7R-CERM 402
PCIE_ENET_D2R_N
C3951 0.1UF 10% 16V X7R-CERM 402
PCIE_ENET_D2R_P
C3955 0.1UF 10% 16V X7R-CERM 402
PCIE_ENET_R2D_C_P
C3956 0.1UF 10% 16V X7R-CERM 402
PCIE_ENET_R2D_C_N
R3943 0 5% 1/16W MF-LF 402
ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
CIV_ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_R_L
ENET_LOW_PWR
ENET_ASF_SMB_CLK
ENET_ASF_SMB_DATA
BCM57765_SCLK
BCM57765_MISO
BCM57765_MOSI
BCM57765_CS_L
TP_BCM57765_SPD100LED_L
TP_BCM57765_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM57765_RDAC

VMAIN_PRSNT (IPO)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
WAKE* (OD)
LOW_PWR (IPD)
SMB_CLK
SMB_DATA (IPD)
SCLK_SPD1000LED*
SI/EEDATA
SO_LINKLED*
CS*/EECLK
SPD100LED*/SERIAL_DO (OD)
TRAFFICLED*/SERIAL_DI (OD)
XTALI
XTALO
RDAC

R3965 1.24K 1% 1/16W MF-LF 402

CRITICAL
U3900
BCM57765B0
QFN-8X8
343S0534

THRM_PAD

TRD0_P, TRD0_N, TRD1_P, TRD1_N, TRD2_P, TRD2_N, TRD3_P, TRD3_N
ENET_MDI_P<0>, ENET_MDI_N<0>, ENET_MDI_P<1>, ENET_MDI_N<1>, ENET_MDI_P<2>, ENET_MDI_N<2>, ENET_MDI_P<3>, ENET_MDI_N<3>

GPIO_0/CR_ACT_LED*
GPIO_1/LR_OUT
GPIO_2/MEDIA_SENSE
SD_DETECT
CR_CMD
CR_CLK
CR_DATA0, CR_DATA1, CR_DATA2, CR_DATA3, CR_DATA4, CR_DATA5, CR_DATA6, CR_DATA7
MS_INS*
CR_LED*/CR_BUS_PWR
CR_WP*
SR_DISABLE

ENET_ASF_GPIO_R
R3930 3.3K 5% 1/16W MF-LF 402
ENET_ASF_GPIO
ENET_MEDIA_SENSE
ENET_CR_DETECT_L
ENET_CR_CMD
R3974 33 5% 1/16W MF-LF 402 (PLACE_NEAR=U3900.26:3 MM)
SDCONN_CMD
ENET_CR_CLK
R3971 33 5% 1/16W MF-LF 402 (PLACE_NEAR=U3900.21:3 MM)
SDCONN_CLK
ENET_CR_DATA<0>, R3950 33 5% 1/16W MF-LF 402, SDCONN_DATA<0>
ENET_CR_DATA<1>, R3951 33 5% 1/16W MF-LF 402, SDCONN_DATA<1>
ENET_CR_DATA<2>, R3952 33 5% 1/16W MF-LF 402, SDCONN_DATA<2>
ENET_CR_DATA<3>, R3953 33 5% 1/16W MF-LF 402, SDCONN_DATA<3>
ENET_CR_DATA<4>, R3975 33 5% 1/16W MF-LF 402, SDCONN_DATA<4>
ENET_CR_DATA<5>, R3976 33 5% 1/16W MF-LF 402, SDCONN_DATA<5>
ENET_CR_DATA<6>, R3977 33 5% 1/16W MF-LF 402, SDCONN_DATA<6>
ENET_CR_DATA<7>, R3978 33 5% 1/16W MF-LF 402, SDCONN_DATA<7>
NC_BCM57765_CE_L_MS_INS_L (NO_TEST=TRUE)
ENET_CR_PWREN
SDCONN_WP
BDM57765_SR_DISABLE
R3980 1K 5% 1/16W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET 1.2V SR IS ENABLED IF SR_DISABLE is PULLed-DOWN.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF 10% 16V X7R-CERM 402
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
CRITICAL
VCC, SCK, CS*, WP*, RESET*, GND, SI, SO
BCM57765_SCLK
BCM57765_CS_L
BCM57765_MOSI
BCM57765_MISO
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8768
SIZE D
REVISION 9.0.0
BRANCH
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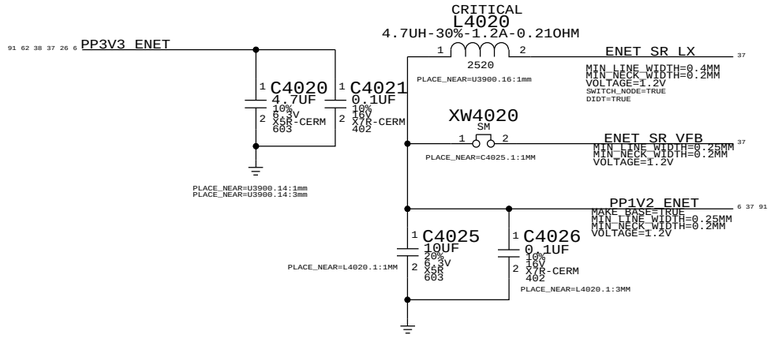
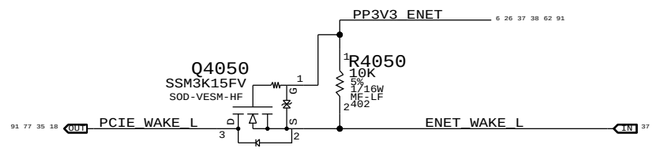
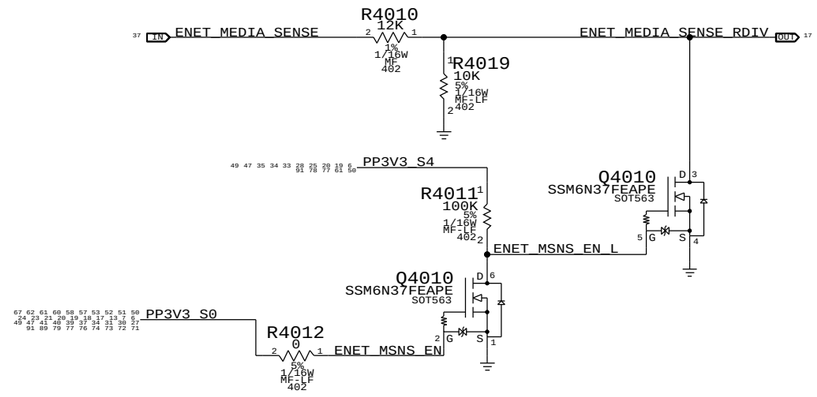
SHEET 37 OF 104

CAESAR IV 1.2V INT.VR CMPTS



Ethernet WAKE# Isolation





SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/30/2010
PAGE TITLE: ETHERNET SUPPORT	
Apple Inc.	DRAWING NUMBER: 051-8768 SIZE: D
	REVISION: 9.0.0
	BRANCH:
	PAGE: 40 OF 512
	SHEET: 38 OF 104

PP3V3_S0

C4100 C4101 C4102 C4103 C4104 C4105 1UF 10% 16V X5R 402-1

C4106 C4107 C4108 C4110 C4111 C4112 C4113 C4114 C4115 1UF 10% 16V X5R 402-1

C4117 C4118 C4119 1UF 10% 16V X5R 402-1

R4110 1 5% 1/10W MF-LF 603

R4117 1 5% 1/10W MF-LF 603

R4119 1 5% 1/10W MF-LF 603

PP3V3_FW_AVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP3V3_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP3V3_FW_PLLVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP1V5_S0

C4124 C4123 C4122 C4121 C4120 1UF 10% 16V X5R 402-1

C4128 C4127 C4126 C4125 1UF 10% 16V X5R 402-1

R4125 1 5% 1/10W MF-LF 603

R4129 1K 5% 1/16W MF-LF 402

PP1V5_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V

PU_FW_VP

C4132 C4131 C4130 1UF 10% 16V X5R 402-1

R4135 1 5% 1/10W MF-LF 603

PP1V96_S0_FW

R4190 4.7 5% 1/16W MF-LF 402

PP1V96_FW_PLLVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V

C4135 1UF 10% 16V X5R 402-1

PP1V96_FW_XTAL
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V

C4137 C4138 C4139 1UF 10% 16V X5R 402-1

C4190 0.22UF 10% 6.3V CERM-X5R 402

Y4190 98P3040MHZ SM CRITICAL
VCC OUT TRI-ST/NC GND

R4191 22 5% 1/16W MF-LF 402

CLK98M_FW_XI_R

TP_CLK98M_TS_L
FLOAT TO ENABLE, LOW TO DISABLE.

Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

FWXIO_REF_PCIE
NEED 14.53K NOMINAL.
R4141 232 1% 1/16W MF-LF 402
R4140 14.3K 1% 1/16W MF-LF 402

PLACEMENT_NOTE=PLACE C4140 CLOSE TO U1400 (MCP)
PLACEMENT_NOTE=PLACE C4141 NEXT TO C4140.

PCIE_FW_R2D_C_P C4140 0.1UF 10% 16V X7R-CERM
PCIE_FW_R2D_C_N C4141 0.1UF 10% 16V X7R-CERM
PCIE_FW_D2R_P C4145 0.1UF 10% 16V X7R-CERM
PCIE_FW_D2R_N C4146 0.1UF 10% 16V X7R-CERM

PLACEMENT_NOTE=PLACE C4145 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4146 NEXT TO C4145.

CRITICAL
U4100
XIO2211
BGA

PCI EXPRESS

FWXIO_REF0_PCIE	A13	REF0_PCIE
FWXIO_REF1_PCIE	A12	REF1_PCIE
FW_RESET_L	B13	PERST*
PCIE_FW_R2D_P	A4	RXP
PCIE_FW_R2D_N	A3	RXN
PCIE_FW_D2R_C_P	A9	TXP
PCIE_FW_D2R_C_N	A8	TXN
FW_CLKREQ_L	J12	CLKREQ*
PCIE_CLK100M_FW_P	A1	REFCLK+
PCIE_CLK100M_FW_N	B1	REFCLK-
FWXIO_REFCLK_SEL	H13	REFCLK_SEL
FWXIO_SCL	J13	SCL
FWXIO_SDA	H12	SDA
	P1	GPIO0
	N2	GPIO1
	P2	GPIO2
	N3	GPIO3
	N4	GPIO4
	P5	GPIO5
	P6	GPIO6
	N6	GPIO7
FW_PME_L	P8	OHCI_PME*
FWXIO_CYCLEOUT	N8	CYCLEOUT
TP_FWXIO_GRST_L	C13	GRST*
TP_FWXIO_JTAG_TMS	E12	RSVD0
TP_FWXIO_JTAG_TDO	F12	RSVD1
TP_FWXIO_JTAG_TDI	F13	RSVD2
FWXIO_JTAG_TCK	G12	RSVD3
	K12	RSVD4
	L12	RSVD5
	L13	RSVD6
FWXIO_SNOOP_EN	M8	RSVD7
	M11	RSVD8
	M12	RSVD9
	M13	RSVD10
	L10	RSVD11
	L11	RSVD12
	L12	RSVD13
	M13	RSVD14
	L10	RSVD15
	M11	RSVD16
FWXIO_JTAG_TRST	D12	RSVD17
FWXIO_VREG_PD33	D13	RSVD18
FWPHY_BMODE	A5	BMODE
FWPHY_TESTM	B2	TESTM
FWPHY_TESTW	A6	VREG_PD
	P13	SE
	P14	SM

(IPU)

(JTAG_TMS) (JTAG_TDO) (JTAG_TDI) (JTAG_TCK) (JTAG_TRST)

338S0765

1394B OHCI & PHY

R4150 1K 5% 1/16W MF-LF 402
R4151 220 5% 1/16W MF-LF 402
R4152 220 5% 1/16W MF-LF 402

NO STUFF
R4153 47K 5% 1/16W MF-LF 402

R4160 1K 5% 1/16W MF-LF 402

(Snoop Enable, for FireBug)

R4162 1K 5% 1/16W MF-LF 402

R4180 1K 5% 1/16W MF-LF 402

R4181 1K 5% 1/16W MF-LF 402

R4182 1K 5% 1/16W MF-LF 402

R4183 1K 5% 1/16W MF-LF 402

R4184 1K 5% 1/16W MF-LF 402

PLLVDD_3_3 PLLVDD_CORE VDD_33 (VDD_3.3_AUX) DVDD_3_3 VDDA_33 AVDD_3_3 VDD_15 VDDA_15 DVDD_CORE VDD_15_COMB VDD_33_COMB VDD_33_COM_IO

FWXIO_VDD15COMB
FWXIO_VDD33COMB
FWXIO_VDD33COMIO

PLLGND GND VSS VSSA VSSA_PCIE

Single-port:
PC[0:2] = '000'

Multiple-ports:
PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

XI	P4	CLK98M_FW_XI
RSVD19	P3	TP_FWOHCI_XO
PC0	E9	FW_PHY_PC0
PC1	E8	
PC2	A11	
DS0	N9	FW_PHY_DS0
DS1	P9	FW_PHY_DS1
LINKON_L	E1	FWOHCI_LINKON_L
LKON	D1	FWPHY_LKON_DS2
LCLK_L	G2	FWOHCI_CLK98M_LCLK
LCLK_P	H2	
PCLK_L	G1	FWPHY_CLK98M_PCLK
PCLK_P	F1	
PINT_L	D2	FWPHY_PINT
PINT_P	D3	
LPS_L	C1	FWOHCI_LPS
LPS_P	C2	
LREQ_L	F2	FWOHCI_LREQ
LREQ_P	E2	
CTL0	H1	NC
CTL1	J1	NC
D0	J2	NC
D1	K2	NC
D2	K1	NC
D3	L1	NC
D4	L2	NC
D5	L3	NC
D6	M2	NC
D7	M3	NC
R0	N1	FWPHY_R0
R1	M1	FWPHY_R1
PD	B3	
CNA	A2	TP_FWPHY_CNA
CPS	P12	FWPHY_CPS
(IPU) PHY_RESET*	B4	FWPHY_RESET_L
TPBIAS0	K13	FW_P0_TPBIAS
RSVD26	G13	NC_FW_P1_TPBIAS
RSVD23	E13	NC_FW_P2_TPBIAS
TPA0+	K14	FW_P0_TPA_P
TPA0-	L14	FW_P0_TPA_N
RSVD25	F14	NC_FW_P1_TPAP
RSVD27	G14	NC_FW_P1_TPAN
RSVD20	B14	NC_FW_P2_TPAP
RSVD21	C14	NC_FW_P2_TPAN
TPB0+	M14	FW_P0_TPB_P
TPB0-	N14	FW_P0_TPB_N
RSVD28	H14	
RSVD29	J14	
RSVD22	D14	
RSVD24	E14	

Unused Ports:

TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N

R4170 1K 5% 1/16W MF-LF 402

PP3V3_S0

R4171 470 5% 1/16W MF-LF 402

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

Strap DSx high on unused ports.

R4175 10K 5% 1/16W MF-LF 402

R4185 6.34K 1% 1/16W MF-LF 402

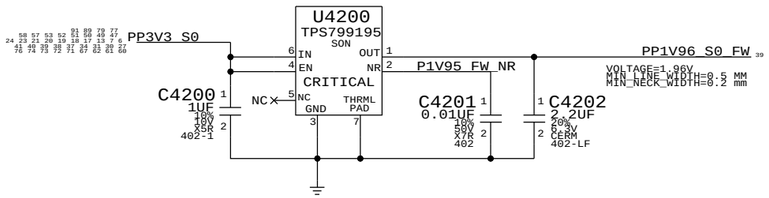
PPVP_FW_PHY_CPS

R4186 390K 5% 1/16W MF-LF 402

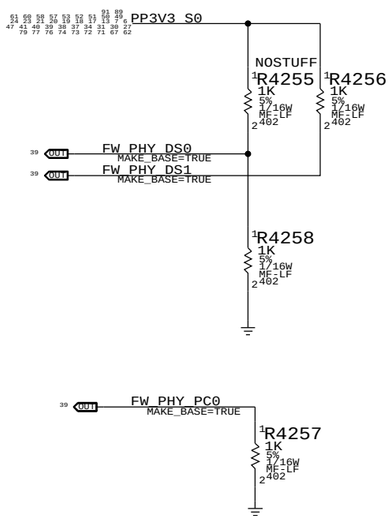
C4189 0.22UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE	FW LLC/PHY (XIO2211B)
Apple Inc.	DRAWING NUMBER 051-8768 SIZE D
	REVISION 9.0.0
	BRANCH
	PAGE 41 OF 512
	SHEET 39 OF 104

1394 PHY 1.95V SUPPLY



1394 PHY STRAPPING OPTIONS

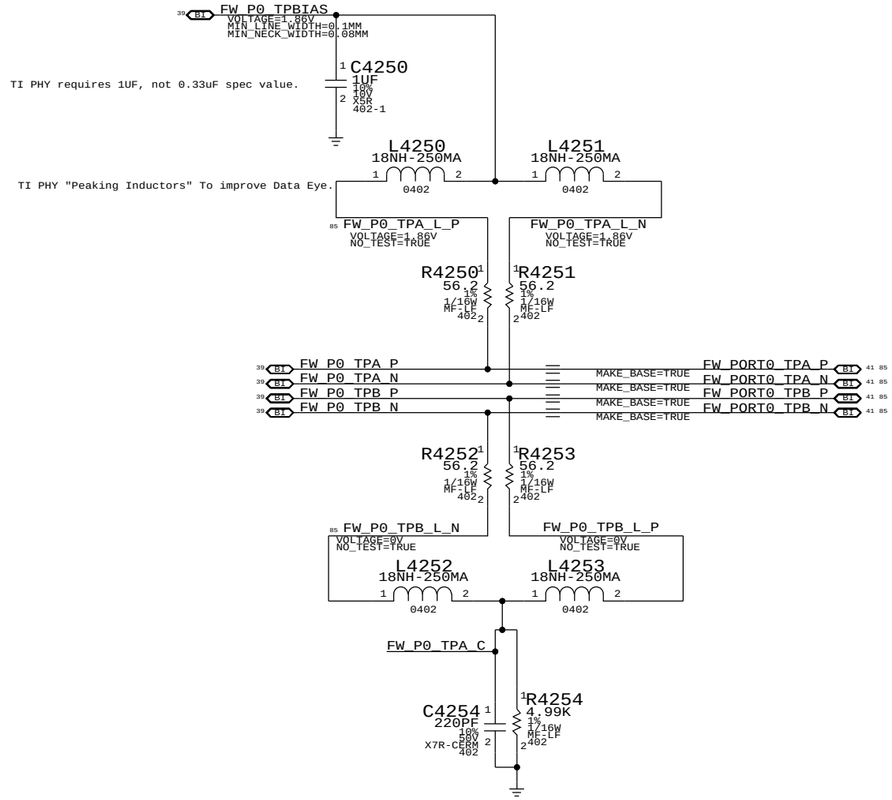


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

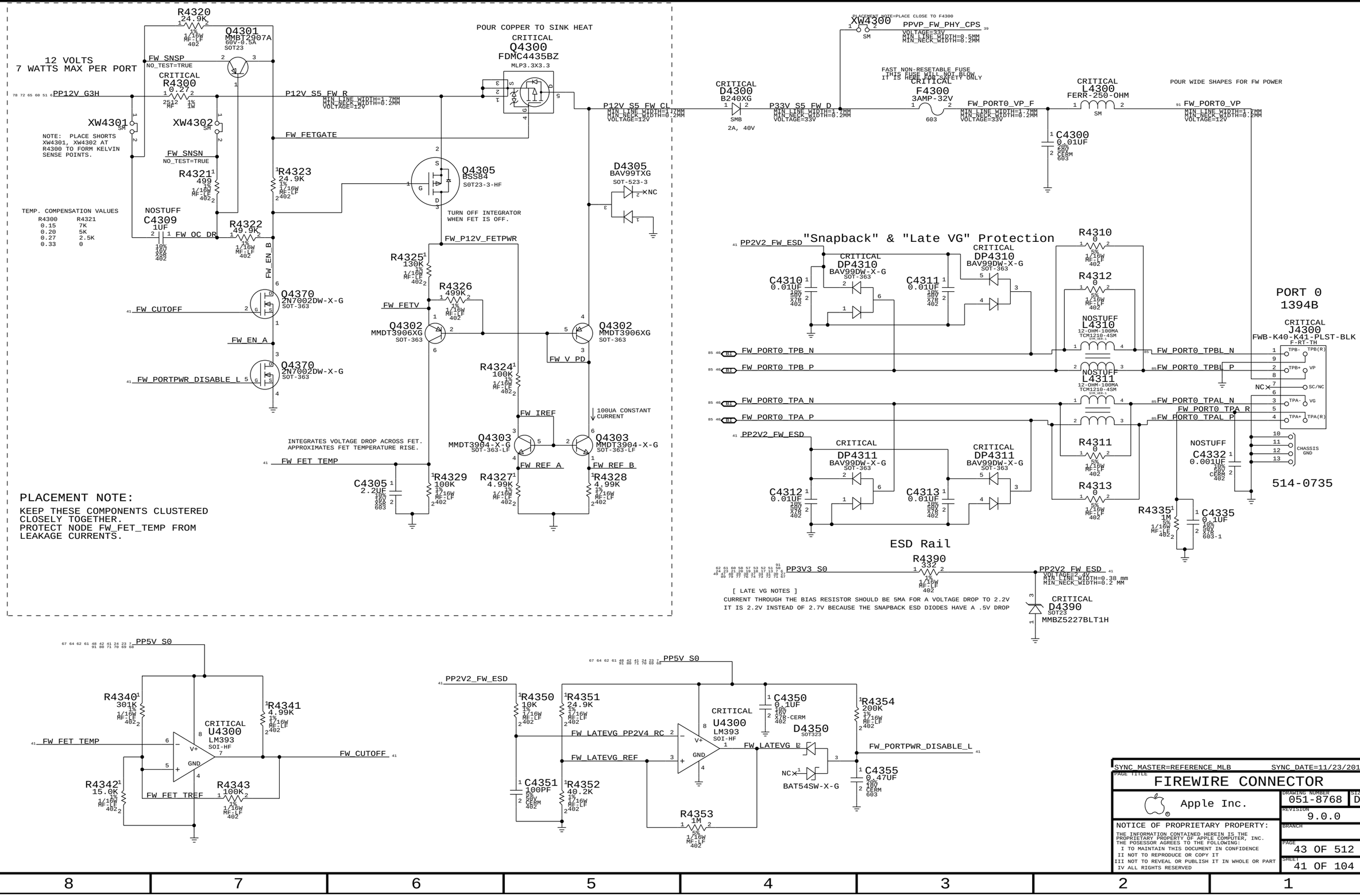
THIS IS NOW ONE PORT ONLY AND HAVE POWER CODE "000"

Termination

PLACE CLOSE TO FIREWIRE PHY (U4100)



SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE	FW: 1394B MISC
Apple Inc.	DRAWING NUMBER 051-8768 · SIZE D
	REVISION 9.0.0
	BRANCH
	PAGE 42 OF 512
	SHEET 40 OF 104



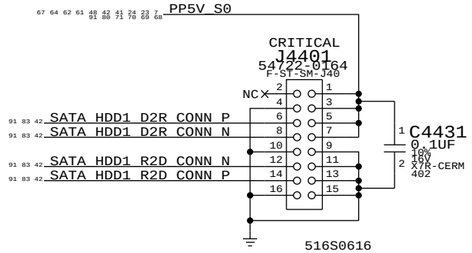
SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

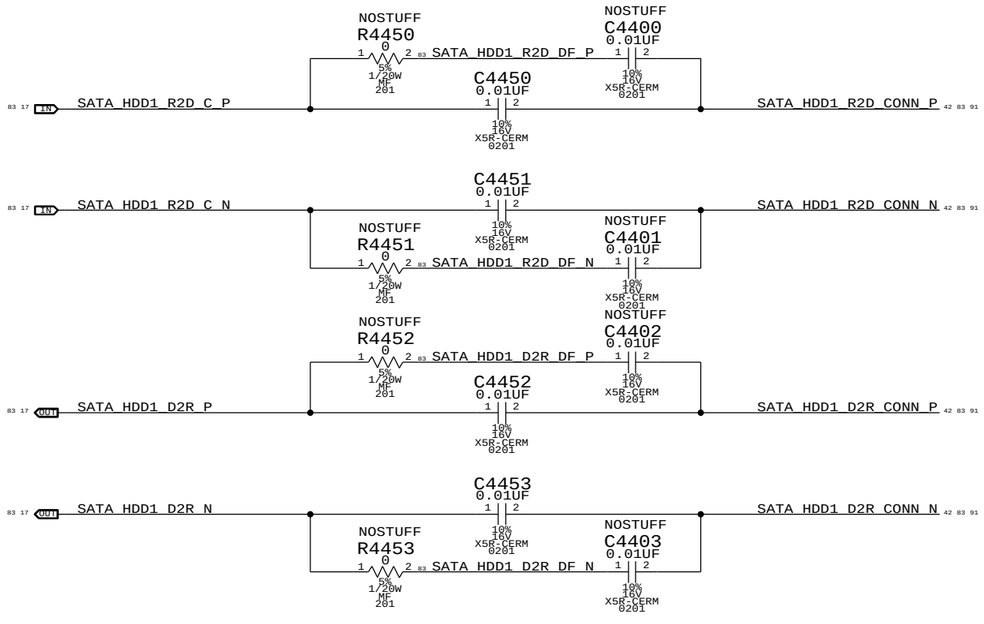
PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

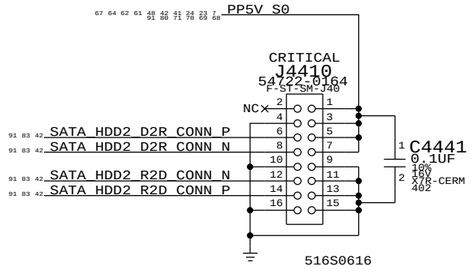
DRAWING NUMBER: 051-8768 SIZE: D
REVISION: 9.0.0
BRANCH:
PAGE: 43 OF 512
SHEET: 41 OF 104

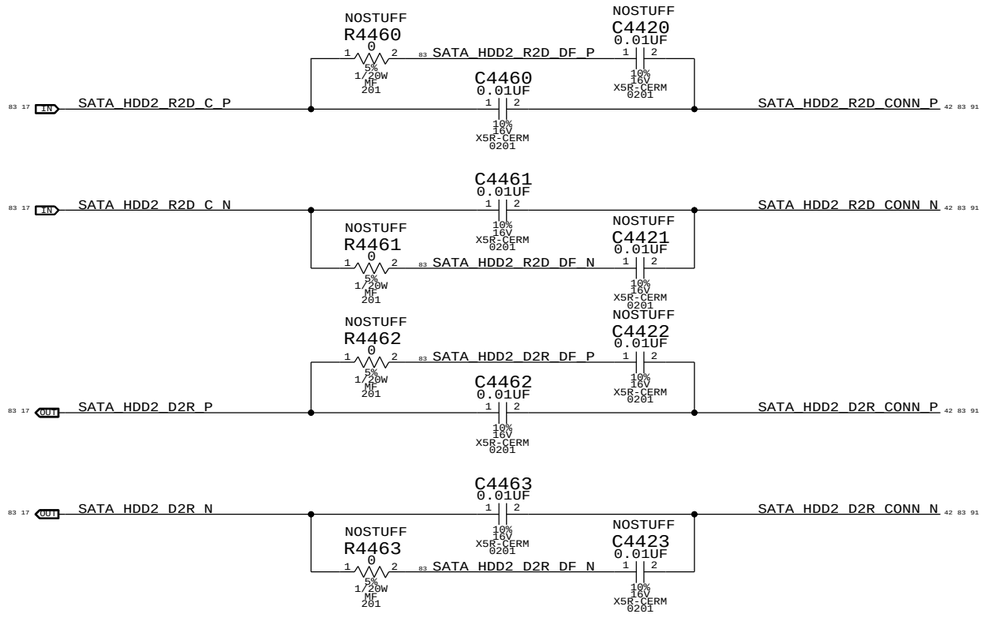
SATA CONNECTOR (HDD1)





SATA CONNECTOR (HDD2)





SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
HDD SATA CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

REVISION 9.0.0

BRANCH

PAGE 44 OF 512

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USB/SMC DEBUG MUX

PLACEMENT_NOTE=Place C4606 and C4604 close to U4601

CRITICAL U4601 TPS2561DR SON
PP5V_S4 → IN_0, IN_1
USB_EXTC_OC_L, USB_EXTB_OC_L → FAULT1*, FAULT2*
OUT1, OUT2 → PP5V_USB2_PORT3
ILIM → U4601_ILIM
R4601 23.2K 1% 1/16W MF-LF 402
C4604 0.1UF 10% 16V X7R-CERM 402
CRITICAL C4606 150UF 20% 6.3V POLY-TANT CASE-B2-SM
C4612 0.1UF 10% 16V X7R-CERM 402
C4603 0.1UF 10% 16V X7R-CERM 402

PP5V_USB2_PORT3: VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

CRITICAL L4600 FERR-220-OHM-2.5A 0603
PP5V_USB2_PORT3 → PP5V_USB2_PORT3_F

PP3V3_G3H
C4650 0.1UF 10% 16V X7R-CERM 402
R4650 10K 5% 1/16W MF-LF 402

CRITICAL U4650 PI3USB102ZLE TQFN
SMC_RX_L, SMC_TX_L, USB_EXTB_P, USB_EXTB_N
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
USB_B_MUXED_N, USB_B_MUXED_P

NOSTUFF R4651 0 5% 1/16W MF-LF 402
NOSTUFF R4652 0 5% 1/16W MF-LF 402

CRITICAL L4602 120-OHM 2012-HF
USB_PORT3_N, USB_PORT3_P

C4605 0.01UF 10% 50V X7R 402

CRITICAL J4600 USB-K40-41 F-RT-TH
VDD, D-, D+, GND, VBUS

CRITICAL D4603 RCLAMP0502B SC-75

514-0709

PORT B

USB_PWR_EN

PP5V_USB2_PORT2
VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

CRITICAL L4610 FERR-220-OHM-2.5A 0603
PP5V_USB2_PORT2 → PP5V_USB2_PORT2_F

C4615 0.01UF 10% 50V X7R 402

CRITICAL L4612 120-OHM 2012-HF
USB_EXTC_N, USB_EXTC_P
USB_PORT2_N, USB_PORT2_P

CRITICAL J4610 USB-K40-41 F-RT-TH

CRITICAL D4600 RCLAMP0502B SC-75

514-0709

PORT C

CRITICAL U4600 TPS2561DR SON
PP5V_S4 → IN_0, IN_1
USB_EXTA_OC_L, USB_EXTD_OC_L → FAULT1*, FAULT2*
OUT1, OUT2 → PP5V_USB2_PORT1
ILIM → U4600_ILIM
R4600 23.2K 1% 1/16W MF-LF 402
C4632 0.1UF 10% 16V X7R-CERM 402
C4623 0.1UF 10% 16V X7R-CERM 402
C4601 0.1UF 10% 16V X7R-CERM 402
CRITICAL C4600 150UF 20% 6.3V POLY-TANT CASE-B2-SM

PLACEMENT_NOTE=Place C4600 and C4601 close to U4600

PP5V_USB2_PORT1
VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

CRITICAL L4620 FERR-220-OHM-2.5A 0603
PP5V_USB2_PORT1 → PP5V_USB2_PORT1_F

C4625 0.01UF 10% 50V X7R 402

CRITICAL J4620 USB-K40-41 F-RT-TH

CRITICAL L4622 120-OHM 2012-HF
USB_EXTD_N, USB_EXTD_P
USB_PORT1_N, USB_PORT1_P

CRITICAL D4601 RCLAMP0502B SC-75

514-0709

PORT D

PP5V_USB2_PORT0
VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

CRITICAL L4630 FERR-220-OHM-2.5A 0603
PP5V_USB2_PORT0 → PP5V_USB2_PORT0_F

C4635 0.01UF 10% 50V X7R 402

CRITICAL J4630 USB-K40-41 F-RT-TH

CRITICAL L4632 120-OHM 2012-HF
USB_EXTA_N, USB_EXTA_P
USB_PORT0_N, USB_PORT0_P

CRITICAL D4602 RCLAMP0502B SC-75

514-0709

PORT A

RIGHT MOST LOOKING AT BACK OF SYSTEM

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/30/2016

PAGE TITLE: USB EXTERNAL CONNECTORS

Apple Inc.

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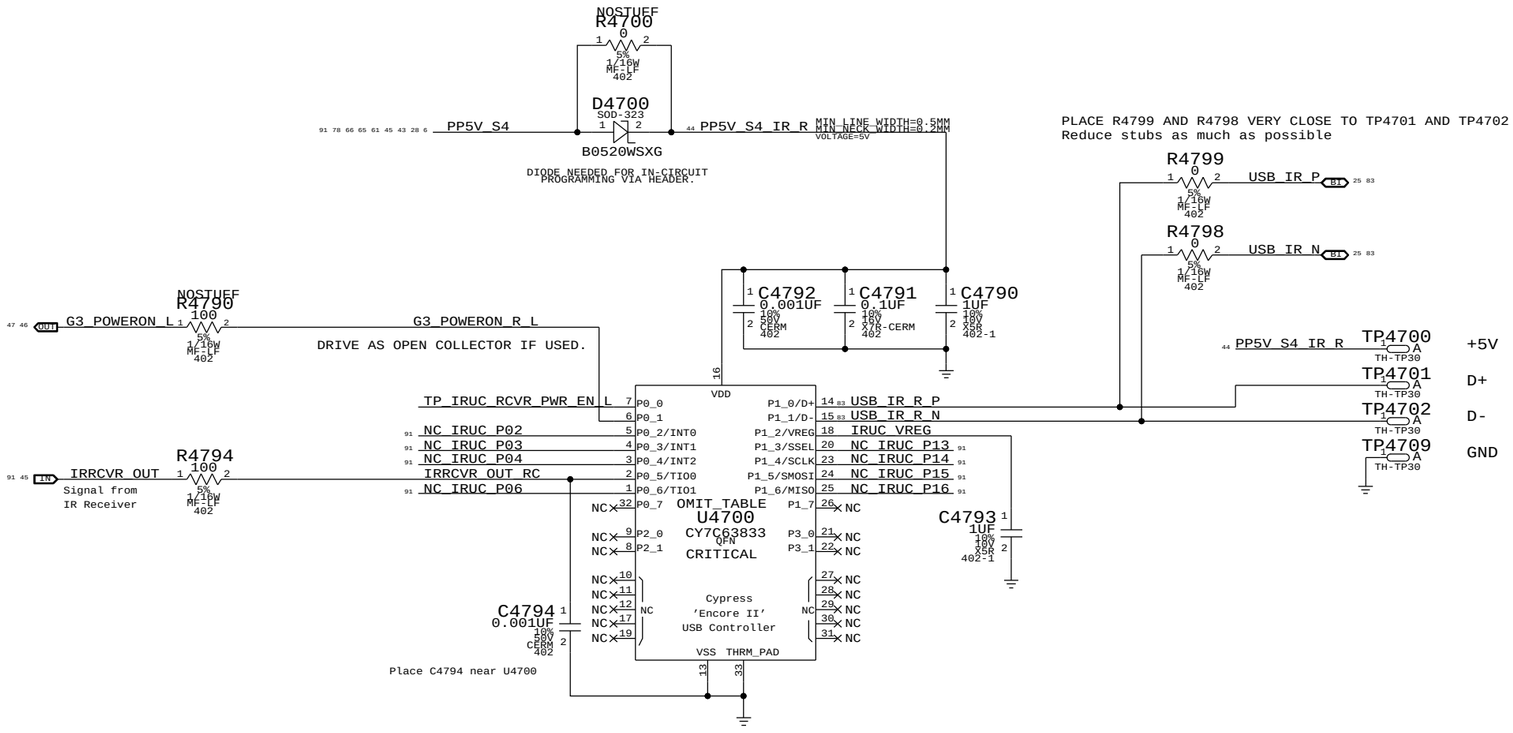
IR Controller



SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE	IR CONTROLLER
Apple Inc.	DRAWING NUMBER 051-8768 · SIZE D
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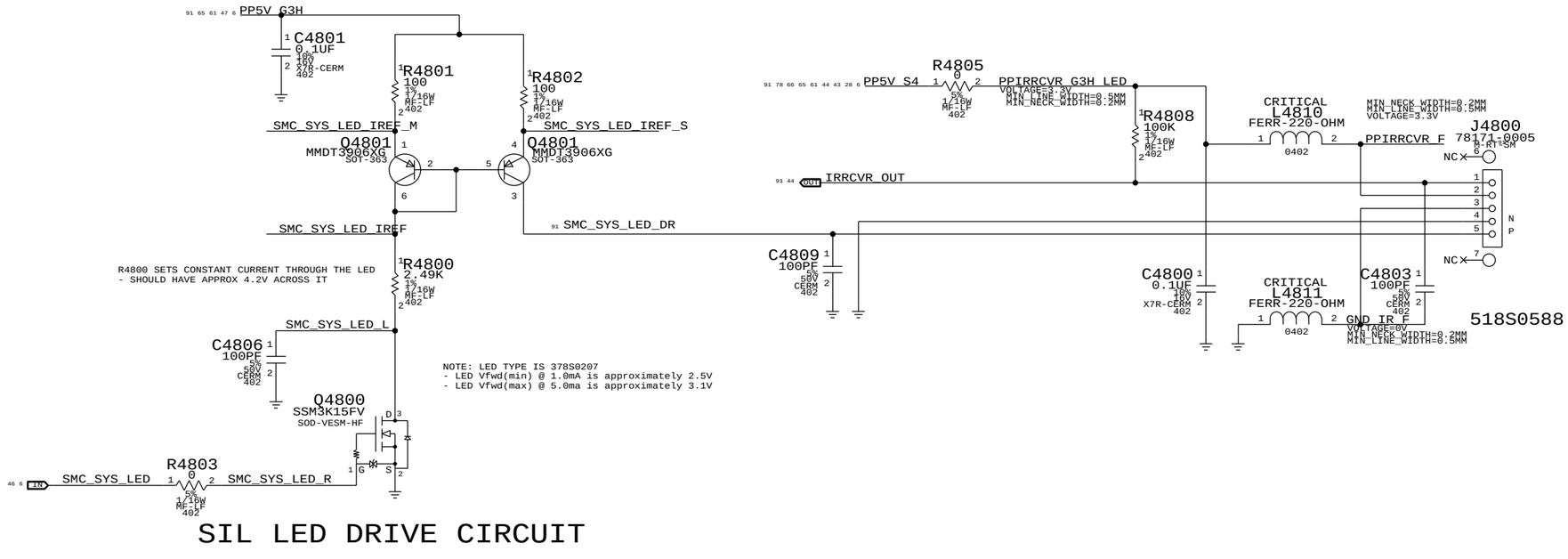
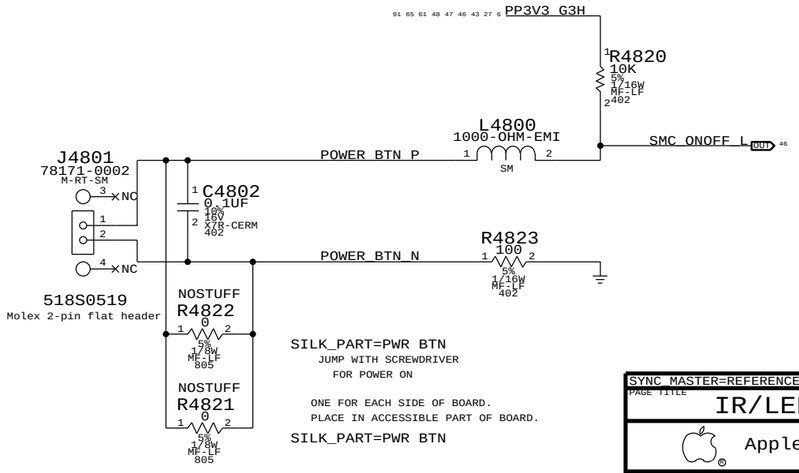
IR/LED BOARD CONNECTOR



SIL LED DRIVE CIRCUIT

Power Button Header



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: IR/LED, PWR BTTN

Apple Inc.

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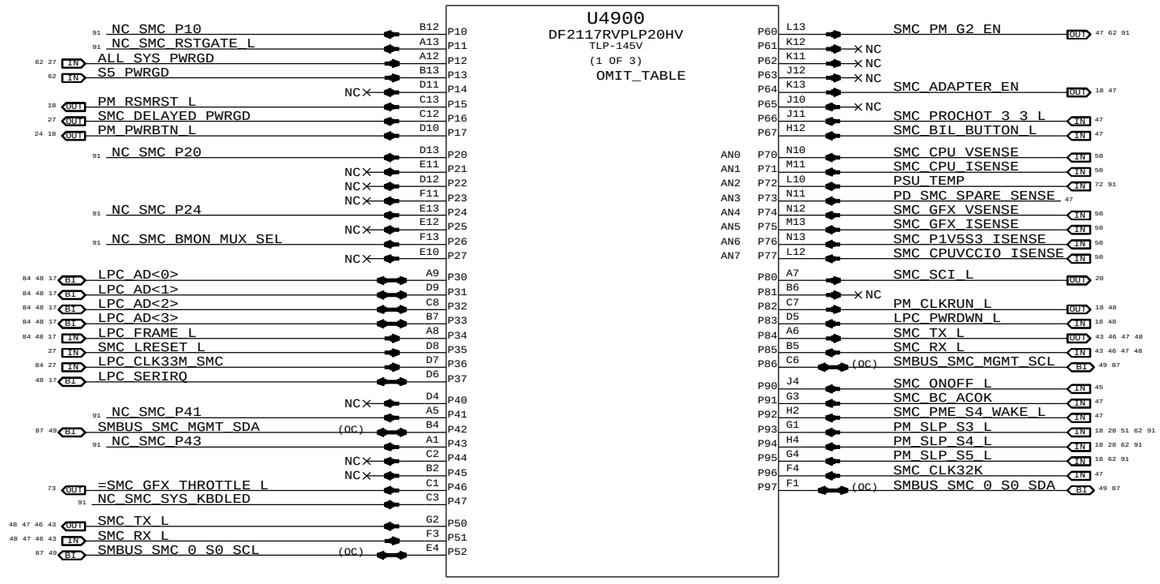
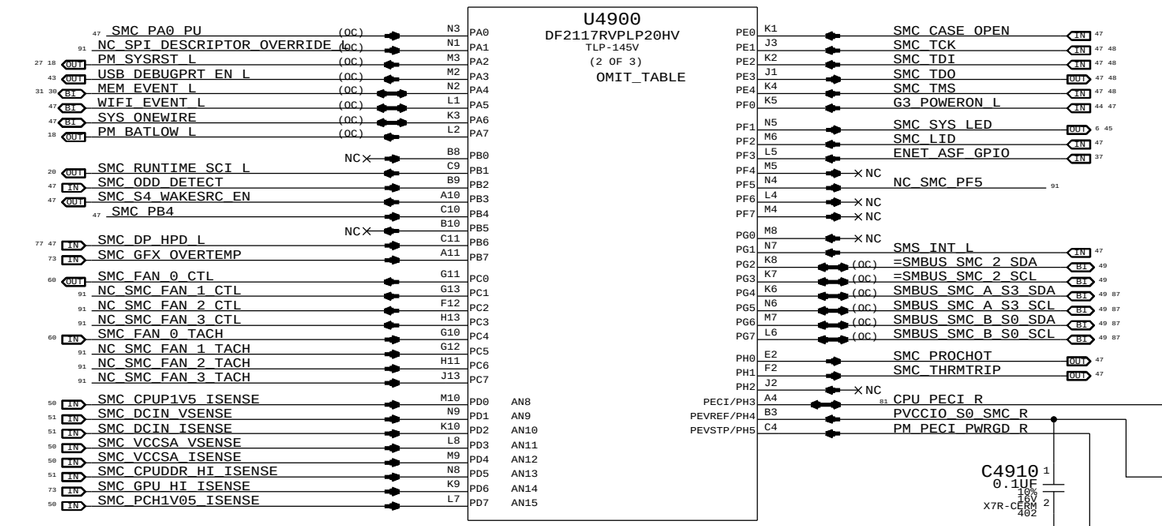
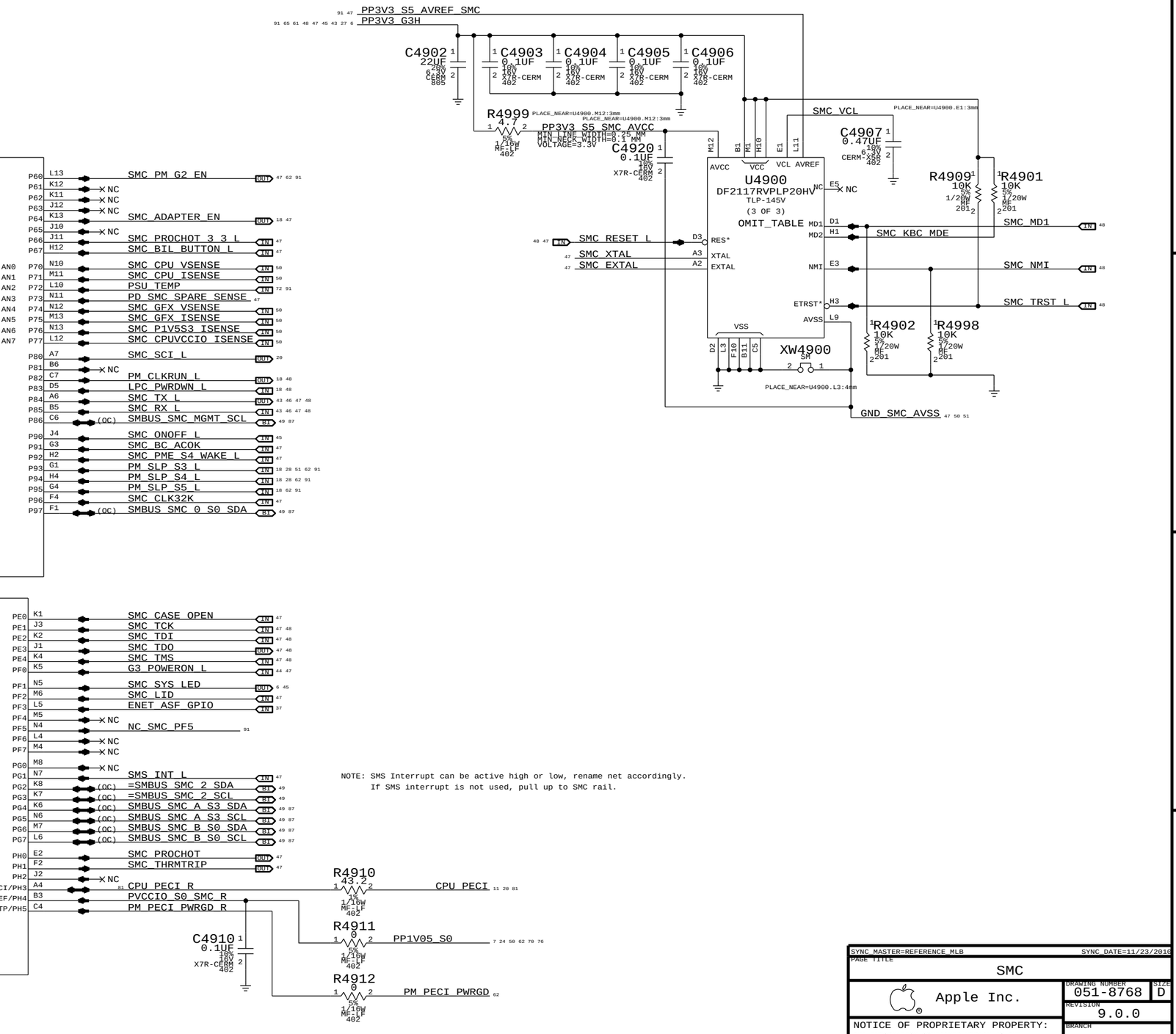
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: SMC

Apple Inc.

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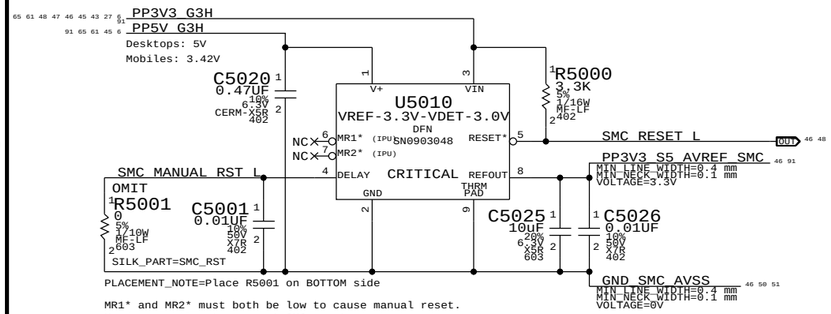
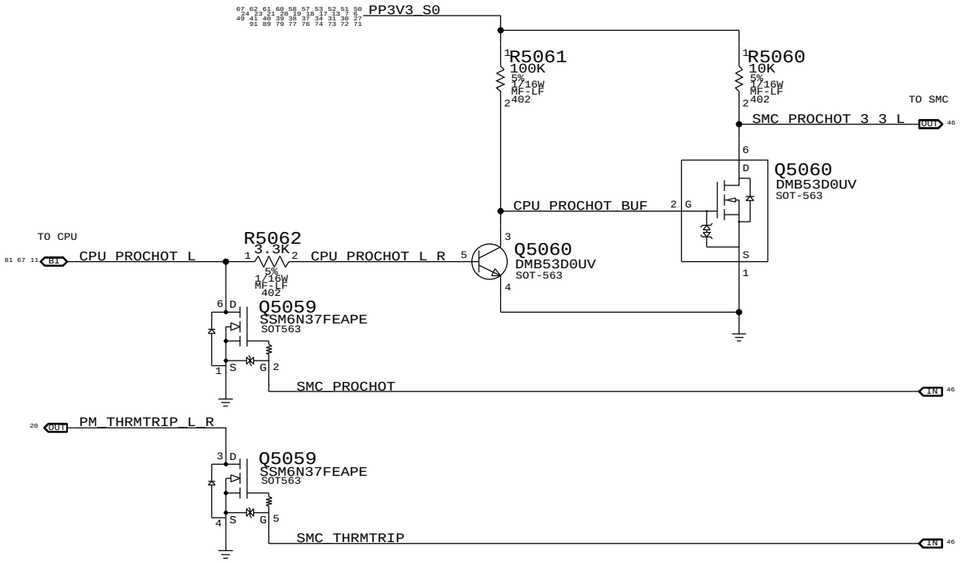
SMC Reset "Button", Supervisor & AVREF Supply



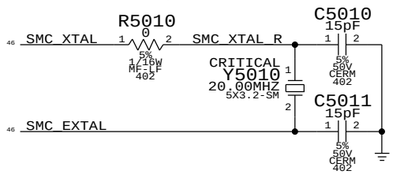
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

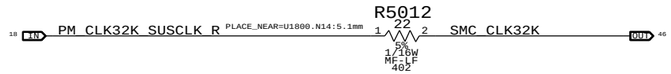
NOTE: Internal pull-ups are to VIN, not V+.

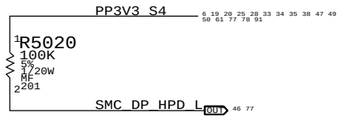
SMC FSB to 3.3V Level Shifting

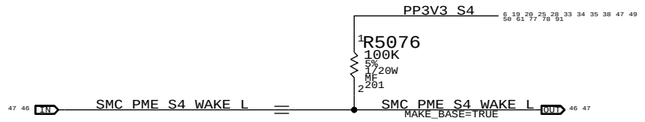


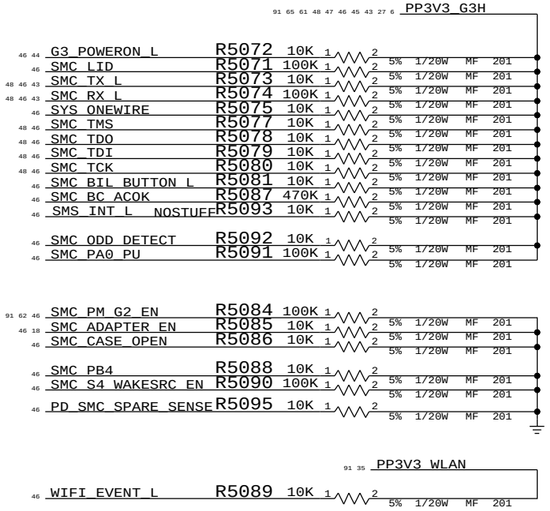
SMC Crystal Circuit











SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: SMC Support

Apple Inc.

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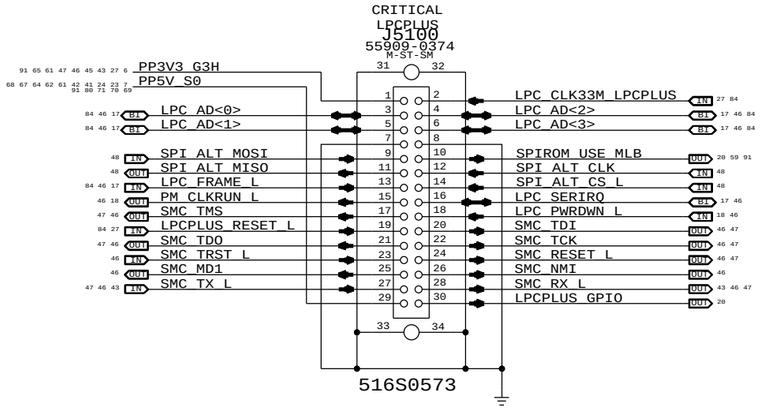
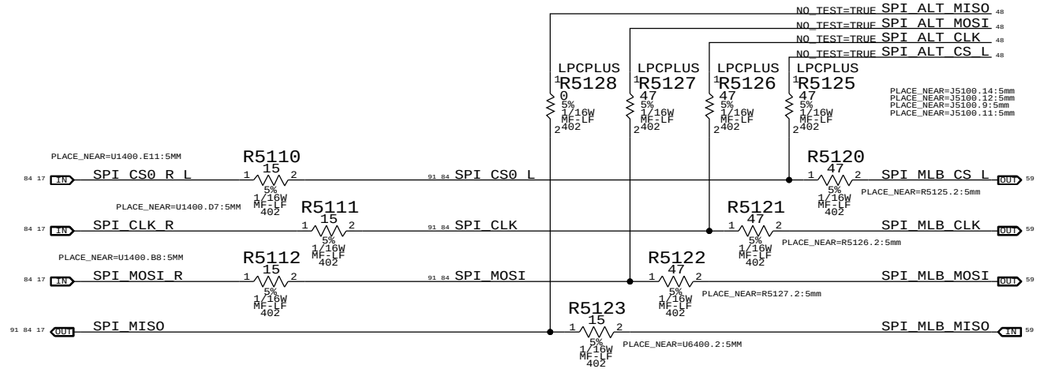
MATT CARD
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
LPC+ Debug Connector

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

BALANCED STAR TOPOLOGY

Cougar-Point
U1800
(MASTER)

SMBUS_PCH_CLK (84, 17) MAKE_BASE=TRUE
SMBUS_PCH_DATA (84, 17) MAKE_BASE=TRUE

R5202 33 5% 1/16W MF-LF 402
R5203 33 5% 1/16W MF-LF 402
R5204 33 5% 1/16W MF-LF 402
R5205 33 5% 1/16W MF-LF 402 VREFMRGN
R5206 33 5% 1/16W MF-LF 402
R5207 33 5% 1/16W MF-LF 402
R5208 33 5% 1/16W MF-LF 402
R5209 33 5% 1/16W MF-LF 402
R5212 33 5% 1/16W MF-LF 402 XDP
R5213 33 5% 1/16W MF-LF 402 XDP

SMB_PCH_STR_SCL (84)
SMB_PCH_STR_SDA (84)
SMB_PCH_DIMM_SCL (84) MAKE_BASE=TRUE
SMB_PCH_DIMM_SDA (84) MAKE_BASE=TRUE
SMB_PCH_VRF_SCL (84) MAKE_BASE=TRUE
SMB_PCH_VRF_SDA (84) MAKE_BASE=TRUE
SMB_PCH_MKY_SCL (84) MAKE_BASE=TRUE
SMB_PCH_MKY_SDA (84) MAKE_BASE=TRUE
SMB_PCH_XDP_SCL (84) MAKE_BASE=TRUE
SMB_PCH_XDP_SDA (84) MAKE_BASE=TRUE

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL (33)
=I2C_VREFDACS_SDA (33)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL (33)
=I2C_PCA9557D_SDA (33)

XDP Connectors
J2500
(MASTER)
=SMBUS_XDP_SCL (24)
=SMBUS_XDP_SDA (24)

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
=I2C_SODIMMA_SCL (30)
=I2C_SODIMMA_SDA (30)

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
=I2C_SODIMMB_SCL (31)
=I2C_SODIMMB_SDA (31)

Mikey
U6800
(Write: 0x72 Read: 0x73)
=I2C_MIKEY_SCL (58)
=I2C_MIKEY_SDA (58)

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
I2C_DPSDRVA_SCL (49) =I2C_DPSDRVA_SCL (49, 77)
I2C_DPSDRVA_SDA (49) =I2C_DPSDRVA_SDA (49, 77)

SDRVI2C:SB
R5237 33 5% 1/16W MF-LF 402
R5236 33 5% 1/16W MF-LF 402

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

Cougar-Point
U1800
(MASTER)

SML_PCH_0_CLK (17) MAKE_BASE=TRUE
SML_PCH_0_DATA (17) MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402

Cougar-Point
U1800
(Write: 0x90 Read: 0x91)

SML_PCH_1_CLK (84, 17) MAKE_BASE=TRUE
SML_PCH_1_DATA (84, 17) MAKE_BASE=TRUE

SMLink 1 is slave port to
access PCH & CPU via PECI.

R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402

SMB_SMC_B_STR_SCL (87) MAKE_BASE=TRUE
SMB_SMC_B_STR_SDA (87) MAKE_BASE=TRUE

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

SMBUS_SMC_0_S0_SCL (87, 46) MAKE_BASE=TRUE
SMBUS_SMC_0_S0_SDA (87, 46) MAKE_BASE=TRUE

T29 Temp
EMC1414-A:U5535
(WRITE: 0X78 READ: 0X79)
=I2C_T29THMSNS_SCL (52)
=I2C_T29THMSNS_SDA (52)

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S4

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

SMBUS_SMC_A_S3_SCL (87, 46) MAKE_BASE=TRUE
SMBUS_SMC_A_S3_SDA (87, 46) MAKE_BASE=TRUE

RMT TEMP
LM952141:U5500
(WRITE: 0X30 READ: 0X31)
=SMBUS_REMOTE_THMSNS_SCL
=SMBUS_REMOTE_THMSNS_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402
R5262 33 5% 1/16W MF-LF 402
R5263 33 5% 1/16W MF-LF 402
R5264 33 5% 1/16W MF-LF 402
R5265 33 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

SMBUS_SMC_B_S0_SCL (87, 46) MAKE_BASE=TRUE
SMBUS_SMC_B_S0_SDA (87, 46) MAKE_BASE=TRUE

SMB_SMC_B_TSN_SCL (87) MAKE_BASE=TRUE
SMB_SMC_B_TSN_SDA (87) MAKE_BASE=TRUE

SYSTEM TEMP SENSORS
EMC1428: U5500
(WRITE: 0X92 READ: 0X93)
=I2C_CPUTHMSNS_SCL (52)
=I2C_CPUTHMSNS_SDA (52)

SMC "2" SMBUS CONNECTIONS

PULL-UPS ON ENET PAGE
TO 3.3V ENET RAIL.

ENET ASF (MINI-LOM)
U3900
(MASTER)

ENET_ASF_SMB_CLK (87, 37) MAKE_BASE=TRUE
ENET_ASF_SMB_DATA (87, 37) MAKE_BASE=TRUE

SMC
H8S_2117RP:U4900
(WRITE: 0X?? READ: 0X??)
=SMBUS_SMC_2_SCL (46)
=SMBUS_SMC_2_SDA (46)

SMC "Management" SMBus Connections

PP3V3_S4

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

SMBUS_SMC_MGMT_SCL (87, 46) MAKE_BASE=TRUE
SMBUS_SMC_MGMT_SDA (87, 46) MAKE_BASE=TRUE

T29 SMBus Connections

PP3V3_S0

T29 IC
U9000
(MASTER)

I2C_T29_SCL (86, 74) MAKE_BASE=TRUE
I2C_T29_SDA (86, 74) MAKE_BASE=TRUE

R5230 4.7K 5% 1/16W MF-LF 402
R5231 4.7K 5% 1/16W MF-LF 402

T29 Port A MCU
J9330
(Write: 0x26 Read: 0x27)
=I2C_T29AMCU_SCL (77)
=I2C_T29AMCU_SDA (77)

SIGNAL_MODEL=EMPTY
SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
I2C_DPSDRVA_SCL (49) =I2C_DPSDRVA_SCL (49, 77)
I2C_DPSDRVA_SDA (49) =I2C_DPSDRVA_SDA (49, 77)

SYNC_MASTER=J40S	SYNC_DATE=11/23/2010
PAGE TITLE	SMBus Connections
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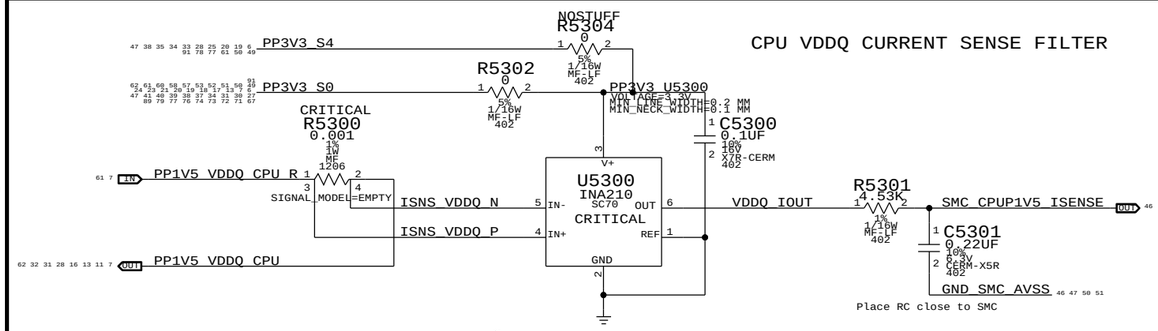
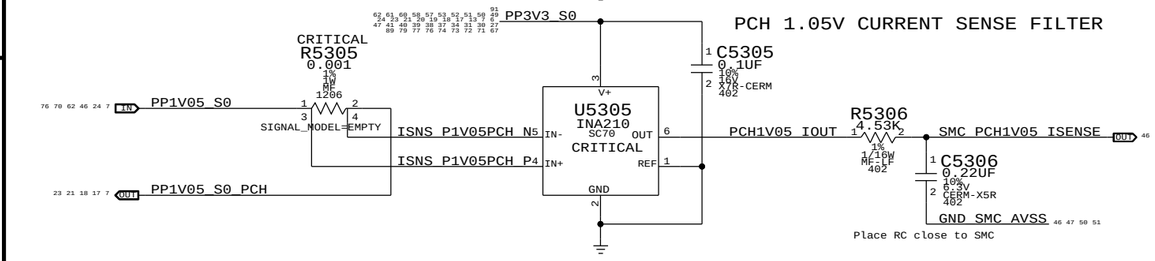
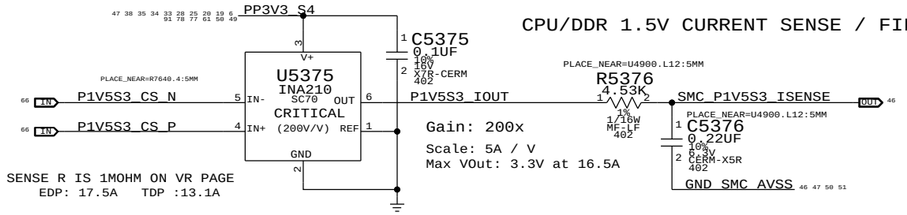
CPU VDDQ CURRENT SENSE FILTER



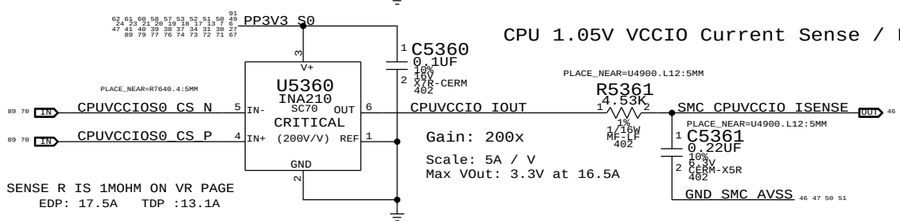
PCH 1.05V CURRENT SENSE FILTER



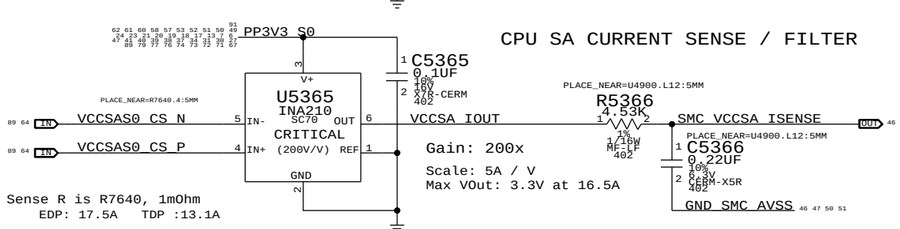
CPU/DDR 1.5V CURRENT SENSE / FILTER



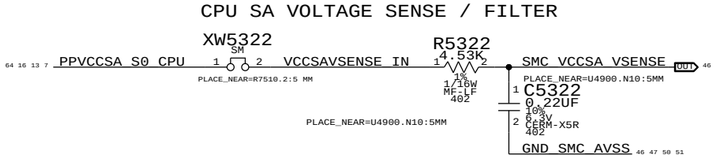
CPU 1.05V VCCIO Current Sense / Filter



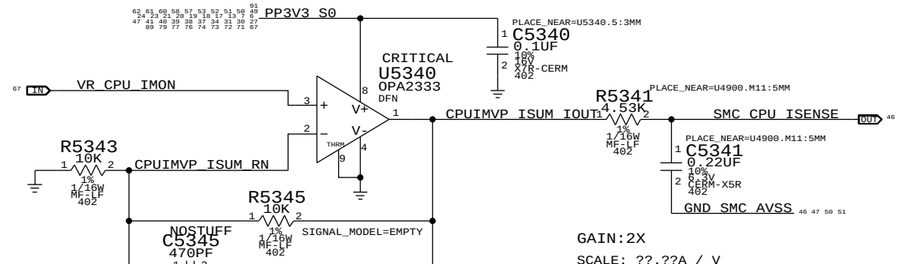
CPU SA CURRENT SENSE / FILTER



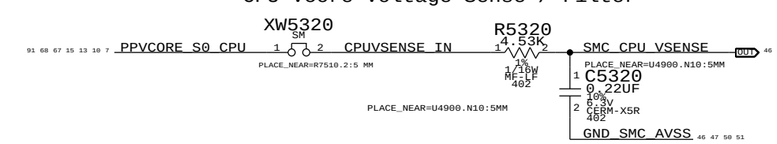
CPU SA VOLTAGE SENSE / FILTER



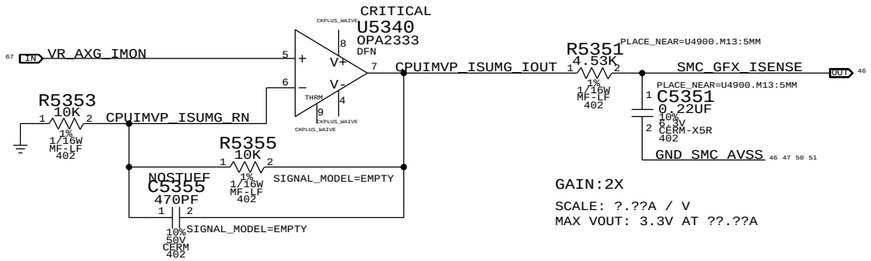
CPU VCORE IMON CURRENT SENSE / FILTER



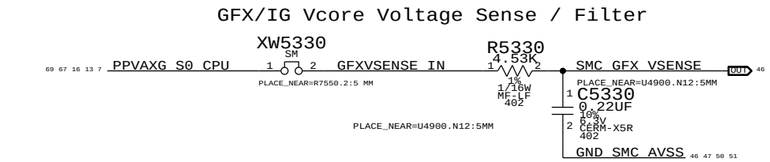
CPU Vcore Voltage Sense / Filter



GFX/IG VCORE IMON CURRENT SENSE / FILTER



GFX/IG Vcore Voltage Sense / Filter



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
Voltage & Load Side Current Sensing

Apple Inc.

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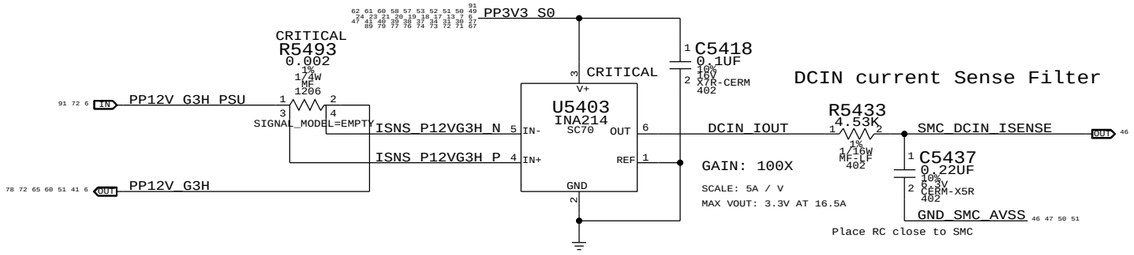
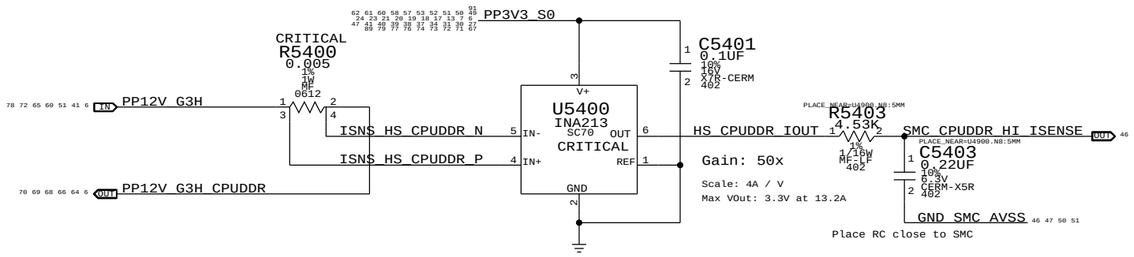
J40I, J40S, AND J40

PSU CURRENT SENSE



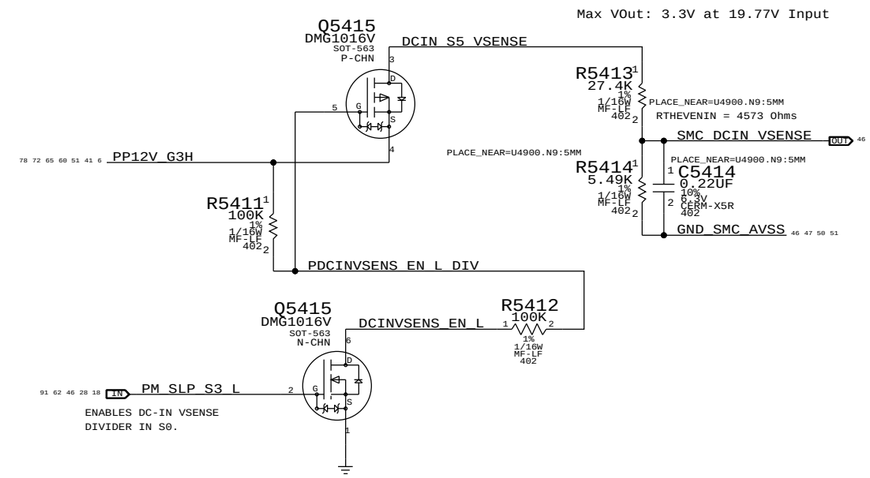
DCIN current Sense Filter

CPU / DDR HIGH SIDE CURRENT SENSE / FILTER



DC-In Voltage Sense Enable & Filter

TURN ON DIVIDER ONLY IN S0.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2011

PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

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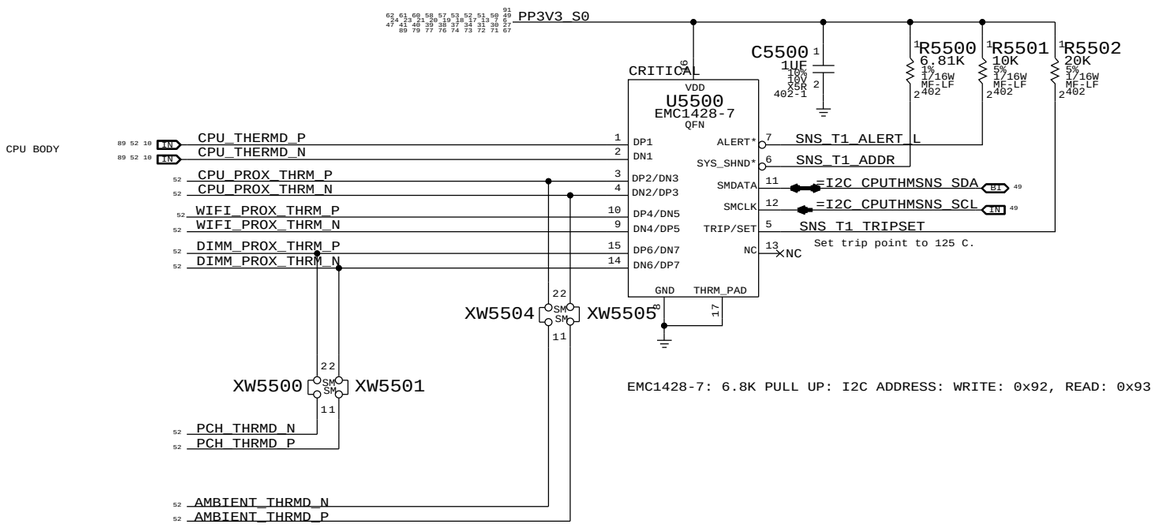
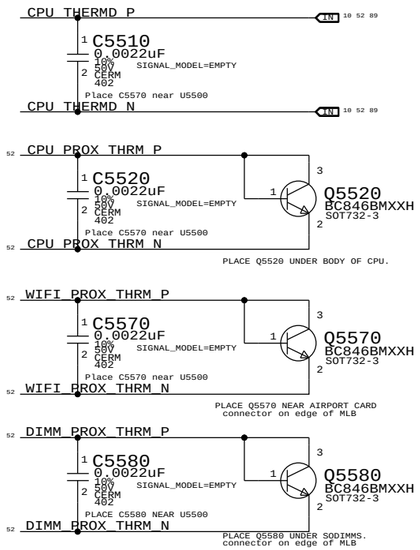
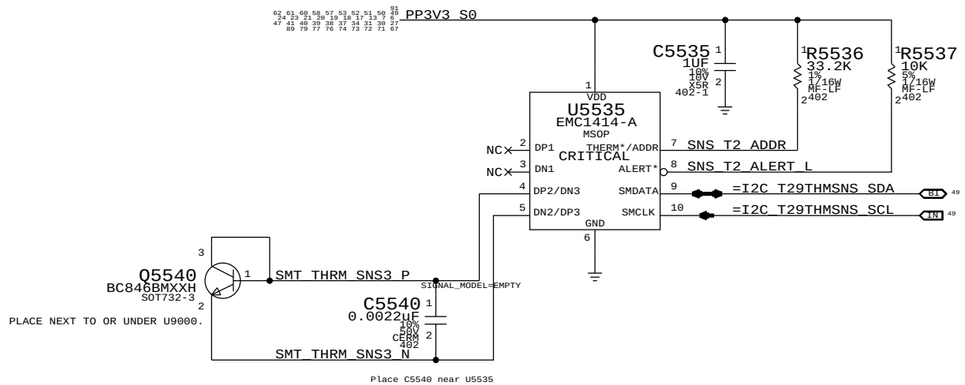




T29 PROXIMITY THERMAL SENSORS



EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC_MASTER=J40S SYNC_DATE=11/23/2010

PAGE TITLE: THERMAL SENSORS

Apple Inc.

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AUDIO CODEC
APPLE P/N 353S3199

PP1V5_S0
CRITICAL C5600 4.7UF 20% 6.3V X5R 0306
CRITICAL C5602 10UF 20% 16V TANT-POLY 2012-LLP
C5603 0.1UF 10% 16V X7R-CERM 402
CRITICAL C5604 10UF 20% 16V TANT-POLY 2012-LLP
C5605 0.1UF 10% 16V X7R-CERM 402
C5606 1UF 10% 16V X5R 402-1
CRITICAL C5608 10UF 20% 6.3V X5R 0508
PP3V3_S0
PP4V5_AUDIO_ANALOG
GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG → R5600 2.67K 1% 1/16W MF-LF 402 → VBIAS_DAC
NC_CS4206_FP

U5600 CS4206B QFN

9	VD		
24	VA_REF		
46	VA_HP		
25	VA		
29	VBIAS_DAC		
44	VHP_FILT+	HPOUT_L	38
41	VHP_FILT-	HPOUT_R	40
		HPREF	39
2	GPIO0/DMIC_SDA1	LINEOUT_L1+	35
12	GPIO1/DMIC_SDA2	LINEOUT_L1-	34
14	GPIO2/SPDIF_OUT2	LINEOUT_R1+	36
15	GPIO3	LINEOUT_R1-	37
13	SENSE_A	LINEOUT_L2+	31
		LINEOUT_L2-	30
		LINEOUT_R2+	32
		LINEOUT_R2-	33
45	FLYP		
43	FLYC		
42	FLYN		
		MICBIAS	16
3	VL_HD		
		VCOM	28
1	VL_IF		
6	BITCLK	LINEIN_L+	21
		LINEIN_C-	22
		LINEIN_R+	23
10	SYNC		
8	SDI	MICIN_L+	18
5	SDO	MICIN_L-	17
11	RESET*	MICIN_R+	19
		MICIN_R-	20
47	SPDIF_IN		
48	SPDIF_OUT		
		VREF+_ADC	27
		DMIC_SCL	4
7	DGND		
49	THRM_PAD		
26	AGND		

EXT HP AMP CNTRL
SPKR AMP CNTRL

NC_AUD_GPIO_0
AUD_GPIO_1
NC_AUD_GPIO_2
NC
AUD_GPIO_3
AUD_SENSE_A

HPOUT_L → NC_AUD_HP_PORT_L → NC
HPOUT_R → NC_AUD_HP_PORT_R → NC
HPREF → AUD_HPREF → XW5610 SM → GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM

LINEOUT_L1+ → AUD_LO2_P_L
LINEOUT_L1- → AUD_LO2_N_L
LINEOUT_R1+ → AUD_LO2_P_R
LINEOUT_R1- → AUD_LO2_N_R
EXTERNAL HP AMP

LINEOUT_L2+ → AUD_LO3_P_L
LINEOUT_L2- → AUD_LO3_N_L
LINEOUT_R2+ → NC_AUD_LO3_P_R → NC
LINEOUT_R2- → NC_AUD_LO3_N_R → NC
SPEAKER AMP

PP4V5_AUDIO_ANALOG → CRITICAL

MICBIAS → NC_CS4206_MICBIAS → NC

VCOM → CS4206_VCOM (MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM) → NC

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0 → R5601 22 5% 1/16W MF-LF 402 → AUD_SDI_R
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN
AUD_SPDIF_OUT ← R5602 22 5% 1/16W MF-LF 402 ← CS4206_SPDIF_OUT

R5603 100K 1% 1/10W MF-LF 402

LINEIN_L+ → AUD_LI_P_L
LINEIN_C- → MAKE_BASE=TRUE → AUD_LI_N_LR
LINEIN_R+ → AUD_LI_P_R

MICIN_L+ → AUD_MIC_INP_L
MICIN_L- → AUD_MIC_INN_L
MICIN_R+ → NC_AUD_MIC_INP_R → NC
MICIN_R- → NC_AUD_MIC_INN_R → NC
EXTERNAL MIC INPUT

VREF+_ADC → CS4206_VREF_ADC (MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM) → NC

DMIC_SCL → TP_AUD_DMIC_CLK → NC

CRITICAL C5613 1UF 10% 10V X5R CASE-P3-HF
CRITICAL C5614 10UF 20% 6.3V POLY-TANT CASE-B2-SM

GND_AUDIO_CODEC

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234

CRITICAL L5651 FERR-120-OHM-1.5A 0402 → PP5V_AUDIO_HPAMP (VOLTAGE=5V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM)
CRITICAL L5650 FERR-120-OHM-1.5A 0402

PP5V_S0_AUDIO → R5650 1.02K 1% 1/20W MF 201 → AUD_REG_SHDN_L
PP3V3_S0

AUD_4V5_REG_IN (VOLTAGE=5V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM)

U5601 MAX8840-4.5V UDFN CRITICAL

1	IN	OUT	6
		BP	4
3	SHDN*		
	GND	NC	5 → NC

MAX8840_BP (MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM)

C5650 0.1UF 10% 16V X7R-CERM 402
C5651 1UF 10% 16V X5R 402-1
C5652 0.001UF 10% 50V X7R 402
C5653 0.01UF 10% 50V X7R 402
C5654 1UF 10% 10V X5R 402-1

PP4V5_AUDIO_ANALOG (VOLTAGE=4.5V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM)

XW5600 SM
XW5601 SM

GND_AUDIO_CODEC (VOLTAGE=0V MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM NO_TEST=TRUE)
GND_AUDIO_HPAMP (VOLTAGE=0V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NO_TEST=TRUE)

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: AUDIO:CODEC

Apple Inc.

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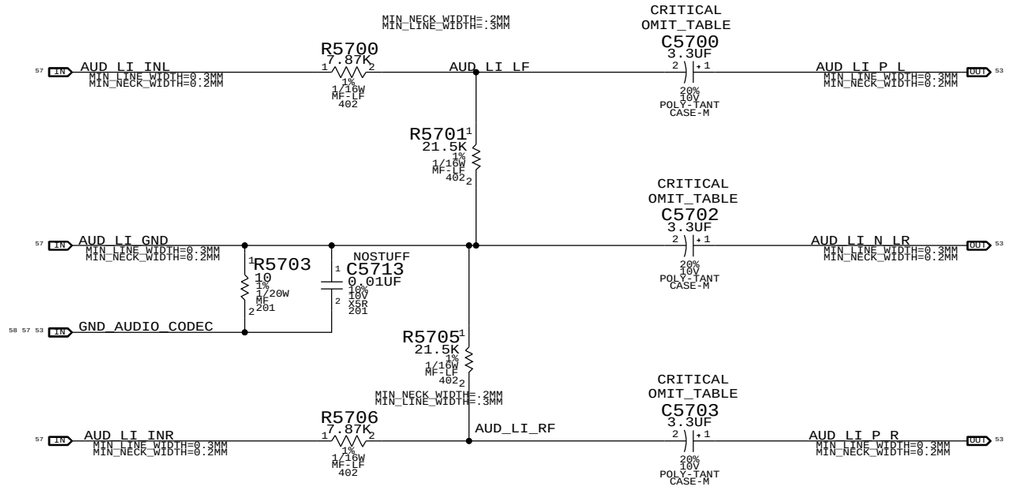
CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0309	3	CAP,TANT,POLY,4.7UF,20%,10V,SMD	C5700,C5702,C5703	CRITICAL	?

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
AUDIO:LINE-IN

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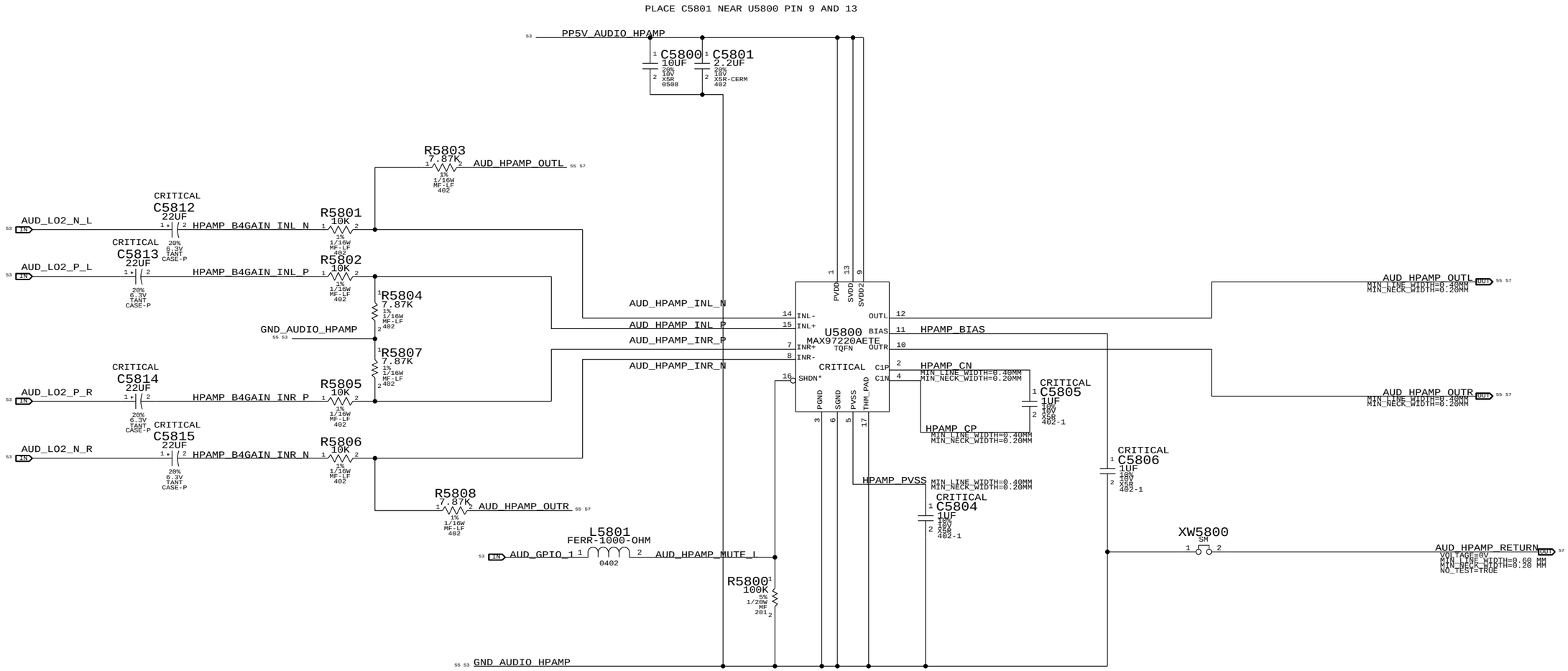
HEADPHONE AMPLIFIER (MAX97220A)

APN:353S3081

VOLTAGE GAIN:-2DB.TO GET 2VRMS FROM 2.67VRMS



DAC FILTER: @ 168KHZ

CODEC FILTER STOPBAND:26.256KHZ, ATTENUATION FROM STOPBAND TO 100KHZ IS 102DB

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

AUDIO:HEADPHONE AMP

Apple Inc.

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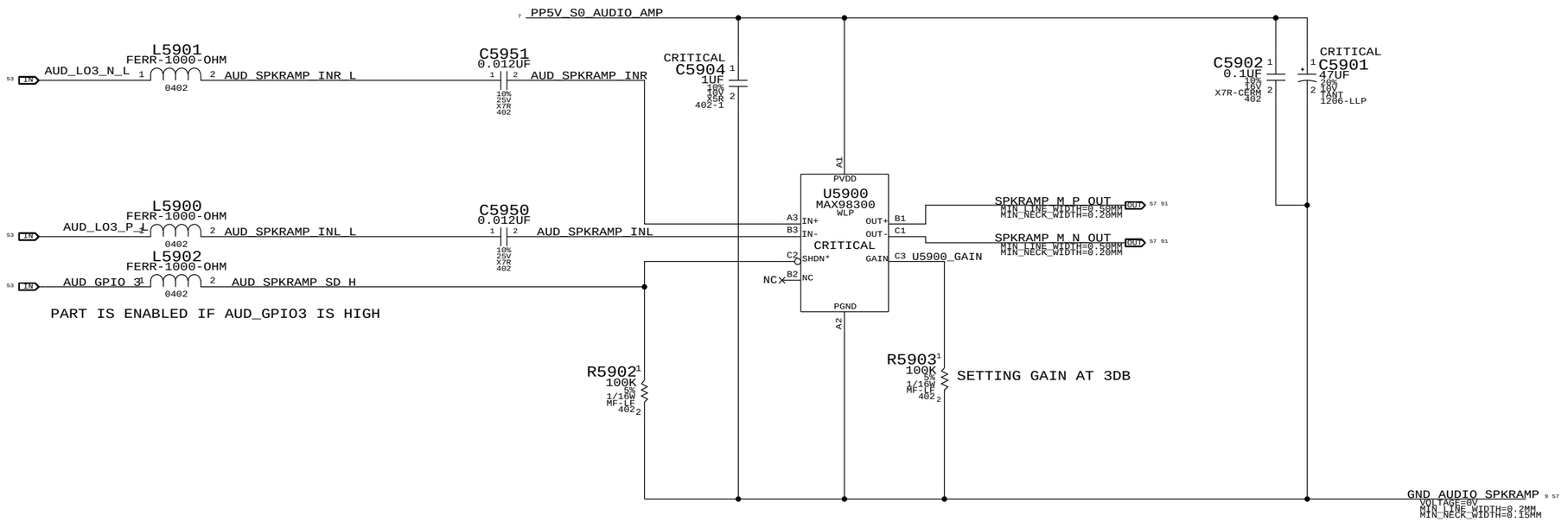
MONO SPEAKER AMPLIFIER

APN 353S2888

GAIN = 3 DB NOM TO ALLOW A LITTLE MORE THAN 1% THD POWER = 2.1W AT 4OHMS.
FC = 470 HZ. RIN AT 3DB IS 28K.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

AUDIO:SPEAKER AMP

Apple Inc.

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AUDIO JACK 1 LO/HP CONNECTOR, SPDIF TX

APN 514-0761
CRITICAL

J6000
AUDIO-TX-RX-SPDIF-BLK-J40
F-RT-TH

AUDIO TX: MIC 5, TYPE_DETECT 4, LEFT 1, RIGHT 2, GND 3, GND 6, HP_DETECT 7, IPHS_DETECT 9, GND 8

AUD_CONNJ1_MIC_HI — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_SLEEVEDET — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_TIP — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_RING — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_SLEEVE — MIN_LINE_WIDTH=0.60 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_TIPDET — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ1_PERIPHDET — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM

L6000 FERR-1000-OHM 0402 — HS_MIC_LO (OUT 58)
L6001 FERR-1000-OHM 0402 — HS_MIC_HI (OUT 58)
L6002 FERR-1000-OHM 0402 — AUD_J1_SLEEVEDET (OUT 58)
L6006 CRITICAL FERR-120-OHM-1.5A 0402 — AUD_HPAMP_OUTL (BI 55)
L6007 CRITICAL FERR-120-OHM-1.5A 0402 — AUD_HPAMP_OUTR (BI 55)
OMIT TABLE L6004 RESISTER ON FERRITE PADS!!
FERR-220-OHM-2.5A 0603 — AUD_HPAMP_RETURN (BI 55)
L6005 FERR-1000-OHM 0402 — AUD_J1_TIPDET (OUT 58)
L6003 FERR-1000-OHM 0402 — AUD_J1_PERIPHDET (OUT 58)
AUD_SPDIF_OUT (IN 53)

DZ6000 6.8V-100PF 402
DZ6002 ESDALC5-1BM2 SOD882
DZ6004 6.8V-100PF 402
DZ6006 ESDALC5-1BM2 SOD882
DZ6001 6.8V-100PF 402
DZ6003 ESDALC5-1BM2 SOD882
DZ6005 ESDALC5-1BM2 SOD882

LED
VIN A, VCC B, GND C
OPERATING VOLTAGE 3.3
POF

GND_CHASSIS_AUDIO_JACK 57

AUDIO JACK 2 LINE IN CONNECTOR, SPDIF RX

AUDIO RX: TYPE_DETECT 13, LEFT 10, RIGHT 11, GND 12
TIP_DETECT 15, GND 14
SENSOR — VDD D, GRD E, VOUT F
OPERATING VOLTAGE 3.3
POF

SHELL 22, SHIELD PINS 23, 24, 25

PP3V3_S0

C6050 1UF 10V X5R 402-1
C6000 1UF 10V X5R 402-1

AUD_CONNJ2_TIP — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ2_RING — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ2_SLEEVE — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_CONNJ2_TIPDET — MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM
AUD_J2_OPT_OUT

L6054 FERR-1000-OHM 0402 — AUD_LI_INL (BI 54)
L6052 FERR-1000-OHM 0402 — AUD_LI_INR (OUT 54)
CRITICAL L6051 600-OHM-300MA 0402 — AUD_LI_GND (OUT 54)
L6053 FERR-1000-OHM 0402 — AUD_J2_TIPDET_R (BI 58)
R6060 22 5% 1/16W MF-LF 402 — AUD_SPDIF_IN (OUT 53)
DO NOT PLACE UNDER SD CARD CONNECTOR.

DZ6052 6.8V-100PF 402
DZ6055 ESDALC5-1BM2 SOD882
DZ6051 ESDALC5-1BM2 SOD882
NOSTUFF C6051 0.01UF 10V X7R 402
DZ6054 ESDALC5-1BM2 SOD882
NOSTUFF C6054 0.01UF 10V X7R 402
DZ6050 6.8V-100PF 402
DZ6053 6.8V-100PF 402

GND_CHASSIS_AUDIO_JACK 57

PLACE ONE DIODE AT EACH CONNECTOR GND PIN, WITH CAP ADJACENT.
ROUTE FROM CONNECTOR PIN TO DIODE AND CAP, THEN TO FERRITE.

GROUND STUFF OPTIONS
PLACE CLOSE TO CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0022	2	RES,ZERO OHM,0603	L6004,L6092	

RESISTER ON FERRITE PADS!!
OMIT TABLE
L6092 FERR-70-OHM-4A 0603
NOSTUFF R6090 0 5% 1/16W MF-LF 402
NOSTUFF R6091 0 5% 1/16W MF-LF 402
GND_CHASSIS_AUDIO_JACK 57 — VOLTAGE=0V, MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM
GND_AUDIO_CODEC 53 54 58

SPEAKER CONNECTOR
APN 518S0519

J6001
78171-0002
M-RT-SM

SPKRAMP_M_P_OUT 1 (91 56 IN)
SPKRAMP_M_N_OUT 2 (91 56 IN)
GND_AUDIO_SPKRAMP 4 (56 9)
3

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: AUDIO:JACKS

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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

FLP = 8.82 KHZ
FHP = 80 HZ

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_1	0X0A(D)
SPEAKER 1	0X04 (4)	0X04 (04)	0X0B (11)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (08)	0X10 (16)	N/A	0X0D(B)

COUGAR POINT OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HDMI OUT	N/A	-	-	N/A	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	GAIN/MUTE	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X05 (05)	0X0C (12)	N/A	0X0C(C)
EXT MIC IN	0X06 (6)	0X06 (06)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY
SPDIF IN	N/A	0X07 (07)	0X0F (15)	N/A	N/A

SYSTEM INT AND GPIO LINES

FUNCTION	
MIKEY ENABLE	SATA4GP/GPIO16
MIKEY INTERRUPT	PIRQG*/GPIO5
PERIPHERAL DETECT	PIRQF*/GPIO3

WRITE: 0X72 READ: 0X73

LOW = DIGITAL (PLASTIC)
HIGH = ANALOG (METAL)

PORT D DETECT

PORT B DETECT (SPDIF DELEGATE)

PORT C DETECT

EXTRACTION NOTIFICATION CKT

KEEP DET TRACE AS SHORT AS POSS

PLACE L6100/C6100 CLOSE TO Q6100/01/02/03

SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE: AUDIO:JACK TRANSLATORS	
Apple Inc.	DRAWING NUMBER: 051-8768 SIZE: D
	REVISION: 9.0.0
	BRANCH:
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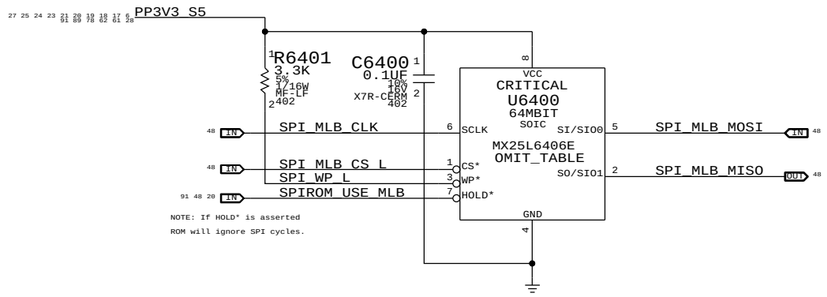

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

SPI BOOT ROM

Apple Inc.

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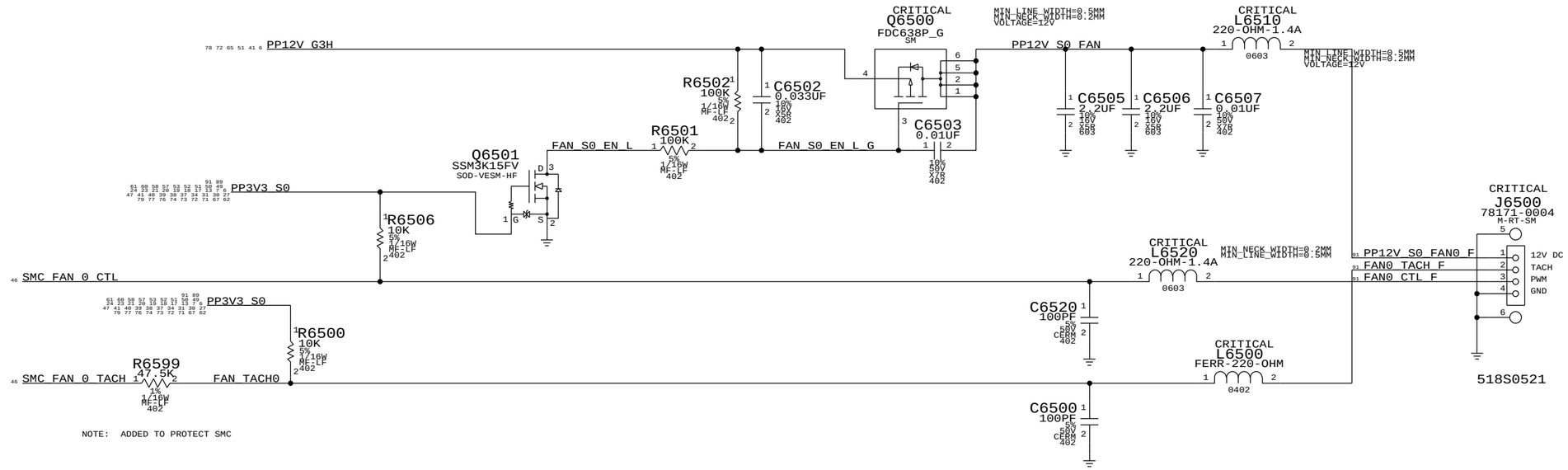
FAN CONTROL CIRCUIT



SYNC_MASTER=REFERENCE_MLB	SYNC_DATE=11/23/2010
PAGE TITLE: Fan Control Circuit	
Apple Inc.	DRAWING NUMBER: 051-8768 SIZE: D
	REVISION: 9.0.0
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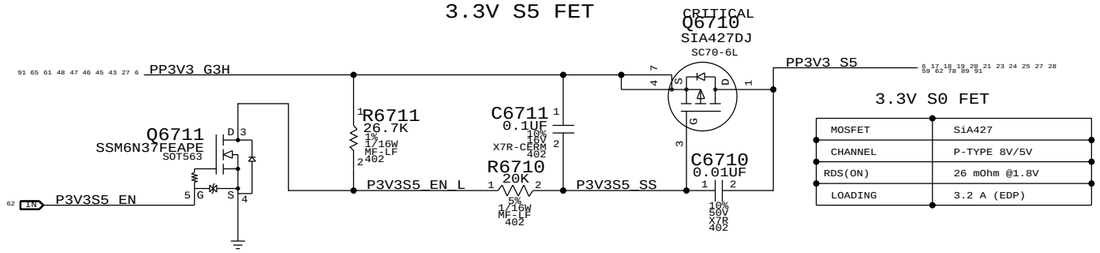
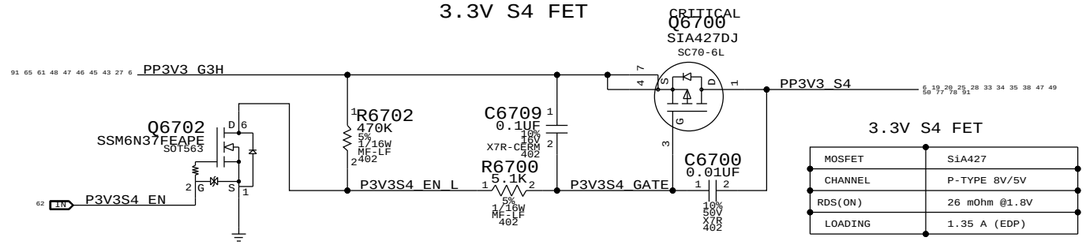
3.3V S5 FET



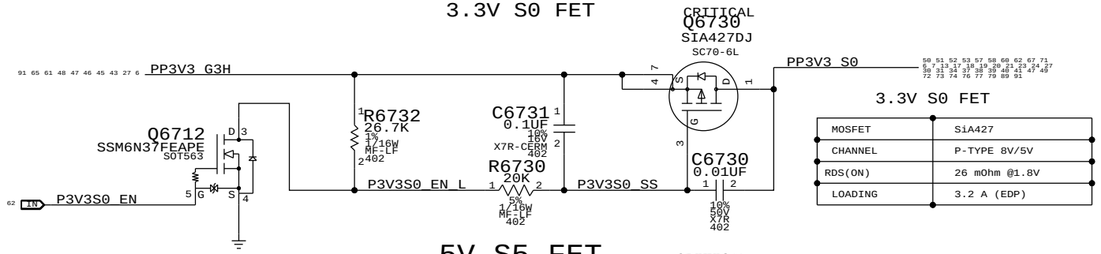
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V S4 FET



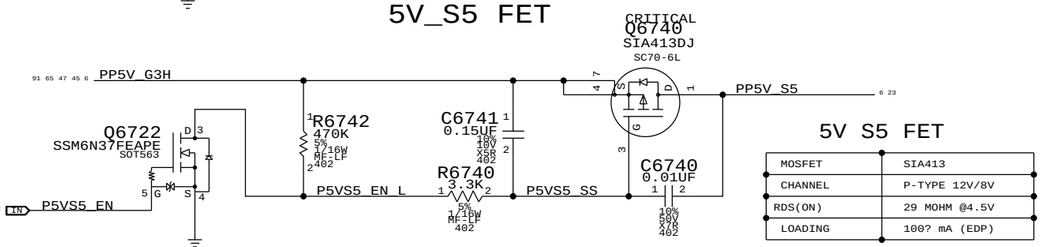
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

3.3V S0 FET



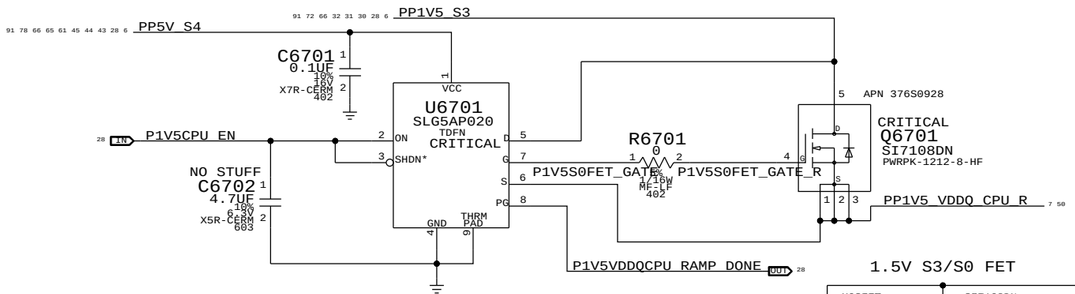
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

5V_S5 FET



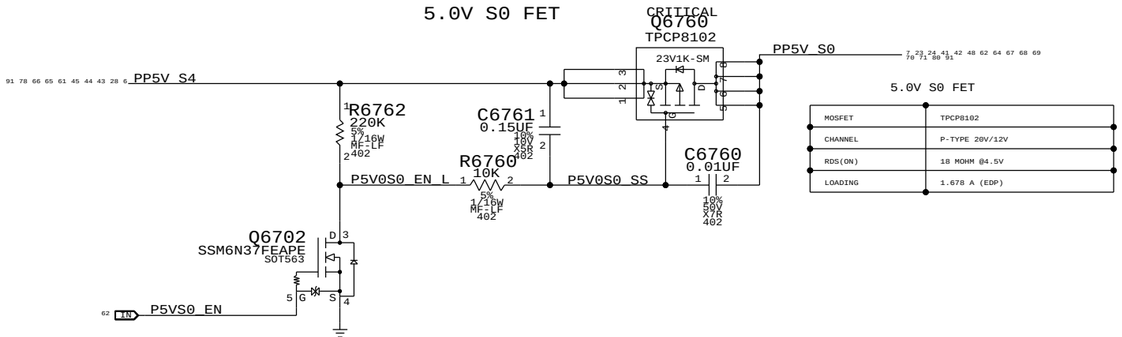
5V S5 FET	
MOSFET	SIA413
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 MOHM @4.5V
LOADING	100? mA (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE 20V/12V
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=REFERENCE_MLB SYNC DATE=12/13/2010

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-8768 SIZE D

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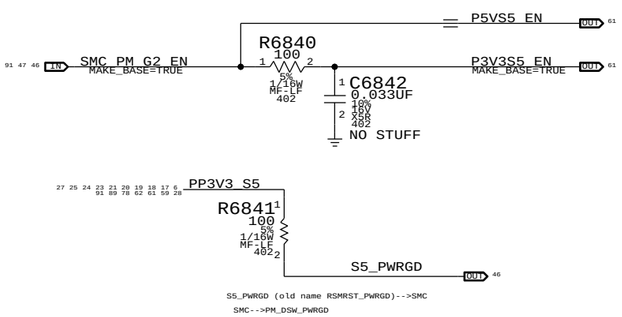
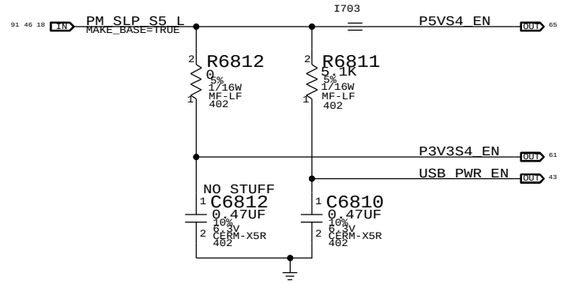
S5 Rail Enables & PGOOD



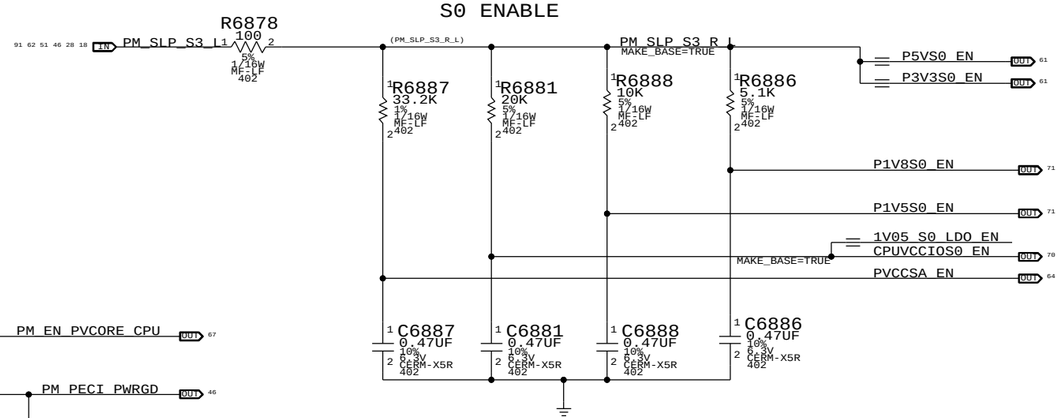
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
STANDBY (S5)	1	0	0	0
AC POWER (G3HOT)	0	0	0	0

3.3V,5V S4 ENABLE

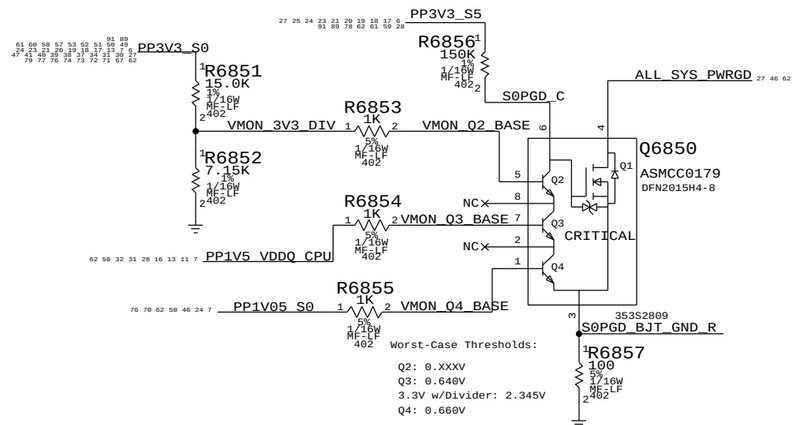


3.3V,5V S3 ENABLE

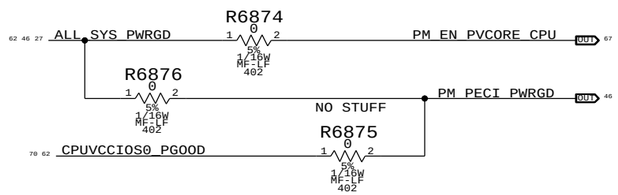
S0 ENABLE



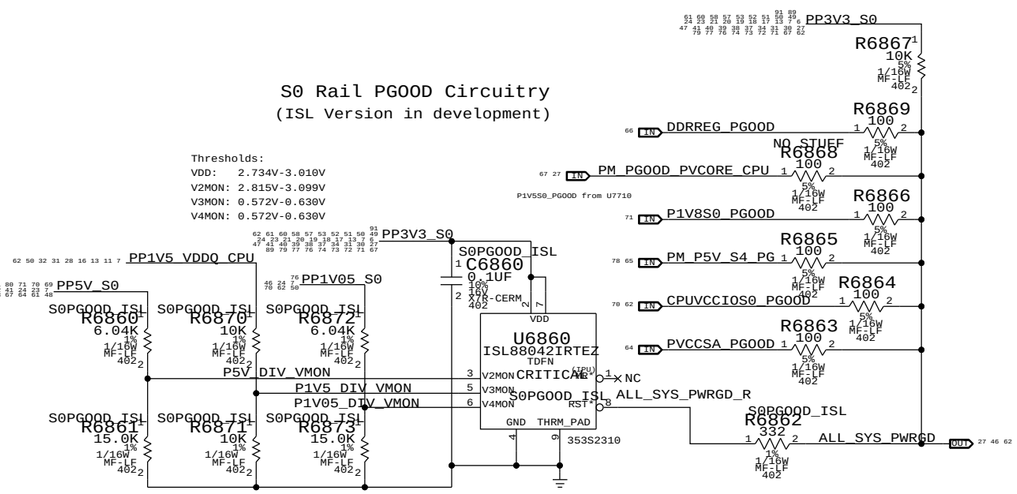
S0 Rail PGOOD (BJT Version)



CPUVCORE ENABLE



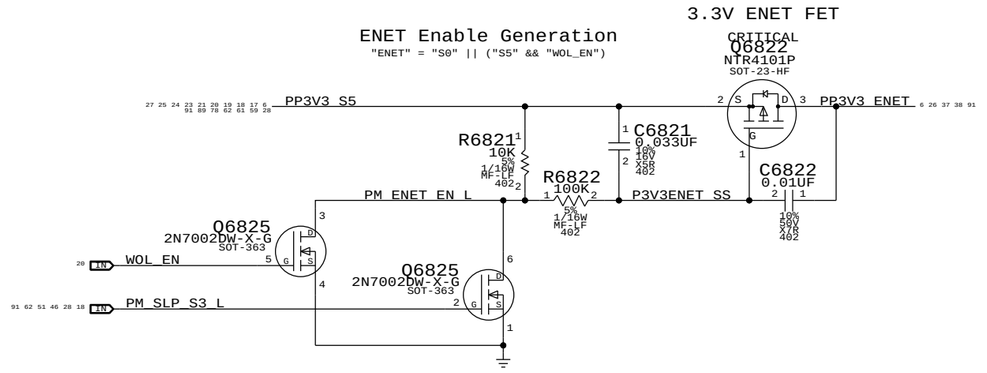
S0 Rail PGOOD Circuitry
(ISL Version in development)



ENET Enable Generation

"ENET" = "S0" || ("S5" && "WOL_EN")

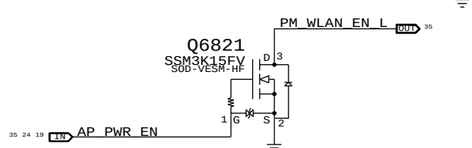
3.3V ENET FET



WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN")

NOTE: S4 TERM IS GUARANTEED BY S3 PULL-UP ON OPEN-DRAIN AP_PWR_EN SIGNAL.



SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2010

PAGE TITLE

Power Control 1/ENABLE

Apple Inc.

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ROOM FOR MORE?

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

POWER CONTROL CONT.

Apple Inc.

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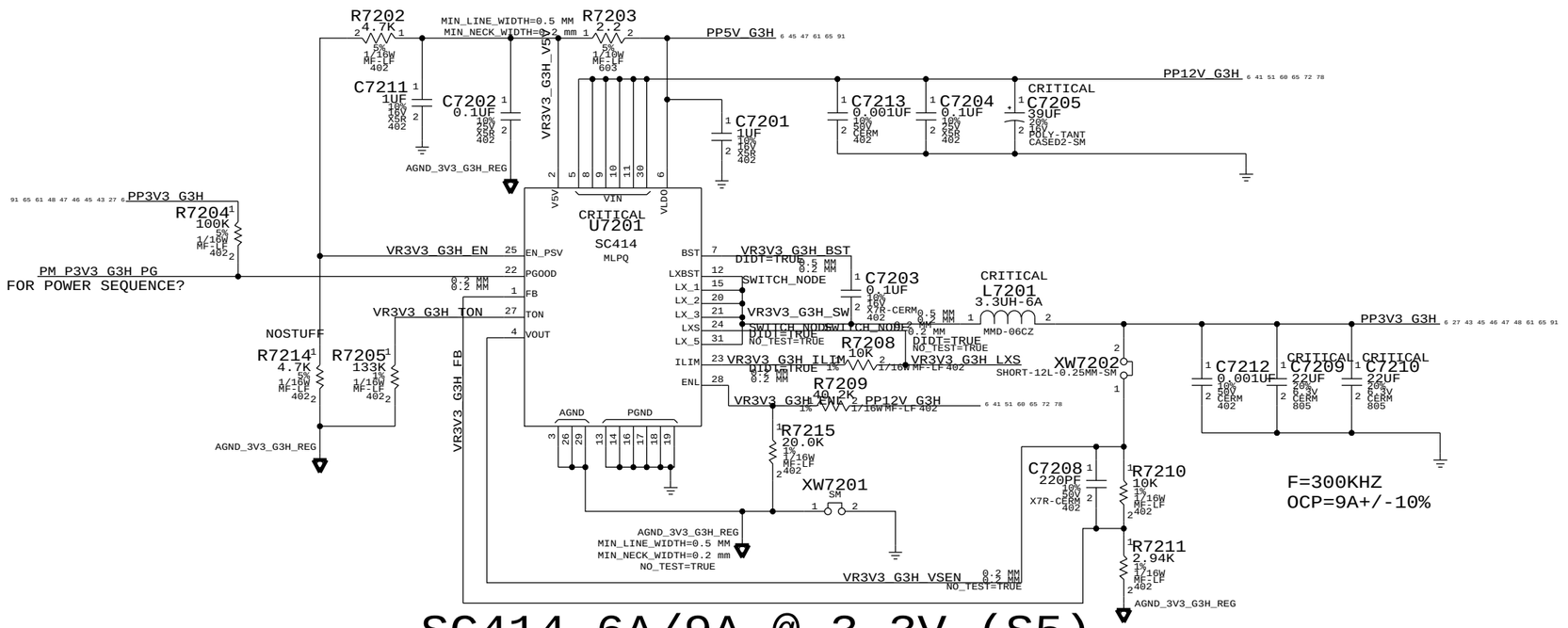

SYNC MASTER=REFERENCE MLB SYNC DATE=11/23/2010

PAGE TITLE

VR - 3.3V S5 AND 5V S4

Apple Inc.

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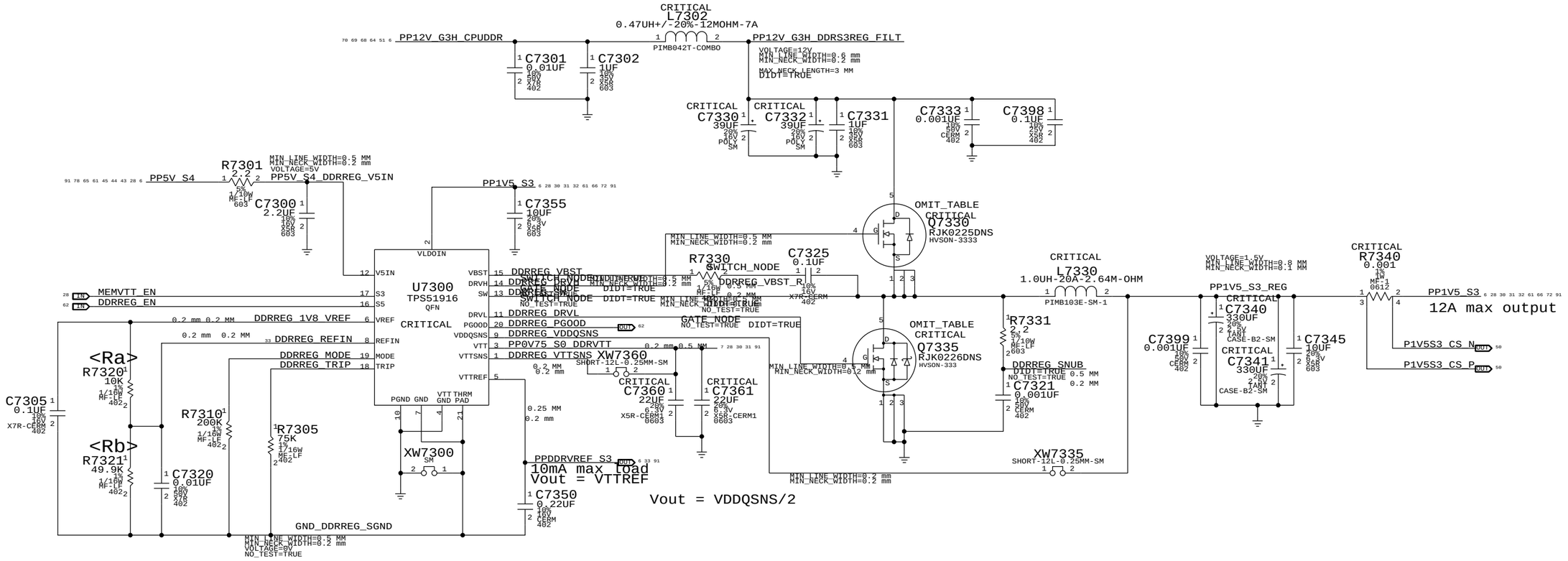

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0979	1	TRA,FET,FAIRCHILD	Q7330	CRITICAL	FET_SET_A:FAIRCHILD
376S0874	1	TRA,FET,FAIRCHILD	Q7335	CRITICAL	FET_SET_A:FAIRCHILD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0964	1	TRA,FET,RENESAS	Q7330	CRITICAL	FET_SET_A:RENESAS
376S0965	1	TRA,FET,RENESAS	Q7335	CRITICAL	FET_SET_A:RENESAS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-3109	1	COMP SET,FETS,FAIRCHILD	CSET1	CRITICAL	FET_SET_A:USE_PHANTOMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-3110	085-3109	FET_SET_A:USE_PHANTOMS	CSET1	COMP SET,FETS,RENESAS

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: DDR 1.5V VR

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

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CPU CORE/AXG REG 1.1V/53A O/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = 53A
AVG = 36A

FS=300KHZ
FS=350KHZ

SYNC_MASTER=J481	SYNC_DATE=11/23/201
PAGE TITLE	VR - CPU VCORE & GPU CONTROLLER
Apple Inc.	DRAWING NUMBER 051-8768 SIZE D
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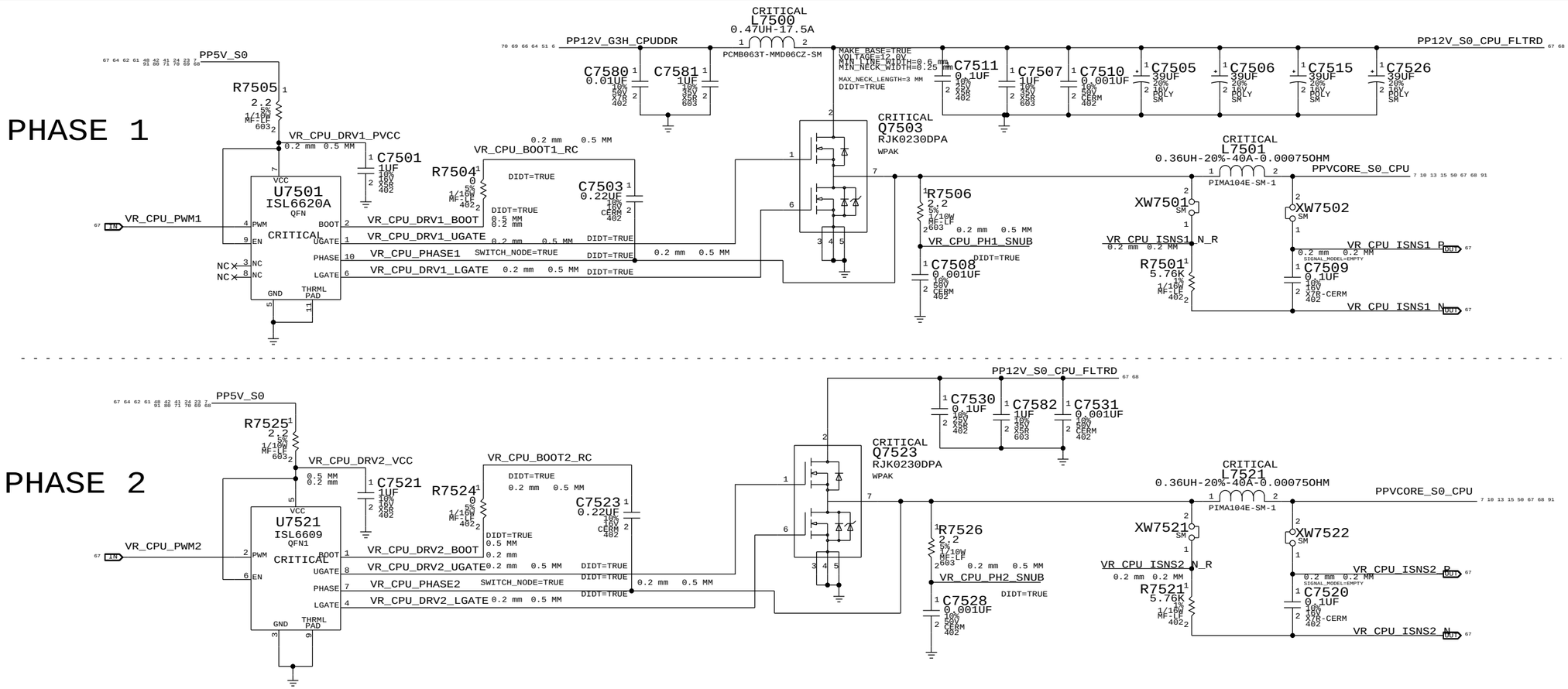

SYNC_MASTER=J40I SYNC_DATE=11/23/2010

PAGE TITLE
VR - CPU VCORE OUTPUT PHASES

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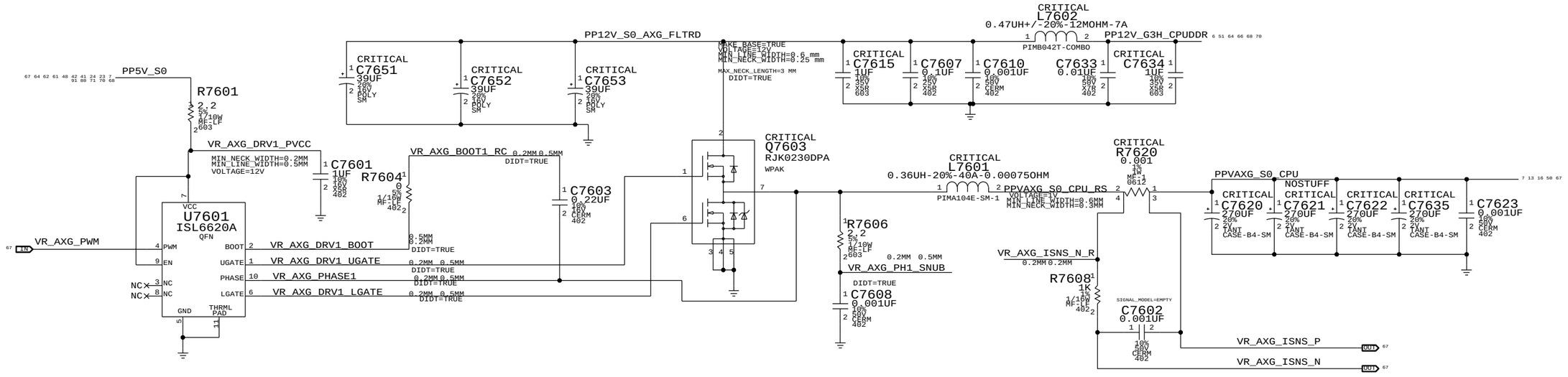
AXG PHASE (22A AVG/33A PEAK, 3.9MOHM LL)



SYNC_MASTER=J40S	SYNC_DATE=12/15/2011
PAGE TITLE	VR - GPU
Apple Inc.	DRAWING NUMBER 051-8768 · SIZE D
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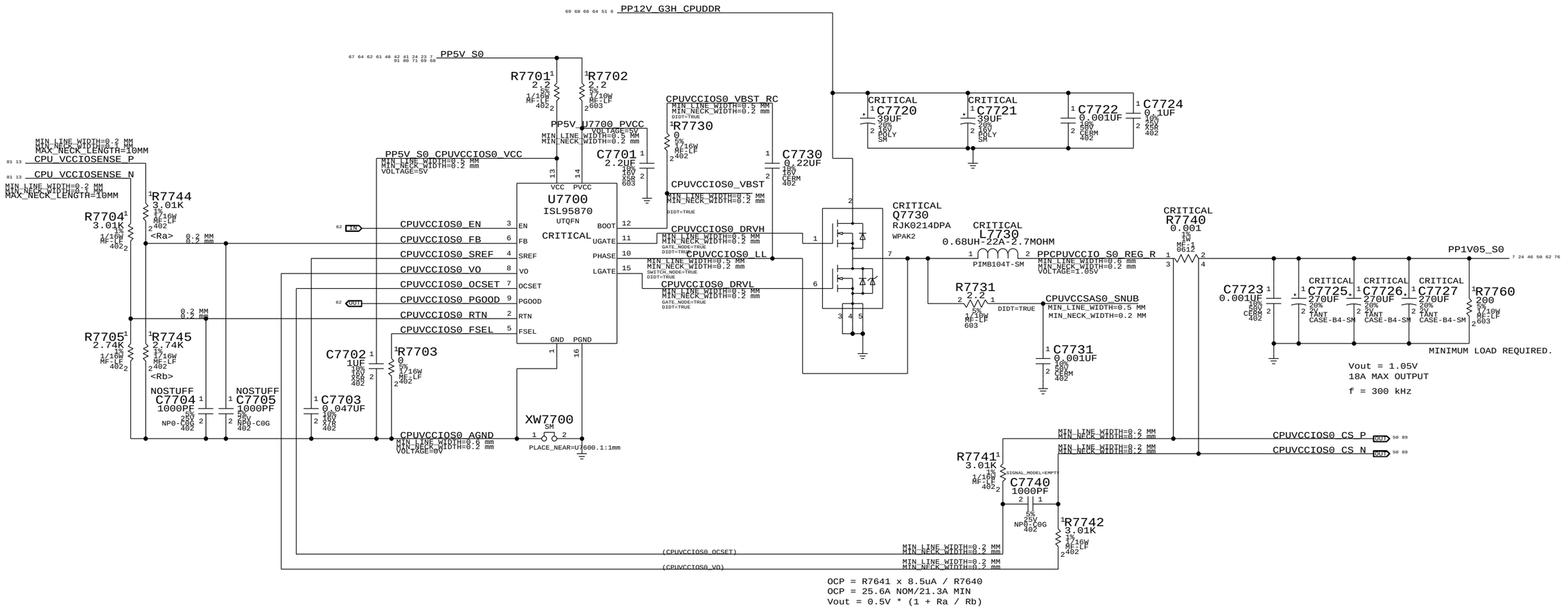
CPU VCCIO (1.05V S0) REGULATOR @ 18A/22A



SYNC_MASTER=J40I	SYNC_DATE=12/02/2010
PAGE TITLE	VR - 1.05V S0
Apple Inc.	DRAWING NUMBER 051-8768 · SIZE D
	REVISION 9.0.0
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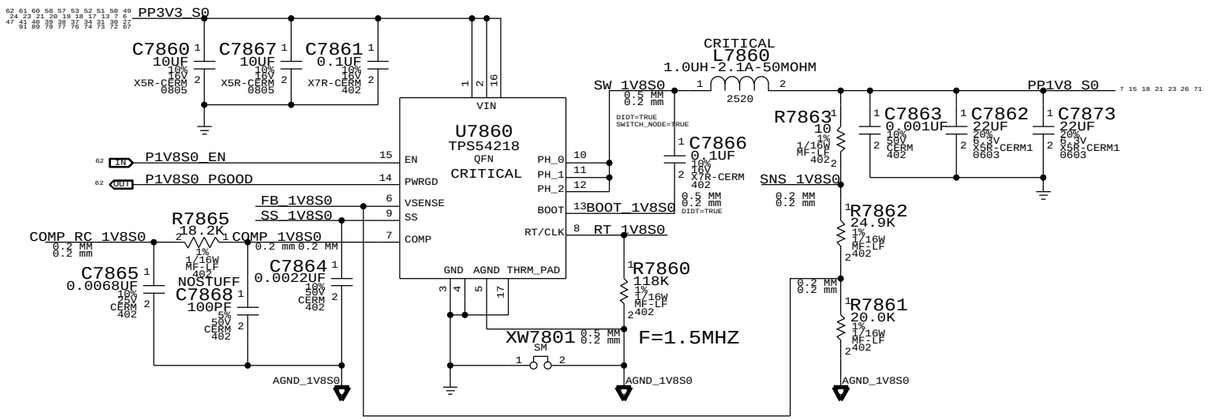
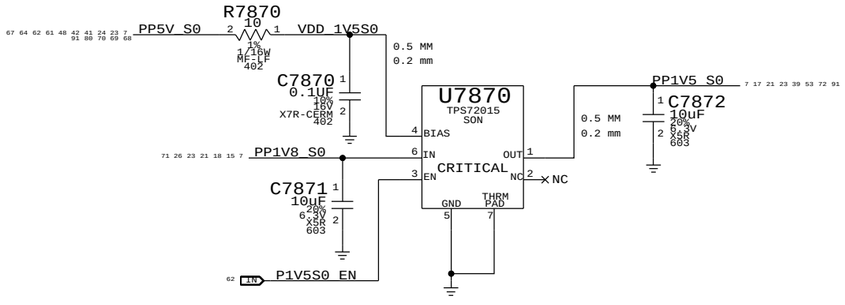
1.8V S0 SWITCHER @ 1.7A/2A



1.5V S0 @ 0.3A/0.5A



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: VR - MISC

Apple Inc.

DRAWING NUMBER: 051-8768 SIZE: D

REVISION: 9.0.0

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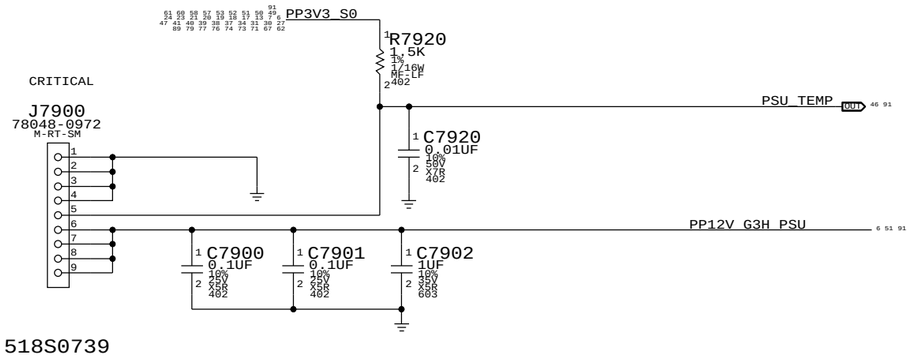
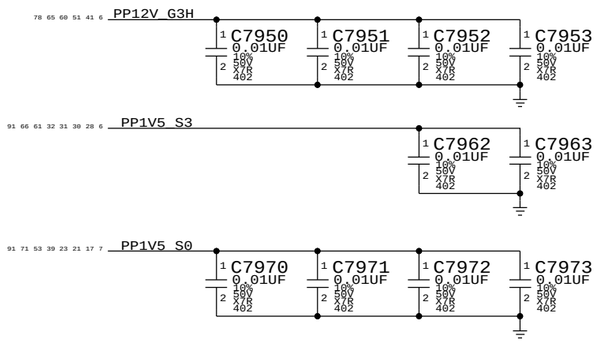


PLACE CAPS AS CLOSE TO J7900 AS POSSIBLE.
BEST IF VIAS ARE AFTER THE CAPS.

SPRINKLE THESE CAPS SOMEWHAT EVENLY AROUND THE PLANES AND ROUTES FOR THESE RAILS.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
PSU CONNECTOR, MISC CAPS

Apple Inc.

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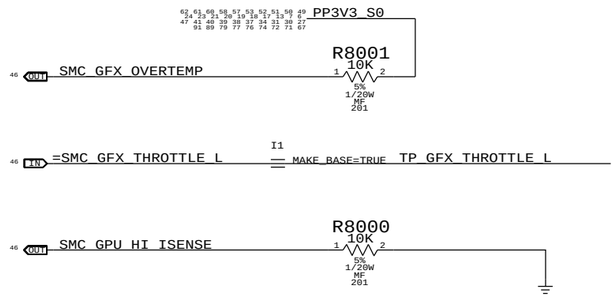

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

NO GPU GLUE

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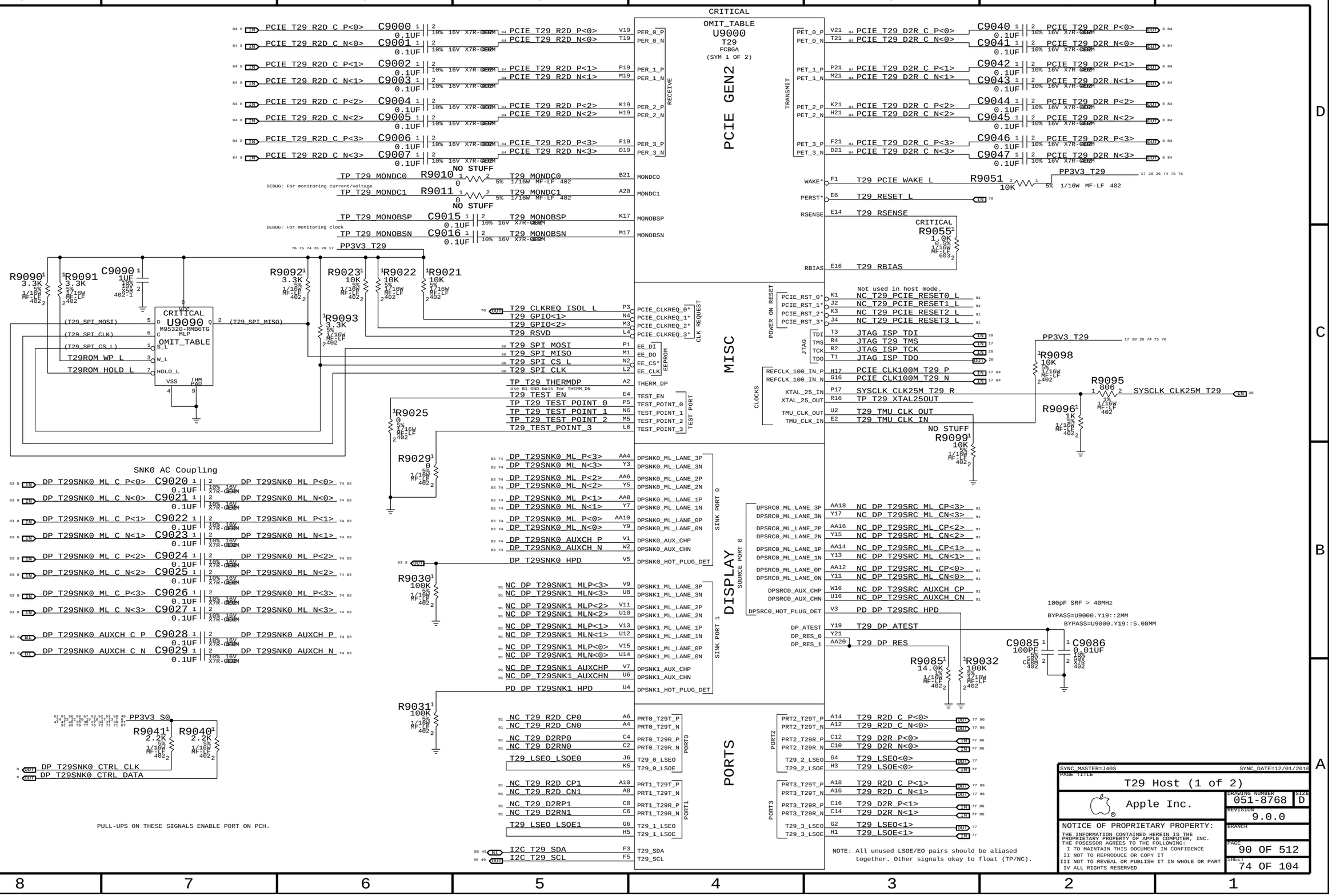
CRITICAL
OMIT_TABLE
U9000
T29
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
MISC
POWER ON RESET
JTAG
CLOCKS
CLK REQUEST
EEPROM
TEST PORT
DISPLAY
SOURCE PORT 0
SINK PORT 0
SINK PORT 1
PORTS
PORT0
PORT1
PORT2
PORT3
PCIE T29 R2D C P<0>
PCIE T29 R2D C N<0>
PCIE T29 R2D C P<1>
PCIE T29 R2D C N<1>
PCIE T29 R2D C P<2>
PCIE T29 R2D C N<2>
PCIE T29 R2D C P<3>
PCIE T29 R2D C N<3>
PCIE T29 R2D P<0>
PCIE T29 R2D N<0>
PCIE T29 R2D P<1>
PCIE T29 R2D N<1>
PCIE T29 R2D P<2>
PCIE T29 R2D N<2>
PCIE T29 R2D P<3>
PCIE T29 R2D N<3>
PCIE T29 D2R C P<0>
PCIE T29 D2R C N<0>
PCIE T29 D2R C P<1>
PCIE T29 D2R C N<1>
PCIE T29 D2R C P<2>
PCIE T29 D2R C N<2>
PCIE T29 D2R C P<3>
PCIE T29 D2R C N<3>
PCIE T29 D2R P<0>
PCIE T29 D2R N<0>
PCIE T29 D2R P<1>
PCIE T29 D2R N<1>
PCIE T29 D2R P<2>
PCIE T29 D2R N<2>
PCIE T29 D2R P<3>
PCIE T29 D2R N<3>
C9000 0.1UF
C9001 0.1UF
C9002 0.1UF
C9003 0.1UF
C9004 0.1UF
C9005 0.1UF
C9006 0.1UF
C9007 0.1UF
C9040 0.1UF
C9041 0.1UF
C9042 0.1UF
C9043 0.1UF
C9044 0.1UF
C9045 0.1UF
C9046 0.1UF
C9047 0.1UF
10% 16V X7R-GEN2M
NO STUFF
R9010 0 5% 1/16W MF-LF 402
R9011 0 5% 1/16W MF-LF 402
TP_T29_MONDC0
TP_T29_MONDC1
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
C9015 0.1UF
C9016 0.1UF
T29_MONOBSP
T29_MONOBSN
MONDC0
MONDC1
MONOBSP
MONOBSN
PP3V3_T29
R9051 10K 5% 1/16W MF-LF 402
T29_PCIE_WAKE_L
T29_RESET_L
T29_RSENSE
T29_RBIAS
R9055 1.0K 0.5% 1/16W MF-LF 603
WAKE*
PERST*
RSENSE
RBIAS
Not used in host mode.
NC_T29_PCIE_RESET0_L
NC_T29_PCIE_RESET1_L
NC_T29_PCIE_RESET2_L
NC_T29_PCIE_RESET3_L
PCIE_RST_0*
PCIE_RST_1*
PCIE_RST_2*
PCIE_RST_3*
T29_JTAG_ISP_TDI
T29_JTAG_ISP_TMS
T29_JTAG_ISP_TCK
T29_JTAG_ISP_TDO
TDI
TMS
TCK
TDO
R9098 10K 5% 1/16W MF-LF 402
R9095 806 1% 1/16W MF-LF 402
R9096 1K 5% 1/16W MF-LF 402
R9099 10K 5% 1/16W MF-LF 402
NO STUFF
PCIE_CLK100M_T29_P
PCIE_CLK100M_T29_N
SYSCLK_CLK25M_T29_R
SYSCLK_CLK25M_T29
T29_TMU_CLK_OUT
T29_TMU_CLK_IN
REFCLK_100_IN_P
REFCLK_100_IN_N
XTAL_25_IN
XTAL_25_OUT
TMU_CLK_OUT
TMU_CLK_IN
R9085 14.0K 1% 1/16W MF-LF 402
R9032 100K 5% 1/16W MF-LF 402
C9085 100PF 5% 50V C0G 402
C9086 0.01UF 10% 25V X7R 402
100pF SRF > 40MHz
BYPASS=U9000.Y19::2MM
BYPASS=U9000.Y19::5.08MM
DP_ATEST
DP_RES_0
DP_RES_1
T29_DP_ATEST
T29_DP_RES
PD_DP_T29SRC_HPD
R9090 3.3K 5% 1/16W MF-LF 402
R9091 3.3K 5% 1/16W MF-LF 402
C9090 1UF 10% 10V X5R 402-1
R9092 3.3K 5% 1/16W MF-LF 402
R9023 10K 5% 1/16W MF-LF 402
R9022 10K 5% 1/16W MF-LF 402
R9021 10K 5% 1/16W MF-LF 402
R9093 3.3K 5% 1/16W MF-LF 402
CRITICAL
U9090
M95320-RMB6TG MLP
OMIT_TABLE
VCC
VSS
THM PAD
(T29_SPI_MOSI)
(T29_SPI_CLK)
(T29_SPI_CS_L)
T29ROM_WP_L
T29ROM_HOLD_L
(T29_SPI_MISO)
S_L
W_L
HOLD_L
T29_CLKREQ_ISOL_L
T29_GPIO<1>
T29_GPIO<2>
T29_RSVD
T29_SPI_MOSI
T29_SPI_MISO
T29_SPI_CS_L
T29_SPI_CLK
PCIE_CLKREQ_0*
PCIE_CLKREQ_1*
PCIE_CLKREQ_2*
PCIE_CLKREQ_3*
EE_DI
EE_DO
EE_CS*
EE_CLK
R9025 0 5% 1/16W MF-LF 402
R9029 0 5% 1/16W MF-LF 402
TP_T29_THERMDP
Use B1 GND ball for THERM_DN
T29_TEST_EN
TP_T29_TEST_POINT_0
TP_T29_TEST_POINT_1
TP_T29_TEST_POINT_2
T29_TEST_POINT_3
THERM_DP
TEST_EN
TEST_POINT_0
TEST_POINT_1
TEST_POINT_2
TEST_POINT_3
SNK0 AC Coupling
DP_T29SNK0_ML_C_P<0>
DP_T29SNK0_ML_C_N<0>
DP_T29SNK0_ML_C_P<1>
DP_T29SNK0_ML_C_N<1>
DP_T29SNK0_ML_C_P<2>
DP_T29SNK0_ML_C_N<2>
DP_T29SNK0_ML_C_P<3>
DP_T29SNK0_ML_C_N<3>
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
C9020 0.1UF
C9021 0.1UF
C9022 0.1UF
C9023 0.1UF
C9024 0.1UF
C9025 0.1UF
C9026 0.1UF
C9027 0.1UF
C9028 0.1UF
C9029 0.1UF
DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_N<3>
DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_N<0>
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DP_T29SNK0_HPD
DPSNK0_ML_LANE_3P
DPSNK0_ML_LANE_3N
DPSNK0_ML_LANE_2P
DPSNK0_ML_LANE_2N
DPSNK0_ML_LANE_1P
DPSNK0_ML_LANE_1N
DPSNK0_ML_LANE_0P
DPSNK0_ML_LANE_0N
DPSNK0_AUX_CHP
DPSNK0_AUX_CHN
DPSNK0_HOT_PLUG_DET
R9030 100K 5% 1/16W MF-LF 402
NC_DP_T29SNK1_MLP<3>
NC_DP_T29SNK1_MLN<3>
NC_DP_T29SNK1_MLP<2>
NC_DP_T29SNK1_MLN<2>
NC_DP_T29SNK1_MLP<1>
NC_DP_T29SNK1_MLN<1>
NC_DP_T29SNK1_MLP<0>
NC_DP_T29SNK1_MLN<0>
NC_DP_T29SNK1_AUXCHP
NC_DP_T29SNK1_AUXCHN
PD_DP_T29SNK1_HPD
DPSNK1_ML_LANE_3P
DPSNK1_ML_LANE_3N
DPSNK1_ML_LANE_2P
DPSNK1_ML_LANE_2N
DPSNK1_ML_LANE_1P
DPSNK1_ML_LANE_1N
DPSNK1_ML_LANE_0P
DPSNK1_ML_LANE_0N
DPSNK1_AUX_CHP
DPSNK1_AUX_CHN
DPSNK1_HOT_PLUG_DET
R9031 100K 5% 1/16W MF-LF 402
DPSRC0_ML_LANE_3P
DPSRC0_ML_LANE_3N
DPSRC0_ML_LANE_2P
DPSRC0_ML_LANE_2N
DPSRC0_ML_LANE_1P
DPSRC0_ML_LANE_1N
DPSRC0_ML_LANE_0P
DPSRC0_ML_LANE_0N
DPSRC0_AUX_CHP
DPSRC0_AUX_CHN
DPSRC0_HOT_PLUG_DET
NC_DP_T29SRC_ML_CP<3>
NC_DP_T29SRC_ML_CN<3>
NC_DP_T29SRC_ML_CP<2>
NC_DP_T29SRC_ML_CN<2>
NC_DP_T29SRC_ML_CP<1>
NC_DP_T29SRC_ML_CN<1>
NC_DP_T29SRC_ML_CP<0>
NC_DP_T29SRC_ML_CN<0>
NC_DP_T29SRC_AUXCH_CP
NC_DP_T29SRC_AUXCH_CN
T29_DP_T29SRC_HPD
NC_T29_R2D_CP0
NC_T29_R2D_CN0
NC_T29_D2RP0
NC_T29_D2RN0
T29_LSEO_LSOE0
PRT0_T29T_P
PRT0_T29T_N
PRT0_T29R_P
PRT0_T29R_N
T29_0_LSEO
T29_0_LSOE
NC_T29_R2D_CP1
NC_T29_R2D_CN1
NC_T29_D2RP1
NC_T29_D2RN1
T29_LSEO_LSOE1
PRT1_T29T_P
PRT1_T29T_N
PRT1_T29R_P
PRT1_T29R_N
T29_1_LSEO
T29_1_LSOE
I2C_T29_SDA
I2C_T29_SCL
T29_SDA
T29_SCL
PRT2_T29T_P
PRT2_T29T_N
PRT2_T29R_P
PRT2_T29R_N
T29_2_LSEO
T29_2_LSOE
T29_R2D_C_P<0>
T29_R2D_C_N<0>
T29_D2R_P<0>
T29_D2R_N<0>
T29_LSEO<0>
T29_LSOE<0>
PRT3_T29T_P
PRT3_T29T_N
PRT3_T29R_P
PRT3_T29R_N
T29_3_LSEO
T29_3_LSOE
T29_R2D_C_P<1>
T29_R2D_C_N<1>
T29_D2R_P<1>
T29_D2R_N<1>
T29_LSEO<1>
T29_LSOE<1>
PP3V3_S0
R9041 2.2K 5% 1/16W MF-LF 402
R9040 2.2K 5% 1/16W MF-LF 402
DP_T29SNK0_CTRL_CLK
DP_T29SNK0_CTRL_DATA
PULL-UPS ON THESE SIGNALS ENABLE PORT ON PCH.
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).
SYNC_MASTER=J40S
SYNC_DATE=12/01/2010
PAGE TITLE
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Apple Inc.
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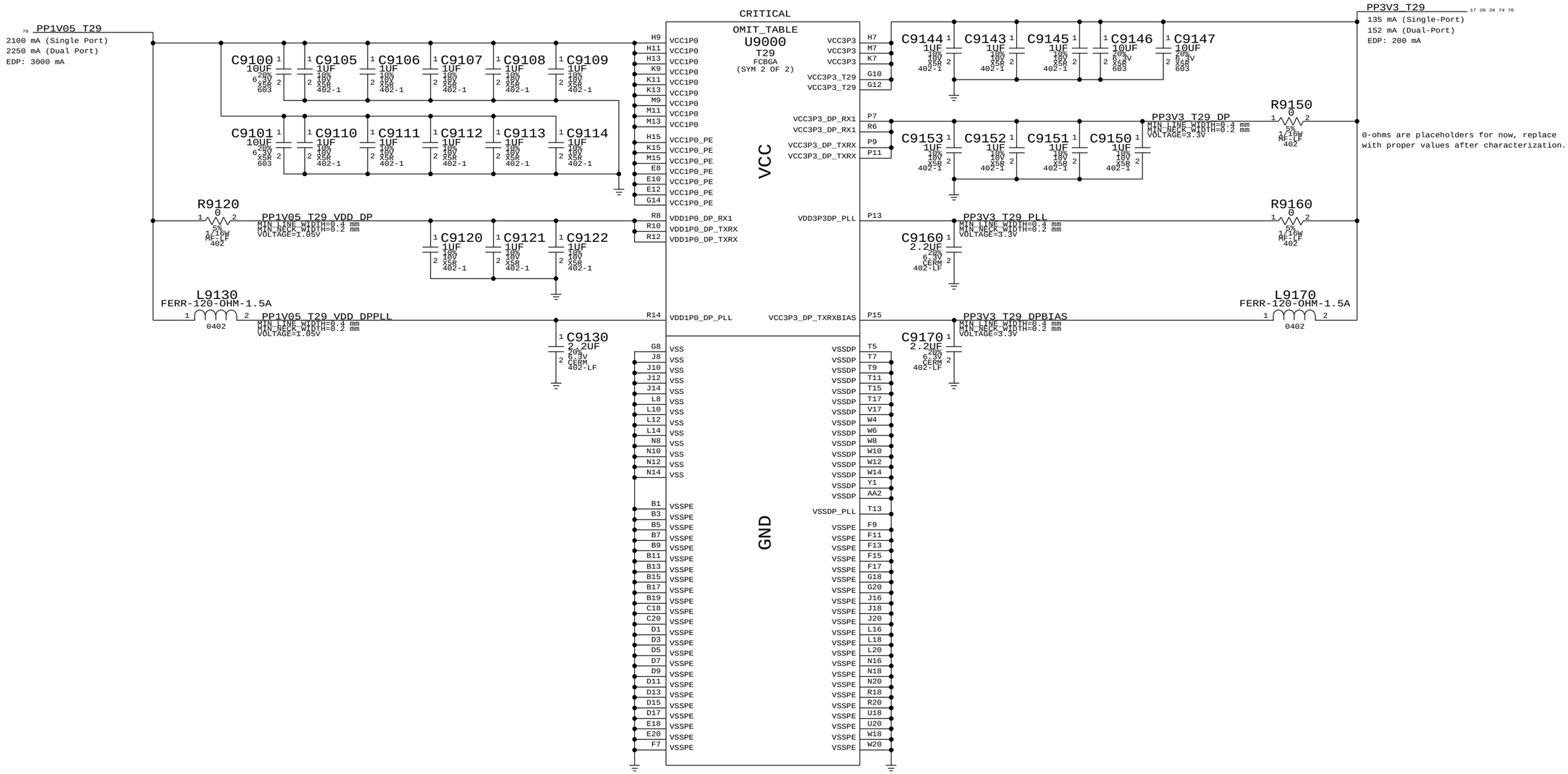

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=J40S SYNC_DATE=11/23/2010

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

SL9202 TH-SP
SL-1.0X0.63-1.4X1.0
SL9203 TH-SP
SL-1.0X0.63-1.4X1.0

OMIT S9200 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9201 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9202 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9203 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9204 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9205 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9206 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9207 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9208 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9209 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9210 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9211 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9212 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9213 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9214 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9215 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9216 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9217 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9218 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9219 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9220 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9221 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9222 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9223 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9224 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9225 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9226 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9227 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9228 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP
OMIT S9229 SM — SHLD-K66-EMI-FRAME-CAN-MAIN-TOP

Supervisor & CLKREQ# Isolation

PP3V3_S0
C9200 0.1UF 10% 25V X5R 402
R9215 10K 5% 1/16W MF-LF 402
Platform (PCIe) Reset
=PLT_RST_T29_GPU
R9203 10K 5% 1/16W MF-LF 402
Open-Drain GPIO
T29_SW_RESET_L
T29_CLKREQ_L
Pull-up provided by SB page.

CRITICAL
U9200 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, MR*, RESET*, EN, OUT (OD), IN, THRM PAD, GND

PP3V3_T29
R9207 100K 5% 1/16W MF-LF 402
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V T29 Switch

Max Current = 1.7A (85C)

PP3V3_S0
C9210 1UF 10% 10V X5R 402-1
U9210 TPS22924 CSP
VIN, VOUT, ON, GND — CRITICAL
PP3V3_T29
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM

1.05V T29 Switch

PP1V05_S0
C9215 1UF 10% 10V X5R 402-1
U9215 TPS22924 CSP
VIN, VOUT, ON, GND — CRITICAL
PP1V05_T29
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM

Max Current = 3.4A (85C)

T29_PWR_EN
R9210 100 5% 1/16W MF-LF 402
U9216 TPS22924 CSP
VIN, VOUT, ON, GND — CRITICAL
T29_PWR_EN_U2916
U3816.A2: PLACE_NEAR=U3815.B2:3 mm
Pull-up provided by SB page.

U9210 & U9215/U9216

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2254	1	FRAME,EMI SHIELD,TB,J40	SH9200	CRITICAL	?

DP/T29 Bias Filters

Prevents high-frequency coupling between 1.5K bias resistors.

DP_A_BIAS
R9231 51 5% 1/20W MF 201 — DP_A_BIAS0P
R9228 51 5% 1/20W MF 201 — DP_A_BIAS0N
C9231 0.01UF 10% 16V X5R-CERM 0201
C9228 0.01UF 10% 16V X5R-CERM 0201
R9230 51 5% 1/20W MF 201 — DP_A_BIAS2P
R9225 51 5% 1/20W MF 201 — DP_A_BIAS2N
C9230 0.01UF 10% 16V X5R-CERM 0201
C9225 0.01UF 10% 16V X5R-CERM 0201

T29_A_BIAS
R9221 51 5% 1/20W MF 201 — T29_A_BIAS0P
R9222 51 5% 1/20W MF 201 — T29_A_BIAS0N
C9221 0.01UF 10% 16V X5R-CERM 0201
C9222 0.01UF 10% 16V X5R-CERM 0201
R9223 51 5% 1/20W MF 201 — T29_A_BIAS1P
R9224 51 5% 1/20W MF 201 — T29_A_BIAS1N
C9223 0.01UF 10% 16V X5R-CERM 0201
C9224 0.01UF 10% 16V X5R-CERM 0201
R9226 51 5% 1/20W MF 201 — T29_A_BIAS2P
R9227 51 5% 1/20W MF 201 — T29_A_BIAS2N
C9226 0.01UF 10% 16V X5R-CERM 0201
C9227 0.01UF 10% 16V X5R-CERM 0201

SYNC_MASTER=J40S SYNC_DATE=11/23/2010

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1UF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1UF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1UF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1UF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1UF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1UF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1UF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1UF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1UF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1UF DP_EXTA_AUXCH_N

PP3V3_S0 R9309 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_P
R9308 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<0>
T29_D2R_P<0>
T29_R2D_C_N<0> L9372 1.0NH+/-0.1NH 0201-1 T29_R2D_C_F_N<0>
T29_R2D_C_P<0> L9373 1.0NH+/-0.1NH 0201-1 T29_R2D_C_F_P<0>
T29_D2R_N<1>
T29_D2R_P<1>
T29_R2D_C_N<1> L9382 1.0NH+/-0.1NH 0201-1 T29_R2D_C_F_N<1>
T29_R2D_C_P<1> L9383 1.0NH+/-0.1NH 0201-1 T29_R2D_C_F_P<1>

OVERSIZE_PAD=0.875 mm^2 (Both L's)

GND_VOID=TRUE (C9370/C9371)
T29_A_BIAS0P VOLTAGE=3.3V
C9370 0.47UF
C9371 0.47UF
T29_A_BIAS0N VOLTAGE=3.3V

(C9372) C9372 0.47UF
(C9373) C9373 0.47UF
T29_A_BIAS2P VOLTAGE=3.3V

GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF
C9381 0.47UF
T29_A_BIAS2N VOLTAGE=3.3V

(C9382) C9382 0.47UF
(C9383) C9383 0.47UF
T29_A_BIAS1N VOLTAGE=3.3V

All 0.47UF: 10% 4V CERM-X5R-1 201

SIGNAL_MODEL=EMPTY
R9372 1.5K 5% 1/20W MF 201
R9373 1.5K 5% 1/20W MF 201
R9382 1.5K 5% 1/20W MF 201
R9383 1.5K 5% 1/20W MF 201
BEAD_PROBE

T29 Path Biasing

D9364 D9372 D9373 D9360 D9382 D9383 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
D9360/D9361: SIGNAL_MODEL=EMPTY
D9382/D9383: SIGNAL_MODEL=T29PIN

T29_D2R_C_P<0> T29_D2R_C_N<0>
T29: TX_0
T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
(D9372/D9373) (D9365.2)
R9374 1.5K R9375 1.5K 5% 1/20W MF 201
T29_D2R_C_P<1> T29_D2R_C_N<1>
T29: TX_1
T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
(D9382/D9383) (D9361.2)
R9384 1.5K R9385 1.5K 5% 1/20W MF 201

DP A Super-Driver

PP3V3_S0
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 10% 16V X7R-CERM 402
C9312 0.1UF 10% 16V X7R-CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NOSTUFF R9311 1K 5% 1/10W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1	IN_D0P	OUT_D0P 30 DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2	IN_D0N	OUT_D0N 29 DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4	IN_D1P	OUT_D1P 28 DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5	IN_D1N	OUT_D1N 27 DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7	IN_D2P	OUT_D2P 25 DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8	IN_D2N	OUT_D2N 24 DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9	IN_D3P	OUT_D3P 23 DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10	IN_D3N	OUT_D3N 22 DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14	IN_SCL	AC_AUXP 20 DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13	IN_SDA	AC_AUXN 19 DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16	IN_AUXP	OUT_AUXP_SCL 18 (DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15	IN_AUXN	OUT_AUXN_SDA 17 (DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3	IN_HPD	(IPD) OUT_HPD 31 (DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26	I2C_CTL_EN (IPU)	
DPSDRVA_I2C_ADDR0	36	I2C_ADDR0 (IPD)	CA_DET 32 DP_A_CA_DET
DPSDRVA_I2C_ADDR1	35	I2C_ADDR1 (IPD)	CEXT 11 DPSDRVA_CEXT
=I2C_DPSDRVA_SCL	38	SCL_CTL	
=I2C_DPSDRVA_SDA	37	SDA_CTL	
DPSDRVA_REXT	12	REXT	
DP_AUXCH_ISOL	39	AUXDDC_OFF (IPD)	
DP_A_PWRDWN_R	34	PD (IPD)	
	6	GND	
	33	THMPAD	

PLACE_NEAR=U9310,11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

DP_EXTA_HPD
R9302 100K 5% 1/16W MF-LF 402
R9319 4.02K 1% 1/16W MF-LF 402
SDRV_PD R9318 0 5% 1/16W MF-LF 402

R9354 30 R9355 30 R9350 30 R9351 30 5% 1/20W MF 201

DP_SDRVA_ML_R_P<0> C9364 0.22UF DP_SDRVA_ML_P<0>
DP_SDRVA_ML_R_N<0> C9365 0.22UF DP_SDRVA_ML_N<0>
DP_SDRVA_ML_R_P<2> C9360 0.22UF DP_SDRVA_ML_P<2>
DP_SDRVA_ML_R_N<2> C9361 0.22UF DP_SDRVA_ML_N<2>
20% 6.3V X5R 0201

R9352 270 5% 1/20W MF 201
R9353 270 5% 1/20W MF 201

C9363 0.1UF C9362 0.1UF C9367 0.1UF C9366 0.1UF C9369 0.1UF C9368 0.1UF
10% 16V X7R-CERM 402

AUXCH Snoop Port, used by PS8301 during training.

Port A MCU

PP3V3_S4 Must be 3.3V DP A port power
C9330 0.1UF C9331 0.1UF 10% 16V X7R-CERM 402

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1	RESET#/PIO0_0	R/PIO1_0/AD1 16 T29DPA_CONFIG1_RC
	2	PIO0_1/CLKOUT	R/PIO1_1/AD2 17 T29DPA_CONFIG2_RC
T29_LSEO<0>	7	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18 T29_A_HV_EN_R
=I2C_T29AMCU_SCL	8	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19 T29_A_UC_ADDR
=I2C_T29AMCU_SDA	9	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20 DP_A_EXT_HPD
T29DPA_HPD	10	PIO0_6/SCK	PIO1_6/RXD 23 T29_A_LSX_P2R
	11	PIO0_7/CTS#	PIO1_7/TXD 24 T29_A_LSX_R2P
T29_LSOE<0>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6 T29_LSEO<1>
T29_LSOE<1>	13	PIO0_9/MOSI/CT16B0_MAT1	
T29_MCU_INT_L	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)	
	15	R/PIO0_11/AD0 (OD)	XTALIN 4
	3	VSS	
	21	THRM PAD	
	25		

I2C Addr: 0x26/0x27 (Wr/Rd)

DP_A_PWRDWN
See Bill C. for layout-specific guidelines for =T29_A_BIAS.
T29_A_BIAS
C9357 0.1UF 10% 16V X7R-CERM 402
=T29_WAKE_L: Desktops use PCIe WAKE# Mobiles use S4 WAKE#
PCIE_WAKE_L
OMIT R9330 0 5% 1/10W MF-LF 402 SWCLK SWDIO
T29_A_UC_ADDR
R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402

R9300 10K R9301 10K 5% 1/16W MF-LF 402
DP_EXTA_DDC_CLK
DP_EXTA_DDC_DATA

R9392 51 R9393 51 5% 1/16W MF-LF 402

R9338 10K 5% 1/16W MF-LF 402
R9334 10K 5% 1/16W MF-LF 402 T29_A_HV_EN

Q9320 SSM3K15FV SOD-VESM-HF
SMC_DP_HPD_L

DP/T29 A Low-Speed MUX

PP3V3_S4 Must be 3.3V DP A port power
C9390 0.1UF C9391 0.1UF 10% 16V X7R-CERM 402
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081A HVQFN

DP_SDRVA_ML_N<3>	31	DIN1_0+	DOUT_0+ 1 T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30	DIN1_0-	DOUT_0- 2 T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27	DIN1_1+	T29: Unused
DP_SDRVA_ML_P<1>	26	DIN1_1-	DOUT_1+ 4 T29DPA_ML_N<1>
DP_SDRVA_AUXCH_P	19	AUX1+	DOUT_1- 5 T29DPA_ML_P<1>
DP_SDRVA_AUXCH_N	18	AUX1-	T29: LSX_A_R2P/P2R (P/N)
DP_SDRVA_HPD	17	HPD_1	AUX+ 6 DP_A_EXT_AUXCH_P
T29_A_RSVD_N	25	DIN2_0+	AUX- 7 DP_A_EXT_AUXCH_N
T29_A_RSVD_P	24	DIN2_0-	T29: RX_1 Bias Sink
(T29_A_LSX_P2R)	23	DIN2_1+	HPD_IN 8 DP_A_EXT_HPD
(T29_A_LSX_R2P)	22	DIN2_1-	
T29_D2R1_BIASP	15	AUX2+	
T29_D2R1_BIASN	14	AUX2-	
	13	HPD_2	
DP_A_PWRDWN	10	GPU_SEL	LO=Port A HI=Port B
T29_A_BIAS	32	AUX_SEL	
	11	NC	
	29	VDD	
	20		
	16		
	12		
	9		
	3		
	28	THMPAD GND	
	33		
	21		

OMIT_TABLE
CKPLUS_WAIVE=NdifPr_badTerm
R9396 1K R9397 1K 5% 1/16W MF-LF 402
R9398 100K 5% 1/16W MF-LF 402
SIGNAL_MODEL=T29DP_MUX

CBTL04DP081A (353S3312) AND PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

DP Path Biasing
R9361 1.5K DP_A_BIAS2N VOLTAGE=3.3V
R9360 1.5K DP_A_BIAS2P VOLTAGE=3.3V
R9365 1.5K DP_A_BIAS0N VOLTAGE=3.3V
R9364 1.5K DP_A_BIAS0P VOLTAGE=3.3V
SIGNAL_MODEL=EMPTY 5% 1/20W MF 201

CRITICAL U9359 74LVCIG04DBDCK SC70
DP_A_PWRDWN DP_A_BIAS
C9358 0.1UF 10% 16V X7R-CERM 402

See Bill C. for layout-specific guidelines for DP_A_BIAS.

IC supports input high while Vcc = 0V.

P2R = Plug to Receptacle
R2P = Receptacle to Plug

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

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3V3(DP)/2V9(T29) PORTA SUPPLY

PP5V_S4
R9431 1.0 5% 1/4W MF-LF 1206
R9432 1.0 5% 1/4W MF-LF 1206
VRT29_VIN
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 mm
C9420 10UF 10% 10V X5R-CERM 0805
CRITICAL
U9401 ISL80101B DFN
VIN, VOUT, ENABLE, SS, ISET, ADJ, PG, GND, THRM PAD
T29_DP_A_PWR_EN
3V3R2V8_SS_A
3V3R2V8_DPAPWR_ADJ
80101A NC
C9421 0.022UF 10% 16V CERM-X5R 402
R9430 25.5K 1/16W 1% MF-LF 402
PM_PGOOD_P3V3_2V8_A
PP3V3R2V8_DPAPWR_D
CRITICAL
D9401 POWERDI-123 DFLS260
PP3V3R12V_SW_DPAPWR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
C9422 10UF 10% 16V X5R-CERM 0805
R9421 20K 1/16W 5% MF-LF 402
C9423 330PF 5% 50V 2 402 COG
R9424 11.5K 1/16W 1% MF-LF 402 <RA>
C9424 10UF 10% 16V X5R 805
C9425 10UF 10% 16V X5R 805
R9450 2.2K 5% 1/10W MF-LF 603
PP5V_S4
R9422 100K 1/16W 5% MF-LF 402
R9423 2.05K 1/16W 1% MF-LF 402 <RB2>
R9425 15.0K 1/16W 1% MF-LF 402 NOSTUFF <RB1>
DP_A_PWRDWN_INV
VO=0.5*(1+ RA/RB)
VO=0.5*(1+ 1.18K/249)=2.87V
PP3V3_S4
R9426 10K 5% 1/16W MF-LF 402
DP_A_PWRDWN_FET_R
Q9420 2N7002DW-X-G SOT-363
T29_A_BIAS
LO: 3V3 FOR DP
HI: 2V8 FOR T29
PP3V3_S5
C9450 0.1UF 10% 50V X5R 603-1
T29_DP_PORTA_PWR_EN
PM_P5V_S4_PG
U9420 MC74VHC1G08 SC70-5
T29_DP_A_PWR_EN
L9400 FERR-120-OHM-3A 0603
PP3V3R12V_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=12V
PP3V3R12V_SW_DPAPWR_F
C9400 0.01UF 10% 16V X5R-CERM 0201

12V T29 PORTA SUPPLY

12 VOLTS
12 WATTS MAX PER PORT

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

CRITICAL (*) U9410 tolerance unknown

PP12V_G3H
R9416 15.0K 1% 1/10W MF-LF 402
C9410 0.1UF 10% 50V X7R 603-1
CRITICAL
U9410 SN1010017 QFN
VIN, VOUT, EN* (PU-Weak!), RTRY*, CT, FLT*, ILIM, IFLT, GND, THRM PAD
C9411 0.1UF 10% 16V X5R 603-1
P12V_T29
CRITICAL
D9410 DSN2 NSR20F20NXXXG
PP3V3R12V_SW_DPAPWR
R9418 0 5% 1/10W MF-LF 603
DPAPWRSW_HVEN_L_R
TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT
DPAPWRSW_CT
R9412 0 5% 1/16W MF-LF 402 <CT>
CRITICAL
D9403 MMBZ5227BLT1H SOT23
NOSTUFF
R9417 13K 5% 1/16W MF-LF 402
R9410 100K 1% 1/16W MF-LF 402 <RFLT>
R9411 174K 1% 1/16W MF-LF 402 <RLIM>
IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000
Q9415 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN

DisplayPort/T29 A Connector

GND_DPACONN_1 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
C9405 0.1UF 10% 6.3V X5R 201
GND_DPACONN_7 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
C9406 0.1UF 10% 6.3V X5R 201
GND_DPACONN_13 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
GND_DPACONN_19 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
L9408 FERR-120-OHM-3A 0603
R9408 12 5% 1/20W MF 201
DP Dir / T29 Dir
T29DPA_ML_P<0> / T29DPA_ML_N<0>
T29DPA_ML_P<1> / T29DPA_ML_N<1>
T29DPA_ML_P<2> / T29DPA_ML_N<2>
GND_VOID=TRUE (Both C's)
C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
T29: TX_0
T29: LSE0
T29: LSOE
T29: TX_1
470k R's for ESD protection on AC-coupled signals.

T29: RX_0
T29_D2R_C_P<0>
T29_D2R_C_N<0>
R9494 1K 1% 1/20W MF 201
R9495 1K 1% 1/20W MF 201
T29: Unused
T29DPA_ML_P<3>
T29DPA_ML_N<3>
T29_A_BIAS1P
T29_A_BIAS1N
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
T29_D2R_C_P<1>
T29_D2R_C_N<1>
T29: RX_1
CRITICAL
L9498 650NH-5%-0.430MA-0.052OHM 0603
L9499 650NH-5%-0.430MA-0.052OHM 0603
T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N
DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N
C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
R9402 12 5% 1/20W MF 201
T29DPA_HPD_R
C9402 0.01UF 10% 16V X5R-CERM 0201
R9441 100K 5% 1/20W MF 201
DPACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
R9401 12 5% 1/20W MF 201
C9401 0.01UF 10% 16V X5R-CERM 0201
T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 201
C9495 330PF 10% 16V X7R 201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

For J9400 T29 SMT pads (3, 5, 17 & 19):

J9400 MINIDSPLYPRT-PL-J40 F-RT-TH CRITICAL
BOT ROW TH PINS: DP_HPD, CONFIG1, CONFIG2, GND, ML_LANE3P, ML_LANE3N, GND, AUX_CHP, AUX_CHN, DP_PWR
TOP ROW SM PINS: GND, ML_LANE0P, ML_LANE0N, GND, ML_LANE1P, ML_LANE1N, GND, ML_LANE2P, ML_LANE2N, RETURN
SHIELD PINS
514-0783

SYNC_MASTER=J40S	SYNC_DATE=12/01/2010
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ONE 0.1UF AND ONE 0.01UF CAP PER POWER PIN.

PP3V3_S0

C9740 0.1UF 10% 16V X7R-CERM 402
C9741 0.01UF 10% 50V X7R 402
C9742 0.1UF 10% 16V X7R-CERM 402
C9743 0.01UF 10% 50V X7R 402
C9744 0.1UF 10% 16V X7R-CERM 402
C9745 0.01UF 10% 50V X7R 402
C9746 0.1UF 10% 16V X7R-CERM 402
C9747 0.01UF 10% 50V X7R 402
C9748 0.1UF 10% 16V X7R-CERM 402
C9749 0.01UF 10% 50V X7R 402
C9750 0.1UF 10% 16V X7R-CERM 402
C9751 0.01UF 10% 50V X7R 402

PLACE DP CAPS NEXT TO U9740

ALL CHANNELS ARE EQUIVALENT.
LANE SWAPPING AND POLARITY REVERSAL ARE ALLOWED.

HDMI_CLK_C_P → C9711 0.1UF 10% 16V X7R-CERM 402 → HDMI_CLK_LS_P
HDMI_CLK_C_N → C9710 0.1UF 10% 16V X7R-CERM 402 → HDMI_CLK_LS_N
HDMI_DATA_C_P<0> → C9713 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_P<0>
HDMI_DATA_C_N<0> → C9712 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_N<0>
HDMI_DATA_C_P<1> → C9715 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_P<1>
HDMI_DATA_C_N<1> → C9714 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_N<1>
HDMI_DATA_C_P<2> → C9717 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_P<2>
HDMI_DATA_C_N<2> → C9716 0.1UF 10% 16V X7R-CERM 402 → HDMI_DATA_LS_N<2>

U9740
PS8171
QFN
CRITICAL

VCC: 2, 15, 21, 26, 40, 46

IN_D1+	39	OUT_D1+	22
IN_D1-	38	OUT_D1-	23
IN_D2+	42	OUT_D2+	19
IN_D2-	41	OUT_D2-	20
IN_D3+	45	OUT_D3+	16
IN_D3-	44	OUT_D3-	17
IN_D4+	48	OUT_D4+	13
IN_D4-	47	OUT_D4-	14
HPDX	7	HPD_SINK	30
PIO	4		
SCL	9	SCL_SINK	28
SDA	8	SDA_SINK	29
DDC_EN	32		
DDCBUF	34		
PEQ	3		
APD	11		
RSV_1	12		
RSV_0	1		
REXT	6		
CEXT	10		
PRE	35		
OE*	25		
EMI1	33		
EMI0	27		
GND	5, 18, 24, 31, 36, 37, 43		
THRM PAD	49		

HDMI_CLK_P
HDMI_CLK_N
HDMI_DATA_P<0>
HDMI_DATA_N<0>
HDMI_DATA_P<1>
HDMI_DATA_N<1>
HDMI_DATA_P<2>
HDMI_DATA_N<2>
HDMI_HPD
HDMI_DDC_CLK_5V
HDMI_DDC_DATA_5V

HDMI_LS_HPD
HDMI_LS_SCL
HDMI_LS_SDA
PP3V3_S0

R9753 4.7K 5% 1/16W MF-LF 402
R9755 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R9757 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R9759 4.7K 5% 1/16W MF-LF 402
R9761 4.7K 5% 1/16W MF-LF 402

HDMI_LS_PIO
HDMI_LS_DDC_EN
HDMI_LS_DDCBUF
HDMI_LS_PEQ
HDMI_LS_APD
PU_HDMI_LS_RSV1

R9750 4.7K 5% 1/16W MF-LF 402
R9754 4.7K 5% 1/16W MF-LF 402
R9756 4.7K 5% 1/16W MF-LF 402
R9758 4.7K 5% 1/16W MF-LF 402 NOSTUFF

PD_HDMI_LS_RSV0

R9740 4.7K 5% 1/16W MF-LF 402
R9741 470 1% 1/16W MF-LF 402
C9760 2.2UF 20% 6.3V CERM 402-LF

HDMI_LS_REXT
HDMI_LS_CEXT

R9763 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R9765 4.7K 5% 1/16W MF-LF 402
R9769 4.7K 5% 1/16W MF-LF 402

HDMI_LS_PRE
HDMI_LS_OE_L
HDMI_LS_EMI1
HDMI_LS_EMI0

R9762 4.7K 5% 1/16W MF-LF 402
R9764 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R9766 4.7K 5% 1/16W MF-LF 402
R9768 4.7K 5% 1/16W MF-LF 402

PP3V3_S0
R9725 10K 5% 1/16W MF-LF 402
R9724 10K 5% 1/16W MF-LF 402
HDMI_LS_SCL
HDMI_LS_SDA

HDMI_LS_HPD
R9726 100K 5% 1/16W MF-LF 402

PIO - HPD INPUT
HIGH INVERT HPD_SINK
LOW NO INVERSION

PEQ - INPUT EQ
HIGH HIGH EQ
MID LOW EQ
LOW MID EQ

APD - AUTOMATIC POWER DOWN
AUTO-POWER-DOWN WHEN HPD_SINK IS LOW.
HIGH ENABLE
MID (RESERVED)
LOW DISABLE

DDCBUF - DDC LEVEL SHIFTER TYPE
HIGH ACTIVE
LOW PASSIVE

EMI0 - EMI FILTER ENABLE 0
HIGH MIDDLE RISE/FALL TIME
MID LARGE RISE/FALL TIME
LOW SMALL RISE/FALL TIME

EMI1 - EMI FILTER ENABLE 1
HIGH NO EFFECT
MID (RESERVED)
LOW EMI FILTER ENABLE

PRE - PRE-EMPHASIS
HIGH LOW PRE-EMPHASIS
MID HIGH PRE-EMPHASIS
LOW NO PRE-EMPHASIS

OE* - OUTPUT ENABLE.
HIGH DISABLE TMDS DRIVERS
LOW ENABLE TMDS DRIVERS

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

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HDMI CONNECTOR

PLACE NEAR J9430 CONNECTOR

CRITICAL L9890 90-OHM-300MA ACM2012H SYM_VER-2
HDMI_DATA_P<0> → HDMI_DATA_CONN_P<0>
HDMI_DATA_N<0> → HDMI_DATA_CONN_N<0>

CRITICAL D9811 RCLAMP0524P SLP2510P8
CRITICAL D9810 RCLAMP0524P SLP2510P8

CRITICAL L9891 90-OHM-300MA ACM2012H SYM_VER-2
HDMI_DATA_P<1> → HDMI_DATA_CONN_P<1>
HDMI_DATA_N<1> → HDMI_DATA_CONN_N<1>

CRITICAL L9892 90-OHM-300MA ACM2012H SYM_VER-2
HDMI_DATA_P<2> → HDMI_DATA_CONN_P<2>
HDMI_DATA_N<2> → HDMI_DATA_CONN_N<2>

CRITICAL D9810 RCLAMP0524P SLP2510P8
CRITICAL D9811 RCLAMP0524P SLP2510P8

CRITICAL L9893 360-OHM-0.100MA ACM2012-SM SYM_VER-2
HDMI_CLK_P → HDMI_CLK_CONN_P
HDMI_CLK_N → HDMI_CLK_CONN_N

(0.055A TO 0.5A LIMITS PER HDMI SPEC.)

PP5V_S0 → C9800 22UF 20% 6.3V X5R-CERM 0603
C9802 0.1UF 10% 16V X7R-CERM 402

CRITICAL U9800 TPS2051B SOT23
IN ← PP5V_S0
EN ← NC_HD_OC (NO_TEST=TRUE)
OUT → PP5V_HDMI_DDC_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM)
OC* → NC_HD_OC
GND

C9803 10UF 20% 6.3V X5R 603

CRITICAL L9830 400-OHM-EMI (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM) SM-1
C9830 0.01UF 20% 50V CERM 603

J9830 HDMI-PLASTIC-J40 F-RT-SM

HDMI_DATA_CONN_P<2>	TMDS_DATA2_P	TMDS_DATA2_SHLD1	HDMI_DATA_CONN_P<1>
HDMI_DATA_CONN_N<2>	TMDS_DATA2_M	TMDS_DATA1_P	HDMI_DATA_CONN_N<1>
	TMDS_DATA1_SHLD1	TMDS_DATA1_M	
HDMI_DATA_CONN_P<0>	TMDS_DATA0_P	TMDS_DATA0_SHLD1	
HDMI_DATA_CONN_N<0>	TMDS_DATA0_M	TMDS_CLK_P	HDMI_CLK_CONN_P
	TMDS_CLK_SHLD	TMDS_CLK_M	HDMI_CLK_CONN_N
TP_HDMI_CEC_CONN	CEC	RSRVD	
HDMI_DDC_CLK_CONN	SCL	SDA	HDMI_DDC_DATA_CONN
	DDC_CED_GND	P_5V_PWR	PP5V_HDMI_DDC_CONN
HDMI_HPD_CONN	HOT_PLUG_DETECT		

CRITICAL SHLD PINS

CRITICAL D9800 RCLAMP0504F SC70-6-1
PP5V_HDMI_DDC_CONN

PLACE CAPS CLOSE TO HDMI CONNECTOR

PP5V_HDMI_DDC_FUSE
R9810 4.7K 5% 1/10W MF-LF 402
R9812 4.7K 5% 1/10W MF-LF 402
C9810 0.01UF 10% 50V X7R 402

HDMI_DDC_CLK_CONN → CRITICAL L9810 FERR-220-OHM 0402 → HDMI_DDC_CLK_F → R9811 33 5% 1/10W MF-LF 402 → HDMI_DDC_CLK_5V
C9811 22PF 5% 50V CERM 402

HDMI_DDC_DATA_CONN → CRITICAL L9811 FERR-220-OHM 0402 → HDMI_DDC_DATA_F → R9813 33 5% 1/10W MF-LF 402 → HDMI_DDC_DATA_5V
C9813 22PF 5% 50V CERM 402

HDMI_HPD_CONN → CRITICAL L9841 FERR-220-OHM 0402 → HDMI_HPD_Q → R9814 10K 5% 1/10W MF-LF 402 → HDMI_HPD
C9814 220PF 10% 50V X7R-CERM 402

100K PULL-DOWN IS BUILT INTO LEVEL SHIFTER.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: HR PDG section 4.1.9, PDDG section 2.5.1

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	8 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	8 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	8 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	8 18
	CPU_50S	CPU_AGTL	FDI_INT	8 18
	CPU_50S	CPU_VID	CPU_VCCSA_VID<1>	13 64
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 67
	CPU_50S	CPU_VID	CPU_VIDALERT_L_R	13
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 67
	CPU_50S	CPU_VID	CPU_VIDSCLK_R	13
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 67
	CPU_50S	CPU_VID	CPU_VIDSOUT_R	13
CPU_PECI	CPU_50S	PCIE	CPU_PECI	11 20 46
	CPU_50S	PCIE	CPU_PECI_R	46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 28
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	10 24
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	10
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	6 11
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 18
	CPU_50S	CPU_AGTL	CPU_VTTSELECT	
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 47 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 67
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	

PEG CLOCK ON PP103 WITH PCIE CONSTRAINTS.

XDP Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
	CPU_50S	CPU_ITP	XDP_CPURST_L	24
CPU_CFG	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	24
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
	CPU_50S	CPU_ITP	XDP_PCH_TCK	17 24
	CPU_50S	CPU_ITP	XDP_PCH_TDI	17 24
	CPU_50S	CPU_ITP	XDP_PCH_TDO	17 24
	CPU_50S	CPU_ITP	XDP_PCH_TMS	17 24
	CPU_50S	CPU_ITP	XDP_TDI	24
	CPU_50S	CPU_ITP	XDP_TDO	24
	CPU_50S	CPU_ITP	XDP_TMS	24
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 27
	CPU_50S	CPU_ITP	XDP_PRESENT_L	24
	CPU_50S	CPU_ITP	XDP_RES_RL	24
	CPU_50S	CPU_ITP	XDP_CPU_PWRBTN_L	24
	CPU_50S	CPU_ITP	XDP_VR_READY	24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2
SOURCE: HR PDG, Section 4.1.9

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK	MEM_85D	MEM_CLK	MEM_A_CLK_P<5..0> 12 30
MEM_A_CLK	MEM_85D	MEM_CLK	MEM_A_CLK_N<5..0> 12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CKE<3..0> 12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CS_L<3..0> 12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_ODT<3..0> 12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 12 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 12 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 12 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 12 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 12 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 12 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 12 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 12 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 12 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 12 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 12 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 12 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 12 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 12 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 12 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 12 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 12 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 12 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 12 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 12 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 12 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 12 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 12 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 12 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 12 29
MEM_B_CLK	MEM_85D	MEM_CLK	MEM_B_CLK_P<5..0> 12 31
MEM_B_CLK	MEM_85D	MEM_CLK	MEM_B_CLK_N<5..0> 12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CKE<3..0> 12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CS_L<3..0> 12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_ODT<3..0> 12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 12 31
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 12 29

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: Memory Constraints

Apple Inc.

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
DP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?
TMDS	*	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
TMDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PDG, TABLES 191,193, Radeon TRM section 7.7.1
PER ANIL: MODIFIED DP CONNECTOR NEEDS 90 OHMS. MEASURE PROTO BOARD AND ADJUST IF NEEDED.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_CONN_N 42 91
	SATA_90D	SATA	SATA_HDD1_D2R_CONN_P 42 91
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_N 17 42
	SATA_90D	SATA	SATA_HDD1_D2R_P 17 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_CONN_N 42 91
	SATA_90D	SATA	SATA_HDD1_R2D_CONN_P 42 91
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_C_N 17 42
	SATA_90D	SATA	SATA_HDD1_R2D_C_P 17 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_CONN_N 42 91
	SATA_90D	SATA	SATA_HDD2_D2R_CONN_P 42 91
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_N 17 42
	SATA_90D	SATA	SATA_HDD2_D2R_P 17 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_CONN_N 42 91
	SATA_90D	SATA	SATA_HDD2_R2D_CONN_P 42 91
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_C_N 17 42
	SATA_90D	SATA	SATA_HDD2_R2D_C_P 17 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_DF_N 42
	SATA_90D	SATA	SATA_HDD1_D2R_DF_P 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_DF_N 42
	SATA_90D	SATA	SATA_HDD1_R2D_DF_P 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_DF_N 42
	SATA_90D	SATA	SATA_HDD2_D2R_DF_P 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_DF_N 42
	SATA_90D	SATA	SATA_HDD2_R2D_DF_P 42
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 17
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 19
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_N 19 25
	USB_85D	USB	USB_HUB1_UP_P 19 25
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_N 19 25
	USB_85D	USB	USB_HUB2_UP_P 19 25
USB_EXTA	USB_85D	USB	USB_EXTA_N 25 43
	USB_85D	USB	USB_EXTA_P 25 43
USB_EXTB	USB_85D	USB	USB_EXTB_N 25 43
	USB_85D	USB	USB_EXTB_P 25 43
USB_EXTC	USB_85D	USB	USB_EXTC_N 25 43
	USB_85D	USB	USB_EXTC_P 25 43
USB_EXTD	USB_85D	USB	USB_EXTD_N 25 43
	USB_85D	USB	USB_EXTD_P 25 43
	USB_85D	USB	USB_PORT0_N 43
	USB_85D	USB	USB_PORT0_P 43
	USB_85D	USB	USB_PORT1_N 43
	USB_85D	USB	USB_PORT1_P 43
	USB_85D	USB	USB_PORT2_N 43
	USB_85D	USB	USB_PORT2_P 43
	USB_85D	USB	USB_PORT3_N 43
	USB_85D	USB	USB_PORT3_P 43
USB_IR	USB_85D	USB	USB_IR_N 25 44
	USB_85D	USB	USB_IR_P 25 44
	USB_85D	USB	USB_IR_R_N 44
	USB_85D	USB	USB_IR_R_P 44
USB_BT	USB_85D	USB	USB_BT_N 25 35
	USB_85D	USB	USB_BT_P 25 35
	USB_85D	USB	USB_BT_CONN_N 35 91
	USB_85D	USB	USB_BT_CONN_P 35 91
	USB_85D	USB	USB_B_MUXED_N 43
	USB_85D	USB	USB_B_MUXED_P 43

DP Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_AUX_CH_CK_N	
	DP_90D	DISPLAYPORT	DP_AUX_CH_CK_P	
	DP_90D	DISPLAYPORT	DP_AUX_CH_C_N	
	DP_90D	DISPLAYPORT	DP_AUX_CH_C_P	
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_N	77 78 86
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_P	77 78 86
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 77
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 77
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_N	77
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_P	77
	DP_90D	DISPLAYPORT	DP_EXTA_DDC_CLK_AUX_P	Manual Diff Pair
	DP_90D	DISPLAYPORT	DP_EXTA_DDC_DATA_AUX_N	Manual Diff Pair
	DP_55S	DISPLAYPORT	DP_EXTA_DDC_CLK	8 77
	DP_55S	DISPLAYPORT	DP_EXTA_DDC_DATA	8 77
	DP_55S	DISPLAYPORT	DP_EXTA_HPD	8 77
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 74
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 74
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	74
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	74
	DP_90D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 77
	DP_90D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 77
	DP_90D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	77
	DP_90D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	77
	DP_90D	DISPLAYPORT	DP_ML_CK_N<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_CK_P<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_C_N<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_C_P<3..0>	
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 74
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 74
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	74
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	74
	DP_55S	DISPLAYPORT	DP_T29SNK0_DDC_CLK	
	DP_55S	DISPLAYPORT	DP_T29SNK0_DDC_DATA	
	DP_55S	DISPLAYPORT	DP_T29SNK0_HPD	8 74
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	
	DP_55S	DISPLAYPORT	DP_T29SNK1_HPD	

HDMI Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	TMDS_100D	TMDS	HDMI_CLK_CONN_N 80
	TMDS_100D	TMDS	HDMI_CLK_CONN_P 80
	TMDS_85D	TMDS	HDMI_CLK_C_N 8 79
	TMDS_85D	TMDS	HDMI_CLK_C_P 8 79
	TMDS_85D	TMDS	HDMI_CLK_LS_N 79
	TMDS_85D	TMDS	HDMI_CLK_LS_P 79
	TMDS_100D	TMDS	HDMI_CLK_N 79 80
	TMDS_100D	TMDS	HDMI_CLK_P 79 80
	TMDS_100D	TMDS	HDMI_DATA_CONN_N<2..0> 80
	TMDS_100D	TMDS	HDMI_DATA_CONN_P<2..0> 80
	TMDS_85D	TMDS	HDMI_DATA_C_N<2..0> 8 79
	TMDS_85D	TMDS	HDMI_DATA_C_P<2..0> 8 79
	TMDS_85D	TMDS	HDMI_DATA_LS_N<2..0> 79
	TMDS_85D	TMDS	HDMI_DATA_LS_P<2..0> 79
	TMDS_100D	TMDS	HDMI_DATA_N<2..0> 79 80
	TMDS_100D	TMDS	HDMI_DATA_P<2..0> 79 80
	TMDS_55S	TMDS	HDMI_LS_SCL 8 79
	TMDS_55S	TMDS	HDMI_LS_SDA 8 79
	TMDS_55S	TMDS	HDMI_LS_HPD 8 79

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	17 46 48
	LPC_50S	LPC	LPC_R_AD<3..0>	17
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	17 46 48
	LPC_50S	LPC	LPC_FRAME_R_L	17
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	27 48
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 46
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 48
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	19 27
	SMB_50S	SMB	SMB_PCH_STR_SCL	49
	SMB_50S	SMB	SMB_PCH_STR_SDA	49
	SMB_50S	SMB	SMB_PCH_DIMM_SCL	49
	SMB_50S	SMB	SMB_PCH_DIMM_SDA	49
	SMB_50S	SMB	SMB_PCH_MKY_SCL	49
	SMB_50S	SMB	SMB_PCH_MKY_SDA	49
	SMB_50S	SMB	SMB_PCH_VRF_SCL	49
	SMB_50S	SMB	SMB_PCH_VRF_SDA	49
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 49
	SMB_50S	SMB	SMBUS_PCH_DATA	17 49
SMBUS_PCH_0_CLK	SMB_50S	SMB	SMB_PCH_XDP_SCL	49
	SMB_50S	SMB	SMB_PCH_XDP_SDA	49
	SMB_50S	SMB	SML_PCH_1_CLK	17 49
	SMB_50S	SMB	SML_PCH_1_DATA	17 49
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 48
	SPI_55S	SPI	SPI_CLK	48 91
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 48
	SPI_55S	SPI	SPI_MOSI	48 91
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 48 91
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 48
	SPI_55S	SPI	SPI_CS0_L	48 91
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 53
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 53
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 53
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 53
	HDA_50S	HDA	AUD_SDI_R	53
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 53
	HDA_50S	HDA	HDA_SDOUT_R	17

T26B	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
T26A	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
T26D	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17
T26C	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
T26H	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
T26G	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 27

	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	35 91
	PCIE_85D	PCIE	PCIE_AP_R2D_N	35 91
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 35
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 35
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	17 35 91
	PCIE_85D	PCIE	PCIE_AP_D2R_N	17 35 91
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
T25	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17
T25A	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17
T26E	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	17 74
T26F	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	17 74
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 17
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	35 91
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	35 91
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 35
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 35
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
T26J	PCIE_T29_R2D	PCIE_85D	PCIE_T29_R2D_C_P<3..0>	8 74
T26K	PCIE_T29_R2D	PCIE_85D	PCIE_T29_R2D_C_N<3..0>	8 74
T26L	PCIE_T29_R2D	PCIE_85D	PCIE_T29_R2D_P<3..0>	74
T26M	PCIE_T29_R2D	PCIE_85D	PCIE_T29_R2D_N<3..0>	74
T26N	PCIE_T29_D2R	PCIE_85D	PCIE_T29_D2R_P<3..0>	8 74
T26P	PCIE_T29_D2R	PCIE_85D	PCIE_T29_D2R_N<3..0>	8 74
T27A	PCIE_T29_D2R	PCIE_85D	PCIE_T29_D2R_C_P<3..0>	74
T26Q	PCIE_T29_D2R	PCIE_85D	PCIE_T29_D2R_C_N<3..0>	74

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ETHERNET CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?
2KV_SPACING	*	0.50 MM	100
2KV_SPACING	TOP,BOTTOM	1.27 MM	100

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_HV	*	*	2KV_SPACING
ENET_HV	ENET_HV	*	ENET_MDI

NOTE: 2.2kV isolation needed on all primary-side ethernet signals. Min 1.27mm separation from all other copper on the board!

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	26 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	26 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 34
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
	ENET_100D	ENET_HV	ENET_MDI_TRAN_N<3..0>	36
	ENET_100D	ENET_HV	ENET_MDI_TRAN_P<3..0>	36
	ENET_50S	ENET_HV	ENET_CENTER_TAP<3..0>	36
		ENET_HV	ENET_CMODE_REF	36

High-voltage isolated ethernet signals.

SD Interface Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SD_55S	SD_INTERFACE	SDCONN_CLK	34 37 91
	SD_55S	SD_INTERFACE	SDCONN_CLK_FF	34
	SD_55S	SD_INTERFACE	SDCONN_CMD	34 37 91
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..0>	34 37 91
	SD_55S	SD_INTERFACE	SDCONN_CLK_R	34
	SD_55S	SD_INTERFACE	SDCONN_CMD_R	34
	SD_55S	SD_INTERFACE	SDCONN_DATA_R<7..0>	34
	SD_55S	SD_INTERFACE	ENET_CR_CLK	37
	SD_55S	SD_INTERFACE	ENET_CR_CMD	37
	SD_55S	SD_INTERFACE	ENET_CR_DATA<7..0>	37
	SD_55S	SD_INTERFACE	SDCONNF_CLK	34
	SD_55S	SD_INTERFACE	SDCONNF_CLK_FF	34

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P1_TPA	FW_110D	FW_TP	FW_P0_TPA_L_N	40
	FW_110D	FW_TP	FW_P0_TPA_L_P	40
FW_P1_TPB	FW_110D	FW_TP	FW_P0_TPB_L_N	40
	FW_110D	FW_TP	FW_P0_TPB_L_P	40
	FW_110D	FW_TP	FW_PORT0_TPAL_N	41
	FW_110D	FW_TP	FW_PORT0_TPAL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPA_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPBL_N	41
	FW_110D	FW_TP	FW_PORT0_TPBL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P	40 41
	50_OHM_SE	CLK_PCIE	CLK98M_FW_XI	39
	50_OHM_SE	CLK_PCIE	CLK98M_FW_XI_R	39

Port 0 and 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	49 74
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	49 74
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	74
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	74
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	74
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	74
	T29DP_90D	T29DP	T29_R2D_C_P<3..0>	74 77
	T29DP_90D	T29DP	T29_R2D_C_N<3..0>	74 77
	T29DP_90D	T29DP	T29_D2R_P<3..0>	74 77
	T29DP_90D	T29DP	T29_D2R_N<3..0>	74 77

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T29_R2D0	T29DP_90D	T29DP	T29_R2D_P<0>	77
T29_R2D0	T29DP_90D	T29DP	T29_R2D_N<0>	77
T29_R2D1	T29DP_90D	T29DP	T29_R2D_P<1>	77
T29_R2D1	T29DP_90D	T29DP	T29_R2D_N<1>	77
T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_P<0>	77 78
T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_N<0>	77 78
T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_P<1>	77 78
T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_N<1>	77 78
	T29DP_90D	T29DP	T29_R2D_C_F_P<1..0>	77
	T29DP_90D	T29DP	T29_R2D_C_F_N<1..0>	77
	T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_P	78
	T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_N	78
	T29DP_90D	T29DP	DP_SDRVA_ML_C_P<3..0>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_C_N<3..0>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_R_P<3..0>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_R_N<3..0>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_P<2>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_N<2>	77
DP_SDRVA_ML	T29DP_90D	T29DP	DP_SDRVA_ML_P<3>	77
DP_SDRVA_ML	T29DP_90D	T29DP	DP_SDRVA_ML_N<3>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_P<0>	77
	T29DP_90D	T29DP	DP_SDRVA_ML_N<0>	77
DP_SDRVA_ML	T29DP_90D	T29DP	DP_SDRVA_ML_P<1>	77
DP_SDRVA_ML	T29DP_90D	T29DP	DP_SDRVA_ML_N<1>	77
DP_SDRVA_AUXCH	T29DP_90D	T29DP	DP_SDRVA_AUXCH_P	77
DP_SDRVA_AUXCH	T29DP_90D	T29DP	DP_SDRVA_AUXCH_N	77
	T29DP_90D	T29DP	DP_SDRVA_AUXCH_C_P	77
	T29DP_90D	T29DP	DP_SDRVA_AUXCH_C_N	77
	T29DP_90D	T29DP	T29DPA_ML_P<3..0>	77 78
	T29DP_90D	T29DP	T29DPA_ML_N<3..0>	77 78
	T29DP_90D	T29DP	T29DPA_ML_C_P<3..0>	77 78
	T29DP_90D	T29DP	T29DPA_ML_C_N<3..0>	77 78
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_P	77 78 83
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_N	77 78 83
	T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_CC_P	
	T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_CC_N	
	T29DP_90D	T29DP	T29_D2R_CC_P<0>	
	T29DP_90D	T29DP	T29_D2R_CC_N<0>	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	46 49
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	46 49
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	46 49
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	ENET_ASF_SMB_CLK	37 49
	SMB_50S	SMB	ENET_ASF_SMB_DATA	37 49
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	46 49
183	SMB_50S	SMB	SMB_SMC_B_STR_SCL	49
184	SMB_50S	SMB	SMB_SMC_B_STR_SDA	49
185	SMB_50S	SMB	SMB_SMC_B_TSN_SCL	49
186	SMB_50S	SMB	SMB_SMC_B_TSN_SDA	49

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M
	100_OHM_DIFF	3X_DIELECTRIC	GPU_CLK_TEST_N
	100_OHM_DIFF	3X_DIELECTRIC	GPU_CLK_TEST_P
DP_AUX_CH	DP_90D	DISPLAYPORT	DP_EG_AUX_CH_P
	DP_90D	DISPLAYPORT	DP_EG_AUX_CH_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	12.7 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Breakout Constraint Overrides

Alternate diffpair width/gap through BGA fanout areas

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_90D	BGA	100_DIFF_BGA
DP_90D	BGA	100_DIFF_BGA
TMDS_85D	BGA	TMDS_85D
ENET_100D	BGA	100_DIFF_BGA
FW_110D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
PCIE_85D	BGA	PCIE_85D
MEM_85D	BGA	MEM_85D
USB_85D	BGA	USB_85D
GDDR5_80D	BGA	GDDR5_80D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	BGA_P075
MEM_50S	BGA	BGA_P075

J40* SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N

J40* SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SB_POWER			PP3V3_S5
SB_POWER			PP3V3_S0
GND			GND

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P
	THERM_1TO1_55S	THERM	CPU_THERMD_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P
	THERM_1TO1_55S	THERM	GPU_TDIODE_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P
	THERM_1TO1_55S	THERM	T29_THERMD_N

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J40* 12 LAYER BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	0.154 MM	0.154 MM	=STANDARD	0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.105 MM	0.105 MM	=STANDARD	0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.110 MM	0.090 MM	=STANDARD	0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.090 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.065 MM	0.065 MM	=STANDARD	0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_P075	TOP	Y	0.110 MM	0.080 MM	10 MM		
BGA_P075	BOTTOM	Y	0.110 MM	0.073 MM	10 MM		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 mlb stackup.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

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Airport/BT/Camera Conn.

FUNC_TEST

TRUE	PCIE_AP_D2R_P	17 35 84	
TRUE	PCIE_AP_D2R_N	17 35 84	
TRUE	PCIE_AP_R2D_P	35 84	
TRUE	PCIE_AP_R2D_N	35 84	
TRUE	PCIE_CLK100M_AP_CONN_P	35 84	
TRUE	PCIE_CLK100M_AP_CONN_N	35 84	
TRUE	AP_CLKREQ_Q_L	35	
TRUE	PCIE_WAKE_L	18 35 38 77	
TRUE	AP_RESET_CONN_L	35	
TRUE	WLAN_THROTTLE_L	35	
TRUE	PP3V3_S4_BT_F	35	
TRUE	PP3V3_WLAN	35 47	3 TPS
TRUE	USB_BT_CONN_P	35 83	
TRUE	USB_BT_CONN_N	35 83	
TRUE	GND		3 TPS

SD Card Connector

NOT USED - REMOVE

FUNC_TEST

FALSE	SDCONN_DATA<7..0>	34 37 85	
FALSE	SDCONN_CMD	34 37 85	
FALSE	SDCONN_CLK	34 37 85	
FALSE	SDCONN_DETECT	34	
FALSE	SDCONN_WP	34 37	
FALSE	PP3V3_SW_SD_PWR	34	
TRUE	GND		2 TPs

SATA HDD Connector

FUNC_TEST

TRUE	PP5V_S0	89 91 7 23 24 41 42 48 61 62 64 69 70 71 88 91	2 TPS
TRUE	SATA_HDD1_D2R_CONN_P	42 83	
TRUE	SATA_HDD1_D2R_CONN_N	42 83	
TRUE	SATA_HDD1_R2D_CONN_N	42 83	
TRUE	SATA_HDD1_R2D_CONN_P	42 83	
TRUE	GND		2 TPS

SATA HDD2 CONNECTOR

FUNC_TEST

TRUE	PP5V_S0	67 68 69 70 7 23 24 41 42 48 61 62 64 71 88 91	2 TPS
TRUE	SATA_HDD2_D2R_CONN_N	42 83	
TRUE	SATA_HDD2_D2R_CONN_P	42 83	
TRUE	SATA_HDD2_R2D_CONN_N	42 83	
TRUE	SATA_HDD2_R2D_CONN_P	42 83	
TRUE	GND		2 TPS

IR/LED,POWER BUTTON CONNECTORS

FUNC_TEST

TRUE	PPIRRCVR_F	45	1 TPS
TRUE	SMC_SYS_LED_DR	45	
TRUE	IRRCVR_OUT	44 45	
TRUE	POWER_BTN_N	45	
TRUE	POWER_BTN_P	45	
TRUE	GND		1 TPS

TEMPERATURE SENSOR CONNECTORS

TRUE	HDD_THRMD_P	
TRUE	HDD_THRMD_N	

Speaker Connectors

FUNC_TEST

TRUE	SPKRAMP_M_P_OUT	56 57	
TRUE	SPKRAMP_M_N_OUT	56 57	

Fan Connectors

FUNC_TEST

TRUE	PP12V_S0_FAN0_F	60	
TRUE	FAN0_CTL_F	60	
TRUE	FAN0_TACH_F	60	
TRUE	GND		1 TPS

PSU CONNECTOR

FUNC_TEST

TRUE	PP12V_G3H_PSU	6 51 72	4 TPS
TRUE	PSU_TEMP	46 72	
TRUE	GND		4 TPS

Power Nets

FUNC_TEST

TRUE	PP3V3_G3_RTC	6 17 18 21 27	
TRUE	PP5V_G3H	6 45 47 61 65	
TRUE	PP3V3_G3H	6 27 43 45 46 47 48 61 65 91	
TRUE	PP3V3_S5	6 17 18 19 20 21 23 24 25 27 28 59 61 62 78 89	
TRUE	PP3V3_ENET	6 26 37 38 62	
TRUE	PP1V2_ENET	6 37 38	
TRUE	PP5V_S4	6 28 43 44 45 61 65 66 78	
TRUE	PP3V3_S4	6 19 20 25 28 33 34 35 38 47 49 59 61 77 78	
TRUE	PP1V5_S3	6 28 30 31 32 61 66 72	
TRUE	PPDDRVREF_S3	6 33 66	
TRUE	PP5V_S0	7 23 24 41 42 48 61 62 64 67 68 69 70 71 88 91	
TRUE	PP3V3_S0	6 7 13 17 18 19 20 21 23 24 27 30 31 34 37 38 39 40 41 47 49 59 61 62 63 71 72 77 88 91	
TRUE	PP1V5_S0	7 17 21 23 39 53 71 72	
TRUE	PP1V05_S0_VCCIO	7 10 11 13 15 67	
TRUE	PP0V75_S0_DDRVTT	7 28 30 31 66	
TRUE	PPVCORE_S0_CPU	7 10 13 15 50 67 68	
TRUE	FW_PORT0_VP	41	
TRUE	PP3V3_S5_AVREF_SMC	46 47	
TRUE	PP4V5_AUDIO_ANALOG	53	
TRUE	PP3V3R12V_SW_DPAPWR_F	78	
TRUE	PP5V_HDMI_DDC_CONN	80	
TRUE	GND		1 TPS
TRUE	SMC_PM_G2_EN	46 47 62	
TRUE	PM_SLP_S5_L	18 46 62	
TRUE	PM_SLP_S4_L	18 28 46 62	
TRUE	PM_SLP_S3_L	18 28 46 51 62	

SPI BOOTROM SIGNALS

FUNC_TEST

TRUE	PP3V3_G3H	91 45 37 43 45 46 47 65	1 TPS
TRUE	SPI_CS0_L	48 84	
TRUE	SPI_CLK	48 84	
TRUE	SPI_MOSI	48 84	
TRUE	SPI_MISO	17 48 84	
TRUE	SPIROM_USE_MLB	20 48 59	
TRUE	GND		1 TPS

NO_TEST

TRUE	NC_AUD_GPIO_0	53
TRUE	NC_AUD_HP_PORT_R	53
TRUE	NC_AUD_MIC_INN_R	53
TRUE	NC_CLINK_CLK	17
TRUE	NC_CRT_IG_BLUE	18
TRUE	NC_CRT_IG_GREEN	18
TRUE	NC_CRT_IG_VSYNC	18
TRUE	NC_DP_OC	
TRUE	NC_EDP_TXN<3..0>	10
TRUE	NC_FW_P1_TPAP	39
TRUE	NC_FW_P2_TPAP	39
TRUE	NC_HD_OC	80
TRUE	NC_HDA_SDIN3	17
TRUE	NC_IG_DP_T29SNK0_AUXCH_CN	
TRUE	NC_IG_DP_T29SNK0_CTRL_DATA	
TRUE	NC_IG_DP_T29SNK0_ML_CP<3..0>	
TRUE	NC_IRUC_P04	44
TRUE	NC_IRUC_P14	44
TRUE	NC_LPC_DREQ0_L	17
TRUE	NC_LVDS_IG_A_DATAN<3..0>	19
TRUE	NC_LVDS_IG_B_CLKP	19
TRUE	NC_LVDS_IG_BKL_ON	19
TRUE	NC_LVDS_IG_CTRL_DATA	19
TRUE	NC_LVDS_IG_PANEL_PWR	19
TRUE	NC_OBSFN_B0	24
TRUE	NC_OBSFN_D01	24
TRUE	NC_PCH_CLKOUT_DPP	17
TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	17
TRUE	NC_PCH_LVDS_VBG	19
TRUE	NC_PCIE_4_D2RP	17
TRUE	NC_PCIE_5_D2RN	17
TRUE	NC_PCIE_5_R2D_CP	17
TRUE	NC_PCIE_6_R2D_CN	17
TRUE	NC_PCIE_7_D2RP	17
TRUE	NC_PCIE_8_D2RN	17
TRUE	NC_PCIE_8_R2D_CP	17
TRUE	NC_PCIE_CLK100M_PE5N	17
TRUE	NC_PCIE_CLK100M_PE6P	20
TRUE	NC_PCIE_CLK100M_PEBN	17
TRUE	NC_PCIE_CLK100M_T29P	
TRUE	NC_PCIE_T29_R2D_CN<3..0>	
TRUE	NC_PEG_CLK100MP	8
TRUE	NC_PEG_D2RP<7..0>	8
TRUE	NC_PEG_R2D_CN<15..12>	10
TRUE	NC_SATA_C_D2RN	17
TRUE	NC_SATA_C_R2D_CP	17
TRUE	NC_SATA_D_R2D_CN	17
TRUE	NC_SATA_E_D2RP	17
TRUE	NC_SATA_F_D2RN	17
TRUE	NC_SATA_F_R2D_CP	17
TRUE	NC_SDVO_STALLN	18
TRUE	NC_SDVO_TVCLKINP	18
TRUE	NC_SMC_FAN_1_TACH	46
TRUE	NC_SMC_FAN_3_CTL	46
TRUE	NC_SMC_P20	46
TRUE	NC_SMC_P43	46
TRUE	NC_SMC_SYS_KBDLED	46
TRUE	NC_USB_1N	19
TRUE	NC_USB_2P	19
TRUE	NC_USB_4N	19
TRUE	NC_USB_5P	19
TRUE	NC_USB_7N	19
TRUE	NC_USB_9P	19
TRUE	NC_USB_11N	19
TRUE	NC_USB_12P	19
TRUE	NC_CPU_AXG_SENSEN	
TRUE	NC_CPU_AXG_VALSENSEP	
TRUE	NC_EG_DP_T29SNK0_AUXCH_CP	
TRUE	NC_EG_DP_T29SNK0_ML_CP<3..0>	
TRUE	NC_FB_A0_ABI_L	
TRUE	NC_FB_A0_CKE_L	
TRUE	NC_FB_A0_CLKP	
TRUE	NC_FB_A0_DBI_L<3..0>	
TRUE	NC_FB_A0_EDC<3..0>	
TRUE	NC_FB_A0_WCLKN<1..0>	
TRUE	NC_FB_A0_WE_L	
TRUE	NC_FB_A1_ABI_L	
TRUE	NC_FB_A1_CKE_L	
TRUE	NC_FB_A1_CLKP	
TRUE	NC_FB_A1_DBI_L<3..0>	
TRUE	NC_FB_A1_EDC<3..0>	
TRUE	NC_FB_A1_WCLKN<1..0>	
TRUE	NC_FB_A1_WE_L	
TRUE	NC_GPU_GENERICB	
TRUE	NC_GPU_GENERICC	
TRUE	NC_GPU_GENERICE	
TRUE	NC_GPU_GENERICF	
TRUE	NC_GPU_GENERICG	
TRUE	NC_LVDS_EG_A_CLKN	
TRUE	NC_LVDS_EG_A_CLKP	
TRUE	NC_LVDS_EG_A_DATAN<3..0>	
TRUE	NC_LVDS_EG_A_DATAP<3..0>	
TRUE	NC_LVDS_EG_B_CLKN	
TRUE	NC_LVDS_EG_B_CLKP	
TRUE	NC_LVDS_EG_B_DATAN<3..0>	
TRUE	NC_LVDS_EG_B_DATAP<3..0>	
TRUE	NC_LVDS_EG_DDC_CLK	
TRUE	NC_LVDS_EG_DDC_DATA	

NO_TEST

TRUE	NC_AUD_GPIO_2	53
TRUE	NC_AUD_LO3_N_R	53
TRUE	NC_AUD_MIC_INP_R	53
TRUE	NC_CLINK_DATA	17
TRUE	NC_CRT_IG_DDC_CLK	18
TRUE	NC_CRT_IG_HSYNC	18
TRUE	NC_CS4206_FP	53
TRUE	NC_EDP_AUXN	10
TRUE	NC_EDP_TXP<3..0>	10
TRUE	NC_FW_P1_TPBIAS	39
TRUE	NC_FW_P2_TPBIAS	39
TRUE	NC_HDA_SDIN1	17
TRUE	NC_IG_D_AUXN	18
TRUE	NC_IG_DP_T29SNK0_AUXCH_CP	
TRUE	NC_IG_DP_T29SNK0_HPD	
TRUE	NC_IRUC_P02	44
TRUE	NC_IRUC_P06	44
TRUE	NC_IRUC_P15	44
TRUE	NC_LVDS_IG_A_CLKN	19
TRUE	NC_LVDS_IG_A_DATAP<3..0>	19
TRUE	NC_LVDS_IG_B_DATAN<3..0>	19
TRUE	NC_LVDS_IG_BKL_PWM	19
TRUE	NC_LVDS_IG_DDC_CLK	19
TRUE	NC_LVDS_IG_VREFH	19
TRUE	NC_OBSFN_B1	24
TRUE	NC_OBSFN_D11	24
TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	17
TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	17
TRUE	NC_PCI_PME_L	19
TRUE	NC_PCIE_4_R2D_CN	17
TRUE	NC_PCIE_5_D2RP	17
TRUE	NC_PCIE_6_D2RN	17
TRUE	NC_PCIE_6_R2D_CP	17
TRUE	NC_PCIE_7_R2D_CN	17
TRUE	NC_PCIE_8_D2RP	17
TRUE	NC_PCIE_CLK100M_EXCARDN	17
TRUE	NC_PCIE_CLK100M_PE5P	17
TRUE	NC_PCIE_CLK100M_PE7N	20
TRUE	NC_PCIE_CLK100M_PEBP	17
TRUE	NC_PCIE_T29_D2RN<3..0>	
TRUE	NC_PCIE_T29_R2D_CP<3..0>	
TRUE	NC_PEG_D2RN<7..0>	8
TRUE	NC_PEG_D2RP<15..12>	10
TRUE	NC_PEG_R2D_CP<7..0>	8
TRUE	NC_SATA_C_D2RP	17
TRUE	NC_SATA_D_D2RN	17
TRUE	NC_SATA_D_R2D_CP	17
TRUE	NC_SATA_E_R2D_CN	17
TRUE	NC_SATA_F_D2RP	17
TRUE	NC_SDVO_INTN	18
TRUE	NC_SDVO_STALLP	18
TRUE	NC_SMC_BMON_MUX_SEL	46
TRUE	NC_SMC_FAN_2_CTL	46
TRUE	NC_SMC_FAN_3_TACH	46
TRUE	NC_SMC_P24	46
TRUE	NC_SMC_PF5	46
TRUE	NC_SPI_DESCRIPTOR_OVERRIDE_L	46
TRUE	NC_USB_1P	19
TRUE	NC_USB_3N	19
TRUE	NC_USB_4P	19
TRUE	NC_USB_6N	19
TRUE	NC_USB_7P	19
TRUE	NC_USB_10N	19
TRUE	NC_USB_11P	19
TRUE	NC_USB_13N	19
TRUE	NC_CPU_AXG_SENSEP	
TRUE	NC_CPU_AXG_VALSENSEN	
TRUE	NC_EG_DP_T29SNK0_AUXCH_CN	
TRUE	NC_EG_DP_T29SNK0_ML_CN<3..0>	
TRUE	NC_FB_A0_A<8..0>	
TRUE	NC_FB_A0_CAS_L	
TRUE	NC_FB_A0_CLKN	
TRUE	NC_FB_A0_CS_L	
TRUE	NC_FB_A0_DQ<31..0>	
TRUE	NC_FB_A0_RAS_L	
TRUE	NC_FB_A0_WCLKP<1..0>	
TRUE	NC_FB_A1_A<8..0>	
TRUE	NC_FB_A1_CAS_L	
TRUE	NC_FB_A1_CLKN	
TRUE	NC_FB_A1_CS_L	
TRUE	NC_FB_A1_DQ<31..0>	
TRUE	NC_FB_A1_RAS_L	
TRUE	NC_FB_A1_WCLKP<1..0>	
TRUE	NC_EDP_HPD	10

NO_TEST

TRUE	NC_AUD_HP_PORT_L	53
TRUE	NC_AUD_LO3_P_R	53
TRUE	NC_BCM57765_CE_L_MS_INS_L	37
TRUE	NC_CLINK_RESET_L	17
TRUE	NC_CRT_IG_DDC_DATA	18
TRUE	NC_CRT_IG_RED	18
TRUE	NC_CS4206_MICBIAS	53
TRUE	NC_EDP_AUXP	10
TRUE	NC_FW_P1_TPAN	39
TRUE	NC_FW_P2_TPAN	39
TRUE	NC_GPIO35	20
TRUE	NC_HDA_SDIN2	17
TRUE	NC_IG_D_AUXP	18
TRUE	NC_IG_DP_T29SNK0_CTRL_CLK	
TRUE	NC_IG_DP_T29SNK0_ML_CN<3..0>	
TRUE	NC_IRUC_P03	44
TRUE	NC_IRUC_P13	44
TRUE	NC_IRUC_P16	44
TRUE	NC_LVDS_IG_A_CLKP	19
TRUE	NC_LVDS_IG_B_CLKN	19
TRUE	NC_LVDS_IG_B_DATAP<3..0>	19
TRUE	NC_LVDS_IG_CTRL_CLK	19
TRUE	NC_LVDS_IG_DDC_DATA	19
TRUE	NC_LVDS_IG_VREFL	19
TRUE	NC_OBSFN_C0	24
TRUE	NC_PCH_CLKOUT_DPN	17
TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	17
TRUE	NC_PCH_LVDS_IBG	19
TRUE	NC_PCIE_4_D2RN	17
TRUE	NC_PCIE_4_R2D_CP	17
TRUE	NC_PCIE_5_R2D_CN	17
TRUE	NC_PCIE_6_D2RP	17
TRUE	NC_PCIE_7_D2RN	17
TRUE	NC_PCIE_7_R2D_CP	17
TRUE	NC_PCIE_8_R2D_CN	17
TRUE	NC_PCIE_CLK100M_EXCARDP	17
TRUE	NC_PCIE_CLK100M_PE6N	20
TRUE	NC_PCIE_CLK100M_PE7P	20
TRUE	NC_PCIE_CLK100M_T29N	
TRUE	NC_PCIE_T29_D2RP<3..0>	
TRUE	NC_PEG_CLK100MN	8
TRUE	NC_PEG_D2RN<15..12>	10
TRUE	NC_PEG_R2D_CN<7..0>	8
TRUE	NC_PEG_R2D_CP<15..12>	10
TRUE	NC_SATA_C_R2D_CN	17
TRUE	NC_SATA_D_D2RP	17
TRUE	NC_SATA_E_D2RN	17
TRUE	NC_SATA_E_R2D_CP	17
TRUE	NC_SATA_F_R2D_CN	17
TRUE	NC_SDVO_INTP	18
TRUE	NC_SDVO_TVCLKINN	18
TRUE	NC_SMC_FAN_1_CTL	46
TRUE	NC_SMC_FAN_2_TACH	46
TRUE	NC_SMC_P10	46
TRUE	NC_SMC_P41	46
TRUE	NC_SMC_RSTGATE_L	46
TRUE	NC_T29_PWR_EN	
TRUE	NC_USB_2N	19
TRUE	NC_USB_3P	19
TRUE	NC_USB_5N	19
TRUE	NC_USB_6P	19
TRUE	NC_USB_9N	19
TRUE	NC_USB_10P	19
TRUE	NC_USB_12N	19
TRUE	NC_USB_13P	19
TRUE	NC_T29_R2D_CP1	74
TRUE	NC_T29_R2D_CP0	74
TRUE	NC_T29_R2D_CN1	74
TRUE	NC_T29_R2D_CN0	74
TRUE	NC_T29_PCIE_RESET3_L	74
TRUE	NC_T29_PCIE_RESET2_L	74
TRUE	NC_T29_PCIE_RESET1_L	74
TRUE	NC_T29_PCIE_RESET0_L	74
TRUE	NC_T29_D2RP1	74
TRUE	NC_T29_D2RP0	74
TRUE	NC_T29_D2RN1	74
TRUE	NC_T29_D2RN0	74
TRUE	NC_DP_T29SRC_ML_CP<3..0>	74
TRUE	NC_DP_T29SRC_ML_CN<3..0>	74
TRUE	NC_DP_T29SRC_AUXCH_CP	74
TRUE	NC_DP_T29SRC_AUXCH_CN	74
TRUE	NC_DP_T29SNK1_MLP<3..0>	74
TRUE	NC_DP_T29SNK1_MLN<3..0>	74
TRUE	NC_DP_T29SNK1_AUXCHP	74
TRUE	NC_DP_T29SNK1_AUXCHN	74

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FORCES CROSS REFERENCE PAGES TO COME AFTER THIS.
SKIPS ANY TEMPORARY PAGES I MIGHT MAKE.

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Title:          Basenet Report
Design:         mlb
Date:           Apr 7 18:57:22 2011

Base nets and synonyms for mlb_lib.MLB(@mlb_lib.mlb(sch_1))
Base Signal          Synonyms                                  Location([Zone][dir])

1V05_S0_LDO_EN       1V05_S0_LDO_EN - @mlb_lib.MLB             62C1
                     CPUVCCIOS0_EN - @mlb_lib.MLB              62C1 70C7
3V3R2V8_DPAPWR_ADJ   3V3R2V8_DPAPWR_ADJ - @mlb_lib.MLB         78D7
3V3R2V8_SS_A         3V3R2V8_SS_A - @mlb_lib.MLB               78D8
80101A_NC            80101A_NC - @mlb_lib.MLB                  78C8
=I2C_DPSDRVA_SCL     =I2C_DPSDRVA_SCL - @mlb_lib.MLB           49B1 49B6 77B7
                     I2C_DPSDRVA_SCL - @mlb_lib.MLB            49B2 49B7
=I2C_DPSDRVA_SDA     =I2C_DPSDRVA_SDA - @mlb_lib.MLB           49B1 49B6 77B7
                     I2C_DPSDRVA_SDA - @mlb_lib.MLB            49B2 49B7
=IG_DP_T29SNK0_CTRL_ =IG_DP_T29SNK0_CTRL_CLK -                 8B8 18C1
CLK                  @mlb_lib.MLB
                     DP_T29SNK0_CTRL_CLK - @mlb_lib.MLB        8B5 74A8
=IG_DP_T29SNK0_CTRL_ =IG_DP_T29SNK0_CTRL_DATA -                8B8 18C1
DATA                 @mlb_lib.MLB
                     DP_T29SNK0_CTRL_DATA - @mlb_lib.MLB       8B5 74A8
=PLT_RST_T29_GPU     =PLT_RST_T29_GPU - @mlb_lib.MLB           27C1 76C8
                     PLT_RST_BUF_L - @mlb_lib.MLB              27C3
=SMC_GFX_THROTTLE_L  =SMC_GFX_THROTTLE_L - @mlb_lib.MLB        46C8 73B6
                     TP_GFX_THROTTLE_L - @mlb_lib.MLB          73B4
ALL_SYS_PWRGD        ALL_SYS_PWRGD - @mlb_lib.MLB              27A8 46D8 62A5 62C5 62C6
ALL_SYS_PWRGD_R      ALL_SYS_PWRGD_R - @mlb_lib.MLB            62A6
AMBIENT_THRMD_N      AMBIENT_THRMD_N - @mlb_lib.MLB            52B3 52C8
AMBIENT_THRMD_P      AMBIENT_THRMD_P - @mlb_lib.MLB            52B3 52C8
AP_CLKREQ_L          AP_CLKREQ_L - @mlb_lib.MLB                17B4 17B5 35A3
AP_CLKREQ_Q_L        AP_CLKREQ_Q_L - @mlb_lib.MLB              35A4 91D7
AP_PWR_EN            AP_PWR_EN - @mlb_lib.MLB                  19C1 24D4 35A3 62A4
AP_RESET_CONN_L      AP_RESET_CONN_L - @mlb_lib.MLB            35B4 91D7
AP_RESET_L           AP_RESET_L - @mlb_lib.MLB                 27D1 35B3
AUD_4V5_REG_IN       AUD_4V5_REG_IN - @mlb_lib.MLB             53A6
AUD_CONNJ1_MIC_HI    AUD_CONNJ1_MIC_HI - @mlb_lib.MLB          57D7
AUD_CONNJ1_PERIPHDET AUD_CONNJ1_PERIPHDET - @mlb_lib.MLB       57C7
AUD_CONNJ1_RING      AUD_CONNJ1_RING - @mlb_lib.MLB            57D7
AUD_CONNJ1_SLEEVE    AUD_CONNJ1_SLEEVE - @mlb_lib.MLB          57C7
AUD_CONNJ1_SLEEVEDET AUD_CONNJ1_SLEEVEDET - @mlb_lib.MLB       57D7
AUD_CONNJ1_TIP       AUD_CONNJ1_TIP - @mlb_lib.MLB             57D7
AUD_CONNJ1_TIPDET    AUD_CONNJ1_TIPDET - @mlb_lib.MLB          57C7
AUD_CONNJ2_RING      AUD_CONNJ2_RING - @mlb_lib.MLB            57B6
AUD_CONNJ2_SLEEVE    AUD_CONNJ2_SLEEVE - @mlb_lib.MLB          57B6
AUD_CONNJ2_TIP       AUD_CONNJ2_TIP - @mlb_lib.MLB             57B6
AUD_CONNJ2_TIPDET    AUD_CONNJ2_TIPDET - @mlb_lib.MLB          57B6
AUD_GPIO_1           AUD_GPIO_1 - @mlb_lib.MLB                 53D7 55B6
AUD_GPIO_3           AUD_GPIO_3 - @mlb_lib.MLB                 53C7 56B7
AUD_HPAMP_INL_N      AUD_HPAMP_INL_N - @mlb_lib.MLB            55C5
AUD_HPAMP_INL_P      AUD_HPAMP_INL_P - @mlb_lib.MLB            55C5
AUD_HPAMP_INR_N      AUD_HPAMP_INR_N - @mlb_lib.MLB            55B5
AUD_HPAMP_INR_P      AUD_HPAMP_INR_P - @mlb_lib.MLB            55C5
AUD_HPAMP_MUTE_L     AUD_HPAMP_MUTE_L - @mlb_lib.MLB           55B5
AUD_HPAMP_OUTL       AUD_HPAMP_OUTL - @mlb_lib.MLB             55C1 55C5 57D3
AUD_HPAMP_OUTR       AUD_HPAMP_OUTR - @mlb_lib.MLB             55B1 55B5 57D3
AUD_HPAMP_RETURN     AUD_HPAMP_RETURN - @mlb_lib.MLB           55B1 57C3
AUD_HPREF            AUD_HPREF - @mlb_lib.MLB                  53D3
AUD_I2C_INT_L        AUD_I2C_INT_L - @mlb_lib.MLB              19D6 58D5
AUD_INJACK_INSERT_L  AUD_INJACK_INSERT_L - @mlb_lib.MLB        58A5
AUD_IPHS_SWITCH_EN   AUD_IPHS_SWITCH_EN - @mlb_lib.MLB         20B1 58D5
AUD_IPHS_SWITCH_EN_P AUD_IPHS_SWITCH_EN_PCH -                  20A1 20B3 20D6
CH                   @mlb_lib.MLB
AUD_IP_PERIPHERAL_DE AUD_IP_PERIPHERAL_DET -                   19D6 58B1
T                    @mlb_lib.MLB
AUD_J1_DET_RC        AUD_J1_DET_RC - @mlb_lib.MLB              58B7
AUD_J1_PERIPHDET     AUD_J1_PERIPHDET - @mlb_lib.MLB           57C3 58A4
AUD_J1_PERIPHDET_INV AUD_J1_PERIPHDET_INV - @mlb_lib.MLB       58A2
AUD_J1_SLEEVEDET     AUD_J1_SLEEVEDET - @mlb_lib.MLB           57D3 58C6 58C8
AUD_J1_SLEEVEDET_INV AUD_J1_SLEEVEDET_INV - @mlb_lib.MLB       58C7
AUD_J1_TIPDET        AUD_J1_TIPDET - @mlb_lib.MLB              57C3 58B8
AUD_J2_DET_RC        AUD_J2_DET_RC - @mlb_lib.MLB              58A6
AUD_J2_OPT_OUT       AUD_J2_OPT_OUT - @mlb_lib.MLB             57B6
AUD_J2_TIPDET_R      AUD_J2_TIPDET_R - @mlb_lib.MLB            57B3 58A7
AUD_LI_GND           AUD_LI_GND - @mlb_lib.MLB                 54C6 57B3
AUD_LI_INL           AUD_LI_INL - @mlb_lib.MLB                 54D6 57B3
AUD_LI_INR           AUD_LI_INR - @mlb_lib.MLB                 54C6 57B3
AUD_LI_LF            AUD_LI_LF - @mlb_lib.MLB                  54D5
AUD_LI_N_LR          AUD_LI_N_LR - @mlb_lib.MLB                53C2 54C3
AUD_LI_P_L           AUD_LI_P_L - @mlb_lib.MLB                 53C2 54D3
AUD_LI_P_R           AUD_LI_P_R - @mlb_lib.MLB                 53C2 54C3
AUD_LI_RF            AUD_LI_RF - @mlb_lib.MLB                  54C5
AUD_LO2_N_L          AUD_LO2_N_L - @mlb_lib.MLB                53D2 55C8
AUD_LO2_N_R          AUD_LO2_N_R - @mlb_lib.MLB                53C2 55B8
AUD_LO2_P_L          AUD_LO2_P_L - @mlb_lib.MLB                53D2 55C8
AUD_LO2_P_R          AUD_LO2_P_R - @mlb_lib.MLB                53D2 55B8
AUD_LO3_N_L          AUD_LO3_N_L - @mlb_lib.MLB                53C2 56C7
AUD_LO3_P_L          AUD_LO3_P_L - @mlb_lib.MLB                53C2 56B7
AUD_MIC_INN_L        AUD_MIC_INN_L - @mlb_lib.MLB              53C2 58C4
AUD_MIC_INP_L        AUD_MIC_INP_L - @mlb_lib.MLB              53C2 58C4
AUD_OUTJACK_INSERT_L AUD_OUTJACK_INSERT_L - @mlb_lib.MLB       58B6
AUD_PERIPH_DET_R     AUD_PERIPH_DET_R - @mlb_lib.MLB           58B2
AUD_PORT_D_DET_L     AUD_PORT_D_DET_L - @mlb_lib.MLB           58C5
AUD_PORT_G_DET_L     AUD_PORT_G_DET_L - @mlb_lib.MLB           58C5
AUD_REG_SHDN_L       AUD_REG_SHDN_L - @mlb_lib.MLB             53A7
AUD_SDI_R            AUD_SDI_R - @mlb_lib.MLB                  53C6 84C3
AUD_SENSE_A          AUD_SENSE_A - @mlb_lib.MLB                53C7 58A7 58C8
AUD_SPDIF_IN         AUD_SPDIF_IN - @mlb_lib.MLB               53C7 57B3
AUD_SPDIF_OUT        AUD_SPDIF_OUT - @mlb_lib.MLB              53C7 57C3
AUD_SPKRAMP_INL      AUD_SPKRAMP_INL - @mlb_lib.MLB            56B6
AUD_SPKRAMP_INL_L    AUD_SPKRAMP_INL_L - @mlb_lib.MLB          56B7
AUD_SPKRAMP_INR      AUD_SPKRAMP_INR - @mlb_lib.MLB            56C6
AUD_SPKRAMP_INR_L    AUD_SPKRAMP_INR_L - @mlb_lib.MLB          56C7
AUD_SPKRAMP_SD_H     AUD_SPKRAMP_SD_H - @mlb_lib.MLB           56B7
BCM5764_CLK25M_XTALI BCM5764_CLK25M_XTALI - @mlb_lib.MLB       26C1 37B6 85D3
                     SYSCLK_CLK25M_ENET - @mlb_lib.MLB         26C3
BCM5764_CLK25M_XTALO BCM5764_CLK25M_XTALO - @mlb_lib.MLB       26C1 37B6 85D3
                     TP_ENET_CLK25M_XTALO - @mlb_lib.MLB       26C3
BCM57765_CS_L        BCM57765_CS_L - @mlb_lib.MLB              37A8 37B6
BCM57765_MISO        BCM57765_MISO - @mlb_lib.MLB              37A6 37B6
BCM57765_MOSI        BCM57765_MOSI - @mlb_lib.MLB              37A6 37B6
BCM57765_RDAC        BCM57765_RDAC - @mlb_lib.MLB              37B6
BCM57765_SCLK        BCM57765_SCLK - @mlb_lib.MLB              37A8 37B6
BCM57765_VMAIN_PRSNT BCM57765_VMAIN_PRSNT - @mlb_lib.MLB       37C6
BCM57765_WAKE_R_L    BCM57765_WAKE_R_L - @mlb_lib.MLB          37B6
BDM57765_SR_DISABLE  BDM57765_SR_DISABLE - @mlb_lib.MLB        37B4
BOOT_1V8S0           BOOT_1V8S0 - @mlb_lib.MLB                 71C6
CATERR_LED           CATERR_LED - @mlb_lib.MLB                 6B1
CATERR_LED_R         CATERR_LED_R - @mlb_lib.MLB               6B1
CATERR_R             CATERR_R - @mlb_lib.MLB                   6B2
CIV_ENET_RESET_L     CIV_ENET_RESET_L - @mlb_lib.MLB           34B2 37B6
CLK98M_FW_XI         CLK98M_FW_XI - @mlb_lib.MLB               39C3 85B3
CLK98M_FW_XI_R       CLK98M_FW_XI_R - @mlb_lib.MLB             39C2 85B3
COMP_1V8S0           COMP_1V8S0 - @mlb_lib.MLB                 71C7

COMP_RC_1V8S0        COMP_RC_1V8S0 - @mlb_lib.MLB              71C8
CPUIMVP_ISUMG_IOUT   CPUIMVP_ISUMG_IOUT - @mlb_lib.MLB         50B3
CPUIMVP_ISUMG_RN     CPUIMVP_ISUMG_RN - @mlb_lib.MLB           50B3
CPUIMVP_ISUM_IOUT    CPUIMVP_ISUM_IOUT - @mlb_lib.MLB          50D2
CPUIMVP_ISUM_RN      CPUIMVP_ISUM_RN - @mlb_lib.MLB            50D3
CPUTHMSNS_D2_N       CPUTHMSNS_D2_N - @mlb_lib.MLB             89B1
CPUTHMSNS_D2_P       CPUTHMSNS_D2_P - @mlb_lib.MLB             89B1
CPUVCCIOS0_AGND      CPUVCCIOS0_AGND - @mlb_lib.MLB            70B6
CPUVCCIOS0_CS_N      CPUVCCIOS0_CS_N - @mlb_lib.MLB            50B8 70B2 89D3
CPUVCCIOS0_CS_P      CPUVCCIOS0_CS_P - @mlb_lib.MLB            50B8 70B2 89D3
CPUVCCIOS0_DRVH      CPUVCCIOS0_DRVH - @mlb_lib.MLB            70C5
CPUVCCIOS0_DRVL      CPUVCCIOS0_DRVL - @mlb_lib.MLB            70C5
CPUVCCIOS0_FB        CPUVCCIOS0_FB - @mlb_lib.MLB              70C6
CPUVCCIOS0_FSEL      CPUVCCIOS0_FSEL - @mlb_lib.MLB            70B6
CPUVCCIOS0_LL        CPUVCCIOS0_LL - @mlb_lib.MLB              70C5
CPUVCCIOS0_OCSET     CPUVCCIOS0_OCSET - @mlb_lib.MLB           70C6
CPUVCCIOS0_PGOOD     CPUVCCIOS0_PGOOD - @mlb_lib.MLB           62A6 62B5 70B7
CPUVCCIOS0_RTN       CPUVCCIOS0_RTN - @mlb_lib.MLB             70B6
CPUVCCIOS0_SREF      CPUVCCIOS0_SREF - @mlb_lib.MLB            70C6
CPUVCCIOS0_VBST      CPUVCCIOS0_VBST - @mlb_lib.MLB            70C5
CPUVCCIOS0_VBST_RC   CPUVCCIOS0_VBST_RC - @mlb_lib.MLB         70C5
CPUVCCIOS0_VO        CPUVCCIOS0_VO - @mlb_lib.MLB              70C6
CPUVCCIO_IOUT        CPUVCCIO_IOUT - @mlb_lib.MLB              50B7
CPUVCCSAS0_SNUB      CPUVCCSAS0_SNUB - @mlb_lib.MLB            70B3
CPUVSENSE_IN         CPUVSENSE_IN - @mlb_lib.MLB               50C3
CPU_AXG_SENSE_N      CPU_AXG_SENSE_N - @mlb_lib.MLB            13B4 67D8 81A3
CPU_AXG_SENSE_P      CPU_AXG_SENSE_P - @mlb_lib.MLB            13B4 67D8 81A3
CPU_AXG_VALSENSE_N   CPU_AXG_VALSENSE_N - @mlb_lib.MLB         10C4 81A3
CPU_AXG_VALSENSE_P   CPU_AXG_VALSENSE_P - @mlb_lib.MLB         10C4 81A3
CPU_CATERR_L         CPU_CATERR_L - @mlb_lib.MLB               6B3 11C6 81B3
CPU_CATERR_RL        CPU_CATERR_RL - @mlb_lib.MLB              6B3
CPU_CFG<0>           CPU_CFG<0> - @mlb_lib.MLB                 10A7 10D3 24C8
CPU_CFG<11..0>       CPU_CFG<11..0> - @mlb_lib.MLB             81B3
CPU_CFG<1>           CPU_CFG<1> - @mlb_lib.MLB                 10A7 10D3
CPU_CFG<2>           CPU_CFG<2> - @mlb_lib.MLB                 10A8 10D3
CPU_CFG<3>           CPU_CFG<3> - @mlb_lib.MLB                 10A7 10D3
CPU_CFG<4>           CPU_CFG<4> - @mlb_lib.MLB                 10A8 10D3
CPU_CFG<5>           CPU_CFG<5> - @mlb_lib.MLB                 10A8 10D3
CPU_CFG<6>           CPU_CFG<6> - @mlb_lib.MLB                 10A8 10D3
CPU_CFG<7>           CPU_CFG<7> - @mlb_lib.MLB                 10A8 10D3
CPU_CFG<16>          CPU_CFG<16> - @mlb_lib.MLB                10A7 10D3
CPU_CFG<17..16>      CPU_CFG<17..16> - @mlb_lib.MLB            81B3
CPU_COMP0            CPU_COMP0 - @mlb_lib.MLB                  81B3
CPU_COMP1            CPU_COMP1 - @mlb_lib.MLB                  81B3
CPU_COMP2            CPU_COMP2 - @mlb_lib.MLB                  81B3
CPU_COMP3            CPU_COMP3 - @mlb_lib.MLB                  81B3
CPU_DC_TEST_BE59_BE6 CPU_DC_TEST_BE59_BE61 -                   10C2
1                    @mlb_lib.MLB
CPU_DC_TEST_BG59_BG6 CPU_DC_TEST_BG59_BG61 -                   10C2
1                    @mlb_lib.MLB
CPU_DC_TEST_C4_BE1_B CPU_DC_TEST_C4_BE1_BG1 -                  10B2
G1                   @mlb_lib.MLB
CPU_DC_TEST_C4_BE3_B CPU_DC_TEST_C4_BE3_BG3 -                  10C2
G3                   @mlb_lib.MLB
CPU_DC_TEST_C4_D3    CPU_DC_TEST_C4_D3 - @mlb_lib.MLB          10C2
CPU_DC_TEST_C59_A59  CPU_DC_TEST_C59_A59 - @mlb_lib.MLB        10C2
CPU_DC_TEST_C61_A61  CPU_DC_TEST_C61_A61 - @mlb_lib.MLB        10C2
CPU_DDR_VREF         CPU_DDR_VREF - @mlb_lib.MLB               13B1 13C1
CPU_MEM_RESET_L      CPU_MEM_RESET_L - @mlb_lib.MLB            11B6 28A8
CPU_MEM_VREFDQ_A     CPU_MEM_VREFDQ_A - @mlb_lib.MLB           10B2 10D1
CPU_MEM_VREFDQ_B     CPU_MEM_VREFDQ_B - @mlb_lib.MLB           10B2 10D1
CPU_PECI             CPU_PECI - @mlb_lib.MLB                   11C6 20D3 46A4 81C3
CPU_PECI_R           CPU_PECI_R - @mlb_lib.MLB                 46A5 81C3
CPU_PEG_COMP         CPU_PEG_COMP - @mlb_lib.MLB               10D5 81B3
CPU_PEG_RBIAS        CPU_PEG_RBIAS - @mlb_lib.MLB              81B3
CPU_PROCHOT_BUF      CPU_PROCHOT_BUF - @mlb_lib.MLB            47D2
CPU_PROCHOT_L        CPU_PROCHOT_L - @mlb_lib.MLB              11C7 47D4 67B6 81B3
CPU_PROCHOT_L_R      CPU_PROCHOT_L_R - @mlb_lib.MLB            47D3
CPU_PROCHOT_R_L      CPU_PROCHOT_R_L - @mlb_lib.MLB            11C6
CPU_PROC_SEL_L       CPU_PROC_SEL_L - @mlb_lib.MLB             11C6 18B4 81B3
CPU_PROX_THRM_N      CPU_PROX_THRM_N - @mlb_lib.MLB            52D3 52D8
CPU_PROX_THRM_P      CPU_PROX_THRM_P - @mlb_lib.MLB            52D3 52D8
CPU_PSI_L            CPU_PSI_L - @mlb_lib.MLB                  81B3
CPU_PWRGD            CPU_PWRGD - @mlb_lib.MLB                  11C6 20D3 24C8 81B3
CPU_RESET_L          CPU_RESET_L - @mlb_lib.MLB                11B7 24C3 27C1
                     PLT_RST_CPU_BUF_L - @mlb_lib.MLB          27C3
CPU_SM_RCOMP<0>      CPU_SM_RCOMP<0> - @mlb_lib.MLB            11B5
CPU_SM_RCOMP<2..0>   CPU_SM_RCOMP<2..0> - @mlb_lib.MLB         81C3
CPU_SM_RCOMP<1>      CPU_SM_RCOMP<1> - @mlb_lib.MLB            11B5
CPU_SM_RCOMP<2>      CPU_SM_RCOMP<2> - @mlb_lib.MLB            11B5
CPU_THERMD_N         CPU_THERMD_N - @mlb_lib.MLB               10C4 52D2 52D8 89B1
CPU_THERMD_P         CPU_THERMD_P - @mlb_lib.MLB               10C4 52D2 52D8 89B1
CPU_VCCIOSENSE_N     CPU_VCCIOSENSE_N - @mlb_lib.MLB           13A5 70C8 81A3
CPU_VCCIOSENSE_P     CPU_VCCIOSENSE_P - @mlb_lib.MLB           13A5 70C8 81B3
CPU_VCCIO_SEL        CPU_VCCIO_SEL - @mlb_lib.MLB              13B7
CPU_VCCSA_SENSE      CPU_VCCSA_SENSE - @mlb_lib.MLB            13C1 64C8
CPU_VCCSA_VID<0>     CPU_VCCSA_VID<0> - @mlb_lib.MLB           13C1 64A6
                     PD_CPU_VCCSA_VID0 - @mlb_lib.MLB          64A5
CPU_VCCSA_VID<1>     CPU_VCCSA_VID<1> - @mlb_lib.MLB           13C1 64B6 81C3
CPU_VCCSENSE_N       CPU_VCCSENSE_N - @mlb_lib.MLB             13A5 67A8 81B3
CPU_VCCSENSE_P       CPU_VCCSENSE_P - @mlb_lib.MLB             13A5 67A8 81B3
CPU_VCC_VALSENSE_N   CPU_VCC_VALSENSE_N - @mlb_lib.MLB         10C4 81A3
CPU_VCC_VALSENSE_P   CPU_VCC_VALSENSE_P - @mlb_lib.MLB         10C4 81A3
CPU_VIDALERT_L       CPU_VIDALERT_L - @mlb_lib.MLB             13B5 67B6 81C3
CPU_VIDALERT_L_R     CPU_VIDALERT_L_R - @mlb_lib.MLB           13B6 81C3
CPU_VIDSCLK          CPU_VIDSCLK - @mlb_lib.MLB                13B5 67C6 81C3
CPU_VIDSCLK_R        CPU_VIDSCLK_R - @mlb_lib.MLB              13B6 81C3
CPU_VIDSOUT          CPU_VIDSOUT - @mlb_lib.MLB                13B5 67B6 81C3
CPU_VIDSOUT_R        CPU_VIDSOUT_R - @mlb_lib.MLB              13B6 81C3
CPU_VTTSELECT        CPU_VTTSELECT - @mlb_lib.MLB              81B3
CS4206_SPDIF_OUT     CS4206_SPDIF_OUT - @mlb_lib.MLB           53C6
CS4206_VCOM          CS4206_VCOM - @mlb_lib.MLB                53C3
CS4206_VREF_ADC      CS4206_VREF_ADC - @mlb_lib.MLB            53C3
DCINVSENS_EN_L       DCINVSENS_EN_L - @mlb_lib.MLB             51C3
DCIN_IOUT            DCIN_IOUT - @mlb_lib.MLB                  51D6
DCIN_S5_VSENSE       DCIN_S5_VSENSE - @mlb_lib.MLB             51D3
DDRREG_1V8_VREF      DDRREG_1V8_VREF - @mlb_lib.MLB            66C7
DDRREG_DRVH          DDRREG_DRVH - @mlb_lib.MLB                66C6
DDRREG_DRVL          DDRREG_DRVL - @mlb_lib.MLB                66C6
DDRREG_MODE          DDRREG_MODE - @mlb_lib.MLB                66C7
DDRREG_PGOOD         DDRREG_PGOOD - @mlb_lib.MLB               62B6 66C5
DDRREG_REFIN         DDRREG_REFIN - @mlb_lib.MLB               33B1 66C7
DDRREG_SNUB          DDRREG_SNUB - @mlb_lib.MLB                66C3
DDRREG_SW            DDRREG_SW - @mlb_lib.MLB                  66C6
DDRREG_TRIP          DDRREG_TRIP - @mlb_lib.MLB                66C7
DDRREG_VBST          DDRREG_VBST - @mlb_lib.MLB                66C6
DDRREG_VBST_R        DDRREG_VBST_R - @mlb_lib.MLB              66C5
DDRREG_VDDQSNS       DDRREG_VDDQSNS - @mlb_lib.MLB             66C6
DDRREG_VTTSNS        DDRREG_VTTSNS - @mlb_lib.MLB              66C6
DIMM_PROX_THRM_N     DIMM_PROX_THRM_N - @mlb_lib.MLB           52C3 52D8
DIMM_PROX_THRM_P     DIMM_PROX_THRM_P - @mlb_lib.MLB           52C3 52D8
DMI_CLK100M_CPU_N    DMI_CLK100M_CPU_N - @mlb_lib.MLB          11C2 17C1 81D3
DMI_CLK100M_CPU_P    DMI_CLK100M_CPU_P - @mlb_lib.MLB          11C2 17C1 81D3
DMI_N2S_N<0>         DMI_N2S_N<0> - @mlb_lib.MLB               10D8 18D8

DMI_N2S_N<3..0>      DMI_N2S_N<3..0> - @mlb_lib.MLB            81D3
DMI_N2S_N<1>         DMI_N2S_N<1> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_N<2>         DMI_N2S_N<2> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_N<3>         DMI_N2S_N<3> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_P<0>         DMI_N2S_P<0> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_P<3..0>      DMI_N2S_P<3..0> - @mlb_lib.MLB            81D3
DMI_N2S_P<1>         DMI_N2S_P<1> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_P<2>         DMI_N2S_P<2> - @mlb_lib.MLB               10D8 18D8
DMI_N2S_P<3>         DMI_N2S_P<3> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_N<0>         DMI_S2N_N<0> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_N<3..0>      DMI_S2N_N<3..0> - @mlb_lib.MLB            81D3
DMI_S2N_N<1>         DMI_S2N_N<1> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_N<2>         DMI_S2N_N<2> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_N<3>         DMI_S2N_N<3> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_P<0>         DMI_S2N_P<0> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_P<3..0>      DMI_S2N_P<3..0> - @mlb_lib.MLB            81D3
DMI_S2N_P<1>         DMI_S2N_P<1> - @mlb_lib.MLB               10D8 18D8
DMI_S2N_P<2>         DMI_S2N_P<2> - @mlb_lib.MLB               10D8 18C8
DMI_S2N_P<3>         DMI_S2N_P<3> - @mlb_lib.MLB               10D8 18C8
DPACONN_20_RC        DPACONN_20_RC - @mlb_lib.MLB              78A5
DPAPWRSW_CT          DPAPWRSW_CT - @mlb_lib.MLB                78D3
DPAPWRSW_HVEN_L_R    DPAPWRSW_HVEN_L_R - @mlb_lib.MLB          78D3
DPAPWRSW_IFLT        DPAPWRSW_IFLT - @mlb_lib.MLB              78D2
DPAPWRSW_ILIM        DPAPWRSW_ILIM - @mlb_lib.MLB              78D2
DPLL_REF_CLKN        DPLL_REF_CLKN - @mlb_lib.MLB              11C3
DPLL_REF_CLKP        DPLL_REF_CLKP - @mlb_lib.MLB              11C3
DPSDRVA_CEXT         DPSDRVA_CEXT - @mlb_lib.MLB               77B6
DPSDRVA_I2C_ADDR0    DPSDRVA_I2C_ADDR0 - @mlb_lib.MLB          77B7
DPSDRVA_I2C_ADDR1    DPSDRVA_I2C_ADDR1 - @mlb_lib.MLB          77B7
DPSDRVA_I2C_CTL_EN   DPSDRVA_I2C_CTL_EN - @mlb_lib.MLB         77B7
DPSDRVA_REXT         DPSDRVA_REXT - @mlb_lib.MLB               77B7
DP_AUXCH_ISOL        DP_AUXCH_ISOL - @mlb_lib.MLB              17C5 77B7
DP_AUX_CH_CK_N       DP_AUX_CH_CK_N - @mlb_lib.MLB             83D1
DP_AUX_CH_CK_P       DP_AUX_CH_CK_P - @mlb_lib.MLB             83D1
DP_AUX_CH_C_N        DP_AUX_CH_C_N - @mlb_lib.MLB              83D1
DP_AUX_CH_C_P        DP_AUX_CH_C_P - @mlb_lib.MLB              83D1
DP_A_BIAS            DP_A_BIAS - @mlb_lib.MLB                  76B5 77C3
DP_A_BIAS0N          DP_A_BIAS0N - @mlb_lib.MLB                76B3 77C1
DP_A_BIAS0P          DP_A_BIAS0P - @mlb_lib.MLB                76B3 77C1
DP_A_BIAS2N          DP_A_BIAS2N - @mlb_lib.MLB                76A3 77C1
DP_A_BIAS2P          DP_A_BIAS2P - @mlb_lib.MLB                76B3 77C1
DP_A_CA_DET          DP_A_CA_DET - @mlb_lib.MLB                77A7 77B5
DP_A_EXT_AUXCH_N     DP_A_EXT_AUXCH_N - @mlb_lib.MLB           77B1 78A7 83D1 86B3
DP_A_EXT_AUXCH_P     DP_A_EXT_AUXCH_P - @mlb_lib.MLB           77B1 78A7 83D1 86B3
DP_A_EXT_HPD         DP_A_EXT_HPD - @mlb_lib.MLB               77A4 77B1
DP_A_PWRDWN          DP_A_PWRDWN - @mlb_lib.MLB                77A8 77B3 77C4
DP_A_PWRDWN_FET_R    DP_A_PWRDWN_FET_R - @mlb_lib.MLB          78C6
DP_A_PWRDWN_INV      DP_A_PWRDWN_INV - @mlb_lib.MLB            78D5
DP_A_PWRDWN_R        DP_A_PWRDWN_R - @mlb_lib.MLB              77B7
DP_EG_AUX_CH_N       DP_EG_AUX_CH_N - @mlb_lib.MLB             88A1
DP_EG_AUX_CH_P       DP_EG_AUX_CH_P - @mlb_lib.MLB             88A1
DP_EXTA_AUXCH_C_N    DP_EXTA_AUXCH_C_N - @mlb_lib.MLB          8C5 77D8 83D1
                     =IG_DP_EXTA_AUXCH_C_N -                   8C8 18D1
                     @mlb_lib.MLB
DP_EXTA_AUXCH_C_P    DP_EXTA_AUXCH_C_P - @mlb_lib.MLB          8C5 77D8 83D1
                     =IG_DP_EXTA_AUXCH_C_P -                   8C8 18D1
                     @mlb_lib.MLB
DP_EXTA_AUXCH_N      DP_EXTA_AUXCH_N - @mlb_lib.MLB            77B7 77D6 83D1
DP_EXTA_AUXCH_P      DP_EXTA_AUXCH_P - @mlb_lib.MLB            77B7 77D6 83D1
DP_EXTA_DDC_CLK      DP_EXTA_DDC_CLK - @mlb_lib.MLB            8C5 77B4 77B7 83D1
                     =IG_DP_EXTA_DDC_CLK - @mlb_lib.MLB        8C8 18D1
DP_EXTA_DDC_CLK_AUX_ DP_EXTA_DDC_CLK_AUX_P -                   83D1
P                    @mlb_lib.MLB
DP_EXTA_DDC_DATA     DP_EXTA_DDC_DATA - @mlb_lib.MLB           8C5 77B4 77B7 83D1
                     =IG_DP_EXTA_DDC_DATA - @mlb_lib.MLB       8C8 18D1
DP_EXTA_DDC_DATA_AUX DP_EXTA_DDC_DATA_AUX_N -                  83D1
_N                   @mlb_lib.MLB
DP_EXTA_HPD          DP_EXTA_HPD - @mlb_lib.MLB                8C5 77B7 77B8 83D1
                     =IG_DP_EXTA_HPD - @mlb_lib.MLB            8C8 18D1
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                     =IG_DP_EXTA_ML_C_N<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_N<3..0> DP_EXTA_ML_C_N<3..0> - @mlb_lib.MLB       8C5 83D1
                     =IG_DP_EXTA_ML_C_N<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_N<1>    DP_EXTA_ML_C_N<1> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_N<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_N<2>    DP_EXTA_ML_C_N<2> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_N<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_N<3>    DP_EXTA_ML_C_N<3> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_N<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_P<0>    DP_EXTA_ML_C_P<0> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_P<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_P<3..0> DP_EXTA_ML_C_P<3..0> - @mlb_lib.MLB       8C5 83C1
                     =IG_DP_EXTA_ML_C_P<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_P<1>    DP_EXTA_ML_C_P<1> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_P<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_P<2>    DP_EXTA_ML_C_P<2> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_P<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_C_P<3>    DP_EXTA_ML_C_P<3> - @mlb_lib.MLB          77D8
                     =IG_DP_EXTA_ML_C_P<3..0> -                8C8
                     @mlb_lib.MLB
DP_EXTA_ML_N<0>      DP_EXTA_ML_N<0> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_N<3..0>   DP_EXTA_ML_N<3..0> - @mlb_lib.MLB         83C1
DP_EXTA_ML_N<1>      DP_EXTA_ML_N<1> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_N<2>      DP_EXTA_ML_N<2> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_N<3>      DP_EXTA_ML_N<3> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_P<0>      DP_EXTA_ML_P<0> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_P<3..0>   DP_EXTA_ML_P<3..0> - @mlb_lib.MLB         83C1
DP_EXTA_ML_P<1>      DP_EXTA_ML_P<1> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_P<2>      DP_EXTA_ML_P<2> - @mlb_lib.MLB            77C7 77D6
DP_EXTA_ML_P<3>      DP_EXTA_ML_P<3> - @mlb_lib.MLB            77C7 77D6
DP_ML_CK_N<3..0>     DP_ML_CK_N<3..0> - @mlb_lib.MLB           83C1
DP_ML_CK_P<3..0>     DP_ML_CK_P<3..0> - @mlb_lib.MLB           83C1
DP_ML_C_N<3..0>      DP_ML_C_N<3..0> - @mlb_lib.MLB            83C1
DP_ML_C_P<3..0>      DP_ML_C_P<3..0> - @mlb_lib.MLB            83C1
DP_SDRVA_AUXCH_C_N   DP_SDRVA_AUXCH_C_N - @mlb_lib.MLB         77B6 86B3
DP_SDRVA_AUXCH_C_P   DP_SDRVA_AUXCH_C_P - @mlb_lib.MLB         77B6 86B3
DP_SDRVA_AUXCH_N     DP_SDRVA_AUXCH_N - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_AUXCH_P     DP_SDRVA_AUXCH_P - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_HPD         DP_SDRVA_HPD - @mlb_lib.MLB               77B3
DP_SDRVA_ML_C_N<0>   DP_SDRVA_ML_C_N<0> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_N<3..0 DP_SDRVA_ML_C_N<3..0> -                   86B3
>                    @mlb_lib.MLB
DP_SDRVA_ML_C_N<1>   DP_SDRVA_ML_C_N<1> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_N<2>   DP_SDRVA_ML_C_N<2> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_N<3>   DP_SDRVA_ML_C_N<3> - @mlb_lib.MLB         77C6

DP_SDRVA_ML_C_P<0>   DP_SDRVA_ML_C_P<0> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_P<3..0 DP_SDRVA_ML_C_P<3..0> -                   86B3
>                    @mlb_lib.MLB
DP_SDRVA_ML_C_P<1>   DP_SDRVA_ML_C_P<1> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_P<2>   DP_SDRVA_ML_C_P<2> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_C_P<3>   DP_SDRVA_ML_C_P<3> - @mlb_lib.MLB         77C6
DP_SDRVA_ML_N<0>     DP_SDRVA_ML_N<0> - @mlb_lib.MLB           77C3 86B3
DP_SDRVA_ML_N<1>     DP_SDRVA_ML_N<1> - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_ML_N<2>     DP_SDRVA_ML_N<2> - @mlb_lib.MLB           77C3 86B3
DP_SDRVA_ML_N<3>     DP_SDRVA_ML_N<3> - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_ML_P<0>     DP_SDRVA_ML_P<0> - @mlb_lib.MLB           77C3 86B3
DP_SDRVA_ML_P<1>     DP_SDRVA_ML_P<1> - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_ML_P<2>     DP_SDRVA_ML_P<2> - @mlb_lib.MLB           77C3 86B3
DP_SDRVA_ML_P<3>     DP_SDRVA_ML_P<3> - @mlb_lib.MLB           77B3 86B3
DP_SDRVA_ML_R_N<0>   DP_SDRVA_ML_R_N<0> - @mlb_lib.MLB         77C4
DP_SDRVA_ML_R_N<3..0 DP_SDRVA_ML_R_N<3..0> -                   86B3
>                    @mlb_lib.MLB
DP_SDRVA_ML_R_N<2>   DP_SDRVA_ML_R_N<2> - @mlb_lib.MLB         77C4
DP_SDRVA_ML_R_P<0>   DP_SDRVA_ML_R_P<0> - @mlb_lib.MLB         77C4
DP_SDRVA_ML_R_P<3..0 DP_SDRVA_ML_R_P<3..0> -                   86B3
>                    @mlb_lib.MLB
DP_SDRVA_ML_R_P<2>   DP_SDRVA_ML_R_P<2> - @mlb_lib.MLB         77C4
DP_T29SNK0_AUXCH_C_N DP_T29SNK0_AUXCH_C_N - @mlb_lib.MLB       8B5 74B8 83D1
                     =IG_DP_T29SNK0_AUXCH_C_N -                8B8 18C1
                     @mlb_lib.MLB
DP_T29SNK0_AUXCH_C_P DP_T29SNK0_AUXCH_C_P - @mlb_lib.MLB       8B5 74B8 83D1
                     =IG_DP_T29SNK0_AUXCH_C_P -                8B8 18C1
                     @mlb_lib.MLB
DP_T29SNK0_AUXCH_N   DP_T29SNK0_AUXCH_N - @mlb_lib.MLB         74B5 74B6 83D1
DP_T29SNK0_AUXCH_P   DP_T29SNK0_AUXCH_P - @mlb_lib.MLB         74B5 74B6 83D1
DP_T29SNK0_DDC_CLK   DP_T29SNK0_DDC_CLK - @mlb_lib.MLB         83C1
DP_T29SNK0_DDC_DATA  DP_T29SNK0_DDC_DATA - @mlb_lib.MLB        83C1
DP_T29SNK0_HPD       DP_T29SNK0_HPD - @mlb_lib.MLB             8B5 74B6 83C1
                     =IG_DP_T29SNK0_HPD - @mlb_lib.MLB         8B8 18C1
DP_T29SNK0_ML_C_N<0> DP_T29SNK0_ML_C_N<0> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_N<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_N<3. DP_T29SNK0_ML_C_N<3..0> -                 8B5 83C1
.0>                  @mlb_lib.MLB
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                     @mlb_lib.MLB
DP_T29SNK0_ML_C_N<1> DP_T29SNK0_ML_C_N<1> - @mlb_lib.MLB       74B8
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                     @mlb_lib.MLB
DP_T29SNK0_ML_C_N<2> DP_T29SNK0_ML_C_N<2> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_N<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_N<3> DP_T29SNK0_ML_C_N<3> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_N<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_P<0> DP_T29SNK0_ML_C_P<0> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_P<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_P<3. DP_T29SNK0_ML_C_P<3..0> -                 8B5 83C1
.0>                  @mlb_lib.MLB
                     =IG_DP_T29SNK0_ML_C_P<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_P<1> DP_T29SNK0_ML_C_P<1> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_P<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_P<2> DP_T29SNK0_ML_C_P<2> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_P<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_C_P<3> DP_T29SNK0_ML_C_P<3> - @mlb_lib.MLB       74B8
                     =IG_DP_T29SNK0_ML_C_P<3..0> -             8B8
                     @mlb_lib.MLB
DP_T29SNK0_ML_N<0>   DP_T29SNK0_ML_N<0> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_N<3..0 DP_T29SNK0_ML_N<3..0> -                   83C1
>                    @mlb_lib.MLB
DP_T29SNK0_ML_N<1>   DP_T29SNK0_ML_N<1> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_N<2>   DP_T29SNK0_ML_N<2> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_N<3>   DP_T29SNK0_ML_N<3> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_P<0>   DP_T29SNK0_ML_P<0> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_P<3..0 DP_T29SNK0_ML_P<3..0> -                   83C1
>                    @mlb_lib.MLB
DP_T29SNK0_ML_P<1>   DP_T29SNK0_ML_P<1> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_P<2>   DP_T29SNK0_ML_P<2> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK0_ML_P<3>   DP_T29SNK0_ML_P<3> - @mlb_lib.MLB         74B5 74B6
DP_T29SNK1_AUXCH_C_N DP_T29SNK1_AUXCH_C_N - @mlb_lib.MLB       83C1
DP_T29SNK1_AUXCH_C_P DP_T29SNK1_AUXCH_C_P - @mlb_lib.MLB       83C1
DP_T29SNK1_AUXCH_N   DP_T29SNK1_AUXCH_N - @mlb_lib.MLB         83C1
DP_T29SNK1_AUXCH_P   DP_T29SNK1_AUXCH_P - @mlb_lib.MLB         83C1
DP_T29SNK1_HPD       DP_T29SNK1_HPD - @mlb_lib.MLB             83C1
DP_T29SNK1_ML_C_N<3. DP_T29SNK1_ML_C_N<3..0> -                 83C1
.0>                  @mlb_lib.MLB
DP_T29SNK1_ML_C_P<3. DP_T29SNK1_ML_C_P<3..0> -                 83C1
.0>                  @mlb_lib.MLB
DP_T29SNK1_ML_N<3..0 DP_T29SNK1_ML_N<3..0> -                   83C1
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DP_T29SNK1_ML_P<3..0 DP_T29SNK1_ML_P<3..0> -                   83C1
>                    @mlb_lib.MLB
EDP_COMP             EDP_COMP - @mlb_lib.MLB                   10C7
ENET_ASF_GPIO        ENET_ASF_GPIO - @mlb_lib.MLB              37B1 46B5
ENET_ASF_GPIO_R      ENET_ASF_GPIO_R - @mlb_lib.MLB            37B3
ENET_ASF_SMB_CLK     ENET_ASF_SMB_CLK - @mlb_lib.MLB           37B6 49D3 87D3
                     =SMBUS_SMC_2_SCL - @mlb_lib.MLB           46B5 49D1
ENET_ASF_SMB_DATA    ENET_ASF_SMB_DATA - @mlb_lib.MLB          37B6 49D3 87D3
                     =SMBUS_SMC_2_SDA - @mlb_lib.MLB           46B5 49D1
ENET_CENTER_TAP<0>   ENET_CENTER_TAP<0> - @mlb_lib.MLB         36B5
ENET_CENTER_TAP<3..0 ENET_CENTER_TAP<3..0> -                   85D3
>                    @mlb_lib.MLB
ENET_CENTER_TAP<1>   ENET_CENTER_TAP<1> - @mlb_lib.MLB         36C4
ENET_CENTER_TAP<2>   ENET_CENTER_TAP<2> - @mlb_lib.MLB         36B5
ENET_CENTER_TAP<3>   ENET_CENTER_TAP<3> - @mlb_lib.MLB         36C4
ENET_CLKREQ_L        ENET_CLKREQ_L - @mlb_lib.MLB              17B4 17B5 37B6
ENET_CMODE_REF       ENET_CMODE_REF - @mlb_lib.MLB             36B4 85D3
ENET_CONN_CTAP       ENET_CONN_CTAP - @mlb_lib.MLB             36D5
ENET_CR_CLK          ENET_CR_CLK - @mlb_lib.MLB                37B3 85C3
ENET_CR_CMD          ENET_CR_CMD - @mlb_lib.MLB                37B3 85C3
ENET_CR_DATA<0>      ENET_CR_DATA<0> - @mlb_lib.MLB            37B3
ENET_CR_DATA<7..0>   ENET_CR_DATA<7..0> - @mlb_lib.MLB         85C3
ENET_CR_DATA<1>      ENET_CR_DATA<1> - @mlb_lib.MLB            37B3
ENET_CR_DATA<2>      ENET_CR_DATA<2> - @mlb_lib.MLB            37B3
ENET_CR_DATA<3>      ENET_CR_DATA<3> - @mlb_lib.MLB            37B3
ENET_CR_DATA<4>      ENET_CR_DATA<4> - @mlb_lib.MLB            37B3
ENET_CR_DATA<5>      ENET_CR_DATA<5> - @mlb_lib.MLB            37B3
ENET_CR_DATA<6>      ENET_CR_DATA<6> - @mlb_lib.MLB            37B3
ENET_CR_DATA<7>      ENET_CR_DATA<7> - @mlb_lib.MLB            37B3
ENET_CR_DETECT_L     ENET_CR_DETECT_L - @mlb_lib.MLB           34B2 37B1
ENET_CR_PWREN        ENET_CR_PWREN - @mlb_lib.MLB              34D4 37B3
ENET_LOW_PWR         ENET_LOW_PWR - @mlb_lib.MLB               20C1 34B5 37B6
ENET_LOW_PWR_PCH     ENET_LOW_PWR_PCH - @mlb_lib.MLB           20A1 20C3 20C6
ENET_MDI_N<0>        ENET_MDI_N<0> - @mlb_lib.MLB              36B8 37C3
ENET_MDI_N<3..0>     ENET_MDI_N<3..0> - @mlb_lib.MLB           85D3
```

ENET_MDI_N<1>	ENET_MDI_N<1> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_N<2>	ENET_MDI_N<2> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_N<3>	ENET_MDI_N<3> - @mlb_lib.MLB	36B8 37B3
ENET_MDI_P<0>	ENET_MDI_P<0> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<3..0>	ENET_MDI_P<3..0> - @mlb_lib.MLB	85D3
ENET_MDI_P<1>	ENET_MDI_P<1> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<2>	ENET_MDI_P<2> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<3>	ENET_MDI_P<3> - @mlb_lib.MLB	36B8 37C3
ENET_MDI_TRAN_N<0>	ENET_MDI_TRAN_N<0> - @mlb_lib.MLB	36B3
ENET_MDI_TRAN_N<3..0>	ENET_MDI_TRAN_N<3..0> - @mlb_lib.MLB	85D3
ENET_MDI_TRAN_N<1>	ENET_MDI_TRAN_N<1> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_N<2>	ENET_MDI_TRAN_N<2> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_N<3>	ENET_MDI_TRAN_N<3> - @mlb_lib.MLB	36B3
ENET_MDI_TRAN_P<0>	ENET_MDI_TRAN_P<0> - @mlb_lib.MLB	36C3
ENET_MDI_TRAN_P<3..0>	ENET_MDI_TRAN_P<3..0> - @mlb_lib.MLB	85D3
ENET_MDI_TRAN_P<1>	ENET_MDI_TRAN_P<1> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_P<2>	ENET_MDI_TRAN_P<2> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_P<3>	ENET_MDI_TRAN_P<3> - @mlb_lib.MLB	36B3
ENET_MEDIA_SENSE	ENET_MEDIA_SENSE - @mlb_lib.MLB	37B1 38B5
ENET_MEDIA_SENSE_RDIV	ENET_MEDIA_SENSE_RDIV - @mlb_lib.MLB	17C8 38B3
ENET_MSNS_EN	ENET_MSNS_EN - @mlb_lib.MLB	38A4
ENET_MSNS_EN_L	ENET_MSNS_EN_L - @mlb_lib.MLB	38A4
ENET_PWR_EN	ENET_PWR_EN - @mlb_lib.MLB	19C1 24D4
ENET_RESET_L	ENET_RESET_L - @mlb_lib.MLB	27D1 34B8 85D3
ENET_SR_LX	ENET_SR_LX - @mlb_lib.MLB	37D4 38D5
ENET_SR_VFB	ENET_SR_VFB - @mlb_lib.MLB	37D4 38C5
ENET_WAKE_L	ENET_WAKE_L - @mlb_lib.MLB	37B8 38C1
EXCARD_CLKREQ_L	EXCARD_CLKREQ_L - @mlb_lib.MLB	17B4 17B5
FAN0_CTL_F	FAN0_CTL_F - @mlb_lib.MLB	60C3 91D5
FAN0_TACH_F	FAN0_TACH_F - @mlb_lib.MLB	60C3 91D5
FAN_S0_EN_L	FAN_S0_EN_L - @mlb_lib.MLB	60C6
FAN_S0_EN_L_G	FAN_S0_EN_L_G - @mlb_lib.MLB	60C5
FAN_TACH0	FAN_TACH0 - @mlb_lib.MLB	60C7
FB_1V8S0	FB_1V8S0 - @mlb_lib.MLB	71C7
FB_B0_A<8..0>	FB_B0_A<8..0> - @mlb_lib.MLB	88D1
FB_B0_ABI_L	FB_B0_ABI_L - @mlb_lib.MLB	88D1
FB_B0_CAS_L	FB_B0_CAS_L - @mlb_lib.MLB	88D1
FB_B0_CKE_L	FB_B0_CKE_L - @mlb_lib.MLB	88D1
FB_B0_CLK_N	FB_B0_CLK_N - @mlb_lib.MLB	88D1
FB_B0_CLK_P	FB_B0_CLK_P - @mlb_lib.MLB	88D1
FB_B0_CS_L	FB_B0_CS_L - @mlb_lib.MLB	88D1
FB_B0_DBI_L<0>	FB_B0_DBI_L<0> - @mlb_lib.MLB	88C1
FB_B0_DBI_L<1>	FB_B0_DBI_L<1> - @mlb_lib.MLB	88C1
FB_B0_DBI_L<2>	FB_B0_DBI_L<2> - @mlb_lib.MLB	88C1
FB_B0_DBI_L<3>	FB_B0_DBI_L<3> - @mlb_lib.MLB	88C1
FB_B0_DQ<7..0>	FB_B0_DQ<7..0> - @mlb_lib.MLB	88C1
FB_B0_DQ<15..8>	FB_B0_DQ<15..8> - @mlb_lib.MLB	88C1
FB_B0_DQ<23..16>	FB_B0_DQ<23..16> - @mlb_lib.MLB	88C1
FB_B0_DQ<31..24>	FB_B0_DQ<31..24> - @mlb_lib.MLB	88C1
FB_B0_EDC<0>	FB_B0_EDC<0> - @mlb_lib.MLB	88D1
FB_B0_EDC<1>	FB_B0_EDC<1> - @mlb_lib.MLB	88D1
FB_B0_EDC<2>	FB_B0_EDC<2> - @mlb_lib.MLB	88D1
FB_B0_EDC<3>	FB_B0_EDC<3> - @mlb_lib.MLB	88C1
FB_B0_RAS_L	FB_B0_RAS_L - @mlb_lib.MLB	88D1
FB_B0_WCLK_N<0>	FB_B0_WCLK_N<0> - @mlb_lib.MLB	88C1
FB_B0_WCLK_N<1>	FB_B0_WCLK_N<1> - @mlb_lib.MLB	88C1
FB_B0_WCLK_P<0>	FB_B0_WCLK_P<0> - @mlb_lib.MLB	88C1
FB_B0_WCLK_P<1>	FB_B0_WCLK_P<1> - @mlb_lib.MLB	88C1
FB_B0_WE_L	FB_B0_WE_L - @mlb_lib.MLB	88D1
FB_B1_A<8..0>	FB_B1_A<8..0> - @mlb_lib.MLB	88D1
FB_B1_ABI_L	FB_B1_ABI_L - @mlb_lib.MLB	88D1
FB_B1_CAS_L	FB_B1_CAS_L - @mlb_lib.MLB	88D1
FB_B1_CKE_L	FB_B1_CKE_L - @mlb_lib.MLB	88D1
FB_B1_CLK_N	FB_B1_CLK_N - @mlb_lib.MLB	88D1
FB_B1_CLK_P	FB_B1_CLK_P - @mlb_lib.MLB	88D1
FB_B1_CS_L	FB_B1_CS_L - @mlb_lib.MLB	88D1
FB_B1_DBI_L<0>	FB_B1_DBI_L<0> - @mlb_lib.MLB	88C1
FB_B1_DBI_L<1>	FB_B1_DBI_L<1> - @mlb_lib.MLB	88C1
FB_B1_DBI_L<2>	FB_B1_DBI_L<2> - @mlb_lib.MLB	88C1
FB_B1_DBI_L<3>	FB_B1_DBI_L<3> - @mlb_lib.MLB	88C1
FB_B1_DQ<7..0>	FB_B1_DQ<7..0> - @mlb_lib.MLB	88C1
FB_B1_DQ<15..8>	FB_B1_DQ<15..8> - @mlb_lib.MLB	88C1
FB_B1_DQ<23..16>	FB_B1_DQ<23..16> - @mlb_lib.MLB	88B1
FB_B1_DQ<31..24>	FB_B1_DQ<31..24> - @mlb_lib.MLB	88B1
FB_B1_EDC<0>	FB_B1_EDC<0> - @mlb_lib.MLB	88C1
FB_B1_EDC<1>	FB_B1_EDC<1> - @mlb_lib.MLB	88C1
FB_B1_EDC<2>	FB_B1_EDC<2> - @mlb_lib.MLB	88C1
FB_B1_EDC<3>	FB_B1_EDC<3> - @mlb_lib.MLB	88C1
FB_B1_RAS_L	FB_B1_RAS_L - @mlb_lib.MLB	88D1
FB_B1_WCLK_N<0>	FB_B1_WCLK_N<0> - @mlb_lib.MLB	88C1
FB_B1_WCLK_N<1>	FB_B1_WCLK_N<1> - @mlb_lib.MLB	88C1
FB_B1_WCLK_P<0>	FB_B1_WCLK_P<0> - @mlb_lib.MLB	88C1
FB_B1_WCLK_P<1>	FB_B1_WCLK_P<1> - @mlb_lib.MLB	88C1
FB_B1_WE_L	FB_B1_WE_L - @mlb_lib.MLB	88D1
FB_RESET_L	FB_RESET_L - @mlb_lib.MLB	88B1
FDI_DATA_N<0>	FDI_DATA_N<0> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<7..0>	FDI_DATA_N<7..0> - @mlb_lib.MLB	8D5 81D3
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<1>	FDI_DATA_N<1> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<2>	FDI_DATA_N<2> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<3>	FDI_DATA_N<3> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<4>	FDI_DATA_N<4> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<5>	FDI_DATA_N<5> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<6>	FDI_DATA_N<6> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_N<7>	FDI_DATA_N<7> - @mlb_lib.MLB	18D5
	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<0>	FDI_DATA_P<0> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<7..0>	FDI_DATA_P<7..0> - @mlb_lib.MLB	8D5 81D3
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<1>	FDI_DATA_P<1> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<2>	FDI_DATA_P<2> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<3>	FDI_DATA_P<3> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<4>	FDI_DATA_P<4> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<5>	FDI_DATA_P<5> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<6>	FDI_DATA_P<6> - @mlb_lib.MLB	18D5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_DATA_P<7>	FDI_DATA_P<7> - @mlb_lib.MLB	18C5
	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D8
FDI_FSYNC<0>	FDI_FSYNC<0> - @mlb_lib.MLB	18C5
	=FDI_FSYNC<1..0> - @mlb_lib.MLB	8D8
FDI_FSYNC<1..0>	FDI_FSYNC<1..0> - @mlb_lib.MLB	8D5 81D3
	=FDI_FSYNC<1..0> - @mlb_lib.MLB	8D8
FDI_FSYNC<1>	FDI_FSYNC<1> - @mlb_lib.MLB	18C5
	=FDI_FSYNC<1..0> - @mlb_lib.MLB	8D8
FDI_INT	FDI_INT - @mlb_lib.MLB	8D5 18C5 81D3
	=FDI_INT - @mlb_lib.MLB	8D8 10C8
FDI_LSYNC<0>	FDI_LSYNC<0> - @mlb_lib.MLB	18C5
	=FDI_LSYNC<1..0> - @mlb_lib.MLB	8D8
FDI_LSYNC<1..0>	FDI_LSYNC<1..0> - @mlb_lib.MLB	8D5 81D3
	=FDI_LSYNC<1..0> - @mlb_lib.MLB	8D8
FDI_LSYNC<1>	FDI_LSYNC<1> - @mlb_lib.MLB	18C5
	=FDI_LSYNC<1..0> - @mlb_lib.MLB	8D8
FWOHCI_CLK98M_LCLK	FWOHCI_CLK98M_LCLK - @mlb_lib.MLB	39C3
FWOHCI_LINKON_L	FWOHCI_LINKON_L - @mlb_lib.MLB	39C3
FWOHCI_LPS	FWOHCI_LPS - @mlb_lib.MLB	39B3
FWOHCI_LREQ	FWOHCI_LREQ - @mlb_lib.MLB	39B3
FWPHY_BMODE	FWPHY_BMODE - @mlb_lib.MLB	39A6
FWPHY_CLK98M_PCLK	FWPHY_CLK98M_PCLK - @mlb_lib.MLB	39B3
FWPHY_CPS	FWPHY_CPS - @mlb_lib.MLB	39B3
FWPHY_LKON_DS2	FWPHY_LKON_DS2 - @mlb_lib.MLB	39C3
FWPHY_PINT	FWPHY_PINT - @mlb_lib.MLB	39B3
FWPHY_R0	FWPHY_R0 - @mlb_lib.MLB	39B3
FWPHY_R1	FWPHY_R1 - @mlb_lib.MLB	39B3
FWPHY_RESET_L	FWPHY_RESET_L - @mlb_lib.MLB	39A3
FWPHY_TESTM	FWPHY_TESTM - @mlb_lib.MLB	39A6
FWPHY_TESTW	FWPHY_TESTW - @mlb_lib.MLB	39A6
FWXIO_CYCLEOUT	FWXIO_CYCLEOUT - @mlb_lib.MLB	39B6
FWXIO_JTAG_TCK	FWXIO_JTAG_TCK - @mlb_lib.MLB	39B6
FWXIO_JTAG_TRST	FWXIO_JTAG_TRST - @mlb_lib.MLB	39A6
FWXIO_REF0_PCIE	FWXIO_REF0_PCIE - @mlb_lib.MLB	39C6
FWXIO_REF1_PCIE	FWXIO_REF1_PCIE - @mlb_lib.MLB	39C6
FWXIO_REFCLK_SEL	FWXIO_REFCLK_SEL - @mlb_lib.MLB	39B6
FWXIO_REF_PCIE	FWXIO_REF_PCIE - @mlb_lib.MLB	39C7
FWXIO_SCL	FWXIO_SCL - @mlb_lib.MLB	39B6
FWXIO_SDA	FWXIO_SDA - @mlb_lib.MLB	39B6
FWXIO_SNOOP_EN	FWXIO_SNOOP_EN - @mlb_lib.MLB	39A6
FWXIO_VDD15COMB	FWXIO_VDD15COMB - @mlb_lib.MLB	39C3
FWXIO_VDD33COMB	FWXIO_VDD33COMB - @mlb_lib.MLB	39C3
FWXIO_VDD33COMIO	FWXIO_VDD33COMIO - @mlb_lib.MLB	39C3
FWXIO_VREG_PD33	FWXIO_VREG_PD33 - @mlb_lib.MLB	39A6
FW_CLKREQ_L	FW_CLKREQ_L - @mlb_lib.MLB	17B5 17C4 39C6
FW_CUTOFF	FW_CUTOFF - @mlb_lib.MLB	41A6 41C8
FW_EN_A	FW_EN_A - @mlb_lib.MLB	41C7
FW_EN_B	FW_EN_B - @mlb_lib.MLB	41C7
FW_FETGATE	FW_FETGATE - @mlb_lib.MLB	41D7
FW_FETV	FW_FETV - @mlb_lib.MLB	41C6
FW_FET_TEMP	FW_FET_TEMP - @mlb_lib.MLB	41A8 41B7
FW_FET_TREF	FW_FET_TREF - @mlb_lib.MLB	41A8
FW_IREF	FW_IREF - @mlb_lib.MLB	41C5
FW_LATEVG_L	FW_LATEVG_L - @mlb_lib.MLB	41A4
FW_LATEVG_PP2V4_RC	FW_LATEVG_PP2V4_RC - @mlb_lib.MLB	41A5
FW_LATEVG_REF	FW_LATEVG_REF - @mlb_lib.MLB	41A5
FW_OC_DR	FW_OC_DR - @mlb_lib.MLB	41C7
FW_P0_TPA_C	FW_P0_TPA_C - @mlb_lib.MLB	40C3
FW_P0_TPA_L_N	FW_P0_TPA_L_N - @mlb_lib.MLB	40D2 85B3
FW_P0_TPA_L_P	FW_P0_TPA_L_P - @mlb_lib.MLB	40D3 85B3
FW_P0_TPBIAS	FW_P0_TPBIAS - @mlb_lib.MLB	39A2 40D4
FW_P0_TPB_L_N	FW_P0_TPB_L_N - @mlb_lib.MLB	40C3 85B3
FW_P0_TPB_L_P	FW_P0_TPB_L_P - @mlb_lib.MLB	40C2 85B3
FW_P12V_FETPWR	FW_P12V_FETPWR - @mlb_lib.MLB	41C6
FW_PHY_DS0	FW_PHY_DS0 - @mlb_lib.MLB	39C2 40B7
FW_PHY_DS1	FW_PHY_DS1 - @mlb_lib.MLB	39C2 40B7
FW_PHY_PC0	FW_PHY_PC0 - @mlb_lib.MLB	39C2 40A7
FW_PME_L	FW_PME_L - @mlb_lib.MLB	20B6 20D6 39B6
FW_PORT0_TPAL_N	FW_PORT0_TPAL_N - @mlb_lib.MLB	41C2 85B3
FW_PORT0_TPAL_P	FW_PORT0_TPAL_P - @mlb_lib.MLB	41C2 85B3
FW_PORT0_TPA_N	FW_PORT0_TPA_N - @mlb_lib.MLB	40C1 41C4 85B3
	FW_P0_TPA_N - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPA_P	FW_PORT0_TPA_P - @mlb_lib.MLB	40C1 41C4 85B3
	FW_P0_TPA_P - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPA_R	FW_PORT0_TPA_R - @mlb_lib.MLB	41C2
FW_PORT0_TPBL_N	FW_PORT0_TPBL_N - @mlb_lib.MLB	41C2 85B3
FW_PORT0_TPBL_P	FW_PORT0_TPBL_P - @mlb_lib.MLB	41C2 85B3
FW_PORT0_TPB_N	FW_PORT0_TPB_N - @mlb_lib.MLB	40C1 41C4 85B3
	FW_P0_TPB_N - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPB_P	FW_PORT0_TPB_P - @mlb_lib.MLB	40C1 41C4 85B3
	FW_P0_TPB_P - @mlb_lib.MLB	39A2 40C3
FW_PORT0_VP	FW_PORT0_VP - @mlb_lib.MLB	41D2 91B5
FW_PORT0_VP_F	FW_PORT0_VP_F - @mlb_lib.MLB	41D2
FW_PORTPWR_DISABLE_L	FW_PORTPWR_DISABLE_L - @mlb_lib.MLB	41A3 41C8
FW_PWR_EN	FW_PWR_EN - @mlb_lib.MLB	20B6 20C6
FW_REF_A	FW_REF_A - @mlb_lib.MLB	41B5
FW_REF_B	FW_REF_B - @mlb_lib.MLB	41B5
FW_RESET_L	FW_RESET_L - @mlb_lib.MLB	27D1 39C6
FW_SNSN	FW_SNSN - @mlb_lib.MLB	41D7
FW_SNSP	FW_SNSP - @mlb_lib.MLB	41D8
FW_V_PD	FW_V_PD - @mlb_lib.MLB	41C5
G3_POWERON_L	G3_POWERON_L - @mlb_lib.MLB	44C7 46B5 47C2
G3_POWERON_R_L	G3_POWERON_R_L - @mlb_lib.MLB	44C6
GFXIMVP_IMON	GFXIMVP_IMON - @mlb_lib.MLB	81A3
GFXVSENSE_IN	GFXVSENSE_IN - @mlb_lib.MLB	50B3
GFX_DPRSLPVR	GFX_DPRSLPVR - @mlb_lib.MLB	81A3
GFX_VID<6..0>	GFX_VID<6..0> - @mlb_lib.MLB	81A3
GFX_VR_EN	GFX_VR_EN - @mlb_lib.MLB	81A3
GMUX_INT	GMUX_INT - @mlb_lib.MLB	20D6 20D8
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @mlb_lib.MLB	53A3 53B7 53D1 53D2 54C6 57C1 58A4 58A4 58A7 58B3 58B8 58B8 58C4
GND_AUDIO_HPAMP	GND_AUDIO_HPAMP - @mlb_lib.MLB	53A3 55A6 55C7
GND_CHASSIS_AUDIO_JACK	GND_CHASSIS_AUDIO_JACK - @mlb_lib.MLB	57A3 57B3 57C3
GND_DDRREG_SGND	GND_DDRREG_SGND - @mlb_lib.MLB	66B7
GND_DPACONN_1	GND_DPACONN_1 - @mlb_lib.MLB	78C3
GND_DPACONN_7	GND_DPACONN_7 - @mlb_lib.MLB	78B3
GND_DPACONN_8	GND_DPACONN_8 - @mlb_lib.MLB	78B6
GND_DPACONN_13	GND_DPACONN_13 - @mlb_lib.MLB	78B3
GND_DPACONN_14	GND_DPACONN_14 - @mlb_lib.MLB	78B6
GND_DPACONN_19	GND_DPACONN_19 - @mlb_lib.MLB	78A3
GND_IR_F	GND_IR_F - @mlb_lib.MLB	45C2
GND_SMC_AVSS	GND_SMC_AVSS - @mlb_lib.MLB	46C2 47D6 50A2 50A5 50A6 50B1 50B5 50B5 50C2 50C5 50D1 50D5 51C2 51C5 51D5
GPIO29_SLP_LAN_L	GPIO29_SLP_LAN_L - @mlb_lib.MLB	18A6 18C5
GPUTHMSNS_D_N	GPUTHMSNS_D_N - @mlb_lib.MLB	89B1
GPUTHMSNS_D_P	GPUTHMSNS_D_P - @mlb_lib.MLB	89B1
GPU_CLK27M	GPU_CLK27M - @mlb_lib.MLB	88B1
GPU_CLK100M	GPU_CLK100M - @mlb_lib.MLB	88B1
GPU_CLK_TEST_N	GPU_CLK_TEST_N - @mlb_lib.MLB	88B1
GPU_CLK_TEST_P	GPU_CLK_TEST_P - @mlb_lib.MLB	88B1
GPU_TDIODE_N	GPU_TDIODE_N - @mlb_lib.MLB	89B1
GPU_TDIODE_P	GPU_TDIODE_P - @mlb_lib.MLB	89B1
HDA_BIT_CLK	HDA_BIT_CLK - @mlb_lib.MLB	17A4 53C7 84C3
HDA_BIT_CLK_R	HDA_BIT_CLK_R - @mlb_lib.MLB	17A5 17D8 84C3
HDA_RST_L	HDA_RST_L - @mlb_lib.MLB	17A4 53C7 84C3
HDA_RST_R_L	HDA_RST_R_L - @mlb_lib.MLB	17A5 17D8 84C3
HDA_SDIN0	HDA_SDIN0 - @mlb_lib.MLB	17D8 53C7 84C3
HDA_SDOUT	HDA_SDOUT - @mlb_lib.MLB	17A4 53C7 84C3
HDA_SDOUT_R	HDA_SDOUT_R - @mlb_lib.MLB	17A3 17A5 17C8 84C3
HDA_SYNC	HDA_SYNC - @mlb_lib.MLB	17A4 53C7 84C3
HDA_SYNC_R	HDA_SYNC_R - @mlb_lib.MLB	17A3 17A5 17D8 84C3
HDD_THRMD_N	HDD_THRMD_N - @mlb_lib.MLB	91A7
HDD_THRMD_P	HDD_THRMD_P - @mlb_lib.MLB	91A7
HDMI_CLK_CONN_N	HDMI_CLK_CONN_N - @mlb_lib.MLB	80B5 80C1 83B1
HDMI_CLK_CONN_P	HDMI_CLK_CONN_P - @mlb_lib.MLB	80C1 80C5 83B1
HDMI_CLK_C_N	HDMI_CLK_C_N - @mlb_lib.MLB	8C5 79D8 83B1
	=IG_HDMI_CLK_C_N - @mlb_lib.MLB	8C8 18B1
HDMI_CLK_C_P	HDMI_CLK_C_P - @mlb_lib.MLB	8C5 79D8 83B1
	=IG_HDMI_CLK_C_P - @mlb_lib.MLB	8C8 18B1
HDMI_CLK_LS_N	HDMI_CLK_LS_N - @mlb_lib.MLB	79D6 83B1
HDMI_CLK_LS_P	HDMI_CLK_LS_P - @mlb_lib.MLB	79D6 83B1
HDMI_CLK_N	HDMI_CLK_N - @mlb_lib.MLB	79D2 80B8 83B1
HDMI_CLK_P	HDMI_CLK_P - @mlb_lib.MLB	79D2 80C8 83B1
HDMI_DATA_CONN_N<0>	HDMI_DATA_CONN_N<0> - @mlb_lib.MLB	80C4 80D5
HDMI_DATA_CONN_N<2..0>	HDMI_DATA_CONN_N<2..0> - @mlb_lib.MLB	83B1
HDMI_DATA_CONN_N<1>	HDMI_DATA_CONN_N<1> - @mlb_lib.MLB	80C1 80C5
HDMI_DATA_CONN_N<2>	HDMI_DATA_CONN_N<2> - @mlb_lib.MLB	80C4 80C5
HDMI_DATA_CONN_P<0>	HDMI_DATA_CONN_P<0> - @mlb_lib.MLB	80C4 80D5
HDMI_DATA_CONN_P<2..0>	HDMI_DATA_CONN_P<2..0> - @mlb_lib.MLB	83B1
HDMI_DATA_CONN_P<1>	HDMI_DATA_CONN_P<1> - @mlb_lib.MLB	80C1 80D5
HDMI_DATA_CONN_P<2>	HDMI_DATA_CONN_P<2> - @mlb_lib.MLB	80C4 80C5
HDMI_DATA_C_N<0>	HDMI_DATA_C_N<0> - @mlb_lib.MLB	79C8
	=IG_HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_N<2..0>	HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8C5 83B1
	=IG_HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_N<1>	HDMI_DATA_C_N<1> - @mlb_lib.MLB	79C8
	=IG_HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_N<2>	HDMI_DATA_C_N<2> - @mlb_lib.MLB	79C8
	=IG_HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_P<0>	HDMI_DATA_C_P<0> - @mlb_lib.MLB	79D8
	=IG_HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_P<2..0>	HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8C5 83A1
	=IG_HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_P<1>	HDMI_DATA_C_P<1> - @mlb_lib.MLB	79C8
	=IG_HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_C_P<2>	HDMI_DATA_C_P<2> - @mlb_lib.MLB	79C8
	=IG_HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8C8
HDMI_DATA_LS_N<0>	HDMI_DATA_LS_N<0> - @mlb_lib.MLB	79C6
HDMI_DATA_LS_N<2..0>	HDMI_DATA_LS_N<2..0> - @mlb_lib.MLB	83A1
HDMI_DATA_LS_N<1>	HDMI_DATA_LS_N<1> - @mlb_lib.MLB	79C6
HDMI_DATA_LS_N<2>	HDMI_DATA_LS_N<2> - @mlb_lib.MLB	79C6
HDMI_DATA_LS_P<0>	HDMI_DATA_LS_P<0> - @mlb_lib.MLB	79D6
HDMI_DATA_LS_P<2..0>	HDMI_DATA_LS_P<2..0> - @mlb_lib.MLB	83A1
HDMI_DATA_LS_P<1>	HDMI_DATA_LS_P<1> - @mlb_lib.MLB	79C6
HDMI_DATA_LS_P<2>	HDMI_DATA_LS_P<2> - @mlb_lib.MLB	79C6
HDMI_DATA_N<0>	HDMI_DATA_N<0> - @mlb_lib.MLB	79C2 80D8
HDMI_DATA_N<2..0>	HDMI_DATA_N<2..0> - @mlb_lib.MLB	83A1
HDMI_DATA_N<1>	HDMI_DATA_N<1> - @mlb_lib.MLB	79C2 80C8
HDMI_DATA_N<2>	HDMI_DATA_N<2> - @mlb_lib.MLB	79C2 80C8
HDMI_DATA_P<0>	HDMI_DATA_P<0> - @mlb_lib.MLB	79D2 80D8
HDMI_DATA_P<2..0>	HDMI_DATA_P<2..0> - @mlb_lib.MLB	83A1
HDMI_DATA_P<1>	HDMI_DATA_P<1> - @mlb_lib.MLB	79C2 80D8
HDMI_DATA_P<2>	HDMI_DATA_P<2> - @mlb_lib.MLB	79C2 80C8
HDMI_DDC_CLK_5V	HDMI_DDC_CLK_5V - @mlb_lib.MLB	79C2 80B4
HDMI_DDC_CLK_CONN	HDMI_DDC_CLK_CONN - @mlb_lib.MLB	80B8 80C4
HDMI_DDC_CLK_F	HDMI_DDC_CLK_F - @mlb_lib.MLB	80B6
HDMI_DDC_DATA_5V	HDMI_DDC_DATA_5V - @mlb_lib.MLB	79C2 80B4
HDMI_DDC_DATA_CONN	HDMI_DDC_DATA_CONN - @mlb_lib.MLB	80A8 80C1
HDMI_DDC_DATA_F	HDMI_DDC_DATA_F - @mlb_lib.MLB	80B6
HDMI_HPD	HDMI_HPD - @mlb_lib.MLB	79C2 80A4
HDMI_HPD_CONN	HDMI_HPD_CONN - @mlb_lib.MLB	80A8 80C4
HDMI_HPD_Q	HDMI_HPD_Q - @mlb_lib.MLB	80A6
HDMI_LS_APD	HDMI_LS_APD - @mlb_lib.MLB	79B6
HDMI_LS_CEXT	HDMI_LS_CEXT - @mlb_lib.MLB	79B5
HDMI_LS_DDCBUF	HDMI_LS_DDCBUF - @mlb_lib.MLB	79C6
HDMI_LS_DDC_EN	HDMI_LS_DDC_EN - @mlb_lib.MLB	79C6
HDMI_LS_EMI0	HDMI_LS_EMI0 - @mlb_lib.MLB	79B4
HDMI_LS_EMI1	HDMI_LS_EMI1 - @mlb_lib.MLB	79B4
HDMI_LS_HPD	HDMI_LS_HPD - @mlb_lib.MLB	8C5 79B5 79C8 83A1
	=IG_HDMI_LS_HPD - @mlb_lib.MLB	8C8 18B1
HDMI_LS_OE_L	HDMI_LS_OE_L - @mlb_lib.MLB	79C4
HDMI_LS_PEQ	HDMI_LS_PEQ - @mlb_lib.MLB	79B6
HDMI_LS_PIO	HDMI_LS_PIO - @mlb_lib.MLB	79C6
HDMI_LS_PRE	HDMI_LS_PRE - @mlb_lib.MLB	79C4
HDMI_LS_REXT	HDMI_LS_REXT - @mlb_lib.MLB	79B5
HDMI_LS_SCL	HDMI_LS_SCL - @mlb_lib.MLB	8C5 79A6 79C8 83A1
	=IG_HDMI_LS_SCL - @mlb_lib.MLB	8C8 18C1
HDMI_LS_SDA	HDMI_LS_SDA - @mlb_lib.MLB	8C5 79A6 79C8 83A1
	=IG_HDMI_LS_SDA - @mlb_lib.MLB	8C8 18C1
HPAMP_B4GAIN_INL_N	HPAMP_B4GAIN_INL_N - @mlb_lib.MLB	55C7
HPAMP_B4GAIN_INL_P	HPAMP_B4GAIN_INL_P - @mlb_lib.MLB	55C7
HPAMP_B4GAIN_INR_N	HPAMP_B4GAIN_INR_N - @mlb_lib.MLB	55B7
HPAMP_B4GAIN_INR_P	HPAMP_B4GAIN_INR_P - @mlb_lib.MLB	55B7
HPAMP_BIAS	HPAMP_BIAS - @mlb_lib.MLB	55C4
HPAMP_CN	HPAMP_CN - @mlb_lib.MLB	55B4
HPAMP_CP	HPAMP_CP - @mlb_lib.MLB	55B4
HPAMP_PVSS	HPAMP_PVSS - @mlb_lib.MLB	55B4
HS_CPUDDR_IOUT	HS_CPUDDR_IOUT - @mlb_lib.MLB	51C6
HS_MIC_BIAS	HS_MIC_BIAS - @mlb_lib.MLB	58D2
HS_MIC_HI	HS_MIC_HI - @mlb_lib.MLB	57D3 58C1
HS_MIC_HI_R	HS_MIC_HI_R - @mlb_lib.MLB	58C3
HS_MIC_LO	HS_MIC_LO - @mlb_lib.MLB	57D3 58C1
HS_RX_BP	HS_RX_BP - @mlb_lib.MLB	58D2
HS_SW_DET	HS_SW_DET - @mlb_lib.MLB	58D2
I2C_T29_SCL	I2C_T29_SCL - @mlb_lib.MLB	49B3 74A5 86C3
	=I2C_T29AMCU_SCL - @mlb_lib.MLB	49B1 77A7
I2C_T29_SDA	I2C_T29_SDA - @mlb_lib.MLB	49B3 74A5 86C3
	=I2C_T29AMCU_SDA - @mlb_lib.MLB	49B1 77A7
ICT_SEL	ICT_SEL - @mlb_lib.MLB	24A5 24A8 24B8
IRRCVR_OUT	IRRCVR_OUT - @mlb_lib.MLB	44B7 45D4 91B7
IRRCVR_OUT_RC	IRRCVR_OUT_RC - @mlb_lib.MLB	44B6
IRUC_VREG	IRUC_VREG - @mlb_lib.MLB	44C4
ISNS_HS_CPUDDR_N	ISNS_HS_CPUDDR_N - @mlb_lib.MLB	51C7
ISNS_HS_CPUDDR_P	ISNS_HS_CPUDDR_P - @mlb_lib.MLB	51C7
ISNS_HS_GPU_N	ISNS_HS_GPU_N - @mlb_lib.MLB	89C3
ISNS_HS_GPU_P	ISNS_HS_GPU_P - @mlb_lib.MLB	89C3
ISNS_P1V05PCH_N	ISNS_P1V05PCH_N - @mlb_lib.MLB	50C7
ISNS_P1V05PCH_P	ISNS_P1V05PCH_P - @mlb_lib.MLB	50C7
ISNS_P12VG3H_N	ISNS_P12VG3H_N - @mlb_lib.MLB	51D7
ISNS_P12VG3H_P	ISNS_P12VG3H_P - @mlb_lib.MLB	51D7
ISNS_VDDQ_N	ISNS_VDDQ_N - @mlb_lib.MLB	50D7
ISNS_VDDQ_P	ISNS_VDDQ_P - @mlb_lib.MLB	50D7
ISOLATE_CPU_MEM_L	ISOLATE_CPU_MEM_L - @mlb_lib.MLB	20C6 28C8
ITPCPU_CLK100M_N	ITPCPU_CLK100M_N - @mlb_lib.MLB	11C2 17A4 81C1
ITPCPU_CLK100M_P	ITPCPU_CLK100M_P - @mlb_lib.MLB	11C2 17A4 81C1
ITPXDP_CLK100M_N	ITPXDP_CLK100M_N - @mlb_lib.MLB	17A5 17B1 24C3 81C1
ITPXDP_CLK100M_P	ITPXDP_CLK100M_P - @mlb_lib.MLB	17A5 17B1 24C3 81C1
ITS_ALIVE	ITS_ALIVE - @mlb_lib.MLB	6C2
ITS_BREATHING	ITS_BREATHING - @mlb_lib.MLB	6C1
ITS_BREATHING_Q	ITS_BREATHING_Q - @mlb_lib.MLB	6C1
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @mlb_lib.MLB	6C2
JTAG_GMUX_TMS	JTAG_GMUX_TMS - @mlb_lib.MLB	19D6
JTAG_ISP_TCK	JTAG_ISP_TCK - @mlb_lib.MLB	20C6 20D8 74C2
JTAG_ISP_TDI	JTAG_ISP_TDI - @mlb_lib.MLB	20A2 20C6 74C2
JTAG_ISP_TDO	JTAG_ISP_TDO - @mlb_lib.MLB	20B6 20C6 74C2
JTAG_T29_TMS	JTAG_T29_TMS - @mlb_lib.MLB	17B5 17C8 74C2
LPCPLUS_GPIO	LPCPLUS_GPIO - @mlb_lib.MLB	20D7 48C3
LPCPLUS_RESET_L	LPCPLUS_RESET_L - @mlb_lib.MLB	27C1 48C5 84D3
LPC_AD<0>	LPC_AD<0> - @mlb_lib.MLB	17D5 46C8 48C5
LPC_AD<3..0>	LPC_AD<3..0> - @mlb_lib.MLB	84D3
LPC_AD<1>	LPC_AD<1> - @mlb_lib.MLB	17D5 46C8 48C5
LPC_AD<2>	LPC_AD<2> - @mlb_lib.MLB	17D5 46C8 48C3
LPC_AD<3>	LPC_AD<3> - @mlb_lib.MLB	17D5 46C8 48C3
LPC_CLK33M_LPCPLUS	LPC_CLK33M_LPCPLUS - @mlb_lib.MLB	27B1 48C3 84D3
LPC_CLK33M_LPCPLUS_R	LPC_CLK33M_LPCPLUS_R - @mlb_lib.MLB	19C6 27B4 84D3
LPC_CLK33M_SMC	LPC_CLK33M_SMC - @mlb_lib.MLB	27B1 46C8 84D3
LPC_CLK33M_SMC_R	LPC_CLK33M_SMC_R - @mlb_lib.MLB	19C6 27B4 84D3
LPC_FRAME_L	LPC_FRAME_L - @mlb_lib.MLB	17D5 46C8 48C5 84D3
LPC_FRAME_R_L	LPC_FRAME_R_L - @mlb_lib.MLB	17D6 84D3
LPC_PWRDWN_L	LPC_PWRDWN_L - @mlb_lib.MLB	18C5 46C5 48C3
LPC_R_AD<0>	LPC_R_AD<0> - @mlb_lib.MLB	17D6
LPC_R_AD<3..0>	LPC_R_AD<3..0> - @mlb_lib.MLB	84D3
LPC_R_AD<1>	LPC_R_AD<1> - @mlb_lib.MLB	17D6
LPC_R_AD<2>	LPC_R_AD<2> - @mlb_lib.MLB	17D6
LPC_R_AD<3>	LPC_R_AD<3> - @mlb_lib.MLB	17D6
LPC_SERIRQ	LPC_SERIRQ - @mlb_lib.MLB	17D5 46C8 48C3
MAX8840_BP	MAX8840_BP - @mlb_lib.MLB	53A5
MEMRESET_ISOL_LS5V_L	MEMRESET_ISOL_LS5V_L - @mlb_lib.MLB	28B7
MEMVTT_EN	MEMVTT_EN - @mlb_lib.MLB	28A4 28C5 66C8
MEMVTT_EN_L	MEMVTT_EN_L - @mlb_lib.MLB	28B6
MEM_A_A<0>	MEM_A_A<0> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<15..0>	MEM_A_A<15..0> - @mlb_lib.MLB	82D3
MEM_A_A<1>	MEM_A_A<1> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<2>	MEM_A_A<2> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<3>	MEM_A_A<3> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<4>	MEM_A_A<4> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<5>	MEM_A_A<5> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<6>	MEM_A_A<6> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<7>	MEM_A_A<7> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<8>	MEM_A_A<8> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<9>	MEM_A_A<9> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<10>	MEM_A_A<10> - @mlb_lib.MLB	12C5 30B7
MEM_A_A<11>	MEM_A_A<11> - @mlb_lib.MLB	12B5 30C5
MEM_A_A<12>	MEM_A_A<12> - @mlb_lib.MLB	12B5 30C7
MEM_A_A<13>	MEM_A_A<13> - @mlb_lib.MLB	12B5 30B7
MEM_A_A<14>	MEM_A_A<14> - @mlb_lib.MLB	12B5 30C5
MEM_A_A<15>	MEM_A_A<15> - @mlb_lib.MLB	12B5 30C5
MEM_A_BA<0>	MEM_A_BA<0> - @mlb_lib.MLB	12B7 30B7
MEM_A_BA<2..0>	MEM_A_BA<2..0> - @mlb_lib.MLB	82D3
MEM_A_BA<1>	MEM_A_BA<1> - @mlb_lib.MLB	12B7 30B5
MEM_A_BA<2>	MEM_A_BA<2> - @mlb_lib.MLB	12B7 30C7
MEM_A_CAS_L	MEM_A_CAS_L - @mlb_lib.MLB	12B7 30B7 82D3
MEM_A_CKE<0>	MEM_A_CKE<0> - @mlb_lib.MLB	12D5 30C7
MEM_A_CKE<3..0>	MEM_A_CKE<3..0> - @mlb_lib.MLB	82D3
MEM_A_CKE<1>	MEM_A_CKE<1> - @mlb_lib.MLB	12D5 30C5
MEM_A_CLK_N<0>	MEM_A_CLK_N<0> - @mlb_lib.MLB	12D5 30C7
MEM_A_CLK_N<5..0>	MEM_A_CLK_N<5..0> - @mlb_lib.MLB	82D3
MEM_A_CLK_N<1>	MEM_A_CLK_N<1> - @mlb_lib.MLB	12D5 30C5
MEM_A_CLK_P<0>	MEM_A_CLK_P<0> - @mlb_lib.MLB	12D5 30C7
MEM_A_CLK_P<5..0>	MEM_A_CLK_P<5..0> - @mlb_lib.MLB	82D3
MEM_A_CLK_P<1>	MEM_A_CLK_P<1> - @mlb_lib.MLB	12D5 30C5
MEM_A_CS_L<0>	MEM_A_CS_L<0> - @mlb_lib.MLB	12D5 30B5
MEM_A_CS_L<3..0>	MEM_A_CS_L<3..0> - @mlb_lib.MLB	82D3
MEM_A_CS_L<1>	MEM_A_CS_L<1> - @mlb_lib.MLB	12D5 30B7
MEM_A_DQ<0>	MEM_A_DQ<0> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<7..0>	MEM_A_DQ<7..0> - @mlb_lib.MLB	82D3
MEM_A_DQ<1>	MEM_A_DQ<1> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<2>	MEM_A_DQ<2> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<3>	MEM_A_DQ<3> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<4>	MEM_A_DQ<4> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<5>	MEM_A_DQ<5> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<6>	MEM_A_DQ<6> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<7>	MEM_A_DQ<7> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<8>	MEM_A_DQ<8> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<15..8>	MEM_A_DQ<15..8> - @mlb_lib.MLB	82D3
MEM_A_DQ<9>	MEM_A_DQ<9> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<10>	MEM_A_DQ<10> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<11>	MEM_A_DQ<11> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<12>	MEM_A_DQ<12> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<13>	MEM_A_DQ<13> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<14>	MEM_A_DQ<14> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<15>	MEM_A_DQ<15> - @mlb_lib.MLB	12D7 29D8
MEM_A_DQ<16>	MEM_A_DQ<16> - @mlb_lib.MLB	12D7 29C8
MEM_A_DQ<23..16>	MEM_A_DQ<23..16> - @mlb_lib.MLB	82D3
MEM_A_DQ<17>	MEM_A_DQ<17> - @mlb_lib.MLB	12D7 29C8
MEM_A_DQ<18>	MEM_A_DQ<18> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<19>	MEM_A_DQ<19> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<20>	MEM_A_DQ<20> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<21>	MEM_A_DQ<21> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<22>	MEM_A_DQ<22> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<23>	MEM_A_DQ<23> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<24>	MEM_A_DQ<24> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<31..24>	MEM_A_DQ<31..24> - @mlb_lib.MLB	82D3
MEM_A_DQ<25>	MEM_A_DQ<25> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<26>	MEM_A_DQ<26> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<27>	MEM_A_DQ<27> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<28>	MEM_A_DQ<28> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<29>	MEM_A_DQ<29> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<30>	MEM_A_DQ<30> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<31>	MEM_A_DQ<31> - @mlb_lib.MLB	12C7 29C8
MEM_A_DQ<32>	MEM_A_DQ<32> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<39..32>	MEM_A_DQ<39..32> - @mlb_lib.MLB	82D3
MEM_A_DQ<33>	MEM_A_DQ<33> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<34>	MEM_A_DQ<34> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<35>	MEM_A_DQ<35> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<36>	MEM_A_DQ<36> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<37>	MEM_A_DQ<37> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<38>	MEM_A_DQ<38> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<39>	MEM_A_DQ<39> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<40>	MEM_A_DQ<40> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<47..40>	MEM_A_DQ<47..40> - @mlb_lib.MLB	82D3

MEM_A_DQ<41>	MEM_A_DQ<41> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<42>	MEM_A_DQ<42> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<43>	MEM_A_DQ<43> - @mlb_lib.MLB	12C7 29B8
MEM_A_DQ<44>	MEM_A_DQ<44> - @mlb_lib.MLB	12B7 29B8
MEM_A_DQ<45>	MEM_A_DQ<45> - @mlb_lib.MLB	12B7 29B8
MEM_A_DQ<46>	MEM_A_DQ<46> - @mlb_lib.MLB	12B7 29B8
MEM_A_DQ<47>	MEM_A_DQ<47> - @mlb_lib.MLB	12B7 29B8
MEM_A_DQ<48>	MEM_A_DQ<48> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<55..48>	MEM_A_DQ<55..48> - @mlb_lib.MLB	82D3
MEM_A_DQ<49>	MEM_A_DQ<49> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<50>	MEM_A_DQ<50> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<51>	MEM_A_DQ<51> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<52>	MEM_A_DQ<52> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<53>	MEM_A_DQ<53> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<54>	MEM_A_DQ<54> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<55>	MEM_A_DQ<55> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<56>	MEM_A_DQ<56> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<63..56>	MEM_A_DQ<63..56> - @mlb_lib.MLB	82D3
MEM_A_DQ<57>	MEM_A_DQ<57> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<58>	MEM_A_DQ<58> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<59>	MEM_A_DQ<59> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<60>	MEM_A_DQ<60> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<61>	MEM_A_DQ<61> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<62>	MEM_A_DQ<62> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQ<63>	MEM_A_DQ<63> - @mlb_lib.MLB	12B7 29A8
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @mlb_lib.MLB	12D5 29D8 82C3
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @mlb_lib.MLB	12D5 29D8 82C3
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @mlb_lib.MLB	12D5 29C8 82C3
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @mlb_lib.MLB	12C5 29C8 82C3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @mlb_lib.MLB	12C5 29B8 82C3
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @mlb_lib.MLB	12C5 29B8 82C3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @mlb_lib.MLB	12C5 29A8 82C3
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @mlb_lib.MLB	12C5 29A8 82C3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @mlb_lib.MLB	12C5 29D8 82D3
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @mlb_lib.MLB	12C5 29D8 82C3
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @mlb_lib.MLB	12C5 29C8 82C3
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @mlb_lib.MLB	12C5 29C8 82C3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @mlb_lib.MLB	12C5 29B8 82C3
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @mlb_lib.MLB	12C5 29B8 82C3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @mlb_lib.MLB	12C5 29A8 82C3
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @mlb_lib.MLB	12C5 29A8 82C3
MEM_A_ODT<0>	MEM_A_ODT<0> - @mlb_lib.MLB	12D5 30B5
MEM_A_ODT<3..0>	MEM_A_ODT<3..0> - @mlb_lib.MLB	82D3
MEM_A_ODT<1>	MEM_A_ODT<1> - @mlb_lib.MLB	12D5 30B5
MEM_A_RAS_L	MEM_A_RAS_L - @mlb_lib.MLB	12B7 30B5 82D3
MEM_A_SA<0>	MEM_A_SA<0> - @mlb_lib.MLB	30A7 30B3
MEM_A_SA<1>	MEM_A_SA<1> - @mlb_lib.MLB	30A7 30B3
MEM_A_WE_L	MEM_A_WE_L - @mlb_lib.MLB	12A7 30B7 82D3
MEM_B_A<0>	MEM_B_A<0> - @mlb_lib.MLB	12C2 31C5
MEM_B_A<15..0>	MEM_B_A<15..0> - @mlb_lib.MLB	82B3
MEM_B_A<1>	MEM_B_A<1> - @mlb_lib.MLB	12C2 31C7
MEM_B_A<2>	MEM_B_A<2> - @mlb_lib.MLB	12C2 31C5
MEM_B_A<3>	MEM_B_A<3> - @mlb_lib.MLB	12C2 31C7
MEM_B_A<4>	MEM_B_A<4> - @mlb_lib.MLB	12C2 31C5
MEM_B_A<5>	MEM_B_A<5> - @mlb_lib.MLB	12C2 31C7
MEM_B_A<6>	MEM_B_A<6> - @mlb_lib.MLB	12C2 31C5
MEM_B_A<7>	MEM_B_A<7> - @mlb_lib.MLB	12C2 31C5
MEM_B_A<8>	MEM_B_A<8> - @mlb_lib.MLB	12C2 31C7
MEM_B_A<9>	MEM_B_A<9> - @mlb_lib.MLB	12C2 31C7
MEM_B_A<10>	MEM_B_A<10> - @mlb_lib.MLB	12C2 31B7
MEM_B_A<11>	MEM_B_A<11> - @mlb_lib.MLB	12B2 31C5
MEM_B_A<12>	MEM_B_A<12> - @mlb_lib.MLB	12B2 31C7
MEM_B_A<13>	MEM_B_A<13> - @mlb_lib.MLB	12B2 31B7
MEM_B_A<14>	MEM_B_A<14> - @mlb_lib.MLB	12B2 31C5
MEM_B_A<15>	MEM_B_A<15> - @mlb_lib.MLB	12B2 31C5
MEM_B_BA<0>	MEM_B_BA<0> - @mlb_lib.MLB	12B4 31B7
MEM_B_BA<2..0>	MEM_B_BA<2..0> - @mlb_lib.MLB	82B3
MEM_B_BA<1>	MEM_B_BA<1> - @mlb_lib.MLB	12B4 31B5
MEM_B_BA<2>	MEM_B_BA<2> - @mlb_lib.MLB	12B4 31C7
MEM_B_CAS_L	MEM_B_CAS_L - @mlb_lib.MLB	12B4 31B7 82B3
MEM_B_CKE<0>	MEM_B_CKE<0> - @mlb_lib.MLB	12D2 31C7
MEM_B_CKE<3..0>	MEM_B_CKE<3..0> - @mlb_lib.MLB	82B3
MEM_B_CKE<1>	MEM_B_CKE<1> - @mlb_lib.MLB	12D2 31C5
MEM_B_CLK_N<0>	MEM_B_CLK_N<0> - @mlb_lib.MLB	12D2 31C7
MEM_B_CLK_N<5..0>	MEM_B_CLK_N<5..0> - @mlb_lib.MLB	82C3
MEM_B_CLK_N<1>	MEM_B_CLK_N<1> - @mlb_lib.MLB	12D2 31C5
MEM_B_CLK_P<0>	MEM_B_CLK_P<0> - @mlb_lib.MLB	12D2 31C7
MEM_B_CLK_P<5..0>	MEM_B_CLK_P<5..0> - @mlb_lib.MLB	82C3
MEM_B_CLK_P<1>	MEM_B_CLK_P<1> - @mlb_lib.MLB	12D2 31C5
MEM_B_CS_L<0>	MEM_B_CS_L<0> - @mlb_lib.MLB	12D2 31B5
MEM_B_CS_L<3..0>	MEM_B_CS_L<3..0> - @mlb_lib.MLB	82B3
MEM_B_CS_L<1>	MEM_B_CS_L<1> - @mlb_lib.MLB	12D2 31B7
MEM_B_DQ<0>	MEM_B_DQ<0> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<7..0>	MEM_B_DQ<7..0> - @mlb_lib.MLB	82B3
MEM_B_DQ<1>	MEM_B_DQ<1> - @mlb_lib.MLB	12D4 29D5
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MEM_B_DQ<4>	MEM_B_DQ<4> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<5>	MEM_B_DQ<5> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<6>	MEM_B_DQ<6> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<7>	MEM_B_DQ<7> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<8>	MEM_B_DQ<8> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<15..8>	MEM_B_DQ<15..8> - @mlb_lib.MLB	82B3
MEM_B_DQ<9>	MEM_B_DQ<9> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<10>	MEM_B_DQ<10> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<11>	MEM_B_DQ<11> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<12>	MEM_B_DQ<12> - @mlb_lib.MLB	12D4 29D5
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MEM_B_DQ<15>	MEM_B_DQ<15> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<16>	MEM_B_DQ<16> - @mlb_lib.MLB	12D4 29C5
MEM_B_DQ<23..16>	MEM_B_DQ<23..16> - @mlb_lib.MLB	82B3
MEM_B_DQ<17>	MEM_B_DQ<17> - @mlb_lib.MLB	12D4 29C5
MEM_B_DQ<18>	MEM_B_DQ<18> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<19>	MEM_B_DQ<19> - @mlb_lib.MLB	12C4 29C5
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MEM_B_DQ<23>	MEM_B_DQ<23> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<24>	MEM_B_DQ<24> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<31..24>	MEM_B_DQ<31..24> - @mlb_lib.MLB	82B3
MEM_B_DQ<25>	MEM_B_DQ<25> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<26>	MEM_B_DQ<26> - @mlb_lib.MLB	12C4 29C5
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MEM_B_DQ<39..32>	MEM_B_DQ<39..32> - @mlb_lib.MLB	82B3
MEM_B_DQ<33>	MEM_B_DQ<33> - @mlb_lib.MLB	12C4 29B5
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MEM_B_DQ<37>	MEM_B_DQ<37> - @mlb_lib.MLB	12C4 29B5
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MEM_B_DQ<39>	MEM_B_DQ<39> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<40>	MEM_B_DQ<40> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<47..40>	MEM_B_DQ<47..40> - @mlb_lib.MLB	82B3
MEM_B_DQ<41>	MEM_B_DQ<41> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<42>	MEM_B_DQ<42> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<43>	MEM_B_DQ<43> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<44>	MEM_B_DQ<44> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<45>	MEM_B_DQ<45> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<46>	MEM_B_DQ<46> - @mlb_lib.MLB	12B4 29B5
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MEM_B_DQ<48>	MEM_B_DQ<48> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<55..48>	MEM_B_DQ<55..48> - @mlb_lib.MLB	82B3
MEM_B_DQ<49>	MEM_B_DQ<49> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<50>	MEM_B_DQ<50> - @mlb_lib.MLB	12B4 29A5
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MEM_B_DQ<52>	MEM_B_DQ<52> - @mlb_lib.MLB	12B4 29A5
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MEM_B_DQ<63..56>	MEM_B_DQ<63..56> - @mlb_lib.MLB	82B3
MEM_B_DQ<57>	MEM_B_DQ<57> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<58>	MEM_B_DQ<58> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<59>	MEM_B_DQ<59> - @mlb_lib.MLB	12B4 29A5
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MEM_B_DQ<61>	MEM_B_DQ<61> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<62>	MEM_B_DQ<62> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<63>	MEM_B_DQ<63> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @mlb_lib.MLB	12D2 29D5 82B3
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @mlb_lib.MLB	12D2 29D5 82B3
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @mlb_lib.MLB	12D2 29C5 82B3
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @mlb_lib.MLB	12C2 29C5 82B3
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @mlb_lib.MLB	12C2 29B5 82A3
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @mlb_lib.MLB	12C2 29B5 82A3
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @mlb_lib.MLB	12C2 29A5 82A3
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @mlb_lib.MLB	12C2 29A5 82A3
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MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @mlb_lib.MLB	12C2 29C5 82B3
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @mlb_lib.MLB	12C2 29B5 82B3
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @mlb_lib.MLB	12C2 29B5 82A3
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @mlb_lib.MLB	12C2 29A5 82A3
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @mlb_lib.MLB	12C2 29A5 82A3
MEM_B_ODT<0>	MEM_B_ODT<0> - @mlb_lib.MLB	12D2 31B5
MEM_B_ODT<3..0>	MEM_B_ODT<3..0> - @mlb_lib.MLB	82B3
MEM_B_ODT<1>	MEM_B_ODT<1> - @mlb_lib.MLB	12D2 31B5
MEM_B_RAS_L	MEM_B_RAS_L - @mlb_lib.MLB	12B4 31B5 82B3
MEM_B_SA<0>	MEM_B_SA<0> - @mlb_lib.MLB	31A7 31B3
MEM_B_SA<1>	MEM_B_SA<1> - @mlb_lib.MLB	31A7 31B3
MEM_B_WE_L	MEM_B_WE_L - @mlb_lib.MLB	12A4 31B7 82B3
MEM_EVENT_L	MEM_EVENT_L - @mlb_lib.MLB	30A5 31A5 46B8
MEM_RESET_L	MEM_RESET_L - @mlb_lib.MLB	28A5 30D5 31D5
NC_AUD_GPIO_0	NC_AUD_GPIO_0 - @mlb_lib.MLB	53D7 91D3
NC_AUD_GPIO_2	NC_AUD_GPIO_2 - @mlb_lib.MLB	53D7 91D2
NC_AUD_HP_PORT_L	NC_AUD_HP_PORT_L - @mlb_lib.MLB	53D2 91D1
NC_AUD_HP_PORT_R	NC_AUD_HP_PORT_R - @mlb_lib.MLB	53D2 91D3
NC_AUD_LO3_N_R	NC_AUD_LO3_N_R - @mlb_lib.MLB	53C2 91D2
NC_AUD_LO3_P_R	NC_AUD_LO3_P_R - @mlb_lib.MLB	53C2 91D1
NC_AUD_MIC_INN_R	NC_AUD_MIC_INN_R - @mlb_lib.MLB	53C2 91D3
NC_AUD_MIC_INP_R	NC_AUD_MIC_INP_R - @mlb_lib.MLB	53C2 91D2
NC_BCM57765_CE_L_MS_INS_L	NC_BCM57765_CE_L_MS_INS_L - @mlb_lib.MLB	37B3 91D1
NC_CLINK_CLK	NC_CLINK_CLK - @mlb_lib.MLB	17B1 91D3
NC_CLINK_DATA	NC_CLINK_DATA - @mlb_lib.MLB	17B1 91D2
NC_CLINK_RESET_L	NC_CLINK_RESET_L - @mlb_lib.MLB	17B1 91D1
NC_CPU_AXG_SENSEN	NC_CPU_AXG_SENSEN - @mlb_lib.MLB	91B3
NC_CPU_AXG_SENSEP	NC_CPU_AXG_SENSEP - @mlb_lib.MLB	91B2
NC_CPU_AXG_VALSENSEN	NC_CPU_AXG_VALSENSEN - @mlb_lib.MLB	91B2
NC_CPU_AXG_VALSENSEP	NC_CPU_AXG_VALSENSEP - @mlb_lib.MLB	91B3
NC_CRT_IG_BLUE	NC_CRT_IG_BLUE - @mlb_lib.MLB	18C4 91D3
NC_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK - @mlb_lib.MLB	18B4 91D2
NC_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA - @mlb_lib.MLB	18B4 91D1
NC_CRT_IG_GREEN	NC_CRT_IG_GREEN - @mlb_lib.MLB	18C4 91D3
NC_CRT_IG_HSYNC	NC_CRT_IG_HSYNC - @mlb_lib.MLB	18B4 91D2
NC_CRT_IG_RED	NC_CRT_IG_RED - @mlb_lib.MLB	18B4 91D1
NC_CRT_IG_VSYNC	NC_CRT_IG_VSYNC - @mlb_lib.MLB	18B4 91D3
NC_CS4206_FP	NC_CS4206_FP - @mlb_lib.MLB	53D5 91D2
NC_CS4206_MICBIAS	NC_CS4206_MICBIAS - @mlb_lib.MLB	53C2 91D1
NC_DP_OC	NC_DP_OC - @mlb_lib.MLB	91D3
NC_DP_T29SNK1_AUXCHN	NC_DP_T29SNK1_AUXCHN - @mlb_lib.MLB	74A5 91A1
NC_DP_T29SNK1_AUXCHP	NC_DP_T29SNK1_AUXCHP - @mlb_lib.MLB	74A5 91A1
NC_DP_T29SNK1_MLN<0>	NC_DP_T29SNK1_MLN<0> - @mlb_lib.MLB	74A5
NC_DP_T29SNK1_MLN<3..0>	NC_DP_T29SNK1_MLN<3..0> - @mlb_lib.MLB	91A1
NC_DP_T29SNK1_MLN<1>	NC_DP_T29SNK1_MLN<1> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLN<2>	NC_DP_T29SNK1_MLN<2> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLN<3>	NC_DP_T29SNK1_MLN<3> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLP<0>	NC_DP_T29SNK1_MLP<0> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLP<3..0>	NC_DP_T29SNK1_MLP<3..0> - @mlb_lib.MLB	91A1
NC_DP_T29SNK1_MLP<1>	NC_DP_T29SNK1_MLP<1> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLP<2>	NC_DP_T29SNK1_MLP<2> - @mlb_lib.MLB	74B5
NC_DP_T29SNK1_MLP<3>	NC_DP_T29SNK1_MLP<3> - @mlb_lib.MLB	74B5
NC_DP_T29SRC_AUXCH_CN	NC_DP_T29SRC_AUXCH_CN - @mlb_lib.MLB	74B3 91A1
NC_DP_T29SRC_AUXCH_CP	NC_DP_T29SRC_AUXCH_CP - @mlb_lib.MLB	74B3 91A1
NC_DP_T29SRC_ML_CN<0>	NC_DP_T29SRC_ML_CN<0> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CN<3..0>	NC_DP_T29SRC_ML_CN<3..0> - @mlb_lib.MLB	91A1
NC_DP_T29SRC_ML_CN<1>	NC_DP_T29SRC_ML_CN<1> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CN<2>	NC_DP_T29SRC_ML_CN<2> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CN<3>	NC_DP_T29SRC_ML_CN<3> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CP<0>	NC_DP_T29SRC_ML_CP<0> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CP<3..0>	NC_DP_T29SRC_ML_CP<3..0> - @mlb_lib.MLB	91A1
NC_DP_T29SRC_ML_CP<1>	NC_DP_T29SRC_ML_CP<1> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CP<2>	NC_DP_T29SRC_ML_CP<2> - @mlb_lib.MLB	74B3
NC_DP_T29SRC_ML_CP<3>	NC_DP_T29SRC_ML_CP<3> - @mlb_lib.MLB	74B3
NC_EDP_AUXN	NC_EDP_AUXN - @mlb_lib.MLB	10B7 91D2
NC_EDP_AUXP	NC_EDP_AUXP - @mlb_lib.MLB	10B7 91D1
NC_EDP_HPD	NC_EDP_HPD - @mlb_lib.MLB	10B7 91A2
NC_EDP_TXN<0>	NC_EDP_TXN<0> - @mlb_lib.MLB	10B7
NC_EDP_TXN<3..0>	NC_EDP_TXN<3..0> - @mlb_lib.MLB	91D3
NC_EDP_TXN<1>	NC_EDP_TXN<1> - @mlb_lib.MLB	10B7
NC_EDP_TXN<2>	NC_EDP_TXN<2> - @mlb_lib.MLB	10B7
NC_EDP_TXN<3>	NC_EDP_TXN<3> - @mlb_lib.MLB	10B7
NC_EDP_TXP<0>	NC_EDP_TXP<0> - @mlb_lib.MLB	10B7
NC_EDP_TXP<3..0>	NC_EDP_TXP<3..0> - @mlb_lib.MLB	91D2
NC_EDP_TXP<1>	NC_EDP_TXP<1> - @mlb_lib.MLB	10B7
NC_EDP_TXP<2>	NC_EDP_TXP<2> - @mlb_lib.MLB	10B7
NC_EDP_TXP<3>	NC_EDP_TXP<3> - @mlb_lib.MLB	10B7
NC_EG_DP_T29SNK0_AUXCH_CN	NC_EG_DP_T29SNK0_AUXCH_CN - @mlb_lib.MLB	91B2
NC_EG_DP_T29SNK0_AUXCH_CP	NC_EG_DP_T29SNK0_AUXCH_CP - @mlb_lib.MLB	91B3
NC_EG_DP_T29SNK0_ML_CN<3..0>	NC_EG_DP_T29SNK0_ML_CN<3..0> - @mlb_lib.MLB	91B2
NC_EG_DP_T29SNK0_ML_CP<3..0>	NC_EG_DP_T29SNK0_ML_CP<3..0> - @mlb_lib.MLB	91B3
NC_FB_A0_A<8..0>	NC_FB_A0_A<8..0> - @mlb_lib.MLB	91B2
NC_FB_A0_ABI_L	NC_FB_A0_ABI_L - @mlb_lib.MLB	91B3
NC_FB_A0_CAS_L	NC_FB_A0_CAS_L - @mlb_lib.MLB	91B2
NC_FB_A0_CKE_L	NC_FB_A0_CKE_L - @mlb_lib.MLB	91B3
NC_FB_A0_CLKN	NC_FB_A0_CLKN - @mlb_lib.MLB	91B2
NC_FB_A0_CLKP	NC_FB_A0_CLKP - @mlb_lib.MLB	91B3
NC_FB_A0_CS_L	NC_FB_A0_CS_L - @mlb_lib.MLB	91B2
NC_FB_A0_DBI_L<3..0>	NC_FB_A0_DBI_L<3..0> - @mlb_lib.MLB	91B3
NC_FB_A0_DQ<31..0>	NC_FB_A0_DQ<31..0> - @mlb_lib.MLB	91A2
NC_FB_A0_EDC<3..0>	NC_FB_A0_EDC<3..0> - @mlb_lib.MLB	91A3
NC_FB_A0_RAS_L	NC_FB_A0_RAS_L - @mlb_lib.MLB	91A2
NC_FB_A0_WCLKN<1..0>	NC_FB_A0_WCLKN<1..0> - @mlb_lib.MLB	91A3
NC_FB_A0_WCLKP<1..0>	NC_FB_A0_WCLKP<1..0> - @mlb_lib.MLB	91A2
NC_FB_A0_WE_L	NC_FB_A0_WE_L - @mlb_lib.MLB	91A3
NC_FB_A1_A<8..0>	NC_FB_A1_A<8..0> - @mlb_lib.MLB	91A2
NC_FB_A1_ABI_L	NC_FB_A1_ABI_L - @mlb_lib.MLB	91A3
NC_FB_A1_CAS_L	NC_FB_A1_CAS_L - @mlb_lib.MLB	91A2
NC_FB_A1_CKE_L	NC_FB_A1_CKE_L - @mlb_lib.MLB	91A3
NC_FB_A1_CLKN	NC_FB_A1_CLKN - @mlb_lib.MLB	91A2
NC_FB_A1_CLKP	NC_FB_A1_CLKP - @mlb_lib.MLB	91A3
NC_FB_A1_CS_L	NC_FB_A1_CS_L - @mlb_lib.MLB	91A2
NC_FB_A1_DBI_L<3..0>	NC_FB_A1_DBI_L<3..0> - @mlb_lib.MLB	91A3
NC_FB_A1_DQ<31..0>	NC_FB_A1_DQ<31..0> - @mlb_lib.MLB	91A2
NC_FB_A1_EDC<3..0>	NC_FB_A1_EDC<3..0> - @mlb_lib.MLB	91A3
NC_FB_A1_RAS_L	NC_FB_A1_RAS_L - @mlb_lib.MLB	91A2
NC_FB_A1_WCLKN<1..0>	NC_FB_A1_WCLKN<1..0> - @mlb_lib.MLB	91A3
NC_FB_A1_WCLKP<1..0>	NC_FB_A1_WCLKP<1..0> - @mlb_lib.MLB	91A2
NC_FB_A1_WE_L	NC_FB_A1_WE_L - @mlb_lib.MLB	91A3
NC_FW_P1_TPAN	NC_FW_P1_TPAN - @mlb_lib.MLB	39A3 91D1
NC_FW_P1_TPAP	NC_FW_P1_TPAP - @mlb_lib.MLB	39A3 91D3
NC_FW_P1_TPBIAS	NC_FW_P1_TPBIAS - @mlb_lib.MLB	39A3 91D2
NC_FW_P2_TPAN	NC_FW_P2_TPAN - @mlb_lib.MLB	39A3 91D1
NC_FW_P2_TPAP	NC_FW_P2_TPAP - @mlb_lib.MLB	39A3 91D3
NC_FW_P2_TPBIAS	NC_FW_P2_TPBIAS - @mlb_lib.MLB	39A3 91D2
NC_GPIO35	NC_GPIO35 - @mlb_lib.MLB	20C6 91D1
NC_GPU_GENERICB	NC_GPU_GENERICB - @mlb_lib.MLB	91A3
NC_GPU_GENERICC	NC_GPU_GENERICC - @mlb_lib.MLB	91A3
NC_GPU_GENERICE	NC_GPU_GENERICE - @mlb_lib.MLB	91A3
NC_GPU_GENERICF	NC_GPU_GENERICF - @mlb_lib.MLB	91A3
NC_GPU_GENERICG	NC_GPU_GENERICG - @mlb_lib.MLB	91A3
NC_HDA_SDIN1	NC_HDA_SDIN1 - @mlb_lib.MLB	17C8 91D2
NC_HDA_SDIN2	NC_HDA_SDIN2 - @mlb_lib.MLB	17C8 91D1
NC_HDA_SDIN3	NC_HDA_SDIN3 - @mlb_lib.MLB	17C8 91D3
NC_HD_OC	NC_HD_OC - @mlb_lib.MLB	80D3 91D3
NC_IG_DP_T29SNK0_AUXCH_CN	NC_IG_DP_T29SNK0_AUXCH_CN - @mlb_lib.MLB	91D3
NC_IG_DP_T29SNK0_AUXCH_CP	NC_IG_DP_T29SNK0_AUXCH_CP - @mlb_lib.MLB	91D2
NC_IG_DP_T29SNK0_CTRL_CLK	NC_IG_DP_T29SNK0_CTRL_CLK - @mlb_lib.MLB	91D1
NC_IG_DP_T29SNK0_CTRL_DATA	NC_IG_DP_T29SNK0_CTRL_DATA - @mlb_lib.MLB	91D3
NC_IG_DP_T29SNK0_HPD	NC_IG_DP_T29SNK0_HPD - @mlb_lib.MLB	91D2
NC_IG_DP_T29SNK0_ML_CN<3..0>	NC_IG_DP_T29SNK0_ML_CN<3..0> - @mlb_lib.MLB	91D1
NC_IG_DP_T29SNK0_ML_CP<3..0>	NC_IG_DP_T29SNK0_ML_CP<3..0> - @mlb_lib.MLB	91D3
NC_IG_D_AUXN	NC_IG_D_AUXN - @mlb_lib.MLB	18C1 91D2
NC_IG_D_AUXP	NC_IG_D_AUXP - @mlb_lib.MLB	18C1 91D1
NC_IRUC_P02	NC_IRUC_P02 - @mlb_lib.MLB	44C6 91D2
NC_IRUC_P03	NC_IRUC_P03 - @mlb_lib.MLB	44C6 91D1
NC_IRUC_P04	NC_IRUC_P04 - @mlb_lib.MLB	44C6 91D3
NC_IRUC_P06	NC_IRUC_P06 - @mlb_lib.MLB	44B6 91D2
NC_IRUC_P13	NC_IRUC_P13 - @mlb_lib.MLB	44C4 91D1
NC_IRUC_P14	NC_IRUC_P14 - @mlb_lib.MLB	44C4 91D3
NC_IRUC_P15	NC_IRUC_P15 - @mlb_lib.MLB	44B4 91D2
NC_IRUC_P16	NC_IRUC_P16 - @mlb_lib.MLB	44B4 91D1
NC_LPC_DREQ0_L	NC_LPC_DREQ0_L - @mlb_lib.MLB	17D5 91D3
NC_LVDS_EG_A_CLKN	NC_LVDS_EG_A_CLKN - @mlb_lib.MLB	91A3
NC_LVDS_EG_A_CLKP	NC_LVDS_EG_A_CLKP - @mlb_lib.MLB	91A3
NC_LVDS_EG_A_DATAN<3..0>	NC_LVDS_EG_A_DATAN<3..0> - @mlb_lib.MLB	91A3
NC_LVDS_EG_A_DATAP<3..0>	NC_LVDS_EG_A_DATAP<3..0> - @mlb_lib.MLB	91A3
NC_LVDS_EG_B_CLKN	NC_LVDS_EG_B_CLKN - @mlb_lib.MLB	91A3
NC_LVDS_EG_B_CLKP	NC_LVDS_EG_B_CLKP - @mlb_lib.MLB	91A3
NC_LVDS_EG_B_DATAN<3..0>	NC_LVDS_EG_B_DATAN<3..0> - @mlb_lib.MLB	91A3
NC_LVDS_EG_B_DATAP<3..0>	NC_LVDS_EG_B_DATAP<3..0> - @mlb_lib.MLB	91A3
NC_LVDS_EG_DDC_CLK	NC_LVDS_EG_DDC_CLK - @mlb_lib.MLB	91A3
NC_LVDS_EG_DDC_DATA	NC_LVDS_EG_DDC_DATA - @mlb_lib.MLB	91A3
NC_LVDS_IG_A_CLKN	NC_LVDS_IG_A_CLKN - @mlb_lib.MLB	19C6 91D2
NC_LVDS_IG_A_CLKP	NC_LVDS_IG_A_CLKP - @mlb_lib.MLB	19C6 91D1
NC_LVDS_IG_A_DATAN<0>	NC_LVDS_IG_A_DATAN<0> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAN<3..0>	NC_LVDS_IG_A_DATAN<3..0> - @mlb_lib.MLB	91D3
NC_LVDS_IG_A_DATAN<1>	NC_LVDS_IG_A_DATAN<1> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAN<2>	NC_LVDS_IG_A_DATAN<2> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAN<3>	NC_LVDS_IG_A_DATAN<3> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAP<0>	NC_LVDS_IG_A_DATAP<0> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAP<3..0>	NC_LVDS_IG_A_DATAP<3..0> - @mlb_lib.MLB	91D2
NC_LVDS_IG_A_DATAP<1>	NC_LVDS_IG_A_DATAP<1> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAP<2>	NC_LVDS_IG_A_DATAP<2> - @mlb_lib.MLB	19C6
NC_LVDS_IG_A_DATAP<3>	NC_LVDS_IG_A_DATAP<3> - @mlb_lib.MLB	19C6
NC_LVDS_IG_BKL_ON	NC_LVDS_IG_BKL_ON - @mlb_lib.MLB	19B6 91D3
NC_LVDS_IG_BKL_PWM	NC_LVDS_IG_BKL_PWM - @mlb_lib.MLB	19B6 91D2
NC_LVDS_IG_B_CLKN	NC_LVDS_IG_B_CLKN - @mlb_lib.MLB	19B6 91D1
NC_LVDS_IG_B_CLKP	NC_LVDS_IG_B_CLKP - @mlb_lib.MLB	19B6 91D3
NC_LVDS_IG_B_DATAN<0>	NC_LVDS_IG_B_DATAN<0> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAN<3..0>	NC_LVDS_IG_B_DATAN<3..0> - @mlb_lib.MLB	91D2
NC_LVDS_IG_B_DATAN<1>	NC_LVDS_IG_B_DATAN<1> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAN<2>	NC_LVDS_IG_B_DATAN<2> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAN<3>	NC_LVDS_IG_B_DATAN<3> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAP<0>	NC_LVDS_IG_B_DATAP<0> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAP<3..0>	NC_LVDS_IG_B_DATAP<3..0> - @mlb_lib.MLB	91D1
NC_LVDS_IG_B_DATAP<1>	NC_LVDS_IG_B_DATAP<1> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAP<2>	NC_LVDS_IG_B_DATAP<2> - @mlb_lib.MLB	19C6
NC_LVDS_IG_B_DATAP<3>	NC_LVDS_IG_B_DATAP<3> - @mlb_lib.MLB	19C6
NC_LVDS_IG_CTRL_CLK	NC_LVDS_IG_CTRL_CLK - @mlb_lib.MLB	19B6 91D1
NC_LVDS_IG_CTRL_DATA	NC_LVDS_IG_CTRL_DATA - @mlb_lib.MLB	19B6 91D3
NC_LVDS_IG_DDC_CLK	NC_LVDS_IG_DDC_CLK - @mlb_lib.MLB	19B6 91D2
NC_LVDS_IG_DDC_DATA	NC_LVDS_IG_DDC_DATA - @mlb_lib.MLB	19B6 91D1
NC_LVDS_IG_PANEL_PWR	NC_LVDS_IG_PANEL_PWR - @mlb_lib.MLB	19B6 91D3
NC_LVDS_IG_VREFH	NC_LVDS_IG_VREFH - @mlb_lib.MLB	19B6 91D2
NC_LVDS_IG_VREFL	NC_LVDS_IG_VREFL - @mlb_lib.MLB	19B6 91D1
NC_OBSFN_B0	NC_OBSFN_B0 - @mlb_lib.MLB	24D7 91C3
NC_OBSFN_B1	NC_OBSFN_B1 - @mlb_lib.MLB	24D7 91C2
NC_OBSFN_C0	NC_OBSFN_C0 - @mlb_lib.MLB	24D4 91C1
NC_OBSFN_D01	NC_OBSFN_D01 - @mlb_lib.MLB	24D4 91C3
NC_OBSFN_D11	NC_OBSFN_D11 - @mlb_lib.MLB	24D4 91C2
NC_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN - @mlb_lib.MLB	17C1 91C1
NC_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP - @mlb_lib.MLB	17C1 91C3
NC_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0 - @mlb_lib.MLB	17B1 91C2
NC_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1 - @mlb_lib.MLB	17B1 91C1
NC_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2 - @mlb_lib.MLB	17B1 91C3
NC_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3 - @mlb_lib.MLB	17B1 91C2
NC_PCH_LVDS_IBG	NC_PCH_LVDS_IBG - @mlb_lib.MLB	19B6 91C1
NC_PCH_LVDS_VBG	NC_PCH_LVDS_VBG - @mlb_lib.MLB	19B6 91C3
NC_PCIE_4_D2RN	NC_PCIE_4_D2RN - @mlb_lib.MLB	17D4 91C1
NC_PCIE_4_D2RP	NC_PCIE_4_D2RP - @mlb_lib.MLB	17D4 91C3
NC_PCIE_4_R2D_CN	NC_PCIE_4_R2D_CN - @mlb_lib.MLB	17D4 91C2
NC_PCIE_4_R2D_CP	NC_PCIE_4_R2D_CP - @mlb_lib.MLB	17D4 91C1
NC_PCIE_5_D2RN	NC_PCIE_5_D2RN - @mlb_lib.MLB	17C4 91C3
NC_PCIE_5_D2RP	NC_PCIE_5_D2RP - @mlb_lib.MLB	17C4 91C2
NC_PCIE_5_R2D_CN	NC_PCIE_5_R2D_CN - @mlb_lib.MLB	17C4 91C1
NC_PCIE_5_R2D_CP	NC_PCIE_5_R2D_CP - @mlb_lib.MLB	17C4 91C3
NC_PCIE_6_D2RN	NC_PCIE_6_D2RN - @mlb_lib.MLB	17C4 91C2
NC_PCIE_6_D2RP	NC_PCIE_6_D2RP - @mlb_lib.MLB	17C4 91C1
NC_PCIE_6_R2D_CN	NC_PCIE_6_R2D_CN - @mlb_lib.MLB	17C4 91C3
NC_PCIE_6_R2D_CP	NC_PCIE_6_R2D_CP - @mlb_lib.MLB	17C4 91C2
NC_PCIE_7_D2RN	NC_PCIE_7_D2RN - @mlb_lib.MLB	17C4 91C1
NC_PCIE_7_D2RP	NC_PCIE_7_D2RP - @mlb_lib.MLB	17C4 91C3
NC_PCIE_7_R2D_CN	NC_PCIE_7_R2D_CN - @mlb_lib.MLB	17C4 91C2
NC_PCIE_7_R2D_CP	NC_PCIE_7_R2D_CP - @mlb_lib.MLB	17C4 91C1
NC_PCIE_8_D2RN	NC_PCIE_8_D2RN - @mlb_lib.MLB	17C4 91C3
NC_PCIE_8_D2RP	NC_PCIE_8_D2RP - @mlb_lib.MLB	17C4 91C2
NC_PCIE_8_R2D_CN	NC_PCIE_8_R2D_CN - @mlb_lib.MLB	17C4 91C1
NC_PCIE_8_R2D_CP	NC_PCIE_8_R2D_CP - @mlb_lib.MLB	17C4 91C3
NC_PCIE_CLK100M_EXCARDN	NC_PCIE_CLK100M_EXCARDN - @mlb_lib.MLB	17B4 91C2
NC_PCIE_CLK100M_EXCARDP	NC_PCIE_CLK100M_EXCARDP - @mlb_lib.MLB	17B4 91C1
NC_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N - @mlb_lib.MLB	17B4 91C3
NC_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P - @mlb_lib.MLB	17B4 91C2
NC_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N - @mlb_lib.MLB	20D3 91C1
NC_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P - @mlb_lib.MLB	20D3 91C3
NC_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N - @mlb_lib.MLB	20D3 91C2
NC_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P - @mlb_lib.MLB	20D3 91C1
NC_PCIE_CLK100M_PEBN	NC_PCIE_CLK100M_PEBN - @mlb_lib.MLB	17B4 91C3
NC_PCIE_CLK100M_PEBP	NC_PCIE_CLK100M_PEBP - @mlb_lib.MLB	17B4 91C2
NC_PCIE_CLK100M_T29N	NC_PCIE_CLK100M_T29N - @mlb_lib.MLB	91C1
NC_PCIE_CLK100M_T29P	NC_PCIE_CLK100M_T29P - @mlb_lib.MLB	91C3
NC_PCIE_T29_D2RN<3..0>	NC_PCIE_T29_D2RN<3..0> - @mlb_lib.MLB	91C2
NC_PCIE_T29_D2RP<3..0>	NC_PCIE_T29_D2RP<3..0> - @mlb_lib.MLB	91C1
NC_PCIE_T29_R2D_CN<3..0>	NC_PCIE_T29_R2D_CN<3..0> - @mlb_lib.MLB	91C3
NC_PCIE_T29_R2D_CP<3..0>	NC_PCIE_T29_R2D_CP<3..0> - @mlb_lib.MLB	91C2
NC_PCI_PME_L	NC_PCI_PME_L - @mlb_lib.MLB	19D6 91C2
NC_PEG_CLK100MN	NC_PEG_CLK100MN - @mlb_lib.MLB	8D5 91C1
	PEG_CLK100M_N - @mlb_lib.MLB	8D8 17C1 84C1
NC_PEG_CLK100MP	NC_PEG_CLK100MP - @mlb_lib.MLB	8D5 91C3
	PEG_CLK100M_P - @mlb_lib.MLB	8D8 17C1 84C1
NC_PEG_D2RN<7..0>	NC_PEG_D2RN<7..0> - @mlb_lib.MLB	8D5 91C2
	=PEG_D2R_N<7..0> - @mlb_lib.MLB	8D8
NC_PEG_D2RN<12>	NC_PEG_D2RN<12> - @mlb_lib.MLB	10D5
NC_PEG_D2RN<15..12>	NC_PEG_D2RN<15..12> - @mlb_lib.MLB	91C1
NC_PEG_D2RN<13>	NC_PEG_D2RN<13> - @mlb_lib.MLB	10D5
NC_PEG_D2RN<14>	NC_PEG_D2RN<14> - @mlb_lib.MLB	10C5
NC_PEG_D2RN<15>	NC_PEG_D2RN<15> - @mlb_lib.MLB	10C5
NC_PEG_D2RP<7..0>	NC_PEG_D2RP<7..0> - @mlb_lib.MLB	8D5 91C3
	=PEG_D2R_P<7..0> - @mlb_lib.MLB	8D8
NC_PEG_D2RP<12>	NC_PEG_D2RP<12> - @mlb_lib.MLB	10C5
NC_PEG_D2RP<15..12>	NC_PEG_D2RP<15..12> - @mlb_lib.MLB	91C2
NC_PEG_D2RP<13>	NC_PEG_D2RP<13> - @mlb_lib.MLB	10C5
NC_PEG_D2RP<14>	NC_PEG_D2RP<14> - @mlb_lib.MLB	10C5
NC_PEG_D2RP<15>	NC_PEG_D2RP<15> - @mlb_lib.MLB	10C5
NC_PEG_R2D_CN<7..0>	NC_PEG_R2D_CN<7..0> - @mlb_lib.MLB	8D5 91C1
	=PEG_R2D_C_N<7..0> - @mlb_lib.MLB	8D8
NC_PEG_R2D_CN<12>	NC_PEG_R2D_CN<12> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CN<15..12>	NC_PEG_R2D_CN<15..12> - @mlb_lib.MLB	91C3
NC_PEG_R2D_CN<13>	NC_PEG_R2D_CN<13> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CN<14>	NC_PEG_R2D_CN<14> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CN<15>	NC_PEG_R2D_CN<15> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CP<7..0>	NC_PEG_R2D_CP<7..0> - @mlb_lib.MLB	8D5 91C2
	=PEG_R2D_C_P<7..0> - @mlb_lib.MLB	8D8
NC_PEG_R2D_CP<12>	NC_PEG_R2D_CP<12> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CP<15..12>	NC_PEG_R2D_CP<15..12> - @mlb_lib.MLB	91C1
NC_PEG_R2D_CP<13>	NC_PEG_R2D_CP<13> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CP<14>	NC_PEG_R2D_CP<14> - @mlb_lib.MLB	10B5
NC_PEG_R2D_CP<15>	NC_PEG_R2D_CP<15> - @mlb_lib.MLB	10B5
NC_SATA_C_D2RN	NC_SATA_C_D2RN - @mlb_lib.MLB	17C5 91C3
NC_SATA_C_D2RP	NC_SATA_C_D2RP - @mlb_lib.MLB	17C5 91C2

NC_SATA_C_R2D_CN	NC_SATA_C_R2D_CN - @mlb_lib.MLB	17C5 91C1
NC_SATA_C_R2D_CP	NC_SATA_C_R2D_CP - @mlb_lib.MLB	17C5 91C3
NC_SATA_D_D2RN	NC_SATA_D_D2RN - @mlb_lib.MLB	17C5 91C2
NC_SATA_D_D2RP	NC_SATA_D_D2RP - @mlb_lib.MLB	17C5 91C1
NC_SATA_D_R2D_CN	NC_SATA_D_R2D_CN - @mlb_lib.MLB	17C5 91C3
NC_SATA_D_R2D_CP	NC_SATA_D_R2D_CP - @mlb_lib.MLB	17C5 91C2
NC_SATA_E_D2RN	NC_SATA_E_D2RN - @mlb_lib.MLB	17C5 91C1
NC_SATA_E_D2RP	NC_SATA_E_D2RP - @mlb_lib.MLB	17C5 91C3
NC_SATA_E_R2D_CN	NC_SATA_E_R2D_CN - @mlb_lib.MLB	17C5 91C2
NC_SATA_E_R2D_CP	NC_SATA_E_R2D_CP - @mlb_lib.MLB	17C5 91C1
NC_SATA_F_D2RN	NC_SATA_F_D2RN - @mlb_lib.MLB	17C5 91C3
NC_SATA_F_D2RP	NC_SATA_F_D2RP - @mlb_lib.MLB	17C5 91C2
NC_SATA_F_R2D_CN	NC_SATA_F_R2D_CN - @mlb_lib.MLB	17C5 91C1
NC_SATA_F_R2D_CP	NC_SATA_F_R2D_CP - @mlb_lib.MLB	17C5 91C3
NC_SDVO_INTN	NC_SDVO_INTN - @mlb_lib.MLB	18D1 91C2
NC_SDVO_INTP	NC_SDVO_INTP - @mlb_lib.MLB	18D1 91C1
NC_SDVO_STALLN	NC_SDVO_STALLN - @mlb_lib.MLB	18D1 91C3
NC_SDVO_STALLP	NC_SDVO_STALLP - @mlb_lib.MLB	18D1 91C2
NC_SDVO_TVCLKINN	NC_SDVO_TVCLKINN - @mlb_lib.MLB	18D1 91C1
NC_SDVO_TVCLKINP	NC_SDVO_TVCLKINP - @mlb_lib.MLB	18D1 91B3
NC_SMC_BMON_MUX_SEL	NC_SMC_BMON_MUX_SEL - @mlb_lib.MLB	46C8 91B2
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL - @mlb_lib.MLB	46A8 91B1
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH - @mlb_lib.MLB	46A8 91B3
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL - @mlb_lib.MLB	46A8 91B2
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH - @mlb_lib.MLB	46A8 91B1
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL - @mlb_lib.MLB	46A8 91B3
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH - @mlb_lib.MLB	46A8 91B2
NC_SMC_P10	NC_SMC_P10 - @mlb_lib.MLB	46D8 91B1
NC_SMC_P20	NC_SMC_P20 - @mlb_lib.MLB	46C8 91B3
NC_SMC_P24	NC_SMC_P24 - @mlb_lib.MLB	46C8 91B2
NC_SMC_P41	NC_SMC_P41 - @mlb_lib.MLB	46C8 91B1
NC_SMC_P43	NC_SMC_P43 - @mlb_lib.MLB	46C8 91B3
NC_SMC_PF5	NC_SMC_PF5 - @mlb_lib.MLB	46B5 91B2
NC_SMC_RSTGATE_L	NC_SMC_RSTGATE_L - @mlb_lib.MLB	46D8 91B1
NC_SMC_SYS_KBDLED	NC_SMC_SYS_KBDLED - @mlb_lib.MLB	46C8 91B3
NC_SPI_DESCRIPTOR_OVERRIDE_L	NC_SPI_DESCRIPTOR_OVERRIDE_L - @mlb_lib.MLB	46B8 91B2
NC_T29_D2RN0	NC_T29_D2RN0 - @mlb_lib.MLB	74A5 91A1
NC_T29_D2RN1	NC_T29_D2RN1 - @mlb_lib.MLB	74A5 91A1
NC_T29_D2RP0	NC_T29_D2RP0 - @mlb_lib.MLB	74A5 91A1
NC_T29_D2RP1	NC_T29_D2RP1 - @mlb_lib.MLB	74A5 91A1
NC_T29_PCIE_RESET0_L	NC_T29_PCIE_RESET0_L - @mlb_lib.MLB	74C3 91B1
NC_T29_PCIE_RESET1_L	NC_T29_PCIE_RESET1_L - @mlb_lib.MLB	74C3 91B1
NC_T29_PCIE_RESET2_L	NC_T29_PCIE_RESET2_L - @mlb_lib.MLB	74C3 91B1
NC_T29_PCIE_RESET3_L	NC_T29_PCIE_RESET3_L - @mlb_lib.MLB	74C3 91B1
NC_T29_PWR_EN	NC_T29_PWR_EN - @mlb_lib.MLB	91B1
NC_T29_R2D_CN0	NC_T29_R2D_CN0 - @mlb_lib.MLB	74A5 91B1
NC_T29_R2D_CN1	NC_T29_R2D_CN1 - @mlb_lib.MLB	74A5 91B1
NC_T29_R2D_CP0	NC_T29_R2D_CP0 - @mlb_lib.MLB	74A5 91B1
NC_T29_R2D_CP1	NC_T29_R2D_CP1 - @mlb_lib.MLB	74A5 91B1
NC_USB_1N	NC_USB_1N - @mlb_lib.MLB	19D4 91B3
NC_USB_1P	NC_USB_1P - @mlb_lib.MLB	19D4 91B2
NC_USB_2N	NC_USB_2N - @mlb_lib.MLB	19D4 91B1
NC_USB_2P	NC_USB_2P - @mlb_lib.MLB	19D4 91B3
NC_USB_3N	NC_USB_3N - @mlb_lib.MLB	19D4 91B2
NC_USB_3P	NC_USB_3P - @mlb_lib.MLB	19D4 91B1
NC_USB_4N	NC_USB_4N - @mlb_lib.MLB	19D4 91B3
NC_USB_4P	NC_USB_4P - @mlb_lib.MLB	19D4 91B2
NC_USB_5N	NC_USB_5N - @mlb_lib.MLB	19D4 91B1
NC_USB_5P	NC_USB_5P - @mlb_lib.MLB	19D4 91B3
NC_USB_6N	NC_USB_6N - @mlb_lib.MLB	19D4 91B2
NC_USB_6P	NC_USB_6P - @mlb_lib.MLB	19D4 91B1
NC_USB_7N	NC_USB_7N - @mlb_lib.MLB	19D4 91B3
NC_USB_7P	NC_USB_7P - @mlb_lib.MLB	19D4 91B2
NC_USB_9N	NC_USB_9N - @mlb_lib.MLB	19C4 91B1
NC_USB_9P	NC_USB_9P - @mlb_lib.MLB	19C4 91B3
NC_USB_10N	NC_USB_10N - @mlb_lib.MLB	19C4 91B2
NC_USB_10P	NC_USB_10P - @mlb_lib.MLB	19C4 91B1
NC_USB_11N	NC_USB_11N - @mlb_lib.MLB	19C4 91B3
NC_USB_11P	NC_USB_11P - @mlb_lib.MLB	19C4 91B2
NC_USB_12N	NC_USB_12N - @mlb_lib.MLB	19C4 91B1
NC_USB_12P	NC_USB_12P - @mlb_lib.MLB	19C4 91B3
NC_USB_13N	NC_USB_13N - @mlb_lib.MLB	19C4 91B2
NC_USB_13P	NC_USB_13P - @mlb_lib.MLB	19C4 91B1
ODD_PWR_EN_L	ODD_PWR_EN_L - @mlb_lib.MLB	20D6 20D8
P1V05_DIV_VMON	P1V05_DIV_VMON - @mlb_lib.MLB	62A7
P1V5CPU_EN	P1V5CPU_EN - @mlb_lib.MLB	28C5 61B8
P1V5CPU_EN_L	P1V5CPU_EN_L - @mlb_lib.MLB	28C6
P1V5S0FET_GATE	P1V5S0FET_GATE - @mlb_lib.MLB	61B7
P1V5S0FET_GATE_R	P1V5S0FET_GATE_R - @mlb_lib.MLB	61B6
P1V5S0_EN	P1V5S0_EN - @mlb_lib.MLB	62C1 71A7
P1V5S3_CS_N	P1V5S3_CS_N - @mlb_lib.MLB	50C8 66C1
P1V5S3_CS_P	P1V5S3_CS_P - @mlb_lib.MLB	50B8 66C1
P1V5S3_IOUT	P1V5S3_IOUT - @mlb_lib.MLB	50C7
P1V5VDDQCPU_RAMP_DONE	P1V5VDDQCPU_RAMP_DONE - @mlb_lib.MLB	28C5 61B6
P1V5_DIV_VMON	P1V5_DIV_VMON - @mlb_lib.MLB	62A7
P1V5_S0_DIV	P1V5_S0_DIV - @mlb_lib.MLB	28C4
P1V8S0_EN	P1V8S0_EN - @mlb_lib.MLB	62C1 71C8
P1V8S0_PGOOD	P1V8S0_PGOOD - @mlb_lib.MLB	62A6 71C8
P1V95_FW_NR	P1V95_FW_NR - @mlb_lib.MLB	40D6
P3V3ENET_SS	P3V3ENET_SS - @mlb_lib.MLB	62B2
P3V3S0_EN	P3V3S0_EN - @mlb_lib.MLB	61C4 62C1
	PM_SLP_S3_R_L - @mlb_lib.MLB	62C2
	P5VS0_EN - @mlb_lib.MLB	61A4 62C1
	PM_SLP_S3_R_L - @mlb_lib.MLB	62C2
	P5VS0_EN - @mlb_lib.MLB	61A4 62C1
P3V3S0_EN_L	P3V3S0_EN_L - @mlb_lib.MLB	61C3
P3V3S0_SS	P3V3S0_SS - @mlb_lib.MLB	61C2
P3V3S3_EN_RC	P3V3S3_EN_RC - @mlb_lib.MLB	25B2
P3V3S4_EN	P3V3S4_EN - @mlb_lib.MLB	61D4 62D1
P3V3S4_EN_L	P3V3S4_EN_L - @mlb_lib.MLB	61D3
P3V3S4_GATE	P3V3S4_GATE - @mlb_lib.MLB	61D3
P3V3S5_EN	P3V3S5_EN - @mlb_lib.MLB	61D8 62D6
P3V3S5_EN_L	P3V3S5_EN_L - @mlb_lib.MLB	61D7
P3V3S5_SS	P3V3S5_SS - @mlb_lib.MLB	61D6
P3V3WLAN_SS	P3V3WLAN_SS - @mlb_lib.MLB	35C2
P3V3WLAN_VMON	P3V3WLAN_VMON - @mlb_lib.MLB	35B4
P5V0S0_EN_L	P5V0S0_EN_L - @mlb_lib.MLB	61B3
P5V0S0_SS	P5V0S0_SS - @mlb_lib.MLB	61B3
P5VS5_EN_L	P5VS5_EN_L - @mlb_lib.MLB	61B3
P5VS5_SS	P5VS5_SS - @mlb_lib.MLB	61B2
P5V_DIV_VMON	P5V_DIV_VMON - @mlb_lib.MLB	62A8
P12V_S5_FW_CL	P12V_S5_FW_CL - @mlb_lib.MLB	41D5
P12V_S5_FW_R	P12V_S5_FW_R - @mlb_lib.MLB	41D7
P12V_T29	P12V_T29 - @mlb_lib.MLB	78D2
P33V_S5_FW_D	P33V_S5_FW_D - @mlb_lib.MLB	41D4
PCA9557D_RESET_L	PCA9557D_RESET_L - @mlb_lib.MLB	27C1 33B7
PCH1V05_IOUT	PCH1V05_IOUT - @mlb_lib.MLB	50C6
PCH_A20GATE	PCH_A20GATE - @mlb_lib.MLB	20D4
PCH_CLK14P3M_REFCLK	PCH_CLK14P3M_REFCLK - @mlb_lib.MLB	17A8 17C1 84B3
PCH_CLK25M_X1	PCH_CLK25M_X1 - @mlb_lib.MLB	17B1 26D1
PCH_CLK25M_X2	PCH_CLK25M_X2 - @mlb_lib.MLB	17B1 26D1
	TP_PCH_CLK25M_X2 - @mlb_lib.MLB	26D3
PCH_CLK32K_RTCX1	PCH_CLK32K_RTCX1 - @mlb_lib.MLB	17D8 27C8
PCH_CLK32K_RTCX2	PCH_CLK32K_RTCX2 - @mlb_lib.MLB	17D8 27C8
PCH_CLK32K_RTCX2_R	PCH_CLK32K_RTCX2_R - @mlb_lib.MLB	27C7
PCH_CLK33M_PCIIN	PCH_CLK33M_PCIIN - @mlb_lib.MLB	17C1 27B1 84B3
PCH_CLK33M_PCIOUT	PCH_CLK33M_PCIOUT - @mlb_lib.MLB	19C6 27B4
PCH_CLK96M_DOT_N	PCH_CLK96M_DOT_N - @mlb_lib.MLB	17A8 17C1 84B3
PCH_CLK96M_DOT_P	PCH_CLK96M_DOT_P - @mlb_lib.MLB	17A8 17C1 84B3
PCH_CLK100M_SATA_N	PCH_CLK100M_SATA_N - @mlb_lib.MLB	17A8 17C1 84B3
PCH_CLK100M_SATA_P	PCH_CLK100M_SATA_P - @mlb_lib.MLB	17A8 17C1 84B3
PCH_CLKIN_GNDN1	PCH_CLKIN_GNDN1 - @mlb_lib.MLB	17B1
PCH_CLKIN_GNDP1	PCH_CLKIN_GNDP1 - @mlb_lib.MLB	17B1
PCH_DAC_IREF	PCH_DAC_IREF - @mlb_lib.MLB	18B4
PCH_DF_TVS	PCH_DF_TVS - @mlb_lib.MLB	18B6
PCH_DMI2RBIAS	PCH_DMI2RBIAS - @mlb_lib.MLB	18C8
PCH_DMI_COMP	PCH_DMI_COMP - @mlb_lib.MLB	18C8
PCH_DSWVRMEN	PCH_DSWVRMEN - @mlb_lib.MLB	18B6
PCH_GPIO0	PCH_GPIO0 - @mlb_lib.MLB	20B6 20D6
PCH_GPIO10_OC6_L	PCH_GPIO10_OC6_L - @mlb_lib.MLB	19C1 24C4
PCH_GPIO11	PCH_GPIO11 - @mlb_lib.MLB	17A3 17D1
PCH_GPIO12	PCH_GPIO12 - @mlb_lib.MLB	20C7 20D6
PCH_GPIO14_OC7_L	PCH_GPIO14_OC7_L - @mlb_lib.MLB	19C1 24C4
PCH_GPIO15	PCH_GPIO15 - @mlb_lib.MLB	20A6 20D6 24D4
PCH_GPIO24	PCH_GPIO24 - @mlb_lib.MLB	20C6 20C7
PCH_GPIO36_SATA2GP	PCH_GPIO36_SATA2GP - @mlb_lib.MLB	20A1 20C6
PCH_GPIO43_OC4_L	PCH_GPIO43_OC4_L - @mlb_lib.MLB	19C1 24C4
PCH_GPIO46	PCH_GPIO46 - @mlb_lib.MLB	20A6 20C6
PCH_GPIO52	PCH_GPIO52 - @mlb_lib.MLB	19D6
PCH_GPIO68_TACH4	PCH_GPIO68_TACH4 - @mlb_lib.MLB	20A6 20C6
PCH_GPIO69_TACH5	PCH_GPIO69_TACH5 - @mlb_lib.MLB	20A6 20C6
PCH_GPIO70_TACH6	PCH_GPIO70_TACH6 - @mlb_lib.MLB	20A6 20C6
PCH_GPIO71_TACH7	PCH_GPIO71_TACH7 - @mlb_lib.MLB	20A6 20C6
PCH_INTRUDER_L	PCH_INTRUDER_L - @mlb_lib.MLB	17A7 17D8
PCH_INTVRMEN_L	PCH_INTVRMEN_L - @mlb_lib.MLB	17A7 17D8
PCH_PCI_GNT1_L	PCH_PCI_GNT1_L - @mlb_lib.MLB	19B8 19D6
PCH_PCI_GNT2_L	PCH_PCI_GNT2_L - @mlb_lib.MLB	19B8 19D6
PCH_PCI_GNT3_L	PCH_PCI_GNT3_L - @mlb_lib.MLB	19B8 19D6
PCH_PECI	PCH_PECI - @mlb_lib.MLB	20D4
PCH_PROCPWRGD	PCH_PROCPWRGD - @mlb_lib.MLB	20D4
PCH_RCIN_L	PCH_RCIN_L - @mlb_lib.MLB	20D4
PCH_RI_L	PCH_RI_L - @mlb_lib.MLB	18C8
PCH_SATA3COMP	PCH_SATA3COMP - @mlb_lib.MLB	17B6 83C3
PCH_SATA3RBIAS	PCH_SATA3RBIAS - @mlb_lib.MLB	17B6
PCH_SATAICOMP	PCH_SATAICOMP - @mlb_lib.MLB	17C6 83C3
PCH_SATALED_L	PCH_SATALED_L - @mlb_lib.MLB	17B5 17C5
PCH_SPKR	PCH_SPKR - @mlb_lib.MLB	17B5 17D8
PCH_SRTCRST_L	PCH_SRTCRST_L - @mlb_lib.MLB	17A7 17D8
PCH_SUSACK_L	PCH_SUSACK_L - @mlb_lib.MLB	18B5 18B5
PCH_THRMD_N	PCH_THRMD_N - @mlb_lib.MLB	52B3 52C8
PCH_THRMD_P	PCH_THRMD_P - @mlb_lib.MLB	52C3 52C8
PCH_USB_RBIAS	PCH_USB_RBIAS - @mlb_lib.MLB	19C4 83C3
PCH_XCLK_RCOMP	PCH_XCLK_RCOMP - @mlb_lib.MLB	17B2
PCIECLKRQ5_L_GPIO44	PCIECLKRQ5_L_GPIO44 - @mlb_lib.MLB	17A5 17B4
PCIE_AP_D2R_N	PCIE_AP_D2R_N - @mlb_lib.MLB	17D4 35D4 84D1 91D7
PCIE_AP_D2R_P	PCIE_AP_D2R_P - @mlb_lib.MLB	17D4 35D4 84D1 91D7
PCIE_AP_R2D_C_N	PCIE_AP_R2D_C_N - @mlb_lib.MLB	17D4 35C4 84D1
PCIE_AP_R2D_C_P	PCIE_AP_R2D_C_P - @mlb_lib.MLB	17D4 35C4 84D1
PCIE_AP_R2D_N	PCIE_AP_R2D_N - @mlb_lib.MLB	35C6 84D1 91D7
PCIE_AP_R2D_P	PCIE_AP_R2D_P - @mlb_lib.MLB	35C6 84D1 91D7
PCIE_CLK100M_AP_CONN_N	PCIE_CLK100M_AP_CONN_N - @mlb_lib.MLB	35C6 84C1 91D7
PCIE_CLK100M_AP_CONN_P	PCIE_CLK100M_AP_CONN_P - @mlb_lib.MLB	35C6 84C1 91D7
PCIE_CLK100M_AP_N	PCIE_CLK100M_AP_N - @mlb_lib.MLB	17C4 35D4 84C1
PCIE_CLK100M_AP_P	PCIE_CLK100M_AP_P - @mlb_lib.MLB	17C4 35D4 84C1
PCIE_CLK100M_ENET_N	PCIE_CLK100M_ENET_N - @mlb_lib.MLB	17C4 37B6 84C1
PCIE_CLK100M_ENET_P	PCIE_CLK100M_ENET_P - @mlb_lib.MLB	17C4 37B6 84C1
PCIE_CLK100M_FW_N	PCIE_CLK100M_FW_N - @mlb_lib.MLB	17C4 39C6 84C1
PCIE_CLK100M_FW_P	PCIE_CLK100M_FW_P - @mlb_lib.MLB	17C4 39C6 84C1
PCIE_CLK100M_PCH_N	PCIE_CLK100M_PCH_N - @mlb_lib.MLB	17A8 17C1 84C1
PCIE_CLK100M_PCH_P	PCIE_CLK100M_PCH_P - @mlb_lib.MLB	17A8 17C1 84C1
PCIE_CLK100M_T29_N	PCIE_CLK100M_T29_N - @mlb_lib.MLB	17B4 74C2 84C1
PCIE_CLK100M_T29_P	PCIE_CLK100M_T29_P - @mlb_lib.MLB	17B4 74C2 84C1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @mlb_lib.MLB	37C6 84D1
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @mlb_lib.MLB	37C6 84D1
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @mlb_lib.MLB	17D4 37C8 84D1
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @mlb_lib.MLB	17D4 37C8 84D1
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @mlb_lib.MLB	17D4 37B8 84D1
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @mlb_lib.MLB	17D4 37C8 84D1
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @mlb_lib.MLB	37C6 84D1
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @mlb_lib.MLB	37C6 84D1
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @mlb_lib.MLB	39C6 84C1
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @mlb_lib.MLB	39C6 84C1
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @mlb_lib.MLB	17D4 39C8 84D1
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @mlb_lib.MLB	17D4 39C8 84D1
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @mlb_lib.MLB	17D4 39C8 84D1
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @mlb_lib.MLB	17D4 39C8 84D1
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @mlb_lib.MLB	39C6 84D1
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @mlb_lib.MLB	39C6 84D1
PCIE_T29_D2R_C_N<0>	PCIE_T29_D2R_C_N<0> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_N<3..0>	PCIE_T29_D2R_C_N<3..0> - @mlb_lib.MLB	84C1
PCIE_T29_D2R_C_N<1>	PCIE_T29_D2R_C_N<1> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_N<2>	PCIE_T29_D2R_C_N<2> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_N<3>	PCIE_T29_D2R_C_N<3> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_P<0>	PCIE_T29_D2R_C_P<0> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_P<3..0>	PCIE_T29_D2R_C_P<3..0> - @mlb_lib.MLB	84C1
PCIE_T29_D2R_C_P<1>	PCIE_T29_D2R_C_P<1> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_P<2>	PCIE_T29_D2R_C_P<2> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_C_P<3>	PCIE_T29_D2R_C_P<3> - @mlb_lib.MLB	74D3
PCIE_T29_D2R_N<0>	PCIE_T29_D2R_N<0> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_N<3..0>	PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C5 84C1
	=PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_N<1>	PCIE_T29_D2R_N<1> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_N<2>	PCIE_T29_D2R_N<2> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_N<3>	PCIE_T29_D2R_N<3> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_P<0>	PCIE_T29_D2R_P<0> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_P<3..0>	PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C5 84C1
	=PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_P<1>	PCIE_T29_D2R_P<1> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_P<2>	PCIE_T29_D2R_P<2> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_D2R_P<3>	PCIE_T29_D2R_P<3> - @mlb_lib.MLB	74D1
	=PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C8
PCIE_T29_R2D_C_N<0>	PCIE_T29_R2D_C_N<0> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_N<3..0>	PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B5 84C1
	=PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_N<1>	PCIE_T29_R2D_C_N<1> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_N<2>	PCIE_T29_R2D_C_N<2> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_N<3>	PCIE_T29_R2D_C_N<3> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_N<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_P<0>	PCIE_T29_R2D_C_P<0> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_P<3..0>	PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B5 84C1
	=PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_P<1>	PCIE_T29_R2D_C_P<1> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_P<2>	PCIE_T29_R2D_C_P<2> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_C_P<3>	PCIE_T29_R2D_C_P<3> - @mlb_lib.MLB	74D7
	=PCIE_T29_R2D_C_P<3..0> - @mlb_lib.MLB	8B8
PCIE_T29_R2D_N<0>	PCIE_T29_R2D_N<0> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_N<3..0>	PCIE_T29_R2D_N<3..0> - @mlb_lib.MLB	84C1
PCIE_T29_R2D_N<1>	PCIE_T29_R2D_N<1> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_N<2>	PCIE_T29_R2D_N<2> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_N<3>	PCIE_T29_R2D_N<3> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_P<0>	PCIE_T29_R2D_P<0> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_P<3..0>	PCIE_T29_R2D_P<3..0> - @mlb_lib.MLB	84C1
PCIE_T29_R2D_P<1>	PCIE_T29_R2D_P<1> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_P<2>	PCIE_T29_R2D_P<2> - @mlb_lib.MLB	74D5
PCIE_T29_R2D_P<3>	PCIE_T29_R2D_P<3> - @mlb_lib.MLB	74D5
PCIE_WAKE_L	PCIE_WAKE_L - @mlb_lib.MLB	18A6 18C5 35D8 38C3 77A8 91D7
PCI_INTA_L	PCI_INTA_L - @mlb_lib.MLB	19D6
PCI_INTB_L	PCI_INTB_L - @mlb_lib.MLB	19D6
PCI_INTC_L	PCI_INTC_L - @mlb_lib.MLB	19D6
PCI_INTD_L	PCI_INTD_L - @mlb_lib.MLB	19D6
PCI_INTE_L	PCI_INTE_L - @mlb_lib.MLB	19D6
PCI_REQ3_L	PCI_REQ3_L - @mlb_lib.MLB	19D6
PDCINVSENS_EN_L_DIV	PDCINVSENS_EN_L_DIV - @mlb_lib.MLB	51C3
PD_DP_T29SNK1_HPD	PD_DP_T29SNK1_HPD - @mlb_lib.MLB	74A5
PD_DP_T29SRC_HPD	PD_DP_T29SRC_HPD - @mlb_lib.MLB	74B3
PD_HDMI_LS_RSV0	PD_HDMI_LS_RSV0 - @mlb_lib.MLB	79C5
PD_PCH_INIT3V3_L	PD_PCH_INIT3V3_L - @mlb_lib.MLB	20A4
PD_SMC_SPARE_SENSE	PD_SMC_SPARE_SENSE - @mlb_lib.MLB	46C5 47B2
PEG_B_CLKRQ_L_GPIO56	PEG_B_CLKRQ_L_GPIO56 - @mlb_lib.MLB	17B4 17B5
PEG_CLKREQ_L	PEG_CLKREQ_L - @mlb_lib.MLB	17B4 17B5
PEG_D2R_C_N<7..0>	PEG_D2R_C_N<7..0> - @mlb_lib.MLB	81A3
PEG_D2R_C_P<7..0>	PEG_D2R_C_P<7..0> - @mlb_lib.MLB	81A3
PEG_D2R_N<7..0>	PEG_D2R_N<7..0> - @mlb_lib.MLB	81A3
PEG_D2R_P<7..0>	PEG_D2R_P<7..0> - @mlb_lib.MLB	81A3
PEG_R2D_C_N<7..0>	PEG_R2D_C_N<7..0> - @mlb_lib.MLB	81A3
PEG_R2D_C_P<7..0>	PEG_R2D_C_P<7..0> - @mlb_lib.MLB	81A3
PEG_R2D_N<7..0>	PEG_R2D_N<7..0> - @mlb_lib.MLB	81A3
PEG_R2D_P<7..0>	PEG_R2D_P<7..0> - @mlb_lib.MLB	81A3
PERIPHDET_FILT	PERIPHDET_FILT - @mlb_lib.MLB	58B3
PLT_RESET2_L	PLT_RESET2_L - @mlb_lib.MLB	27D3 28B5
PLT_RESET_L	PLT_RESET_L - @mlb_lib.MLB	19D6 27D4
PLT_RESET_LS1V1_L	PLT_RESET_LS1V1_L - @mlb_lib.MLB	11B6
PM_BATLOW_L	PM_BATLOW_L - @mlb_lib.MLB	18C8 46B8
PM_CLK32K_SUSCLK_R	PM_CLK32K_SUSCLK_R - @mlb_lib.MLB	18C5 47C6
PM_CLKRUN_L	PM_CLKRUN_L - @mlb_lib.MLB	18A4 18C5 46C5 48C5
PM_DPRSLPVR	PM_DPRSLPVR - @mlb_lib.MLB	81B3
PM_ENET_EN_L	PM_ENET_EN_L - @mlb_lib.MLB	62B3
PM_EN_PVCORE_CPU	PM_EN_PVCORE_CPU - @mlb_lib.MLB	62C4 67B3
PM_MEM_PWRGD	PM_MEM_PWRGD - @mlb_lib.MLB	11C7 18C8 28D1 81C3
PM_MEM_PWRGD_L	PM_MEM_PWRGD_L - @mlb_lib.MLB	28C3
PM_MEM_PWRGD_R	PM_MEM_PWRGD_R - @mlb_lib.MLB	11C6
PM_P3V3_G3H_PG	PM_P3V3_G3H_PG - @mlb_lib.MLB	65C8
PM_P5V_S4_PG	PM_P5V_S4_PG - @mlb_lib.MLB	62A6 65A8 78C8
PM_PCH_PWROK	PM_PCH_PWROK - @mlb_lib.MLB	18C8 18C8 20B3 20B3 20C3 27A5
PM_PCH_SYS_PWROK	PM_PCH_SYS_PWROK - @mlb_lib.MLB	18C8 24C8 27A5
PM_PECI_PWRGD	PM_PECI_PWRGD - @mlb_lib.MLB	46A4 62C4
PM_PECI_PWRGD_R	PM_PECI_PWRGD_R - @mlb_lib.MLB	46A5
PM_PGOOD_P3V3_2V8_A	PM_PGOOD_P3V3_2V8_A - @mlb_lib.MLB	78C7
PM_PGOOD_PVAXG	PM_PGOOD_PVAXG - @mlb_lib.MLB	67B3
PM_PGOOD_PVCORE_CPU	PM_PGOOD_PVCORE_CPU - @mlb_lib.MLB	27A8 62B6 67C6
PM_PWRBTN_L	PM_PWRBTN_L - @mlb_lib.MLB	18A6 18C8 24C8 46C8
PM_RSMRST_L	PM_RSMRST_L - @mlb_lib.MLB	18C8 46D8
PM_S0_PGOOD	PM_S0_PGOOD - @mlb_lib.MLB	27A7
PM_SLP_S3_L	PM_SLP_S3_L - @mlb_lib.MLB	18A5 18C5 28C5 46C5 51C4 62A4 62C4 91B5
PM_SLP_S4_L	PM_SLP_S4_L - @mlb_lib.MLB	18A5 18C5 28D6 46C5 62D6 91B5
	DDRREG_EN - @mlb_lib.MLB	62D4 66C8
PM_SLP_S5_L	PM_SLP_S5_L - @mlb_lib.MLB	18A5 18C5 46C5 62D3 91B5
	P5VS4_EN - @mlb_lib.MLB	62D1 65B8
PM_SYNC	PM_SYNC - @mlb_lib.MLB	11C6 18C5 81C3
PM_SYSRST_L	PM_SYSRST_L - @mlb_lib.MLB	18C8 27A3 46B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @mlb_lib.MLB	11C6 20C2 81B3
PM_THRMTRIP_L_R	PM_THRMTRIP_L_R - @mlb_lib.MLB	20D4 47C4
PM_WLAN_EN_L	PM_WLAN_EN_L - @mlb_lib.MLB	35C1 62A2
POWER_BTN_N	POWER_BTN_N - @mlb_lib.MLB	45A3 91B7
POWER_BTN_P	POWER_BTN_P - @mlb_lib.MLB	45B3 91B7
PP0V75_S0_DDRVTT	PP0V75_S0_DDRVTT - @mlb_lib.MLB	7C4 28B3 30A5 30A7 30C2 31A5 31A7 31C2 66C5 91B5
PP0V75_S3_MEM_VREFCA_A	PP0V75_S3_MEM_VREFCA_A - @mlb_lib.MLB	30B5 30C2 33C1
PP0V75_S3_MEM_VREFCA_B	PP0V75_S3_MEM_VREFCA_B - @mlb_lib.MLB	31B5 31C2 33C1
PP0V75_S3_MEM_VREFDQ_A	PP0V75_S3_MEM_VREFDQ_A - @mlb_lib.MLB	10B3 30D2 30D7 33D1
PP0V75_S3_MEM_VREFDQ_B	PP0V75_S3_MEM_VREFDQ_B - @mlb_lib.MLB	10B3 31D2 31D7 33D1
PP1V2_ENET	PP1V2_ENET - @mlb_lib.MLB	6D3 37D2 38C5 91C5
PP1V2_ENET_PHY_AVDDL	PP1V2_ENET_PHY_AVDDL - @mlb_lib.MLB	37D3
PP1V2_ENET_PHY_GPHYPLL	PP1V2_ENET_PHY_GPHYPLL - @mlb_lib.MLB	37C3
PP1V2_ENET_PHY_PCIEPLL	PP1V2_ENET_PHY_PCIEPLL - @mlb_lib.MLB	37D3
PP1V05_S0_PCH	PP1V05_S0_PCH - @mlb_lib.MLB	7D4 17C5 17C5 17D2 18D8 21B1 21B1 21B5 21B7 21B7 21B7 21B7 21C1 21C4 21C4 21C4 21C5 21C5 21C5 21C5 21C7 21C7 23B2 23B2 23B6 23C1 23C2 23C2 23C5 23D1 23D2 23D2 23D5 23D8 50C8
PP1V05_S0_PCH_VCCADPLLA_F	PP1V05_S0_PCH_VCCADPLLA_F - @mlb_lib.MLB	21B8 23B3
PP1V05_S0_PCH_VCCADPLLA_R	PP1V05_S0_PCH_VCCADPLLA_R - @mlb_lib.MLB	23B5
PP1V05_S0_PCH_VCCADPLLB_F	PP1V05_S0_PCH_VCCADPLLB_F - @mlb_lib.MLB	21B8 23B3
PP1V05_S0_PCH_VCCADPLLB_R	PP1V05_S0_PCH_VCCADPLLB_R - @mlb_lib.MLB	23B5
PP1V05_S0_PCH_VCCCLKDMI_F	PP1V05_S0_PCH_VCCCLKDMI_F - @mlb_lib.MLB	21C1 23D6
PP1V05_S0_PCH_VCCCLKDMI_R	PP1V05_S0_PCH_VCCCLKDMI_R - @mlb_lib.MLB	23D7
PP1V05_S0_VCCIO	PP1V05_S0_VCCIO - @mlb_lib.MLB	7D4 10C8 10D4 11B7 11C7 13B5 13B5 13D6 15B8 67B6 91B5
	PP1V05_S0 - @mlb_lib.MLB	7D4 24B3 24B4 24D1 24D6 46A4 50C8 62A7 62B8 70C1 76A8
PP1V05_S0_VCCQ	PP1V05_S0_VCCQ - @mlb_lib.MLB	11D3 13B6 15A6
PP1V05_S5_PCH	PP1V05_S5_PCH - @mlb_lib.MLB	24B3
PP1V05_T29	PP1V05_T29 - @mlb_lib.MLB	75D8 76A6 76C6
PP1V05_T29_VDD_DP	PP1V05_T29_VDD_DP - @mlb_lib.MLB	75C7
PP1V05_T29_VDD_DPPLL	PP1V05_T29_VDD_DPPLL - @mlb_lib.MLB	75C7
PP1V5_FW_VDDA	PP1V5_FW_VDDA - @mlb_lib.MLB	39D2
PP1V5_S0	PP1V5_S0 - @mlb_lib.MLB	7C7 17B4 21B5 23D4 39D1 53D7 71B5 72B3 91B5
PP1V5_S3	PP1V5_S3 - @mlb_lib.MLB	6B3 28B5 30C5 30C7 30D4 31C5 31C7 31D4 32B6 61B7 66C1 66C6 72B3 91C5
PP1V5_S3_CPU_VCCDQ	PP1V5_S3_CPU_VCCDQ - @mlb_lib.MLB	13C1 16A6
PP1V5_S3_REG	PP1V5_S3_REG - @mlb_lib.MLB	66C3
PP1V5_VDDQ_CPU	PP1V5_VDDQ_CPU - @mlb_lib.MLB	7A4 11C7 13B2 13D2 16B8 28D4 31A5 32B6 50D8 62A8 62C8
PP1V5_VDDQ_CPU_R	PP1V5_VDDQ_CPU_R - @mlb_lib.MLB	7B4 50D8 61B5
PP1V8_S0	PP1V8_S0 - @mlb_lib.MLB	7D4 15B3 18C5 21B1 21B7 21C1 21C1 21C5 23D3 26D7 71B7 71D4
PP1V8_S0_CPU_VCCPLL_R	PP1V8_S0_CPU_VCCPLL_R - @mlb_lib.MLB	7C4 13B4 15B1
PP1V96_FW_PLLVDD	PP1V96_FW_PLLVDD - @mlb_lib.MLB	39D2
PP1V96_FW_XTAL	PP1V96_FW_XTAL - @mlb_lib.MLB	39C1
PP1V96_S0_FW	PP1V96_S0_FW - @mlb_lib.MLB	39D1 40D5
PP2V2_FW_ESD	PP2V2_FW_ESD - @mlb_lib.MLB	41A6 41B2 41C4 41C4
PP3V3R1V8_ENET_LR_OUT	PP3V3R1V8_ENET_LR_OUT - @mlb_lib.MLB	37C1 37D5
PP3V3R2V8_DPAPWR_D	PP3V3R2V8_DPAPWR_D - @mlb_lib.MLB	78D7
PP3V3R12V_SW_DPAPWR	PP3V3R12V_SW_DPAPWR - @mlb_lib.MLB	78C6 78D1 78D4
PP3V3R12V_SW_DPAPWR_F	PP3V3R12V_SW_DPAPWR_F - @mlb_lib.MLB	78C4 91B5
PP3V3_ENET	PP3V3_ENET - @mlb_lib.MLB	6D3 26D7 26D7 37A8 37D8 38C2 38D7 62B1 91C5
PP3V3_ENET_PHY_AVDDH	PP3V3_ENET_PHY_AVDDH - @mlb_lib.MLB	37C6
PP3V3_ENET_PHY_BIASVDDH	PP3V3_ENET_PHY_BIASVDDH - @mlb_lib.MLB	37D6
PP3V3_ENET_PHY_XTALVDDH	PP3V3_ENET_PHY_XTALVDDH - @mlb_lib.MLB	37D6
PP3V3_FW_AVDD	PP3V3_FW_AVDD - @mlb_lib.MLB	39D7
PP3V3_FW_PLLVDD	PP3V3_FW_PLLVDD - @mlb_lib.MLB	39D7
PP3V3_FW_VDDA	PP3V3_FW_VDDA - @mlb_lib.MLB	39D7
PP3V3_G3H	PP3V3_G3H - @mlb_lib.MLB	6B7 6D2 6D3 27D7 43D5 45B2 46D4 47C1 47D8 48D5 61C4 61D4 61D8 65C3 65D7 91A5 91C5
PP3V3_G3_RTC	PP3V3_G3_RTC - @mlb_lib.MLB	6D7 17B8 18B5 21B8 27D6 91C5
PP3V3_S0	PP3V3_S0 - @mlb_lib.MLB	6C2 7C7 13B6 17A6 17B7 17C5 17D5 18B5 19D8 20A5 20A8 20B8 20D2 20D7 21B4 21C1 21C5 21C5 23A6 23A6 23A8 23A8 23C6 23C8 23C8 24D7 27A4 27A7 27C4 27C4 30A7 30B3 31A7 31B3 34D4 37C7 38A5 39B8 39C1 39D8 40B7 40D7 41B4 47D3 49A8 49B3 49B5 49B8 49D5 49D8 50B7 50B7 50D3 50D7 50D8 51C7 51D7 52B6 52D7 53A8 53D1 57B8 58A4 58D4 60C7 60C7 61C1 62A7 62B6 62C8 67D2 67D5 71D8 72C7 73C5 74A7 76B8 76C8 77B5 77C4 77C8 77D6 79A7 79C2 79C7 79D1 89C1 91C5
PP3V3_S0_AUDIO_F	PP3V3_S0_AUDIO_F - @mlb_lib.MLB	58A3 58A7 58B4 58B8 58C8
PP3V3_S0_HS_RX	PP3V3_S0_HS_RX - @mlb_lib.MLB	58D3
PP3V3_S0_PCH_VCC3_3_CLK_F	PP3V3_S0_PCH_VCC3_3_CLK_F - @mlb_lib.MLB	21D8 23C3
PP3V3_S0_PCH_VCC3_3_CLK_R	PP3V3_S0_PCH_VCC3_3_CLK_R - @mlb_lib.MLB	23C5
PP3V3_S0_PCH_VCCA_DAC_F	PP3V3_S0_PCH_VCCA_DAC_F - @mlb_lib.MLB	21B1 23C6
PP3V3_S4	PP3V3_S4 - @mlb_lib.MLB	6B3 6D2 19C2 20B3 20C3 20C3 25A3 25B3 25C3 25C3 25C3 25C8 25D8 28B8 28C7 28C7 33D8 34B6 34C5 35B3 35C1 35C4 38B4 47B4 47B4 49C3 49C5 50C7 50D8 61D1 77B6 77C2 78C6 91C5
PP3V3_S4_BT_F	PP3V3_S4_BT_F - @mlb_lib.MLB	35C6 91D7
PP3V3_S4_VREFMRGN_CTRL	PP3V3_S4_VREFMRGN_CTRL - @mlb_lib.MLB	33C7
PP3V3_S4_VREFMRGN_DAC	PP3V3_S4_VREFMRGN_DAC - @mlb_lib.MLB	33D7
PP3V3_S5	PP3V3_S5 - @mlb_lib.MLB	6A7 17A3 17A6 17B7 18A8 18A8 18D8 19C2 20A7 20B7 20C8 21B5 21B5 21C1 21D5 21D8 23B8 23C4 23D1 23D4 23D5 24B3 24B8 24C2 25C3 27A6 27A7 28D4 59C6 61D5 62B3 62C7 62D8 78C7 89C1 91C5
PP3V3_S5_AVREF_SMC	PP3V3_S5_AVREF_SMC - @mlb_lib.MLB	46D4 47D6 91B5

PP3V3_S5_SMC_AVCC	PP3V3_S5_SMC_AVCC - @mlb_lib.MLB	46D3
PP3V3_SW_SD_PWR	PP3V3_SW_SD_PWR - @mlb_lib.MLB	34D2 91C7
PP3V3_T29	PP3V3_T29 - @mlb_lib.MLB	17B6 20B3 20B8 26D7 74C2 74C6 74D2 75D1 76B6 76C6
PP3V3_T29_DP	PP3V3_T29_DP - @mlb_lib.MLB	75D3
PP3V3_T29_DPBIAS	PP3V3_T29_DPBIAS - @mlb_lib.MLB	75C4
PP3V3_T29_PLL	PP3V3_T29_PLL - @mlb_lib.MLB	75C4
PP3V3_U5300	PP3V3_U5300 - @mlb_lib.MLB	50D6
PP3V3_WLAN	PP3V3_WLAN - @mlb_lib.MLB	35C6 35D7 47A1 91D7
PP3V3_WLAN_FET	PP3V3_WLAN_FET - @mlb_lib.MLB	35C3
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @mlb_lib.MLB	53A3 53C5 53D1 53D7 91B5
PP5V_AUDIO_HPAMP	PP5V_AUDIO_HPAMP - @mlb_lib.MLB	53A6 55D6
PP5V_G3H	PP5V_G3H - @mlb_lib.MLB	6B7 45D6 47D8 61C4 65B7 65D5 91C5
PP5V_HDMI_DDC_CONN	PP5V_HDMI_DDC_CONN - @mlb_lib.MLB	80B6 80C1 91B5
PP5V_HDMI_DDC_FUSE	PP5V_HDMI_DDC_FUSE - @mlb_lib.MLB	80B5 80D2
PP5V_S0	PP5V_S0 - @mlb_lib.MLB	7D7 23C8 24B4 24B4 41A5 41B8 42D3 42D6 48D5 61B1 62A8 64C6 67D5 68C7 68D7 69D8 70C6 71B7 80D4 91B7 91C5 91C7
PP5V_S0_AUDIO	PP5V_S0_AUDIO - @mlb_lib.MLB	7D7 53A8
PP5V_S0_AUDIO_AMP	PP5V_S0_AUDIO_AMP - @mlb_lib.MLB	7C7 56C6
PP5V_S0_CPUVCCIOS0_VCC	PP5V_S0_CPUVCCIOS0_VCC - @mlb_lib.MLB	70C6
PP5V_S0_CPU_VCORE_VCC	PP5V_S0_CPU_VCORE_VCC - @mlb_lib.MLB	67B1 67B4 67B8 67C7 67D4
PP5V_S0_PCH_V5REF	PP5V_S0_PCH_V5REF - @mlb_lib.MLB	21D5 23B6
PP5V_S0_VCCSAS0_VCC	PP5V_S0_VCCSAS0_VCC - @mlb_lib.MLB	64C6
PP5V_S4	PP5V_S4 - @mlb_lib.MLB	6C3 28B3 28B6 43C8 43D8 44C6 45D4 61B4 61B8 65B2 66C7 78D6 78D8 91C5
PP5V_S4_DDRREG_V5IN	PP5V_S4_DDRREG_V5IN - @mlb_lib.MLB	66C7
PP5V_S4_IR_R	PP5V_S4_IR_R - @mlb_lib.MLB	44C3 44C5
PP5V_S5	PP5V_S5 - @mlb_lib.MLB	6A7 23B8 61C1
PP5V_SUS_PCH_V5REFSUS	PP5V_SUS_PCH_V5REFSUS - @mlb_lib.MLB	21B5 23B7
PP5V_U7100_PVCC	PP5V_U7100_PVCC - @mlb_lib.MLB	64C5
PP5V_U7700_PVCC	PP5V_U7700_PVCC - @mlb_lib.MLB	70C6
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @mlb_lib.MLB	43B6
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @mlb_lib.MLB	43B4
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @mlb_lib.MLB	43C6
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @mlb_lib.MLB	43C4
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @mlb_lib.MLB	43C6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @mlb_lib.MLB	43C2
PP5V_USB2_PORT3	PP5V_USB2_PORT3 - @mlb_lib.MLB	43D5
PP5V_USB2_PORT3_F	PP5V_USB2_PORT3_F - @mlb_lib.MLB	43D2
PP12V_G3H	PP12V_G3H - @mlb_lib.MLB	6C7 41D8 51C8 51D4 51D8 60D7 65B8 65C4 65D3 72C3 78D4
PP12V_G3H_CPUDDR	PP12V_G3H_CPUDDR - @mlb_lib.MLB	6C6 51C8 64D5 66D6 68D6 69D3 70D5
PP12V_G3H_DDRS3REG_FILT	PP12V_G3H_DDRS3REG_FILT - @mlb_lib.MLB	66D4
PP12V_G3H_GPU	PP12V_G3H_GPU - @mlb_lib.MLB	6C6
PP12V_G3H_PSU	PP12V_G3H_PSU - @mlb_lib.MLB	6C7 51D8 72B5 91D5
PP12V_S0_AXG_FLTRD	PP12V_S0_AXG_FLTRD - @mlb_lib.MLB	69D5
PP12V_S0_CPU_FLTRD	PP12V_S0_CPU_FLTRD - @mlb_lib.MLB	67B2 68C3 68D2
PP12V_S0_FAN	PP12V_S0_FAN - @mlb_lib.MLB	60D4
PP12V_S0_FAN0_F	PP12V_S0_FAN0_F - @mlb_lib.MLB	60C3 91D5
PPCPUVCCIO_S0_REG_R	PPCPUVCCIO_S0_REG_R - @mlb_lib.MLB	70C3
PPDDRVREF_S3	PPDDRVREF_S3 - @mlb_lib.MLB	6A3 33D3 66B5 91C5
PPIRRCVR_F	PPIRRCVR_F - @mlb_lib.MLB	45D2 91B7
PPIRRCVR_G3H_LED	PPIRRCVR_G3H_LED - @mlb_lib.MLB	45D3
PPUSB_HUB1_CRFILT	PPUSB_HUB1_CRFILT - @mlb_lib.MLB	25D5
PPUSB_HUB1_PLLFILT	PPUSB_HUB1_PLLFILT - @mlb_lib.MLB	25D5
PPUSB_HUB2_CRFILT	PPUSB_HUB2_CRFILT - @mlb_lib.MLB	25B5
PPUSB_HUB2_PLLFILT	PPUSB_HUB2_PLLFILT - @mlb_lib.MLB	25B5
PPVAXG_S0_CPU	PPVAXG_S0_CPU - @mlb_lib.MLB	7B7 13D4 16D8 50B3 67D8 69C1
PPVAXG_S0_CPU_RS	PPVAXG_S0_CPU_RS - @mlb_lib.MLB	69C4
PPVBATT_G3_RTC	PPVBATT_G3_RTC - @mlb_lib.MLB	6D7 27D8
PPVBATT_G3_RTC_R	PPVBATT_G3_RTC_R - @mlb_lib.MLB	27D7
PPVCCSA_S0_CPU	PPVCCSA_S0_CPU - @mlb_lib.MLB	7B7 13B4 13C1 16B4 50A7 64C1
PPVCCSA_S0_REG_R	PPVCCSA_S0_REG_R - @mlb_lib.MLB	64C3
PPVCORE_S0_CPU	PPVCORE_S0_CPU - @mlb_lib.MLB	7B7 10D4 10D4 13D8 15D8 50C3 67A8 68A4 68C2 68D2 91B5
PPVOUT_G3_PCH_DCPRTC	PPVOUT_G3_PCH_DCPRTC - @mlb_lib.MLB	21C8
PPVOUT_S0_PCH_DCPSST	PPVOUT_S0_PCH_DCPSST - @mlb_lib.MLB	21B8
PPVP_FW_PHY_CPS	PPVP_FW_PHY_CPS - @mlb_lib.MLB	39B1 41D3
PSU_TEMP	PSU_TEMP - @mlb_lib.MLB	46C5 72C5 91C5
PU_FW_VP	PU_FW_VP - @mlb_lib.MLB	39D2
PU_HDMI_LS_RSV1	PU_HDMI_LS_RSV1 - @mlb_lib.MLB	79B6
PU_SDCONN_OC_L	PU_SDCONN_OC_L - @mlb_lib.MLB	34D3
PU_USB1_PRT4N	PU_USB1_PRT4N - @mlb_lib.MLB	25C5
PU_USB1_PRT4P	PU_USB1_PRT4P - @mlb_lib.MLB	25C5
PU_USB2_PRT4N	PU_USB2_PRT4N - @mlb_lib.MLB	25A5
PU_USB2_PRT4P	PU_USB2_PRT4P - @mlb_lib.MLB	25A5
PVCCIO_S0_SMC_R	PVCCIO_S0_SMC_R - @mlb_lib.MLB	46A5
PVCCSA_EN	PVCCSA_EN - @mlb_lib.MLB	62C1 64C6
PVCCSA_PGOOD	PVCCSA_PGOOD - @mlb_lib.MLB	62A6 64C6
RTC_RESET_L	RTC_RESET_L - @mlb_lib.MLB	17A7 17D8
RT_1V8S0	RT_1V8S0 - @mlb_lib.MLB	71C6
S0PGD_BJT_GND_R	S0PGD_BJT_GND_R - @mlb_lib.MLB	62B6
S0PGD_C	S0PGD_C - @mlb_lib.MLB	62C7
S5_PWRGD	S5_PWRGD - @mlb_lib.MLB	46D8 62D7
SATARDRVR_EN	SATARDRVR_EN - @mlb_lib.MLB	17A5 17C5
SATA_HDD1_D2R_CONN_N	SATA_HDD1_D2R_CONN_N - @mlb_lib.MLB	42B5 42D7 83D3 91C7
SATA_HDD1_D2R_CONN_P	SATA_HDD1_D2R_CONN_P - @mlb_lib.MLB	42B5 42D7 83D3 91C7
SATA_HDD1_D2R_DF_N	SATA_HDD1_D2R_DF_N - @mlb_lib.MLB	42A7 83D3
SATA_HDD1_D2R_DF_P	SATA_HDD1_D2R_DF_P - @mlb_lib.MLB	42B7 83D3
SATA_HDD1_D2R_N	SATA_HDD1_D2R_N - @mlb_lib.MLB	17D5 42B8 83D3
SATA_HDD1_D2R_P	SATA_HDD1_D2R_P - @mlb_lib.MLB	17D5 42B8 83D3
SATA_HDD1_R2D_CONN_N	SATA_HDD1_R2D_CONN_N - @mlb_lib.MLB	42B5 42C7 83D3 91C7
SATA_HDD1_R2D_CONN_P	SATA_HDD1_R2D_CONN_P - @mlb_lib.MLB	42C5 42C7 83D3 91C7
SATA_HDD1_R2D_C_N	SATA_HDD1_R2D_C_N - @mlb_lib.MLB	17D5 42B8 83D3
SATA_HDD1_R2D_C_P	SATA_HDD1_R2D_C_P - @mlb_lib.MLB	17D5 42C8 83D3
SATA_HDD1_R2D_DF_N	SATA_HDD1_R2D_DF_N - @mlb_lib.MLB	42B7 83D3
SATA_HDD1_R2D_DF_P	SATA_HDD1_R2D_DF_P - @mlb_lib.MLB	42C7 83D3
SATA_HDD2_D2R_CONN_N	SATA_HDD2_D2R_CONN_N - @mlb_lib.MLB	42B1 42D4 83D3 91B7
SATA_HDD2_D2R_CONN_P	SATA_HDD2_D2R_CONN_P - @mlb_lib.MLB	42B1 42D4 83D3 91B7
SATA_HDD2_D2R_DF_N	SATA_HDD2_D2R_DF_N - @mlb_lib.MLB	42A3 83D3
SATA_HDD2_D2R_DF_P	SATA_HDD2_D2R_DF_P - @mlb_lib.MLB	42B3 83C3
SATA_HDD2_D2R_N	SATA_HDD2_D2R_N - @mlb_lib.MLB	17D5 42B4 83D3
SATA_HDD2_D2R_P	SATA_HDD2_D2R_P - @mlb_lib.MLB	17D5 42B4 83D3
SATA_HDD2_R2D_CONN_N	SATA_HDD2_R2D_CONN_N - @mlb_lib.MLB	42B1 42C4 83D3 91B7
SATA_HDD2_R2D_CONN_P	SATA_HDD2_R2D_CONN_P - @mlb_lib.MLB	42C1 42C4 83D3 91B7
SATA_HDD2_R2D_C_N	SATA_HDD2_R2D_C_N - @mlb_lib.MLB	17D5 42B4 83D3
SATA_HDD2_R2D_C_P	SATA_HDD2_R2D_C_P - @mlb_lib.MLB	17D5 42C4 83D3
SATA_HDD2_R2D_DF_N	SATA_HDD2_R2D_DF_N - @mlb_lib.MLB	42B3 83C3
SATA_HDD2_R2D_DF_P	SATA_HDD2_R2D_DF_P - @mlb_lib.MLB	42C3 83C3
SDCONNF_CLK	SDCONNF_CLK - @mlb_lib.MLB	34C5 85C3

SDCONNF_CLK_FF	SDCONNF_CLK_FF - @mlb_lib.MLB	34C6 85C3
SDCONN_CLK	SDCONN_CLK - @mlb_lib.MLB	34C7 37B1 85C3 91C7
SDCONN_CLK_FF	SDCONN_CLK_FF - @mlb_lib.MLB	34C4 85C3
SDCONN_CLK_R	SDCONN_CLK_R - @mlb_lib.MLB	34C3 85C3
SDCONN_CMD	SDCONN_CMD - @mlb_lib.MLB	34C5 37B1 85C3 91C7
SDCONN_CMD_R	SDCONN_CMD_R - @mlb_lib.MLB	34C3 34D7 85C3
SDCONN_DATA<0>	SDCONN_DATA<0> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<7..0>	SDCONN_DATA<7..0> - @mlb_lib.MLB	85C3 91C7
SDCONN_DATA<1>	SDCONN_DATA<1> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<2>	SDCONN_DATA<2> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<3>	SDCONN_DATA<3> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<4>	SDCONN_DATA<4> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<5>	SDCONN_DATA<5> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<6>	SDCONN_DATA<6> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA<7>	SDCONN_DATA<7> - @mlb_lib.MLB	34C5 37B1
SDCONN_DATA_R<0>	SDCONN_DATA_R<0> - @mlb_lib.MLB	34C3 34D7
SDCONN_DATA_R<7..0>	SDCONN_DATA_R<7..0> - @mlb_lib.MLB	85C3
SDCONN_DATA_R<1>	SDCONN_DATA_R<1> - @mlb_lib.MLB	34C3 34D7
SDCONN_DATA_R<2>	SDCONN_DATA_R<2> - @mlb_lib.MLB	34C3 34D7
SDCONN_DATA_R<3>	SDCONN_DATA_R<3> - @mlb_lib.MLB	34C3 34C7
SDCONN_DATA_R<4>	SDCONN_DATA_R<4> - @mlb_lib.MLB	34C3 34C7
SDCONN_DATA_R<5>	SDCONN_DATA_R<5> - @mlb_lib.MLB	34C3 34C7
SDCONN_DATA_R<6>	SDCONN_DATA_R<6> - @mlb_lib.MLB	34C3 34C7
SDCONN_DATA_R<7>	SDCONN_DATA_R<7> - @mlb_lib.MLB	34C3 34C7
SDCONN_DETECT	SDCONN_DETECT - @mlb_lib.MLB	34B6 34C3 34C7 91C7
SDCONN_DETECT_L	SDCONN_DETECT_L - @mlb_lib.MLB	34B5
SDCONN_STATE_CHANGE	SDCONN_STATE_CHANGE - @mlb_lib.MLB	19C1 24C4 34B2
SDCONN_STATE_CHANGE_S1R	SDCONN_STATE_CHANGE_S1R - @mlb_lib.MLB	34B4
SDCONN_STATE_CHANGE_S2R	SDCONN_STATE_CHANGE_S2R - @mlb_lib.MLB	34A4
SDCONN_WP	SDCONN_WP - @mlb_lib.MLB	34C3 34C7 37B1 91C7
SLG_ENET_RESET_L	SLG_ENET_RESET_L - @mlb_lib.MLB	34B7
SLG_ENET_RESET_R_L	SLG_ENET_RESET_R_L - @mlb_lib.MLB	34B4
SMBUS_PCH_CLK	SMBUS_PCH_CLK - @mlb_lib.MLB	17D1 49D8 84D3
SMBUS_PCH_DATA	SMBUS_PCH_DATA - @mlb_lib.MLB	17D1 49D8 84C3
SMBUS_SMC_0_S0_SCL	SMBUS_SMC_0_S0_SCL - @mlb_lib.MLB	46B8 49D6 87D3
	=I2C_T29THMSNS_SCL - @mlb_lib.MLB	49D3 52B5
SMBUS_SMC_0_S0_SDA	SMBUS_SMC_0_S0_SDA - @mlb_lib.MLB	46C5 49D6 87D3
	=I2C_T29THMSNS_SDA - @mlb_lib.MLB	49D3 52B5
SMBUS_SMC_A_S3_SCL	SMBUS_SMC_A_S3_SCL - @mlb_lib.MLB	46A5 49C6 87D3
	=SMBUS_REMOTE_THMSNS_SCL - @mlb_lib.MLB	49C3
SMBUS_SMC_A_S3_SDA	SMBUS_SMC_A_S3_SDA - @mlb_lib.MLB	46A5 49C6 87D3
	=SMBUS_REMOTE_THMSNS_SDA - @mlb_lib.MLB	49C3
SMBUS_SMC_B_S0_SCL	SMBUS_SMC_B_S0_SCL - @mlb_lib.MLB	46A5 49A5 87D3
SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA - @mlb_lib.MLB	46A5 49A5 87D3
SMBUS_SMC_MGMT_SCL	SMBUS_SMC_MGMT_SCL - @mlb_lib.MLB	46C5 49C3 87D3
SMBUS_SMC_MGMT_SDA	SMBUS_SMC_MGMT_SDA - @mlb_lib.MLB	46C8 49C3 87D3
SMB_PCH_DIMM_SCL	SMB_PCH_DIMM_SCL - @mlb_lib.MLB	49D6 84D3
	=I2C_SODIMMB_SCL - @mlb_lib.MLB	31A5 49C6
	=I2C_SODIMMA_SCL - @mlb_lib.MLB	30A5 49D6
	=I2C_SODIMMB_SCL - @mlb_lib.MLB	31A5 49C6
	=I2C_SODIMMA_SCL - @mlb_lib.MLB	30A5 49D6
SMB_PCH_DIMM_SDA	SMB_PCH_DIMM_SDA - @mlb_lib.MLB	49D6 84D3
	=I2C_SODIMMB_SDA - @mlb_lib.MLB	31A5 49C6
	=I2C_SODIMMA_SDA - @mlb_lib.MLB	30A5 49C6
	=I2C_SODIMMB_SDA - @mlb_lib.MLB	31A5 49C6
	=I2C_SODIMMA_SDA - @mlb_lib.MLB	30A5 49C6
SMB_PCH_MKY_SCL	SMB_PCH_MKY_SCL - @mlb_lib.MLB	49C6 84D3
	=I2C_MIKEY_SCL - @mlb_lib.MLB	49C6 58D5
SMB_PCH_MKY_SDA	SMB_PCH_MKY_SDA - @mlb_lib.MLB	49C6 84D3
	=I2C_MIKEY_SDA - @mlb_lib.MLB	49C6 58D5
SMB_PCH_STR_SCL	SMB_PCH_STR_SCL - @mlb_lib.MLB	49D6 84D3
SMB_PCH_STR_SDA	SMB_PCH_STR_SDA - @mlb_lib.MLB	49D6 84D3
SMB_PCH_VRF_SCL	SMB_PCH_VRF_SCL - @mlb_lib.MLB	49D8 84D3
	=I2C_PCA9557D_SCL - @mlb_lib.MLB	33C7 49C8
	=I2C_VREFDACS_SCL - @mlb_lib.MLB	33D7 49C8
	=I2C_PCA9557D_SCL - @mlb_lib.MLB	33C7 49C8
SMB_PCH_VRF_SDA	SMB_PCH_VRF_SDA - @mlb_lib.MLB	49D8 84D3
	=I2C_PCA9557D_SDA - @mlb_lib.MLB	33C7 49C8
	=I2C_VREFDACS_SDA - @mlb_lib.MLB	33D7 49C8
	=I2C_PCA9557D_SDA - @mlb_lib.MLB	33C7 49C8
SMB_PCH_XDP_SCL	SMB_PCH_XDP_SCL - @mlb_lib.MLB	49C8 84C3
	=SMBUS_XDP_SCL - @mlb_lib.MLB	24C7 49B8
SMB_PCH_XDP_SDA	SMB_PCH_XDP_SDA - @mlb_lib.MLB	49C8 84C3
	=SMBUS_XDP_SDA - @mlb_lib.MLB	24C7 49B8
SMB_SMC_B_STR_SCL	SMB_SMC_B_STR_SCL - @mlb_lib.MLB	49A5 87D3
SMB_SMC_B_STR_SDA	SMB_SMC_B_STR_SDA - @mlb_lib.MLB	49A5 87D3
SMB_SMC_B_TSN_SCL	SMB_SMC_B_TSN_SCL - @mlb_lib.MLB	49A3 87D3
	=I2C_CPUTHMSNS_SCL - @mlb_lib.MLB	49A3 52D5
SMB_SMC_B_TSN_SDA	SMB_SMC_B_TSN_SDA - @mlb_lib.MLB	49A3 87D3
	=I2C_CPUTHMSNS_SDA - @mlb_lib.MLB	49A3 52D5
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @mlb_lib.MLB	18C8 46D5 47B2
SMC_BC_ACOK	SMC_BC_ACOK - @mlb_lib.MLB	46C5 47B2
SMC_BIL_BUTTON_L	SMC_BIL_BUTTON_L - @mlb_lib.MLB	46C5 47B2
SMC_CASE_OPEN	SMC_CASE_OPEN - @mlb_lib.MLB	46B5 47B2
SMC_CLK32K	SMC_CLK32K - @mlb_lib.MLB	46C5 47C4
SMC_CPUDDR_HI_ISENSE	SMC_CPUDDR_HI_ISENSE - @mlb_lib.MLB	46A8 51C5
SMC_CPUP1V5_ISENSE	SMC_CPUP1V5_ISENSE - @mlb_lib.MLB	46A8 50D5
SMC_CPUVCCIO_ISENSE	SMC_CPUVCCIO_ISENSE - @mlb_lib.MLB	46C5 50B5
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @mlb_lib.MLB	46C5 50D1
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @mlb_lib.MLB	46C5 50C1
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE - @mlb_lib.MLB	46A8 51D5
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE - @mlb_lib.MLB	46A8 51D1
SMC_DELAYED_PWRGD	SMC_DELAYED_PWRGD - @mlb_lib.MLB	27A7 46D8
SMC_DP_HPD_L	SMC_DP_HPD_L - @mlb_lib.MLB	46B8 47B4 77A4
SMC_EXTAL	SMC_EXTAL - @mlb_lib.MLB	46C3 47B8
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @mlb_lib.MLB	46B8 60C8
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @mlb_lib.MLB	46A8 60C8
SMC_GFX_ISENSE	SMC_GFX_ISENSE - @mlb_lib.MLB	46C5 50B1
SMC_GFX_OVERTEMP	SMC_GFX_OVERTEMP - @mlb_lib.MLB	46B8 73B6
SMC_GFX_VSENSE	SMC_GFX_VSENSE - @mlb_lib.MLB	46C5 50B1
SMC_GPU_HI_ISENSE	SMC_GPU_HI_ISENSE - @mlb_lib.MLB	46A8 73B6
SMC_KBC_MDE	SMC_KBC_MDE - @mlb_lib.MLB	46D2
SMC_LID	SMC_LID - @mlb_lib.MLB	46B5 47C2
SMC_LRESET_L	SMC_LRESET_L - @mlb_lib.MLB	27C1 46C8
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @mlb_lib.MLB	47D8
SMC_MD1	SMC_MD1 - @mlb_lib.MLB	46D1 48C5
SMC_NMI	SMC_NMI - @mlb_lib.MLB	46C1 48C3
SMC_ODD_DETECT	SMC_ODD_DETECT - @mlb_lib.MLB	46B8 47B2
SMC_ONOFF_L	SMC_ONOFF_L - @mlb_lib.MLB	45B2 46C5
SMC_P1V5S3_ISENSE	SMC_P1V5S3_ISENSE - @mlb_lib.MLB	46C5 50C5
SMC_PA0_PU	SMC_PA0_PU - @mlb_lib.MLB	46B8 47B2
SMC_PB4	SMC_PB4 - @mlb_lib.MLB	46B8 47B2
SMC_PCH1V05_ISENSE	SMC_PCH1V05_ISENSE - @mlb_lib.MLB	46A8 50C5
SMC_PME_S4_WAKE_L	SMC_PME_S4_WAKE_L - @mlb_lib.MLB	46C5 47A4 47A6
SMC_PM_G2_EN	SMC_PM_G2_EN - @mlb_lib.MLB	46D5 47B2 62D8 91B5
	P5VS5_EN - @mlb_lib.MLB	61B4 62D6
SMC_PROCHOT	SMC_PROCHOT - @mlb_lib.MLB	46A5 47C1
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @mlb_lib.MLB	46D5 47D1
SMC_RESET_L	SMC_RESET_L - @mlb_lib.MLB	46D3 47D6 48C3
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @mlb_lib.MLB	20A4 20D6 46B8

SMC_RX_L	SMC_RX_L - @mlb_lib.MLB	43D5 46B8 46C5 47B2 48C3
SMC_S4_WAKESRC_EN	SMC_S4_WAKESRC_EN - @mlb_lib.MLB	46B8 47B2
SMC_SCI_L	SMC_SCI_L - @mlb_lib.MLB	20A6 20C6 46C5
SMC_SYS_LED	SMC_SYS_LED - @mlb_lib.MLB	6C2 45C7 46B5
SMC_SYS_LED_DR	SMC_SYS_LED_DR - @mlb_lib.MLB	45C5 91B7
SMC_SYS_LED_IREF	SMC_SYS_LED_IREF - @mlb_lib.MLB	45C6
SMC_SYS_LED_IREF_M	SMC_SYS_LED_IREF_M - @mlb_lib.MLB	45D6
SMC_SYS_LED_IREF_S	SMC_SYS_LED_IREF_S - @mlb_lib.MLB	45D5
SMC_SYS_LED_L	SMC_SYS_LED_L - @mlb_lib.MLB	45C6
SMC_SYS_LED_R	SMC_SYS_LED_R - @mlb_lib.MLB	45C6
SMC_TCK	SMC_TCK - @mlb_lib.MLB	46B5 47B2 48C3
SMC_TDI	SMC_TDI - @mlb_lib.MLB	46B5 47B2 48C3
SMC_TDO	SMC_TDO - @mlb_lib.MLB	46B5 47B2 48C5
SMC_THRMTRIP	SMC_THRMTRIP - @mlb_lib.MLB	46A5 47C1
SMC_TMS	SMC_TMS - @mlb_lib.MLB	46B5 47B2 48C5
SMC_TRST_L	SMC_TRST_L - @mlb_lib.MLB	46C1 48C5
SMC_TX_L	SMC_TX_L - @mlb_lib.MLB	43D5 46B8 46C5 47B2 48C5
SMC_VCCSA_ISENSE	SMC_VCCSA_ISENSE - @mlb_lib.MLB	46A8 50A5
SMC_VCCSA_VSENSE	SMC_VCCSA_VSENSE - @mlb_lib.MLB	46A8 50A5
SMC_VCL	SMC_VCL - @mlb_lib.MLB	46D2
SMC_XTAL	SMC_XTAL - @mlb_lib.MLB	46C3 47B8
SMC_XTAL_R	SMC_XTAL_R - @mlb_lib.MLB	47B7
SML_PCH_0_ALERT_L	SML_PCH_0_ALERT_L - @mlb_lib.MLB	17A3 17D1
SML_PCH_0_CLK	SML_PCH_0_CLK - @mlb_lib.MLB	17D1 49B8
SML_PCH_0_DATA	SML_PCH_0_DATA - @mlb_lib.MLB	17D1 49B8
SML_PCH_1_ALERT_L	SML_PCH_1_ALERT_L - @mlb_lib.MLB	17A3 17D1
SML_PCH_1_CLK	SML_PCH_1_CLK - @mlb_lib.MLB	17D1 49A8 84C3
SML_PCH_1_DATA	SML_PCH_1_DATA - @mlb_lib.MLB	17D1 49A8 84C3
SMS_INT_L	SMS_INT_L - @mlb_lib.MLB	46B5 47B2
SMT_THRM_SNS3_N	SMT_THRM_SNS3_N - @mlb_lib.MLB	52A7
SMT_THRM_SNS3_P	SMT_THRM_SNS3_P - @mlb_lib.MLB	52A7
SNS_1V8S0	SNS_1V8S0 - @mlb_lib.MLB	71C6
SNS_T1_ADDR	SNS_T1_ADDR - @mlb_lib.MLB	52D6
SNS_T1_ALERT_L	SNS_T1_ALERT_L - @mlb_lib.MLB	52D6
SNS_T1_TRIPSET	SNS_T1_TRIPSET - @mlb_lib.MLB	52D6
SNS_T2_ADDR	SNS_T2_ADDR - @mlb_lib.MLB	52B6
SNS_T2_ALERT_L	SNS_T2_ALERT_L - @mlb_lib.MLB	52B6
SPIROM_USE_MLB	SPIROM_USE_MLB - @mlb_lib.MLB	20C6 20C7 48C3 59B5 91A5
SPI_ALT_CLK	SPI_ALT_CLK - @mlb_lib.MLB	48B3 48C3
SPI_ALT_CS_L	SPI_ALT_CS_L - @mlb_lib.MLB	48B3 48C3
SPI_ALT_MISO	SPI_ALT_MISO - @mlb_lib.MLB	48B3 48C5
SPI_ALT_MOSI	SPI_ALT_MOSI - @mlb_lib.MLB	48B3 48C5
SPI_CLK	SPI_CLK - @mlb_lib.MLB	48B5 84C3 91A5
SPI_CLK_R	SPI_CLK_R - @mlb_lib.MLB	17C8 48B6 84C3
SPI_CS0_L	SPI_CS0_L - @mlb_lib.MLB	48B5 84C3 91A5
SPI_CS0_R_L	SPI_CS0_R_L - @mlb_lib.MLB	17C8 48B6 84C3
SPI_MISO	SPI_MISO - @mlb_lib.MLB	17C8 48A6 84C3 91A5
SPI_MLB_CLK	SPI_MLB_CLK - @mlb_lib.MLB	48B3 59C5
SPI_MLB_CS_L	SPI_MLB_CS_L - @mlb_lib.MLB	48B3 59C5
SPI_MLB_MISO	SPI_MLB_MISO - @mlb_lib.MLB	48A3 59C4
SPI_MLB_MOSI	SPI_MLB_MOSI - @mlb_lib.MLB	48A3 59C4
SPI_MOSI	SPI_MOSI - @mlb_lib.MLB	48A5 84C3 91A5
SPI_MOSI_R	SPI_MOSI_R - @mlb_lib.MLB	17C8 48A6 84C3
SPI_WP_L	SPI_WP_L - @mlb_lib.MLB	59C5
SPKRAMP_M_N_OUT	SPKRAMP_M_N_OUT - @mlb_lib.MLB	56B3 57B2 91D5
SPKRAMP_M_P_OUT	SPKRAMP_M_P_OUT - @mlb_lib.MLB	56B3 57B2 91D5
SS_1V8S0	SS_1V8S0 - @mlb_lib.MLB	71C7
SUSWARN_L	SUSWARN_L - @mlb_lib.MLB	18A6 18B7 18C8
SW_1V8S0	SW_1V8S0 - @mlb_lib.MLB	71D6
SYSCLK_CLK25M_ENET_SR	SYSCLK_CLK25M_ENET_SR - @mlb_lib.MLB	26C4
SYSCLK_CLK25M_SB	SYSCLK_CLK25M_SB - @mlb_lib.MLB	26C4
SYSCLK_CLK25M_T29	SYSCLK_CLK25M_T29 - @mlb_lib.MLB	26C2 74C1
SYSCLK_CLK25M_T29_R	SYSCLK_CLK25M_T29_R - @mlb_lib.MLB	74C3
SYSCLK_CLK25M_T29_SR	SYSCLK_CLK25M_T29_SR - @mlb_lib.MLB	26C4
SYSCLK_CLK25M_X1	SYSCLK_CLK25M_X1 - @mlb_lib.MLB	26C6
SYSCLK_CLK25M_X2	SYSCLK_CLK25M_X2 - @mlb_lib.MLB	26C7
SYSCLK_CLK25M_X2_R	SYSCLK_CLK25M_X2_R - @mlb_lib.MLB	26C6
SYS_ONEWIRE	SYS_ONEWIRE - @mlb_lib.MLB	46B8 47B2
SYS_PWROK_R	SYS_PWROK_R - @mlb_lib.MLB	27A6
T29DPA_CONFIG1_RC	T29DPA_CONFIG1_RC - @mlb_lib.MLB	77A4 78A8
T29DPA_CONFIG2_RC	T29DPA_CONFIG2_RC - @mlb_lib.MLB	77A4 78A8
T29DPA_D2R1_AUXCH_CC_N	T29DPA_D2R1_AUXCH_CC_N - @mlb_lib.MLB	86A3
T29DPA_D2R1_AUXCH_CC_P	T29DPA_D2R1_AUXCH_CC_P - @mlb_lib.MLB	86A3
T29DPA_D2R1_AUXCH_N	T29DPA_D2R1_AUXCH_N - @mlb_lib.MLB	78B6 86B3
T29DPA_D2R1_AUXCH_P	T29DPA_D2R1_AUXCH_P - @mlb_lib.MLB	78B6 86B3
T29DPA_HPD	T29DPA_HPD - @mlb_lib.MLB	77A7 78A8
T29DPA_HPD_R	T29DPA_HPD_R - @mlb_lib.MLB	78A5
T29DPA_ML_C_N<0>	T29DPA_ML_C_N<0> - @mlb_lib.MLB	77D1 78B1
T29DPA_ML_C_N<3..0>	T29DPA_ML_C_N<3..0> - @mlb_lib.MLB	86B3
T29DPA_ML_C_N<2>	T29DPA_ML_C_N<2> - @mlb_lib.MLB	77D1 78B1
T29DPA_ML_C_P<0>	T29DPA_ML_C_P<0> - @mlb_lib.MLB	77D1 78B1
T29DPA_ML_C_P<3..0>	T29DPA_ML_C_P<3..0> - @mlb_lib.MLB	86B3
T29DPA_ML_C_P<2>	T29DPA_ML_C_P<2> - @mlb_lib.MLB	77D1 78B1
T29DPA_ML_N<0>	T29DPA_ML_N<0> - @mlb_lib.MLB	78B3
T29DPA_ML_N<3..0>	T29DPA_ML_N<3..0> - @mlb_lib.MLB	86B3
T29DPA_ML_N<1>	T29DPA_ML_N<1> - @mlb_lib.MLB	77B1 78B1
T29DPA_ML_N<2>	T29DPA_ML_N<2> - @mlb_lib.MLB	78B3
T29DPA_ML_N<3>	T29DPA_ML_N<3> - @mlb_lib.MLB	77B1 78B8
T29DPA_ML_P<0>	T29DPA_ML_P<0> - @mlb_lib.MLB	78B3
T29DPA_ML_P<3..0>	T29DPA_ML_P<3..0> - @mlb_lib.MLB	86B3
T29DPA_ML_P<1>	T29DPA_ML_P<1> - @mlb_lib.MLB	77B1 78B1
T29DPA_ML_P<2>	T29DPA_ML_P<2> - @mlb_lib.MLB	78B3
T29DPA_ML_P<3>	T29DPA_ML_P<3> - @mlb_lib.MLB	77B1 78B8
T29ROM_HOLD_L	T29ROM_HOLD_L - @mlb_lib.MLB	74C8
T29ROM_WP_L	T29ROM_WP_L - @mlb_lib.MLB	74C8
T29_A_BIAS	T29_A_BIAS - @mlb_lib.MLB	76B3 77A8 77B3 78C6
T29_A_BIAS0N	T29_A_BIAS0N - @mlb_lib.MLB	76B1 77D4
T29_A_BIAS0P	T29_A_BIAS0P - @mlb_lib.MLB	76B1 77D4
T29_A_BIAS1N	T29_A_BIAS1N - @mlb_lib.MLB	76B1 78B8
T29_A_BIAS1P	T29_A_BIAS1P - @mlb_lib.MLB	76B1 78B8
T29_A_BIAS2N	T29_A_BIAS2N - @mlb_lib.MLB	76A1 77C4
T29_A_BIAS2P	T29_A_BIAS2P - @mlb_lib.MLB	76A1 77D4
T29_A_HV_EN	T29_A_HV_EN - @mlb_lib.MLB	77A3 78C4
T29_A_HV_EN_R	T29_A_HV_EN_R - @mlb_lib.MLB	77A5
T29_A_LSX_P2R	T29_A_LSX_P2R - @mlb_lib.MLB	77A5
T29_A_LSX_R2P	T29_A_LSX_R2P - @mlb_lib.MLB	77A5
T29_A_RSVD_N	T29_A_RSVD_N - @mlb_lib.MLB	77B3
T29_A_RSVD_P	T29_A_RSVD_P - @mlb_lib.MLB	77B3
T29_A_UC_ADDR	T29_A_UC_ADDR - @mlb_lib.MLB	77A4 77A8
T29_CLKREQ_ISOL_L	T29_CLKREQ_ISOL_L - @mlb_lib.MLB	74C5 76B6
T29_CLKREQ_L	T29_CLKREQ_L - @mlb_lib.MLB	17B4 17B5 76B8
T29_D2R1_BIASN	T29_D2R1_BIASN - @mlb_lib.MLB	77B3
T29_D2R1_BIASP	T29_D2R1_BIASP - @mlb_lib.MLB	77B3
T29_D2R_CC_N<0>	T29_D2R_CC_N<0> - @mlb_lib.MLB	86A3
T29_D2R_CC_P<0>	T29_D2R_CC_P<0> - @mlb_lib.MLB	86A3
T29_D2R_C_N<0>	T29_D2R_C_N<0> - @mlb_lib.MLB	77D1 78B8 86C3
T29_D2R_C_N<1>	T29_D2R_C_N<1> - @mlb_lib.MLB	77D1 78B8 86C3
T29_D2R_C_P<0>	T29_D2R_C_P<0> - @mlb_lib.MLB	77D1 78B8 86C3
T29_D2R_C_P<1>	T29_D2R_C_P<1> - @mlb_lib.MLB	77D1 78B8 86C3
T29_D2R_N<0>	T29_D2R_N<0> - @mlb_lib.MLB	74A3 77D5
T29_D2R_N<3..0>	T29_D2R_N<3..0> - @mlb_lib.MLB	86C3

T29_D2R_N<1>	T29_D2R_N<1> - @mlb_lib.MLB	74A3 77D5
T29_D2R_P<0>	T29_D2R_P<0> - @mlb_lib.MLB	74A3 77D5
T29_D2R_P<3..0>	T29_D2R_P<3..0> - @mlb_lib.MLB	86C3
T29_D2R_P<1>	T29_D2R_P<1> - @mlb_lib.MLB	74A3 77D5
T29_DP_ATEST	T29_DP_ATEST - @mlb_lib.MLB	74B3
T29_DP_A_PWR_EN	T29_DP_A_PWR_EN - @mlb_lib.MLB	78C7 78D8
T29_DP_PORTA_PWR_EN	T29_DP_PORTA_PWR_EN - @mlb_lib.MLB	19C1 24D4 78C8
T29_DP_RES	T29_DP_RES - @mlb_lib.MLB	74B3
T29_GPIO<1>	T29_GPIO<1> - @mlb_lib.MLB	74C5
T29_GPIO<2>	T29_GPIO<2> - @mlb_lib.MLB	74C5
T29_LSEO<0>	T29_LSEO<0> - @mlb_lib.MLB	74A3 77A7
T29_LSEO<1>	T29_LSEO<1> - @mlb_lib.MLB	74A3 77A4
T29_LSEO_LSOE0	T29_LSEO_LSOE0 - @mlb_lib.MLB	74A5
T29_LSEO_LSOE1	T29_LSEO_LSOE1 - @mlb_lib.MLB	74A5
T29_LSOE<0>	T29_LSOE<0> - @mlb_lib.MLB	74A3 77A7
T29_LSOE<1>	T29_LSOE<1> - @mlb_lib.MLB	74A3 77A7
T29_MCU_INT_L	T29_MCU_INT_L - @mlb_lib.MLB	19D6 77A7
T29_MONDC0	T29_MONDC0 - @mlb_lib.MLB	74D5
T29_MONDC1	T29_MONDC1 - @mlb_lib.MLB	74D5
T29_MONOBSN	T29_MONOBSN - @mlb_lib.MLB	74C5
T29_MONOBSP	T29_MONOBSP - @mlb_lib.MLB	74D5
T29_PCIE_WAKE_L	T29_PCIE_WAKE_L - @mlb_lib.MLB	74D3
T29_PWR_EN	T29_PWR_EN - @mlb_lib.MLB	20B1 76A8
T29_PWR_EN_PCH	T29_PWR_EN_PCH - @mlb_lib.MLB	17D5 20B3
T29_PWR_EN_U2916	T29_PWR_EN_U2916 - @mlb_lib.MLB	76A7
T29_R2D_C_F_N<0>	T29_R2D_C_F_N<0> - @mlb_lib.MLB	77D4
T29_R2D_C_F_N<1..0>	T29_R2D_C_F_N<1..0> - @mlb_lib.MLB	86B3
T29_R2D_C_F_N<1>	T29_R2D_C_F_N<1> - @mlb_lib.MLB	77D4
T29_R2D_C_F_P<0>	T29_R2D_C_F_P<0> - @mlb_lib.MLB	77D4
T29_R2D_C_F_P<1..0>	T29_R2D_C_F_P<1..0> - @mlb_lib.MLB	86B3
T29_R2D_C_F_P<1>	T29_R2D_C_F_P<1> - @mlb_lib.MLB	77D4
T29_R2D_C_N<0>	T29_R2D_C_N<0> - @mlb_lib.MLB	74A3 77D5
T29_R2D_C_N<3..0>	T29_R2D_C_N<3..0> - @mlb_lib.MLB	86C3
T29_R2D_C_N<1>	T29_R2D_C_N<1> - @mlb_lib.MLB	74A3 77D5
T29_R2D_C_P<0>	T29_R2D_C_P<0> - @mlb_lib.MLB	74A3 77D5
T29_R2D_C_P<3..0>	T29_R2D_C_P<3..0> - @mlb_lib.MLB	86C3
T29_R2D_C_P<1>	T29_R2D_C_P<1> - @mlb_lib.MLB	74A3 77D5
T29_R2D_N<0>	T29_R2D_N<0> - @mlb_lib.MLB	77D3 86C3
T29_R2D_N<1>	T29_R2D_N<1> - @mlb_lib.MLB	77D3 86C3
T29_R2D_P<0>	T29_R2D_P<0> - @mlb_lib.MLB	77D3 86C3
T29_R2D_P<1>	T29_R2D_P<1> - @mlb_lib.MLB	77D3 86C3
T29_RBIAS	T29_RBIAS - @mlb_lib.MLB	74C3
T29_RESET_L	T29_RESET_L - @mlb_lib.MLB	74D2 76C6
T29_RSENSE	T29_RSENSE - @mlb_lib.MLB	74D3
T29_RSVD	T29_RSVD - @mlb_lib.MLB	74C5
T29_SPI_CLK	T29_SPI_CLK - @mlb_lib.MLB	74C5 86C3
T29_SPI_CS_L	T29_SPI_CS_L - @mlb_lib.MLB	74C5 86C3
T29_SPI_MISO	T29_SPI_MISO - @mlb_lib.MLB	74C5 86C3
T29_SPI_MOSI	T29_SPI_MOSI - @mlb_lib.MLB	74C5 86C3
T29_SW_RESET_L	T29_SW_RESET_L - @mlb_lib.MLB	20A4 20C6 76B8
T29_TEST_EN	T29_TEST_EN - @mlb_lib.MLB	74C5
T29_TEST_POINT_3	T29_TEST_POINT_3 - @mlb_lib.MLB	74C5
T29_THERMD_N	T29_THERMD_N - @mlb_lib.MLB	89B1
T29_THERMD_P	T29_THERMD_P - @mlb_lib.MLB	89B1
T29_TMU_CLK_IN	T29_TMU_CLK_IN - @mlb_lib.MLB	74C3
T29_TMU_CLK_OUT	T29_TMU_CLK_OUT - @mlb_lib.MLB	74C3
TIPDET_UNFILT	TIPDET_UNFILT - @mlb_lib.MLB	58A3 58D4
TP_1V05_S0_PCH_VCCAPLLEXP	TP_1V05_S0_PCH_VCCAPLLEXP - @mlb_lib.MLB	21C4
TP_AUD_DMIC_CLK	TP_AUD_DMIC_CLK - @mlb_lib.MLB	53C2
TP_BCM57765_SPD100LED_L	TP_BCM57765_SPD100LED_L - @mlb_lib.MLB	37B6
TP_BCM57765_TRAFFICLED_L	TP_BCM57765_TRAFFICLED_L - @mlb_lib.MLB	37B6
TP_CLK98M_TS_L	TP_CLK98M_TS_L - @mlb_lib.MLB	39C1
TP_CPU_CFG<8>	TP_CPU_CFG<8> - @mlb_lib.MLB	10D3
TP_CPU_CFG<9>	TP_CPU_CFG<9> - @mlb_lib.MLB	10D3
TP_CPU_CFG<10>	TP_CPU_CFG<10> - @mlb_lib.MLB	10D3
TP_CPU_CFG<11>	TP_CPU_CFG<11> - @mlb_lib.MLB	10D3
TP_CPU_CFG<12>	TP_CPU_CFG<12> - @mlb_lib.MLB	10D3
TP_CPU_CFG<13>	TP_CPU_CFG<13> - @mlb_lib.MLB	10D3
TP_CPU_CFG<14>	TP_CPU_CFG<14> - @mlb_lib.MLB	10D3
TP_CPU_CFG<15>	TP_CPU_CFG<15> - @mlb_lib.MLB	10D3
TP_CPU_CFG<17>	TP_CPU_CFG<17> - @mlb_lib.MLB	10D3
TP_CPU_DC_TEST_A4	TP_CPU_DC_TEST_A4 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_A58	TP_CPU_DC_TEST_A58 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_BD1	TP_CPU_DC_TEST_BD1 - @mlb_lib.MLB	10B1
TP_CPU_DC_TEST_BD61	TP_CPU_DC_TEST_BD61 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_BG4	TP_CPU_DC_TEST_BG4 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_BG58	TP_CPU_DC_TEST_BG58 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_D1	TP_CPU_DC_TEST_D1 - @mlb_lib.MLB	10C1
TP_CPU_DC_TEST_D61	TP_CPU_DC_TEST_D61 - @mlb_lib.MLB	10C1
TP_CPU_VCC_DIE_SENSE	TP_CPU_VCC_DIE_SENSE - @mlb_lib.MLB	10C4
TP_CPU_VDDQ_SENSEN	TP_CPU_VDDQ_SENSEN - @mlb_lib.MLB	13C1
TP_CPU_VDDQ_SENSEP	TP_CPU_VDDQ_SENSEP - @mlb_lib.MLB	13C1
TP_DPAPWRSW_FLT_L	TP_DPAPWRSW_FLT_L - @mlb_lib.MLB	78D1
TP_FWOHCI_XO	TP_FWOHCI_XO - @mlb_lib.MLB	39C2
TP_FWPHY_CNA	TP_FWPHY_CNA - @mlb_lib.MLB	39B2
TP_FWXIO_GRST_L	TP_FWXIO_GRST_L - @mlb_lib.MLB	39B6
TP_FWXIO_JTAG_TDI	TP_FWXIO_JTAG_TDI - @mlb_lib.MLB	39B6
TP_FWXIO_JTAG_TDO	TP_FWXIO_JTAG_TDO - @mlb_lib.MLB	39B6
TP_FWXIO_JTAG_TMS	TP_FWXIO_JTAG_TMS - @mlb_lib.MLB	39B6
TP_HDMI_CEC_CONN	TP_HDMI_CEC_CONN - @mlb_lib.MLB	80C4
TP_IRUC_RCVR_PWR_EN_L	TP_IRUC_RCVR_PWR_EN_L - @mlb_lib.MLB	44C6
TP_LPC_CLK33M_GMUX_R	TP_LPC_CLK33M_GMUX_R - @mlb_lib.MLB	19C6
TP_PCH_TP23	TP_PCH_TP23 - @mlb_lib.MLB	18C5
TP_PCI_CLK33M_OUT3	TP_PCI_CLK33M_OUT3 - @mlb_lib.MLB	19C6
TP_PM_SLP_A_L	TP_PM_SLP_A_L - @mlb_lib.MLB	18C5
TP_PM_SLP_SUS_L	TP_PM_SLP_SUS_L - @mlb_lib.MLB	18B5
TP_PPVOUT_PCH_DCPSUSBYP	TP_PPVOUT_PCH_DCPSUSBYP - @mlb_lib.MLB	21D8
TP_SPI_CS1_L	TP_SPI_CS1_L - @mlb_lib.MLB	17C8
TP_T29_MONDC0	TP_T29_MONDC0 - @mlb_lib.MLB	74D6
TP_T29_MONDC1	TP_T29_MONDC1 - @mlb_lib.MLB	74D6
TP_T29_MONOBSN	TP_T29_MONOBSN - @mlb_lib.MLB	74C6
TP_T29_MONOBSP	TP_T29_MONOBSP - @mlb_lib.MLB	74D6
TP_T29_TEST_POINT_0	TP_T29_TEST_POINT_0 - @mlb_lib.MLB	74C5
TP_T29_TEST_POINT_1	TP_T29_TEST_POINT_1 - @mlb_lib.MLB	74C5
TP_T29_TEST_POINT_2	TP_T29_TEST_POINT_2 - @mlb_lib.MLB	74C5
TP_T29_THERMDP	TP_T29_THERMDP - @mlb_lib.MLB	74C5
TP_T29_XTAL25OUT	TP_T29_XTAL25OUT - @mlb_lib.MLB	74C3
TP_USB_HUB1_OCS1	TP_USB_HUB1_OCS1 - @mlb_lib.MLB	25C4
TP_USB_HUB1_OCS4	TP_USB_HUB1_OCS4 - @mlb_lib.MLB	25C4
TP_USB_HUB1_PRTPWR1	TP_USB_HUB1_PRTPWR1 - @mlb_lib.MLB	25C4
TP_USB_HUB1_PRTPWR2	TP_USB_HUB1_PRTPWR2 - @mlb_lib.MLB	25C4
TP_USB_HUB1_PRTPWR3	TP_USB_HUB1_PRTPWR3 - @mlb_lib.MLB	25C4
TP_USB_HUB1_PRTPWR4	TP_USB_HUB1_PRTPWR4 - @mlb_lib.MLB	25C4
TP_USB_HUB2_OCS1	TP_USB_HUB2_OCS1 - @mlb_lib.MLB	25A4
TP_USB_HUB2_OCS4	TP_USB_HUB2_OCS4 - @mlb_lib.MLB	25A4
TP_USB_HUB2_PRTPWR1	TP_USB_HUB2_PRTPWR1 - @mlb_lib.MLB	25A4
TP_USB_HUB2_PRTPWR2	TP_USB_HUB2_PRTPWR2 - @mlb_lib.MLB	25A4
TP_USB_HUB2_PRTPWR3	TP_USB_HUB2_PRTPWR3 - @mlb_lib.MLB	25A4
TP_USB_HUB2_PRTPWR4	TP_USB_HUB2_PRTPWR4 - @mlb_lib.MLB	25A4

U4600_ILIM	U4600_ILIM - @mlb_lib.MLB	43C7
U4601_ILIM	U4601_ILIM - @mlb_lib.MLB	43D7
US900_GAIN	US900_GAIN - @mlb_lib.MLB	56B4
USB_BT_CONN_N	USB_BT_CONN_N - @mlb_lib.MLB	35C6 83B3 91D7
USB_BT_CONN_P	USB_BT_CONN_P - @mlb_lib.MLB	35C6 83B3 91D7
USB_BT_N	USB_BT_N - @mlb_lib.MLB	25B4 35C4 83B3
USB_BT_P	USB_BT_P - @mlb_lib.MLB	25B4 35C4 83B3
USB_B_MUXED_N	USB_B_MUXED_N - @mlb_lib.MLB	43D3 83B3
USB_B_MUXED_P	USB_B_MUXED_P - @mlb_lib.MLB	43D3 83B3
USB_DEBUGPRT_EN_L	USB_DEBUGPRT_EN_L - @mlb_lib.MLB	43C3 46B8
USB_EXTA_N	USB_EXTA_N - @mlb_lib.MLB	25A4 43A6 83C3
USB_EXTA_OC_L	USB_EXTA_OC_L - @mlb_lib.MLB	25A4 43C8
USB_EXTA_P	USB_EXTA_P - @mlb_lib.MLB	25A4 43A6 83C3
USB_EXTB_N	USB_EXTB_N - @mlb_lib.MLB	25C4 43D5 83B3
USB_EXTB_OC_L	USB_EXTB_OC_L - @mlb_lib.MLB	25C4 43D8
USB_EXTB_P	USB_EXTB_P - @mlb_lib.MLB	25C4 43D5 83B3
USB_EXTC_N	USB_EXTC_N - @mlb_lib.MLB	25C4 43C3 83B3
USB_EXTC_OC_L	USB_EXTC_OC_L - @mlb_lib.MLB	25C4 43D8
USB_EXTC_P	USB_EXTC_P - @mlb_lib.MLB	25C4 43B3 83B3
USB_EXTD_N	USB_EXTD_N - @mlb_lib.MLB	25B4 43B6 83B3
USB_EXTD_OC_L	USB_EXTD_OC_L - @mlb_lib.MLB	25A4 43B8
USB_EXTD_P	USB_EXTD_P - @mlb_lib.MLB	25A4 43B6 83B3
USB_HUB1_CFG_SEL0	USB_HUB1_CFG_SEL0 - @mlb_lib.MLB	25C6
USB_HUB1_CFG_SEL1	USB_HUB1_CFG_SEL1 - @mlb_lib.MLB	25C6
USB_HUB1_NONREM0	USB_HUB1_NONREM0 - @mlb_lib.MLB	25C6
USB_HUB1_NONREM1	USB_HUB1_NONREM1 - @mlb_lib.MLB	25C6
USB_HUB1_RBIAS	USB_HUB1_RBIAS - @mlb_lib.MLB	25C5
USB_HUB1_TEST	USB_HUB1_TEST - @mlb_lib.MLB	25C6
USB_HUB1_UP_N	USB_HUB1_UP_N - @mlb_lib.MLB	19D3 25C4 83C3
USB_HUB1_UP_P	USB_HUB1_UP_P - @mlb_lib.MLB	19D3 25C4 83C3
USB_HUB1_VBUS_DET	USB_HUB1_VBUS_DET - @mlb_lib.MLB	25C5
USB_HUB1_XTAL1	USB_HUB1_XTAL1 - @mlb_lib.MLB	25C6
USB_HUB1_XTAL2	USB_HUB1_XTAL2 - @mlb_lib.MLB	25C6
USB_HUB2_CFG_SEL0	USB_HUB2_CFG_SEL0 - @mlb_lib.MLB	25A6
USB_HUB2_CFG_SEL1	USB_HUB2_CFG_SEL1 - @mlb_lib.MLB	25A6
USB_HUB2_NONREM0	USB_HUB2_NONREM0 - @mlb_lib.MLB	25A6
USB_HUB2_NONREM1	USB_HUB2_NONREM1 - @mlb_lib.MLB	25A6
USB_HUB2_RBIAS	USB_HUB2_RBIAS - @mlb_lib.MLB	25A5
USB_HUB2_TEST	USB_HUB2_TEST - @mlb_lib.MLB	25B6
USB_HUB2_UP_N	USB_HUB2_UP_N - @mlb_lib.MLB	19D3 25A4 83C3
USB_HUB2_UP_P	USB_HUB2_UP_P - @mlb_lib.MLB	19C3 25A4 83C3
USB_HUB2_VBUS_DET	USB_HUB2_VBUS_DET - @mlb_lib.MLB	25A5
USB_HUB2_XTAL1	USB_HUB2_XTAL1 - @mlb_lib.MLB	25B6
USB_HUB2_XTAL2	USB_HUB2_XTAL2 - @mlb_lib.MLB	25A6
USB_HUB_RESET	USB_HUB_RESET - @mlb_lib.MLB	25B2
USB_HUB_RESET_L	USB_HUB_RESET_L - @mlb_lib.MLB	25B1 25B6 25C6
USB_HUB_SOFT_RESET_L	USB_HUB_SOFT_RESET_L - @mlb_lib.MLB	19C1 24D4 25B2
USB_IR_N	USB_IR_N - @mlb_lib.MLB	25C4 44C3 83B3
USB_IR_P	USB_IR_P - @mlb_lib.MLB	25C4 44C3 83B3
USB_IR_R_N	USB_IR_R_N - @mlb_lib.MLB	44C4 83B3
USB_IR_R_P	USB_IR_R_P - @mlb_lib.MLB	44C4 83B3
USB_PORT0_N	USB_PORT0_N - @mlb_lib.MLB	43A4 83B3
USB_PORT0_P	USB_PORT0_P - @mlb_lib.MLB	43A4 83B3
USB_PORT1_N	USB_PORT1_N - @mlb_lib.MLB	43B5 83B3
USB_PORT1_P	USB_PORT1_P - @mlb_lib.MLB	43B5 83B3
USB_PORT2_N	USB_PORT2_N - @mlb_lib.MLB	43C2 83B3
USB_PORT2_P	USB_PORT2_P - @mlb_lib.MLB	43B2 83B3
USB_PORT3_N	USB_PORT3_N - @mlb_lib.MLB	43D2 83B3
USB_PORT3_P	USB_PORT3_P - @mlb_lib.MLB	43D2 83B3
USB_PWR_EN	USB_PWR_EN - @mlb_lib.MLB	43C8 62D1
VBIAS_DAC	VBIAS_DAC - @mlb_lib.MLB	53D5
VCCSAS0_AGND	VCCSAS0_AGND - @mlb_lib.MLB	64B6
VCCSAS0_BOOT_RC	VCCSAS0_BOOT_RC - @mlb_lib.MLB	64C5
VCCSAS0_CS_N	VCCSAS0_CS_N - @mlb_lib.MLB	50A8 64B2 89D3
VCCSAS0_CS_P	VCCSAS0_CS_P - @mlb_lib.MLB	50A8 64B2 89D3
VCCSAS0_DRVH	VCCSAS0_DRVH - @mlb_lib.MLB	64C5
VCCSAS0_DRVL	VCCSAS0_DRVL - @mlb_lib.MLB	64C5
VCCSAS0_FB	VCCSAS0_FB - @mlb_lib.MLB	64C6
VCCSAS0_FSEL	VCCSAS0_FSEL - @mlb_lib.MLB	64B6
VCCSAS0_LL	VCCSAS0_LL - @mlb_lib.MLB	64C5
VCCSAS0_OCSET	VCCSAS0_OCSET - @mlb_lib.MLB	64C6
VCCSAS0_SET0	VCCSAS0_SET0 - @mlb_lib.MLB	64B6
VCCSAS0_SET1	VCCSAS0_SET1 - @mlb_lib.MLB	64B6
VCCSAS0_SNUB	VCCSAS0_SNUB - @mlb_lib.MLB	64C3
VCCSAS0_SREF	VCCSAS0_SREF - @mlb_lib.MLB	64C6
VCCSAS0_VBST	VCCSAS0_VBST - @mlb_lib.MLB	64C5
VCCSAS0_VO	VCCSAS0_VO - @mlb_lib.MLB	64C6
VCCSAVSENSE_IN	VCCSAVSENSE_IN - @mlb_lib.MLB	50A7
VCCSA_IOUT	VCCSA_IOUT - @mlb_lib.MLB	50A7
VDDQ_IOUT	VDDQ_IOUT - @mlb_lib.MLB	50D6
VDD_1V550	VDD_1V550 - @mlb_lib.MLB	71B7
VMON_3V3_DIV	VMON_3V3_DIV - @mlb_lib.MLB	62C8
VMON_Q2_BASE	VMON_Q2_BASE - @mlb_lib.MLB	62C7
VMON_Q3_BASE	VMON_Q3_BASE - @mlb_lib.MLB	62C7
VMON_Q4_BASE	VMON_Q4_BASE - @mlb_lib.MLB	62B7
VR3V3_G3H_BST	VR3V3_G3H_BST - @mlb_lib.MLB	65D5
VR3V3_G3H_EN	VR3V3_G3H_EN - @mlb_lib.MLB	65D6
VR3V3_G3H_ENL	VR3V3_G3H_ENL - @mlb_lib.MLB	65C5
VR3V3_G3H_FB	VR3V3_G3H_FB - @mlb_lib.MLB	65C6
VR3V3_G3H_ILIM	VR3V3_G3H_ILIM - @mlb_lib.MLB	65C5
VR3V3_G3H_LXS	VR3V3_G3H_LXS - @mlb_lib.MLB	65C4
VR3V3_G3H_SW	VR3V3_G3H_SW - @mlb_lib.MLB	65C5
VR3V3_G3H_TON	VR3V3_G3H_TON - @mlb_lib.MLB	65C6
VR3V3_G3H_VSV	VR3V3_G3H_VSV - @mlb_lib.MLB	65D6
VR3V3_G3H_VSEN	VR3V3_G3H_VSEN - @mlb_lib.MLB	65C5
VR5V_G3H_SW	VR5V_G3H_SW - @mlb_lib.MLB	65B5
VR5V_G3H_VCC	VR5V_G3H_VCC - @mlb_lib.MLB	65B5
VR5V_S4_BOOT	VR5V_S4_BOOT - @mlb_lib.MLB	65B5
VR5V_S4_COMP	VR5V_S4_COMP - @mlb_lib.MLB	65A5
VR5V_S4_COMP_RC	VR5V_S4_COMP_RC - @mlb_lib.MLB	65A5
VR5V_S4_EN_IC	VR5V_S4_EN_IC - @mlb_lib.MLB	65B6
VR5V_S4_FB	VR5V_S4_FB - @mlb_lib.MLB	65A5
VR5V_S4_FB_RC	VR5V_S4_FB_RC - @mlb_lib.MLB	65A4
VR5V_S4_FB_SNS	VR5V_S4_FB_SNS - @mlb_lib.MLB	65A3
VR5V_S4_OCSET	VR5V_S4_OCSET - @mlb_lib.MLB	65A5
VR5V_S4_RT	VR5V_S4_RT - @mlb_lib.MLB	65A6
VR5V_S4_SS	VR5V_S4_SS - @mlb_lib.MLB	65A6
VREFMRGN_CA_SODIMMA_ BUF	VREFMRGN_CA_SODIMMA_BUF - @mlb_lib.MLB	33C3
VREFMRGN_CA_SODIMMA_ EN	VREFMRGN_CA_SODIMMA_EN - @mlb_lib.MLB	33C5
VREFMRGN_CA_SODIMMB_ BUF	VREFMRGN_CA_SODIMMB_BUF - @mlb_lib.MLB	33B3
VREFMRGN_CA_SODIMMB_ EN	VREFMRGN_CA_SODIMMB_EN - @mlb_lib.MLB	33C5
VREFMRGN_DQ_SODIMMA_ BUF	VREFMRGN_DQ_SODIMMA_BUF - @mlb_lib.MLB	33D3
VREFMRGN_DQ_SODIMMA_ EN	VREFMRGN_DQ_SODIMMA_EN - @mlb_lib.MLB	33C5
VREFMRGN_DQ_SODIMMB_ BUF	VREFMRGN_DQ_SODIMMB_BUF - @mlb_lib.MLB	33C3
VREFMRGN_DQ_SODIMMB_ EN	VREFMRGN_DQ_SODIMMB_EN - @mlb_lib.MLB	33C5
VREFMRGN_FRAMEBUF_BU	VREFMRGN_FRAMEBUF_BUF -	33B4

F	@mlb_lib.MLB	
VREFMRGN_FRAMEBUF_EN	VREFMRGN_FRAMEBUF_EN - @mlb_lib.MLB	33C5
VREFMRGN_MEMVREG_BUF	VREFMRGN_MEMVREG_BUF - @mlb_lib.MLB	33B3
VREFMRGN_MEMVREG_EN	VREFMRGN_MEMVREG_EN - @mlb_lib.MLB	33C5
VREFMRGN_MEMVREG_FBV	VREFMRGN_MEMVREG_FBVREF -	33D5
REF	@mlb_lib.MLB	
VREFMRGN_SODIMMA_DQ	VREFMRGN_SODIMMA_DQ - @mlb_lib.MLB	33D5
VREFMRGN_SODIMMB_DQ	VREFMRGN_SODIMMB_DQ - @mlb_lib.MLB	33D5
VREFMRGN_SODIMMS_CA	VREFMRGN_SODIMMS_CA - @mlb_lib.MLB	33D5
VRT29_VIN	VRT29_VIN - @mlb_lib.MLB	78D8
VR_AXG_BOOT1_RC	VR_AXG_BOOT1_RC - @mlb_lib.MLB	69C6
VR_AXG_COMP	VR_AXG_COMP - @mlb_lib.MLB	67C5
VR_AXG_COMP_RC	VR_AXG_COMP_RC - @mlb_lib.MLB	67C7
VR_AXG_DRV1_BOOT	VR_AXG_DRV1_BOOT - @mlb_lib.MLB	69C7
VR_AXG_DRV1_LGATE	VR_AXG_DRV1_LGATE - @mlb_lib.MLB	69C7
VR_AXG_DRV1_PVCC	VR_AXG_DRV1_PVCC - @mlb_lib.MLB	69C7
VR_AXG_DRV1_UGATE	VR_AXG_DRV1_UGATE - @mlb_lib.MLB	69C7
VR_AXG_FB	VR_AXG_FB - @mlb_lib.MLB	67C4
VR_AXG_HFREQ_COMP	VR_AXG_HFREQ_COMP - @mlb_lib.MLB	67C5
VR_AXG_IMON	VR_AXG_IMON - @mlb_lib.MLB	50B4 67B1
VR_AXG_ISNS_N	VR_AXG_ISNS_N - @mlb_lib.MLB	67C1 69B2
VR_AXG_ISNS_N_R	VR_AXG_ISNS_N_R - @mlb_lib.MLB	69C4
VR_AXG_ISNS_P	VR_AXG_ISNS_P - @mlb_lib.MLB	67C1 69C2
VR_AXG_ISNS_RP	VR_AXG_ISNS_RP - @mlb_lib.MLB	67C3
VR_AXG_PH1_SNUB	VR_AXG_PH1_SNUB - @mlb_lib.MLB	69C4
VR_AXG_PHASE1	VR_AXG_PHASE1 - @mlb_lib.MLB	69C7
VR_AXG_PWM	VR_AXG_PWM - @mlb_lib.MLB	67D1 69C8
VR_AXG_RGND	VR_AXG_RGND - @mlb_lib.MLB	67C5
VR_AXG_SW_FREQ	VR_AXG_SW_FREQ - @mlb_lib.MLB	67B3
VR_AXG_TCOMP	VR_AXG_TCOMP - @mlb_lib.MLB	67C4
VR_AXG_TM	VR_AXG_TM - @mlb_lib.MLB	67D4
VR_AXG_TMN	VR_AXG_TMN - @mlb_lib.MLB	67C5
VR_AXG_VSEN	VR_AXG_VSEN - @mlb_lib.MLB	67C5
VR_AXG_VSNS_R_N	VR_AXG_VSNS_R_N - @mlb_lib.MLB	67D7
VR_AXG_VSNS_R_P	VR_AXG_VSNS_R_P - @mlb_lib.MLB	67D7
VR_AXG_VSNS_XW_N	VR_AXG_VSNS_XW_N - @mlb_lib.MLB	67D7
VR_AXG_VSNS_XW_P	VR_AXG_VSNS_XW_P - @mlb_lib.MLB	67D8
VR_CPU_BOOT1_RC	VR_CPU_BOOT1_RC - @mlb_lib.MLB	68D6
VR_CPU_BOOT2_RC	VR_CPU_BOOT2_RC - @mlb_lib.MLB	68C6
VR_CPU_COMP	VR_CPU_COMP - @mlb_lib.MLB	67B5
VR_CPU_DRV1_BOOT	VR_CPU_DRV1_BOOT - @mlb_lib.MLB	68D7
VR_CPU_DRV1_LGATE	VR_CPU_DRV1_LGATE - @mlb_lib.MLB	68D7
VR_CPU_DRV1_PVCC	VR_CPU_DRV1_PVCC - @mlb_lib.MLB	68D7
VR_CPU_DRV1_UGATE	VR_CPU_DRV1_UGATE - @mlb_lib.MLB	68D7
VR_CPU_DRV2_BOOT	VR_CPU_DRV2_BOOT - @mlb_lib.MLB	68C7
VR_CPU_DRV2_LGATE	VR_CPU_DRV2_LGATE - @mlb_lib.MLB	68B7
VR_CPU_DRV2_UGATE	VR_CPU_DRV2_UGATE - @mlb_lib.MLB	68C7
VR_CPU_DRV2_VCC	VR_CPU_DRV2_VCC - @mlb_lib.MLB	68C7
VR_CPU_FB	VR_CPU_FB - @mlb_lib.MLB	67B5
VR_CPU_FB2	VR_CPU_FB2 - @mlb_lib.MLB	67B8
VR_CPU_FB_RC	VR_CPU_FB_RC - @mlb_lib.MLB	67C8
VR_CPU_FDVID	VR_CPU_FDVID - @mlb_lib.MLB	67C5
VR_CPU_HFREQ_COMP	VR_CPU_HFREQ_COMP - @mlb_lib.MLB	67B5
VR_CPU_IAUTO	VR_CPU_IAUTO - @mlb_lib.MLB	67B5
VR_CPU_IMON	VR_CPU_IMON - @mlb_lib.MLB	50D4 67B5
VR_CPU_ISNS1_N	VR_CPU_ISNS1_N - @mlb_lib.MLB	67C1 68C2
VR_CPU_ISNS1_N_R	VR_CPU_ISNS1_N_R - @mlb_lib.MLB	68D3
VR_CPU_ISNS1_P	VR_CPU_ISNS1_P - @mlb_lib.MLB	67C1 68D2
VR_CPU_ISNS2_N	VR_CPU_ISNS2_N - @mlb_lib.MLB	67C1 68B2
VR_CPU_ISNS2_N_R	VR_CPU_ISNS2_N_R - @mlb_lib.MLB	68C3
VR_CPU_ISNS2_P	VR_CPU_ISNS2_P - @mlb_lib.MLB	67C1 68C2
VR_CPU_N_PSI	VR_CPU_N_PSI - @mlb_lib.MLB	67C5
VR_CPU_PH1_SNUB	VR_CPU_PH1_SNUB - @mlb_lib.MLB	68D4
VR_CPU_PH2_SNUB	VR_CPU_PH2_SNUB - @mlb_lib.MLB	68C4
VR_CPU_PHASE1	VR_CPU_PHASE1 - @mlb_lib.MLB	68D7
VR_CPU_PHASE2	VR_CPU_PHASE2 - @mlb_lib.MLB	68C7
VR_CPU_PSICOMP	VR_CPU_PSICOMP - @mlb_lib.MLB	67B5
VR_CPU_PSICOMP1	VR_CPU_PSICOMP1 - @mlb_lib.MLB	67C8
VR_CPU_PWM1	VR_CPU_PWM1 - @mlb_lib.MLB	67C1 68D8
VR_CPU_PWM2	VR_CPU_PWM2 - @mlb_lib.MLB	67C1 68C8
VR_CPU_PWM3	VR_CPU_PWM3 - @mlb_lib.MLB	67C3
VR_CPU_PWM4	VR_CPU_PWM4 - @mlb_lib.MLB	67C3
VR_CPU_RAMP_ADJ	VR_CPU_RAMP_ADJ - @mlb_lib.MLB	67B3
VR_CPU_RGND	VR_CPU_RGND - @mlb_lib.MLB	67A7
VR_CPU_SUTH	VR_CPU_SUTH - @mlb_lib.MLB	67C5
VR_CPU_SW_FREQ	VR_CPU_SW_FREQ - @mlb_lib.MLB	67B3
VR_CPU_TM	VR_CPU_TM - @mlb_lib.MLB	67B5
VR_CPU_TMN	VR_CPU_TMN - @mlb_lib.MLB	67A7
VR_CPU_VSEN	VR_CPU_VSEN - @mlb_lib.MLB	67A6
VR_CPU_VSNS_R_N	VR_CPU_VSNS_R_N - @mlb_lib.MLB	67A7
VR_CPU_VSNS_R_P	VR_CPU_VSNS_R_P - @mlb_lib.MLB	67A7
VR_CPU_VSNS_XW_N	VR_CPU_VSNS_XW_N - @mlb_lib.MLB	67A8
VR_CPU_VSNS_XW_P	VR_CPU_VSNS_XW_P - @mlb_lib.MLB	67A8
VR_EN_PWR_OVP	VR_EN_PWR_OVP - @mlb_lib.MLB	67B3
VR_HOT_L	VR_HOT_L - @mlb_lib.MLB	67B5
VR_RSET	VR_RSET - @mlb_lib.MLB	67B4
VR_SEN_R2	VR_SEN_R2 - @mlb_lib.MLB	67D7
VTTCLAMP_EN	VTTCLAMP_EN - @mlb_lib.MLB	28B3
VTTCLAMP_L	VTTCLAMP_L - @mlb_lib.MLB	28B2
WIFI_EVENT_L	WIFI_EVENT_L - @mlb_lib.MLB	46B8 47A2
WIFI_PROX_THRM_N	WIFI_PROX_THRM_N - @mlb_lib.MLB	52C3 52D8
WIFI_PROX_THRM_P	WIFI_PROX_THRM_P - @mlb_lib.MLB	52C3 52D8
WLAN_THROTTLE_L	WLAN_THROTTLE_L - @mlb_lib.MLB	35D7 91D7
WOL_EN	WOL_EN - @mlb_lib.MLB	20B8 26C6 62A4
XDP_BPM_L<0>	XDP_BPM_L<0> - @mlb_lib.MLB	11B2 24D7
XDP_BPM_L<3..0>	XDP_BPM_L<3..0> - @mlb_lib.MLB	81D1
XDP_BPM_L<1>	XDP_BPM_L<1> - @mlb_lib.MLB	11B2 24D7
XDP_BPM_L<2>	XDP_BPM_L<2> - @mlb_lib.MLB	11B2 24D7
XDP_BPM_L<3>	XDP_BPM_L<3> - @mlb_lib.MLB	11B2 24D7
XDP_BPM_L<4>	XDP_BPM_L<4> - @mlb_lib.MLB	11B2 24C7
XDP_BPM_L<7..4>	XDP_BPM_L<7..4> - @mlb_lib.MLB	81D1
XDP_BPM_L<5>	XDP_BPM_L<5> - @mlb_lib.MLB	11B2 24C7
XDP_BPM_L<6>	XDP_BPM_L<6> - @mlb_lib.MLB	11B2 24C7
XDP_BPM_L<7>	XDP_BPM_L<7> - @mlb_lib.MLB	11B2 24C7
XDP_CPURST_L	XDP_CPURST_L - @mlb_lib.MLB	24C5 81D1
XDP_CPU_CFG<0>	XDP_CPU_CFG<0> - @mlb_lib.MLB	24C7 81D1
XDP_CPU_CLK100M_N	XDP_CPU_CLK100M_N - @mlb_lib.MLB	24C5 81C1
XDP_CPU_CLK100M_P	XDP_CPU_CLK100M_P - @mlb_lib.MLB	24C5 81C1
XDP_CPU_PRDY_L	XDP_CPU_PRDY_L - @mlb_lib.MLB	11C2 24D7 81D1
XDP_CPU_PREQ_L	XDP_CPU_PREQ_L - @mlb_lib.MLB	11C2 24D7 81D1
XDP_CPU_PWRBTN_L	XDP_CPU_PWRBTN_L - @mlb_lib.MLB	24C7 81C1
XDP_CPU_PWRGD	XDP_CPU_PWRGD - @mlb_lib.MLB	24C7 81C1
XDP_CPU_TCK	XDP_CPU_TCK - @mlb_lib.MLB	11C2 24A8 24C7 24D2 81D1
XDP_CPU_TDI	XDP_CPU_TDI - @mlb_lib.MLB	11C2 24B6 24D2 81D1
XDP_CPU_TDO	XDP_CPU_TDO - @mlb_lib.MLB	11C2 24A6 24D2 81D1
XDP_CPU_TMS	XDP_CPU_TMS - @mlb_lib.MLB	11C2 24A6 24D2 81D1
XDP_CPU_TRST_L	XDP_CPU_TRST_L - @mlb_lib.MLB	11C2 24C4 24D2 81D1
XDP_DBRESET_L	XDP_DBRESET_L - @mlb_lib.MLB	11C2 24C4 27A4 81C1
XDP_PCH_TCK	XDP_PCH_TCK - @mlb_lib.MLB	17C8 24A4 24A8 24C7 81D1
XDP_PCH_TDI	XDP_PCH_TDI - @mlb_lib.MLB	17C8 24A4 24B6 81D1
XDP_PCH_TDO	XDP_PCH_TDO - @mlb_lib.MLB	17C8 24A4 24B6 81D1
XDP_PCH_TMS	XDP_PCH_TMS - @mlb_lib.MLB	17C8 24A4 24B6 81D1
XDP_PRESENT_L	XDP_PRESENT_L - @mlb_lib.MLB	24B2 24C4 81C1
XDP_RES_RL	XDP_RES_RL - @mlb_lib.MLB	24C2 81C1

XDP_SEL	XDP_SEL - @mlb_lib.MLB	24A8 24B1 24B8
XDP_TDI	XDP_TDI - @mlb_lib.MLB	24B8 24C4 81D1
XDP_TDO	XDP_TDO - @mlb_lib.MLB	24A8 24C4 81D1
XDP_TMS	XDP_TMS - @mlb_lib.MLB	24A4 24C4 81D1
XDP_VR_READY	XDP_VR_READY - @mlb_lib.MLB	24C7 81C1

Title: Cref Part Report
Design: mlb
Date: Apr 7 18:57:22 2011

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C161E	CAP_603	mlb[15A7]
C161F	CAP_0402-1	mlb[15A7]
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C162B	CAP_0402-1	mlb[15A6]
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C2850	CAP_402	mlb[27A7]
C2860	CAP_402	mlb[27A6]
C2880	CAP_402	mlb[27B3]
C2916	CAP_402	mlb[28B5]
C2920	CAP_402	mlb[28C3]
C2951	CAP_402	mlb[28B3]
C3100	CAP_603	mlb[30D3]
C3101	CAP_603	mlb[30D3]
C3110	CAP_402	mlb[30D3]
C3111	CAP_402	mlb[30D3]
C3112	CAP_402	mlb[30D2]
C3113	CAP_402	mlb[30D2]
C3114	CAP_402	mlb[30D2]
C3115	CAP_402	mlb[30D1]
C3116	CAP_402	mlb[30D1]
C3117	CAP_402	mlb[30D1]
C3130	CAP_402-LF	mlb[30D1]
C3131	CAP_402	mlb[30D1]
C3132	CAP_402	mlb[30D1]
C3135	CAP_402-LF	mlb[30C1]
C3136	CAP_402	mlb[30C1]
C3137	CAP_402	mlb[30C1]
C3140	CAP_402-LF	mlb[30B2]
C3150	CAP_402-LF	mlb[30C1]
C3151	CAP_402-LF	mlb[30C1]
C3152	CAP_402	mlb[30C1]
C3200	CAP_603	mlb[31D3]
C3201	CAP_603	mlb[31D3]
C3210	CAP_402	mlb[31D3]
C3211	CAP_402	mlb[31D3]
C3212	CAP_402	mlb[31D2]
C3213	CAP_402	mlb[31D2]
C3214	CAP_402	mlb[31D2]
C3215	CAP_402	mlb[31D1]
C3216	CAP_402	mlb[31D1]
C3217	CAP_402	mlb[31D1]
C3222	CAP_402	mlb[31A4]
C3224	CAP_402	mlb[31A4]
C3226	CAP_402	mlb[31A3]
C3228	CAP_402	mlb[31A2]
C3230	CAP_402-LF	mlb[31D1]
C3231	CAP_402	mlb[31D1]
C3232	CAP_402	mlb[31D1]
C3235	CAP_402-LF	mlb[31C1]
C3236	CAP_402	mlb[31C1]
C3237	CAP_402	mlb[31C1]
C3240	CAP_402-LF	mlb[31B2]
C3250	CAP_402-LF	mlb[31C1]
C3251	CAP_402-LF	mlb[31C1]
C3252	CAP_402	mlb[31C1]
C3331	CAP_402	mlb[32B5]
C3332	CAP_402	mlb[32B4]
C3333	CAP_402	mlb[32B4]
C3334	CAP_402	mlb[32B4]
C3336	CAP_402	mlb[32B3]
C3338	CAP_402	mlb[32A5]
C3339	CAP_402	mlb[32A5]
C3340	CAP_402	mlb[32A4]
C3341	CAP_402	mlb[32A4]
C3342	CAP_402	mlb[32A4]
C3400	CAP_402-LF	mlb[33D6]
C3401	CAP_402	mlb[33D6]
C3402	CAP_402	mlb[33C6]
C3403	CAP_402	mlb[33D4]
C3404	CAP_402	mlb[33C4]
C3405	CAP_402	mlb[33B4]
C3500	CAP_402	mlb[34D4]
C3501	CAP_603	mlb[34D4]
C3505	CAP_402	mlb[34D2]
C3507	CAP_603	mlb[34D3]
C3511	CAP_402	mlb[34D8]
C3512	CAP_402	mlb[34D8]
C3513	CAP_402	mlb[34D8]
C3514	CAP_402	mlb[34D8]
C3515	CAP_402	mlb[34C8]
C3516	CAP_402	mlb[34C8]
C3517	CAP_402	mlb[34C8]
C3518	CAP_402	mlb[34C8]
C3519	CAP_402	mlb[34C8]
C3520	CAP_402	mlb[34C8]
C3521	CAP_402	mlb[34C8]
C3530	CAP_402-1	mlb[34B4]
C3535	CAP_402-1	mlb[34B4]
C3541	CAP_402	mlb[34C6]
C3542	CAP_402	mlb[34C7]
C3550	CAP_402	mlb[34C3]
C3551	CAP_402	mlb[34C4]
C3620	CAP_0805	mlb[35B5]
C3621	CAP_402	mlb[35B5]
C3622	CAP_402	mlb[35B7]
C3623	CAP_402	mlb[35B6]
C3624	CAP_402-1	mlb[35B6]
C3630	CAP_402	mlb[35C5]
C3631	CAP_402	mlb[35C5]
C3632	CAP_402	mlb[35C6]
C3633	CAP_402-1	mlb[35C6]
C3640	CAP_402	mlb[35B3]
C3650	CAP_402	mlb[35C3]
C3651	CAP_402	mlb[35C2]
C3800	CAP_402	mlb[36D5]
C3801	CAP_402	mlb[36D4]
C3802	CAP_402	mlb[36D4]
C3803	CAP_402	mlb[36D4]
C3810	CAP_1206	mlb[36B3]
C3900	CAP_402	mlb[37D6]
C3905	CAP_402	mlb[37D6]
C3910	CAP_402	mlb[37C6]
C3911	CAP_402	mlb[37C5]
C3915	CAP_603	mlb[37C5]
C3916	CAP_402	mlb[37C5]
C3920	CAP_603	mlb[37D3]
C3921	CAP_402	mlb[37D4]
C3925	CAP_603	mlb[37D3]
C3926	CAP_402	mlb[37D4]
C3930	CAP_603	mlb[37C3]
C3931	CAP_402	mlb[37C4]
C3935	CAP_0805	mlb[37C3]
C3936	CAP_402	mlb[37C3]
C3950	CAP_402	mlb[37C7]
C3951	CAP_402	mlb[37C7]
C3955	CAP_402	mlb[37C7]
C3956	CAP_402	mlb[37B7]
C3970	CAP_603	mlb[37C2]
C3971	CAP_402	mlb[37C2]
C3972	CAP_402	mlb[37C2]
C3990	CAP_402	mlb[37A7]
C4020	CAP_603	mlb[38D7]
C4021	CAP_402	mlb[38D7]
C4025	CAP_603	mlb[38C6]
C4026	CAP_402	mlb[38C6]
C4100	CAP_402-1	mlb[39D7]
C4101	CAP_402-1	mlb[39D7]
C4102	CAP_402-1	mlb[39D6]
C4103	CAP_402-1	mlb[39D6]
C4104	CAP_402-1	mlb[39D6]
C4105	CAP_402-1	mlb[39D6]
C4106	CAP_402-1	mlb[39D6]
C4107	CAP_402-1	mlb[39D6]
C4108	CAP_402-1	mlb[39D6]
C4110	CAP_402-1	mlb[39D7]
C4111	CAP_402-1	mlb[39D7]
C4112	CAP_402-1	mlb[39D6]
C4113	CAP_402-1	mlb[39D6]
C4114	CAP_402-1	mlb[39D6]
C4115	CAP_402-1	mlb[39D6]
C4117	CAP_402-1	mlb[39C6]
C4118	CAP_402-1	mlb[39C6]
C4119	CAP_402-1	mlb[39C6]
C4120	CAP_402-1	mlb[39D2]
C4121	CAP_402-1	mlb[39D3]
C4122	CAP_402-1	mlb[39D3]
C4123	CAP_402-1	mlb[39D3]
C4124	CAP_402-1	mlb[39D3]
C4125	CAP_402-1	mlb[39D2]
C4126	CAP_402-1	mlb[39D3]
C4127	CAP_402-1	mlb[39D3]
C4128	CAP_402-1	mlb[39D3]
C4130	CAP_402-1	mlb[39D2]
C4131	CAP_402-1	mlb[39D2]
C4132	CAP_402-1	mlb[39D2]
C4135	CAP_402-1	mlb[39C2]
C4137	CAP_402-1	mlb[39C3]
C4138	CAP_402-1	mlb[39C3]
C4139	CAP_402-1	mlb[39C2]
C4140	CAP_402	mlb[39C7]
C4141	CAP_402	mlb[39C7]
C4145	CAP_402	mlb[39C7]
C4146	CAP_402	mlb[39C7]
C4189	CAP_402	mlb[39A2]
C4190	CAP_402	mlb[39C1]
C4200	CAP_402-1	mlb[40D7]
C4201	CAP_402	mlb[40D6]
C4202	CAP_402-LF	mlb[40D6]
C4250	CAP_402-1	mlb[40D3]
C4254	CAP_402	mlb[40B3]
C4300	CAP_603	mlb[41D2]
C4305	CAP_603	mlb[41B6]
C4309	CAP_402	mlb[41C7]
C4310	CAP_402	mlb[41C4]
C4311	CAP_402	mlb[41C3]
C4312	CAP_402	mlb[41B4]
C4313	CAP_402	mlb[41B3]
C4332	CAP_402	mlb[41B1]
C4335	CAP_603-1	mlb[41B2]
C4350	CAP_402	mlb[41A4]
C4351	CAP_402	mlb[41A5]
C4355	CAP_603	mlb[41A3]
C4400	CAP_0201	mlb[42C6]
C4401	CAP_0201	mlb[42B6]
C4402	CAP_0201	mlb[42B6]
C4403	CAP_0201	mlb[42A6]
C4420	CAP_0201	mlb[42C2]
C4421	CAP_0201	mlb[42B2]
C4422	CAP_0201	mlb[42B2]
C4423	CAP_0201	mlb[42A2]
C4431	CAP_402	mlb[42D6]
C4441	CAP_402	mlb[42D3]
C4450	CAP_0201	mlb[42C6]

C4451	CAP_0201	mlb[42B6]
C4452	CAP_0201	mlb[42B6]
C4453	CAP_0201	mlb[42B6]
C4460	CAP_0201	mlb[42C3]
C4461	CAP_0201	mlb[42B3]
C4462	CAP_0201	mlb[42B3]
C4463	CAP_0201	mlb[42B3]
C4600	CAP_P_CASE-B2-SM	mlb[43B7]
C4601	CAP_402	mlb[43B8]
C4603	CAP_402	mlb[43D6]
C4604	CAP_402	mlb[43D8]
C4605	CAP_402	mlb[43D2]
C4606	CAP_P_CASE-B2-SM	mlb[43D8]
C4612	CAP_402	mlb[43D6]
C4615	CAP_402	mlb[43C2]
C4623	CAP_402	mlb[43B6]
C4625	CAP_402	mlb[43B4]
C4632	CAP_402	mlb[43B6]
C4635	CAP_402	mlb[43A4]
C4650	CAP_402	mlb[43D5]
C4790	CAP_402-1	mlb[44C4]
C4791	CAP_402	mlb[44C4]
C4792	CAP_402	mlb[44C5]
C4793	CAP_402-1	mlb[44B4]
C4794	CAP_402	mlb[44B5]
C4800	CAP_402	mlb[45C3]
C4801	CAP_402	mlb[45D6]
C4802	CAP_402	mlb[45A3]
C4803	CAP_402	mlb[45C2]
C4806	CAP_402	mlb[45C6]
C4809	CAP_402	mlb[45C4]
C4902	CAP_805	mlb[46D4]
C4903	CAP_402	mlb[46D4]
C4904	CAP_402	mlb[46D3]
C4905	CAP_402	mlb[46D3]
C4906	CAP_402	mlb[46D3]
C4907	CAP_402	mlb[46D2]
C4910	CAP_402	mlb[46A5]
C4920	CAP_402	mlb[46D3]
C5001	CAP_402	mlb[47D8]
C5010	CAP_402	mlb[47B7]
C5011	CAP_402	mlb[47B7]
C5020	CAP_402	mlb[47D7]
C5025	CAP_603	mlb[47D7]
C5026	CAP_402	mlb[47D6]
C5300	CAP_402	mlb[50D6]
C5301	CAP_402	mlb[50D5]
C5305	CAP_402	mlb[50C6]
C5306	CAP_402	mlb[50C5]
C5320	CAP_402	mlb[50C2]
C5322	CAP_402	mlb[50A6]
C5330	CAP_402	mlb[50B2]
C5340	CAP_402	mlb[50D2]
C5341	CAP_402	mlb[50D2]
C5345	CAP_402	mlb[50D3]
C5351	CAP_402	mlb[50B2]
C5355	CAP_402	mlb[50B3]
C5360	CAP_402	mlb[50B7]
C5361	CAP_402	mlb[50B6]
C5365	CAP_402	mlb[50A7]
C5366	CAP_402	mlb[50A6]
C5375	CAP_402	mlb[50C7]
C5376	CAP_402	mlb[50B6]
C5401	CAP_402	mlb[51C6]
C5403	CAP_402	mlb[51C5]
C5414	CAP_402	mlb[51D2]
C5418	CAP_402	mlb[51D6]
C5437	CAP_402	mlb[51D5]
C5500	CAP_402-1	mlb[52D6]
C5510	CAP_402	mlb[52D3]
C5520	CAP_402	mlb[52D3]
C5535	CAP_402-1	mlb[52B5]
C5540	CAP_402	mlb[52A6]
C5570	CAP_402	mlb[52C3]
C5580	CAP_402	mlb[52C3]
C5600	CAP_0306	mlb[53D6]
C5602	CAP_P_2012-LLP	mlb[53D5]
C5603	CAP_402	mlb[53D4]
C5604	CAP_P_2012-LLP	mlb[53D4]
C5605	CAP_402	mlb[53D3]
C5606	CAP_402-1	mlb[53D3]
C5608	CAP_0508	mlb[53D3]
C5613	CAP_P_CASE-P3-HF	mlb[53B4]
C5614	CAP_P_CASE-B2-SM	mlb[53B4]
C5650	CAP_402	mlb[53A7]
C5651	CAP_402-1	mlb[53A6]
C5652	CAP_402	mlb[53A6]
C5653	CAP_402	mlb[53A4]
C5654	CAP_402-1	mlb[53A4]
C5700	CAP_P_CASE-M	mlb[54D4]
C5702	CAP_P_CASE-M	mlb[54C4]
C5703	CAP_P_CASE-M	mlb[54C4]
C5713	CAP_201	mlb[54C5]
C5800	CAP_0508	mlb[55D5]
C5801	CAP_402	mlb[55D5]
C5804	CAP_402-1	mlb[55B4]
C5805	CAP_402-1	mlb[55B3]
C5806	CAP_402-1	mlb[55B3]
C5812	CAP_P_CASE-P	mlb[55C7]
C5813	CAP_P_CASE-P	mlb[55C7]
C5814	CAP_P_CASE-P	mlb[55B7]
C5815	CAP_P_CASE-P	mlb[55B7]
C5901	CAP_P_1206-LLP	mlb[56C3]
C5902	CAP_402	mlb[56C3]
C5904	CAP_402-1	mlb[56C5]
C5950	CAP_402	mlb[56B6]
C5951	CAP_402	mlb[56C6]
C6000	CAP_402-1	mlb[57A8]
C6050	CAP_402-1	mlb[57A8]
C6051	CAP_402	mlb[57A7]
C6054	CAP_402	mlb[57A6]
C6100	CAP_402	mlb[58A3]
C6101	CAP_402	mlb[58B7]
C6102	CAP_402	mlb[58B7]
C6111	CAP_402	mlb[58A6]
C6160	CAP_402	mlb[58A3]
C6180	CAP_603	mlb[58D3]
C6181	CAP_402	mlb[58C2]
C6182	CAP_P_603-HF	mlb[58C2]
C6183	CAP_402	mlb[58C3]
C6184	CAP_402	mlb[58C3]
C6185	CAP_402	mlb[58C2]
C6186	CAP_402	mlb[58C3]
C6187	CAP_402	mlb[58D3]

C6400	CAP_402	mlb[59C5]
C6500	CAP_402	mlb[60C4]
C6502	CAP_402	mlb[60D5]
C6503	CAP_402	mlb[60C4]
C6505	CAP_603	mlb[60C4]
C6506	CAP_603	mlb[60C3]
C6507	CAP_402	mlb[60C3]
C6520	CAP_402	mlb[60C4]
C6700	CAP_402	mlb[61D2]
C6701	CAP_402	mlb[61B7]
C6702	CAP_603	mlb[61B7]
C6709	CAP_402	mlb[61D3]
C6710	CAP_402	mlb[61D6]
C6711	CAP_402	mlb[61D6]
C6730	CAP_402	mlb[61C2]
C6731	CAP_402	mlb[61C3]
C6740	CAP_402	mlb[61B2]
C6741	CAP_402	mlb[61C3]
C6760	CAP_402	mlb[61B2]
C6761	CAP_402	mlb[61B3]
C6810	CAP_402	mlb[62D2]
C6812	CAP_402	mlb[62D3]
C6821	CAP_402	mlb[62B2]
C6822	CAP_402	mlb[62B1]
C6842	CAP_402	mlb[62D7]
C6860	CAP_402	mlb[62A7]
C6881	CAP_402	mlb[62C3]
C6886	CAP_402	mlb[62C2]
C6887	CAP_402	mlb[62C3]
C6888	CAP_402	mlb[62C2]
C7101	CAP_603	mlb[64C5]
C7102	CAP_402	mlb[64B6]
C7103	CAP_402	mlb[64B6]
C7105	CAP_402	mlb[64B7]
C7119	CAP_402	mlb[64B3]
C7120	CAP_P_SM	mlb[64C3]
C7121	CAP_402	mlb[64C3]
C7122	CAP_402	mlb[64C3]
C7123	CAP_402	mlb[64B2]
C7130	CAP_402	mlb[64C4]
C7140	CAP_402	mlb[64B3]
C7201	CAP_402	mlb[65D5]
C7202	CAP_402	mlb[65D6]
C7203	CAP_402	mlb[65C5]
C7204	CAP_402	mlb[65D4]
C7205	CAP_P_CASED2-SM	mlb[65D4]
C7208	CAP_402	mlb[65C4]
C7209	CAP_805	mlb[65C3]
C7210	CAP_805	mlb[65C3]
C7211	CAP_402	mlb[65D6]
C7212	CAP_402	mlb[65C3]
C7213	CAP_402	mlb[65D5]
C7250	CAP_402	mlb[65B6]
C7251	CAP_P_SM	mlb[65B7]
C7252	CAP_603	mlb[65B7]
C7253	CAP_402	mlb[65B7]
C7254	CAP_402	mlb[65B5]
C7255	CAP_402	mlb[65A6]
C7256	CAP_402	mlb[65B4]
C7257	CAP_402	mlb[65A5]
C7258	CAP_402	mlb[65A5]
C7259	CAP_402	mlb[65A4]
C7260	CAP_402	mlb[65A3]
C7261	CAP_0805	mlb[65A3]
C7262	CAP_P_CASE-B2-SM	mlb[65A3]
C7300	CAP_603	mlb[66C7]
C7301	CAP_402	mlb[66D6]
C7302	CAP_603	mlb[66D5]
C7305	CAP_402	mlb[66B8]
C7320	CAP_402	mlb[66B7]
C7321	CAP_402	mlb[66B4]
C7325	CAP_402	mlb[66C4]
C7330	CAP_P_SM	mlb[66C5]
C7331	CAP_603	mlb[66C4]
C7332	CAP_P_SM	mlb[66C4]
C7333	CAP_402	mlb[66C4]
C7340	CAP_P_CASE-B2-SM	mlb[66C3]
C7341	CAP_P_CASE-B2-SM	mlb[66C2]
C7345	CAP_603	mlb[66C2]
C7350	CAP_402	mlb[66B6]
C7355	CAP_603	mlb[66C6]
C7360	CAP_0603	mlb[66B5]
C7361	CAP_0603	mlb[66B5]
C7398	CAP_402	mlb[66C3]
C7399	CAP_402	mlb[66C3]
C7400	CAP_402	mlb[67C2]
C7401	CAP_402	mlb[67C2]
C7402	CAP_402	mlb[67C2]
C7403	CAP_402	mlb[67C2]
C7404	CAP_402	mlb[67C2]
C7405	CAP_402	mlb[67B2]
C7406	CAP_402	mlb[67C2]
C7409	CAP_402	mlb[67C4]
C7411	CAP_402	mlb[67A2]
C7412	CAP_402	mlb[67B2]
C7413	CAP_402	mlb[67D5]
C7414	CAP_603	mlb[67C3]
C7416	CAP_402	mlb[67D7]
C7417	CAP_402	mlb[67C7]
C7418	CAP_402	mlb[67C7]
C7419	CAP_402	mlb[67C8]
C7420	CAP_402	mlb[67C7]
C7422	CAP_402	mlb[67B8]
C7423	CAP_402	mlb[67B7]
C7426	CAP_402	mlb[67A6]
C7427	CAP_402	mlb[67A5]
C7432	CAP_402	mlb[67B7]
C7455	CAP_402	mlb[67D6]
C7456	CAP_402	mlb[67D6]
C7457	CAP_402	mlb[67D6]
C7458	CAP_402	mlb[67A6]
C7459	CAP_402	mlb[67A7]
C7460	CAP_402	mlb[67A6]
C7501	CAP_402	mlb[68D7]
C7503	CAP_402	mlb[68D5]
C7505	CAP_P_SM	mlb[68D3]
C7506	CAP_P_SM	mlb[68D3]
C7507	CAP_603	mlb[68D4]
C7508	CAP_402	mlb[68D4]
C7509	CAP_402	mlb[68D3]
C7510	CAP_402	mlb[68D4]
C7511	CAP_402	mlb[68D4]
C7515	CAP_P_SM	mlb[68D3]
C7520	CAP_402	mlb[68B3]

C7521	CAP_402	mlb[68C7]
C7523	CAP_402	mlb[68C5]
C7526	CAP_P_SM	mlb[68D2]
C7528	CAP_402	mlb[68B4]
C7530	CAP_402	mlb[68C4]
C7531	CAP_402	mlb[68C4]
C7560	CAP_P_CASE-B4-SM	mlb[68A7]
C7561	CAP_P_CASE-B4-SM	mlb[68A6]
C7562	CAP_P_CASE-B4-SM	mlb[68A6]
C7563	CAP_P_CASE-B4-SM	mlb[68A6]
C7564	CAP_P_CASE-B4-SM	mlb[68A5]
C7565	CAP_P_CASE-B4-SM	mlb[68A5]
C7580	CAP_402	mlb[68D5]
C7581	CAP_603	mlb[68D5]
C7582	CAP_603	mlb[68C4]
C7601	CAP_402	mlb[69C7]
C7602	CAP_402	mlb[69C3]
C7603	CAP_402	mlb[69C6]
C7607	CAP_402	mlb[69D4]
C7608	CAP_402	mlb[69C4]
C7610	CAP_402	mlb[69D4]
C7615	CAP_603	mlb[69D4]
C7620	CAP_P_CASE-B4-SM	mlb[69C3]
C7621	CAP_P_CASE-B4-SM	mlb[69C2]
C7622	CAP_P_CASE-B4-SM	mlb[69C2]
C7623	CAP_402	mlb[69C1]
C7633	CAP_402	mlb[69D3]
C7634	CAP_603	mlb[69D3]
C7635	CAP_P_CASE-B4-SM	mlb[69C2]
C7651	CAP_P_SM	mlb[69D7]
C7652	CAP_P_SM	mlb[69C6]
C7653	CAP_P_SM	mlb[69C5]
C7701	CAP_603	mlb[70C5]
C7702	CAP_402	mlb[70B6]
C7703	CAP_402	mlb[70B7]
C7704	CAP_402	mlb[70B7]
C7705	CAP_402	mlb[70B7]
C7720	CAP_P_SM	mlb[70C4]
C7721	CAP_P_SM	mlb[70C4]
C7722	CAP_402	mlb[70C3]
C7723	CAP_402	mlb[70C2]
C7724	CAP_402	mlb[70C3]
C7725	CAP_P_CASE-B4-SM	mlb[70C2]
C7726	CAP_P_CASE-B4-SM	mlb[70C2]
C7727	CAP_P_CASE-B4-SM	mlb[70C2]
C7730	CAP_402	mlb[70C5]
C7731	CAP_402	mlb[70B3]
C7740	CAP_402	mlb[70B3]
C7860	CAP_0805	mlb[71D7]
C7861	CAP_402	mlb[71D7]
C7862	CAP_0603	mlb[71D5]
C7863	CAP_402	mlb[71D5]
C7864	CAP_402	mlb[71C7]
C7865	CAP_402	mlb[71C8]
C7866	CAP_402	mlb[71D6]
C7867	CAP_0805	mlb[71D7]
C7868	CAP_402	mlb[71C7]
C7870	CAP_402	mlb[71B7]
C7871	CAP_603	mlb[71A7]
C7872	CAP_603	mlb[71B6]
C7873	CAP_0603	mlb[71D5]
C7900	CAP_402	mlb[72B7]
C7901	CAP_402	mlb[72B7]
C7902	CAP_603	mlb[72B6]
C7920	CAP_402	mlb[72B6]
C7950	CAP_402	mlb[72C2]
C7951	CAP_402	mlb[72C2]
C7952	CAP_402	mlb[72C2]
C7953	CAP_402	mlb[72C1]
C7962	CAP_402	mlb[72B2]
C7963	CAP_402	mlb[72B1]
C7970	CAP_402	mlb[72B2]
C7971	CAP_402	mlb[72B2]
C7972	CAP_402	mlb[72B2]
C7973	CAP_402	mlb[72B1]
C9000	CAP_402	mlb[74D6]
C9001	CAP_402	mlb[74D6]
C9002	CAP_402	mlb[74D6]
C9003	CAP_402	mlb[74D6]
C9004	CAP_402	mlb[74D6]
C9005	CAP_402	mlb[74D6]
C9006	CAP_402	mlb[74D6]
C9007	CAP_402	mlb[74D6]
C9015	CAP_402	mlb[74D5]
C9016	CAP_402	mlb[74C5]
C9020	CAP_402	mlb[74B7]
C9021	CAP_402	mlb[74B7]
C9022	CAP_402	mlb[74B7]
C9023	CAP_402	mlb[74B7]
C9024	CAP_402	mlb[74B7]
C9025	CAP_402	mlb[74B7]
C9026	CAP_402	mlb[74B7]
C9027	CAP_402	mlb[74B7]
C9028	CAP_402	mlb[74B7]
C9029	CAP_402	mlb[74B7]
C9040	CAP_402	mlb[74D2]
C9041	CAP_402	mlb[74D2]
C9042	CAP_402	mlb[74D2]
C9043	CAP_402	mlb[74D2]
C9044	CAP_402	mlb[74D2]
C9045	CAP_402	mlb[74D2]
C9046	CAP_402	mlb[74D2]
C9047	CAP_402	mlb[74D2]
C9085	CAP_402	mlb[74B2]
C9086	CAP_402	mlb[74B2]
C9090	CAP_402-1	mlb[74C7]
C9100	CAP_603	mlb[75D7]
C9101	CAP_603	mlb[75D7]
C9105	CAP_402-1	mlb[75D7]
C9106	CAP_402-1	mlb[75D6]
C9107	CAP_402-1	mlb[75D6]
C9108	CAP_402-1	mlb[75D6]
C9109	CAP_402-1	mlb[75D5]
C9110	CAP_402-1	mlb[75D7]
C9111	CAP_402-1	mlb[75D6]
C9112	CAP_402-1	mlb[75D6]
C9113	CAP_402-1	mlb[75D6]
C9114	CAP_402-1	mlb[75D5]
C9120	CAP_402-1	mlb[75C6]
C9121	CAP_402-1	mlb[75C6]
C9122	CAP_402-1	mlb[75C5]
C9130	CAP_402-LF	mlb[75C5]
C9143	CAP_402-1	mlb[75D3]
C9144	CAP_402-1	mlb[75D4]

C9145	CAP_402-1	mlb[75D3]
C9146	CAP_603	mlb[75D3]
C9147	CAP_603	mlb[75D3]
C9150	CAP_402-1	mlb[75C3]
C9151	CAP_402-1	mlb[75C3]
C9152	CAP_402-1	mlb[75C3]
C9153	CAP_402-1	mlb[75C4]
C9160	CAP_402-LF	mlb[75C4]
C9170	CAP_402-LF	mlb[75C4]
C9200	CAP_402	mlb[76C7]
C9210	CAP_402-1	mlb[76B7]
C9215	CAP_402-1	mlb[76A7]
C9221	CAP_0201	mlb[76B2]
C9222	CAP_0201	mlb[76B2]
C9223	CAP_0201	mlb[76B2]
C9224	CAP_0201	mlb[76B2]
C9225	CAP_0201	mlb[76A4]
C9226	CAP_0201	mlb[76A2]
C9227	CAP_0201	mlb[76A2]
C9228	CAP_0201	mlb[76B4]
C9230	CAP_0201	mlb[76A4]
C9231	CAP_0201	mlb[76B4]
C9300	CAP_402	mlb[77D7]
C9301	CAP_402	mlb[77D7]
C9302	CAP_402	mlb[77D7]
C9303	CAP_402	mlb[77D7]
C9304	CAP_402	mlb[77D7]
C9305	CAP_402	mlb[77D7]
C9306	CAP_402	mlb[77D7]
C9307	CAP_402	mlb[77D7]
C9308	CAP_402	mlb[77D7]
C9309	CAP_402	mlb[77D7]
C9310	CAP_402-LF	mlb[77C7]
C9311	CAP_402	mlb[77C7]
C9312	CAP_402	mlb[77C7]
C9319	CAP_402-LF	mlb[77B5]
C9330	CAP_402	mlb[77A5]
C9331	CAP_402	mlb[77A5]
C9357	CAP_402	mlb[77A7]
C9358	CAP_402	mlb[77C3]
C9359	CAP_402	mlb[77C3]
C9360	CAP_0201	mlb[77C3]
C9361	CAP_0201	mlb[77C3]
C9362	CAP_402	mlb[77C4]
C9363	CAP_402	mlb[77C4]
C9364	CAP_0201	mlb[77C3]
C9365	CAP_0201	mlb[77C3]
C9366	CAP_402	mlb[77C4]
C9367	CAP_402	mlb[77C4]
C9368	CAP_402	mlb[77B4]
C9369	CAP_402	mlb[77B4]
C9370	CAP_201	mlb[77D3]
C9371	CAP_201	mlb[77D3]
C9372	CAP_201	mlb[77D3]
C9373	CAP_201	mlb[77D3]
C9380	CAP_201	mlb[77D3]
C9381	CAP_201	mlb[77D3]
C9382	CAP_201	mlb[77D3]
C9383	CAP_201	mlb[77D3]
C9390	CAP_402	mlb[77B1]
C9391	CAP_402	mlb[77B1]
C9400	CAP_402	mlb[78C6]
C9401	CAP_0201	mlb[78A6]
C9402	CAP_0201	mlb[78A6]
C9405	CAP_201	mlb[78C2]
C9406	CAP_201	mlb[78B2]
C9410	CAP_603-1	mlb[78D3]
C9411	CAP_603-1	mlb[78D2]
C9420	CAP_0805	mlb[78D8]
C9421	CAP_402	mlb[78D8]
C9422	CAP_0805	mlb[78D7]
C9423	CAP_402	mlb[78D6]
C9424	CAP_805	mlb[78D5]
C9425	CAP_805	mlb[78D5]
C9450	CAP_603-1	mlb[78C7]
C9470	CAP_201	mlb[78B2]
C9471	CAP_201	mlb[78B2]
C9472	CAP_201	mlb[78B2]
C9473	CAP_201	mlb[78B2]
C9494	CAP_201	mlb[78A7]
C9495	CAP_201	mlb[78A7]
C9498	CAP_402	mlb[78A7]
C9499	CAP_402	mlb[78A6]
C9710	CAP_402	mlb[79D7]
C9711	CAP_402	mlb[79D7]
C9712	CAP_402	mlb[79C7]
C9713	CAP_402	mlb[79D7]
C9714	CAP_402	mlb[79C7]
C9715	CAP_402	mlb[79C7]
C9716	CAP_402	mlb[79C7]
C9717	CAP_402	mlb[79C7]
C9740	CAP_402	mlb[79D3]
C9741	CAP_402	mlb[79D2]
C9742	CAP_402	mlb[79D2]
C9743	CAP_402	mlb[79D2]
C9744	CAP_402	mlb[79D4]
C9745	CAP_402	mlb[79D4]
C9746	CAP_402	mlb[79D3]
C9747	CAP_402	mlb[79D3]
C9748	CAP_402	mlb[79D3]
C9749	CAP_402	mlb[79D2]
C9750	CAP_402	mlb[79D2]
C9751	CAP_402	mlb[79D2]
C9760	CAP_402-LF	mlb[79B5]
C9800	CAP_0603	mlb[80C4]
C9802	CAP_402	mlb[80C4]
C9803	CAP_603	mlb[80C3]
C9810	CAP_402	mlb[80B5]
C9811	CAP_402	mlb[80B6]
C9813	CAP_402	mlb[80A6]
C9814	CAP_402	mlb[80A6]
C9830	CAP_603	mlb[80C2]
CL3601	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3602	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3603	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3604	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3606	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3608	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]

CL3614	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]	
CL3615	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]	
CL3616	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]	
CL3617	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]	
CL3618	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]	
D2400	DIODE_SCHOT_6PB_SOT-363	mlb[23B7 23C7]	
D2600	DIODE_SCHOT_SOD-523	mlb[25B1]	
D2800	DIODE_SCHOT_6PB_SOT-363	mlb[27D6]	
D3800	RCLAMP0524P_SLP2510P8	mlb[36B7]	
D3801	RCLAMP0524P_SLP2510P8	mlb[36B7]	
D4300	DIODE_SMB	mlb[41D4]	
D4305	DIODE_3P_CA_SOT-523-3	mlb[41D5]	
D4350	DIODE_SCHOT_3P_SOT323	mlb[41A4]	
D4390	ZENER_SOT23	mlb[41B2]	
D4600	DIODE_SCHOT_3P_A_SC-75	mlb[43B2]	
D4601	DIODE_SCHOT_3P_A_SC-75	mlb[43B4]	
D4602	DIODE_SCHOT_3P_A_SC-75	mlb[43A4]	
D4603	DIODE_SCHOT_3P_A_SC-75	mlb[43C2]	
D4700	DIODE_SCHOT_SOD-323	mlb[44C5]	
D9360	DIODE_TSLP-2-7	mlb[77D2]	
D9361	DIODE_TSLP-2-7	mlb[77C2]	
D9364	DIODE_TSLP-2-7	mlb[77D2]	
D9365	DIODE_TSLP-2-7	mlb[77D2]	
D9372	DIODE_TSLP-2-7	mlb[77D2]	
D9373	DIODE_TSLP-2-7	mlb[77D2]	
D9382	DIODE_TSLP-2-7	mlb[77D2]	
D9383	DIODE_TSLP-2-7	mlb[77D2]	
D9401	DIODE_SCHOT_POWERDI-123	mlb[78D6]	
D9403	ZENER_SOT23	mlb[78D3]	
D9410	DIODE_SCHOT_DSN2	mlb[78D1]	
D9498	DIODE_TSLP-2-7	mlb[78B7]	
D9499	DIODE_TSLP-2-7	mlb[78B7]	
D9800	RCLAMP0504F_SC70-6-1	mlb[80B7]	
D9810	RCLAMP0524P_SLP2510P8	mlb[80D6 80C6]	
D9811	RCLAMP0524P_SLP2510P8	mlb[80D6 80C6]	
DP4310	DIODE_DUAL_6P_SOT-363	mlb[41C3 41C3]	
DP4311	DIODE_DUAL_6P_SOT-363	mlb[41B3 41B3]	
DZ6000	SUPPR_TRANSIENT1_402	mlb[57C6]	
DZ6001	SUPPR_TRANSIENT1_402	mlb[57C6]	
DZ6002	SUPPR_TRANSIENT1_SOD882	mlb[57C6]	
DZ6003	SUPPR_TRANSIENT1_402	mlb[57C5]	
DZ6004	SUPPR_TRANSIENT1_402	mlb[57C5]	
DZ6005	SUPPR_TRANSIENT1_SOD882	mlb[57C5]	
DZ6006	SUPPR_TRANSIENT1_SOD882	mlb[57C5]	
DZ6050	SUPPR_TRANSIENT1_402	mlb[57A5]	
DZ6051	SUPPR_TRANSIENT1_SOD882	mlb[57A7]	
DZ6052	SUPPR_TRANSIENT1_402	mlb[57A5]	
DZ6053	SUPPR_TRANSIENT1_402	mlb[57A5]	
DZ6054	SUPPR_TRANSIENT1_SOD882	mlb[57A6]	
DZ6055	SUPPR_TRANSIENT1_SOD882	mlb[57A6]	
F4300	FUSE_603	mlb[41D3]	
J0900	TP1_SM-TP3P4X1P8-TOP	mlb[9B5]	
J0901	TP1_SM-TP3P4X1P8-TOP	mlb[9B5]	
J2500	CON_F60ST_D_SM1_F-ST-SM	mlb[24D6]	
J2800	BATTERY_2P_SM	mlb[27D8]	
J3100	CON_F408RT_4MT_DDR3IMM_SM1_F-RT-SM	mlb[30D6]	
J3100	CON_F408RT_4MT_DDR3IMM_SM1_F-RT-SM	mlb[31D6]	
J3500	CON_F16RT_4MT_SDCARD_S_TH_F-RT-TH	mlb[34C2]	
J3601	CON_F30ST_D4MT_SM_F-ST-SM	mlb[35D6]	
J3800	CON_RJ45_8RT_D4MT_TH2_F-R-TH	mlb[36C1]	
J4300	CON_F9RT_D4MT_1394B_TH_F-RT-TH	mlb[41C1]	
J4401	CON_F16ST_D_SM_F-ST-SM-J40	mlb[42D6]	
J4410	CON_F16ST_D_SM_F-ST-SM-J40	mlb[42D3]	
J4600	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43D1]	
J4610	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43C1]	
J4620	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43B4]	
J4630	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43A3]	
J4800	CON_M5RT_S2MT_SMA_M-RT-SM	mlb[45D2]	
J4801	CON_M2RT_S2MT_SM_M-RT-SM	mlb[45A4]	
J5100	CON_M30ST_D4MT_SM_M-ST-SM	mlb[48D4]	
J6000	CON_F21RT_4MT_AUDIO_SPDIF_TH1_F-RT-TH	mlb[57C8]	
J6001	CON_M2RT_S2MT_SM_M-RT-SM	mlb[57B1]	
J6500	CON_M4RT_S2MT_SM_M-RT-SM	mlb[60C2]	
J7900	CON_M9RT_S_SM_M-RT-SM	mlb[72B8]	
J9400	CON_F20RT_D16MT_DSPLYPRT_TH_F-RT-TH	mlb[78B3]	
J9830	CON_F19RT_17MT_HDMI_F-RT-SM	mlb[80C3]	

L2406	IND_0805	mlb[23D8]	
L2451	IND_0603	mlb[23C4]	
L2490	IND_0603	mlb[23B4]	
L2491	IND_0603	mlb[23B4]	
L3540	IND_0402	mlb[34C6]	
L3541	IND_0402	mlb[34C5]	
L3550	IND_0402	mlb[34C4]	
L3551	IND_0402	mlb[34C3]	
L3601	FILTER_4P2_DLP11S	mlb[35D5]	
L3603	FILTER_4P2_DLP0NS	mlb[35C5]	
L3604	IND_0603	mlb[35C5]	
L3606	IND_0402	mlb[35C5]	
L3900	IND_SM	mlb[37D7]	
L3905	IND_SM	mlb[37D7]	
L3910	IND_SM	mlb[37C7]	
L3920	IND_SM	mlb[37D2]	
L3925	IND_SM	mlb[37D2]	
L3930	IND_SM	mlb[37C2]	
L4020	IND_2520	mlb[38D6]	
L4250	IND_0402	mlb[40D3]	
L4251	IND_0402	mlb[40D2]	
L4252	IND_0402	mlb[40C3]	
L4253	IND_0402	mlb[40C2]	
L4300	IND_SM	mlb[41D2]	
L4310	FILTER_4P_TCM1210-4SM	mlb[41C2]	
L4311	FILTER_4P_TCM1210-4SM	mlb[41C2]	
L4600	IND_0603	mlb[43D3]	
L4602	FILTER_4P_2012-HF	mlb[43D3]	
L4610	IND_0603	mlb[43C3]	
L4612	FILTER_4P_2012-HF	mlb[43B3]	
L4620	IND_0603	mlb[43C5]	
L4622	FILTER_4P_2012-HF	mlb[43B5]	
L4630	IND_0603	mlb[43A5]	
L4632	FILTER_4P_2012-HF	mlb[43A5]	
L4800	IND_SM	mlb[45B2]	
L4810	IND_0402	mlb[45D2]	
L4811	IND_0402	mlb[45C2]	
L5650	IND_0402	mlb[53A7]	
L5651	IND_0402	mlb[53A7]	
L5801	IND_0402	mlb[55B5]	
L5900	IND_0402	mlb[56B7]	
L5901	IND_0402	mlb[56C7]	
L5902	IND_0402	mlb[56B7]	
L6000	IND_0402	mlb[57D4]	
L6001	IND_0402	mlb[57D4]	
L6002	IND_0402	mlb[57D4]	
L6003	IND_0402	mlb[57C4]	
L6004	IND_0603	mlb[57C4]	
L6005	IND_0402	mlb[57C4]	
L6006	IND_0402	mlb[57D4]	
L6007	IND_0402	mlb[57D4]	
L6051	IND_0402	mlb[57B4]	
L6052	IND_0402	mlb[57B4]	
L6053	IND_0402	mlb[57B4]	
L6054	IND_0402	mlb[57B4]	
L6092	IND_0603	mlb[57C2]	
L6100	IND_0402	mlb[58A3]	
L6180	IND_0402	mlb[58D3]	
L6500	IND_0402	mlb[60C3]	
L6510	FILTER_2P_0603	mlb[60D3]	
L6520	FILTER_2P_0603	mlb[60C3]	
L7100	IND_FDV0630H-SM	mlb[64C3]	
L7201	IND_MMD-06CZ	mlb[65C4]	
L7251	IND_PIMB065T-SM	mlb[65B4]	
L7302	IND_PIMB042T-COMBO	mlb[66D5]	
L7330	IND_PIMB103E-SM-1	mlb[66C3]	
L7500	IND_PCMB063T-MMD06CZ-SM	mlb[68D5]	
L7501	IND_PIMA104E-SM-1	mlb[68D3]	
L7521	IND_PIMA104E-SM-1	mlb[68C3]	
L7601	IND_PIMA104E-SM-1	mlb[69C4]	
L7602	IND_PIMB042T-COMBO	mlb[69D3]	
L7730	IND_PIMB104T-SM	mlb[70C3]	
L7860	IND_2520	mlb[71D6]	
L9130	IND_0402	mlb[75C7]	
L9170	IND_0402	mlb[75C2]	
L9372	IND_0201-1	mlb[77D4]	
L9373	IND_0201-1	mlb[77D4]	
L9382	IND_0201-1	mlb[77D4]	
L9383	IND_0201-1	mlb[77D4]	
L9400	IND_0603	mlb[78C5]	
L9408	IND_0603	mlb[78A2]	
L9498	IND_0603	mlb[78B6]	
L9499	IND_0603	mlb[78A6]	
L9810	IND_0402	mlb[80B6]	
L9811	IND_0402	mlb[80A6]	
L9830	IND_SM-1	mlb[80D2]	
L9841	IND_0402	mlb[80A6]	
L9890	FILTER_4P_ACM2012H	mlb[80D7]	
L9891	FILTER_4P_ACM2012H	mlb[80C7]	
L9892	FILTER_4P_ACM2012H	mlb[80C7]	
L9893	FILTER_4P_ACM2012-SM	mlb[80B7]	
LED0600	LED_2.0X1.25MM-SM	mlb[6C3]	
LED0602	LED_2.0X1.25MM-SM	mlb[6C2]	
LED0603	LED_2.0X1.25MM-SM	mlb[6C1]	
LED0605	LED_2X125-SM	mlb[6B1]	
Q0603	TRA_SSM3K15FV_SOD-VESM-HF	mlb[6C2]	
Q0605	TRA_NMOSFET_NPN_6P2_SOT-563	mlb[6B2 6B2]	
Q2520	TRA_SSM3K15FV_SOD-VESM-HF	mlb[24B5]	
Q2530	TRA_PNP_SOT323_SOT323	mlb[24C1]	
Q2550	TRA_SSM3K15FV_SOD-VESM-HF	mlb[24B3]	
Q2640	TRA_2N7002DW_SOT-363	mlb[25B2 25B1]	
Q2900	TRA_DUAL_SSM6N15FE_SOT563	mlb[28B6 28C6]	
Q2905	TRA_DUAL_SSM6N15FE_SOT563	mlb[28C6 28C6]	
Q2910	TRA_DUAL_SSM6N15FE_SOT563	mlb[28B6 28B6]	
Q2915	TRA_DUAL_SSM6N15FE_SOT563	mlb[28B7 28B6]	
Q2920	TRA_NMOSFET_NPN_6P2_SOT-563	mlb[28C2 28C3]	
Q2950	TRA_DUAL_SSM6N15FE_SOT563	mlb[28B2 28B3]	
Q3530	TRA_SSM3K15FV_SOD-VESM-HF	mlb[34B5]	
Q3650	TRA_MOSFET_PCHN_8P4_23V1K-SM	mlb[35C3]	

Q4010	TRA_DUAL_SSM6N15FE_SOT563	mlb[38A4 38B3]	
Q4050	TRA_SSM3K15FV_SOD-VESM-HF	mlb[38C3]	
Q4300	TRA_MOSFET_PCHN_5P1_MLP3.3X3.3	mlb[41D5]	
Q4301	TRA_PNP_SOT23_SOT23	mlb[41D7]	
Q4302	TRA_DUAL_MMDT3906_SOT-363	mlb[41C6 41C5]	
Q4303	TRA_DUAL_MMDT3904_SOT-363-LF	mlb[41B5 41B5]	
Q4305	TRA_BSS84_S0T23-3-HF	mlb[41D6]	
Q4370	TRA_2N7002DW_SOT-363	mlb[41C7 41C7]	
Q4800	TRA_SSM3K15FV_SOD-VESM-HF	mlb[45C6]	
Q4801	TRA_DUAL_MMDT3906_SOT-363	mlb[45D5 45D5]	
Q5059	TRA_DUAL_SSM6N15FE_SOT563	mlb[47D3 47C3]	
Q5060	TRA_NMOSFET_NPN_6P2_SOT-563	mlb[47D2 47D2]	
Q5415	TRA_DUAL_COMP_DMG101_SOT-563	mlb[51D3 51C3]	
Q5520	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52D2]	
Q5540	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52A7]	
Q5560	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52B2]	
Q5570	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52C2]	
Q5580	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52C2]	
Q5590	TRA_BC846BM3T5G_NPN_SOT732-3	mlb[52B2]	
Q6100	TRA_DUAL_SSM6N15FE_SOT563	mlb[58C7 58B6]	
Q6101	TRA_DUAL_SSM6N15FE_SOT563	mlb[58C5 58C6]	
Q6102	TRA_SSM3K15FV_SOD-VESM-HF	mlb[58A5]	
Q6103	TRA_DUAL_SSM6N15FE_SOT563	mlb[58B3 58B2]	
Q6500	TRA_FDC638P_SM	mlb[60D4]	
Q6501	TRA_SSM3K15FV_SOD-VESM-HF	mlb[60C6]	
Q6700	TRA_MOSFET_PCHN_4P_SC70-6L	mlb[61D2]	
Q6701	TRA_MOSFET_NCHN_PWRPK-1212-8-HF	mlb[61B6]	
Q6702	TRA_DUAL_SSM6N15FE_SOT563	mlb[61B3 61D4]	
Q6710	TRA_MOSFET_PCHN_4P_SC70-6L	mlb[61D6]	
Q6711	TRA_DUAL_SSM6N15FE_SOT563	mlb[61D7]	
Q6712	TRA_DUAL_SSM6N15FE_SOT563	mlb[61C4]	
Q6722	TRA_DUAL_SSM6N15FE_SOT563	mlb[61C4]	
Q6730	TRA_MOSFET_PCHN_4P_SC70-6L	mlb[61C2]	
Q6740	TRA_MOSFET_PCHN_4P_SC70-6L	mlb[61C2]	
Q6760	TRA_MOSFET_PCHN_8P4_23V1K-SM	mlb[61B2]	
Q6821	TRA_SSM3K15FV_SOD-VESM-HF	mlb[62A3]	
Q6822	TRA_SINGLE_MOSFET_PCHN-HF_SOT-23-HF	mlb[62B1]	
Q6825	TRA_2N7002DW_SOT-363	mlb[62A2 62A3]	
Q6850	TRA_NMOSFET_NPN_8P_DFN2015H4-8	mlb[62C7]	
Q7100	TRA_DUAL_MOSFET_NCHN9_WPAK2	mlb[64C4]	
Q7330	TRA_MOSFET_NCHN_5P1_HVSON-3333	mlb[66C4]	
Q7335	TRA_MOSFET_NCHN_5P5_HVSON-333	mlb[66C4]	
Q7503	TRA_DUAL_MOSFET_NCHN9_WPAK	mlb[68D5]	
Q7523	TRA_DUAL_MOSFET_NCHN9_WPAK	mlb[68C5]	
Q7603	TRA_DUAL_MOSFET_NCHN9_WPAK	mlb[69C5]	
Q7730	TRA_DUAL_MOSFET_NCHN9_WPAK2	mlb[70C4]	
Q9320	TRA_SSM3K15FV_SOD-VESM-HF	mlb[77A4]	
Q9415	TRA_SSM3K15FV_SOD-VESM-HF	mlb[78C4]	
Q9420	TRA_2N7002DW_SOT-363	mlb[78C6 78C6]	
R0600	RES_402	mlb[6D3]	
R0602	RES_402	mlb[6D2]	
R0603	RES_402	mlb[6D1]	
R0605	RES_402	mlb[6C1]	
R0615	RES_402	mlb[6B2]	
R0616	RES_402	mlb[6B3]	
R1010	RES_402	mlb[10D5]	
R1020	RES_402	mlb[10B2]	
R1021	RES_402	mlb[10B2]	
R1022	RES_402	mlb[10B2]	
R1023	RES_402	mlb[10B3]	
R1030	RES_402	mlb[10C8]	
R1040	RES_402	mlb[10A7]	
R1041	RES_402	mlb[10A6]	
R1042	RES_402	mlb[10A8]	
R1043	RES_402	mlb[10A6]	
R1044	RES_402	mlb[10A8]	
R1045	RES_402	mlb[10A7]	
R1046	RES_402	mlb[10A7]	
R1047	RES_402	mlb[10A7]	
R1049	RES_402	mlb[10A6]	
R1064	RES_402	mlb[10D4]	
R1065	RES_402	mlb[10C4]	
R1070	RES_402	mlb[10D4]	
R1071	RES_402	mlb[10C4]	
R1100	RES_402	mlb[11C5]	
R1101	RES_402	mlb[11C6]	
R1102	RES_402	mlb[11C5]	
R1103	RES_402	mlb[11C6]	
R1104	RES_402	mlb[11C5]	
R1111	RES_402	mlb[11B4]	

R1112	RES_402	mlb[11B5]	
R1113	RES_402	mlb[11B5]	
R1114	RES_402	mlb[11B5]	
R1120	RES_402	mlb[11C7]	
R1121	RES_402	mlb[11C6]	
R1125	RES_402	mlb[11B6]	
R1126	RES_402	mlb[11B7]	
R1140	RES_402	mlb[11C2]	
R1141	RES_402	mlb[11C2]	
R1300	RES_402	mlb[13B5]	
R1302	RES_402	mlb[13B6]	
R1310	RES_402	mlb[13B5]	
R1311	RES_402	mlb[13B5]	
R1312	RES_402	mlb[13B5]	
R1313	RES_402	mlb[13B2]	
R1314	RES_402	mlb[13B2]	
R1320	RES_402	mlb[13B6]	
R1330	RES_402	mlb[13B1]	
R1331	RES_402	mlb[13B1]	
R1362	RES_402	mlb[13A5]	
R1363	RES_402	mlb[13A5]	
R1382	RES_402	mlb[13C1]	
R1600	RES_402	mlb[15B2]	
R1601	RES_0603	mlb[15A7]	
R1702	RES_0603	mlb[16A7]	
R1800	RES_201	mlb[17A8]	
R1801	RES_201	mlb[17A8]	
R1802	RES_201	mlb[17B7]	
R1803	RES_201	mlb[17B7]	
R1810	RES_201	mlb[17A5]	
R1811	RES_201	mlb[17A4]	
R1812	RES_201	mlb[17A5]	
R1813	RES_201	mlb[17A4]	
R1820	RES_201	mlb[17D5]	
R1830	RES_201	mlb[17C5]	
R1831	RES_201	mlb[17C5]	
R1832	RES_201	mlb[17B5]	
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R1853	RES_201	mlb[17A3]	
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R1855	RES_201	mlb[17A2]	
R1860	RES_201	mlb[17D5]	
R1861	RES_201	mlb[17D5]	
R1862	RES_201	mlb[17D5]	
R1863	RES_201	mlb[17D5]	
R1864	RES_201	mlb[17D5]	
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R1897	RES_201	mlb[17A6]	
R1900	RES_201	mlb[18D8]	
R1905	RES_201	mlb[18D8]	
R1909	RES_201	mlb[18B7]	
R1915	RES_201	mlb[18B5]	
R1920	RES_201	mlb[18C8]	
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R1922	RES_201	mlb[18A4]	
R1924	RES_201	mlb[18A4]	
R1925	RES_201	mlb[18A7]	
R1951	RES_201	mlb[18B4]	
R1980	RES_201	mlb[18B5]	
R1981	RES_201	mlb[18C5]	
R1982	RES_201	mlb[18A7]	
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R2017	RES_201	mlb[19D7]	
R2018	RES_201	mlb[19D7]	
R2030	RES_201	mlb[19D7]	
R2031	RES_201	mlb[19D7]	
R2052	RES_201	mlb[19A7]	
R2053	RES_201	mlb[19A7]	
R2054	RES_201	mlb[19A6]	
R2060	RES_201	mlb[19C3]	
R2061	RES_201	mlb[19C3]	
R2062	RES_201	mlb[19C3]	
R2064	RES_201	mlb[19C3]	
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R2067	RES_201	mlb[19C2]	
R2068	RES_201	mlb[19C2]	
R2069	RES_201	mlb[19C2]	
R2070	RES_201	mlb[19B4]	
R2111	RES_201	mlb[20D8]	
R2112	RES_201	mlb[20D7]	
R2113	RES_201	mlb[20D7]	
R2114	RES_201	mlb[20A7]	
R2115	RES_201	mlb[20A7]	
R2116	RES_201	mlb[20A3]	
R2117	RES_201	mlb[20A6]	
R2118	RES_201	mlb[20A2]	
R2130	RES_201	mlb[20A3]	
R2140	RES_201	mlb[20D3]	
R2150	RES_201	mlb[20D3]	
R2155	RES_201	mlb[20D3]	
R2156	RES_201	mlb[20C3]	

R6881	RES_402	mlb[62C3]
R6886	RES_402	mlb[62C2]
R6887	RES_402	mlb[62C3]
R6888	RES_402	mlb[62C2]
R7101	RES_402	mlb[64C5]
R7102	RES_603	mlb[64C5]
R7103	RES_402	mlb[64B6]
R7104	RES_402	mlb[64C7]
R7120	RES_603	mlb[64C3]
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R7146	RES_402	mlb[64C6]
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R7160	RES_603	mlb[64B2]
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R7204	RES_402	mlb[65D7]
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R7211	RES_402	mlb[65C4]
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R7301	RES_603	mlb[66C7]
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R7321	RES_402	mlb[66B8]
R7330	RES_402	mlb[66C5]
R7331	RES_603	mlb[66C4]
R7340	RES_SENSE_0612	mlb[66C2]
R7405	RES_402	mlb[67D3]
R7406	RES_402	mlb[67D3]
R7408	RES_402	mlb[67C2]
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R7432	RES_402	mlb[67C7]
R7433	RES_402	mlb[67C7]
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R7506	RES_603	mlb[68D4]
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R7524	RES_402	mlb[68C6]
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R7526	RES_603	mlb[68C4]
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R7620	RES_SENSE_0612	mlb[69C3]
R7701	RES_402	mlb[70C6]
R7702	RES_603	mlb[70C5]
R7703	RES_402	mlb[70B6]
R7704	RES_402	mlb[70C8]
R7705	RES_402	mlb[70B8]
R7730	RES_402	mlb[70C5]
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R7741	RES_402	mlb[70B3]
R7742	RES_402	mlb[70B3]
R7744	RES_402	mlb[70C7]
R7745	RES_402	mlb[70B7]
R7760	RES_603	mlb[70B1]
R7860	RES_402	mlb[71C6]
R7861	RES_402	mlb[71C5]
R7862	RES_402	mlb[71C5]
R7863	RES_402	mlb[71D5]
R7865	RES_402	mlb[71C7]
R7870	RES_402	mlb[71B7]
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R8000	RES_201	mlb[73B4]
R8001	RES_201	mlb[73B4]
R9010	RES_402	mlb[74D5]
R9011	RES_402	mlb[74D5]
R9021	RES_402	mlb[74C6]
R9022	RES_402	mlb[74C6]
R9023	RES_402	mlb[74C6]
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R9031	RES_402	mlb[74A6]
R9032	RES_402	mlb[74A3]
R9040	RES_402	mlb[74A7]
R9041	RES_402	mlb[74A7]
R9051	RES_402	mlb[74D2]
R9055	RES_603	mlb[74C3]
R9085	RES_402	mlb[74A3]
R9090	RES_402	mlb[74C8]
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R9092	RES_402	mlb[74C6]
R9093	RES_402	mlb[74C6]
R9095	RES_402	mlb[74C2]
R9096	RES_402	mlb[74C2]
R9098	RES_402	mlb[74C2]
R9099	RES_402	mlb[74B3]
R9120	RES_402	mlb[75C7]
R9150	RES_402	mlb[75D2]
R9160	RES_402	mlb[75C2]
R9203	RES_402	mlb[76C7]
R9207	RES_402	mlb[76C6]
R9210	RES_402	mlb[76A7]
R9215	RES_402	mlb[76C7]
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R9228	RES_201	mlb[76B4]
R9230	RES_201	mlb[76B4]
R9231	RES_201	mlb[76B4]
R9300	RES_402	mlb[77B5]
R9301	RES_402	mlb[77B5]
R9302	RES_402	mlb[77B8]
R9308	RES_402	mlb[77C7]
R9309	RES_402	mlb[77D7]
R9310	RES_402	mlb[77B8]
R9311	RES_402	mlb[77B8]
R9312	RES_402	mlb[77B8]
R9318	RES_402	mlb[77B7]
R9319	RES_402	mlb[77B8]
R9330	RES_402	mlb[77A8]
R9334	RES_402	mlb[77A4]
R9335	RES_402	mlb[77A5]
R9336	RES_402	mlb[77A5]
R9338	RES_402	mlb[77A4]
R9339	RES_402	mlb[77A3]
R9350	RES_201	mlb[77C5]
R9351	RES_201	mlb[77C5]
R9352	RES_201	mlb[77C5]
R9353	RES_201	mlb[77C4]
R9354	RES_201	mlb[77C5]
R9355	RES_201	mlb[77C5]
R9360	RES_201	mlb[77C2]
R9361	RES_201	mlb[77C2]
R9364	RES_201	mlb[77C2]
R9365	RES_201	mlb[77C2]
R9372	RES_201	mlb[77D3]
R9373	RES_201	mlb[77D3]
R9374	RES_201	mlb[77D1]
R9375	RES_201	mlb[77D1]
R9382	RES_201	mlb[77D3]
R9383	RES_201	mlb[77D3]
R9384	RES_201	mlb[77C1]
R9385	RES_201	mlb[77C1]
R9392	RES_402	mlb[77B4]
R9393	RES_402	mlb[77B4]
R9396	RES_402	mlb[77B3]
R9397	RES_402	mlb[77B3]
R9398	RES_402	mlb[77B1]
R9399	RES_402	mlb[77B2]
R9401	RES_201	mlb[78A5]
R9402	RES_201	mlb[78A5]
R9403	RES_201	mlb[78B6]
R9404	RES_201	mlb[78B6]
R9407	RES_201	mlb[78B2]
R9408	RES_201	mlb[78A2]
R9410	RES_402	mlb[78C1]
R9411	RES_402	mlb[78C1]
R9412	RES_402	mlb[78C3]
R9416	RES_402	mlb[78D3]
R9417	RES_402	mlb[78D3]
R9418	RES_603	mlb[78D1]
R9421	RES_402	mlb[78D6]
R9422	RES_402	mlb[78D7]
R9423	RES_402	mlb[78D6]
R9424	RES_402	mlb[78D5]
R9425	RES_402	mlb[78D5]
R9426	RES_402	mlb[78C6]
R9430	RES_402	mlb[78C8]
R9431	RES_1206	mlb[78D8]
R9432	RES_1206	mlb[78D8]
R9441	RES_201	mlb[78A6]
R9450	RES_603	mlb[78D4]
R9451	RES_201	mlb[78A7]
R9452	RES_201	mlb[78A7]
R9470	RES_201	mlb[78B2]
R9471	RES_201	mlb[78B2]
R9472	RES_201	mlb[78A2]
R9473	RES_201	mlb[78A2]
R9494	RES_201	mlb[78B7]
R9495	RES_201	mlb[78B7]
R9498	RES_201	mlb[78B8]
R9499	RES_201	mlb[78B8]
R9724	RES_402	mlb[79A6]
R9725	RES_402	mlb[79A7]
R9726	RES_402	mlb[79A5]
R9740	RES_402	mlb[79B5]
R9741	RES_402	mlb[79B5]
R9750	RES_402	mlb[79B7]
R9753	RES_402	mlb[79C7]
R9754	RES_402	mlb[79B7]
R9755	RES_402	mlb[79C7]
R9756	RES_402	mlb[79B6]
R9757	RES_402	mlb[79C6]
R9758	RES_402	mlb[79B6]
R9759	RES_402	mlb[79C6]
R9761	RES_402	mlb[79C6]
R9762	RES_402	mlb[79B3]
R9763	RES_402	mlb[79C3]
R9764	RES_402	mlb[79B3]
R9765	RES_402	mlb[79C3]
R9766	RES_402	mlb[79B3]
R9768	RES_402	mlb[79B3]
R9769	RES_402	mlb[79C3]
R9810	RES_402	mlb[80B5]
R9811	RES_402	mlb[80B5]
R9812	RES_402	mlb[80B5]
R9813	RES_402	mlb[80A5]
R9814	RES_402	mlb[80A5]
RT7403	THERMISTER_0603	mlb[67D4]
RT7404	THERMISTER_0603	mlb[67A7]
S9200	SHLD_1P_SM	mlb[76D5]
S9201	SHLD_1P_SM	mlb[76D3]
S9202	SHLD_1P_SM	mlb[76D2]
S9203	SHLD_1P_SM	mlb[76D4]
S9204	SHLD_1P_SM	mlb[76D3]
S9205	SHLD_1P_SM	mlb[76D5]
S9206	SHLD_1P_SM	mlb[76D3]
S9207	SHLD_1P_SM	mlb[76D2]
S9208	SHLD_1P_SM	mlb[76D4]
S9209	SHLD_1P_SM	mlb[76D3]
S9210	SHLD_1P_SM	mlb[76D5]
S9211	SHLD_1P_SM	mlb[76D3]
S9212	SHLD_1P_SM	mlb[76D2]
S9213	SHLD_1P_SM	mlb[76D4]
S9214	SHLD_1P_SM	mlb[76D3]
S9215	SHLD_1P_SM	mlb[76D5]
S9216	SHLD_1P_SM	mlb[76D3]
S9217	SHLD_1P_SM	mlb[76D2]
S9218	SHLD_1P_SM	mlb[76D4]
S9219	SHLD_1P_SM	mlb[76D3]
S9220	SHLD_1P_SM	mlb[76C5]
S9221	SHLD_1P_SM	mlb[76C3]
S9222	SHLD_1P_SM	mlb[76C2]
S9223	SHLD_1P_SM	mlb[76C4]
S9224	SHLD_1P_SM	mlb[76C3]
S9225	SHLD_1P_SM	mlb[76C5]
S9226	SHLD_1P_SM	mlb[76C3]
S9227	SHLD_1P_SM	mlb[76C2]
S9228	SHLD_1P_SM	mlb[76C4]
S9229	SHLD_1P_SM	mlb[76C3]
SDF3600	PCB_STANDOFF	mlb[35A7]
SDF3601	PCB_STANDOFF	mlb[35A7]
SDF3602	PCB_STANDOFF	mlb[35A6]
SL9202	SLOT_TH-SP	mlb[76D6]
SL9203	SLOT_TH-SP	mlb[76D6]
T3801	XFR_TLA_6T213LF_SM	mlb[36C5]
T3802	XFR_TLA_6T213LF_SM	mlb[36C5]
TP4700	TP_TH-TP30	mlb[44C3]
TP4701	TP_TH-TP30	mlb[44C3]
TP4702	TP_TH-TP30	mlb[44C3]
TP4709	TP_TH-TP30	mlb[44C3]
U1000	SANDY_1023BGA_BGA	mlb[10D3 10D7]
U1000	SANDY_1023BGA_BGA	mlb[11C4]
U1000	SANDY_1023BGA_BGA	mlb[12D3 12D7]
U1000	SANDY_1023BGA_BGA	mlb[13D3 13D8]
U1000	SANDY_1023BGA_BGA	mlb[14D5 14D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[17D3 17D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[18D3 18D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[19D5]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[20D5]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[21D7 21C3]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[22D3 22D6]
U2150	MC74VHC1G08_SC70-HF	mlb[20C3]
U2151	MC74VHC1G08_SC70-HF	mlb[20B3]
U2152	MC74VHC1G08_SC70-HF	mlb[20B3]
U2520	SN74LV4066ARGYR_QFN1	mlb[24A7 24A7 24B7 24B7]
U2600	USB2513B_QFN	mlb[25D6]
U2650	USB2513B_QFN	mlb[25B6]
U2700	SLG3NB148_TQFN	mlb[26D5]
U2840	SN74LVC1G17_SOT553_S OT-553	mlb[27C3]
U2850	MC74VHC1G08_SC70-HF	mlb[27A7]
U2860	MC74VHC1G08_SC70-HF	mlb[27A6]
U2880	SN74LVC1G07_SC70	mlb[27C3]
U3400	DAC5574_MSOP	mlb[33D6]
U3401	PCA9557RGY_QFN	mlb[33C6]
U3402	OPAMP_MAX4253_UCSP_U CSP	mlb[33D3 33C3]
U3403	OPAMP_MAX4253_UCSP_U CSP	mlb[33B3 33C3]
U3404	OPAMP_MAX4253_UCSP_U CSP	mlb[33B3 33A3]
U3500	SWI_TPS2065_DGN	mlb[34D3]
U3530	SLG4AP014_TDFN	mlb[34B5]
U3535	SLG4AP014_TDFN	mlb[34B5]
U3540	SLG4AP016_TDFN	mlb[35B3]
U3900	BCM57765_1_QFN-8X8	mlb[37C5]
U3990	FLASH_AT45DB011D_SOI C-8S1	mlb[37A7]
U4100	XIO2211_1SYM_BGA	mlb[39C5]
U4200	LREG_TPS799195_SON	mlb[40D7]
U4300	COMPARATOR_LM393_SOI -HF	mlb[41A7 41A4]
U4600	SWI_TPS2561_SON	mlb[43C7]
U4601	SWI_TPS2561_SON	mlb[43D7]
U4650	PI3USB102_TQFN	mlb[43D4]
U4700	CY7C63833_QFN	mlb[44C5]
U4900	H8S2117RP_TLP-145V	mlb[46D3 46B7 46D7]
U5010	VREF_SN0903048_DFN	mlb[47D7]
U5300	INA210_SC70	mlb[50D7]
U5305	INA210_SC70	mlb[50C7]
U5340	OPAMP_OPA2333_DFN	mlb[50B3 50D3]
U5360	INA210_SC70	mlb[50B7]
U5365	INA210_SC70	mlb[50A7]
U5375	INA210_SC70	mlb[50C7]
U5400	INA210_SC70	mlb[51C7]
U5403	INA214_SC70	mlb[51D7]
U5500	EMC1428_QFN	mlb[52D6]
U5535	EMC1414_MSOP10_MSOP	mlb[52B6]
U5600	CS4206B_QFN	mlb[53D5]
U5601	MAX8840_UDFN	mlb[53A5]
U5800	AMP_MAX97220_TQFN	mlb[55C4]
U5900	AUDIO_MAX98300_WLP	mlb[56C5]
U6106	CD3282A1_WCSP	mlb[58D3]
U6400	FLASH_MX25L6406E_SOI C	mlb[59C5]
U6701	SLG5AP021_TDFN	mlb[61B7]
U6860	ISL88042_TDFN	mlb[62A7]
U7100	ISL95870A_UTQFN	mlb[64C5]
U7201	SC414_MLPQ	mlb[65D6]
U7251	IR3859MPBF_QFN	mlb[65B6]
U7300	TPS51916_QFN	mlb[66C6]
U7400	ISL6364_QFN	mlb[67C4]
U7501	ISL6620A_QFN	mlb[68D7]
U7521	ISL6609_QFN1	mlb[68C7]
U7601	ISL6620A_QFN	mlb[69C7]
U7700	ISL95870_UTQFN	mlb[70C6]
U7860	TPS54218_QFN	mlb[71D7]
U7870	LREG_TPS720XX_DRV_SO N	mlb[71B6]
U9000	T29_FCBGA	mlb[74D4]
U9000	T29_FCBGA	mlb[75D5]
U9090	EEPROM_M95320_MLP8_M LP	mlb[74C7]
U9200	SLG4AP016_TDFN	mlb[76C7]
U9210	TPS22924_CSP	mlb[76B7]
U9215	TPS22924_CSP	mlb[76A7]
U9216	TPS22924_CSP	mlb[76A7]
U9310	PS8301_A2_QFN	mlb[77C6]
U9330	LPC1112A_HVQFN25_HVQ FN25	mlb[77A6]
U9359	SN74LVC1G04_SC70	mlb[77C3]
U9390	CBTL04DP081_HVQFN	mlb[77B2]
U9401	ISL80101B_DFN	mlb[78D7]
U9410	SN1010017_QFN	mlb[78D2]
U9420	MC74VHC1G08_SC70-HF	mlb[78C7]
U9740	PS8171_QFN	mlb[79D4]
U9800	SWI_TPS2051B_SOT23	mlb[80D3]
XW0700	SHORT_SM	mlb[7D8]
XW0701	SHORT_SM	mlb[7C8]
XW4020	SHORT_SM	mlb[38C6]
XW4300	SHORT_SM	mlb[41D3]
XW4301	SHORT_SM	mlb[41D8]
XW4302	SHORT_SM	mlb[41D7]
XW4900	SHORT_SM	mlb[46C2]
XW5320	SHORT_SM	mlb[50C3]
XW5322	SHORT_SM	mlb[50A7]
XW5330	SHORT_SM	mlb[50B3]
XW5500	SHORT_SM	mlb[52C7]
XW5501	SHORT_SM	mlb[52C7]
XW5504	SHORT_SM	mlb[52C6]
XW5505	SHORT_SM	mlb[52C6]
XW5600	SHORT_SM	mlb[53A6]
XW5601	SHORT_SM	mlb[53A6]
XW5610	SHORT_SM	mlb[53D2]
XW5800	SHORT_SM	mlb[55B3]
XW6180	SHORT_SM	mlb[58B2]
XW7100	SHORT_SM	mlb[64B5]
XW7201	SHORT_SM	mlb[65C5]
XW7202	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[65C4]
XW7251	SHORT_SM	mlb[65A6]
XW7300	SHORT_SM	mlb[66B6]
XW7335	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[66B3]
XW7360	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[66C5]
XW7401	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[67C5]
XW7402	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[67A7]
XW7420	SHORT_SM	mlb[67D8]
XW7423	SHORT_SM	mlb[67A8]
XW7430	SHORT_SM	mlb[67D8]
XW7433	SHORT_SM	mlb[67A8]
XW7501	SHORT_SM	mlb[68D3]
XW7502	SHORT_SM	mlb[68D3]
XW7521	SHORT_SM	mlb[68C3]
XW7522	SHORT_SM	mlb[68C3]
XW7700	SHORT_SM	mlb[70B6]
XW7801	SHORT_SM	mlb[71C6]
Y2600	CRYSTAL_5X3.2X1.4-SM	mlb[25D7]
Y2650	CRYSTAL_5X3.2X1.4-SM	mlb[25B7]
Y2705	CRYSTAL_4PIN_SM-3.2X 2.5MM	mlb[26C7]
Y2810	CRYSTAL_4PIN_SM-2	mlb[27C6]
Y4190	OSC_4PIN_TSNC_SM	mlb[39C1]
Y5010	CRYSTAL_5X3.2-SM	mlb[47B7]
ZH0930	HOLE_VIA	mlb[9B8]
ZH0931	HOLE_VIA	mlb[9B8]
ZH0932	HOLE_VIA	mlb[9A8]
ZH0933	HOLE_VIA	mlb[9A8]
ZH0934	HOLE_VIA	mlb[9A8]
ZH0935	HOLE_VIA	mlb[9B8]
ZH0936	HOLE_VIA	mlb[9A8]
ZH0937	HOLE_VIA	mlb[9A8]
ZH0938	HOLE_VIA	mlb[9A8]
ZH0940	HOLE_VIA	mlb[9B7]
ZH0941	HOLE_VIA	mlb[9B7]
ZH0942	HOLE_VIA	mlb[9A7]
ZH0943	HOLE_VIA	mlb[9A7]
ZH0944	HOLE_VIA	mlb[9A7]
ZH0945	HOLE_VIA	mlb[9B7]
ZH0946	HOLE_VIA	mlb[9A7]
ZH0947	HOLE_VIA	mlb[9A7]
ZH0948	HOLE_VIA	mlb[9A7]
ZH0949	HOLE_VIA	mlb[9A7]
ZH0950	HOLE_VIA	mlb[9B7]
ZH0951	HOLE_VIA	mlb[9B7]
ZH0952	HOLE_VIA	mlb[9A7]
ZH0953	HOLE_VIA	mlb[9A7]
ZH0954	HOLE_VIA	mlb[9A7]

ZH0955	HOLE_VIA	mlb[9B6]
ZH0956	HOLE_VIA	mlb[9B6]
ZH0957	HOLE_VIA	mlb[9A6]
ZH0958	HOLE_VIA	mlb[9A6]
ZP0900	POGO_PIN_1P_SM	mlb[9D4]
ZP0901	POGO_PIN_1P_SM	mlb[9D4]
ZP0902	POGO_PIN_1P_SM	mlb[9D3]
ZP0903	POGO_PIN_1P_SM	mlb[9D3]
ZP0907	POGO_PIN_1P_SM	mlb[9D1]
ZP0920	POGO_PIN_1P_SM	mlb[9C3]
ZP0921	POGO_PIN_1P_SM	mlb[9C3]
ZP0922	POGO_PIN_1P_SM	mlb[9C2]
ZT0840	PCB_STANDOFF	mlb[8C1]
ZT0841	PCB_STANDOFF	mlb[8C1]
ZT0910	BOSS	mlb[9C8]
ZT0911	BOSS	mlb[9B8]
ZT0912	BOSS	mlb[9C7]
ZT0913	BOSS	mlb[9B7]
ZT0914	BOSS	mlb[9B8]
ZT0915	BOSS	mlb[9B7]
ZT0940	PCB_STANDOFF	mlb[9C8]
ZT0941	PCB_STANDOFF	mlb[9C6]
ZT0960	PCB_STANDOFF	mlb[9D8]
ZT0961	PCB_STANDOFF	mlb[9D6]
ZT0962	PCB_STANDOFF	mlb[9D8]
ZT0966	PCB_STANDOFF	mlb[9D7]
ZT0970	PCB_STANDOFF	mlb[9C3]