COMPAL CONFIDENTIAL

MODEL NAME : *VAW50*

PCB NO : *LA-A101P (DA8000WA000)*

BOM P/N :

GPIO MAP: 3.0

Alpine 15"

Haswell ULT

Gerber Date : 2013-08-22

REV : 1.0

@ : Nopop Component

1@ : M/B SPI ROM

TAA@ : TAA/B SPI ROM

CONN@ : Connector Component

DIS@ : Discrete Pop Component

UMA@ : UMA Pop Component

EMI@ : EMI Component

ESD@ : ESD Component

RF@ : RF Component

XDP@ : XDP Component

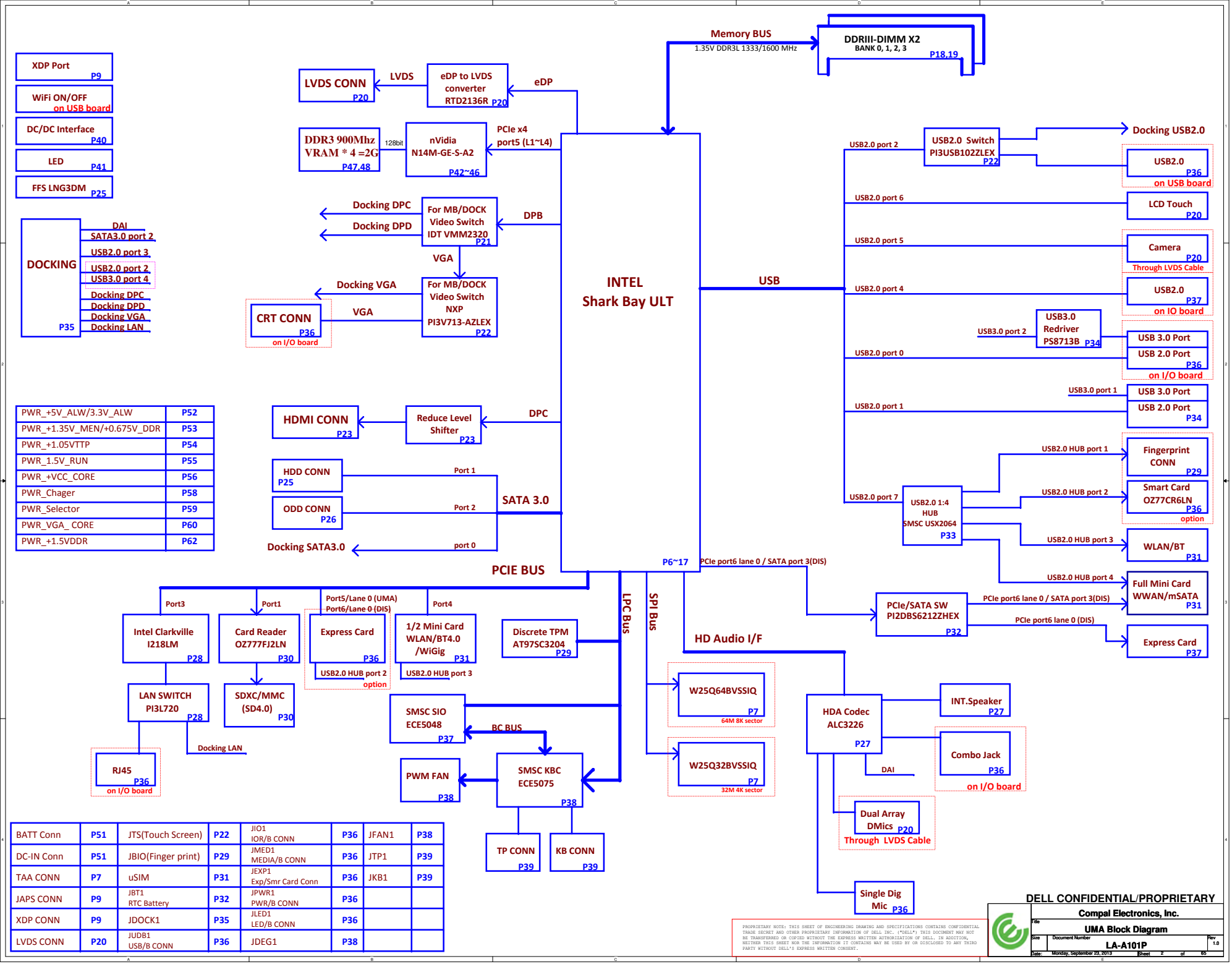
eTP@ : TS eTP Component

NeTP@ : TS non - eTP Component

: Short Pad

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: LA-A101P	Rev: 1.0
Date: Monday, September 23, 2013	Sheet 1 of 65	



BATT Conn	P51	JTS(Touch Screen)	P22	JIO1 IOR/B CONN	P36	JFAN1	P38
DC-IN Conn	P51	JBIO(Finger print)	P29	JMED1 MEDIA/B CONN	P36	JTP1	P39
TAA CONN	P7	uSIM	P31	JEXP1 Exp/Smr Card Conn	P36	JKB1	P39
JAPS CONN	P9	JBT1 RTC Battery	P32	JPWR1 PWR/B CONN	P36		
XDP CONN	P9	JDOCK1	P35	JLED1 LED/B CONN	P36		
LVDS CONN	P20	JUDB1 USB/B CONN	P36	JDEG1	P38		

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Title: UMA Block Diagram

Size: LA-A101P | Document Number | Rev 1.0

Date: Monday, September 23, 2013 | Sheet 2 of 65

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->MB-->LEFT
	USB3.0 2		USB3.0-->IOB-->Rear Right
PCIE 1	USB3.0 3		PCIE1-->MMI PCIE
PCIE 2	USB3.0 4		USB3.0-->Docking
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			GPU(DIS)/Express card(UMA)
PCIE 6		SATA 3	WWAN(mSATA)/Express card(PCIE)
		SATA 2	ODD
		SATA 1	HDD
		SATA 0	DOCK

	USB PORT#	DESTINATION
HSW ULT	0	Ext Port 1(I/O) RIGHT
	1	Ext Port 2 (MB/Debug Port) LEFT
	2	USB 2.0 Switch
	3	E-DOCK1
	4	Ext Port 4 (I/O) USB2.0
	5	Camera
	6	Touch Screen
	7	USB HUB

OC#	USB Port	DESTINATION
USB_OC0#	0	IOR/B USB3.0
USB_OC1#	1	M/B USB3.0
USB_OC2#	2 (USB Switch)	USB/B USB2.0
USB_OC3#	4	IOR/B USB 2.0

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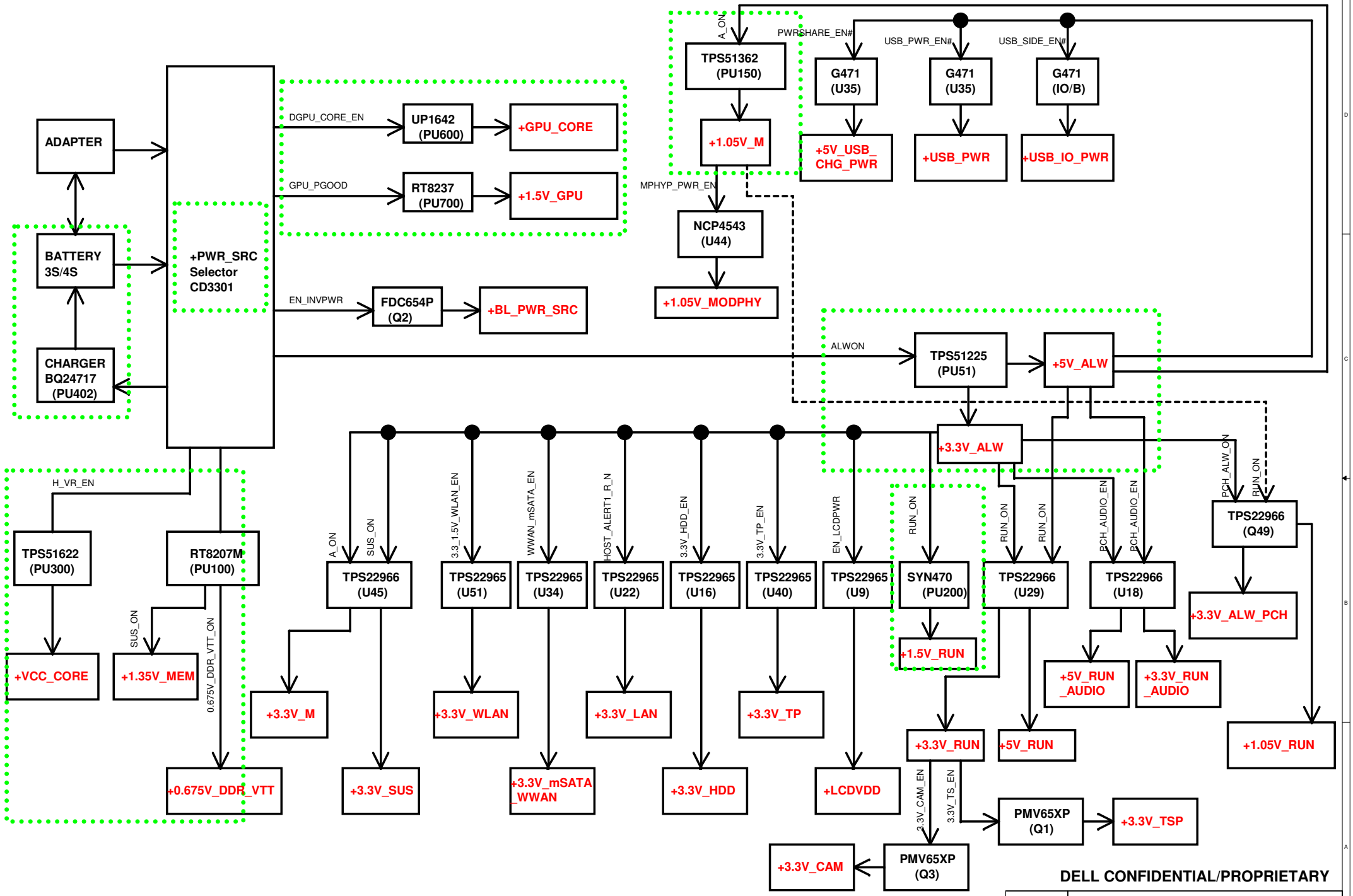
Title: Index and Config.

Size | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 3 of 65



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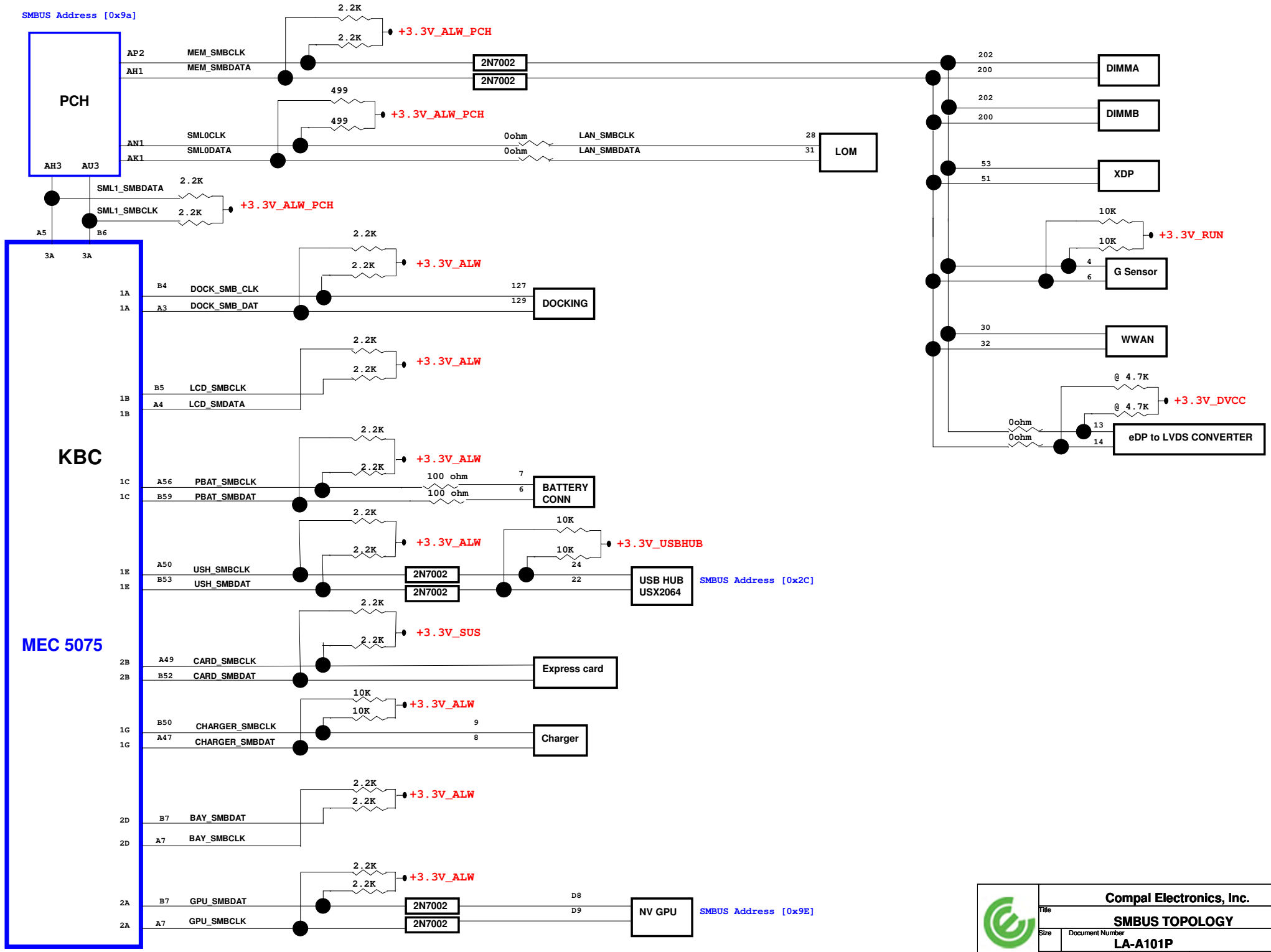
Title: Power Rail

Size: | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 4 of 65



Compal Electronics, Inc.	
Title	SMBUS TOPOLOGY
Size	Document Number: LA-A101P
Rev	1.0
Date:	Monday, September 23, 2013
Sheet	5 of 65

+RTC_CELL

330K_0402_1%~D RC1

PCH_INTVRMEN

330K_0402_1%~D @ RC2

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3.3V_ALW_PCH

@ RC3 1K_0402_1%~D PCH_AZ_SDOUT

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

+1.05V_M

RC16 0_0603_5% @

+1.05V_M_JTAG

RC17 51_0402_1%~D PCH_JTAG_TDI

RC18 51_0402_1%~D PCH_JTAG_TDO

RC20 51_0402_1%~D PCH_JTAG_TMS

@ RC10 1K_0402_1%~D PCH_JTAG_JTAGX

@ RC22 51_0402_1%~D PCH_JTAG_TCK

reference 479493 figure 7-1

CC1 15P_0402_50V8J

PCH_RTCX1_R — RC4 0_0402_5% — PCH_RTCX1

YC1 32.768KHZ_12.5PF_Q13FC1350000~D

RC5 10M_0402_5%~D

CC2 15P_0402_50V8J

PCH_RTCX2

+RTC_CELL

RC7 1M_0402_5%~D

RC8 20K_0402_5%~D

RC6 20K_0402_5%~D

INTRUDER#

PCH_INTVRMEN

SRTCRST#

PCH_RTCRST#

[9] PCH_RTCRST#

@ ME1 SHORT PADS~D

CC3 1U_0402_6.3V6K~D

@ CMOS1 SHORT PADS~D

CC4 1U_0402_6.3V6K~D

CMOS place near DIMM

UC1E HASWELL_MCP_E

RTCX1
RTCX2
INTRUDER
INTVRMEN
SRTCRST
RTCRST

RTC

PCH_AZ_BITCLK
PCH_AZ_SYNC
PCH_AZ_RST#
PCH_AZ_CODEC_SDIN0

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST/I2S_MCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN/I2S1_TXD
HDA_DOCK_RST/I2S1_SFRM
I2S1_SCLK

AUDIO

[27] PCH_AZ_CODEC_SDIN0

[37] ME_FWP — RC9 1K_0402_1%~D — PCH_AZ_SDOUT

SATA

[9] PCH_JTAG_TRST# — PCH_JTAG_TRST#
[9] PCH_JTAG_TCK — PCH_JTAG_TCK
[9] PCH_JTAG_TDI — PCH_JTAG_TDI
[9] PCH_JTAG_TDO — PCH_JTAG_TDO
[9] PCH_JTAG_TMS — PCH_JTAG_TMS
[9] PCH_JTAG_JTAGX — PCH_JTAG_JTAGX

PCH_TRST
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
RSVD
RSVD
JTAGX
RSVD

JTAG

5 OF 19

Rev1p2

SATA_RN0/PERN6_L3 — J5 — SATA_PRX_DKTX_N0_C [35]
SATA_RP0/PERP6_L3 — H5 — SATA_PRX_DKTX_P0_C [35]
SATA_TN0/PETN6_L3 — B15 — SATA_PTX_DKRX_N0_C [35]
SATA_TP0/PETP6_L3 — A15 — SATA_PTX_DKRX_P0_C [35]

DOCK

SATA_RN1/PERN6_L2 — J8 — SATA_PRX_DTX_N1_C [25]
SATA_RP1/PERP6_L2 — H8 — SATA_PRX_DTX_P1_C [25]
SATA_TN1/PETN6_L2 — A17 — SATA_PTX_DRX_N1_C [25]
SATA_TP1/PETP6_L2 — B17 — SATA_PTX_DRX_P1_C [25]

SATA HDD

SATA_RN2/PERN6_L1 — J6 — SATA_ODD_PRX_DTX_N2_C [26]
SATA_RP2/PERP6_L1 — H6 — SATA_ODD_PRX_DTX_P2_C [26]
SATA_TN2/PETN6_L1 — B14 — SATA_ODD_PTX_DRX_N2_C [26]
SATA_TP2/PETP6_L1 — C15 — SATA_ODD_PTX_DRX_P2_C [26]

ODD

PCH Rx side need use strap pin to update PCIE +/-

SATA_RN3/PERN6_L0 — F5 — EXP_PRX_EXPTX_N6 — EXP_PRX_EXPTX_N6 [32]
SATA_RP3/PERP6_L0 — E5 — EXP_PRX_EXPTX_P6 — EXP_PRX_EXPTX_P6 [32]
SATA_TN3/PETN6_L0 — C17 — EXP_PTX_EXPRX_N6 — EXP_PTX_EXPRX_N6 [32]
SATA_TP3/PETP6_L0 — D17 — EXP_PTX_EXPRX_P6 — EXP_PTX_EXPRX_P6 [32]

Express card/mSATA

SATA0GP/GPIO34 — V1 — MPCIE_RST# — MPCIE_RST# [31]
SATA1GP/GPIO35 — U1 — HDD_DET# — HDD_DET# [25]
SATA2GP/GPIO36 — V6 — PCH_GPIO36 — PCH_GPIO36 [12]
SATA3GP/GPIO37 — AC1 — MCARD_PCIE_MSATA# — MCARD_PCIE_MSATA# [37]

SATA_IREF — A12 — SATA_IREF — 2 — @ — 1 — RC14 0_0402_5% — PCH_ASATA3PLL

RSVD — L11
RSVD — K10
RSVD — C12
SATA_RCOMP — U3 — SATA_COMP
SATALED — SATA_ACT# — SATA_ACT# [41]

+3.3V_RUN

HDD_DET# — RC11 100K_0402_5%~D

MPCIE_RST# — RC138 10K_0402_5%~D

MCARD_PCIE_MSATA# — RC12 10K_0402_5%~D

Shark_Bay_ULT_PDG 0.9:
the sampled value for the GPIO corresponding to the particular port during boot time.
SATA3GP/GPIO37-->SATAP3:
1:SATA
0:PCIe

SATA_IREF

SATA_IREF min 4mil trace at break-out and 12-15mil trace with <0.2 ohms and length total <= 500mils. Requires 12 mils isolation from all High Speed IO and clocks.

SATA Impedance Compensation

+PCH_ASATA3PLL

SATA_COMP — RC19 3.01K_0402_1%~D

SATA_RCOMP min 4mil trace at break-out and 12-15mil trace with <0.2 ohms and length total <= 500mils. Requires 12 mils isolation from all High Speed IO and clocks.

reference FFRD sch 0.5

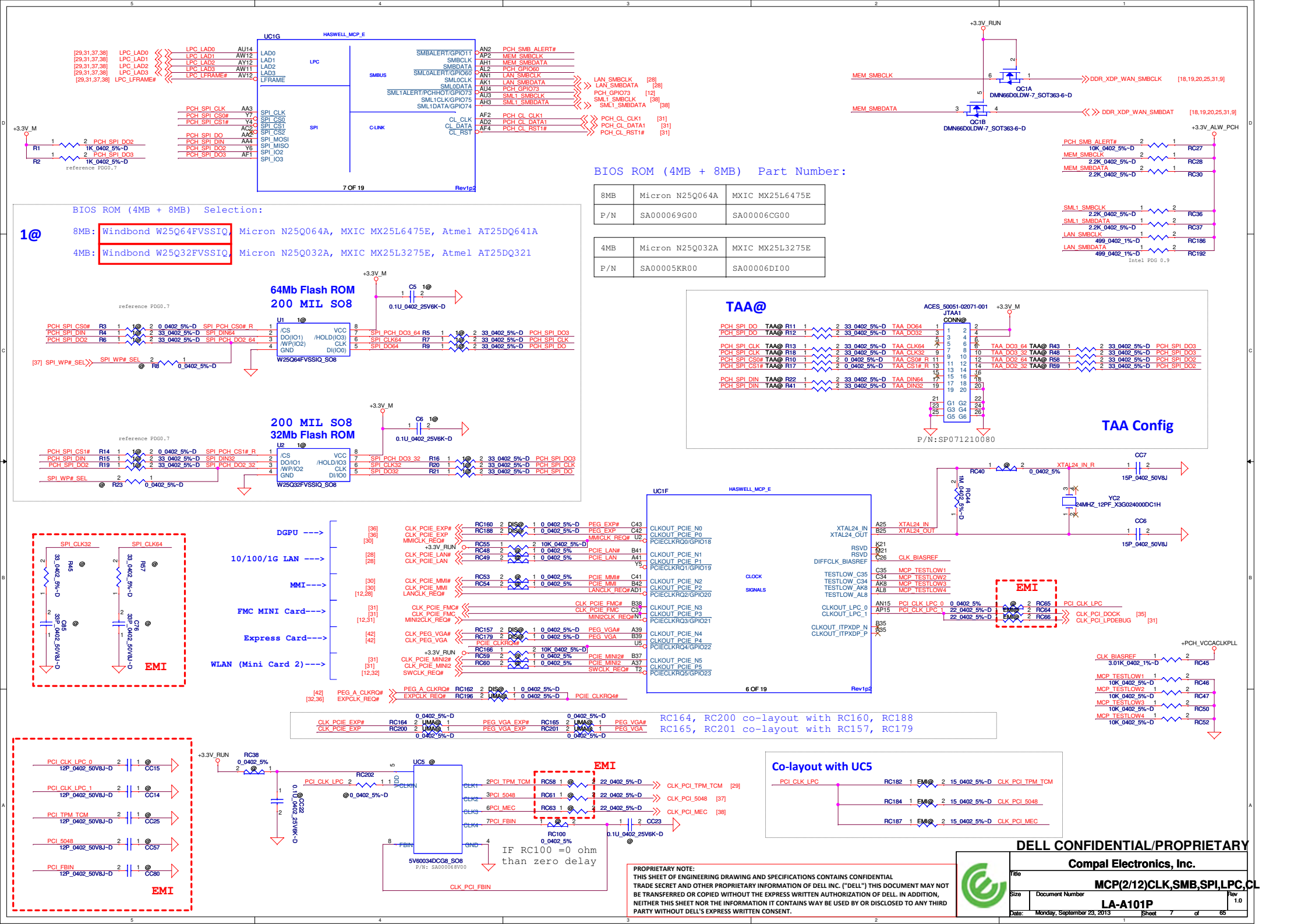
HDA for Codec

[27] PCH_AZ_CODEC_SDOUT — RC23 33_0402_5%~D — PCH_AZ_SDOUT
[27] PCH_AZ_CODEC_SYNC — RC24 33_0402_5%~D — PCH_AZ_SYNC
[27] PCH_AZ_CODEC_RST# — RC25 33_0402_5%~D — PCH_AZ_RST#
[27] PCH_AZ_CODEC_BITCLK — RC26 33_0402_5%~D — PCH_AZ_BITCLK

@ C25 27P_0402_50N8J~D

EMI

Compal Electronics, Inc.
Title: MCP(1/12) RTC,SATA,HDA,JTAG
Size: — Document Number: LA-A101P — Rev: 1.0
Date: Monday, September 23, 2013 Sheet 6 of 65


UC1G
HASWELL_MCP_E
LPC
SMBUS
SPI
C-LINK
7 OF 19
Rev1p2
BIOS ROM (4MB + 8MB) Selection:
1@
8MB: Windbond W25Q64FVSSIQ, Micron N25Q064A, MXIC MX25L6475E, Atmel AT25DQ641A
4MB: Windbond W25Q32FVSSIQ, Micron N25Q032A, MXIC MX25L3275E, Atmel AT25DQ321
BIOS ROM (4MB + 8MB) Part Number:
8MB | Micron N25Q064A | MXIC MX25L6475E
P/N | SA000069G00 | SA00006CG00
4MB | Micron N25Q032A | MXIC MX25L3275E
P/N | SA00005KR00 | SA00006DI00
64Mb Flash ROM
200 MIL SO8
W25Q64FVSSIQ_SO8
200 MIL SO8
32Mb Flash ROM
W25Q32FVSSIQ_SO8
TAA@
TAA Config
P/N:SP071210080
UC1F
HASWELL_MCP_E
CLOCK SIGNALS
6 OF 19
Rev1p2
DGPU --->
10/100/1G LAN --->
MMI--->
FMC MINI Card--->
Express Card--->
WLAN (Mini Card 2)--->
EMI
RC164, RC200 co-layout with RC160, RC188
RC165, RC201 co-layout with RC157, RC179
Co-layout with UC5
UC5
5V60034DCG8_SO8
IF RC100 =0 ohm
than zero delay
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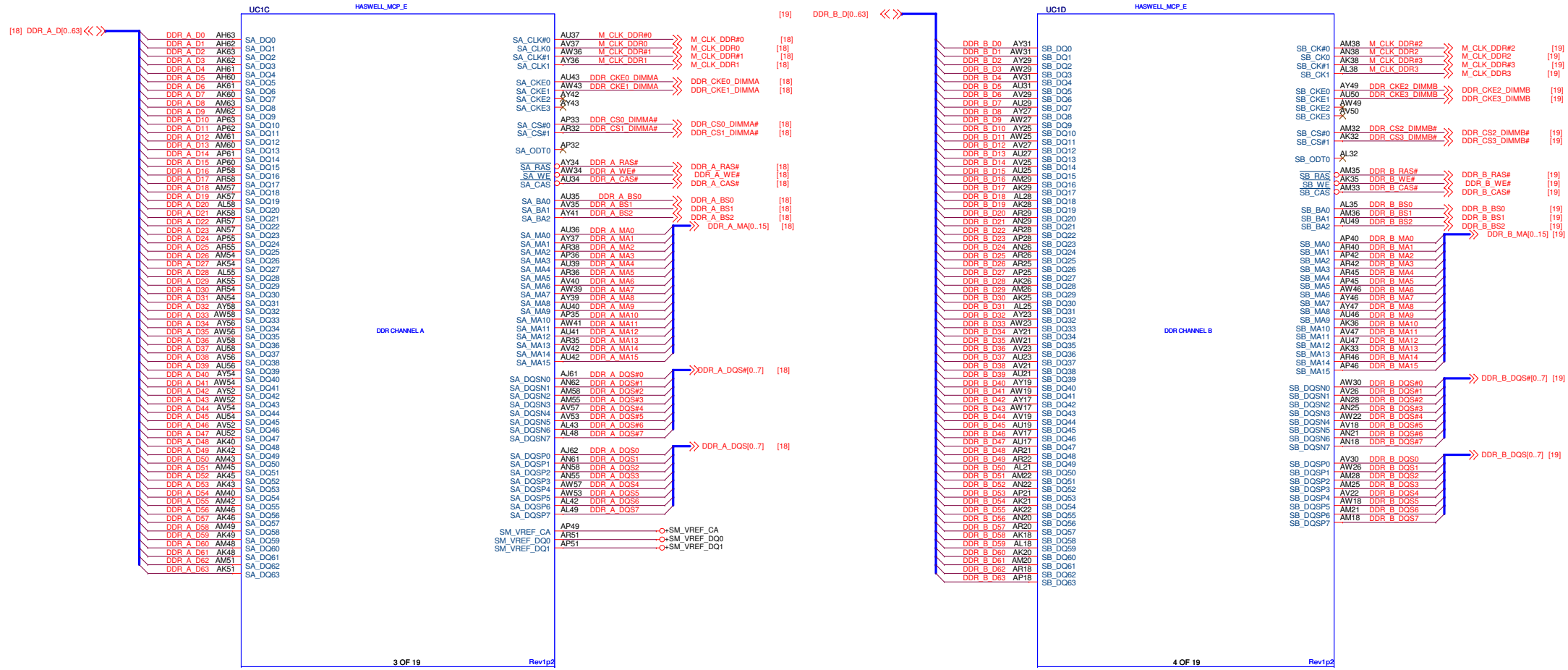
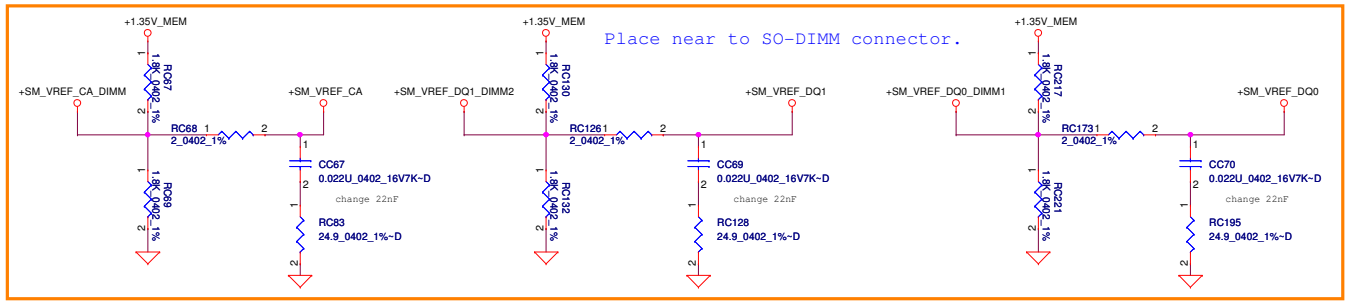
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
MCP(2/12)CLK,SMB,SPI,LPC,CL
Size
Document Number
LA-A101P
Rev
1.0
Date: Monday, September 23, 2013
Sheet 7 of 65





Refer to Intel request PDG1.0 P148

Compal Electronics, Inc.

Title: Cover Page

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Date: Monday, September 23, 2013 | Sheet 8 of 65

DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86,R319,RC267	RC79,RC82,RC265
Depop	RC79,RC82,RC265	RC86,R319,RC267

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

DDR3 COMPENSATION SIGNALS

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

Place near JXDP1

Place near JXDP1.47

Place near JXDP1.48

X-Build Change

X-Build Change

EMI

PU/PD for JTAG signals

Compal Electronics, Inc.

Title: MCP(4/12) PM, JTAG,MISC

Size: | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 9 of 65

Intel check list has updated correctly

DP HUB <-----

HDMI<-----

UC1A — HASWELL_MCP_E — DDI / EDP — 1 OF 19 — Rev1p2

[21]	DDI1_LANE_N0	DDI1_LANE_N0	C54	DDI1_TXN0	EDP_TXN0	C45	EDP_CPU_LANE_N0
[21]	DDI1_LANE_P0	DDI1_LANE_P0	C55	DDI1_TXP0	EDP_TXP0	B46	EDP_CPU_LANE_P0
[21]	DDI1_LANE_N1	DDI1_LANE_N1	B58	DDI1_TXN1	EDP_TXN1	A47	EDP_CPU_LANE_N1
[21]	DDI1_LANE_P1	DDI1_LANE_P1	C58	DDI1_TXP1	EDP_TXP1	B47	EDP_CPU_LANE_P1
[21]	DDI1_LANE_N2	DDI1_LANE_N2	B55	DDI1_TXN2			
[21]	DDI1_LANE_P2	DDI1_LANE_P2	A55	DDI1_TXP2	EDP_TXN2	C47	
[21]	DDI1_LANE_N3	DDI1_LANE_N3	A57	DDI1_TXN3	EDP_TXP2	C46	
[21]	DDI1_LANE_P3	DDI1_LANE_P3	B57	DDI1_TXP3	EDP_TXN3	A49	
					EDP_TXP3	B49	
[23]	TMDS_N2	TMDS_N2	C51	DDI2_TXN0			
[23]	TMDS_P2	TMDS_P2	C50	DDI2_TXP0	EDP_AUXN	A45	EDP_CPU_AUX#
[23]	TMDS_N1	TMDS_N1	C53	DDI2_TXN1	EDP_AUXP	B45	EDP_CPU_AUX
[23]	TMDS_P1	TMDS_P1	B54	DDI2_TXP1			
[23]	TMDS_N0	TMDS_N0	C49	DDI2_TXN2	EDP_RCOMP	D20	EDP_COMP
[23]	TMDS_P0	TMDS_P0	B50	DDI2_TXP2	EDP_DISP_UTIL	A43	
[23]	TMDS_CLK#	TMDS_CLK#	A53	DDI2_TXN3			
[23]	TMDS_CLK	TMDS_CLK	B53	DDI2_TXP3			

COMPENSATION PU FOR eDP

follow intel feedback

+VCCIOA_OUT

EDP_COMP — 24.9_0402_1%~D — RC134

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

+3.3V_RUN

RC137	ODD_DA#	100K_0402_5%~D
RC140	TOUCHPAD_INTR#	10K_0402_5%~D
RC146	PIRQ#_TPM	10K_0402_5%~D
RC148	PIRQD	10K_0402_5%~D

reference 0.55 design chane log WW23_2

UC1I — HASWELL_MCP_E — eDP SIDEBAND / DISPLAY / GPIO — 9 OF 19 — Rev1p2

[20]	EDP_BIA_PWM	EDP_BIA_PWM	B8	EDP_BKLCTL	DDPB_CTRLCLK	B9	CPU_DPB_CTRLCLK
[20]	PANEL_BKLEN	PANEL_BKLEN	A9	EDP_BKLEN	DDPB_CTRLDATA	C9	CPU_DPB_CTRLDAT
[20,37]	ENVDD_PCH	ENVDD_PCH	C6	EDP_VDDEN	DDPC_CTRLCLK	D9	TMDS_DDC_SCL
					DDPC_CTRLDATA	D11	TMDS_DDC_SDA
[26]	ODD_DA#	ODD_DA#	U6				
[12,37,60,62]	DGPU_PWROK	DGPU_PWROK	P4	PIRQA/GPIO77	DDPB_AUXN	C5	CPU_DPB_AUX#
		PIRQ#_TPM	N4	PIRQB/GPIO78	DDPB_AUXP	B5	CPU_DPB_AUX
[12,25] HDD_FALL_INT	0_0402_5%~D	R73		PIRQC/GPIO79	DDPC_AUXN	B6	CPU_DPC_AUX#
	0_0402_5%~D	R75	PIRQD	N2	DDPC_AUXP	A6	CPU_DPC_AUX
			AD3	PIRQD/GPIO80			
				PME			
		TOUCHPAD_INTR#	U7		DDPB_HPD	C8	DPB_HPD
[12]	TOUCH_RST_N_GYRO_INT1	TOUCH_RST_N_GYRO_INT1	L1	GPIO55	DDPC_HPD	A8	TMDS_HPD
[49]	DGPU_PWR_EN	DGPU_PWR_EN	L3	GPIO52	EDP_HPD	D6	EDP_CPU_HPD
[60]	DGPU_CORE_EN	DGPU_CORE_EN	R5	GPIO54			
	CODEC_IRQ	CODEC_IRQ	L4	GPIO51			
				GPIO53			

RC152	ENVDD_PCH	100K_0402_5%~D
RC154	CODEC_IRQ	1K_0402_1%~D
RC306	DGPU_PWR_EN	10K_0402_5%~D
RC305	DGPU_CORE_EN	10K_0402_5%~D

DDPB_HPD / DDPC_HPD / EDP_HPD — 100K_0402_5%~D — RC158

reference PDG 0.9

Intel WW18 Strapping option

Intel WW18 Strapping option

+3.3V_RUN

RP1 2.2K_0804_8P4R_5%

CPU_DPB_CTRLCLK	8	1
CPU_DPB_CTRLDAT	7	2
TMDS_DDC_SCL	6	3
TMDS_DDC_SDA	5	4

CPU_DPB_AUX#	100K_0402_5%~D	RC147
CPU_DPC_AUX#	100K_0402_5%~D	RC149

DPB_HPD	100K_0402_5%~D	RC156
CPU_DPB_AUX	100K_0402_5%~D	RC153
CPU_DPC_AUX	100K_0402_5%~D	RC155

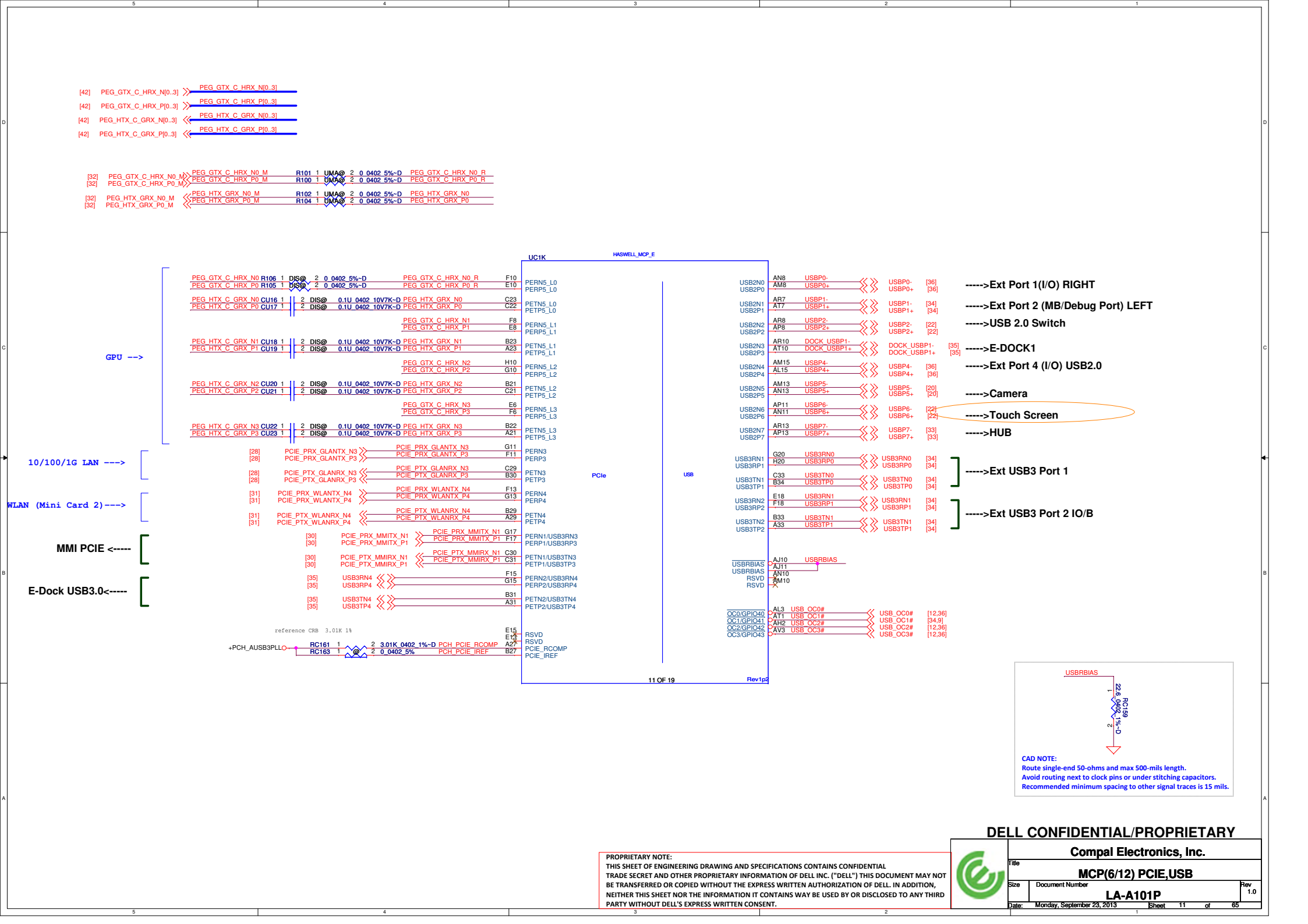
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: MCP(5/12) DDI,EDP,GPIO

Size: | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 10 of 65



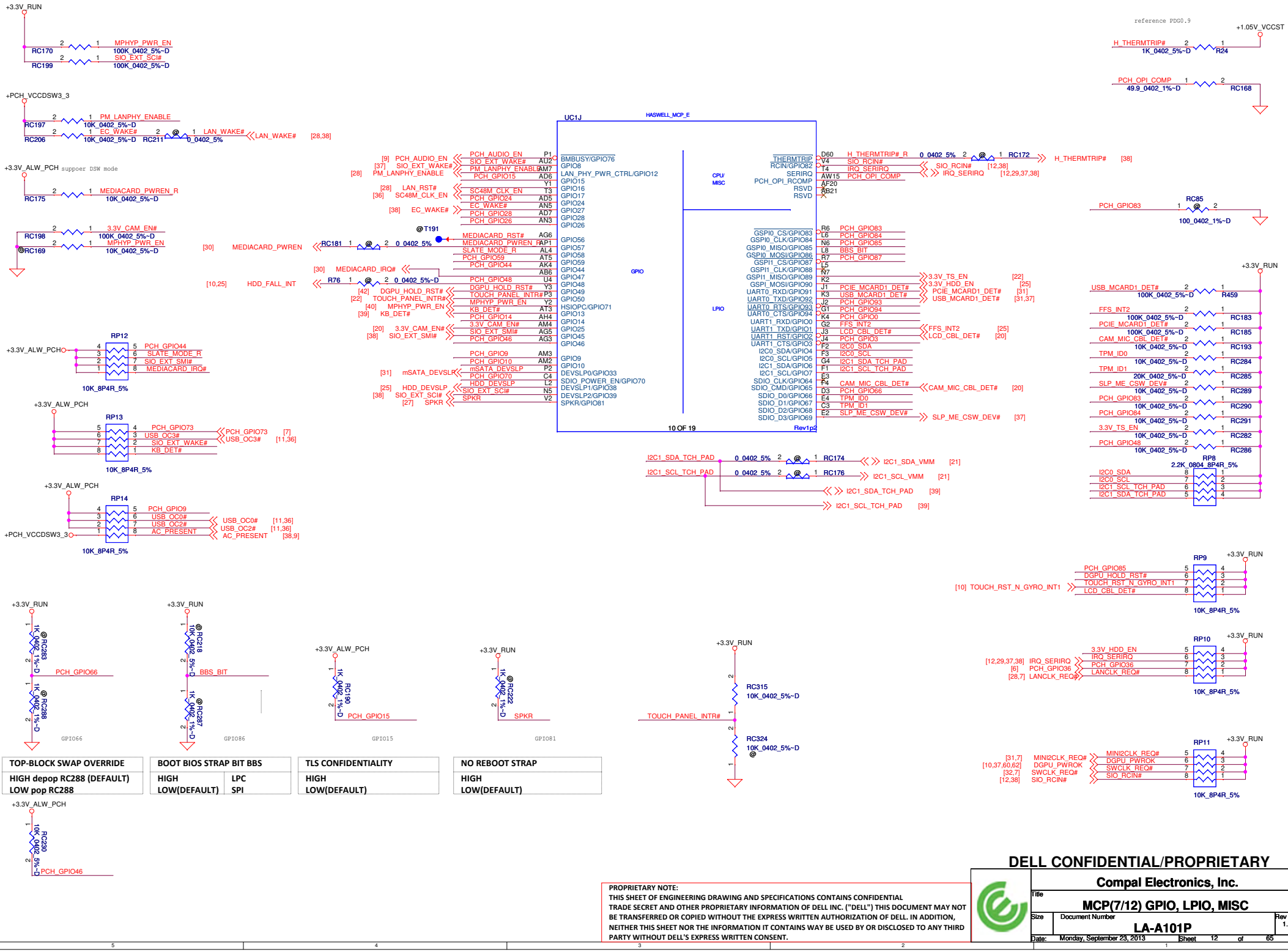
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: MCP(6/12) PCIE,USB

Size: | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 11 of 65



TOP-BLOCK SWAP OVERRIDE
HIGH depop RC288 (DEFAULT)
LOW pop RC288

BOOT BIOS STRAP BIT BBS	
HIGH	LPC
LOW(DEFAULT)	SPI

TLS CONFIDENTIALITY
HIGH
LOW(DEFAULT)

NO REBOOT STRAP
HIGH
LOW(DEFAULT)

Compal Electronics, Inc.

Title: MCP(7/12) GPIO, LPIO, MISC

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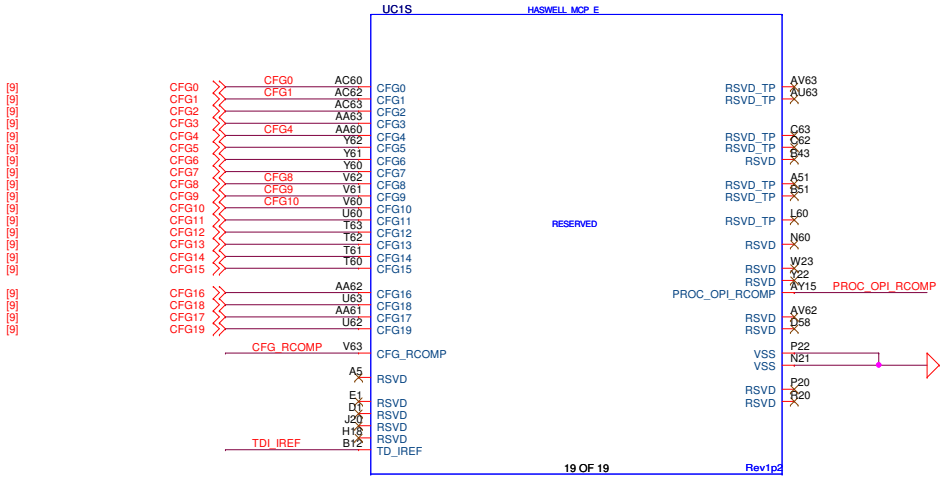
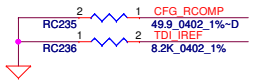
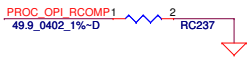
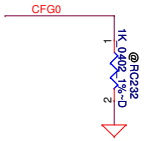
CFG STRAPS for CPU

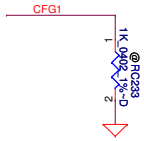




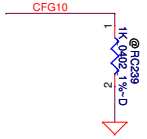


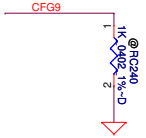


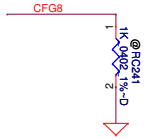
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

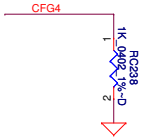


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: MCP(8/12) CFG, RSVD

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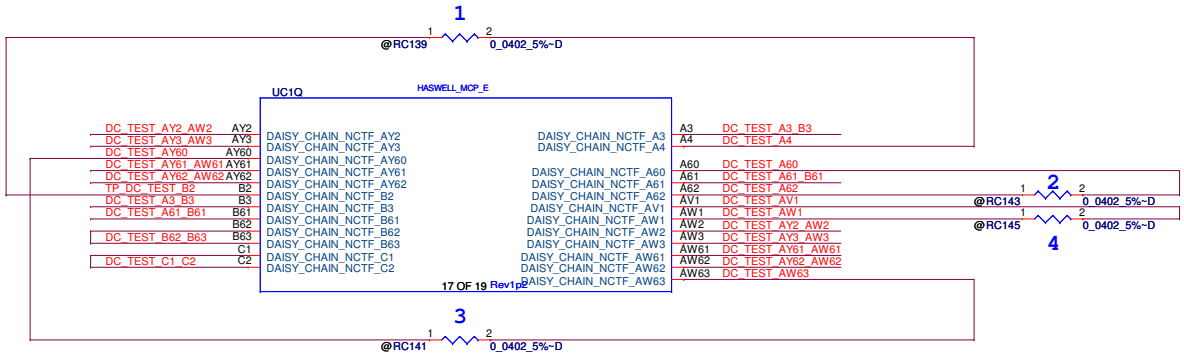
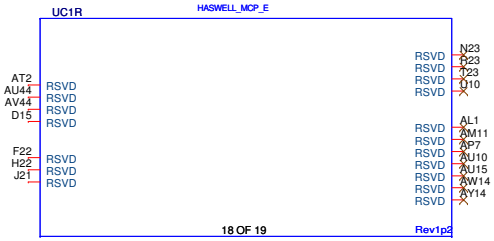


Package Daisy Chain:

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

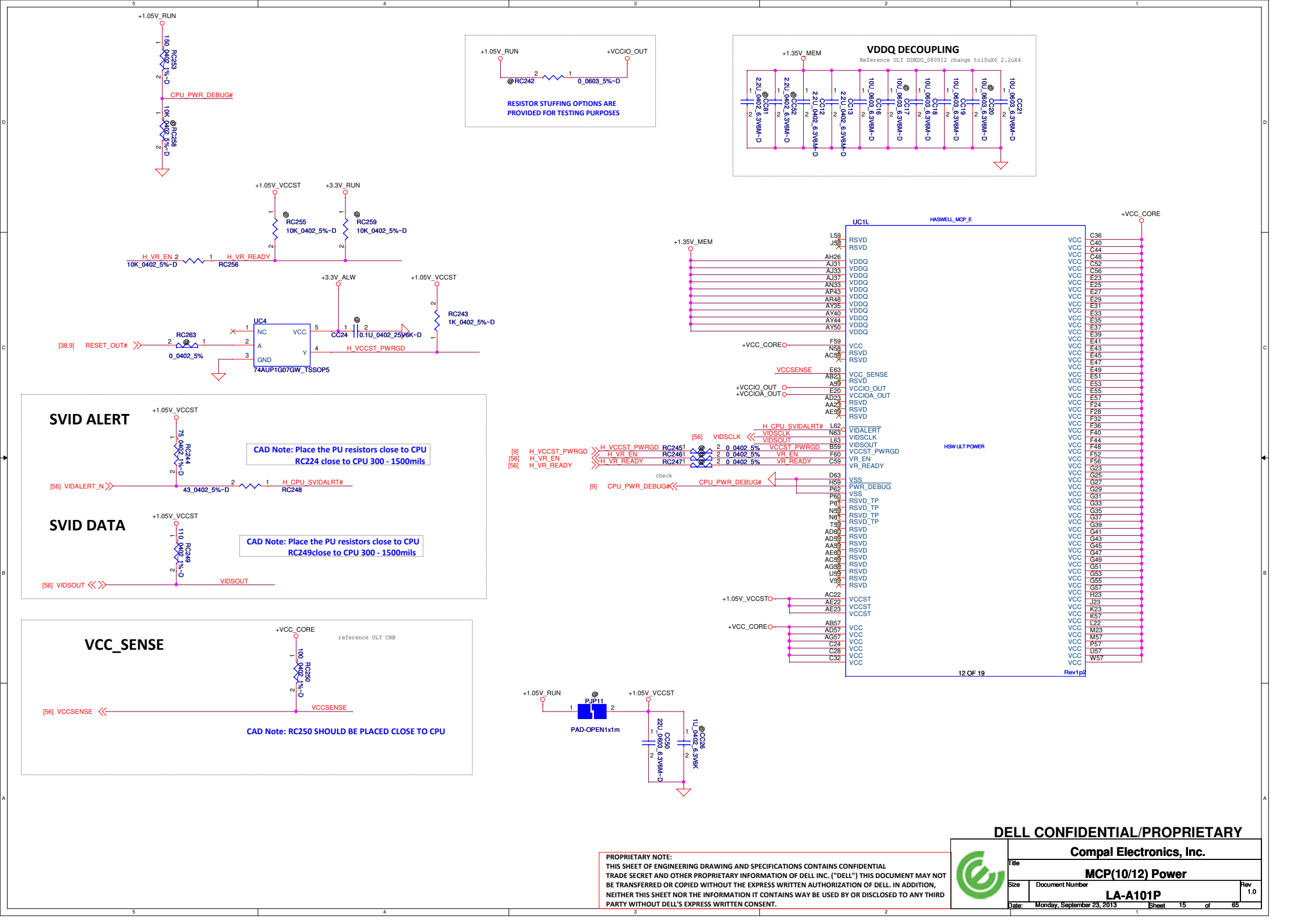


Compal Electronics, Inc.

Title: MCP(9/12) TP,RSVD

Size | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 14 of 65



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Compal Electronics, Inc.

Title: MCP(10/12) Power

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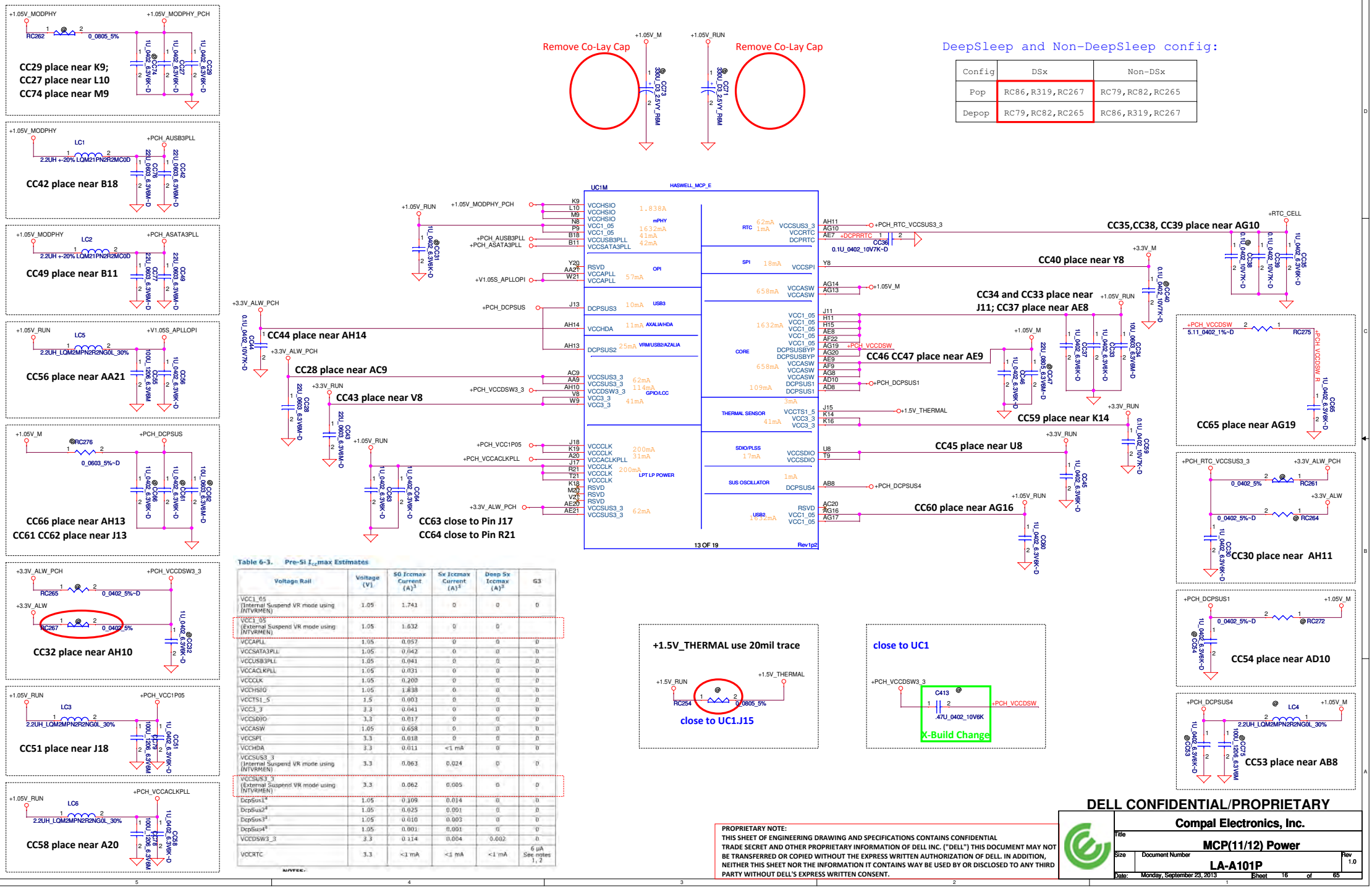
Date: Monday, September 23, 2013 | Sheet 15 of 65


CC29 place near K9;
CC27 place near L10
CC74 place near M9
CC42 place near B18
CC49 place near B11
CC56 place near AA21
CC66 place near AH13
CC61 CC62 place near J13
CC32 place near AH10
CC51 place near J18
CC58 place near A20
Remove Co-Lay Cap
Remove Co-Lay Cap
DeepSleep and Non-DeepSleep config:
Config | DSx | Non-DSx
Pop | RC86,R319,RC267 | RC79,RC82,RC265
Depop | RC79,RC82,RC265 | RC86,R319,RC267
CC44 place near AH14
CC28 place near AC9
CC43 place near V8
CC63 close to Pin J17
CC64 close to Pin R21
CC35,CC38, CC39 place near AG10
CC40 place near Y8
CC34 and CC33 place near J11; CC37 place near AE8
CC46 CC47 place near AE9
CC59 place near K14
CC45 place near U8
CC60 place near AG16
CC65 place near AG19
CC30 place near AH11
CC54 place near AD10
CC53 place near AB8
+1.5V_THERMAL use 20mil trace
close to UC1.J15
close to UC1
X-Build Change
Table 6-3. Pre-Si Iccmax Estimates
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Compal Electronics, Inc.
Title
MCP(11/12) Power
Size
Document Number
LA-A101P
Rev
1.0
Date: Monday, September 23, 2013
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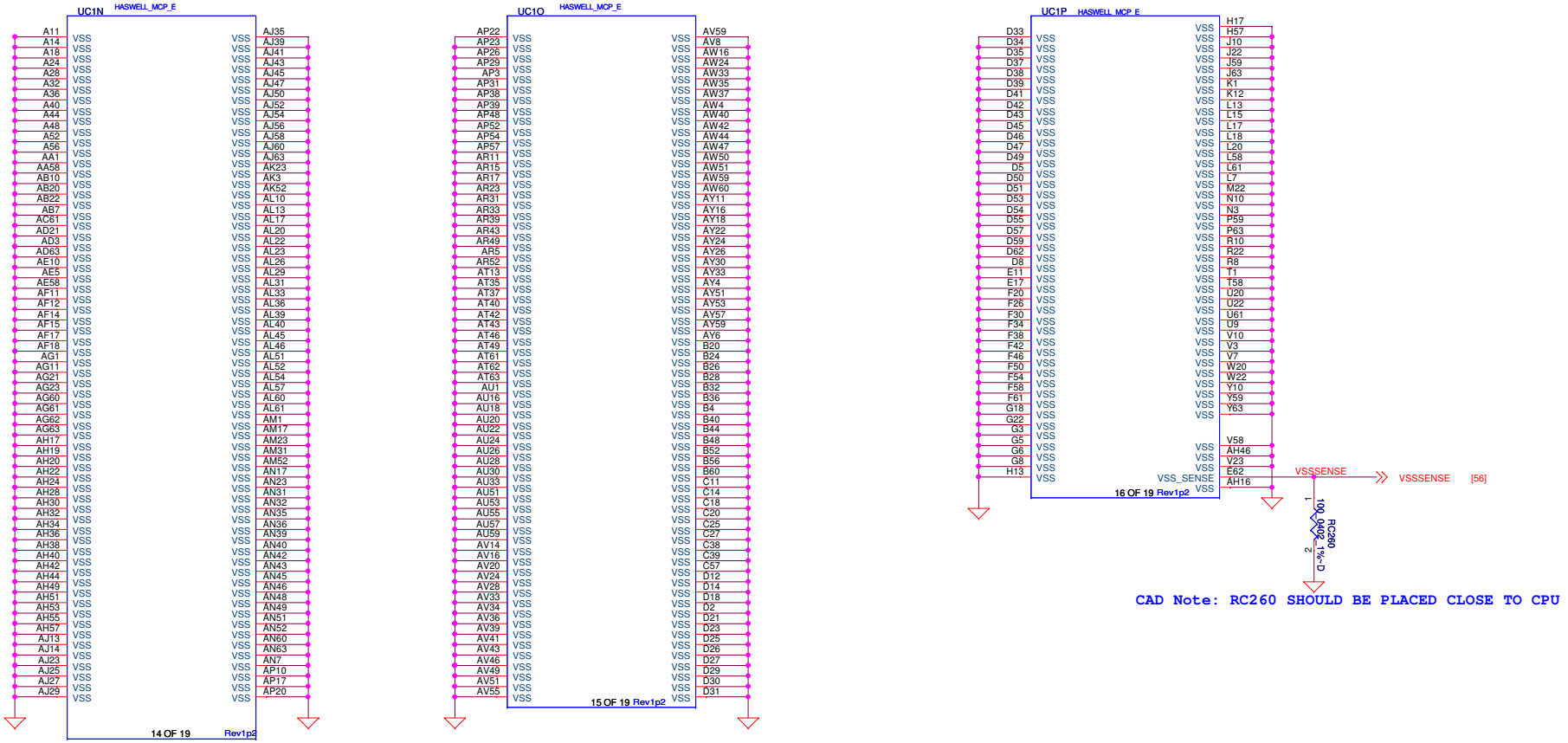

Compal Electronics, Inc.

Title: MCP(12/12) VSS

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2-3A to 1 DIMMs/channel

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM1.203,204

X-Build Change

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Document Number: LA-A101P Rev: 1.0

Date: Monday, September 23, 2013 Sheet 18 of 65

2-3A to 1 DIMMs/channel

All VREF traces should have 10 mil trace width

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

X-Build Change

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size: | Document Number: LA-A101P | Rev: 1.0

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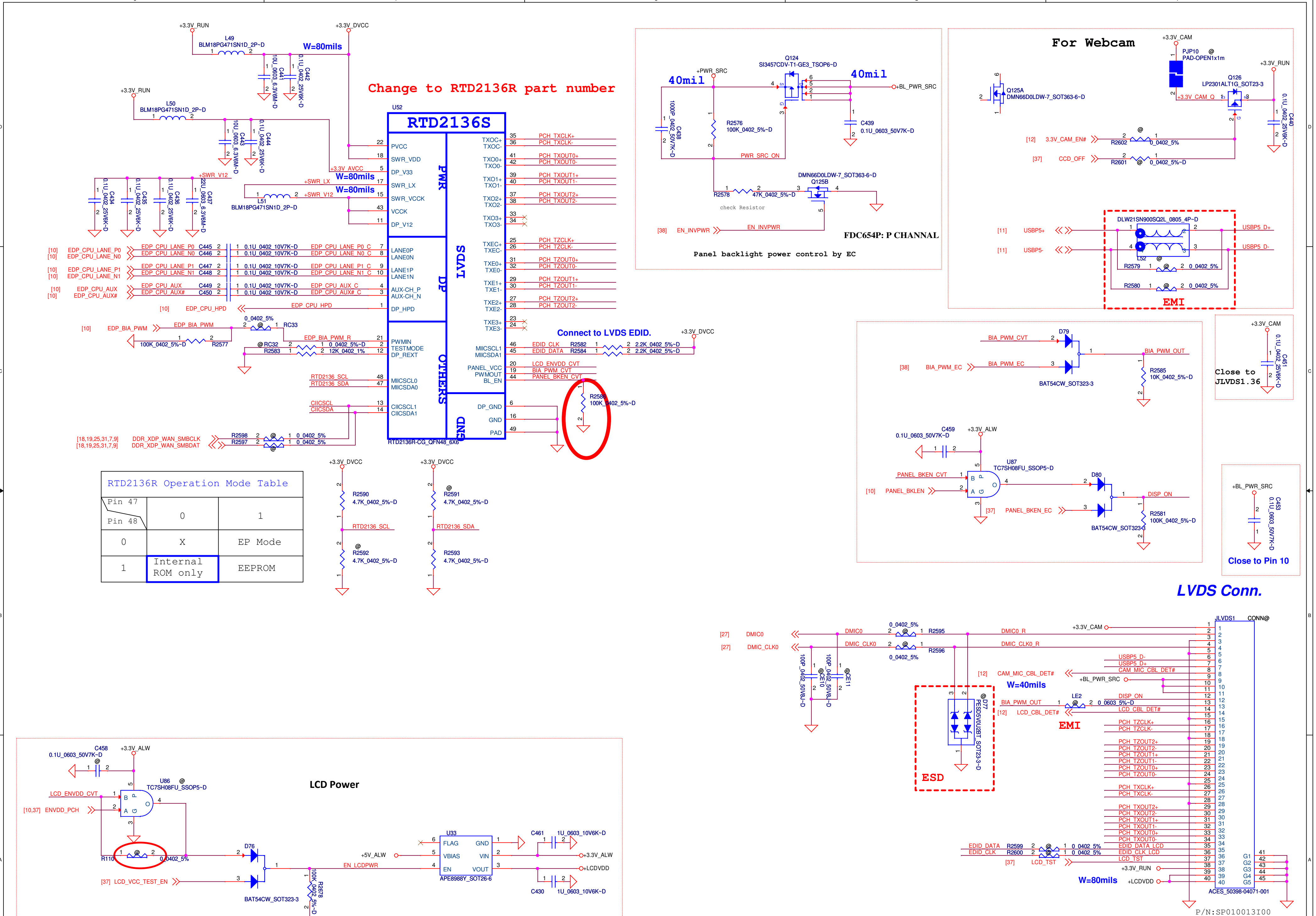


Change to RTD2136R part number
RTD2136S
U52
RTD2136R-CG_QFN48_6X6
PWR
LVDS
DP
OTHERS
GND
W=80mils
40mil
Q124
SI3457CDV-T1-GE3_TSOP6~D
Q125B
DMN66D0LDW-7_SOT363-6~D
check Resistor
FDC654P: P CHANNAL
Panel backlight power control by EC
For Webcam
PJP10
PAD-OPEN1x1m
Q125A
DMN66D0LDW-7_SOT363-6~D
Q126
LP2301ALT1G_SOT23-3
DLW21SN900SQ2L_0805_4P~D
EMI
Connect to LVDS EDID.
BAT54CW_SOT323-3
Close to JLVDS1.36
U87
TC7SH08FU_SSOP5~D
Close to Pin 10
LVDS Conn.
JLVDS1
CONN@
ACES_50398-04071-001
W=40mils
ESD
PESD5V0U2BT_SOT23-3~D
U86
TC7SH08FU_SSOP5~D
LCD Power
U33
APE8988Y_SOT26-6
D76
BAT54CW_SOT323-3
P/N:SP010013I00

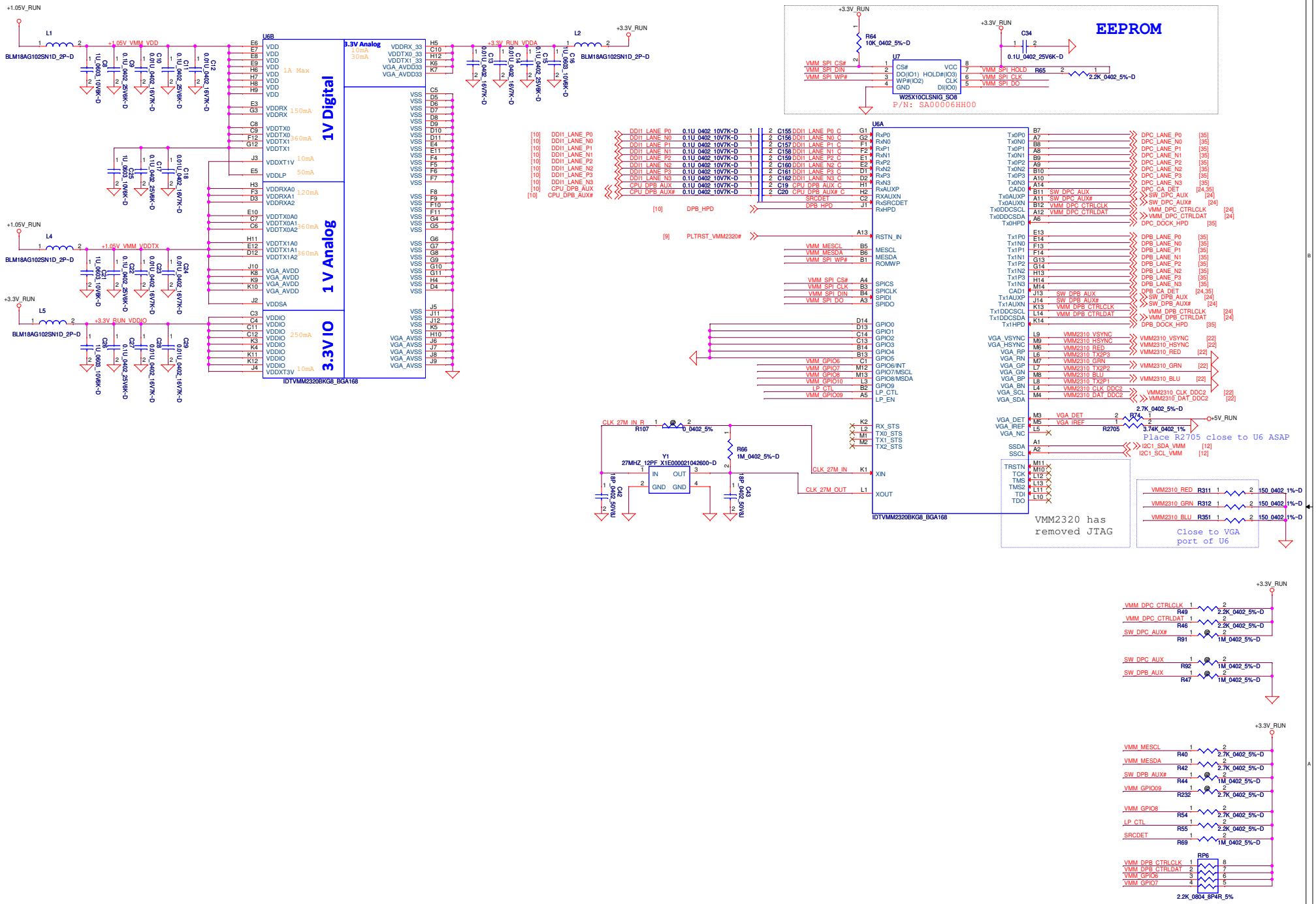
RTD2136R Operation Mode Table

Pin 47 / Pin 48	0	1
0	X	EP Mode
1	Internal ROM only	EEPROM

Compal Electronics, Inc.

Title: **eDP to LVDS**

Size | Document Number | Rev 1.0



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Title	IDT VMM2320 DP and VGA SW
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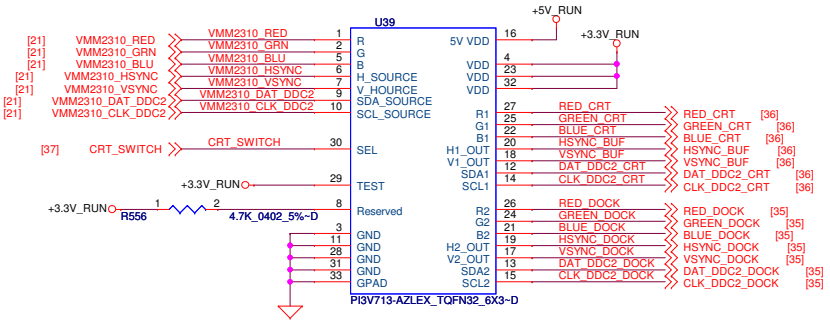
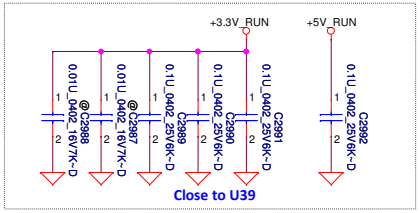
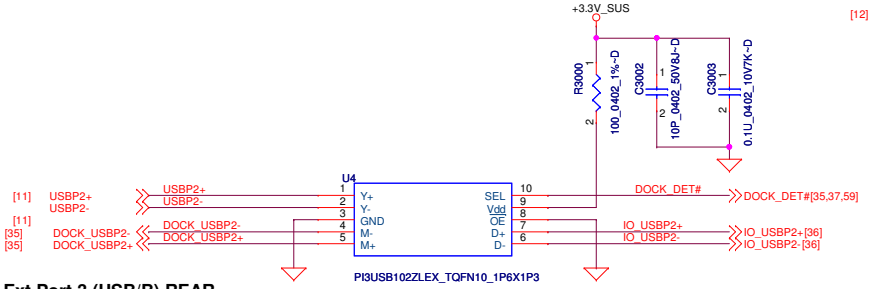
CRT SW for MB/DOCK





SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

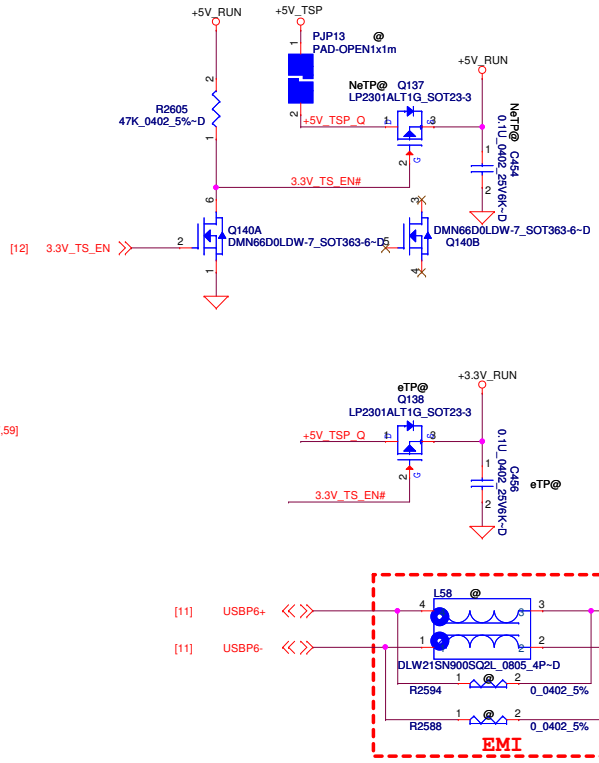
USB 2.0 Switch



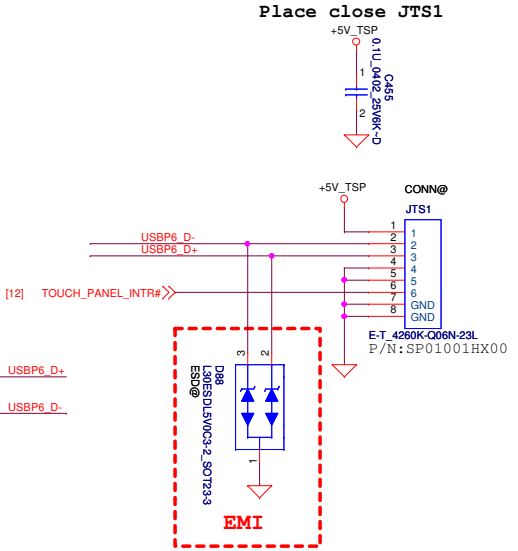
Ext Port 3 (USB/B) REAR

E-DOCK2

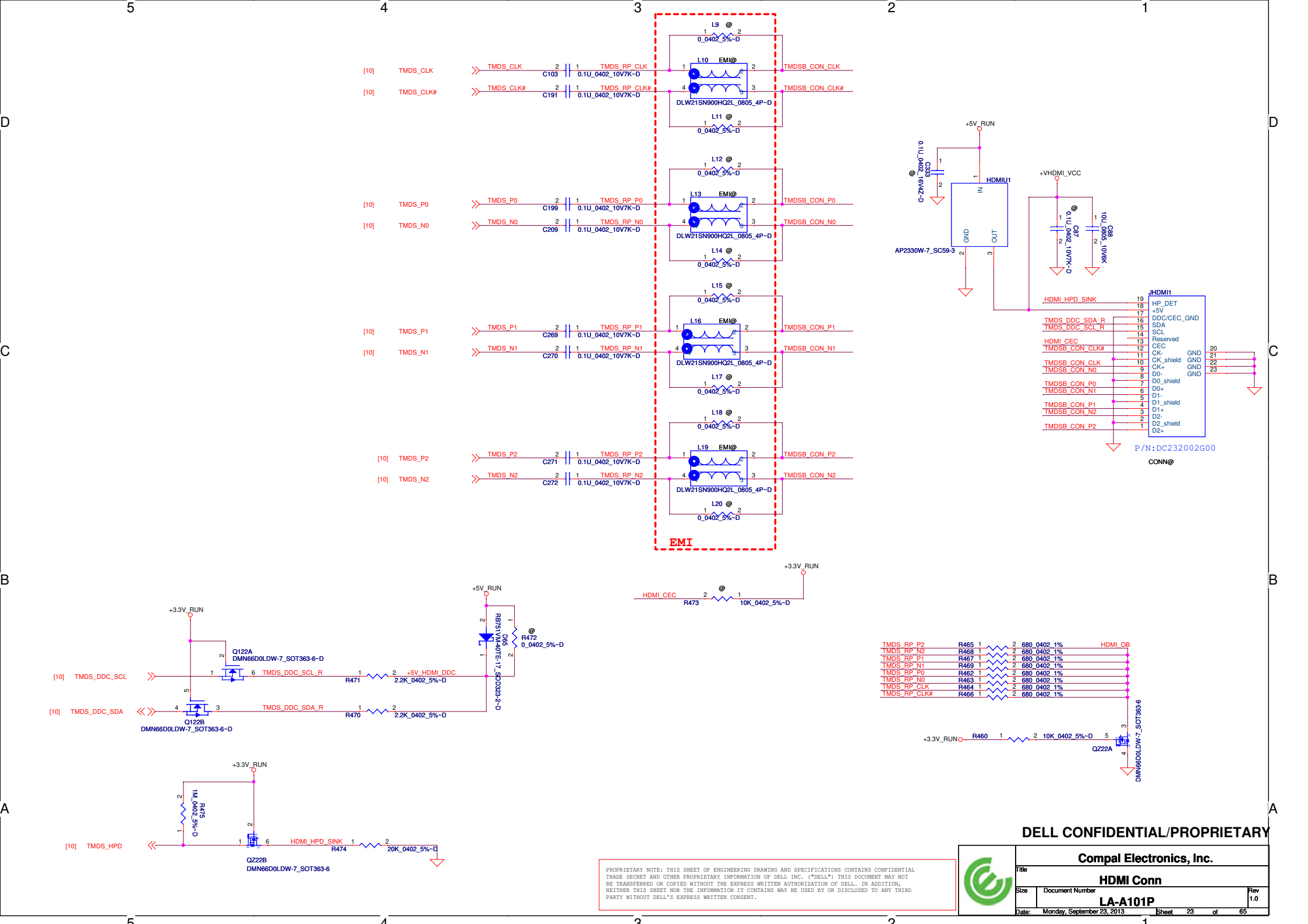
SEL	Y+	Y
L (Dock)	M+	M-
H(IO)	D+	D-



Touch Screen Connector



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date 2012/07/15	Title: CRT switch/Conn and TS
			Size: Document Number: Rev 1.0
			Date: Monday, September 23, 2013 Sheet 22 of 65



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Compal Electronics, Inc.

Title: HDMI Conn

Size | Document Number: LA-A101P | Rev: 1.0

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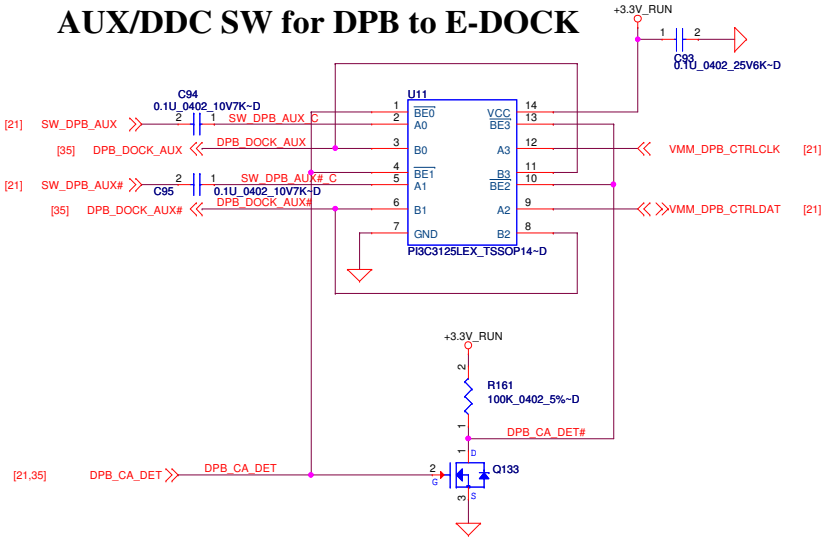
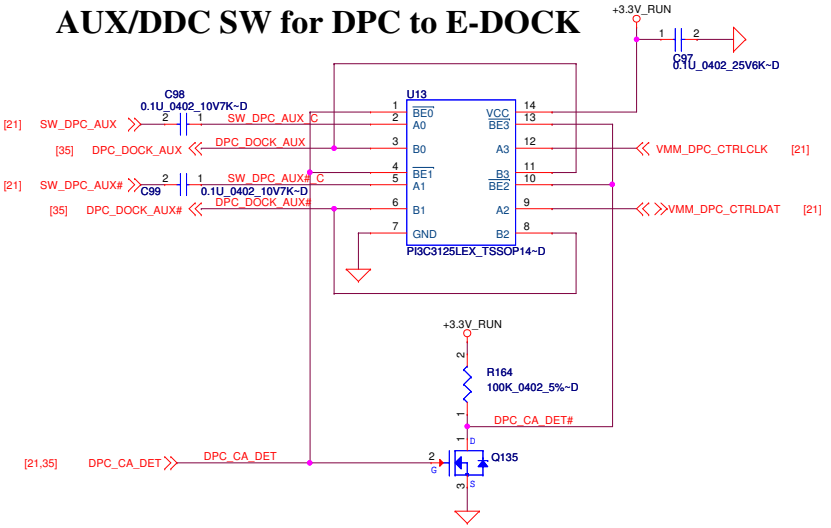
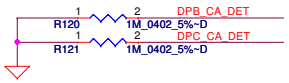
AUX/DDC SW for DPB to E-DOCK



AUX/DDC SW for DPC to E-DOCK





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Compal Electronics, Inc.	
Title	DP SW DP125
Size	Document Number: LA-A101P
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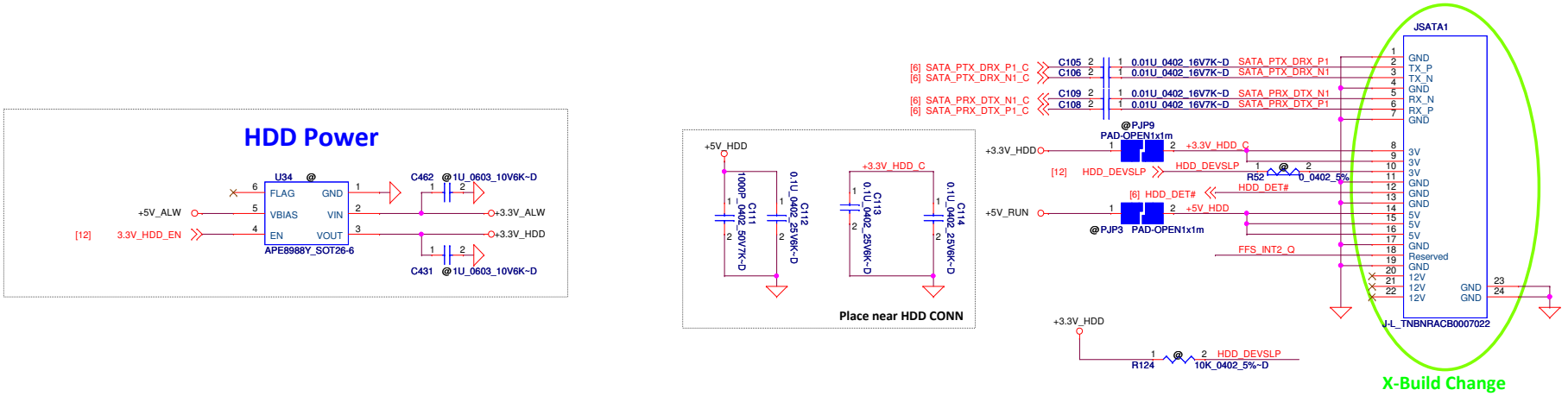

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Compal Electronics, Inc.

Title: HDD CONN

Size | Document Number: LA-A101P | Rev: 1.0

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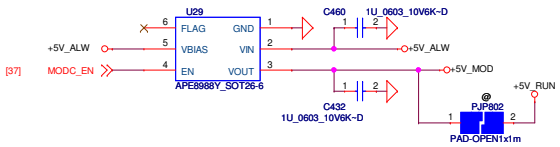
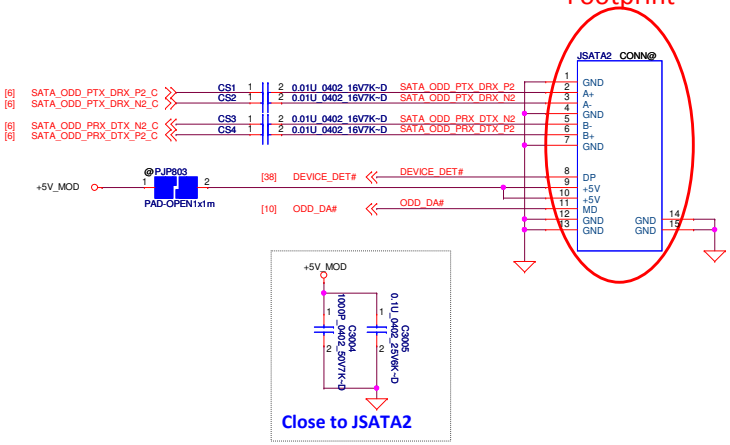
ODD power



Footprint



Compal Electronics, Inc.

Title: ODD module

Size | Document Number: LA-A101P | Rev: 1.0

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Internal Speakers Header

40 mils trace keep 10 mil spacing

DVDD_IO should match with HDA Bus level

EMI

ESD

Close to U17

Place R142 close to codec

Place R136 close to codec

X-Build Change

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Close to U17 pin5

Close to U17 pin6

Analog 5V

Analog 3.3V

2A: 80 mil width

SLEEVE/RING2 : keep 40mils trace
AUD_HP_OUT_R/AUD_HP_OUT_L : keep 15mils trace

Place C134 close to Codec

Place close to Codec

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S (for Global Headset)

Pay attention to Audio no sound issue.

Compal Electronics, Inc.

Title: Azalia (HD) Codec - ALC3226

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X-Build Change

SA000066W4L I218

SA00005OO3L I217 (A3)

Pin 6 is SVR_EN in Clarkville

Pin 2 is WAKE_EN in Clarkville

SMBus Device Address 0xC8

Place C188 close to pin5

Note:
+1.0V_LAN will work at 0.95V to 1.15V

Place C177, C180 and L26 close to U21

LAN ANALOG SWITCH

Layout Notice : Place bead as close PI3L720 as possible

EMI

DOCKED	1: TO DOCK
	0: TO RJ45

To LED on LAN jack

Compal Electronics, Inc.

Title: LAN Lewisville / LAN SW

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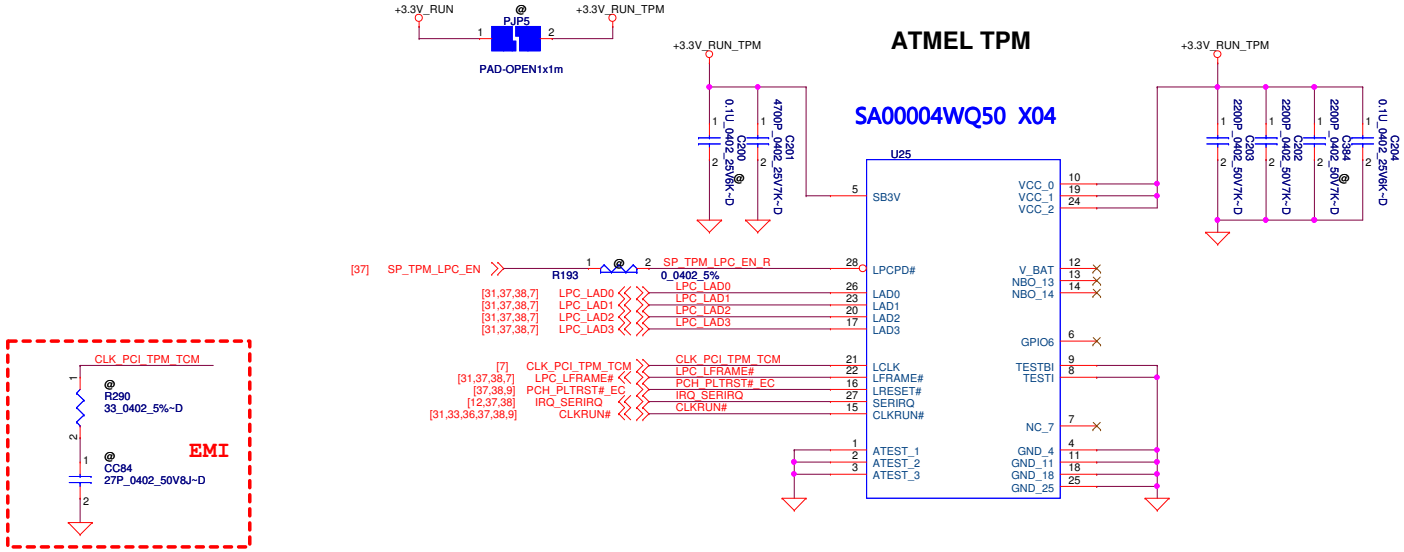
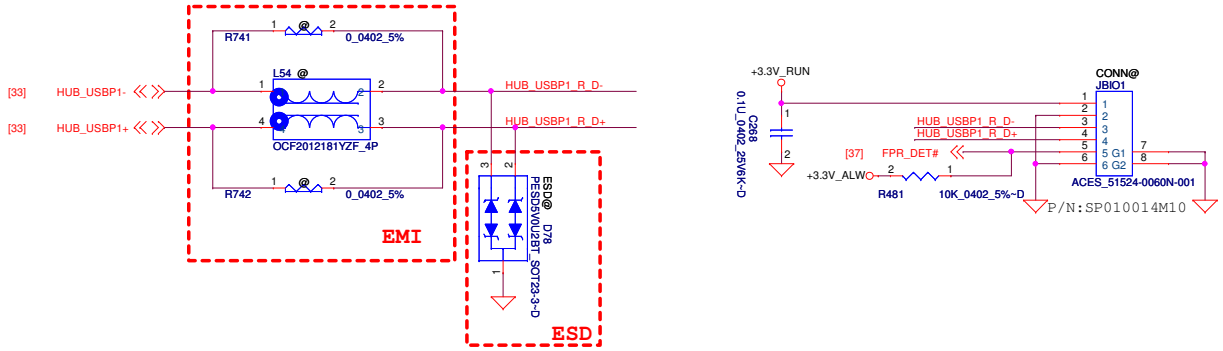


Finger print module



Compal Electronics, Inc.

Title: TPM/FP

Size | Document Number: LA-A101P | Rev: 1.0

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homestay ES1(no SD4.0)
M00 (symbol has been updated 26~36 pin swap)

U27 OZ777FJ2LN

OZ777FJ2LN_QFN48P_6X6

L36 close to U27.31 within 200mils
+1.2V_LDO, +1.2V_LDO_AIN trace width 30mils

C210 close to U27.42
C211 C212 close to U27.23

C215 close to U27.9
C213 C214 close to U27.35

C215 must close to U27.27 within 50mils
C214 must close to U27.9 within 50mils
C213 must close to U27.9 with 100mils
L35 must close to U38.9 within 200mils
+3.3V_RUN_AIN trace width 30mils

C227 near U27.22

C228 C229 near U27.24

30mils width

R205 must be close to U27 pin4 less than 100mils

check MEDIACARD_PWREN pull up to 3.3VRUN or connect to PCH.

EMI

please routing daisy chain
1. from U27.38 (SD_D0) -> U27.32 (SD_RCLK_P) -> L46.4
2. From U27.37 (SD_D1) -> U27.33 (SD_RCLK_N) -> L46.1

Near to JSD1

JSD1 CONN@ ALPS_SCDADA0101_NR

NO MMC+

Modify Footprint

IO0_LDOSEL:
High: Select internal LDO for main area core power.
Low: Select external LDO for main area core power.

Compal Electronics, Inc.

Title: Card Reader OZ777FJ2

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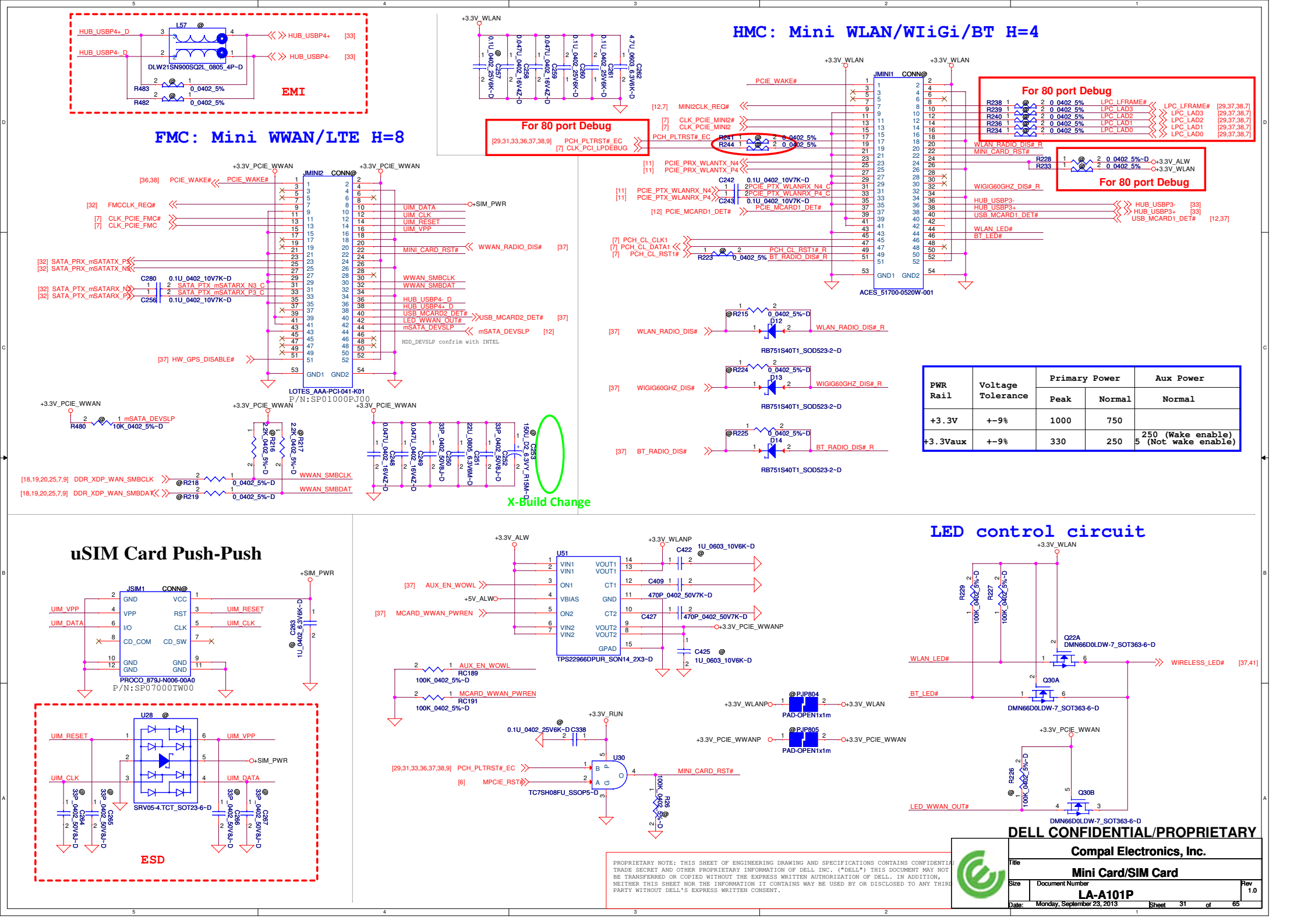
EMI
HUB_USBP4+_D
HUB_USBP4-_D
HUB_USBP4+
HUB_USBP4-
DLW21SN900SQ2L_0805_4P~D
R483 0_0402_5%
R482 0_0402_5%
FMC: Mini WWAN/LTE H=8
JMINI2 CONN@
LOTES_AAA-PCI-041-K01
P/N:SP01000PJ00
+3.3V_PCIE_WWAN
PCIE_WAKE#
FMCCLK_REQ#
CLK_PCIE_FMC#
CLK_PCIE_FMC
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
+SIM_PWR
MINI_CARD_RST#
WWAN_RADIO_DIS#
WWAN_SMBCLK
WWAN_SMBDAT
HUB_USBP4-_D
HUB_USBP4+_D
USB_MCARD2_DET#
LED_WWAN_OUT#
mSATA_DEVSLP
HDD_DEVSLP confrim with INTEL
HW_GPS_DISABLE#
SATA_PRX_mSATATX_P3
SATA_PRX_mSATATX_N3
SATA_PTX_mSATARX_N3_C
SATA_PTX_mSATARX_P3_C
C280 0.1U_0402_10V7K~D
C256 0.1U_0402_10V7K~D
R480 10K_0402_5%~D
R216 2.2K_0402_5%~D
R217 2.2K_0402_5%~D
R218 0_0402_5%~D
R219 0_0402_5%~D
DDR_XDP_WAN_SMBCLK
DDR_XDP_WAN_SMBDAT
C253 150U_D2_6.3VY_R15M~D
X-Build Change
HMC: Mini WLAN/WIiGi/BT H=4
JMINI1 CONN@
ACES_51700-0520W-001
+3.3V_WLAN
PCIE_WAKE#
MINI2CLK_REQ#
CLK_PCIE_MINI2#
CLK_PCIE_MINI2
PCH_PLTRST#_EC
CLK_PCI_LPDEBUG
PCIE_PRX_WLANTX_N4
PCIE_PRX_WLANTX_P4
PCIE_PTX_WLANRX_N4_C
PCIE_PTX_WLANRX_P4_C
PCIE_MCARD1_DET#
PCH_CL_CLK1
PCH_CL_DATA1
PCH_CL_RST1#
WLAN_RADIO_DIS#_R
MINI_CARD_RST#
WIGIG60GHZ_DIS#_R
BT_RADIO_DIS#_R
HUB_USBP3-
HUB_USBP3+
USB_MCARD1_DET#
WLAN_LED#
BT_LED#
C242 0.1U_0402_10V7K~D
C243 0.1U_0402_10V7K~D
R223 0_0402_5%
For 80 port Debug
R238 0_0402_5%
R239 0_0402_5%
R240 0_0402_5%
R236 0_0402_5%
R234 0_0402_5%
LPC_LFRAME#
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
R228 0_0402_5%~D
R233 0_0402_5%
+3.3V_ALW
+3.3V_WLAN
D12 RB751S40T1_SOD523-2~D
D13 RB751S40T1_SOD523-2~D
D14 RB751S40T1_SOD523-2~D
R215 0_0402_5%~D
R224 0_0402_5%~D
R225 0_0402_5%~D
WLAN_RADIO_DIS#
WIGIG60GHZ_DIS#
BT_RADIO_DIS#
PWR Rail
Voltage Tolerance
Primary Power
Peak
Normal
Aux Power
Normal
+3.3V
+-9%
1000
750
+3.3Vaux
+-9%
330
250
250 (Wake enable)
5 (Not wake enable)
uSIM Card Push-Push
JSIM1 CONN@
PROCO_879J-N006-00A0
P/N:SP07000TW00
+SIM_PWR
UIM_VPP
UIM_DATA
UIM_RESET
UIM_CLK
C263 1U_0402_6.3V6K~D
ESD
U28 @
SRV05-4.TCT_SOT23-6~D
C264 33P_0402_50V8J~D
C265 33P_0402_50V8J~D
C266 33P_0402_50V8J~D
C267 33P_0402_50V8J~D
+3.3V_ALW
+3.3V_WLANP
U51
TPS22966DPUR_SON14_2X3~D
AUX_EN_WOWL
+5V_ALW
MCARD_WWAN_PWREN
C422 1U_0603_10V6K~D
C409 470P_0402_50V7K~D
C427 470P_0402_50V7K~D
C425 1U_0603_10V6K~D
RC189 100K_0402_5%~D
RC191 100K_0402_5%~D
+3.3V_RUN
C338 0.1U_0402_25V6K~D
U30
TC7SH08FU_SSOP5~D
PCH_PLTRST#_EC
MPCIE_RST#
MINI_CARD_RST#
R26 100K_0402_5%~D
PJP804 PAD-OPEN1x1m
PJP805 PAD-OPEN1x1m
+3.3V_WLAN
+3.3V_PCIE_WWANP
LED control circuit
Q22A DMN66D0LDW-7_SOT363-6~D
Q30A DMN66D0LDW-7_SOT363-6~D
Q30B DMN66D0LDW-7_SOT363-6~D
R229 100K_0402_5%~D
R227 100K_0402_5%~D
R226 100K_0402_5%~D
WLAN_LED#
BT_LED#
LED_WWAN_OUT#
WIRELESS_LED#
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Compal Electronics, Inc.
Title
Mini Card/SIM Card
Size
Document Number
LA-A101P
Rev
1.0
Date: Monday, September 23, 2013
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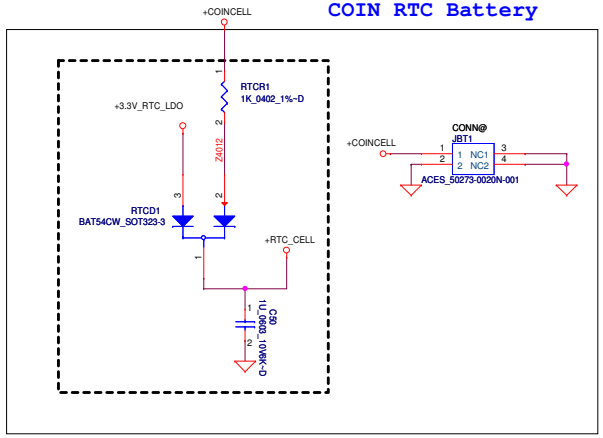
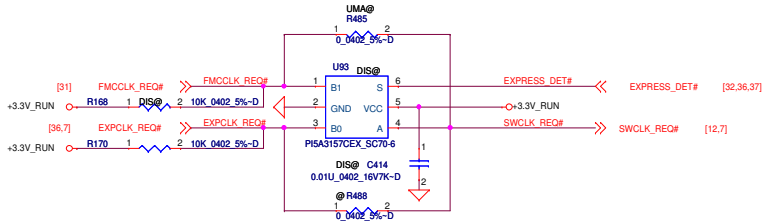
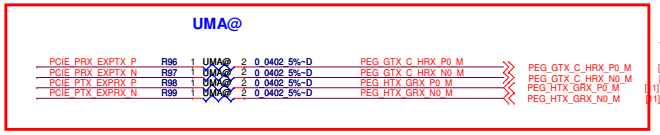
EXP/FMC PCIe clock/REQ Switch

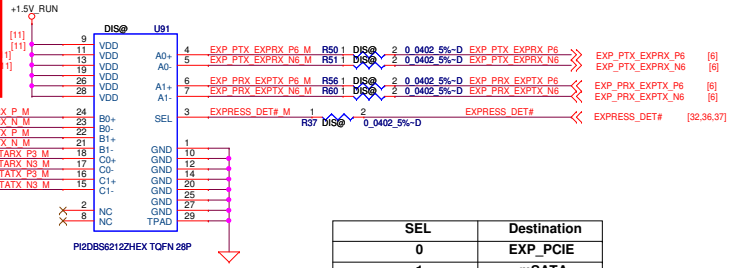
COIN RTC Battery



B \ S	EXPRESS_DET#
EXPCLK_REQ#	0
FMCCLK_REQ#	1

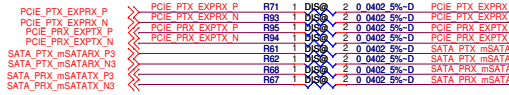






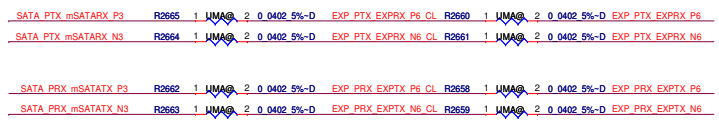
EXPRESS <-----

WWAN FMC <-----



SEL	Destination
0	EXP_PCIE
1	mSATA

UMA@ Co-Layout with PI2DBS6212 PCIE/SATA SW

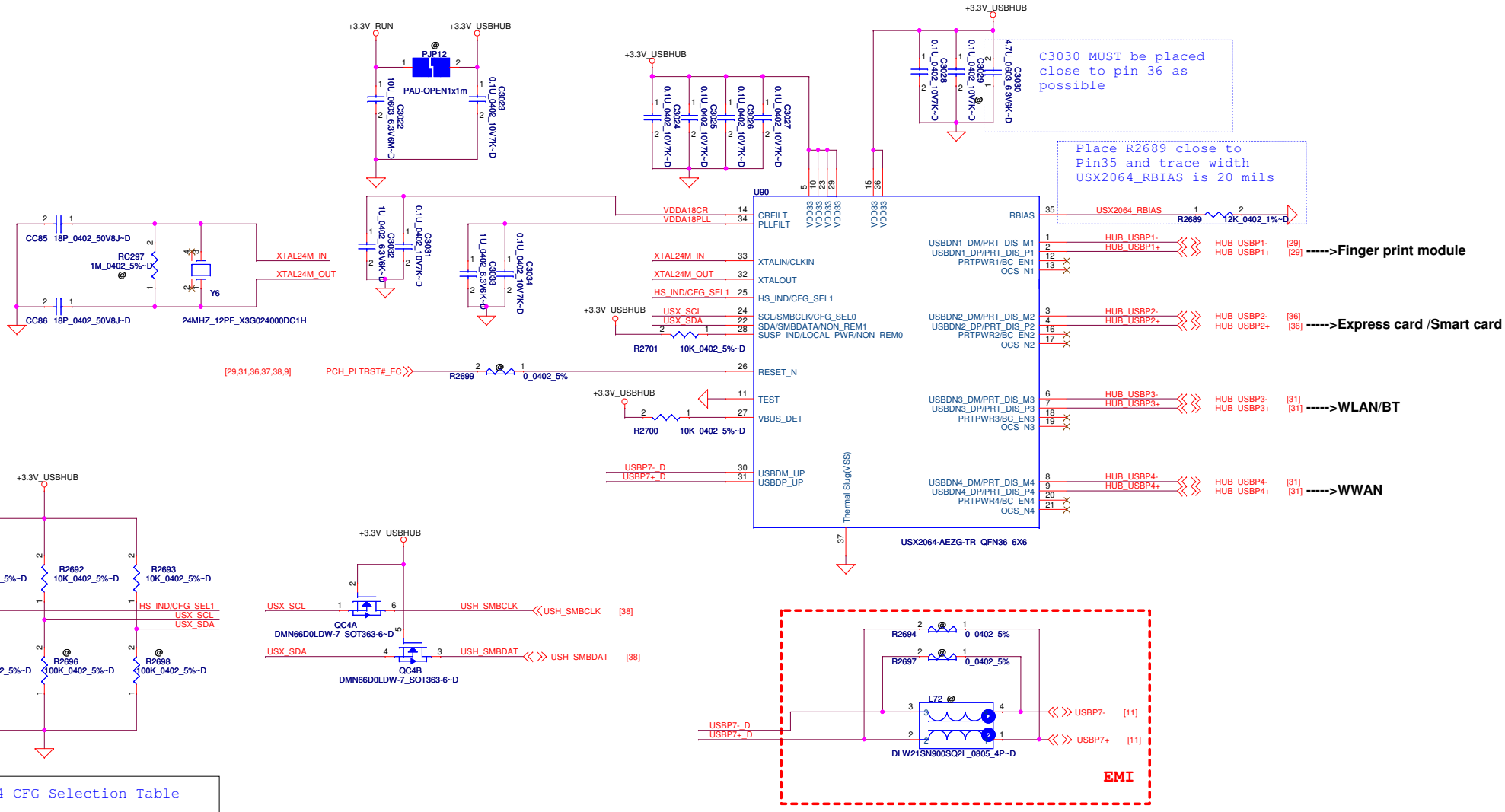


Compal Electronics, Inc.

Title: RTC Batt/PCIE_SATA SW

Size | Document Number: LA-A101P | Rev: 1.0

Date: Monday, September 23, 2013 | Sheet 32 of 65



USX2064 CFG Selection Table		
CFG_SEL[0] / CFG_SEL[1]	0	1
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM

Compal Electronics, Inc.

Title: USB2.0 HUB-USX2064

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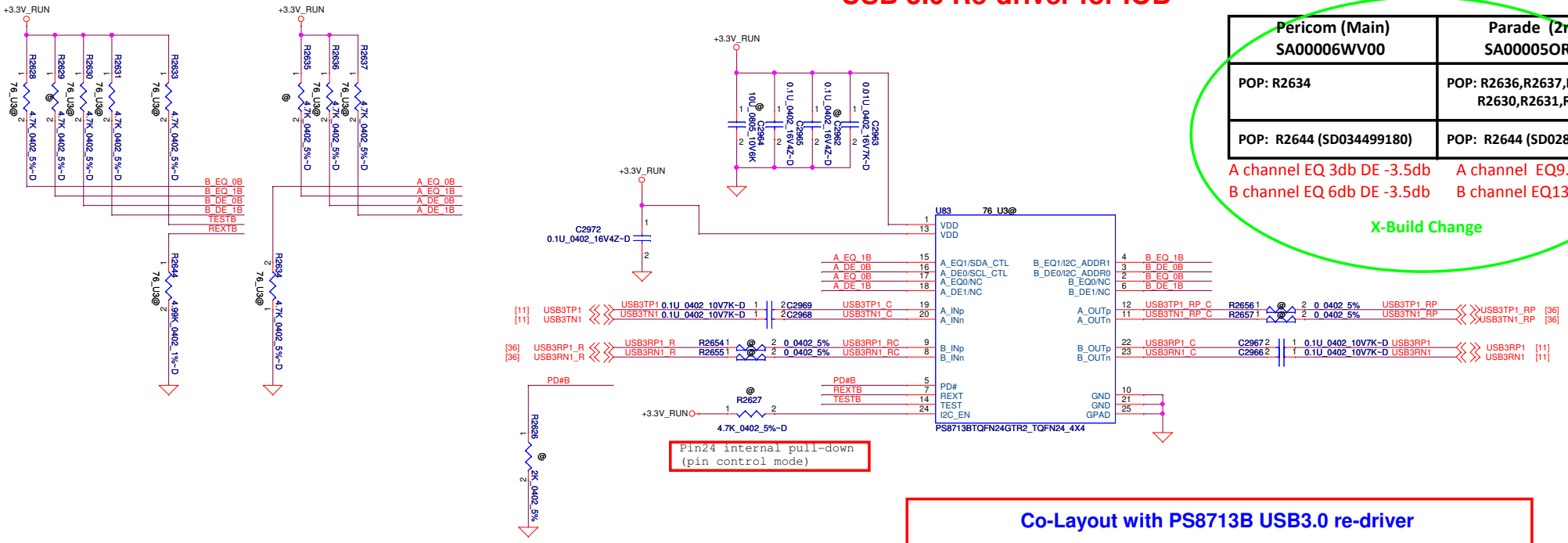
USB 3.0 Re-driver for IOB

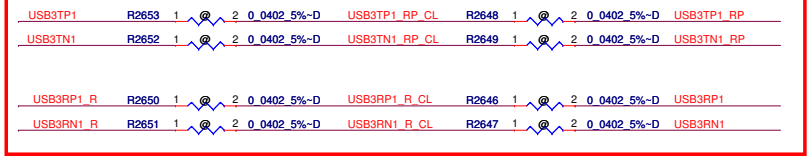
Pericom (Main) SA00006WV00	Parade (2nd) SA00005OR20
POP: R2634	POP: R2636,R2637,R2628, R2630,R2631,R2633,
POP: R2644 (SD034499180)	POP: R2644 (SD028430180)

A channel EQ 3db DE -3.5db A channel EQ9.5 DE 5
B channel EQ 6db DE -3.5db B channel EQ13 DE 5

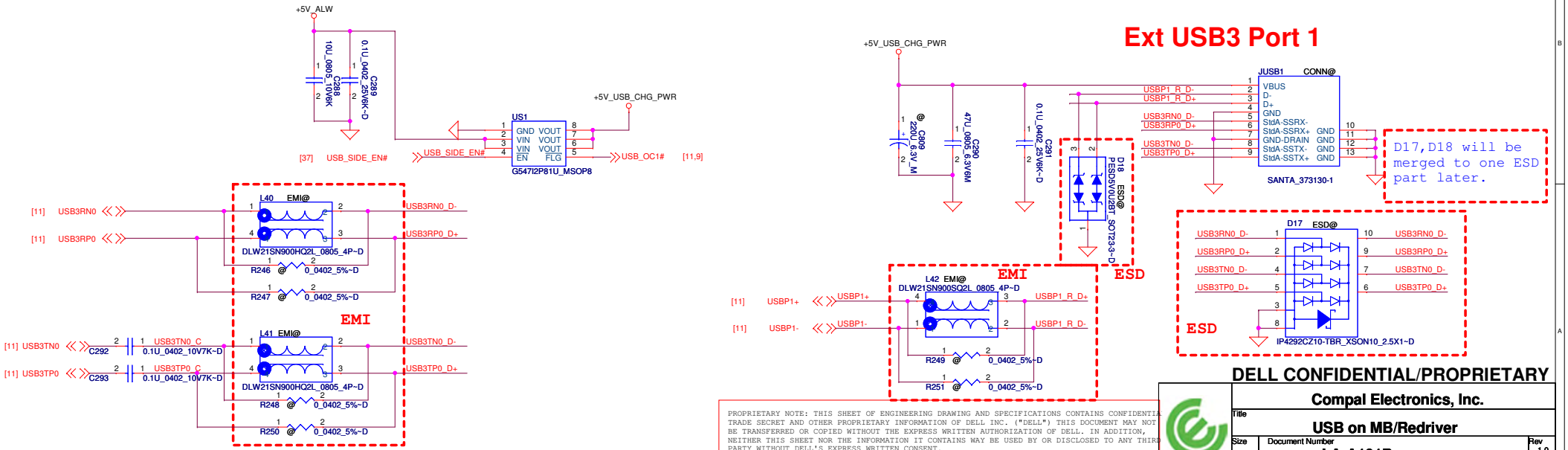
X-Build Change



Co-Layout with PS8713B USB3.0 re-driver



Ext USB3 Port 1



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Compal Electronics, Inc.

Title: USB on MB/Redriver

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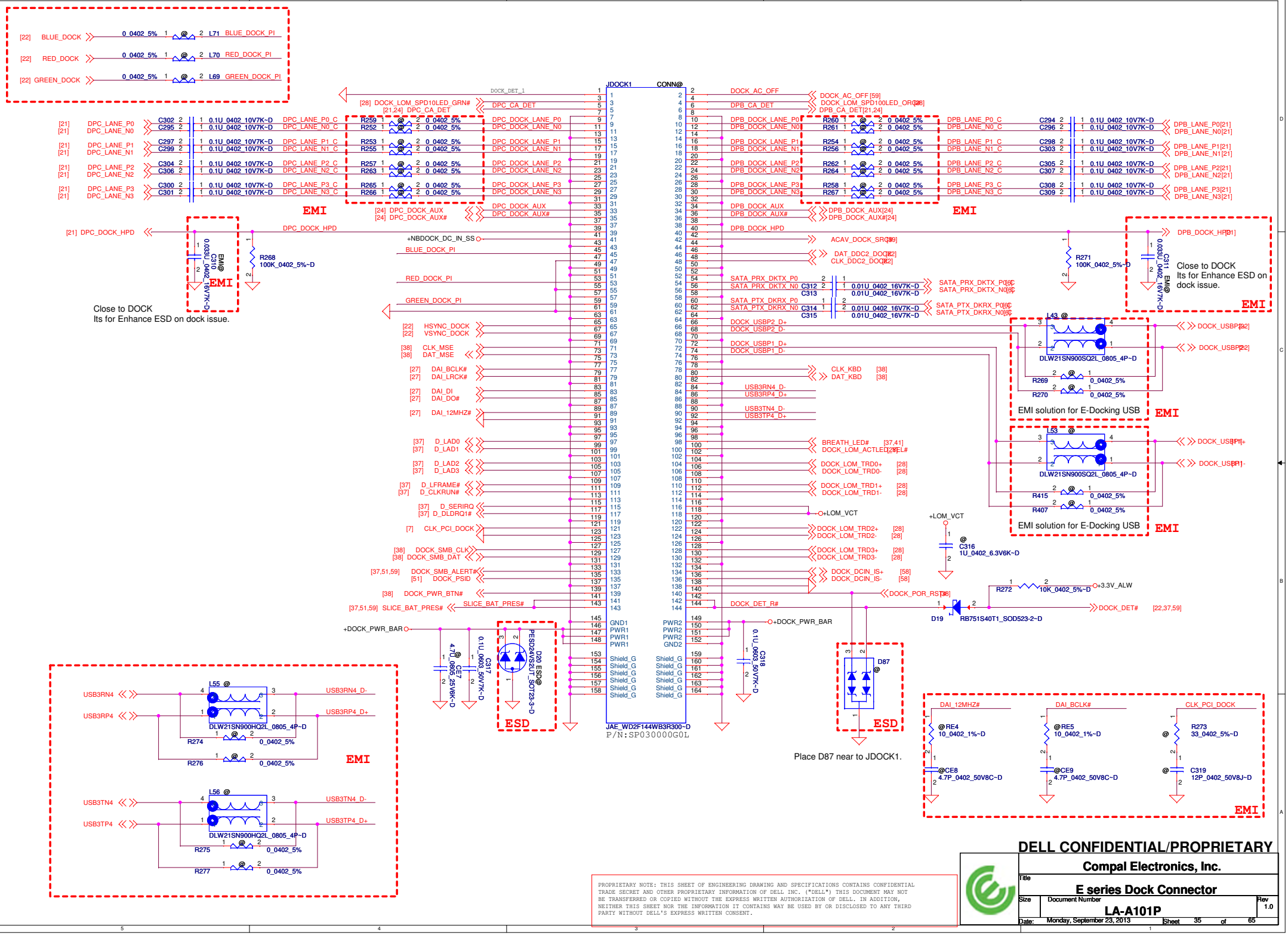
JDOCK1
CONN@
JAE_WD2F144WB3R300~D
P/N:SP030000G0L
EMI
ESD
Close to DOCK
Its for Enhance ESD on dock issue.
EMI solution for E-Docking USB
Place D87 near to JDOCK1.
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Compal Electronics, Inc.
E series Dock Connector
LA-A101P
Monday, September 23, 2013
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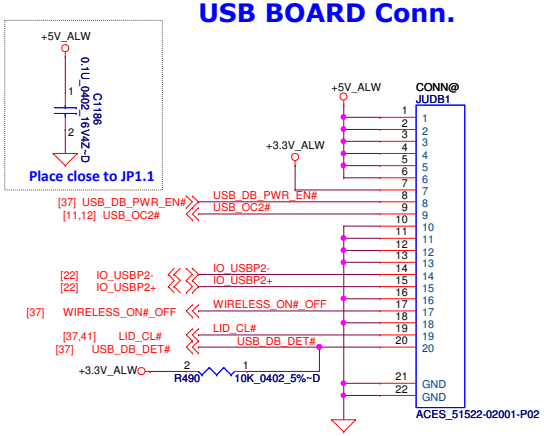
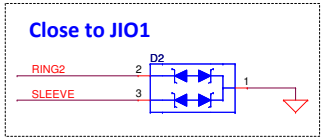
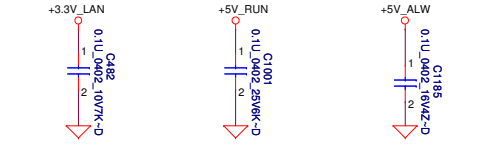
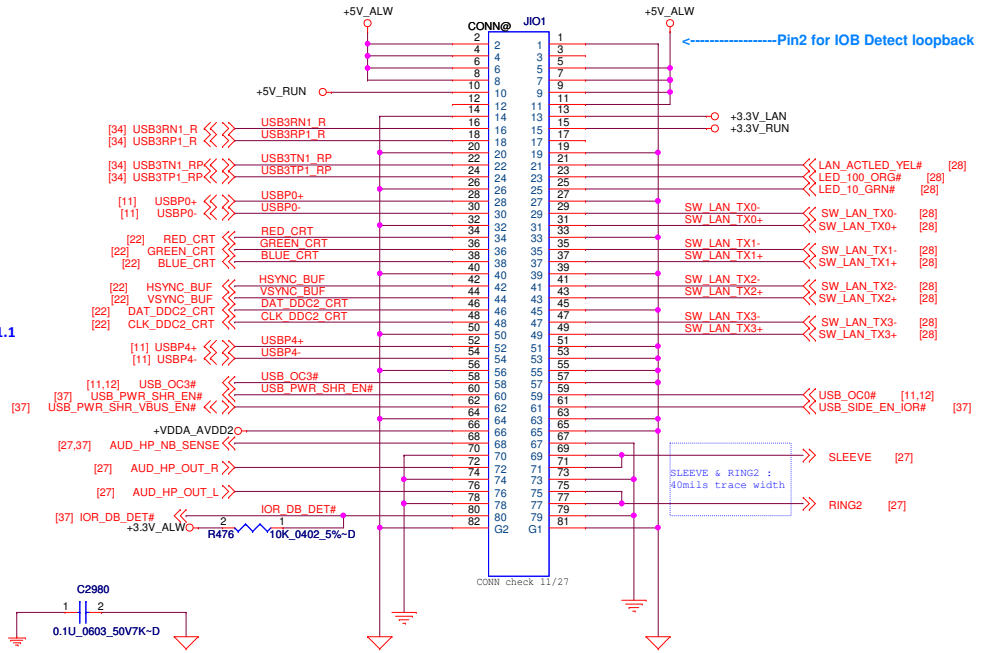
USB BOARD Conn.

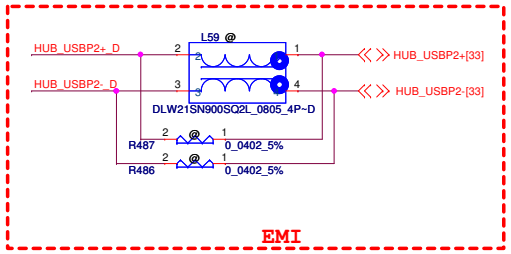


Close to JIO1

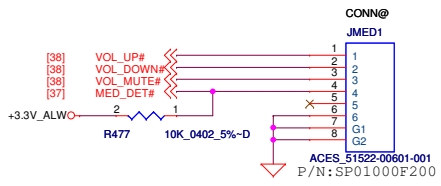




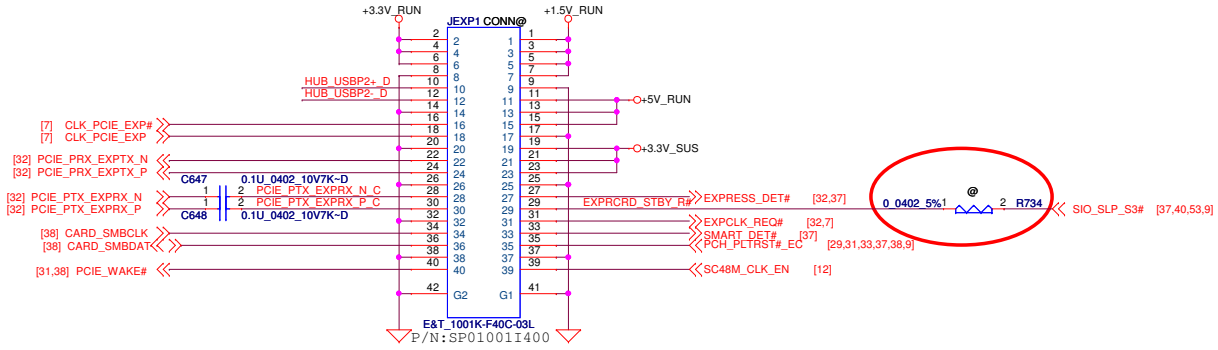




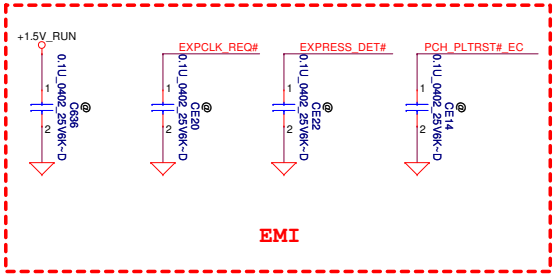
MEDIA BOARD Conn.

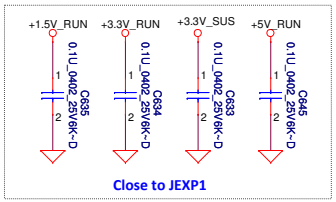


Express/Smart Card Conn.

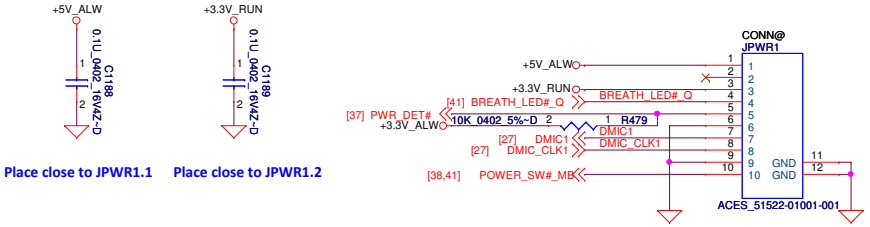


Link CIS

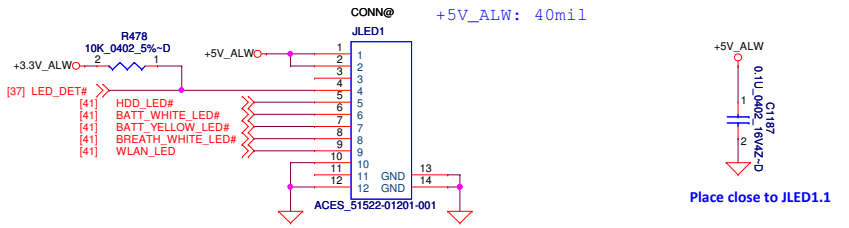




POWER BOARD Conn.



LED EXTERNAL BOARD Conn.



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Compal Electronics, Inc.		
Title: I/O Conn		
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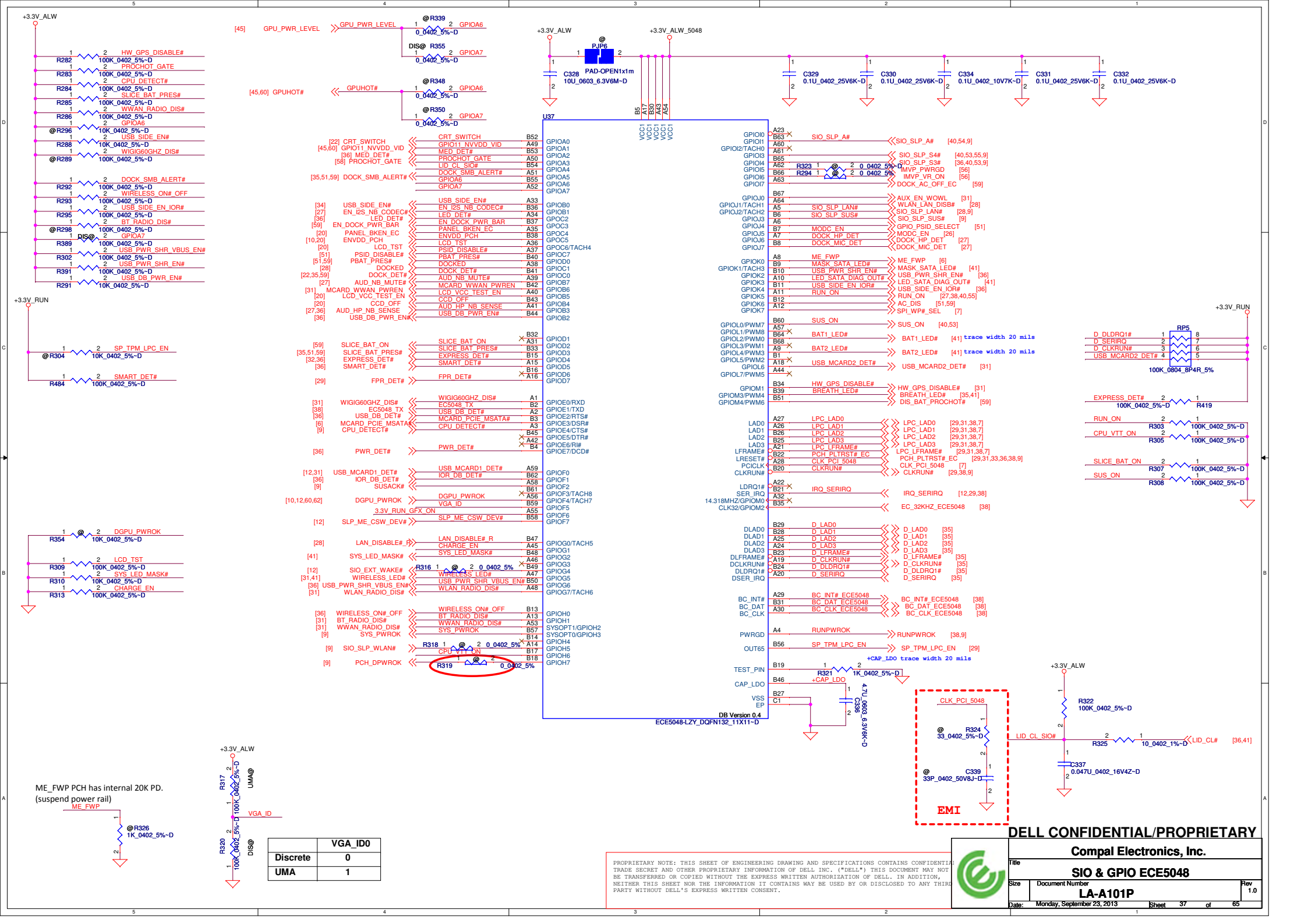
+3.3V_ALW
R282 HW_GPS_DISABLE# 100K_0402_5%~D
R283 PROCHOT_GATE 100K_0402_5%~D
R284 GPU_DETECT# 100K_0402_5%~D
R285 SLICE_BAT_PRES# 100K_0402_5%~D
R286 WWAN_RADIO_DIS# 100K_0402_5%~D
@R296 GPIOA6 10K_0402_5%~D
R288 USB_SIDE_EN# 10K_0402_5%~D
@R289 WIGIG60GHZ_DIS# 100K_0402_5%~D
R292 DOCK_SMB_ALERT# 100K_0402_5%~D
R293 WIRELESS_ON#_OFF 100K_0402_5%~D
R295 USB_SIDE_EN_IOR# 100K_0402_5%~D
@R298 BT_RADIO_DIS# 100K_0402_5%~D
R389 DIS@ GPIOA7 100K_0402_5%~D
R302 USB_PWR_SHR_VBUS_EN# 100K_0402_5%~D
R391 USB_PWR_SHR_EN# 100K_0402_5%~D
R291 USB_DB_PWR_EN# 10K_0402_5%~D
+3.3V_RUN
@R304 SP_TPM_LPC_EN 10K_0402_5%~D
R484 SMART_DET# 100K_0402_5%~D
R354 @ DGPU_PWROK 10K_0402_5%~D
R309 LCD_TST 100K_0402_5%~D
R310 SYS_LED_MASK# 10K_0402_5%~D
R313 CHARGE_EN 100K_0402_5%~D
[45] GPU_PWR_LEVEL GPU_PWR_LEVEL @R339 0_0402_5%~D GPIOA6
DIS@ R355 0_0402_5%~D GPIOA7
[45,60] GPUHOT# GPUHOT# @R348 0_0402_5%~D GPIOA6
@R350 0_0402_5%~D GPIOA7
+3.3V_ALW
@ PJP6 PAD-OPEN1x1m
C328 10U_0603_6.3V6M~D
+3.3V_ALW_5048
C329 0.1U_0402_25V6K~D
C330 0.1U_0402_25V6K~D
C334 0.1U_0402_10V7K~D
C331 0.1U_0402_25V6K~D
C332 0.1U_0402_25V6K~D
B5 A37 A43 A54 VCC1
U37
[22] CRT_SWITCH CRT_SWITCH B52 GPIOA0
[45,60] GPIO11_NVVDD_VID GPIO11_NVVDD_VID A49 GPIOA1
[36] MED_DET# MED_DET# B53 GPIOA2
[58] PROCHOT_GATE PROCHOT_GATE A50 GPIOA3
LID_CL_SIO# B54 GPIOA4
[35,51,59] DOCK_SMB_ALERT# DOCK_SMB_ALERT# A51 GPIOA5
GPIOA6 B55 GPIOA6
GPIOA7 A52 GPIOA7
[34] USB_SIDE_EN# USB_SIDE_EN# A33 GPIOB0
[27] EN_I2S_NB_CODEC# EN_I2S_NB_CODEC# B36 GPIOB1
[36] LED_DET# LED_DET# A34 GPIOC2
[59] EN_DOCK_PWR_BAR EN_DOCK_PWR_BAR B37 GPIOC3
[20] PANEL_BKEN_EC PANEL_BKEN_EC A35 GPIOC4
[10,20] ENVDD_PCH ENVDD_PCH B38 GPIOC5
[20] LCD_TST LCD_TST A36 GPIOC6/TACH4
[51] PSID_DISABLE# PSID_DISABLE# A37 GPIOC7
[51,59] PBAT_PRES# PBAT_PRES# B40 GPIOD0
[28] DOCKED DOCKED A38 GPIOC1
[22,35,59] DOCK_DET# DOCK_DET# B41 GPIOC0
[27] AUD_NB_MUTE# AUD_NB_MUTE# A39 GPIOB7
[31] MCARD_WWAN_PWREN MCARD_WWAN_PWREN B42 GPIOB6
[20] LCD_VCC_TEST_EN LCD_VCC_TEST_EN A40 GPIOB5
[20] CCD_OFF CCD_OFF B43 GPIOB4
[27,36] AUD_HP_NB_SENSE AUD_HP_NB_SENSE A41 GPIOB3
[36] USB_DB_PWR_EN# USB_DB_PWR_EN# B44 GPIOB2
B32 GPIOD1
[59] SLICE_BAT_ON SLICE_BAT_ON A31 GPIOD2
[35,51,59] SLICE_BAT_PRES# SLICE_BAT_PRES# B33 GPIOD3
[32,36] EXPRESS_DET# EXPRESS_DET# B15 GPIOD4
[36] SMART_DET# SMART_DET# A15 GPIOD5
B16 GPIOD6
[29] FPR_DET# FPR_DET# A16 GPIOD7
[31] WIGIG60GHZ_DIS# WIGIG60GHZ_DIS# A1 GPIOE0/RXD
[38] EC5048_TX EC5048_TX B2 GPIOE1/TXD
[36] USB_DB_DET# USB_DB_DET# A2 GPIOE2/RTS#
[6] MCARD_PCIE_MSATA# MCARD_PCIE_MSATA# B3 GPIOE3/DSR#
[9] CPU_DETECT# CPU_DETECT# A3 GPIOE4/CTS#
B45 GPIOE5/DTR#
A42 GPIOE6/RI#
[36] PWR_DET# PWR_DET# B4 GPIOE7/DCD#
[12,31] USB_MCARD1_DET# USB_MCARD1_DET# A59 GPIOF0
[36] IOR_DB_DET# IOR_DB_DET# B62 GPIOF1
[9] SUSACK# A58 GPIOF2
B61 GPIOF3/TACH8
[10,12,60,62] DGPU_PWROK DGPU_PWROK A56 GPIOF4/TACH7
VGA_ID B59 GPIOF5
3.3V_RUN_GFX_ON A55 GPIOF6
[12] SLP_ME_CSW_DEV# SLP_ME_CSW_DEV# B58 GPIOF7
[28] LAN_DISABLE#_R LAN_DISABLE#_R B47 GPIOG0/TACH5
CHARGE_EN A45 GPIOG1
[41] SYS_LED_MASK# SYS_LED_MASK# B48 GPIOG2
A46 GPIOG3
[12] SIO_EXT_WAKE# R316 @ 0_0402_5% B49 GPIOG4
[31,41] WIRELESS_LED# WIRELESS_LED# A47 GPIOG5
[36] USB_PWR_SHR_VBUS_EN# USB_PWR_SHR_VBUS_EN# B50 GPIOG6
[31] WLAN_RADIO_DIS# WLAN_RADIO_DIS# A48 GPIOG7/TACH6
[36] WIRELESS_ON#_OFF WIRELESS_ON#_OFF B13 GPIOH0
[31] BT_RADIO_DIS# BT_RADIO_DIS# A13 GPIOH1
[31] WWAN_RADIO_DIS# WWAN_RADIO_DIS# A53 SYSOPT1/GPIOH2
[9] SYS_PWROK SYS_PWROK B57 SYSOPT0/GPIOH3
B14 GPIOH4
[9] SIO_SLP_WLAN# R318 @ 0_0402_5% CPU_VTT_ON A14 GPIOH5
B17 GPIOH6
[9] PCH_DPWROK R319 @ 0_0402_5% B18 GPIOH7
DB Version 0.4
ECE5048-LZY_DQFN132_11X11~D
GPIOI0 A23
GPIOI1 B63 SIO_SLP_A# SIO_SLP_A# [40,54,9]
GPIOI2/TACH0 A60
GPIOI3 A61 SIO_SLP_S4# [40,53,55,9]
GPIOI4 B65 SIO_SLP_S3# [36,40,53,9]
GPIOI5 A62 R323 @ 0_0402_5% IMVP_PWRGD [56]
GPIOI6 B66 R294 @ 0_0402_5% IMVP_VR_ON [56]
GPIOI7 A63 DOCK_AC_OFF_EC [59]
GPIOJ0 B67
GPIOJ1/TACH1 A64 AUX_EN_WOWL [31]
GPIOJ2/TACH2 A5 SIO_SLP_LAN# WLAN_LAN_DISB# [28]
GPIOJ3 B6 SIO_SLP_LAN# SIO_SLP_SUS# [28,9]
GPIOJ4 A6 SIO_SLP_SUS# [9]
GPIOJ5 B7 MODC_EN GPIO_PSID_SELECT [51]
GPIOJ6 A7 DOCK_HP_DET MODC_EN [26]
GPIOJ7 B8 DOCK_MIC_DET DOCK_HP_DET [27]
DOCK_MIC_DET [27]
GPIOK0 A8 ME_FWP ME_FWP [6]
GPIOK1/TACH3 B9 MASK_SATA_LED# MASK_SATA_LED# [41]
GPIOK2 B10 USB_PWR_SHR_EN# USB_PWR_SHR_EN# [36]
GPIOK3 A10 LED_SATA_DIAG_OUT# LED_SATA_DIAG_OUT# [41]
GPIOK4 B11 USB_SIDE_EN_IOR# USB_SIDE_EN_IOR# [36]
GPIOK5 A11 RUN_ON RUN_ON [27,38,40,55]
GPIOK6 B12 AC_DIS AC_DIS [51,59]
GPIOK7 A12 SPI_WP#_SEL [7]
GPIOL0/PWM7 B60 SUS_ON SUS_ON [40,53]
GPIOL1/PWM8 A57
GPIOL2/PWM0 B64 BAT1_LED# BAT1_LED# [41] trace width 20 mils
GPIOL3/PWM1 B68
GPIOL4/PWM3 A9 BAT2_LED# BAT2_LED# [41] trace width 20 mils
GPIOL5/PWM2 B1
GPIOL6 A18 USB_MCARD2_DET# USB_MCARD2_DET# [31]
GPIOL7/PWM5 A44
GPIOM1 B34 HW_GPS_DISABLE# HW_GPS_DISABLE# [31]
GPIOM3/PWM4 B39 BREATH_LED# BREATH_LED# [35,41]
GPIOM4/PWM6 B51 DIS_BAT_PROCHOT# [59]
LAD0 A27 LPC_LAD0 LPC_LAD0 [29,31,38,7]
LAD1 A26 LPC_LAD1 LPC_LAD1 [29,31,38,7]
LAD2 B26 LPC_LAD2 LPC_LAD2 [29,31,38,7]
LAD3 B25 LPC_LAD3 LPC_LAD3 [29,31,38,7]
LFRAME# A21 LPC_LFRAME# LPC_LFRAME# [29,31,38,7]
LRESET# B22 PCH_PLTRST#_EC PCH_PLTRST#_EC [29,31,33,36,38,9]
PCICLK A28 CLK_PCI_5048 CLK_PCI_5048 [7]
CLKRUN# B20 CLKRUN# CLKRUN# [29,38,9]
LDRQ1# A22
SER_IRQ B21 IRQ_SERIRQ IRQ_SERIRQ [12,29,38]
14.318MHZ/GPIOM0 A32
CLK32/GPIOM2 B35 EC_32KHZ_ECE5048 [38]
DLAD0 B29 D_LAD0 D_LAD0 [35]
DLAD1 B28 D_LAD1 D_LAD1 [35]
DLAD2 A25 D_LAD2 D_LAD2 [35]
DLAD3 A24 D_LAD3 D_LAD3 [35]
DLFRAME# B23 D_LFRAME# D_LFRAME# [35]
DCLKRUN# A19 D_CLKRUN# D_CLKRUN# [35]
DLDRQ1# B24 D_DLDRQ1# D_DLDRQ1# [35]
DSER_IRQ A20 D_SERIRQ D_SERIRQ [35]
BC_INT# A29 BC_INT#_ECE5048 BC_INT#_ECE5048 [38]
BC_DAT B31 BC_DAT_ECE5048 BC_DAT_ECE5048 [38]
BC_CLK A30 BC_CLK_ECE5048 BC_CLK_ECE5048 [38]
PWRGD A4 RUNPWROK RUNPWROK [38,9]
OUT65 B56 SP_TPM_LPC_EN SP_TPM_LPC_EN [29]
+CAP_LDO trace width 20 mils
TEST_PIN B19 R321 1K_0402_5%~D
CAP_LDO B46 +CAP_LDO C339 4.7U_0603_6.3V6K~D
VSS B27
EP C1
+3.3V_RUN
RP5 100K_0804_8P4R_5%
D_DLDRQ1# D_SERIRQ D_CLKRUN# USB_MCARD2_DET#
EXPRESS_DET# 100K_0402_5%~D R419
RUN_ON R303 100K_0402_5%~D
CPU_VTT_ON R305 100K_0402_5%~D
SLICE_BAT_ON R307 100K_0402_5%~D
SUS_ON R308 100K_0402_5%~D
CLK_PCI_5048
@ R324 33_0402_5%~D
@ C339 33P_0402_50V8J~D
EMI
+3.3V_ALW
R322 100K_0402_5%~D
LID_CL_SIO# R325 10_0402_1%~D LID_CL# [36,41]
C337 0.047U_0402_16V4Z~D
ME_FWP has internal 20K PD.
(suspend power rail)
ME_FWP
@R326 1K_0402_5%~D
+3.3V_ALW
R317 UMA@ 100K_0402_5%~D
VGA_ID
R320 DIS@ 100K_0402_5%~D
VGA_ID0
Discrete 0
UMA 1
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Title: SIO & GPIO ECE5048
Size: Document Number: LA-A101P
Rev: 1.0
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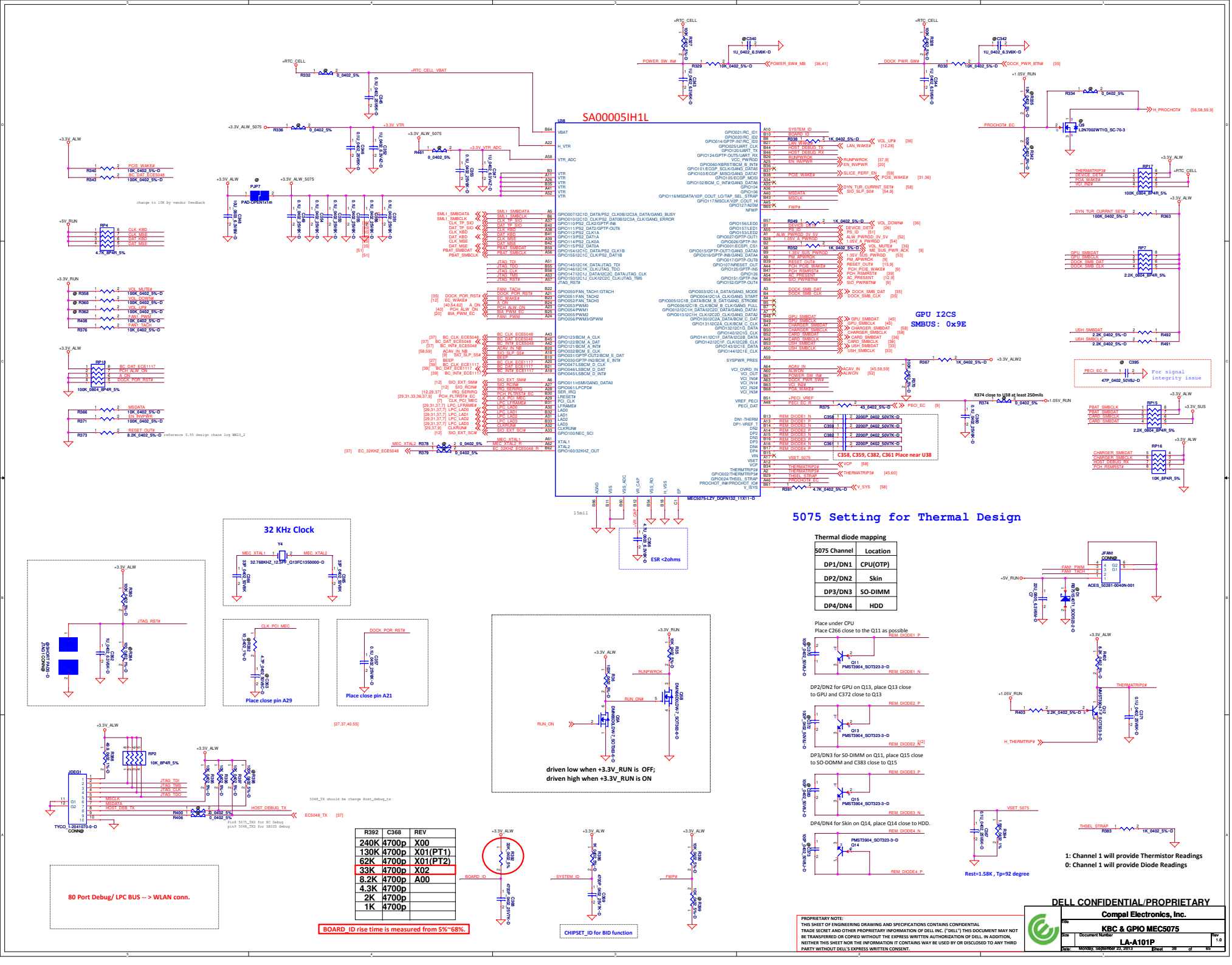
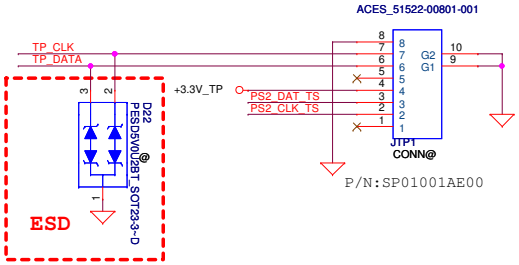
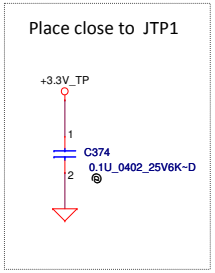
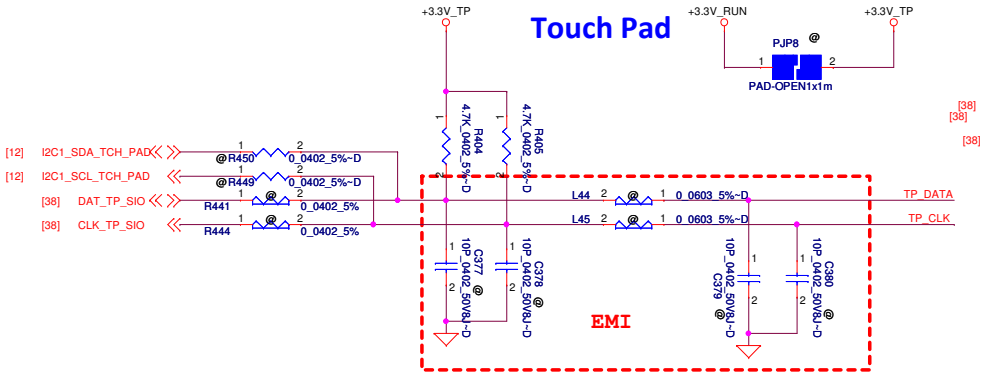
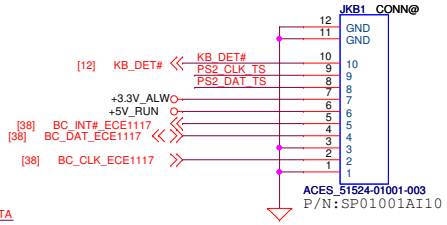


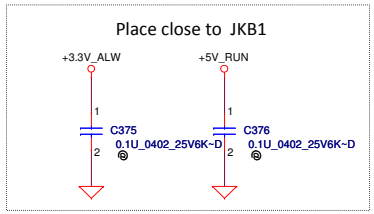
R392	C368	REV
240K	4700p	X00
130K	4700p	X01(PT1)
62K	4700p	X01(PT2)
33K	4700p	X02
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

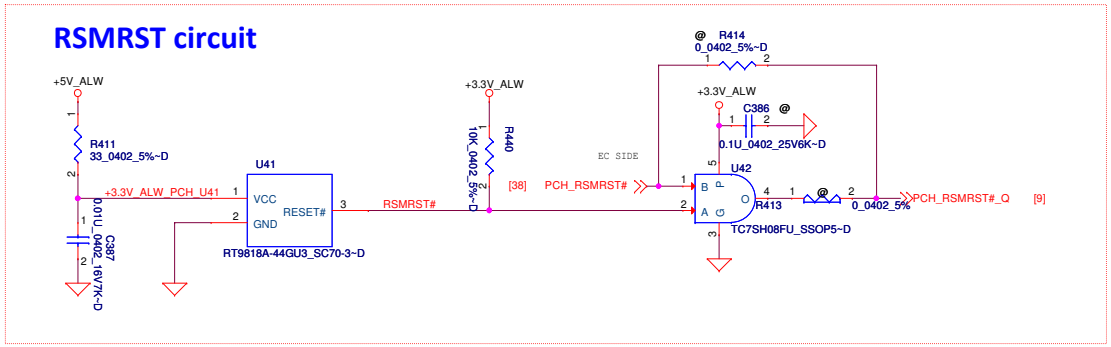












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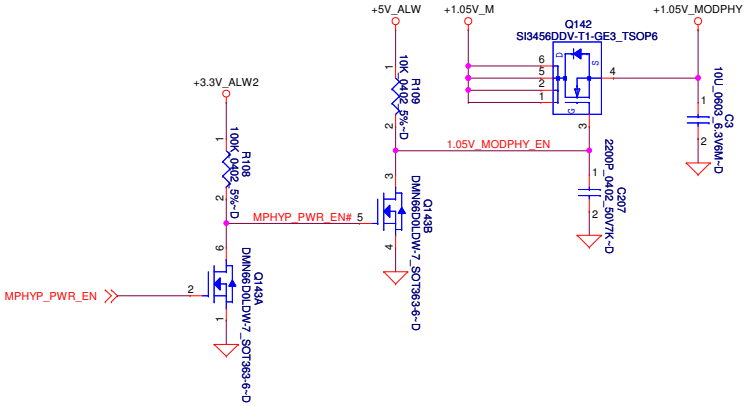
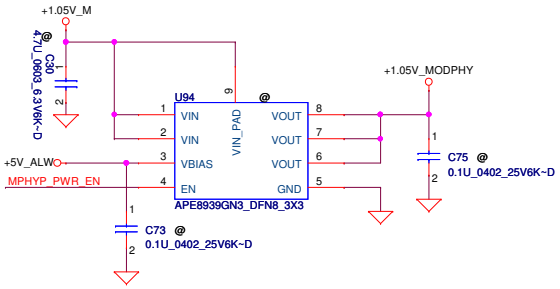
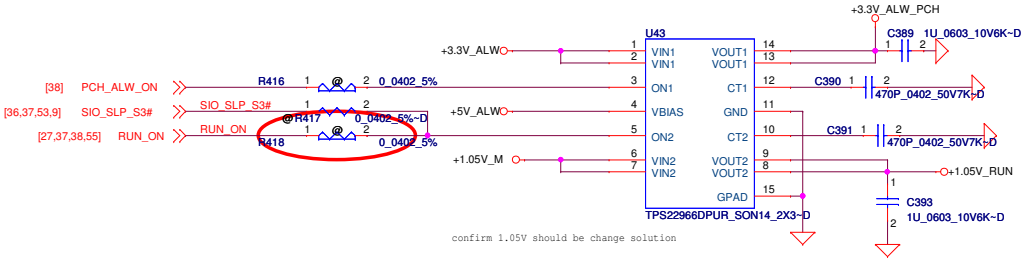
DC/DC Interface

+1.05V_MODPHY source

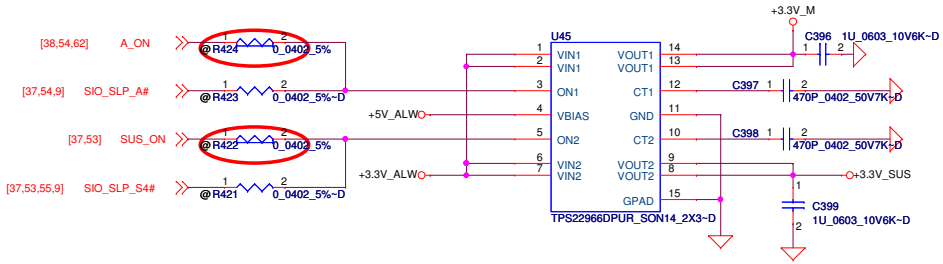




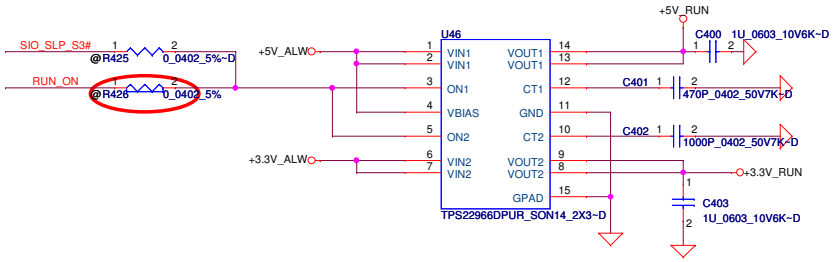
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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Title: POWER CONTROL

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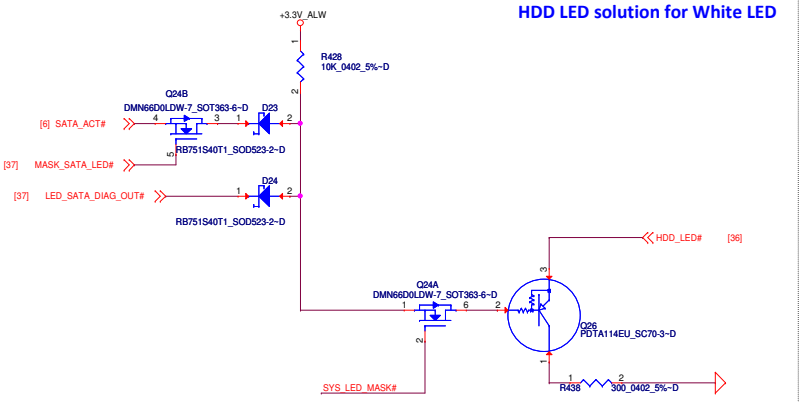
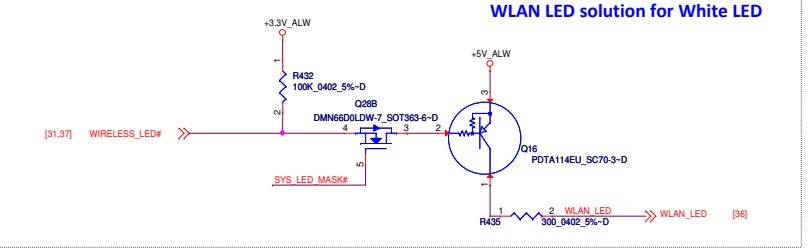
HDD LED solution for White LED

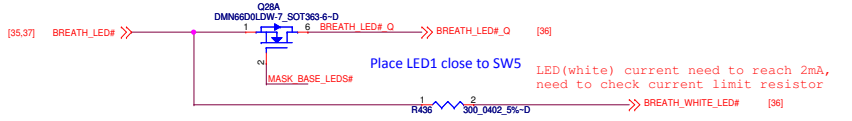


WLAN LED solution for White LED

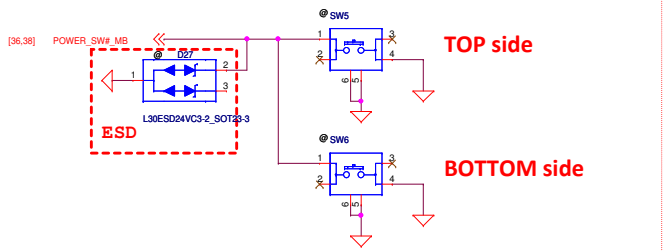


Battery LED

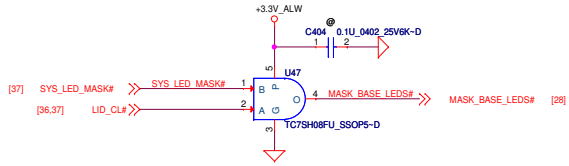
Breath LED

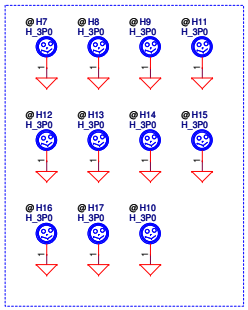


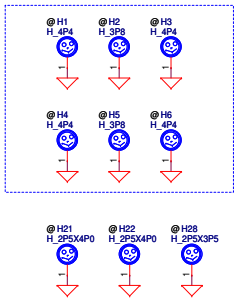
POWER & INSTANT ON SWITCH

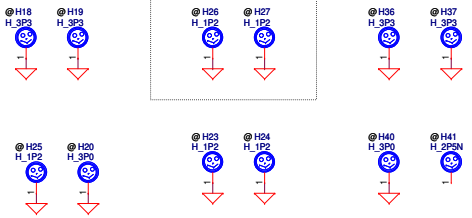


Lid has beed moved to DB.

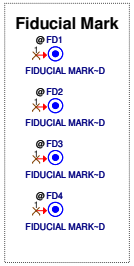








Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

ZZZ

DA8000WA000

Compal Electronics, Inc.

Title: PAD & ME & LED

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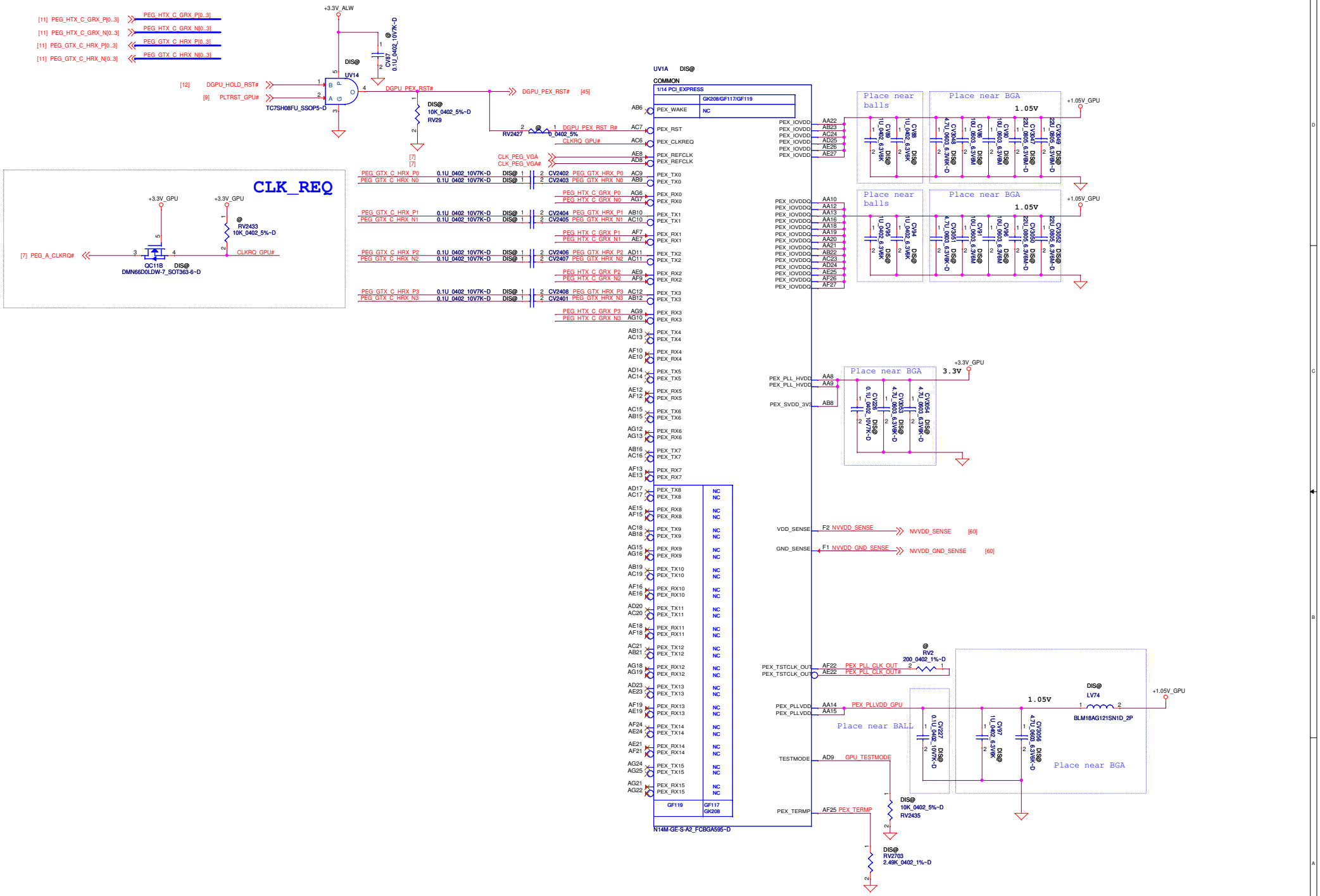

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Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **NV(1/5)-PCIE EXPRESS**

Size	Document Number	Rev
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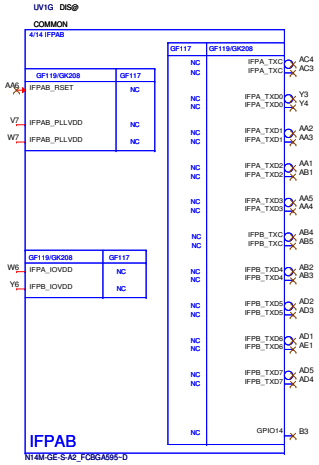
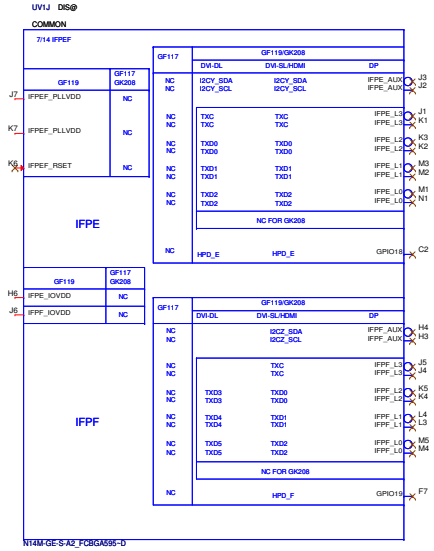
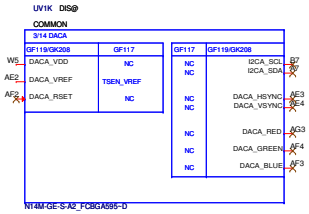
IFPA/B



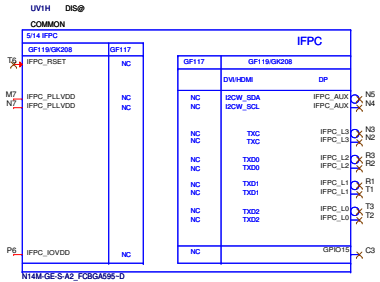
IFPE/F



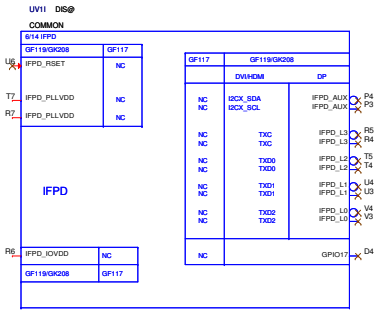
DAC_A



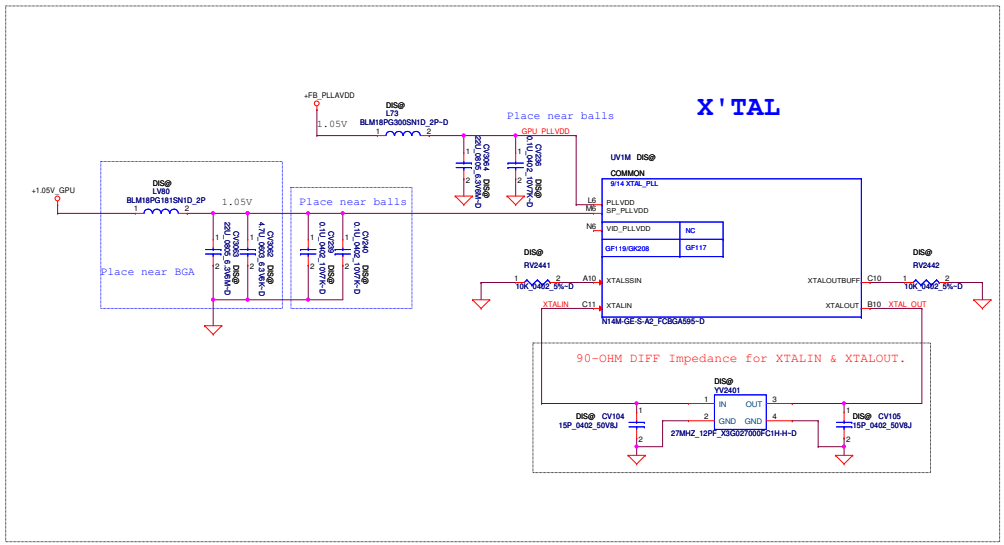
IFPC



IFPD



X'TAL



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	NV(2/5)-IFP_ABCDEF_DAC_XTAL		
Size: Custom	Document Number: LA-A101P		Rev: 1.0
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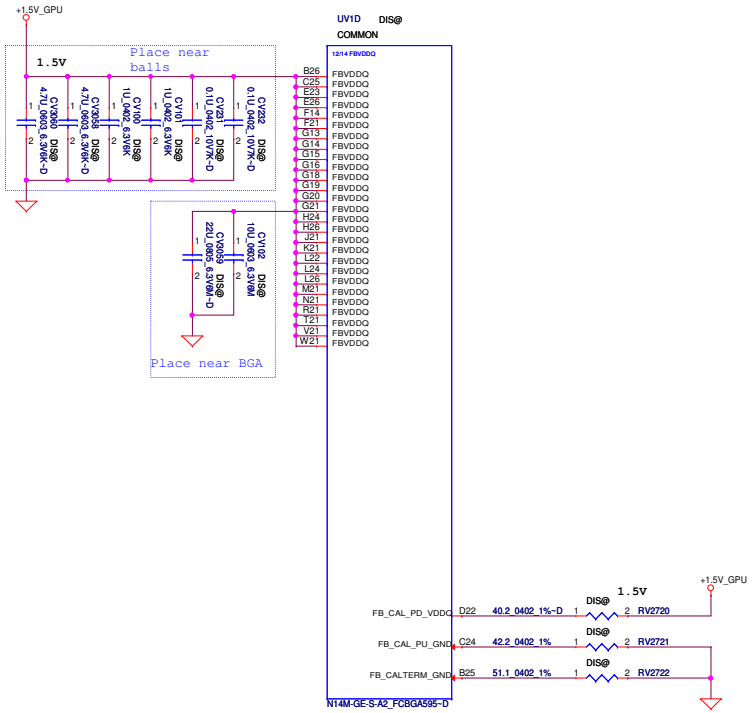
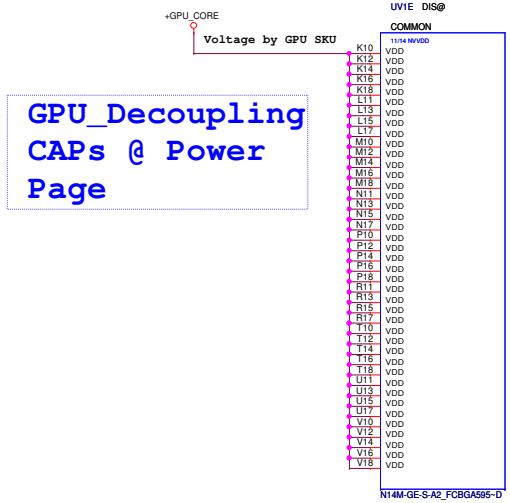
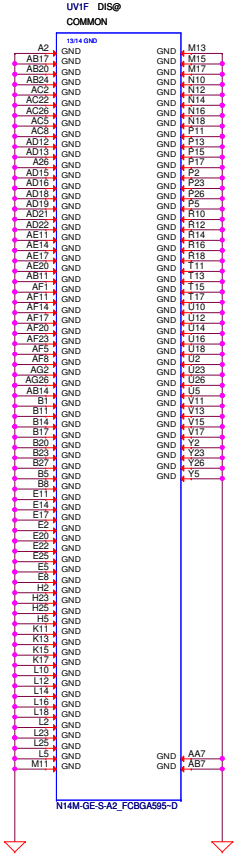
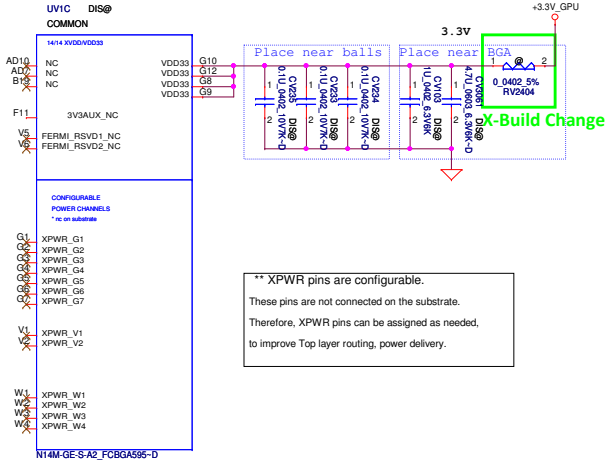




GPU_Decoupling CAPs @ Power Page





** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

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Compal Electronics, Inc.

Title: NV(3/5)-POWER_GND

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GPIO

VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

For Boundary Scan using.

UV1N DIS@
COMMON
8/14 MISC1

THERMDN E12
THERMDP F12

@T186 GPU_JTAG_TCK AE5 JTAG_TCK
@T187 GPU_JTAG_TMS AD6 JTAG_TMS
@T188 GPU_JTAG_TDI AE6 JTAG_TDI
@T189 GPU_JTAG_TDO AF6 JTAG_TDO
@T190 GPU_JTAG_TRST# AG4 JTAG_TRST

RV88 10K_0402_5% DIS@

I2CS_SCL D9 I2CS_SCL 2.2K 0402 5%~D RV49 +3.3V_GPU
I2CS_SDA D8 I2CS_SDA 2.2K 0402 5%~D RV50
I2CC_SCL A9 I2CC_SCL 2.2K 0402 5%~D RV45
I2CC_SDA B9 I2CC_SDA 2.2K 0402 5%~D RV46

GF117	GF119 GK208
NC	I2CB_SCL C9
NC	I2CB_SDA C8

GPIO0 C6
GPIO1 C2
GPIO2 D6
GPIO3 C7
GPIO4 C9
GPIO5 A3
GPIO6 A4
GPIO7 B6
GPIO8 A6 GPIO8_THERMATRIP# RV48 DIS@ 100K_0402_5%~D
GPIO9 F8 GPIO09_GPUHOT# RV34 DIS@ 100K_0402_5%~D
GPIO10 C3
GPIO11 E7 GPIO11_NVVDD_VID_R
GPIO12 D7 GPIO12_AC_DETECT RV35 DIS@ 100K_0402_5%~D
GPIO13 B4 GPIO13_NVVDD_PSI_R RV2446 DIS@ 100K_0402_5%~D

GK208	GF117	GF119
GPIO16	NC	GPIO16 D5
GPIO20	NC	GPIO20 C5
GPIO8	NC	GPIO21 C4

N14M-GE-S-A2_FCBGA595~D

I2CS SMBUS: 0x9E

I2CS_SCL → QC9A DIS@ DMN66D0LDW-7_SOT363-6-D → GPU_SMBCLK [38]
I2CS_SDA → QC9B DIS@ DMN66D0LDW-7_SOT363-6-D → GPU_SMBDAT [38]

DGPU_PEX_RST# → DIS@ R346 0_0402_5%~D → @ R347 0_0402_5%~D → +3.3V_GPU

GPIO8_THERMATRIP# → QC6A DIS@ DMN66D0LDW-7_SOT363-6-D → THERMATRIP3# [38,60]

GPIO11_NVVDD_VID_R → QC6B DIS@ DMN66D0LDW-7_SOT363-6-D → GPIO11_NVVDD_VID [37,60]

GPIO12_AC_DETECT → QC8A DIS@ DMN66D0LDW-7_SOT363-6-D
@ R344 0_0402_5%~D → ACAV_IN [38,58,59]
DIS@ R345 0_0402_5%~D → GPU_PWR_LEVEL [37]

GPIO13_NVVDD_PSI_R → QC8B DIS@ DMN66D0LDW-7_SOT363-6-D → GPIO13_NVVDD_PSI [60]

GPIO09_GPUHOT# → QC11A DIS@ DMN66D0LDW-7_SOT363-6-D → GPUHOT# [37,60]

UV1L DIS@
COMMON
10/14 MISC2

GF117/GF119/GK208	
VMON_IN0 E10	NC
VMON_IN1 F10	NC

STRAP0 D1 STRAP0
STRAP1 D2 STRAP1
STRAP2 E4 STRAP2
STRAP3 E3 STRAP3
STRAP4 D3 STRAP4

GF119	GF117 GK208
STRAP5_NC C1	NC

STRAPREF0 F6 MULTISTRAP_REF0_GND
MULTISTRAP_REF1_GND F4
MULTISTRAP_REF2_GND F5

GF119	GF117 GK208
MULTISTRAP_REF1_GND	NC
MULTISTRAP_REF2_GND	NC

@ RV2723 40.2K_0402_1%~D

De-POP RV2723 for N14M-GE and Binary Strap Mode

ROM_CS D12
ROM_SI B12 ROM_SI
ROM_SO A12 ROM_SO
ROM_SCLK C12 ROM_SCLK

BUFRST D11 RV2444 DIS@ 10K_0402_5%~D

NC	PGOOD D10
GF117 GK208	GF119

NC	CEC E9
GF117 GK208 GF119	

N14M-GE-S-A2_FCBGA595~D

ROM_SI
ROM_SO
ROM_SCLK

10K_0402_1%~D RV89 DIS@
10K_0402_1%~D RV92 DIS@
10K_0402_1%~D RV90 DIS@

STRAP

STRAP[3:0]
RAM_CF[3:0]
(Micron) MT41K256M16HA-107GM: 0xD = 1101
(Hynix) H5TC4G63AFR-11C: 0x4 = 0100

+3.3V_GPU

@ 10K_0402_1%~D RV94
X76@ RV2651 10K_0402_1%~D
X76@ RV2647 10K_0402_1%~D
X76@ RV2649 10K_0402_1%~D
X76@ RV2653 10K_0402_1%~D

STRAP0
STRAP1
STRAP2
STRAP3
STRAP4

DIS@ 10K_0402_1%~D RV93
X76@ RV2652 10K_0402_1%~D
X76@ RV2648 10K_0402_1%~D
X76@ RV2650 10K_0402_1%~D
X76@ RV2654 10K_0402_1%~D

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.
Title: NV(4/5)-GPIO_BIOS_STRAP
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UV1B DIS@

N14M-GE-S-A2_FCBGA595~D

COMMON

2/14 FBA

[47] FBA_D[0..31]

[48] FBA_D[32..63]

FBA_D0	E18	FBA_D0	
FBA_D1	F18	FBA_D1	
FBA_D2	E16	FBA_D2	
FBA_D3	F17	FBA_D3	
FBA_D4	D20	FBA_D4	
FBA_D5	D21	FBA_D5	
FBA_D6	F20	FBA_D6	
FBA_D7	E21	FBA_D7	
FBA_D8	E15	FBA_D8	
FBA_D9	D15	FBA_D9	
FBA_D10	F15	FBA_D10	
FBA_D11	F13	FBA_D11	
FBA_D12	C13	FBA_D12	
FBA_D13	B13	FBA_D13	
FBA_D14	E13	FBA_D14	
FBA_D15	D13	FBA_D15	
FBA_D16	B15	FBA_D16	
FBA_D17	C16	FBA_D17	
FBA_D18	A13	FBA_D18	
FBA_D19	A15	FBA_D19	
FBA_D20	B18	FBA_D20	
FBA_D21	A18	FBA_D21	
FBA_D22	A19	FBA_D22	
FBA_D23	C19	FBA_D23	
FBA_D24	B24	FBA_D24	
FBA_D25	C23	FBA_D25	
FBA_D26	A25	FBA_D26	
FBA_D27	A24	FBA_D27	
FBA_D28	A21	FBA_D28	
FBA_D29	B21	FBA_D29	
FBA_D30	C20	FBA_D30	
FBA_D31	C21	FBA_D31	
FBA_D32	R22	FBA_D32	
FBA_D33	R24	FBA_D33	
FBA_D34	T22	FBA_D34	
FBA_D35	R23	FBA_D35	
FBA_D36	N25	FBA_D36	
FBA_D37	N26	FBA_D37	
FBA_D38	N23	FBA_D38	
FBA_D39	N24	FBA_D39	
FBA_D40	V23	FBA_D40	
FBA_D41	V22	FBA_D41	
FBA_D42	T23	FBA_D42	
FBA_D43	U22	FBA_D43	
FBA_D44	Y24	FBA_D44	
FBA_D45	AA24	FBA_D45	
FBA_D46	Y22	FBA_D46	
FBA_D47	AA23	FBA_D47	
FBA_D48	AD27	FBA_D48	
FBA_D49	AB25	FBA_D49	
FBA_D50	AD26	FBA_D50	
FBA_D51	AC25	FBA_D51	
FBA_D52	AA27	FBA_D52	
FBA_D53	AA26	FBA_D53	
FBA_D54	W26	FBA_D54	
FBA_D55	Y25	FBA_D55	
FBA_D56	R26	FBA_D56	
FBA_D57	T25	FBA_D57	
FBA_D58	N27	FBA_D58	
FBA_D59	R27	FBA_D59	
FBA_D60	V26	FBA_D60	
FBA_D61	V27	FBA_D61	
FBA_D62	W27	FBA_D62	
FBA_D63	W25	FBA_D63	

[47] DQMA[3..0]

[48] DQMA[7..4]

DQMA0	D19	FBA_DQM0
DQMA1	D14	FBA_DQM1
DQMA2	C17	FBA_DQM2
DQMA3	C22	FBA_DQM3
DQMA4	P24	FBA_DQM4
DQMA5	W24	FBA_DQM5
DQMA6	AA25	FBA_DQM6
DQMA7	U25	FBA_DQM7

[47] QSA[3..0]

[48] QSA[7..4]

QSA0	E19	FBA_DQS_WP0
QSA1	C15	FBA_DQS_WP1
QSA2	B16	FBA_DQS_WP2
QSA3	B22	FBA_DQS_WP3
QSA4	R25	FBA_DQS_WP4
QSA5	W23	FBA_DQS_WP5
QSA6	AB26	FBA_DQS_WP6
QSA7	T26	FBA_DQS_WP7

[47] QSA#[3..0]

[48] QSA#[7..4]

QSA#0	F19	FBA_DQS_RN0
QSA#1	C14	FBA_DQS_RN1
QSA#2	A16	FBA_DQS_RN2
QSA#3	A22	FBA_DQS_RN3
QSA#4	P25	FBA_DQS_RN4
QSA#5	W22	FBA_DQS_RN5
QSA#6	AB27	FBA_DQS_RN6
QSA#7	T27	FBA_DQS_RN7

For VRAM DEBUG using

@ T171 FB_VREF D23 FB_VREF_PROBE

NC	FB_CLAMP F3
GF119	GF117/GK208

DIS@ RV2436 10K_0402_5%~D

FB_PLLAVDD	FB_DLLAVDD H22
GF117	GF119/GK208

FBA_CMD[0..31] [47,48]

FBA_CMD0	C27	FBA_CMD0
FBA_CMD1	C26	SNN_FBA_CMD1
FBA_CMD2	E24	FBA_CMD2
FBA_CMD3	F24	FBA_CMD3
FBA_CMD4	D27	FBA_CMD4
FBA_CMD5	D26	FBA_CMD5
FBA_CMD6	F25	FBA_CMD6
FBA_CMD7	F26	FBA_CMD7
FBA_CMD8	F23	FBA_CMD8
FBA_CMD9	G22	FBA_CMD9
FBA_CMD10	G23	FBA_CMD10
FBA_CMD11	G24	FBA_CMD11
FBA_CMD12	F27	FBA_CMD12
FBA_CMD13	G25	FBA_CMD13
FBA_CMD14	G27	FBA_CMD14
FBA_CMD15	G26	FBA_CMD15
FBA_CMD16	M24	FBA_CMD16
FBA_CMD17	M23	SNN_FBA_CMD17
FBA_CMD18	K24	FBA_CMD18
FBA_CMD19	K23	FBA_CMD19
FBA_CMD20	M27	FBA_CMD20
FBA_CMD21	M26	FBA_CMD21
FBA_CMD22	M25	FBA_CMD22
FBA_CMD23	K26	FBA_CMD23
FBA_CMD24	K22	FBA_CMD24
FBA_CMD25	J23	FBA_CMD25
FBA_CMD26	J25	FBA_CMD26
FBA_CMD27	J24	FBA_CMD27
FBA_CMD28	K27	FBA_CMD28
FBA_CMD29	K25	FBA_CMD29
FBA_CMD30	J27	FBA_CMD30
FBA_CMD31	J26	SNN_FBA_CMD31

FBA_RST

FBA_CMD5 — DIS@ 10K_0402_5%~D RV2447

FBA_DOT_L — FBA_CMD2

FBA_DOT_H — FBA_CMD18

FBA_CKE_L — FBA_CMD3

FBA_CKE_H — FBA_CMD19

RV2437 DIS@ 10K_0402_1%~D

RV2438 DIS@ 10K_0402_1%~D

RV2439 DIS@ 10K_0402_1%~D

RV2440 DIS@ 10K_0402_1%~D

FBVDDQ_GPU

+1.5V_GPU

@ RV2704 60.4_0402_1%~D 1.5V

FBA_DEBUG0 F22

FBA_DEBUG1 J22

60.4_0402_1%~D RV2705 @

FBA_CLK0	D24	CLKA0	CLKA0 [47]
FBA_CLK0#	D25	CLKA0#	CLKA0# [47]
FBA_CLK1	N22	CLKA1	CLKA1 [48]
FBA_CLK1#	M22	CLKA1#	CLKA1# [48]

FBA_WCK01	D18	SNN_FBA_WCK01
FBA_WCK01#	C18	SNN_FBA_WCK01#
FBA_WCK23	D17	SNN_FBA_WCK23
FBA_WCK23#	D16	SNN_FBA_WCK23#
FBA_WCK45	T24	SNN_FBA_WCK45
FBA_WCK45#	U24	SNN_FBA_WCK45#
FBA_WCK67	V24	SNN_FBA_WCK67
FBA_WCK67#	V25	SNN_FBA_WCK67#

+FB_PLLAVDD

FB_PLLAVDD F16

FB_PLLAVDD P22

+FB_PLLAVDD — 1.05V — DIS@ LV76 BLM18PG300SN1D_2P~D — +1.05V_GPU

CV228 0.1U_0402_10V7K~D DIS@

CV3057 22U_0805_6.3V6M~D DIS@

Place near BALL

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(5/5)-MEMORY FBA

Size: Custom | Document Number: LA-A101P | Rev: 1.0

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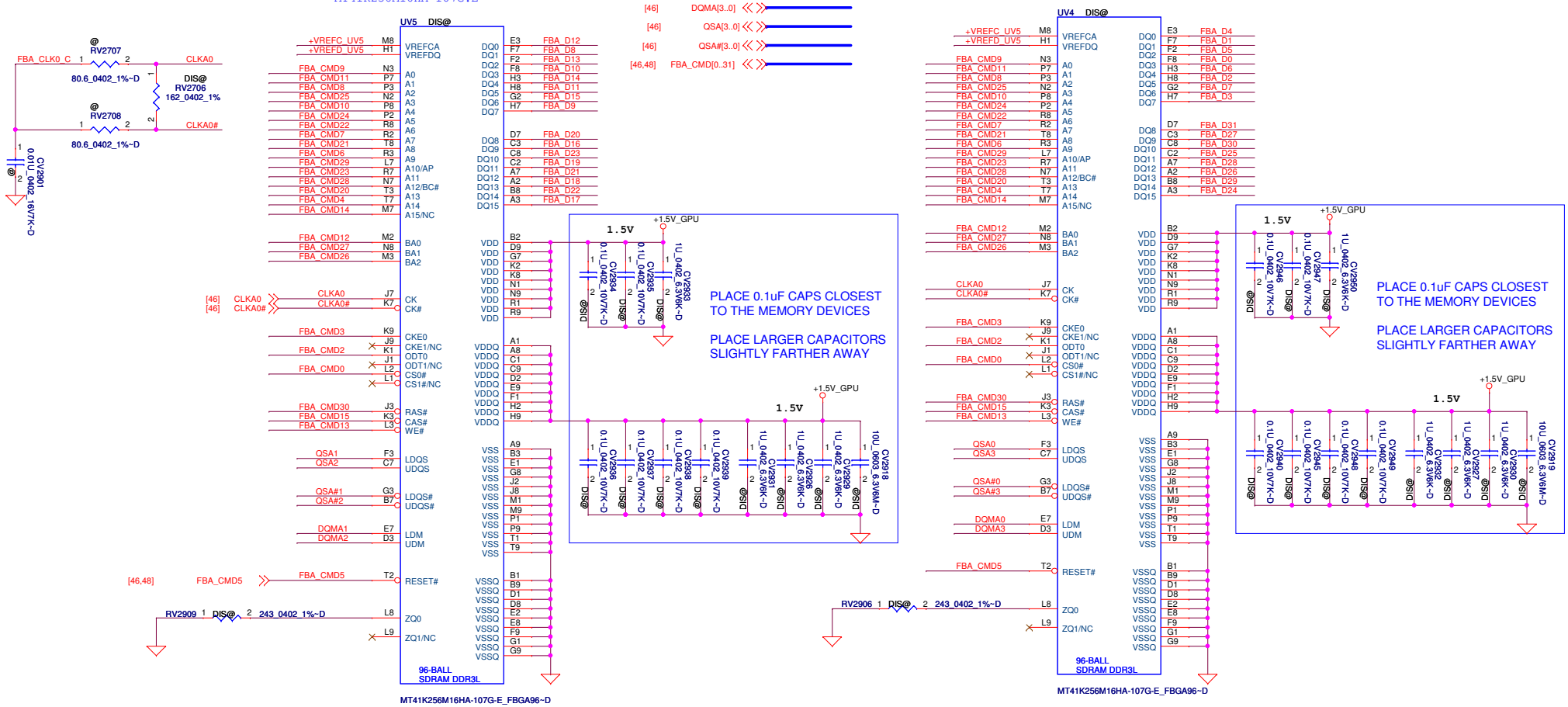
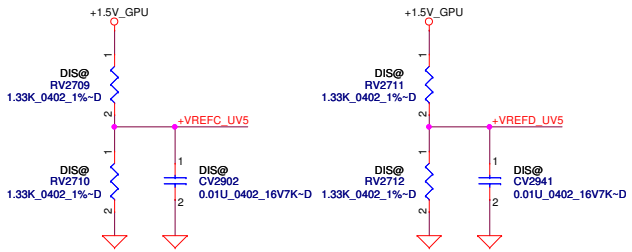
Memory Partition A - Lower 32 bits [31..0]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

[46] FBA_D[0..31]
[46] DQMA[3..0]
[46] QSA[3..0]
[46] QSA#[3..0]
[46,48] FBA_CMD[0..31]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E





HYNIX
UV5 PCB-MB X76_HYN@
UV4 PCB-MB X76_HYN@

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title: VRAM_DDR3_A Lower			
Size: Custom	Document Number: LA-A101P		Rev: 1.0
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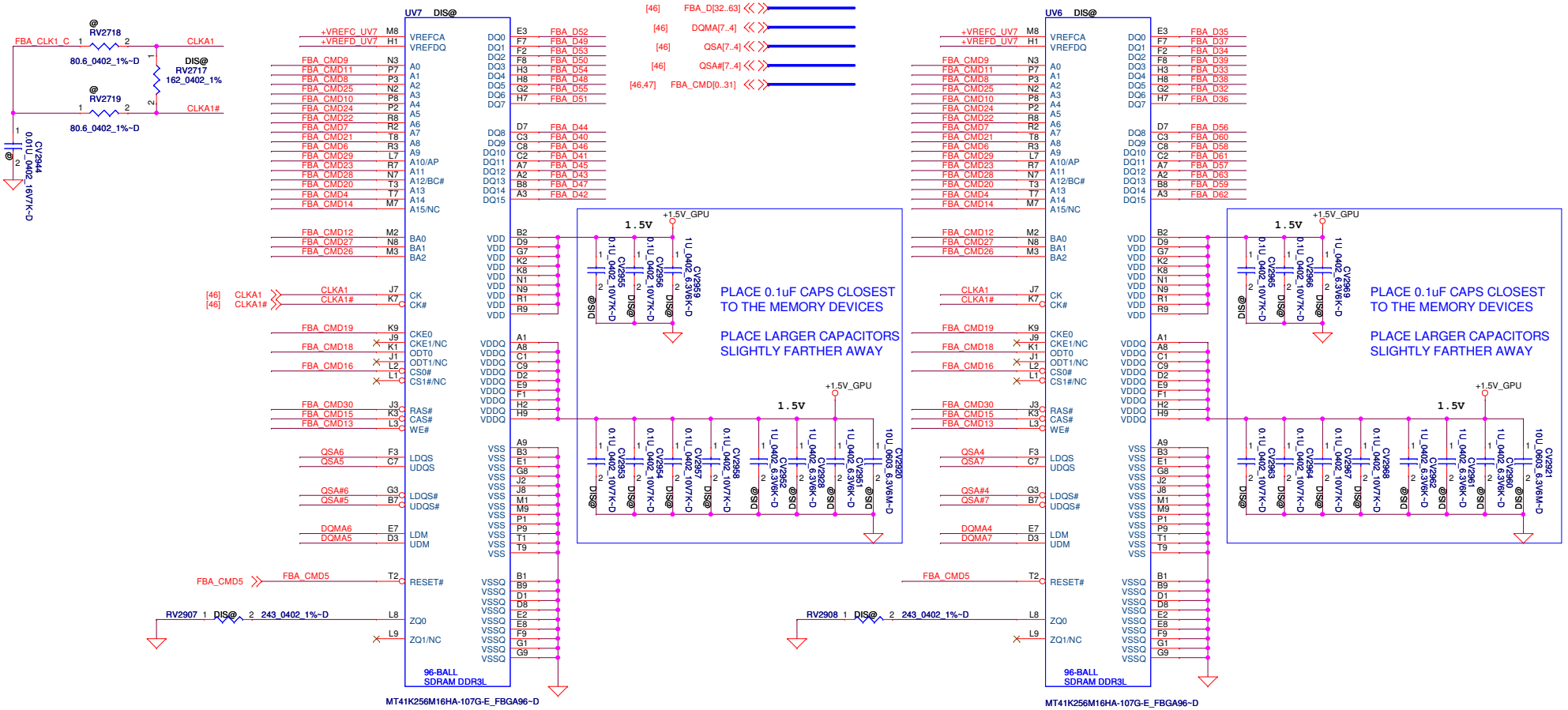
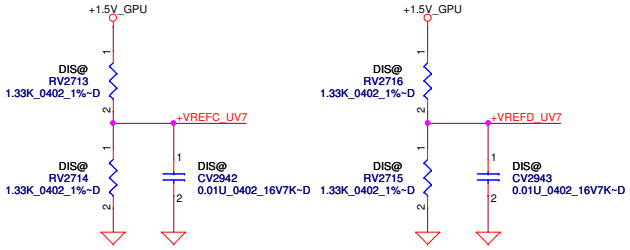
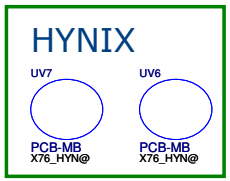
Memory Partition A – Upper 32 bits [64..32]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E







A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: VRAM_DDR3_A Upper

Size	Document Number	Rev
Custom	LA-A101P	1.0

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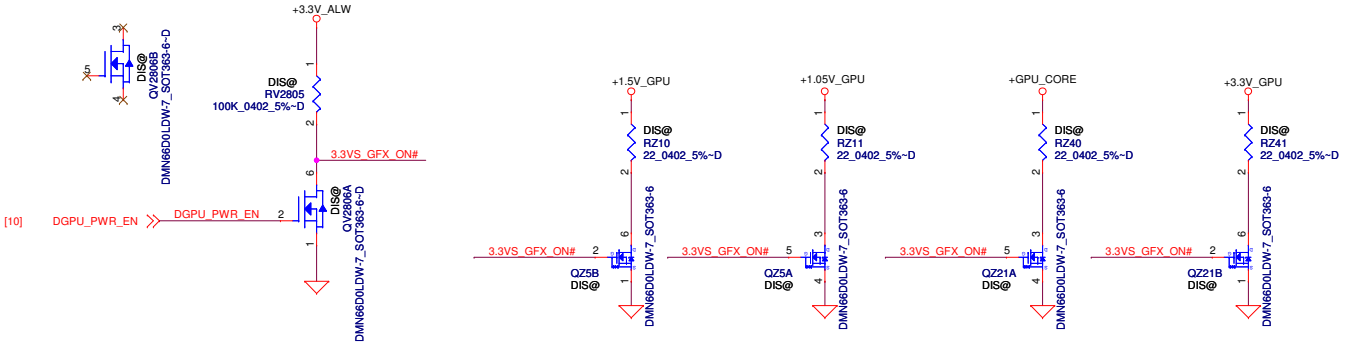
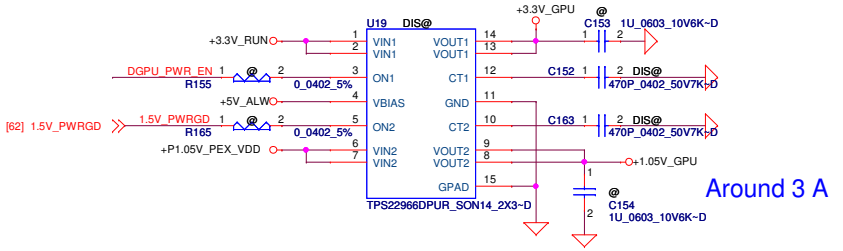
GPU Power Discharge Path



+3.3VRUN to +3.3V_RUN_GFX

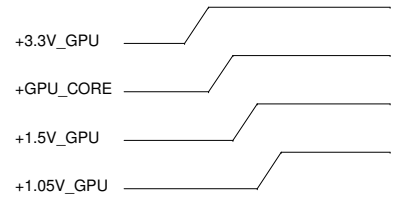
Around 1.4 A



Around 3 A

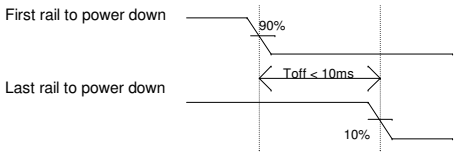
+1.05V_MP to +1.05V_PEX_VDD

GPU Power Up Power Rail Sequence

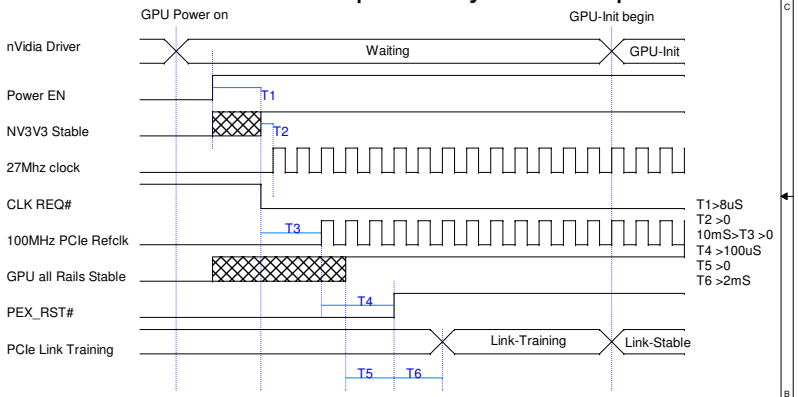


The ramp time for any rail must be more than 40us.

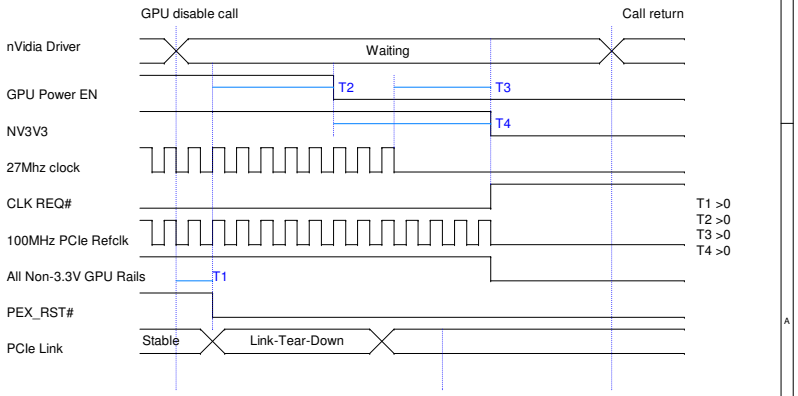
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.	
Title	VGA_DC/DC Interface
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Title: BLANK PAGE

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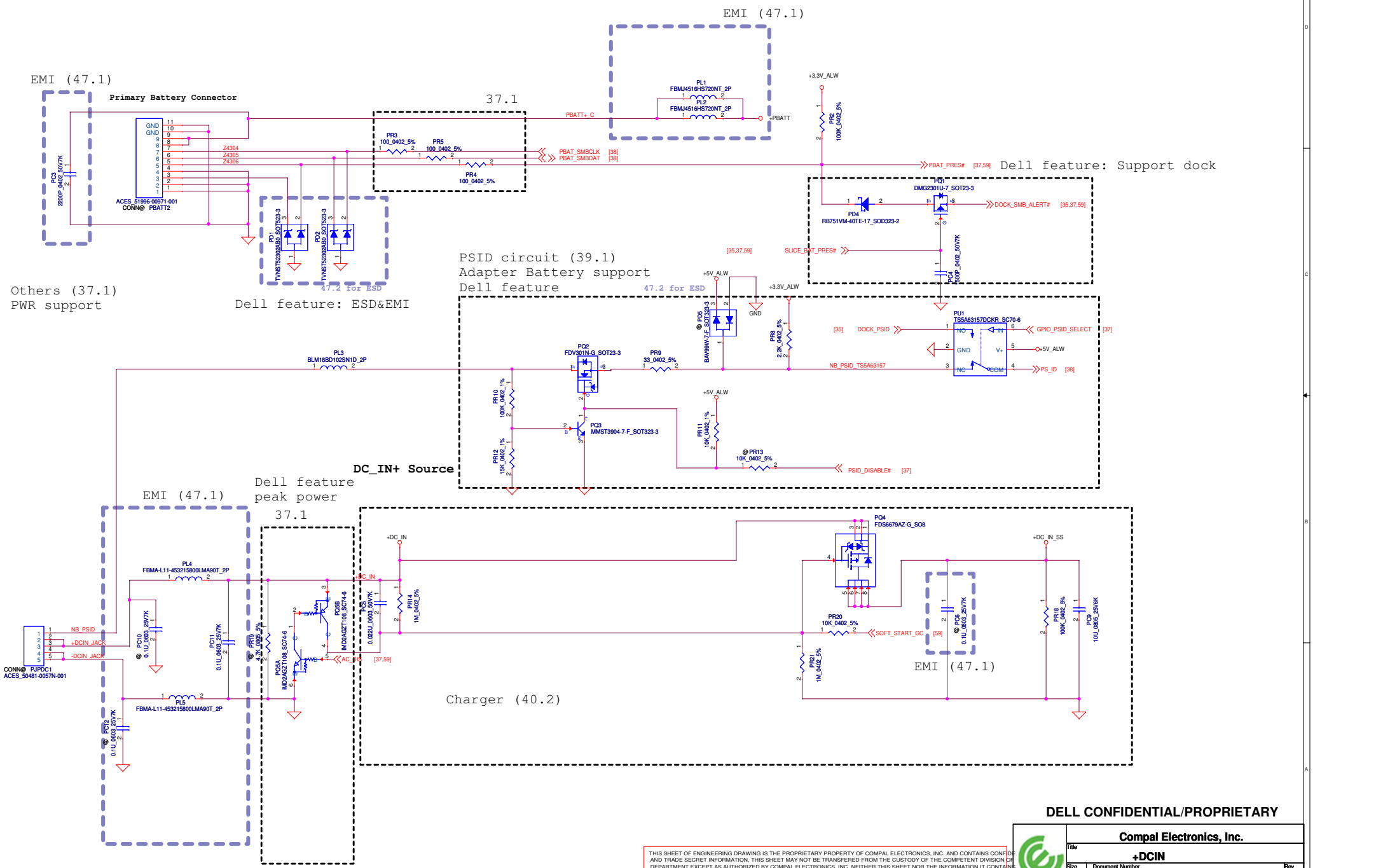

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Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-A101P	Rev: 1.0
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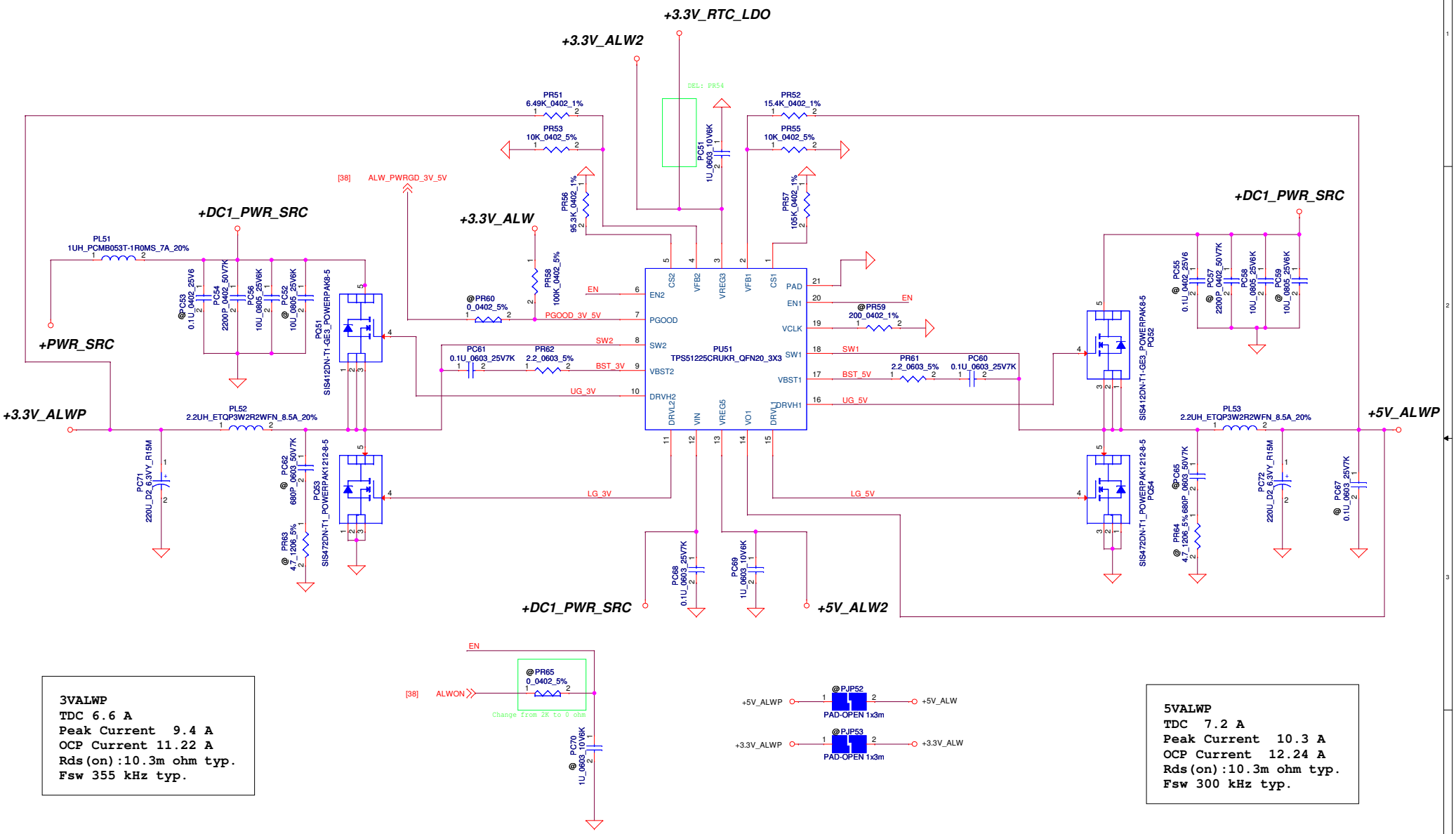

3VALWP
TDC 6.6 A
Peak Current 9.4 A
OCP Current 11.22 A
Rds(on):10.3m ohm typ.
Fsw 355 kHz typ.

5VALWP
TDC 7.2 A
Peak Current 10.3 A
OCP Current 12.24 A
Rds(on):10.3m ohm typ.
Fsw 300 kHz typ.

Compal Electronics, Inc.
Title: PWR_+5V_ALW/3.3V_ALW
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1.35Volt +/- 5%
TDC: 7.2 A
Peak Current: 10.3 A
OCP current: 12.24 A
Rds(on):14.5m ohm typ
Fsw

0.675Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.8925A

+PWR_SRC
@PJP100
PAD-OPEN 1x2m~D
1.35V_B+
PC100 10U_0805_25V6K
@PC101 10U_0805_25V6K
@PC102 0.1U_0402_25V6
PC103 2200P_0402_50V7K
PR100 2.2_0603_5%
BOOT_1.35V
DH_1.35V
SW_1.35V
DL_1.35V
PC104 0.22U_0603_16V7K
SI4128DY-T1-GE3_SO8 PQ100
SI4134DY-T1-GE3_SO8 PQ101
+1.35V_MEN_P
PL100 2.2UH_ETQP3W2R2WFN_8.5A_20%
PC116 330U_2.5V_M
PC109 @ 680P_0603_50V7K
SNUB_1.35V
@PR103 4.7_1206_5%
+5V_ALW
PR102 5.1_0603_5%
VDD_1.35V
PC111 1U_0603_10V6K
PR101 19.6K_0402_1%
CS_1.35V
PC107 1U_0603_10V6K
PU100 G5616ARZ1U_TQFN20_3X3
LX DH BST VLDOIN VTT PAD VTTGND VTTSNS GND VTTREF VDDQSNS VDDQSET PGOOD TON S5 S3 DL PGND CS VPP VCC
+VLDOIN_1.35V
@PJP101
PAD-OPEN1x1m
+1.35V_MEN_P
+0.675V_P
PC105 10U_0805_6.3V6M
PC106 10U_0805_6.3V6M
+V_DDR_REF
PC112 0.033U_0402_16V7K
FB sense trace
when FB pull down to GND
+1.35V_MEN_P
PR105 8.06K_0402_1%
1.35V_FB
PC113 100P_0402_50V8J
PR109 10K_0402_1%
@PC114 0.1U_0402_10V7K
FB sense trace
+3.3V_ALW
PR104 100K_0402_5%
[38] 1.35V_SUS_PWRGD
PR106 1M_0402_1%
1.35V_B+
@PR107 0_0402_5%
[37,40,55,9] SIO_SLP_S4#
S5_1.35V
@PR108 0_0402_5%
[37,40] SUS_ON
@PC115 0.1U_0402_10V7K
@PR110 0_0402_5%
[18] 0.675V_DDR_VTT_ON
@PR111 0_0402_5%
[36,37,40,9] SIO_SLP_S3#

Mode	S3	S5	+1.35V_MEN_P	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

@PJP102
JUMP_1x3m
+1.35V_MEN_P
@PJP103
JUMP_1x3m
+1.35V_MEM

+0.675V_P
@PJP104
PAD-OPEN1x1m
+0.675V_DDR_VTT

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Compal Electronics, Inc.
Title: PWR_+1.35V_MEN/+0.675V_DDR
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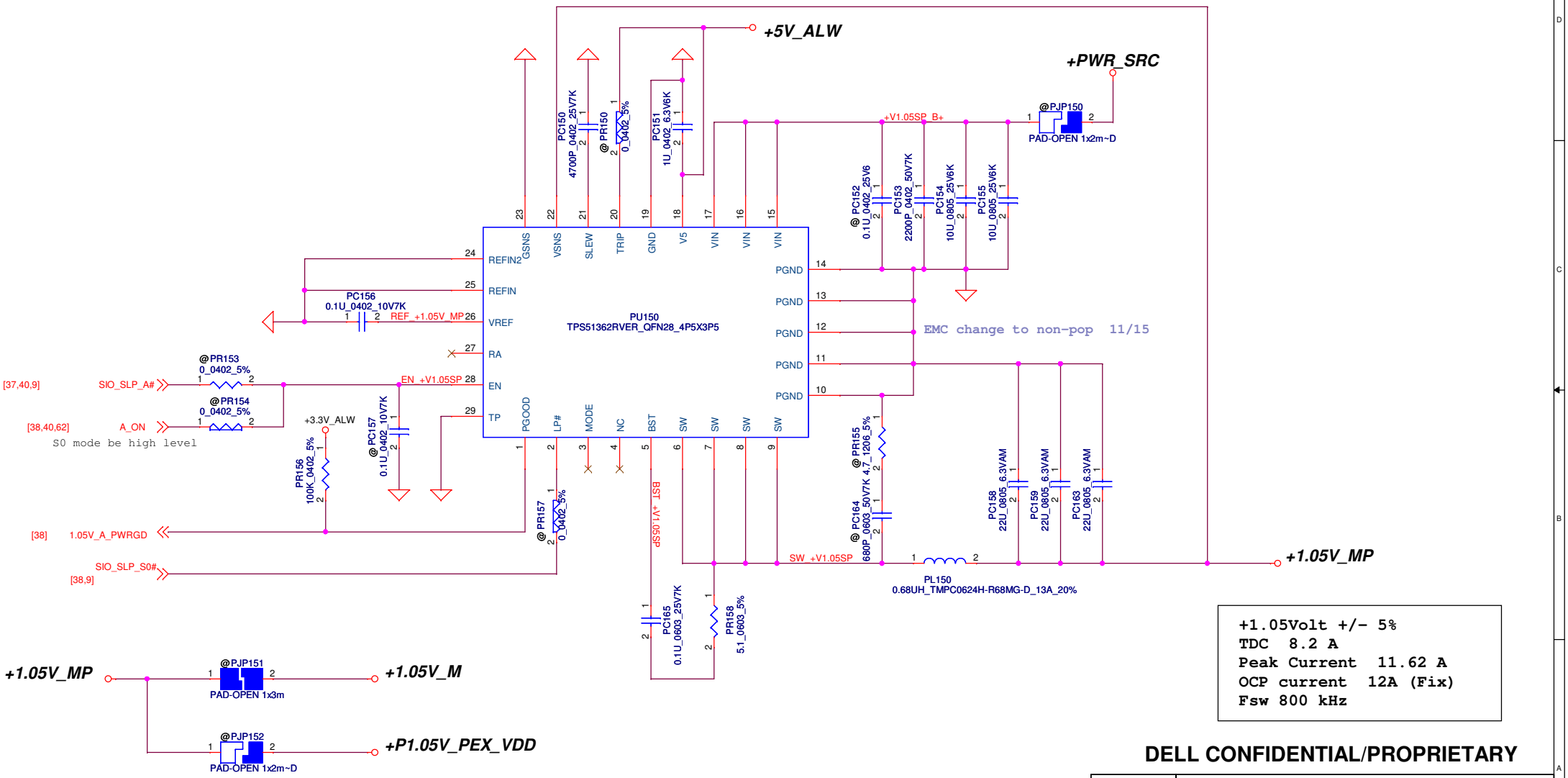

+1.05Volt +/- 5%
TDC 8.2 A
Peak Current 11.62 A
OCP current 12A (Fix)
Fsw 800 kHz

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Compal Electronics, Inc.		
Title: PWR_+1.05VTTP		
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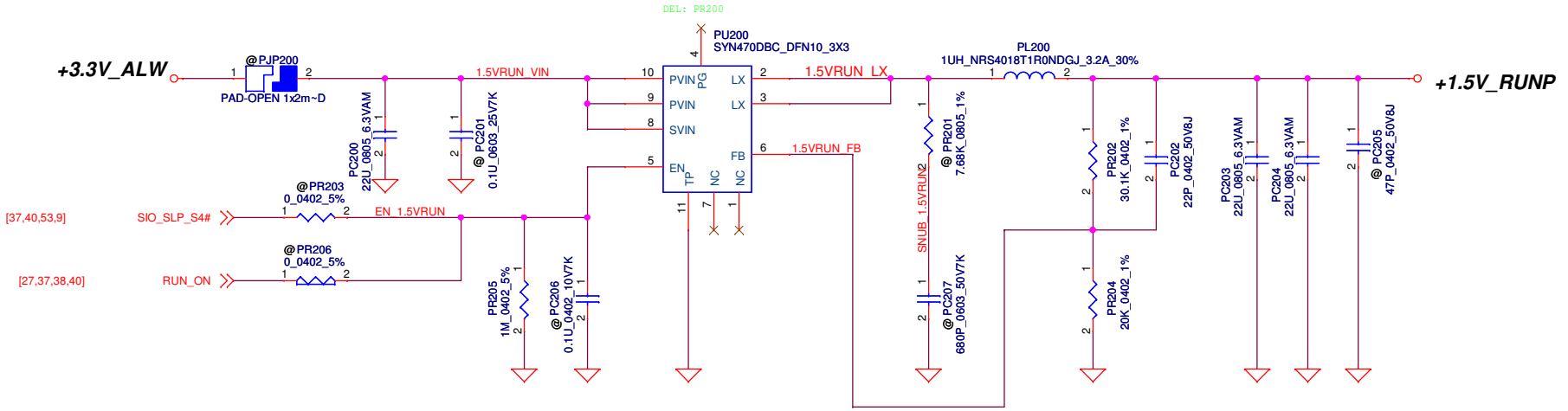
1.5Volt
Frequency 1MHz
TDC 0.65A
Peak Current 0.93A
OCP current 3.5A (Fix)



VFB=0.6V Vo=VFB*(1+PR202/PR204)=0.6*(1+30.1K/20K)=1.503V

+1.5V_RUNP @PJP201 PAD-OPEN 1x2m~D +1.5V_RUN

Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: PWR_1.5V_RUN

Size: B | Document Number | Rev: 1.0

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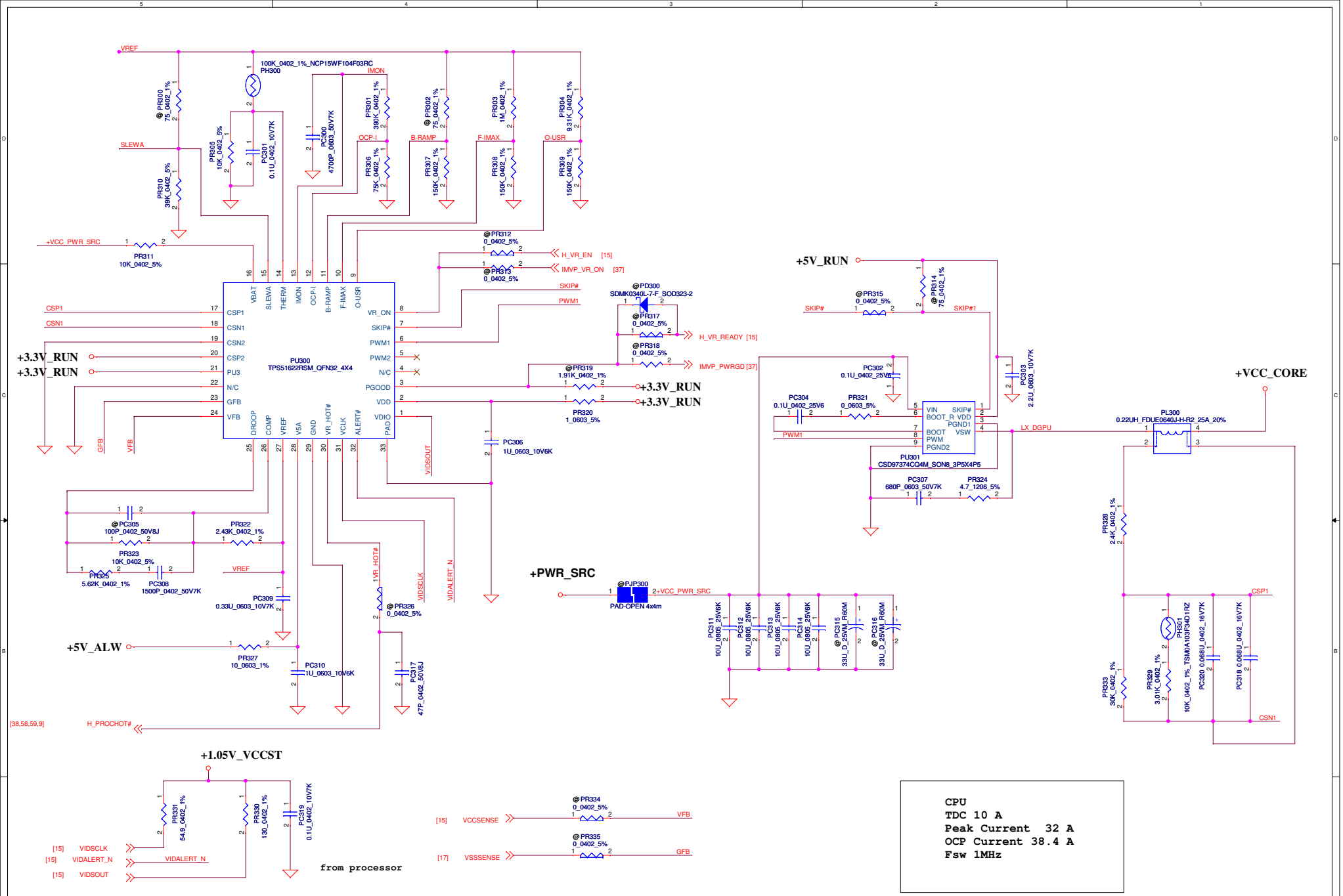

Compal Electronics, Inc.

Title: PWR_+VCC_CORE

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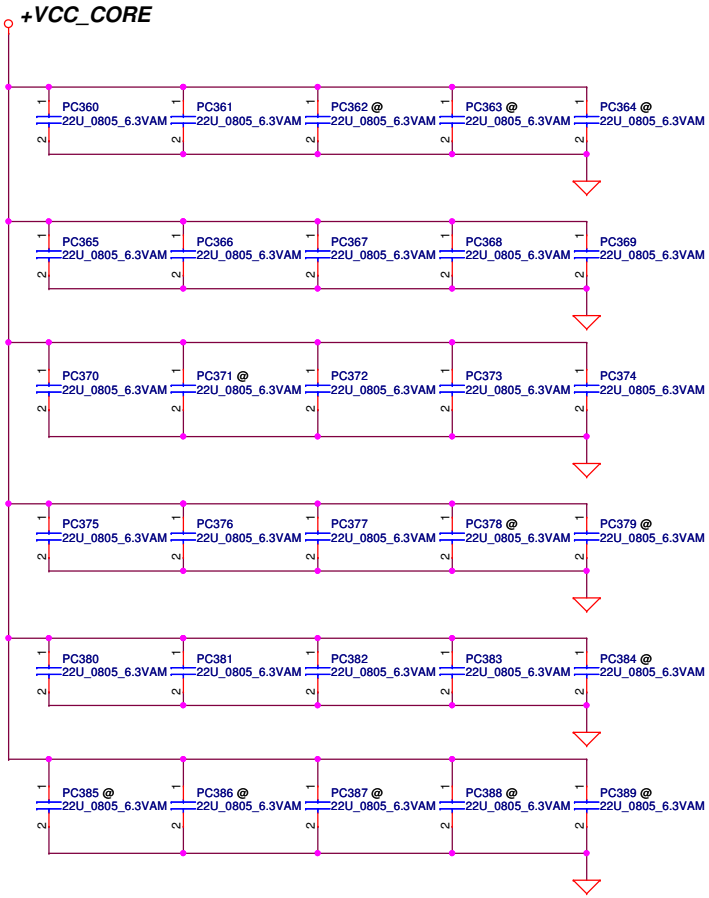

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Compal Electronics, Inc.		
Title: PWR_PROCESSOR DECOUPLING		
Size	Document Number: LA-A101P	Rev: 1.0
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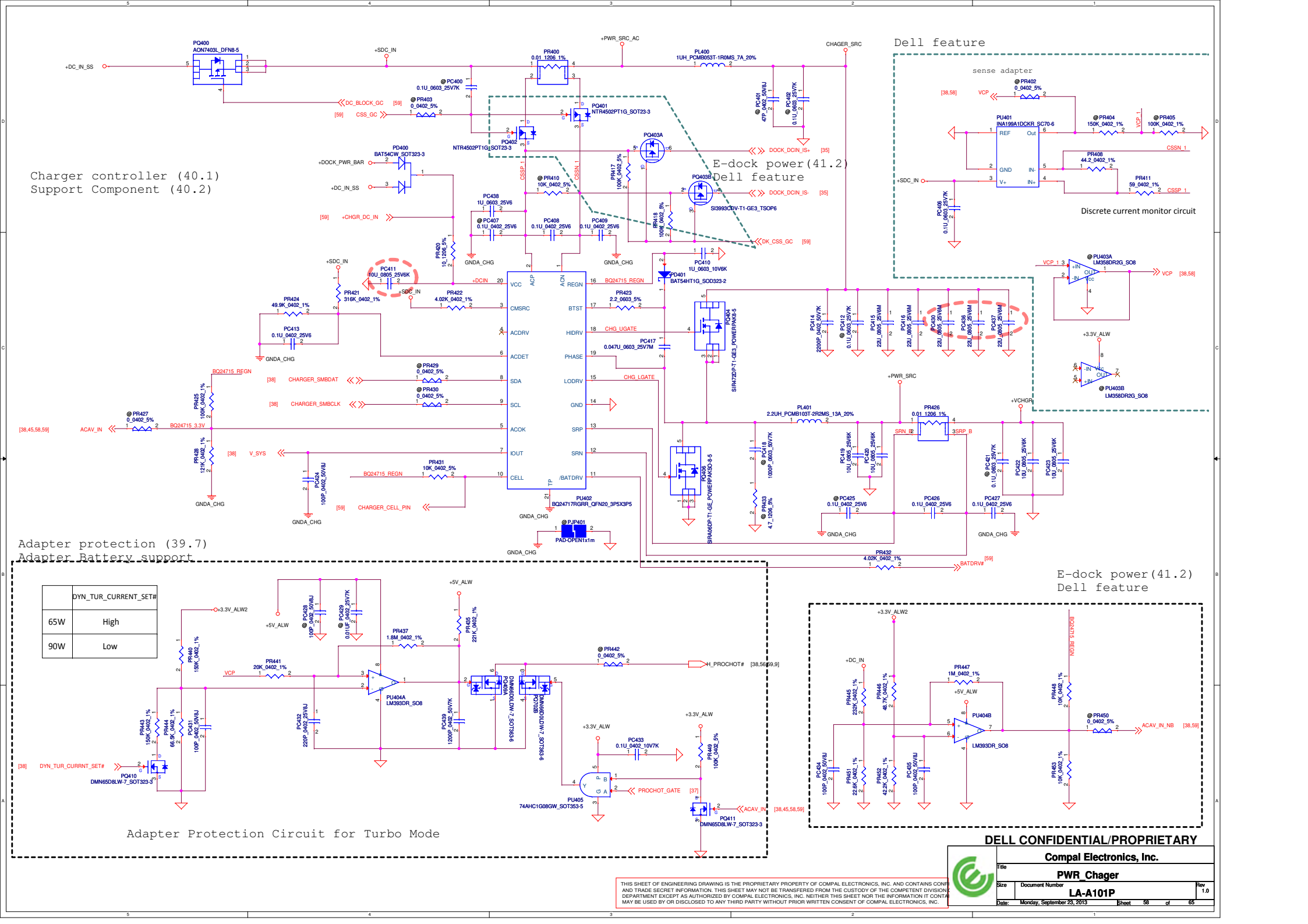

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Compal Electronics, Inc.

Title: PWR_Chager

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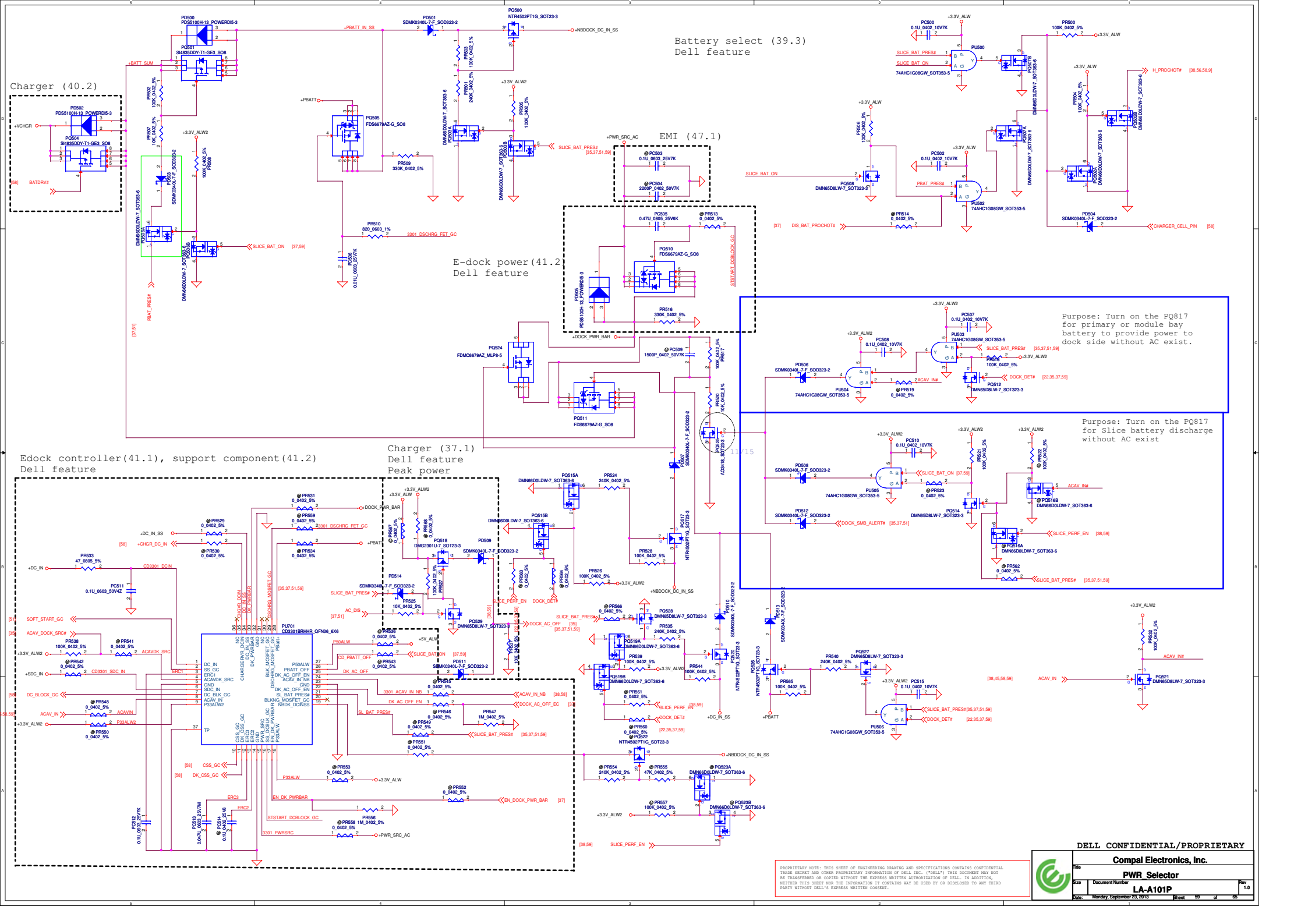
Charger (40.2)
Battery select (39.3)
Dell feature
EMI (47.1)
E-dock power(41.2
Dell feature
Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.
Purpose: Turn on the PQ817 for Slice battery discharge without AC exist
Edock controller(41.1), support component(41.2)
Dell feature
Charger (37.1)
Dell feature
Peak power
PU701
CD3301BRHHR_QFN36_6X6
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_Selector
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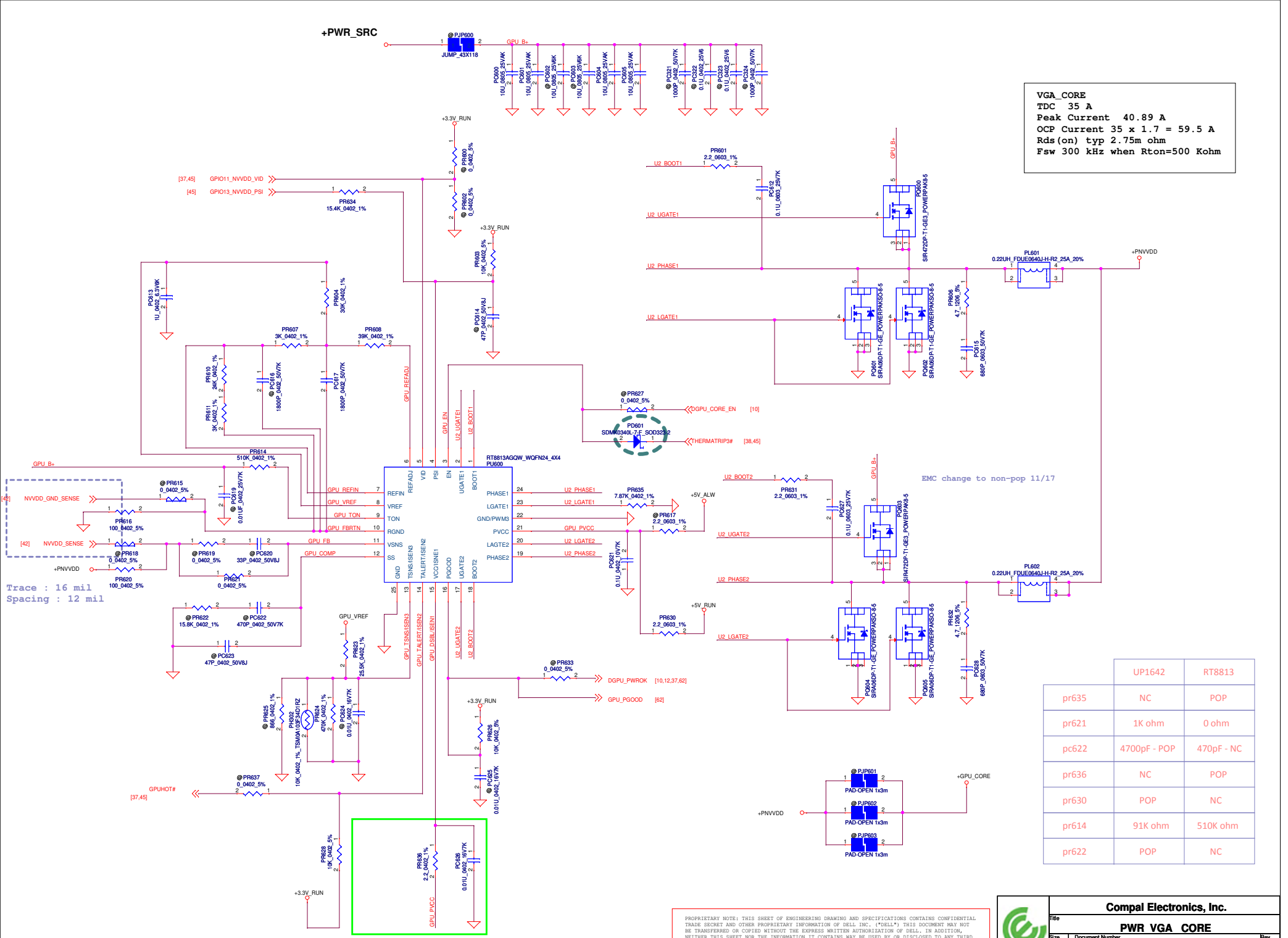

	UP1642	RT8813
pr635	NC	POP
pr621	1K ohm	0 ohm
pc622	4700pF - POP	470pF - NC
pr636	NC	POP
pr630	POP	NC
pr614	91K ohm	510K ohm
pr622	POP	NC

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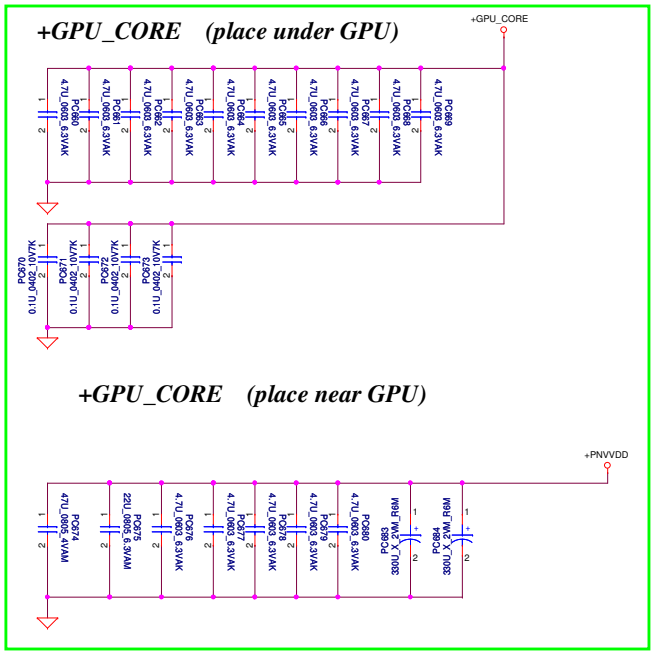

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Title: PWR_GPU_DECOUPLING

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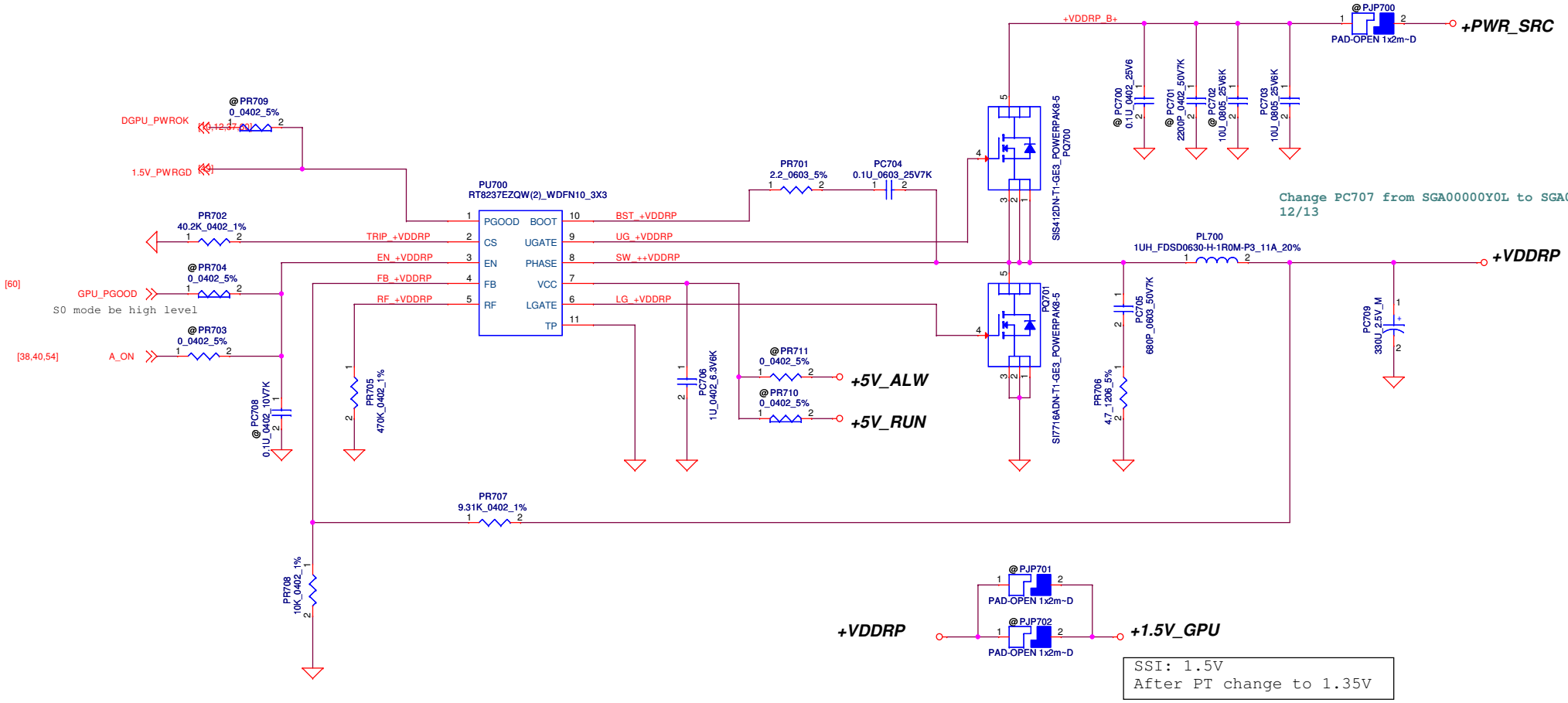

Compal Electronics, Inc.

Title	PWR_+1.5VDDR	
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VAW50 Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	58	Adapter Protection Circuit	2013/1/30	Power	PC432 220pF is not popular part	Change to 0402 size	X00
2	59	P59-PWR_Selector	2013/2/4	Power	Battery voltage leakage to docking if only battery	Add: PD513, PQ526, PR565, PR540, PQ527, PU506, PC515	X00
3	56	Vcore fine tune	2013/2/7	Power	Vcore fine tune	Modify: PR306, PR301, PR333, PR328, PR325, PR322, PL300	X00
4	57	Vcorecapacitor reduce	2013/2/7	Power	Vcore output capacitor reduce	NC: PC364, PC371, PC378, PC385, PC386	X00
5	58	Charger	2013/2/18	Power	Reserve H_PROCHOT# delay time fine tune by soft ware	Add "MODULE_BATT_PRES#" and PR454(Cancel 3/19)	X00
6	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 240K to 100K: PR503, PR528, PR544, PR565	X00
7	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 47K to 240K: PR501, PR524, PR535, PR540	X00
8	59	P59-PWR_Selector	2013/2/26	Power	SUT will unexpected shut down if un-docking during S0/S3	Add: PQ528, PR566	X00
9	51	"PBAT_PRES#" ESD fail	2013/3/4	Power	ESD PD1 fail, even connect 3.3V to VBUS pin	Change PD1 to PD1, PD2(TVNST52302AB0)	X00
10	59	P59-PWR_Selector	2013/3/6	Power	SB903380020 FDN338P derating fail	PQ500, PQ517,PQ520,PQ522,PQ526 change to SB000007900, PQ1change to SB00000PJX0	X00
11	51	PC5 down size	2013/3/12	Power	PC5 down size	Change PC5 from 0805 to 0603 size	X00
12	51,59	AC_DIS# net change	2013/3/12	Power	AC_DIS# should high enable, not low enable	AC_DIS# change to AC_DIS	X00
13		EMC open issue	2013/3/18	Power	Add parts for EMI	PR606,PC615, PR632, PC628, PR706, PC705, PR324, PC307	X00
14	60, 62	PU600, PU601 VCC	2013/3/19	Power	DIS S3 power consumption voer 200mW	Add PR630 PR711, PR710 for reserve +5V_RUN	X00
15	61	Change DGPU output cap	2013/3/19	Power	EA test fail- 15"	Change PC683,PC684	X00
16	62	GPU DDR change to 1.35V	2013/3/19	Power	Change VDDR output voltage from 1.5V to 1.35V	Change PR707 from 11.5K to 9.1K	X00
17	54	+1.05V dynamic load test	2013/3/19	Power	+1.05V dynamic load over spec	Change PL150 from 1uH to 0.68uH	X00
18	58	Change output chock	2013/3/20	Power	Same as 14" for height limit	Charger output choke change to 2.2uH	X00
19	60	0 ohm resistor	2013/3/21	Power	0 ohm 1% vender is not correct in ISPD	Change PR621 0ohm from 1% to 5%	X00
20	54	1.05V dynamic over spec	2013/3/21	Power	1.05V dynamic over spec	Change PL150 from 1uH to 0.68uH	X00
21	59	Modify for Peak power	2013/3/21	Power	Modify schematic	PQ529, PQ518, PR527 and PR567	X00
22	52	Del +5V_ALWP output cap co-layout	2013/5/7	Power	PL52, PL53 two choke placement too closely issue.	Del PC66 and fine tune PL52/53 location	X01
23	62	DGPU DDR voltage fine tune	2013/5/10	Power	VRAM 1.35V output fine tune from 1.342V to 1.36V	PR707 change from 9.1K to 9.31K	X01
24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	51	15" 組裝問題	2013/5/10	Power	PC9 short battery latch snap	Move location	X01
26	56	15" Vcore find tune	2013/5/29	Power	14" Vcore find tune for LL and DIMON	PR322=4.53K->2.43K; non-POP:PC379, PC388; POP:PC365, PC366	X02
27	59	Selector	2013/5/30	Power	For 3V/5V volgate level, change VDS rating from 30V to 20V	PQ1, PQ518 change to 20V rating DMG2301U-7_SOT23-3	X02
28	62	Thermal de-ratgin issue	2013/5/29	Power	MLCC are exceeded derating criteria (75C)	Change to X6S/X7R: PC600, PC601, PC604, PC605, PC674	X02
29	59	Change part number	2013/6/6	Power	Part number -N0 is for other customer	SE043474KN0 change to SE043474K80	X02
30	NA	15" NPI report request(,6/6)	2013/6/7	Power	Component pad too small	PL100/PL52/PL53/PL150 pad ?度change from 8 to 8.4mm	X02
31	NA	15" NPI report request(,6/6)	2013/6/7	Power	Co-lay need select 1 conponent	Del NC: PC681, PC682, PJP1,PL301,PC707, PC110, PC64,PJP400, PL600, PJP51	X02

VAW50 Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	27	Change to bead	2013/08/02	EMI	Populate bead 70 ohm(BLM15AG700SN1) on R137 and R139		1.0
2	27	音壓測試fail	2013/08/02	Safety	R162 , R166 change from 9.1 ohm to 18 ohm		1.0
3	9, 44	Change to short-pad	2013/08/02	EE	Location : RC194,RC204,RC208,RC209, RV2404		1.0
4	28	Change CPN	2013/08/02	EE	Type change to T & R	SA000066W4L	1.0
5	34	USB3.0 Re-driver	2013/08/02	EE	Pull-up and Pull-down resister	R2628, R2629, R2630, R2631, R2633, R2634, R2635, R2636, R2637, R2644	1.0
6	18, 19 31	Del Cap	2013/08/02	EE	Delete Co-Lay cap	C810, CD100, CD101	1.0
7	25	Modify footprint	2013/08/14	EE	Location : JSATA1	NPI	1.0
8	41	銅柱 Size	2013/08/22	EE	Location : H1, H2, H3, H4, H5, H6		1.0
9	16	BT issue	2013/08/22	EE	Add 0.47uF between “+PCH_VCCDSW3_3” and “+PCH_VCCDSW”	C413	1.0
10	36	EMI Request	2013/08/22	EMI	Add D2 on “Sleeve” & “Ring2” and connect to DGND		1.0
11	41	LED resister	2013/08/22	EE	Change to 300 ohm	R429, R433, R436, R438, R436	1.0
12	41	POWER BOTTON		EE	Un-pop power botton.	SW6	1.1

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