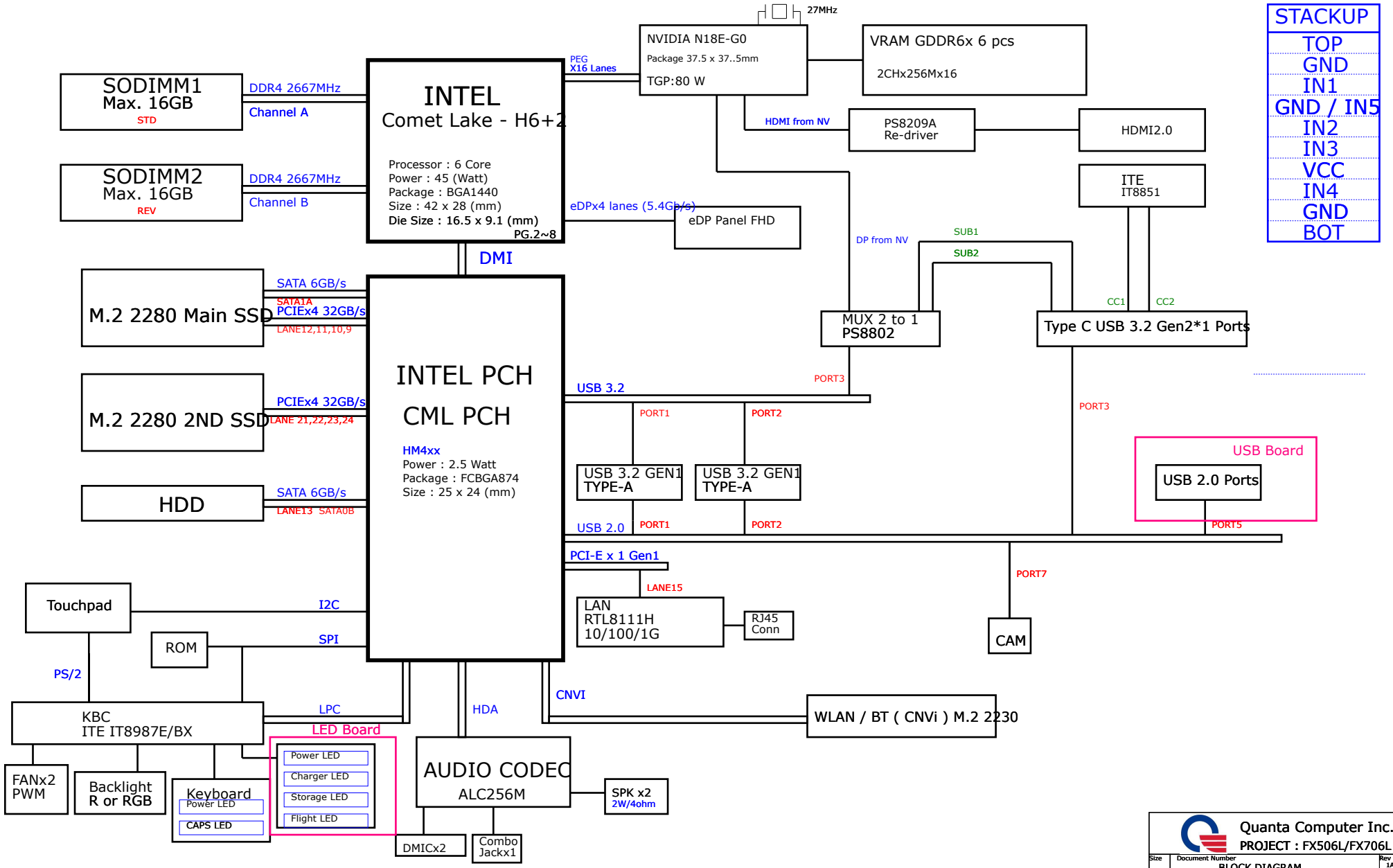
ASUS FX506LU N18E-G0 Block Diagram

01



STACKUP
TOP
GND
IN1
GND / IN5
IN2
IN3
VCC
IN4
GND
BOT

Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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Model
FX506LU

REV
ER

CHANGE LIST

Item	Stage	Page	Owner	Change explanation
01	ER	29	EE	ER-000:Del RUN_ON for 1.2V_MUX enable....1113
02	ER	29	EE	ER-001:Change G9090 to G986I to solve PD issue.and +1.2V_HDMI ripple issue....1113
03	ER	29	EE	ER-002:Add N-MOSFET to +1.2V_HDMI for ripple issue....1113
04	ER	39	EE	ER-004:Change +1.2V to +1.2V_HDMI power rail name....1113
05	ER	29	EE	ER-005:Del +3V power rail and SR9 and SR7 to shortpad....1113.
06	ER	29	EE	ER-006:Change +3V_PD to LDO for ripple issue....1113.
07	ER	39	EE	ER-007:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113
08	ER	29	EE	ER-008:No mount SR82 for surge issue....1113.
09	ER	29	EE	ER-009:DEL PD to MUX SMBUS....1113.
10	ER	29	EE	ER-010:Change no mount:SQ1,SR66,SR67, NO USED....1113.
11	ER	39	EE	ER-011:Change no mount:HQ3, NO USED....1113.
12	ER	29	EE	ER-012:Change SR61,SR62,SR63 TO NO-MOUNT for shortpad....1113.
13	ER	11	EE	ER-013:Change R206 TO NO-MOUNT for shortpad....1113.
14	ER	16	EE	ER-014:Change R858 and C1094,R856 TO NO-MOUNT....1113.
15	ER	7	EE	ER-015:Change C269 1000P to 10U_4 for power ripple....1113.
16	ER	18	EE	ER-016:Add 0.1U near MR5....1113.
17	ER	19	EE	ER-017:Add 0.1U near MR10....1113.
18	ER	32	EE	ER-018:Change C1116 *47U to 10U_4 for ripple....1113.
19	ER	22	EE	ER-019:Change GPIO27_IFPC_HPD to GPIO27_IFPC_HPD# for Low active....1113.
20	ER	22	EE	ER-020:Change GPIO18_IFPE_HPD to GPIO18_IFPE_HPD# for Low active....1113.
21	ER	28	EE	ER-021:Del RP1/RP2/RP3/RP4 and EMI by pass for EMI request....1113.
22	ER	07	EE	ER-022:Change C289,C73,C72 from 47uF to 22uF for PASs VRTT...1119
23	ER	29	EE	ER-023:Change SU10 part number for E ver and 08FW to fix PD2.0 fail issue....1120.
24	ER	36	EE	ER-024:Change KR122 00hm to no-mount for no support....1120
25	ER	28	EE	ER-025:Change AR47,AR48 to BLM15AG221SN1D and C1072 C1073 to 10P For EMI issue and signal pass....1122.
26	ER	31	EE	ER-026: Change 2.1ohm to 5.1ohm for fix TDR issue....1122.
27	ER	12	EE	ER-027: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.
28	ER	23	EE	ER-028: Change VRI13 to 10Kfor fixed GPU timing issue....1122.
29	ER	34	EE	ER-029: Change C355,C356 to no-mount for fix TP timing issue....1122.
30	ER	35	EE	ER-030:Add AR47 moat resistor between AGND&DGND and connect to AU1 pin20 for active speaker noise issue in S5...1122.
31	ER	37	EE	ER-031:Del KQ15/KQ13 for no support Red backlight....1125.
32	ER	23	EE	ER-032:Fix voltage ripple over spec ....1128.
33	ER	35	EE	ER-031:AR14 and AR5 change from 22 ohm to 10 ohm increasing the FSOV margin.
34	ER	30	EE	ER-032:Remove CON6 for USB board FFC CONN
35	ER	30	EE	ER-E33:Reserve CON6 for USB board FFC CONN.....1206
36	ER	31	EE	ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brigtness
37	ER			
38	ER			
39	ER	54	Power	ER-001:PR63I from 1000hm to 105ohm for +1.0V_GPU_output voltage.
40	ER	48	Power	ER-002:Add PC169 & PC170 47pF for ASUS SDW.
41	ER	41	Power	ER-003:Change PR1093 from 16.9k to 18.7k to set IA iccmax 128A for CML H base.
42	ER	41	Power	ER-004:Change PC1061 from 68pF to 330pF to correct L_DCR matching.
43	ER	41	Power	ER-005:Change PR1078 from 422 to 442 ohm to to set OCP 180A for H62.
44	ER	41	Power	ER-006:Change PC1068 from NI to 47nF to correct L_CDR matching.
45	ER	41	Power	ER-008:Change PR1078 from 365 to 287 ohm to set OCP 116A for H42.
46	ER	41	Power	ER-009:Change PR1057 to 71.2k to correct IMONA for H42.
47	ER	41	Power	ER-010:Change PR1070 from 5.11k to 3.3k to correct DCLL for H42.
48	ER	43	Power	ER-011:PC1333,PC1334,PC1335,PC1336,PC1337,PC1338 add 22uF to reduce ripple by VTT test
49	ER	41	Power	ER-012:Change PC1044 from 10nF to 15nF to correct L_DCR matching for SA.
50	ER	41	Power	ER-013:Change PC1050 from 220pF to 680pF to reduce undershoot for SA.
51	ER	47	Power	ER-014:Delete PD12 & PD13 for SHDN# issue.
52	ER	47	Power	ER-015:PC157 1000P change to 2200P for meet HDD rise time SPEC.
53	ER	47	Power	ER-016:PC164 1000P change to 680P for meet TP rise time SPEC.
54	ER	45	Power	ER-017:PR1397 change to 6.49K+-1% for output voltage up.
55	ER	54	Power	ER-018:PR642 change from 24.9K to 25.5K by EE request
56	ER	56	Power	ER-019: PC295 & PC299 NC, 180W/G0 just 9pcs
57	ER	41-56	Power	ER-020:00hm change to short pad.
58	ER	41-56	Power	ER-021:Remove output short pad.
59	ER	47	Power	ER-022:Reserve MAIND signal
60	ER	45	Power	ER-023: +1.05V_VCCSTG enable signal change to RUN_ON by EE request
61	ER	47~49	Power	ER-024:add test point PTP1~6 for ASUS request
62	ER	47	Power	ER-025:Reserve PC1405 for EMI request
63	ER	50	Power	ER-026:PU24 change to MP2886AGU-0144-Z by nVidia requests VRM from RC mode to liner mode
64	ER	49	Power	ER-027:Set Pmon(max) on 360W
65	ER	53	Power	ER-028:Fix FBVDDQ voltage due to support G0 only
66	ER	44	Power	ER-029:VCCIO enable signal change to CI0_GATE# by EE request
67	ER	45	Power	ER-030: +1.05V_VCCSTG enable signal change to CI0_VCCSTG_EN; mount PU1332 for debug

DOC NO.	PROJECT MODEL :	BKLG/BKLH	APPROVED BY:		DATE:	2018/01/17
	PART NUMBER:		DRAWING BY:		REVISON:	1A

02

Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	POWER UP SEQUENCE	2A

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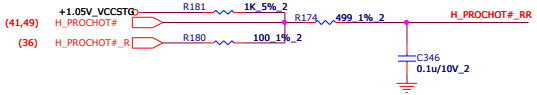
Comet Lake Processor (CLK,MISC,JTAG)

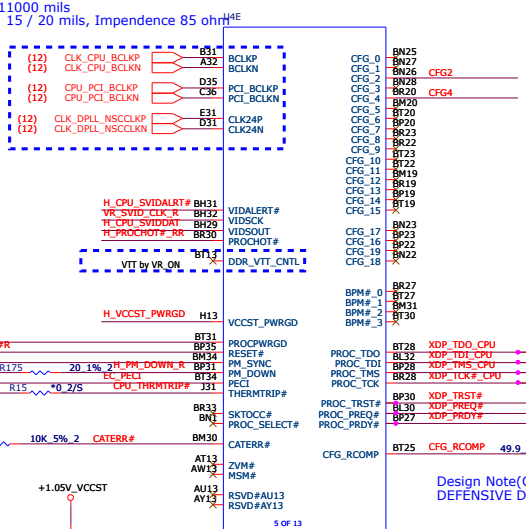
03

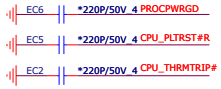
Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

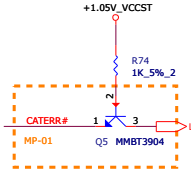
PROCHOT# (50ohm)
Trace Length <11 inches

Cb need placment near VR





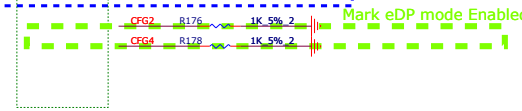




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;

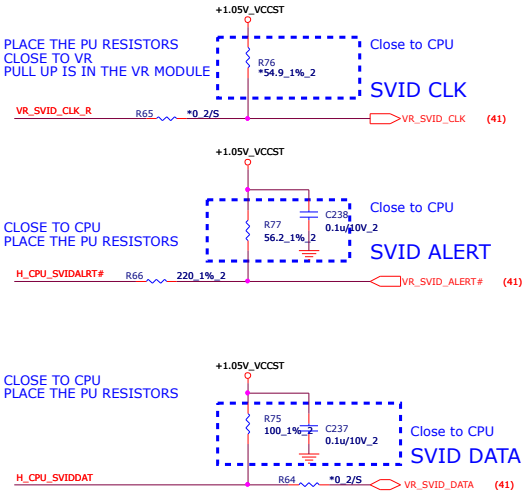


Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

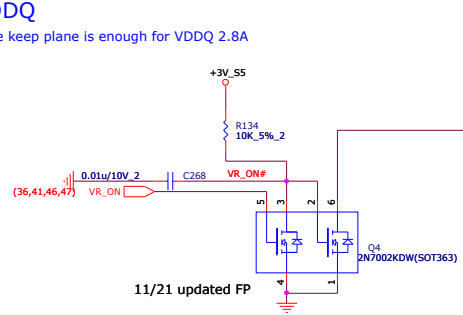
CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

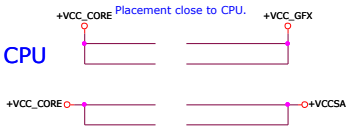


CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



Under CPU



11/21 updated FP

Quanta Computer Inc.
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Size	Document Number	Rev
	CML 1/7 (JTAG/MISC)	2A

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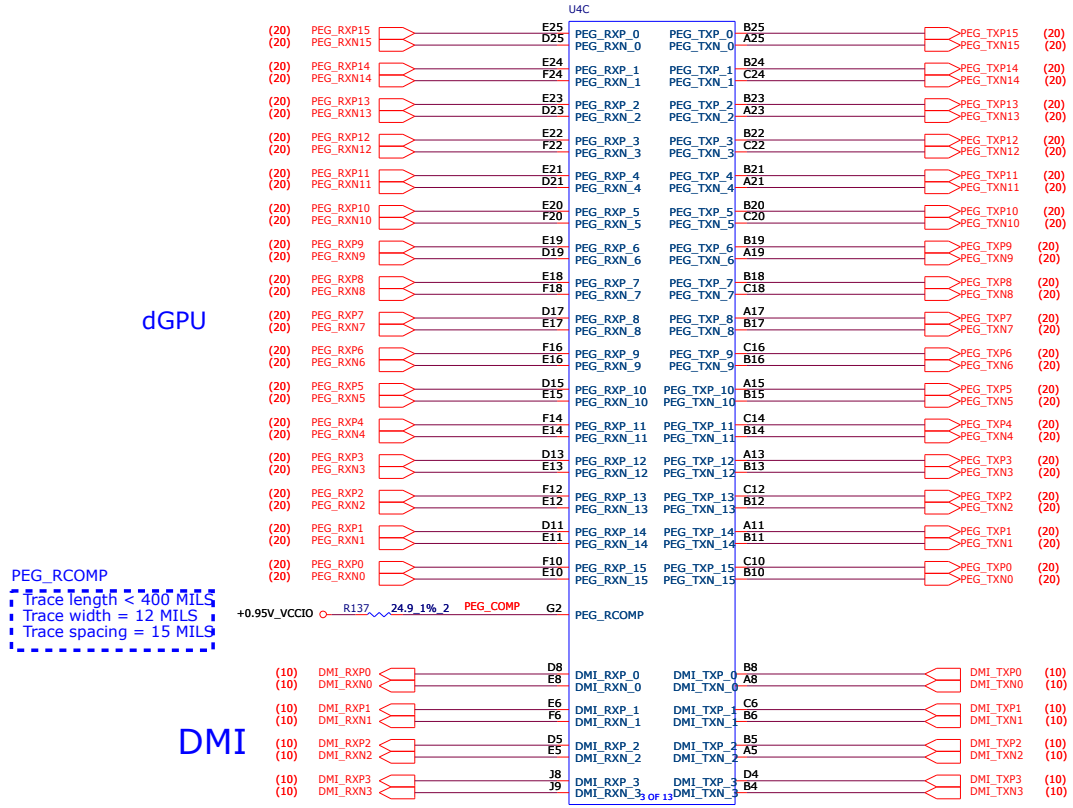
Comet Lake Processor (DMI,PEG,FDI)



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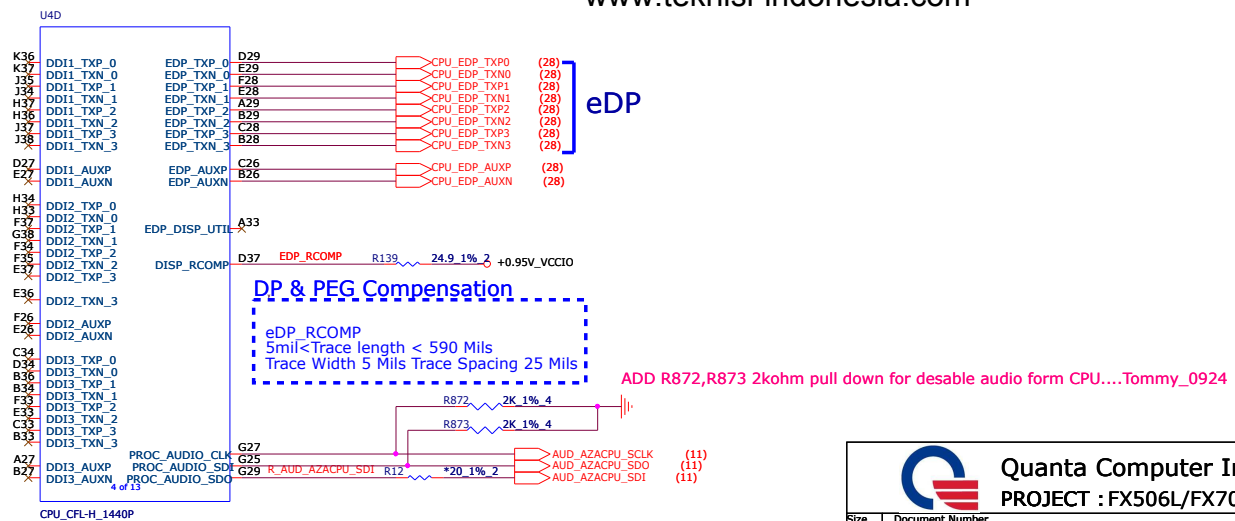

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	CML 2/7 (DMI/EDP/PEG)	2A
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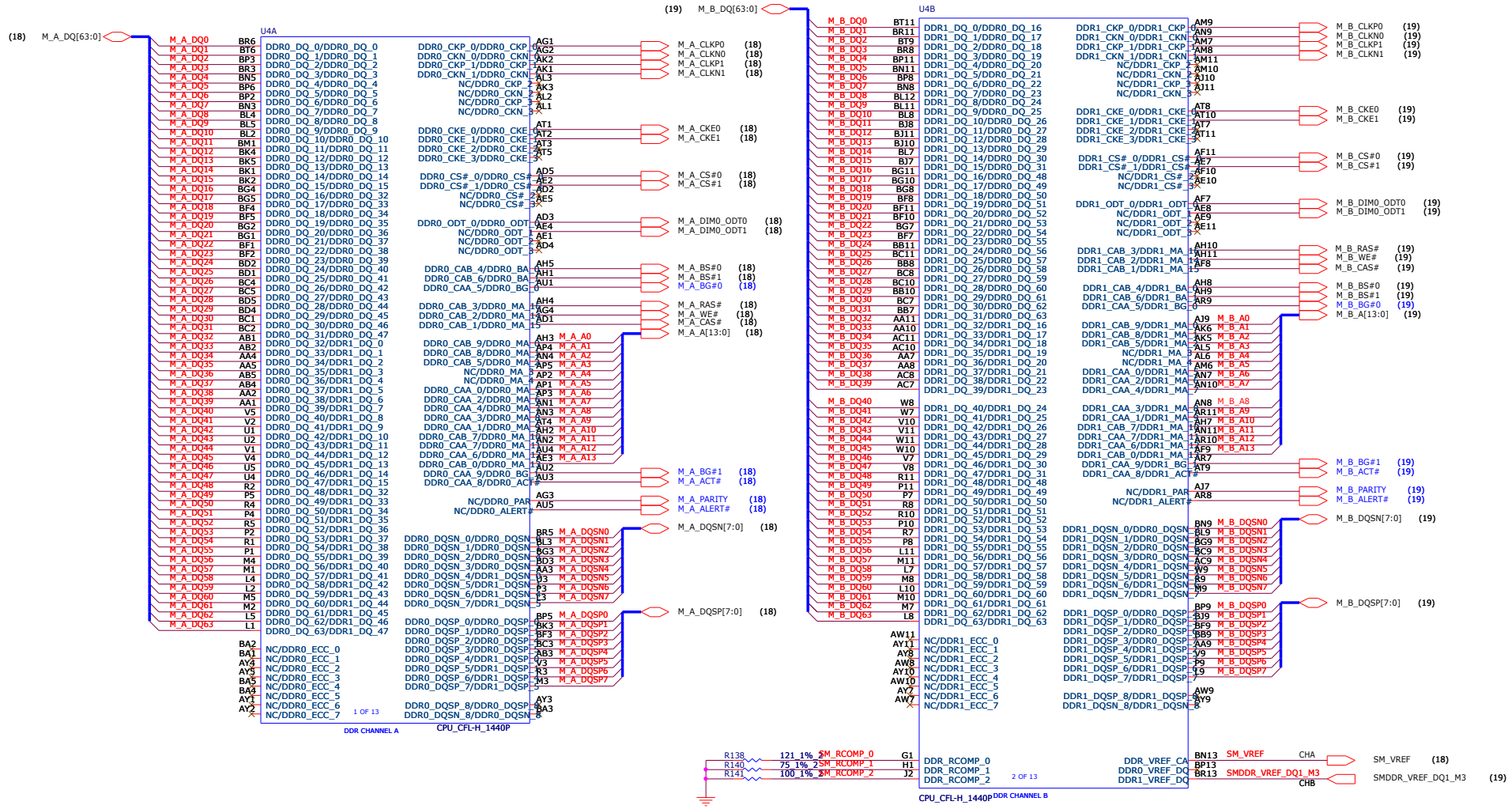
Comet Lake Processor (DDR4)

Interleaved

05



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PROJECT : FX506L/FX706L	
Size	Document Number: CML 3/7 (DDR4 I/F) — Rev: 2A
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CML Processor (POWER)

Follow CML H page 126 to 45W(GT2): +VCCGT=32A

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	CML 4/7 (POWER/GT)	2A

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Follow CML H EDS page 135 to 45W(GT2): VCCSA=11.1A

ER-022:Change C289,C73,C72 From 47uF to 22uF for PASS VRTT...1119

Follow CML H EDS page 135 45W: VDDQ=3.3A

Follow CML H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V

U4L

11.1 A

2.8 A

6.4A

0.26 A

0.12 A

0.145 A

12 OF 13

CPU_CFL-H_1440P

For C10 power function

Close to U1.BH13/BJ13/G11

Close to U1.H29,G30

Under CPU

Close CPU

Short-Pad

ER-015:Change C269 1000P to 10U_4 for power ripple....1113.

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	CML 5/7 (POWER&GND)	2A

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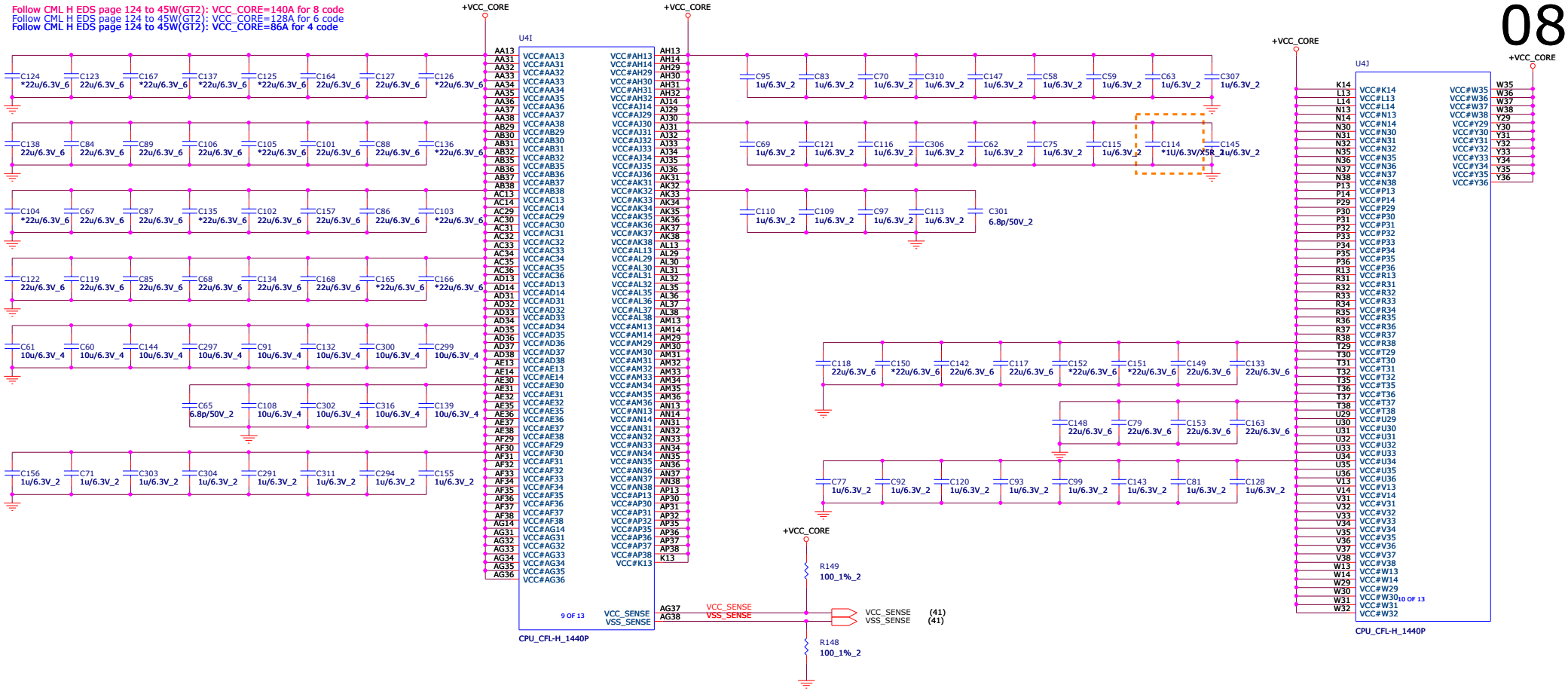
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=140A for 8 code
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=128A for 6 code
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=86A for 4 code



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

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	CML 6/7 (POWER&GND)	2A

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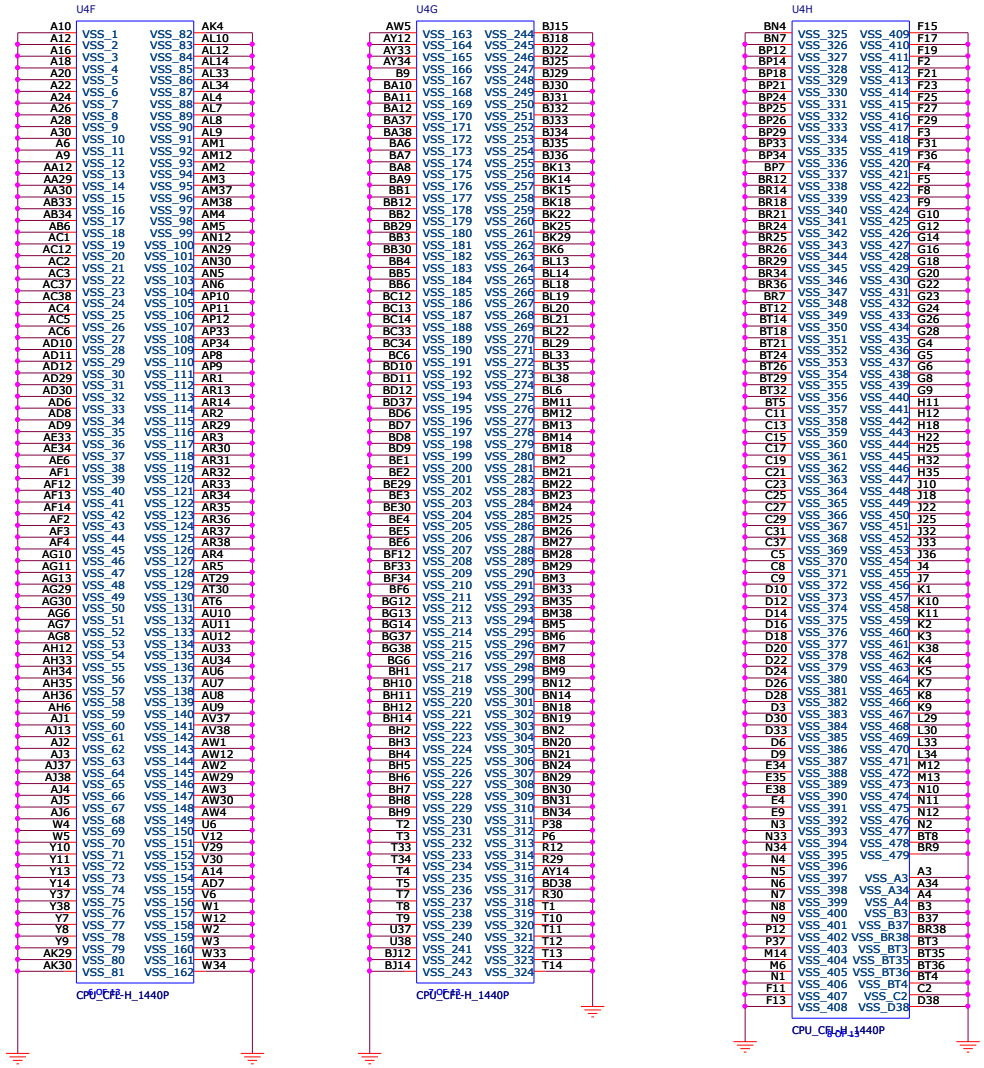
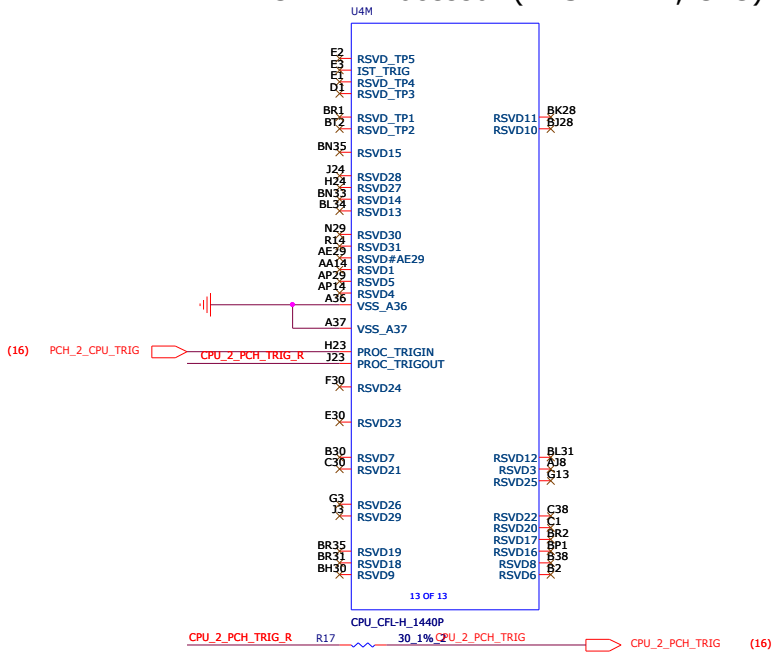
CML-H Processor (GND)



CML-H Processor (RESERVED, CFG)



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	CML 7/7 (GND)	2A
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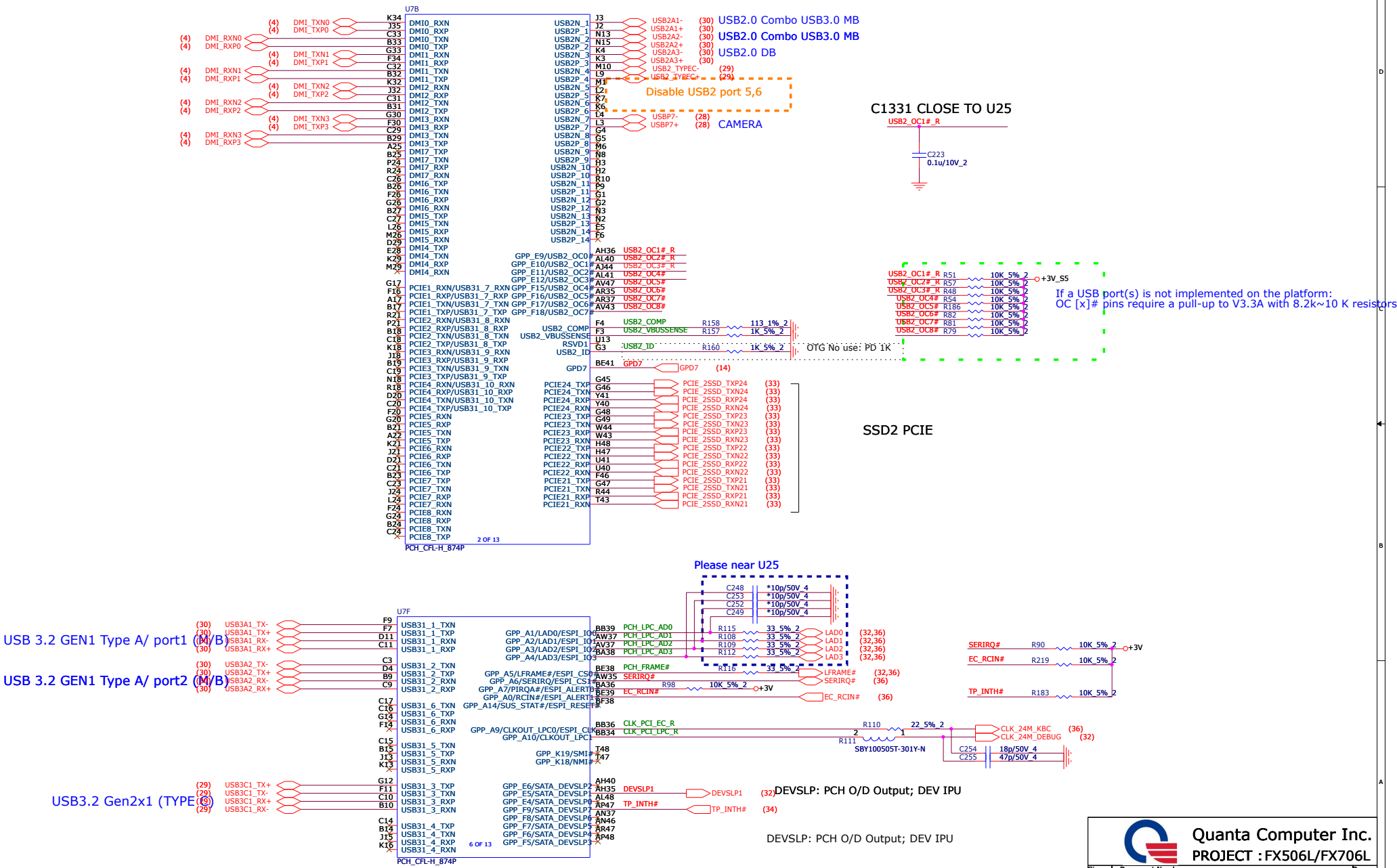

Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	2A
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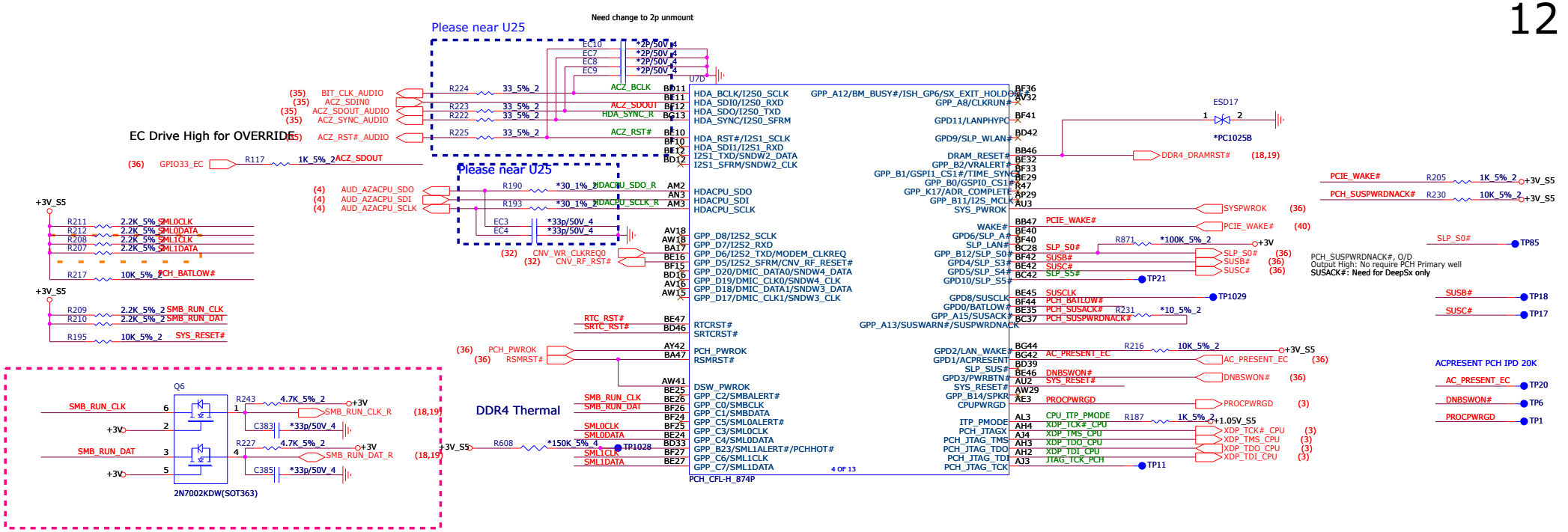

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PROJECT : FX506L/FX706L		
Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	2A
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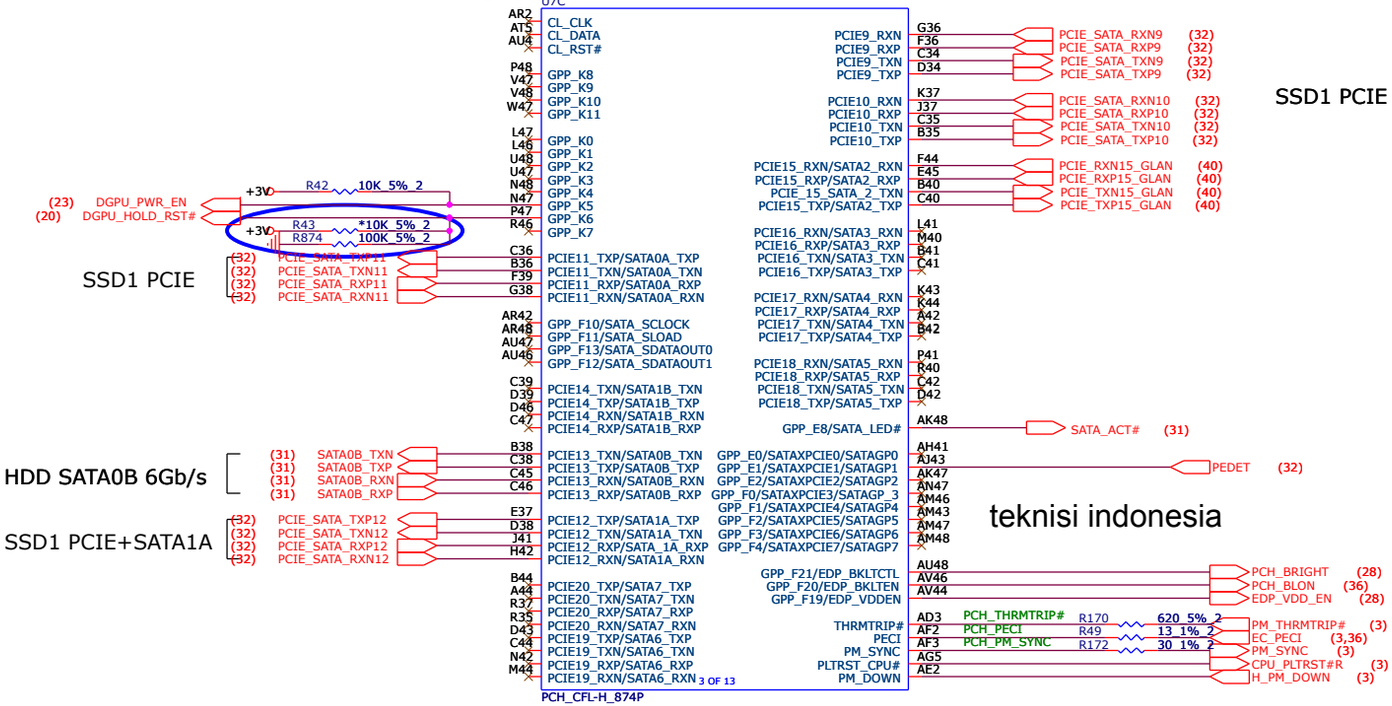
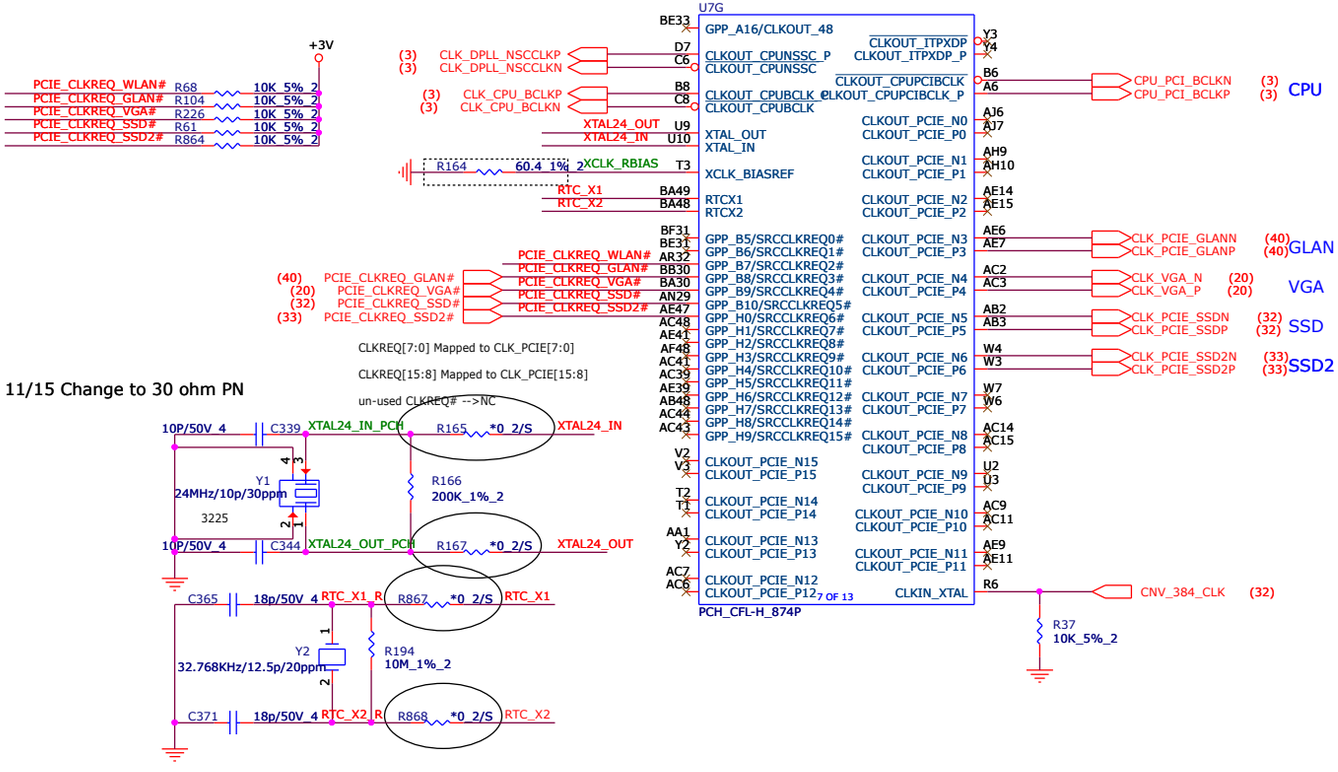
ER-027: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.



SATAPCIE[7:0]: BIOS Enable PCH IPU 20K

PCH SATAPCIE
H-->PCIE
L-->SATA
BISO PSCPSP_Px_STRP = 1

Add 2ND SSD for PCIE....Tommy_0816



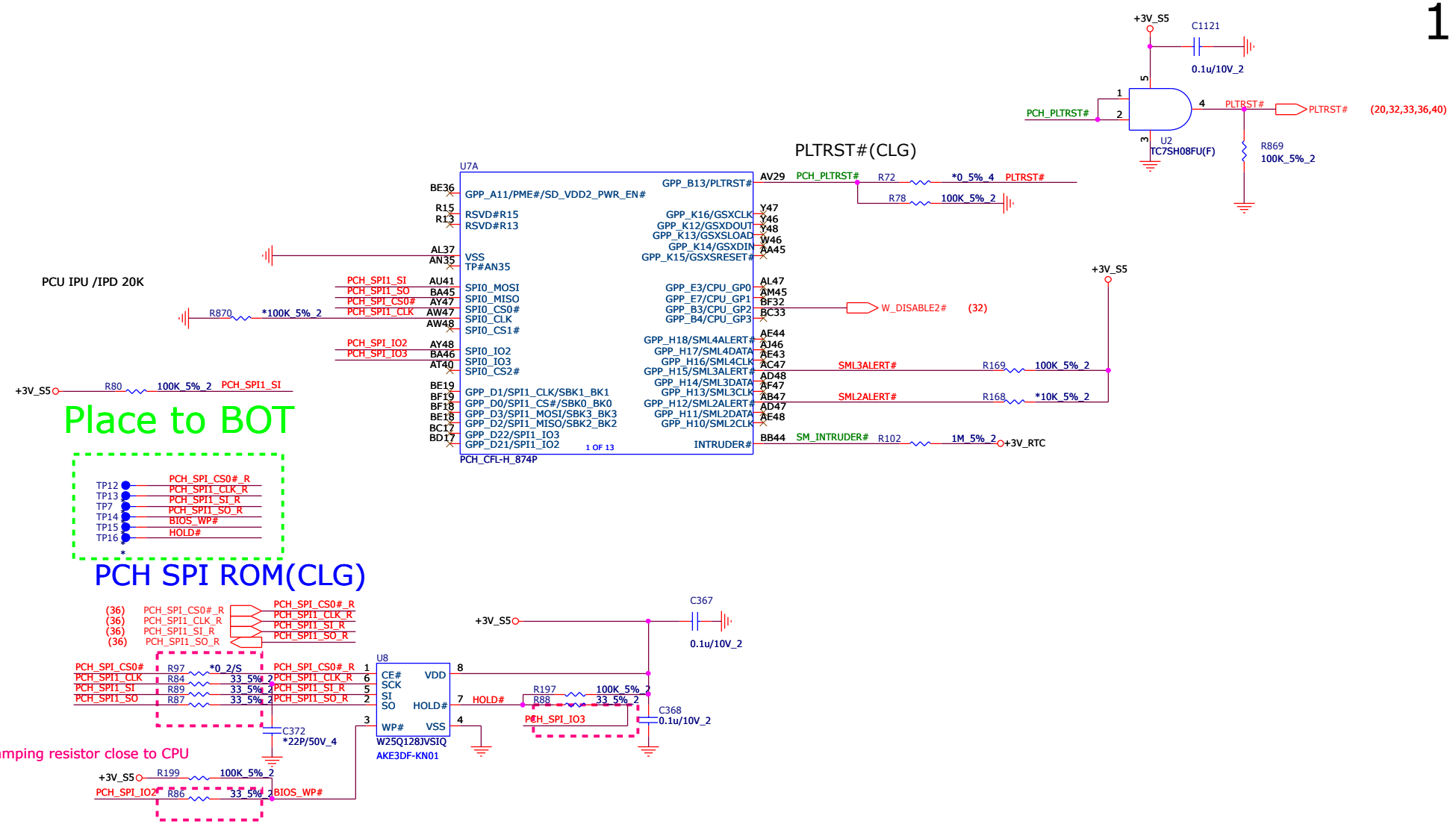
PLTRST#(CLG)

PCU IPU /IPD 20K

Place to BOT

PCH SPI ROM(CLG)

Put damping resistor close to CPU



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PROJECT : FX506L/FX706L

Size	Document Number	Rev
	PCH 4/7 (GPIO/MISC)	2A
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	BOARD_ID0	
i7 DDR 3200MHz	0	
i5 DDR 2933MHz	1	

Cannon Lake PCH-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) Default 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default 1 = Enable No Reboot Mode	
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) Default 1 = Enable Intel ME Cryp to TLS PU to support AMT TLS	
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	0 = *SPI (iPD 20K) Default 1 = LPC	
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) Default 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSMRST#	0 = *Master Attached Flash Sharing (MAFS) enabled (iPD 20K)Default 1 = Slave Attached Flash Sharing (SAFS) enabled.	
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) (Default) 1 =Port B is detected	
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) (Default) 1 =Port C is detected	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	PCH_PWROK	0 = *Port D is not detected (iPD 20K) (Default) 1 =Port D is detected	
GPP_F23	Display Port F Detected	PCH_PWROK	0 = *Port F is not detected (iPD 20K) (Default) 1 =Port F is detected	CFL - H CPU Not Support DDI Port F
GPP_J4 CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	RSMRST#	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. 0 = *38.4MHz XTAL frequency selected. (iPD 20K) (Default) 1 = 24MHz XTAL frequency selected.	
GPP_J6 CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. (Default) 1 = Integrated CNVi disable.	
GPP_J9	1.8V VCCPSPI	RSMRST#	0 = *VCCSPI is connected to 3.3V rail. (iPD 20K) (Default) 1 = VCCSPI is connected to 1.8V rail	
GPD7	Reserved	DSW_PWROK	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	External pull-up is required. Recommend 100K.

Warning: This strap must be configured to '0' (SAFS is disabled)
if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

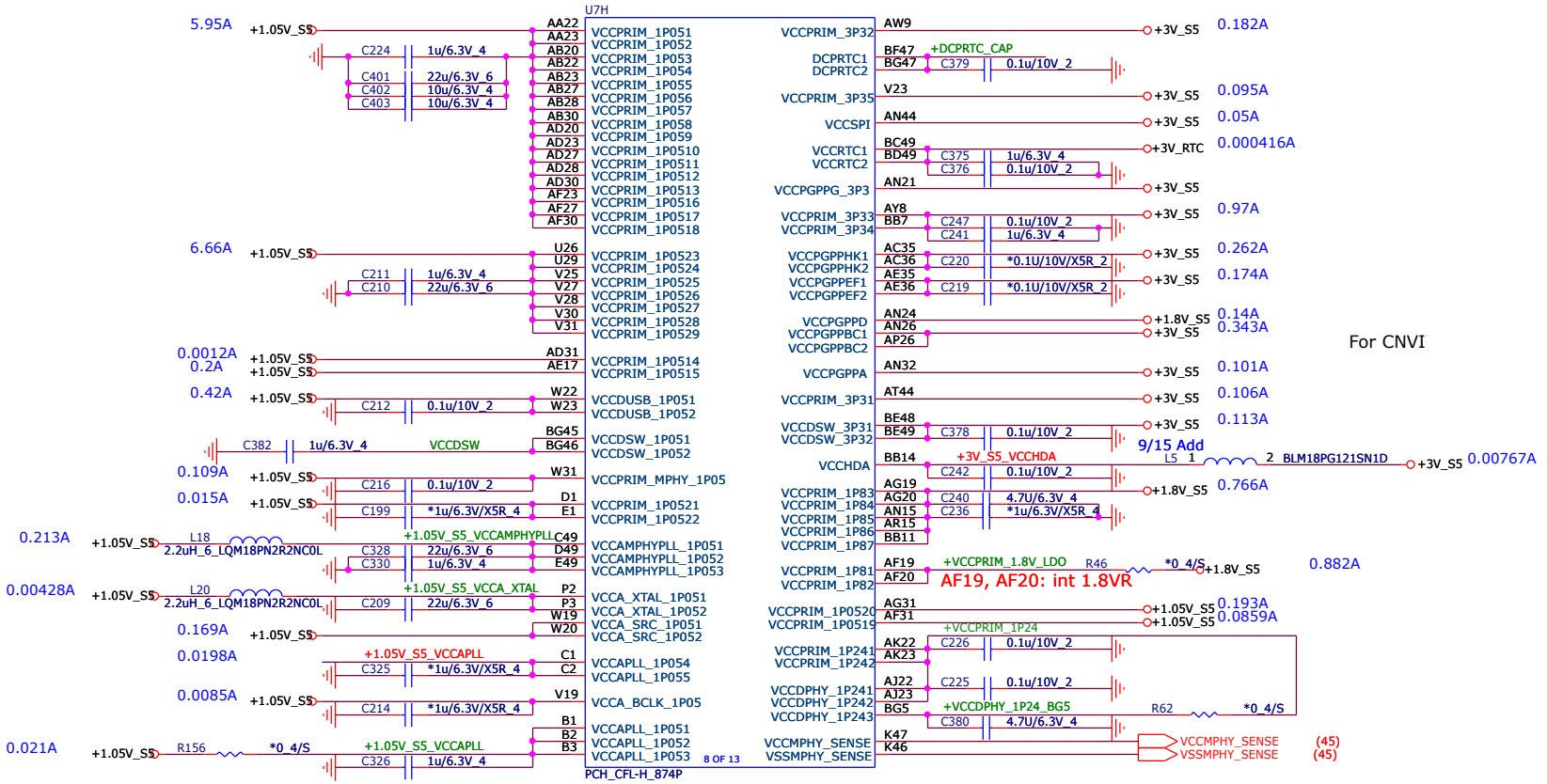
Change R58,R59,R843,R842 mount to no mount for no support DDI....Tommy_0903

PCH Strap: GPP_J4 = XTAL SELECT-1
HIGH -> 24 MHZ / LOW -> 38.4 MHZ

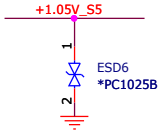
PCH Strap: GPP_J6 = M.2 CNVI STRAP
HIGH -> DISABLE / LOW -> ENABLE

Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1'
for the proper functionality of the SPI (Flash) I/Os

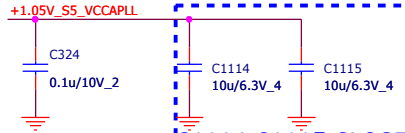
need to add +1.05V power rail



ESD6 CLOSE TO U7



C324 CLOSE TO U7.B2



1.24V for CNVi logic = VCCDPHY_1P24 & +VCCPRIM_1P24
This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.
Refer to the Platform Design Guide for implementation details.

C1114,C1115 CLOSE TO U7.C1 pin

Quanta Computer Inc.		
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	PCH 6/7 (POWER)	2A
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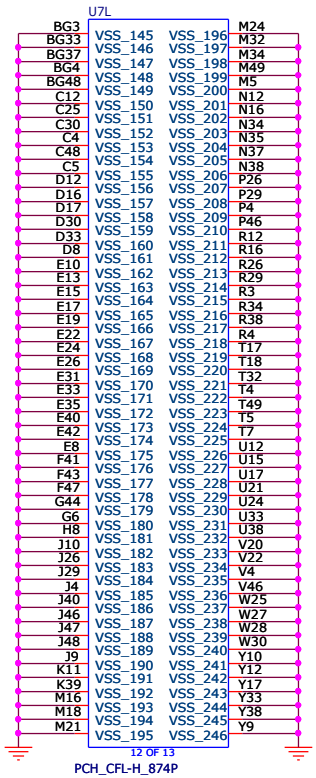
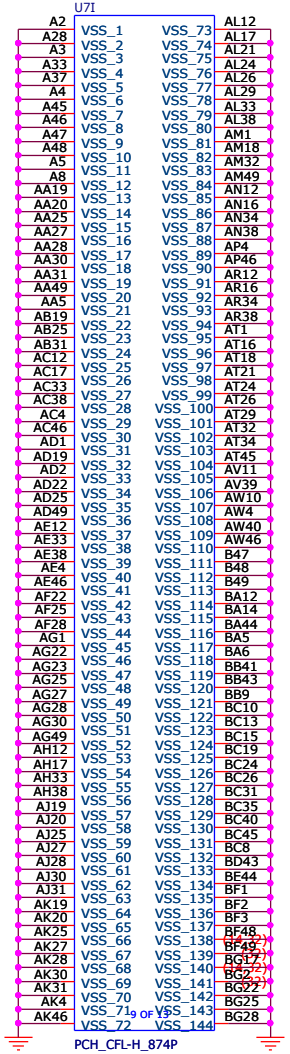
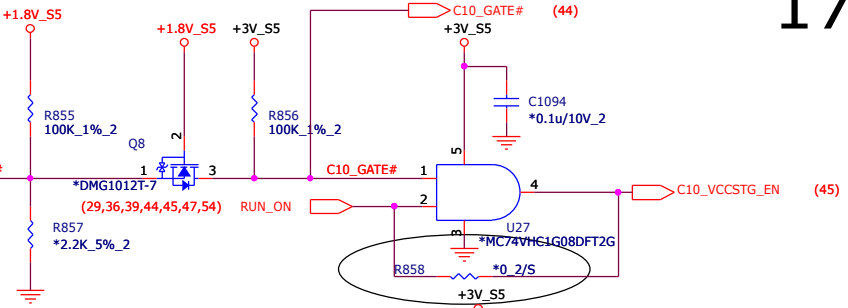
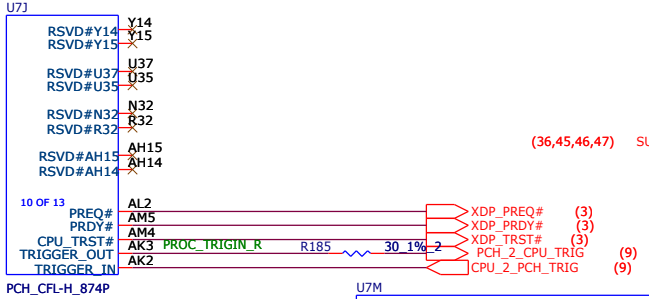
ER-014:Change R858 and C1094,R856 TO NO-MOUNT....1113.

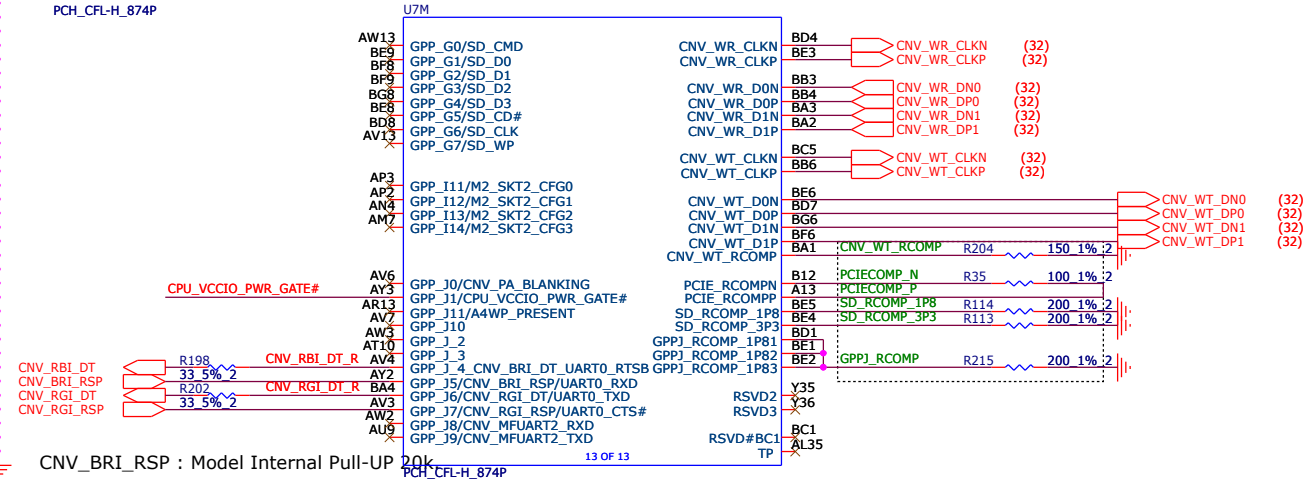






ER-E35:Reserve U28 for C10 GATE# support.



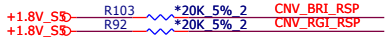


CNV_BRI_RSP : Model Internal Pull-UP 20k.

CNV_RGI_RSP : Model Internal Pull-UP 20k.

Close to U25

Follow #571483 CFL-H CRB0.9 Reserve Pull-H Resistor.



Quanta Computer Inc.

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	PCH 7/7 (GND/CNV)	2A

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SMT GASKET-BOT

S10 EMI-3x2x2 GB0MB002010
S11 EMI-3x2x2 GB0MB002010
S12 EMI-3x2x2 GB0MB002010
S13 EMI-3x2x2 GB0MB002010
S14 EMI-3x2x2 GB0MB002010
S15 EMI-3x2x2 GB0MB002010

CPU上上上上上上

FAN

H5 *HG-C315D158P2
H7 *HG-C315D158P2
H4 *H-TC256I177BC217D177P2
H16 *hg-c256d177p2

CPU / GPU brket

H8 *H-TC217I146BC185D146P2
H9 *H-TC217I146BC185D146P2
H10 *HG-TC217IBC185D146
H11 *HG-TC217IBC185D146
H12 *HG-TC217IBC185D146P2
H13 *HG-TC217IBC185D146P2
H14 *HG-TC217IBC185D146P2
H15 *HG-TC217IBC185D146

Audio上上上上

H21 *HG-C315D158P2

2nd SSD NUT

H42 H-TC217BC136D136PT
H43 h-tic197bc118d118p2
H44 h-tic197bc118d118p2

PCH NUT

USB2.0 CONN GP

S9 *SPAD-RE323X238

H1 *H-TC256BC236D177P2
H2 *h-c71d71n
H3 *h-o71x83d71x83n
H6 *spad-re236x157np
H17 *h-c154d154n
H19 *SPAD-BKXD-2
H45 *SPAD-BKXD-2
H41 *H-BKX-2

Type C

H22 *H-BKX-1
H24 *h-c236d118p2
H25 *H-O118X169D118X169N

H27 *he-220x67
H28 *he-220x67
H29 *he-220x67
H30 *he-220x67
H31 *he-220x67
H32 *he-220x67
H33 *he-220x67
H34 *he-220x67
H35 *he-220x67

2D barcode

H39 *2D-BARCODE-8X8-S
H40 *2D-BARCODE-8X8-S

USB2 PAD

SP2 *spad-c177np
SP3 *SPAD-RE315X91
SP4 *SPAD-C236

DDR4 clip PAD

S1 *RHC-CP-15T06 FBDZ1005010
S2 *RHC-CP-15T06 FBDZ1005010
S3 *RHC-CP-15T06 FBDZ1005010
S4 *RHC-CP-15T06 FBDZ1005010
S8 *RHC-CP-15T06 FBDZ1005010

placement on TOP SIDE VIN Plane

VIN
EMIC8 EMIC10 EMIC12 EMIC14 EMIC16 100p/50V_2
EMIC73 EMIC74 EMIC75 EMIC76 EMIC77 0.1U/50V/X5R_4
For EMI Request ! 20190923

VIN
EMIC7 EMIC9 EMIC11 EMIC13 EMIC15 EMIC17 EMIC18 EMIC19 EMIC20 EMIC21 EMIC22 EMIC23 EMIC24 EMIC25 EMIC26 EMIC27 EMIC28 EMIC29 EMIC30 EMIC31 EMIC32 100p/50V_2

placement on TOP SIDE VA+ Plane

VA
EMIC33 EMIC35 EMIC37 EMIC39 EMIC41 EMIC43 EMIC45 EMIC47 EMIC49 EMIC51 EMIC53 EMIC55 EMIC57 100p/50V_2

VA+
EMIC34 EMIC36 EMIC38 EMIC40 EMIC42 EMIC44 EMIC46 100p/50V_2

+3V_S5 +5V_S5
EMIC78 EMIC79 EMIC80 EMIC81 0.1U/10V/X5R_2
For EMI Request ! 20190923

+0.95V_VCCIO +VCC_CORE +VCC_GFX +3V_S5
EMIC82 EMIC83 EMIC84 EMIC85 0.1U/10V/X5R_2
For EMI Request ! 20190923

Quanta Computer Inc.
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Size	Document Number	Rev
	HOLE	1A

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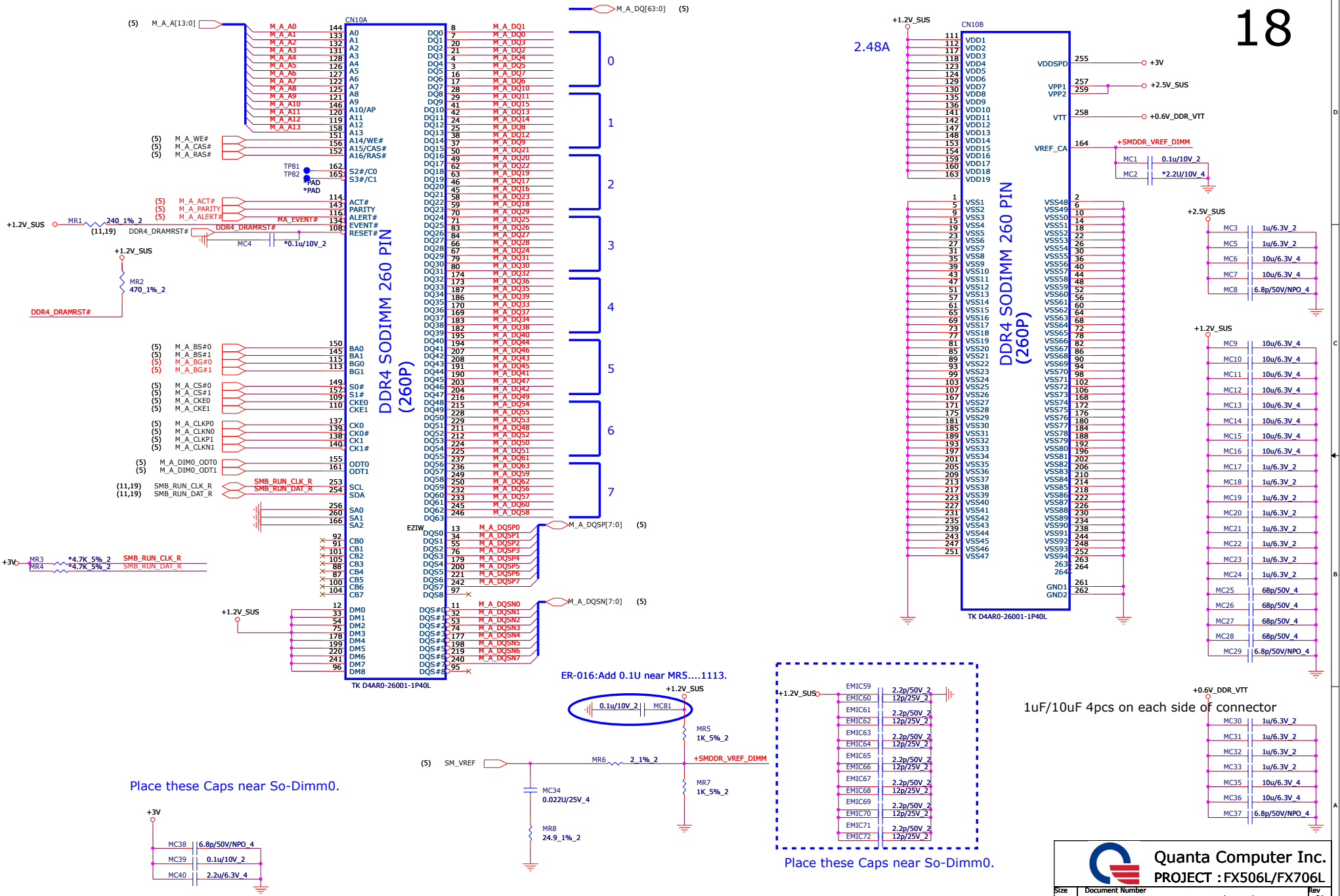
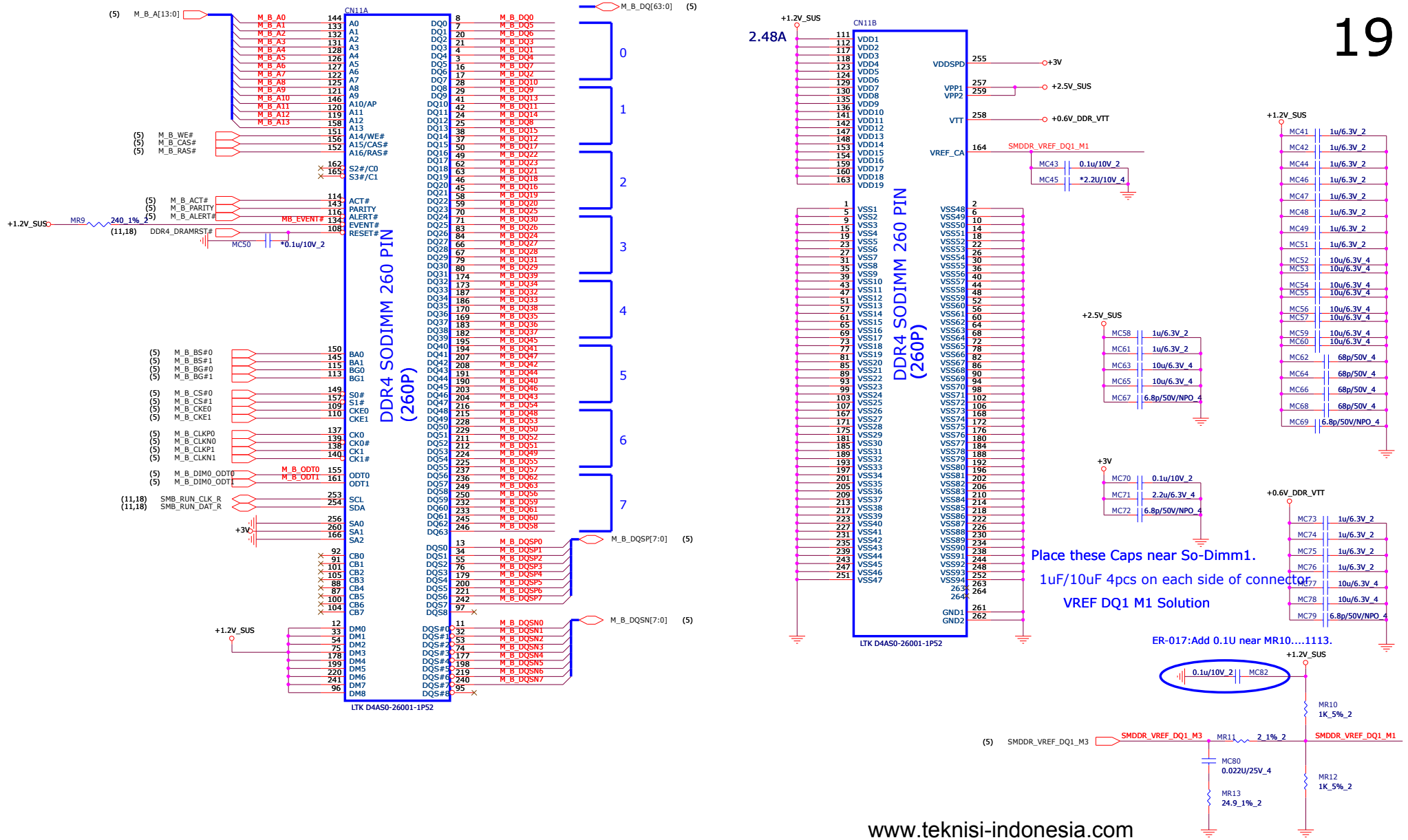
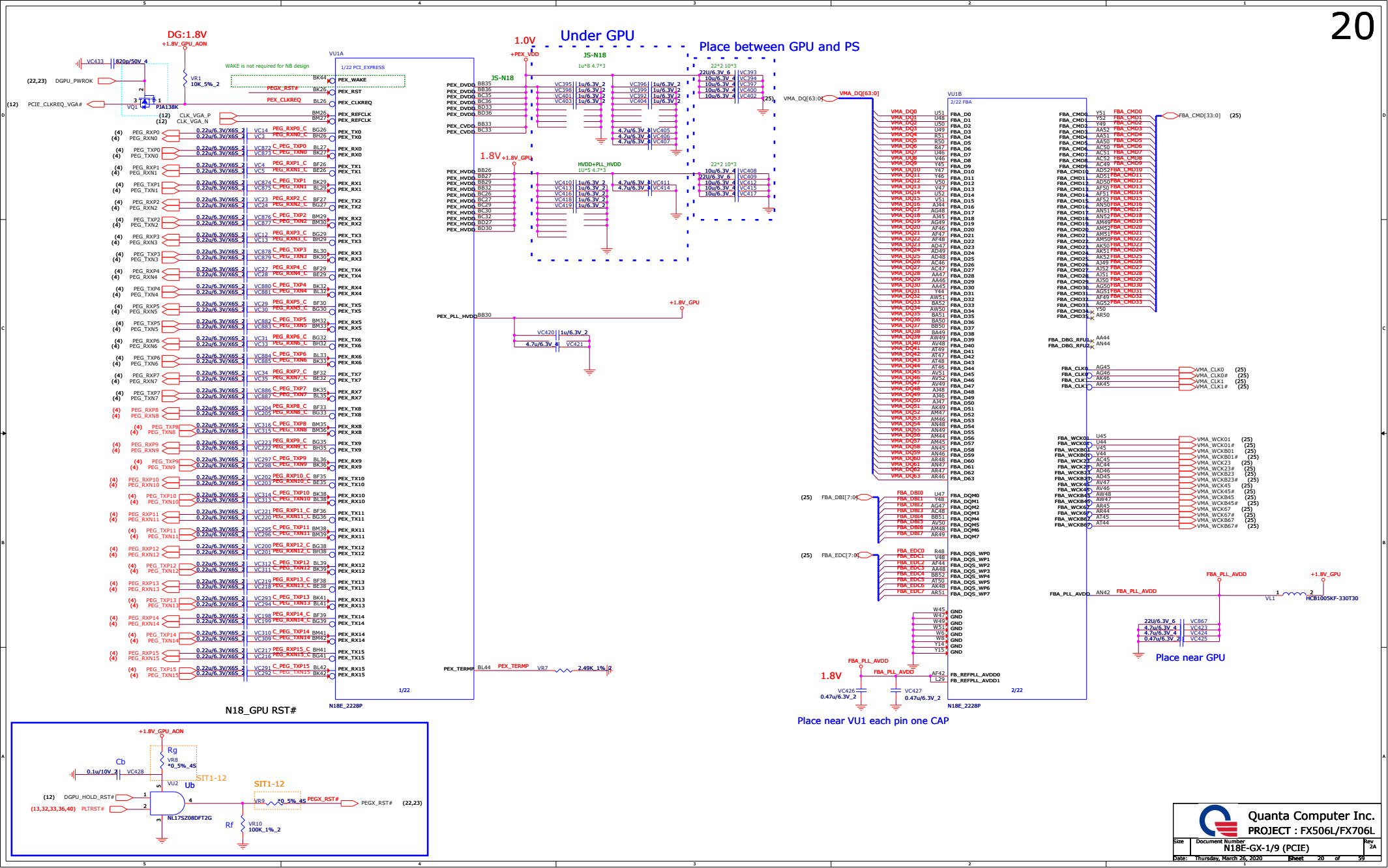


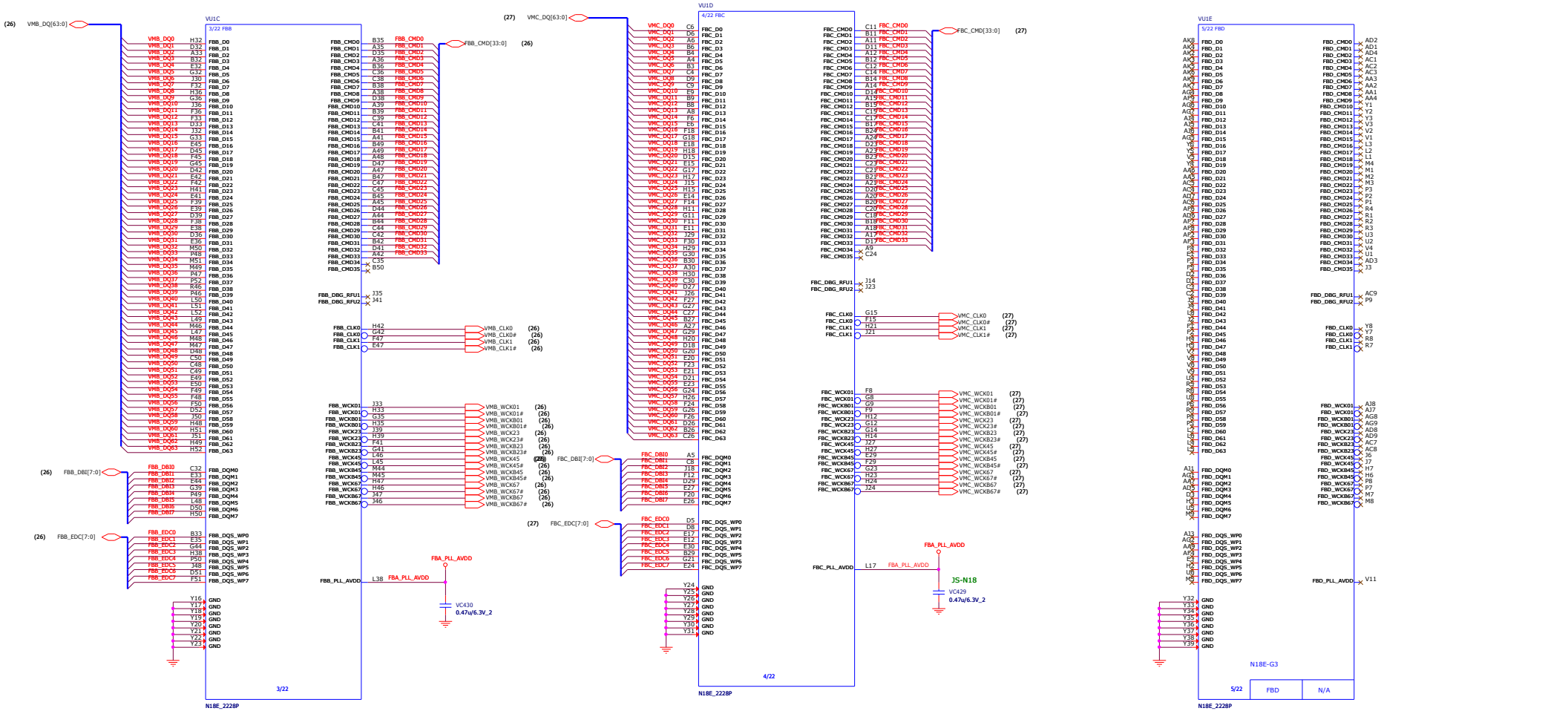
Quanta Computer Inc.	
PROJECT : FX506L/FX706L	
Size	Document Number: DDR4 DIMM0-RVS(4.0H)-CHA
Rev	2A
Date: Thursday, March 26, 2020	Sheet 18 of 59



19

Quanta Computer Inc.	
PROJECT : FX506L/FX706L	
Size	Document Number: DDR4 DIMM1-STD(4.0H)-CHB
Rev	2A
Date: Thursday, March 26, 2020	Sheet 19 of 59


DG:1.8V
Under GPU
Place between GPU and PS
Place near GPU
Place near VU1 each pin one CAP
N18_GPU RST#
N18E_2228P
Quanta Computer Inc.
PROJECT : FX506L/FX706L
N18E-GX-1/9 (PCIE)
Thursday, March 26, 2020



Quanta Computer Inc.			
PROJECT : FX506L/FX706L			
Size	Document Number		Rev
	N18E-GX-2/9 (Memory)		2A
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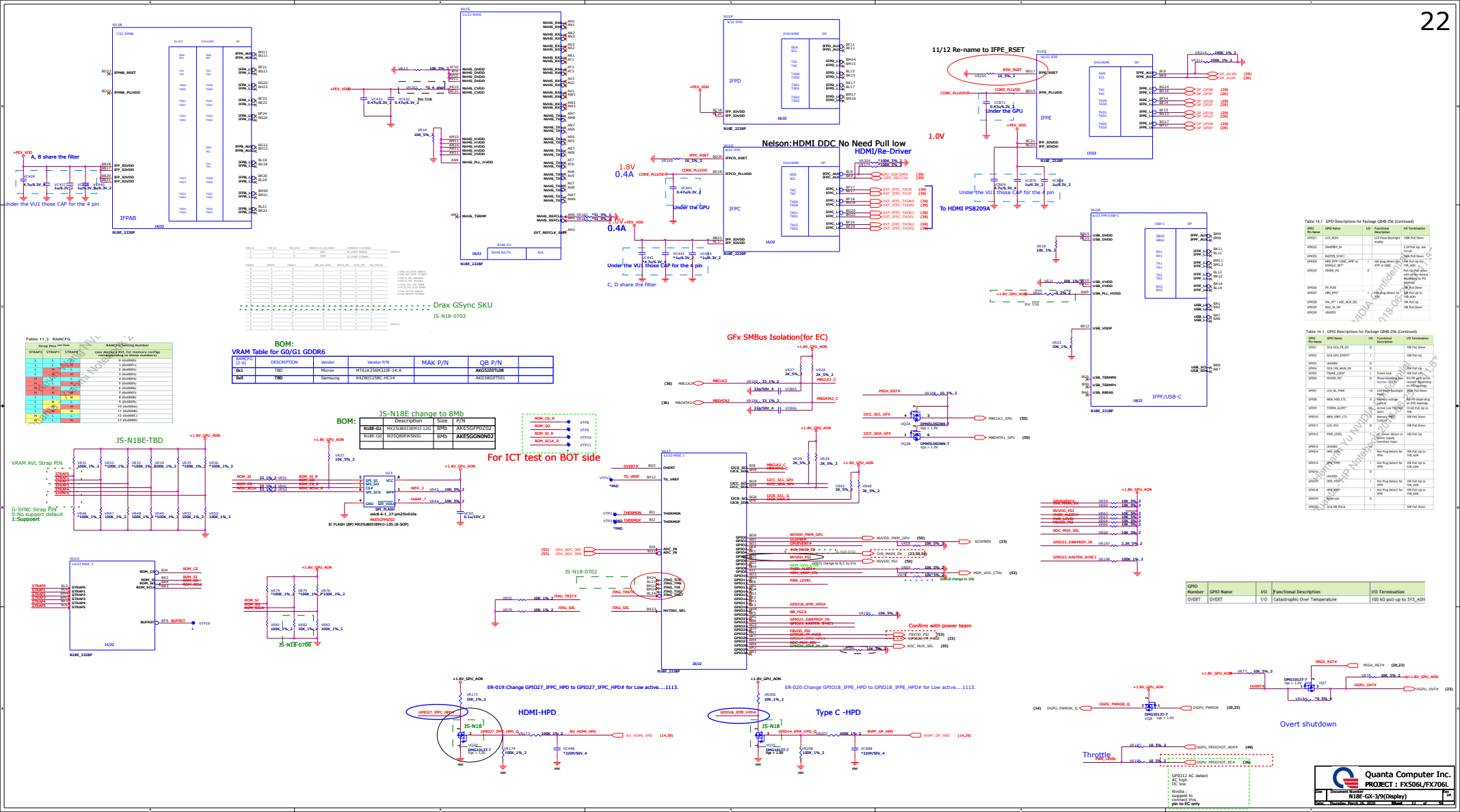


Table 11.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number (see description BYL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
H	M	L	12 (0x000C)
H	L	M	13 (0x000D)

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	MAK P/N	QB P/N
0x1	TBD	Micron	MT61K256M32JE-14:A		AKD5IZ0TL08
0x0	TBD	Samsung	K4ZB0325BC-HC14		AKD5BG0T501

	Description	Size	P/N
N18E-G1	MX25U8035EM1I-12G	8Mb	AKE5GFP0Z0Z
N18E-G0	W25Q80EWSNIG	8Mb	AKE5GGN0N0Z

Table 14.1 GPIO Descriptions for Package GB4B-256 (Continued)

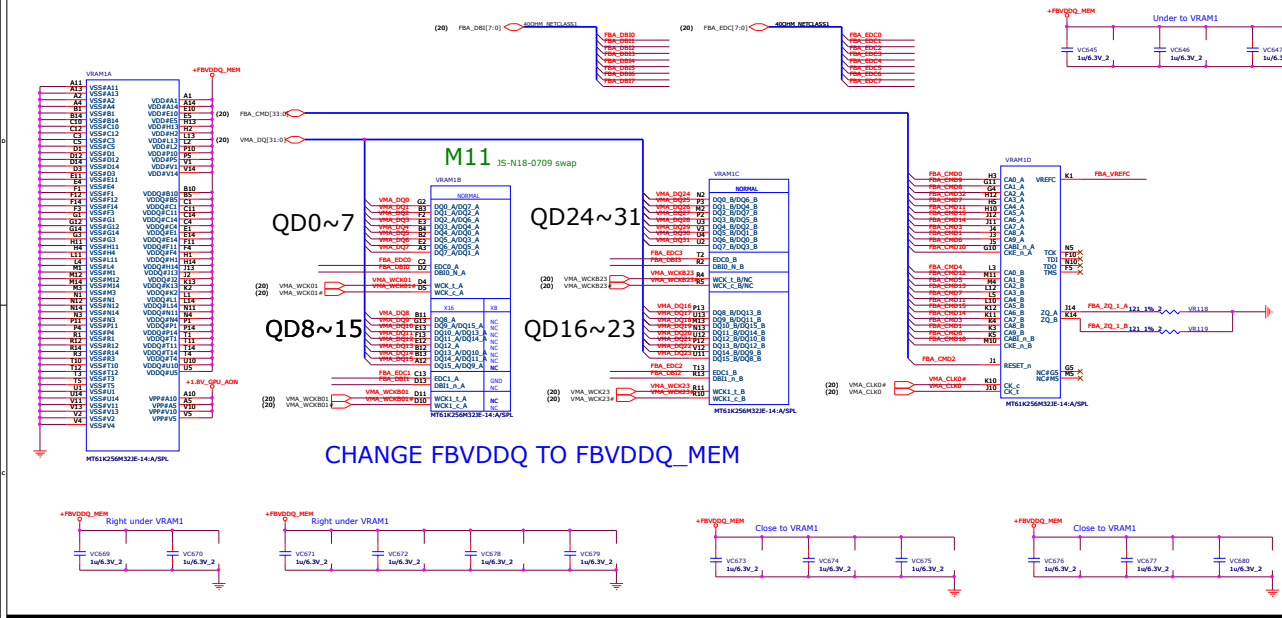
GPIO Pin Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO21	LCD_BLEN		LCD Panel Backlight enable	100K Pull Down
GPIO22	SYNCPREF_EN			2.2K Pull Up, see circuit
GPIO23	RASTER_SYNC1			100K Pull Down
GPIO24	HPD_EFFI*/GSC_SPR0* or DONGLE_RST*	I	Hot plug detect for EFFI or GSC	10K Pull Up to 1V8, ADH
GPIO25	FBVDD_PSI	O		Pull Up/Pull down with config related depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot plug detect for IFPC	10K Pull Up to 1V8_ADH
GPIO28	PML_RT* / ADC_MUX_SEL			10K Pull Up
GPIO29	ECLK_IN_SW			10K Pull Down
GPIO30	UNUSED			

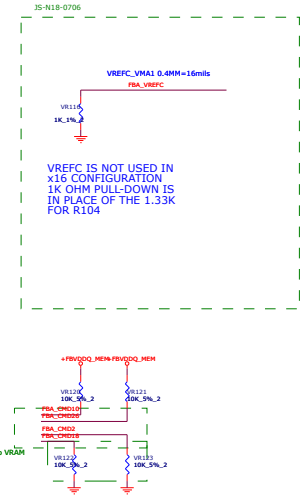
Table 14.1 GPIO Descriptions for Package GB4B-256 (Continued)

GPIO Pin Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO1	GC6/GC6_FB_EN	O		10K Pull Down
GPIO2	GC6/GPU_EVENT*	I		10K Pull Up
GPIO3	UNUSED			
GPIO4	GC6/ VID_MARK_EN	O		10K Pull Up
GPIO5	FRAME_LOCK*	O	Frame lock	10K Pull UPs
GPIO6	WIMOD_EN*	O	Power Switching Gate Driver ENABLE	PU/PD with series resistor depending on PD topology
GPIO7	LCD_BL_PWM	/O	LCD Panel Backlight PWM	10K Pull Down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	3V/VO depending on DVD topology
GPIO9	THERM_ALERT*	I	Active Low Thermal Alert	10 kΩ Pull Up to 1V8
GPIO10	MEM_VREF_CTL	O	External VREF control	10K Pull Down
GPIO11	LCD_VCC	O		10K Pull Up
GPIO12	PWR_LEVEL	I	DC_power detect or power supply overdrive input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_ADH
GPIO15	PML_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_ADH
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_ADH
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_ADH
GPIO19	Reserved	O		
GPIO20	GC6/MB_FGC6			10K Pull Down

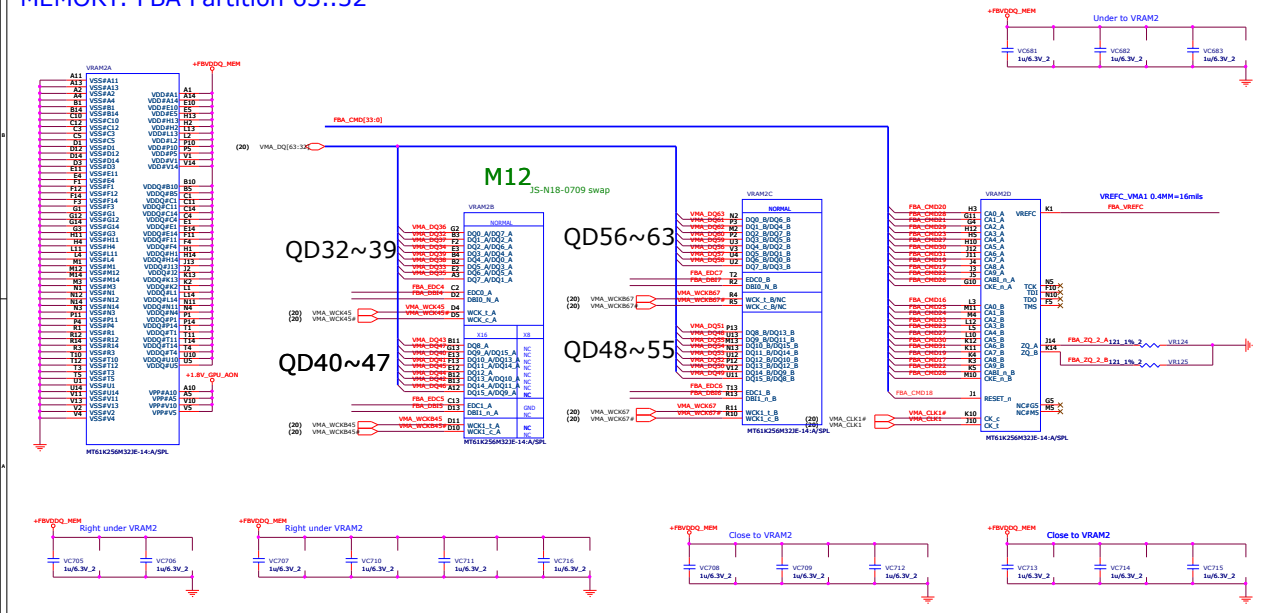
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

MEMORY: FBA Partition 31..0





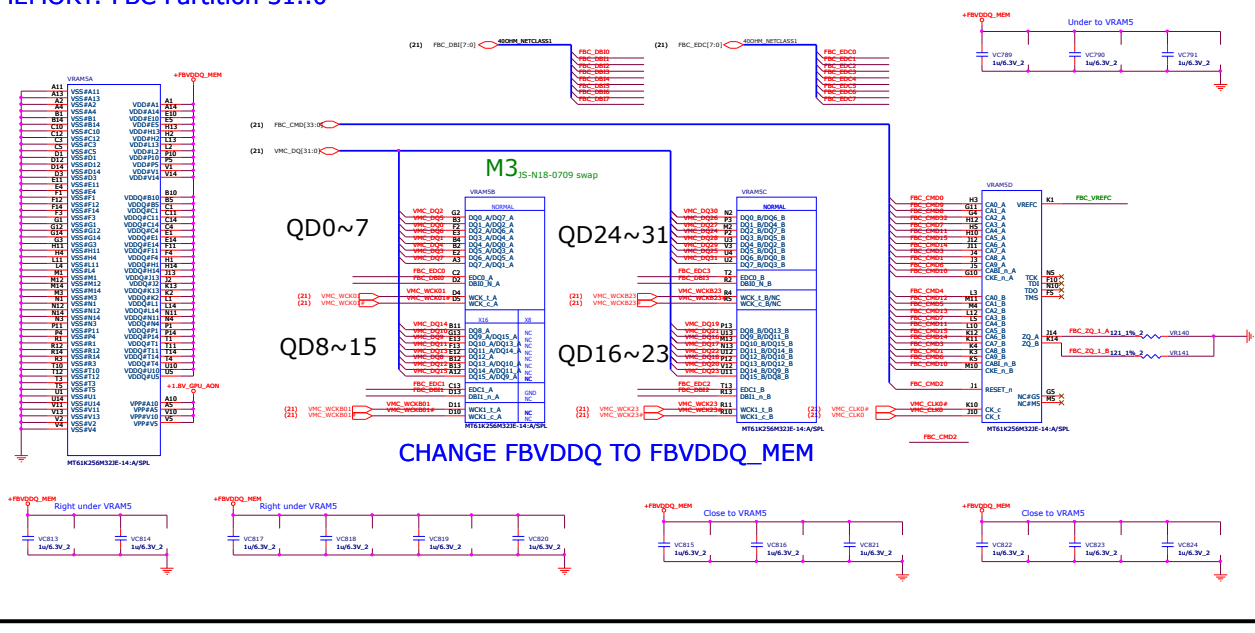
MEMORY: FBA Partition 63..32



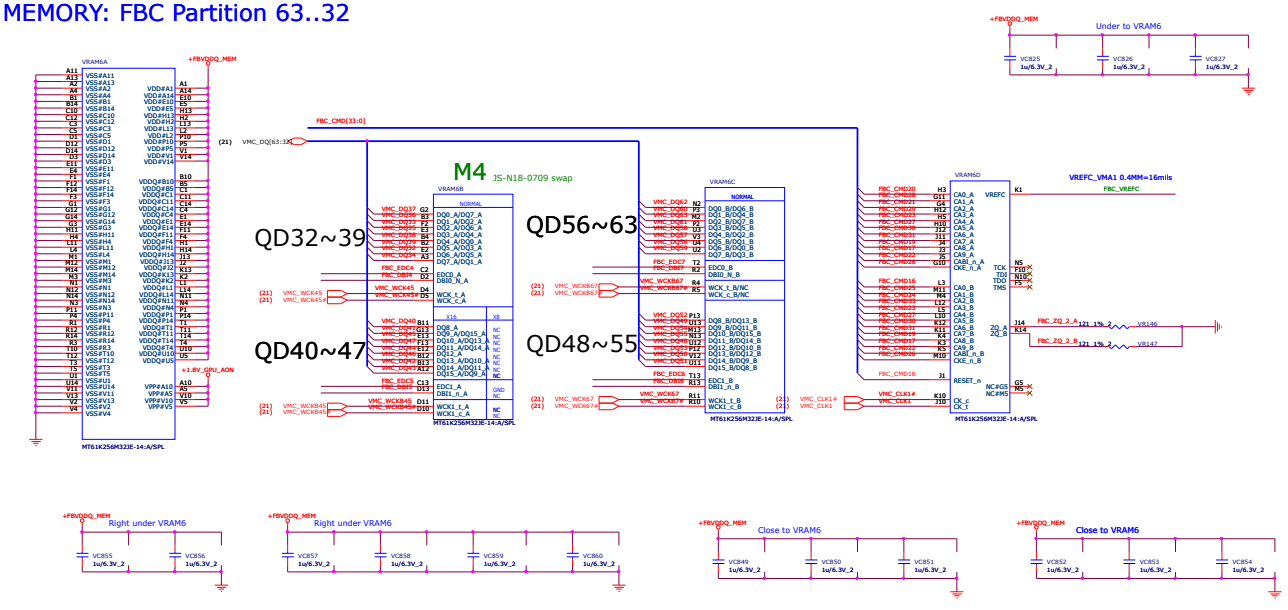
GDDR6 CMD Mapping	Lower 0..31 DRAM1 CHA-Byte 0,1	Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

teknisi indonesia

MEMORY: FBC Partition 31..0



MEMORY: FBC Partition 63..32



GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD5	CMD25
CA2_B	CMD13	CMD24
CA3_B	CMD7	CMD33
CA4_B	CMD11	CMD23
CA5_B	CMD15	CMD27
CA6_B	CMD14	CMD30
CA7_B	CMD3	CMD31
CA8_B	CMD1	CMD19
CA9_B	CMD6	CMD17
CABI_B	CMD10	CMD22
CKE_B		CMD26
RESET*	CMD2	CMD18

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eDP Conn.

ER-025:Change EMIL5.EMIL6 to BLM15AG221SN1D and C1072 C1073 to 10P For EMI issue and signal pass....1122.

Camera

ER-021:Del RP1/RP2/RP3/RP4 and EMI by pass for EMI request....1113.

MCM2012B900GBE

*HCM2012GD500AE

*PC1025B

51540-04001-V01

USB Camera Power

I rush =0.5A/0.5ms
IDD = 0.3A

Vout=1.2*(1+R1/R2)
3.49V

G917T11U

1.5A

Change to FFC type....Tommy

2.5A / 100mils

G9661MF11U

Vout=0.8*(1+Rg/Rh)=0.8(1+12K/3.6K)=3.46V
3.46V

Vout1 = (1+Rg/Rh)*0.8

PD Controller

DP MUX

Type C

CE_DP	CE_USB	FLIP	
L	H	L	SSRX/TX to TX1/RX1
L	H	H	SSRX/TX to TX2/RX2
H	L	L	ML0 to RX2, ML1 to TX2, ML2 to TX1, ML3 to RX1
H	L	H	ML3 to RX2, ML2 to TX2, ML1 to TX1, ML0 to RX1
H	H	L	SSRX to RX1, SSTX to TX1, ML0 to RX2, ML1 to TX2
H	H	H	SSRX to RX2, SSTX to TX2, ML0 to RX1, ML1 to TX1

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	Type C & PD& DP MUX	2A
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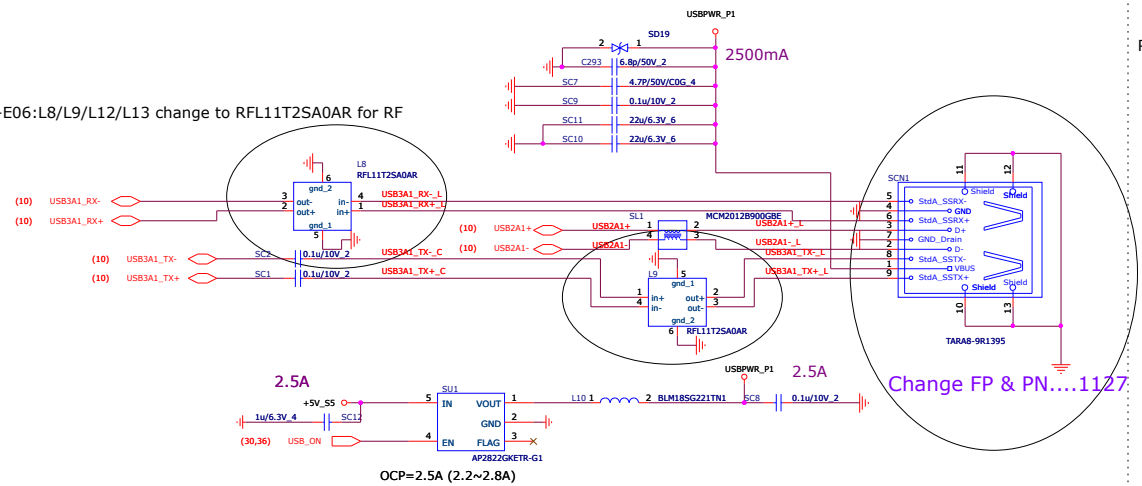
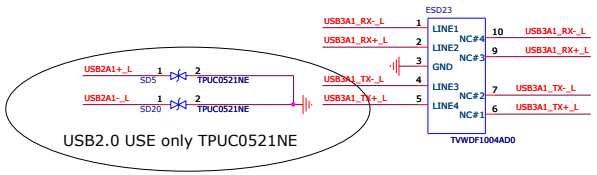
USB 3.2 GEN1 Type A/ PORT1

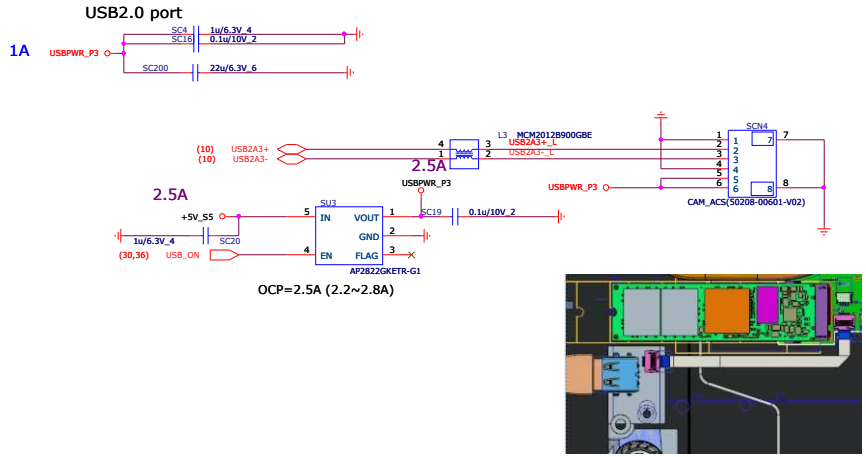
PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF





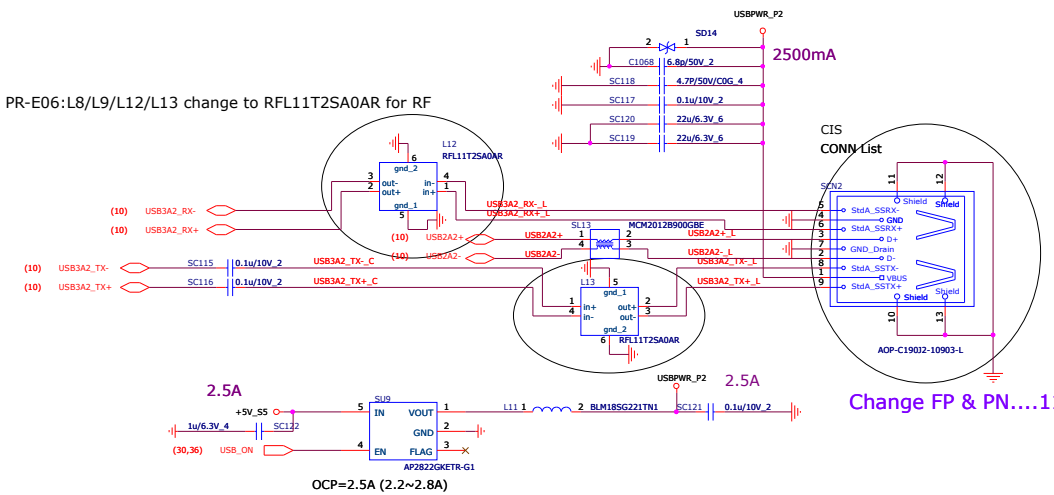
USB 2.0 PORT1

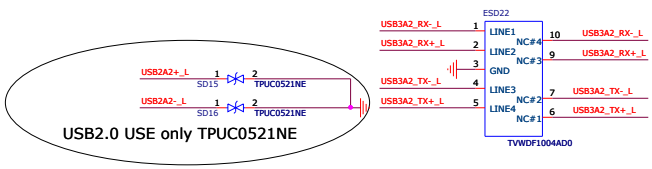
PR-E02:Remove CON6 for USB board FFC CONN.....0217



USB 3.2 GEN1 Type A/PORT2

PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF





Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	USB3.0/USB2.0	2A
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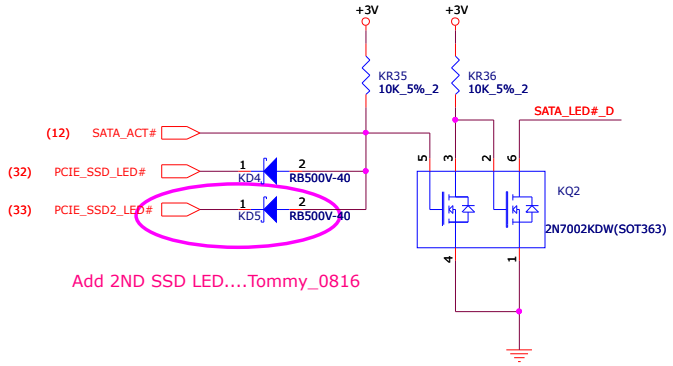
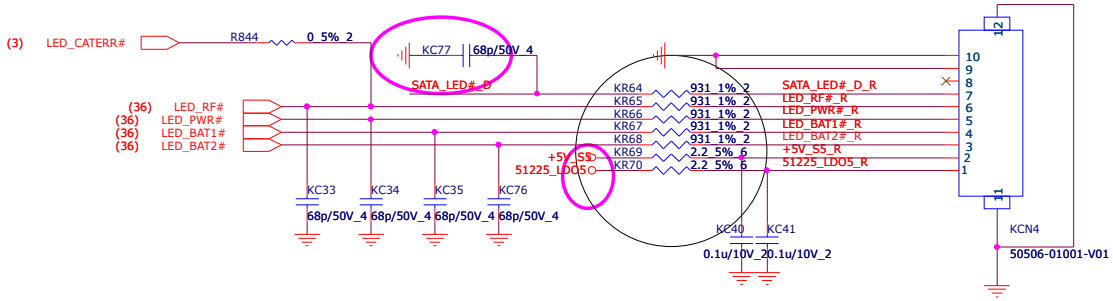
LED

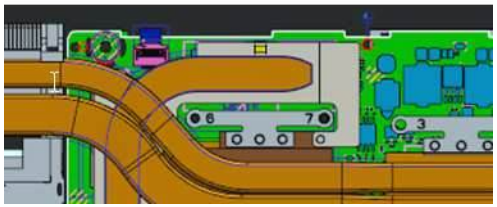


Add 2ND SSD LED....Tommy_0816

Add 68P for EMI....Tommy_0912

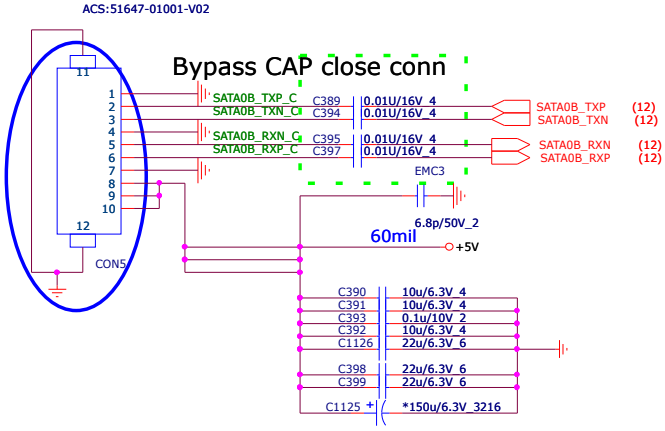


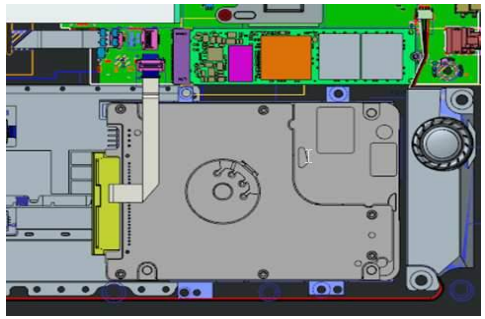
ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brigtness



SATA HDD FFC

ER-032:Change HDD FFC pin define for ME cable routing....1126

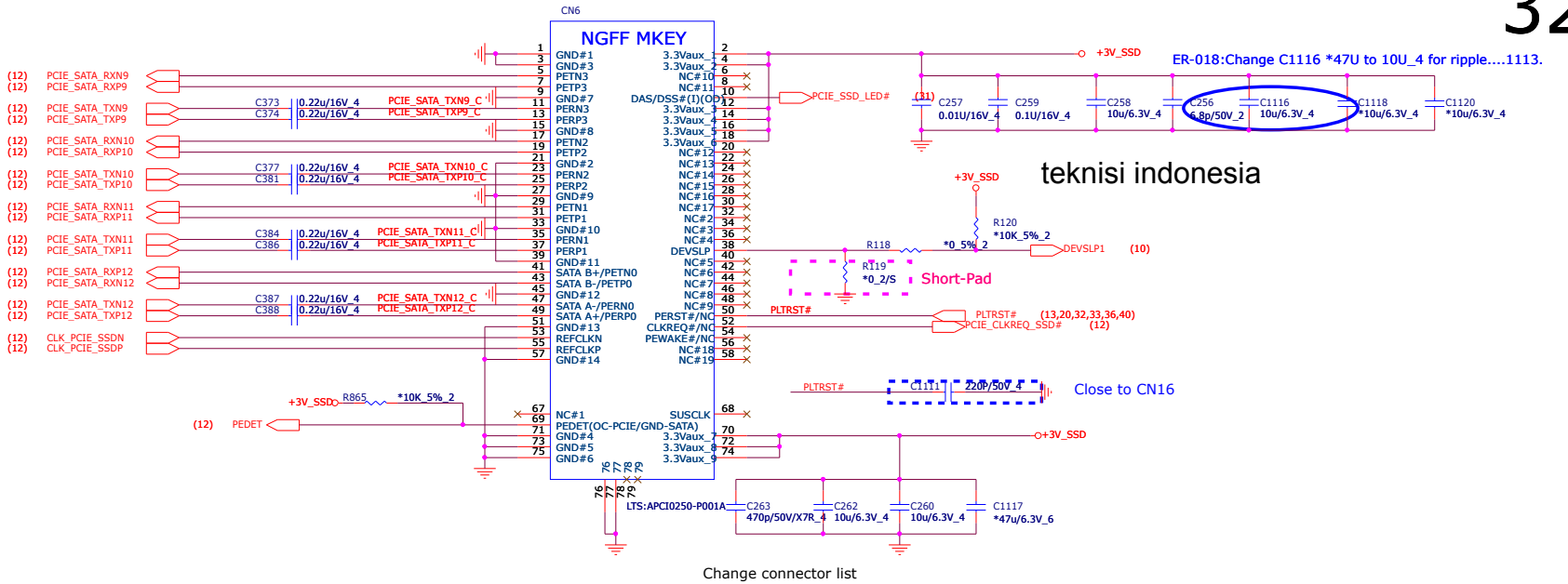




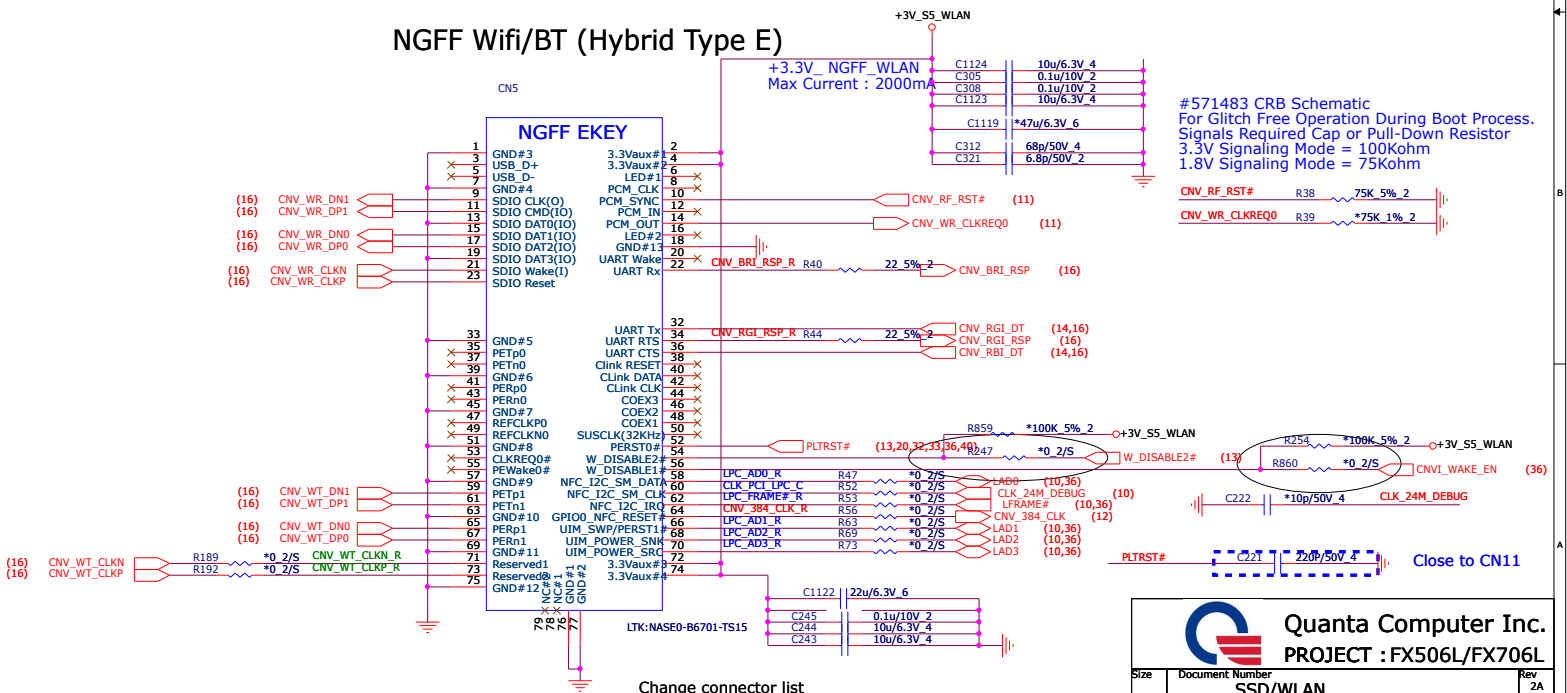
Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	HDD/LED	2A
Date: Thursday, March 26, 2020	Sheet 31 of 59	

Main SSD



WLAN/BT



Quanta Computer Inc.			
PROJECT : FX506L/FX706L			
Size	Document Number		Rev
	SSD/WLAN		2A
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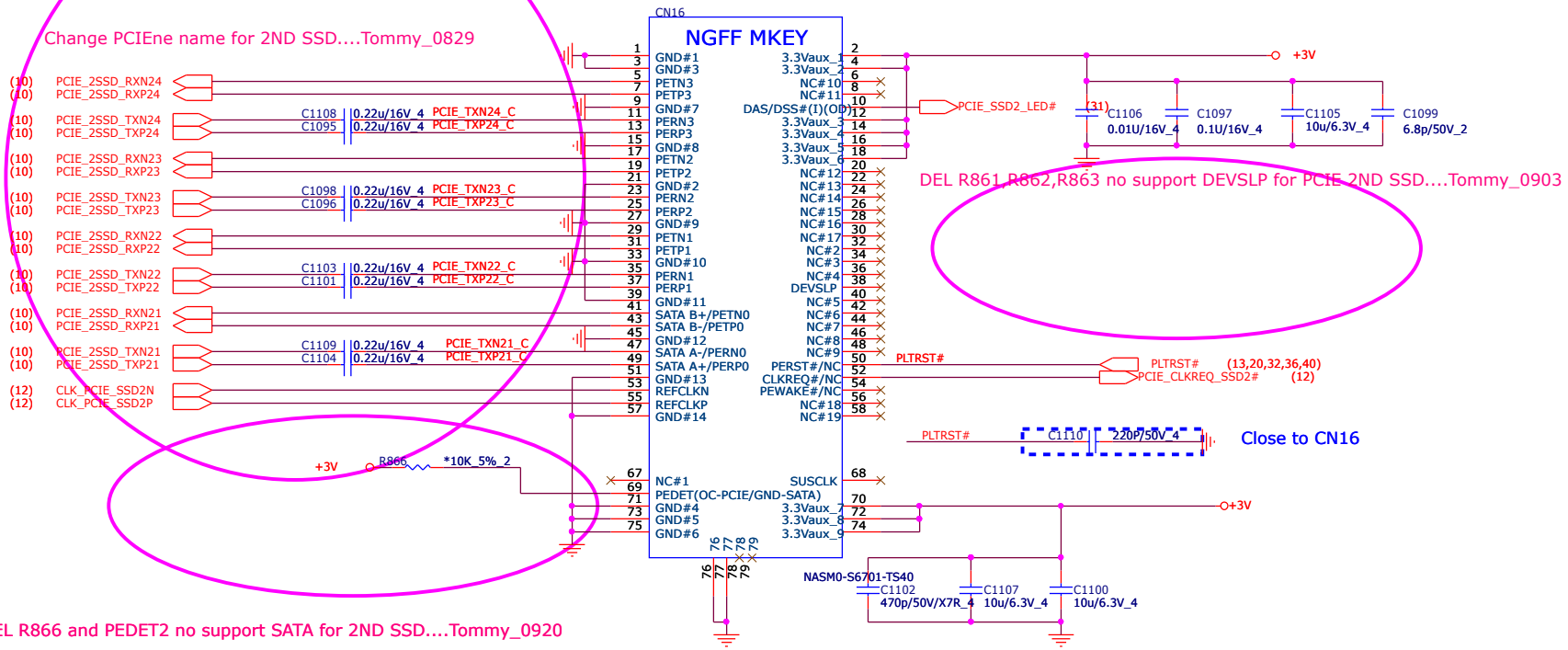
2ND SSD



Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
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	2ND SSD	2A
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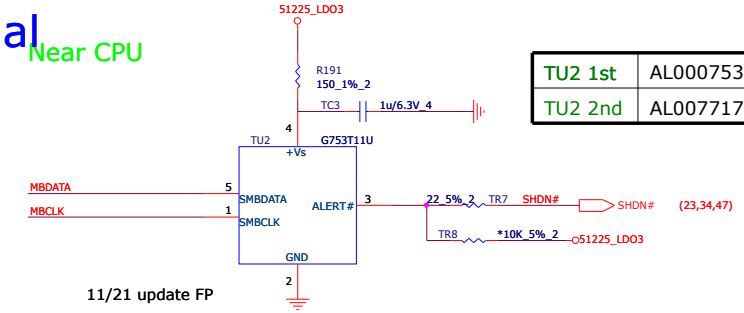
Thermal

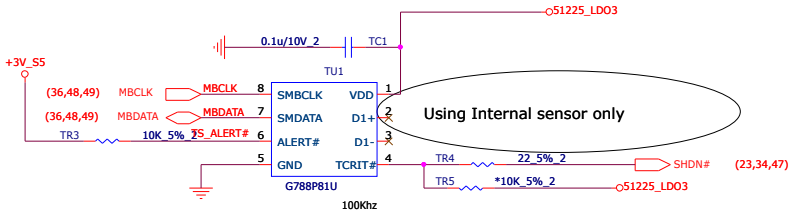
Near CPU

TU2 1st	AL000753000
TU2 2nd	AL007717000

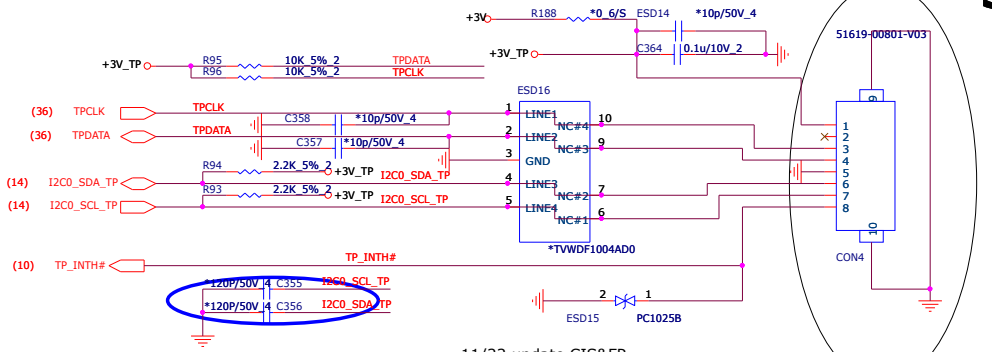


11/21 update FP

Near GPU



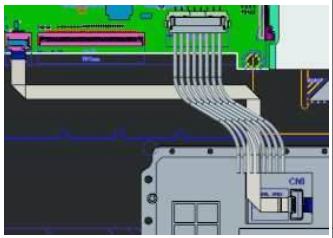
Touch Pad Connector AA type



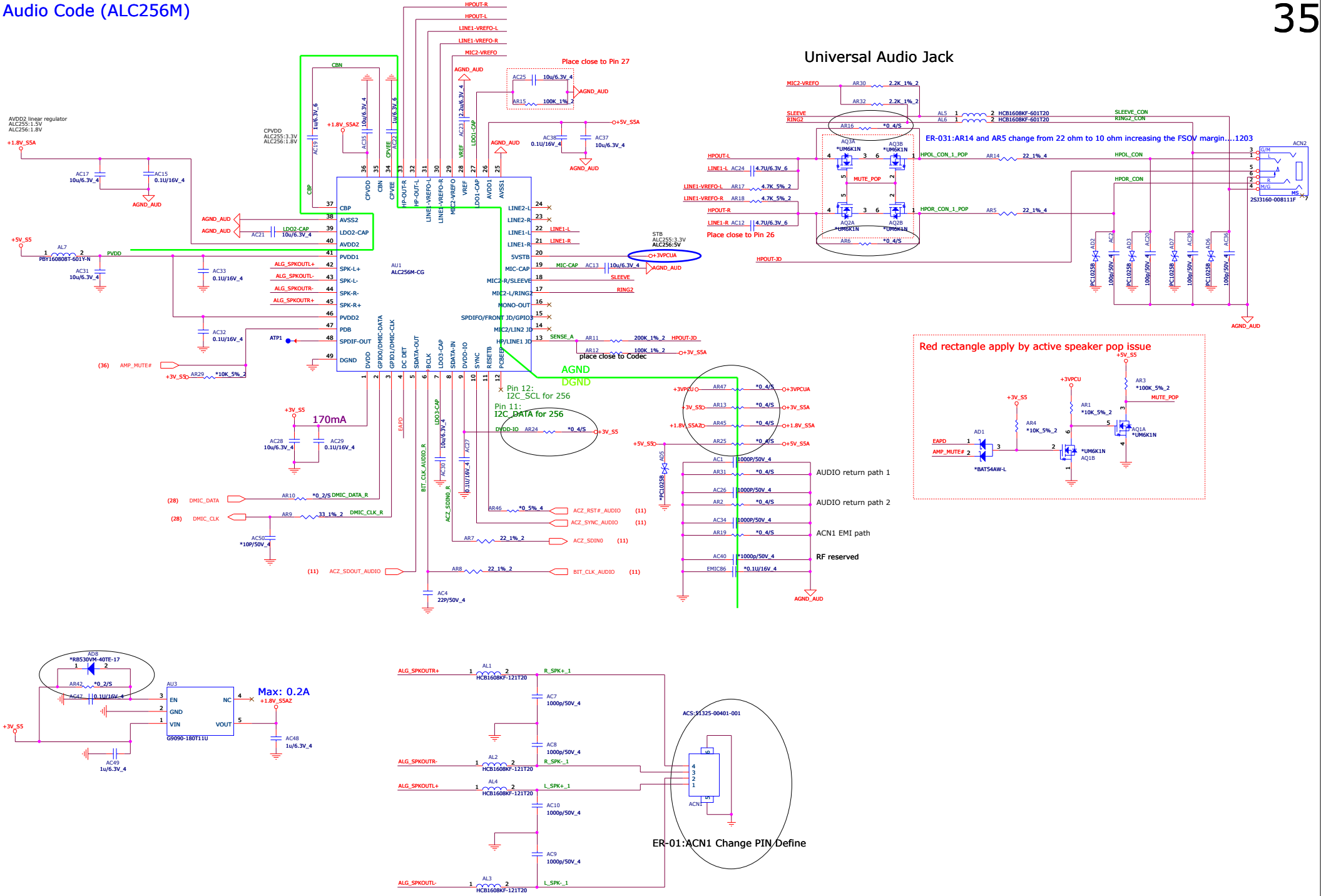
11/22 update CIS&FP

ER-029: Change C355,C356 to no-mount for fix TP timing issue....1122.

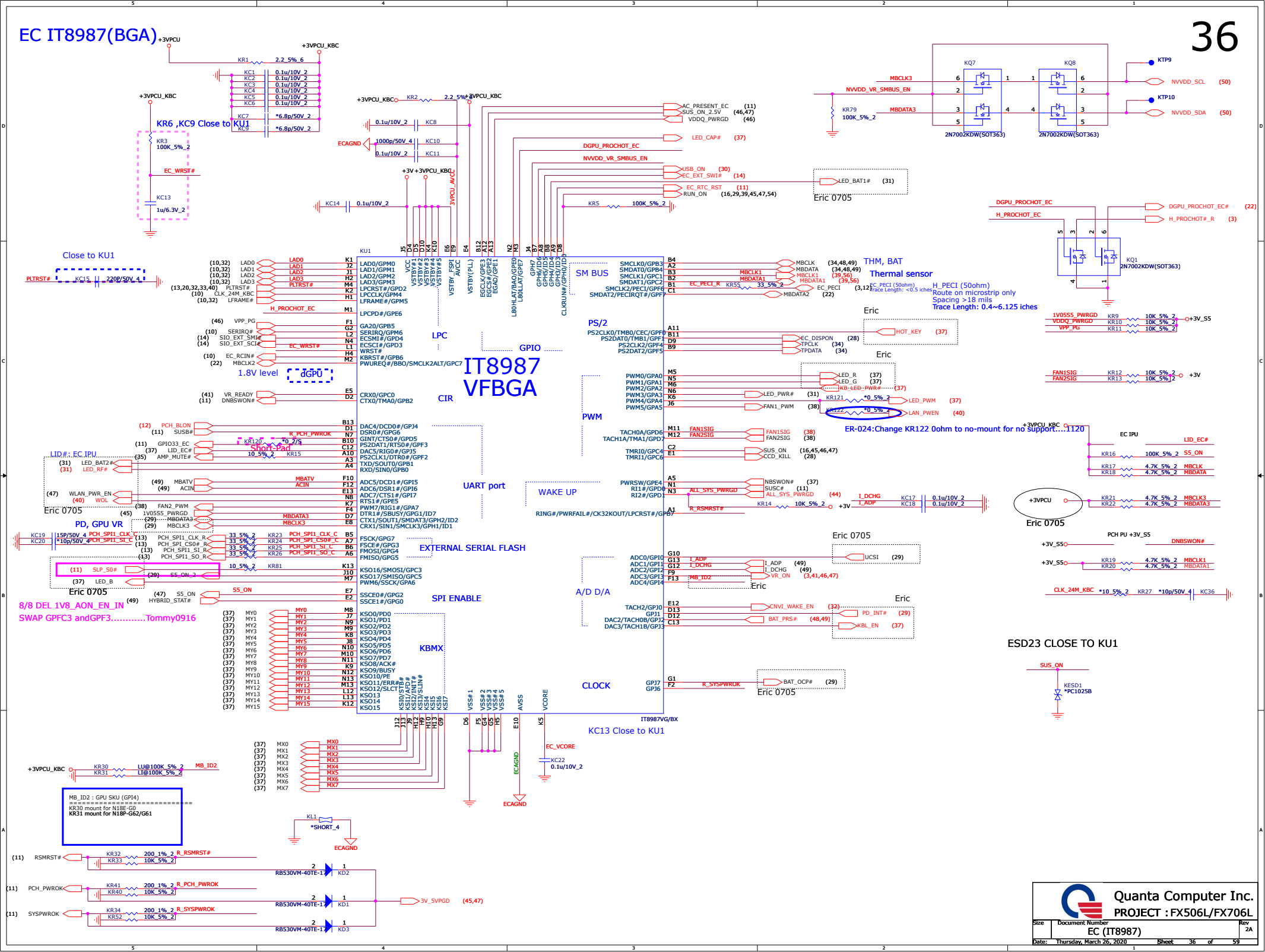
Change connector list



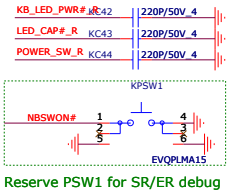
Audio Code (ALC256M)



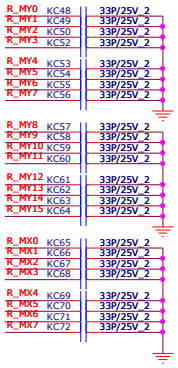
EC IT8987(BGA)

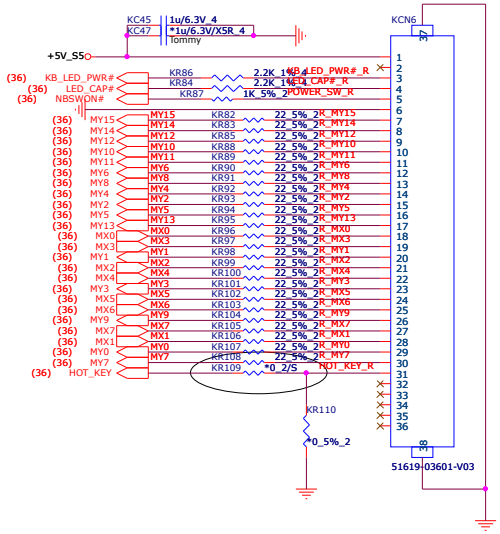


KEYBOARD Con.



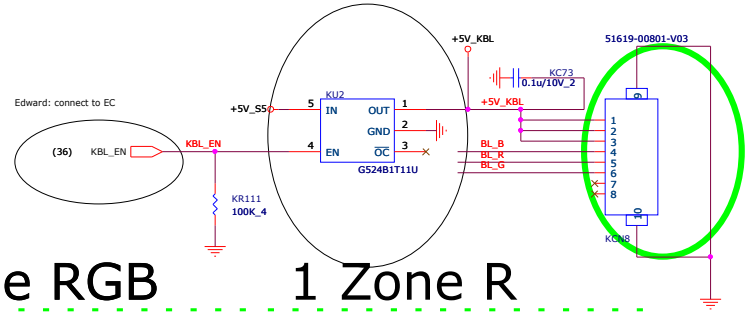
Reserve PSW1 for SR/ER debug



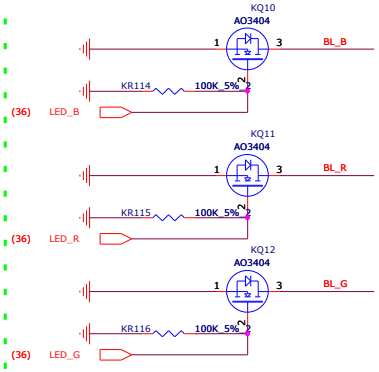


KEYBOARD BACKLIGHT Con.

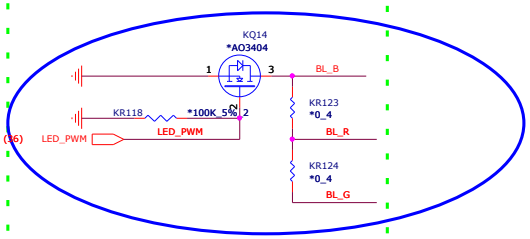
8/7 Change to footprint.



1 Zone RGB

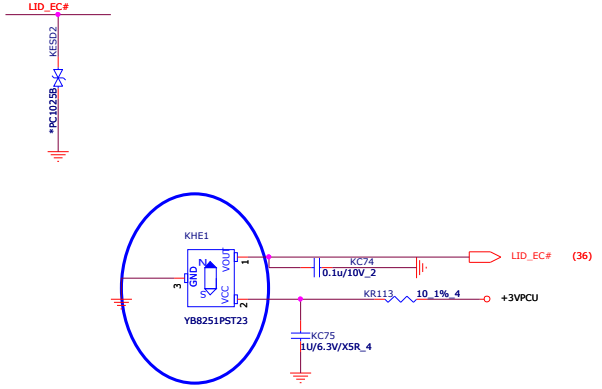


1 Zone R



ER-031:Del KQ15/KQ13 for no support Red backlight....1125.

ESD23 CLOSE TO KHE1



ER-033:Change footprint for SMT request....1126.

Quanta Computer Inc.
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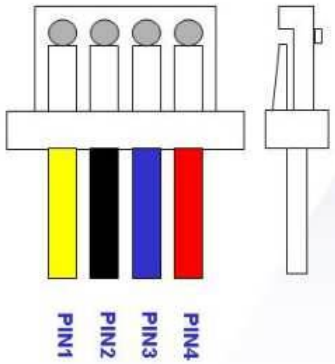
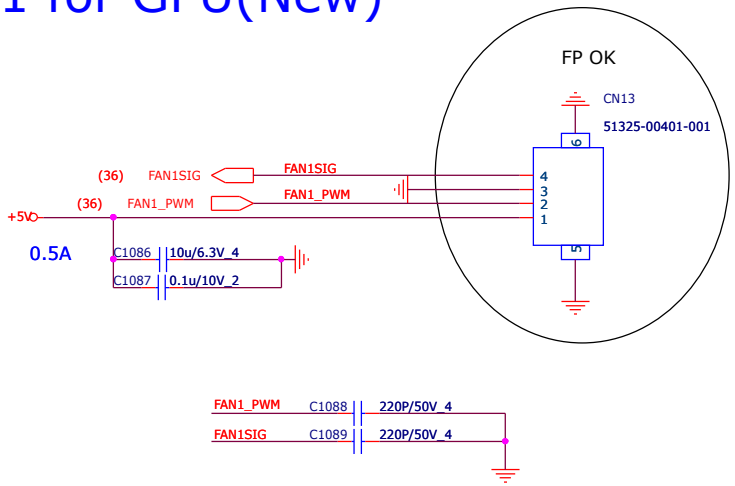
4Pins Fan Connector Pins Definition

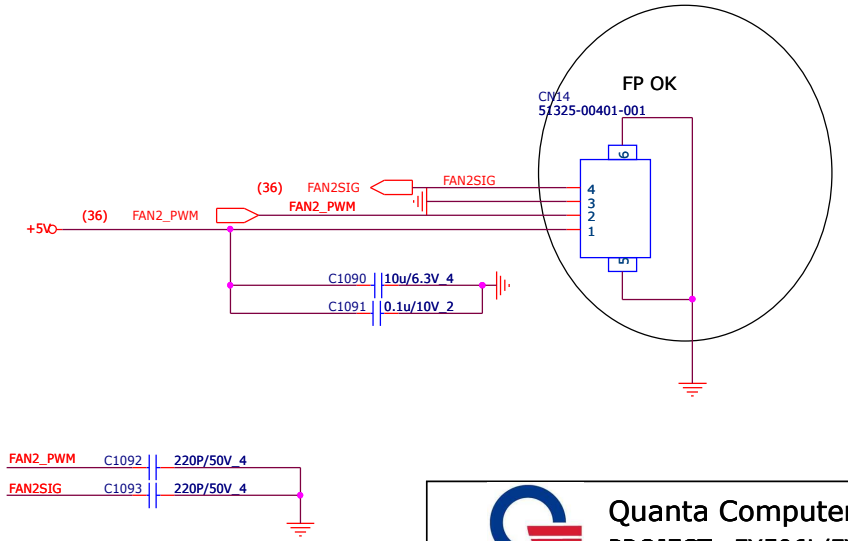


Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

FAN1 for GPU(New)



FAN2 for CPU



Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	FAN	2A
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HDMI 2.0 Re-Driver

ER-011:Change no mount:HQ3, NO USED....1113.

Optional

ER-004:Change +1.2V to +1.2V_HDMI power rail name....1113

ER-026: Change 2.1ohm to 5.1ohm for fix TDR issue....1122.

I2C address:0x19-02xF

NV_DP_HPD to PCH and Level shift to NV

From GPU

EMI Solution

FP & PN changed

Near CON side

Near CON side

20 mils

PR-E08:HDMI DDC pull-up resister change from 2.2K to 3K for HDMI protocol issue

HPD and +5V_HDMI use TPUC0521NE only

teknisi indonesia

Prevent current leakage when GPU is power off

ER-007:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113

Internally pull up ~150K

Internally pull up ~150K

DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input

Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensaton for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

I2C Slave Address selection; Internal pull down, 3.3V I/O:
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.

HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

Quanta Computer Inc.
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	HDMI 2.0 Redriver	2A

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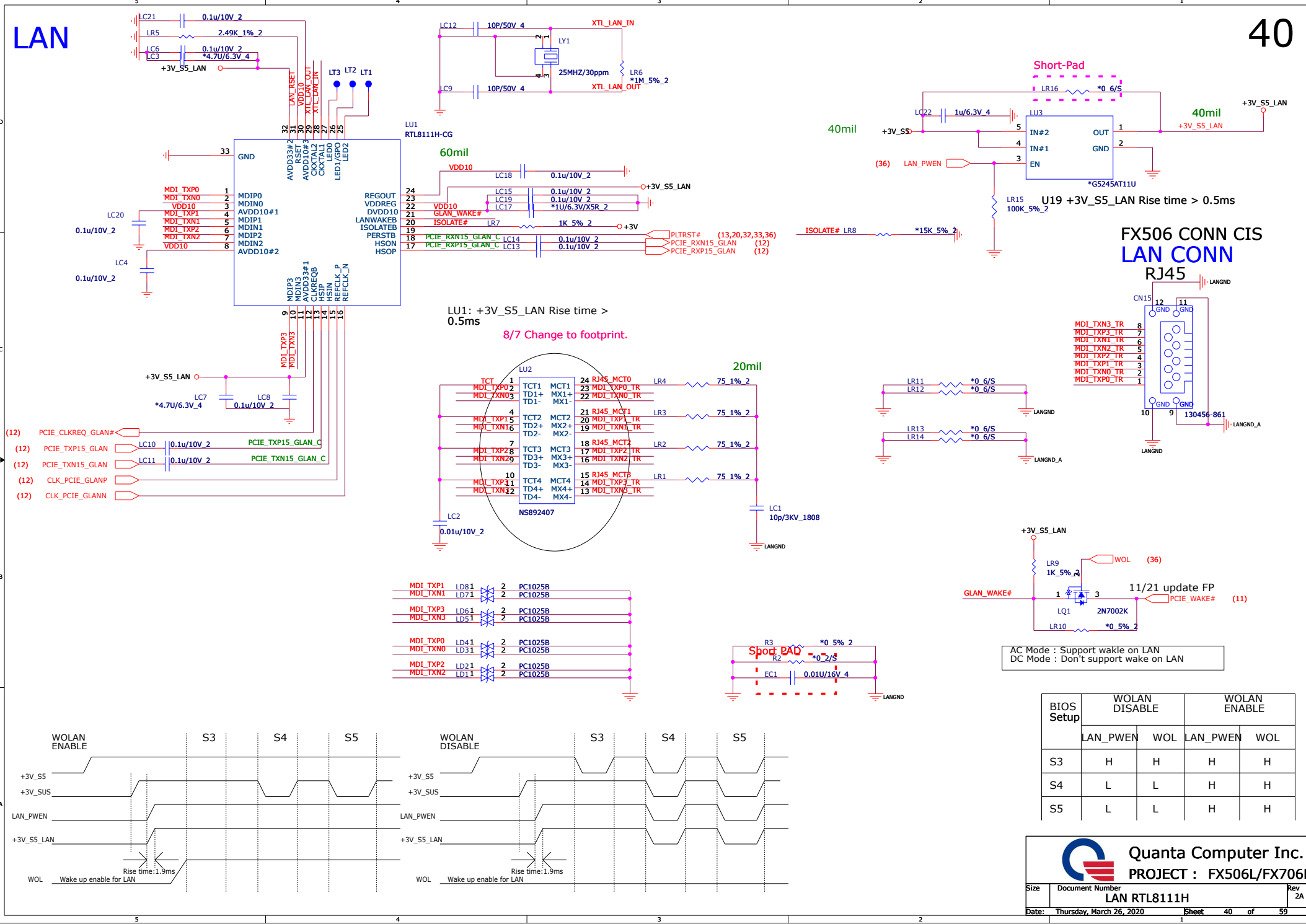
LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

Quanta Computer Inc.
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	LAN RTL8111H	2A
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45W H62/H42: GFX_CORE LL=-2.7mV/A

I@ is for H42
E@ is for H62

	H62	H42
PR1078	442_1%_4(CS14422FB16)	287_1%_4(CS12872FB18)
PR1057	107K_1%_4(CS41072FB11)	71.5K_1%_4(CS37152FB11)
PR1070	5.11K_1%_4(CS25112FB15)	3.3K_1%_4(CS23302FB12)
PQ1228 PQ1231 Pq1232	QN3110M6N(BAM31100000)	**QN3109M6N(BAM31090000)**

Place NTC close to the GFX_CORE inductor

Place NTC close to the VCCSA inductor

ISL95880HRTZ-T

Typ Setting= 105C

Place NTC close to the VCORE Hot-Spot.

Place NTC close to the GFX_VCORE Hot-Spot.

Place NTC close to the VCORE inductor of phase 1

45W H62/H42: VCCSA LL=-10.3mV/A

45W H62/H42_Base: Max=11.1A, PL2=10A

45W H62/H42: VCORE LL=-1.7mV/A

PROG SETTING

PROG1 — PR1089 110K_1%_2 — 95855-PROG1
PROG2 — PR1093 1.87K_1%_2 — 95855-PROG2
PROG3 — PR1090 41.2K_1%_2 — 95855-PROG3
PROG4 — PR1094 121K_1%_2 — 95855-PROG4
PROG5 — PR1091 63.4K_1%_2 — 95855-PROG5

VR_A: VCORE, 45W-H62/H42: 3-Phase, Imax=128A, IOCP=189A, FSW=300K
VR_B: GFXCORE, H62/H42: 1-Phase, Imax=32A, IOCP=51.4A, FSW=300K
VR_C: VCCSA, H62/H42: Imax=11.1A, IOCP=20.4A, FSW=583K

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Size | Document Number: CPU CONTROL IC/VCCSA | Rev 3A
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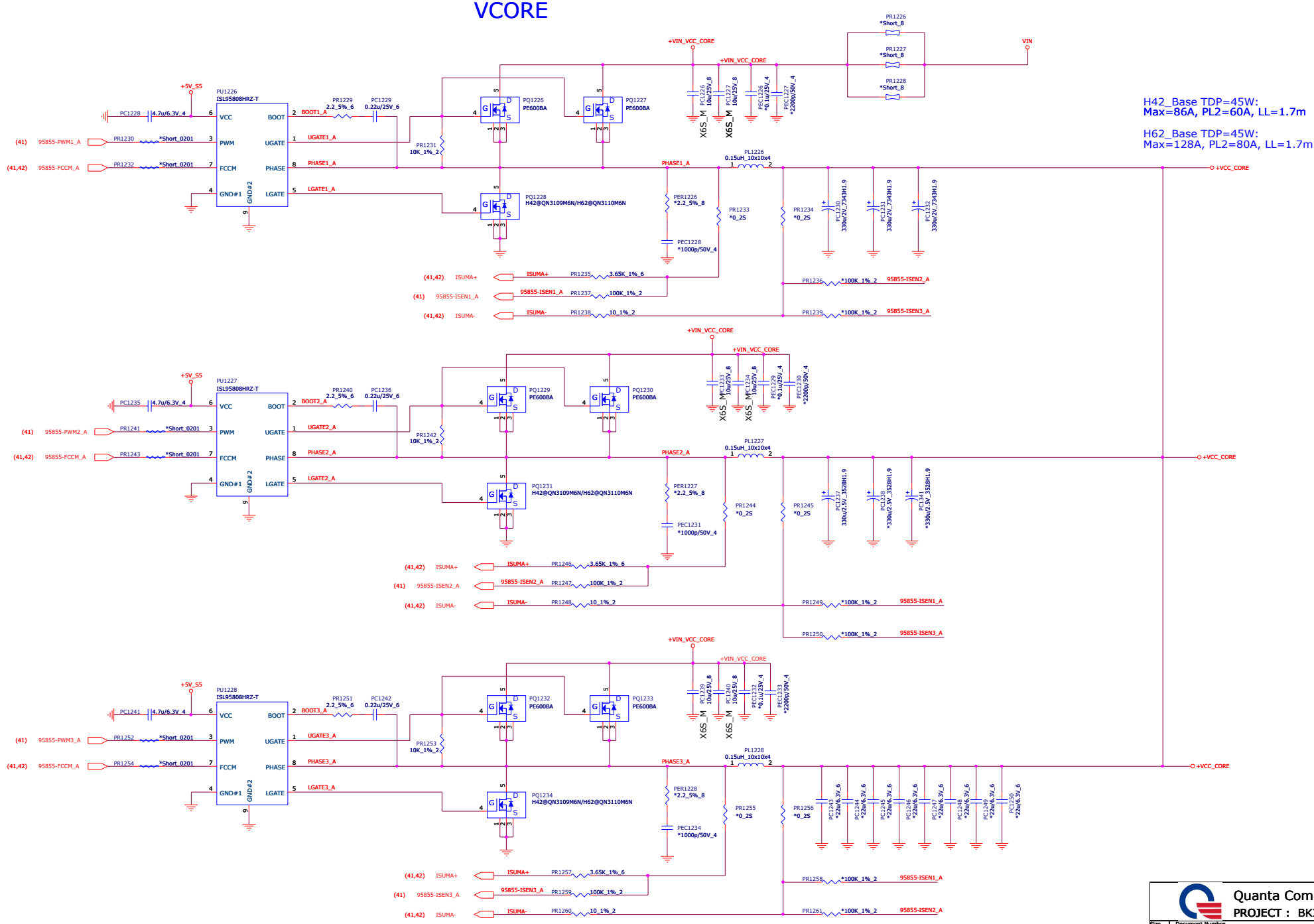
VCORE



Quanta Computer Inc.
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	VCORE POWER	3A
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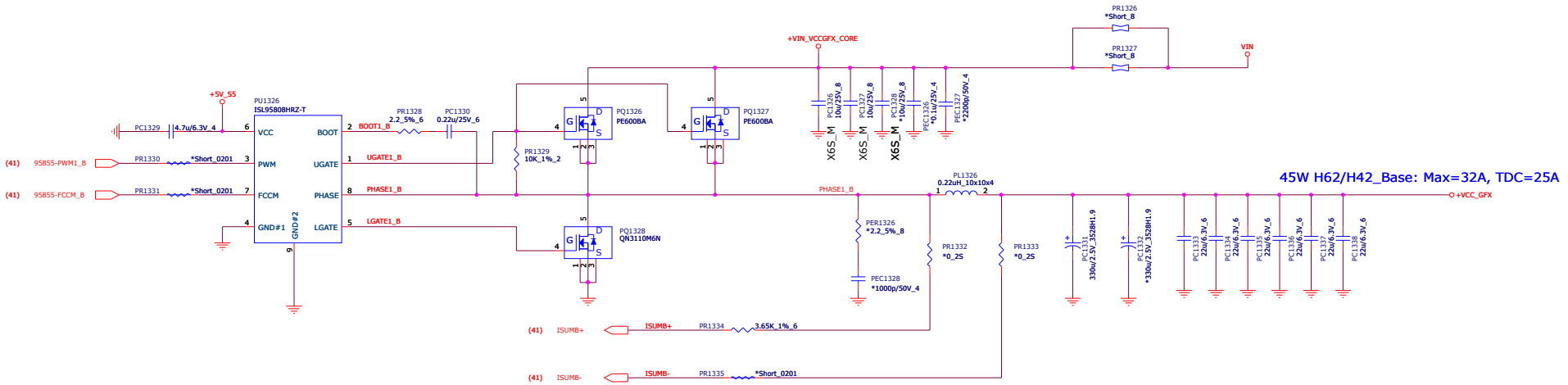
GFX_CORE



Quanta Computer Inc.		
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Size	Document Number: GFX CORE POWER	Rev: 3A
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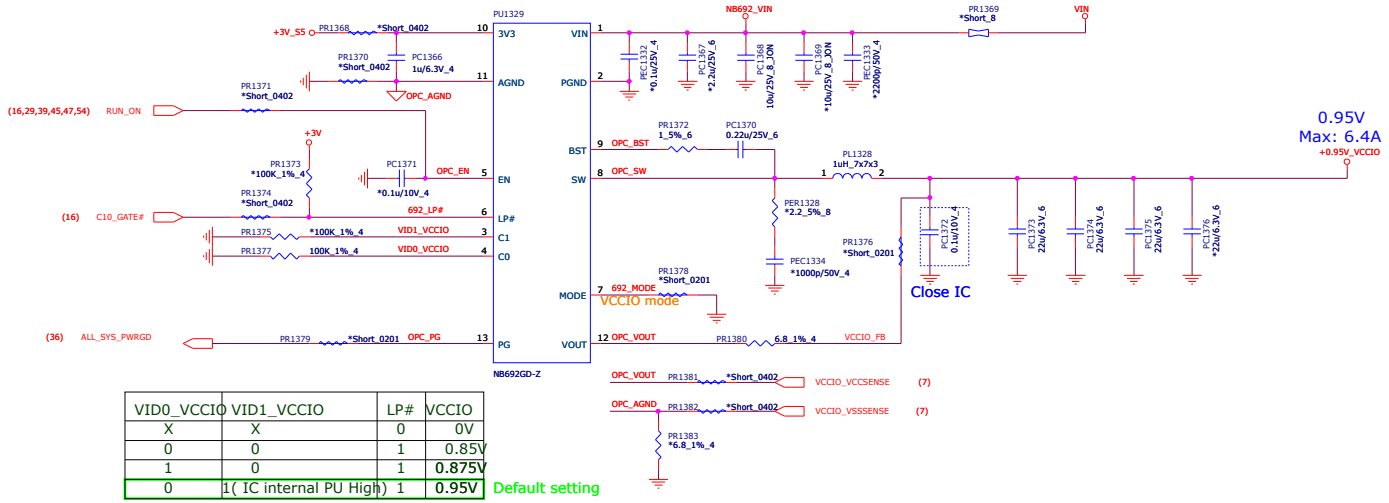
VCCIO



VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	0.875V
0	1(IC internal PU High)	1	0.95V

Default setting

Quanta Computer Inc.
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	POWER(1.05V_VCCPRIM/0.95V_VCCIO)	2A
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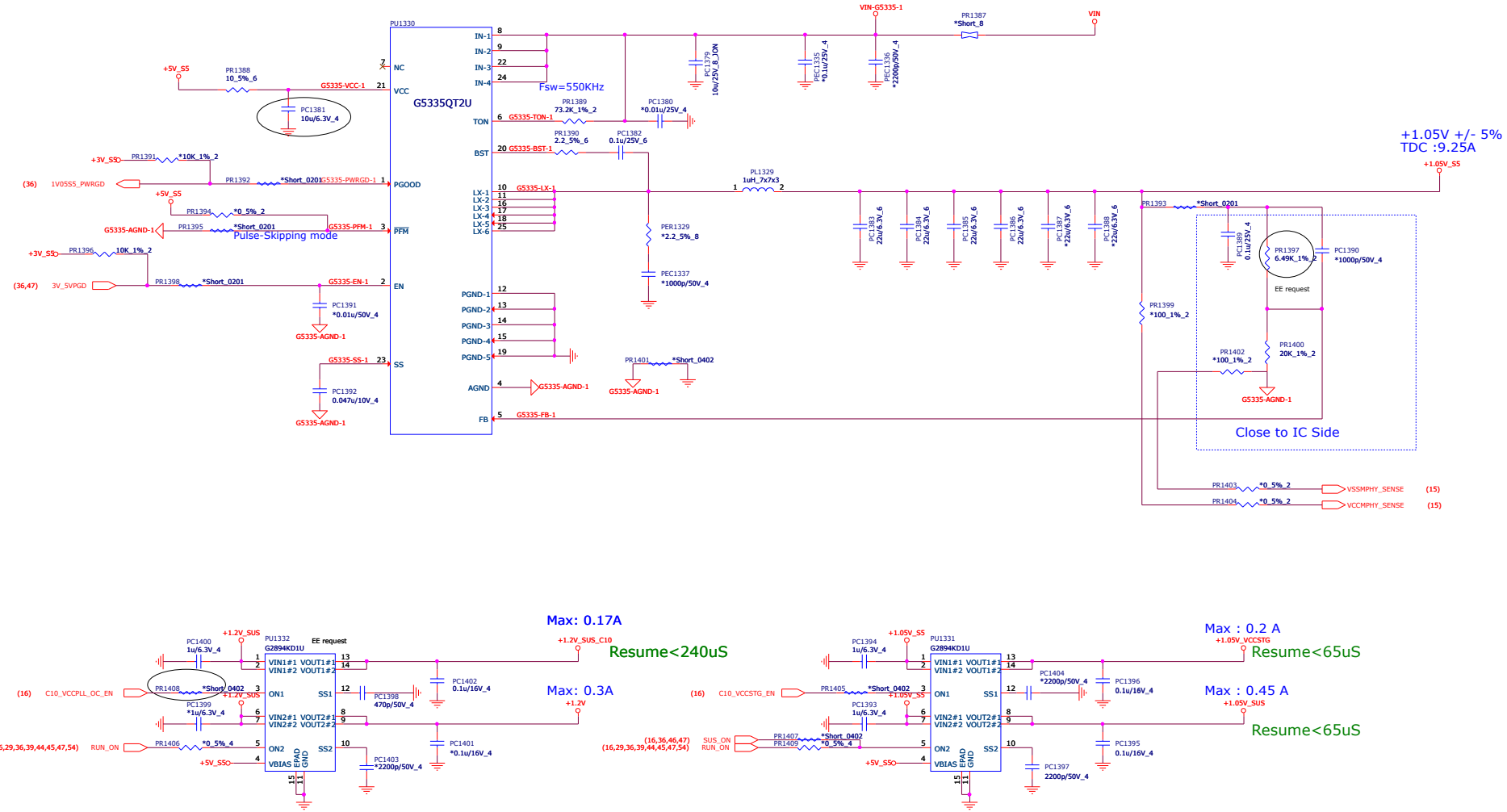
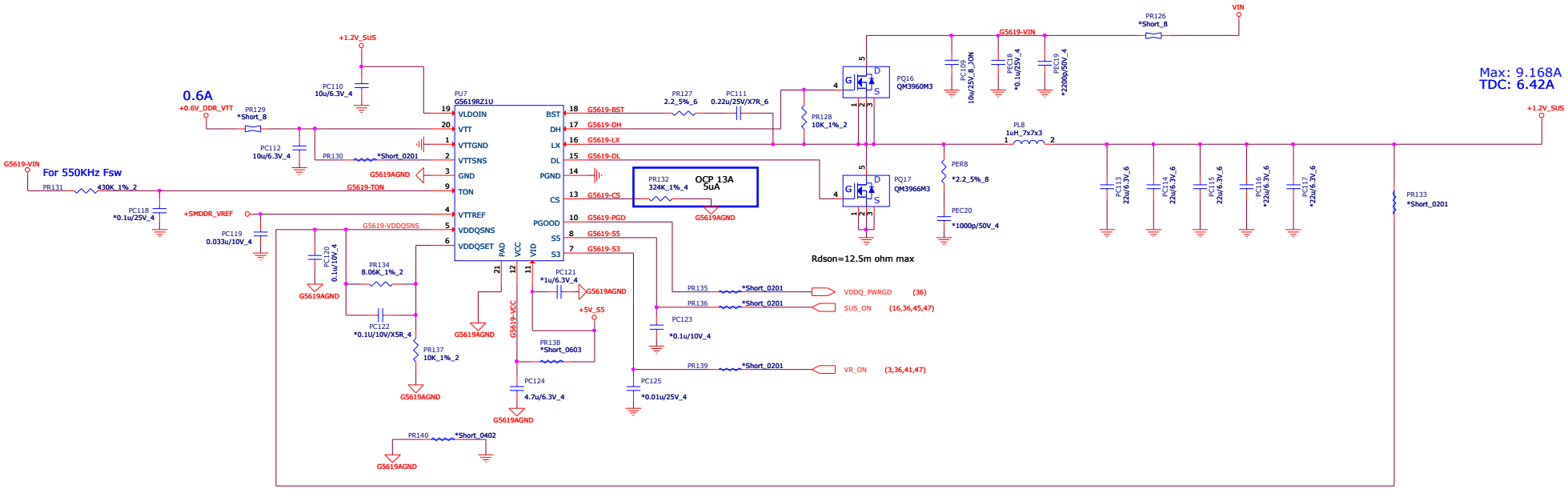
+1.05V_S5

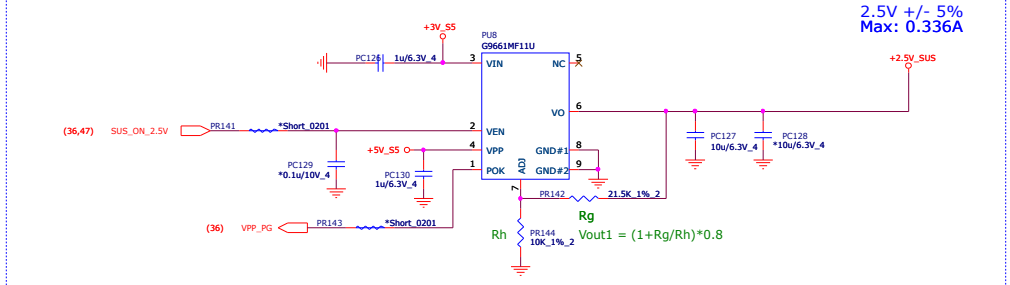

PU1330
G5335QT2U
NC
VCC
PGOOD
PFM
EN
SS
TON
BST
LX-1
LX-2
LX-3
LX-4
LX-5
LX-6
IN-1
IN-2
IN-3
IN-4
PGND-1
PGND-2
PGND-3
PGND-4
PGND-5
AGND
FB
Fsw=550KHz
Pulse-Skipping mode
EE request
Close to IC Side
+1.05V +/- 5%
TDC :9.25A
Max: 0.17A
Resume<240uS
Max: 0.3A
Max : 0.2 A
Resume<65uS
Max : 0.45 A
Resume<65uS
PU1332
PU1331
G2894KD1U

1.2VSUS & VTT_MEM



STATE	S3	S5	+1.2V_SUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

+2.5V_SUS



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	1.2VSUS/VTT		3A
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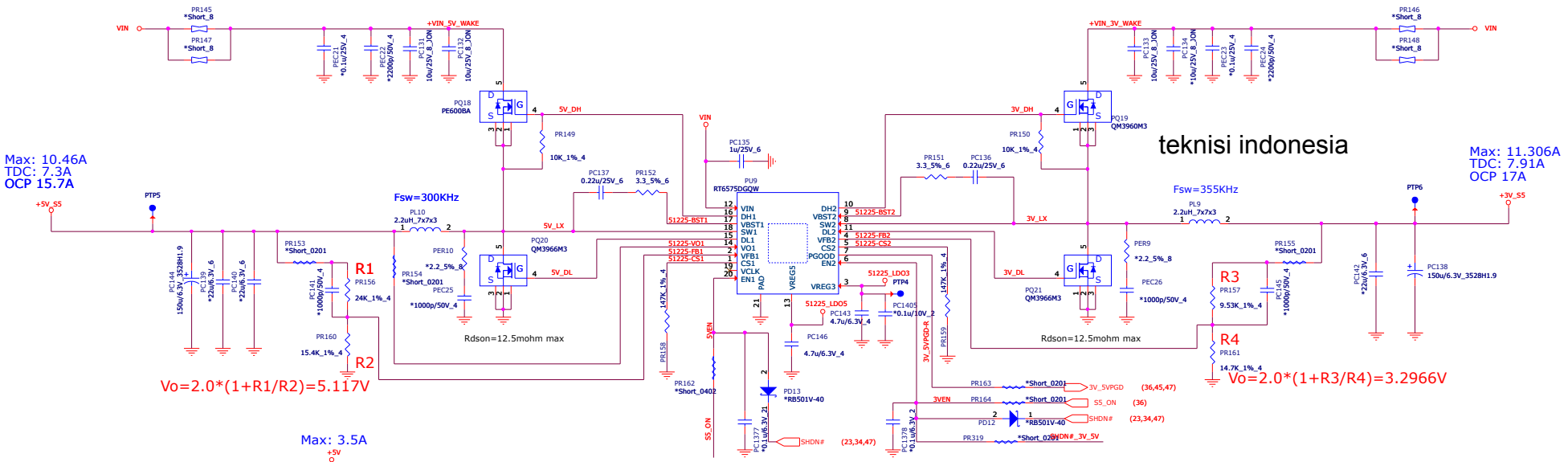
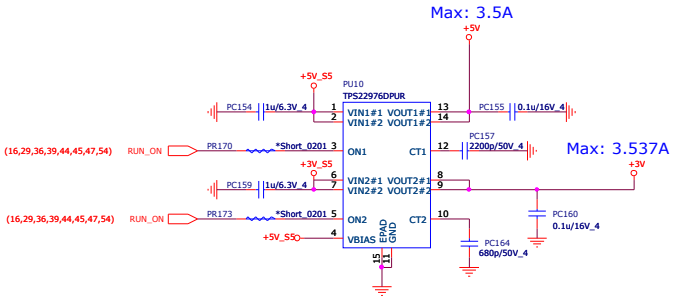
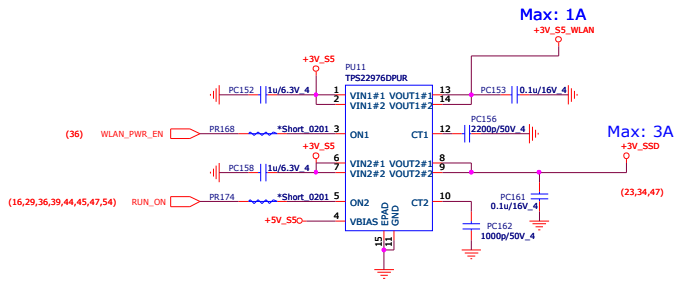
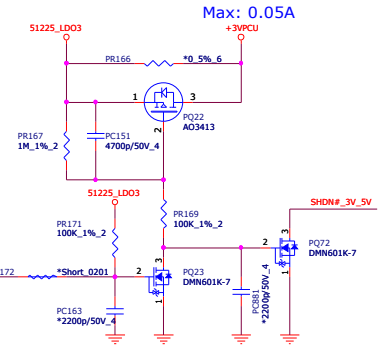
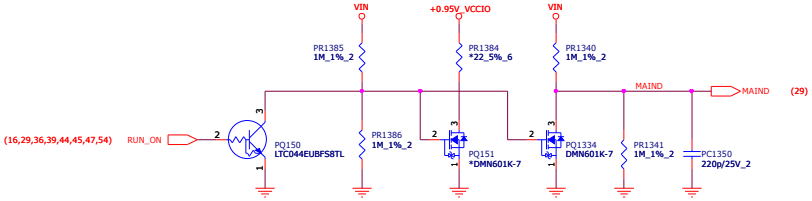
3.3V & 5V

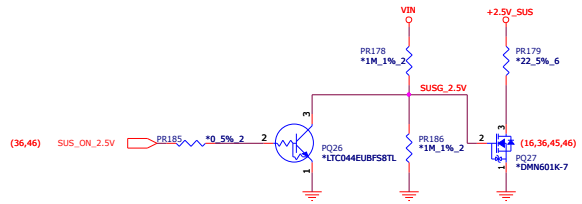


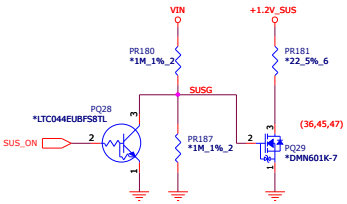


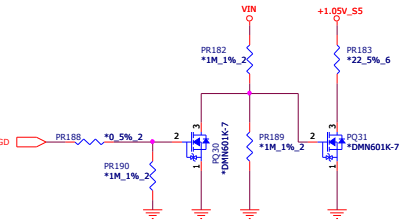


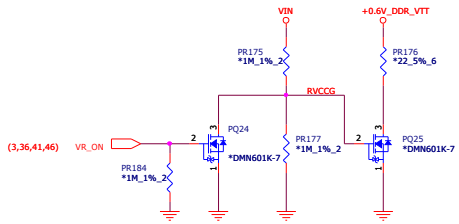












Quanta Computer Inc.
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	3.3V/5V	3A
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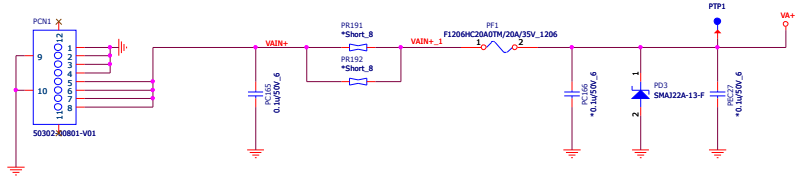
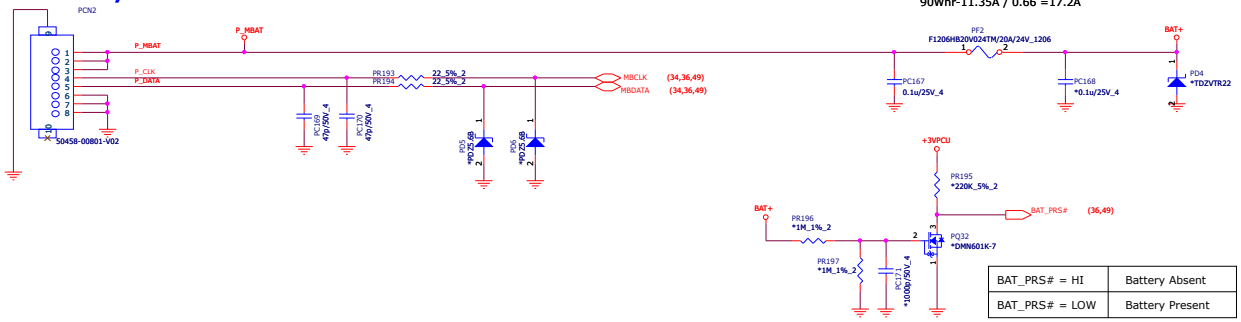
AC IN (On-Board DC-Jack)

Fuse Rating =
IR(max) /(0.75*0.88)
230W/19.5V / 0.66 =17.87A



Battery IN

Fuse Rating =
IR(max) /(0.75*0.88)
90Whr-11.35A / 0.66 =17.2A

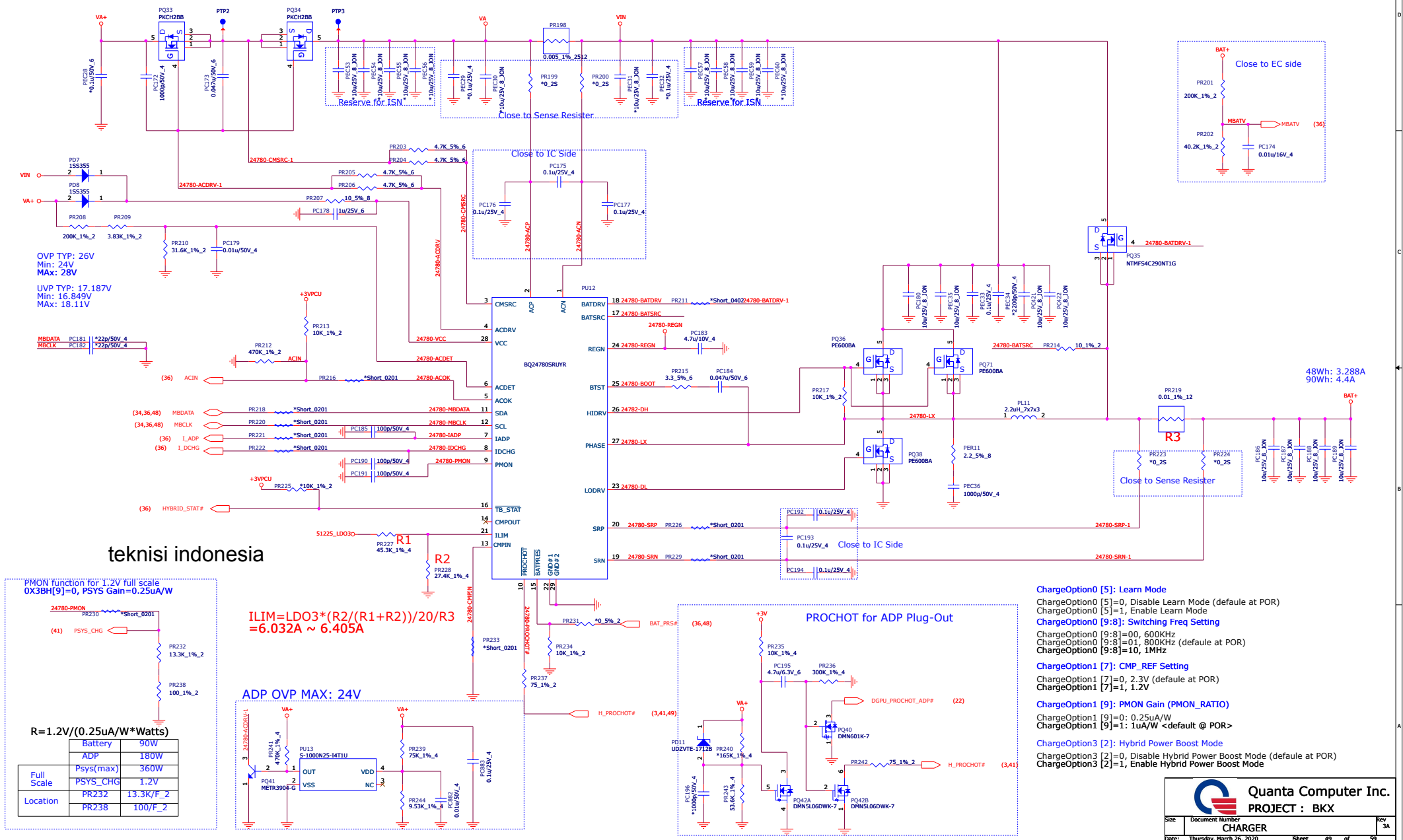


BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present

Quanta Computer Inc.
PROJECT : BKX

Size	Document Number	Rev
	AD IN/BAT IN	3A

Date: Thursday, March 26, 2020 Sheet 48 of 59


OVP TYP: 26V
Min: 24V
MAx: 28V
UVP TYP: 17.187V
Min: 16.849V
MAx: 18.11V
Reserve for ISN
Close to Sense Resister
Close to IC Side
Close to EC side
48Wh: 3.288A
90Wh: 4.4A
BQ24780SRUYR
teknisi indonesia
PMON function for 1.2V full scale
0X3BH[9]=0, PSYS Gain=0.25uA/W
R=1.2V/(0.25uA/W*Watts)
Battery 90W
ADP 180W
Full Scale
Psys(max) 360W
PSYS_CHG 1.2V
Location
PR232 13.3K_1%_2
PR238 100_1%_2
ILIM=LDO3*(R2/(R1+R2))/20/R3
=6.032A ~ 6.405A
ADP OVP MAX: 24V
PROCHOT for ADP Plug-Out
ChargeOption0 [5]: Learn Mode
ChargeOption0 [5]=0, Disable Learn Mode (defaule at POR)
ChargeOption0 [5]=1, Enable Learn Mode
ChargeOption0 [9:8]: Switching Freq Setting
ChargeOption0 [9:8]=00, 600KHz
ChargeOption0 [9:8]=01, 800KHz (defaule at POR)
ChargeOption0 [9:8]=10, 1MHz
ChargeOption1 [7]: CMP_REF Setting
ChargeOption1 [7]=0, 2.3V (defaule at POR)
ChargeOption1 [7]=1, 1.2V
ChargeOption1 [9]: PMON Gain (PMON_RATIO)
ChargeOption1 [9]=0: 0.25uA/W
ChargeOption1 [9]=1: 1uA/W <default @ POR>
ChargeOption3 [2]: Hybrid Power Boost Mode
ChargeOption3 [2]=0, Disable Hybrid Power Boost Mode (defaule at POR)
ChargeOption3 [2]=1, Enable Hybrid Power Boost Mode
Quanta Computer Inc.
PROJECT : BKX
CHARGER
Thursday, March 26, 2020
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contact to EC side separate SMBUS port

N18E-G0, TGP=80W, TDC=82A, Max=225A

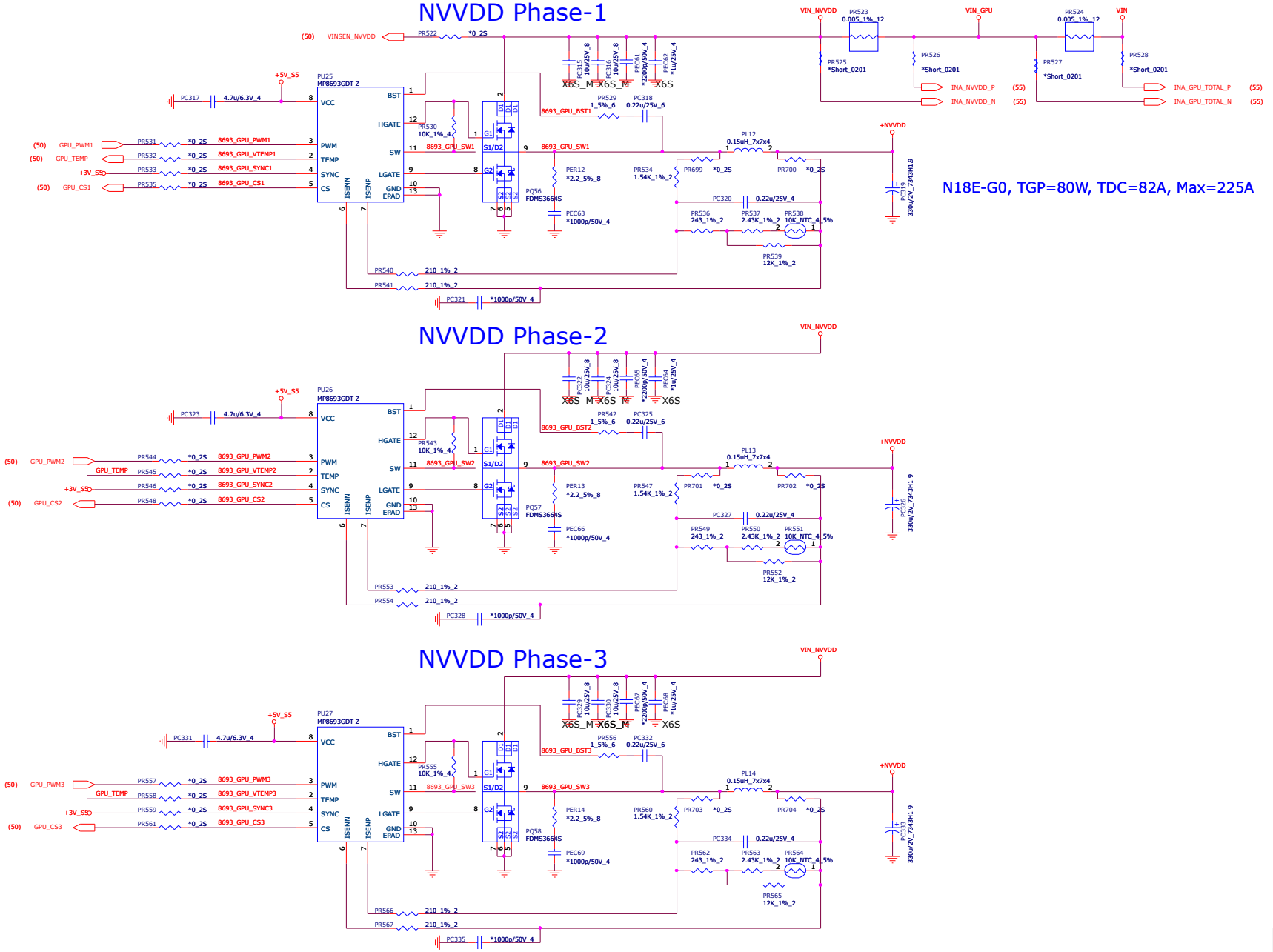
MP2886AGU-0135-Z : Switching Freq Setting=300KHz

Thermistor NTC close to hotest area

PSI	PWM Status
1	Forced CCM for all phases
0	Adjustable low phase count
Hi-Z	Auto phase-shedding enabled

MP2886AGU-0144-Z

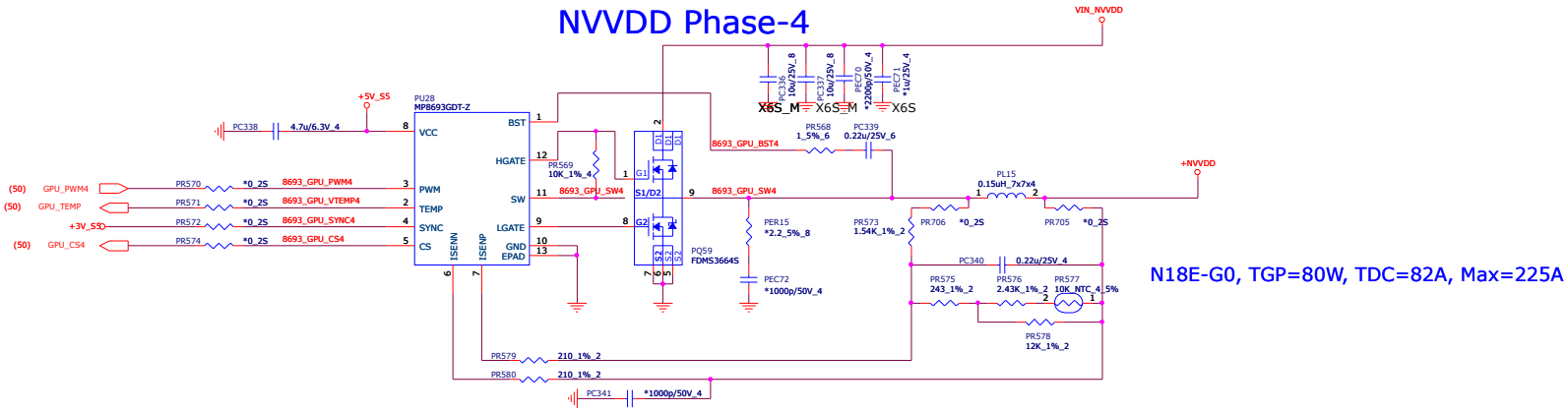
PU24



Quanta Computer Inc.
PROJECT : BKX

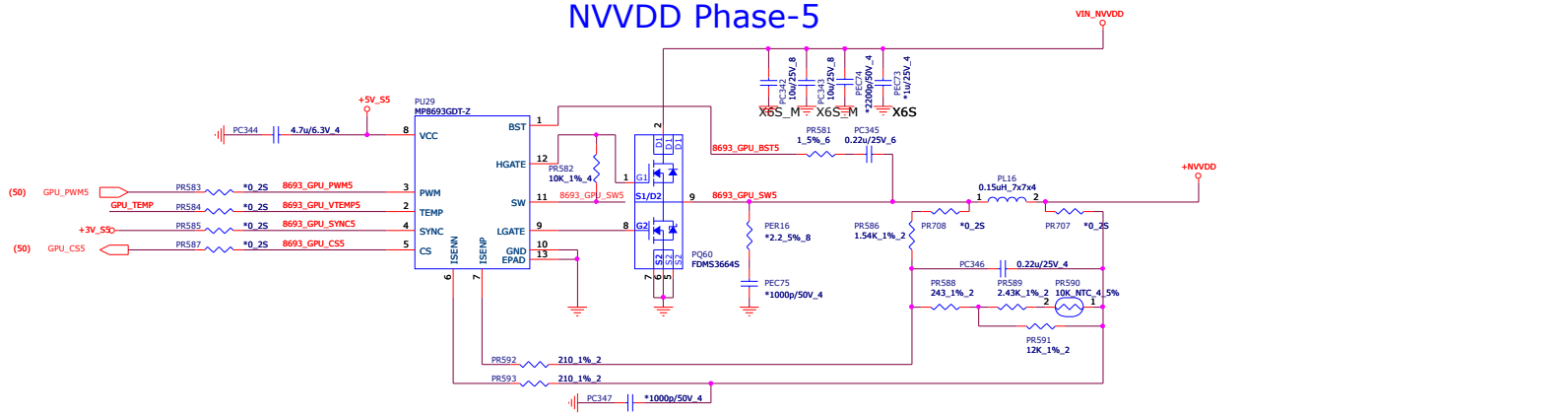
Size	Document Number	Rev
	dGPU CORE MP2886A)	2A
Date: Thursday, March 26, 2020	Sheet 51 of 59	

NVVDD Phase-4



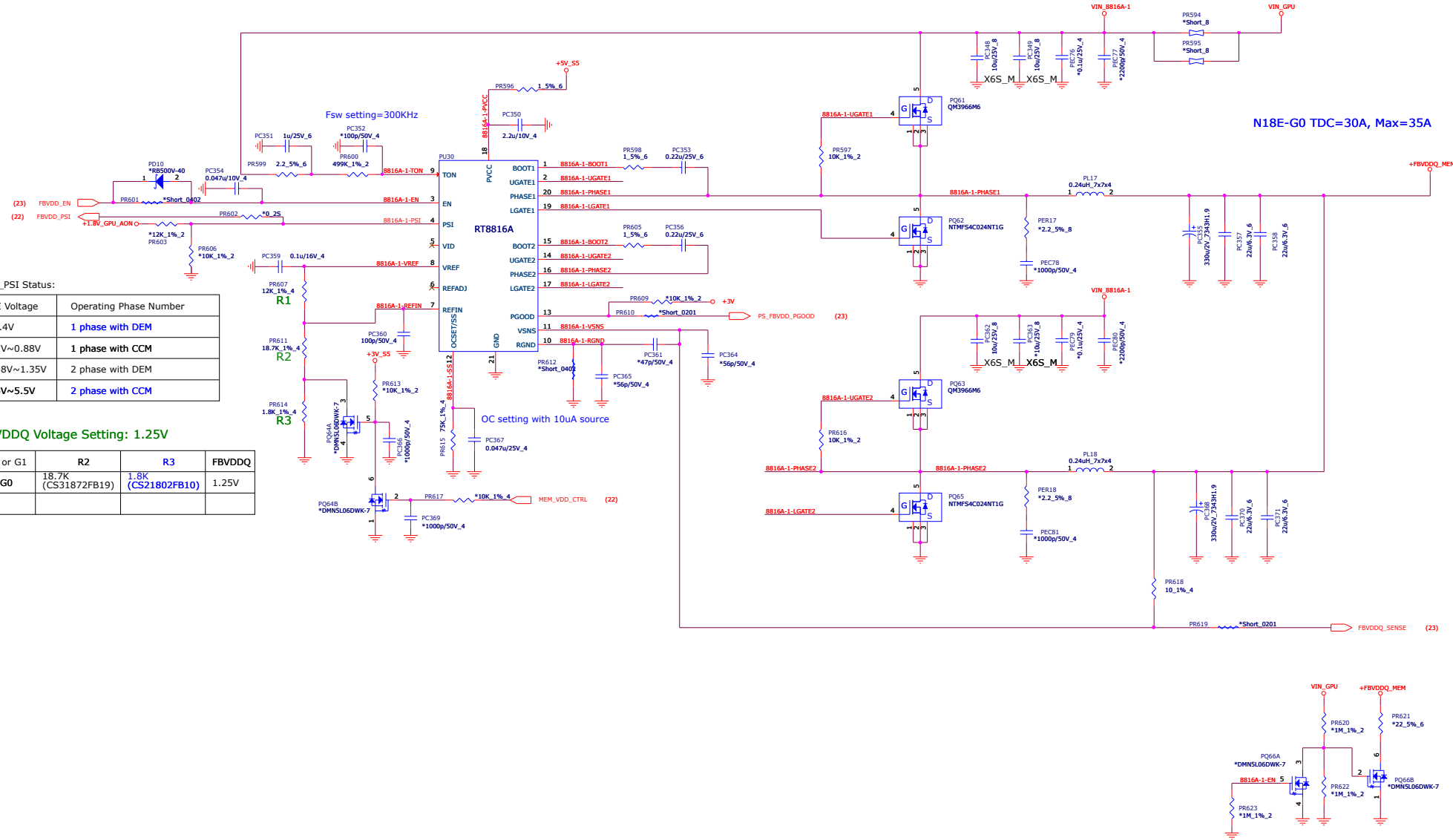
N18E-G0, TGP=80W, TDC=82A, Max=225A

NVVDD Phase-5



Quanta Computer Inc.		
PROJECT : BKX		
Size	Document Number: dGPU CORE MP2886A)	Rev: 2A
Date: Thursday, March 26, 2020	Sheet 52 of 59	

+FBVDDQ_MEM

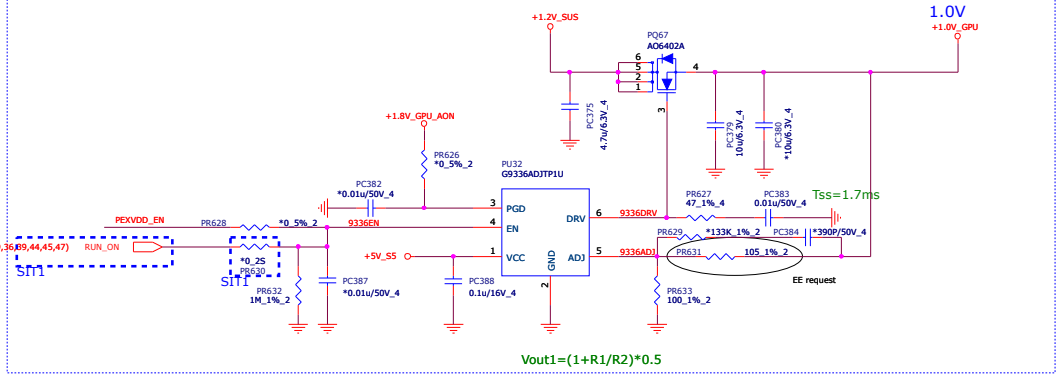


Quanta Computer Inc.	
PROJECT : BKX	
Size	Document Number: +FBVDDQ_MEM (RT8816A) — Rev 2A
Date: Thursday, March 26, 2020	Sheet 53 of 59

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

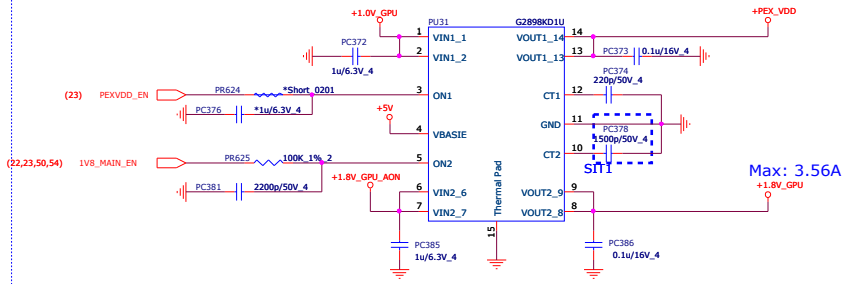
+1.0V_GPU

N18E-G0 TDC=1.6A, Max=2.5A

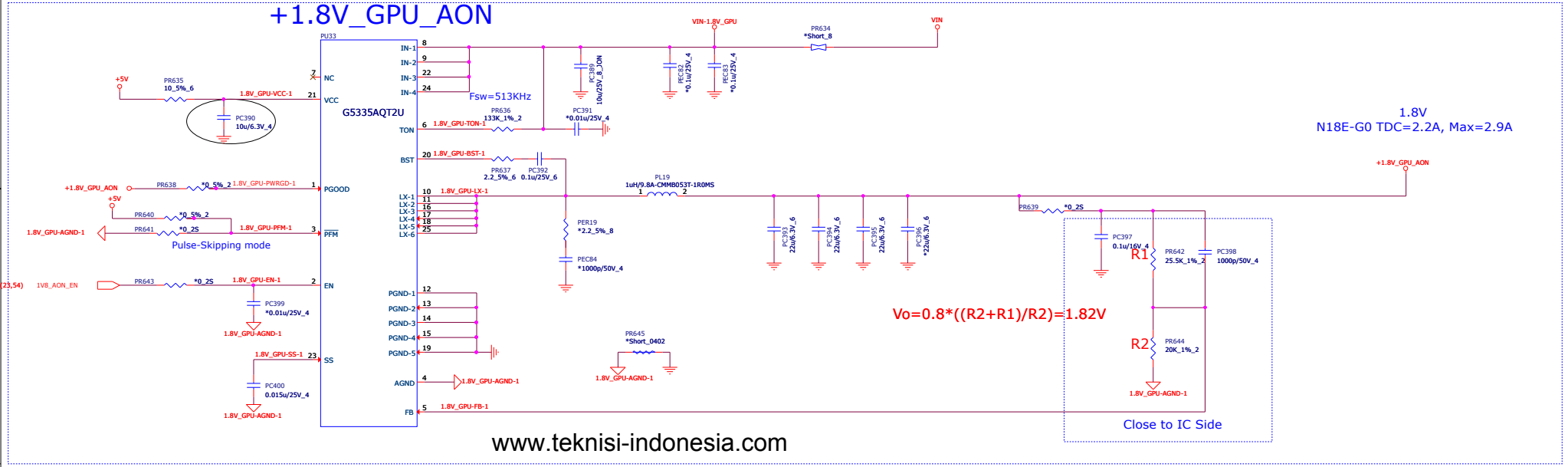


Load Switch for GPU

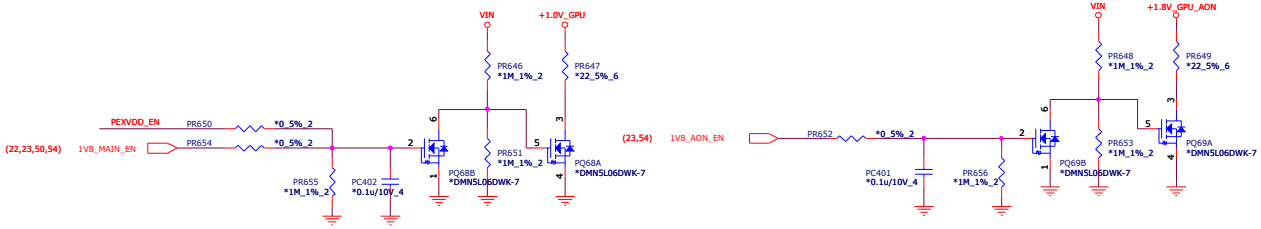
N18E-G0 TDC=1.6A, Max=2.5A

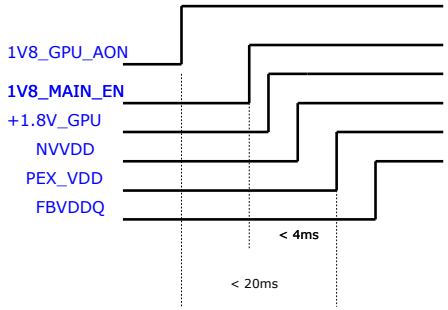


+1.8V_GPU_AON



Discharge

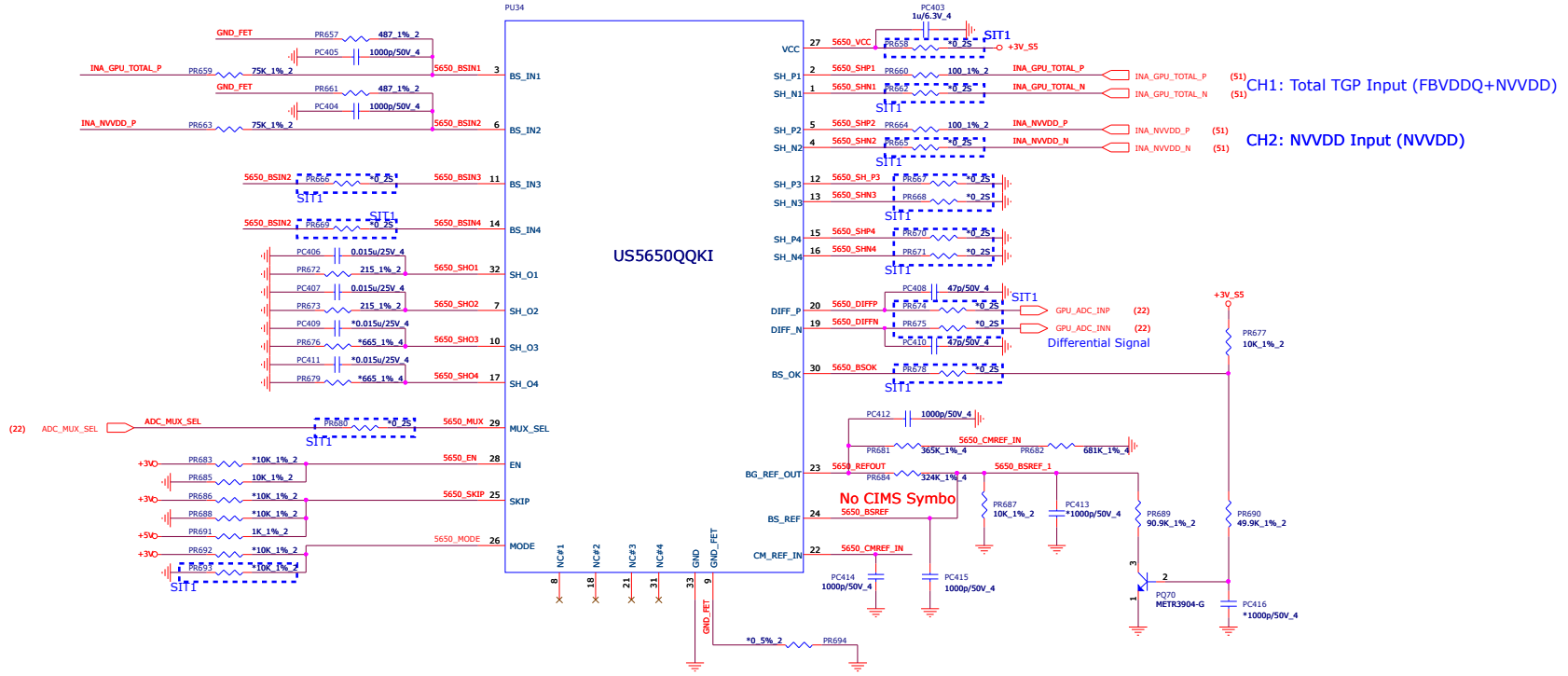




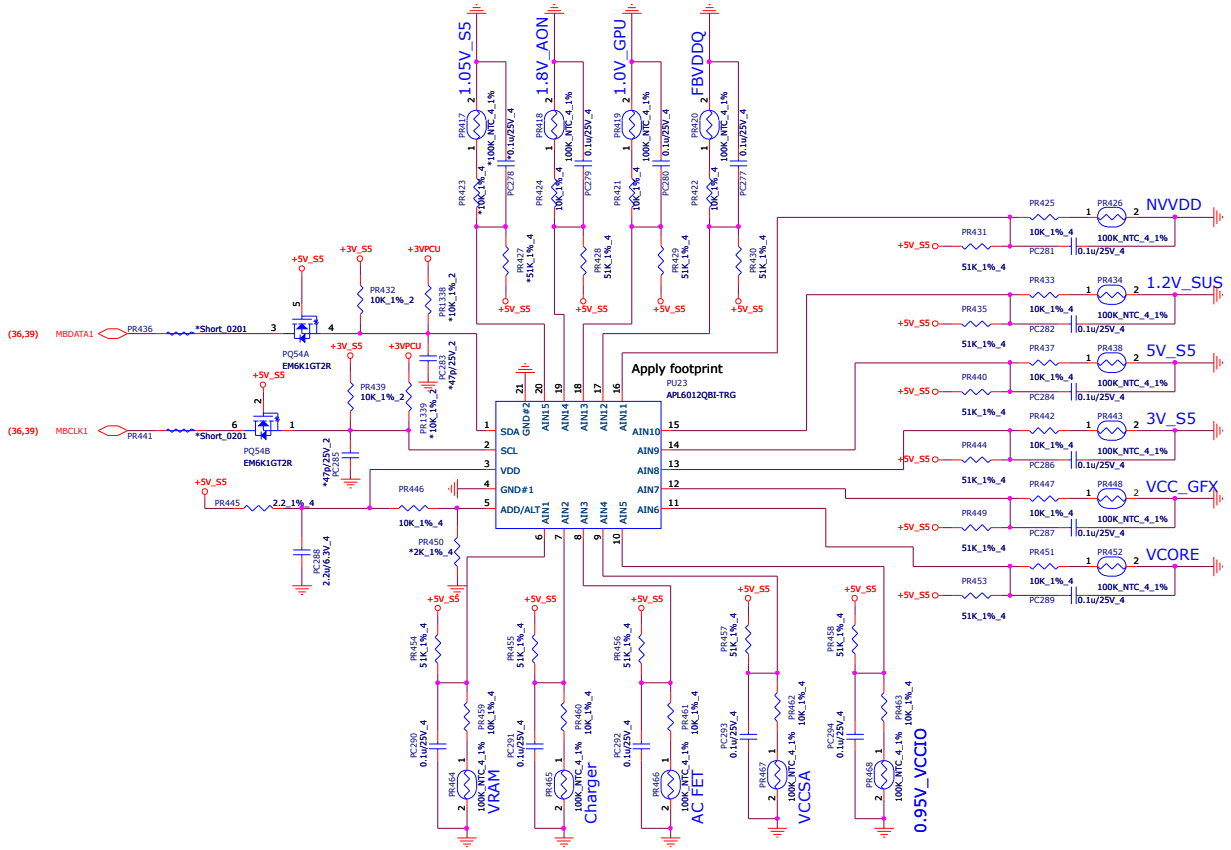
Quanta Computer Inc.
PROJECT : BKX

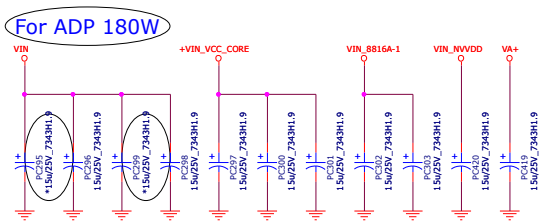
Size	Document Number	Rev
	+1.8V_GPU_AON / 1.0V_GPU	2A
Date: Thursday, March 26, 2020	Sheet 54 of 59	

OVR-M

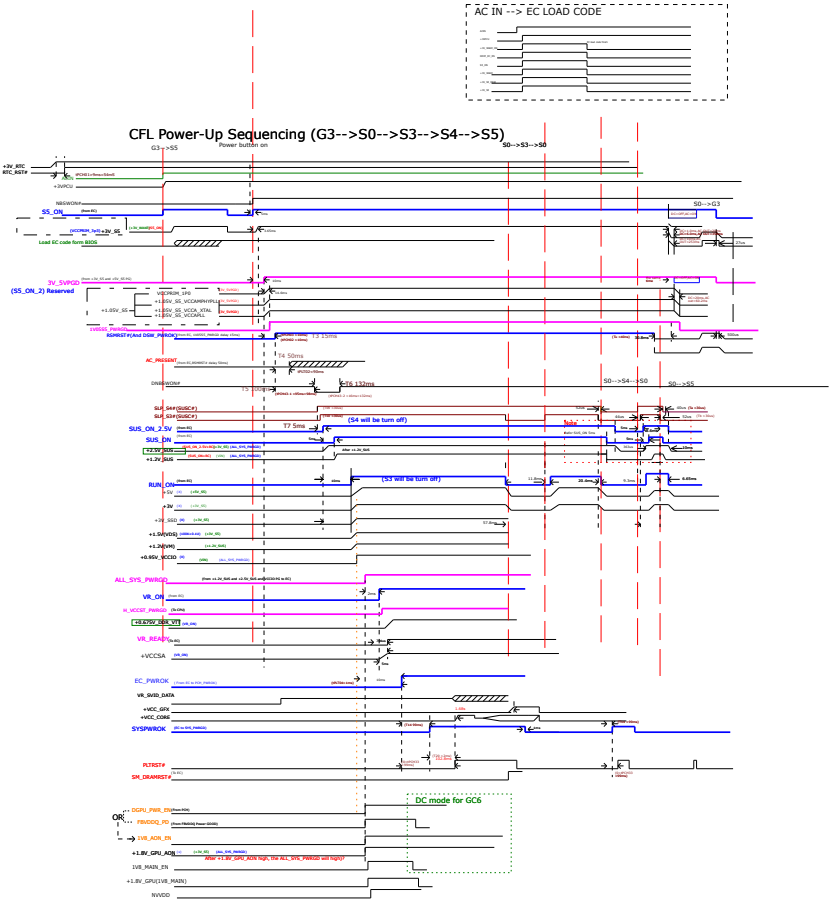


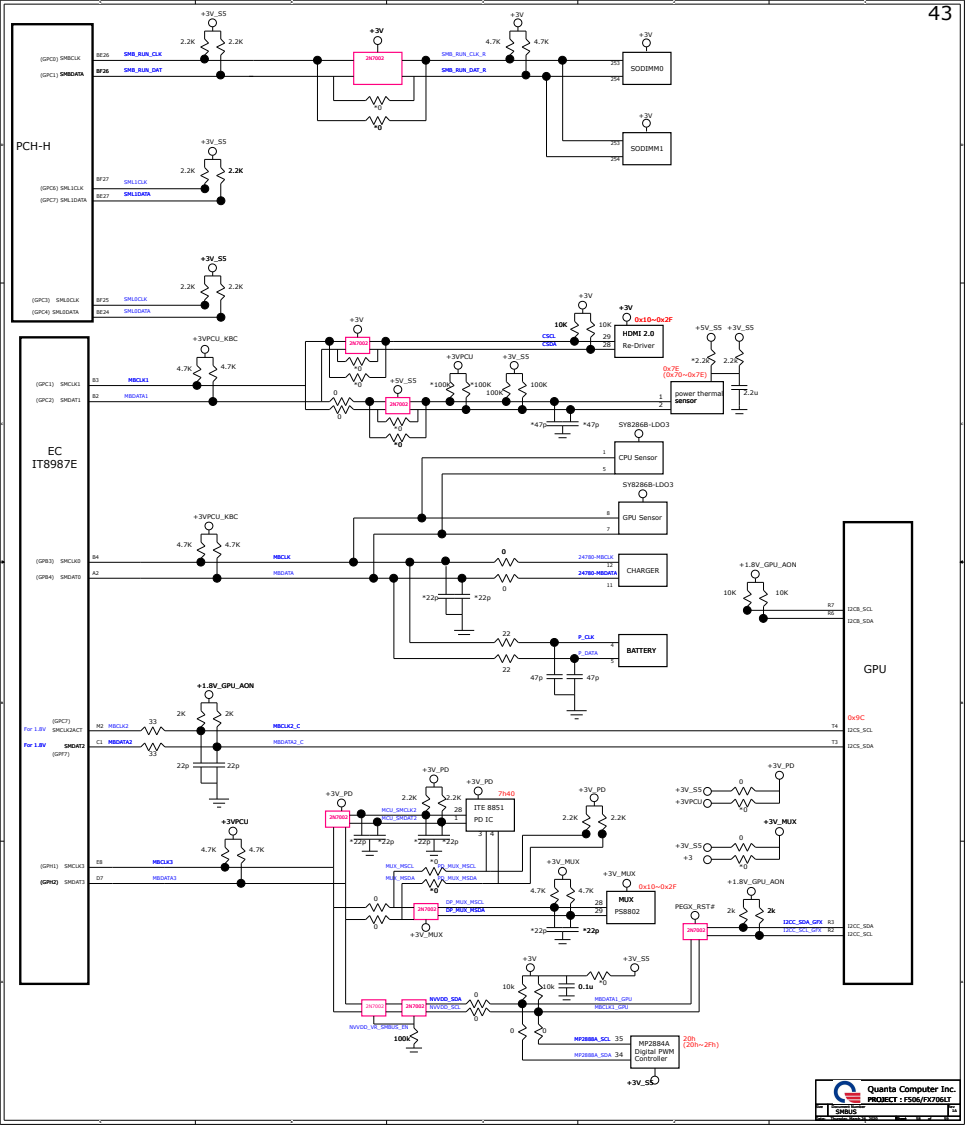
Quanta Computer Inc.	
PROJECT : BKX	
Size	Document Number: VGAMON (OVR-M, US5650PQKI) — Rev 2A
Date: Thursday, March 26, 2020	Sheet 55 of 59





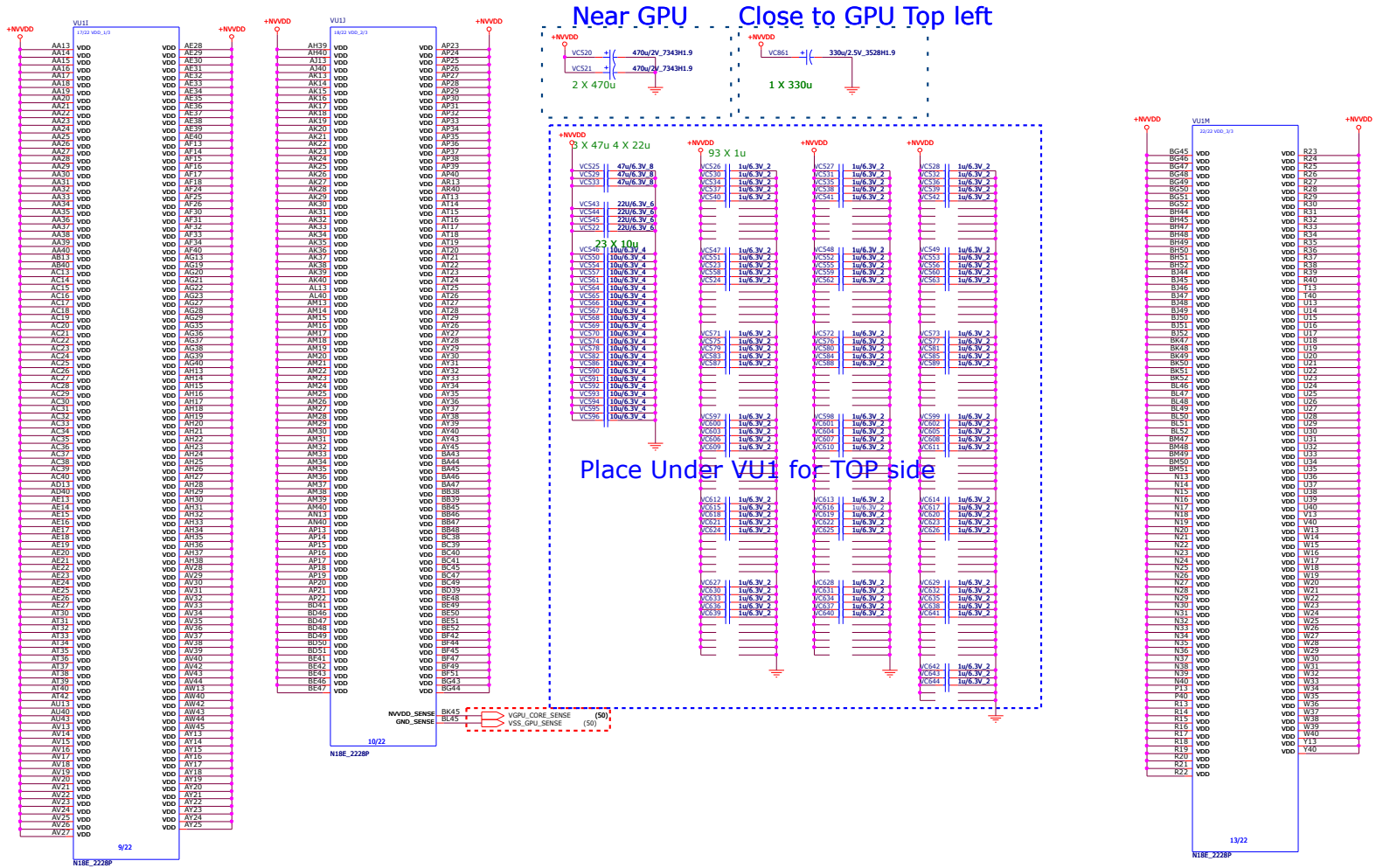
Quanta Computer Inc.		
PROJECT : BKX		
Size	Document Number: VGAMON (OVR-M, US5650PQKI)	Rev: 1A
Date: Thursday, March 26, 2020	Sheet 56 of 59	


AC IN --> EC LOAD CODE
CFL Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)
G3->S5
Power button on
S0-->S3-->S0
S0-->G3
S0-->S4-->S0
S0-->S5
+3V_RTC
RTC_RST#
+3VPCU
NBSWON#
SS_ON
Load EC code form BIOS
3V_SVPGD
(S5_ON_2) Reserved
VCCRCOR_1P0
+1.05V_S0_VCCAMPHYPLL
+1.05V_S0_VCCA_XTAL
+1.05V_S0_VCCAPLL
+1.05V_S0
SYSSSE_PWRGD
BSHRSTP(Add DSW_PWROK)
T3 150ms
T4 50ms
T5 150ms
T6 132ms
AC_PRESENT
DNBSWON#
SUS_S4#(SUSC#)
SUS_S3#(SUSC#)
(S4 will be turn off)
SUS_ON_2.5V
SUS_ON
+2.5V_SUS
+1.2V_SUS
T7 5ms
RUN_ON
(S3 will be turn off)
+5V
+3V
+3V_SSD
+1.5VVDD
+1.2V(VH)
+0.95V_VCCIO
ALL_SYS_PWRGD
VR_ON
H_VCCST_PWRGD
+0.675V_DDR_VTT
VR_READY
+VCCSA
EC_PWROK
VR_SVID_DATA
+VCC_GFX
+VCC_CORE
SYSPWROK
PLTRST#
SM_DRAMRST#
DC mode for GC6
OR
DGPU_PWR_EN
FBVDDQ_EN
1V8_AON_EN
+1.8V_GPU_AON
1V8_MAIN_EN
+1.8V_GPU(1V8_MAIN)
NVVDD


PCH-H
(GPC0) SMBCLK
(GPC1) SMBDATA
BE26 SMB_RUN_CLK
BF26 SMB_RUN_DAT
SMB_RUN_CLK_R
SMB_RUN_DAT_R
SODIMM0
SODIMM1
(GPC6) SML1CLK
(GPC7) SML1DATA
BF27 SML1CLK
BE27 SML1DATA
(GPC3) SML0CLK
(GPC4) SML0DATA
BF25 SML0CLK
BE24 SML0DATA
EC
IT8987E
(GPC1) SMCLK1
(GPC2) SMDAT1
B3 MBCLK1
B2 MBDATA1
HDMI 2.0
Re-Driver
0x10~0x2F
power thermal sensor
0x7E (0x70~0x7E)
SY8286B-LDO3
CPU Sensor
GPU Sensor
(GPB3) SMCLK0
(GPB4) SMDAT0
B4 MBCLK
A2 MBDATA
CHARGER
BATTERY
GPU
I2CB_SCL
I2CB_SDA
(GPC7) SMCLK2ACT
For 1.8V
For 1.8V SMDAT2
(GPF7)
M2 MBCLK2
C1 MBDATA2
MBCLK2_C
MBDATA2_C
0x9C
I2CS_SCL
I2CS_SDA
ITE 8851
PD IC
7h40
(GPH11) SMCLK3
(GPH2) SMDAT3
E8 MBCLK3
D7 MBDATA3
MUX
PS8802
0x10~0x2F
PEGX_RST#
I2CC_SDA_GFX
I2CC_SCL_GFX
I2CC_SDA
I2CC_SCL
NVVDD_SDA
NVVDD_SCL
NVVDD_VR_SMBUS_EN
MP2884A
Digital PWM Controller
20h (20h=2Fh)
MP2884A_SCL 35
MP2884A_SDA 34
MBDATA1_GPU
MBCLK1_GPU
Quanta Computer Inc.
PROJECT : FS06/FX706LT
SMBUS

OS status	S0	S0ix	S3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	C10	S3	S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")	
RUN_ON	H	H	L	L	L	L	L	
+3V	H	H	L	L	L	L	L	
+5V	H	H	L	L	L	L	L	
+0.675V_DDR_VTT	H	H	L	L	L	L	L	
+VCCSA	H	H	L	L	L	L	L	
+VCC_GFX	H	H	L	L	L	L	L	
+VCC_CORE	H	H	L	L	L	L	L	
C10_GATE	H	L	L	L	L	L	L	
+1.05V_VCCSTG	H	L	L	L	L	L	L	
+0.95V_VCCIO	H	L	L	L	L	L		
+1.2V_SUS_C10(VCCPLL_OC)	H	L	L	L	L	L	L	
SUS_ON	H	H	H	L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H	H	L	L	L	L	
+1.05V_SUS	H	H	H	L	L	L	L	
+1.2V_SUS	H	H	H	L	L	L	L	
SUS_ON_2.5V	H	H	H	L	L	L	L	
+2.5V_SUS	H	H	H	L	L	L	L	
S5_ON_2	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	L	L	
+1.8V_S5(From PCH)	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	

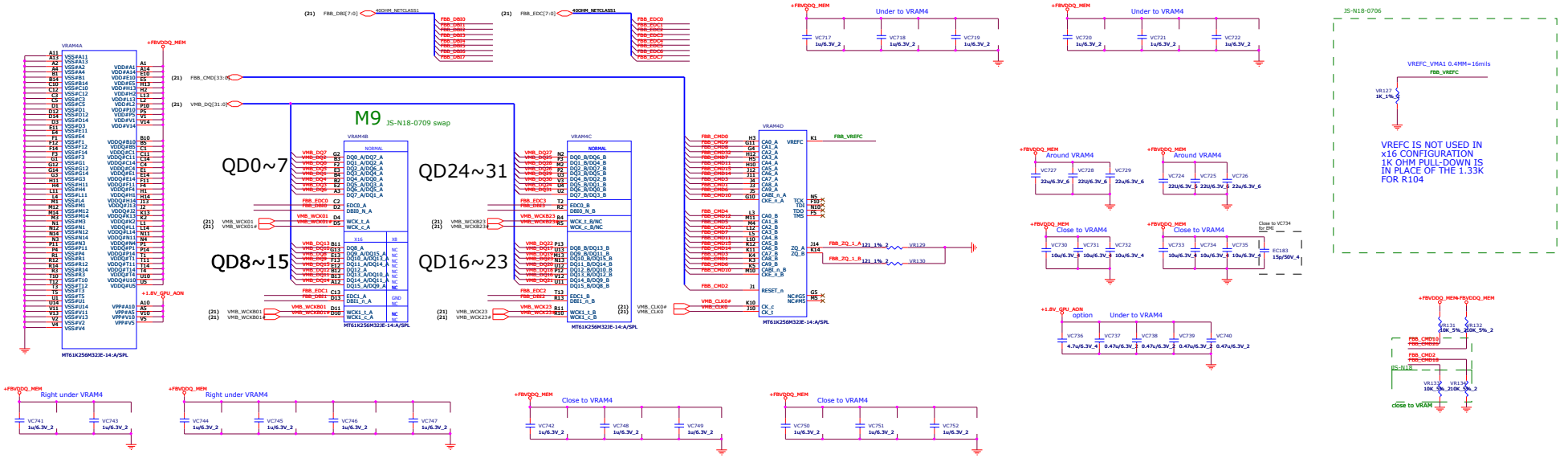
Quanta Computer Inc.			
PROJECT : FX506L/FX706L			
Size	Document Number POWER MAP		Rev 1A
Date: Thursday, March 26, 2020	Sheet 59 of 59		



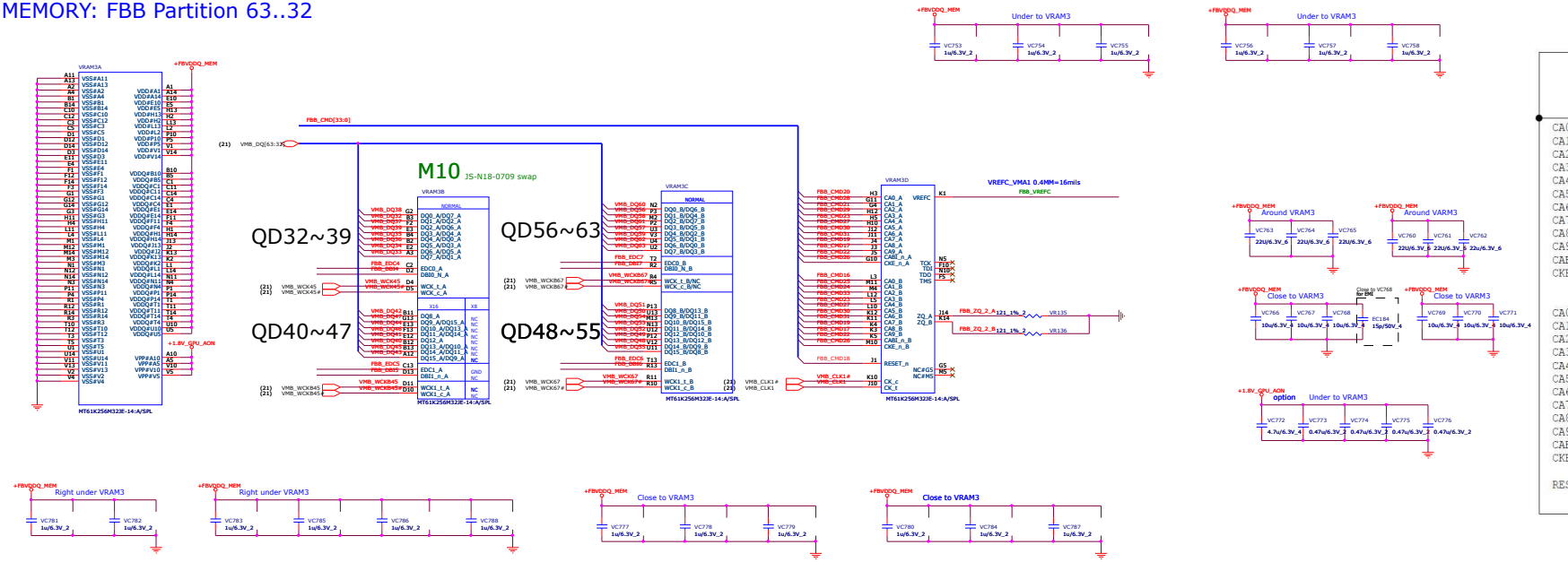
Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	N18E-GX-5/9 (Power)	2A
Date: Thursday, March 26, 2020	Sheet 24 of 59	

MEMORY: FBB Partition 31..0

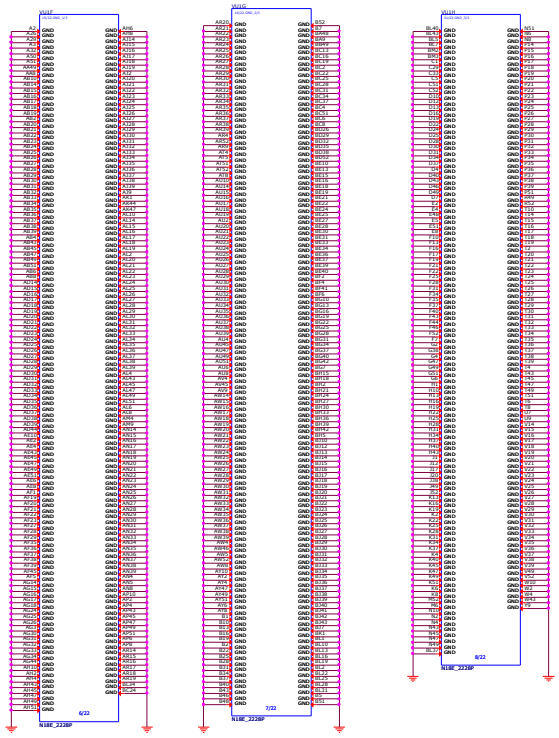


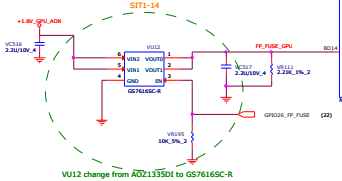
MEMORY: FBB Partition 63..32

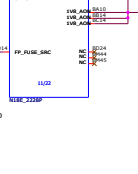


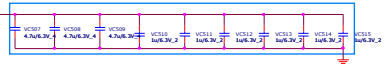
GDDR6 CMD Mapping	Lower 0..31 DRAM1 CHA-Byte 0,1	x16 Mode Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

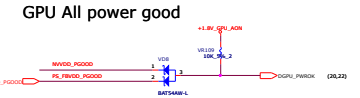
Quanta Computer Inc.
PROJECT : FX506L/FX706L
Size: Document Number: N18E-GX-6/9(GDDR5) Rev: 2A
Date: Thursday, March 26, 2020 Sheet 26 of 39

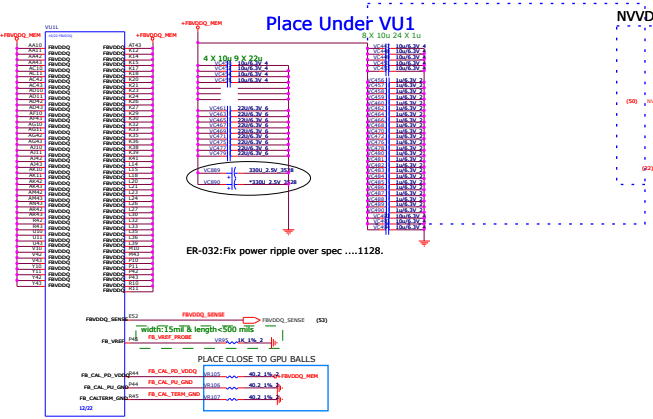


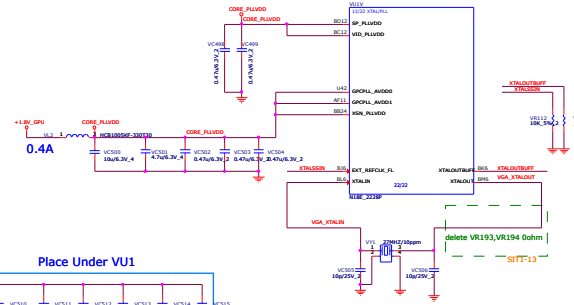


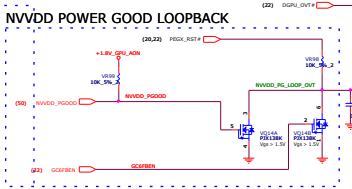


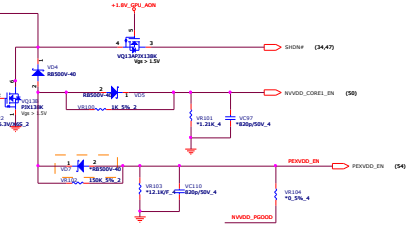




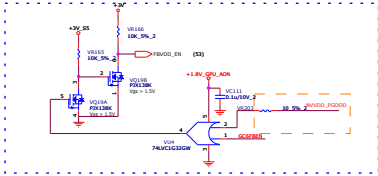








For GC6



	GC6_1V8_MAIN_EN	GC6FBEN	NB_FGC6	1V8_AON	+1.8V_GPU	+NVVDD	+PEX_VDD	FBVDDQ
POWER ON	1	0	0	ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FGC6	0	1	1	ON	ON	OFF	ON	ON

For Power off sequence