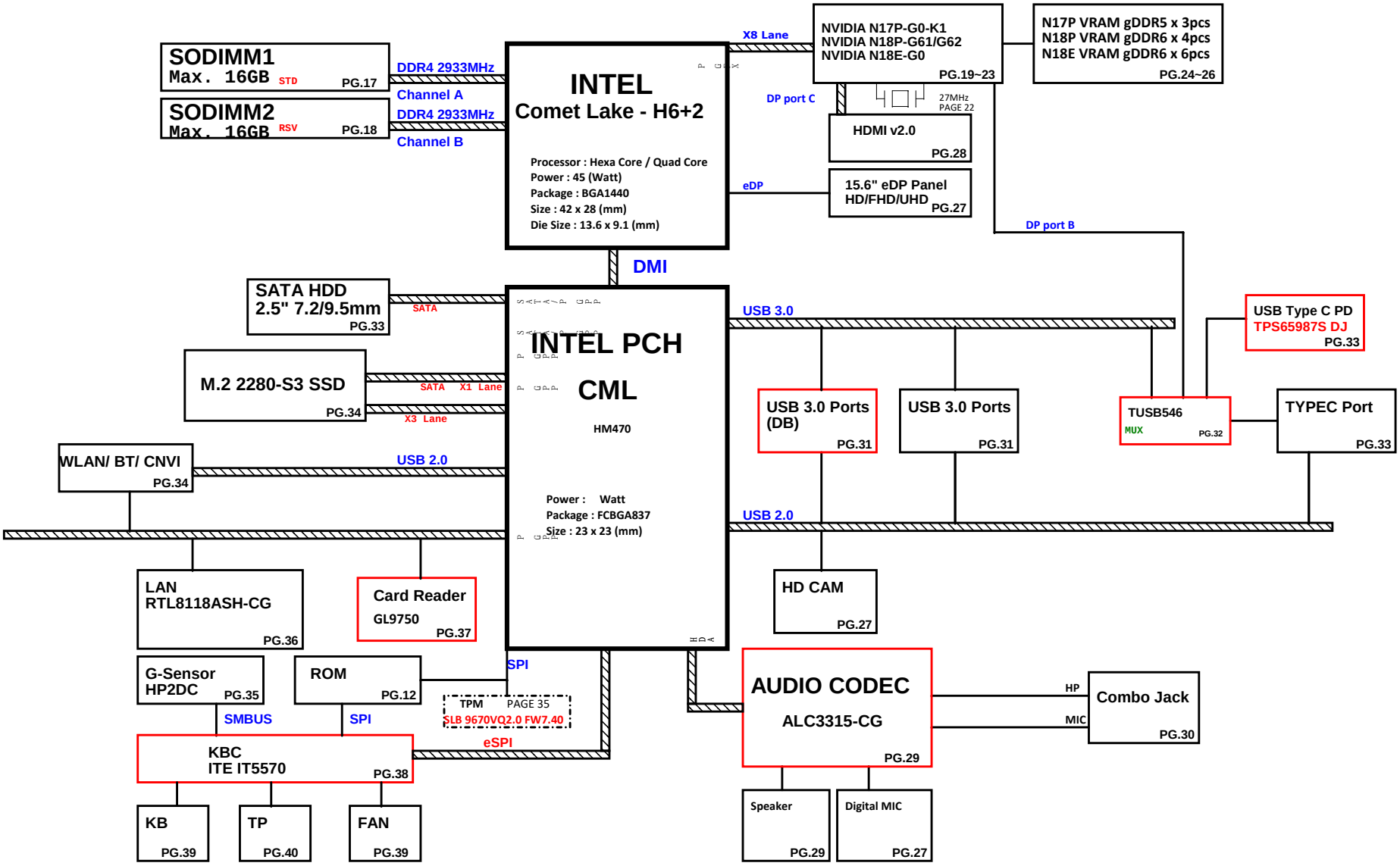
Comet Lake System Block Diagram

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



PROJECT :G3JB
Quanta Computer Inc.
NB5
Size C | Document Number Block Diagram | Rev 1A
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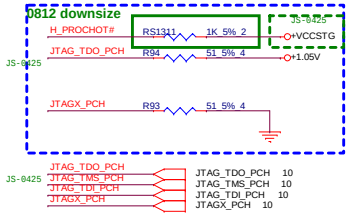
CFL-H Processor (CLK,MISC,JTAG)

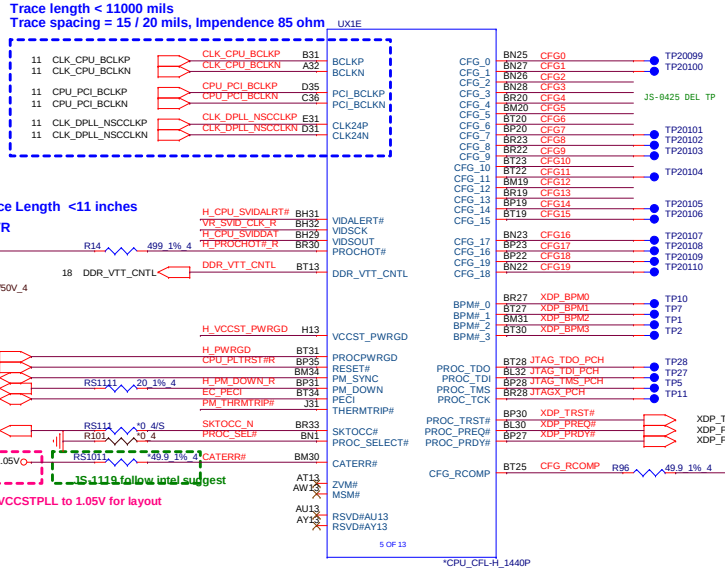
02

Processor pull-up (CPU) 0808 Follow G3EA del Reserve PD res

0812 downsize



Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm



Layout Notes:
PROCHOT# (50ohm) Trace Length <11 inches
Ca need placment near VR

Layout Notes:
H_PWRGD (50ohm) Trace Length: 1~11 inches
CPU_PLTRST# (50ohm) Trace Length: 10~17 inches
PM_SYNC (50ohm) Trace Length: 1~11.25 inches

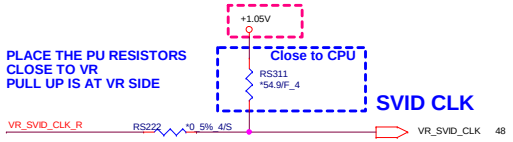
0709 Change from VCCSTPLL to 1.05V for layout

CPU CORE SVID

Layout Notes:
1.Need routing together
2.ALERT need between CLK and DATA.

0627 Change from VCCSTPLL to 1.05V for layout

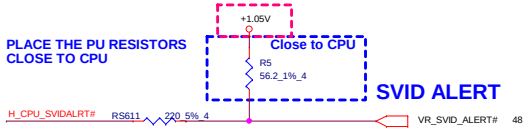
PLACE THE PU RESISTORS CLOSE TO VR PULL UP IS AT VR SIDE



SVID CLK

0627 Change from VCCSTPLL to 1.05V for layout

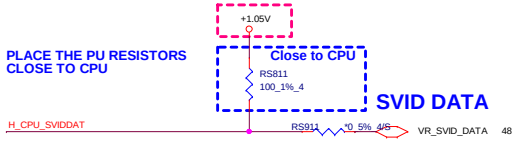
PLACE THE PU RESISTORS CLOSE TO CPU



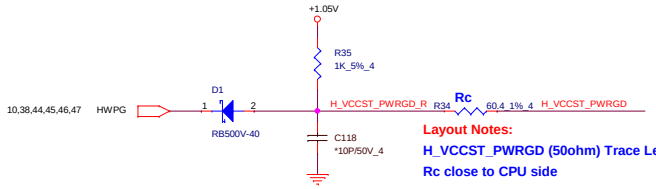
SVID ALERT

0627 Change from VCCSTPLL to 1.05V for layout

PLACE THE PU RESISTORS CLOSE TO CPU

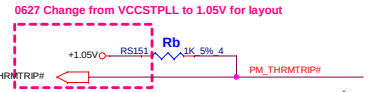


SVID DATA

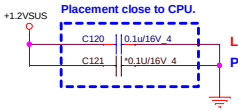


Layout Notes:
H_VCCST_PWRGD (50ohm) Trace Length: 0.3" - 1.5"
Rc close to CPU side

0627 Change from VCCSTPLL to 1.05V for layout



Layout Notes:
THERMTRIP# (50ohm) Trace Length: 1.1~12 inches
Rb need placment near PCH



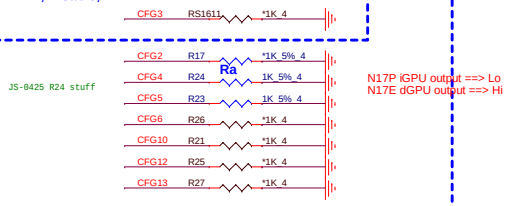
Layout Notes:
Please keep VDDQ plane is enough for 2.8A

	CFG[4]	Ra
EDP Output from DGPU	Hi	Non Stuff
EDP Output from iGPU	Low	Stuff

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;



N17P iGPU output ==> Lo
N17E dGPU output ==> Hi

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	**x1 = Normal operation** x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled **x0 = Enabled**	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved **x10 = 2 x8 PCI Express** x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	**x1 = PEG train follow RESETB de-asseted** x0 = PEG wait for BIOS fro training	

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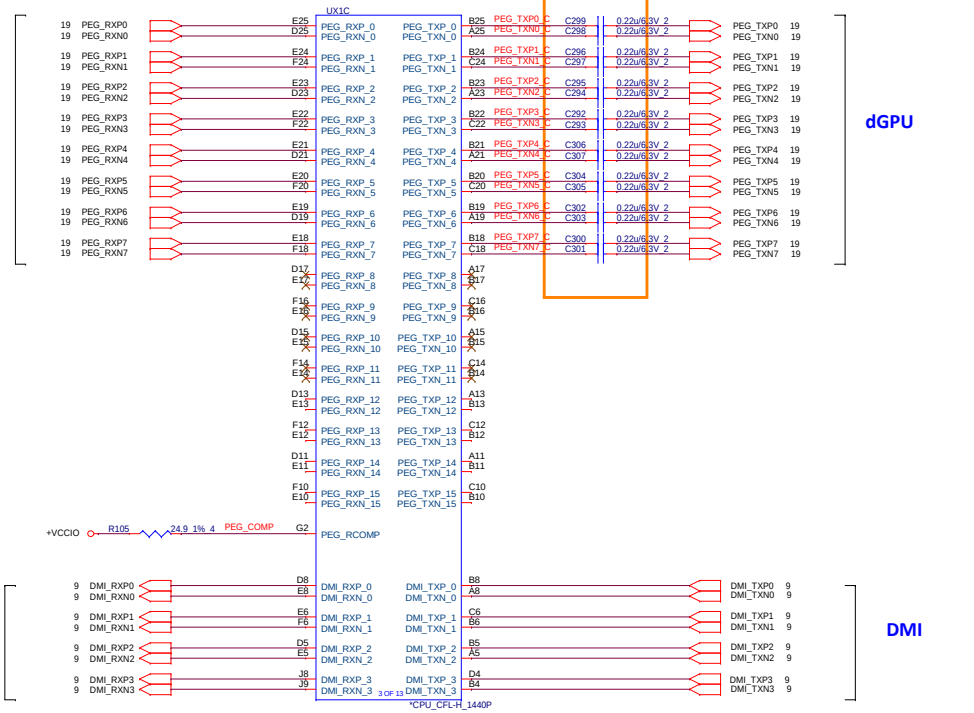
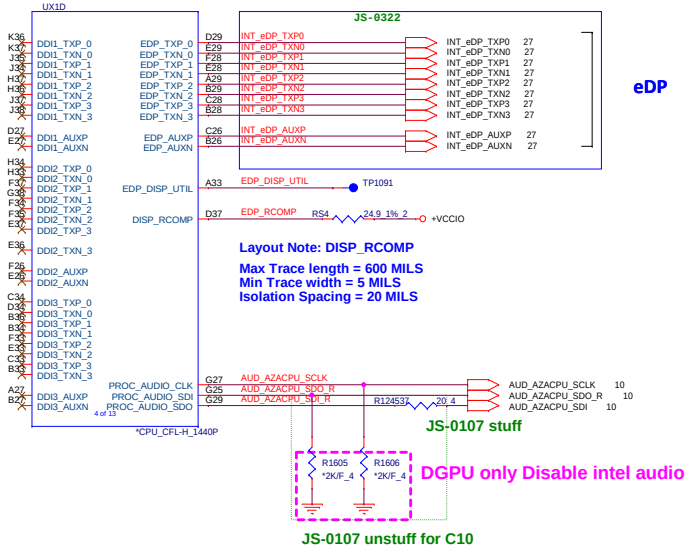
CFL-H Processor (DMI,PEG,FDI)

0822 follow starmade downsize



Layout Note: PEG_RCOMP

Max Trace length = 600 MILS
Min Trace width = 5 MILS
Trace spacing to others = 15 MILS



Layout Note: DISP_RCOMP

Max Trace length = 600 MILS
Min Trace width = 5 MILS
Isolation Spacing = 20 MILS

JS-0107 stuff

R1605 *2K/F_4
R1606 *2K/F_4

DGPU only Disable intel audio

JS-0107 unstuff for C10

https://realschematic.com

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	Quanta Computer Inc.
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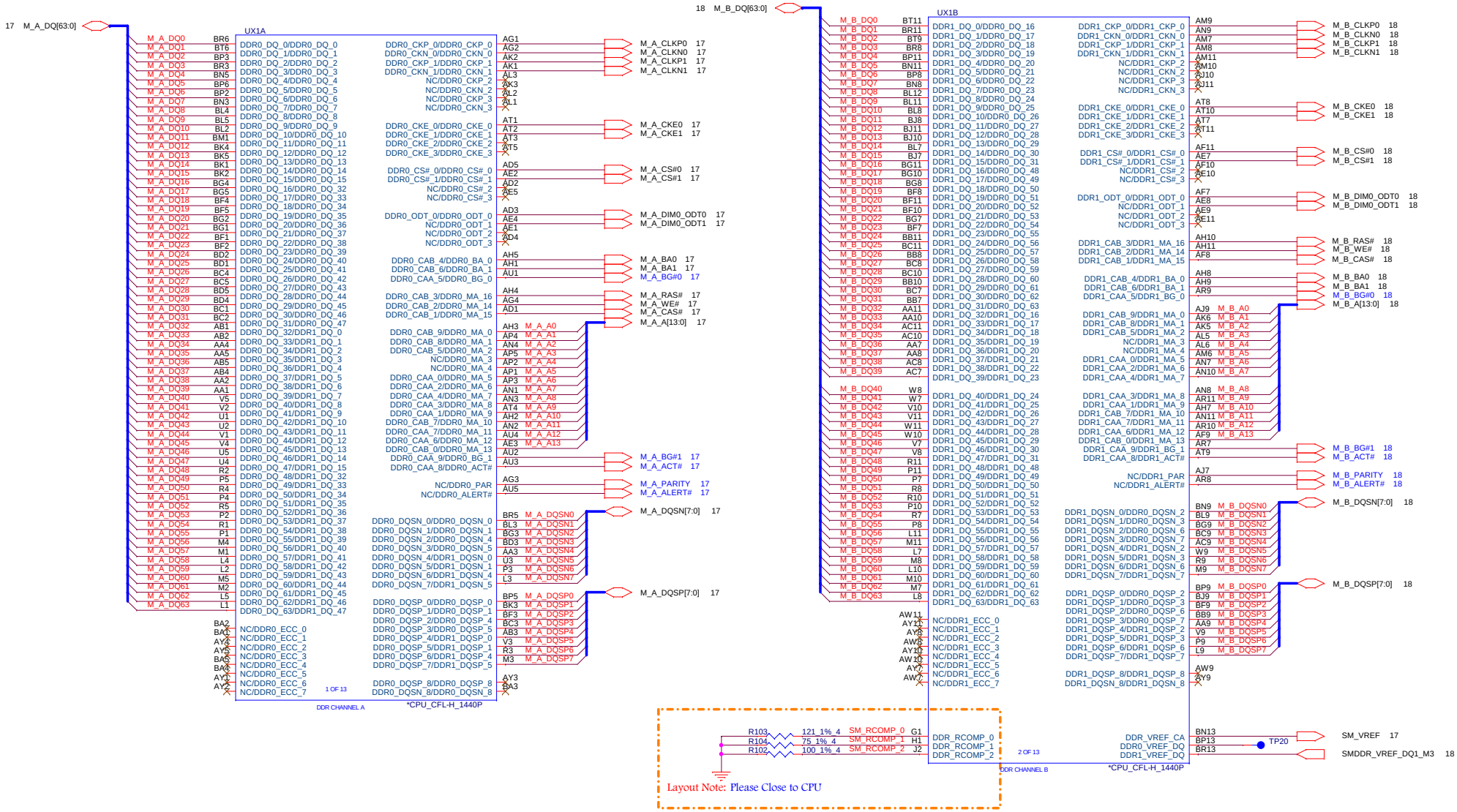
CFL-H Processor (DDR4)



NB5	PROJECT :G3JB Quanta Computer Inc.	
Size: Custom	Document Number: CFL-H 3/7 (DDR4 I/F)	Rev: 1A
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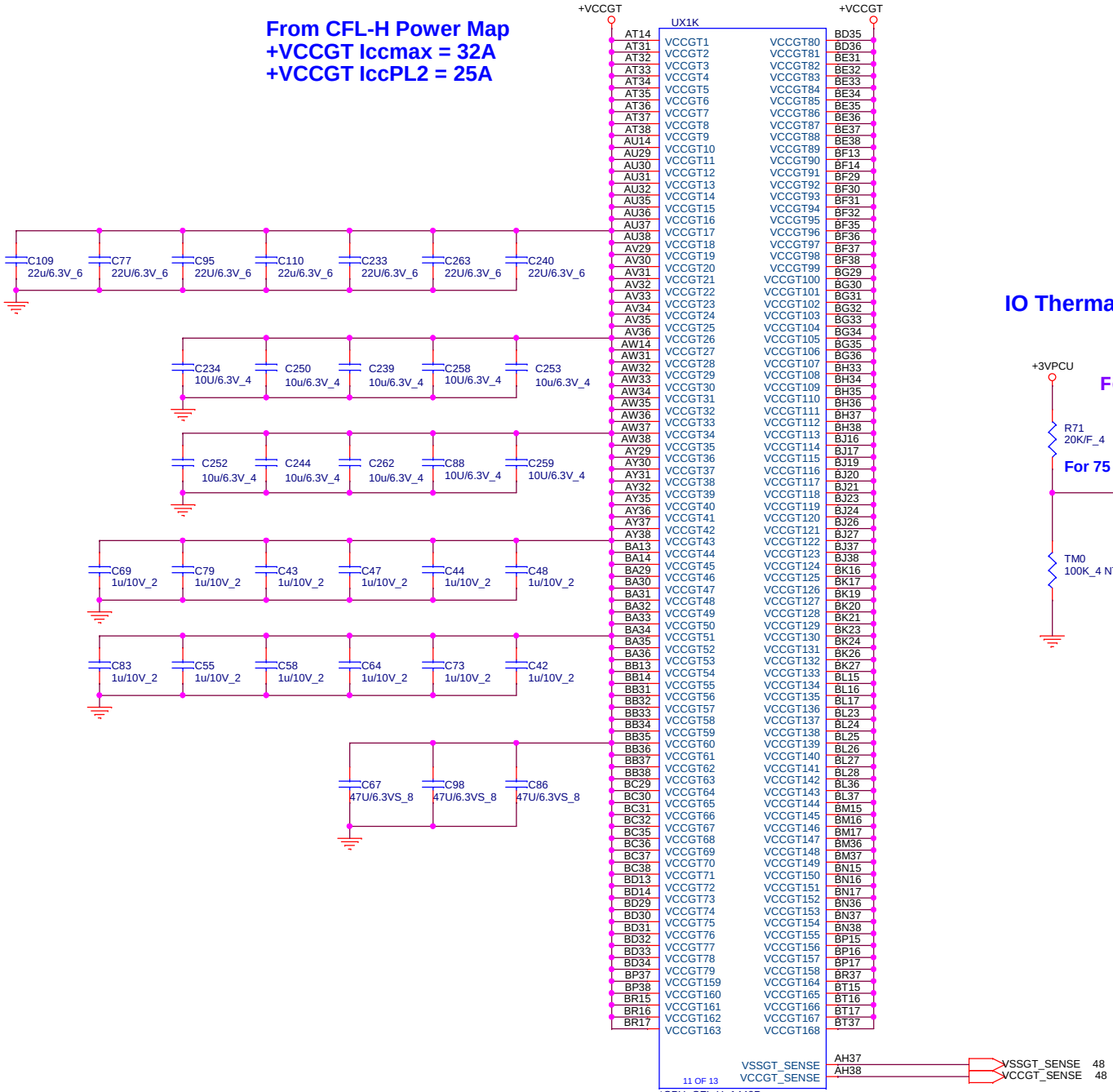
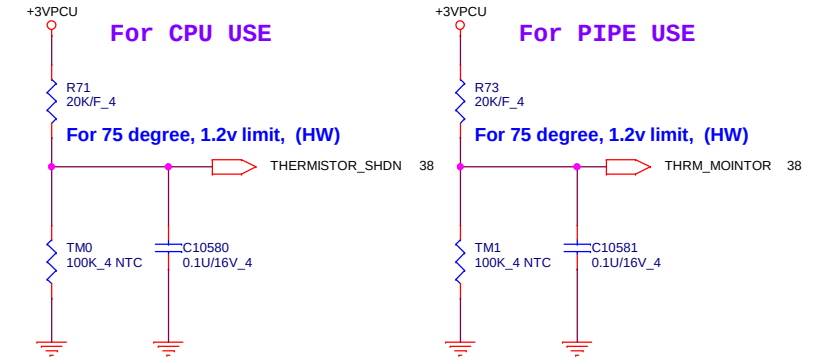
Coffee Lake Processor (POWER)

05

From CFL-H Power Map
+VCCGT Iccmax = 32A
+VCCGT IccPL2 = 25A



IO Thermal Protect



NB5	PROJECT :G3JB Quanta Computer Inc.	
Size: B	Document Number: CFL-H 4/7 (POWER)	Rev: 1A
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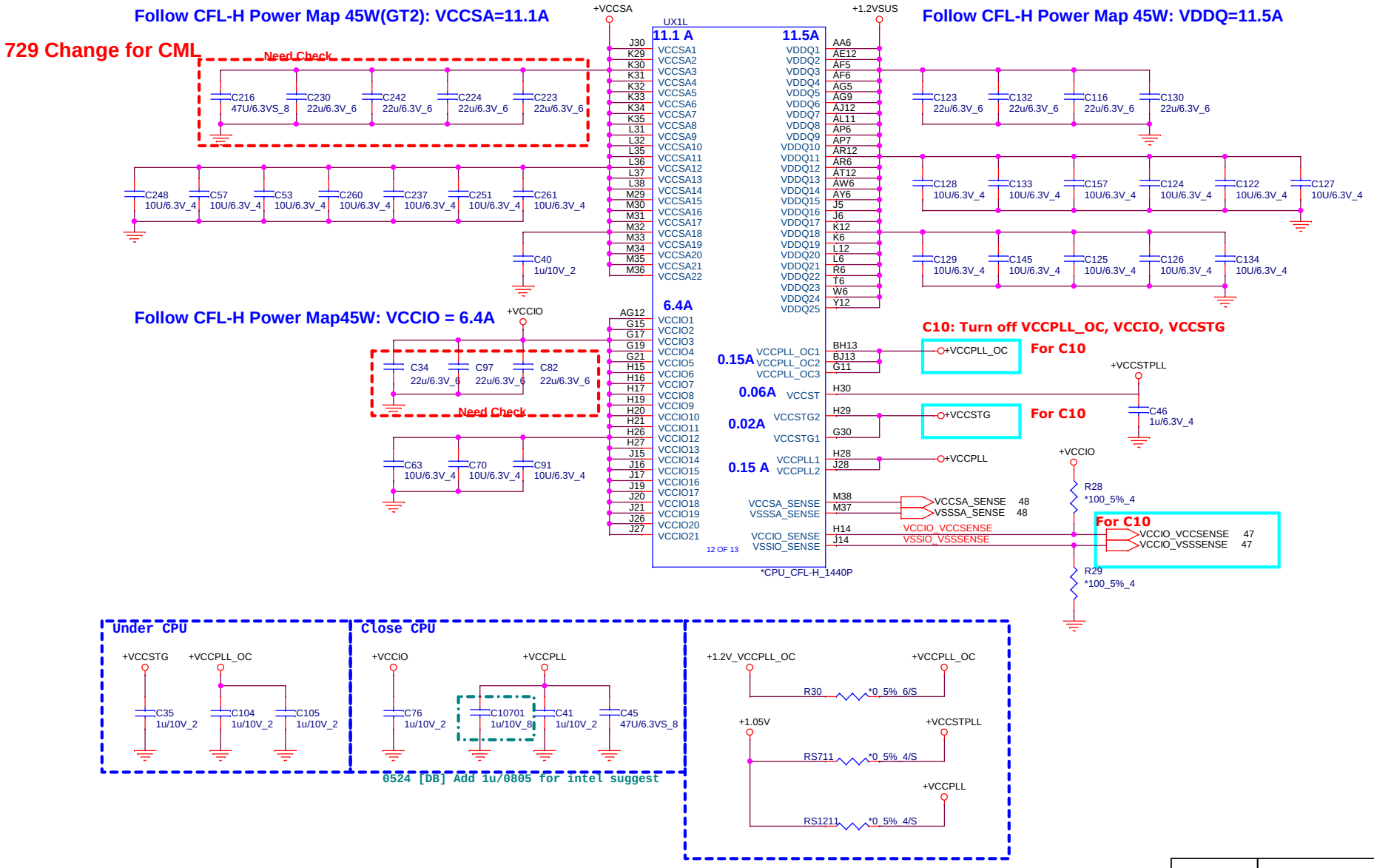

NB5	PROJECT :G3JB Quanta Computer Inc.	
Size: B	Document Number: CFL-H 5/7 (POWER&GND)	Rev: 1A
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Follow CFL-H Power Map 6 + 2 45W 80A

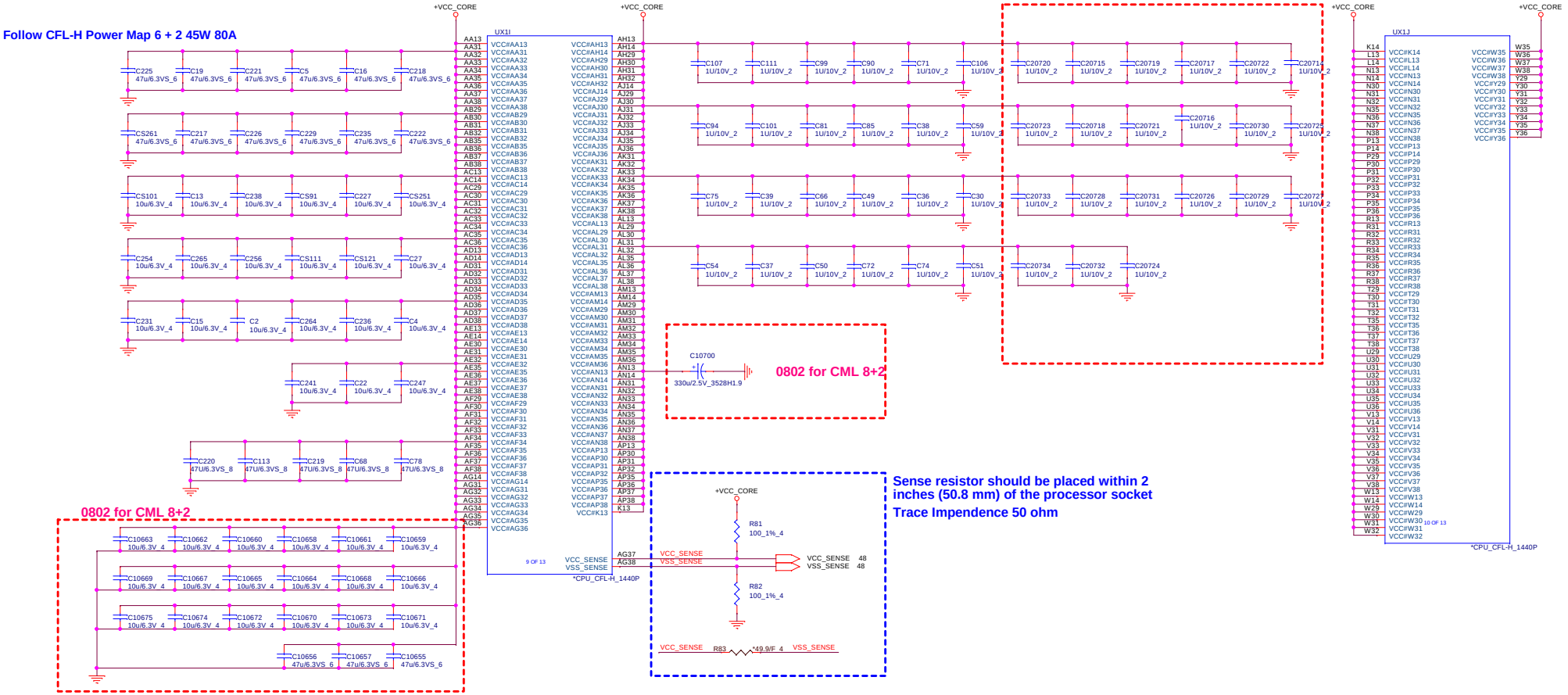
0729 Add & Change for CML H 8+2

0802 for CML 8+2

0802 for CML 8+2

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm



NB5	PROJECT :G3JB Quanta Computer Inc.	
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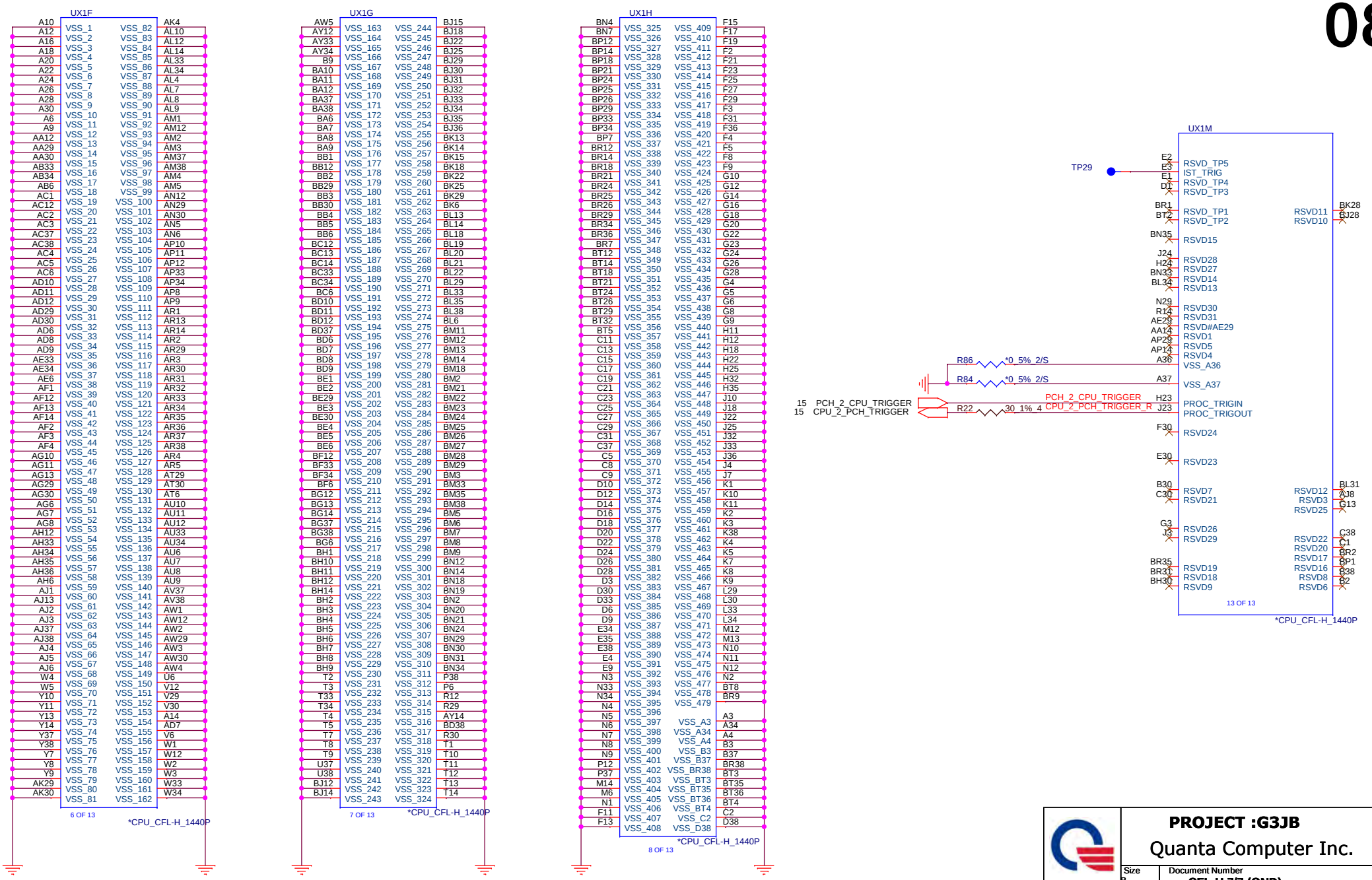
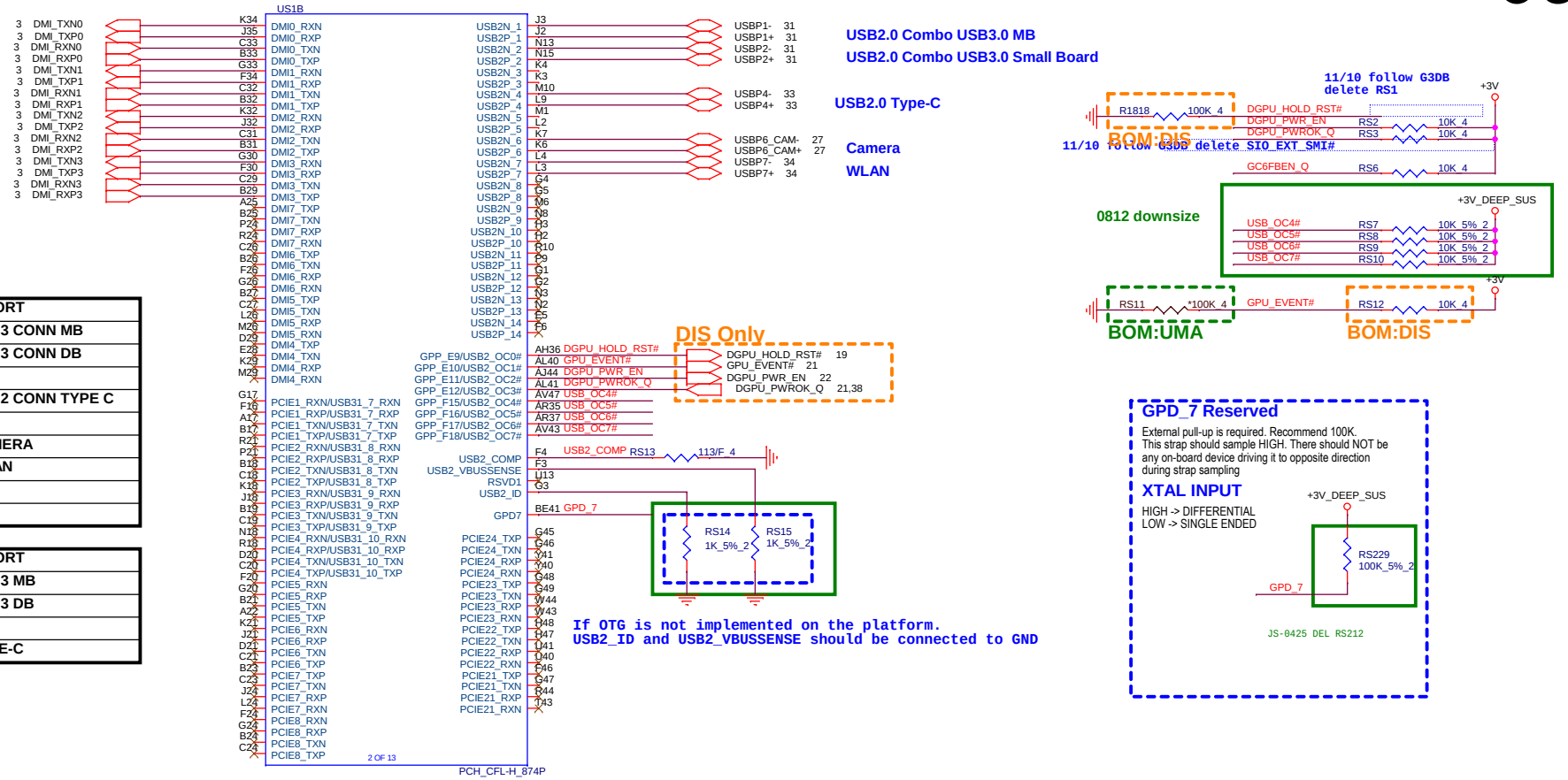
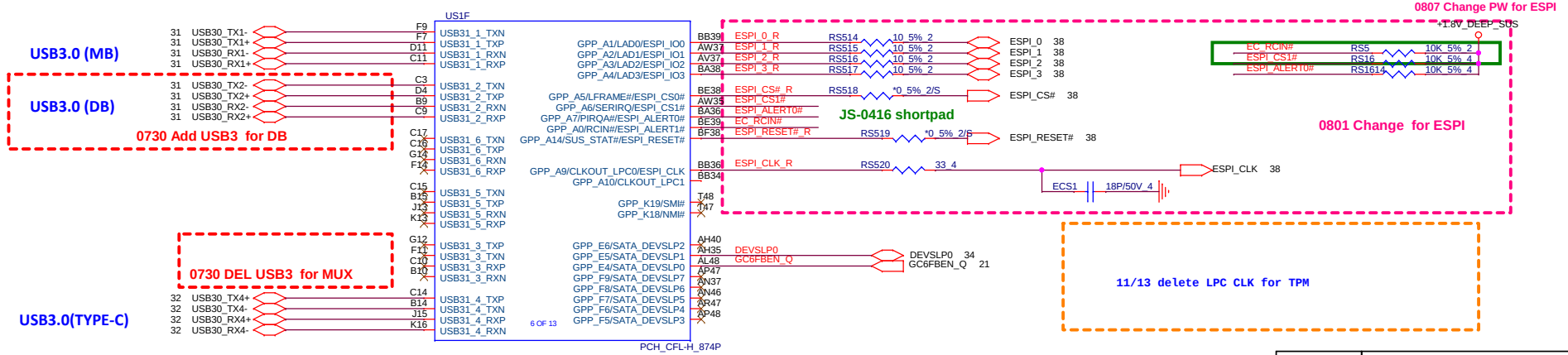


USB 2.0 PORT	
PORT1	USB3 CONN MB
PORT2	USB3 CONN DB
PORT3	NC
PORT4	USB2 CONN TYPE C
PORT5	NC
PORT6	CAMERA
PORT7	WLAN
PORT8	NC
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	NC
PORT4	TYPE-C





PROJECT :G3JB

Quanta Computer Inc.

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Custom	PCH 1/7 (DMI/USB/PCIE)	1A

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HDA Bus

ME Lock Function

For EMI

0731 Change for ESPI

JS-0107 stuff for C10

JS-0918 del colay

0801 Change for ESPI

0812 downsize

0801 follow G3EA PU 3vS5

0808 follow G3EA del Reserve sch

11/15 confirm with EC, then follow G37L,

Touch Pad DDR4

System PWROK

For DS3 Sequence

For DS3 -->Ra
Non-DS3 -->Rb

JS-0416 shortpad

0731 DEL

RTC Circuitry(RTC)

JS-0416 shortpad

RTC Power trace width 20mils.

JS-0502

JS-0109 FOR ICT

For HWPG Sequence

For Power Sequence.

0731 DEL

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NB5	
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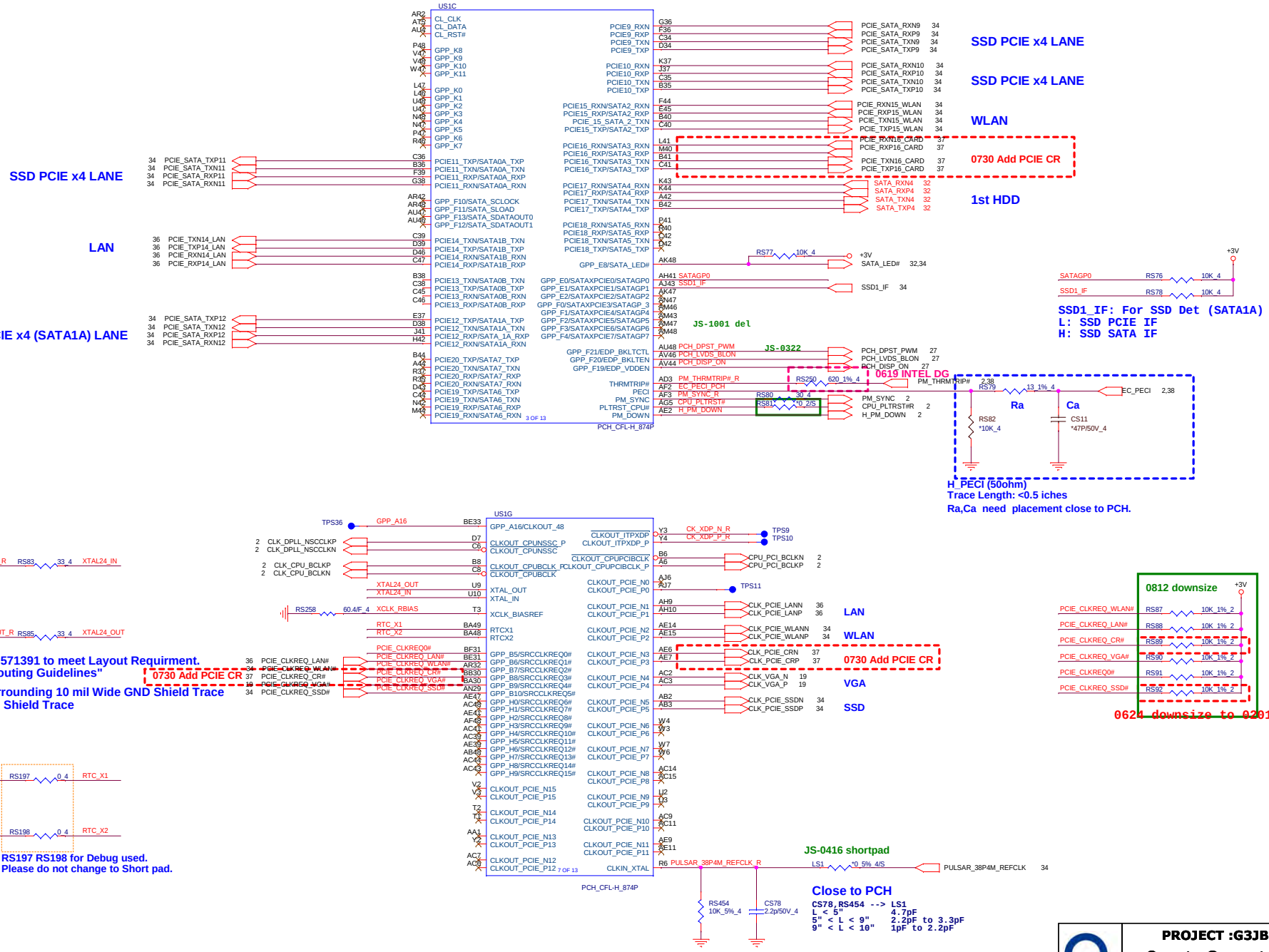
PCIE PORT	
PCIE1-8	NC
PCIE9	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	SSD (SATA 1a)
PCIE13	NC
PCIE14	LAN
PCIE15	WLAN
PCIE16	card reader
PCIE17	1st HDD (SATA 4)
PCIE18-24	NC



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Quanta Computer Inc.	
Size	Custom
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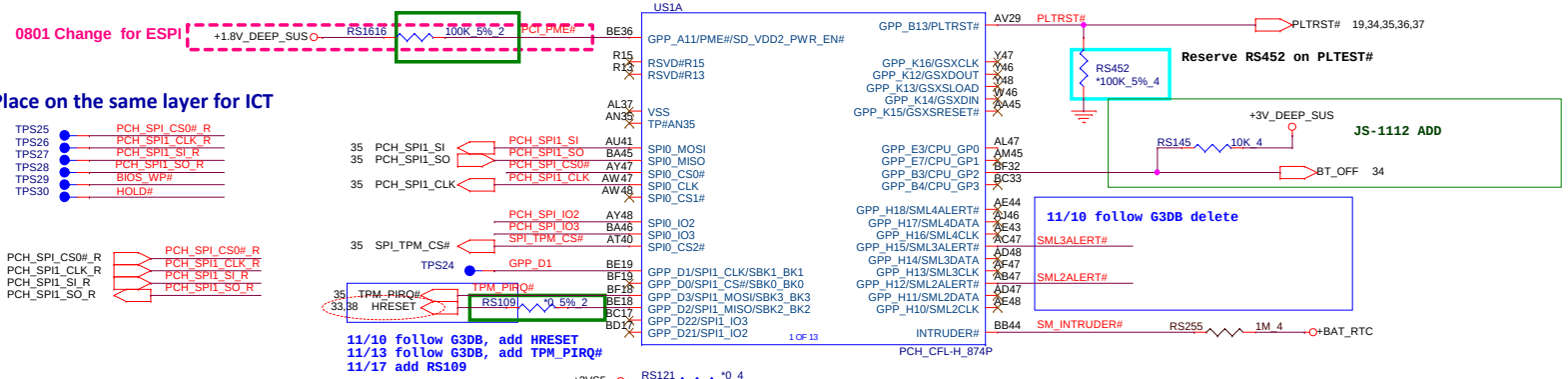
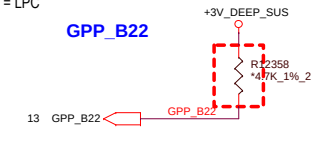


Vender	Size	P/N
MAX	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSIQ)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DFHS08FS023 or DG008000011

DB DG008000012 WSON8 SOCKET
AKE2DF00Q00 WSON8

BOOT SELECT STRAP

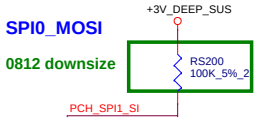
This Signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6).
0 = SPI (Default)
1 = LPC



0624 downsize to 0201

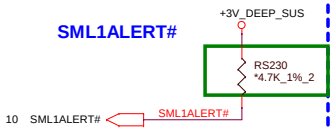
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



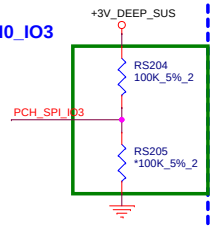
IntelR DCI-OOB

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB



RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

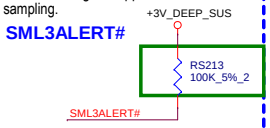


ESPI/LPC SELECT STRAP

This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

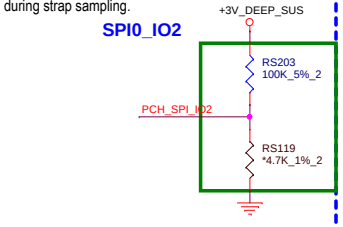
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



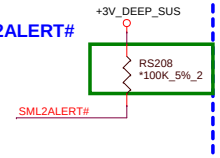
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



ESPI FLASH SHARING MODE

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.



0812 downsize

Pin Straps (Sheet 2 of 4)

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning:** **If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

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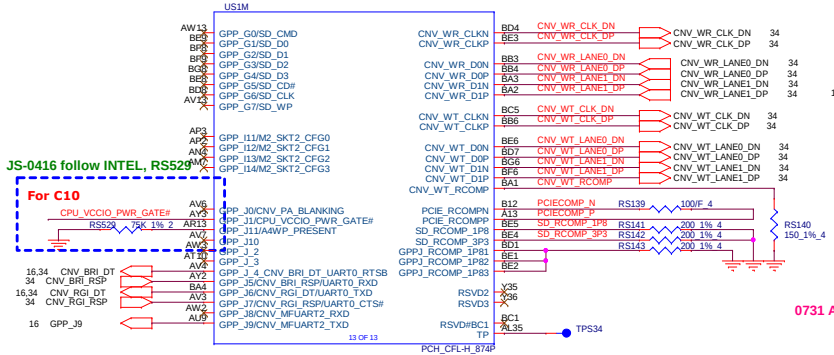
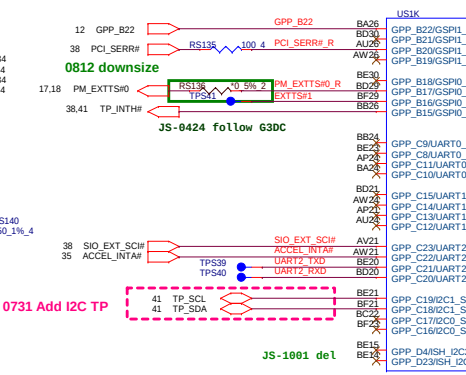
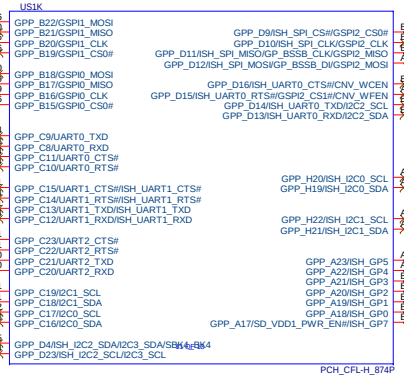
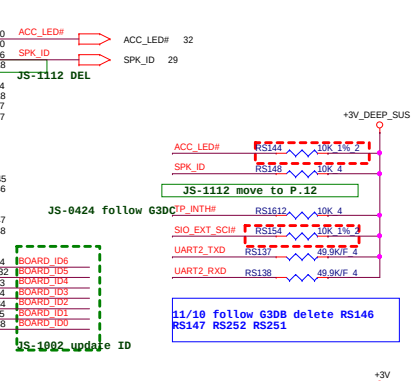
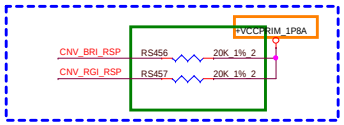




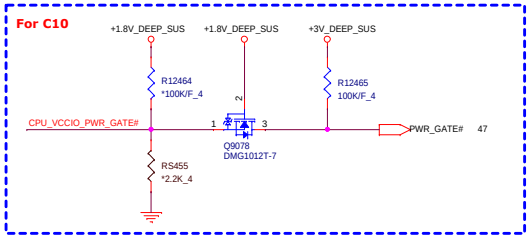




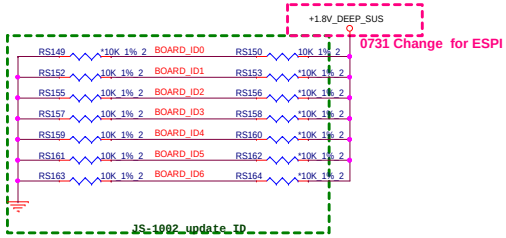


For Touch Panel

11/10 delete

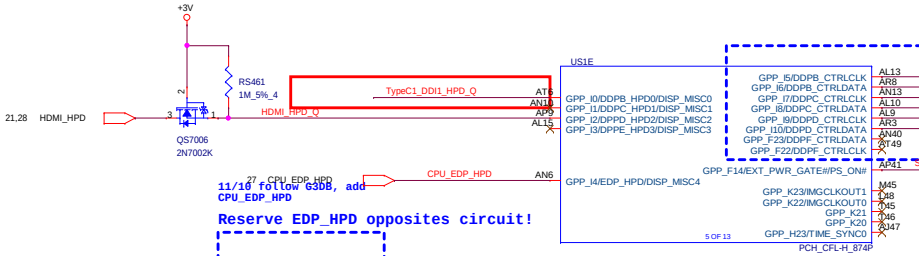


CFL-H/N17P-G0
CFL-H/N18P-G61/G62
CFL-H/N18E-G0

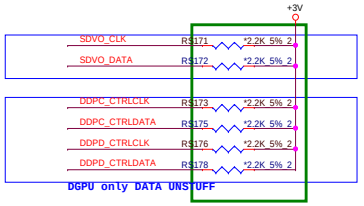


Board ID

Model	Board ID [6:5] ID6;ID5	Board ID [4] ID4	Board ID [3] ID3	Board ID [2:1:0] ID2;ID1;ID0	
Definition	00 : Reserve	0: Reserve	0: Reserve JS-0225 update	100 : N18E-G0-gDDR6-G3JC 101 : N18E-G1-65 110 : Reserve 111 : Reserve JS-0225 update	000 : N18P-G61-gDDR6-G3JB Default 001 : N18P-G62-gDDR6-G3JB 010 : Reserve 011 : N17P-G0-gDDR5-G3JA



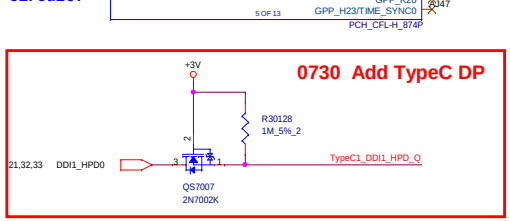
12/11 add SDVO_CLK & SDVO_DATA
12/12 add DDPC_CTRLCLK & DDPC_CTRLDATA
add DDPD_CTRLCLK & DDPD_CTRLDATA



GPP_I6 / DDPB_CTRLDATA:
For eDP used, need add in Muxless and UMA System.
This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_I8 / DDPC_CTRLDATA:
This signal has a weak internal Pull-down.
0 = Port C is not detected. (Default)
1 = Port C is detected.

GPP_I10 /DDPD_CTRLDATA:
For eDP used, need add in Muxless and UMA System.
This signal has a weak internal pull-down.
0 = Port D is not detected. (Default)
1 = Port D is detected.



NB5	PROJECT :G3JB Quanta Computer Inc.	
Size: C	Document Number: PCH 5/7 (GPIO)	Rev: 1A
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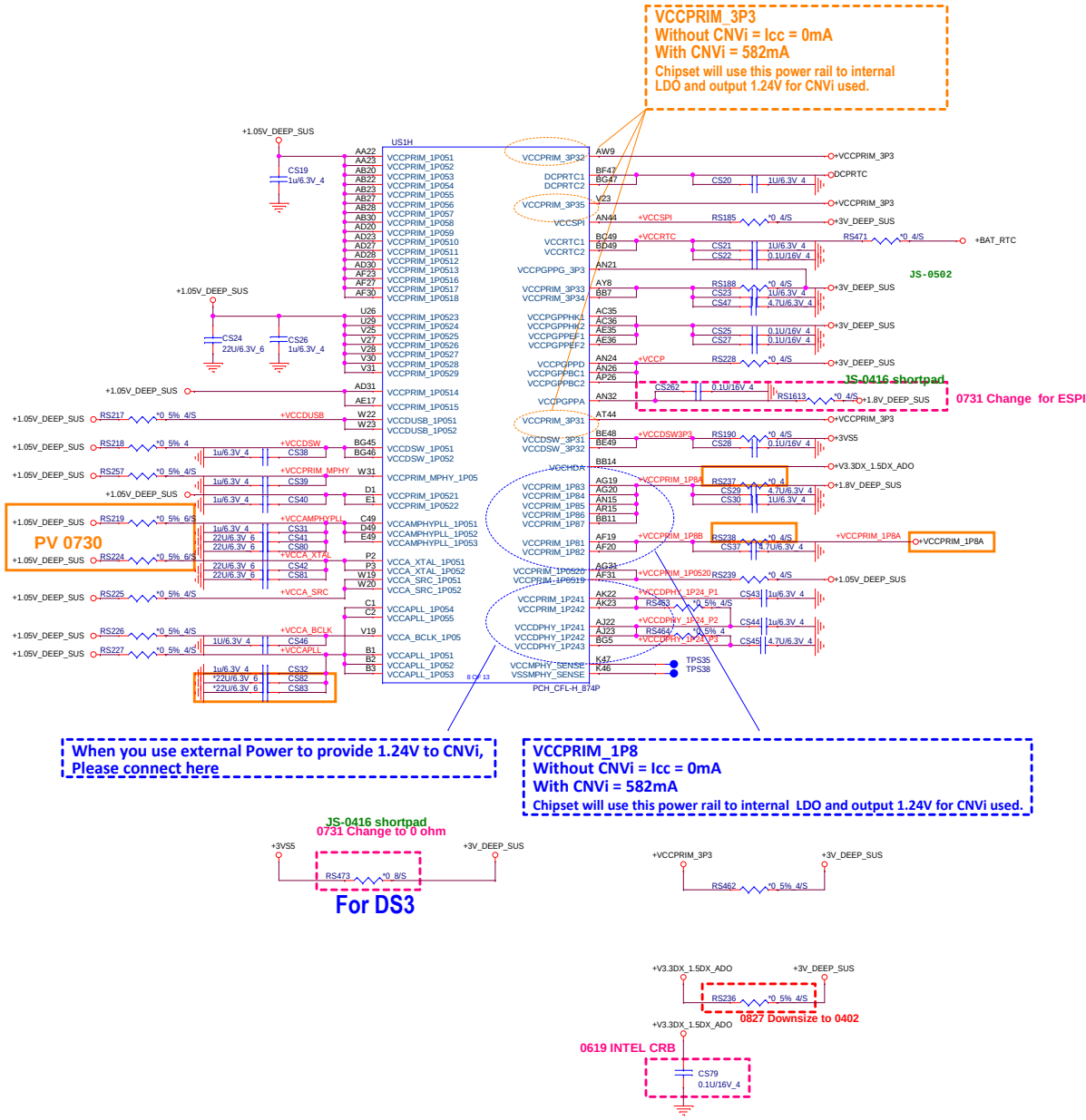
Please follow below table to check Layout

PCH-H Estimated I_{cc}[3] with Integrated 1.8V VRM Mode OFF (H Mobile SKUs)

Voltage Rail	Voltage (V)	S0 Iccmax Current[2] (A)	Sx Icc Idle Current[4] (mA)	S0ix Icccmax Current (mA)	Deep Sx Icc Idle Current (mA)	G3 (µA)
VCCAPLL_1P05	1.05	0.034	0.2	0.801	0	0
VCCA_BCLK_1P05	1.05	0.007	0.1	0.087	0	0
VCCA_SRC_1P05	1.05	0.141	0.3	0.838	0	0
VCCA_XTAL_1P05	1.05	0.005	0.544	0.195	0	0
VCCAMPHYPLL_1P05	1.05	0.114	0.4	1.192	0	0
VCCPRIM_1P05	1.05	4.174 HSIO Lane Adder refer to Table 10-7 column HALO	40.344	0.477A	0	0
VCCPRIM_MPHY_1P05	1.05	0.088	0.2	1.22	0	0
VCCDSW_1P05	1.05	0.01	0.2	0.001	0.2	0
VCCDUSB_1P05	1.05	0.33	1.288	16.373	0	0
VCCHDA	3.3	0.007	0.1	4.908	0	0
VCCDSW_3P3	3.3	0.094	0.2	0.705	1.05	0
VCCPRIM_3P3	3.3	0.318	0.3	0.916	0	0
VCCPGPPA	3.3	0.085	0.1	0.103	0	0
VCCPGPPBC	3.3	0.286	0.2	0.232	0	0
VCCPGPPD	3.3	0.117	0.1	0.109	0	0
VCCPGPPEF	3.3	0.145	0.2	0.094	0	0
VCCPGPPG_3P3	3.3	0.121	0.1	0.072	0	0
VCCPGPPHK	3.3	0.219	0.2	0.138	0	0
VCCPRIM_1P8	1.8	0.152 CNVi Adder refer to Table 10-8, column HALO	6.607	9.411	0	0
VCCRTC[1]	3.0	0.31mA	0.299	0.075	0.316	6
VCCSPI	3.3	0.042	0.1	0.153	0	0

Notes:
1. The VCC rail ICC data is taken at 3.0V while the system is in a mechanical off (G3) state at room temperature.
2. Iccmax estimates assumes 110 °C.
3. The Iccmax value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).
4. Sx Icc Idle assumes PCH is idle and ME is power gated.
5. Sx Icc at 3.3V level is assumed. Sx Icc data at the 1.8 V and/or 1.5V level not measured.



NB5	PROJECT :G3JB
	Quanta Computer Inc.
Size C	Document Number PCH 6/7 (POWER) Rev 1A
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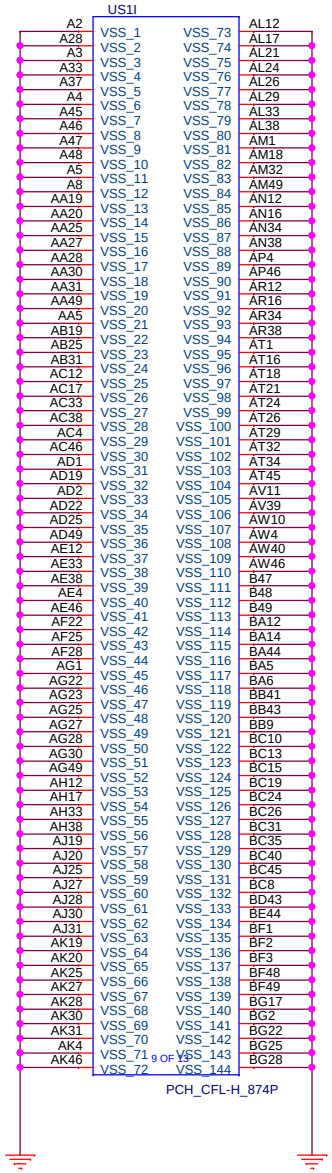

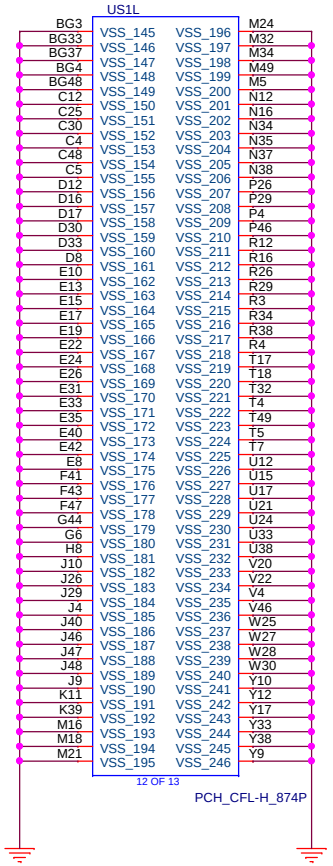

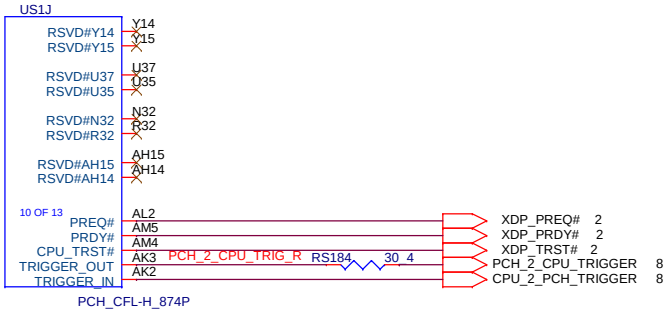

NB5

PROJECT :G3JB

Quanta Computer Inc.

Size	Document Number	Rev
B	PCH 7/7 (GND)	1A

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Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Pin Straps (Sheet 3 of 4)

Signal	Usage	When Sampled	Comment
SPI0_IO3 Page12	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT# Page12	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_CTRLDATA Page13	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA Page13	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA Page13	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23 NA	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

TOP SWAP OVERRIDE STRAP

The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address

0624 downsize to 0201

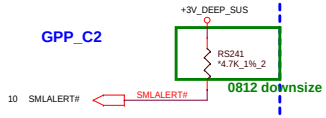
NO REBOOT IF SAMPLED HIGH

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

11/10 follow G3D delete

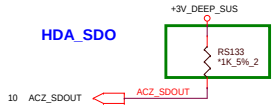
TLS CONFIDENTIALITY ENABLED

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.



0812 downsize

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.

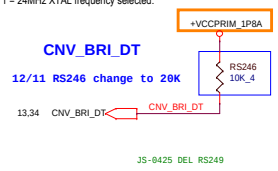


Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7 Page9	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

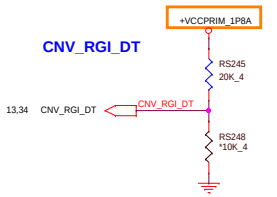
XTAL Frequency Select

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.



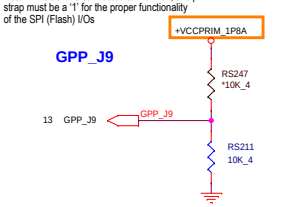
M.2 CNVi Mode Select ???

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



GPP_J9 1.8V VCCPSPI:

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os



NB5	PROJECT :G3JB Quanta Computer Inc.	
	Size: — Document Number: Strap Pins	Rev: 1A
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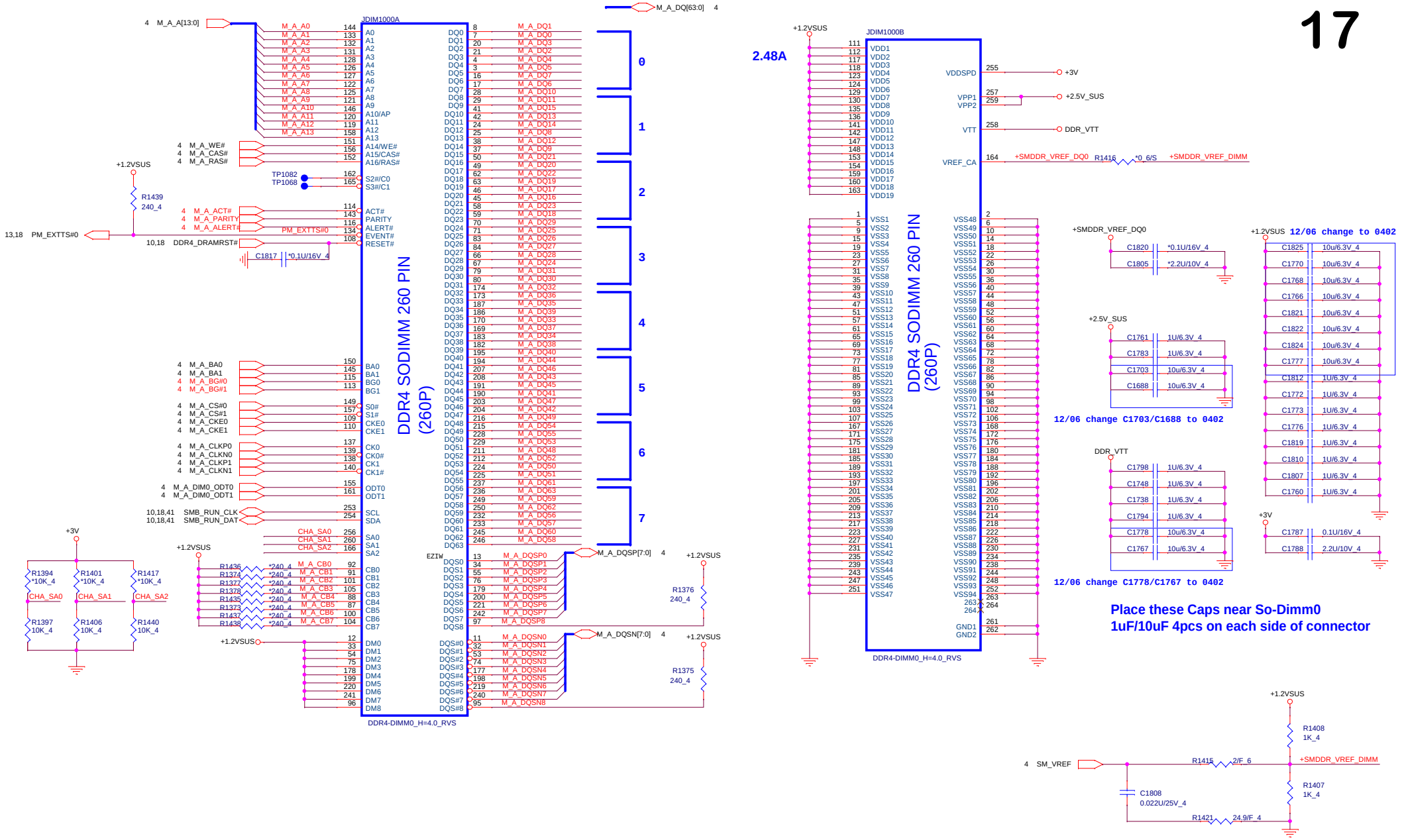
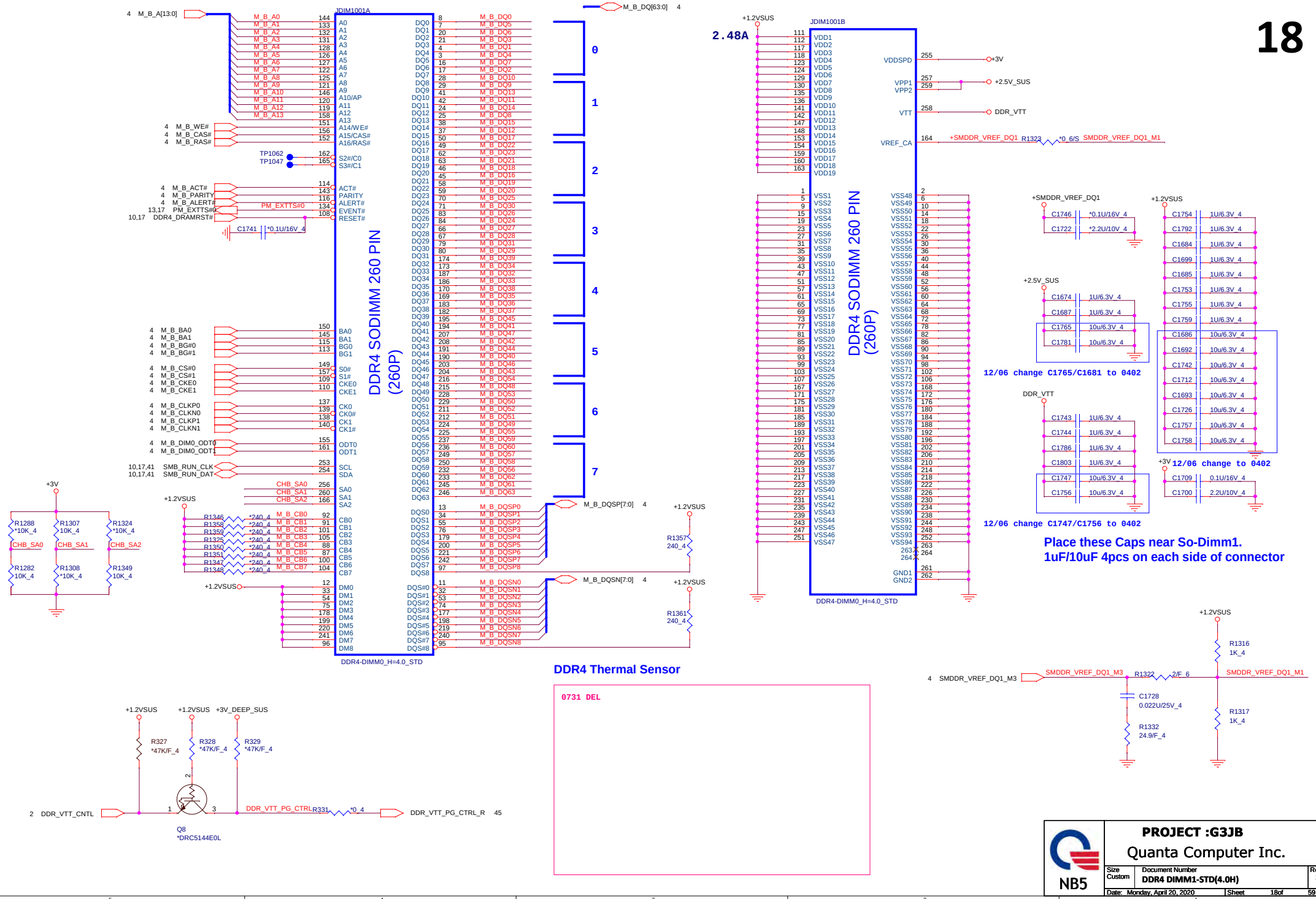
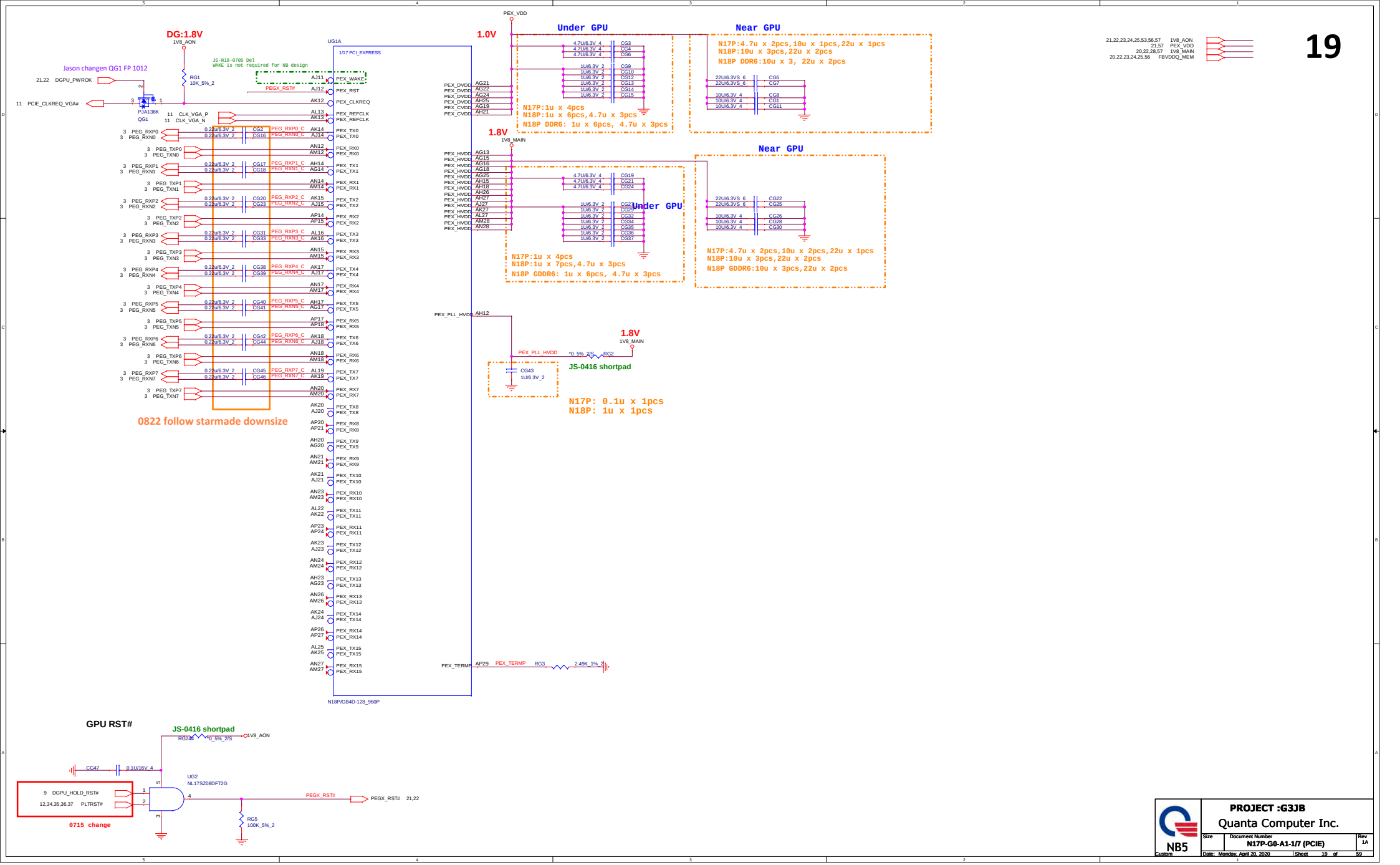
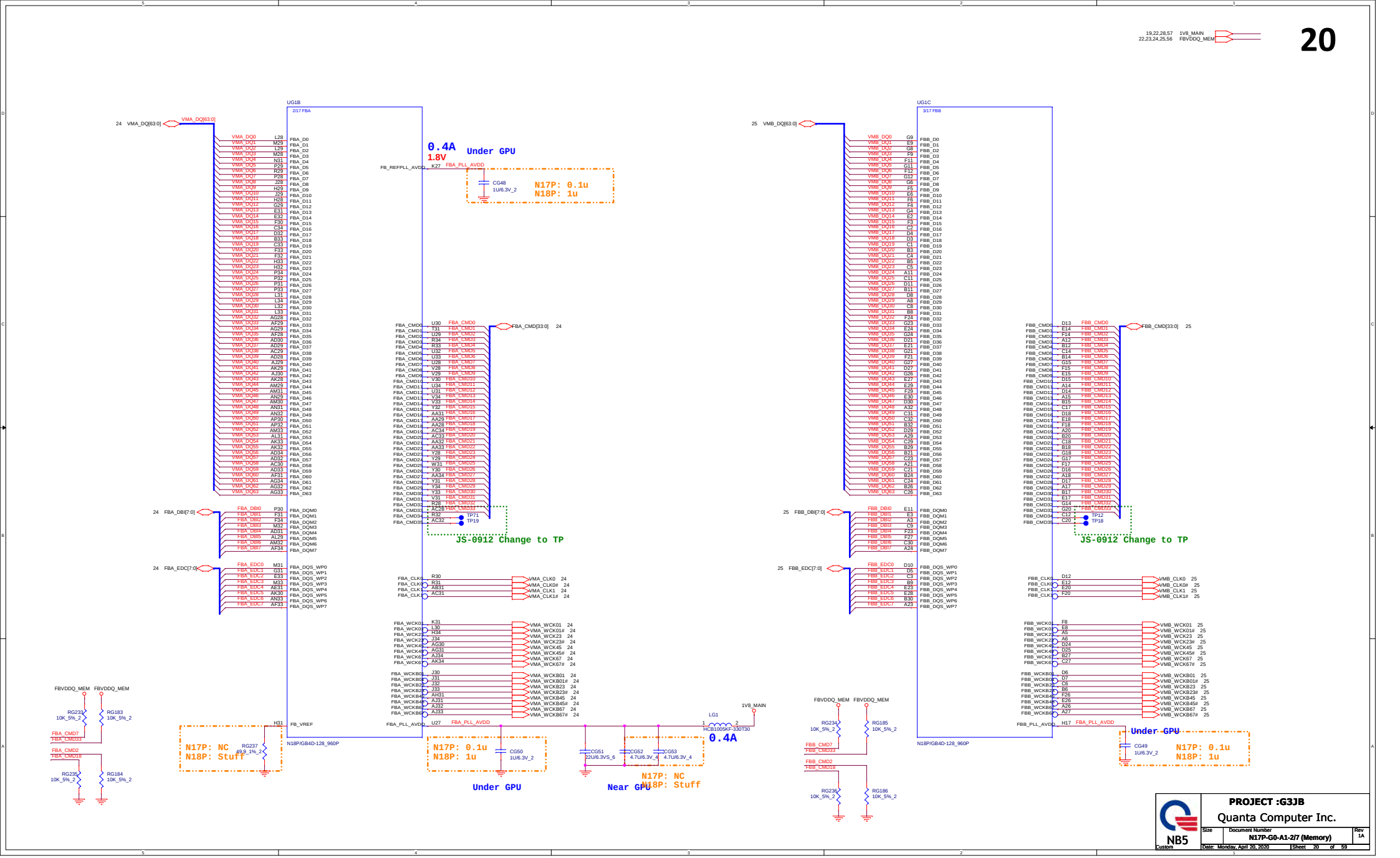


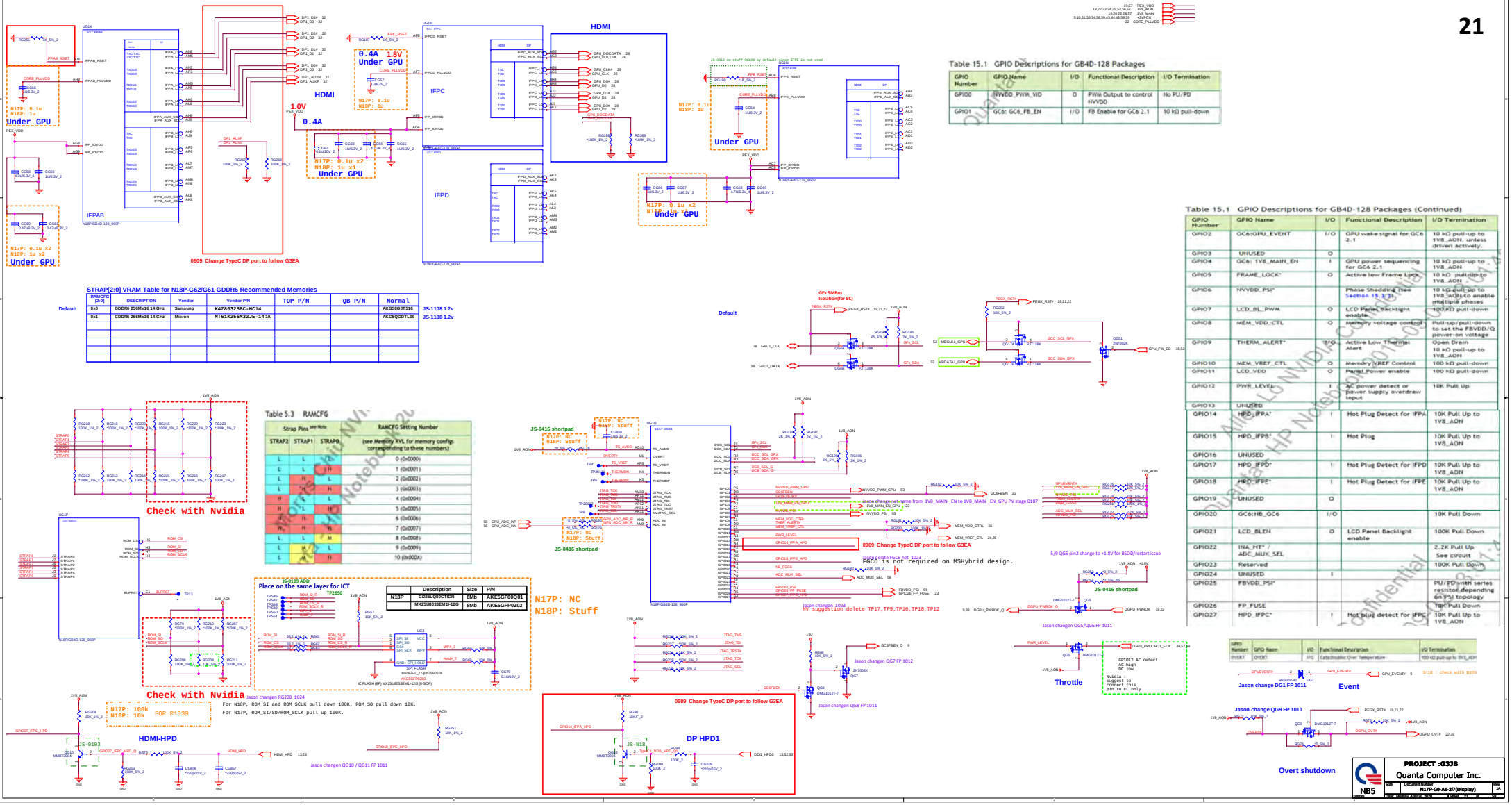
NB5	PROJECT :G3JB
	Quanta Computer Inc.
Size: Custom	Document Number: DDR4 DIMM0-RSV(4.0H)
Rev: 1A	
Date: Monday, April 20, 2020	Sheet 17of 59

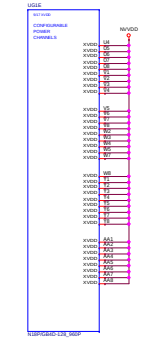


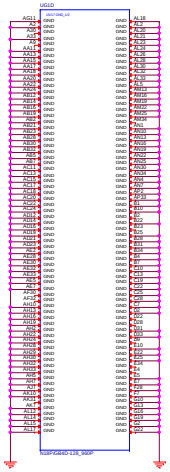
PROJECT :G3JB			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: DDR4 DIMM1-STD(4.0H)	Rev: 1A
	Date: Monday, April 20, 2020	Sheet: 18of	59

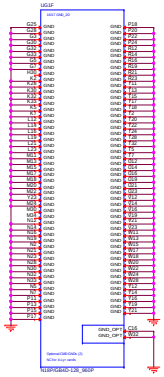


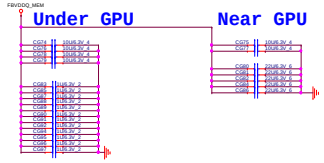












Note: JS-0925 NV suggestion change to NC even N18P only

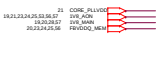
BOTH GP107 AND TU117-G5 NEED
NC AF30,AF32,AK31,AM34,F34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

If N18P only, connect these pin to GND

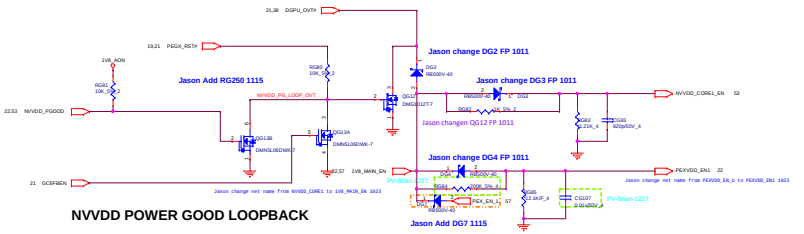
If N17P/N18P co-layout, leave these pin NC

If N17P only, leave these pin NC

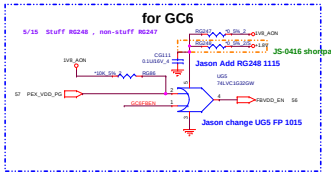
Jason remove those FGC6 1023

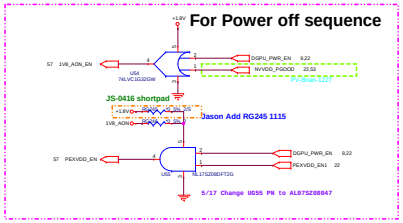


Overt temp ckt for NVVDD

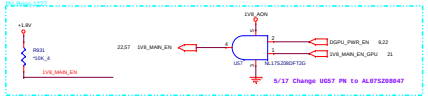


NVVDD POWER GOOD LOOPBACK

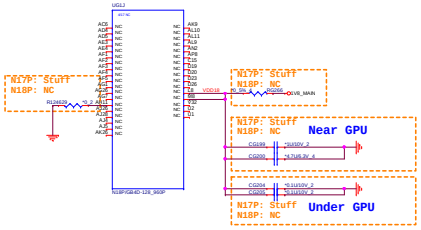


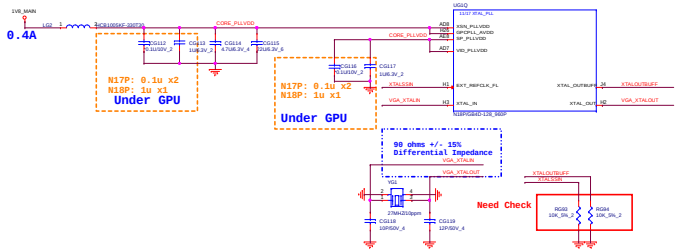


Jason add For Power off sequence 1023

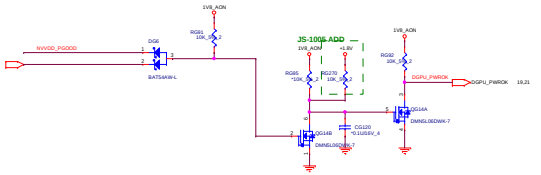


	GC6_1V8_MAIN_EN	GC6FBEN	NB_FGC6	1V8_AON	1V8_MAIN	NVVDD	PEX_VDD	FBVDDQ
POWER ON	1	0	0	ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FGC6	0	1	1	ON	ON	OFF	ON	ON





GPU All power good



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NB5
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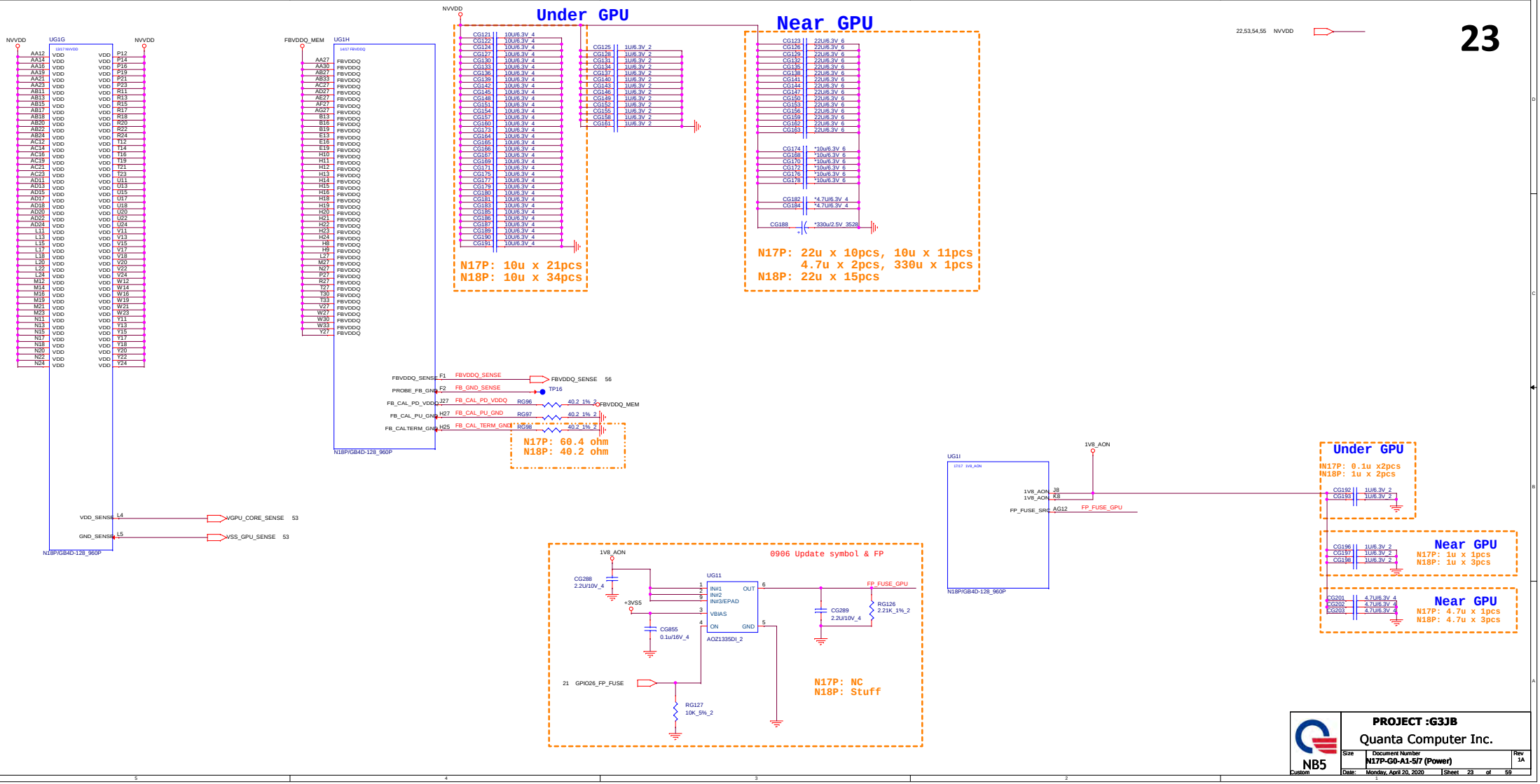

NB5 Custom	PROJECT :G3JB Quanta Computer Inc.	
	Size: Document Number: N17P-G0-A1-5/7 (Power)	Rev: 1A
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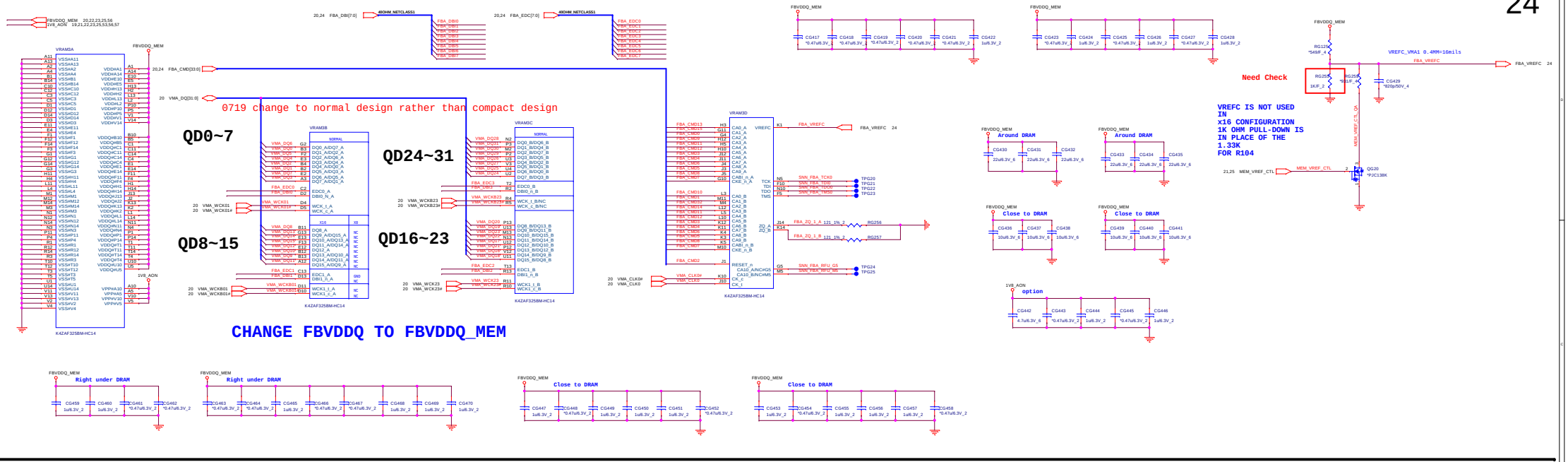
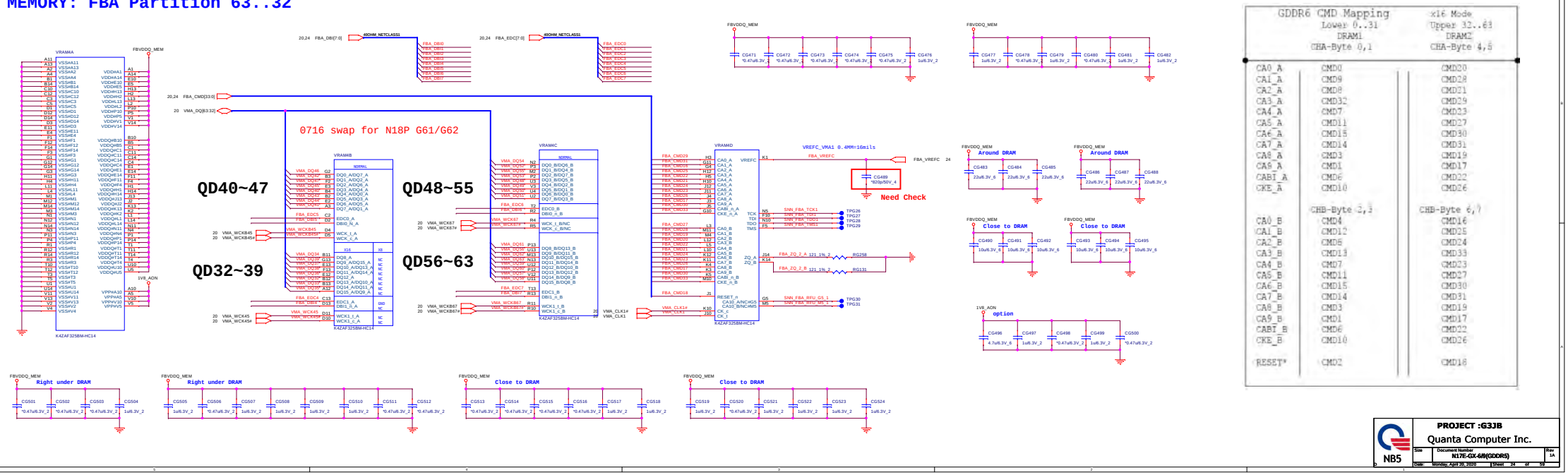
MEMORY: FBA Partition 31..0



MEMORY: FBA Partition 63..32



GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

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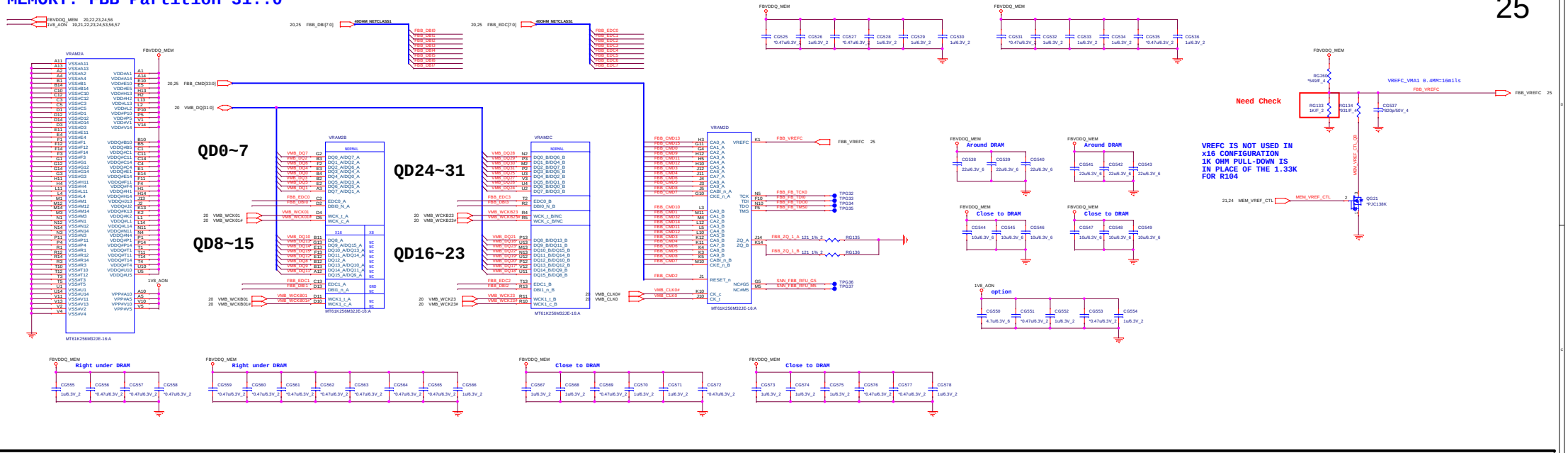
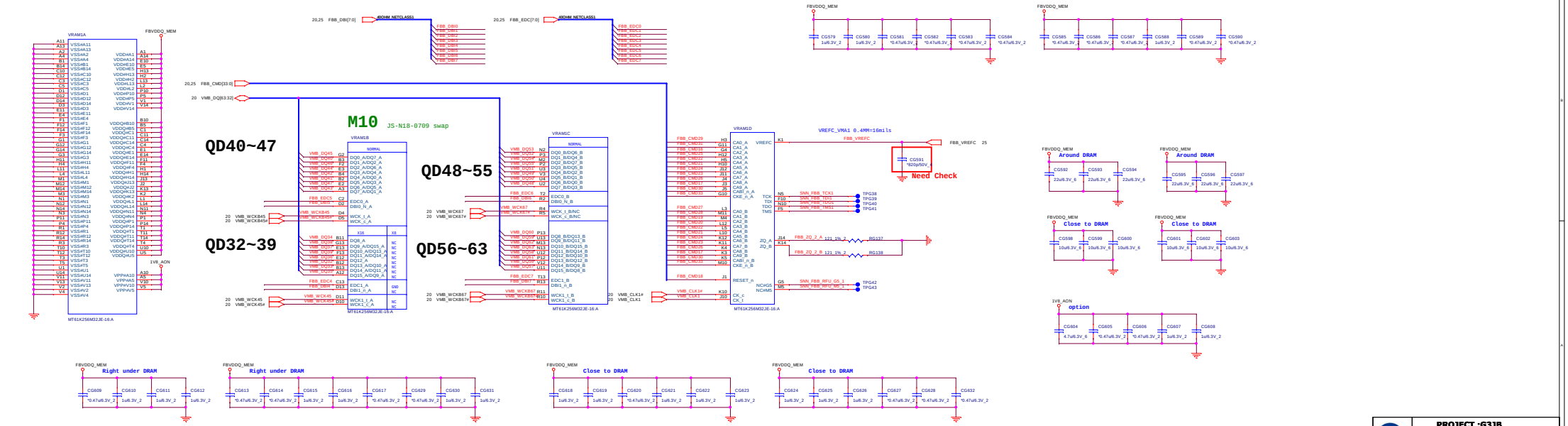
MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



NB5	PROJECT :G3JB Quanta Computer Inc.	
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NB5

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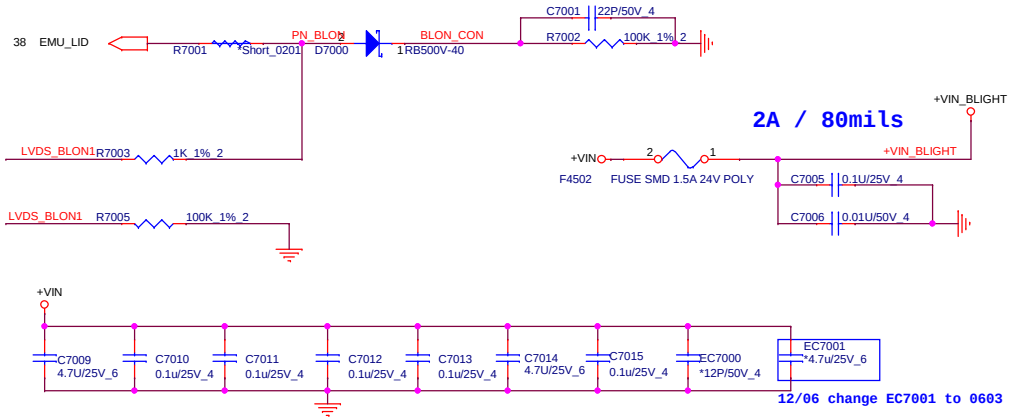
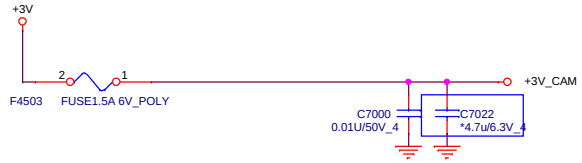
LID Switch

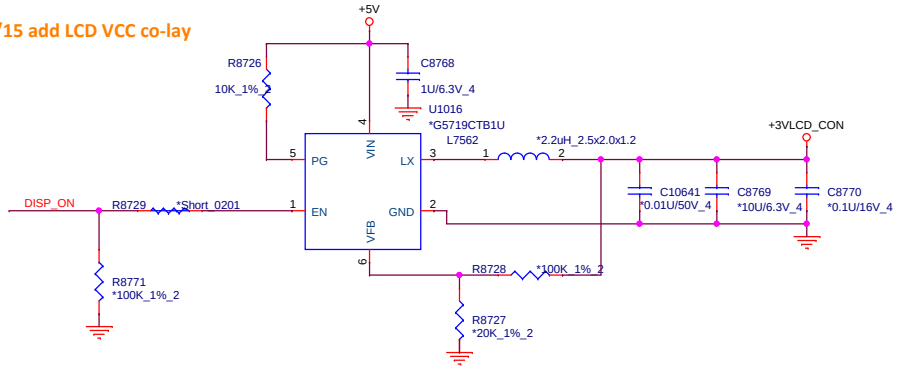


Touch screen



2/13 : Del TS Power

2/15 add LCD VCC co-lay



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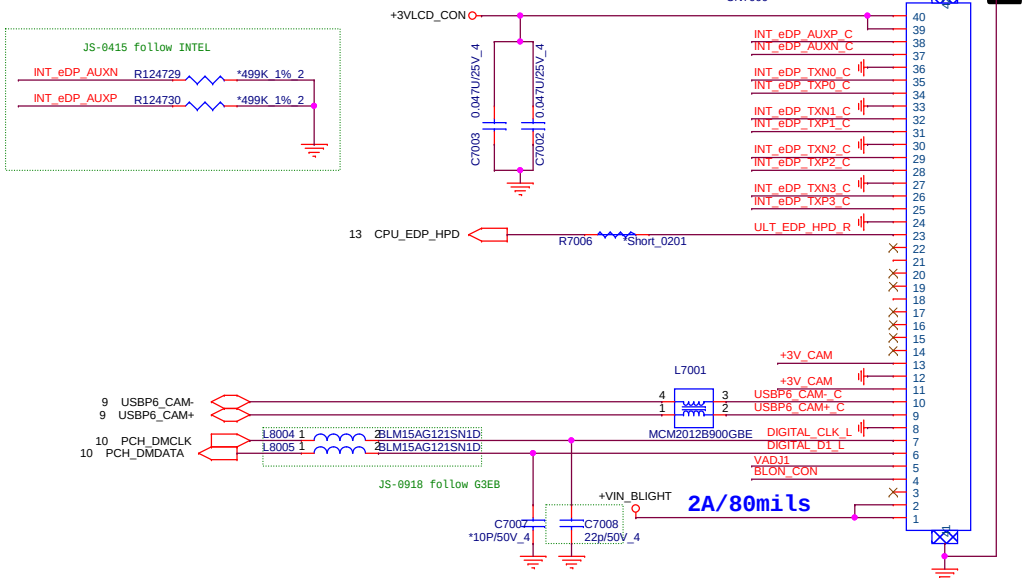
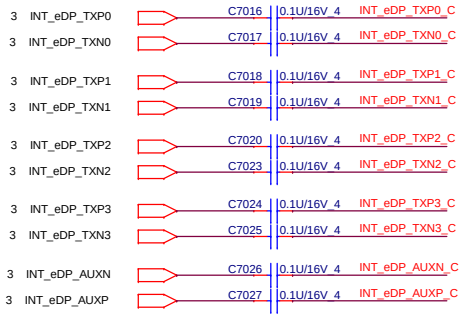
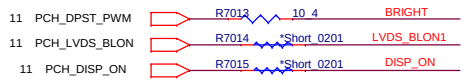
eDP Conn.

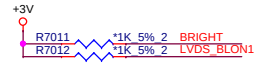
3/17 : Change CN7000 FP

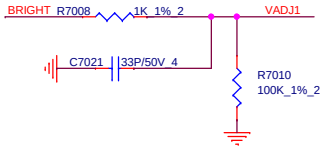
FFC 40P 1R FR
51693-0400t-v01-40p-l
DFFC40FR103
CN7000

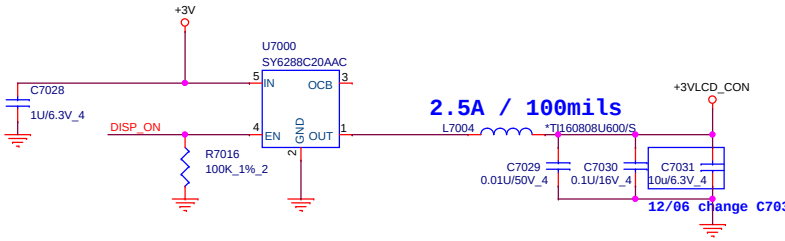












9,10,11,13,16,17,18,21,29,32,34,35,36,37,38,40,41,48,52,53,54,55,56,57 +3V
5,10,31,33,34,38,39,43,44,48,58,59 +3VPCU
28,29,32,35,40,49,50,51,52,58 +5V
40,41,42,43,44,45,46,47,49,51,54,56 +VIN

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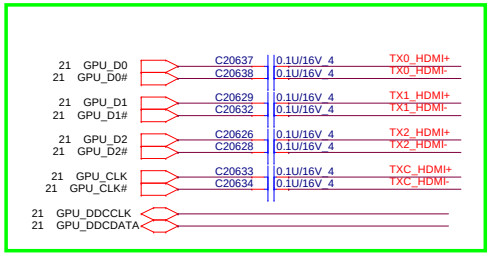
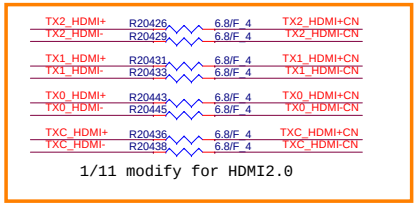
9,10,11,13,16,17,18,21,27,29,32,34,35,36,37,38,40,41,48,52,53,54,55,56,57 +3V

27,29,32,35,40,49,50,51,52,58 +5V

11/03 modify for HDMI2.0



01/11 change to 0 ohm for NV suggest



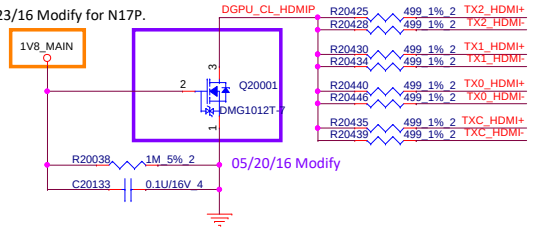
1/11 modify for HDMI2.0

01/11 unstuff for HDMI output from GPU

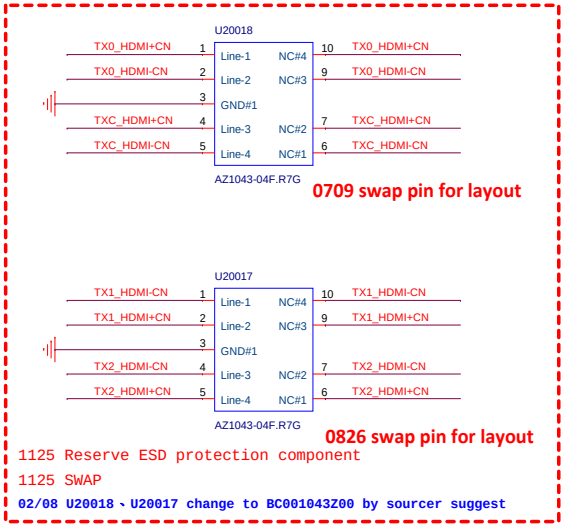
EMI Solution

11/04 modify for HDMI2.0

03/23/16 Modify for N17P.



ESD



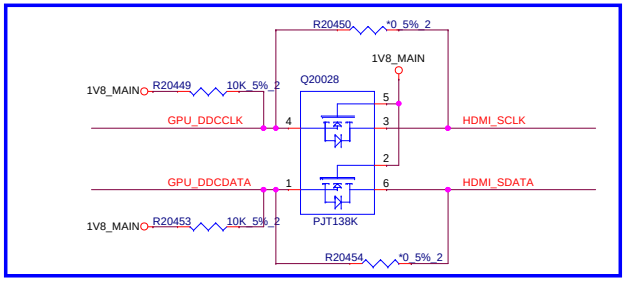
1125 Reserve ESD protection component

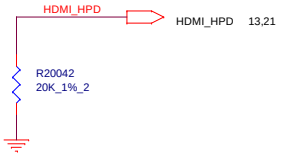
1125 SWAP

02/08 U20018、U20017 change to BC001043Z00 by sourcer suggest

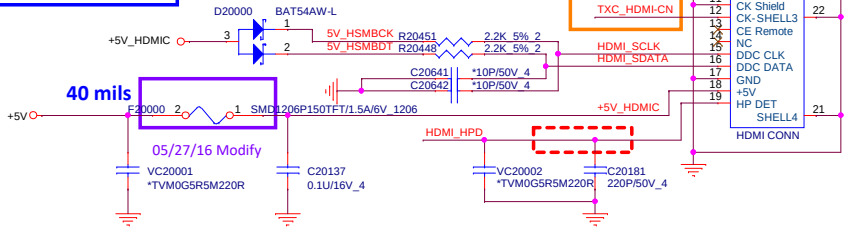
HDMI SMBus Isolation

Close to HDMI connector





01/15 update to DFHD19MR440



NB5

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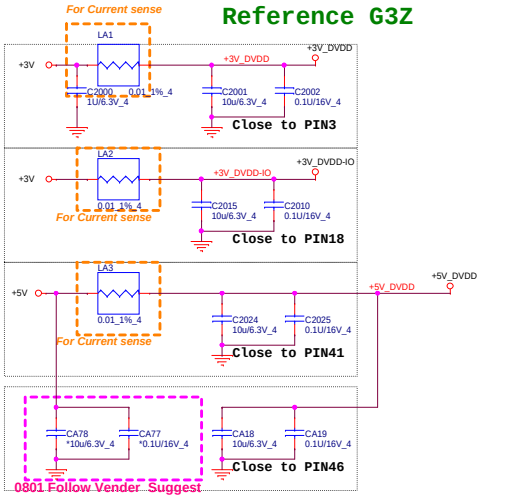
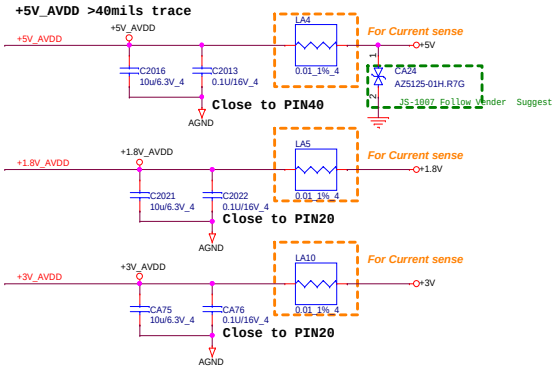
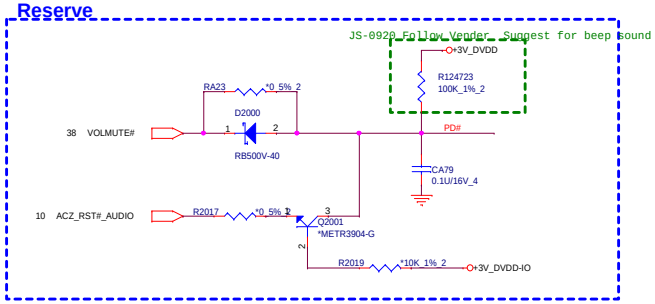
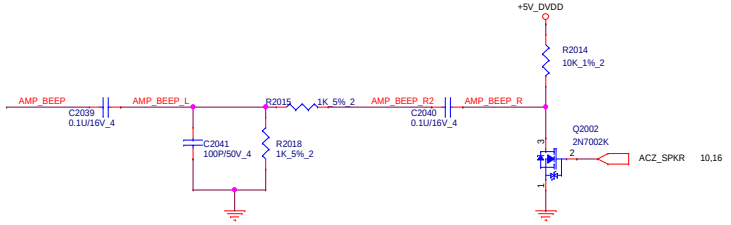
Reference G3Z

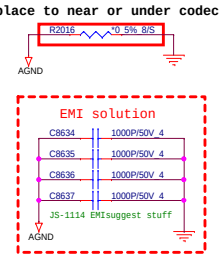


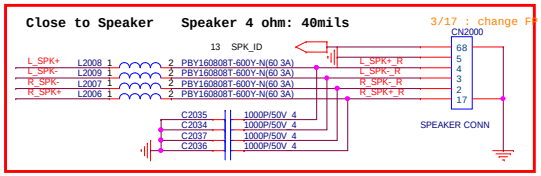


Reserve









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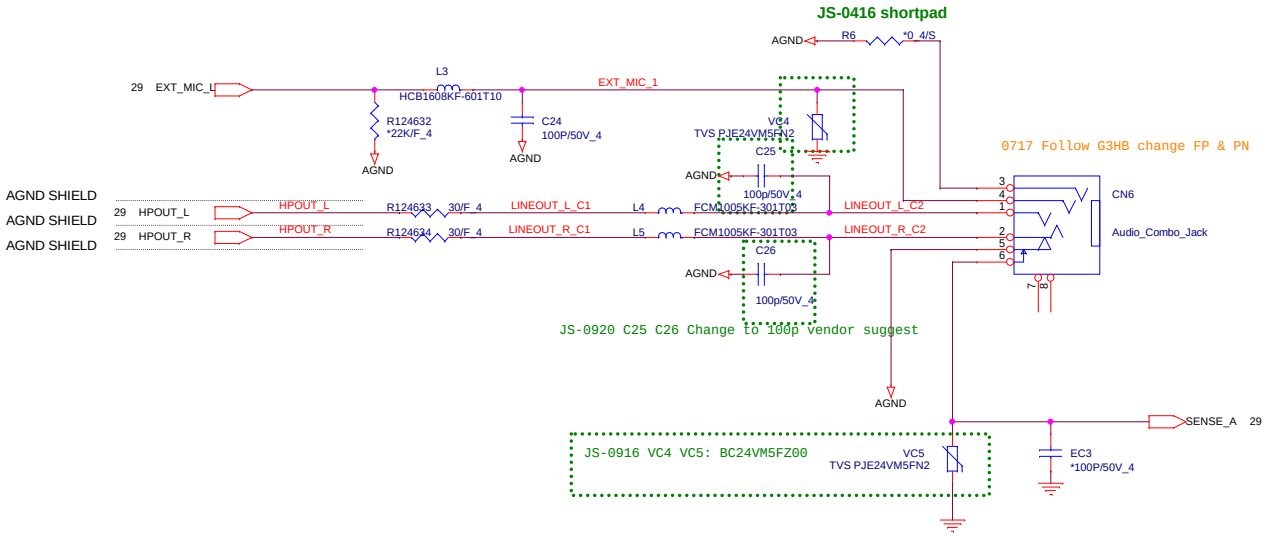
Head Phone out



HOLE

NB5	PROJECT :G3JB Quanta Computer Inc.	
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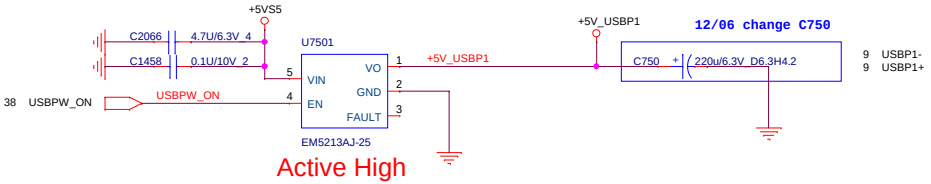
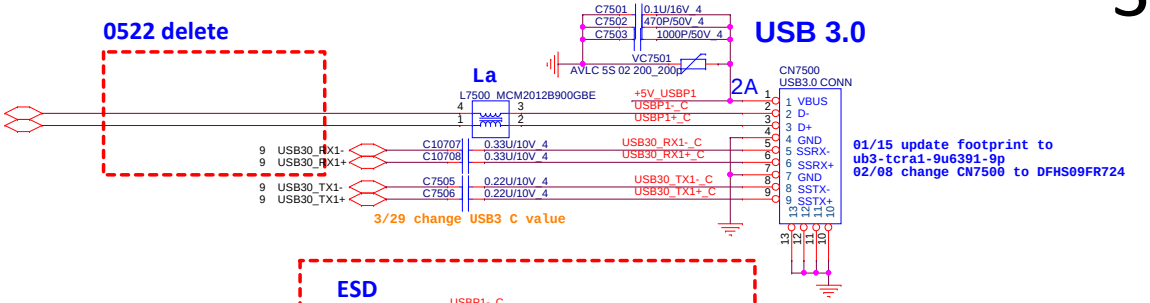
USB BC1.2



Active High

0522 delete

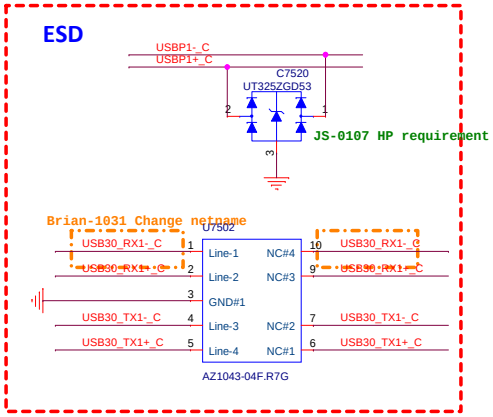
USB 3.0



3/29 change USB3 C value

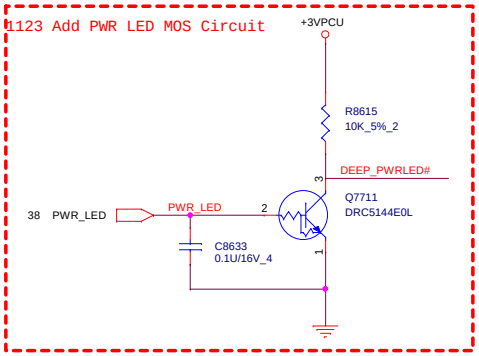
01/15 update footprint to ub3-tcra1-9u6391-9p
02/08 change CN7500 to DFHS09FR724

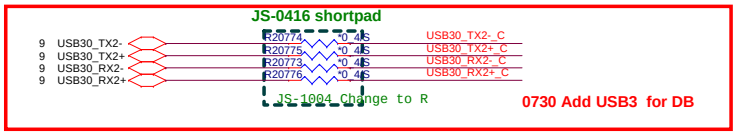
ESD

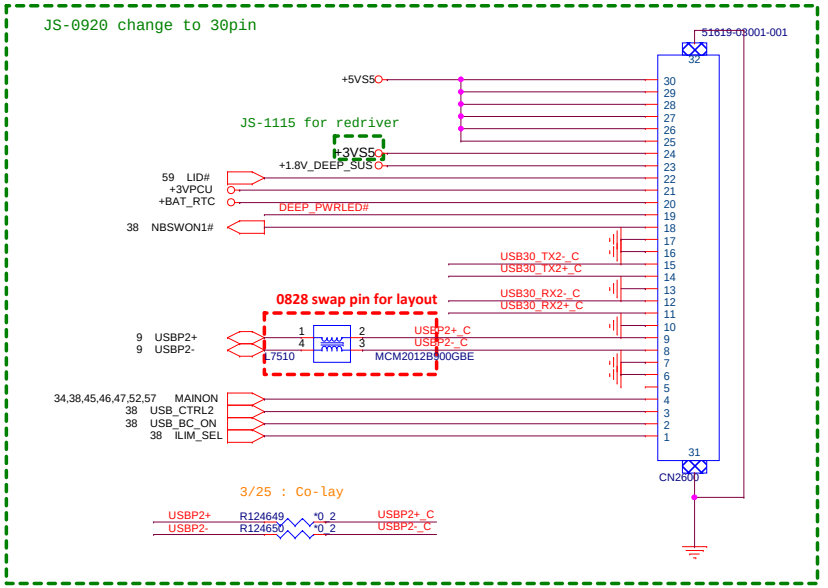


Daughter Board

Power LED







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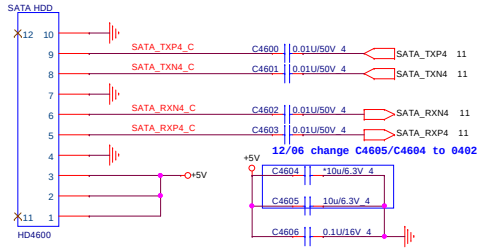
HDD



SATA LED

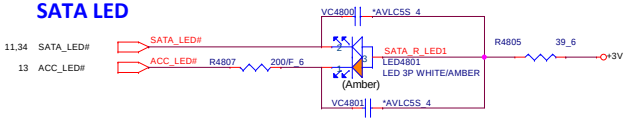


Table 7. TUSB546-DCI Receiver Equalization GPIO Control

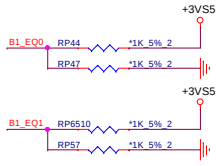
Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	0.2	0	0	-1.6	0	0	1.0
1	0	R	1.2	0	R	-0.5	0	R	3.3
2	0	F	2.2	0	F	0.5	0	F	4.9
3	0	1	3.3	0	1	1.6	0	1	6.5
4	R	0	4.2	R	0	2.4	R	0	7.5
5	R	R	5.1	R	R	3.4	R	R	8.6
6	R	F	5.9	R	F	4.1	R	F	9.5
7	R	1	6.7	R	1	4.9	R	1	10.4
8	F	0	7.4	F	0	5.7	F	0	11.1
9	F	R	8.1	F	R	6.4	F	R	11.7
10	F	F	8.7	F	F	6.9	F	F	12.3
11	F	1	9.3	F	1	7.5	F	1	12.8
12	1	0	9.7	1	0	8.0	1	0	13.2
13	1	R	10.2	1	R	8.5	1	R	13.6
14	1	F	10.6	1	F	8.9	1	F	14.0
15	1	1	11.1	1	1	9.4	1	1	14.4

TUSB546 Pin Control Mode

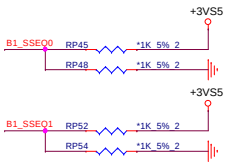
CTL1	CTL0	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

MUX TUSB546I

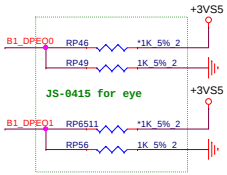
I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V



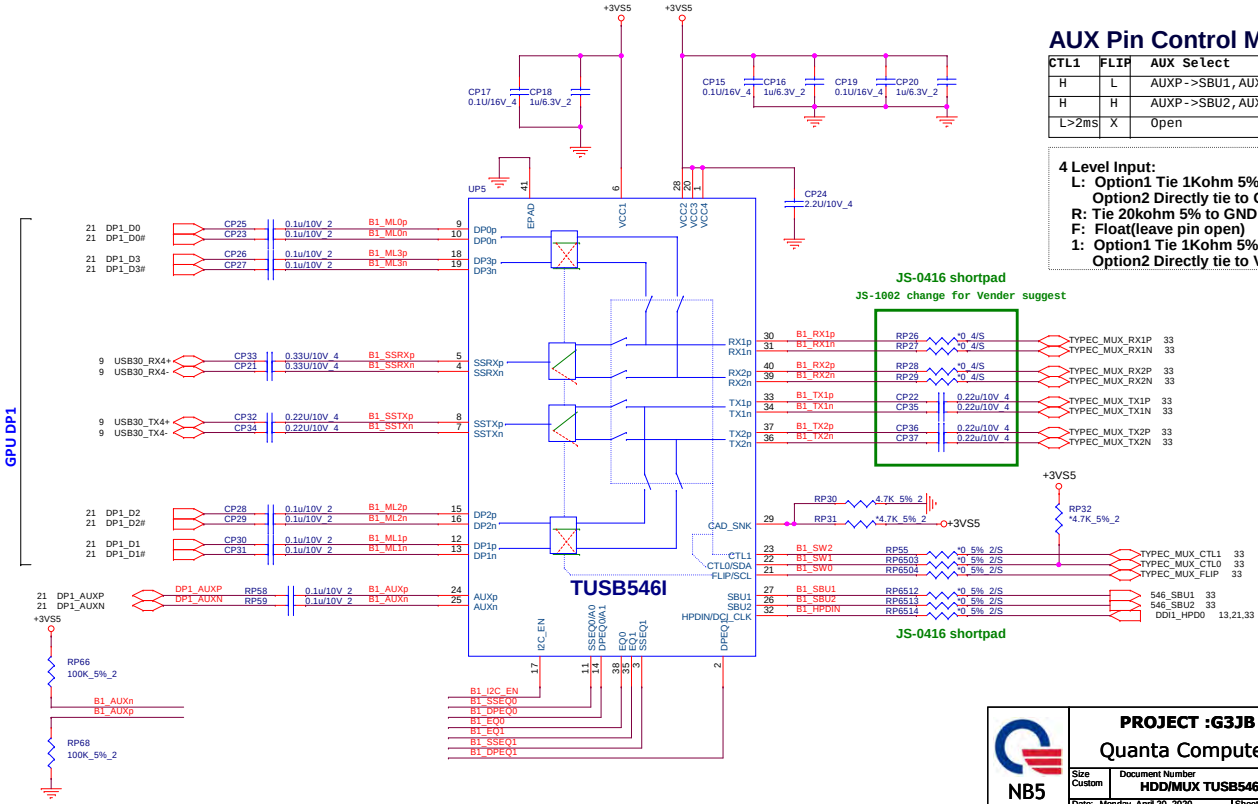
EQ0,EQ1 : USB receiver equalizer gain
for downstream facing RX1 & RX2
F,F(Default)



SSEQ0,SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress



DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress



AUX Pin Control Mode

CTL1	FLIP	AUX Select
H	L	AUXP->SBU1,AUXN->SBU2
H	H	AUXP->SBU2,AUXN->SBU1
L>2ms	X	Open

4 Level Input:
- L: Option1 Tie 1Kohm 5% to GND
  Option2 Directly tie to GND
- R: Tie 20kohm 5% to GND
- F: Float(leave pin open)
- 1: Option1 Tie 1Kohm 5% to Vcc
  Option2 Directly tie to Vcc

NB5

PROJECT :G3JB

Quanta Computer Inc.

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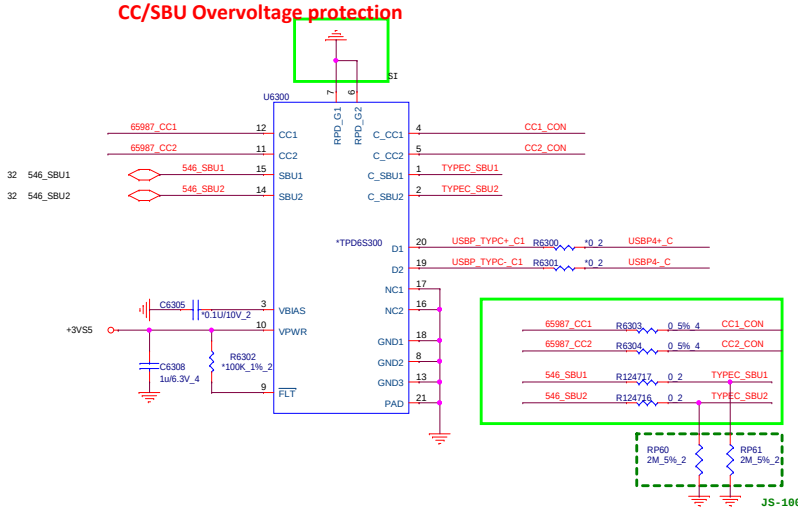
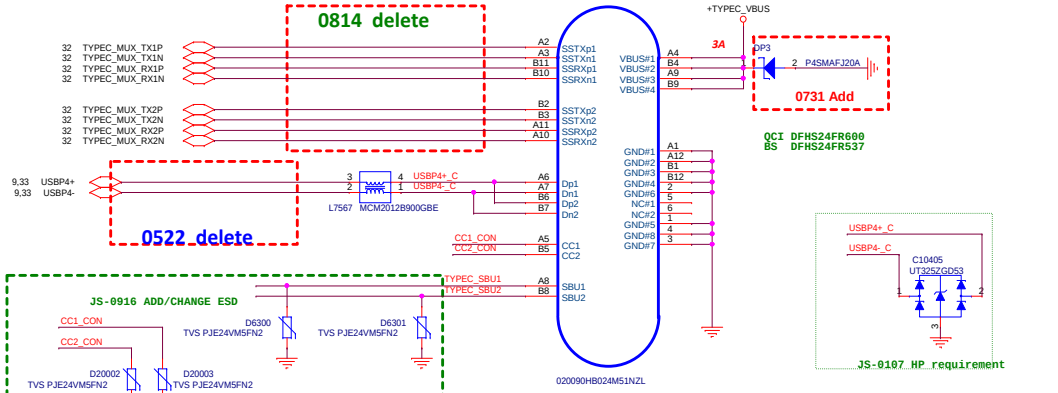
TYPE-C

CC/SBU Overvoltage protection



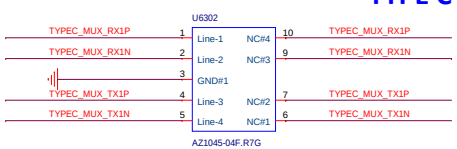
TYPE-C CONN

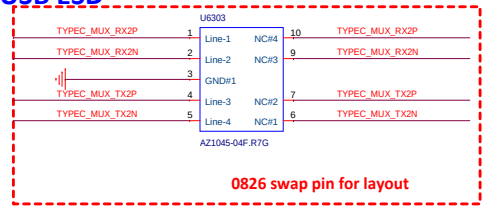
3/17 : change conn FP



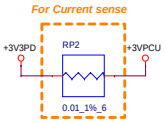
JS-0916 ADD/CHANGE ESD

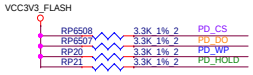
TYPE C USB ESD

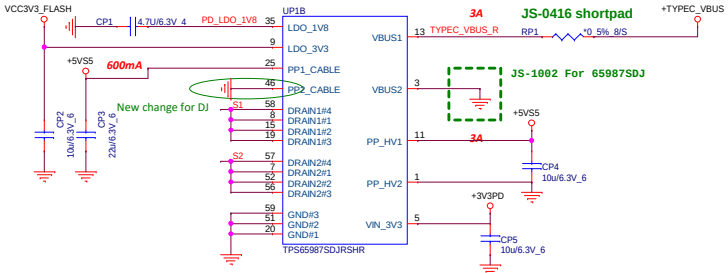


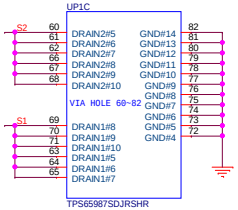


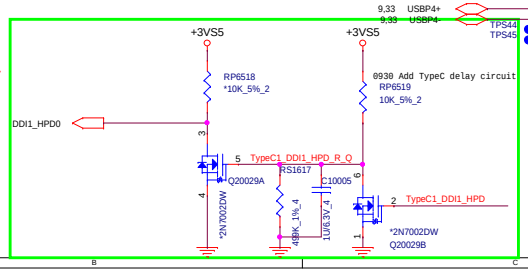
SN1809018
65987SDJ AL180901000

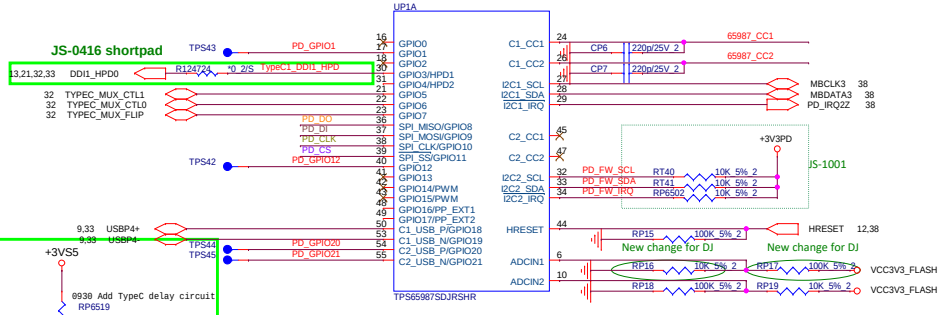












https://realschematic.com

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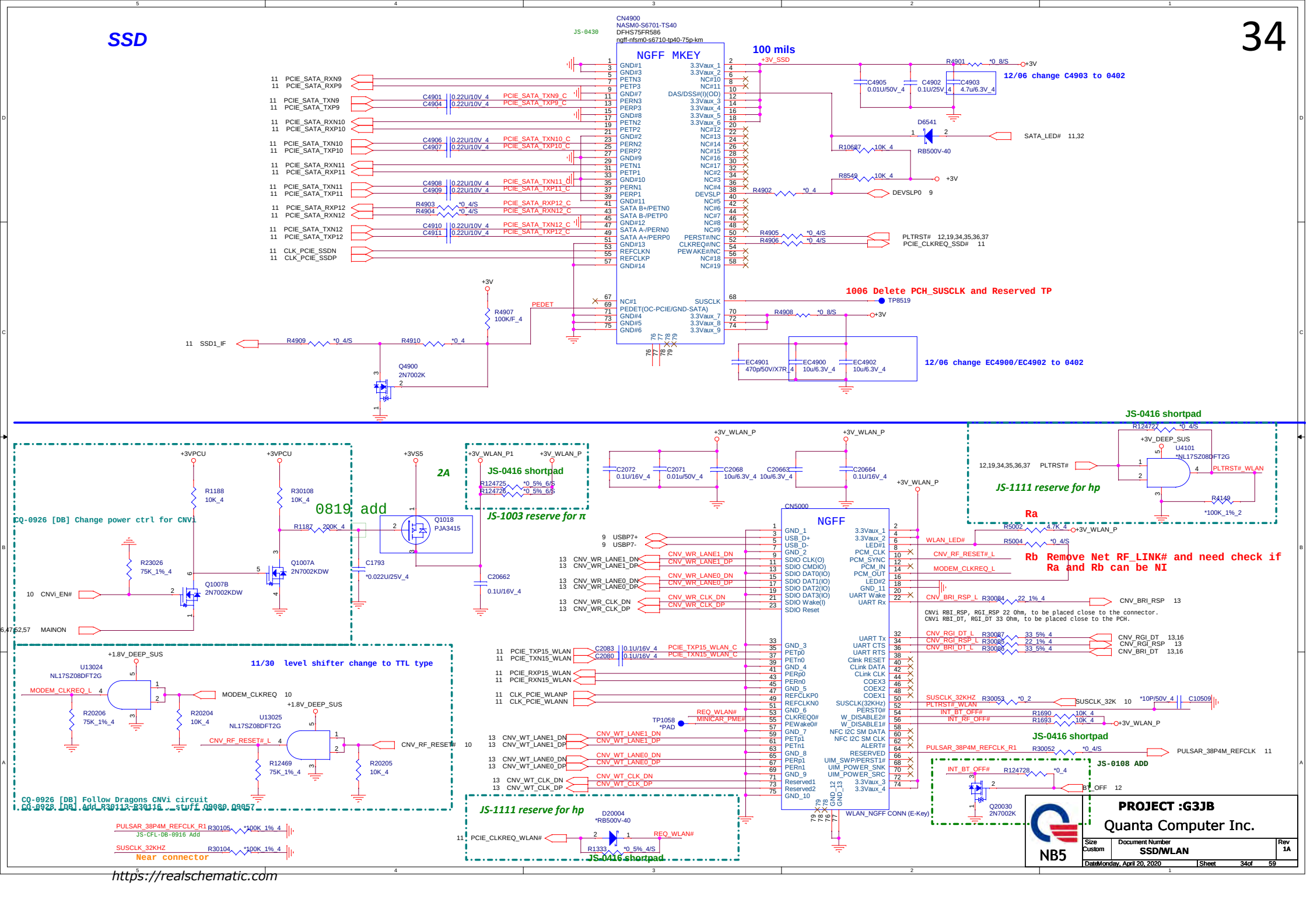
SSD



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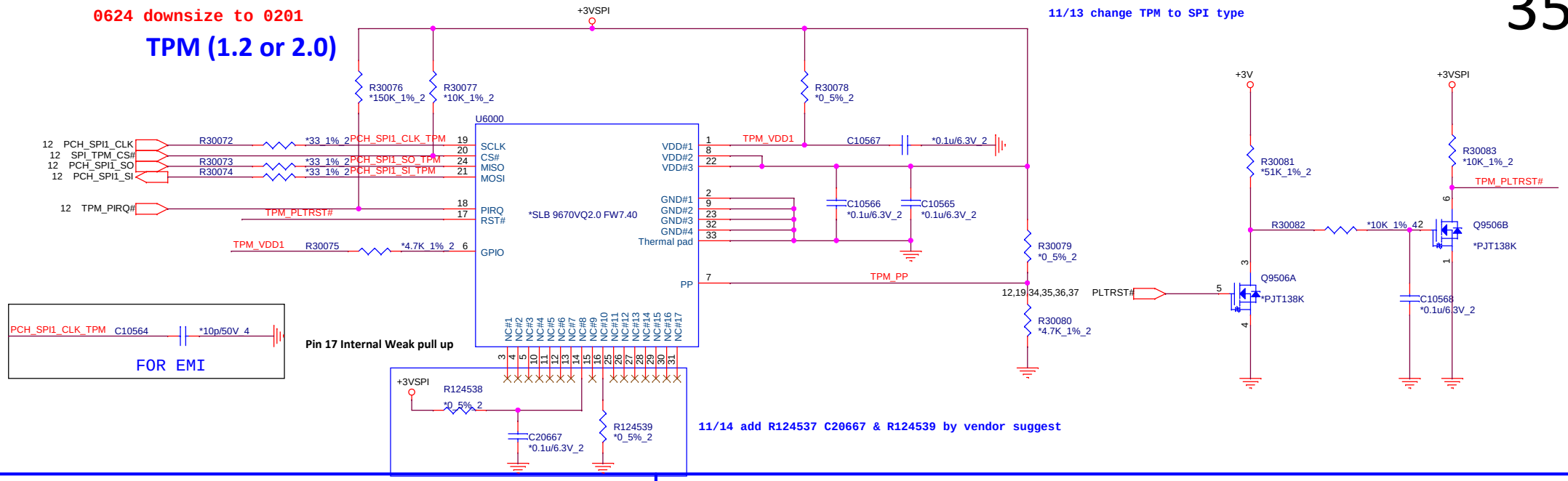
JS-0424 FROM G35P

0624 downsize to 0201

TPM (1.2 or 2.0)

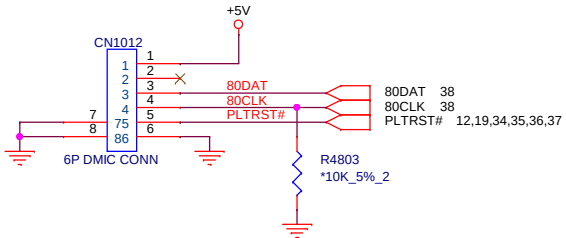
11/13 change TPM to SPI type



11/14 add R124537 C20667 & R124539 by vendor suggest

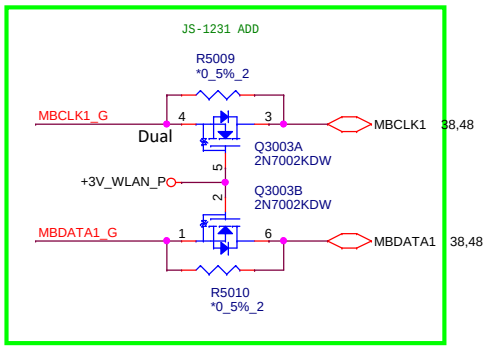
0801 Follow G3EA

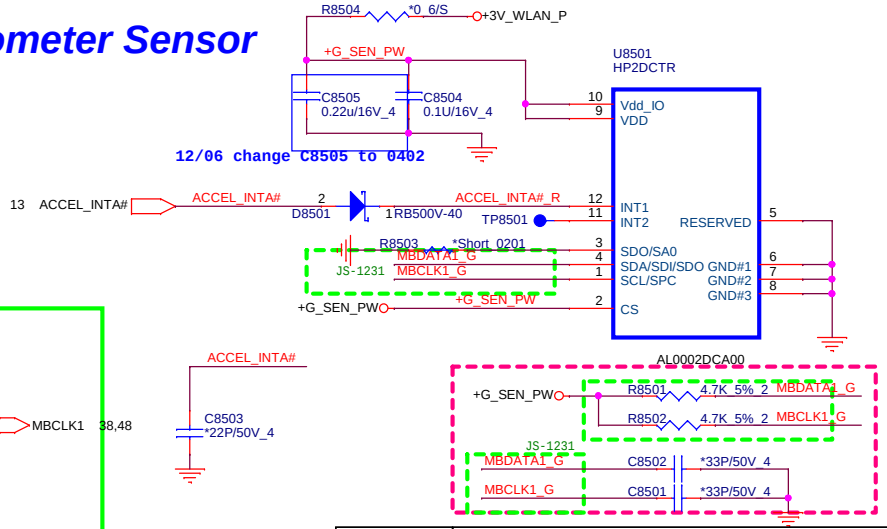
For debug



Accelerometer Sensor

12/06 change C8505 to 0402





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B	TPM/IR CAM/Sensor	1A
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NB5

LAN & RJ45

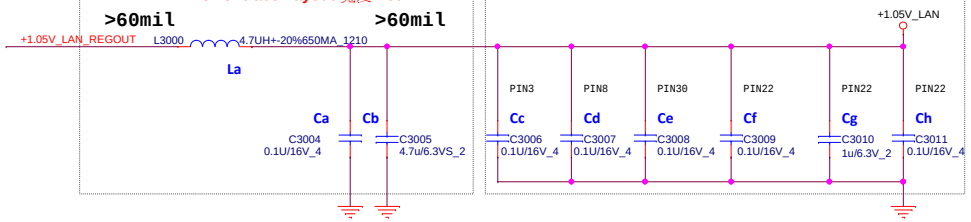
For SWR mode support RTL8111HSH/RTL8107ESH

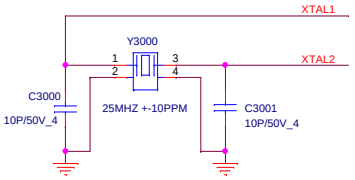
Stuff La, Ca ,Cb

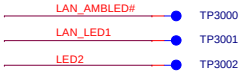
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

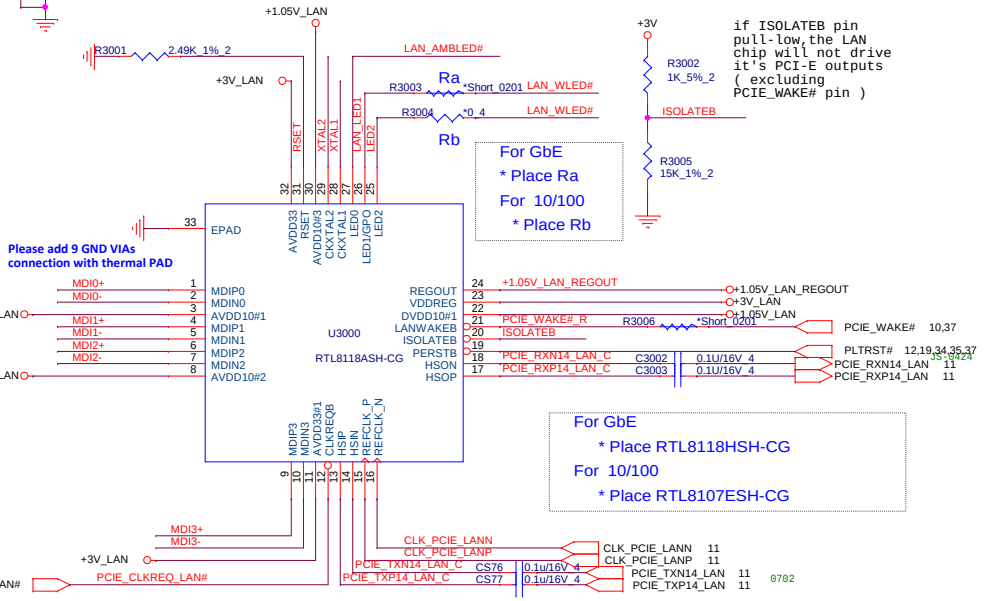
* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil

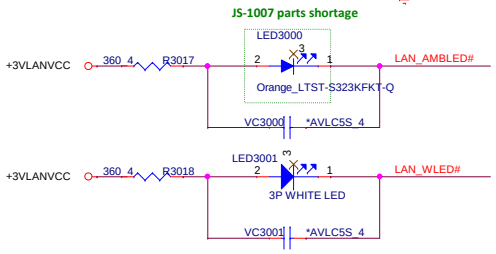






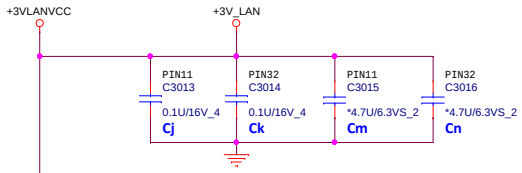


JS-1007 parts shortage



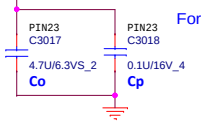
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

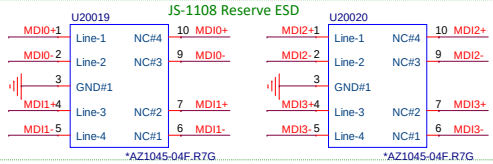


For SWR mode support RTL8111HSH/RTL8107ESH

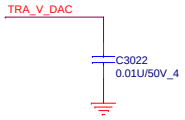
Stuff Co, Cp



JS-1108 Reserve ESD

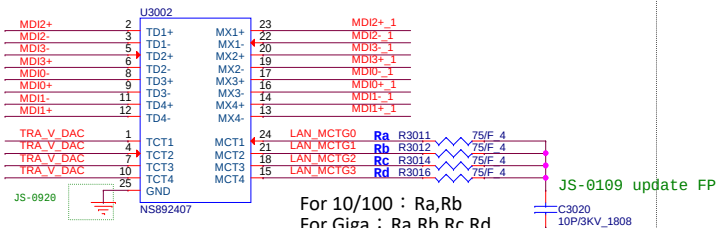


For 10/100：Ua
For Giga：Ub



1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00

Ub



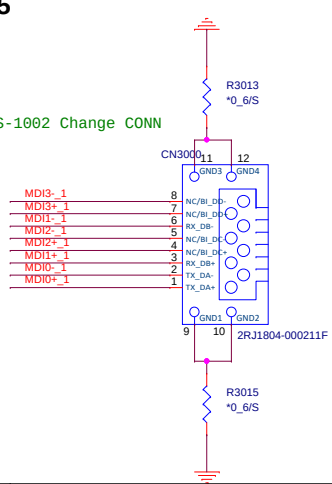
For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

9,10,11,13,16,17,18,21,27,29,32,34,35,37,38,40,41,48,52,53,54,55,56,57
52 +3V
+3VLANVCC

RJ45

JS-1002 Change CONN



NB5

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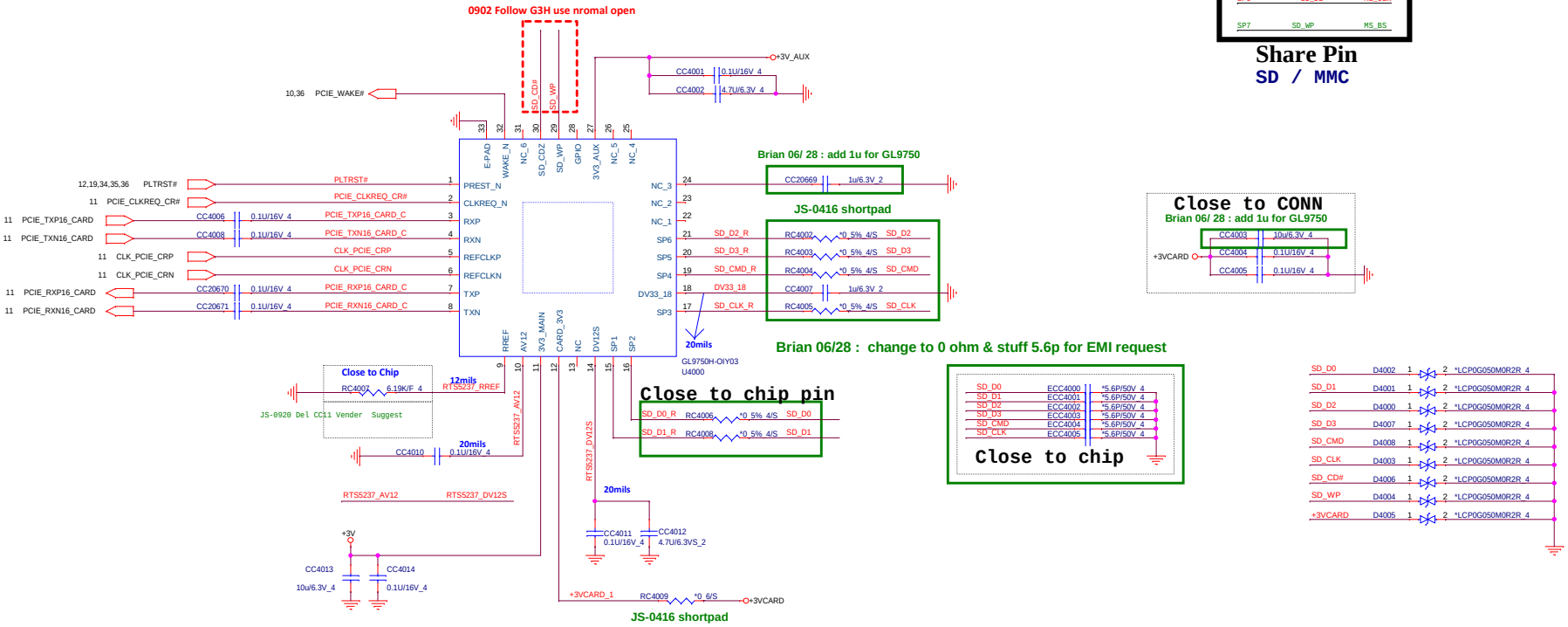
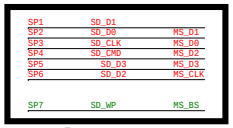
GL9750H PCIE CARD READER Controller

03





Share Pin
SD / MMC

Close to CONN
Brian 06/ 28 : add 1u for GL9750

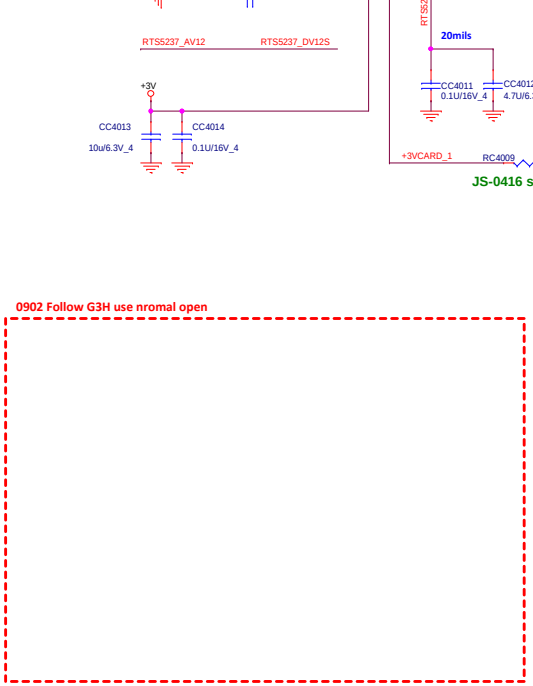
SD Connector

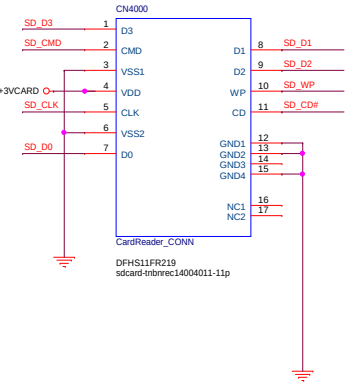
Without card	CD —o o— CD/WP com WP —o o— CD/WP com
inserted card(unlock)	CD —o—o— CD/WP com WP —o—o— CD/WP com
inserted card(lock)	CD —o—o— CD/WP com WP —o o— CD/WP com

Pin Define

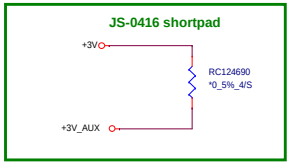
Pin No.	NAME	Pin No.	NAME
1	CD/DAT3	8	DAT1
2	CMD	9	DAT2
3	Vss1	10	WP Pin
4	VDD	11	CD Pin
5	CLK		
6	Vss2		
7	DAT0		

0902 Follow G3H use nromal open

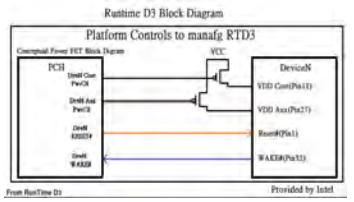




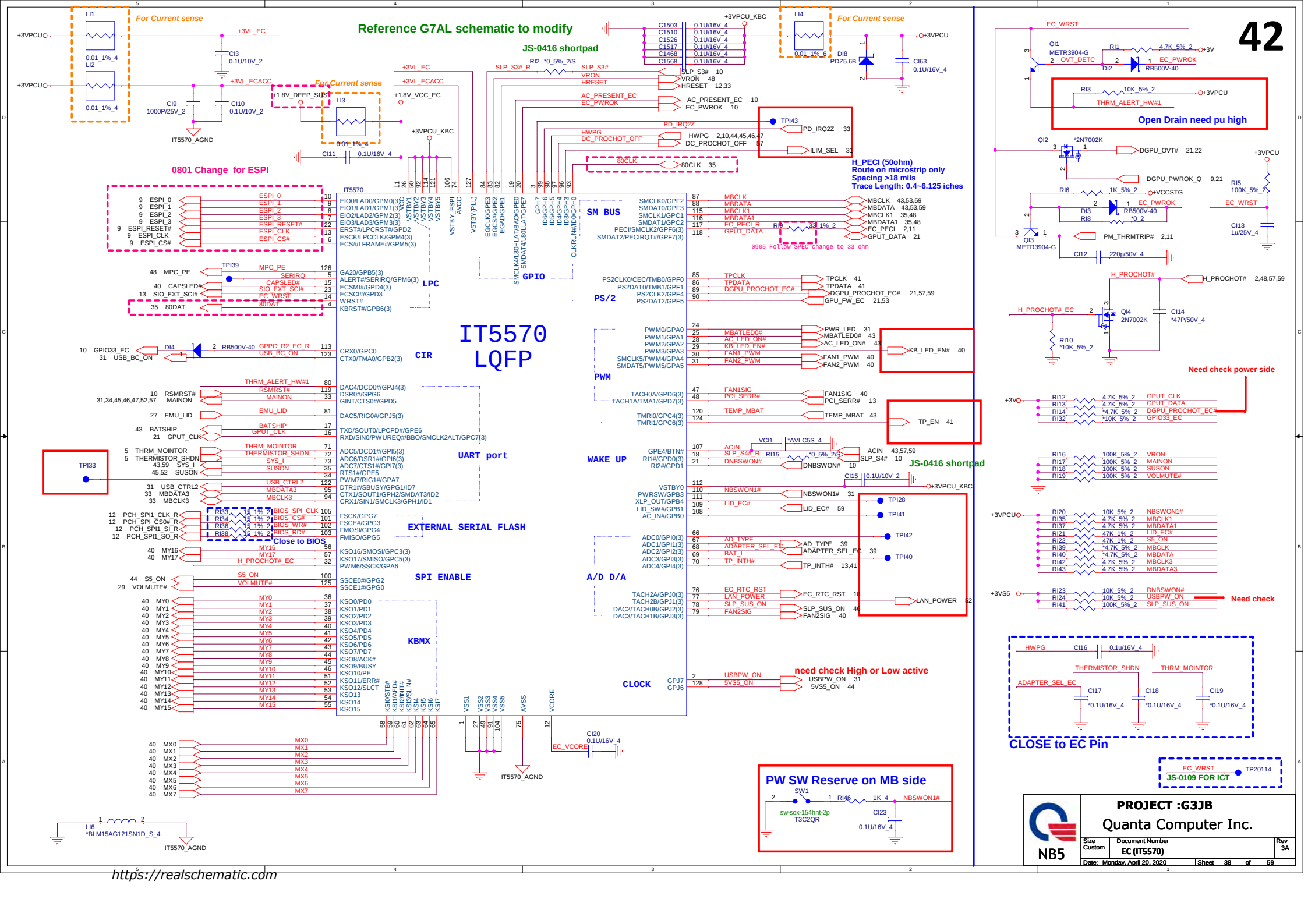
RTD3



Support Runtime D3 mode => R12 don't mount
No Support Runtime D3 mode =>R12 mount
Form System's PCIE interface



NB5	PROJECT :G3JB Quanta Computer Inc. Size C · Document Number CR RTS5237S/CR SOCKET · Rev 1A Date Monday, April 20, 2020 · Sheet 37 of 59


Reference G7AL schematic to modify
JS-0416 shortpad
For Current sense
0801 Change for ESPI
IT5570
LQFP
SM BUS
GPIO
LPC
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
0985 Follow SPEC change to 33 ohm
Open Drain need pu high
Need check power side
Need check
Close to BIOS
need check High or Low active
PW SW Reserve on MB side
CLOSE to EC Pin
JS-0109 FOR ICT
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EC (IT5570)
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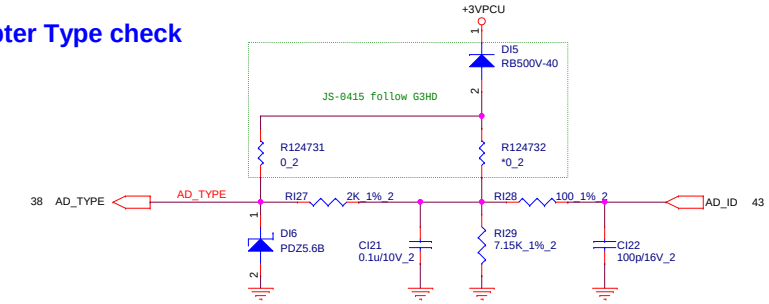
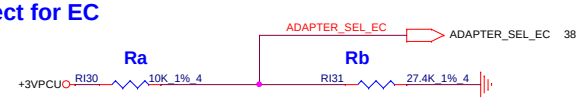
https://realschematic.com

Adapter Type check



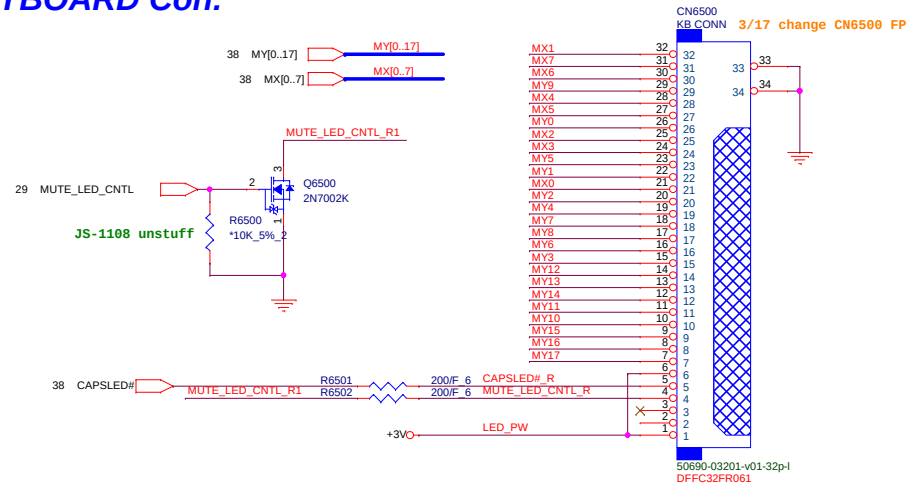
Adapter select for EC



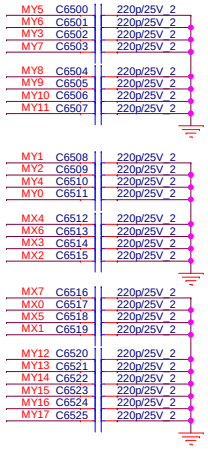
	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	N18E
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	N18P
135W	10K(CS31002FB26)	17.8K(CS31782FB10)	2.11V	N17P
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check

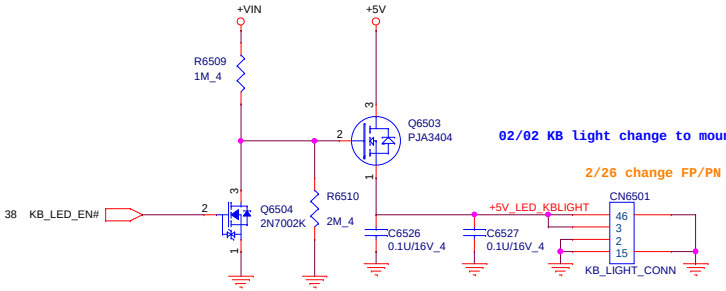
KEYBOARD Con.



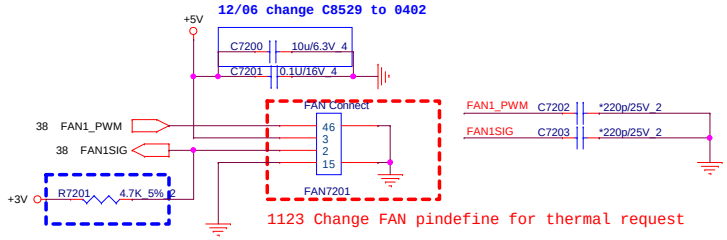
0821 follow starmade del KB PU RES



KB LIGHT CONN

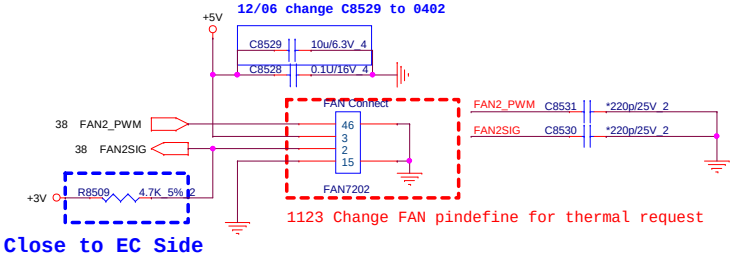


FAN



Close to EC Side

3/17 change FAN7201/FAN7202 FP



Close to EC Side

0827 DEL RGB reserved

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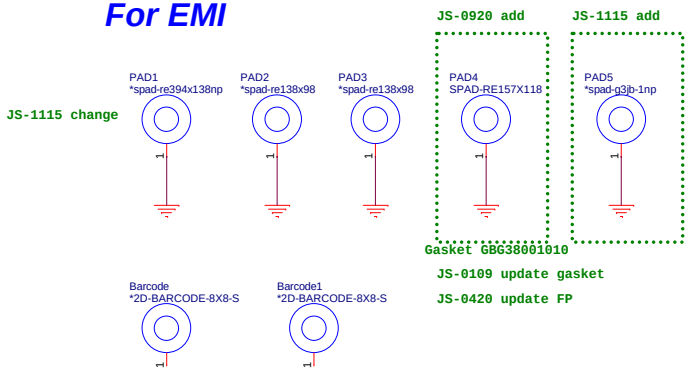
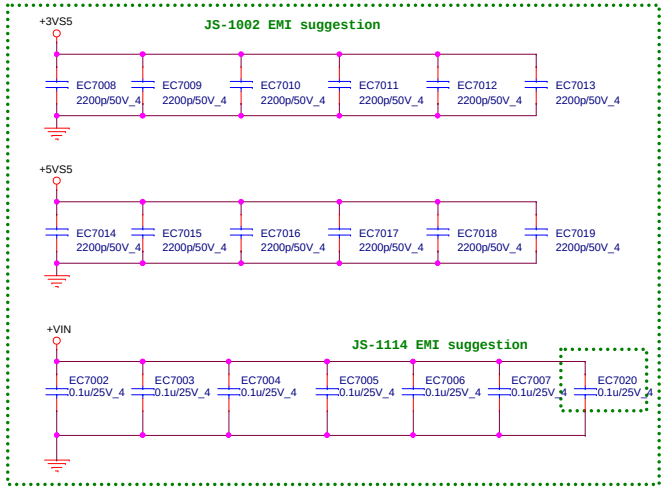
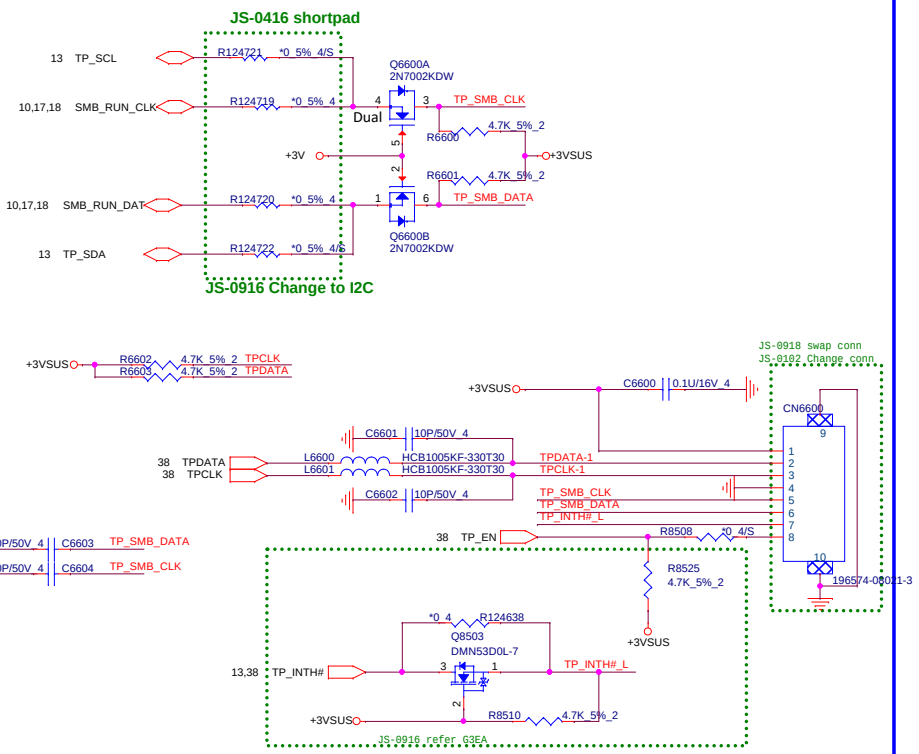
RF Solution

For EMI



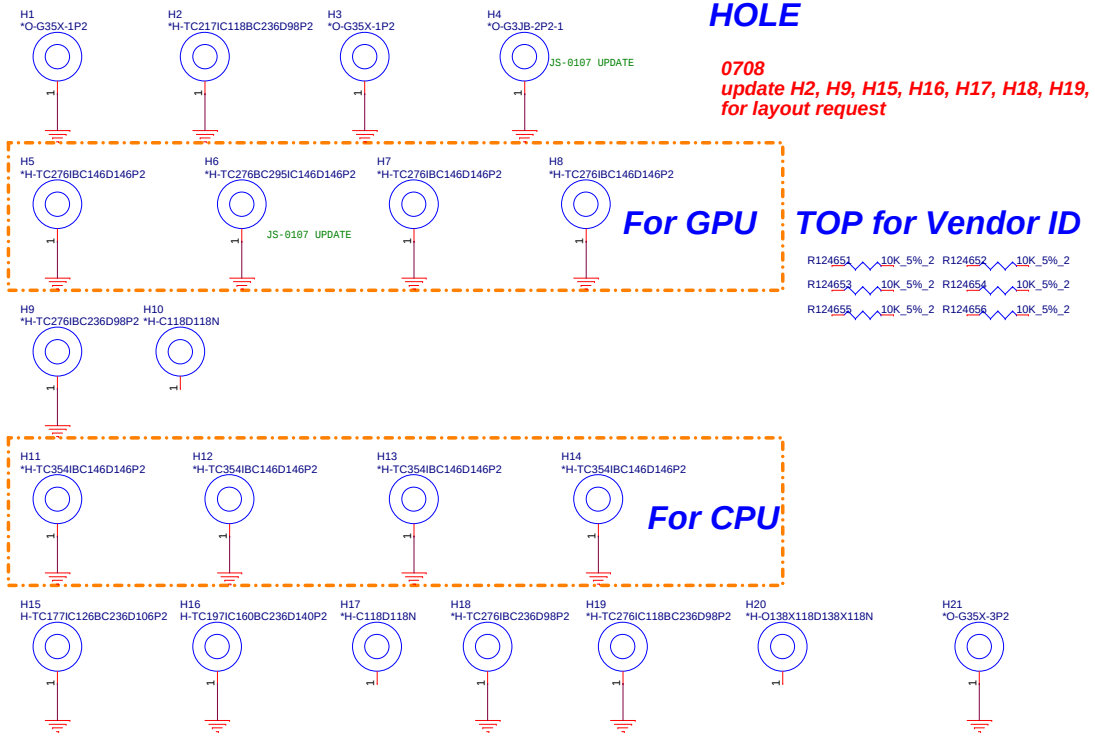


Touch Pad Connector



HOLE

0708
update H2, H9, H15, H16, H17, H18, H19, H20 for layout request



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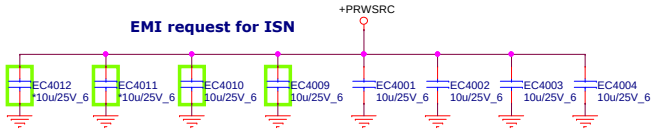

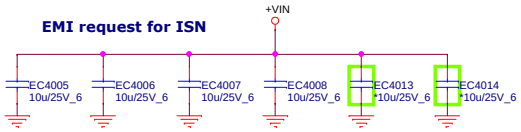

NB5

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Quanta Computer Inc.

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+3VPCU 5,10,31,33,34,38,39,44,48,58,59
+5VPCU 29,44,46,52,57
+PRWSRC 42
+BAT_RTC 10,12,14,31,59

150W/19.5V/7.6A

CN1001
51280-01201-V01

PQ1004 AONS32310 SI updated 11/20
PQ1003 AONS32310
PQ1002 AONS32314
PQ1001 AONS32314

Place this ZVS close to Diode away DC jack

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

15.6"

PU1001 BQ24738HRGRR

Place this R&C close to EC

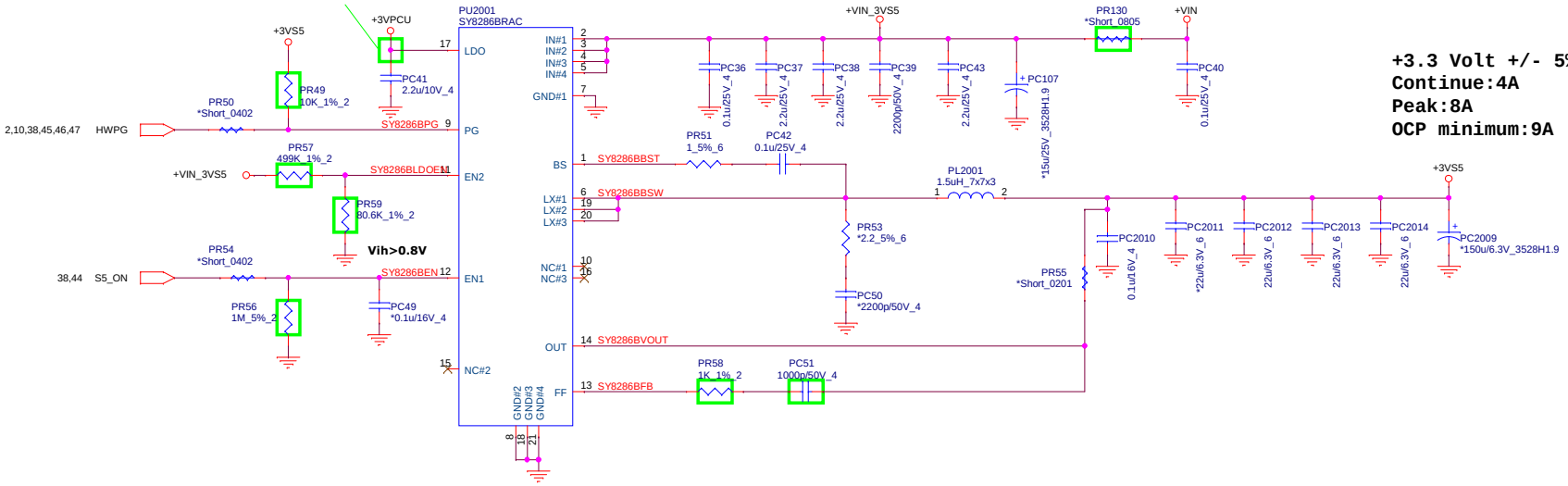
Setting MAX Icharge to 5A

https://realschematic.com

PROJECT :G3JB
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Charger (BQ24738H) | Rev: 1A
Date: Monday, April 20, 2020 | Sheet: 43of 59

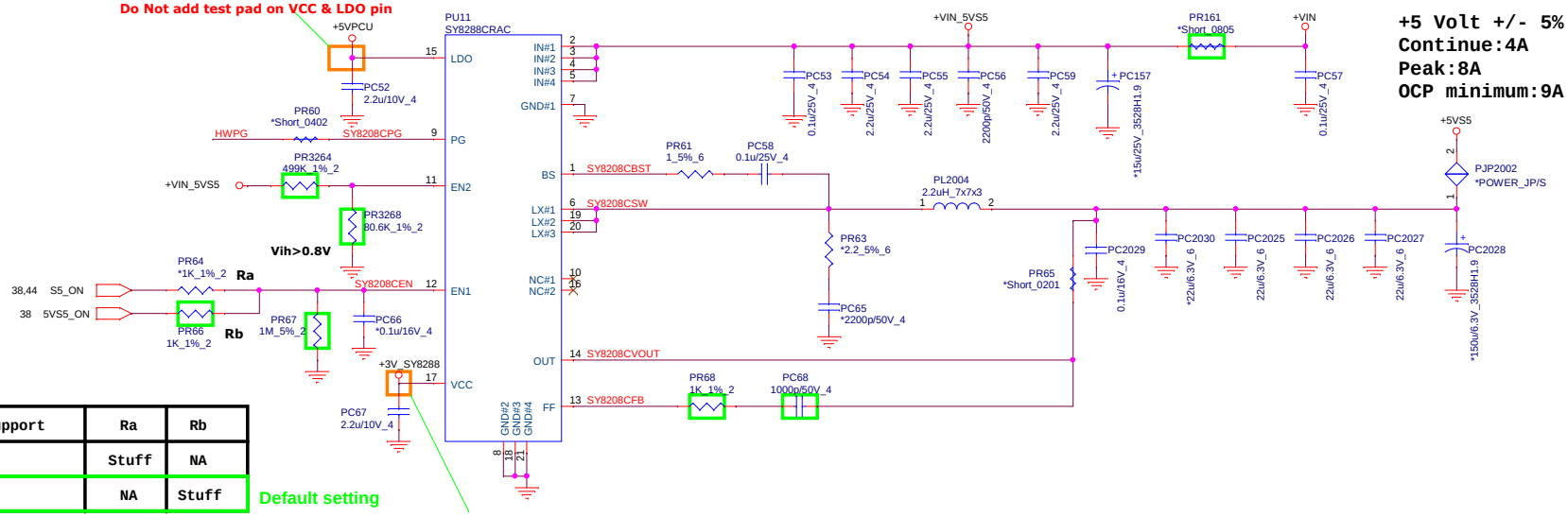
+VIN 27,40,41,42,43,45,46,47,49,51,54,56
+3VS5 10,12,14,23,31,32,33,34,38,41,45,46,47,48,52,57,58
+5VS5 10,31,33,41,45,46,47,52,53,56,57
+3VPCU 5,10,31,33,34,38,39,43,48,58,59
+5VPCU 29,43,46,52,57

Do Not add test pad on LDO pin



+3.3 Volt +/- 5%
Continue:4A
Peak:8A
OCP minimum:9A

Do Not add test pad on VCC & LDO pin



+5 Volt +/- 5%
Continue:4A
Peak:8A
OCP minimum:9A

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Default setting

Do Not add test pad on VCC & LDO pin

Link H/W prochot circuit

3VCC is to make use of internal driver 10mA maximum when heavy loading (internal current limit is 15mA typ.)

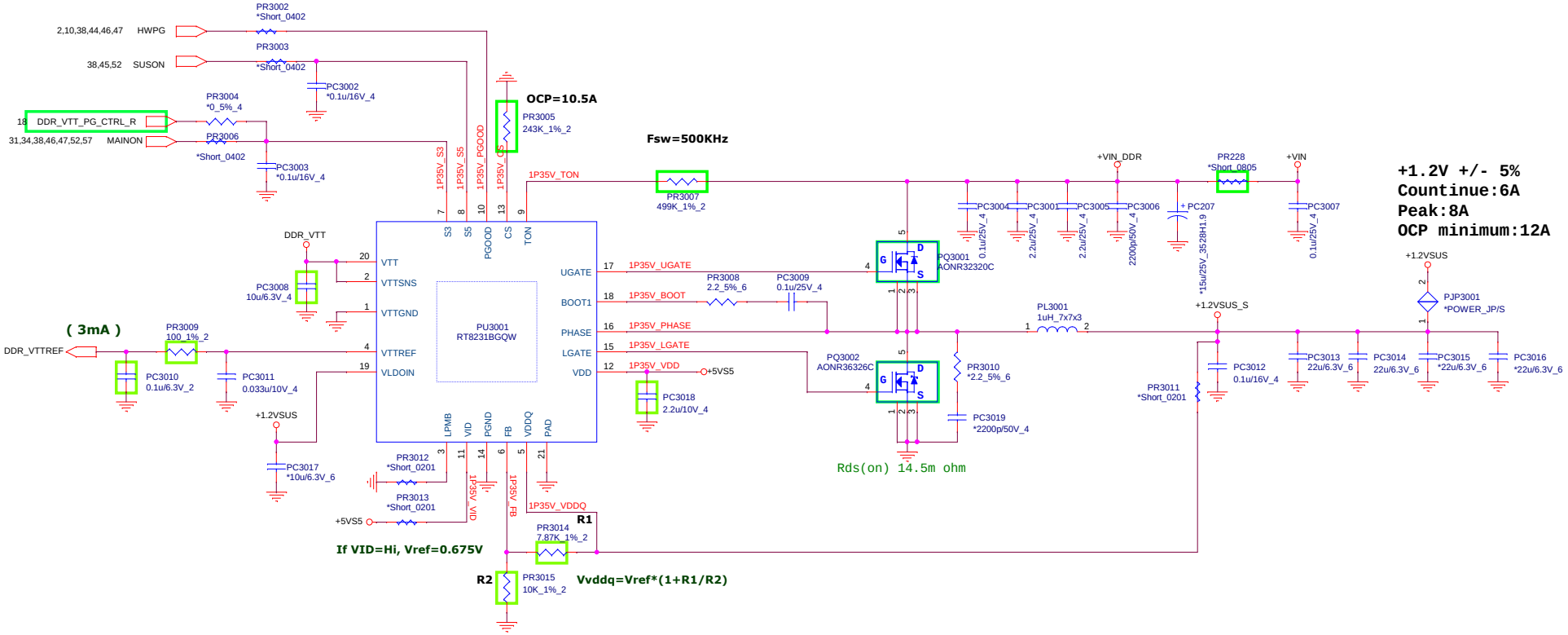
NB5

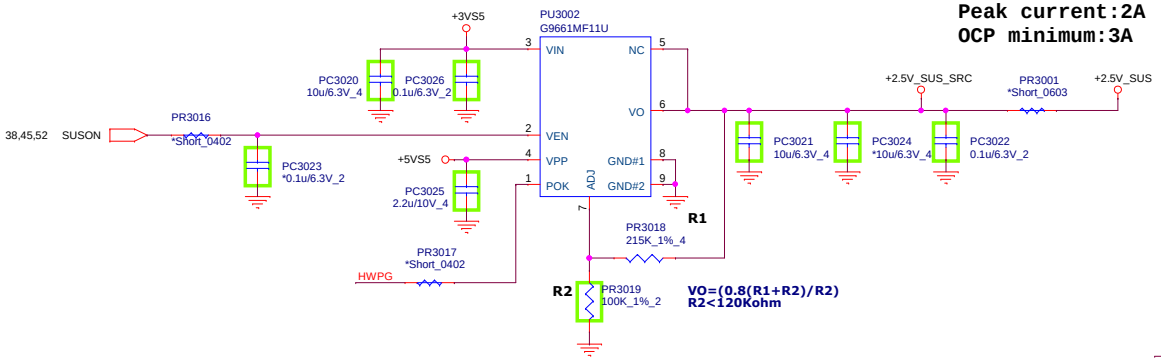
PROJECT :G3JB

Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A

Date: Monday, April 20, 2020 Sheet 44 of 59





+VIN 27,40,41,42,43,44,46,47,49,51,54,56
+5VS5 10,31,33,41,44,46,47,52,53,56,57
+1.2VSUS 2,6,10,17,18,47
DDR_VTT 17,18
+2.5V_SUS 17,18

NB5

PROJECT :G3JB

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR4 (RT8231B)	1A
Date: Monday, April 20, 2020	Sheet 45of 59	

+VIN 27,40,41,42,43,44,45,47,49,51,54,56
+3VS5 10,12,14,23,31,32,33,34,38,41,44,45,47,48,52,57,58
+5VS5 10,31,33,41,44,45,47,52,53,56,57
+1.05V_DEEP_SUS 10,14,47
+1.8V_DEEP_SUS 9,10,12,13,14,31,34,38,57
+1.8V 21,22,29
+1.05V 2,6,10,57

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Continue:8A
Peak:10.32A
OCP minimum:12A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

PU501 AOZ2261AQI-18
PR505 84.5K_1%_2
PR512 5.1_1%_6
PC521 4.7u/6.3V_4
PC502 0.1u/25V_4
PC503 2.2u/25V_4
PC504 2.2u/25V_4
PC507 *15u/25V_3528H1.9
PC505 2200p/50V_4
PR513 *Short_0805
PC506 0.1u/25V_4
PR506 1_5%_6
PC522 0.1u/25V_4
PL501 1.5uH_7x7x3
7x7x3mm
PR501 *2.2_5%_6
PC501 *2200p/50V_4
PR502 *Short_0201
PC511 0.1u/6.3V_2
PC512 22u/6.3V_6
PC513 22u/6.3V_6
PC514 22u/6.3V_6
PC515 22u/6.3V_6
PC516 *150u/6.3V_3528H1.9
PR507 *Short_0402
PR508 100K_1%_2
PC523 *0.1u/6.3V_2
PR509 *Short_0402
PC524 0.1u/25V_4
PR510 3.16K_1%_2
PR511 10K_1%_2
R1
Vout1=(1+R1/R2)*0.8

	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL	3.16K	CS23162FB04	1.05V

Volume Segment
+VCCSTPLL: 0.06A
Vcc_STG: 0.02A
Vcc_PLL: 0.15A
<= 65us, full load ready
(Vcc_ST+Vcc_PLL)

PU500 74AHCT1G08GW
PC597 0.1u/6.3V_2
PR558 *0_5%_2
PR559 866_1%_4
PQ500 DMG3414U-7
PR564 *Short_0402
PR563 *0_5%_4
PC596 0.1u/16V_4
PC595 0.1u/6.3V_2
PC592 *10u/6.3V_4
PC593 *0.1u/6.3V_2
PC598 22u/6.3V_6
PC570 0.1u/6.3V_2
PC591 0.1u/6.3V_2
PU552 AOZ1331ADI
PR561 *0_5%_4
PC576 0.1u/16V_4
PC577 *0.1u/6.3V_2
PC594 0.1u/6.3V_2
PC575 *10u/6.3V_4
PR562 *Short_0402
PC578 *0.1u/6.3V_2
PR560 *Short_0603_R
PC579 *1000p/25V_2
PC580 1000p/25V_2
0.5A
0.5A

SI updated 11/15

PR575 1M_5%_4
PR573 22_5%_8
PR574 2M_1%_4
PQ501A 2N7002KDW
PQ501B 2N7002KDW

PU551 G2823D
PC551 *2200p/25V_2
PR551 *2.2_5%_6
PR565 *Short_0402
PR571 *Short_0603
PR572 10_1%_6
PC572 0.01u/50V_4
PC571 10u/6.3V_4
PC590 1u/6.3V_4
PL551 1uH_2.5x2.0x1.2
PC574 *22p/50V_4
PC573 *68p/50V_4
PR568 20K_1%_2
PC581 *0.1u/6.3V_2
PR566 *Short_0402
PR567 10K_1%_2
R1
R2
V0=0.6*(R1+R2)/R2

1.8VS5 +/- 3%
TDC:3A
EDP:4A

PR569 *Short_0201
PC561 0.1u/6.3V_2
PC562 22u/6.3V_6
PC563 *10u/6.3V_4
PR570 *Short_0603

https://realschematic.com

NB5
PROJECT :G3JB
Quanta Computer Inc.
Size Custom | Document Number +1V_DEEP_SUS/1.8V(AOZ2261) | Rev 1A
Date: Monday, April 20, 2020 | Sheet 46 of 59

Volume Segment

SKY/KBY-U22/U42/U23e
Vcc_IO: 3.4A/1V
Stuff PU601

Volume Segment

SKY/KBY-H 22/42/44e
Vcc_IO: 5.5A/0.95V
Stuff PU601 & merge 1V_deep_sus

Volume Segment

CNL U22
Vcc_IO: 5.1A/0.95V
Vcc_IO: Can merge +1.05V_deep_sus
Unstuff PU603
Unstuff PU601

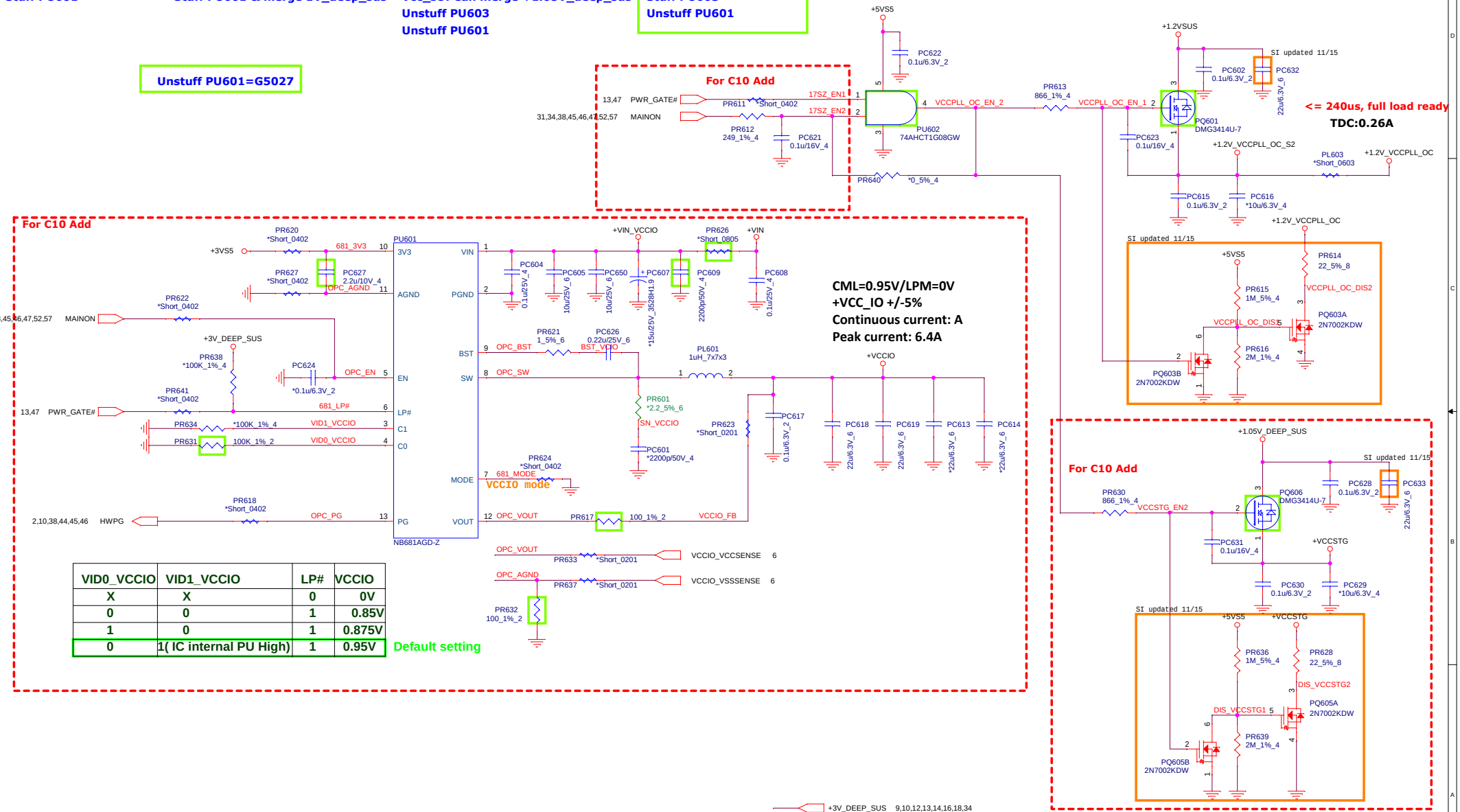
Default setting

Volume Segment

CML H6/H4
Vcc_IO: 6.4A/0.95V
Stuff PU603
Unstuff PU601

Unstuff PU601=G5027

C10: turn off VCCPLL_OC , VCCIO , VCCSTG



+3V_DEEP_SUS 9,10,12,13,14,16,18,34
+VCCSTG 2,6,38
+3VS5 10,12,14,23,31,32,33,34,38,41,44,45,46,48,52,57,58
+5VS5 10,31,33,41,44,45,46,52,53,56,57
+VCCIO 3,6
+1.05V_DEEP_SUS 10,14,46
+1.2V_VCCPLL_OC 6
+1.2VSUS 2,6,10,17,18,45
+VIN 27,40,41,42,43,44,45,46,49,51,54,56

PROJECT :G3JB
Quanta Computer Inc.
NB5
Size: Custom | Document Number: +1.0V/+VCCSTPLL/+VCCIO | Rev: 1A
Date: Monday, April 20, 2020 | Sheet 47 of 59

CFL change
PMBUS(Connect to EC)

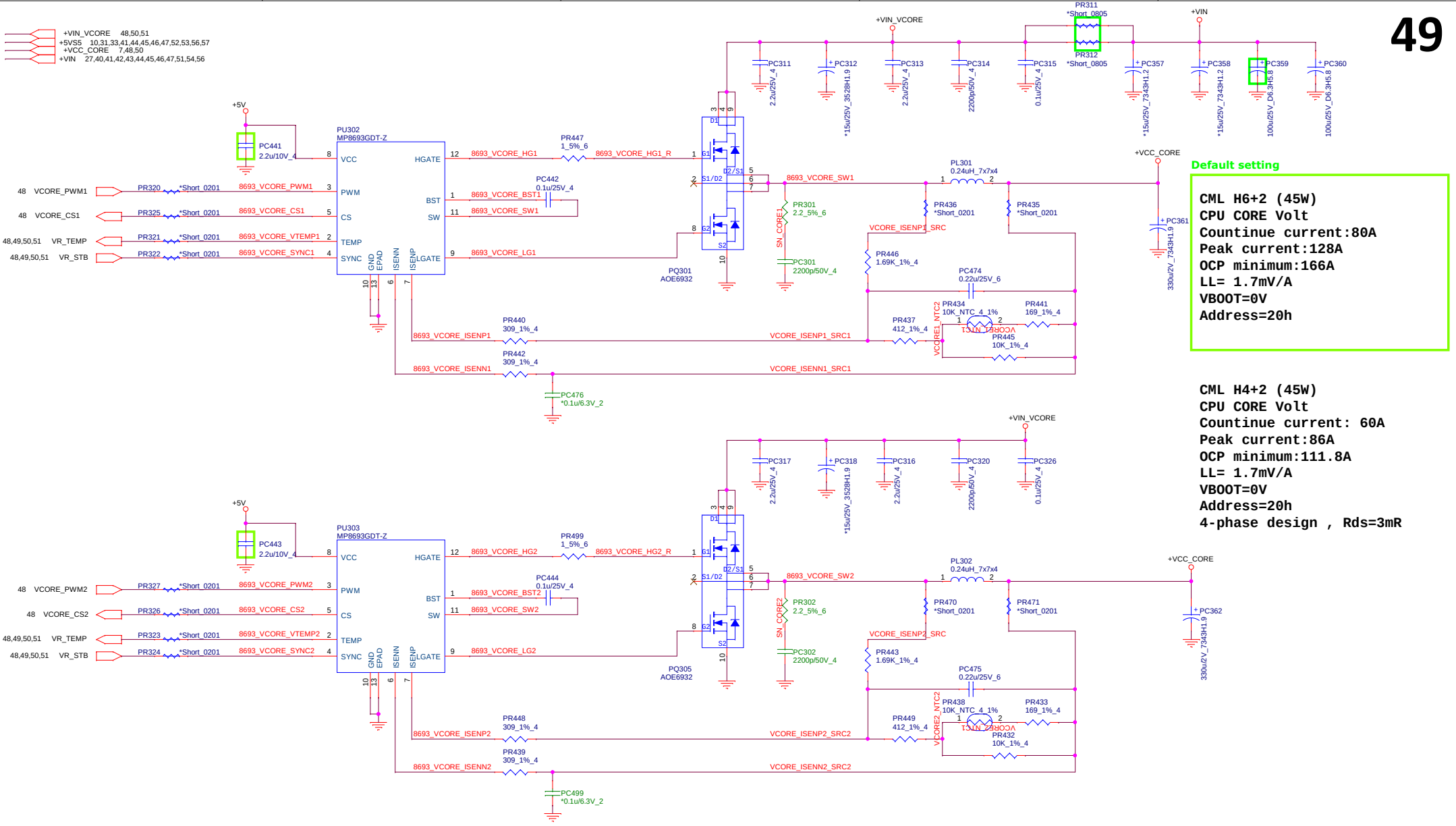
Connect to PCH, for saving mode, Pull high-->no used

PM BUS Address=20h

To EC pin77

CPU Design	P/N	Vender P/N	
4+1+1 (CORE,GT,Dr.MOS)=4+1+1	AL002949041	MP2949AGQKT-0290-Z	Default setting
3+2+1 (CORE,GT,SA)=3+2+1	AL002949019	MP2949AGQKT-0099-Z	
4+1+1 (CORE,GT,Dr+MOS)=4+1+1	AL002949032	MP2949AGQKT-0199-Z	

PROJECT :G3JB
Quanta Computer Inc.
NB5
Size | Document Number: DDR3 (MP2949AGQKT-0098-Z) | Rev: 1A
Monday, April 20, 2020 | Sheet 48 of 59



Default setting

```
CML H6+2 (45W)
CPU CORE Volt
Countinue current:80A
Peak current:128A
OCP minimum:166A
LL= 1.7mV/A
VBOOT=0V
Address=20h
```

```
CML H4+2 (45W)
CPU CORE Volt
Countinue current: 60A
Peak current:86A
OCP minimum:111.8A
LL= 1.7mV/A
VBOOT=0V
Address=20h
4-phase design , Rds=3mR
```

	ALL POWER CLIP		Cout	
CFL H6+2	4 phase BAM69320002 ; AOE6932 ;1.8mR		2PCS 330u/7343	Default setting
CFL H4+2	4 phase BAM69360000 ; AOE6936 ;3mR		2PCS 330u/7343	

PROJECT :G3JB

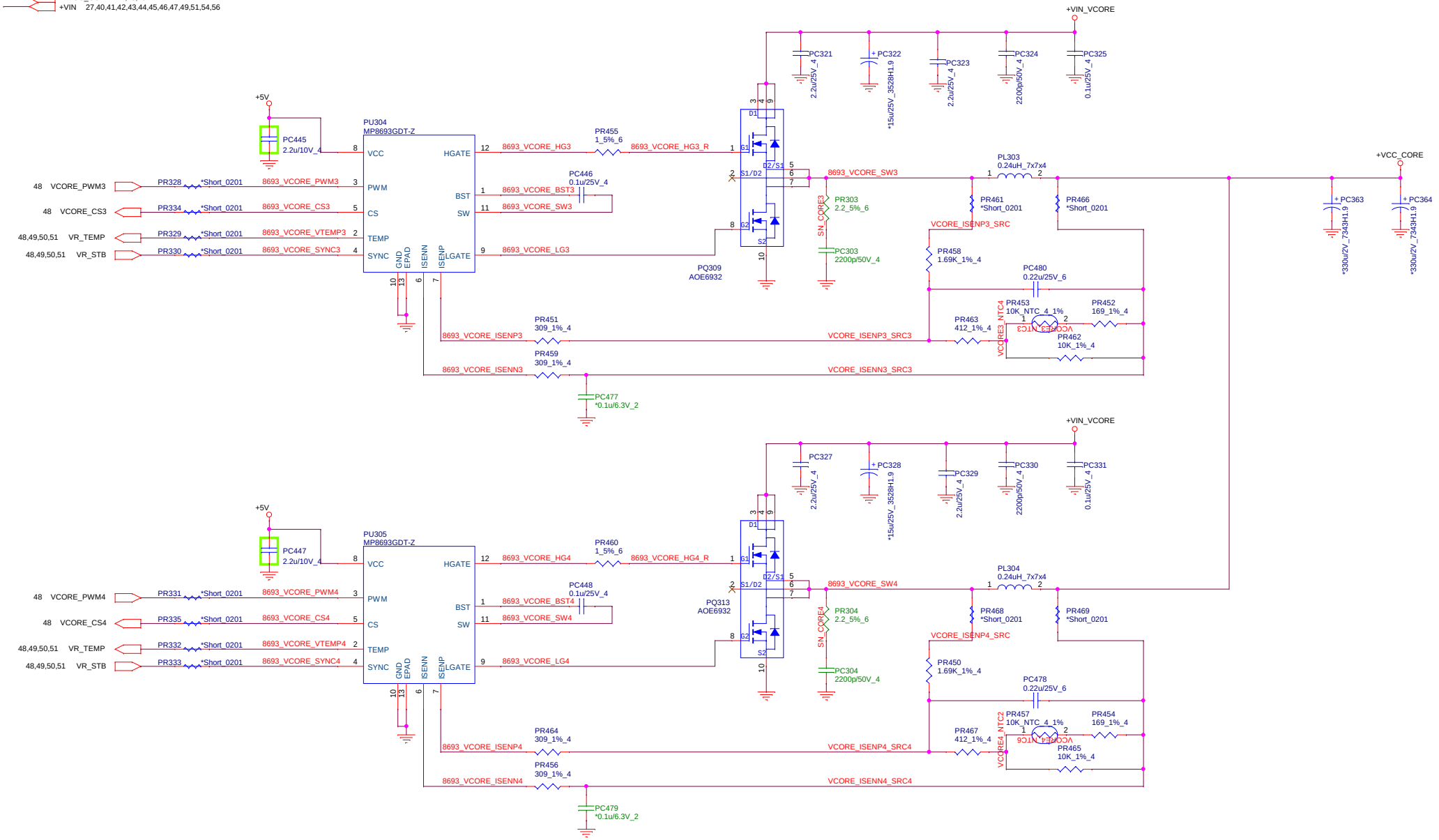
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	85 -- +VCC_CORE (MP86903-C)	1A

Date: Monday, April 20, 2020 Sheet 49 of 59

+VIN_VCORE 48,49,51
+5VS5 10,31,33,41,44,45,46,47,52,53,56,57
+VCC_CORE 7,48,49
+VIN 27,40,41,42,43,44,45,46,47,49,51,54,56



NB5

PROJECT :G3JB

Quanta Computer Inc.

Size	Document Number	Rev
Custom	85 -- +VCC_CORE (MP86903-C)	1A
Date: Monday, April 20, 2020	Sheet 50 of 59	

+VCCSA 6,48
+5VS5 10,31,33,41,44,45,46,47,52,53,56,57
+3VS5 10,12,14,23,31,32,33,34,38,41,44,45,46,47,48,52,57,58
+VCCGT 5,48
+VIN 27,40,41,42,43,44,45,46,47,49,54,56
+VIN_VCORE 48,49,50

+VIN_GT
PR313 *Short_0805
+VIN

PC381 2.2u/25V_4
PC382 *15u/25V_3528H1.9
PC383 2.2u/25V_4
PC384 2200p/50V_4
PC385 0.1u/25V_4

+5V
PC453 2.2u/10V_4

PU308
MP8693GDT-Z

48 GT_PWM5 — PR345 *Short_0201 — 8693_GT_PWM1 — PWM
48 VCCGT_CS1 — PR354 *Short_0201 — 8693_GT_CS1 — CS
48,49,50,51 VR_TEMP — PR346 *Short_0201 — 8693_GT_VTEMP1 — TEMP
48,49,50,51 VR_STB — PR347 *Short_0201 — 8693_GT_SYNC1 — SYNC

VCC, HGATE, BST, SW, LGATE, GND, EPAD, ISENN, ISENP

8693_GT_HG1 — PR348 1_5%_6 — 8693_GT_HG1_R
PC454 0.1u/25V_4
8693_GT_BST1
8693_GT_SW1
8693_GT_LG1

PQ317 AOE6932
D1, D2/S1, S1/D2, G1, G2, S2

8693_GT_SW1
PR307 2.2_5%_6
SN_GT
PC307 2200p/50V_4

PL307 0.24uH_7x7x4
PR490 *Short_0201
PR489 *Short_0201
+VCCGT
PC401 330u/2V_7343H1.9
PC402 *330u/2V_7343H1.9

GT_ISENP1_SRC
PR355 1.69K_1%_4
PC456 0.22u/25V_6
PR486 10K_NTC_4_1%
PR485 169_1%_4
PR487 412_1%_4
GT_NTC2
GT_VIN
PR484 10K_1%_4

8693_GT_ISENP1 — PR349 309_1%_4 — GT_ISENP1_SRC1
8693_GT_ISENN1 — PR350 309_1%_4 — GT_ISENN1_SRC1
PC455 0.1u/6.3V_2

Rdson=1.05mohm max

CFL H6+2/H4+2 (45W)
GT Volt
Countinue current: 25A
Peak current:32A
OCP minimum:41.6A
LL= 2.7mV/A
VBOOT=0V
Address=01h

+VIN_SA
PR314 *Short_0805
+VIN_VCORE

PC421 2.2u/25V_4
PC422 *15u/25V_3528H1.9
PC423 2.2u/25V_4
PC424 2200p/50V_4
PC425 0.1u/25V_4

+5V
PC457 2.2u/10V_4

PU401
MP8693GDT-Z

48 VCCSA_PWM6 — PR351 *Short_0201 — 8693_VCCSA_PWM — PWM
48 VCCSA_CS1 — PR353 *Short_0201 — 8693_VCCSA_CS — CS
48,49,50,51 VR_TEMP — PR356 *Short_0201 — 8693_VCCSA_VTEMP — TEMP
48,49,50,51 VR_STB — PR352 *Short_0201 — 8693_VCCSA_SYNC — SYNC

VCC, HGATE, BST, SW, LGATE, GND, EPAD, ISENN, ISENP

8693_SA_HG1 — PR480 1_5%_6 — 8693_SA_HG1_R
PC482 0.1u/25V_4
SA_BST
8693_SA_SW1
8693_SA_LG1

PQ321 AONY36356
D1, S1/D2, G1, G2, S2

8693_SA_SW1
PR309 2.2_5%_6
SN_SA1
PC309 2200p/50V_4

PL401 0.68uH_7x7x3
PR482 *Short_0201
PR473 *Short_0201
+VCCSA
PC430 22u/6.3V_6
PC431 22u/6.3V_6
PC432 *22u/6.3V_6
PC433 *22u/6.3V_6

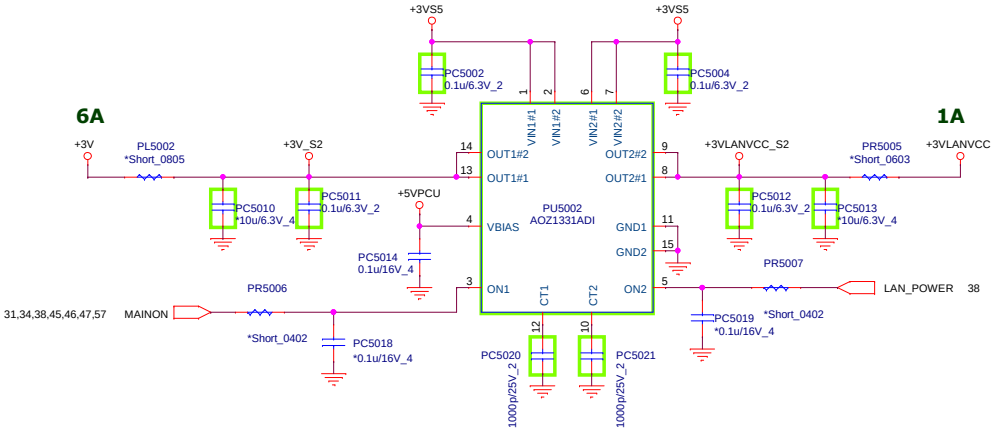
SA_ISENP1_SRC
PR481 1.91K_1%_4
PC483 0.1u/25V_6
PR477 10K_NTC_4_1%
PR475 1.69K_1%_4
PR472 715_1%_4
SA_NTC2
SA_VIN
PR476 12K_1%_4

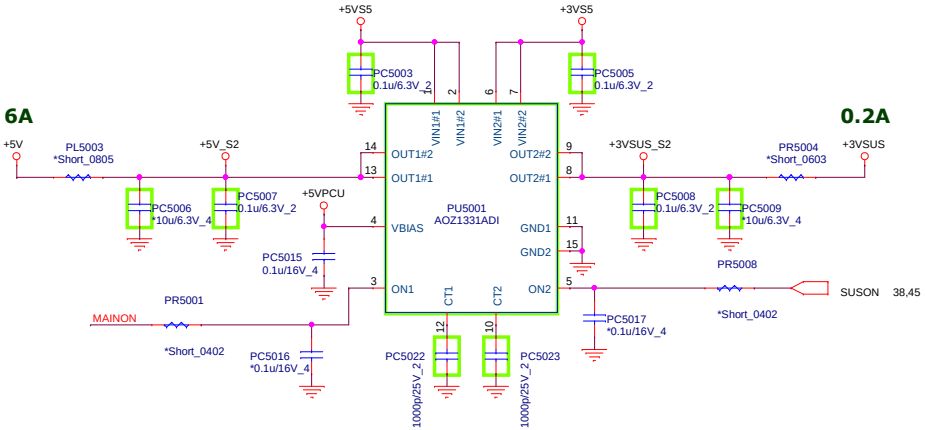
8693_SA_ISENP1 — PR479 1.69K_1%_4 — SA_ISENP1_SRC1
8693_SA_ISENN1 — PR478 1.69K_1%_4 — SA_ISENN1_SRC1
PC481 *0.1u/6.3V_2

CFL H6+2/H4+2 (45W)
VCCSA Volt
Countinue current: 10A
Peak current:11.1A
OCP minimum:16A
LL= 11.4mV/A
VBOOT=1.05V
Address=02h

NB5	PROJECT :G3JB Quanta Computer Inc.	
	Size: Custom — Document Number: 86 -- +VCC_GT/+VCC_SA	Rev: 1A
	Date: Monday, April 20, 2020 — Sheet 51 of 59	

+3V 9,10,11,13,16,17,18,21,27,29,32,34,35,36,37,38,40,41,48,53,54,55,56,57
+5V 27,28,29,32,35,40,49,50,51,58
+3VS5 10,12,14,23,31,32,33,34,38,41,44,45,46,47,48,57,58
+5VS5 10,31,33,41,44,45,46,47,53,56,57
+3VSUS 41
+3VLANVCC 36
+5V_CAM
+3V_DEEP_SUS 9,10,12,13,14,16,18,34,47



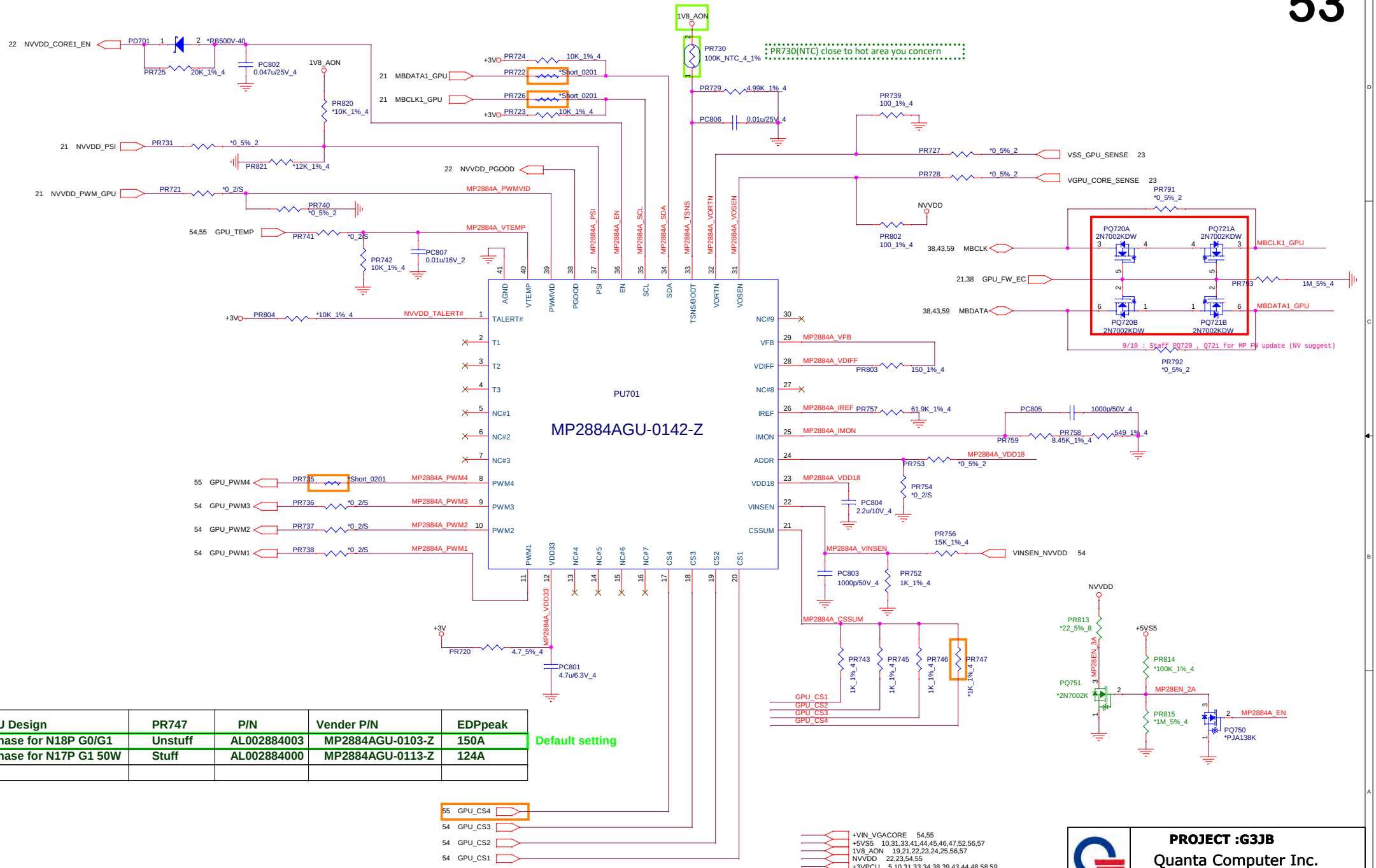


NB5

PROJECT :G3JB

Quanta Computer Inc.

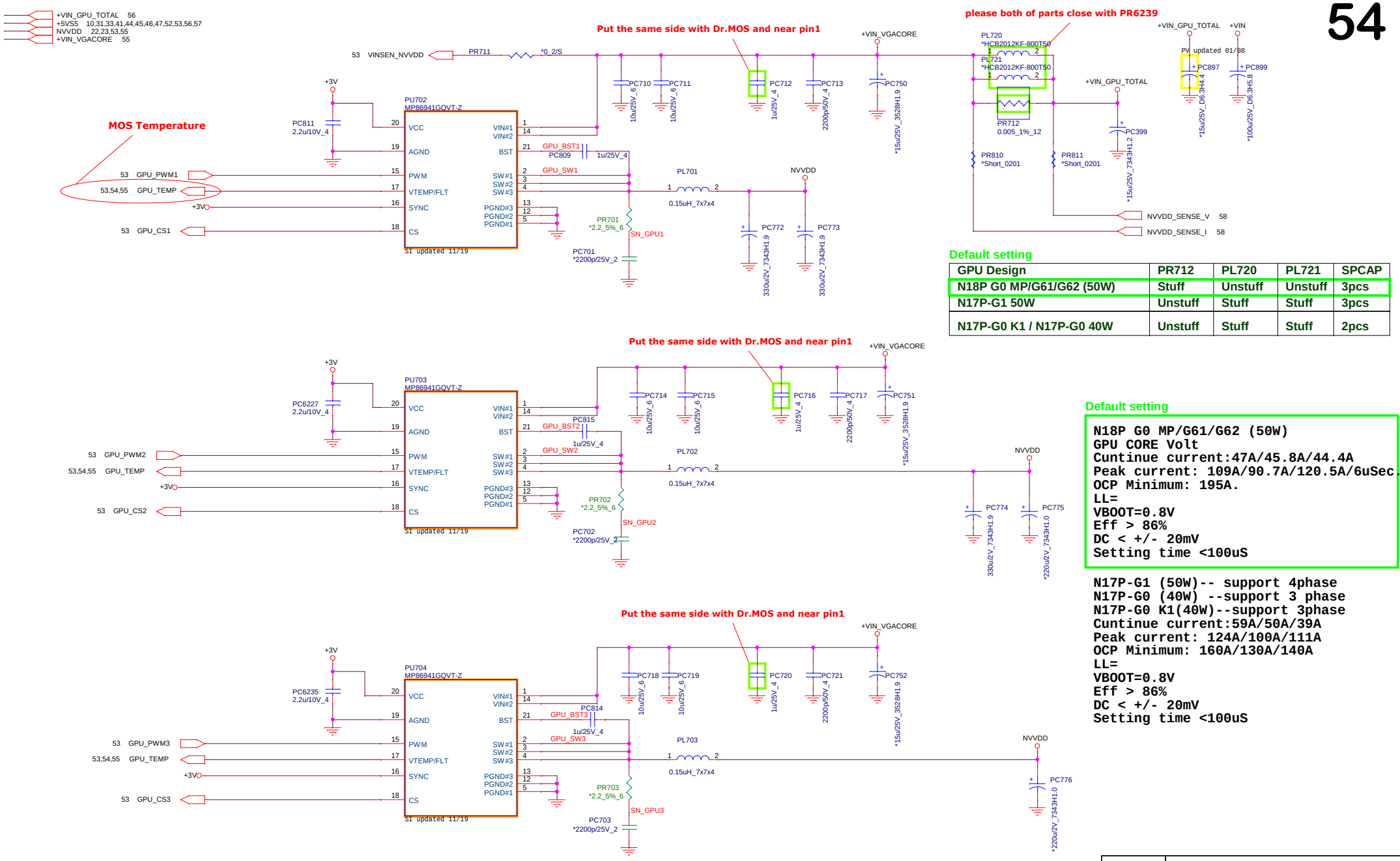
Size	Document Number	Rev
Custom	Load switch IC (AOZ1331D)	1A
Date: Monday, April 20, 2020	Sheet 52of 59	



GPU Design	PR747	P/N	Vender P/N	EDPpeak
3 Phase for N18P G0/G1	Unstuff	AL002884003	MP2884AGU-0103-Z	150A
4 Phase for N17P G1 50W	Stuff	AL002884000	MP2884AGU-0113-Z	124A

Default setting

NB5	PROJECT :G3JB		
	Quanta Computer Inc.		
	Size: Custom	Document Number: +VGACORE (MP2884AGU)	Rev: 1A
	Date: Monday, April 20, 2020	Sheet 53of 59	



Default setting

GPU Design	PR712	PL720	PL721	SPCAP
N18P G0 MP/G61/G62 (50W)	Stuff	Unstuff	Unstuff	3pcs
N17P-G1 50W	Unstuff	Stuff	Stuff	3pcs
N17P-G0 K1 / N17P-G0 40W	Unstuff	Stuff	Stuff	2pcs

Default setting

```
N18P G0 MP/G61/G62 (50W)
GPU CORE Volt
Cuntinue current:47A/45.8A/44.4A
Peak current: 109A/90.7A/120.5A/6uSec.
OCP Minimum: 195A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS
```

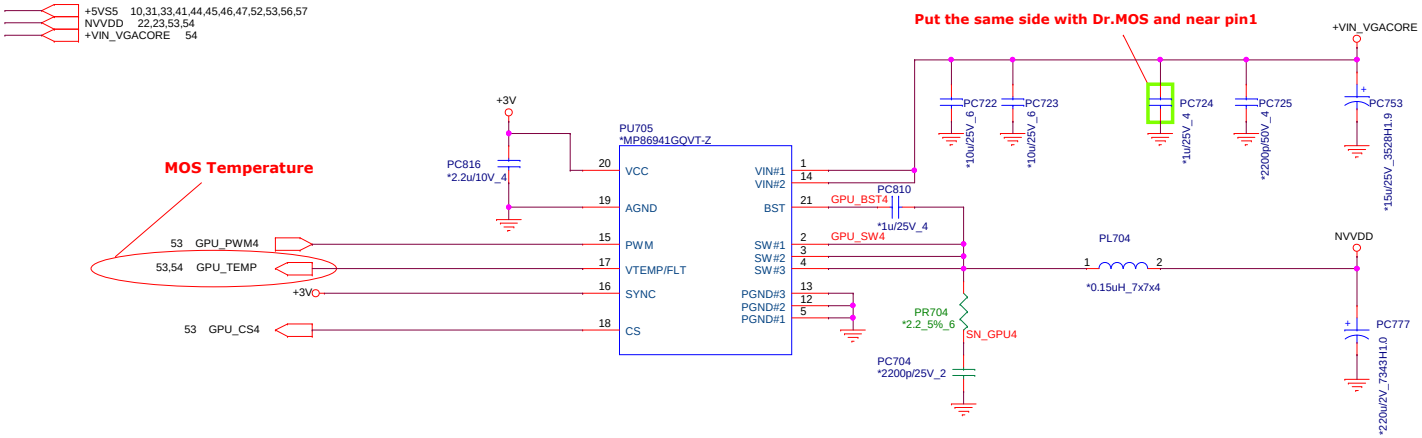
```
N17P-G1 (50W)-- support 4phase
N17P-G0 (40W) --support 3 phase
N17P-G0 K1(40W)--support 3phase
Cuntinue current:59A/50A/39A
Peak current: 124A/100A/111A
OCP Minimum: 160A/130A/140A
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS
```

NB5

PROJECT :G3JB

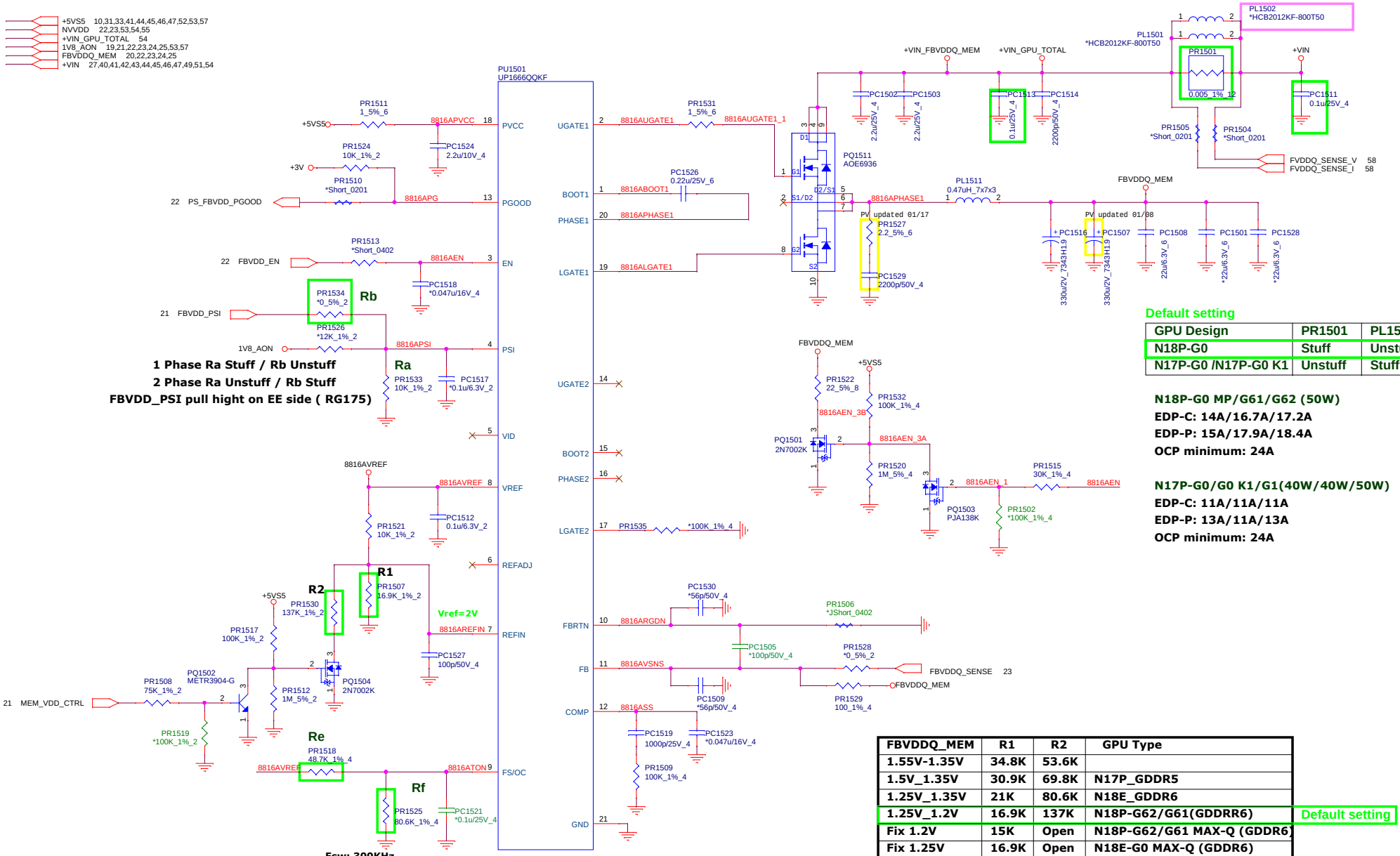
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE (NCP81151)	1A
Date: Monday, April 20, 2020	Sheet 54of 59	



NB5	PROJECT :G3JB Quanta Computer Inc.	
Size: Custom	Document Number: +VCORE (NCP81151)	Rev: 1A
Date: Monday, April 20, 2020	Sheet: 55of 59	

+5VS5 10,31,33,41,44,45,46,47,52,53,57
NVVDD 22,23,53,54,55
+VIN_GPU_TOTAL 54
1V8_AON 19,21,22,23,24,25,53,57
FBVDDQ_MEM 20,22,23,24,25
+VIN 27,40,41,42,43,44,45,46,47,49,51,54



1 Phase Ra Stuff / Rb Unstuff
2 Phase Ra Unstuff / Rb Stuff
FBVDD_PSI pull hight on EE side (RG175)

Fsw: 300KHz

	Ra	Re	Rf	OCP
N18P G0 1-Phase	Stuff	48.7K	80.6K	25A
N18E G0 2-Phase	Unstuff	47.5K	78.7K	48A

Default setting

Default setting

GPU Design	PR1501	PL1501	SPCAP
N18P-G0	Stuff	Unstuff	2pcs
N17P-G0 /N17P-G0 K1	Unstuff	Stuff	1pcs

N18P-G0 MP/G61/G62 (50W)
EDP-C: 14A/16.7A/17.2A
EDP-P: 15A/17.9A/18.4A
OCP minimum: 24A

N17P-G0/G0 K1/G1(40W/40W/50W)
EDP-C: 11A/11A/11A
EDP-P: 13A/11A/13A
OCP minimum: 24A

FBVDDQ_MEM	R1	R2	GPU Type	
1.55V-1.35V	34.8K	53.6K		
1.5V_1.35V	30.9K	69.8K	N17P_GDDR5	
1.25V_1.35V	21K	80.6K	N18E_GDDR6	
1.25V_1.2V	16.9K	137K	N18P-G62/G61(GDDRR6)	Default setting
Fix 1.2V	15K	Open	N18P-G62/G61 MAX-Q (GDDR6)	
Fix 1.25V	16.9K	Open	N18E-G0 MAX-Q (GDDR6)	
Fix 1.35V	21K	Open		
Fix 1.5V	30.1K	Open		

MEM_VDD_CTRL	FBVDDQ_MEM	MEM Type
1	1.25V	GDDR6
0	1.2V	
1	1.5V	GDDR5
0	1.35V	

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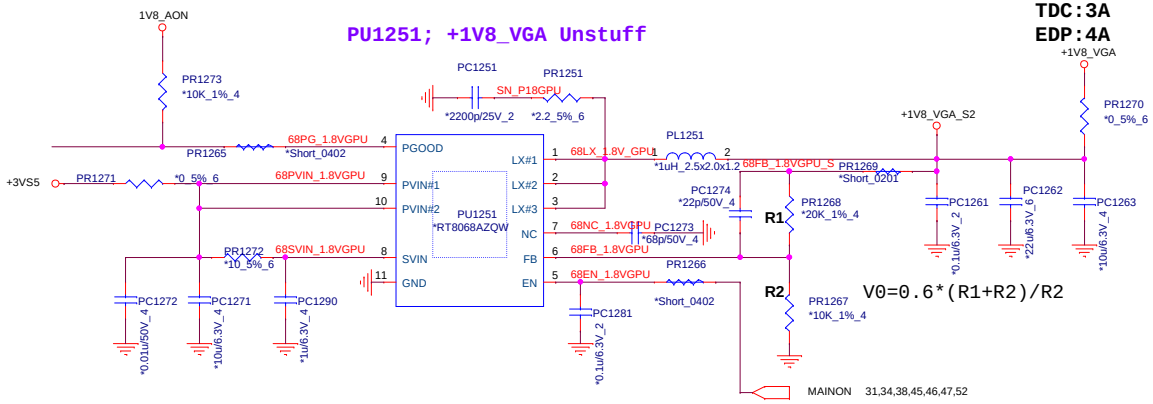
+VIN 27,40,41,42,43,44,45,46,47,49,51,54,56
+3VS5 10,12,14,23,31,32,33,34,38,41,44,45,46,47,48,52,58
+5VS5 10,31,33,41,44,45,46,47,52,53,56
1V8_MAIN 19,20,22,28
1V8_AON 19,21,22,23,24,25,53,56
+1.2VSUS 2,6,10,17,18,45,47
PEX_VDD 19,21

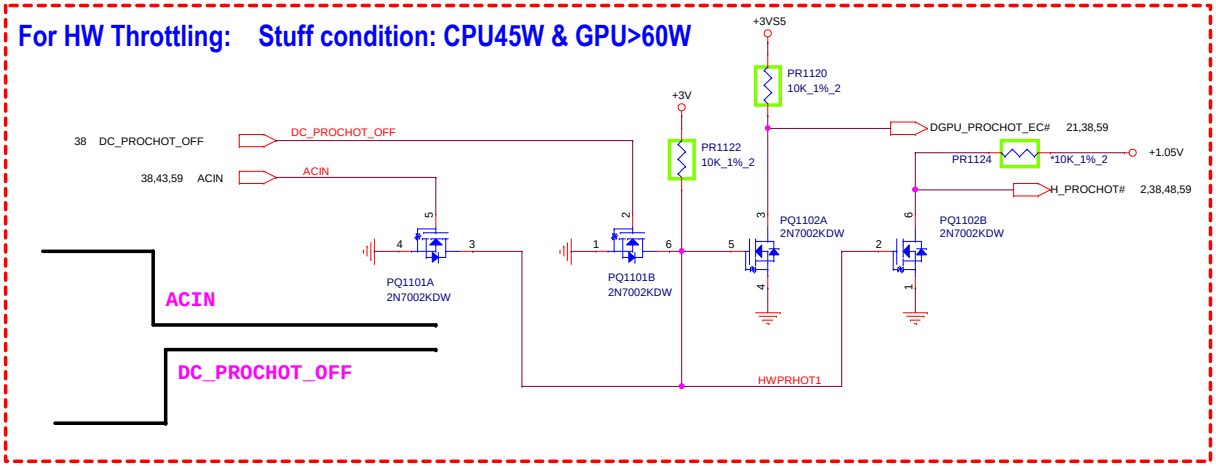
PU1251; +1V8_VGA Unstuff

1.8VS5 +/- 3%
TDC:3A
EDP:4A

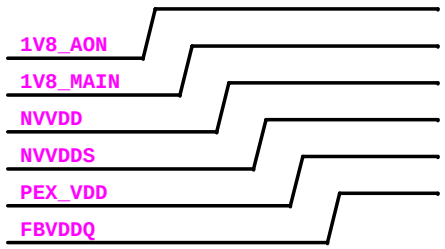


N18x

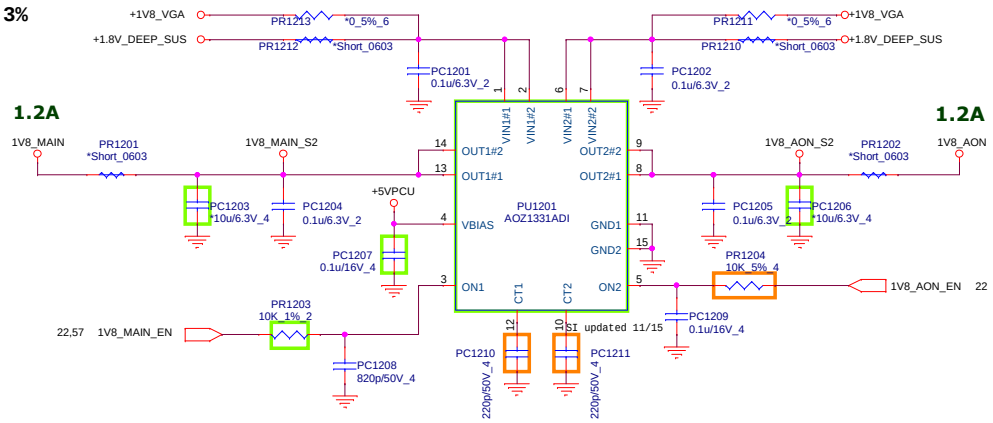
For HW Throttling: Stuff condition: CPU45W & GPU>60W



N17P G0/G1



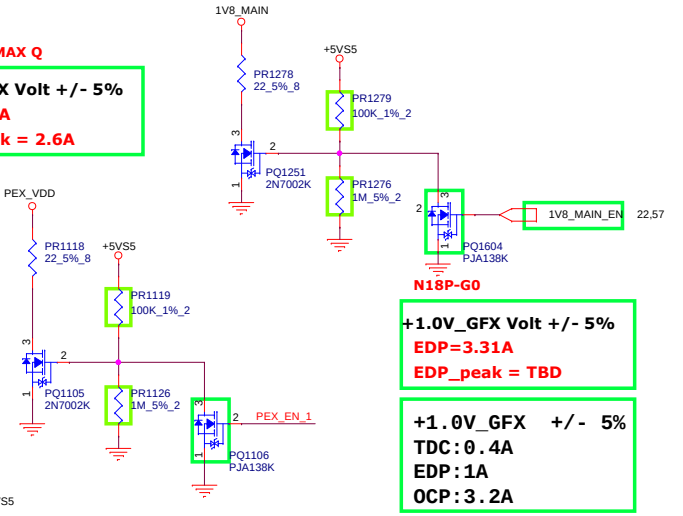
1.2A



1.2A

N18E-G0 MAX Q

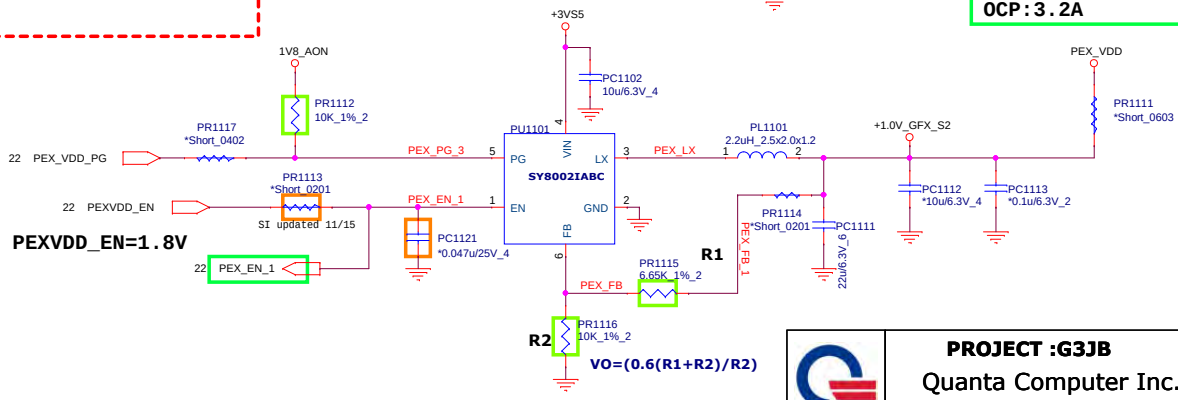
+1.0V_GFX Volt +/- 5%
EDP=2.2A
EDP_peak = 2.6A



N18P-G0

+1.0V_GFX Volt +/- 5%
EDP=3.31A
EDP_peak = TBD

+1.0V_GFX +/- 5%
TDC:0.4A
EDP:1A
OCP:3.2A



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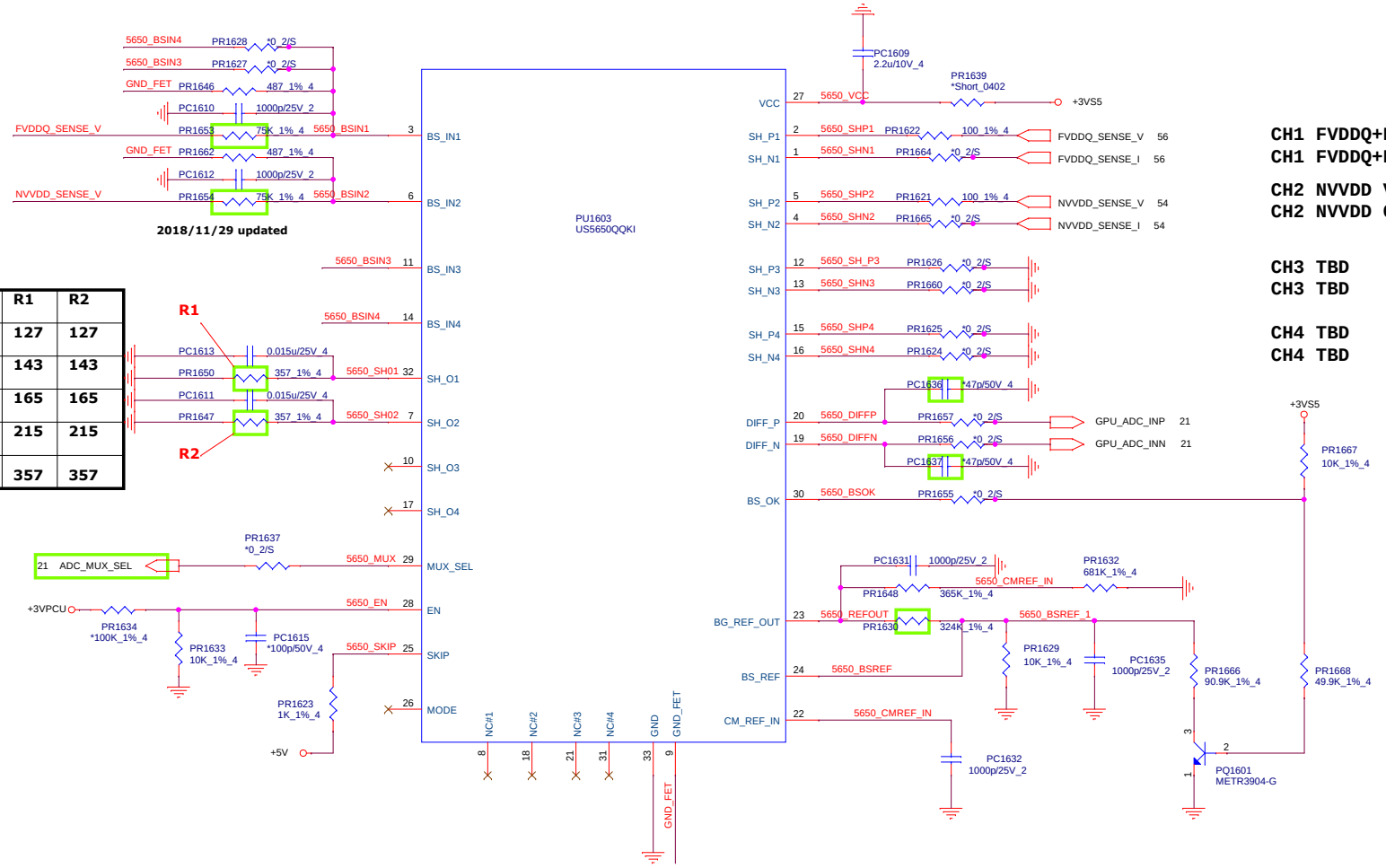
+3V 9,10,11,13,16,17,18,21,27,29,32,34,35,36,37,38,40,41,48,52,53,54,55,56,57

For N18P, N17P unstuff

UPI OVR Setting	R1	R2
N18E G3 (150W+)	127	127
N18E G2 (115W to 130W)	143	143
100W to 110W	165	165
N18E-G0,N18E-G1 (75W to 90W) N18E-G2 MaxQ,N18E-G3 MaXQ	215	215
N18P G0 N18P G0 MaxQ N18E G0 MaxQ (70W or Lower)	357	357



CH1 FVDDQ+NVDD VOLTAGE
CH1 FVDDQ+NVDD CURRENT

CH2 NVVDD VOLTAGE
CH2 NVVDD CURRENT

CH3 TBD
CH3 TBD

CH4 TBD
CH4 TBD

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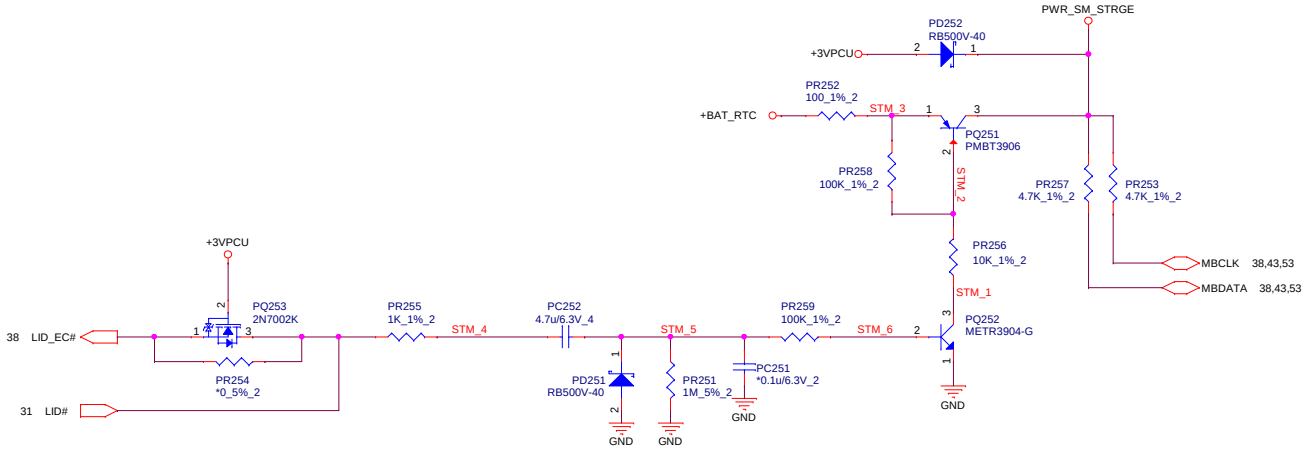
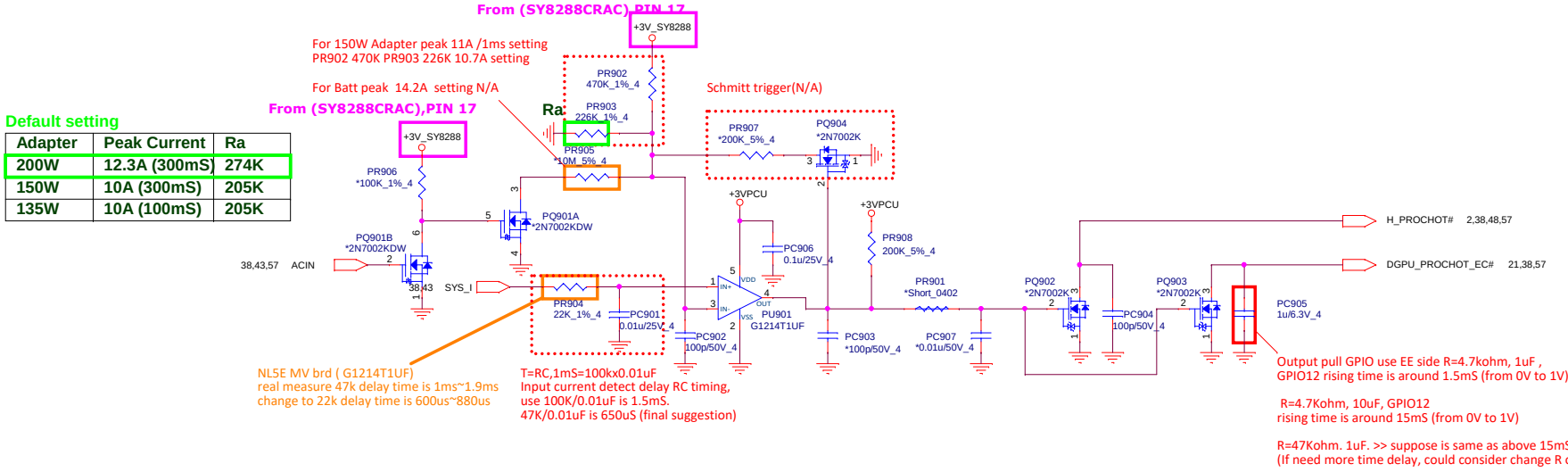
10,12,14,31,43 +BAT_RTC
5,10,31,33,34,38,39,43,44,48,58 +3VPCU





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