PCB Number:14050-1
ECO# number : 817473

BOM Configuration
(R_):Unmount
(C_):Carrizo
(L_):Carrizo-L
(G_):GPU
(H_):UMA
(T_):TOUCH
(D_):Debug used
(B_):Battery Charger
(P_):for non-pAIO and
W/O Battery Charger

PCB BOARD SIZE
6 Layers

185mm X 230mm

-1 BUILD

AMD Carrioz/-L Platform

LAN : Gb LAN RTL8111H

AUDIO: ALC3661

SIO_EC:ITE8739

<Core Design>

DELL

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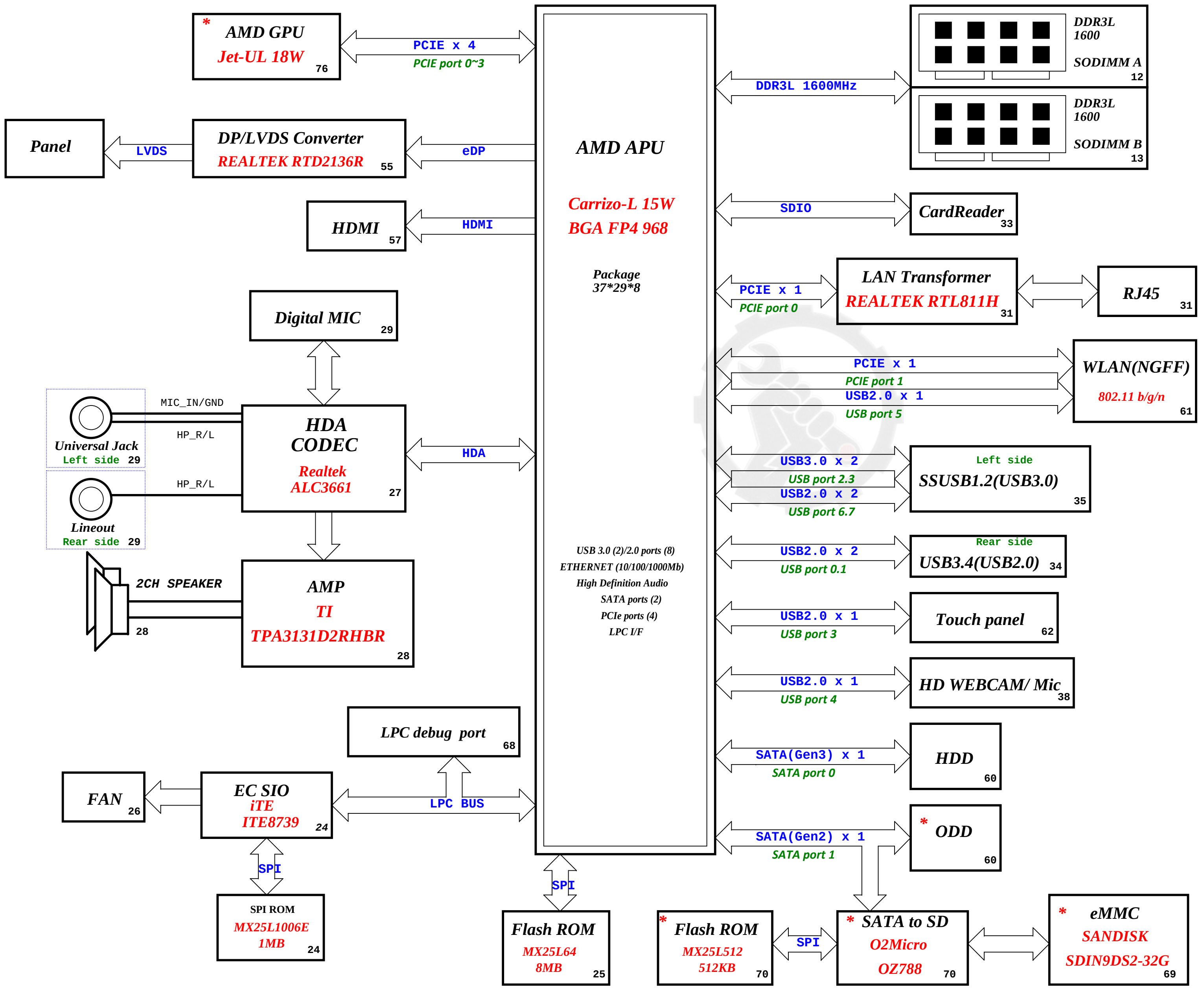
Title: ***001_Cover Page***		
Size: C	Document Number: **Rosa_Carrizo AIO**	Rev: **-1**
Date: Tuesday, August 09, 2016	Sheet 1 of 105	

Project Name: Orchid/Ontario Carrizo AIO
Project Code: 3PD02001000
PCB Version: 1
PCB Number :14050

AMD Carrizo-L Block Diagram



INPUTS	OUTPUTS	
AD+	DCBATOUT	42
CPU Core Power NCP81128MNTXG-GP		44,45
INPUTS	OUTPUTS	
DCBATOUT	CPU_VCORE VDDNB	
* **GFX Core Power** ISL62882CHRTZ-T-GP		83
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
SYSTEM DC/DC RT8243BZQW-GP		49
INPUTS	OUTPUTS	
DCBATOUT	V_3P3_A V_5P0_A	
DDR3L SUS RT8207MZQW-GP-U		50
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 V_0P675_S3	
CPU 0.95V RT8237CZQW-2-GP		48
INPUTS	OUTPUTS	
DCBATOUT	0D95V_S5	
SYSTEM DC/DC RT6220AGQUF-GP		51
INPUTS	OUTPUTS	
DCBATOUT	1D8V_S5	
System LDO 1.5V APL5930KAI-TRG-1-GP		52
INPUTS	OUTPUTS	
1D8V_S5	1D5V_S5	
***System LDO 0.775V** APL5337KAI-TRG-GP		47
INPUTS	OUTPUTS	
1D8V_S5	FCH_0.775_S5	
* **System LDO 1V** RT9025-25ZSP-1-GP		70
INPUTS	OUTPUTS	
VCC3	DVCC1_02	
System switchs		
INPUTS	OUTPUTS	
V_3P3_A	SB3V	
V_3P3_A	VCC3	
1D8V_S5	* 1D8V_VGA_S0	
V_5P0_A	SB5V	
V_5P0_A	VCC	
V_5P0_A	VCC5_USB	
VCC3	* 3D3V_VGA_S0	
1D8V_S5	1D8V_S0	
0D95V_S5	* 0D95V_VGA_S0	
0D95V_S5	0D95V_S0	

PCB LAYER

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: 002_Block Diagram
Size: C | Document Number: Rosa_Carrizo AIO | Rev: -1
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D C B A

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Title		
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Date: Tuesday, August 09, 2016	Sheet 3 of 105	

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Title		
Size: A	Document Number: **Rosa_Carrizo AIO**	Rev: **-1**
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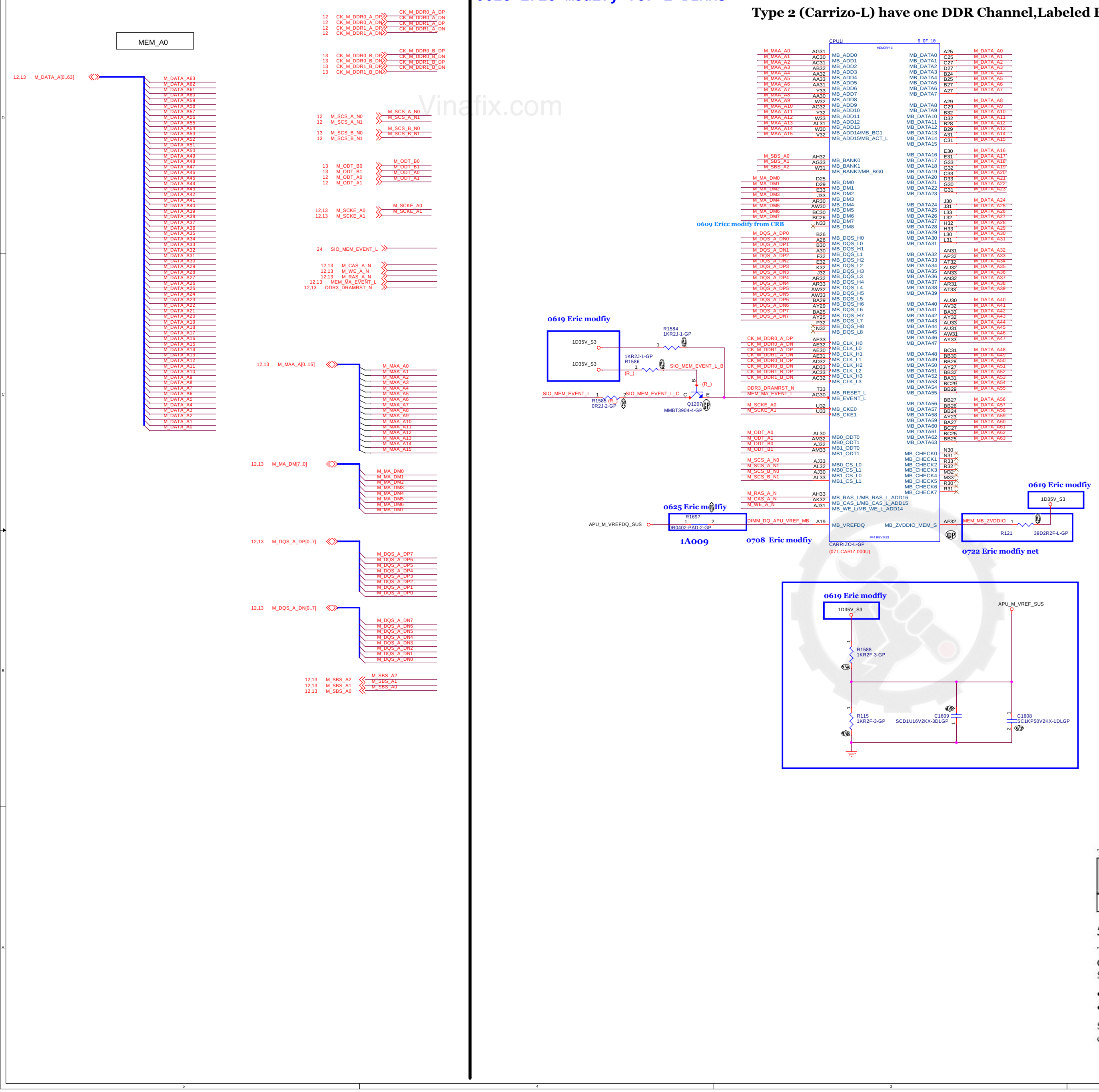
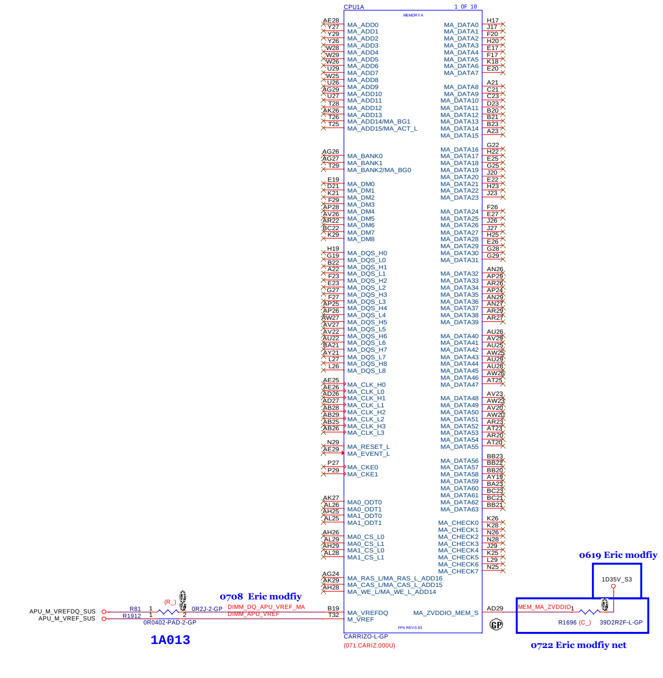
0625 Eric modify for 2 DIMMs

Type 2 (Carrizo-L) have one DDR Channel,Labeled B





Group	Signal Name	Pin Type[1]		Connection		Termination[6]		Level Shift[4]		Termination Voltage	
		FP4 Processor Types									
		1	2	1	2	1	2	1	2	1	2
	MA_ZVDDIO_MEM_S	A		Pull-up resistor	–	39.2Ω (± 1%)	–	–		VDDIO_MEM_S3	–
	MB_ZVDDIO_MEM_S	A		Pull-up resistor		39.2Ω (± 1%)		–		VDDIO_MEM_S3	

Table 3. Valid Socketed-Memory Configurations

Memory Type	Board Layers	Number of DIMM Sockets	Number of DIMMs Populated	DIMM 0	DIMM 1
UDIMM	4 or 6	1	1	SR/DR	–
		2	1	–	SR/DR
			2	SR/DR	SR/DR
SO-DIMM	6	1	1	SR/DR	–
		2	1	–	SR/DR
			2	SR/DR	SR/DR

Table 13. Memory Feature Compatibility

Memory Feature	FP4 Package	
	Type 1	Type 2
Memory Controller(s)	DDR3 Dual Channel	DDR3 Single Channel

5.1 Memory Interface

There are four signal groups for the memory bus interface—a Data group, a Control group, an Address/Command group, and a Clock group. The two types of FP4 processors support different memory configurations. See Table 1 for a list of FP4 processor type feature sets.

- Type 1 processors have two DDR3 channels, labeled A and B.
- Type 2 processors have one DDR3 channel, labeled B.

See the sections that follow for memory package-specific and implementation-specific information and design considerations.

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Title	005_APU_FP4(DDR3L)	
Size: D	Document Number: Rosa_Carrizo AIO	Rev: -1
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Title		
Size A	Document Number Rosa_Carrizo AIO	Rev -1
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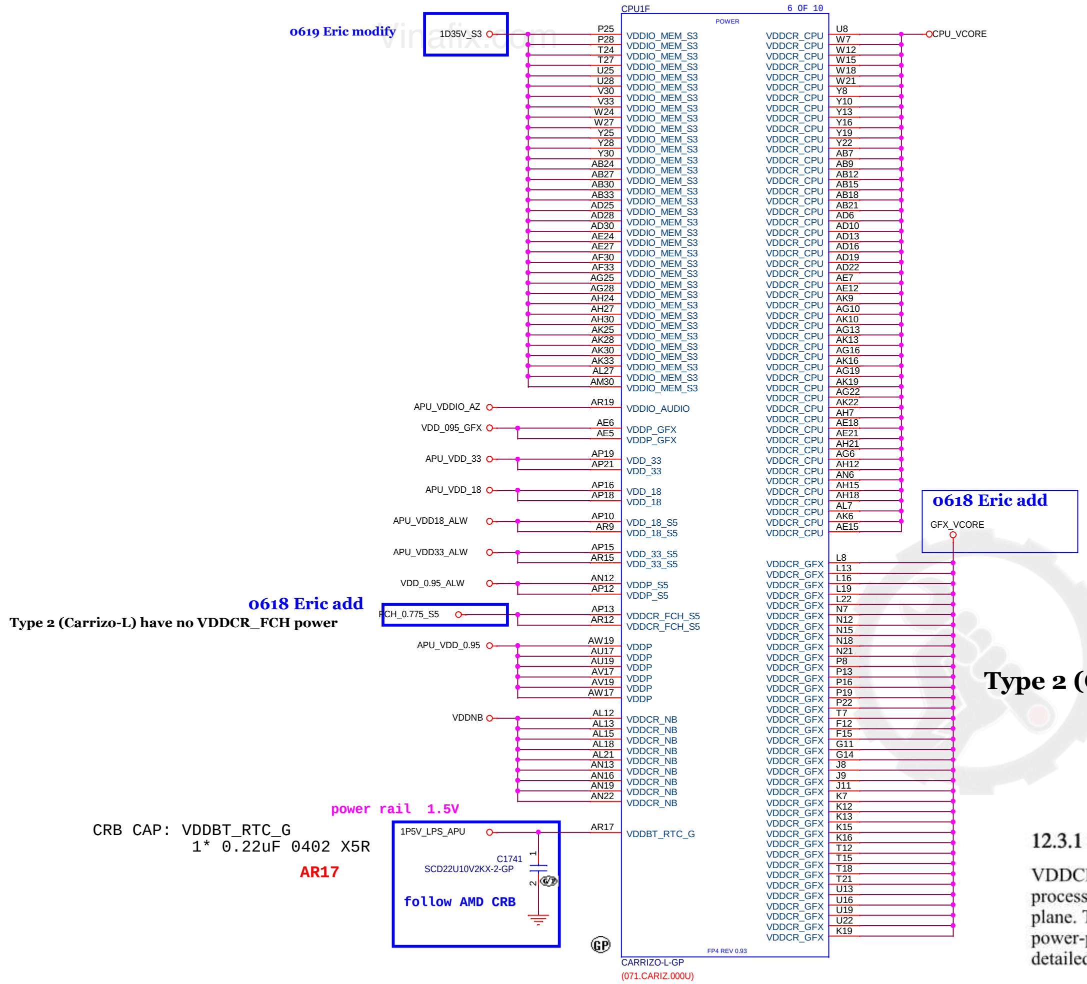
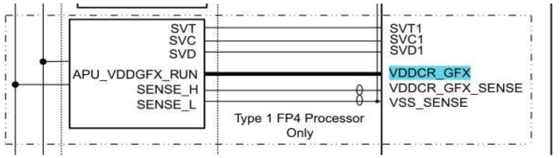


Type 2 (Carrizo-L) have no VDDCR_GFX power

12.3.1 CPU, Northbridge, and GPU Voltages

VDDCR_CPU is the voltage rail for the CPU core. VDDCR_NB powers the Northbridge and for FP4 Type 2 processors the integrated GPU circuitry. FP4 Type 1 processors have a separate VDDCR_GFX GPU power plane. The number of capacitors that can be placed on the layout is different depending on the via placement and power-plane cut. Vias connecting to capacitors should have masks up to the via hole. See Table 107 for a detailed list of required capacitors for VDDCR_CPU, VDDCR_NB, and VDDCR_GFX.



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Title	007_APU_FP4 (POWER)
Size C	Document Number: Rosa_Carrizo AIO — Rev -1
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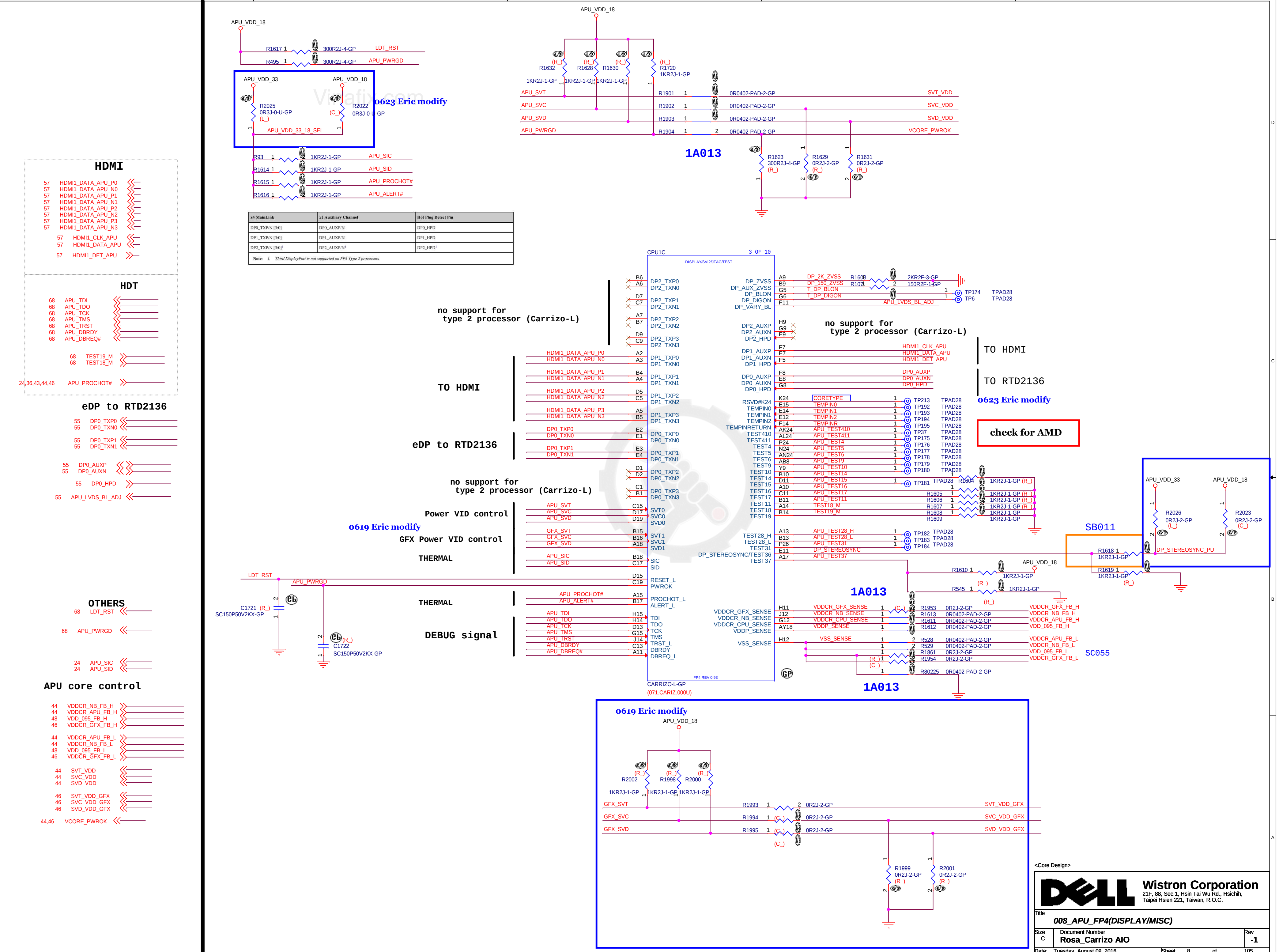

x4 MainLink	x1 Auxiliary Channel	Hot Plug Detect Pin
DP0_TXP/N [3:0]	DP0_AUXP/N	DP0_HPD
DP1_TXP/N [3:0]	DP1_AUXP/N	DP1_HPD
DP2_TXP/N [3:0][1]	DP2_AUXP/N[1]	DP2_HPD[1]
Note: 1. *Third DisplayPort is not supported on FP4 Type 2 processors*		

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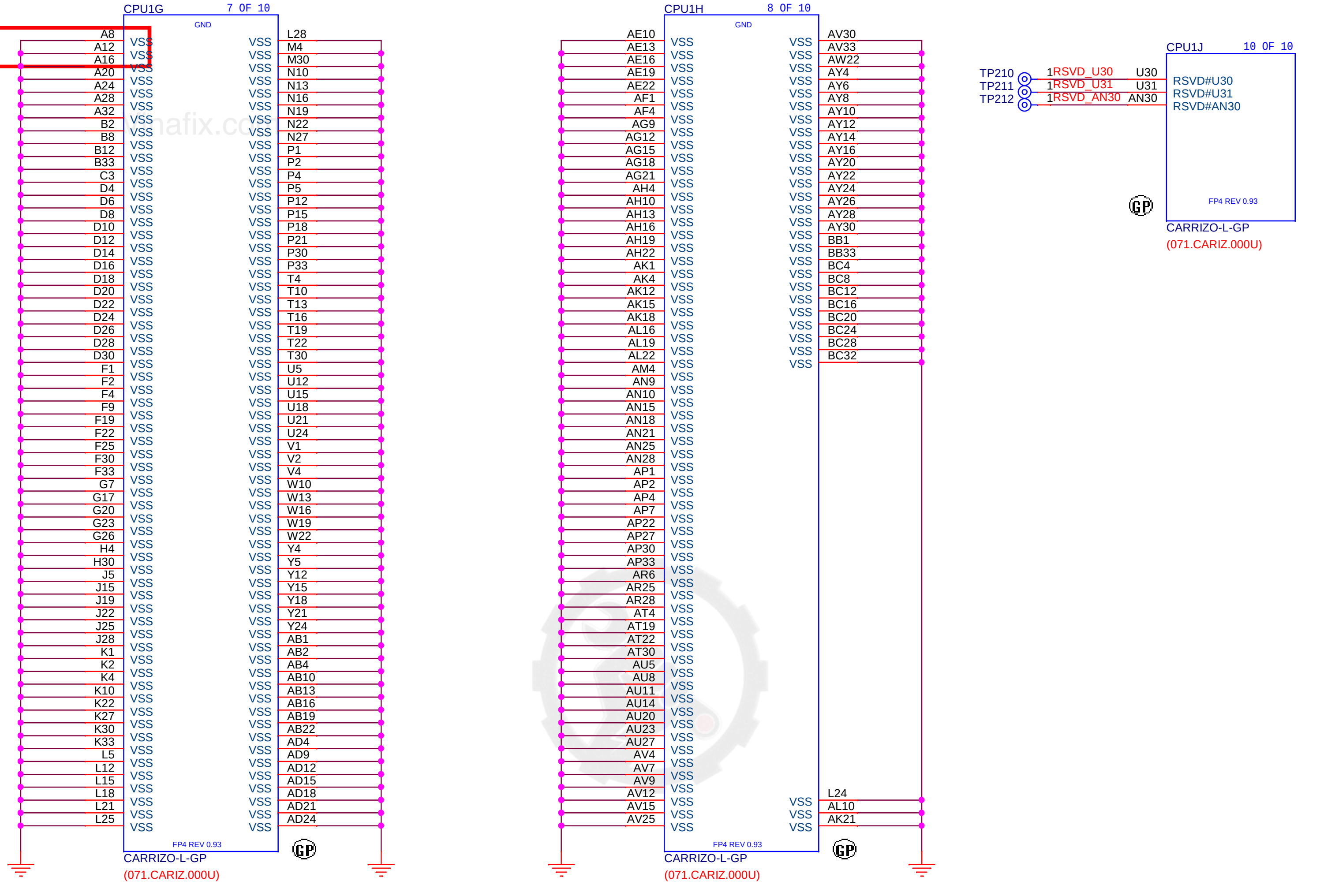
Title: *008_APU_FP4(DISPLAY/MISC)*

Size: C | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 8 of 105

AMD CRB for socket



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Title	*009_APU_FP4 (VSS)*	
Size B	Document Number **Rosa_Carrizo AIO**	Rev **-1**
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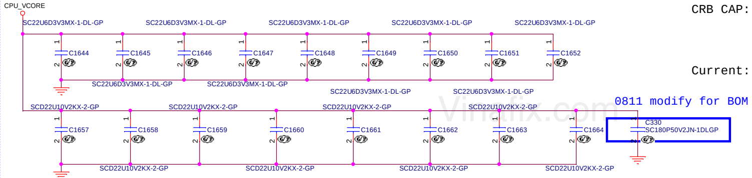
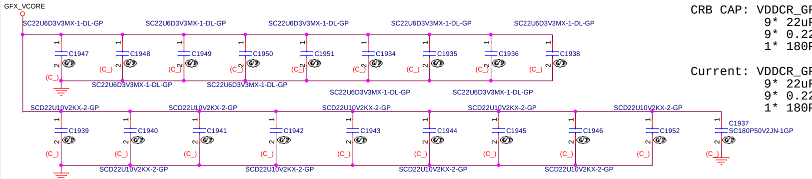


BOTTOM SIDE DECOUPLING UNDER APU

CRB CAP: VDDCR_CPU
9* 22uF 0603 X5R
8* 0.22uF 0402 X5R
1* 180P 0402 NPO

Current: VDDCR_CPU
9* 22uF 0603 X5R
8* 0.22uF 0402 X5R
1* 180P 0402 NPO

0619 Eric add

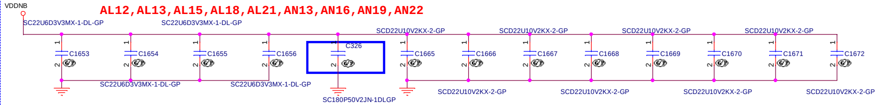


BOTTOM SIDE DECOUPLING UNDER APU

CRB CAP: VDDCR_GFX
9* 22uF 0603 X5R
9* 0.22uF 0402 X5R
1* 180P 0402 NPO

Current: VDDCR_GFX
9* 22uF 0603 X5R
9* 0.22uF 0402 X5R
1* 180P 0402 NPO

AL12,AL13,AL15,AL18,AL21,AN13,AN16,AN19,AN22



BOTTOM SIDE DECOUPLING UNDER APU

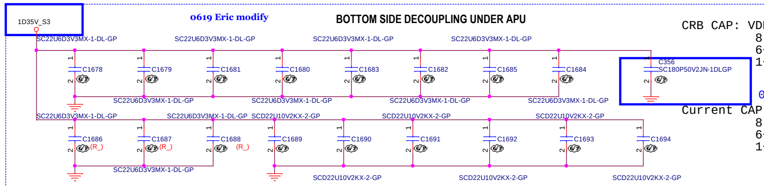
0811 modify for BOM

CRB CAP: VDDCR_NB
4* 22uF 0603 X5R
8* 0.22uF 0402 X5R
1* 180P 0402 NPO

Current CAP: VDDCR_NB
4* 22uF 0603 X5R
8* 0.22uF 0402 X5R
1* 180P 0402 NPO

0619 Eric modify

BOTTOM SIDE DECOUPLING UNDER APU



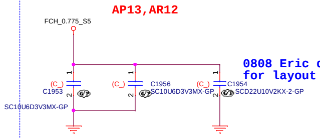
CRB CAP: VDDIO_MEM_ S3
8* 22uF 0603 X5R ,3*DNI
6+4(DIMM side)* 0.22uF 0402 X5R
1+2(DIMM side* 180P 0402 NPO

0811 modify for BOM

Current CAP: VDDIO_MEM_ S3
8* 22uF 0603 X5R ,3*DNI
6+4(DIMM side)* 0.22uF 0402 X5R
1+2(DIMM side)* 180P 0402 NPO

0619 Eric add

AP13,AR12

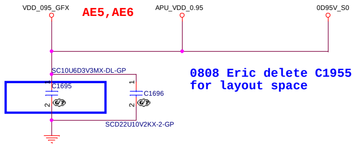


0808 Eric delete C1955
for layout space

BOTTOM SIDE DECOUPLING UNDER APU

CRB CAP: VDDCR_FCH_S5
2* 10uF 0402 X5R
1* 0.22uF 0402 X5R
Current CAP: VDDCR_FCH_S5
~~2* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R

AE5,AE6



0624 Eric modify Q'ty

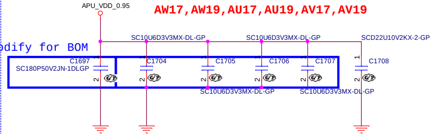
0808 Eric delete C1955 and short pad
for layout space

BOTTOM SIDE DECOUPLING UNDER APU

CRB CAP: VDDP_GFX
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R
Current CAP: VDDP_GFX
~~1* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R

AW17,AW19,AU17,AU19,AV17,AV19

0811 modify for BOM



BOTTOM SIDE DECOUPLING UNDER APU

0624 Eric modify Q'ty
CRB CAP: VDDP
4* 10uF 0402 X5R
1* 0.22uF 0402 X5R
1* 180P 0402 NPO

Current CAP: VDDP
~~4* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R
1* 180P 0402 NPO

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Title: 010_APU_FP4(POWER CAP1)		
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
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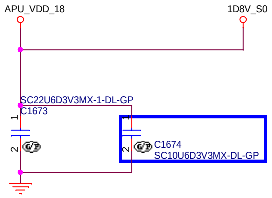
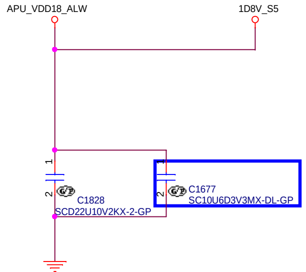
AP16,AP18



CRB CAP: VDDP_18
1* 10uF 0402 X5R
1* 22uF 0603 X5R

Current CAP: VDDP_18
~~1* 10uF 0603 X5R~~
1* 22uF 0603 X5R



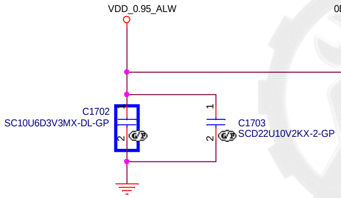
AP10,AR9

CRB CAP: VDDP_18_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R

Current CAP: VDDP_18_S5
~~1* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R

delete for 0.95V_DUAL power rail, no use 0.95V_DUAL from CRB

AN12,AP12



CRB CAP: VDDP_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R

Current CAP: VDDP_S5
~~1* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R

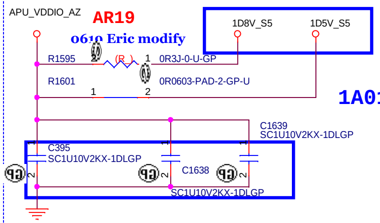
CRB CAP: VDDIO_AUDIO
3* 1uF 0402 X5R

Current CAP: VDDIO_AUDIO
3* 1uF 0402 X5R

CRB CAP: VDD_33
1* 10uF 0402 X5R
Current CAP: VDD_33
~~1* 10uF 0603 X5R~~

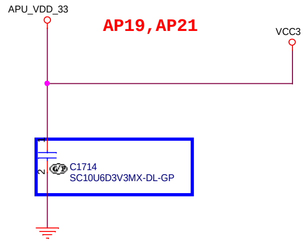
CRB CAP: VDD_33_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R
Current CAP: VDD_33_S5
~~1* 10uF 0603 X5R~~
1* 0.22uF 0402 X5R

AR19

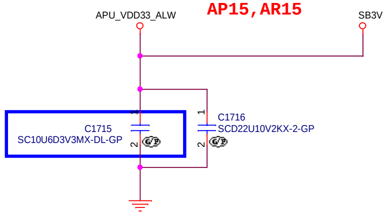


1A015

AP19,AP21



AP15,AR15



0624 Eric delete

0624 Eric delete

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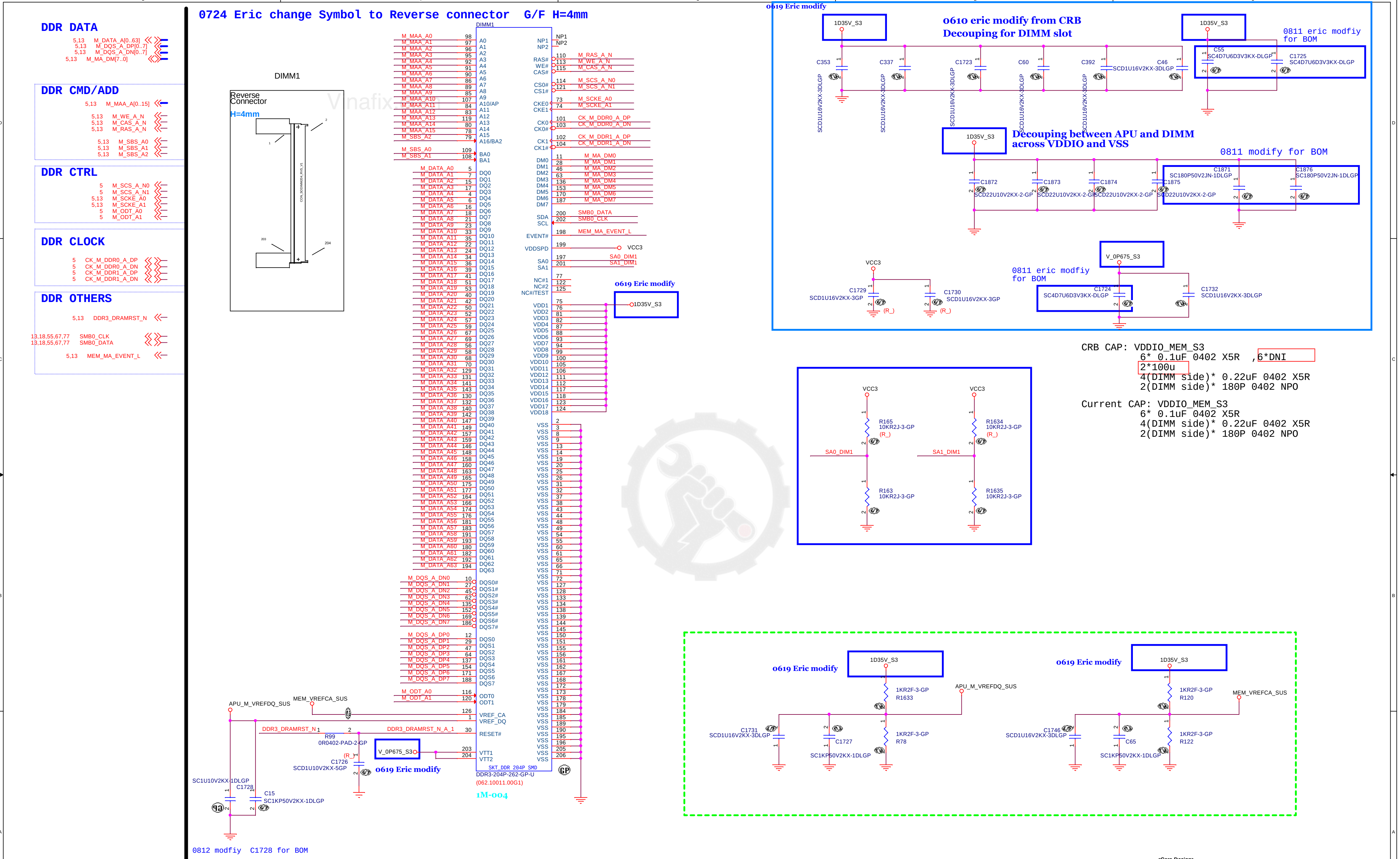
Title
011_APU_FP4(POWER CAP2)

Size	Document Number	Rev
Custom	Rosa_Carrizo AIO	-1

Date: Tuesday, August 09, 2016 Sheet 11 of 105



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Title	012_DDR3_SODIMM1		
Size: Custom	Document Number: Rosa_Carrizo AIO		Rev: -1
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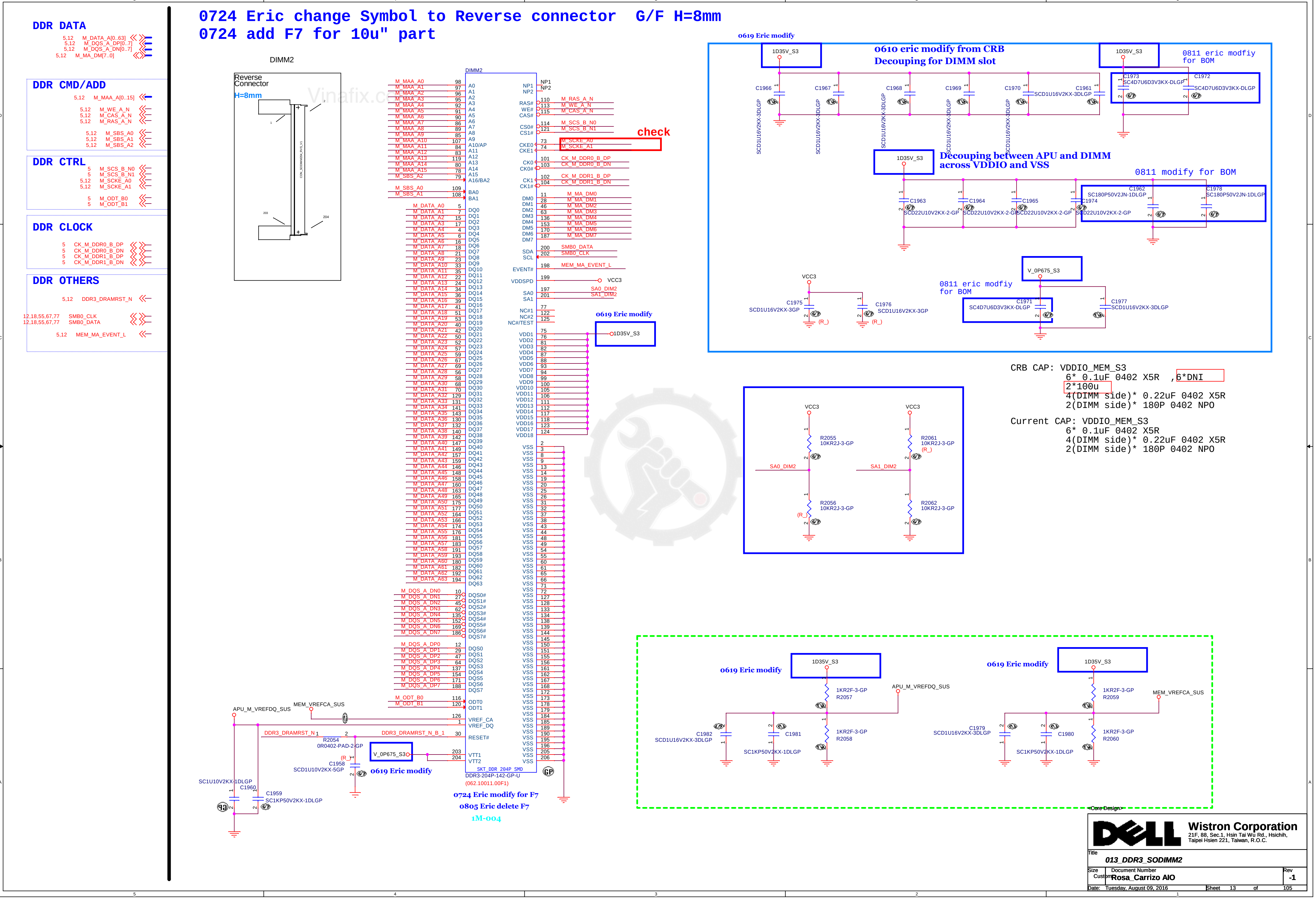

0724 Eric change Symbol to Reverse connector G/F H=8mm
0724 add F7 for 10u" part
DDR DATA
M_DATA_A[0..63]
M_DQS_A_DP[0..7]
M_DQS_A_DN[0..7]
M_MA_DM[7..0]
DDR CMD/ADD
M_MAA_A[0..15]
M_WE_A_N
M_CAS_A_N
M_RAS_A_N
M_SBS_A0
M_SBS_A1
M_SBS_A2
DDR CTRL
M_SCS_B_N0
M_SCS_B_N1
M_SCKE_A0
M_SCKE_A1
M_ODT_B0
M_ODT_B1
DDR CLOCK
CK_M_DDR0_B_DP
CK_M_DDR0_B_DN
CK_M_DDR1_B_DP
CK_M_DDR1_B_DN
DDR OTHERS
DDR3_DRAMRST_N
SMB0_CLK
SMB0_DATA
MEM_MA_EVENT_L
DIMM2
Reverse Connector
H=8mm
check
0619 Eric modify
0610 eric modify from CRB
Decoupling for DIMM slot
0811 eric modfiy for BOM
Decoupling between APU and DIMM across VDDIO and VSS
0811 modify for BOM
0811 eric modfiy for BOM
CRB CAP: VDDIO_MEM_S3
6* 0.1uF 0402 X5R ,6*DNI
2*100u
4(DIMM side)* 0.22uF 0402 X5R
2(DIMM side)* 180P 0402 NPO
Current CAP: VDDIO_MEM_S3
6* 0.1uF 0402 X5R
4(DIMM side)* 0.22uF 0402 X5R
2(DIMM side)* 180P 0402 NPO
DDR3-204P-142-GP-U
(062.10011.00F1)
0724 Eric modify for F7
0805 Eric delete F7
1M-004
APU_M_VREFDQ_SUS
MEM_VREFCA_SUS
DDR3_DRAMRST_N_B_1
0619 Eric modify
<Core Design>
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Title
013_DDR3_SODIMM2
Size Custom
Document Number
Rosa_Carrizo AIO
Rev -1
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Title		
Size A4	Document Number **Rosa_Carrizo AIO**	Rev **-1**
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Strap Pin

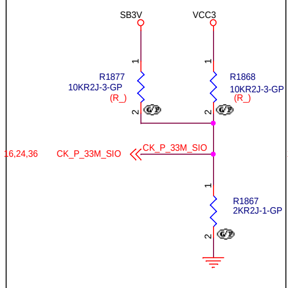
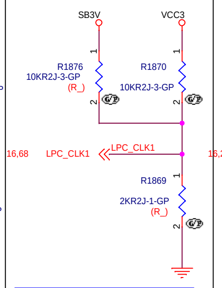
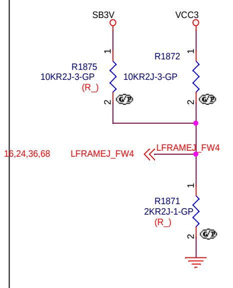
Description	LPC_CLK0	LPC_CLK1	LFRAME_L
GPIO	CK_P_33M_SIO	LPC_CLK1	LFRAMEJ_FW4
Schematic			
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM

Table 90. Strapping Options

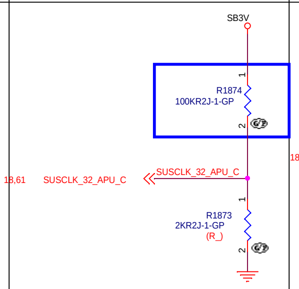
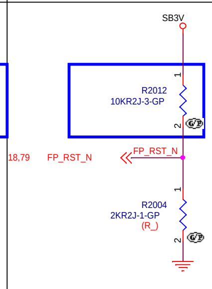
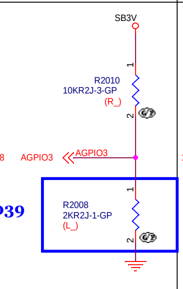
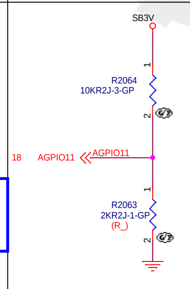
SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LFRAME_L	ROMTYPE	II	1	0	LPC ROM
				1	SPI ROM (Default)
LPCCLK1	CLKGEN	II	1	0	Reserved
				1	Configured for internal clock-generator (Default)
LPCCLK0	BOOTFAILTIMER	II	0	0	Boot Fail Timer Disabled (Default)

Table 90. Strapping Options (continued)

SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LPCCLK0	BOOTFAILTIMER	II	0	1	Boot Fail Timer Enabled
RTCCLK	RTC Coin Battery	I	1	0	RTC Coin Battery is not implemented
				1	RTC Coin Battery is implemented (Default)
SYS_RESET_L	ShortReset	I	1	0	Reserved
				1	Normal powerup/reset timing (Default)
AGPIO3	Alternate Reset	I	1	0	Traditional Reset logic (Type 1 FP4 Processor Only) 2 kΩ (± 5%) pull-down resistor to VSS
				1	Enhanced Reset logic (Default) for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5
				Note:	• *Platforms that are designed for AOAC complaint are recommended to use Alternate Reset* • *To ensure the strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config value until 20 ms after RsmRstB has risen to at least 3.0 v.*

Strap Pin

SB012 Eric modfiy BOM

Description	RTC_CLK Int pull-up	SYS_RSET_L	AGPIO3	BLINK
GPIO	SUSCLK_32_APU_C	FP_RST_N	AGPIO3	AGPIO11
Schematic			SB039 	
PULL HIGH	RTC coin Battery is not implemented (DEFAULT)	normal reset mode (DEFAULT)	Enhanced Reset logic (Default) for faster resume from S5	LDT_RST#/LDT_PWRGD output to APU (DEFAULT)
PULL LOW	RTC coin Battery is implemented	short reset mode	Traditional Reset logic (DEFAULT)	LDT_RST#/LDT_PWRGD output to Pads

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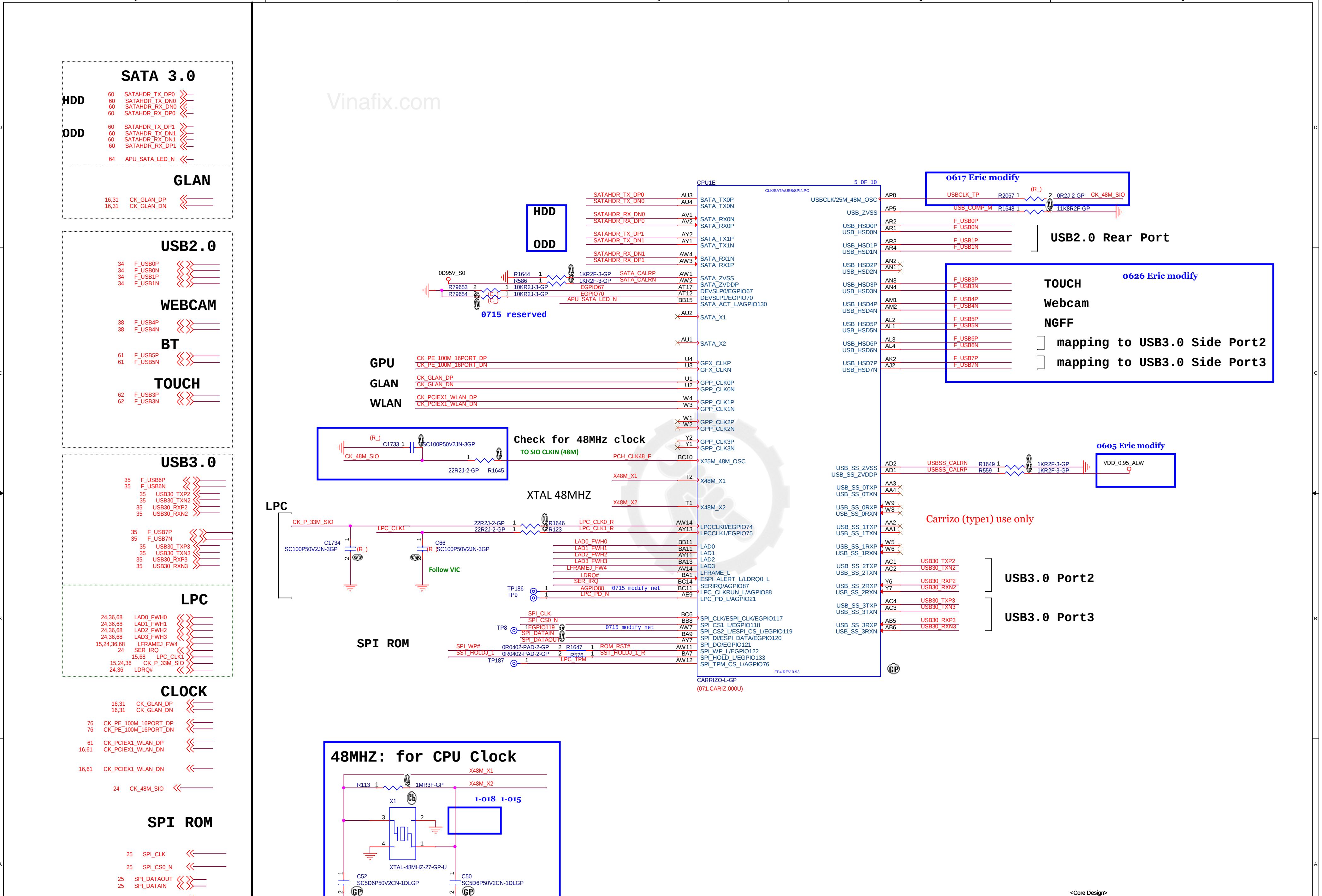
Title	015_APU_FP4 (STRAP)	
Size C	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 15 of 105	



<Core Design>

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Title	016_APU_FP4(SATA/USB/LPC/SPI)	
Size C	Document Number: Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 16 of 105	

Blanking

<Core Design>

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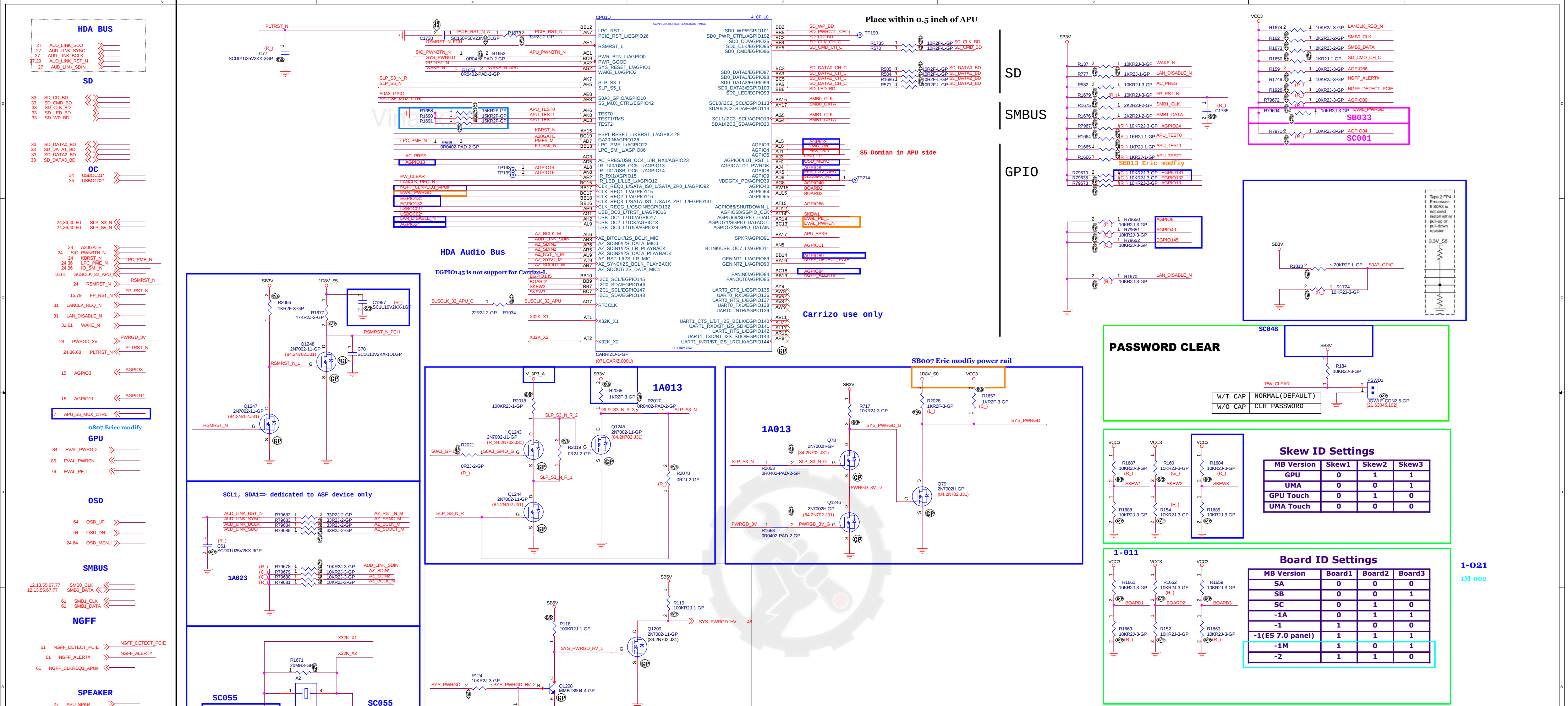
Title	
Size A4	Document Number **Rosa_Carrizo AIO** — Rev **-1**
Date: Tuesday, August 09, 2016	Sheet 17 of 105



PASSWORD CLEAR

W/T CAP	NORMAL(DEFAULT)
W/O CAP	CLR PASSWORD

Skew ID Settings

MB Version	Skew1	Skew2	Skew3
GPU	0	1	1
UMA	0	0	1
GPU Touch	0	1	0
UMA Touch	0	0	0

Board ID Settings

MB Version	Board1	Board2	Board3
SA	0	0	0
SB	0	0	1
SC	0	1	0
-1A	0	1	1
-1	1	0	0
-1(ES 7.0 panel)	1	1	1
-1M	1	0	1
-2	1	1	0

<Core Design>

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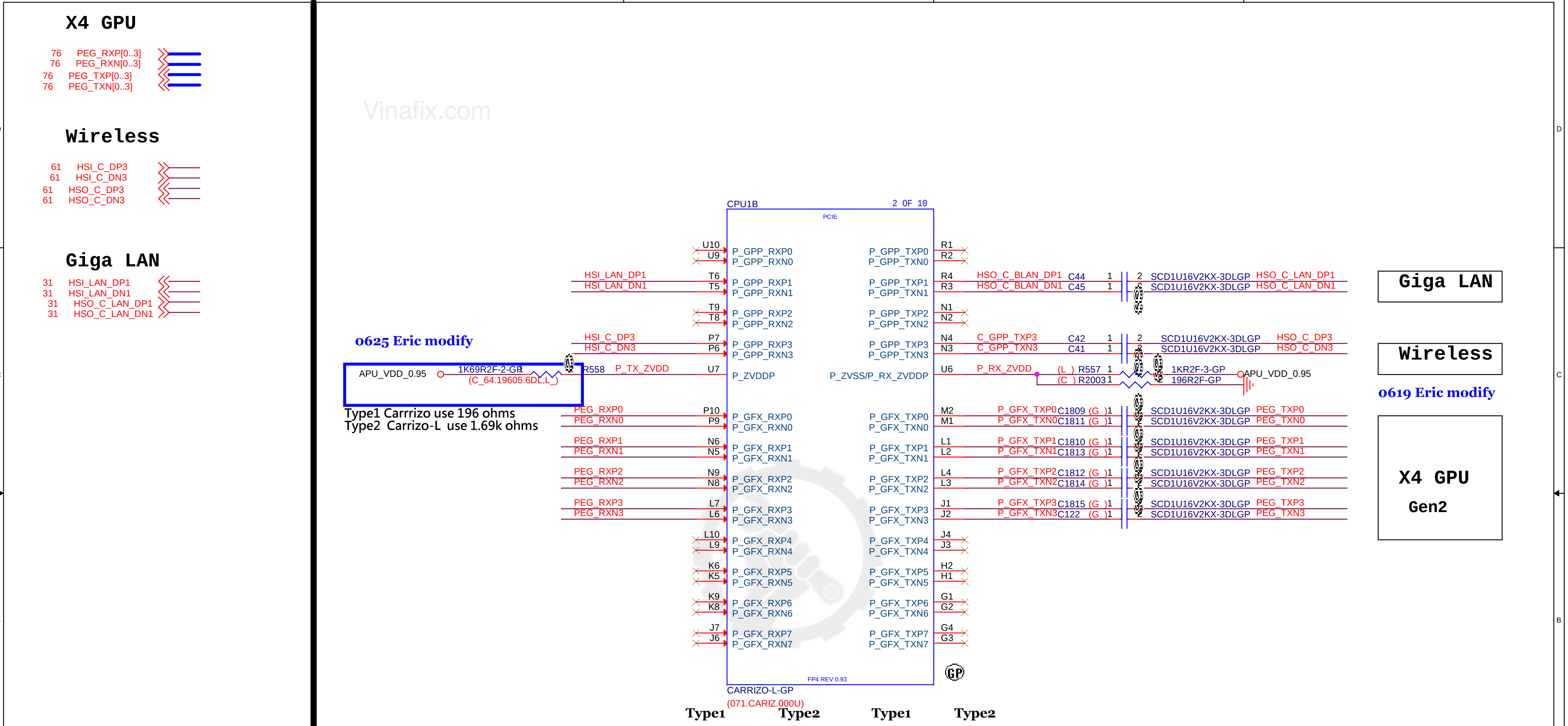
Title: *018_APU_(GPIO/AZ/I2C/SD/UARTS)*

Size: Custom | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 18 of 105



		Type1	Type2	Type1	Type2			
P_ZVDDP	A	Pull-up resistor		196Ω (± 1%)	1.69 kΩ (± 1%)	–	VDDP	
P_ZVSS/ P_RX_ZVDDP	A	Pull-down resistor	Pull-up resistor	196Ω (± 1%)	1 kΩ (± 1%)	–	VSS	VDDP

<Core Design>

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Title: 019_APU_FP4(PCIE I/F)

Size: B | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 19 of 105

Blanking

<Core Design>

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Title		
Size A4	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 20 of 105	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 21 of 105	

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<Core Design>

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Title		
Size A4	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 22 of 105	

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<Core Design>

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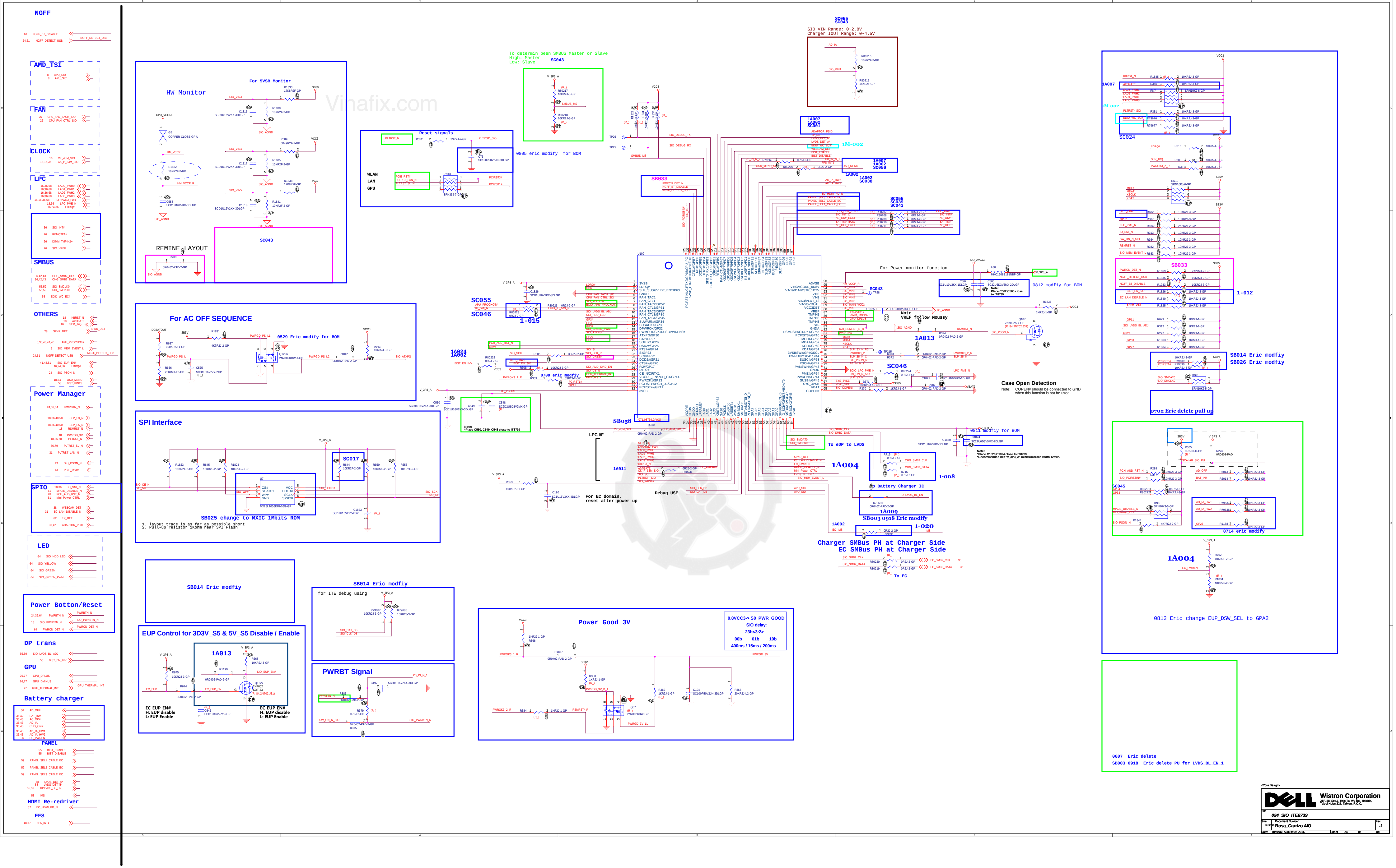
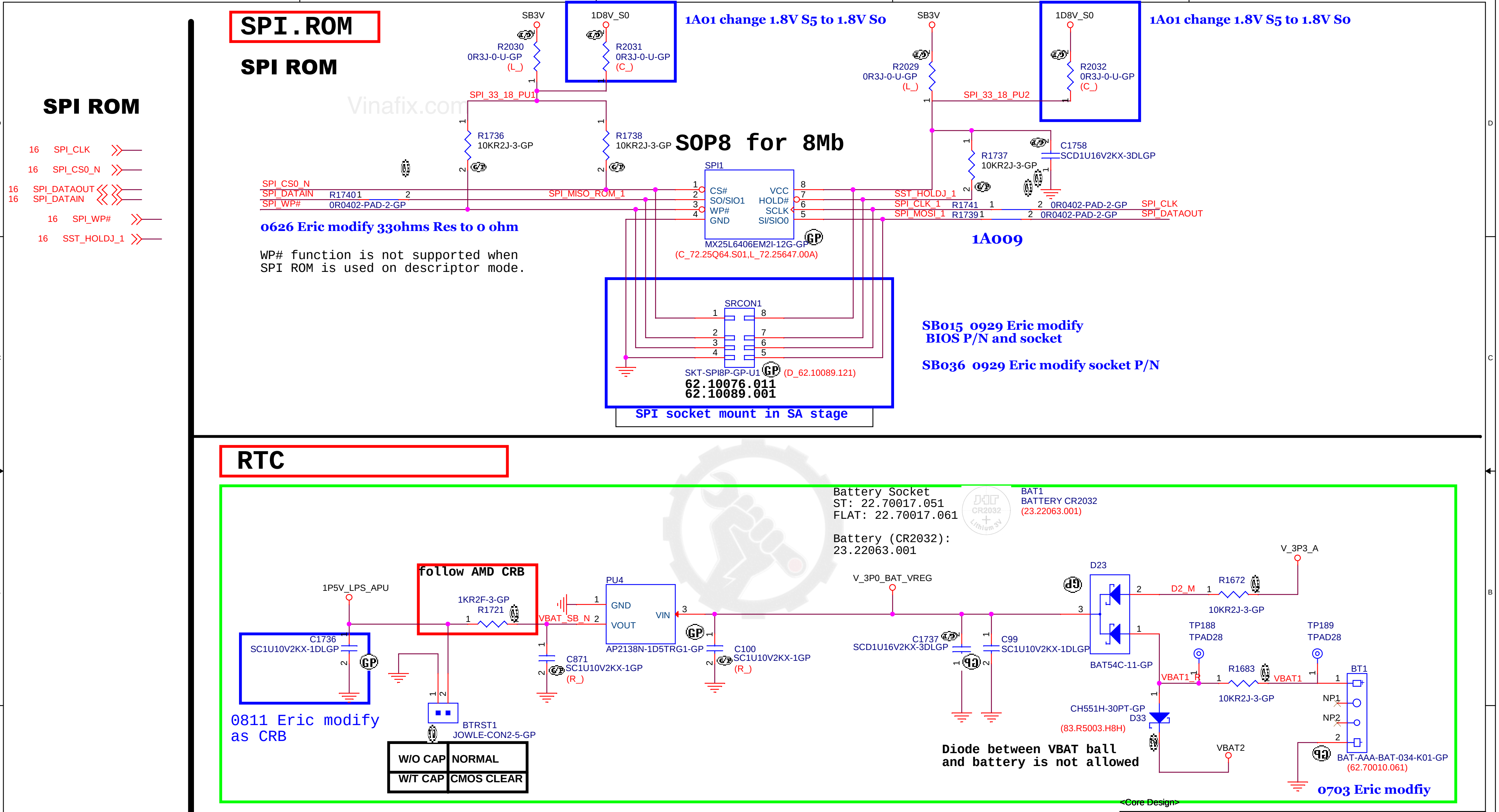
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size A4	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 23 of 105	



NGFF
AMD_TSI
FAN
CLOCK
LPC
SMBUS
OTHERS
Power Manager
GPIO
LED
Power Botton/Reset
DP trans
GPU
Battery charger
PANEL
HDMI Re-redriver
FFS
HW Monitor
For 5VSB Monitor
REMINE LAYOUT
SC043
Reset signals
WLAN
LAN
GPU
0805 eric modify for BOM
To determin been SMBUS Master or Slave
High: Master
Low: Slave
SIO VIN Range: 0~2.8V
Charger IOUT Range: 0~4.5V
SC055
SC043
1A007
1A002
SC001
SB033
SC055
SC039
SC043
For Power monitor function
0812 modify for BOM
For AC OFF SEQUENCE
0529 Eric modify for BOM
SC055
SC046
1-015
1A024
1A002
0709 eric modify
SPI Interface
SC017
SB025 change to MXIC 1Mbits ROM
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash
LPC I/F
1A011
For EC domain, reset after power up
Debug USE
SB058
To eDP to LVDS
1A004
1-008
Battery Charger IC
1A009
SB003 0918 Eric modify
1-020
Charger SMBus PH at Charger Side
EC SMBus PH at Charger Side
To EC
SC046
1A013
Case Open Detection
Note: COPEN# should be connected to GND when this function is not be used.
0811 modify for BOM
SC024
SB033
1-012
SB014 Eric modify
SB026 Eric modify
0702 Eric delete pull up
SC045
0714 eric modify
1A004
0812 Eric change EUP_DSW_SEL to GPA2
0607 Eric delete
SB003 0918 Eric delete PU for LVDS_BL_EN_1
SB014 Eric modfiy
for ITE debug using
EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable
1A013
EC_EUP_EN#
H: EUP disable
L: EUP Enable
PWRBT Signal
Power Good 3V
0.8VCC3->S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
Wistron Corporation
024_SIO_ITE8739
Rosa_Carrizo AIO



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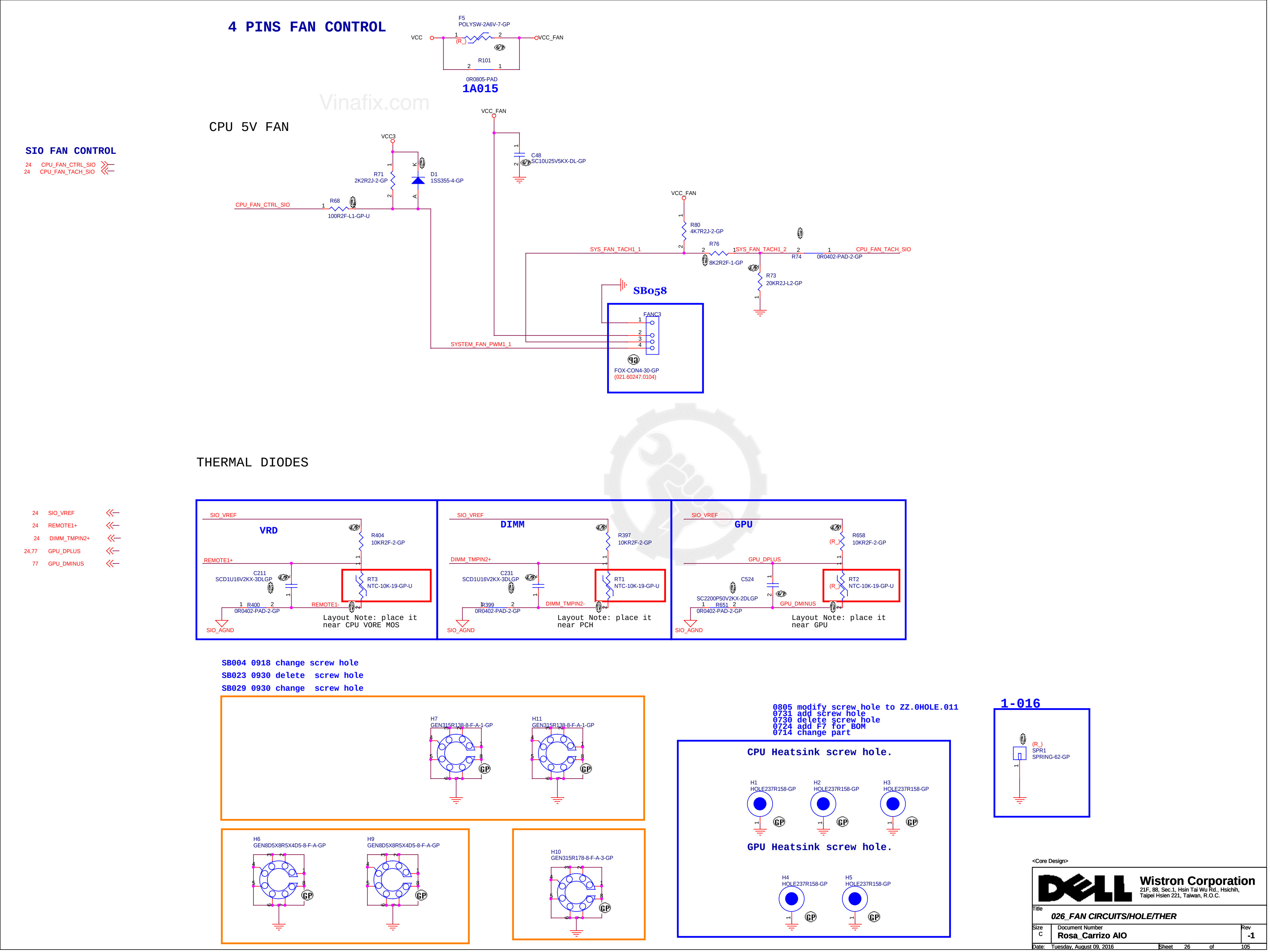
Title: *025_Flash ROM/RTC*

Size	Document Number	Rev
B	Rosa_Carrizo AIO	-1

Date: Tuesday, August 09, 2016 Sheet 25 of 105



<Core Design>

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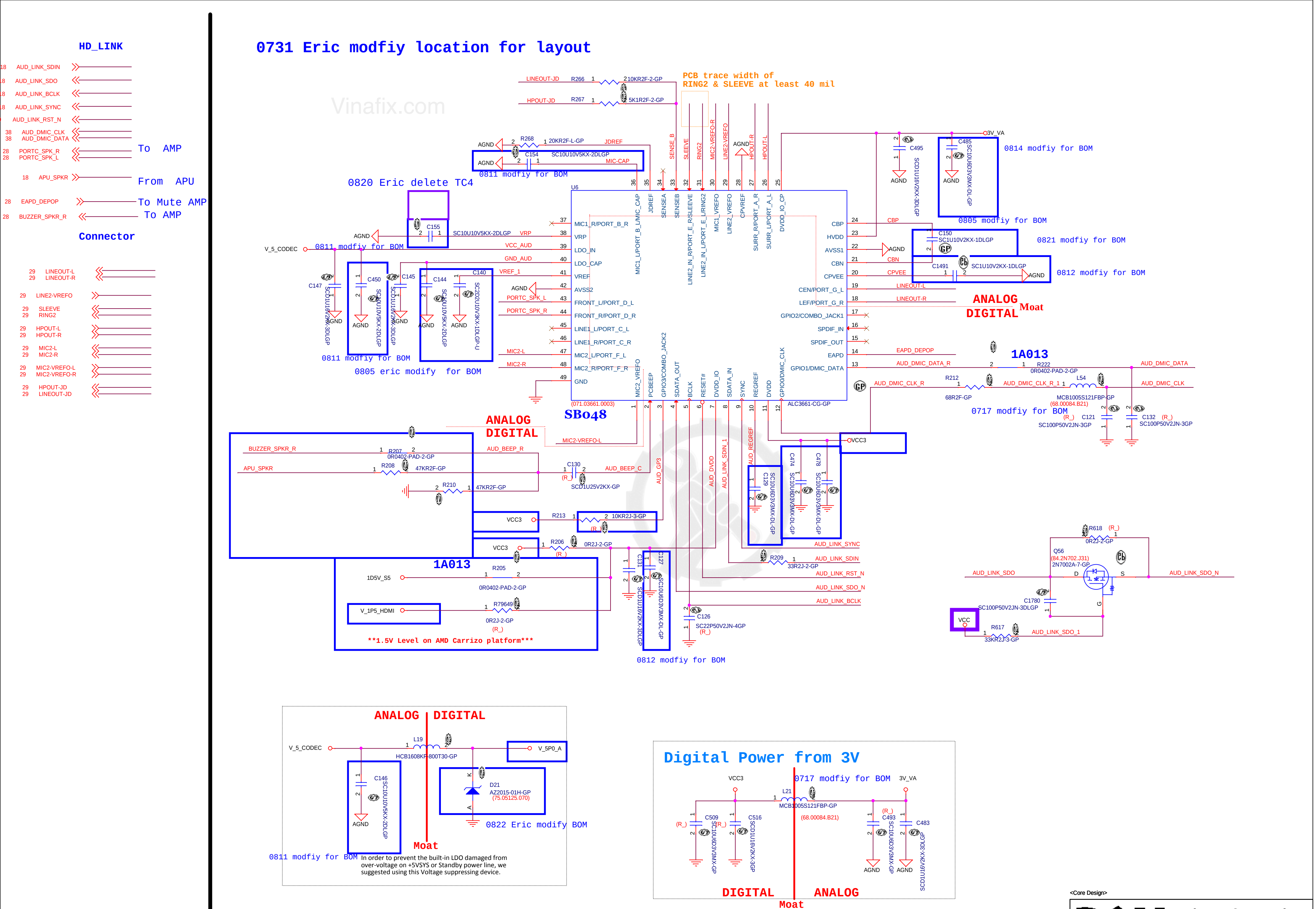
Title	026_FAN CIRCUITS/HOLE/THER
Size	C
Document Number	Rosa_Carrizo AIO
Rev	-1
Date:	Tuesday, August 09, 2016
Sheet	26 of 105



<Core Design>

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Title	027_AUDIO ALC3220	
Size C	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 27 of 105	

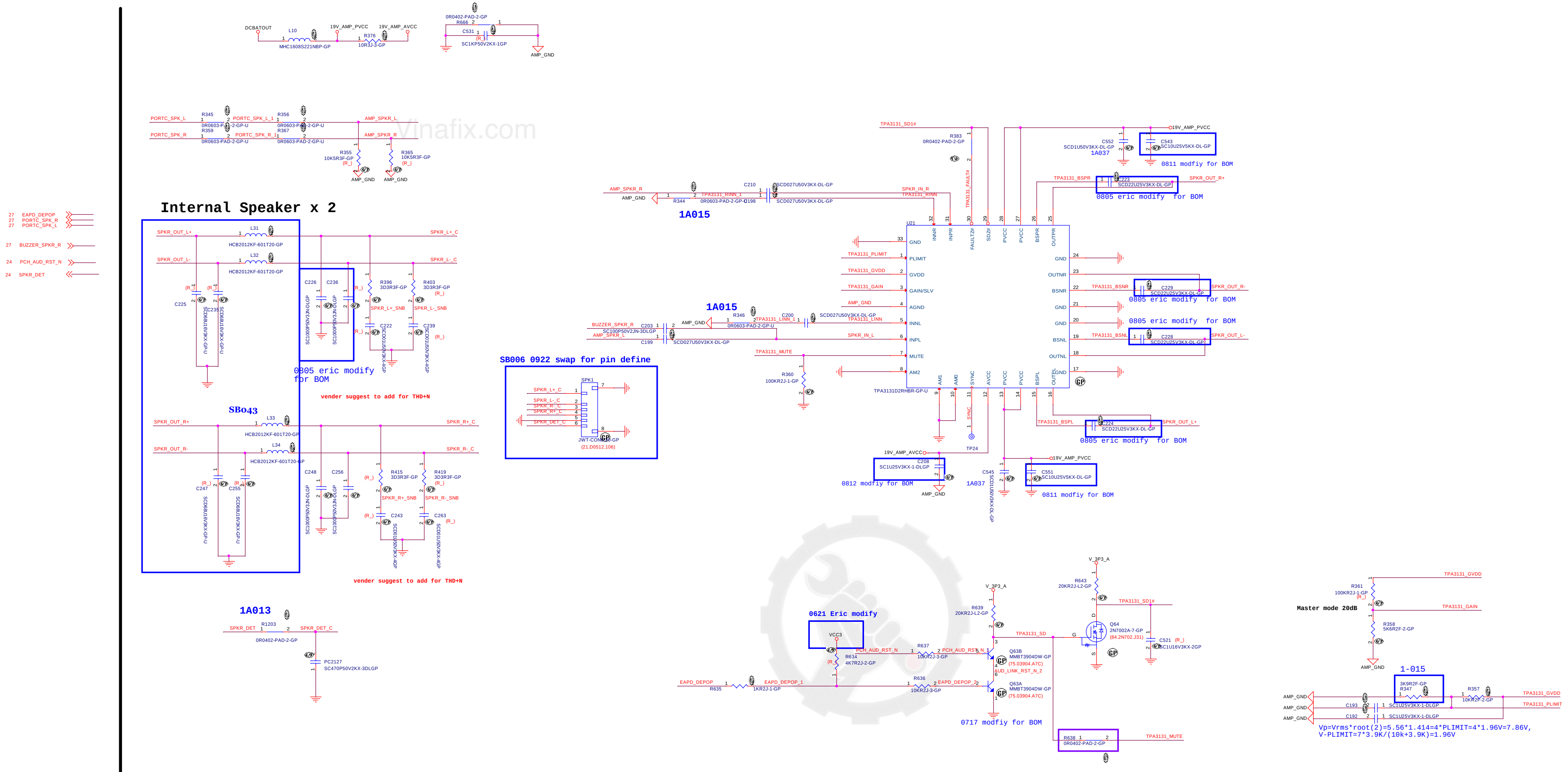

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \text{ for unclipped power} \quad (2)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

Table 3. POWER LIMIT Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Short	Open	17.90
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to $1V_{rms}$.

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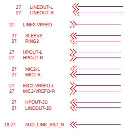
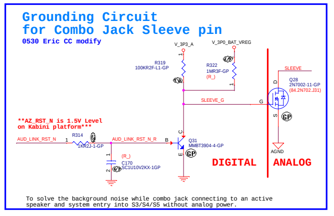
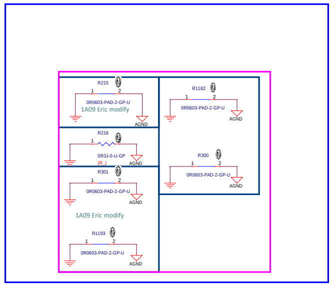
Title: 028_AMP TPA3131

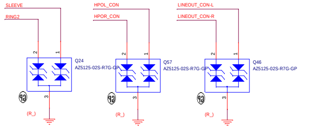
Size: D | Document Number: Rosa_Carrizo AIO | Rev: -1

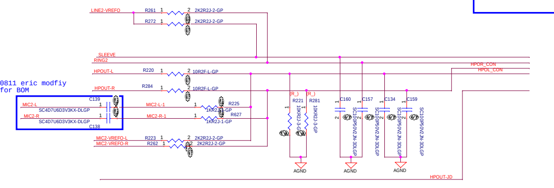


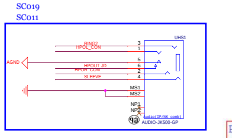
0731 Eric modfiy location for layout



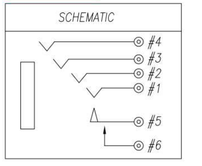








Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND



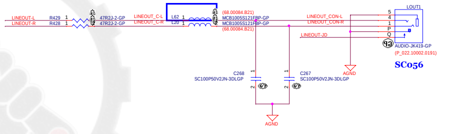
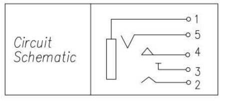
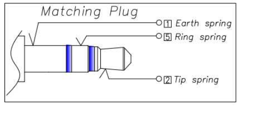


TABLE A: Circuit





4-pin 3.5mm Headset Connector Pinout

Nokia, Lenovo mobile

Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Microphone**
4	Sleeve	**Ground / Common**

iPhone, Samsung, Blackberry, HTC

Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Ground / Common**
4	Sleeve	**Microphone**

<Core Design>

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Title	029_MIC/SPEAKER/AUDIO JACK
Size: Custom	Document Number: Rosa_Carrizo AIO — Rev -1
Date: Tuesday, August 09, 2016	Sheet 29 of 105

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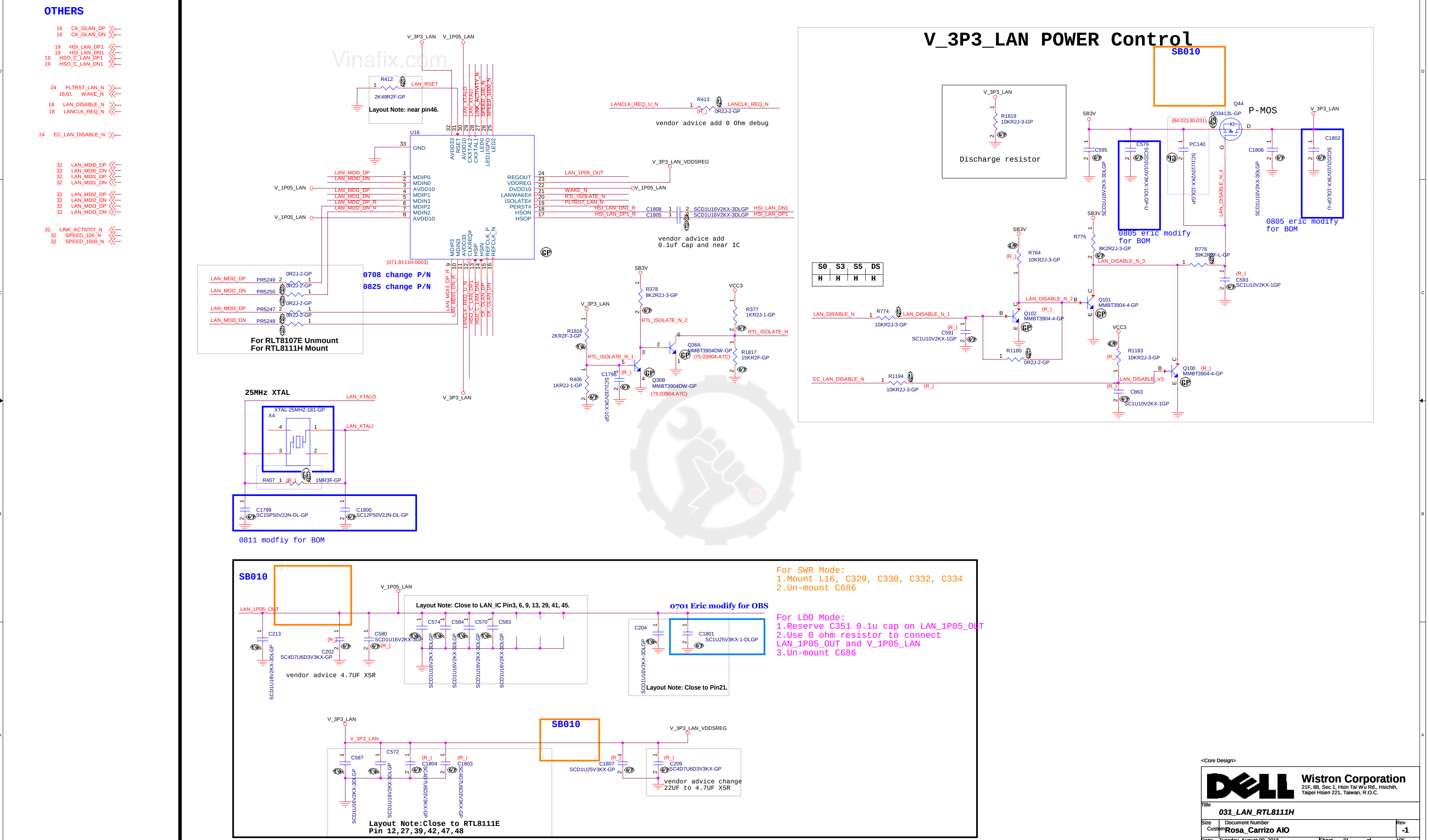
Title		
Size: A	Document Number: **Rosa_Carrizo AIO**	Rev: **-1**
Date: Tuesday, August 09, 2016	Sheet 30 of 105	



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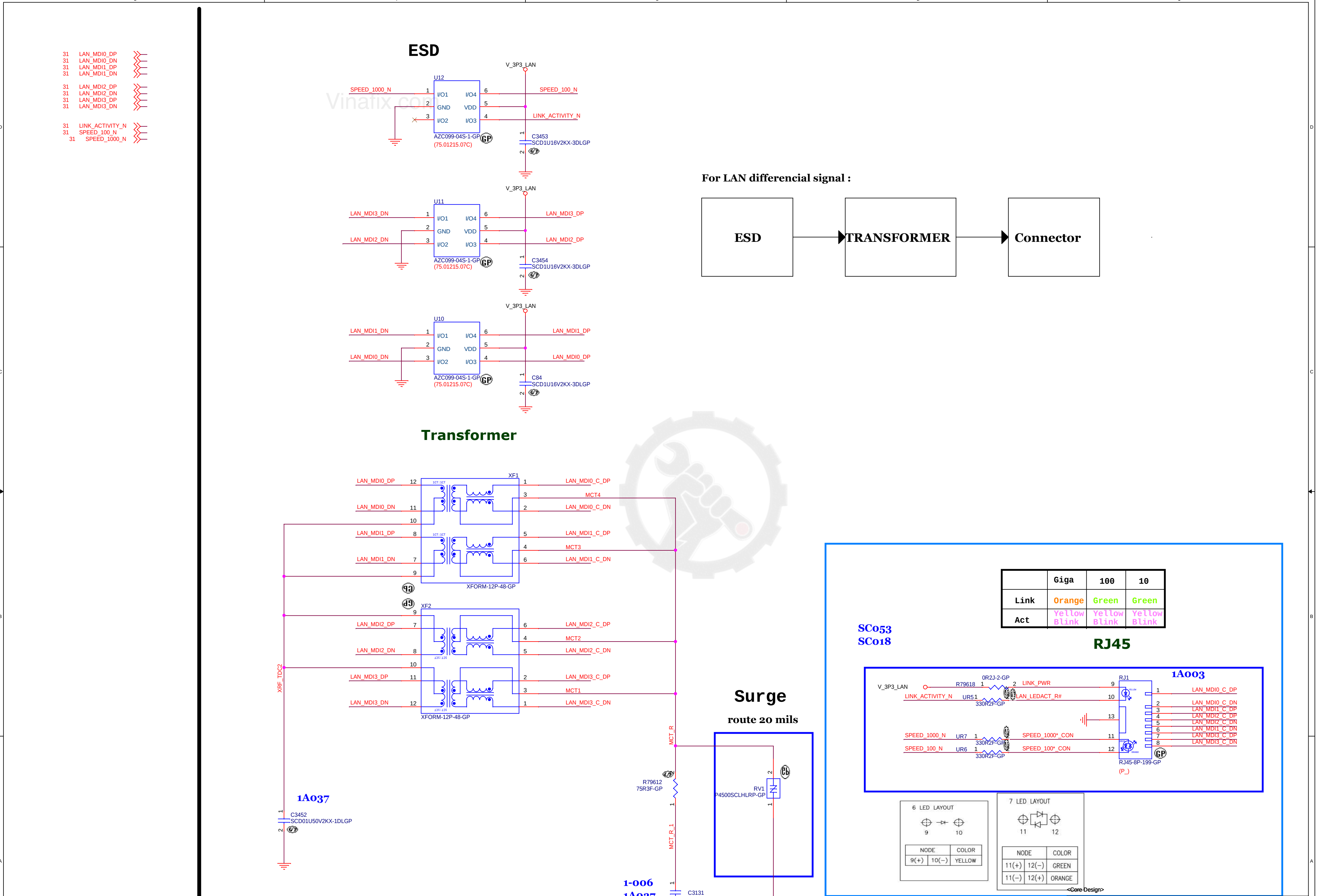
Title		
031_LAN_RTL8111H		
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 31 of 105	



	Giga	100	10
Link	Orange	Green	Green
Act	Yellow Blink	Yellow Blink	Yellow Blink

NODE		COLOR
9(+)	10(-)	YELLOW

NODE		COLOR
11(+)	12(-)	GREEN
11(-)	12(+)	ORANGE

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Title: 032_RJ45+Transformer

Size: C | Document Number: Rosa_Carrizo AIO | Rev: -1

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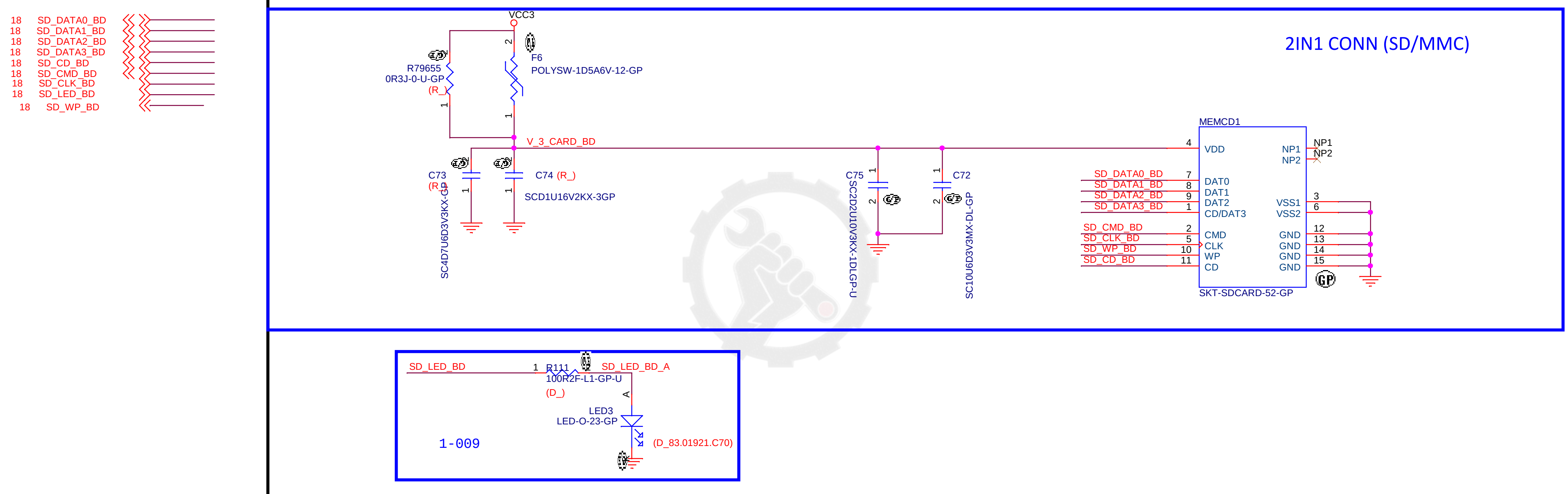
CAER READER



<Core Design>

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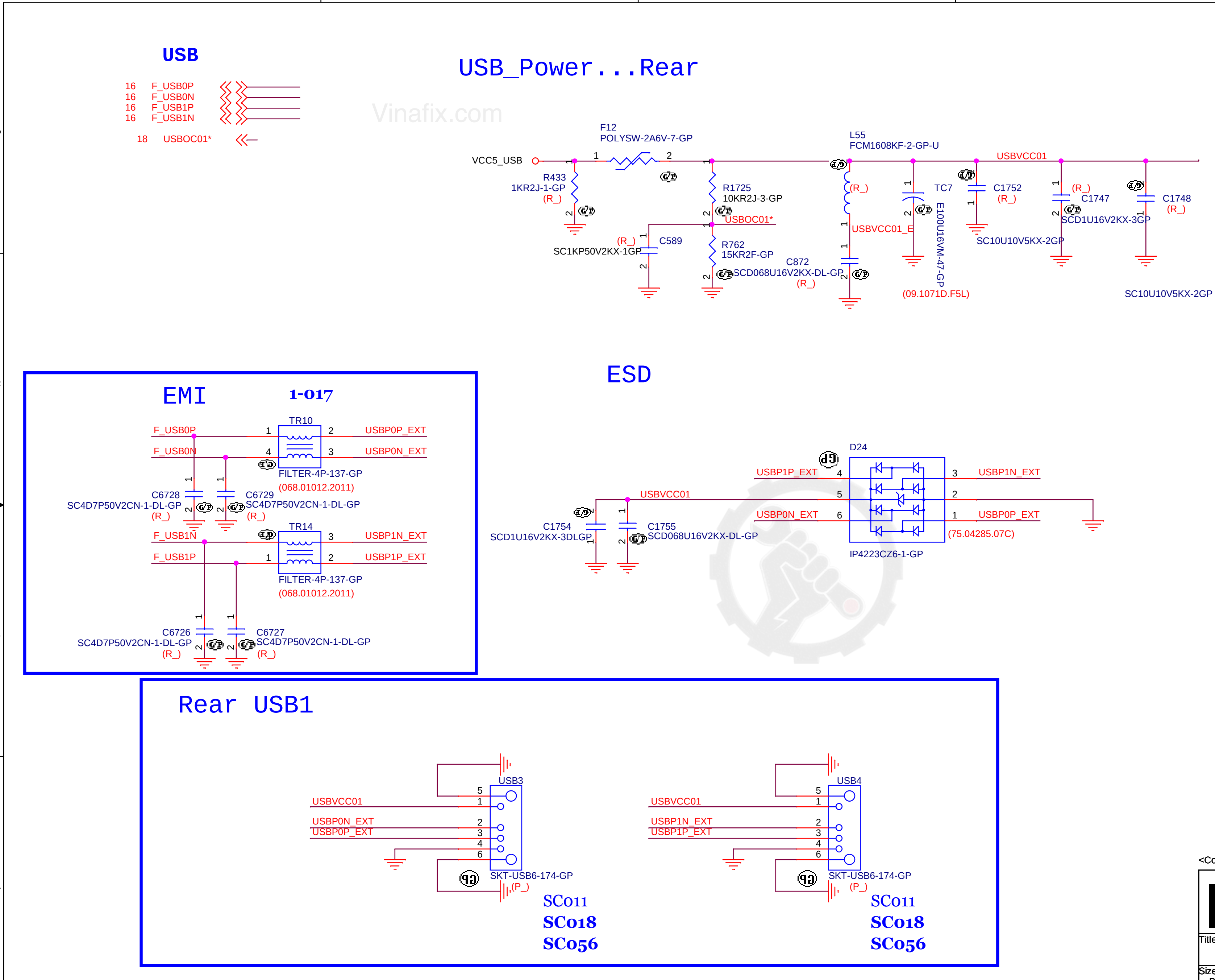
Title: *033_CardReader Conn*

Size	Document Number	Rev
B	Rosa_Carrizo AIO	-1

Date: Tuesday, August 09, 2016 Sheet 33 of 105



<Core Design>

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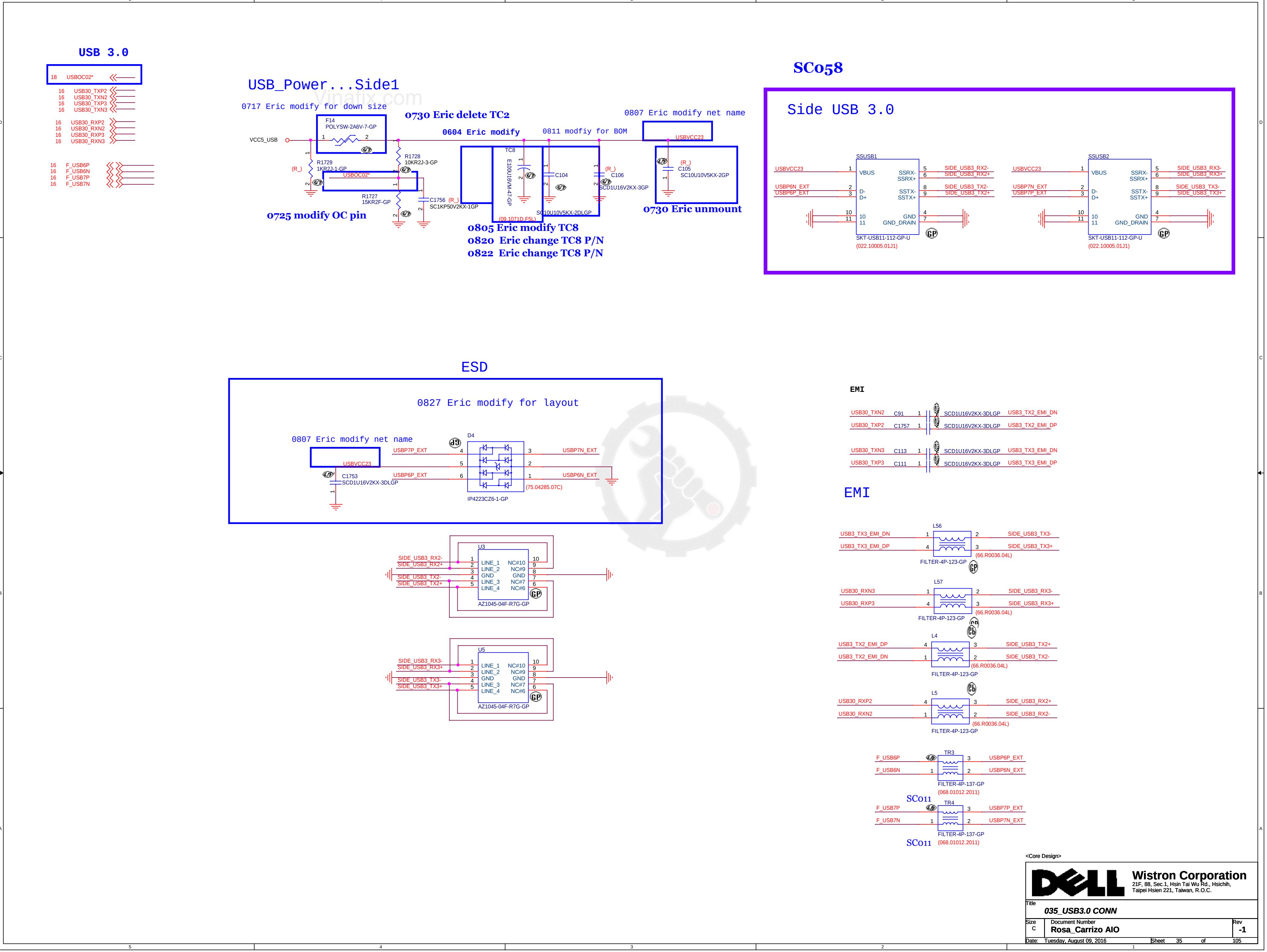
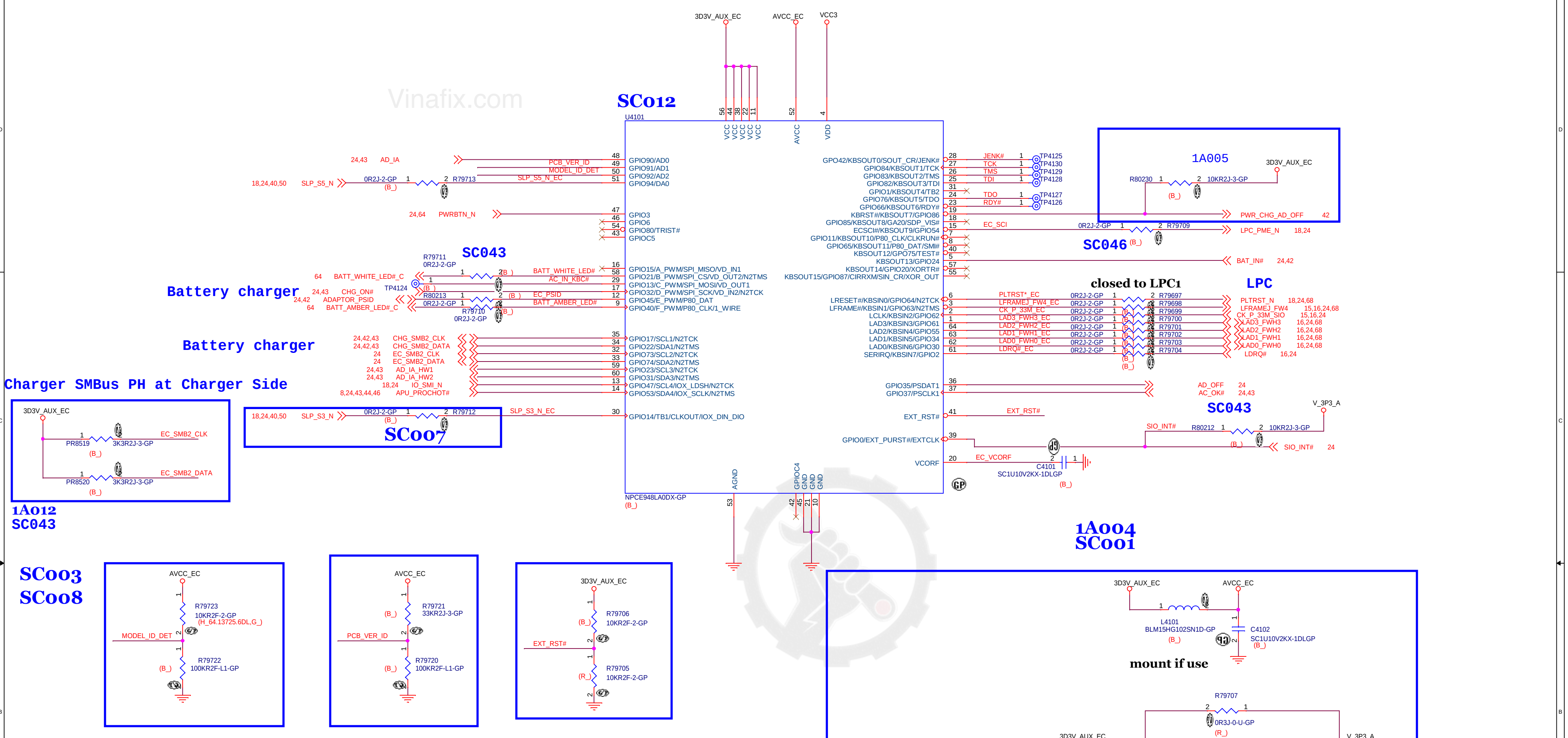
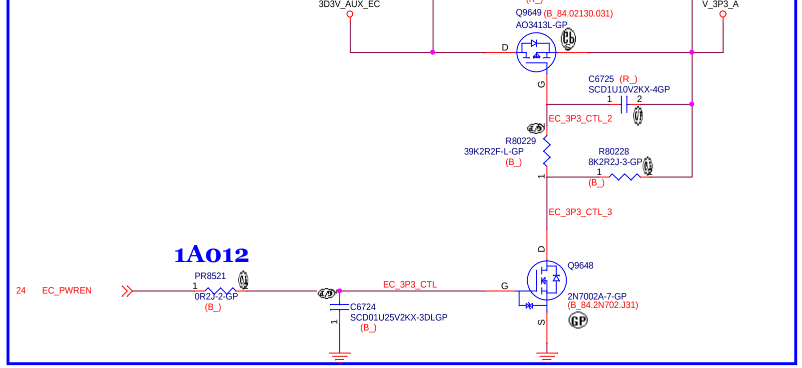
Title: 034_USB2.0 CONN		
Size: B	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 34 of 105	


USB 3.0
18 USBOC02*
16 USB30_TXP2
16 USB30_TXN2
16 USB30_TXP3
16 USB30_TXN3
16 USB30_RXP2
16 USB30_RXN2
16 USB30_RXP3
16 USB30_RXN3
16 F_USB6P
16 F_USB6N
16 F_USB7P
16 F_USB7N
USB_Power...Side1
0717 Eric modify for down size
0730 Eric delete TC2
0604 Eric modify
0811 modfiy for BOM
0807 Eric modify net name
VCC5_USB
F14
POLYSW-2A6V-7-GP
R1729
1KR2J-1-GP
R1728
10KR2J-3-GP
R1727
15KR2F-GP
USBOC02*
C1756
SC1KP50V2KX-1GP
TC8
E100U16VM-47-GP
(09.1071D.F5L)
C104
SC10U10V5KX-2DLGP
C106
SCD1U16V2KX-3GP
USBVCC23
C105
SC10U10V5KX-2GP
0725 modify OC pin
0805 Eric modify TC8
0820 Eric change TC8 P/N
0822 Eric change TC8 P/N
0730 Eric unmount
SC058
Side USB 3.0
SSUSB1
USBVCC23
USBP6N_EXT
USBP6P_EXT
VBUS
D-
D+
SSRX-
SSRX+
SSTX-
SSTX+
GND
GND_DRAIN
SIDE_USB3_RX2-
SIDE_USB3_RX2+
SIDE_USB3_TX2-
SIDE_USB3_TX2+
SKT-USB11-112-GP-U
(022.10005.01J1)
SSUSB2
USBP7N_EXT
USBP7P_EXT
SIDE_USB3_RX3-
SIDE_USB3_RX3+
SIDE_USB3_TX3-
SIDE_USB3_TX3+
ESD
0827 Eric modify for layout
0807 Eric modify net name
D4
USBP7P_EXT
USBP7N_EXT
USBP6P_EXT
USBP6N_EXT
C1753
SCD1U16V2KX-3DLGP
IP4223CZ6-1-GP
(75.04285.07C)
U3
LINE_1 LINE_2 GND LINE_3 LINE_4
NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP
U5
AZ1045-04F-R7G-GP
EMI
USB30_TXN2 C91 SCD1U16V2KX-3DLGP USB3_TX2_EMI_DN
USB30_TXP2 C1757 SCD1U16V2KX-3DLGP USB3_TX2_EMI_DP
USB30_TXN3 C113 SCD1U16V2KX-3DLGP USB3_TX3_EMI_DN
USB30_TXP3 C111 SCD1U16V2KX-3DLGP USB3_TX3_EMI_DP
EMI
L56
USB3_TX3_EMI_DN
USB3_TX3_EMI_DP
SIDE_USB3_TX3-
SIDE_USB3_TX3+
(66.R0036.04L)
FILTER-4P-123-GP
L57
USB30_RXN3
USB30_RXP3
SIDE_USB3_RX3-
SIDE_USB3_RX3+
L4
USB3_TX2_EMI_DP
USB3_TX2_EMI_DN
SIDE_USB3_TX2+
SIDE_USB3_TX2-
L5
USB30_RXP2
USB30_RXN2
SIDE_USB3_RX2+
SIDE_USB3_RX2-
TR3
F_USB6P
F_USB6N
USBP6P_EXT
USBP6N_EXT
FILTER-4P-137-GP
(068.01012.2011)
SC011
TR4
F_USB7P
F_USB7N
USBP7P_EXT
USBP7N_EXT
FILTER-4P-137-GP
(068.01012.2011)
SC011
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
035_USB3.0 CONN
Size C
Document Number
Rosa_Carrizo AIO
Rev -1
Date: Tuesday, August 09, 2016
Sheet 35 of 105





PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage
SA	100.0 K	10.0 K	3.000 V
SB	100.0 K	20.0 K	2.750 V
SC	100.0 K	33.0 K	2.481 V
-1	100.0 K	47.0 K	2.245 V

MOEDL_ID_DET	Pull-Low Register	Pull-High Register	Typical Voltage
Carrizo GPU	100.0 K	10.0 K	3.000 V
Carrizo UMA	100.0 K	13.7 K	2.902 V
Braswell GPU	100.0 K	57.6 K	2.094 V
Braswell UMA	100.0 K	64.9 K	2.001 V
SKL-U GPU	100.0 K	154.0 K	1.299 V
SKL-U UMA	100.0 K	200.0 K	1.100 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

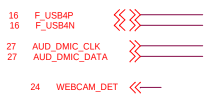
Title: 036_EC_NPCE948L

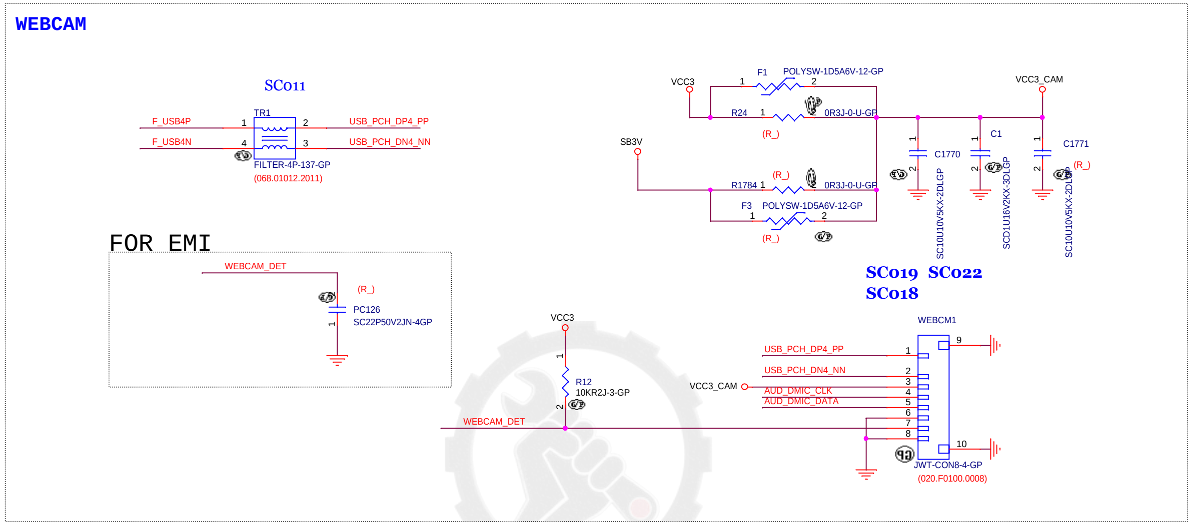
Size: C | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 36 of 105

Blanking

WEBCAM





<Core Design>

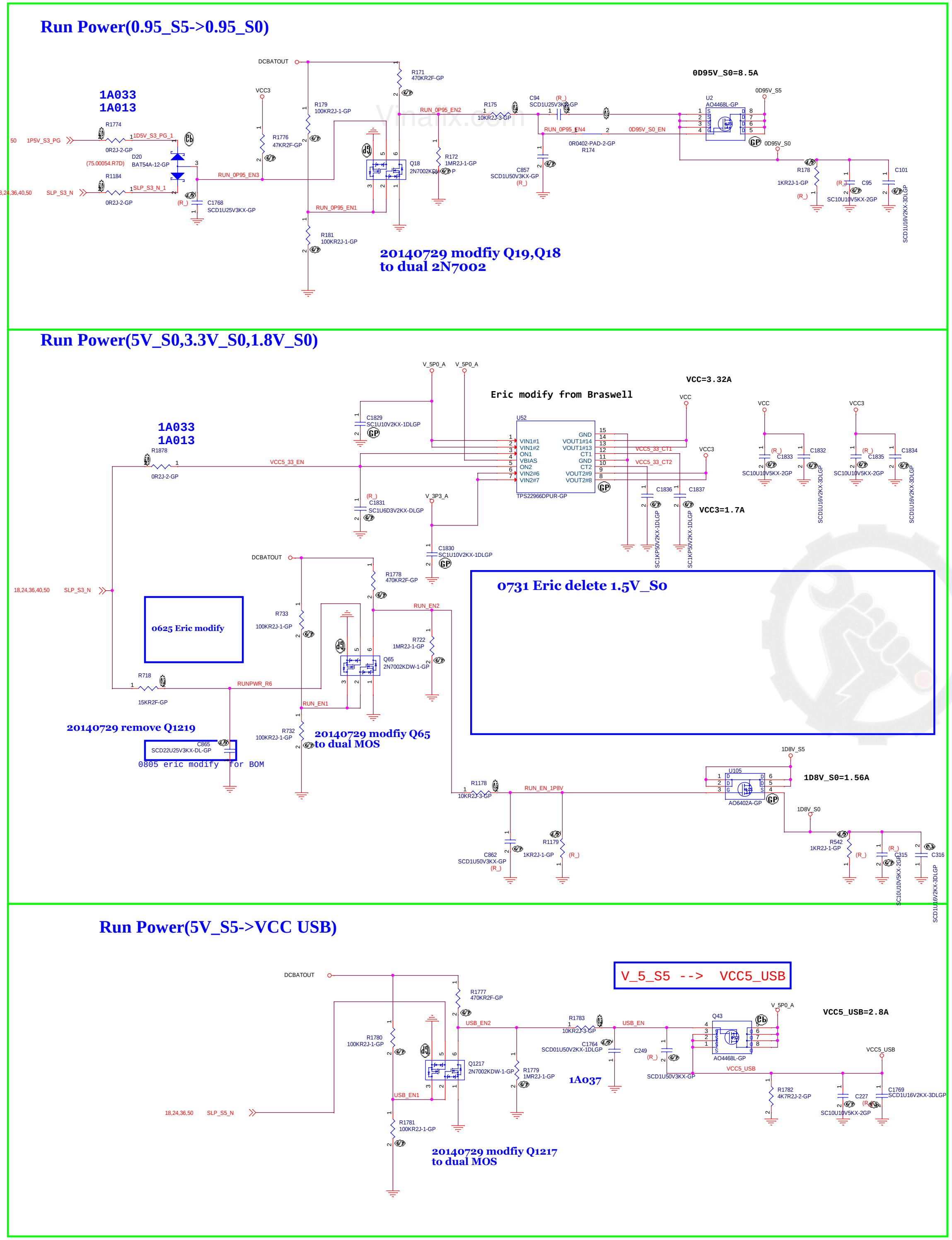
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	038_WEBCAM	
Size C	Document Number: Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 38 of 105	

Blanking

<Core Design>

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title			
Size: A	Document Number: Rosa_Carrizo AIO		Rev: -1
Date: Tuesday, August 09, 2016	Sheet 39	of 105	

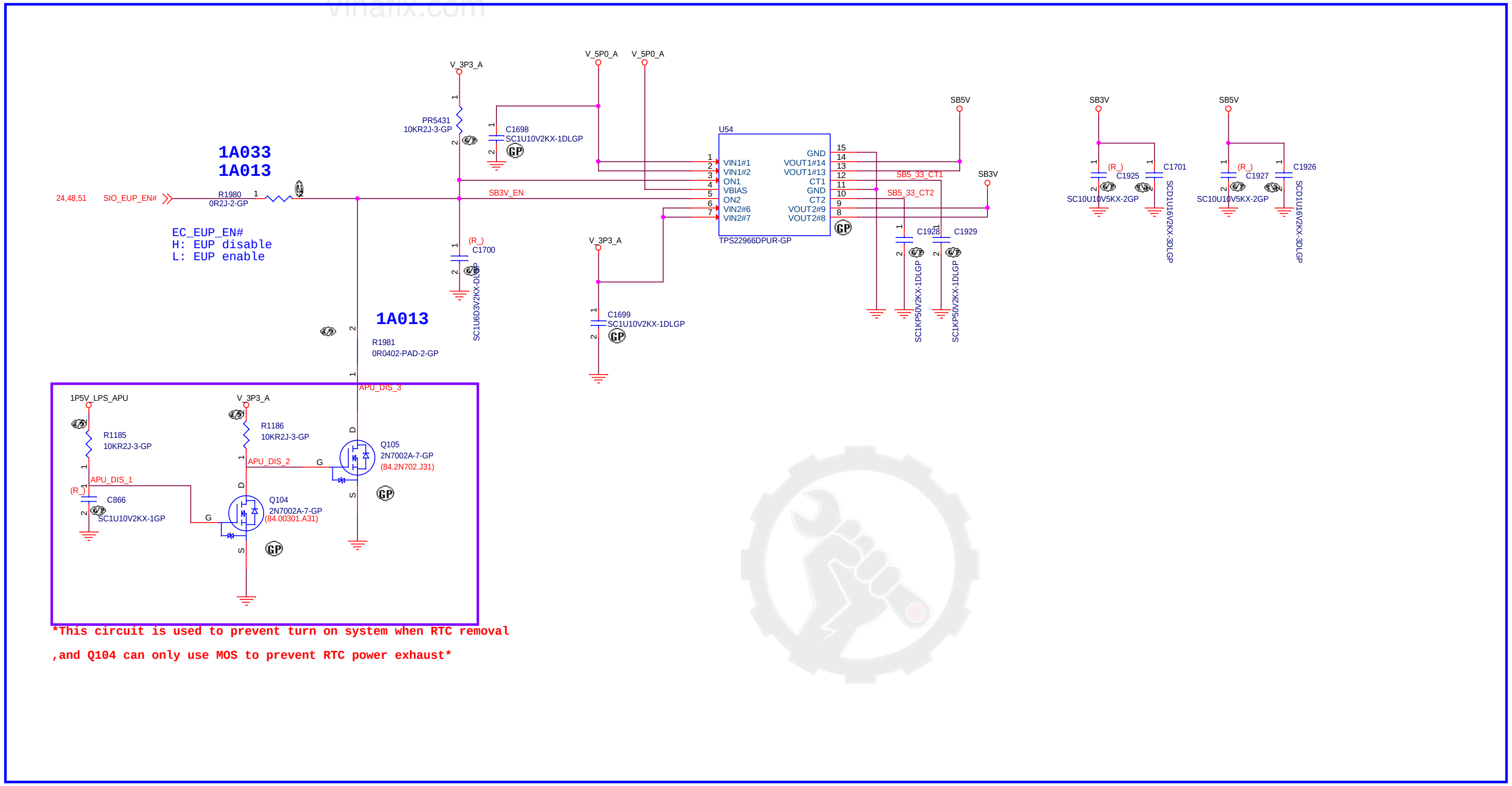


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

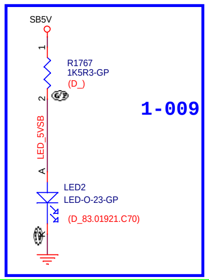
Title	040_Run PWR/USB PWR	
Size Custom	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 40 of 105	

0618 Eric modfiy from Braswell
EUP Power



This circuit is used to prevent turn on system when RTC removal ,and Q104 can only use MOS to prevent RTC power exhaust

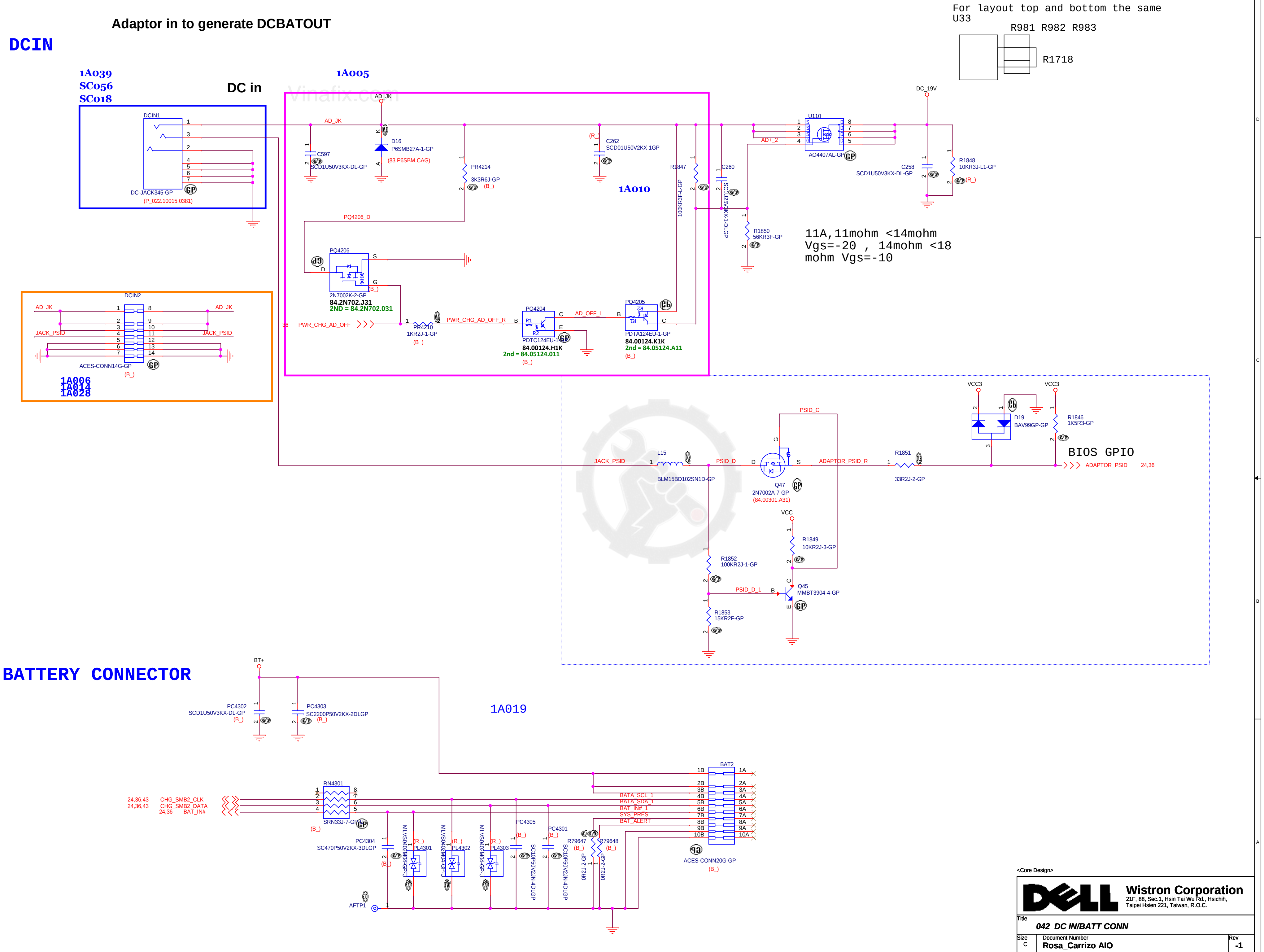
VCC5SB LED



<Core Design>

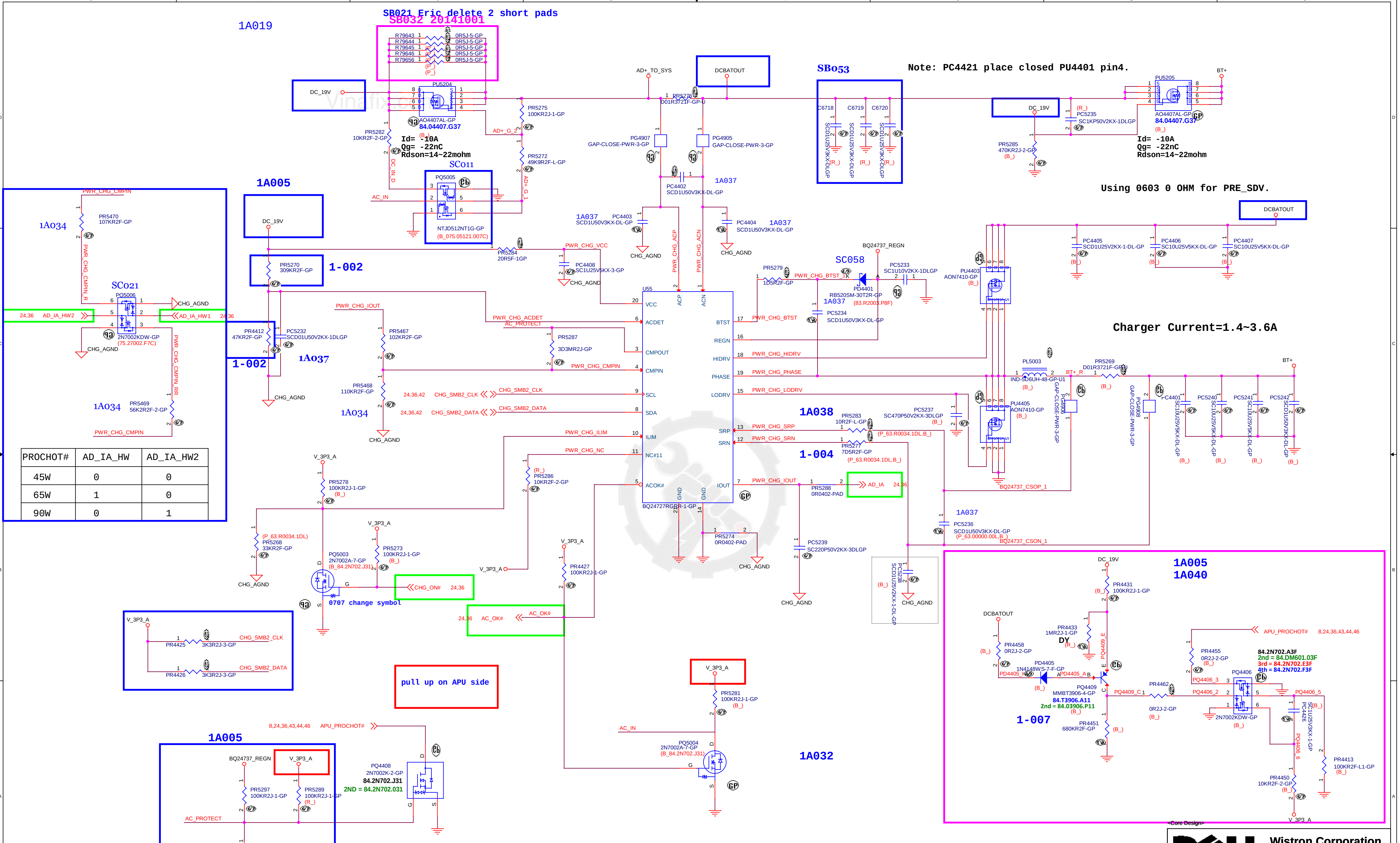
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	041_DSW_POWER_CTL
Size	C
Document Number	Rosa_Carrizo AIO
Rev	-1
Date	Tuesday, August 09, 2016
Sheet	41 of 105



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	042_DC IN/BATT CONN
Size C	Document Number: Rosa_Carrizo AIO
Rev	-1
Date: Tuesday, August 09, 2016	Sheet 42 of 105



PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 043_CHARGER

Size: Custom | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 43 of 105

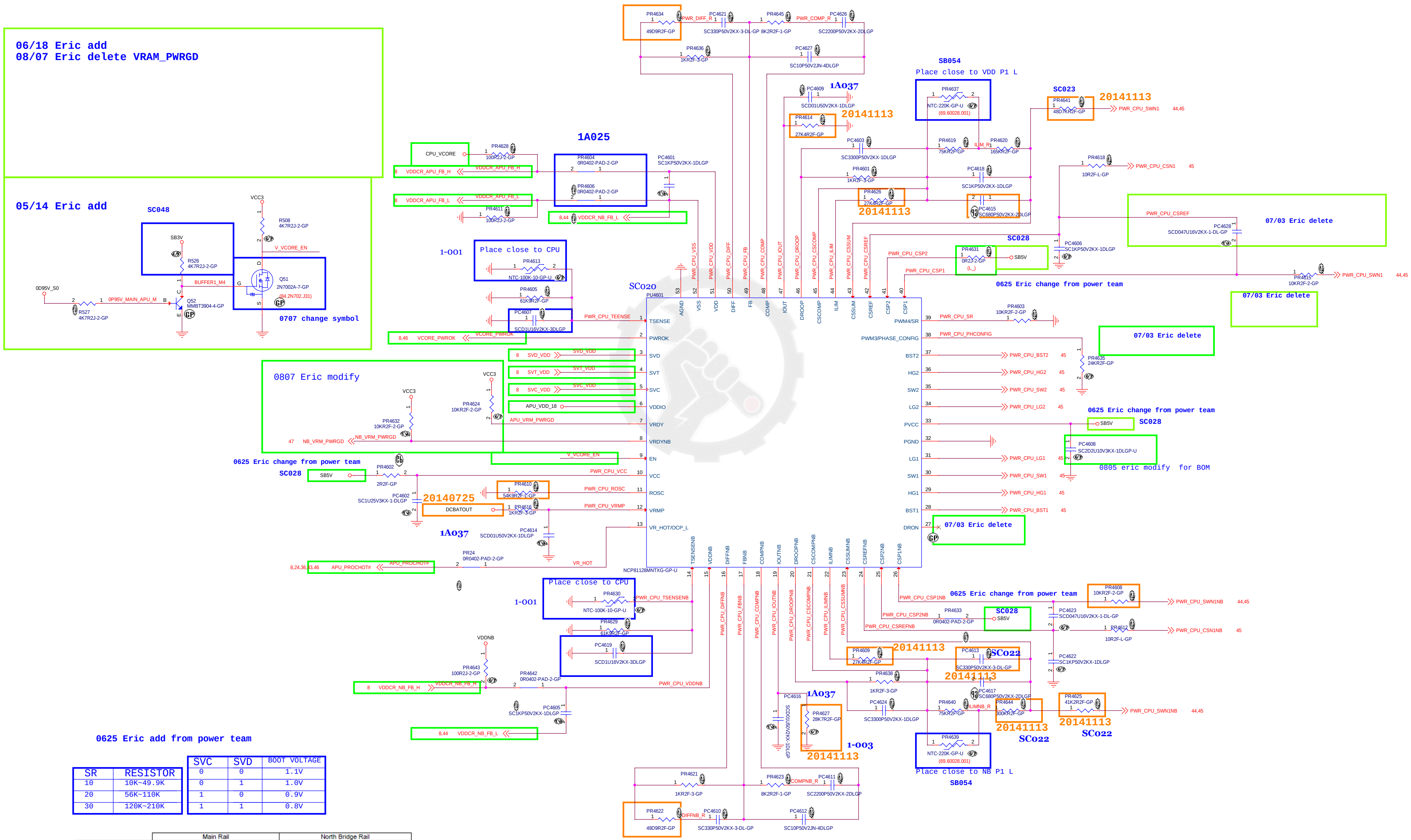
07/03 Eric modify from power team

power team

EE

DCBATOUT--> VDDNB

DCBATOUT--> CPU_VCORE



0625 Eric add from power team

SR	RESISTOR
10	10K~49.9K
20	56K~110K
30	120K~210K

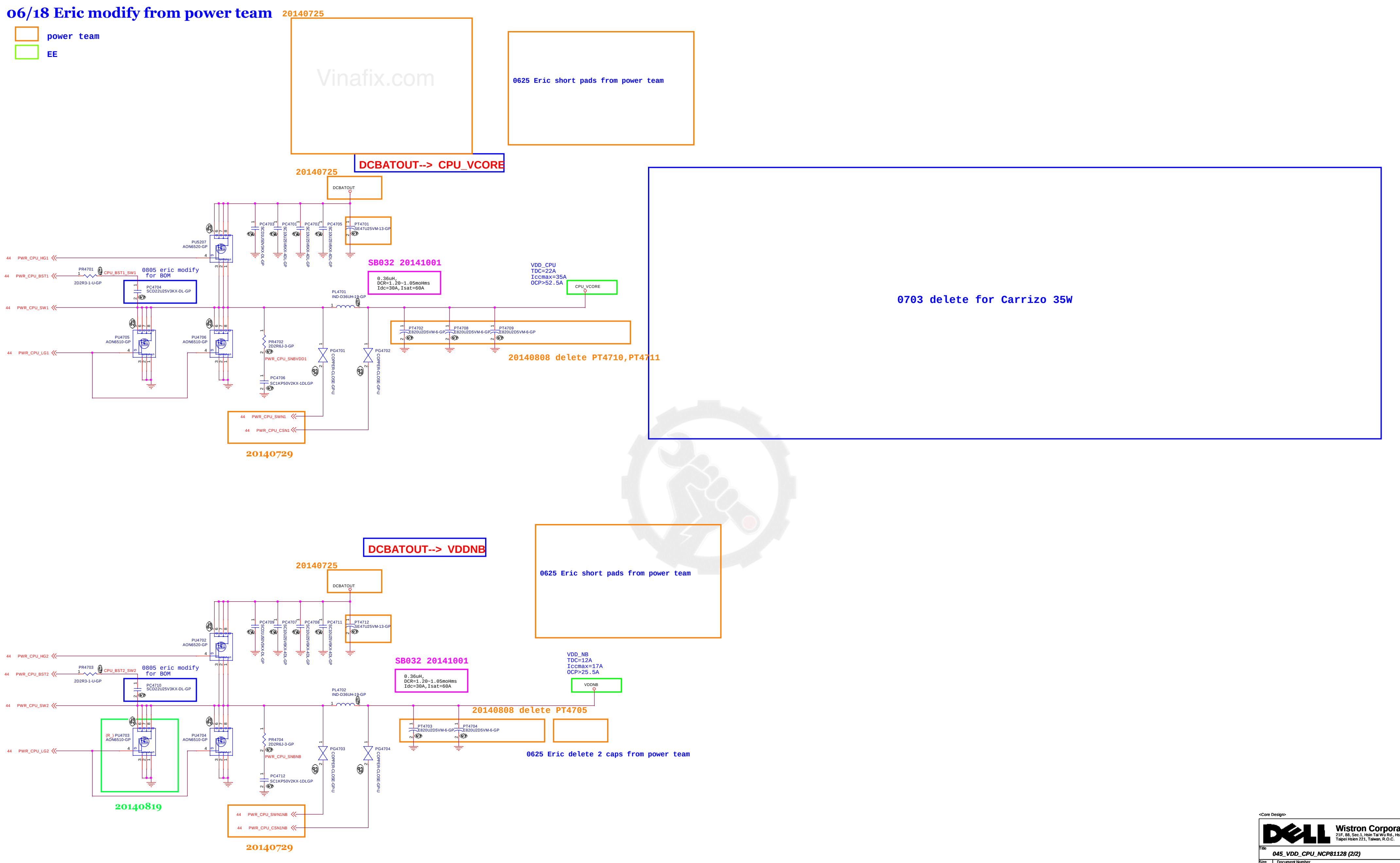
SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

		Main Rail		North Bridge Rail	
Config	Resistor value	Phase 1	Phase 2	Phase 1	Phase 2
1	220k/open	SW1,HG1,BST1,LG1	SW2, HG2,BST2,LG2	PWM3	PWM4
2	130k	PWM3	SW1,HG1,BST1,LG1	PWM4	SW2, HG2,BST2,LG2
3	75k	PWM3	PWM4	SW1,HG1,BST1,LG1	SW2, HG2,BST2,LG2
4	24k	SW1,HG1,BST1,LG1	PWM3	SW2, HG2,BST2,LG2	PWM4

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	044_VDD_CPU_NCP81128 (1/2)	
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 44 of 105	



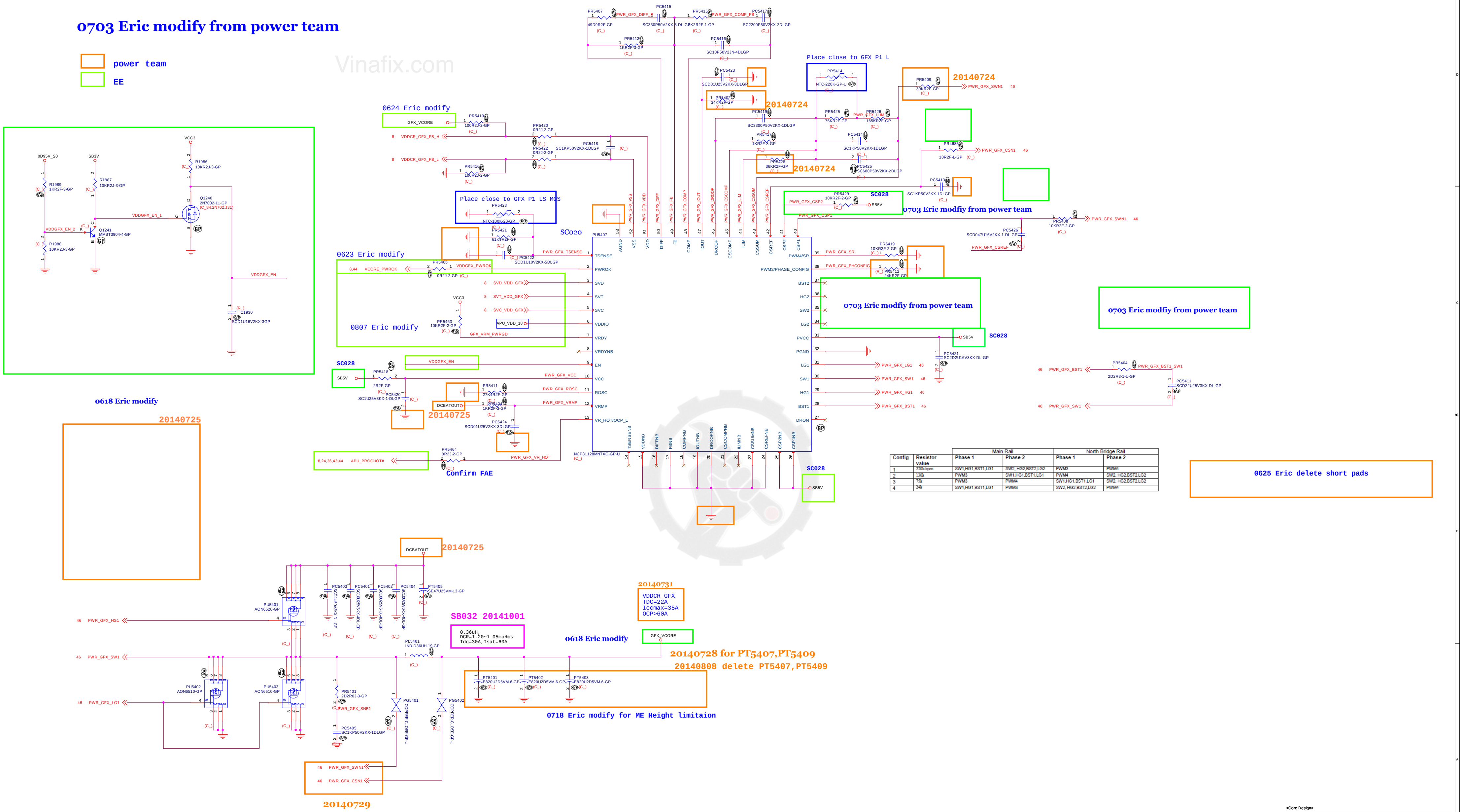
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	045_VDD_CPU_NCP81128 (2/2)
Size	D
Document Number	Rosa_Carrizo AIO
Rev	-1
Date:	Tuesday, August 09, 2016
Sheet	45 of 105

0703 Eric modify from power team

power team
EE



Config	Resistor value	Main Rail Phase 1	Main Rail Phase 2	North Bridge Rail Phase 1	North Bridge Rail Phase 2
1	220k/open	SW1,HG1,BST1,LG1	SW2, HG2,BST2,LG2	PWM3	PWM4
2	130k	PWM3	SW1,HG1,BST1,LG1	PWM4	SW2, HG2,BST2,LG2
3	75k	PWM3	PWM4	SW1,HG1,BST1,LG1	SW2, HG2,BST2,LG2
4	24k	SW1,HG1,BST1,LG1	PWM3	SW2, HG2,BST2,LG2	PWM4

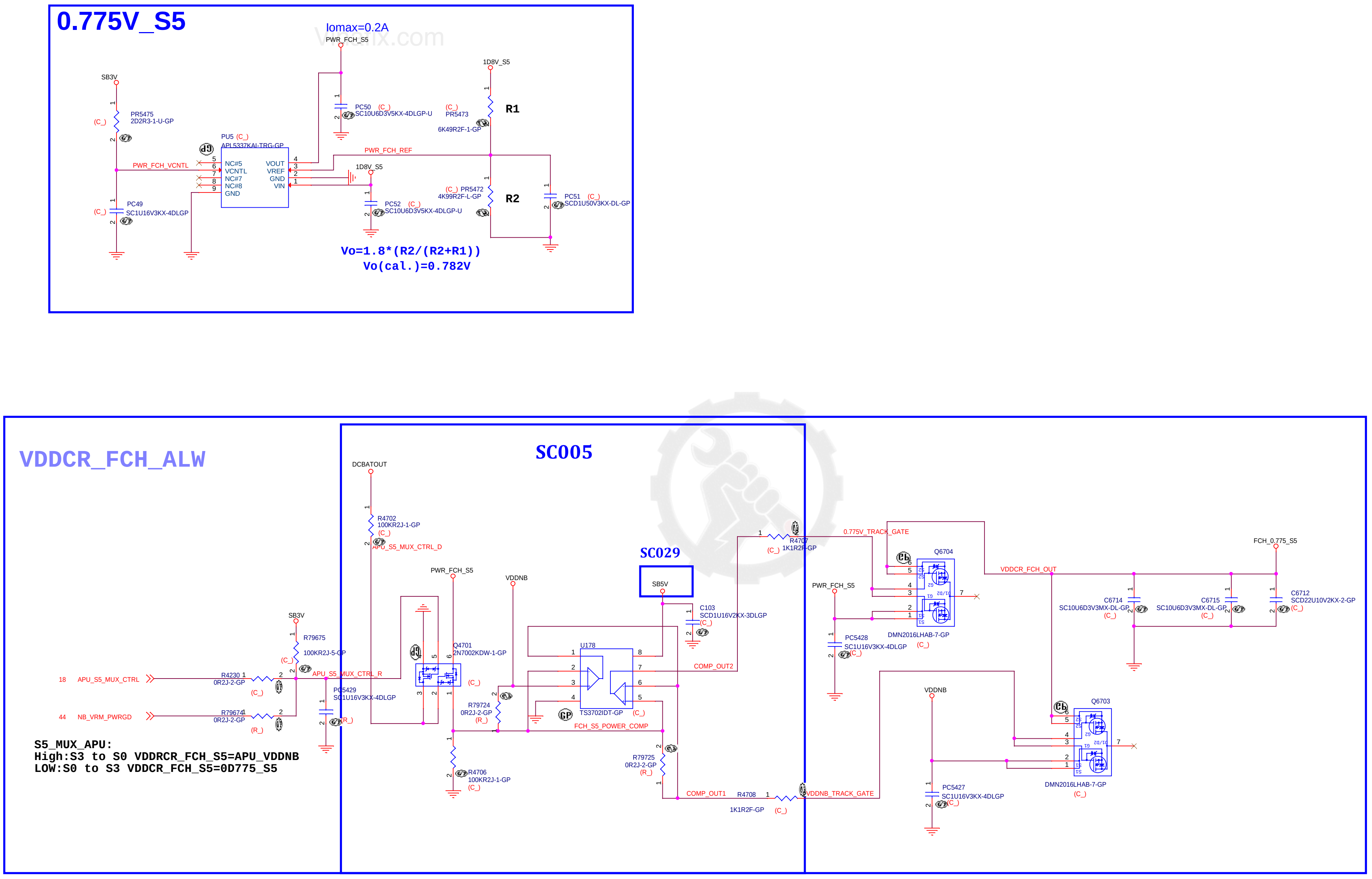
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 046. VDDCR_GFX
Size: D | Document Number: Rosa_Carrizo AIO | Rev: -1
Date: Tuesday, August 09, 2016 | Sheet 46 of 105

V_1P8_S5 --> V_0P775_S5

0807 Eric modify



S5_MUX_APU:
High:S3 to S0 VDDRCR_FCH_S5=APU_VDDNB
LOW:S0 to S3 VDDCR_FCH_S5=0D775_S5

<Core Design>

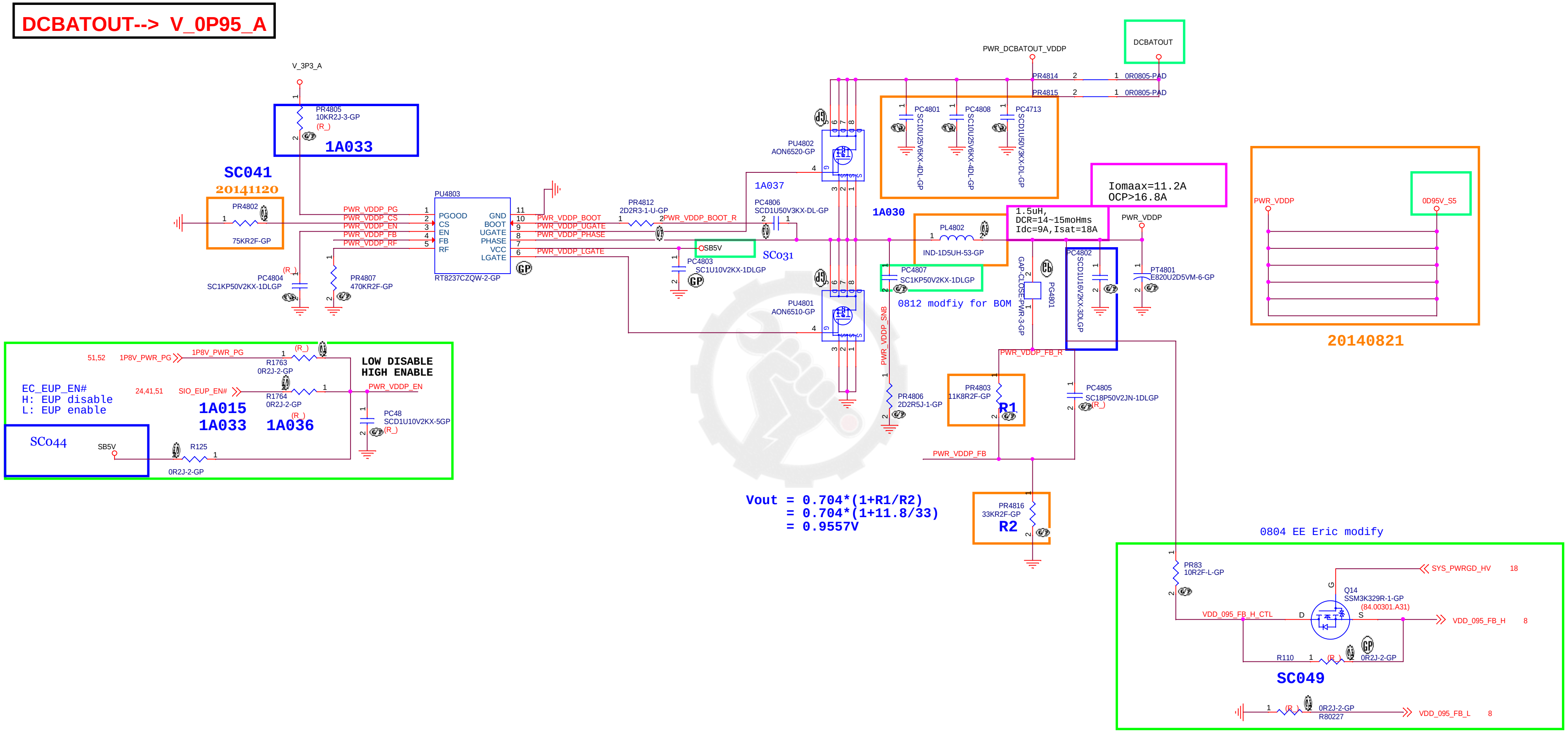
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 047_VDDCR_FCH_S5		
Size: C	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 47 of 105	

05/26 Eric modify from power team

power team

EE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	048_VDDP_0D95V(RT8237C)	
Size C	Document Number: Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 48 of 105	

05/26 Eric modify from power team

- power team
- EE

DCBATOUT--> V_3P3_A

DCBATOUT--> V_5P0_A

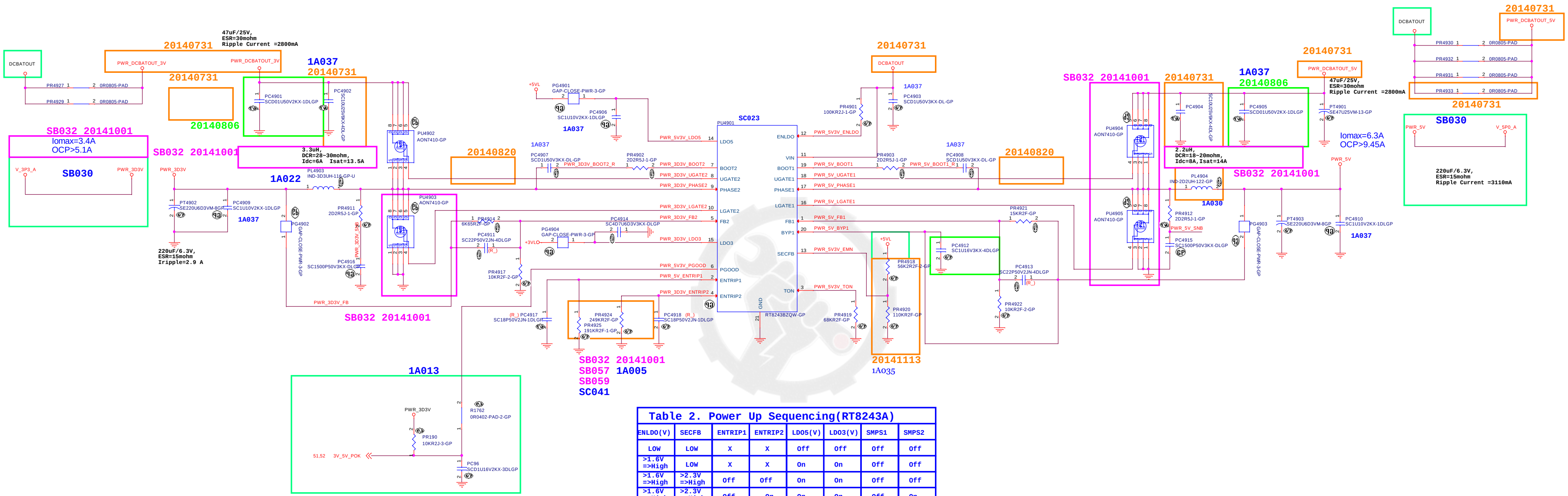


Table 2. Power Up Sequencing(RT8243A)							
ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

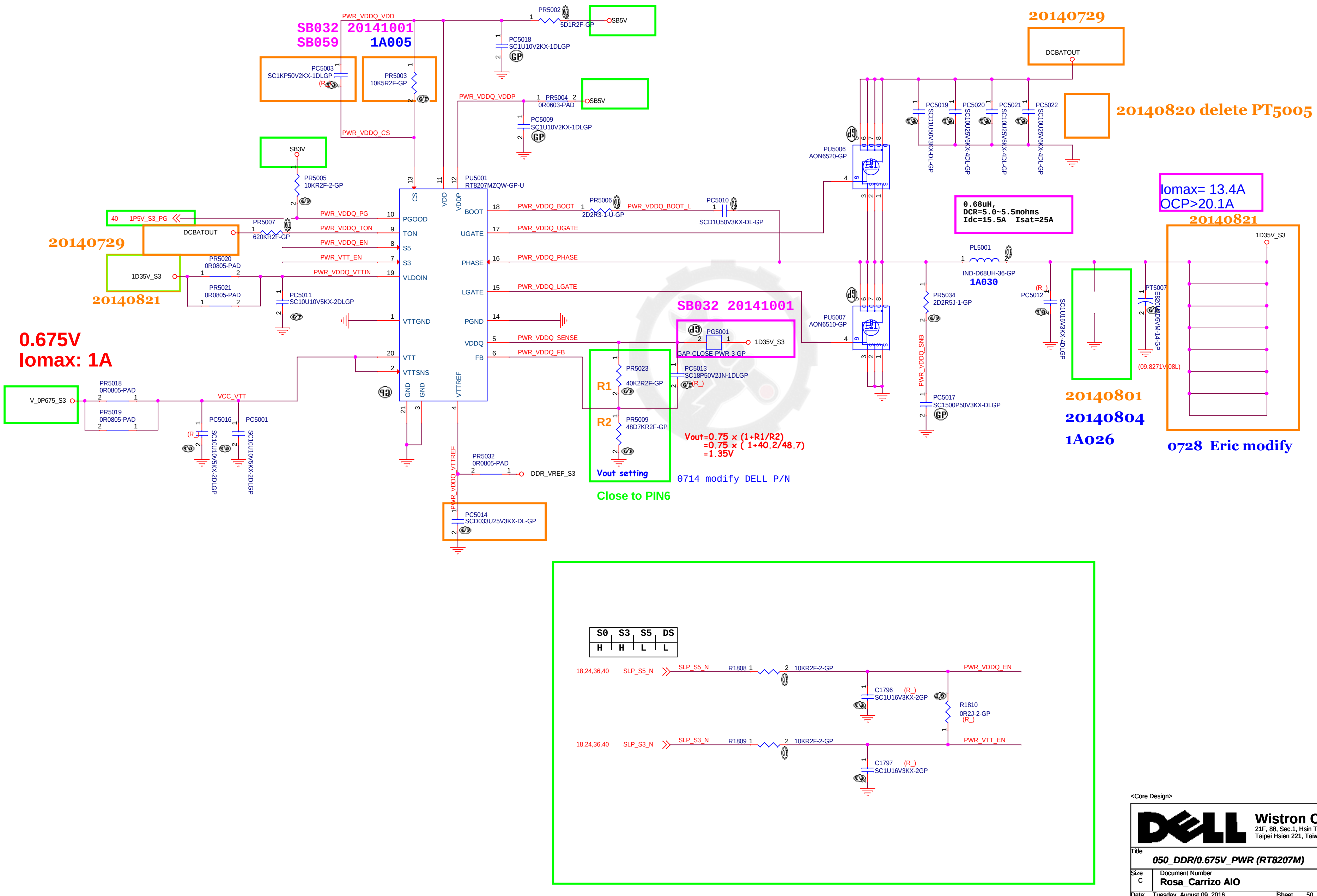
<Core Design>
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 049_5V & 3.3V(RT8243A)
Size: D Document Number: Rosa_Carrizo AIO Rev: -1
Date: Tuesday, August 09, 2016 Sheet 49 of 105

05/26 Eric modify from power team

DCBATOUT--> V_1P35_S3

power team

EE



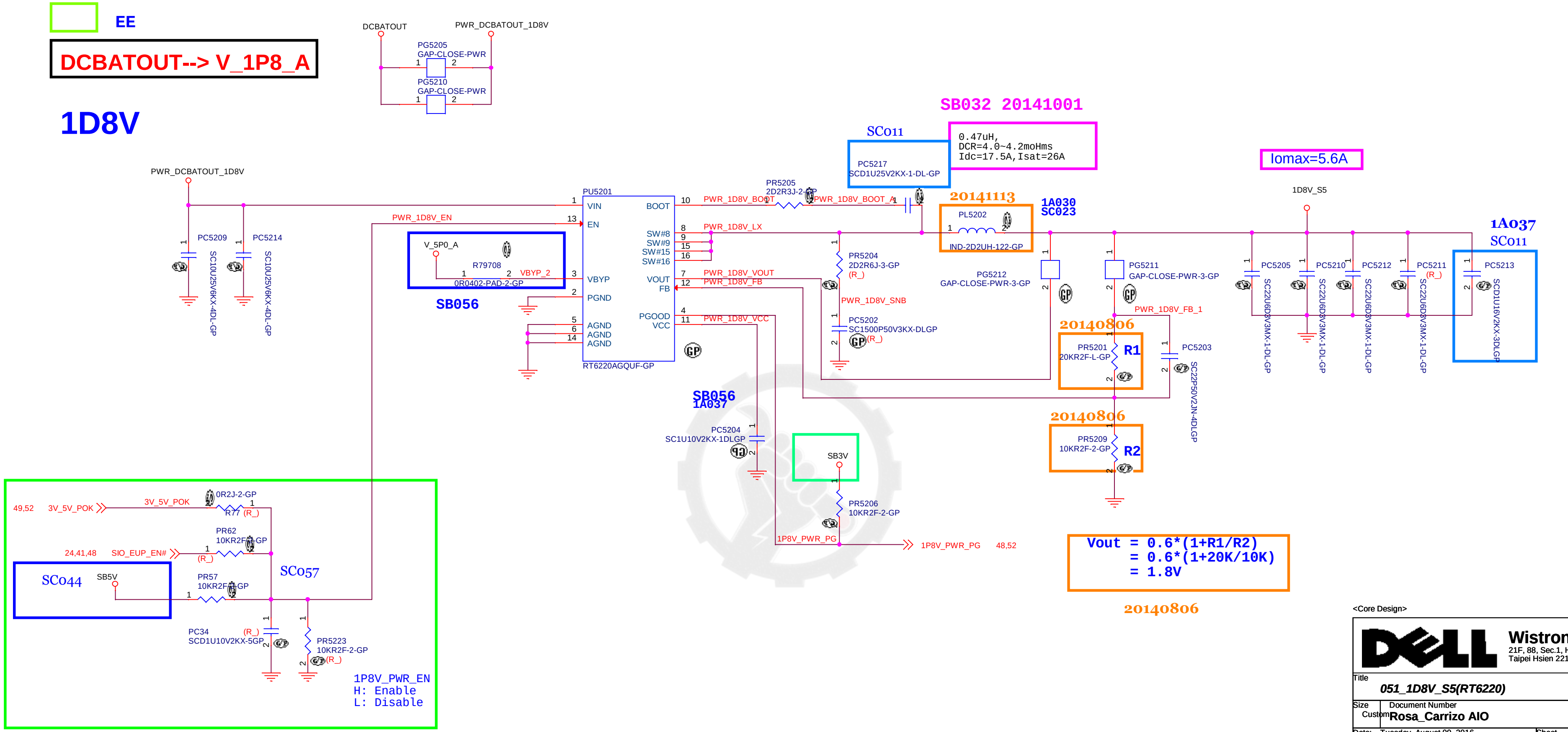
SB051 1009 Eric modify from power team

power team

EE

DCBATOUT--> V_1P8_A

1D8V



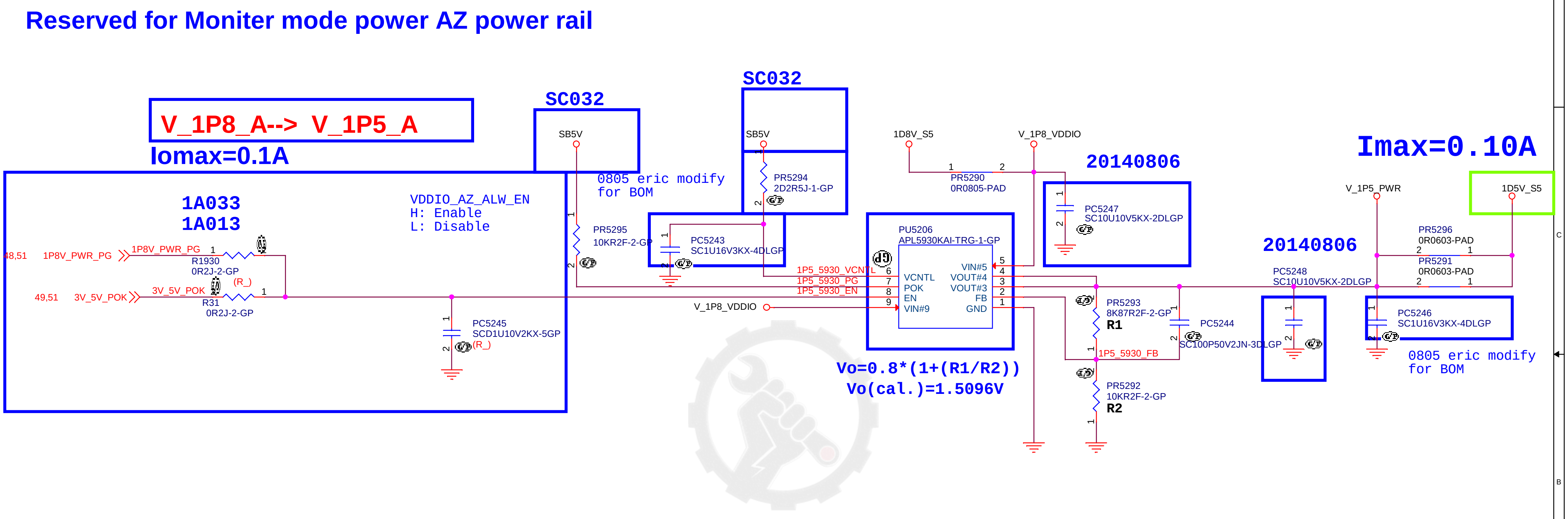
Vout = 0.6*(1+R1/R2)
= 0.6*(1+20K/10K)
= 1.8V

20140806

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	051_1D8V_S5(RT6220)
Size	Custom
Document Number	Rosa_Carrizo AIO
Rev	-1
Date:	Tuesday, August 09, 2016
Sheet	51 of 105



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	052_1D5V_S5(APL5930)	
Size B	Document Number: Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 52 of 105	

<Core Design>

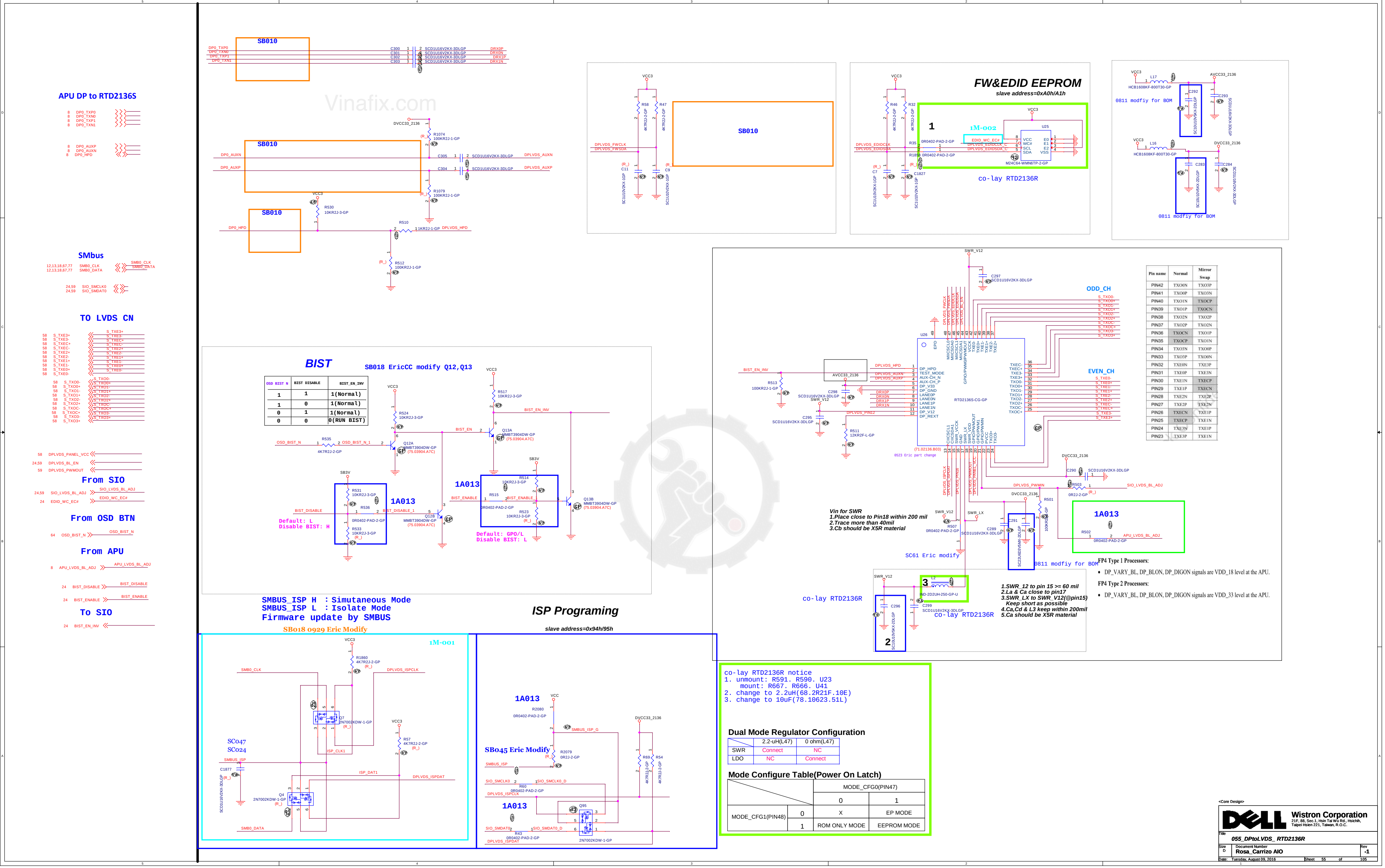
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size C	Document Number Rosa_Carrizo AIO	Rev -1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: D	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 54 of 105	



OSD_BIST_N	BIST_DISABLE	BIST_EN_INV
1	1	1(Normal)
1	0	1(Normal)
0	1	1(Normal)
0	0	0(RUN BIST)

Pin name	Normal	Mirror Swap
PIN42	TXO0N	TXO3P
PIN41	TXO0P	TXO3N
PIN40	TXO1N	TXOCP
PIN39	TXO1P	TXOCN
PIN38	TXO2N	TXO2P
PIN37	TXO2P	TXO2N
PIN36	TXOCN	TXO1P
PIN35	TXOCP	TXO1N
PIN34	TXO3N	TXO0P
PIN33	TXO3P	TXO0N
PIN32	TXE0N	TXE3P
PIN31	TXE0P	TXE3N
PIN30	TXE1N	TXECP
PIN29	TXE1P	TXECN
PIN28	TXE2N	TXE2P
PIN27	TXE2P	TXE2N
PIN26	TXECN	TXE1P
PIN25	TXECP	TXE1N
PIN24	TXE3N	TXE1P
PIN23	TXE3P	TXE1N

co-lay RTD2136R notice
1. unmount: R591. R590. U23
mount: R667. R666. U41
2. change to 2.2uH(68.2R21F.10E)
3. change to 10uF(78.10623.51L)

Dual Mode Regulator Configuration

	2.2-uH(L47)	0 ohm(L47)
SWR	Connect	NC
LDO	NC	Connect

Mode Configure Table(Power On Latch)

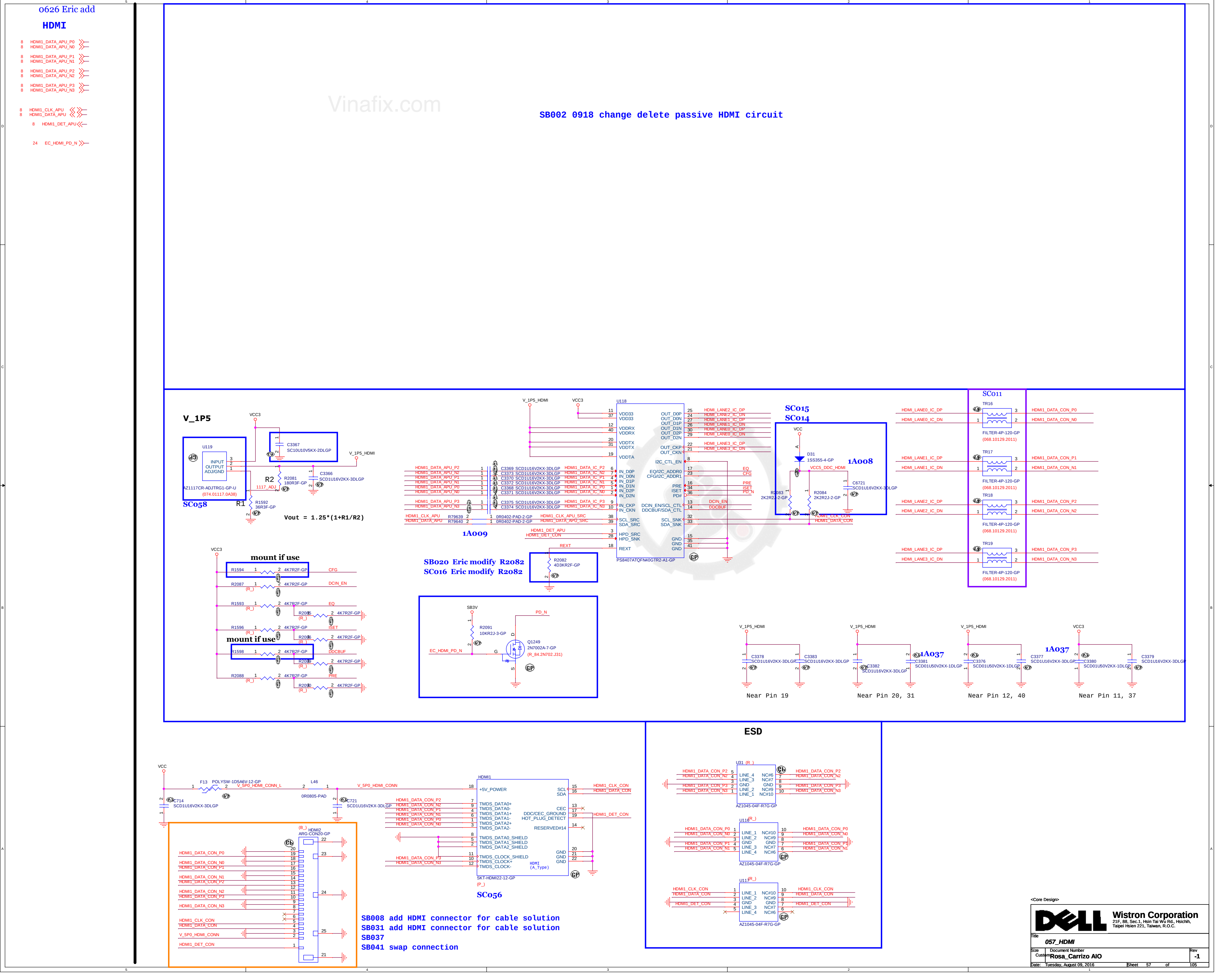
		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 055_DPtoLVDS_RTD2136R
Size: D | Document Number: Rosa_Carrizo AIO | Rev: -1
Date: Tuesday, August 09, 2016 | Sheet 55 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size D	Document Number **Rosa_Carrizo AIO**	Rev -1
Date: Tuesday, August 09, 2016	Sheet 56 of 105	



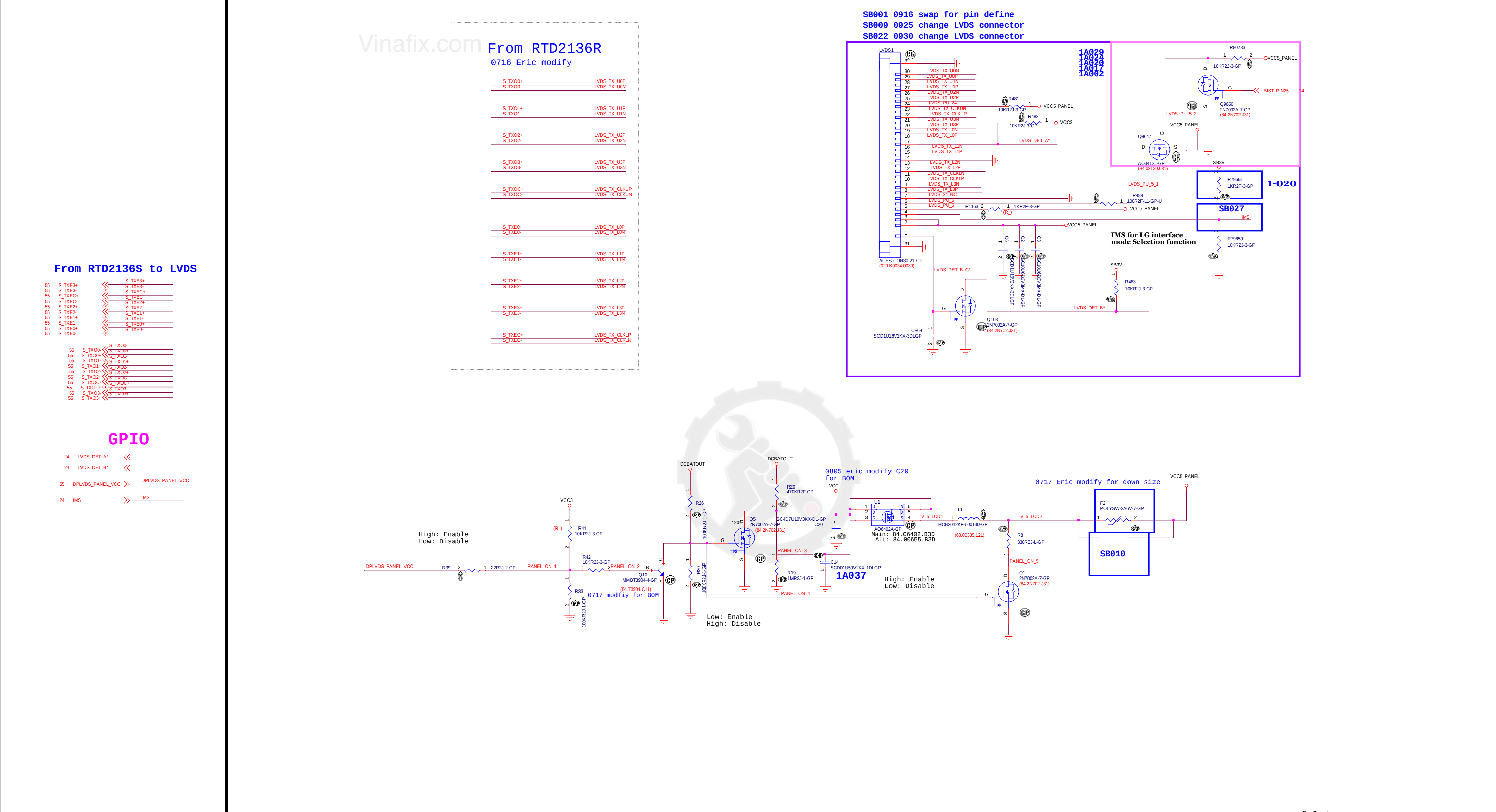
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 057_HDMI

Size: Custom | Document Number: Rosa_Carrizo AIO | Rev: -1

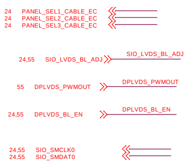
Date: Tuesday, August 09, 2016 | Sheet 57 of 105



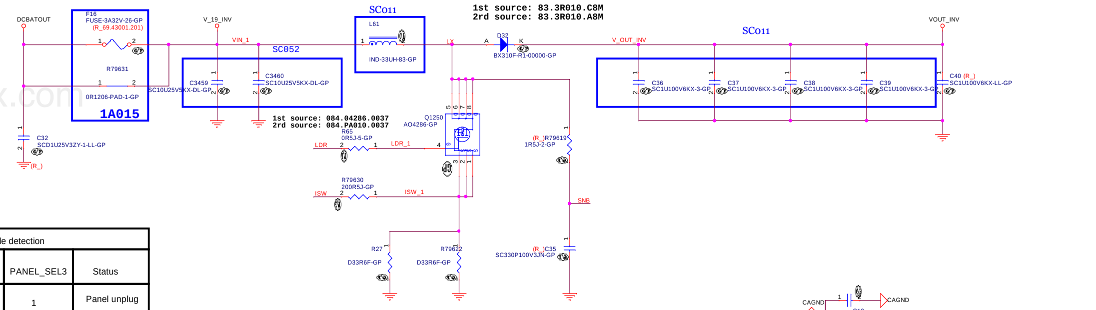
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

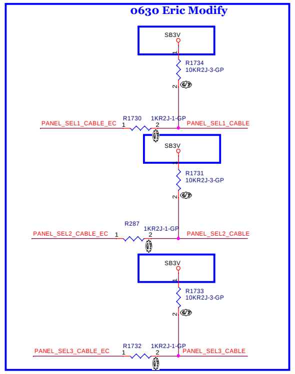
Title	058_Panel control	
Size Custom	Document Number Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 58 of 105	



0708 Ericc modify AGND



Cable detection			
PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug

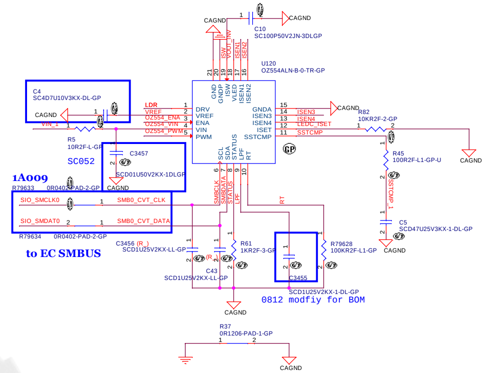


SC004

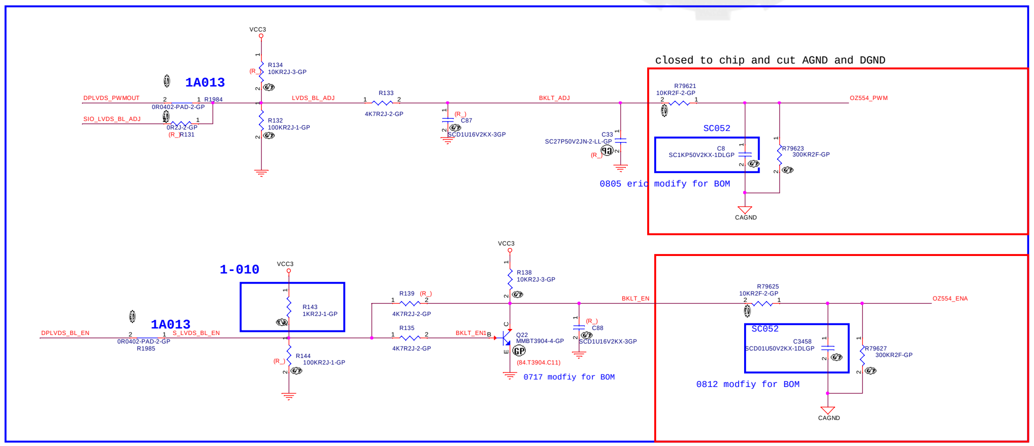
23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
LG	1	0	0	3,4 Vout 1,2,3 RTN
BOE	1	1	0	3,4 Vout 1,2,3 RTN
AUO	1	0	1	3,4 Vout 1,2,3,4 RTN

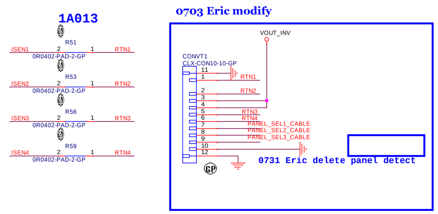
19.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
AUO	0	1	0	3,4 Vout 1,2,3,4 RTN
LG	0	0	1	3,4 Vout 1,2 RTN

21.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
LG	0	0	0	3,4 Vout 1,6 RTN
Sansung	0	1	1	2,3 Vout 1,4 RTN



1-019





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 059_OZ554A LED Converter

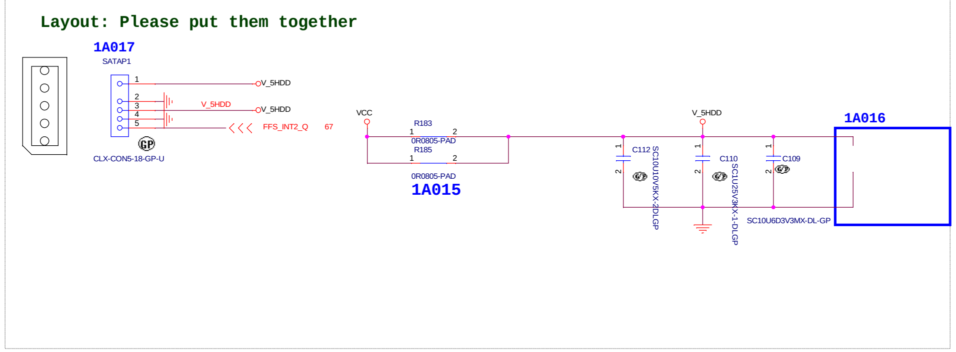
Size: D | Document Number: Rosa_Carrizo AIO | Rev: -1

Date: Tuesday, August 09, 2016 | Sheet 59 of 105

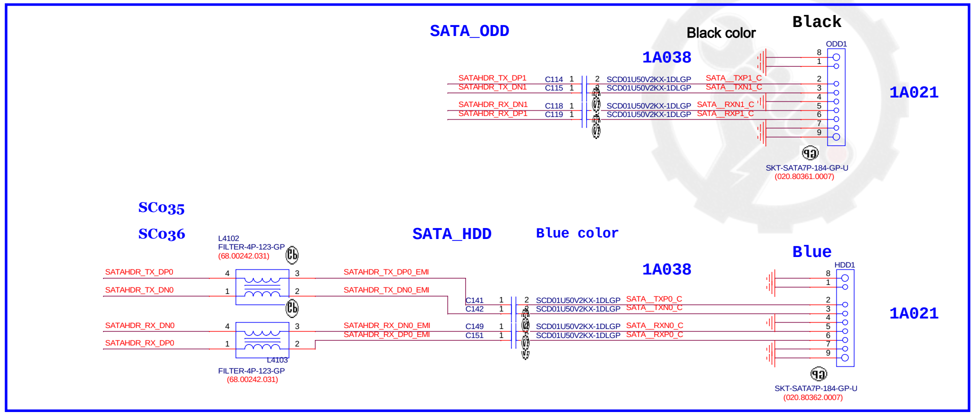
SATA

16 SATAHDR_RX_DP0
16 SATAHDR_RX_DN0
16 SATAHDR_TX_DN0
16 SATAHDR_TX_DP0
16 SATAHDR_RX_DP1
16 SATAHDR_RX_DN1
16 SATAHDR_TX_DN1
16 SATAHDR_TX_DP1

SATA



0811 Eric modfiy SATA connector
0725 Eric modfiy SATA connector



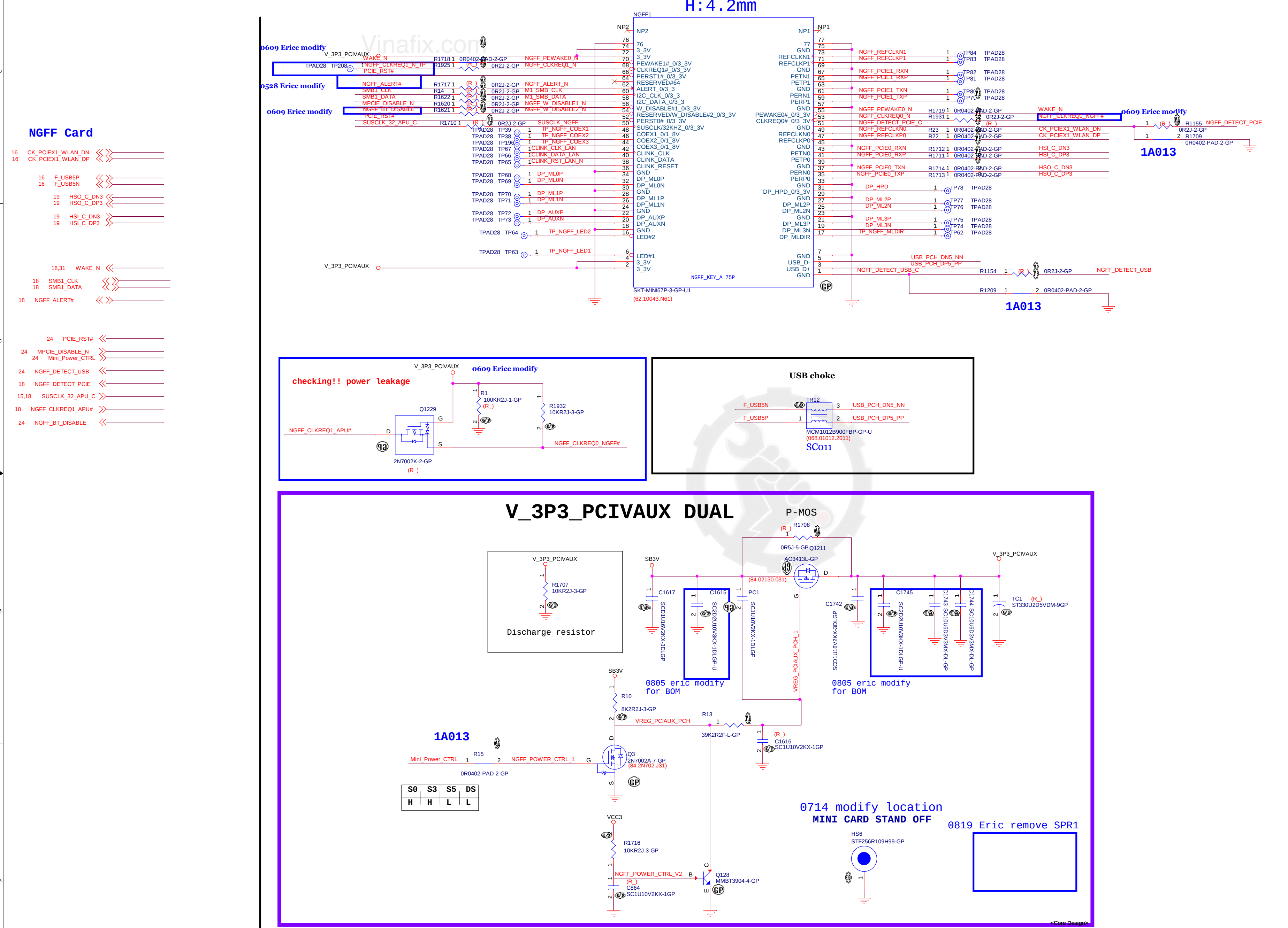
<Core Design>

DELL

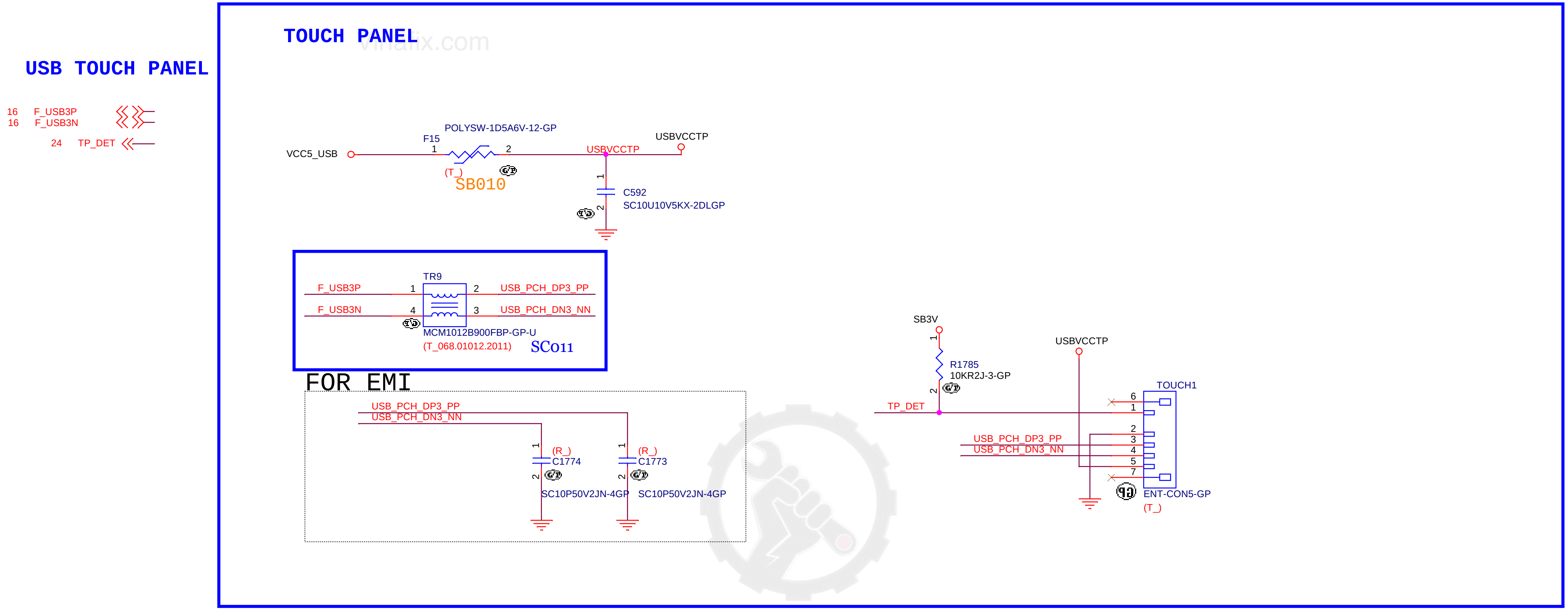
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	060_HDD/ODD	
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
Date: Tuesday, August 09, 2016	Sheet 60 of 105	

NGFF(A Key)



S0	S3	S5	DS
H	H	L	L



<Core Design>

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Title: *062_TOUCH*

Size: B | Document Number: **Rosa_Carrizo AIO** | Rev: **-1**

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<Core Design>

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Title		
Size A4	Document Number Rosa_Carrizo AIO	Rev -1
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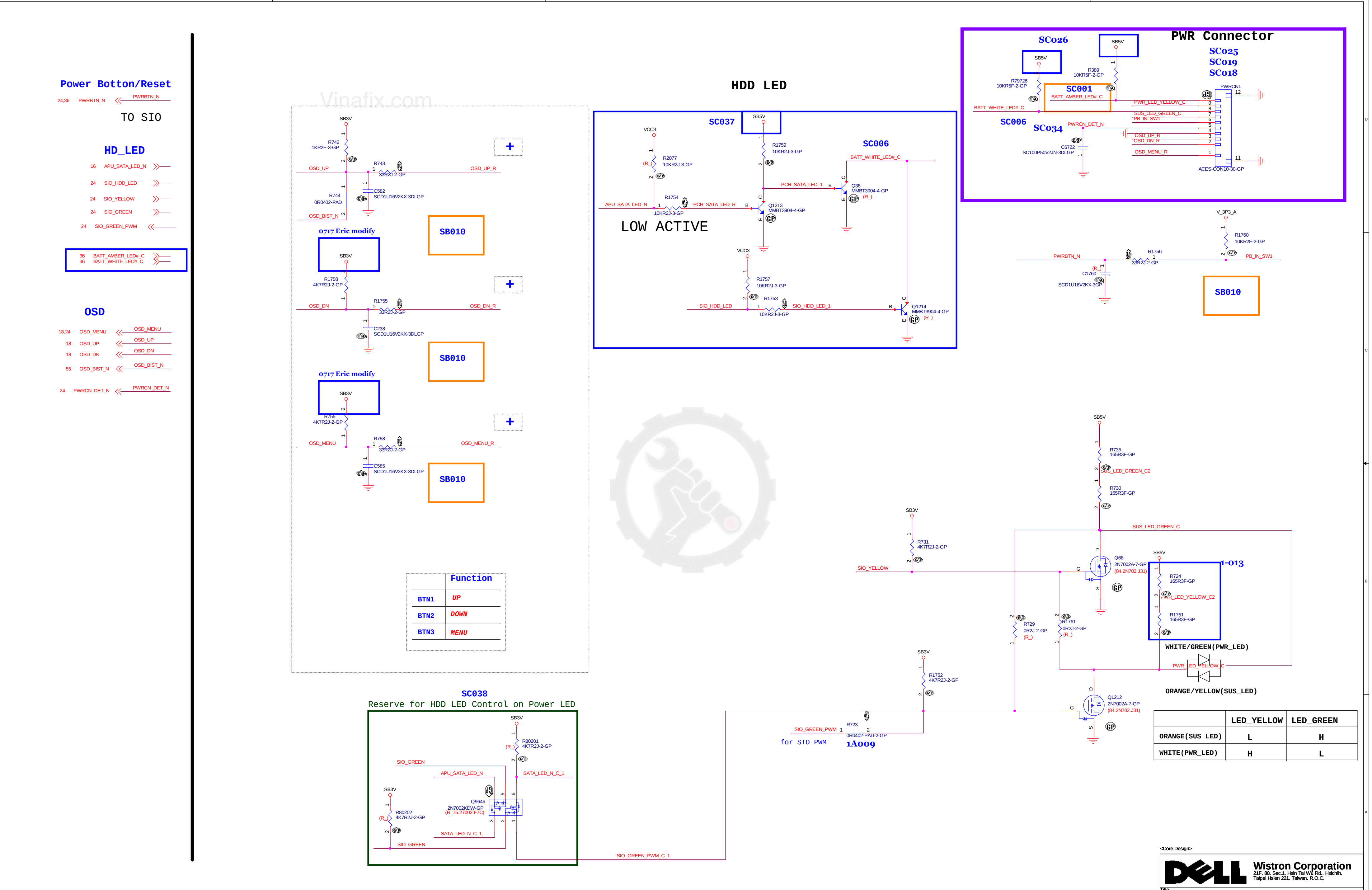

	Function
BTN1	UP
BTN2	DOWN
BTN3	MENU

	LED_YELLOW	LED_GREEN
ORANGE(SUS_LED)	L	H
WHITE(PWR_LED)	H	L

<Core Design>

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Title: 064_LED Board/Power button

Size: Custom | Document Number: Rosa_Carrizo AIO | Rev: -1

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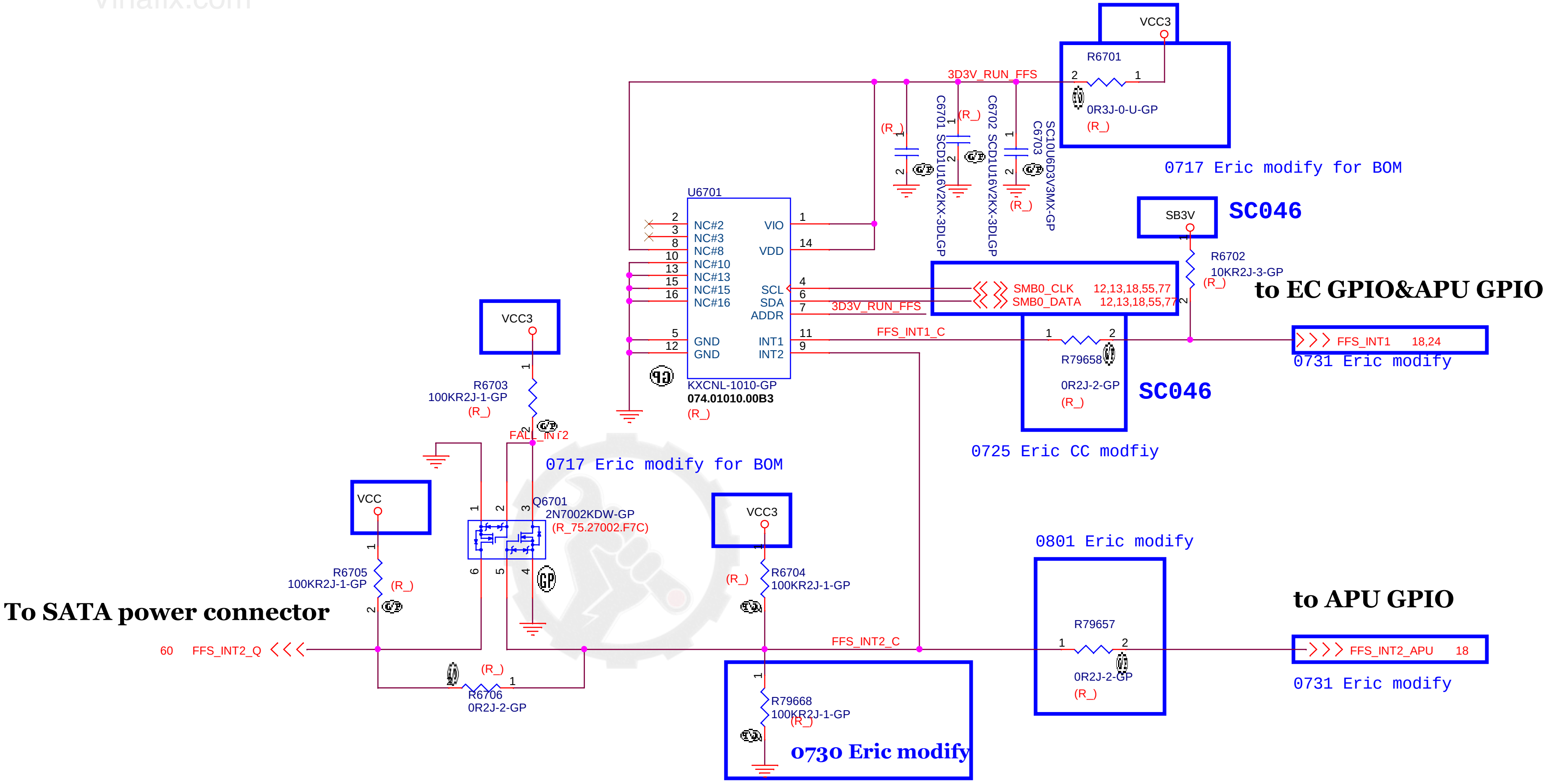
Free Fall Sensor

0716 modfiy from PLANO



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title	067_FFS(NEW)	
Size B	Document Number Rosa_Carrizo AIO	Rev -1
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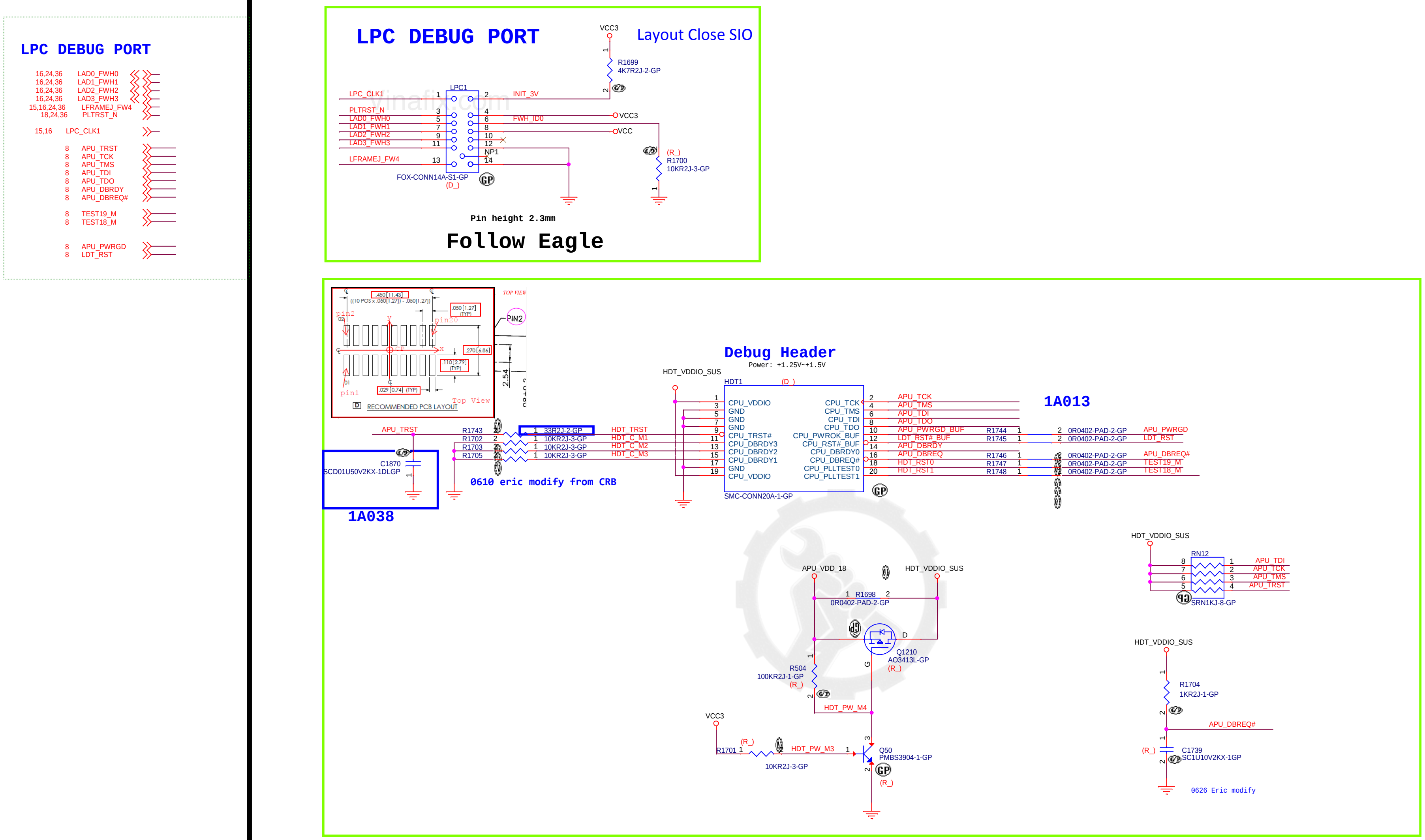

<Core Design>

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Title	068_DEBUG/HDT	
Size: C	Document Number: Rosa_Carrizo AIO	Rev: -1
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5 4 3 2 1

D C B A

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Size A4	Document Number **Rosa_Carrizo AIO**	Rev **-1**
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Title		
Size A4	Document Number **Rosa_Carrizo AIO**	Rev **-1**
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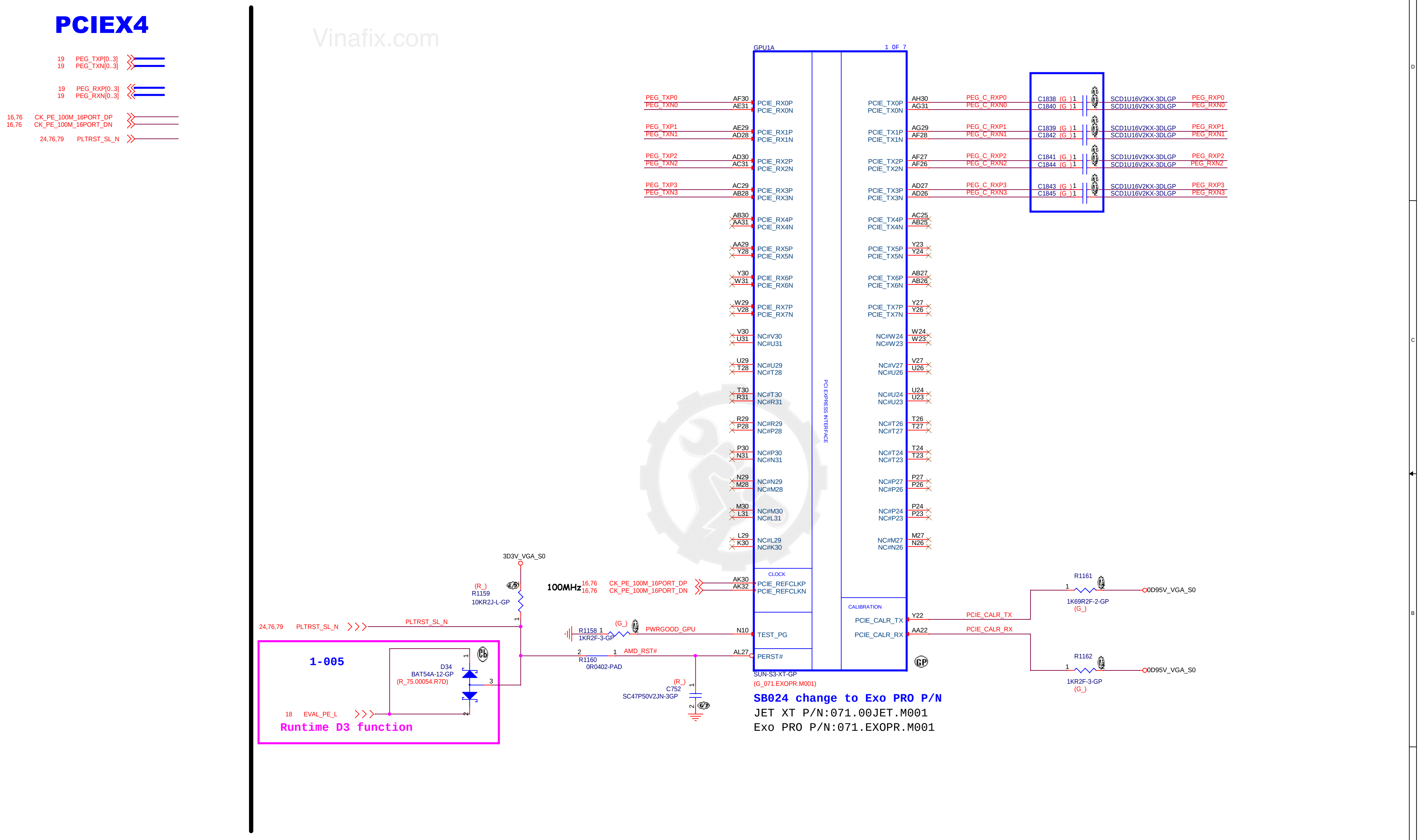

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Title	076_GPU Exo PCIE	
Size C	Document Number: Rosa_Carrizo AIO	Rev -1
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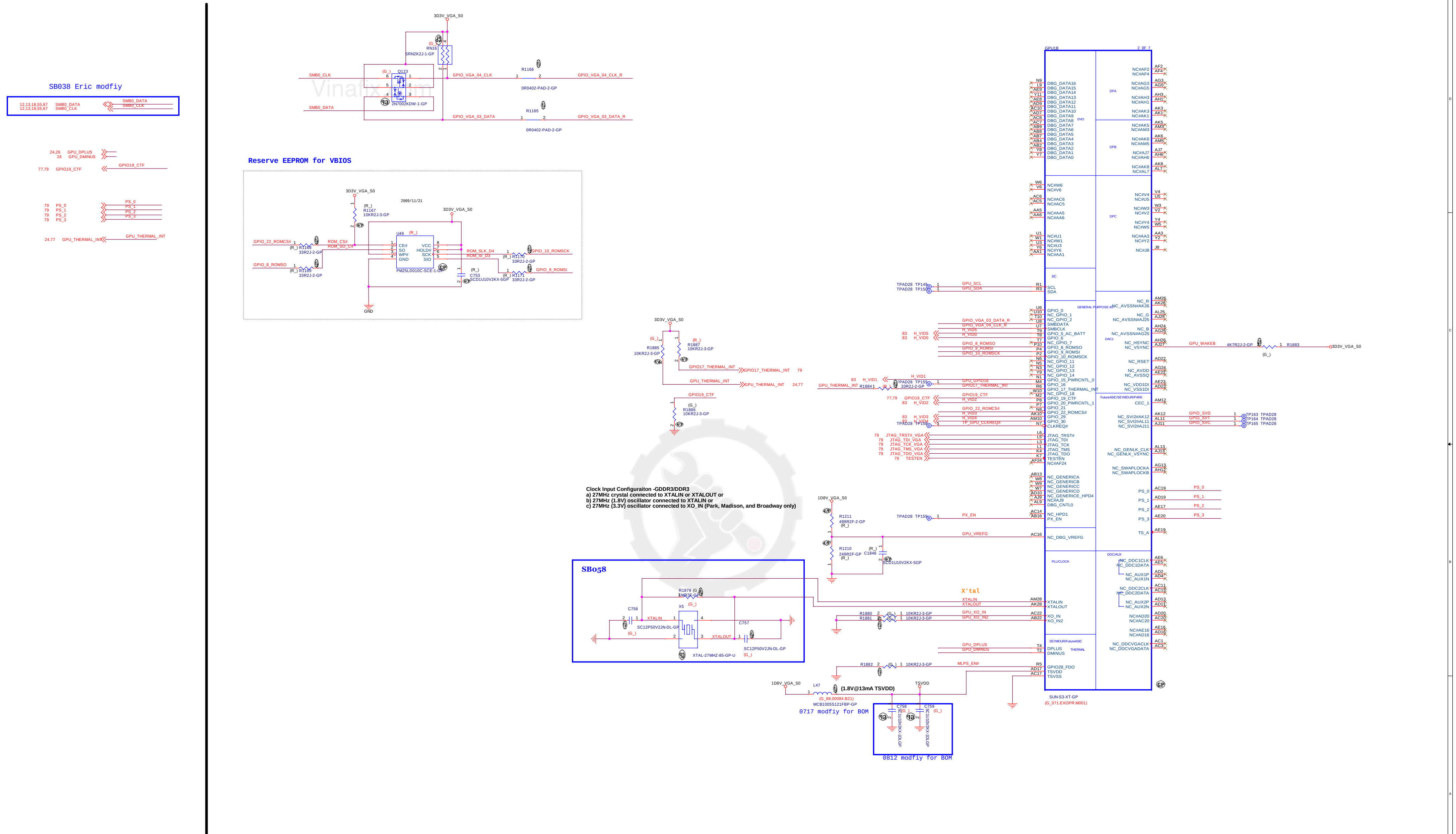

<Core Design>

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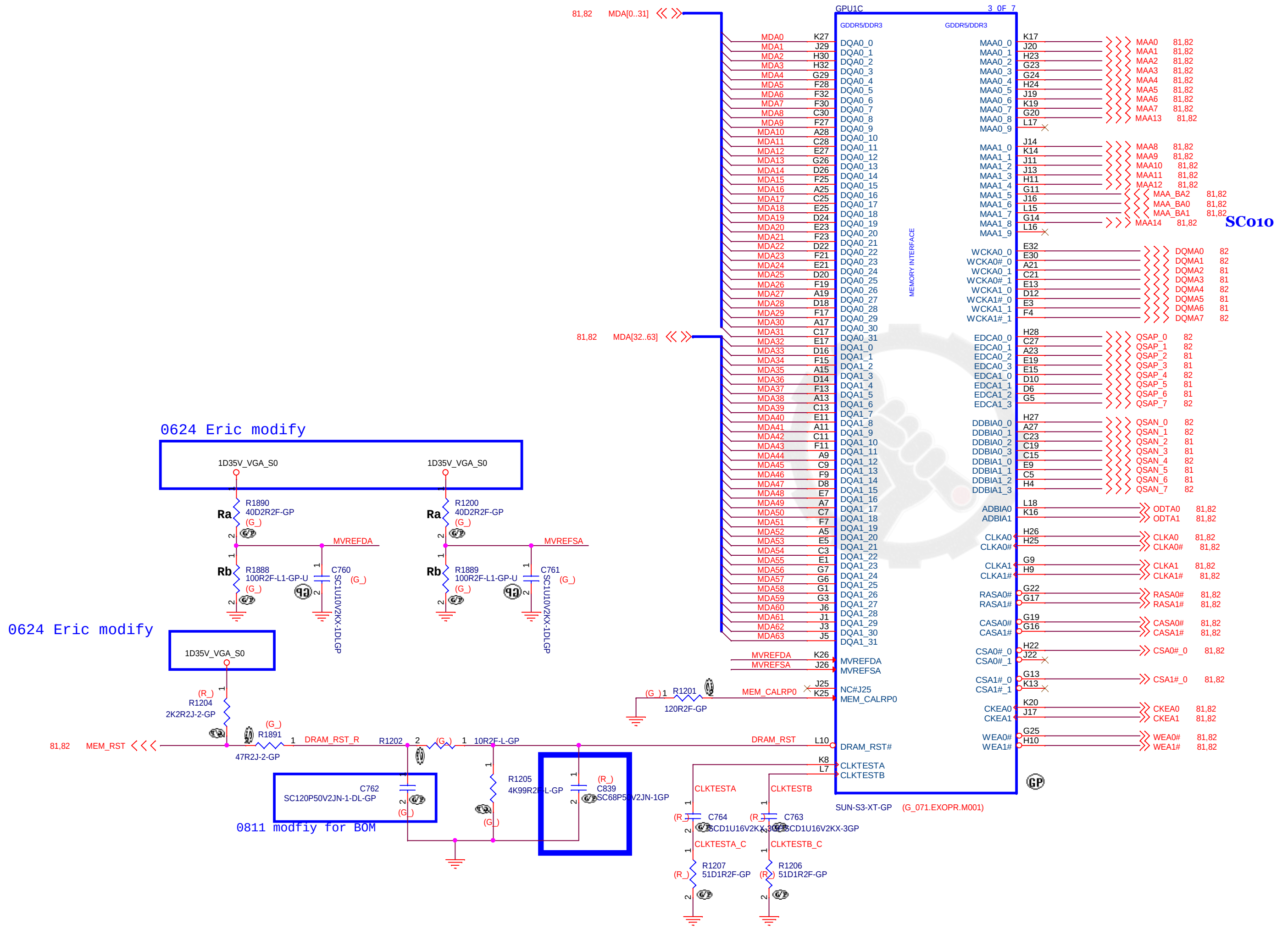
Title	077_GPU_Exo I/O	
Size D	Document Number: Rosa_Carrizo AIO	Rev -1
Date: Tuesday, August 09, 2016	Sheet 77 of 105	



<Core Design>

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Title: 078_GPU_Exo MEMORY

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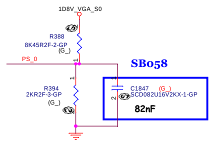
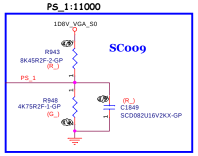
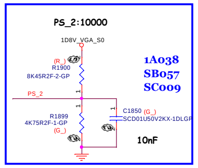
Aperture Size = 256MB
PS_0:01001



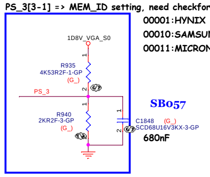
PS_1[1]=0 => PCIe GEN2
PS_1:11000



PS_2:10000

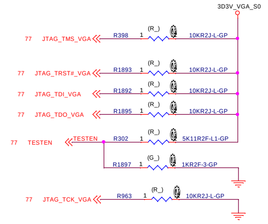


PS_3[3-1] => MEM_ID setting, need checkfor AMD
00001:HYNIX 2G R935:8K45 R940:2K
00010:SAMSUNG 2G R935:4K53 R940:2K
00011:MICRON 2G R935:6K98 R940:4k99



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0"(PD)	"1"(PU)	"0"(PD)
JTAG_TRST#	"1"(PU)	"1"(PU)	NC
JTAG_TCK	"0"(PD)	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC



PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM	Design dependent, see the description.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved	N/A

PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 48).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.

PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/ HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero enables all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

Capacitor Lookup Table for Bits [5:4]

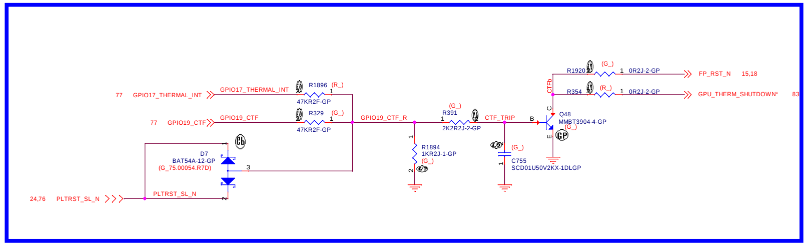
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

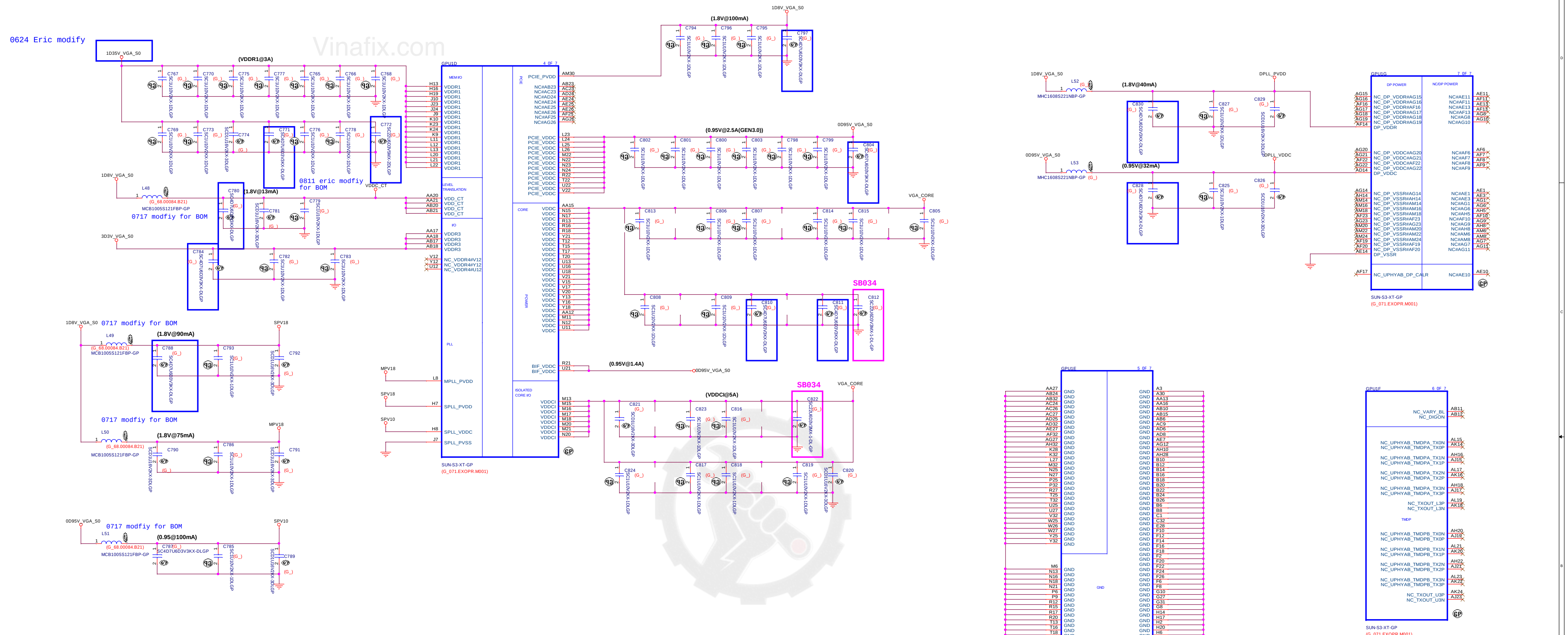
Resistor Divider Lookup Table for Bits [3:1]

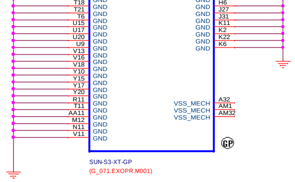
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

THERMAL PROTECTION







For cost effective designs,

VDDCI and VDDC can share one common regulator

supplying the total TDC of both rails

VDDC and VDDCI vias should be separate underneath the ASIC and only joined on the unified power plane

For designs that target maximal performance,

a dedicated regulator for VDDCI with two selectable output levels is required.

VDDCI FB is available on Topaz.

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Title	080_GPU_Exo POWER	
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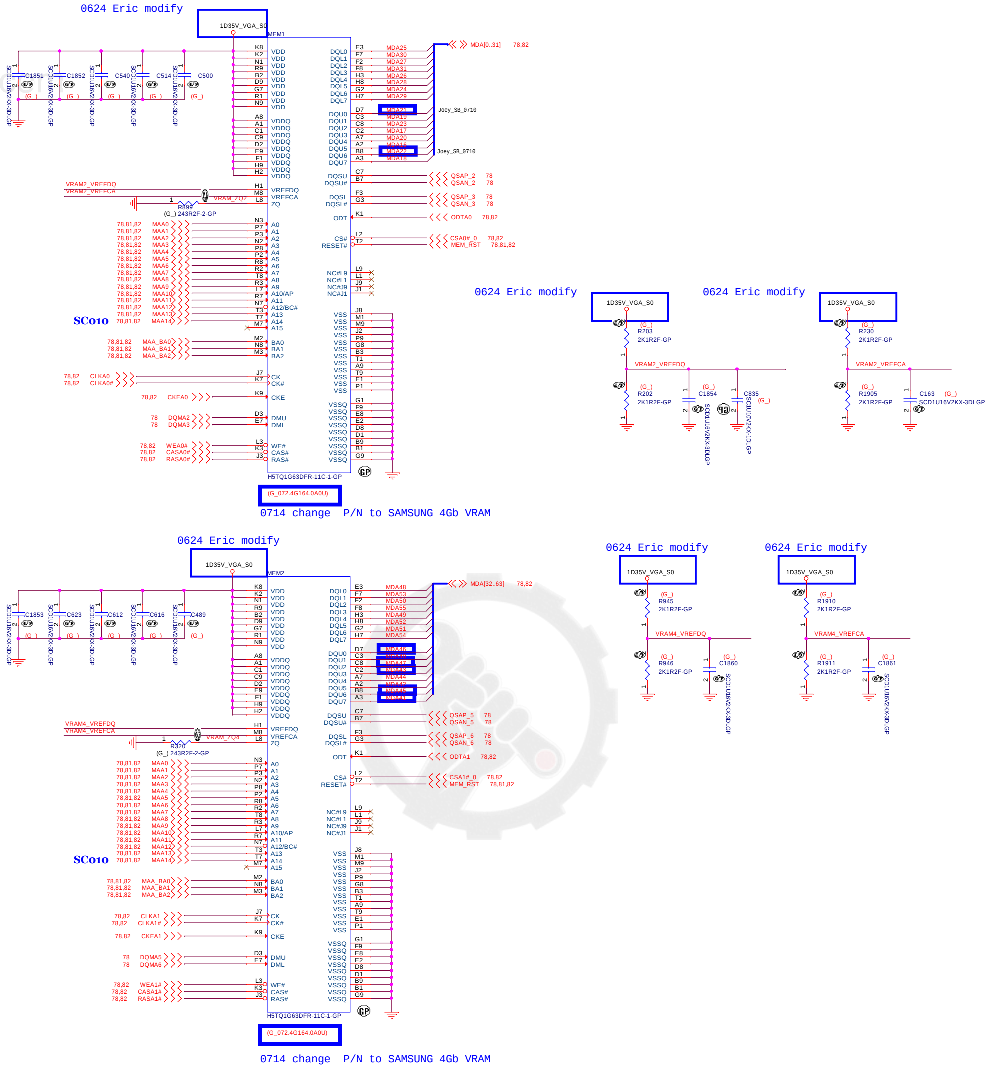

256M*16 VRAM
072.4G164.0A0U - SAMSUNG K4W4G1646D-BC1A
72.05463.D0U - Hynix H5TC4G63AFR-11C

<Core Design>

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Title	081_VRAM1,2(1/2)		
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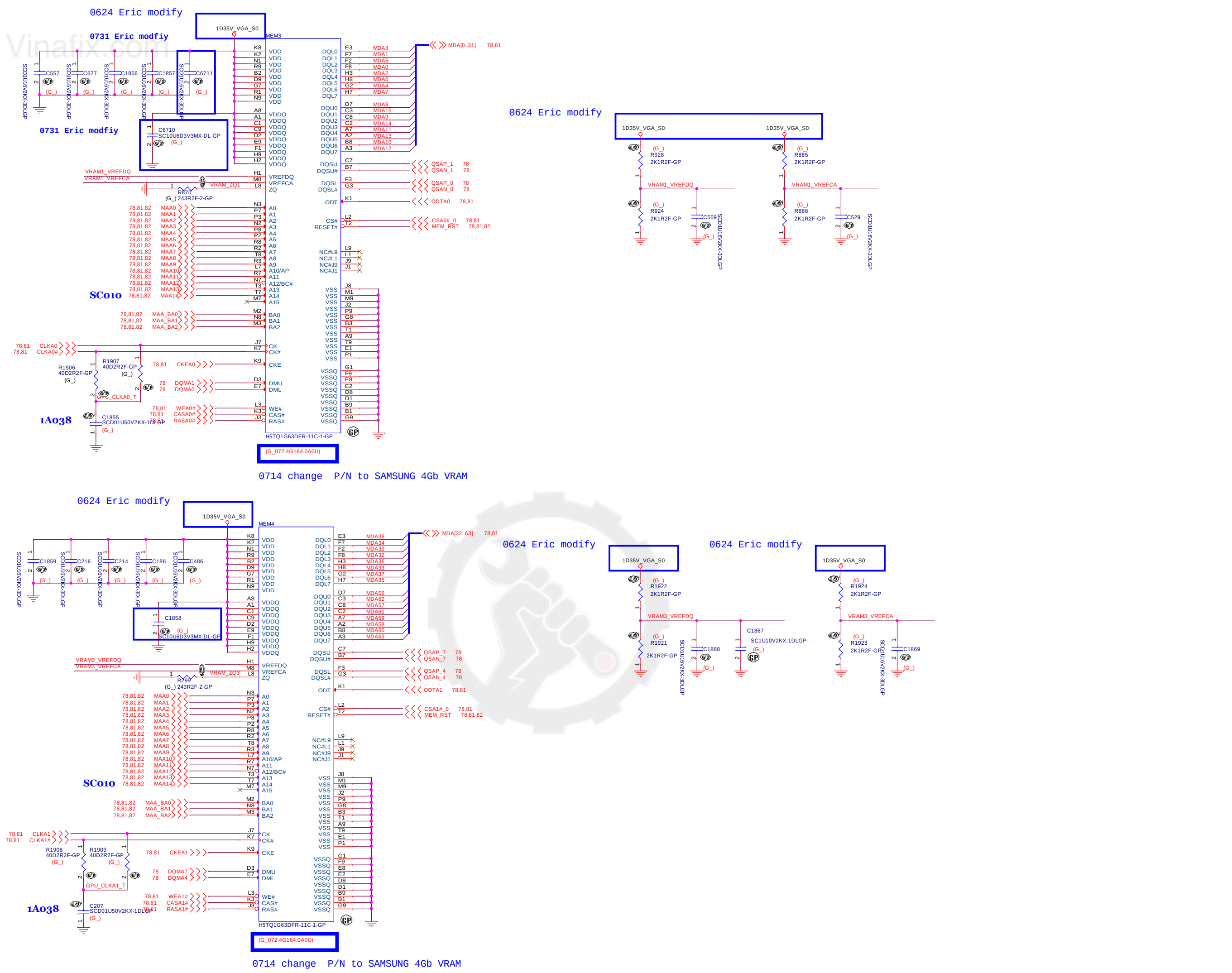

256M*16 VRAM
072.4G164.0A0U - SAMSUNG K4W4G1646D-BC1A
72.05463.D0U - Hynix H5TC4G63AFR-11C

<Core Design>

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Title	082_VRAM3,4(2/2)	
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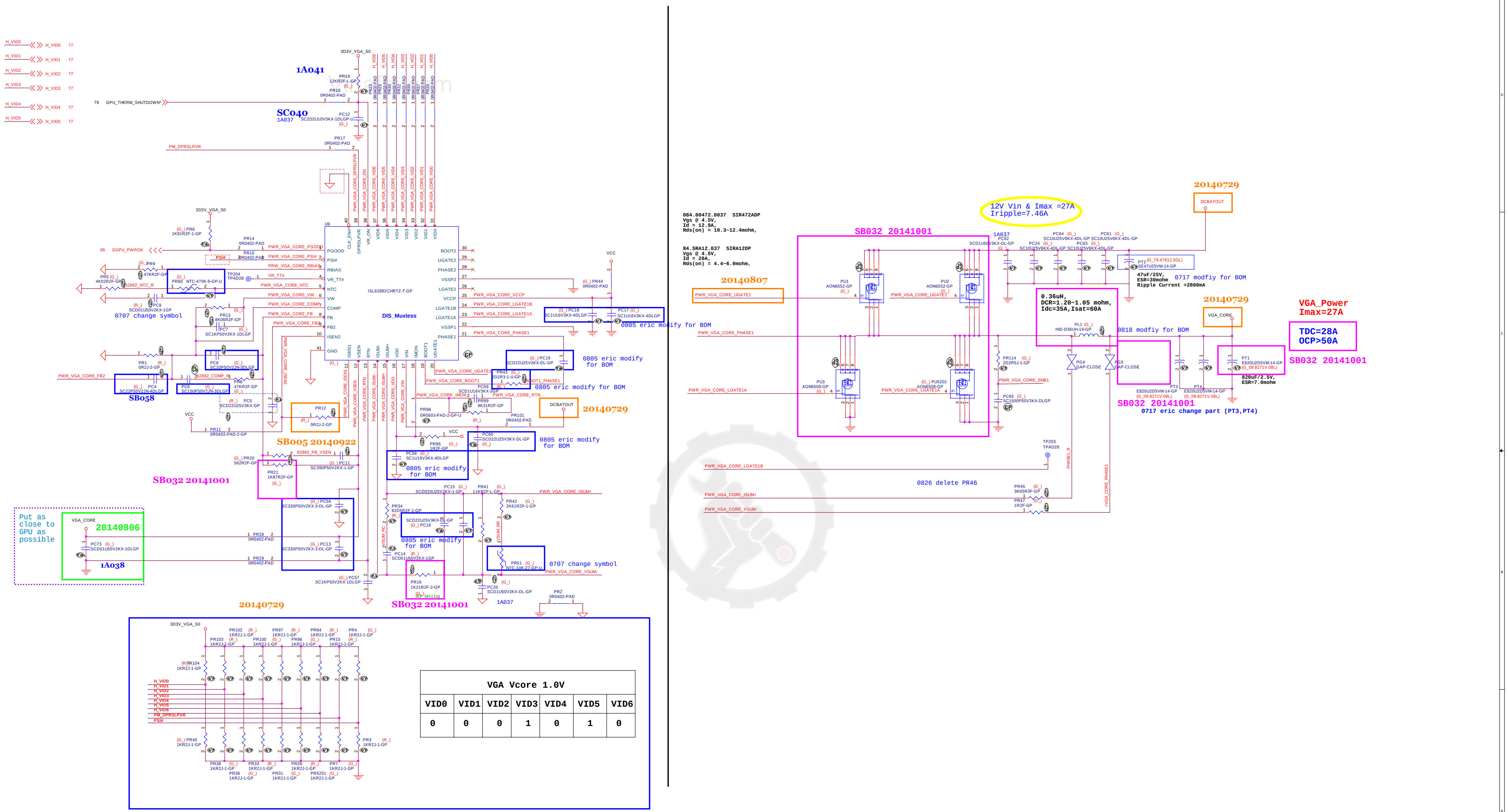

VGA Vcore 1.0V						
VID0	VID1	VID2	VID3	VID4	VID5	VID6
0	0	0	1	0	1	0

<Core Design>

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Title: 083_GPU_POWER CORE

Size: D | Document Number: Rosa_Carrizo AIO | Rev: -1

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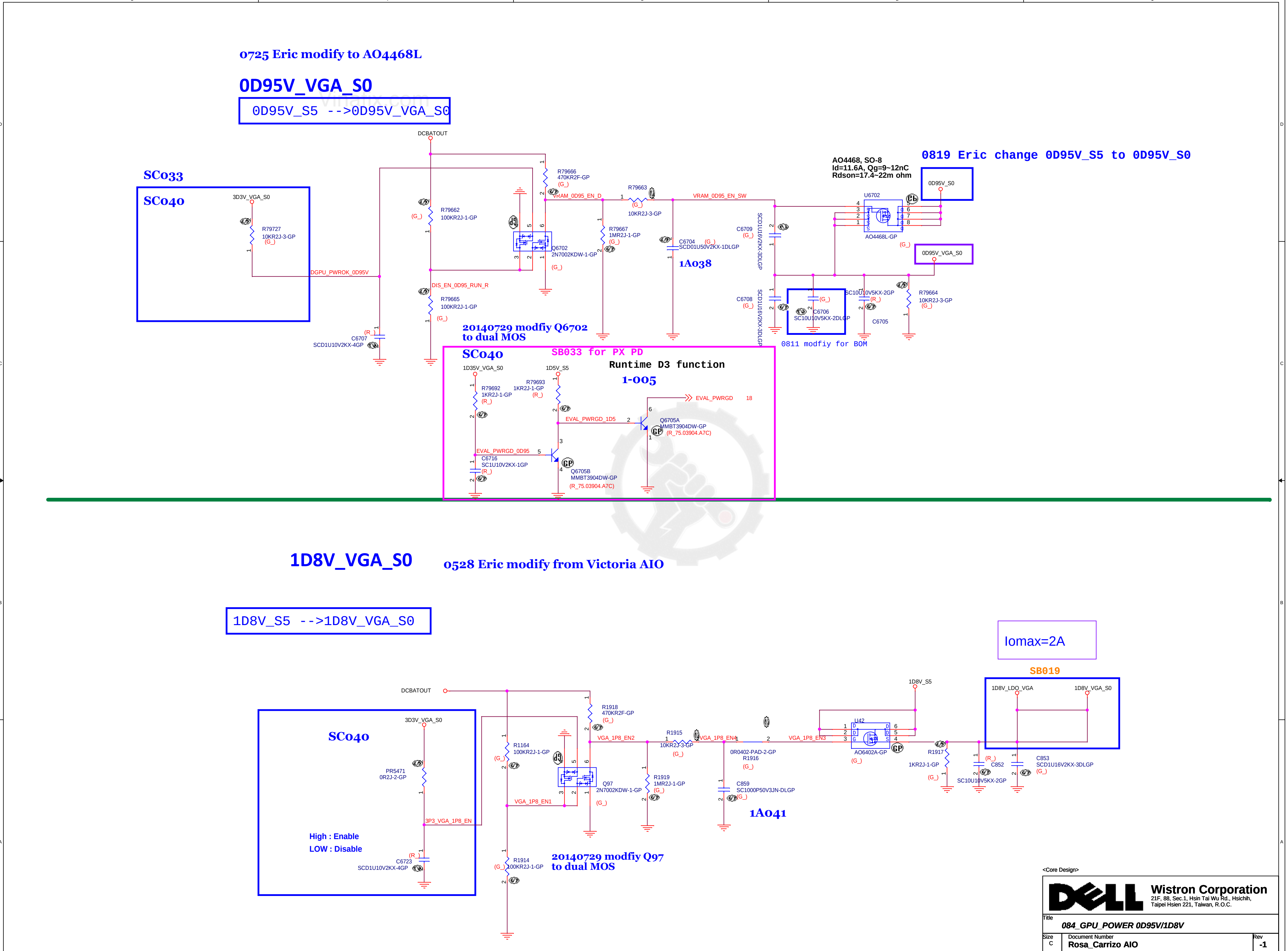

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Title		
084_GPU_POWER 0D95V/1D8V		
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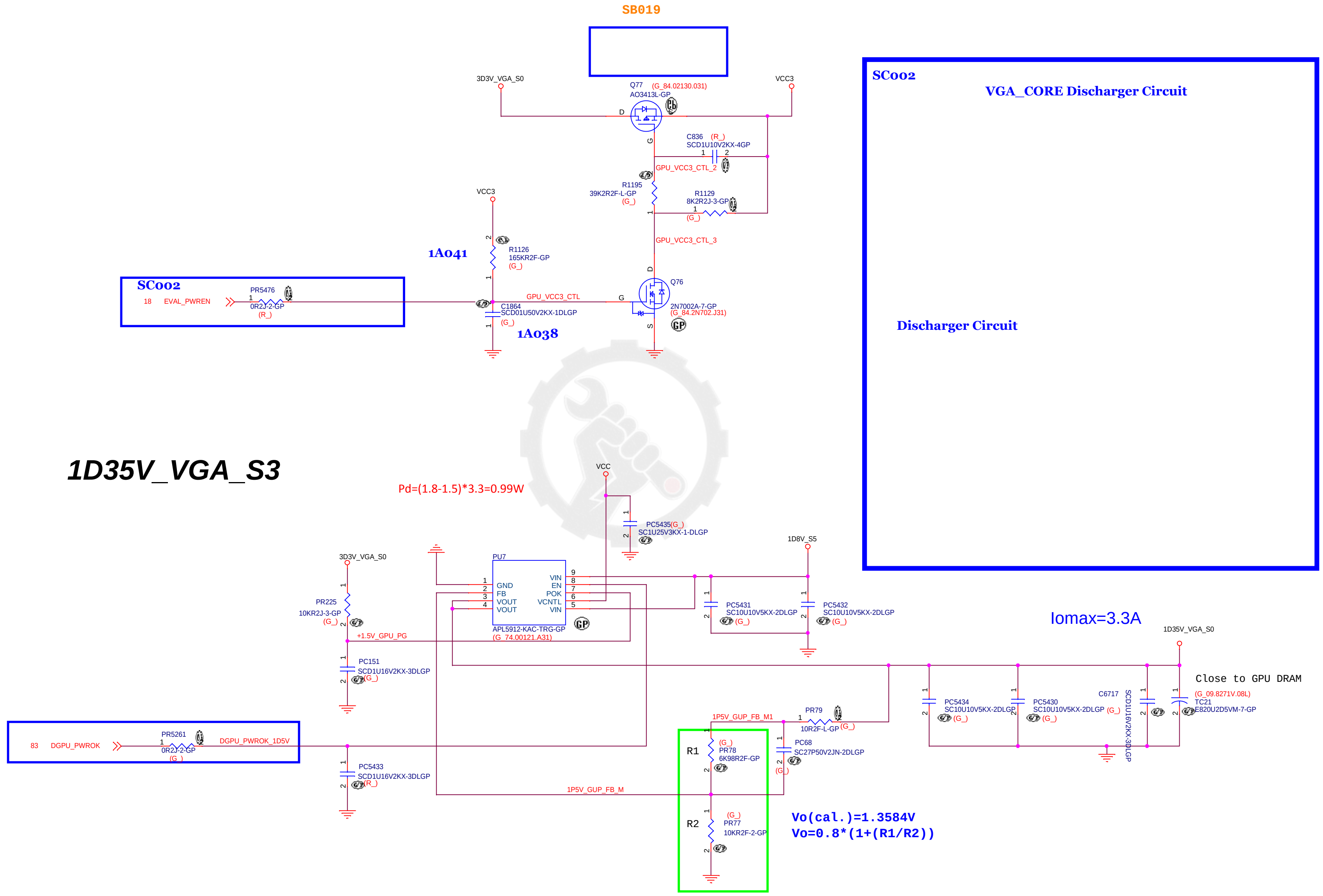
3D3V_VGA_S0

3D3V_S0 to 3D3V_DELAY Transfer

1D35V_VGA_S3



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Title	085_GPU_POWER 3D3V/ 1D35V	
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Title					
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Title

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6-1.2-7c(2.40) stack up and impedance

[illegible]	6-1.2-7c	[illegible]	1. Impedance Control tolerance +/- 10%
[illegible] (mm)	1.2 ± 0.12		2. Coupon [illegible] Impedance report [illegible] Wistron [illegible]

Stack up

			Thickness (mil)
L1	TOP		1.7
		PP	2.7
L2	G/P ※3		1.2
		Core	4
L3	Signal		1.2
		PP	24
L4	Signal		1.2
		Core	4
L5	G/P		1.2
		PP	2.7
L6	Bottom		1.7

Impedance Request List

Spec \ Layer	L1 (Ref. Plane) ※1	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)
Single Ended Type (Trace width : mil)				
27.4Ω	12.0 (L2)	16.0 (L2/L5)	16.0 (L2/L5)	12.0 (L5)
33Ω	9.0 (L2)	12.0 (L2/L5)	12.0 (L2/L5)	9.0 (L5)
34Ω	8.5 (L2)	11.5(L2/L5)	11.5 (L2/L5)	8.5 (L5)
35Ω	8.0 (L2)	10.5 (L2/5)	10.5 (L2/5)	8.0 (L5)
37.5Ω	7.0 (L2)	9.5 (L2/L5)	9.5 (L2/L5)	7.0 (L5)
39Ω	6.5 (L2) ※4	9.0(L2/L5)	9.0(L2/L5)	6.5 (L5) ※4
40Ω	6.5 (L2) ※4	8.5 (L2/L5)	8.5 (L2/L5)	6.5 (L5) ※4
42Ω	5.5 (L2)	7.5 (L2/L5)	7.5 (L2/L5)	5.5 (L5)
45Ω	5.0 (L2)	6.5 (L2/L5)	6.5 (L2/L5)	5.0 (L5)
48Ω	4.5 (L2)	5.5 (L2/L5)	5.5 (L2/L5)	4.5 (L5)
50Ω	4.0 (L2)	5.0 (L2/L5)	5.0 (L2/L5)	4.0 (L5)
52Ω	3.5 (L2) ※2	4.5 (L2/L5)	4.5 (L2/L5)	3.5 (L5) ※2
55Ω	NA	4.0 (L2/L5)	4.0 (L2/L5)	NA
Differential Type (Trace width/Space width/Trace width: mil)				
110Ω	NA	3.5/13/3.5(L2/L5)	3.5/13/3.5(L2/L5)	NA
100Ω	3.5/10/3.5(L2)	4/9/4(L2/L5)	4/9/4(L2/L5)	3.5/10/3.5(L5)
95Ω	3.5/6/3.5(L2);4/10/4(L2)	4/6.5/4(L2/L5)	4/6.5/4(L2/L5)	3.5/6/3.5(L5);4/10/4(L5)
93Ω	3.5/5.5/3.5(L2);4/8/4(L2)	4/5.5/4(L2/L5);5/9/5(L2/L5)	4/5.5/4(L2/L5);5/9/5(L2/L5)	3.5/5.5/3.5(L5);4/8/4(L5)
90Ω	4/6/4(L2)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/6/4(L5)
85Ω	4/4.5/4(L2);5/8/5(L2)	5/5.5/5(L2/L5);5/5.5/5(L2/L4)	5/5.5/5(L2/L5);5/5.5/5(L3/L5)	4/4.5/4(L5);5/8/5(L5)
80Ω	5/5/5(L2)	6/6/6(L2/L5)	6/6/6(L2/L5)	5/5/5(L5)
75Ω	6/6/6(L2)	7/6/7(L2/L5)	7/6/7(L2/L5)	6/6/6(L5)
72Ω	7/8/7(L2)	7/5/7(L2/L5)	7/5/7(L2/L5)	7/8/7(L5)
70Ω	7/6/7(L2)	8/6/8(L2/L5)	8/6/8(L2/L5)	7/6/7(L5)
68Ω	6.5/4/6.5(L2)	7.5/4/7.5(L2/L5)	7.5/4/7.5(L2/L5)	6.5/4/6.5(L5)
65Ω	8/6/8(L2)	9/5/9(L2/L5)	9/5/9(L2/L5)	8/6/8(L5)

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Title: ***101_Stackup***

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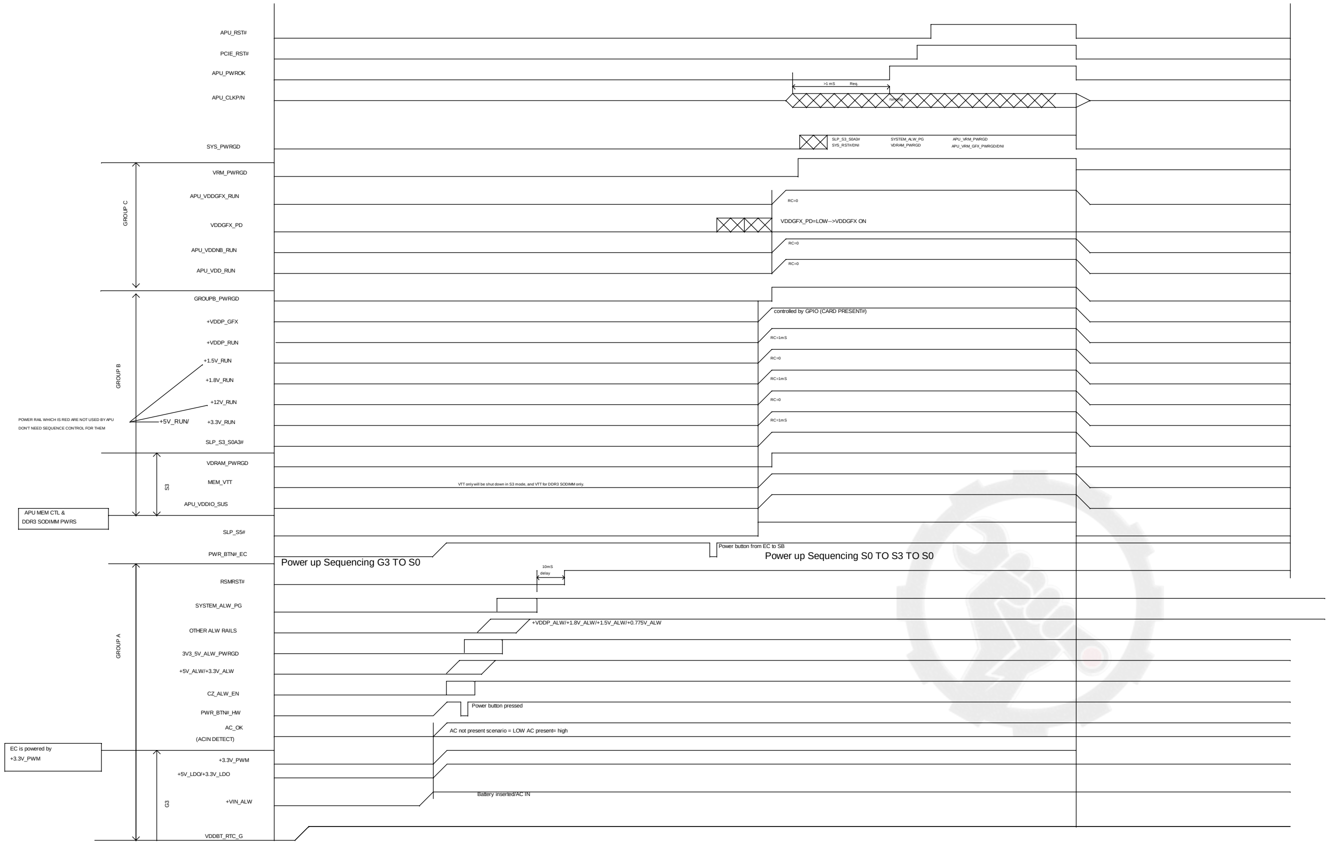
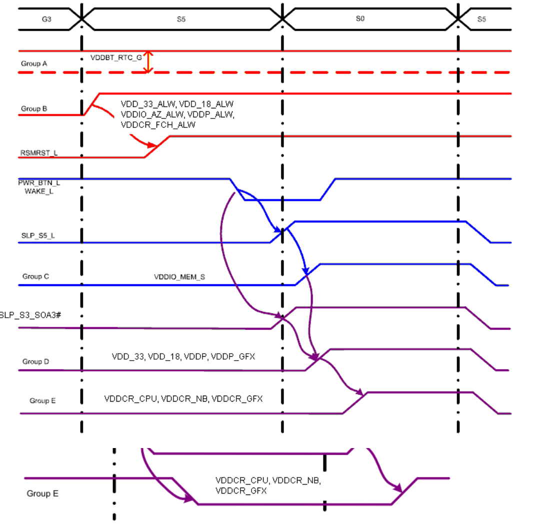
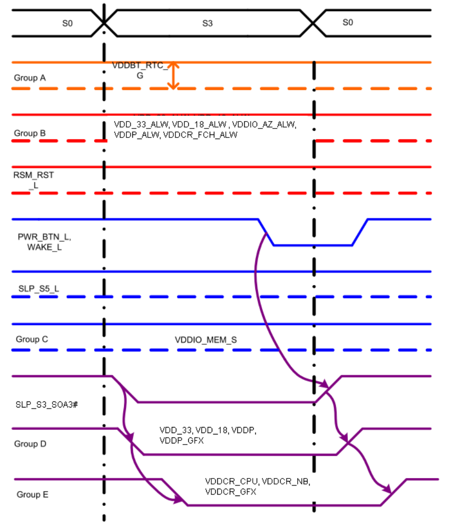
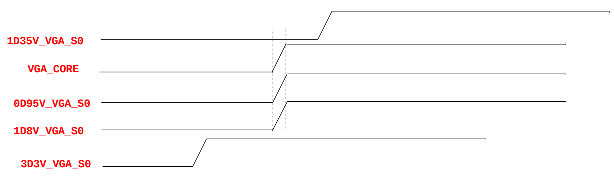
FROM AMD CRB BOARD







AMD GPU squence



Power on Sequence required:

1. There is no sequencing requirement between power supplies within the individual power groups.
2. All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequenceing Group B is greater than 10% of its specified minimum operating voltage.
3. All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
4. All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

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Title	102_Power Sequence	
Size D	Document Number: Rosa_Carrizo AIO	Rev -1
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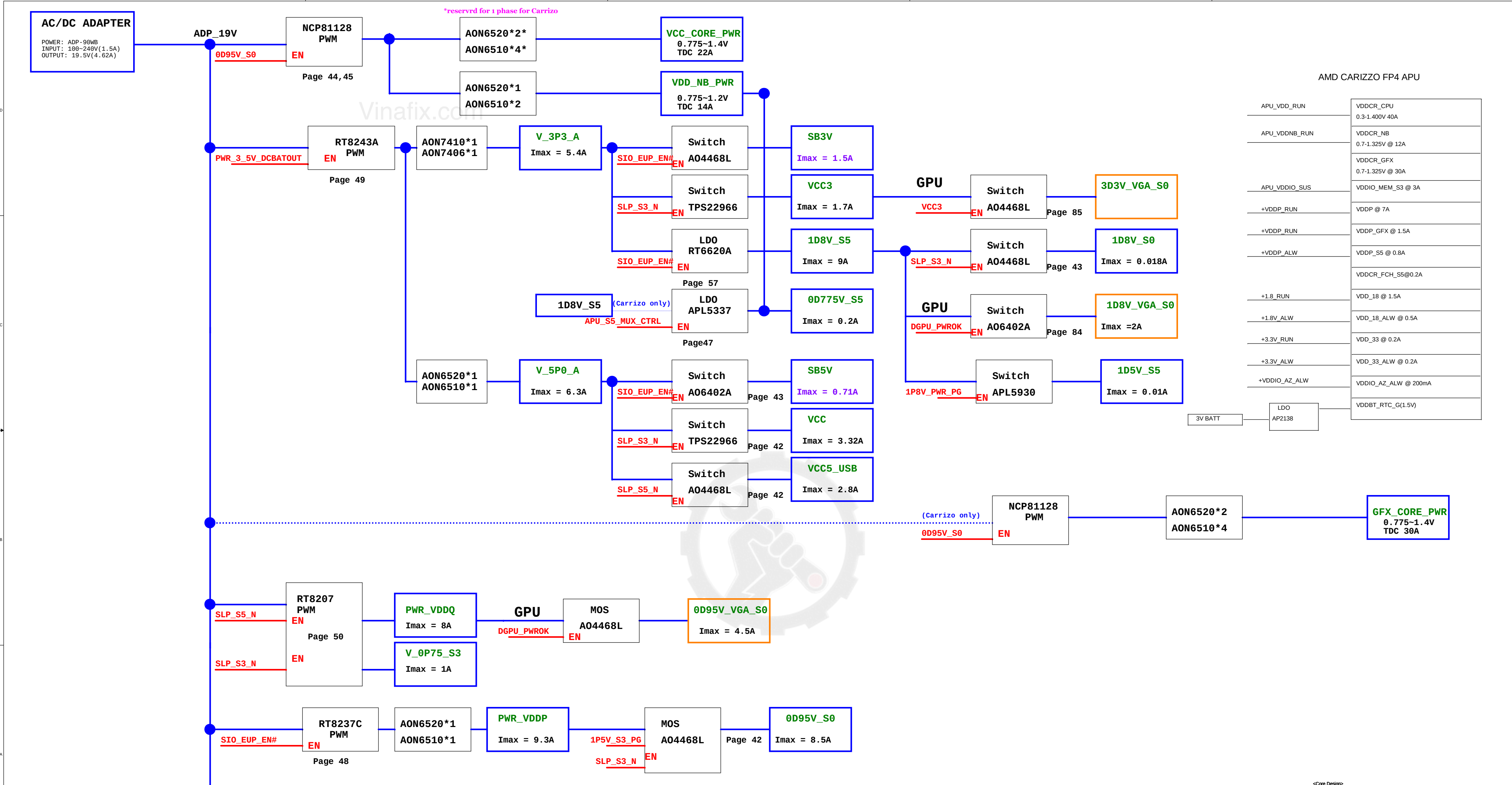

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Title	103_Power block Diagram	
Size: Custom	Document Number: Rosa_Carrizo AIO	Rev: -1
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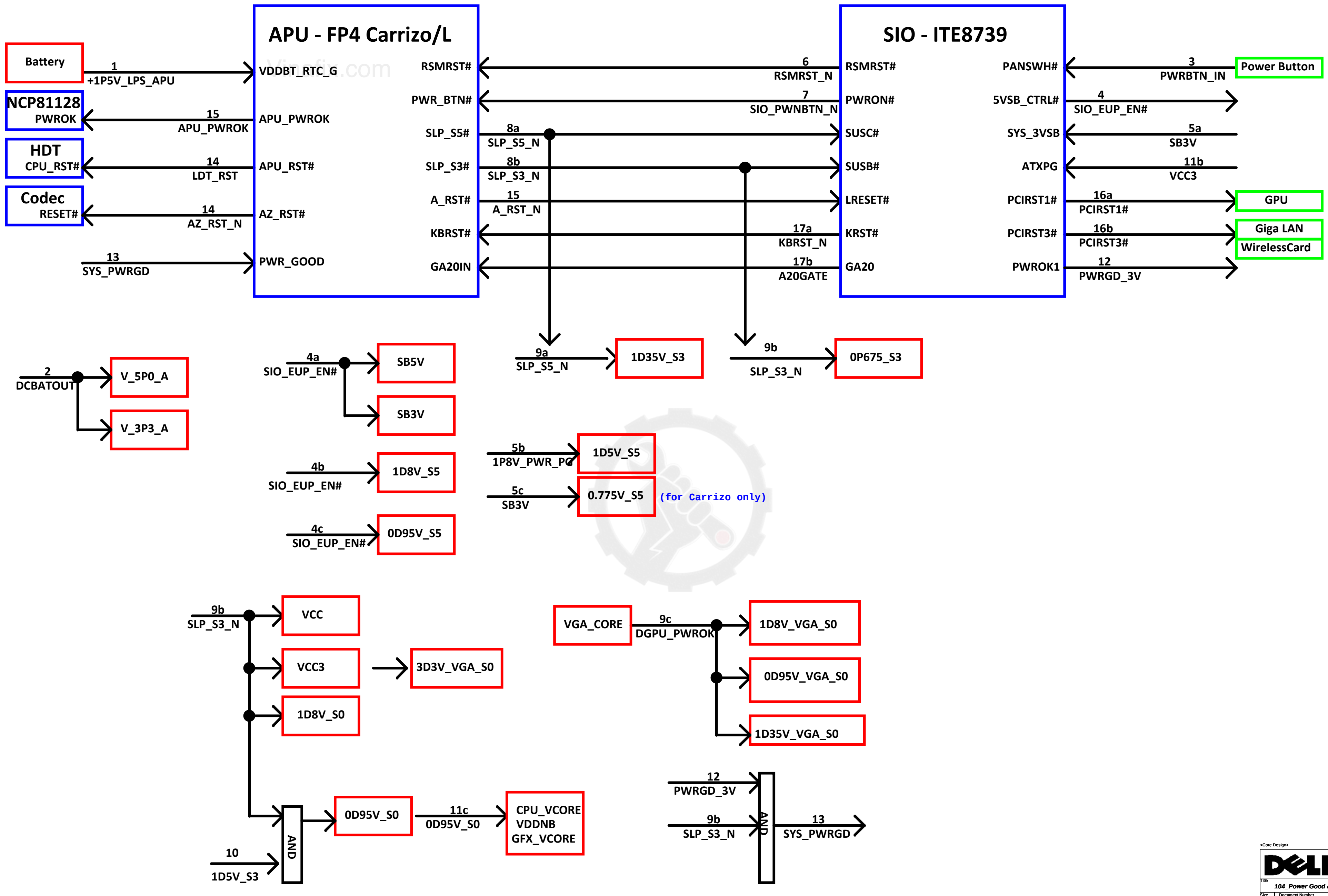

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Title	104_Power Good & Reset Diagram	
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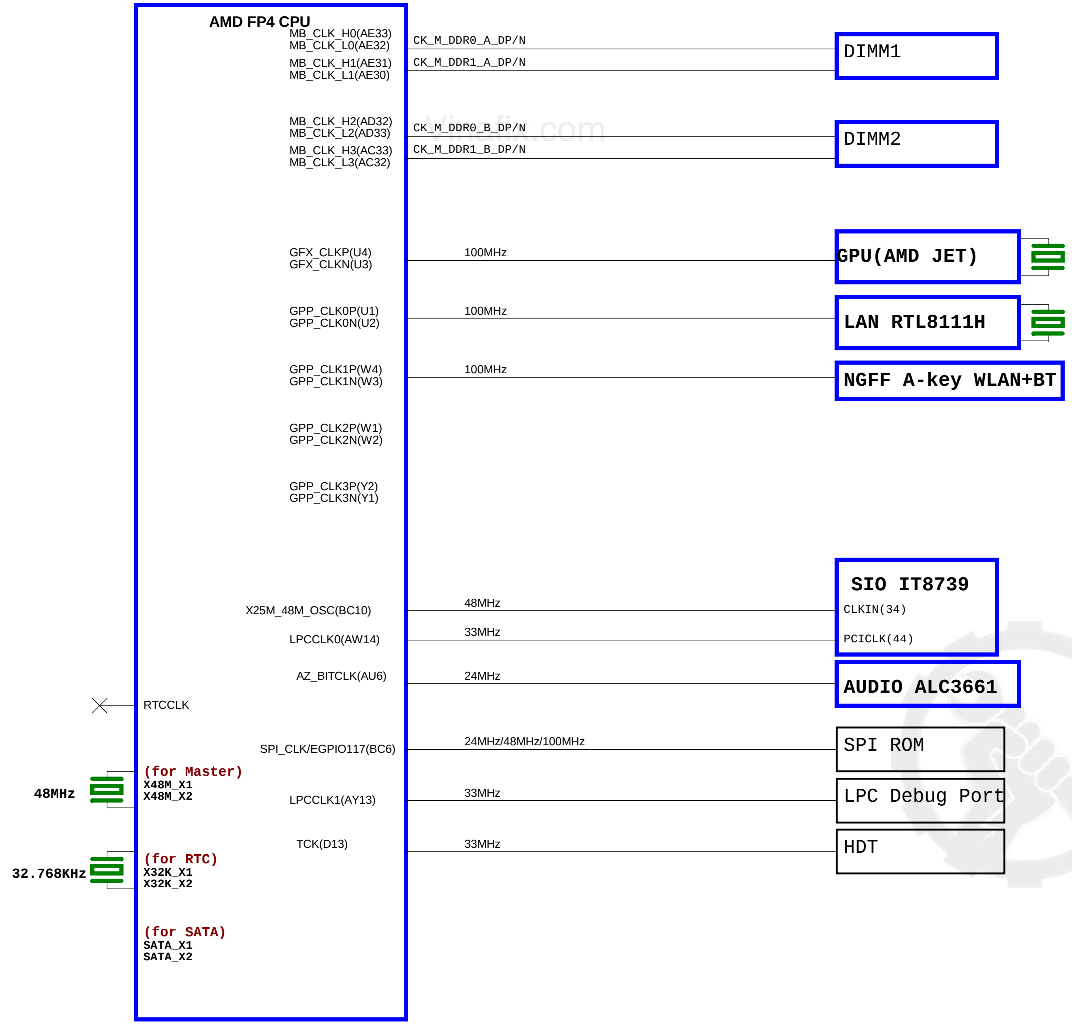
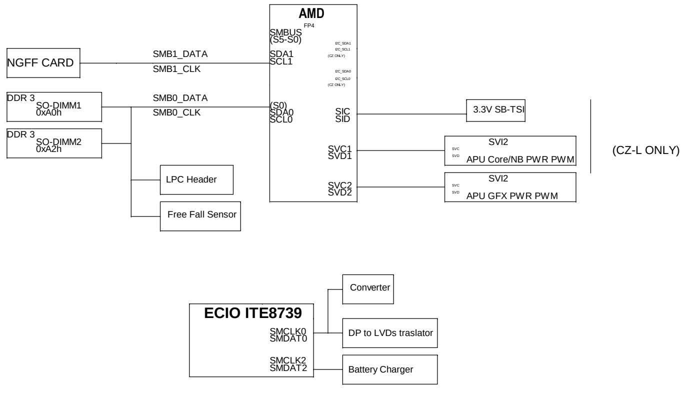


SMBus Block Diagram

ALL SLAVE ADDRESS IS 8-BIT INCLUDING W/R BIT
SLAVE ADDRESS FOR SLOT/HEADER PLEASE REFER TO MODULE SPEC



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Title: *105_Clock/SMBUS Diagram*		
Size: Custom	Document Number: **Rosa_Carrizo AIO**	Rev: -1
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