MS-7C09

ATX:226mm*185mm

Ver: 1.1

Intel -CoffeeLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *4 Phase*

*GT POWER PAK *2 Phase*

System Chipset:

Cannon Lake H310C

Onboard Chip:

SIO: NCT5567D
HD Audio Codec: ALC887
LAN: RTL8111H
Flash ROM: SPI 128 MB
DP to VGA: RTD2166
CUT VBAT: SLG4B41231

PWM:

VCORE - RT3607

DDR - RT8231

DDR VPP25 - MP2333

PCH(1.0V) - RT8125E

VCCSA - RT8125E

VCCIO - SY8288

Main Memory:

*DDR4 * 2 (Dual Channel)*

ACPI:

5VDAUL: uP7501

5VDIMM: uP7501

3VSB: GS7133+N MOS

3VDSW: GS7133

VCCSTPLL: GS7133

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

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Size	Document Description	Rev
Custom	Cover Sheet	1.1

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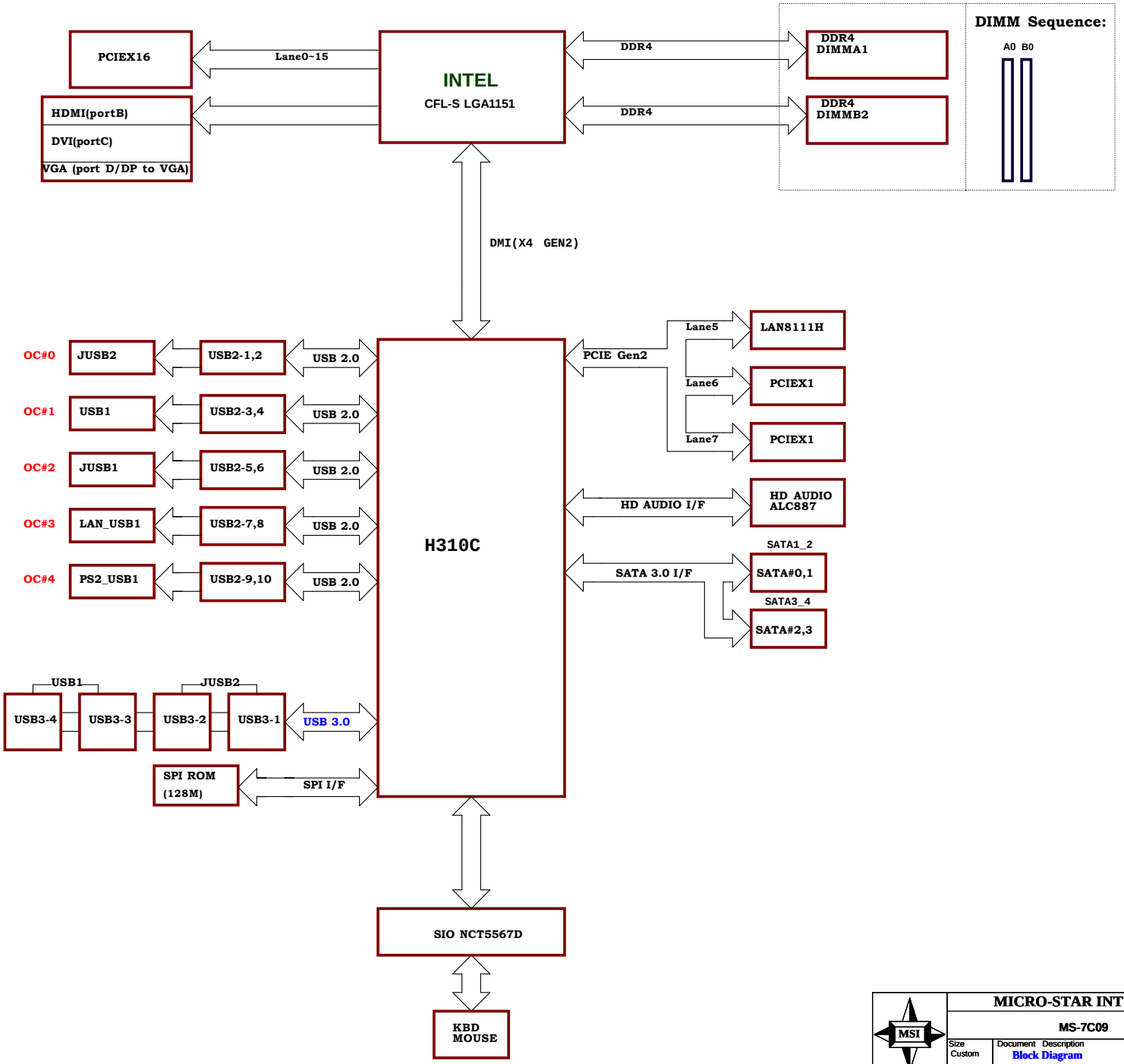
MS-7B33 Block Diagram



Slot Sequence:

PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN2)
PCIE X1	(By PCH GEN2)

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Size	Document Description	Rev
Custom	Block Diagram	1.1

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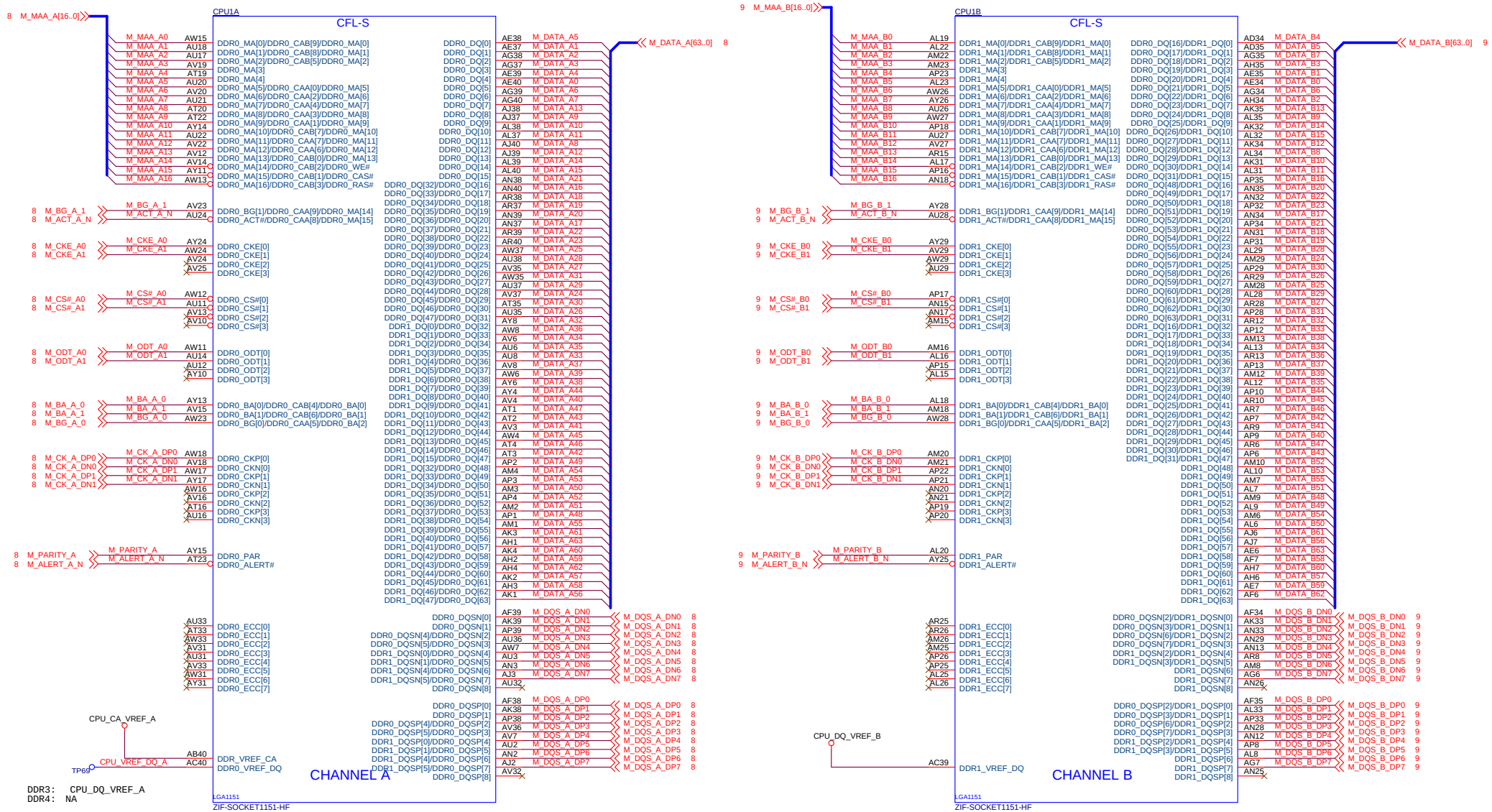

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MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: CPU-Memory
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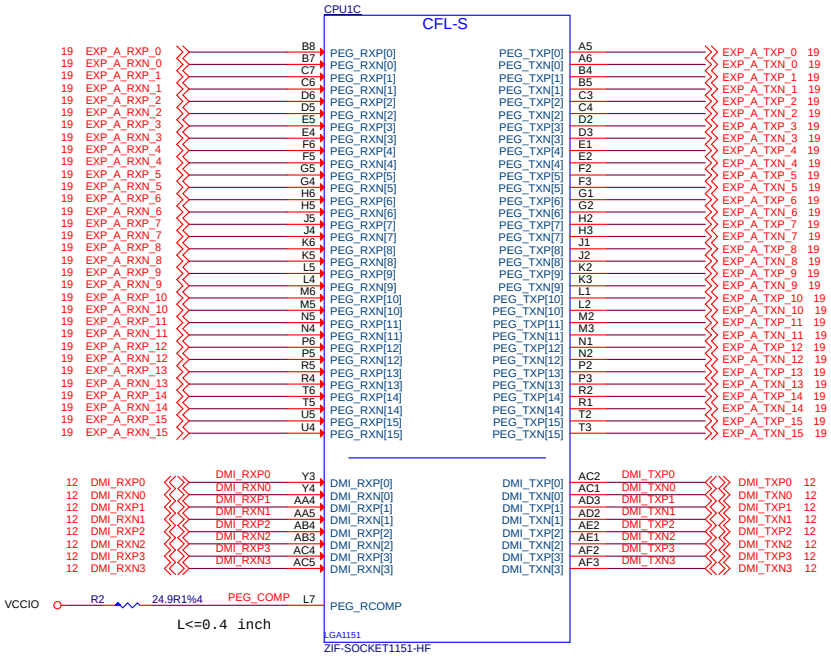
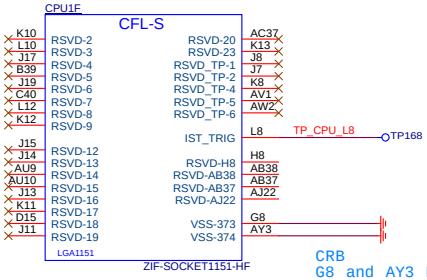
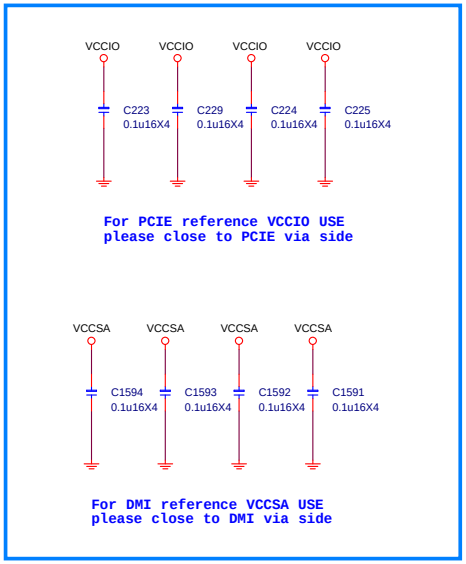
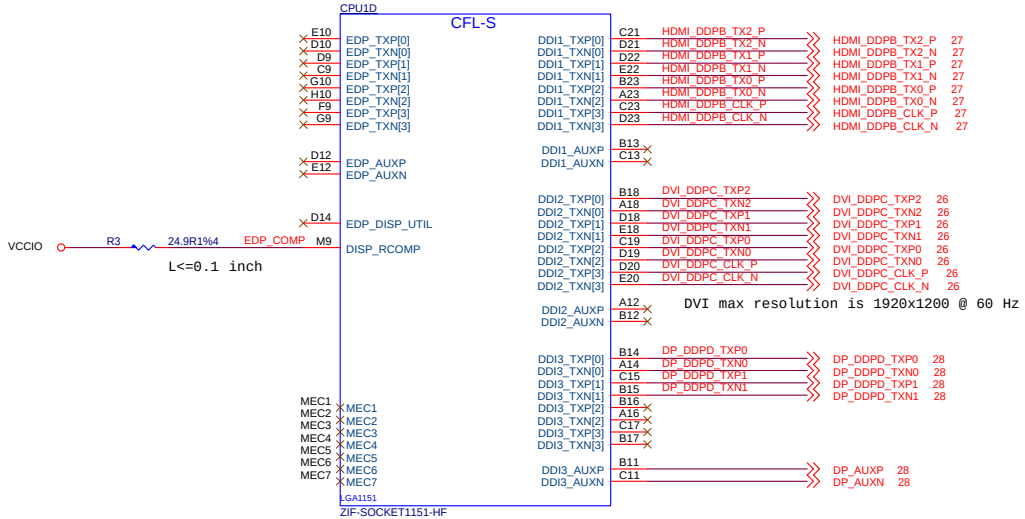




CRB
G8 and AY3 Pins can connect directly to GND.





MICRO-STAR INT'L CO.,LTD	
MS-7C09	
Size: Custom	Document Description: CPU-PEG/Display
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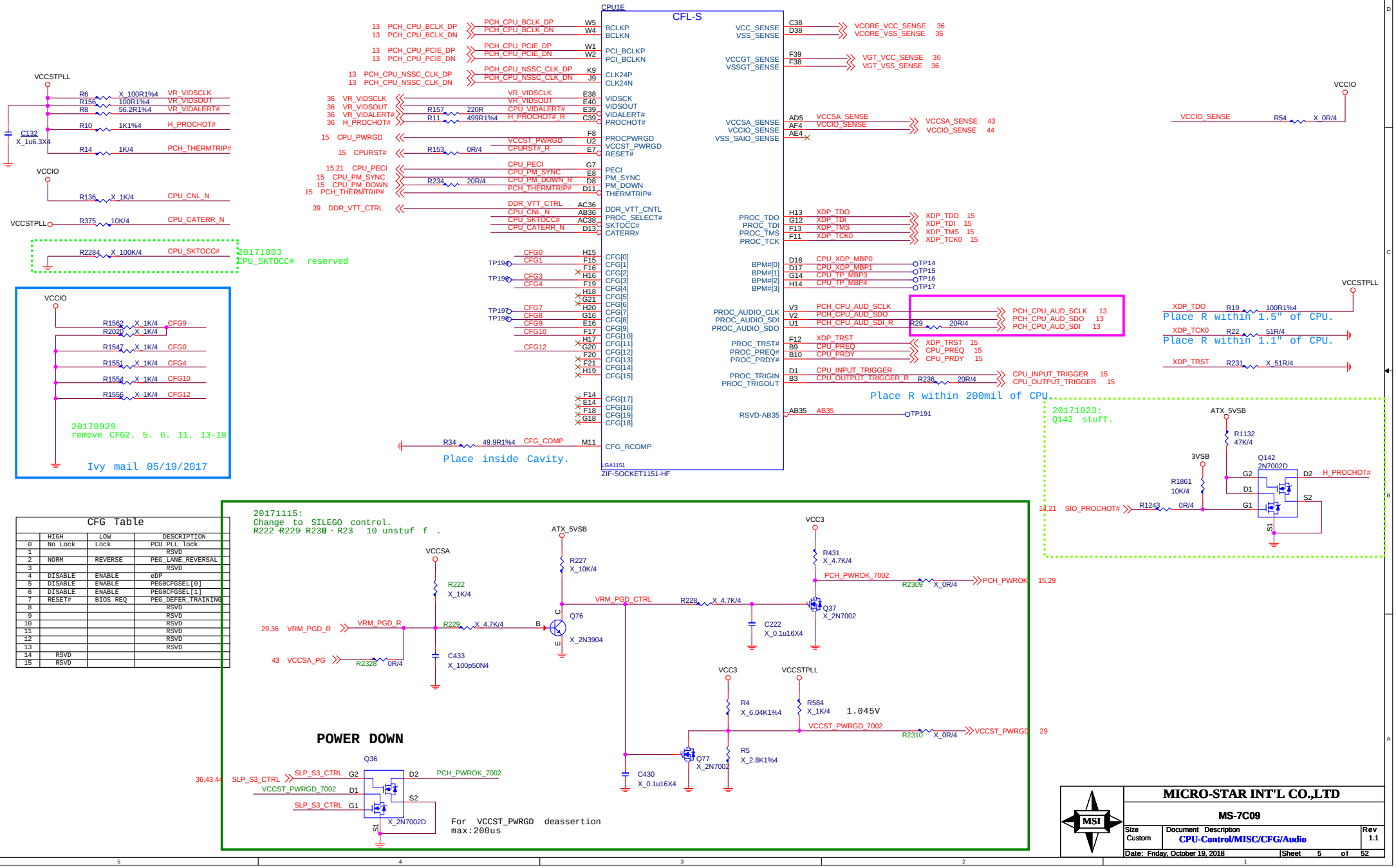

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

MICRO-STAR INT'L CO.,LTD		
MS-7C09		
Size: Custom	Document Description: CPU-Control/MISC/CFG/Audio	Rev: 1.1
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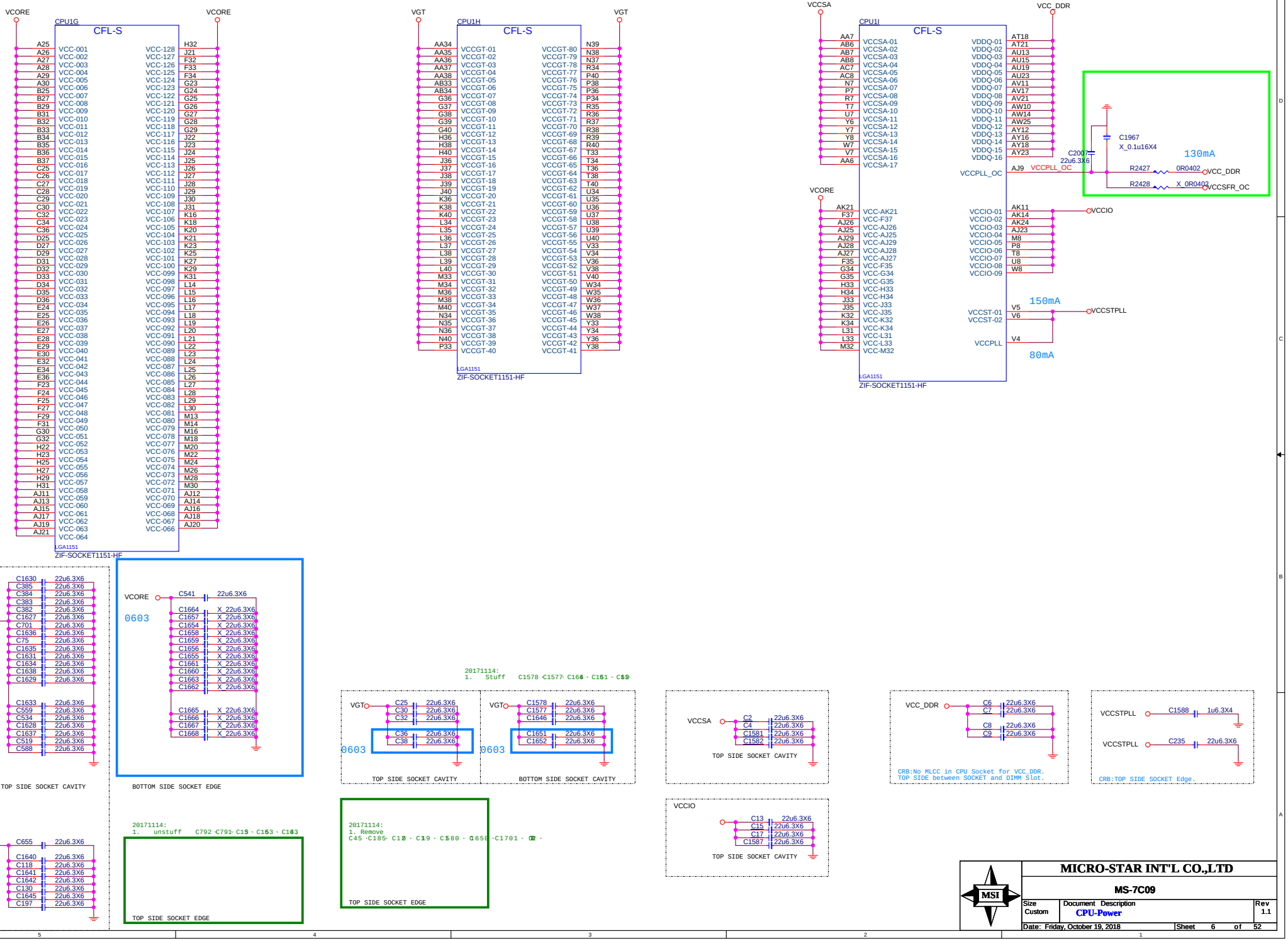
VCORE
CPU1G
CFL-S
VCC-001 VCC-002 VCC-003 VCC-004 VCC-005 VCC-006 VCC-007 VCC-008 VCC-009 VCC-010 VCC-011 VCC-012 VCC-013 VCC-014 VCC-015 VCC-016 VCC-017 VCC-018 VCC-019 VCC-020 VCC-021 VCC-022 VCC-023 VCC-024 VCC-025 VCC-026 VCC-027 VCC-028 VCC-029 VCC-030 VCC-031 VCC-032 VCC-033 VCC-034 VCC-035 VCC-036 VCC-037 VCC-038 VCC-039 VCC-040 VCC-041 VCC-042 VCC-043 VCC-044 VCC-045 VCC-046 VCC-047 VCC-048 VCC-049 VCC-050 VCC-051 VCC-052 VCC-053 VCC-054 VCC-055 VCC-056 VCC-057 VCC-058 VCC-059 VCC-060 VCC-061 VCC-062 VCC-063 VCC-064
VCC-128 VCC-127 VCC-126 VCC-125 VCC-124 VCC-123 VCC-122 VCC-121 VCC-120 VCC-119 VCC-118 VCC-117 VCC-116 VCC-115 VCC-114 VCC-113 VCC-112 VCC-111 VCC-110 VCC-109 VCC-108 VCC-107 VCC-106 VCC-105 VCC-104 VCC-103 VCC-102 VCC-101 VCC-100 VCC-099 VCC-098 VCC-097 VCC-096 VCC-095 VCC-094 VCC-093 VCC-092 VCC-091 VCC-090 VCC-089 VCC-088 VCC-087 VCC-086 VCC-085 VCC-084 VCC-083 VCC-082 VCC-081 VCC-080 VCC-079 VCC-078 VCC-077 VCC-076 VCC-075 VCC-074 VCC-073 VCC-072 VCC-071 VCC-070 VCC-069 VCC-068 VCC-067 VCC-066
LGA1151
ZIF-SOCKET1151-HF
VGT
CPU1H
CFL-S
VCCGT-01 VCCGT-02 VCCGT-03 VCCGT-04 VCCGT-05 VCCGT-06 VCCGT-07 VCCGT-08 VCCGT-09 VCCGT-10 VCCGT-11 VCCGT-12 VCCGT-13 VCCGT-14 VCCGT-15 VCCGT-16 VCCGT-17 VCCGT-18 VCCGT-19 VCCGT-20 VCCGT-21 VCCGT-22 VCCGT-23 VCCGT-24 VCCGT-25 VCCGT-26 VCCGT-27 VCCGT-28 VCCGT-29 VCCGT-30 VCCGT-31 VCCGT-32 VCCGT-33 VCCGT-34 VCCGT-35 VCCGT-36 VCCGT-37 VCCGT-38 VCCGT-39 VCCGT-40
VCCGT-80 VCCGT-79 VCCGT-78 VCCGT-77 VCCGT-76 VCCGT-75 VCCGT-74 VCCGT-73 VCCGT-72 VCCGT-71 VCCGT-70 VCCGT-69 VCCGT-68 VCCGT-67 VCCGT-66 VCCGT-65 VCCGT-64 VCCGT-63 VCCGT-62 VCCGT-61 VCCGT-60 VCCGT-59 VCCGT-58 VCCGT-57 VCCGT-56 VCCGT-55 VCCGT-54 VCCGT-53 VCCGT-52 VCCGT-51 VCCGT-50 VCCGT-49 VCCGT-48 VCCGT-47 VCCGT-46 VCCGT-45 VCCGT-44 VCCGT-43 VCCGT-42 VCCGT-41
LGA1151
ZIF-SOCKET1151-HF
VCCSA
VCC_DDR
CPU1I
CFL-S
VCCSA-01 VCCSA-02 VCCSA-03 VCCSA-04 VCCSA-05 VCCSA-06 VCCSA-07 VCCSA-08 VCCSA-09 VCCSA-10 VCCSA-11 VCCSA-12 VCCSA-13 VCCSA-14 VCCSA-15 VCCSA-16 VCCSA-17
VDDQ-01 VDDQ-02 VDDQ-03 VDDQ-04 VDDQ-05 VDDQ-06 VDDQ-07 VDDQ-08 VDDQ-09 VDDQ-10 VDDQ-11 VDDQ-12 VDDQ-13 VDDQ-14 VDDQ-15 VDDQ-16
VCCPLL_OC
VCCIO-01 VCCIO-02 VCCIO-03 VCCIO-04 VCCIO-05 VCCIO-06 VCCIO-07 VCCIO-08 VCCIO-09
VCCST-01 VCCST-02
VCCPLL
VCORE
VCC-AK21 VCC-F37 VCC-AJ26 VCC-AJ25 VCC-AJ29 VCC-AJ28 VCC-AJ27 VCC-F35 VCC-G34 VCC-G35 VCC-H33 VCC-H34 VCC-J33 VCC-J35 VCC-K32 VCC-K34 VCC-L31 VCC-L33 VCC-M32
LGA1151
ZIF-SOCKET1151-HF
C1967
X_0.1u16X4
C2007
22u6.3X6
130mA
R2427
0R0402
R2428
X_0R0402
VCC_DDR
VCCSFR_OC
VCCPLL_OC
VCCIO
150mA
VCCSTPLL
80mA
C1630 C385 C384 C383 C382 C1627 C701 C1636 C75 C1635 C1631 C1634 C1638 C1629
C1633 C559 C534 C1628 C1637 C519 C588
0603
TOP SIDE SOCKET CAVITY
C541
C1664 C1657 C1654 C1658 C1659 C1656 C1655 C1661 C1660 C1663 C1662
C1665 C1666 C1667 C1668
0603
BOTTOM SIDE SOCKET EDGE
C655
C1640 C118 C1641 C1642 C130 C1645 C197
20171114:
1. unstuff C792 C791 C15 C163 C163
TOP SIDE SOCKET EDGE
20171114:
1. Stuff C1578 C1577 C164 C161 C59
C25 C30 C32
C36 C38
0603
TOP SIDE SOCKET CAVITY
C1578 C1577 C1646
C1651 C1652
0603
BOTTOM SIDE SOCKET CAVITY
20171114:
1. Remove
C45 C185 C12 C19 C180 C165 C1701 C2
TOP SIDE SOCKET EDGE
C2 C4 C1581 C1582
TOP SIDE SOCKET CAVITY
C13 C15 C17 C1587
TOP SIDE SOCKET CAVITY
C6 C7 C8 C9
CRB:No MLCC in CPU Socket for VCC_DDR.
TOP SIDE between SOCKET and DIMM Slot.
C1588
C235
CRB:TOP SIDE SOCKET Edge.
MICRO-STAR INT'L CO.,LTD
MS-7C09
Size Custom
Document Description CPU-Power
Rev 1.1
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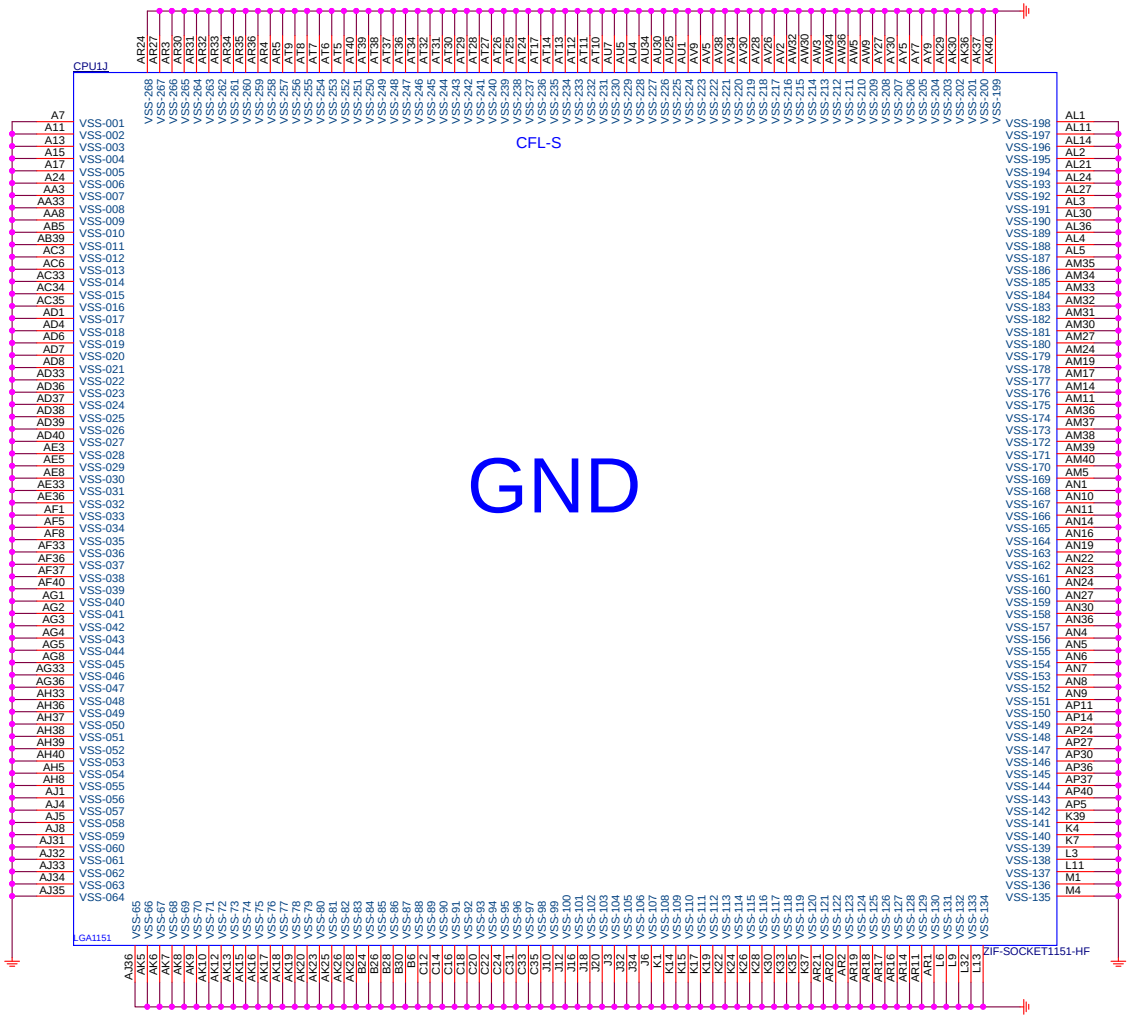

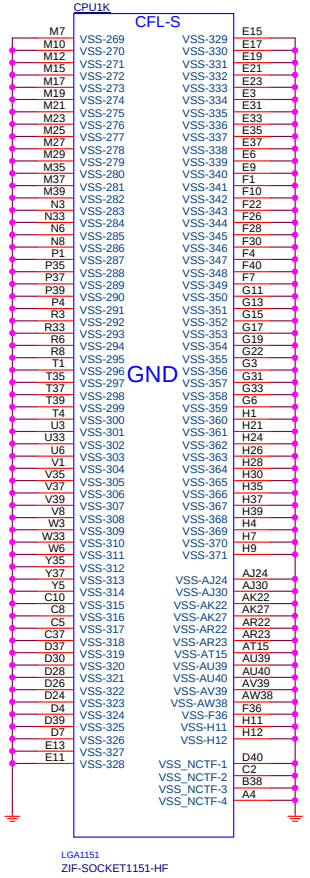

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MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C09	
Size: Custom	Document Description: CPU-GND	Rev: 1.1
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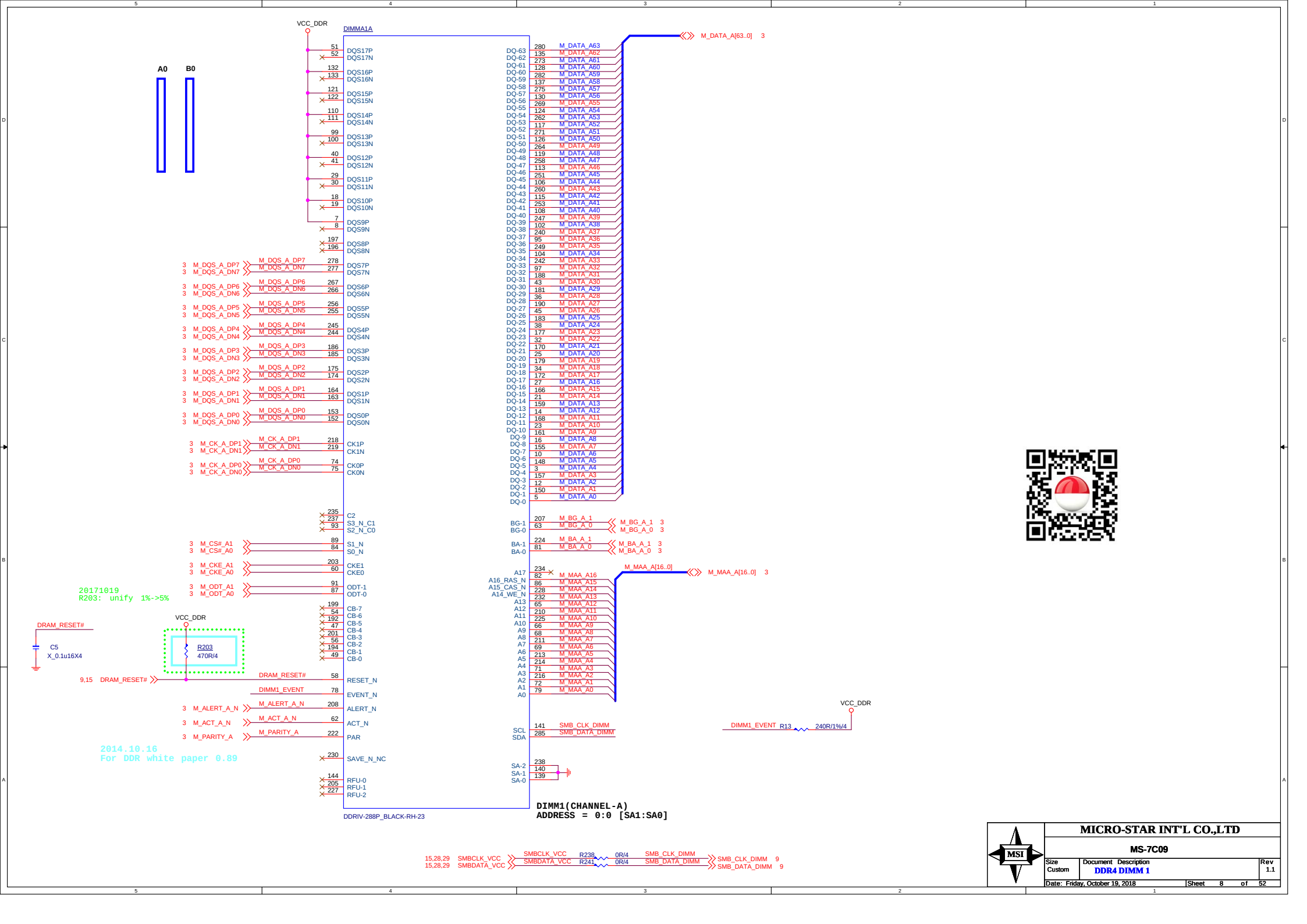
VCC_DDR
DIMMA1A
A0
B0
DDRIV-288P_BLACK-RH-23
M_DATA_A[63..0]
M_MAA_A[16..0]
M_BG_A_1
M_BG_A_0
M_BA_A_1
M_BA_A_0
20171019
R203: unify 1%->5%
DRAM_RESET#
C5
X_0.1u16X4
R203
470R/4
DIMM1_EVENT
R13
240R/1%/4
2014.10.16
For DDR white paper 0.89
SMBCLK_VCC
SMBDATA_VCC
R238
R241
0R/4
SMB_CLK_DIMM
SMB_DATA_DIMM
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7C09
DDR4 DIMM 1
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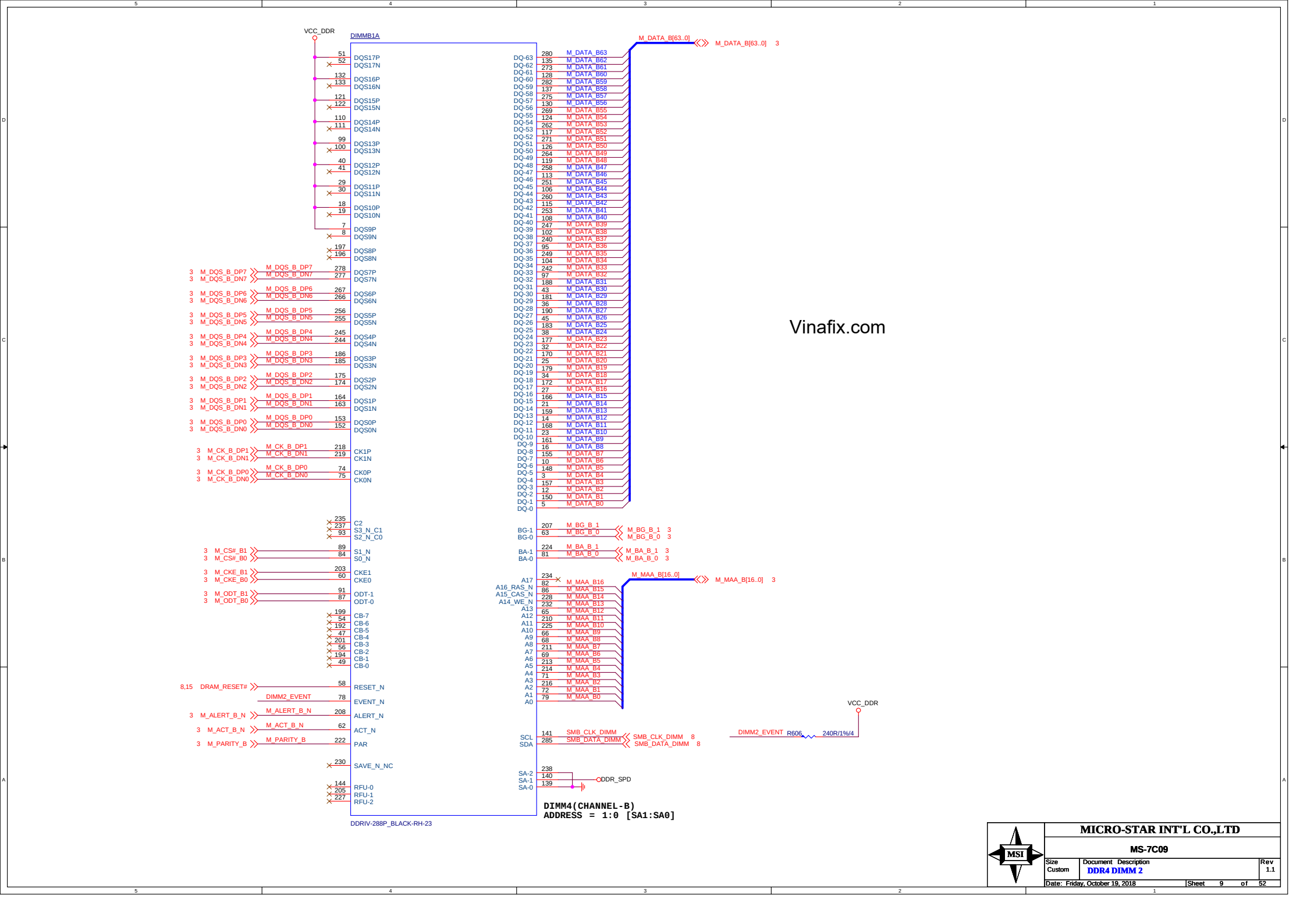
VCC_DDR
DIMMB1A
M_DATA_B[63..0]
M_DATA_B[63..0] 3
DQS17P
DQS17N
DQS16P
DQS16N
DQS15P
DQS15N
DQS14P
DQS14N
DQS13P
DQS13N
DQS12P
DQS12N
DQS11P
DQS11N
DQS10P
DQS10N
DQS9P
DQS9N
DQS8P
DQS8N
DQS7P
DQS7N
DQS6P
DQS6N
DQS5P
DQS5N
DQS4P
DQS4N
DQS3P
DQS3N
DQS2P
DQS2N
DQS1P
DQS1N
DQS0P
DQS0N
CK1P
CK1N
CK0P
CK0N
C2
S3_N_C1
S2_N_C0
S1_N
S0_N
CKE1
CKE0
ODT-1
ODT-0
CB-7
CB-6
CB-5
CB-4
CB-3
CB-2
CB-1
CB-0
RESET_N
EVENT_N
ALERT_N
ACT_N
PAR
SAVE_N_NC
RFU-0
RFU-1
RFU-2
DQ-63 DQ-62 DQ-61 DQ-60 DQ-59 DQ-58 DQ-57 DQ-56 DQ-55 DQ-54 DQ-53 DQ-52 DQ-51 DQ-50 DQ-49 DQ-48 DQ-47 DQ-46 DQ-45 DQ-44 DQ-43 DQ-42 DQ-41 DQ-40 DQ-39 DQ-38 DQ-37 DQ-36 DQ-35 DQ-34 DQ-33 DQ-32 DQ-31 DQ-30 DQ-29 DQ-28 DQ-27 DQ-26 DQ-25 DQ-24 DQ-23 DQ-22 DQ-21 DQ-20 DQ-19 DQ-18 DQ-17 DQ-16 DQ-15 DQ-14 DQ-13 DQ-12 DQ-11 DQ-10 DQ-9 DQ-8 DQ-7 DQ-6 DQ-5 DQ-4 DQ-3 DQ-2 DQ-1 DQ-0
M_DATA_B63 M_DATA_B62 M_DATA_B61 M_DATA_B60 M_DATA_B59 M_DATA_B58 M_DATA_B57 M_DATA_B56 M_DATA_B55 M_DATA_B54 M_DATA_B53 M_DATA_B52 M_DATA_B51 M_DATA_B50 M_DATA_B49 M_DATA_B48 M_DATA_B47 M_DATA_B46 M_DATA_B45 M_DATA_B44 M_DATA_B43 M_DATA_B42 M_DATA_B41 M_DATA_B40 M_DATA_B39 M_DATA_B38 M_DATA_B37 M_DATA_B36 M_DATA_B35 M_DATA_B34 M_DATA_B33 M_DATA_B32 M_DATA_B31 M_DATA_B30 M_DATA_B29 M_DATA_B28 M_DATA_B27 M_DATA_B26 M_DATA_B25 M_DATA_B24 M_DATA_B23 M_DATA_B22 M_DATA_B21 M_DATA_B20 M_DATA_B19 M_DATA_B18 M_DATA_B17 M_DATA_B16 M_DATA_B15 M_DATA_B14 M_DATA_B13 M_DATA_B12 M_DATA_B11 M_DATA_B10 M_DATA_B9 M_DATA_B8 M_DATA_B7 M_DATA_B6 M_DATA_B5 M_DATA_B4 M_DATA_B3 M_DATA_B2 M_DATA_B1 M_DATA_B0
BG-1 BG-0
M_BG_B_1 M_BG_B_0
M_BG_B_1 3
M_BG_B_0 3
BA-1 BA-0
M_BA_B_1 M_BA_B_0
M_BA_B_1 3
M_BA_B_0 3
A17 A16_RAS_N A15_CAS_N A14_WE_N A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
M_MAA_B16 M_MAA_B15 M_MAA_B14 M_MAA_B13 M_MAA_B12 M_MAA_B11 M_MAA_B10 M_MAA_B9 M_MAA_B8 M_MAA_B7 M_MAA_B6 M_MAA_B5 M_MAA_B4 M_MAA_B3 M_MAA_B2 M_MAA_B1 M_MAA_B0
M_MAA_B[16..0]
M_MAA_B[16..0] 3
SCL SDA
SMB_CLK_DIMM SMB_DATA_DIMM
SMB_CLK_DIMM 8
SMB_DATA_DIMM 8
SA-2 SA-1 SA-0
DDR_SPD
DIMM2_EVENT
R606
240R/1%/4
VCC_DDR
M_DQS_B_DP7 M_DQS_B_DN7
M_DQS_B_DP6 M_DQS_B_DN6
M_DQS_B_DP5 M_DQS_B_DN5
M_DQS_B_DP4 M_DQS_B_DN4
M_DQS_B_DP3 M_DQS_B_DN3
M_DQS_B_DP2 M_DQS_B_DN2
M_DQS_B_DP1 M_DQS_B_DN1
M_DQS_B_DP0 M_DQS_B_DN0
M_CK_B_DP1 M_CK_B_DN1
M_CK_B_DP0 M_CK_B_DN0
M_CS#_B1 M_CS#_B0
M_CKE_B1 M_CKE_B0
M_ODT_B1 M_ODT_B0
DRAM_RESET#
DIMM2_EVENT
M_ALERT_B_N
M_ACT_B_N
M_PARITY_B
DDRIV-288P_BLACK-RH-23
DIMM4(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
Vinafix.com
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description DDR4 DIMM 2
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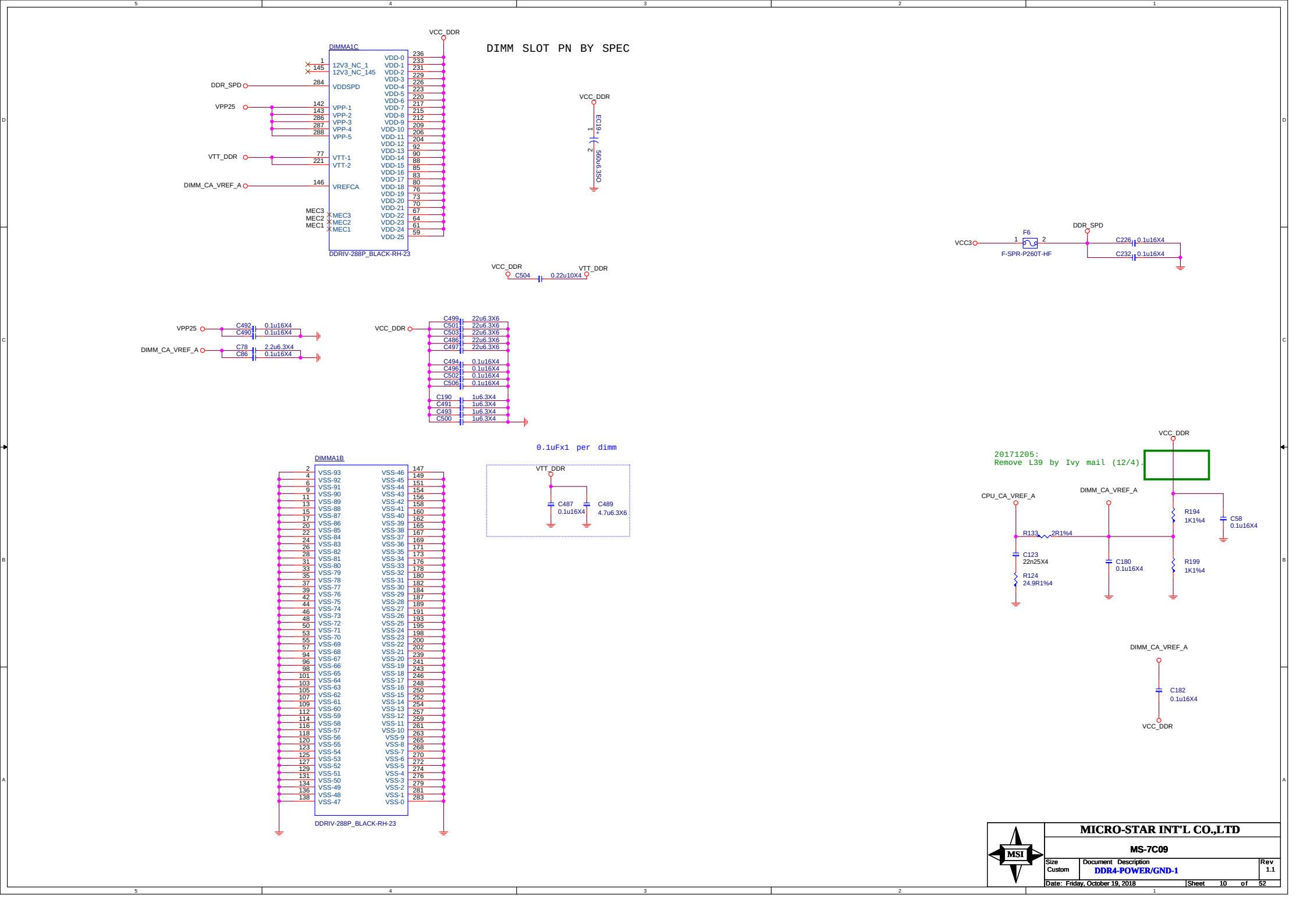
DIMM SLOT PN BY SPEC
DIMMA1C
DDRIV-288P_BLACK-RH-23
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
VDDSPD
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT-1
VTT-2
VREFCA
MEC3
MEC2
MEC1
EC19+
560u6.3SO
C504
0.22u10X4
C492
C490
0.1u16X4
C78
C86
2.2u6.3X4
C499
C501
C503
C486
C497
22u6.3X6
C494
C496
C502
C506
C190
C491
C493
C500
1u6.3X4
0.1uFx1 per dimm
C487
C489
4.7u6.3X6
DIMMA1B
VCC3
F6
F-SPR-P260T-HF
C226
C232
20171205:
Remove L39 by Ivy mail (12/4).
CPU_CA_VREF_A
R133
2R1%4
R194
1K1%4
C58
C123
22n25X4
R124
24.9R1%4
C180
R199
C182
MICRO-STAR INT'L CO.,LTD
MS-7C09
Size
Custom
Document Description
DDR4-POWER/GND-1
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1.1
Date: Friday, October 19, 2018
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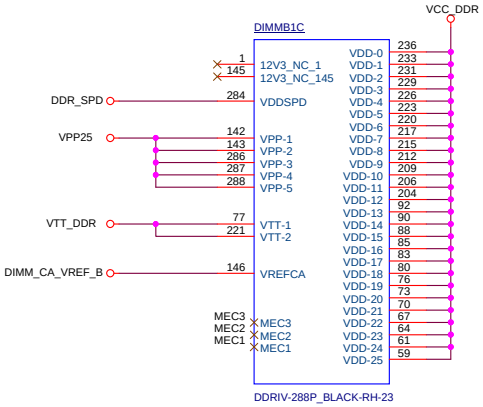
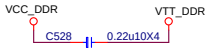
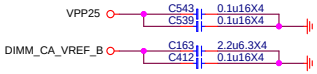
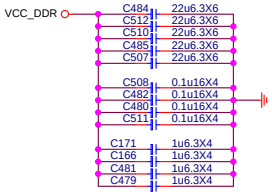


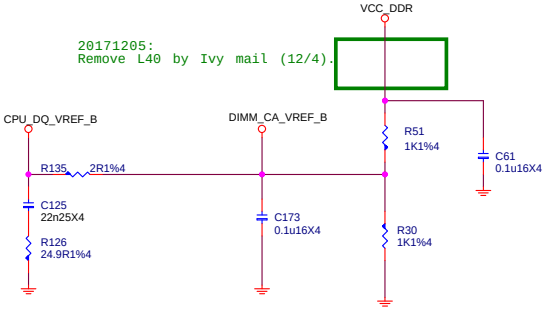


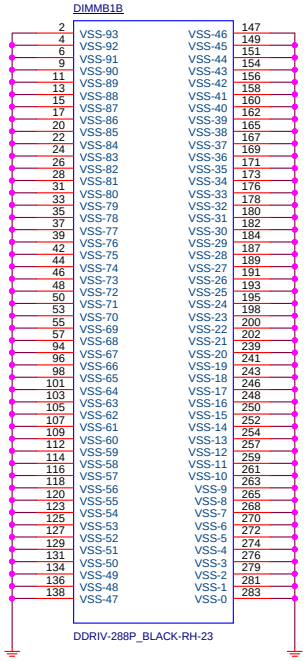
Place close to DIMM2



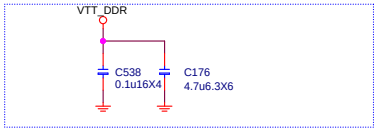


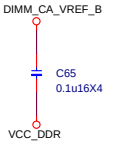
20171205:
Remove L40 by Ivy mail (12/4).





0.1uFx1 per dimm





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C09	
Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 1.1
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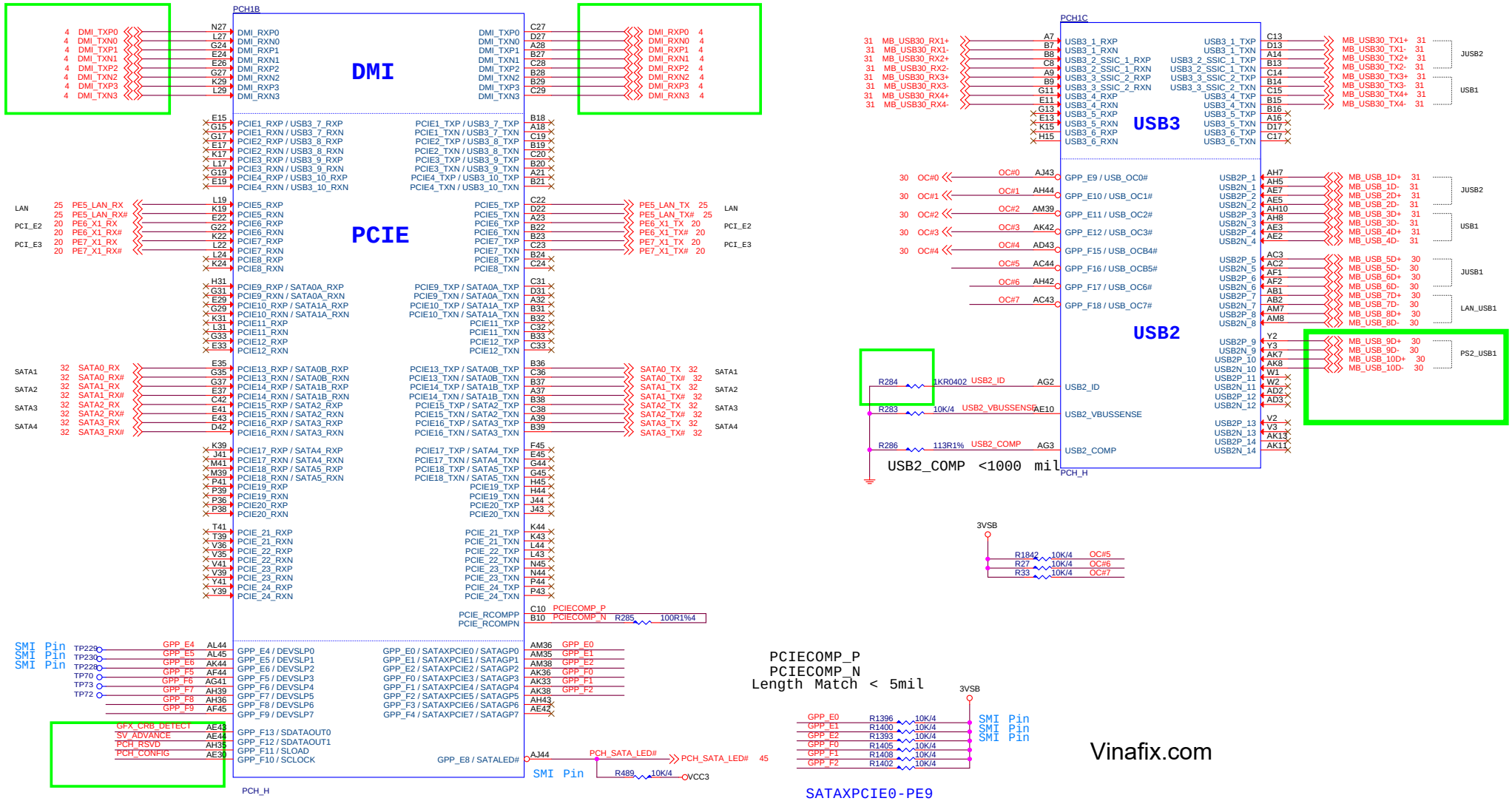

MICRO-STAR INT'L CO.,LTD	
MS-7C09	
Size: Custom	Document Description: PCH-USB/PCIE/DMI/SATA
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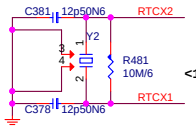
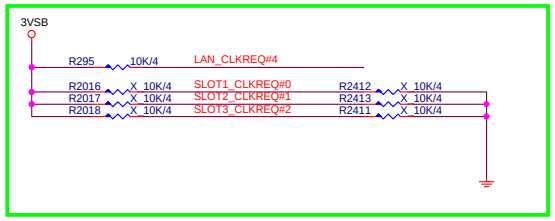
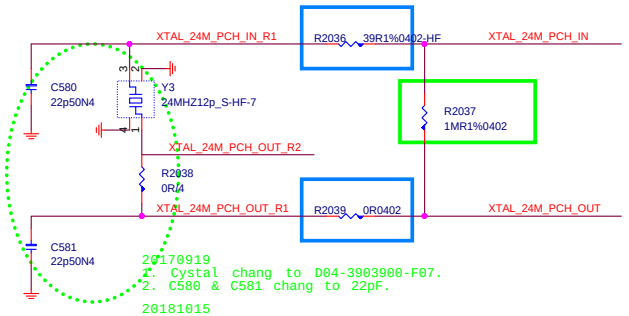
RTC Block

Close to PCH



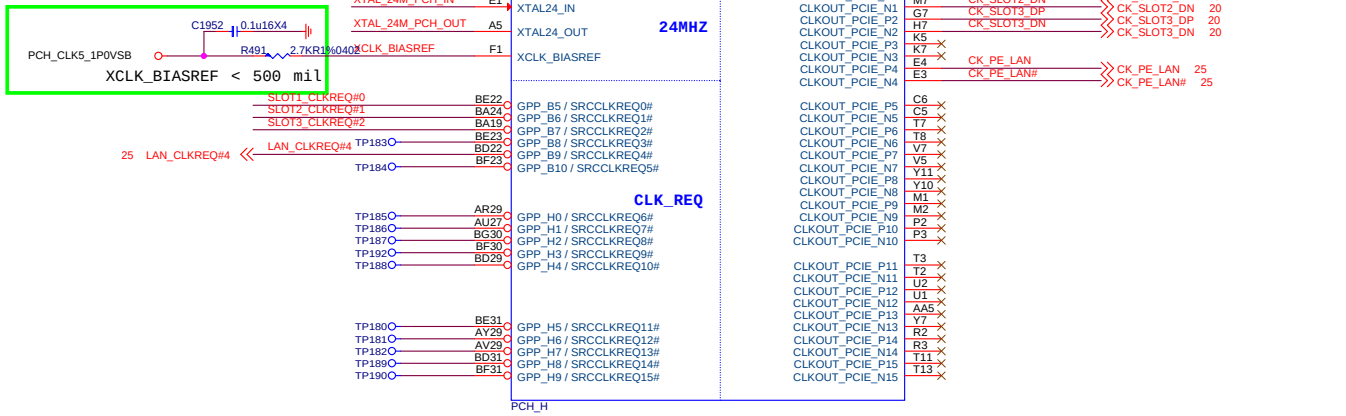
<1 inch



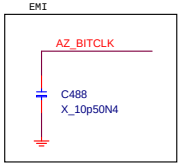


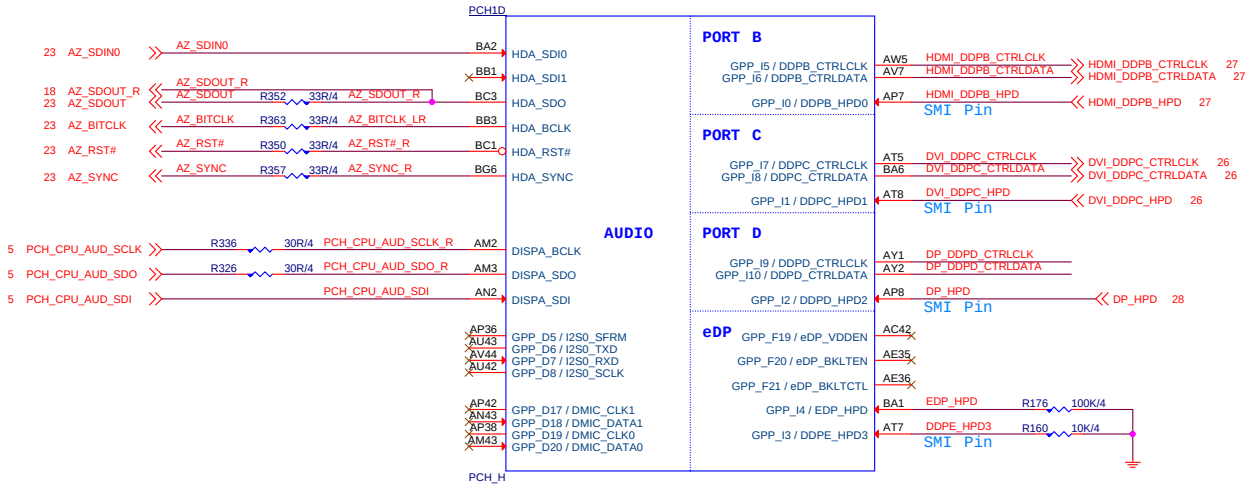
20170919
1. Cystal chang to D04-3903900-F07.
2. C580 & C581 chang to 22pF.

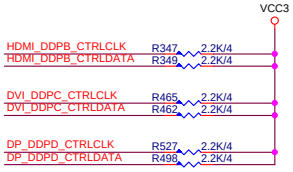
20181015
1. R2036 change to 39ohm



20171019
R1365: unify 1%->5%





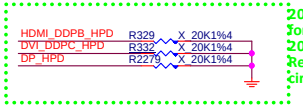


DDPx_CTRLCLK/DATA:
Enable: Pull up to 3.3V
Disable: No connect

Port B HDMI

Port C DVI

Port D DisplayPort to VGA



20170927:
for BOM modify.
20170928:
Reserve DP_HPD to GND
cirsuit.

Add DDI_HPD pull down

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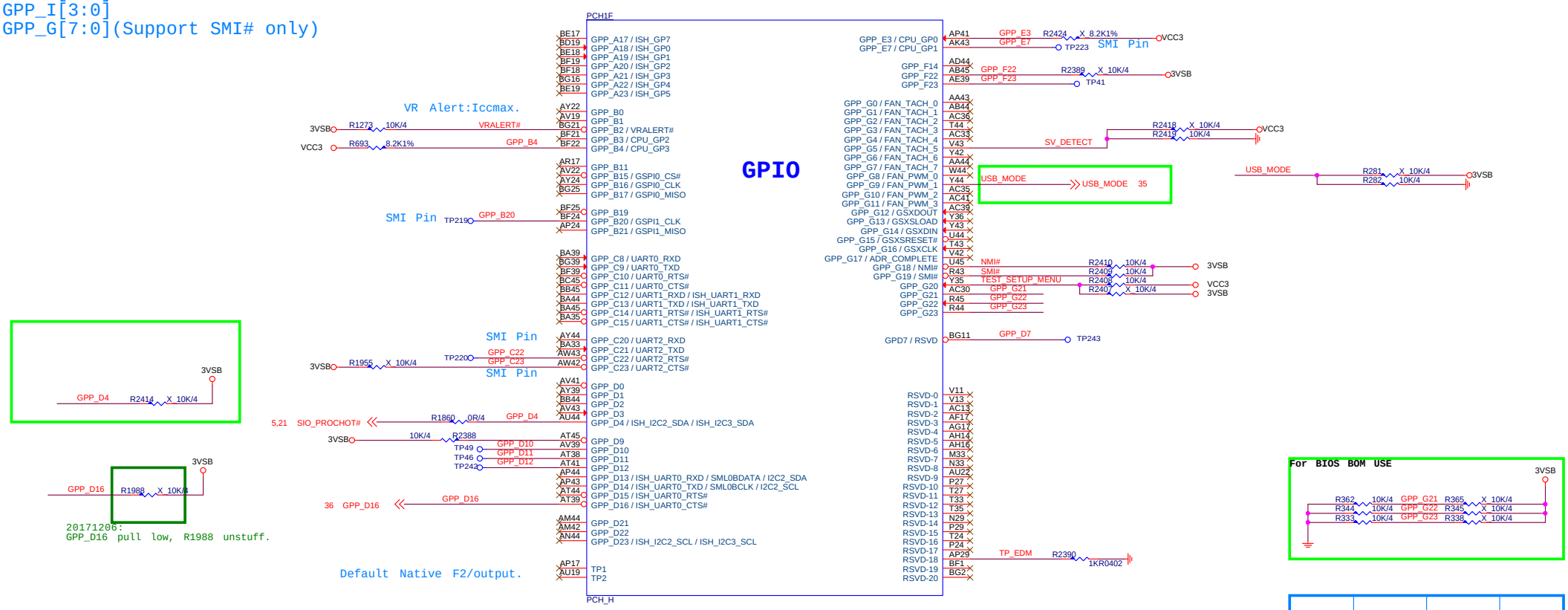
GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)



	GPP_I12	GPP_I13	GPP_I14
H310_VH	0	0	0
H310_VD	0	0	1

Vinafix.com

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CRB no RSVD.

CRB 3VDUAL

C1884 C1885 C188 、C18 87 clo se P CH 500~1000mil

20171208:
Follow Eric mail 20171129,
1. reserved to VCC3.
2. reserved MLCC 1up for LPC EMI.

ESPI_CS1#/ALERT0#/ALERT1#(Server Only)

R2360~R2363 close PCH 500~1000mil.

To SIO

FAN MODE USE

20170922
Add 0LL function.

LANPHY USE by SPEC

20170922
Add 0LL function.

20171006
follow 1003 *300 series update.

PCH_H

LPC

SMB

Power Management

STRAP

SPI

JTAG

Default Native E1/input/3VDSW

Place R390 within 200mil of PCH.

PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan

20170919
add RC delay on PCH_DPWROK, laster than RSMRST# when down.
20171115
1. Add SILEGO- R2257 unstuff connect DPWROK_SLG.
2. Add SILEGO- R2313 unstuff connect RSMRST#_SLG.

CRB RSVD pull up to +V3P3_DUAL.
20171208:
Follow Eric mail 20171129,
PCH_CLKRUN# reserved to 3VSB.

Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.

Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.

Place within 1.5" of PCH Pin.

2016.01.13 Add RSMRST# Patch Circuit
When NO Battery Can't Power On

20171122:
add SILGO sequency IC Q12 unstuff.

RSMRST# USE solution

放背面分支點

RTC

CRB

2014.12.29

Chassis Intrusion

擺在一起注意 到 所有的SMBUS的分支)

CFL CRB

20171012:
2N7002*2 -> 2N7002D

20180130
for SMBus low level,
R452、R426、R612、R7 2
->1.6KR.

SMBUS ESD

close to PCH

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MS-7C09	
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC
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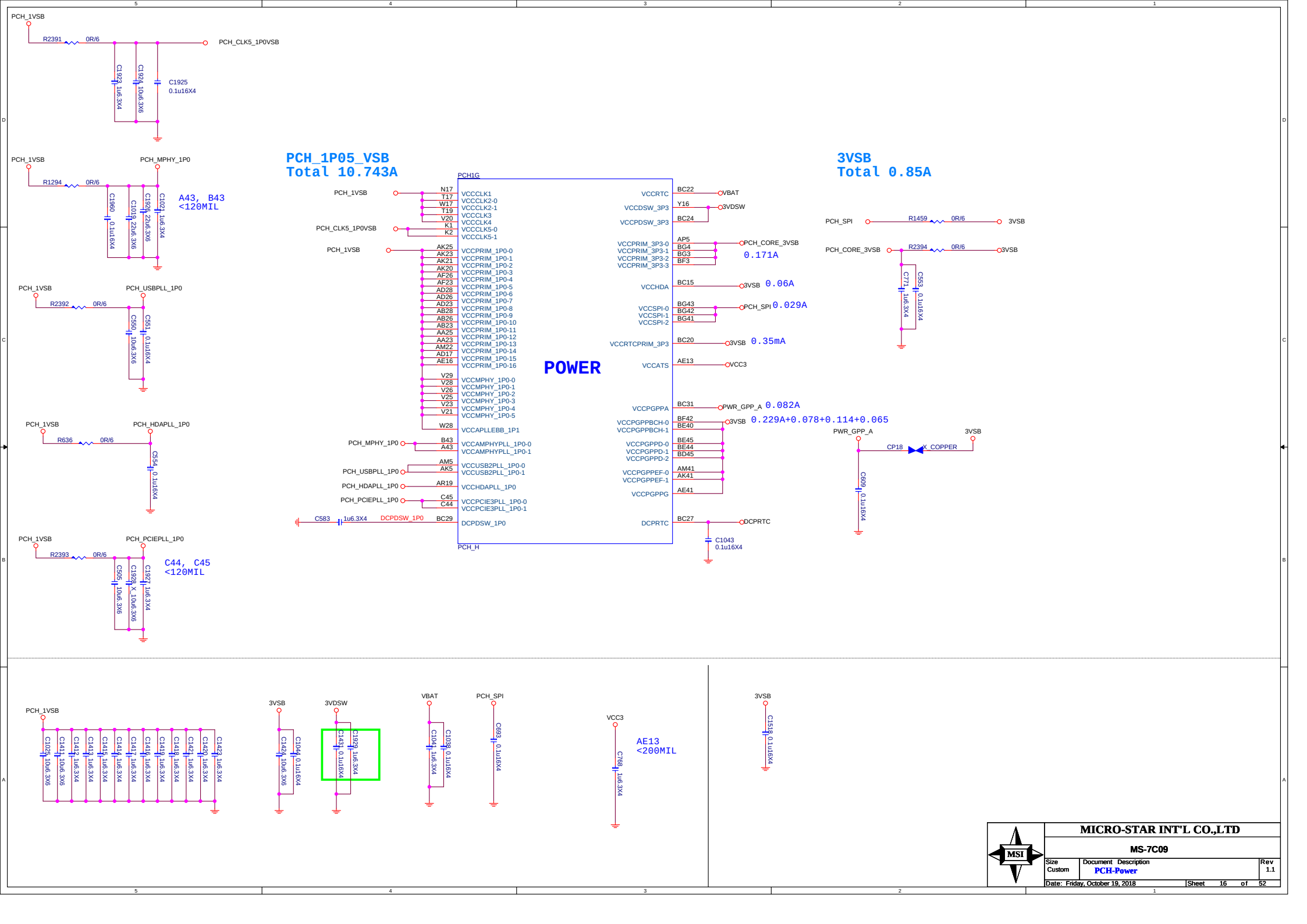
PCH_1VSB
R2391 0R/6
PCH_CLK5_1P0VSB
C1923 1u6.3X4
C1924 10u6.3X6
C1925 0.1u16X4
PCH_1VSB
PCH_MPHY_1P0
R1294 0R/6
C1960 0.1u16X4
C1019 22u6.3X6
C1926 22u6.3X6
C1021 1u6.3X4
A43, B43
<120MIL
PCH_1VSB
PCH_USBPLL_1P0
R2392 0R/6
C550 10u6.3X6
C551 0.1u16X4
PCH_1VSB
PCH_HDAPLL_1P0
R636 0R/6
C554 0.1u16X4
PCH_1VSB
PCH_PCIEPLL_1P0
R2393 0R/6
C505 10u6.3X6
C1928 X_10u6.3X6
C1927 1u6.3X4
C44, C45
<120MIL
PCH_1P05_VSB
Total 10.743A
PCH1G
PCH_1VSB
PCH_CLK5_1P0VSB
PCH_1VSB
PCH_MPHY_1P0
PCH_USBPLL_1P0
PCH_HDAPLL_1P0
PCH_PCIEPLL_1P0
C583 1u6.3X4 DCPDSW_1P0
POWER
PCH_H
VCCRTC BC22 VBAT
VCCDSW_3P3 Y16 3VDSW
VCCPDSW_3P3 BC24
VCCPRIM_3P3-0 VCCPRIM_3P3-1 VCCPRIM_3P3-2 VCCPRIM_3P3-3 AP5 BG4 BG3 BF3 PCH_CORE_3VSB
0.171A
VCCHDA BC15 3VSB 0.06A
VCCSPI-0 VCCSPI-1 VCCSPI-2 BG43 BG42 BG41 PCH_SPI 0.029A
VCCRTCPRIM_3P3 BC20 3VSB 0.35mA
VCCATS AE13 VCC3
VCCPGPPA BC31 PWR_GPP_A 0.082A
VCCPGPPBCH-0 VCCPGPPBCH-1 BF42 BE40 3VSB 0.229A+0.078+0.114+0.065
VCCPGPPD-0 VCCPGPPD-1 VCCPGPPD-2 BE45 BE44 BD45
VCCPGPPEF-0 VCCPGPPEF-1 AM41 AK41
VCCPGPPG AE41
DCPRTC BC27 DCPRTC
C1043 0.1u16X4
3VSB
Total 0.85A
PCH_SPI R1459 0R/6 3VSB
PCH_CORE_3VSB R2394 0R/6 3VSB
C771 1u6.3X4
C553 0.1u16X4
PWR_GPP_A
CP18 X_COPPER
3VSB
C689 0.1u16X4
PCH_1VSB
C1038 C1411 C1412 C1413 C1414 C1415 C1417 C1416 C1418 C1419 C1421 C1420 C1422
10u6.3X6 1u6.3X4
3VSB
3VDSW
C1042 10u6.3X6
C1044 0.1u16X4
C143 0.1u16X4
C1923 1u6.3X4
VBAT
C1041 1u6.3X4
C1039 0.1u16X4
PCH_SPI
C693 0.1u16X4
VCC3
C768 1u6.3X4
AE13
<200MIL
3VSB
C1518 0.1u16X4
MICRO-STAR INT'L CO.,LTD
MS-7C09
Size Custom
Document Description PCH-Power
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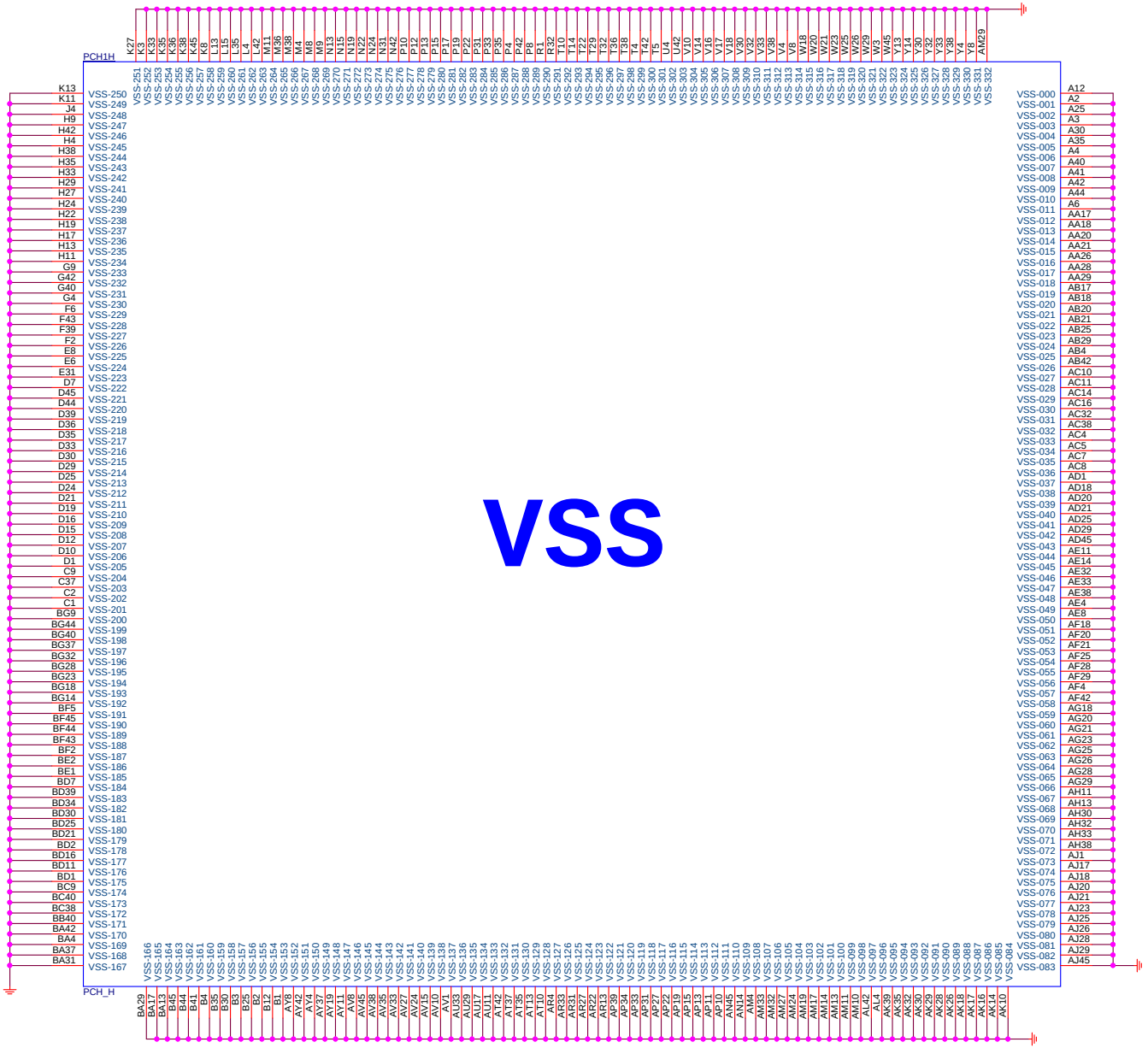

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Size: Custom	Document Description: PCH-GND
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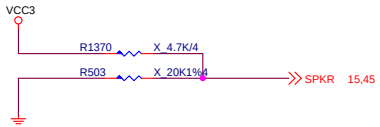
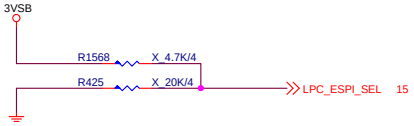
TOP Swap



Internal pull-down 20K is disabled after PLTRST#

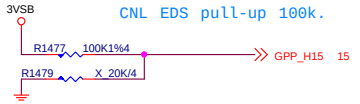
LPC eSPI Mode



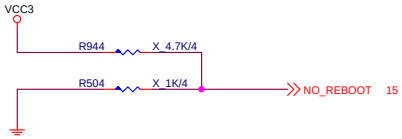
0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Reserved



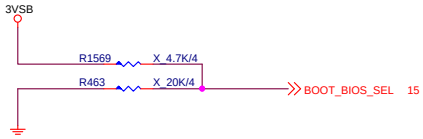
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

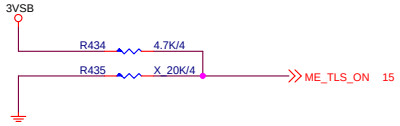
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

AMT and SBA with confidentiality

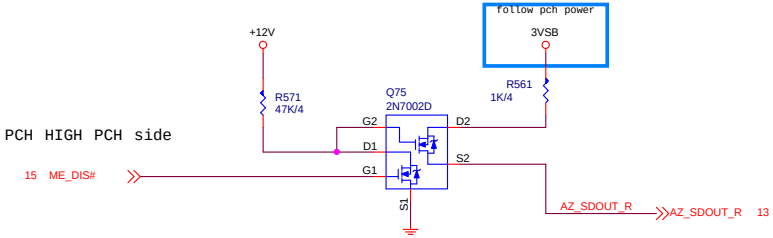


0 : DISABLE
1 : ENABLE (Default)

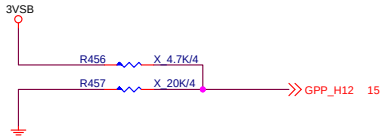
Internal pull-down 20K is disabled after RSMRST

HDA_SDO

ME flash by GPIO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

Reserved

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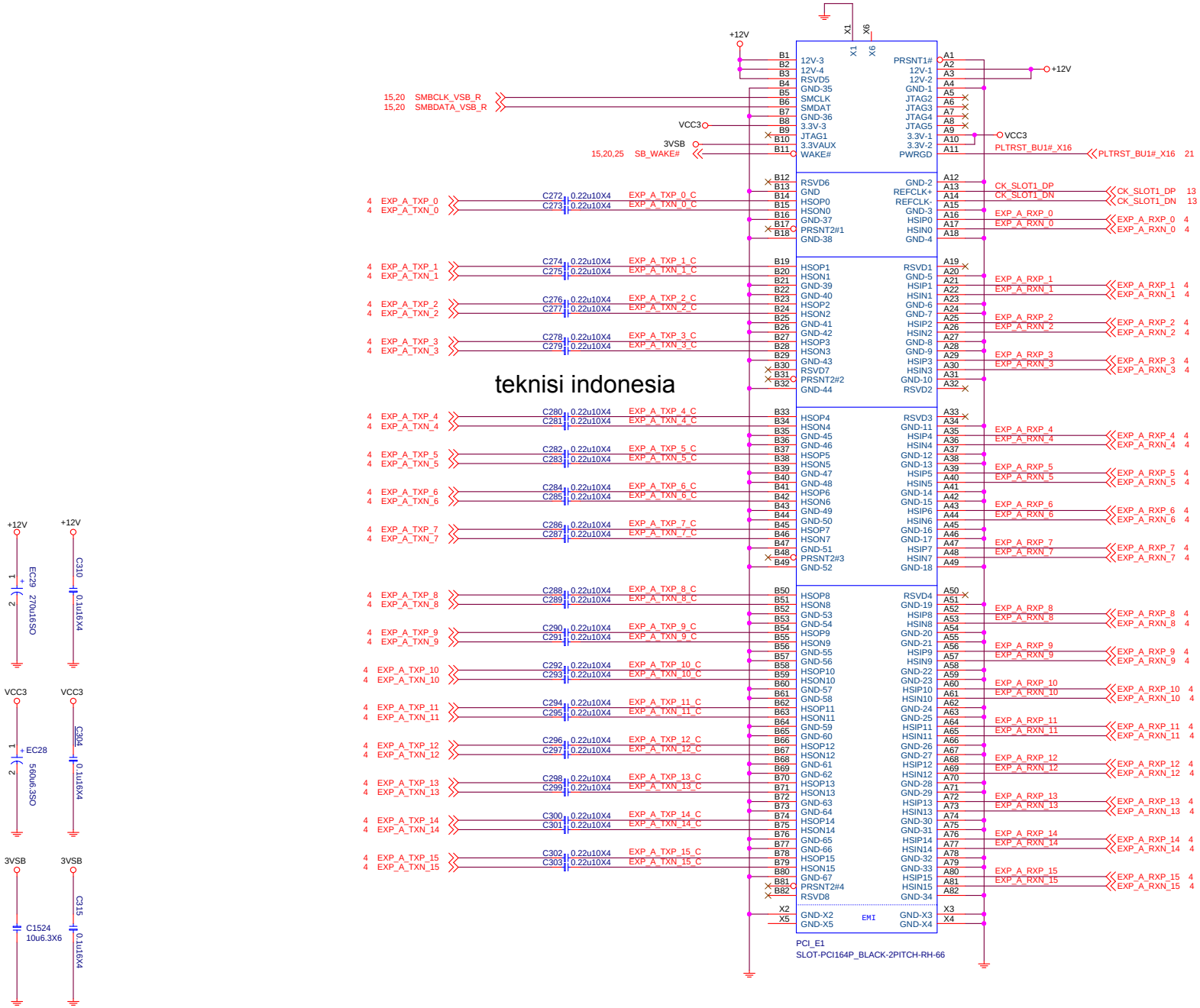

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Size: Custom	Document Description: PCIE SLOT-CPU(X16)
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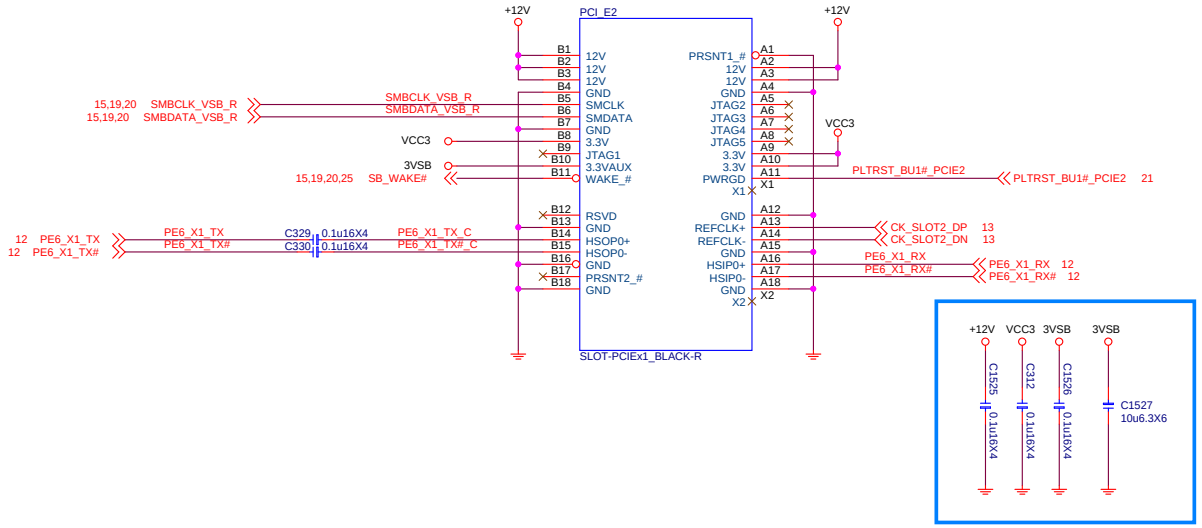

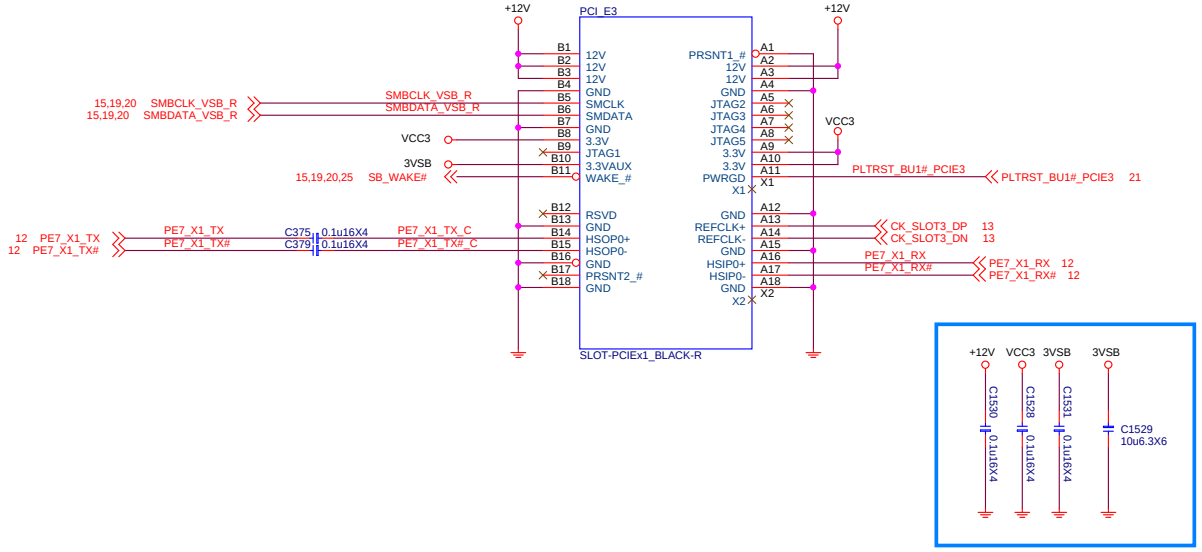

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Size: Custom	Document Description: PCIE SLOT-PCH(X1)	Rev: 1.1
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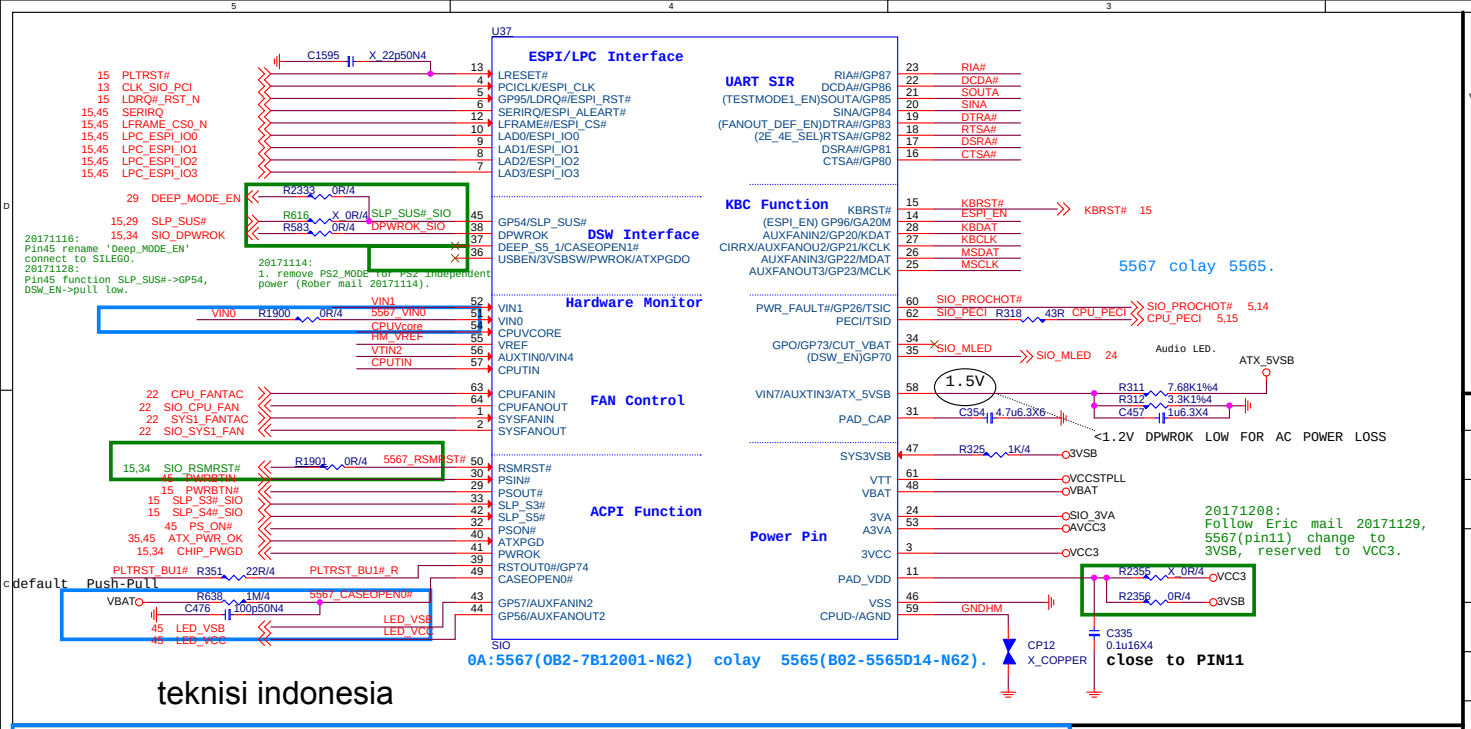
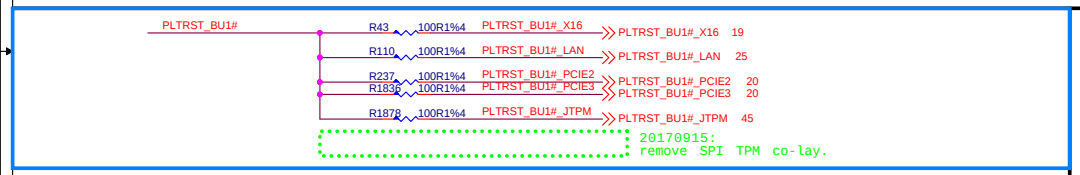
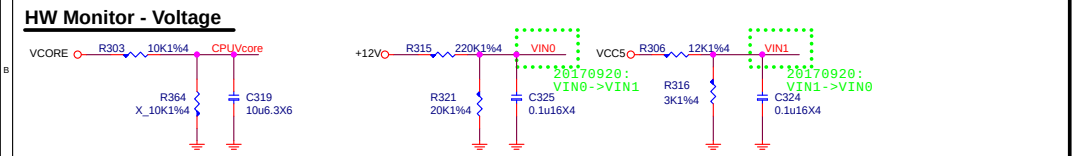
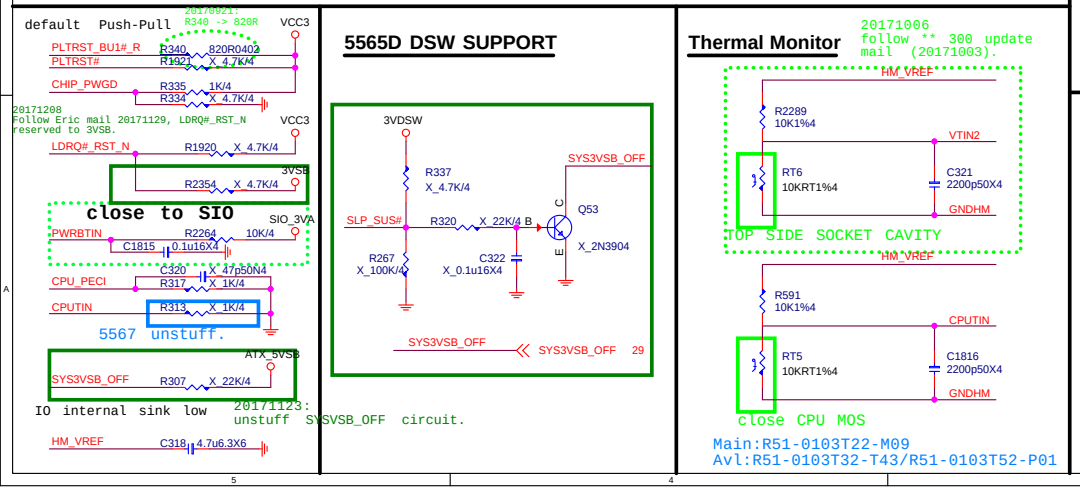
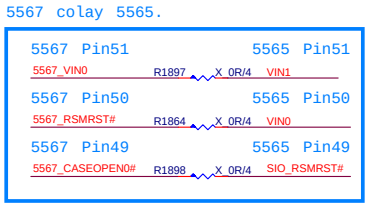


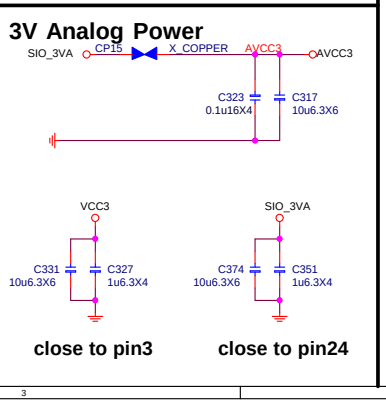
teknisi indonesia

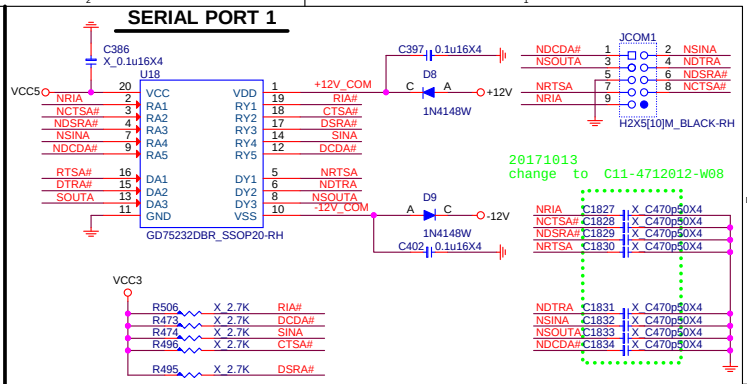




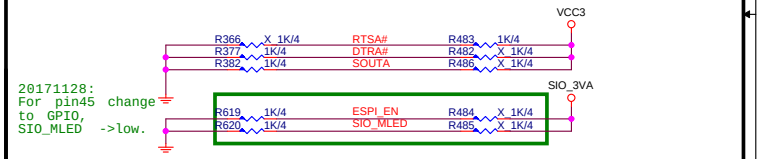


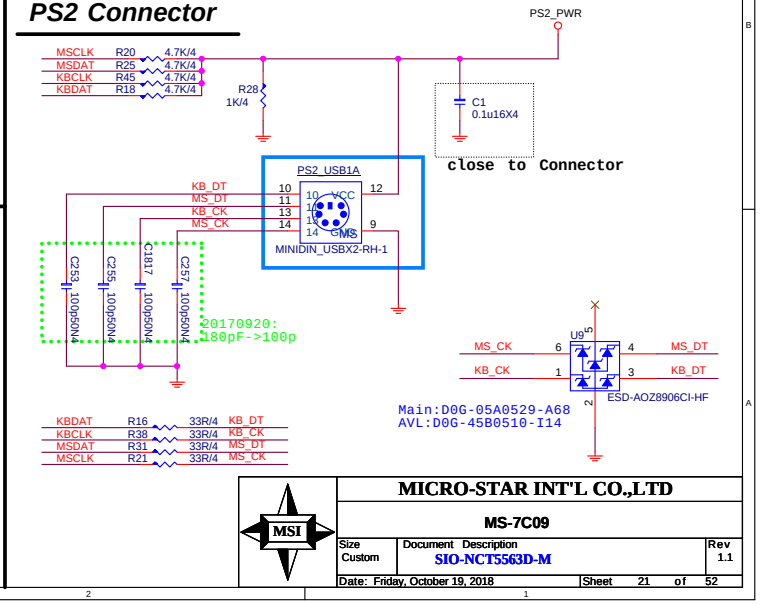






PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN





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Size: Custom	Document Description: SIO-NCT5563D-M
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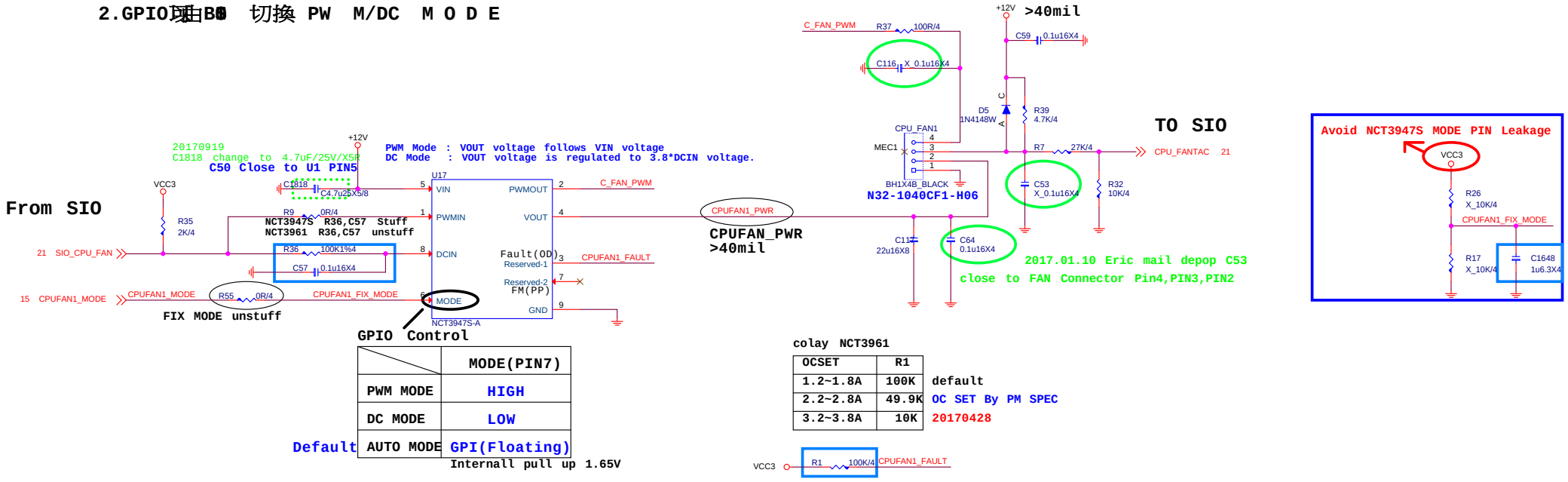
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO由B0 切换 PW M/DC M O D E



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

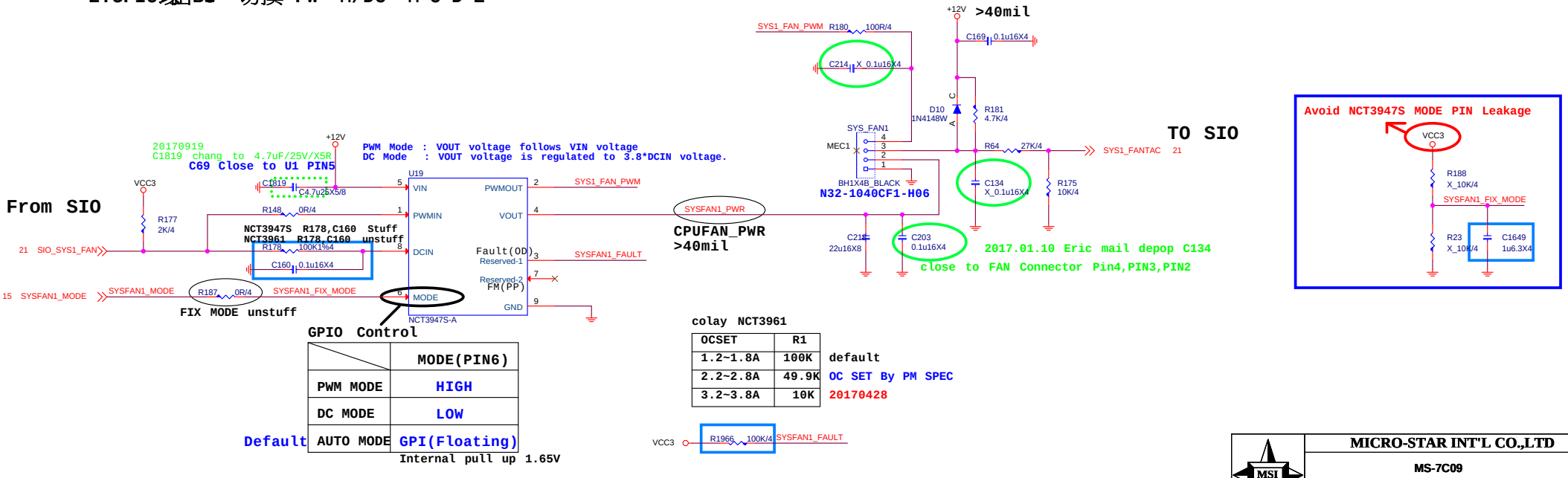
Internall pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO由B0 切换 PW M/DC M O D E



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internal pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

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Type B:
ALC892/887

CA14 closed PIN25
CA30 closed PIN38
CA31 closed PIN38

12mA
Closed codec
48mA
Closed Codec
CA16.CA17 close to Pin27

ALC887-CG-RH

Varistor
D0G-2710510-I05
Close to Jack

2.2k for better recording quality

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

20171115:
follow Robert mail(20171114), mlcc change to ESD.

Vinafix.com

EMI

Closed Codec

0R for cost down

CA23,CA24 close to LA1

Varistor
D0G-2710510-I05
Close to Jack

Close to Front panel
For HDA/AC97 front cable.

N31-2051411-H06

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Size: Custom	Document Description: AUDIO - ALC892/887
Rev: 1.1	
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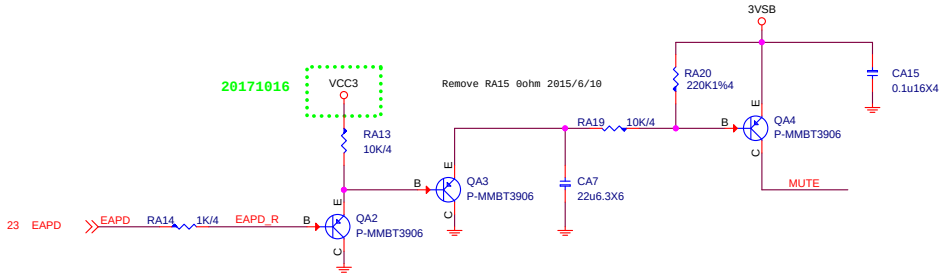
Rear Line OUT De-POP circuit

History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

De-pop circuit for Rear Line out & Front Headphone out)

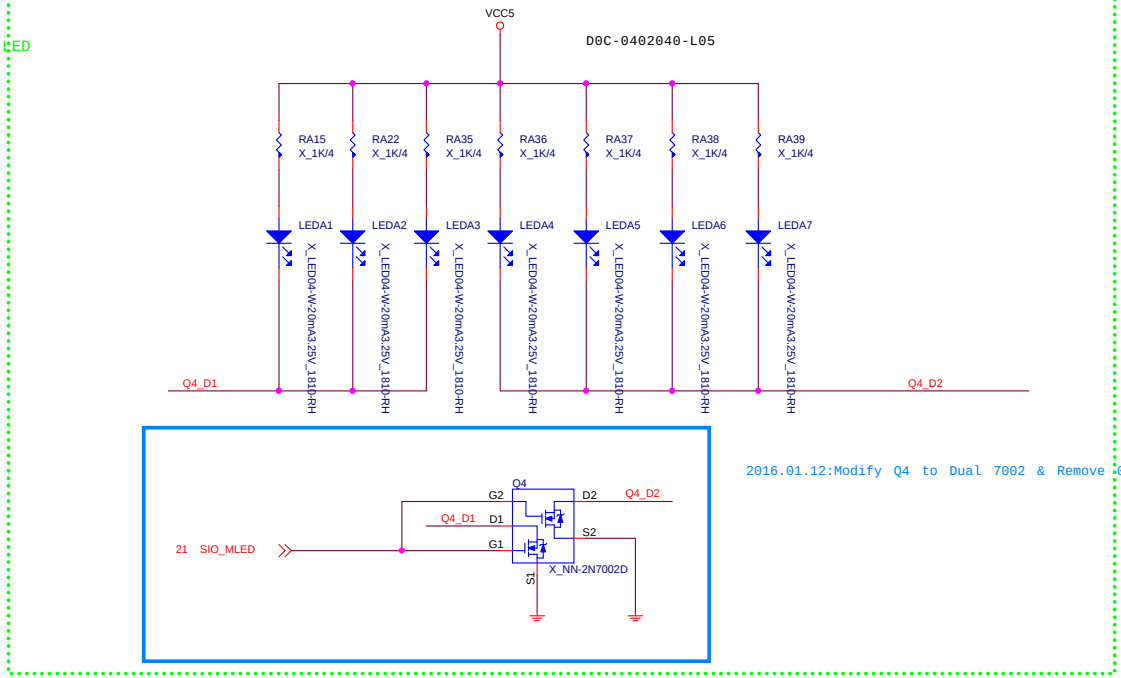


Digital

Analog

Audio LED

20170915:
Cancel Audio LED



2016.01.12:Modify Q4 to Dual 7002 & Remove 0R

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	MS-7C09	
Size: Custom	Document Description: AUDIO - depop circuit	Rev: 1.1
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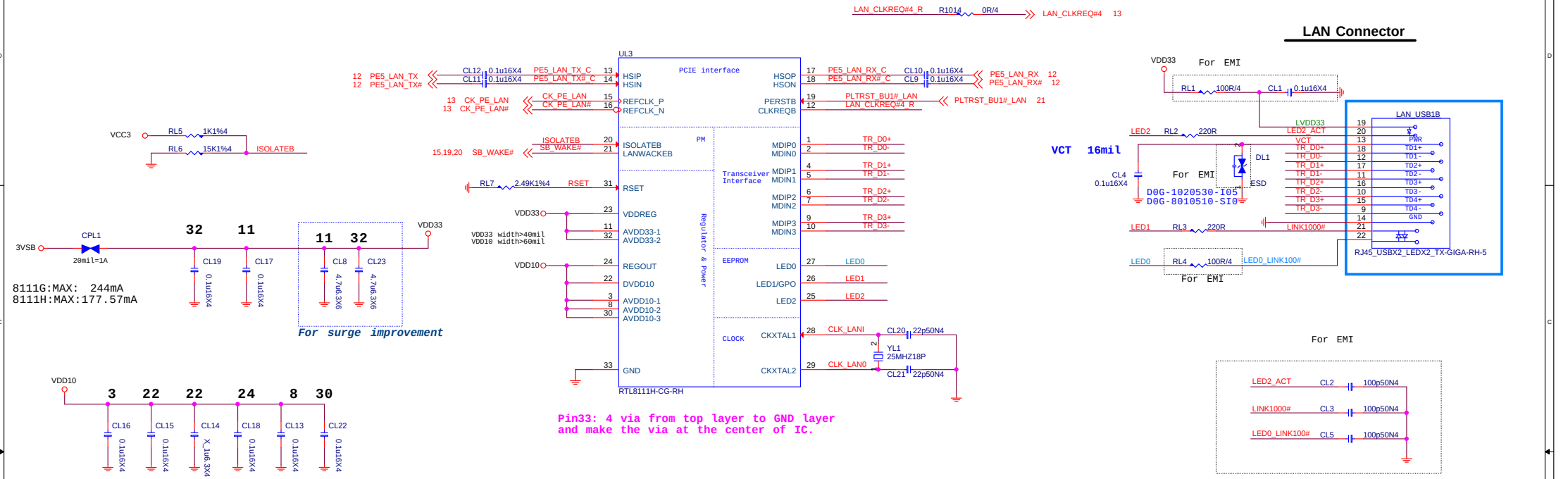
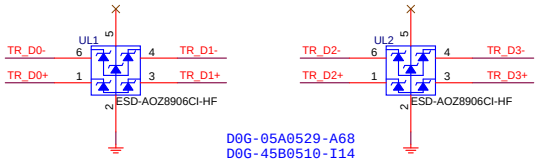
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



ESD Protect

UL1 & UL2 close to connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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Custom	LAN - RTL8111H	1.1

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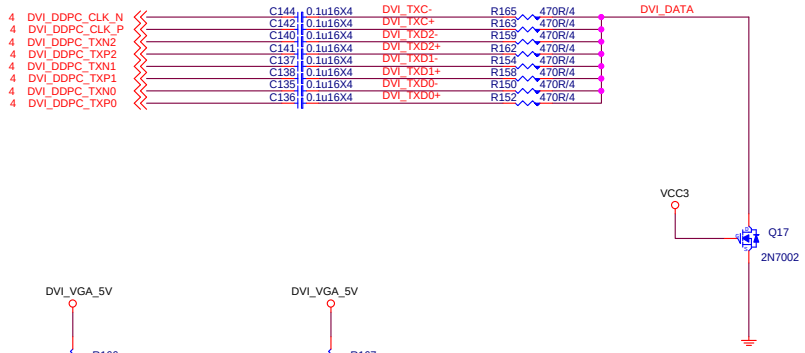
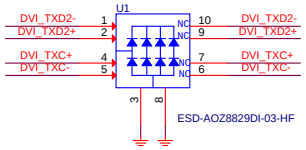
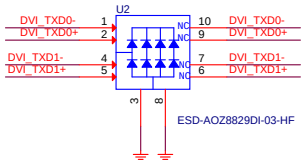
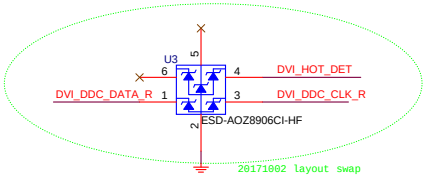
DVI level shifter

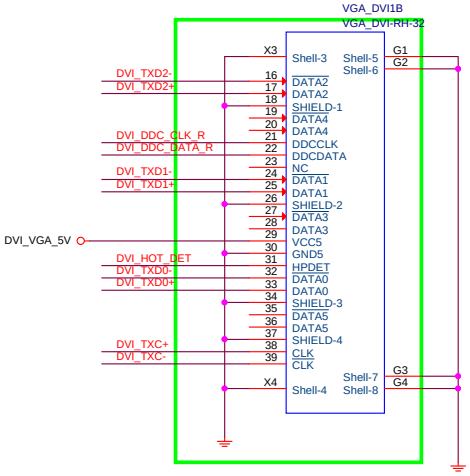
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

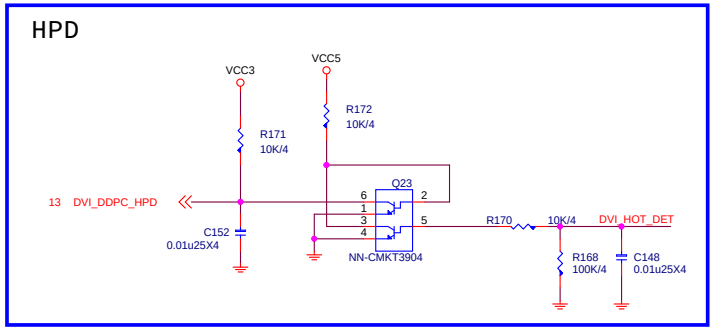


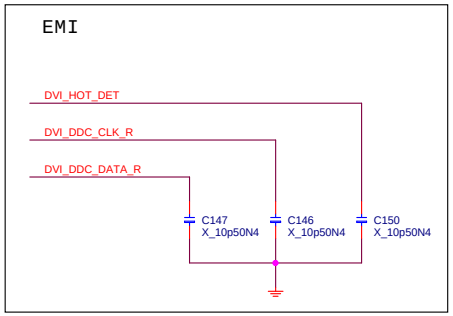


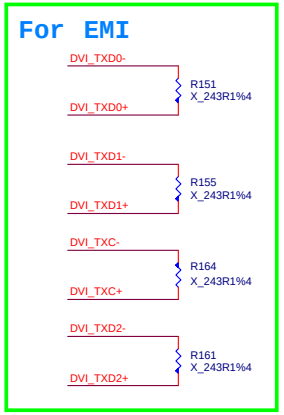












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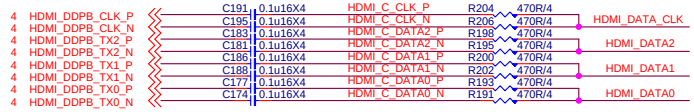
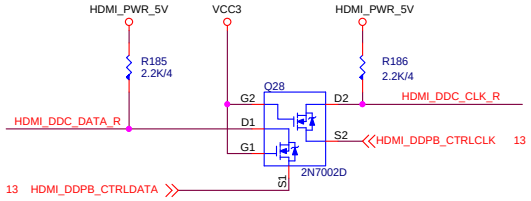
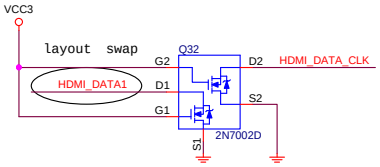
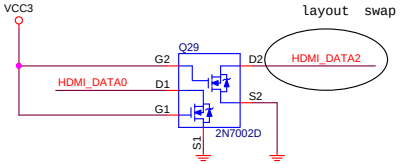
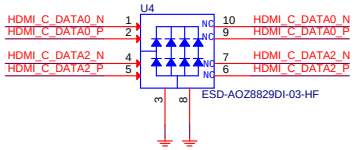
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

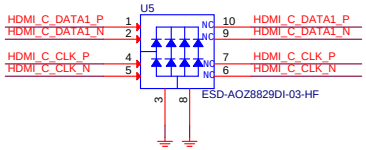




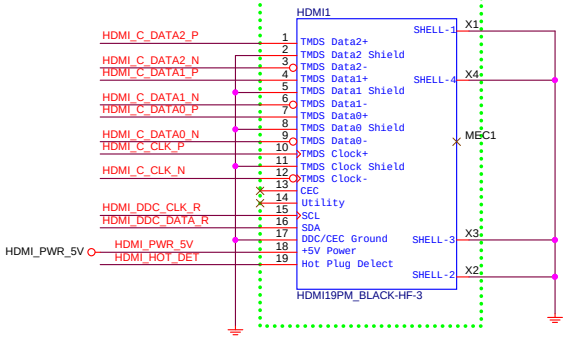


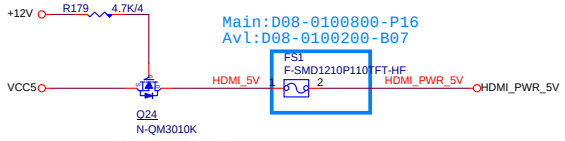




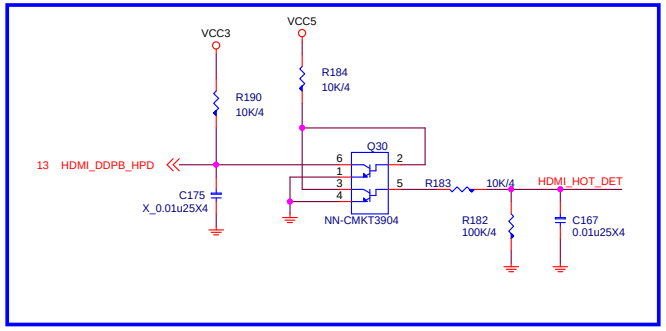


20170920:
connector->N5Y-19M0721-L06

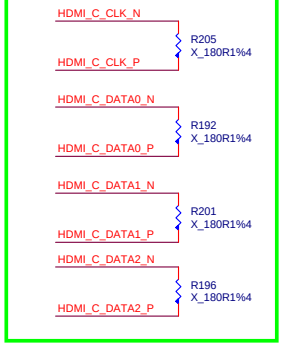


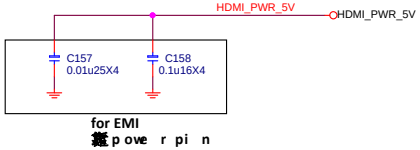


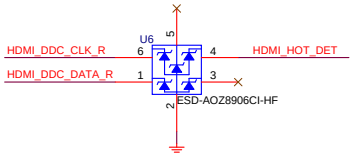
HPD



For EMI







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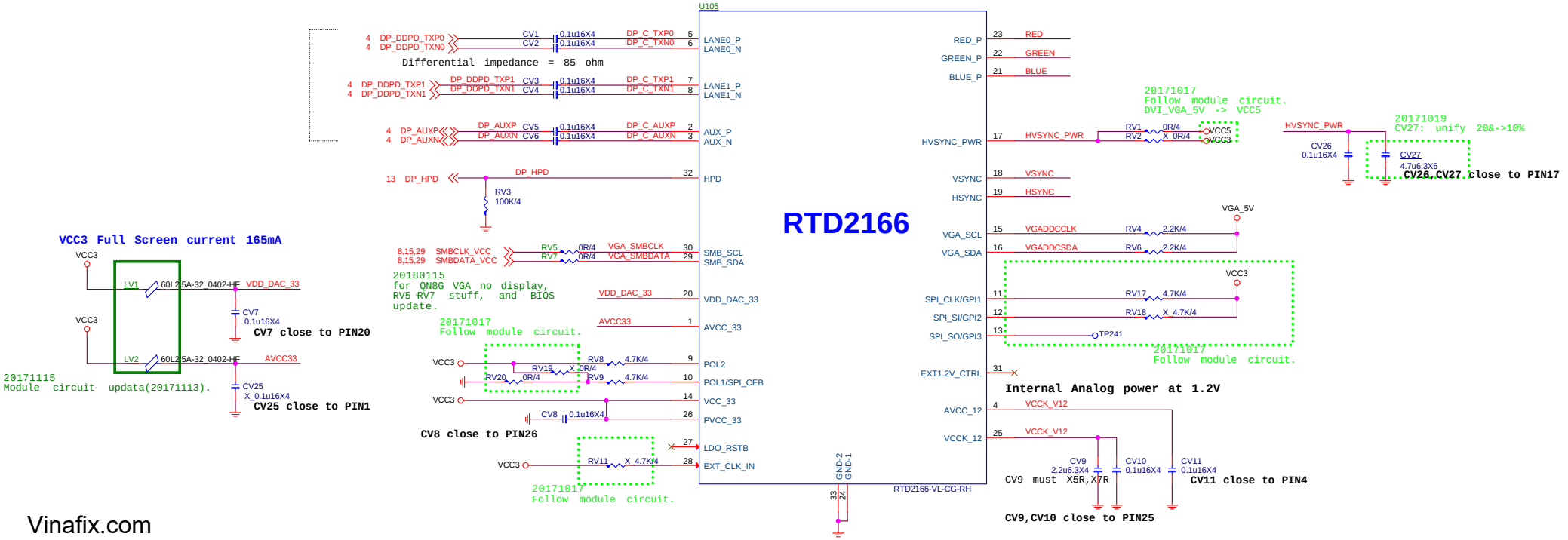
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

20171130:
U105 -> B0B-02166C-R09, change R,G,B internal driving.



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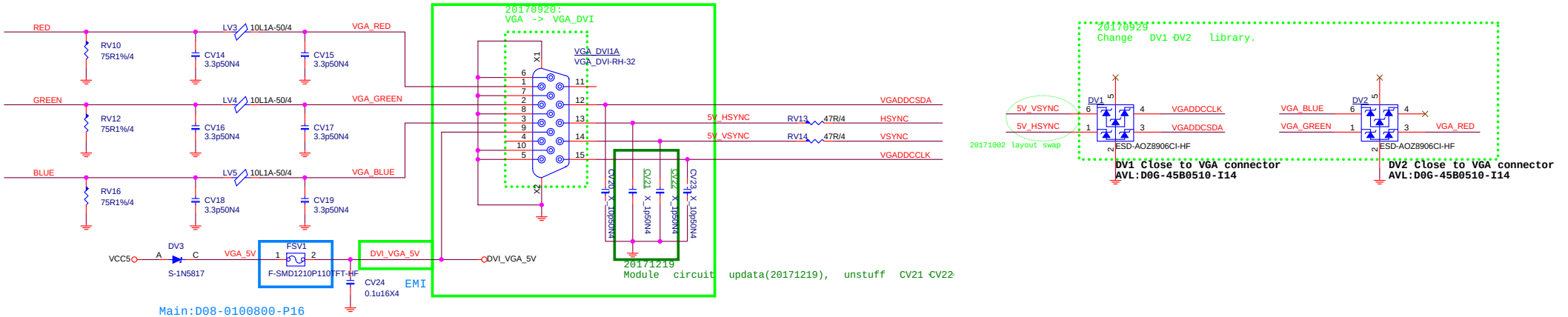
RTD2166 SMBus address is 68h.



Main:D08-0100800-P16
Avl:D08-0100200-B07

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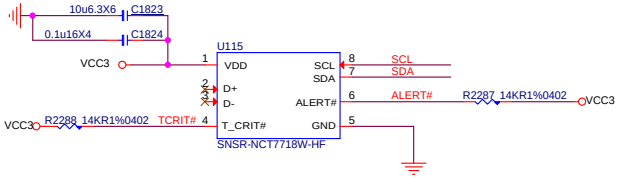
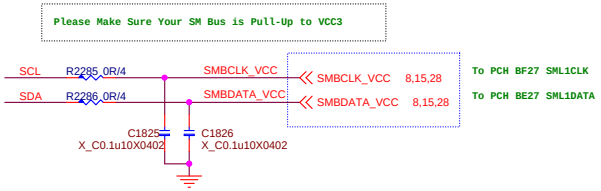
NCT7718W

20171006
follow ** 300 update mail(2017100), Add for monitored system thremal monitor.

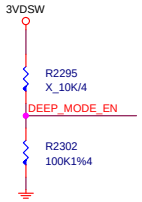
TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



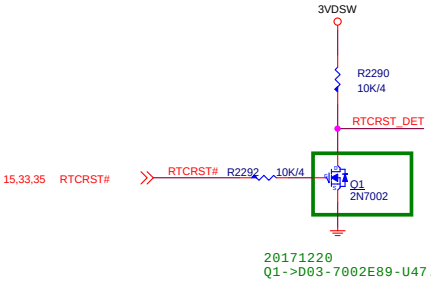


NCT7718W SM Bus address is 98h (1001100xb)
Default: ALERT# Output Comparator Mode

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

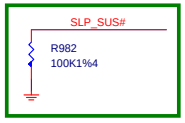


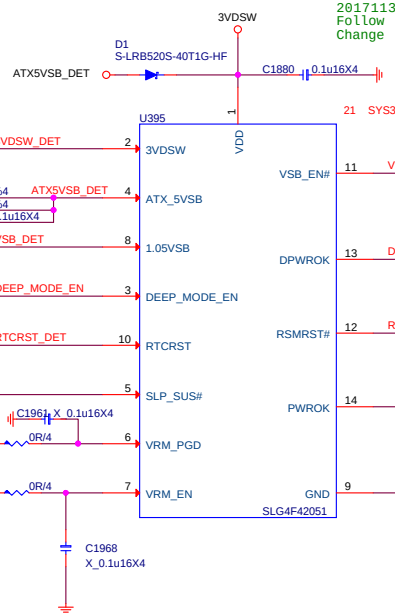
34 ATX5VSB_DET



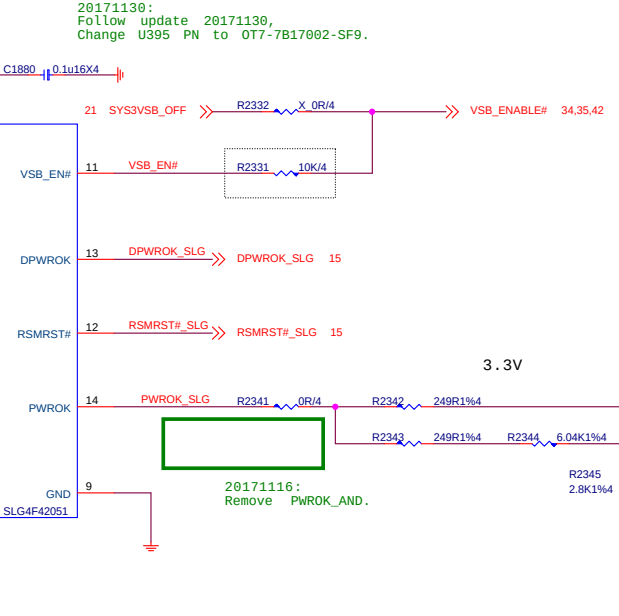
20171220
Q1->D03-7002E89-U47.

20171130:
Follow update 20171130,
SLP_SUS# pull down 100k.





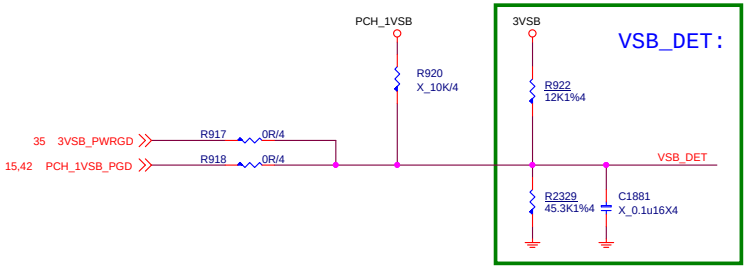
ATX5VSB_DET:
high:2.7v/low:2.55v



3.3V

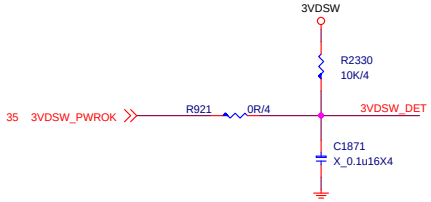
20171130:
Follow update 20171130,
Change U395 PN to OT7-7B17002-SF9.

20171116:
Remove PWROK_AND.



VSB_DET:

20171130:
Follow update 20171130,
R922 -> 12K/ R2329 -> 45.3K



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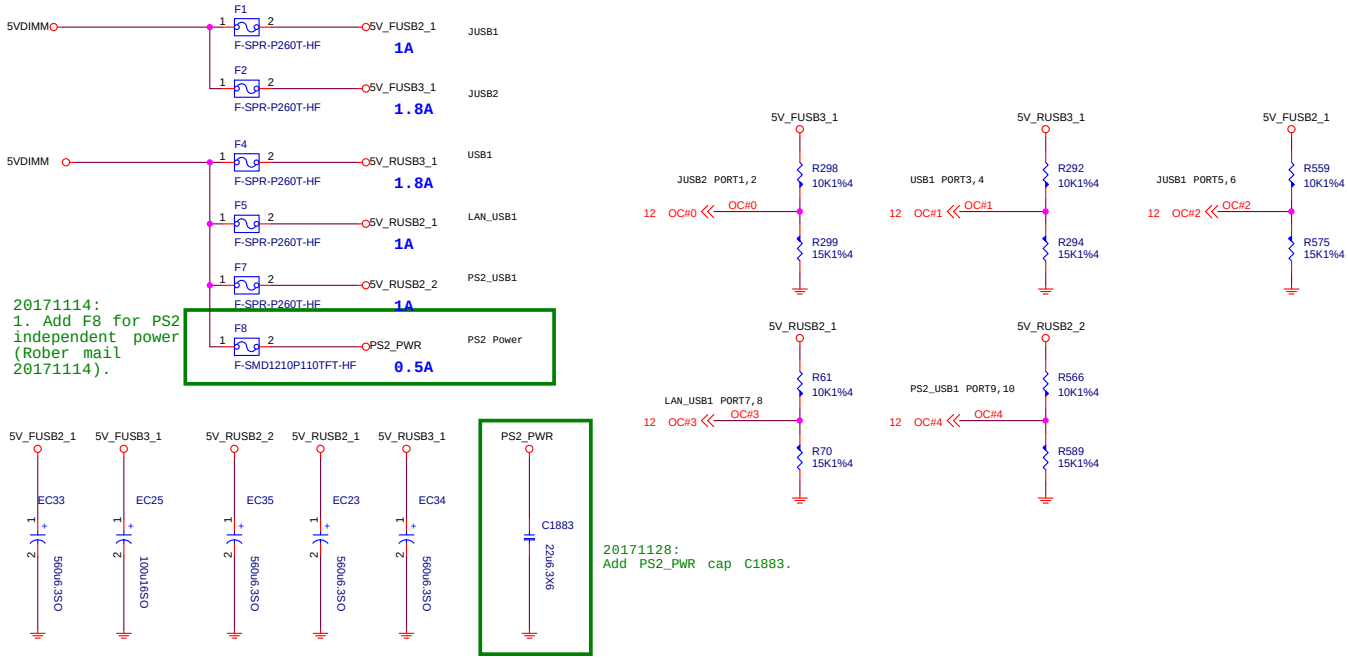
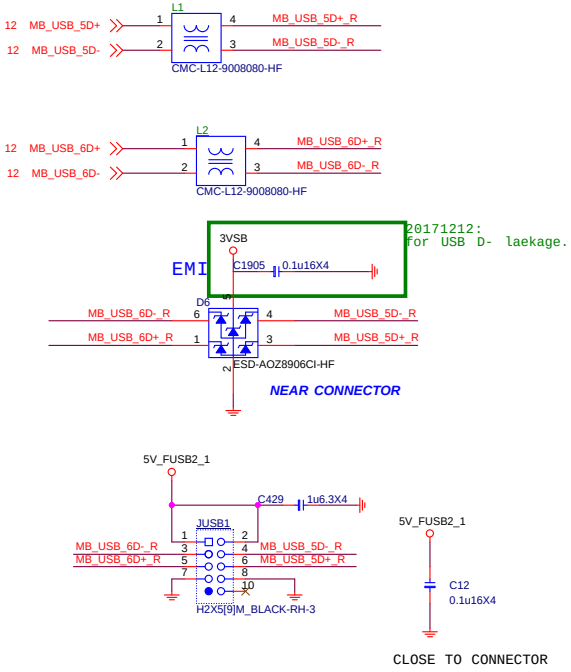
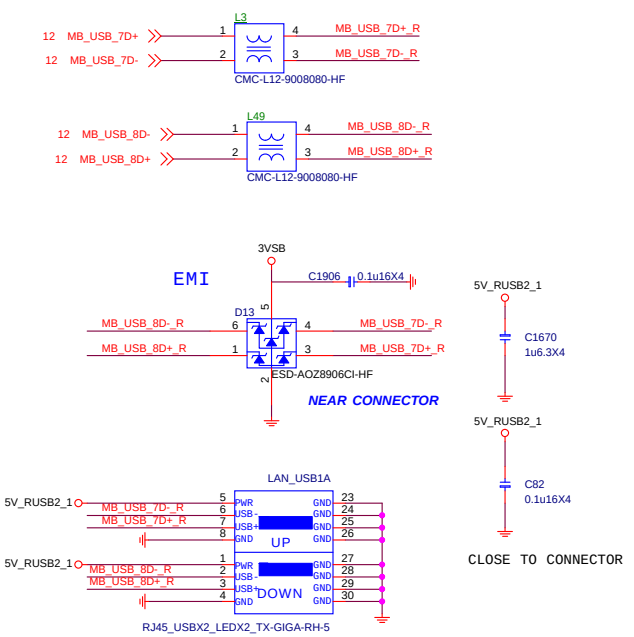


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
JUSB2	5V_FUSB3_1	Port1,2	OC#0
USB1	5V_RUSB3_1	Port3,4	OC#1
JUSB1	5V_FUSB2_1	Port5,6	OC#2
LAN_USB1	5V_RUSB2_1	Port7,14	OC#3
PS2_USB1	5V_RUSB2_2	Port8,9	OC#4

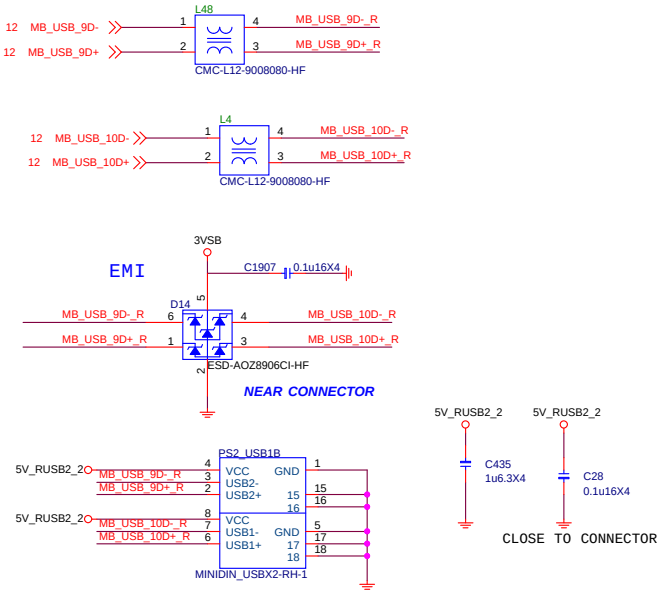
JUSB2 PORT 5,6



LAN_USB1 PORT 7, 8



PS2_USB1 PORT 8, 9



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Custom	USB2.0 Connector	1.1

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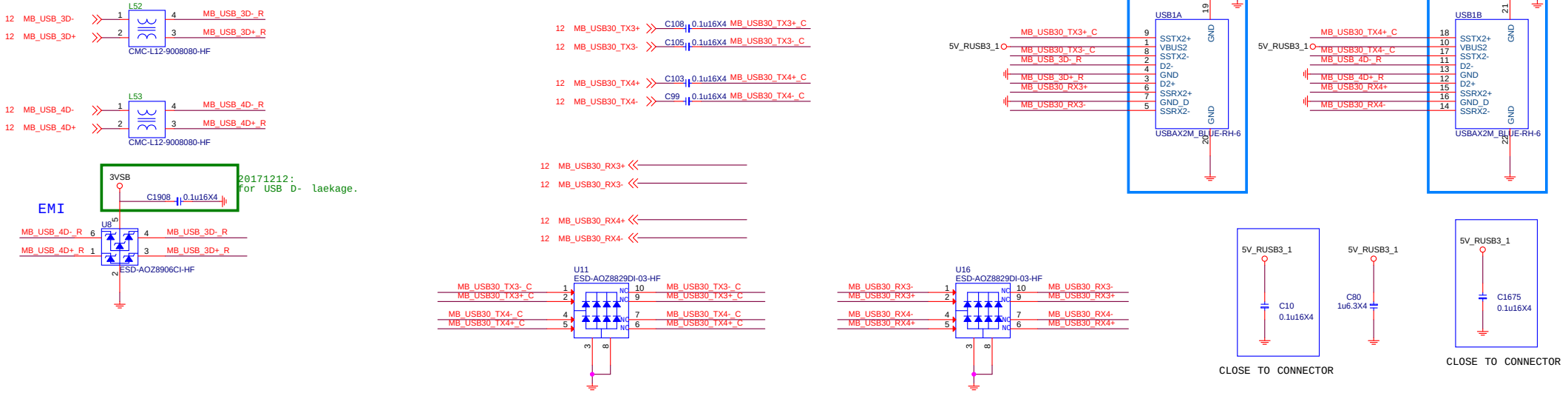
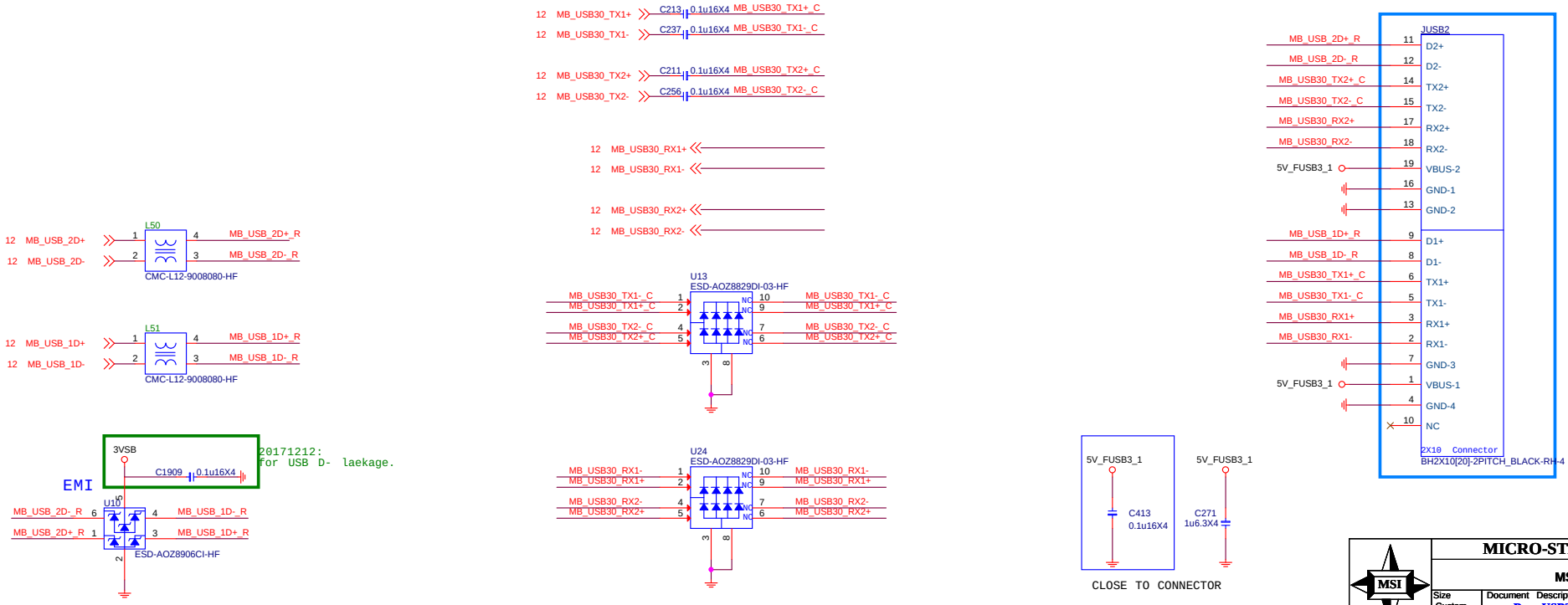
Rear USB1 port 9,10



Front JUSB3 port 1,2



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MS-7C09		
Size: Custom	Document Description: Rear USB3 & Front Connector	Rev: 1.1
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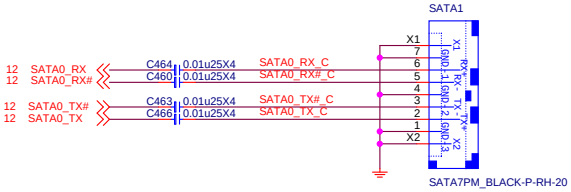

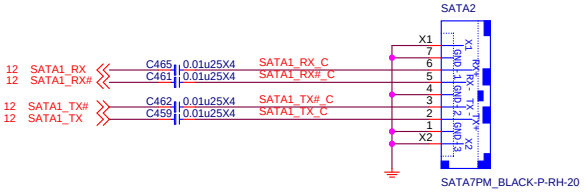

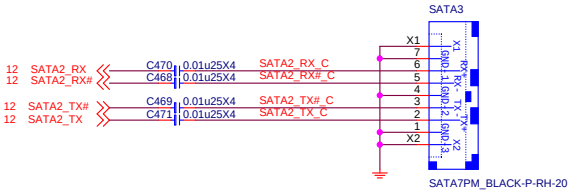

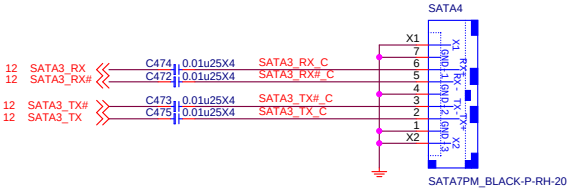

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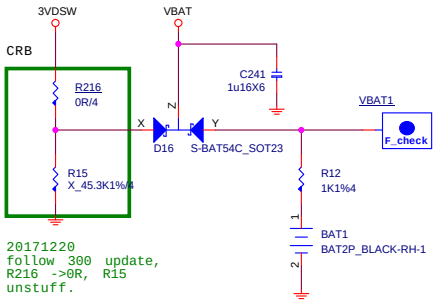
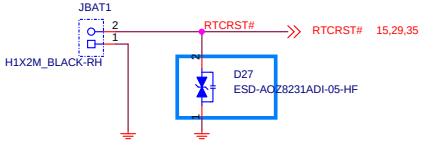
VBAT



20171220
follow 300 update,
R216 ->0R, R15
unstuff.



By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: CUT VBAT circuit	Rev: 1.1
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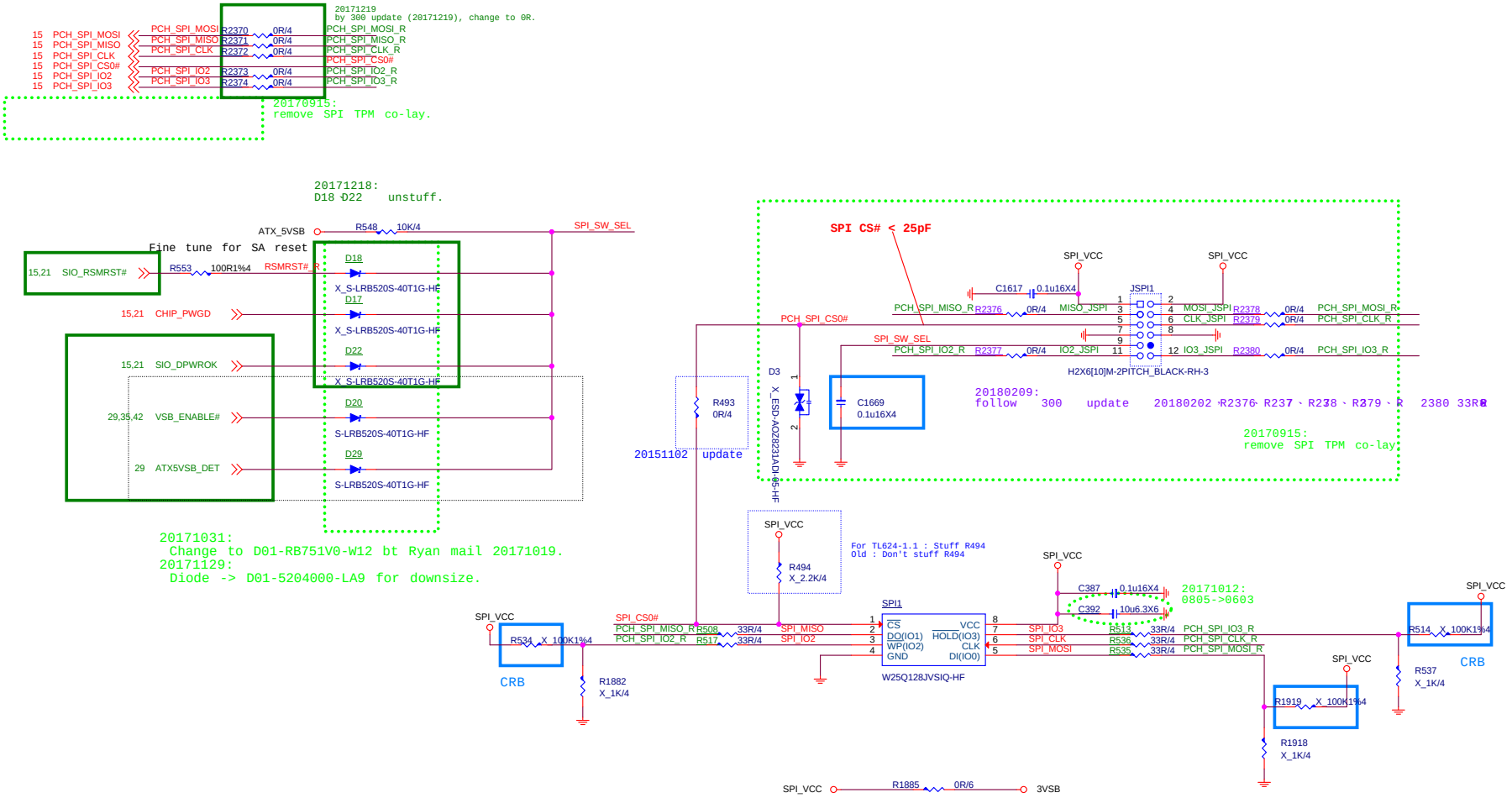

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: BIOS ROM	Rev: 1.1
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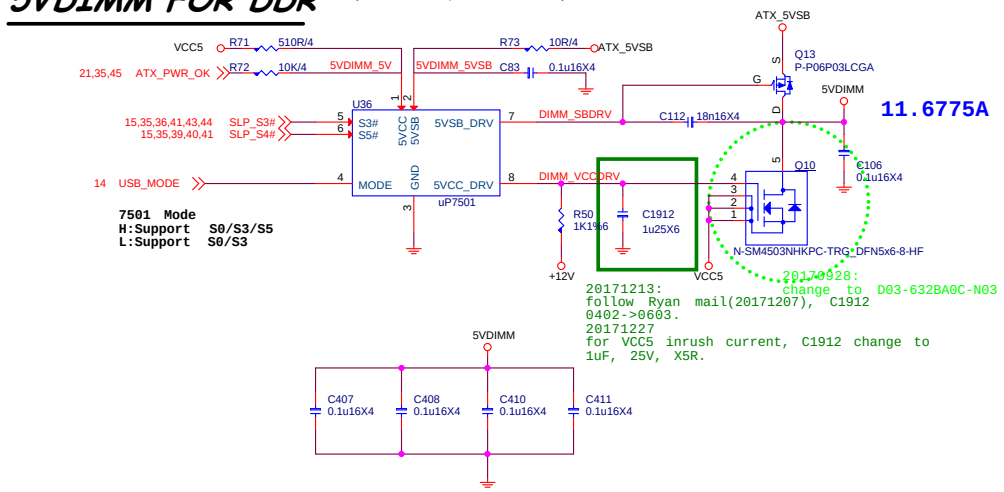
5VDIMM FOR DDR

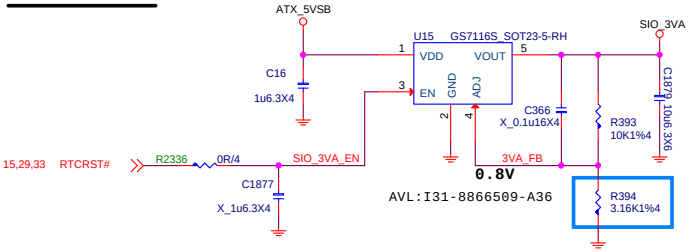
(3A for DDR,6.6A for USB)



SIO_3VA

20mA

3.33V



Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.02
=1.7*0.02
=0.034W

teknisi indonesia

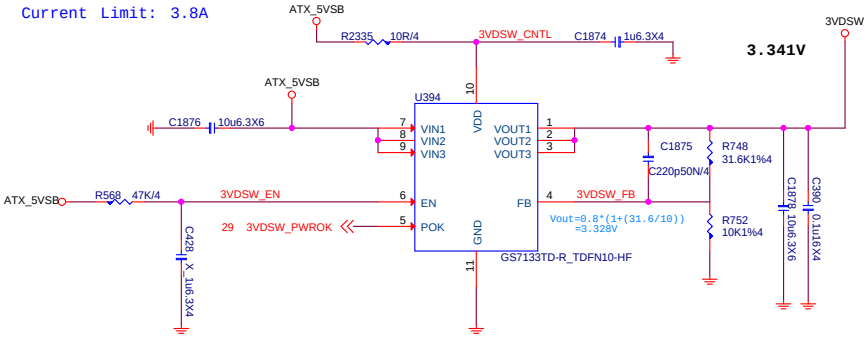
3VDSW

20171123:
1. Remove SIO_DPWROK (Q185) circuit.
2. Change 3VDSW IC to I31-S71330C-N03.

3.3V; 113.6mA

Current Limit: 3.8A

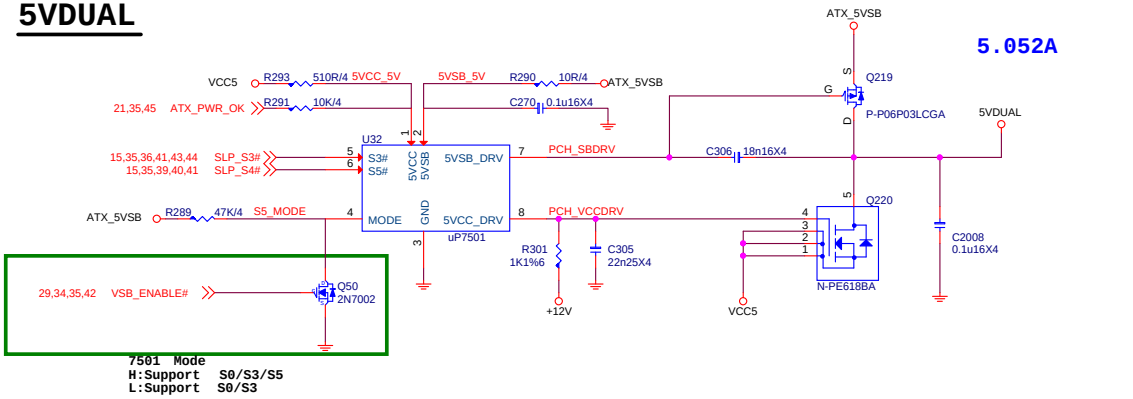
113mA(PCH)+0.6mA(RTC)

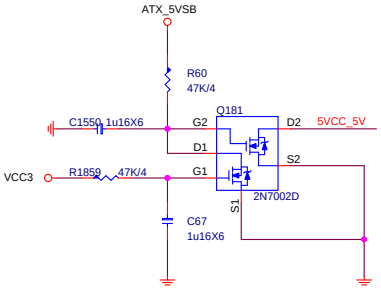


Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.114
=1.7*0.114
=0.194W

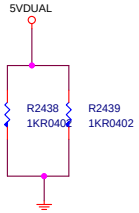
5VDUAL

5.052A



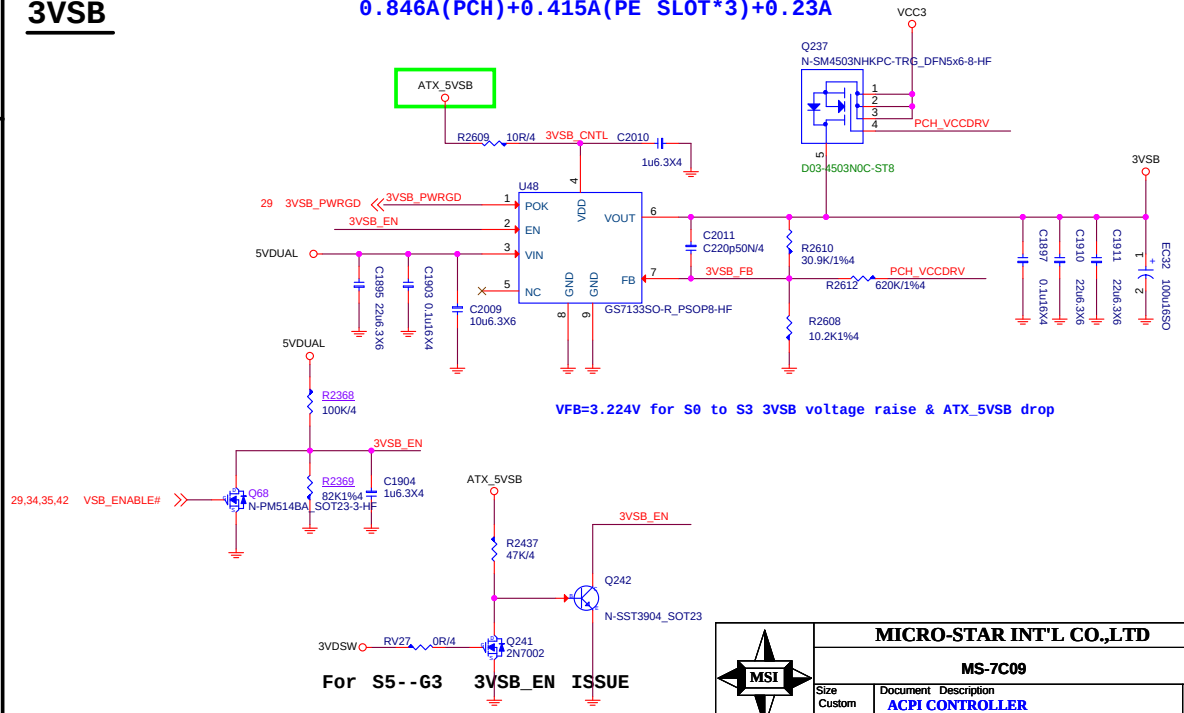


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



3VSB

0.846A(PCH)+0.415A(PE SLOT*3)+0.23A



MICRO-STAR INT'L CO.,LTD

MS-7C09

Size	Document Description	Rev
Custom	ACPI CONTROLLER	1.1

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VCORE Iccmax 138A,TDC 91A, OCP 213A.
VGT Iccmax 45A,TDC 30A, OCP72A.

20171018
follow Xiao mail, R1828 unstuff, VRHOT asserted by SIO.

20171114:
1. R99 18.7K->18KR.

20171114:
1. Power solution R2274 340R->1.18KR.
2. R2272 0603->0402.

VCORE Default VR_HOT 115℃, ALERT 97 ℃

20171018
follow 7B33 Xiao mail (10/18).

VGT ALERT 97℃

20170915:
cancel loadline adjust function.

0LL_EN:
Zero load-line function setting.
Connect to 5V can enable 0LL function.

20170922 Add 0LL function.

VOFS=0.4*(VOFSM-1.7)
-500mV<VOFS<590mV .
Disable offset function,OFSM Pin to GND.

20171114:
power solution:
1. R117 47.5K->57.6KR.
2. R1967 1.82K->162R.
3. R116 17.8K->21KR.
4. R1968 191R->422R.
5. R129 33.2K->69.4KR.
6. R1973 1.2K->1.54KR.
7. R139 3.32K->6.19KR.
8. R1974 118R->0R.

20170927:
R2278 10Kohm for ESD.

Jumper insert,VCORE/VGT 0.8V.

SET1:Iccmax:134A,OCP:160%*Iccmax,DVID 61mV

SETA1:Iccmax:48A,OCP:160%*Iccmax,DVID 39.7mV

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 cintrol ICCMAX,OCP setting
SETA2 control Internal compensation

20171206:
add R2353 to pull low GPP_D16.

R2 Default 11.32K

R1 Default 190.57K

VCORE Thermal Protection Table

GPP_D16	R1	R2	Thermal Alert#	VR_HOT#	Thermal Alert#/VR_HOT#
GPI(0) Default	274.32K	8.55K	97℃	115℃	84.35%
GPI(1)	112.45K	11.32K	106℃	115℃	92.17%

MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: PWM-RT3607BC | Rev: 1.1

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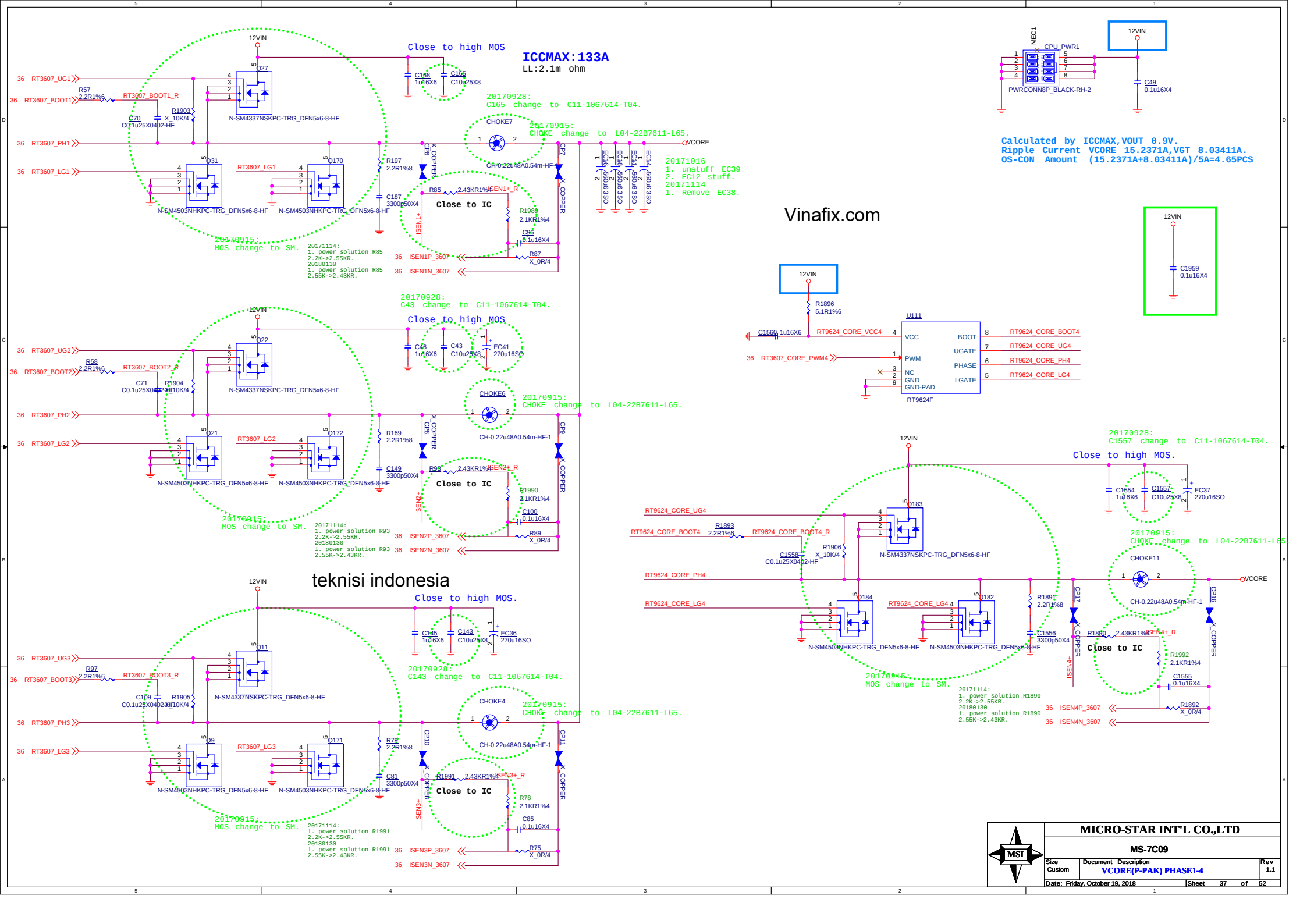
ICCMAX:133A
LL:2.1m ohm
Close to high MOS
Close to IC
20170928:
C165 change to C11-1067614-T04.
20170915:
CHOKE change to L04-22B7611-L65.
20170915:
MOS change to SM.
20171114:
1. power solution R85
2.2K->2.55KR.
20180130
1. power solution R85
2.55K->2.43KR.
20171016
1. unstuff EC39
2. EC12 stuff.
20171114
1. Remove EC38.
Vinafix.com
Calculated by ICCMAX,VOUT 0.9V.
Ripple Current VCORE 15.2371A,VGT 8.03411A.
OS-CON Amount (15.2371A+8.03411A)/5A=4.65PCS
20170928:
C43 change to C11-1067614-T04.
20170915:
CHOKE change to L04-22B7611-L65.
20170915:
MOS change to SM.
20171114:
1. power solution R93
2.2K->2.55KR.
20180130
1. power solution R93
2.55K->2.43KR.
teknisi indonesia
20170928:
C143 change to C11-1067614-T04.
20170915:
CHOKE change to L04-22B7611-L65.
20170915:
MOS change to SM.
20171114:
1. power solution R1991
2.2K->2.55KR.
20180130
1. power solution R1991
2.55K->2.43KR.
20170928:
C1557 change to C11-1067614-T04.
20170915:
CHOKE change to L04-22B7611-L65.
20170915:
MOS change to SM.
20171114:
1. power solution R1890
2.2K->2.55KR.
20180130
1. power solution R1890
2.55K->2.43KR.
MICRO-STAR INT'L CO.,LTD
MS-7C09
VCORE(P-PAK) PHASE1-4
Date: Friday, October 19, 2018
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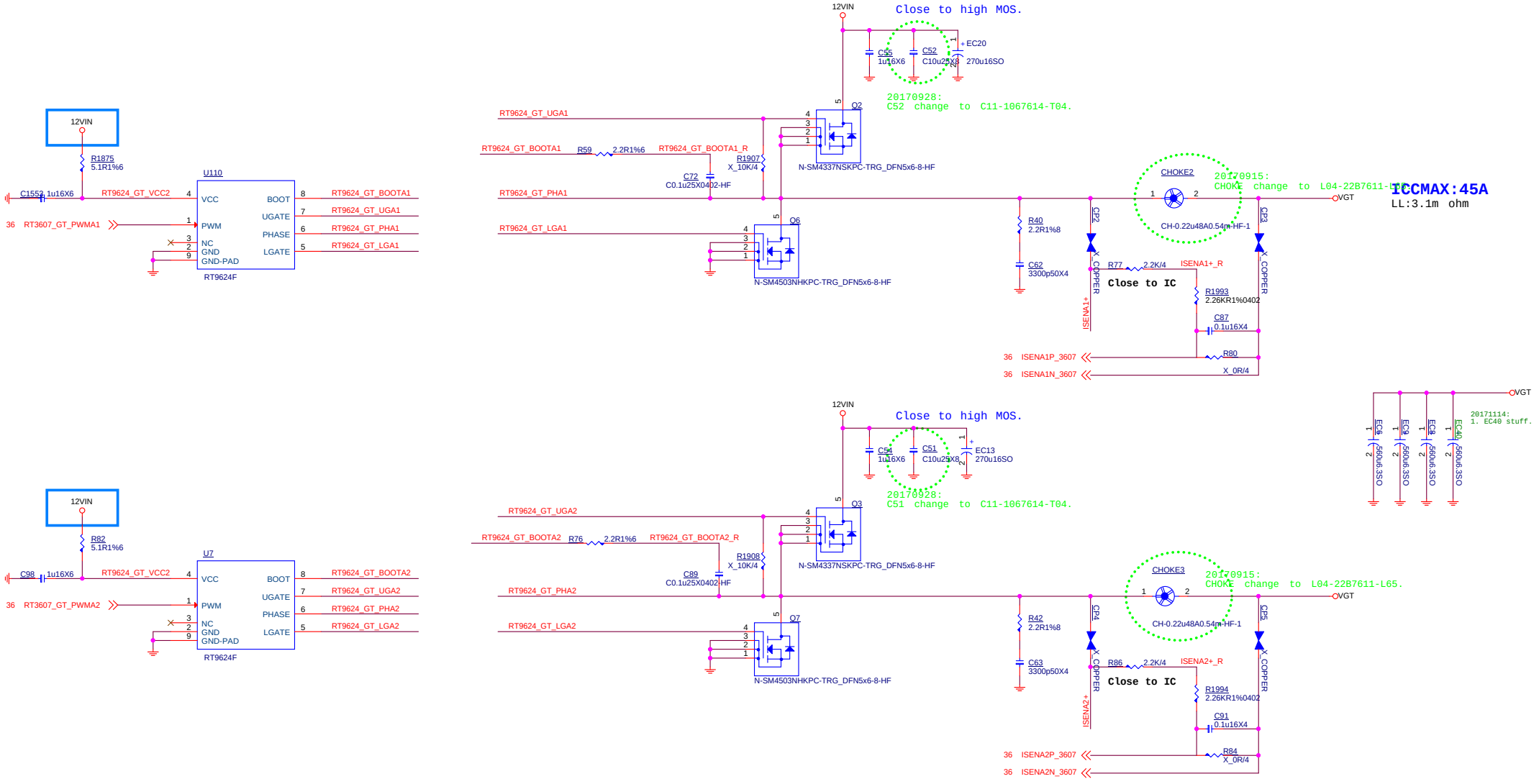

MICRO-STAR INT'L CO.,LTD		
MS-7C09		
Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 1.1
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VCC_DDR

1.2V, 3.3A+ 5.85A+0.375A=9.525A

3.3A FOR CPU
5.85A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

Vgs:5V->Rds(on):5.1mOhm
*Ilimit=(Rlimit/Rds(on))*5uA/10*
*=(140Kohm/5.1mohm)*5uA/10*
=13.73A

*0.4V<=Rlimit *5uA<=3V*

Vgs:5V->Rds(on):3.9mOhm
*Ilimit=(Rlimit/Rds(on))*5uA/10*
*=(140Kohm/3.9mohm)*5uA/10*
=17.95A

Iin=9.525A*1.2V/0.8/5V=2.8575A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A.

VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=9.525 * 0.427
= 4.06797A

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f:426.57KHz

Current Limit 2.6A

FB:0.75V

MAX:9.525A

1.2V

SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down

MS-7981 Add. Package C-states above C8 function

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

0.1uFx1 per dimm

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MS-7C09	
Size: Custom	Document Description: DDR-RT8231
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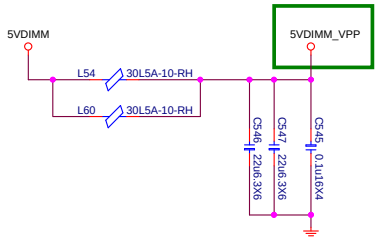
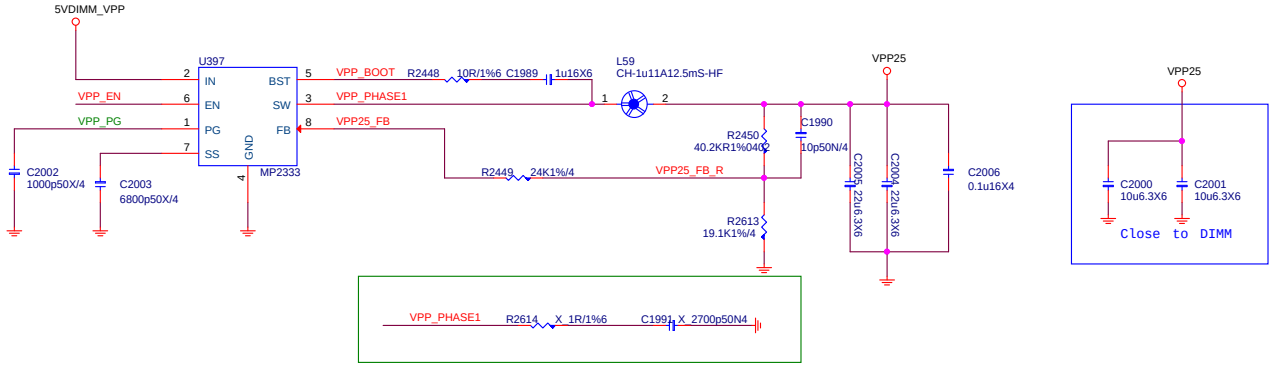
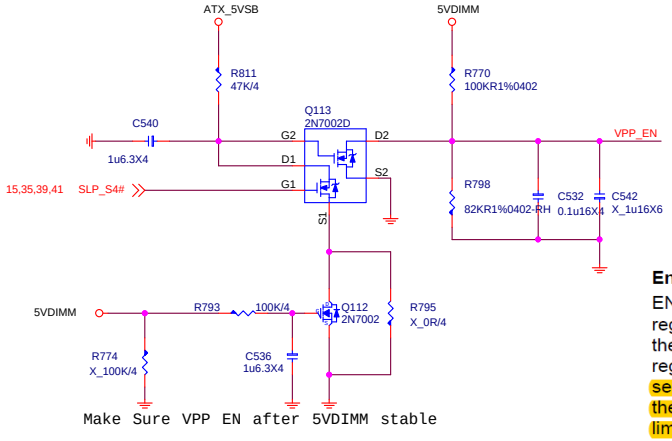
2DIMM :1.12A FOR DDR VPP2.5V

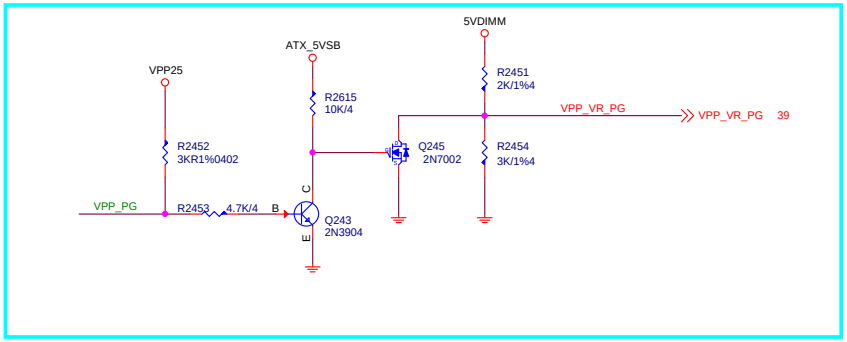
VPP25 Power
2.5V; 2A







ENABLE HIGH:1.16~1.29V



Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14µA.

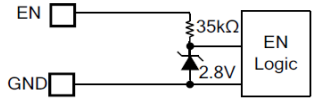


Figure 2: Zener Diode between EN and GND

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	MS-7C09	
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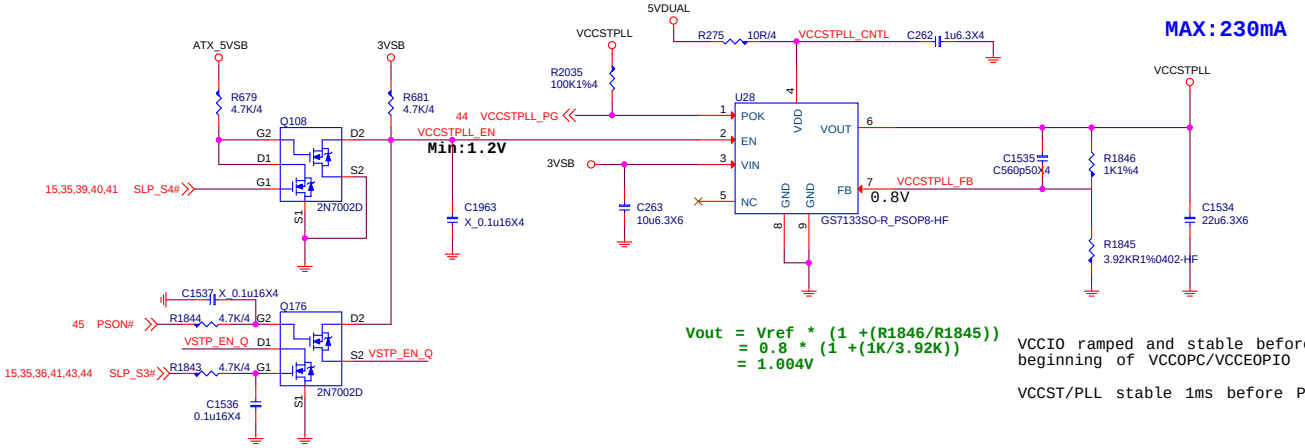
VCCSTPLL

1.0V; 230mA



MAX:230mA

Power Loss=(Vin-Vou)*Iout
=(3.3-1.0)*0.23
=2.3*0.23
=0.529W

Vout = Vref * (1 +(R1846/R1845))
= 0.8 * (1 +(1K/3.92K))
= 1.004V

VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

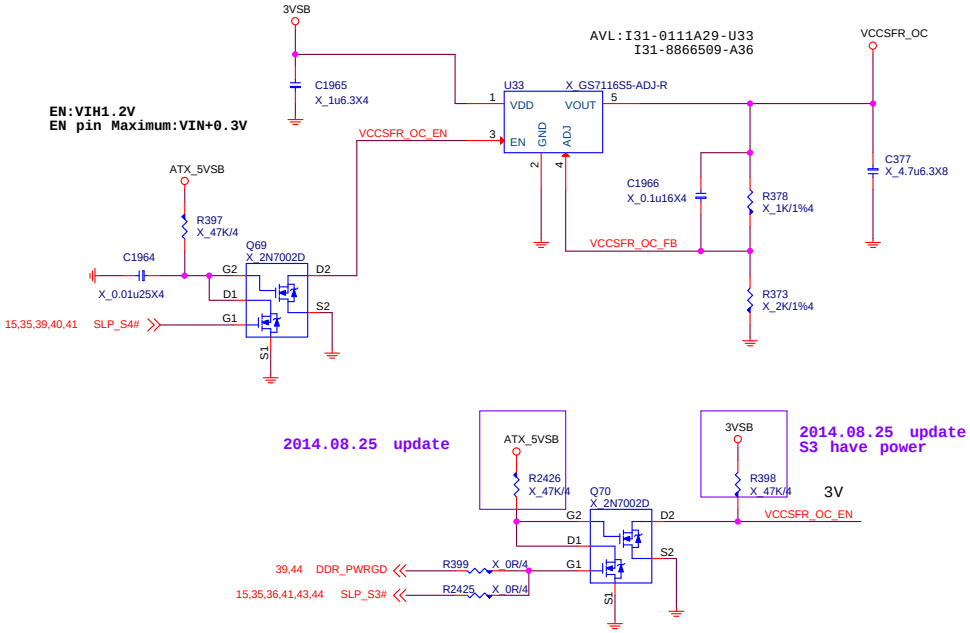
VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

2014.08.21 update

1.2V; 130mA

Power Loss=(Vin-Vou)*Iout
=(3.3-1.2)*0.13
=2.1*0.13
=0.273W



2014.08.25 update

2014.08.25 update
S3 have power

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MS-7C09		
Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 1.1
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PCH_1VSB

1.05V; 10.285A

Rocpset:5.6K
OCP(min)=Rocset*Iocset/Rdson(Low side)
=6.2K*10uA/5.1mohm
=12.16A

OCP(max)=Rocset*Iocset/Rdson(Low side)
=6.2K*10uA/3.9mohm
=15.90A

Rdson(low)5V
D03-4503N0C-ST8
Max:5.1mohm Min:3.9mohm

Irms =Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=16.685*0.407
=6.79A

Iin=10.285A*1.05V/0.8/5V=2.7A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A.

20170921:
input bead 3顆>2顆 .

20180209:
R407 806R->750R, for OV level.

POR:4.2V
EN:2.4V

5VDUAL
R403 10R/8
C362 1u16X6
U34
PCH_1VSB_EN
PCH_1VSB_PGD
PCH_REFOUT
PCH_REFIN
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
RT8125EGQW_WDFN10-HF
PCH_BOOT
PCH_PHASE
PCH_UGATE
PCH_LGATE
R1996 0R/6
PCH_BOOT_R
C349 0.1u16X4
15,29 PCH_1VSB_PGD
C364 1000p50X4
R407 806R1%0402-RH
C365 1000p50X4
CP13
X_COPPER
R374 6.2K1%4
20171116
R374: 7.15K->6.2KR
for OCP
PCH_CORE_FB_R
R1909 X_10K/4
Q57
Q56
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
R330 2.2R/8
C328 2200p50X4
CHOKE10
CH-0.82u18A4.6mS-HF
20170918 change
L04-82B7090-M26
by Ivy mail.
5VDUAL_PCH_IN
C333 0.1u16X4
C314 10u6.3X6
C1607 22u6.3X6
C1605 1u6.3X4
L5 30L5A-10-RH
L11 30L5A-10-RH
EC26 560u6.3SO
C307 1K/4
C1606 0.1u16X4
5VDUAL
PCH_1VSB
EC31 560u6.3SO
EC30 560u6.3SO
C369 22u6.3X6
C371 10u6.3X6
C368 10u6.3X6
C360 1u6.3X4
MAX:10.285A

20180209:
follow 300 update
20180209 C307 stuff
1KR for dummy load.

39 PCH_CORE_OV
PCH_CORE_OV

to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

C376 X_0.01u25X4
PCH_TYPE3
R437 X_0R/4
R441 1K1%4
PCH_MPHY_SENSE_R
R439 3.92KR1%0402-HF

PCH_1VSB
R2002 0R/4
20171019
R2002: unify 1%->5%
20180130
PCH1P05_FB change to local sense
R2002->0R R2001 unstuff.

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5376uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 1.0V

5VDUAL
20171003
300 Series update
R1027 47K/4
PCH_1VSB_EN
C372 X_0.1u16X4
ATX_5VSB
R408 47K/4
Q58 2N7002
C788 X_0.1u16X4
3VSB
R446 10K/4
Q106 2N3904
R1031 X_2.21K1%4
29,34,35 VSB_ENABLE#
Q216 2N7002

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MICRO-STAR INT'L CO.,LTD
MS-7C09
Size: Custom
Document Description: PCH Core power
Rev: 1.1
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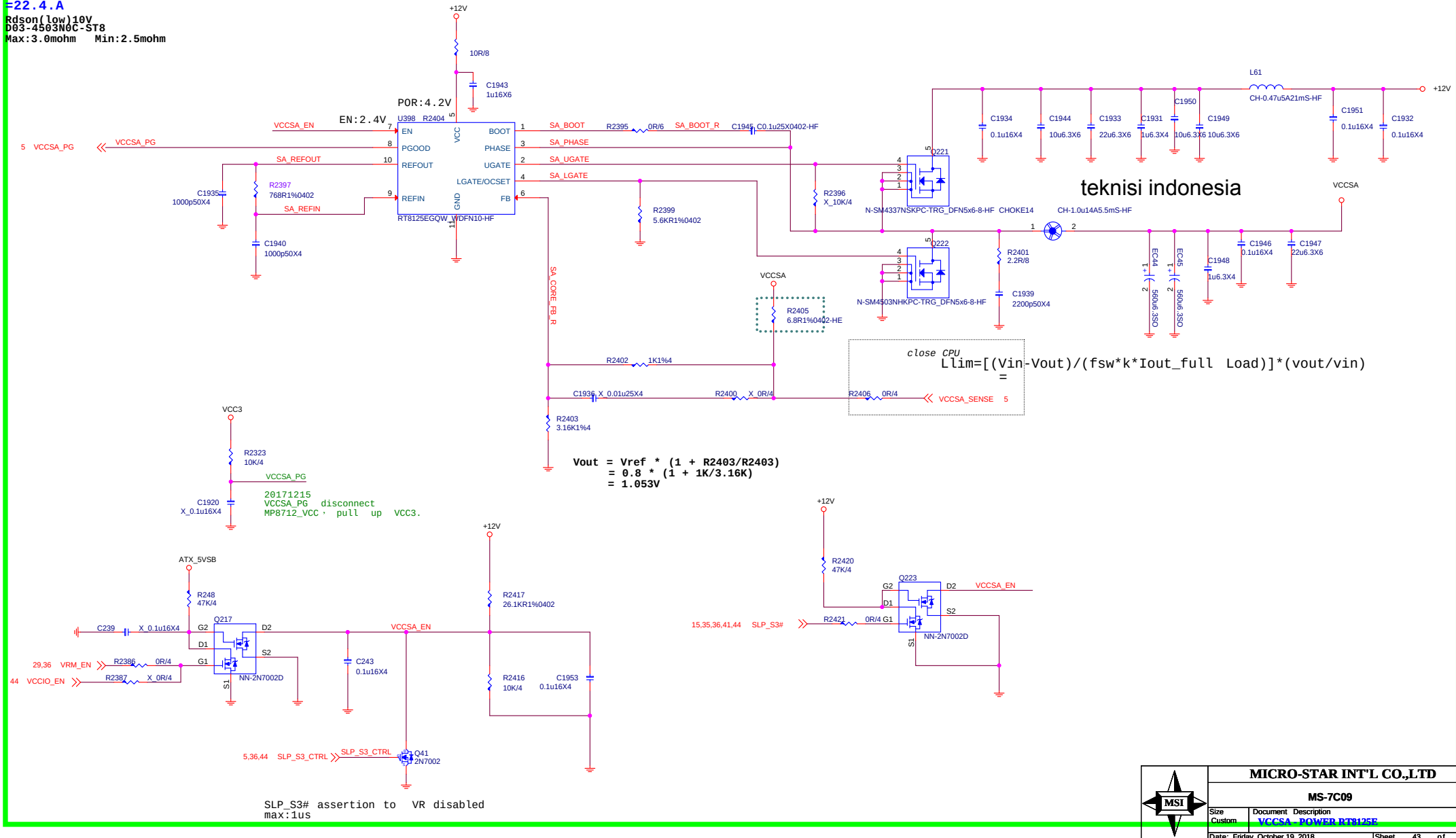
SA Power:1.05V,11.1A

Irms = Iout/N * SQRT[ND*(1-DN)]
=12.3 *SQRT[0.0875*0.9125]
= 3.47A <5000ma

Rocpset:5.6K
OCP(min)=Rocset*Iocset/Rdson(Low side)
=5.6K*10uA/3.0mohm
=18.67A

OCP(max)=Rocset*Iocset/Rdson(Low side)
=5.6K*10uA/2.5mohm
=22.4.A

Rdson(low)10V
D03-4503N0C-ST8
Max:3.0mohm Min:2.5mohm



MICRO-STAR INT'L CO.,LTD	
MS-7C09	
Size: Custom	Document Description: VCCSA - POWER RT8125E
Rev: 1.1	
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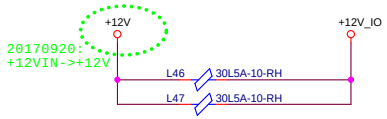
VCCIO

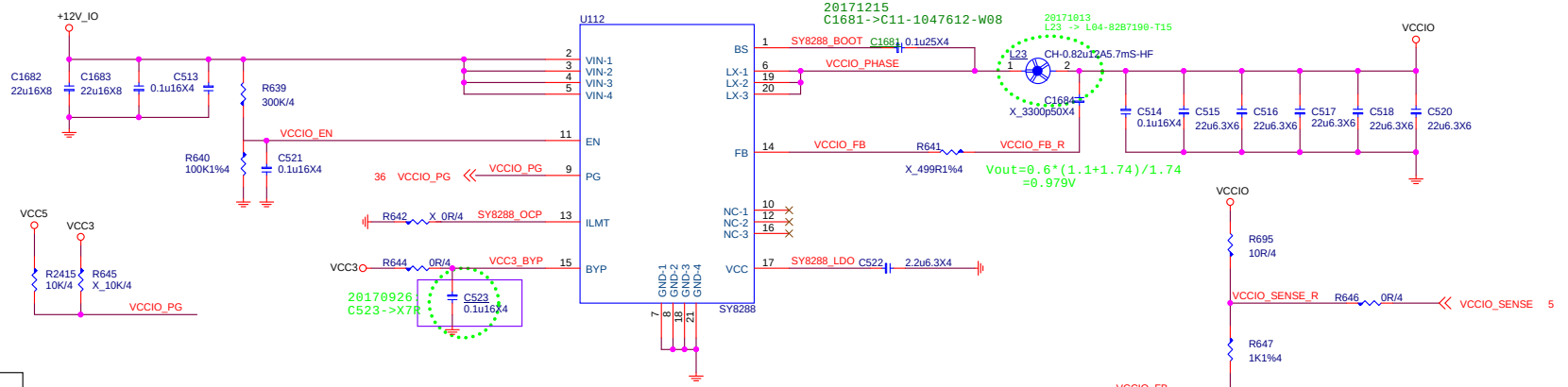
0.95V; 6.4A

OCP: 12A (floating)

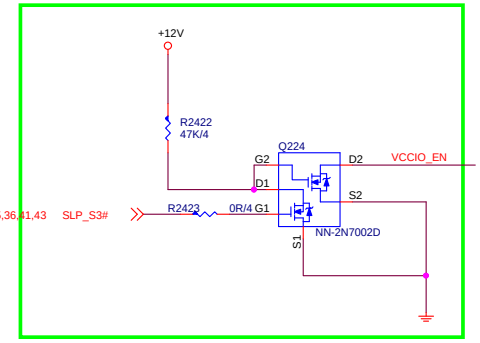
20170919
TPS22976 -> SY8288 by Ivy mail (20170918).

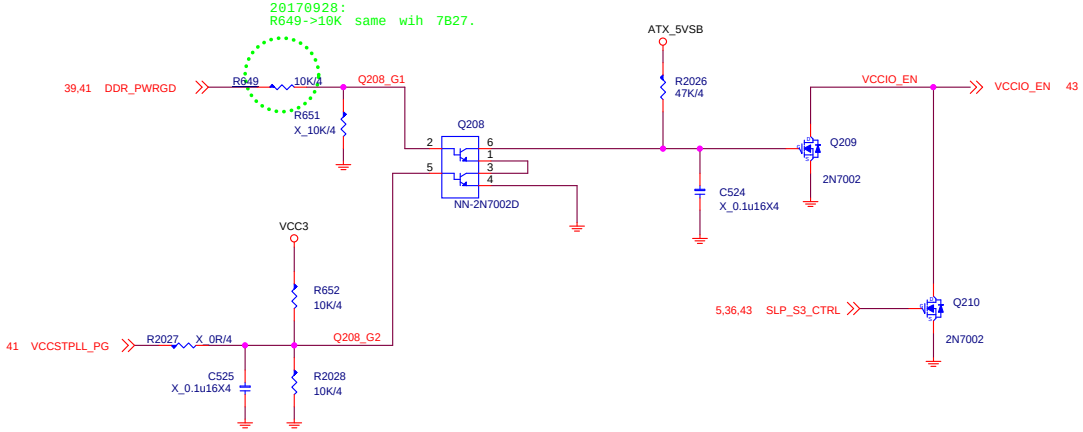


Iin=6.4A*0.95V/0.8/12V=0.63A
L02-3008043-M26
Over 85℃ ,Rated Current 1.5A.



SY8288_pin13	OCP
0	8A
floating	12A
1	16A





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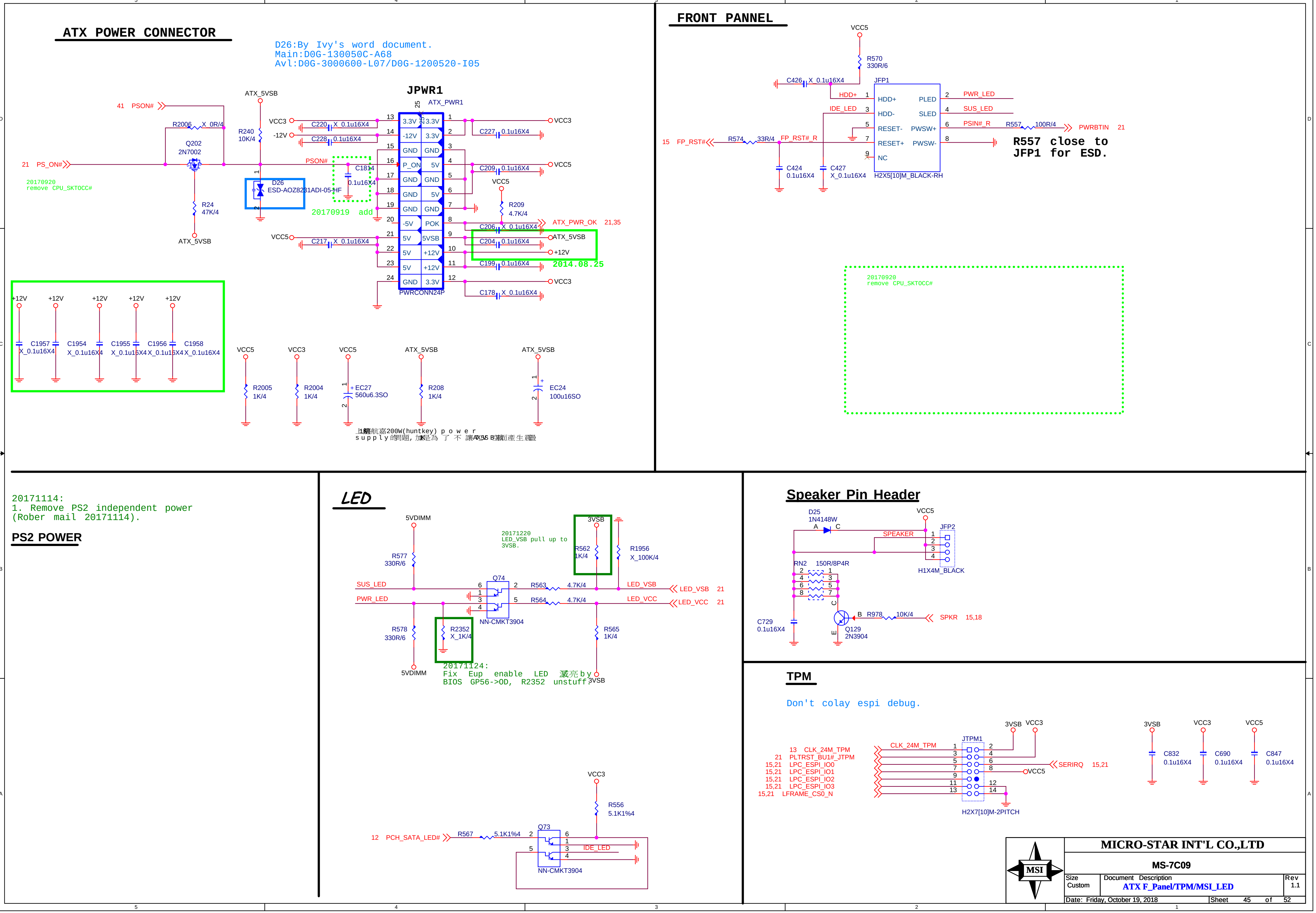

ATX POWER CONNECTOR
D26:By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05
JPWR1
ATX_PWR1
PWRCONN24P
PSON#
PS_ON#
Q202
2N7002
R2006 X_0R/4
R240 10K/4
R24 47K/4
D26 ESD-AOZ8231ADI-05-HF
C1814 0.1u16X4
20170919 add
20170920 remove CPU_SKTOCC#
ATX_5VSB
VCC3
VCC5
-12V
+12V
ATX_PWR_OK 21,35
R209 4.7K/4
2014.08.25
C1957 X_0.1u16X4
C1954 X_0.1u16X4
C1955 X_0.1u16X4
C1956 X_0.1u16X4
C1958 X_0.1u16X4
R2005 1K/4
R2004 1K/4
EC27 560u6.3SO
R208 1K/4
EC24 100u16SO
FRONT PANNEL
R570 330R/6
C426 X_0.1u16X4
JFP1
HDD+
HDD-
RESET-
RESET+
NC
PLED
SLED
PWSW+
PWSW-
PWR_LED
SUS_LED
PSIN#_R
R557 100R/4
PWRBTIN 21
IDE_LED
15 FP_RST#
R574 33R/4
FP_RST#_R
C424 0.1u16X4
C427 X_0.1u16X4
H2X5[10]M_BLACK-RH
R557 close to JFP1 for ESD.
20170920 remove CPU_SKTOCC#
20171114:
1. Remove PS2 independent power (Rober mail 20171114).
PS2 POWER
LED
5VDIMM
R577 330R/6
R578 330R/6
SUS_LED
PWR_LED
Q74
NN-CMKT3904
R563 4.7K/4
R564 4.7K/4
3VSB
R562 1K/4
R1956 X_100K/4
20171220 LED_VSB pull up to 3VSB.
LED_VSB 21
LED_VCC 21
R2352 X_1K/4
R565 1K/4
20171124: Fix Eup enable LED 滅亮 by BIOS GP56->OD, R2352 unstuff
R556 5.1K1%4
12 PCH_SATA_LED#
R567 5.1K1%4
Q73
NN-CMKT3904
Speaker Pin Header
D25 1N4148W
SPEAKER
JFP2
H1X4M_BLACK
RN2 150R/8P4R
C729 0.1u16X4
R978 10K/4
SPKR 15,18
Q129 2N3904
TPM
Don't colay espi debug.
JTPM1
H2X7[10]M-2PITCH
13 CLK_24M_TPM
21 PLTRST_BU1#_JTPM
15,21 LPC_ESPI_IO0
15,21 LPC_ESPI_IO1
15,21 LPC_ESPI_IO2
15,21 LPC_ESPI_IO3
15,21 LFRAME_CS0_N
SERIRQ 15,21
C832 0.1u16X4
C690 0.1u16X4
C847 0.1u16X4
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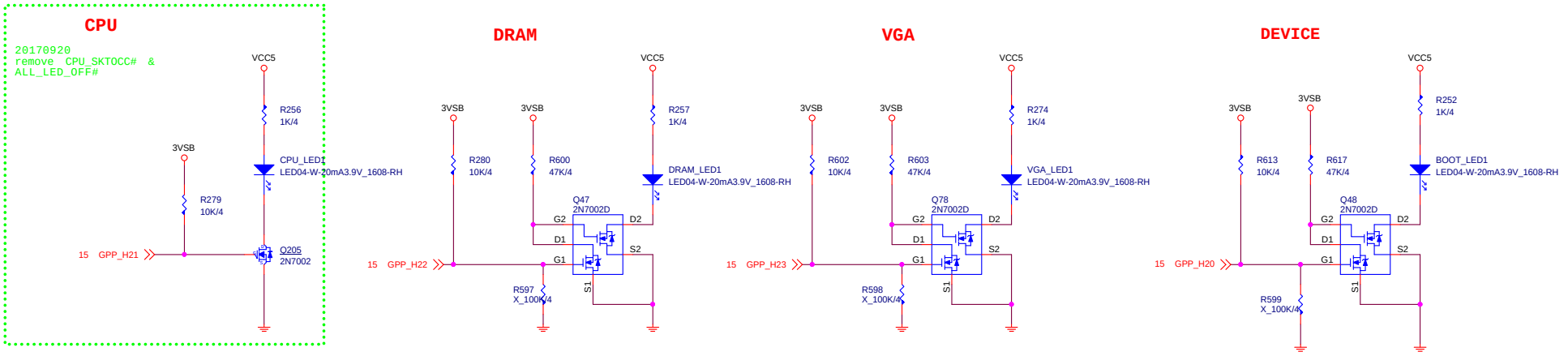
DEBUG LED



LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

關 機 斷 電 狀 態下 ， 3個LED先 維 持 d e f a 亮暗開 機 電後
1. 首 先 進行 CPU check CPU L E D 亮， check PASS 後則 C P U LED滅掉
2. 接 著 依 序進行M emory /m emor y LED亮 chec k PASS後 則me m o r y 開 機。
3. VGA的 check/VGA LED 亮 ，che ck PA S S後則 VGA L E D 滅掉 。
4. 因 此 最 後 正 常 順 利開 機 後 ， 三 個 L E D燈 都 是 滅 掉 的 。(系 統 重 啟 或其他原因造成系統重開機，則LED仍按上述行為動作)

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EMI CAP

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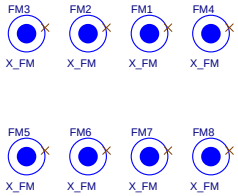
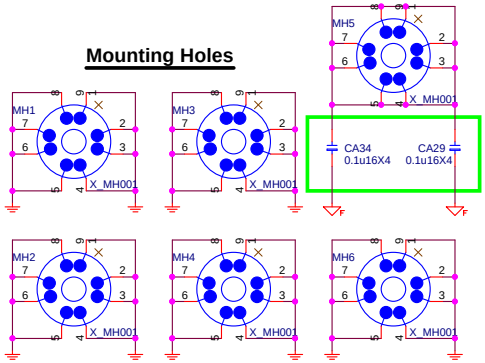
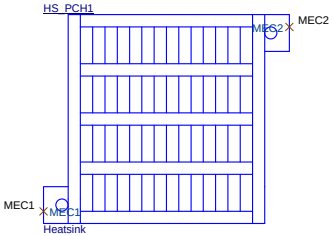
Optical Fiducial Marks-120

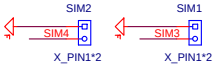


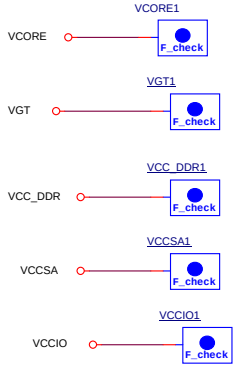
Mounting Holes





Simulation





G51-M1SPN22-Q13

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