MS-7C08

ATX:230mm*185mm

VRE:1.2

Intel -CoffeeLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *4Phase*

*GT POWER PAK *2 Phase*

System Chipset:

H310C

Onboard Chip:

SIO: NUVOTON 5567
HD Audio Codec: ALC887
LAN: INTEL I219V
Flash ROM: SPI 64 MB

PWM:

VCORE - RT3607	*138A*
VGT- RT3607	*45A*
DDR - RT8231	*11.525A*
DDR VPP25- MP2333	*1.12A*
PCH(1.0V) - RT8125E	*10.743A*
VCCSA - RT8125E	*11.1A*
VCCIO - SY8288	*6.4A*

Main Memory:

*DDR4 * 2 (Dual Channel)*

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:MP2147

3VDSW:GS7133

VCCSTPLL:GS7133

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

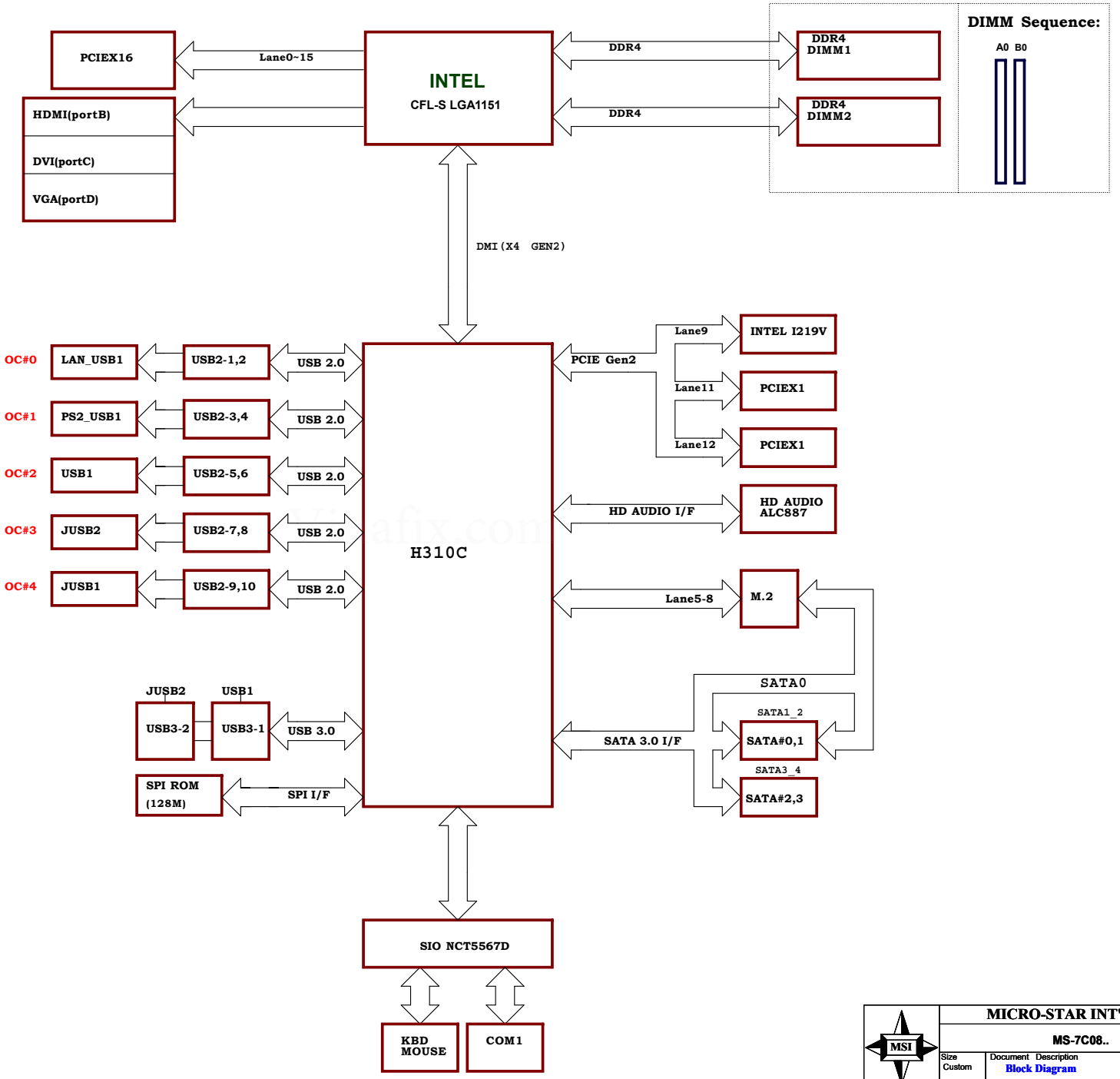
MICRO-STAR INT'L CO.,LTD

MS-7C08..

Size: Custom | Document Description: Cover Sheet | Rev: 1.2

Date: Wednesday, December 12, 2018 | Sheet 1 of 60

Block Diagram



Slot Sequence:

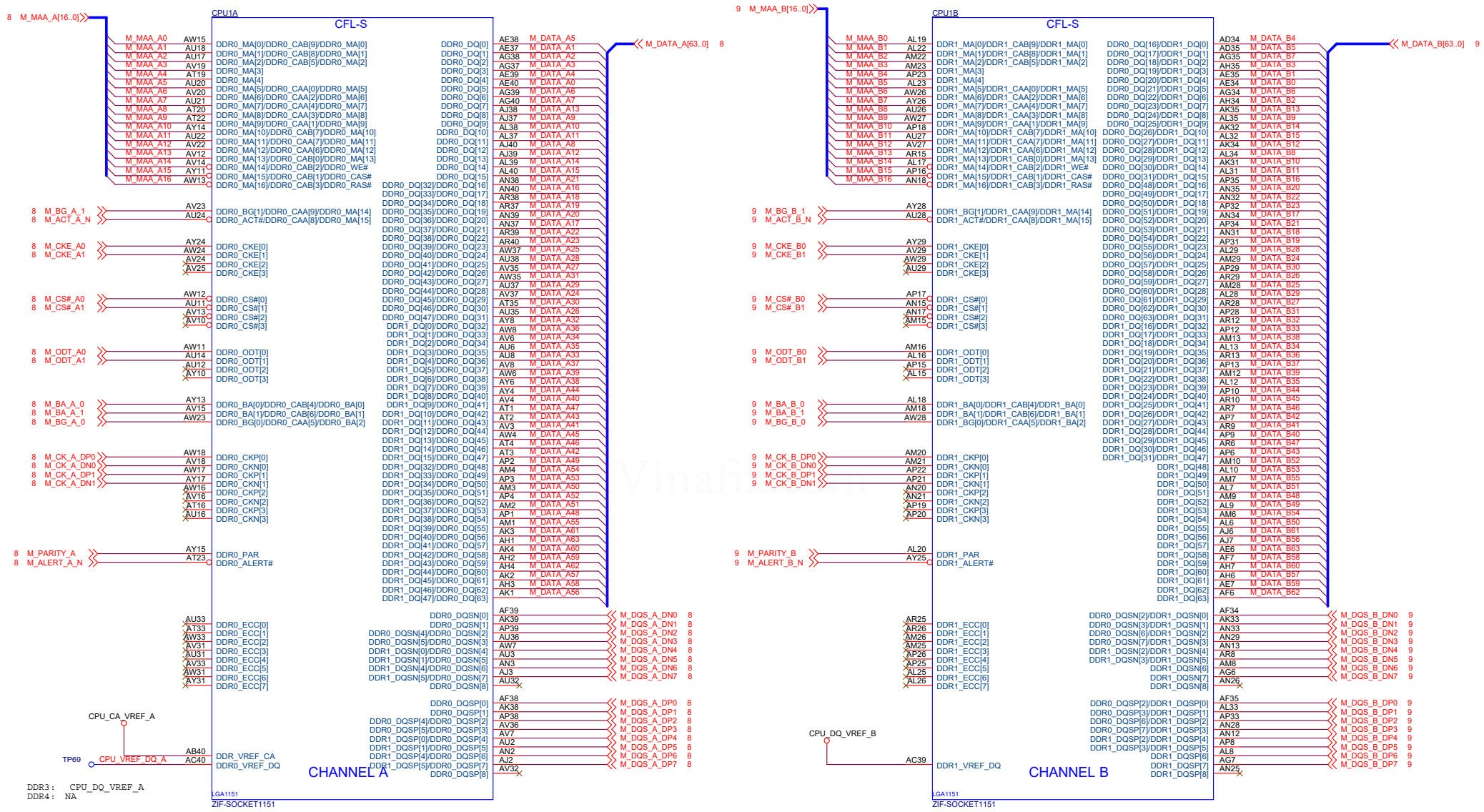
M2_1 (By PCH GEN2)

PCIE X16 (By CPU GEN3)

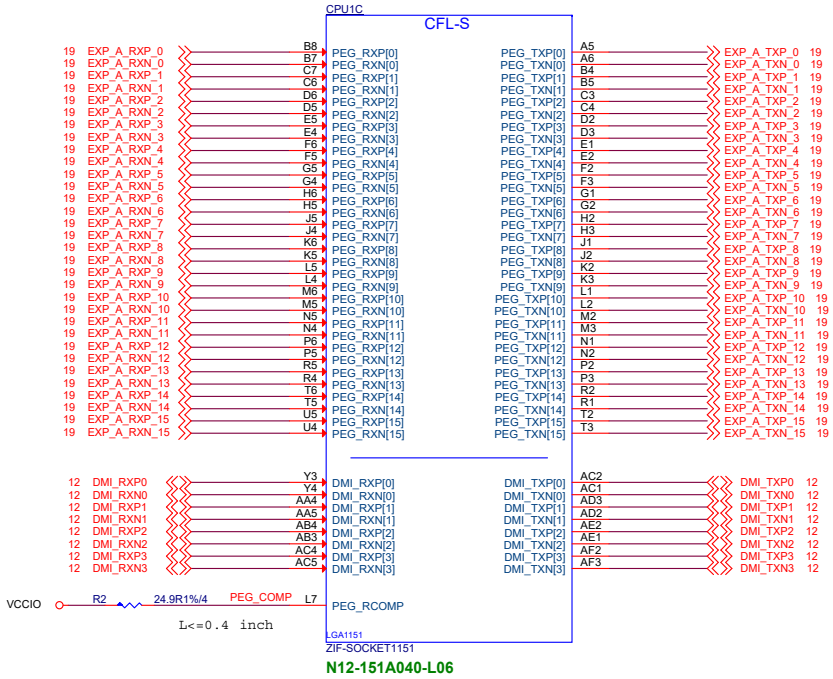
PCIE X1 (By PCH GEN2)

PCIE X1 (By PCH GEN2)

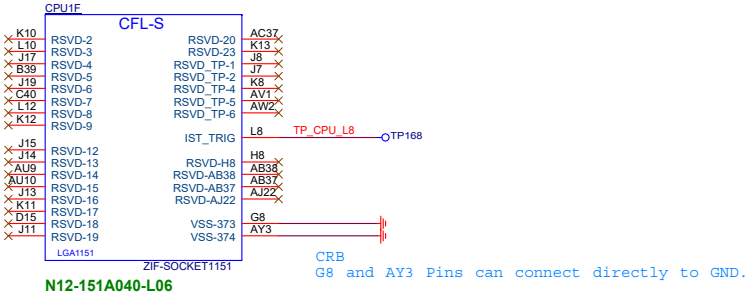
MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: Block Diagram	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 2 of 60	



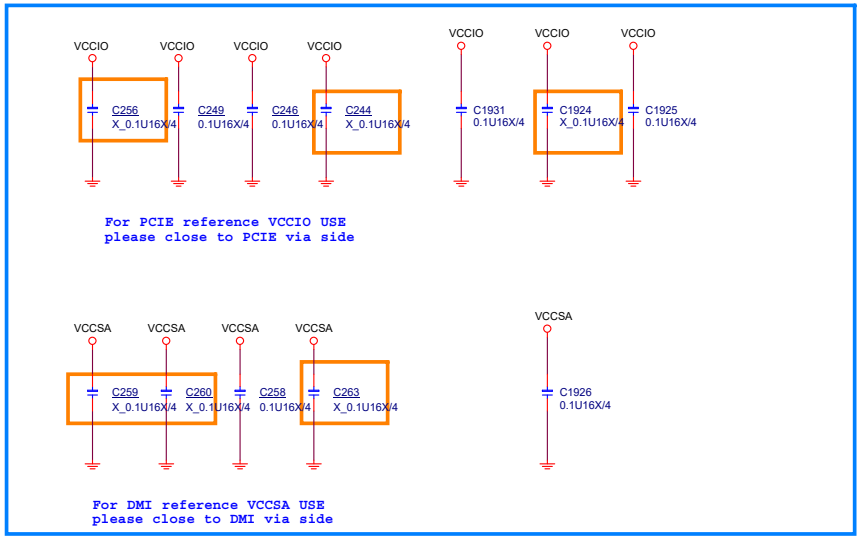
Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7C08..
Size	Custom
Document Description	CPU-Memory
Rev	1.2
Date	Wednesday, December 12, 2018
Sheet	3 of 60

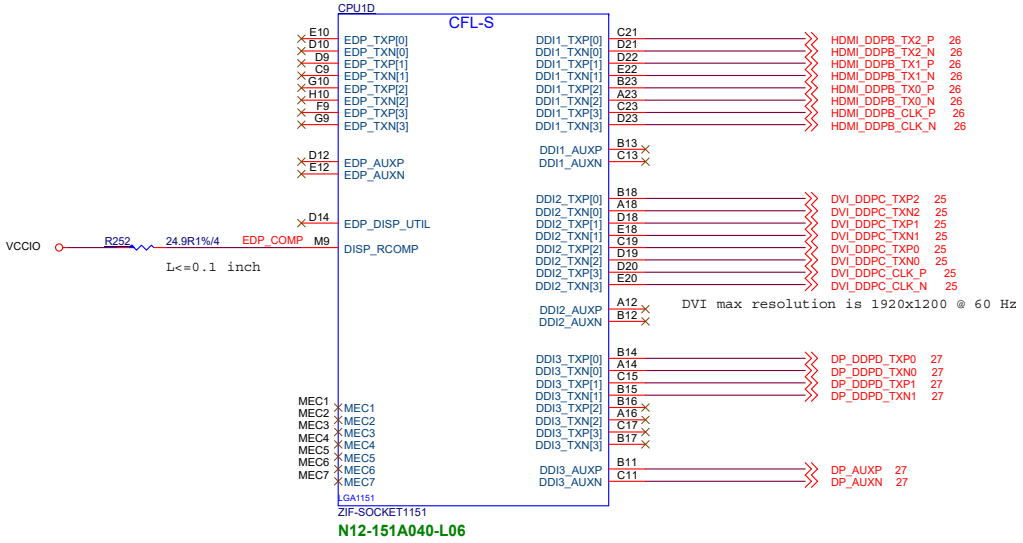


N12-151A040-L06



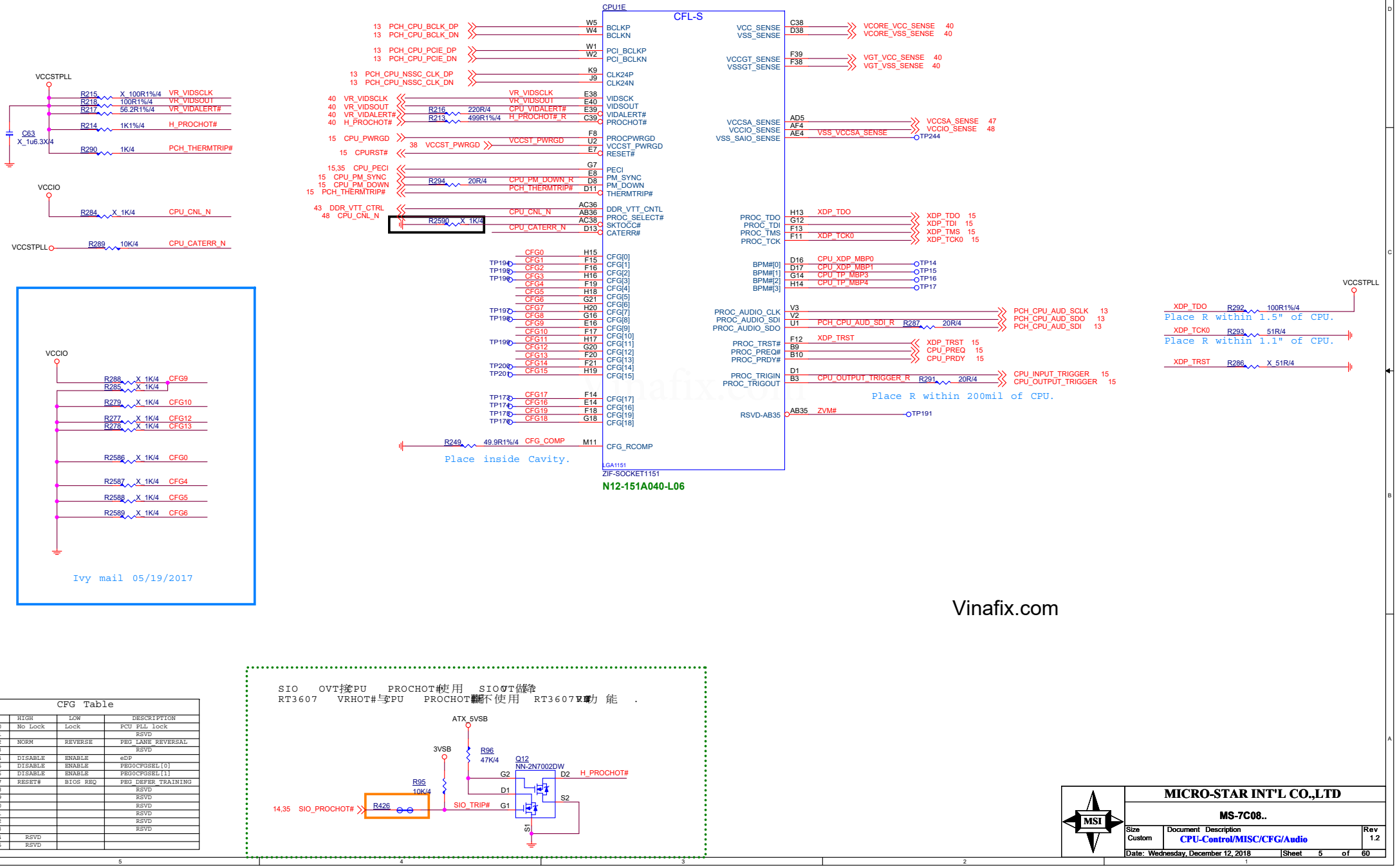
N12-151A040-L06





N12-151A040-L06

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: CPU-PEG/Display	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 4 of 60	

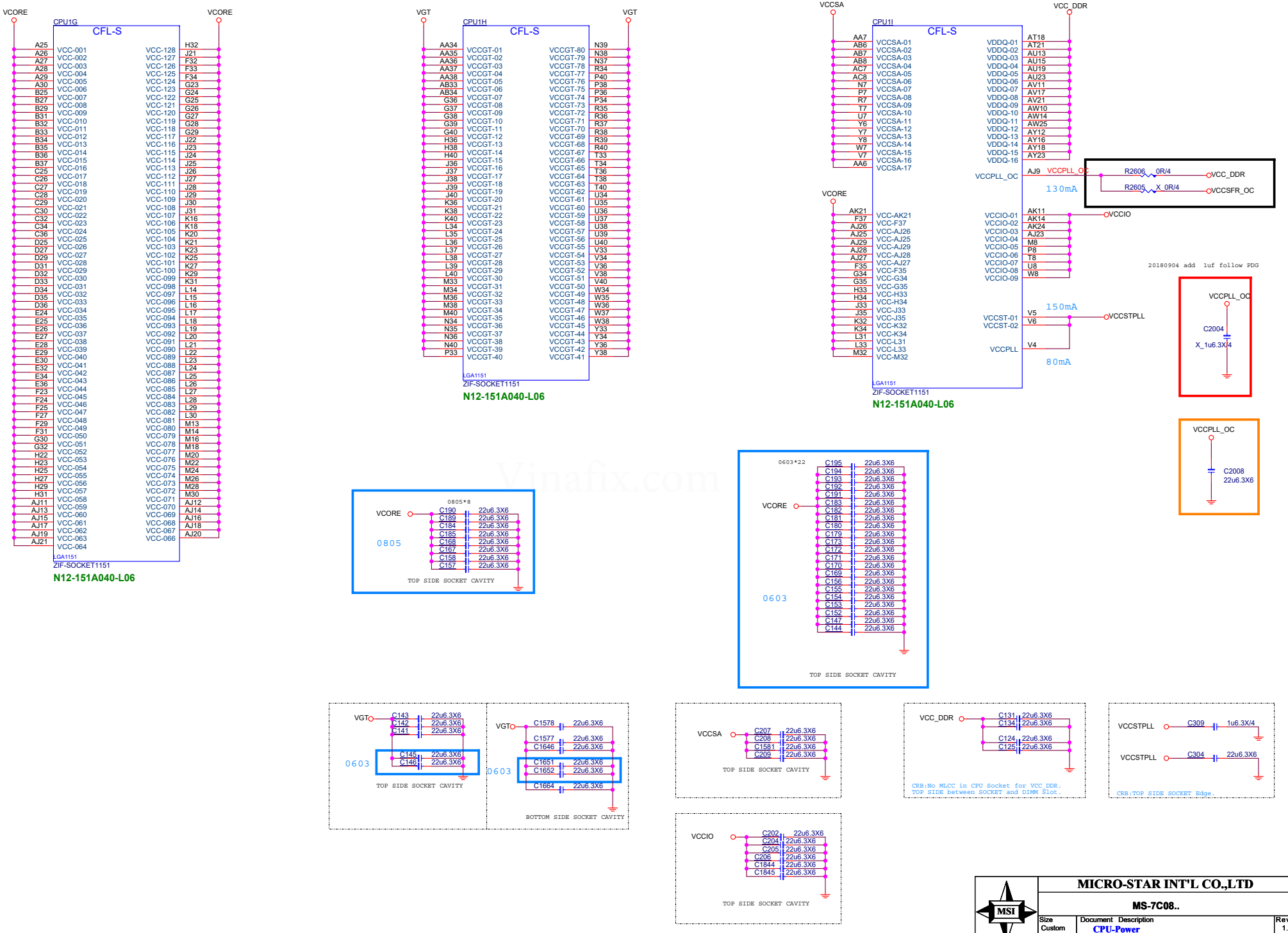


SIO OVT接CPU PROCHOT#使用 SIOOVT做保
RT3607 VRHOT#与CPU PROCHOT#都不使用 RT3607VR功 能 .

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: CPU-Control/MISC/CFG/Audio	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 5 of 60	

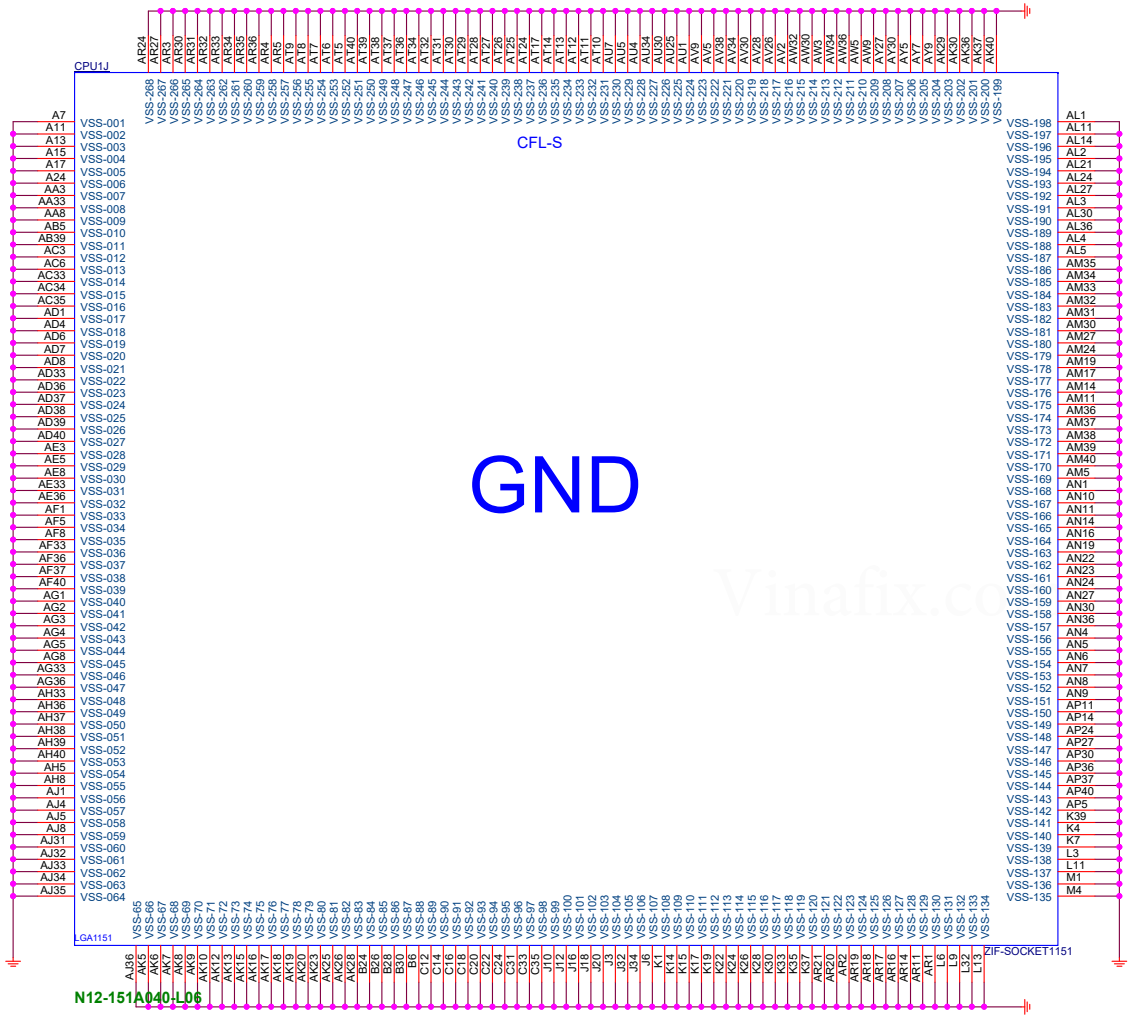


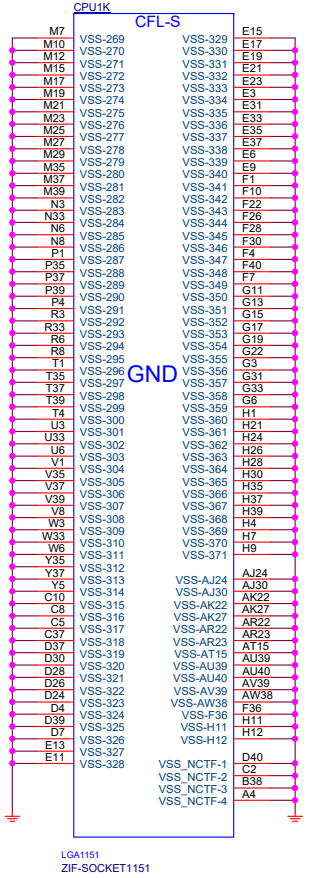
MICRO-STAR INT'L CO.,LTD

MS-7C08..

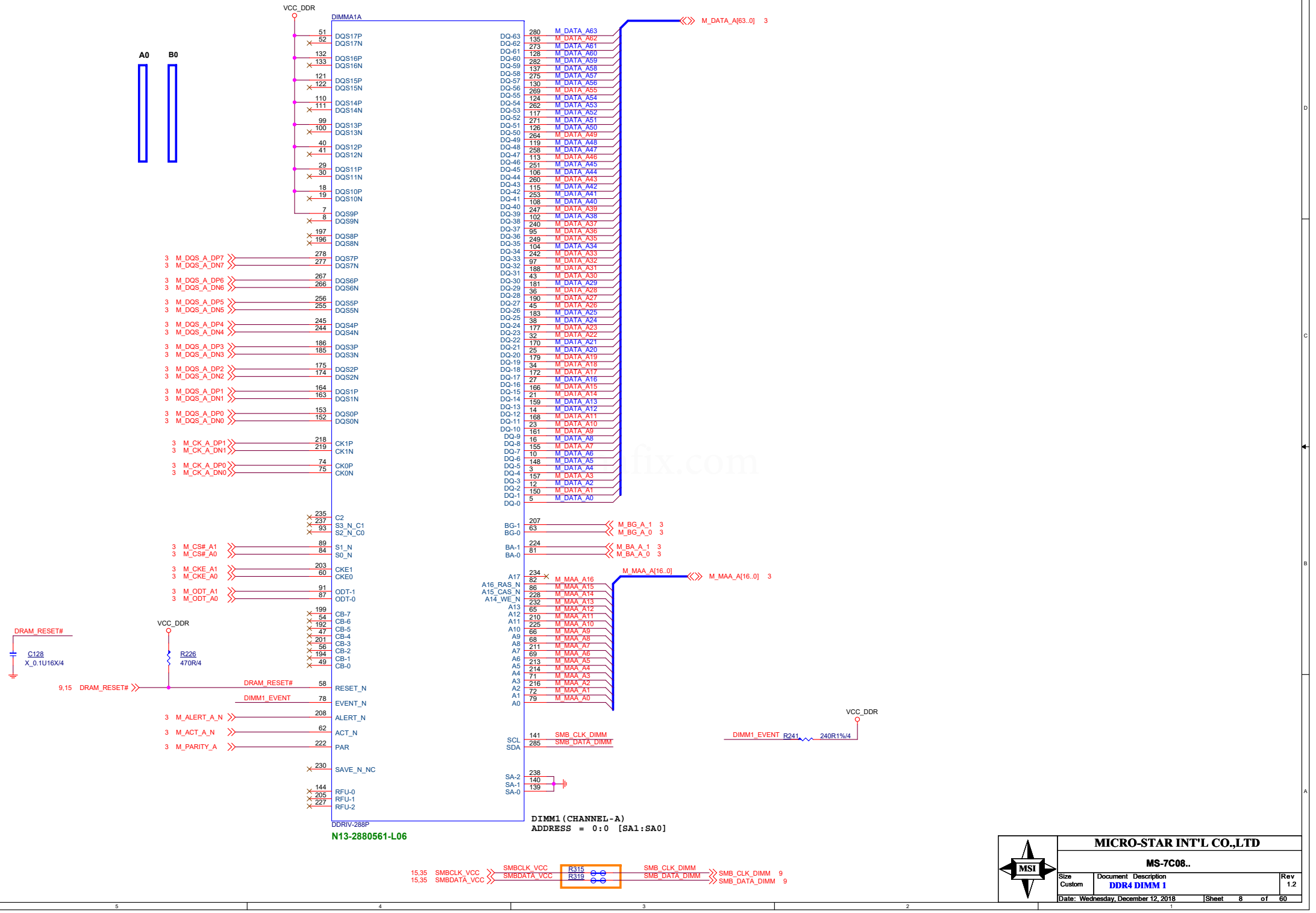
Size	Document Description	Rev
Custom	CPU-Power	1.2

Date: Wednesday, December 12, 2018 Sheet 6 of 60





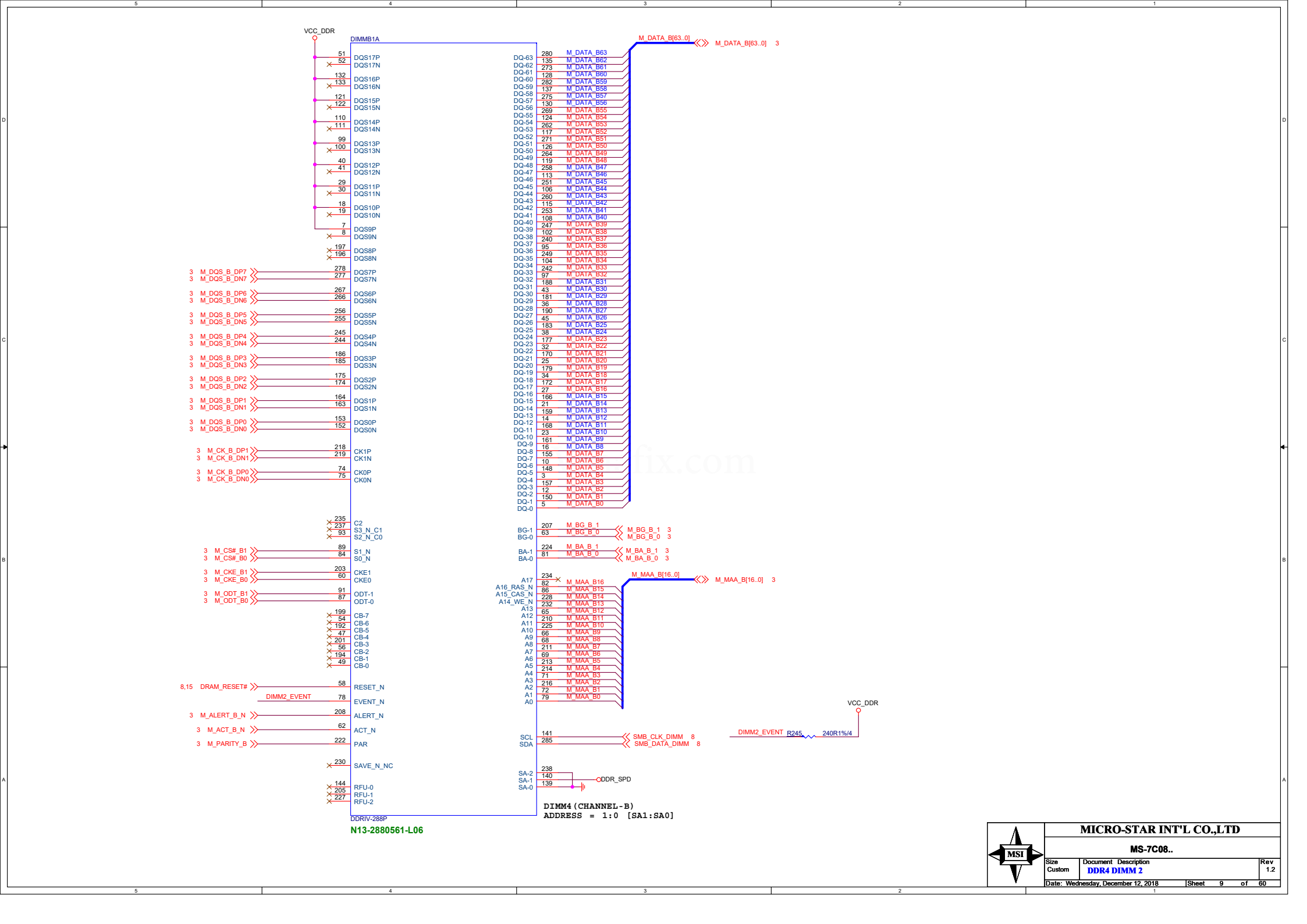
MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: CPU-GND	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 7 of 60	



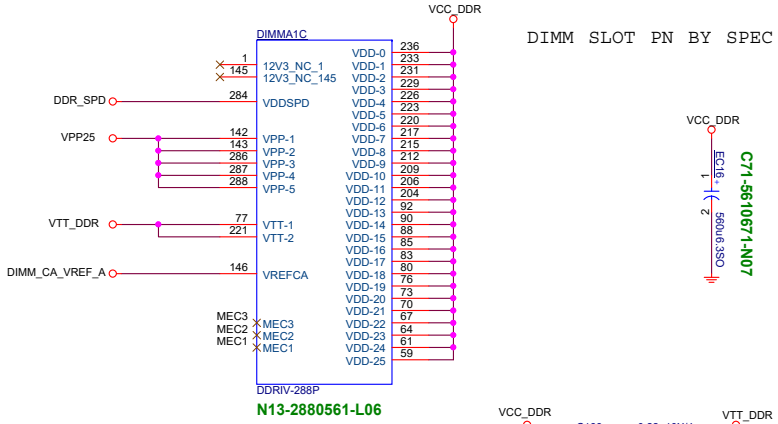
N13-2880561-L06

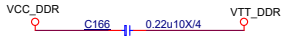
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

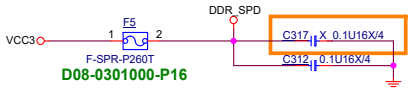
MICRO-STAR INT'L CO.,LTD	
MS-7C08..	
Size: Custom	Document Description: DDR4 DIMM 1
Rev: 1.2	
Date: Wednesday, December 12, 2018	Sheet 8 of 60

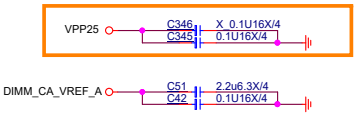


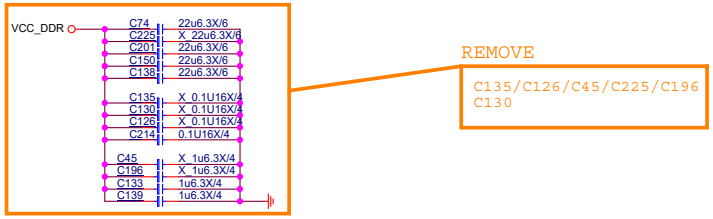
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: DDR4 DIMM 2	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 9 of 60	

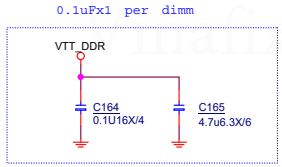


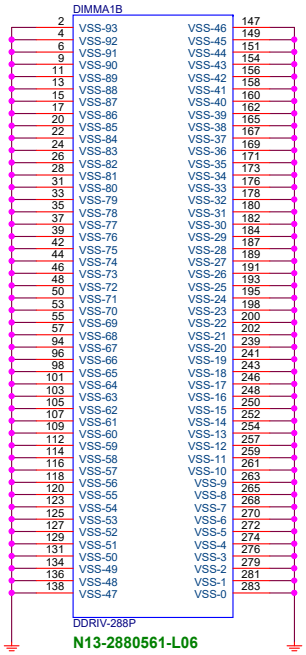


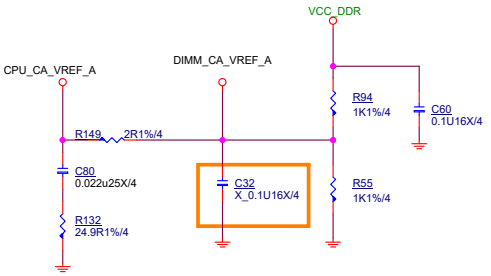


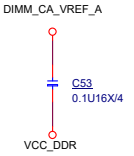




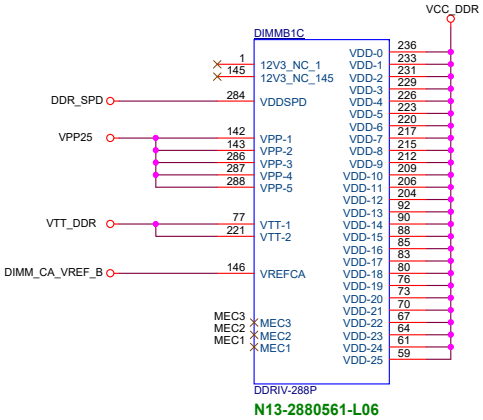


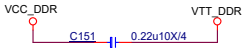


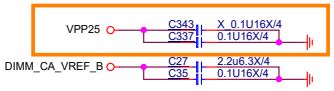


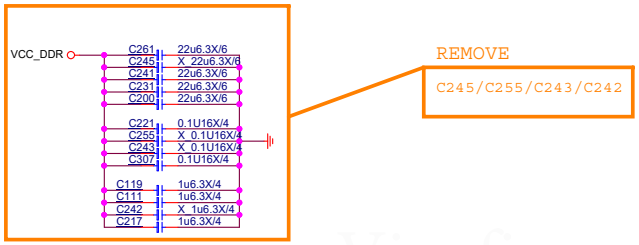


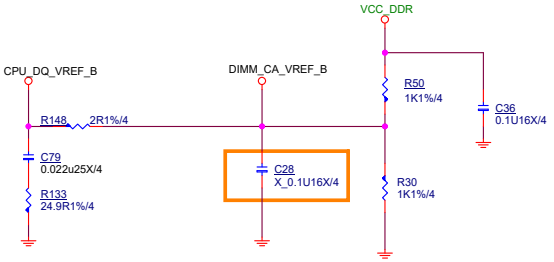
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 10 of 60	

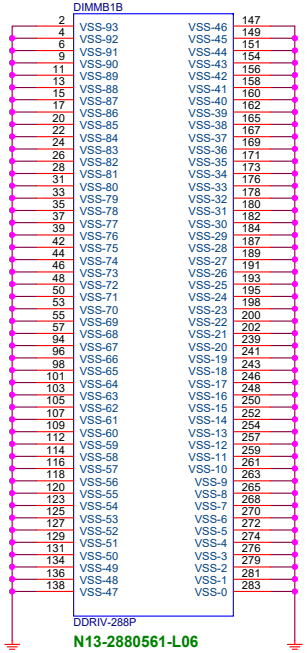


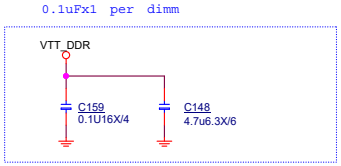


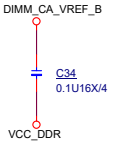












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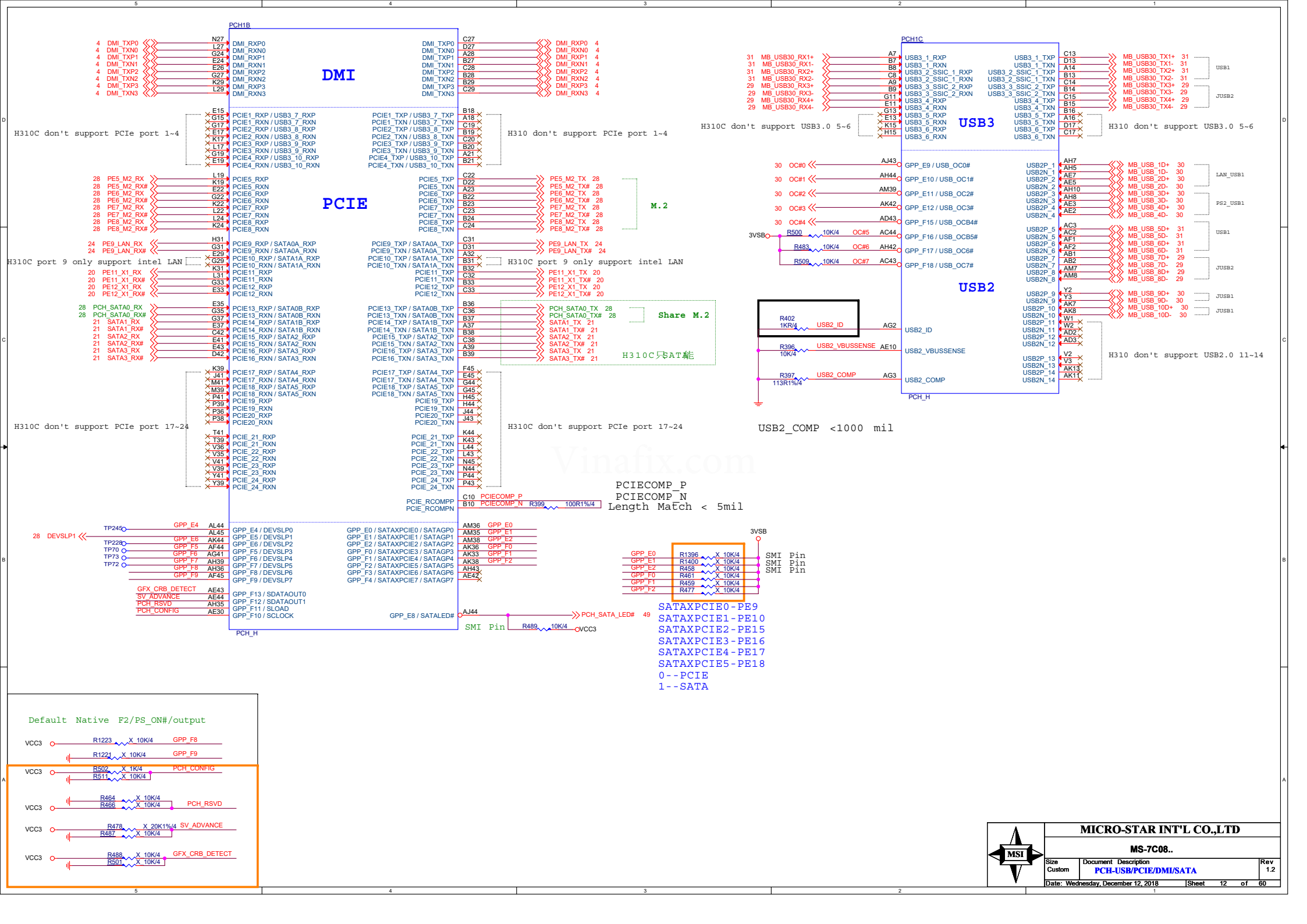
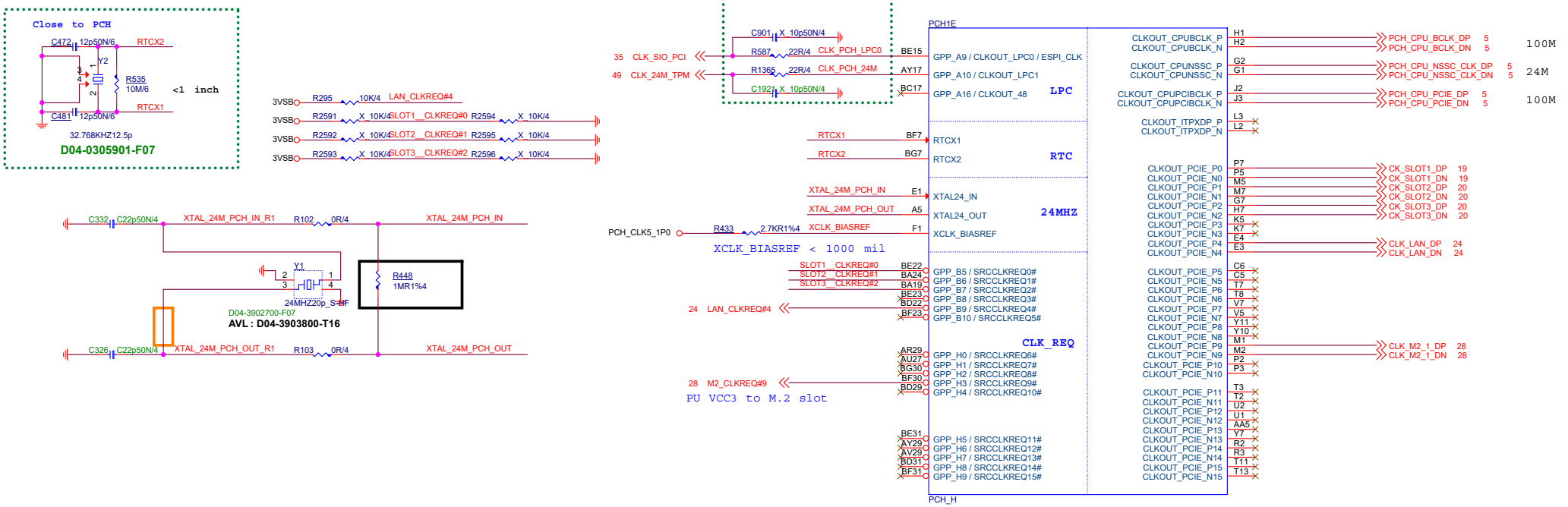
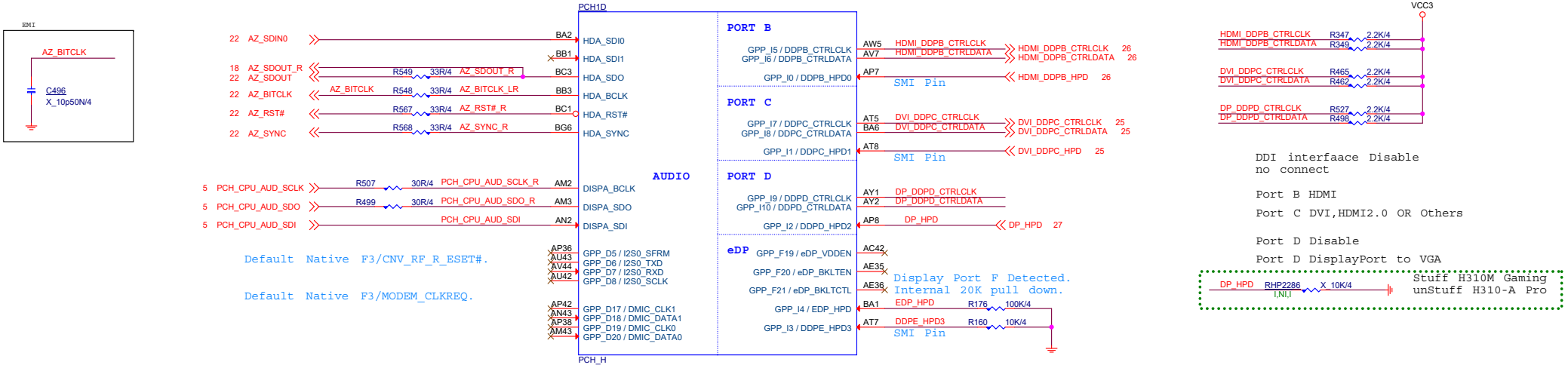
	MS-7C08..	
Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 11 of 60	


PCH1B
DMI
PCIE
M.2
H310C don't support PCIe port 1~4
H310 don't support PCIe port 1~4
H310C port 9 only support intel LAN
H310C don't support PCIe port 17~24
Share M.2
H310C只SATA能
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
PCH_H
PCH1C
USB3
USB2
H310C don't support USB3.0 5~6
H310 don't support USB3.0 5~6
H310 don't support USB2.0 11~14
USB2_COMP <1000 mil
Default Native F2/PS_ON#/output
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
SMI Pin
MICRO-STAR INT'L CO.,LTD
MS-7C08..
PCH-USB/PCIE/DMI/SATA
Date: Wednesday, December 12, 2018
Sheet 12 of 60

RTC Block



Vinafix.com



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MICRO-STAR INT'L CO.,LTD

MS-7C08..

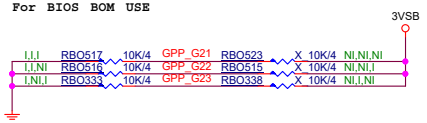
Size	Document Description	Rev
Custom	PCH-Audio/Display/Clock	1.2

Date: Wednesday, December 12, 2018 Sheet 13 of 60

GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)

	GPP_I12	GPP_I13	GPP_I14
H310_GPLUS	0	0	0

For BIOS BOM USE

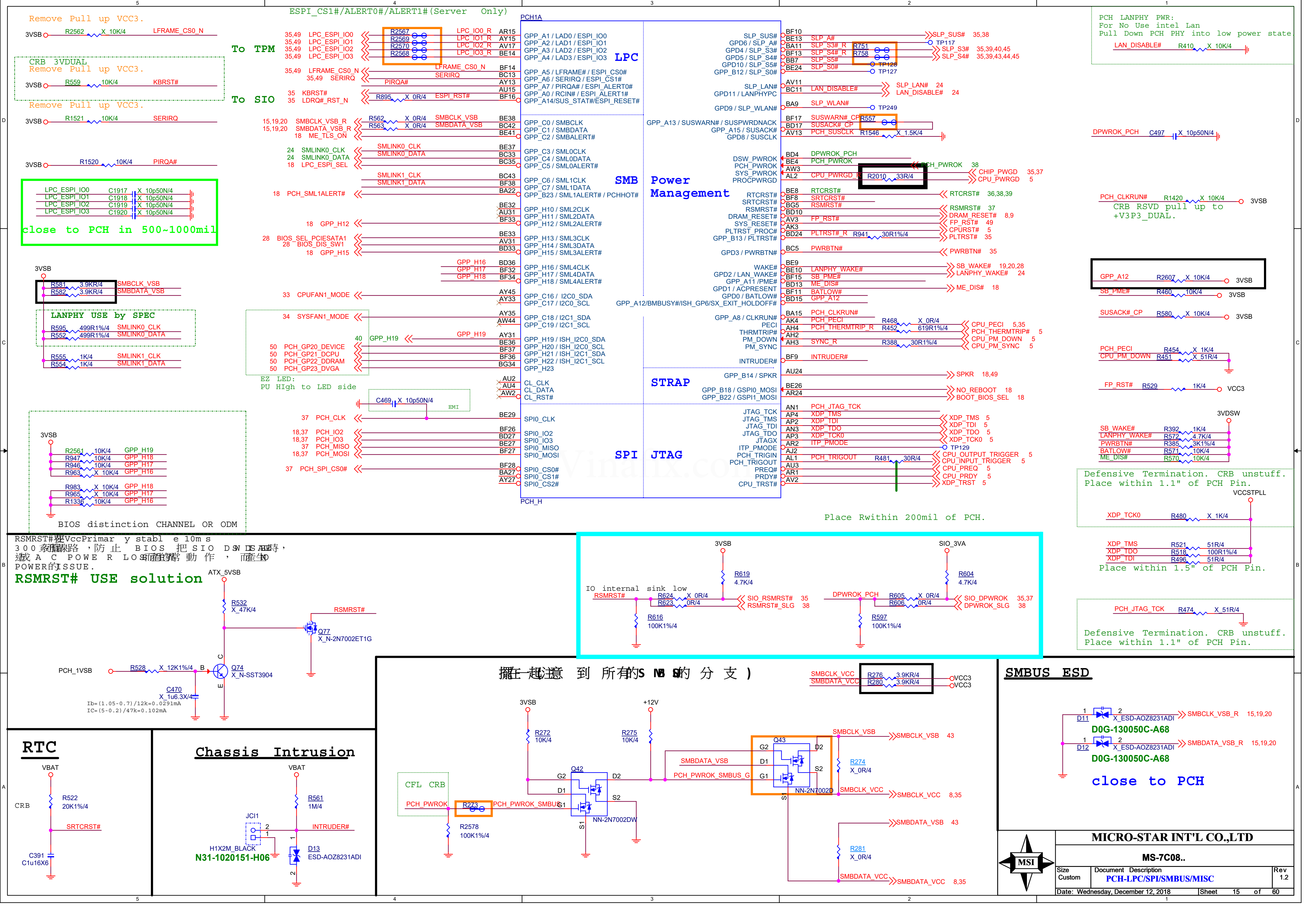


MICRO-STAR INT'L CO.,LTD

MS-7C08..

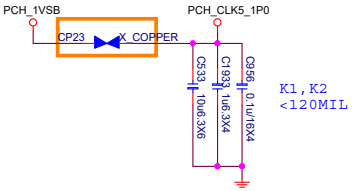
Size	Document Description	Rev
Custom	PCH-GPIO/USBOC#/SATASTRAP	1.2

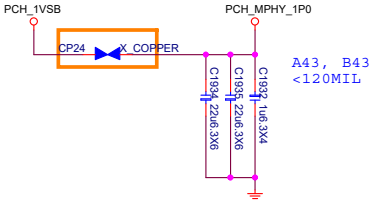
Date: Wednesday, December 12, 2018 Sheet 14 of 60

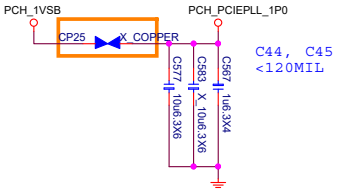


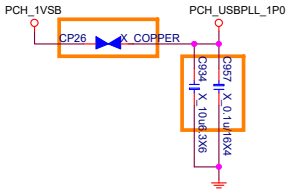
Remove Pull up VCC3.
ESPI_CS1#/ALERT0#/ALERT1#(Server Only)
To TPM
To SIO
CRB 3VDUAL
close to PCH in 500~1000mil
LANPHY USE by SPEC
EZ LED:
PU HIgh to LED side
BIOS distinction CHANNEL OR ODM
LPC
SMB
Power Management
STRAP
SPI
JTAG
PCH1A
PCH_H
PCH LANPHY PWR:
For No Use intel Lan
Pull Down PCH PHY into low power state
CRB RSVD pull up to +V3P3_DUAL.
Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.
Place within 1.5" of PCH Pin.
Place Rwithin 200mil of PCH.
IO internal sink low
RSMRST# USE solution
Ib=(1.05-0.7)/12k=0.0291mA
IC=(5-0.2)/47k=0.102mA
RTC
Chassis Intrusion
CFL CRB
SMBUS ESD
close to PCH
D0G-130050C-A68
N31-1020151-H06
MICRO-STAR INT'L CO.,LTD
MS-7C08..
Size Custom
Document Description
PCH-LPC/SPI/SMBUS/MISC
Rev 1.2
Date: Wednesday, December 12, 2018
Sheet 15 of 60

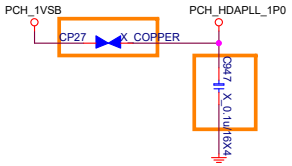
PCH_1VSB 8.72A
VCC3 0.007A
3VSB 0.846A

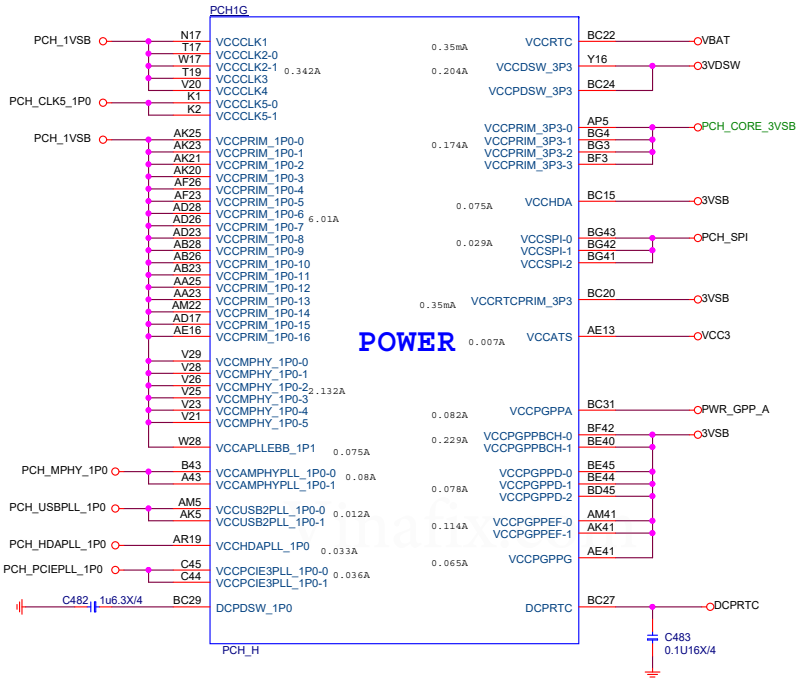


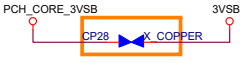


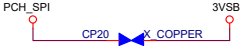


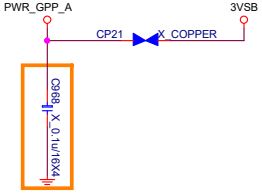


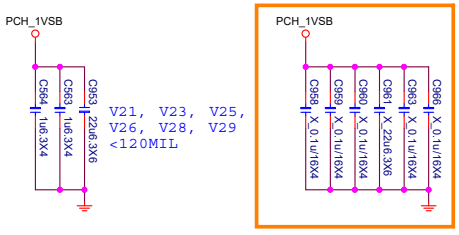


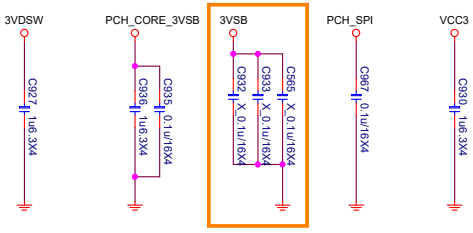


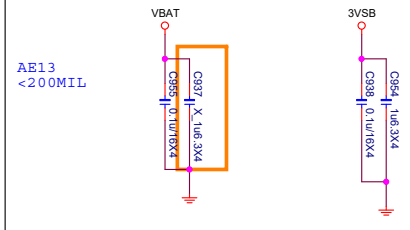










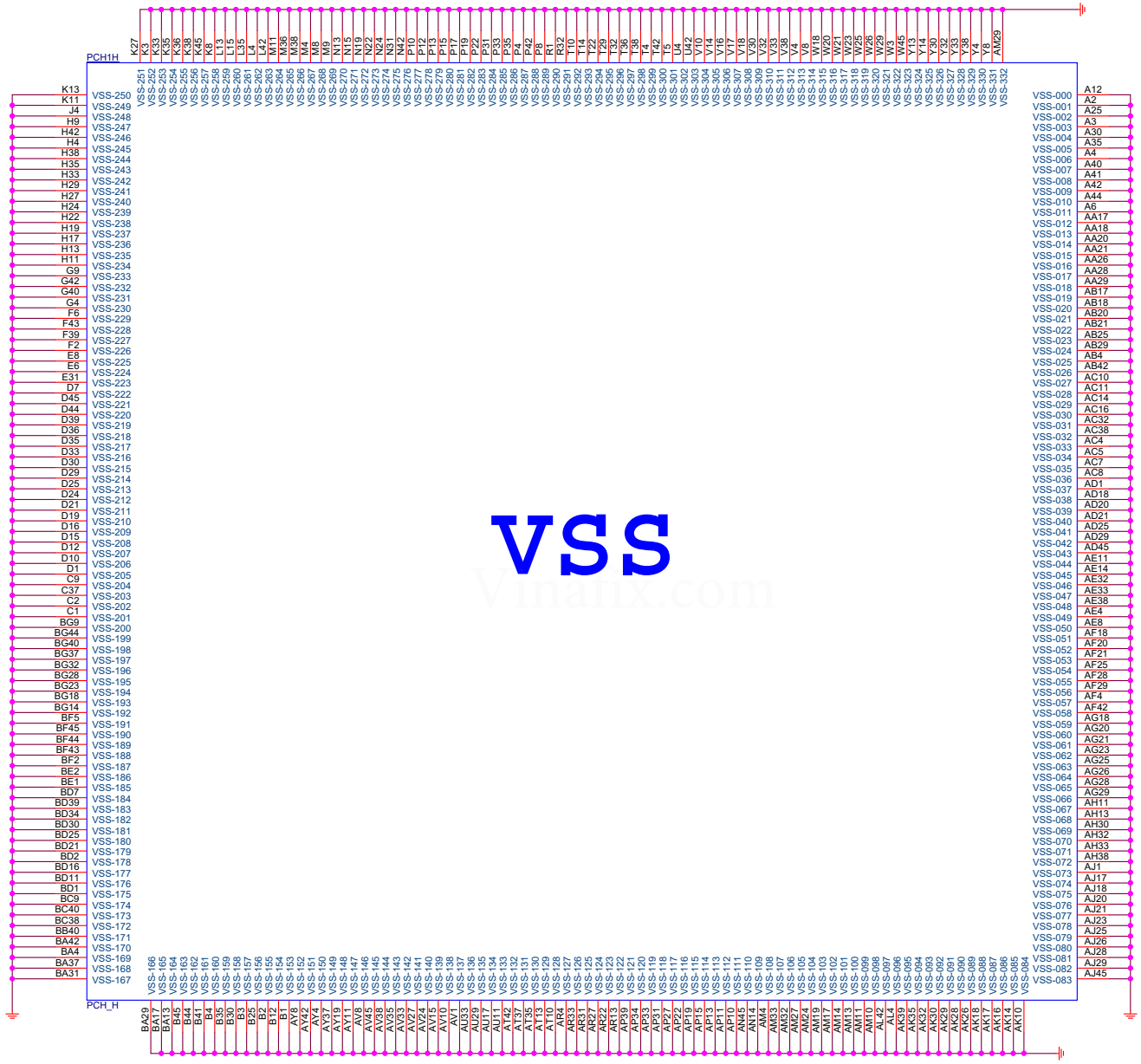


MICRO-STAR INT'L CO.,LTD

MS-7C08..

Size	Document Description	Rev
Custom	PCH-Power	1.2

Date: Wednesday, December 12, 2018 Sheet 16 of 60



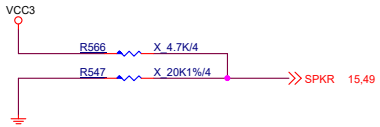
MICRO-STAR INT'L CO.,LTD

MS-7C08..

Size	Document Description	Rev
Custom	PCH-GND	1.2

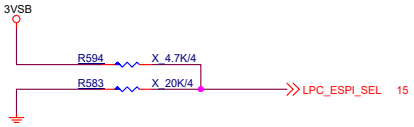
Date: Wednesday, December 12, 2018 | Sheet 17 of 60

TOP Swap



Internal pull-down 20K is disabled after PLTRST#

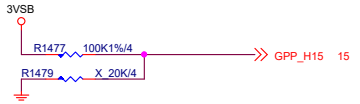
LPC eSPI Mode



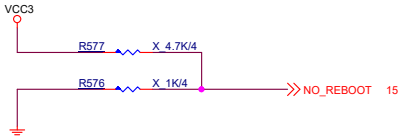
0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Reserved



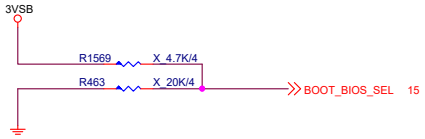
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

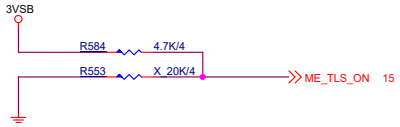
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

AMT and SBA with confidentiality

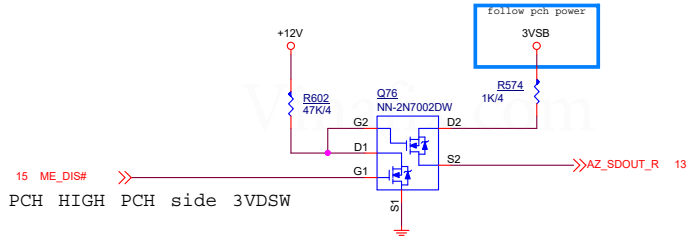


0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

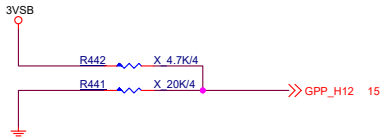
HDA_SDO

ME flash by GPIO



PCH HIGH PCH side 3VDSW

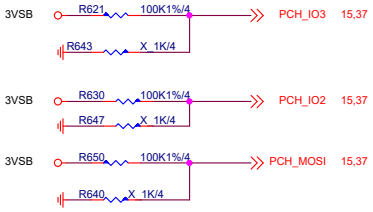
ESPI FLASH SHARING MODE



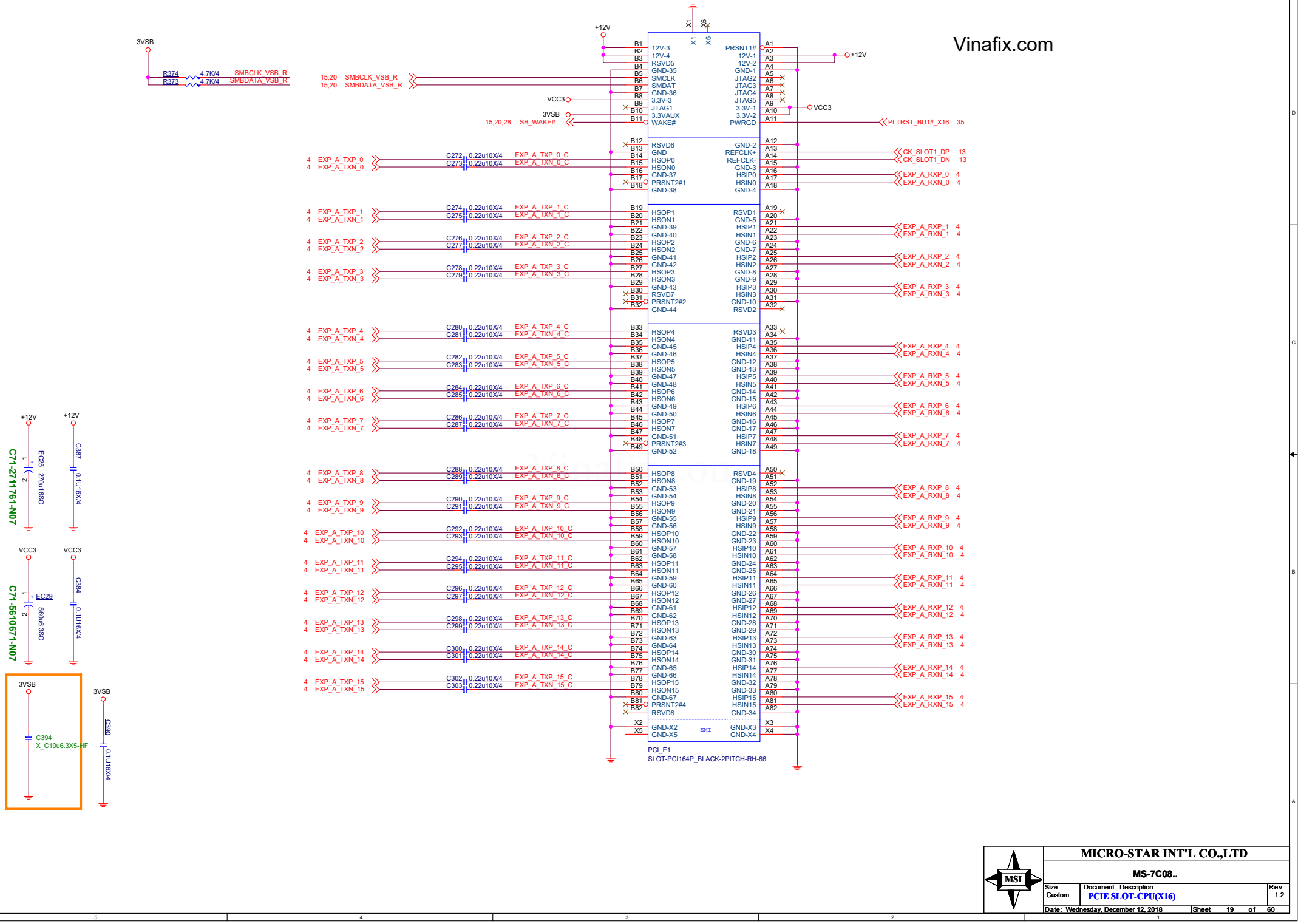
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

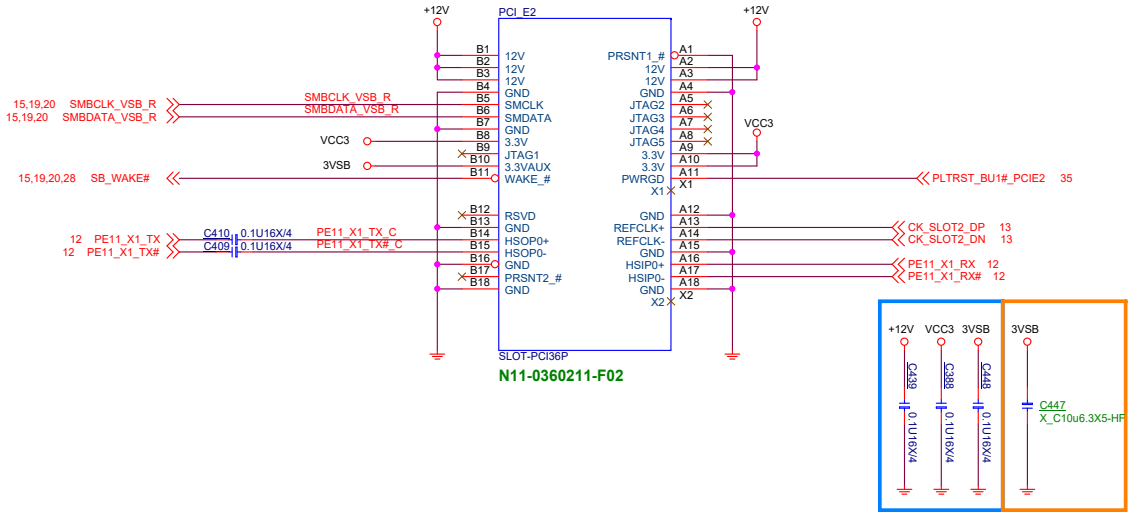
Internal pull-down 20K is disabled after RSMRST

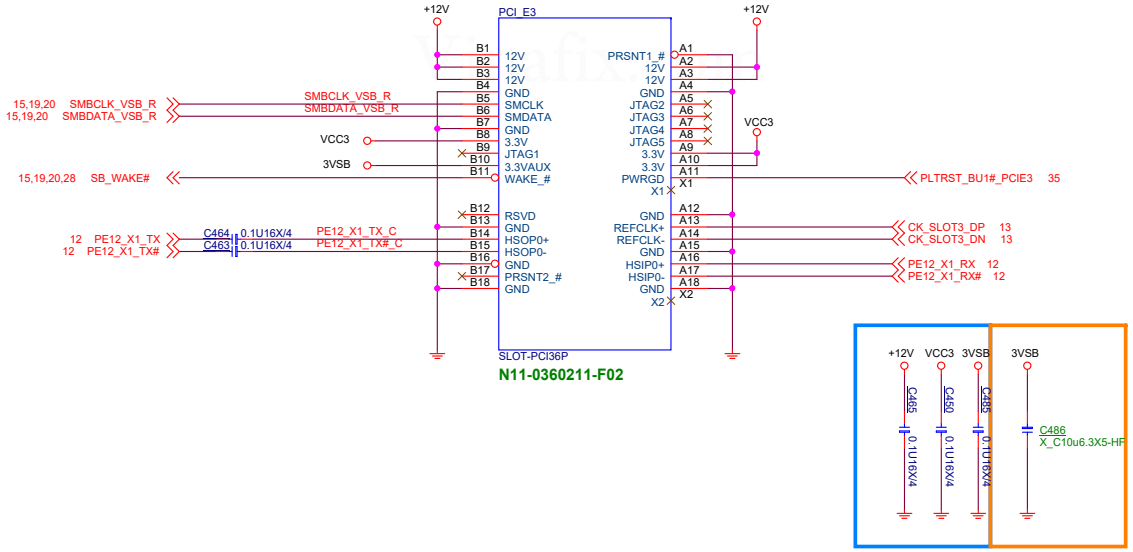
Reserved



MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: PCH-Strap	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 18 of 60	


Vinafix.com
PCI_E1
SLOT-PCI164P_BLACK-2PITCH-RH-66
MICRO-STAR INT'L CO.,LTD
MS-7C08..
PCIE SLOT-CPU(X16)
Rev 1.2
Date: Wednesday, December 12, 2018
Sheet 19 of 60





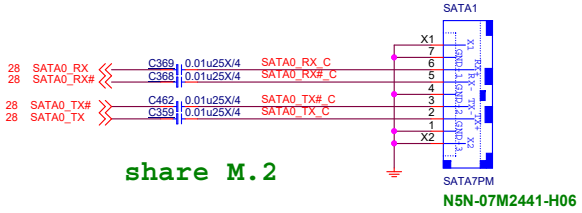
MICRO-STAR INT'L CO.,LTD

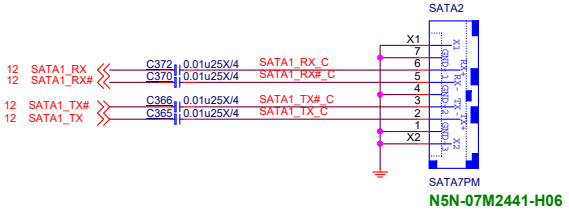
MS-7C08..

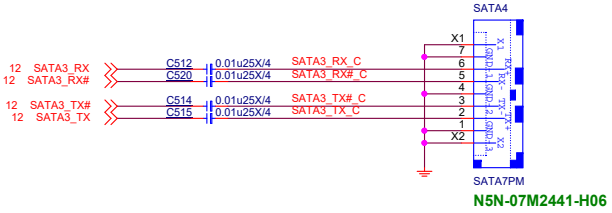
Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	1.2

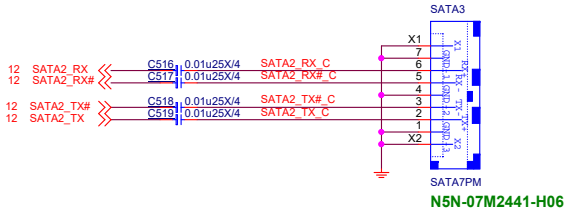
Date: Wednesday, December 12, 2018 Sheet 20 of 60

SATA 6G







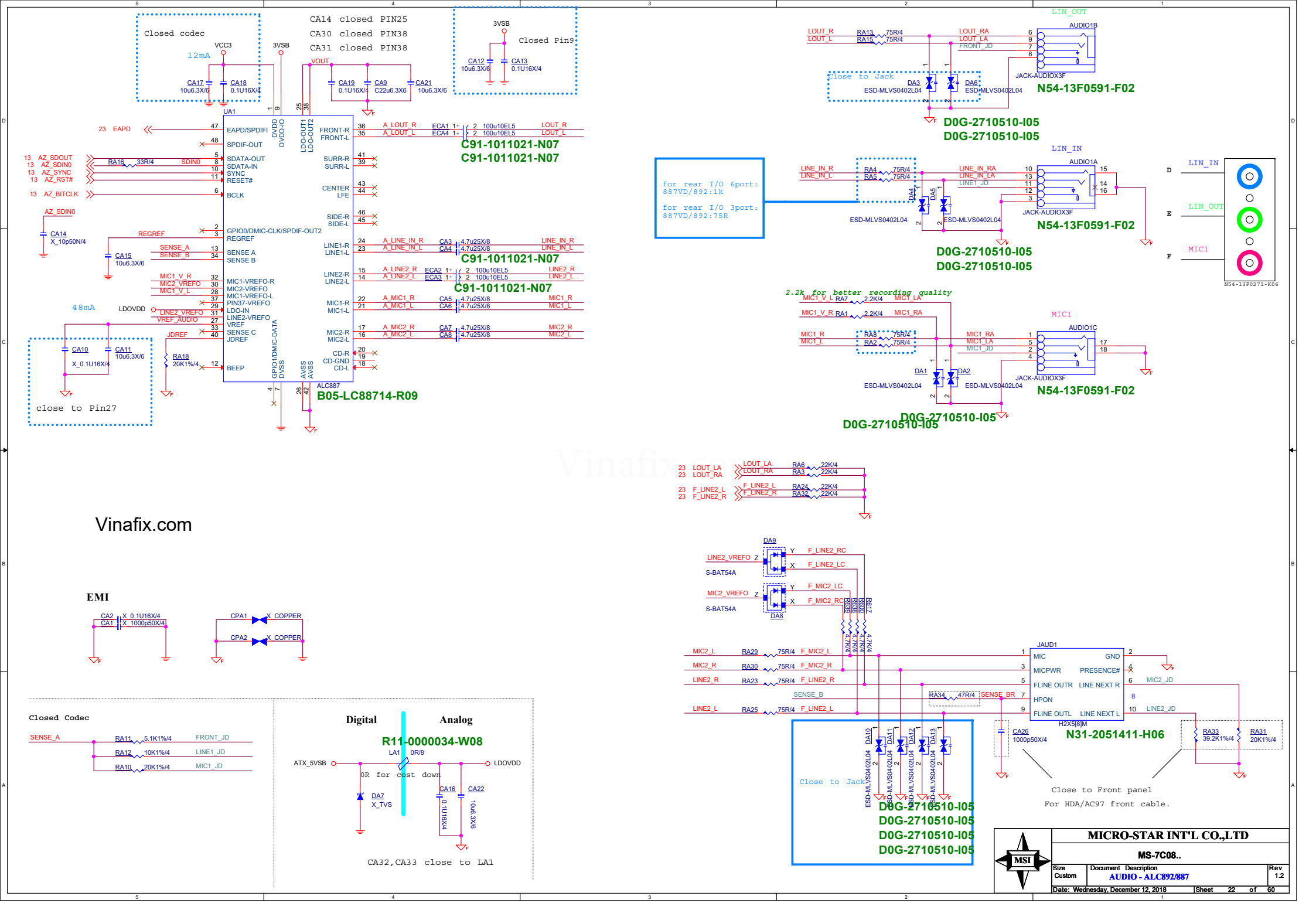


MICRO-STAR INT'L CO.,LTD

MS-7C08..

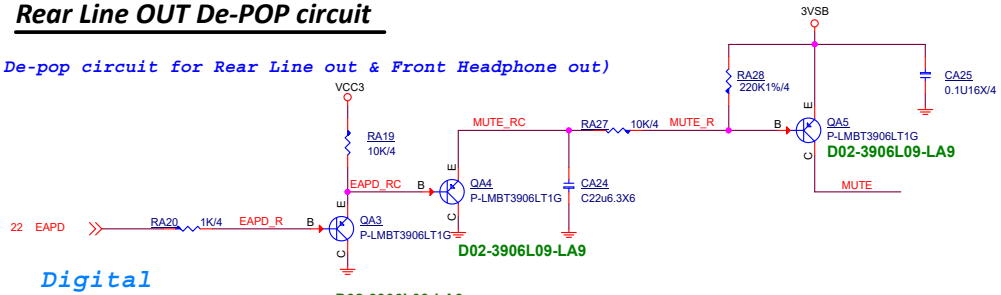
Size	Document Description	Rev
Custom	SATA connector	1.2

Date: Wednesday, December 12, 2018 Sheet 21 of 60

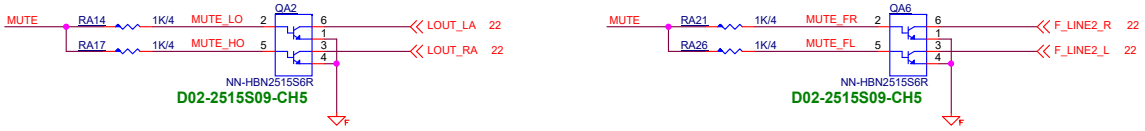

Closed codec
VCC3
12mA
3VSB
CA17 10u6.3X/6
CA18 0.1U16X/4
CA14 closed PIN25
CA30 closed PIN38
CA31 closed PIN38
VOUT
CA19 0.1U16X/4
CA9 C22u6.3X6
CA21 10u6.3X/6
Closed Pin9
CA12 10u6.3X/6
CA13 0.1U16X/4
UA1
EAPD/SPDIFI
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
SENSE C
JDREF
BEEP
GPIO1/DMIC-DATA
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
CD-R
CD-GND
CD-L
AVSS
ALC887
B05-LC88714-R09
C91-1011021-N07
C91-1011021-N07
C91-1011021-N07
close to Pin27
LIN_OUT
AUDIO1B
JACK-AUDIOX3F
close to Jack
ESD-MLVS0402L04
N54-13F0591-F02
D0G-2710510-I05
D0G-2710510-I05
LIN_IN
AUDIO1A
for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R
N54-13F0591-F02
D0G-2710510-I05
D0G-2710510-I05
N54-13F0271-K06
2.2k for better recording quality
MIC1
AUDIO1C
N54-13F0591-F02
D0G-2710510-I05
D0G-2710510-I05
Vinafix.com
EMI
Closed Codec
Digital
Analog
R11-0000034-W08
ATX_5VSB
LDOVDD
0R for cost down
CA32,CA33 close to LA1
DA9
DA8
S-BAT54A
JAUD1
H2X5[8]M
N31-2051411-H06
Close to Jack
Close to Front panel
For HDA/AC97 front cable.
MICRO-STAR INT'L CO.,LTD
MS-7C08..
AUDIO - ALC892/887
Date: Wednesday, December 12, 2018
Sheet 22 of 60

Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

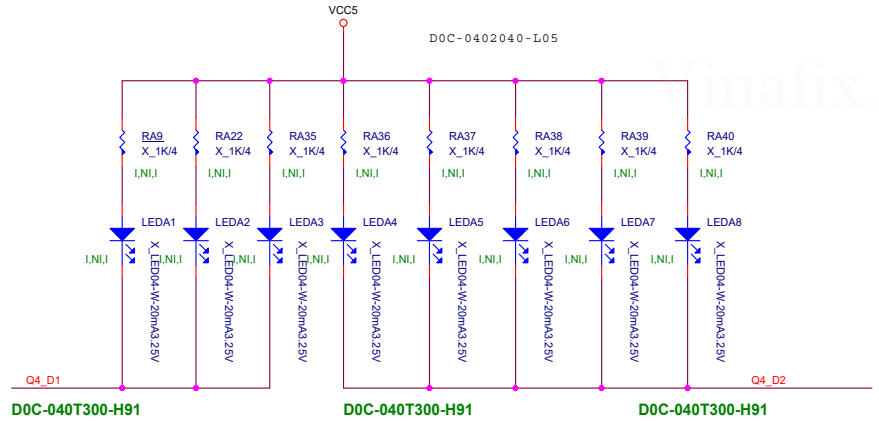


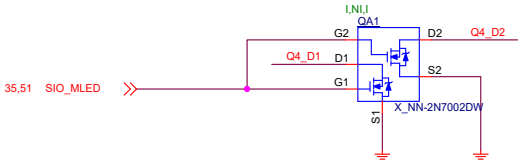
Analog



Audio moat is transparent and width 40mil

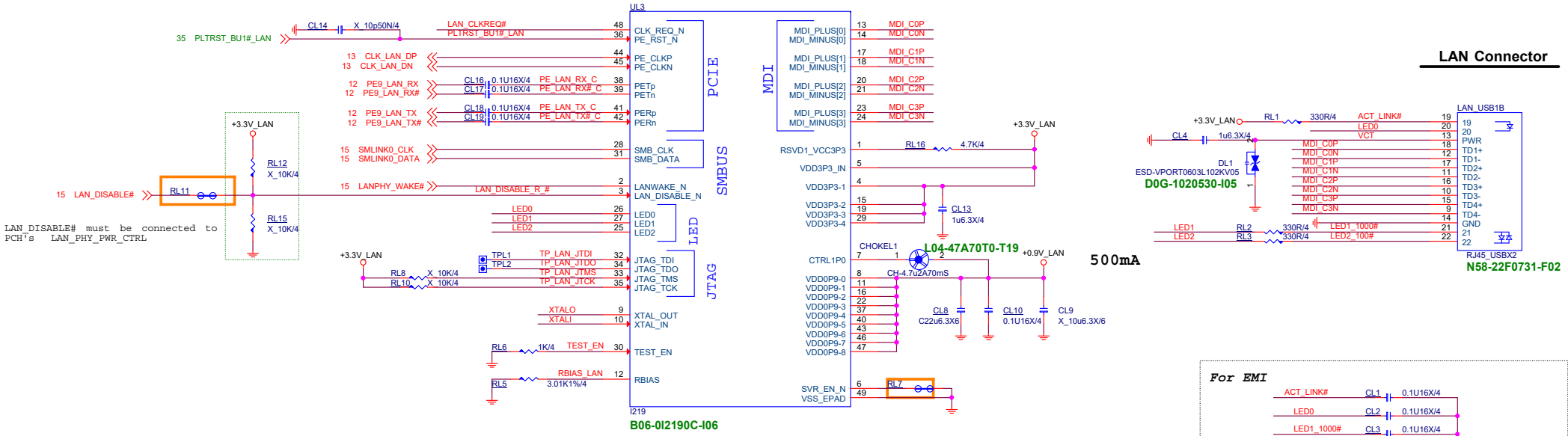
Audio LED





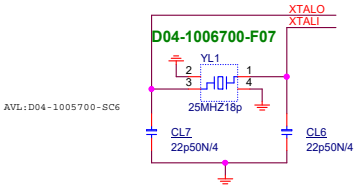
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: AUDIO - depop circuit	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 23 of 60	

Intel Lan- I219



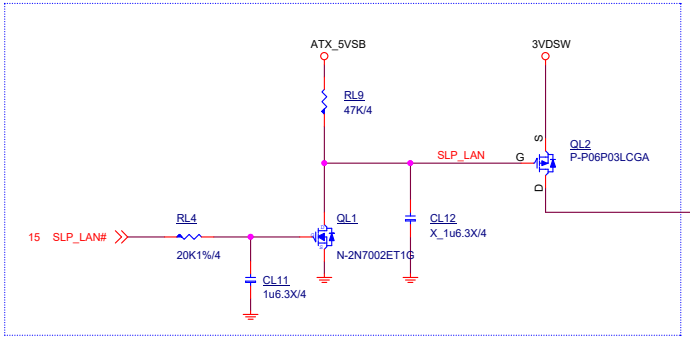
B06-0I2190C-I06

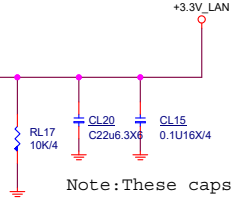
LAN Connector



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.





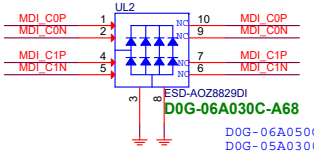
+3.3V_LAN

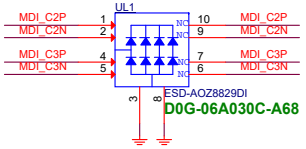
I219:542mW

Note:These caps closed to PHY

For EMI

UL2&UL3 close to connector



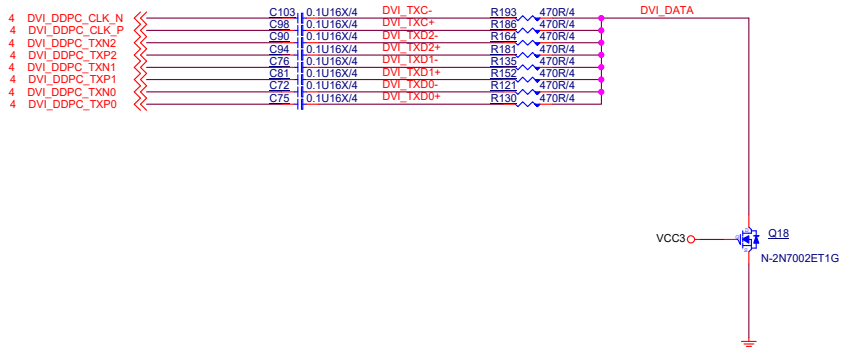


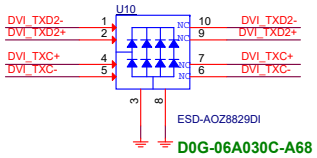
Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue).
Otherpairing combination is ok.

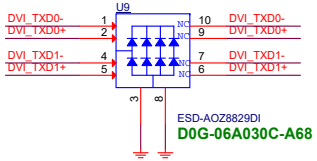
MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: LAN - I219	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 24 of 60	

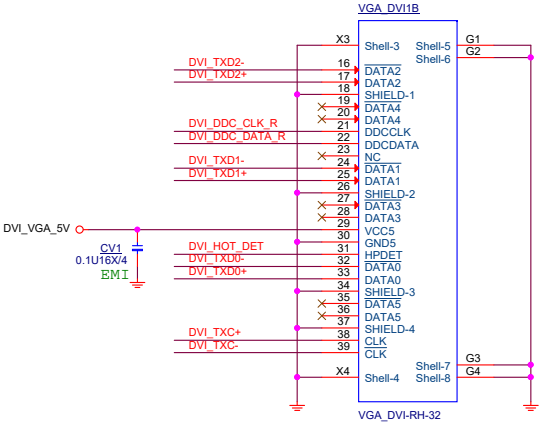
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

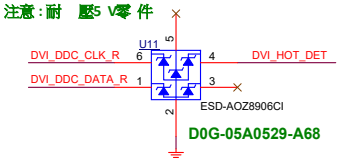




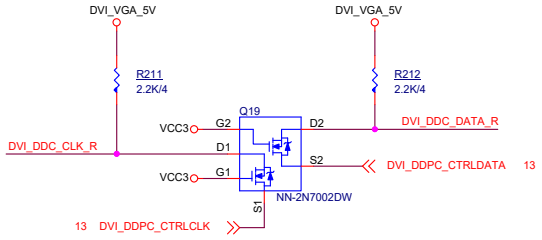




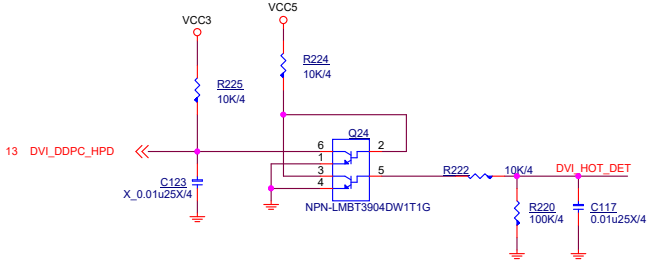
注意:耐 壓5 V零 件

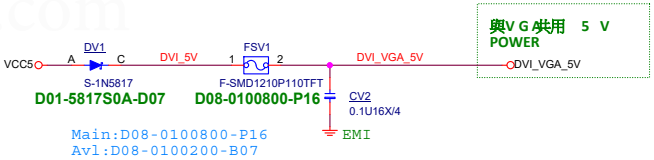


LEVEL SHIFT using I2C Repeater



HPD





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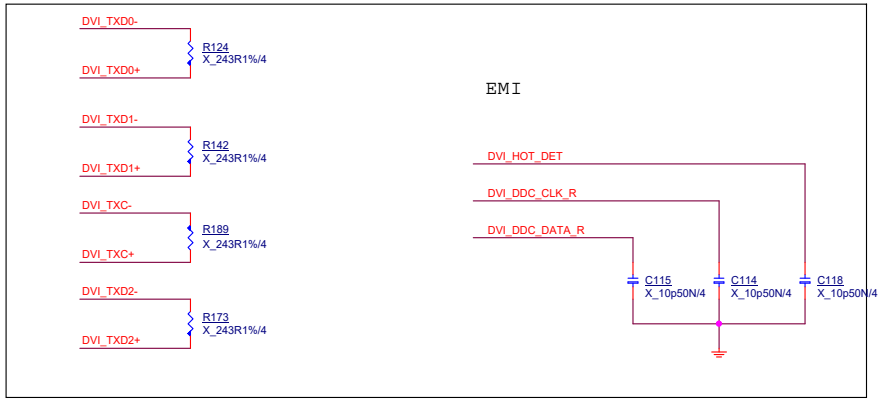
Avl:D08-0100200-B07



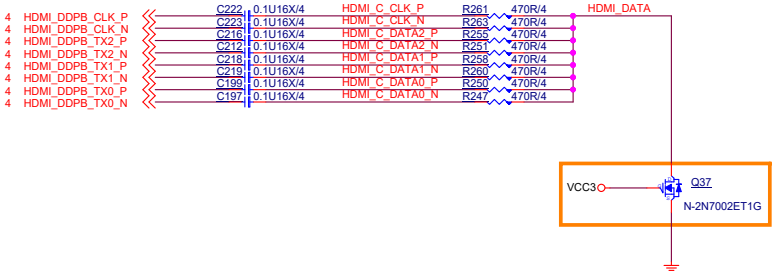
MICRO-STAR INT'L CO.,LTD

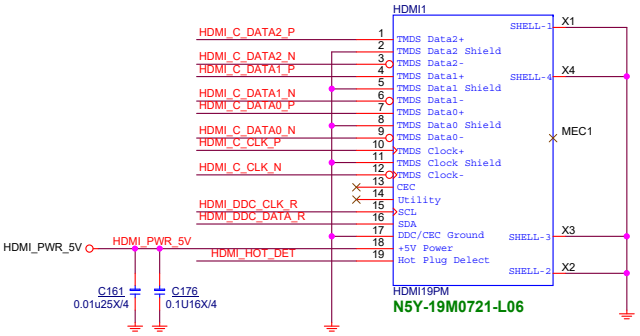
MS-7C08..

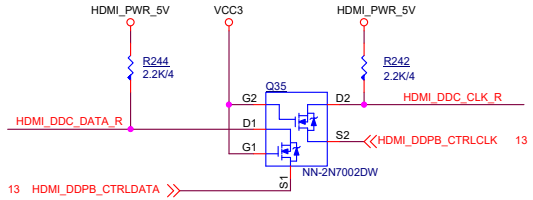
Size	Document Description	Rev
Custom	DVI	1.2

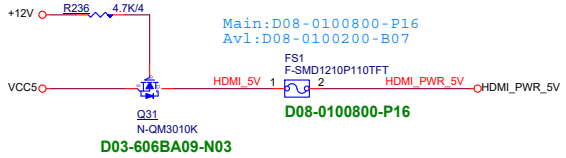
Date: Wednesday, December 12, 2018 Sheet 25 of 60

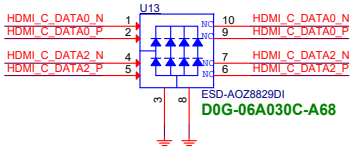
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

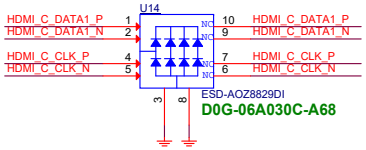


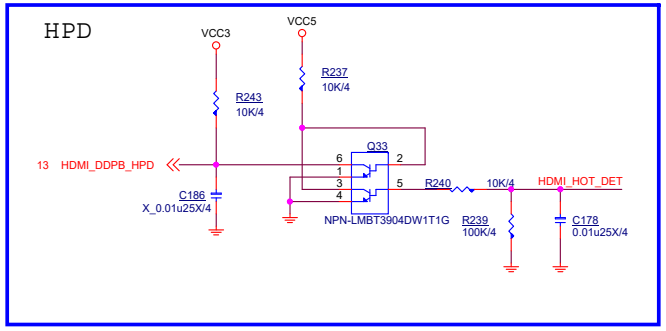


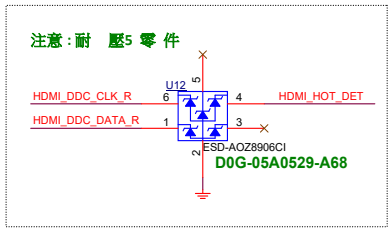


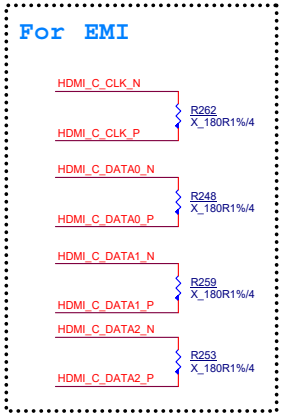








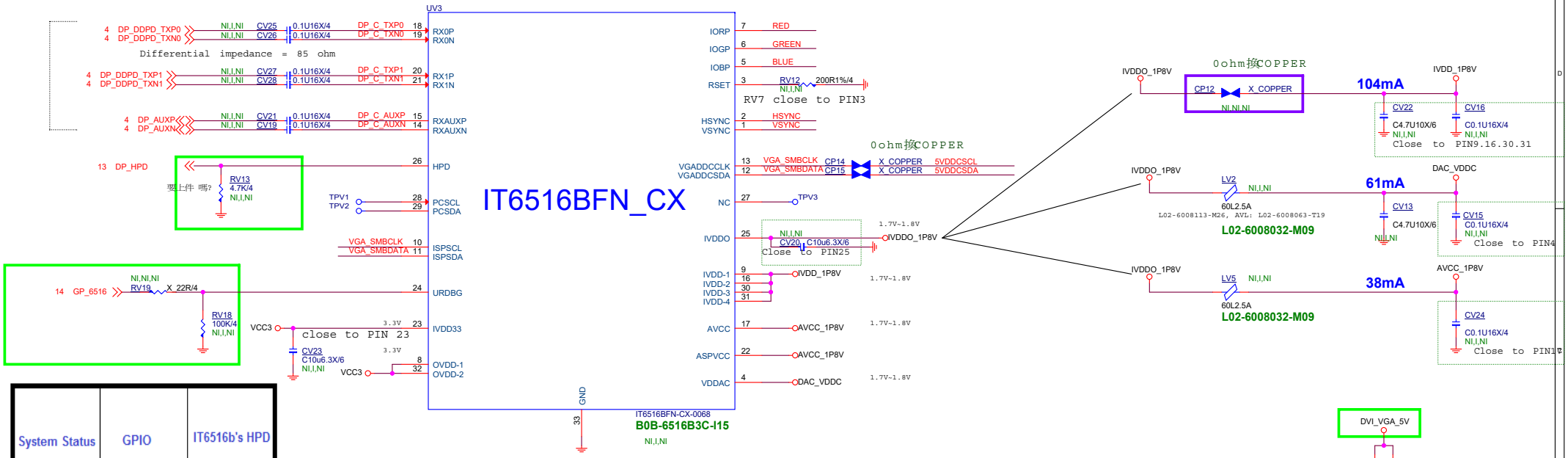




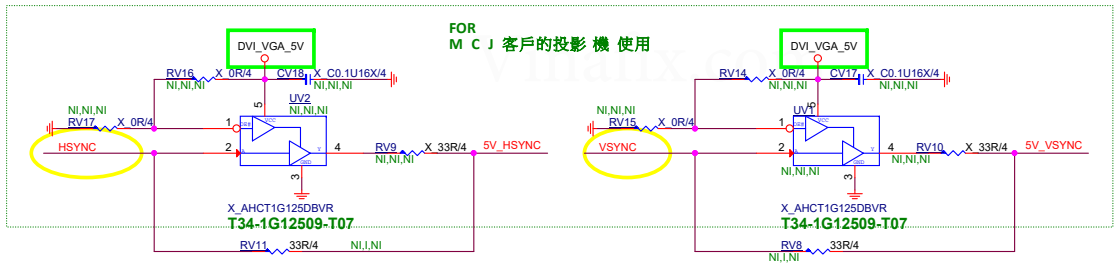
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: HDMI Connector	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 26 of 60	

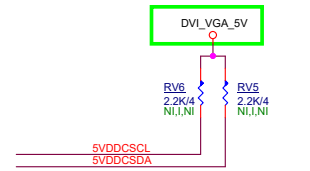
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

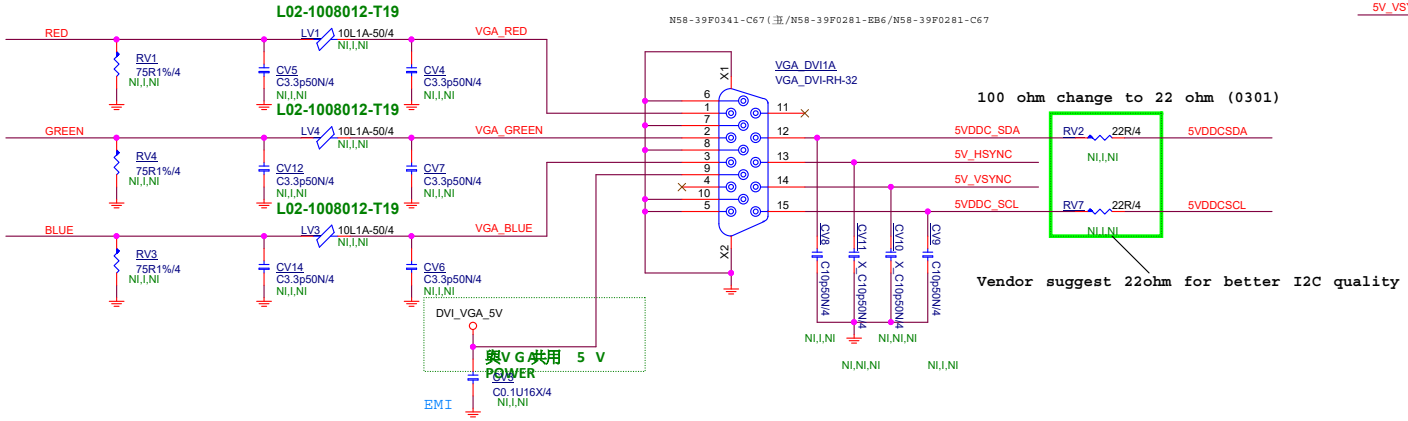


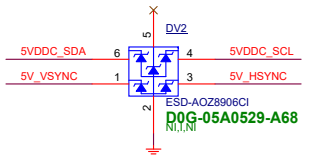
System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

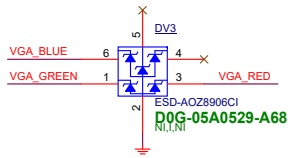




If have VSIS1.2 SPEC requset,can change bead to L02-2208012-M09 use, It test pass.







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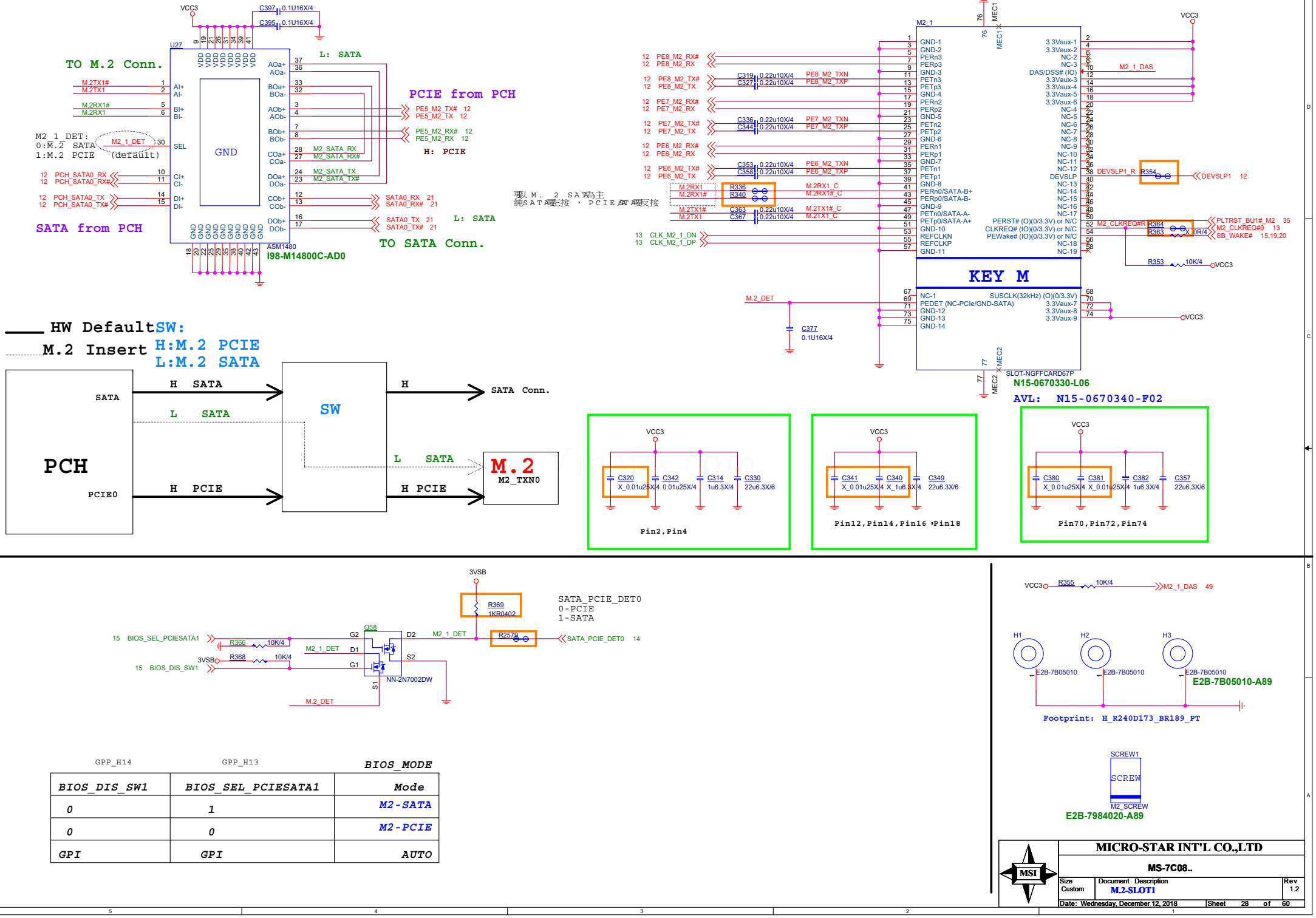
MS-7C08..

Size: Custom | Document Description: VGA - IT6516 | Rev: 1.2

Date: Wednesday, December 12, 2018 | Sheet 27 of 60



要默认M.2 SATA為主
純SATA硬碟接，PCIE/ST硬碟反接

GPP_H14	GPP_H13	BIOS_MODE
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

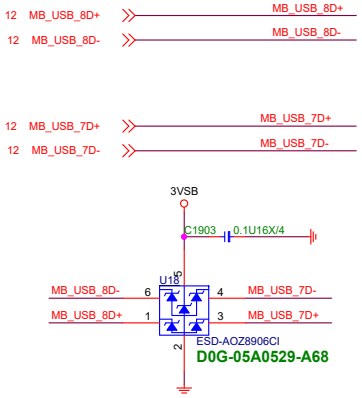
MICRO-STAR INT'L CO.,LTD

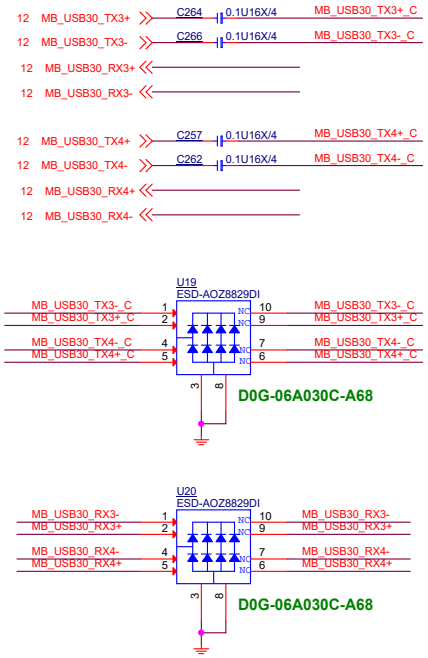
MS-7C08..

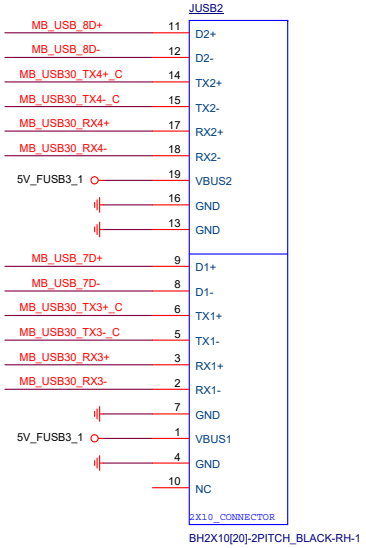
Size	Document Description	Rev
Custom	M.2-SLOT1	1.2

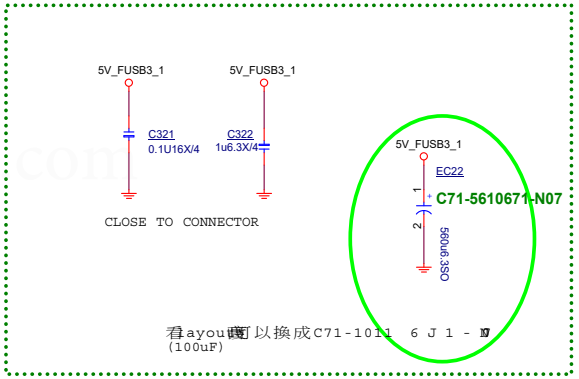
Date: Wednesday, December 12, 2018 Sheet 28 of 60

Front JUSB3 port 7,8

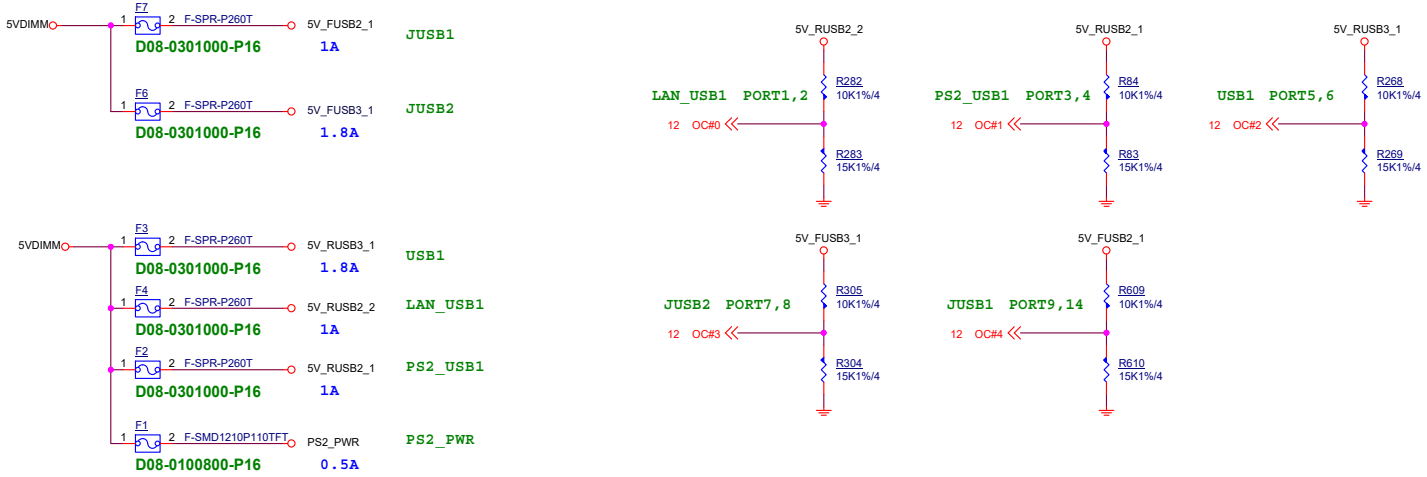






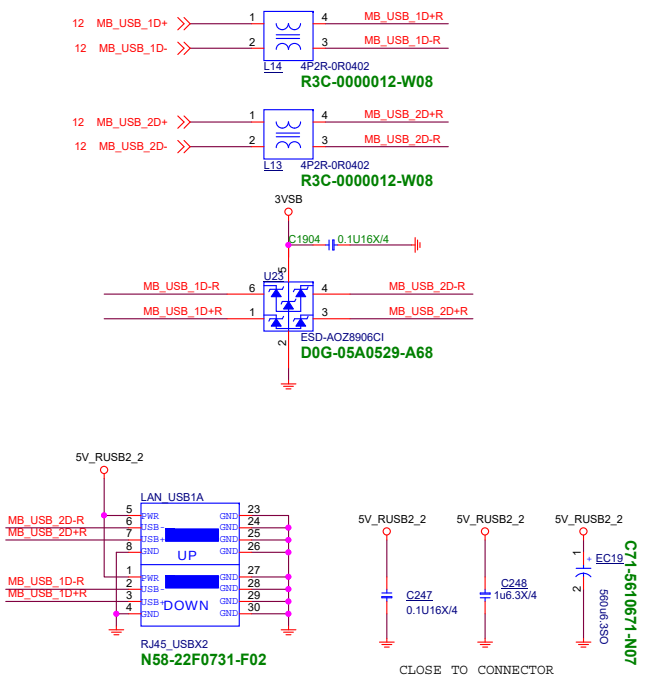


MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: Front USB3.0 Connector	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 29 of 60	

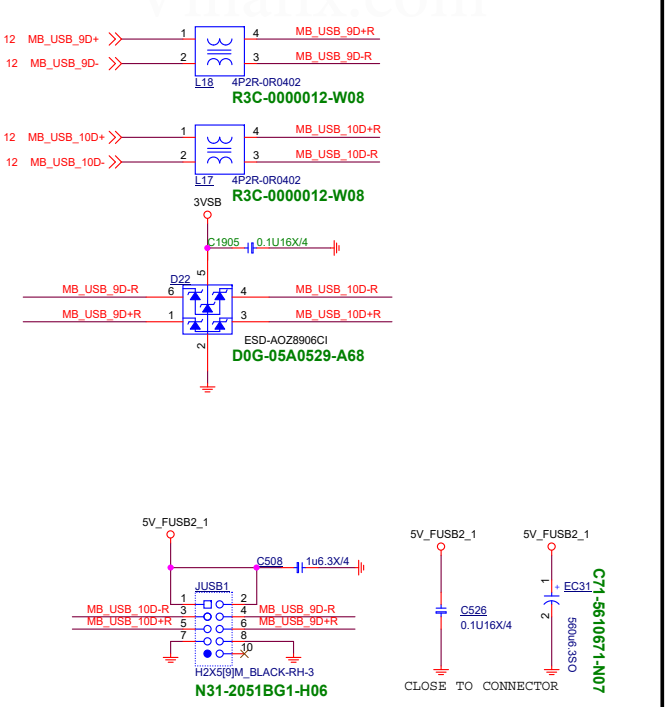


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_RUSB2_2	Port1,2	OC#0
PS2_USB1	5V_RUSB2_1	Port3,4	OC#1
USB1	5V_RUSB3_1	Port5,6	OC#2
JUSB2	5V_FUSB3_1	Port7,8	OC#3
JUSB1	5V_FUSB2_1	Port9,14	OC#4

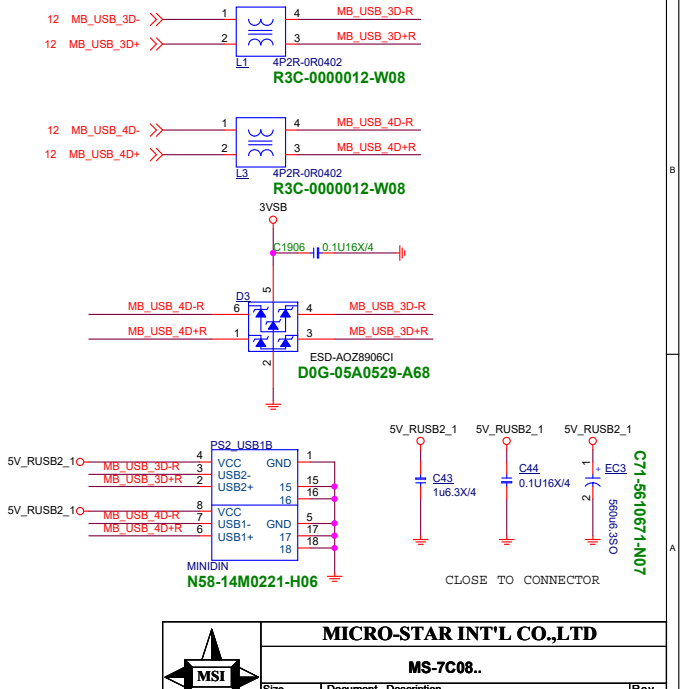
Rear USB1 port 1,2



JUSB1 PORT 9,14



PS2_USB1 PORT 3,4



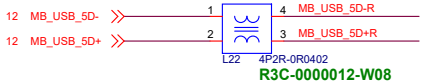
MICRO-STAR INT'L CO.,LTD

MS-7C08..

Size	Document Description	Rev
Custom	USB2.0 Connector	1.2

Date: Wednesday, December 12, 2018 | Sheet 30 of 60

REAR USB1 Connect



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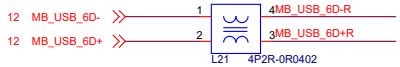
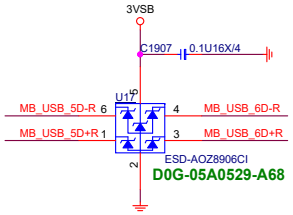


R3C-0000012-W08



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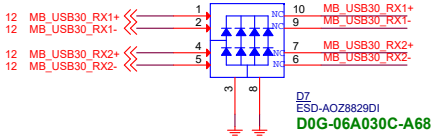

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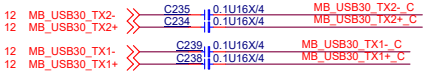

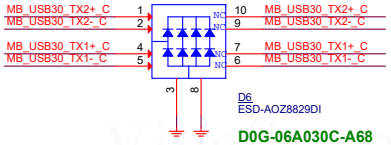

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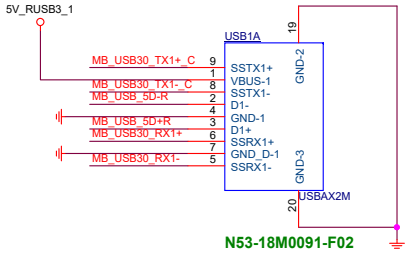
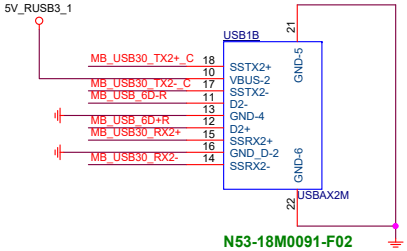


N53-18M0091-F02



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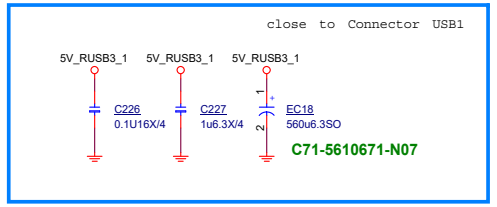
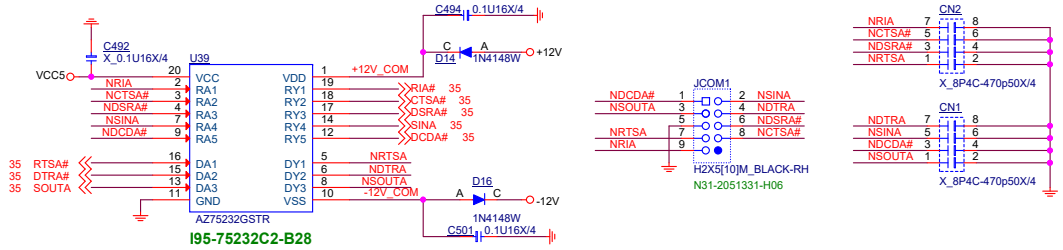


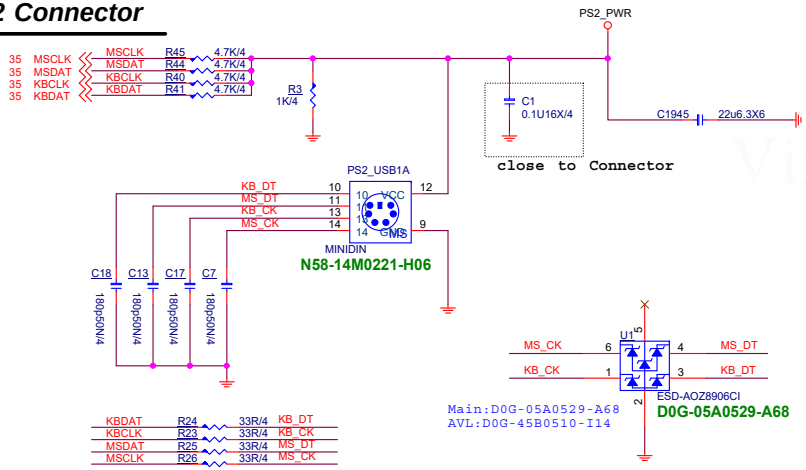
C71-5610671-N07

MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: REAR USB1 Connect	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 31 of 60	

SERIAL PORT 1



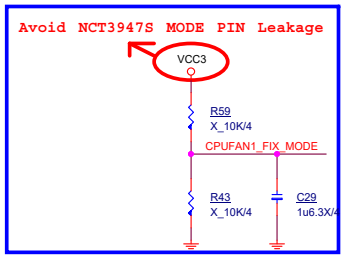
PS2 Connector

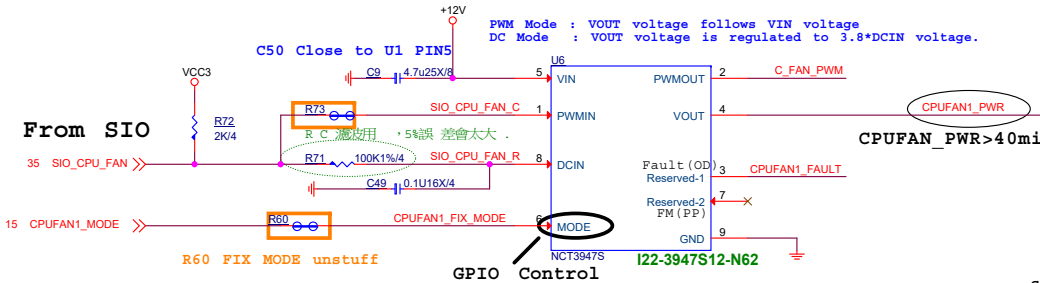


MICRO-STAR INT'L CO.,LTD	
MS-7C08..	
Size: Custom	Document Description: SERIAL POR/PS2
Rev: 1.2	
Date: Wednesday, December 12, 2018	Sheet 32 of 60

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

GPIO可由BIOS 切換 PWM/DCMODE



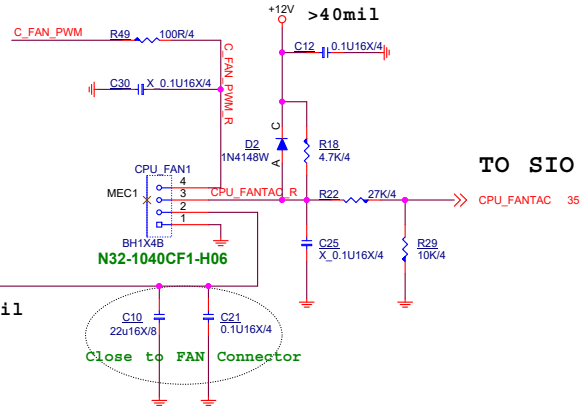


CPUFAN_PWR>40mil

GPIO Control

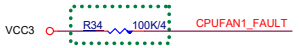
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428



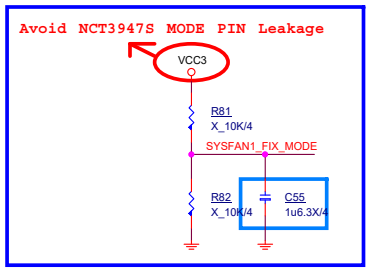
MICRO-STAR INT'L CO.,LTD

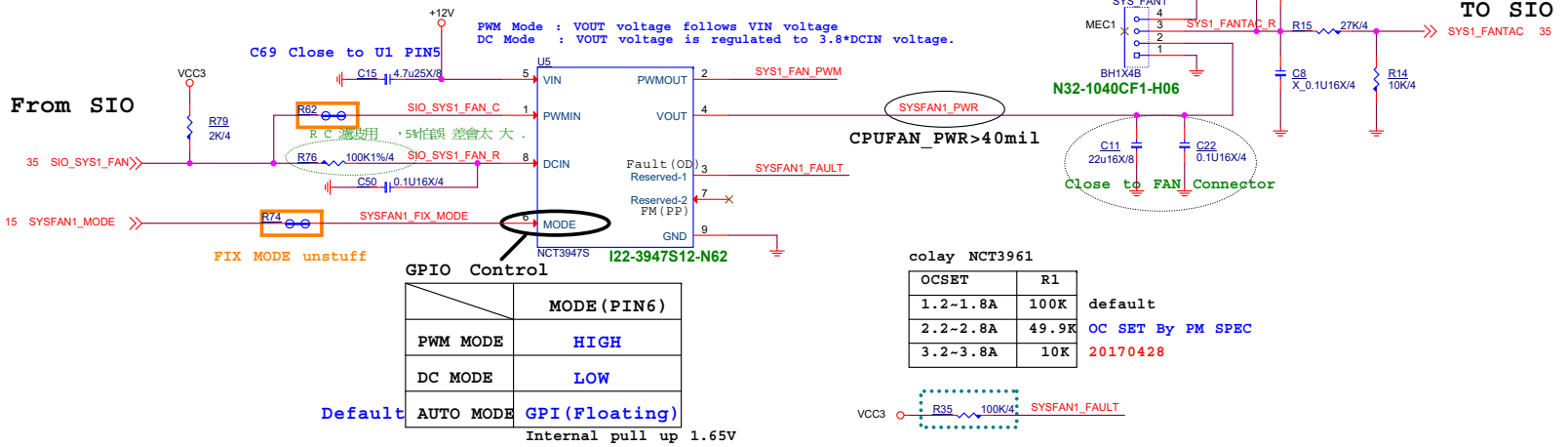
MS-7C08..

Size: Custom | Document Description: CPU FAN | Rev: 1.2

Date: Wednesday, December 12, 2018 | Sheet 33 of 60

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE





GPIO Control

	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internal pull up 1.65V

colay NCT3961

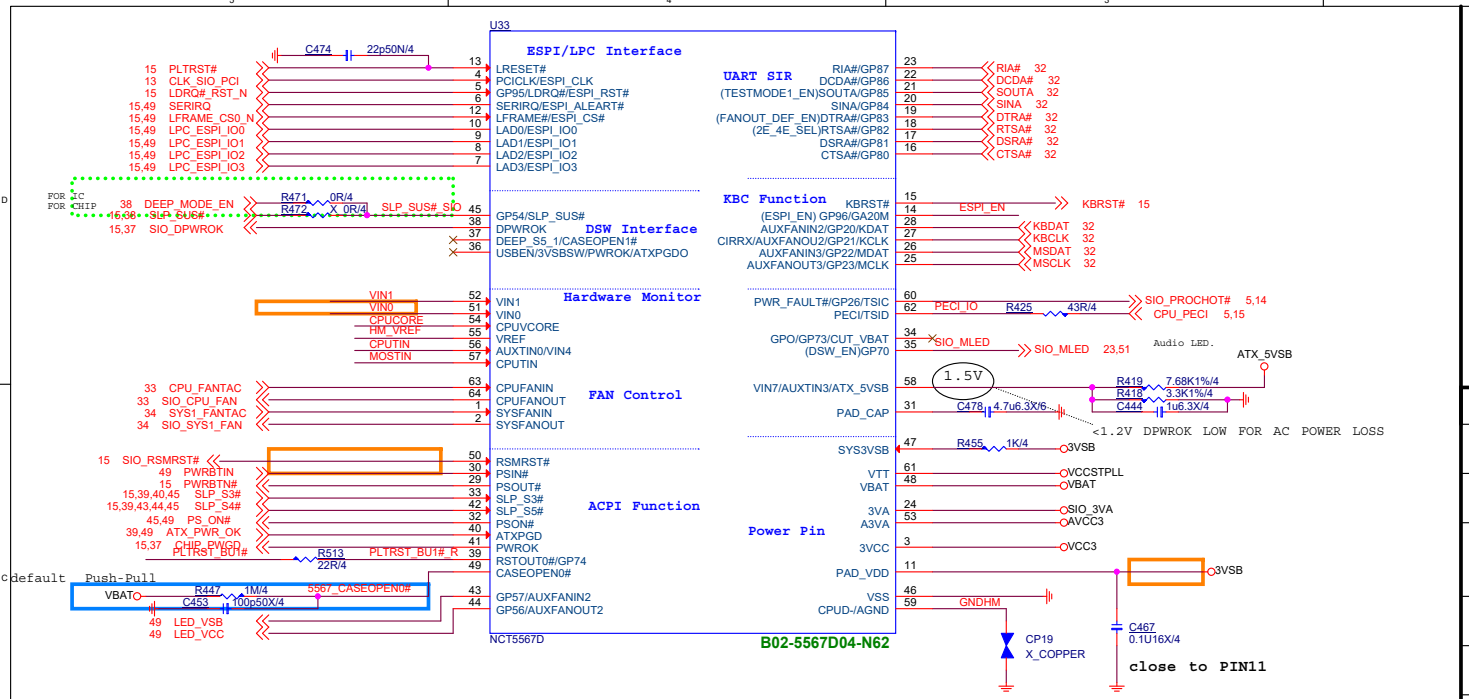
OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

MICRO-STAR INT'L CO.,LTD

MS-7C08..

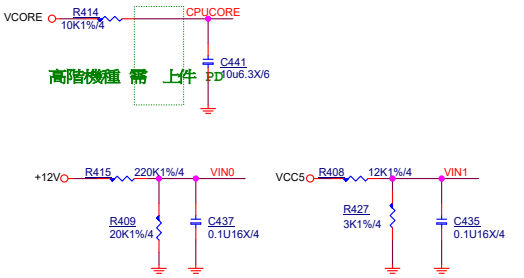
Size: Custom | Document Description: SYSTEM FAN | Rev: 1.2

Date: Wednesday, December 12, 2018 | Sheet 34 of 60

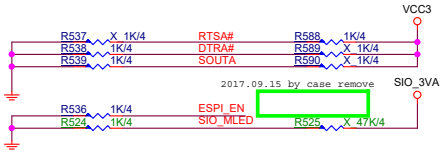


NCT7718W

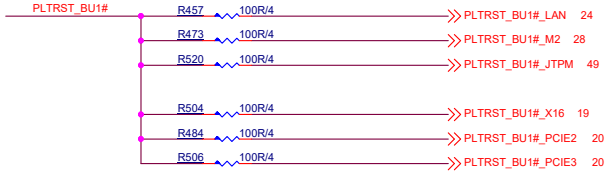
HW Monitor - Voltage



PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN



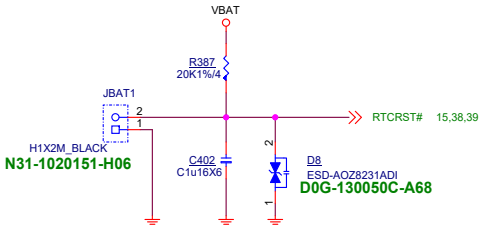
need near SIO



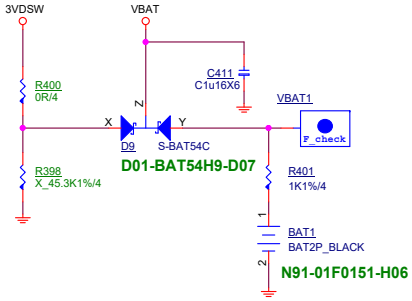
Remove 5567 colay 5565.

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: SIO NCT6797-1	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 35 of 60	

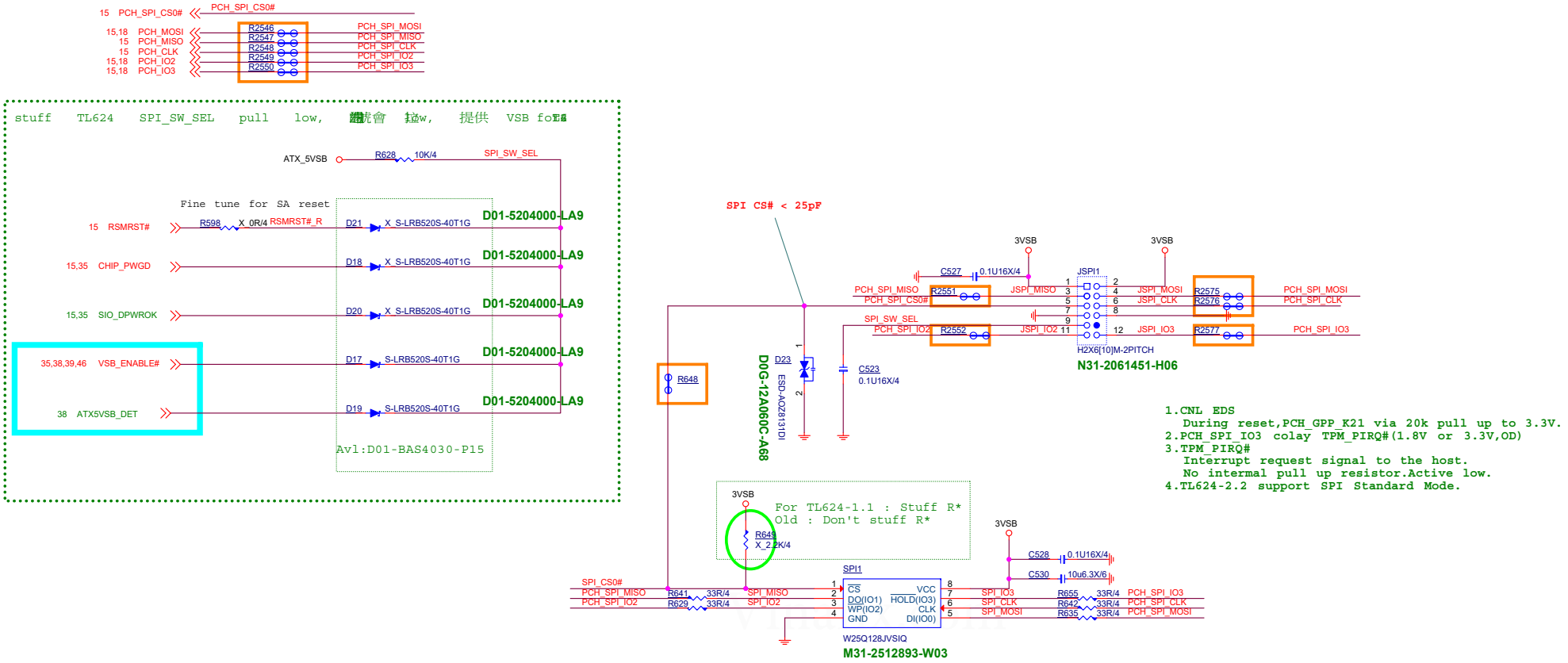
Cut VBAT



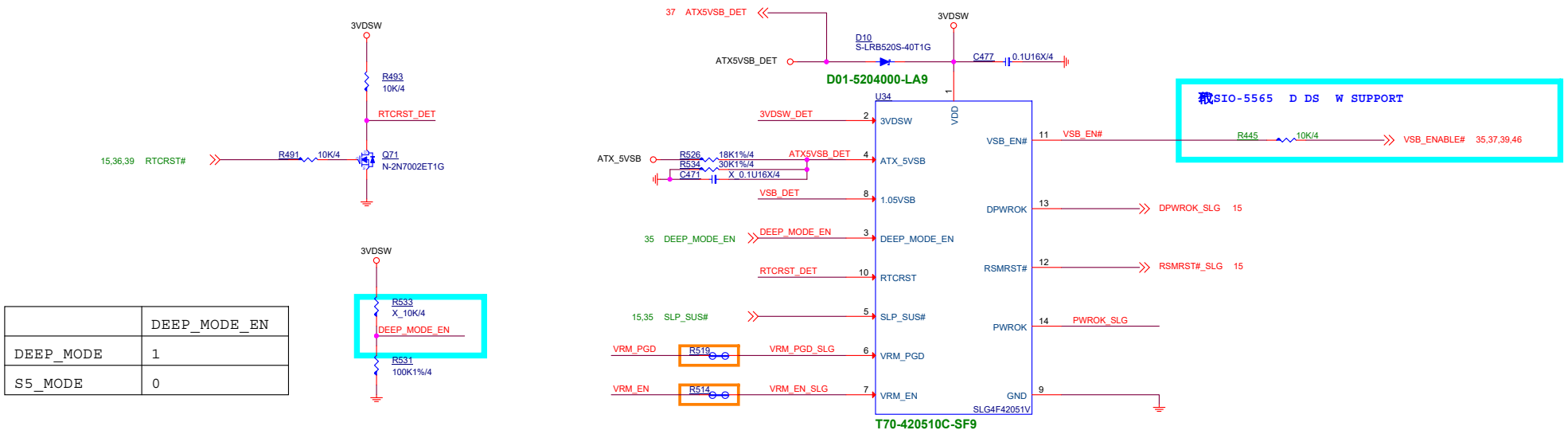
VBAT



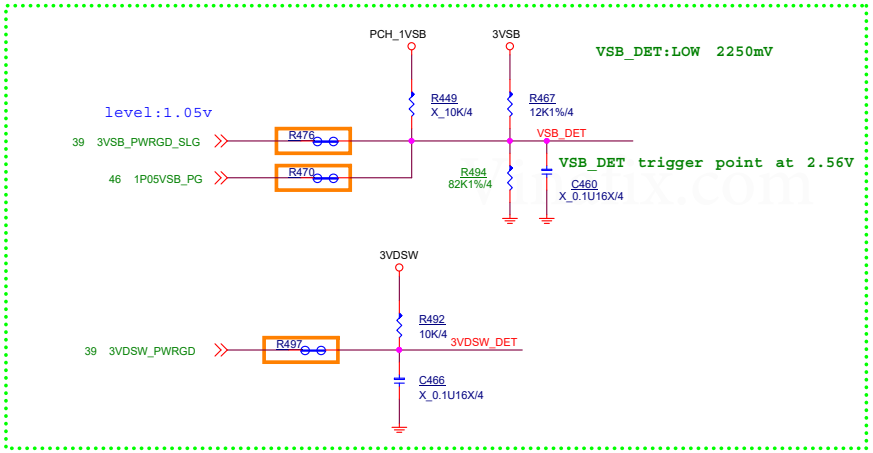
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: CUT VBAT circuit	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 36 of 60	

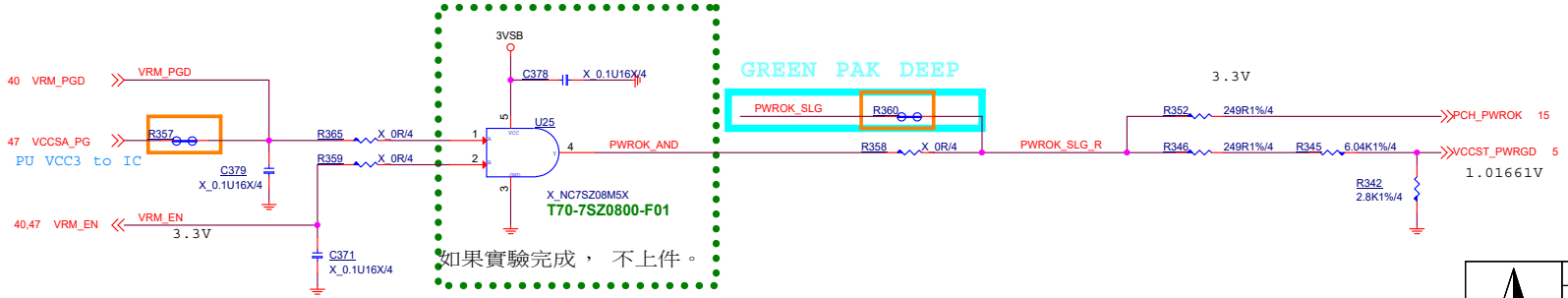


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: BIOS ROM	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 37 of 60	



	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0





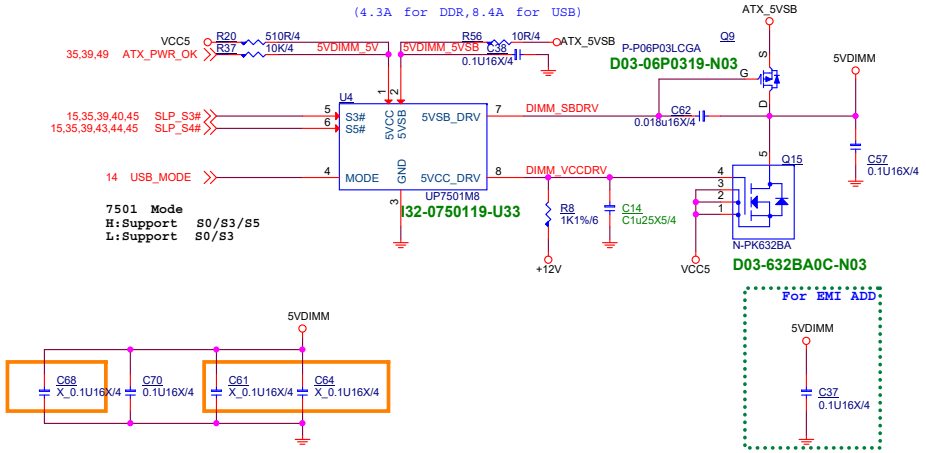
MICRO-STAR INT'L CO.,LTD

MS-7C08..

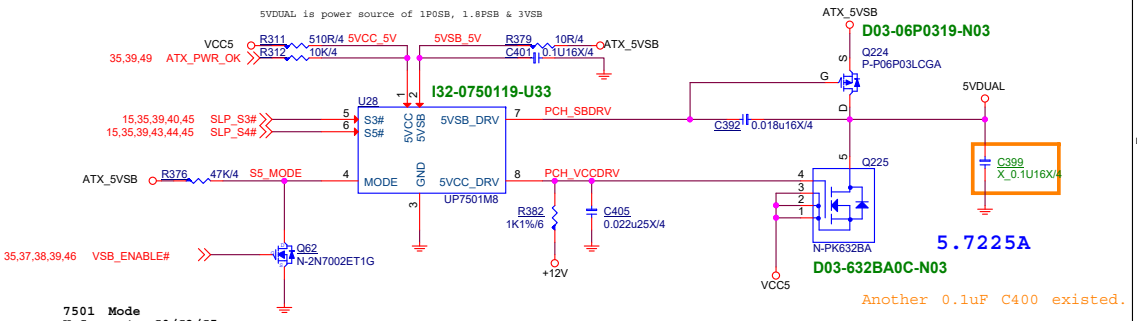
Size	Document Description	Rev
Custom	GREEN PAK DEEP	1.2

Date: Wednesday, December 12, 2018 Sheet 38 of 60

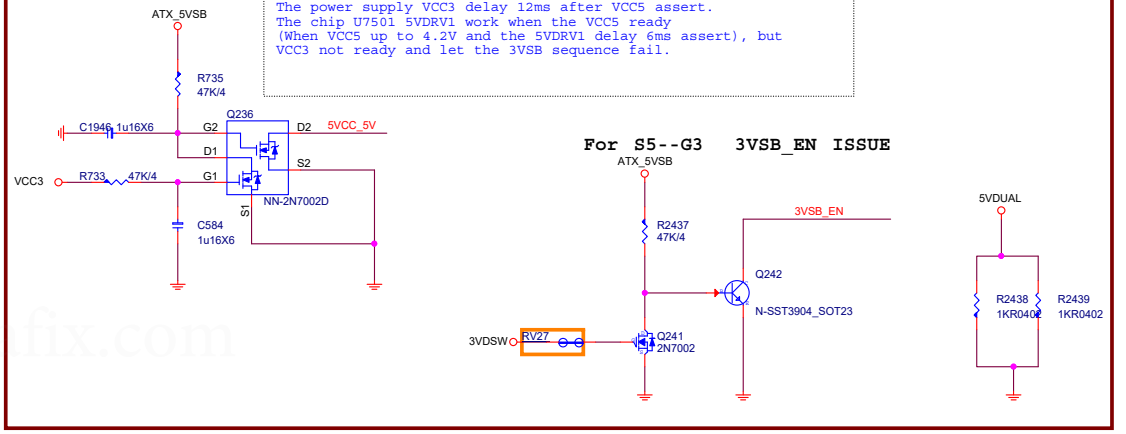
5VDIMM@5V/11.3075A



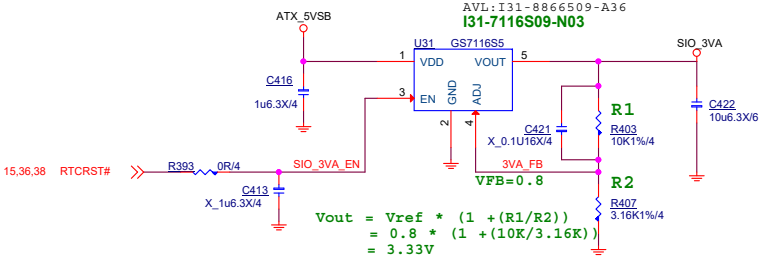
5VDUAL@5V/5.7225A



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

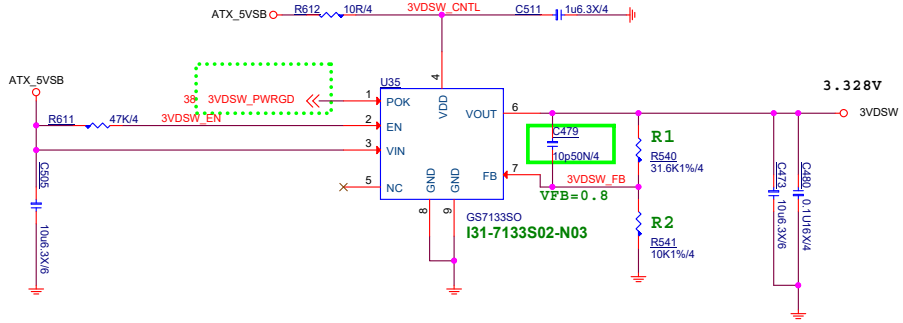


SIO_3VA@3.3V/20mA



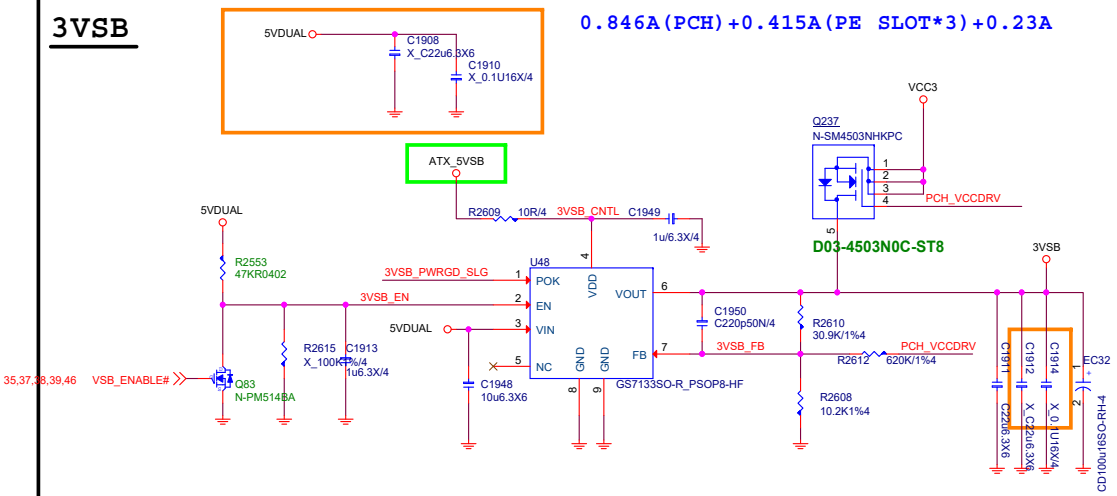
3VDSW@3.3V/0.3A

Intel Lan
不能用小顆 C ，因為LAN瞬間電流會很大。
113mA(PCH)+0.6mA(RTC)+200mA(LAN-I219)+SIO



3VSB

0.846A(PCH)+0.415A(PE SLOT*3)+0.23A



MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: ACPI CONTROLLER	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 39 of 60	

VCORE Iccmax 138A,TDC 91A.OCP 160A
VGT Iccmax 48A,TDC 30A.OCP 60A

Sensor POR min 2V

SLP_S3# assertion to IMVP VRM_EN deassertion max:1us

0LL_EN:
Zero load-line function setting.
Connect to 5V can enable 0LL function.

VOFS=0.4*(VOFSM-1.7)
-500mV<VOFS<590mV
Disable offset function,OFSM Pin to GND.

VCORE Default VR_HOT 120℃ , ALERT 110 ℃

ALERT 97℃ .

I32-3607B0C-R11

Iccmax:138A,OCP:120%*Iccmax,QR Trigger Level PS0/PS1 30/15mV,DVID 61mV

Iccmax:45A,OCP:120%*Iccmax,QR Trigger Level PS0/PS1 15/10mV,DVID 61mV

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 control ICCMAX,OCP setting
SETA2 control Internal compensation

close to phasel CHOKE

close to phasel CHOKE

R2 Default 8.53K

R1 Default 274K

2017.09.26 For default thermal alert# 97 ℃

Jumper insert,VCORE/VGT 0.8V.

Vinafix.com

VCORE Thermal Protection Table

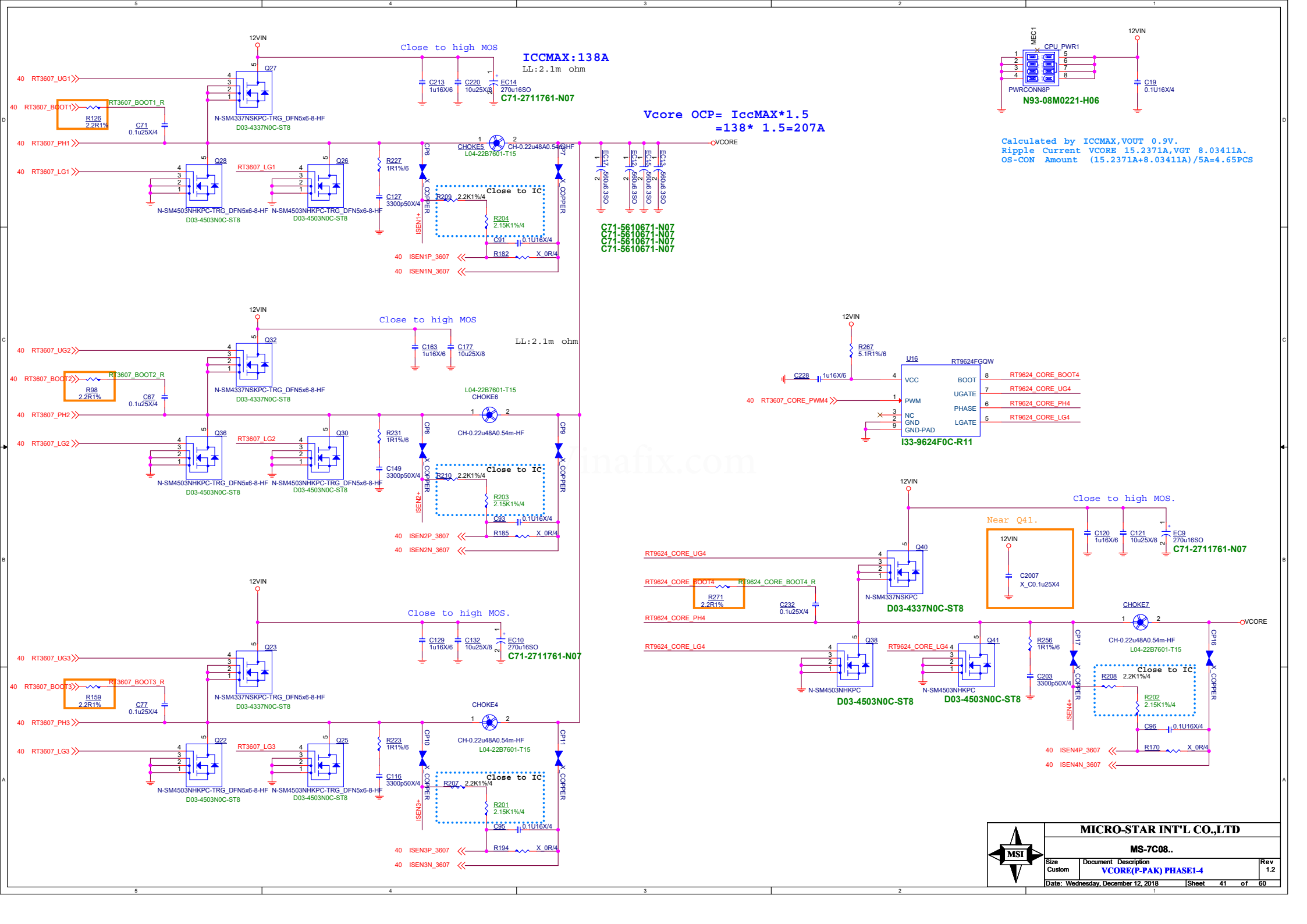
GPP_D16	R1	R2	Thermal Alert#	VR_HOT#	SIO_PROCHOT#
GPI(1)	112.55K	11.3K	106℃	NC	115℃
GPI(0) Default	274K	8.53K	97℃	NC	115℃

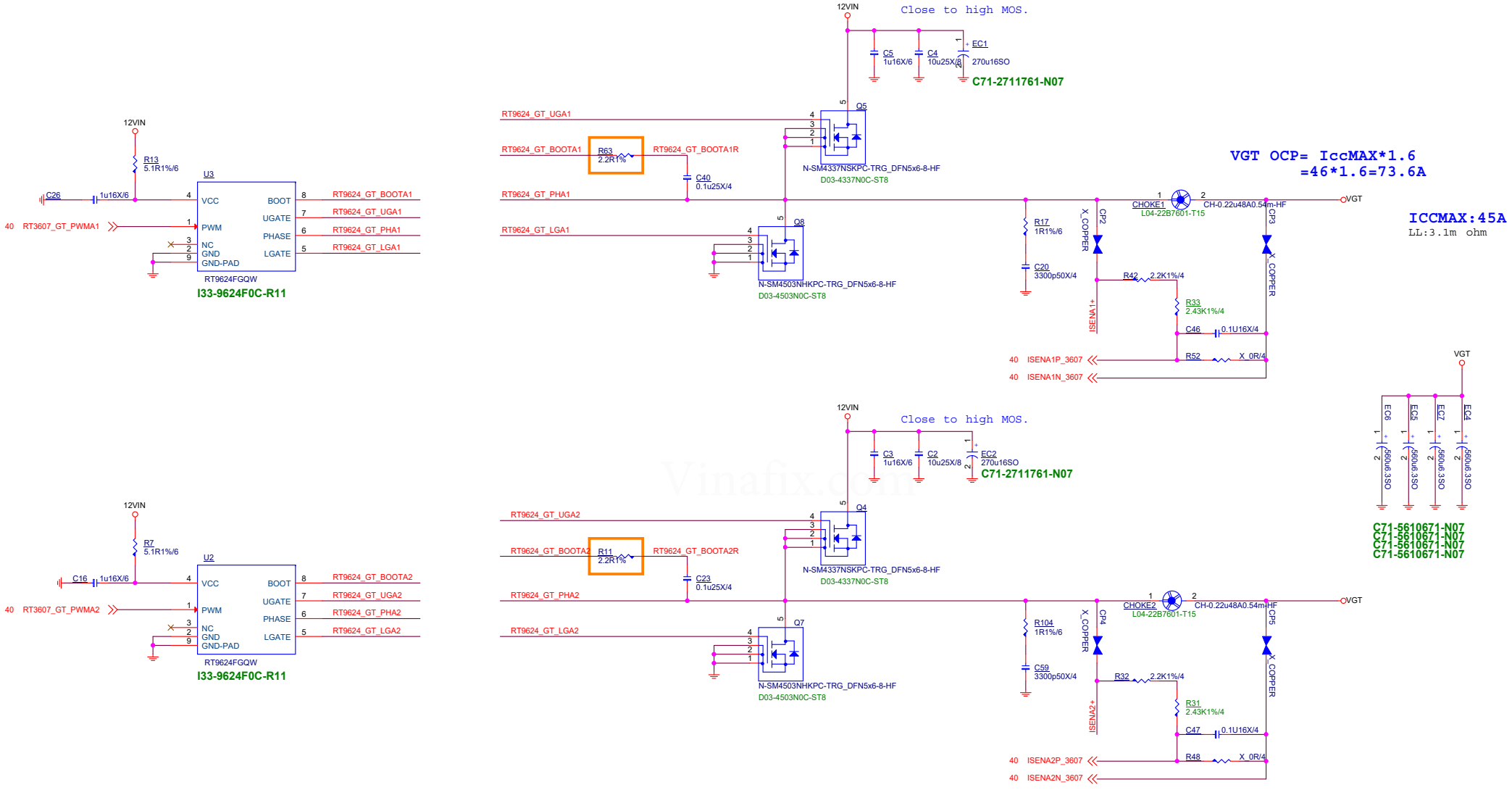
MICRO-STAR INT'L CO.,LTD

MS-7C08..

Size Custom | Document Description PWM-RT3607BC | Rev 1.2

Date: Wednesday, December 12, 2018 | Sheet 40 of 60


ICCMAX:138A
LL:2.1m ohm
Vcore OCP= IccMAX*1.5
=138* 1.5=207A
Calculated by ICCMAX,VOUT 0.9V.
Ripple Current VCORE 15.2371A,VGT 8.03411A.
OS-CON Amount (15.2371A+8.03411A)/5A=4.65PCS
Close to high MOS
Close to high MOS.
Close to IC
Near Q41.
12VIN
VCORE
C71-2711761-N07
C71-5610671-N07
N93-08M0221-H06
I33-9624F0C-R11
D03-4337N0C-ST8
D03-4503N0C-ST8
MICRO-STAR INT'L CO.,LTD
MS-7C08..
VCORE(P-PAK) PHASE1-4
Date: Wednesday, December 12, 2018
Sheet 41 of 60



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 42 of 60	

VCC_DDR@1.2V/11.525A

4503 Rdson
10V 2.5~3mohm
4.5V 3.9~5.1mohm

DDR4_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU
10A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

11.64A

D03-632BA0C-N03 3.9~5.1mohm/4.5V
Current limit= 174K*5uA/3.9mohm)= 22.3A
Current limit= 174K*5uA/5.1mohm)=17.1A
OUTPUT CHOCKE Isat=32A
Vcs=174K*5uA=0.87V(Spec:0.4V~3V)

Vout=0.75V/1.65K*(1.65K+1K)=1.204V

NCT3933 source 10uA
Vout=[VREF*(1+R171/R153)]+10uA*R171
=0.75V*(1+1K/1.65K)+10uA*1K=1.204V+0.010V=1.215V

NCT3933 sink 10uA
Vout=[VREF*(1+R171/R153)]-10uA*R171
=0.75V*(1+1K/1.69K)-10uA*1K=1.204V-0.010V=1.195V

Iin=IOCP*Vout/08/Vin
=22.3A*1.2V/0.8/5V=6.69A

0R/0603/0.1W/50mOhm

VID	Reference Voltage (V)
H	0.675
L	0.75

R11-0000013-W08
R11-0000013-W08
R11-0000013-W08

C71-5610671-N07

Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=11.525 * 0.427
= 4.921A

f:426.57KHz

VFB=0.75

R1

R2

VTT

Current Limit 2.6A

I32-8231A0C-R11

Vout = Vref * (1 +(R1/R2))
= 0.75 * (1 +(1K/1.65K))
= 1.204V

From SIO pin 6,PU SIO.

SLP_S4# de-assertion to
VDDQ ramp down start

L=tON*(VIN-VDDQ)/(LIR*ILOAD(MAX))
tON=636.4456ns
LIR:20%~40%
L:0.63uH~1.27uH.

MAX:11.525A
1.2V

L04-82B7211-L65

C71-5610671-N07

0.1uFx1 per dimm

VPP ramp down after VDDQ ramp down

MS-7981 Add. Package C-states above C8 function

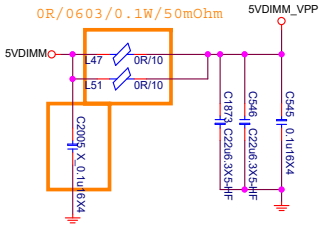
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

I34-3933U09-N62

MICRO-STAR INT'L CO.,LTD	
MS-7C08..	
Size: Custom	Document Description: DDR-RT8231
Date: Wednesday, December 12, 2018	Sheet 43 of 60
	Rev: 1.2

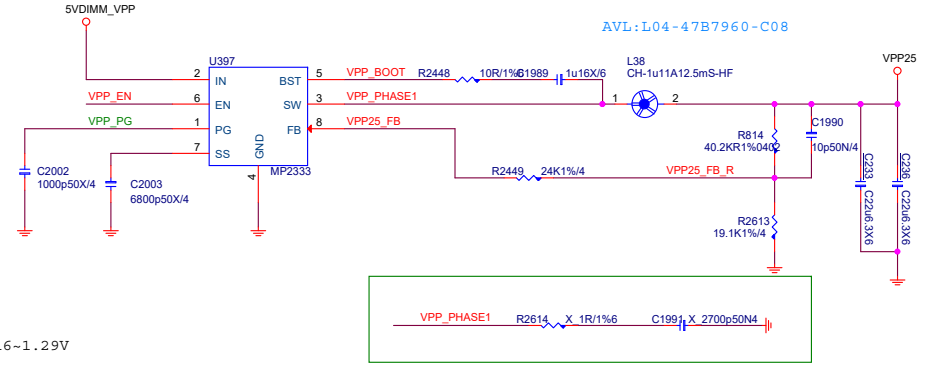
VPP25 @2.5V/2A



Current Limit 4A.
CHOKE Isat=6A

Iin=4A*2.5V/0.8/5V=2.5A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=1A



ENABLE HIGH:1.16~1.29V

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14µA.

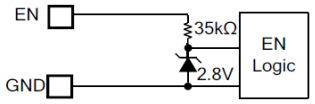
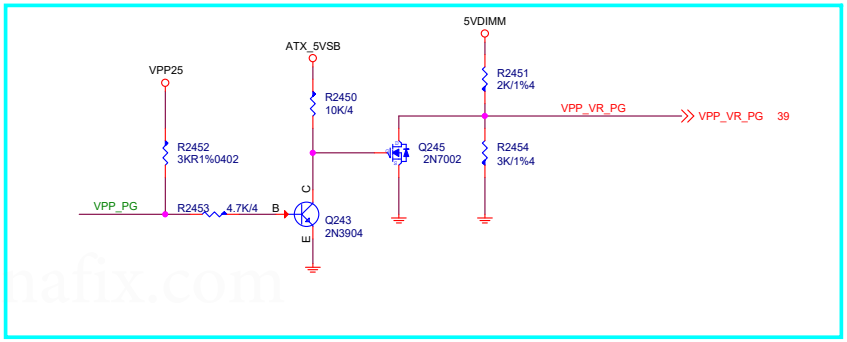
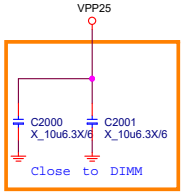
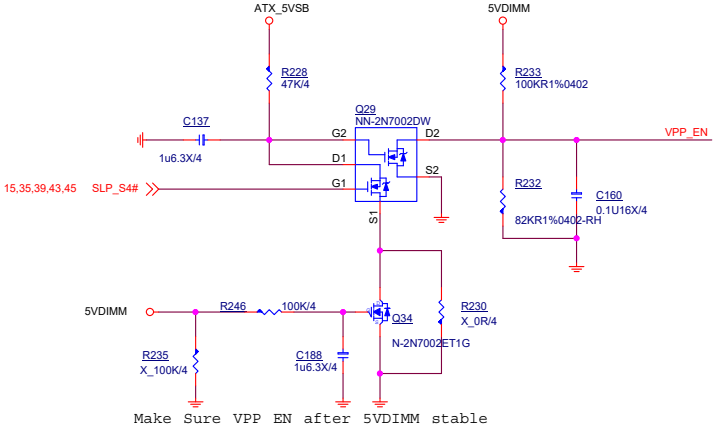


Figure 2: Zener Diode between EN and GND







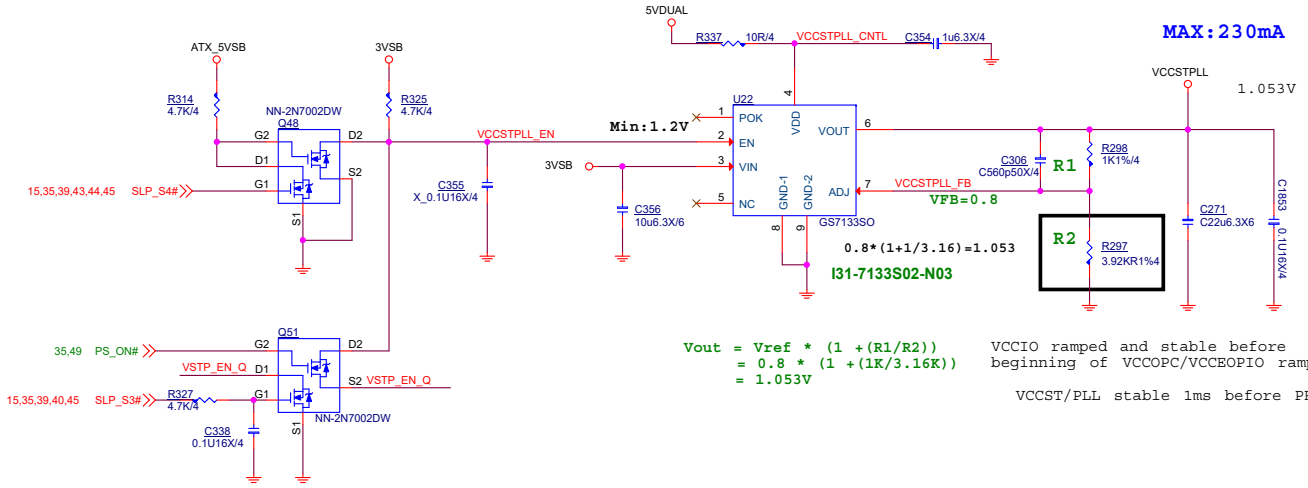
ENABLE HIGH:1.2V

Make Sure VPP EN after 5VDIMM stable

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: DDR-MP2143-VPP25	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 44 of 60	

VCCSTPLL@1.05V/230mA

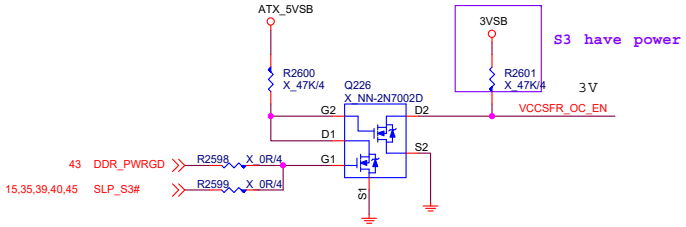
VCCSTPLL change 1.05V to 1V



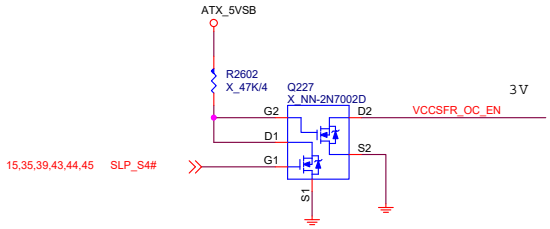
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.053V

VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD



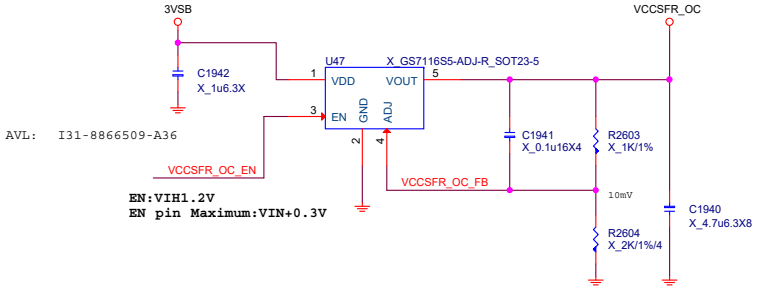
2018.06.19 unstuff,spec stuff VCC_DDR



from NCT3933

VCCPLL_OC

1.2V; 110mA AJ9



EN:VIH1.2V
EN pin Maximum:VIN+0.3V

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: VCCSTPLL&VCCSFR_OC	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 45 of 60	

PCH_1VSB@1V/8.72A

4503 Rdson
10V 2.5~3mohm
4.5V 3.9~5.1mohm

Current limit= 6.65K*10uA/3.9mohm)=17.05A
Current limit= 6.65K*10uA/5.1mohm)=13.04A
CHOKE Isat=18A
From CHOKE I-L Curve,when I=25A, L=0.6uH.

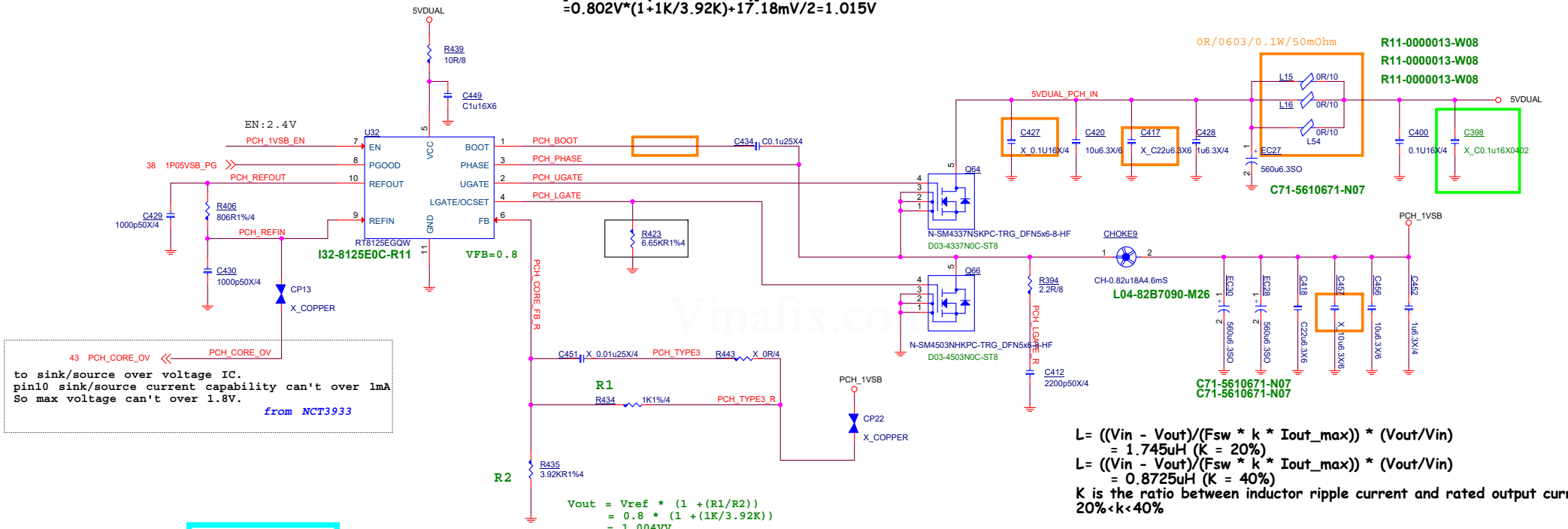
Default Vout=1V

NCT3933 sink 10uA
VREFIN =VREFOUT-10uA*R406=796mV-8mV=788mV
Vout=[VREFOUT*(1+R434/R435)]+ΔVout/2
=0.788V*(1+1K/3.92K)+17.18mV/2=0.997V

NCT3933 source 10uA
VREFIN =VREFOUT+10uA*R407=796mV+8mV=804mV
Vout=[VREFOUT*(1+R434/R435)]+ΔVout/2
=0.802V*(1+1K/3.92K)+17.18mV/2=1.015V

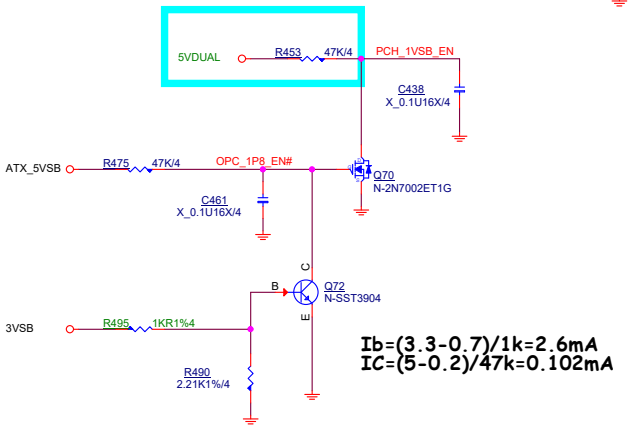
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=8.72 * 0.276
=2.407A

Iin=IOCP*Vout/08/Vin
=17.05A*1.V/0.8/5V=4.2625A

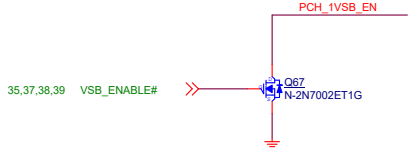


L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 1.745uH (K = 20%)
L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8725uH (K = 40%)
K is the ratio between inductor ripple current and rated output current.
20%<k<40%

ΔVout_ESR = ΔIL*ESR =40%*8.72A*4mOhm=13.952mV
ΔVout_C = ΔIL*1/(8*Cout*f_SW) =40%*8.72A/(8*560uF*2*300KHz) =1.3mV
Vout_SAG=ESR*Δ Iout =4mOhm*10.743A=34.88mV



Ib=(3.3-0.7)/1k=2.6mA
IC=(5-0.2)/47k=0.102mA



MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: PCH Core power	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 46 of 60	

VCCSA@1.05V/11.1A

4503 Rdson
10V 2.5~3mohm
4.5V 3.9~5.1mohm

Current limit= 5.1K*10uA/2.5mohm)=20.4A
Current limit= 5.1K*10uA/3mohm)=17A
CHOKE Isat=17A
From CHOKE I-L Curve,when I=25A, L=0.6uH.

Width:>20mil

+12V R324 10R/6 VCCSA_VCC C347 1u16X/6

VCC3 R335 10K/4

EN:VIH2.4V
EN pin Maximum:6.5V

U24 RT8125EGQW
I32-8125E0C-R11

VCCSA_EN 7 EN
8 PGOOD
SA_REFOUT 10 REFOUT
9 REFIN
SA_REFIN
VCC 5
GND 11
BOOT 1 SA_BOOT1 C328 C0.1u25X4
PHASE 3 SA_PH1
UGATE 2 SA_UG1
LGATE/OCSET 4 SA_LG1
FB 6 SA_FB

38 VCCSA_PG

C348 1000p50X/4
R329 768R1%/4
C361 1000p50X/4

FB:0.8V

R1 R331 1K1%/4 VCCSA_SENSE_R
C362 X_100p50N/4
R2 R332 3.16K1%/4

VCCSA R330 10R1%/4
CP30 X_COPPER VCCSA_SENSE 5

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.053V

Vout=[VREFOUT*(1+R331/R332)]+ΔVout/2
=0.794V*(1+1K/3.16K)+17.76mV/2=1.053V
VREFOUT=0.794V

+12V C318 X_0.1U16X/4

+12V L52 CH-0.47u5A21mS-HF

Iin=IOCP*Vout/08/Vin
=20.4A*1.05V/0.8/12V=2.23A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 3.13649A

+12V_SA
C351 1u16X/6
C331 C10u25X8
C334 22u16X/8
C333 22u16X/8
C335 X_0.1U16X/4
C350 X_C0.1u25X4

SA_UG1 Q50 N-SM4337NSKPC-TRG_DFN5x6-8-HF D03-4337N0C-ST8

VCCSA 13 A

CHOKE8 MAX:11.1A
CH-1.0u14A5.5mS
L04-01073F0-M26

1.05V,11.1A VCCSA

SA_PH1
R2471 2.2R/8
SA_PH1_R
snubber C1902 3300p50X/4
0908 stuff Snubber

C267 1u6.3X/4
C269 C22u6.3X6
C265 C22u6.3X6
EC21 560u6.3SO
EC20 560u6.3SO
C71-5610671-N07

SA_LG1 Q45 N-SM4503NHKPC-TRG_DFN5x6-8-HF D03-4503N0C-ST8
R320 5.1K1%/4

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 1.4386uH (K = 20%)
L= ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7193uH (K = 40%)
K is the ratio between inductor ripple current and rated output current.
20%<k<40%

ATX_5VSB R343 47K/4
+12V R334 26.1K1%/4

C364 0.1U16X/4 VCCSA_EN_G2 Q53 NN-2N7002DW
G2 D2
D1
G1 S2
S1
38,40 VRM_EN R344 0R/4 VCCSA_EN_G1
48 VCCIO_EN R341 X_0R/4

VCCSA_EN 3.3V
R339 10K1%/4
C360 0.1U16X/4

EN:VIH2.4V
EN pin Maximum:6.5V

VCCSA_EN
40,48 SLP_S3_CTRL Q54 N-2N7002ET1G

SLP_S3# assertion to VR disabled
max:1us

ΔVout_ESR = ΔIL*ESR =40%*11.1A*4mOhm=17.76mV
ΔVout_C = ΔIL*1/(8*Cout*f SW) =40%*11.1A/(8*560uF*2*300KHz) =1.65mV
Vout_SAG=ESR*ΔIout =4mOhm*11.1A=44.4mV

MICRO-STAR INT'L CO.,LTD
MS-7C08..
Size Custom
Document Description VCCSA - POWER NB685GQ
Rev 1.2
Date: Wednesday, December 12, 2018 Sheet 47 of 60

VCCIO@0.95V/6.4A

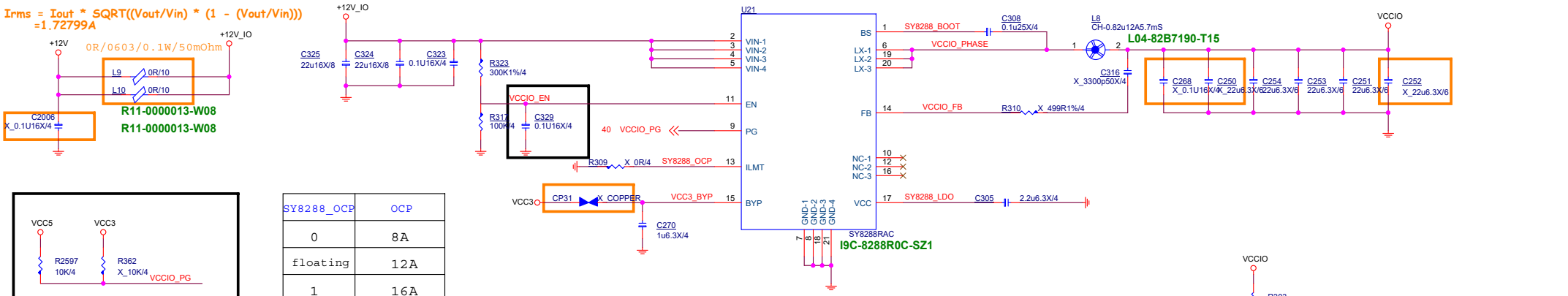
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

Iin=14A*0.95V/0.8/5V=3.325A

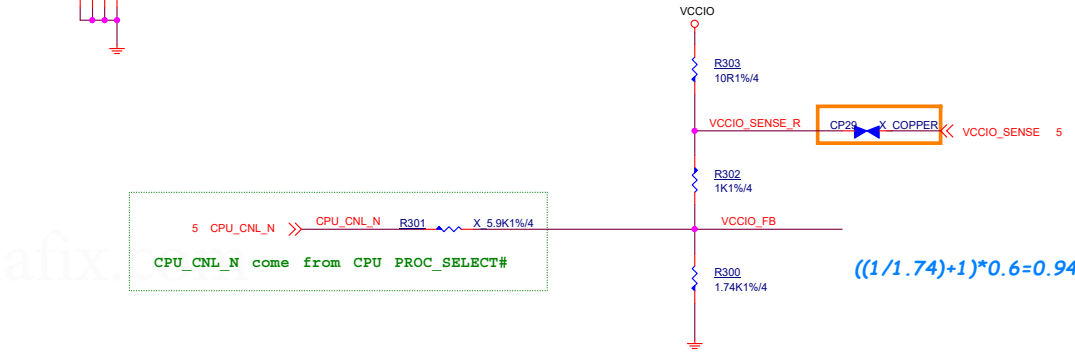
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
=1.72799A

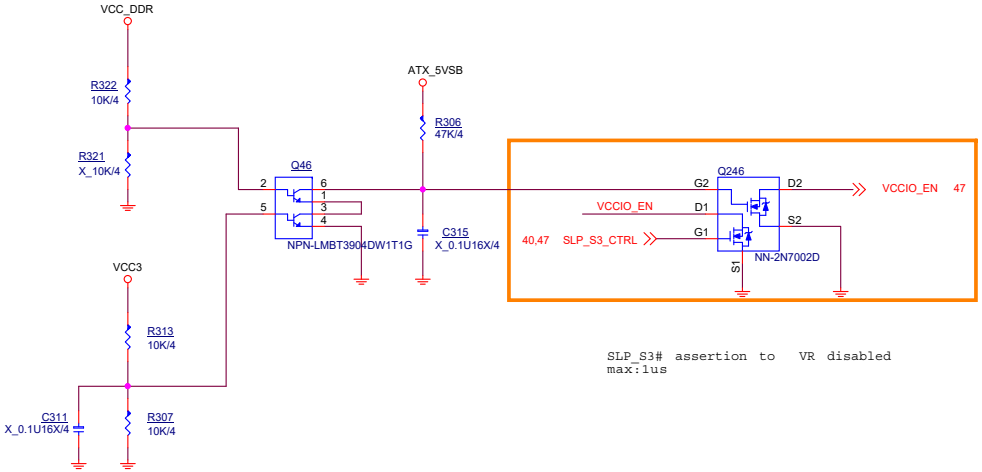
VCCIO 區12A(floating)

MAX:6.4A

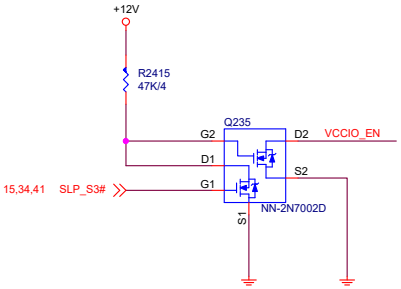


SY8288_OCP	OCP
0	8A
floating	12A
1	16A



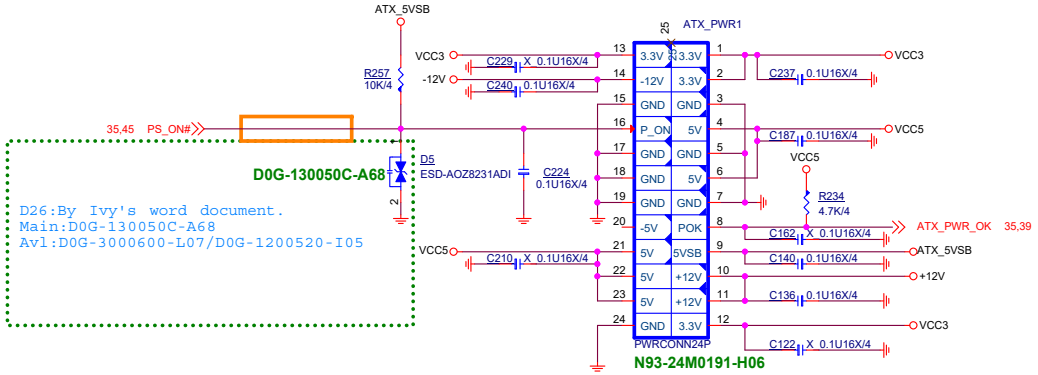


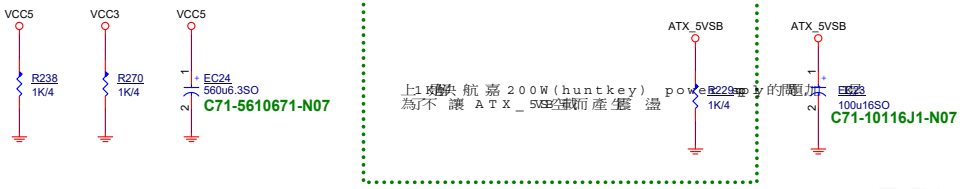
SLP_S3# assertion to VR disabled
max:1us



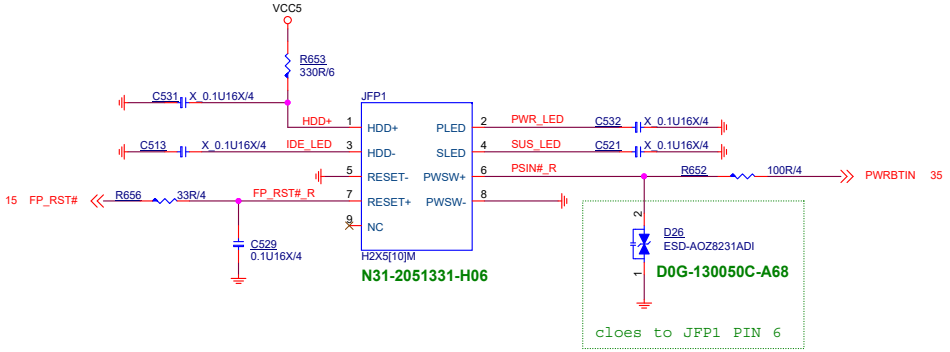
MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: VCCIO - POWER SY8288	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 48 of 60	

ATX POWER CONNECTOR

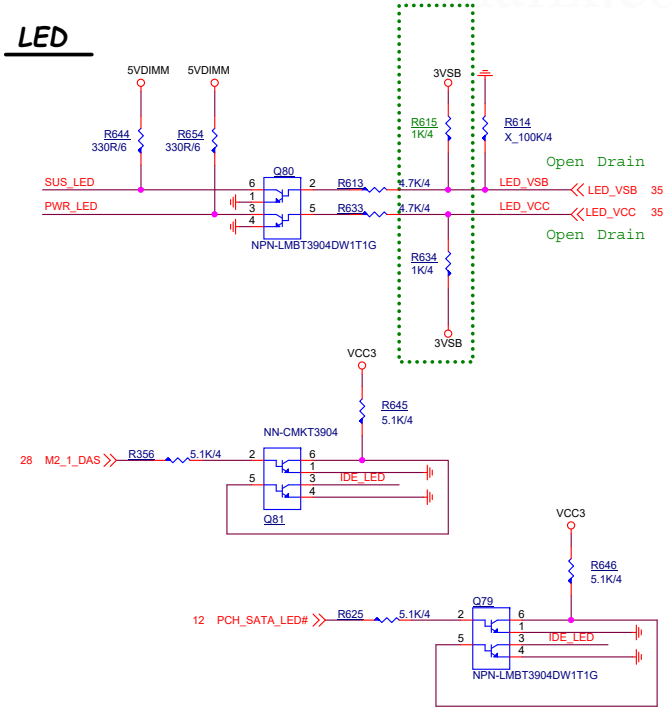




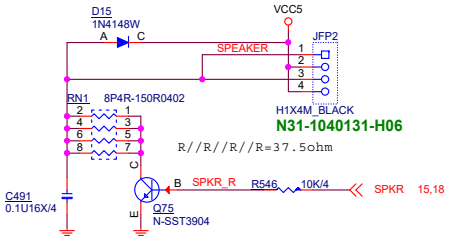
FRONT PANNEL



LED

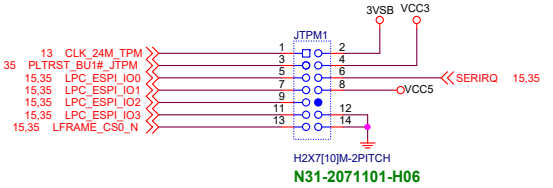


Speaker Pin Header



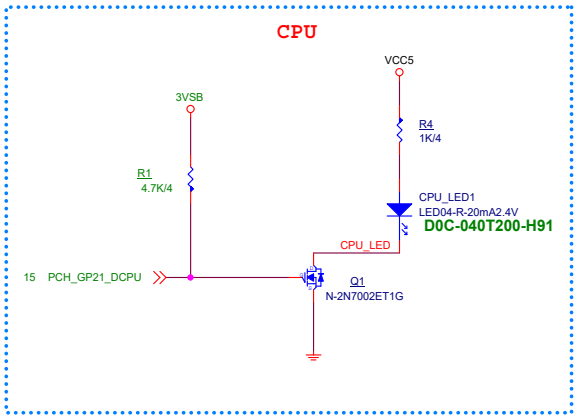
Ib=(5-0.7)/37.5=0.1146mA
IC=(5-0.2)/10k=0.48mA

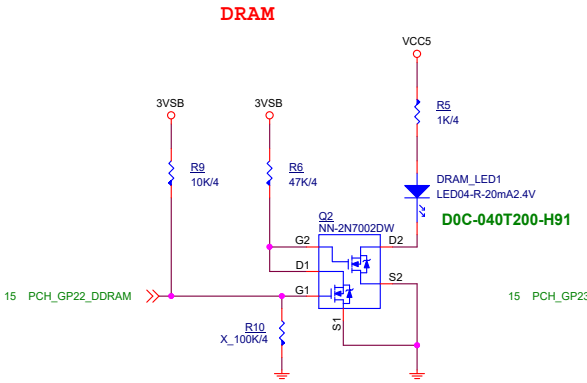
TPM

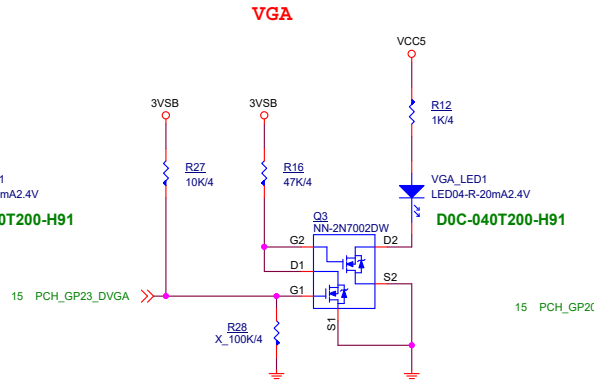


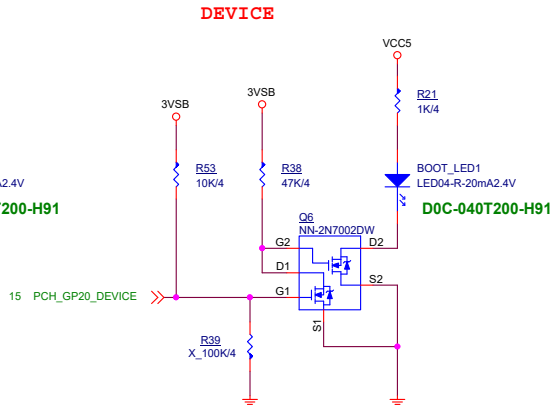
MICRO-STAR INT'L CO.,LTD	
MS-7C08..	
Size: Custom	Document Description: ATX F_Panel/TPM/MSI_LED
Rev: 1.2	
Date: Wednesday, December 12, 2018	Sheet 49 of 60

EZ DEBUG LED









LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

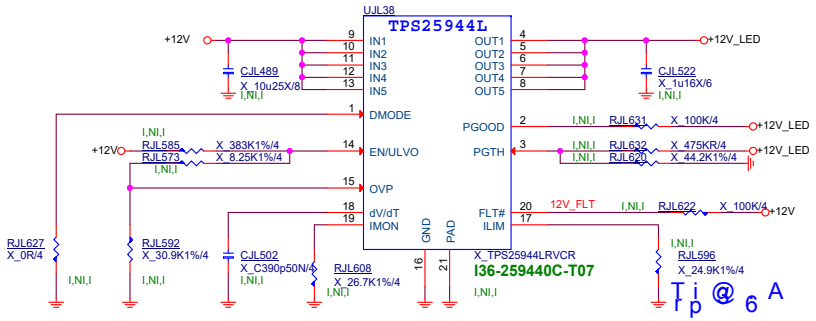
WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

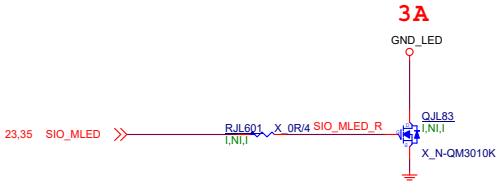
關 機 斷 電 狀 態下 ， 3個LED先 維 持 d e f a ul燈開機 燈：
1. 首 先 進行 CPU check CPU L E D 亮， check PASS 後則 C P U E D滅掉。
2. 接 著 依 序進行M emory /m emor y LED亮 chec k PASS後 則m m or y LED滅 掉 。
3. VGA的 check/VGA LED 亮 ，che ck PA S S後則 VGA L E D 滅 掉。
4. 因 此 最 後 正 常 順 利開機 後 ， 三個燈 都滅掉。
（ 系 統 重 啟 或 其 他 原 因 造成 系 統 重 開機則D的指 燈為 熄）

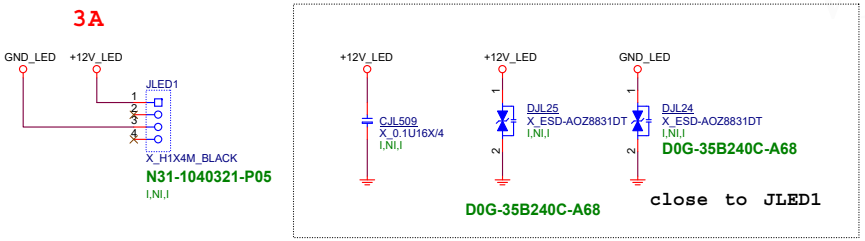
MICRO-STAR INT'L CO.,LTD	
MS-7C08..	
Size: Custom	Document Description: ALL LED Control
Rev: 1.2	
Date: Wednesday, December 12, 2018	Sheet 50 of 60

LED Control by SIO(JLED1)

unstuff







MICRO-STAR INT'L CO.,LTD		
MS-7C08..		
Size: Custom	Document Description: JLED	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 51 of 60	

OPTION BOM PARTS

LAB1

B310
Lable

MKT

G51-M1SPN25-Q13

PCB1

7C08_12

PD0-07C0812-E48

CPU_H1

CPU
鐵 座

CPU_H1

E21-7557050-L06

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C08..	
Size: Custom	Document Description: OPTION BOM	Rev: 1.2
Date: Wednesday, December 12, 2018	Sheet 52 of 60	

BAT1_X1

BAT-BCR2032P

D06-0100101-K26

HDMI_LA1

HDMI LABEL

Y01-RHDMI03-000

BIOS_LA1

AMI

G51-M1SPXXA-A09

LA10

MKT

Y02-MU00170-CFO

Optical Fiducial Marks-120

FM4 FM2 FM1 FM3

X_FM X_FM X_FM X_FM

FM5 FM6 FM7 FM8

X_FM X_FM X_FM X_FM

Simulation

SIM2 SIM1

X_PIN1*2 X_PIN1*2

Mounting Holes

MH1 MH3 MH5

MH2 MH4 MH6

X_MH001

CA23 0.1U16X/4 CA20 0.1U16X/4

HOLES_4S

VPP25 TP_VPP25

VTT_DDR TP_VTT_DDR

5VDIMM TP_5VDIMM

3VSB TP_3VSB

3VDSW TP_3VDSW

VCORE TP_Vcore

VGT TP_VGT

VCCSTPLL TP_VCCSTPLL

VCCIO TP_VCCIO

VCCSA TP_VCCSA

VCC_DDR TP_VCC_DDR

PCH_1VSB TP_PCH_1P05_VSB

SIO_3VA TP_SIO_3VA

Near SIO CHIP

+12V TP_+12V

VCC5 TP_VCC5

PCH_HS1

PCH

1

2

ISO

VCORE1 VCORE F_check

VGT2 VGT F_check

VCC_DDR2 VCC_DDR F_check

VCCSA2 VCCSA F_check

VCCIO2 VCCIO F_check

return path

5VDIMM C230 X_0.1U16X/4

5VDIMM C1938 0.1U16X/4

5VDIMM C1939 0.1U16X/4

+12V C383 X_0.1U16X/4

+12V C339 X_0.1U16X/4

+12V C2009 X_0.1U16X/4

For M2 reference +12V USE please close to under M2

VCCSA C310 X_0.1U16X/4

for moat use

5VDIMM C1943 0.1U16X/4

3VSB C1944 X_0.1U16X/4

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Size: Custom

Document Description: Manual Parts

Rev: 1.2

Date: Wednesday, December 12, 2018

Sheet 53 of 60