COMPAL CONFIDENTIAL

MODEL NAME : DDP80

PCB NO : LA-F711P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge MLK 15 UMA

Cof f ee Lake H

2018-01-11

REV : 0.5 (X02)

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESD Component
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
XDP@ : XDP Component
CONN@ : Connector Component
eSPI@ : eSPI interface
LPC@ : LPC interface
15U@ : Lat i t ude c conf i
15P@ : Precision conf i g
DS3@ : Deep sleep support
NDS3@ : non Deep sleep support

MB PCB

Part Number	Description
DA8001D0000	PCB 26H LA-F711P REV0 MB UMA 1

Layout Dell logo

REV: X02
PWB: GXXF6

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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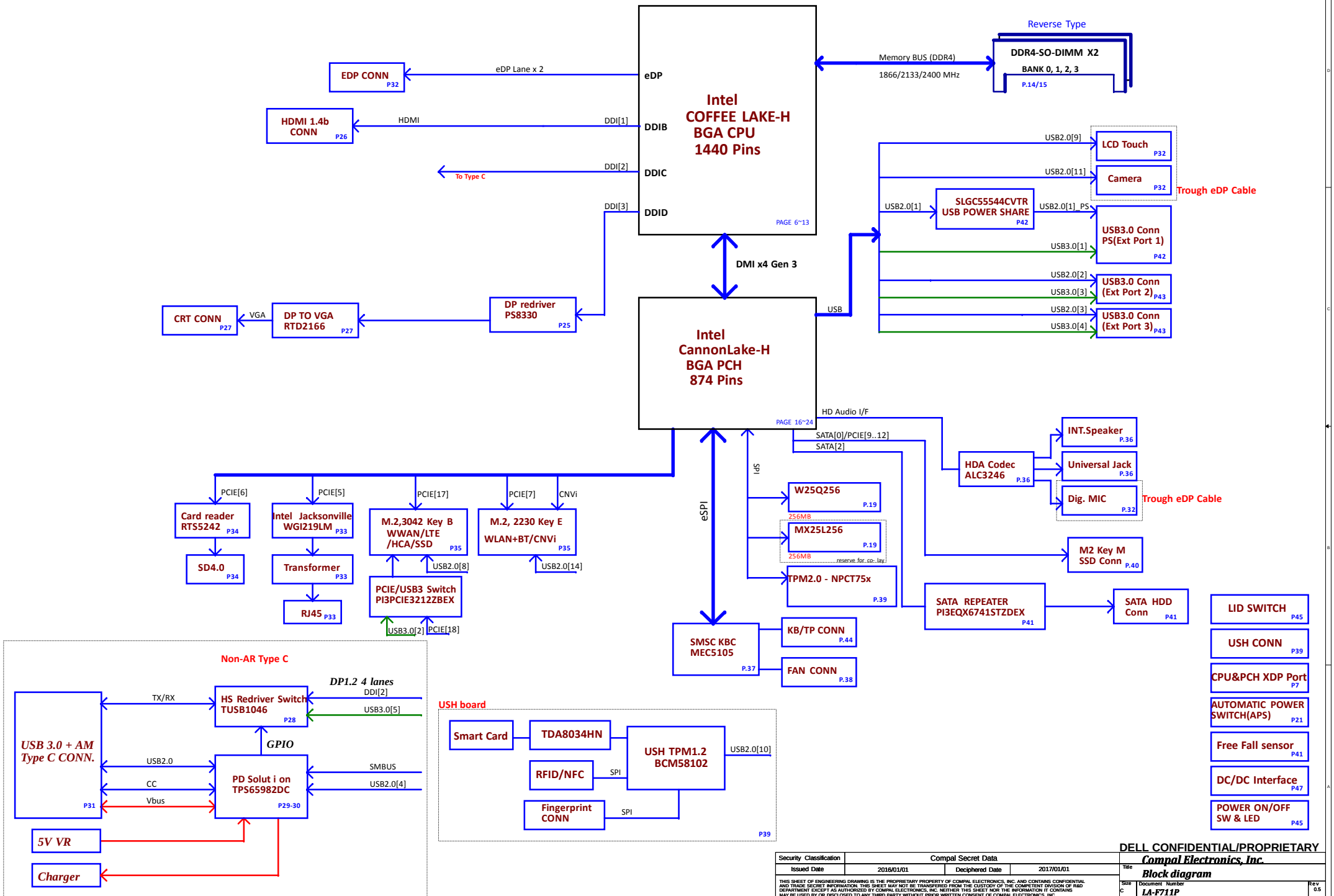
Title: Cover Sheet

Size: A | Document Number: LA-F711P | Rev: 0.5

Date: Thursday, January 18, 2018 | Sheet 1 of 63

Breckenridge MLK 15 UMA non-TBT Block Diagram



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Title: Block diagram			
Size: C	Document Number: LA-F711P		Rev: 0.5
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

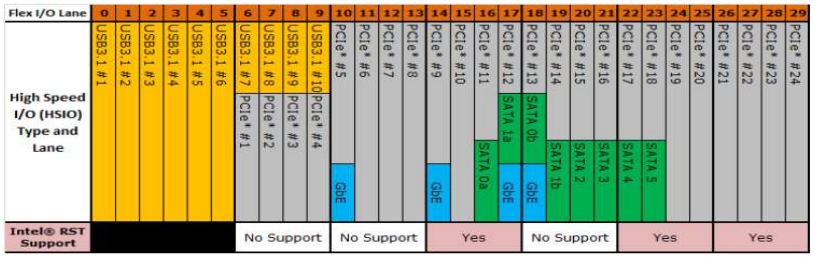
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->REAR
USB3.0-5				JUSBC1-->TypeC
USB3.0-6				NA
USB3.0-7		PCIE-1		NA
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-0A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->Lef t
3	JUSB3-->Rear
4	Type C
5	NA
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO

VIDEO	DESTINATION
eDP	LCD
DDI-B	JHDMI1
DDI-C	Type-C
DDI-D	MB VGA

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
3	Sig 1		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	8.90
4	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
5	Sig2		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	8.20
6	Sig3		Copper foil	1oz	1.35
		3.6	Core	4mil	4.00
7	GND2		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)			47.2		46.60000
					1.18364



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Title: Port Assignment

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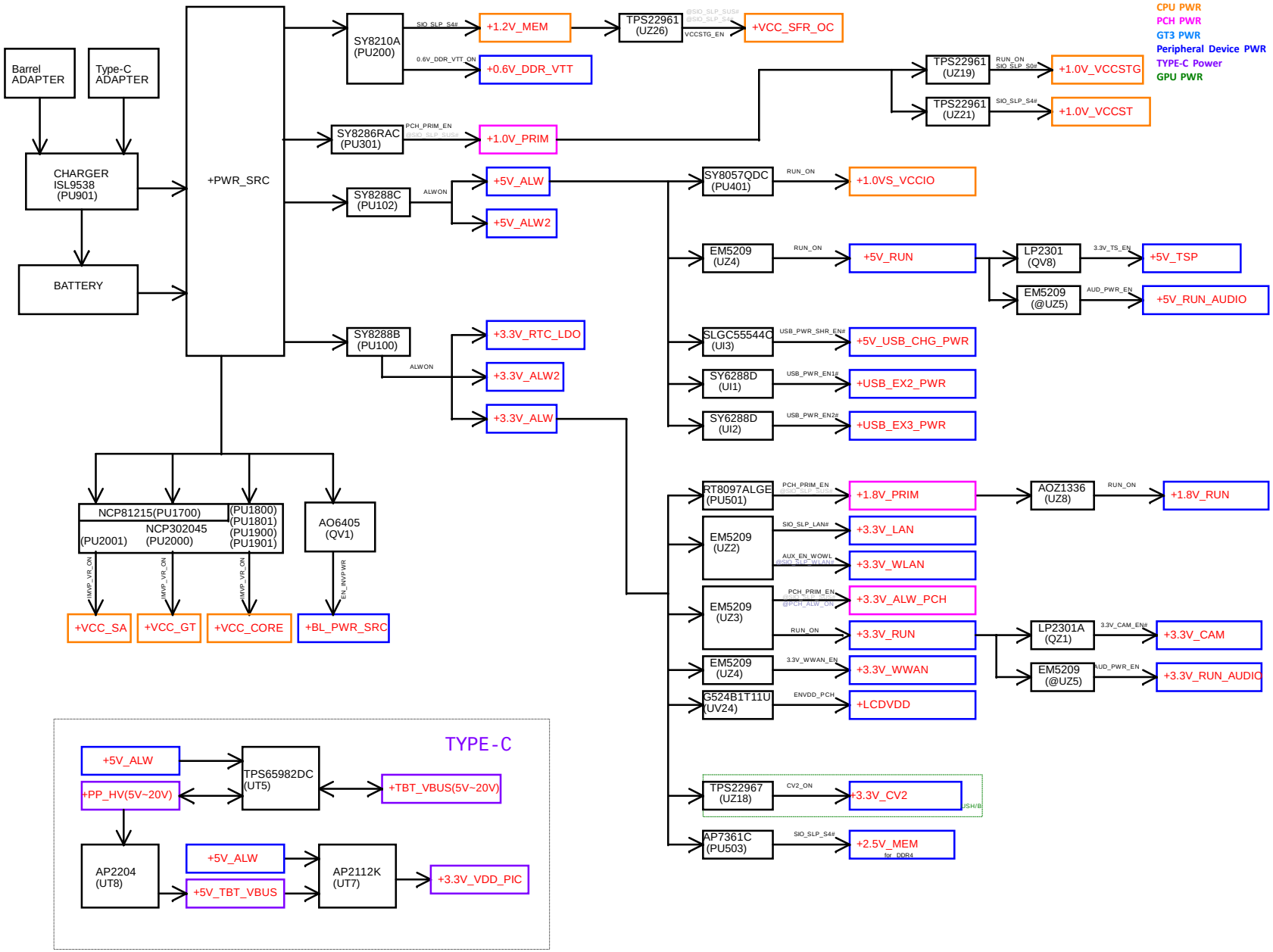

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Compal Electronics, Inc.

Title: Power Rails

Size	Document Number	Rev
C	LA-F711P	0.5

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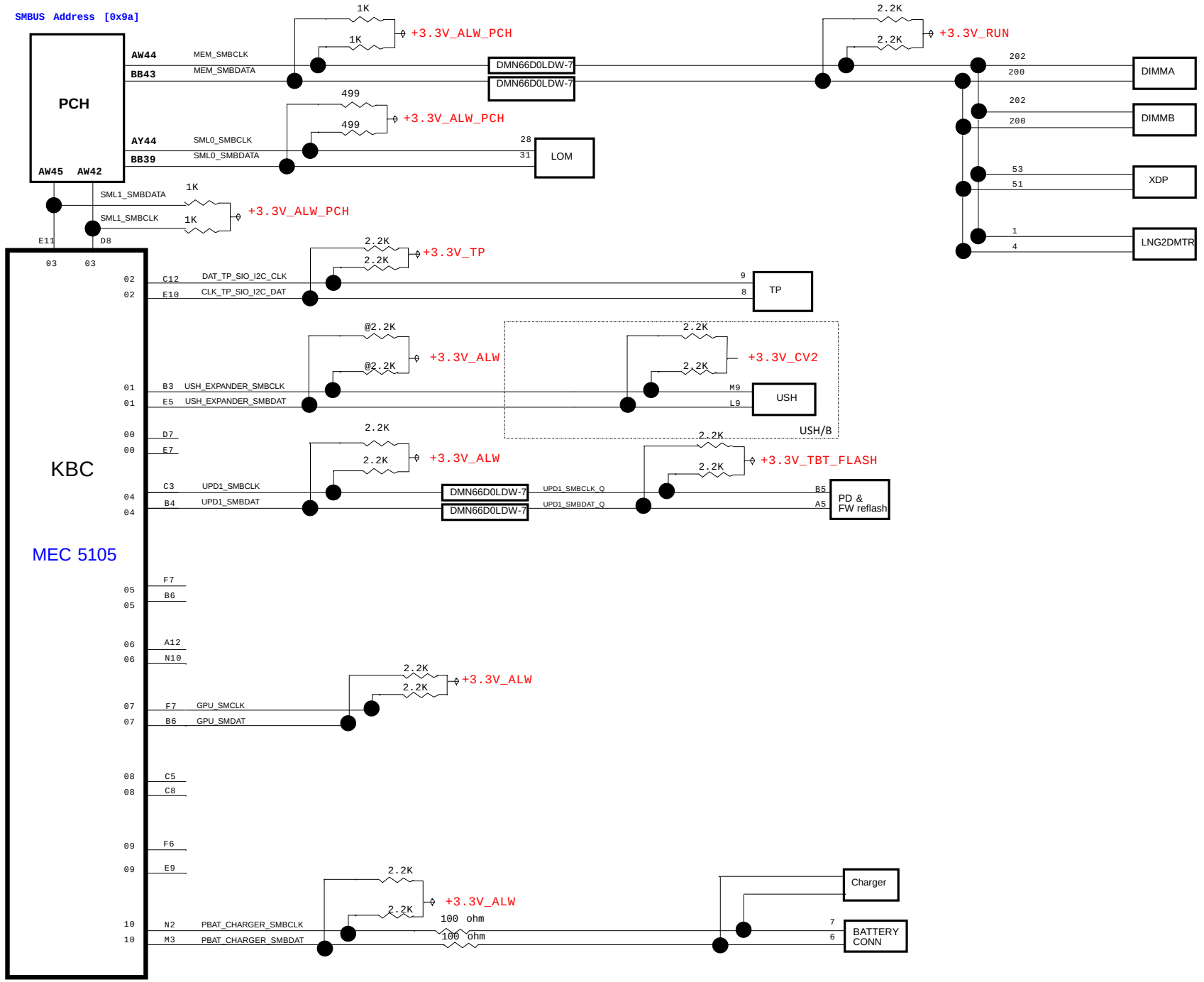

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: SMbus Block Diagram

Size	Document Number	Rev
B	LA-F711P	0.5

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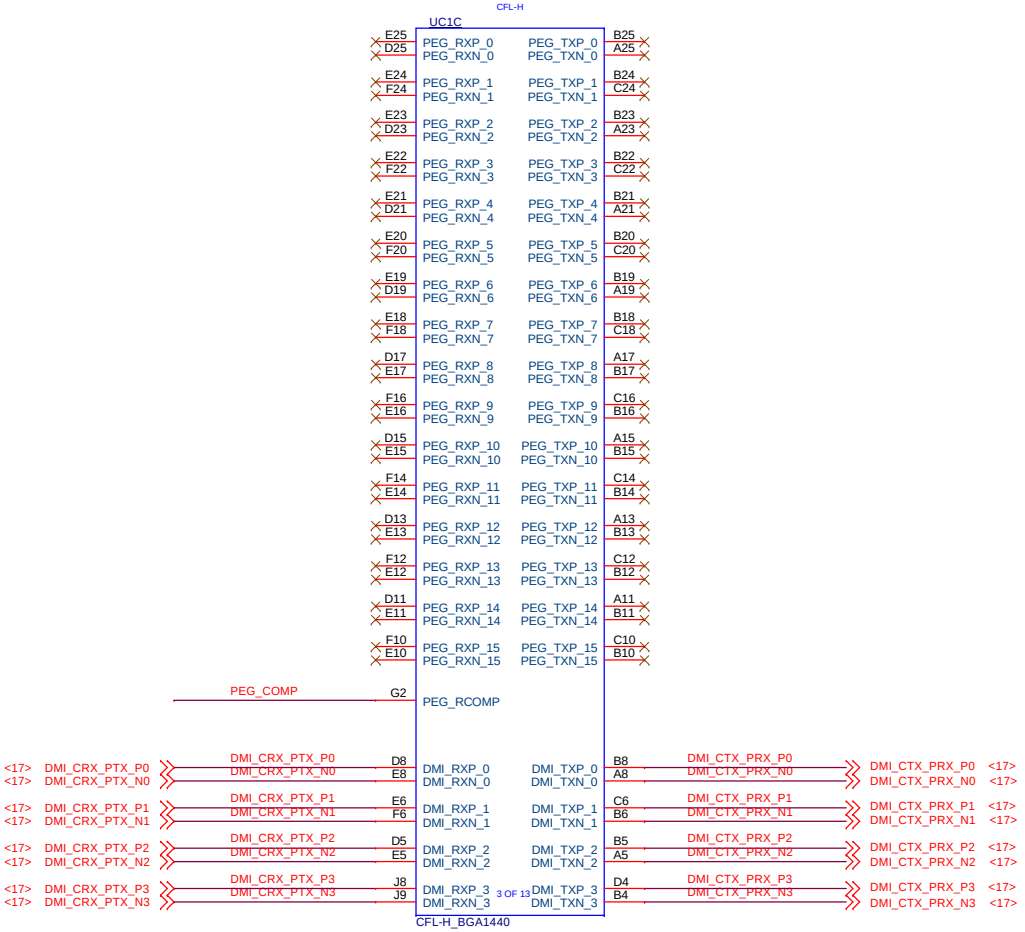

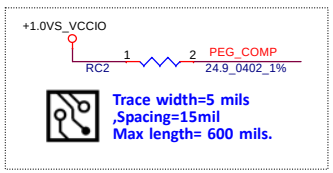

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Title: CFL-H (1/8)

Size	Document Number	Rev
A	LA-F711P	0.5

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CPU XDP

Place near JXDP1.47

Place near JXDP1

Place near JXDP1.41

ESD request,Place near JXDP1 side.

just remind to check layout !!

ESD_Request:place_near_CPU_side

RF Request

Place close CPU side

pop RC171 for CNL
depop RC171 for SKL & KBL (CFL CRB rev0.5)

CFG11	
DMI_AC_coupled	
HALF-SWING DC coupled	1
FULL-SWING AC coupling	0

CFG12	
PMSYNC2.0	1
LEGACY	0

CFG10	
SAFE mode boot	
active	1
Not active	0

CFG9	
SVID NOT Present	
Present	1
Not presnet	0

CFG8	
CFG UNLOCK	
disable	1
enable	0

CFG1	
PCHLESS MODE (CRB) Reserved CFG lane (EDS)	
NORMAL	1
PCHLESS	0

CFG13	
SYNC & AYNC MODE	
ASYNCHRONOUS	1
SYNCHRONOUS	0

CFG0	
Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2	
PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4	
eDP enable	
Disabled	1
Enabled	0

CFG5 / CFG6	
PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG7	
PEG Training	
(default) PEG Train immediately following RESET# de-assertion	1
PEG Wait for BIOS for training	0

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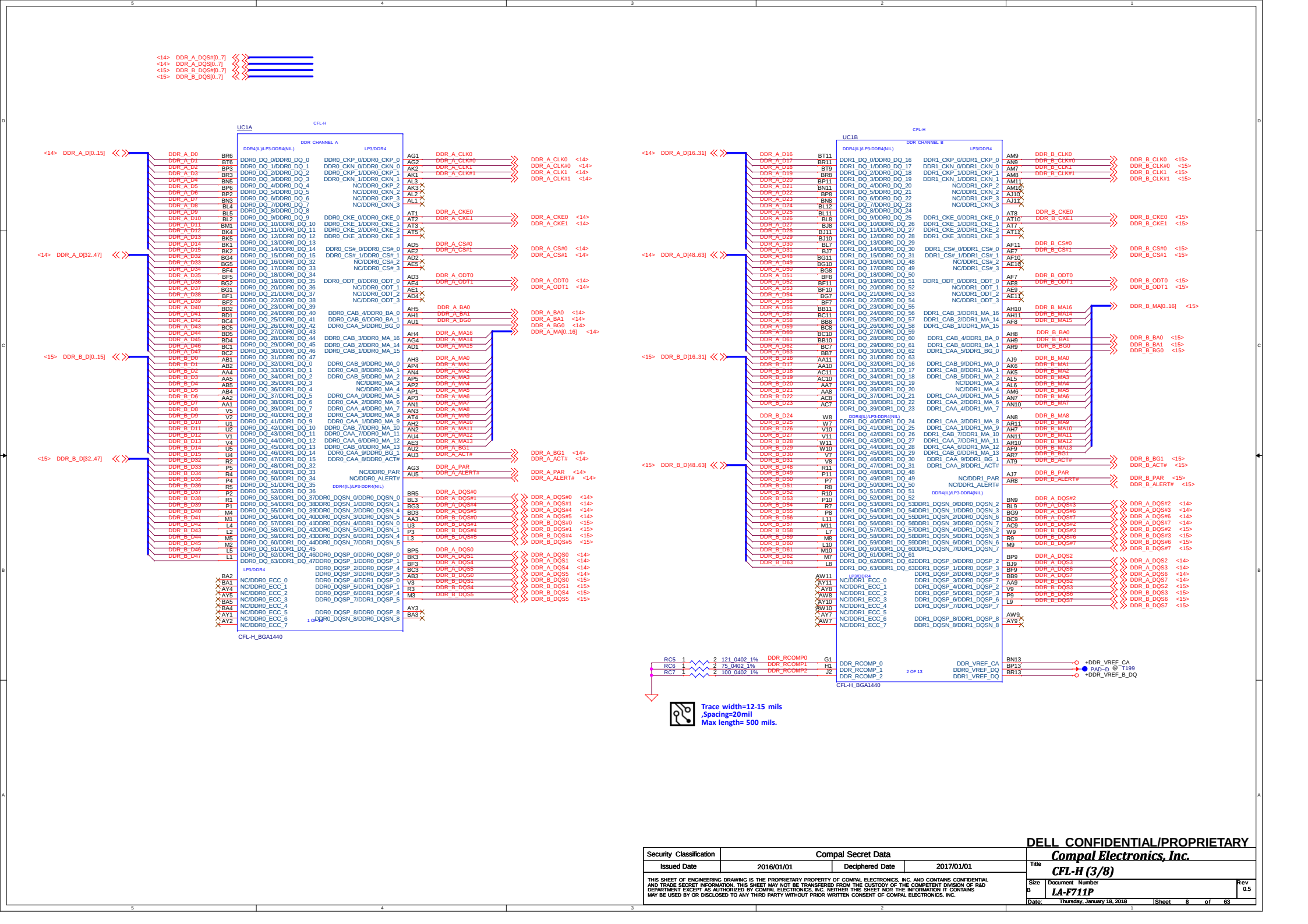
CFL-H (2/8)

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Size	Document Number	Rev
B	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 7 of 63



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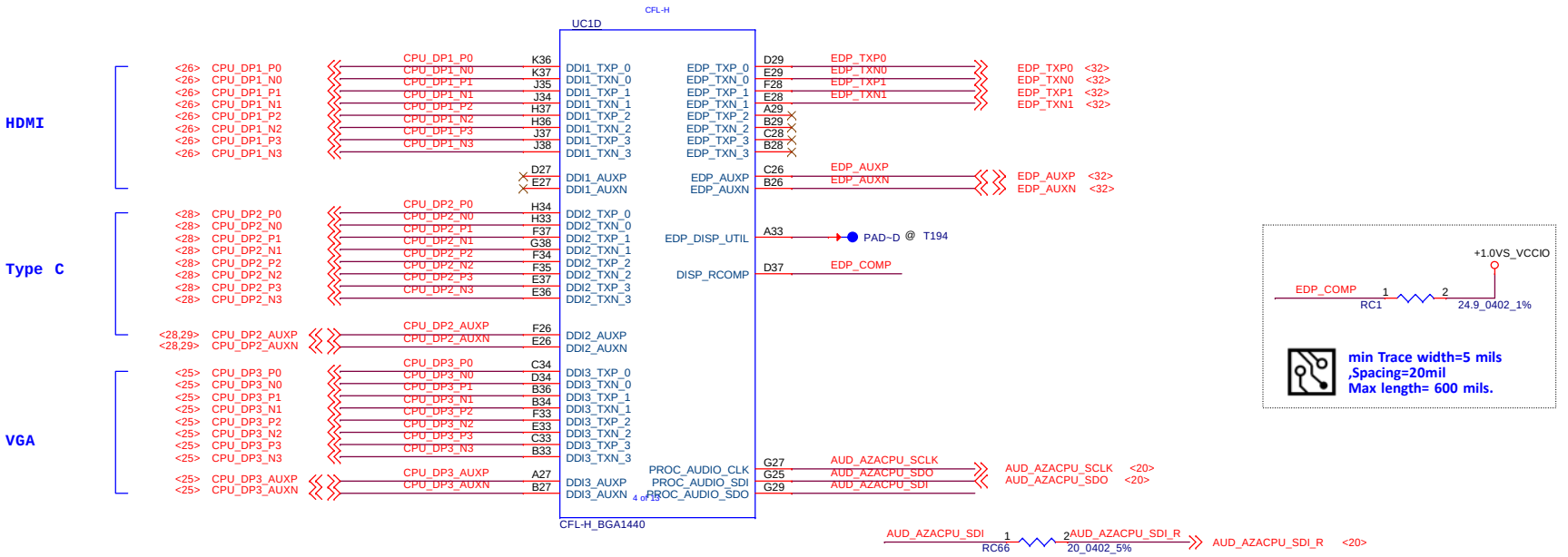
Title	CFL-H (3/8)	
Size B	Document Number LA-F711P	Rev 0.5
Date: Thursday, January 18, 2018	Sheet 8 of 63	



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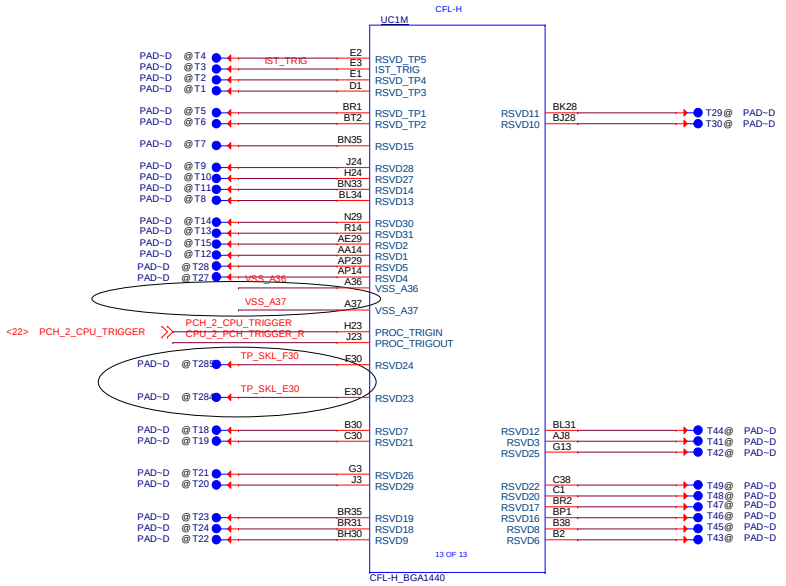
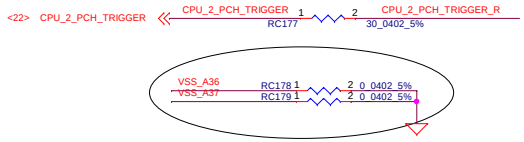
Title: CFL-H (4/8)

Size: A | Document Number: LA-F711P | Rev: 0.5

Date: Thursday, January 18, 2018 | Sheet 9 of 63





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: CFL-H (5/8)

Size	Document Number	Rev
B	LA-F711P	0.5

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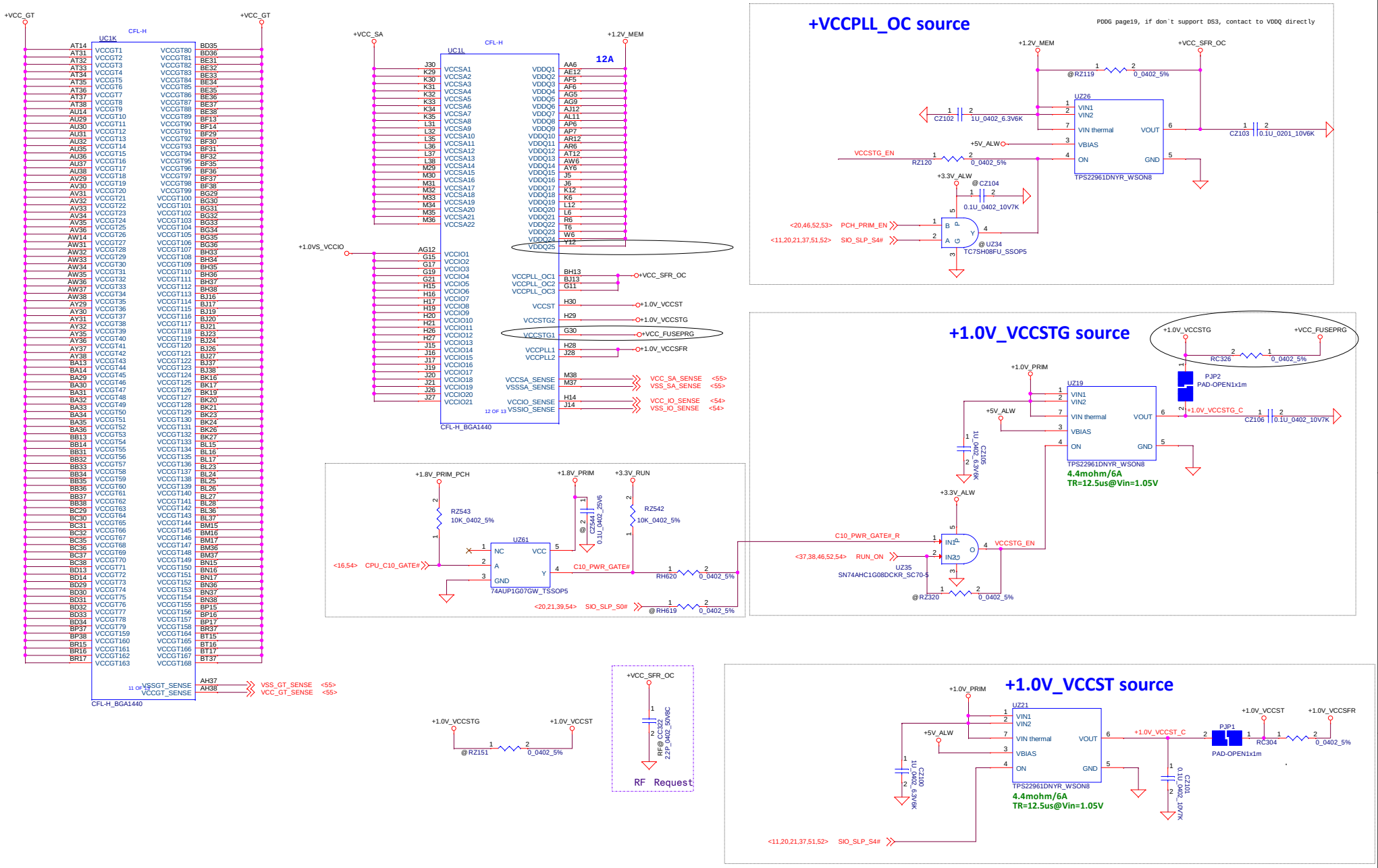

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Title: **CFL-H (6/8)**

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For SKL-H 4+2
Remove VCCOPC/VCCEOPIO/
VCCOPC_1P8 Cap

PLACE CAP BACKSIDE

+1.2V_MEM
+1.0V_VCCSTG
+1.0V_VCCSFR
+1.0V_VCCST
+VCC_SFR_OC

10U_0603_6.3V6M-D CC185
1U_0201_6.3V6M CC186
1U_0201_6.3V6M @ CC195
1U_0201_6.3V6M CC192
1U_0201_6.3V6M CC191
1U_0201_6.3V6M CC210
1U_0201_6.3V6M CC209

close to UC1.Y12

+1.0VS_VCCIO
PLACE CAP BACKSIDE
10U_0603_6.3V6M CC188
10U_0603_6.3V6M CC187
10U_0603_6.3V6M @ CC272

PLACE CAP BACKSIDE or BOARD EDGE
+1.0V_VCCSFR
22U_0603_6.3V6M CC333

PDG rev1.0

+1.0V_VCCST
1U_0402_6.3V6K CC193
1U_0402_6.3V6K CC194

Remove to Power (+VCC_SA cap)

+1.2V_MEM
+1.2V_MEM DECOUPLING
PLACE CAP BACKSIDE
10U_0603_6.3V6M-D CC161
10U_0603_6.3V6M-D CC170
10U_0603_6.3V6M-D CC164
10U_0603_6.3V6M-D CC168
10U_0603_6.3V6M-D CC163
10U_0603_6.3V6M-D CC169
10U_0603_6.3V6M-D CC171
10U_0603_6.3V6M-D CC165
10U_0603_6.3V6M-D CC172
10U_0603_6.3V6M-D CC167
22U_0603_6.3V6M CC321
22U_0603_6.3V6M CC322
22U_0603_6.3V6M CC323
22U_0603_6.3V6M CC324

+VCC_CORE
UC1J
CFL-H
CFL-H_BGA1440
10 OF 13

K14 L13 L14 N13 N14 N30 N31 N32 N35 N36 N37 N38 P13 P14 P29 P30 P31 P32 P33 P34 P35 P36 R13 R31 R32 R33 R34 R35 R36 R37 R38 T29 T30 T31 T32 T35 T36 T37 T38 U29 U30 U31 U32 U33 U34 U35 U36 V13 V14 V31 V32 V33 V34 V35 V36 V37 V38 W13 W14 W29 W30 W31 W32

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63

W35 W36 W37 W38 Y29 Y30 Y31 Y32 Y33 Y34 Y35 Y36

VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75

+VCC_CORE
UC1I
CFL-H
CFL-H_BGA1440
9 OF 13

AA13 AA31 AA32 AA33 AA34 AA35 AA36 AA37 AA38 AB29 AB30 AB31 AB32 AB35 AB36 AB37 AB38 AC13 AC14 AC29 AC30 AC31 AC32 AC33 AC34 AC35 AC36 AD13 AD14 AD31 AD32 AD33 AD34 AD35 AD36 AD37 AD38 AE13 AE14 AE30 AE31 AE32 AE35 AE36 AE37 AE38 AF29 AF30 AF31 AF32 AF33 AF34 AF35 AF36 AF37 AF38 AG14 AG31 AG32 AG33 AG34 AG35 AG36

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63

AH13 AH14 AH29 AH30 AH31 AH32 AJ14 AJ29 AJ30 AJ31 AJ32 AJ33 AJ34 AJ35 AJ36 AK31 AK32 AK33 AK34 AK35 AK36 AK37 AK38 AL13 AL29 AL30 AL31 AL32 AL35 AL36 AL37 AL38 AM13 AM14 AM29 AM30 AM31 AM32 AM33 AM34 AM35 AM36 AN13 AN14 AN31 AN32 AN33 AN34 AN35 AN36 AN37 AN38 AP13 AP30 AP31 AP32 AP35 AP36 AP37 AP38 K13

VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100 VCC101 VCC102 VCC103 VCC104 VCC105 VCC106 VCC107 VCC108 VCC109 VCC110 VCC111 VCC112 VCC113 VCC114 VCC115 VCC116 VCC117 VCC118 VCC119 VCC120 VCC121 VCC122 VCC123 VCC124

AG37 AG38

VCC_SENSE
VSS_SENSE

+VCC_CORE
RC140 100_0402_1%
RC141 100_0402_1%

VCC_SENSE <55>
VSS_SENSE <55>

VSS_SENSE
@RC221 49.9_0402_1%
VCC_SENSE

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Compal Electronics, Inc.

Title: CFL-H (7/8)

Size	Document Number	Rev
B	LA-F711P	0.5

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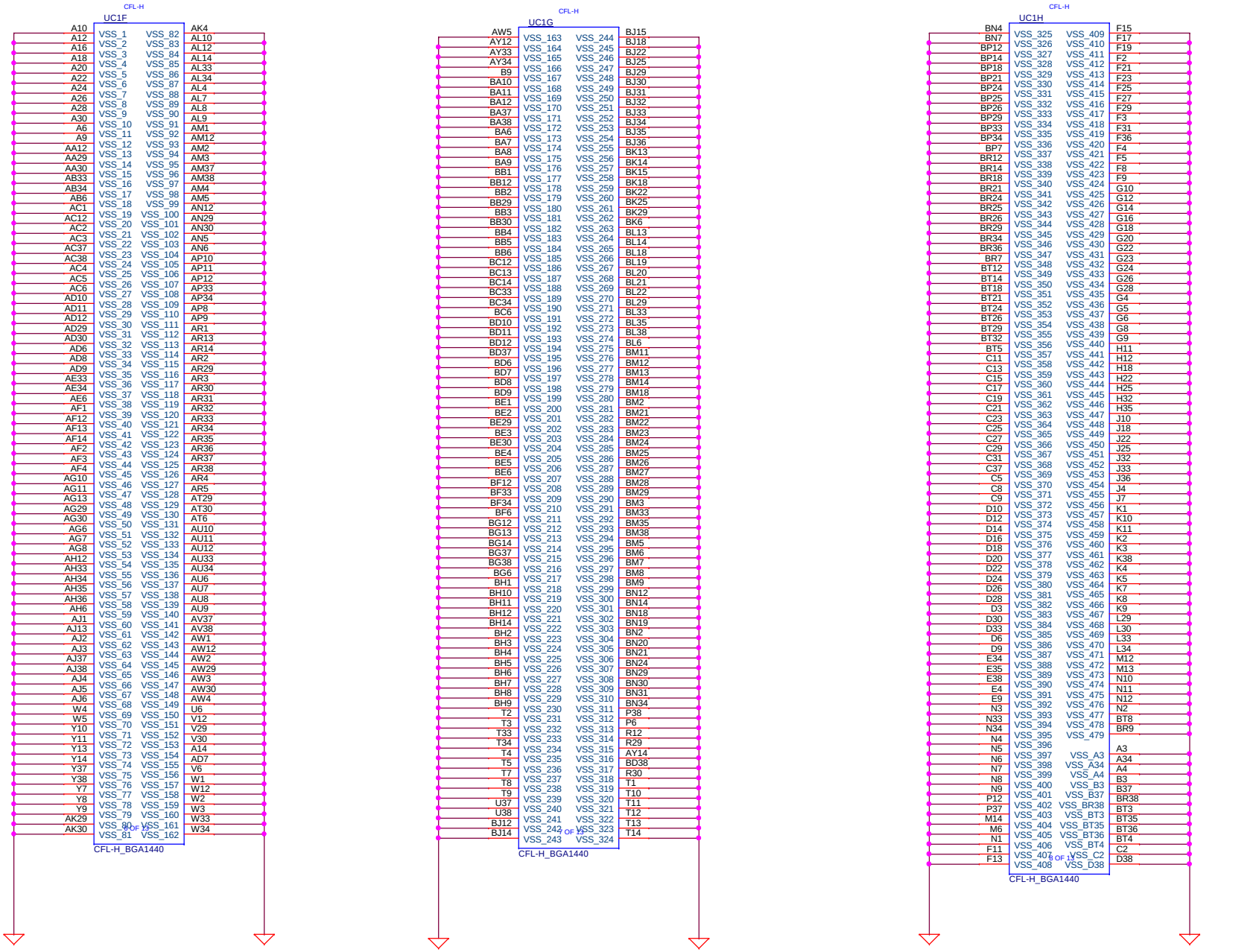

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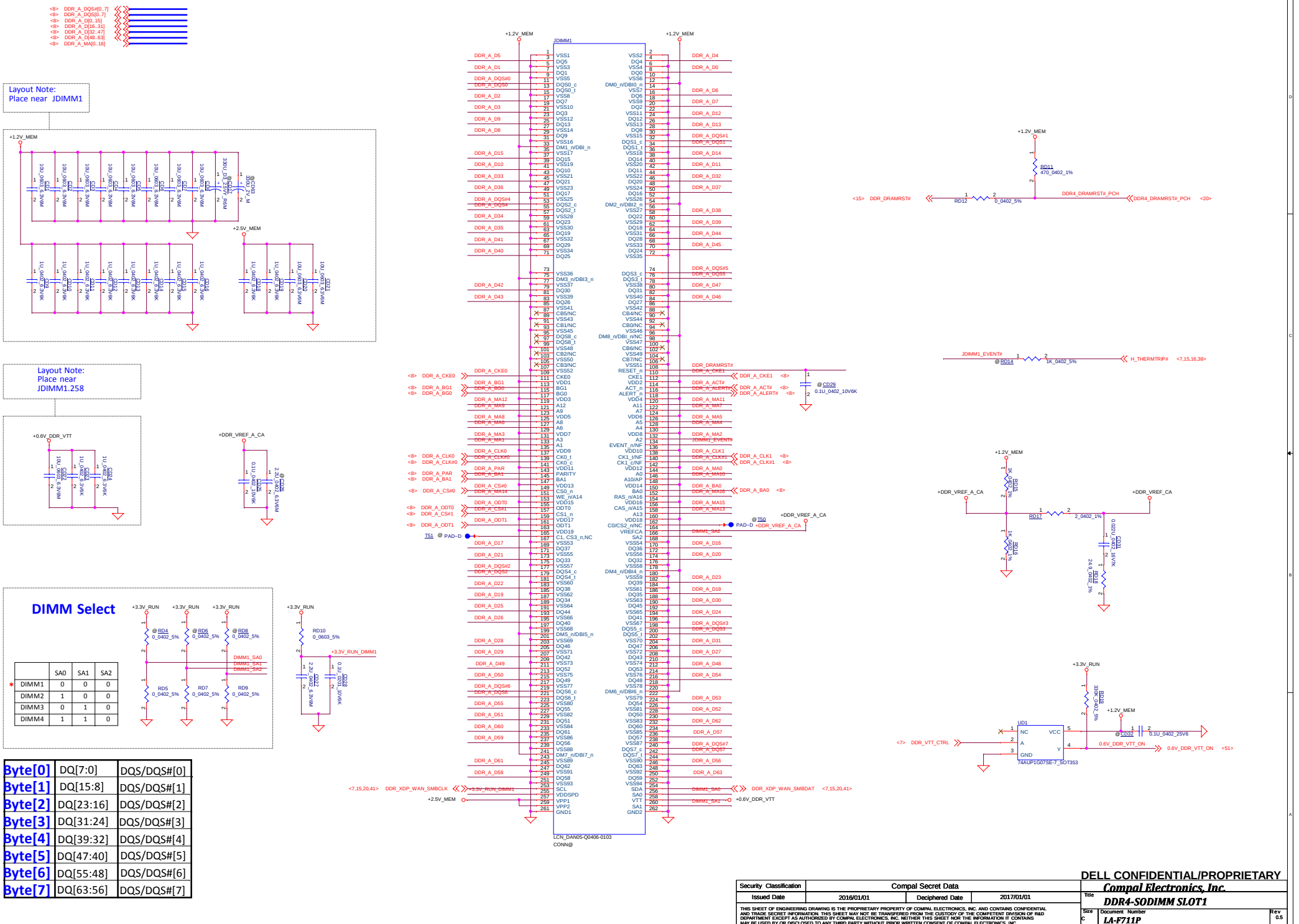
Compal Electronics, Inc.

Title: CFL-H (8/8)

Size	Document Number	Rev
A	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 13 of 63



Security Classification	Compal Secret Data
Issued Date	2016/01/01
Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	DDR4-SODIMM SLOT1
Size	C
Document Number	LA-F711P
Rev	0.5
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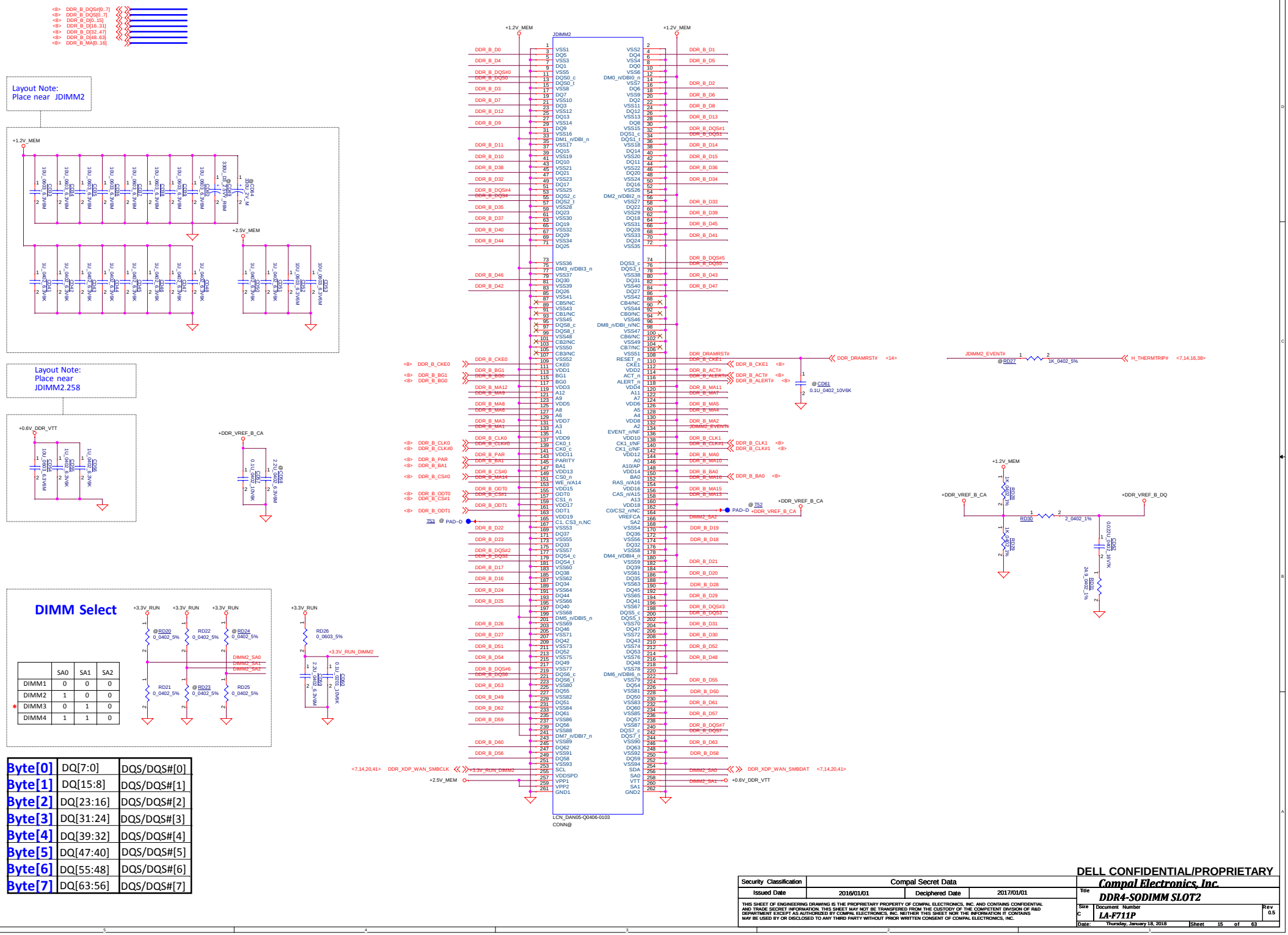

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Compal Electronics, Inc.

Title: DDR4-SODIMM SLOT2

Size	Document Number	Rev
C	LA-F711P	0.5

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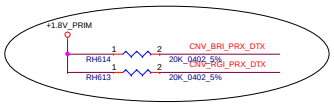
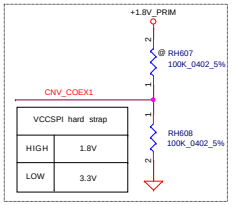
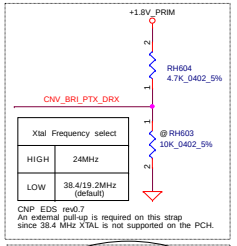
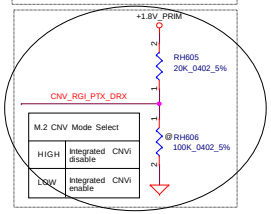


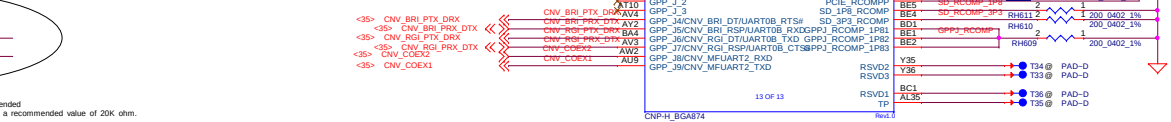
CFL PDG rev0.5
To avoid floating input at the I/O pin it is recommended
to add a weak pull up resistor to the SOC pin with a recommended value of 20K ohm.



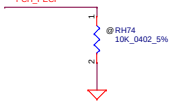


CNP EDS rev0.7
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.





SPSGP0	0	SATAGP0	1=SATA	0=PCIE
SPSGP1	1	m2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	m3042_PCIE#_SATA	1=SATA	0=PCIE
SPSGP5	0	SPTAGP5	1=SATA	0=PCIE



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	CannonLake PCH-H (1/9)		
Size	Document Number		Rev
C	LA-F711P		0.5
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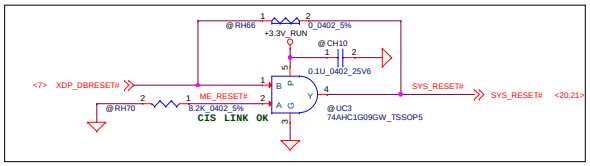
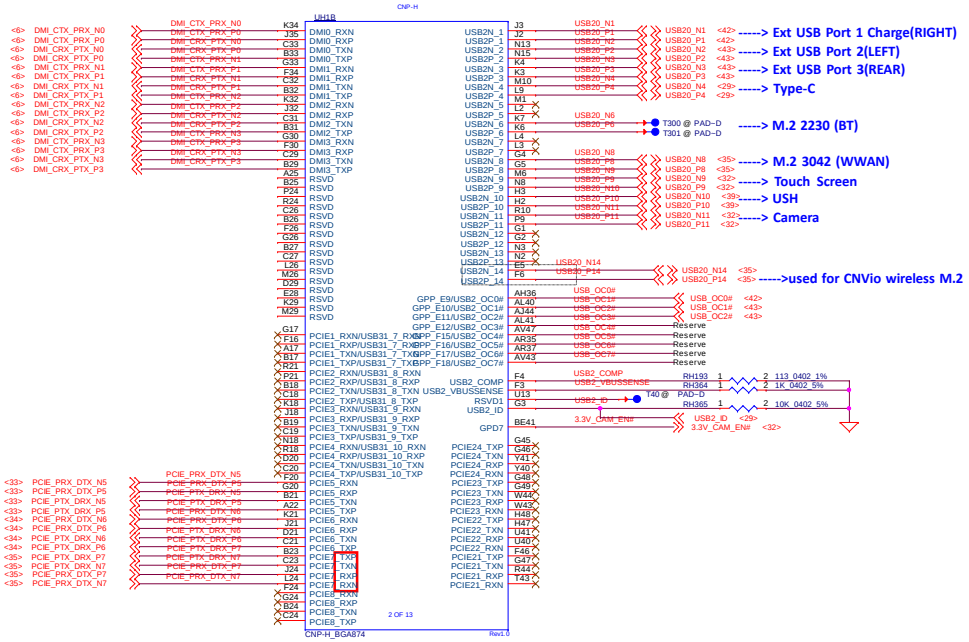
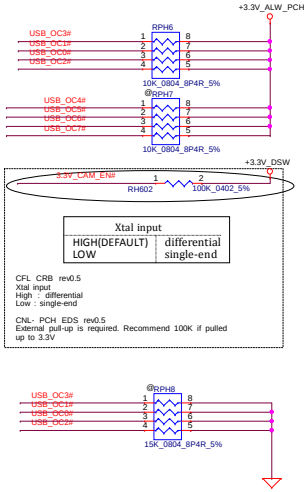
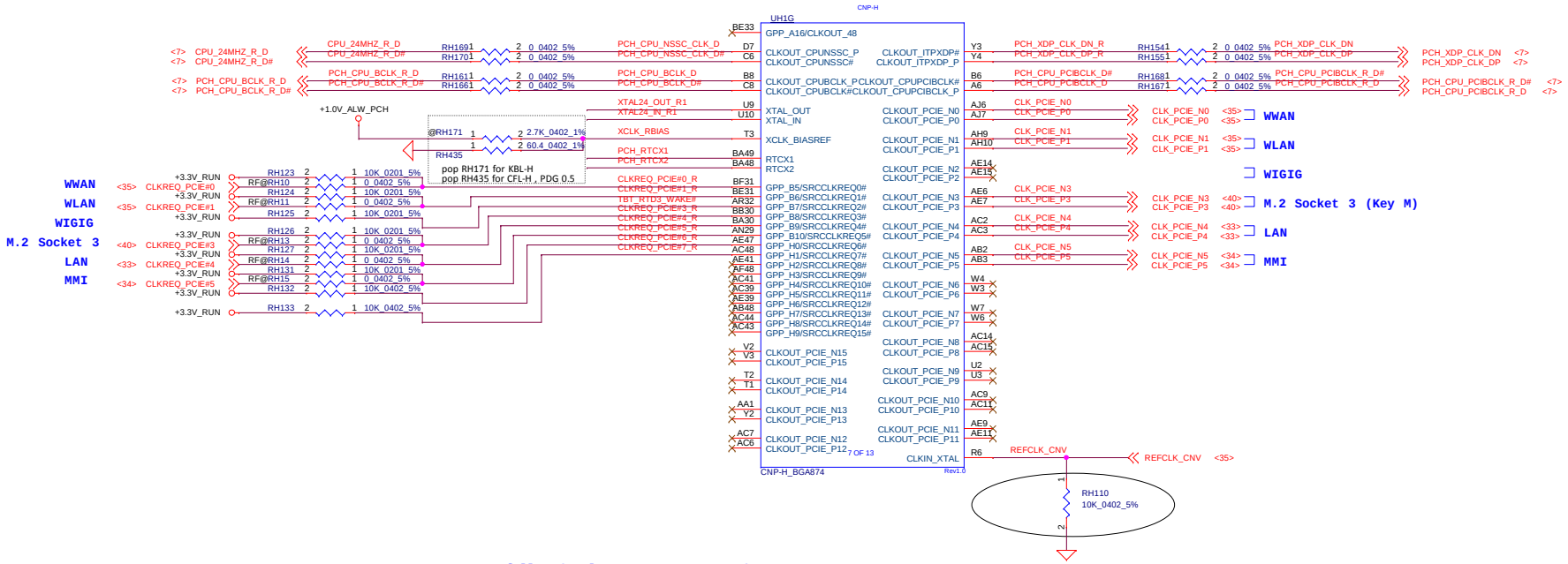




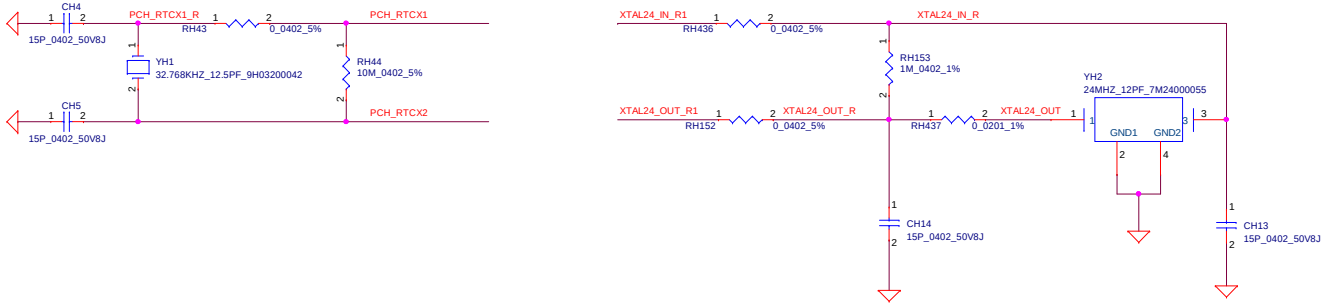


Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	CannonLake PCH-H (2/9)		
Size	Document Number		Rev
C	LA-F711P		0.5
Date:	Friday, January 26, 2018	Sheet	17 of 63



follow intel CFL-H PDG rev0.5, but CRB rev0.5 - CSLP1
follow intel CRB design - CSLP2, EVT



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *CannonLake PCH-H (3/9)*

Size	Document Number	Rev
B	*LA-F711P*	0.5

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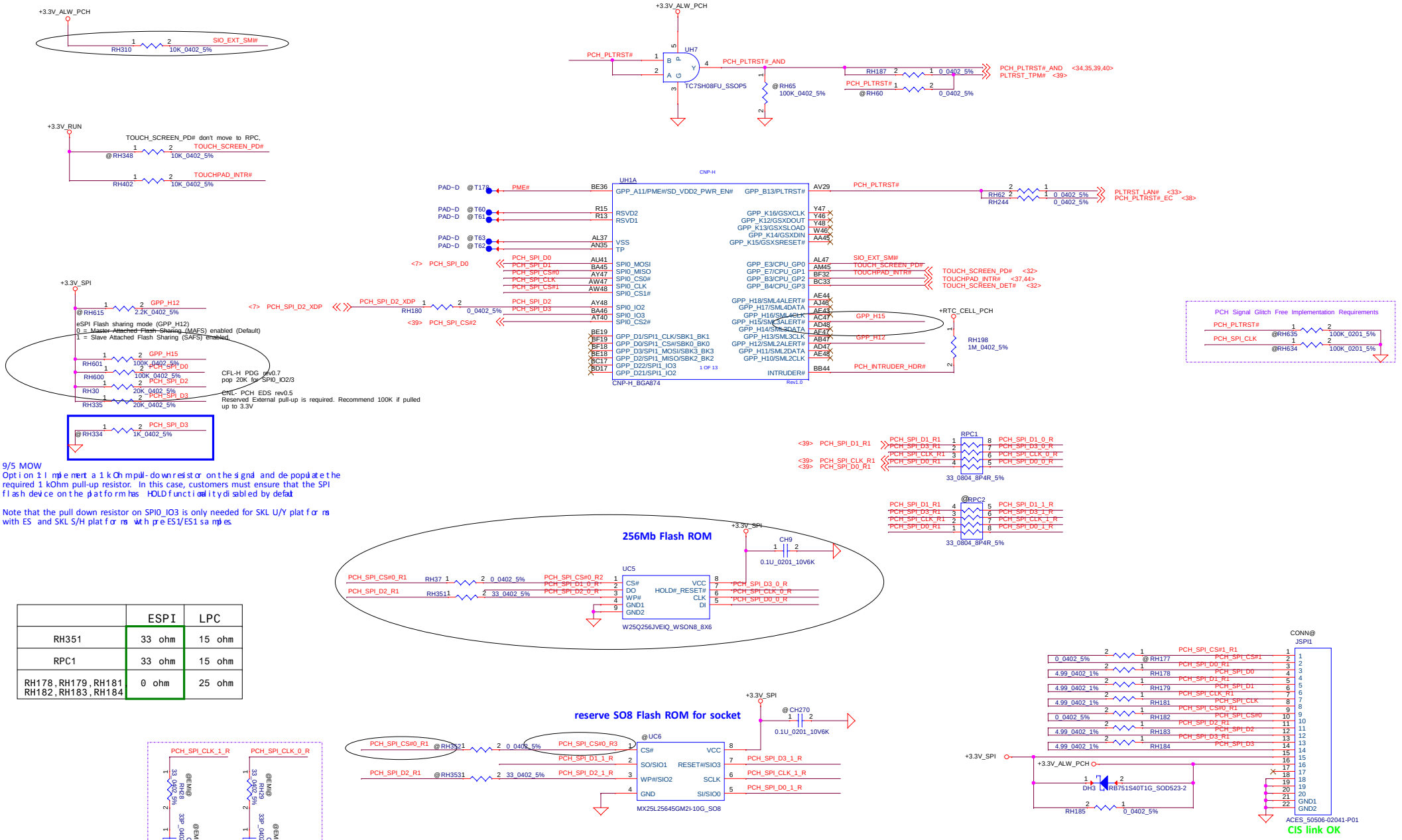

	ESPI	LPC
RH351	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RH178,RH179,RH181 RH182,RH183,RH184	0 ohm	25 ohm

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *CannonLake PCH-H (4/9)*

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Ext USB Port 1 Charge(RIGHT)

M.2 3042 (LTE)

Type C

Ext USB Port 2(LEFT)

Ext USB Port 3(REAR)

RF Request

CFL-H CRB rev0.5

Intel DCI-OOB

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.

If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionalityis used, leave float.

If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entirere gion of the SPI flash to be updated using FPT

ME_FWP PCH has internal 20K PD. (suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

RH215

POP	NO Support Deep sleep
DE-POP	Support Deep sleep

For DS3:
Pop RE349, RE536, RH439, RH441, RH443
Depop DH1, RH215, RH440, RH442

For NDS3 :
Pop DH1, RH215, RH440, RH442
Depop RE349, RE536, RH439, RH441, RH443

PCH Signal Glitch Free Implementation Requirements

ESD_Request,place_near_PCH_side

ESD request,Place near PCH side.

CHECK,LPC_CLK_FOR_DEBUG_CARD?

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: CannonLake PCH-H (5/9)

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B	LA-F711P	0.5

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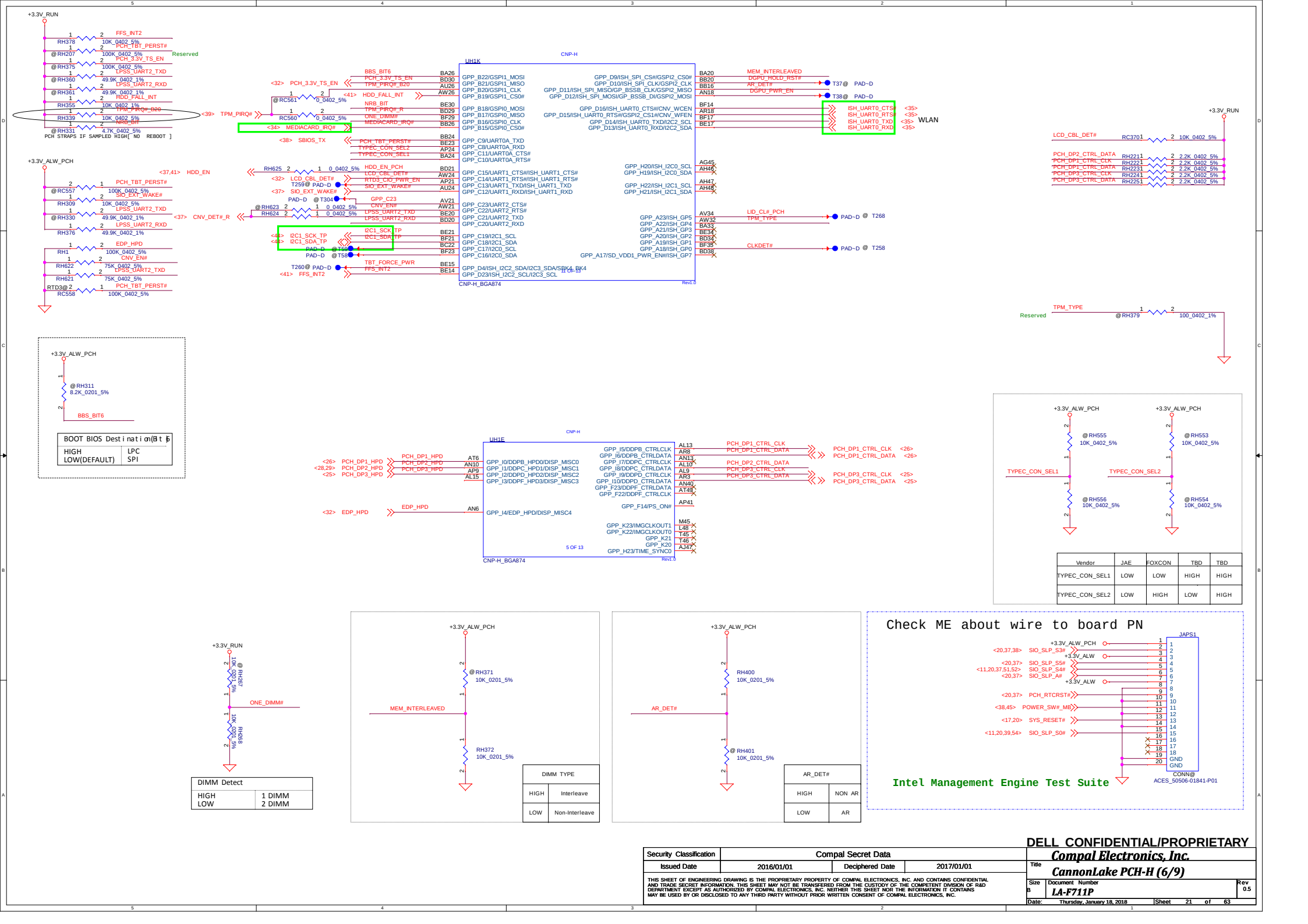

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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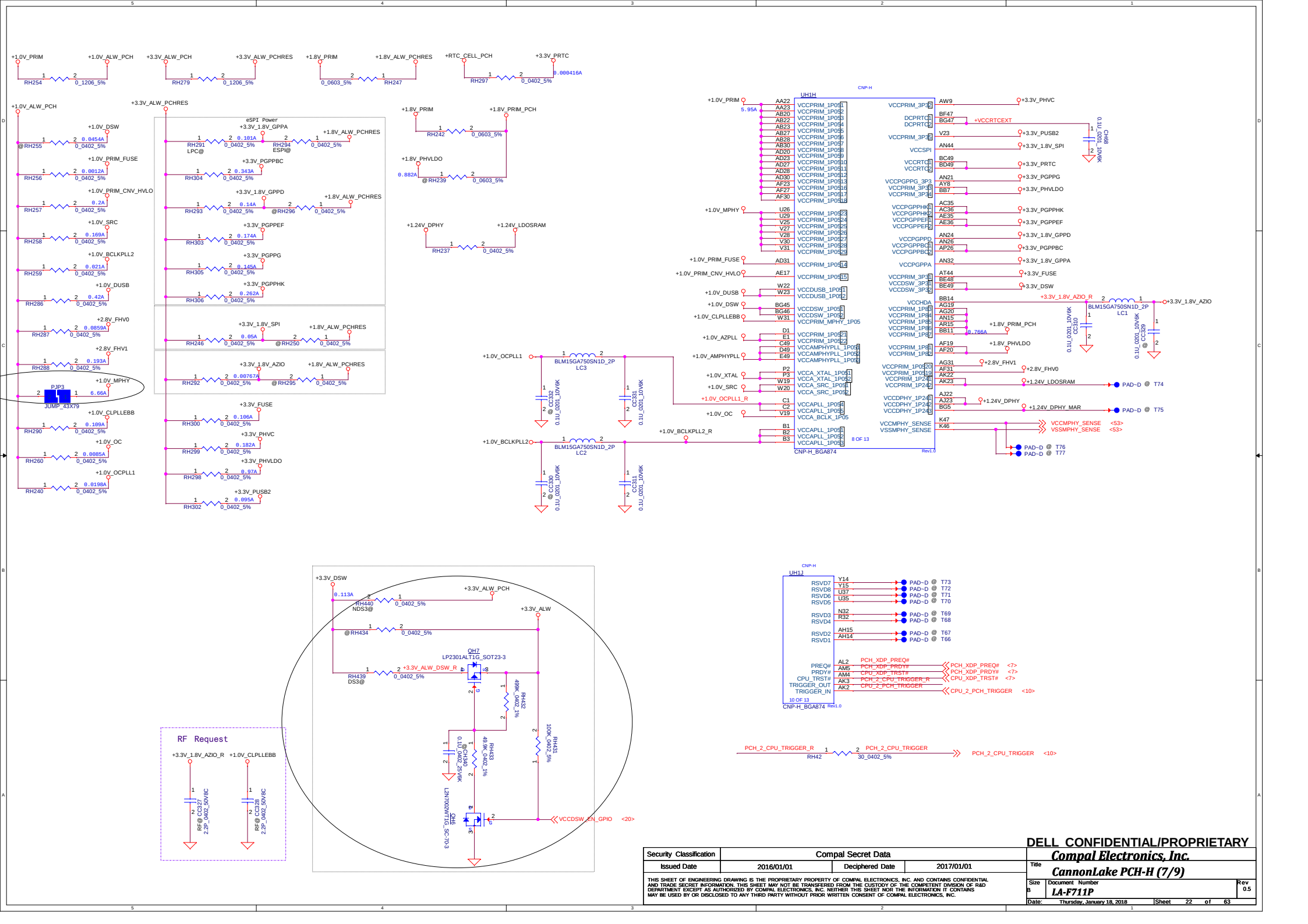
Compal Electronics, Inc.

Title: *CannonLake PCH-H (6/9)*

Size	Document Number	Rev
B	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 21 of 63



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *CannonLake PCH-H (7/9)*

Size	Document Number	Rev
B	*LA-F711P*	0.5

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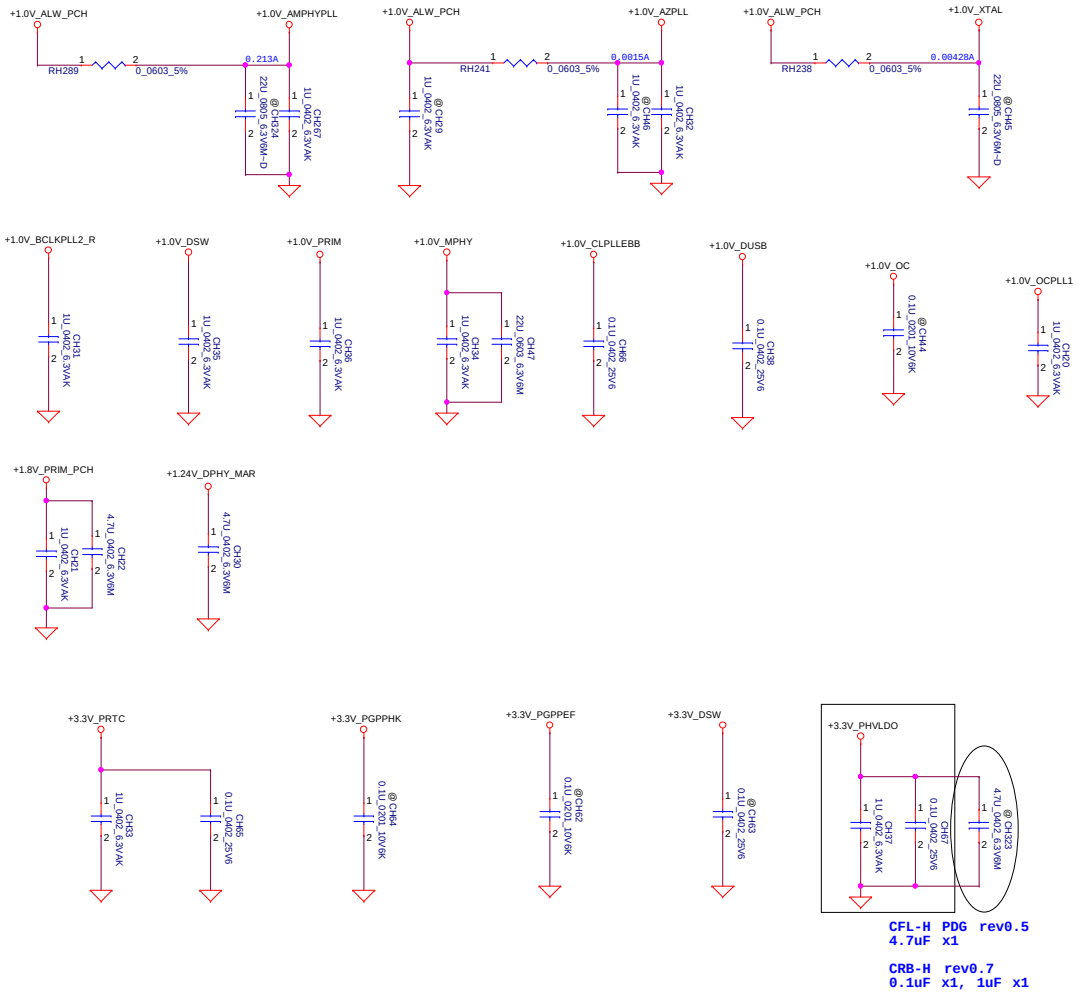

CFL-H PDG rev0.5
4.7uF x1

CRB-H rev0.7
0.1uF x1, 1uF x1

Compal Electronics, Inc.			
Title: CannonLake PCH-H (8/9)			
Size: B	Document Number: LA-F711P		Rev: 0.5
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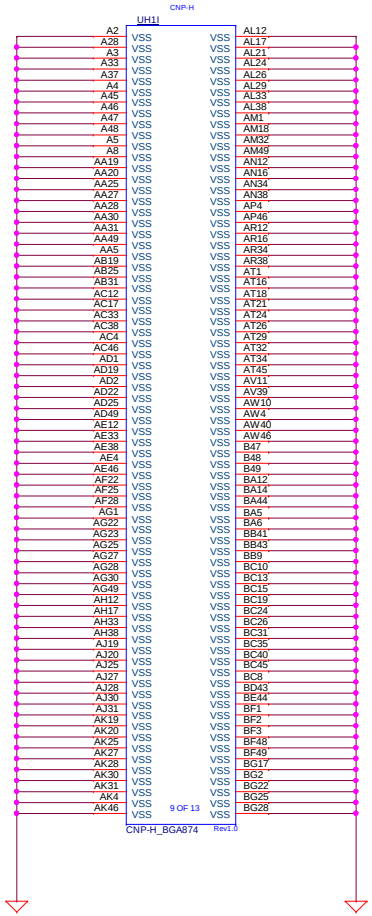

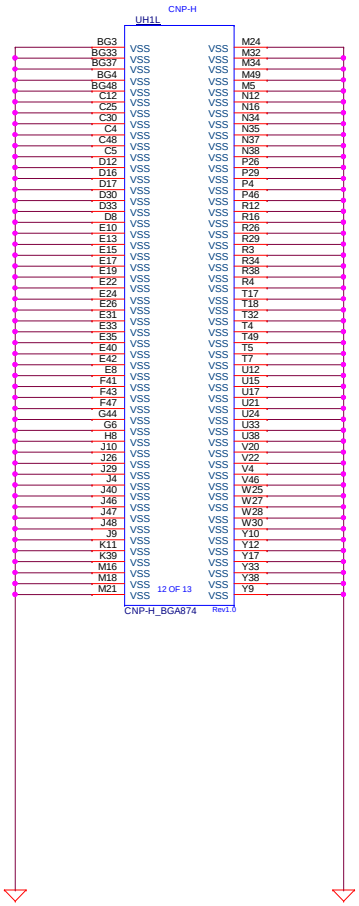

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: CannonLake PCH-H (9/9)		
Size: B	Document Number: LA-F711P	Rev: 0.5
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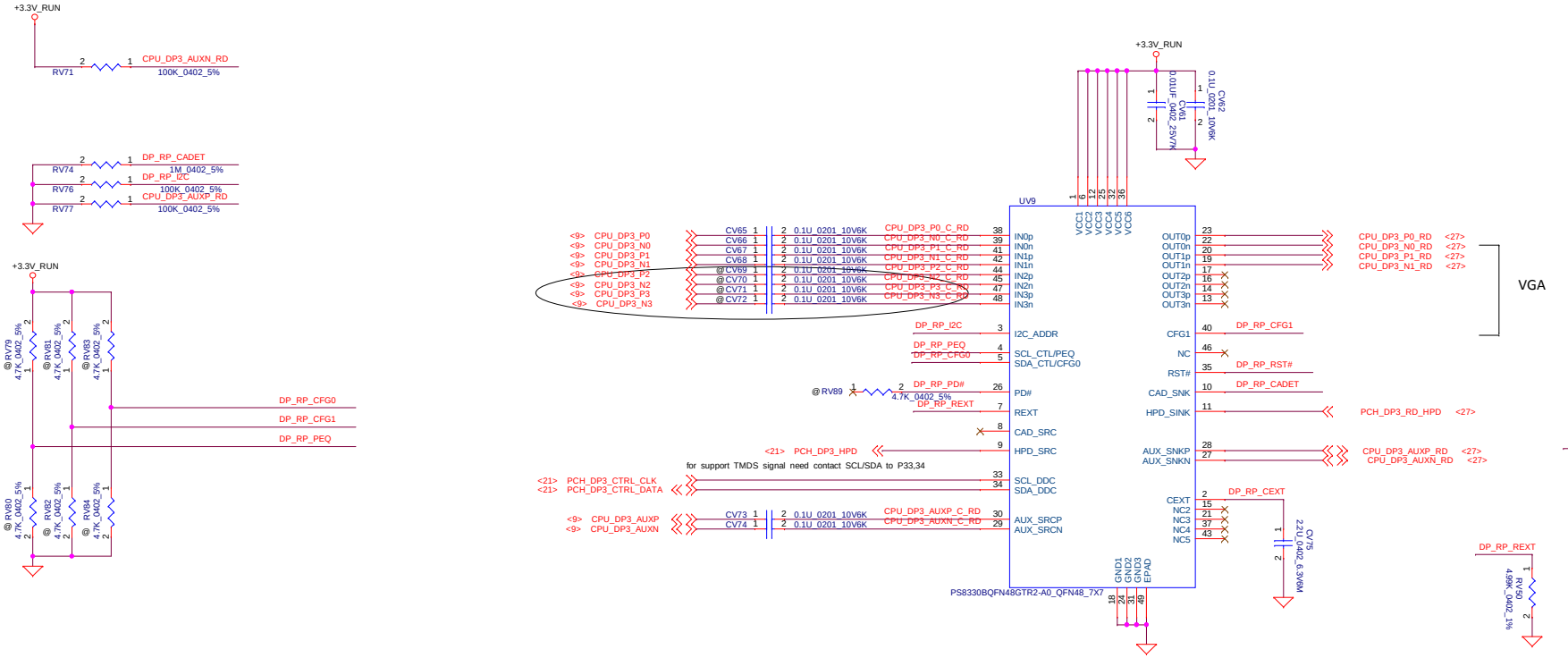

DP_RP_CFG0 :
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3 3V I / O
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

DP_RP_CFG1 :
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

DP_RP_PEQ :
Programmable input equalization levels; Internal pull down at ~150kΩ, 3 3VI / O
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DP SW2 PS8338

Size	Document Number	Rev
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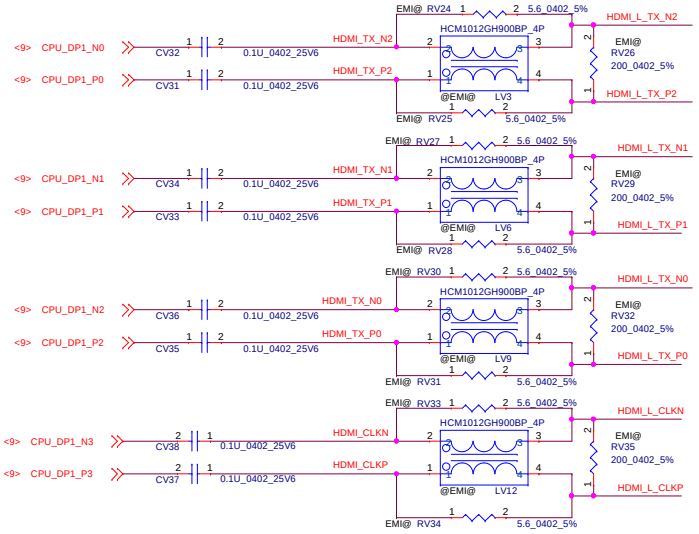
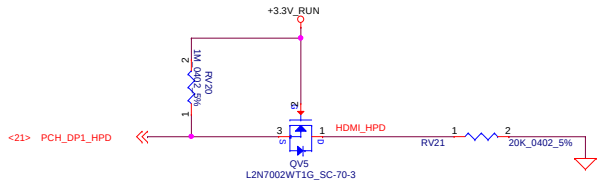
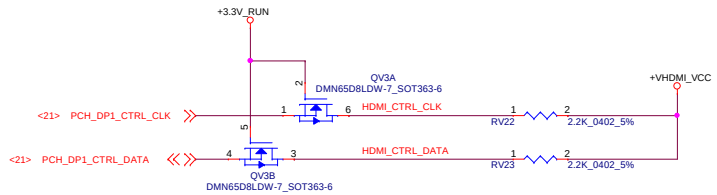
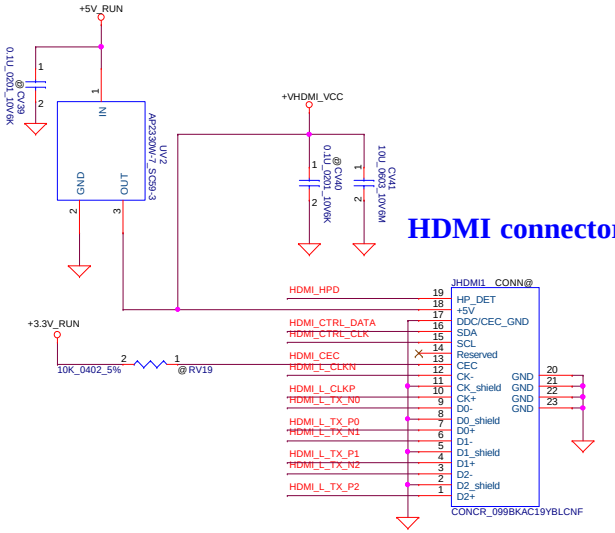
For Breckenridge 15

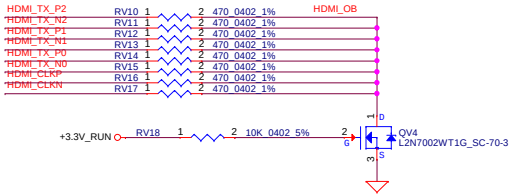








LINK 099BKAC19YBLCNF DONE



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title	HDMI CONN	
Size B	Document Number LA-F711P	Rev 0.5
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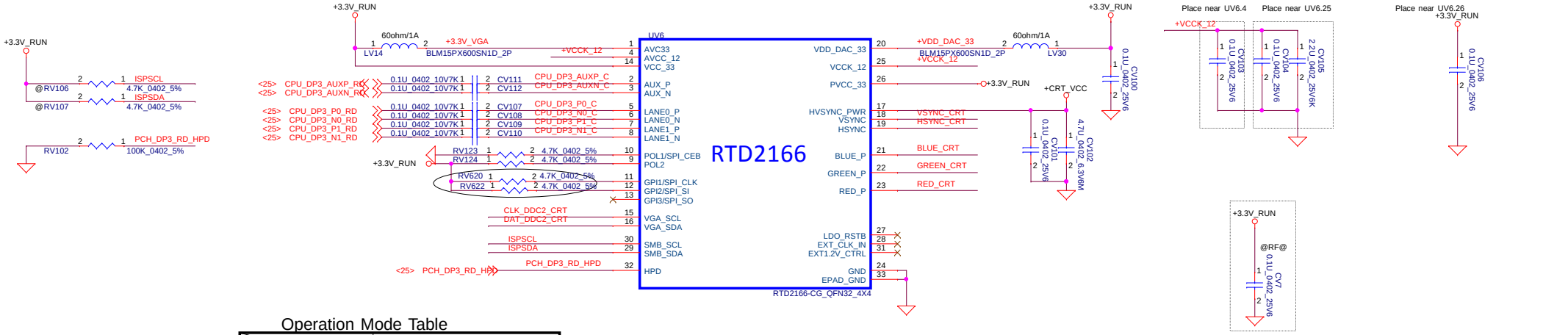
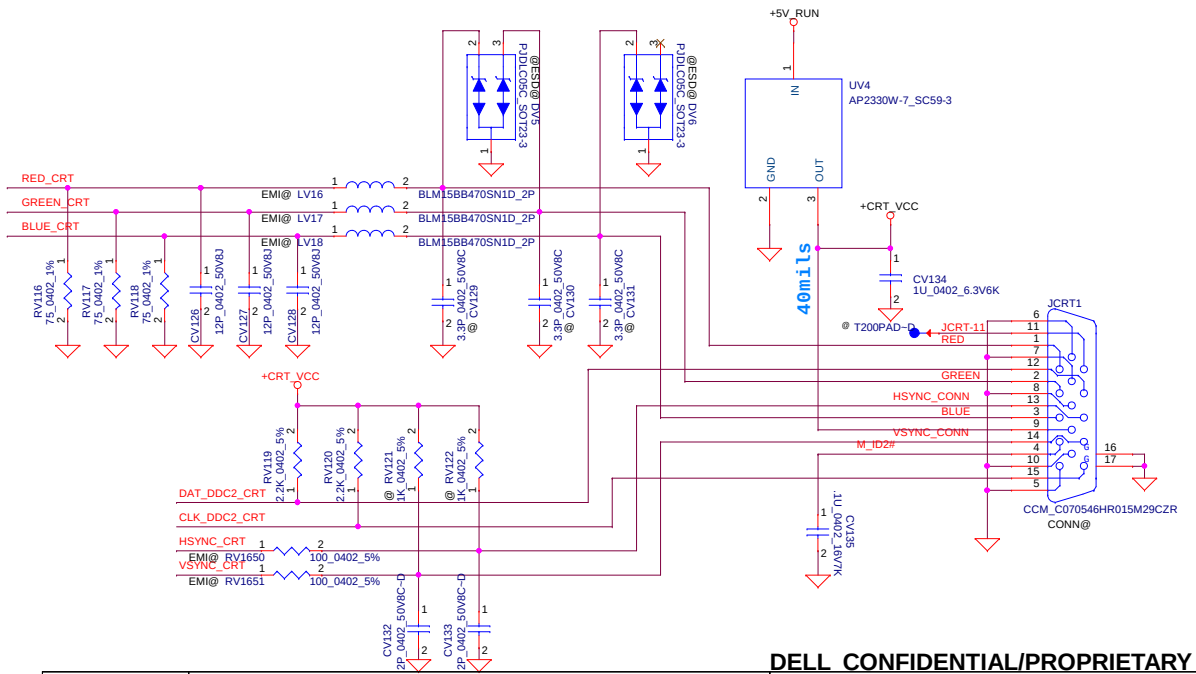
For TBT SW2_DP2
For non-TBT SW1_DP2

For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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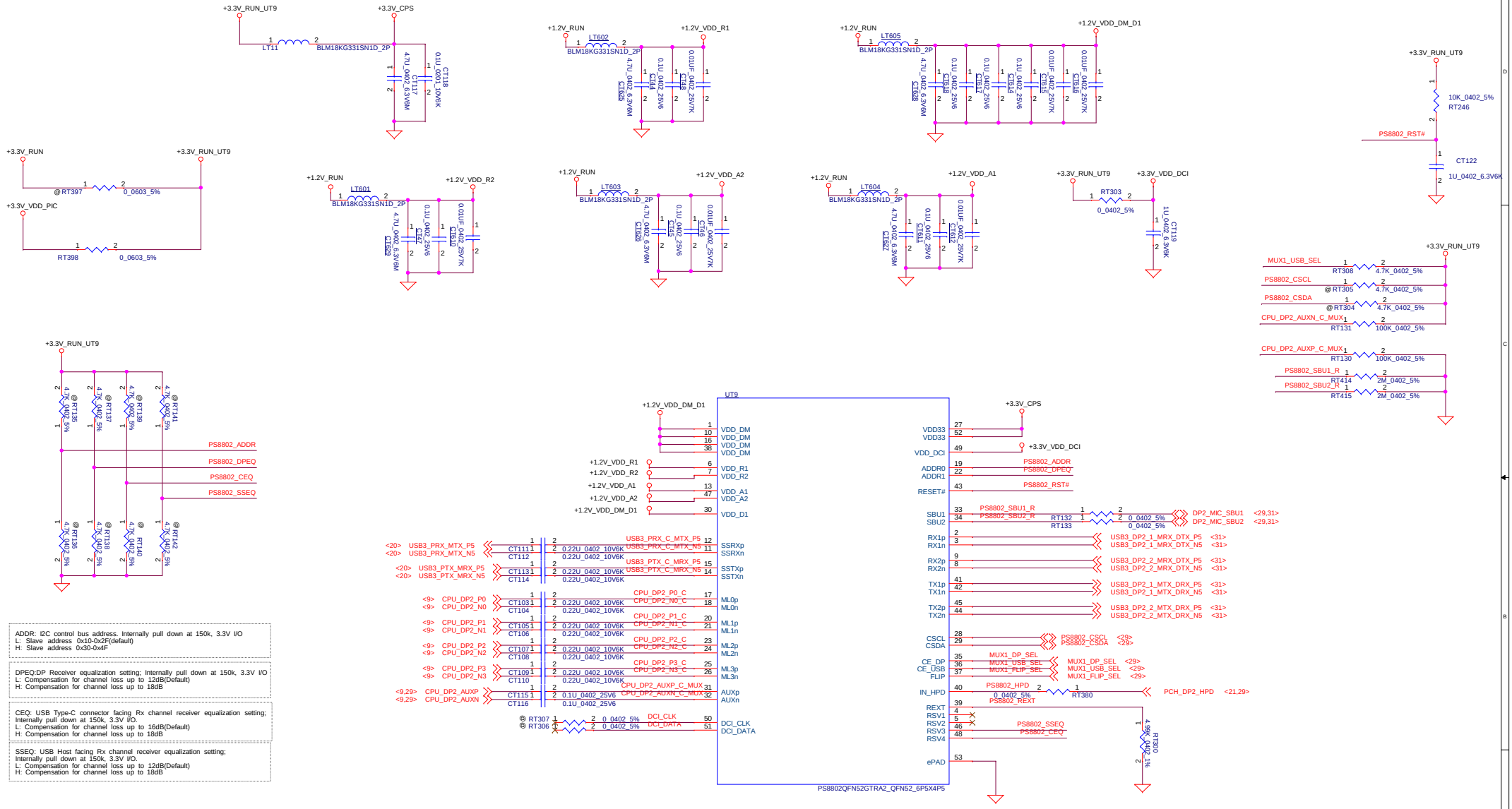
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	DP to VGA & VGA Conn		
Size	Document Number		Rev
Custom	LA-F711P		0.5
Date:	Thursday, January 18, 2018	Sheet	27 of 63



ADDR: I2C control bus address. Internally pull down at 150k, 3.3V I/O
L: Slave address 0x10-0x2F(default)
H: Slave address 0x30-0x4F

DPEQ:DP Receiver equalization setting; Internally pull down at 150k, 3.3V I/O
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

CEQ: USB Type-C connector facing Rx channel receiver equalization setting; Internally pull down at 150k, 3.3V I/O.
L: Compensation for channel loss up to 16dB(Default)
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting; Internally pull down at 150k, 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *DP/USB3 Re-timer PS8802*

Size	Document Number	Rev
B	*LA-F711P*	0.5

Date: Wednesday, January 31, 2018 | Sheet 28 of 63

For Non-AR config

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

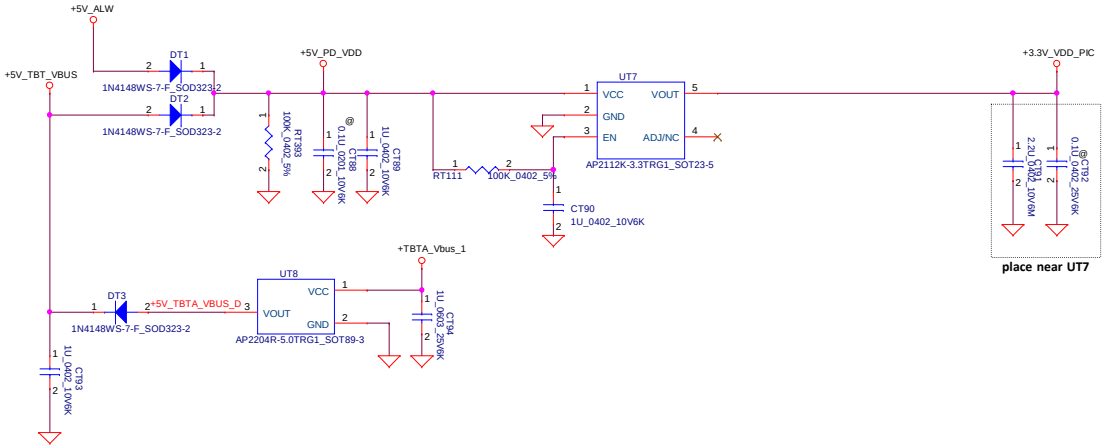
Route in pass through manner so AUX can be snooped by 546

change TPS65982DB -> DC

RF requeat

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: [Type C]PD Controller TI			
Size: C	Document Number: LA-F711P		Rev: 0.5
Date: Thursday, January 18, 2018		Sheet 29 of 63	



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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

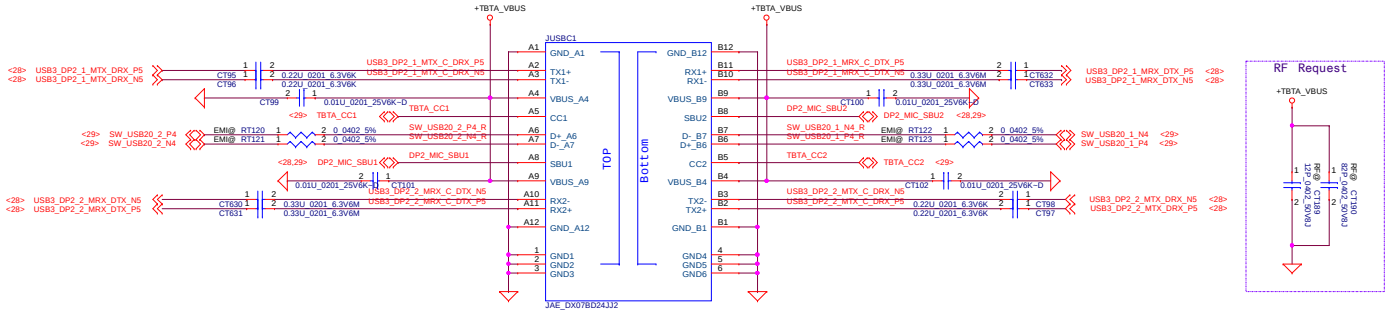
Title: [Type C]PD Power

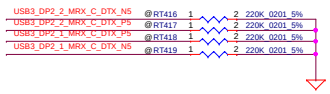
Size	Document Number	Rev
B	LA-F711P	0.5

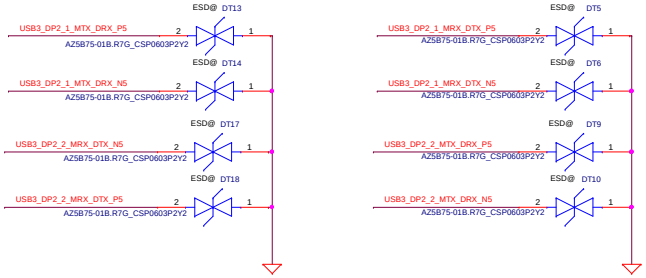
Date: Thursday, January 18, 2018 | Sheet 30 of 63

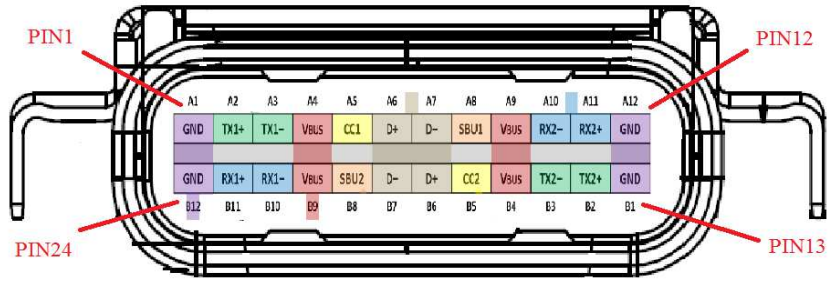
For NON AR Config

CT630~633 use SD043000080 (0 ohm) for CSLP3 build









change typeC ESD part from SC40000AR00 to SC40000DF00

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size: C | Document Number: LA-F711P | Rev: 0.5

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For Breckenridge 14

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

JEDP1
ACES_50398-04041-001
CONN@

EXC24CQ900U_4P
LV27 EMI@

ESD depop locat i on

RF Request

If touch panel, GPIO Low-> Touch Mic. EQ ; others the GPIO is High -> Non-Touch Mic. EQ

Reserve for EA

ACES_50208-0060N-P01

For BL_PWR_SRC & LCDVDD monitor

QV18 MMBT3906H_SOT23-3
QV19 MMBT3904WT1G SC70-3
QV20 MMBT3906H_SOT23-3
QV21 MMBT3904WT1G SC70-3
DV11 RB751S40T1G_SOD523-2
DV12 RB751S40T1G_SOD523-2

For Touchscreen

QV8 LP2301ALT1G_SOT23-3
QV7 L2N7002WT1G_SC-70-3

WebCAM

QZ1 LP2301ALT1G_SOT23-3
EXC24CQ900U_4P
LZ1 EMI@

Backlight POWER

QV1 AO6405_TSOP6
QV2 L2N7002WT1G_SC-70-3

Co-lay:
Short PJP13;Depop RZ90

LCDVDD POWER

UV24 GS24B1T11U_SOT23-5

Co-lay:
Short PJP12;Depop RZ93

DV3 BAT54CW_SOT323-3

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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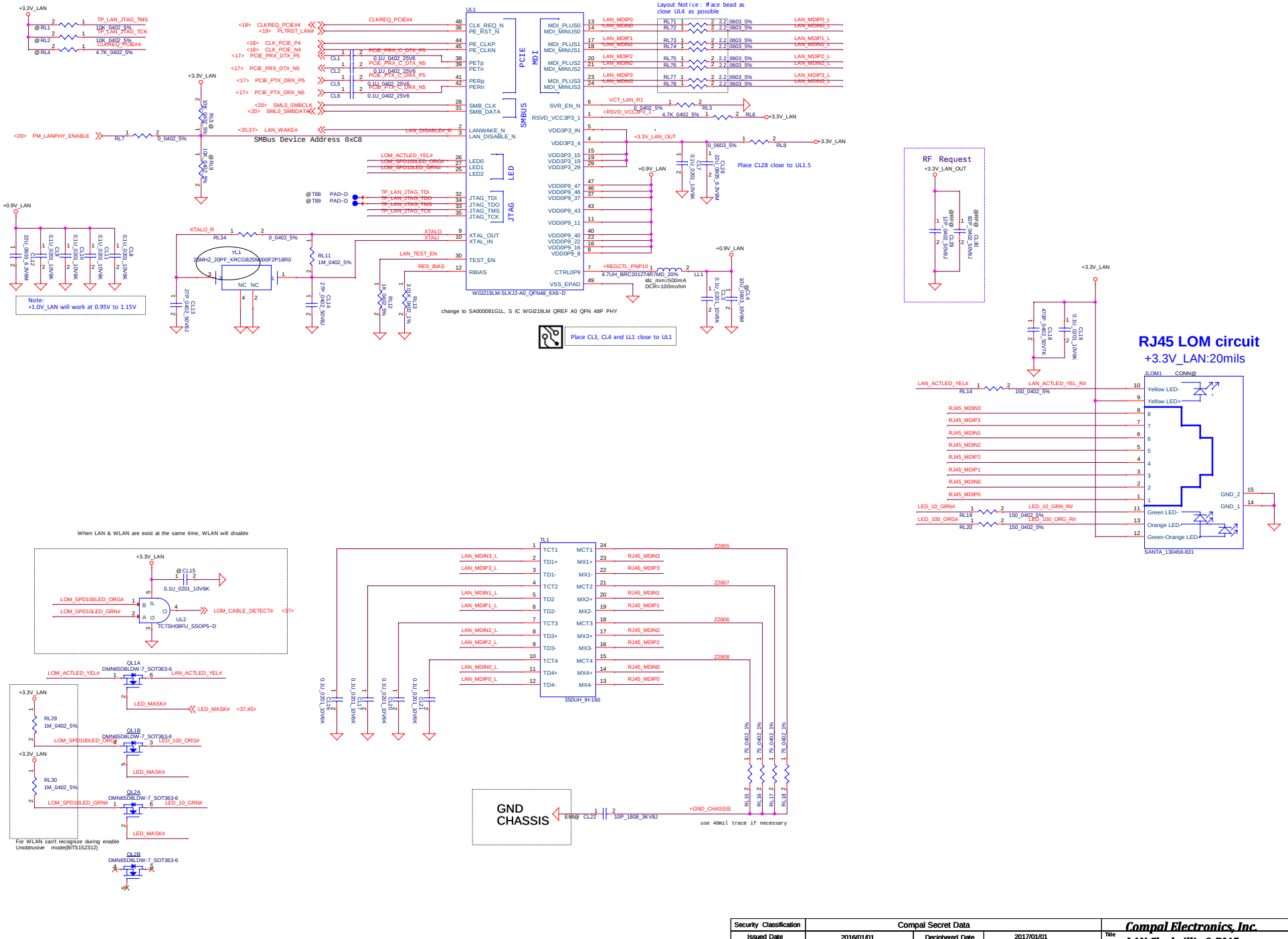
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size	Document Number	Rev
C	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 32 of 63



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc. LAN Clarkvillie & RJ45
Size	C
Document Number	LA-F711P
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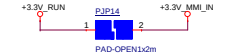
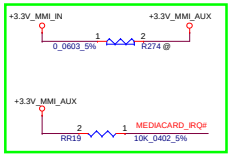
Date:	Thursday, January 18, 2018
Sheet	33 of 63

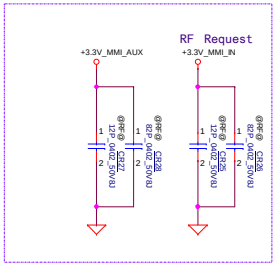
For PCIE Interface

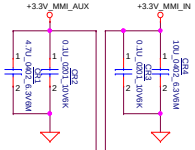


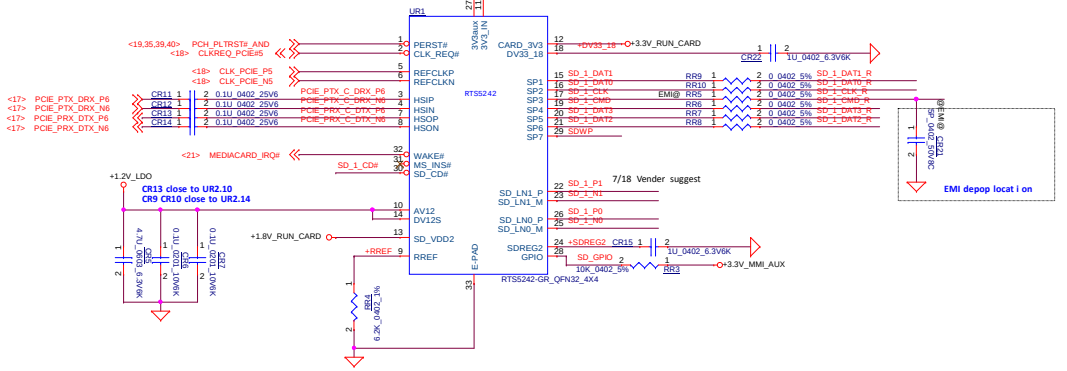


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)

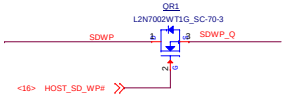
7/18 Vender suggest.

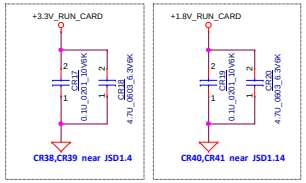


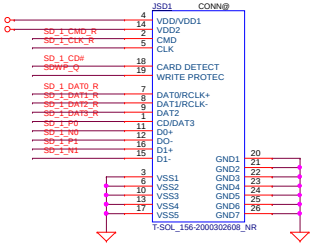




HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)







LINK SP070011U00 DONE

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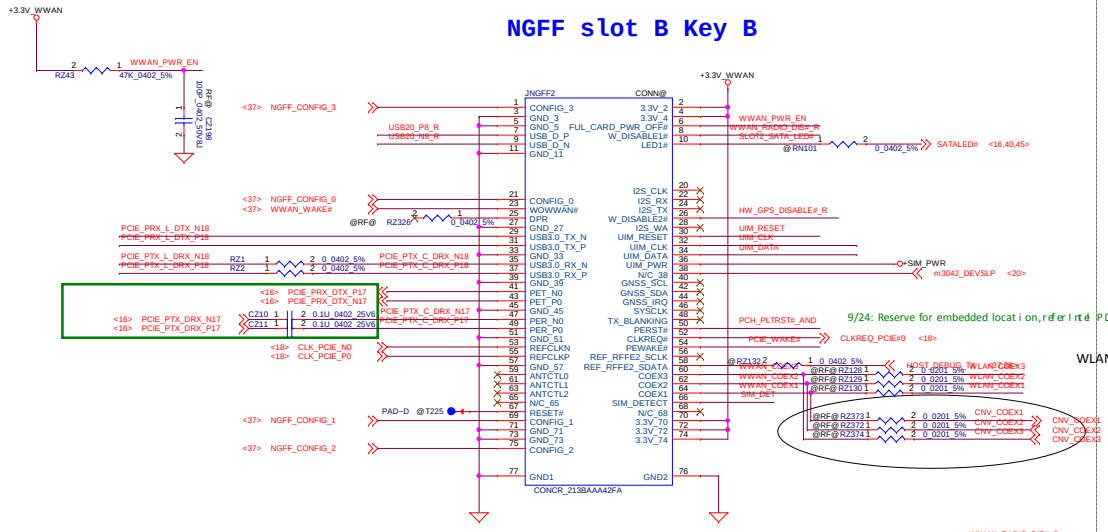
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

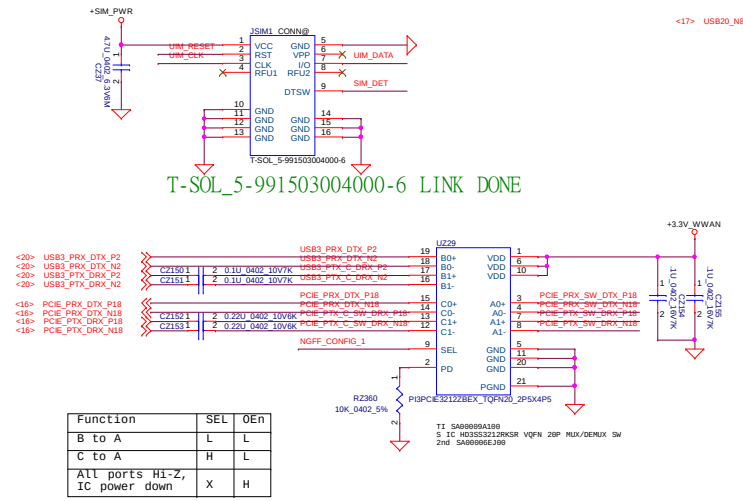
Compal Electronics, Inc.			
Title: Card Reader			
Size: C	Document Number: LA-F711P		Rev: 0.5
Date: Thursday, January 18, 2018		Sheet 34 of 63	

NGFF slot B Key B



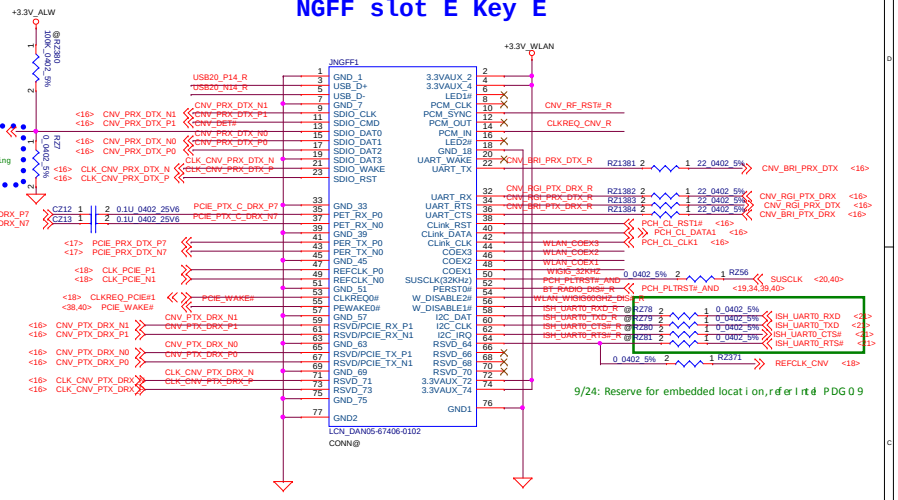
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

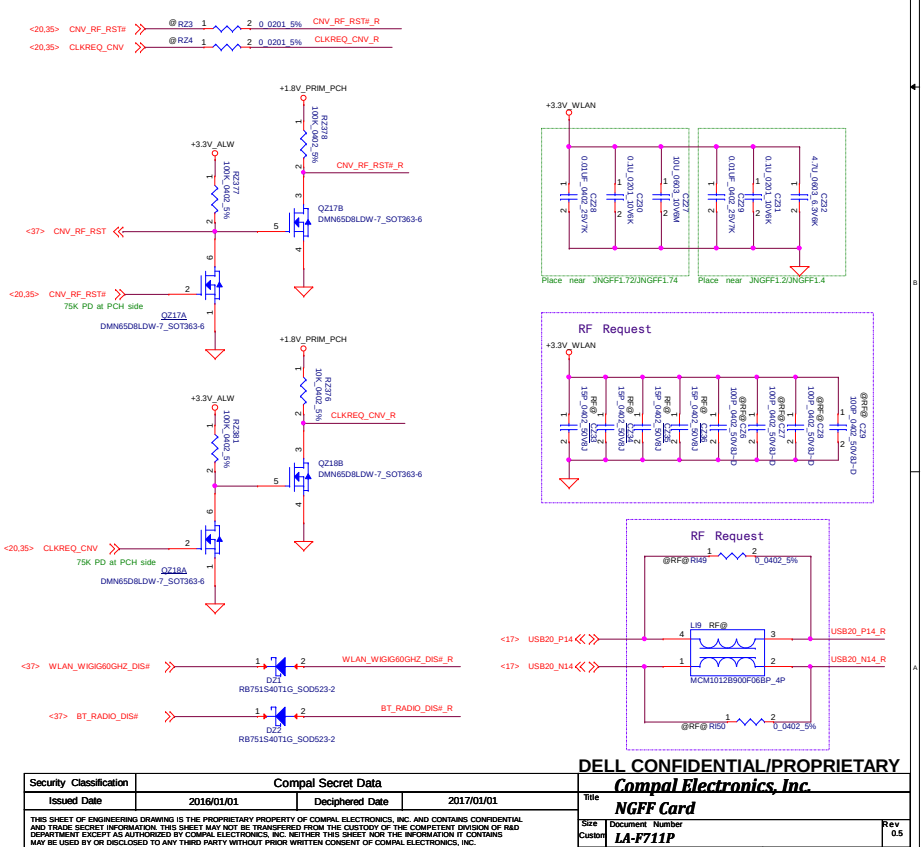
SIM Card Push-Push



Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

NGFF slot E Key E





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: NGFF Card

Size	Document Number	Rev
Custom	LA-F711P	0.5
Date: Thursday, January 18, 2018	Sheet 35 of 63	

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1

ACES_50278-00401-001

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

EM5209VF_DFN14_3X2

place at AGND and DGND plane

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

ALC3246-CG_MQFN48_6X6

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Only BR15U UMA use LA2,LA3,because 6L

Normal Open

SINGA_2SJ3095-059111F

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Compal Electronics, Inc.

Codec ALC3246

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Size	Document Number	Rev
C	LA-F711P	0.5
Date:	Thursday, January 18, 2018	Sheet 36 of 63

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

RF Request

close to pin G8/M9

Close to pin H1

Close to pin N5

Deep Sleep support

non Deep Sleep	1
Deep Sleep	0

VGA_ID0

Discrete	0
UMA	1

must to check H_PROCHOT# with PWR team

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

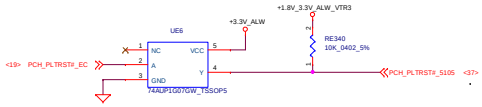
Compal Electronics, Inc.

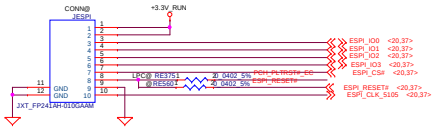
Title: EC MEC5105

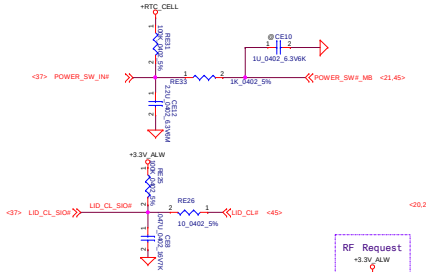
Size: Custom | Document Number: LA-F711P | Rev: 0.5

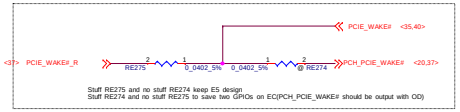
Date: Thursday, January 18, 2018 | Sheet 37 of 63

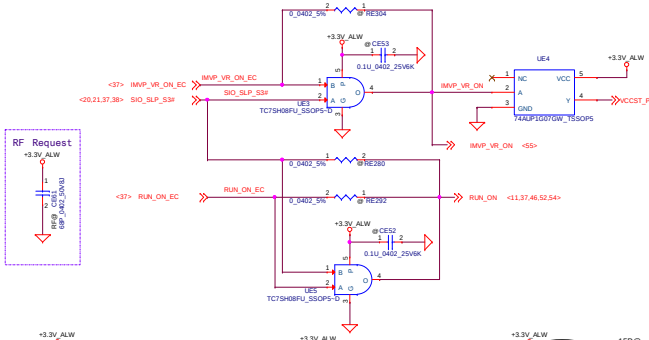
For BR UMA



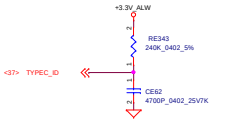






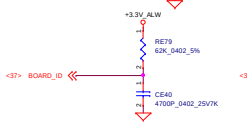


RF Request



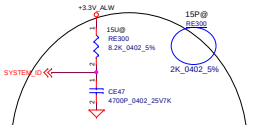
RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise ti me is measured from 5%~68%



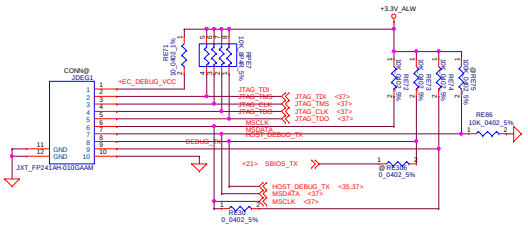
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
* 62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
4.3K	4700p	A00
2K	4700p	
1K	4700p	

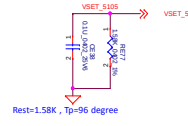
BOARD_ID rise ti me is measured from 5%~68%

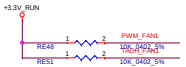


RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	BR15 H
* 4.3K	4700p	17"
* 2K	4700p	BR15 P
1K	4700p	

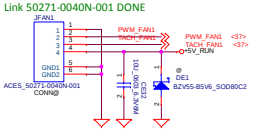
PANEL_ID rise ti me is measured from 5%~68%





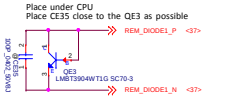


Link 50271-0040N-001 DONE

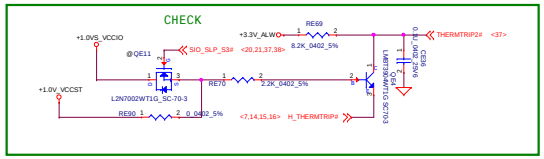


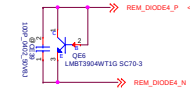
Thermal diode mapping

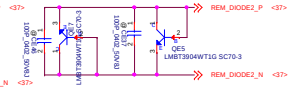
5105 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



DP2/DN2 for WiGig on QE5, place QE5 close to Type-C and CE37 close to QE5







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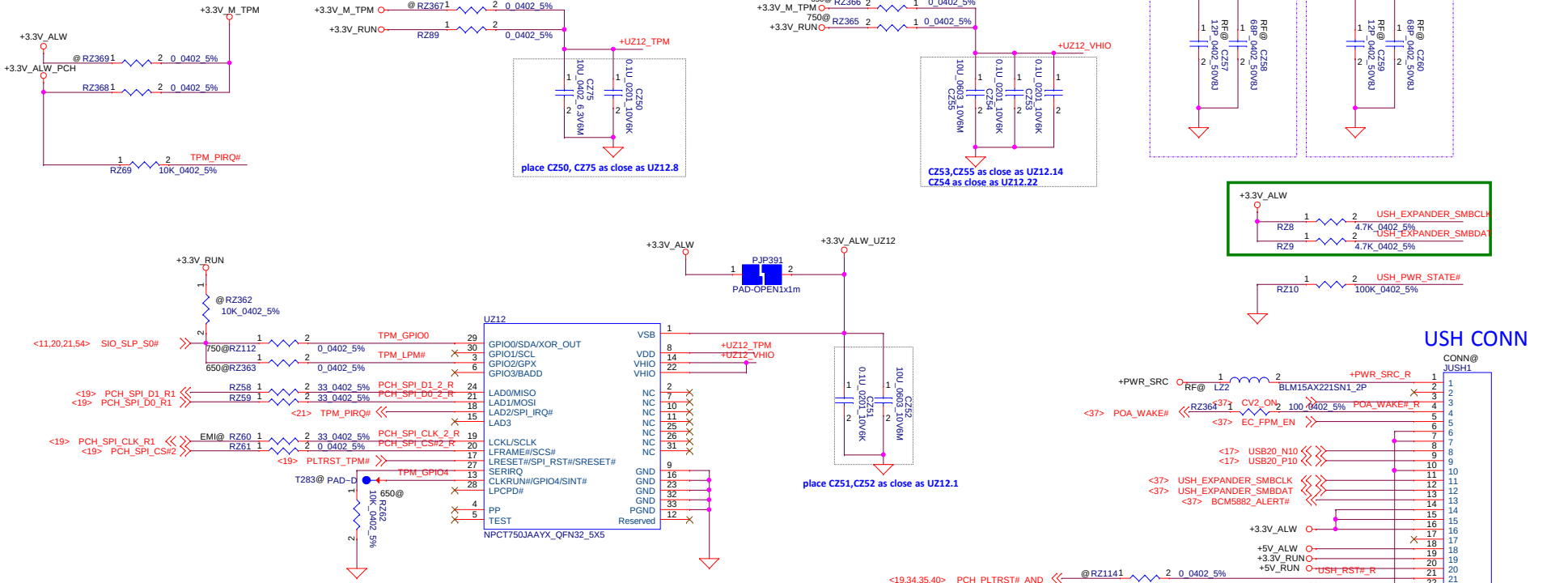
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	MEC5105 SUPPORT		
Size	Document Number		Rev
Custom	LA-F711P		0.5
Date:	Thursday, January 19, 2017	Sheet	38 of 63

For NUVOTON TPM



2018/01/04: change to MP sample : SA0000AQ220

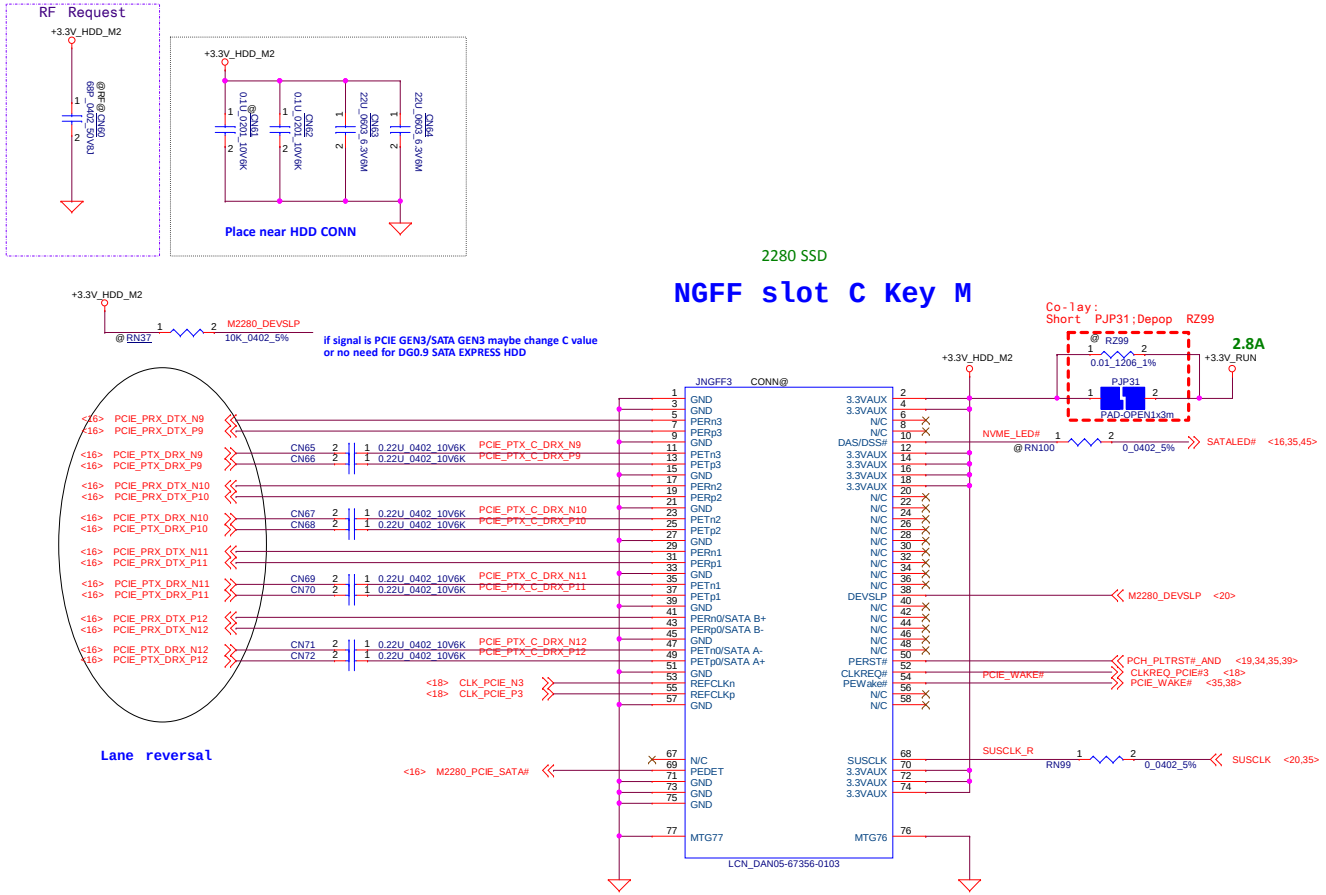
need to link SA0000AQ200

	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: USH & TPM			
Size: Custom	Document Number: LA-F711P		Rev: 0.5
Date: Thursday, January 18, 2018		Sheet 39 of 63	

For Breckenridge 15



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Security Classification	Compal Secret Data	
Issued Date	2016/01/01	Deciphered Date 2017/01/01

Compal Electronics, Inc.

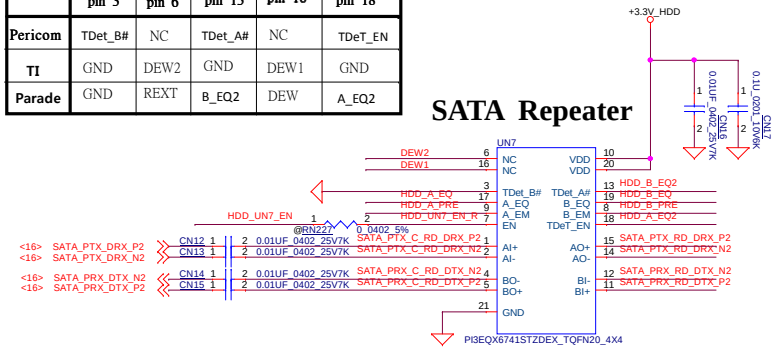
Title: M2 2280 Socket

Size	Document Number	Rev
B	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 40 of 63

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

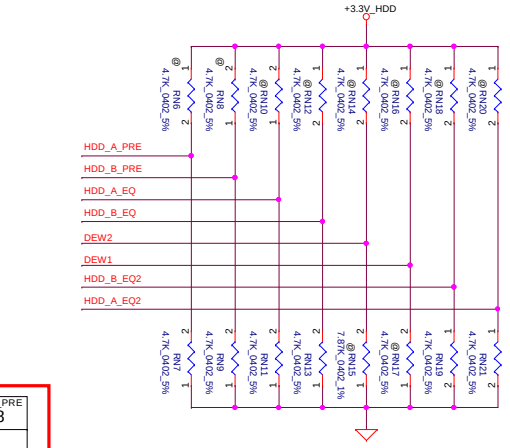
SATA Repeater

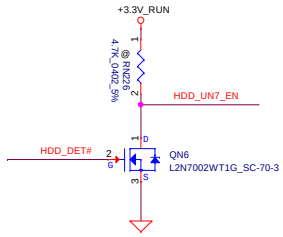


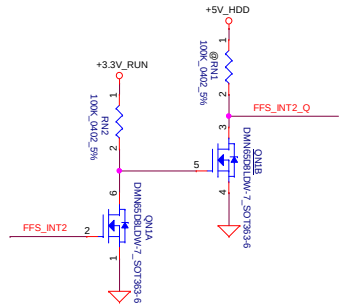
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2)	A_EQ	B_EQ		A_EM	B_EM
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-6dB	-6dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

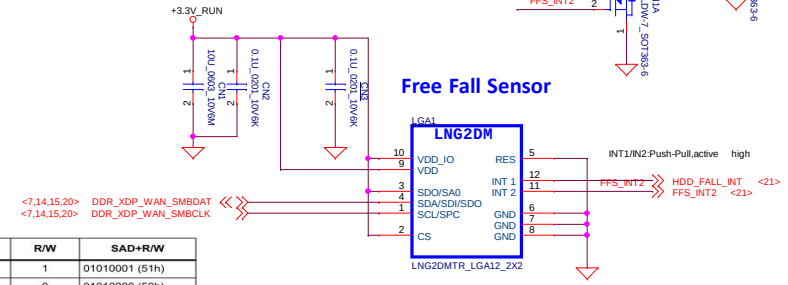
* red color is current setting

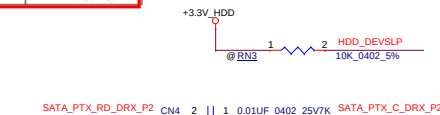


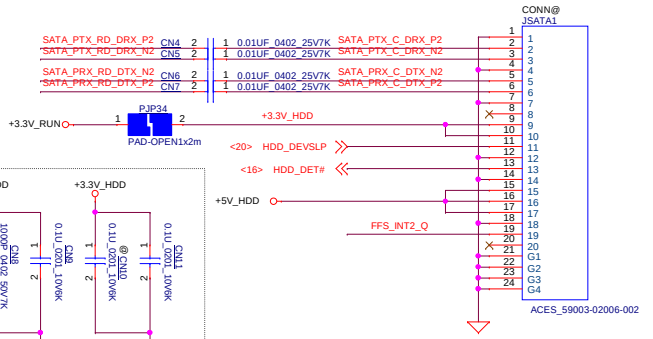


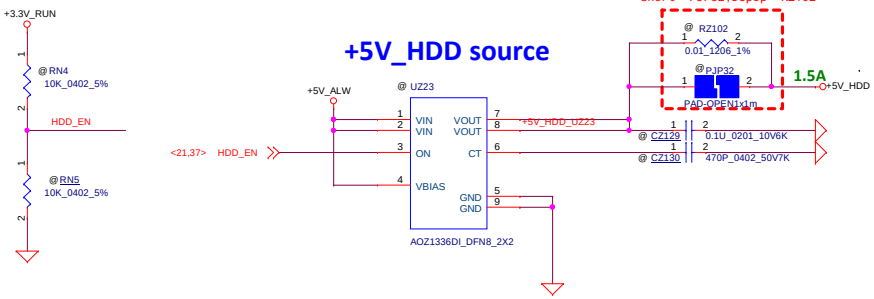


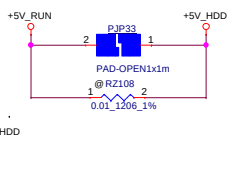
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)











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Issued Date	2016/01/01	Deciphered Date 2017/01/01

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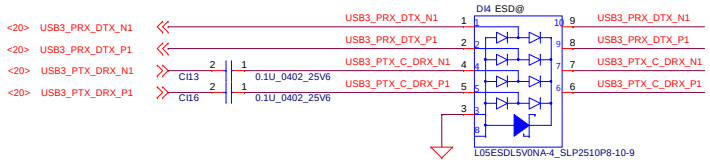
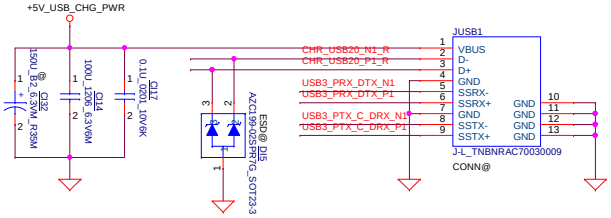
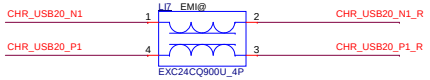
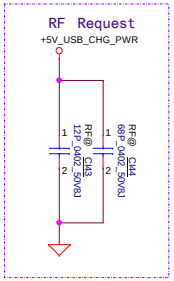
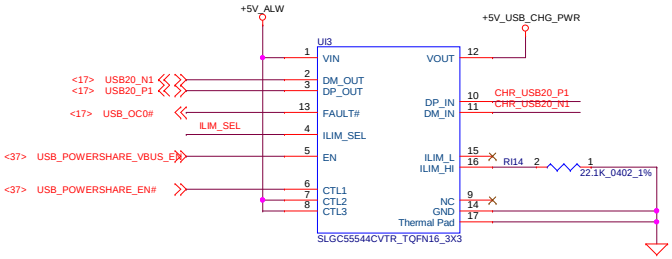
For PWR SW + Charger combine IC

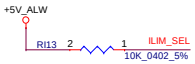


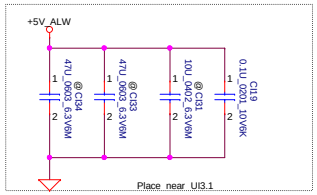












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Compal Electronics, Inc.

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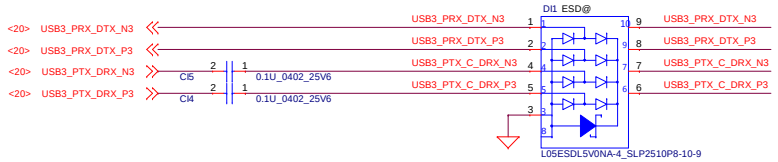
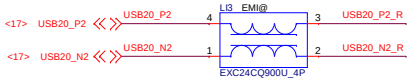
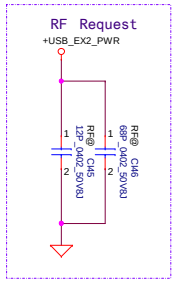
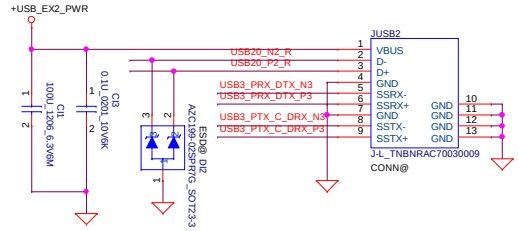
For Breckenridge 14&15/Steamboat 14

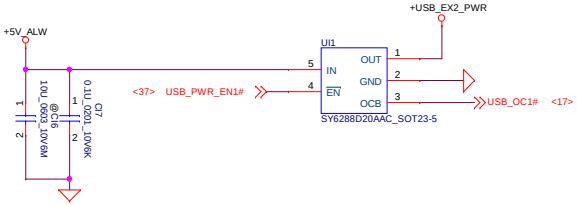


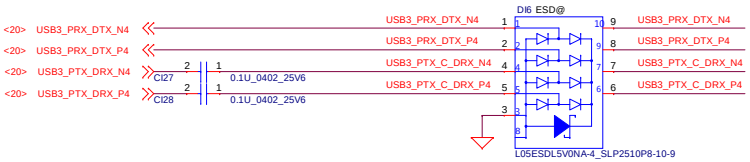


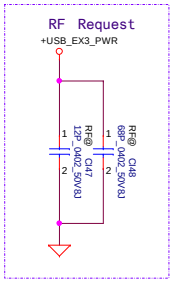


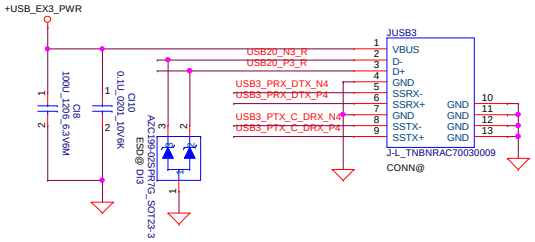


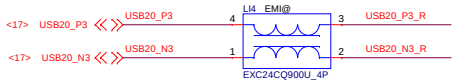
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

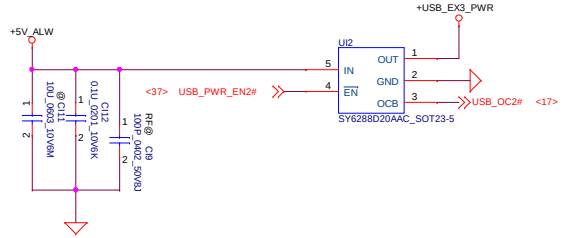












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Compal Electronics, Inc.

Title: JUSB2&JUSB3

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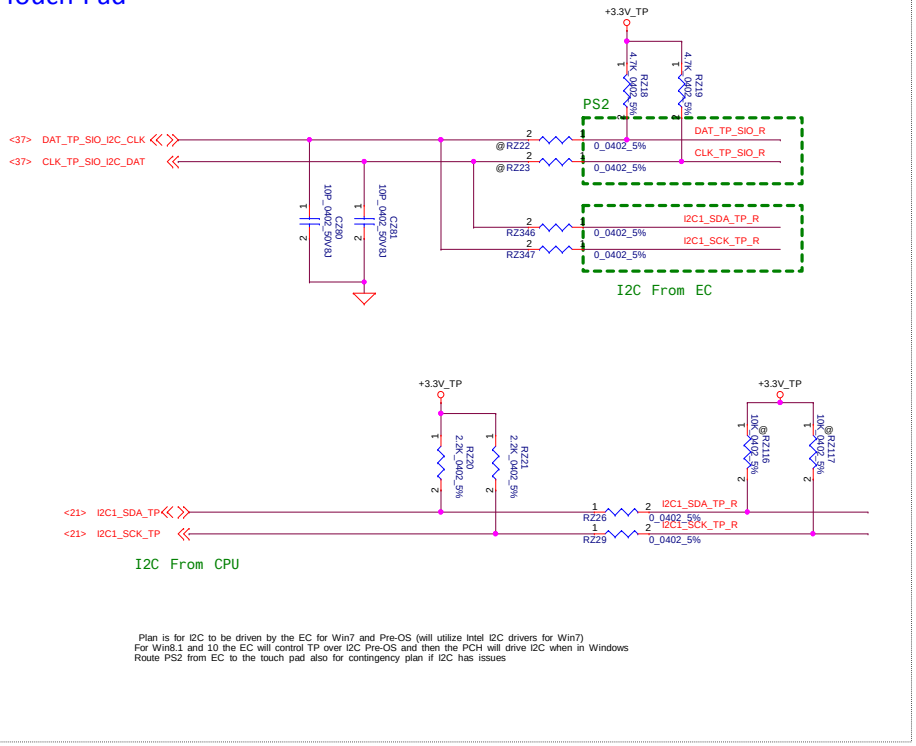
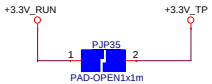
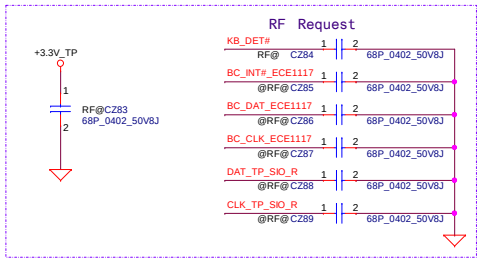
Touch Pad

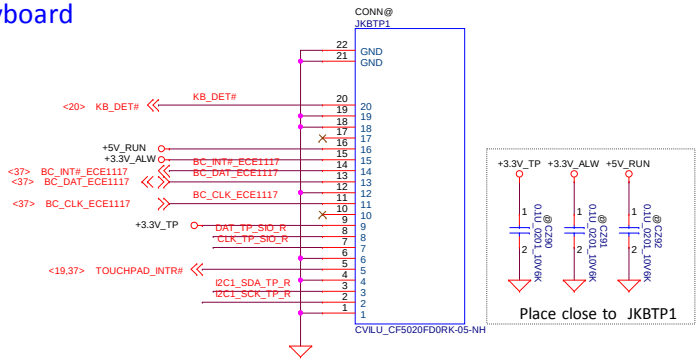


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

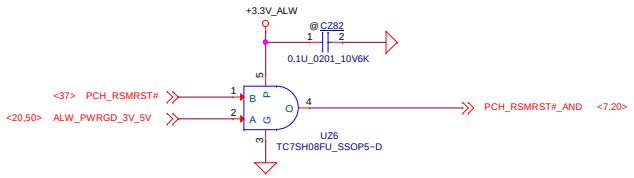




Keyboard



RSMRST circuit



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title	*Keyboard*	
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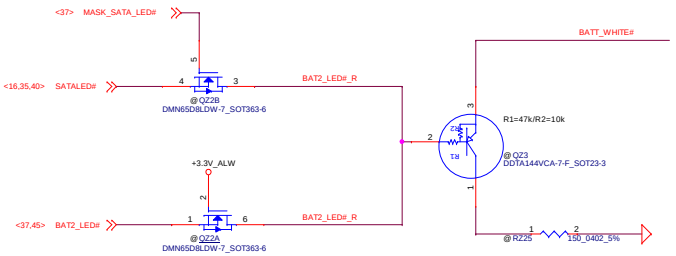
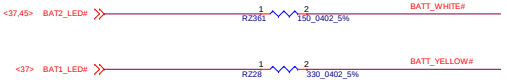
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key " Fn+H"

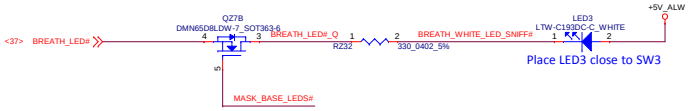


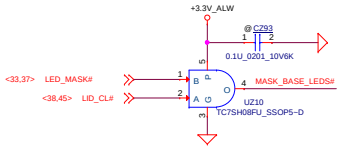
Bat tery LED



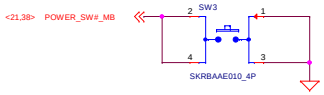
Breath LED

LED P/N change to SCS0000FL00 from SCS0000BA00

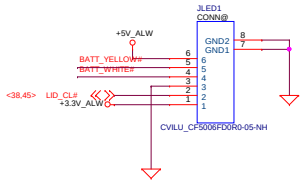




POWER & INSTANT ON SWITCH



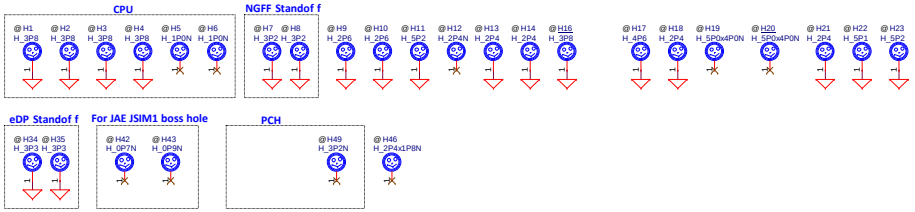
LED board CONN



Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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Title: PAD, LED

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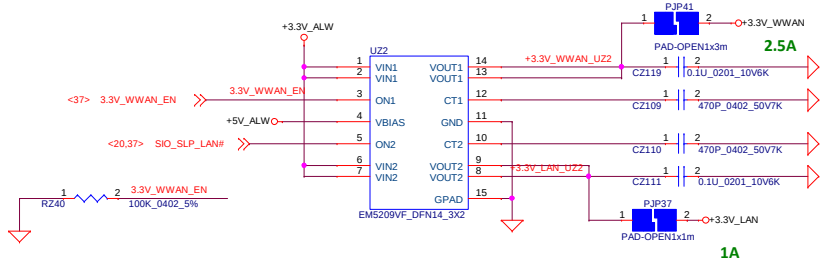
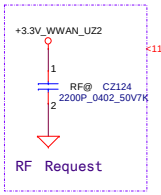
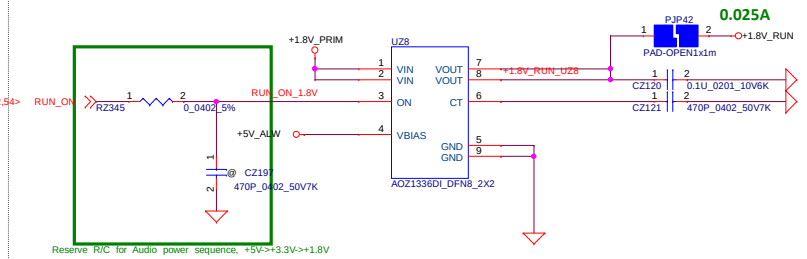
+3.3V_WWAN/+3.3V_LAN source

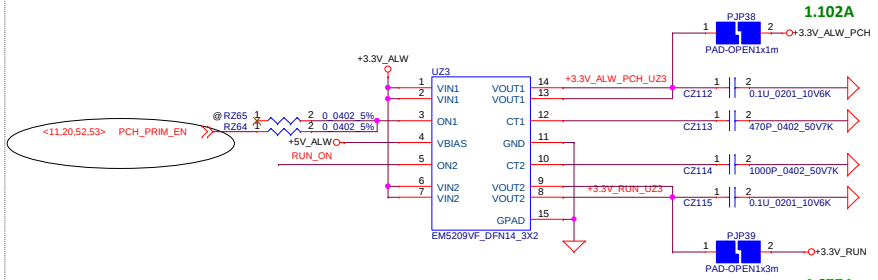


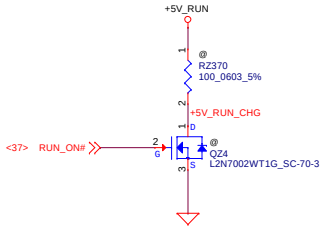


+1.8V_RUN source



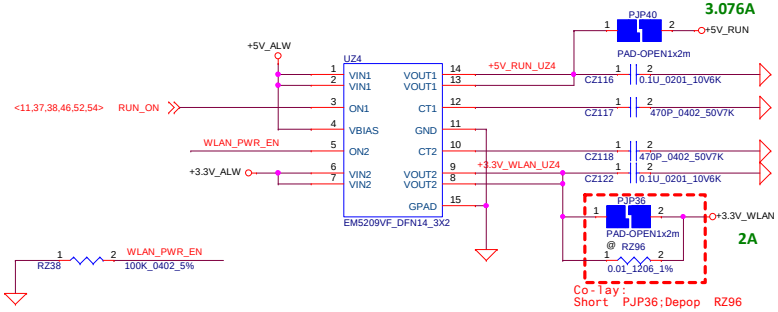
+3.3V_ALW_PCH/+3.3V_RUN source

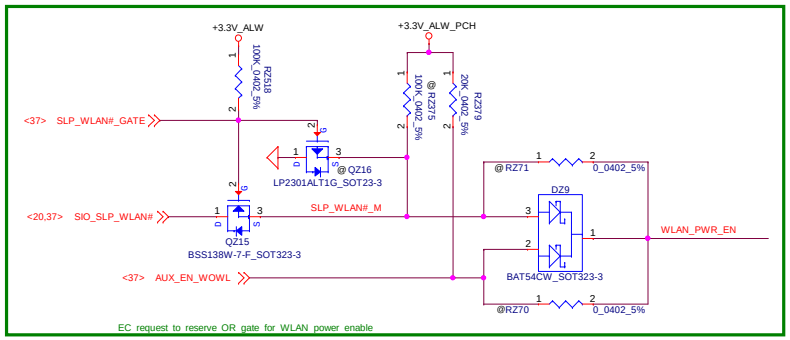




Reserve for S3 no power issue (+5V_RUN discharge circuit)

+5V_RUN/+3.3V_WLAN source





Security Classification	Compal Secret Data		
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Title: Power control

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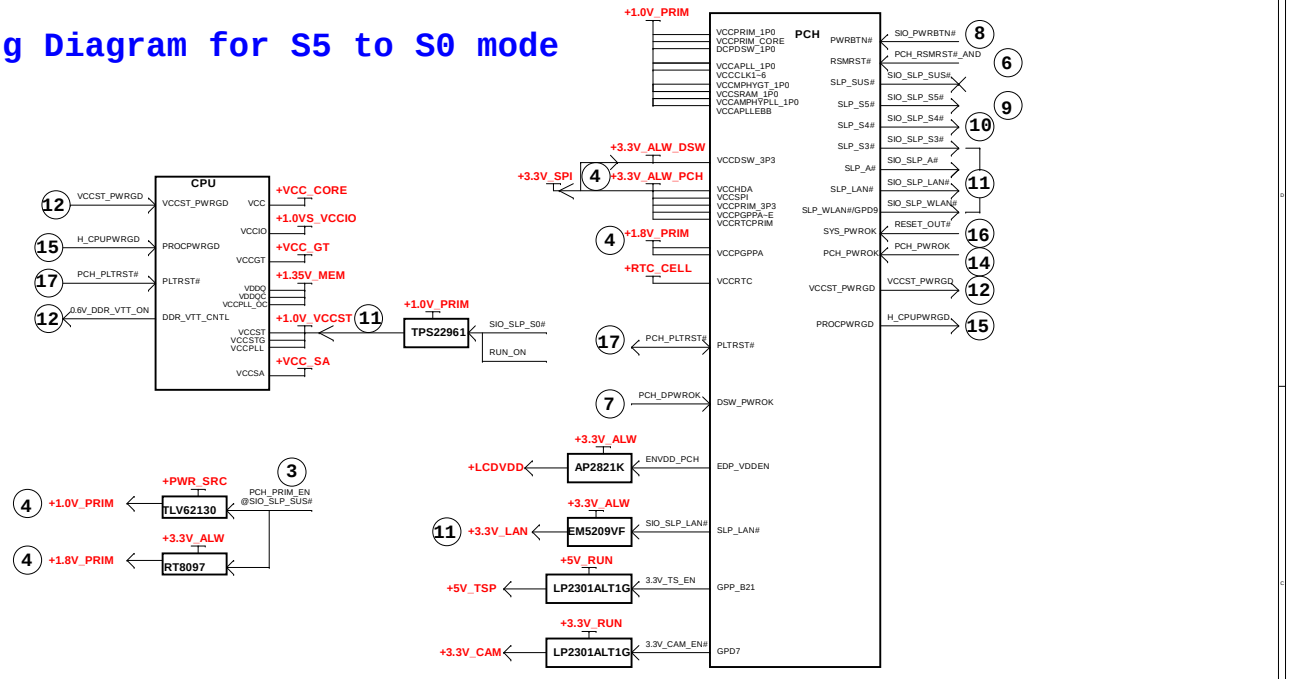
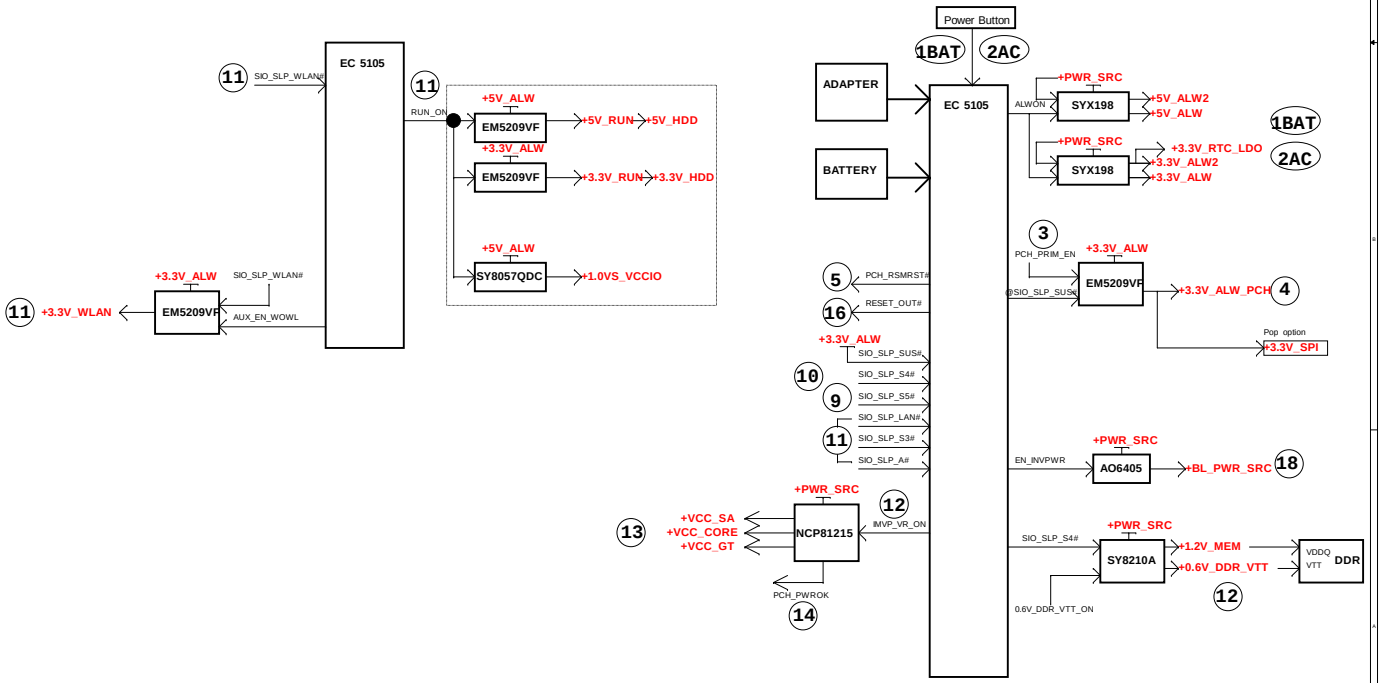
Timing Diagram for S5 to S0 mode





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: LA-F711P | Rev: 0.5

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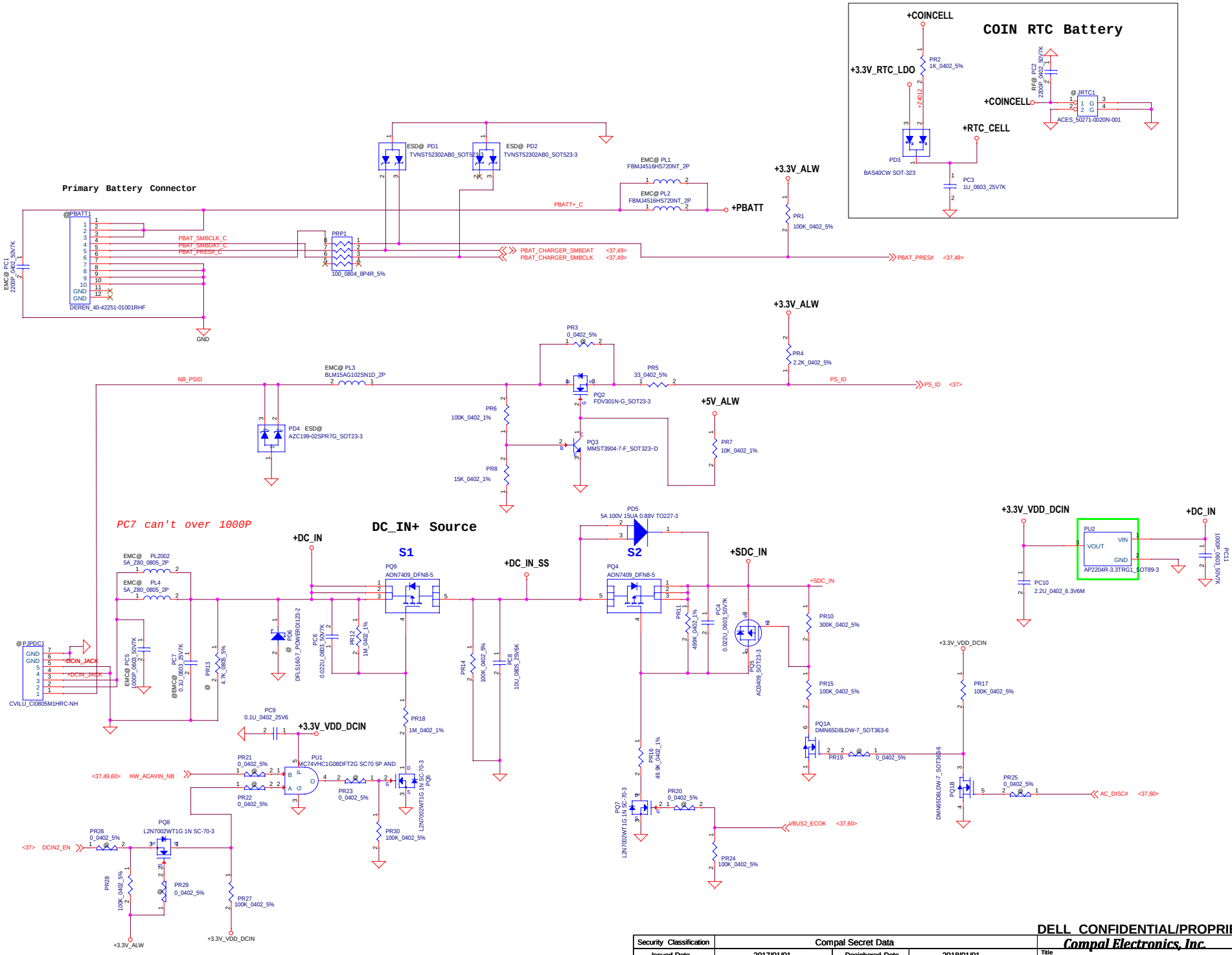

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Compal Electronics, Inc.

Title: +DCIN

Size	Document Number	Rev
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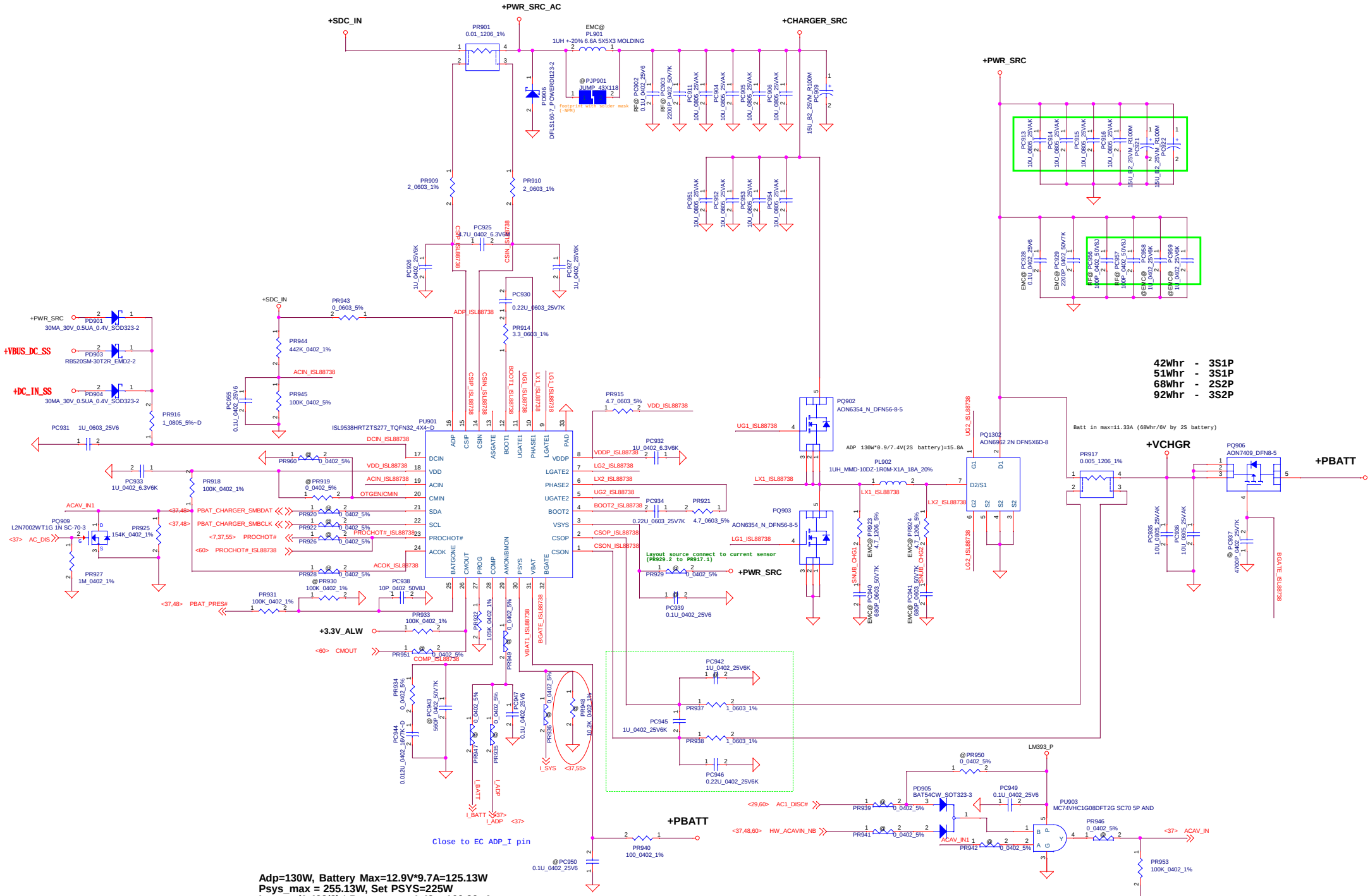

Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

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Compal Electronics, Inc.

Title: *PWR_CHARGER_ISL9237 (Colay)*

Size	Document Number	Rev
Custom	*LA-F711P*	0.5

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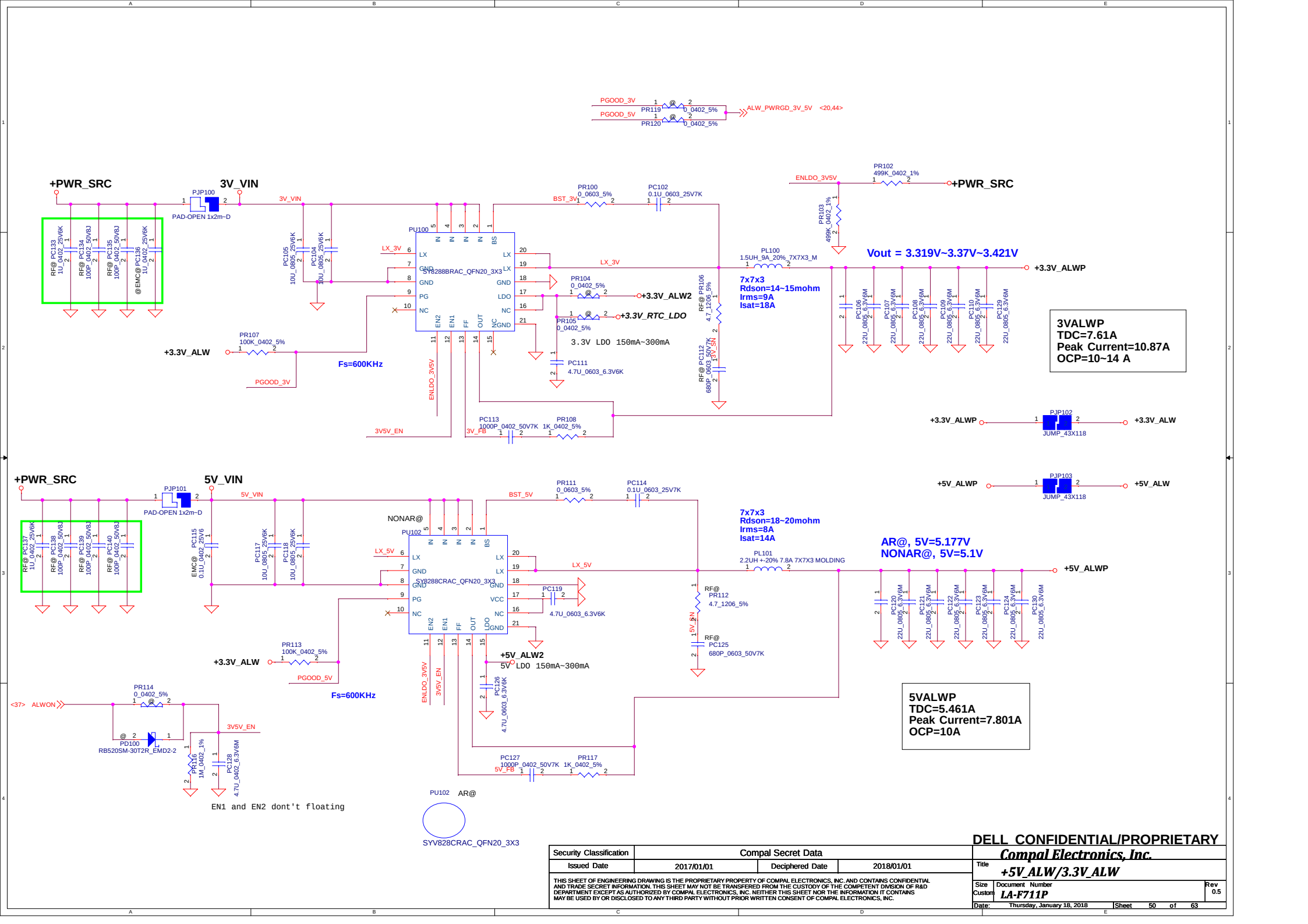

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Issued Date	2017/01/01	Deciphered Date	2018/01/01

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Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size	Document Number	Rev
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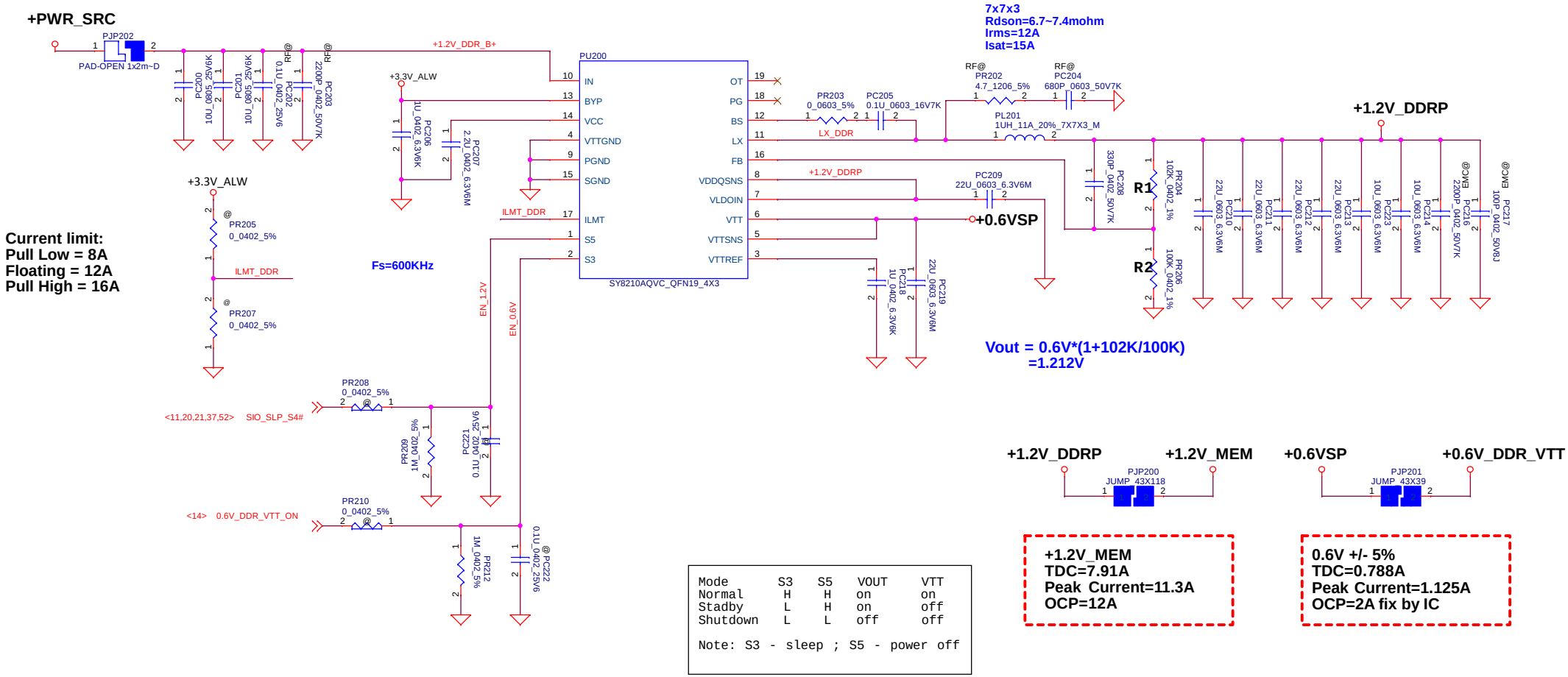

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_MEM
TDC=7.91A
Peak Current=11.3A
OCP=12A

0.6V +/- 5%
TDC=0.788A
Peak Current=1.125A
OCP=2A fix by IC

Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size: Custom | Document Number: LA-F711P | Rev: 0.5

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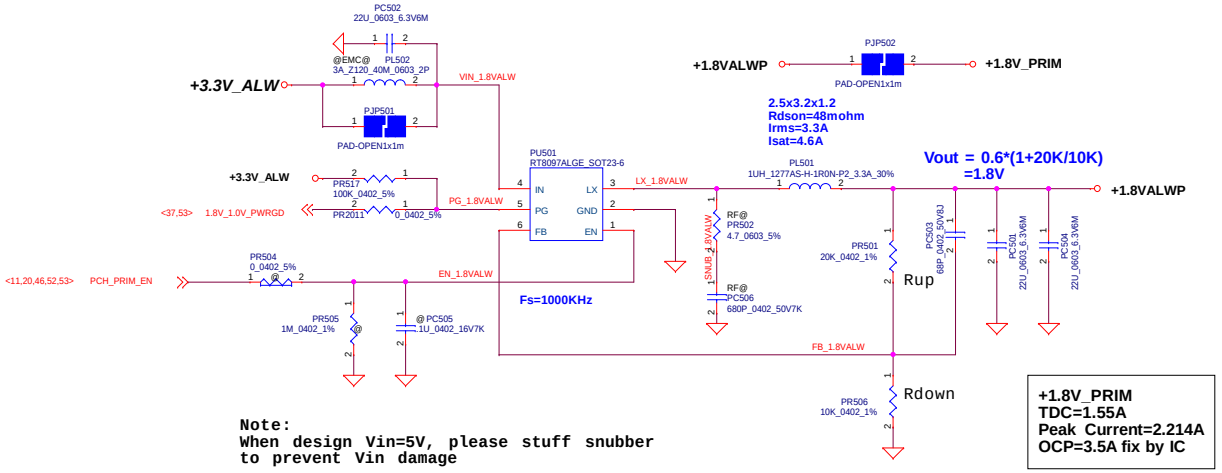
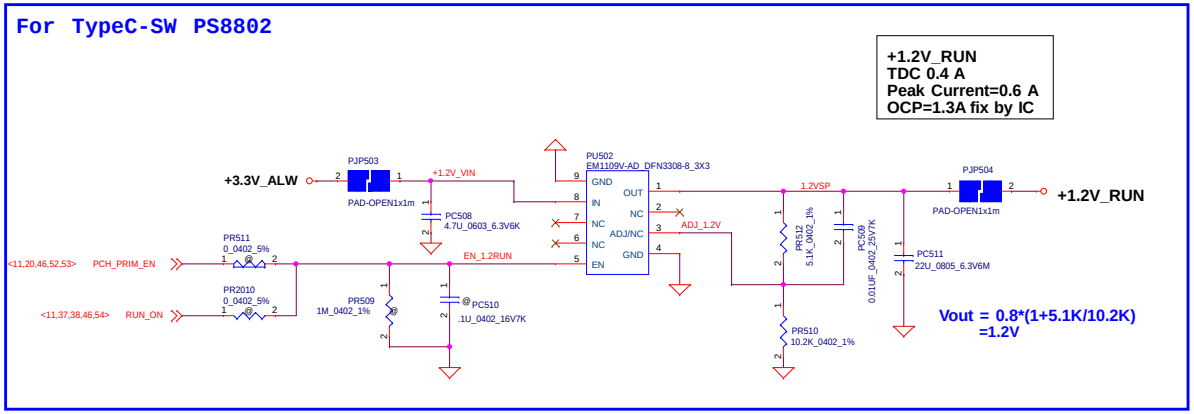
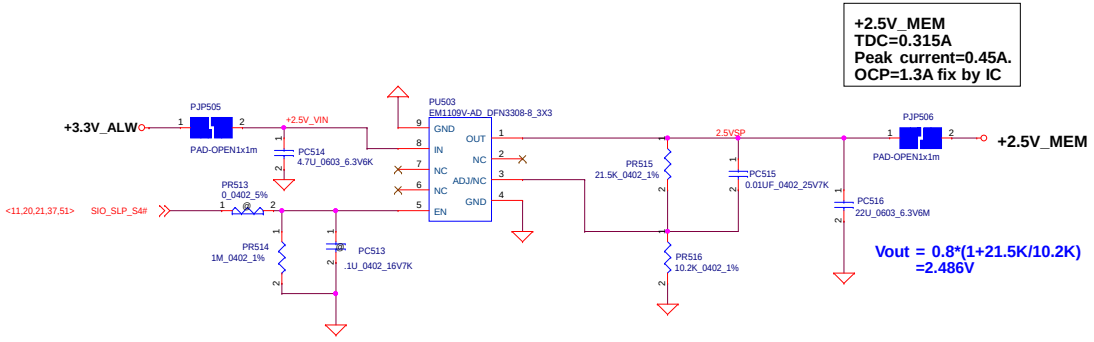


For TypeC-SW PS8802





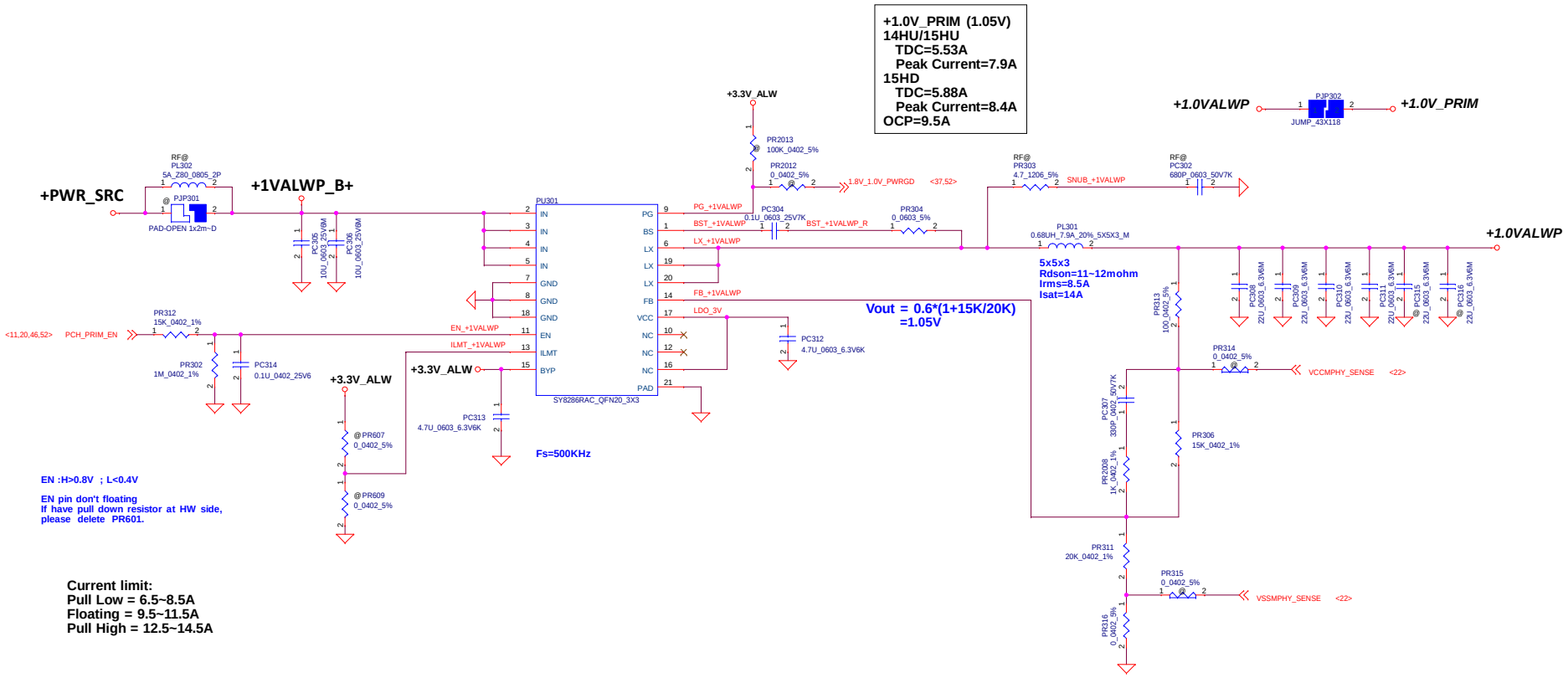
Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: +1.8VALWP/+1.2V_RUN/2.5V_MEN

Size	Document Number	Rev
C	LA-F711P	0.5

Date: Thursday, January 18, 2018 | Sheet 52 of 63



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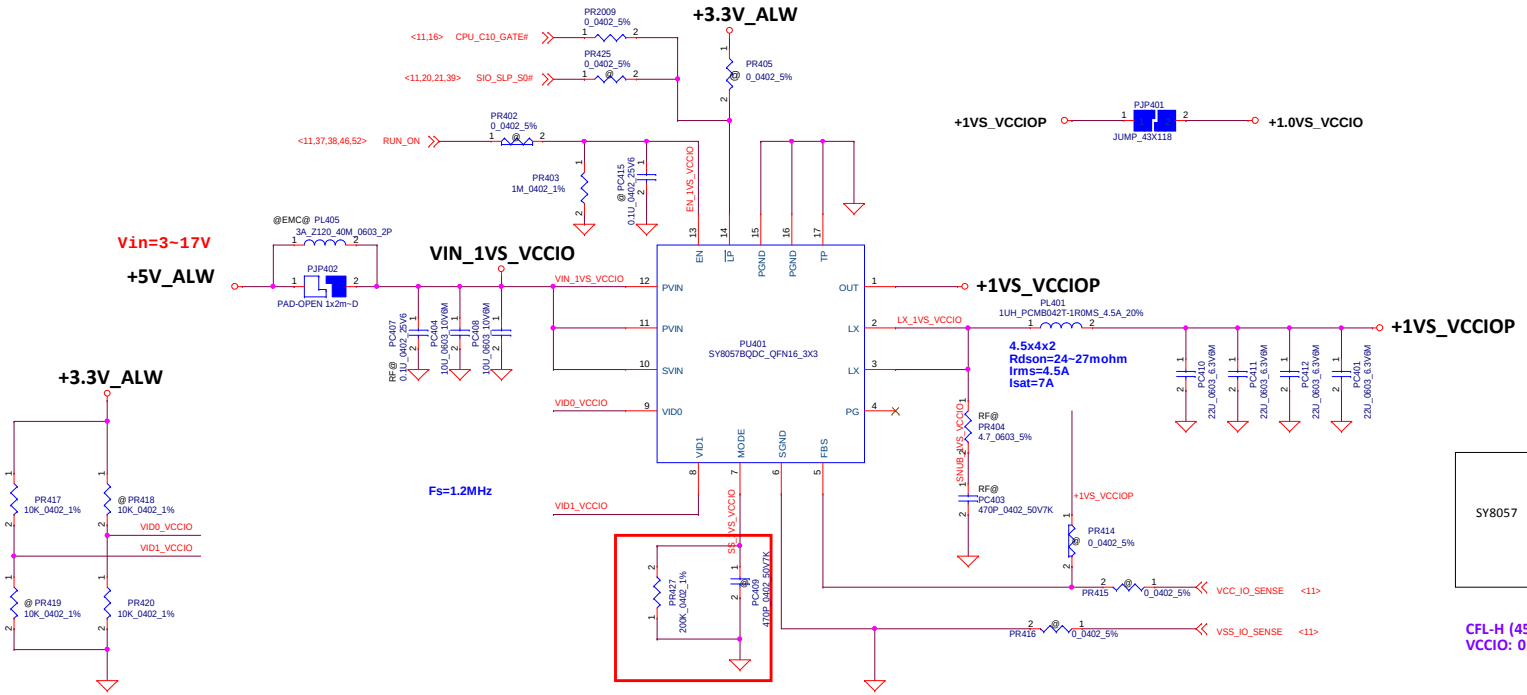
Compal Electronics, Inc.		
Title: +1VALWP		
Size	Document Number: LA-F711P	Rev: 0.5
Date: Thursday, January 18, 2018	Sheet 53 of 63	



+1.0VS_VCCIO
Peak Current=6.4A

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
SY8057	0	X	X	0(LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

CFL-H (45W)
VCCIO: 0.95V, Max current=6.4A

Preset the different pull down resistor to choose the required power rail

(VCCIO/PCH/EDRAM/EOPIO applications.)
RMODE>500k or floating = Vcc_PRIM_CORE.
RMODE=200k = Vcc_IO.
RMODE=0 = Vcc_EDRAM.

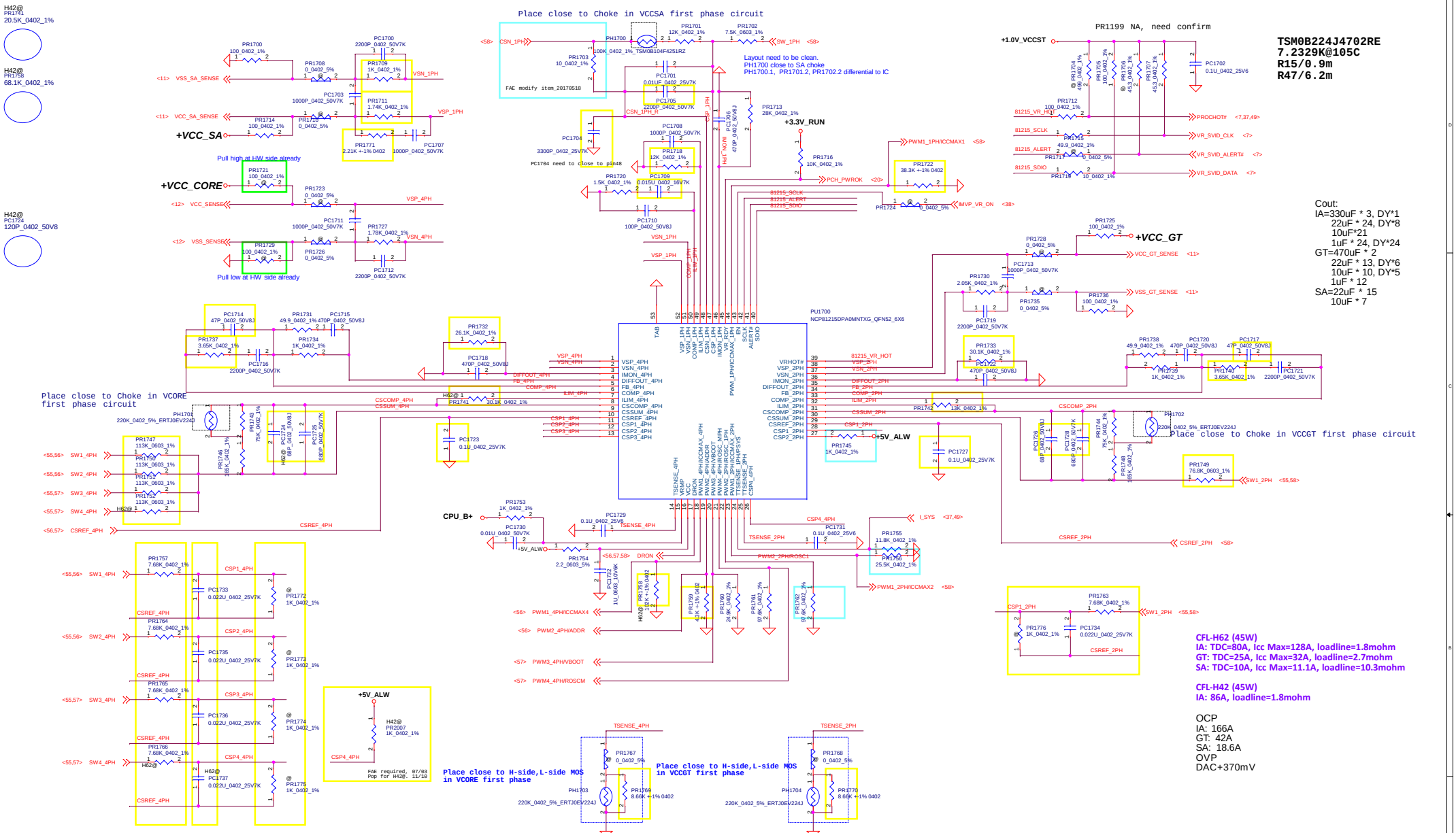
Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: +1VS_VCCIO

Size	Document Number	Rev
C	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 54 of 63

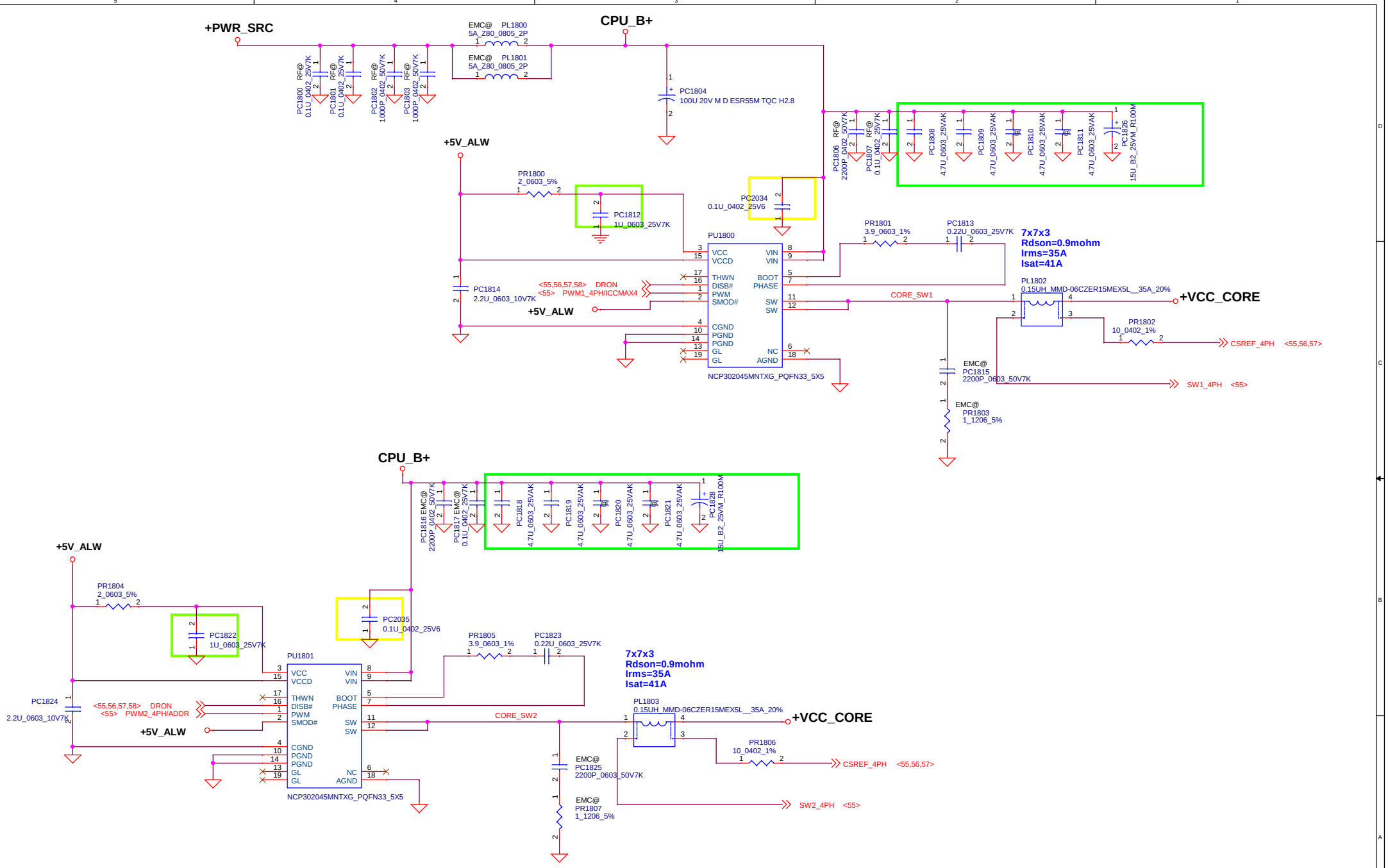


Compal Electronics, Inc.

Title: NCP81215

Size: | Document Number: LA-F711P | Rev: 0.5

Date: Thursday, January 18, 2018 | Sheet 55 of 63



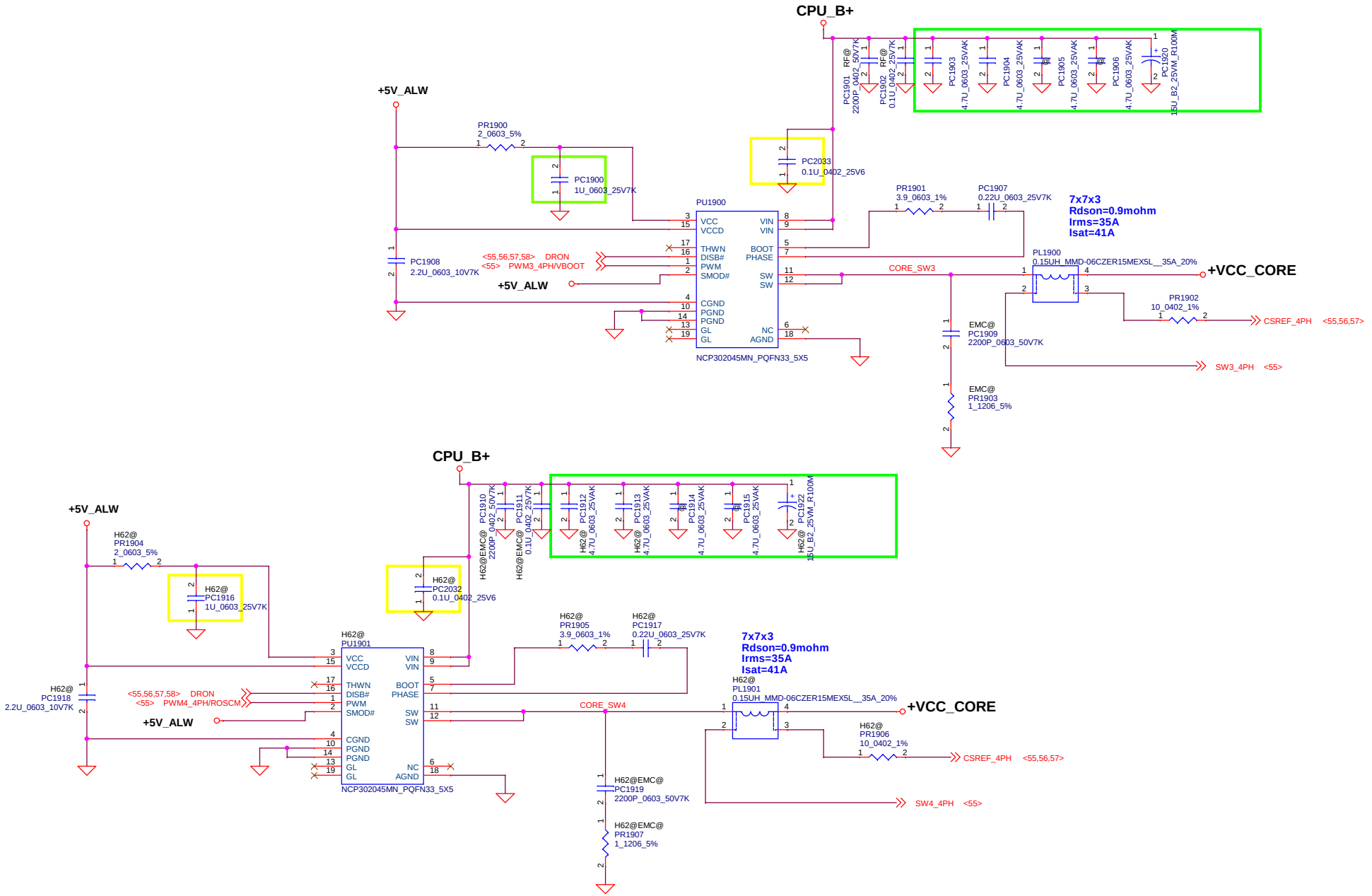
Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: **+VCC_CORE_Phase1&2**

Size	Document Number	Rev
	LA-F711P	0.5

Date: Thursday, January 18, 2018 | Sheet 56 of 63



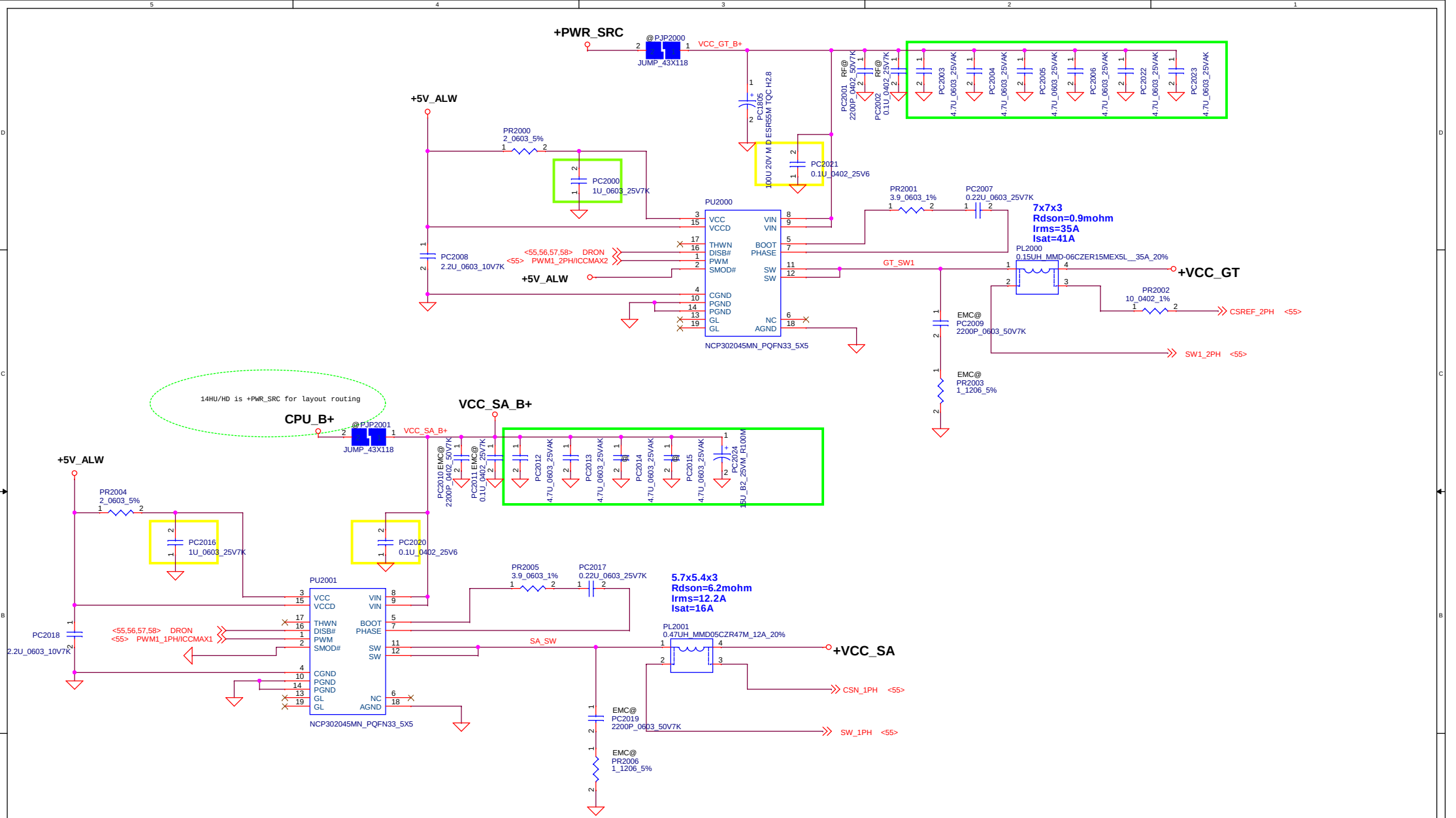
Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: +VCC_CORE_Phase3&4

Size	Document Number	Rev
	LA-F711P	0.5

Date: Thursday, January 18, 2018 | Sheet 57 of 63



Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: **+VCC_GT/+VCC_SA**

Size	Document Number	Rev
	LA-F711P	0.5

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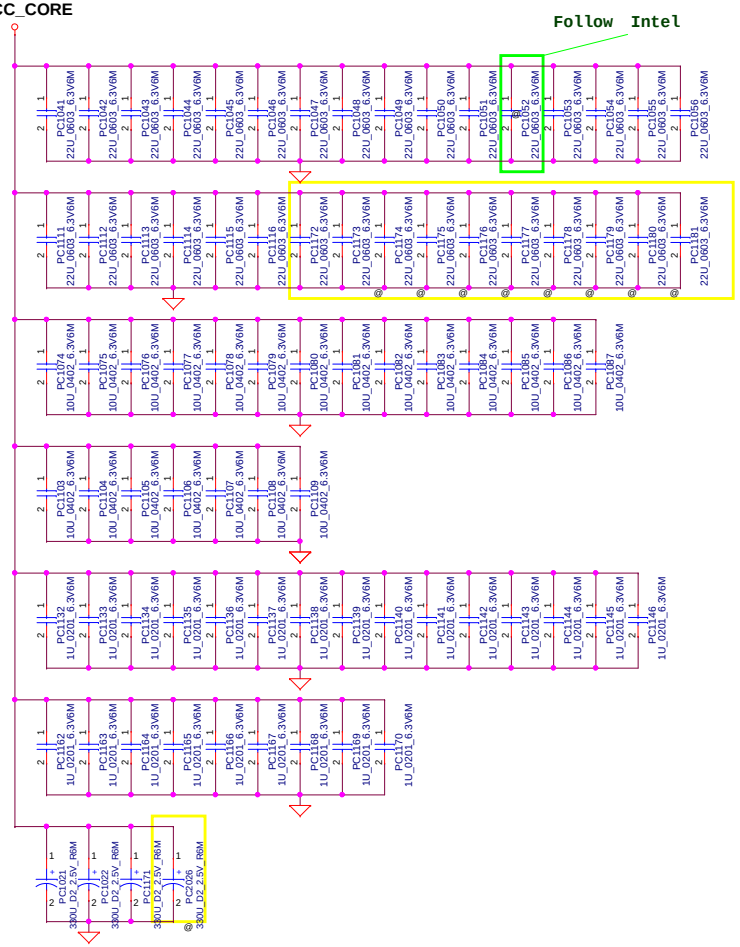
VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs + 10U_0402*21 pcs + 1U_0201*24 pcs
Primary Side.
22U_0603 * 11 pcs+330u_D2*3 pcs

+VCC_CORE

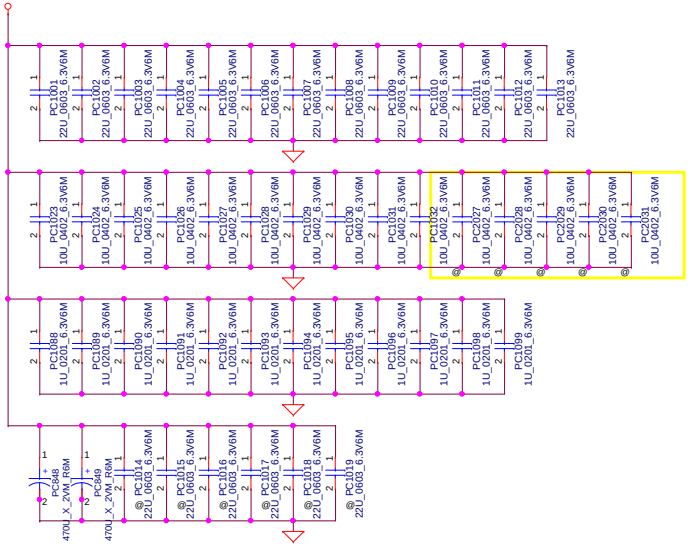
Follow Intel



Cout:
IA=330uF * 3, DY*1
22uF * 24, DY*8
10uF*21
1uF * 24, DY*24
GT=470uF * 2
22uF * 13, DY*6
10uF * 10, DY*5
1uF * 12
SA=22uF * 15
10uF * 7

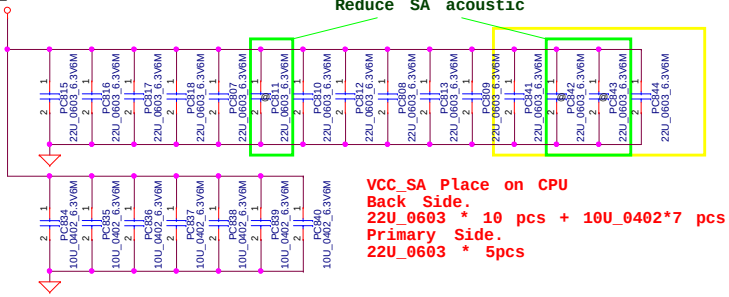
VCC_GT Place on CPU
Back Side.
22U_0603 * 6 pcs +10U_0402*10 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 7 pcs +470u_D2*2 pcs

+VCC_GT



+VCC_SA

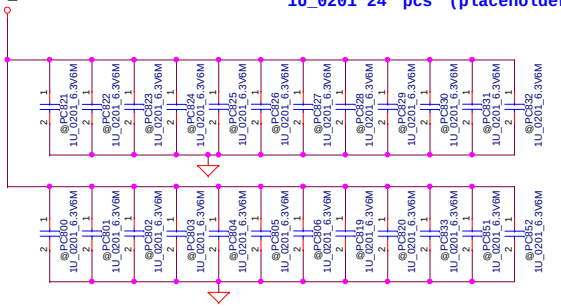
Reduce SA acoustic



VCC_SA Place on CPU
Back Side.
22U_0603 * 10 pcs + 10U_0402*7 pcs
Primary Side.
22U_0603 * 5pcs

+VCC_CORE

+VCC_CORE Place on CPU
1U_0201*24 pcs (placeholder)



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Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size: Custom | Document Number: LA-F711P | Rev: 0.5

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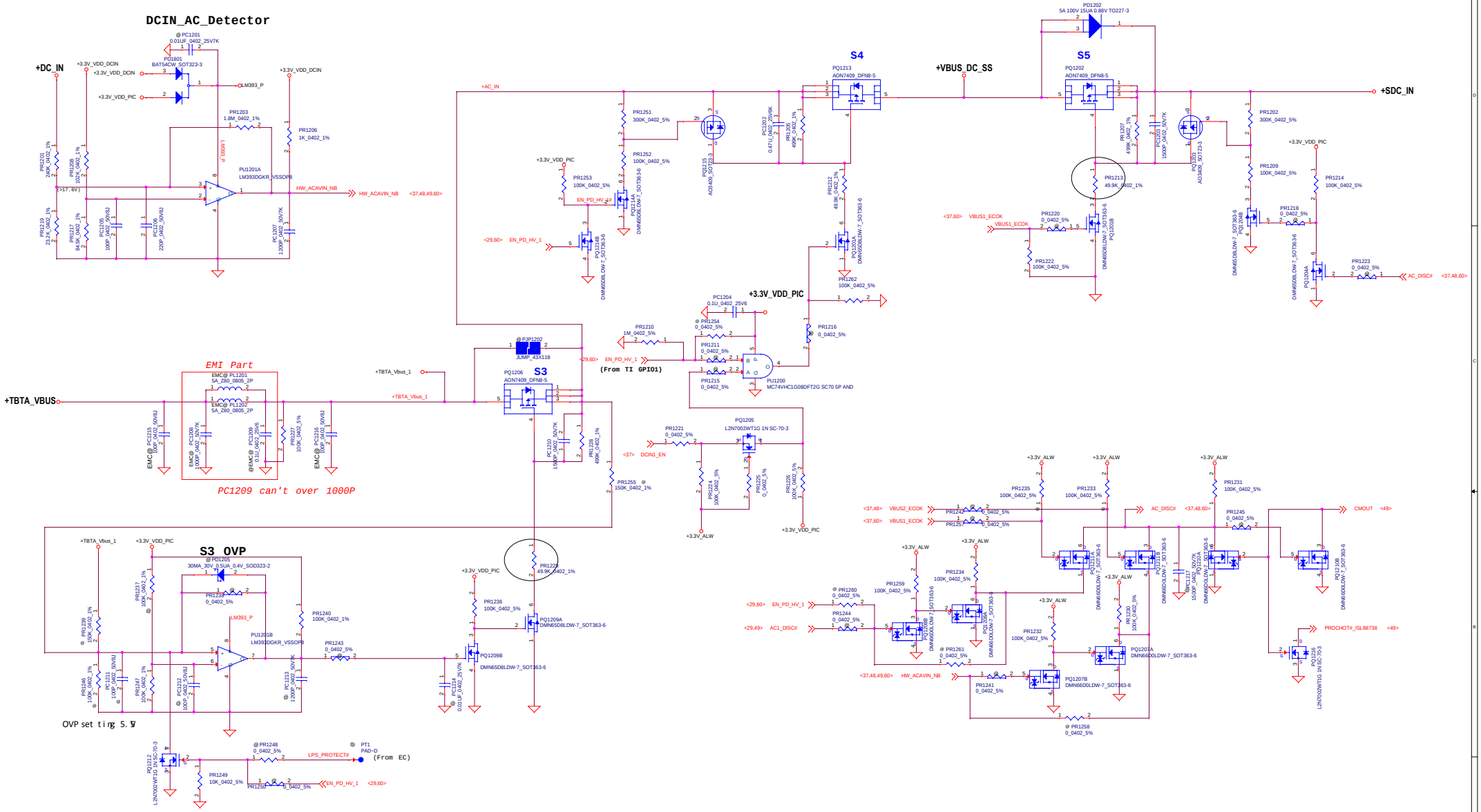


Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

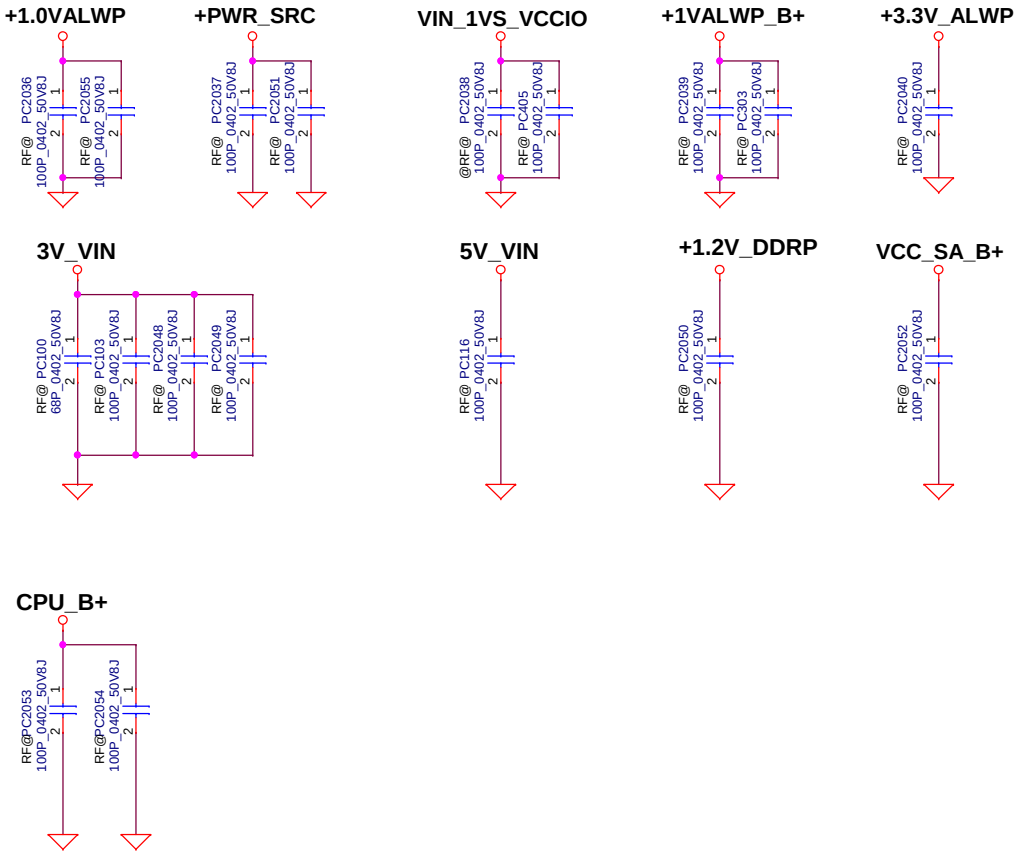
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: ParkCity_TypeC_PD

Size	Document Number	Rev
Custom	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 60 of 63



Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: **RF CAP**

Size	Document Number	Rev
B	LA-F711P	0.5

Date: Thursday, January 18, 2018 Sheet 61 of 63

Version Change List (P. I. R. List)

Item	Date	Reason for change	Description	Phase
1	2017/11/17	Follow Intel design Fine tune PSYS setting to 225W Fine tune PCH sequence	Unpop PC1052 Unpop PR948, change PR1755 to 11.8K ohm Change PR312 to 15K ohm	X02
2	2017/11/17	Update CPU VR circuit to support H42 CPU	Change PC1705 to 2.2nF, PC1726 to 68pF, PR1749 to 76.8K, PR1730 to 2.05K, PR1727 to 1.78K, Change PC1724 to 68pF for H62 Unpop PR1752, PR1766, PC1737, PC1910, PC1911, PC1912, PC1913, PC1916, PC1917, PC1918, PC1919, PC1922, PC2032, PL1901, PR1904, PR1905, PR1906, PR1907, PU1901 Pop PR2007 1K ohm	X02
3	2017/12/08	For RF requirement	Add PC2053, PC2054, PC2055	X02
4	2018/01/04	Reserve for power on sequence modified	Add PR2010 0ohm, Reserve PR2011, PR2012, modify 1.8V_PRIM_PWRGD to 1.8V_1.0V_PWRGD	X02
5	2018/01/08	Change 0ohm to Short PAD	Change PR26, PR29, PR21, PR22, PR23, PR20, PR19, PR25, PR960, PR920, PR922, PR926, PR928, PR951, PR947, PR935, PR936, PR929, PR939, PR941, PR942, PR946, PR949, PR104, PR105, PR119, PR120, PR114, PR208, PR210, PR504, PR511, PR513, PR314, PR315, PR402, PR414, PR1708, PR1710, PR1723, PR1726, PR1767, PR1768, PR1728, PR1735, PR1724, PR1717, PR1238, PR1250, PR1211, PR1215, PR1216, PR1220, PR1218, PR1223, PR1242, PR1257, PR1244, PR1241, PR1245 to short PAD	X02
		Change JUMP to NPM footprint	Change PJP901 to JUMP_43X118-NPM	

Security Classification	Compal Secret Data		
Issued Date	2017/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.			
Title	PWR P.I.R		
Size: Custom	Document Number: LA-F711P		Rev: 0.5
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	all	HW	2017/08/22	COMPAL	To avoid in-rush current caused voltage drop	1. Add soft start solution(only reserved) on QV8,QZ1 (add CV1635, CZ1200, RZ1388,RV1400) 2. Add soft start solution(only reserved) on QE15,QH7 (add CH349,RE565)" 3. reserve RV9, CV1638	0.2(X01)
2	4	HW	2017/08/22	COMPAL	do NOT to use PEG reserved for UMA	depop RC324	0.2 (X01)
3	37	HW	2017/08/22	COMPAL	board ID	Change RE79 to 130Kohm? (rev. X01)	0.2 (X01)
4	35	HW	2017/08/22	COMPAL	modify CLKREQ_CNV & detect pin circuit	1. remove DZ10 2. add RZ381, QZ18, RH618 3. add RH621, RH622, RH623, RH624 for PCH CNV_DET connect to EC GPIO054 4. depop RE562, RH330, RZ380 5. add RZ7 short to GND for Jngff1.13 6. add RE100, RE101 for CNV_DET_EC BOM option	0.2 (X01)
5	21	HW	2017/08/22	COMPAL	TPM Pin connectivity requirement	Add RC560,RC561(reserved) BOM options.	0.2 (X01)
6	11	HW	2017/08/22	COMPAL	External Power Gate control for C10.	Add UZ61,CZ544,RZ542,RZ543, RH619, RH620 for	0.2 (X01)
7	35	HW	2017/08/22	COMPAL	Intel PDG rev. 1.0 updated	add RZ1381~RZ1384 for CNVi RSP & DT	0.2 (X01)
8	37	HW	2017/08/22	COMPAL	GPIO map for EC	Add RH625, RE566 for HDD_EN BOM option	0.2 (X01)
9	41	HW	2017/08/22	COMPAL	DELL sch. review	depop RN5	0.2 (X01)
10	37	HW	2017/08/22	COMPAL	To avoid USB_POWERSHARE spike before EC stable when power up.(follow WH)	reserve RE702 for USB_POWERSHARE_VBUS_EN	0.2 (X01)
11	27	HW	2017/08/22	COMPAL	VGA EA request	1. LV19, LV20 change to RV1650, RV1651(100 ohm) 2. CV132, CV133 change to 2P	0.2 (X01)
12	all	HW	2017/08/22	COMPAL	Xtal EA request	1. CH13, CH14 change to 15p 2. CE28, CE29 change to 12p (CE28 keep 10p for 15HD) 3. CV606, CV607 change to 18p 4. RV619 change to 1k	0.2 (X01)
13	all	HW	2017/08/22	COMPAL	RF request	1. pop CA5, CV11, CZ62, CZ63, CZ64, CZ66, CZ67, CZ68, 2. add CI9 3. change RZ85 to LZ2	0.2 (X01)
14	eDP	HW	2017/09/20	COMPAL	touch screen soft start reserve	reserve RV9, CV1638	0.2 (X01)
15	audio	HW	2017/09/20	COMPAL	aduio EA request	depop CH268	0.2 (X01)
16	typeC SW	HW	2017/09/20	COMPAL	typeC EA request	1. depop RT136, RT142, RT144 2. pop RT307	0.2 (X01)
17	EC	HW	2017/09/20	COMPAL	vendor request	depop RE57	0.2 (X01)
18	eDP	HW	2017/12/13	COMPAL	battery life request	RV625, RV630 change from 4.7k to 47k	0.3 (X01)
19	CPU&PCH	HW	2017/12/13	COMPAL	Intel guideline update	1. RH178, RH179, RH181, RH182, RH184 change from 0 ohm to 5 ohm 2. Add CC333(0603) for VCCPLL 3. reserve RH626~RH627 & CH341~CH349 for PCH signal glitch free	0.3 (X01)
20	EC	HW	2017/12/13	COMPAL	follow EC request for X10	reserve RE703(0 ohm) between PCH to EC	0.3 (X01)
21	eDP	HW	2017/12/13	COMPAL	DELL request	QV28 3 reserve RV1656 [0 ohm] to +3.3V_ALW	0.3 (X01)
22	CPU	HW	2017/12/13	COMPAL	ESD request	1. CC32, CC269 change BS from XDP@ to ESD@ 2. add CC334, CC335 for +1.0V_VCCSTG	0.3 (X01)
23	CPU	HW	2017/12/13	COMPAL	add short protection fot typeC	add CT630~633, RT416~419 between re-timer and connector	0.3 (X01)
24	CNVi	HW	2017/12/13	COMPAL	intel MOW50 CNVi WP update	RZ1382, RZ1384 change from 33 ohm to 22 ohm	0.3 (X01)
25	EC	HW	2017/12/13	COMPAL	board ID	RE79 change to 62k	0.3 (X01)
26	TPM	HW	2018/01/08	COMPAL	TPM change to MP part	UZ12 change CPN from SA0000AQZ00 to SA0000AQZ20	0.4 (X02)
27	EC	HW	2018/01/08	COMPAL	reserve for power on sequence modification	1.8V_PRIM_PWRGD rename to 1.8V_1.0V_PWRGD	0.4 (X02)
28	CPU	HW	2018/01/08	COMPAL	Intel PDG updated	pop CC333	0.4 (X02)
29	typeC SW	HW	2018/01/08	COMPAL	USB3.1 Gen2 EA fail	14HU & 15HU typeC-SW change to parade solution	0.5 (X02)

Compal Electronics, Inc.

Title: B.E.P.I.R (1/1)

Size: Custom | Number: | Rev: X01

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