EL8 Block Diagram

VCC_CORE

GMCH_CORE

VCC1.1
VCC1.2
VCC1.5
1.5VSUS

VCC3
3V_STBY

VCC5
5V_STBY
+12V

Intel
Yorkfield/Wolfdale
Q9000/E8000
LGA775
Page 3,4

CLOCK GENERATOR
CK505
CV193
Page 2

FSB(800/1067/1333HZ)

800/1067 MHZ DDR III

CH A: DDRIII-UDIMM0/1
CH B: DDRIII-UDIMM0/1
Page 14,15,16,17

NB
Eaglelake
G45/P43
1254 pin
Page 5,7,8,9

PCI-E 2.0 16X

MXM CONNECTOR
Page 18

LVDS

LCD PANEL
23" Full HD

SDVO

LVDS Transmitter
CH7308B
Page 19

DMI

SATA - HDD(2.5)
Page 22
SATA 4

SATA - HDD(3.5)
Page 22
SATA 1

SATA - ODD
Page 22
SATA 2

eSATA
Page 22
SATA 3

WLAN
Page 25
USB-10

USB 2.0

Camera
Page 19
USB-1

BT KB/Mouse
Page 27

Bluetooth
Page 26
USB-2

USB*4(Rear)
Page 27
USB-6,7
8,9

TV
Page 25
USB-11

USB*2(Side)
Page 26
USB-3,5

Touch Screen
Page 27
USB-0

Azalia

SB
ICH10
676 pin
Page 10,11,12,13

PCI-Express 1X

PCIE-2
MINI CARD-1
WLAN
Page 25

PCIE-3
MINI CARD-2
TV card
Page 25

PCIE-1
LAN
RTL8111DL
Page 26

PCIE-4
Card Reader
JMB385
Page 27

WLAN antenna

TV antenna

RJ45

Media Slot

LPC

32.768KHz

ITE8512
Page 26

HP
Page 30

MIC IN
Page 30

INT SPK
Page 29

DMIC IN
Page 30

AUDIO CODEC
ALC888S-VC2
Page 29

LINE IN

5.1 Channel

IR
Blaster
Page 3

FAN
Page 26

FLASH
ROM
Page 28

CIR
Page 28

Daughter
Board

MXM module
314 pin

B-CAS board
10 pin

Card Reader
20 pin

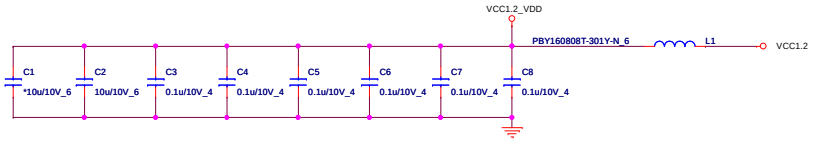
HP/MIC
Light SW
10 pin

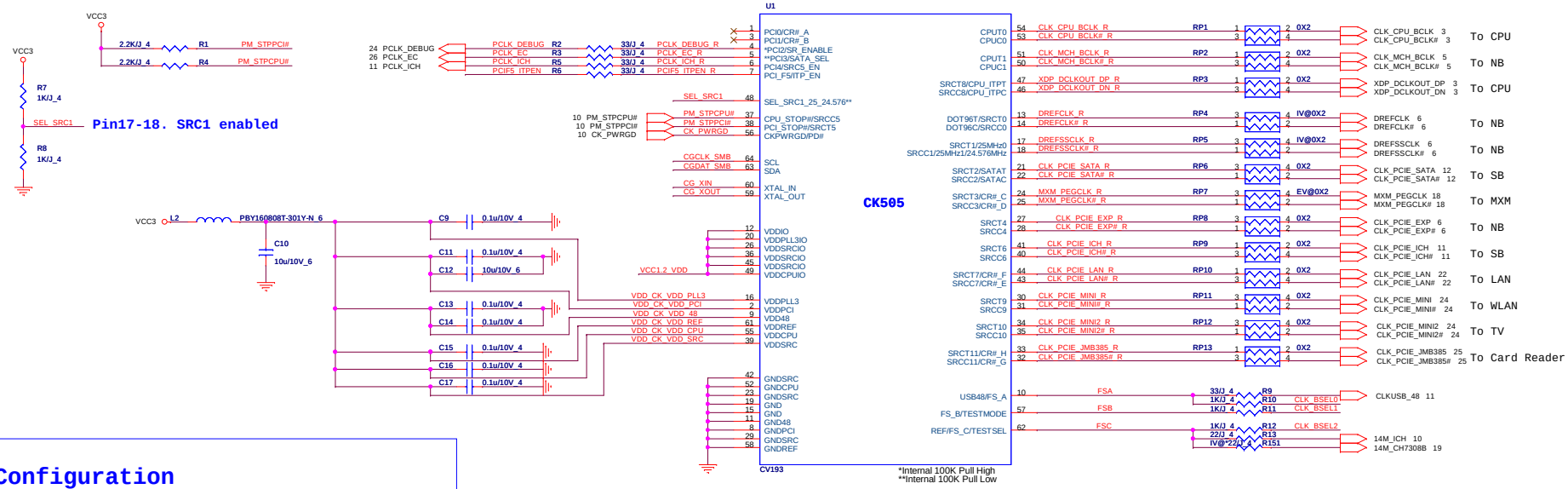
Power button
LED
TBD

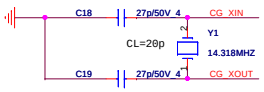
PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, March 09, 2009	Sheet 1 of 34	

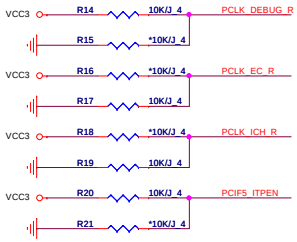
Clock Generator







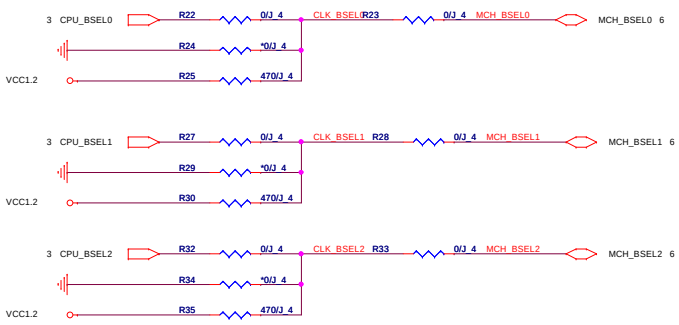
Strap Configuration



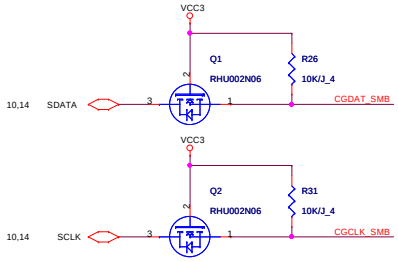
FREQ. SEL TABLE

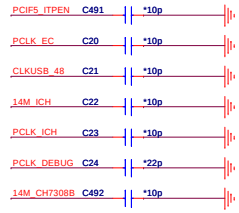
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved



Clock Gen I2C





PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
	CLK. GEN./ CK505	1A
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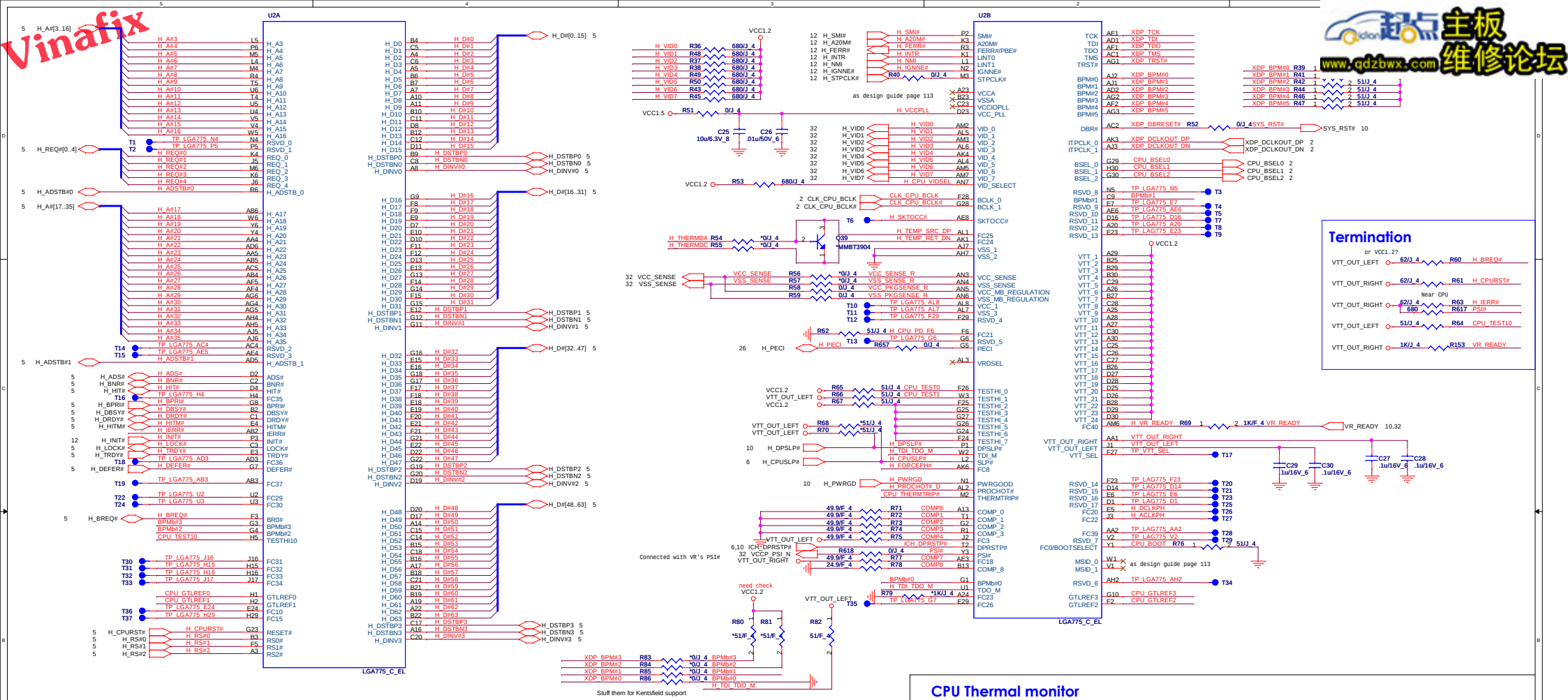

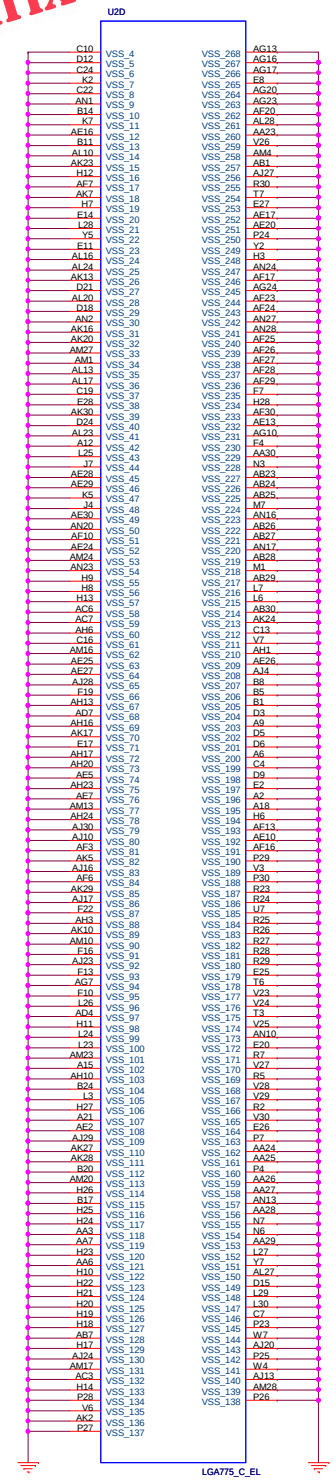

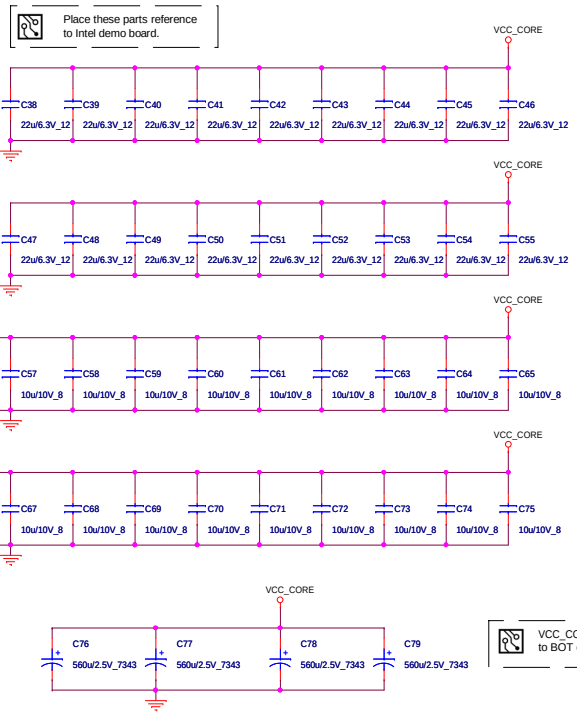

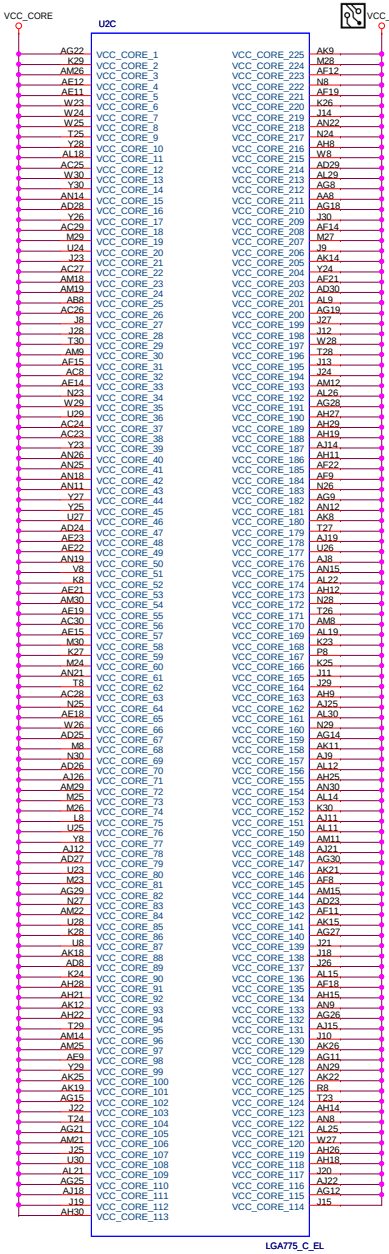

Yorkfield/Wolfdale CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	100A	Yorkfield@65W
VCC_CORE	O	X	X	VID	75A	Wolfdale
VTT	O	X	X	VCC1.2	8A	After VCC stable
VTT	O	X	X	VCC1.2	7A	Before VCC stable
VCC_PLL	O	X	X	VCC1.5	260mA	

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Size	Document Number	Rev
	CPU(2/2)- Power	1A
Date: Monday, March 09, 2009	Sheet 4 of 34	

VCC1.2
R113 301/F_4
R112 100/F_4
R114 51/J_4 H_SWING
C80 0.1u/10V_4
0.25*VCCP
W:10,S:10 , L<3"
BreakoutL<0.25"
49.9/F as schematic checklist

W:10,S:7 , L<0.5"
BreakoutL<0.25"
H_RCOMP
R115 16.5/F_4

VCC1.2
R116 57.6/F_4
R117 51/J_4 MCH_GTLREF0
R118 100/F_4
C82 1u/10V_6
C81 220p/10V_4
0.365*VCCP
W:10,S:20 , L<1.5"
49.9/F as schematic checklist

VCC1.2
R119 57.6/F_4
R120 51/J_4 MCH_GTLREF1
R121 100/F_4
C83 1u/10V_6
C84 220p/10V_4
0.365*VCCP
W:10,S:20 , L<1.5"
49.9/F as schematic checklist

U4A
EAGLELAKE_DDR3
SYM_REV = 1.5GC

3 H_A#[3..16]
3 H_A#[17..35]
3 H_REQ#[0..4]
3 H_DSTBP[3..0]
3 H_DSTBN[3..0]
3 H_DINV#[3..0]
3 H_ADS#
3 H_TRDY#
3 H_DRDY#
3 H_DEFER#
3 H_HITM#
3 H_HIT#
3 H_LOCK#
3 H_BREQ#
3 H_BNR#
3 H_BPRI#
3 H_DBSY#
3 H_RS#[2..0]
3 H_CPURST#

H_A#3 L36 FSB_AB_3
H_A#4 L37 FSB_AB_4
H_A#5 J38 FSB_AB_5
H_A#6 E40 FSB_AB_6
H_A#7 H39 FSB_AB_7
H_A#8 L38 FSB_AB_8
H_A#9 L43 FSB_AB_9
H_A#10 N39 FSB_AB_10
H_A#11 N35 FSB_AB_11
H_A#12 N37 FSB_AB_12
H_A#13 J41 FSB_AB_13
H_A#14 N40 FSB_AB_14
H_A#15 M45 FSB_AB_15
H_A#16 R35 FSB_AB_16
H_A#17 T36 FSB_AB_17
H_A#18 R36 FSB_AB_18
H_A#19 R34 FSB_AB_19
H_A#20 R37 FSB_AB_20
H_A#21 R39 FSB_AB_21
H_A#22 U38 FSB_AB_22
H_A#23 T37 FSB_AB_23
H_A#24 U34 FSB_AB_24
H_A#25 U40 FSB_AB_25
H_A#26 T34 FSB_AB_26
H_A#27 Y36 FSB_AB_27
H_A#28 U35 FSB_AB_28
H_A#29 AA35 FSB_AB_29
H_A#30 U37 FSB_AB_30
H_A#31 Y37 FSB_AB_31
H_A#32 Y34 FSB_AB_32
H_A#33 Y38 FSB_AB_33
H_A#34 AA37 FSB_AB_34
H_A#35 AA36 FSB_AB_35

H_REQ#0 G38 FSB_REQB_0
H_REQ#1 K35 FSB_REQB_1
H_REQ#2 J39 FSB_REQB_2
H_REQ#3 C43 FSB_REQB_3
H_REQ#4 G39 FSB_REQB_4

H_ADSTB#0 J40 FSB_ADSTBB_0
H_ADSTB#1 T39 FSB_ADSTBB_1

H_DSTBP0 C39 FSB_DSTBPB_0
H_DSTBN0 B39 FSB_DSTBNB_0
H_DINV#0 B40 FSB_DINVB_0
H_DSTBP1 K31 FSB_DSTBPB_1
H_DSTBN1 J31 FSB_DSTBNB_1
H_DINV#1 F33 FSB_DINVB_1
H_DSTBP2 J25 FSB_DSTBPB_2
H_DSTBN2 K25 FSB_DSTBNB_2
H_DINV#2 F26 FSB_DINVB_2
H_DSTBP3 C32 FSB_DSTBPB_3
H_DSTBN3 D32 FSB_DSTBNB_3
H_DINV#3 D30 FSB_DINVB_3

H_ADS# J42 FSB_ADSB
H_TRDY# L40 FSB_TRDYB
H_DRDY# J43 FSB_DRDYB
H_DEFER# G44 FSB_DEFERB
H_HITM# K44 FSB_HITMB
H_HIT# H45 FSB_HITB
H_LOCK# H40 FSB_LOCKB
H_BREQ# L42 FSB_BREQ0B
H_BNR# J44 FSB_BNRB
H_BPRI# H37 FSB_BPRIB
H_DBSY# H42 FSB_DBSYB
H_RS#0 G43 FSB_RSB_0
H_RS#1 L44 FSB_RSB_1
H_RS#2 G42 FSB_RSB_2
H_CPURST# D27 FSB_CPURSTB

T38 TP_MCH_N25 N25 RSVD_05

1 OF 9
EAGLELAKE_FCBGA1254

FSB_DB_0 E44 H_D#0
FSB_DB_1 C44 H_D#1
FSB_DB_2 D44 H_D#2
FSB_DB_3 C41 H_D#3
FSB_DB_4 E43 H_D#4
FSB_DB_5 B43 H_D#5
FSB_DB_6 D40 H_D#6
FSB_DB_7 B42 H_D#7
FSB_DB_8 B38 H_D#8
FSB_DB_9 E38 H_D#9
FSB_DB_10 A38 H_D#10
FSB_DB_11 B37 H_D#11
FSB_DB_12 D38 H_D#12
FSB_DB_13 C37 H_D#13
FSB_DB_14 D37 H_D#14
FSB_DB_15 B36 H_D#15
FSB_DB_16 E37 H_D#16
FSB_DB_17 J35 H_D#17
FSB_DB_18 H35 H_D#18
FSB_DB_19 E37 H_D#19
FSB_DB_20 G37 H_D#20
FSB_DB_21 J33 H_D#21
FSB_DB_22 L33 H_D#22
FSB_DB_23 G33 H_D#23
FSB_DB_24 L31 H_D#24
FSB_DB_25 M31 H_D#25
FSB_DB_26 M30 H_D#26
FSB_DB_27 J30 H_D#27
FSB_DB_28 G31 H_D#28
FSB_DB_29 K30 H_D#29
FSB_DB_30 M29 H_D#30
FSB_DB_31 G30 H_D#31
FSB_DB_32 J29 H_D#32
FSB_DB_33 F29 H_D#33
FSB_DB_34 H29 H_D#34
FSB_DB_35 L25 H_D#35
FSB_DB_36 K26 H_D#36
FSB_DB_37 L29 H_D#37
FSB_DB_38 J26 H_D#38
FSB_DB_39 M26 H_D#39
FSB_DB_40 H26 H_D#40
FSB_DB_41 E25 H_D#41
FSB_DB_42 E24 H_D#42
FSB_DB_43 G25 H_D#43
FSB_DB_44 H24 H_D#44
FSB_DB_45 L24 H_D#45
FSB_DB_46 J24 H_D#46
FSB_DB_47 N24 H_D#47
FSB_DB_48 C28 H_D#48
FSB_DB_49 B31 H_D#49
FSB_DB_50 E35 H_D#50
FSB_DB_51 C35 H_D#51
FSB_DB_52 B35 H_D#52
FSB_DB_53 D35 H_D#53
FSB_DB_54 D31 H_D#54
FSB_DB_55 A34 H_D#55
FSB_DB_56 B32 H_D#56
FSB_DB_57 E31 H_D#57
FSB_DB_58 D28 H_D#58
FSB_DB_59 A29 H_D#59
FSB_DB_60 C30 H_D#60
FSB_DB_61 B30 H_D#61
FSB_DB_62 E27 H_D#62
FSB_DB_63 B28 H_D#63

H_D#[0..15] 3
H_D#[16..31] 3
H_D#[32..47] 3
H_D#[48..63] 3

FSB_SWING B24 H_SWING
FSB_RCOMP A23 H_RCOMP
FSB_DVREF C22 MCH_GTLREF0
FSB_ACCVREF B23 MCH_GTLREF1
HPL_CLKINP P29 CLK_MCH_BCLK
HPL_CLKINN P30 CLK_MCH_BCLK#

CLK_MCH_BCLK 2
CLK_MCH_BCLK# 2

FSB

PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
	NB (1/5) HOST	1A
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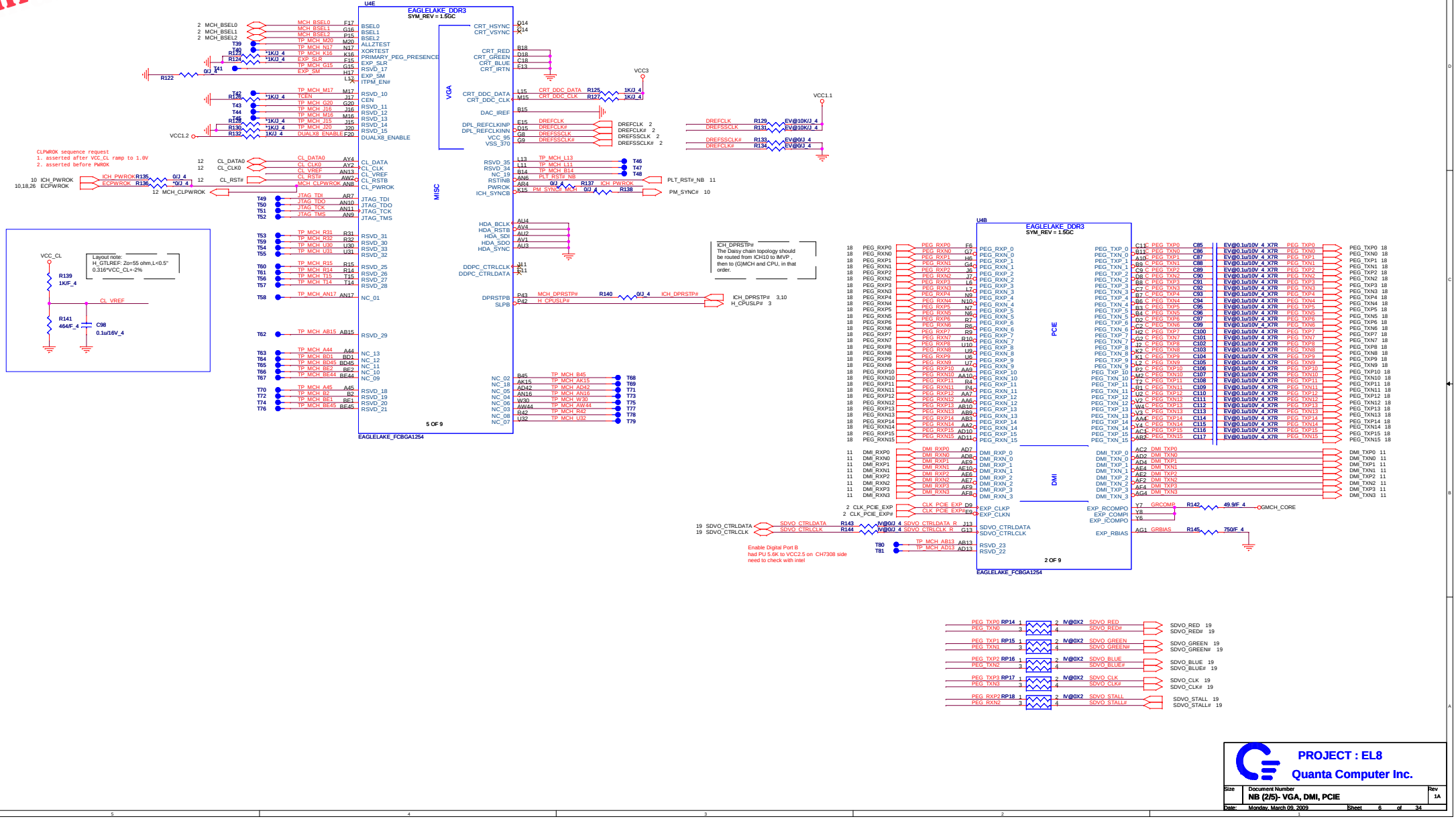

PROJECT : EL8
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Size	Document Number	Rev
	NB (2/5)- VGA, DMI, PCIE	1A

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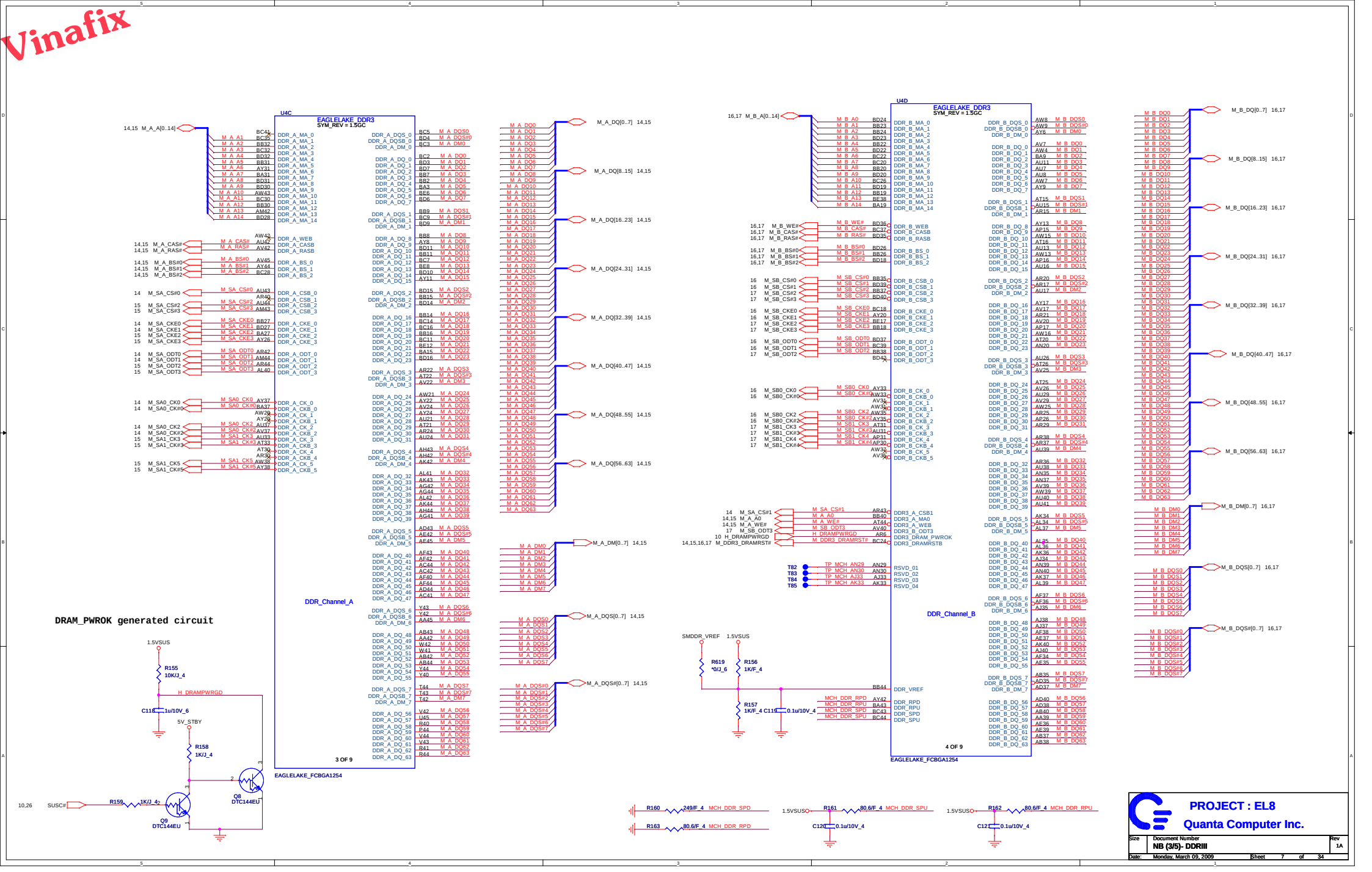
PROJECT : EL8
Quanta Computer Inc.



PROJECT : EL8
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Size	Document Number	Rev
	NB (3/5)- DDRIII	1A

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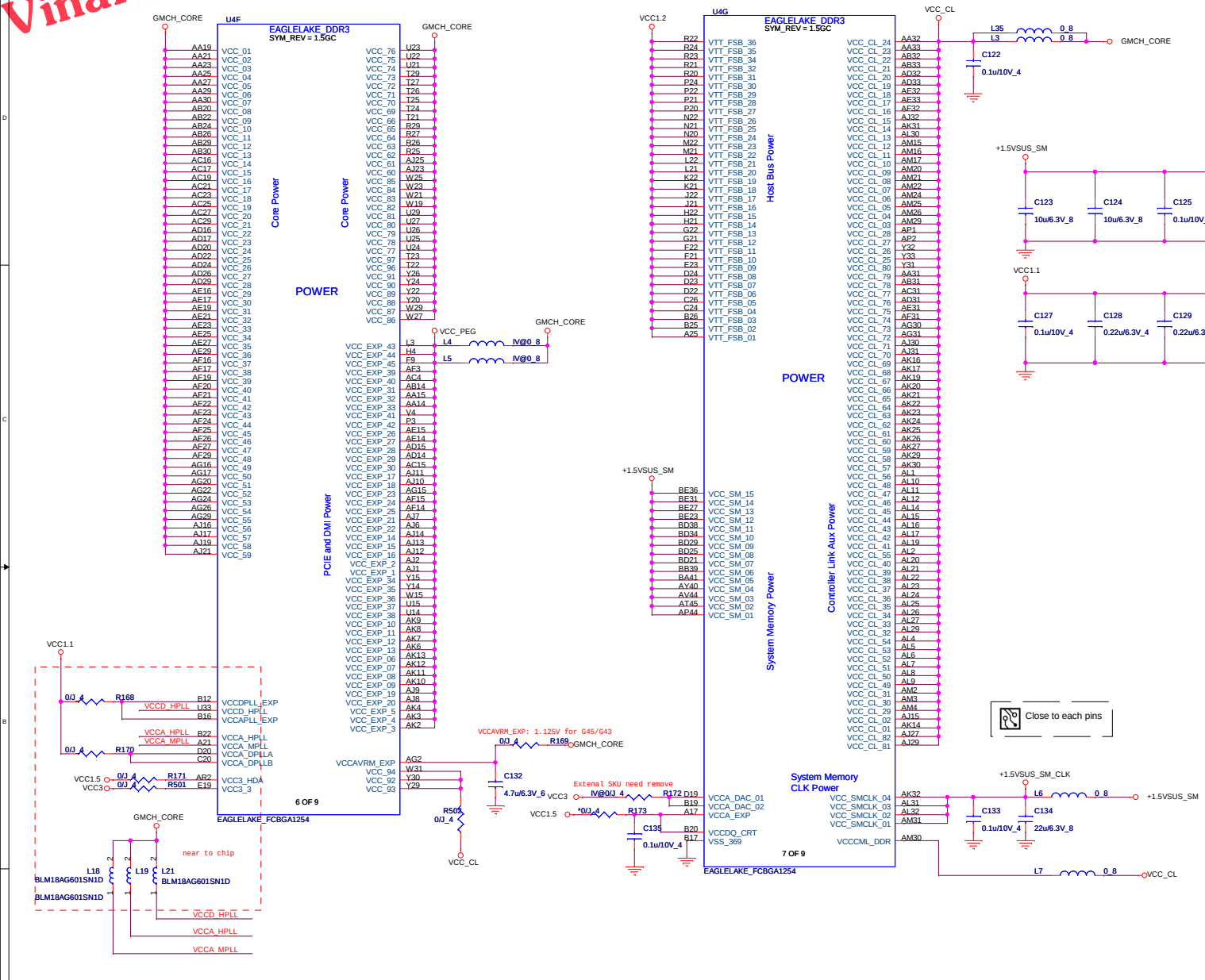

SKU	G45	P43
GMCH_CORE	1.125V	1.1V

NB Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_SM	O	O	X	1.5VSUS	1963mA	
VCC_SMCLK	O	O	X	1.5VSUS	288mA	
VCC_EXP	O	X	X	GMCH_CORE	3082mA	SDVO, PCIE, DMI
VCCA_EXP	O	X	X	VCC1.5	6mA	SDVO, PCIE Analog
VTT_FSB	O	X	X	VCC1.2	914mA	
VCC	O	X	X	GMCH_CORE	17984mA	
VCC_CL	O	X	X	GMCH_CORE	4666mA	
VCC3_3	O	X	X	VCC3	14mA	
VCCA_DAC	O	X	X	VCC3	74mA	
VCCDQ_CRT	O	X	X	VCC1.5	0mA	
VCCAPLL_EXP	O	X	X	VCC1.1	20mA	
VCCDPLL_EXP	O	X	X	VCC1.1	X	
VCCA_DPLLA	O	X	X	VCC1.1	59mA	
VCCA_DPLLB	O	X	X	VCC1.1	59mA	
VCCA_HPLL	O	X	X	VCC1.1	31mA	
VCCD_HPLL	O	X	X	VCC1.1	X	
VCCA_MPLL	O	X	X	VCC1.1	83mA	

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Size	Document Number	Rev
	NB (4/5)- Power	1A

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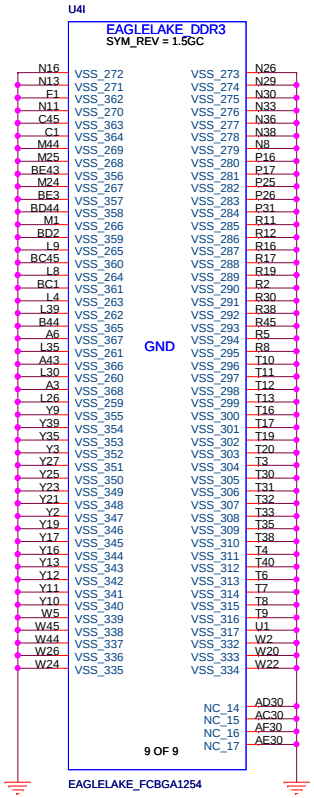

PROJECT : EL8

Quanta Computer Inc.

Size	Document Number	Rev
	NB (5/5)- VSS	1A
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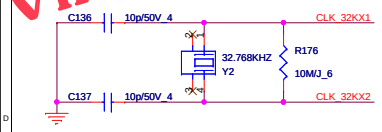
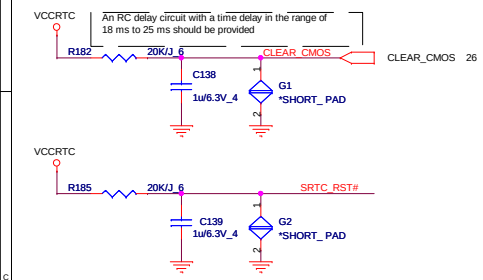
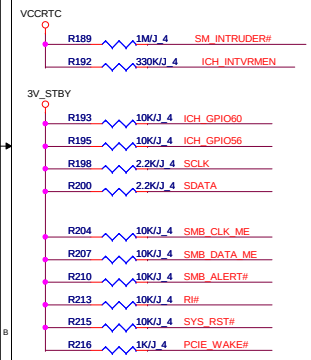
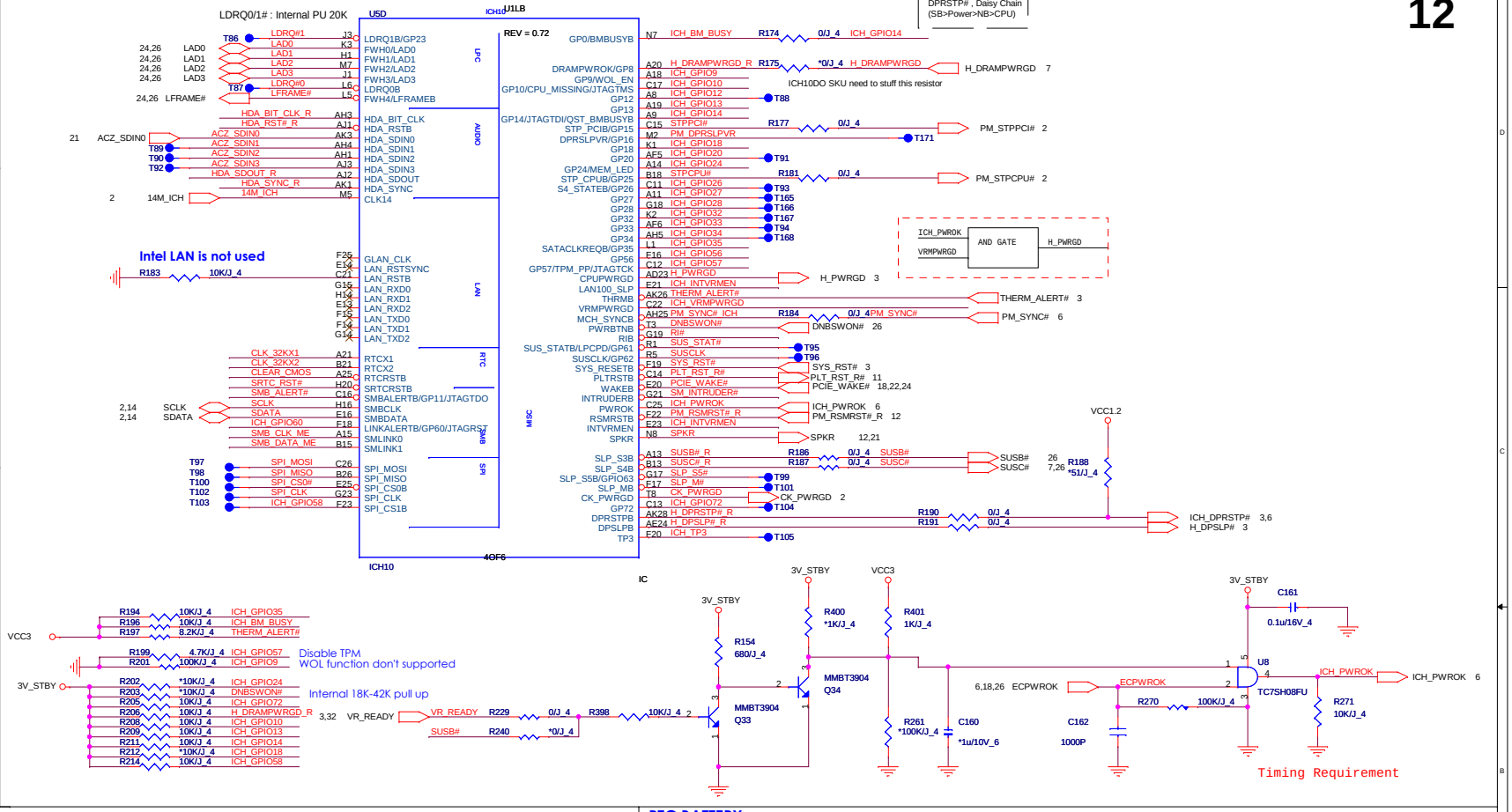
RTC CRYSTAL



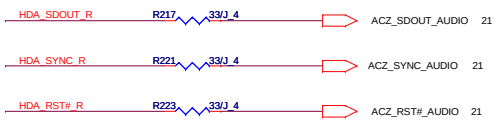
RESET JUMP

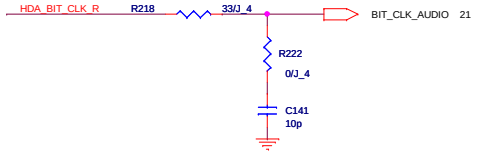




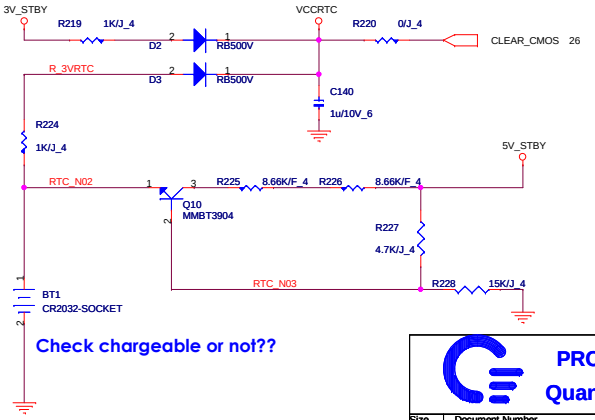


HD Audio I/F(CODEC& iHDMI)





RTC BATTERY



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 R230 *1K/J_4	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUT_R R231 *3.3K/J_4 +3V_HDA_IO_ICH	

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

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Size	Document Number	Rev
	SB (1/4)- HOST	1A

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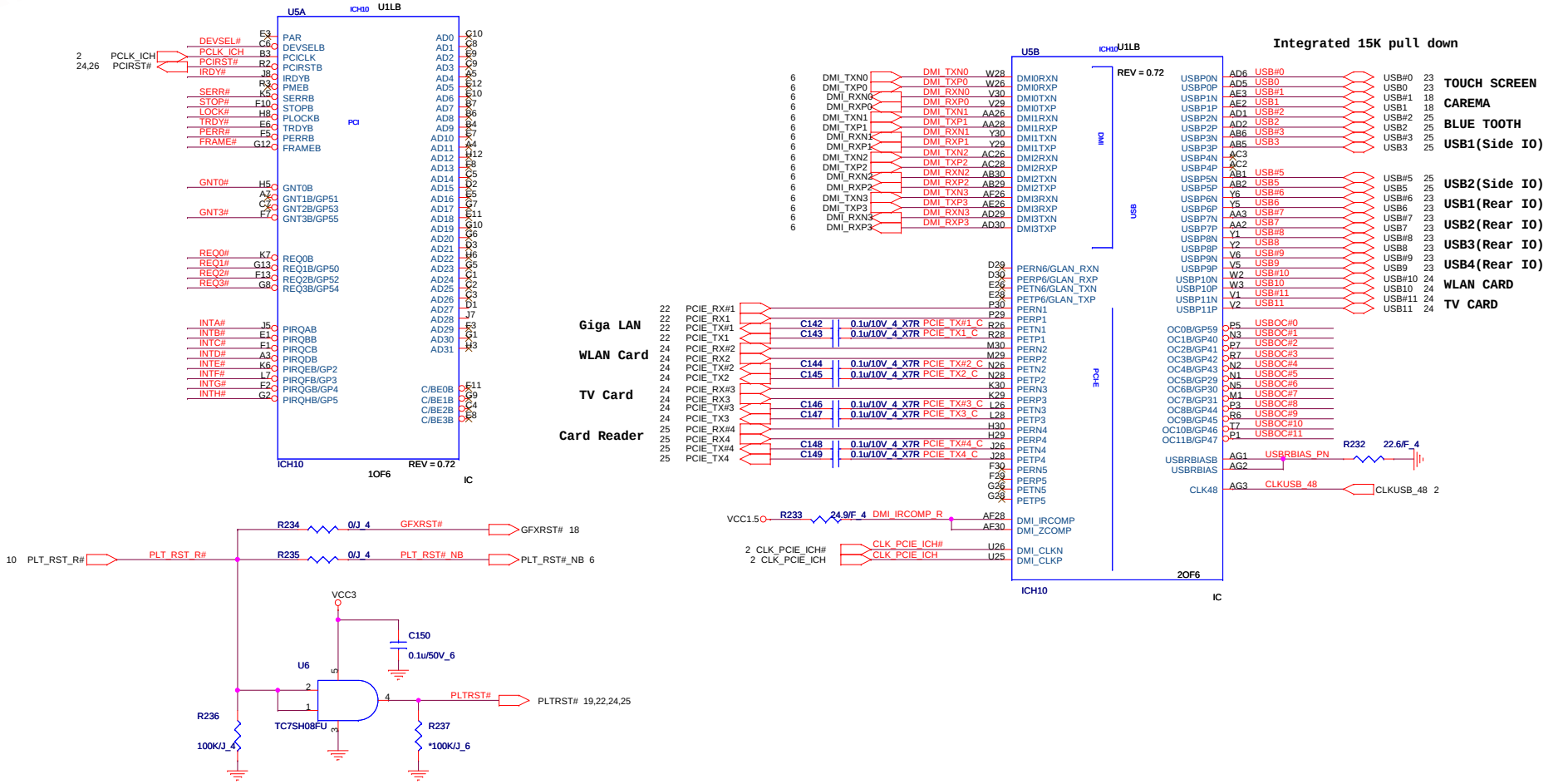
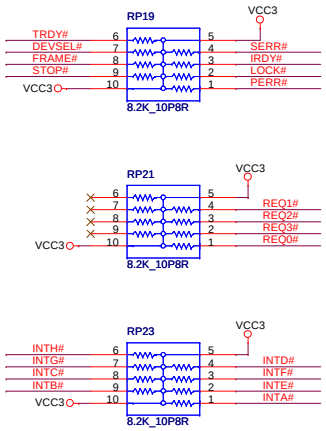


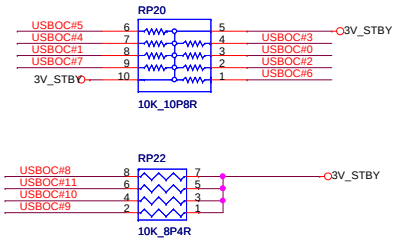
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R238 *1K/J_4
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R239 *1K/J_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		

PCI PULL-UP



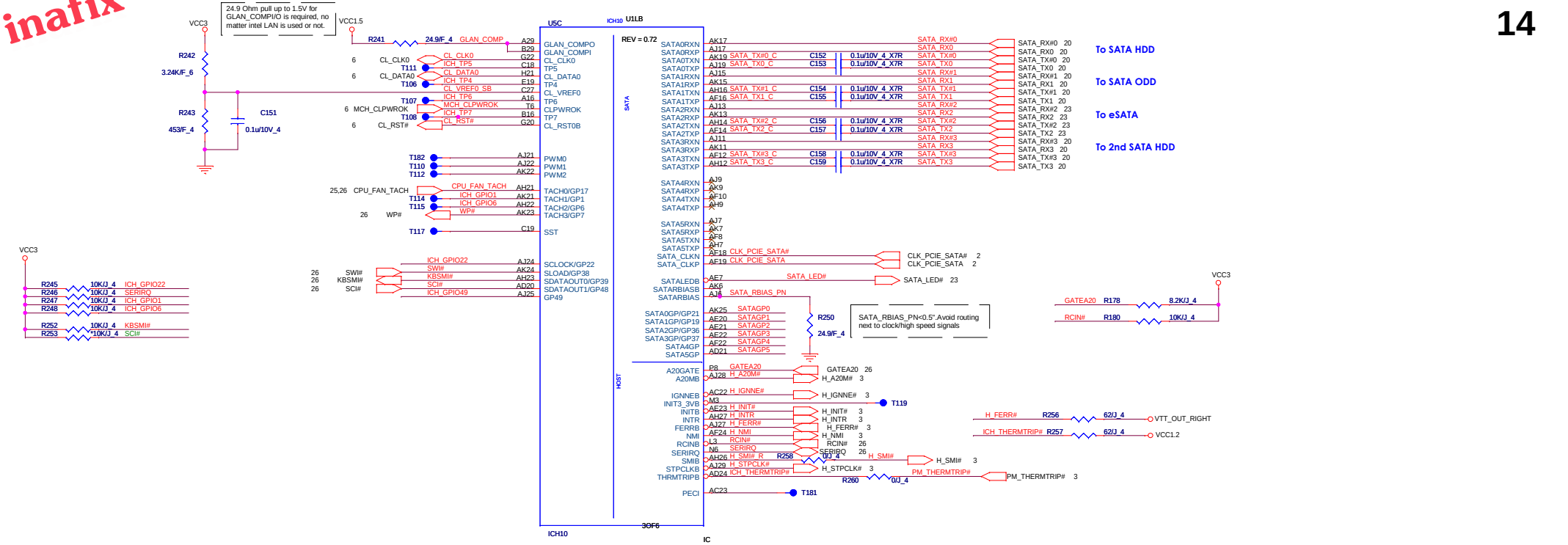
USBOC# PULL-UP



PROJECT : EL8

Quanta Computer Inc.

Size	Document Number	Rev
	SB (2/4) PCIE/PCI/USB/DMI	1A
Date: Monday, March 09, 2009	Sheet 11 of 34	



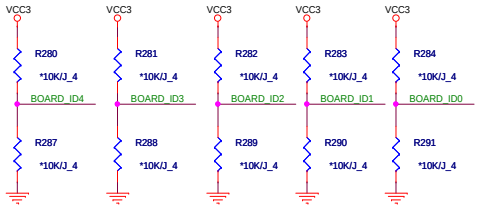
South Bridge Strap Pin (3/3)

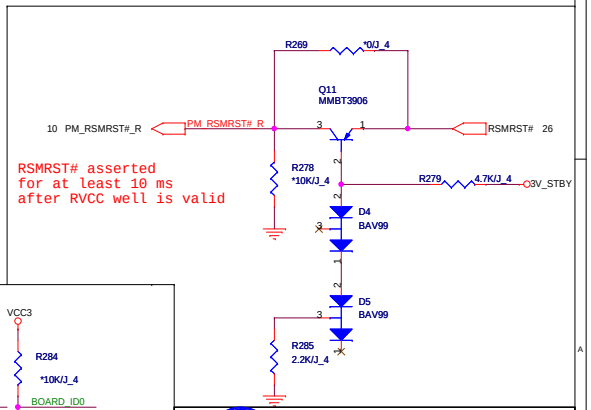
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R286 *1K/J_4 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = AC coupled 1 = DC coupled Internal PU	ICH_GPIO49 R292 *1K/J_4

Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				





PROJECT : EL8

Quanta Computer Inc.

Size	Document Number	Rev
	SB(3/4) SATA/GPIO	1A

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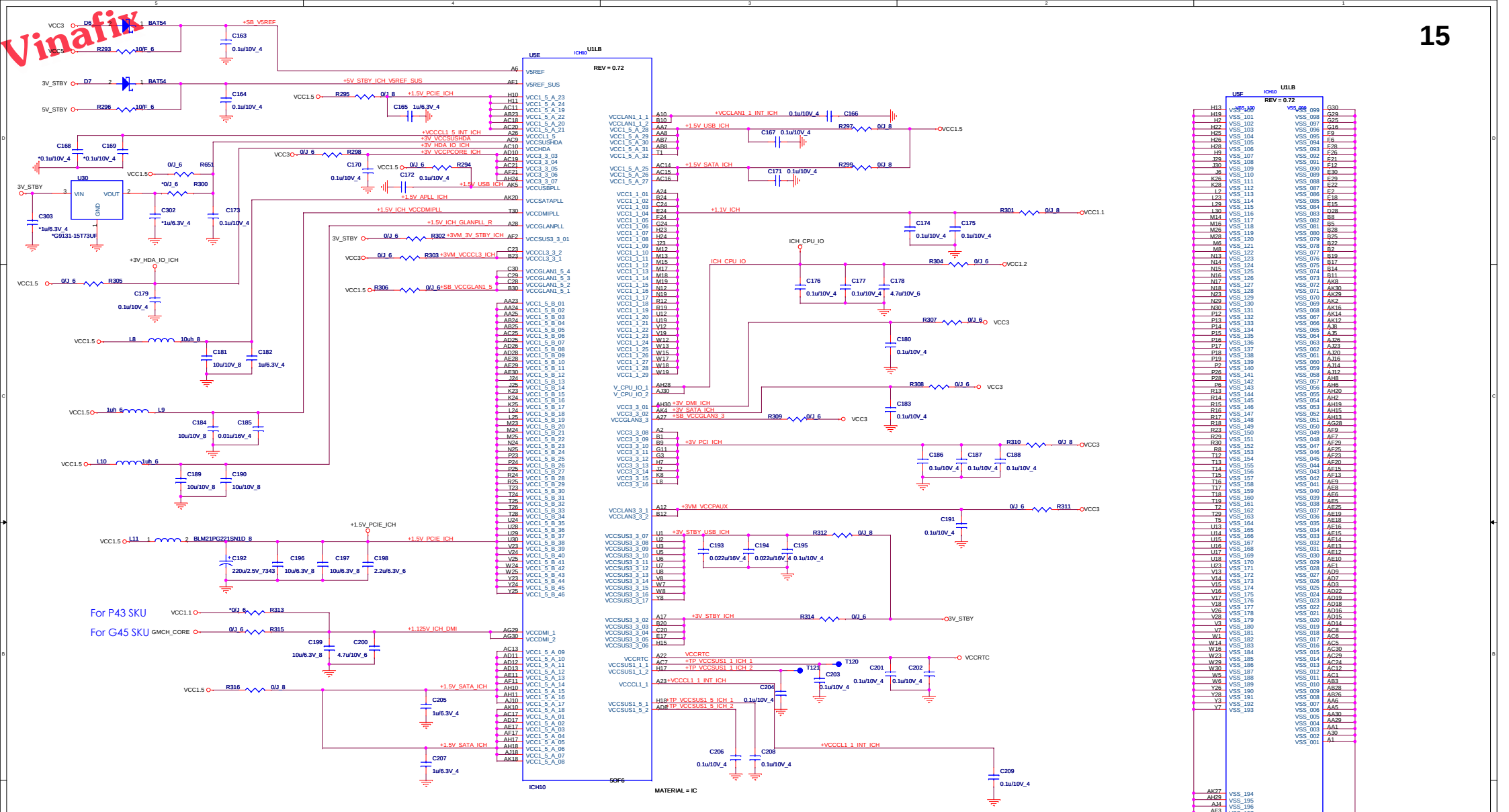

SB Power Status and max current table(1/2)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	VCCRTC	6uA	6uA@G3
V5REF	O	X	X	VCC5	2mA	
V5REF_SUS	O	O	O	5V_STBY	2mA	2mA@S0,1mA@S3/S5
VCC1_5_B	O	X	X	VCC1.5	646mA	
VCCSATAPLL	O	X	X	VCC1.5	47mA	
VCC1_5_A	O	X	X	VCC1.5	1644mA	
VCCUSBPLL	O	X	X	VCC1.5	11mA	
VCCLAN1_1	X	X	X	1.1V	X	Internal VR powered, S3/S5 powered when AMT actived
VCCLAN3_3	O	X	X	VCC3	78mA	78mA@S3/S5 powered when AMT actived
VCCGLANPLL	O	X	X	VCC1.5	23mA	
VCCGLAN1_5	O	X	X	VCC1.5	80mA	
VCCGLAN3_3	O	X	X	VCC3	1mA	

SB Power Status and max current table(2/2)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_1	O	X	X	VCC1.1	1.634A	ICH CORE
VCCDMIPLL	O	X	X	VCC1.5	23mA	
VCC_DMI	O	X	X	GMCH_CORE	50mA	1.125V@G45, 1.1V@P43
V_CPU_IO	O	X	X	VCC1.2	2mA	
VCC3_3	O	X	X	VCC3	308mA	
VCCHDA	O	X	X	VCC1.5	70mA	
VCCSUSHDA	O	O	O	RVCC1.5	70mA	
VCCSUS1_1	X	X	X	1.1V	X	Internal VR powered
VCCSUS1_5	X	X	X	1.5V	X	Internal VR powered
VCCSUS3_3	O	O	O	3V_STBY	212mA	53mA@S3/S5
VCCCL1_1	X	X	X	1.1V	X	Internal VR powered
VCCCL1_5	X	X	X	1.5V	X	Internal VR powered
VCCCL3_3	O	X	X	VCC3	1mA	S3/S5 powered when AMT actived

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Size	Document Number	Rev
	SB(4/4) POWER/VSS	1A
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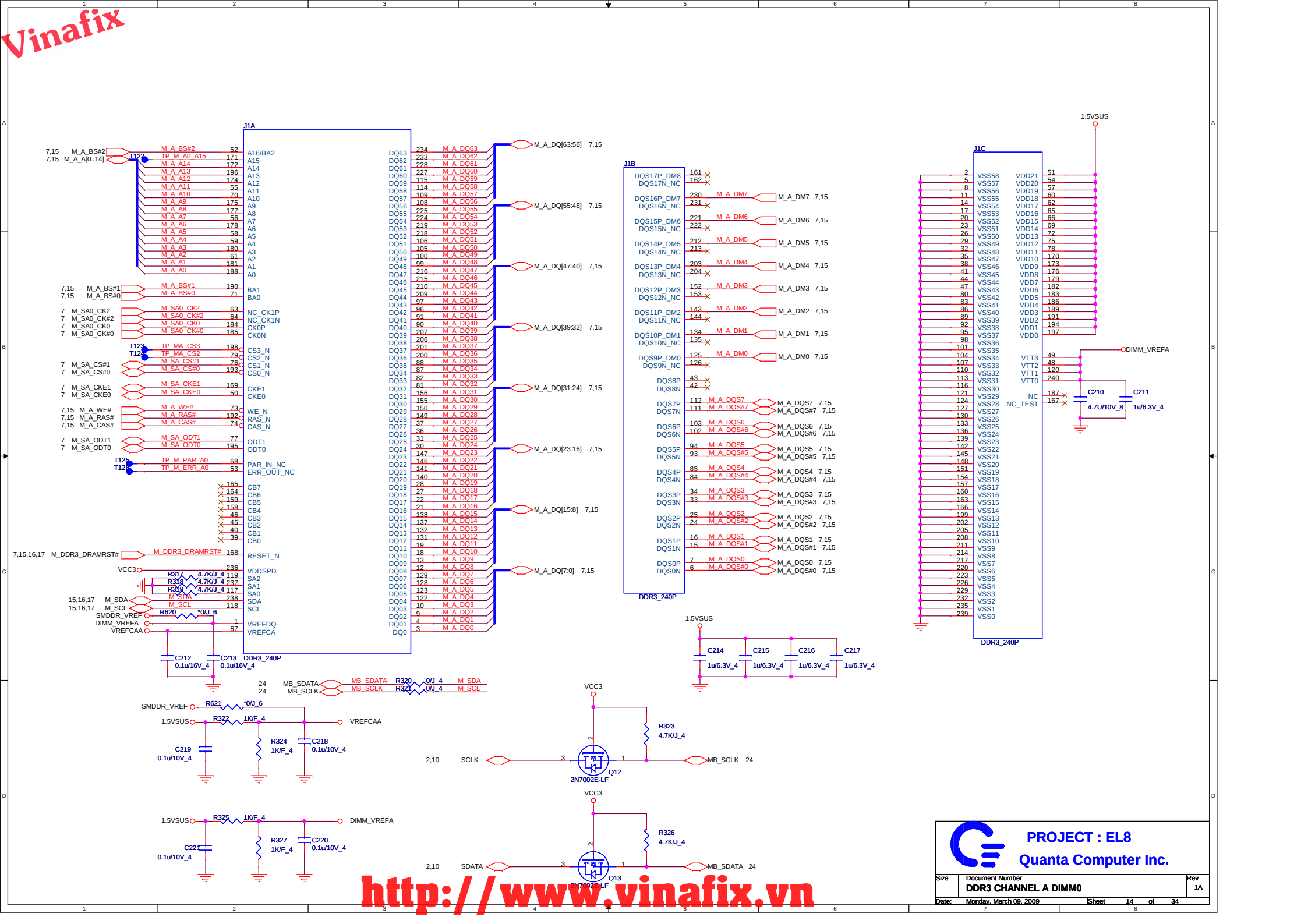

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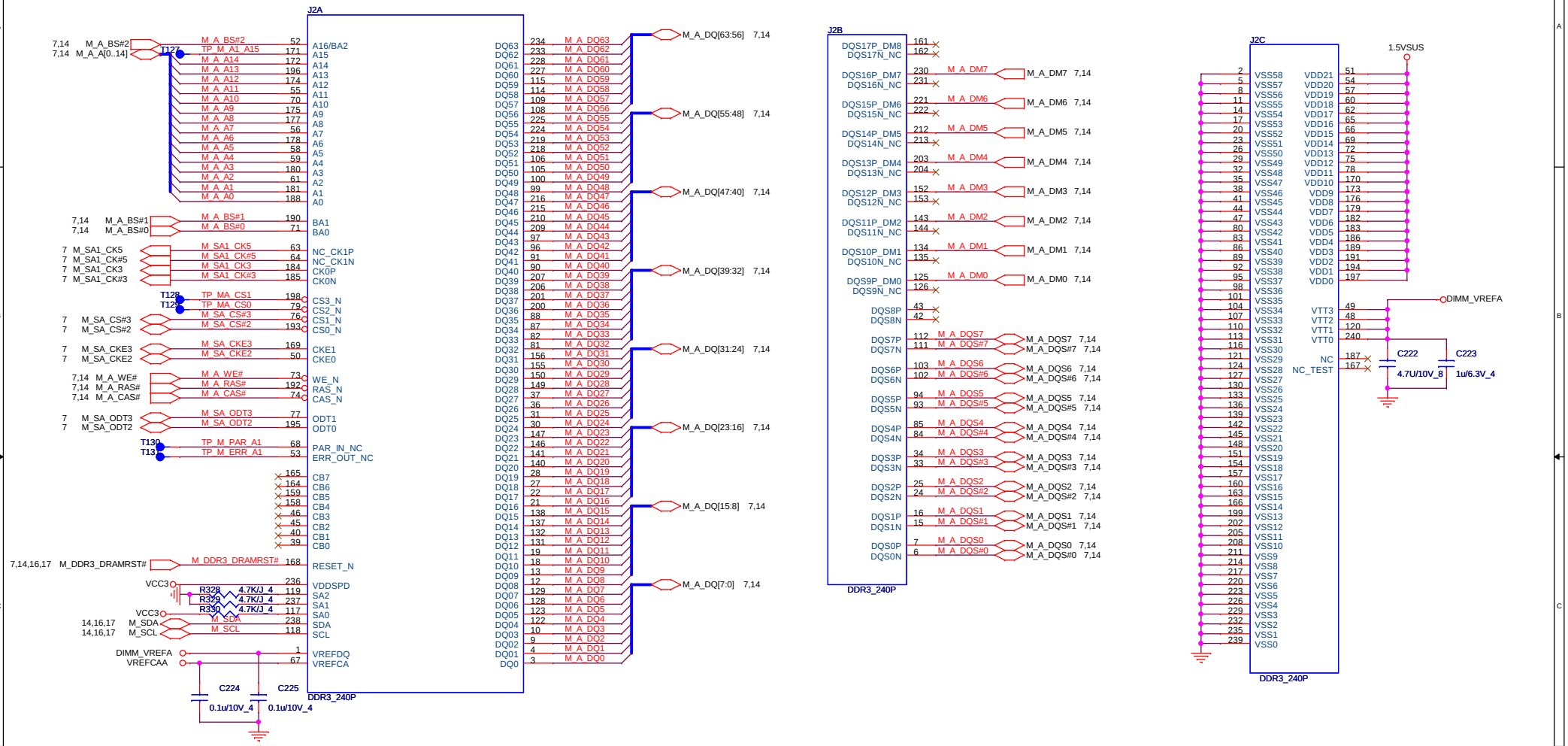
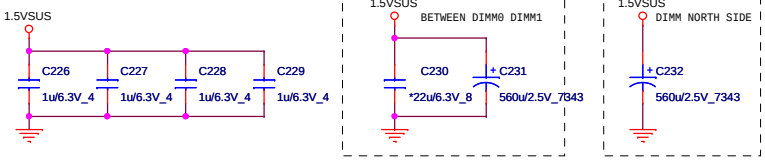
Quanta Computer Inc.			
Size	Document Number		Rev
	DDR3 CHANNEL A DIMM0		1A
Date:	Monday, March 09, 2009	Sheet 14 of 34	





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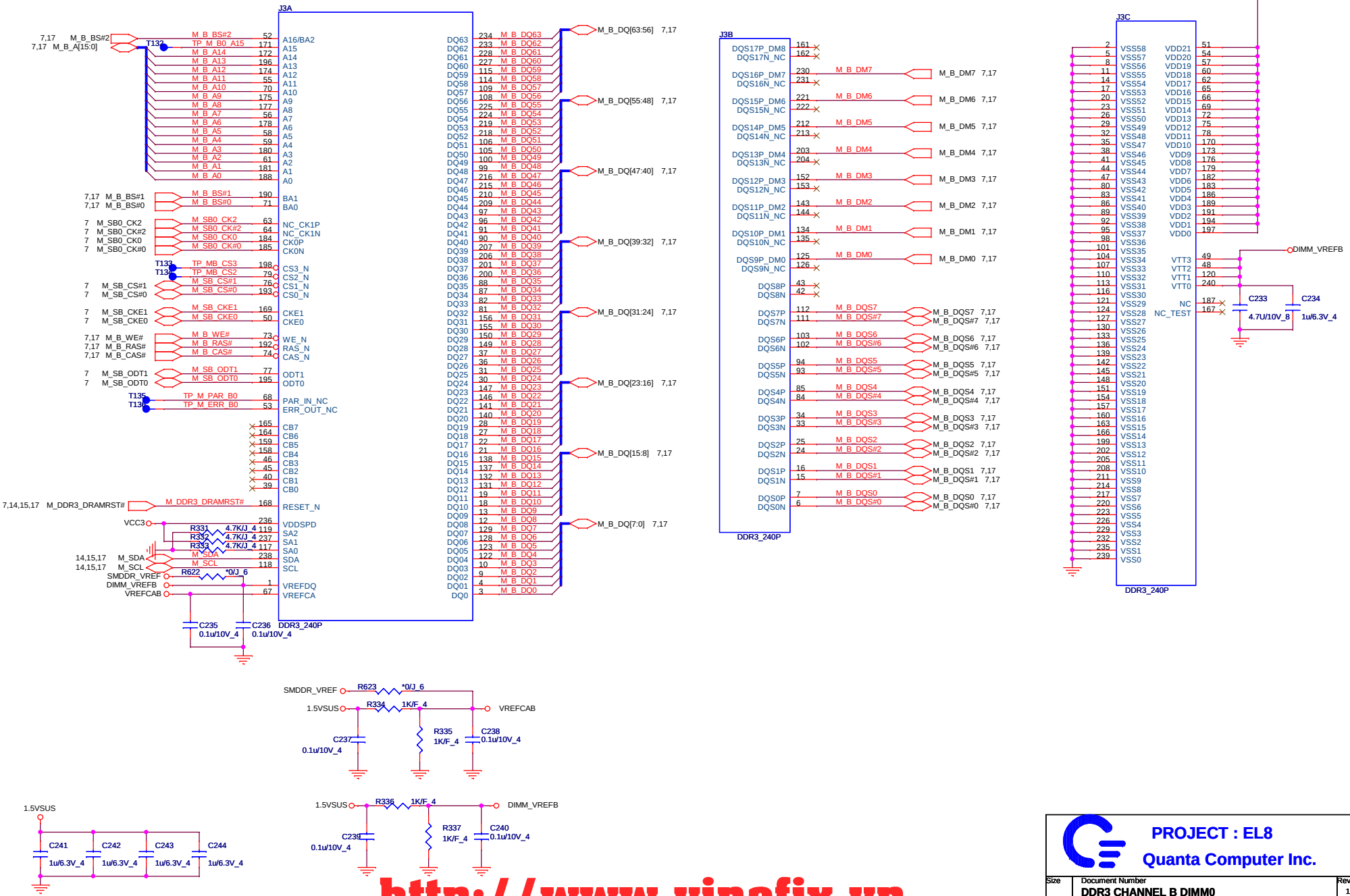
Size	Document Number	Rev
	DDR3 CHANNEL A DIMM1	1A
Date: Monday, March 09, 2009	Sheet 15 of 34	



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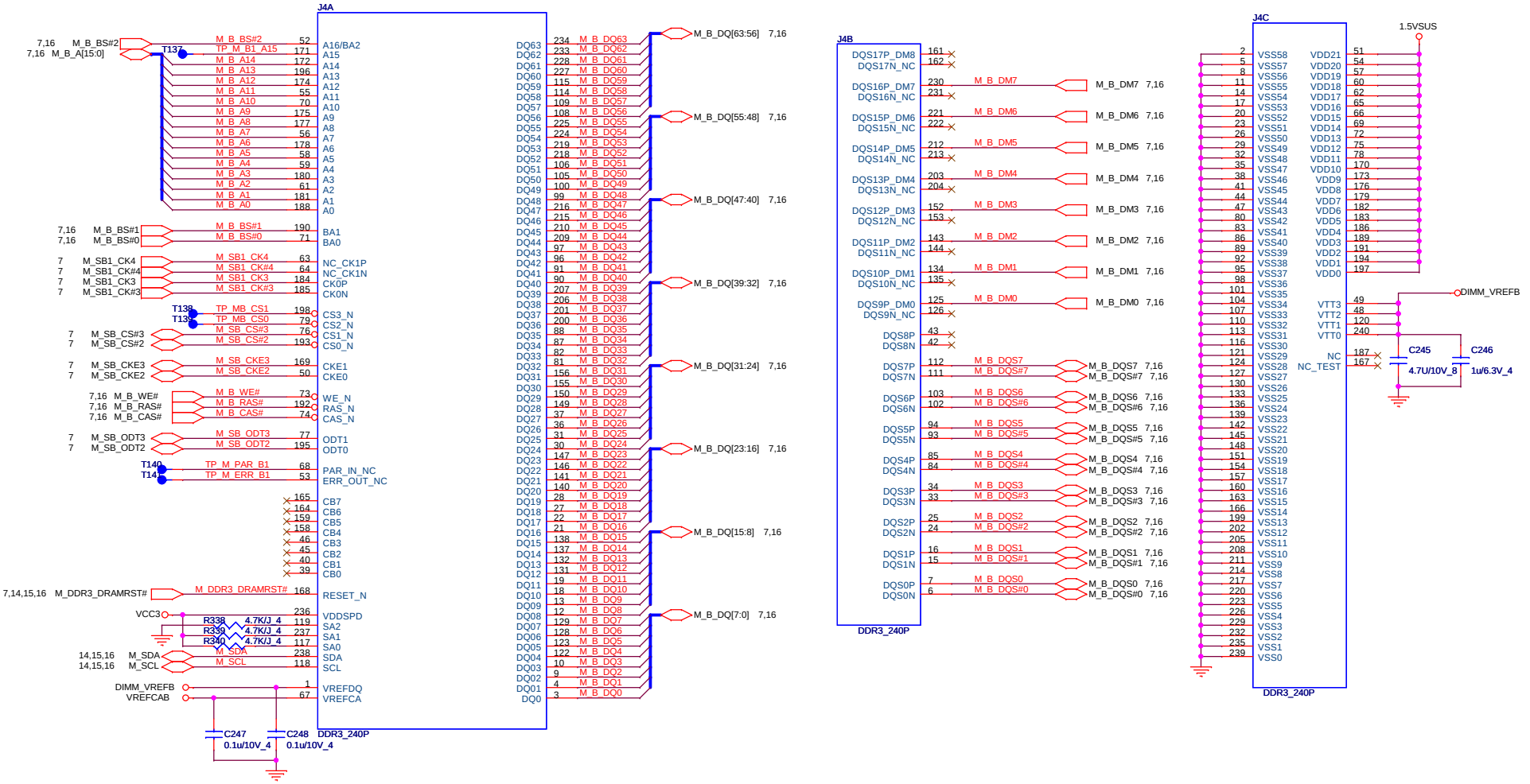
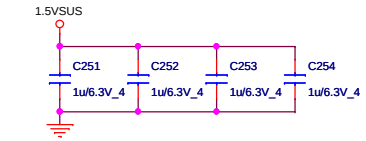
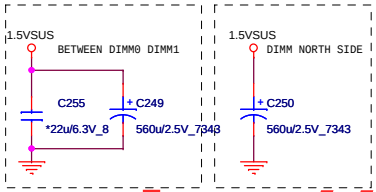
Size	Document Number	Rev
	DDR3 CHANNEL B DIMM0	1A
Date: Monday, March 09, 2009	Sheet 16 of 34	







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Size	Document Number	Rev
	DDR3 CHANNEL B DIMM1	1A
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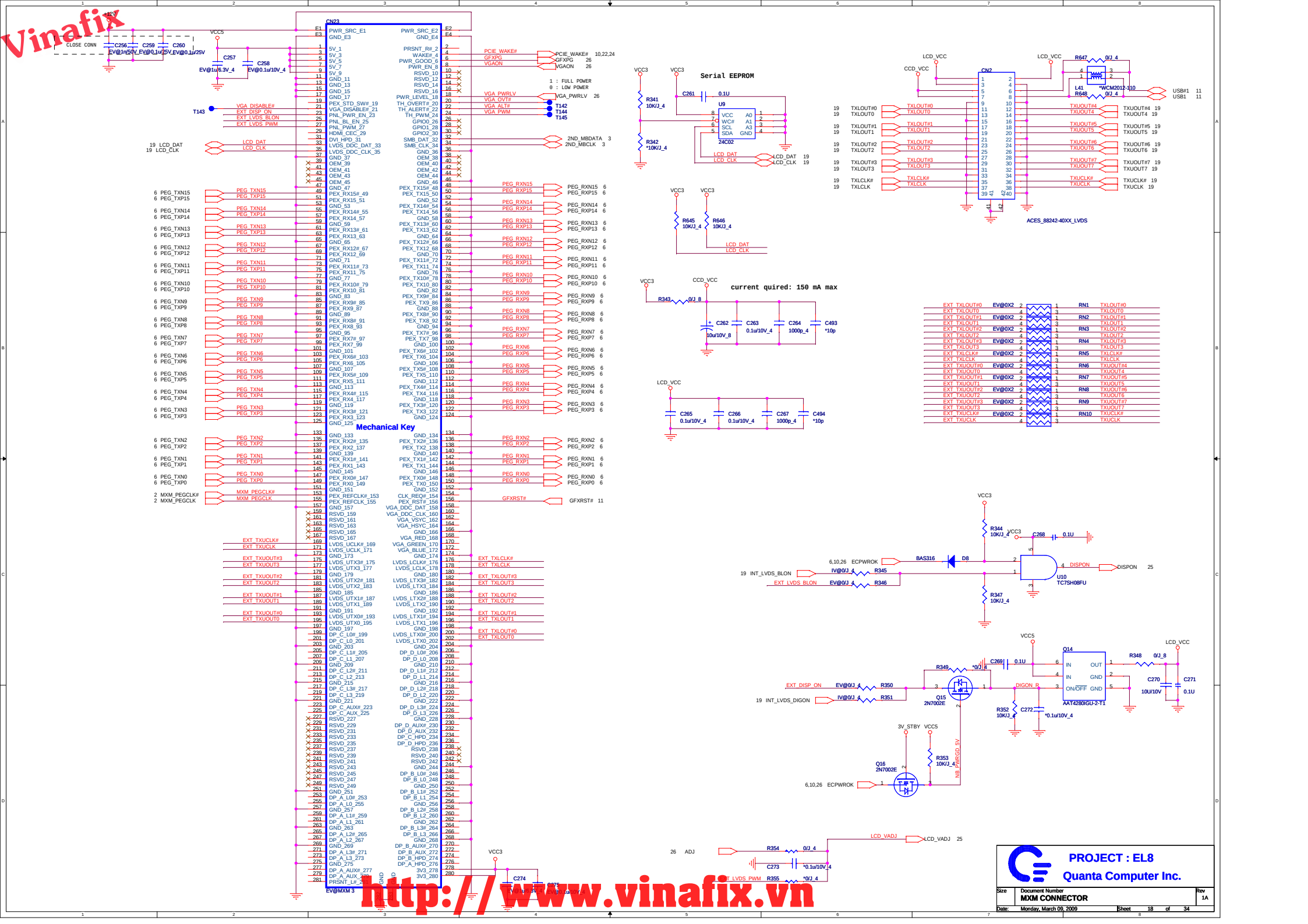
CN23
Mechanical Key
EV@MXM 3
Serial EEPROM
current quired: 150 mA max
CN2
ACES_88242-40XX_LVDS
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Quanta Computer Inc.
MXM CONNECTOR
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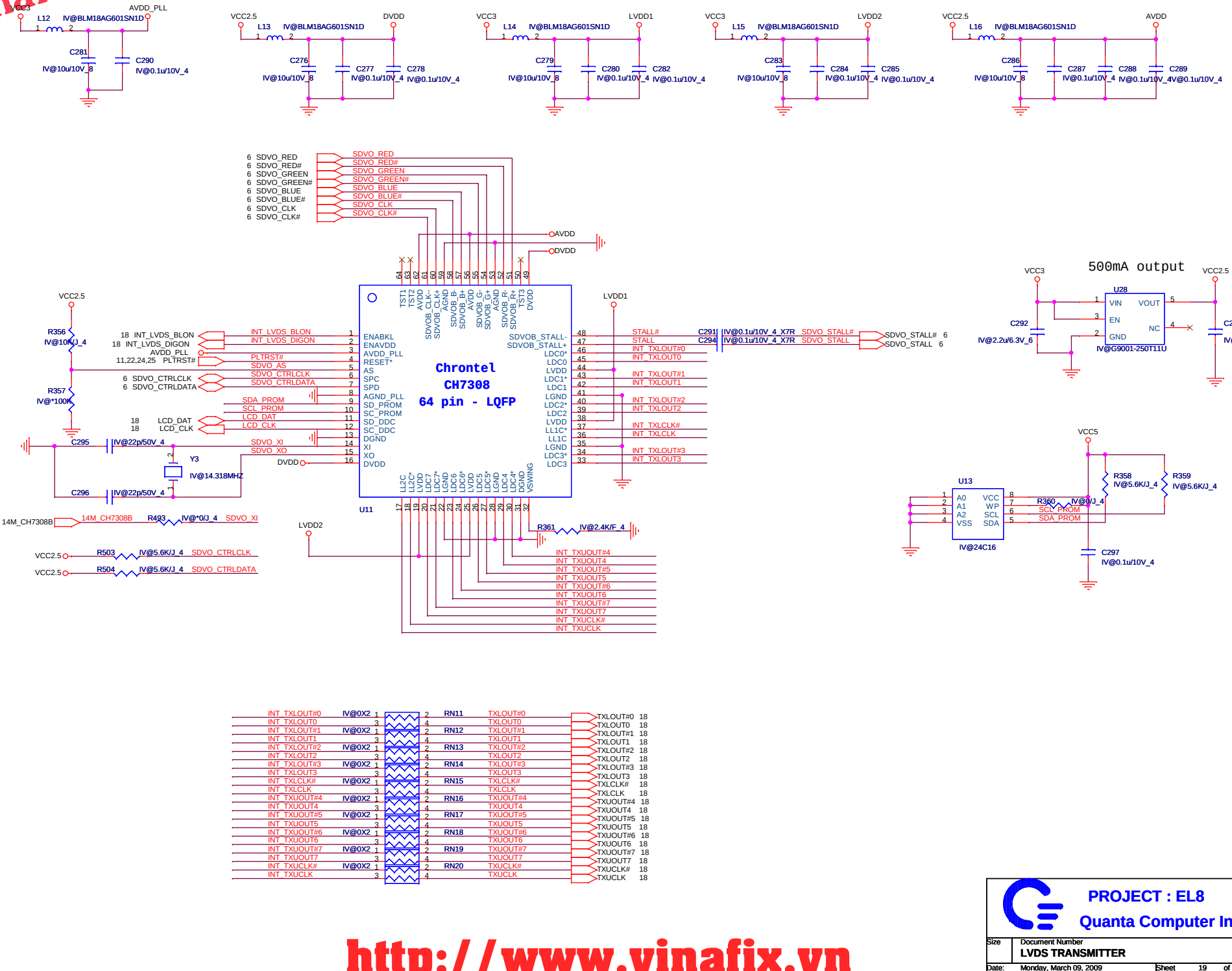
http://www.vinafix.vn



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Size	Document Number	Rev
	LVDS TRANSMITTER	1A

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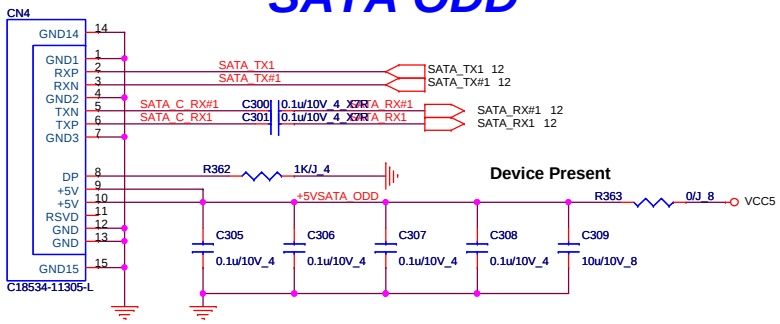
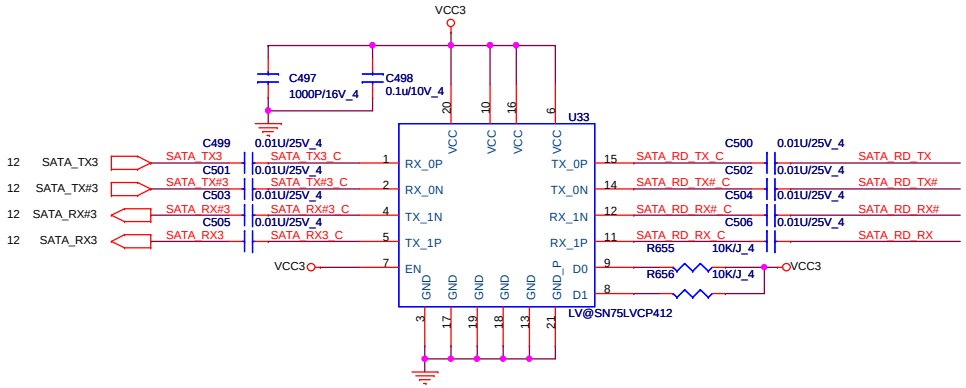
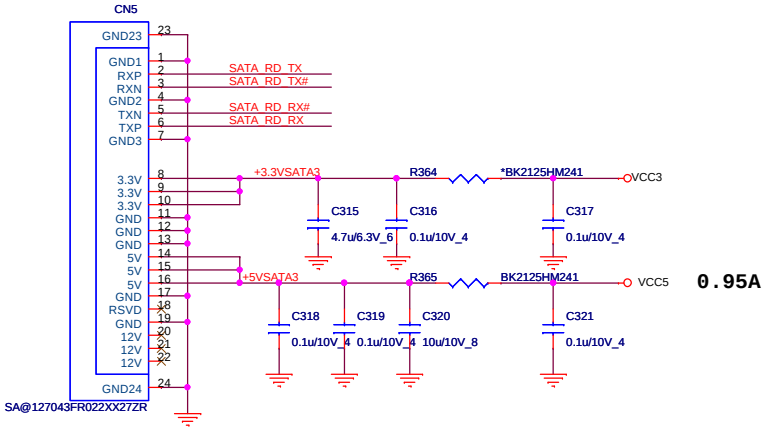
SATA ODD

2.1A



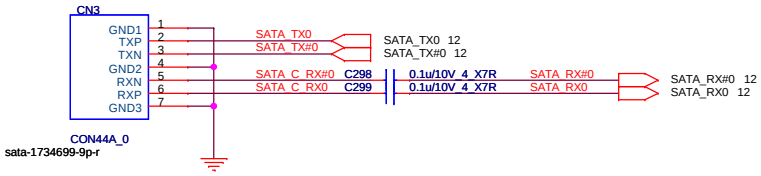


2nd SATA HDD(2.5")



0.95A

SATA HDD(3.5")



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Quanta Computer Inc.

Size	Document Number	Rev
	3.5HDD/2.5HDD/ODD	1A
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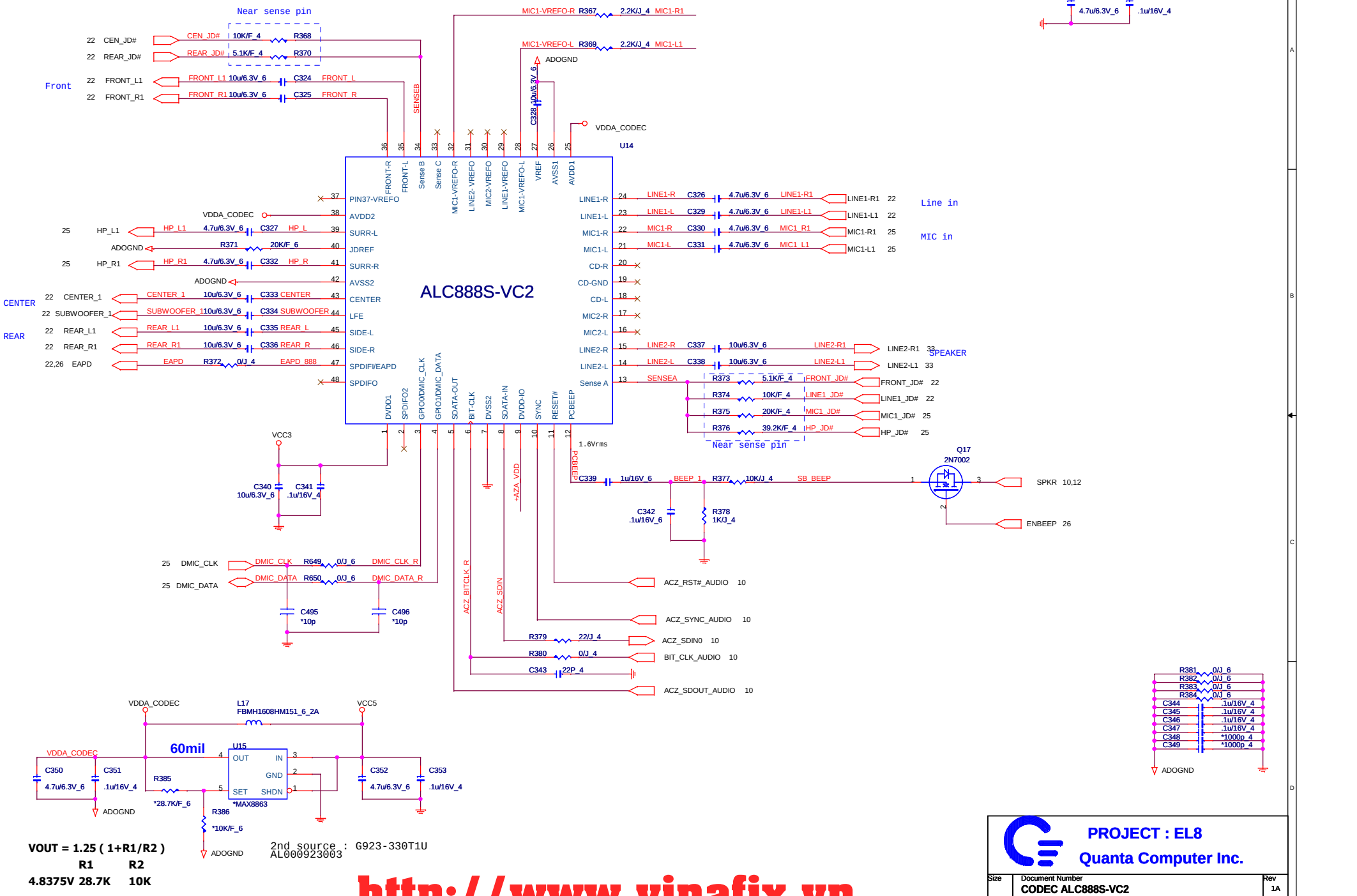
CODEC



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Quanta Computer Inc.

Size	Document Number	Rev
	CODEC ALC888S-VC2	1A
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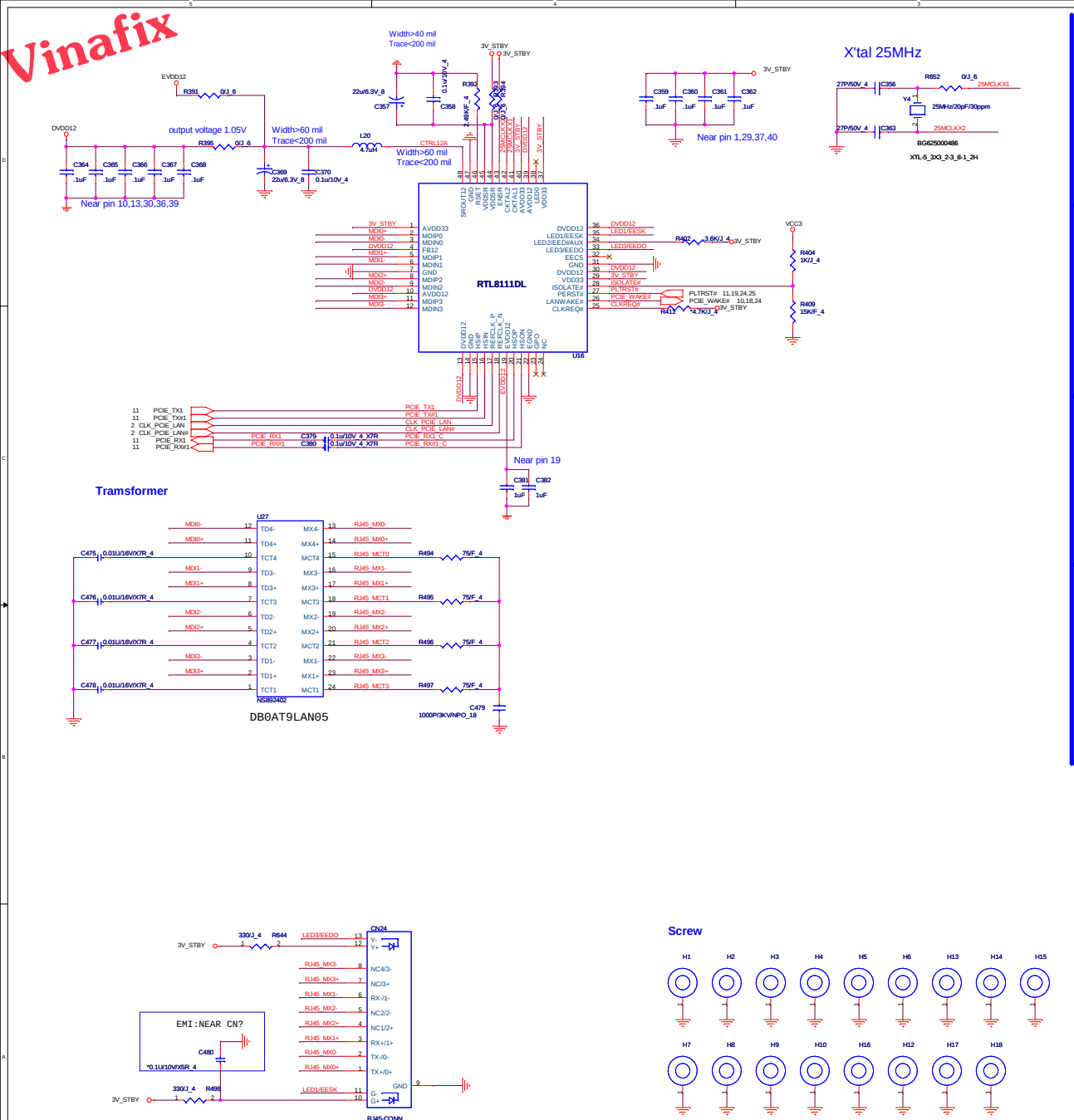
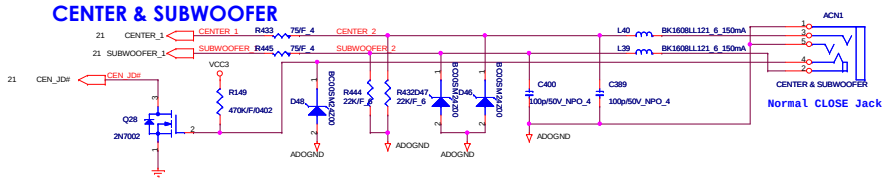


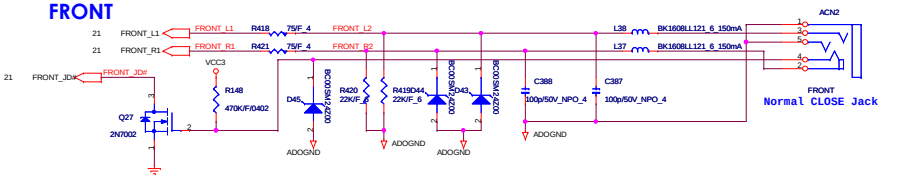
Tramsformer

Screw

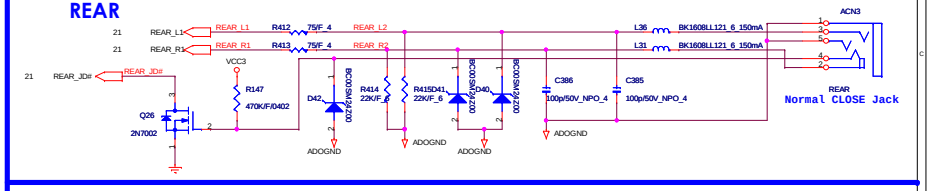
CENTER & SUBWOOFER



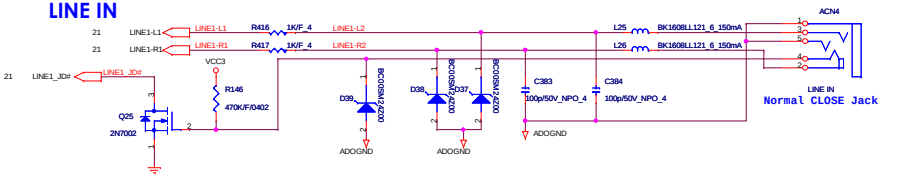
FRONT



REAR

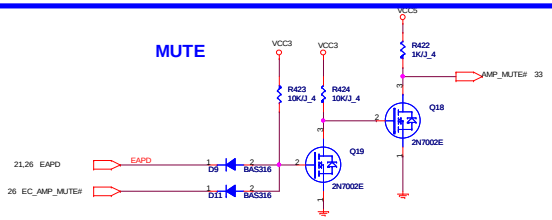


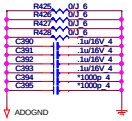
LINE IN



EC_AMP_MUTE#	EAPD	HP_MUTE#	AMP_MUTE#
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

MUTE





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Size	Document Number	Rev
	LAN/Audio jack	1A
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REAR USB PORT X4

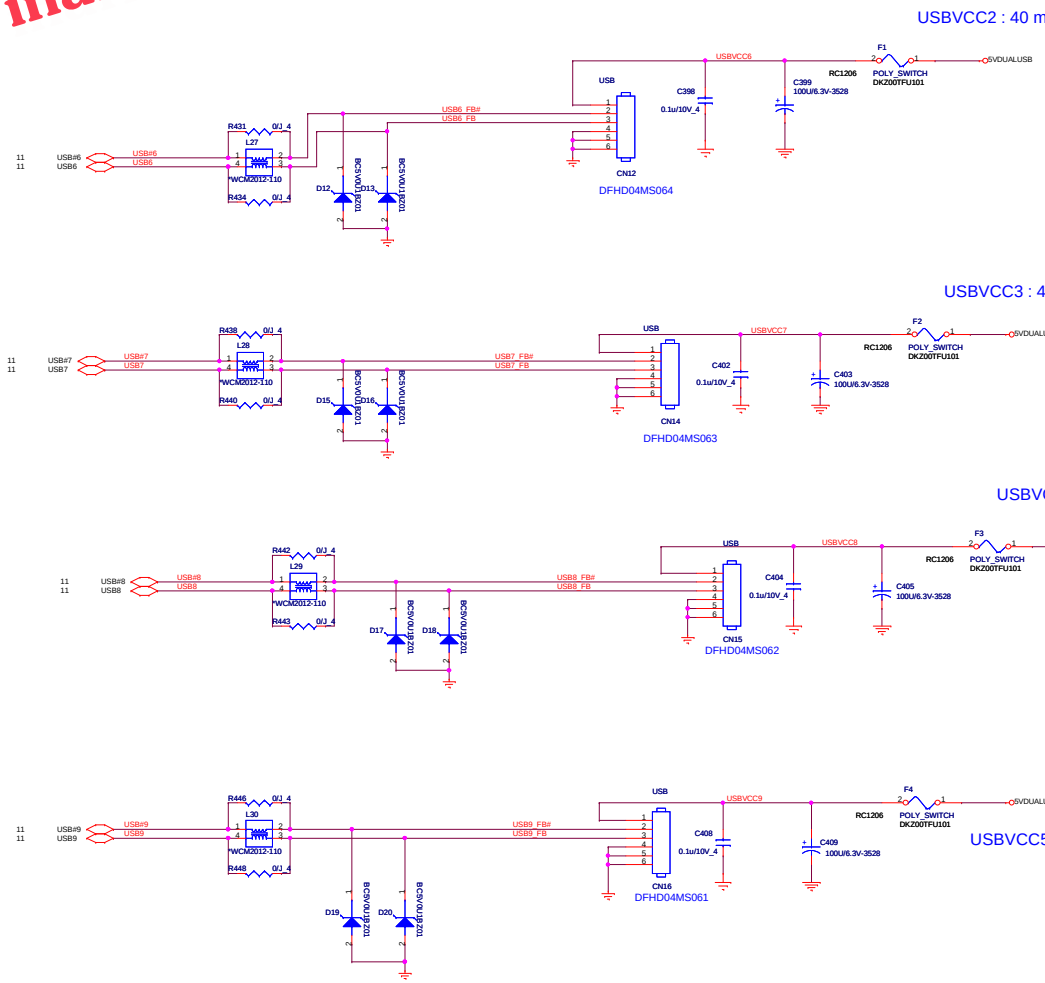
USBVCC2 : 40 mil

USBVCC3 : 40 mil

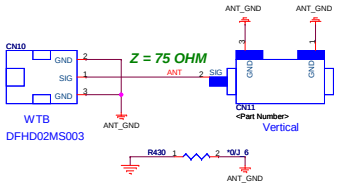
USBVCC4 : 40 mil

USBVCC5 : 40 mil

160mils

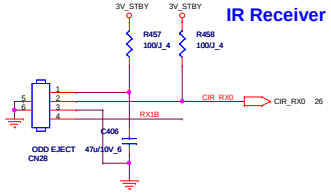


TV ANT. CONNECTOR

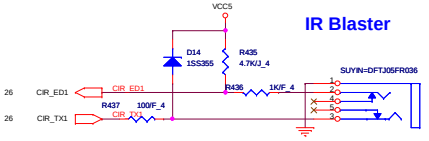


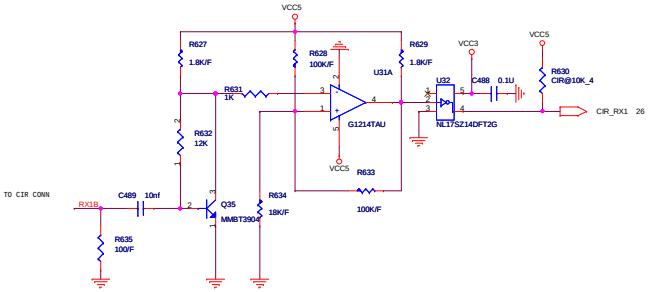
ESATA CONN

IR Receiver

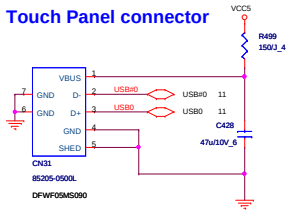


IR Blaster

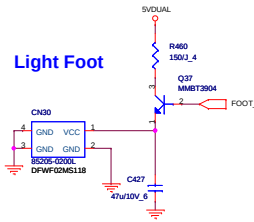




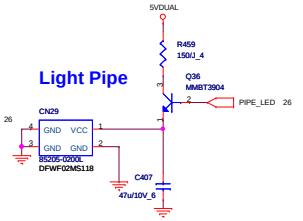
Touch Panel connector



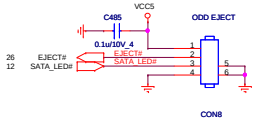
Light Foot



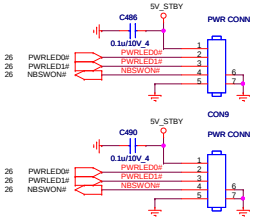
Light Pipe



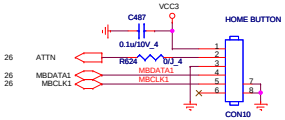
ODD BUTTON



POWER BUTTON



HOME BUTTON



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Quanta Computer Inc.

Size	Document Number	Rev
	USB CONN	1A
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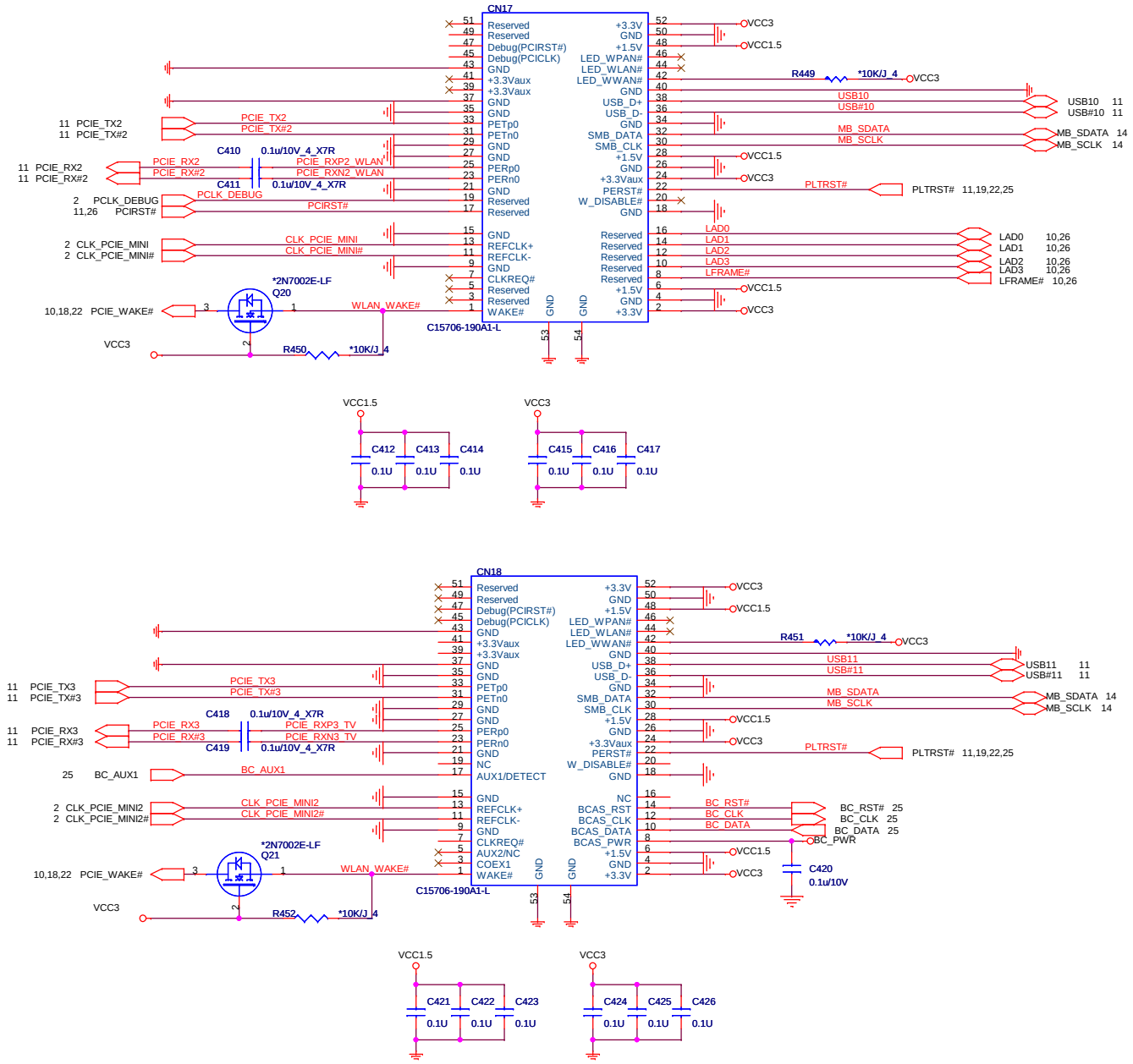

PROJECT : EL8
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCIE(WLAN/TV)	1A
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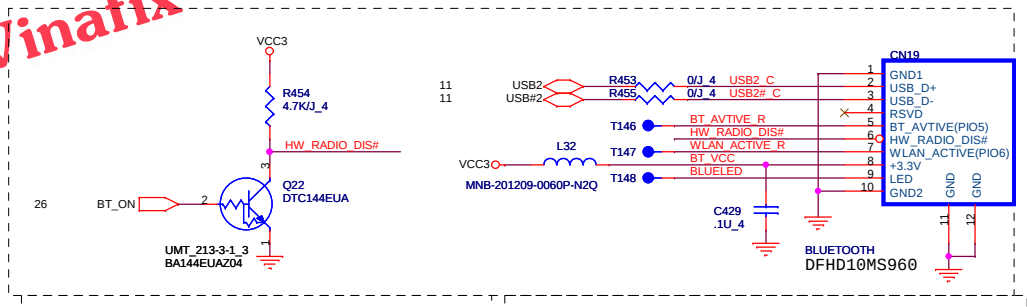

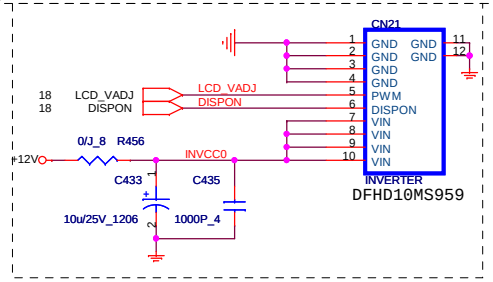

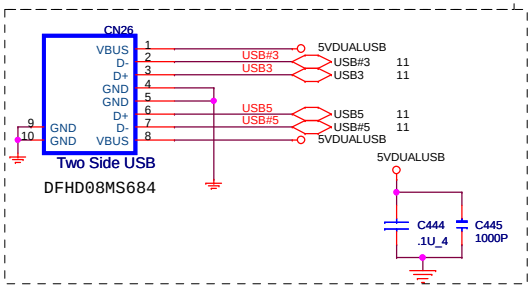

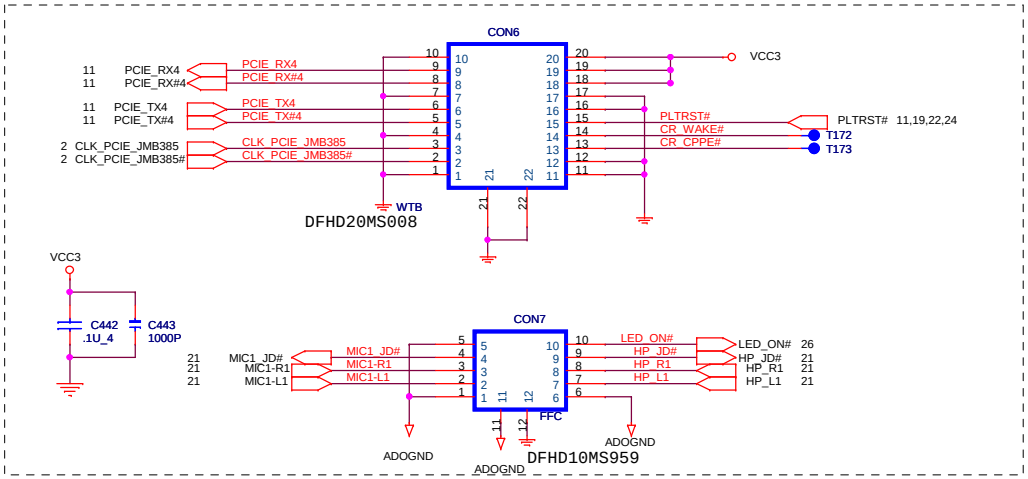

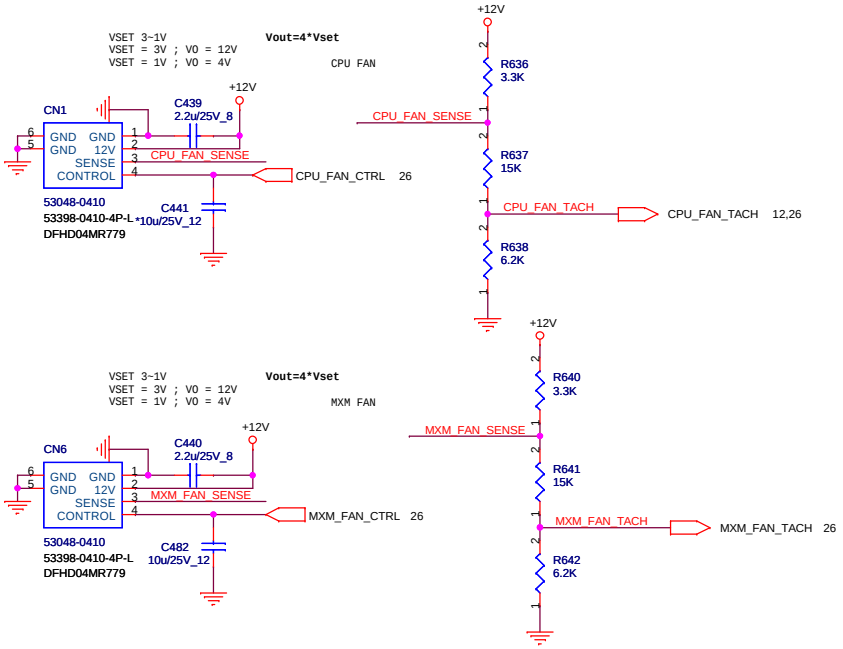

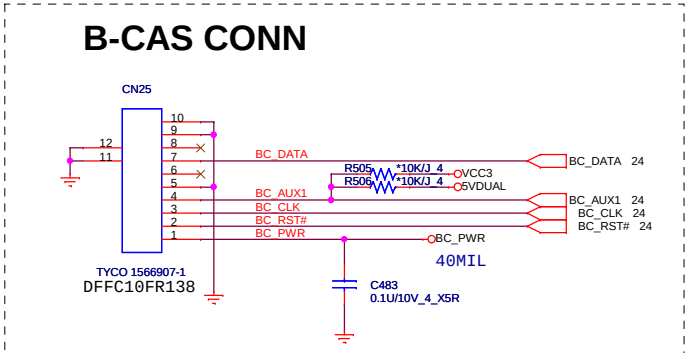

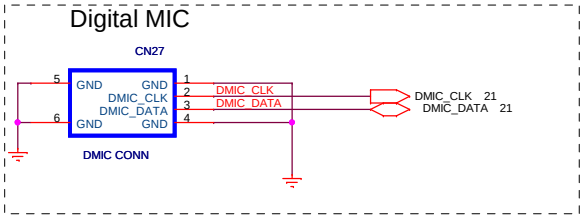

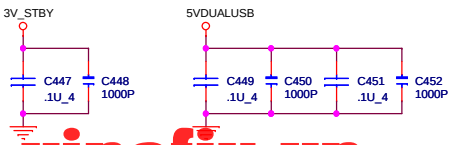

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Size	Document Number	Rev
	CONNECTOR	1A
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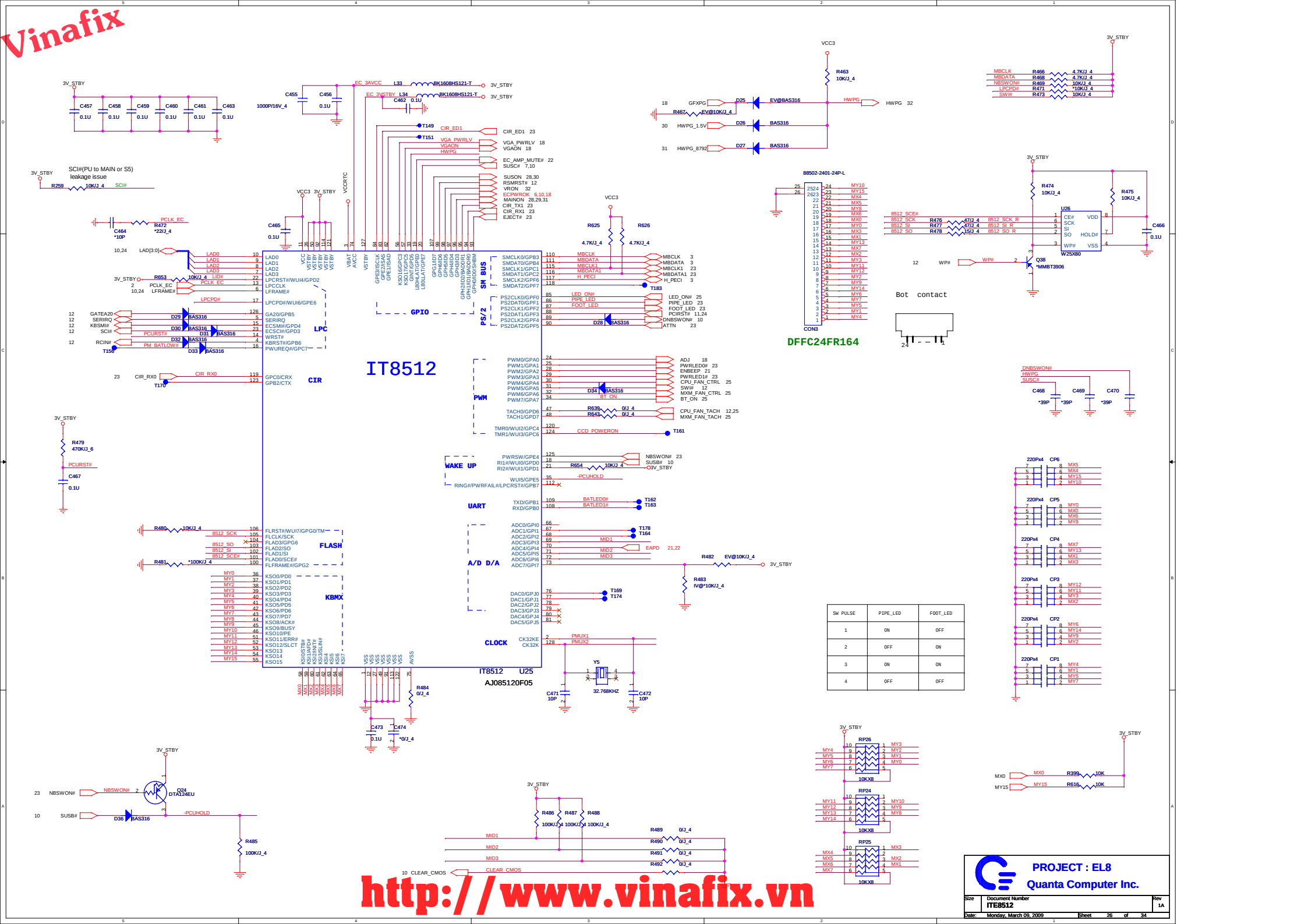
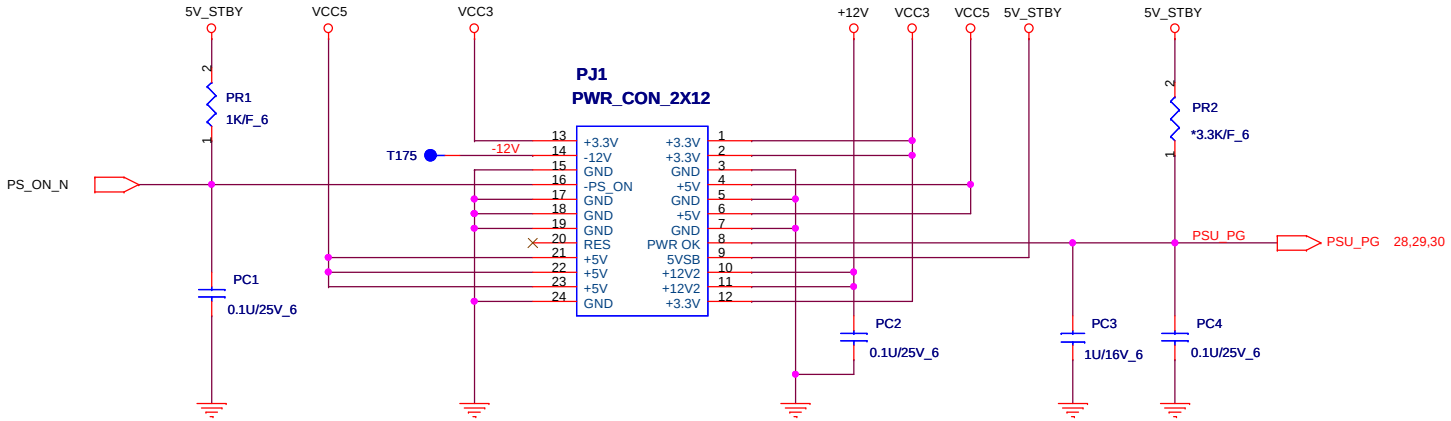


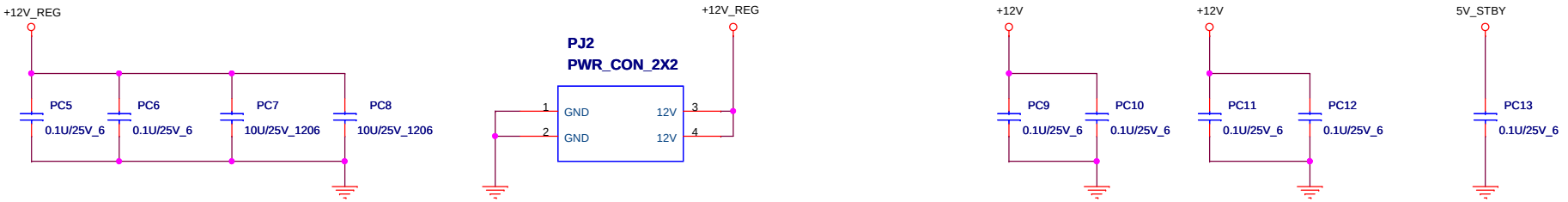
SW PULSE	PIPE_LED	FOOT_LED
1	ON	OFF
2	OFF	ON
3	ON	ON
4	OFF	OFF

PSU 24PIN Connector



P3V3_STB : Stand-by power source only
P3V3 : Normal power source only
P3V3_DUAL : Both power source switching

4PIN +12V_REG for CPU_CORE



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	PWR_CONNECTOR	1A
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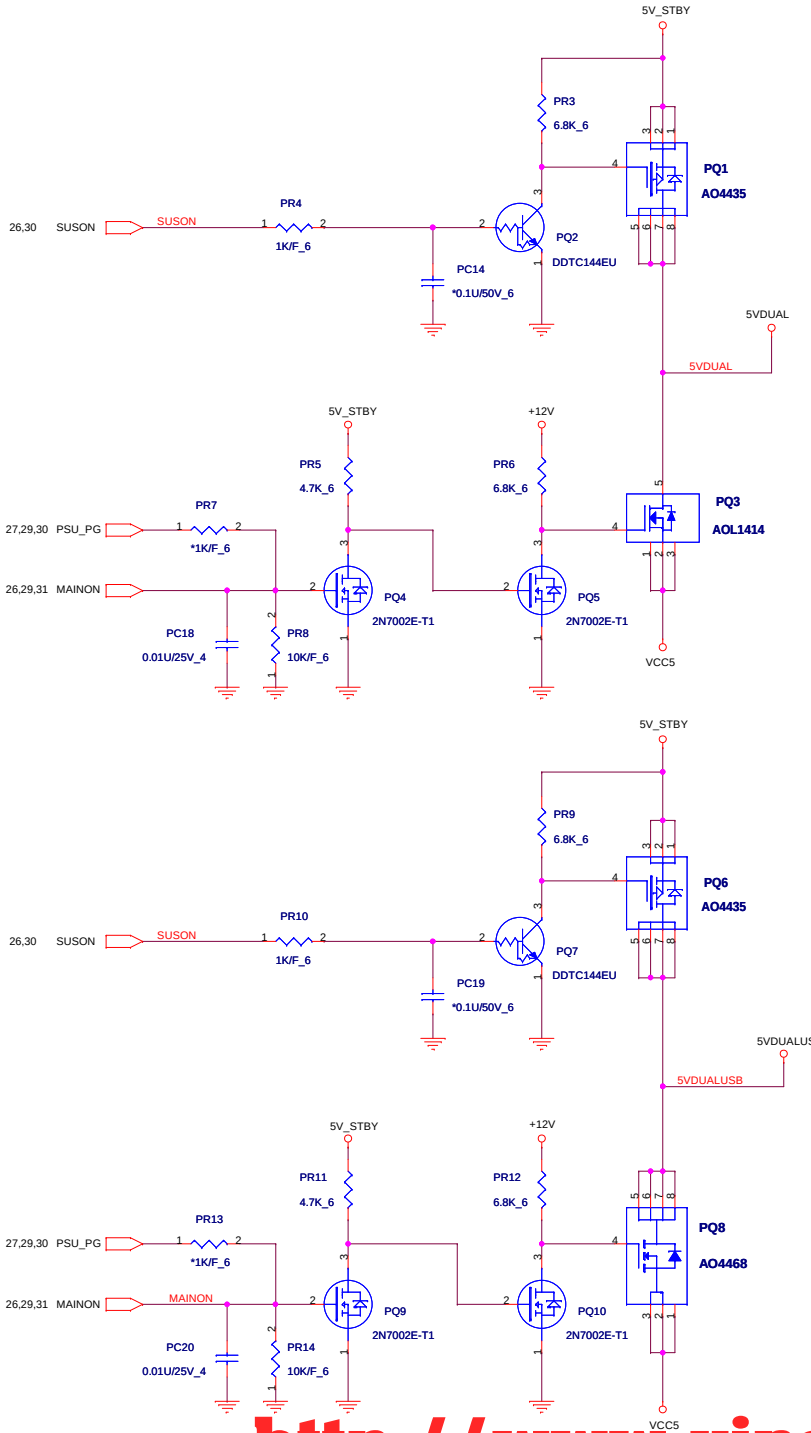
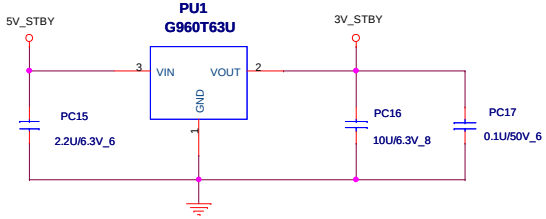
5VDUAL, 5VDUALUSB, 3V_STBY



for EC



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	5VDUAL, 5VDUALUSB & 3V_STBY	1A
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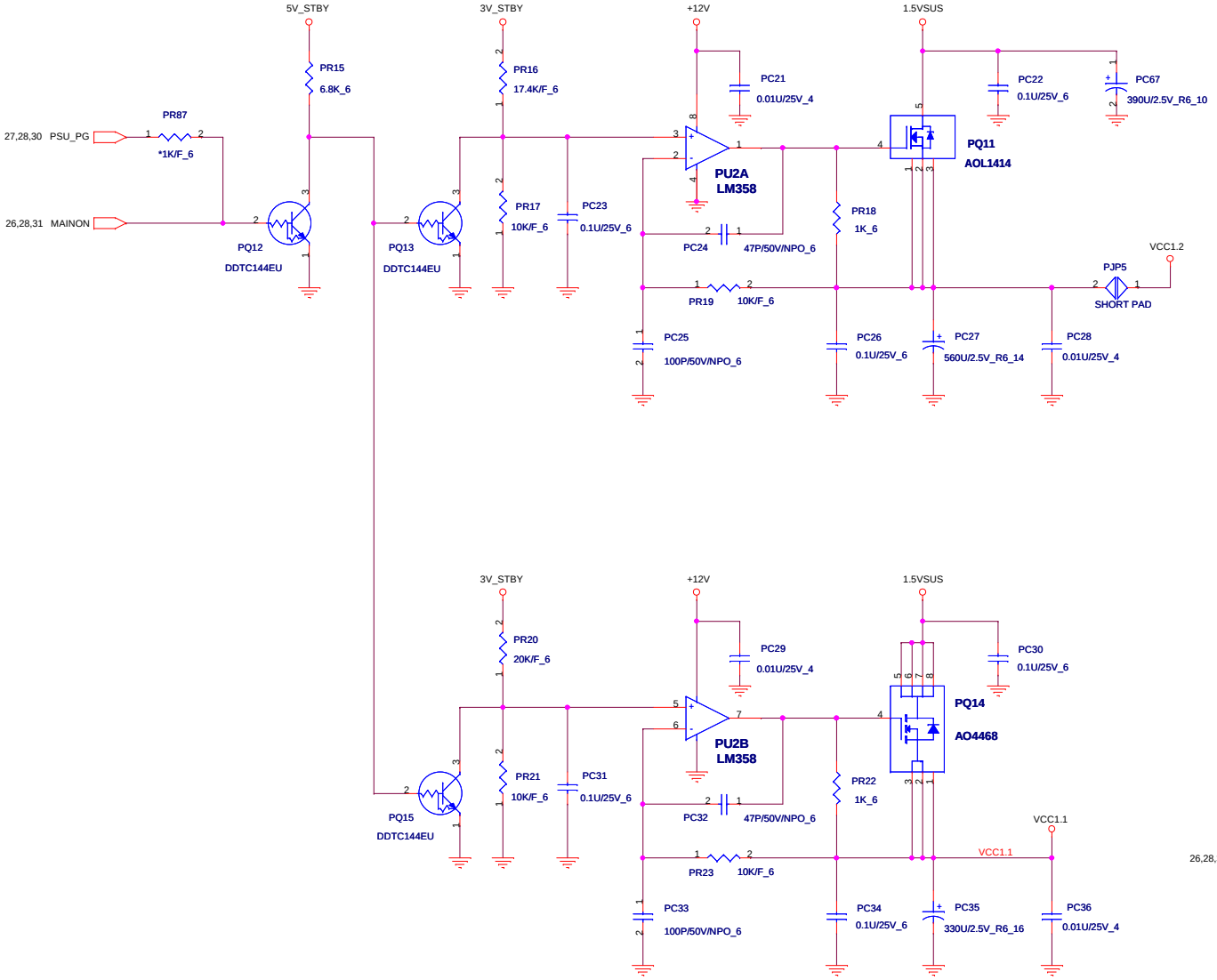
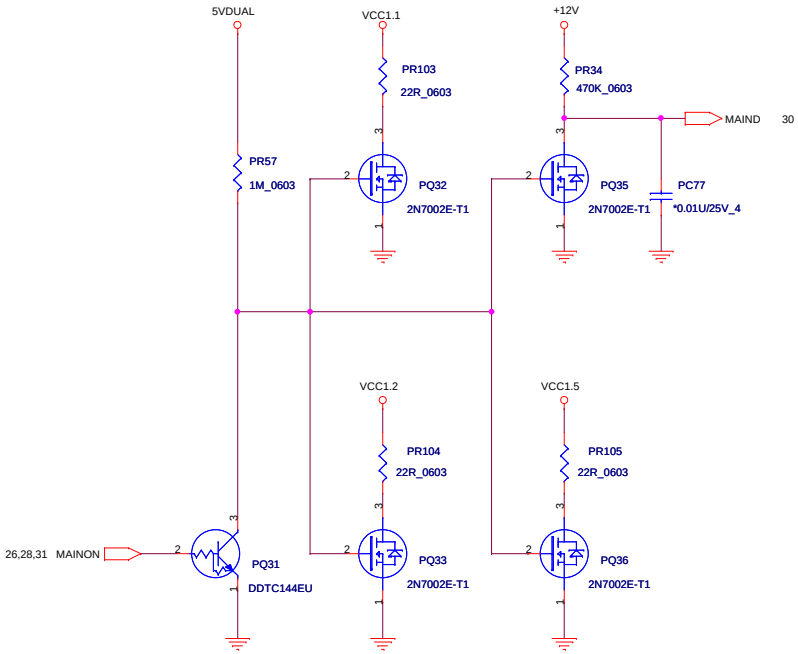
VCC1.2, VCC1.1





For ICH10

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	VCC1.1 & VCC1.2	1A
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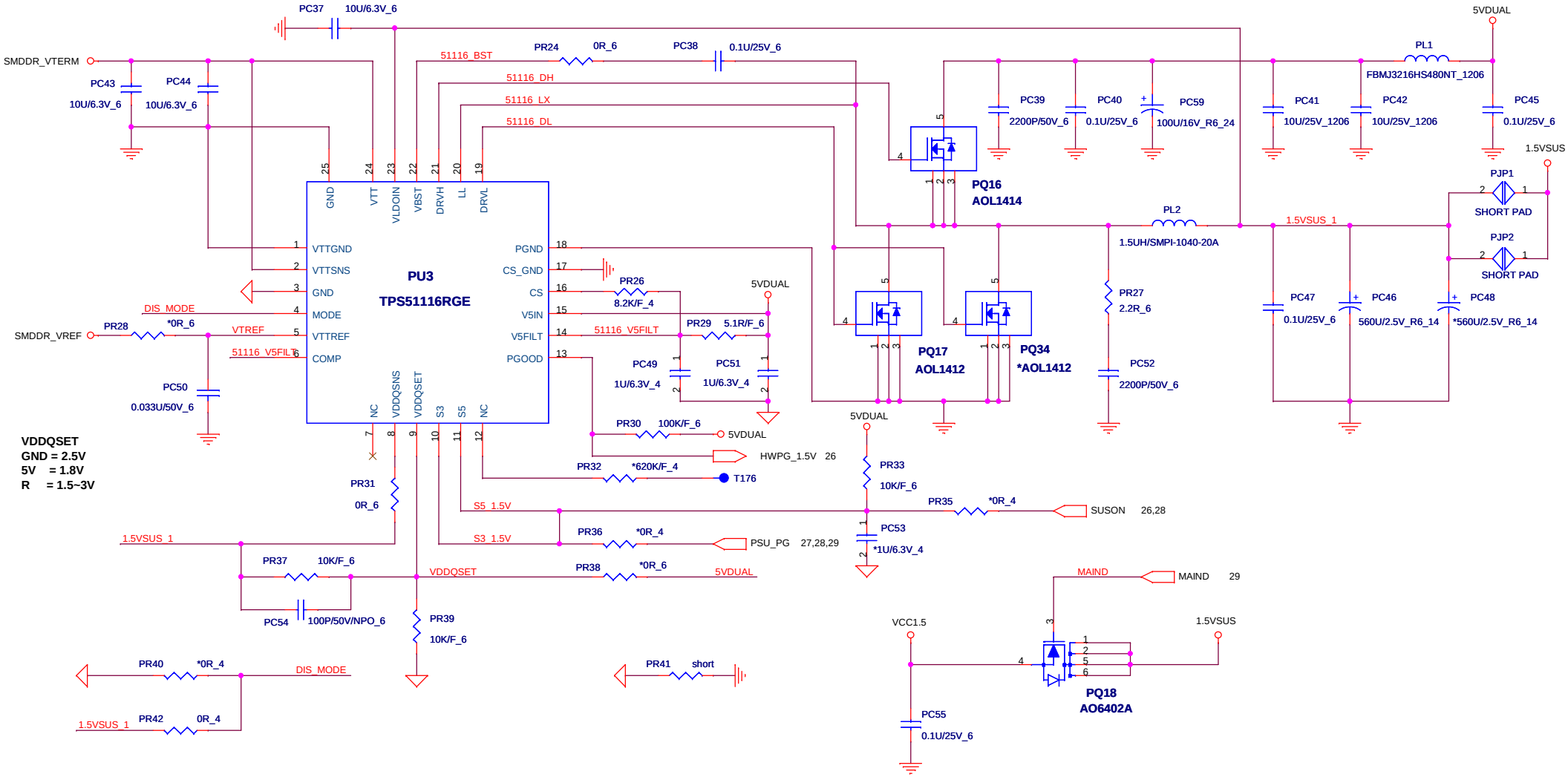
DDR3 1.5V(TPS51116)



del_IL=(5V-1.5V)x1.5V/(1.5ux400Kx19V)=4.6A

(10uAxPR26/Rdson)+del_IL/2=Iocp

(10uAx8.2K/4.6m)+del_IL/2=20.1A

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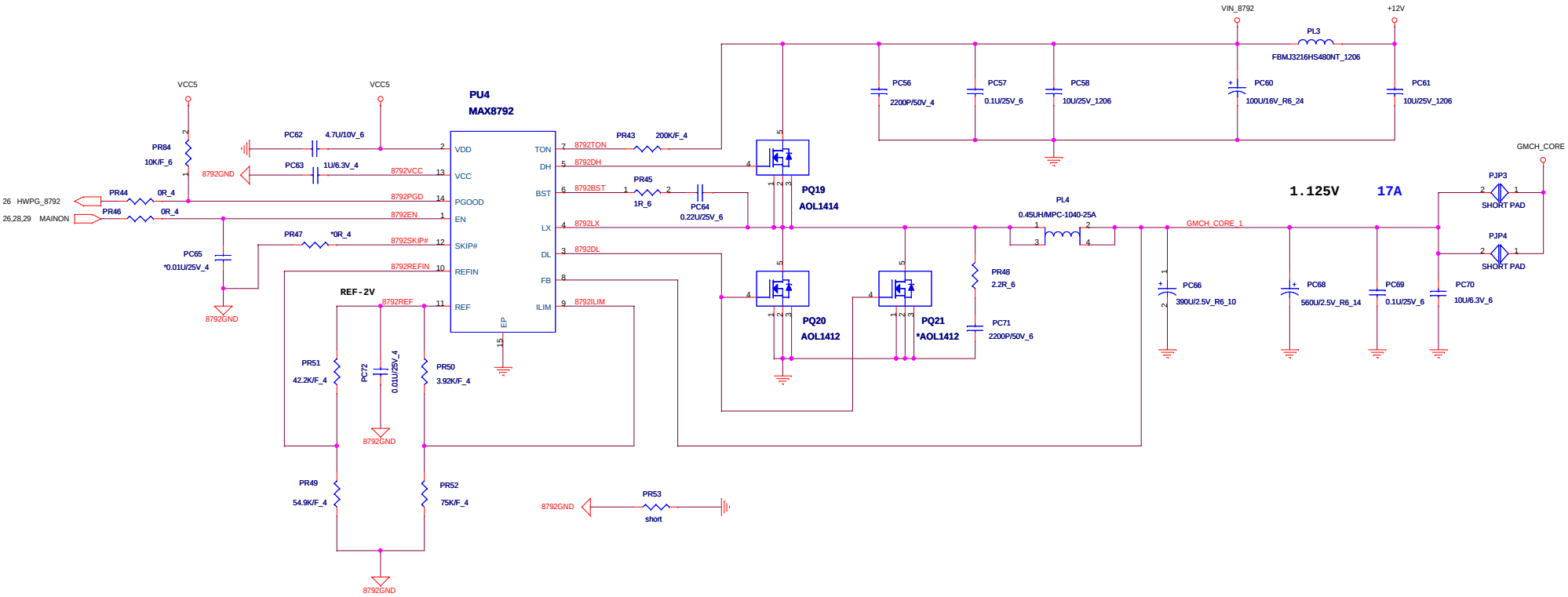
G43 GMCH_CORE



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	GMCH_CORE	1A

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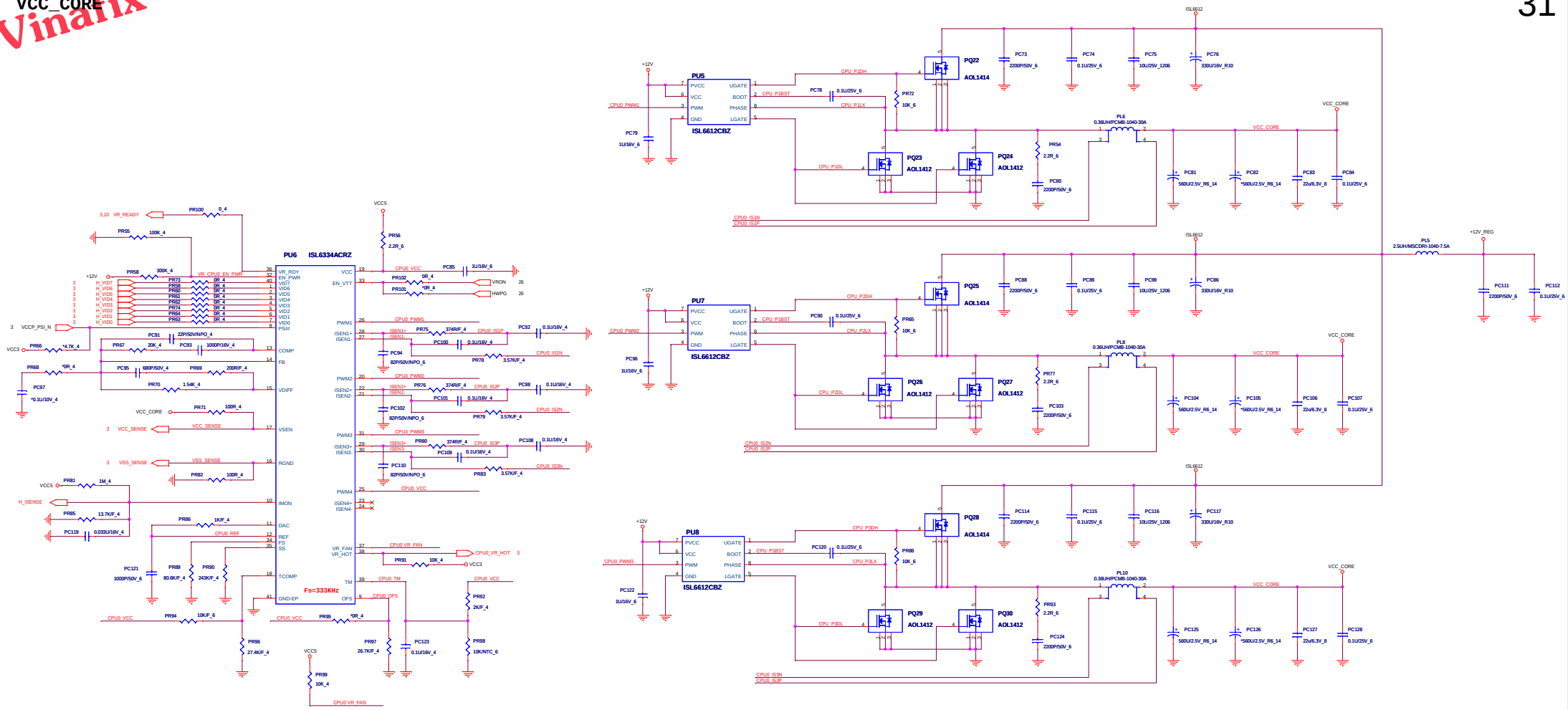

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VCC_CORE
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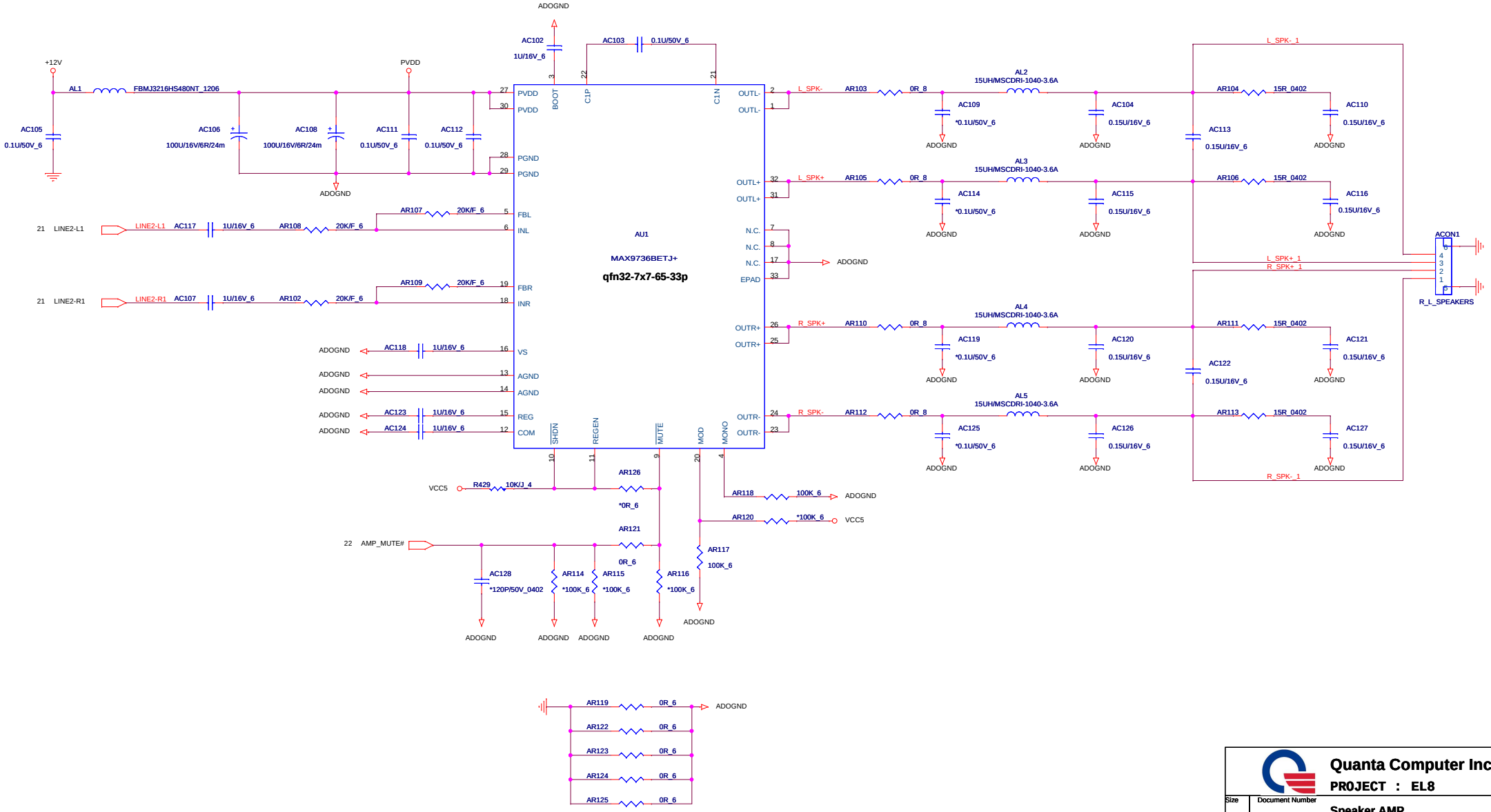
Speaker AMP.



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	Speaker AMP.	1A
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