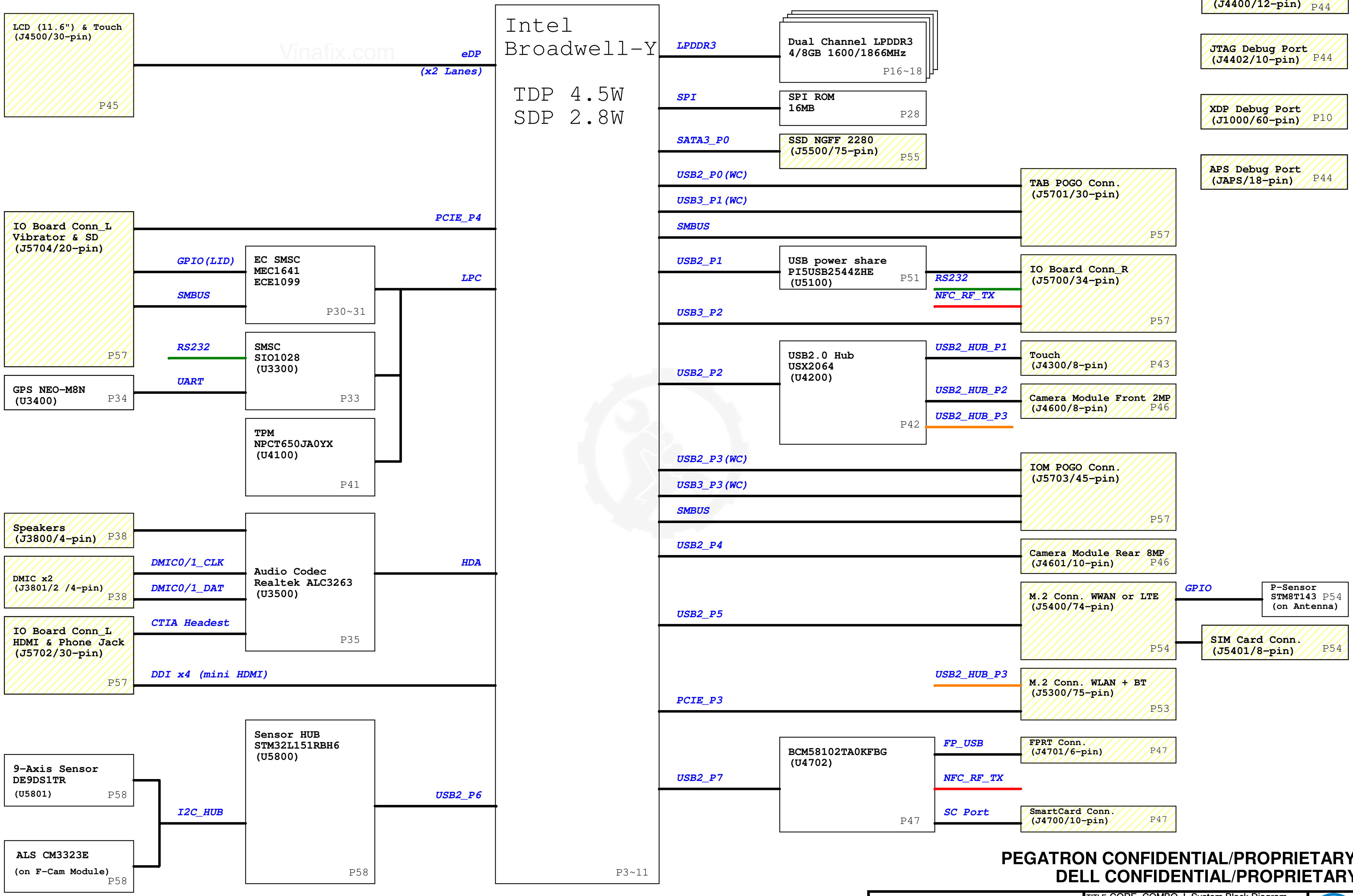
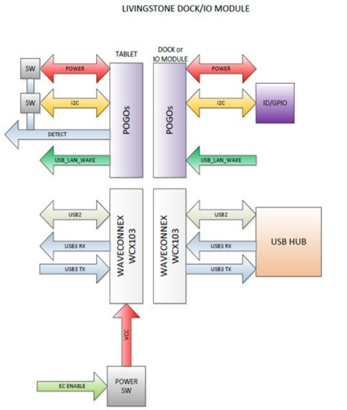
Livingstone Tablet CORE_L System Block Diagram (X04)



TITLE CORE_COMBO_L System Block Diagram			
DWG NO. CORE_L		REV. 2.0	
DATE Wednesday, May 06, 2015		SHEET 1 of 99	

BDW PCIe/USB3.0/SATA Port Map Configuration

PCIe	USB3.0	SATA	Destination
	USB3.0 1		Dock
	USB3.0 2		USB3.0 Port
PCIe 1	USB3.0 3		IOM_ POGO_L
PCIe 2	USB3.0 4		NC
PCIe 3			WLAN
PCIe 4			Card Reader
PCIe 5			NC
PCIe 6		SATA 3	NC
		SATA 2	NC
		SATA 1	NC
		SATA 0	SSD



BDW USB 2.0 Port Map Configuration

USB2.0	Destination
0	DOCK_POGO_L
1	USB3.0 Port
2	USB2.0 HUB
3	IOM_ POGO_L
4	Rear Cam (8M)
5	WWAN
6	Sensor Hub
7	FPR/SC/NFC (USH)

USB 2.0 HUB Port Map Configuration

USB2.0	Destination
1	TSC
2	Front Cam(2M)
3	WLAN
4	NC

BDW SMB/I2C Port Map Configuration

SMB / I2C	Destination
SMB	WWAN / XDP
SML0	NC
SML1	EC MEC1641
I2C0	NC
I2C1	NC

EC1641 SMB Port Map Configuration

SMB	Destination
SMB0	PCH
SMB1	IO Module
SMB3	Batt Left
SMB4	Dock
SMB5	Charger,USH,USB Hub
SMB7	Batt Right

BDW LPC Port Map Configuration

LPC	Destination
LPC	EC1641 / LPC Debug / SIO1028

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TITLE CPU(1)_***			
DWG NO. CORE_L		REV. 2.0	
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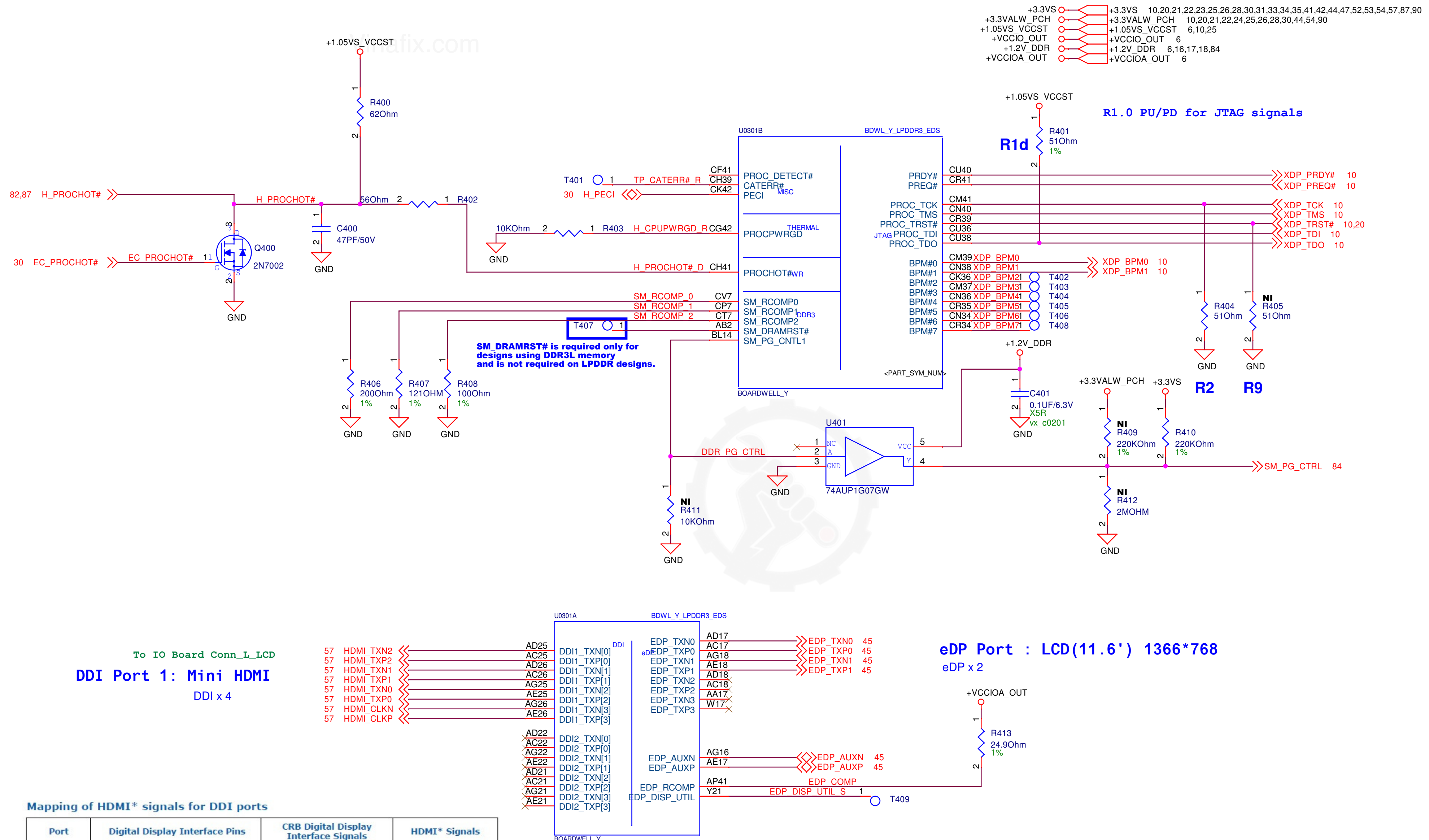
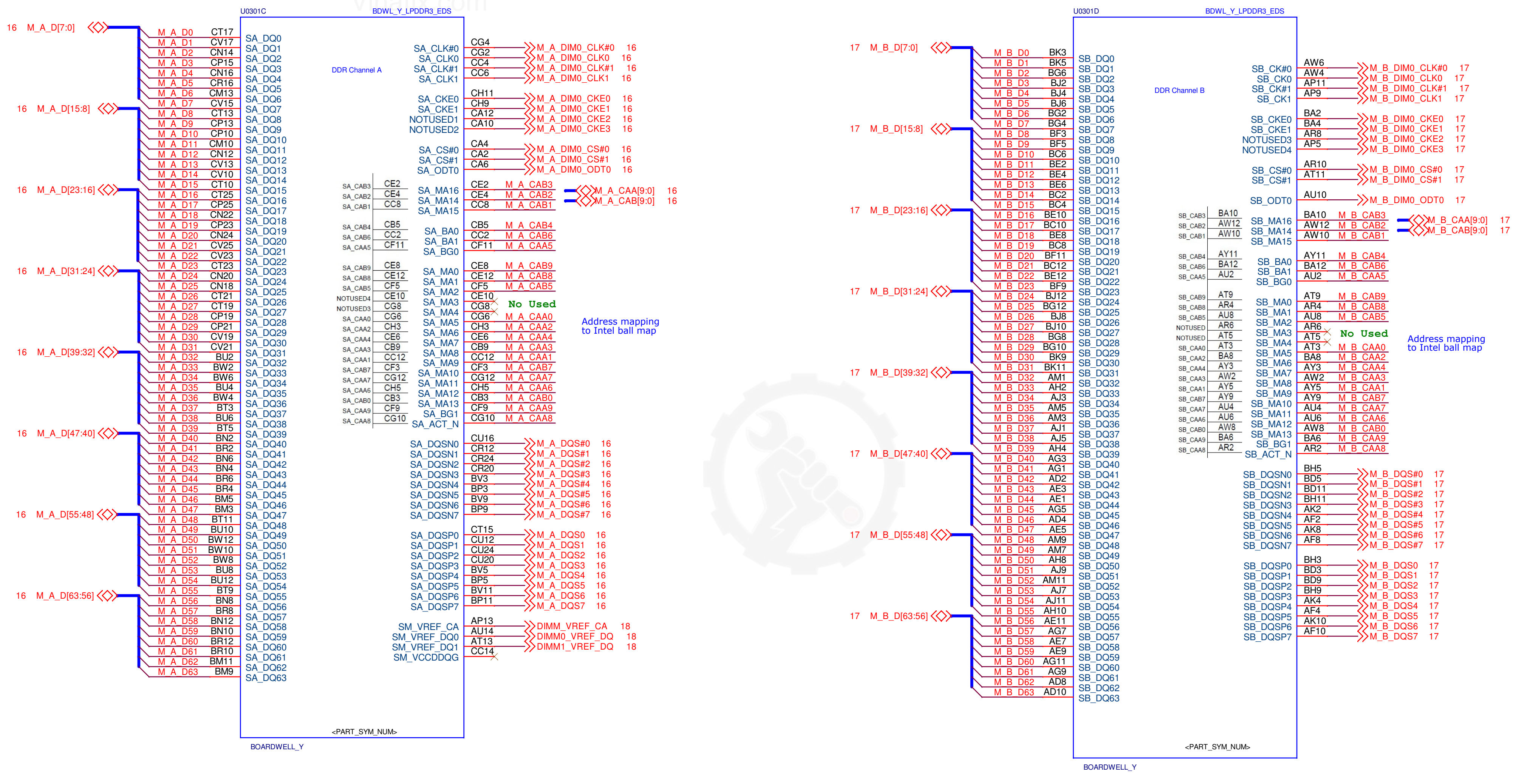


Mapping of HDMI* signals for DDI ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

TITLE CPU(2)_BPM,RCOMP,DDI.EDP
DWG NO. CORE_L
REV. 2.0
DATE Wednesday, May 06, 2015



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TITLE	CPU(3)_LPDDR3
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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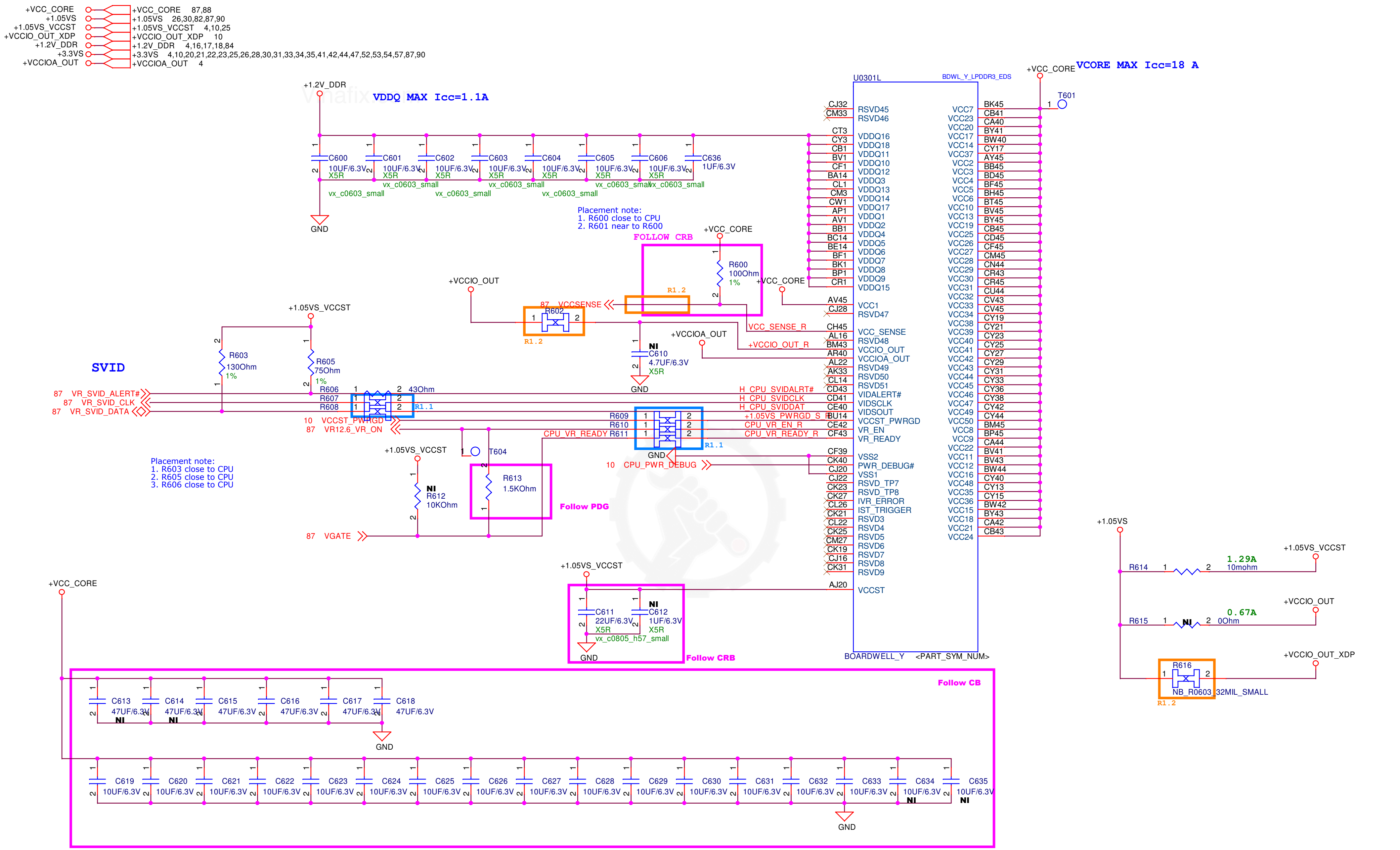

Decoupling guide from Intel (EE)

+VCORE 47uF * 4pcs (stuff)
10uF * 15Pcs (stuff)
10uF * 2pcs (non stuff)
47uF * 2pcs (non stuff)

Decoupling guide from Intel (EE)

VDDQ(+1.35V) 2.2uF * 4pcs (stuff)
10uF * 6pcs (stuff)

TITLE	CPU(4)_BDW POWER
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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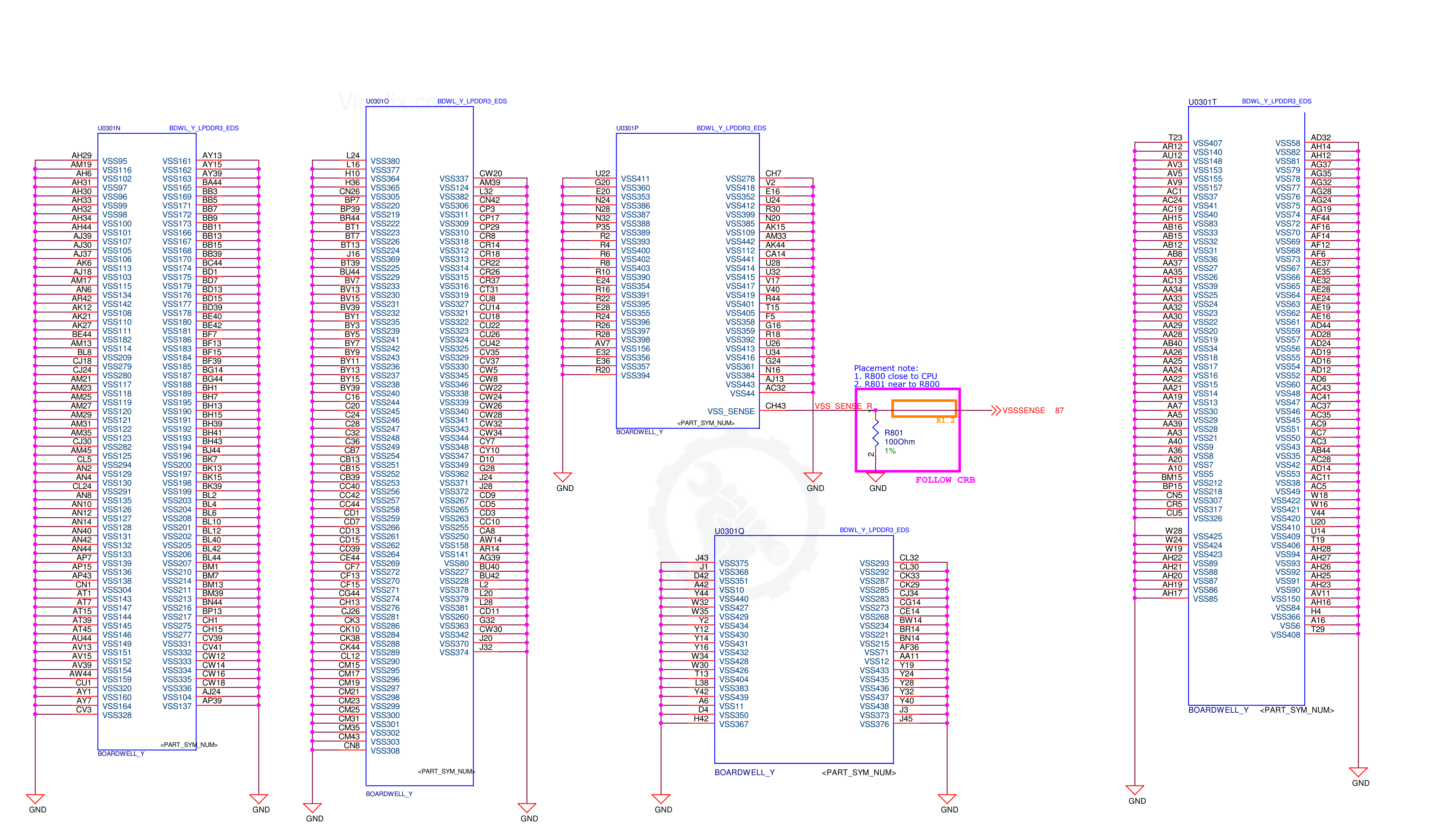
TITLE CPU(5)_****			
DWG NO. CORE_L		REV. 2.0	
DATE Wednesday, May 06, 2015		SHEET 7 of 99	



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TITLE CPU(6)_GND			
DWG NO.	CORE_L	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	8 of 99

CFG strapping information:

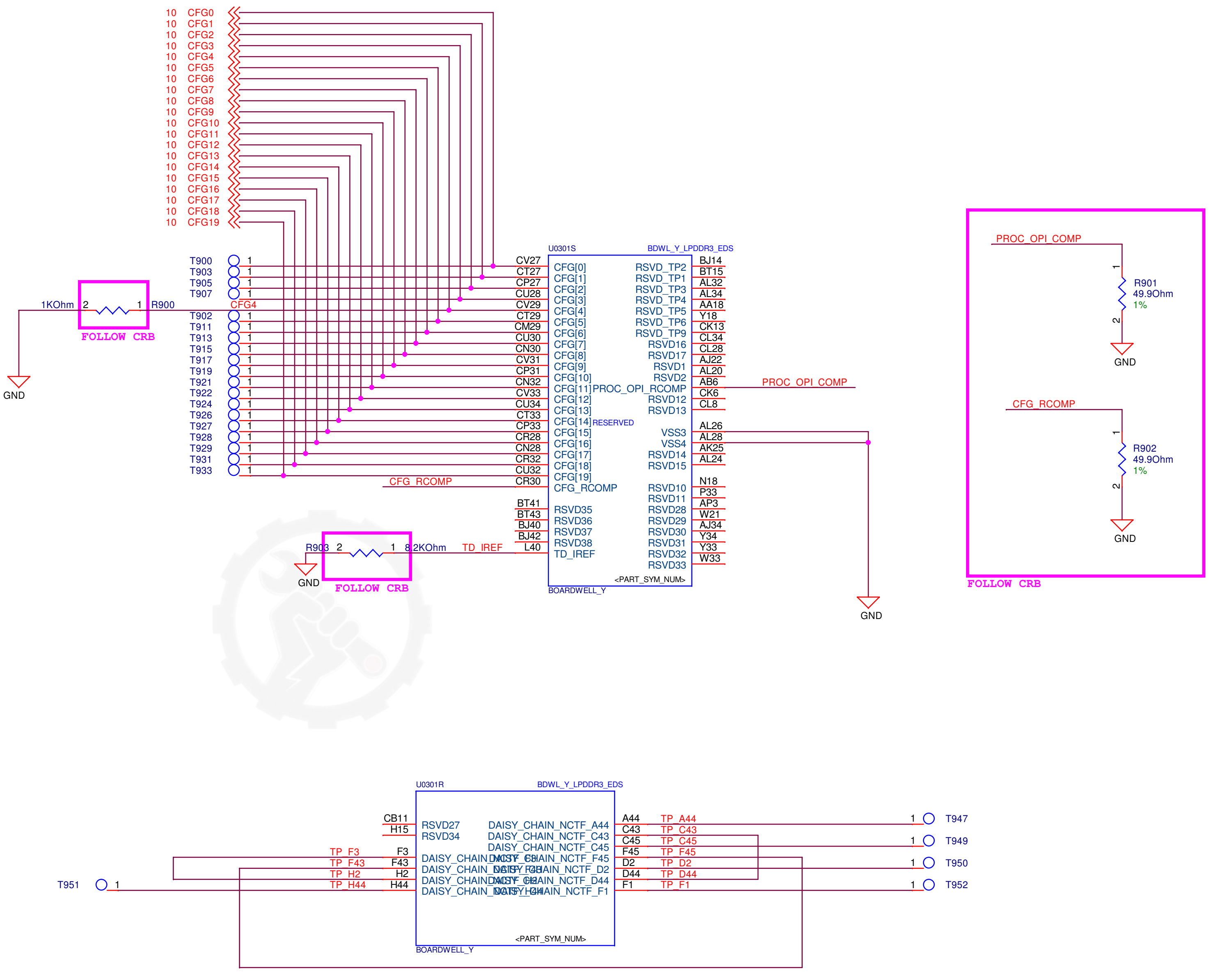
The CFG signals have a default value of '1'
CFG[20:0] - INT. PU

CFG[3:0]: Reserved configuration lane.
A test point may be placed on the board for these lanes.

CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[19:5]: Reserved configuration lanes.
A test point may be placed on the board for these lands.



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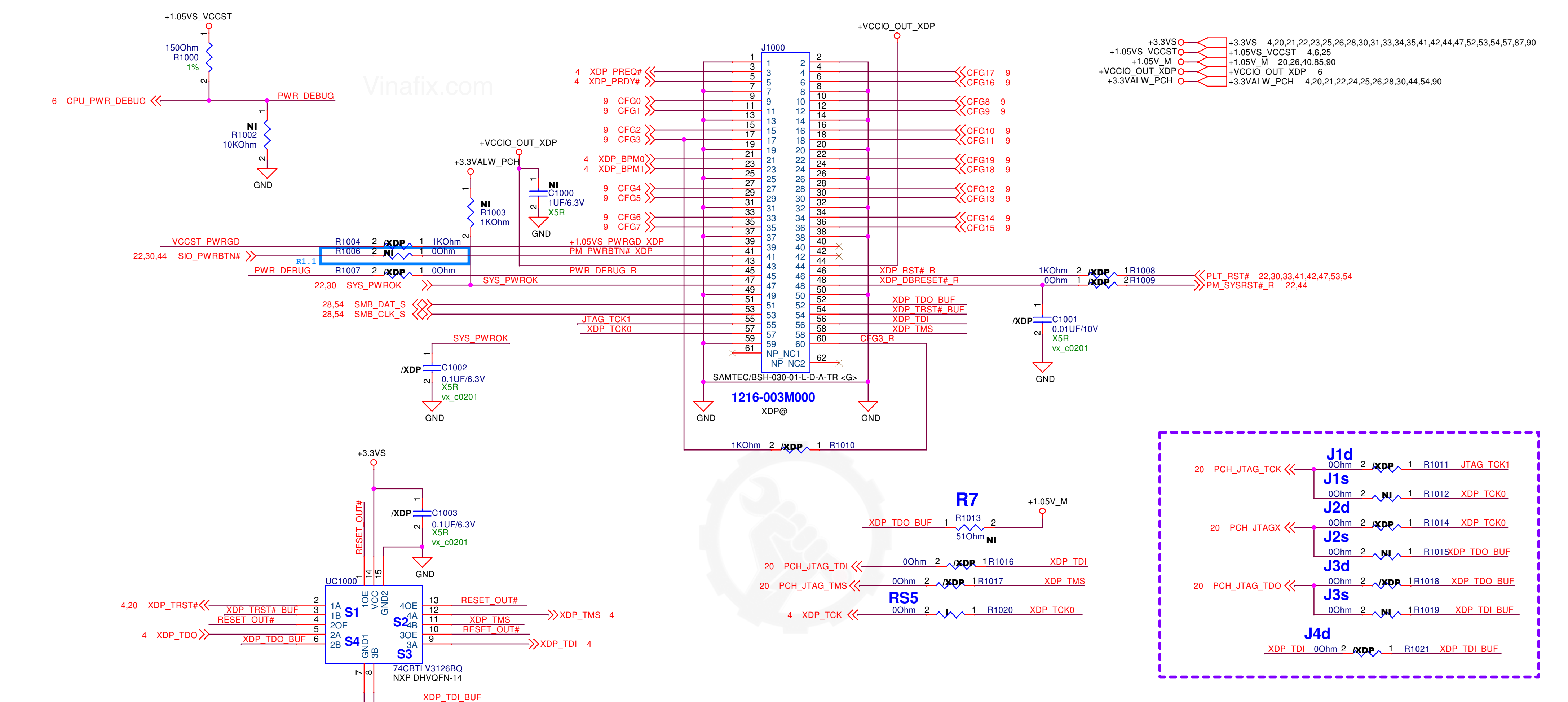
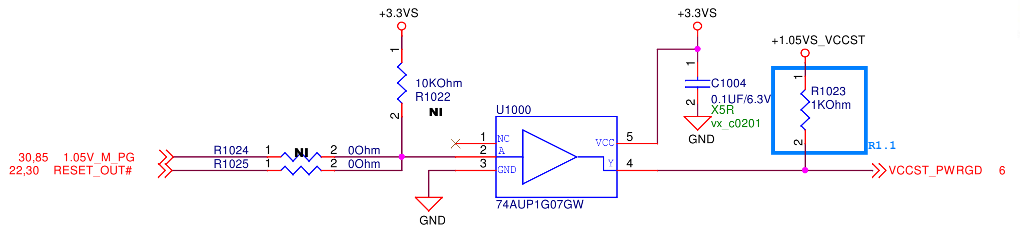
TITLE	CPU(7)_RESERVED		
DWG NO.	CORE_L	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	9 of 99

CPU XDP connector



Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In this topology, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s , J2s , J3s , R2, R3, R4, R5	R1, J1d, J2d, J3d , J4d



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TITLE CPU_PCH_XDP			
DWG NO.	CORE_L	REV.	2.0
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Version	Date	Page	Describtion
X00	2014-08-12		First Release
X01	2014-11-28	10	1. remove R1006 2. change R1023 to 1K ohm
		28	1. add CON2800 ROM Socket 2. remove R2816/R2817/R2818/R2819/R2820/R2821
		44	1. remove SPI Debug Port
		20	1. modify RTC circuit PN (X2000 / C2000 / C2003)
		30	1. modify R3052 to 10K ohm

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TITLE *****			
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TITLE *****	
DWG NO. CORE_L	REV. 2.0
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TITLE *****			
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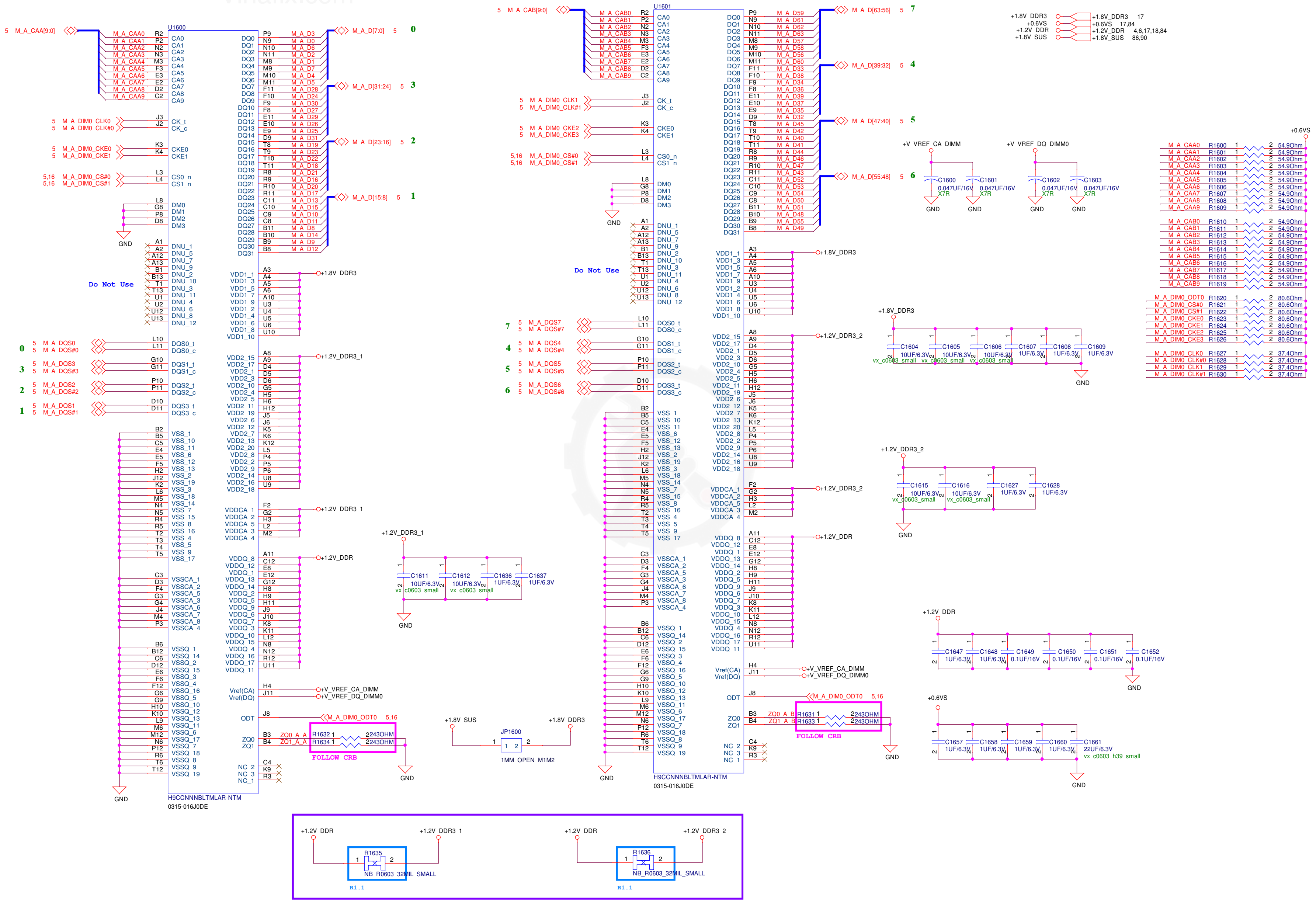

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TITLE	LPDDR3(1)_MEMORY DOWN CHA
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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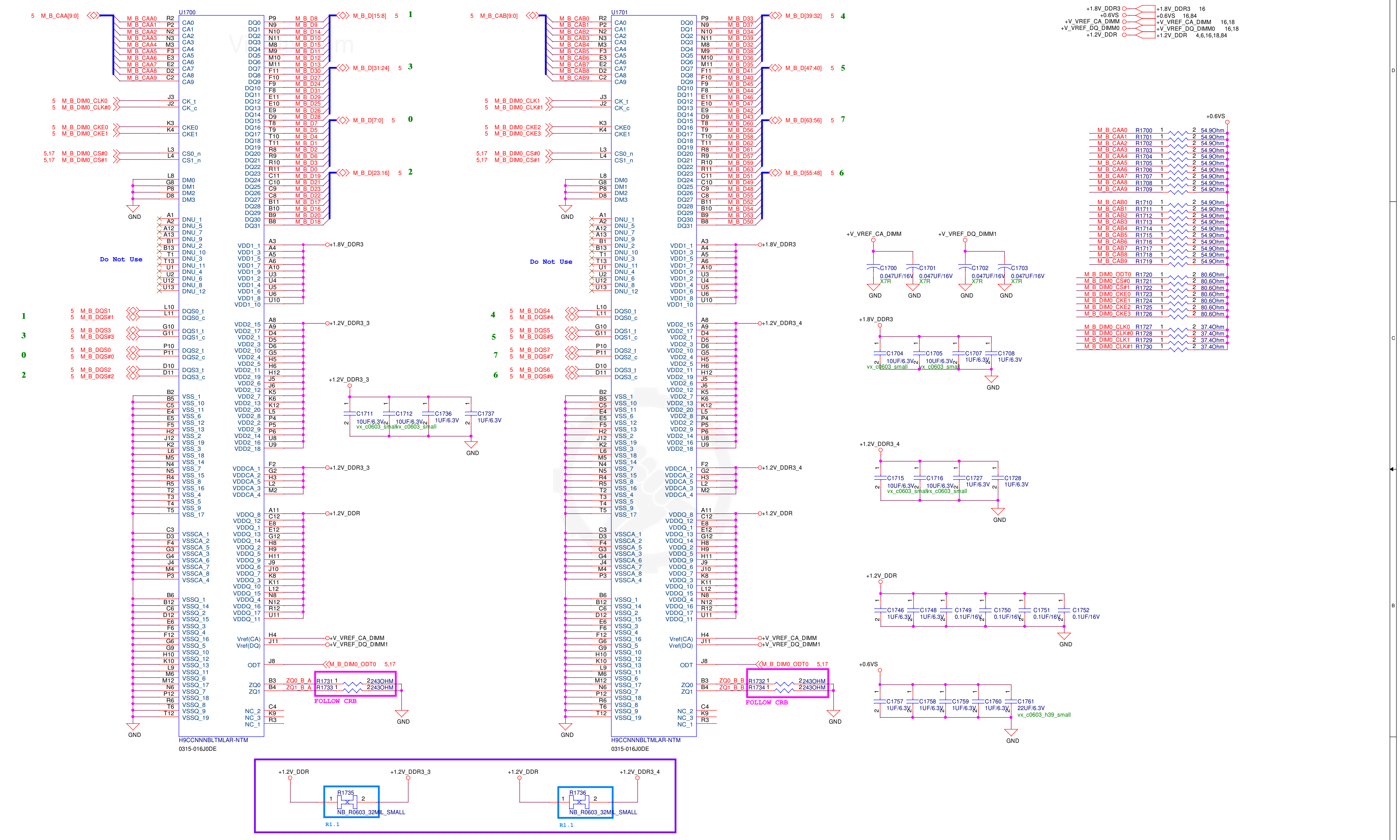

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TITLE	LPDDR3(2)_MEMORY DOWN CHB
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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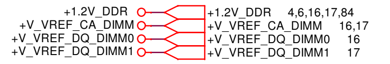
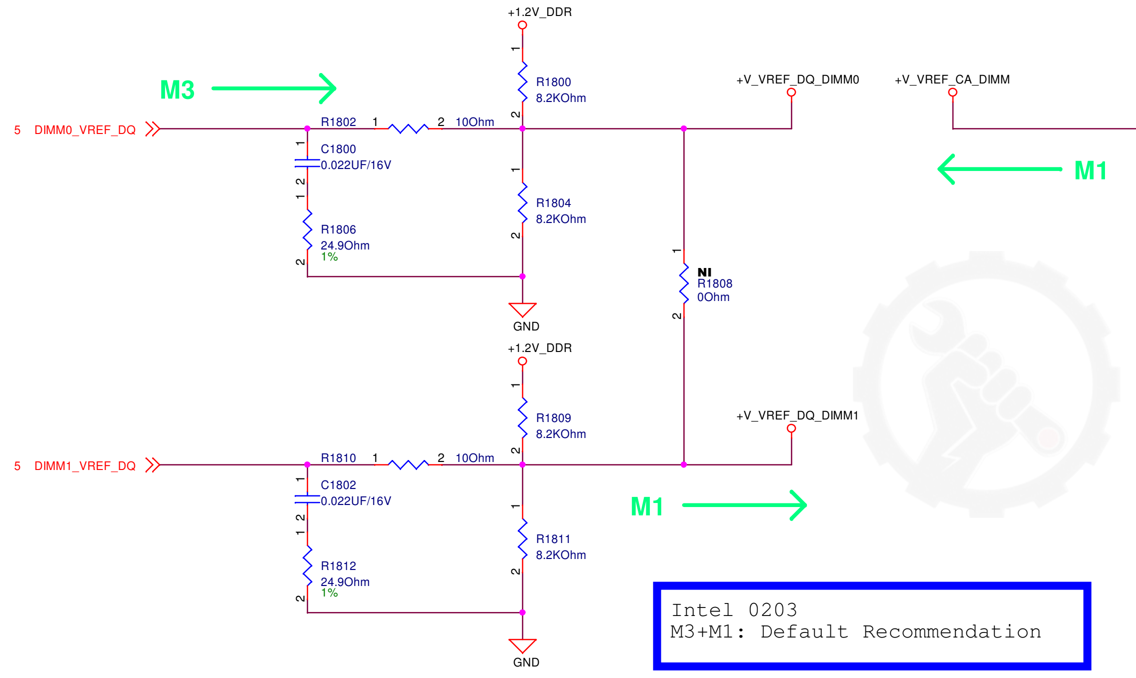


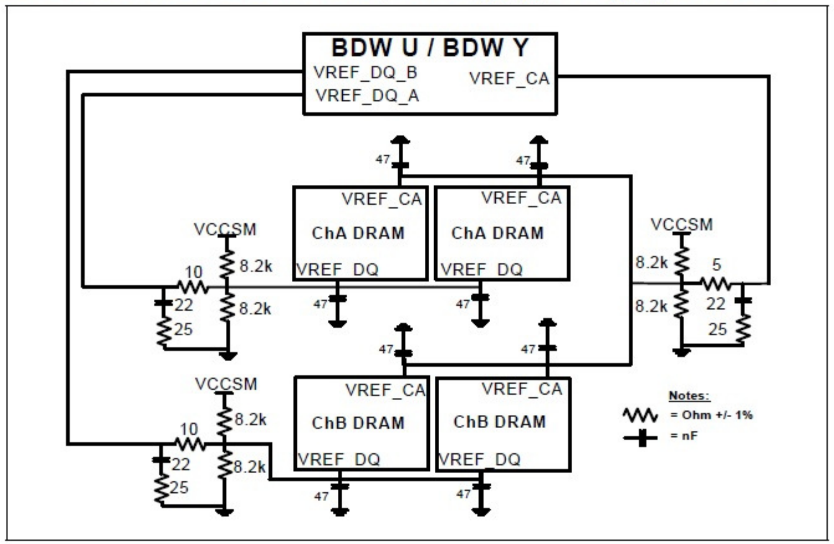
LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



Intel 0203
M3+M1: Default Recommendation

14.BDW U and BDW Y LPDDR3 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



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TITLE	LPDDR3(3)_Vref Voltage		
DWG NO.	CORE_L	REV.	2.0
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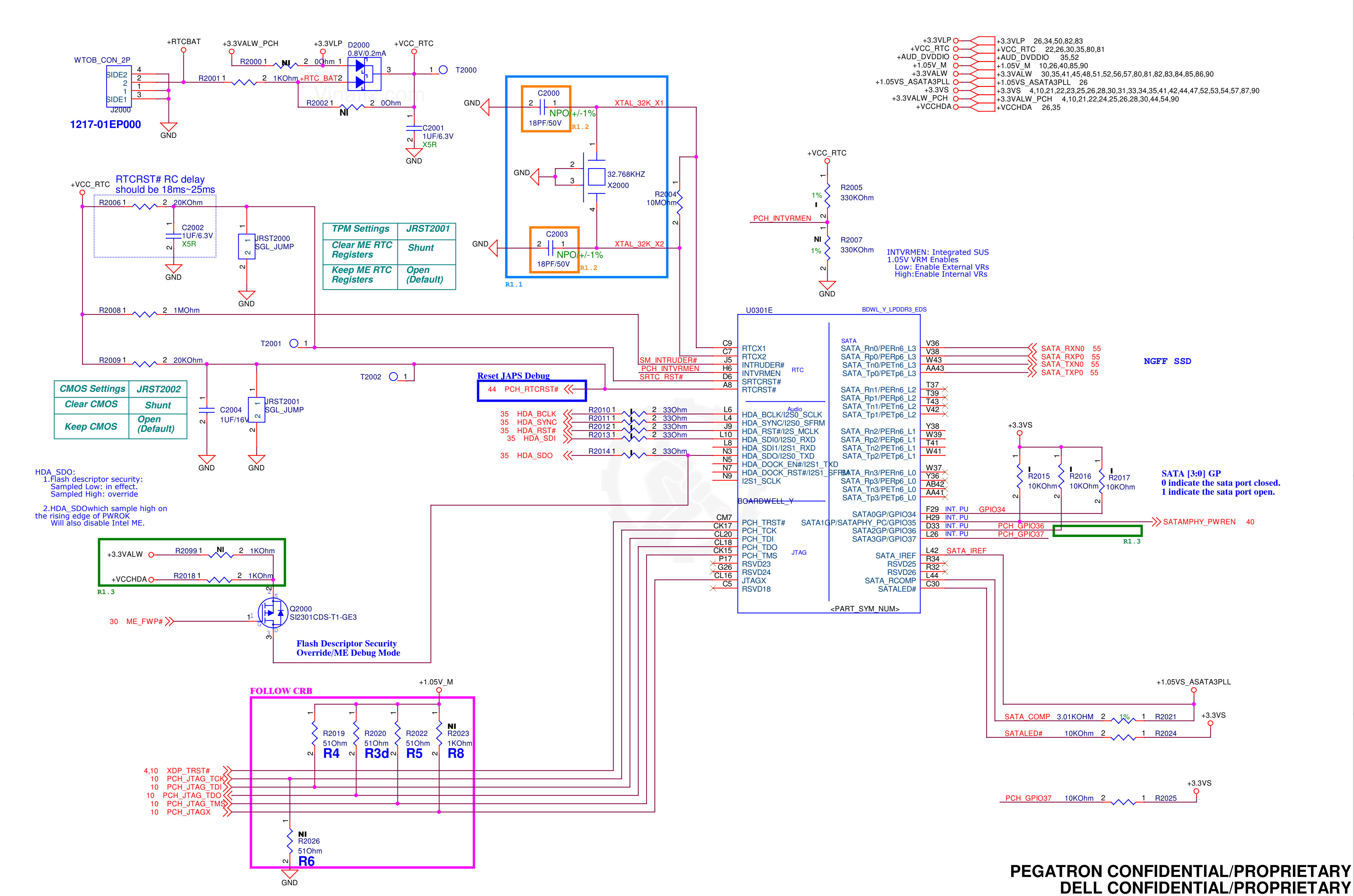

TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

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TITLE PCH(1)_SATA,HDA,RTC
DWG NO. CORE_L
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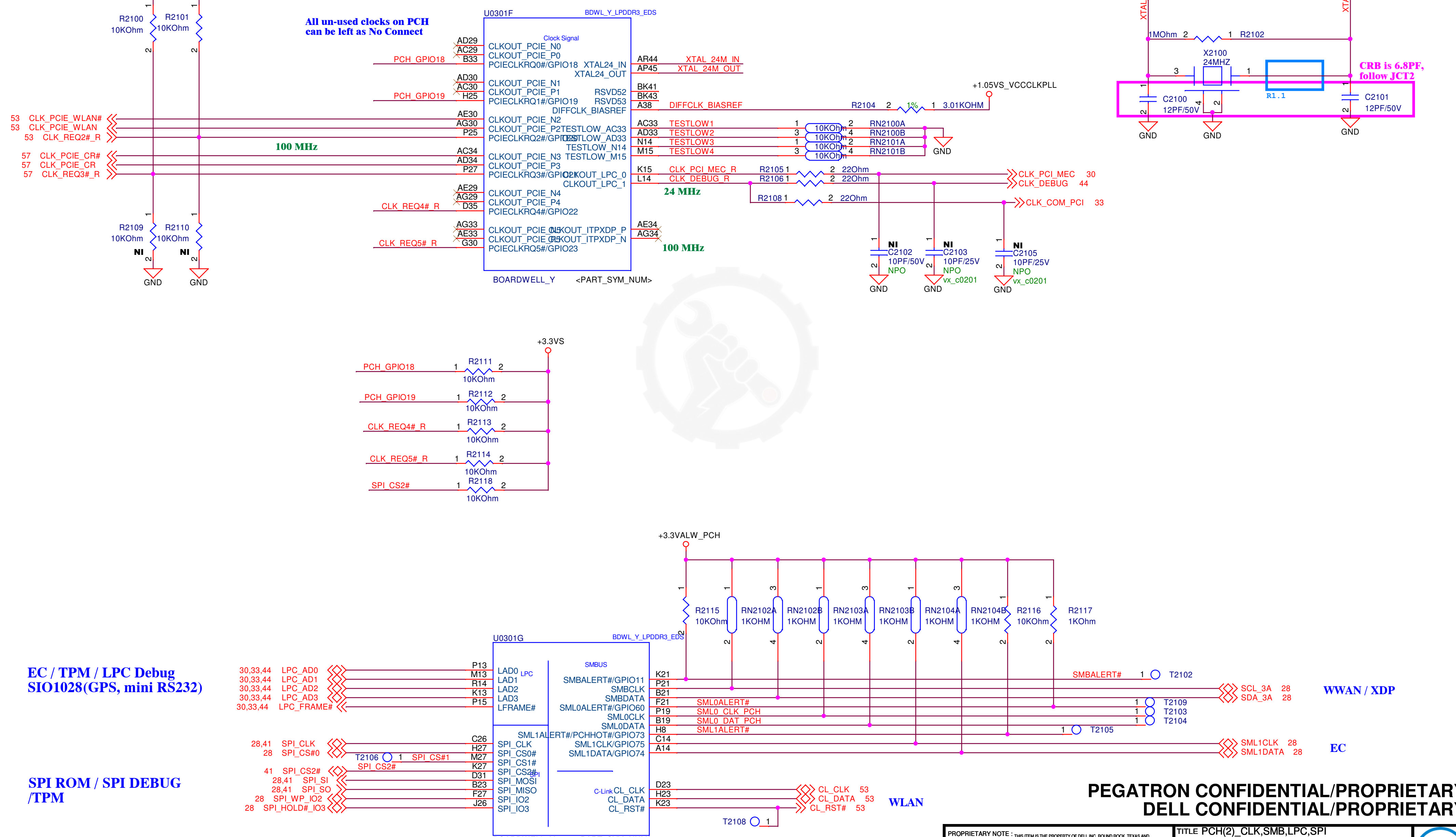
PCIE_CLK	
PCIE_CLK_0	
PCIE_CLK_1	
PCIE_CLK_2	NGFF (WLAN)
PCIE_CLK_3	Card Reader
PCIE_CLK_4	
PCIE_CLK_5	

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

PCH CLKREQ Setting:
Not connected to device.
PCIECLKRQ[5:0]# are core well powered.

All un-used clocks on PCH can be left as No Connect



EC / TPM / LPC Debug
SIO1028(GPS, mini RS232)

SPI ROM / SPI DEBUG /TPM

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TITLE	PCH(2)_CLK,SMB,LPC,SPI
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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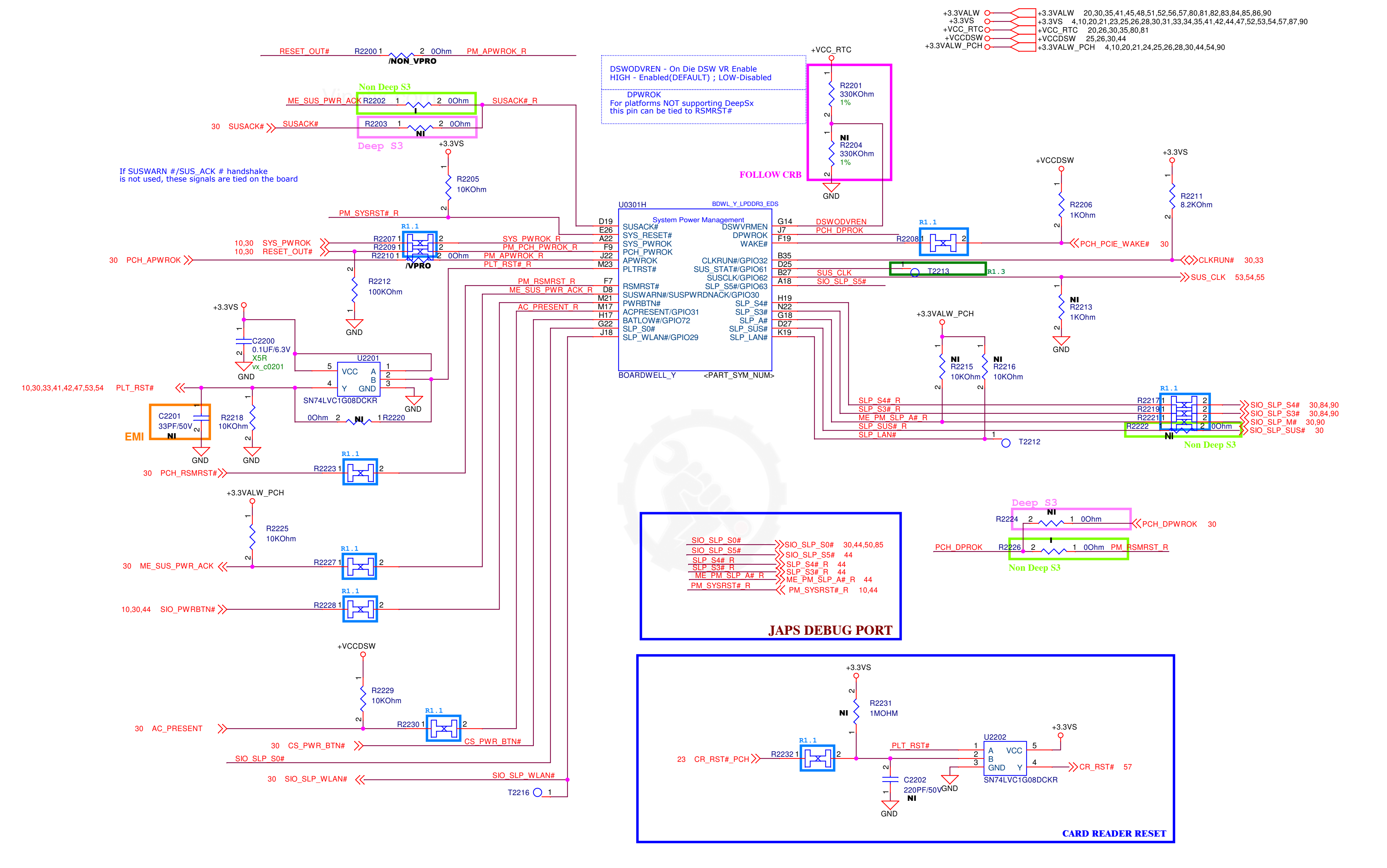

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TITLE	PCH(3)_SYS PWR		
DWG NO.	CORE_L	REV.	2.0
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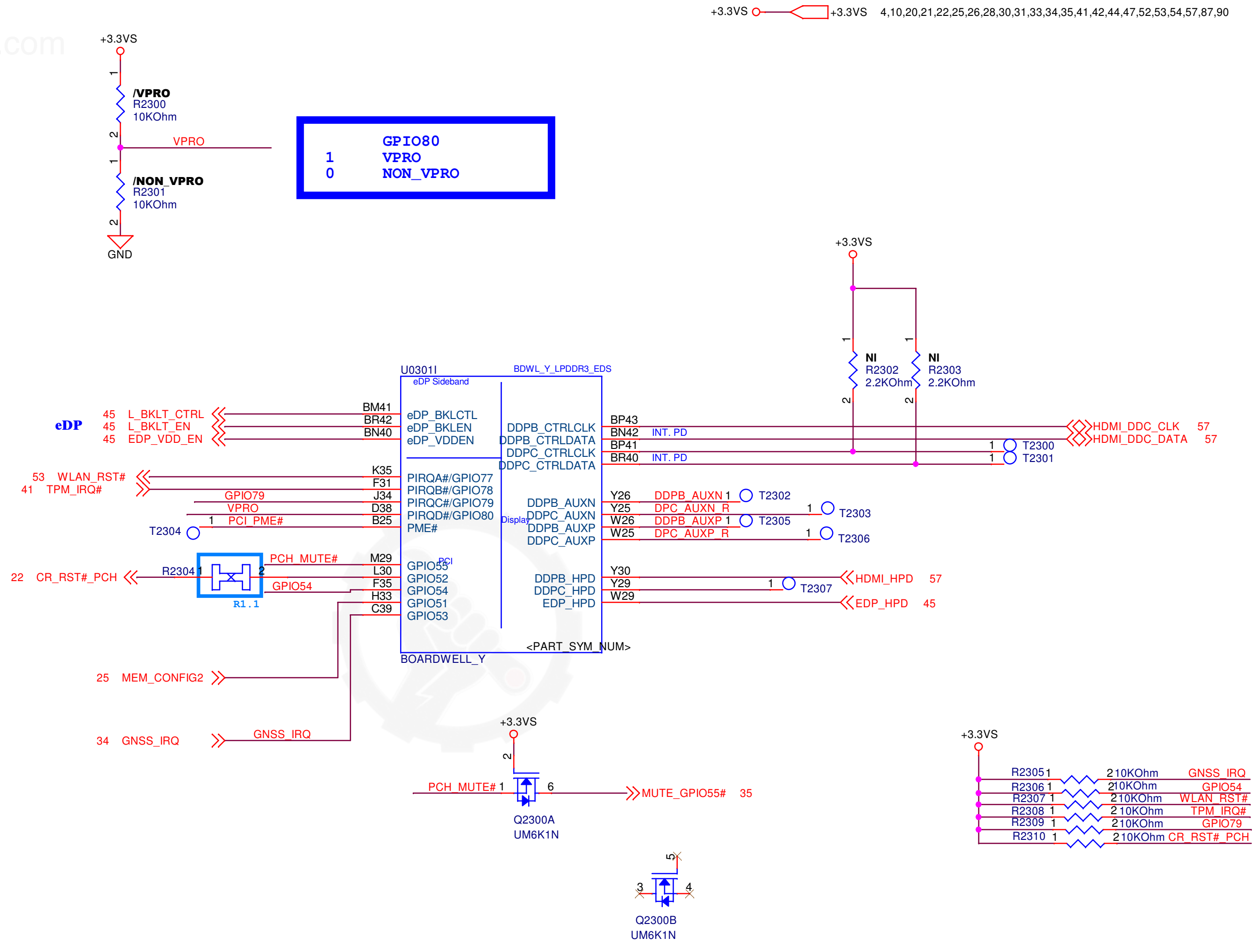
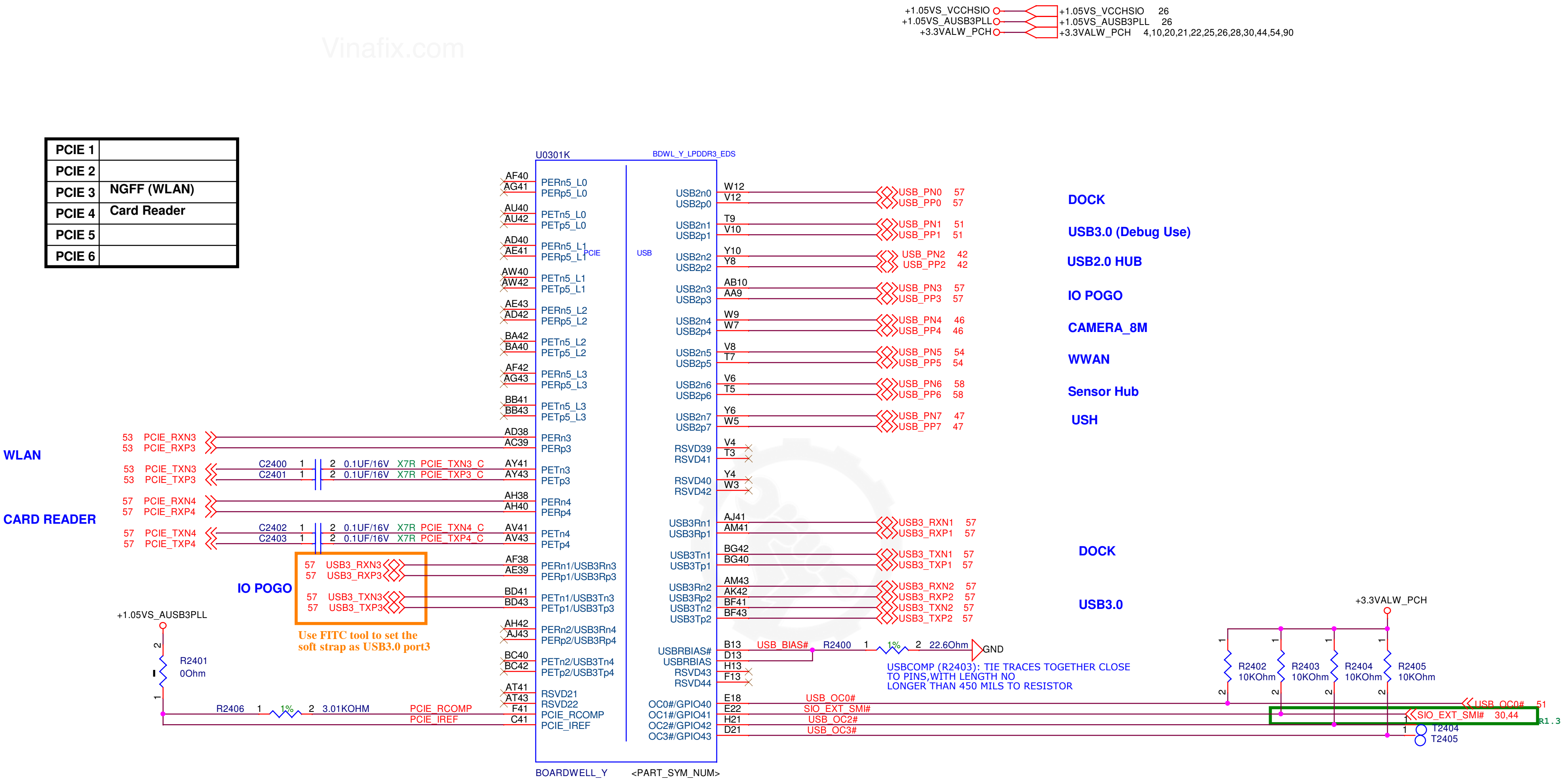


TITLE PCH(4)_DP,PIRQ

DWG NO. CORE_L REV. 2.0

DATE Wednesday, May 06, 2015 SHEET 23 of 99

PCIE 1	
PCIE 2	
PCIE 3	NGFF (WLAN)
PCIE 4	Card Reader
PCIE 5	
PCIE 6	



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TITLE	PCH(5)_PCIE,USB
DWG NO.	CORE_L
REV.	2.0
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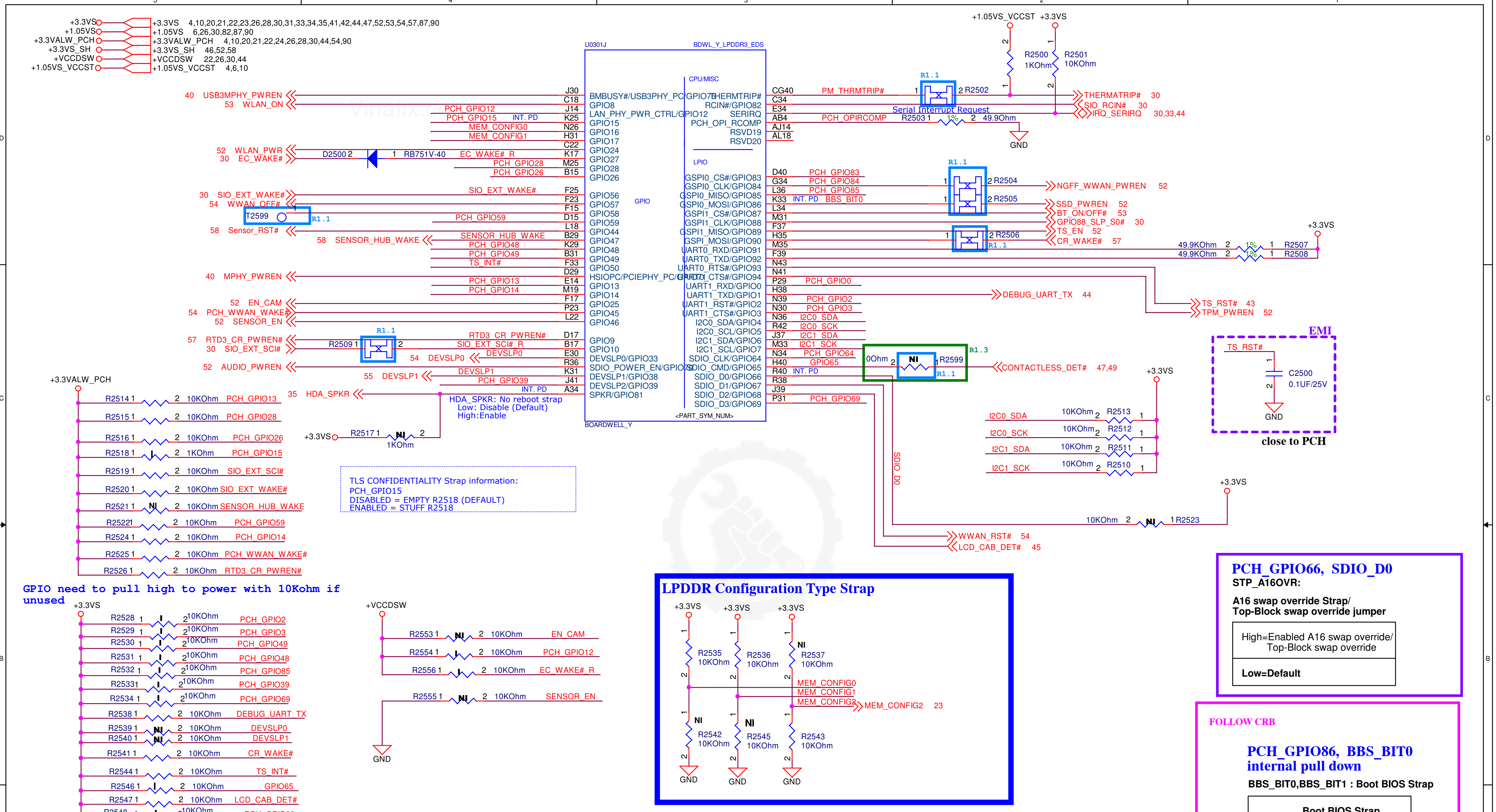

GPIO Pin	Pin Name	Micron EDF8132A3MA-JD -F-R (8Gb)	Micron EDFA232A2MA-JD-F-R (16 Gb)	SK HYNIX/H9CCNNN 8GTMLAR-NTD(8Gb)	SK HYNIX/H9CCNNN BJTMLAR-NTD (16 Gb)	SAMSUNG/K4E8E 304EE-EGCE (8Gb)	SAMSUNG/K4E6E 304EE-EGCE (16 Gb)
PCH_GPIO16	MEM_CONFIG0	0	1	0	1	0	1
PCH_GPIO17	MEM_CONFIG1	0	0	1	1	0	0
PCH_GPIO51	MEM_CONFIG2	0	0	0	0	1	1

PCH_GPIO66, SDIO_D0

STP_A16OVR:

A16 swap override Strap/ Top-Block swap override jumper

High=Enabled A16 swap override/ Top-Block swap override
Low=Default

FOLLOW CRB

PCH_GPIO86, BBS_BIT0 internal pull down

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC
0	SPI **(PCH)**

Sampled on rising edge of PWROK.

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TITLE	PCH(6)_I2C,GPIO,UART,SDIO
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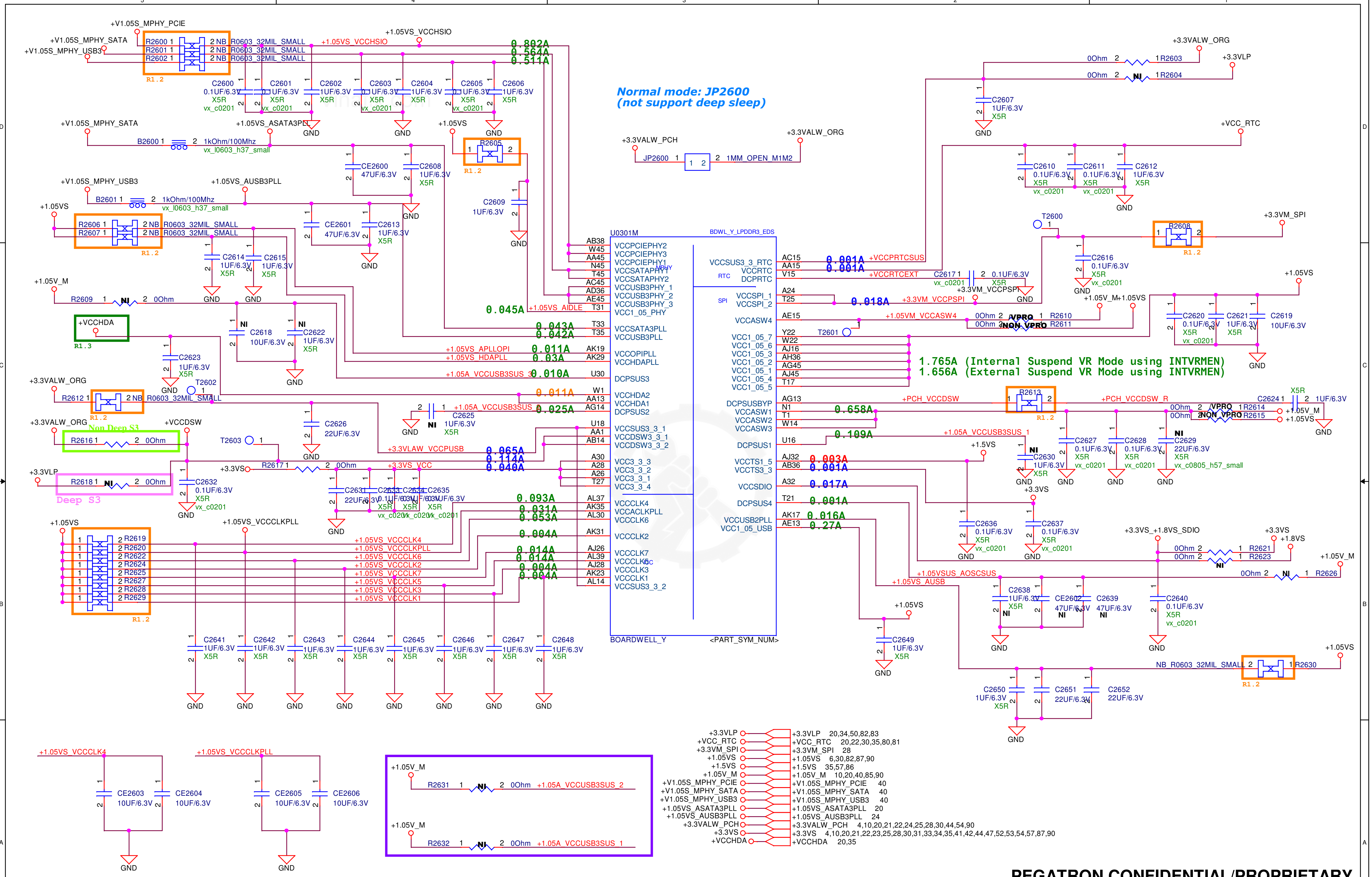

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TITLE	PCH(7)_POWER
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TITLE	PCH(8)_***		
DWG NO.	CORE_L	REV.	2.0
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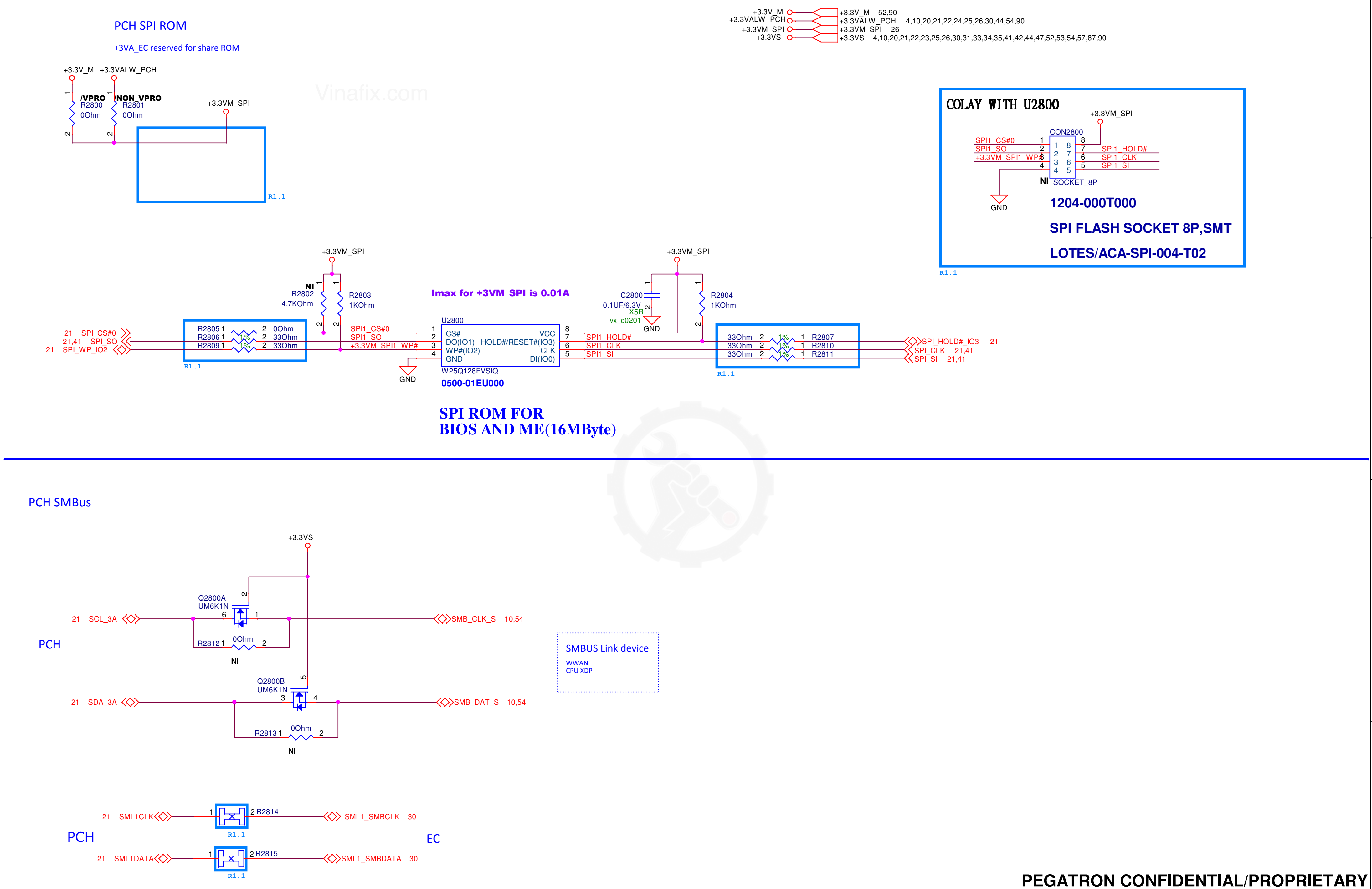

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TITLE	PCH(9)_SPI ROM,SMB
DWG NO.	CORE_L
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TITLE *****			
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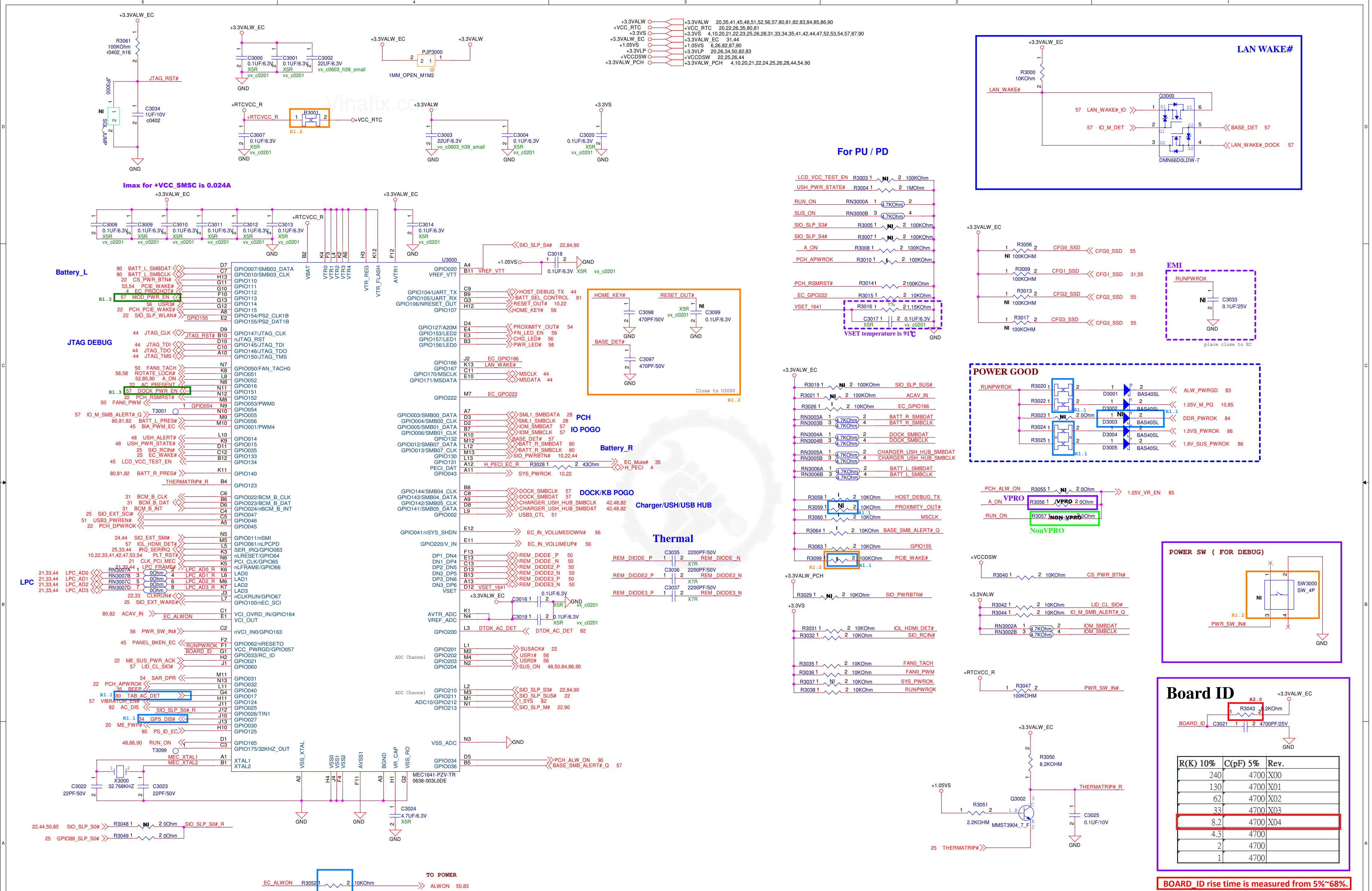

Board ID

R(K) 10%	C(pF) 5%	Rev.
240	4700	X00
130	4700	X01
62	4700	X02
33	4700	X03
8.2	4700	X04
4.3	4700	
2	4700	
1	4700	

BOARD_ID rise time is measured from 5%~68%.

TITLE	EC_MEC1641
DWG NO.	CORE_L
REV.	2.0
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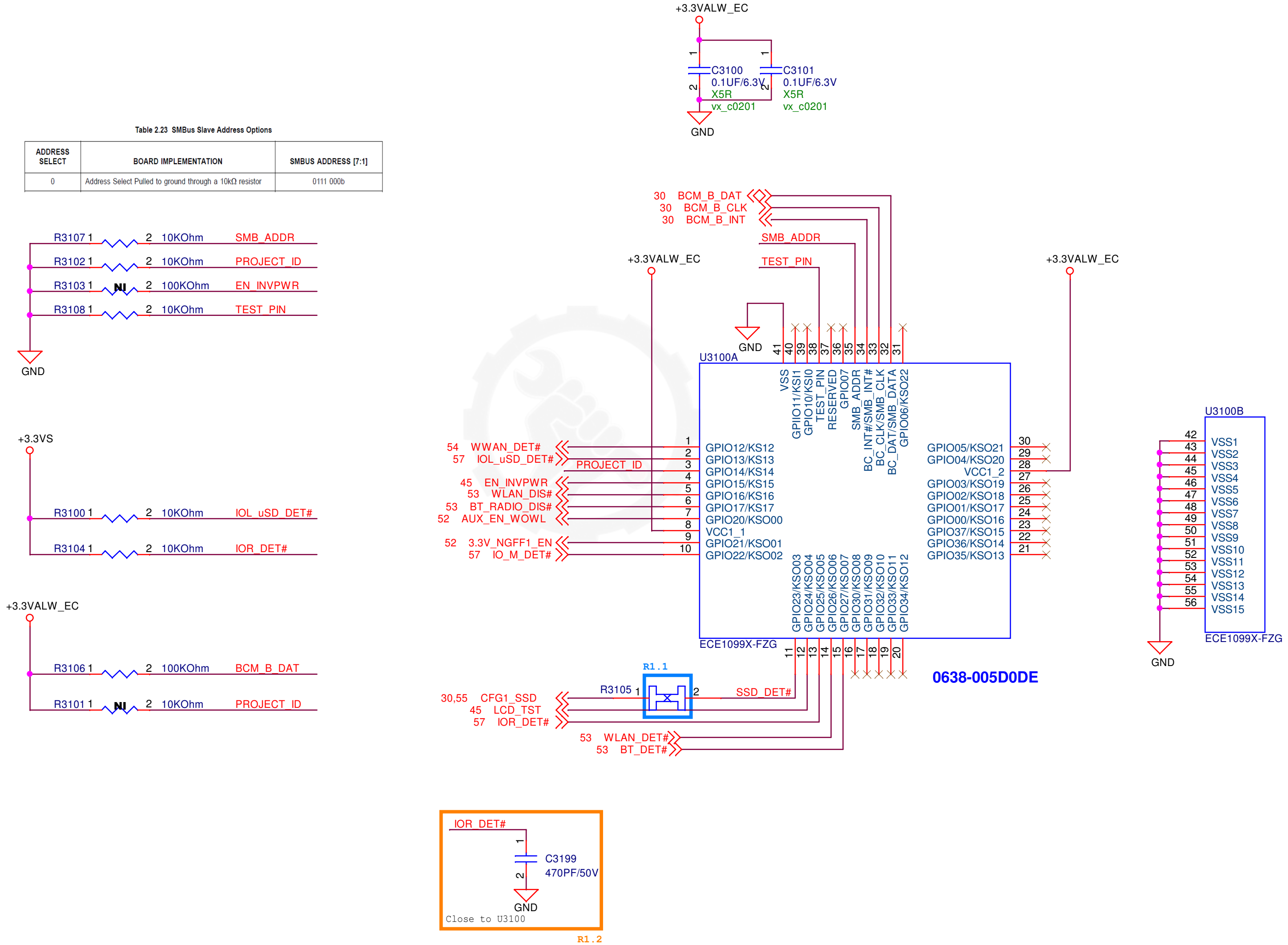
Table 2.23 SMBus Slave Address Options

ADDRESS SELECT	BOARD IMPLEMENTATION	SMBUS ADDRESS [7:1]
0	Address Select Pulled to ground through a 10kΩ resistor	0111 000b



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TITLE	EC_ECE1099
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5 4 3 2 1

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TITLE ***			
DWG NO.	CORE_L	REV.	2.0
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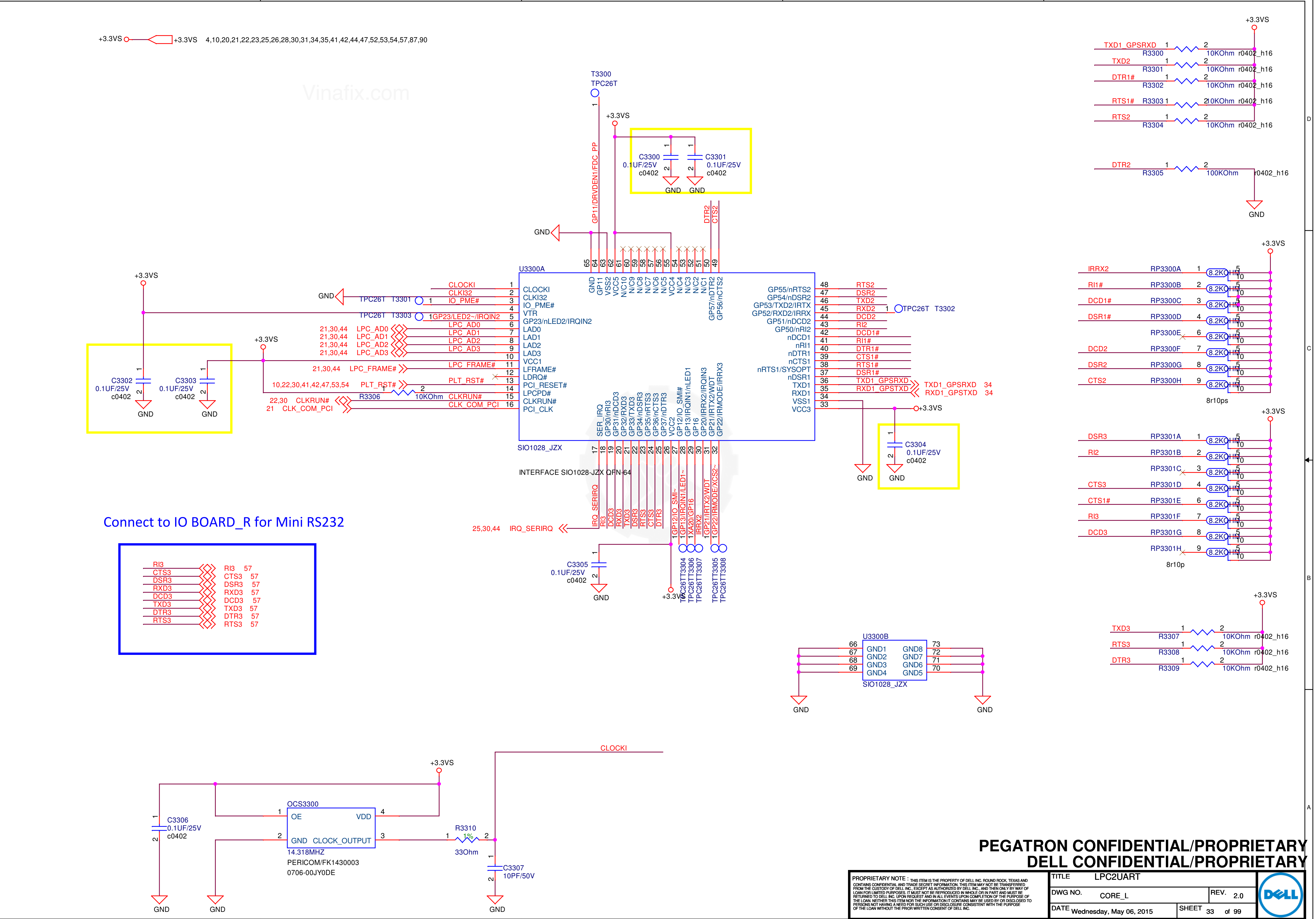

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TITLE	LPC2UART
DWG NO.	CORE_L
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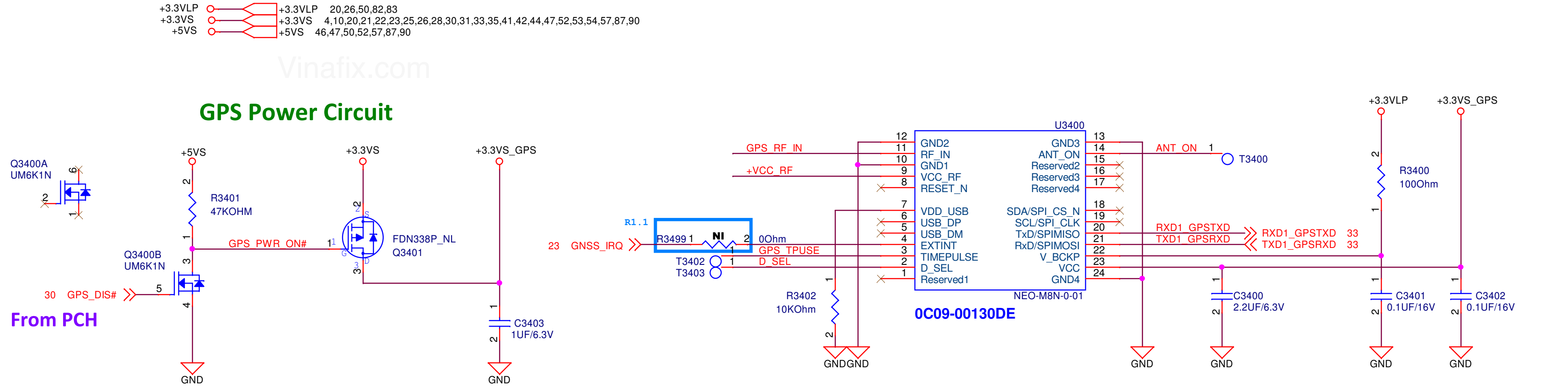
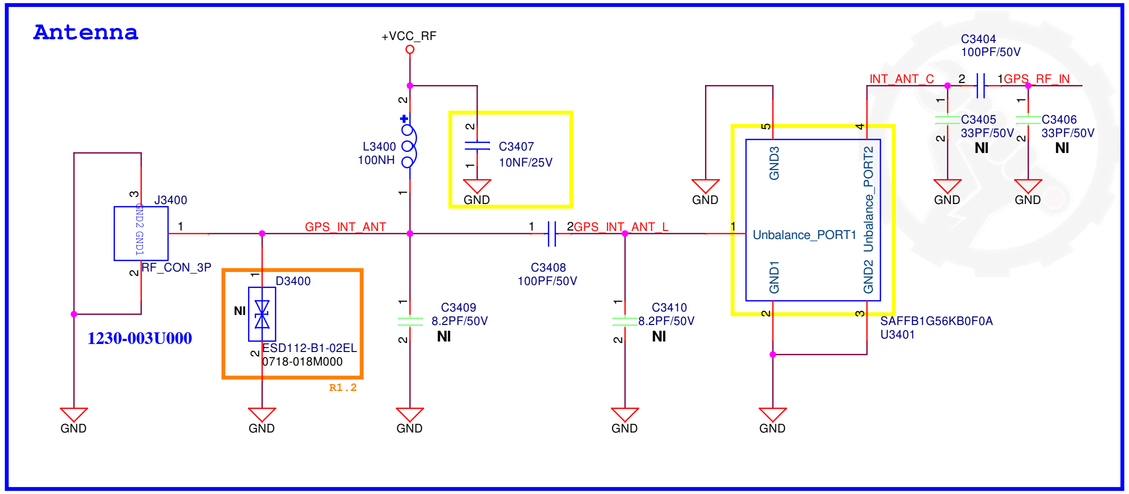
GPS Power Circuit



Antenna



PIN #	D_SEL="1" (left open)	D_SEL ="0" (connected to GND)
6	UART TX	SPI MISO
7	UART RX	SPI MOSI
8	DDC SCL	SPI CLK
9	DDC SDA	SPI CS_N

Table 6: Data interface selection by D_SEL

owed ripple on VCC=50 mVpp

a good GND connection to all GND pins of the module, ply with a large ground plane.

mmended to connect a backup battery to V_BCKP in order le Warm and Hot Start features on the receivers. Otherwise connect to GND.

VDDUSB	7	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6 V. If no USB serial port used connect to GND.

TITLE GPS			
DWG NO. CORE_L		REV. 2.0	
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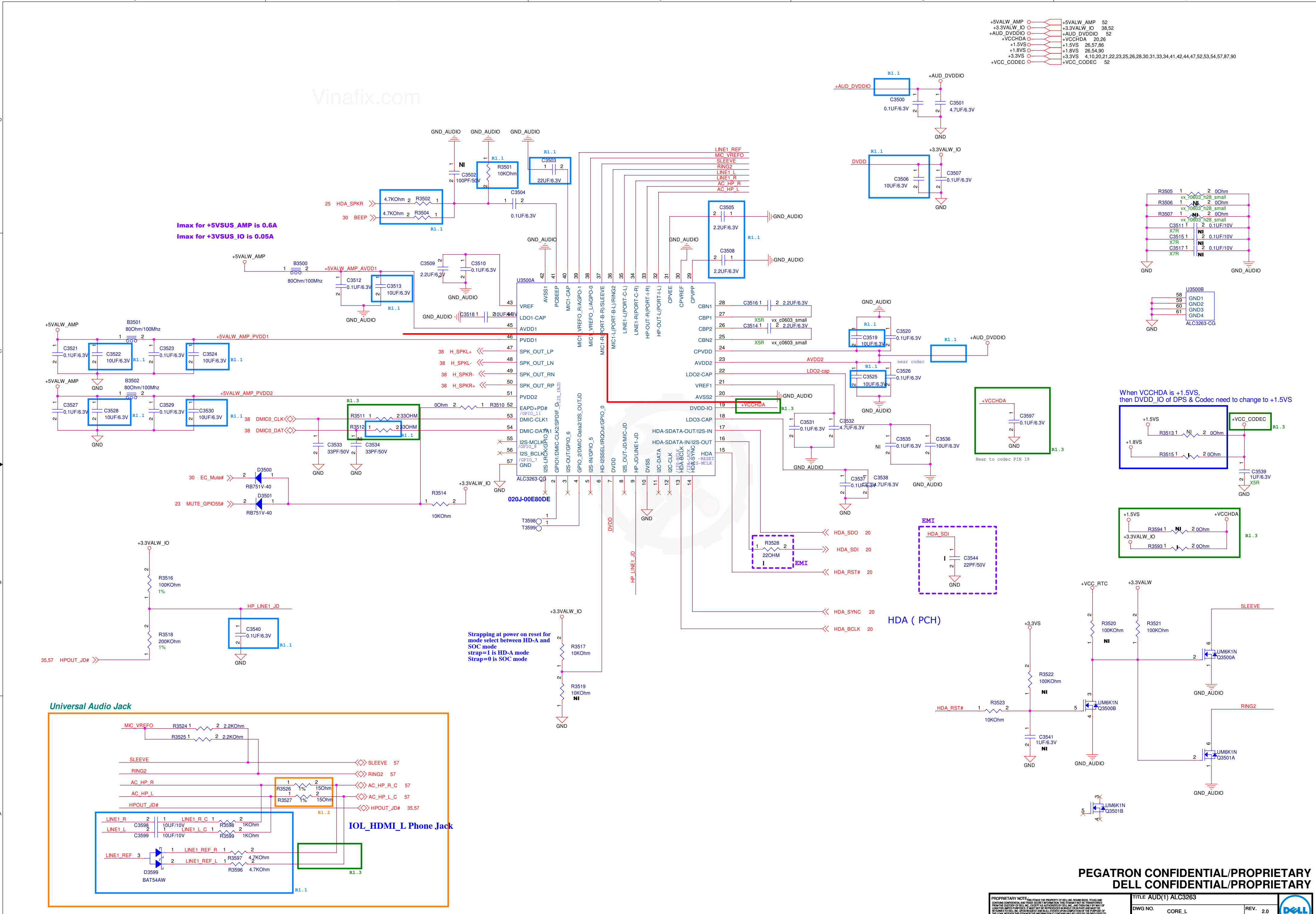

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TITLE AUD(1) ALC3263		
DWG NO. CORE_L		REV. 2.0
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TITLE	AUD(2) ***		
DWG NO.	CORE_L	REV.	2.0
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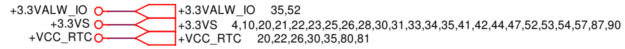
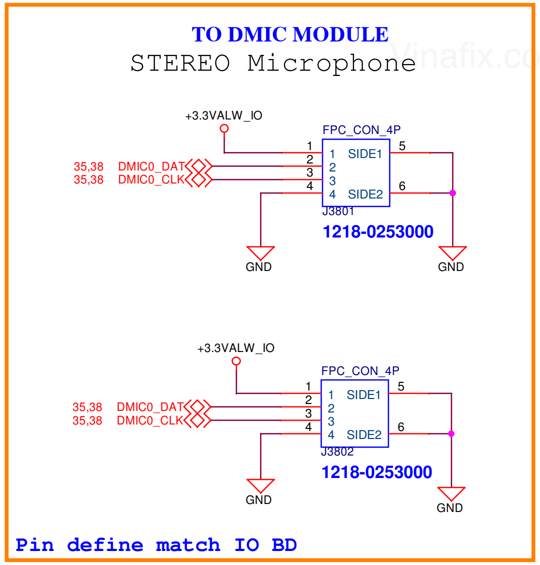
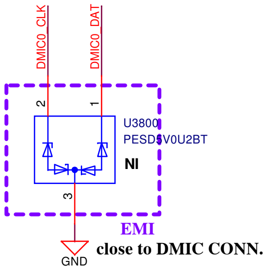
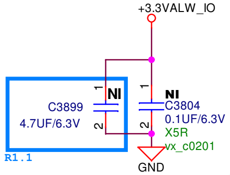


Internal DMIC Conn.







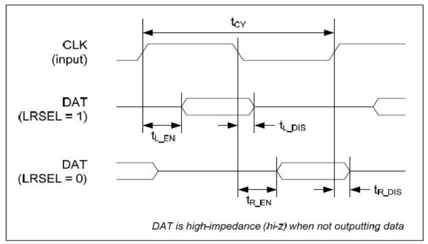
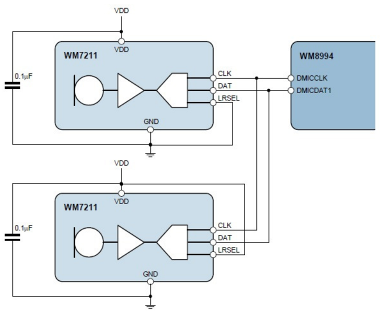
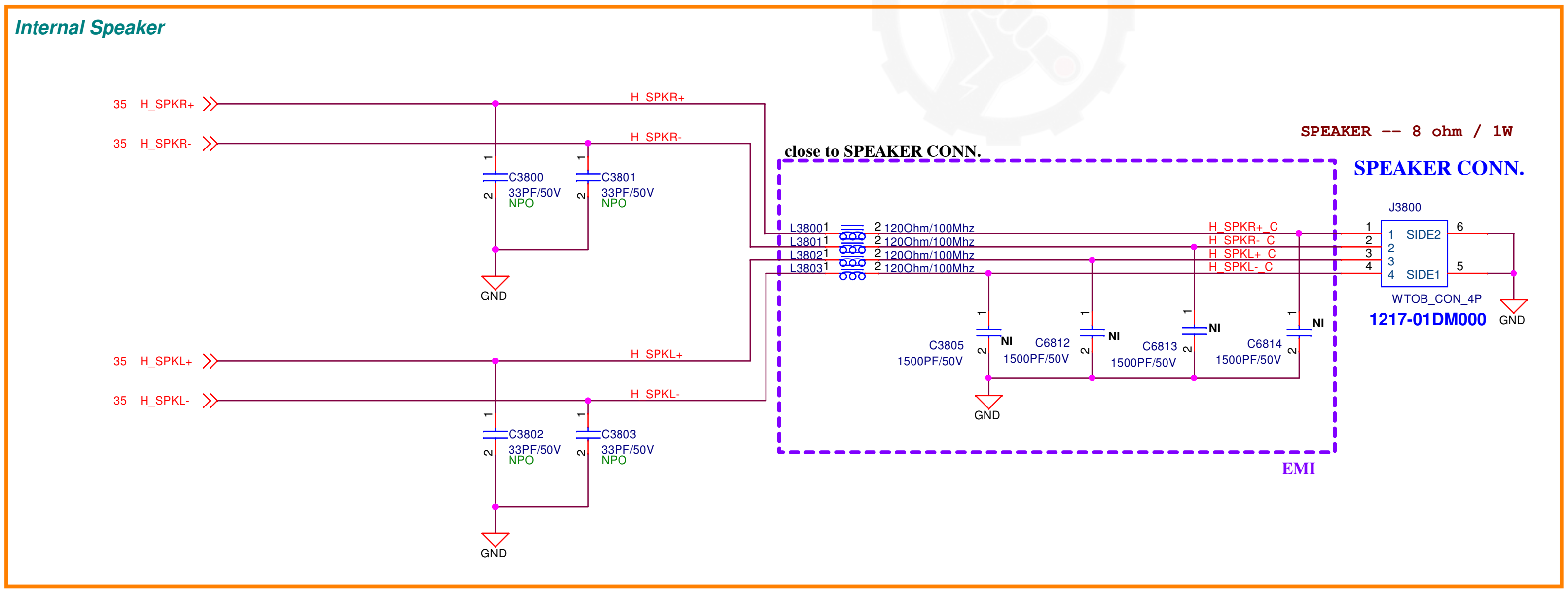


Figure 1 Digital Microphone Interface Timing



Internal Speaker



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TITLE	AUD(3)_DMIC / SPEAKER
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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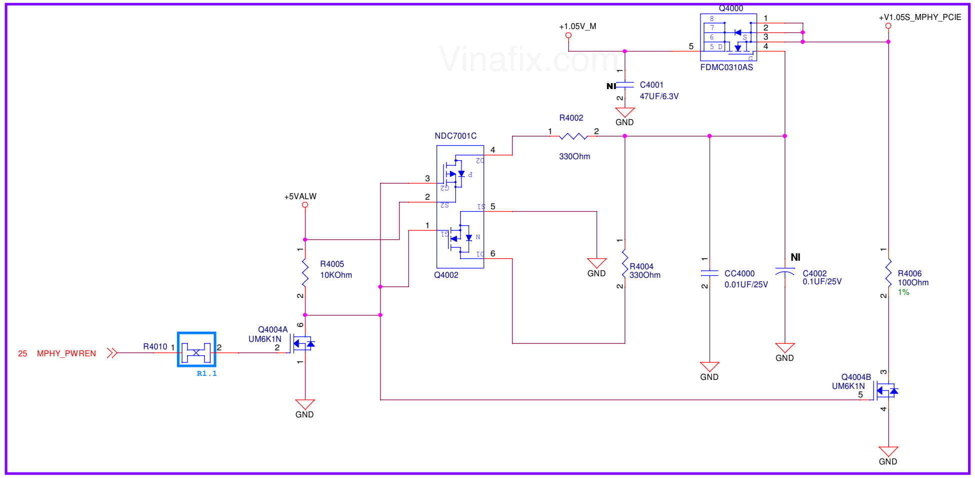
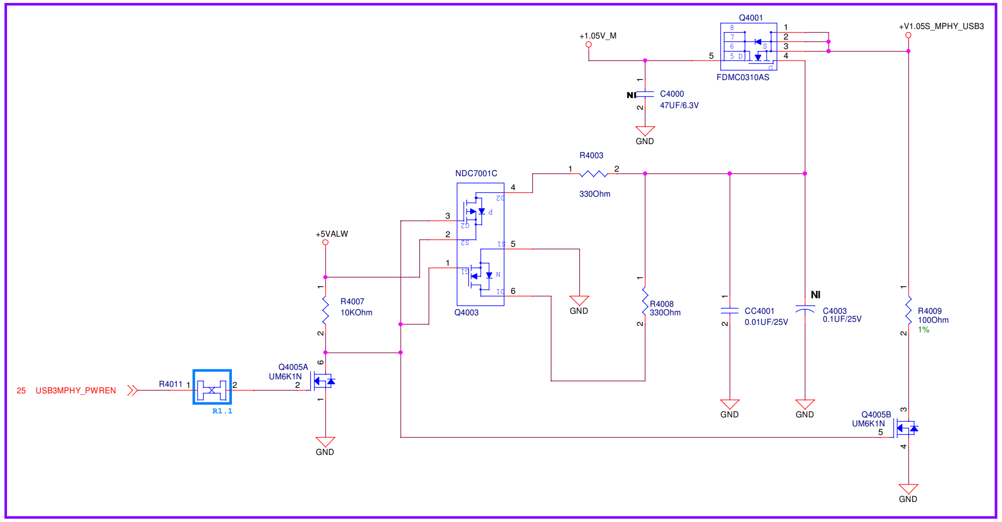
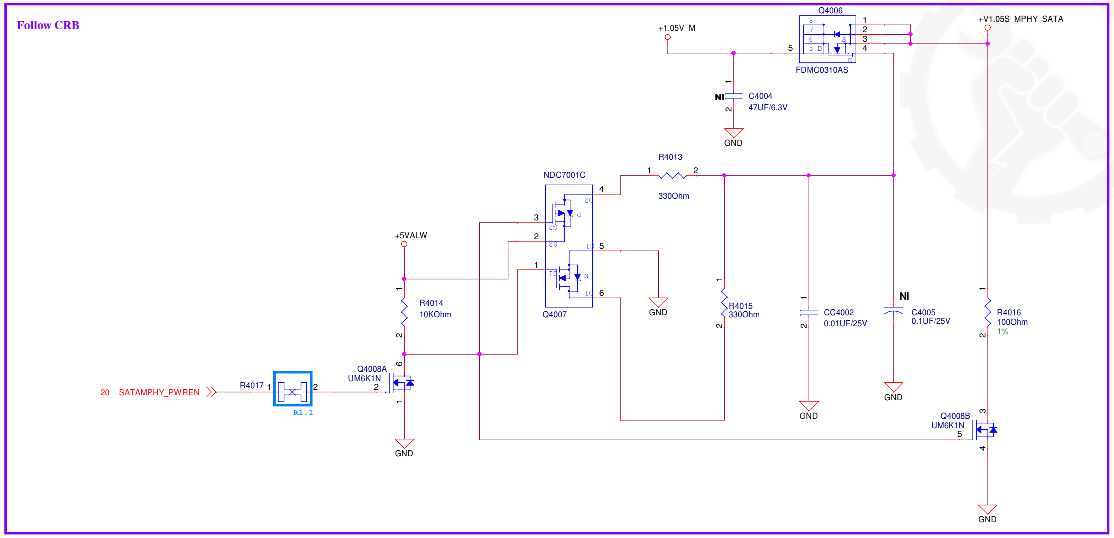
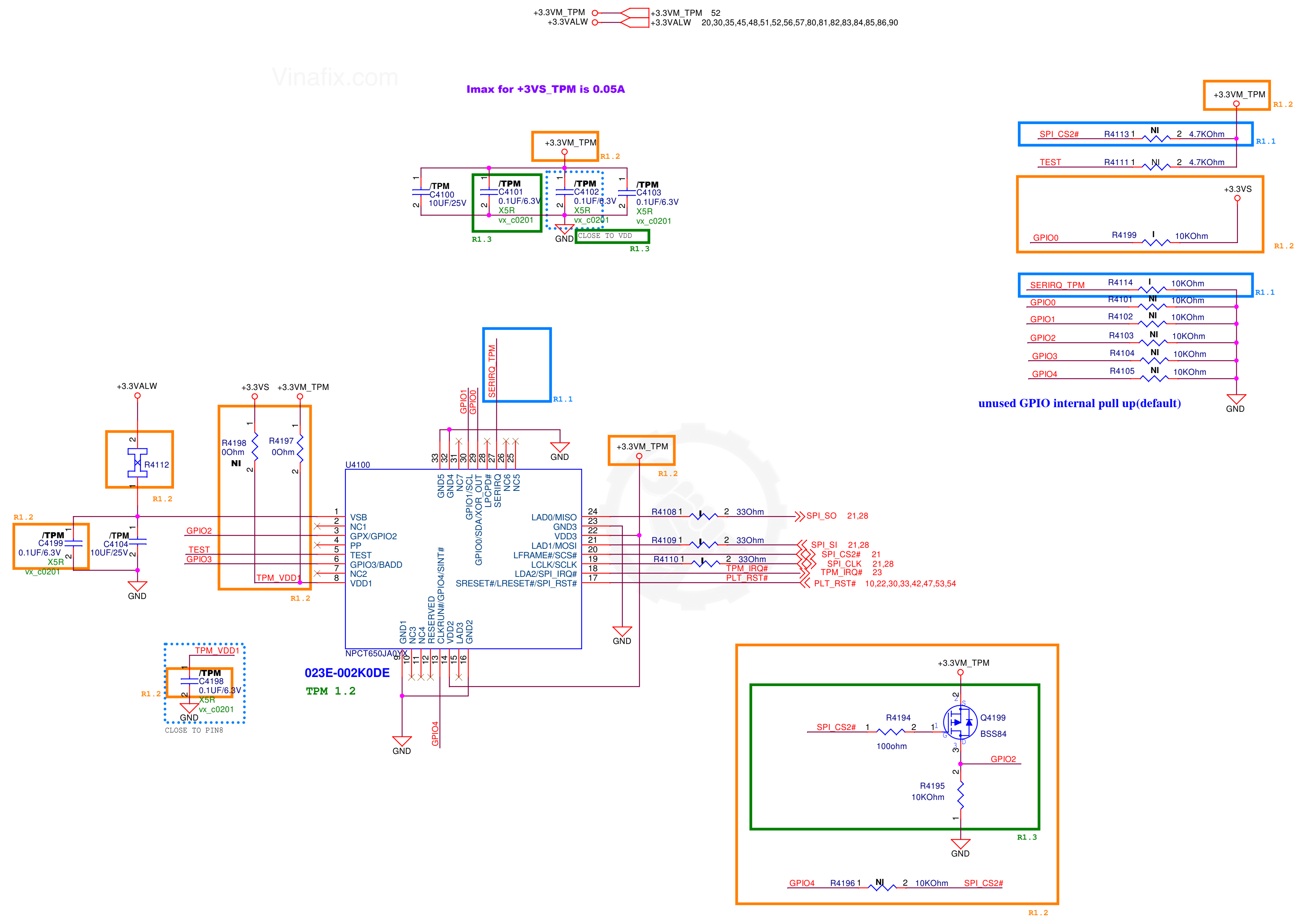






+5VALW — +5VALW 46,48,50,51,52,56,57,80,83,84,87,90
+V1.05S_MPHY_PCIE — +V1.05S_MPHY_PCIE 26
+V1.05S_MPHY_SATA — +V1.05S_MPHY_SATA 26
+V1.05S_MPHY_USB3 — +V1.05S_MPHY_USB3 26
+1.05V_M — +1.05V_M 10,20,26,85,90

TITLE PHY POWER SW		
DWG NO. CORE_L		REV. 2.0
DATE Wednesday, May 06, 2015	SHEET 40	of 99



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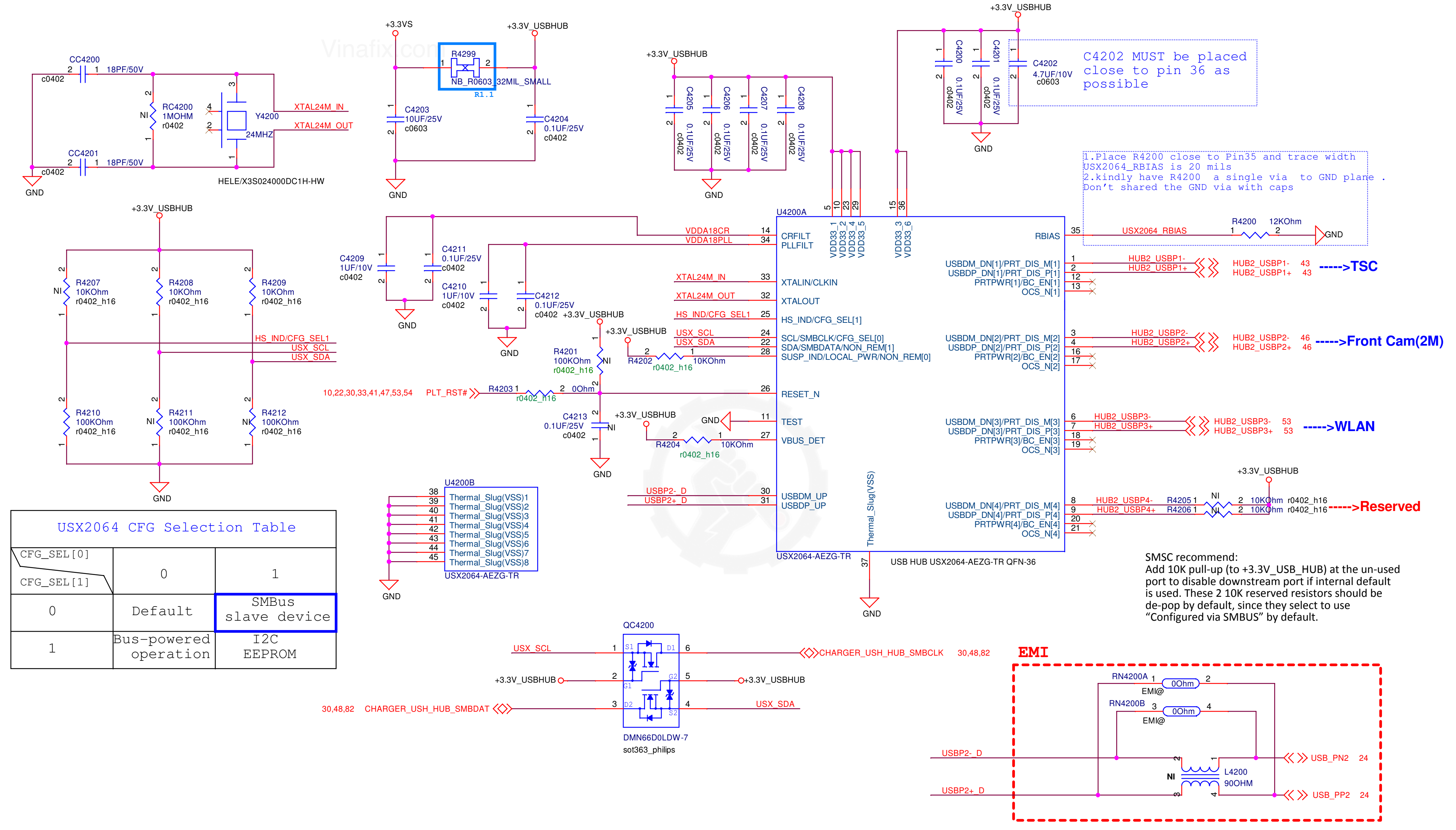
TITLE	TPM_NPCT650		
DWG NO.	CORE_L	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	41 of 99



USX2064 CFG Selection Table

CFG_SEL[0] / CFG_SEL[1]	0	1
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM

SMSC recommend:
Add 10K pull-up (to +3.3V_USB_HUB) at the un-used port to disable downstream port if internal default is used. These 2 10K reserved resistors should be de-pop by default, since they select to use "Configured via SMBUS" by default.

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TITLE	USB2.0 HUB
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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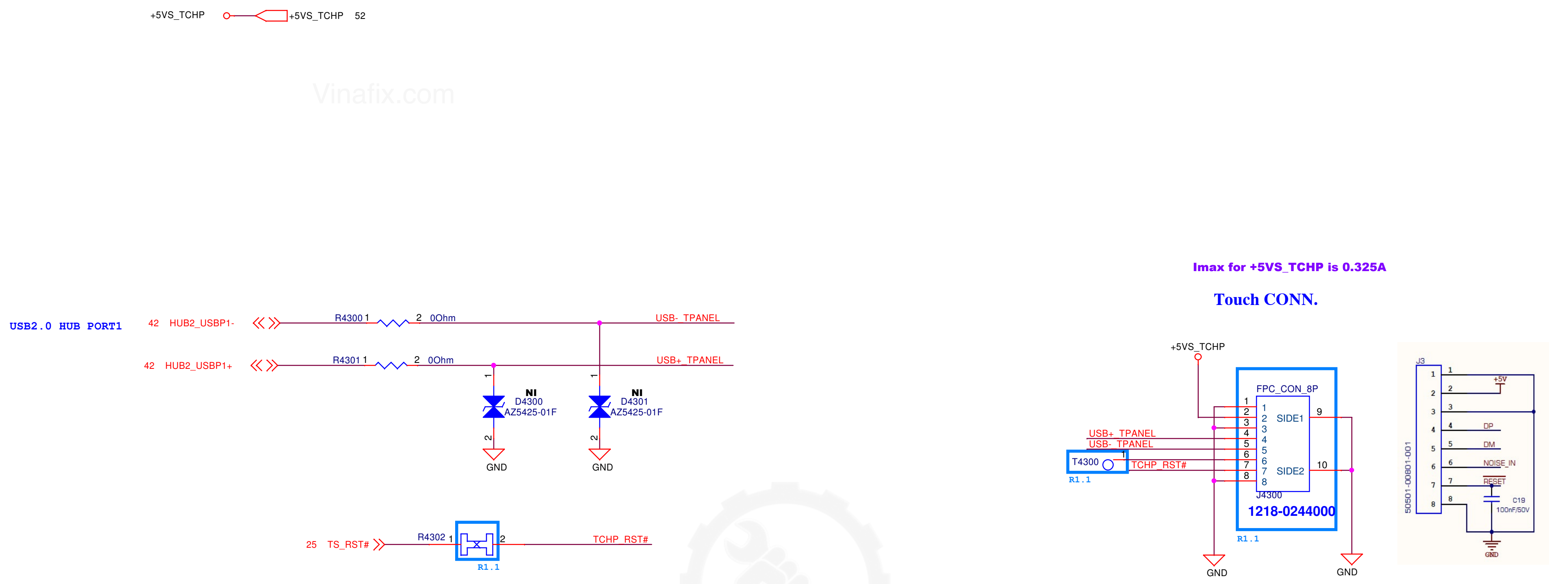

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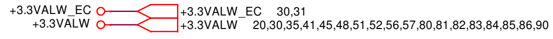
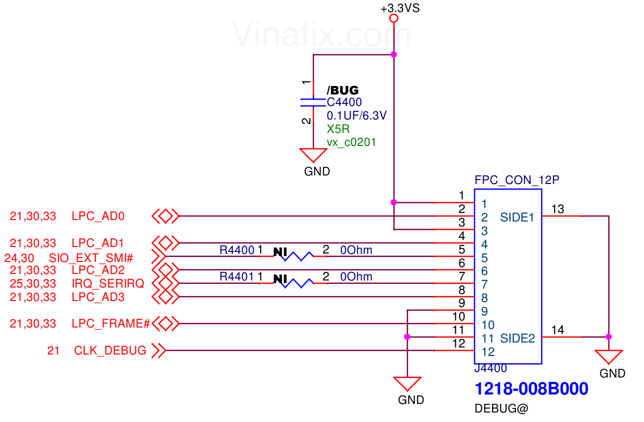
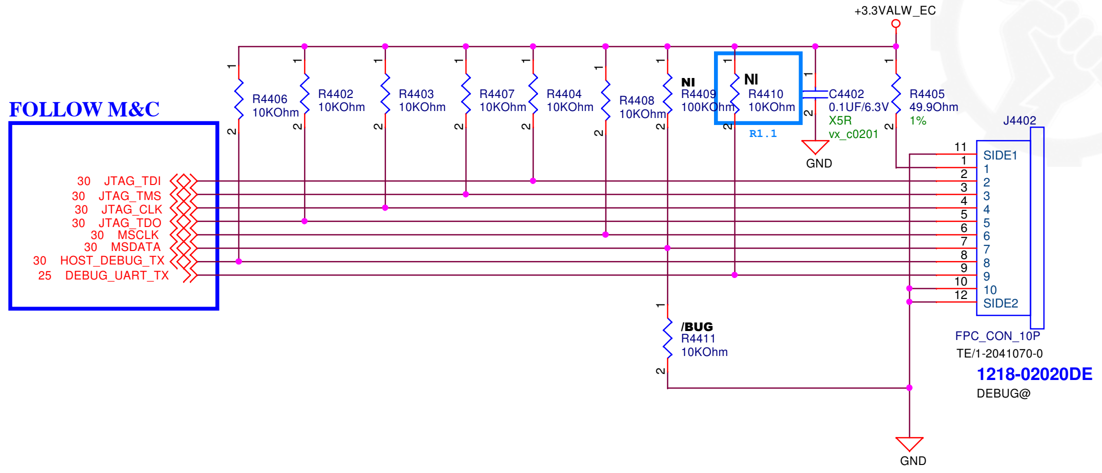
TITLE	Touch Screen
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
SHEET	43 of 99



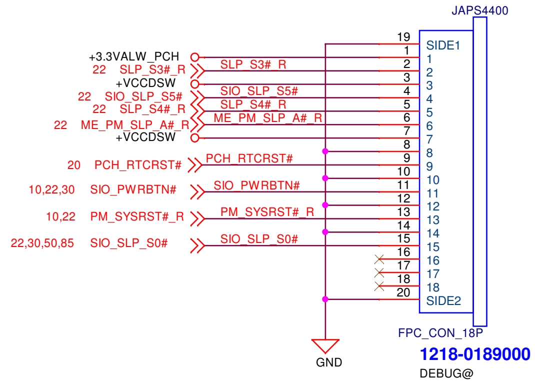
LPC Debug Port



JTAG Debug Port



JAPS Debug Port



R1.1

TITLE	Debug CONN
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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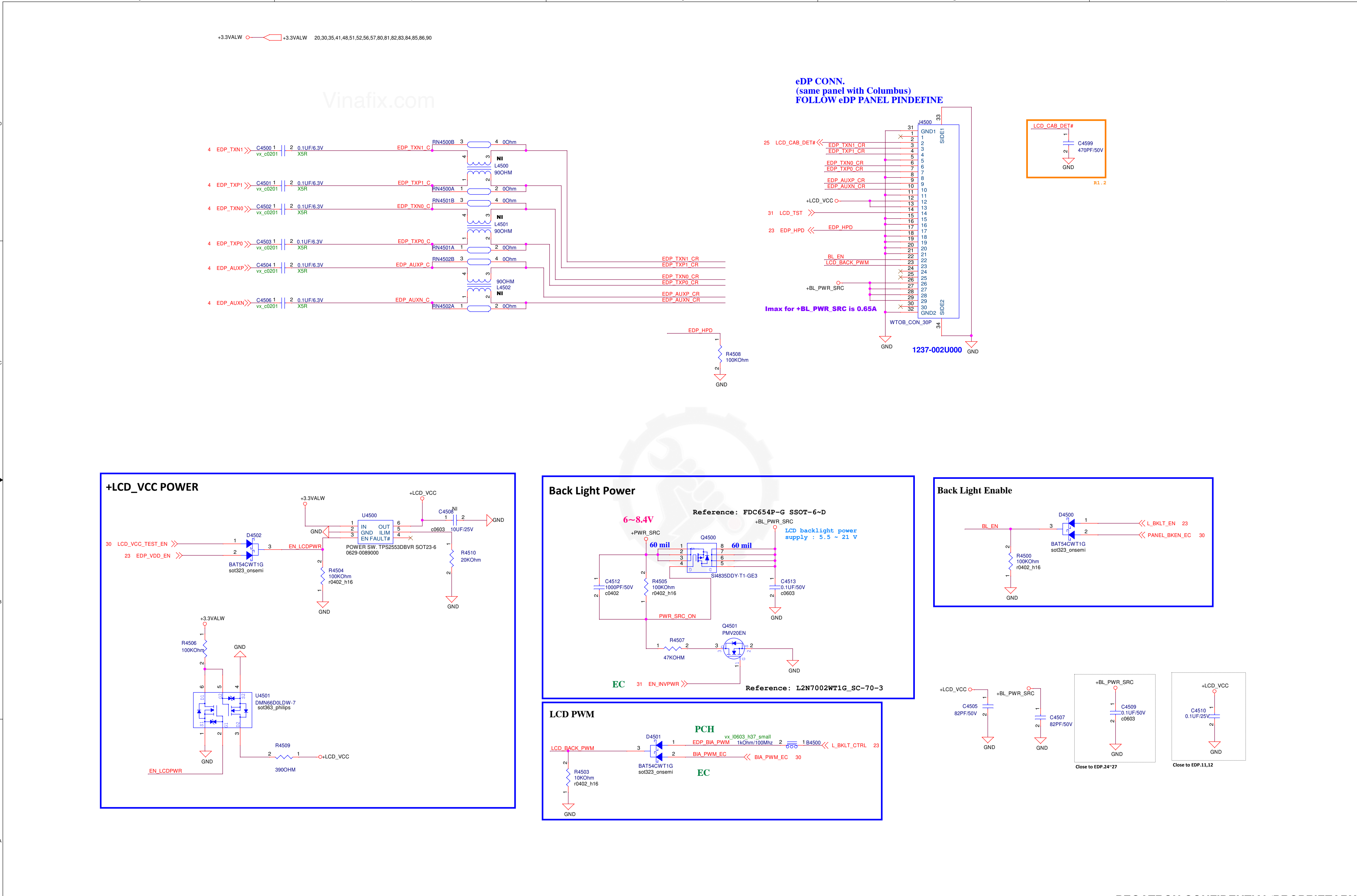

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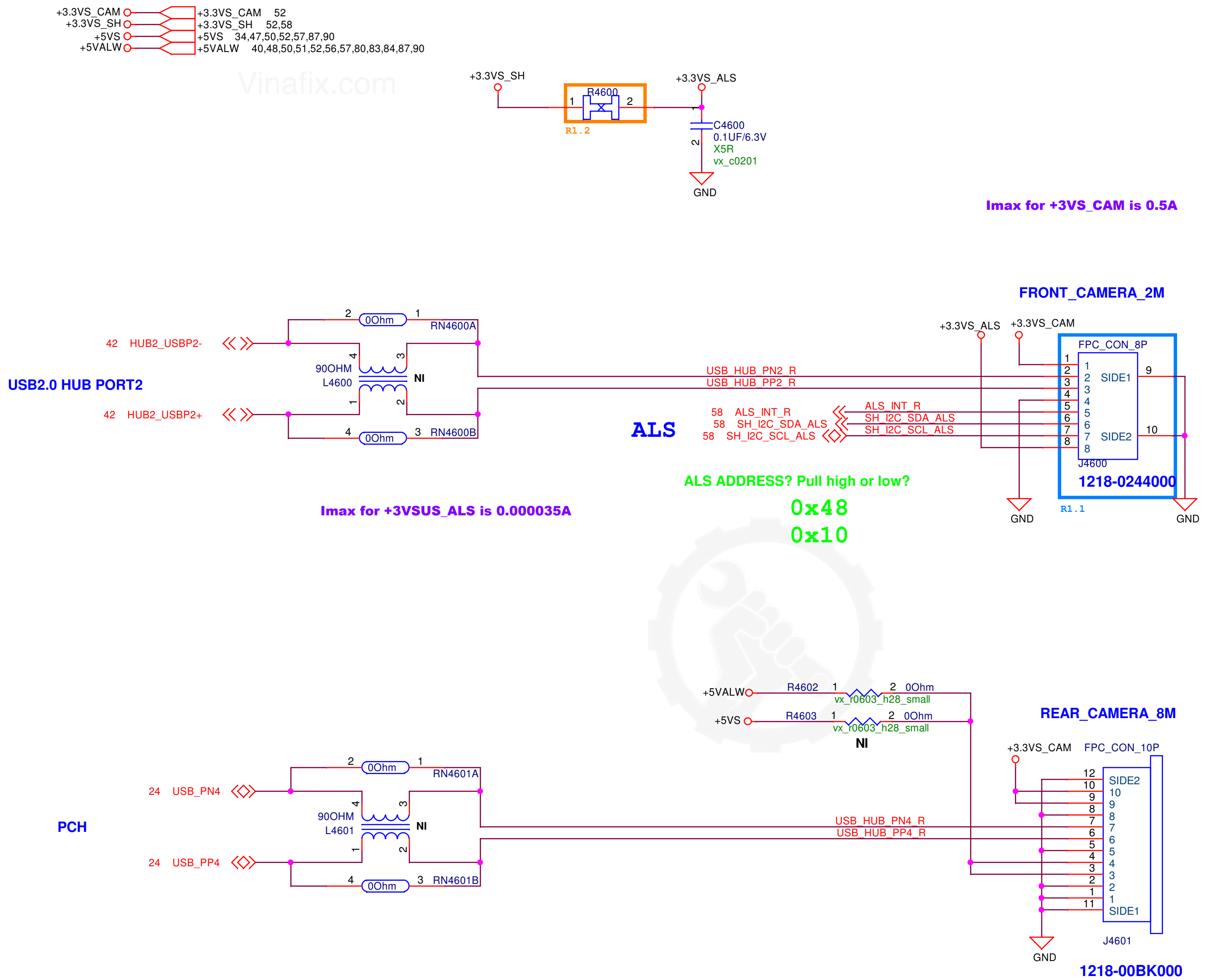
TITLE	eDP Connector	
DWG NO.	CORE_L	REV. 2.0
DATE	Wednesday, May 06, 2015	SHEET 45 of 99



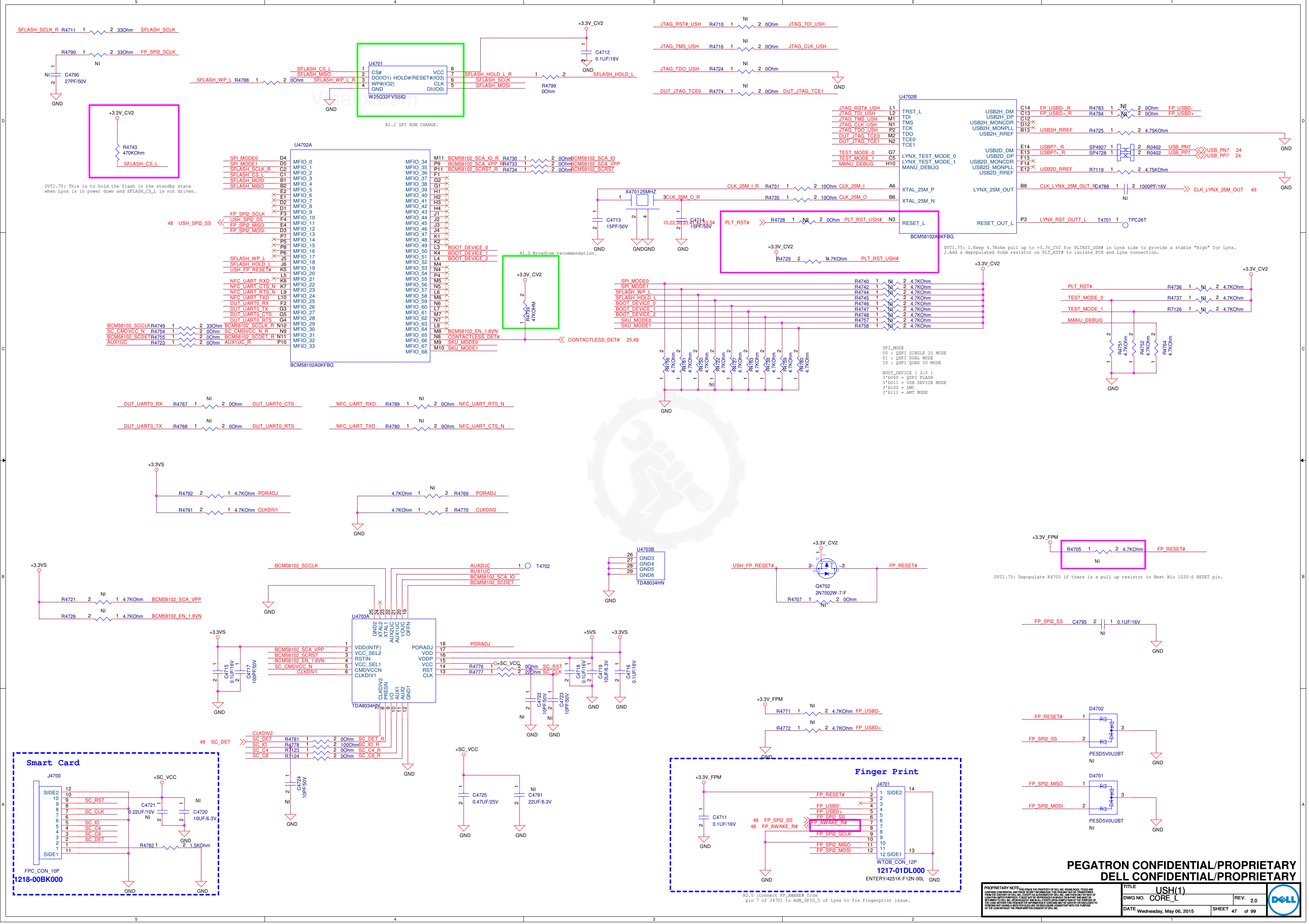
Device Side

CN table	
1	USB_3V3
2	DM
3	DP
4	GND
5	ALS_INT
6	ALS_DATA
7	ALS_CLK
8	ALS_VDD

Device Side

CN table	
1	VCC
2	VCC
3	GND
4	DM
5	DP
6	GND
7	LED_VCC
8	LED_VCC
9	LED_GND
10	LED_GND

TITLE CAMERA_FRONT/REAR
DWG NO. CORE_L
REV. 2.0
DATE Wednesday, May 06, 2015


U4701
W25Q32FVSSIQ
R1.2 SPI ROM CHANGE.
DVT1.75: This is to hold the flash in the standby state when Lynx is in power down and SFLASH_CS_L is not driven.
U4702A
BCM58102A0KFBG
R1.2 Broadcom recommendation.
U4702B
BCM58102A0KFBG
X4701 25MHZ
DVT1.75: 1.Keep 4.7KOhm pull up to +3.3V_CV2 for PLTRST_USH# in Lynx side to provide a stable "High" for Lynx.
2.Add a depopulated 0ohm resistor on PLT_RST# to isolate PCH and Lynx connection.
SPI_MODE
00 : QSPI SINGLE IO MODE
01 : QSPI DUAL MODE
10 : QSPI QUAD IO MODE
NOOT_DEVICE [2:0]
3'b000 = QSPI FLASH
3'b011 = USB DEVICE MODE
3'b100 = SMC
3'b111 = AMT MODE
U4703B
TDA8034HN
U4703A
TDA8034HN
Q4702
2N7002W-7-F
DVT1.75: Depopulate R4705 if there is a pull up resistor in Next Bio 1020-S RESET pin.
Smart Card
J4700
FPC_CON_10P
1218-00BK000
Finger Print
J4701
WTOB_CON_12P
1217-01DL000
ENTERY/4251K-F12N-00L
R2.0 :Connect FP_AWAKE# from pin 7 of J4701 to AON_GPIO_5 of Lynx to fix fingerprint issue.
D4702
PESD5V0U2BT
D4701
PESD5V0U2BT
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TITLE USH(1)
DWG NO. CORE_L
REV. 2.0
DATE Wednesday, May 06, 2015
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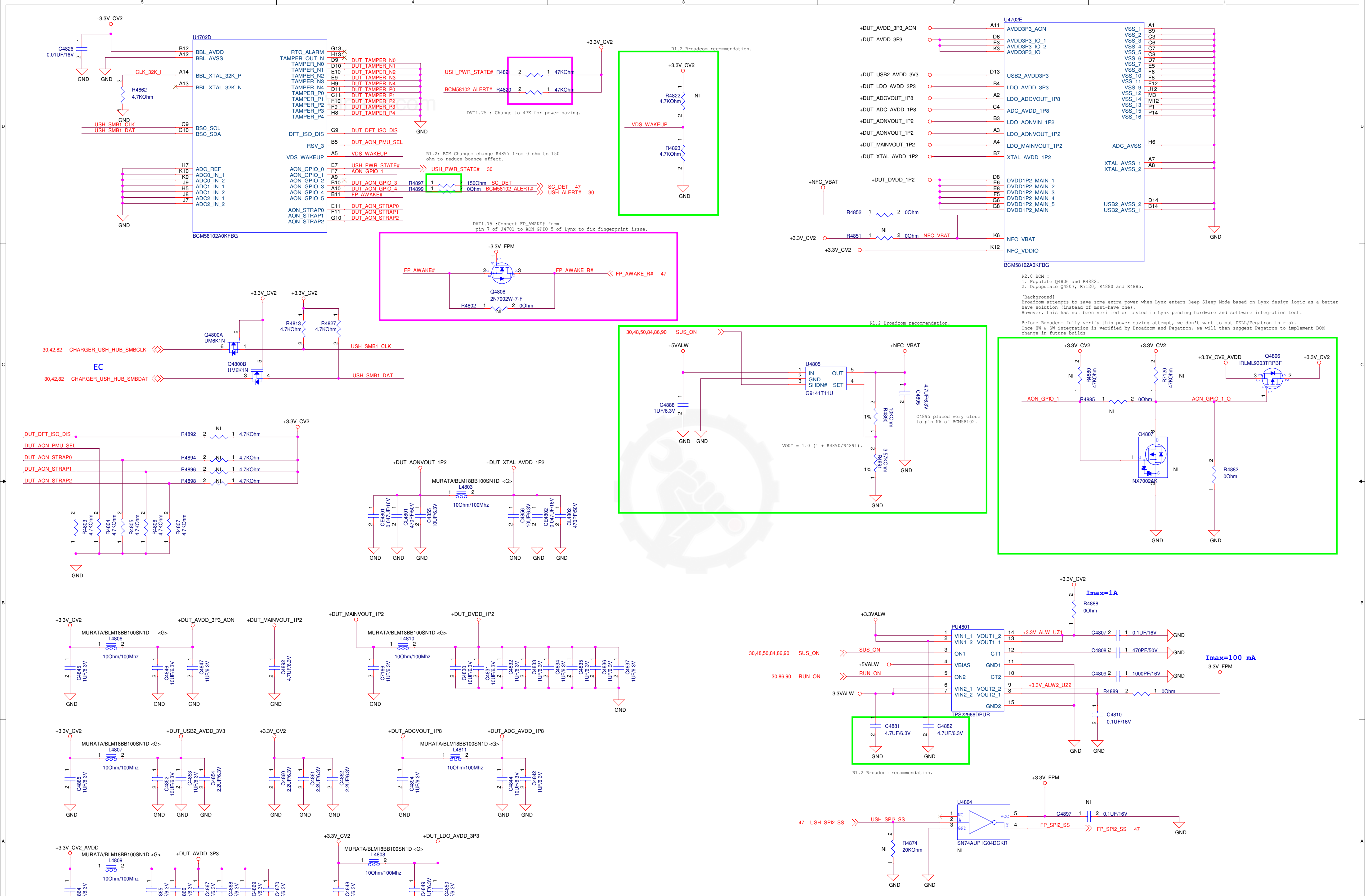

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PROPRIETARY NOTE

TITLE	USH(2)
DWG NO.	CORE_L
REV.	2.0
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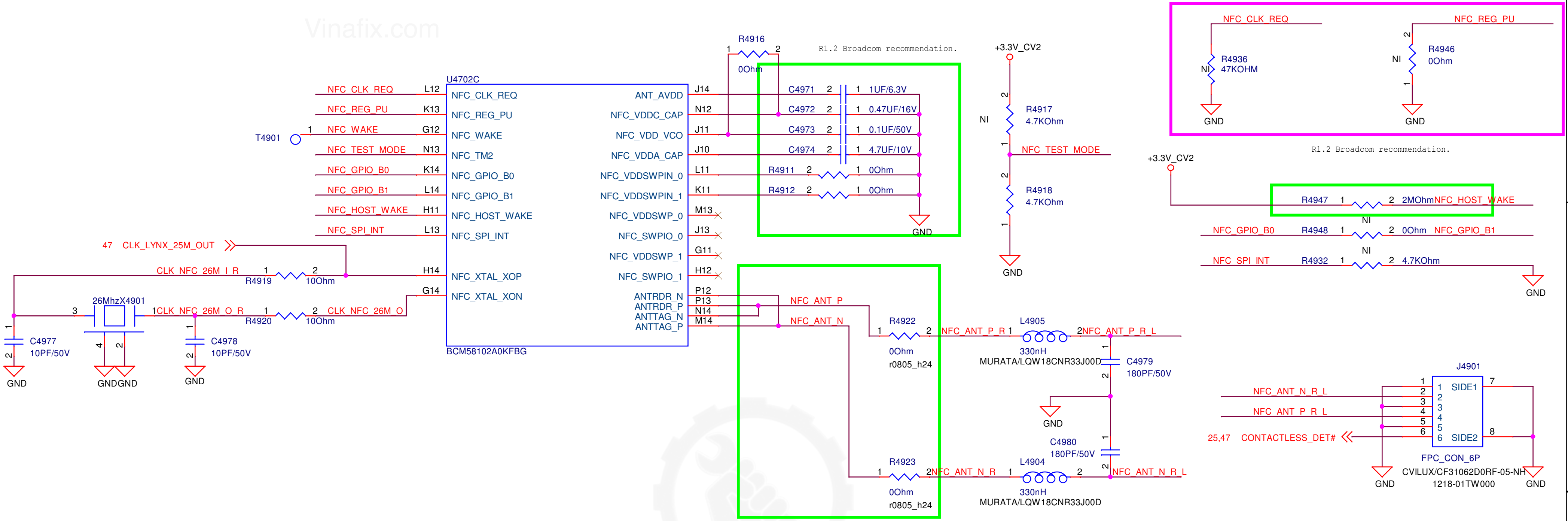
DVT1.75 BCR: The CLK_REQ on 20795 does not have internal pull down resistor.
This can potentially keep CLK_REQ high when the chip is off. If local Xtal is always used then there is no need to have this resistor. However, we may try to use 25MHz host clock from Lynx to 20795 in near future in order to save BOM cost, we need to add this pull-down resistor in advance.



R1.2 BCM : Add a populated "0ohm" (0805 footprint) resistor between Lynx and L4905 and L4904 respectively.

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TITLE	USH(3)
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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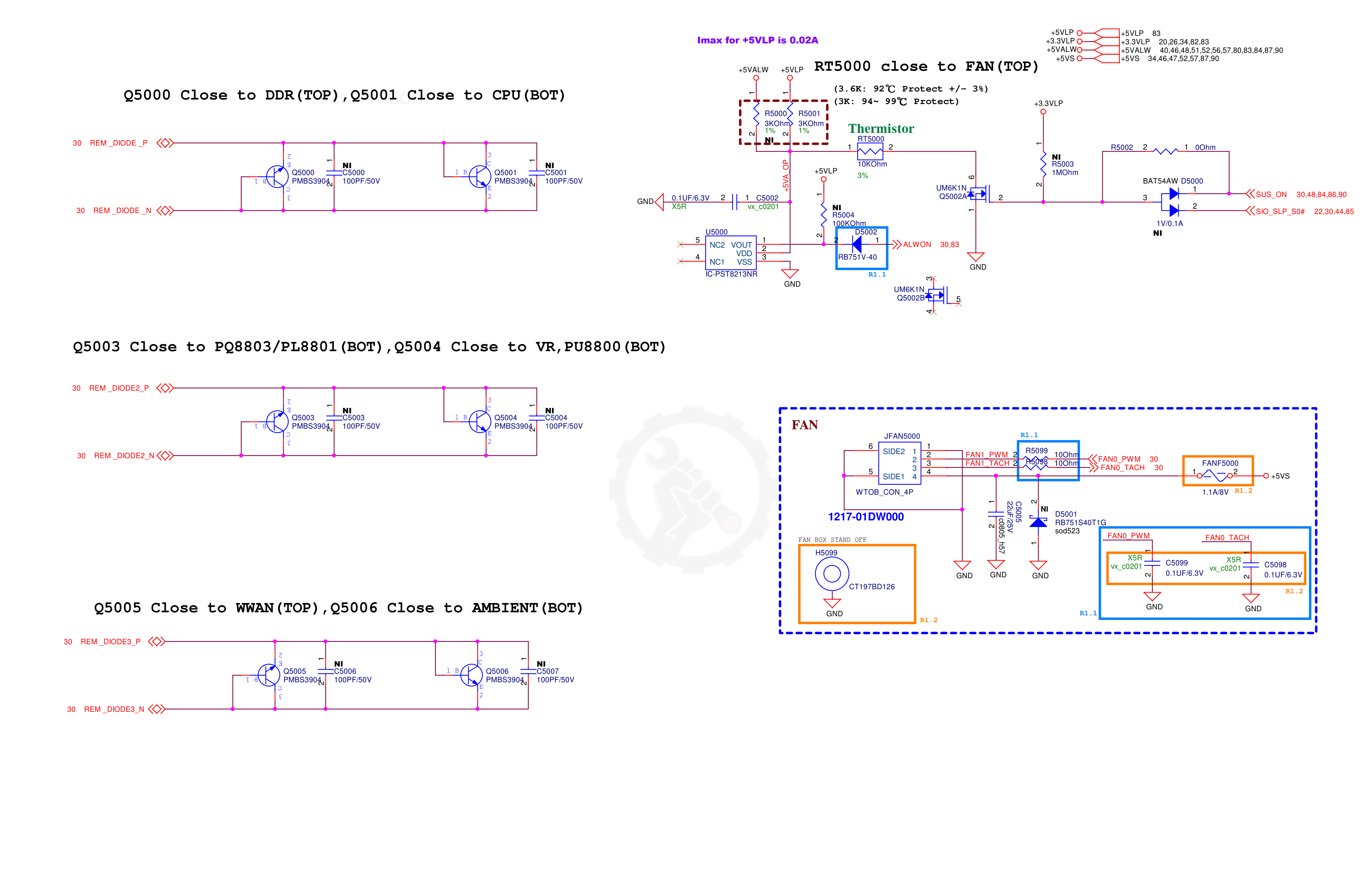

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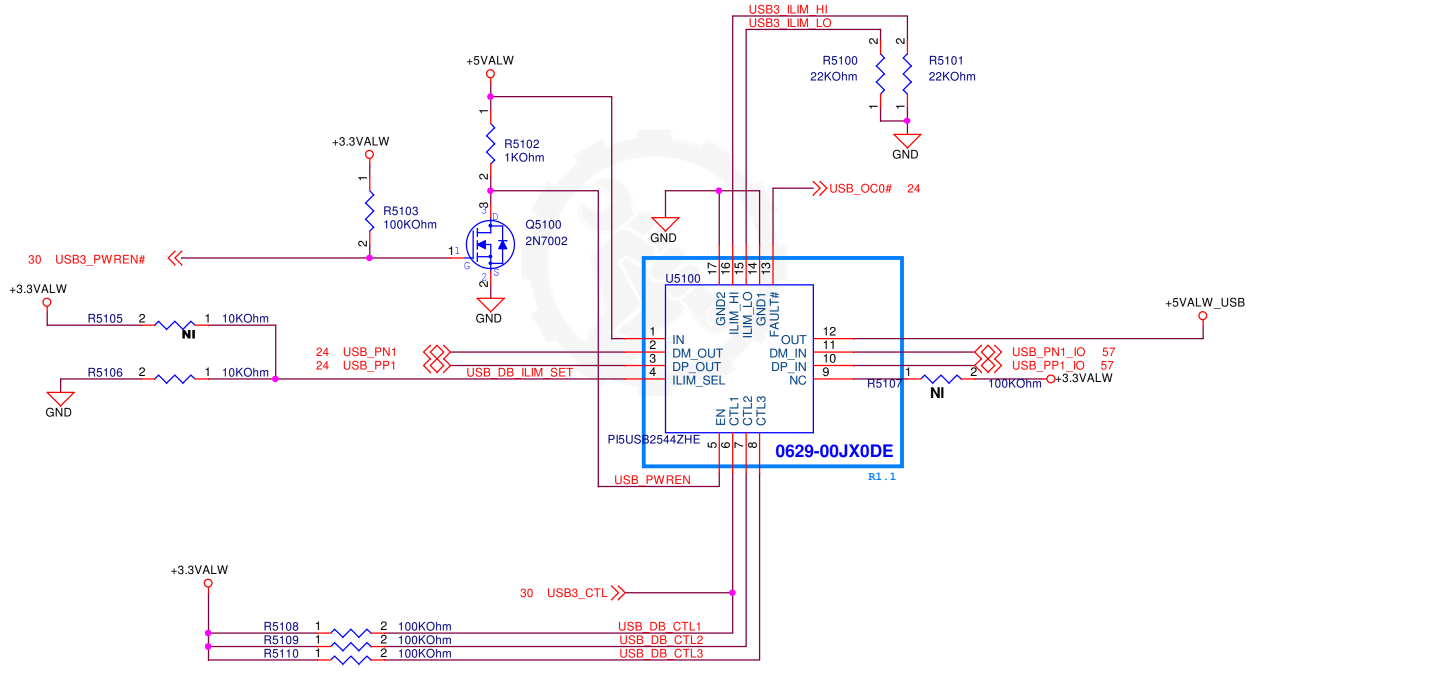
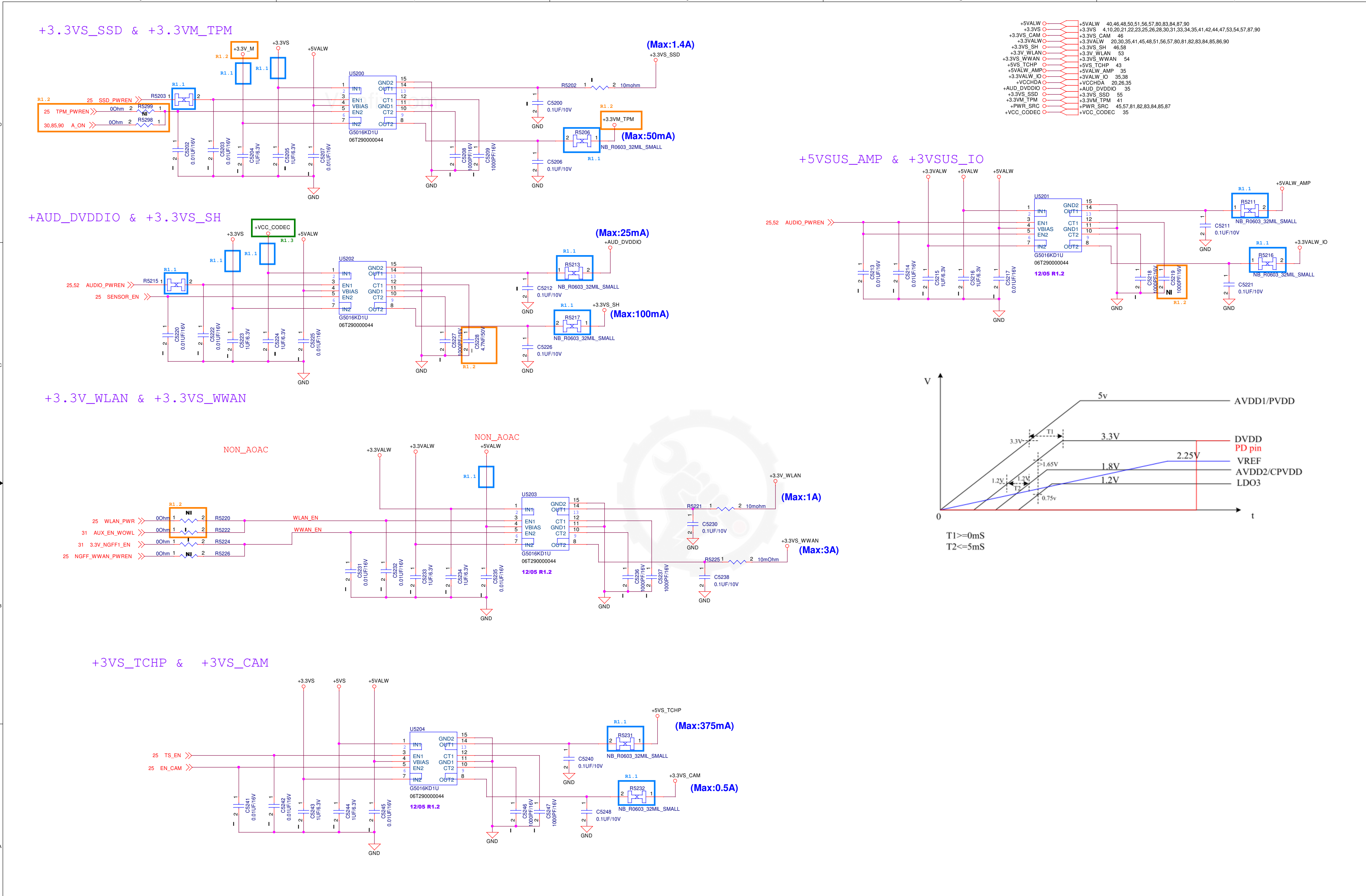
TITLE THERMAL Sensors / FAN			
DWG NO.	CORE_L	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	50 of 99

+5VALW +5VALW 40,46,48,50,52,56,57,80,83,84,87,90
+3.3VALW +3.3VALW 20,30,35,41,45,48,52,56,57,80,81,82,83,84,85,86,90
+5VALW_USB +5VALW_USB 57

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
ILIM_SEL Current Limit						
I_{OS}	OUT Current-limit(2)	V_{ILIM_SEL}= 0 V R_{ILIM_LO}=210kΩ	205	240	275	mA
		V_{ILIM_SEL}= 0 V R_{ILIM_LO}=80.6kΩ	575	625	680	
		V_{ILIM_SEL}= 0 V R_{ILIM_LO}=22.1kΩ	2120	2275	2430	
		V_{ILIM_SEL}= V_{IN} R_{ILIM_HI}=20kΩ	2340	2510	2685	
		V_{ILIM_SEL}= V_{IN} R_{ILIM_HI}=16.9kΩ	2770	2970	3170	
t_{IOS}	Response time to OUT short circuit(1)	V_{IN} = 5.0V, R=0.1Ω, lead length=2”	-	1.5	-	µs



TITLE	USB Charger
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
SHEET	51 of 99



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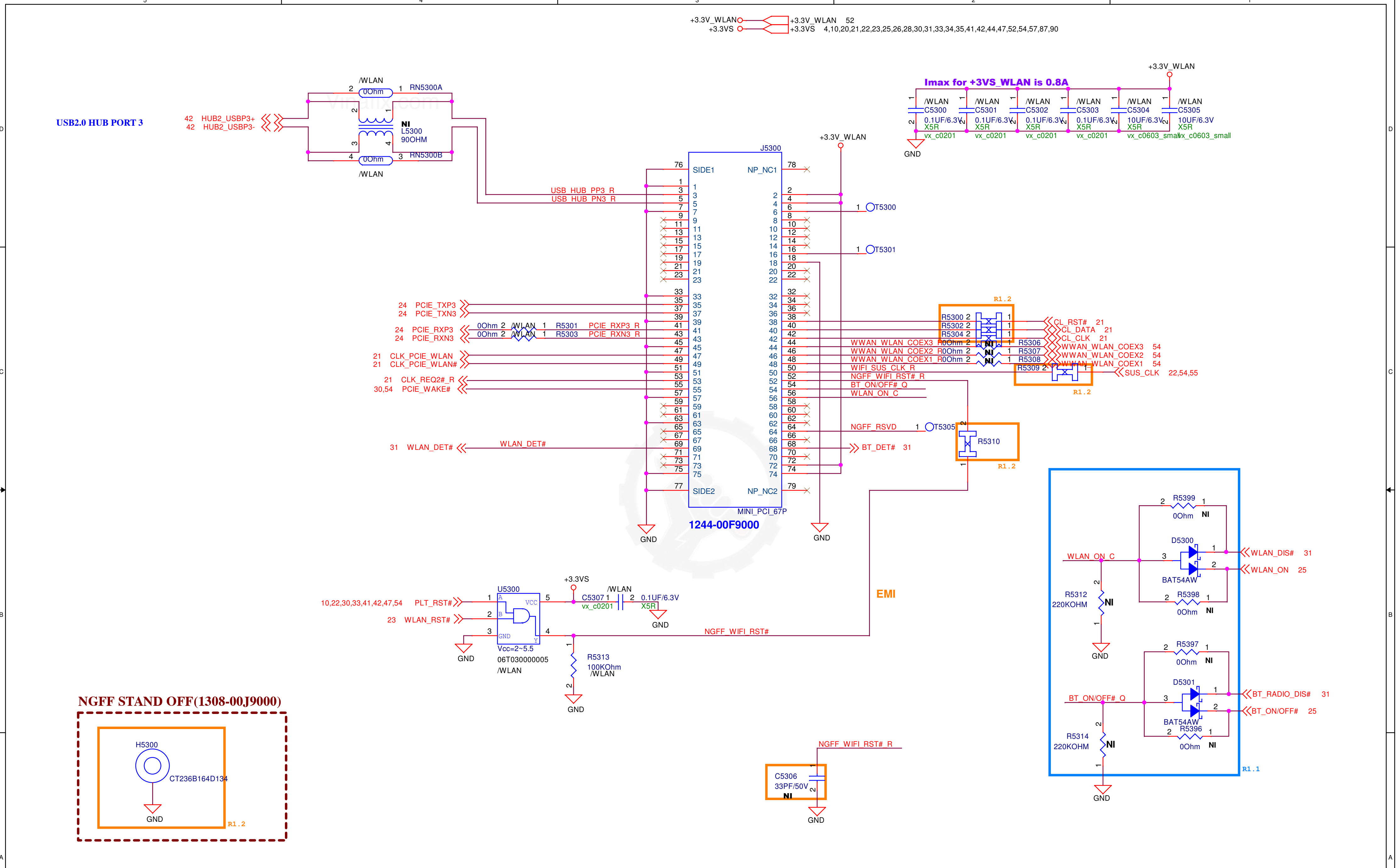
TITLE PWR_SW		
DWG NO. CORE_L		REV. 2.0
DATE Wednesday, May 06, 2015	SHEET 52 of 99	



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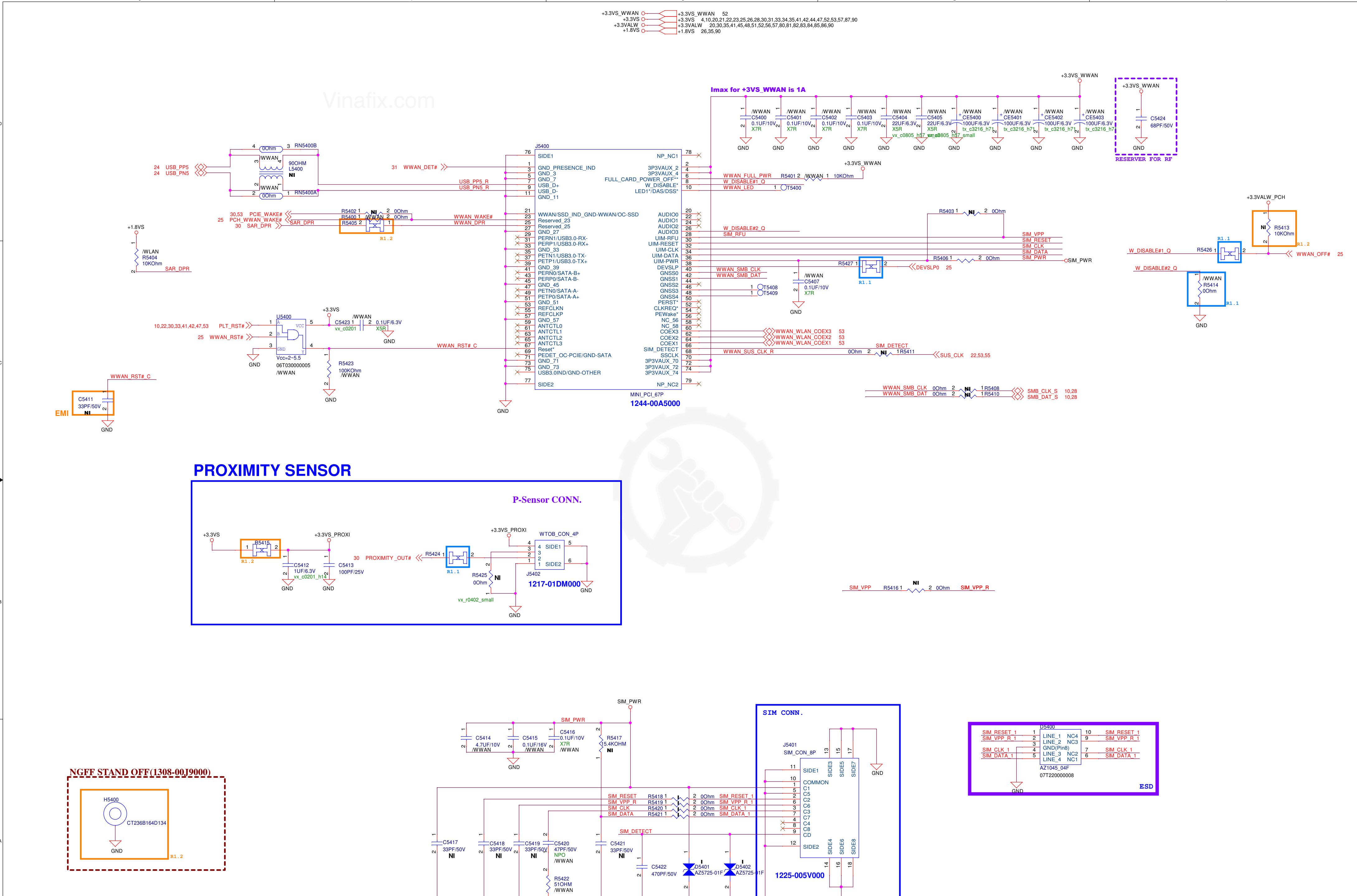
TITLE	NGFF_WLAN
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
SHEET	53 of 99



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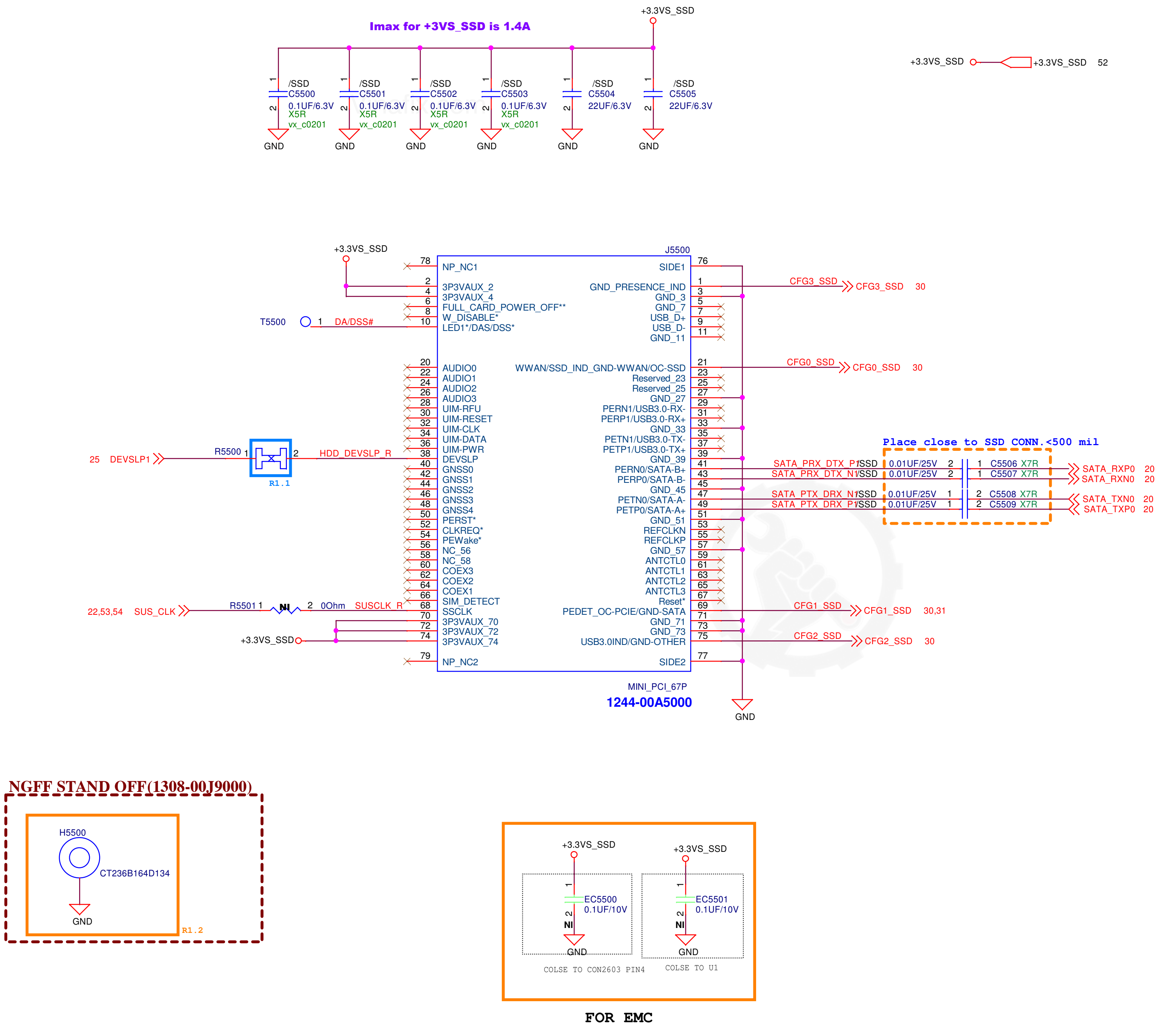
TITLE	NGFF_WWAN
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
SHEET	54 of 99



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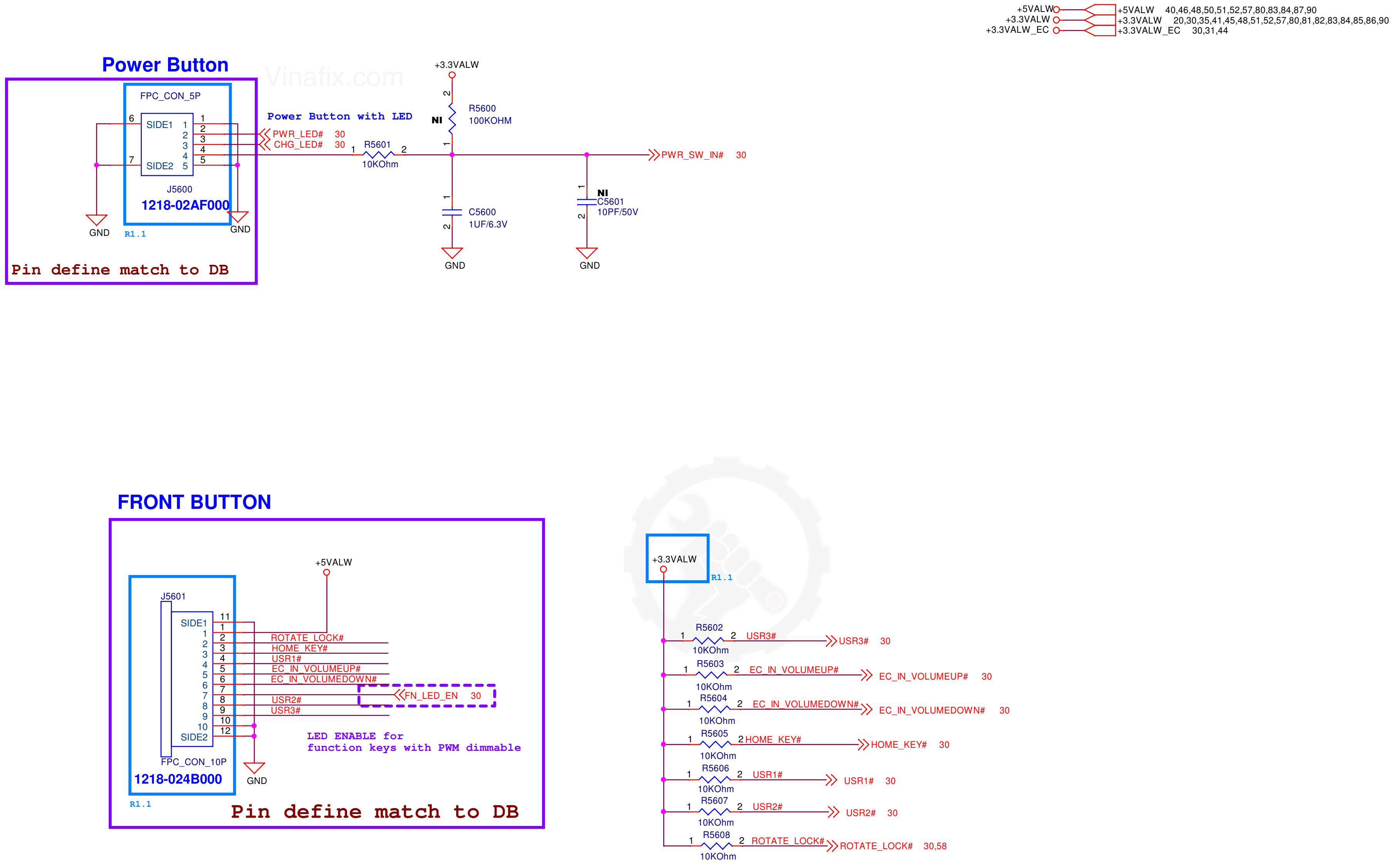
TITLE NGFF_SSD
DWG NO. CORE_L
REV. 2.0
DATE Wednesday, May 06, 2015



TITLE	Buttons(power,front) / LED
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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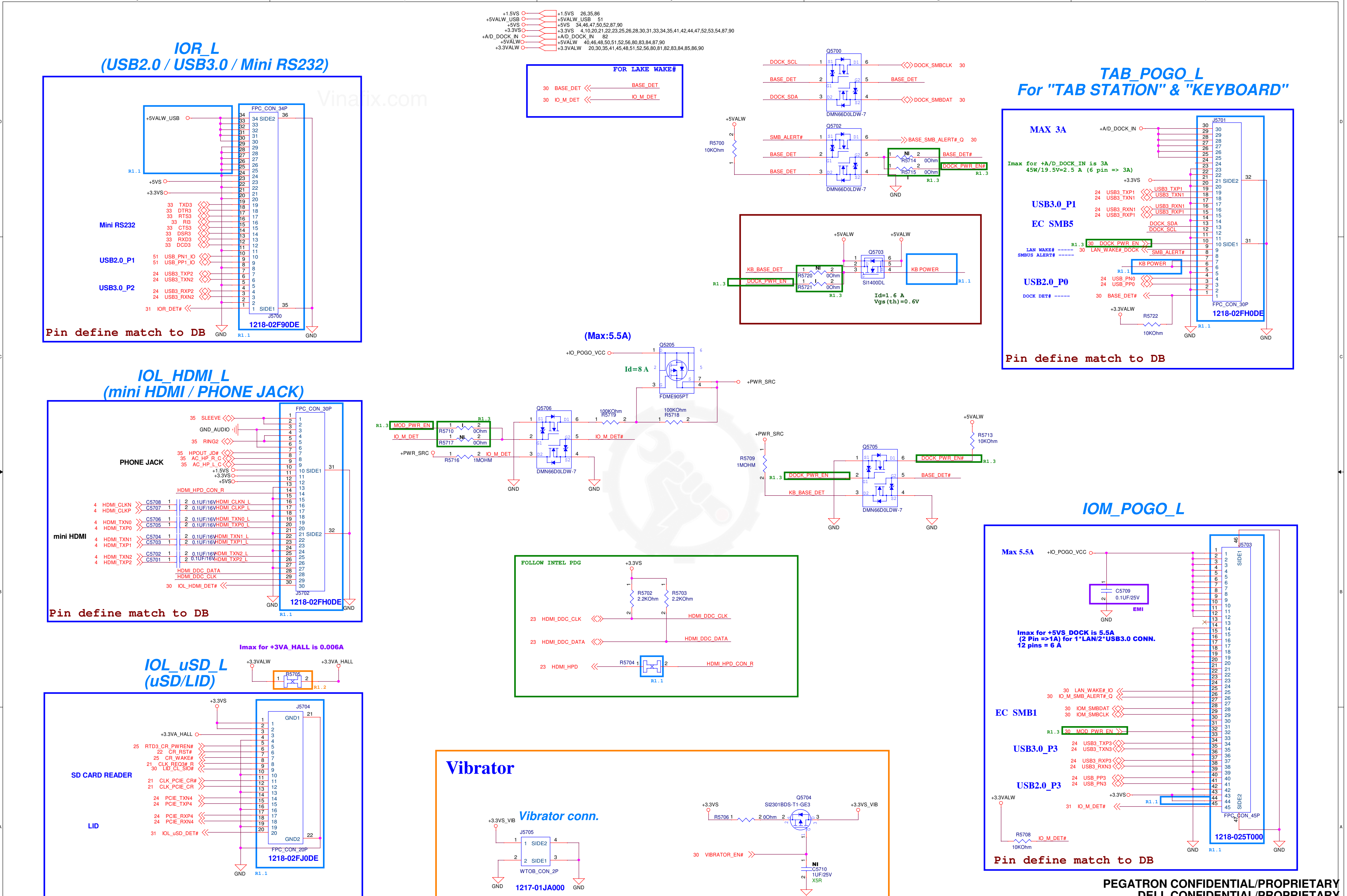

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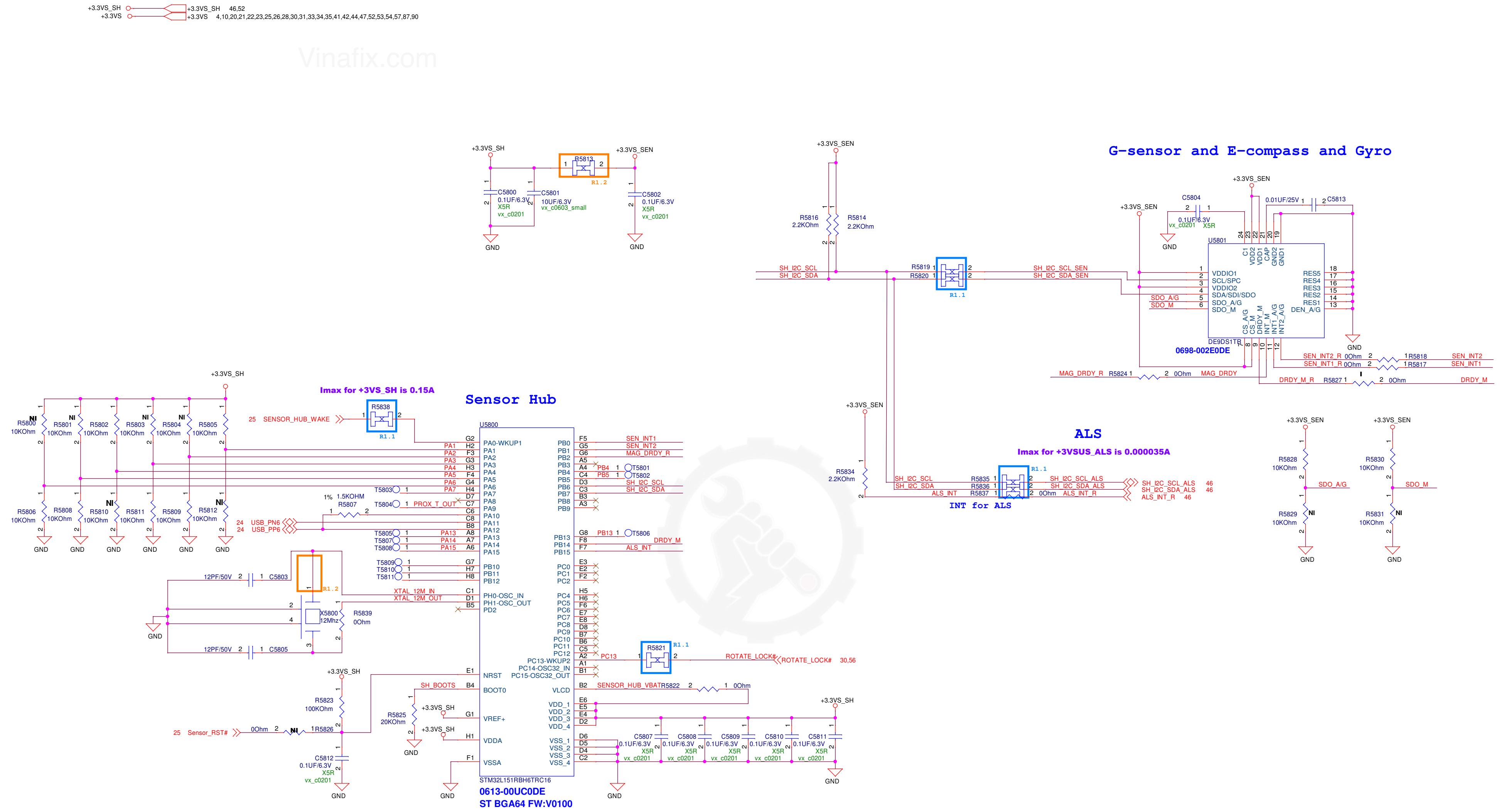
TITLE DB CONN		
DWG NO. CORE_L		REV. 2.0
DATE Wednesday, May 06, 2015		SHEET 57 of 99



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TITLE	SENSOR HUB / SENSOR x3
DWG NO.	CORE_L
REV.	2.0
DATE	Wednesday, May 06, 2015
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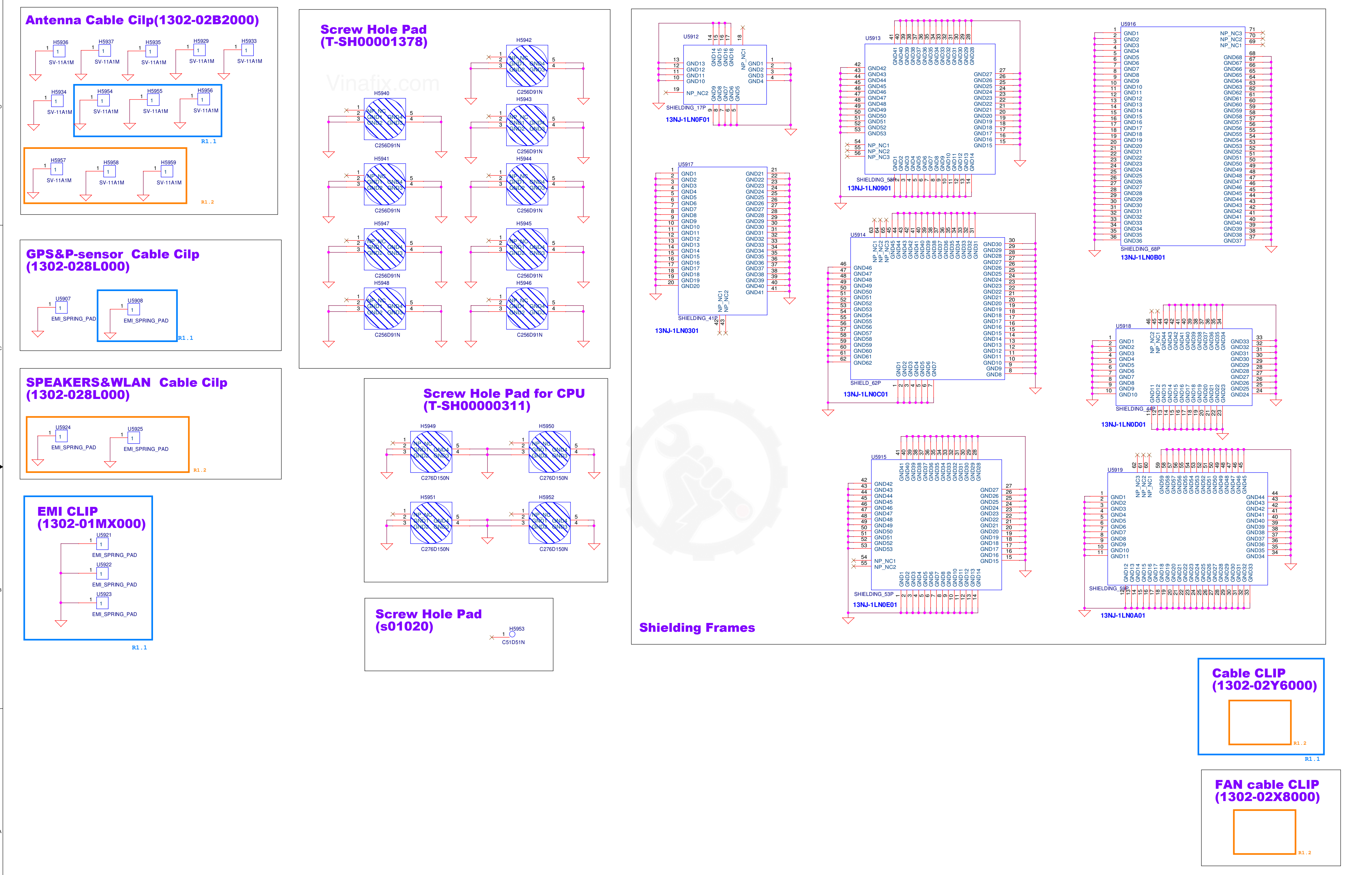

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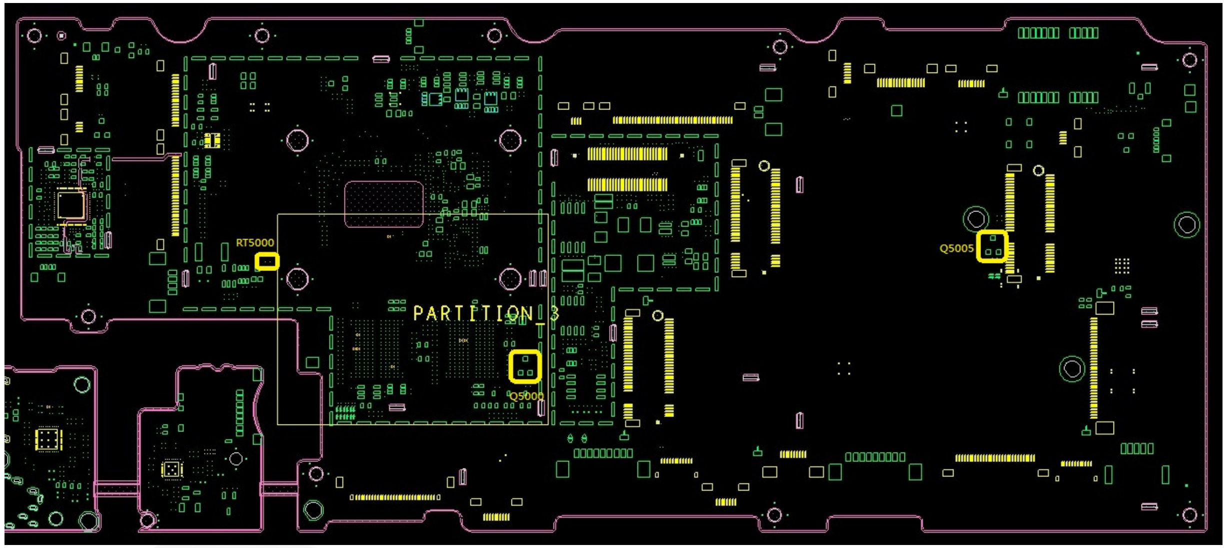
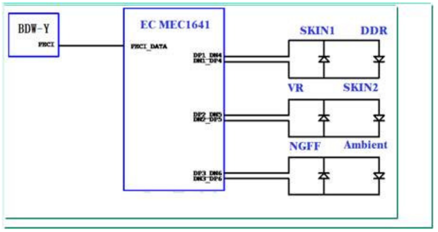
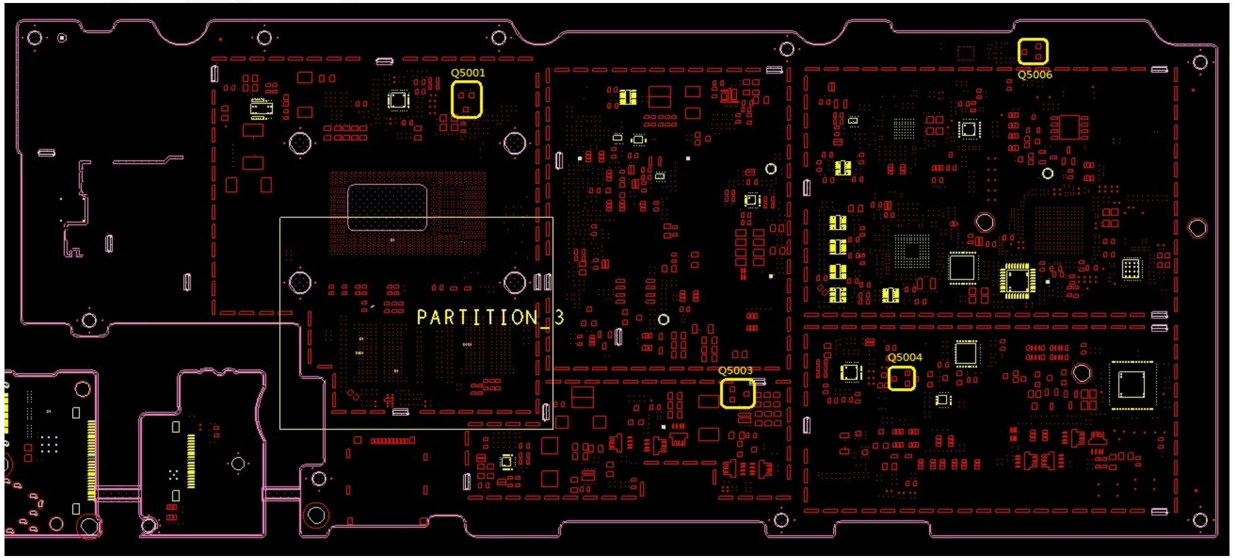
TITLE ME_CONN,Skew Hole			
DWG NO. CORE_L		REV. 2.0	
DATE Wednesday, May 06, 2015	SHEET 59 of 99		

Thermal sensor block diagram

Item	Description / Location
Sensor 1	Q5000 Close to DDR(TOP)
Sensor 2	Q5001 Close to CPU(BOT)
Sensor 3	Q5003 Close to PQ8803/PL8801(BOT)
Sensor 4	Q5004 Close to VR,PU8800(BOT)
Sensor 5	Q5005 Close to WWAN(TOP)
Sensor 6	Q5006 Close to AMBIENT(BOT)
Sensor 7	RT5000 close to FAN(TOP)

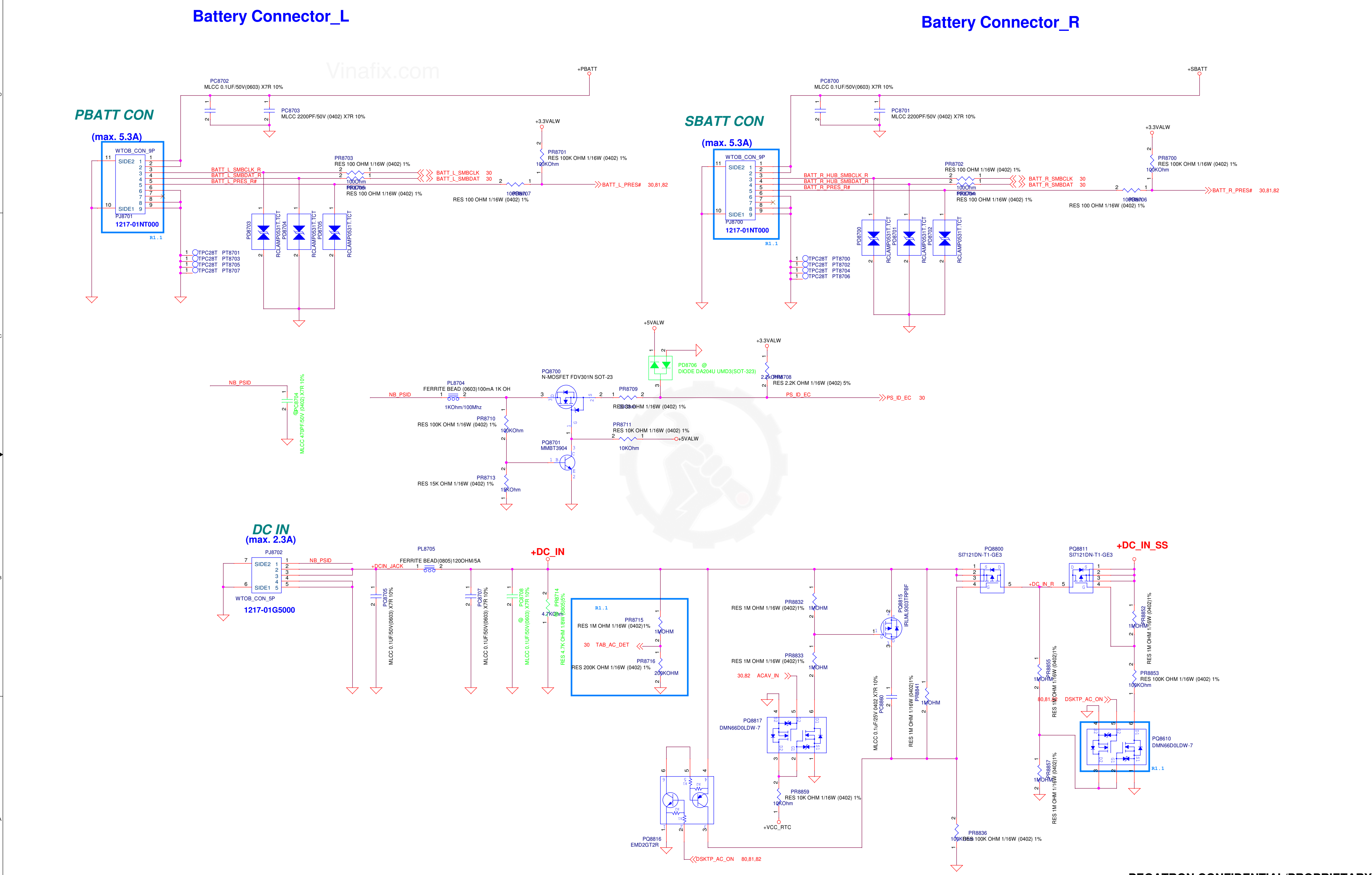






TITLE	Thermal sensor block diagram		
DWG NO.	CORE_L	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	60 of 99

Main Board



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TITLE	PWR_+DCIN
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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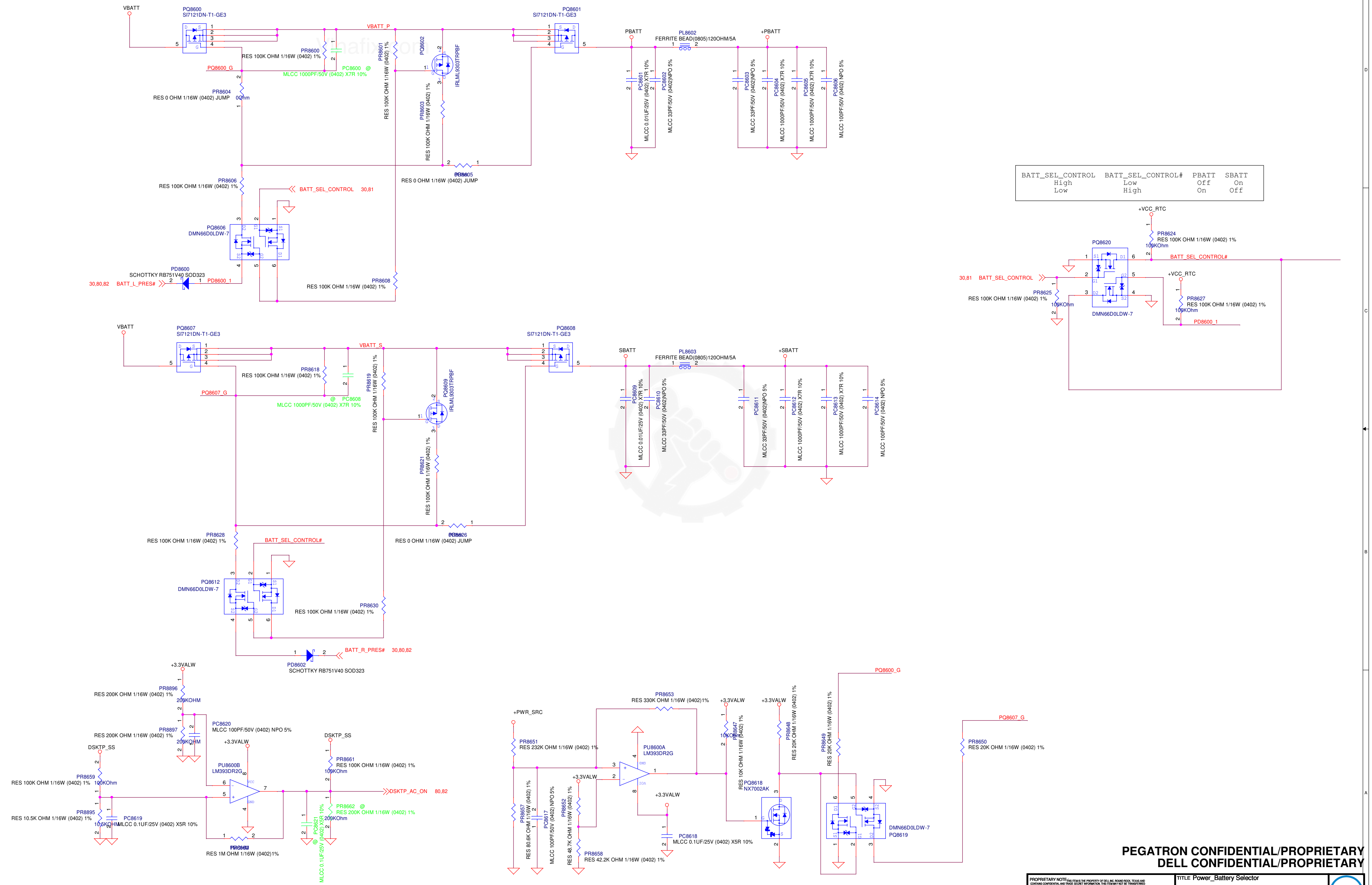
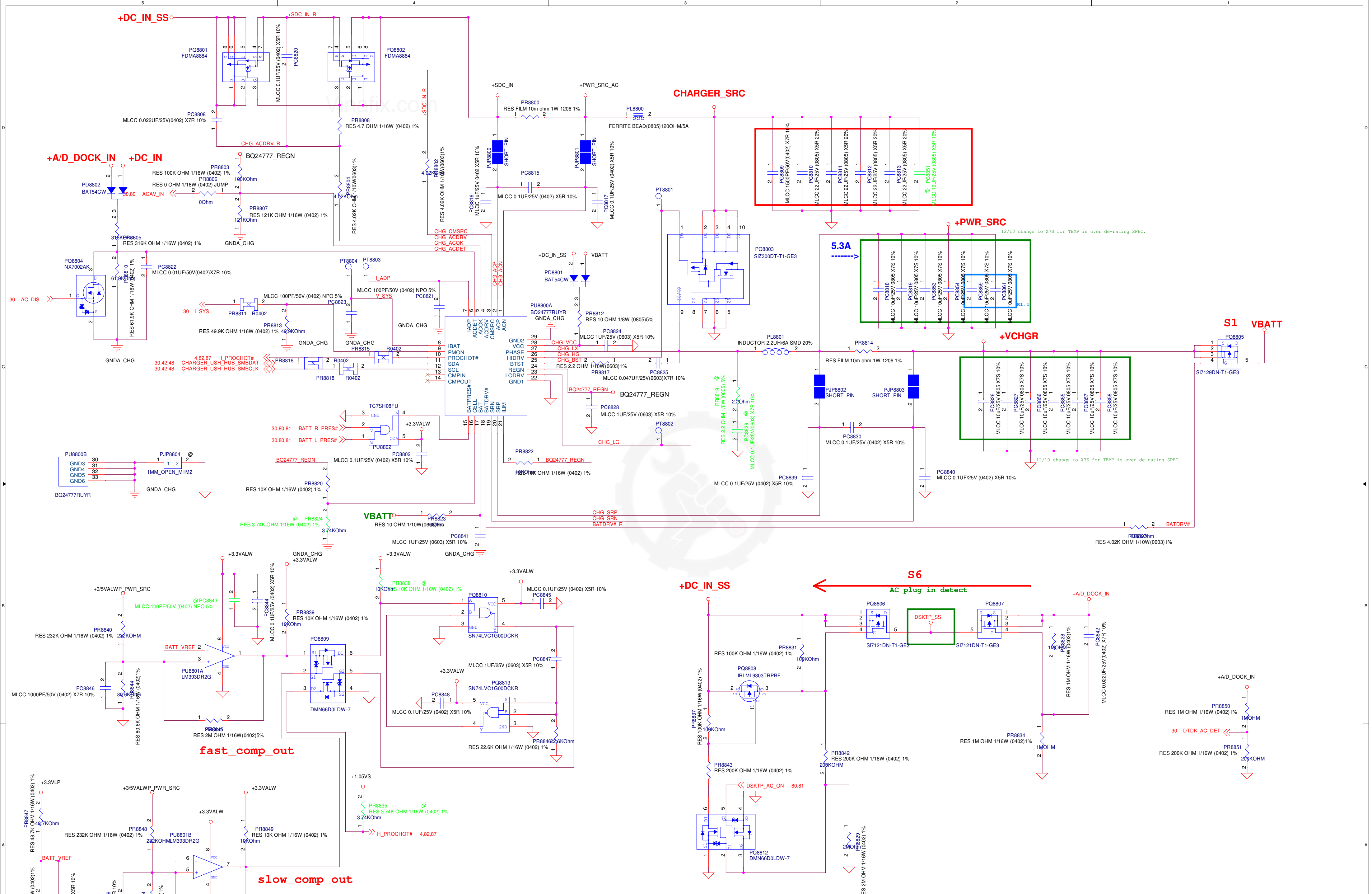


BATT_SEL_CONTROL	BATT_SEL_CONTROL#	PBATT	SBATT
High	Low	Off	On
Low	High	On	Off

TITLE	Power_Battery Selector		
DWG NO.	CORE_B	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	81 of 99



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TITLE	POWER_CHARGER
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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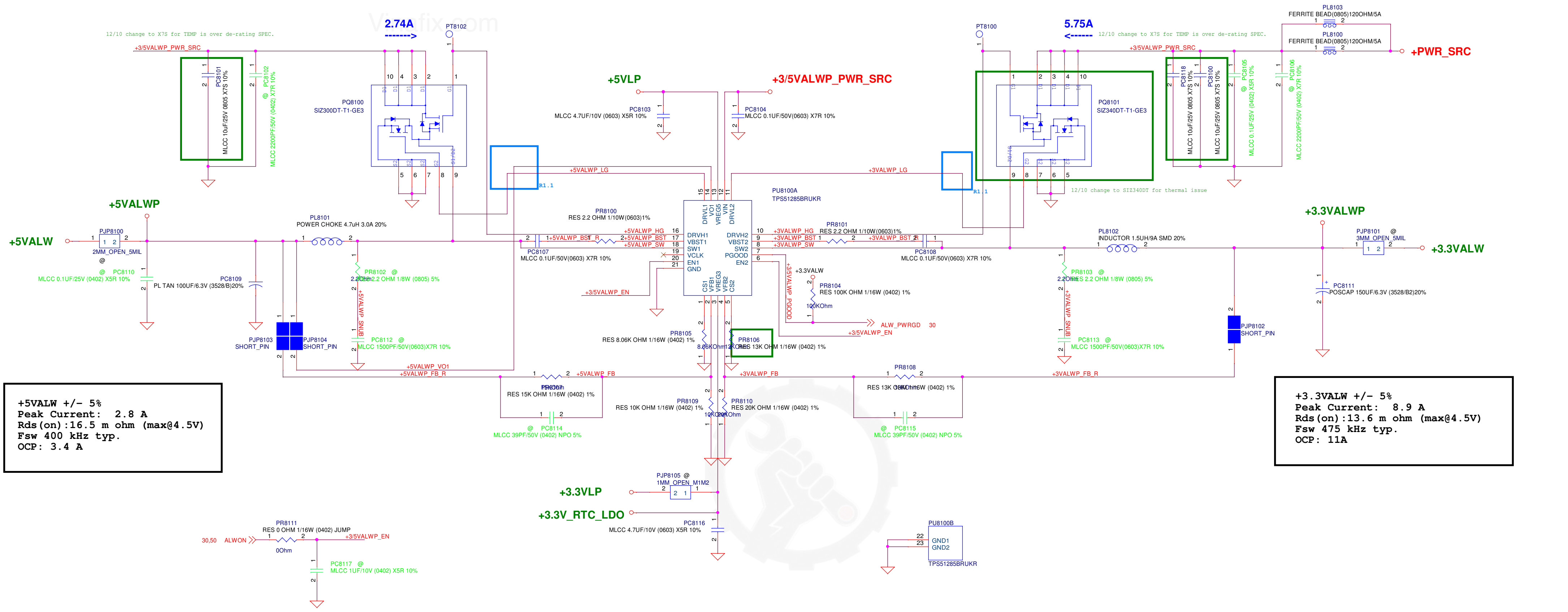


```
+5VALW +/- 5%
Peak Current:  2.8 A
Rds(on):16.5 m ohm (max@4.5V)
Fsw 400 kHz typ.
OCP: 3.4 A
```

```
+3.3VALW +/- 5%
Peak Current:  8.9 A
Rds(on):13.6 m ohm (max@4.5V)
Fsw 475 kHz typ.
OCP: 11A
```

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TITLE	PWR_+5VALWP/+3.3VALWP
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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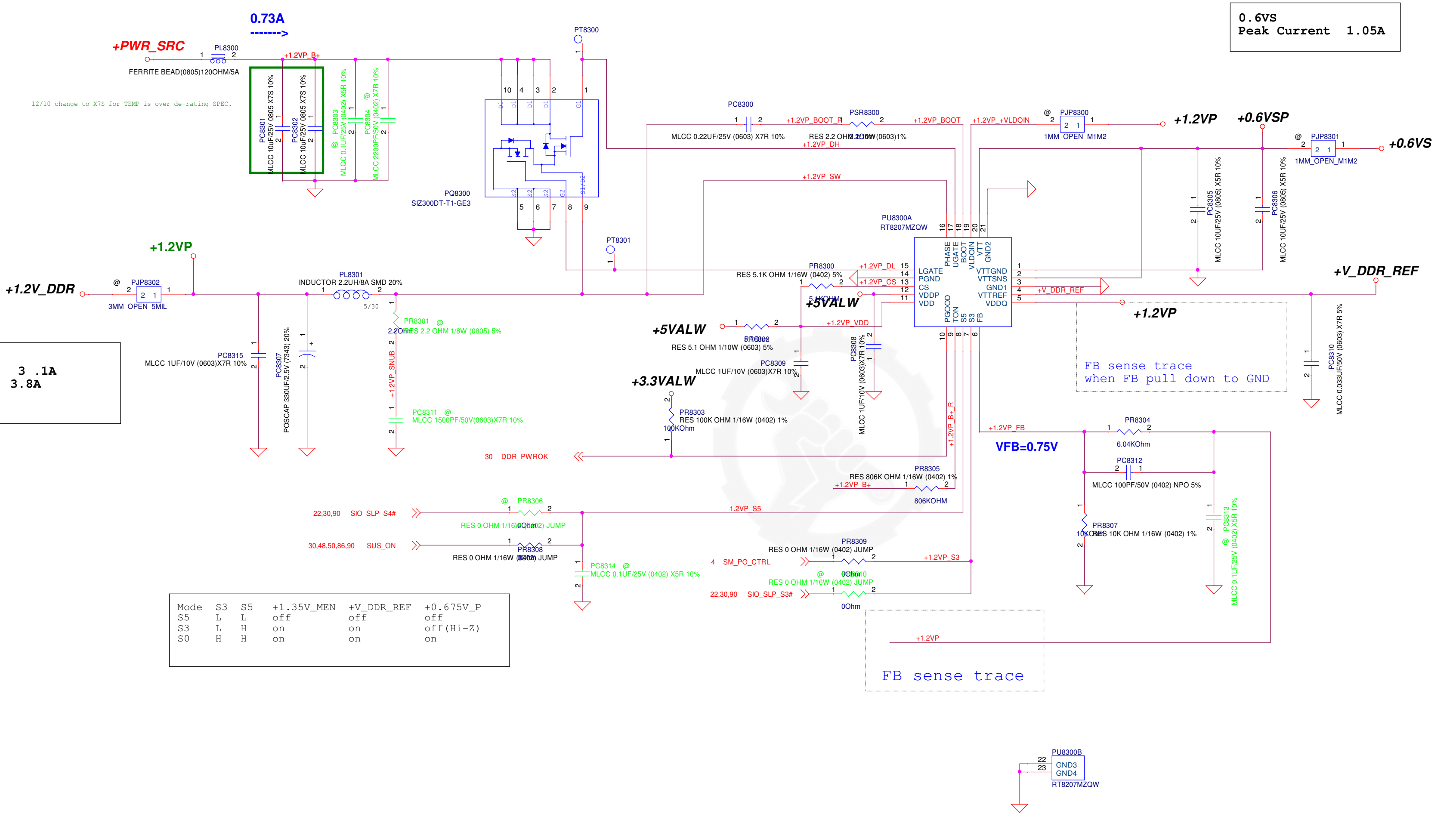
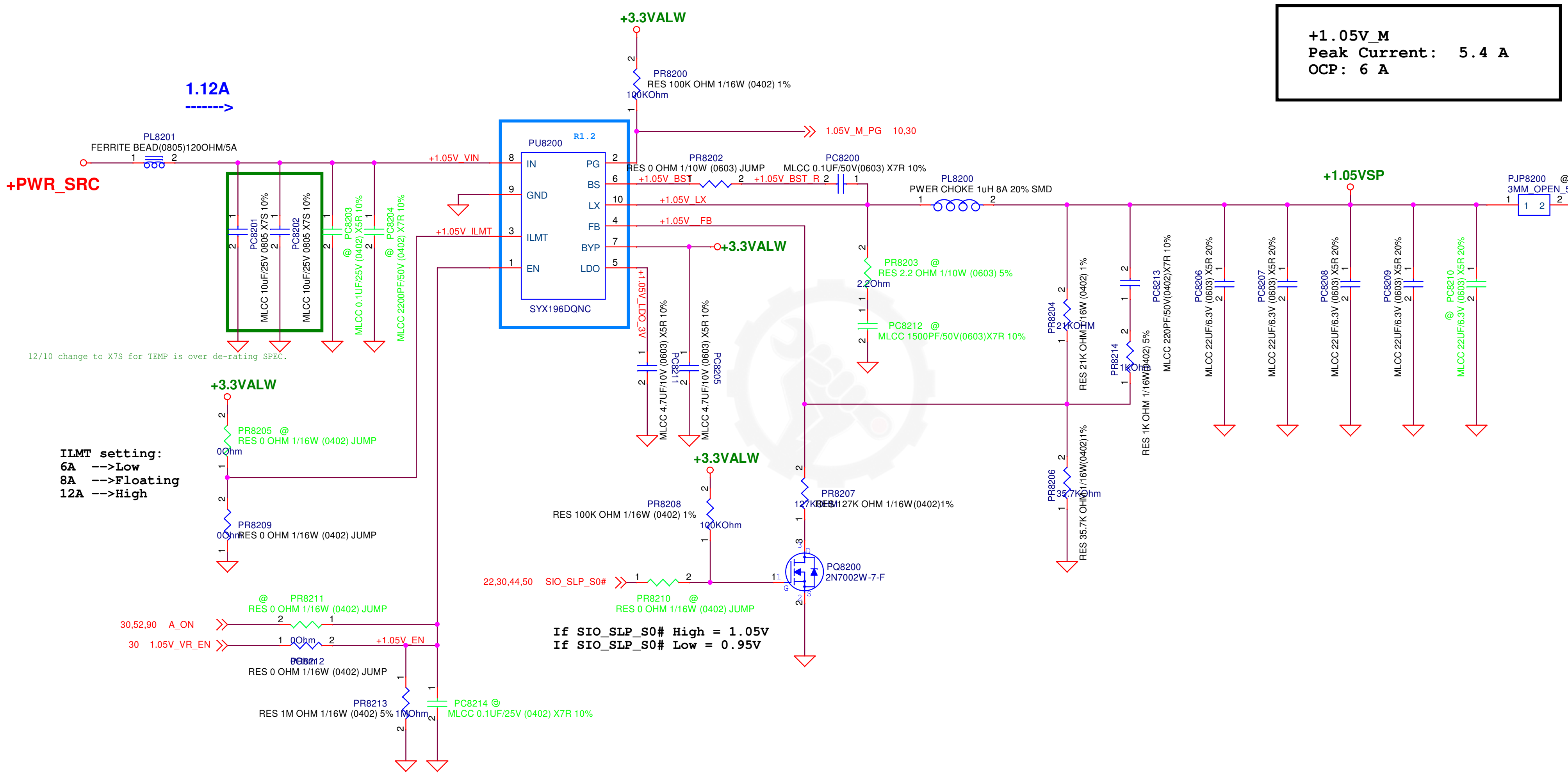


0.6VS
Peak Current 1.05A

1.2VP +/- 5%
Peak Current: 3 .1A
OCP current: 3.8A
Fsw=300 kHz

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on



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TITLE	POWER_ +1.05VM		
DWG NO.	CORE_B	REV.	2.0
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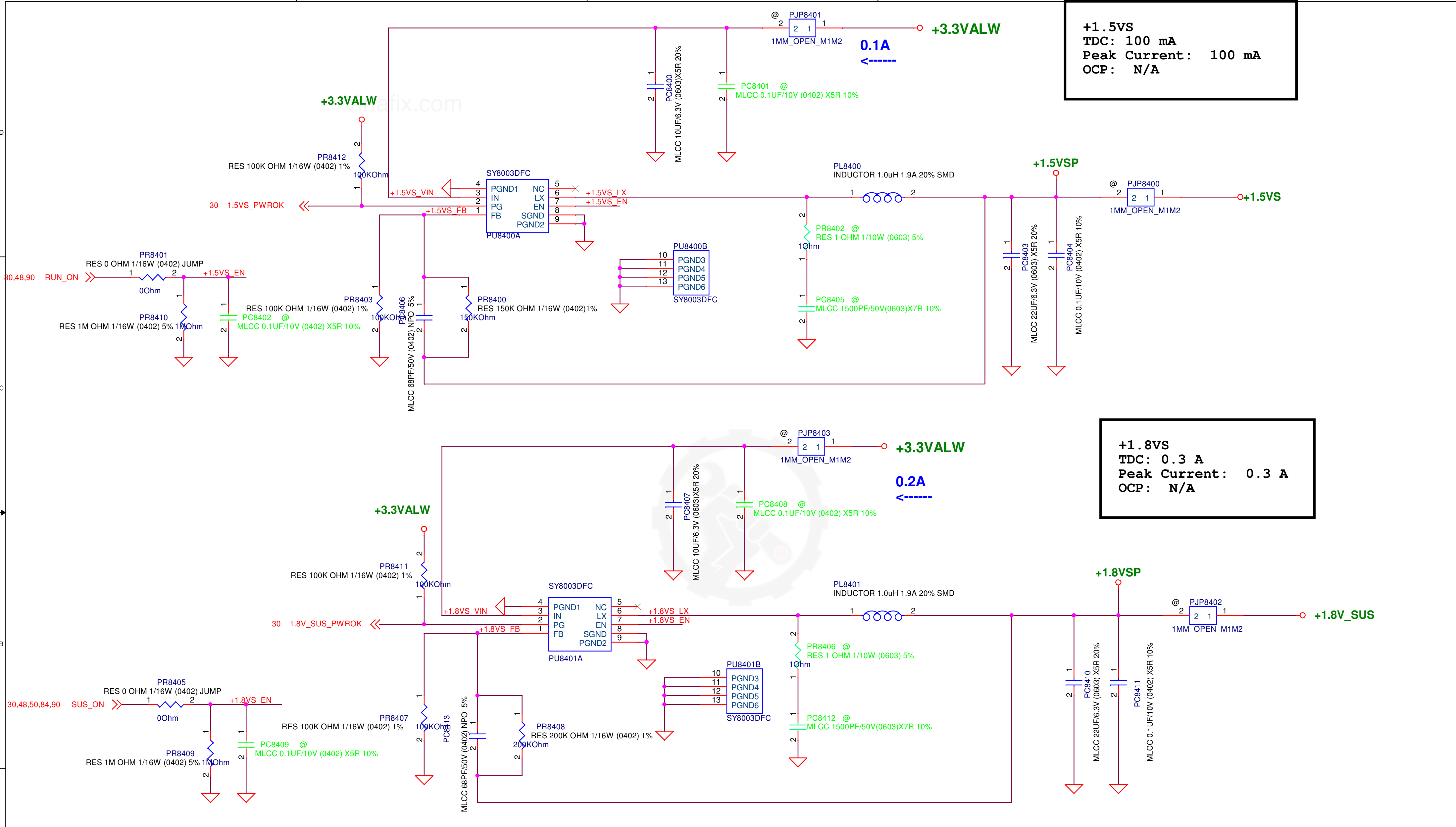

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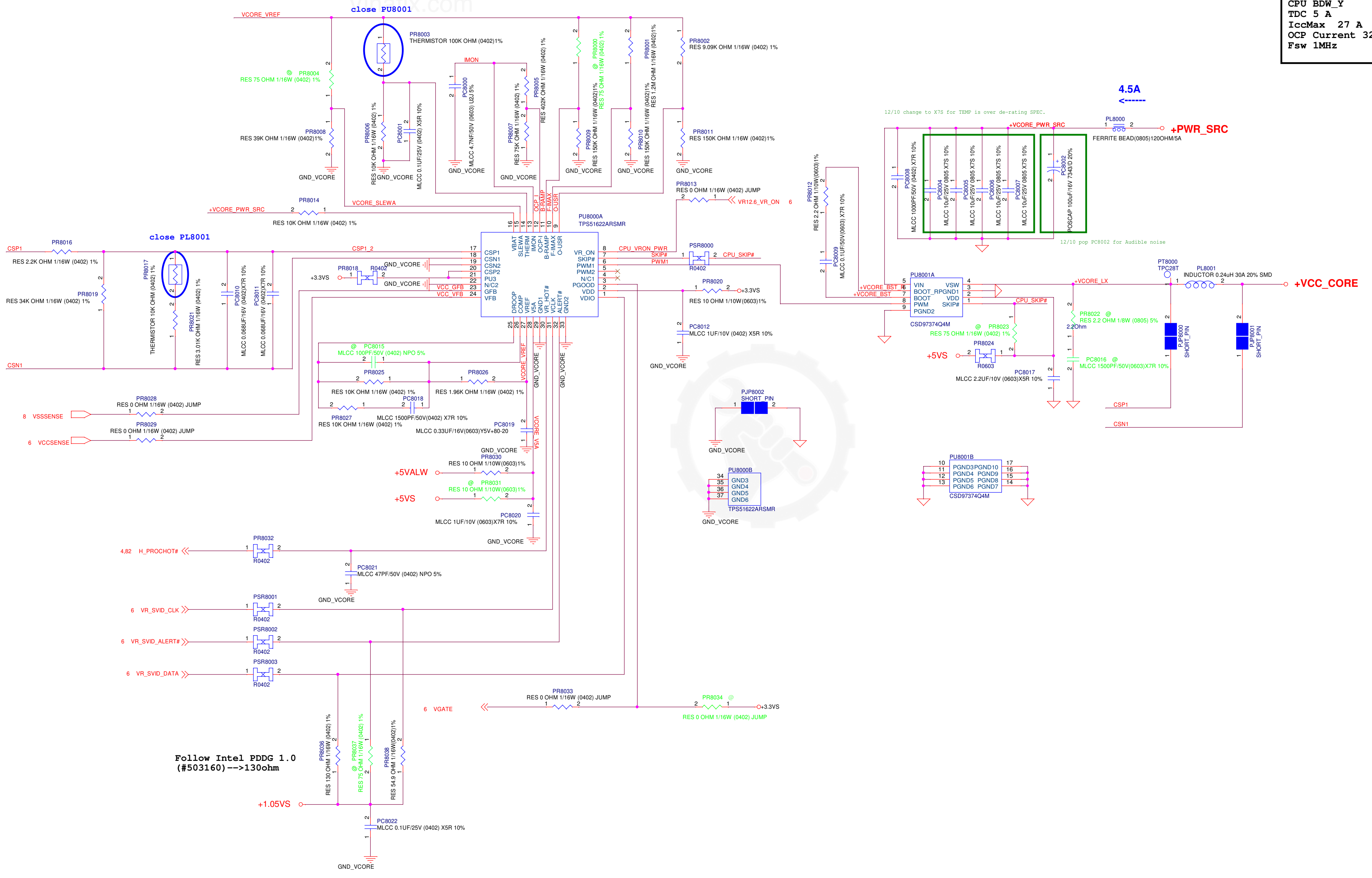
DELL CONFIDENTIAL/PROPRIETARY

TITLE	POWER_1.5V & 1.8V		
DWG NO.	CORE_B	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	86 of 99

CPU BDW_Y
TDC 5 A
IccMax 27 A
OCP Current 32.4 A
Fsw 1MHz



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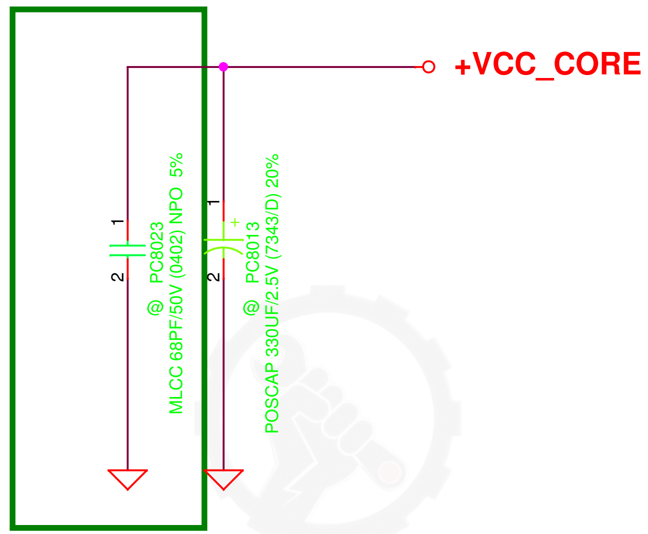
TITLE	PWR: +VCORE
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
SHEET	87 of 99



reserve PC8023 for WWAN low/high band TIS solution

TITLE PWR_CPU Decoupling			
DWG NO. CORE_B		REV. 2.0	
DATE Wednesday, May 06, 2015		SHEET 88	of 99

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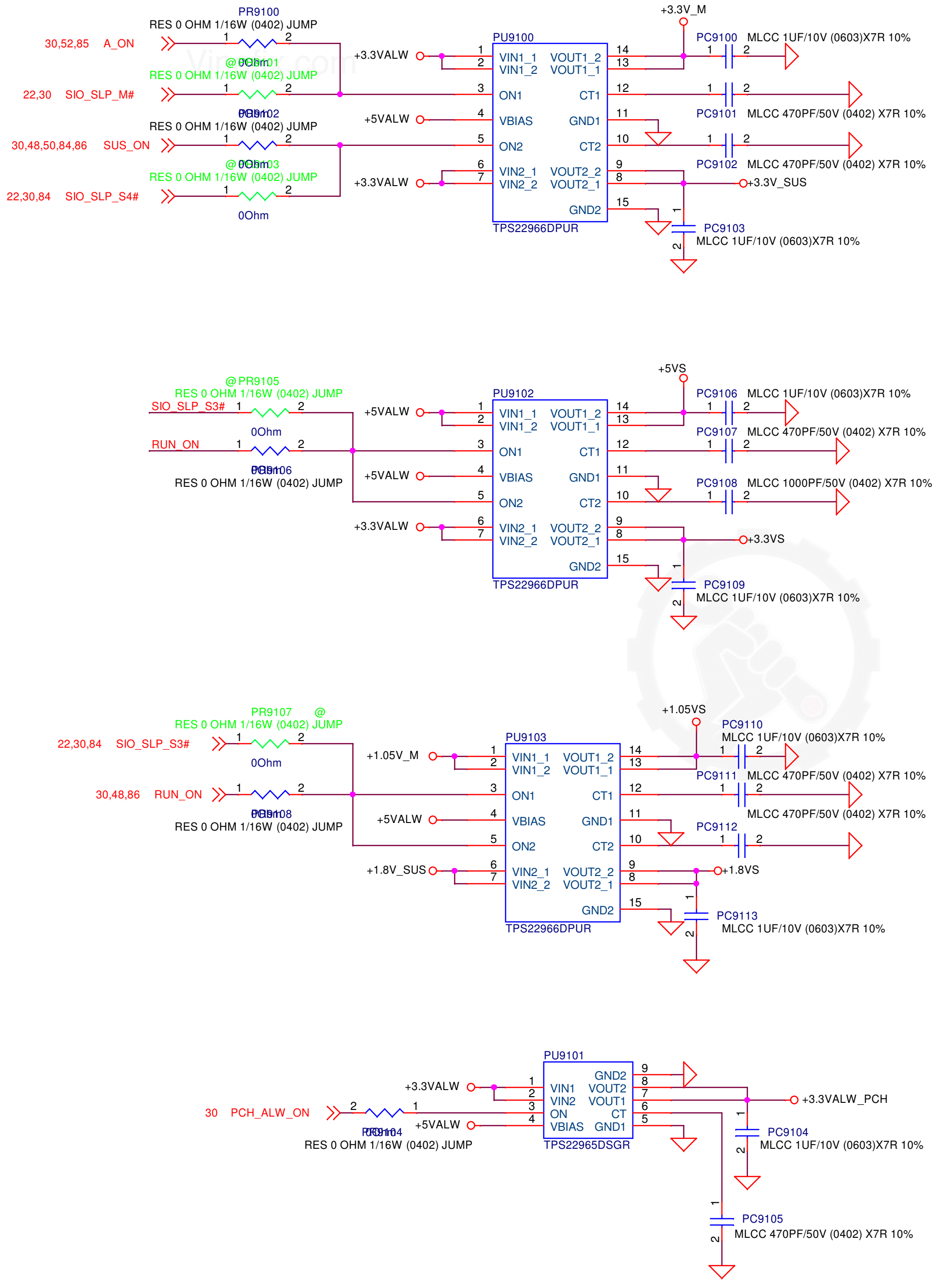
TITLE *****			
DWG NO.	CORE_B	REV.	2.0
DATE	Wednesday, May 06, 2015	SHEET	89 of 99



TITLE	POWER_LOAD SWITCH
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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TITLE	
DWG NO. CORE_B	REV. 2.0
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TITLE BLANK PAGE			
DWG NO. CORE_B		REV. 2.0	
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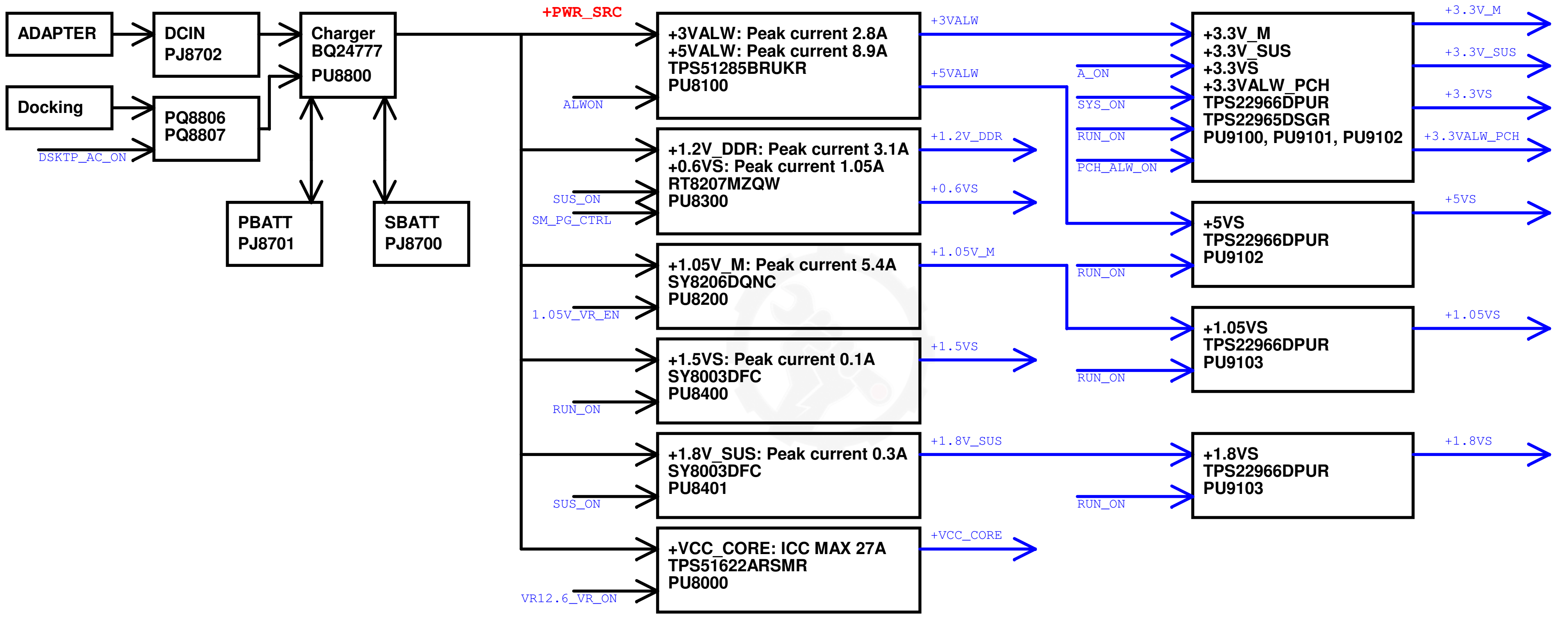
modify notice

Version	Date	Description



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TITLE POWER TREE			
DWG NO. CORE_B		REV. 2.0	
DATE Wednesday, May 06, 2015		SHEET 96	of 99

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TITLE	BLANK PAGE
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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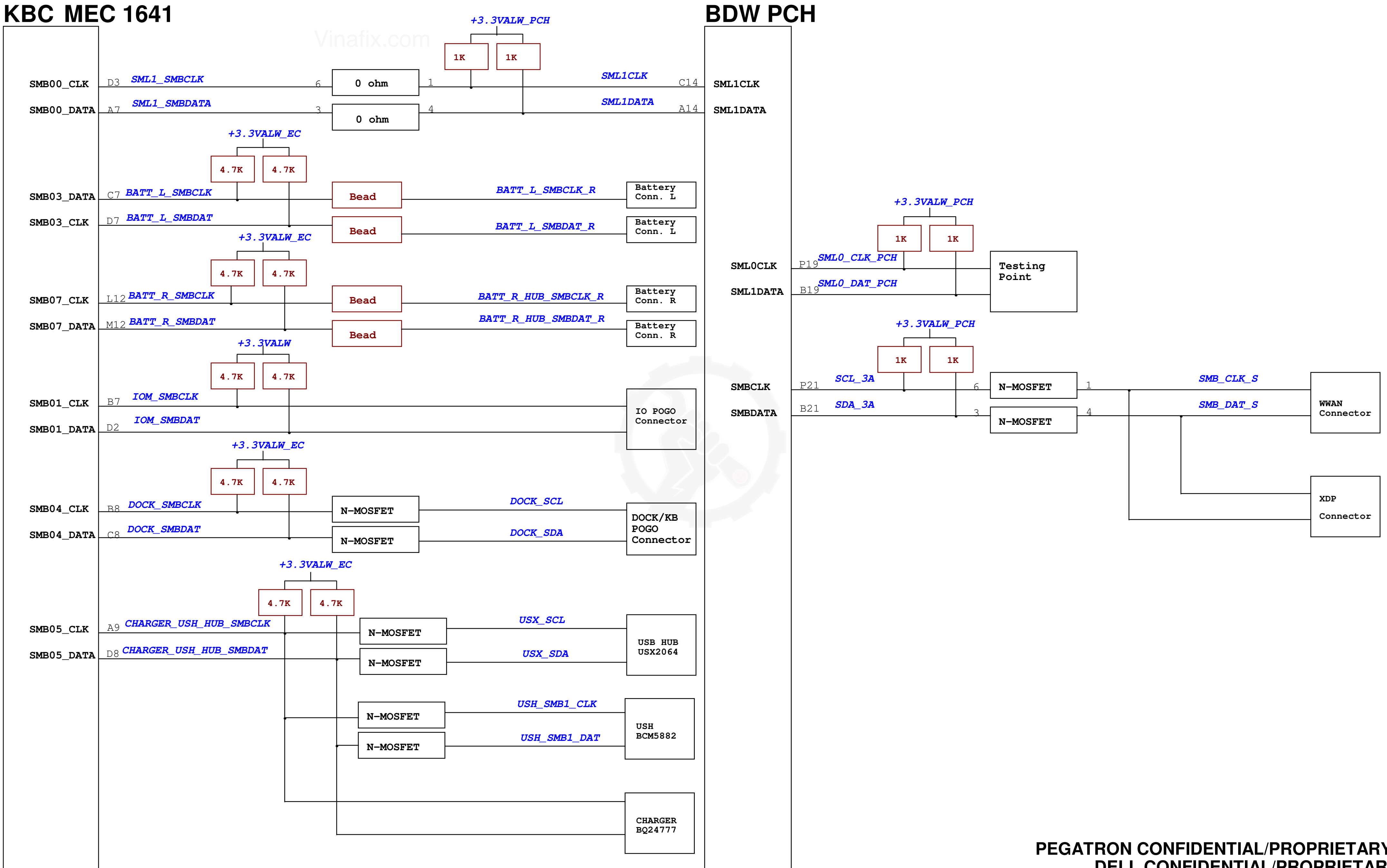
LIVINGSTONE SMBUS Block Diagram (X01)



TITLE	SMBUS & I2C
DWG NO.	CORE_B
REV.	2.0
DATE	Wednesday, May 06, 2015
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TITLE ***		
DWG NO. CORE_B		REV. 2.0
DATE Wednesday, May 06, 2015	SHEET 99 of 99	