Compal Confidential

LA-F901P Schematics Document

intel Coffee Lake S with DDR4 + CNP + AMD GPU (M17)

AIO M/B

3/13 , 2018

REV : 1.0

Security Classification	Compal Secret Data		
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Title: *Cover Page*		
Size: Custom	Document Number: LA-F901P M/B	Rev: 0.1
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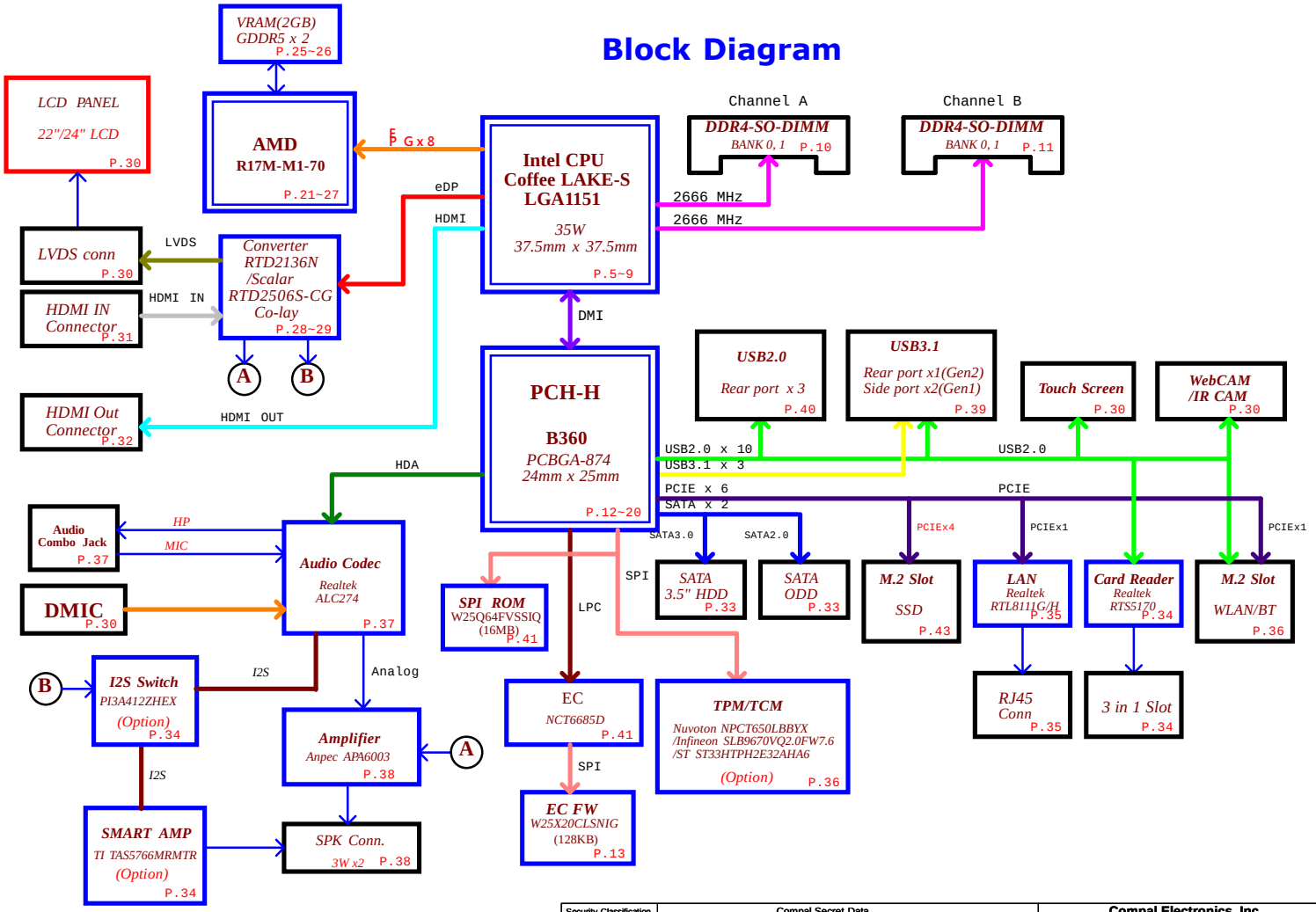
PCB Size : 169 mm x 240 mm

Block Diagram



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Title	Black Diagram
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PCIE Port Table

No.	Port	Device
5	11	NC
6	12	LAN
7	13	WLAN
8	14	NC
21	27	SSD
22	28	SSD
23	29	SSD
24	30	SSD

SATA Port Table

No.	Port	Device
1	17	NC
2	18	NC
3	19	HDD
4	20	ODD
5	21	NC
6	22	NC
7	23	NC
8	24	NC

USB2.0 Port Table

Port	Device	OC# Pin
1	USB 2.0 Rear IO Port 1	OC#0
2	USB 2.0 Rear IO Port 2	OC#1
3	USB 2.0 Rear IO Port 3	OC#1
4	USB 2.0/3.0 (Rear IO)	OC#2
5	USB 2.0/3.0 (IO/B Port 2)	OC#3
6	USB 2.0/3.0 (IO/B Port 1)	OC#3
7	Web Camera	NA
8	Card Reader	NA
9	TOUCH	NA
10	WLAN/BT	NA

USB3.0 Port Table

No.	Port	Device
1	1	NC
2	2	USB3.0 (IO Board Port 1) GEN1
3	3	USB3.0 (IO Board Port 2) GEN1
4	4	USB3.0 (Rear IO) GEN2
5	5	NC
6	6	NC

DDI Port Table

No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	NC
3	DDI3	NC

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VALW_S5	1.8V always on power rail	ON	OFF	OFF
+1.05VALW_S5	1.05V always on power rail for PCH	ON	ON	ON
+1.05V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_VCCSA_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+VCC_CORE_S0	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SKU ID(Project) Table

SKU (UMA&DIS)	V4/V5 EVT BOM Configure Table
431AAE38L01 (UMA) Converter	
431AAE38L02 (DIS) Samsung 2G Converter	
431AAE38L03 (DIS) Micron 2G Scalar	

SKU ID(Project) Table

SKU (UMA&DIS)	C4/C5 EVT BOM Configure Table
431A7C38L51 (DIS) Hynix 2G Scalar	

BOM Structure Table

BOM Structure	BTO Item

EC SM Bus0 Address

Device	Address	HEX
Converter RTD-2136N	1001-0100xb	94
GPU	1000-0010xb	82
PCH	1001-0000xb	90
Thermal	1001-1010xb	9A

EC SM Bus2 Address

Device	Address	HEX
Scalar RTD-2506S	x	x
LCD Backlight	0110-0010xb	62
TI TAS5766MRMTR	1001-1010xb	9A

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

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Title: Notes List

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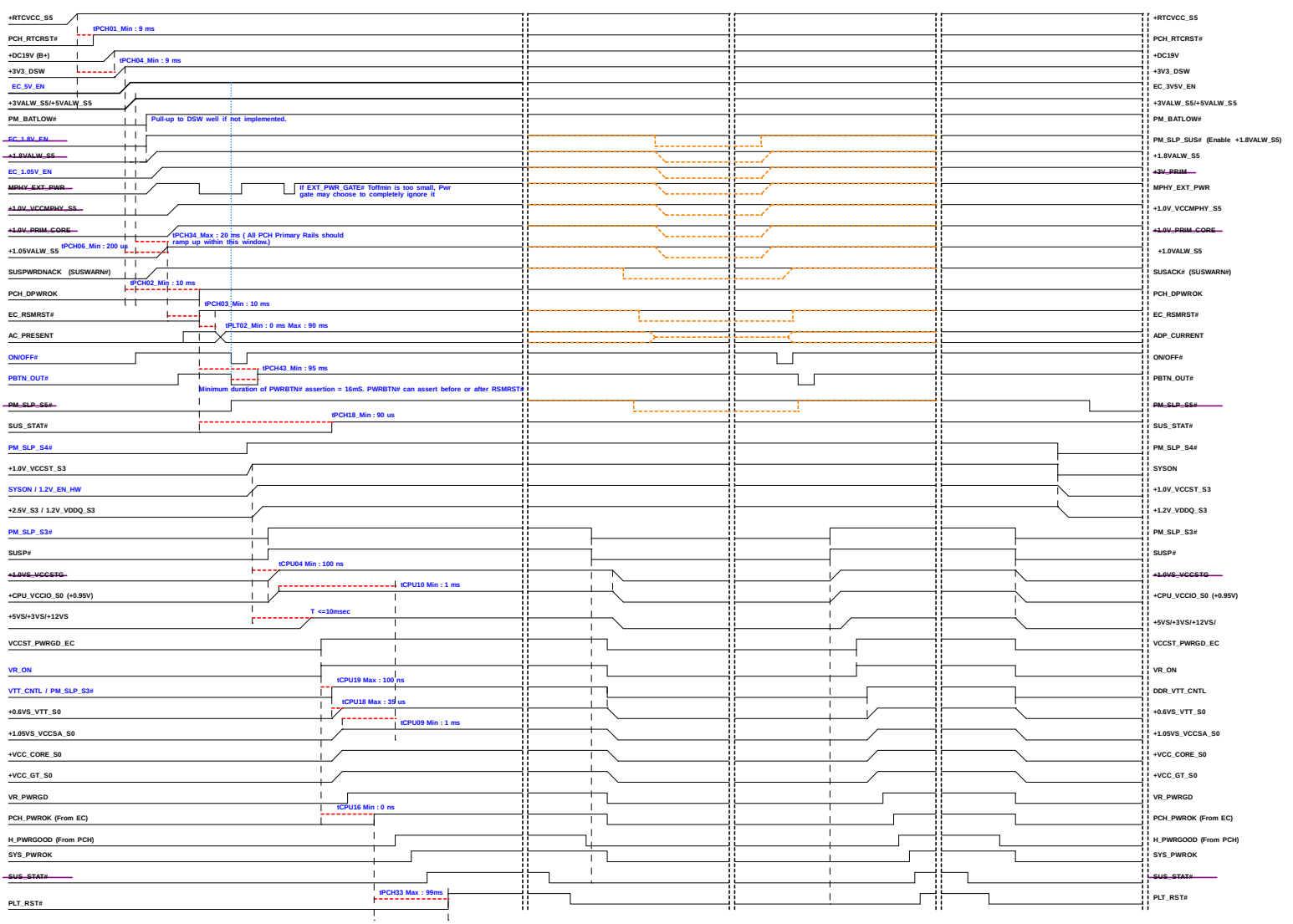
Power Sequence_SKL-S [Deep Sx Platform]



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			Size: C — Document Number: LA-F901P M/B — Rev: 0.1
			Date: Tuesday, March 11, 2014 — Sheet 6 of 67

+VCC_CORE

VGATE

SYS_PWROK

PCH_PLTRST#

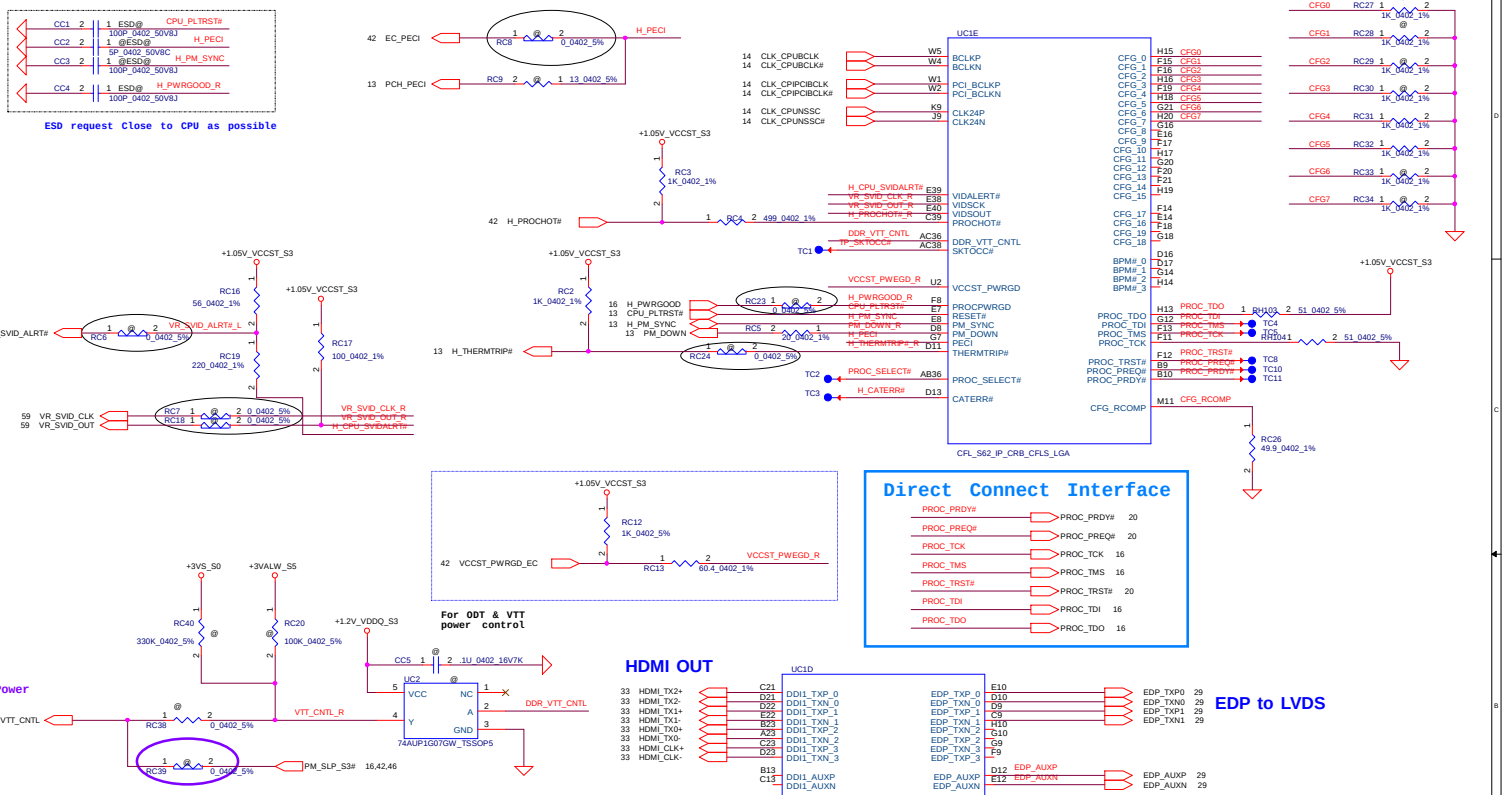

Table 7-1. Mapping of HDMI* Signals for DDI Ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

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Title	Skylake JTAG/XDP/DDI
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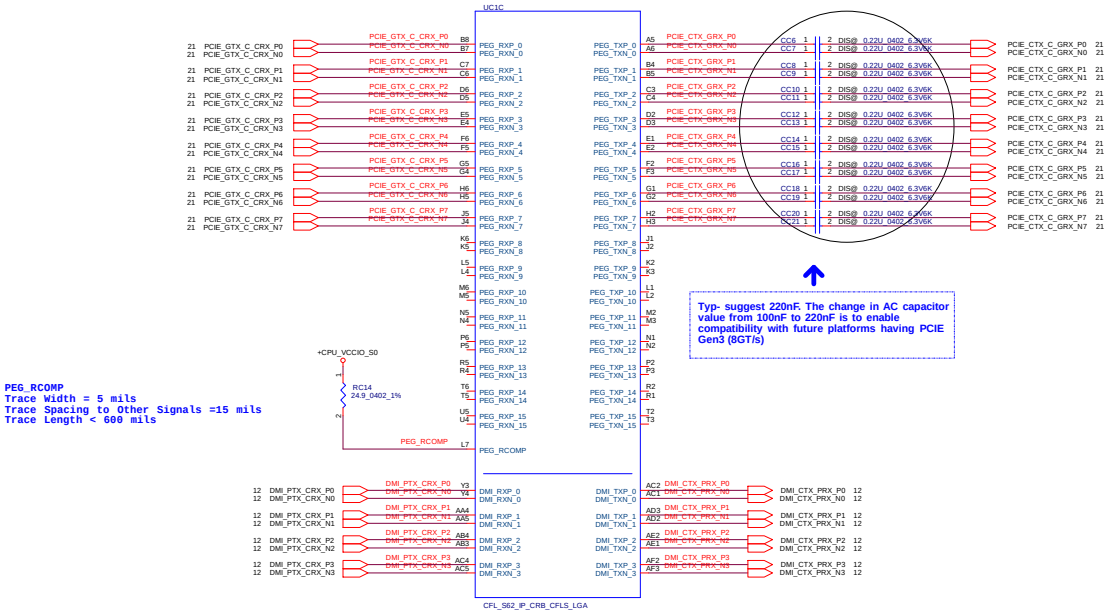

PEG_RCOMP
Trace Width = 5 mils
Trace Spacing to Other Signals =15 mils
Trace Length < 600 mils

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Compal Electronics, Inc.

Title: *Skylake DMI/PEG/FDI*

Size	Document Number	Rev
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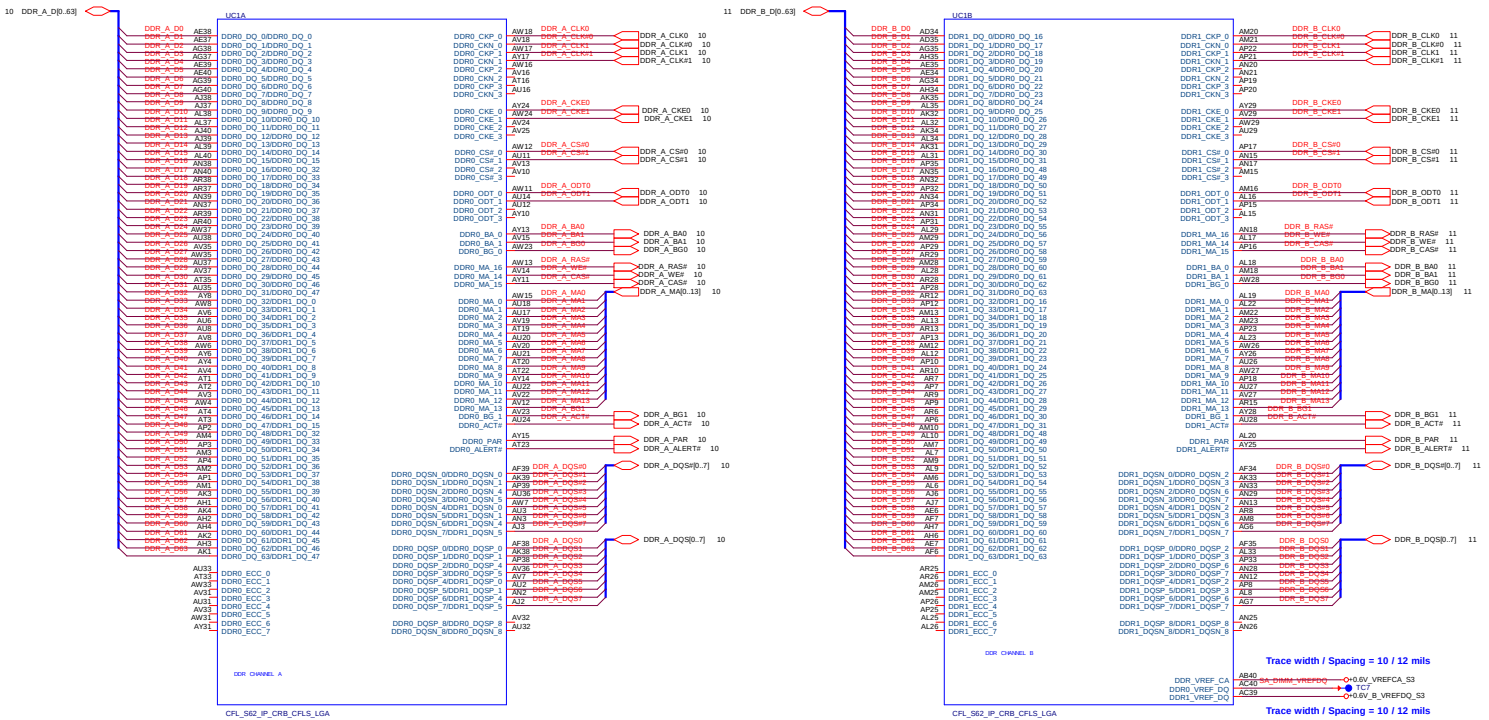

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Issued Date	2015/12/25	Deciphered Date	2013/09/01

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Title: ***Skylake DDR4***

Size	Document Number	Rev
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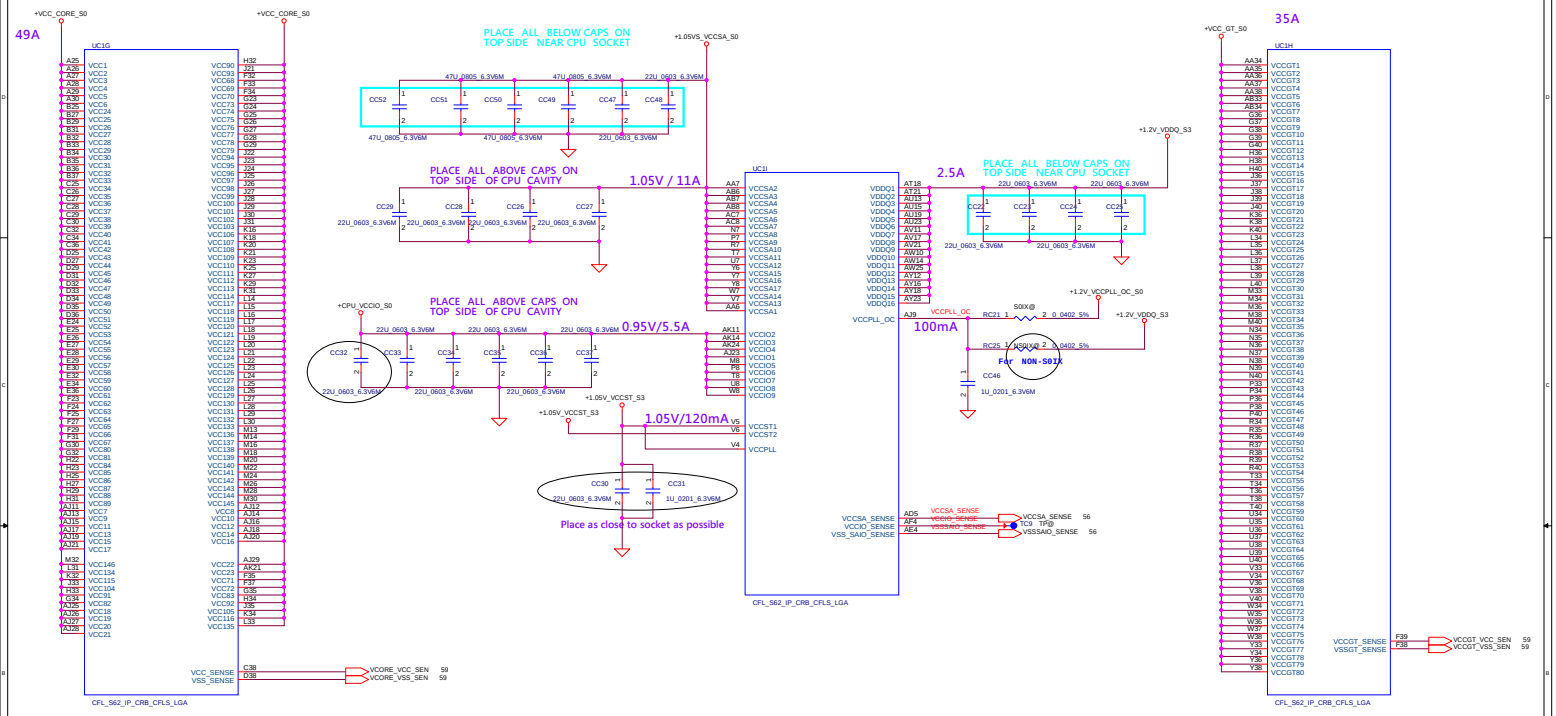

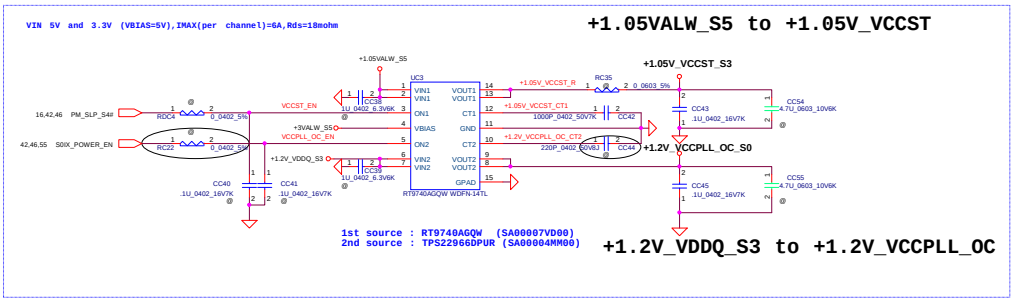

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Title: Skylake POWER

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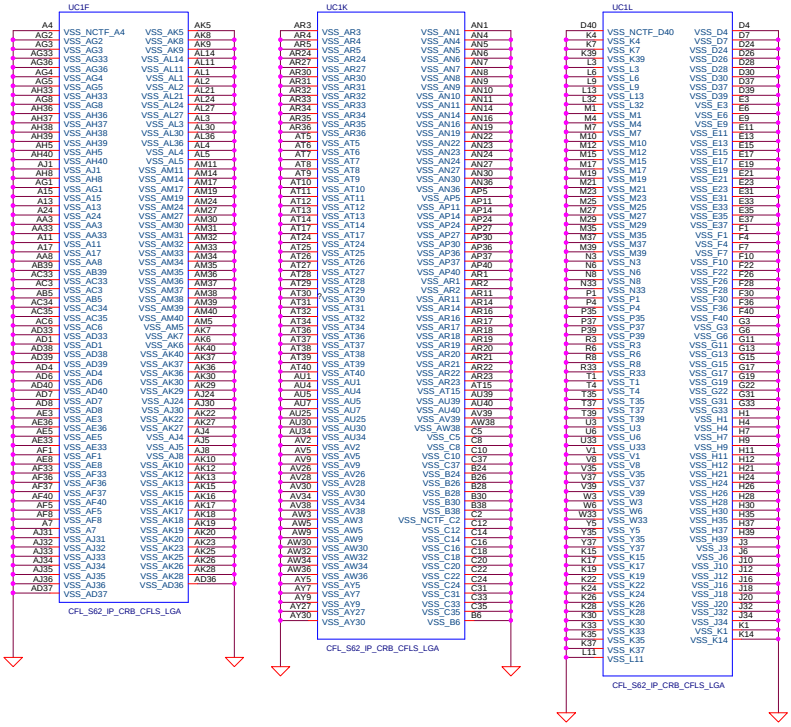

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Title: ***Skylake GND/RSVD***

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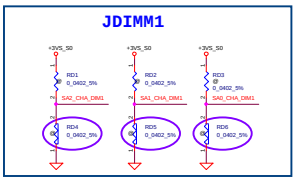
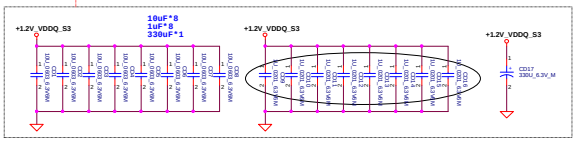
INTERLEAVE CHANNEL-A



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

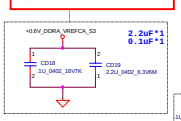
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

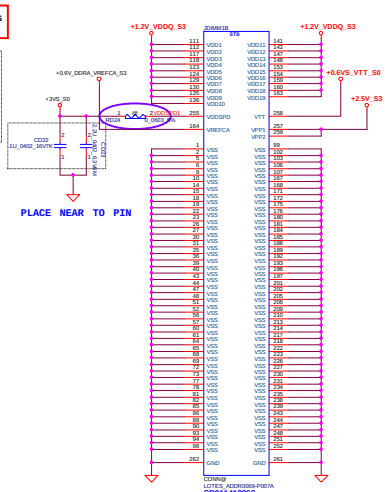
Layout Note:
Place near JDIMM1



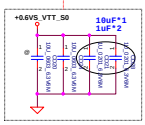
(8.0 mm) STD

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

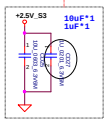


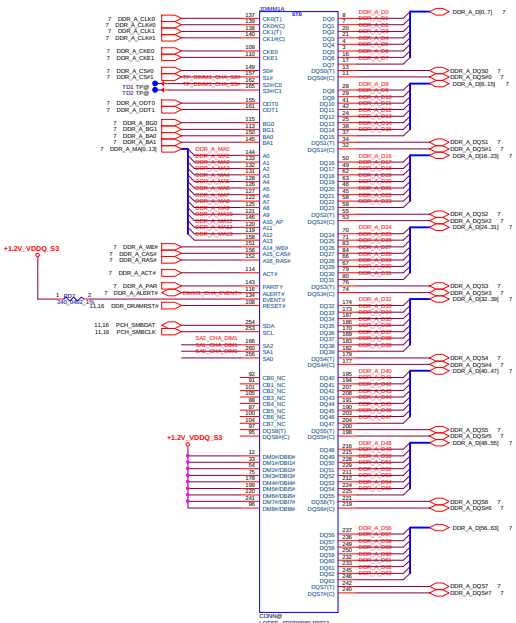


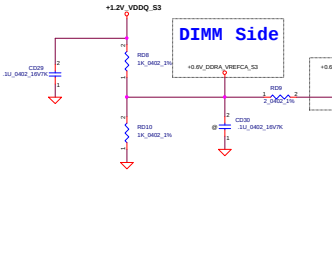
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1







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			Title: DDR4_DIMMA
			Size: Custom; Document Number: LA-F901P M/B; Rev: 0.1
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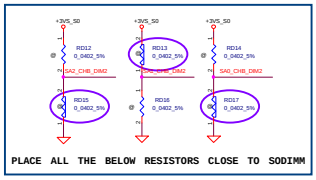
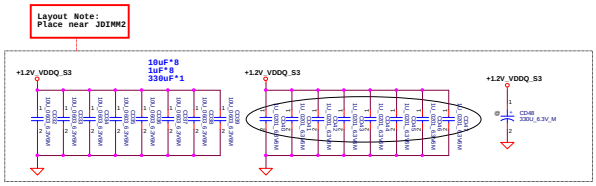
INTERLEAVE
CHANNEL-B

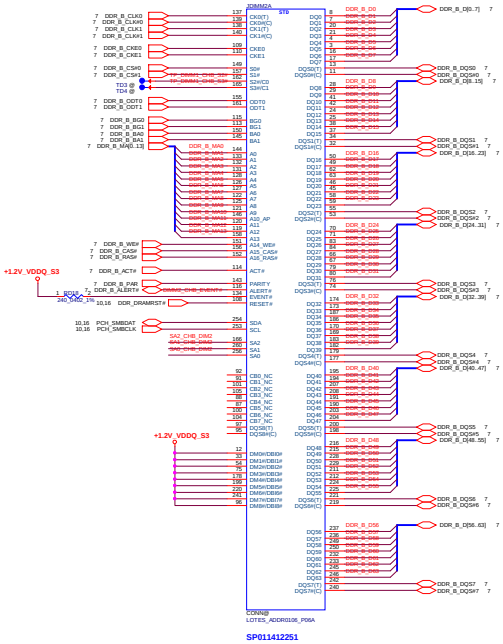


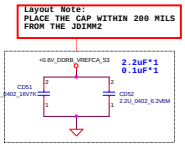
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

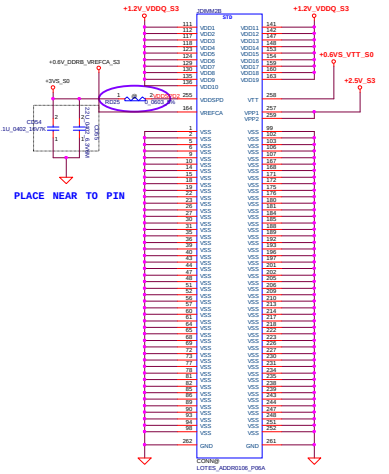
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

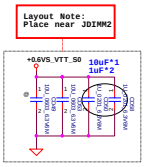


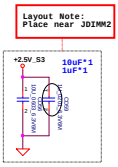
(4.0 mm) STD

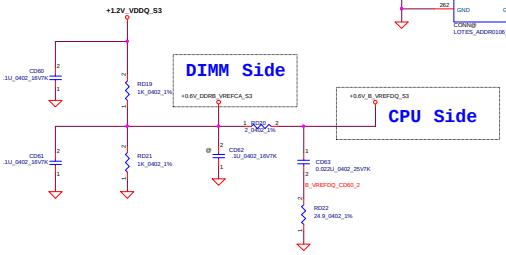


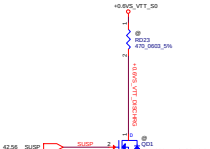












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Issued Date	2015/12/25	Deciphered Date	2015/12/31
Title	DDR4 DIMMB		
Size	Document Number		Rev
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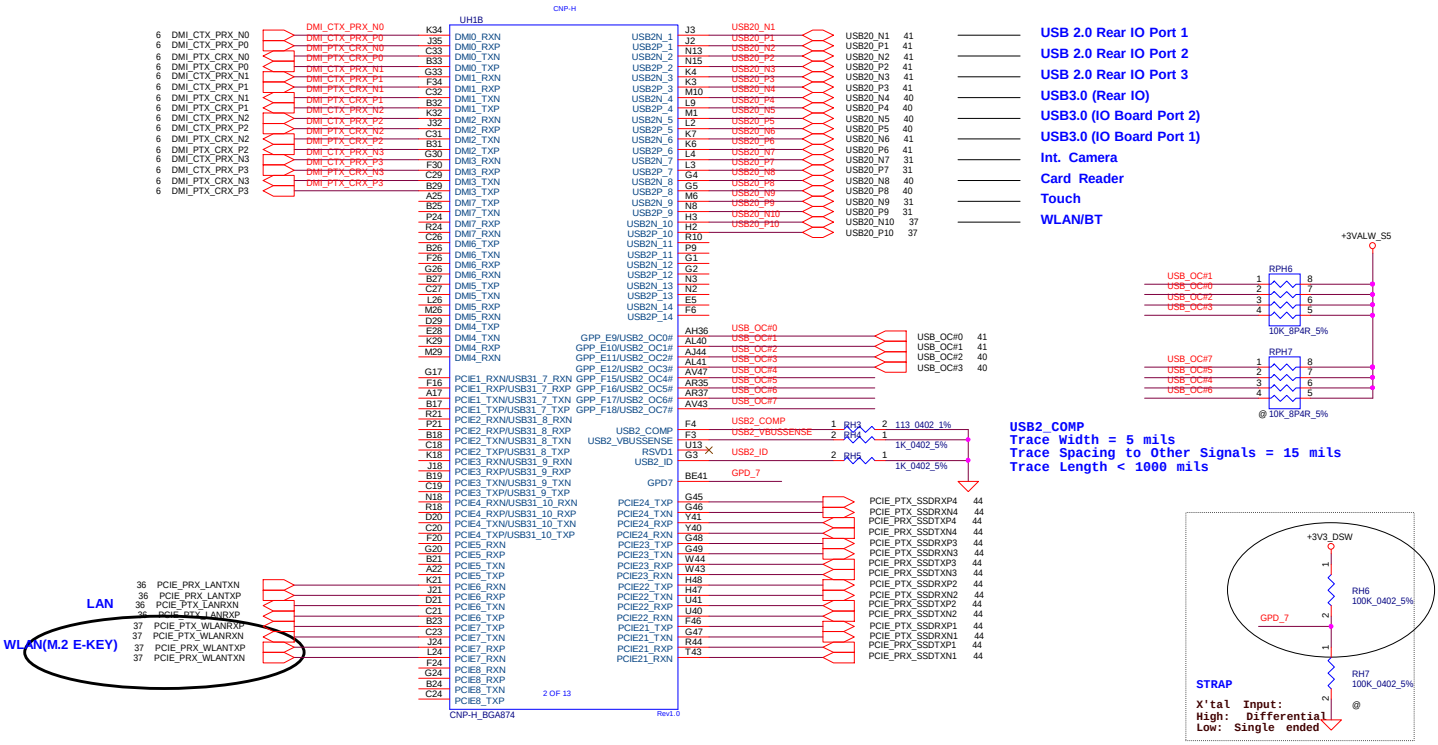

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Compal Electronics, Inc.

Title: *PCH_DMI/USB2/PCIE*

Size	Document Number	Rev
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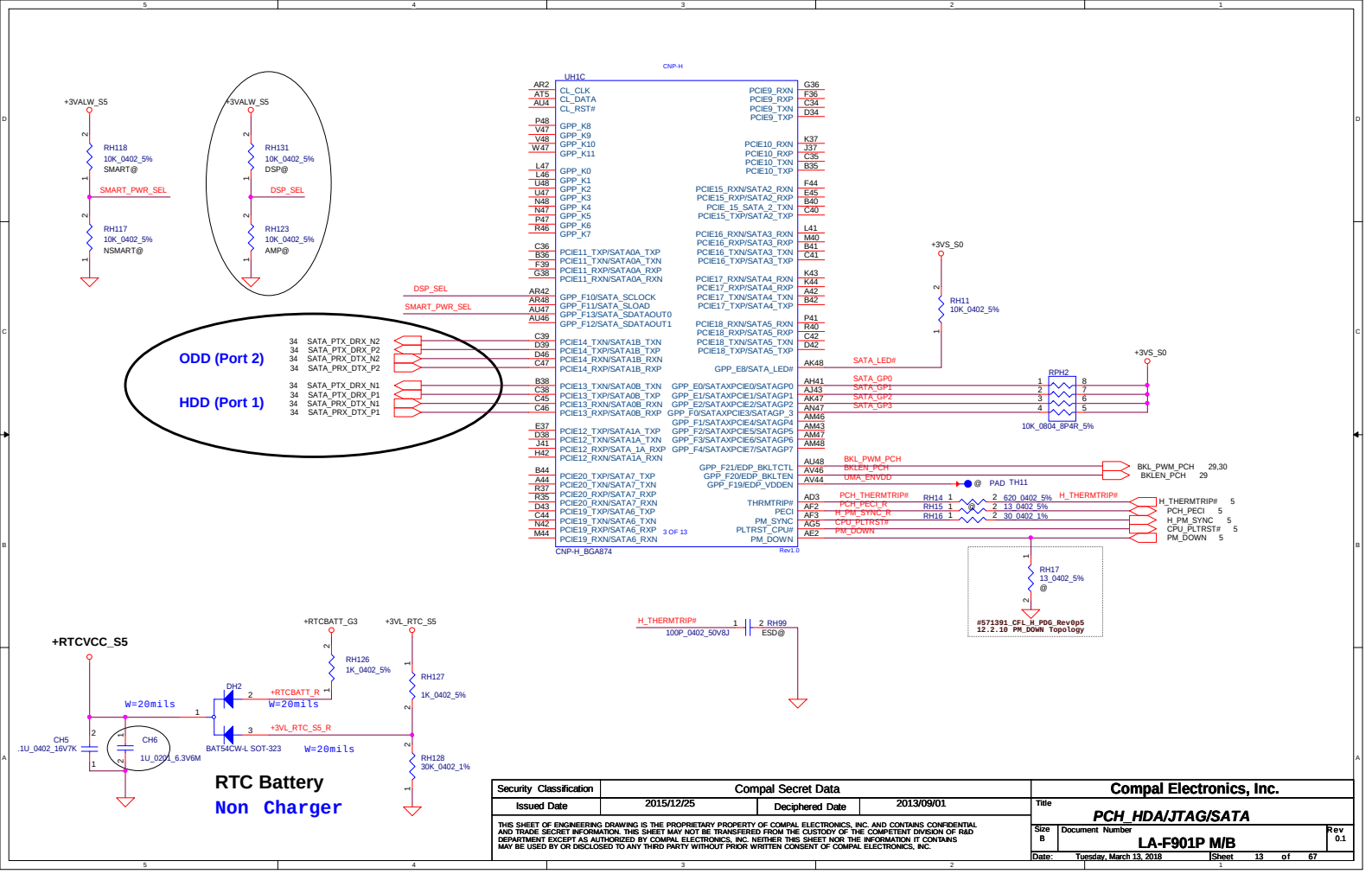

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Issued Date	2015/12/25	Deciphered Date	2013/09/01

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Title: *PCH_HDA/JTAG/SATA*

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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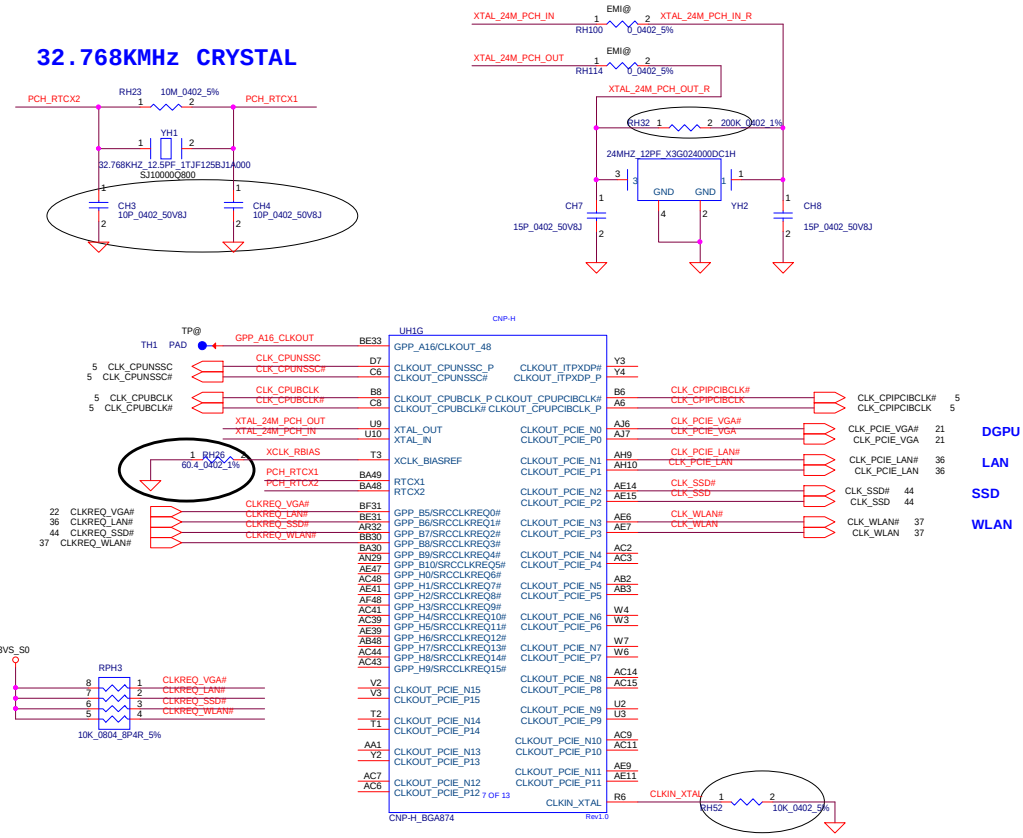

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Issued Date	2015/12/25	Deciphered Date 2013/09/01	Title: PCH_CLK\LPC\SPI\SMBUS
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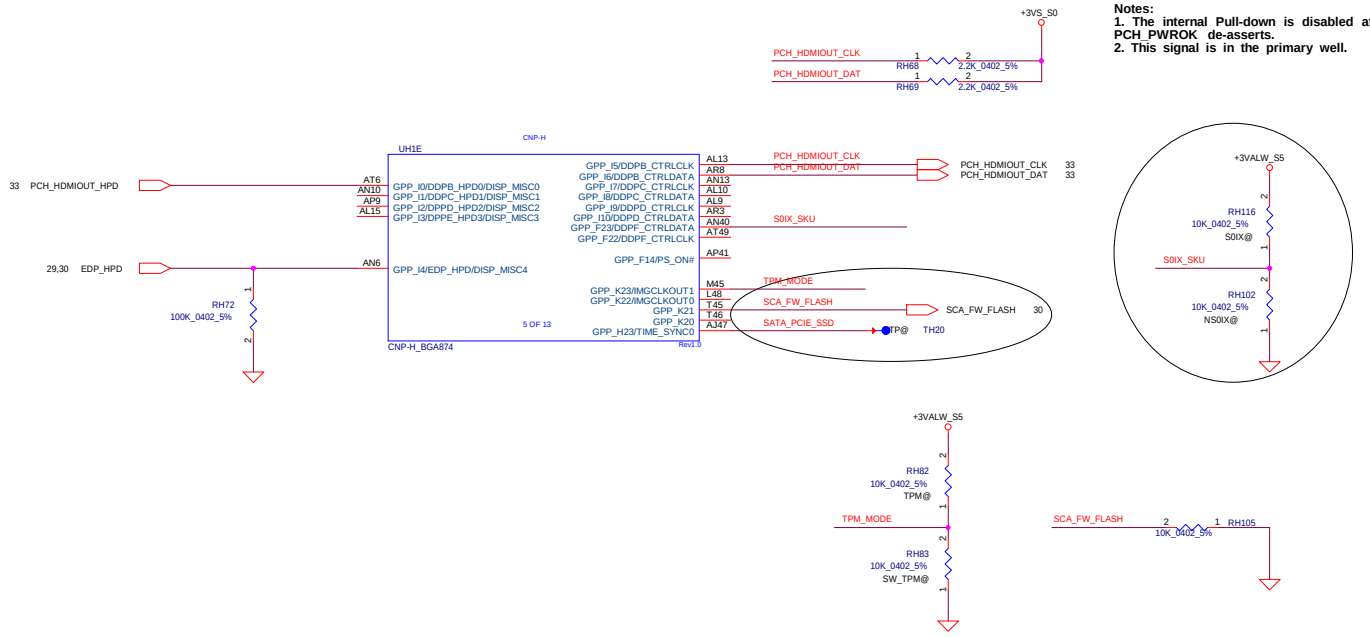
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***PCH_CRT/DDC***

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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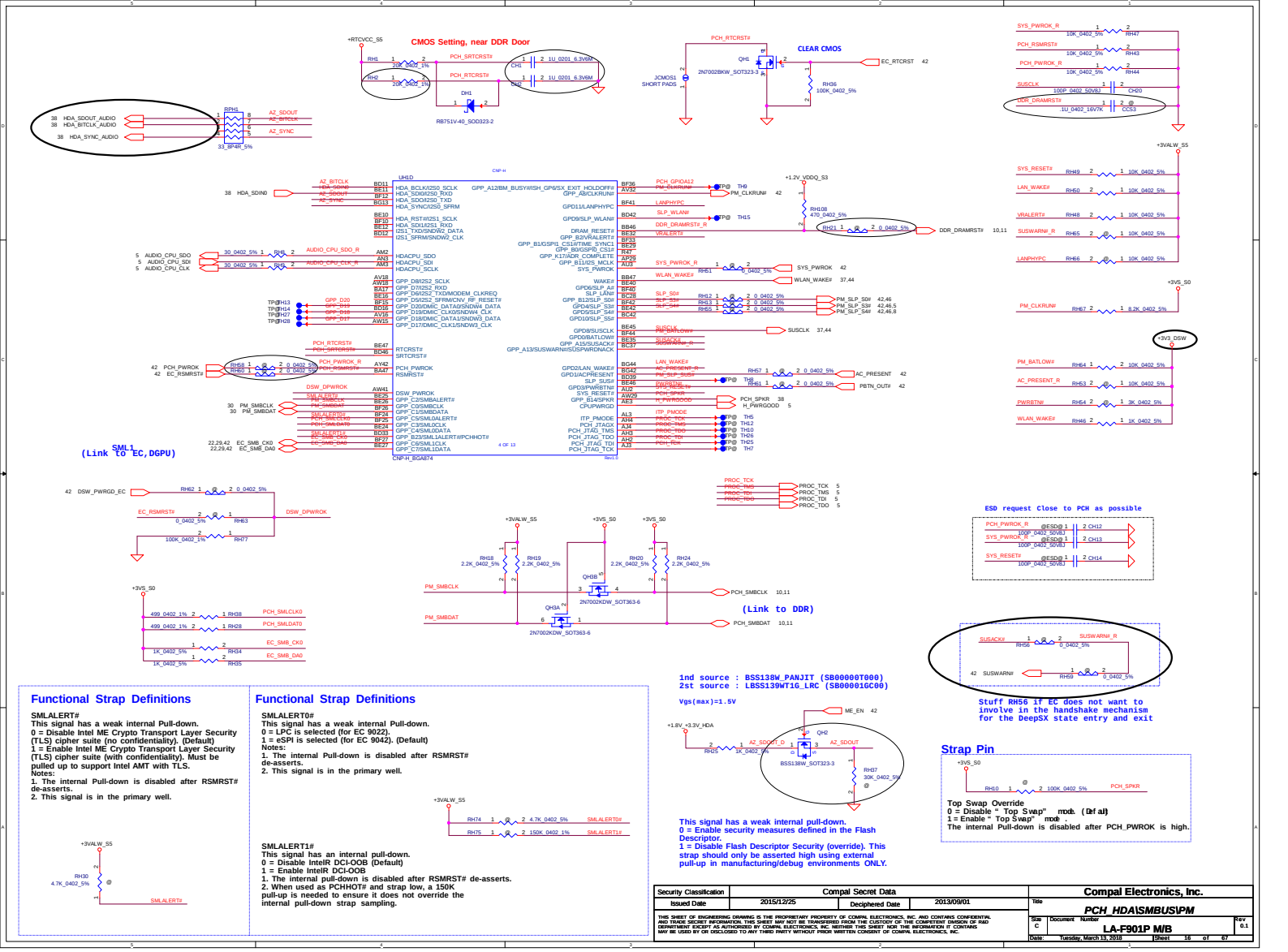

Functional Strap Definitions

SMLALERT#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Functional Strap Definitions

SMLALERT0#
This signal has a weak internal Pull-down.
0 = LPC is selected (for EC 9022).
1 = eSPI is selected (for EC 9042). (Default)
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

SMLALERT1#
This signal has an internal pull-down.
0 = Disable Intel® DCI-OOB (Default)
1 = Enable Intel® DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

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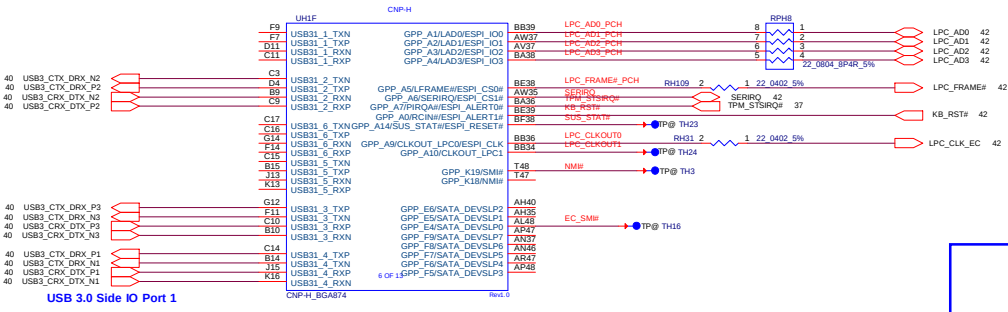
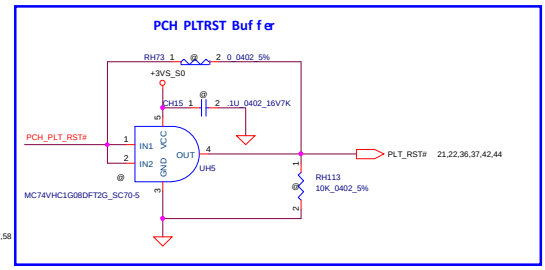
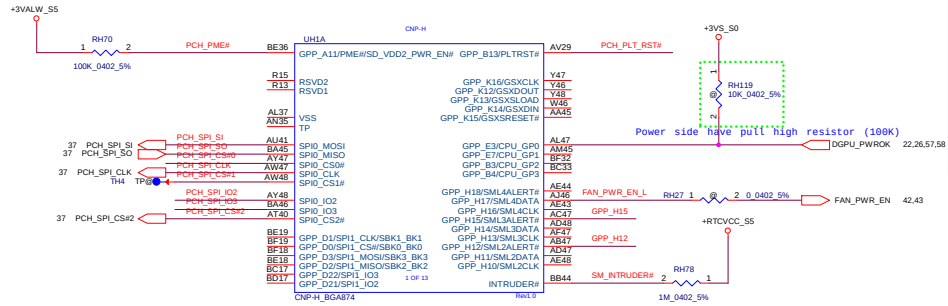
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Title	PCH_HDA\SMBUS\PM		
Size C	Document Number LA-F901P M/B		Rev 0.1
Date: Tuesday, March 13, 2018	Sheet 16 of 67		

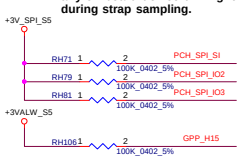






Functional Strap Definitions

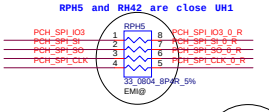
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

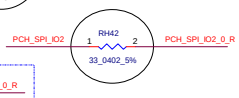


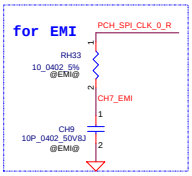
Functional Strap Definitions

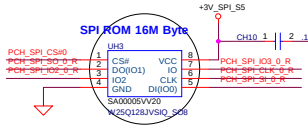
SML2ALERT#
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to ' 0 if the eSPI or LPC strap is configured to ' 0

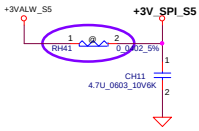
RPH5 and RH42 are close UH1











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Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: **PCH_PCI-E/USB**

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1
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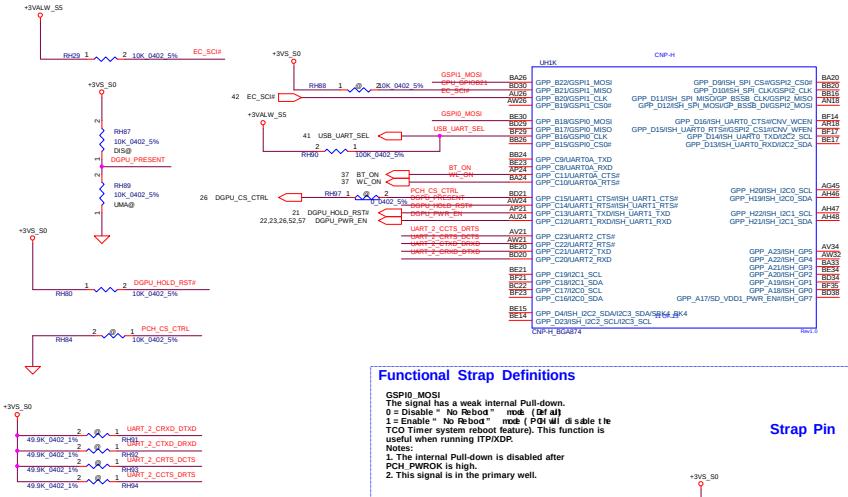

Functional Strap Definitions

GSPI0_MOSI
The signal has a weak internal Pull-down.
0 = Disable " No Reboot " mode. (Default)
1 = Enable " No Reboot " mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

GSPI1_MOSI
This Signal has a weak internal Pull-down.
0: SPI (Default)
1: LPC
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

Strap Pin

Intel® 300 Series Chipset Preliminary HSIO Lane Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
USB 3.1 Gen 1 / Gen 2 #1	USB 3.1 Gen 1 / Gen 2 #2	USB 3.1 Gen 1 / Gen 2 #3	USB 3.1 Gen 1 / Gen 2 #4	USB 3.1 Gen 1 / Gen 2 #5	USB 3.1 Gen 1 / Gen 2 #6	USB 3.1 Gen 1 #7 / PCIe 3.0 #1	USB 3.1 Gen 1 #8 / PCIe 3.0 #2	USB 3.1 Gen 1 #9 / PCIe 3.0 #3	USB 3.1 Gen 1 #10 / PCIe 3.0 #4	PCIe 3.0 #5 / GbE (LAN)	PCIe 3.0 #6	PCIe 3.0 #7	PCIe 3.0 #8	PCIe 3.0 #9 / GbE (LAN)	PCIe 3.0 #10	PCIe 3.0 #11 / SATA #0	PCIe 3.0 #12 / SATA #1 / GbE (LAN)	PCIe 3.0 #13 / SATA #0 / GbE (LAN)	PCIe 3.0 #14 / SATA #1	PCIe 3.0 #15 / SATA #2	PCIe 3.0 #16 / SATA #3	PCIe 3.0 #17 / SATA #4	PCIe 3.0 #18 / SATA #5	PCIe 3.0 #19	PCIe 3.0 #20	PCIe 3.0 #21	PCIe 3.0 #22	PCIe 3.0 #23	PCIe 3.0 #24
						x4				x4				x4				x4				x4				x4			
						x2		x2		x2		x2		x2				x2	x2			x2	x2			x2		X2	
						No Remapping				No Remapping				Intel® RST for PCIe Storage				No Remapping				Intel® RST for PCIe Storage				Intel® RST for PCIe Storage			

SKU

H310	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen1	N/A	N/A	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B360	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1	USB3.1 Gen 1	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe	PCIe	PCIe

SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14

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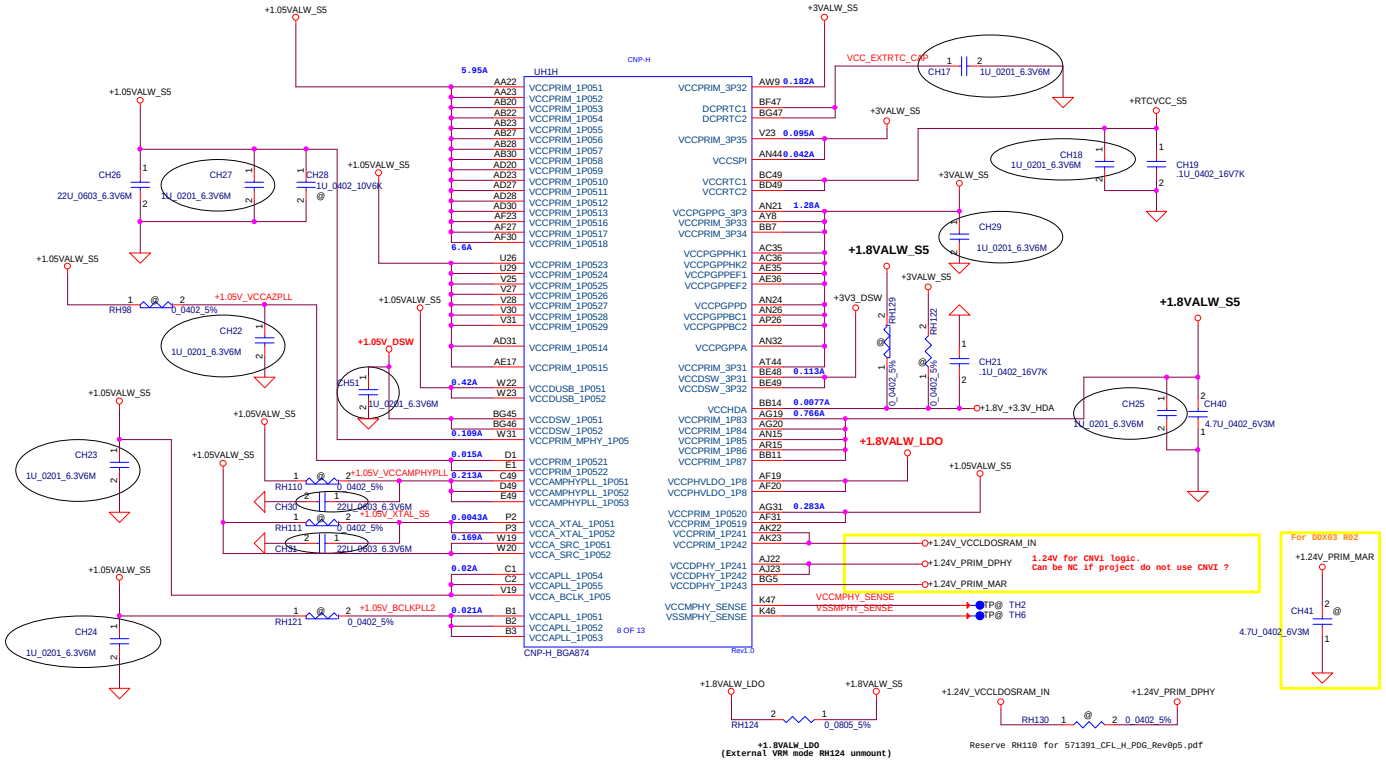
			Size: C / Document Number: LA-F901P M/B / Rev: 0.1
			Date: Tuesday, March 13, 2018 / Sheet 18 of 67

Need to confirm the decoupling and Power requirment



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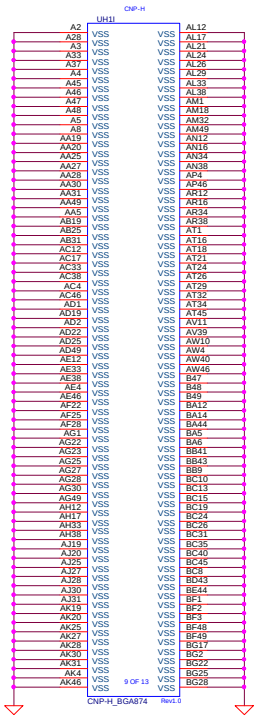
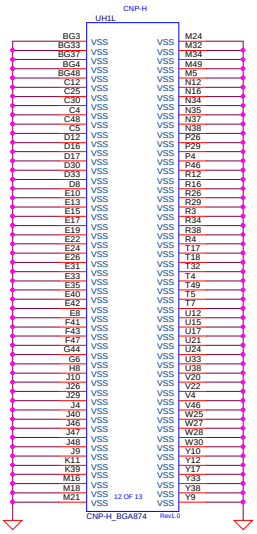
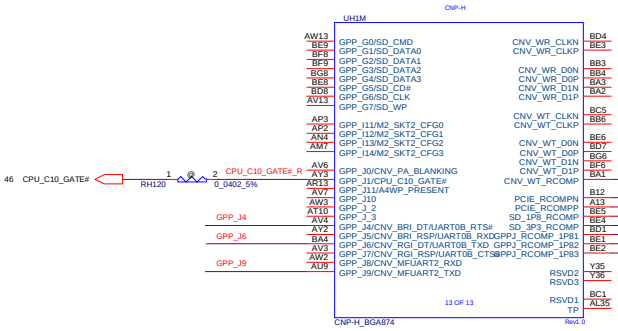
Title: PCH_POWER

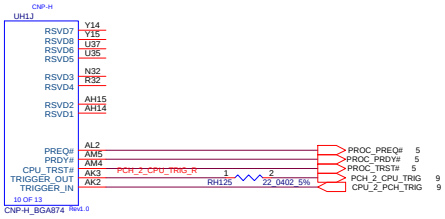
Size	Document Number	Rev
B	LA-F901P M/B	0.1

Date: Tuesday, March 13, 2018 Sheet 19 of 67









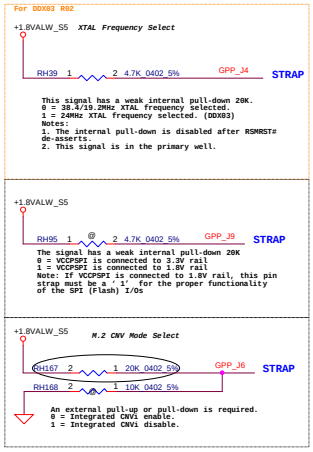


Table 18-1. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

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Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***PCH_GND & CNVi***

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1
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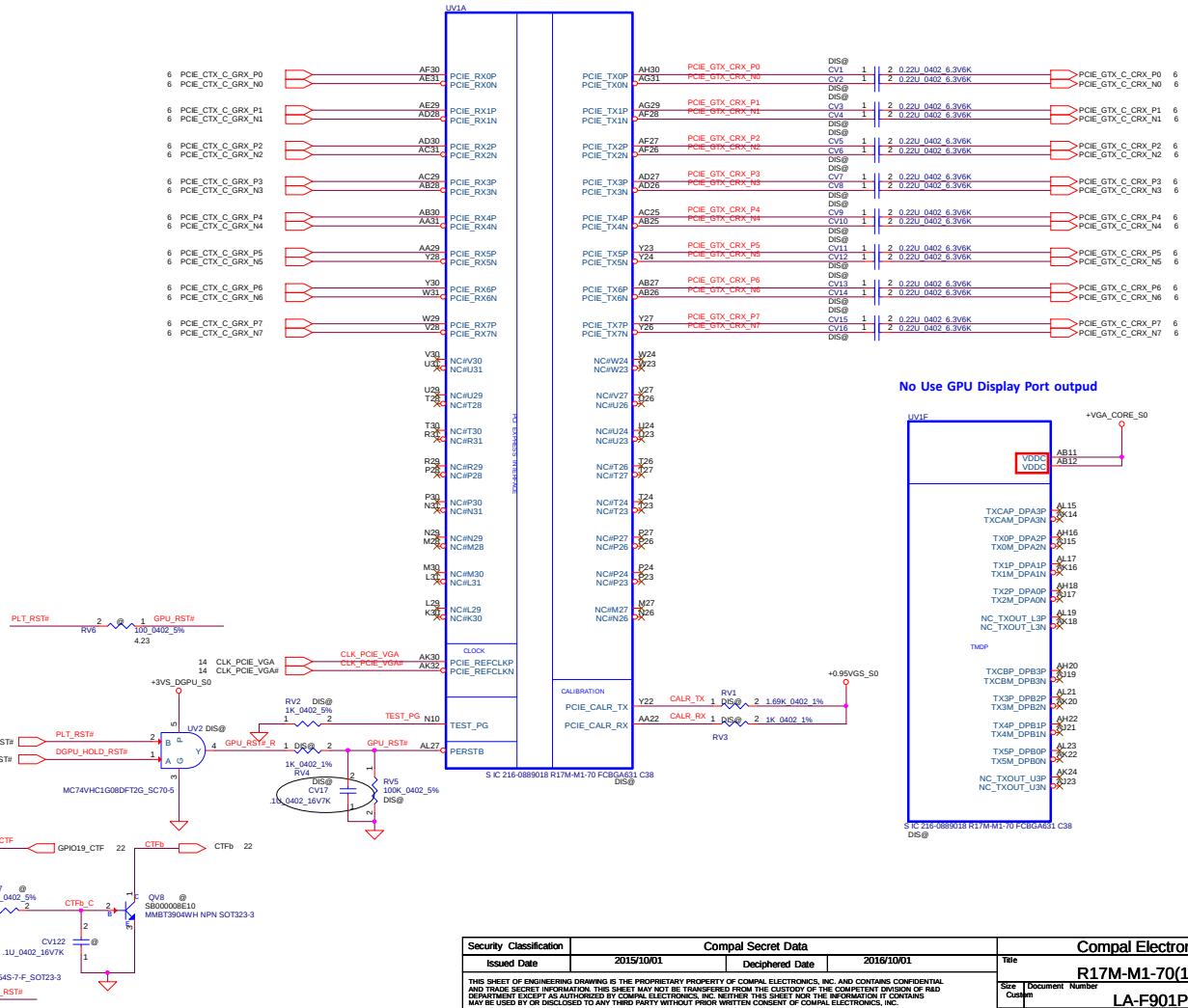

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Compal Electronics, Inc.

Title: R17M-M1-70(1/6) PCIE/DP

Size	Document Number	Rev
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Meso/M16M-R16M-M2-50

GPIO_11, 12, and 13 are added back.

The following balls cease to work as GPIOs or designated functional pins, and become **VDDC**:

- GPIO_1
- GPIO_2
- GPIO_14_HPD2
- GPIO_18_HPD3

The following ball ceases to work as a GPIO or designated functional pin, and becomes **NC**:

- GPIO_7_BLON

"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36.

The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:

- VARY_BL (AB11)
- DIGON (AB12)
- GENERICA (AB13)
- GENERICC (W8)
- DDC2CLK (AC11)
- DDC2DATA (AC13)
- HPD1 (AC14)
- GPIO_1 (U10)
- GPIO_2 (T10)
- GPIO_18 (W10)
- GPIO_14_HPD2 (Y9)

Exo/R16M-M1-30

The following balls cease to work as GPIOs or designated functional pins, and become **NC**:

- GPIO_1
- GPIO_2
- GPIO_7_BLON
- GPIO_13
- GPIO_12
- GPIO_13
- GPIO_14_HPD2
- GPIO_18_HPD3

"Jet"/"Sun" has a total of 25 VDDC balls.

The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".

10/26 Modify

EC Side pull high at page 16

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

When PS_2 bit 3=0, PS_0 bits [3:1] define the size of the Primary Memory Aperture as per table opposite

Setting Memory Aperture Size

PS_0[3] romddf g_2	PS_0[2] romddf g_1	PS_0[1] romddf cg_0	Memory Aperture Size
0	0	0	128 MB
0	0	1	256 MB
0	1	0	64 MB
0	1	1	Reserved
1	0	0	512 MB-Not Supported
1	0	1	1 GB-Not Supported
1	1	0	2 GB-Not Supported
1	1	1	4 GB-Not Supported

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 00/25

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

MLPS MEMORY ID Setting:

Board Config[2:0]	Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID [2:0]					
0	000	Samsung gDDR5	128Mx32 2PCS	1GB	K4G41325FB-HC28	SA00009TT40
1	001	Hynix gDDR5	128Mx32 2PCS	1GB	H5GC4H24AJR-T2C	SA00008HQ00
2	010	Micron gDDR5	256Mx32 2PCS	2GB	MT51J256M32HF-70:A	SA00009TV00
3	011	Samsung gDDR5	256Mx32 2PCS	2GB	K4G80325FB-HC28	SA00009ZD10
4	100	Hynix gDDR5	256Mx32 3PCS	2GB	H5GC8H24MJR-R0C	SA00009U100

X7668038L01 : RV28 = NC , RV22 = 4.75K
X7668038L02 : RV28 = 8.45K , RV22 = 2K
X7668038L03 : RV28 = 4.53K , RV22 = 2K
X7668038L04 : RV28 = 6.98K , RV22 = 4.99K

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

ZZZ4 Hynix 2G HSG@ Part Number = SA00009U120
ZZZ5 Samsung 2G S2G@ Part Number = SA00009ZD20
ZZZ6 Micron 2G M2G@ Part Number = SA00009TV30

Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R17M-M1-70(2/6) MSIC

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

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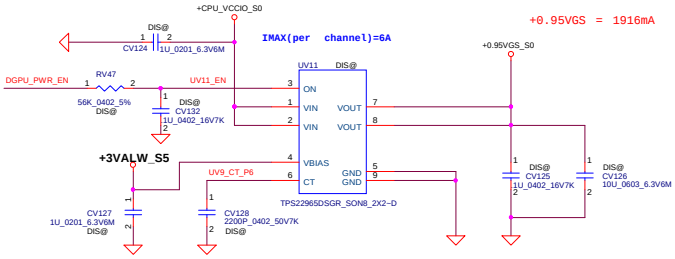
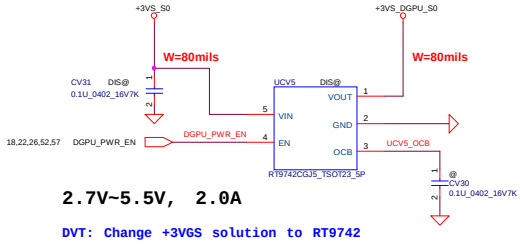
+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch



1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X500)

+3VALW to +3VGS

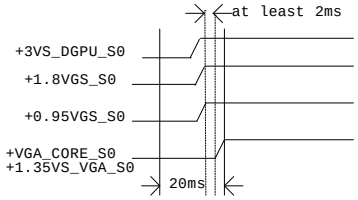


2.7V~5.5V, 2.0A

DVT: Change +3VGS solution to RT9742

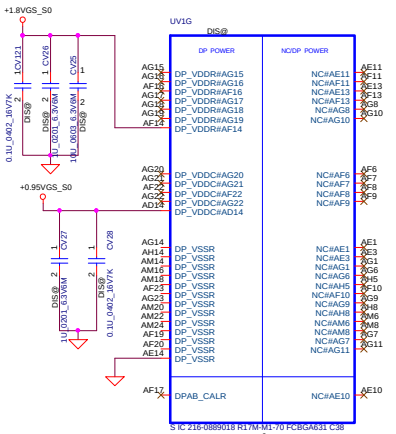
DGPU Power Sequence

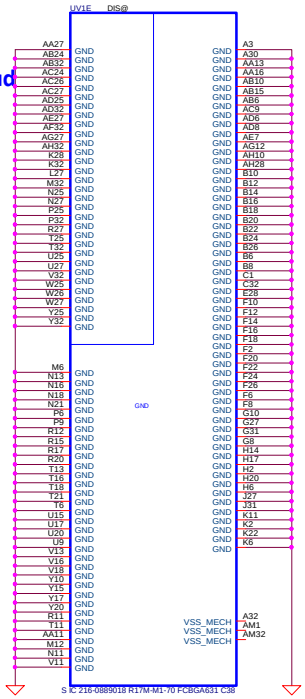
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

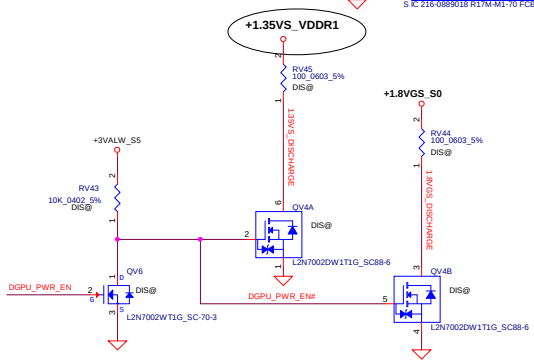


1.the 3.3-V rail ramp up first.
2.the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up

No Use GPU Display Port outpud







Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R17M-M1-70 (3/6) PWR/GND

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

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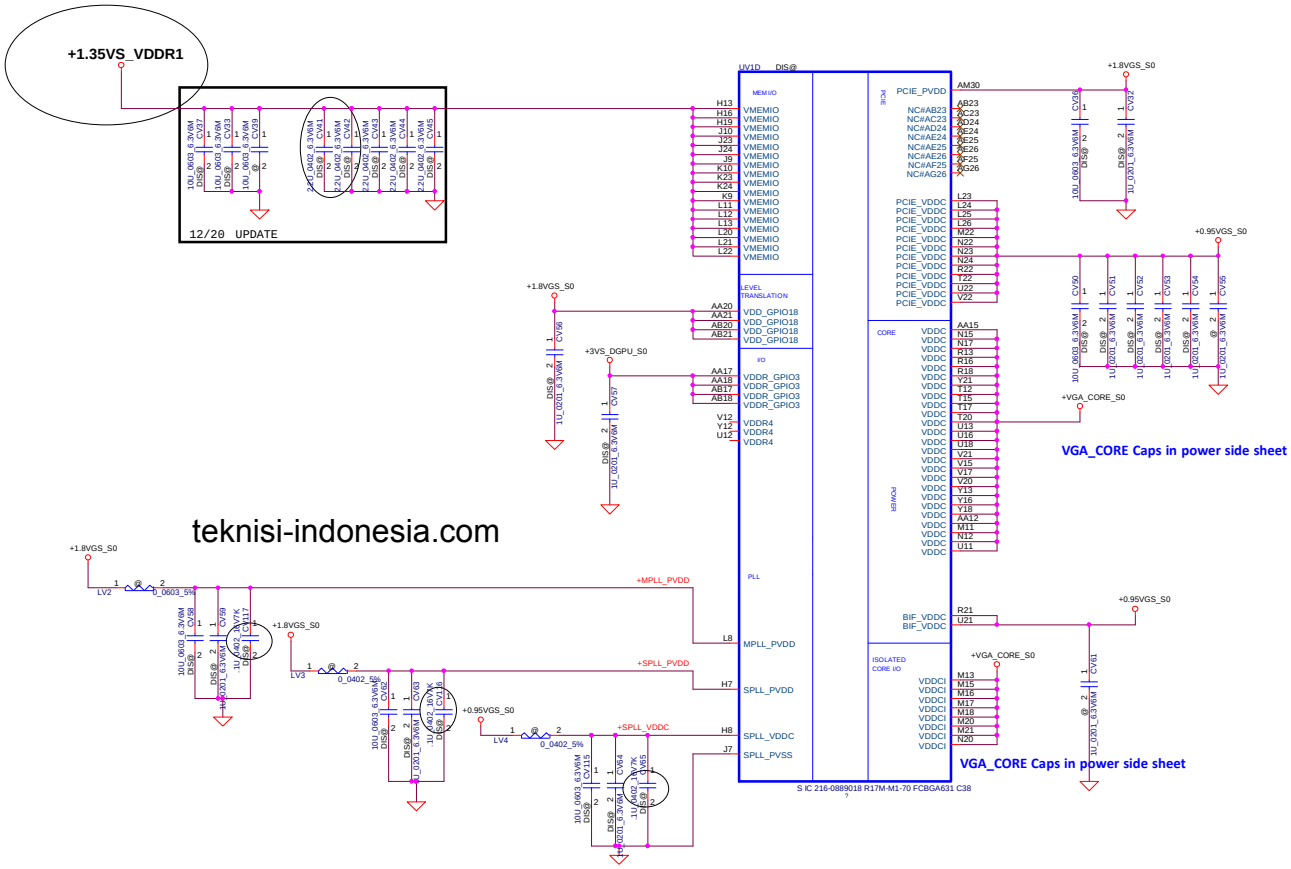

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Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R17M-M1-70(4/6) PWR

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

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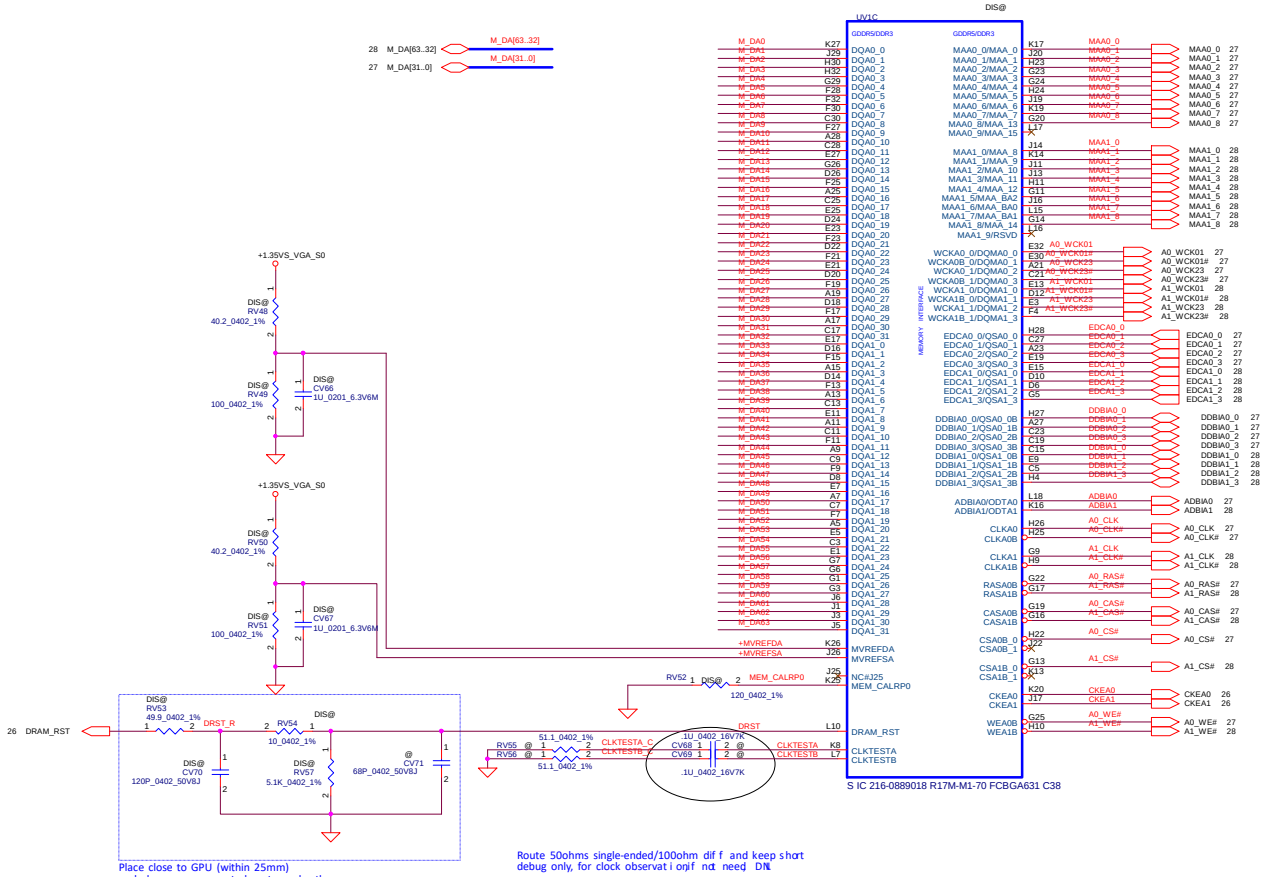

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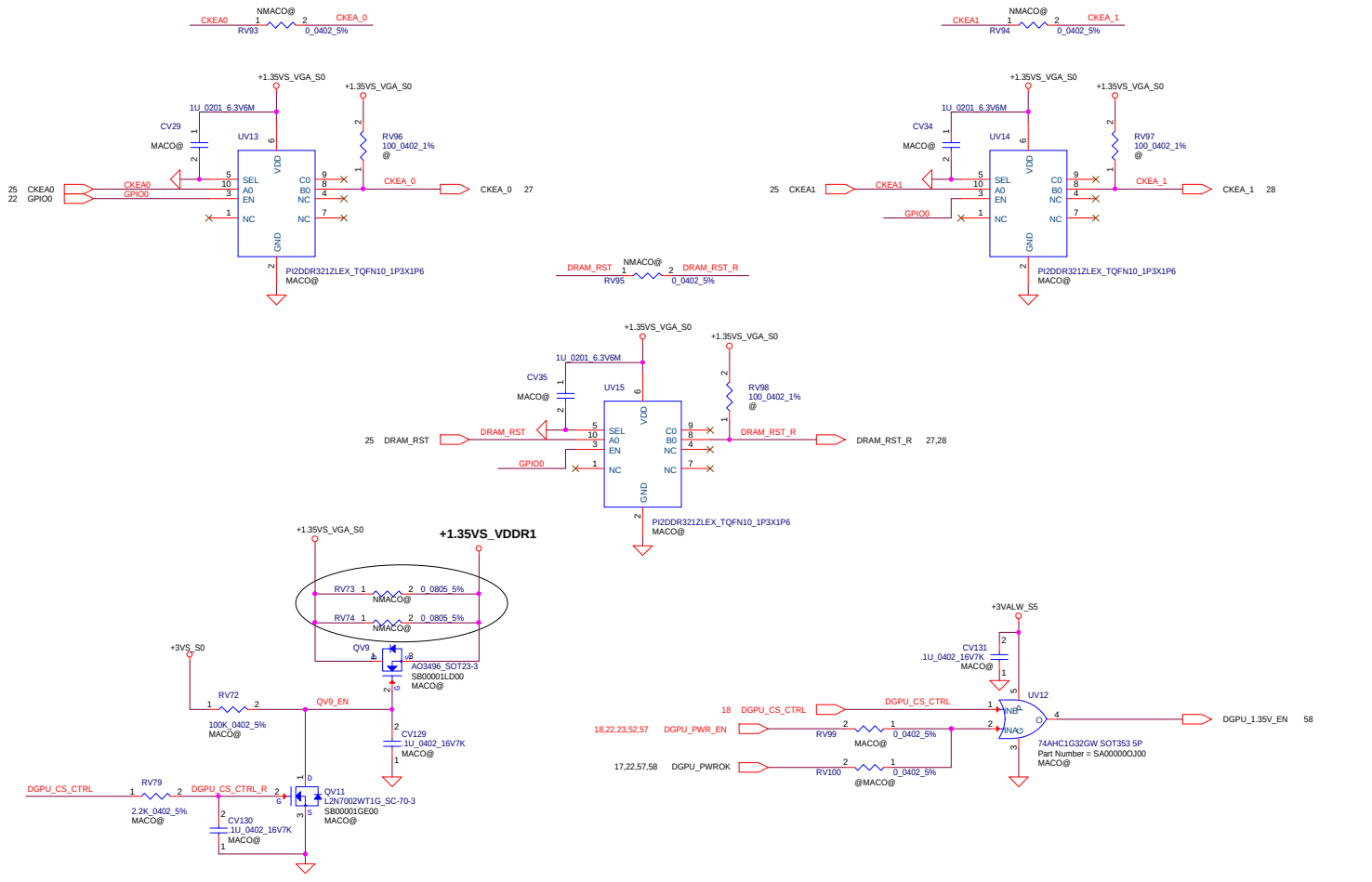
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R17M-M1-70(5/6) MEM

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

Date: Tuesday, March 13, 2018 | Sheet 25 of 67



Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

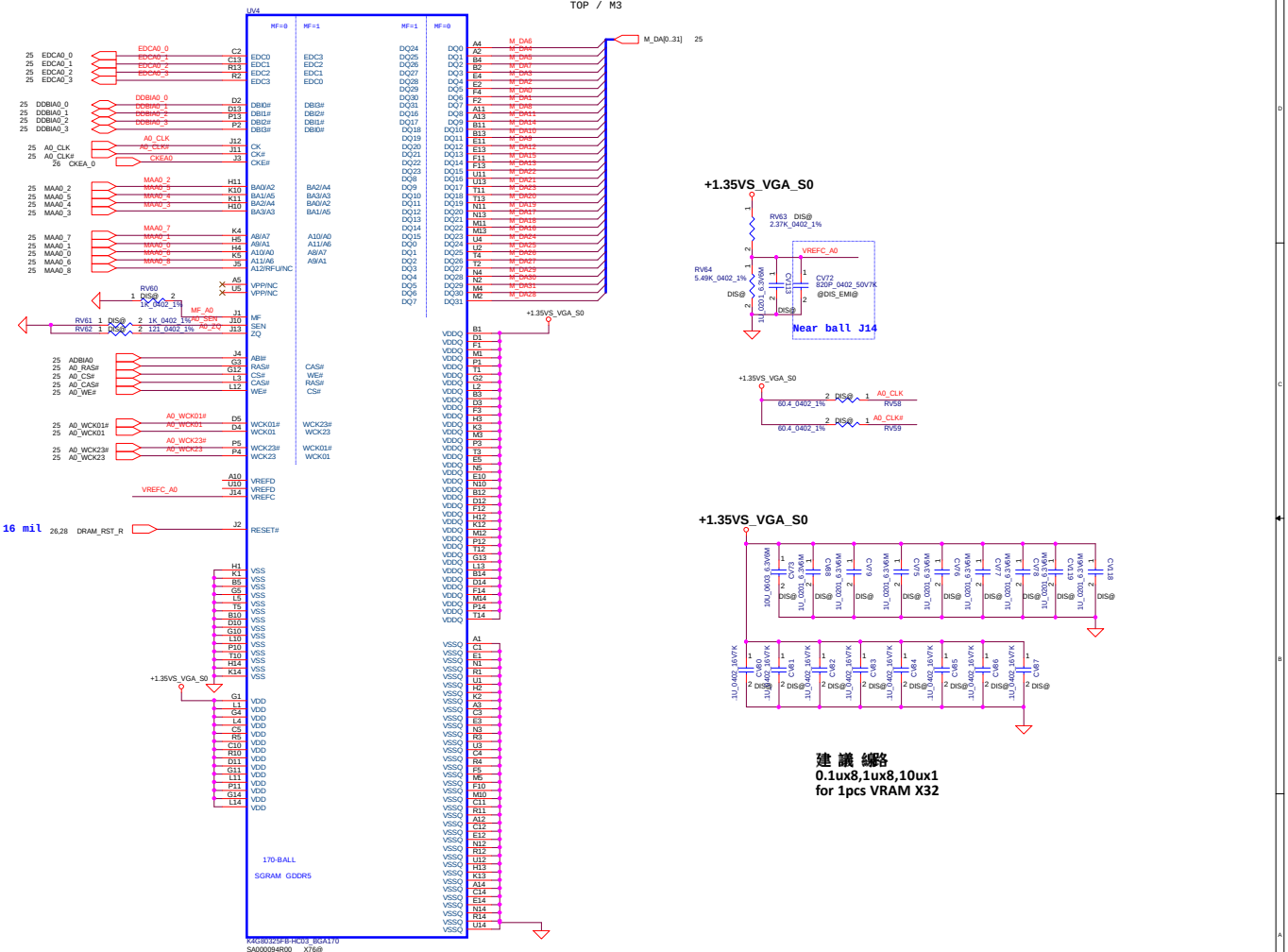
Title: R17M-M1-70(6/6)_VDDR1

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

Date: Tuesday, March 13, 2018 Sheet 26 of 67

Memory Partition A Lower -32 bits

TOP / M3

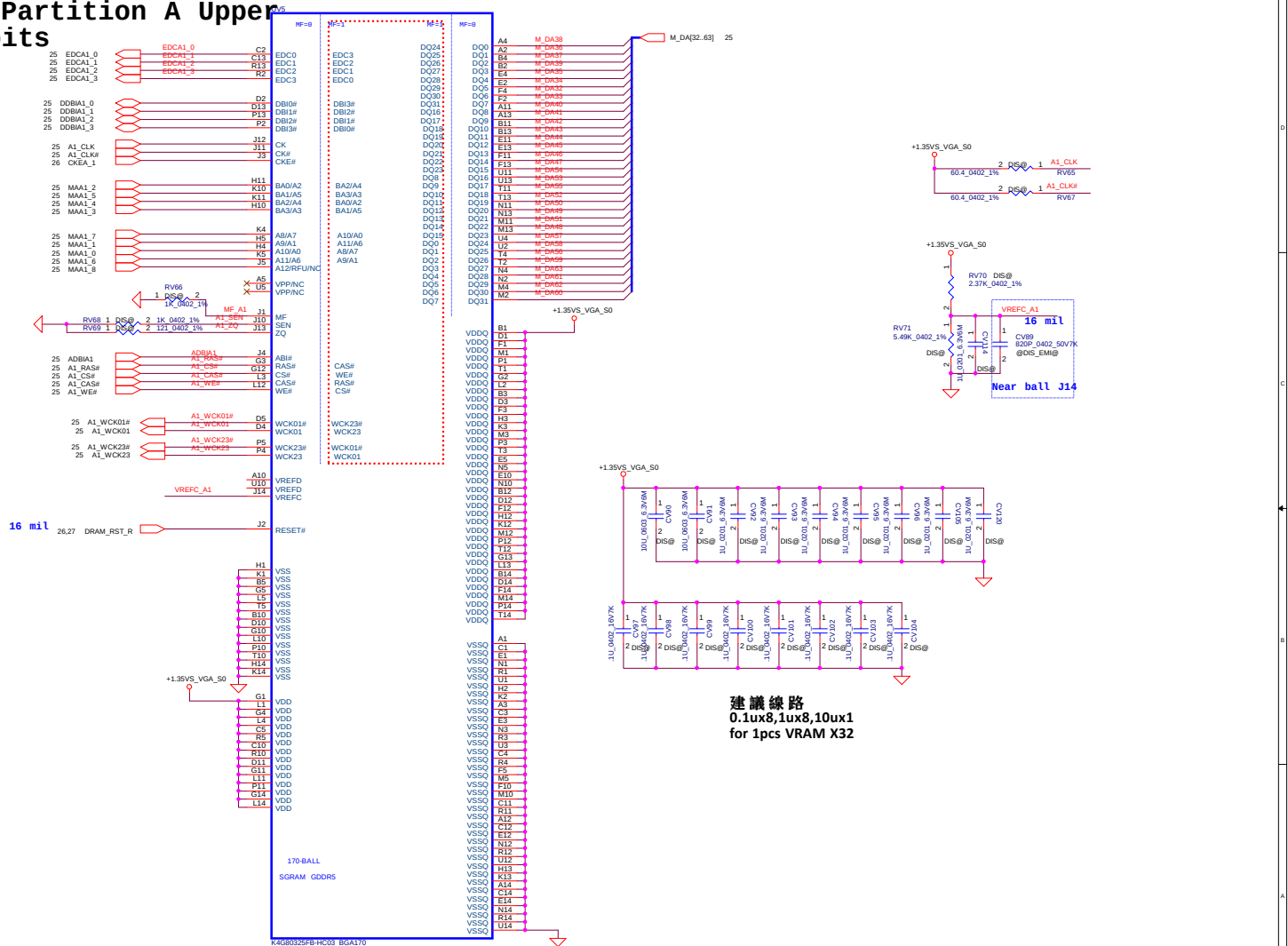


建 議 繪
0.1ux8,1ux8,10ux1
for 1pcs VRAM X32

Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

Compal Electronics, Inc.			
Title	GDDR5 VRAM A Lower		
Size	Document Number	LA-F901P M/B	Rev 0.1
Date: Tuesday, March 13, 2018	Sheet 27 of 67		

Memory Partition A Upper - 32 bits



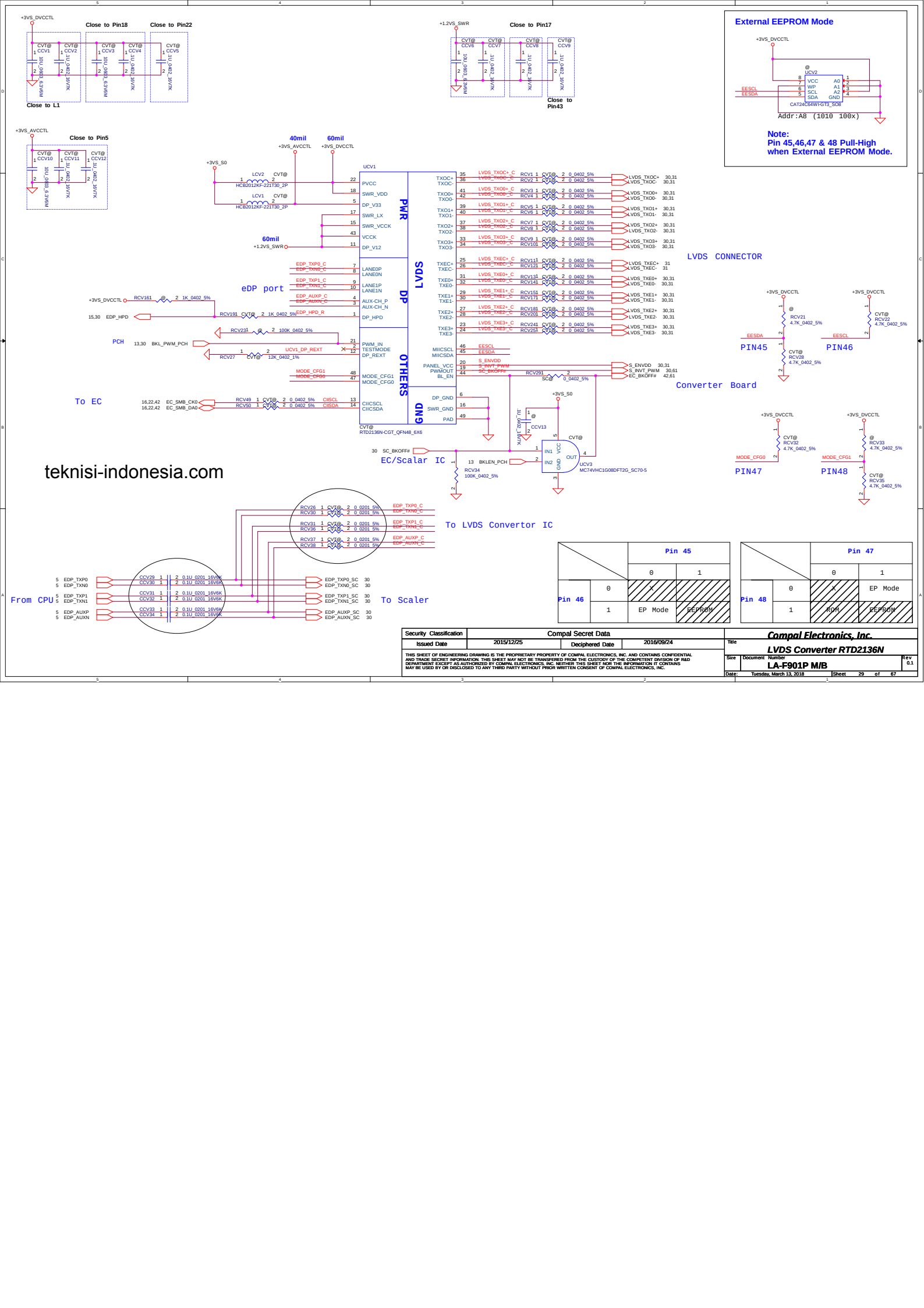
Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

Compal Electronics, Inc.

Title: GDDR5_A Upper

Size	Document Number	Rev
	LA-F901P M/B	0.1

Date: Tuesday, March 13, 2018 Sheet 28 of 67


External EEPROM Mode
Addr:A8 (1010 100x)
Note:
Pin 45,46,47 & 48 Pull-High
when External EEPROM Mode.
LVDS CONNECTOR
eDP port
PCH
To EC
EC/Scalar IC
Converter Board
PIN45
PIN46
PIN47
PIN48
teknisi-indonesia.com
To LVDS Convertor IC
From CPU
To Scaler
Pin 45
Pin 46
Pin 47
Pin 48
EP Mode
EEPROM
ROM
Compal Electronics, Inc.
LVDS Converter RTD2136N
LA-F901P M/B
Compal Secret Data
2015/12/25
2016/09/24
Tuesday, March 13, 2018
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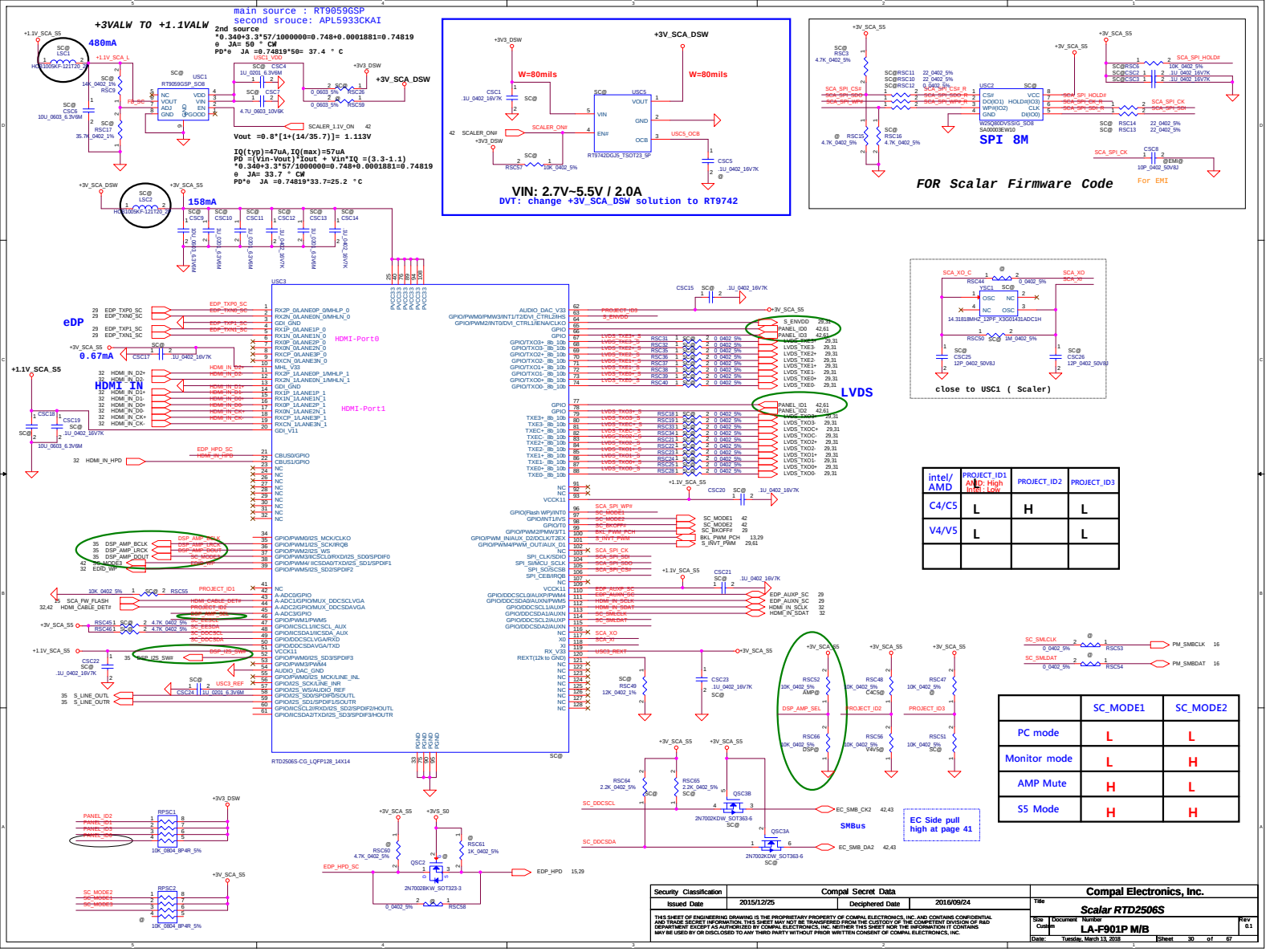


intel/ AMD	PROJECT_ID1 AMD: High Intel: Low	PROJECT_ID2	PROJECT_ID3
C4/C5	L	H	L
V4/V5	L		L

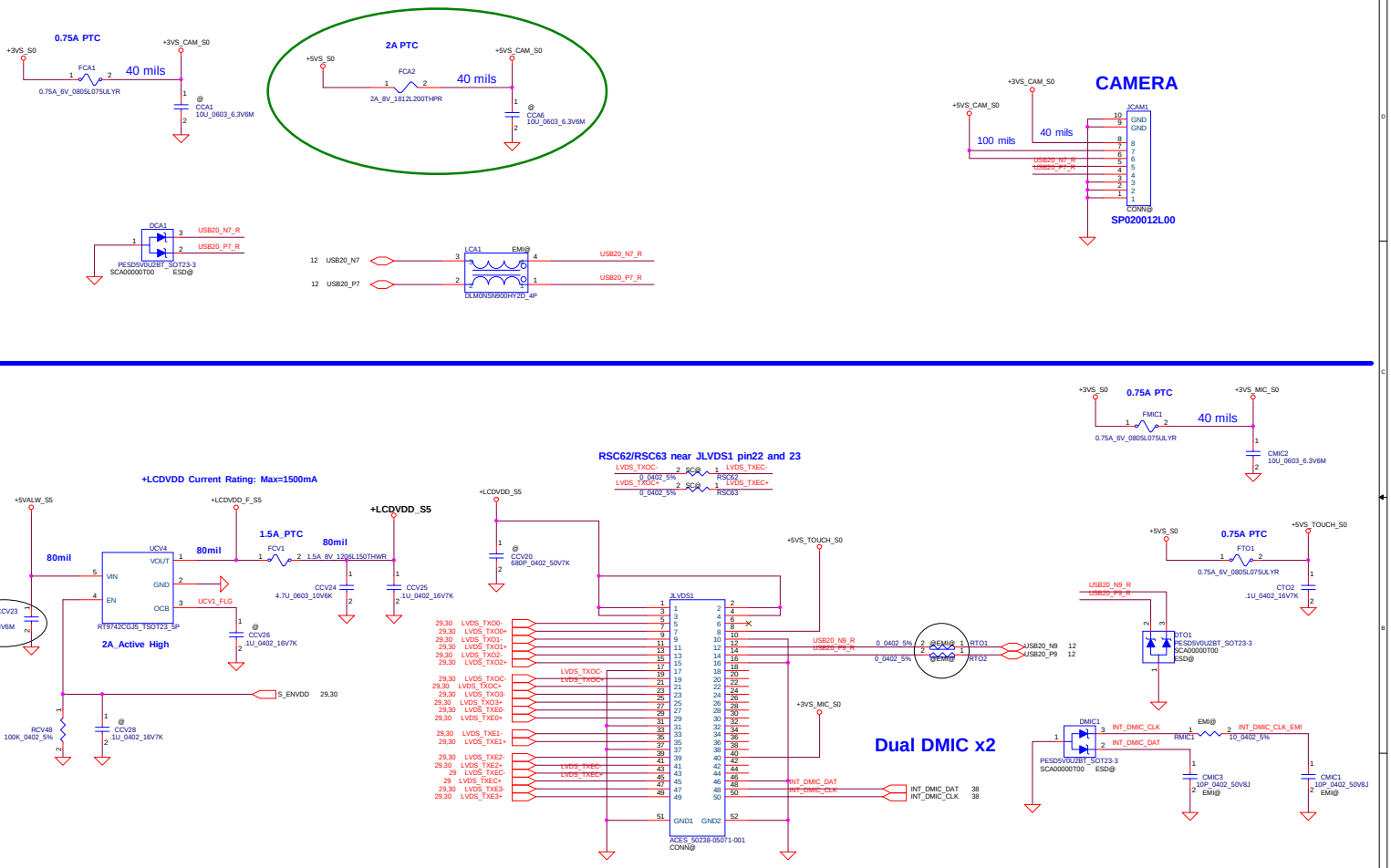
	SC_MODE1	SC_MODE2
PC mode	L	L
Monitor mode	L	H
AMP Mute	H	L
S5 Mode	H	H

EC Side pull high at page 41

SMBus

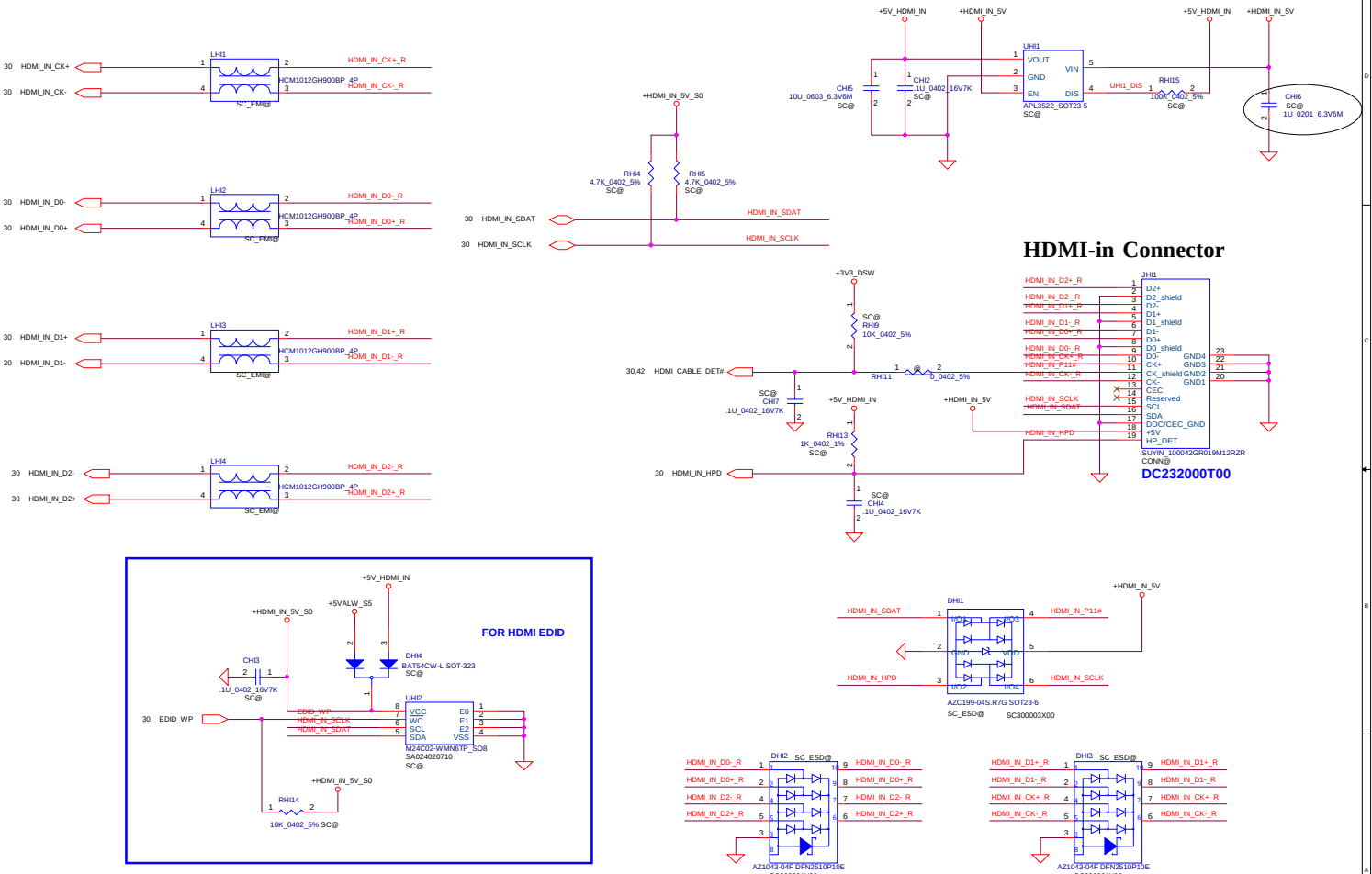
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title: Scalar RTD2506S			
Size: Custom	Document Number: LA-F901P M/B		Rev: 0.1
Date: Tuesday, March 13, 2018	Sheet 30 of 67		



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title: LVDS/Convertor/CAM/Touch			
Size: Custom	Document Number: LA-F901P M/B		Rev: 0.1
Date: Tuesday, March 13, 2018		Sheet 31 of 67	



HDMI-in Connector

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

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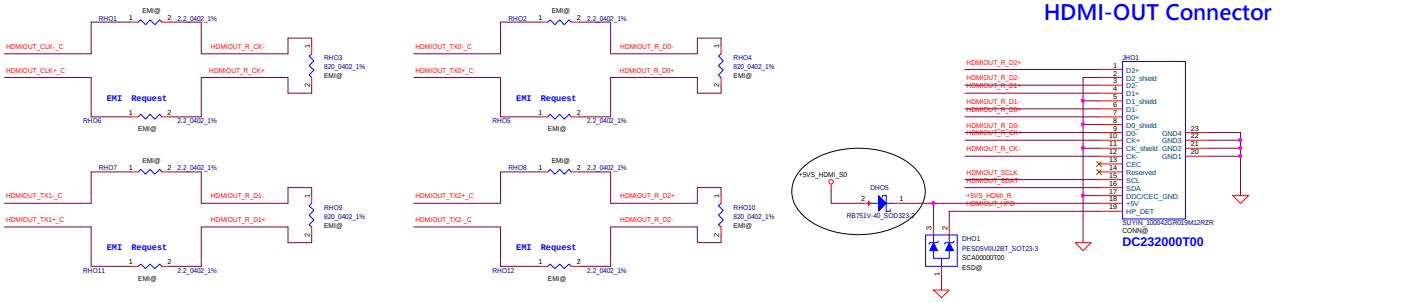
Compal Electronics, Inc.

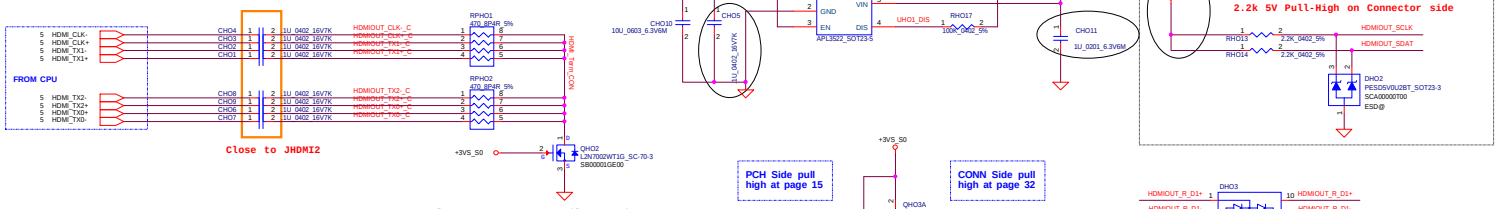
Title: *HDMI-IN conn*

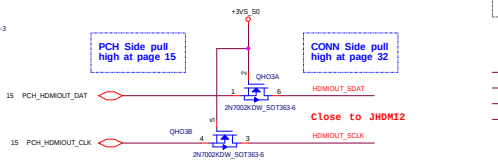
Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

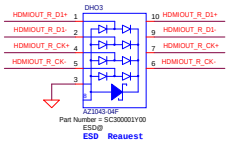
Date: Tuesday, March 13, 2018 Sheet 32 of 67

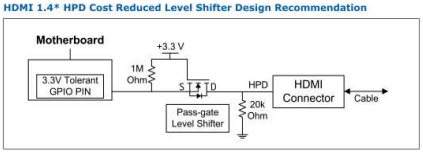
HDMI-OUT Connector

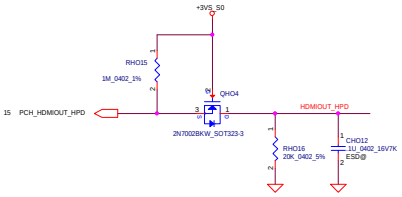


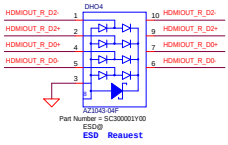












Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

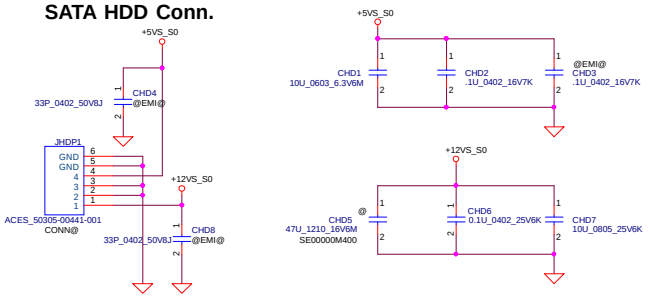
Compal Electronics, Inc.

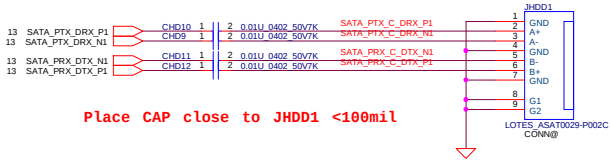
Title: **HDMI IN**

Size | Document Number | Rev: **LA-F901P M/B** | 0.1

Date: Tuesday, March 13, 2018 | Sheet 33 of 67

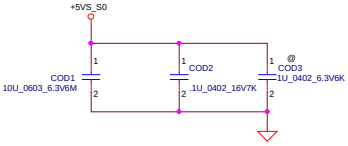
SATA HDD Conn.

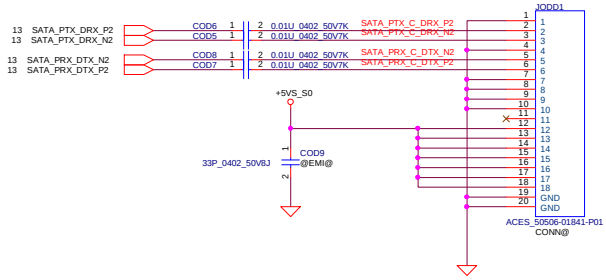




Place CAP close to JHDD1 <100mil

SATA ODD Conn





Place CAP close to JODD1 <100mil

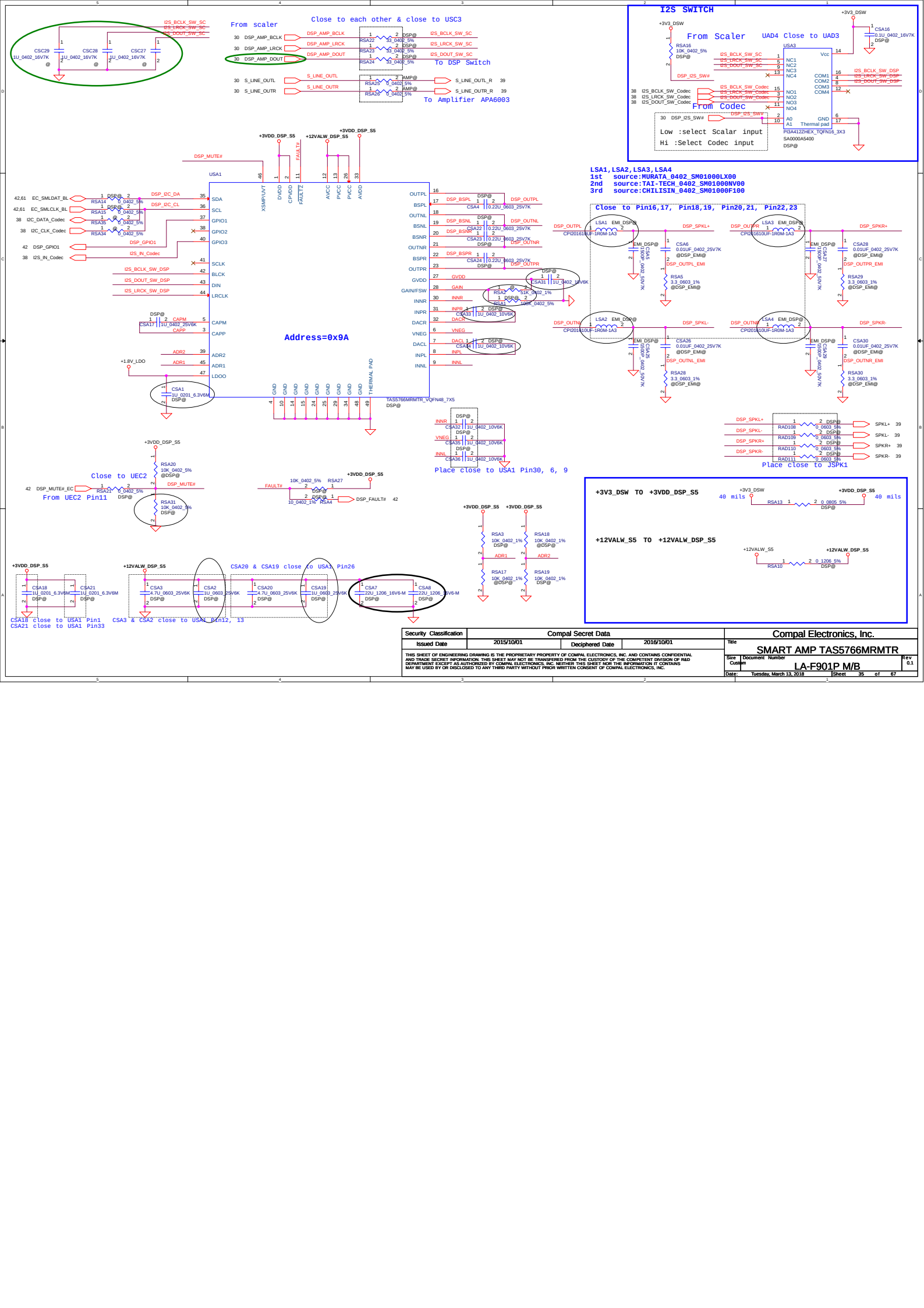
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***HDD/ODD***

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

Date: Tuesday, March 13, 2018 Sheet 34 of 67



Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

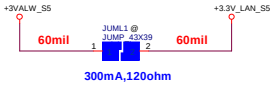
Compal Electronics, Inc.

Title: SMART AMP TAS5766MRMTR

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

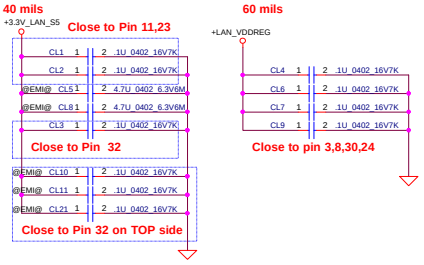
Date: Tuesday, March 13, 2018 | Sheet 35 of 67

WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)



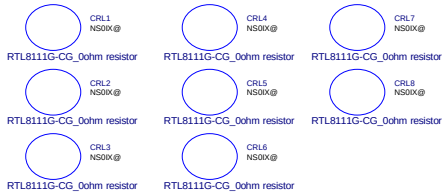
LED Status

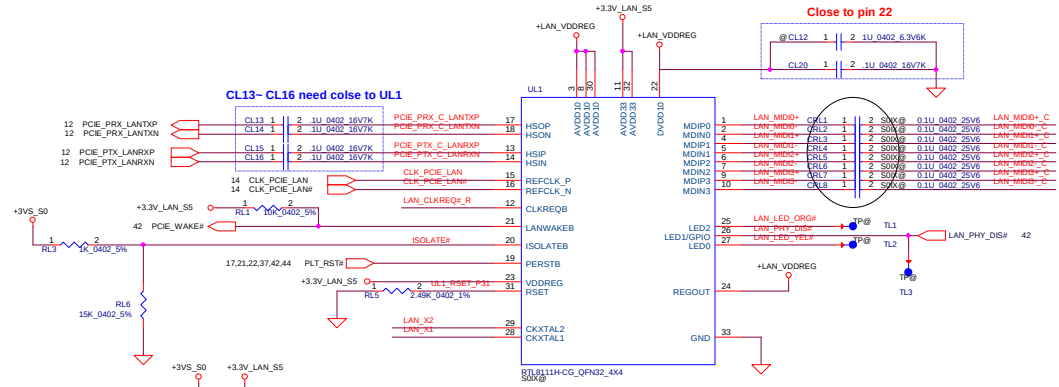
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

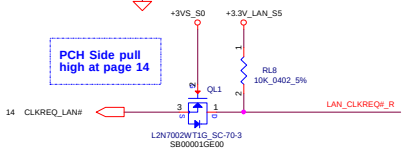
blinking

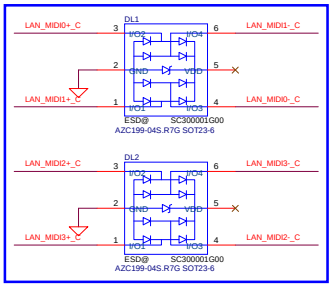
8111G resistor/8111H capacitor

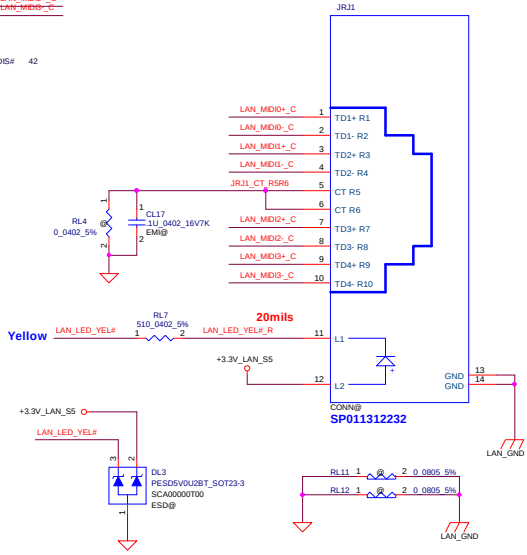


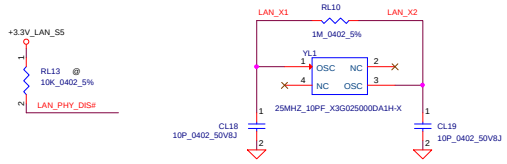


8111G/8111H LAN chip









Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

Compal Electronics, Inc.

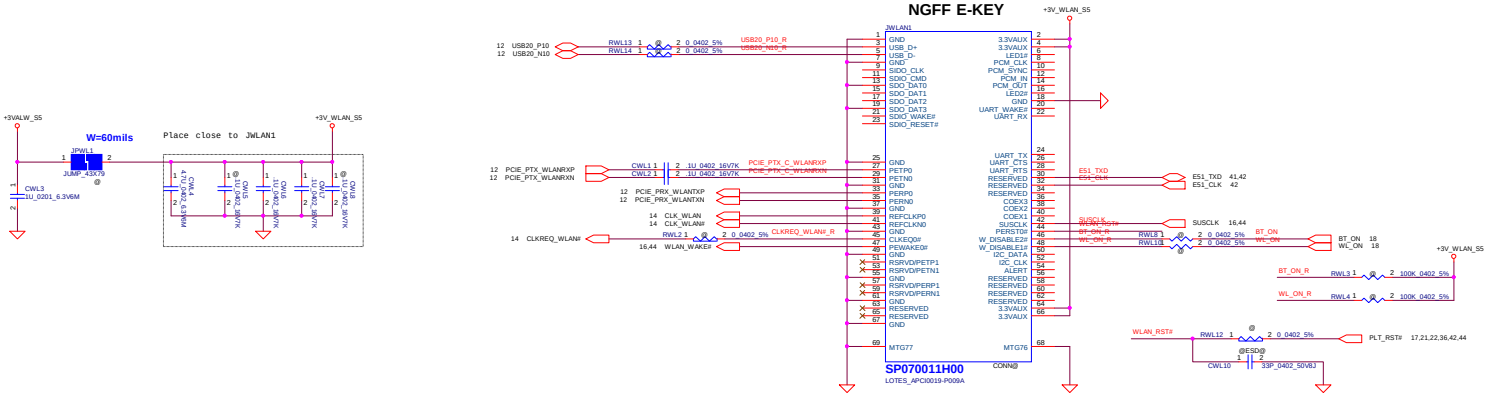
Title: **LAN RTL8111G/H**

Size: Custom | Document Number: **LA-F901P M/B** | Rev: 0.1

Date: Tuesday, March 13, 2018 | Sheet 36 of 67

WLAN (WIFI/BT Combo)

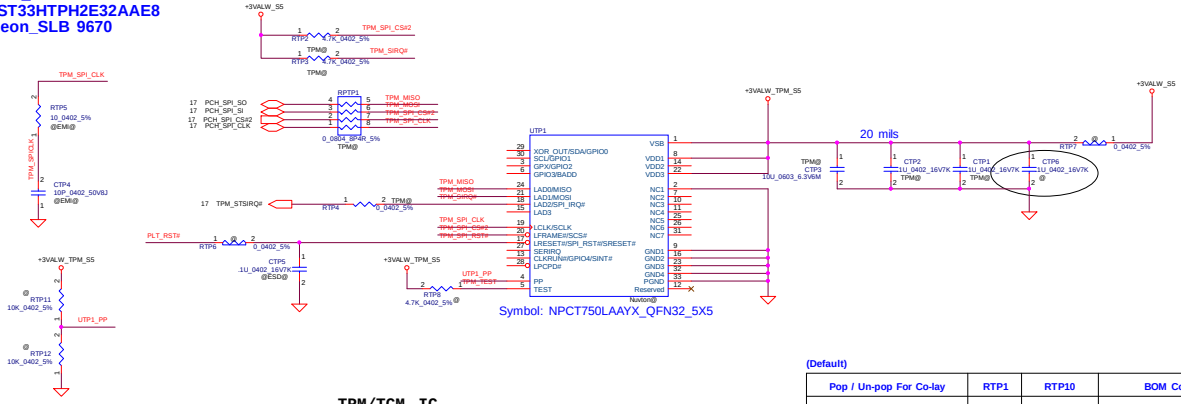
WLAN Conn.
NGFF E-KEY



TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



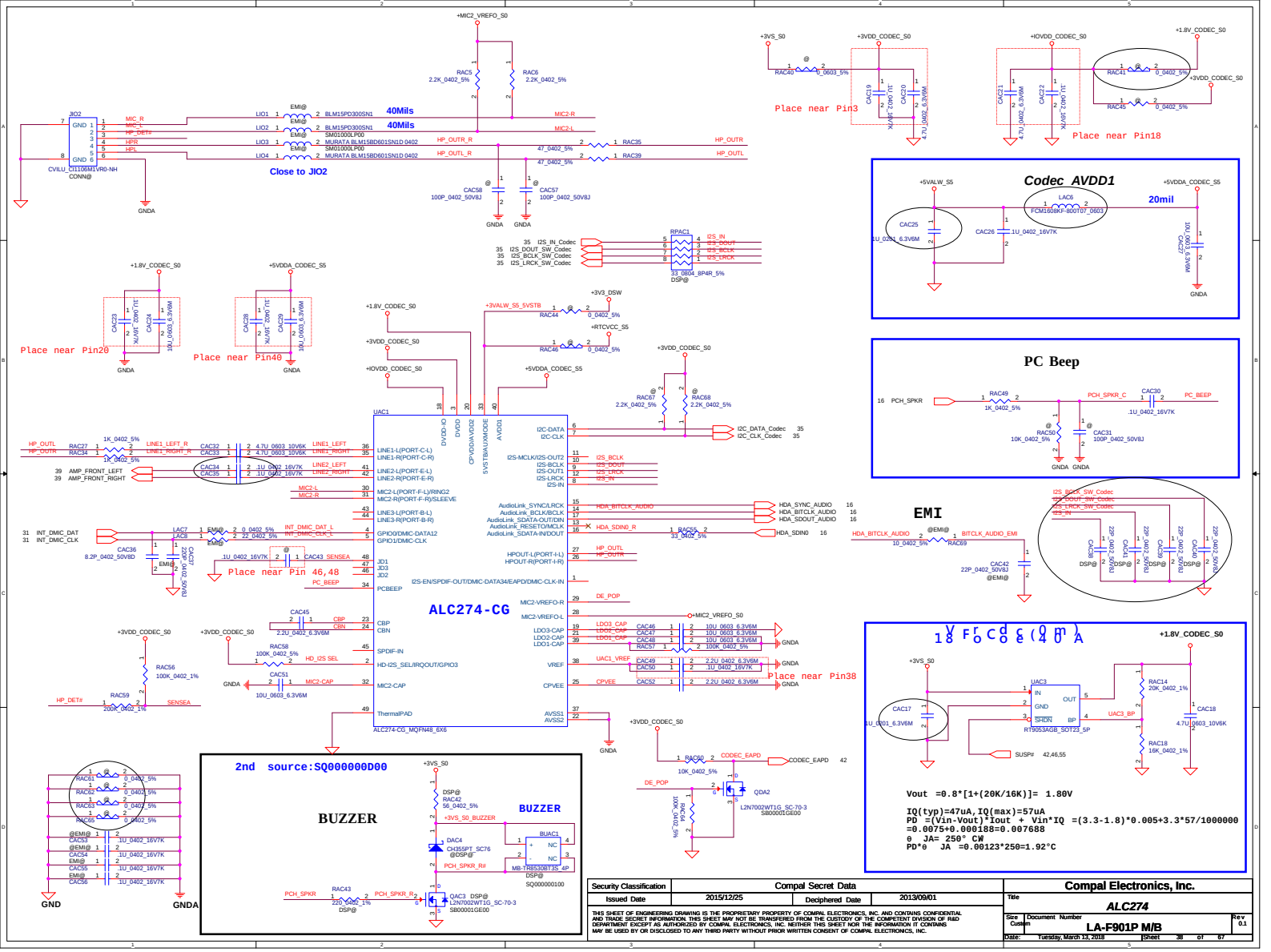
TPM/TCM IC

(Default)

Pop / Un-pop For Co-lay	RTP1	RTP10	BOM Config
Nuvton_NPCT650LBAYX (SPI)	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	X	X	Infineon@+TPM@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date	2015/10/02

Title	WLAN (NGFF) / TPM		
Size	Document Number		Rev 0.1
	LA-F901P M/B		
Date: Tuesday, March 13, 2018		Sheet 37 of 67	



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

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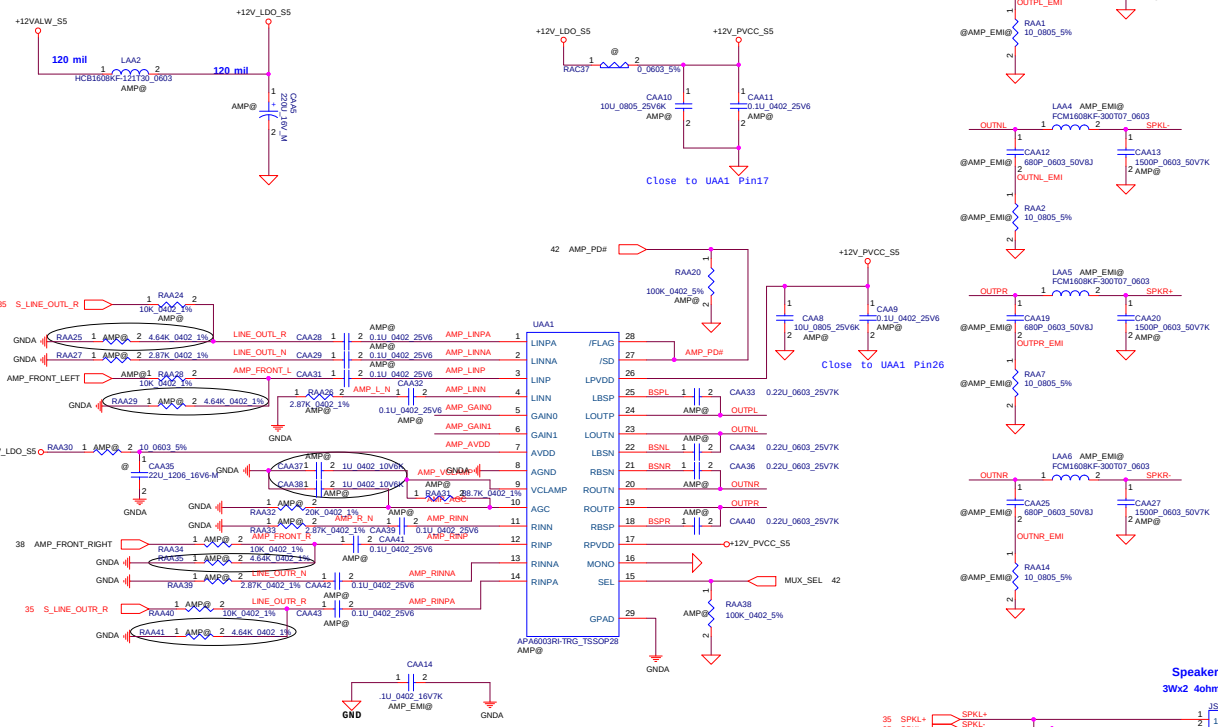
Compal Electronics, Inc.

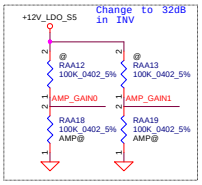
Title: *ALC274*

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

Date: Tuesday, March 13, 2018 | Sheet 38 of 67



APA6003 for Speaker (CRB)



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

MUX_SEL	L=Audio Codec Input source H=Scalar Input source

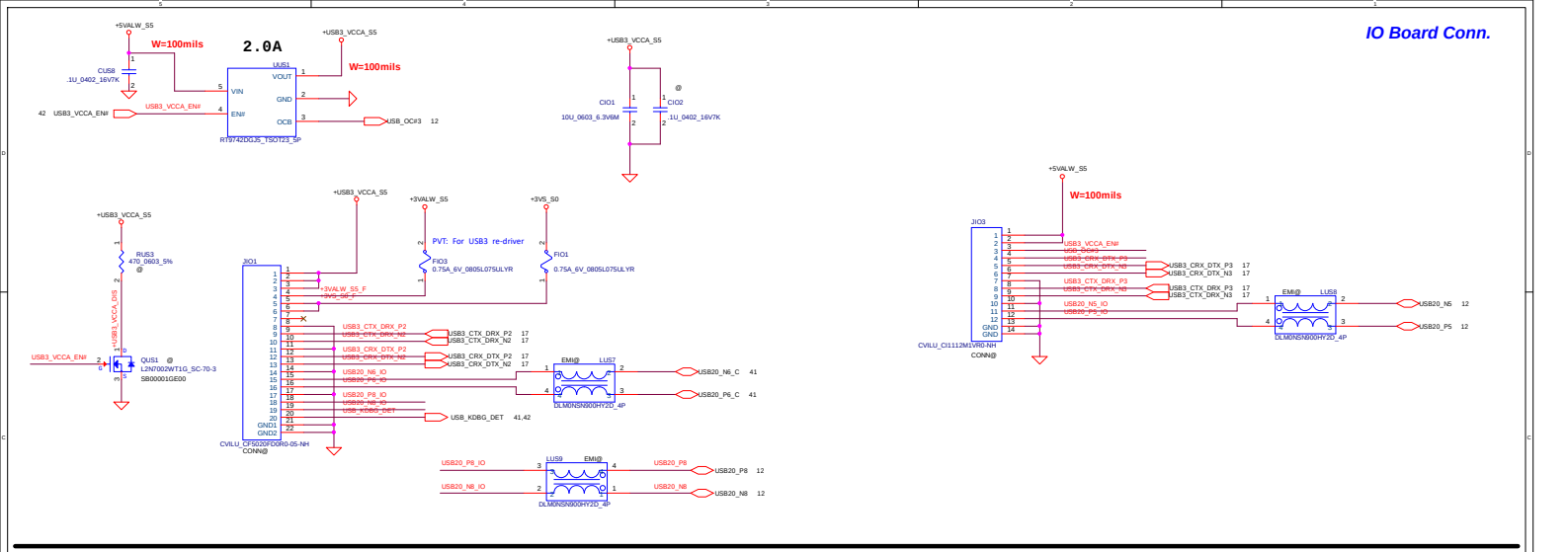
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

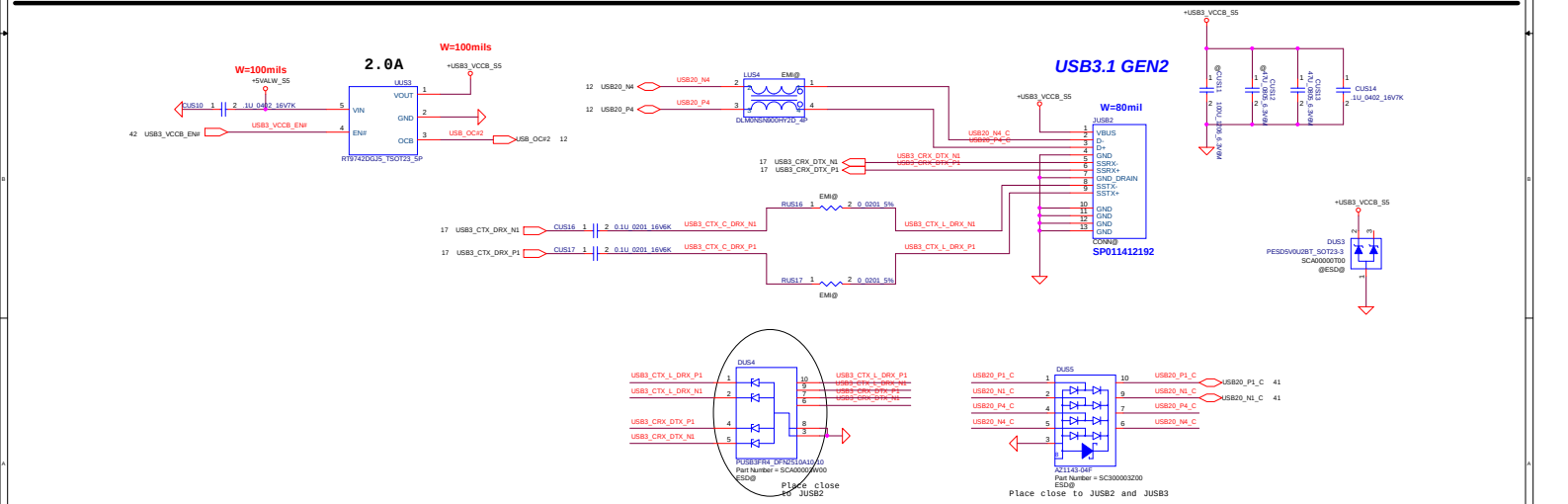
Compal Electronics, Inc.

Title: **Amp ANPEC APA6003**

Size: Custom | Document Number: **LA-F901P M/B** | Rev: 0.1

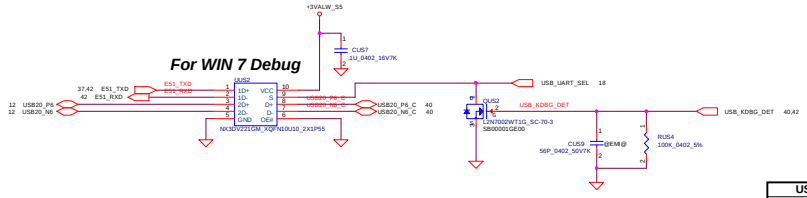
Date: Tuesday, March 13, 2018 | Sheet 39 of 67



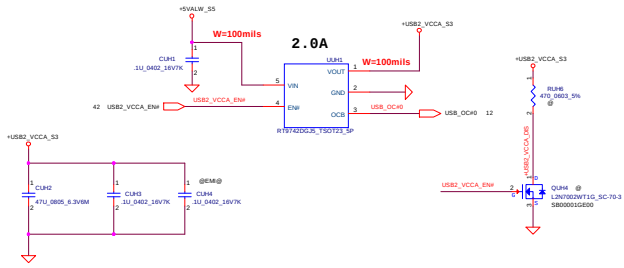


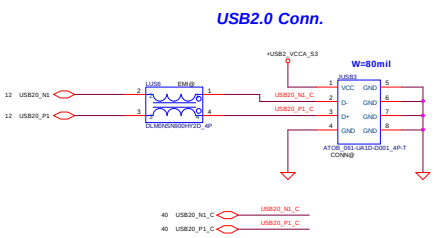
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date	2016/09/24

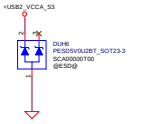
Title	Side USB3.0 x 2/IO Board Conn.		
Size C	Document Number LA-F903P M/B		Rev 0.1
Date: Tuesday, March 13, 2018	Sheet 40 of 67		



USB MUX Selection	
KDBG_MUX_SEL	Output
H	D = D2
L	D = D1

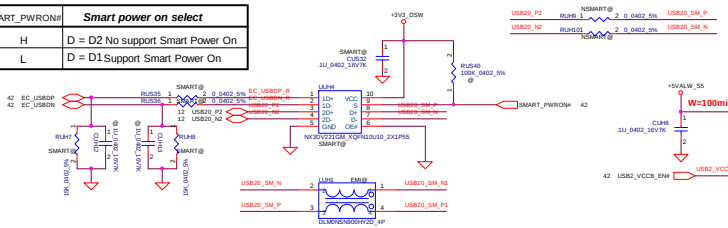


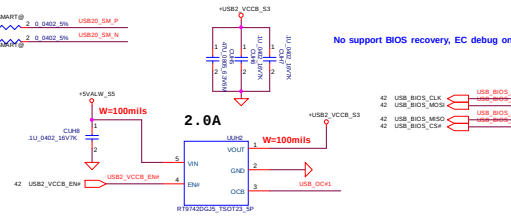




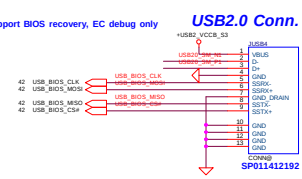
Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

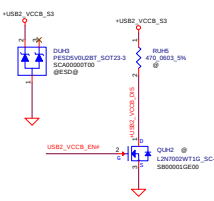
SMART_PWRON#	Smart power on select
H	D = D2 No support Smart Power On
L	D = D1 Support Smart Power On

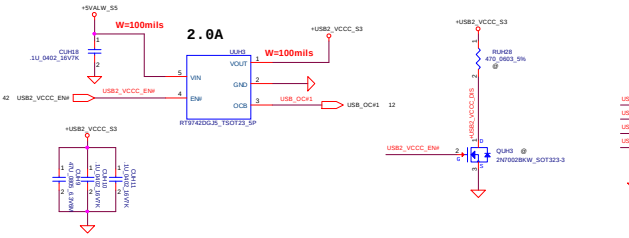


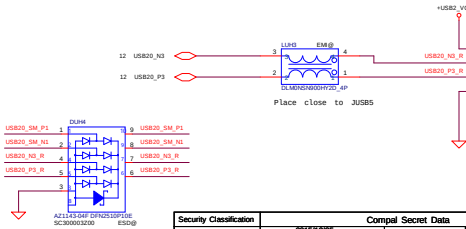


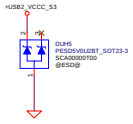
No support BIOS recovery, EC debug only





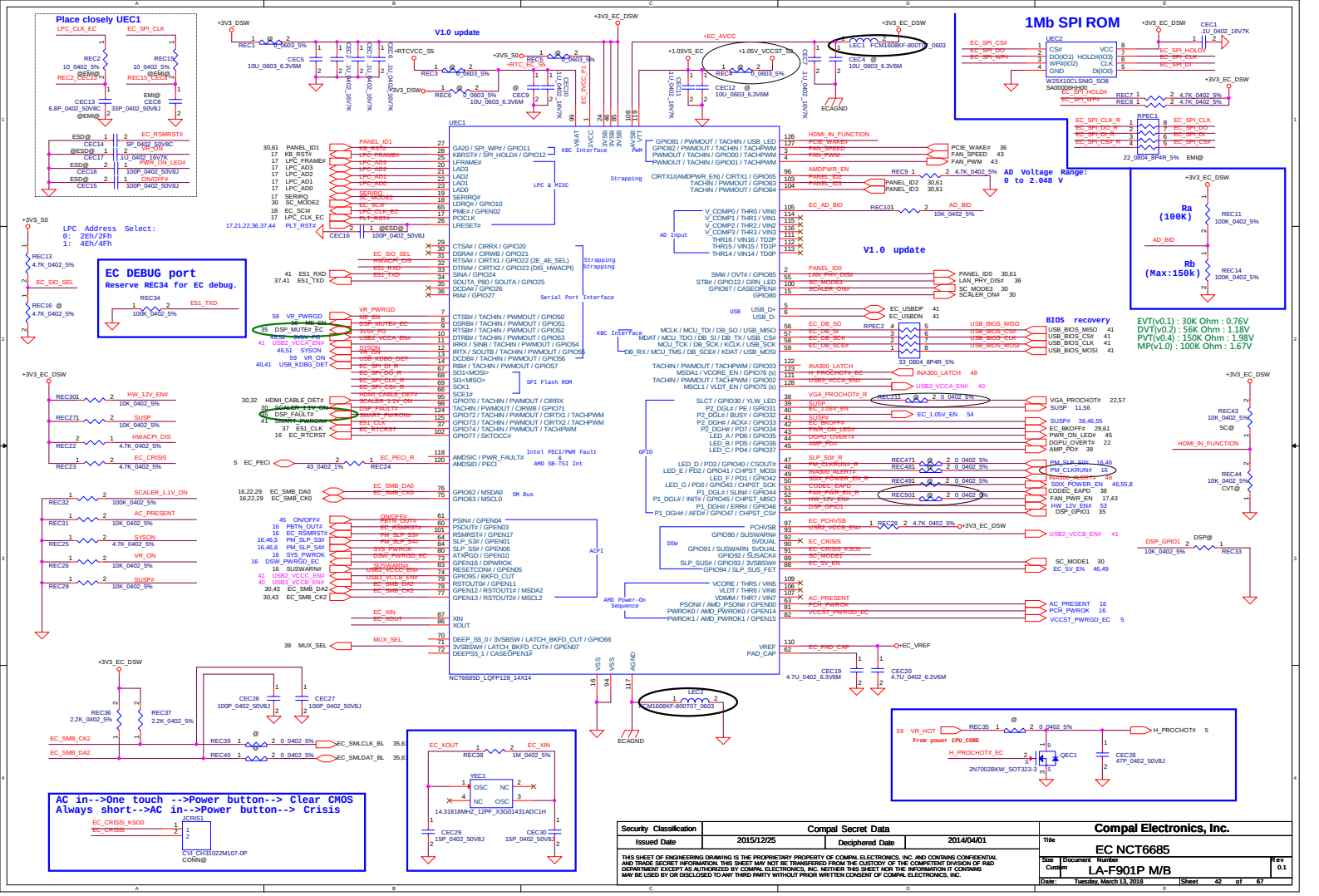


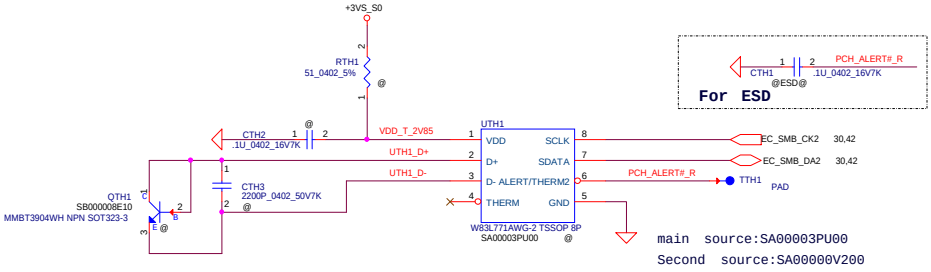


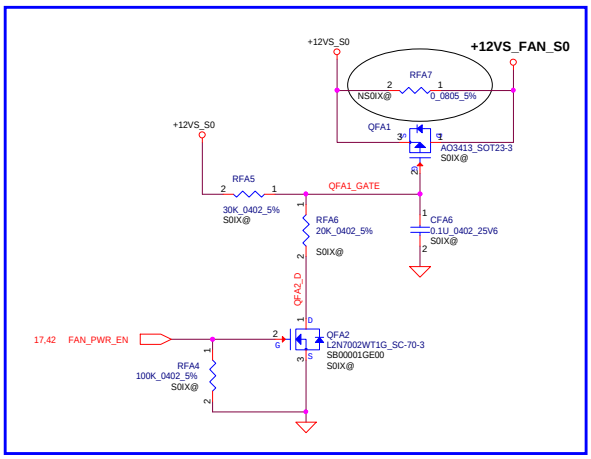


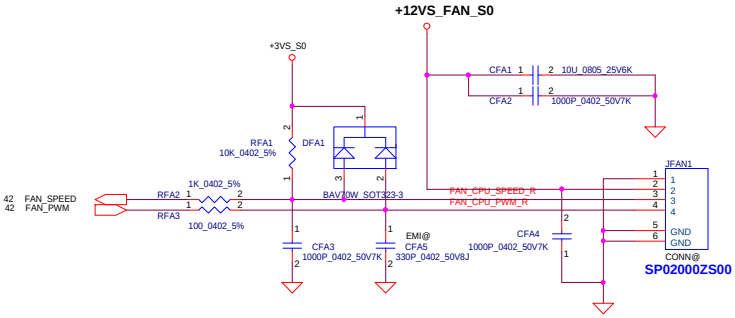
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title: Rear USB2.0 x 3			
Size: Custom	Document Number: LA-F901P M/B		Rev: 0.1
Date: Tuesday, March 13, 2018	Sheet 41 of 67		


Place closely UEC1
V1.0 update
1Mb SPI ROM
EC DEBUG port
Reserve REC34 for EC debug.
LPC Address Select:
0: 2Eh/2Fh
1: 4Eh/4Fh
V1.0 update
AD Voltage Range:
0 to 2.048 V
BIOS recovery
EVT(v0.1) : 30K Ohm : 0.76V
DVT(v0.2) : 56K Ohm : 1.18V
PVT(v0.4) : 150K Ohm : 1.98V
MP(v1.0) : 100K Ohm : 1.67V
AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis
From power CPU_CORE
NCT6685D_LQFP128_14X14
Compal Electronics, Inc.
EC NCT6685
LA-F901P M/B
Security Classification
Compal Secret Data
Issued Date
2015/12/25
Deciphered Date
2014/04/01
Tuesday, March 13, 2018
Sheet 42 of 67

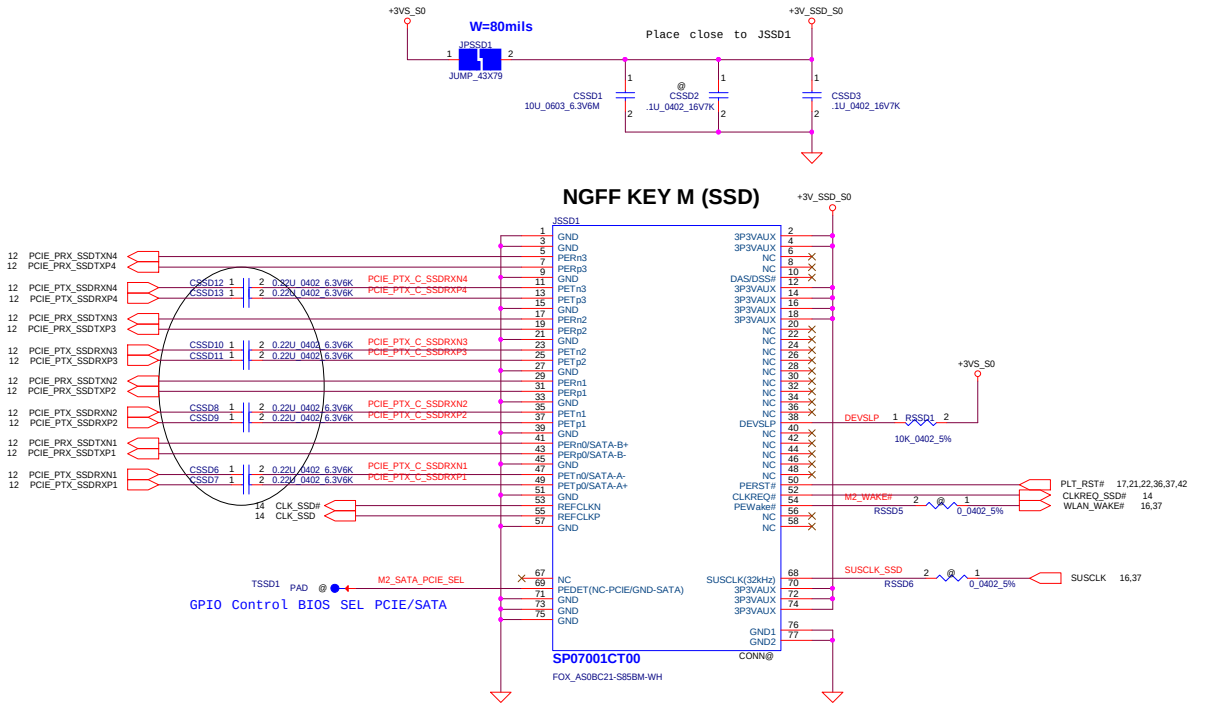






Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

Compal Electronics, Inc.		
Title	FAN/Thernal Sensor	
Size	Document Number LA-F901P M/B	Rev 0.1
Date: Tuesday, March 13, 2018	Sheet 43 of 67	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date 2013/09/01	Title: SSD (M2)
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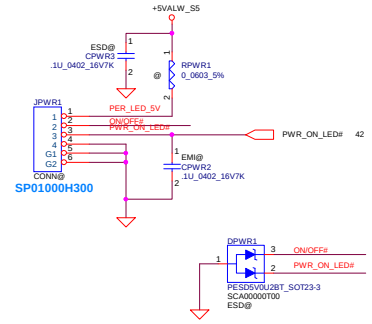
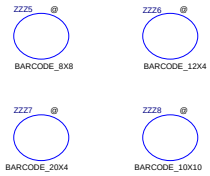
			Date: Tuesday, March 13, 2018; Sheet 44 of 67

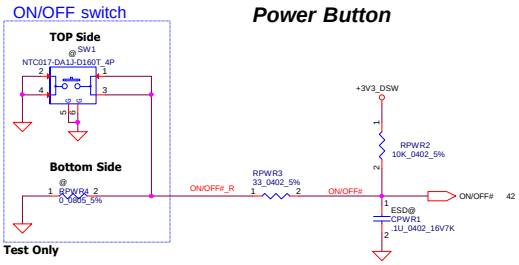


BARCODE



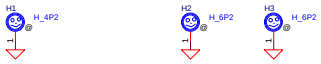
ON/OFF switch

Power Button



WIFI Hole

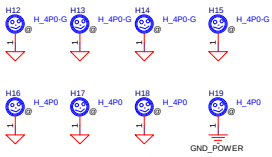
SSD Hole



Other Hole

Screw Hole

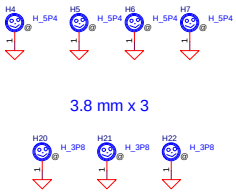
4.0 mm x 8



CPU Hole

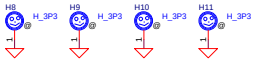
5.4mm x 4

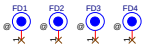
3.8 mm x 3



GPU Hole

3.3 mm x 4





Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

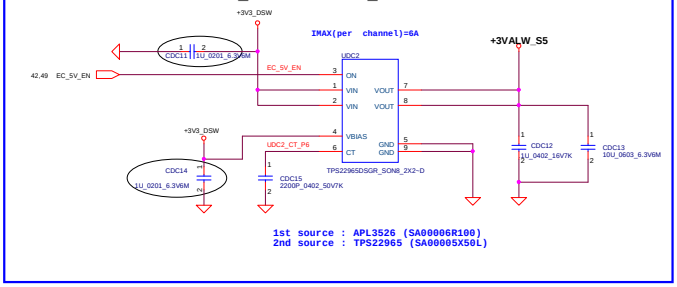
Compal Electronics, Inc.

Title: **PWR SW/LED/SCREW**

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

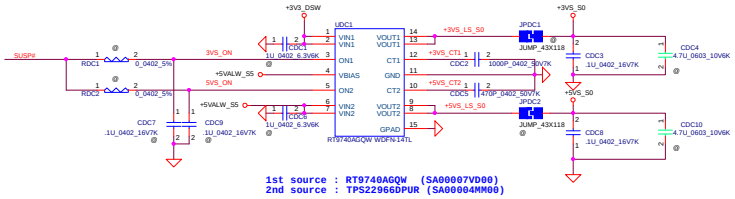
Date: Tuesday, March 13, 2018 Sheet 45 of 67

+3VDSW_S5 to +3VALW_S5 Transfer

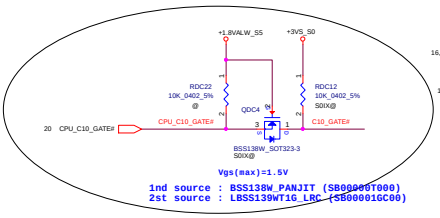


1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

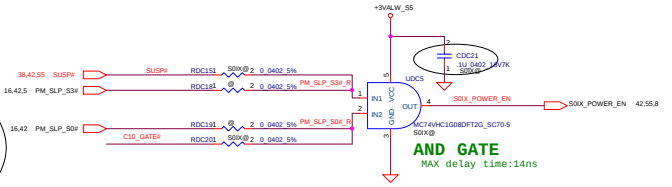


1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)



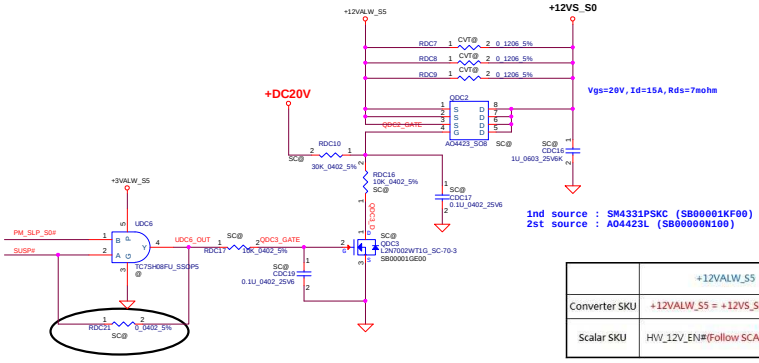
Vgs(max)=1.5V

1nd source : BSS138W_PANJIT (SB00000T000)
2st source : LBSS139WT1G_LRC (SB00001GC00)



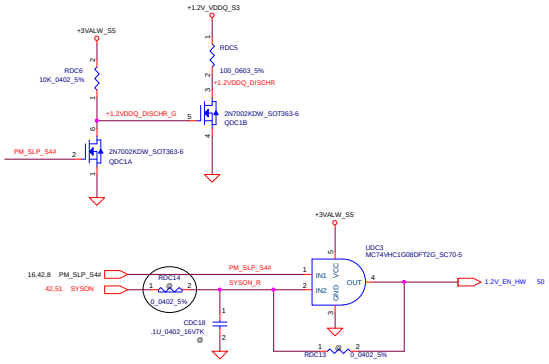
AND GATE
MAX delay time:14ns

+12VALW_S5 TO +12VS_S0 (PMOS)



Vgs=20V,Id=15A,Rds=7mohm

1nd source : SM4331PSKC (SB00001KF00)
2st source : AO4423L (SB00000N100)



	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALER_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC17

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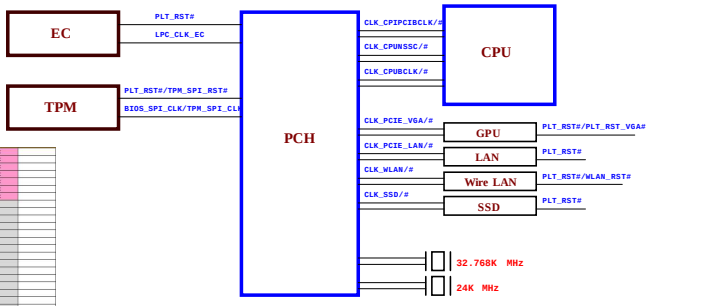
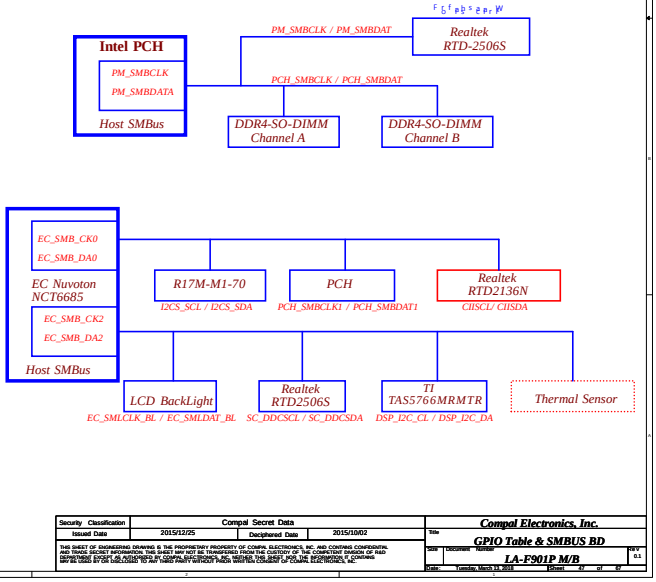
			Size: C / Document Number: LA-F901P M/B / Rev: 0.1
			Date: Tuesday, March 13, 2018 / Sheet: 46 of 67

System clock and Reset map



SMBUS Block Diagram



Security Classification	Compal Secret Data	
Issued Date	2015/12/25	Deciphered Date 2015/10/02

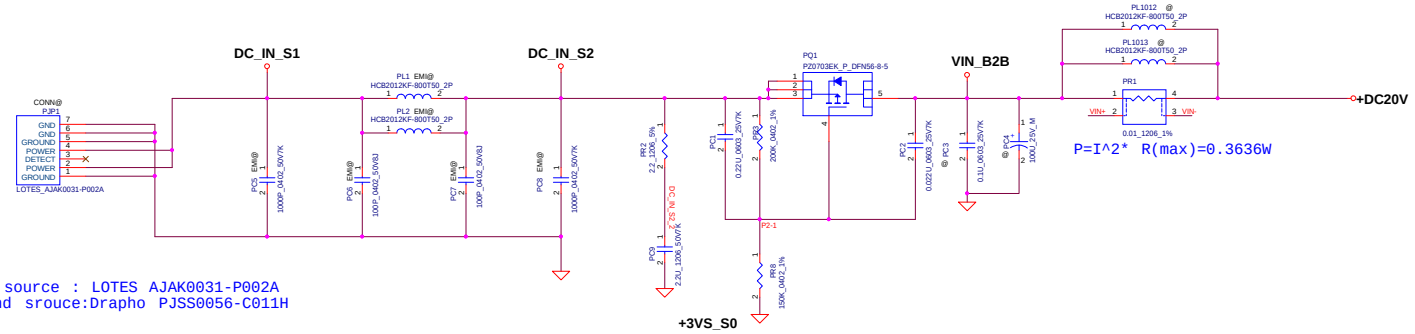
Compal Electronics, Inc.			
Title: GPIO Table & SMBUS BD			
Size:	Document Number: LA-F901P M/B		Rev: 0.1
Date: Tuesday, March 15, 2016	Sheet 47 of 87		

Main source: PZ0703EK
PD =I^2*Rds(on)=6^2*7m ohm=0.252W
θ JA= 50° C/W*0.252W=12.6°C

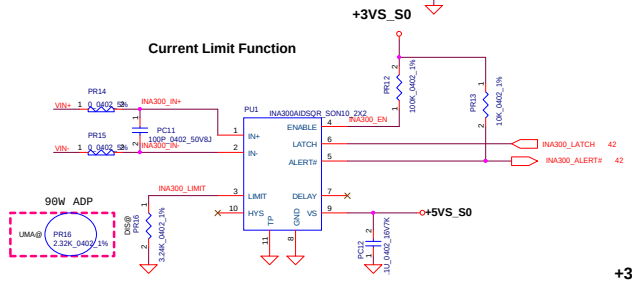
Second source: AON6405L
PD =I^2*Rds(on)=6^2*7m ohm=0.252W
θ JA= 50° C/W*0.252W=12.6°C

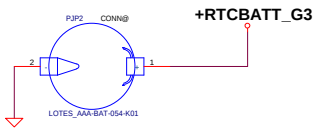
Third source: SIR403EDP-T1-GE3
PD =I^2*Rds(on)=6^2*6.5m ohm=0.234W
θ JA= 65° C/W*0.468W=15.21° C

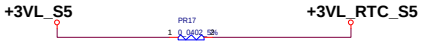
BOM Control



main source : LOTES AJAK0031-P002A
second srouce:Drapho PJSS0056-C011H







90W:
Full Load(100%) --> 4.5A
Vtrip=4.5*10m=45mV
VLimit=Vtrip; Rlimit=(45mV+0.5mV)/20uA= 2.275K

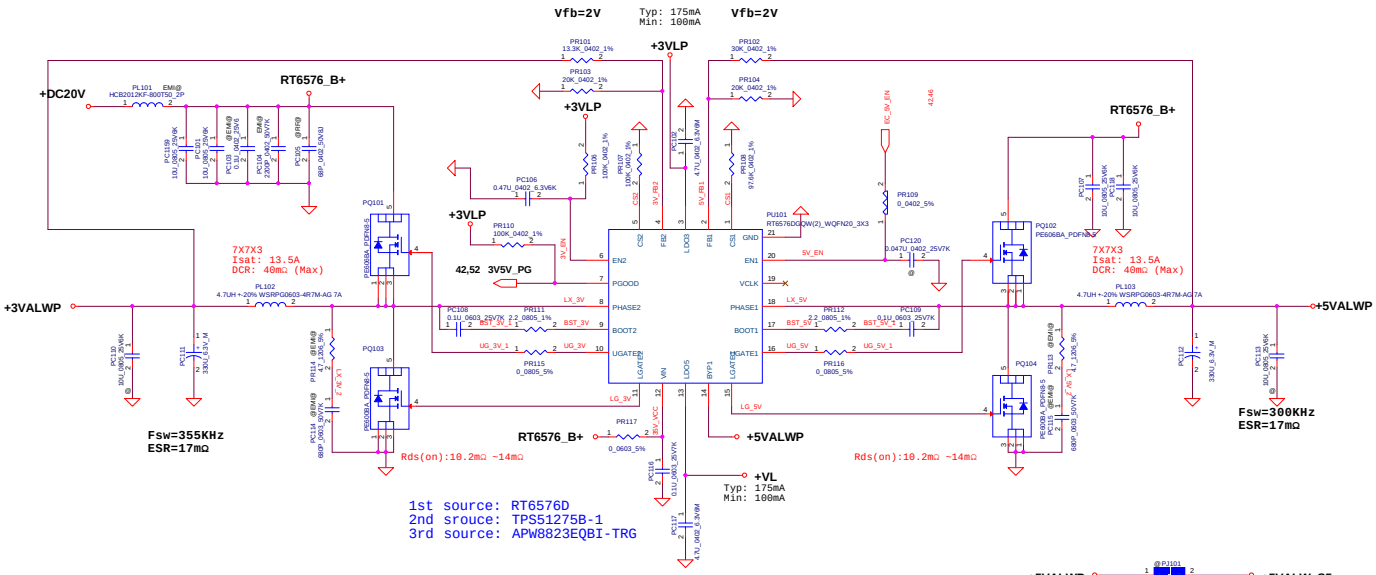
Trigger(116.7%) -->5.25A (@105W)
Vtrip=5.25*10m=52.5mV
Rlimit=(52.5mV+0.5mV)/20uA=2.65K
Select Rlimit=2.61K
I_Trigger-->5.22A

DIS SKU 120W:
Full Load(100%) --> 6A
Vtrip=6*10m=60mV
VLimit=Vtrip; Rlimit=(60mV+0.5mV)/20uA= 3.025K

Trigger(112.5%) --> 6.75A (@135W)
Vtrip=6.75*10m=67.5mV
Rlimit=(67.5mV+0.5mV)/20uA=3.4K
Select Rlimit=3.4K
I_Trigger-->6.75A

Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.			
Title: DCIN / CONN			
Size: Custom	Document Number		Rev: 0.1
Date: Tuesday, March 13, 2018	Sheet 48 of 67		



+3VALWP
Vin = 20V
Iin =3.3*7.87/0.85/20
= 1.527A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+3VALWP
Imax=5.5 ; Ipeak=7.87 ;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=12.03A~12.25A
Iin_ripple=2.05A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.65A
LIR=Delta IL/Ipeak=0.21
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=428.88uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.07uF

+5VALWP
Vin = 20V
Iin =5*7/0.85/20
= 2.06A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
=5V

+5VALWP
Imax=4.9A,Ipeak=7A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.96A~12.18A
Iin_ripple=2.12A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta IL/Ipeak=0.38
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=180.6uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.53uF

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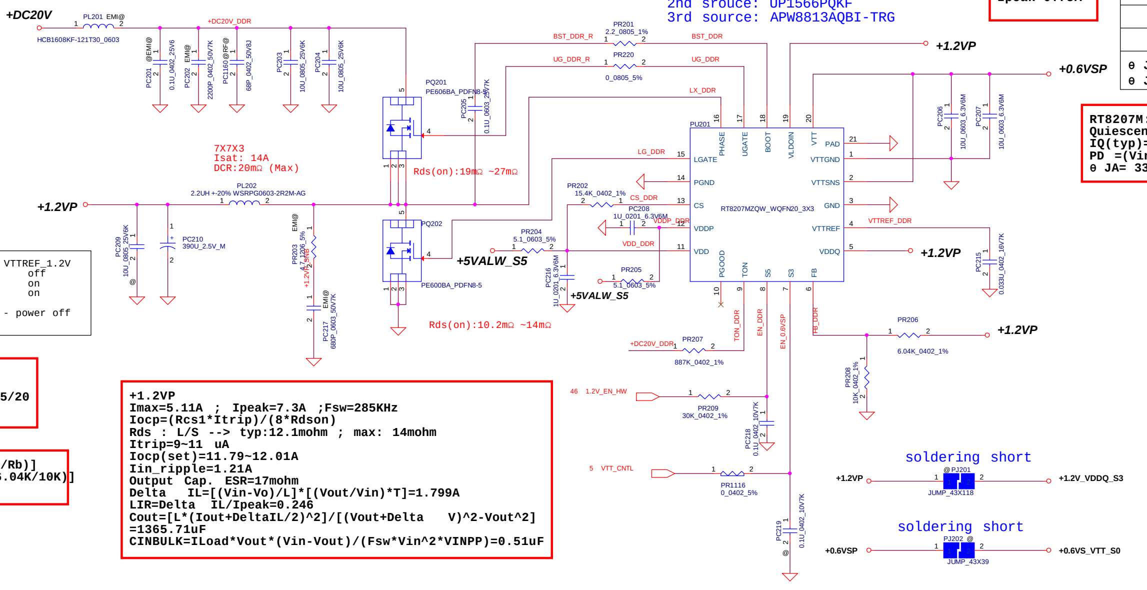
			Size: C; Document Number: ; Rev: 0.1
			Date: Tuesday, March 19, 2013; Sheet 49 of 67

1st source: RT8207MZQW
2nd srouce: UP1566PQKF
3rd source: APW8813AQBI-TRG



+0.6VSP
TDC=0.53A
Ipeak=0.75A

Vo	0.6	
Vin	1.2	
Io	0.75	
PD	0.455	
θ JA(main) θ JA(2nd)	52 68	° C/W

RT8207M:
Quiescent Current (GND Current)
IQ(typ)=0.47mA,IQ(max)=1mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.455W
θ JA= 33.7° C/W*0.903=23.66°C

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin =7.3*1.2/0.85/20
= 0.51A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=5.11A ; Ipeak=7.3A ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.79~12.01A
Iin_ripple=1.21A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.799A
LIR=Delta IL/Ipeak=0.246
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1365.71uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.51uF

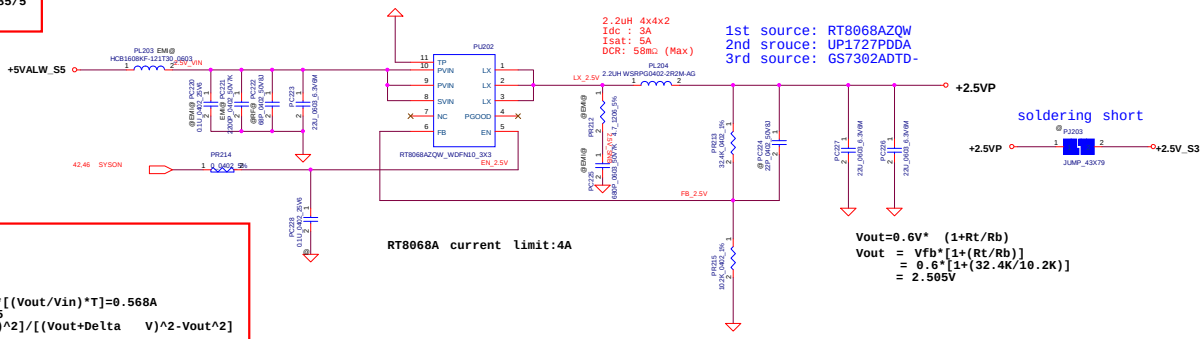
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **+1.2VP/+0.6VSP/+2.5VP**

Size: Custom | Document Number | Rev 0.1

+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A



+2.5VP
Ipeak=2.24A ;Fsw=1MHz
Ilimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF

RT8068A current limit:4A

Vout=0.6V* (1+Rt/Rb)
Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(32.4K/10.2K)]
= 2.505V

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Issued Date	2013/08/15	Deciphered Date	2013/08/29

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Title: **+2.5VP**

Size	Document Number	Rev
C		0.1

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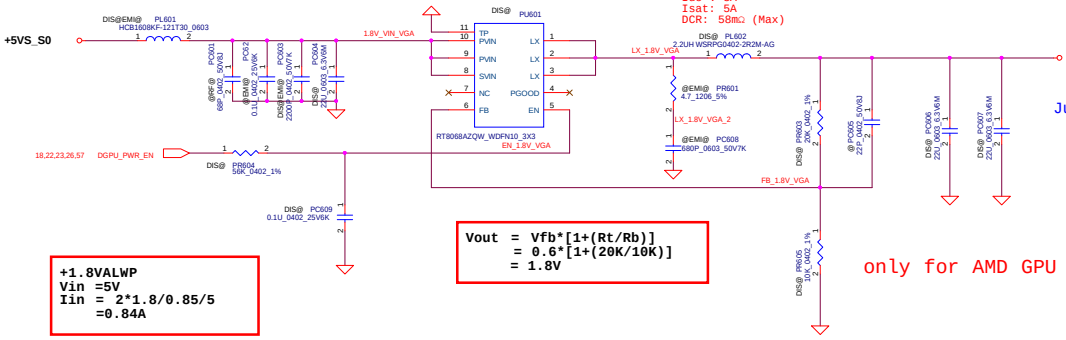
1st source: RT8068A
2nd srouce: UP1727P
3rd source: GS7302SADTD-R

2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR: 58mΩ (Max)



Jumper on HW side(JGPU1)

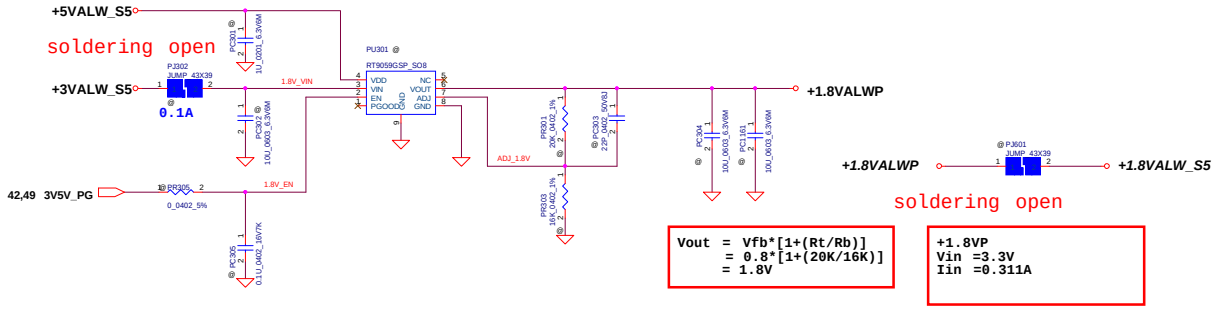
only for AMD GPU

```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.6*[1+(20K/10K)]
     = 1.8V
```

```
+1.8VALWP
Vin =5V
Iin = 2*1.8/0.85/5
    =0.84A
```

```
+1.8VALWP
Ipeak=0.514A  ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.69A
Delta  IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta  IL/Ipeak=0.26
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta  V)^2-Vout^2]
=18.3uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.65uF
```

main source : RT9059GSP
second souce: APL5933CKAI
third source : GS7166




```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(20K/16K)]
     = 1.8V
```

```
+1.8VP
Vin =3.3V
Iin =0.311A
```

Vo	1.8	V
Vin	3.3	V
Io	0.65	A
PD	0.456	W
θ JA(main) θ JA(2nd)	33.7 50	°C/W

```
+1.8VS
Ipeak=0.311A  ;
Current  Limit=3.1A(min)~3.6A(Typ)~4.2A(Max)

RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA,IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.978W
θ JA= 33.7° C/W*0.903=32.99°C
```


Compal Electronics, Inc.

Title: +1.8VSP

Size | Document Number | Rev 0.1

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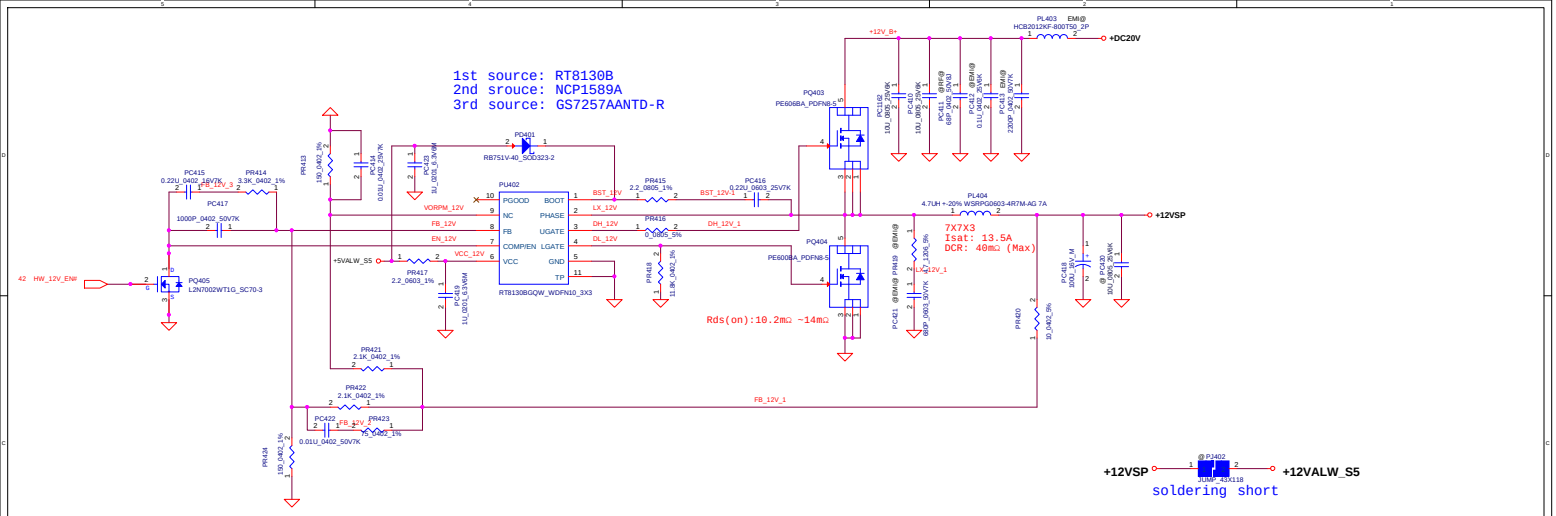


```
+12VSP
Imax=2.52A,Ipeak=3.6A   ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10.11~11.98A
Iin_ripple=0.94A
Output Cap. ESR=24mohm
Delta   Il=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta  IL/Ipeak=0.946
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=9.55uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.01uF
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 0.8*[1+(2.1K/150)]
      = 12V
```

```
+12VSP
Vin = 20V
Iin =  12*2.1/0.85/20
     = 2.42A
```


Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title: +12VSP			
Size: C	Document Number		Rev: 0.1
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+VPCH_1.0VP
Ipeak=4.49A,Imax=3.143A ; Iocp=10A~14A

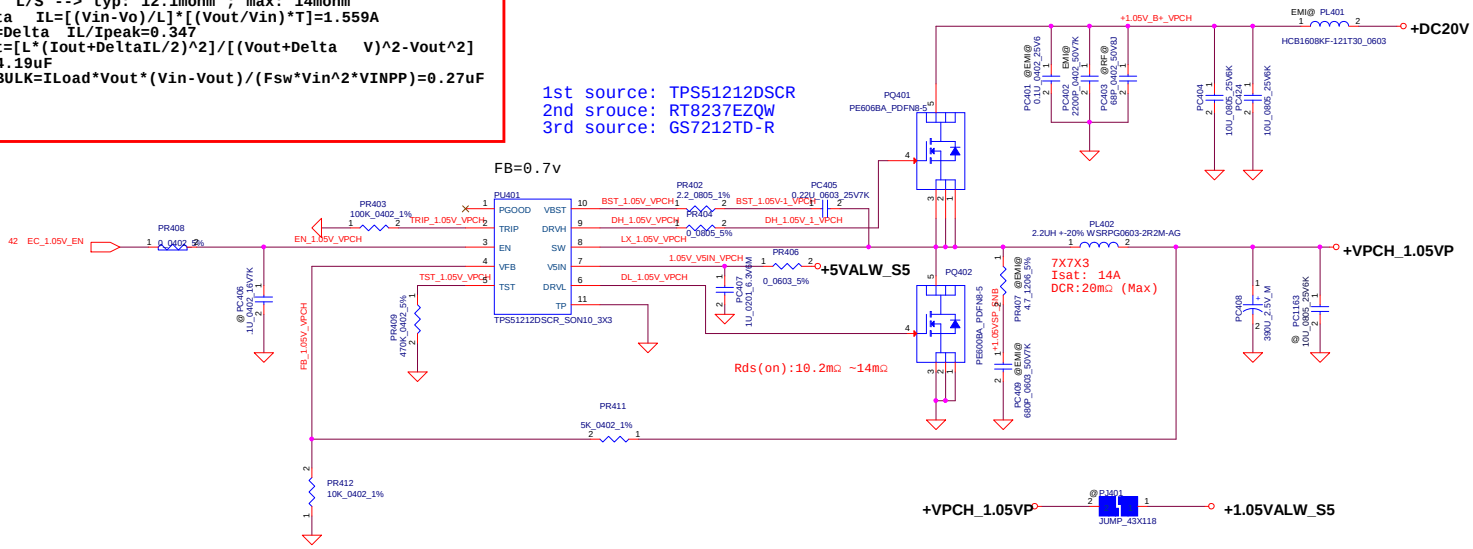
Fsw=290K
Iin_ripple= 0.75A
Output Cap. ESR=17mohm
Rds L/S --> typ: 12.1mohm ; max: 14mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.559A
LIR=Delta IL/Ipeak=0.347
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=504.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.27uF

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/10K)]
= 1.05V

+VPCH_1.0VP
Vin = 20V
Iin = 1.0*10.24/0.85/20
= 0.602A

1st source: TPS51212DSCR
2nd srouce: RT8237EZQW
3rd source: GS7212TD-R

FB=0.7v



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: +VPCH_1.0VP/+12VSP

Size	Document Number	Rev
Custom		0.1

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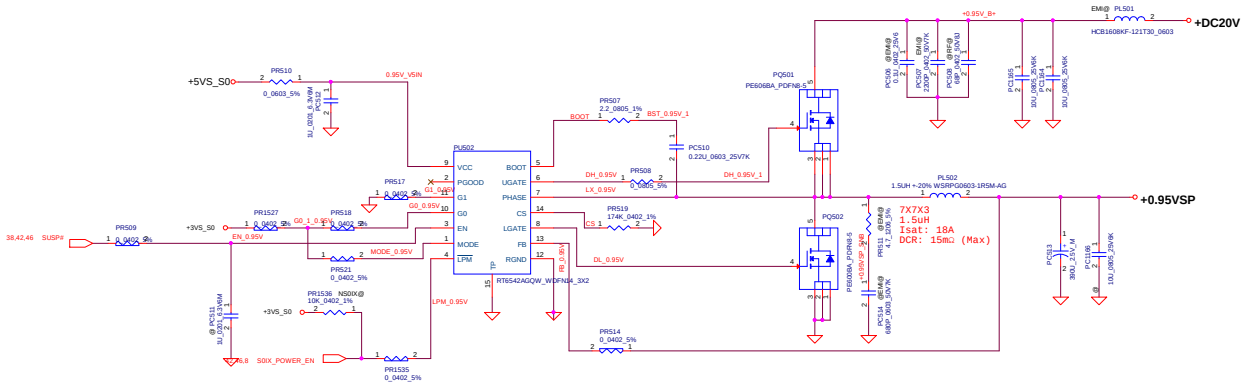


NS0IX@ for non-morden standby

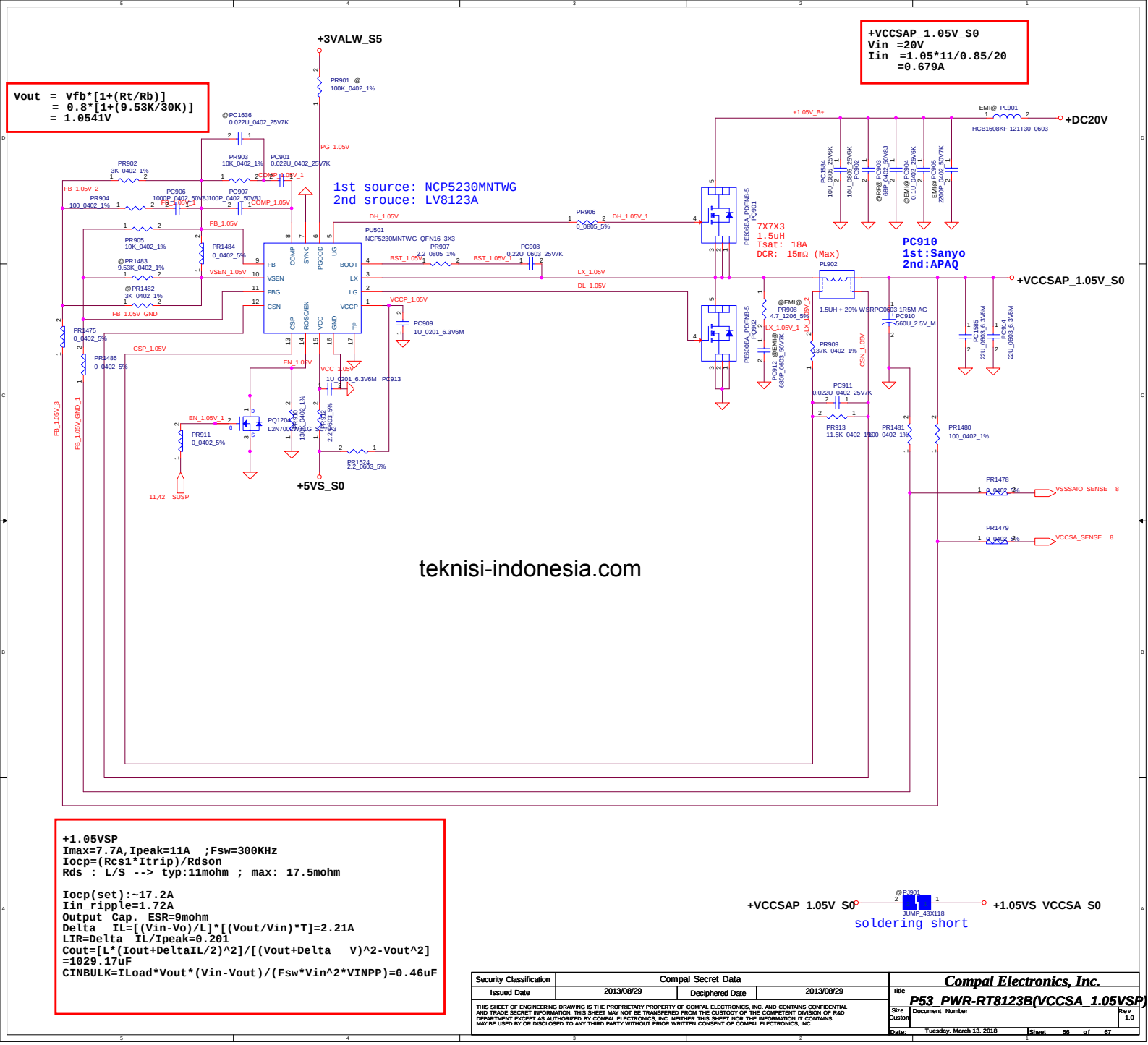
+0.95VSP
Imax=5.845,Ipeak=8.35A ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.3~13.59A
Iin_ripple=1.24A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta IL/Ipeak=0.249
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =1293.74uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.46uF

+0.95VSP
Vin = 20V
Iin =0.95*8.35/0.85/20
= 0.466A

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/14.3K)]
= 0.95V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2017/10/19

Title	+CPU_VCCIO_+0.95VSP		
Size	Document Number		Rev
Custom			0.1
Date:	Tuesday, March 13, 2018	Sheet	55 of 67



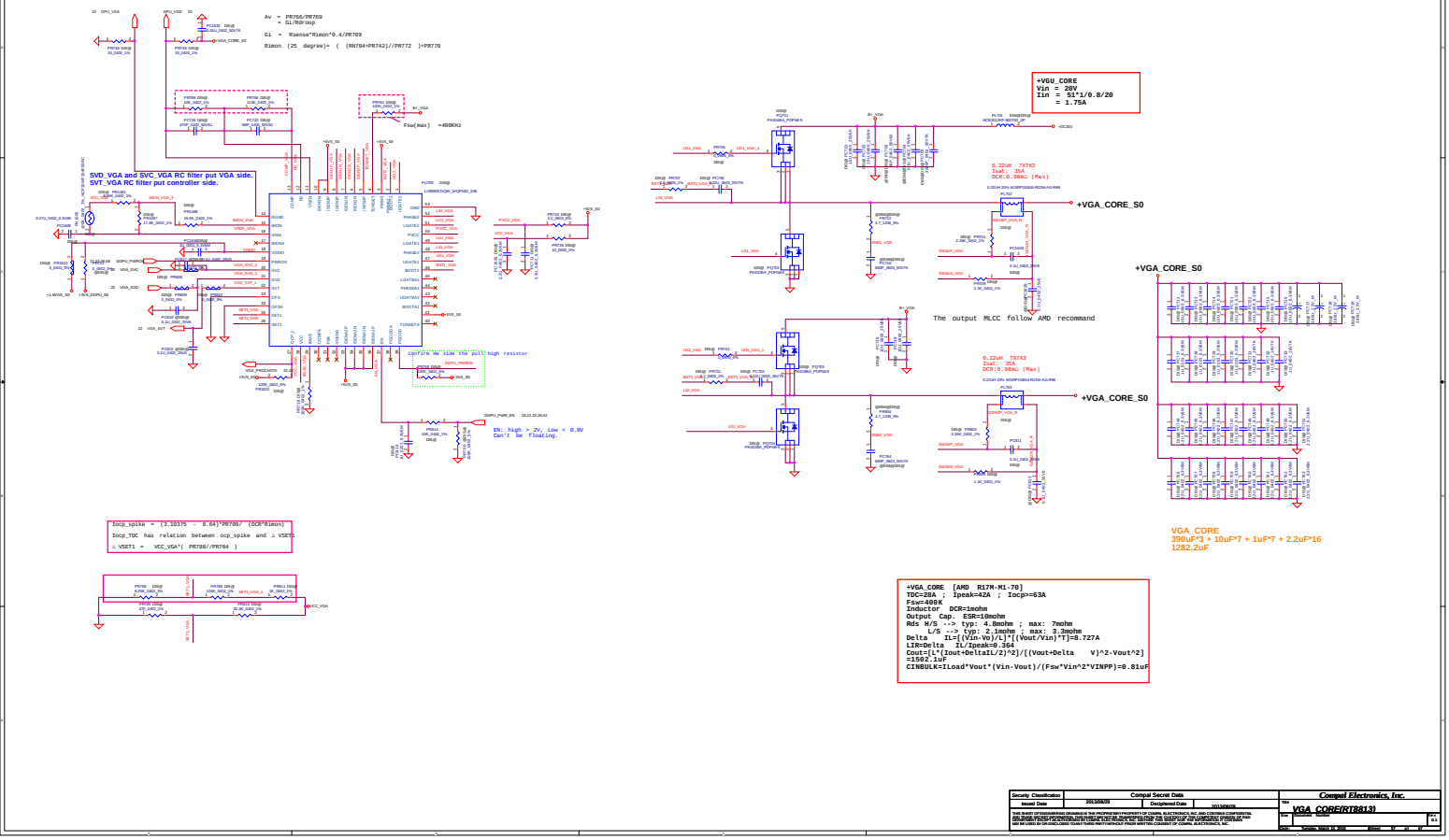
Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: P53_PWR-RT8123B(VCCSA_1.05VSP)

Size	Document Number	Rev
Custom		1.0

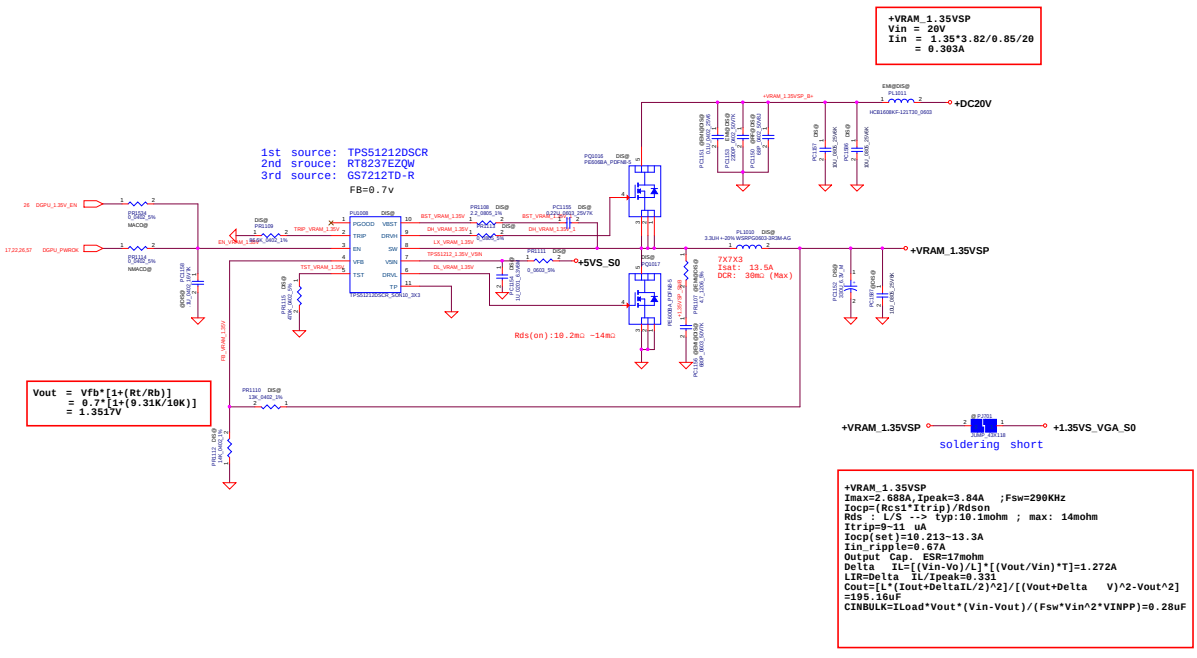
Date: Tuesday, March 13, 2018 Sheet 56 of 67



VGA_CORE
390uF*3 + 10uF*7 + 1uF*7 + 2.2uF*16
1282.2uF

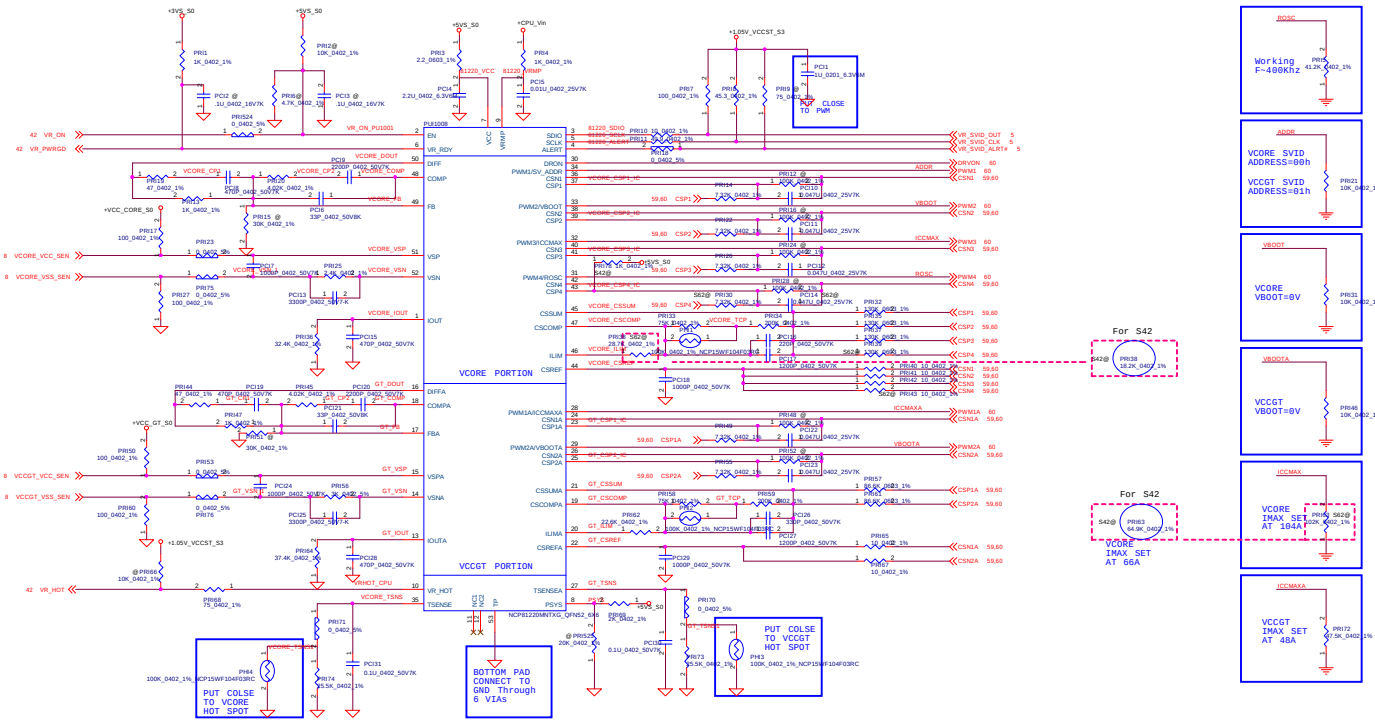
+VGA_CORE [AMD R17M-M1-70]
TDC=25A ; Ipeak=42A ; Iocp=63A
Fsw=400K
Inductor DCR=1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=8.727A
LIR=Delta IL/Ipeak=0.364
Cout=[L*(Iout+0.5*DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1592.1uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF

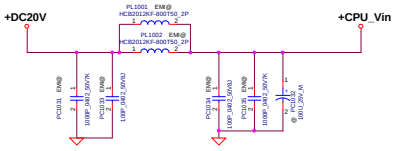
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/09	Deciphered Date	2014/08/09
Title	VGA_CORE(RT8813)		
Size	Document Number		Rev 0.3
Date: Tuesday, March 04, 2014		Sheet 57 of 67	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/29	Deciphered Date	2013/08/29
Title: VRAM_1.35V			
Size: Custom	Document Number:		Rev: 0.1
Date: Tuesday, March 11, 2014		Sheet 58 of 67	

Intel Coffeelake IMVP8 POWER CFL - S-LINE 62/42/22 35W 4+2 PHASE





CFL-S-LINE 62/42/22 35W

+CPU_CORE
TDC=74A,Ipeak=104A Fsw=400K,OCP:135A ~ 176.8A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.241
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =1110.03
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF

+GFX_CORE
TDC=34A,Ipeak=48A Fsw=400K,OCP:62.4A ~81.6A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.358
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

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Issued Date	2010/01/25	Deciphered Date	2017/10/19

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Title: **CPU_CORE_1**

Size	Document Number	Rev
Custom		0.1

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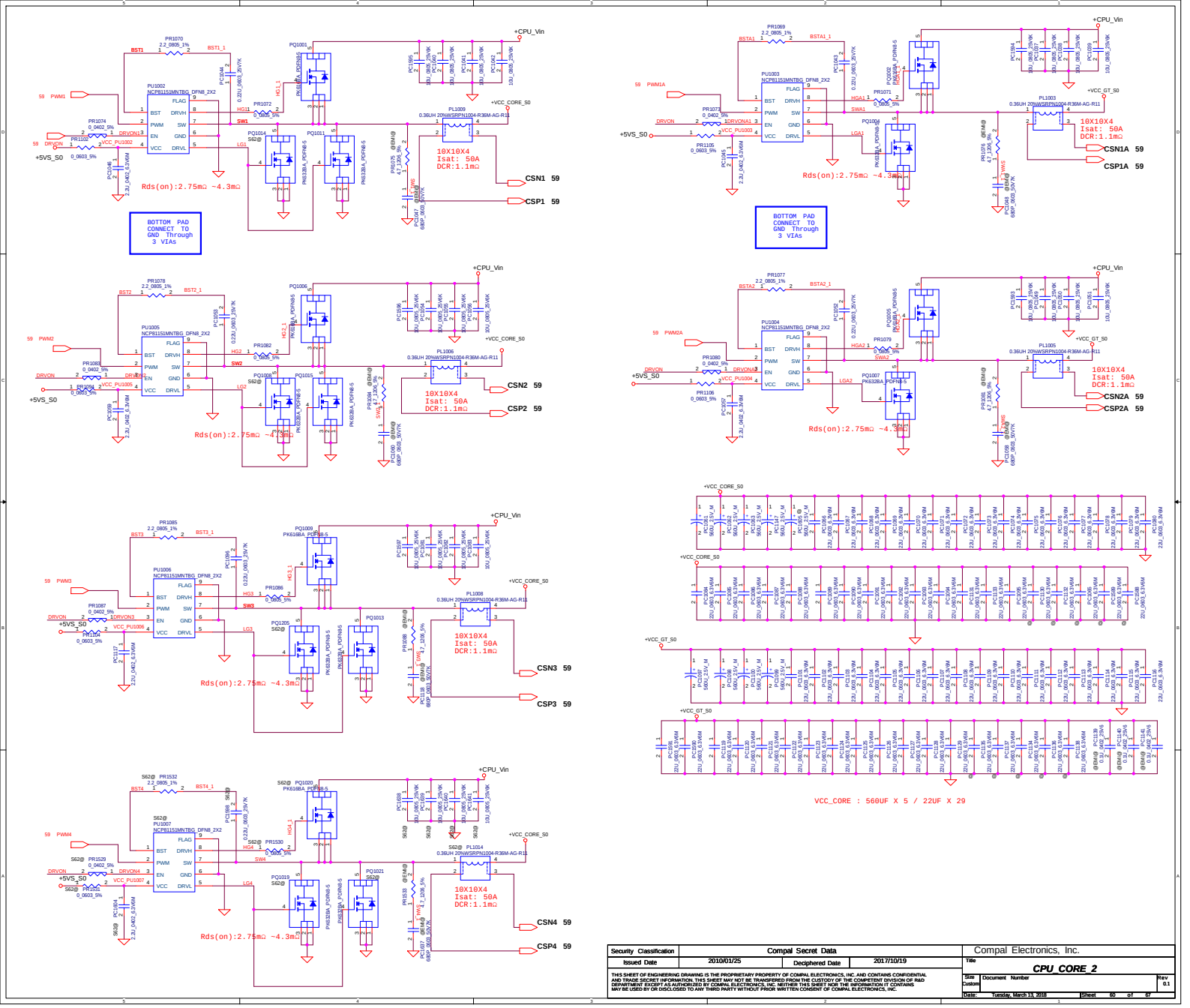
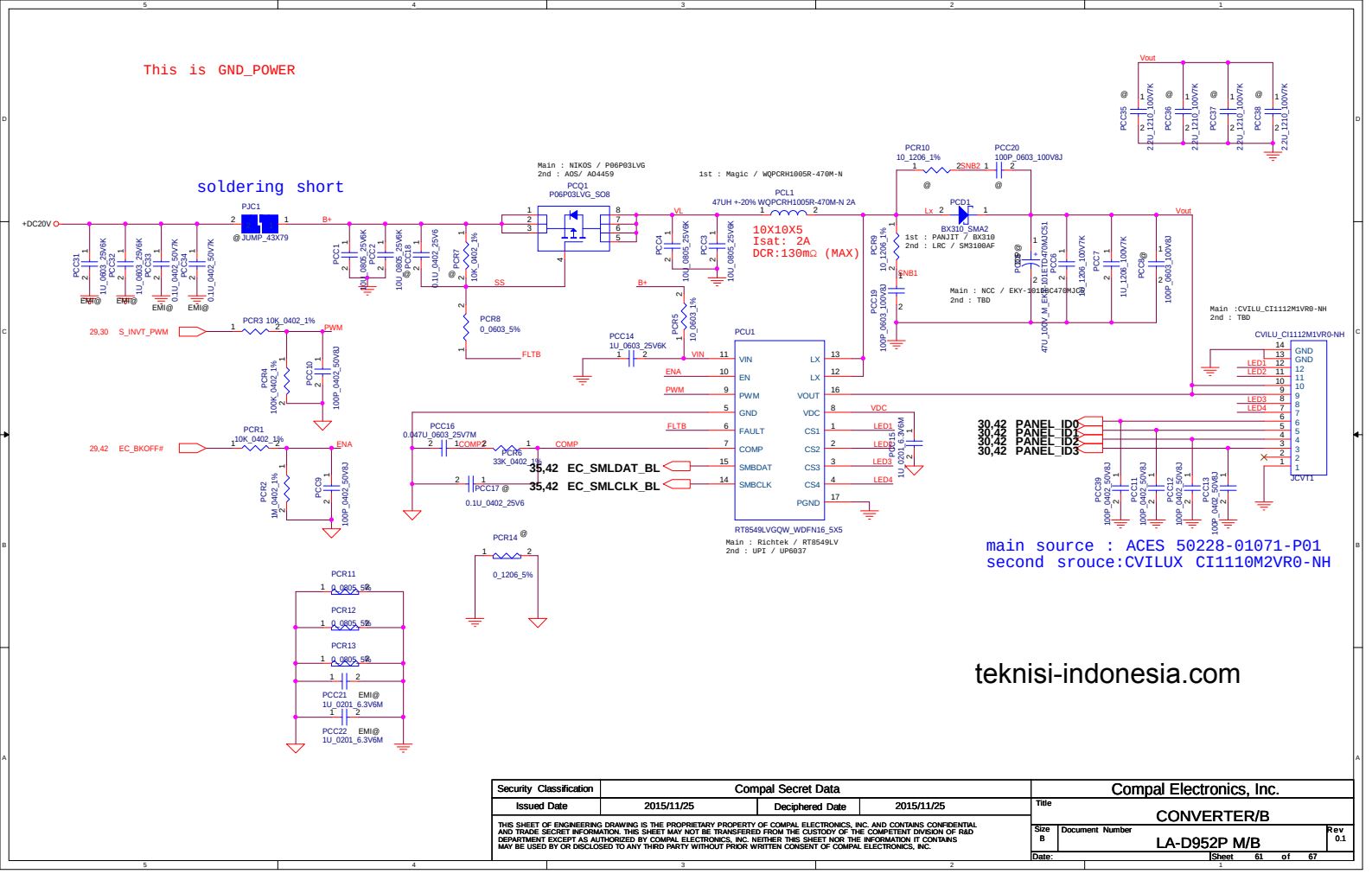
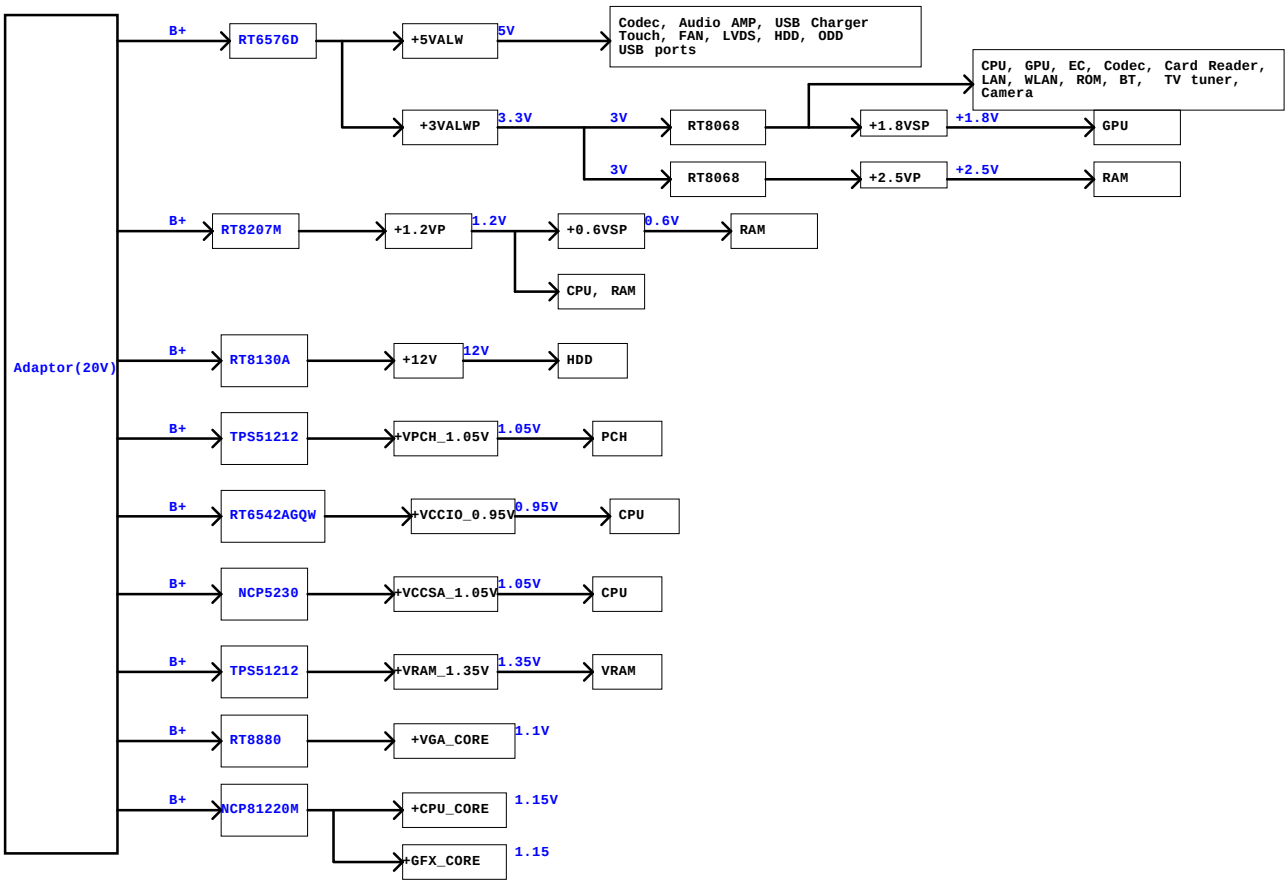


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2017/10/19
Title	CPU_CORE_2		
Size: Custom	Document Number		Rev: 0.1
Date: Tuesday, March 13, 2018	Sheet 60 of 67		



Security Classification	Compal Secret Data		
Issued Date	2015/11/25	Deciphered Date	2015/11/25

Compal Electronics, Inc.			
Title	CONVERTER/B		
Size B	Document Number	LA-D952P M/B	Rev 0.1
Date:		Sheet 61 of 67	



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: **Power Rail**

Size	Document Number	Rev
Custom		0.1

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