MS-7500 0A

CPU:

BTX(264.16mm X 266.4mm)

AMD AM2R2+ Socket940

System Chipset:

North Bridge --- AMD-ATI RX780/RS780

South Bridge --- AMD-ATI SB700

OnBoard Chipset:

Clock Gen:ICS RS475

AZALIA Codec:ADI1884

LAN(PHY):BOARDCOM 5754 (5764)

SIO:SMSC 5327

Flash ROM: 32 MB SPI (CHIP)

Main Memory:

DDRII (667/800MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 1

PWM:

Controller:ISL6323 (4-Phase 89W)

ACPI:

INTERSIL

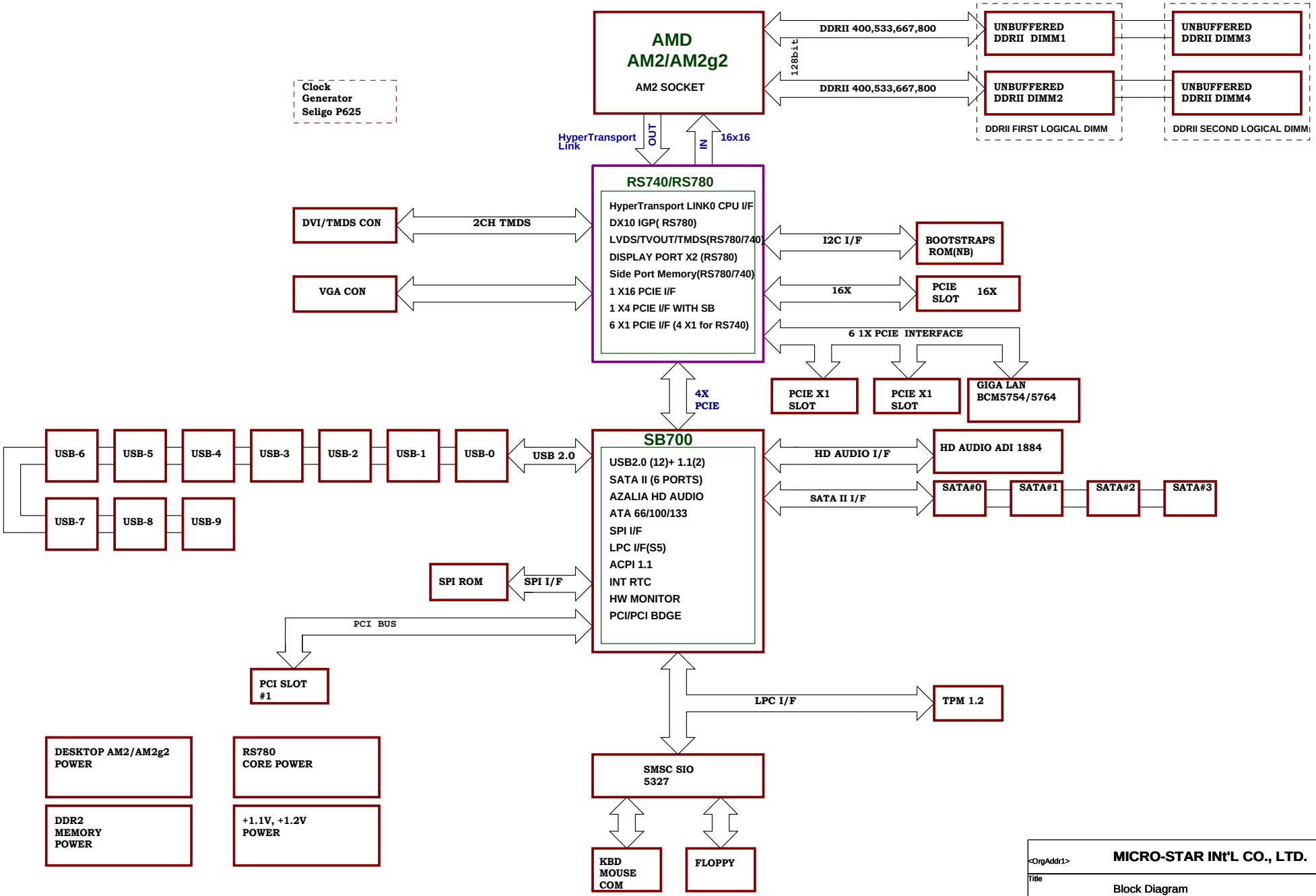
Other:

FDD *1
SATA(SATA2-300MB/s) *4
USB2.0 *10 (Rear*6 Front*4)
DVI*1
VGA PORT *1
PRINT Header *1
TPM *1
COM PORT *1
COM Header *1

<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	Cover Sheet	
Size	Document Number: MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 1 of 46	

AMD CONFIDENTIAL

RX780/RS780 + SB700 CUSTOMER DESKTOP REFERENCE DESIGN



<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	Block Diagram	
Size	Document Number: MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 2 of 46	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MA0_CLK_H0/L0 MEM_MA0_CLK_H1/L1 MEM_MA0_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MB0_CLK_H0/L0 MEM_MB0_CLK_H1/L1 MEM_MB0_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	QUAD STACK	USB0- USB0+ USB1- USB1+ USB2- USB2+ USB3- USB3+	USB_OC#0 (OC#0~1)
	LAN_USB1	USB4- USB4+ USB5- USB5+	USB_OC#1 (OC#2)
Front	FRONT USB	USB6- USB6+ USB7- USB7+	USB_OC#2 (OC#3)
	MEDIA CARD READER	USB8- USB8+ USB9- USB9+	USB_OC#3 (OC#4)

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ0# PCI_GNT0#	AD20	PCICLK2_SLOT1 (PCICLK2)
TPM				LPCCLK0
SIO				PCICLK5_SIO (PCICLK5)

PCI RESET DEVICE

SB 700	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

MICRO-STAR INt'L CO., LTD.

Title: Device Map

Size | Document Number: MS-7500 | Rev: 0A

Date: Thursday, July 12, 2007 | Sheet 3 of 46

TABLE 37
SIO8 GPIO ASSIGNMENTS

SIO GPIO	Function	Comment
GP 11	CHAFAN_PWM	Chassis Fan PWM command input, install 1K PU to +3.3 V
GP 12	RC_ID	Multi-state GPIO
GP 13	PME#	PME# from PCI slots.
GP 14	SMB Data Main	
GP 15	3V_SW_AUX	3V DUAL control
GP 16	WAKE#	PCI Express WAKE#, 1K PU to +3.3 V SB
GP 17	SMB_CLK_M	SMBus clock main
GP 21	DIAG_BEEP	Diagnostic beep signal; route to internal speaker amplifier
GP 22	CPUFAN_PWM	CPU Fan PWM command input, install 1K PU to +3.3 V
GP 23	**AUDIO_AMP_DIS#**	**To disable internal speaker.**

SIO GPIO	Function	Comment
GP 24	~~HOOD_SW_DET~~	~~Intrusion Switch Detect. Route to P125.1. Add 8.2K pullup to +3.3 V.~~
GP 25	~~HOOD_SENSE#~~	~~1M PU to SIO_BAT~~
GP 26	SKTOCC#	Route to SKTOCC# on CPU, install 10M PU to BATT, CPU occupied signal
GP 27	WAKE_OUT#	Wake Disable Output.
GP 30	LED_COLOR	Route to P5.4, front LED/button header, power LED driver
GP 31	LED_BLINK	Route to P5.2, front LED/button header, power LED driver
GP 32	TRMTRIP#	Route to Thermtrip# voltage translation, 8.2K PU to +3.3 V, CPU shutdown
GP 33	HD_LED_IN#	Route to Hard Drive LED control circuit.
GP 36	SMBCLK_THERM	SMB clock for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 37	SMBDATA_THERM	SMB data for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 40	DENSEL#	Route to P10.2, floppy connector
GP 41	HD_LED_OUT#	Hard drive LED output
GP 42	RING#	Power management output to Southbridge RI# input, 8.2K PU to +3.3 V SB
GP 43	SMB_CLK_R	SMBus clock resume
GP 44	~~HOOD_LOCK#~~	~~Route to P124.1, install 2.2K pullup to +5 V~~
GP 45	~~HOOD_UNLOCK#~~	~~Route to P124.6, install 2.2K pullup to +5 V~~
GP 46	LPC_SMI#	LPC SMI output to Southbridge, install 8.2K pull up to +3.3 V SB
GP 50	RI2#	Route to 2nd serial port RI# pin.
GP 51	DCD2#	Route to 2nd serial port DCD# pin.
GP 52	RXD2	Route to 2nd serial port RxDAT pin.
GP 53	TXD2	Route to 2nd serial port TxDAT pin.
GP 54	DSR2#	Route to 2nd serial port DSR# pin.
GP 55	RTS2#	Route to 2nd serial port RTS# pin.
GP 56	CTS2#	Route to 2nd serial port CTS# pin.
GP 57	DTR2#	Route to 2nd serial port DTR# pin.
GP 60	CLAMP_CTRL	Clamp Control Signal. Route to power bleed off transistors.
GP 61	SIO_PCIE_RST#	Reset; route to PCI Express X1 and x16 slots
GP 62	PWRBTN_IN#	Front panel power button input
GP 63	SLP_S3#	Connected to S3 sleep input from Southbridge
GP 64	SLP_S4#	Connected to SLP_S4# (not S5) sleep input from Southbridge
GP 66	PWRBTN_OUT#	Route to Southbridge PWRBTN# input
GP 67	PSON#	Power supply main voltage control; route to P1. 16, install 2.2K PU to +5 VAUX
GP 70	USB_PWR#	Connected to SLP_S5#
GP 71	SMB DATA Resume	
GP 72	5V_DUAL_Control	Controls aux voltage FET on 5V_DUAL circuit
GP 73	CHAFAN2_TACH	Power supply tach input; 4.7K PU to +3.3 V
GP 74	CHAFAN2_PWM	Power supply PWM command input; 1K PU to +3.3 V
GP 75	PWRGD_30MS	Power Good delayed 30 ms. 1K PU to + 3 V SB
GP 76	PWRGD_50MS#	Inverted Power Good delayed 50 ms. 1K PU to + 3 V SB
GP 85	CPUFAN_TACH	Tach input from CPU fan connector, 4.7K PU to +3.3 V

ATI SB700 GPIO Matrix

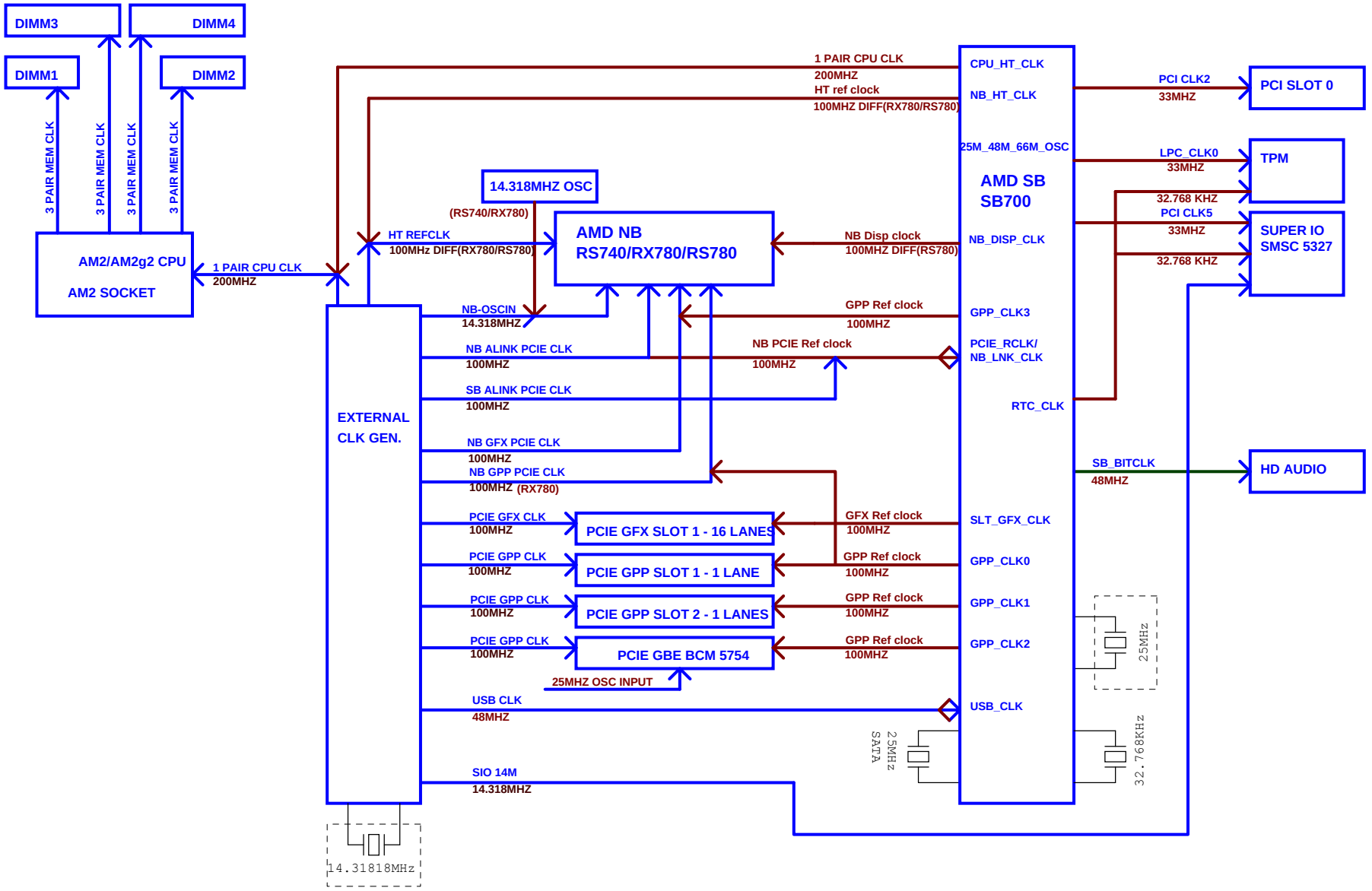
Pin Capabilities							Pin Defaults			BIOS Assignments			
Pin	GPIO	Alternate Functions	Strapping Funtion / Internal PU or PD	Input/ Output	Power Well	Voltage Tolerance	Default Signal Definition	Default Buffer Type	Default Output Level	Function	Input/ Output	Output Level	Motherboard Function
A27	GPIO 0	SSMUXSEL/SATA_IS3#		I/O/D	Vcc3_3	5		I		GPIO 0	I		BRD_ID0
~~A26~~	~~GPIO 1~~	~~ROM_CS#~~		I/O	Vcc3_3	5		I		GPIO 1	I		
B26	GPIO 2	SPKR		I/O	Vcc3_3	5		I		SPKR	O		SB600 SPKR OUT
M4	GPIO 3	FANOUT0		I/O	Vcc3_3	5		I		GPIO 3	I		BRD_ID2
B27	GPIO 4	SMARTVOLT/SATA_IS2#		I/O	Vcc3_3	5		TRI-STATE		GPIO 4	I		BRD_REV0
D23	GPIO 5	SHUTDOWN#		I/O	Vcc3_3	5		TRI-STATE		GPIO 5	I		BRD_REV1
B29	GPIO 6	GHI#/SATA_IS1#		I/OD	Vcc3_3	5		TRI-STATE		GPIO 6	I		CHASSIS_ID0
A23	GPIO 7	~~WD_PWRGD~~		I/O	Vcc3_3	5		TRI-STATE		GPIO 7	I		
C26	GPIO 8	DDC1_SDA		I/O	Vcc3_3	5		TRI-STATE		GPIO 8	I		CHASSIS_ID2
D26	GPIO 9	DDC1_SCL		I/O	Vcc3_3	5		TRI-STATE		GPIO 9	1		BRD_ID1
C28	GPIO 10	SATA_IS0#		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 10	I		CHASSIS_ID1
J6	GPIO 11	SPI_DO		I/O	VccSUS3_3	3.3		TRI-STATE		SPI_DO	O		SPI DATA-OUT
J3	GPIO 12	SPI_DI		I/O	VccSUS3_3	3.3		TRI-STATE		SPI_DI	I		SPI DATA-IN
C23	GPIO 13	LAN_RST#		OD	Vcc3_3	5		O					
G5	GPIO 14	ROM_RST#		I/O	Vcc3_3	5		O		ROM_RST#	O		LPC ROM RST#
AD28	GPIO 15	IDE_D0		I/O	Vcc3_3	5		TRI-STATE		IDE_D0	I/O		IDE_D0
AD26	GPIO 16	IDE_D1		I/O	Vcc3_3	5		TRI-STATE		IDE_D1	I/O		IDE_D1
AE29	GPIO 17	IDE_D2		I/O	Vcc3_3	5		TRI-STATE		IDE_D2	I/O		IDE_D2
AF27	GPIO 18	IDE_D3		I/O	Vcc3_3	5		TRI-STATE		IDE_D3	I/O		IDE_D3
AG29	GPIO 19	IDE_D4		I/O	Vcc3_3	5		TRI-STATE		IDE_D4	I/O		IDE_D4
AH28	GPIO 20	IDE_D5		I/O	Vcc3_3	5		TRI-STATE		IDE_D5	I/O		IDE_D5
AJ28	GPIO 21	IDE_D6		I/O	Vcc3_3	5		TRI-STATE		IDE_D6	I/O		IDE_D6
AJ27	GPIO 22	IDE_D7		I/O	Vcc3_3	5		TRI-STATE		IDE_D7	I/O		IDE_D7
AH27	GPIO 23	IDE_D8		I/O	Vcc3_3	5		TRI-STATE		IDE_D8	I/O		IDE_D8
AD27	GPIO 24	IDE_D9		I/O	Vcc3_3	5		TRI-STATE		IDE_D9	I/O		IDE_D9
AG28	GPIO 25	IDE_D10		I/O	Vcc3_3	5		TRI-STATE		IDE_D10	I/O		IDE_D10
AF28	GPIO 26	IDE_D11		I/O	Vcc3_3	5		TRI-STATE		IDE_D11	I/O		IDE_D11
AG29	GPIO 27	IDE_D12		I/O	Vcc3_3	5		TRI-STATE		IDE_D12	I/O		IDE_D12
AE28	GPIO 28	IDE_D13		I/O	Vcc3_3	5		TRI-STATE		IDE_D13	I/O		IDE_D13
AD25	GPIO 29	IDE_D14		I/O	Vcc3_3	5		TRI-STATE		IDE_D14	I/O		IDE_D14
AD29	GPIO 30	IDE_D15		I/O	Vcc3_3	5		TRI-STATE		IDE_D15	I/O		IDE_D15
G2	GPIO 31	SPI_HOLD#		I/O	VccSUS3_3	3.3		TRI-STATE		SPI_HOLD#	O		SPI HOLD#
G6	GPIO 32	SPI_CS#		I/O	VccSUS3_3	3.3		TRI-STATE		SPI_CS#	O		SPI CHIP SELECT#
AD3	GPIO 33	INTE#		I/O	Vcc3_3	5		TRI-STATE		INTE#			PCI INTE#
AF1	GPIO 34	INTF#		I/O	Vcc3_3	5		TRI-STATE		INTF#			PCI INTF#
AF4	GPIO35	INTG#		I/O	Vcc3_3	5		TRI-STATE		INTG#			PCI INTG#
AF3	GPIO36	INTH#		I/O	Vcc3_3	5		TRI-STATE		INTH#			PCI INTH#
B24	~~GPIO37~~	~~DPSLP_OD#~~	Open drain. Requires external pullup to Vcc3_3.	I/O	Vcc3_3	5		TRI-STATE					
L1	~~GPIO38~~	~~AC_BITCLK~~		I/O	Vcc3_3	5		I					
L2	GPIO39	AC_SDOUT	STRAP: high=enable debug straps, low=use hardcoded defaults	I/O	Vcc3_3	5		O					
M3	GPIO40	CLK_REQ2#/SATA_IS5#		I/O	Vcc3_3	5		I		GPIO 40	I		PWR_SUPP_DET
T1	GPIO41	PCICLK5		I/O	Vcc3_3	5		O					
L4	GPIO42	AZ_SDIN0		I/O	VccSUS3_3	3.3		I					
J2	GPIO43	AZ_SDIN1		I/O	VccSUS3_3	3.3		I					
J4	GPIO44	AZ_SDIN2		I/O	VccSUS3_3	3.3		I					
L5	~~GPIO45~~	~~AC_RST#~~		I/O	VccSUS3_3	3.3		O		GPIO 45	O		
K2	GPIO46	AZ_SDIN3		I/O	Vcc3_3	5		I		ACZ_SDIN3	I		AZALIA AUDIO IN
G3	GPIO47	SPI_CLK		I/O	VccSUS3_3	3.3		O		SPI_CLK	O		SPI CLOCK
T3	GPIO 48	FANOUT1		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 48	I		COMM_B_DET#
V4	GPIO 49	FANOUT2		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 49	I		FRONT_AUD_DET#
N3	GPIO 50	FANIN0		I/O	Vcc3_3	3.3		TRISTATE		GPIO 50	I		FRONT_USB_DET#
P2	GPIO 51	FANIN1		I/O	Vcc3_3	3.3		TRISTATE		GPIO 51	I		FLASH_SEC_OVERRIDE
W4	GPIO 52	FANIN2		I/O	Vcc3_3	3.3		TRISTATE		GPIO 52	I		PASSWORD_ENABLE
V5	GPIO 53	VIN0		I/O	Vcc3_3	3.3		TRISTATE		GPIO 53	I		BOOT_BLOCK_ENABLE
L7	GPIO 54	VIN1		I/O	Vcc3_3	3.3		TRISTATE		GPIO 54	I		BOOT_BLOCK_RECOVERY#
M8	GPIO 55	VIN2		I/O	Vcc3_3	3.3		TRISTATE					
V8	GPIO 56	VIN3		I/O	Vcc3_3	3.3		TRISTATE					
M6	GPIO 57	VIN4		I/O	Vcc3_3	3.3		TRISTATE					
P4	GPIO 58	VIN5		I/O	Vcc3_3	3.3		TRISTATE					
M7	GPIO 59	VIN6		I/O	Vcc3_3	3.3		TRISTATE					
V7	GPIO 60	VIN7		I/O	Vcc3_3	3.3		TRISTATE					
P7	GPIO 61	TEMPIN0		I/O	Vcc3_3	3.3		TRISTATE					
P8	GPIO 62	TEMPIN1		I/O	Vcc3_3	3.3		TRISTATE					
T6	GPIO 63	TEMPIN2		I/O	Vcc3_3	3.3		TRISTATE					
T7	GPIO 64	TEMPIN3/TALERT#		I/O	Vcc3_3	3.3		TRISTATE					
W22	GPIO 65	BMREQ#/REQ5#		I/O	Vcc3_3	3.3		TRISTATE		BMREQ#	I		Nortbridge BMREQ#
A4	GPIO 66	LLB#		I/O	VccSUS3_3	3.3		TRISTATE					
AC12	GPIO 67	SATA_ACT#		I/O	Vcc3_3	3.3		TRISTATE		SATA_ACT#	O		SATA LED
AH26	GPIO 68	LDRQ1#/GNT5#		I/O	Vcc3_3	5		TRISTATE		LDRQ1#	I		Previously used by LPC TPM header. Reserve for TPM?
F5	GPIO 69	RTC_IRQ#		I/O	VccSUS3_3/ VBAT	3.3		O					
AH8	GPIO 70	REQ3#		I/O	Vcc3_3	5		TRISTATE					
AH5	GPIO 71	REQ4#		I/O	Vcc3_3	5		TRISTATE					
AB12	GPIO 72	GNT3#		I/O	Vcc3_3	5		O					
AG4	GPIO 73	GNT4#		I/O	Vcc3_3	5		O					

MICRO-STAR INt'L CO., LTD.

Title: GPIO Table

Size: | Document Number: MS-7500 | Rev: 0A

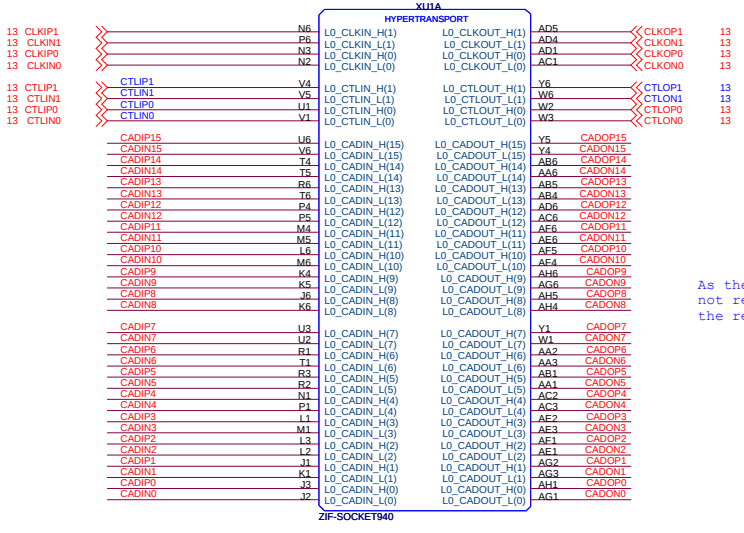
Date: Thursday, July 12, 2007 | Sheet 4 of 46



External clock mode

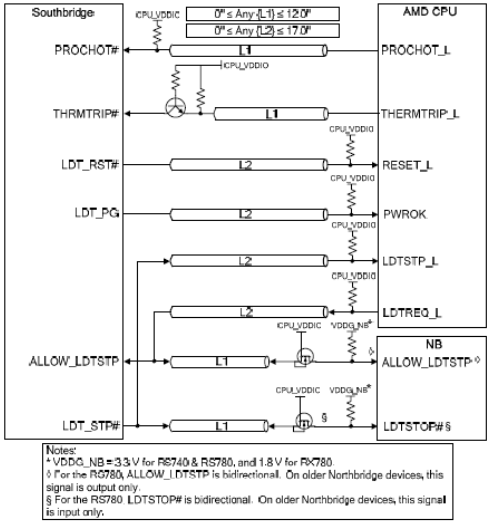
Internal clock mode

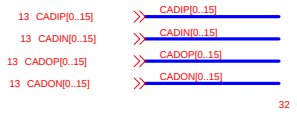
MICRO-STAR INt'L CO., LTD.		
Title: Clock Distribution		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 5 of 46	



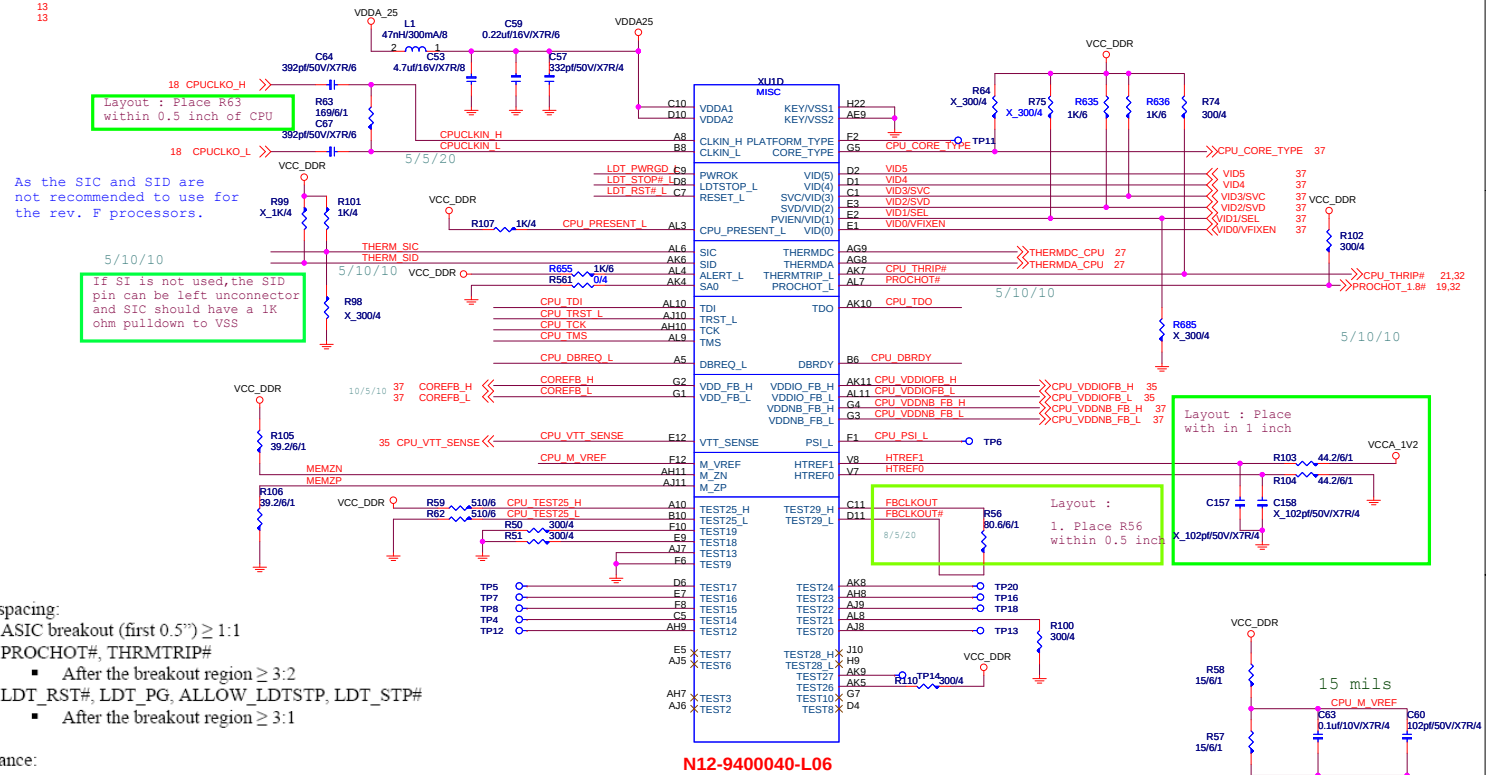
N12-9400040-L06

15u





32 CPU_PRESENT_L — CPU_PRESENT_L



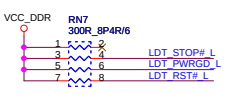
N12-9400040-L06

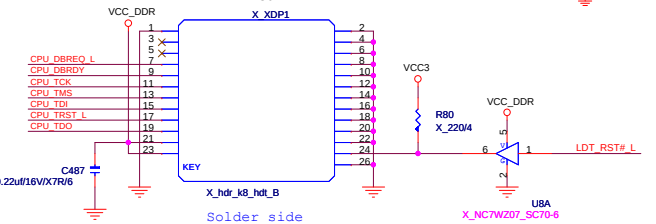
Trace spacing:

- ASIC breakout (first 0.5") ≥ 1:1
- PROCHOT#, THRMTRIP#
  - After the breakout region ≥ 3:2
- LDT_RST#, LDT_PG, ALLOW_LDTSTP, LDT_STP#
  - After the breakout region ≥ 3:1

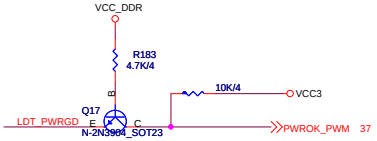
Impedance:

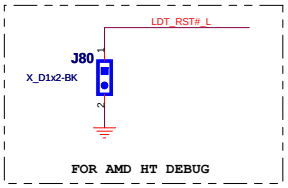
- 60 Ω ± 15%
- Reference to a solid GND or PWR plane.





For S3 issue(LDT RST can not still low)



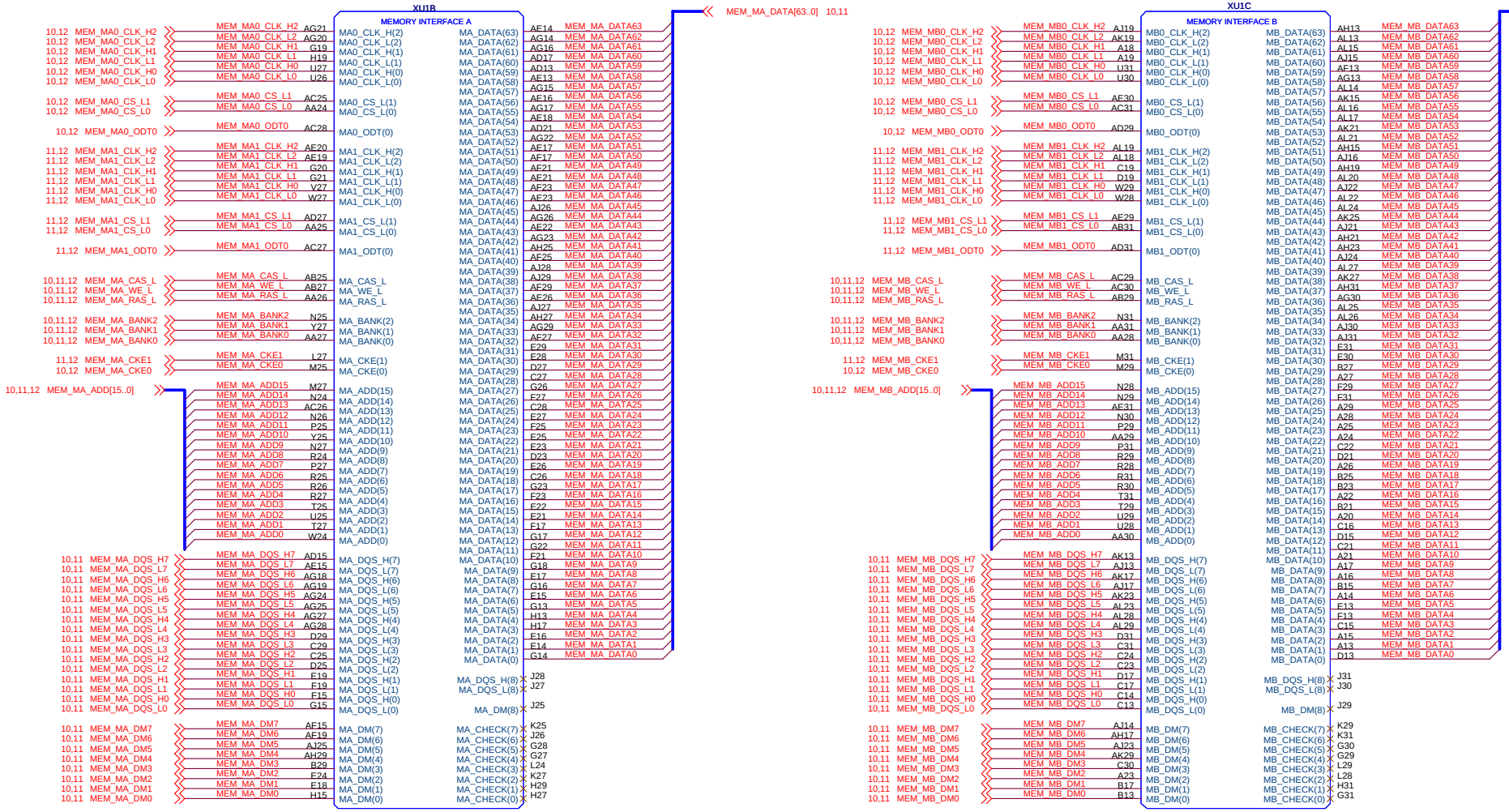


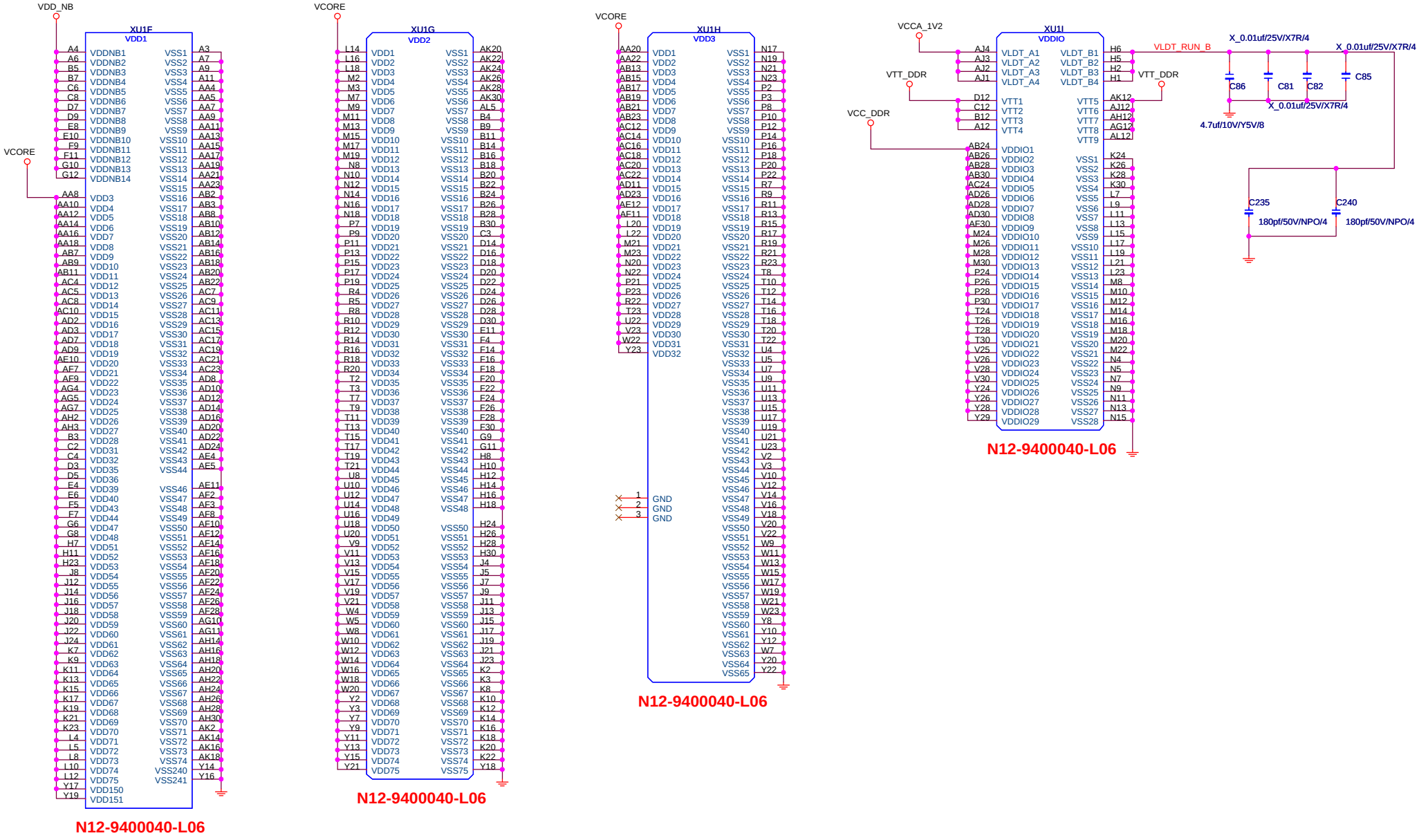
- XDP debug connector SAMTEC ASP-68200-13 or equivalent (bottom side, proto-only).

XDP1

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	GND	GND	2
3	NC	GND	4
5	NC	GND	6
7	DBREQL	GND	8
9	DBRDY	GND	10
11	TCK	GND	12
13	TMS	GND	14
15	TDI	GND	16
17	TRST_L	GND	18
19	TDO	GND	20
21	VCC_PROC	GND	22
23	VCC_PROC	LDT_RST#	24
		GND	26

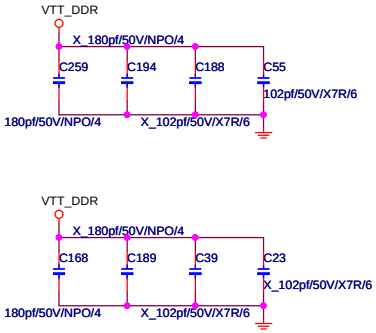
MICRO-STAR INt'L CO., LTD.			
Title: PU-HT & Straps			
Size	Document Number: MS-7500		Rev: 0A
Date: Thursday, July 12, 2007	Sheet 6 of 46		


XU1B
MEMORY INTERFACE A
MEM_MA_DATA[63..0] 10,11
MEM_MA0_CLK_H2 AG21
MEM_MA0_CLK_L2 AG20
MEM_MA0_CLK_H1 G19
MEM_MA0_CLK_L1 H19
MEM_MA0_CLK_H0 U27
MEM_MA0_CLK_L0 U26
MEM_MA0_CS_L1 AC25
MEM_MA0_CS_L0 AA24
MEM_MA0_ODT0 AC28
MEM_MA1_CLK_H2 AE20
MEM_MA1_CLK_L2 AE19
MEM_MA1_CLK_H1 G20
MEM_MA1_CLK_L1 G21
MEM_MA1_CLK_H0 V27
MEM_MA1_CLK_L0 W27
MEM_MA1_CS_L1 AD27
MEM_MA1_CS_L0 AA25
MEM_MA1_ODT0 AC27
MEM_MA_CAS_L AB25
MEM_MA_WE_L AB27
MEM_MA_RAS_L AA26
MEM_MA_BANK2 N25
MEM_MA_BANK1 Y27
MEM_MA_BANK0 AA27
MEM_MA_CKE1 L27
MEM_MA_CKE0 M25
MEM_MA_ADD15 M27
MEM_MA_ADD14 N24
MEM_MA_ADD13 AC26
MEM_MA_ADD12 N26
MEM_MA_ADD11 P25
MEM_MA_ADD10 Y25
MEM_MA_ADD9 N27
MEM_MA_ADD8 R24
MEM_MA_ADD7 P27
MEM_MA_ADD6 R25
MEM_MA_ADD5 R26
MEM_MA_ADD4 R27
MEM_MA_ADD3 T25
MEM_MA_ADD2 U25
MEM_MA_ADD1 T27
MEM_MA_ADD0 W24
MEM_MA_DQS_H7 AD15
MEM_MA_DQS_L7 AE15
MEM_MA_DQS_H6 AG18
MEM_MA_DQS_L6 AG19
MEM_MA_DQS_H5 AG24
MEM_MA_DQS_L5 AG25
MEM_MA_DQS_H4 AG27
MEM_MA_DQS_L4 AG28
MEM_MA_DQS_H3 D29
MEM_MA_DQS_L3 C29
MEM_MA_DQS_H2 C25
MEM_MA_DQS_L2 D25
MEM_MA_DQS_H1 E19
MEM_MA_DQS_L1 F19
MEM_MA_DQS_H0 F15
MEM_MA_DQS_L0 G15
MEM_MA_DM7 AF15
MEM_MA_DM6 AF19
MEM_MA_DM5 AJ25
MEM_MA_DM4 AH29
MEM_MA_DM3 B29
MEM_MA_DM2 E24
MEM_MA_DM1 E18
MEM_MA_DM0 H15
MA0_CLK_H(2)
MA0_CLK_L(2)
MA0_CLK_H(1)
MA0_CLK_L(1)
MA0_CLK_H(0)
MA0_CLK_L(0)
MA0_CS_L(1)
MA0_CS_L(0)
MA0_ODT(0)
MA1_CLK_H(2)
MA1_CLK_L(2)
MA1_CLK_H(1)
MA1_CLK_L(1)
MA1_CLK_H(0)
MA1_CLK_L(0)
MA1_CS_L(1)
MA1_CS_L(0)
MA1_ODT(0)
MA_CAS_L
MA_WE_L
MA_RAS_L
MA_BANK(2)
MA_BANK(1)
MA_BANK(0)
MA_CKE(1)
MA_CKE(0)
MA_ADD(15)
MA_ADD(14)
MA_ADD(13)
MA_ADD(12)
MA_ADD(11)
MA_ADD(10)
MA_ADD(9)
MA_ADD(8)
MA_ADD(7)
MA_ADD(6)
MA_ADD(5)
MA_ADD(4)
MA_ADD(3)
MA_ADD(2)
MA_ADD(1)
MA_ADD(0)
MA_DQS_H(7)
MA_DQS_L(7)
MA_DQS_H(6)
MA_DQS_L(6)
MA_DQS_H(5)
MA_DQS_L(5)
MA_DQS_H(4)
MA_DQS_L(4)
MA_DQS_H(3)
MA_DQS_L(3)
MA_DQS_H(2)
MA_DQS_L(2)
MA_DQS_H(1)
MA_DQS_L(1)
MA_DQS_H(0)
MA_DQS_L(0)
MA_DM(7)
MA_DM(6)
MA_DM(5)
MA_DM(4)
MA_DM(3)
MA_DM(2)
MA_DM(1)
MA_DM(0)
MA_DATA(63)
MA_DATA(62)
MA_DATA(61)
MA_DATA(60)
MA_DATA(59)
MA_DATA(58)
MA_DATA(57)
MA_DATA(56)
MA_DATA(55)
MA_DATA(54)
MA_DATA(53)
MA_DATA(52)
MA_DATA(51)
MA_DATA(50)
MA_DATA(49)
MA_DATA(48)
MA_DATA(47)
MA_DATA(46)
MA_DATA(45)
MA_DATA(44)
MA_DATA(43)
MA_DATA(42)
MA_DATA(41)
MA_DATA(40)
MA_DATA(39)
MA_DATA(38)
MA_DATA(37)
MA_DATA(36)
MA_DATA(35)
MA_DATA(34)
MA_DATA(33)
MA_DATA(32)
MA_DATA(31)
MA_DATA(30)
MA_DATA(29)
MA_DATA(28)
MA_DATA(27)
MA_DATA(26)
MA_DATA(25)
MA_DATA(24)
MA_DATA(23)
MA_DATA(22)
MA_DATA(21)
MA_DATA(20)
MA_DATA(19)
MA_DATA(18)
MA_DATA(17)
MA_DATA(16)
MA_DATA(15)
MA_DATA(14)
MA_DATA(13)
MA_DATA(12)
MA_DATA(11)
MA_DATA(10)
MA_DATA(9)
MA_DATA(8)
MA_DATA(7)
MA_DATA(6)
MA_DATA(5)
MA_DATA(4)
MA_DATA(3)
MA_DATA(2)
MA_DATA(1)
MA_DATA(0)
MA_DQS_H(8) J28
MA_DQS_L(8) J27
MA_DM(8) J25
MA_CHECK(7) K25
MA_CHECK(6) J26
MA_CHECK(5) G28
MA_CHECK(4) G27
MA_CHECK(3) L24
MA_CHECK(2) K27
MA_CHECK(1) H29
MA_CHECK(0) H27
AE14 MEM_MA_DATA63
AG14 MEM_MA_DATA62
AG16 MEM_MA_DATA61
AD17 MEM_MA_DATA60
AD13 MEM_MA_DATA59
AE13 MEM_MA_DATA58
AG15 MEM_MA_DATA57
AE16 MEM_MA_DATA56
AG17 MEM_MA_DATA55
AE18 MEM_MA_DATA54
AD21 MEM_MA_DATA53
AG22 MEM_MA_DATA52
AE17 MEM_MA_DATA51
AF17 MEM_MA_DATA50
AF21 MEM_MA_DATA49
AE21 MEM_MA_DATA48
AF23 MEM_MA_DATA47
AE23 MEM_MA_DATA46
AJ26 MEM_MA_DATA45
AG26 MEM_MA_DATA44
AE22 MEM_MA_DATA43
AG23 MEM_MA_DATA42
AH25 MEM_MA_DATA41
AF25 MEM_MA_DATA40
AJ28 MEM_MA_DATA39
AJ29 MEM_MA_DATA38
AF29 MEM_MA_DATA37
AF26 MEM_MA_DATA36
AJ27 MEM_MA_DATA35
AH27 MEM_MA_DATA34
AG29 MEM_MA_DATA33
AF27 MEM_MA_DATA32
E29 MEM_MA_DATA31
E28 MEM_MA_DATA30
D27 MEM_MA_DATA29
C27 MEM_MA_DATA28
G26 MEM_MA_DATA27
F27 MEM_MA_DATA26
C28 MEM_MA_DATA25
E27 MEM_MA_DATA24
F25 MEM_MA_DATA23
E25 MEM_MA_DATA22
F23 MEM_MA_DATA21
D23 MEM_MA_DATA20
E26 MEM_MA_DATA19
C26 MEM_MA_DATA18
G23 MEM_MA_DATA17
F23 MEM_MA_DATA16
F22 MEM_MA_DATA15
E21 MEM_MA_DATA14
F17 MEM_MA_DATA13
G17 MEM_MA_DATA12
G22 MEM_MA_DATA11
F21 MEM_MA_DATA10
G18 MEM_MA_DATA9
E17 MEM_MA_DATA8
G16 MEM_MA_DATA7
E15 MEM_MA_DATA6
G13 MEM_MA_DATA5
H13 MEM_MA_DATA4
H17 MEM_MA_DATA3
F16 MEM_MA_DATA2
E14 MEM_MA_DATA1
G14 MEM_MA_DATA0
XU1C
MEMORY INTERFACE B
MEM_MB_DATA[63..0] 10,11
MEM_MB0_CLK_H2 AJ19
MEM_MB0_CLK_L2 AK19
MEM_MB0_CLK_H1 A18
MEM_MB0_CLK_L1 A19
MEM_MB0_CLK_H0 U31
MEM_MB0_CLK_L0 U30
MEM_MB0_CS_L1 AE30
MEM_MB0_CS_L0 AC31
MEM_MB0_ODT0 AD29
MEM_MB1_CLK_H2 AL19
MEM_MB1_CLK_L2 AL18
MEM_MB1_CLK_H1 C19
MEM_MB1_CLK_L1 D19
MEM_MB1_CLK_H0 W29
MEM_MB1_CLK_L0 W28
MEM_MB1_CS_L1 AE29
MEM_MB1_CS_L0 AB31
MEM_MB1_ODT0 AD31
MEM_MB_CAS_L AC29
MEM_MB_WE_L AC30
MEM_MB_RAS_L AB29
MEM_MB_BANK2 N31
MEM_MB_BANK1 AA31
MEM_MB_BANK0 AA28
MEM_MB_CKE1 M31
MEM_MB_CKE0 M29
MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30
MEM_MB_DQS_H7 AK13
MEM_MB_DQS_L7 AJ13
MEM_MB_DQS_H6 AK17
MEM_MB_DQS_L6 AJ17
MEM_MB_DQS_H5 AK23
MEM_MB_DQS_L5 AL23
MEM_MB_DQS_H4 AL28
MEM_MB_DQS_L4 AL29
MEM_MB_DQS_H3 D31
MEM_MB_DQS_L3 C31
MEM_MB_DQS_H2 C24
MEM_MB_DQS_L2 C23
MEM_MB_DQS_H1 D17
MEM_MB_DQS_L1 C17
MEM_MB_DQS_H0 C14
MEM_MB_DQS_L0 C13
MEM_MB_DM7 AJ14
MEM_MB_DM6 AH17
MEM_MB_DM5 AJ23
MEM_MB_DM4 AK29
MEM_MB_DM3 C30
MEM_MB_DM2 A23
MEM_MB_DM1 B17
MEM_MB_DM0 B13
MB0_CLK_H(2)
MB0_CLK_L(2)
MB0_CLK_H(1)
MB0_CLK_L(1)
MB0_CLK_H(0)
MB0_CLK_L(0)
MB0_CS_L(1)
MB0_CS_L(0)
MB0_ODT(0)
MB1_CLK_H(2)
MB1_CLK_L(2)
MB1_CLK_H(1)
MB1_CLK_L(1)
MB1_CLK_H(0)
MB1_CLK_L(0)
MB1_CS_L(1)
MB1_CS_L(0)
MB1_ODT(0)
MB_CAS_L
MB_WE_L
MB_RAS_L
MB_BANK(2)
MB_BANK(1)
MB_BANK(0)
MB_CKE(1)
MB_CKE(0)
MB_ADD(15)
MB_ADD(14)
MB_ADD(13)
MB_ADD(12)
MB_ADD(11)
MB_ADD(10)
MB_ADD(9)
MB_ADD(8)
MB_ADD(7)
MB_ADD(6)
MB_ADD(5)
MB_ADD(4)
MB_ADD(3)
MB_ADD(2)
MB_ADD(1)
MB_ADD(0)
MB_DQS_H(7)
MB_DQS_L(7)
MB_DQS_H(6)
MB_DQS_L(6)
MB_DQS_H(5)
MB_DQS_L(5)
MB_DQS_H(4)
MB_DQS_L(4)
MB_DQS_H(3)
MB_DQS_L(3)
MB_DQS_H(2)
MB_DQS_L(2)
MB_DQS_H(1)
MB_DQS_L(1)
MB_DQS_H(0)
MB_DQS_L(0)
MB_DM(7)
MB_DM(6)
MB_DM(5)
MB_DM(4)
MB_DM(3)
MB_DM(2)
MB_DM(1)
MB_DM(0)
MB_DATA(63)
MB_DATA(62)
MB_DATA(61)
MB_DATA(60)
MB_DATA(59)
MB_DATA(58)
MB_DATA(57)
MB_DATA(56)
MB_DATA(55)
MB_DATA(54)
MB_DATA(53)
MB_DATA(52)
MB_DATA(51)
MB_DATA(50)
MB_DATA(49)
MB_DATA(48)
MB_DATA(47)
MB_DATA(46)
MB_DATA(45)
MB_DATA(44)
MB_DATA(43)
MB_DATA(42)
MB_DATA(41)
MB_DATA(40)
MB_DATA(39)
MB_DATA(38)
MB_DATA(37)
MB_DATA(36)
MB_DATA(35)
MB_DATA(34)
MB_DATA(33)
MB_DATA(32)
MB_DATA(31)
MB_DATA(30)
MB_DATA(29)
MB_DATA(28)
MB_DATA(27)
MB_DATA(26)
MB_DATA(25)
MB_DATA(24)
MB_DATA(23)
MB_DATA(22)
MB_DATA(21)
MB_DATA(20)
MB_DATA(19)
MB_DATA(18)
MB_DATA(17)
MB_DATA(16)
MB_DATA(15)
MB_DATA(14)
MB_DATA(13)
MB_DATA(12)
MB_DATA(11)
MB_DATA(10)
MB_DATA(9)
MB_DATA(8)
MB_DATA(7)
MB_DATA(6)
MB_DATA(5)
MB_DATA(4)
MB_DATA(3)
MB_DATA(2)
MB_DATA(1)
MB_DATA(0)
MB_DQS_H(8) J31
MB_DQS_L(8) J30
MB_DM(8) J29
MB_CHECK(7) K29
MB_CHECK(6) K31
MB_CHECK(5) G30
MB_CHECK(4) G29
MB_CHECK(3) L29
MB_CHECK(2) L28
MB_CHECK(1) H31
MB_CHECK(0) G31
AH13 MEM_MB_DATA63
AL13 MEM_MB_DATA62
AL15 MEM_MB_DATA61
AJ15 MEM_MB_DATA60
AF13 MEM_MB_DATA59
AG13 MEM_MB_DATA58
AL14 MEM_MB_DATA57
AK15 MEM_MB_DATA56
AL16 MEM_MB_DATA55
AL17 MEM_MB_DATA54
AK21 MEM_MB_DATA53
AL21 MEM_MB_DATA52
AH15 MEM_MB_DATA51
AJ16 MEM_MB_DATA50
AH19 MEM_MB_DATA49
AL20 MEM_MB_DATA48
AJ22 MEM_MB_DATA47
AL22 MEM_MB_DATA46
AL24 MEM_MB_DATA45
AK25 MEM_MB_DATA44
AJ21 MEM_MB_DATA43
AH21 MEM_MB_DATA42
AH23 MEM_MB_DATA41
AJ24 MEM_MB_DATA40
AL27 MEM_MB_DATA39
AK27 MEM_MB_DATA38
AH31 MEM_MB_DATA37
AG30 MEM_MB_DATA36
AL25 MEM_MB_DATA35
AL26 MEM_MB_DATA34
AJ30 MEM_MB_DATA33
AJ31 MEM_MB_DATA32
E31 MEM_MB_DATA31
E30 MEM_MB_DATA30
B27 MEM_MB_DATA29
A27 MEM_MB_DATA28
F29 MEM_MB_DATA27
F31 MEM_MB_DATA26
A29 MEM_MB_DATA25
A28 MEM_MB_DATA24
A25 MEM_MB_DATA23
A24 MEM_MB_DATA22
C22 MEM_MB_DATA21
D21 MEM_MB_DATA20
A26 MEM_MB_DATA19
B25 MEM_MB_DATA18
B23 MEM_MB_DATA17
A22 MEM_MB_DATA16
B21 MEM_MB_DATA15
A20 MEM_MB_DATA14
C16 MEM_MB_DATA13
D15 MEM_MB_DATA12
C21 MEM_MB_DATA11
A21 MEM_MB_DATA10
A17 MEM_MB_DATA9
A16 MEM_MB_DATA8
B15 MEM_MB_DATA7
A14 MEM_MB_DATA6
E13 MEM_MB_DATA5
F13 MEM_MB_DATA4
C15 MEM_MB_DATA3
A15 MEM_MB_DATA2
A13 MEM_MB_DATA1
D13 MEM_MB_DATA0
N12-9400040-L06
N12-9400040-L06
MICRO-STAR INt'L CO., LTD.
Title
CPU-Memory
Size
Document Number
MS-7500
Rev 0A
Date: Thursday, July 12, 2007
Sheet 7 of 46

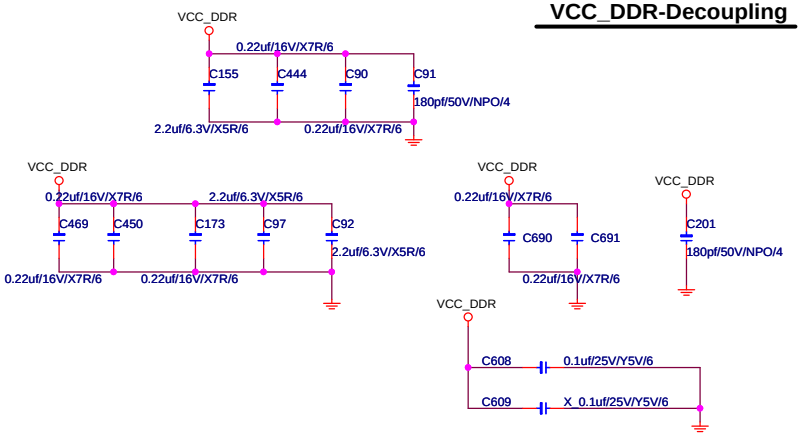


MICRO-STAR INt'L CO., LTD.			
Title: CPU-Power & GND			
Size	Document Number: MS-7500		Rev: 0A
Date: Thursday, July 12, 2007	Sheet 8 of 46		

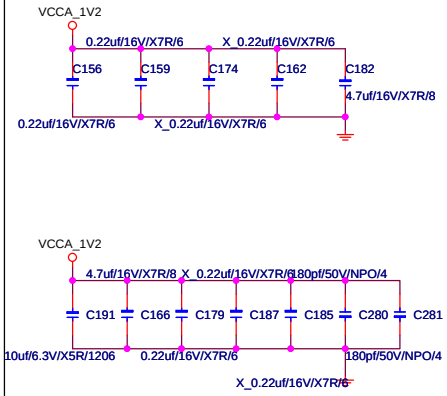
VTT_DDR-Decoupling

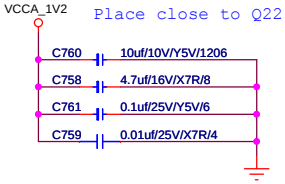


VCC_DDR-Decoupling

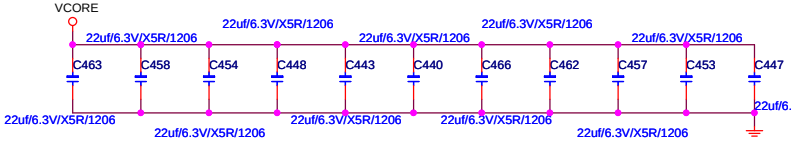


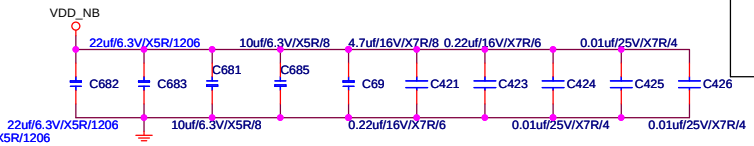
VCCA_1V2-Decoupling

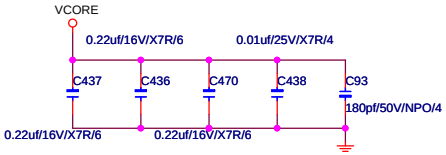


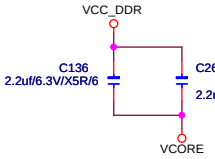


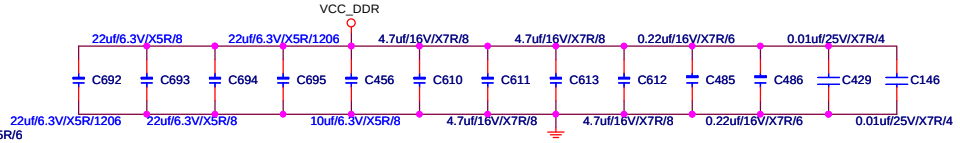
VCORE-Decoupling

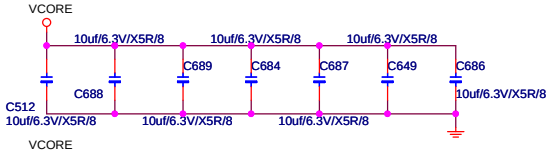


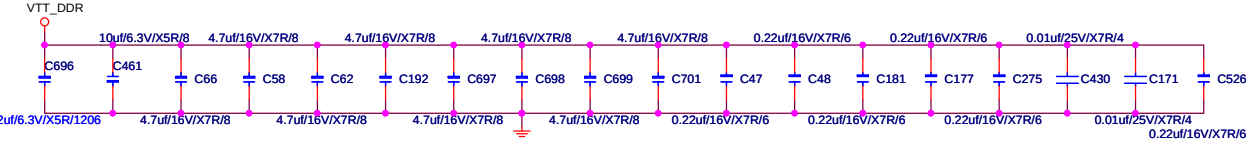


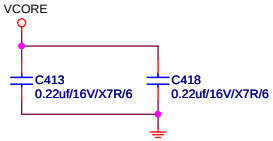


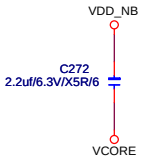


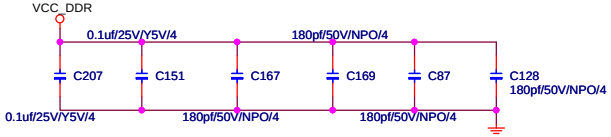


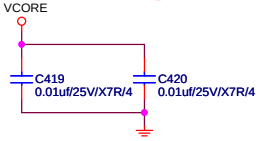


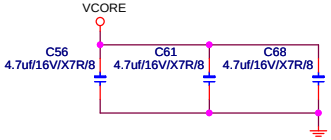




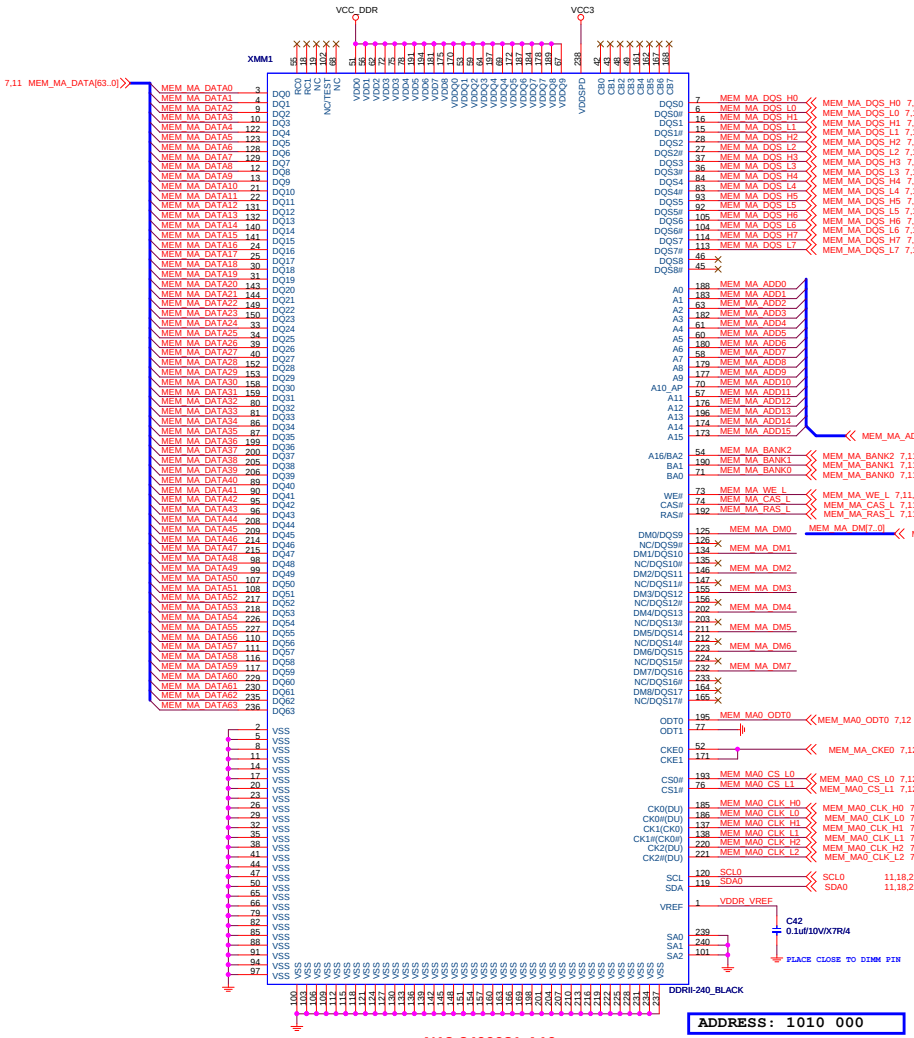


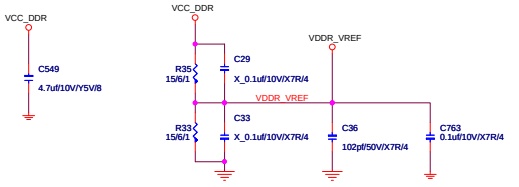


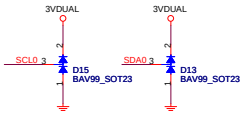


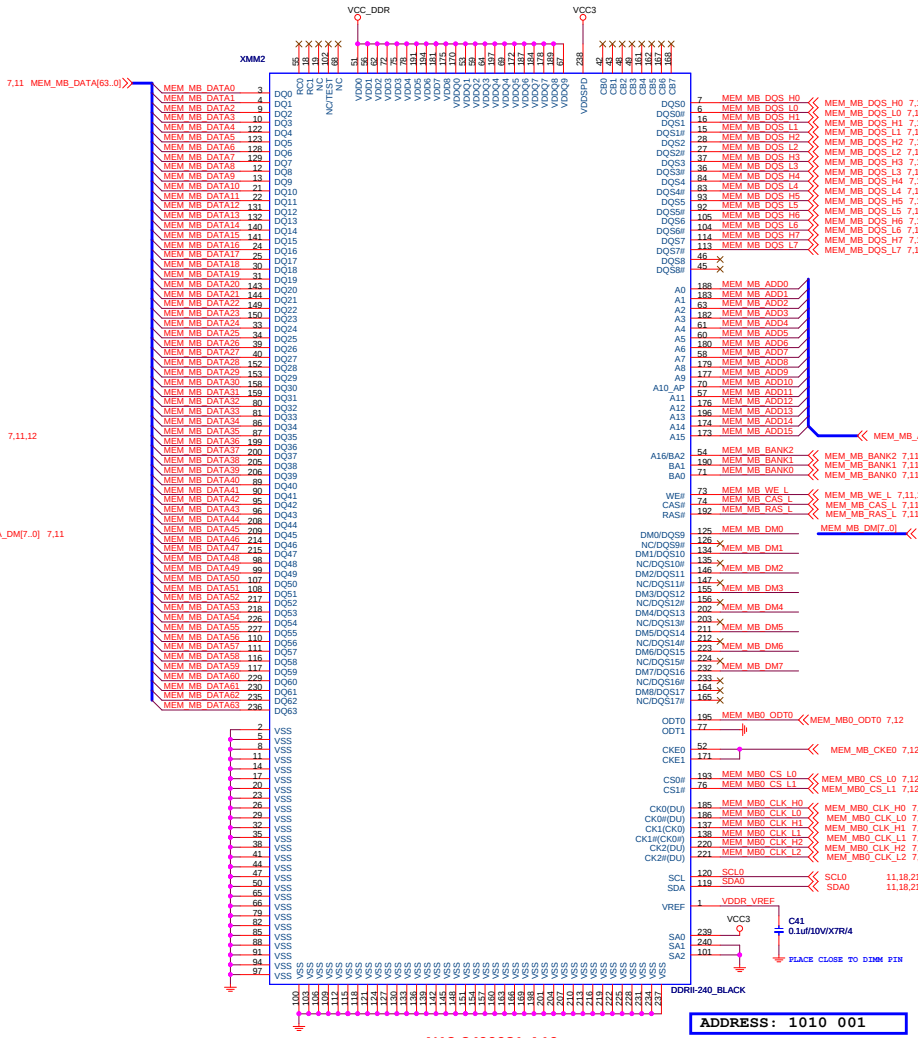


MICRO-STAR INt'L CO., LTD.		
Title: CPU-Decoupling		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 9 of 46	

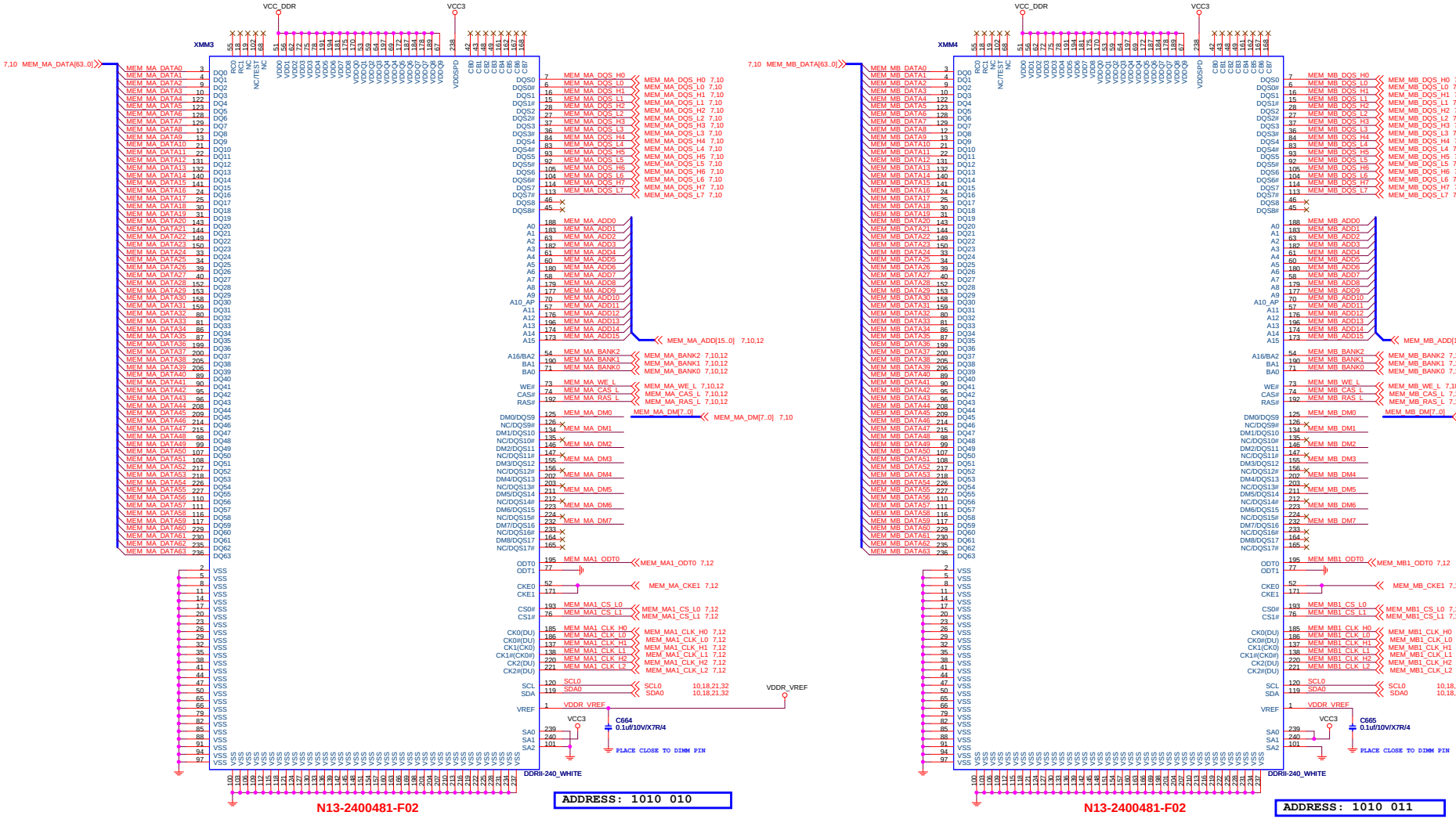




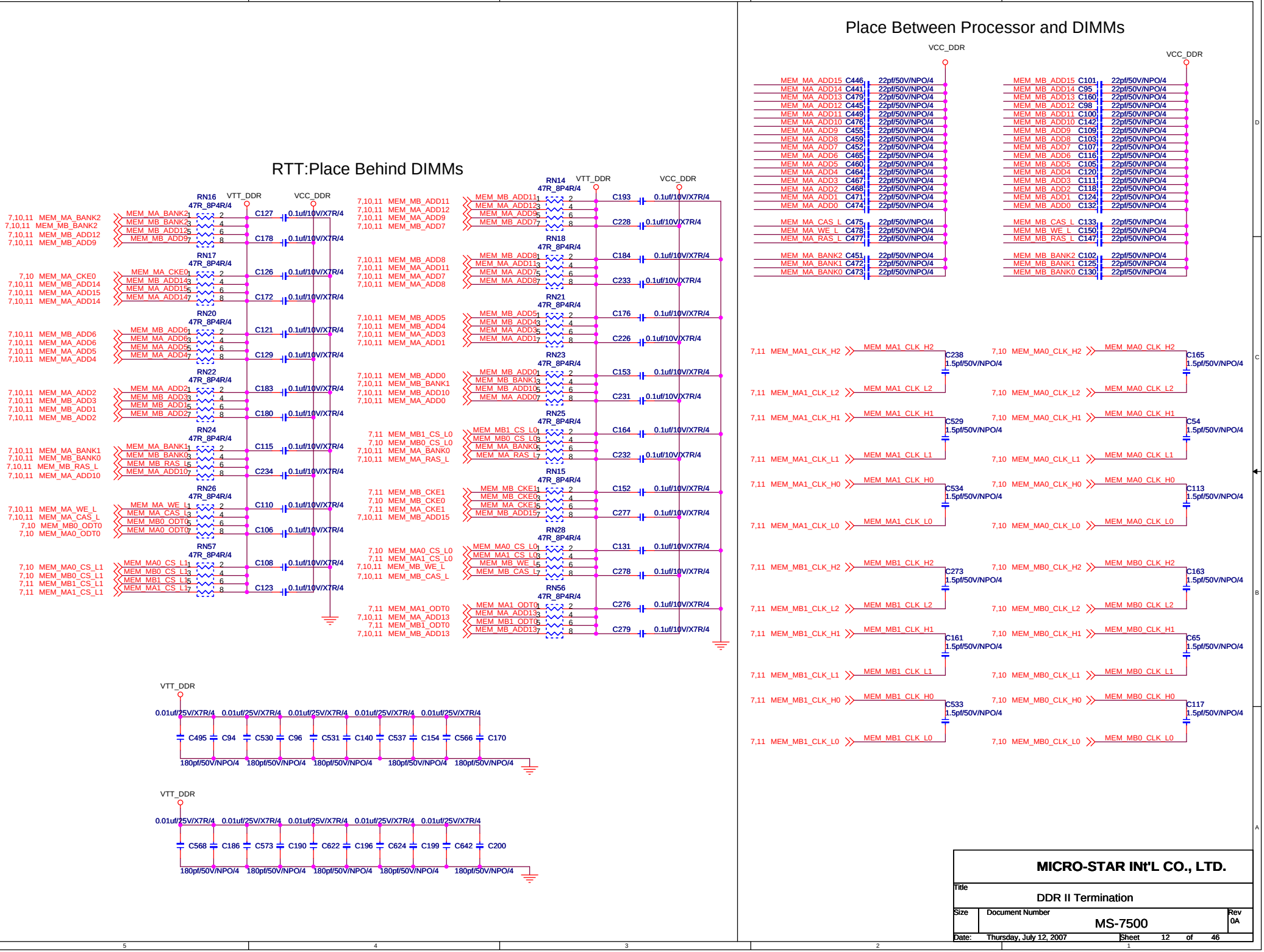


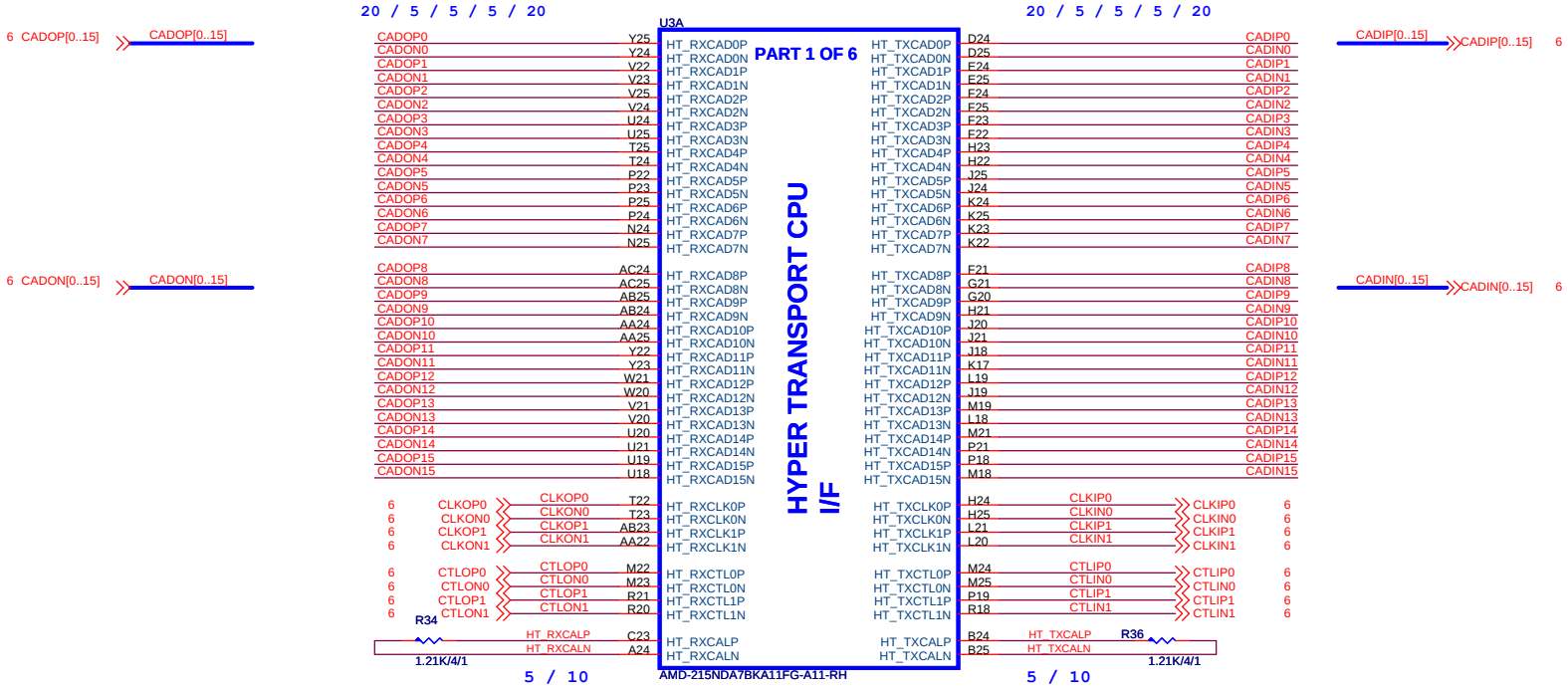


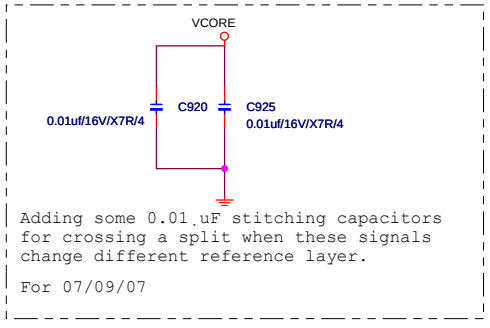
MICRO-STAR INt'L CO., LTD.		
Title: FIRST LOGICAL DDR DIMM		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 10 of 46	



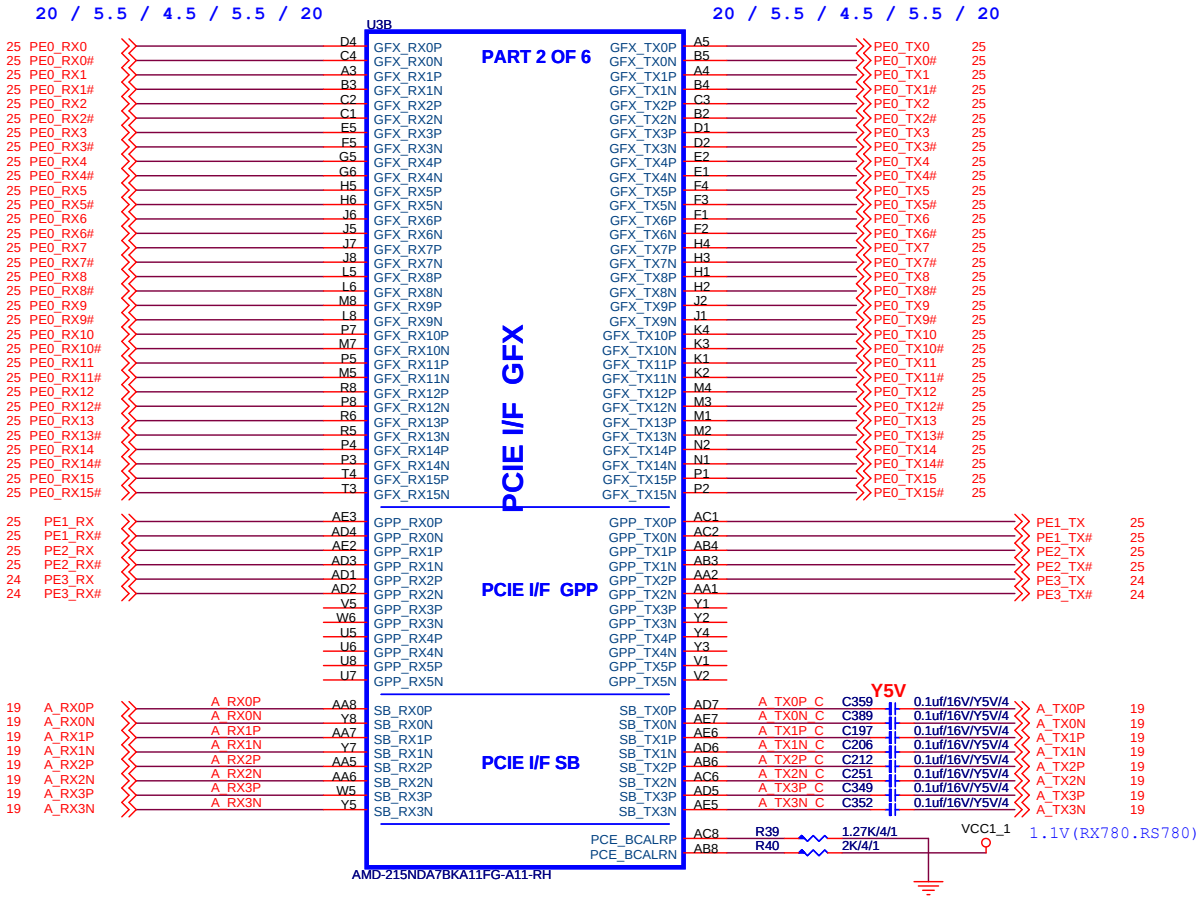
MICRO-STAR INt'L CO., LTD.			
Title: SECOND LOGICAL DDR DIMM			
Size	Document Number: MS-7500		Rev: 0A
Date: Thursday, July 12, 2007	Sheet 11 of 46		

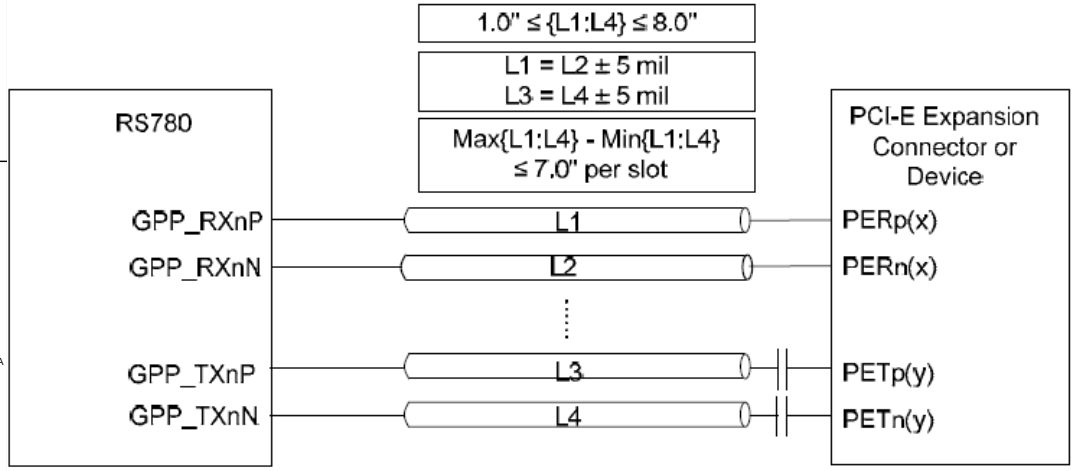

RTT:Place Behind DIMMs
Place Between Processor and DIMMs
VTT_DDR
VCC_DDR
RN16
47R_8P4R/4
RN17
RN20
RN22
RN24
RN26
RN57
RN14
RN18
RN21
RN23
RN25
RN15
RN28
RN56
7,10,11 MEM_MA_BANK2
7,10,11 MEM_MB_BANK2
7,10,11 MEM_MB_ADD12
7,10,11 MEM_MB_ADD9
MEM_MA_BANK2
MEM_MB_BANK2
MEM_MB_ADD12
MEM_MB_ADD9
C127
C178
0.1uf/10V/X7R/4
7,10 MEM_MA_CKE0
7,10,11 MEM_MB_ADD14
7,10,11 MEM_MA_ADD15
7,10,11 MEM_MA_ADD14
MEM_MA_CKE0
MEM_MB_ADD14
MEM_MA_ADD15
MEM_MA_ADD14
C126
C172
7,10,11 MEM_MB_ADD6
7,10,11 MEM_MA_ADD6
7,10,11 MEM_MA_ADD5
7,10,11 MEM_MA_ADD4
MEM_MB_ADD6
MEM_MA_ADD6
MEM_MA_ADD5
MEM_MA_ADD4
C121
C129
7,10,11 MEM_MA_ADD2
7,10,11 MEM_MB_ADD3
7,10,11 MEM_MB_ADD1
7,10,11 MEM_MB_ADD2
MEM_MA_ADD2
MEM_MB_ADD3
MEM_MB_ADD1
MEM_MB_ADD2
C183
C180
7,10,11 MEM_MA_BANK1
7,10,11 MEM_MB_BANK0
7,10,11 MEM_MB_RAS_L
7,10,11 MEM_MA_ADD10
MEM_MA_BANK1
MEM_MB_BANK0
MEM_MB_RAS_L
MEM_MA_ADD10
C115
C234
7,10,11 MEM_MA_WE_L
7,10,11 MEM_MA_CAS_L
7,10 MEM_MB0_ODT0
7,10 MEM_MA0_ODT0
MEM_MA_WE_L
MEM_MA_CAS_L
MEM_MB0_ODT0
MEM_MA0_ODT0
C110
C106
7,10 MEM_MA0_CS_L1
7,10 MEM_MB0_CS_L1
7,11 MEM_MB1_CS_L1
7,11 MEM_MA1_CS_L1
MEM_MA0_CS_L1
MEM_MB0_CS_L1
MEM_MB1_CS_L1
MEM_MA1_CS_L1
C108
C123
7,10,11 MEM_MB_ADD11
7,10,11 MEM_MA_ADD12
7,10,11 MEM_MA_ADD9
7,10,11 MEM_MB_ADD7
MEM_MB_ADD11
MEM_MA_ADD12
MEM_MA_ADD9
MEM_MB_ADD7
C193
C228
7,10,11 MEM_MB_ADD8
7,10,11 MEM_MA_ADD11
7,10,11 MEM_MA_ADD7
7,10,11 MEM_MA_ADD8
MEM_MB_ADD8
MEM_MA_ADD11
MEM_MA_ADD7
MEM_MA_ADD8
C184
C233
7,10,11 MEM_MB_ADD5
7,10,11 MEM_MB_ADD4
7,10,11 MEM_MA_ADD3
7,10,11 MEM_MA_ADD1
MEM_MB_ADD5
MEM_MB_ADD4
MEM_MA_ADD3
MEM_MA_ADD1
C176
C226
7,10,11 MEM_MB_ADD0
7,10,11 MEM_MB_BANK1
7,10,11 MEM_MB_ADD10
7,10,11 MEM_MA_ADD0
MEM_MB_ADD0
MEM_MB_BANK1
MEM_MB_ADD10
MEM_MA_ADD0
C153
C231
7,11 MEM_MB1_CS_L0
7,10 MEM_MB0_CS_L0
7,10,11 MEM_MA_BANK0
7,10,11 MEM_MA_RAS_L
MEM_MB1_CS_L0
MEM_MB0_CS_L0
MEM_MA_BANK0
MEM_MA_RAS_L
C164
C232
7,11 MEM_MB_CKE1
7,10 MEM_MB_CKE0
7,11 MEM_MA_CKE1
7,10,11 MEM_MB_ADD15
MEM_MB_CKE1
MEM_MB_CKE0
MEM_MA_CKE1
MEM_MB_ADD15
C152
C277
7,10 MEM_MA0_CS_L0
7,11 MEM_MA1_CS_L0
7,10,11 MEM_MB_WE_L
7,10,11 MEM_MB_CAS_L
MEM_MA0_CS_L0
MEM_MA1_CS_L0
MEM_MB_WE_L
MEM_MB_CAS_L
C131
C278
7,11 MEM_MA1_ODT0
7,10,11 MEM_MA_ADD13
7,11 MEM_MB1_ODT0
7,10,11 MEM_MB_ADD13
MEM_MA1_ODT0
MEM_MA_ADD13
MEM_MB1_ODT0
MEM_MB_ADD13
C276
C279
0.01uf/25V/X7R/4
C495 C94 C530 C96 C531 C140 C537 C154 C566 C170
180pf/50V/NPO/4
C568 C186 C573 C190 C622 C196 C624 C199 C642 C200
MEM_MA_ADD15 C446
MEM_MA_ADD14 C441
MEM_MA_ADD13 C479
MEM_MA_ADD12 C445
MEM_MA_ADD11 C449
MEM_MA_ADD10 C476
MEM_MA_ADD9 C455
MEM_MA_ADD8 C459
MEM_MA_ADD7 C452
MEM_MA_ADD6 C465
MEM_MA_ADD5 C460
MEM_MA_ADD4 C464
MEM_MA_ADD3 C467
MEM_MA_ADD2 C468
MEM_MA_ADD1 C471
MEM_MA_ADD0 C474
MEM_MA_CAS_L C475
MEM_MA_WE_L C478
MEM_MA_RAS_L C477
MEM_MA_BANK2 C451
MEM_MA_BANK1 C472
MEM_MA_BANK0 C473
22pf/50V/NPO/4
MEM_MB_ADD15 C101
MEM_MB_ADD14 C95
MEM_MB_ADD13 C160
MEM_MB_ADD12 C98
MEM_MB_ADD11 C100
MEM_MB_ADD10 C142
MEM_MB_ADD9 C109
MEM_MB_ADD8 C103
MEM_MB_ADD7 C107
MEM_MB_ADD6 C116
MEM_MB_ADD5 C105
MEM_MB_ADD4 C120
MEM_MB_ADD3 C111
MEM_MB_ADD2 C118
MEM_MB_ADD1 C124
MEM_MB_ADD0 C132
MEM_MB_CAS_L C133
MEM_MB_WE_L C150
MEM_MB_RAS_L C147
MEM_MB_BANK2 C102
MEM_MB_BANK1 C125
MEM_MB_BANK0 C130
7,11 MEM_MA1_CLK_H2
7,11 MEM_MA1_CLK_L2
7,11 MEM_MA1_CLK_H1
7,11 MEM_MA1_CLK_L1
7,11 MEM_MA1_CLK_H0
7,11 MEM_MA1_CLK_L0
MEM_MA1_CLK_H2
MEM_MA1_CLK_L2
MEM_MA1_CLK_H1
MEM_MA1_CLK_L1
MEM_MA1_CLK_H0
MEM_MA1_CLK_L0
C238
C529
C534
1.5pf/50V/NPO/4
7,10 MEM_MA0_CLK_H2
7,10 MEM_MA0_CLK_L2
7,10 MEM_MA0_CLK_H1
7,10 MEM_MA0_CLK_L1
7,10 MEM_MA0_CLK_H0
7,10 MEM_MA0_CLK_L0
MEM_MA0_CLK_H2
MEM_MA0_CLK_L2
MEM_MA0_CLK_H1
MEM_MA0_CLK_L1
MEM_MA0_CLK_H0
MEM_MA0_CLK_L0
C165
C54
C113
7,11 MEM_MB1_CLK_H2
7,11 MEM_MB1_CLK_L2
7,11 MEM_MB1_CLK_H1
7,11 MEM_MB1_CLK_L1
7,11 MEM_MB1_CLK_H0
7,11 MEM_MB1_CLK_L0
MEM_MB1_CLK_H2
MEM_MB1_CLK_L2
MEM_MB1_CLK_H1
MEM_MB1_CLK_L1
MEM_MB1_CLK_H0
MEM_MB1_CLK_L0
C273
C161
C533
7,10 MEM_MB0_CLK_H2
7,10 MEM_MB0_CLK_L2
7,10 MEM_MB0_CLK_H1
7,10 MEM_MB0_CLK_L1
7,10 MEM_MB0_CLK_H0
7,10 MEM_MB0_CLK_L0
MEM_MB0_CLK_H2
MEM_MB0_CLK_L2
MEM_MB0_CLK_H1
MEM_MB0_CLK_L1
MEM_MB0_CLK_H0
MEM_MB0_CLK_L0
C163
C65
C117
MICRO-STAR INt'L CO., LTD.
Title
DDR II Termination
Size
Document Number
MS-7500
Rev
0A
Date: Thursday, July 12, 2007
Sheet 12 of 46





MICRO-STAR INt'L CO., LTD.		
Title: RS780/RX780-HT LINK I/F		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 13 of 46	





RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

MICRO-STAR INt'L CO., LTD.		
Title: RX780/RS780-PCIE I/F		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 14 of 46	

RX740/RS740/RS780 difference table

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RX780/RS740/RS780 JTAG PIN MAPPING

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)

RX780: pin DFT_GPIO5
RS780: pin VSYNC

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

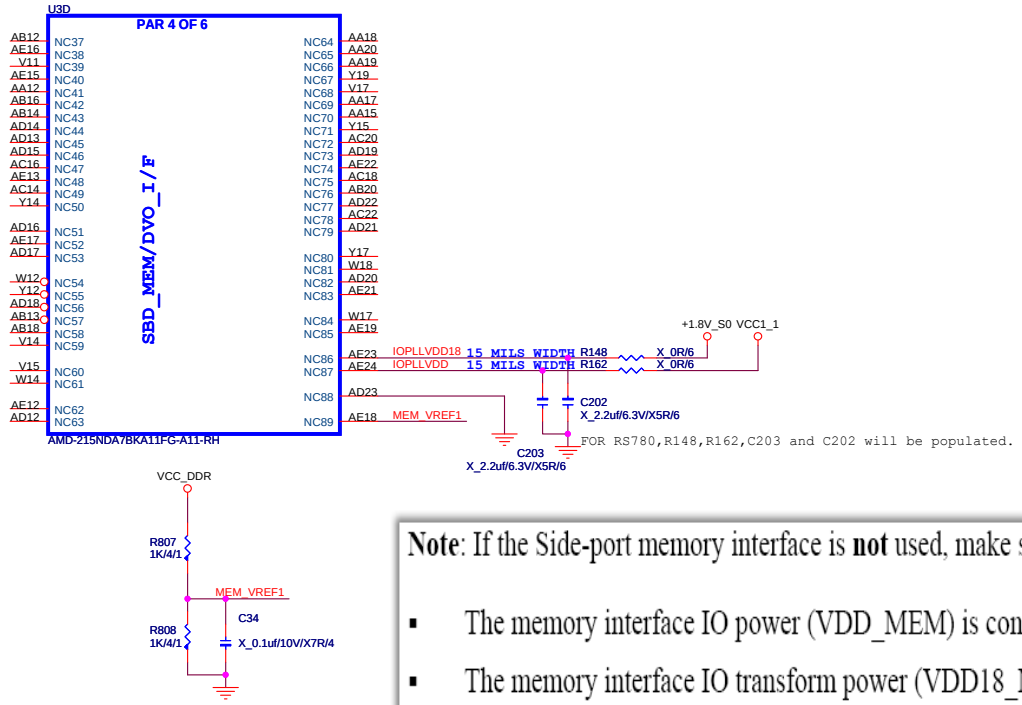
RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Appicable

Note: for RS780, change R198 to 150R as AUX_CAL, place close to pin C8

Title	RX780/RS780-SYSTEM I/F
Size	Document Number: MS-7500
Rev	0A
Date:	Thursday, July 12, 2007
Sheet	15 of 46

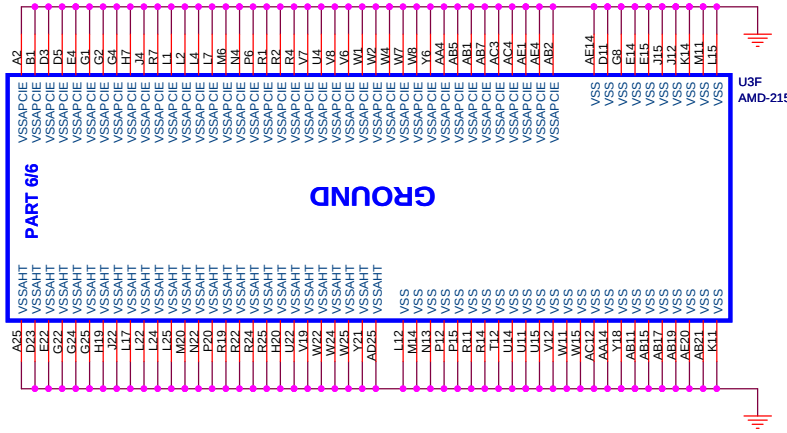
MICRO-STAR INt'L CO., LTD.



Note: If the Side-port memory interface is **not** used, make sure that:

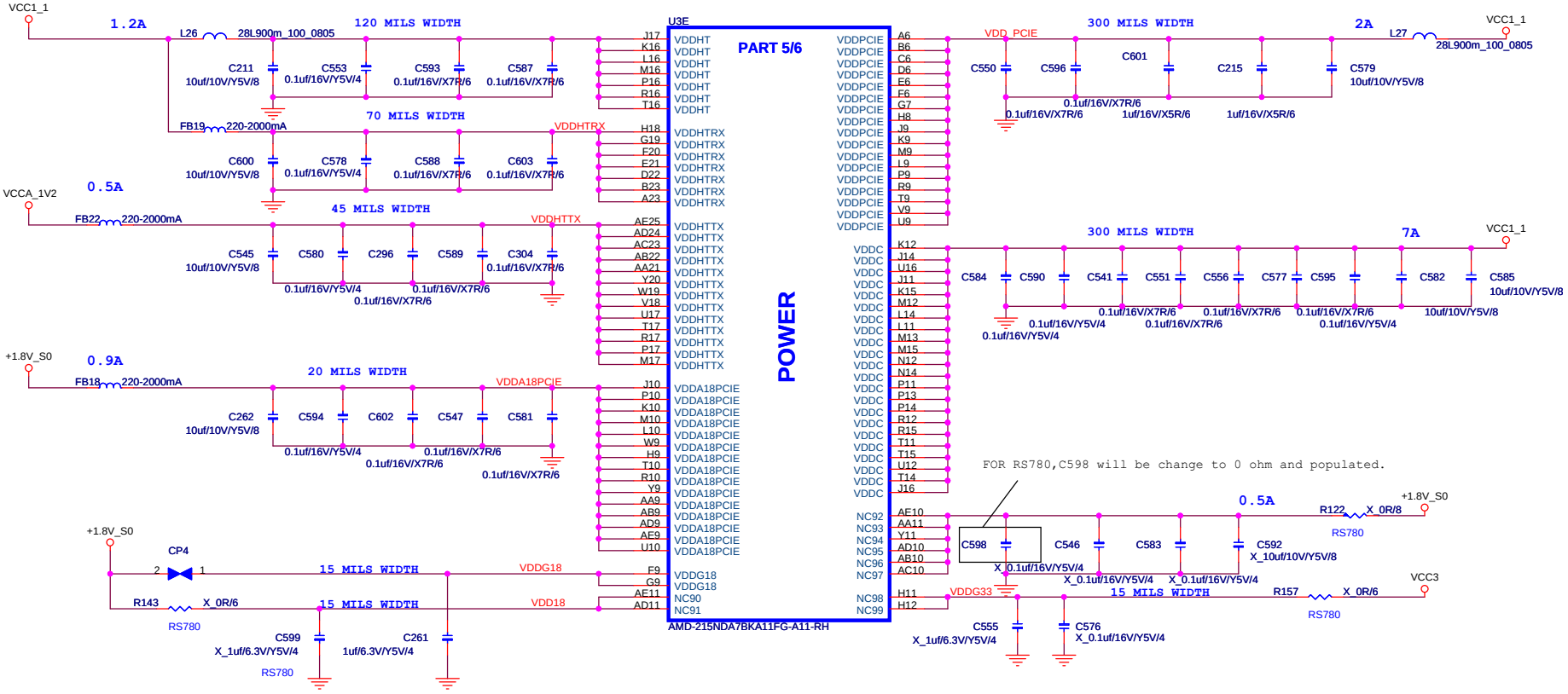
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

MICRO-STAR INt'L CO., LTD.		
Title: SPMEM/STRAPS		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 16 of 46	



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

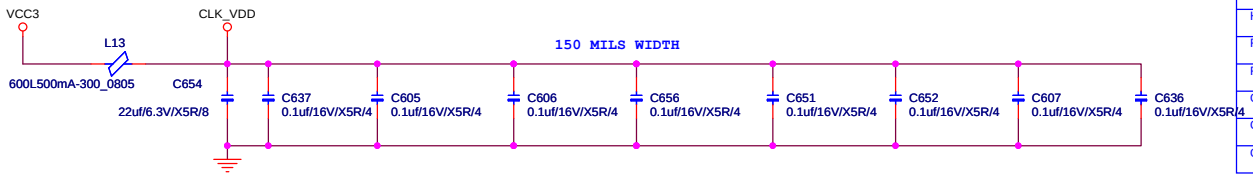


MICRO-STAR INt'L CO., LTD.		
Title	RX780/RS780-POWER	
Size	Document Number MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 17 of 46	

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

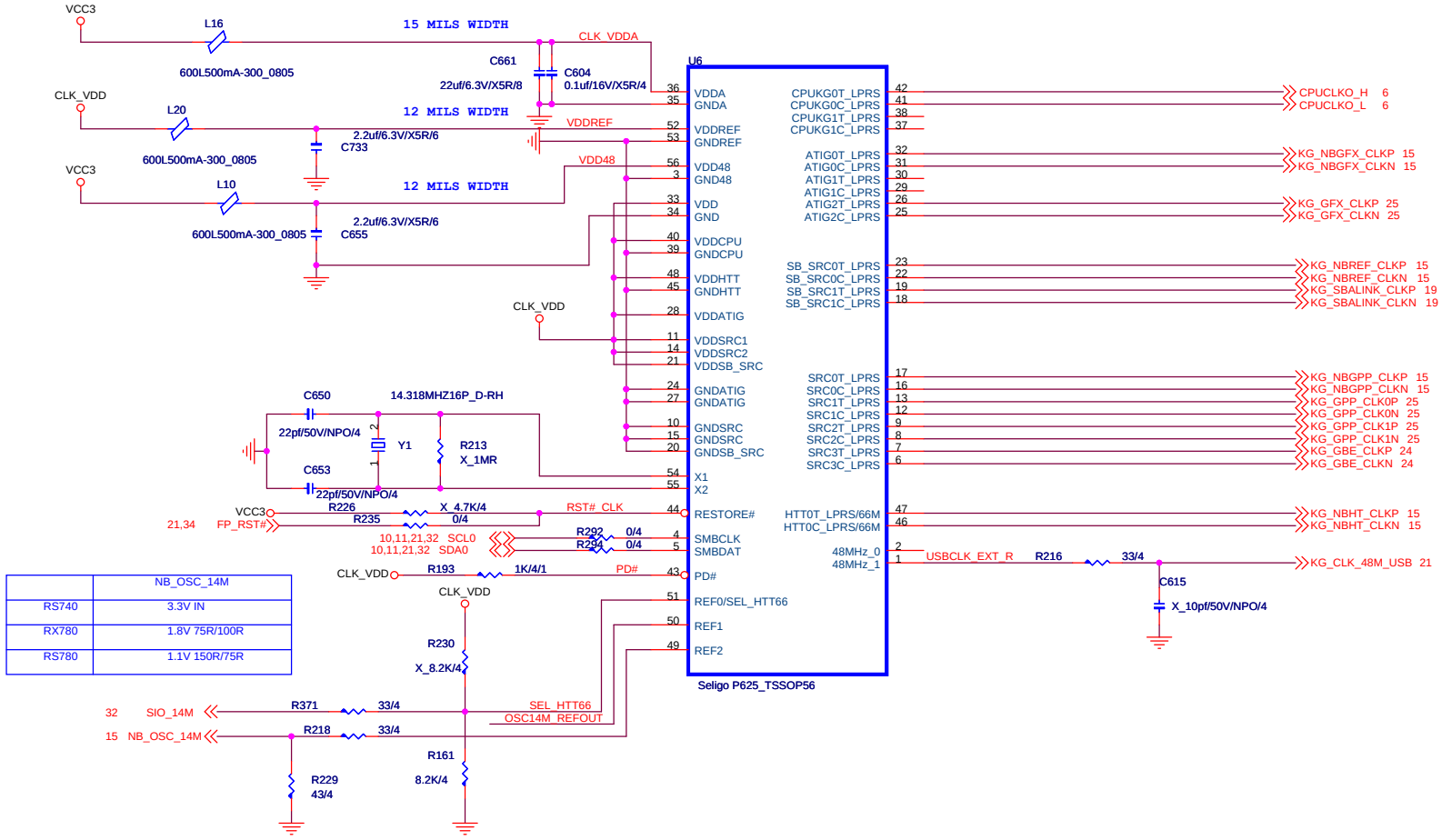
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U6 AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U6 POWER PIN



	NB_OSC_14M
RS740	3.3V IN
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

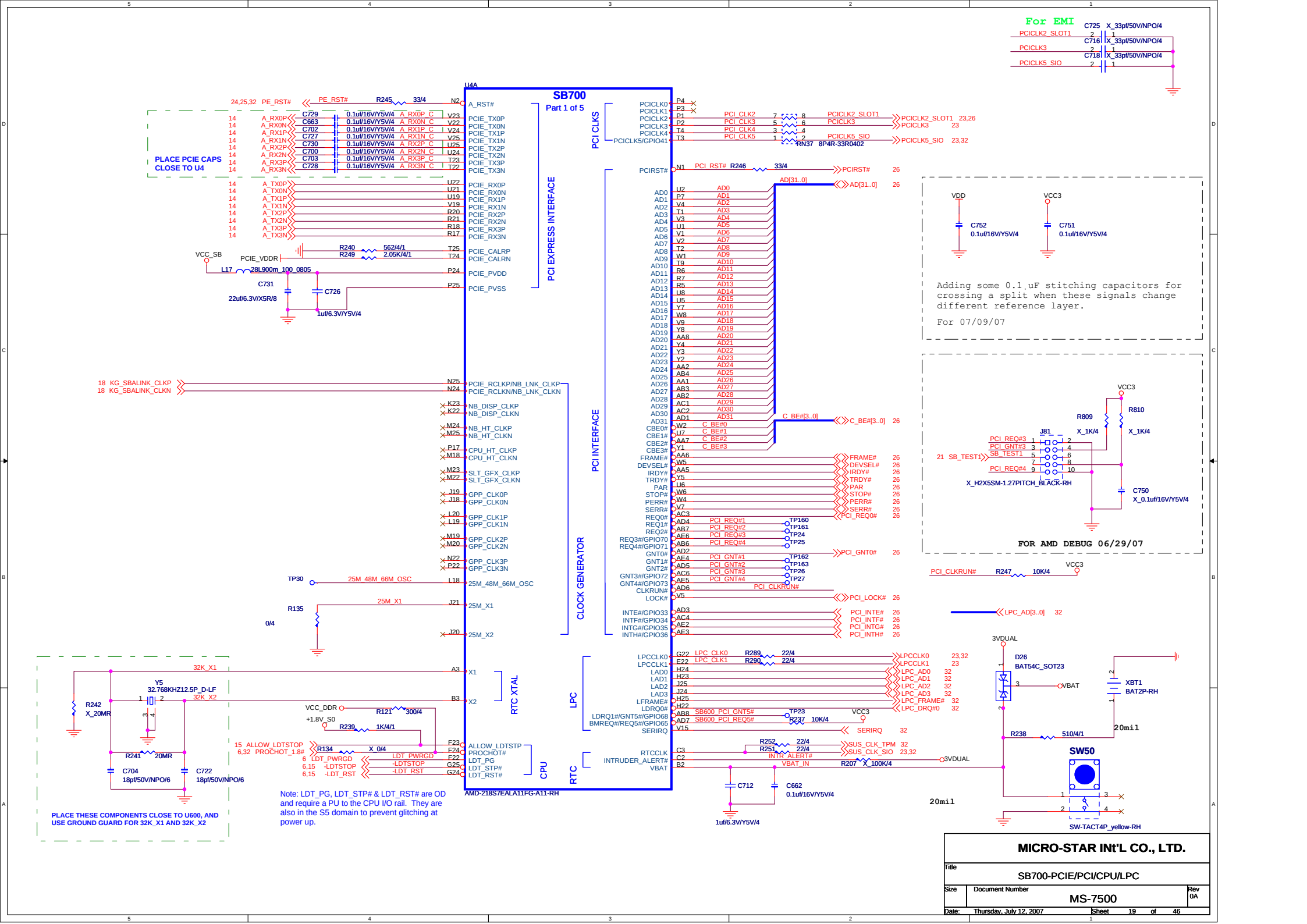
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

MICRO-STAR INt'L CO., LTD.

Title: Clock-Gen Seligo P625

Size | Document Number: MS-7500 | Rev: 0A

Date: Thursday, July 12, 2007 | Sheet 18 of 46


For EMI
C725 X_33pf/50V/NPO/4
C716 X_33pf/50V/NPO/4
C718 X_33pf/50V/NPO/4
PCICLK2_SLOT1
PCICLK3
PCICLK5_SIO
U4A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
PLACE PCIE CAPS CLOSE TO U4
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
AMD-218S7EALA11FG-A11-RH
Adding some 0.1uF stitching capacitors for crossing a split when these signals change different reference layer.
For 07/09/07
FOR AMD DEBUG 06/29/07
X_H2X5SSM-1.27PITCH_BLACK-RH
SW-TACT4P_yellow-RH
MICRO-STAR INt'L CO., LTD.
SB700-PCIE/PCI/CPU/LPC
MS-7500
Thursday, July 12, 2007
19 of 46

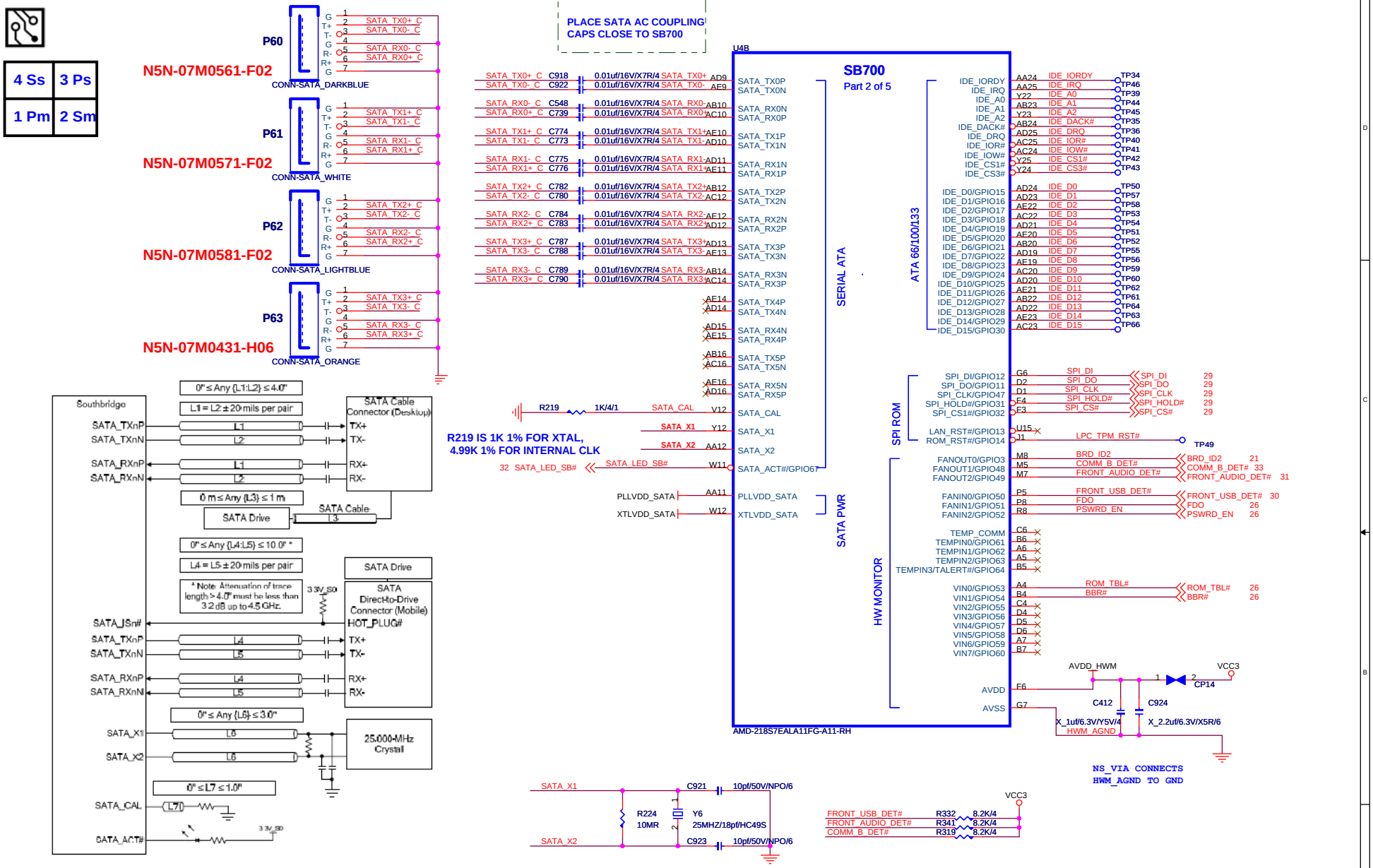


Figure 29: Layout Guidelines the Serial ATA Signals

Trace spacing:

- ASIC breakout (first 0.5") ≥ 1:1
- After the breakout region ≥ 5:1 on both sides of pair.

Impedance:

- 100 Ω ± 15% differential.
- Reference to a solid GND (not PWR) plane.

MICRO-STAR INt'L CO., LTD.			
Title	SB700-SATA/IDE/HWM/SPI		
Size	Document Number	MS-7500	Rev 0A
Date:	Thursday, July 12, 2007	Sheet 20 of 46	

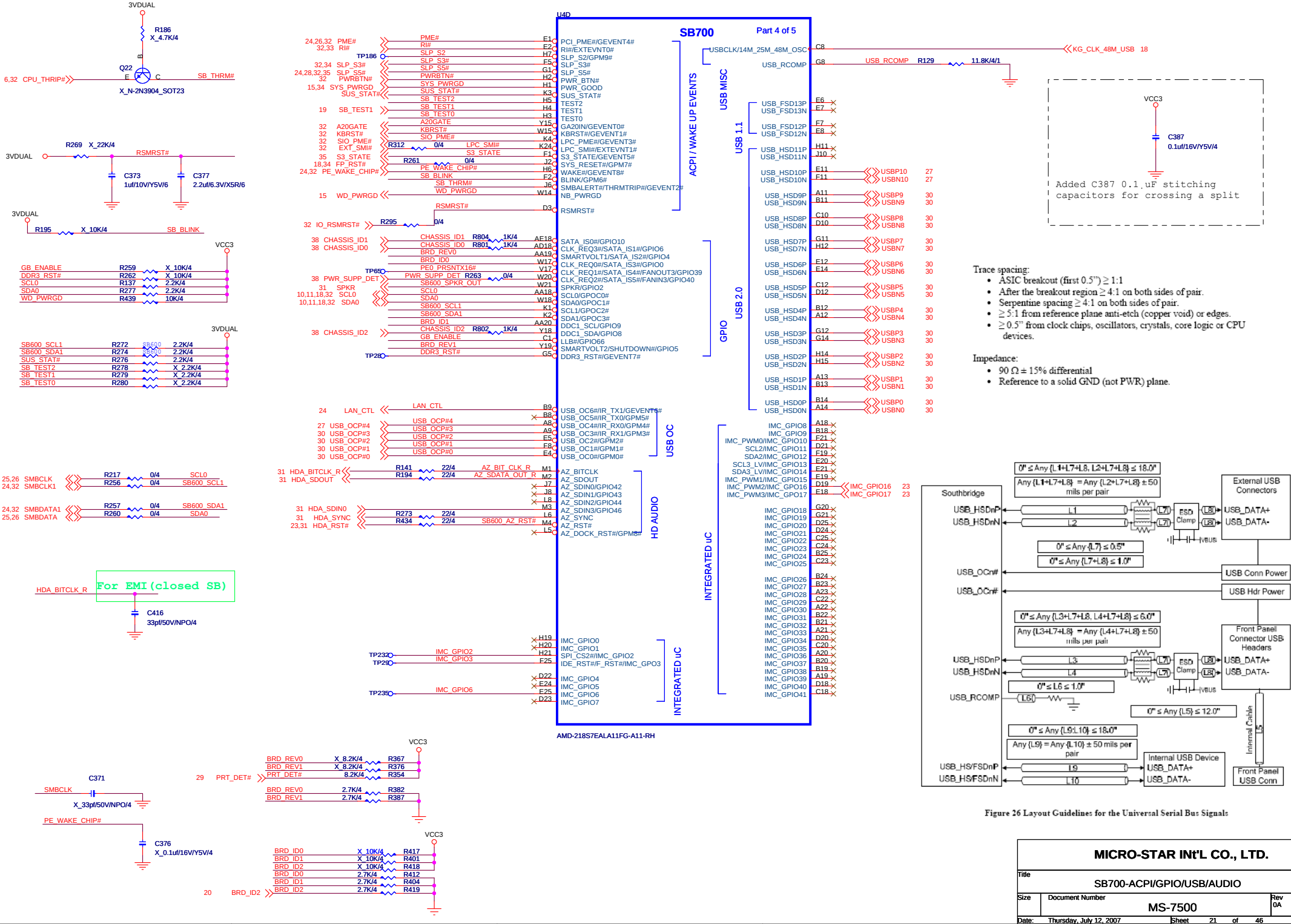
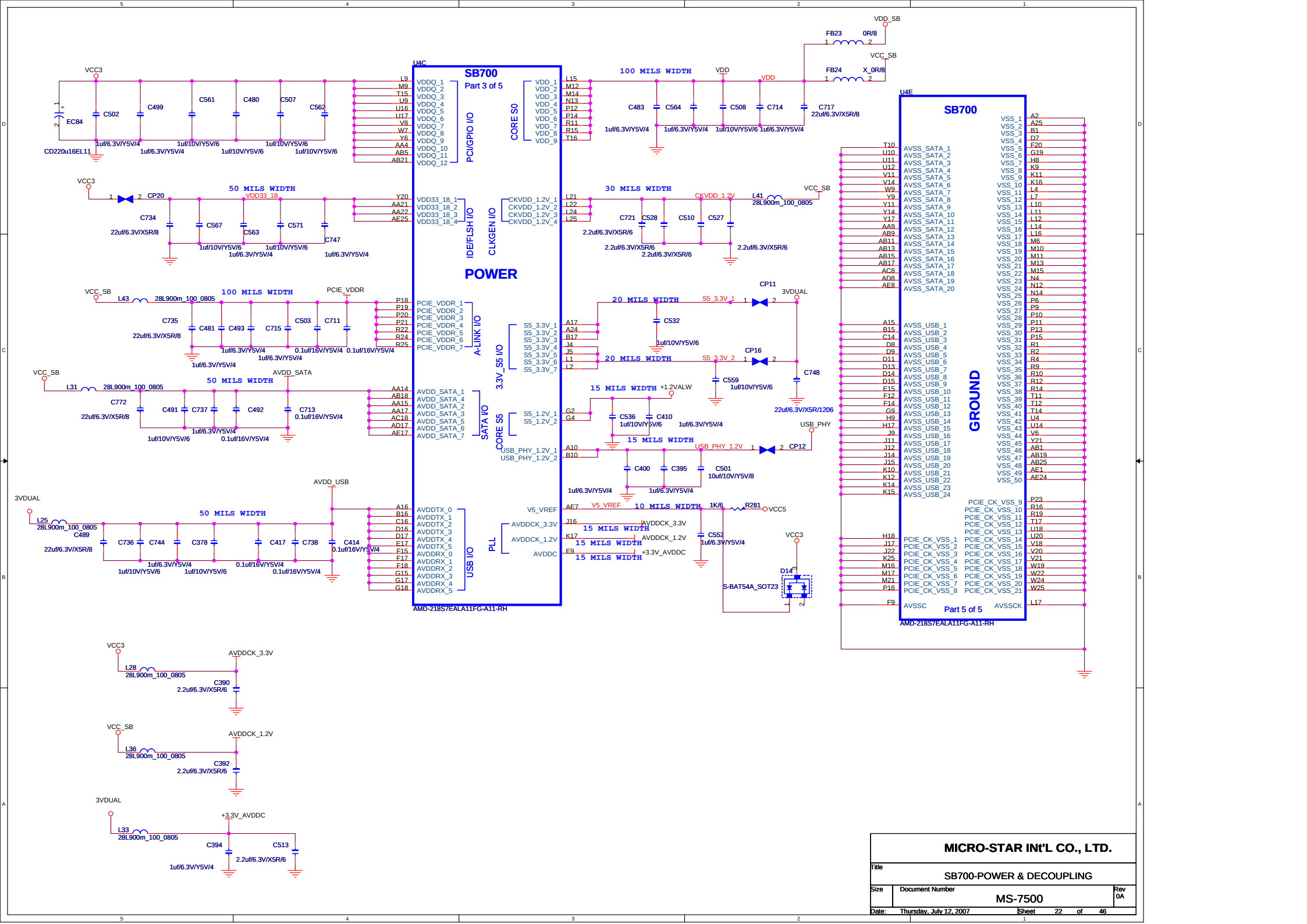
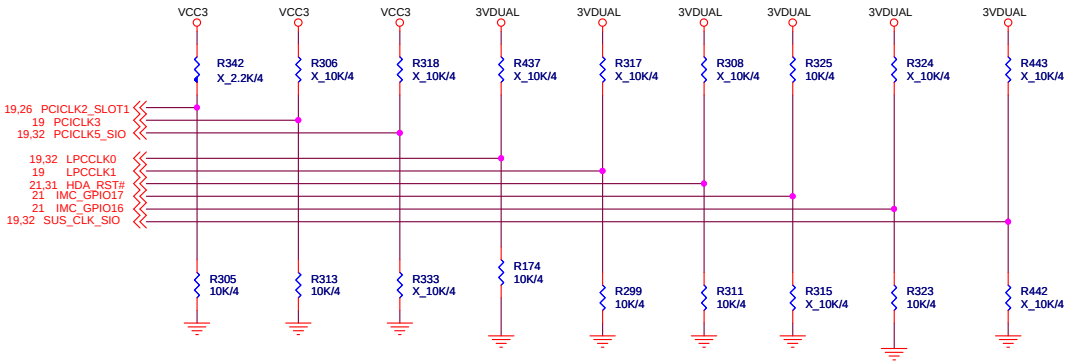


Figure 26 Layout Guidelines for the Universal Serial Bus Signals


SB700
Part 3 of 5
POWER
AMD-218S7EALA11FG-A11-RH
SB700
Part 5 of 5
GROUND
AMD-218S7EALA11FG-A11-RH
MICRO-STAR INt'L CO., LTD.
SB700-POWER & DECOUPLING
MS-7500
Rev 0A
Thursday, July 12, 2007
Sheet 22 of 46

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	RESERVED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INt'L CO., LTD.

Title: SB700-STRAPS

Size | Document Number: MS-7500 | Rev 0A

Date: Thursday, July 12, 2007 Sheet 23 of 46

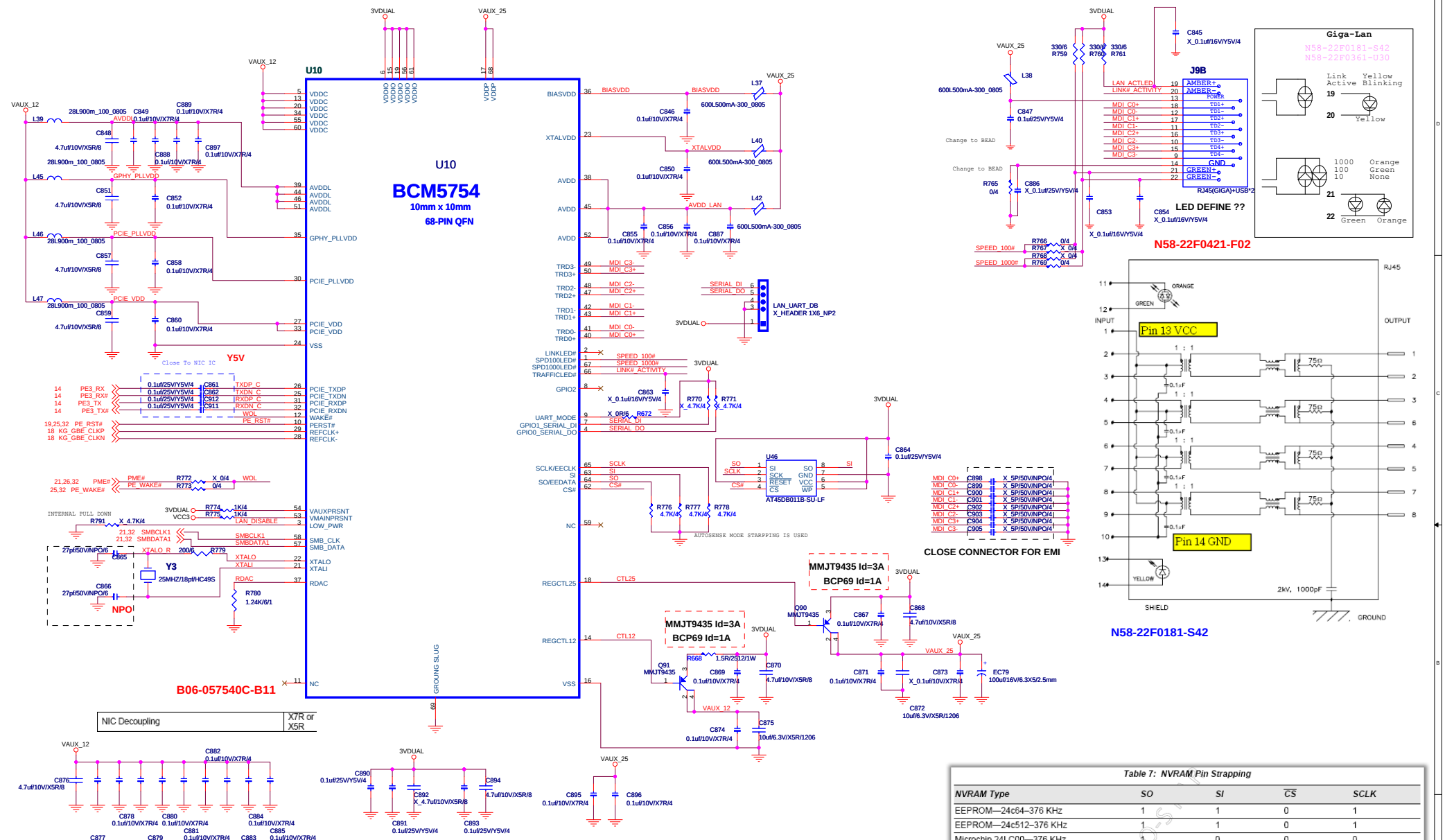
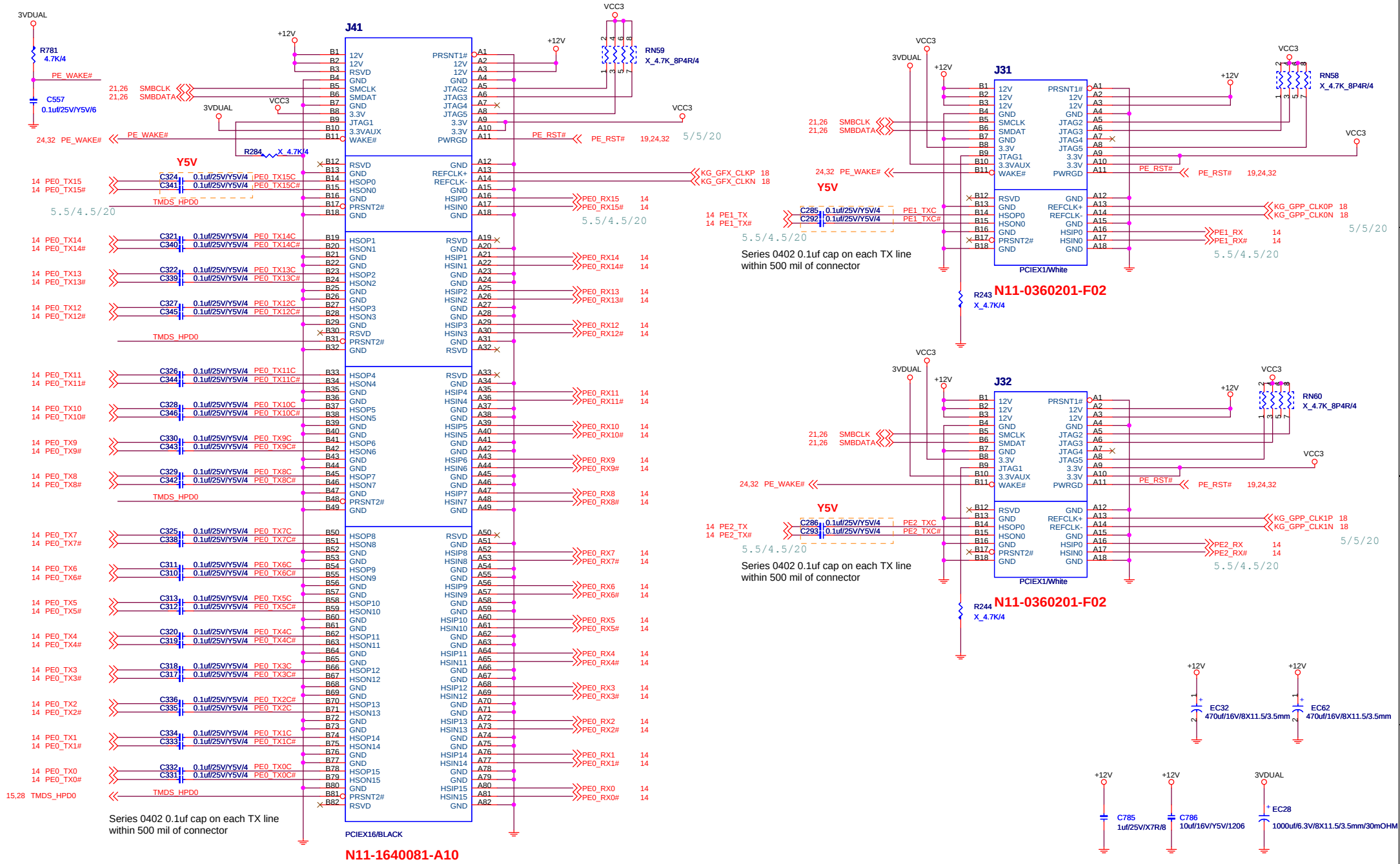


Table 7: NVRAM Pin Strapping

NVRAM Type	SO	SI	$\overline{CS}$	SCLK
EEPROM—24c64–376 KHz	1	1	0	1
EEPROM—24c512–376 KHz	1	1	0	1
Microchip 24LC00—376 KHz	1	0	0	0
Microchip 24LC01—376 KHz	1	0	0	0
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0
Atmel AT45DB011B	1	0	1	1
Atmel AT45DB021B	1	0	1	1
Atmel AT45DB041B	1	0	1	1
Autosense	0	0	1	0

MICRO-STAR INT'L CO., LTD.			
Title: GIGABIT ETHERNET			
Size	Document Number: MS-7500		Rev: 0A
Date: Thursday, July 12, 2007	Sheet 24 of 46		



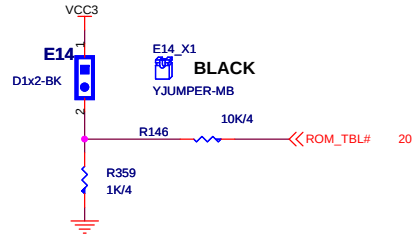
PCI Express Signal Coupling	Y5V

T:2 , H:4.5 ,W:5.5 ,S:4.5,Er:4.2 ,Zo=91.8 Ohm

20 / 5.5 / 4.5 / 5.5 / 20

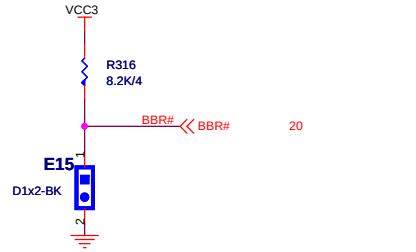
MICRO-STAR INt'L CO., LTD.	
Title	PCIE x 16 , x1 Slots.
Size	Document Number: MS-7500 — Rev: 0A
Date: Thursday, July 12, 2007	Sheet 25 of 46

BOOT BLOCK WRITE JUMPER



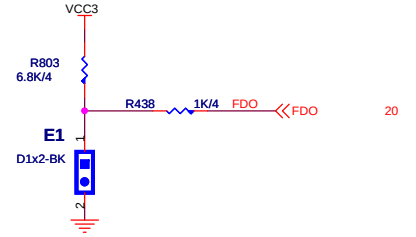
N31-1020211-P05

BOOT BLOCK RECOVERY HEADER



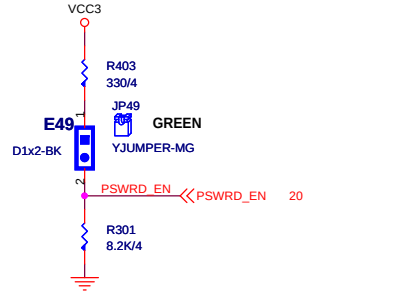
N31-1020211-P05

FLASH DESCRIPTOR OVERRIDE



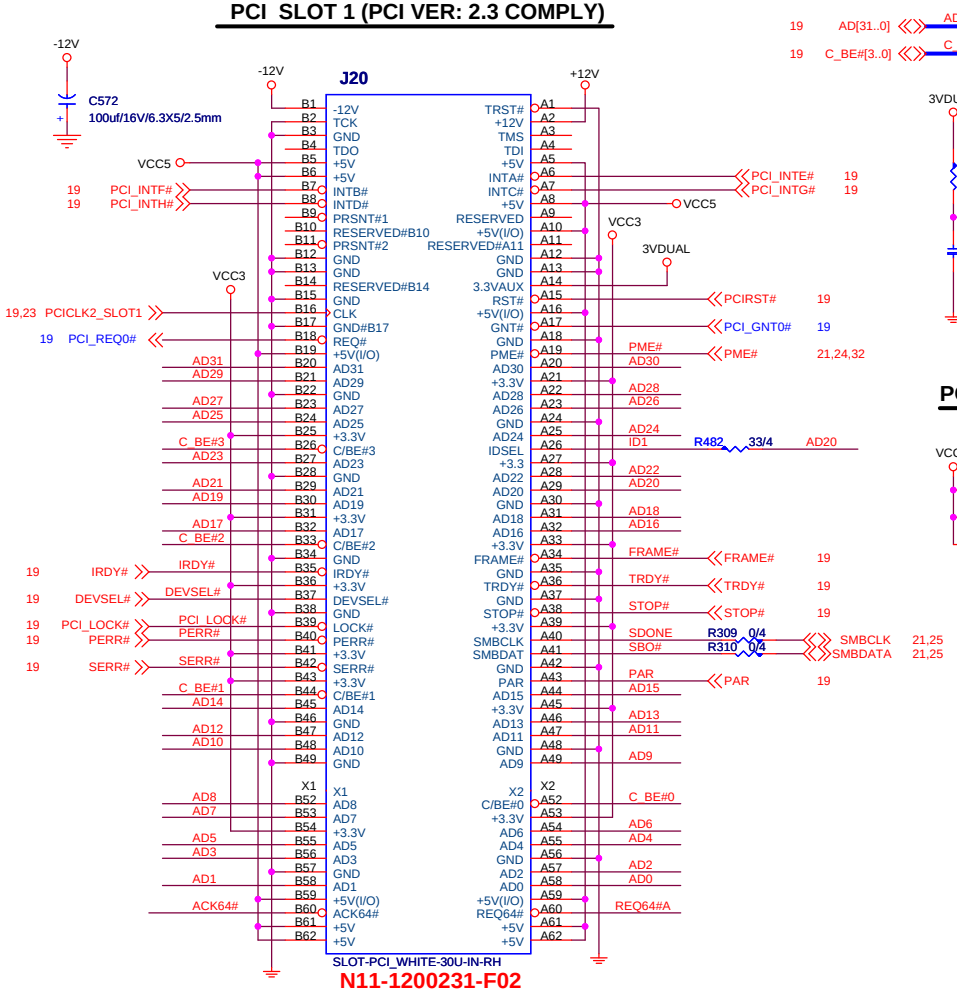
N31-1020211-P05

PASSWORD JUMPER



N31-1020211-P05

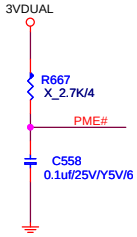
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



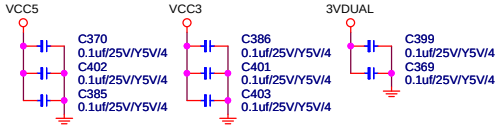
N11-1200231-F02

SB700
PCI SLOT1
IDSEL = AD20
PCI_REQ0#
PCI_GNT0#
PCI_INTE#

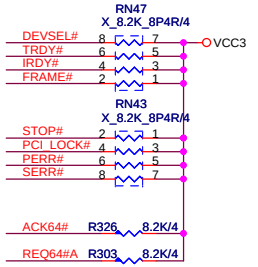
PCIRST#
PCICLK2_SLOT1

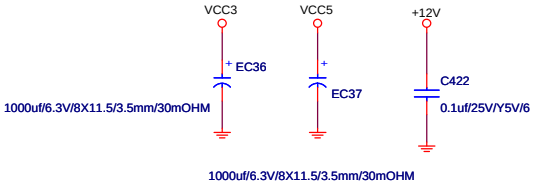


PCI SLOT DECOUPLING CAPACITORS



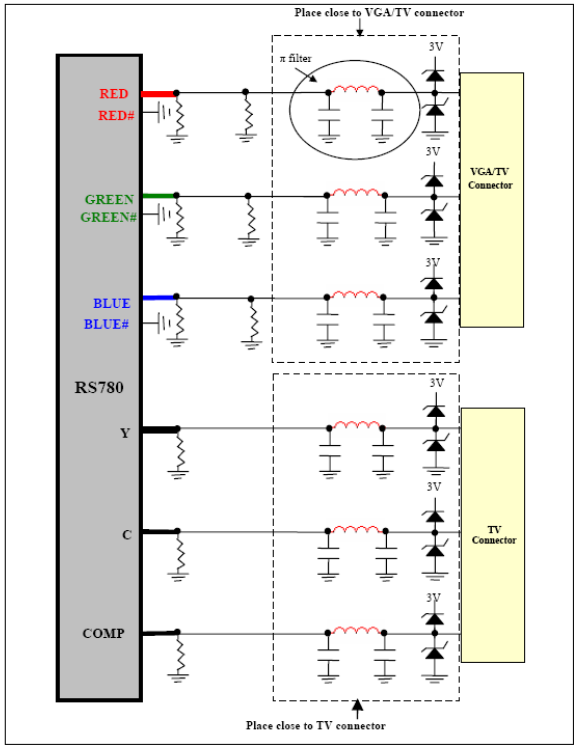
PCI PULL-UP / DOWN RESISTORS





MICRO-STAR INt'L CO., LTD.		
Title: PCI Slot1		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 26 of 46	

Figure 29: Placement of VGA and TV-Out Connectors



VGA CONN BLOCK

close VGA connector

POWER CIRCUIT FOR USB PORT 10

120 mils

40 mils

FRONT PANEL USB CONNECTOR FOR USB PORT 10

Trace lengths must be less 5 inches

Match pairs to 50 mil.

NEAR USB CONNECTOR

N32-2051671-H06

FRONT USE DETECT

Temperature Sensing

CPU & NB temperature sensor

D0F-0104302-S32

COLSE TO FDD CONN.

COLSE TO HDD

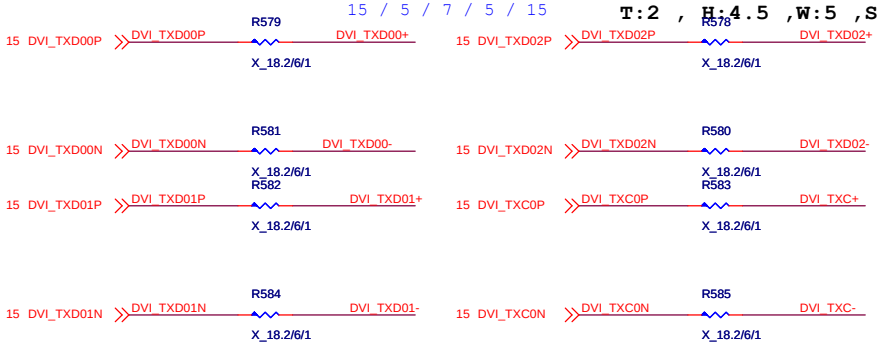
CLOSE TO HDR

COLSE CHIPSET

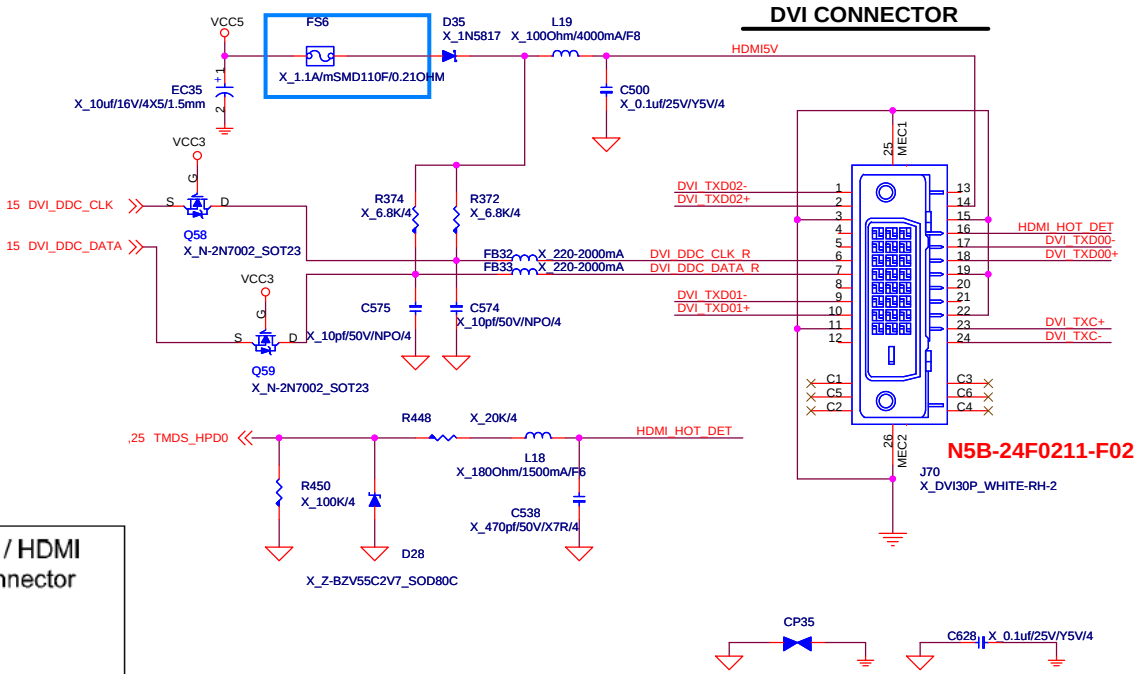
X_N51-15F0521-F02

MICRO-STAR INt'L CO., LTD.	
Title	VGA CONNECTOR
Size	Document Number: MS-7500 — Rev: 0A
Date: Thursday, July 12, 2007	Sheet 27 of 46

15 / 5 / 7 / 5 / 15 T:2 , H:4.5 ,W:5 ,S:7,Er:4.2 ,Zo=104.8 Ohm



DVI CONNECTOR



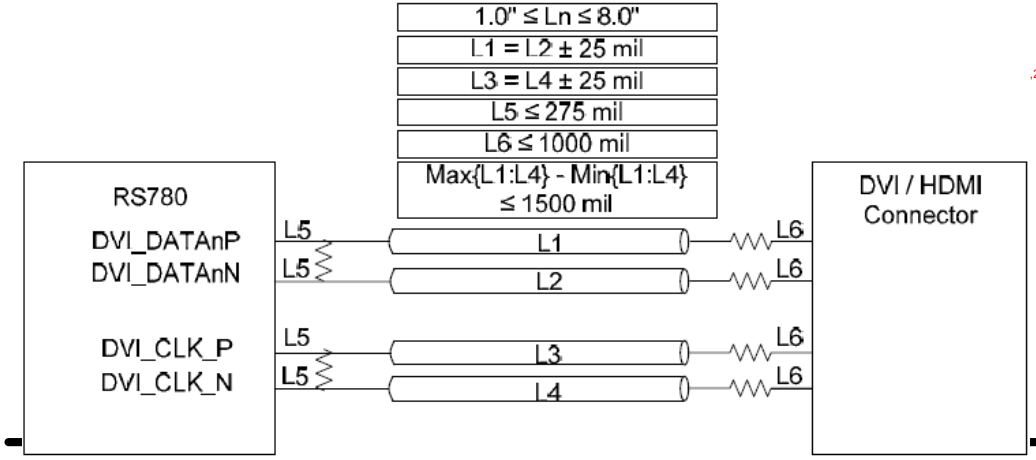
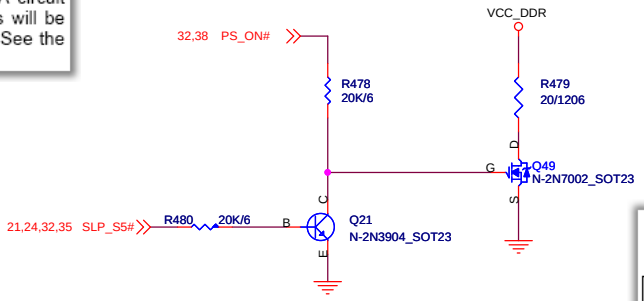


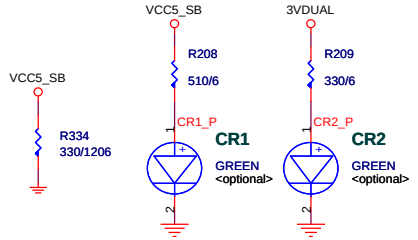
Figure 32: Layout Guidelines for the DVI/HDMI Signals

7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.

MEMORY VOLTAGE BLEED-OFF CIRCUIT





BLEED-OFF CIRCUIT

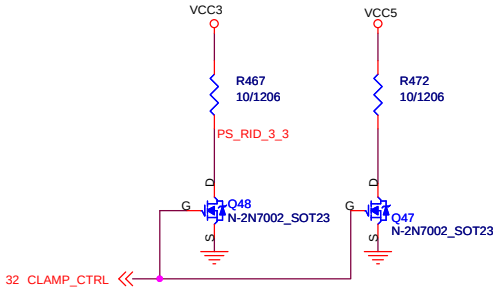
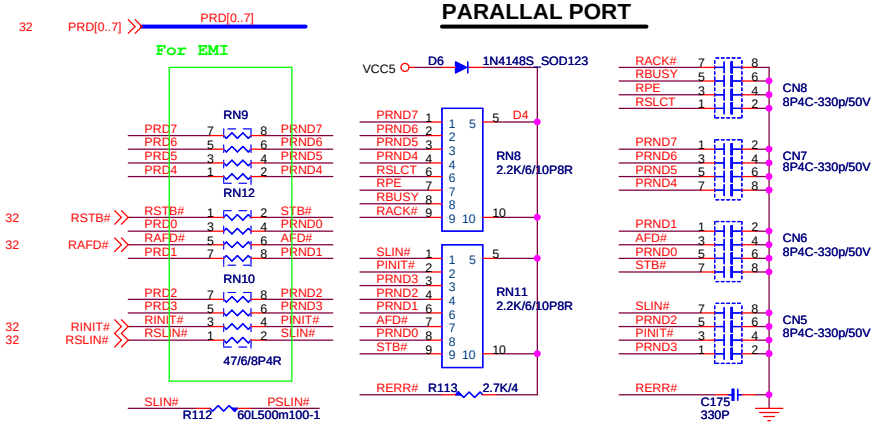


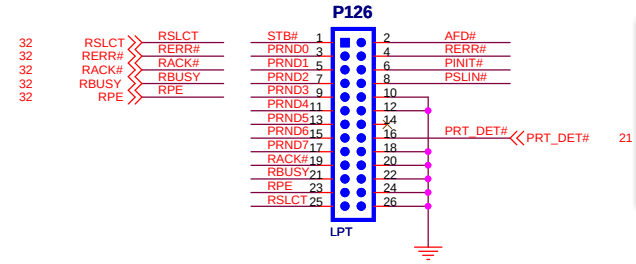
TABLE 38
SYSTEM BOARD LED REQUIREMENTS

Function	Ref Des	Color
+5 V AUX	CR1	Green
+3 V AUX	CR2	Green

MICRO-STAR INt'L CO., LTD.		
Title: DVI CONNECTOR / BLEED OFF		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 28 of 46	

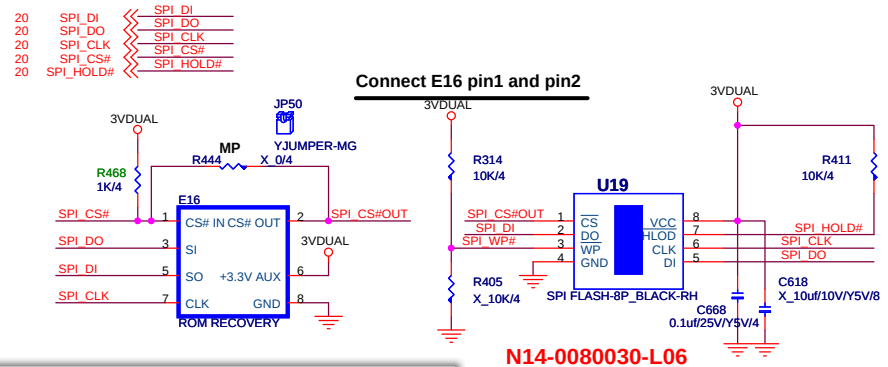
PARALLAL PORT





P/N , FOOTPRINT

SPI ROM



N14-0080030-L06

TABLE 22
ROM RECOVERY HEADER DEFINITION

E16

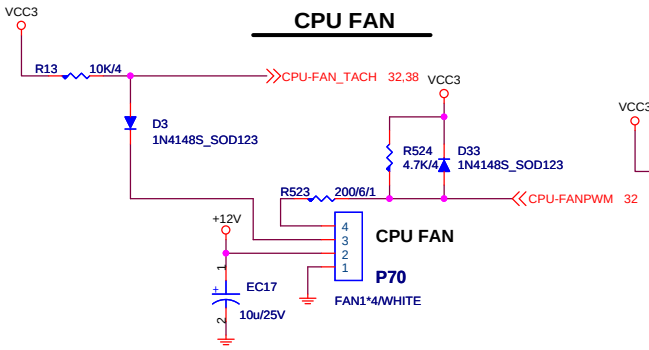
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	CS# IN	CS# OUT	2
3	SI	KEY (no pin)	4
5	SO	VCC (+3.3V AUX)	6
7	CLK	GND	8

Parallel Port 2 x13 header

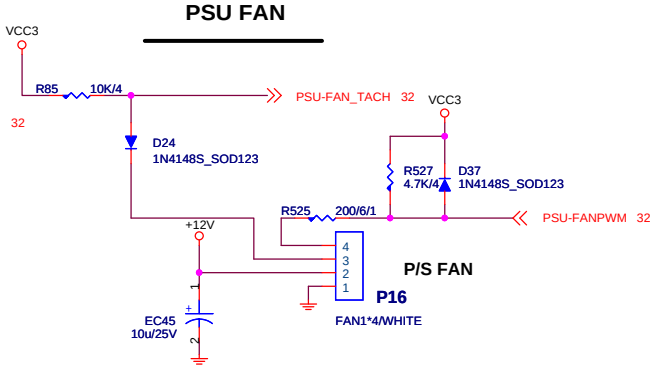
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

FAN BOLCK

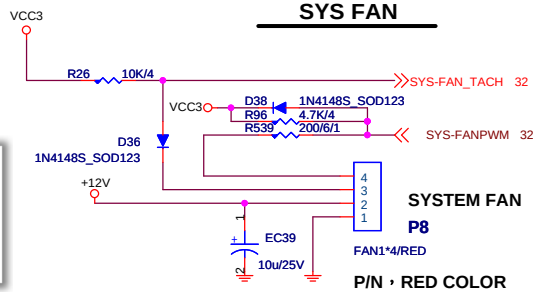
CPU FAN



PSU FAN



SYS FAN



P/N，RED COLOR

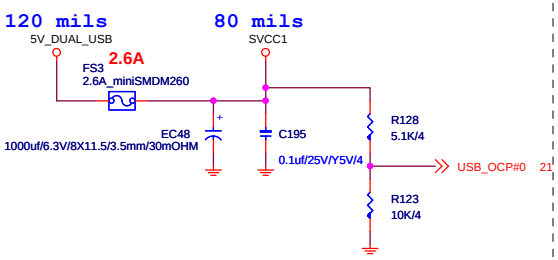
P70 – CPU P8 – Chassis P16 – Power Supply

Pin #	Signal Name
1	GND
2	+12 V
3	FAN TACH
4	FAN PWM INPUT

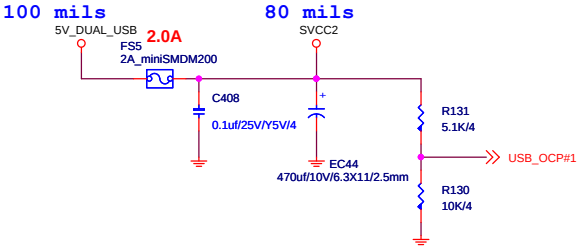
MICRO-STAR INt'L CO., LTD.

Title	SPI ROM / FAN / LPT	
Size	Document Number MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 29 of 46	

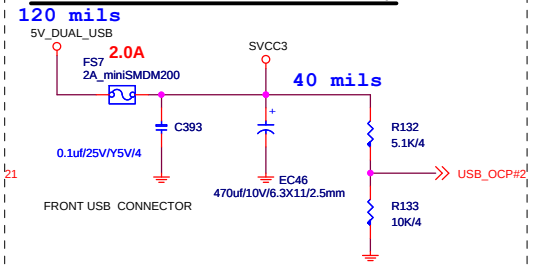
POWER CIRCUIT FOR USB PORT 0,1,2,3



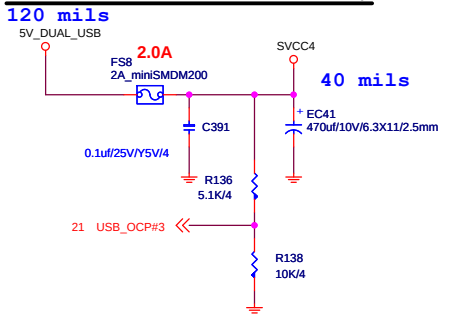
POWER CIRCUIT FOR USB PORT 4,5



POWER CIRCUIT FOR USB PORT 6,7

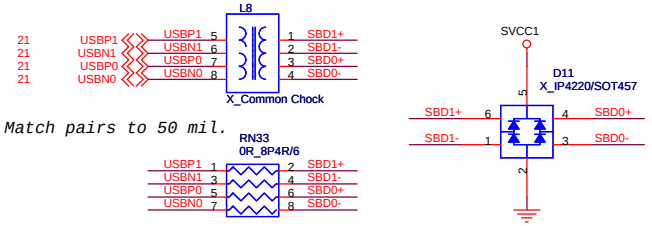


POWER CIRCUIT FOR USB PORT 8,9



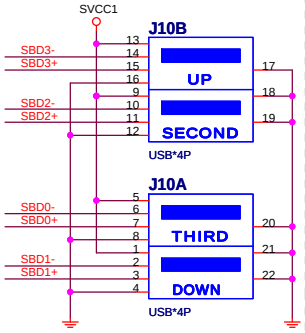
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3

Trace lengths must be less 12 inches



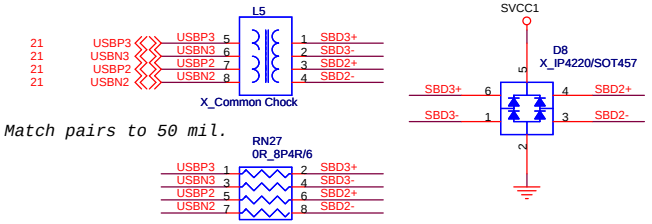
Match pairs to 50 mil.

NEAR USB CONNECTOR



N53-16M0041-A10

Trace lengths must be less 12 inches



Match pairs to 50 mil.

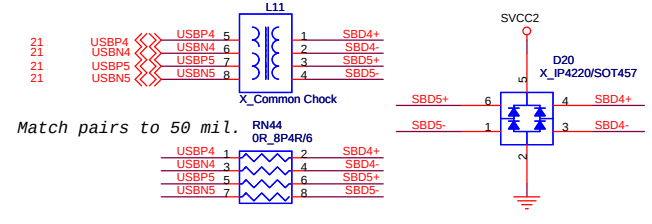
NEAR USB CONNECTOR

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

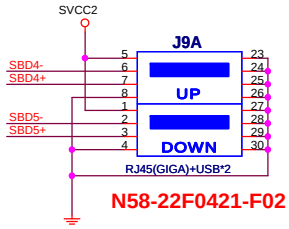
REAL USB CONNECTOR WITH RJ45 FOR USB PORT 4,5

Trace lengths must be less 5 inches



Match pairs to 50 mil.

NEAR USB CONNECTOR



N58-22F0421-F02

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

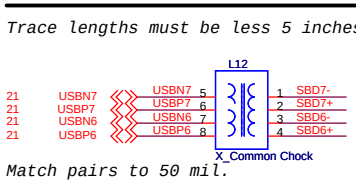
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

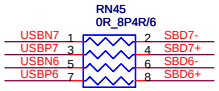
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

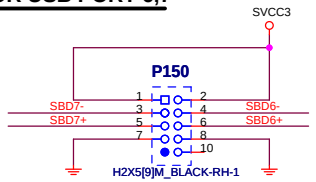
Trace lengths must be less 5 inches



Match pairs to 50 mil.



NEAR USB CONNECTOR



N31-2051391-H06

COLOR BLACK

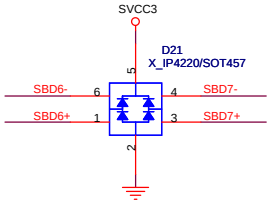


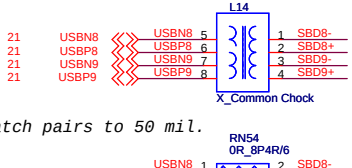
TABLE 10
MEDIA CARD READER USB HEADER DEFINITION (TOP VIEW)

P150

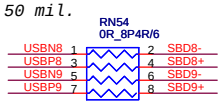
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 4 (-)	USB Port 5 (-)	4
5	USB Port 4 (+)	USB Port 5 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	No Connect	10

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

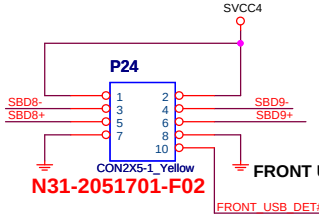
Trace lengths must be less 5 inches



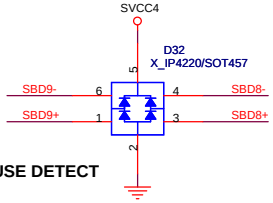
Match pairs to 50 mil.



NEAR USB CONNECTOR



N31-2051701-F02



T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

TABLE 9
FRONT I/O USB HEADER DEFINITION (TOP VIEW)

P24

Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 8 (-)	USB Port 9 (-)	4
5	USB Port 8 (+)	USB Port 9 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	FRONT USB DETECT#	10

MICRO-STAR INt'L CO., LTD.

Title: USB Conn.

Size | Document Number: MS-7500 | Rev: 0A

Date: Thursday, July 12, 2007 | Sheet 30 of 46

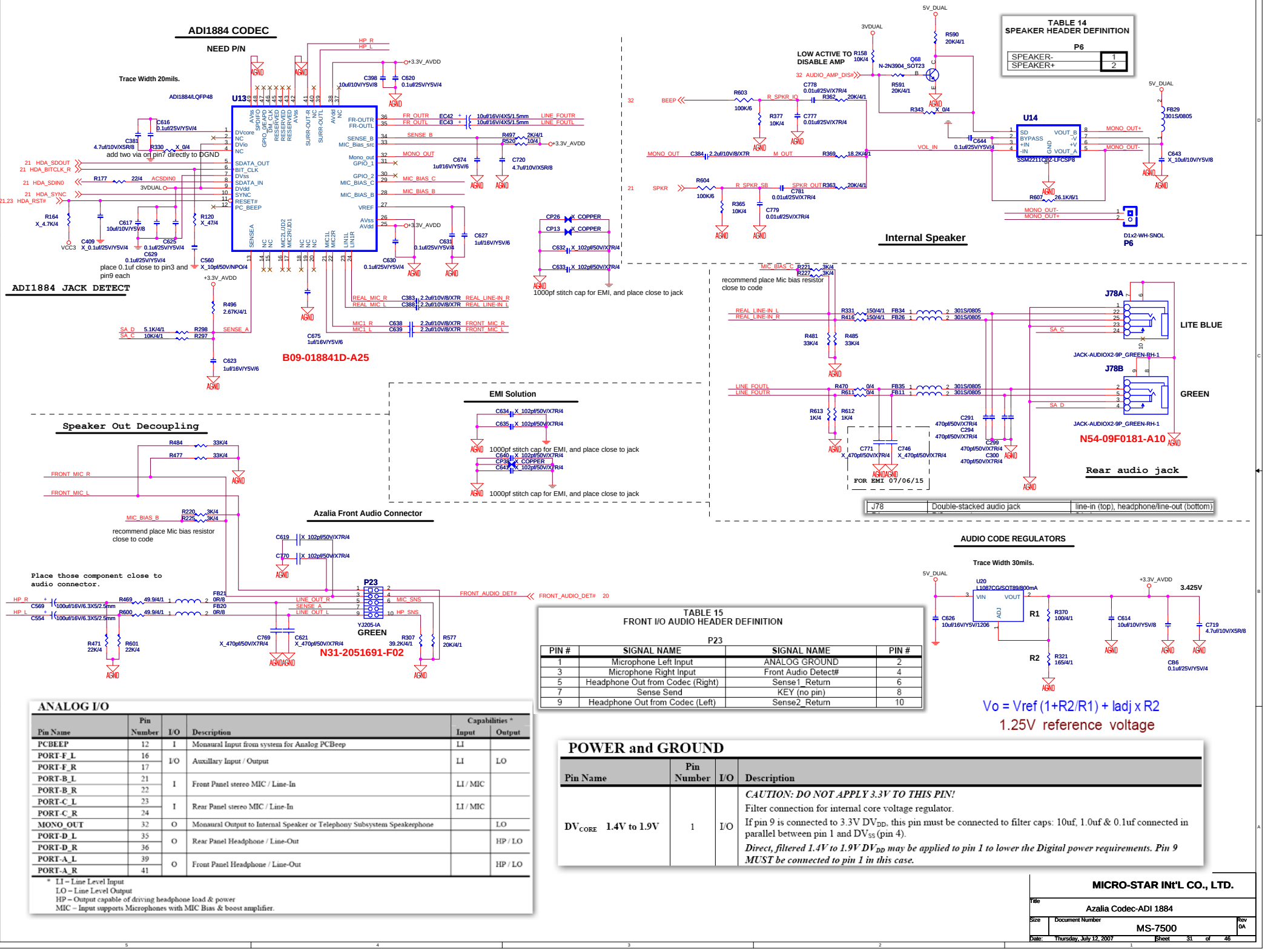


TABLE 15
FRONT I/O AUDIO HEADER DEFINITION

P23

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	Microphone Left Input	ANALOG GROUND	2
3	Microphone Right Input	Front Audio Detect#	4
5	Headphone Out from Codec (Right)	Sense1_Return	6
7	Sense Send	KEY (no pin)	8
9	Headphone Out from Codec (Left)	Sense2_Return	10

ANALOG I/O

Pin Name	Pin Number	I/O	Description	Capabilities * Input	Capabilities * Output
PCBEEP	12	I	Monaural Input from system for Analog PCBeep	LI	
PORT-F_L	16	I/O	Auxillary Input / Output	LI	LO
PORT-F_R	17				
PORT-B_L	21	I	Front Panel stereo MIC / Line-In	LI / MIC	
PORT-B_R	22				
PORT-C_L	23	I	Rear Panel stereo MIC / Line-In	LI / MIC	
PORT-C_R	24				
MONO_OUT	32	O	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone		LO
PORT-D_L	35	O	Rear Panel Headphone / Line-Out		HP / LO
PORT-D_R	36				
PORT-A_L	39	O	Front Panel Headphone / Line-Out		HP / LO
PORT-A_R	41				

* LI – Line Level Input
LO – Line Level Output
HP – Output capable of driving headphone load & power
MIC – Input supports Microphones with MIC Bias & boost amplifier.

POWER and GROUND

Pin Name	Pin Number	I/O	Description
DV_{CORE} 1.4V to 1.9V	1	I/O	*CAUTION: DO NOT APPLY 3.3V TO THIS PIN!* Filter connection for internal core voltage regulator. If pin 9 is connected to 3.3V DV_{DD}, this pin must be connected to filter caps: 10uf, 1.0uf & 0.1uf connected in parallel between pin 1 and DV_{SS} (pin 4). *Direct, filtered 1.4V to 1.9V DV_{DD} may be applied to pin 1 to lower the Digital power requirements. Pin 9 MUST be connected to pin 1 in this case.*

MICRO-STAR INT'L CO., LTD.

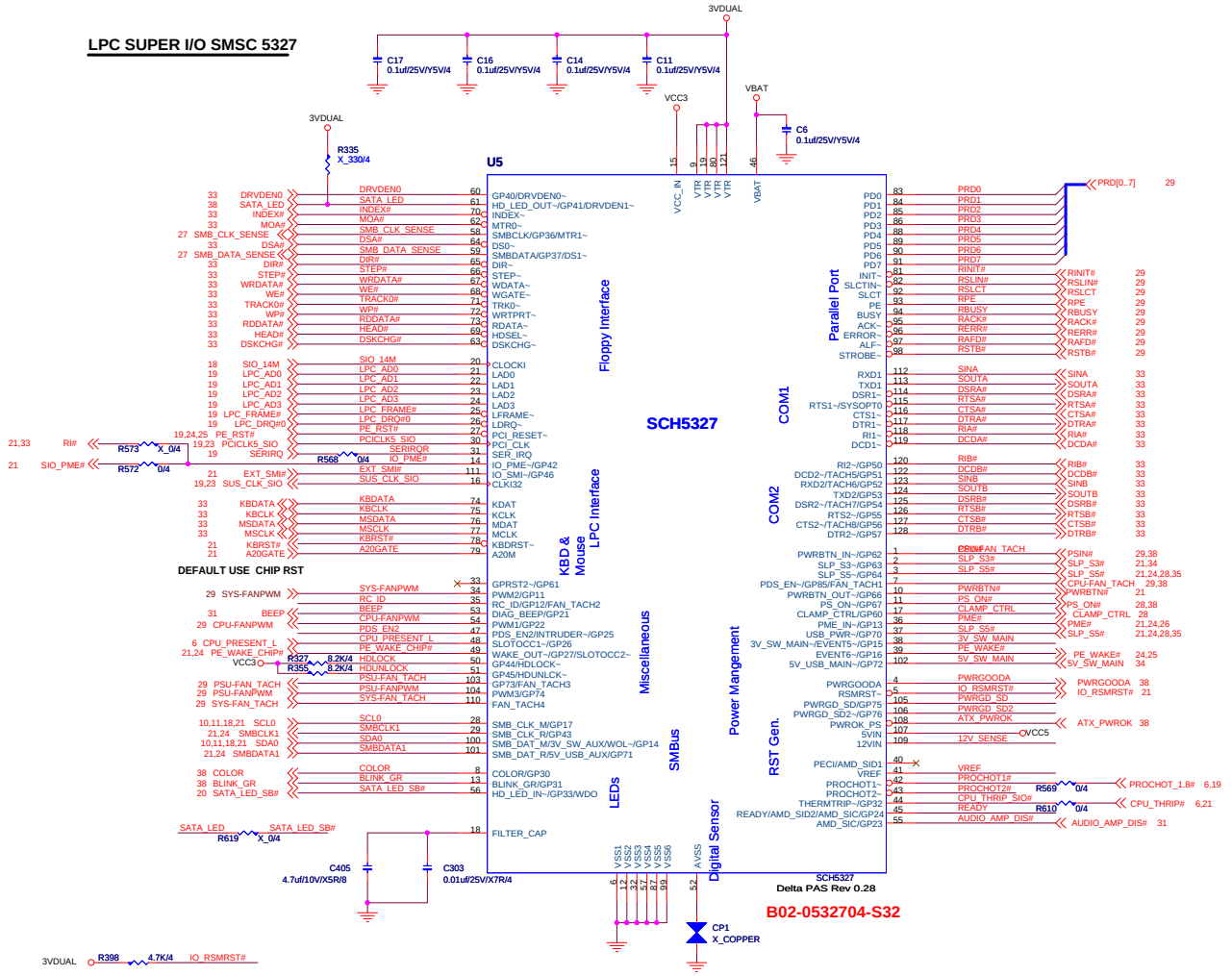
Title: Azalia Codec-ADI 1884

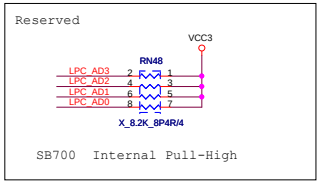
Size | Document Number: MS-7500 | Rev 0A

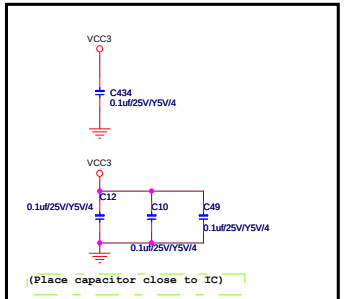
Date: Thursday, July 12, 2007 | Sheet 31 of 46

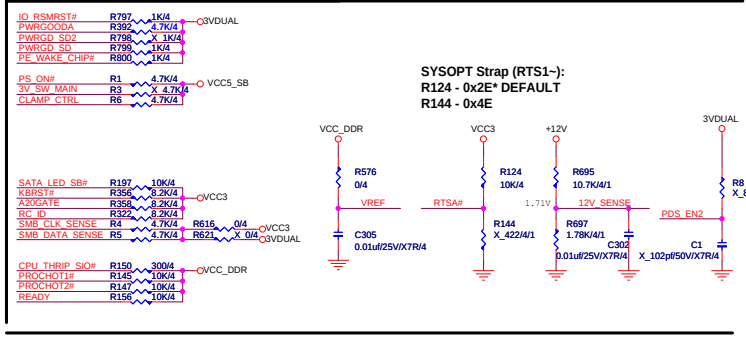
LPC length should be less than 18 inches.

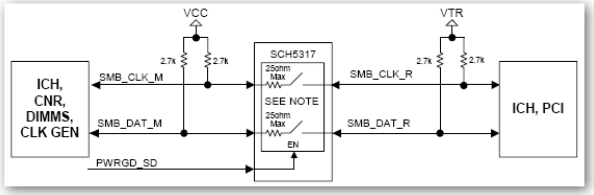
LPC SUPER I/O SMSC 5327



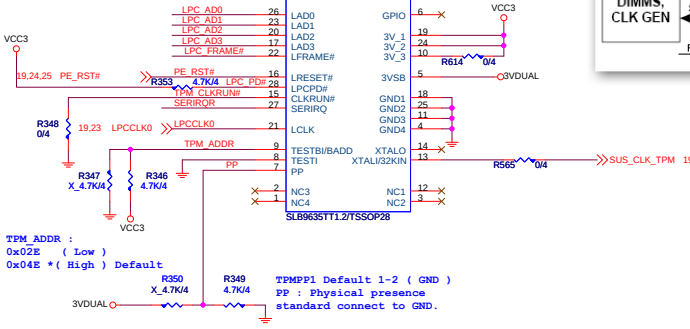






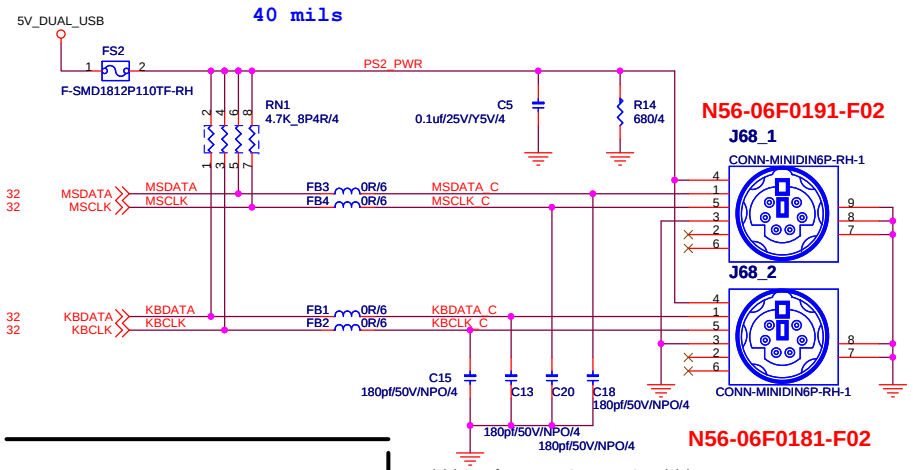


TPM 1.2

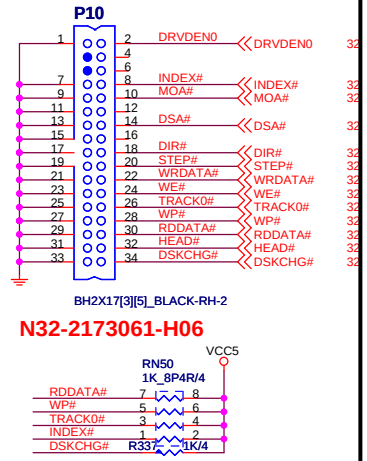


MICRO-STAR INT'L CO., LTD.	
Title	SIO-SMSC5327 / TPM
Size	Document Number: MS-7500 — Rev 0A
Date: Thursday, July 12, 2007	Sheet 32 of 46

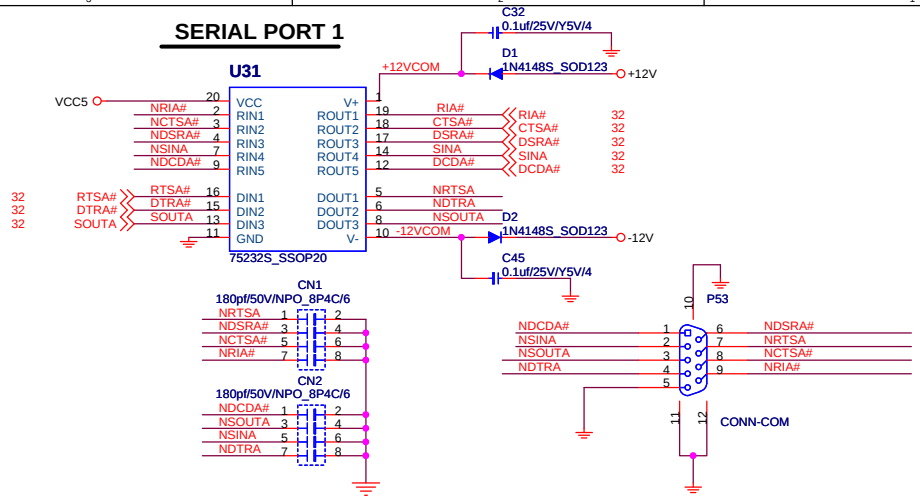
PS2 KEYBOARD & MOUSE CONNECTOR



FLOPPY CONN BOLCK



SERIAL PORT 1



SERIAL PORT 2

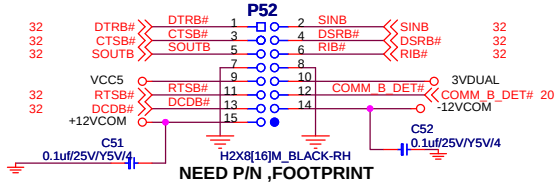
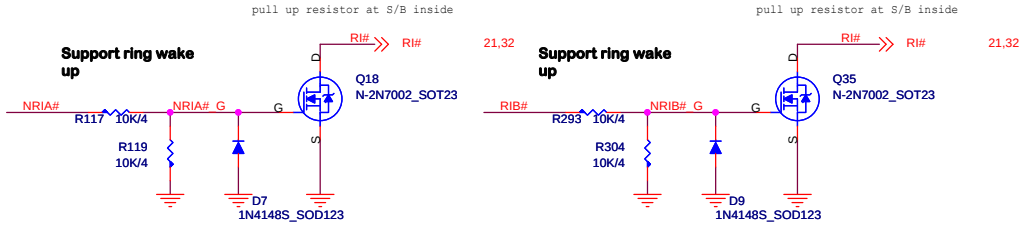


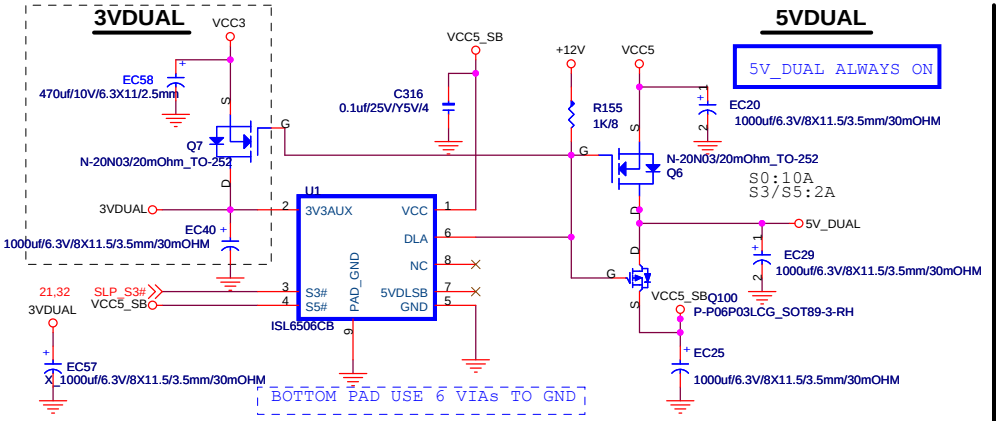
TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

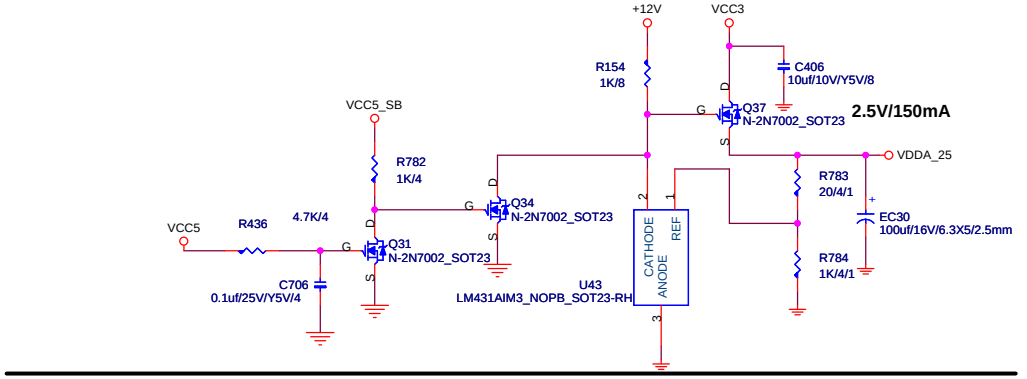


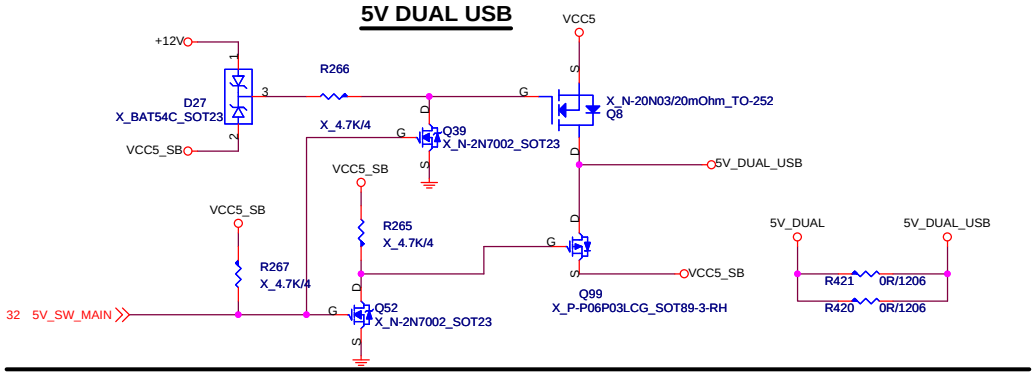
MICRO-STAR INt'L CO., LTD.		
Title: KB/MS&COM1&Floppy Conn.		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 33 of 46	

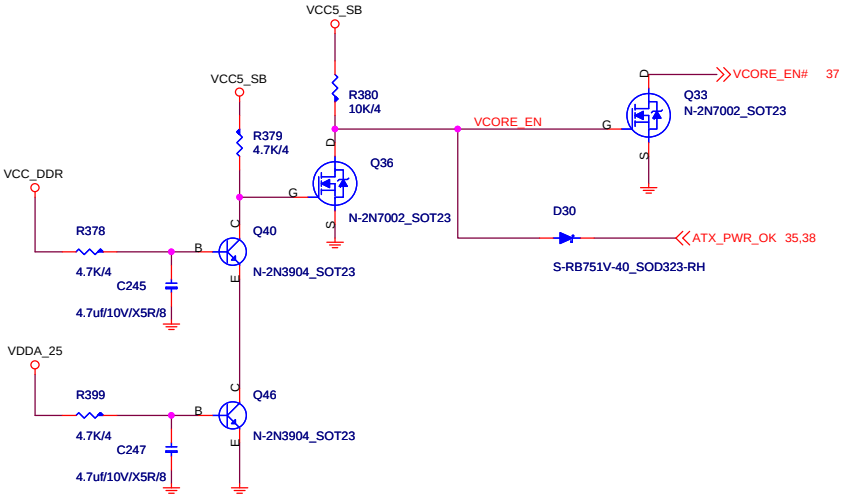


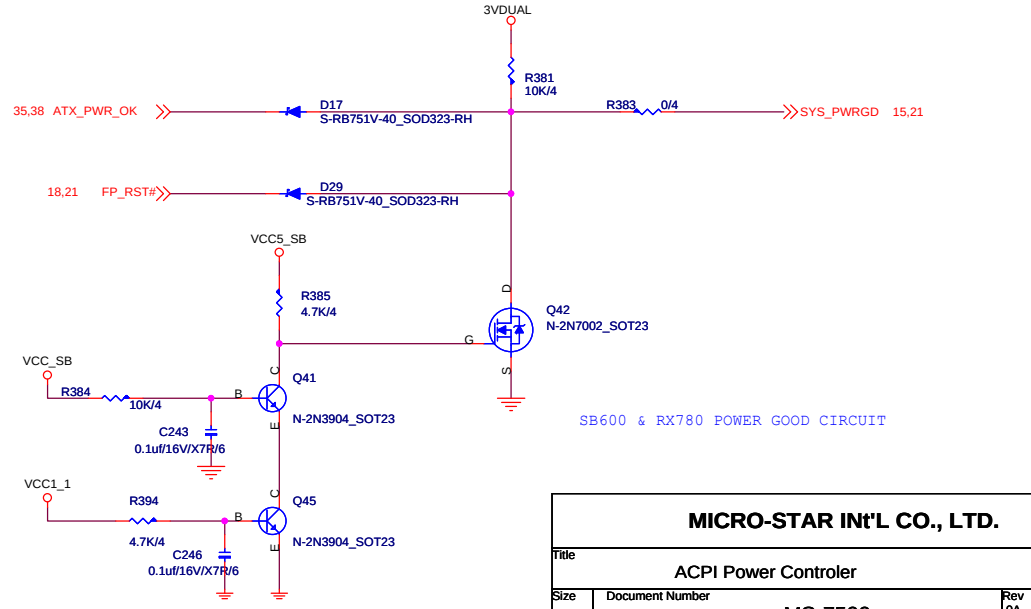
ACPI POWER STATE SUPPORT

Voltage	S0/S1	S3	S4/S5	S5	No AC
3.3 V Main	On	Off	Off	Off	Off
5 V Main	On	Off	Off	Off	Off
12 V	On	Off	Off	Off	Off
-12 V	On	Off	Off	Off	Off
CPU Core Voltage	On	Off	Off	Off	Off
RS780 core/SB600	On	Off	Off	Off	Off
1.8 V DDR2_VDDQ	On	On	On	Off	Off
0.9 V DDR2_VTT	On	On	On	Off	Off
5 V Standby	On	On	On	On	Off
3.3 V Standby	On	On	On	On	Off
5 V Dual (USB-PS/2)	On – main	On – aux	Off	Off	Off
5 V Dual (Memory)	On – main	On – aux	On – aux	Off	Off
3.3 V Dual (PCI)	On – main	On – aux	On – aux	On – aux	Off
3.3 V LAN (EPW)	On	On	On	On	Off
3.3 V Digital Audio	On	On	Off	Off	Off
5 V Analog Audio	On	Off	Off	Off	Off
Battery/RTC Voltage	On	On	On	On	On









MICRO-STAR INt'L CO., LTD.		
Title: ACPI Power Controler		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 34 of 46	

DDR II 1.8V POWER

Irms(MAX) of VCC_DDR=18A

High-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

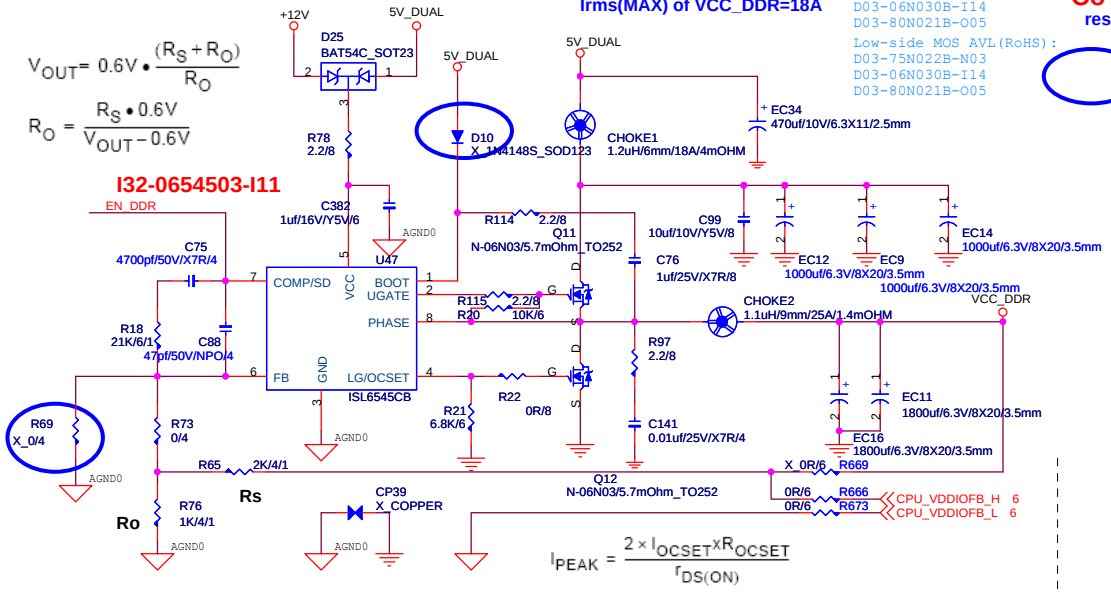
Low-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

Co-lay ISL6545 and NCP1582A
reserved for NCP1582A

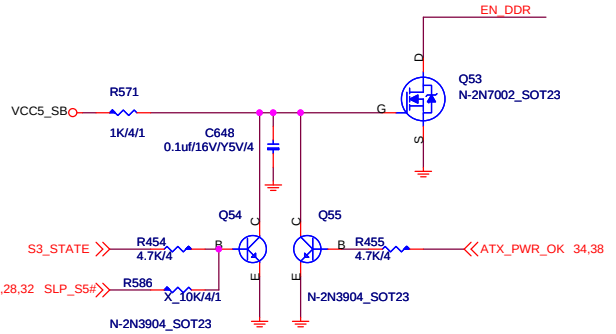
$$V_{OUT} = 0.6V \bullet \frac{(R_S + R_O)}{R_O}$$

$$R_O = \frac{R_S \bullet 0.6V}{V_{OUT} - 0.6V}$$

I32-0654503-I11

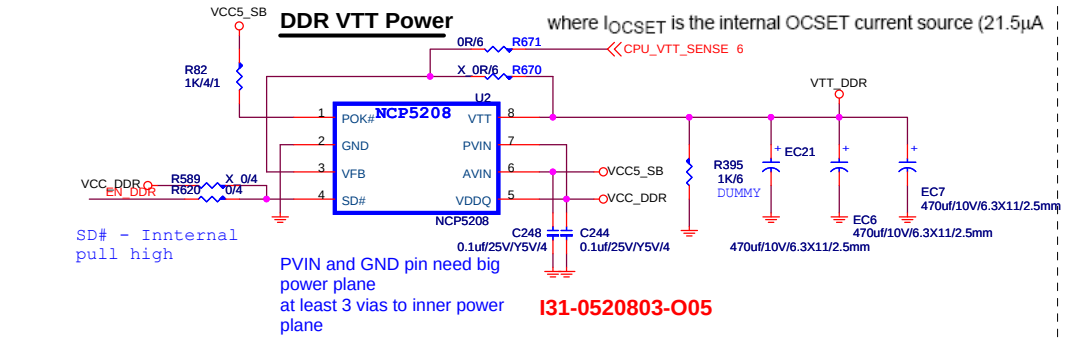


$$I_{PEAK} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$



DDR VTT Power

where I_{OCSET} is the internal OCSET current source (21.5µA

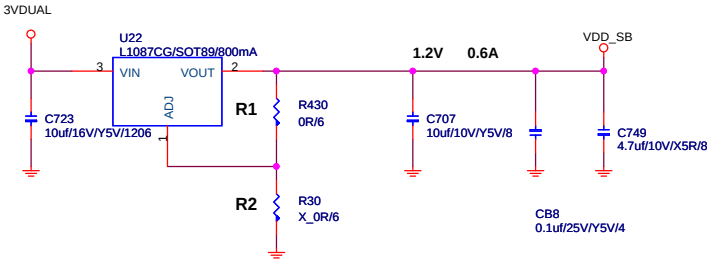


I31-0520803-O05

SHUTDOWN CONTROL						
Shutdown Pin Enable Threshold	–	VSD	1.14	1.24	1.34	V

Vo = Vref (1+R2/R1) + ladj x R2

1.25V reference voltage

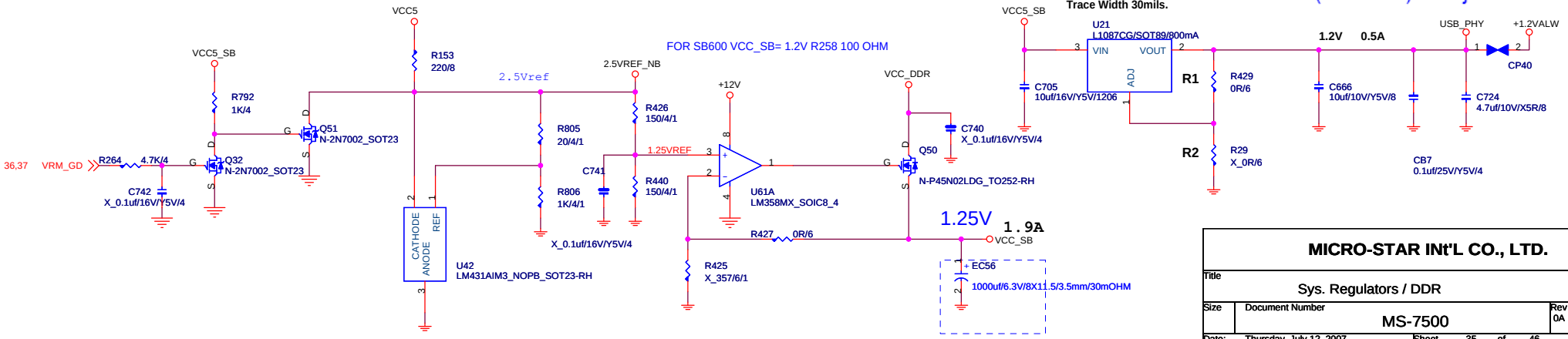


PA_SB700AA1

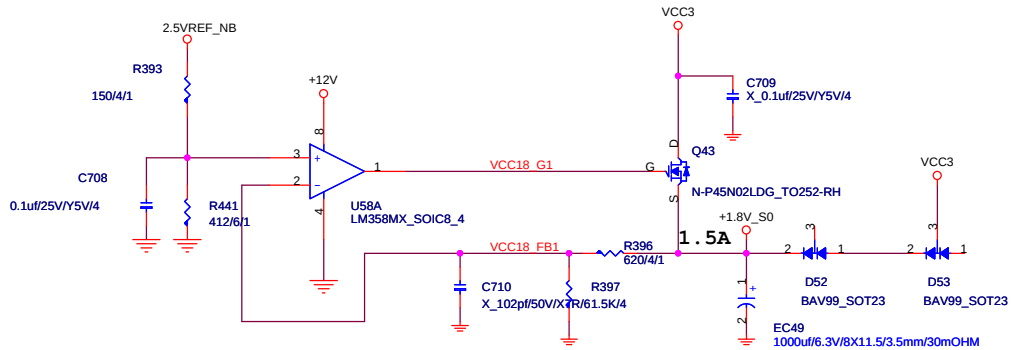
1.25V reference voltage

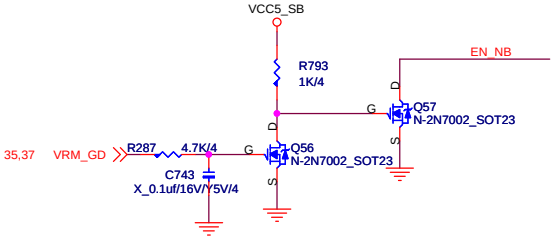
Vo = Vref (1+R2/R1) + ladj x R2

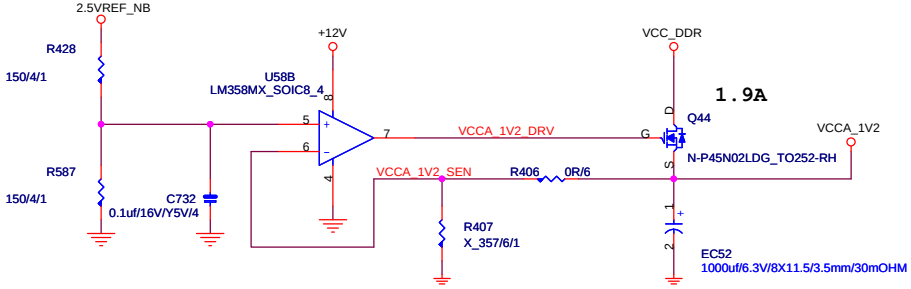
Trace Width 30mils.



MICRO-STAR INt'L CO., LTD.			
Title	Sys. Regulators / DDR		
Size	Document Number	MS-7500	Rev 0A
Date:	Thursday, July 12, 2007	Sheet 35 of 46	





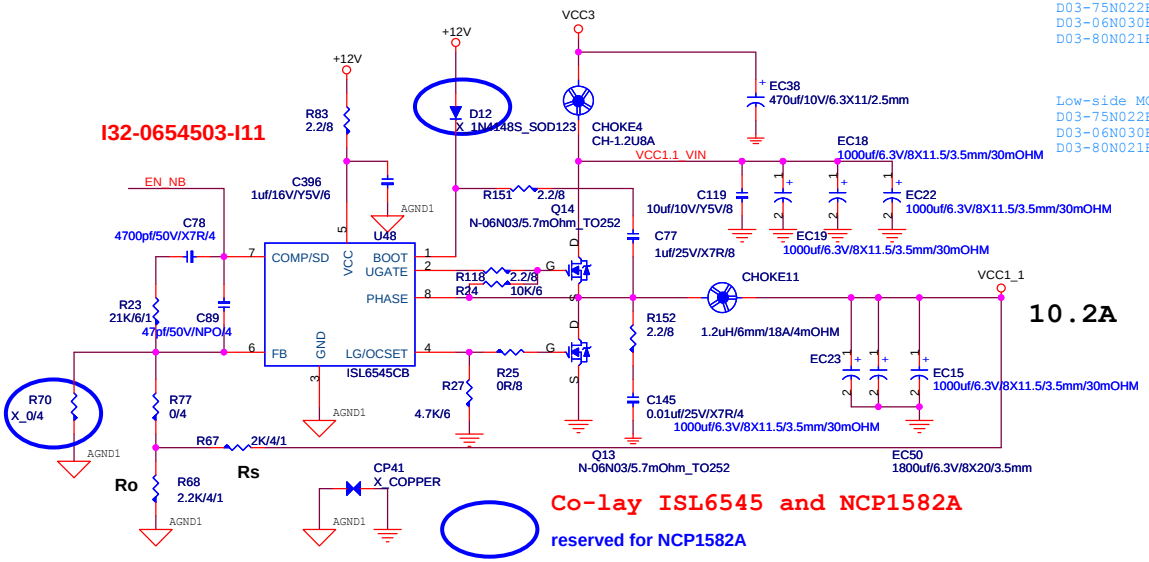


High-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

Low-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

- VLDT Max Current Requirement
  - HT Gen1 - 500mA
  - HT Gen3 - 1.4A

I32-0654503-I11



Co-lay ISL6545 and NCP1582A

reserved for NCP1582A

IF Q13,Q14 USE 9.m OHM , R27=5.1K

R27

$$V_{OUT} = 0.6V \bullet \frac{(R_S + R_O)}{R_O}$$

$$R_O = \frac{R_S \bullet 0.6V}{V_{OUT} - 0.6V}$$

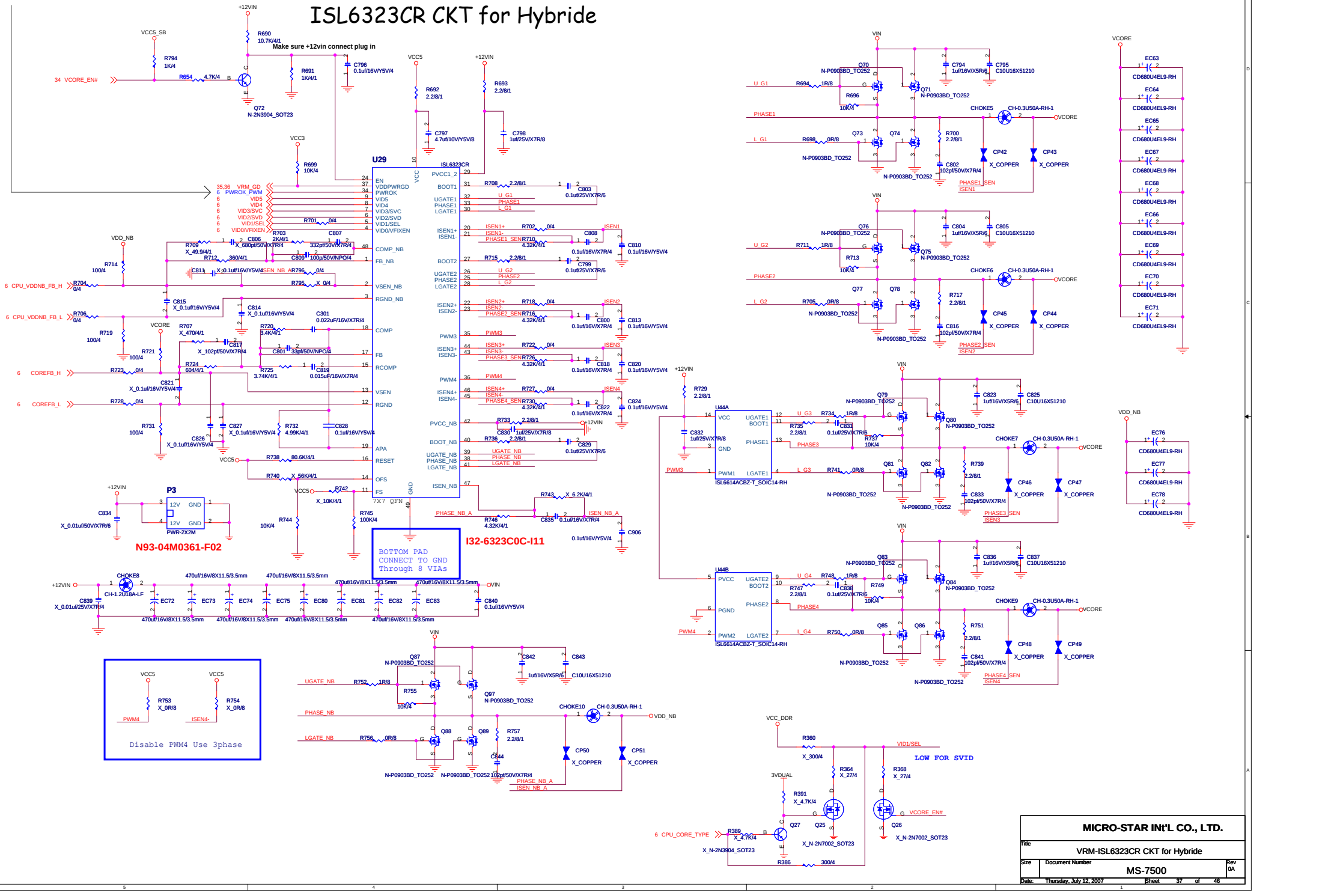
$$I_{PEAK} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (21.5µA

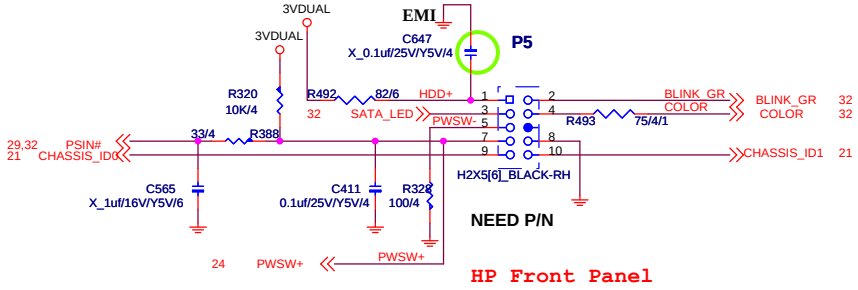
MICRO-STAR INt'L CO., LTD.		
Title: CORE PWR 1.2/1.1/CPU_HTVDD1.2		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 36 of 46	

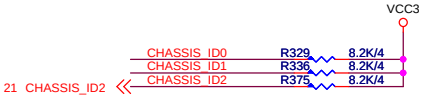
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWROK Input HIGH Threshold		2	-	-	V
PWROK Input LOW Threshold		-	-	0.8	V

ISL6323CR CKT for Hybride



Front Panel





HD_LED +	1	2	PWR_LED + (BLINK)
HD_LED -	3	4	PWR_LED – (COLOR)
GND	5	6	(key)
POWER_BUTTON#	7	8	GND
CHASSIS_ID0	9	10	CHASSIS_ID1

ATX Connector

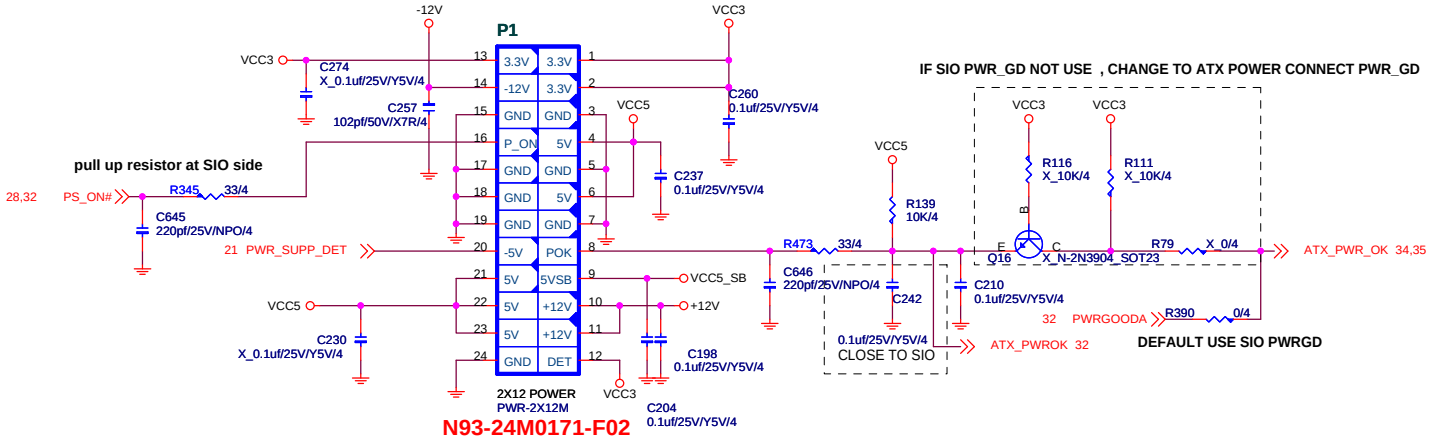
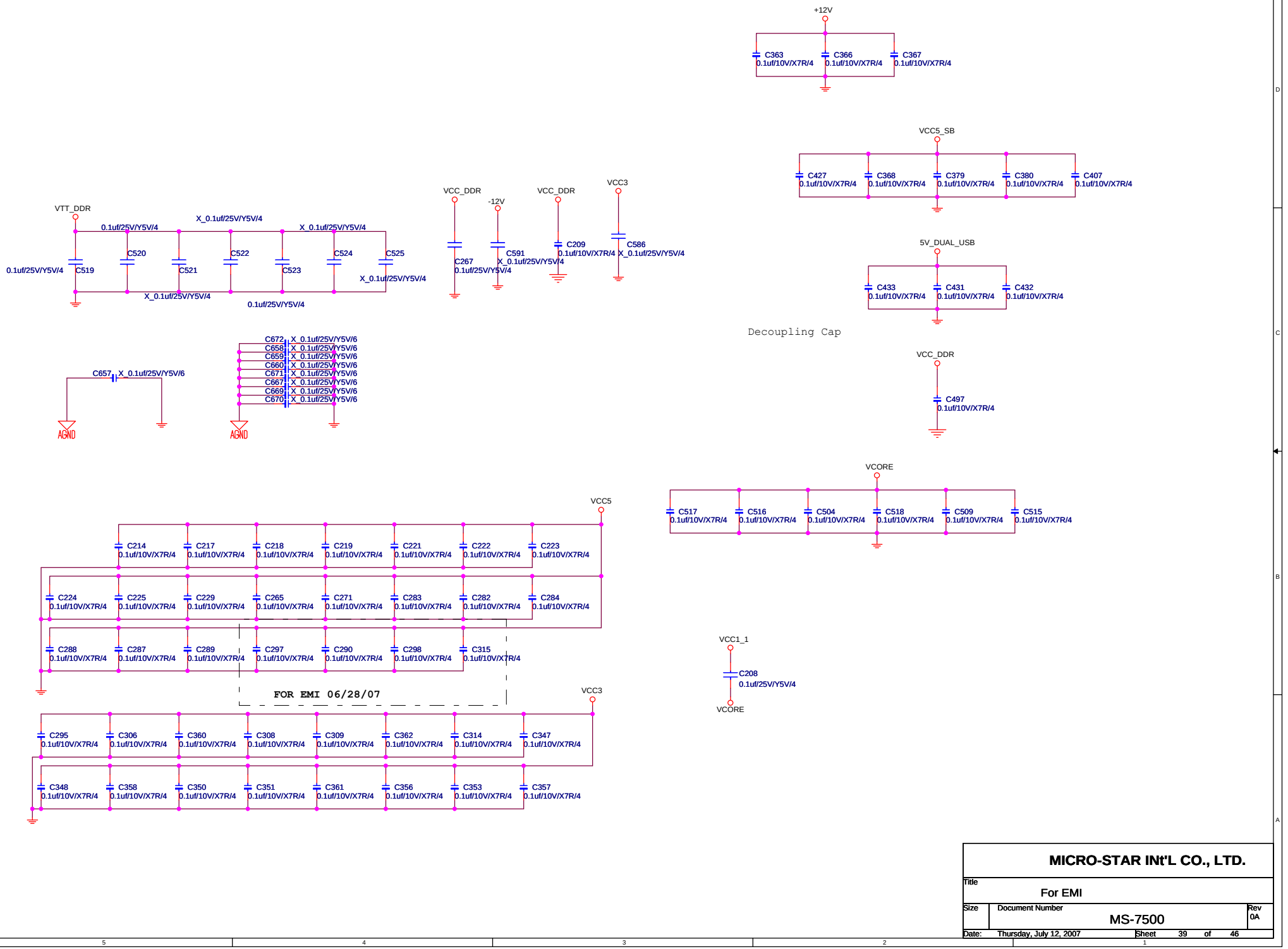


TABLE 5
POWER SUPPLY CONNECTOR PINOUT

	P1		
+3.3 V	13	1	+3.3 V
-12 V	14	2	+3.3 V
GND	15	3	GND
PSON#	16	4	+5 V
GND	17	5	GND
GND	18	6	+5 V
GND	19	7	GND
NOT USED	20	8	POWER OK
+5 V	21	9	+5 V STANDBY
+5 V	22	10	+12 V
+5 V	23	11	+12 V
GND	24	12	+3.3 V

MICRO-STAR INt'L CO., LTD.

Title	Front Panel	
Size	Document Number: MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 38 of 46	

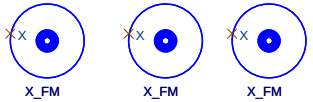


MICRO-STAR INt'L CO., LTD.

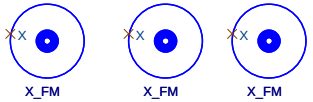
Title	For EMI	
Size	Document Number: MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 39 of 46	

Optics Orientation Holes

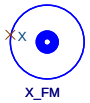
FM1 FM3 FM4



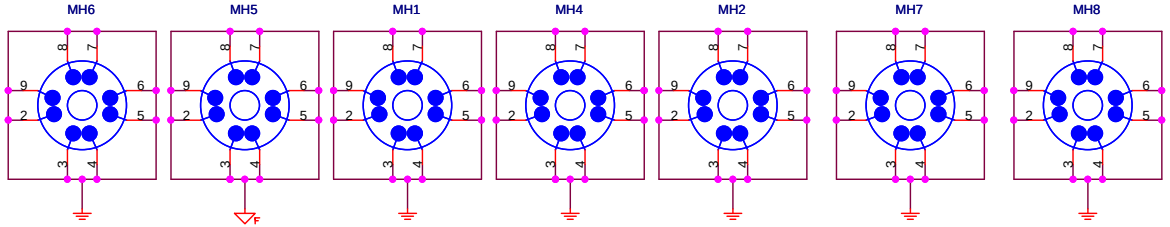
FM2 FM5 FM6



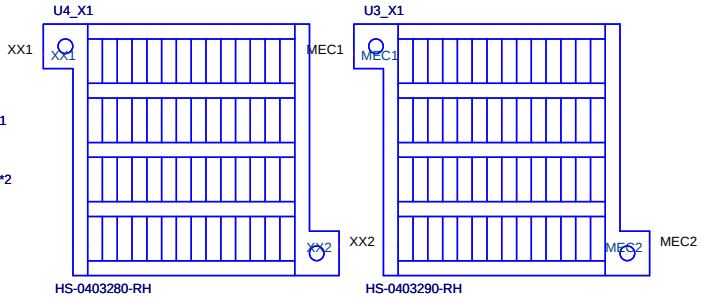
FM7



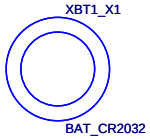
Mounting Holes



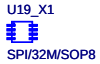
NB/SB FAN/HEAT-SINK



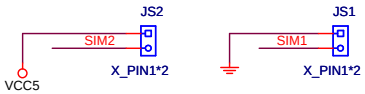
BATTERY



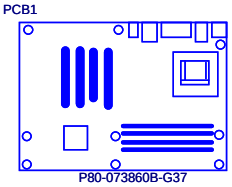
BIOS



Simulation

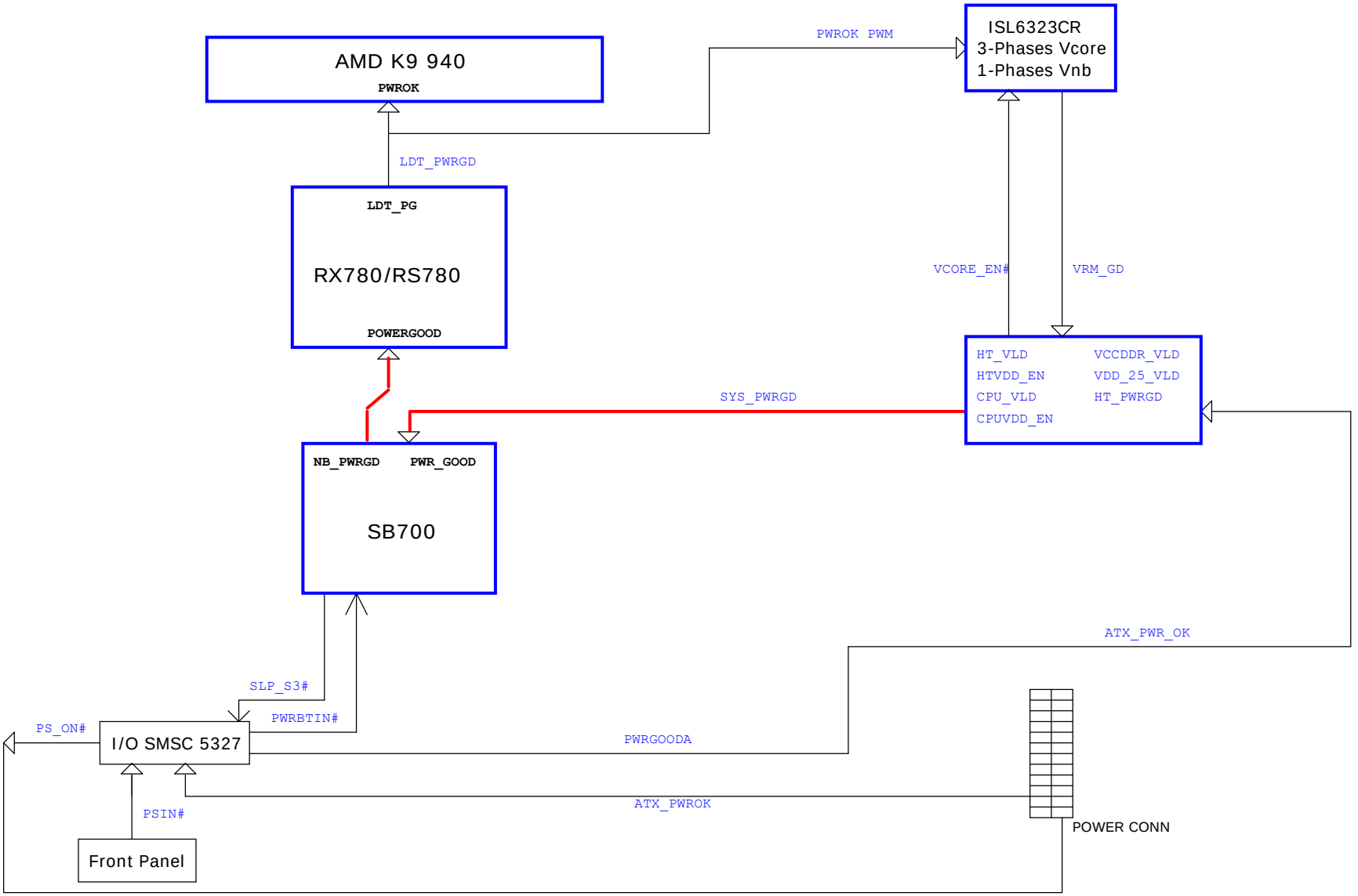


PCB

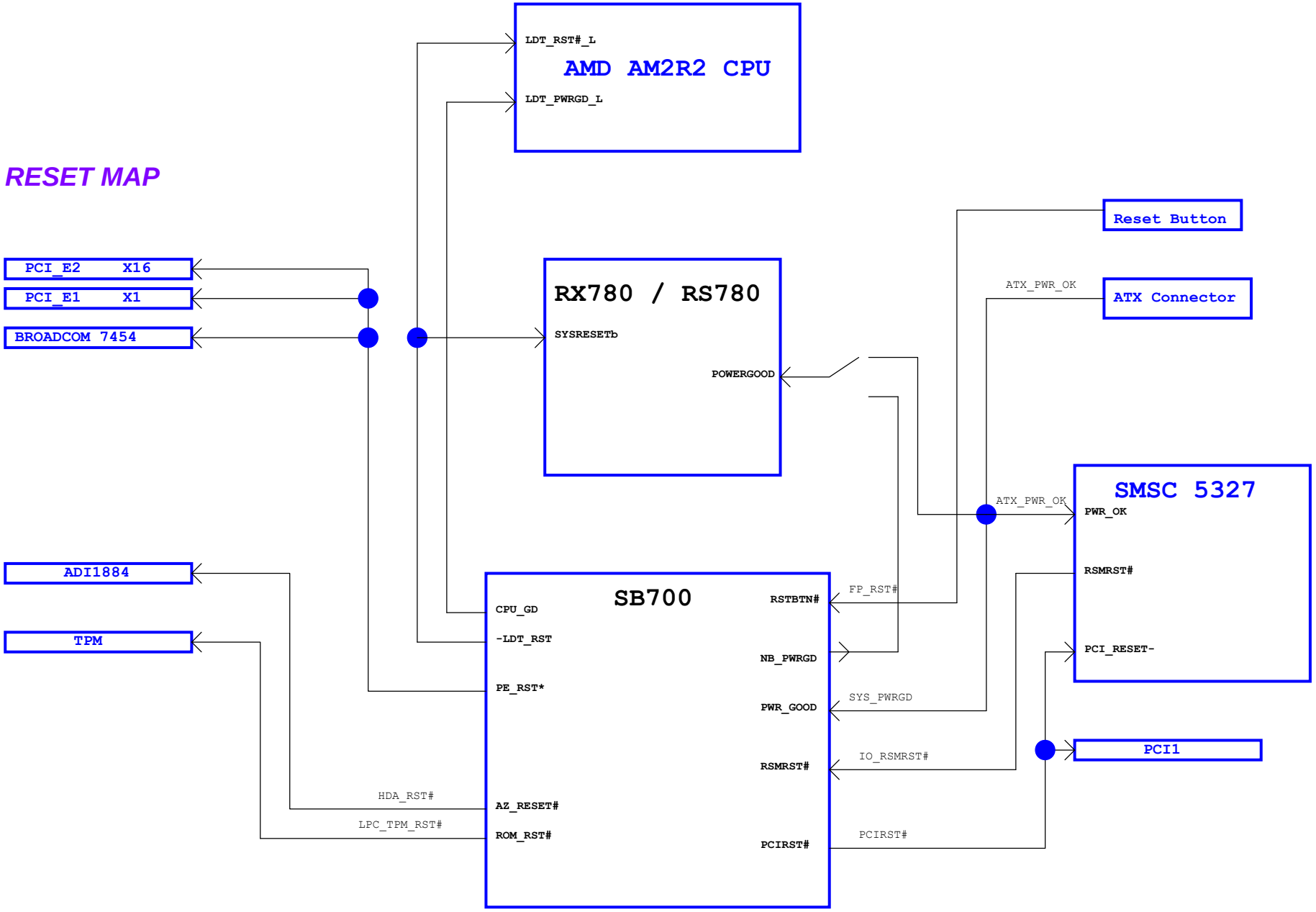


MICRO-STAR INt'L CO., LTD.		
Title: BOM - Option Parts		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 40 of 46	

PWROK MAP



MICRO-STAR INt'L CO., LTD.		
Title: PWROK MAP		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 41 of 46	



MICRO-STAR INt'L CO., LTD.		
Title: RESET MAP		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 42 of 46	

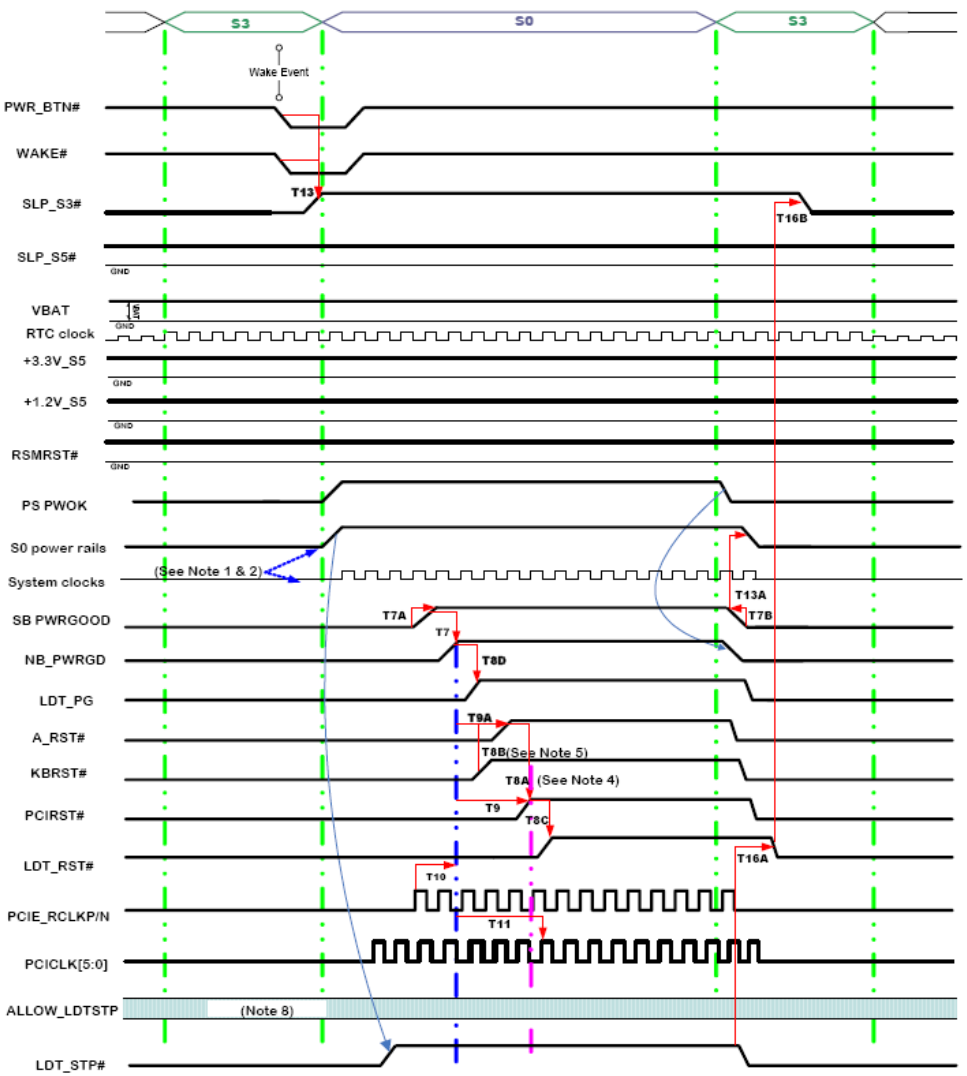


Figure 4-1: SB700 Power Up/Down Sequence

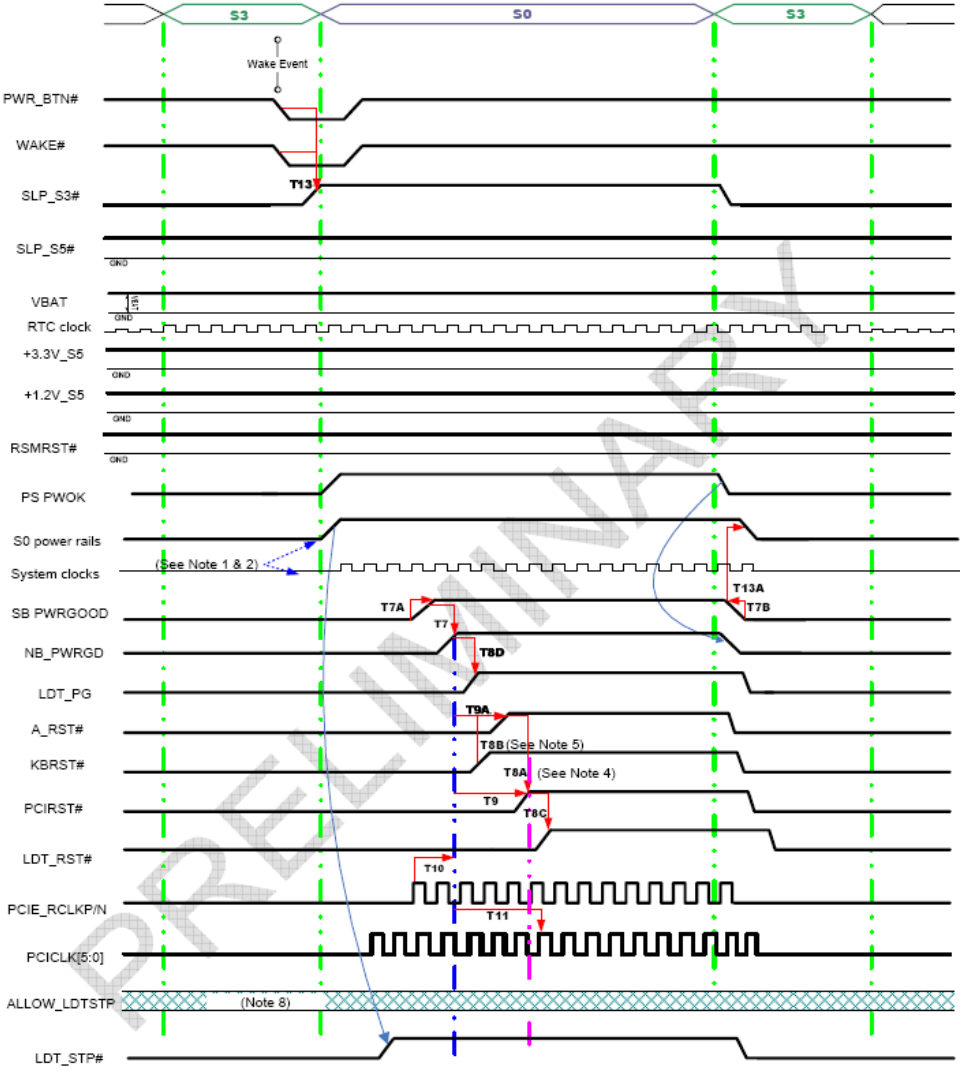
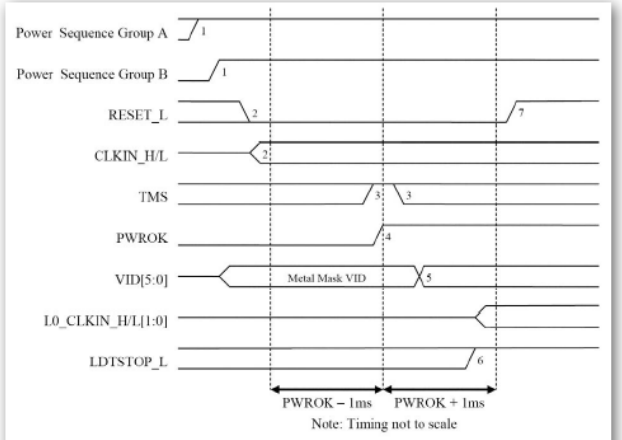


Figure 4-2: SB700 S3/S0 Power Up/Down Sequence

MICRO-STAR INt'L CO., LTD.		
Title: Power Sequence		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 43 of 46	



igure 2. **Power-up Power Supply and Signal Sequencing**

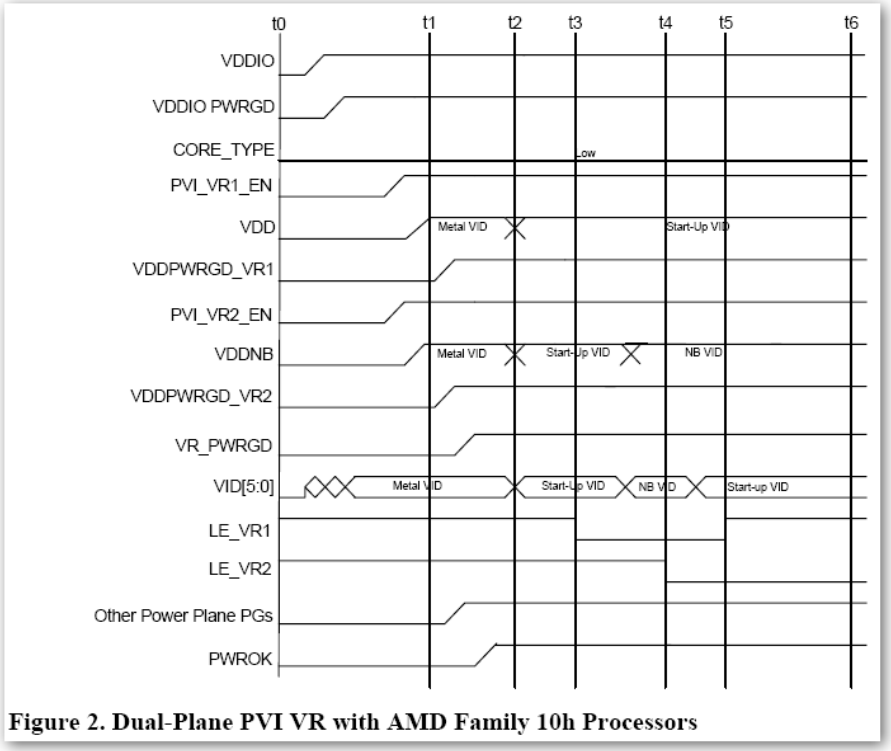


Figure 2. Dual-Plane PVI VR with AMD Family 10h Processors

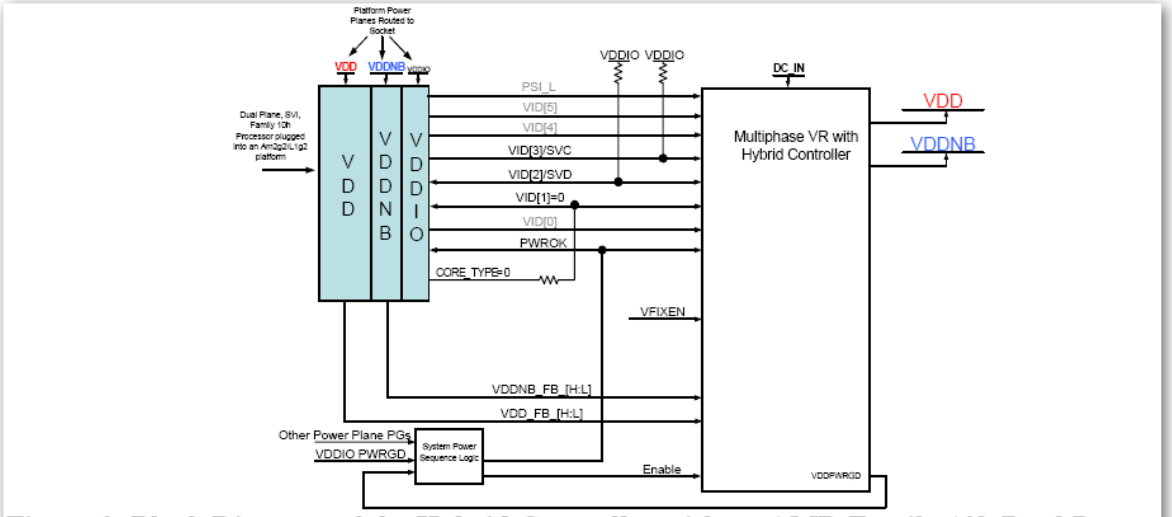
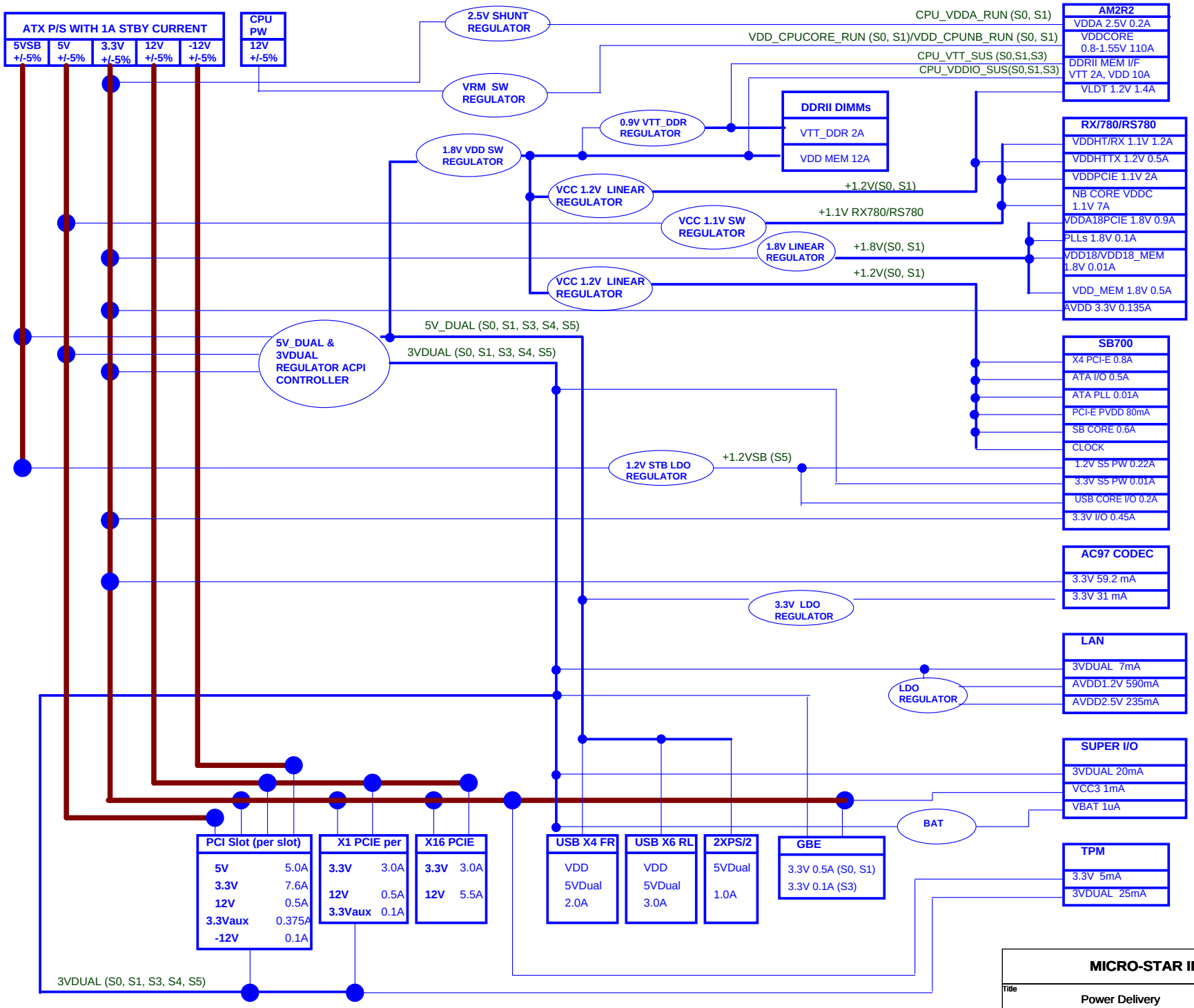


Figure 9. Block Diagram of the Hybrid Controller with an AMD Family 10h Dual Power Plane Processor (or Later) Operating in SVI Mode

MICRO-STAR INt'L CO., LTD.		
Title: CPU / VR Power Sequence		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 44 of 46	



MICRO-STAR INt'L CO., LTD.

Title	Power Delivery	
Size	Document Number: MS-7500	Rev 0A
Date: Thursday, July 12, 2007	Sheet 45 of 46	

MS-7500 0A

06/05/07 Preliminary release

06/15/07

Page 06:R108,R109,R657 AND R658 have been deleted.

Page 15:C542,C597 AND C745 have been added(FOR EMI).

Page 15:R93,R126,R165,R190,R199 R201,R167,R204,R270,R255,R179,R222,R236 and R248 have been deleted(using external CLK-GEN)

Page 15:R175,R179,Q15 and R291 have been added(level-shift for ALLOW_LDTSTOP).

Page 15:R197,R45 and R47 have been deleted(DVI single channel).

Page 18:R338,R339,R340 AND R361 have been deleted(using external CLK-GEN)

Page 19:R176,R211,R214 AND R215 have been deleted(using external CLK-GEN)

Page 19:R242 AND R250 have been deleted.

Page 19:R125 PULLUP 3VDUAL.

Page 19:Add R276.

Page 23:R285,R183,R212,R186,R288,R203R,R189,R366,R357,R352,R351and R344 have been deleted(SB700 HAS 15K INTERNAL PULLUP FOR PCI_AD[30:23)

Page 24:R187,R431,R433 AND R432 have been deleted(using external CLK-GEN)

Page 25:R408,R409,R394,R402,R414,R415,R410,R424,R430,R422 and R423 have been deleted(using external CLK-GEN)

Page 28:R625,R626,R627,R628,R629,R630 have been deleted(using DVI single channel)

Page 31:C771 and C746 have been added(FOR EMI).

06/22/07

Page 06:C157,C158,R99 have been unpopulated,RN3 and R102 have been populated.

Page 06:U51,RN2 have been deleted(for AMD recommand),R74 and J80 have been added.

Page 06:Add R183 and Q17(level-shift).

Page 15:R42,RN43 and Q104 have been deleted,U62 has been added.

Page 15:R172,R175,R181,R192 and R187 have been changed from 3Kohm to 4.7Kohm.

Page 15:R182 has been changed from 2Kohm to 10Kohm.

Page 15:C570 has been changed from 2.2uF to 4.7uF.

Page 17:Add ferrite bead L18,L26,L27,FB19,FB22.

Page 18:L10,L13,L16 and L20 have been populated.

Page 18:C654 and C661have been changed from 10uF to 22uF.

Page 18:C655 and C733 have been changed from 1uF to 2.2uF.

Page 15:R161,R223,R230 and R231 been changed from 10Kohm to 8.2Kohm.

Page 19:R241 has been changed from 5.1Mohm to 20Mohm,R242 has been added.

Page 19: C323,C354,Y4,R168 have been deleted.U4.J21 connected to GND(25M_X1).

Page 20:L29,C412,C924 have been unpopulated.

Page 21:RN36,RN38,Rn35,RN39,Rn40,C372,C511,C535 and C707 have been deleted,R278,R279 and R280 have been added.

Page 21:Add R186 and Q22 (level-shift).

Page 21:SMBDATA1 and SMBCLK1 have been connected U10.

Page 22:Add C394,C513,C748,L22,L36,L41 and EC84,delete C484,C527,C723.

Page 22:C489,C717,C734,C735 and C772 have been changed from 10uF to 22uF.

Page 22:C378,C390,C480,C507,C508,C561,C563,C564,C567,C571,C714,C736,C744 and C747 have been changed from 0.1uF to 1uF.

Page 22:C392,C510,C527,C528 and C721 have been changed from 1uF to 2.2uF.

Page 23:R308,R318 and R333 have been unpopulated,R311 have been populated.

Page 25:Add RN 58,RN59,RN60.

Page 26:RN43,RN47 have been unpopulated.

Page 27:R180,R300 have been changed from 3Kohm to 4.7Kohm,and R89,R91 have been changed from 2.2Kohm to 6.8Kohm.

Page 28:R581~R585,R578~R580 have been changed from 18ohm to 18.2ohm,and R372,R374 have been changed from 2.2Kohm to 6.8Kohm.

Page 28:L21~L24 have been deleted.

Page 31:R177 has been changed from 10ohm to 22ohm.

Page 34:Add R394,C246 and Q45 (AMD recommand).

Page 35:Add R673 (CPU_VDDIOFB_L).

Page 35:Add C723,U22,R430,R30,C707,cb8 and C749 (for PA_SB700AA1).

Page 40:Add U4_X1 (SB HEATSINK).

06/26/07

Page 16:Add R807,R808,C34(for NB MEM_VREF).

Page 18:U6 has been changed from ICS9LPRS472 (MLF 64pin) to ICS9LPRS475 (TSSOP 56pin).

Page 18:R231and R223 have been deleted.

Page 20:L29 has been deleted and CP14 has been added.

06/27/07

Page 34:C245 has been changed from 0.1uF to 4.7uF.(power sequence)

06/28/07

Page 39:Add C290,C297,C298,C315 for EMI.

06/29/07

Page 15:R173,R135,R574,R196 have been deleted and R189,R190,R196 have been added.

Page 16:R148,R162,C202 and C203 have been unpopulated.

Page 19:Add R809,R810,C750,J81 FOR AMD debug.

Page 21:R125 has been deleted.

Page 22:C414 has been populated.

Page 24:R766 and R769 have been populated,R767 and R768 unpopulated.(for HP LAN LED spec)

Page 27:D44,D45 and D46 pin2 connect to VCC3.

Page 36:Add D52,D53.

07/04/07

Page 6:R64 has been unpopulated.

07/05/07

Page 34:Add R399,C247,Q46 for S3 function.

07/09/07

Page 13:Adding C920,C925 0.01 uF stitching capacitors for crossing a split when these signals change different reference layer.

Page 19:Adding C751,C752 0.1 uF stitching capacitors for crossing a split when these signals change different reference layer.

07/11/07

Page 21:Addied C387 0.1 uF stitching capacitors for crossing a split when these signals change different reference layer.

Page 32: R575 has been deleted.

MICRO-STAR INt'L CO., LTD.		
Title: History		
Size	Document Number: MS-7500	Rev: 0A
Date: Thursday, July 12, 2007	Sheet 46 of 46	