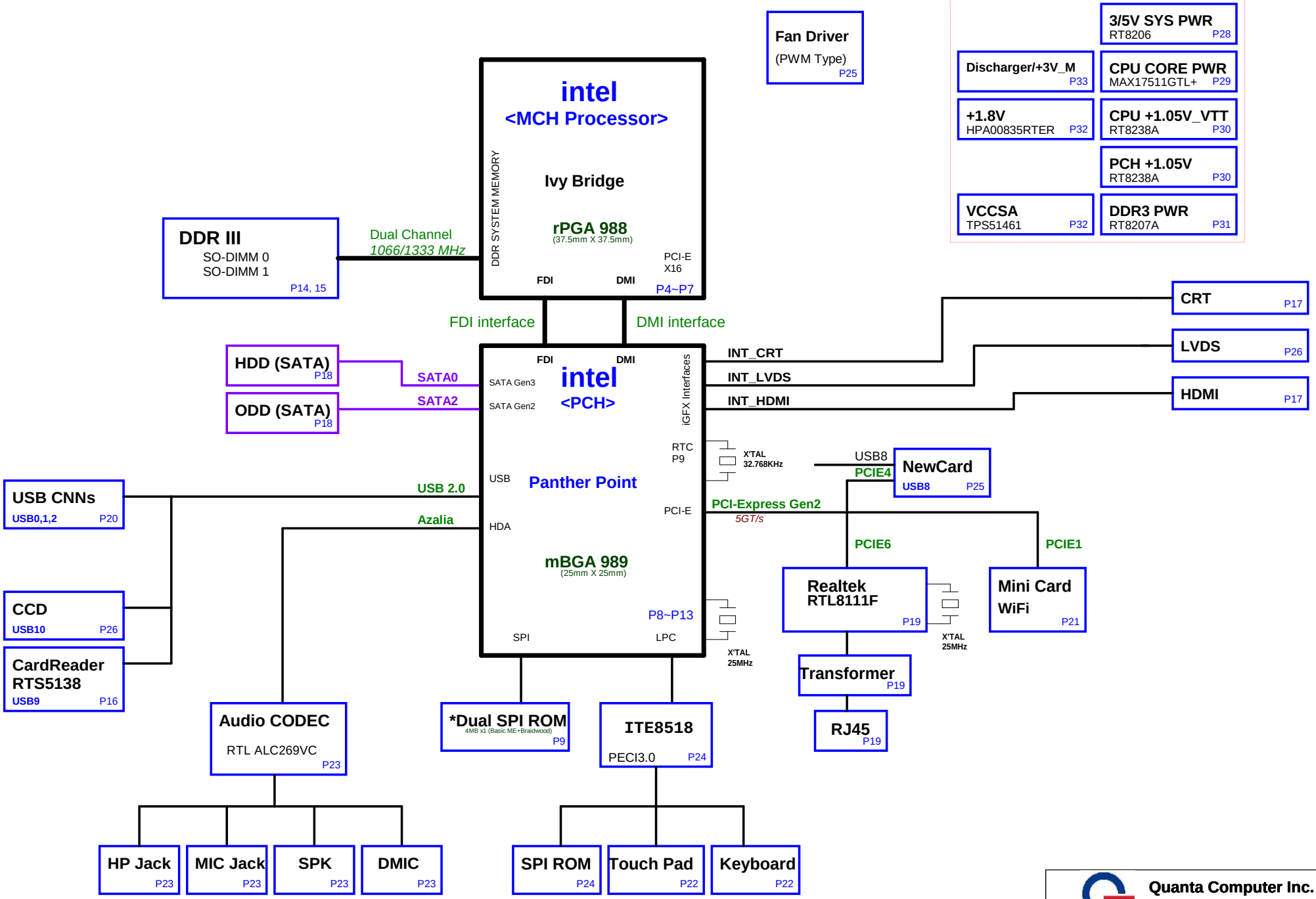
FH5B BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : FH5B

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	Block Diagram	1A

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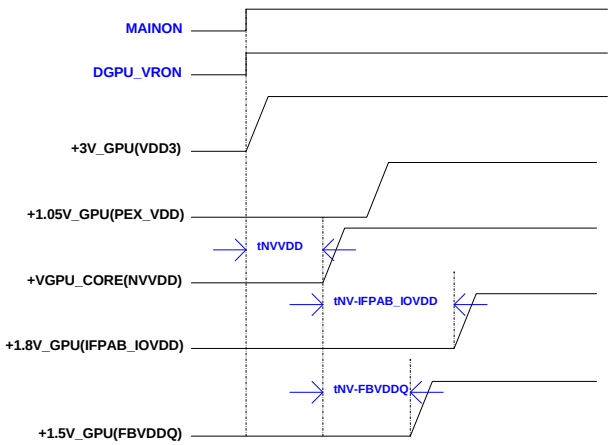
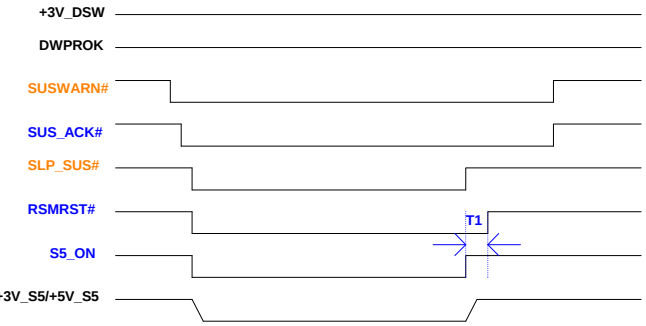
N12P-GE Power Up Sequence



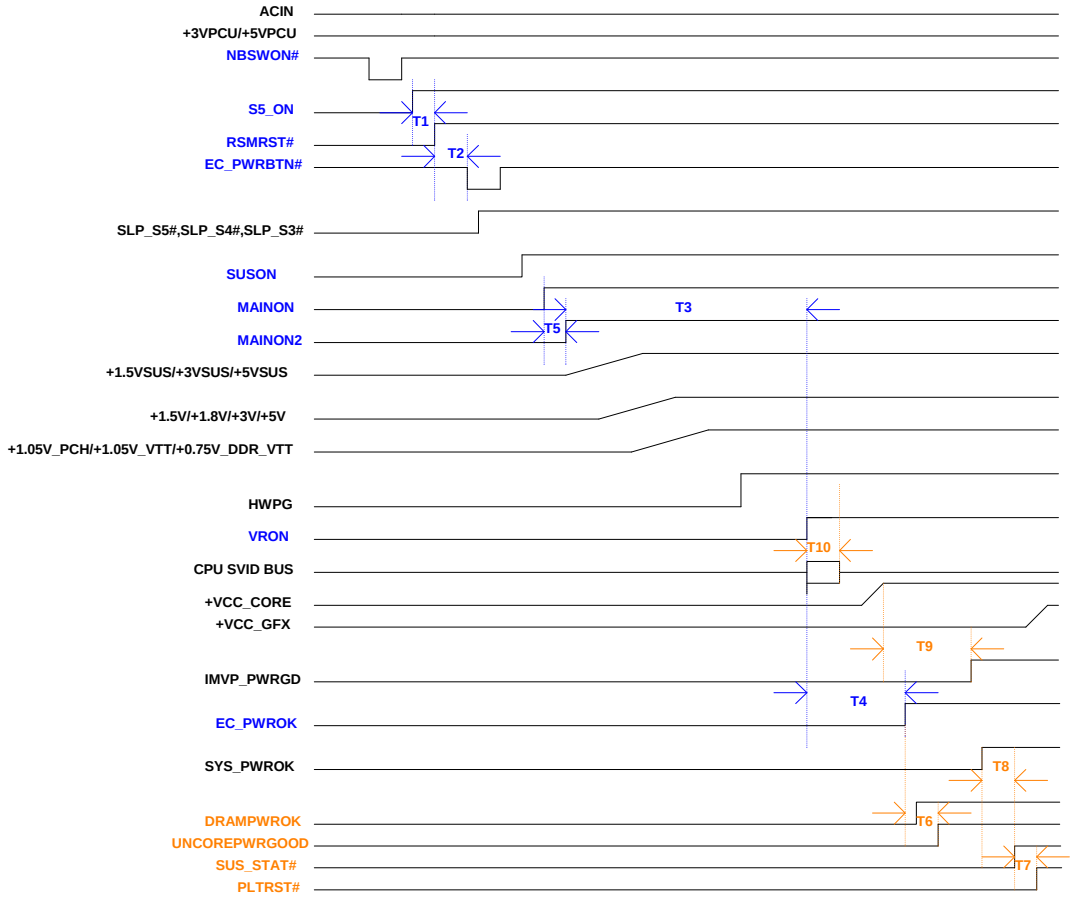
N12P-GE Power up Sequence
tNVVDD>0
tNV-IFPAB_IOVDD>0
tNV-FBVDDQ>0

Deep S4/S5 off-on Sequence

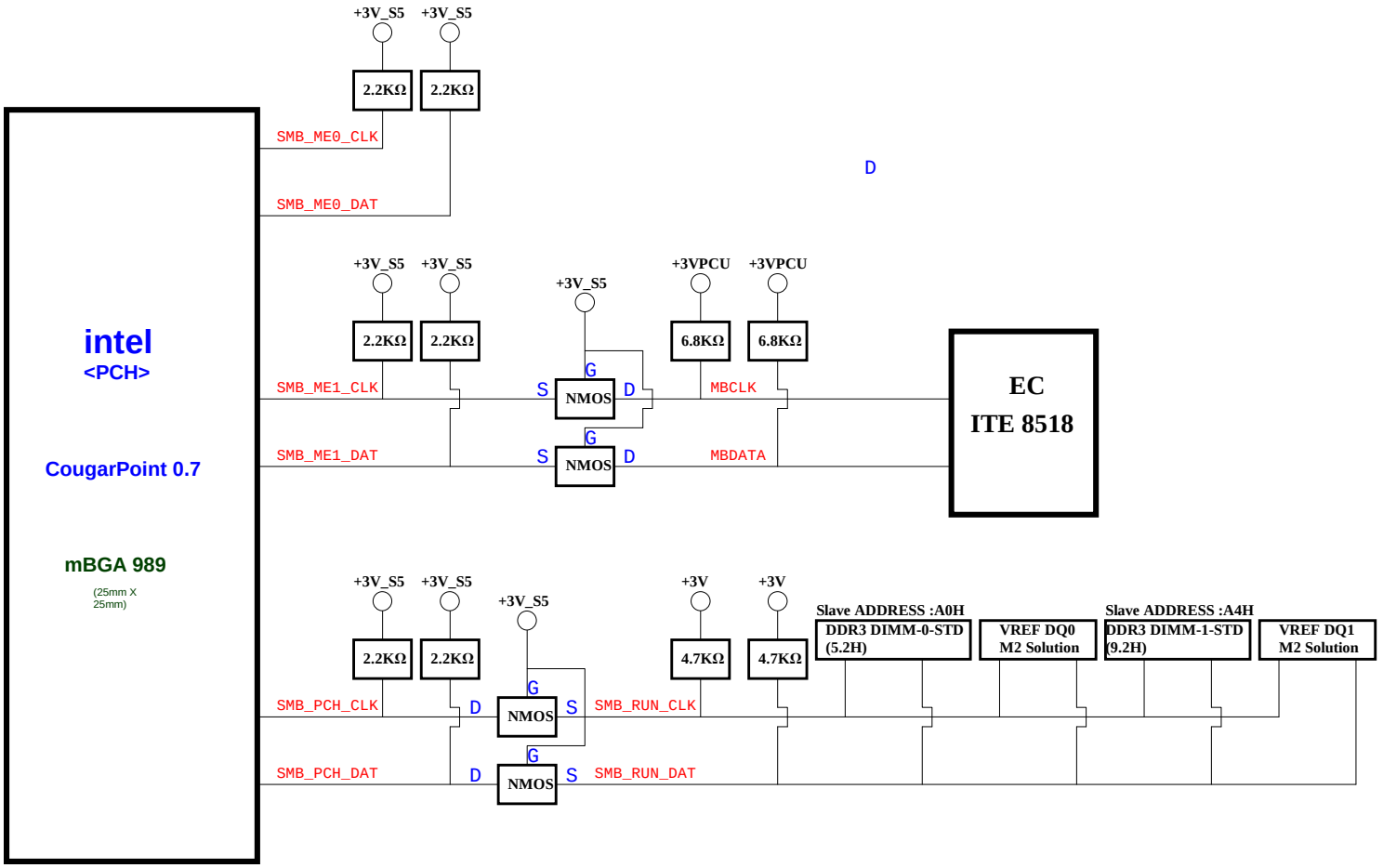


Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence



System Power Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON to MAINON2 =500us
T6: EC_PWROK to UNCOREPWRGOOD =2ms(Min)
T7: SUS_STAT# to PLTRST# =60us(Min)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9: +VCC_CORE to IMVP_PWRGD =5ms(Max)
T10: VRON to accept SVID command. =5ms(Max)



Quanta Computer Inc.
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	SMBus Address	1A

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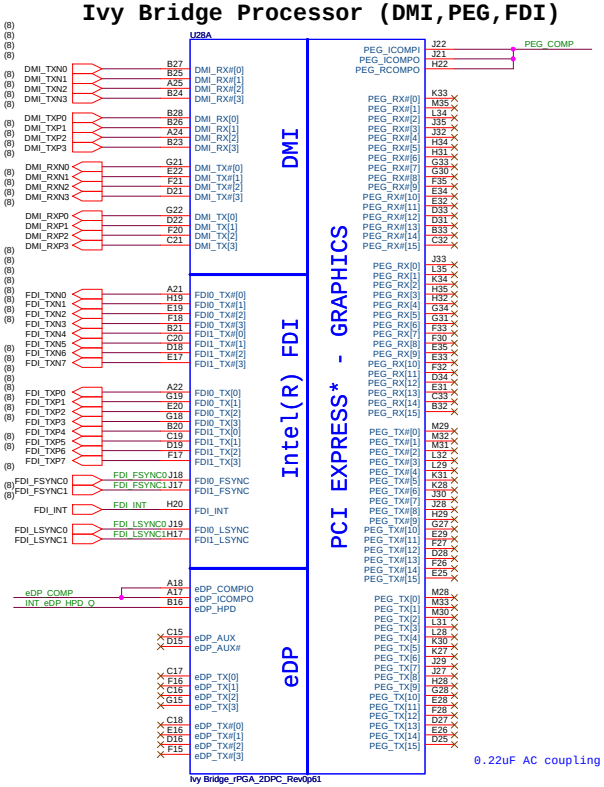
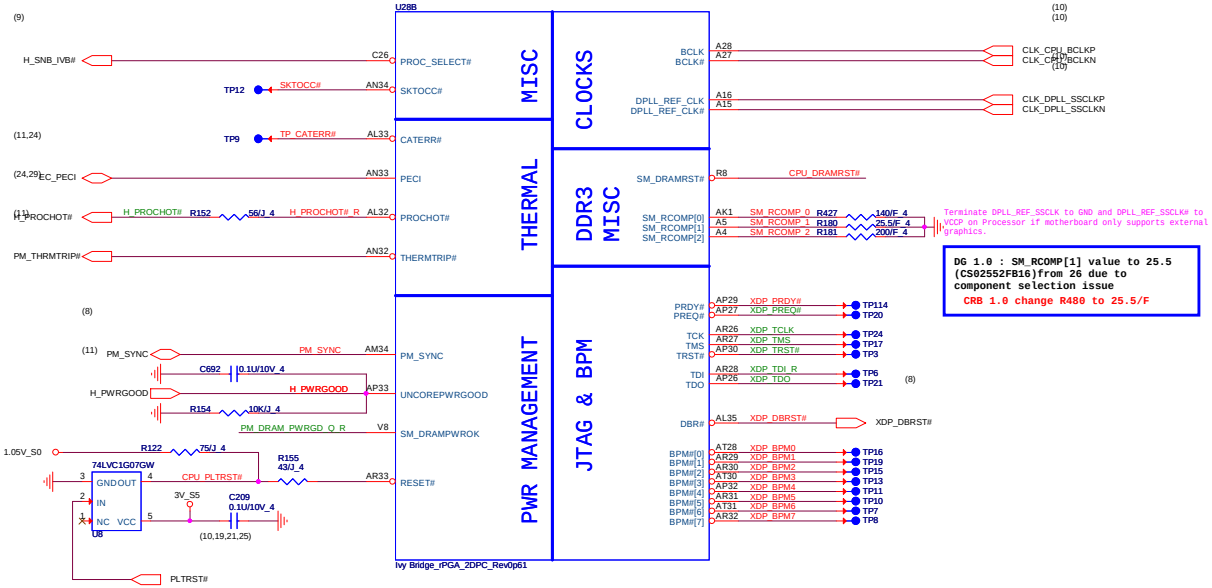
Ivy Bridge Processor (DMI,PEG,FDI)



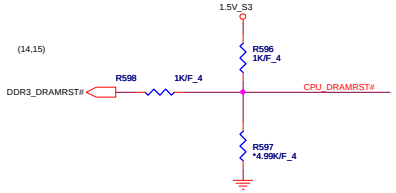
0.22uF AC coupling Caps for PCIE GEN1/2/3

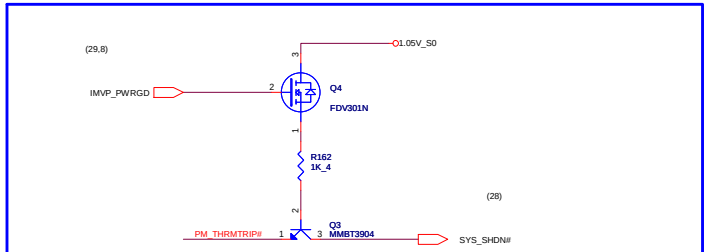
Ivy Bridge Processor (CLK,MISC,JTAG)

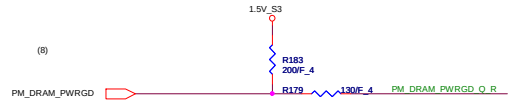


DG 1.0 : SM_RCOMP[1] value to 25.5 (CS02552FB16)from 26 due to component selection issue

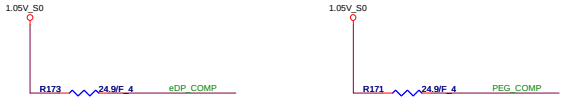
CRB 1.0 change R480 to 25.5/F







DP & PEG Compensation



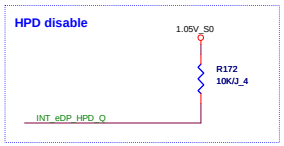
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

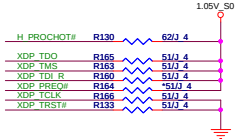
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

eDP Hot-plug

CAD Note: Place PU resistor within 2 inches of CPU



Processor pull-up(CPU)



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	Ivy Bridge 1/4	1A

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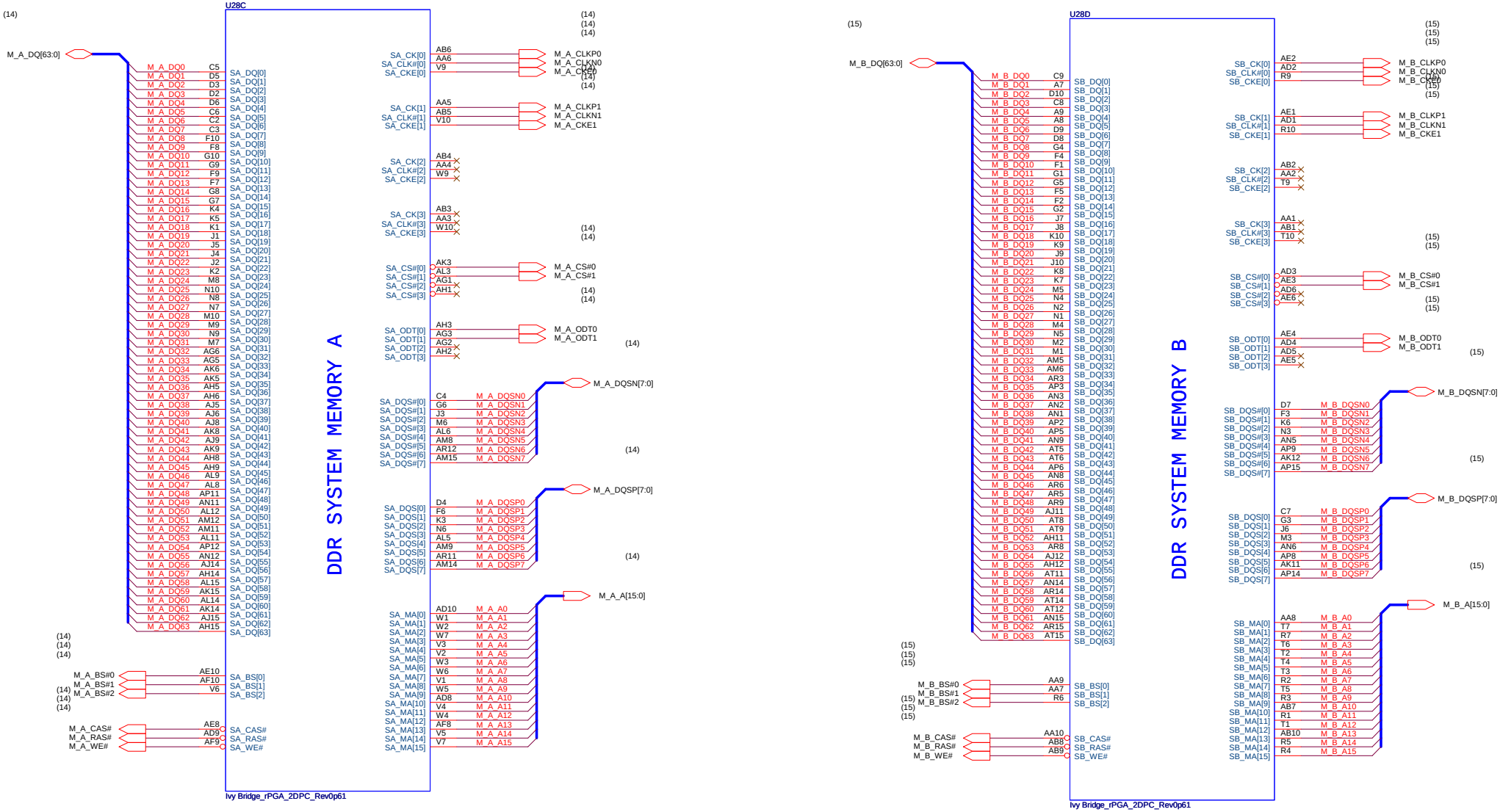
Ivy Bridge Processor (DDR3)



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	Ivy Bridge 2/4	1A

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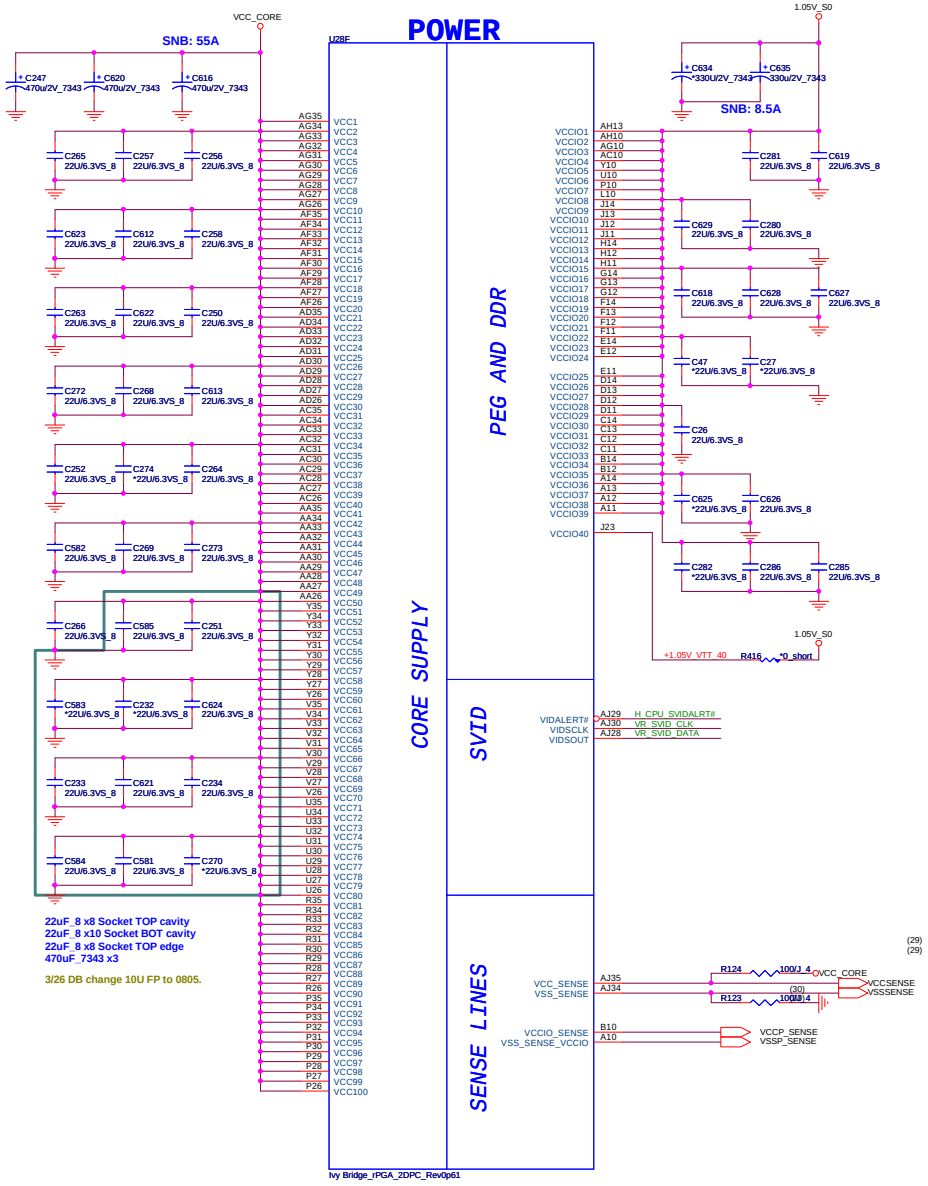
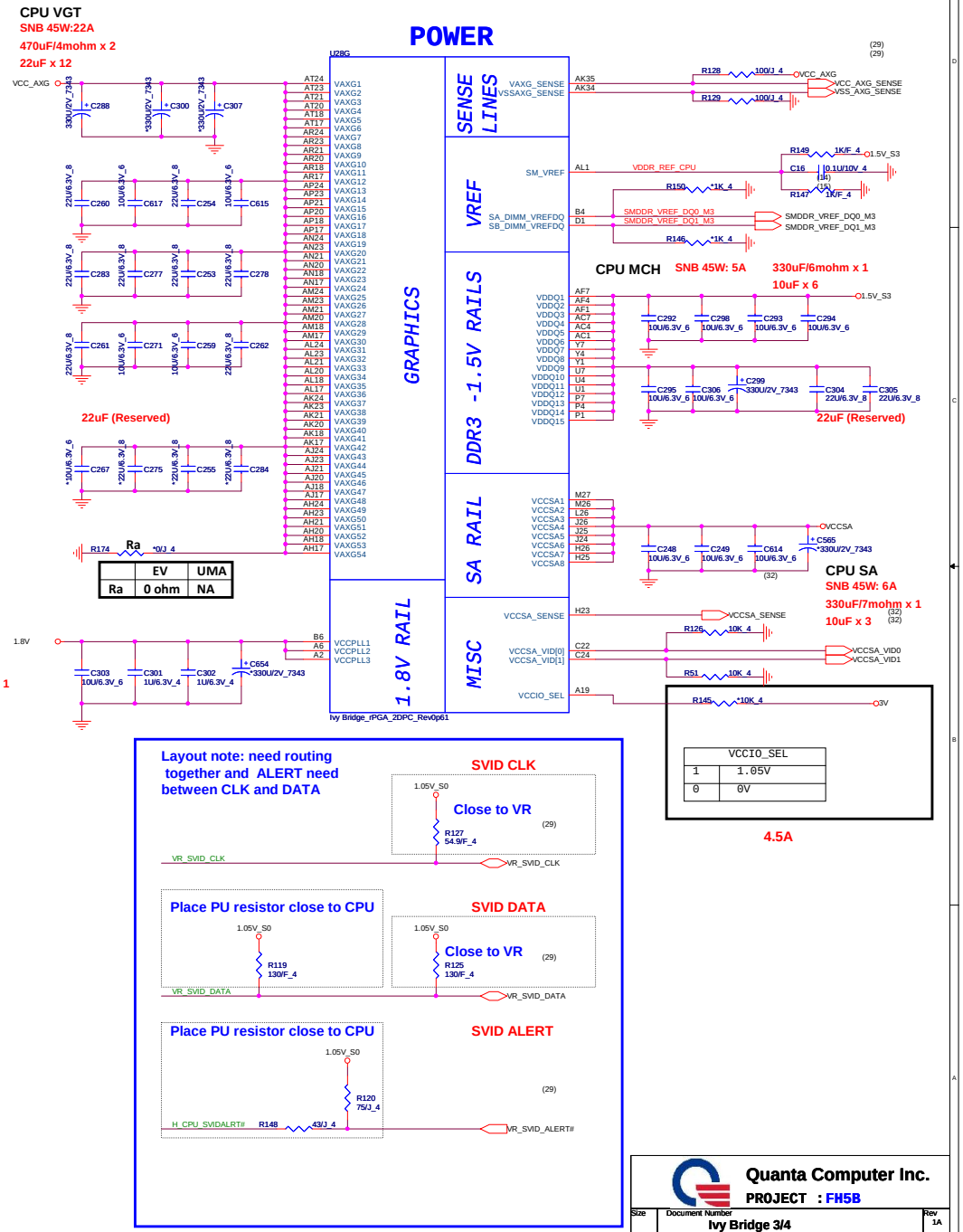
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

Ivy Bridge Processor (POWER)



Ivy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK — Close to VR — R127 54.9/F_4 — VR_SVID_CLK

SVID DATA — Place PU resistor close to CPU — R119 130/F_4 — Close to VR — R125 130/F_4 — VR_SVID_DATA

SVID ALERT — Place PU resistor close to CPU — R120 75/J_4 — R148 43/J_4 — VR_SVID_ALERT#

VCCIO_SEL	
1	1.05V
0	0V

	EV	UMA
Ra	0 ohm	NA

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	Ivy Bridge 3/4	1A

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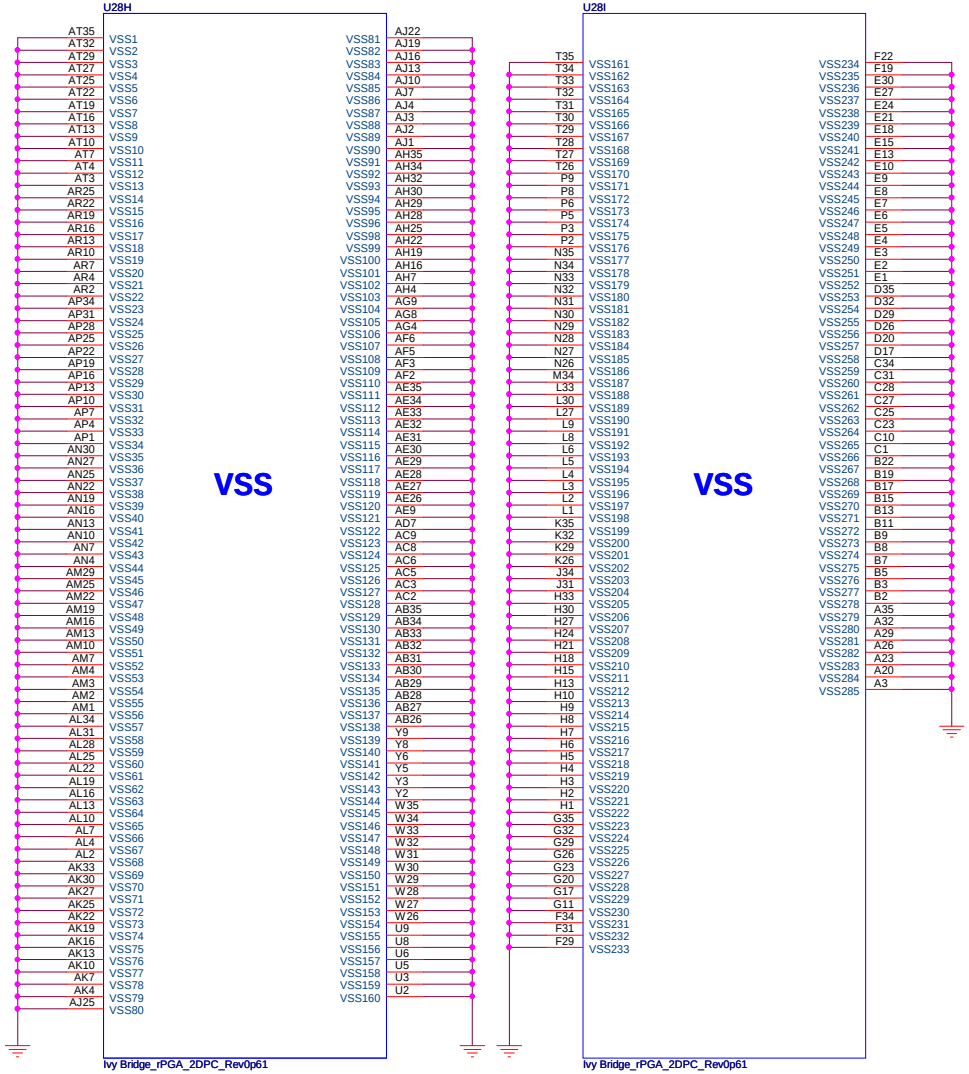
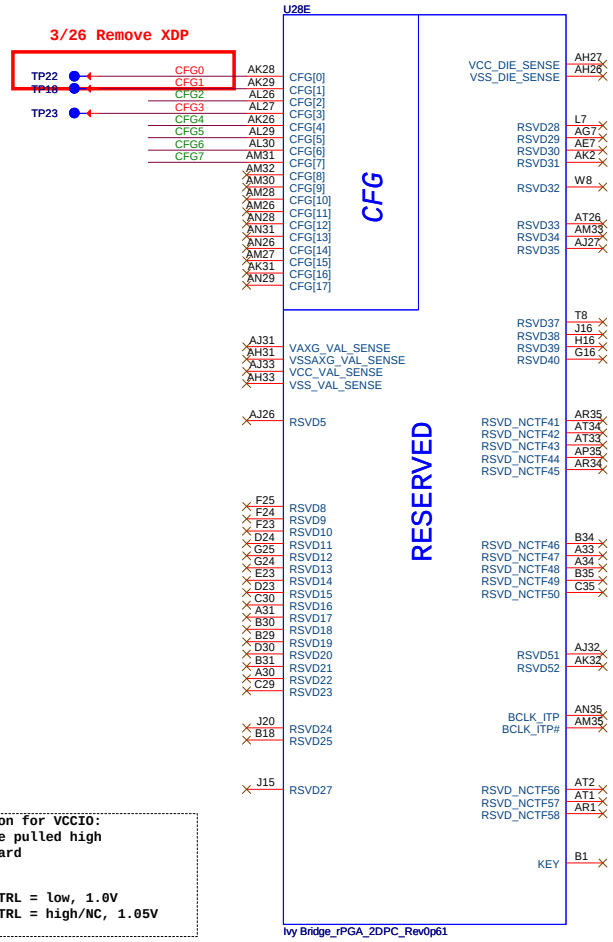
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



Voltage selection for VCCIO:
this pin must be pulled high
on the motherboard

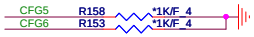
On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

For rPGA socket, RSVD59 pin should be left NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG3 PEG Static x4 Lane	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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	Ivy Bridge 4/4	1A

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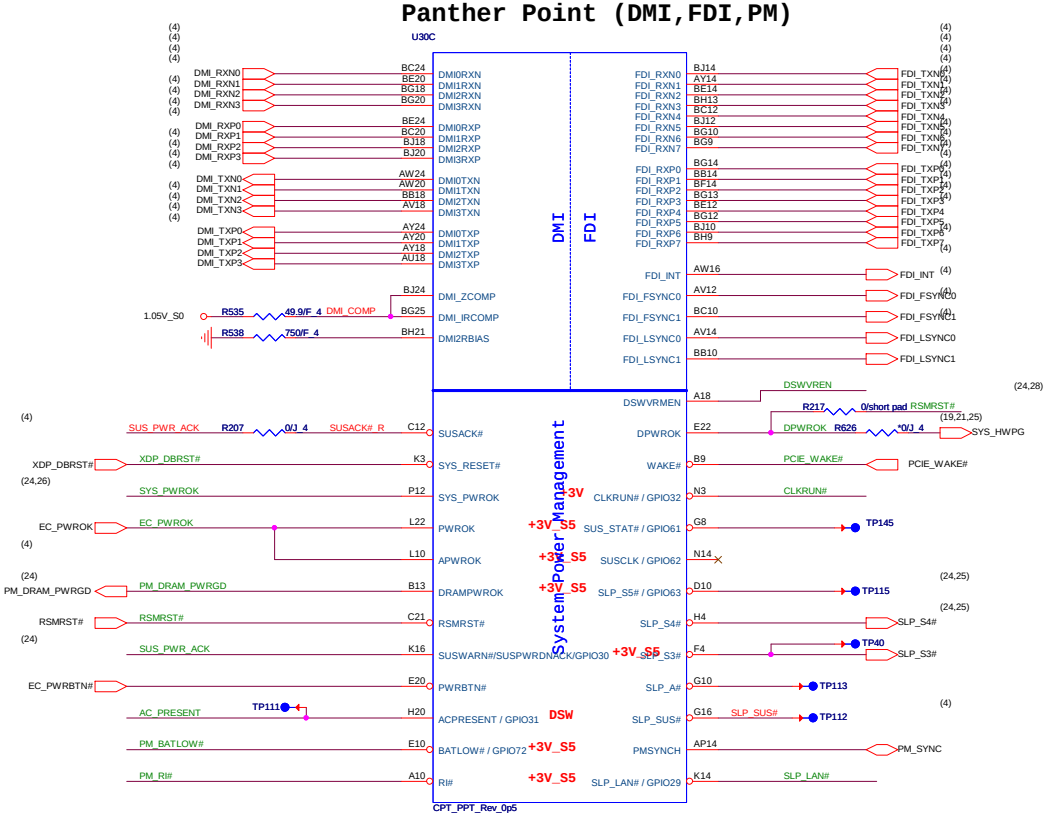
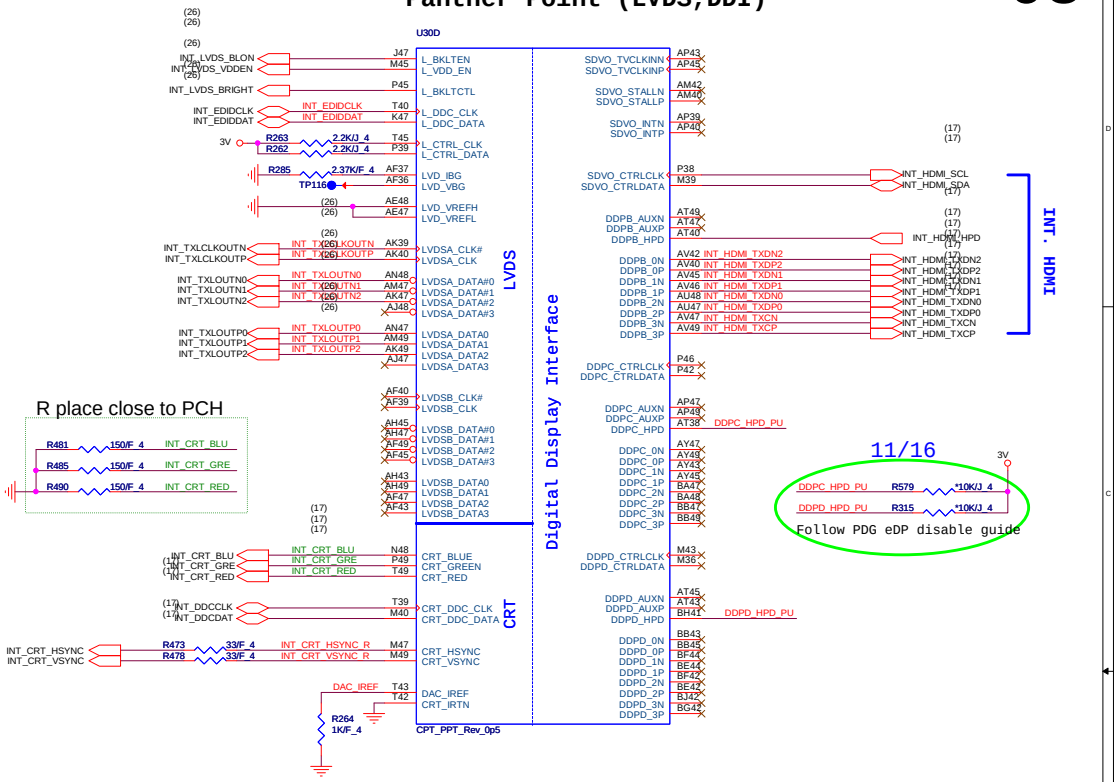
Panther Point (DMI,FDI,PM)



Panther Point (LVDS,DDI)

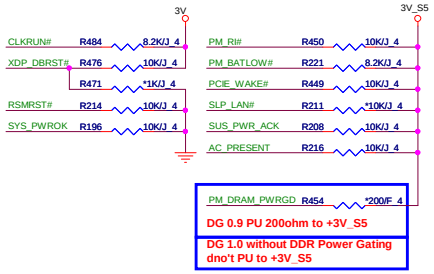


R place close to PCH

11/16

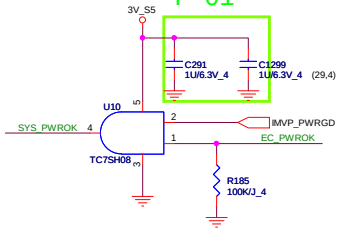
Follow PDG eDP disable guide

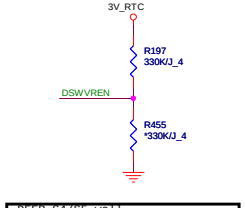
PCH Pull-high/low(CLG)



System PWR_OK(CLG)

F-01





DEEP S4/S5 well
On Die DSW VR Enable

High = Enable (Default)
Low = Disable

DPWROK FOR DSW (Deep Sx Well)

Quanta Computer Inc.
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	Panther Point 1/6	1A
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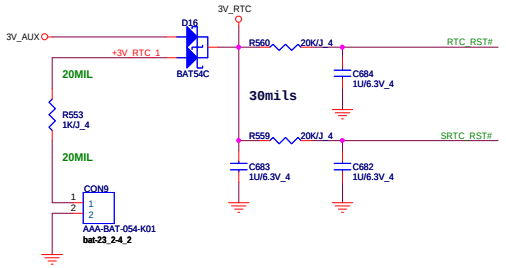
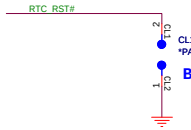
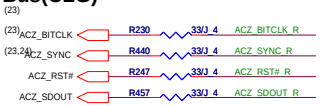
RTC Circuitry(RTC)



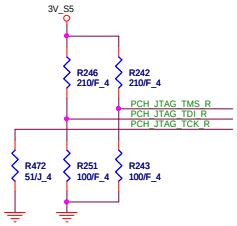
RESET JUMP (Near ROOM DOOR)



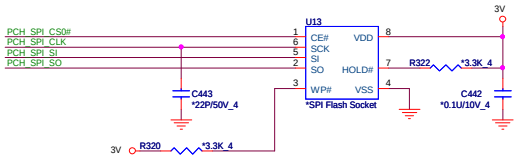
HDA Bus(CLG)



PCH JTAG Debug (CLG)



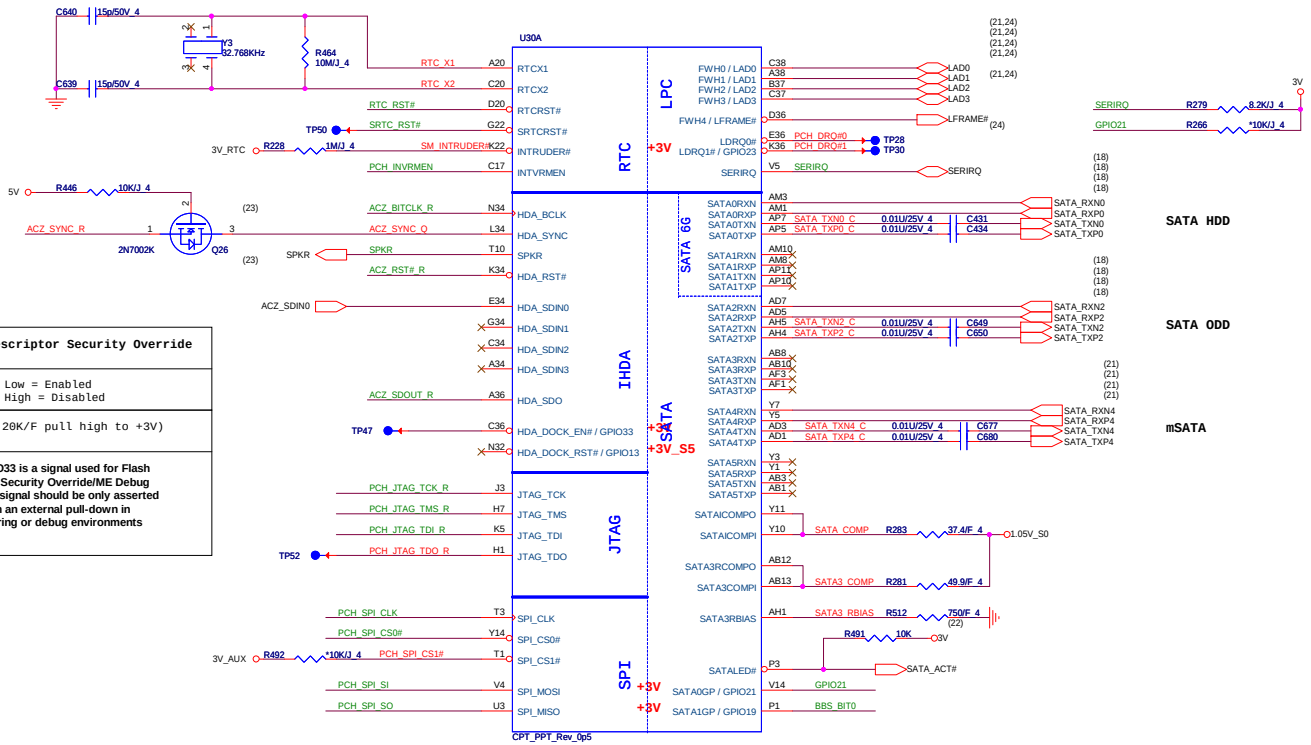
PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH2(CLG)

Panther Point (HDA,JTAG,SATA)



Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled
(Internal 20K/F pull high to +3V)	

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting internal PD	PWROK	**0 = Default (weak pull-down 20K)** 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override internal PU	PWROK	0 = "top-block swap" mode **1 = Default (weak pull-up 20K)**
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1] internal PU	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0] internal PU	PWROK	
HDA_SDO	Flash Descriptor Security internal PD	RSMRST	**0 = Default (weak pull-up 20K)** 1 = Override
DF_TVS	DMI/FDI Termination voltage internal PD	PWROK	**0 = Set to Vss** **1 = Set to Vcc (weak pull-up 20K)**
GPIO28	On-die PLL Voltage Regulator internal PU	RSMRST#	0 = Disable **1 = Enable (Default)**
HDA_SYNC	On-Die PLL VR Voltage Select internal PD	RSMRST	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Intel ME TLS with no confidentiality 1 = Intel ME TLS with confidentiality

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

GNT[3:0]# functionality is not available on Mobile. Used as GPIO only.

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

R8361 change to 1K ohm follow DG1.0 and chklist 1.0 It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.

New Add in CPT EDS Rev1.0 at 0316 , Needs to be pulled High for Huron River platform.

Need check schematic

Quanta Computer Inc.
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	Panther Point 2/6	1A

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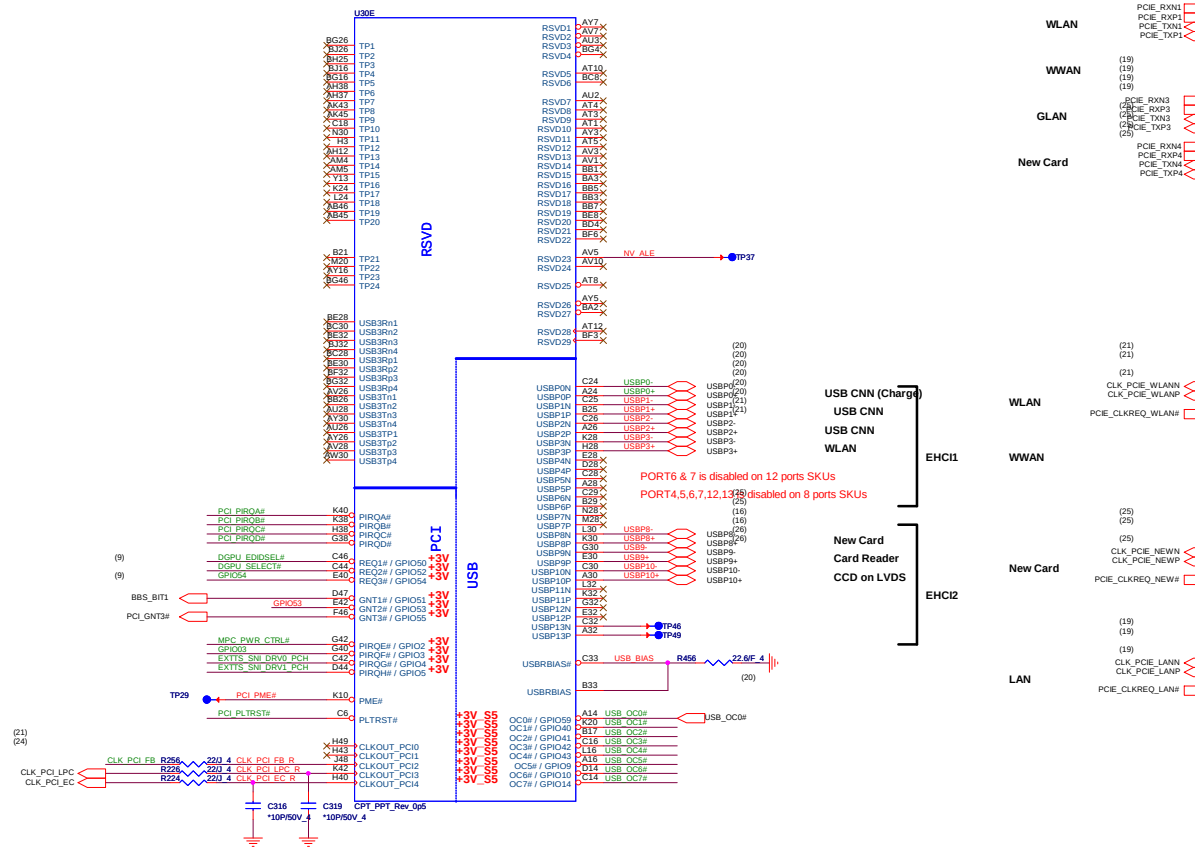
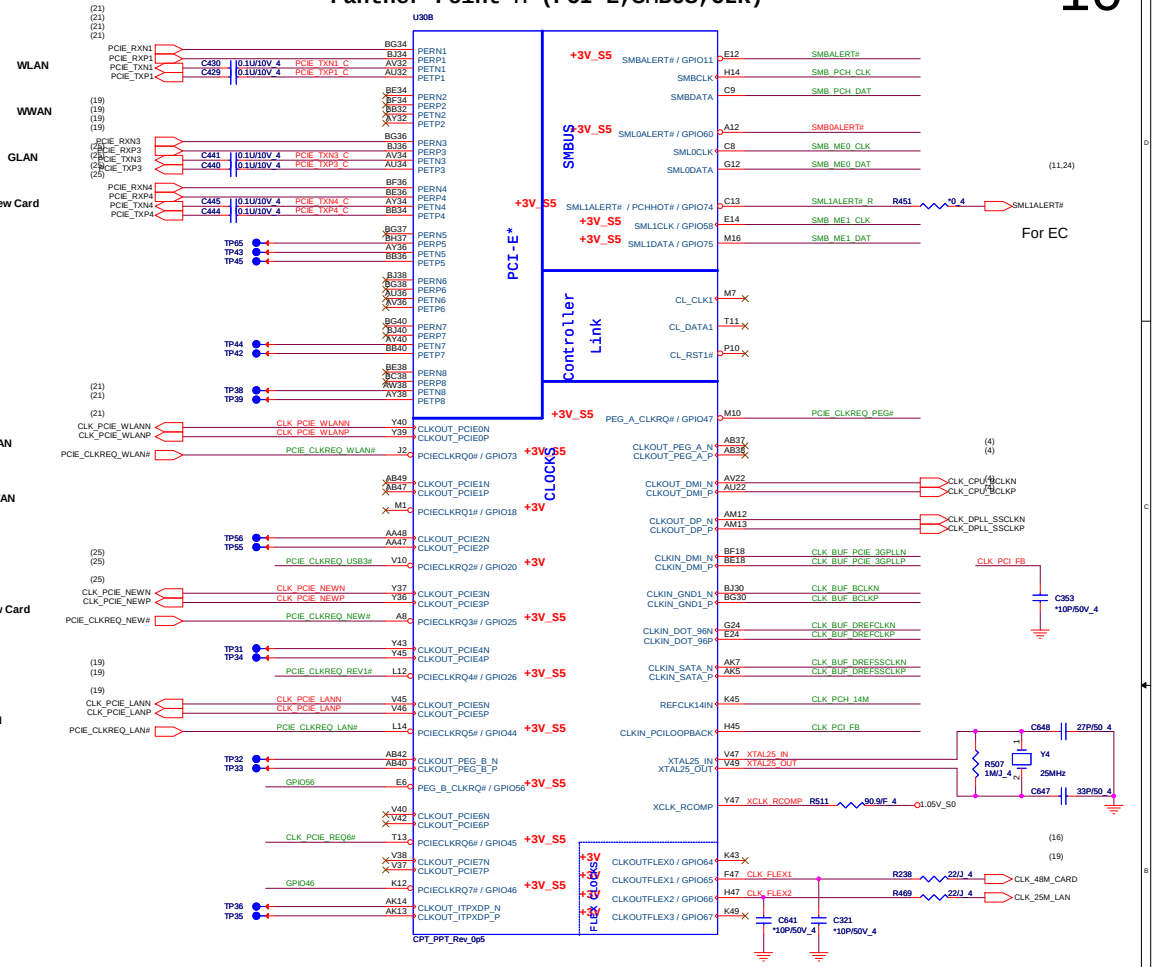
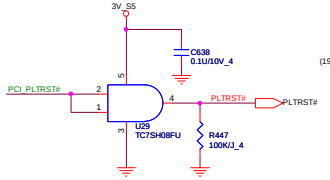
Panther Point-M (PCI,USB,NVRAM)



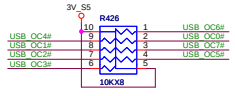
Panther Point-M (PCI-E,SMBUS,CLK)

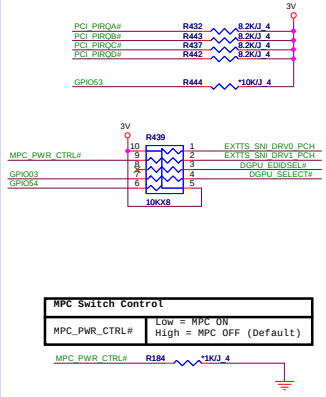


PLTRST#(CLG)

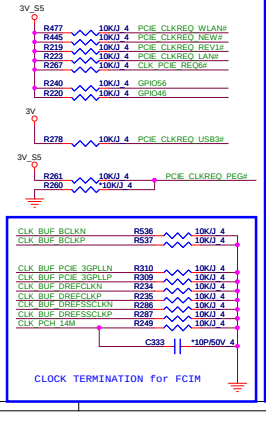


PCI/USBOC# Pull-up(CLG)

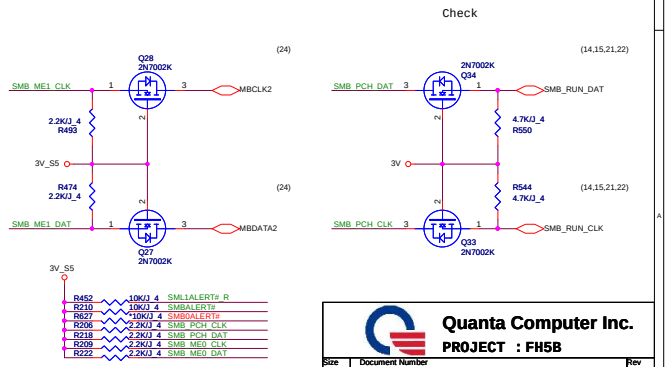




CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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Size	Document Number	Rev
	Panther Point 3/6	1A

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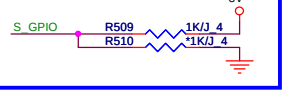
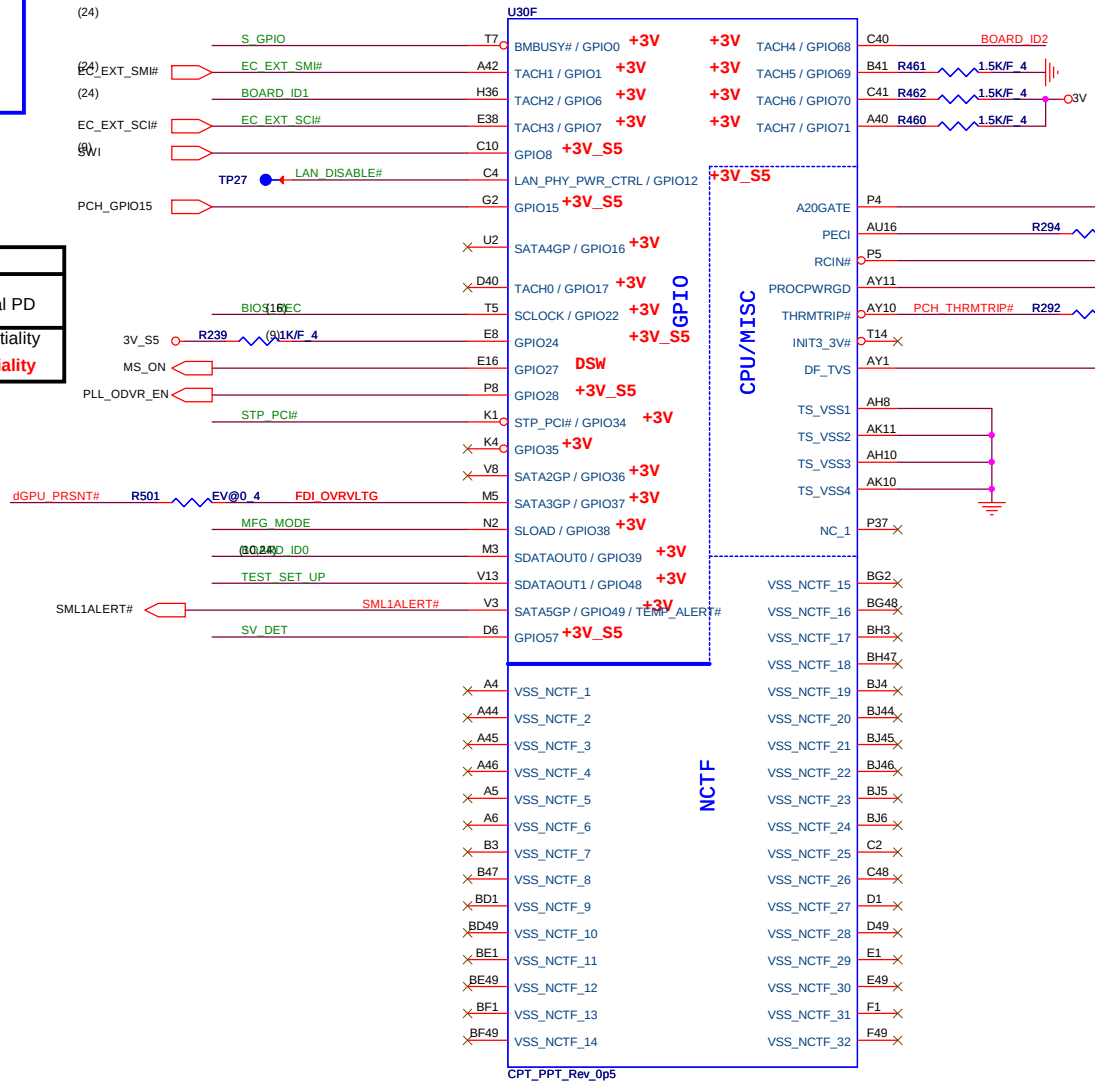
Panther Point (GPIO,VSS_NCTF,RSVD)

SGPIO



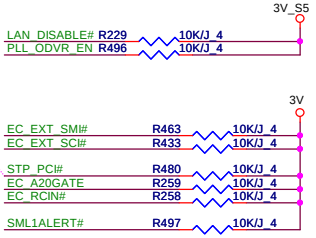
GPIO15

Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD
0 = Intel ME TLS with no confidentiality
1 = Intel ME TLS with confidentiality



Muxed with STP_PCI#
If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3S.

GPIO Pull-up/Pull-down(CLG)



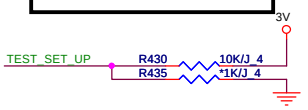
SATA[3:2]GP/GPIO[37:36] internal Pull-down 20K
SATA2GP/GPIO36 (FDI_OVRVLTG) & SATA3GP/GPIO37 (DMI_OVRVLTG)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY	High = Disable (Default) Low = Enable

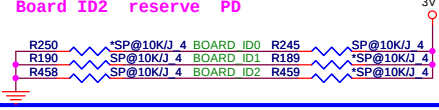
SV_SET_UP
High = Strong (Default)



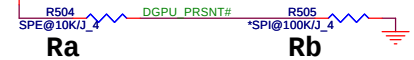
MFG-TEST

[ID0:D1]	0:0	0:1	1:0	1:1
Fuction	UMA	Optimus (Hynix)	Optimus (Samsung)	Rev.

Board ID2 reserve PD



	EV	UMA
Stuff	Ra	Rb



Ra **Rb**

Quanta Computer Inc.
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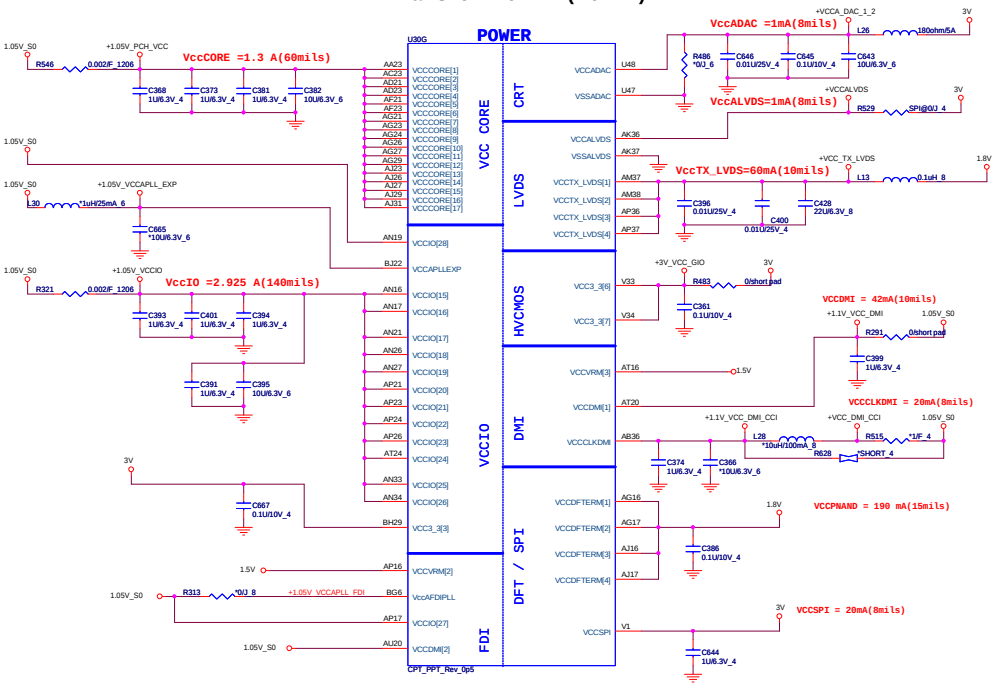
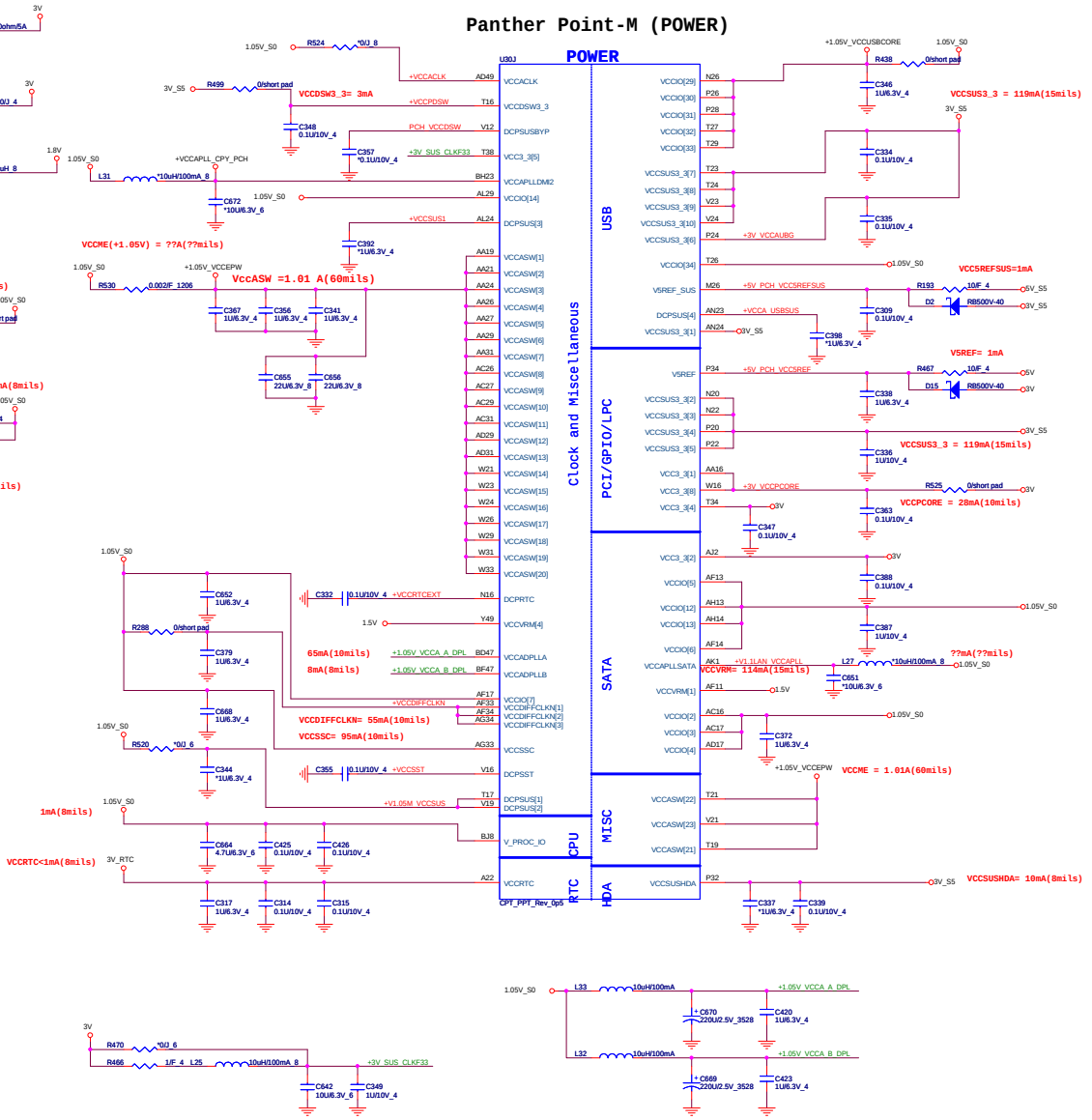
PCH5(CLG)

Panther POINT (POWER)



Panther Point-M (POWER)



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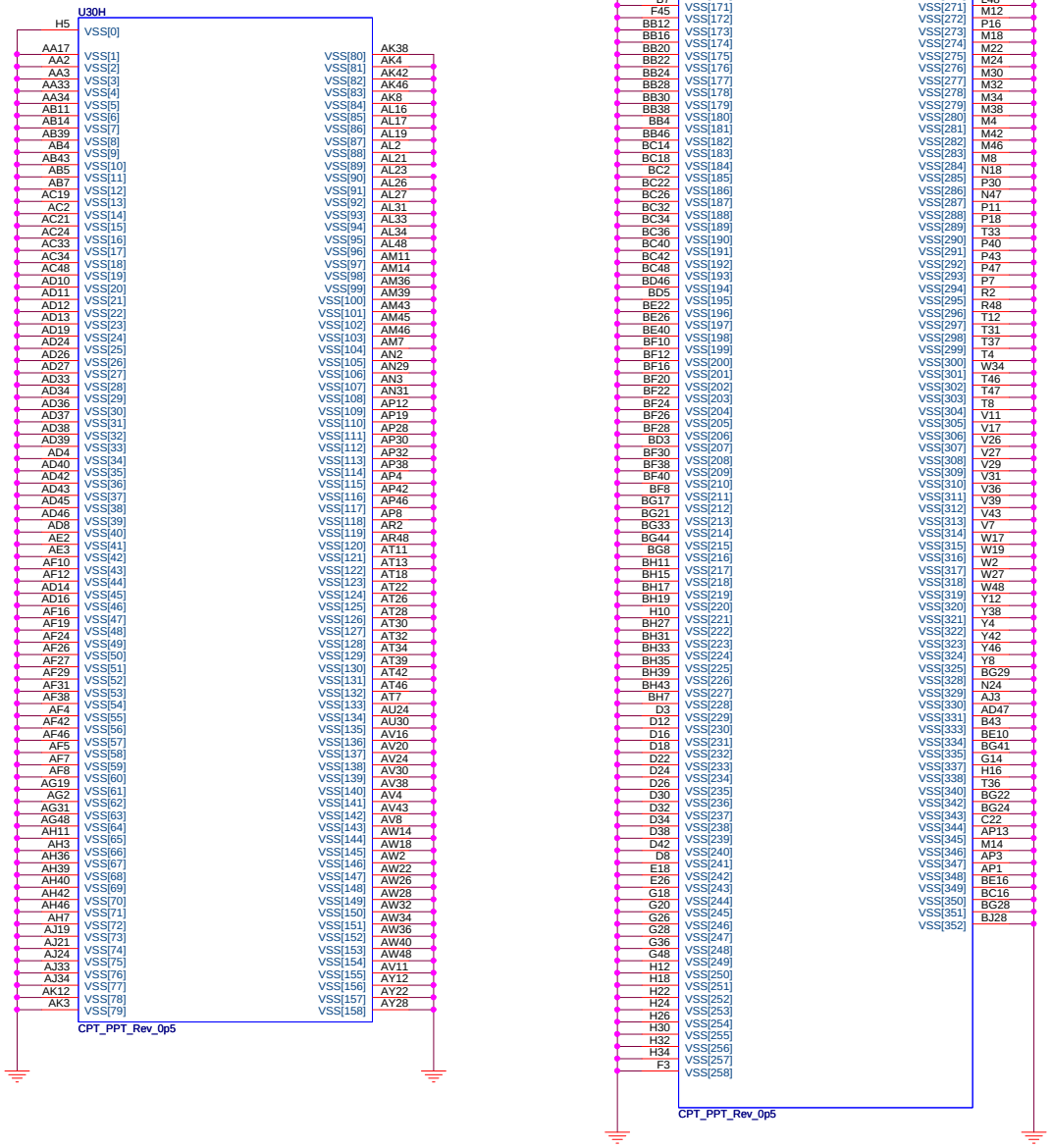
IBEX PEAK-M (GND)



Quanta Computer Inc.

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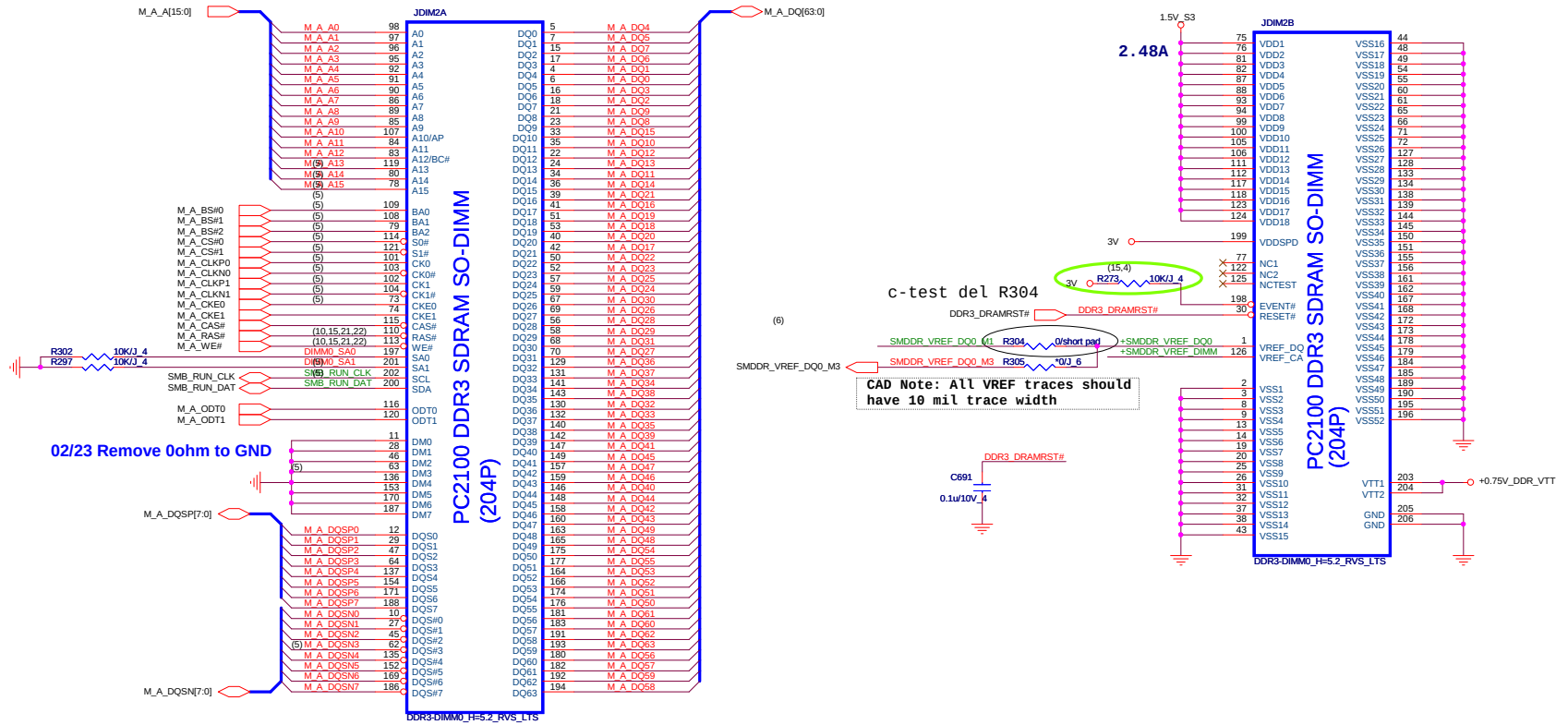
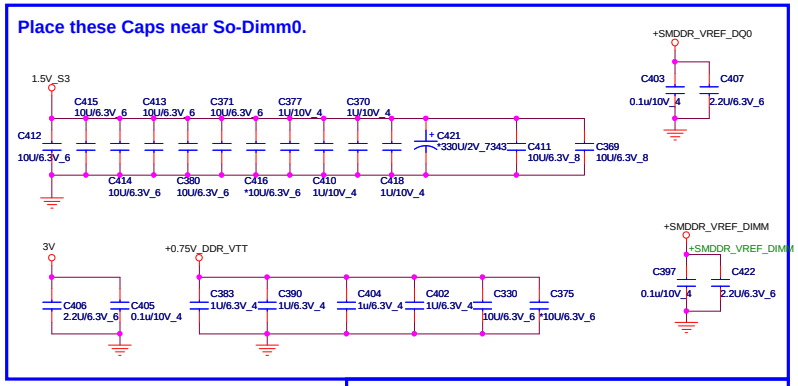
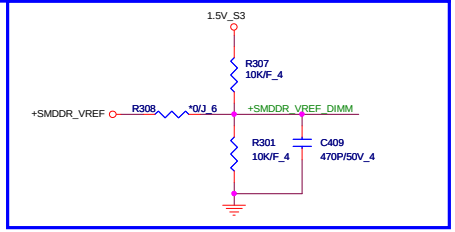
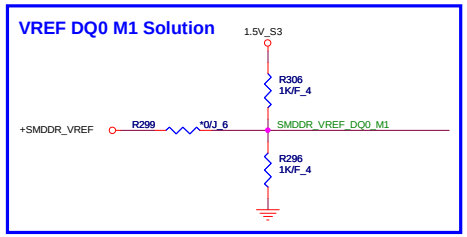
DDR_STD(DDR)









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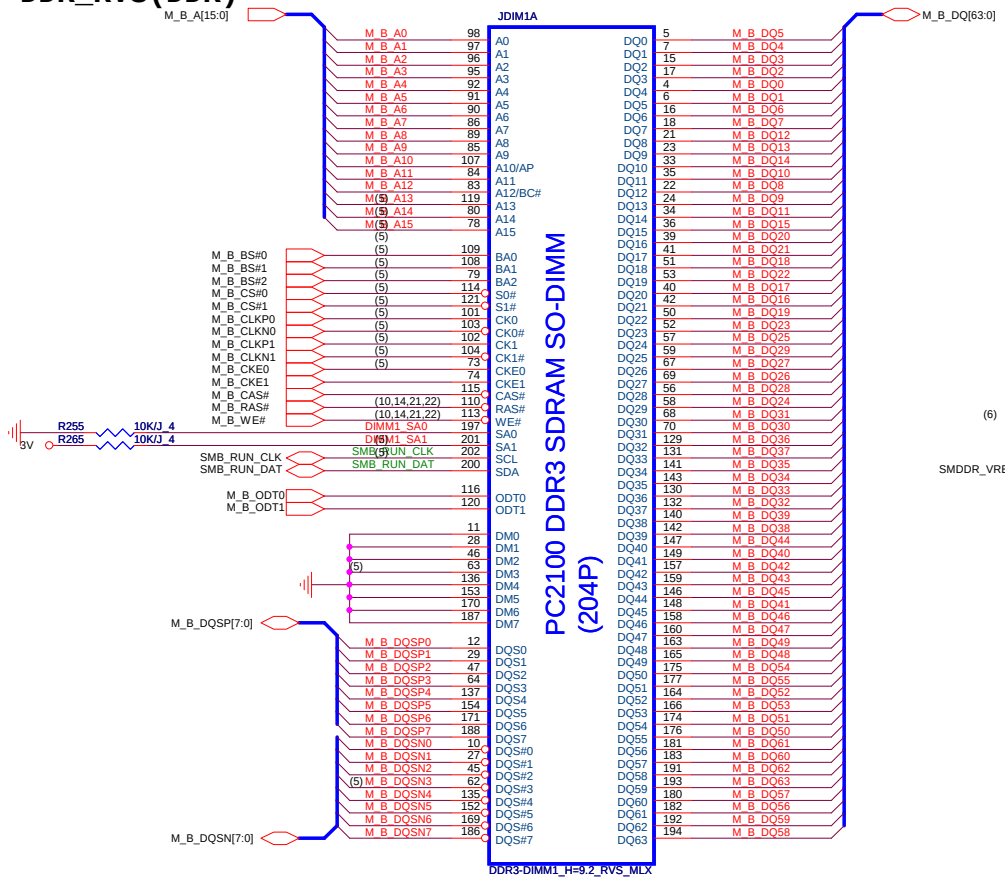
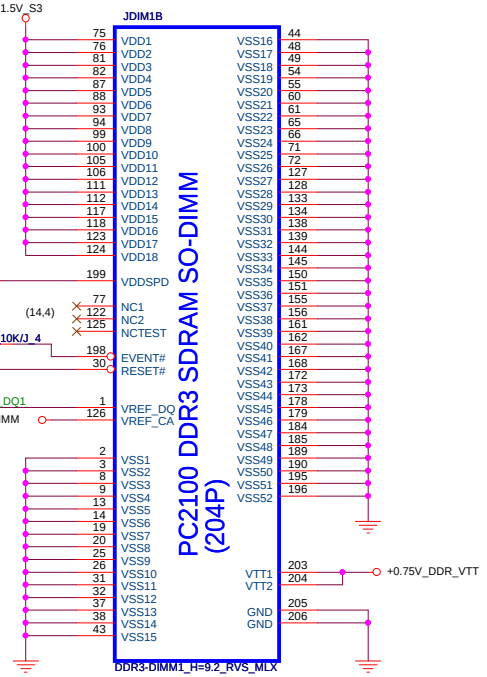
DDR_RVS(DDR)





c-test del R268

R254 10K/J_4

DDR3_DRAMRST#

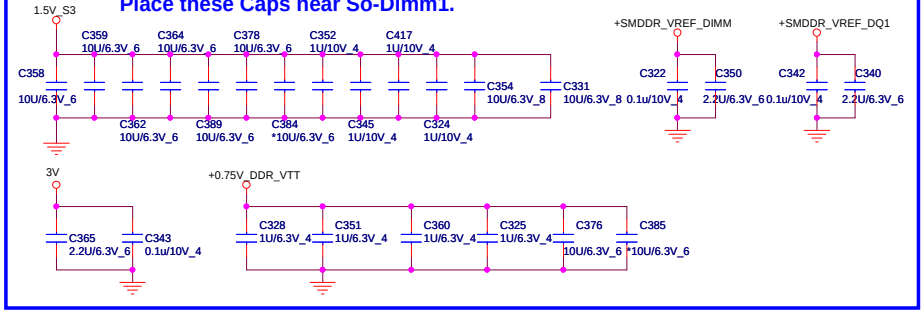
SMDDR_VREF_DQ1_M1 R268 0/short pad +SMDDR_VREF_DQ1

SMDDR_VREF_DQ1_M3 R257 *0/J_6 +SMDDR_VREF_DIMM

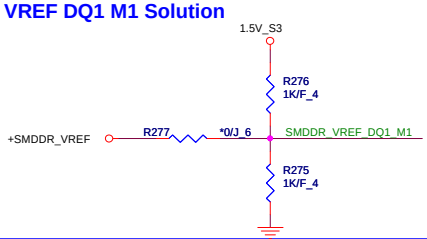
SMDDR_VREF_DQ1_M3

CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

Quanta Computer Inc.

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	DDRIII SO-DIMM-1	1A
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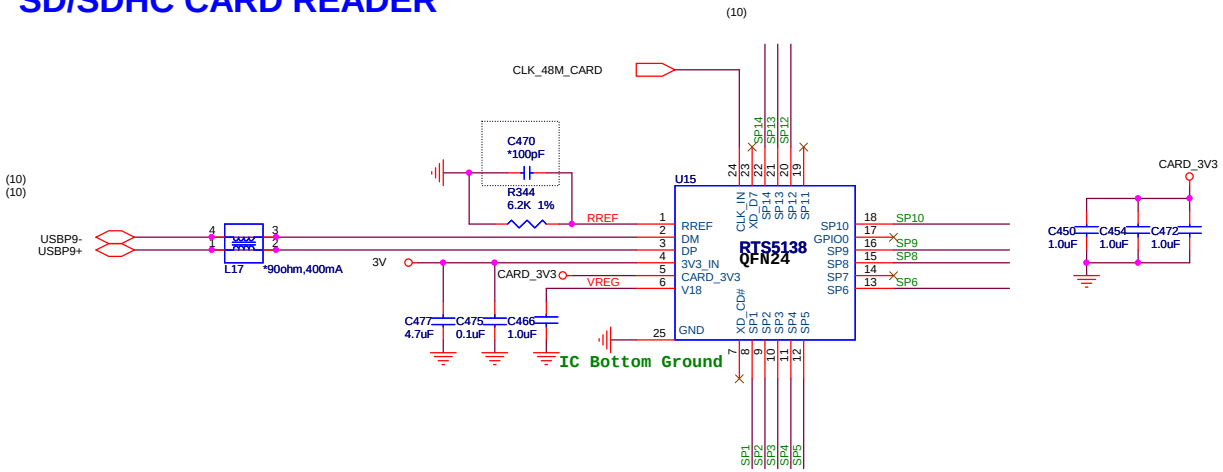
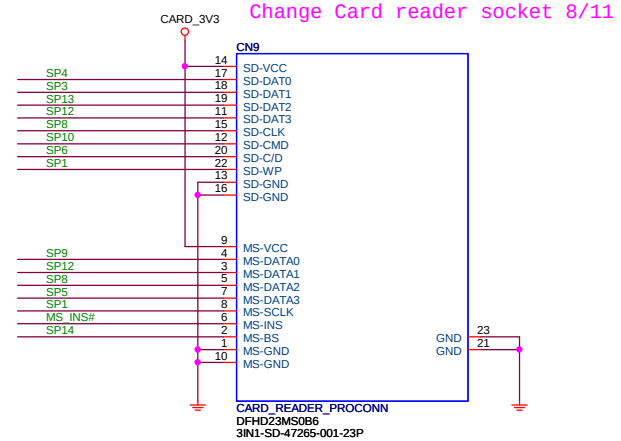
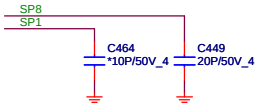
RST5138 SIDO

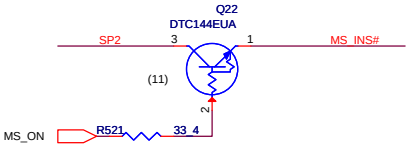
SD/SDHC CARD READER



SD/MS CONNDETOR







Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	

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	Card Reader RST5138	1A
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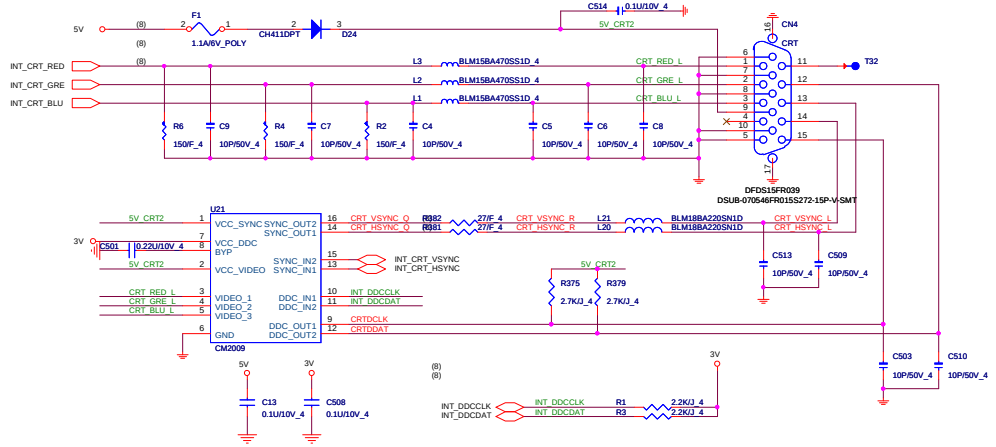
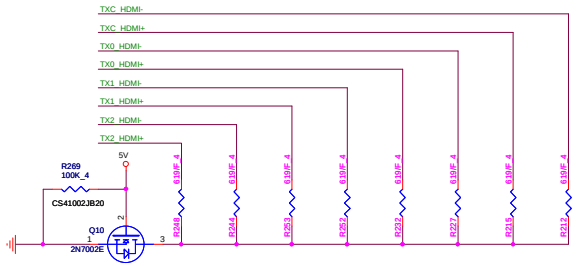
CRT CONN/DDC LEVEL SHIFT

40mils

TBD CN5500 FOOTPRINT



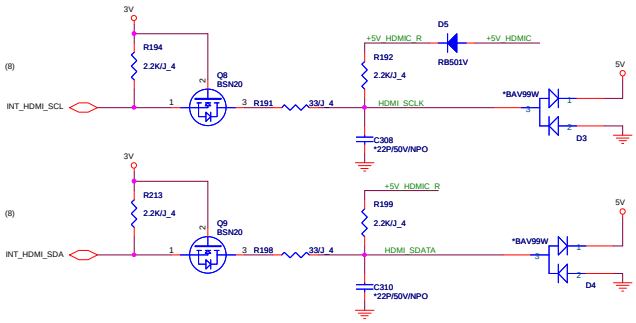


PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

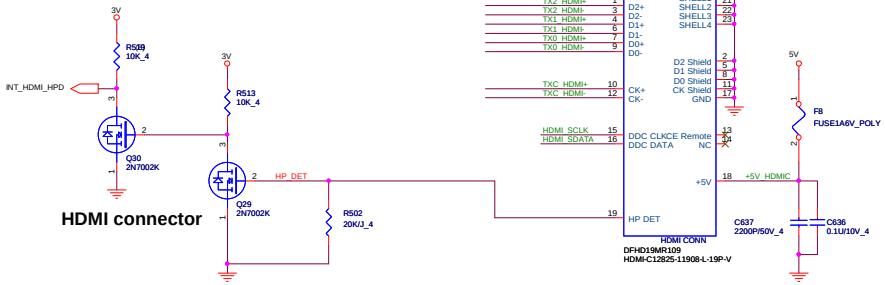
INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR

INT_HDMI_TXCN	INT_HDMI_TXCN	C311	0.1U/10V_4	TXC_HDMI-
INT_HDMI_TXCP	INT_HDMI_TXCP	C312	0.1U/10V_4	TXC_HDMI+
INT_HDMI_TXDN0	INT_HDMI_TXDN0	C327	0.1U/10V_4	TX0_HDMI-
INT_HDMI_TXDP0	INT_HDMI_TXDP0	C329	0.1U/10V_4	TX0_HDMI+
INT_HDMI_TXDN1	INT_HDMI_TXDN1	C313	0.1U/10V_4	TX1_HDMI-
INT_HDMI_TXDP1	INT_HDMI_TXDP1	C318	0.1U/10V_4	TX1_HDMI+
INT_HDMI_TXDN2	INT_HDMI_TXDN2	C320	0.1U/10V_4	TX2_HDMI-
INT_HDMI_TXDP2	INT_HDMI_TXDP2	C323	0.1U/10V_4	TX2_HDMI+



HDMI CONN



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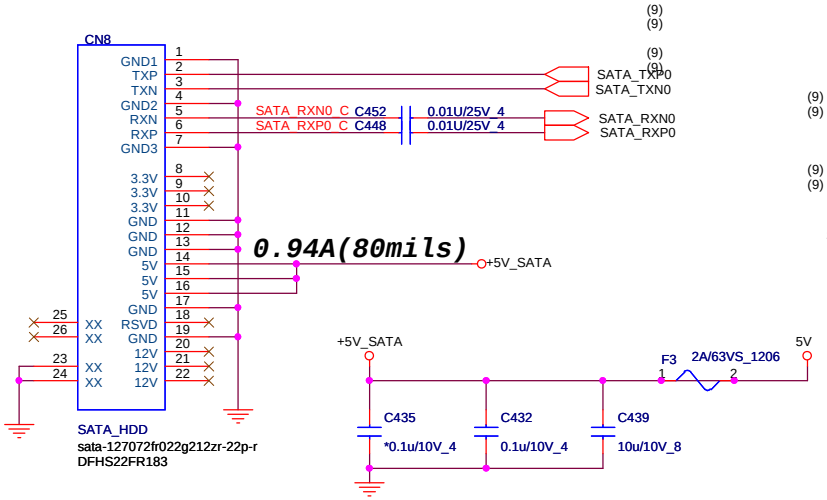
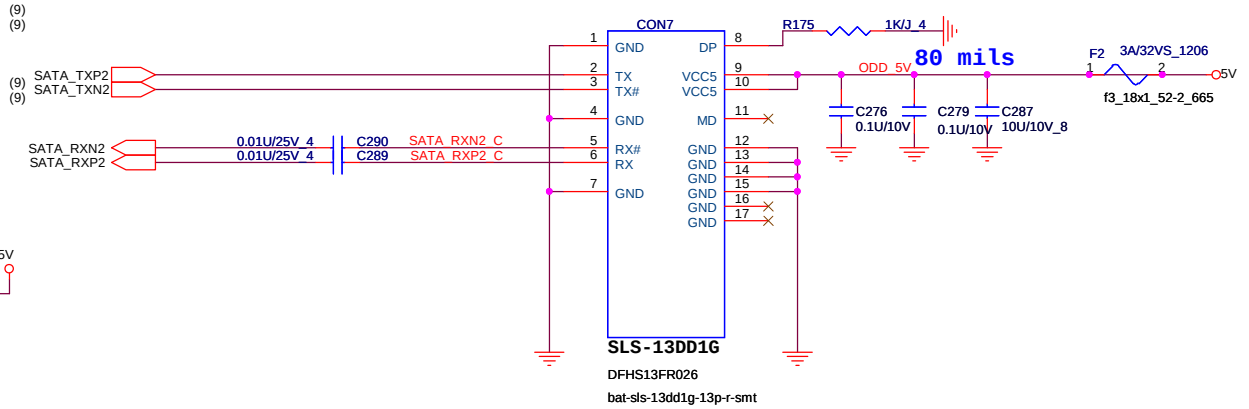
2.5" SATA HDD



SATA ODD

ODD CONN



H6 FH1 H-TC100BC256D59P2
H23 FH1 H-BC197D142PB
H20 FH1 H-BC197D142PB
H11 FH1 H-BC217I95D55PB
H14 FH1 H-BC217I95D55PB
H16 FH1 H-TC217BC248D142P2
H7 FH1 H-TC217BC248D142P2
H9 FH1 H-TC217BC248D142P2
H12 *FH1 H-C217D118P2
H8 *FH1 H-C315D126P2
H18 *FH1 H-C315D126P2

H27 *FH1 H-C98D98N
H3 *FH1 H-C98D98N
H13 *FH1 H-MS15-1

H24 *HG-C295D126P2
H26 *HG-FH5-MB-1-D126P2
H19 *HG-C315D126P2
H1 *HG-C315D126P2
H21 *HG-C236D126P2
H2 *HG-C315D126P2

CPU Socket
H17

H5 *HG-MS15-3
H10 *HG-MS15-2
H22 *HG-TC315BC350D126P2
H28 *HG-C315D126P2
H25 *HG-C315D126P2
H4 *HG-C315D126P2
H15 *HG-MS15-3

H31 *FH1 spad-c177
H32 *FH1 spad-c177
H33 *FH1 spad-c177
H34 *FH1 spad-c177

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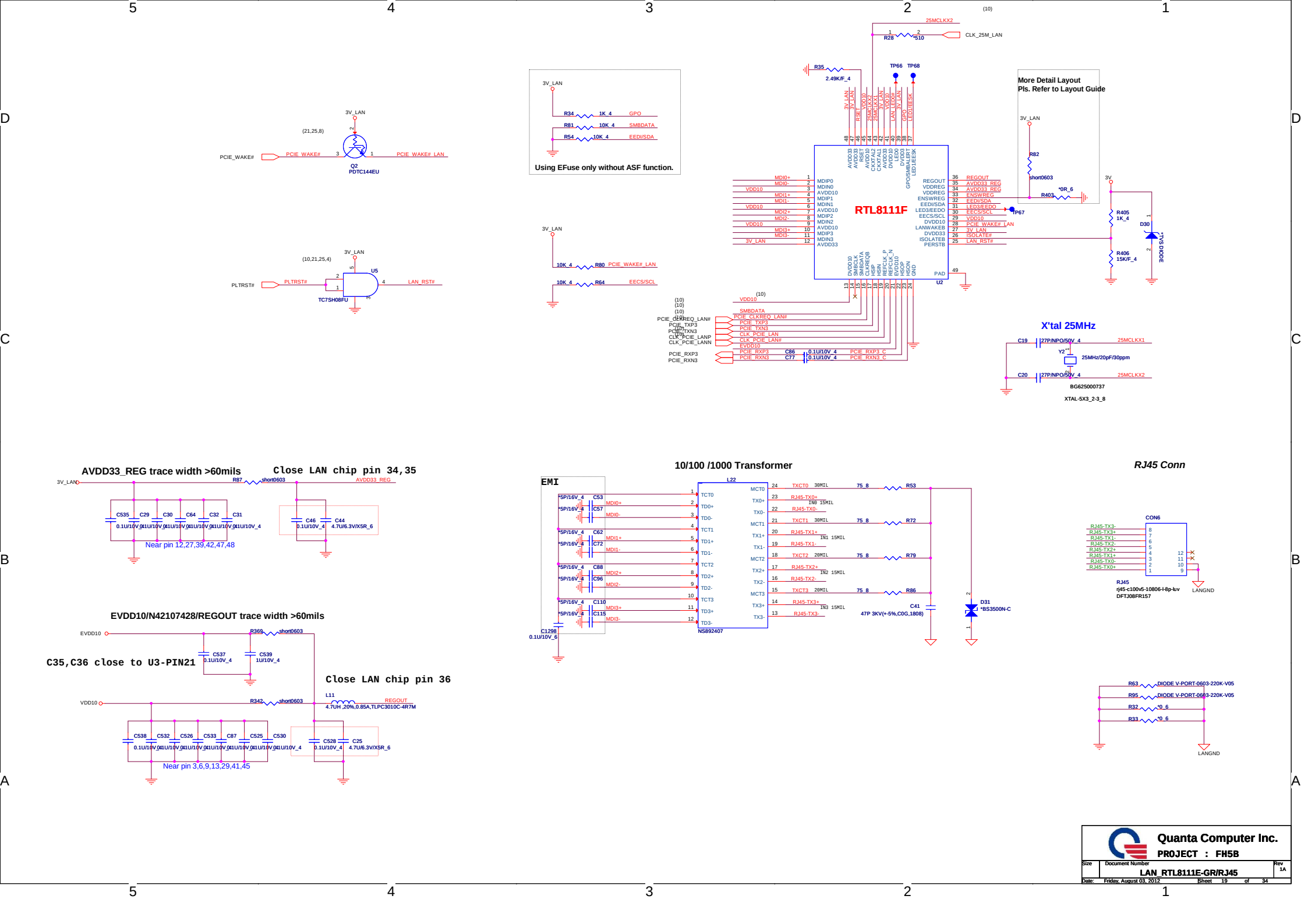

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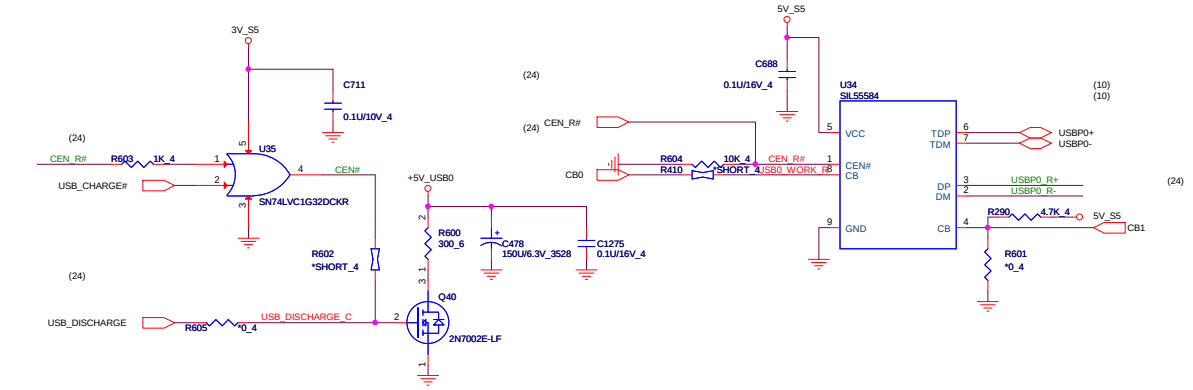
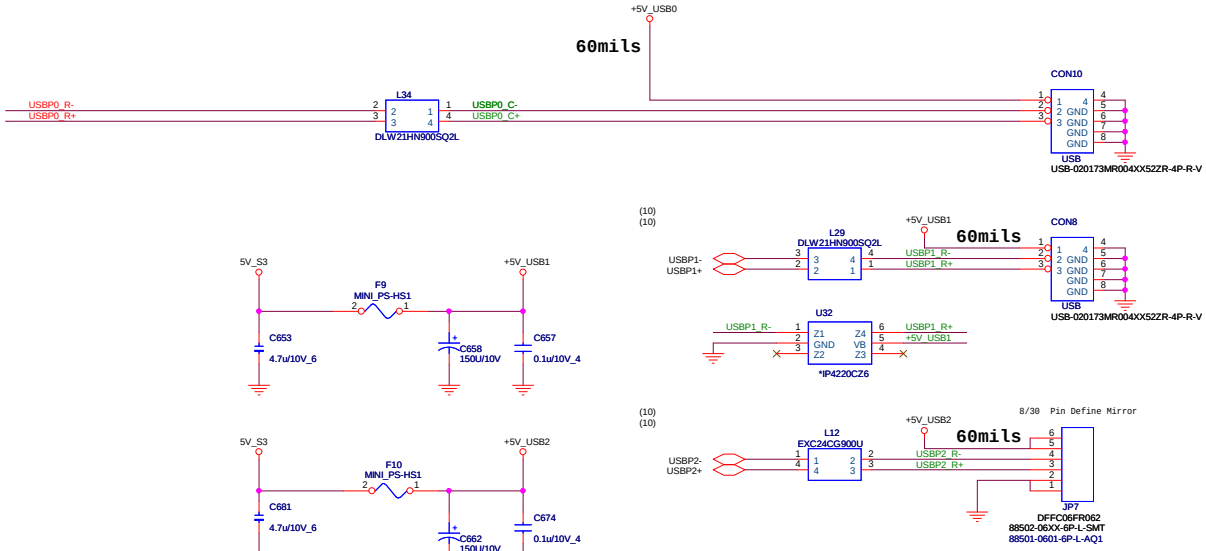
S5 Charge



CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP



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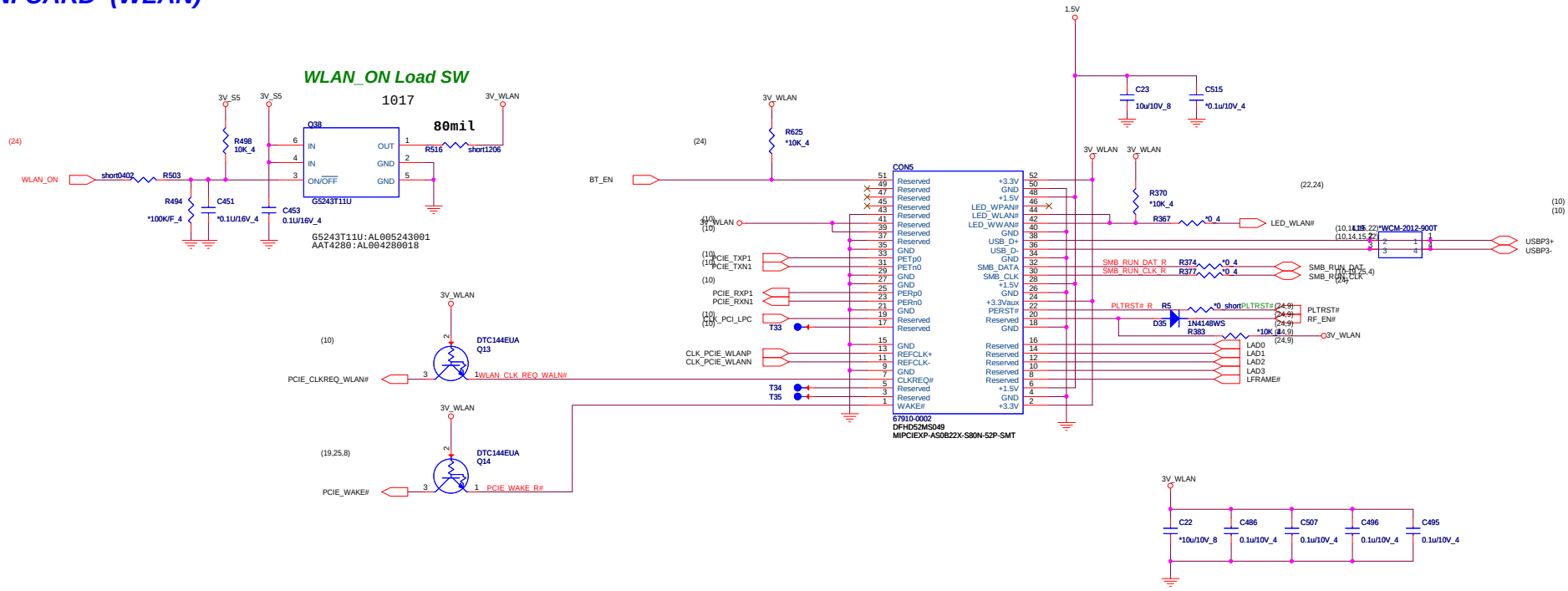
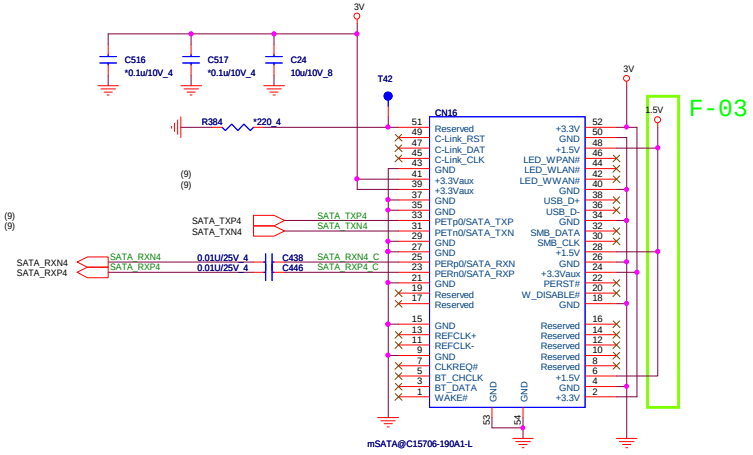
MINI CARD (WLAN)



mSATA reserved



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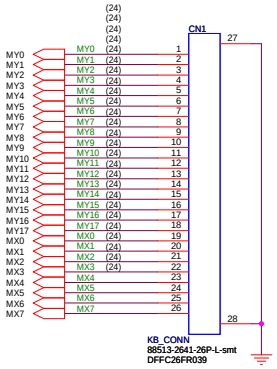
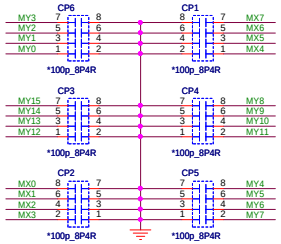
Keyboard(KBC)

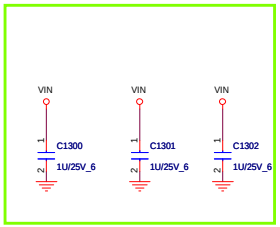


For EMI Reserve Caps for debug



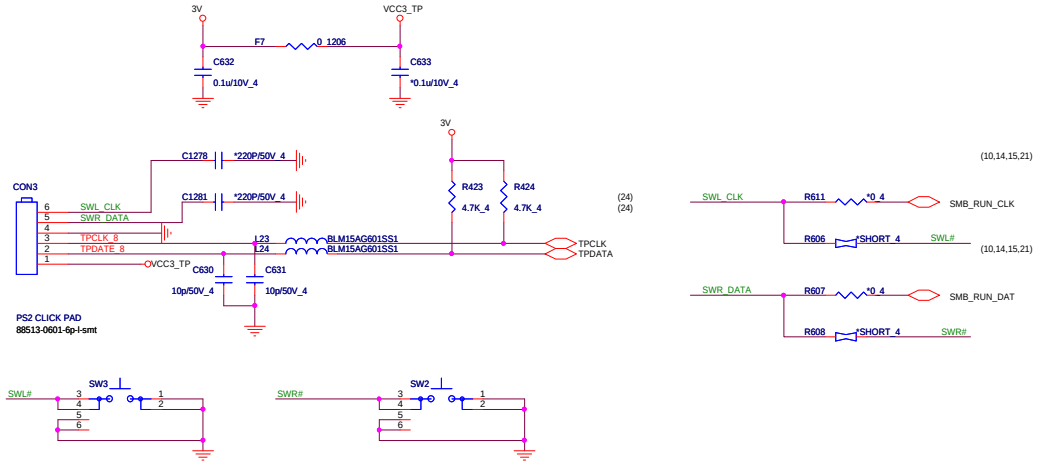
Decaupling Cap

F-02

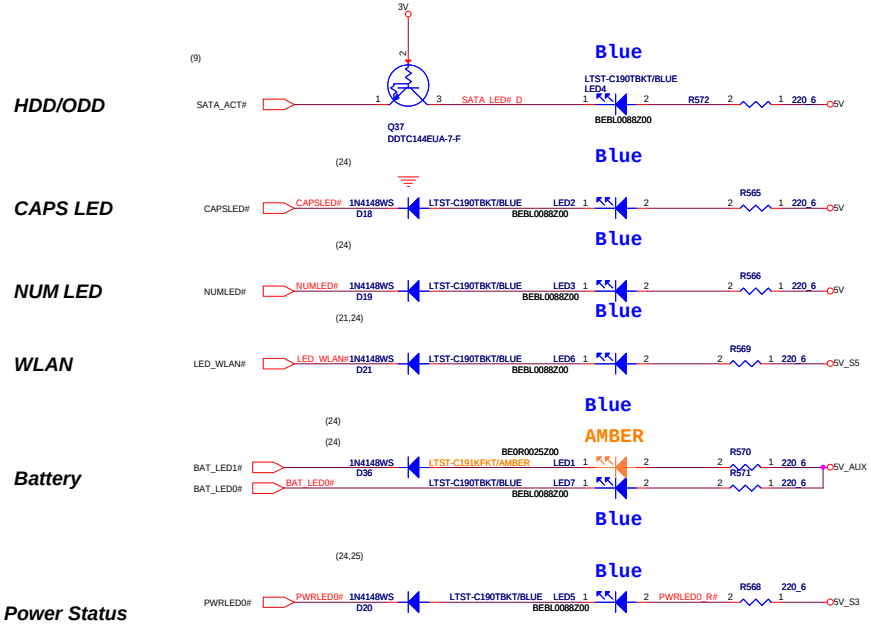


Touch Pad

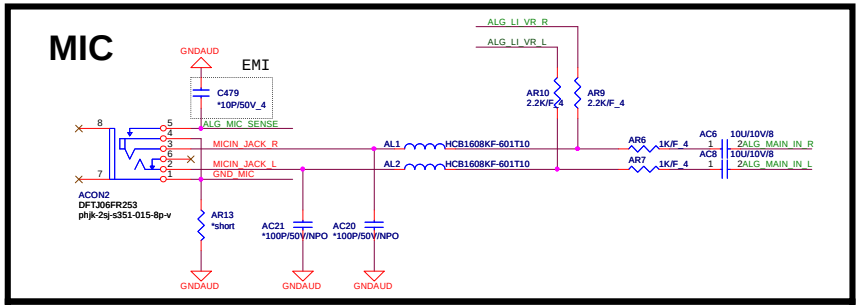
SMBUS CLICK PAD reserve

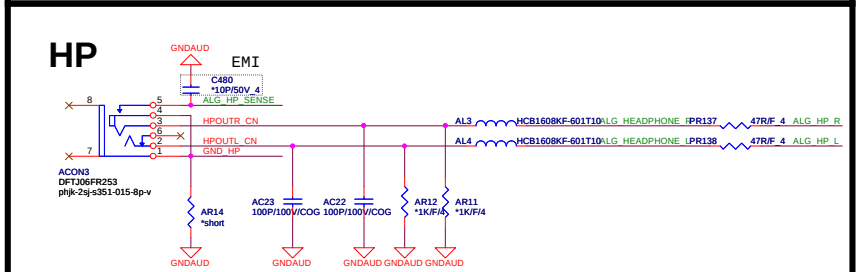


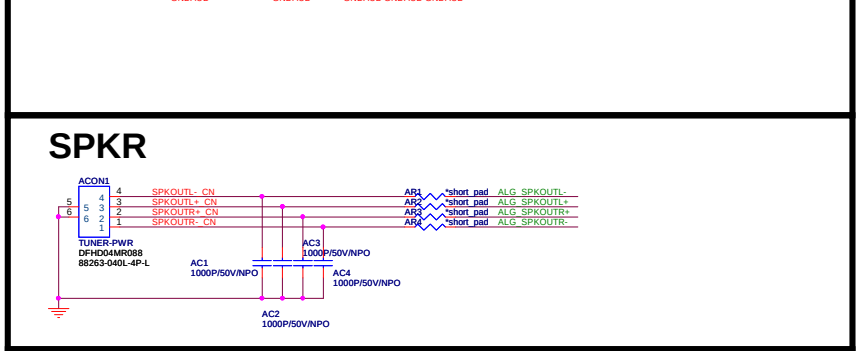
LED

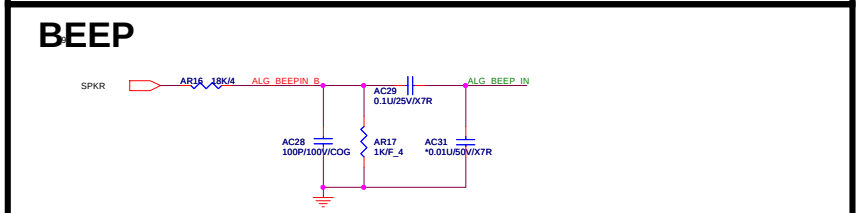


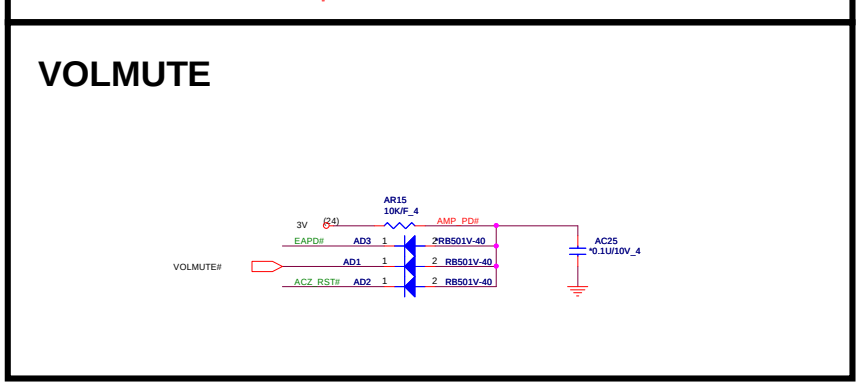
Codec ALC269-VC

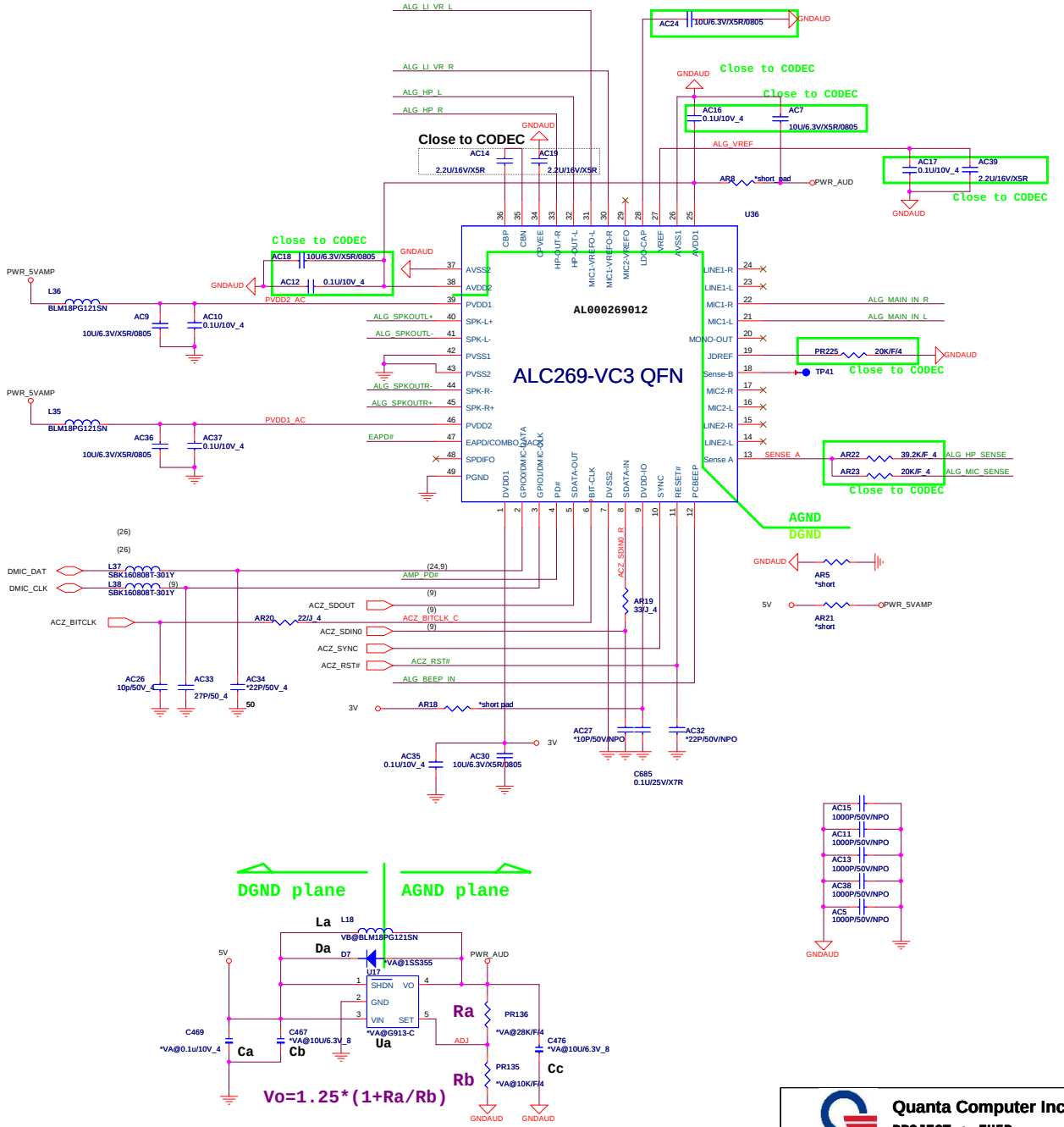




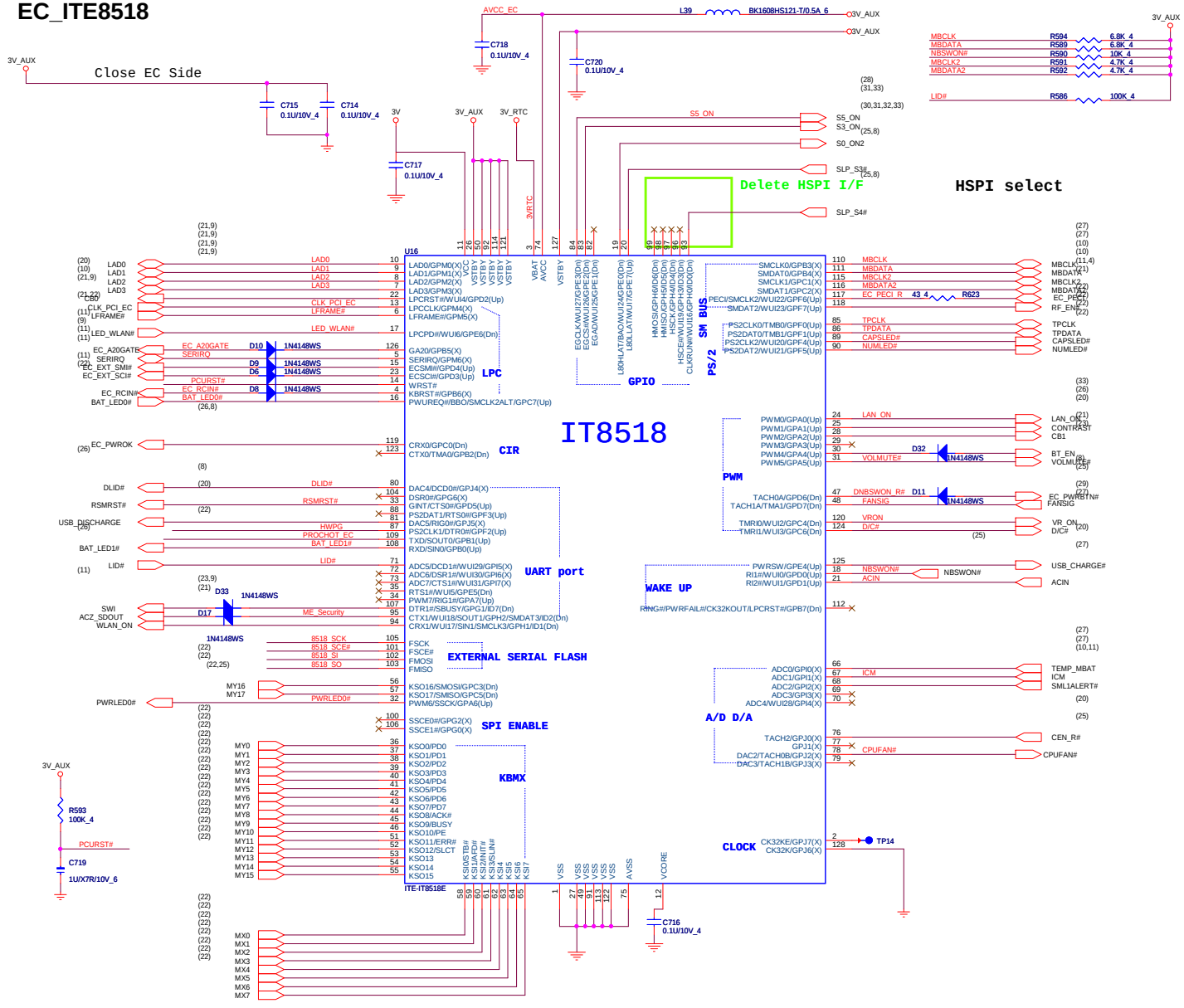


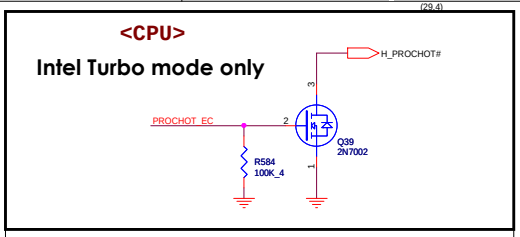


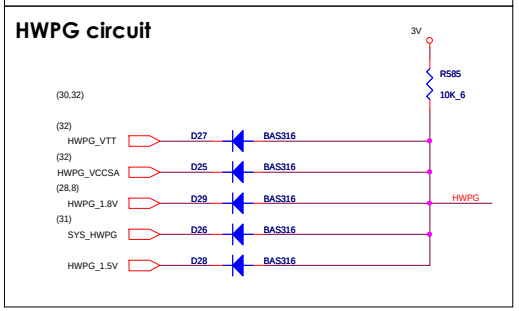


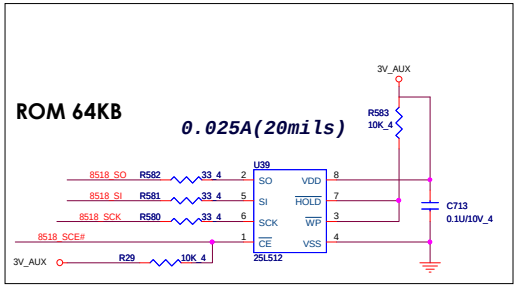


EC_ITE8518









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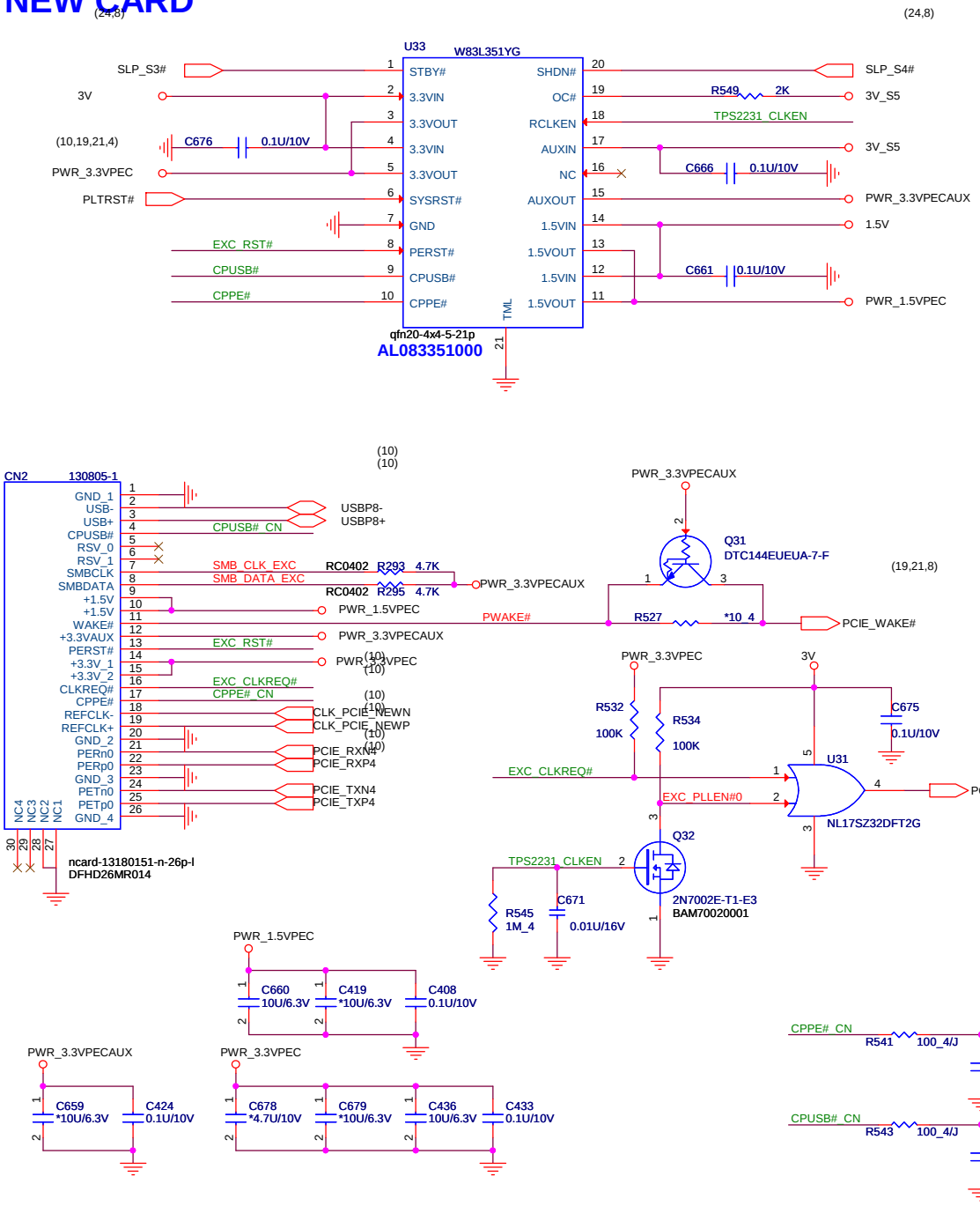
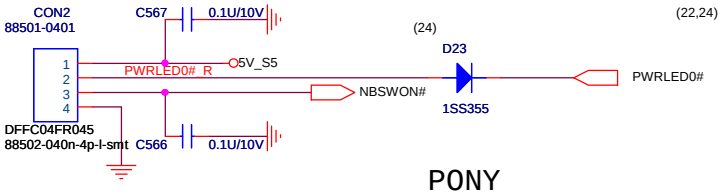
NEW CARD



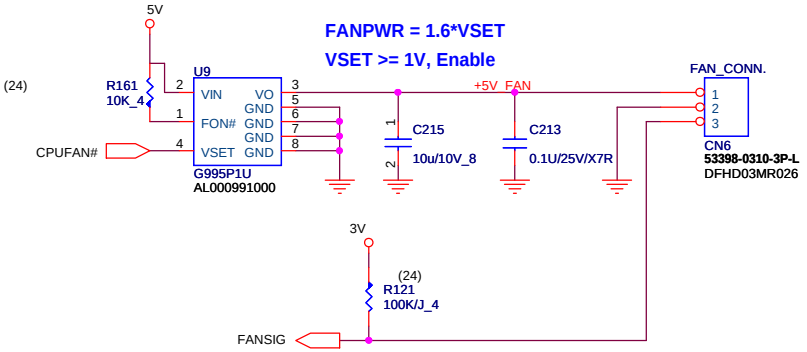
PW BOARD CON



c-test change to +5V_S5

PONY
add D23

CPU FAN CTRL



Quanta Computer Inc.		
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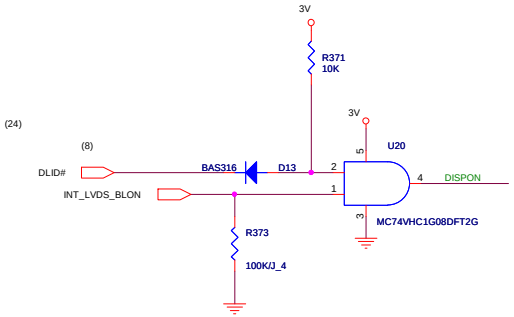
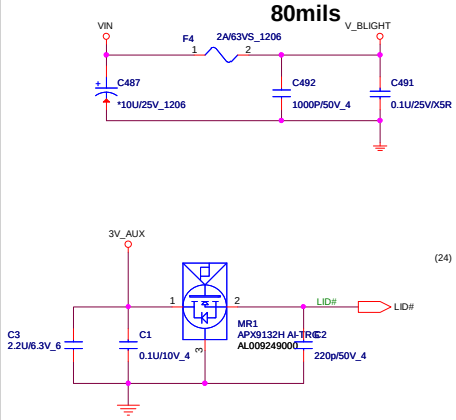
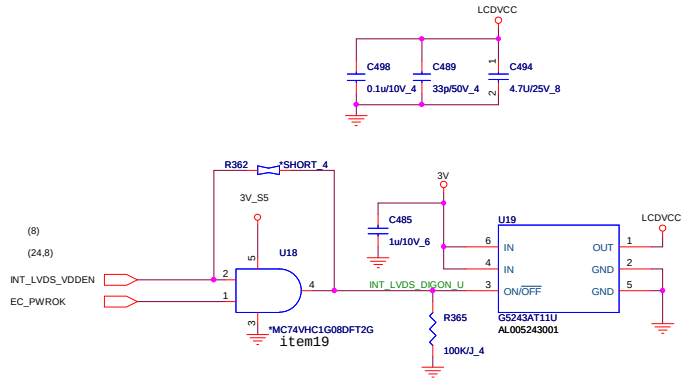
BACKLIGHT Control(LVDS)



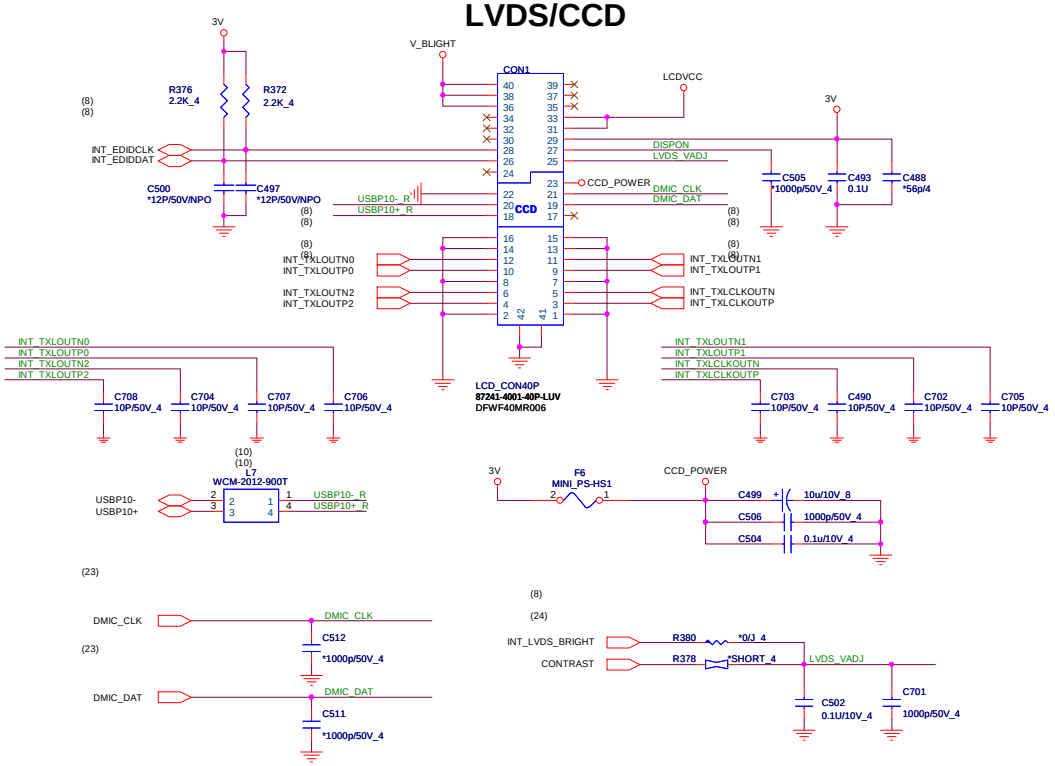
BACKLIGHT POWER



LED Panel POWER SWITCH(LVDS)



LVDS/CCD



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Size	Document Number	Rev
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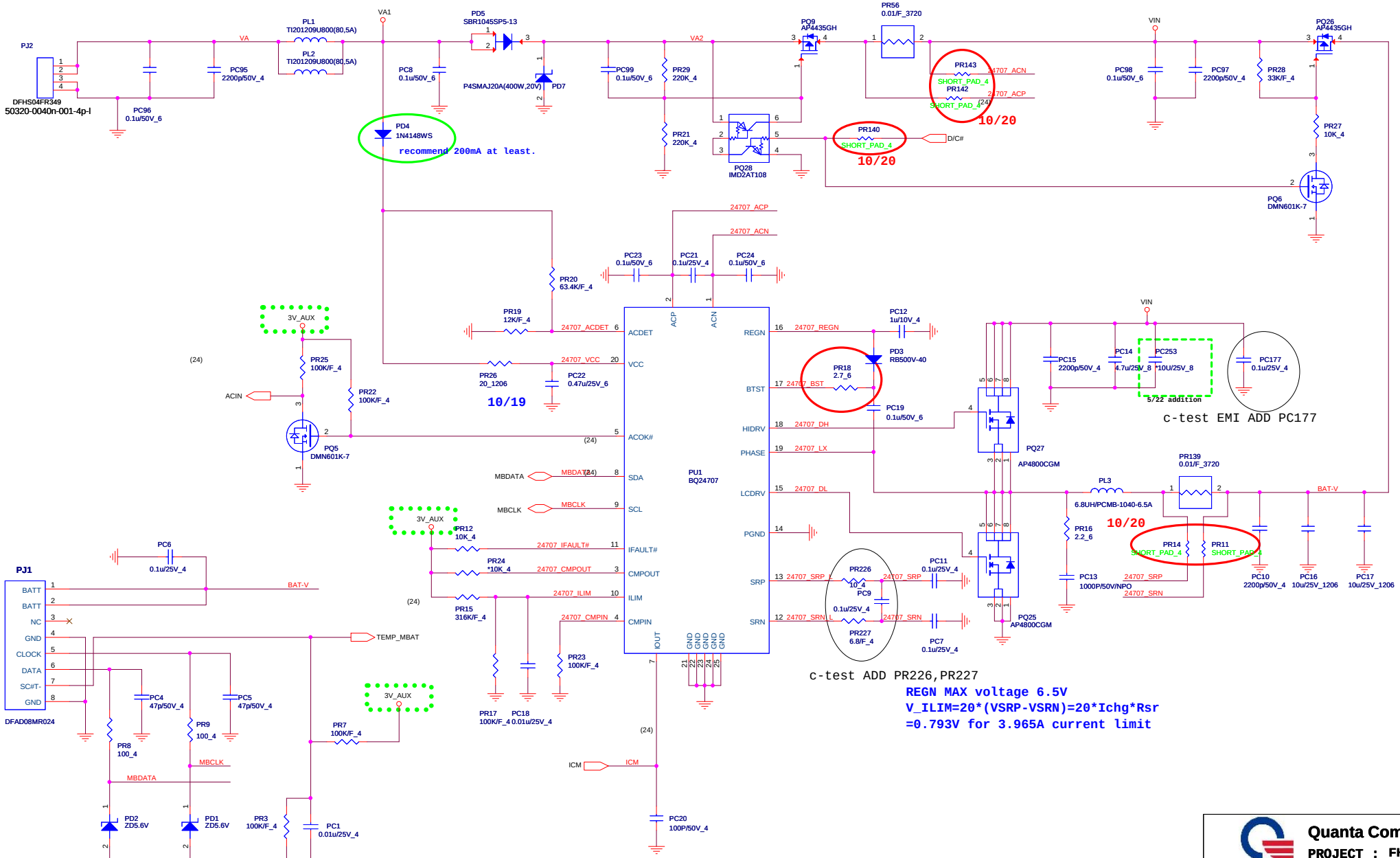

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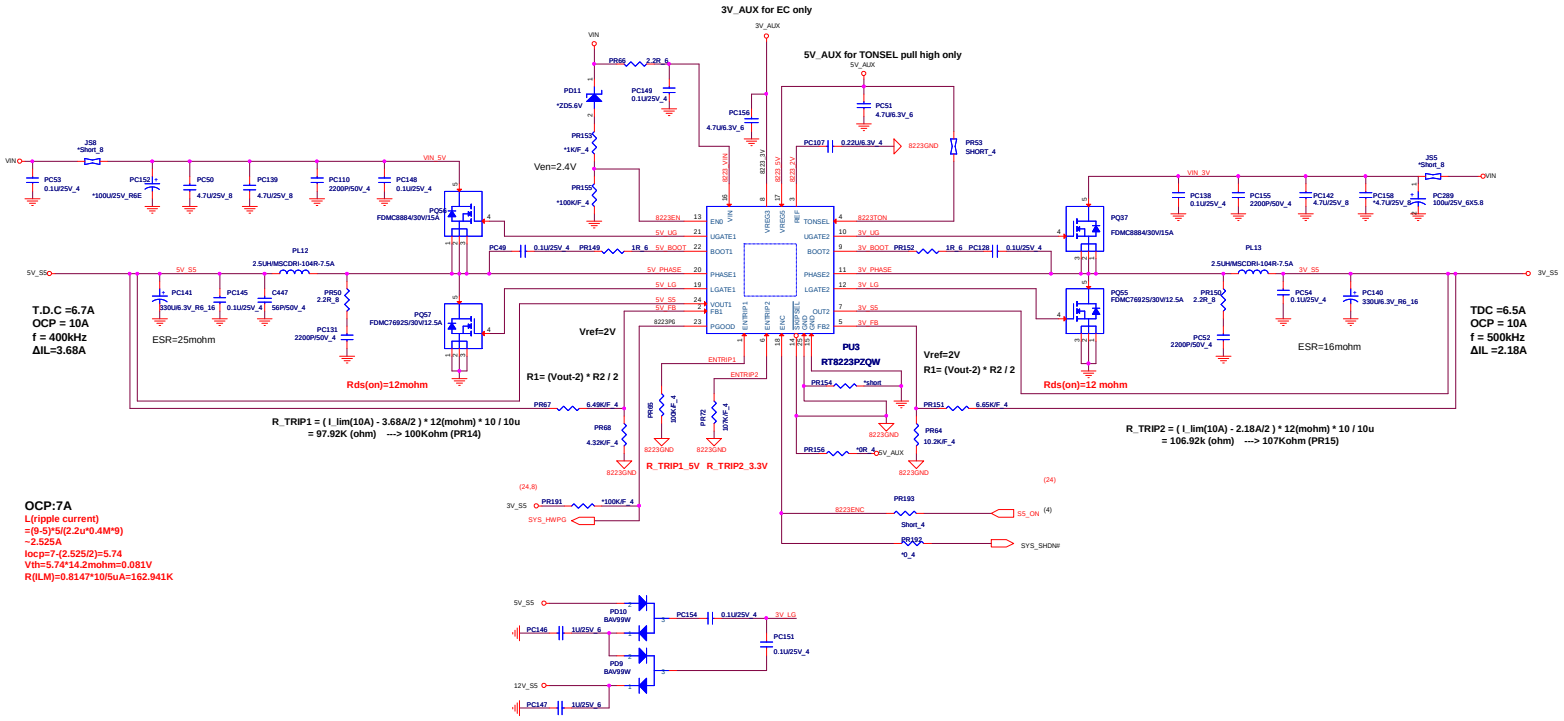
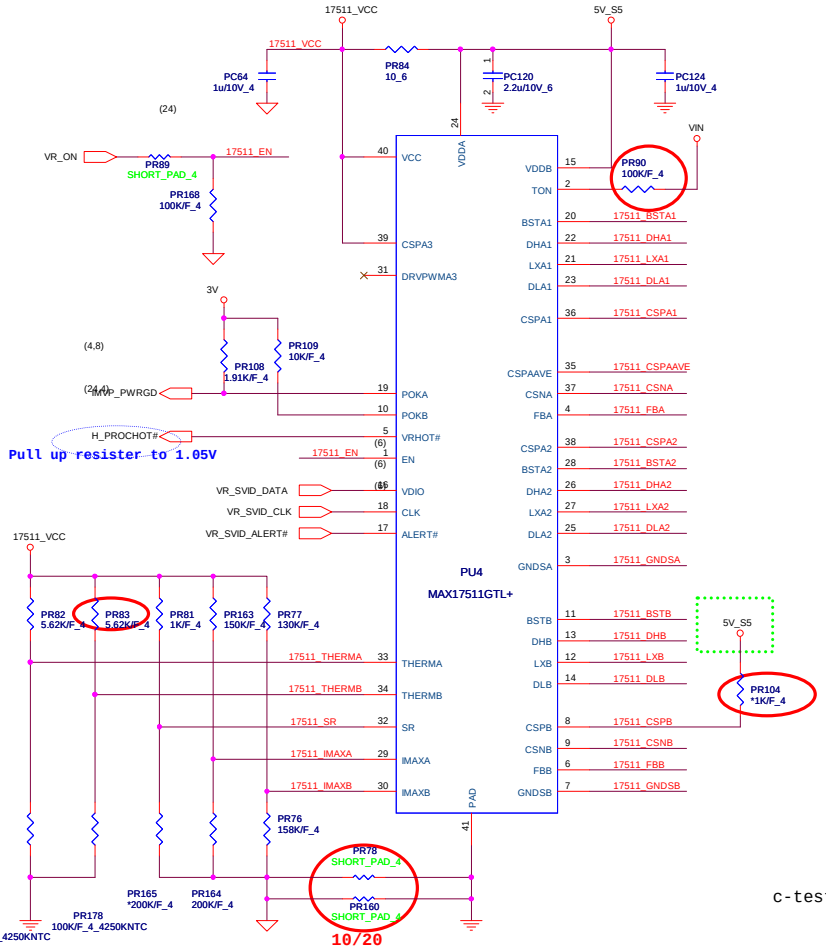
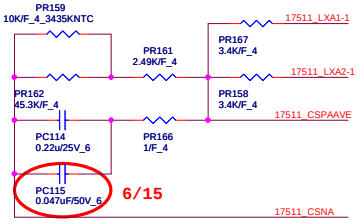
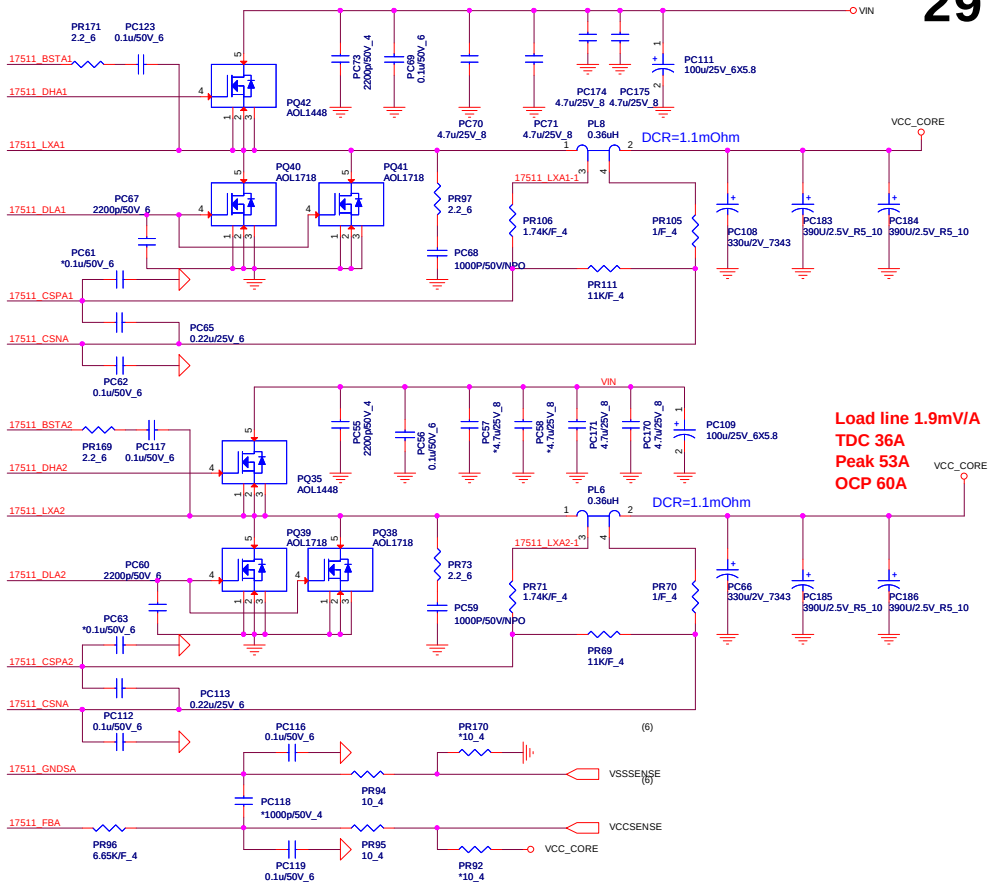
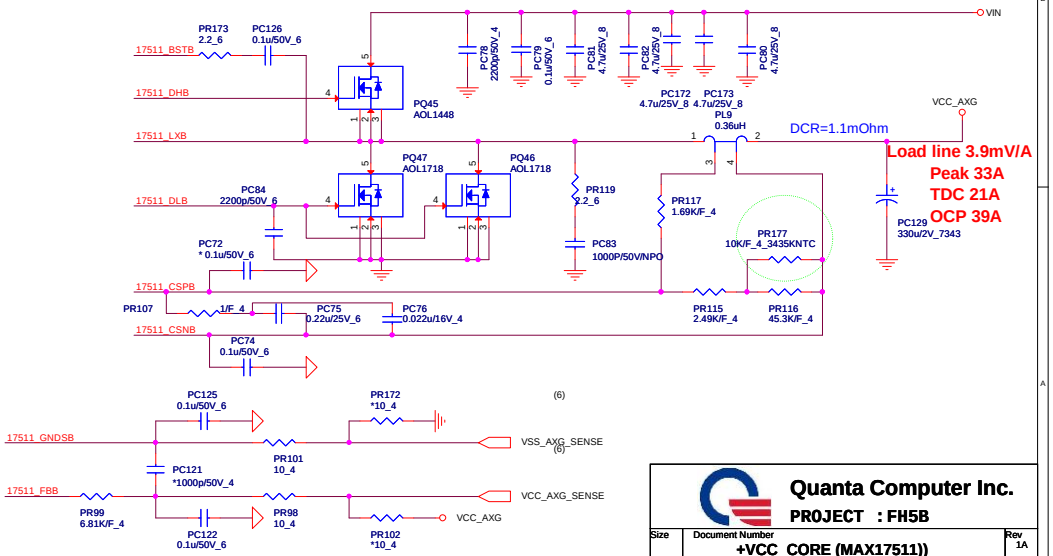

3V_AUX for EC only
5V_AUX for TONSEL pull high only
Ven=2.4V
Vref=2V
R1= (Vout-2) * R2 / 2
PU3
RT8223PZQW
T.D.C =6.7A
OCP = 10A
f = 400kHz
ΔIL=3.68A
ESR=25mohm
Rds(on)=12mohm
R_TRIP1 = (I_lim(10A) - 3.68A/2) * 12(mohm) * 10 / 10u
= 97.92K (ohm) ---> 100Kohm (PR14)
TDC =6.5A
OCP = 10A
f = 500kHz
ΔIL =2.18A
ESR=16mohm
Rds(on)=12 mohm
R_TRIP2 = (I_lim(10A) - 2.18A/2) * 12(mohm) * 10 / 10u
= 106.92k (ohm) ---> 107Kohm (PR15)
R_TRIP1_5V R_TRIP2_3.3V
OCP:7A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=7-(2.525/2)=5.74
Vth=5.74*14.2mohm=0.081V
R(ILM)=0.8147*10/5uA=162.941K







c-test ADD PC172,PC173,PC174,PC175



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	+VCC_CORE (MAX17511))	1A

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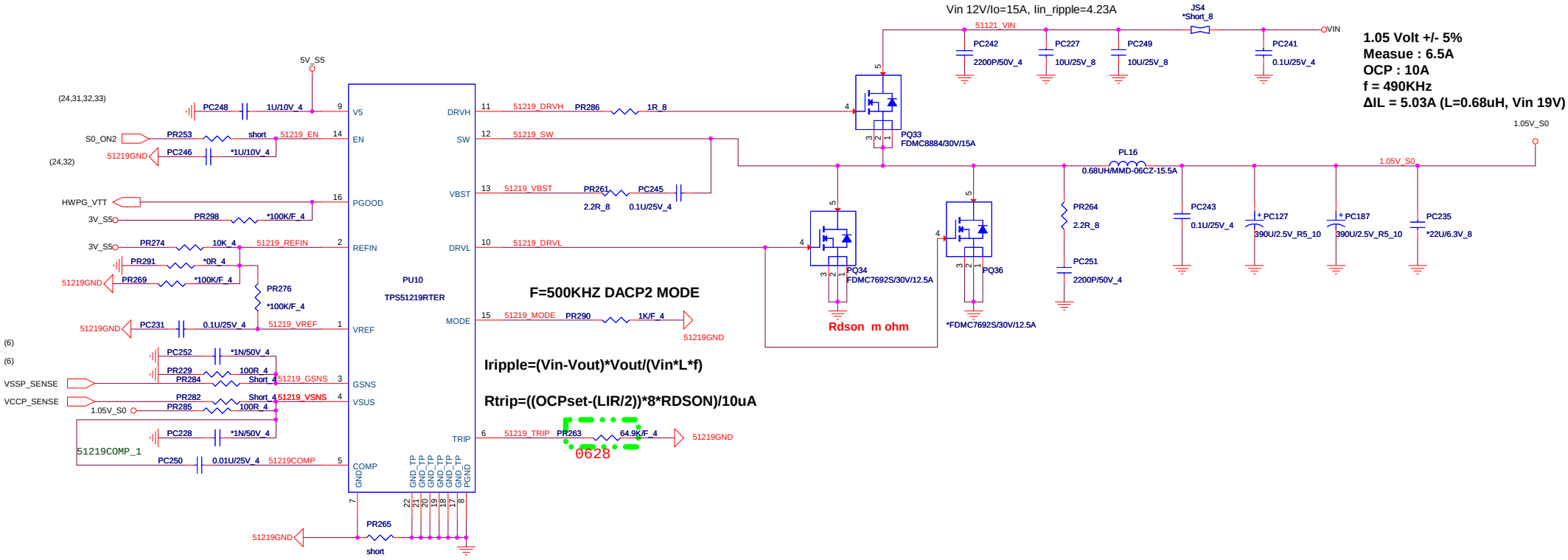

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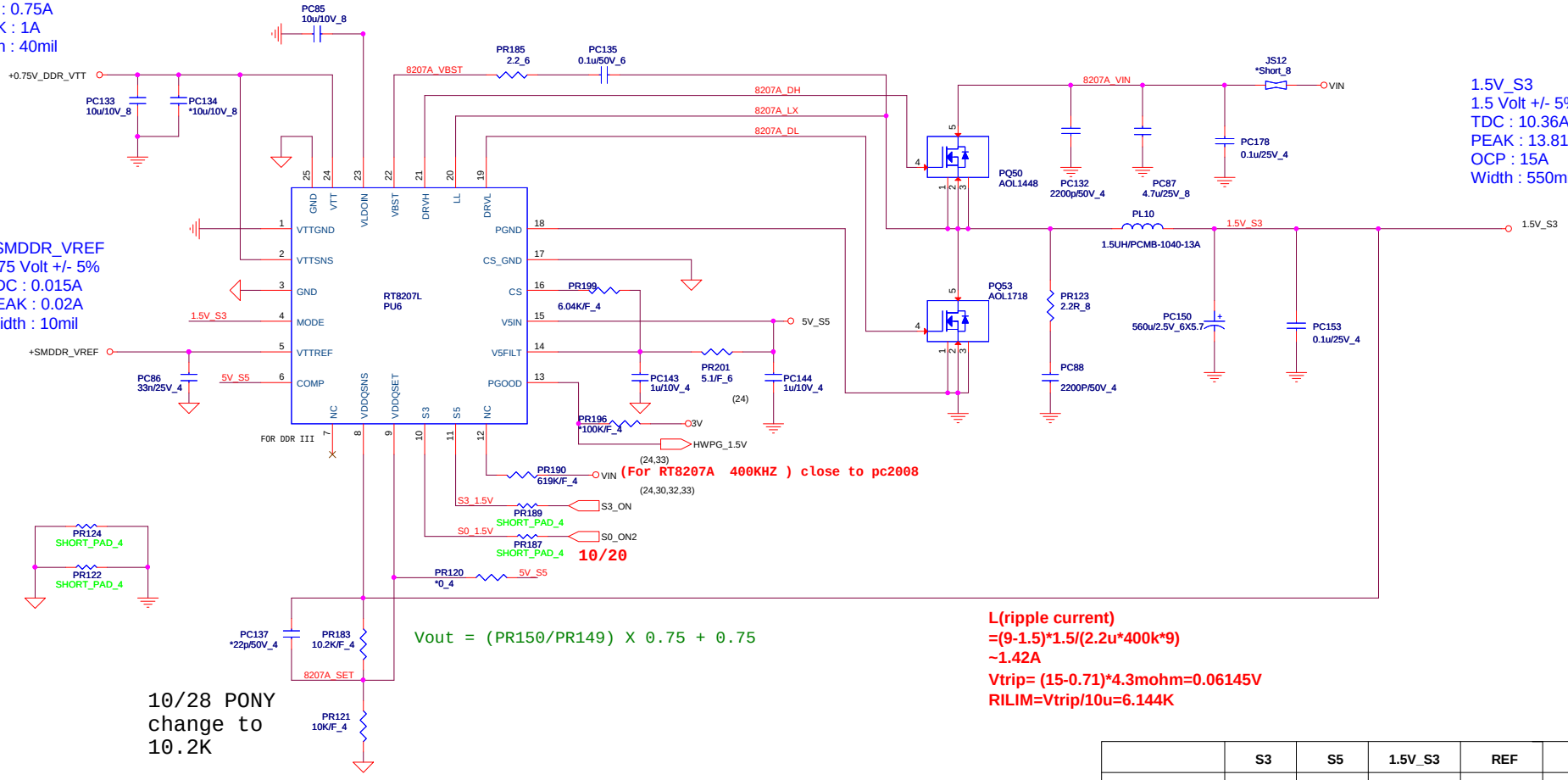
+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.015A
PEAK : 0.02A
Width : 10mil

1.5V_S3
1.5 Volt +/- 5%
TDC : 10.36A
PEAK : 13.81A
OCP : 15A
Width : 550mil



Vout = (PR150/PR149) X 0.75 + 0.75

10/28 PONY change to 10.2K

L(ripple current)
=(9-1.5)*1.5/(2.2u*400k*9)
~1.42A
Vtrip= (15-0.71)*4.3mohm=0.06145V
RILIM=Vtrip/10u=6.144K

	S3	S5	1.5V_S3	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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	DDR 1.5V(RT8207)	1A

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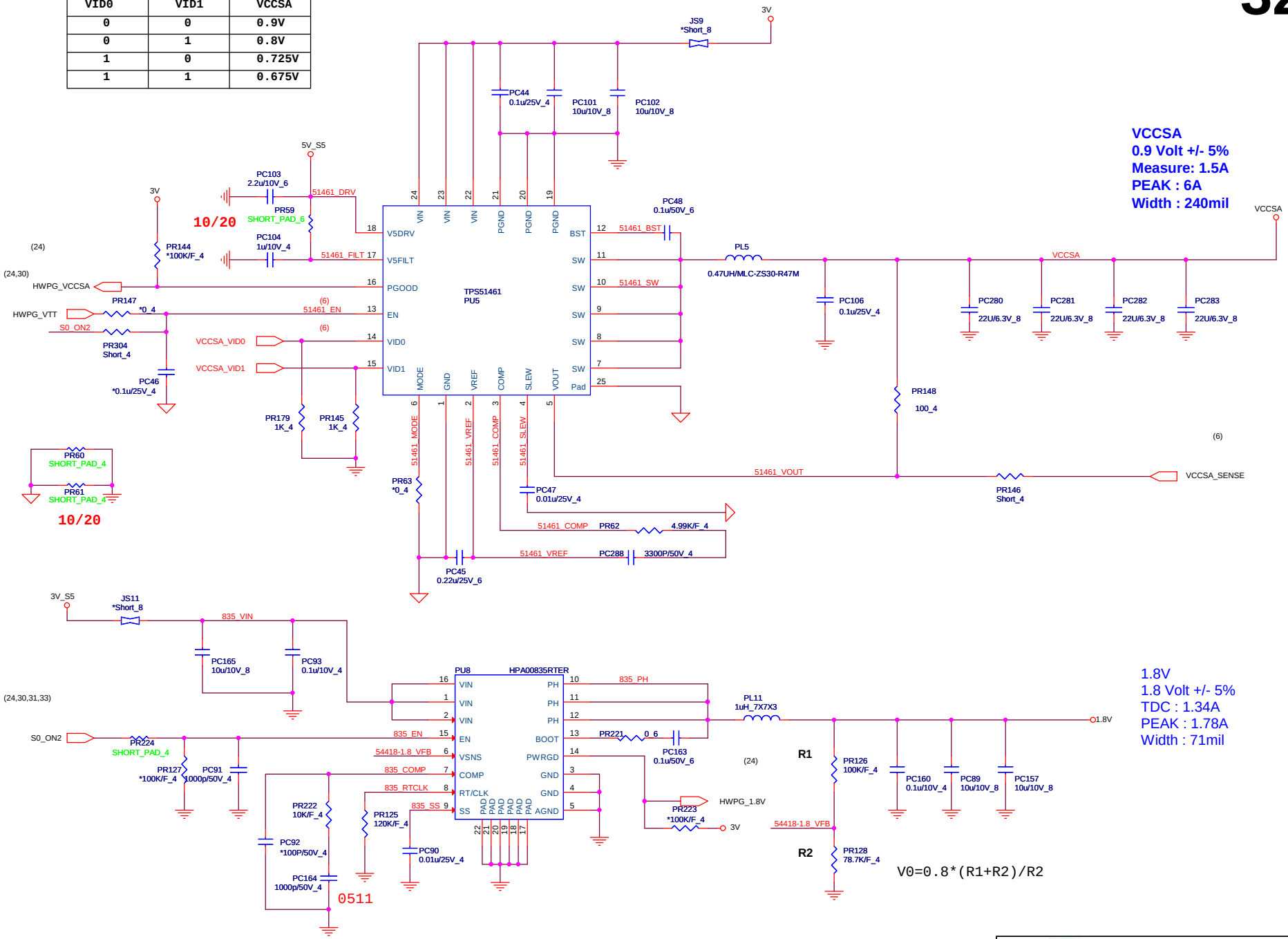
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



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PROJECT : FH5B	
Size	Document Number: VCCSA(TPS51461)/+1.8V(HPA00835) — Rev 1A
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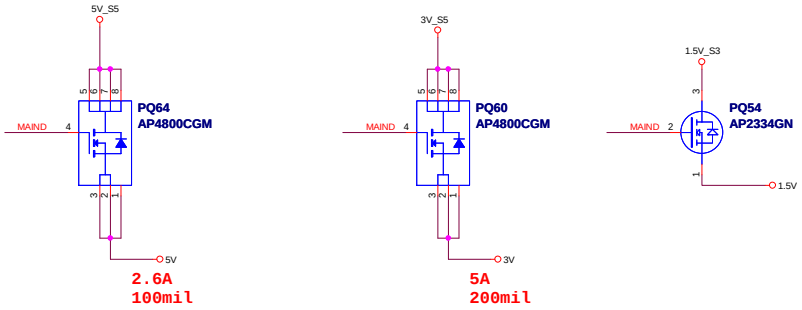
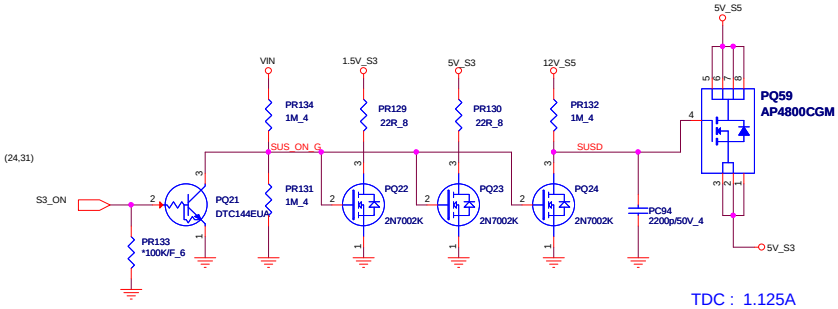
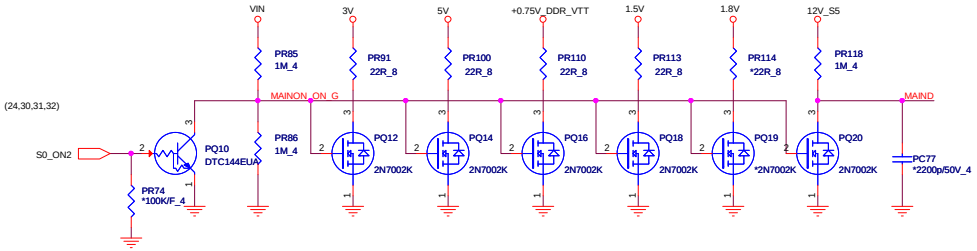
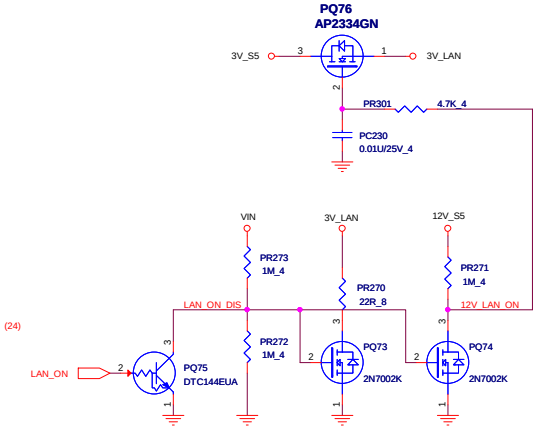




TDC : 1.125A
PEAK : 1.5A
Width : 60mil





Quanta Computer Inc.		
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Model

FH5B MB

CHANGE LIST

REV	
B	The update dtae:5/8 JS8,JS5 ,JS12,JS4,JS15,JS9 ,JS11 change to 0805 short pad JS6,JS7,JS10change to Jump short pad Delete JS12,JS13 short pad Add PC183,PC184,PC185,PC186 390uF OSCON at VCC core add PU8 VIN pin 1,2,16 net name 835_VIN
F	F-01:Add Decaupling Cap C291,C1299 1uf -Page 08 F-02:Add Decaupling Cap C1300,1301,1302 -page22 F-03:Add 1.5V power rail for mSATA -page 21
C	

Quanta Computer Inc.
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	Change list	1A

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DOC NO.					
PROJECT MODEL :	FH5B	APPROVED BY:		DATE:	2012/05/10
PART NUMBER:		DRAWING BY:		REVISON:	1A