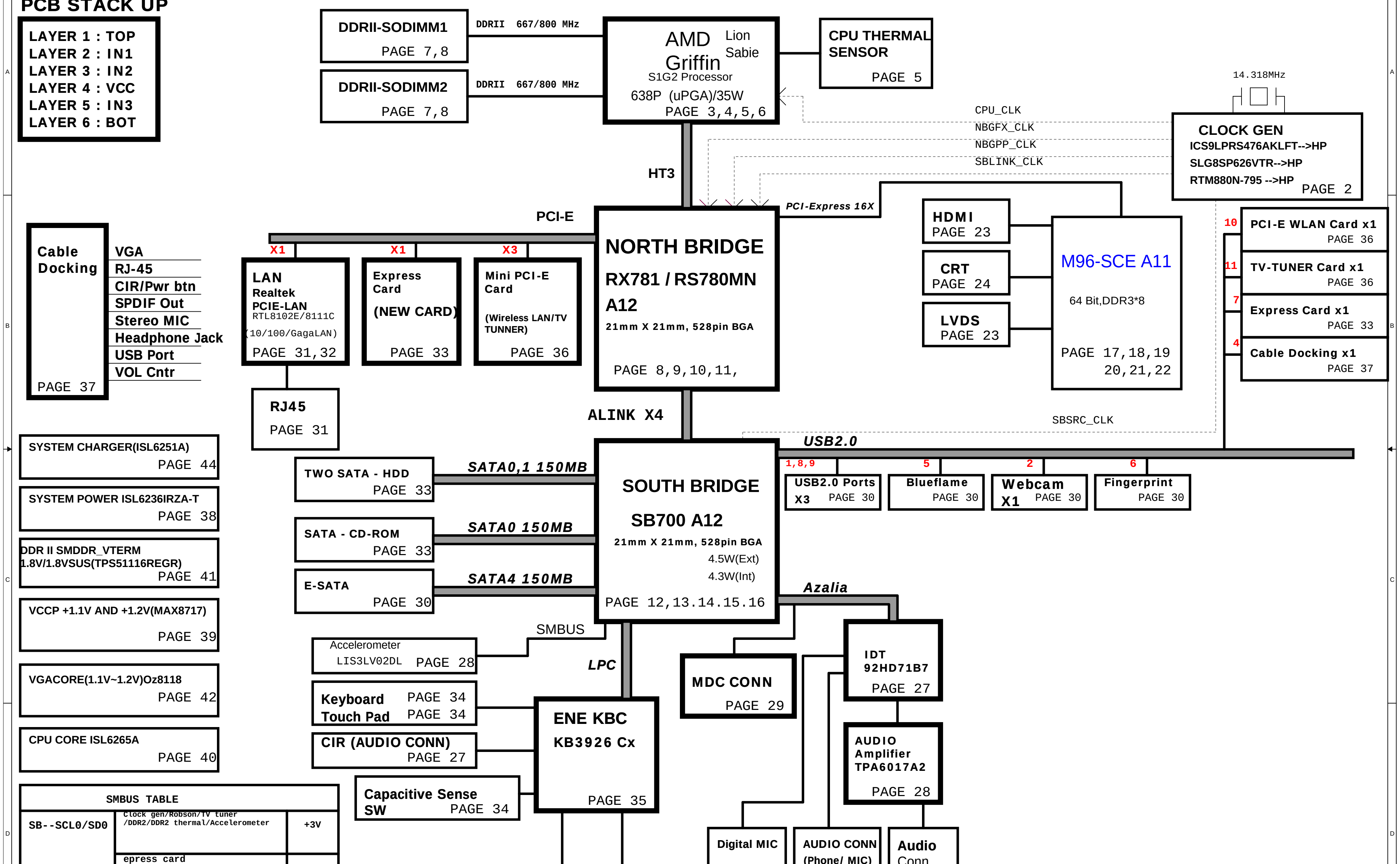
UT12 SYSTEM DIAGRAM

01



SMBUS TABLE

SB--SCL0/SD0	clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
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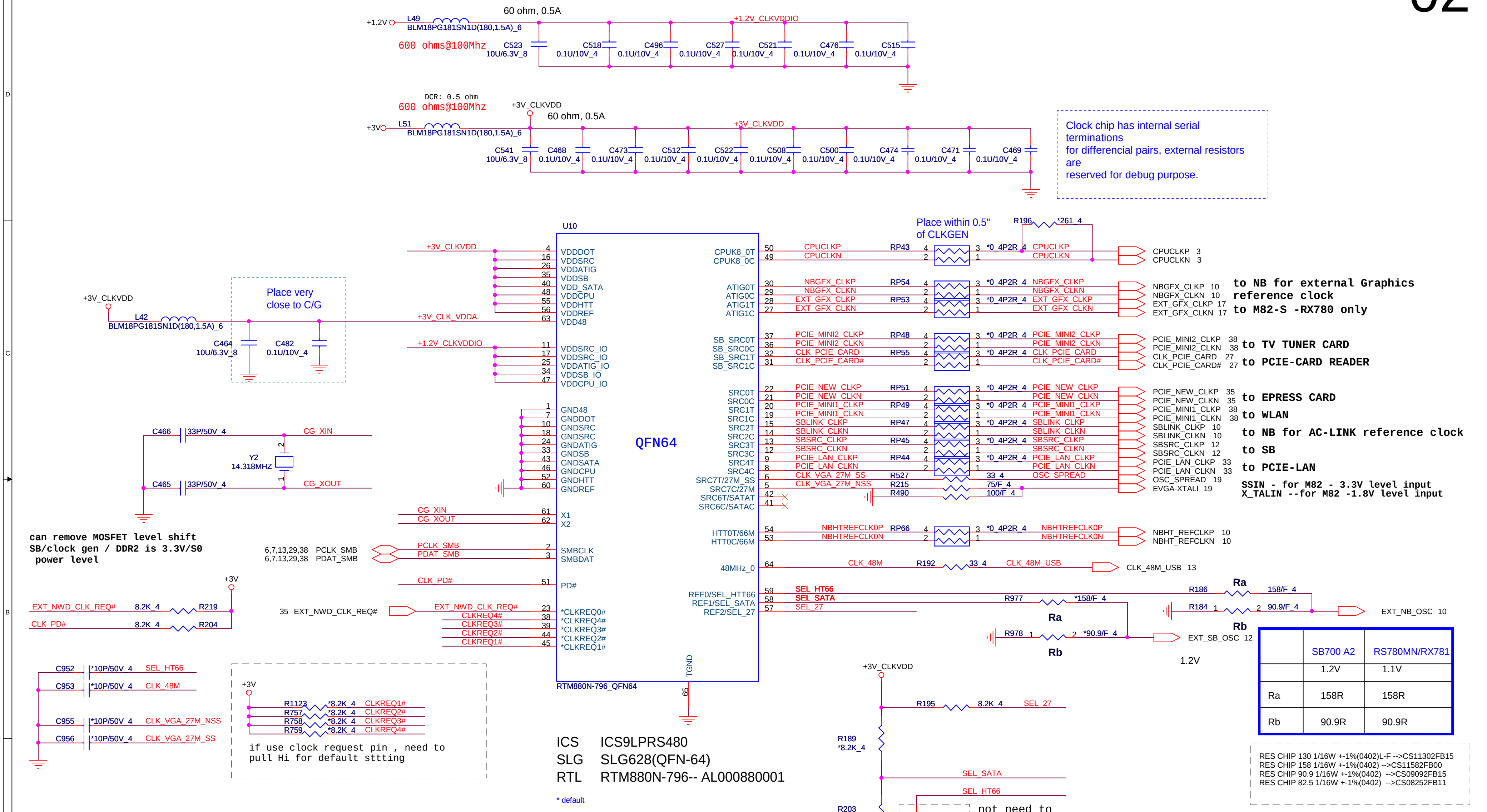
Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Thursday, October 16, 2008 Sheet 1 of 48



ICS ICS9LPRS480
SLG SLG628(QFN-64)
RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

	SB700 A2	RS780MN/RX781
	1.2V	1.1V
Ra	158R	158R
Rb	90.9R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

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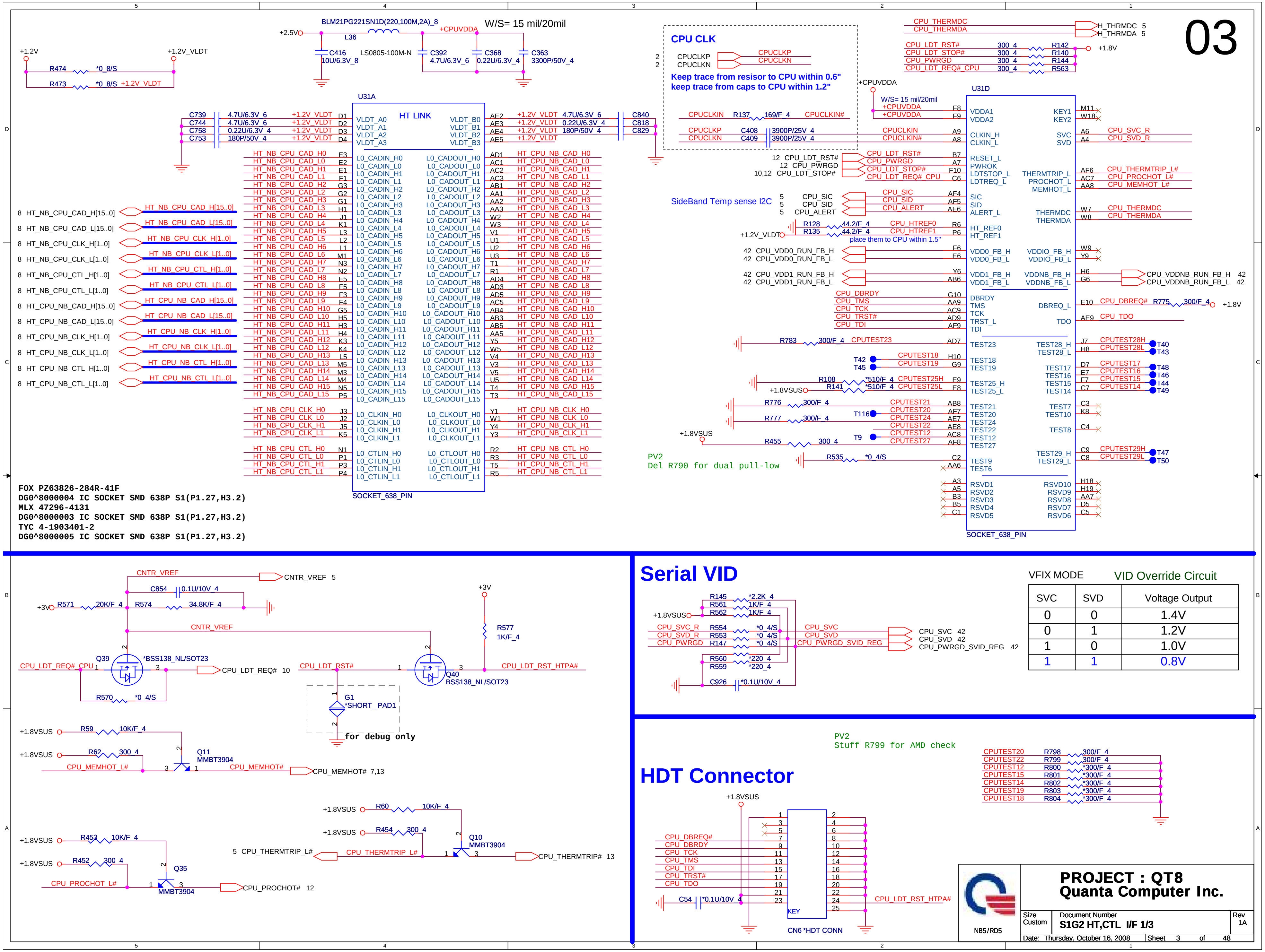
NB5/RD5

Size	Document Number	Rev
Custom	Clock Generator	1A

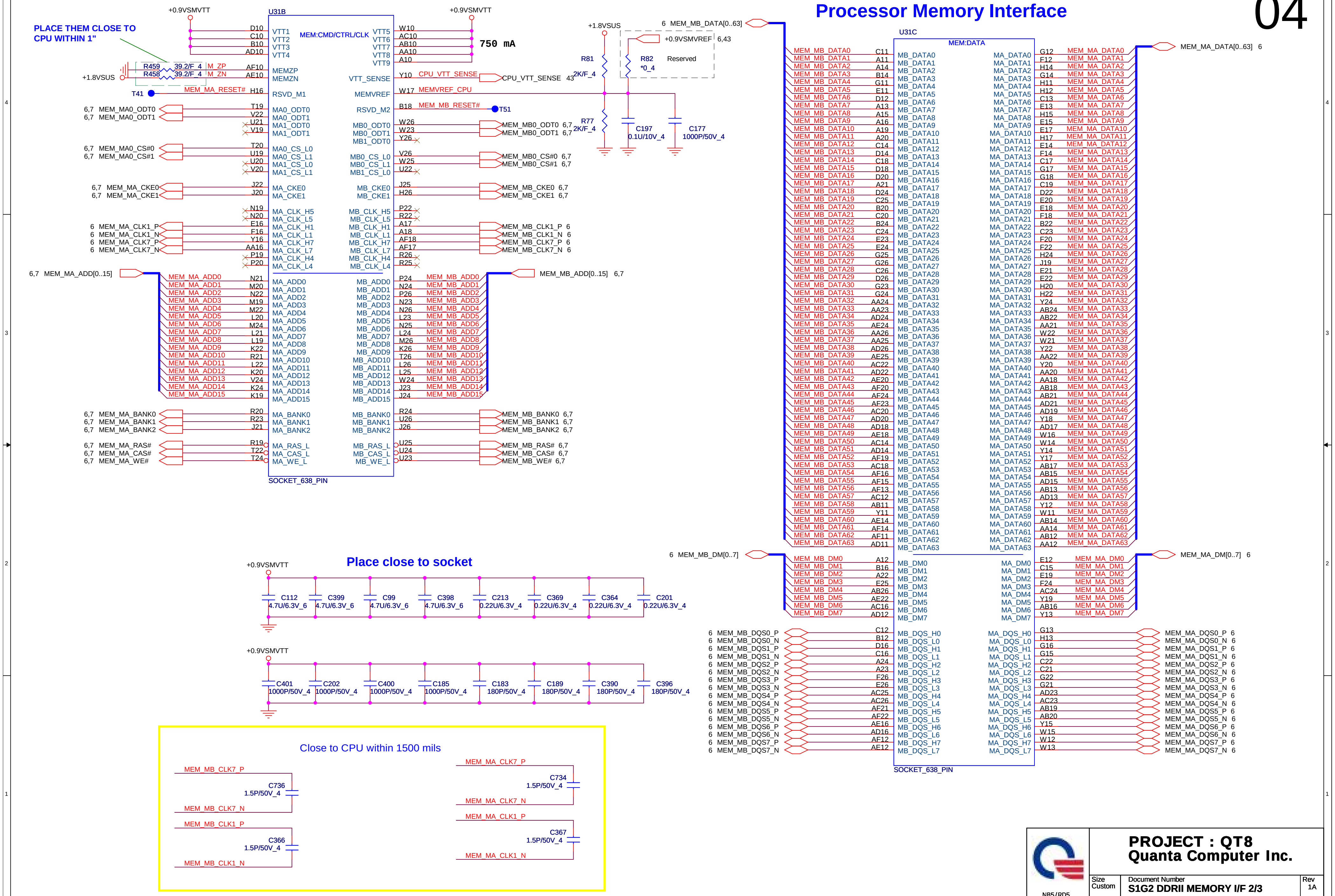
Date: Thursday, October 16, 2008 Sheet 2 of 48



SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

Processor Memory Interface

04



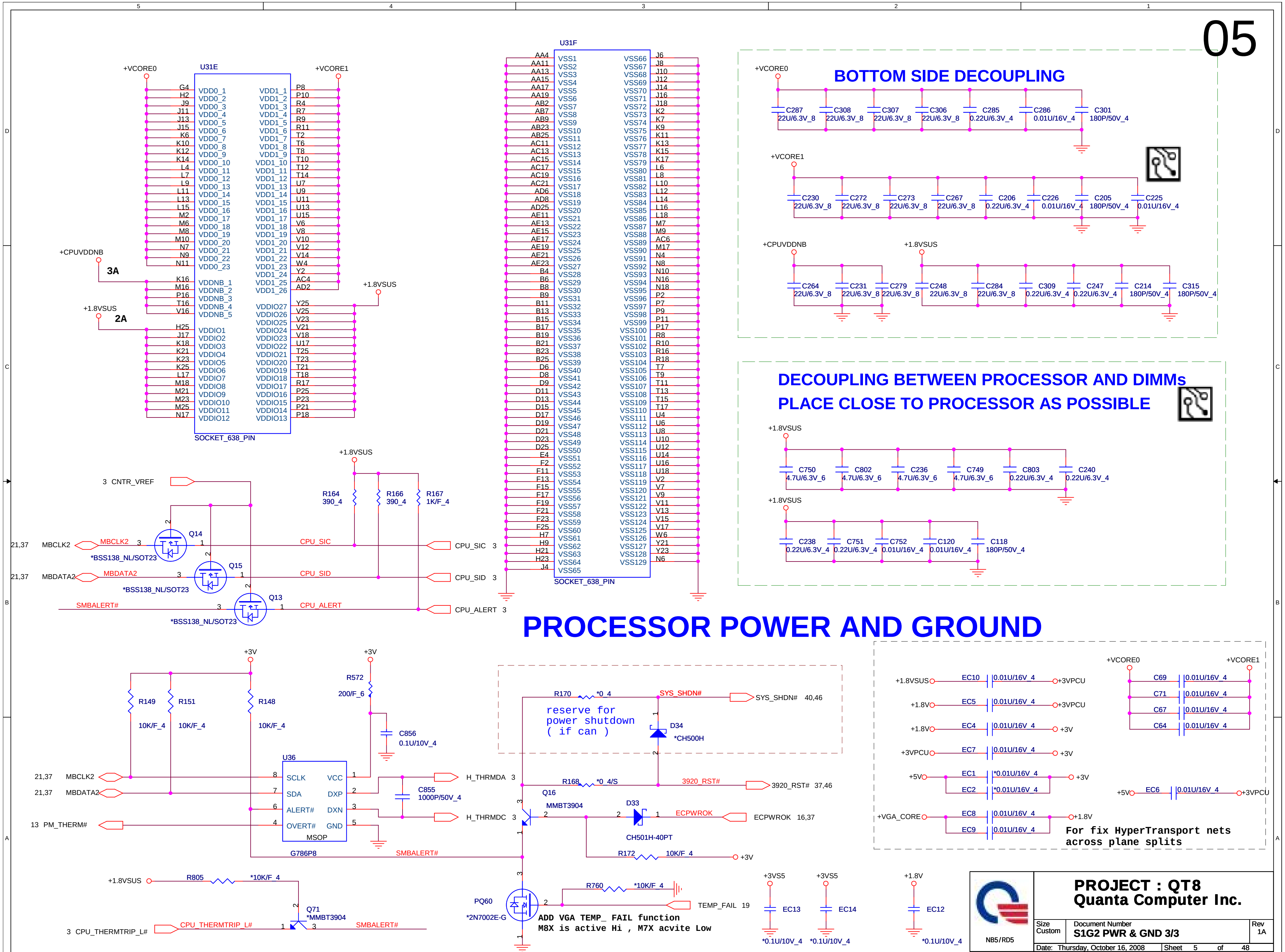
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	S1G2 DDRII MEMORY I/F 2/3	1A

Date: Thursday, October 16, 2008 | Sheet 4 of 48

05

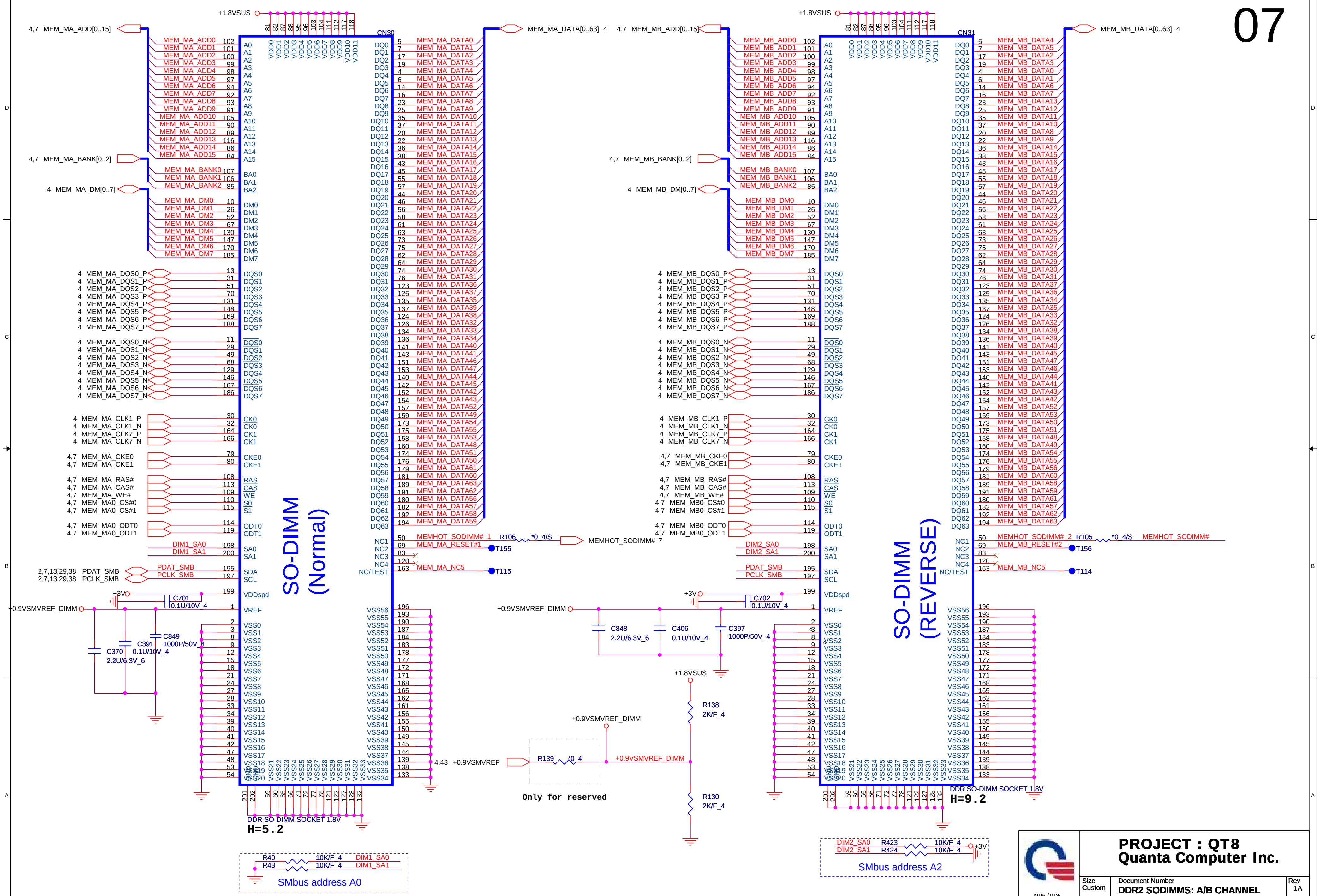


PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

Date: Thursday, October 16, 2008 Sheet 5 of 48

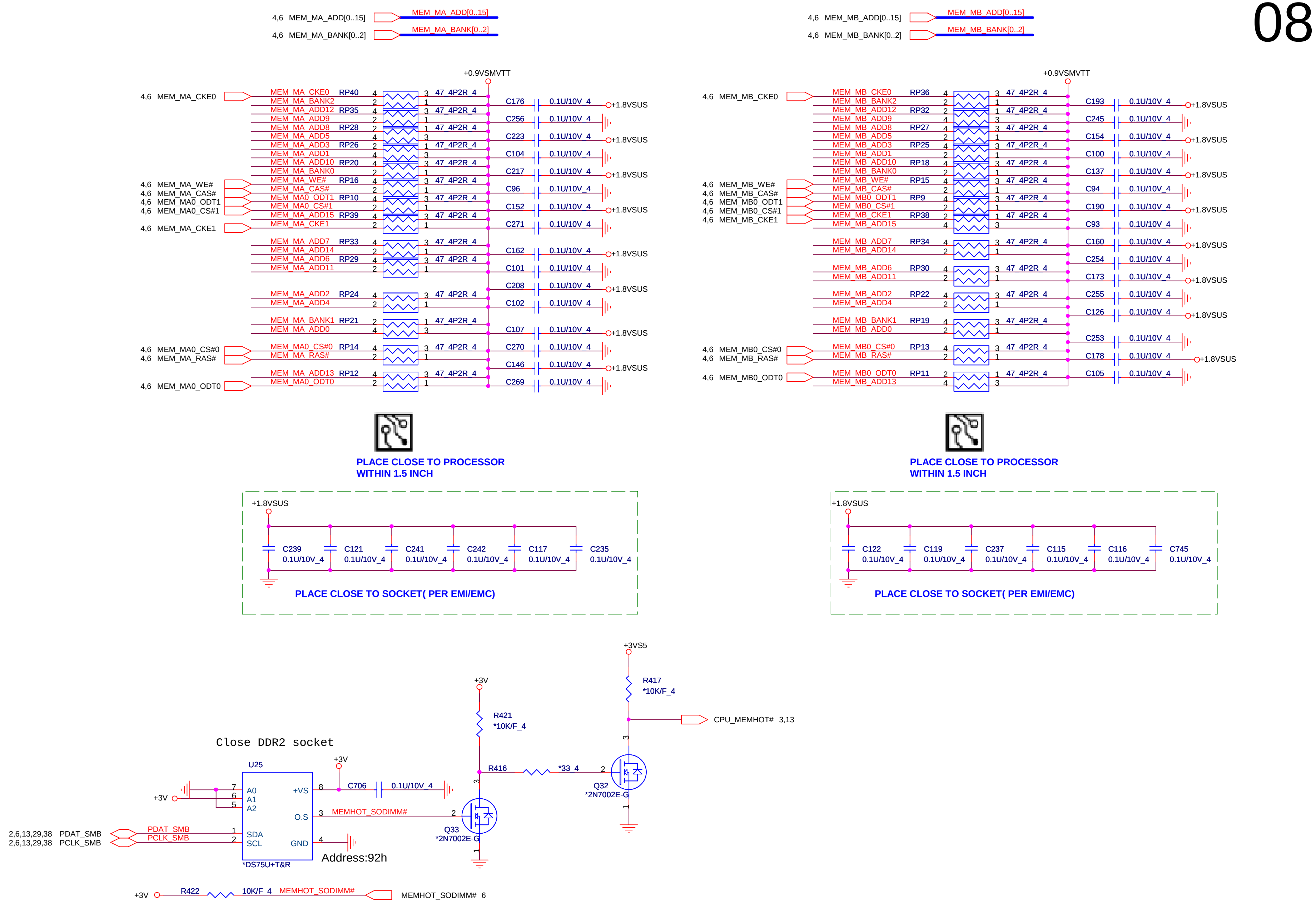


PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	1A

Date: Thursday, October 16, 2008 | Sheet 6 of 48



PROJECT : QT8
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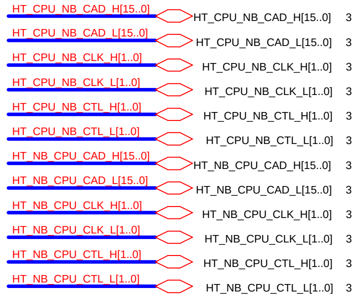
NB5/RD5

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

Date: Thursday, October 16, 2008 | Sheet 7 of 48

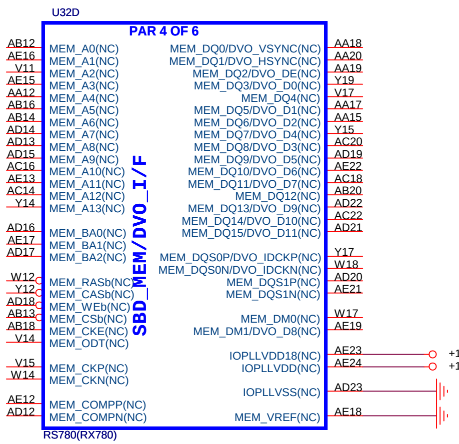


signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

This block is for UMA RS780 only , RX780 can remove all component



IOPLLVDD18 - memory PLL
not applicable to RX780

IOPLLVDD- memory PLL
not applicable to RX780

NB5/RD5

PROJECT : QT8
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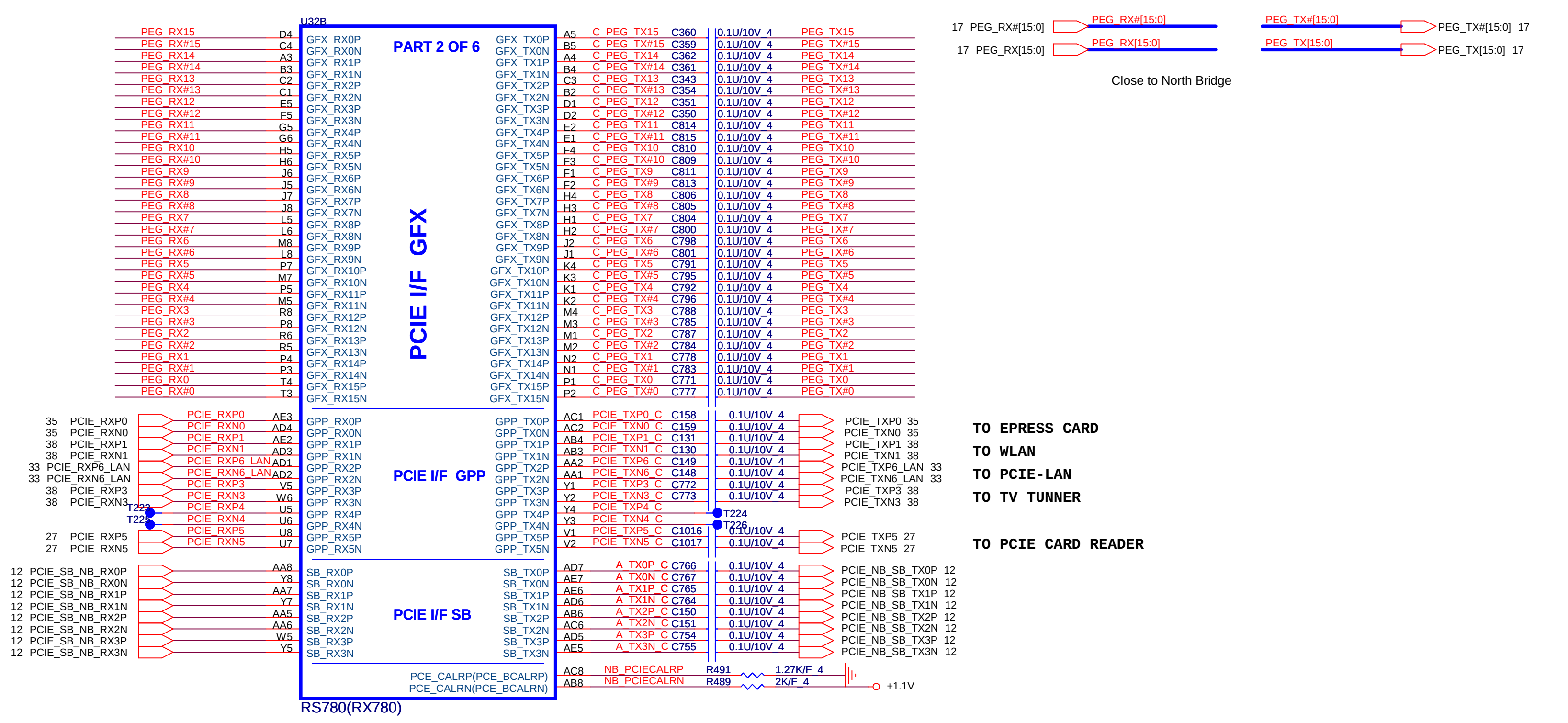
Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A



RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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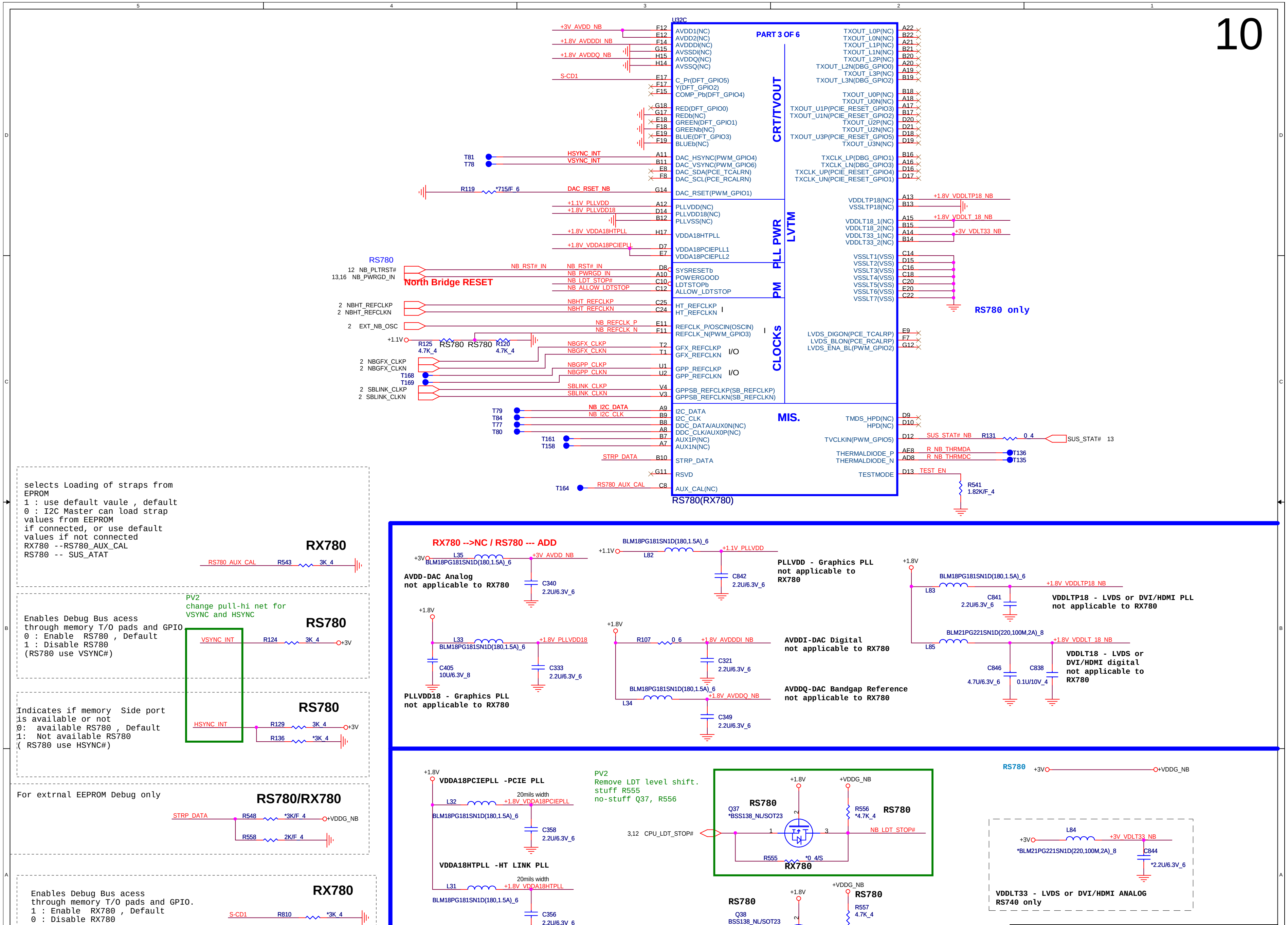
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

Date: Thursday, October 16, 2008 | Sheet 9 of 48

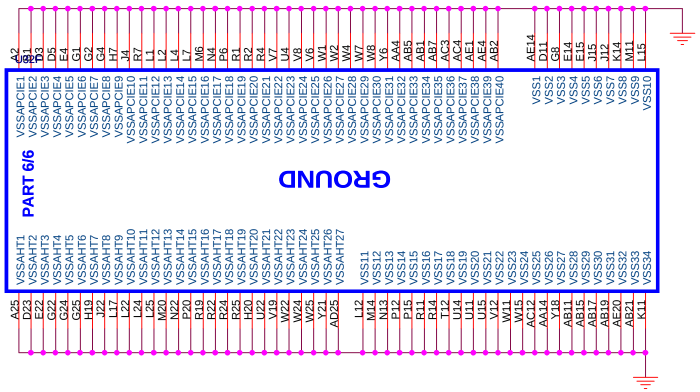


PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A

Date: Thursday, October 16, 2008 Sheet 10 of 48

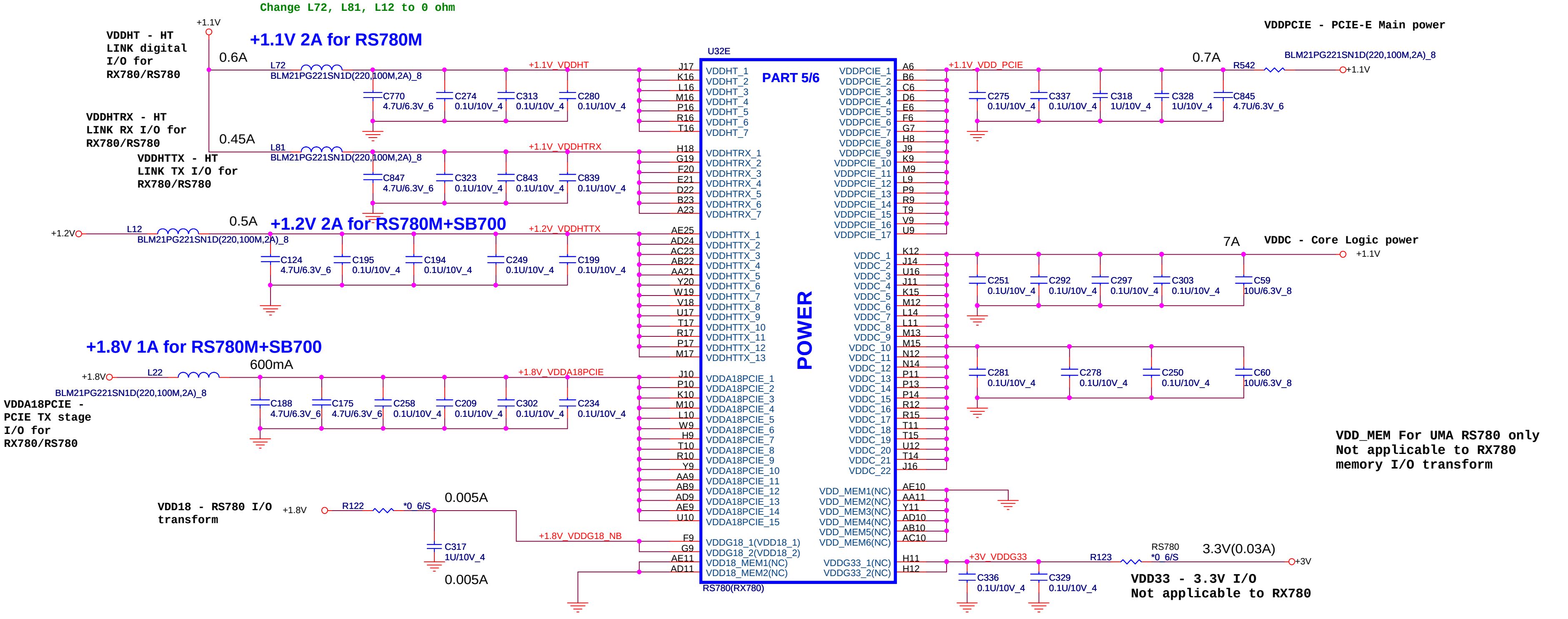
NB5/RD5



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

PV2
Change L72, L81, L12 to 0 ohm

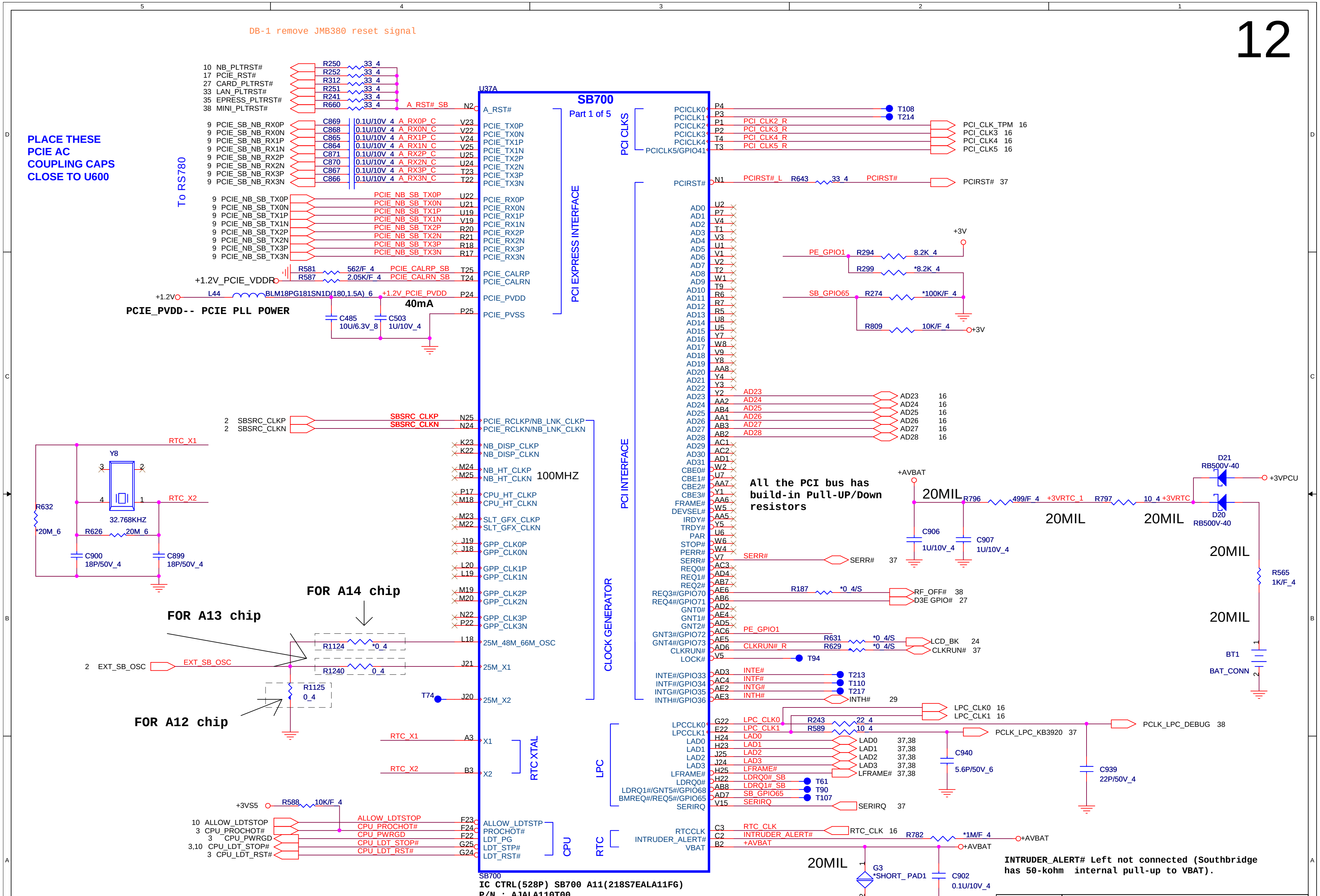


PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

Date: Thursday, October 16, 2008 Sheet 11 of 48

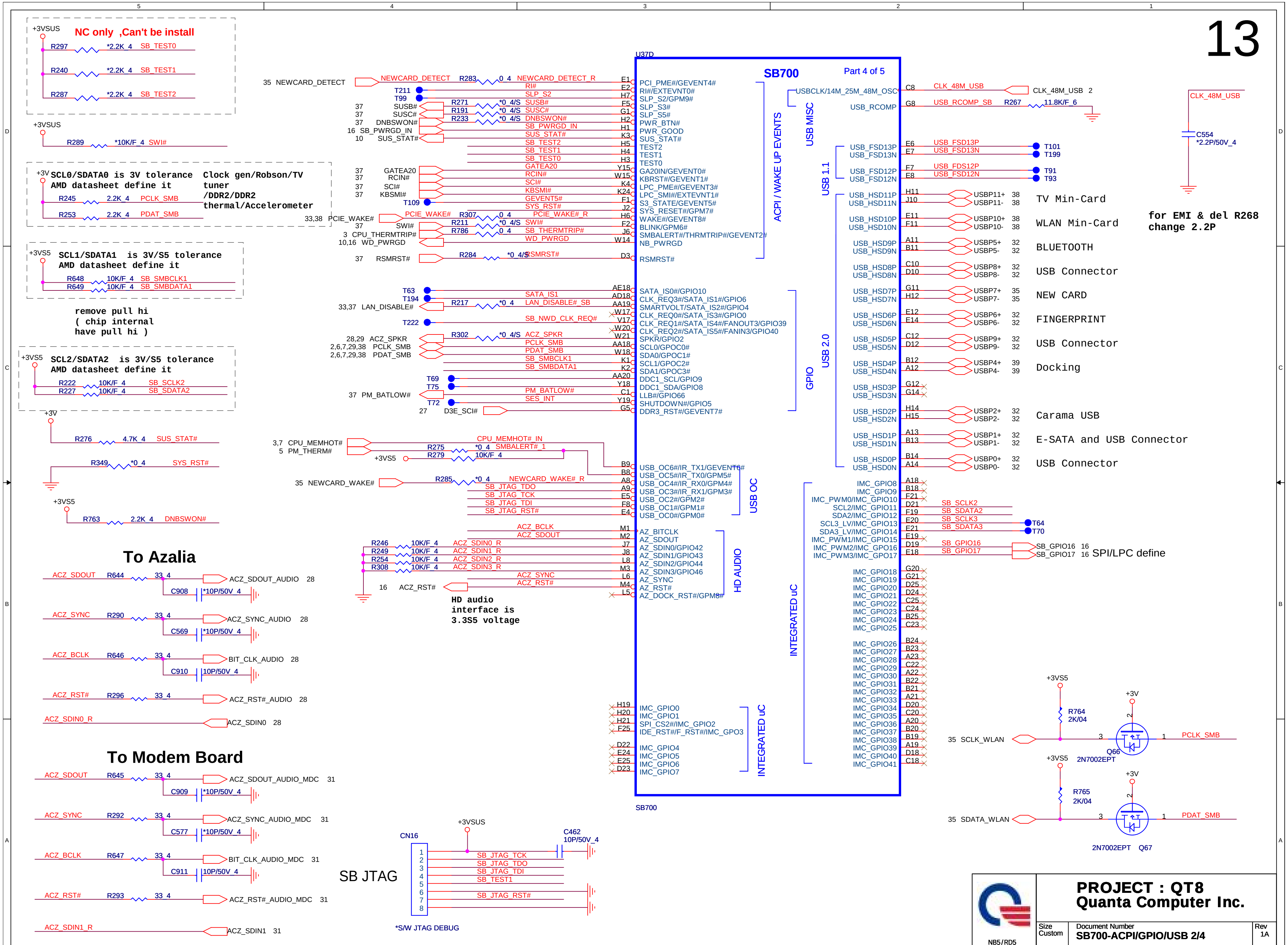


PROJECT : QT8
Quanta Computer Inc.

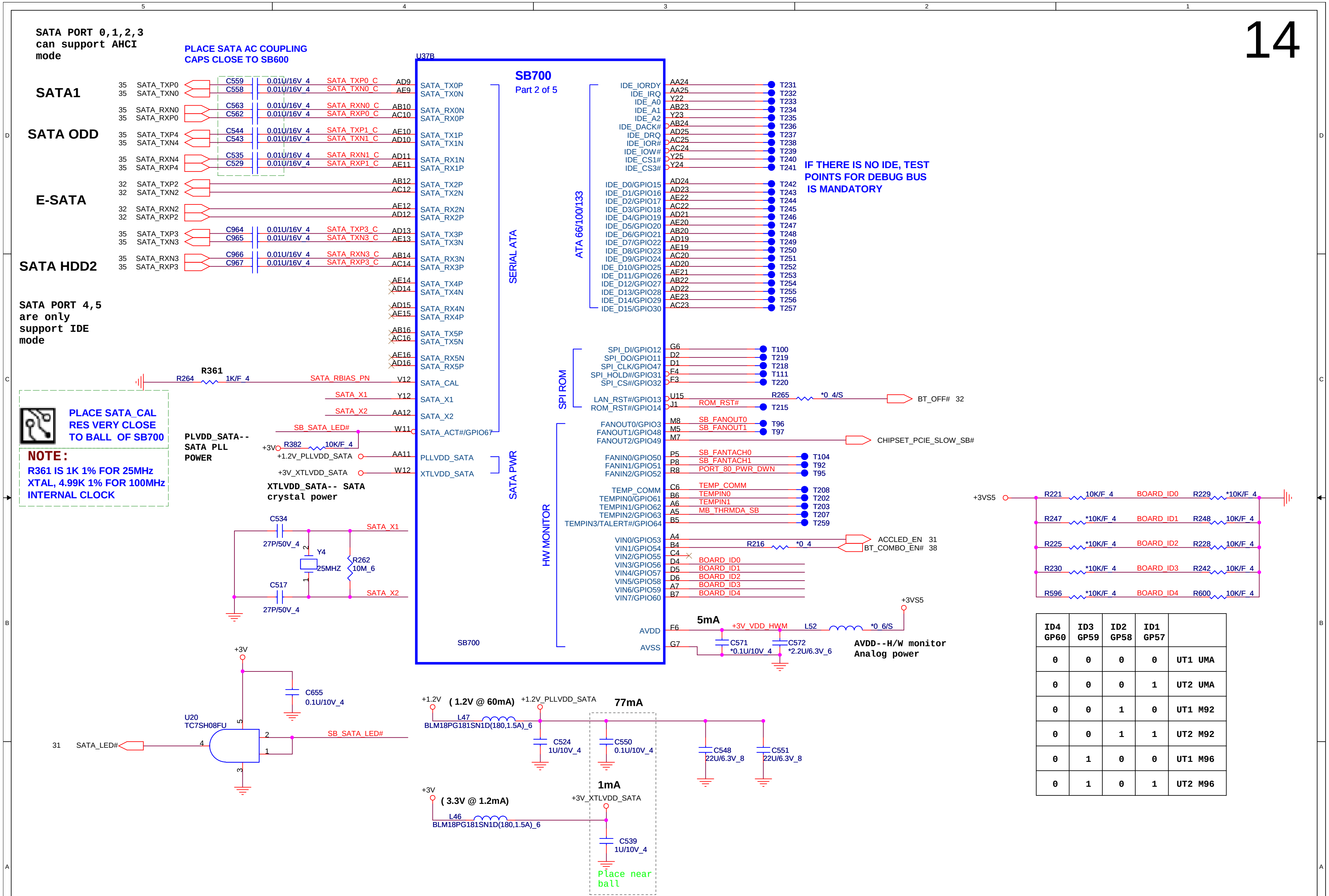
NB5/RD5

Size	Document Number	Rev
Custom	SB700-PCIE/PCI/CPU/LPC 1/4	1A

Date: Thursday, October 16, 2008 Sheet 12 of 48



NB5/RD5	PROJECT : QT8 Quanta Computer Inc.		
Size: Custom	Document Number: SB700-ACPI/GPIO/USB 2/4		Rev: 1A
Date: Thursday, October 16, 2008	Sheet 13 of 48		

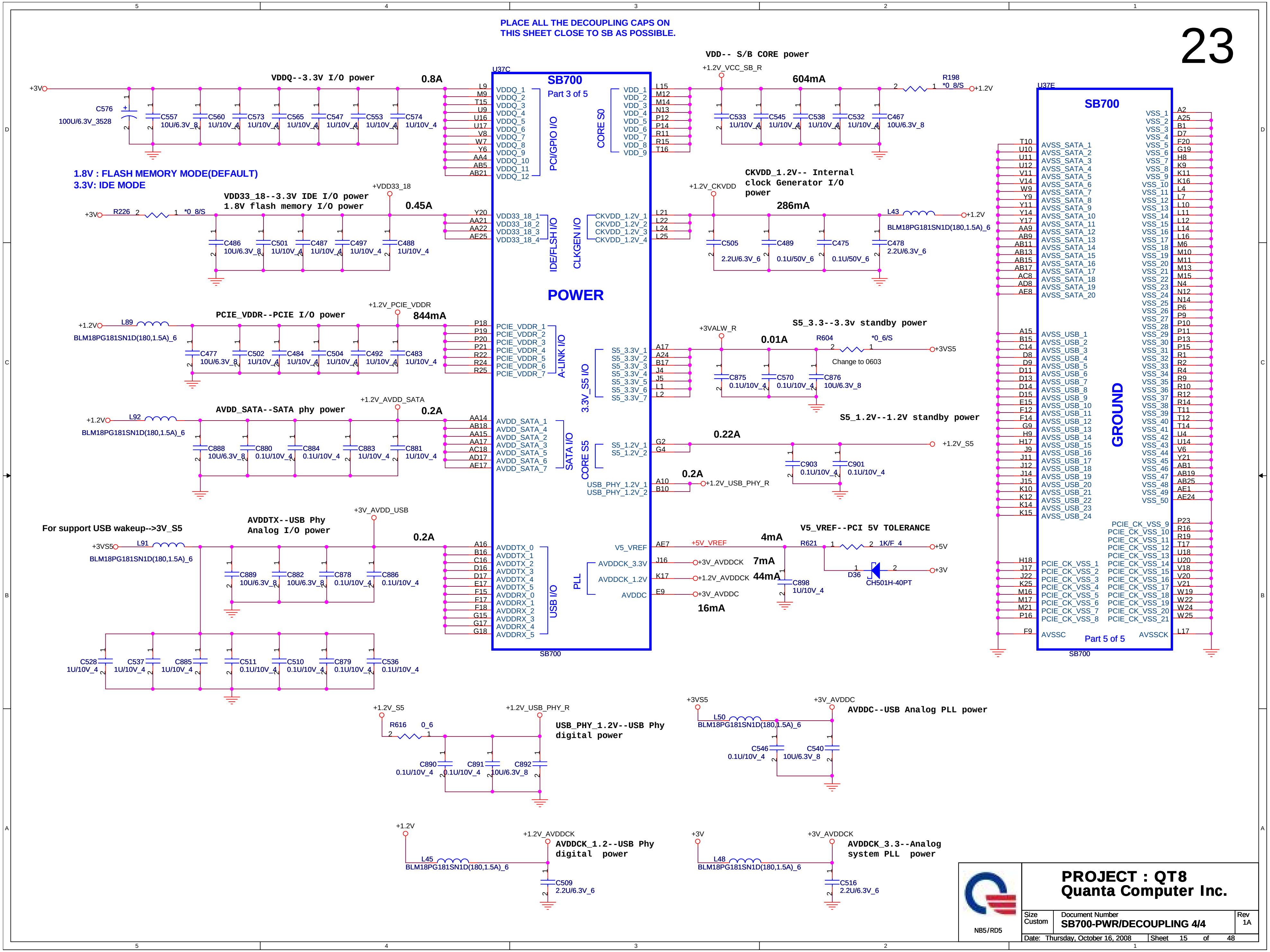


ID4 GP60	ID3 GP59	ID2 GP58	ID1 GP57	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

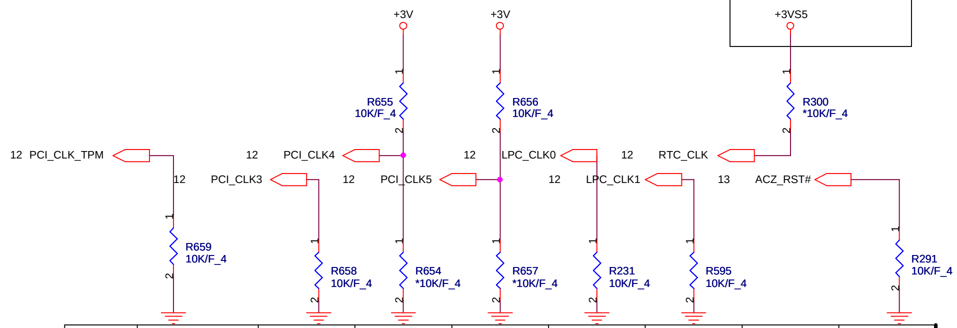


PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.
23
VDDQ--3.3V I/O power
0.8A
VDD-- S/B CORE power
604mA
SB700
Part 3 of 5
PCI/GPIO I/O
CORE S0
1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE
VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power
0.45A
CKVDD_1.2V-- Internal
clock Generator I/O
power
286mA
IDE/FLSH I/O
CLKGEN I/O
POWER
PCIE_VDDR--PCIE I/O power
844mA
A-LINK I/O
S5_3.3--3.3v standby power
0.01A
Change to 0603
3.3V_S5 I/O
AVDD_SATA--SATA phy power
0.2A
SATA I/O
CORE S5
S5_1.2V--1.2V standby power
0.22A
0.2A
For support USB wakeup-->3V_S5
AVDDTX--USB Phy
Analog I/O power
0.2A
V5_VREF--PCI 5V TOLERANCE
4mA
7mA
44mA
16mA
PLL
USB I/O
SB700
Part 5 of 5
GROUND
USB_PHY_1.2V--USB Phy
digital power
AVDDC--USB Analog PLL power
AVDDCK_1.2--USB Phy
digital power
AVDDCK_3.3--Analog
system PLL power
PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number SB700-PWR/DECOUPLING 4/4
Rev 1A
Date: Thursday, October 16, 2008
Sheet 15 of 48

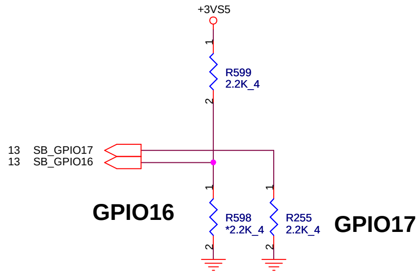
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

It must ready refore RSMRST#



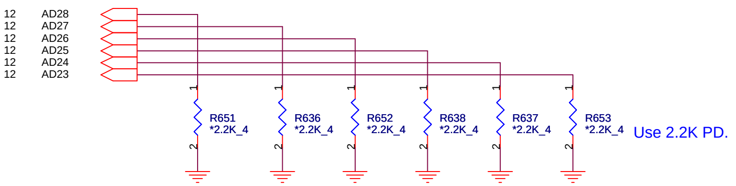
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

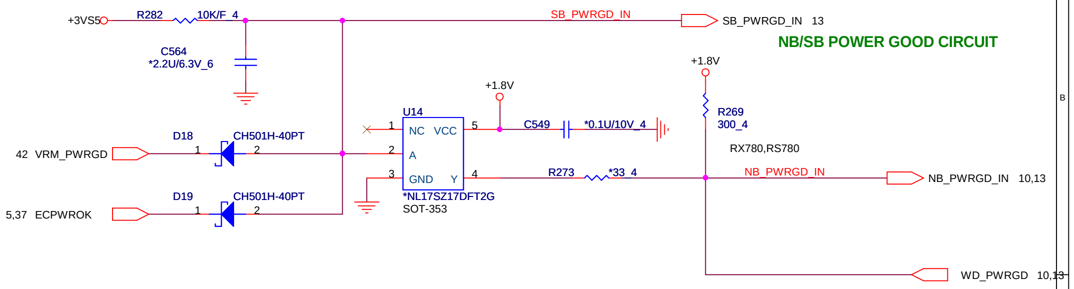
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



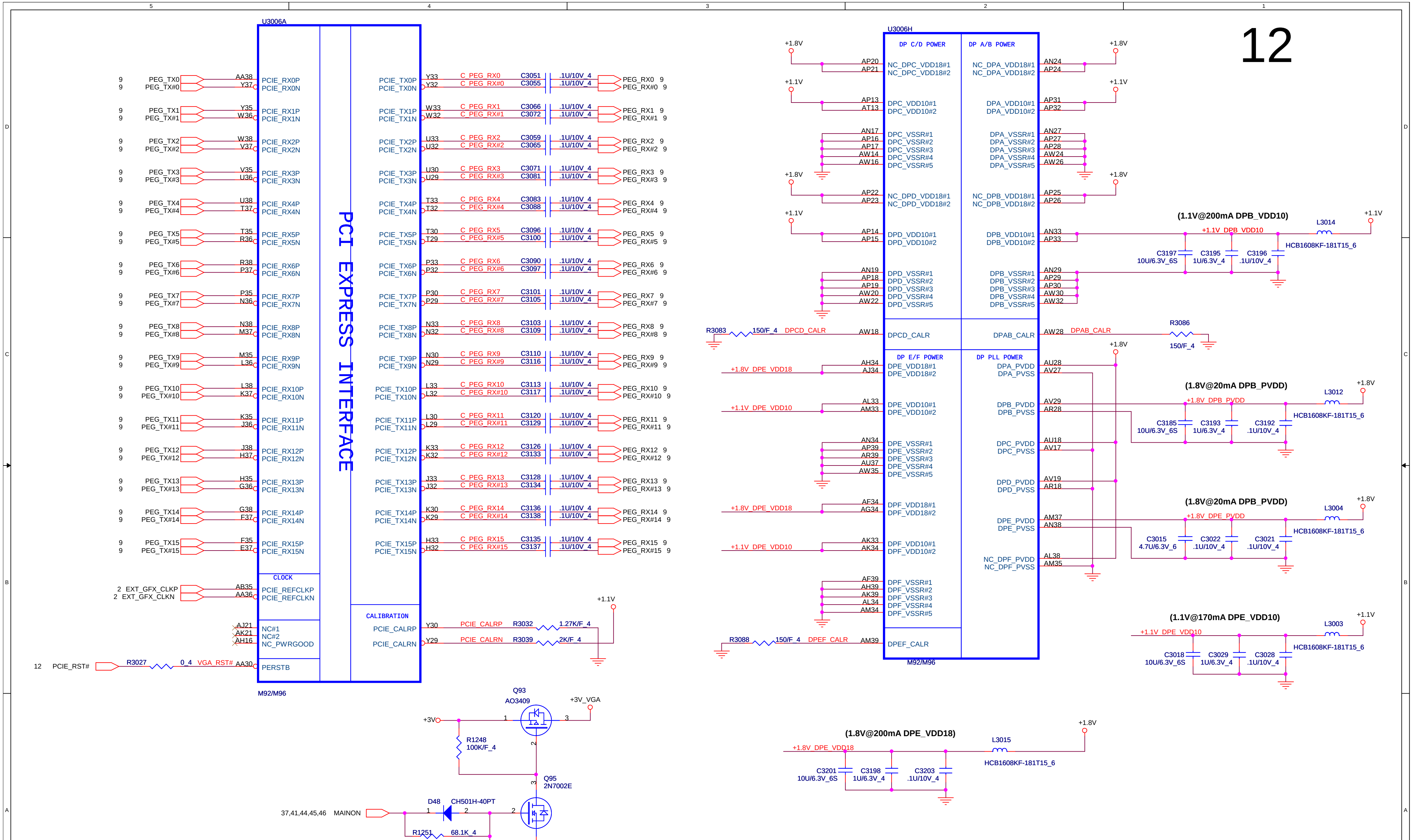
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

NB/SB POWER GOOD CIRCUIT



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

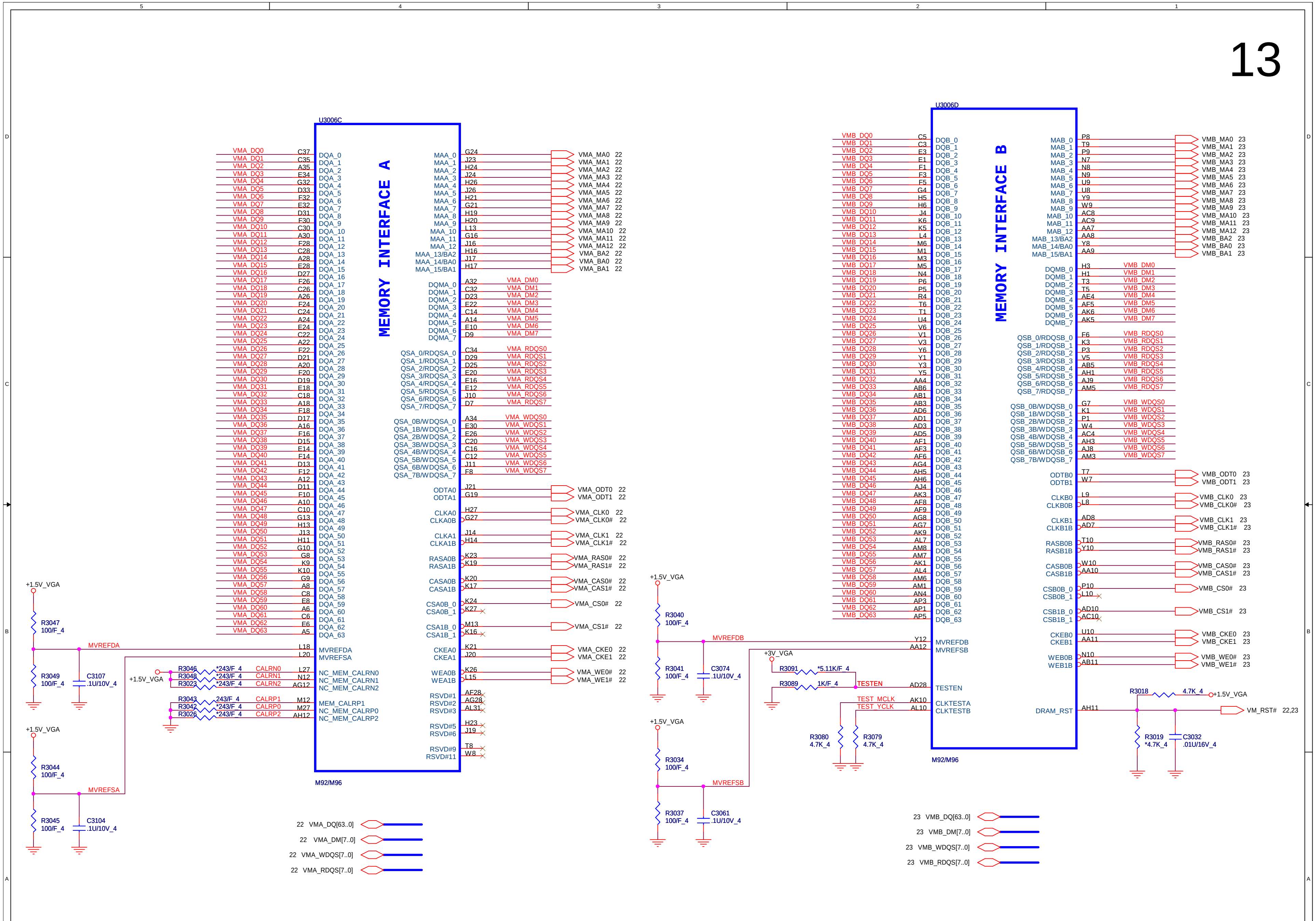


PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	M92/M96 (PCIE / DP POWER)	DB

Date: Thursday, October 16, 2008 | Sheet 17 of 43

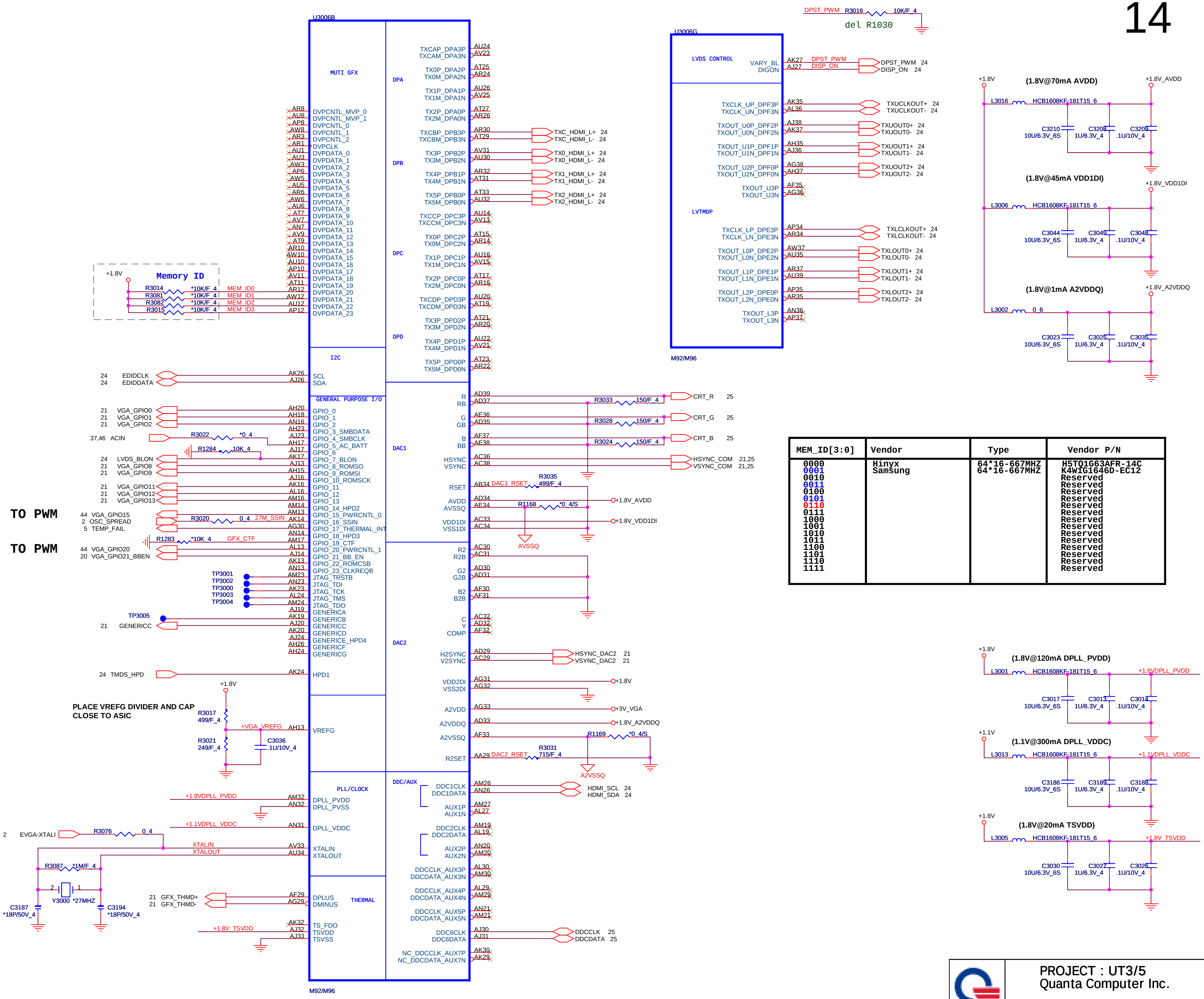


PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	M92/M96 (Memory I/F)	DB

Date: Thursday, October 16, 2008 | Sheet 18 of 43

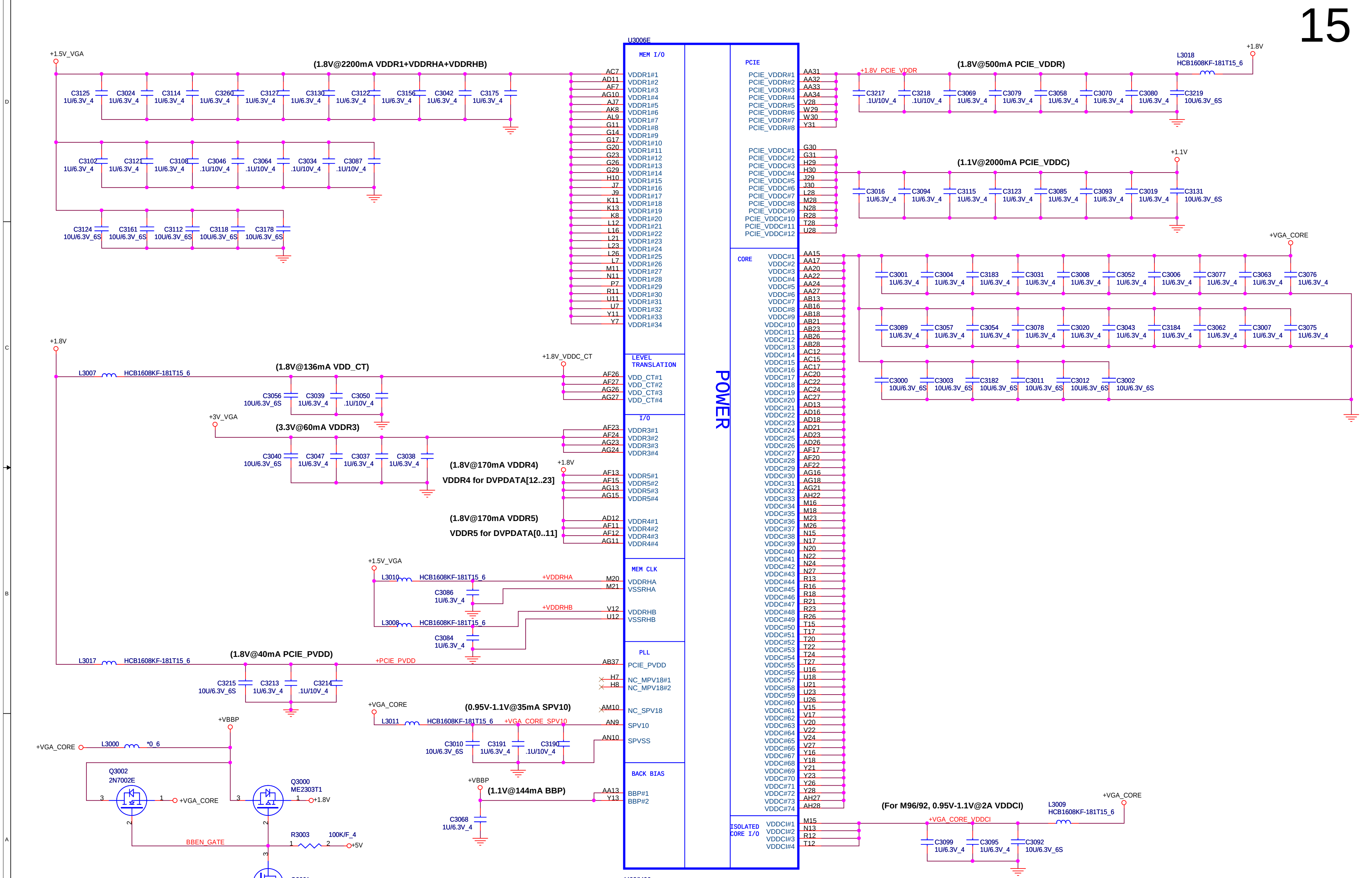


MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinyx	64*16-667MHZ	H5TQ1G63AFR-14C
0001	Samsung	64*16-667MHZ	K4W1G1646D-EC12
0010			Reserved
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size: Custom
Document Number: M92/M96 (Main)
Rev: DB

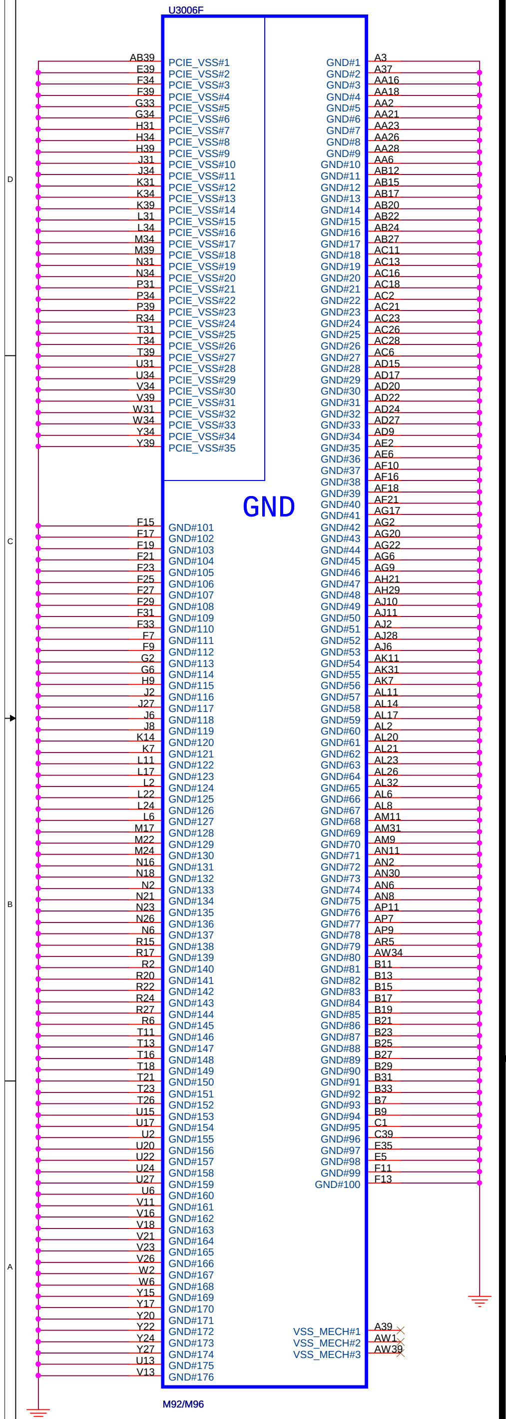


PROJECT : UT3/5
Quanta Computer Inc.

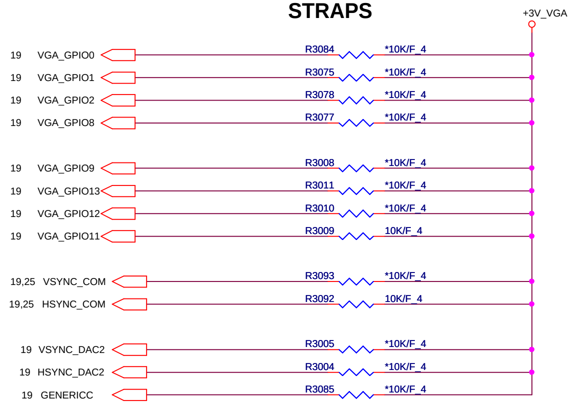
NB5

Size	Document Number	Rev
Custom	M92/M96(POWER AND NC)	DB

Date: Thursday, October 16, 2008 Sheet 20 of 43



STRAPS



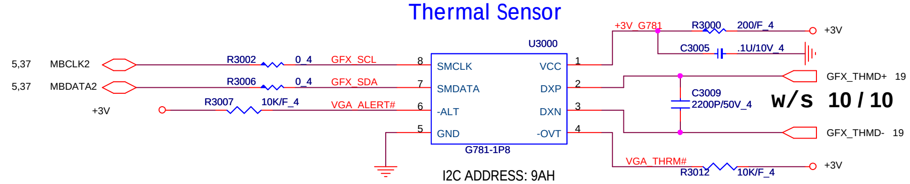
Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0

Overlap pads to save space and to prevent assembly of both resistors.

Layout

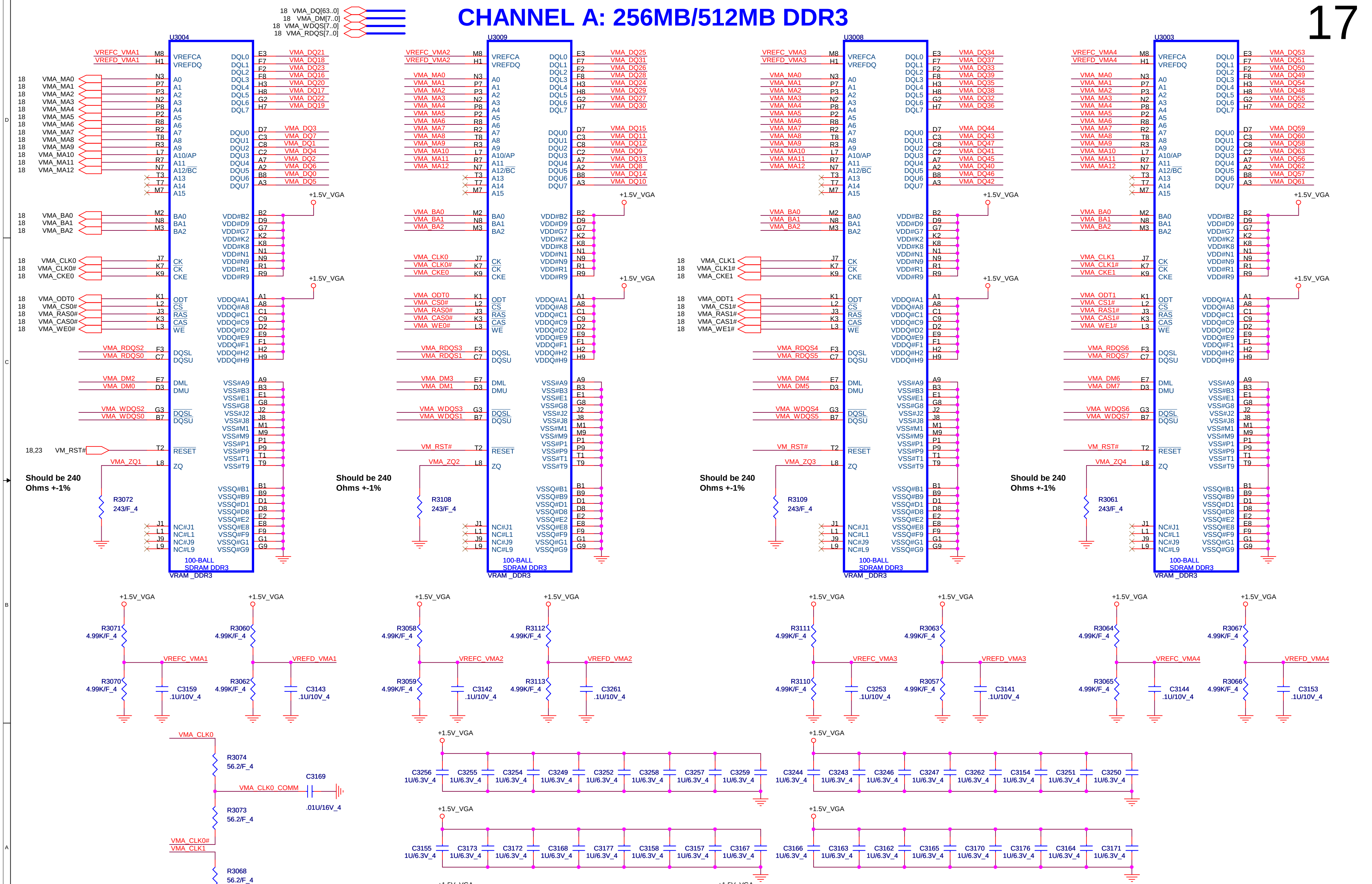
Ground — Signal — High logic voltage

Thermal Sensor



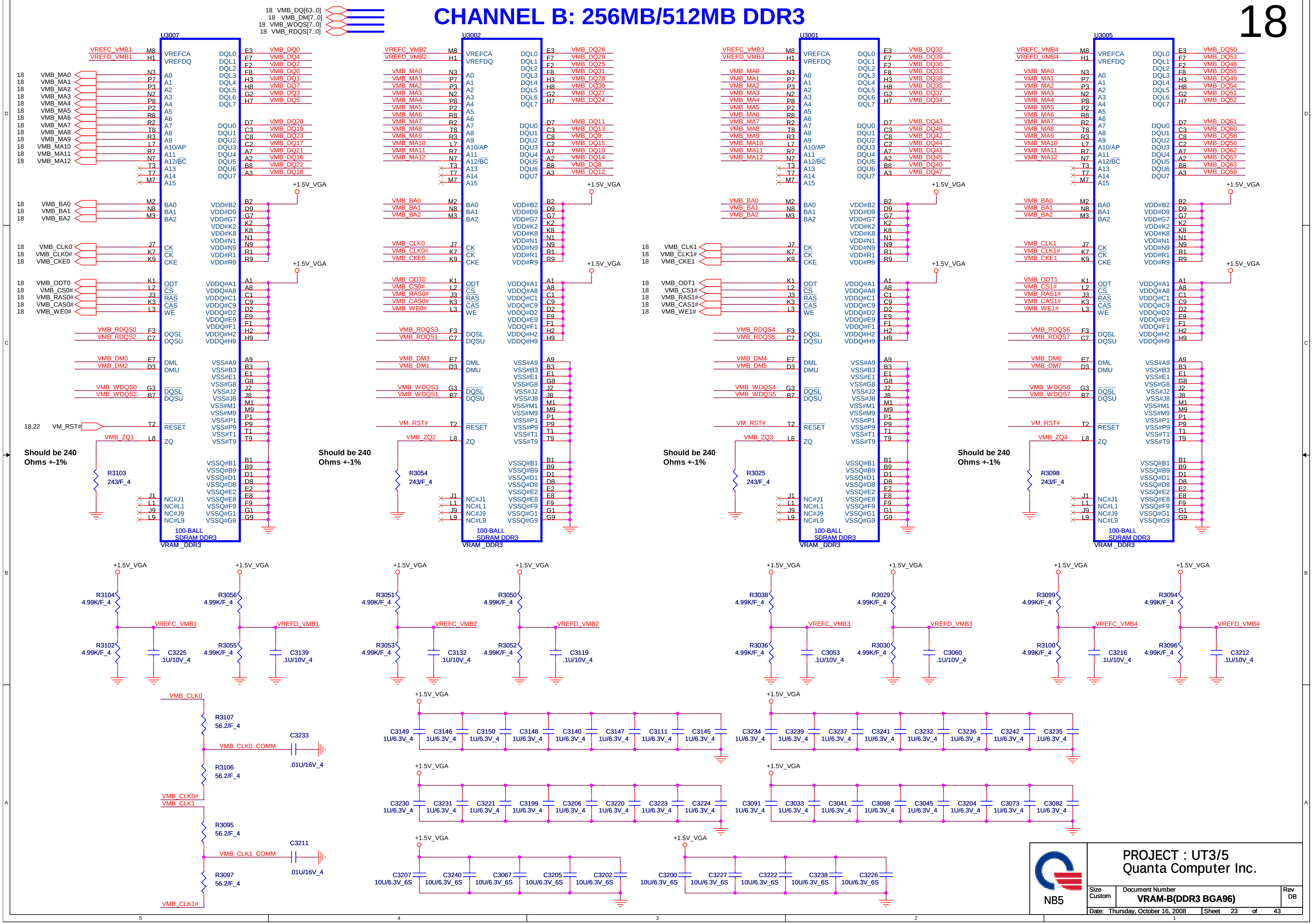
I2C ADDRESS: 9AH

CHANNEL A: 256MB/512MB DDR3



NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: VRAM-A(DDR3 BGA96)	Rev: DB
Date: Thursday, October 16, 2008	Sheet 22 of 43	

CHANNEL B: 256MB/512MB DDR3

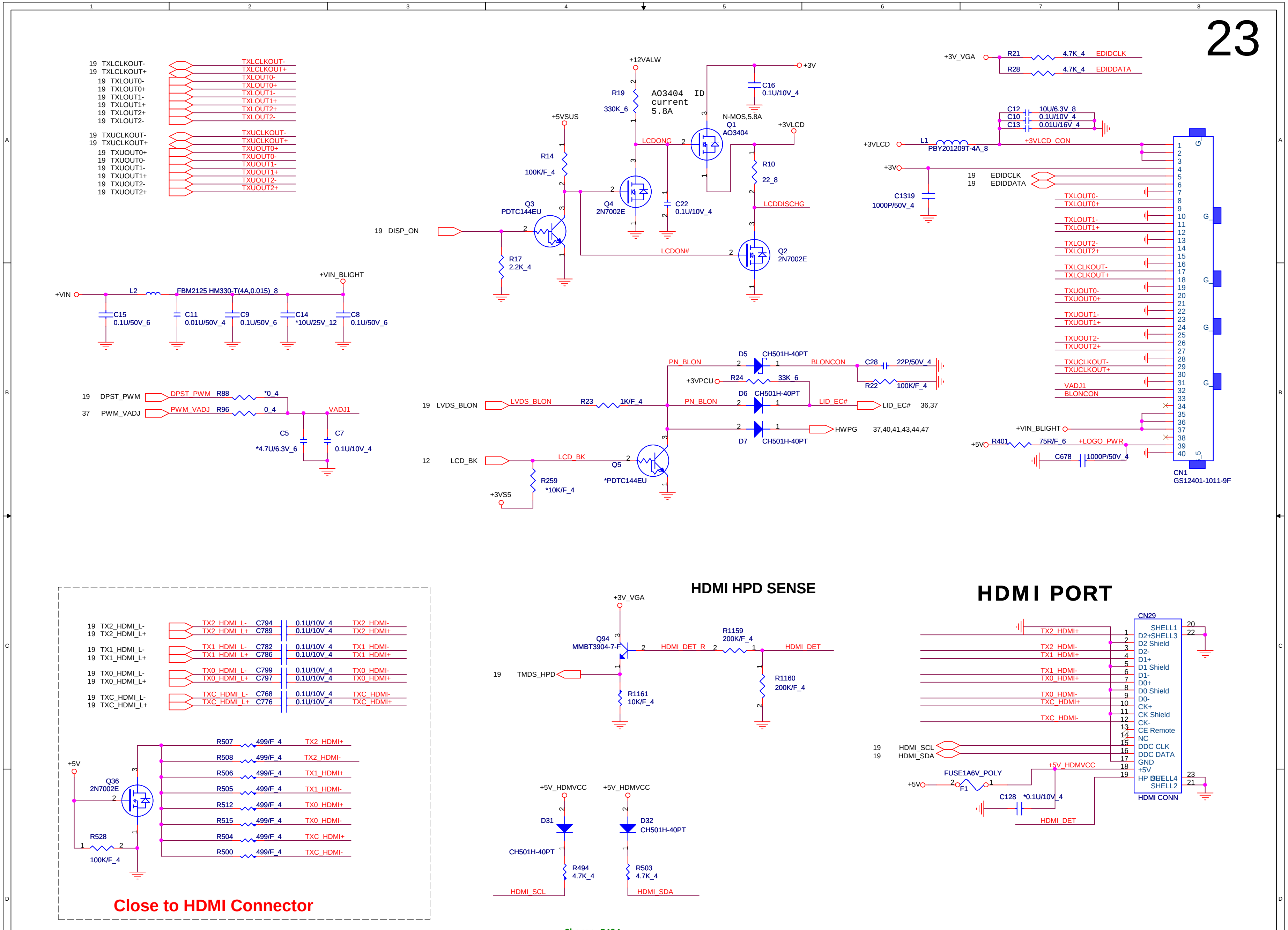


NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B(DDR3 BGA96)	DB

Date: Thursday, October 16, 2008 | Sheet 23 of 43



Change R494,
R503 to 4.7K for
AMD on PV
PV2
DIS use 4.7K
UMA use 2K

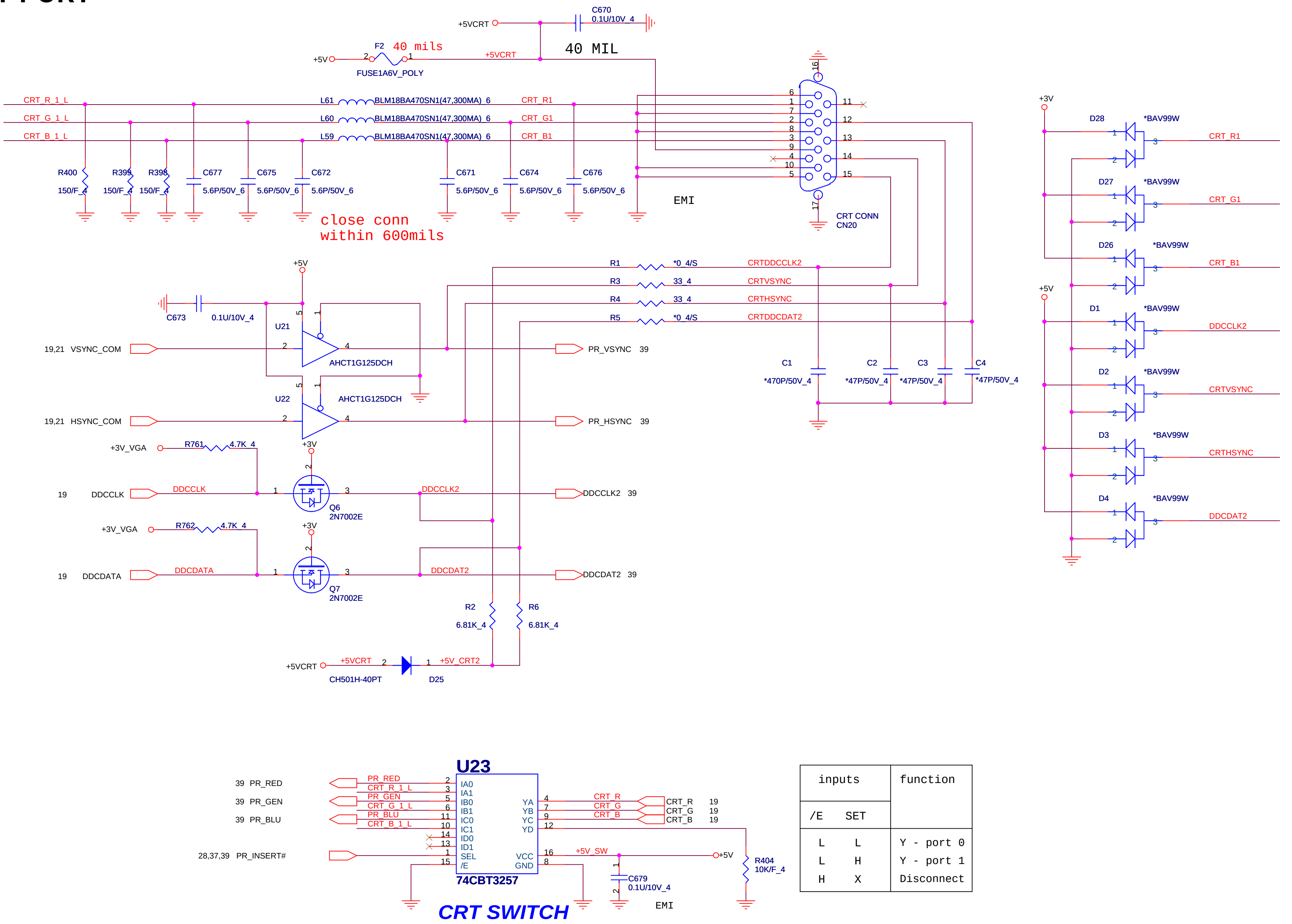
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	LCD CONN,HDMI CONN	1A

Date: Thursday, October 16, 2008 Sheet 24 of 48

CRT PORT



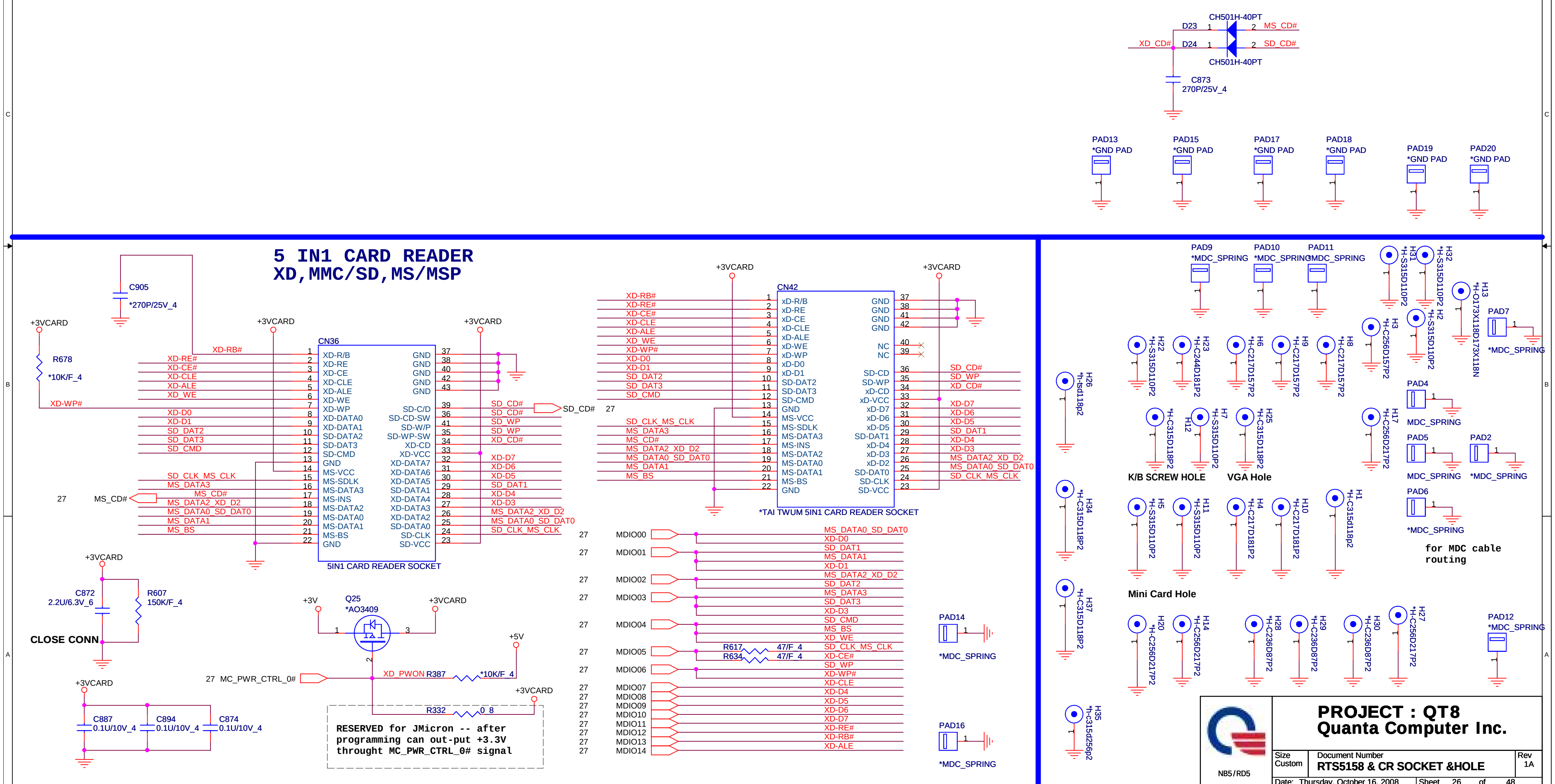
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	CRT	1A

Date: Thursday, October 16, 2008 Sheet 25 of 48

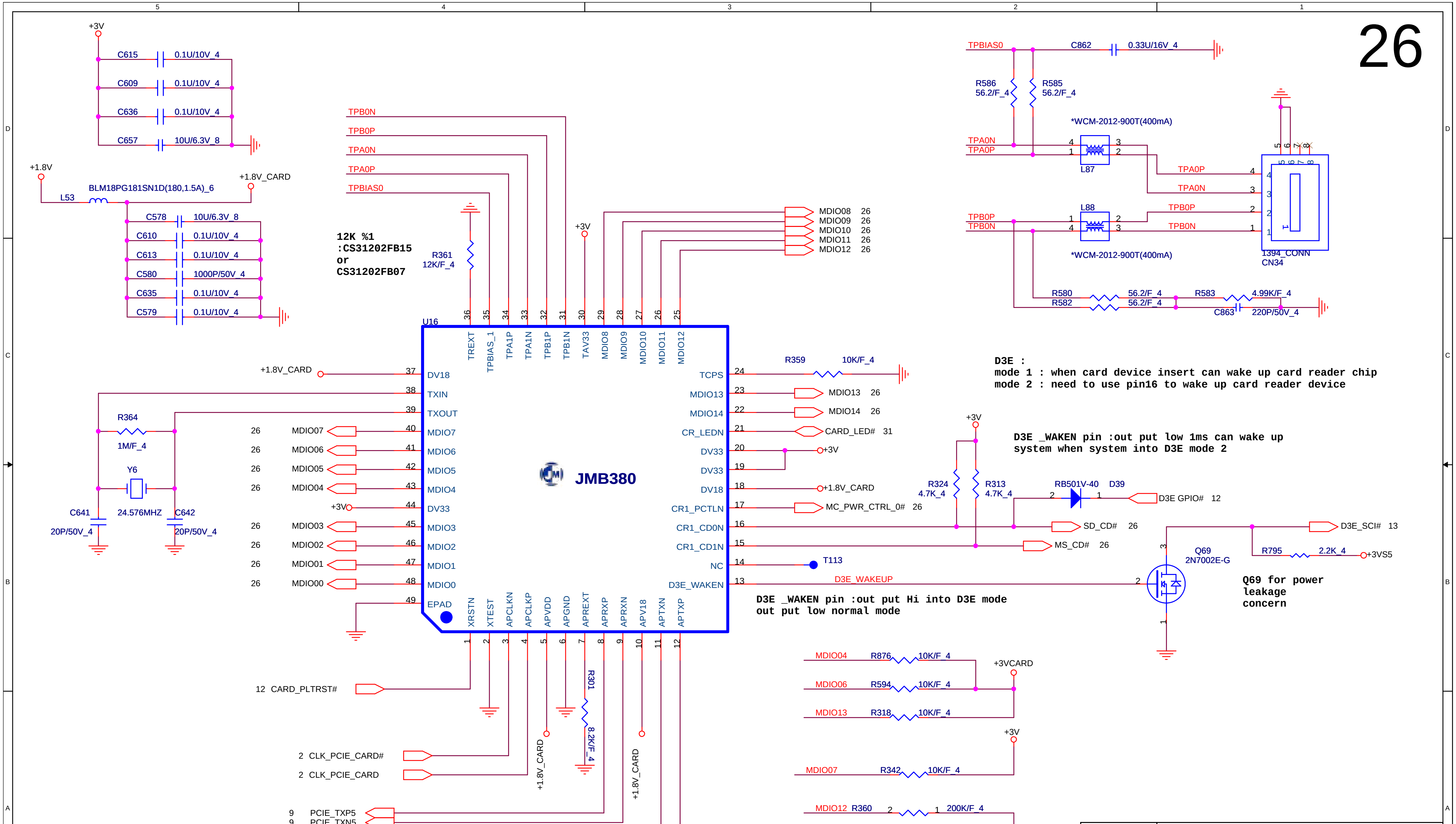


PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

Date: Thursday, October 16, 2008 | Sheet 26 of 48

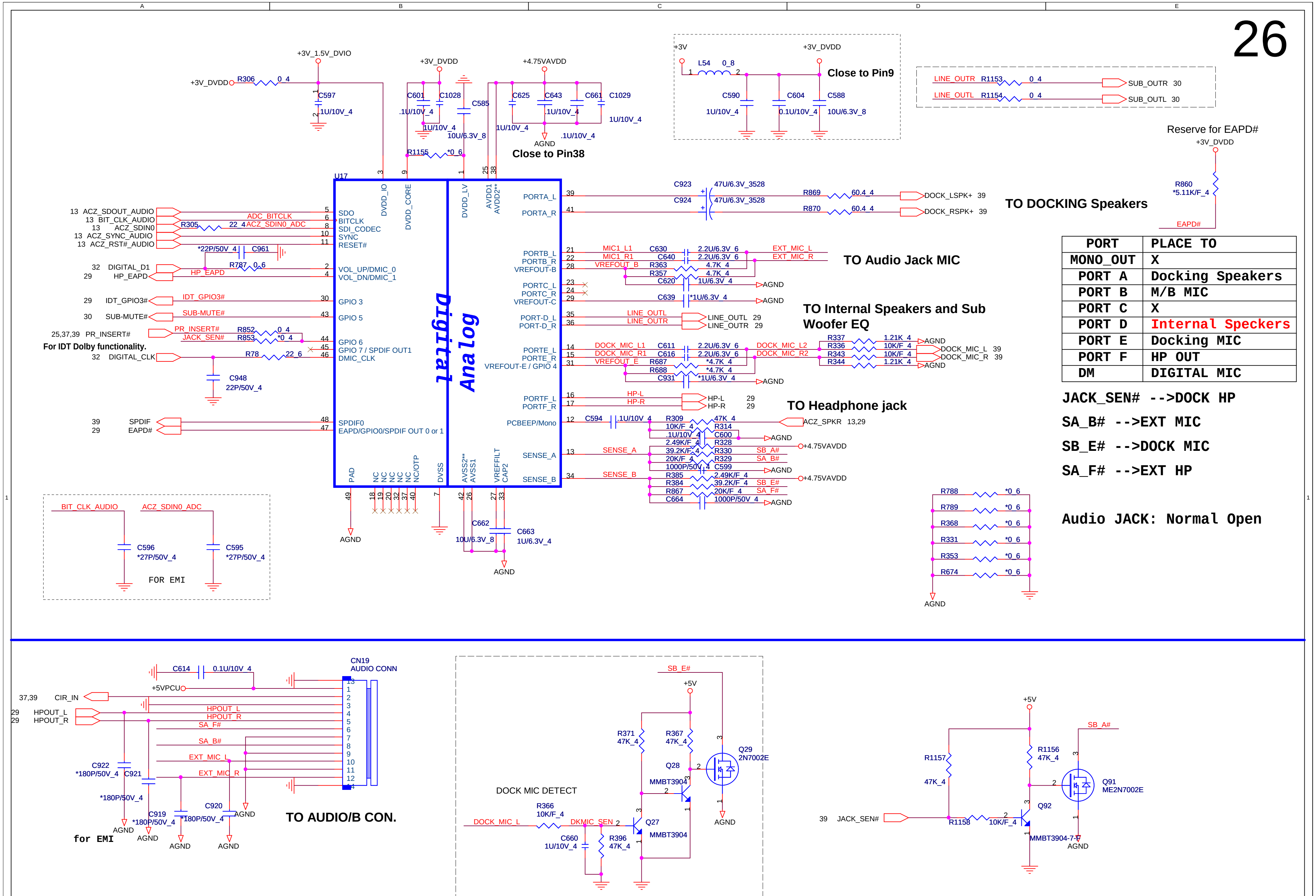


NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	1A

Date: Thursday, October 16, 2008 | Sheet 27 of 48



PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

JACK_SEN# -->DOCK HP

SA_B# -->EXT MIC

SB_E# -->DOCK MIC

SA_F# -->EXT HP

Audio JACK: Normal Open

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

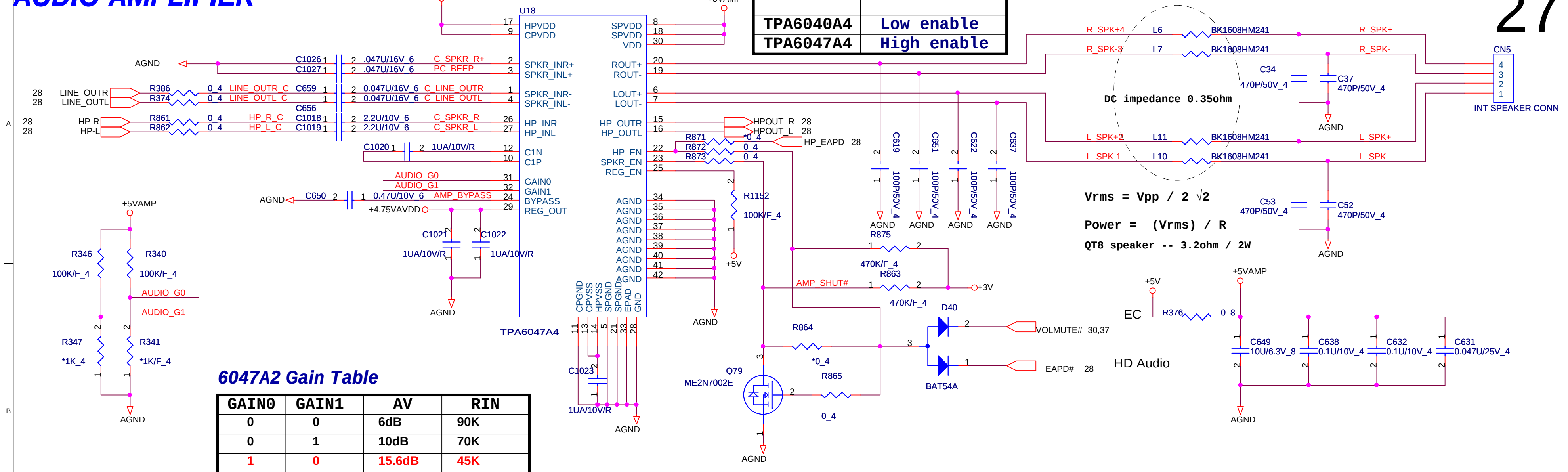
Size	Document Number	Rev
Custom	Azalia AD1883	1A

Date: Thursday, October 16, 2008 Sheet 28 of 48

AUDIO AMPLIFIER

PIN23 SPKR_EN

TPA6040A4	Low enable
TPA6047A4	High enable



DC impedance 0.35ohm

Vrms = Vpp / 2 √2

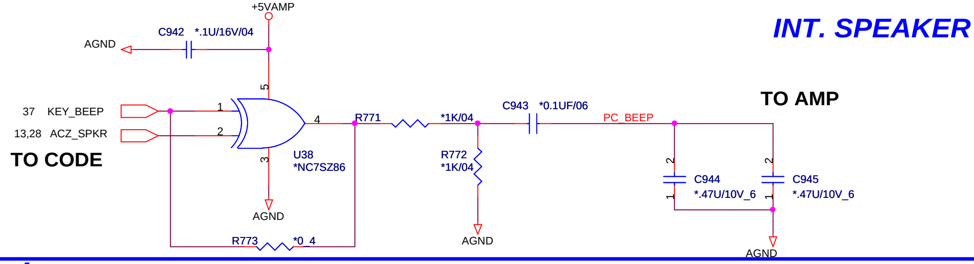
Power = (Vrms) / R

QT8 speaker -- 3.2ohm / 2W

6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

PC-BEEP



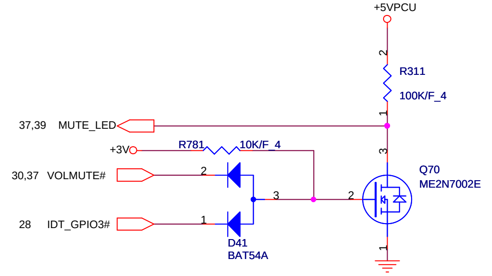
TO CODE

INT. SPEAKER

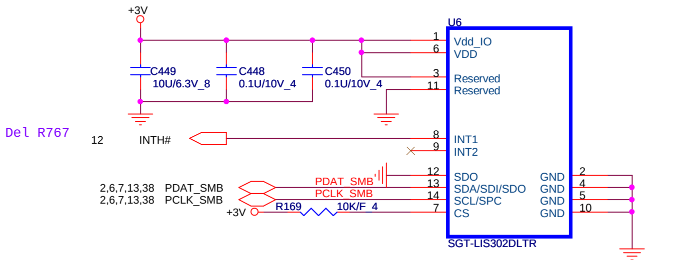
TO AMP

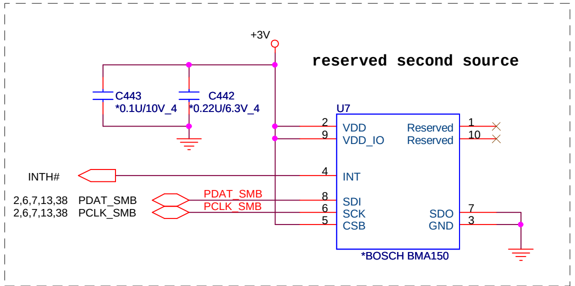
MUTE_LED

Low -->un-MUTE
High-->Mute



Acceleration sensor

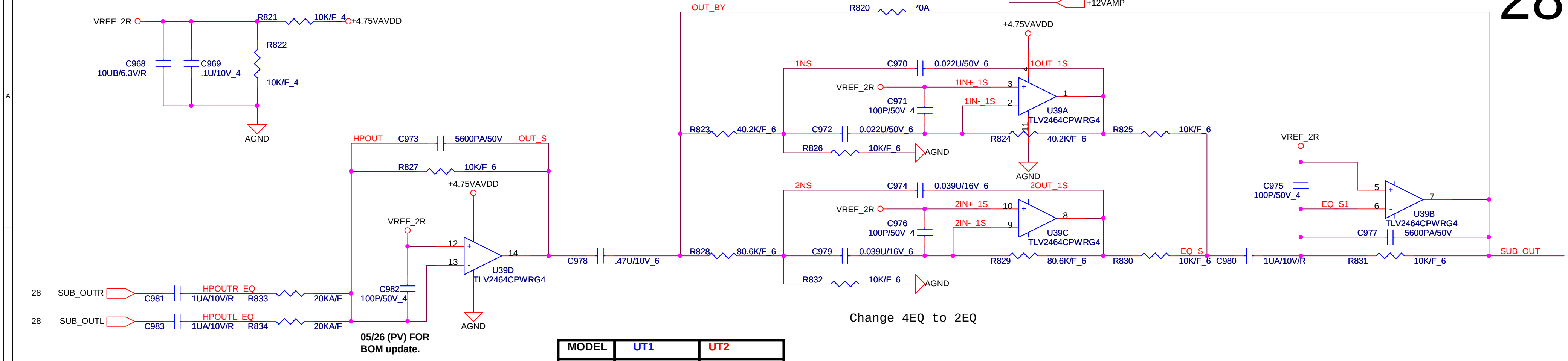




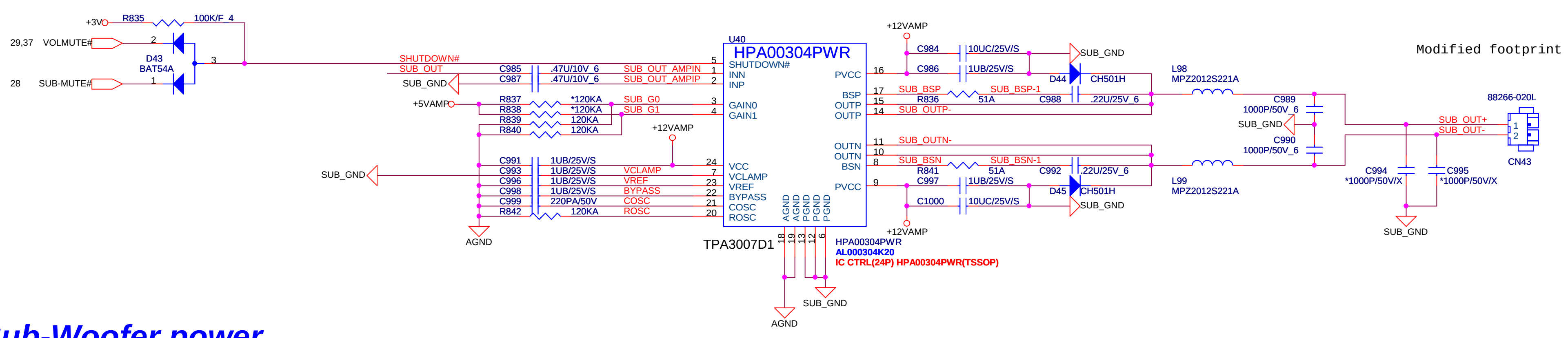
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

EQ FOR SUBWOOFER

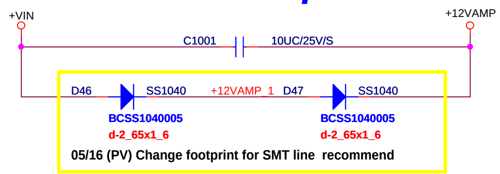
+3V 2,3,5,6,7,10,11,12,13,14,15,16,17,21,24,25,26,27,28,29,31,32,33,35,37,38,39,40,41,45
+5VAMP 29
+4.75VAVDD 28,29
+12VAMP

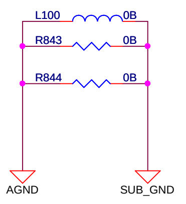


MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C979	0.027U/25V_6	0.039U/16V_6



Sub-Woofer power





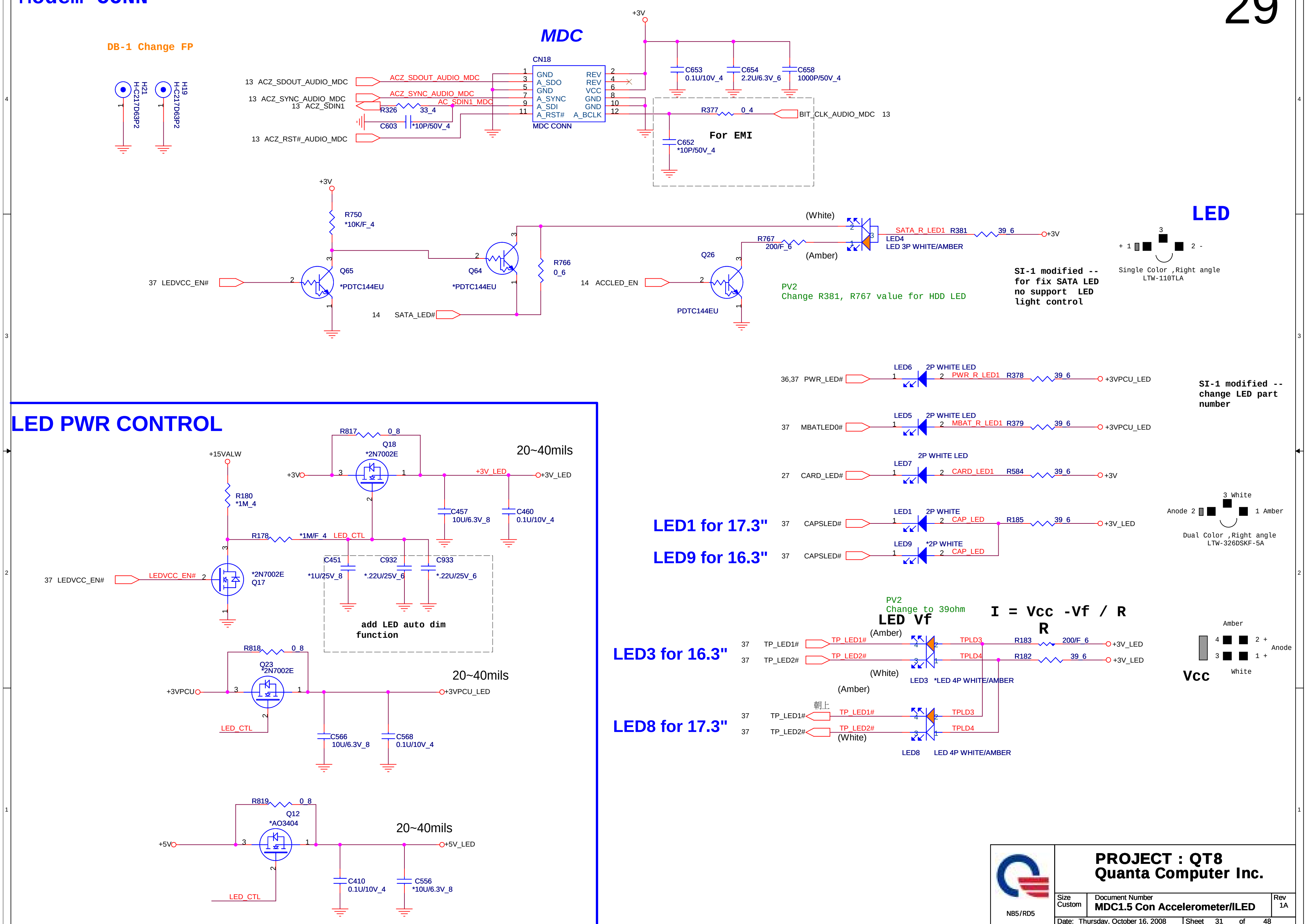
NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	DB

Date: Thursday, October 16, 2008 Sheet 30 of 48

Modem CONN

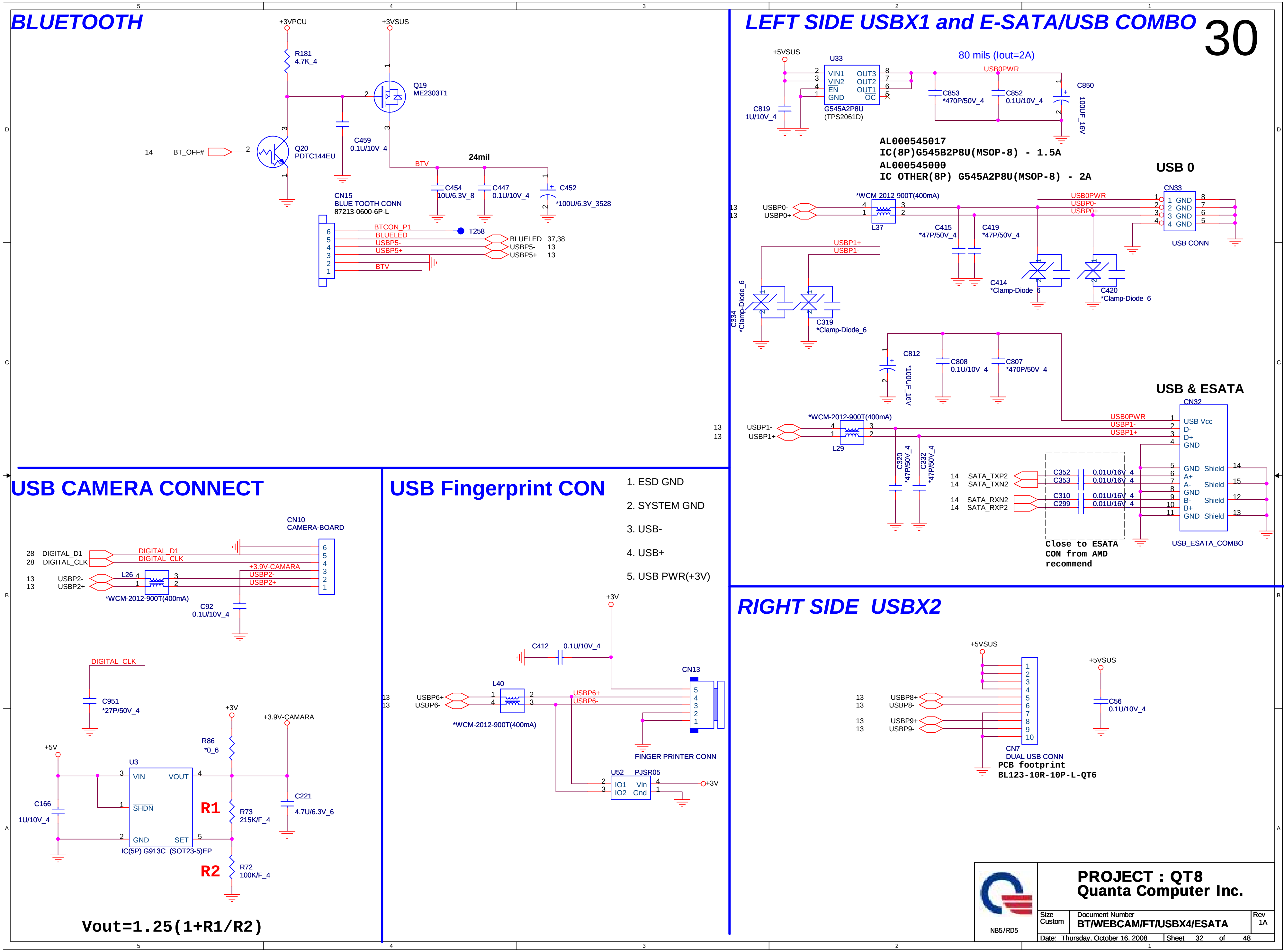


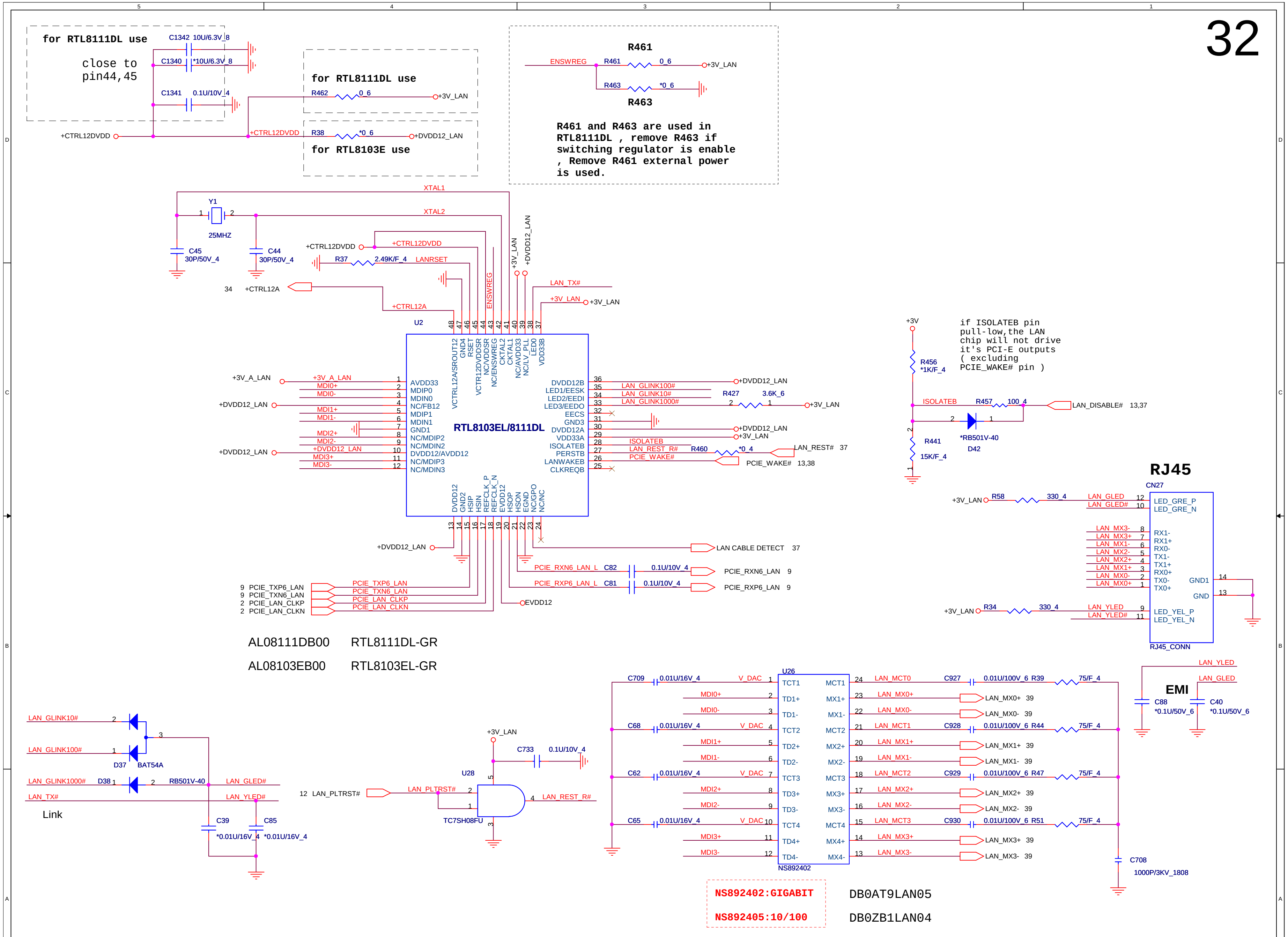
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

Date: Thursday, October 16, 2008 Sheet 31 of 48


BLUETOOTH
+3VPCU
+3VSUS
R181
4.7K_4
Q19
ME2303T1
Q20
PDTC144EU
14 BT_OFF#
C459
0.1U/10V_4
BTV
24mil
C454
10U/6.3V_8
C447
0.1U/10V_4
C452
*100U/6.3V_3528
CN15
BLUE TOOTH CONN
87213-0600-6P-L
BTCON_P1
T258
BLUELED
USBP5-
USBP5+
BLUELED 37,38
USBP5- 13
USBP5+ 13
LEFT SIDE USBX1 and E-SATA/USB COMBO
30
+5VSUS
U33
VIN1 VIN2 EN GND
OUT3 OUT2 OUT1 OC
G545A2P8U
(TPS2061D)
C819
1U/10V_4
80 mils (Iout=2A)
USB0PWR
C853
*470P/50V_4
C852
0.1U/10V_4
C850
100UF_16V
AL000545017
IC(8P)G545B2P8U(MSOP-8) - 1.5A
AL000545000
IC OTHER(8P) G545A2P8U(MSOP-8) - 2A
USB 0
*WCM-2012-900T(400mA)
USBP0-
USBP0+
L37
C415
*47P/50V_4
C419
*47P/50V_4
CN33
USB CONN
USBP1+
USBP1-
C414
*Clamp-Diode_6
C420
*Clamp-Diode_6
C334
*Clamp-Diode_6
C319
*Clamp-Diode_6
C812
*100UF_16V
C808
0.1U/10V_4
C807
*470P/50V_4
USB & ESATA
CN32
USB Vcc
D-
D+
GND
A+
A-
B-
B+
Shield
USBP1-
USBP1+
L29
C320
*47P/50V_4
C332
*47P/50V_4
14 SATA_TXP2
14 SATA_TXN2
14 SATA_RXN2
14 SATA_RXP2
C352
C353
C310
C299
0.01U/16V_4
Close to ESATA
CON from AMD
recommend
USB_ESATA_COMBO
USB CAMERA CONNECT
CN10
CAMERA-BOARD
28 DIGITAL_D1
28 DIGITAL_CLK
13 USBP2-
13 USBP2+
L26
*WCM-2012-900T(400mA)
+3.9V-CAMARA
C92
0.1U/10V_4
DIGITAL_CLK
C951
*27P/50V_4
+5V
C166
1U/10V_4
U3
VIN
VOUT
SHDN
GND
SET
IC(5P) G913C (SOT23-5)EP
+3V
R86
*0_6
R1
R73
215K/F_4
R2
R72
100K/F_4
+3.9V-CAMARA
C221
4.7U/6.3V_6
Vout=1.25(1+R1/R2)
USB Fingerprint CON
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)
+3V
C412
0.1U/10V_4
L40
13 USBP6+
13 USBP6-
*WCM-2012-900T(400mA)
CN13
FINGER PRINTER CONN
U52
PJSR05
IO1 IO2 Vin Gnd
+3V
RIGHT SIDE USBX2
+5VSUS
13 USBP8+
13 USBP8-
13 USBP9+
13 USBP9-
CN7
DUAL USB CONN
PCB footprint
BL123-10R-10P-L-QT6
C56
0.1U/10V_4
NB5/RD5
PROJECT : QT8
Quanta Computer Inc.
Size Custom
Document Number
BT/WEBCAM/FT/USBX4/ESATA
Rev 1A
Date: Thursday, October 16, 2008
Sheet 32 of 48

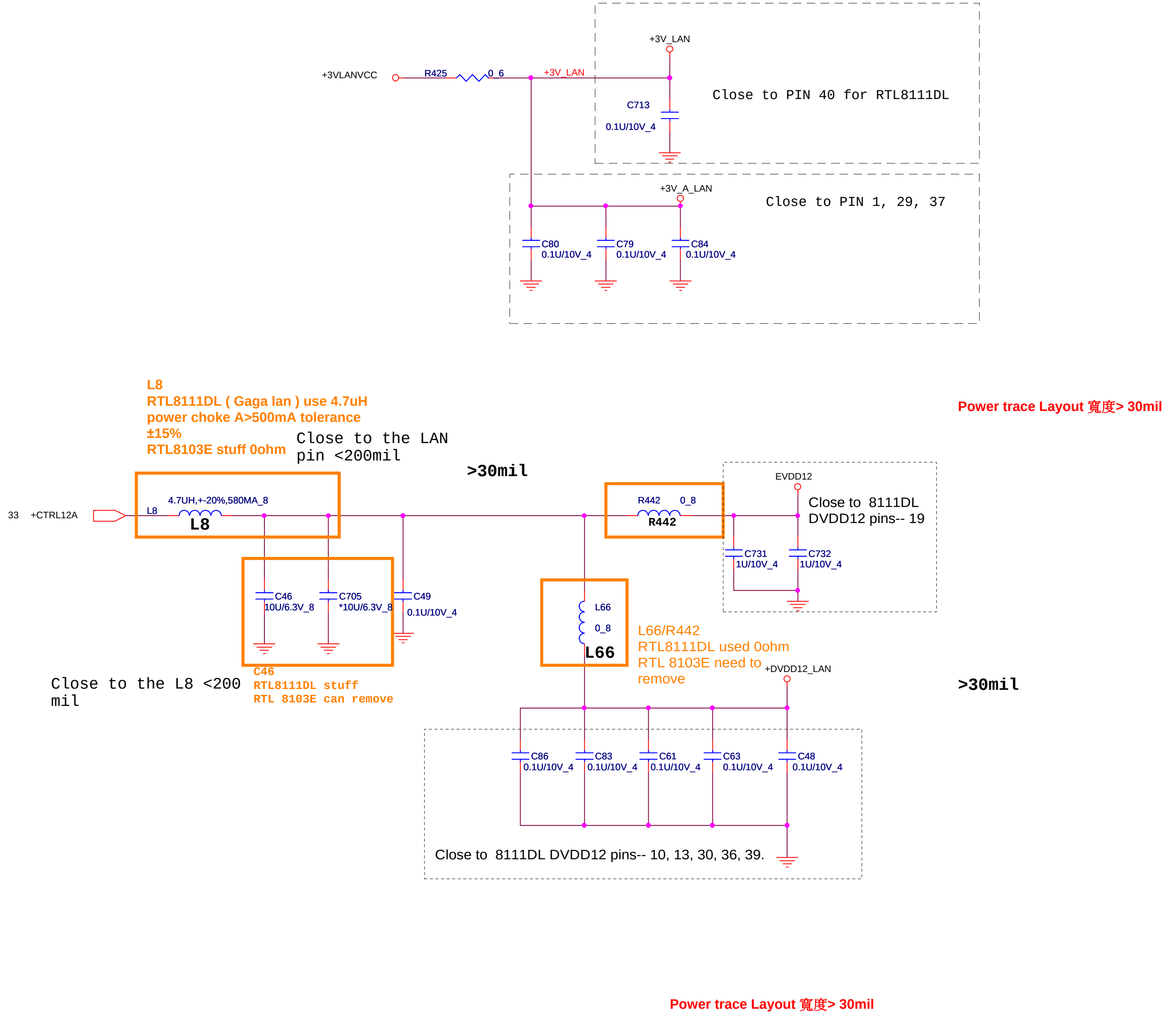


PROJECT : UT12
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ11-RJ45 CN	1A

Date: Thursday, October 16, 2008 | Sheet 33 of 47



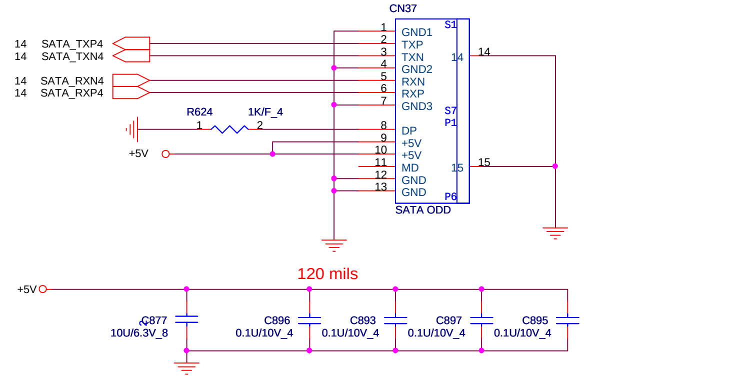
NB5

PROJECT : UT12
Quanta Computer Inc.

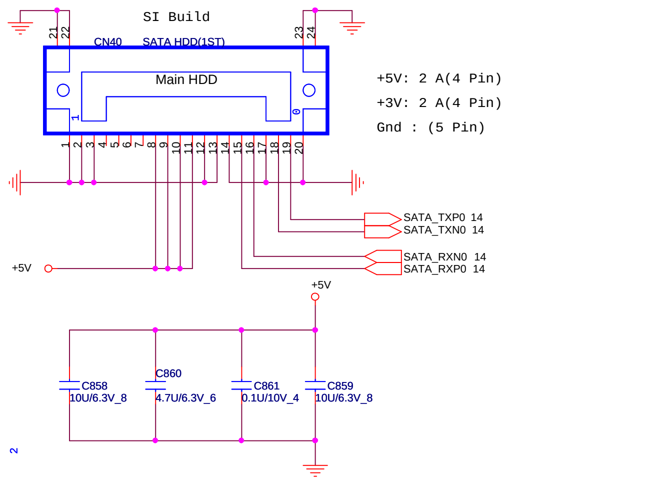
Size	Document Number	Rev
Custom	LAN Power	1A

Date: Thursday, October 16, 2008 | Sheet 34 of 47

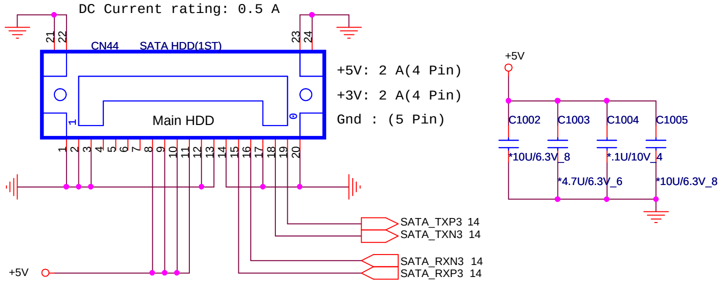
SATA CD-ROM



SATA_1 HDD CONNECTOR

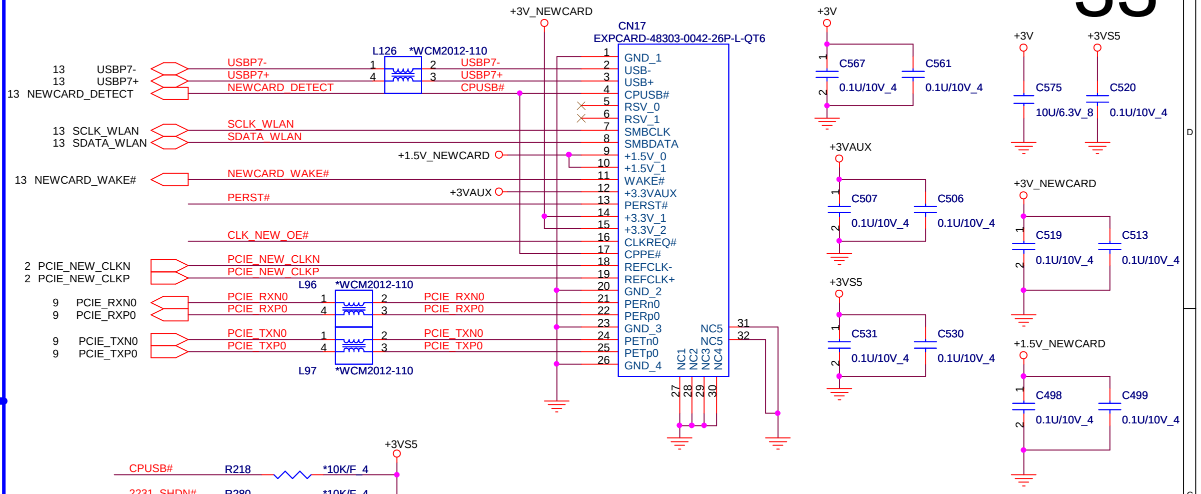


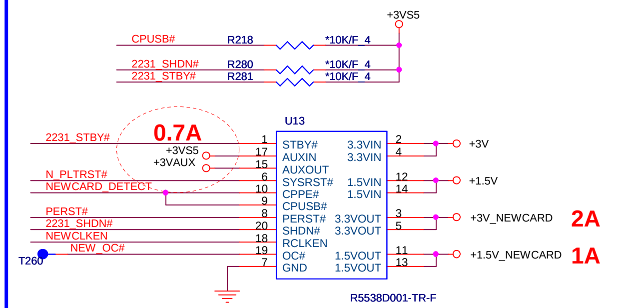
SATA_2 CONNECTOR

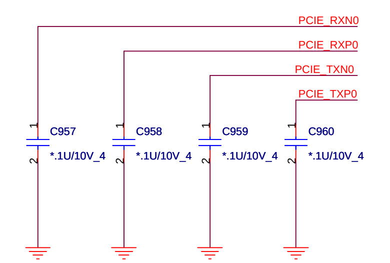


NEWCARD

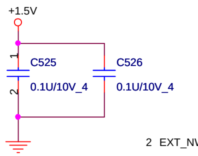
NEWCARD (PCIEXPRESS*1 + USB*1)

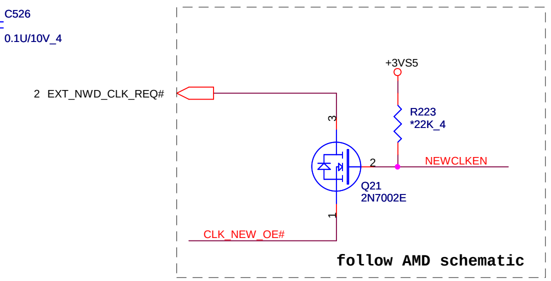


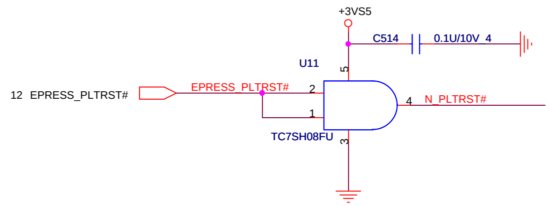




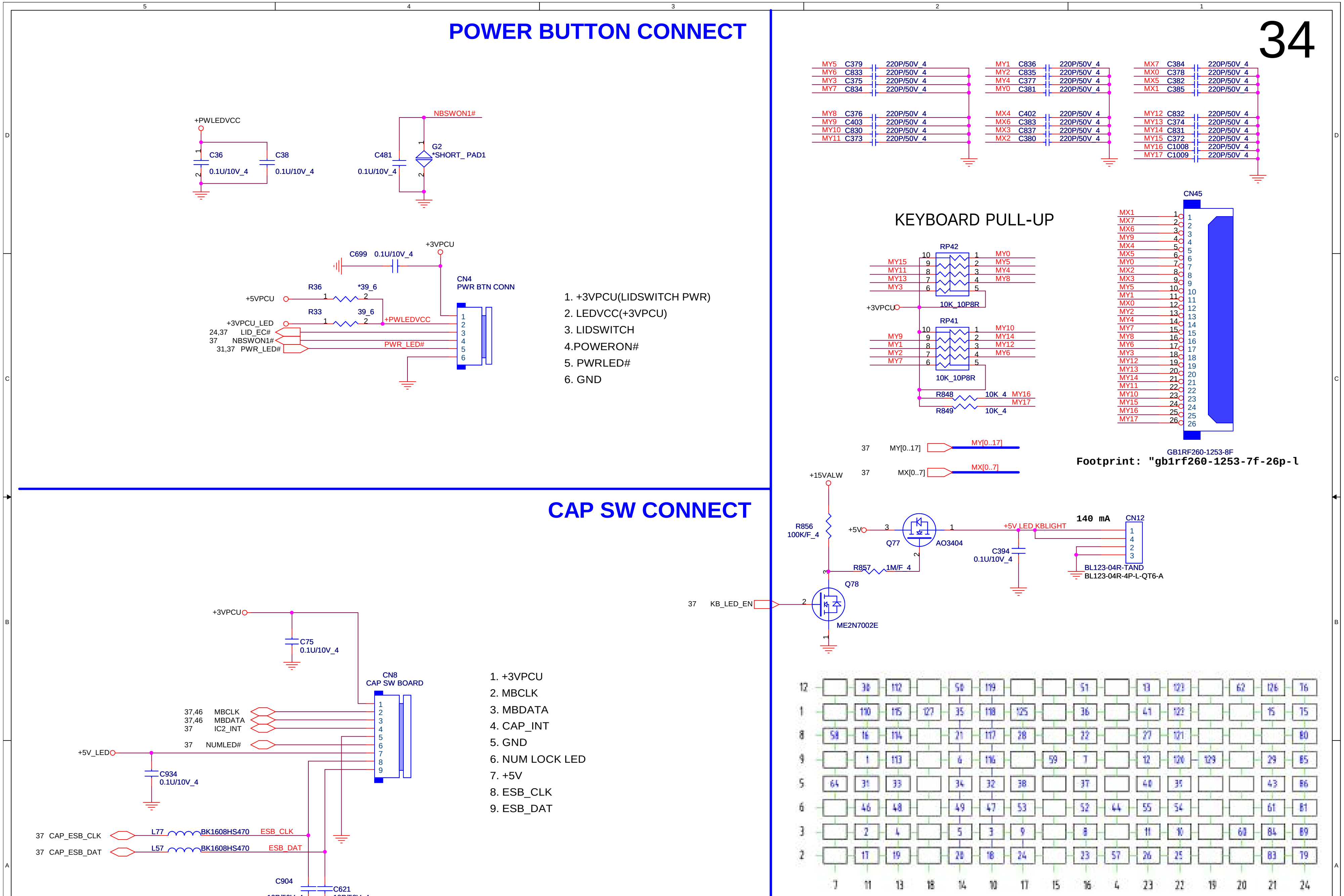
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN





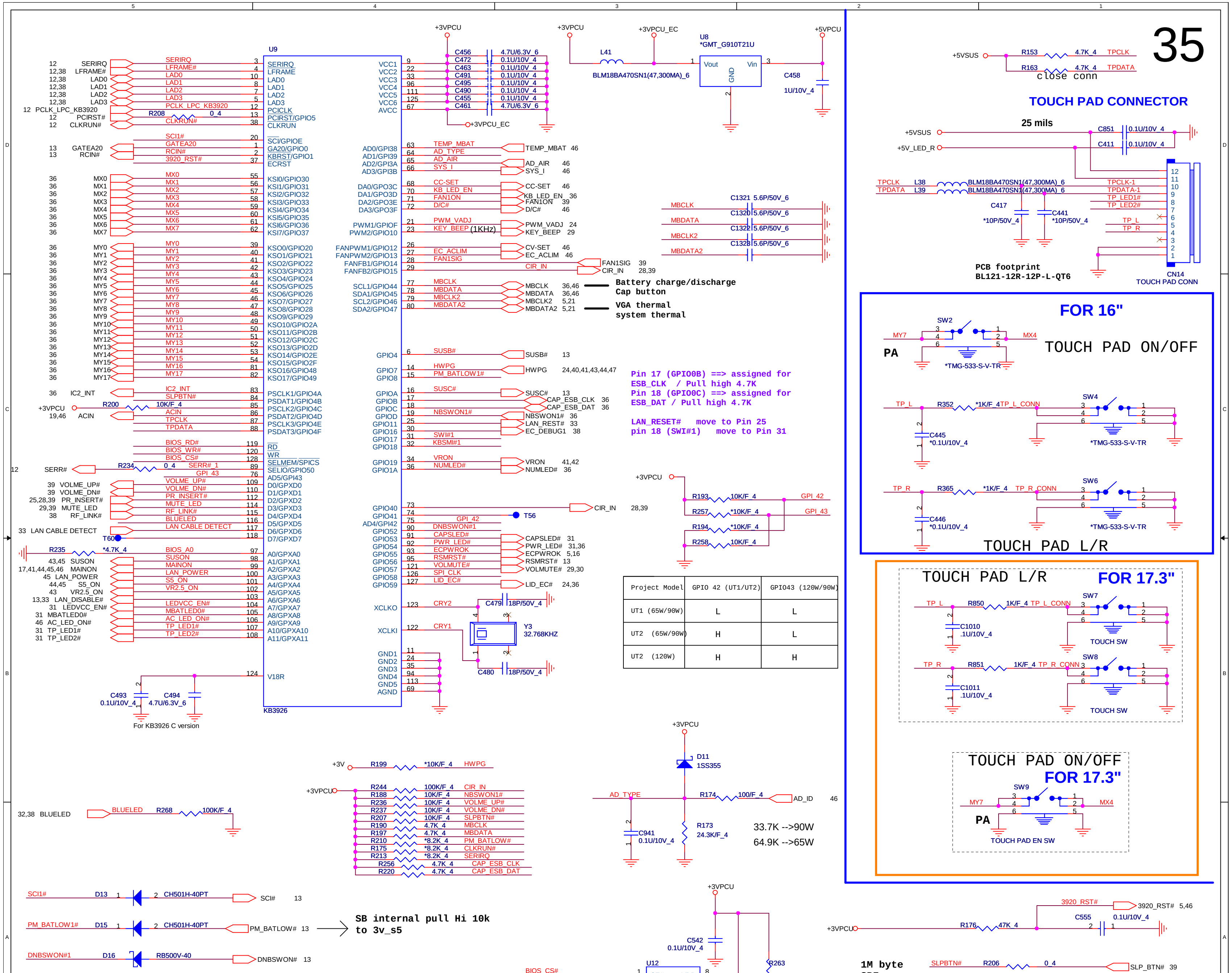


NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: NEW CARD/SATA ODD/SATA HDD	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 35 of 48	



NB5/RD5	**PROJECT : QT8** **Quanta Computer Inc.**
Size: Custom	Document Number: LED/KEYBOARD/SW — Rev 1A
Date: Thursday, October 16, 2008	Sheet 36 of 48

35



Project Model	GPIO 42 (UT1/UT2)	GPIO43 (120W/90W)
UT1 (65W/90W)	L	L
UT2 (65W/90W)	H	L
UT2 (120W)	H	H

SST AKE5GFK0Z09
WINBOND AKE3GFP0N08
PME AKE3GZP0500
EON AKE3GZP0Q00

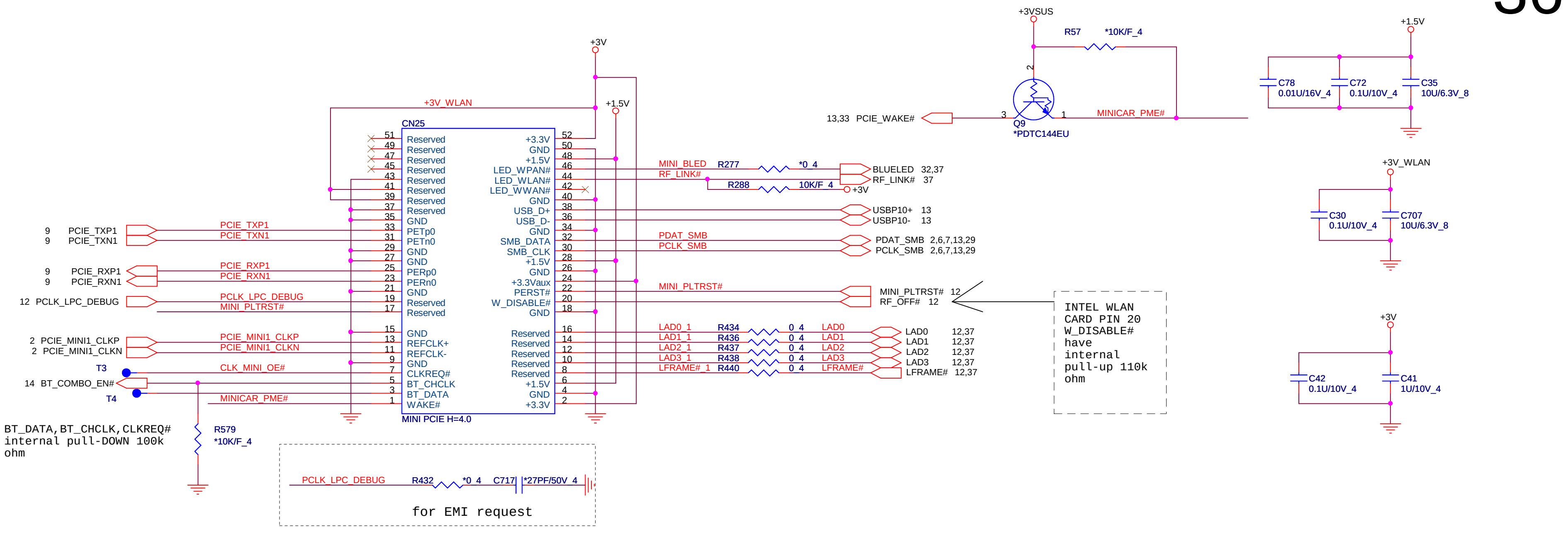
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

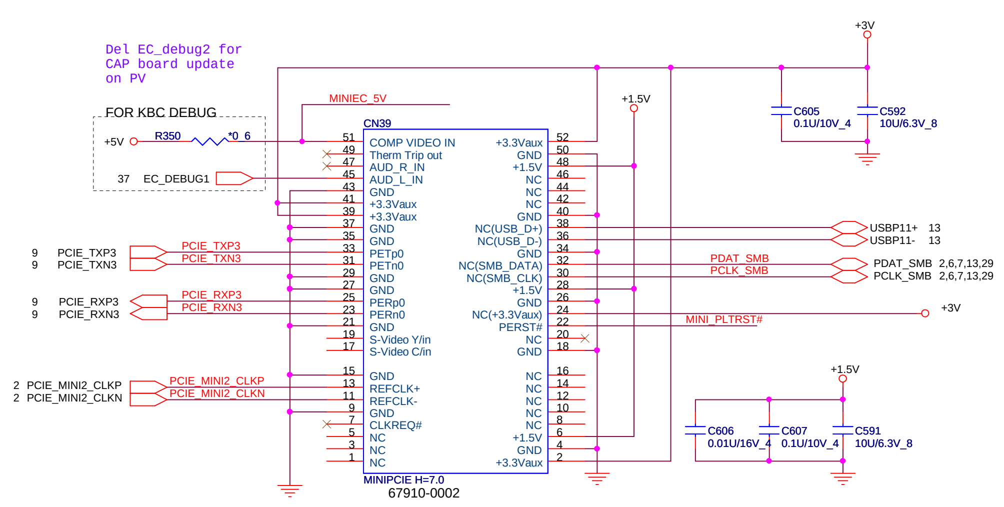
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Thursday, October 16, 2008 Sheet 37 of 48

Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 TV tuner card



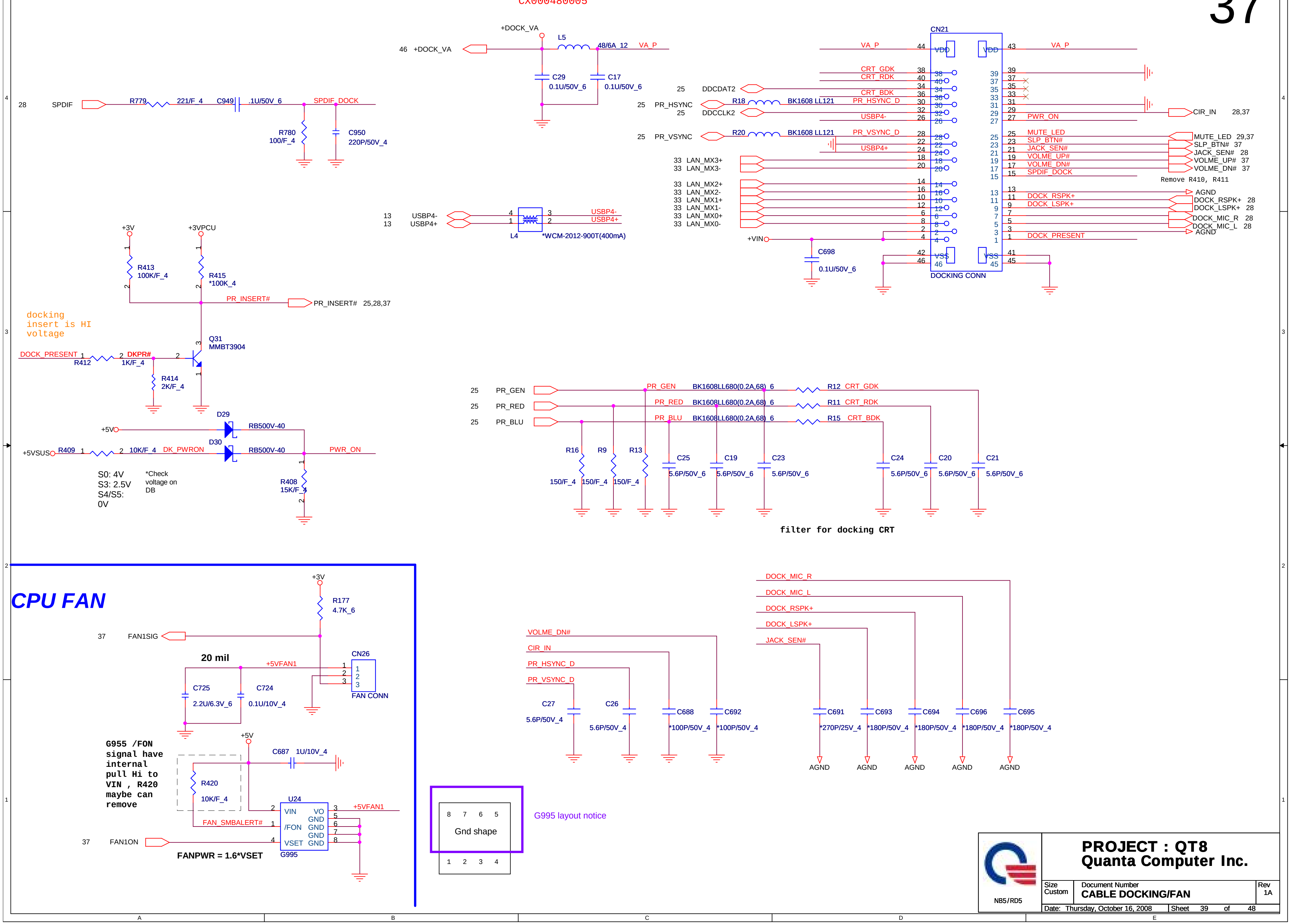
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	Mini CARD X 3	1A

Date: Thursday, October 16, 2008 Sheet 38 of 48

CABLE DOCK



CPU FAN

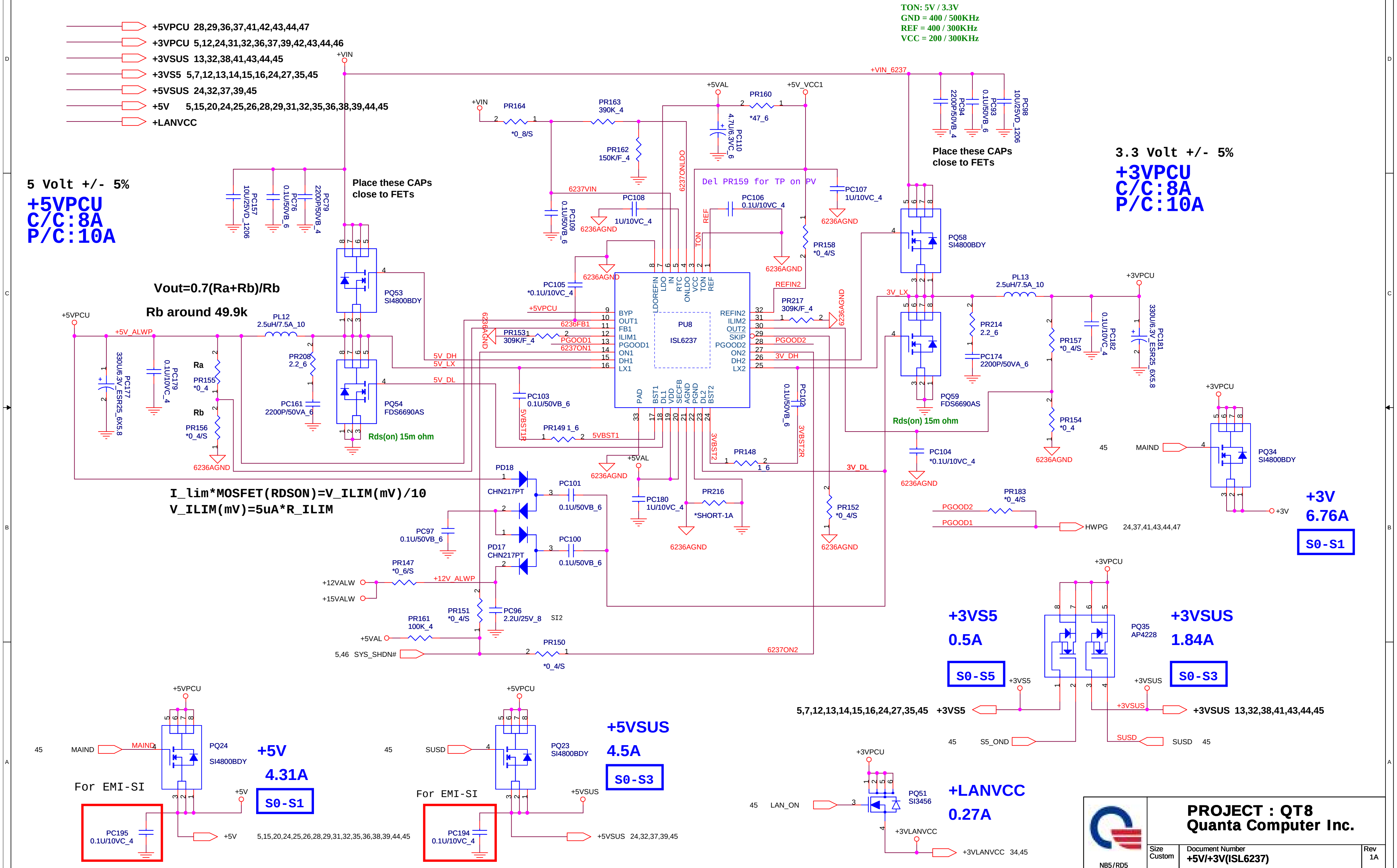
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

Date: Thursday, October 16, 2008 Sheet 39 of 48

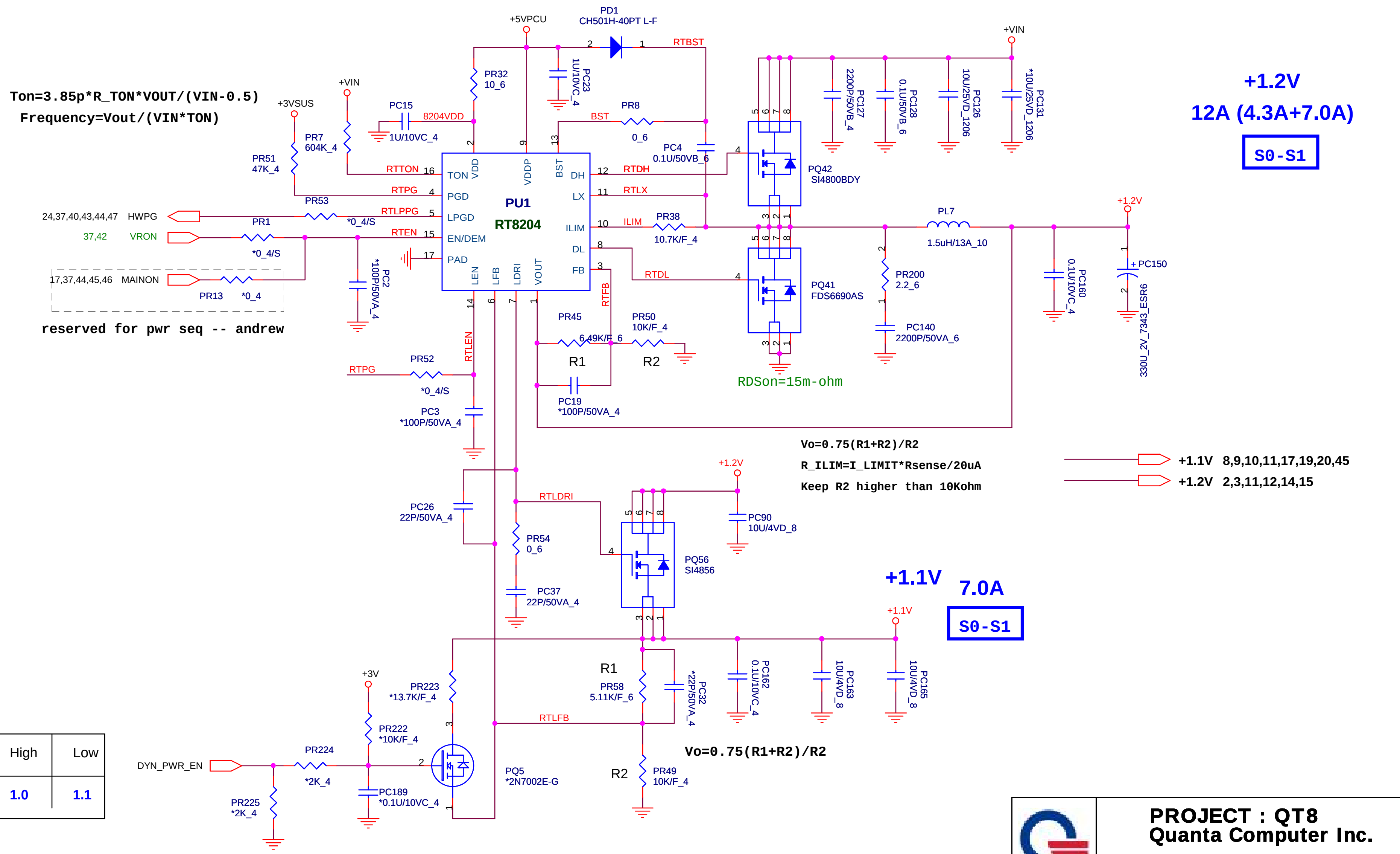
DC/DC +3VPCU/+ 5VPCU/ +12VALW



PROJECT : QT8		
Quanta Computer Inc.		
Size: Custom	Document Number: +5V/+3V(ISL6237)	Rev: 1A
Date: Thursday, October 16, 2008	Sheet 40 of 48	

NB5/RD5

+1.1V & +1.2V



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

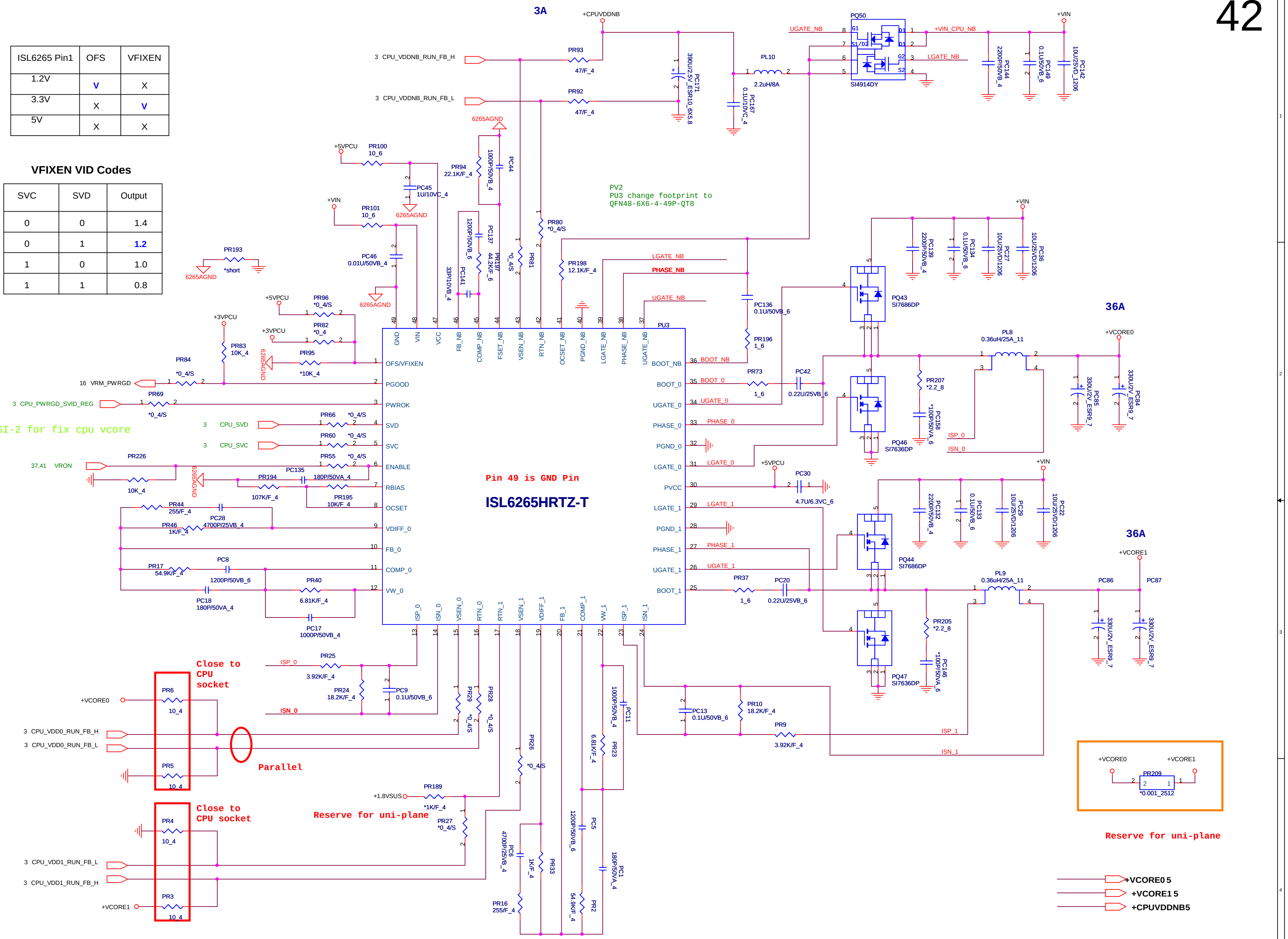
Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	1A

Date: Thursday, October 16, 2008 | Sheet 41 of 48

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

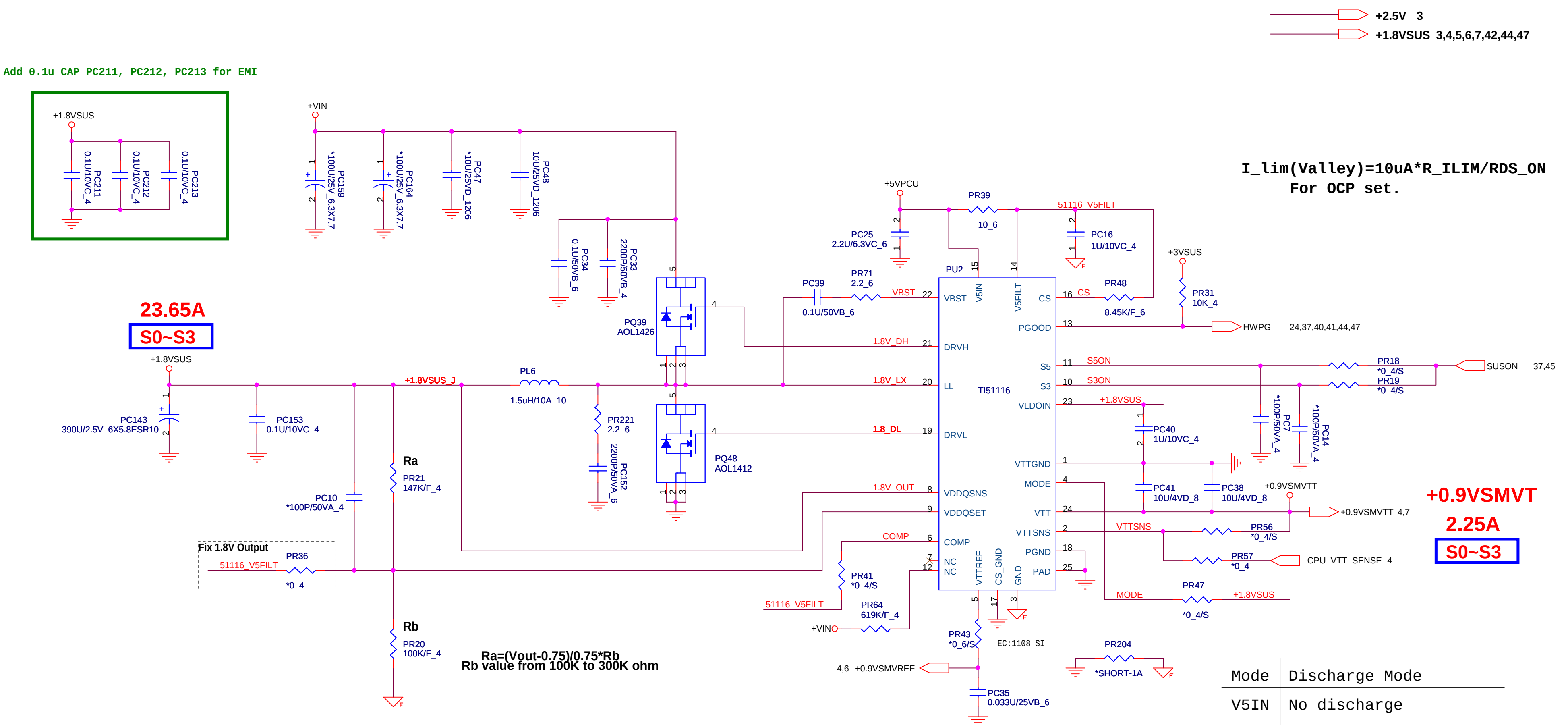


PROJECT : QT8 Quanta Computer Inc.			
Size C	Document Number CPU_CORE(ISL6265)		Rev 1A
Date: Thursday, October 16, 2008		Sheet 42 of 48	

NB5/RD5

Add 0.1u CAP PC211, PC212, PC213 for EMI

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

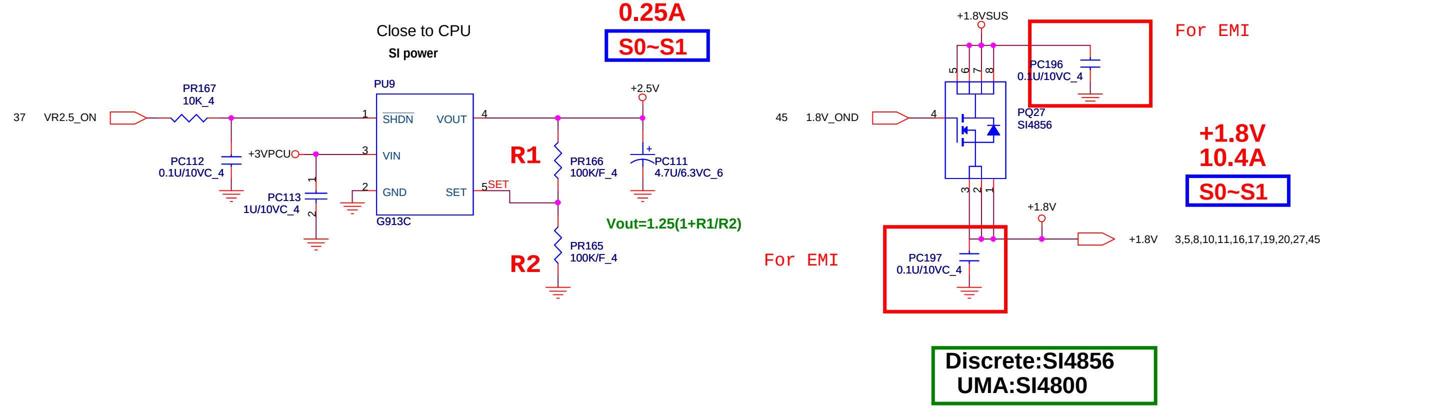


Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V



Discrete:SI4856
UMA:SI4800

PROJECT : QT8
Quanta Computer Inc.

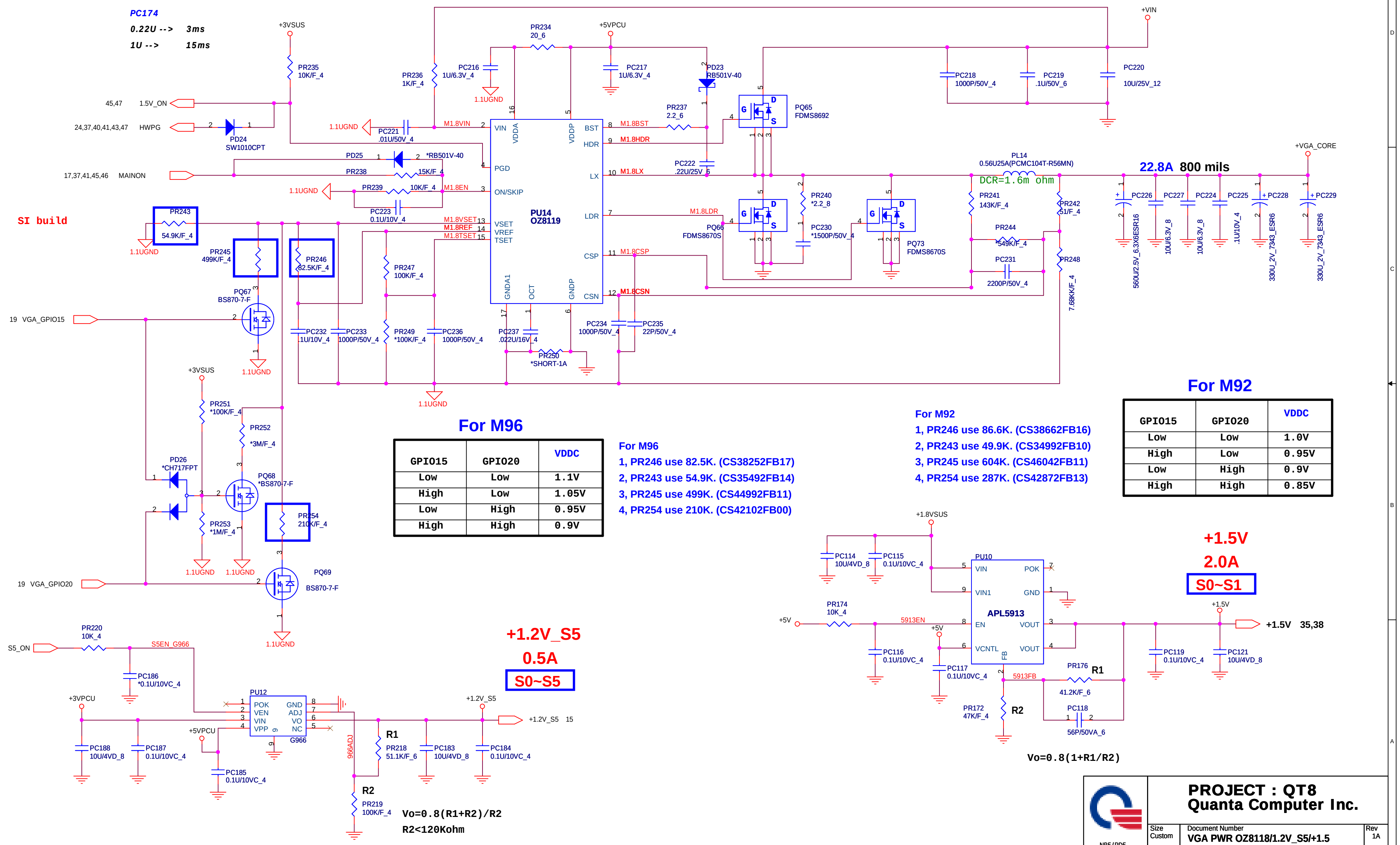
NB5/RD5

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A

Date: Thursday, October 16, 2008 | Sheet 43 of 48

VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



For M96

GPIO15	GPIO20	VDDC
Low	Low	1.1V
High	Low	1.05V
Low	High	0.95V
High	High	0.9V

For M96
1, PR246 use 82.5K. (CS38252FB17)
2, PR243 use 54.9K. (CS35492FB14)
3, PR245 use 499K. (CS44992FB11)
4, PR254 use 210K. (CS42102FB00)

For M92
1, PR246 use 86.6K. (CS38662FB16)
2, PR243 use 49.9K. (CS34992FB10)
3, PR245 use 604K. (CS46042FB11)
4, PR254 use 287K. (CS42872FB13)

For M92

GPIO15	GPIO20	VDDC
Low	Low	1.0V
High	Low	0.95V
Low	High	0.9V
High	High	0.85V

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	VGA PWR OZ8118/1.2V_S5/+1.5	1A

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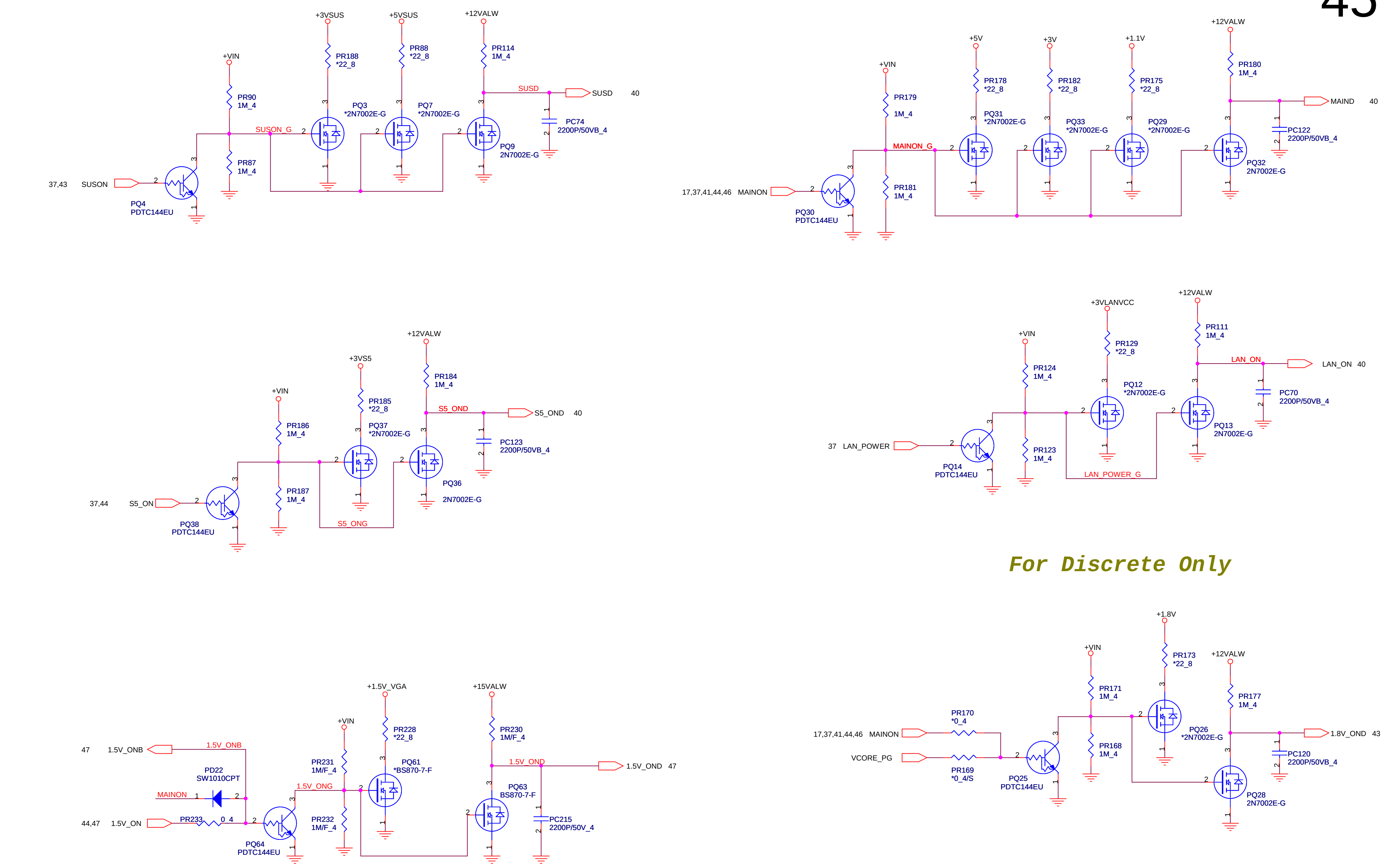
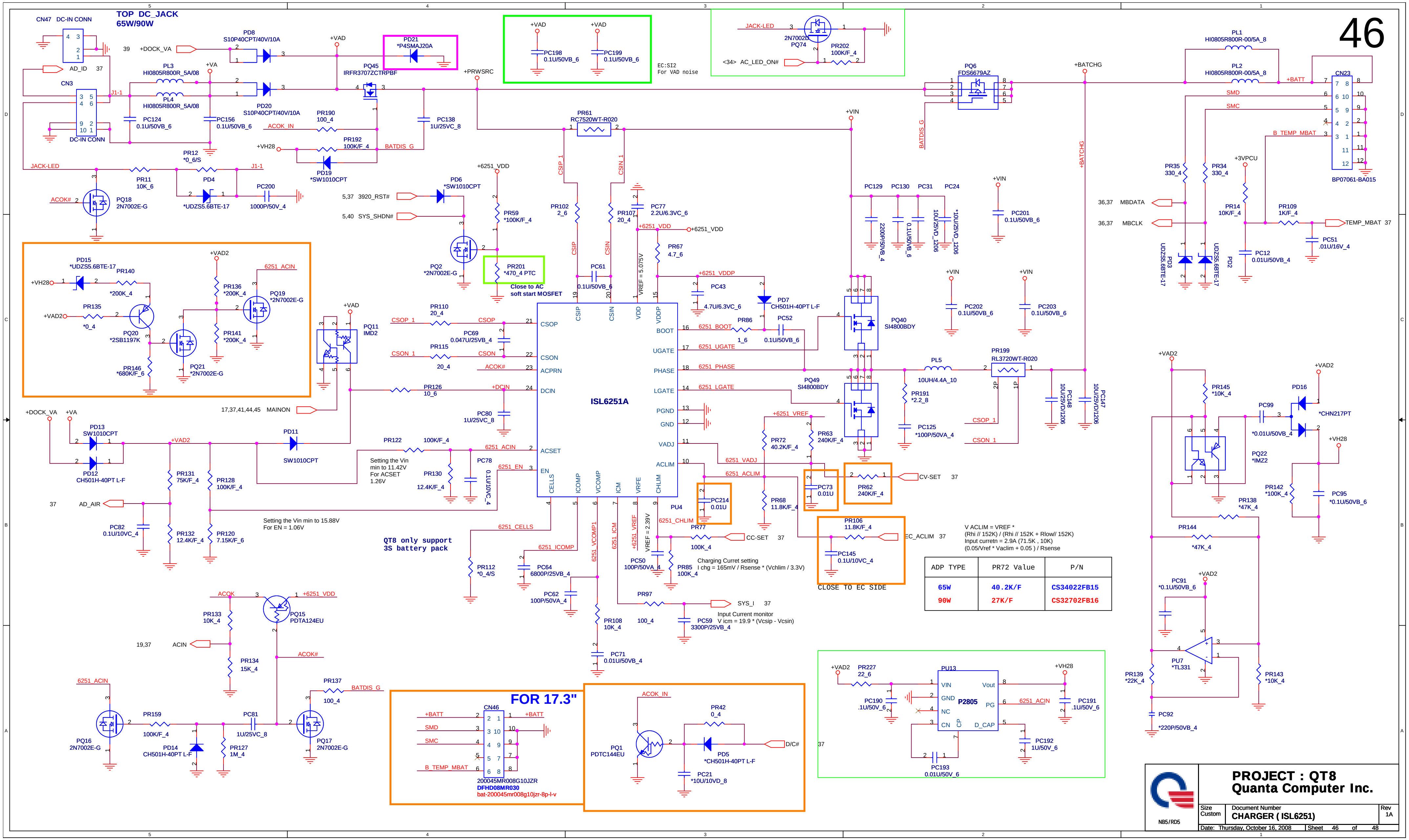


NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	1A

Date: Thursday, October 16, 2008 Sheet 45 of 48



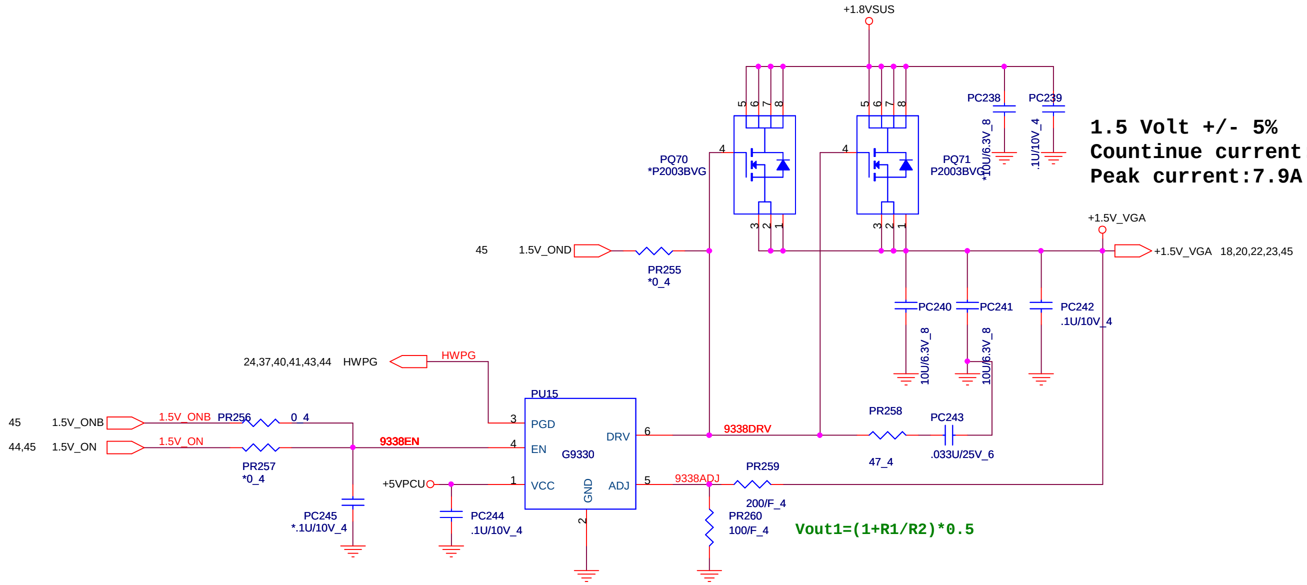
ADP TYPE	PR72 Value	P/N
65W	40.2K/F	CS34022FB15
90W	27K/F	CS32702FB16

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251)	1A

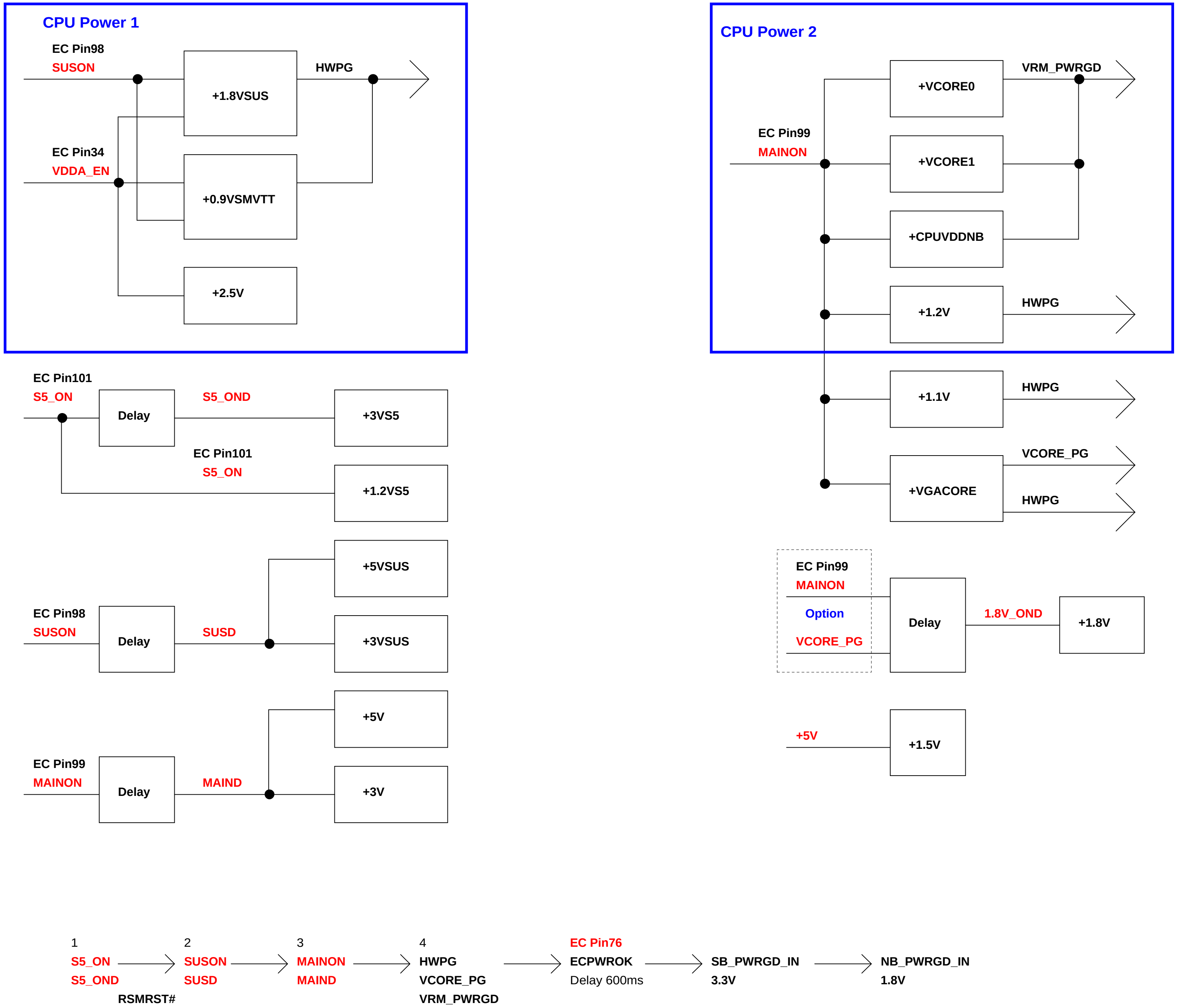
NB5/RD5

Date: Thursday, October 16, 2008 Sheet 46 of 48



1.5 Volt +/- 5%
Countinue current:4A
Peak current:7.9A

VRAM	Mounted	N/A	PQ33 P/N
Others	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	PR232	BAM44960000
Samsung	PR232	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	BAM48560029



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

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