Model Name: B460 HD3

REV: 1.01

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1200-A
05	CPU_LGA1200-B-DDR4
06	CPU_LGA1200-C
07	CPU_LGA1200-D + Hearsink
08	DDR4 CHANNEL A
09	DDR4 CHANNEL B
10	PCH_CLK BUFFER
11	PCH_DMI,USB,PCIE
12	PCH_MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR
15	PCH GND
16	ITE 8688 LPC IO
17	HWM
18	FAN CTRL--SIO
19	DUAL BIOS
20	CEC Logic
21	PCI EXPRESS*16 SLOT
22	PCI EXPRESS*4 SLOT
23	PCI EXPRESS*1 SLOT
24	SATA 3
25	M.2 X4 (A)
26	M.2 X4 (Q)
27	ISL95866 PWM-IRON
28	ISL95866 VCORE-IRON
29	ISL95866 VCCGT-IRON
30	VCCSA_VCCIO_VCCPLL

SHEET	TITLE
31	RT8237_DDR_BEAD
32	RT8068A_VPP
33	RT8237_PCH-BEAD
34	DISCRETE POWER
35	NCT3933
36	ATX POWER , A_-PROCHOT
37	KB_MS_USB
38	DP HDMI CONN
39	DVI CONN
40	USB3.2 TYPE A + C
41	Blank
42	INTEL I219V
43	USB30_LAN CONNECTOR-I219V
44	Realtek ALC1200
45	REAR AUDIO JACK
46	IT5702
47	DEBUG LED + AMBENT LED
48	FRONT_USB32
49	REAR CONN USB3.2
50	F_PANEL
51	COM, LPT, TPM
52	M.2 WIFI
53	GENESYS GL850S_1
54	EMI-ESD
55	POWER MAP
56	NTC MAP
57	DLED STRIP
58	SM BUS SWITCH
59	

GIGABYTE Technology

Title: Cover Sheet

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Model Name: B460 HD3

Rev 1.01
2020/03/18

TIP/TOP: 9MA32MS2H-00-11C
P-Code: U17132

Component value change history

Data	Change Item	Reason
2019/10/24	0.1 New BOM release PCB:0.1	Modify from B365 M AORUS Elitte
2020/02/11	0.2 E-BOM release PCB:0.2	1. FIX TPM CS PIN. 2. FIX SMBUS 3. DDR SLOT RESERVE IRON BOX FOOTPRINT. BOM GRAY_BLACK CHECK. 4. UPDATE M_2Q_SB BOM. 5. X16, X4 SLOT USE GRAY_BLACK BOM. CHECK 6. ADD N_GPP_F12 FOR PWM PATCH. 7. MODIFY Z490 UD R1.01 DDR layout 8. USB7 TX/RX CHANGE 9. DDR7 NA (LPT ISSUE)
2020/03/02	1.0 D-BOM release PCB:1.0	1. Add NQ8/NR21/NR22 (P.12) 2. 修改 CPU VCCSFR_OC & VCCSTG P & VCCFPGM* 的POWER 來源(P.6/P.30)) 3. LAPW1 3VDUAL-->3VDUAL_PCH 4. Note24 (WR112-->VCCSTG,ADD WR26,WR25 NA,NRN&NR70-->VCCSTG,N_PCH_TDO-->NR70) 5. P9-P12 M.2 support SATA Mode,SATA Detect pin 必須改為GPP_E0 6. SATA 文字面修改 7. NBC11 , NBC28 上件(for USB SSC measure) 8. remove BIOS socket 9. Location : NR34 200K-->1M
2020/03/13	1.0 P-BOM release PCB:1.01	1.ADD DDR14.DGR6 2.Remove DDQ4.DGQ4.DGR5.DDR13.DGC5.DDC6 3. DAR44=698R , DAR41=7.5K , DAR126=11K , AR52=82.5K 4. MC19 , MR24 , MC20 , MR26 上件 5. NR9 , NR10 , NR11 FOR REQ PULL UP 6. CHIPSET -->10HB1-03B460-10R 7. ADD WR6 (Note33) 8. MR23 / MR25 -->2.2/4(Note30 b) 9. JP8 PULL UP OR87 NA , OR23上件 10. 9MB46HD3-00-10C

Circuit or PCB layout change

Data	Change Item	Reason
2019/10/24	0.1 New BOM release PCB:0.1	Modify from B365 M AORUS Elitte
2020/01/22	0.2 E-BOM release PCB:0.2	1. PCIEx16-->灰色 無鐵殼(11AC1-023164-D1R/D3R) 2. PCIEx4-->灰色 (11AC1-023065-51R/53R) 3. M2 螺柱更改為H8.5,針對PHSION MODUL零件過近問題

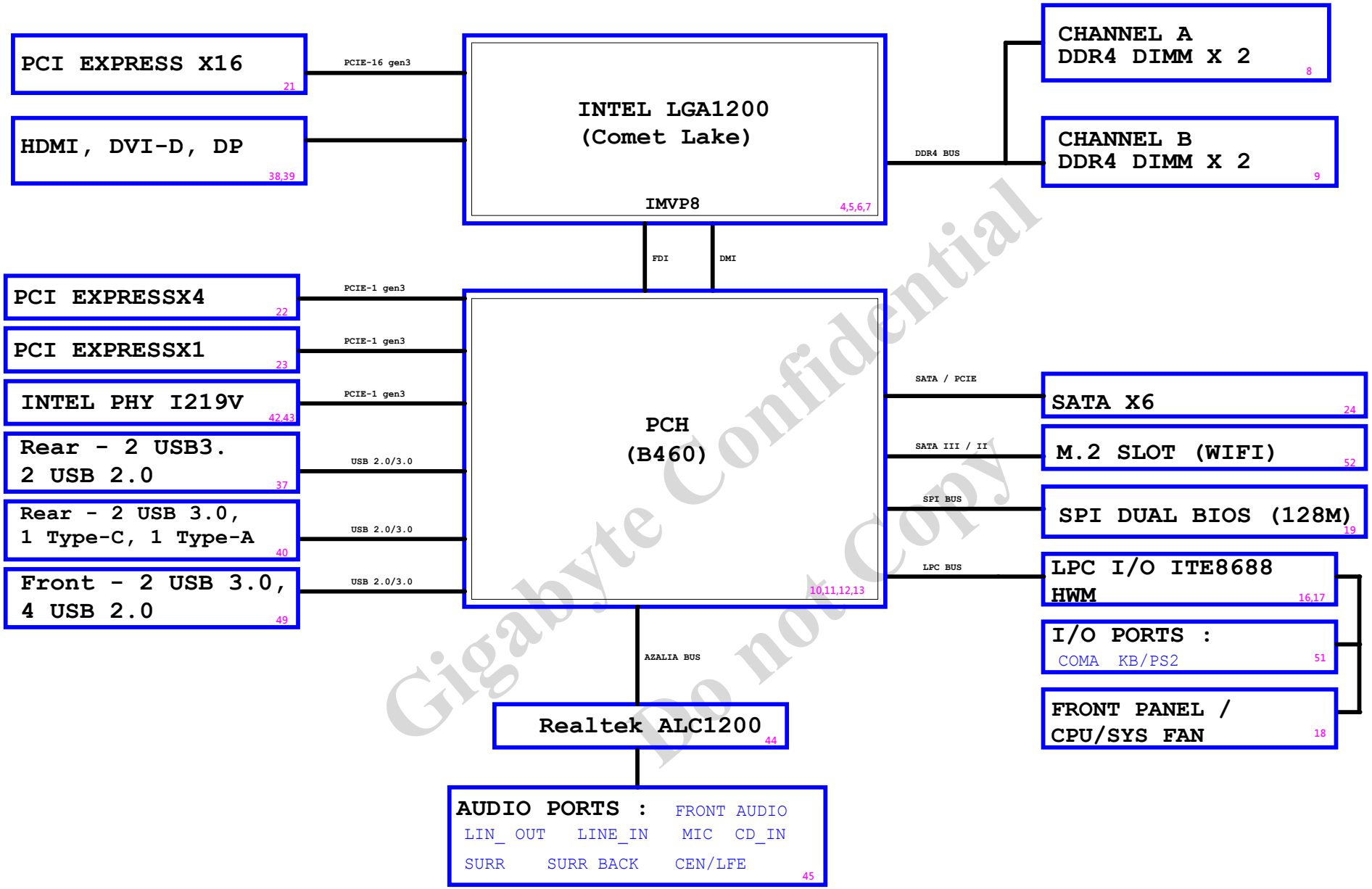
GIGABYTE™

Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: B460 HD3 | Rev: 1.01

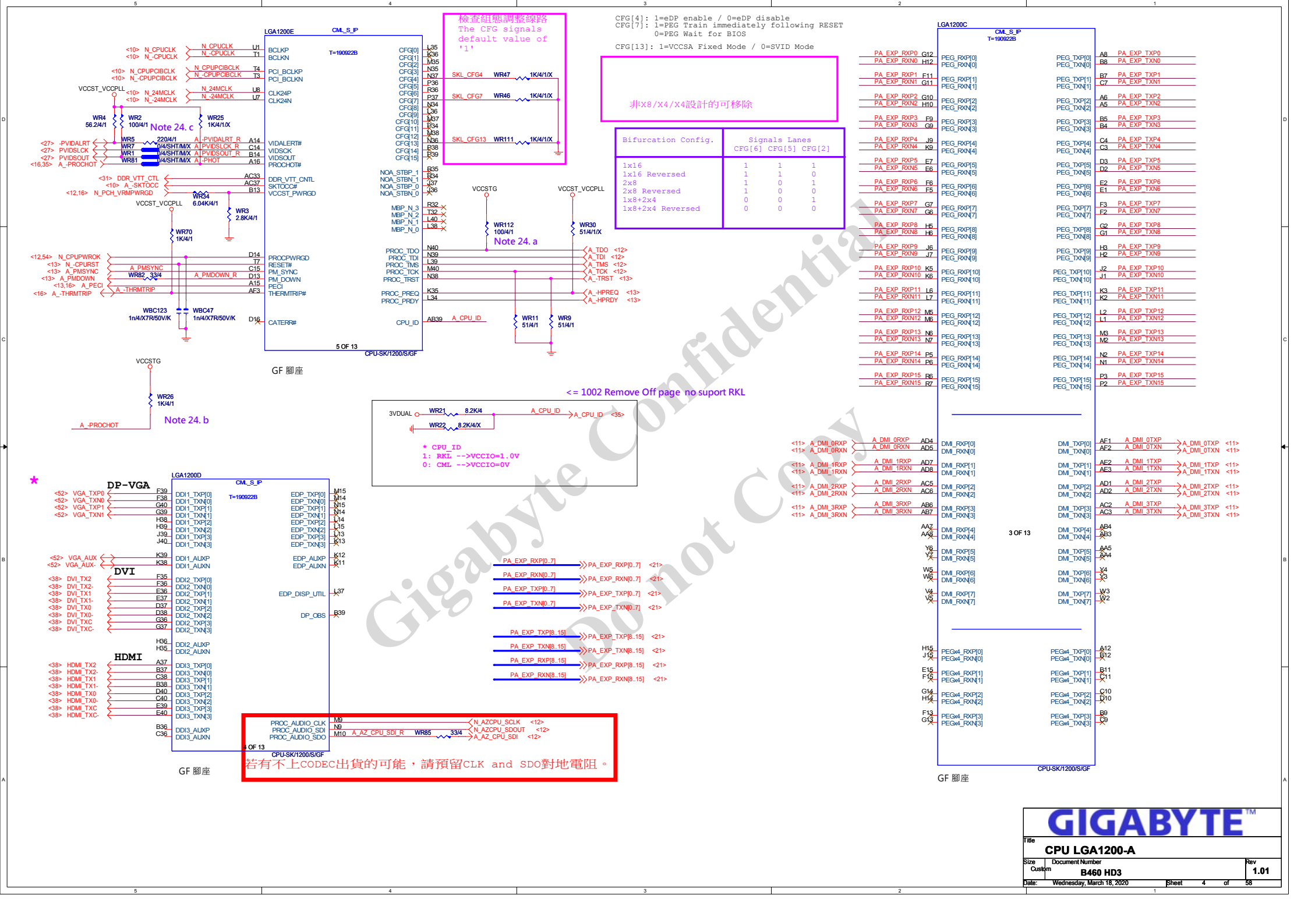
Date: Thursday, April 09, 2020 | Sheet 2 of 58

BLOCK DIAGRAM



GIGABYTE Technology

Title	BLOCK DIAGRAM	
Size: C	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 3 of 58	


LGA1200E
CML_S_IP
T=190922B
檢查組態調整線路
The CFG signals default value of '1'
CFG[4]: 1=eDP enable / 0=eDP disable
CFG[7]: 1=PEG Train immediately following RESET
0=PEG Wait for BIOS
CFG[13]: 1=VCCSA Fixed Mode / 0=SVID Mode
非X8/X4/X4設計的可移除
Bifurcation Config.
Signals Lanes CFG[6] CFG[5] CFG[2]
1x16 1 1 1
1x16 Reversed 1 1 0
2x8 1 0 1
2x8 Reversed 1 0 0
1x8+2x4 0 0 1
1x8+2x4 Reversed 0 0 0
Note 24. c
Note 24. a
Note 24. b
5 OF 13
CPU-SK/1200/S/GF
GF 腳座
<= 1002 Remove Off page no suport RKL
* CPU_ID
1: RKL -->VCCIO=1.0V
0: CML -->VCCIO=0V
LGA1200C
3 OF 13
LGA1200D
4 OF 13
DP-VGA
DVI
HDMI
若有不上CODEC出貨的可能，請預留CLK and SDO對地電阻。
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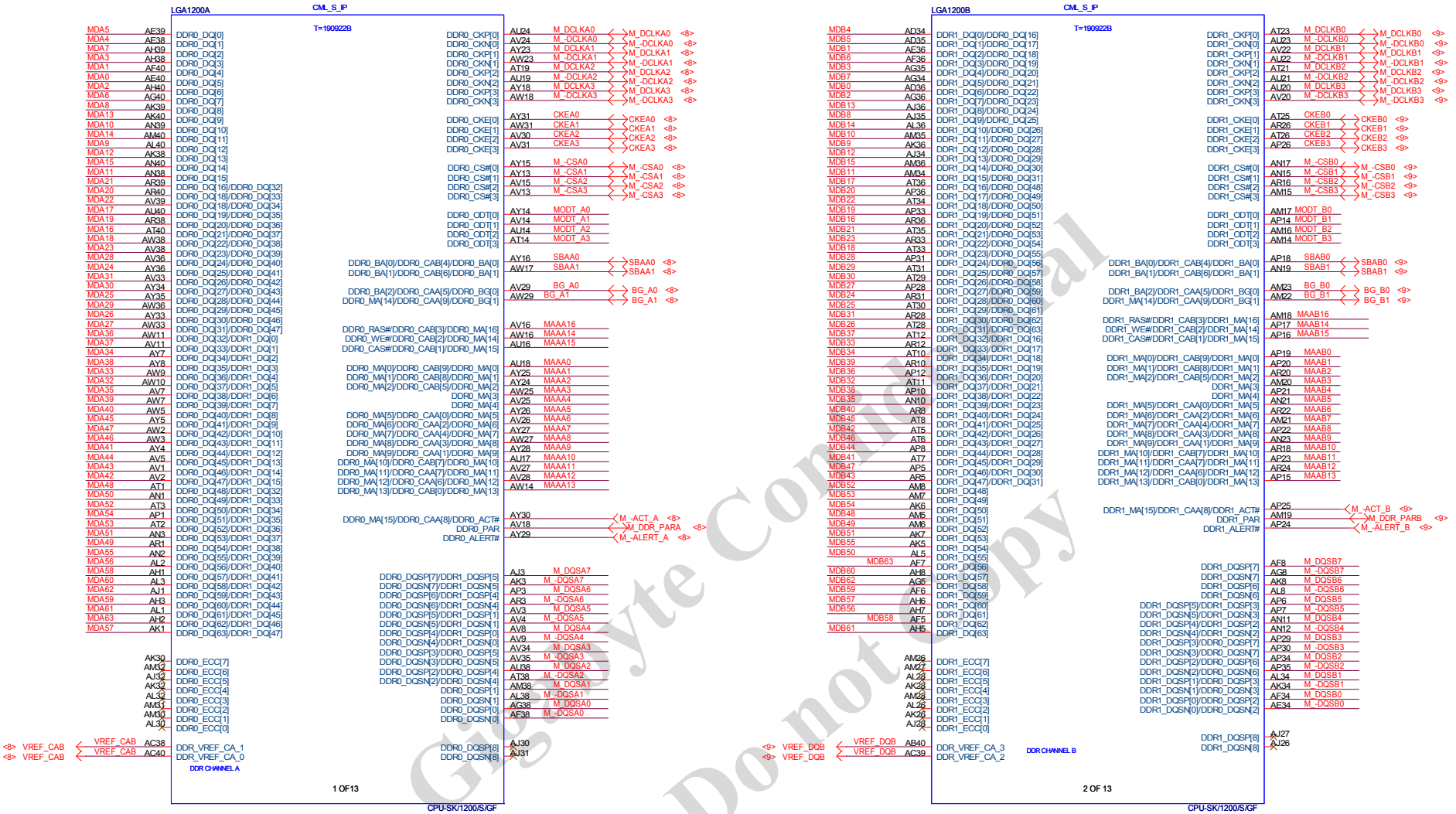
Do not Copy
GIGABYTE
Title
CPU LGA1200-A
Size Custom
Document Number B460 HD3
Rev 1.01
Date: Wednesday, March 18, 2020
Sheet 4 of 58



191002A

VCCSA

WBC56 22u/6/X5R/6.3V/M

WBC57 22u/6/X5R/6.3V/M

DCC56 22u/6/X5R/6.3V/M

放CPU SOCKET (TOP LAYER)

VCCSA

放CPU SOCKET (Bottom LAYER)

VCCIO2 CAP

放CPU SOCKET (TOP LAYER)

VCCIO2 CAP

放CPU SOCKET (Bottom LAYER)

VCCIO

WBC53 22u/6/X5R/6.3V/M

WBC54 22u/6/X5R/6.3V/M

WBC59 22u/6/X5R/6.3V/M

放CPU SOCKET (TOP LAYER)

+VCCDDQ_EDGECAP2

WBC75 22u/6/X5R/6.3V/M

+VCCDDQ_EDGECAP1

WBC76 22u/6/X5R/6.3V/M

放CPU SOCKET (Bottom LAYER)

1004 Removed

*CML增加,RKL才會用到

VCCGT

LGA1200J CML_S_IP T=190922B

VCCGT_SENSE AB37 → VCCGT_SENSE <27>

VSSGT_SENSE AB38 → VSSGT_SENSE <27>

VCCIO_0
VOUT = 0.95V FOR CML
VOUT = 1.05V FOR RKL
IOUT = 8A

12 OF 13

CPU-SK/1200/S/GF

GF 腳座

1014 Removed

1004 Removed

VCCSA

LGA1200K CML_S_IP T=190922B

VDDQ

VCCDDQ_EDGECAP2 → +VCCDDQ_EDGECAP2

VCCDDQ_EDGECAP1 → +VCCDDQ_EDGECAP1

VCCST → VCCST_VCCPLL

VCCSFR → VCCST_VCCPLL

VCCSFR_OC → VDDQ

VCCSTG → VCCSTG

VCCFPGM → VCCSTG

VCCSA_SENSE

VCCIO_1_2_SENSE

VCCIO_0_SENSE

VSS_SA_VCCIO_0_SENSE

11 OF 13

CPU-SK/1200/S/GF

GF 腳座

CML=0.17A
RKL=0.25A

W_OVU1 AP7365-WG-7/SOT23-5/600mA

Vout=0.8*(R1+R2)/R2

W_OVC1 2.2u/4/X5R/6.3V/M

W_OVR3 1K/4/1

W_OVC4 22P/4/NPO/50V/J

W_OVC6 10U/6/X5R/6.3V/M

W_OVR14 1.6K/4/1

W_OVC5 0.1u/4/X7R/16V/K

W_OVC8 22u/6/X5R/6.3V/M

W_OVC9 22u/6/X5R/6.3V/M

WBC77 22u/6/X5R/6.3V/M

Note 37 a/b

W_OVR5 8.2K/4

W_OVR6 8.2K/4

W_OVR4 8.2K/4

W_OVQ1 SOT23

W_OVQ2 SOT23 2N7002/SOT23/25pF/5

W_OVC7 0.01u/4/X7R/25V/K/X

MMBT2222A/SOT23/600mA/40

LGA1200L CML_S_IP T=190922B

A_CPU_PCH_TO_R WR88 33/4 → A_CPU_PCH_TO <13>

N_PCH_CPU_TI <13>

WR6 0/4

Note 33

13 OF 13

CPU-SK/1200/S/GF

GF 腳座

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Title: CPU LGA1200-C

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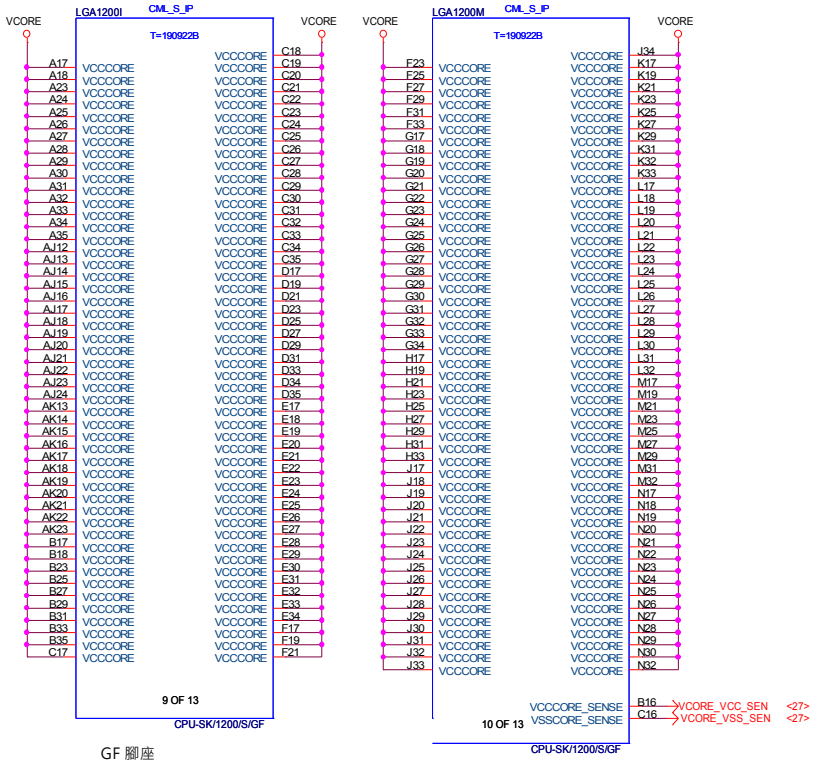
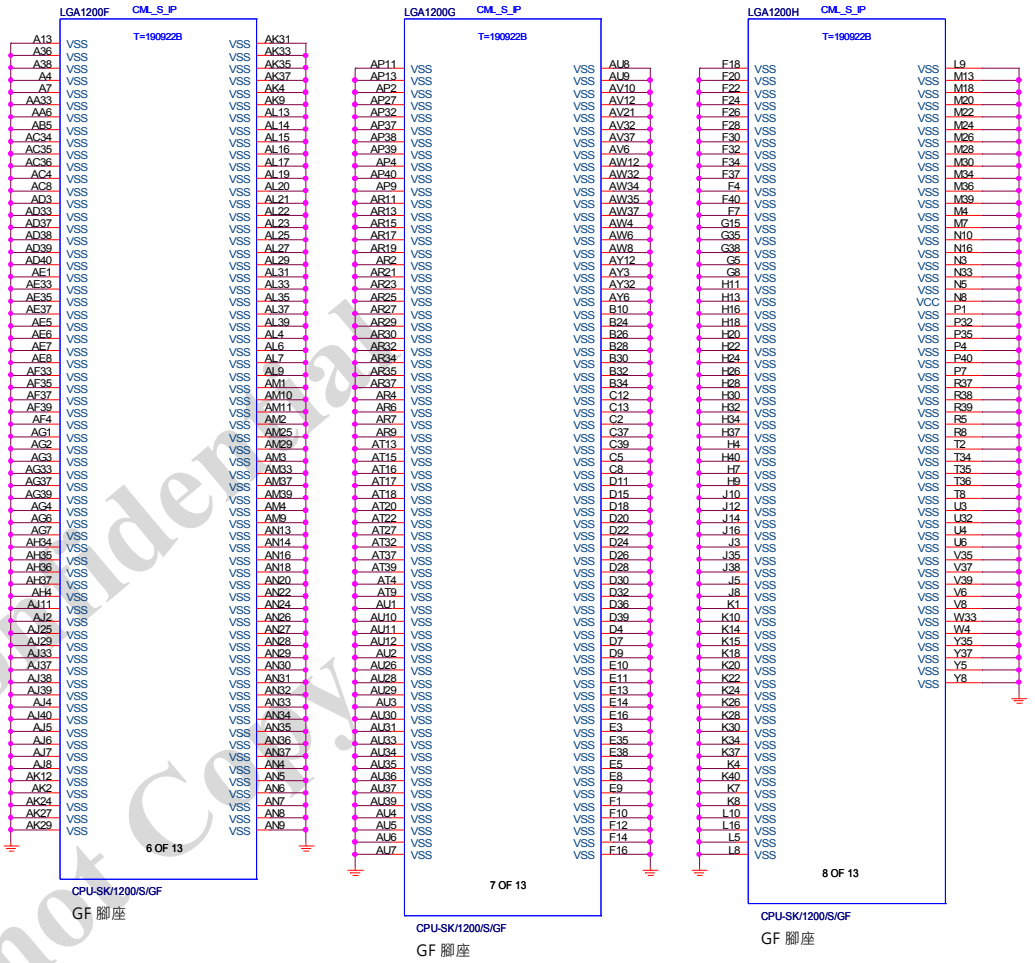
Date: Tuesday, March 31, 2020 | Sheet 6 of 58



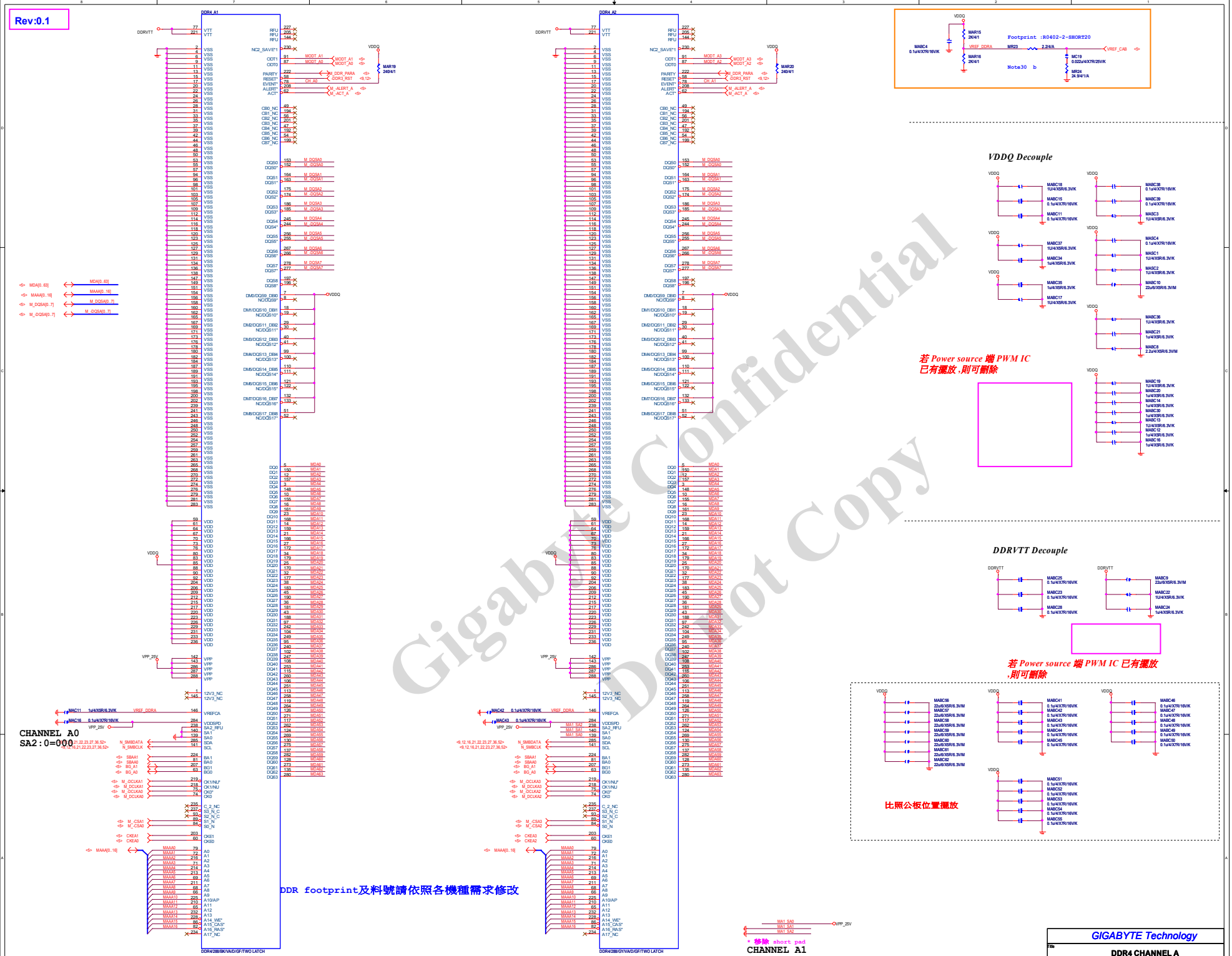


* 刪 Vcore 電容

GIGABYTE™

Title	CPU LGA1200-D	
Size: Custom	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 7 of 58	

Rev:0.1



VDDQ Decouple

若 Power source 端 PWM IC 已有擺放,則可刪除

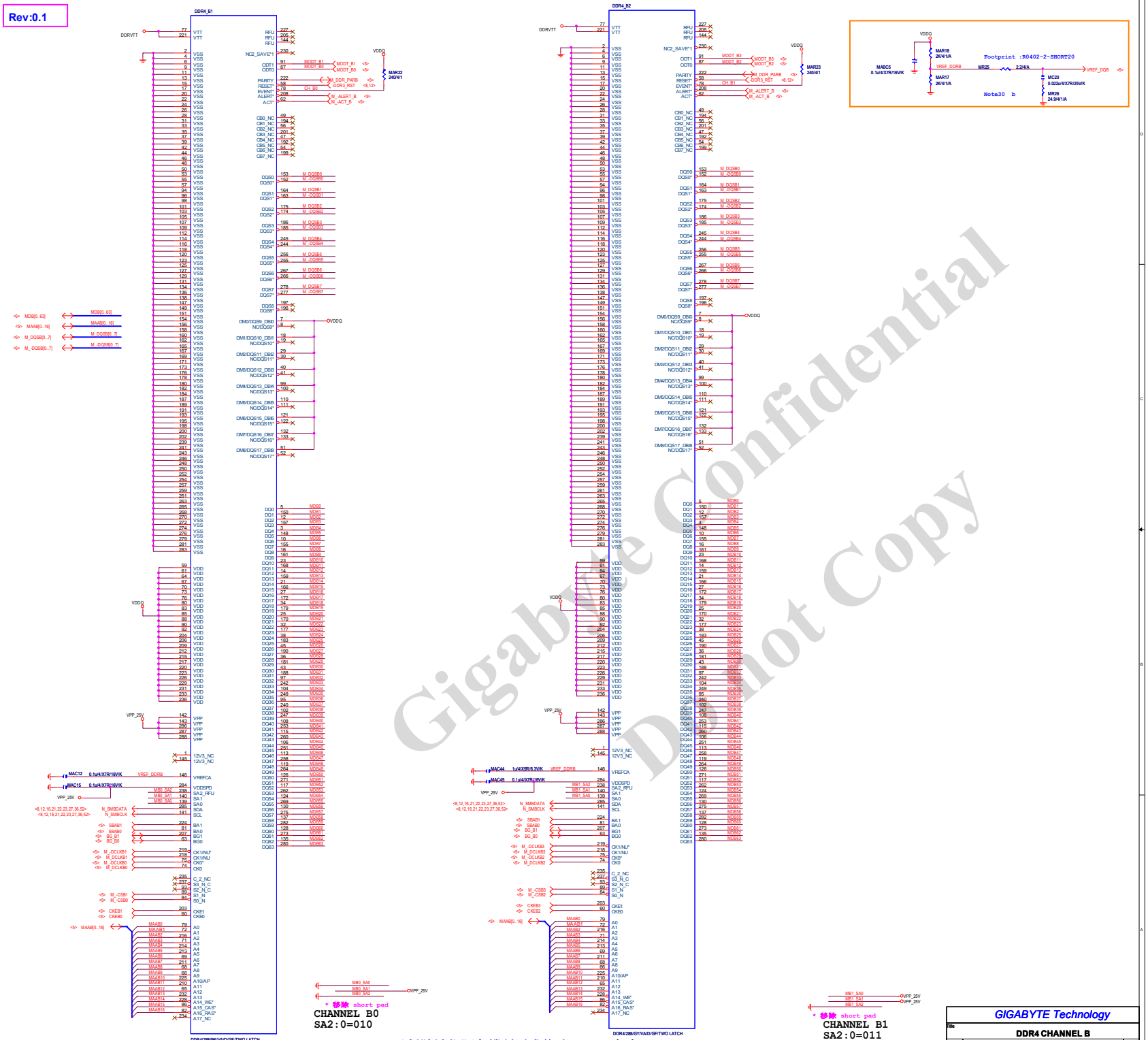
DDRVTT Decouple

若 Power source 端 PWM IC 已有擺放,則可刪除

比照公板位置擺放

GIGABYTE Technology			
Title: DDR4 CHANNEL A			
Size: Custom	Document Number: B460 HD3		Rev: 1.0
Date:		Sheet 8 of 58	

Rev:0.1



黑色

灰色

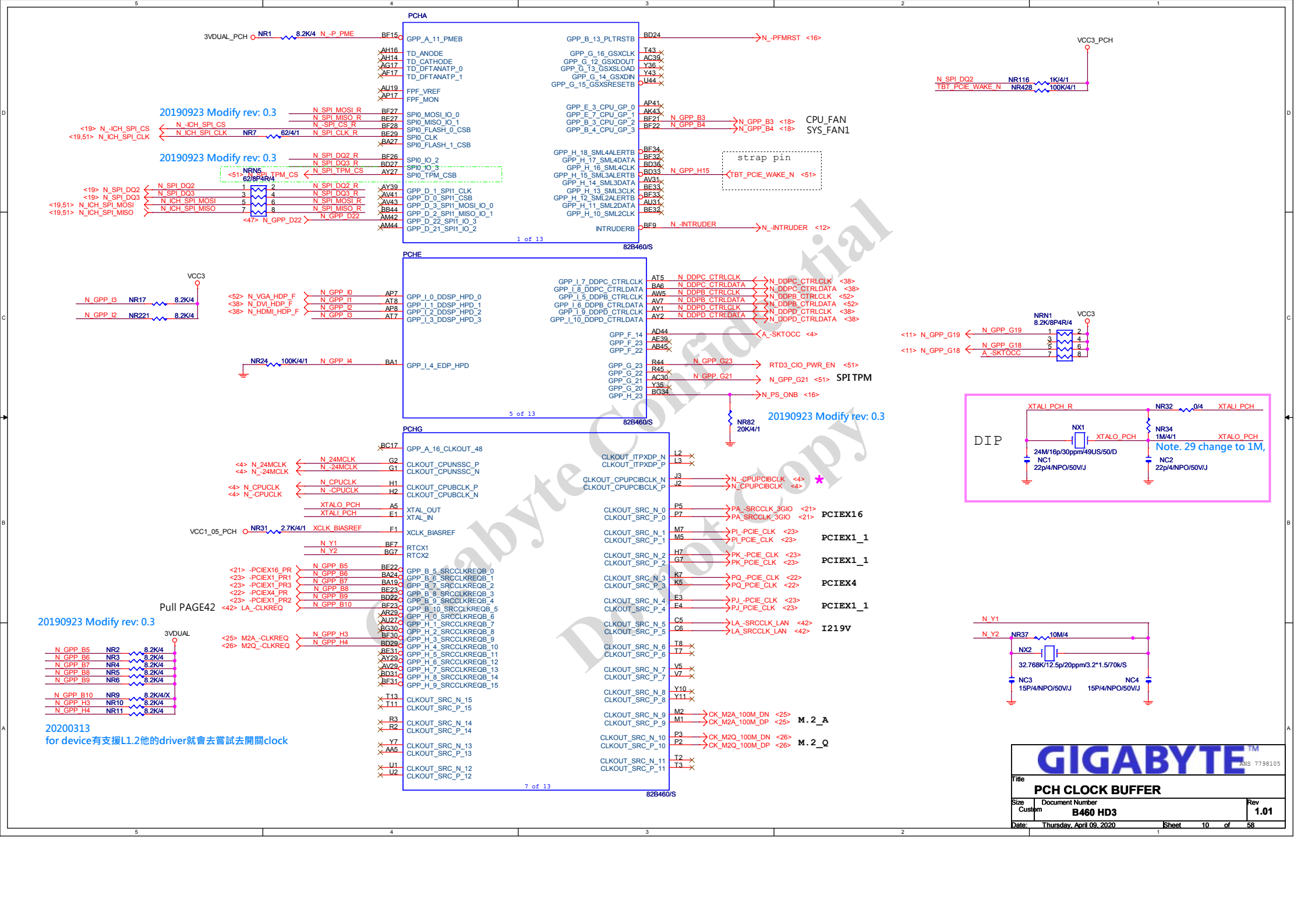
* 移除 short pad

CHANNEL B0
SA2:0=010

CHANNEL B1
SA2:0=011

DDR footprint及料號請依照各機種需求修改

GIGABYTE Technology		
Title: DDR4 CHANNEL B		
Size: Custom	Document Number: B460 HD3	Rev: 1.0
Date:	Sheet 9 of 58	

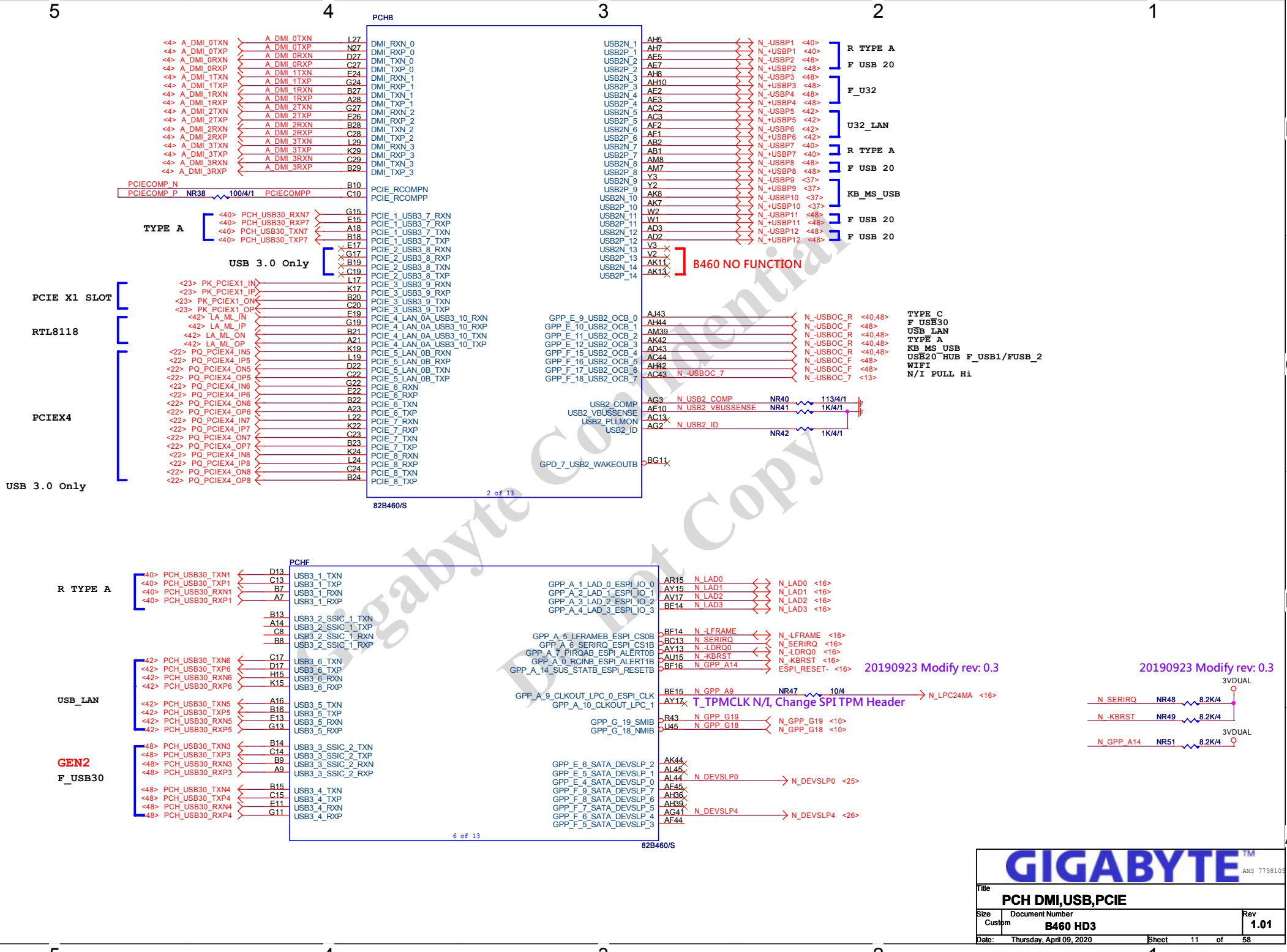


GIGABYTE™ ANS 7798105

Title: PCH CLOCK BUFFER

Size	Document Number	Rev
Custom	B460 HD3	1.01

Date: Thursday, April 09, 2020 Sheet 10 of 58



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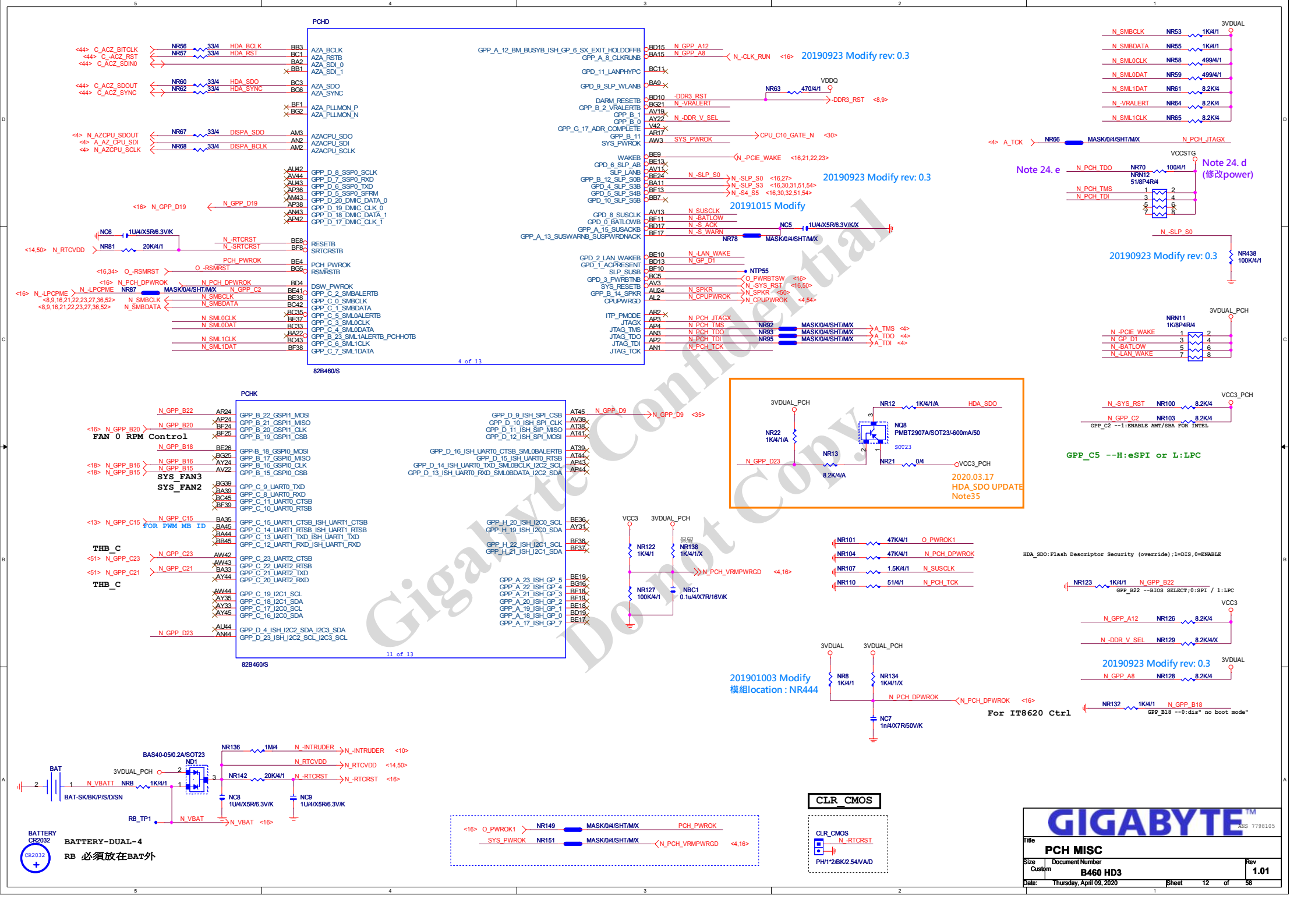
Title	PCH DMI,USB,PCIE		
Size: Custom	Document Number: B460 HD3		Rev: 1.01
Date: Thursday, April 09, 2020	Sheet 11 of 58		



Title	PCH MISC
Size	Custom
Document Number	B460 HD3
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Date:	Thursday, April 09, 2020
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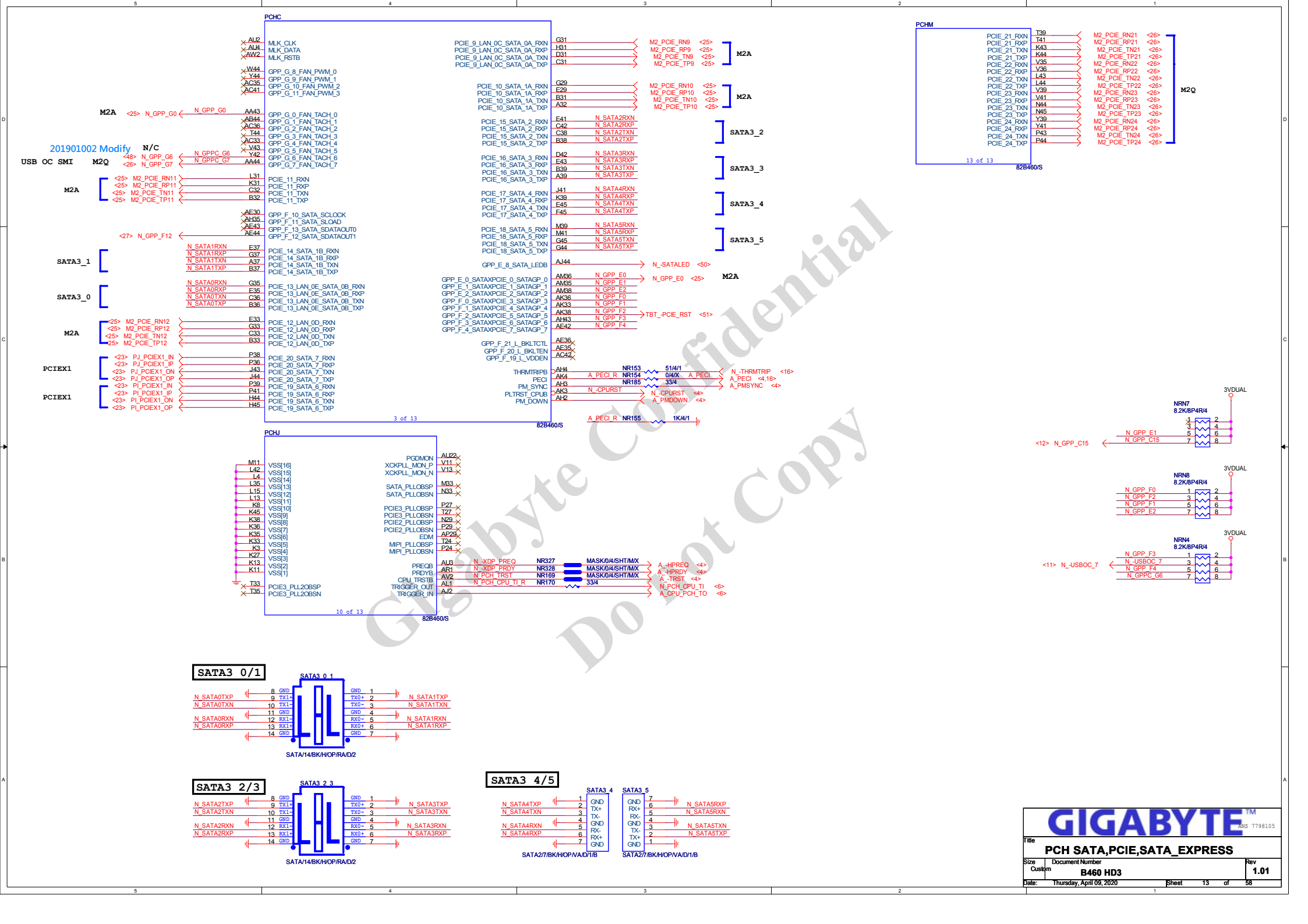
PCHC
MLK_CLK
MLK_DATA
MLK_RSTB
GPP_G_8_FAN_PWM_0
GPP_G_9_FAN_PWM_1
GPP_G_10_FAN_PWM_2
GPP_G_11_FAN_PWM_3
M2A
N_GPP_G0
GPP_G_0_FAN_TACH_0
GPP_G_1_FAN_TACH_1
GPP_G_2_FAN_TACH_2
GPP_G_3_FAN_TACH_3
GPP_G_4_FAN_TACH_4
GPP_G_5_FAN_TACH_5
GPP_G_6_FAN_TACH_6
GPP_G_7_FAN_TACH_7
201901002 Modify
N/C
USB OC SMI
M2Q
N_GPPC_G6
N_GPPC_G7
N_GPP_G6
N_GPP_G7
M2A
PCIE_11_RXN
PCIE_11_RXP
PCIE_11_TXN
PCIE_11_TXP
GPP_F_10_SATA_SCLOCK
GPP_F_11_SATA_SLOAD
GPP_F_13_SATA_SDATAOUT0
GPP_F_12_SATA_SDATAOUT1
N_GPP_F12
SATA3_1
PCIE_14_SATA_1B_RXN
PCIE_14_SATA_1B_RXP
PCIE_14_SATA_1B_TXN
PCIE_14_SATA_1B_TXP
SATA3_0
PCIE_13_LAN_0E_SATA_0B_RXN
PCIE_13_LAN_0E_SATA_0B_RXP
PCIE_13_LAN_0E_SATA_0B_TXN
PCIE_13_LAN_0E_SATA_0B_TXP
M2A
PCIE_12_LAN_0D_RXN
PCIE_12_LAN_0D_RXP
PCIE_12_LAN_0D_TXN
PCIE_12_LAN_0D_TXP
PCIEX1
PCIE_20_SATA_7_RXN
PCIE_20_SATA_7_RXP
PCIE_20_SATA_7_TXN
PCIE_20_SATA_7_TXP
PCIEX1
PCIE_19_SATA_6_RXN
PCIE_19_SATA_6_RXP
PCIE_19_SATA_6_TXN
PCIE_19_SATA_6_TXP
3 of 13
82B460/S
PCIE_9_LAN_0C_SATA_0A_RXN
PCIE_9_LAN_0C_SATA_0A_RXP
PCIE_9_LAN_0C_SATA_0A_TXN
PCIE_9_LAN_0C_SATA_0A_TXP
M2A
PCIE_10_SATA_1A_RXN
PCIE_10_SATA_1A_RXP
PCIE_10_SATA_1A_TXN
PCIE_10_SATA_1A_TXP
M2A
PCIE_15_SATA_2_RXN
PCIE_15_SATA_2_RXP
PCIE_15_SATA_2_TXN
PCIE_15_SATA_2_TXP
SATA3_2
PCIE_16_SATA_3_RXN
PCIE_16_SATA_3_RXP
PCIE_16_SATA_3_TXN
PCIE_16_SATA_3_TXP
SATA3_3
PCIE_17_SATA_4_RXN
PCIE_17_SATA_4_RXP
PCIE_17_SATA_4_TXN
PCIE_17_SATA_4_TXP
SATA3_4
PCIE_18_SATA_5_RXN
PCIE_18_SATA_5_RXP
PCIE_18_SATA_5_TXN
PCIE_18_SATA_5_TXP
SATA3_5
GPP_E_8_SATA_LEDB
N_SATALED
GPP_E_0_SATAXPCIE_0_SATAGP_0
GPP_E_1_SATAXPCIE_1_SATAGP_1
GPP_E_2_SATAXPCIE_2_SATAGP_2
GPP_F_0_SATAXPCIE_3_SATAGP_3
GPP_F_1_SATAXPCIE_4_SATAGP_4
GPP_F_2_SATAXPCIE_5_SATAGP_5
GPP_F_3_SATAXPCIE_6_SATAGP_6
GPP_F_4_SATAXPCIE_7_SATAGP_7
N_GPP_E0
N_GPP_E1
N_GPP_E2
N_GPP_F0
N_GPP_F1
N_GPP_F2
N_GPP_F3
N_GPP_E0
M2A
TBT_-PCIE_RST
GPP_F_21_L_BKLTCTL
GPP_F_20_L_BKLTEN
GPP_F_19_L_VDDEN
THRMTRIPB
PECI
PM_SYNC
PLTRST_CPUB
PM_DOWN
A_PECI_R
NR153
NR154
NR185
NR155
51/4/1
0/4/X
33/4
1K/4/1
N_-THRMTRIP
A_PECI
A_PMSYNC
N_-CPURST
A_PMDOWN
PCHJ
VSS[16]
VSS[15]
VSS[14]
VSS[13]
VSS[12]
VSS[11]
VSS[10]
VSS[9]
VSS[8]
VSS[7]
VSS[6]
VSS[5]
VSS[4]
VSS[3]
VSS[2]
VSS[1]
PCIE3_PLL2OBSP
PCIE3_PLL2OBSN
PGDMON
XCKPLL_MON_P
XCKPLL_MON_N
SATA_PLLOBSP
SATA_PLLOBSN
PCIE3_PLLOBSP
PCIE3_PLLOBSN
PCIE2_PLLOBSP
PCIE2_PLLOBSN
EDMI
MIPI_PLLOBSP
MIPI_PLLOBSN
PREQB
PRDYB
CPU_TRSTB
TRIGGER_OUT
TRIGGER_IN
N_XDP_PREQ
N_XDP_PRDY
N_PCH_TRST
N_PCH_CPU_TI_R
NR327
NR328
NR169
NR170
MASK/0/4/SHT/M/X
MASK/0/4/SHT/M/X
MASK/0/4/SHT/M/X
33/4
A_-HPREQ
A_-HPRDY
A_-TRST
N_PCH_CPU_TI
A_CPU_PCH_TO
10 of 13
82B460/S
PCHM
PCIE_21_RXN
PCIE_21_RXP
PCIE_21_TXN
PCIE_21_TXP
PCIE_22_RXN
PCIE_22_RXP
PCIE_22_TXN
PCIE_22_TXP
PCIE_23_RXN
PCIE_23_RXP
PCIE_23_TXN
PCIE_23_TXP
PCIE_24_RXN
PCIE_24_RXP
PCIE_24_TXN
PCIE_24_TXP
M2Q
13 of 13
82B460/S
3VDUAL
NRN7
8.2K/8P4R/4
N_GPP_E1
N_GPP_C15
N_GPP_C15
NRN8
8.2K/8P4R/4
N_GPP_F0
N_GPP_F2
N_GPP_F1
N_GPP_E2
NRN4
8.2K/8P4R/4
N_GPP_F3
N_-USBOC_7
N_GPP_F4
N_GPPC_G6
N_-USBOC_7
SATA3 0/1
SATA3_0_1
N_SATA0TXP
N_SATA0TXN
N_SATA0RXN
N_SATA0RXP
N_SATA1TXP
N_SATA1TXN
N_SATA1RXN
N_SATA1RXP
SATA/14/BK/H/OP/RA/D/2
SATA3 2/3
SATA3_2_3
N_SATA2TXP
N_SATA2TXN
N_SATA2RXN
N_SATA2RXP
N_SATA3TXP
N_SATA3TXN
N_SATA3RXN
N_SATA3RXP
SATA/14/BK/H/OP/RA/D/2
SATA3 4/5
SATA3_4
SATA3_5
N_SATA4TXP
N_SATA4TXN
N_SATA4RXN
N_SATA4RXP
N_SATA5RXP
N_SATA5RXN
N_SATA5TXN
N_SATA5TXP
SATA2/7/BK/H/OP/VA/D/1/B
SATA2/7/BK/H/OP/VA/D/1/B
GIGABYTE
ANS 7798105
Title
PCH SATA,PCIE,SATA_EXPRESS
Size
Custom
Document Number
B460 HD3
Rev
1.01
Date:
Thursday, April 09, 2020
Sheet
13
of
58
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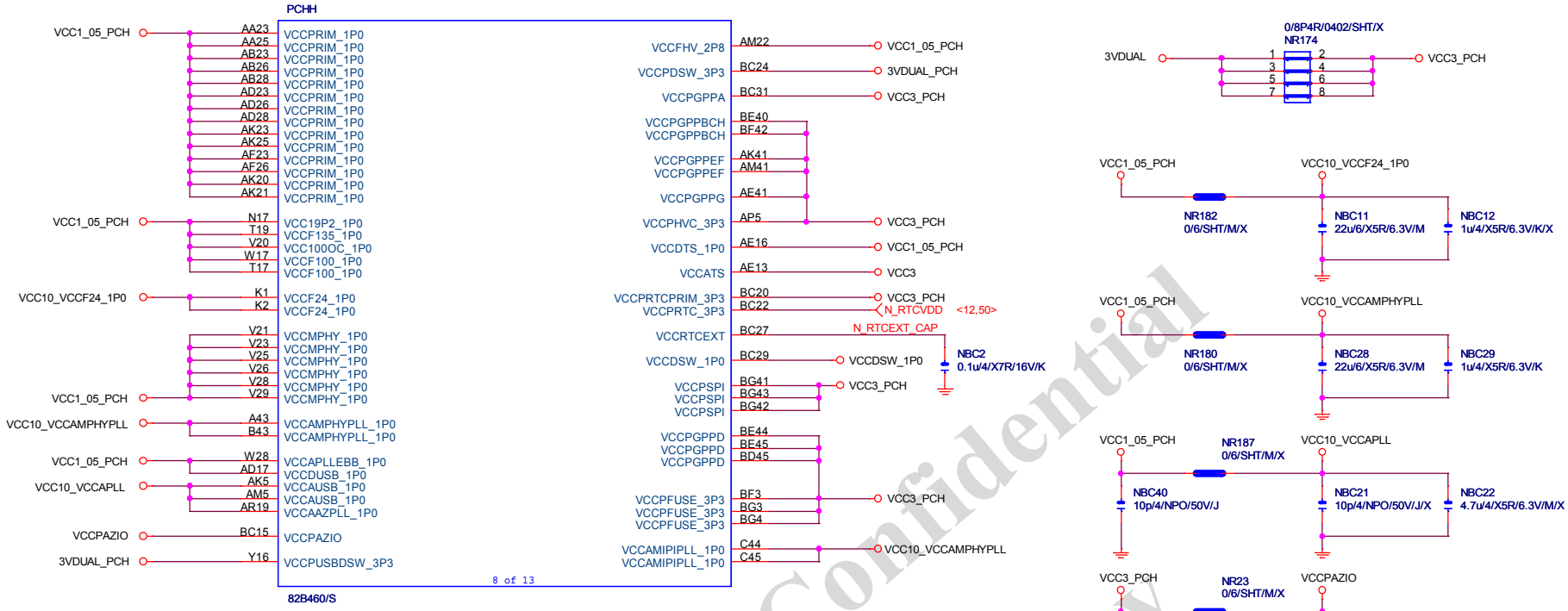

GIGABYTE™ ANS 7798105

Title	PCH PWR		
Size B	Document Number B460 HD3		Rev 1.01
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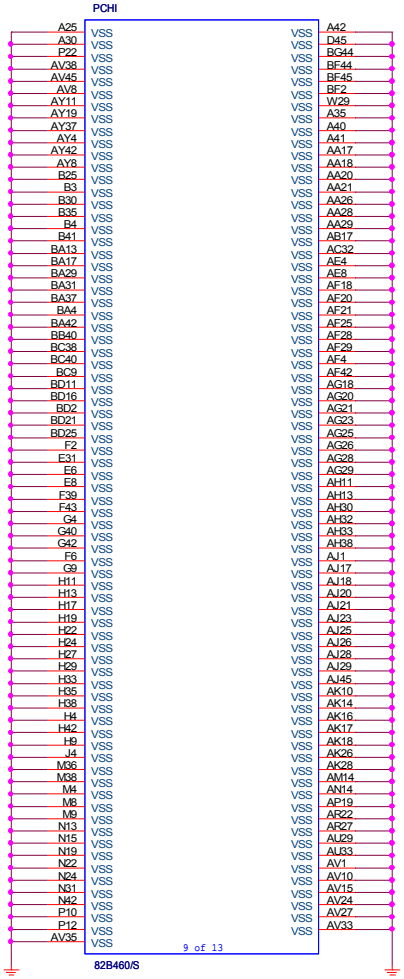
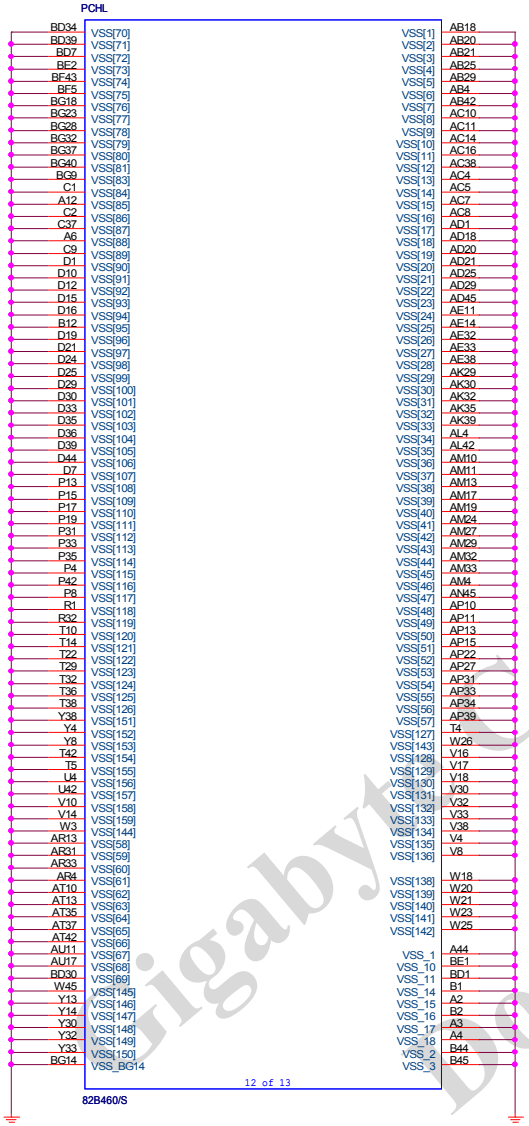
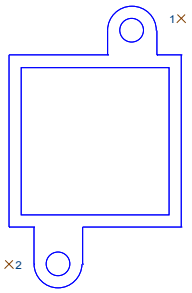


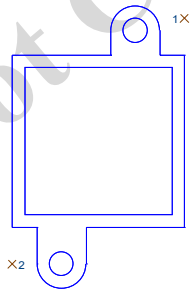




T+R

Footprint : SINK_Z490_AORUS_MASTER

MOS_HS
HEAT SINK(12SP2-S09426-21R_12SP2-S09426-22R_12SP2-S09426-23R)



後窗裝甲 (便宜+IO SHIELD))

Footprint :SINK_Z490_AORUS_MASTER_PCH

PCH_HS
HEAT SINK(12SP2-S08604-21R_12SP2-S08604-22R_12SP2-S08604-23R)

GIGABYTE™ ANS 7798105

Title: PCH GND		
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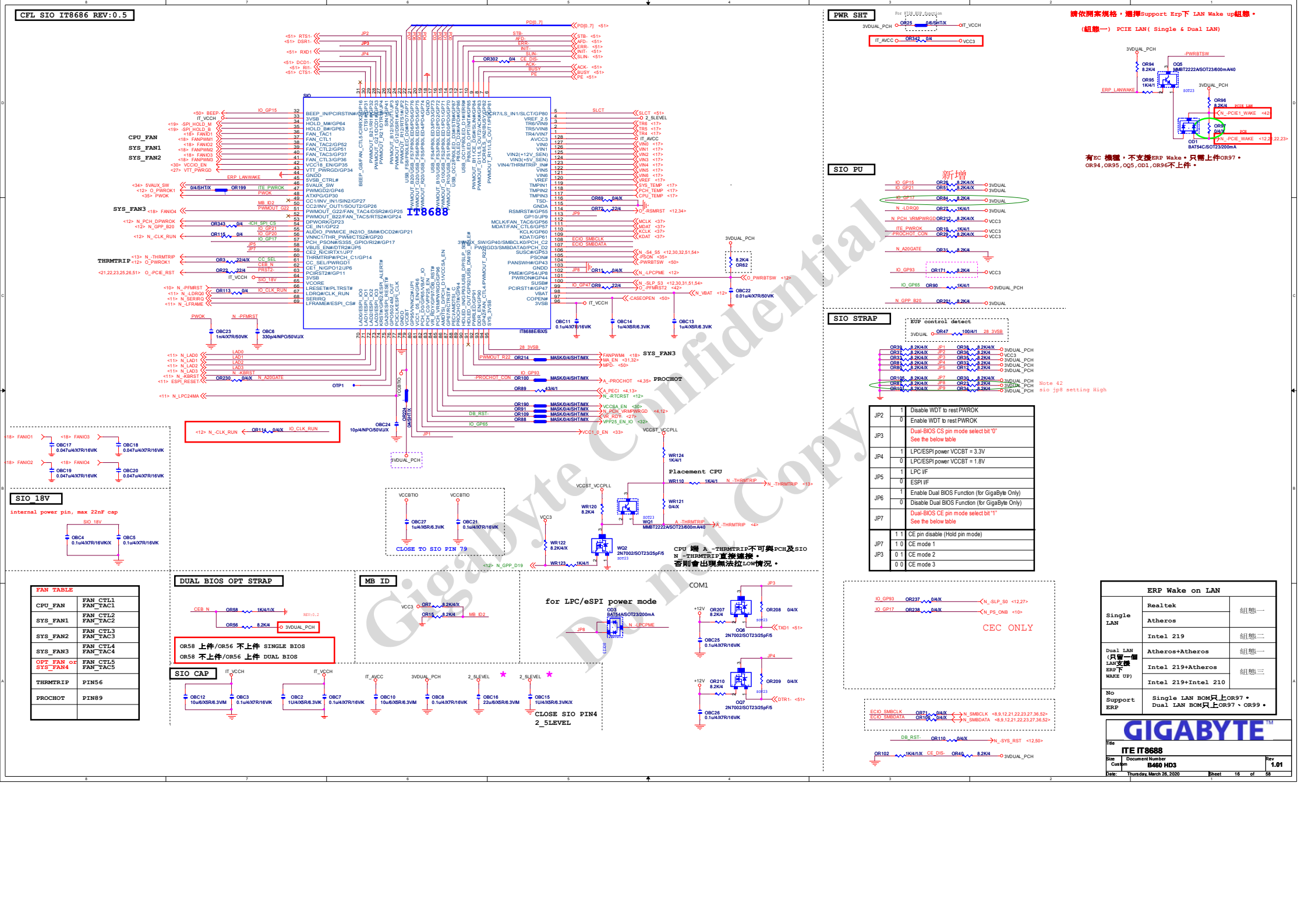

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	
	Intel 219	組態二
Dual LAN (只留一個LAN支援ERP下WAKE UP)	Atheros+Atheros	組態一
	Intel 219+Atheros	組態三
	Intel 219+Intel 210	
No Support ERP	Single LAN BOM只上OR97。 Dual LAN BOM只上OR97、OR99。	

GIGABYTE

Title	ITE IT8688	
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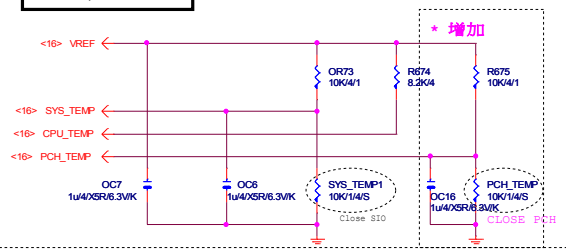
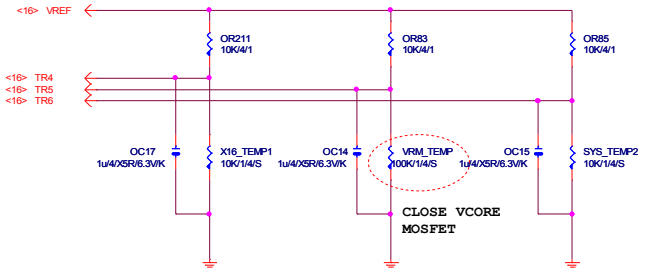
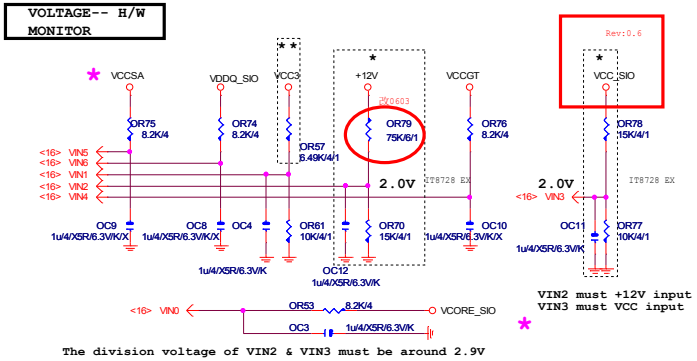
TEMP H/W MONITOR

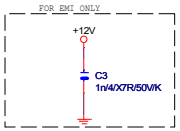


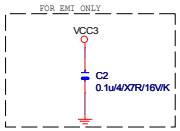
5個FAN時使用



VOLTAGE-- H/W MONITOR







★Update 2015-04.24

GIGABYTE Technology		
Title: HWM,KB/MS, FAN CTRL		
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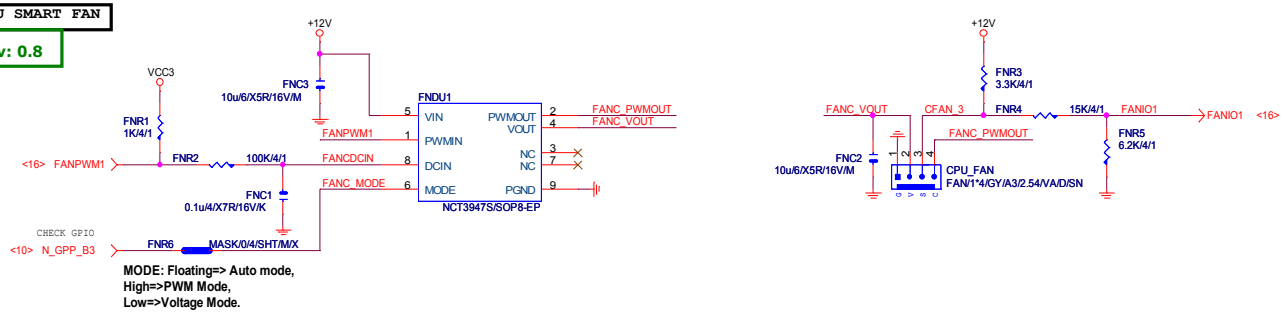
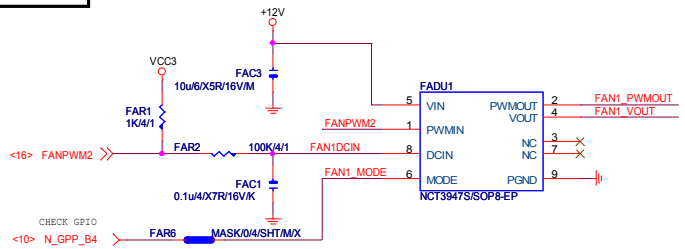
CPU SMART FAN

Rev: 0.8

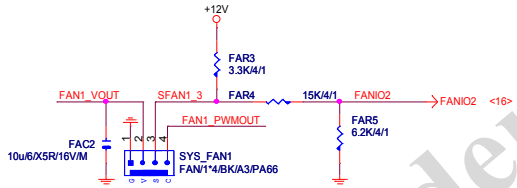


MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

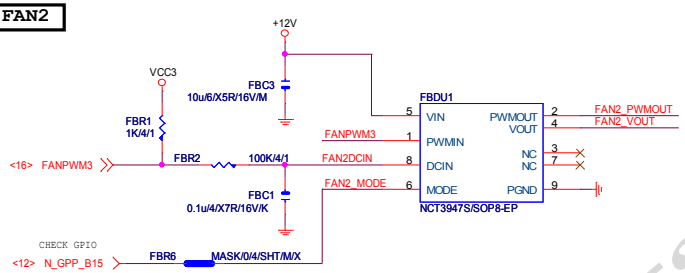
SYSTEM FAN1



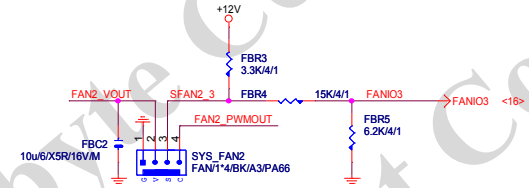
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.



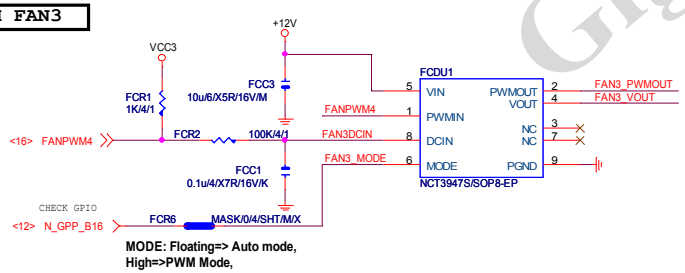
SYSTEM FAN2



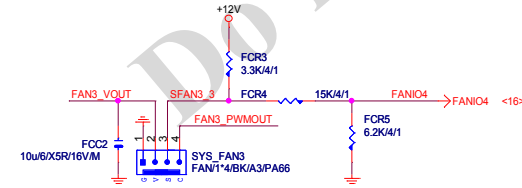
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.



SYSTEM FAN3



MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.



GIGABYTE Technology		
Title: FAN CTRL		
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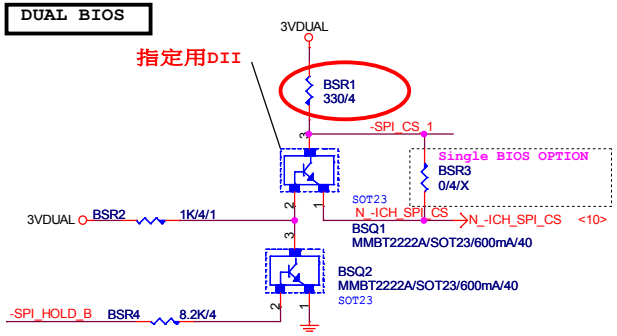
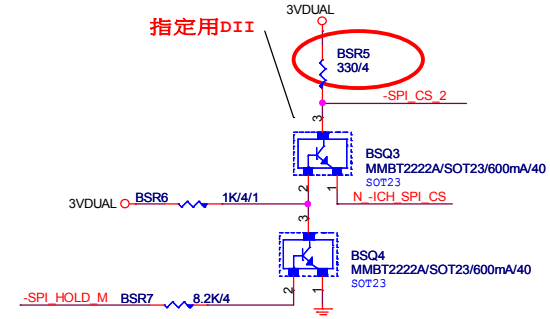
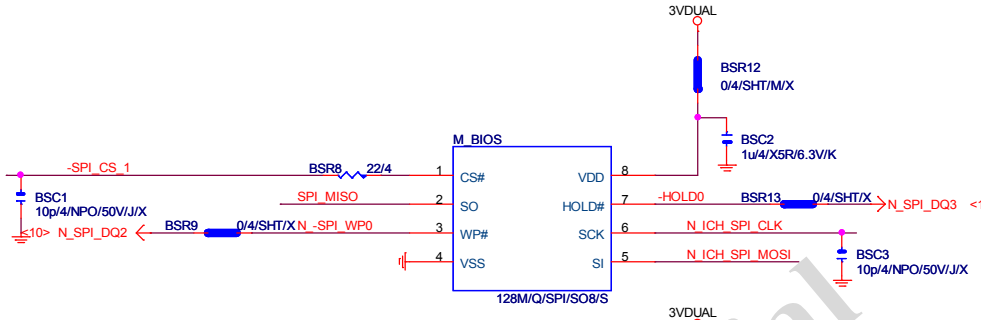
DUAL BIOS

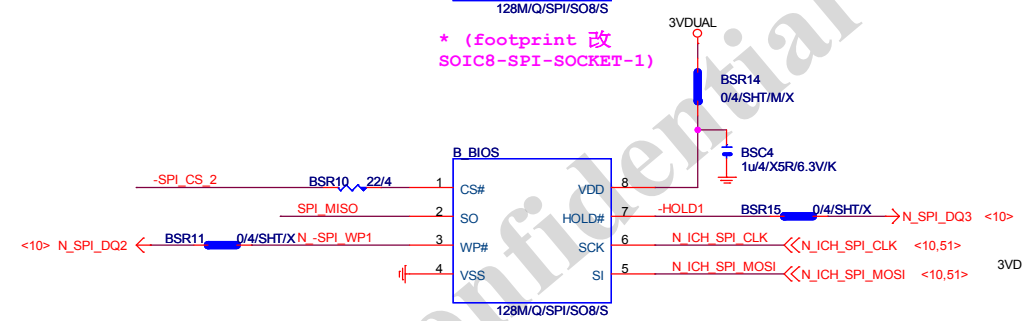
指定用DII



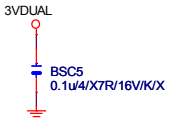




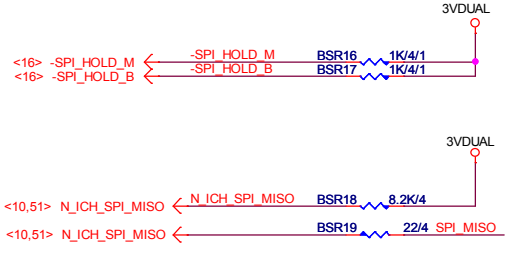
* (footprint 改 SOIC8-SPI-SOCKET-1)



* (footprint 改 IC8-BIOS)

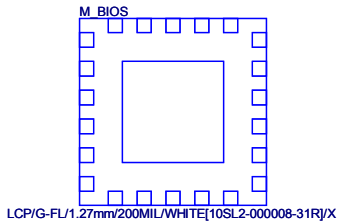


MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K



* 試產先上 , PVT 移除

GIGABYTE Technology

Title: BIOS

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GIGABYTE™

Title	CEC relate circuit	
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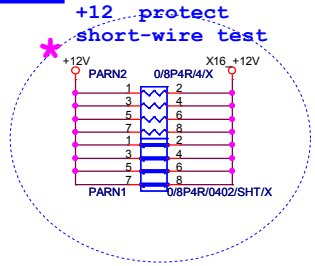
+12 protect short-wire test



PCIESLOT-164STH

3GIO_*16

PCIEX16

X16_+12V

PAR1 0/4/SHT/M/X

PAR2 0/4/SHT/M/X

PAR3 0/4/SHT/M/X

PAR4 0/4/X

PAR5 0/4/X

PAR6 0/4/X

<8,9,12,16,22,23,27,36,52> N_SMBCLK

<8,9,12,16,22,23,27,36,52> N_SMBDATA

VCC3

3VDUAL

<12,16,22,23> N_-PCIE_WAKE

O_-PCIE_RST <16,22,23,25,26,51>

PAC1 33p/4/NPO/50V/J

KEY

1002 Modify

-PCIEX16_PR

PA_SRCCLK_3GIO <10>

PA_-SRCCLK_3GIO <10>

<10> -PCIEX16_PR

PA_EXP_RXP[0..15] PA_EXP_RXP[0..15] <4>

PA_EXP_RXN[0..15] PA_EXP_RXN[0..15] <4>

PA_EXP_TXP[0..15] PA_EXP_TXP[0..15] <4>

PA_EXP_TXN[0..15] PA_EXP_TXN[0..15] <4>

PA_EXP_TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA_EXP_TXN7_C
PA_EXP_TXP8	PAC21	0.22u/4/X5R/6.3V/K	PA_EXP_TXP8_C
PA_EXP_TXN8	PAC20	0.22u/4/X5R/6.3V/K	PA_EXP_TXN8_C
PA_EXP_TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA_EXP_TXP9_C
PA_EXP_TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA_EXP_TXN9_C
PA_EXP_TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA_EXP_TXP10_C
PA_EXP_TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA_EXP_TXN10_C
PA_EXP_TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA_EXP_TXP11_C
PA_EXP_TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA_EXP_TXN11_C
PA_EXP_TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA_EXP_TXP12_C
PA_EXP_TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA_EXP_TXN12_C
PA_EXP_TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA_EXP_TXP13_C
PA_EXP_TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA_EXP_TXN13_C
PA_EXP_TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA_EXP_TXP14_C
PA_EXP_TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA_EXP_TXN14_C
PA_EXP_TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA_EXP_TXP15_C
PA_EXP_TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA_EXP_TXN15_C

PCIEX16:16/5/5/5/16

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCI-E/16X-164P/GY/LONG DOUBLE/HK*2

灰色

VCC3

PABC2 0.1u/4/X7R/16V/K

PABC3 0.1u/4/X7R/16V/K

PABC4 0.1u/4/X7R/16V/K/X

+12V

PAEC1 270u/FP/D/16V/8C/A/10m

X16_+12V

PABC1 0.1u/4/X7R/16V/K

VCC3

PAEC2 560u/FP/D/6.3V/69/A/7m

GIGABYTE Technology

Title: PCI EXPRESS * 16

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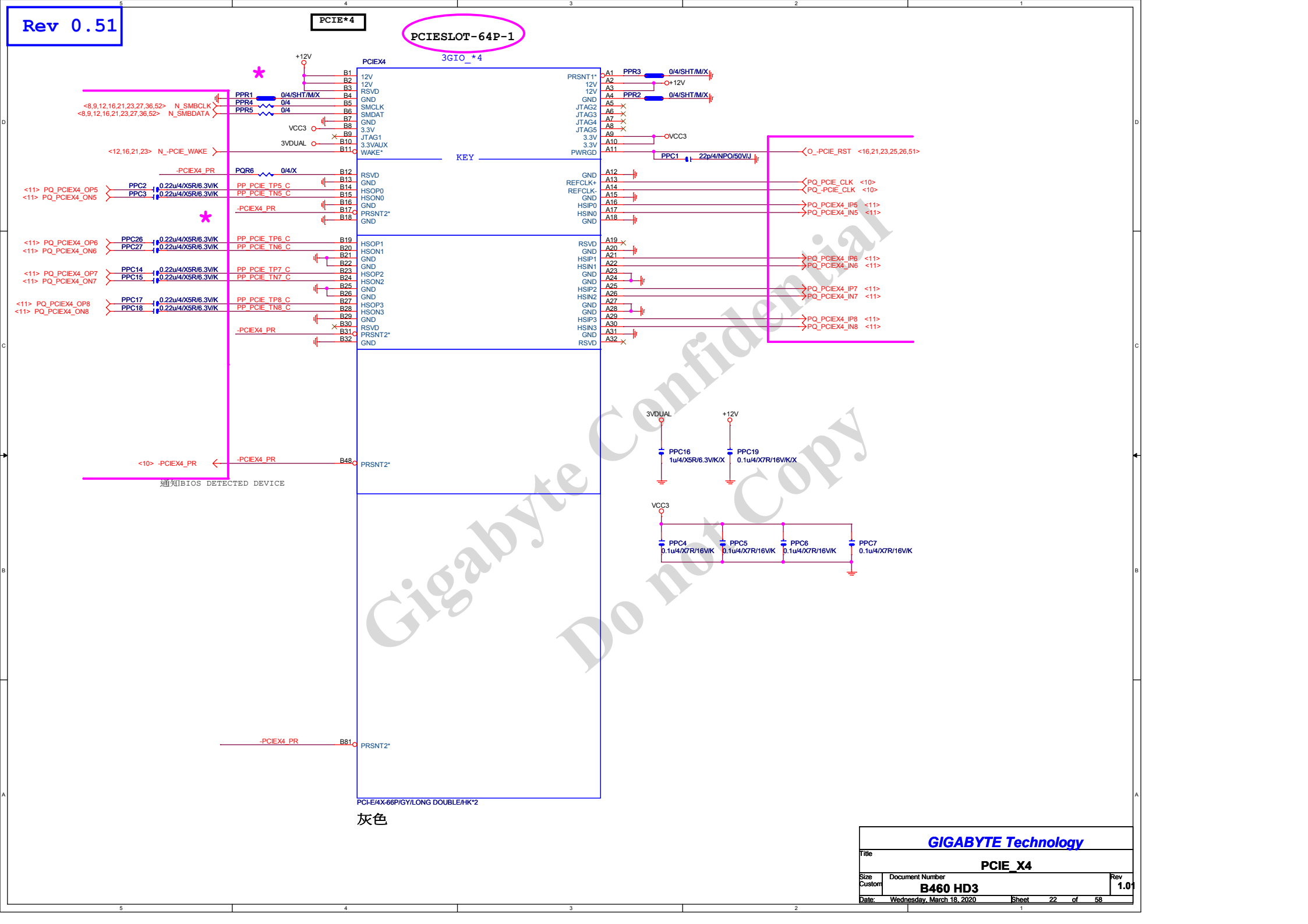
Rev 0.51

PCIE*4

PCIESLOT-64P-1

3GIO_*4



PCI-E/4X-66P/GY/LONG DOUBLE/HK*2

灰色

GIGABYTE Technology

Title: PCIE_X4

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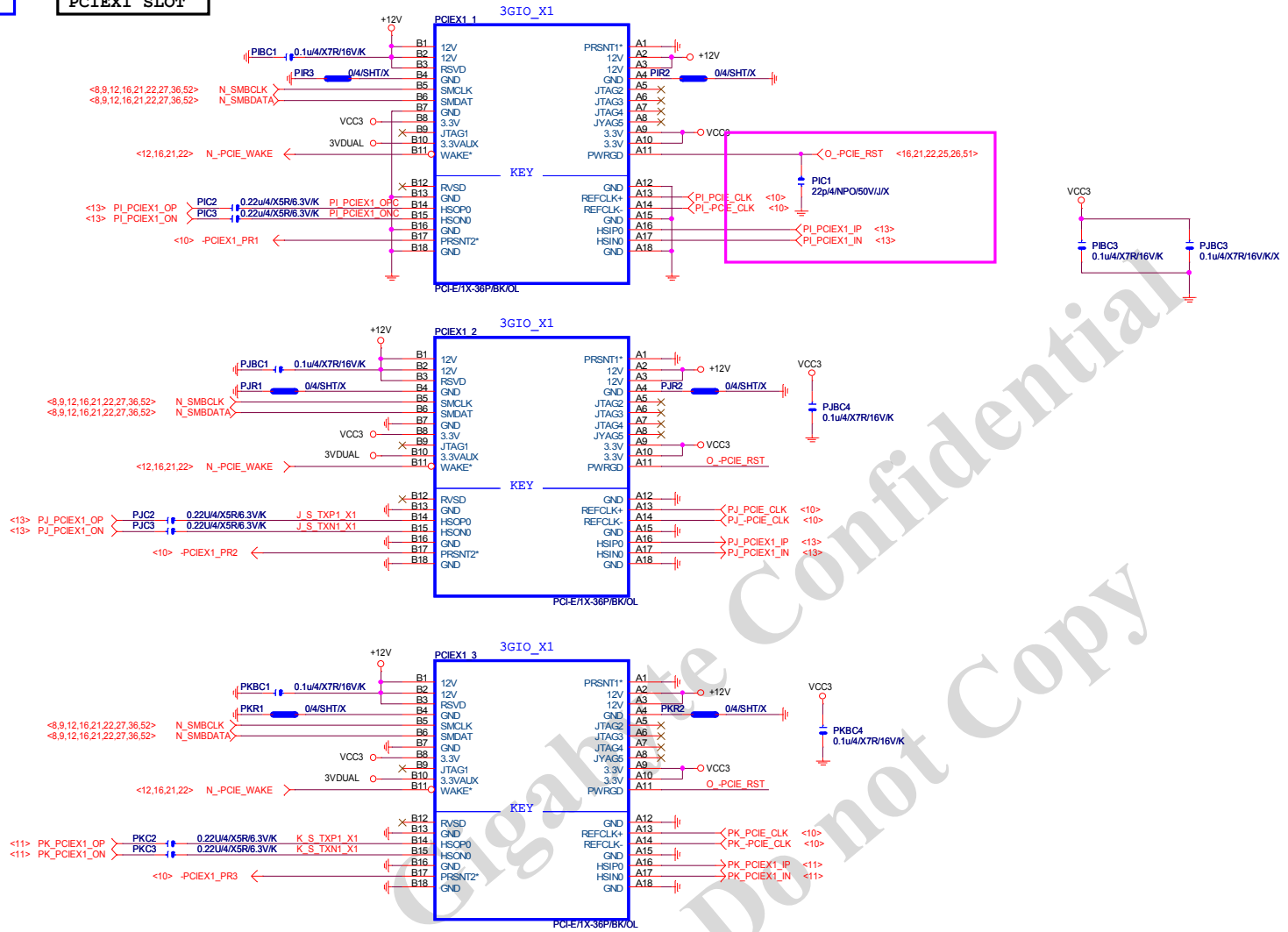
Rev 0.51

PCIEX1 SLOT



GIGABYTE Technology		
Title: PCIE_X4		
Size: Custom	Document Number: B460 HD3	Rev: 1.01
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GIGABYTE Technology

Title: SATA

Size	Document Number	Rev
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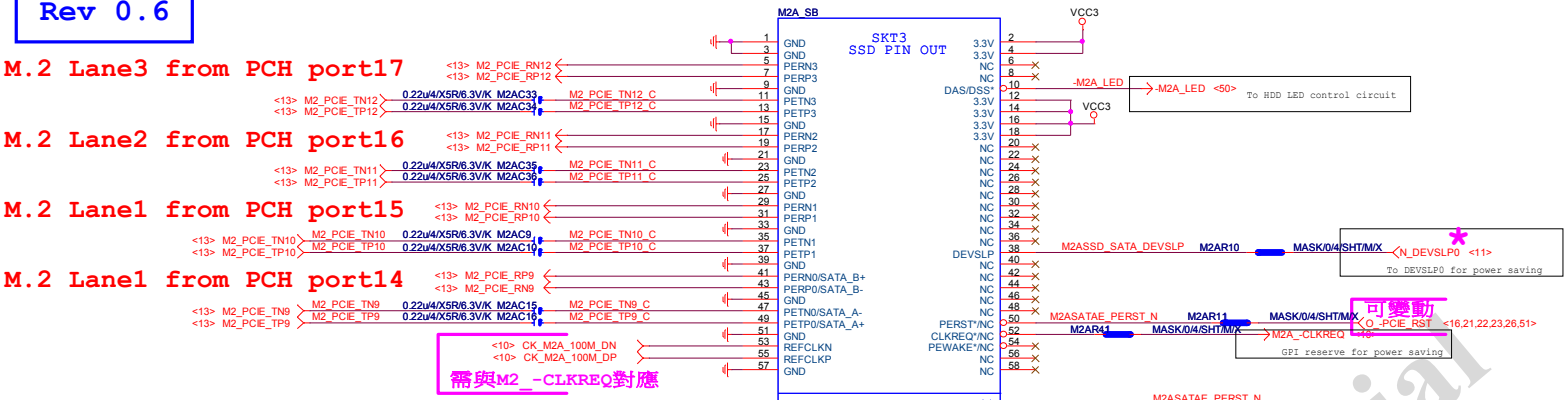
Rev 0.6

M.2 Lane3 from PCH port17

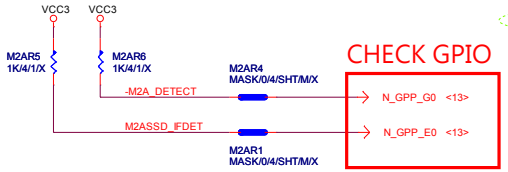
M.2 Lane2 from PCH port16

M.2 Lane1 from PCH port15

M.2 Lane1 from PCH port14

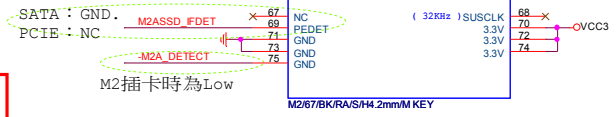


支援SATA and M.2 function

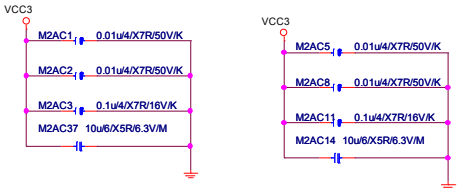


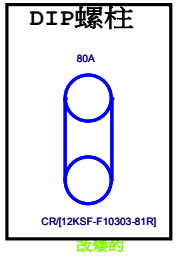
SATA : GND.
PCIE : NC

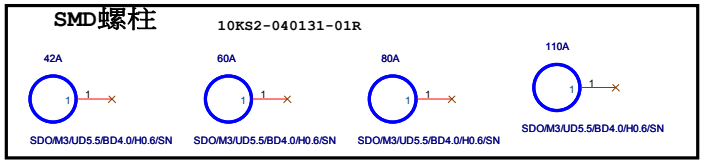
M2插卡時為Low



* footprint:
NGFF-M-75P-8CM-3A-SMD --> M2_80_H2MM8W







Footprint : HOLE_C236D165-A

GIGABYTE Technology		
Title: M.2 X4		
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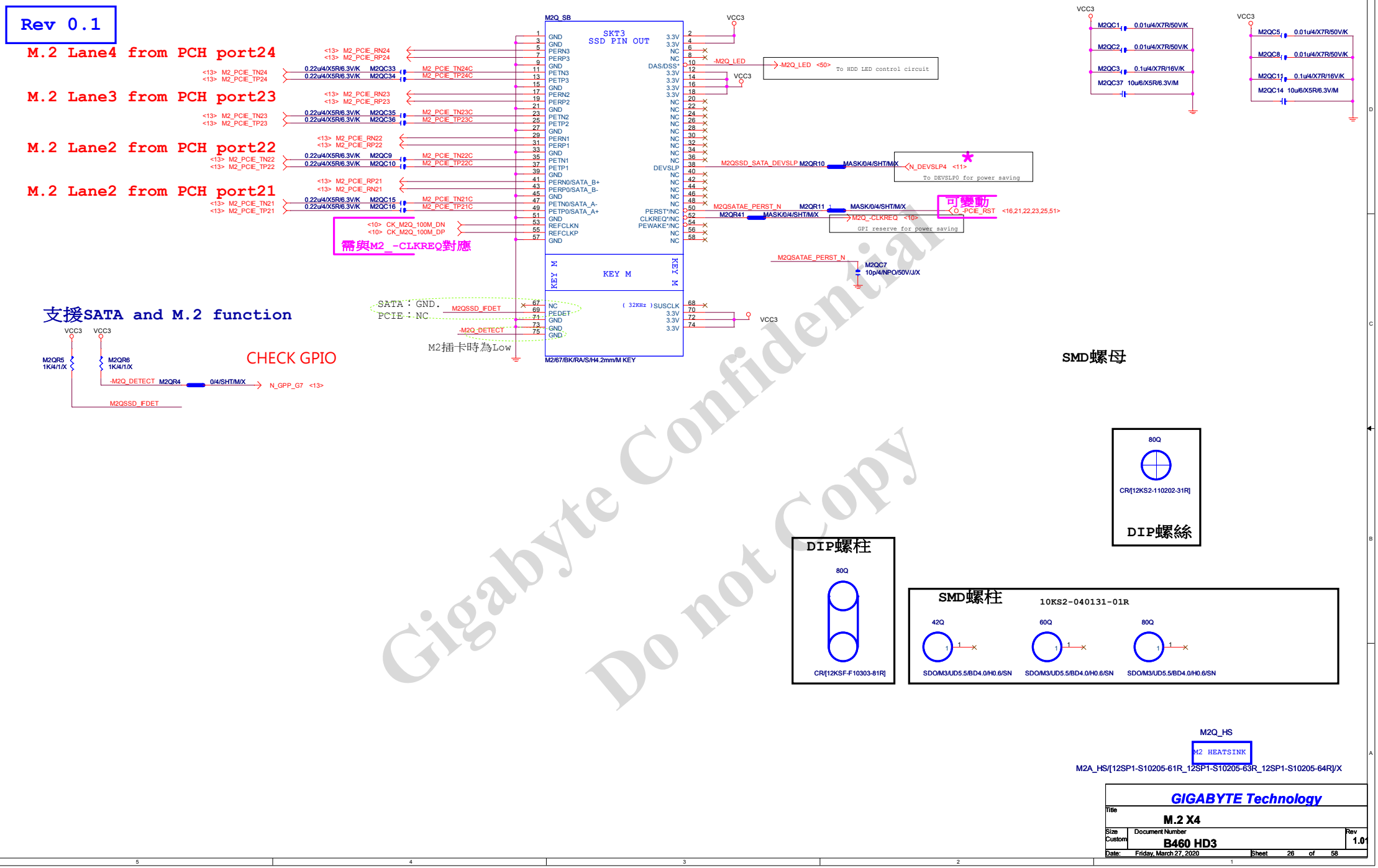

GIGABYTE Technology		
Title: M.2 X4		
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REV:0.11

CEC:DAR133.DAR132 上件.DAR18.DAR19.DAR23.DAR131不上件

non CEC:DAR133.DAR132 不上件.DAR18.DAR19.DAR23.上件.
DAR131改short pad
DAR131 short pad footprint:R0603-RH-SHORT30-MASK

VCORE_SIO — VCORE_VS MASK/0/4/SHT/M/X — VCORE
請注意擺放位置

201901002 Modify

DC-LL --> 2.1mohm

DC-LL --> 3.1mohm

VCORE	ISL95856	ISL95866
DAR137	X	V
DAR138	V	X
DAR139	X	V
DAC15	V	X
DAR79	V	X
DAR33	V	X

VCCGT	ISL95856	ISL95866
DAR140	X	V
DAR141	V	X
DAR142	X	V
DAC27	V	X
DAR80	V	X
DAR51	V	X

for ISL95856 DISABLE PH3

DAR44-->787 ohm
OCP-->200A

DAR71-->499ohm
OCP-->74A

CLOSE DA_DL1 DC SIDE

CLOSE PHASE 1 MOSFET

CLOSE DE_DL1 DC SIDE

CLOSE PHASE 1 MOSFET

CLOSE PWM

CLOSE PWM

connect to N_GPP_F12

ISL95866CHRZ-T/QFN-52

GIGABYTE™

Title: ISL95866_PWM

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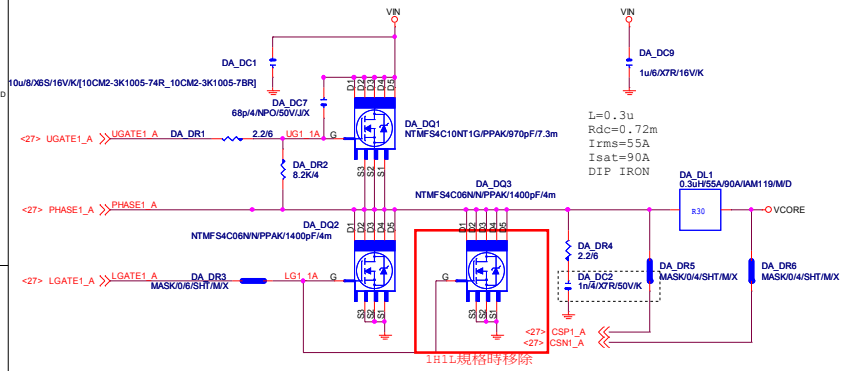
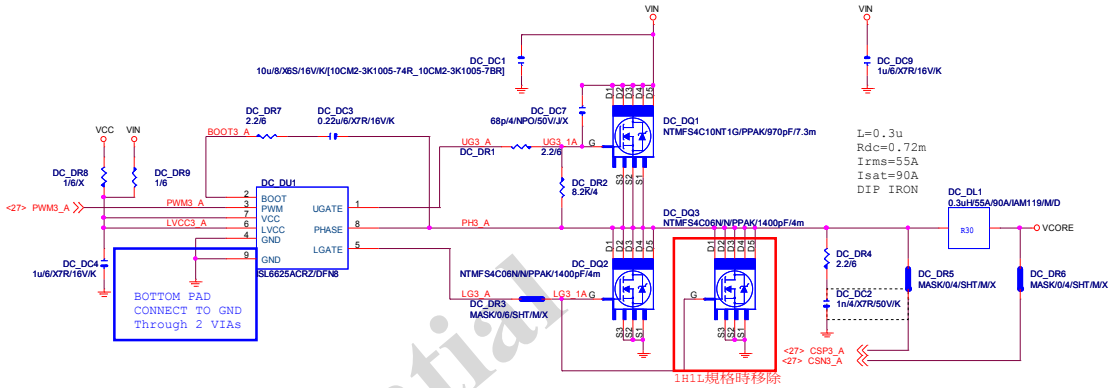
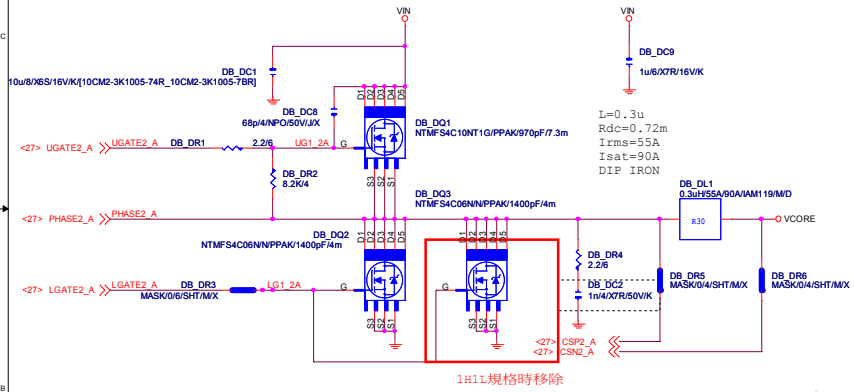
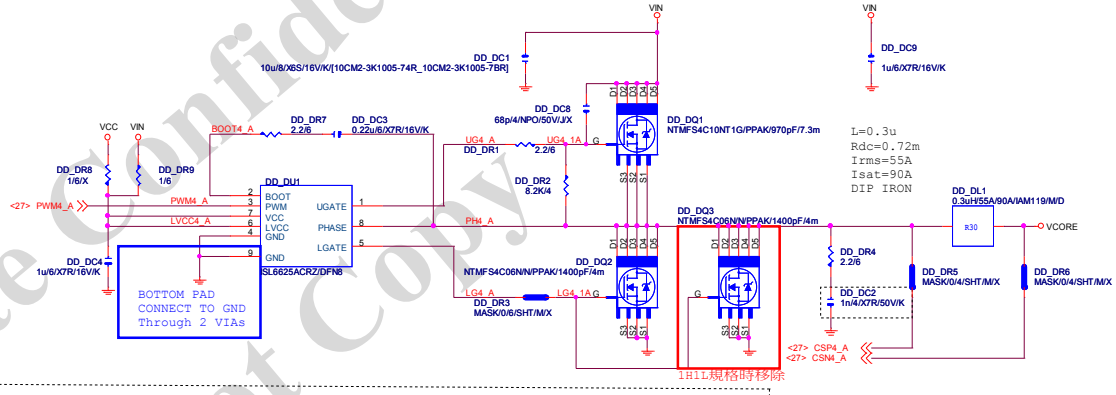
VCORE

CHOKE-R30M-jj1w-at



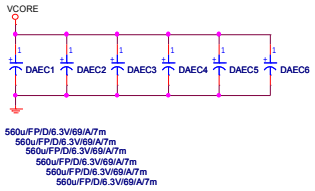


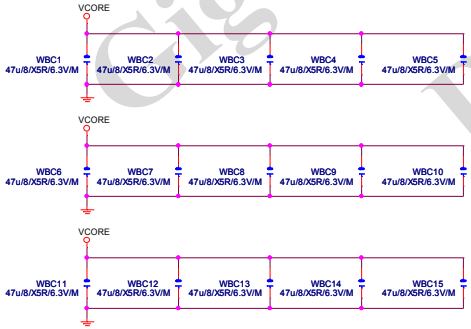


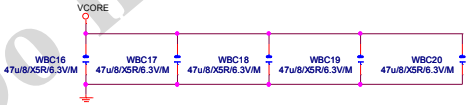


VCORE CAP

560u*6PCS
22u*20PCS



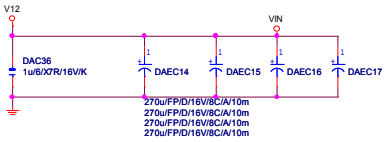




放CPU SOCKET (TOP LAYER)

VIN CAP

270u*4PCS



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Title	ISL95856_MOS	
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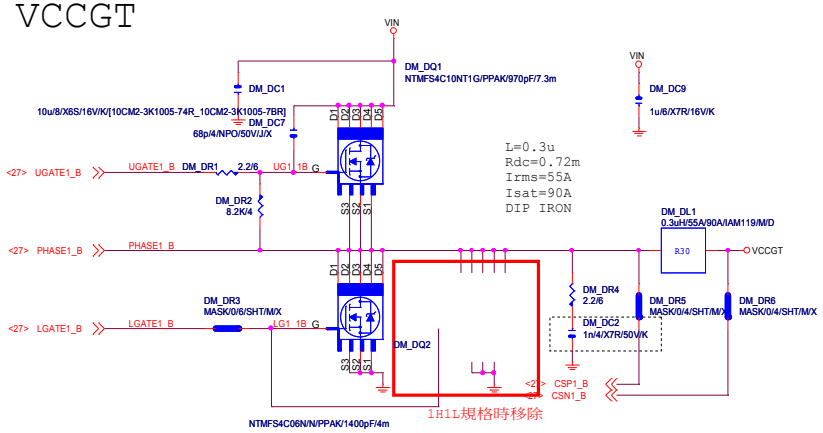
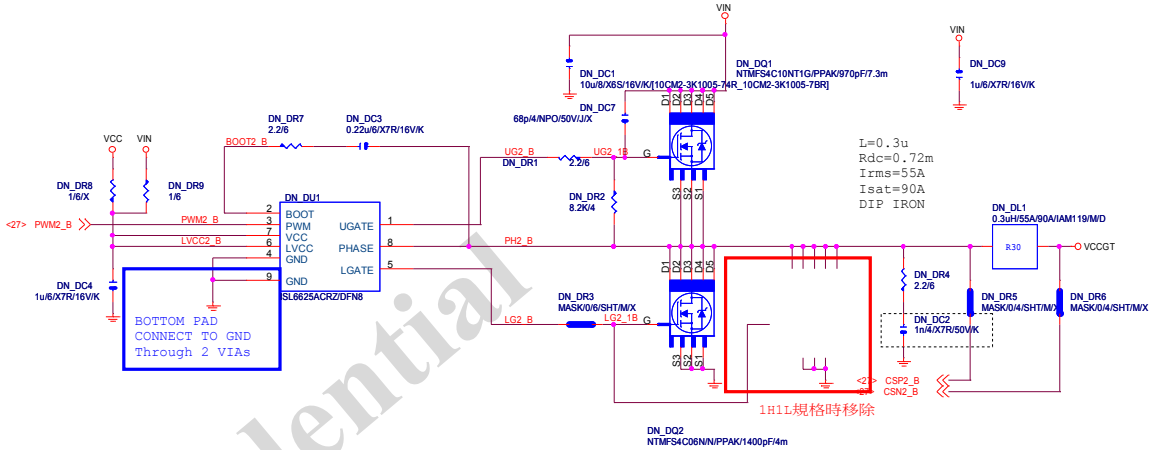
REV::0.55

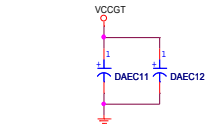
VCCGT



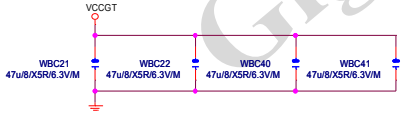


VCCGT CAP

560u*2PCS
22u*4PCS



560u/FP/D/6.3V/69/A/7m
560u/FP/D/6.3V/69/A/7m



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Title	ISL95856_MOS	
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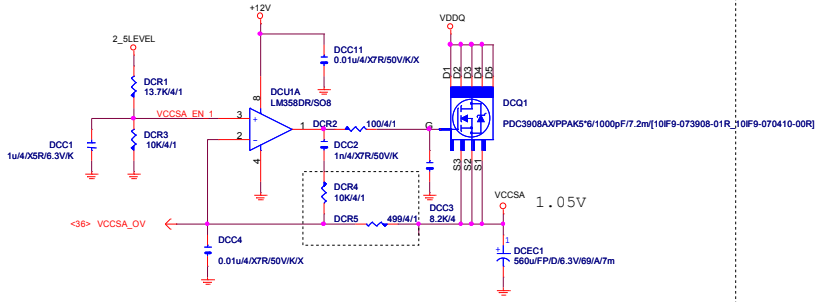
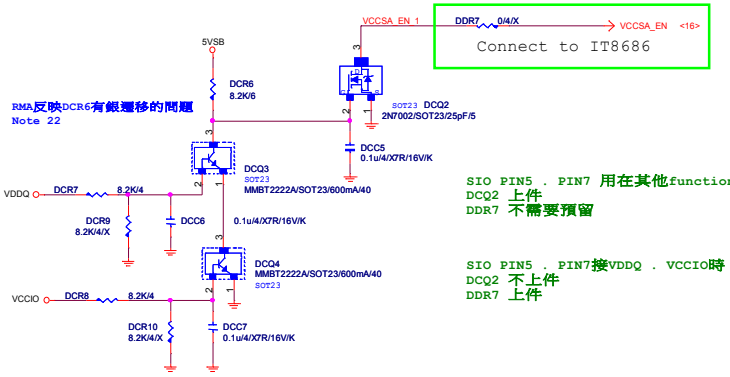
REV:0.3

VCCSA

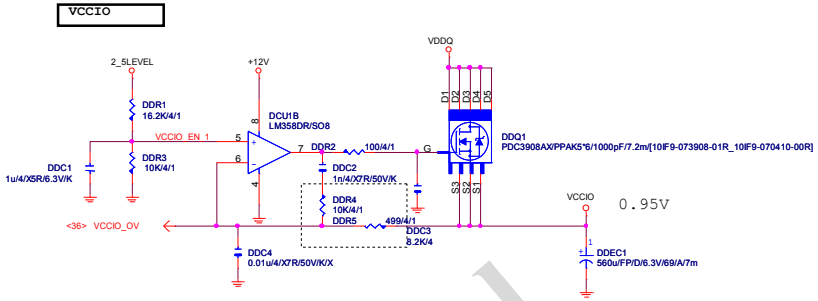


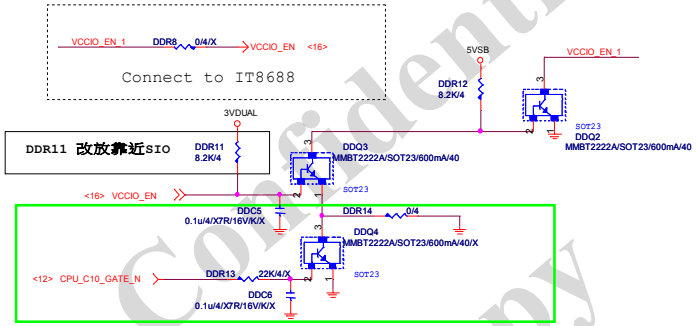


SIO PIN5 . PIN7 用在其他function時
DCQ2 上件
DDR7 不需要預留

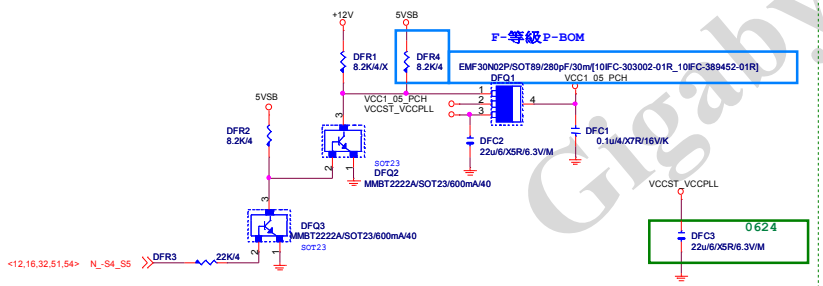
SIO PIN5 . PIN7接VDDQ . VCCIO時
DCQ2 不上件
DDR7 上件

VCCIO

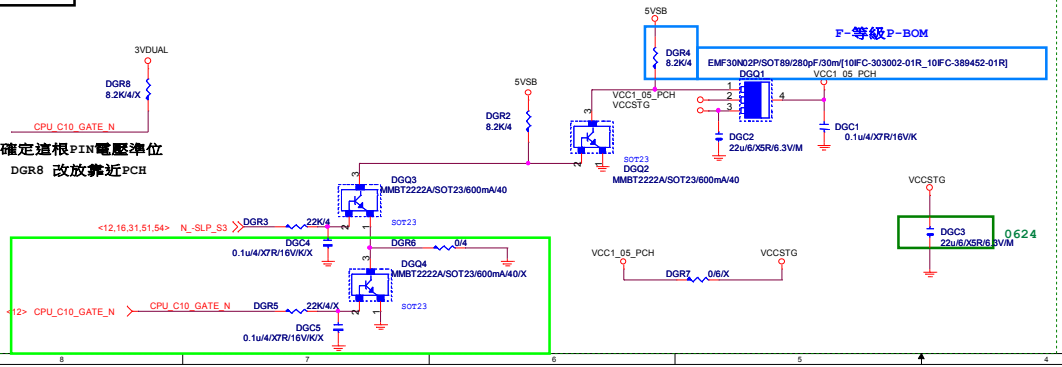




VCCST_VCCPLL



VCCSTG



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Title	VCCSA_VCCIO_no 44E	
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REV:0.3

DDR4

上件

MA_DR38.MA_DC15

VPP_25V使用8120.8068A.RT8237時上件

DDR VIN CAP
560u*2PCS

CHOKE與CAP料號可變

note 6
10IF9-070410-00R+10IF9-040406-10R
自動插件 CHOKE05U-40A-1PQ-AT

SUPPORT DDR4

1.2V

25A MAX

L=1u
DCR=2.5 mohm
Isat=35A
Idc=28A

請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

Remote sense請從最重的負載端點拉回

PIN7-->20mil
PIN1-->6mil
PIN2-->6mil
PIN5-->6mil
PIN3-->6mil

FS=290K
OCP=40A

MOSFET請依MOSFET使用規則.自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKSO8/2070pF/4.3m]

PWR SEQ

CLOSE TO DDR POWER PLANE

For power sequence require

VPP_25V使用8120時上件

MAU1上RT9045時上件(不可MASK)

DDRVTT

NCT3103S/SOP8/2A/[10GL2-203103-01R]

1.1A MAX

DDR CAP 560u*4PCS 22u*2PCS

* 大電容 x4

Footprint
EC6D8MM-RH-2

DDRVTT CAP

* 大電容 x0

GIGABYTE

Title	RT8237_DDR4 POWER	
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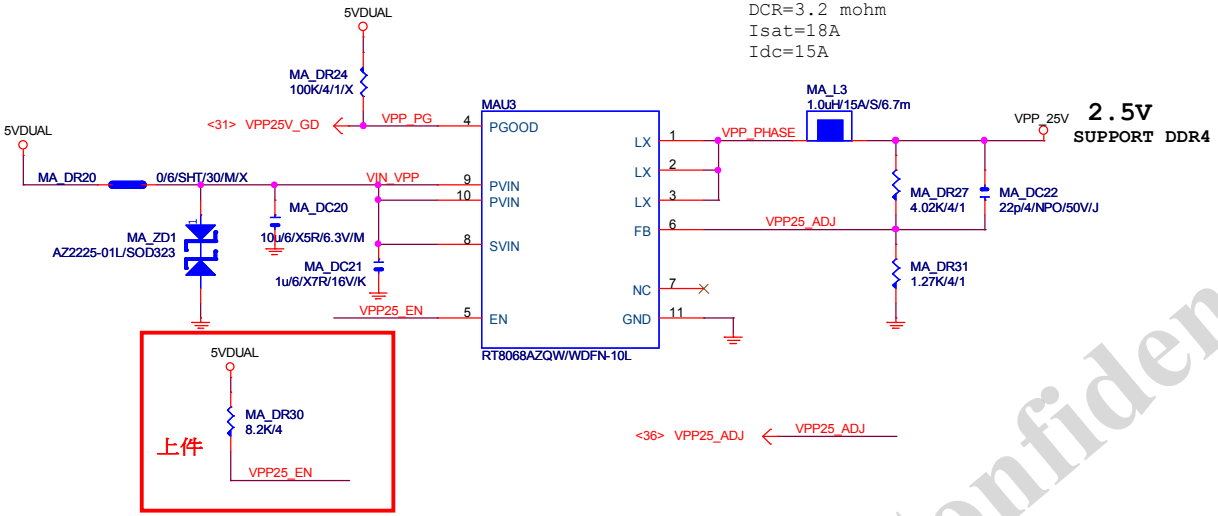
REV:0.1

VPP_25V

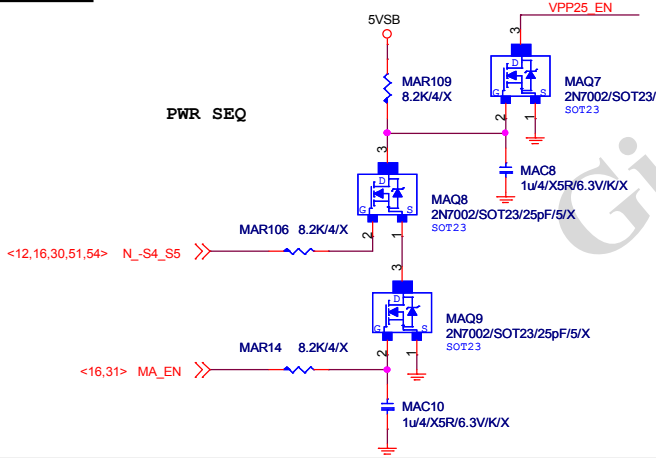
CHOKE與CAP料號可變

L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

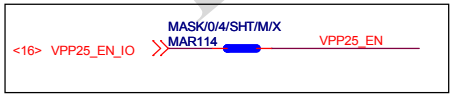


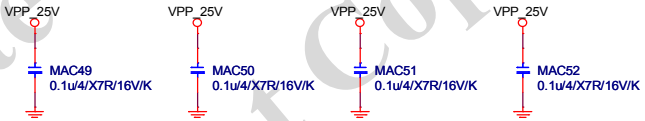
PWR SEQ

* 刪 MA_DR32



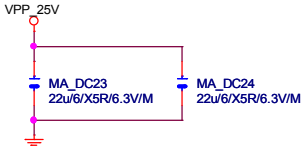
<== VPP25_EN CTRL by SIO, 外部線路不上件, 1014 modify





VPP CAP 22u*1PCS

* 大電容 x0



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Title	RT8068A_VPP25 POWER	
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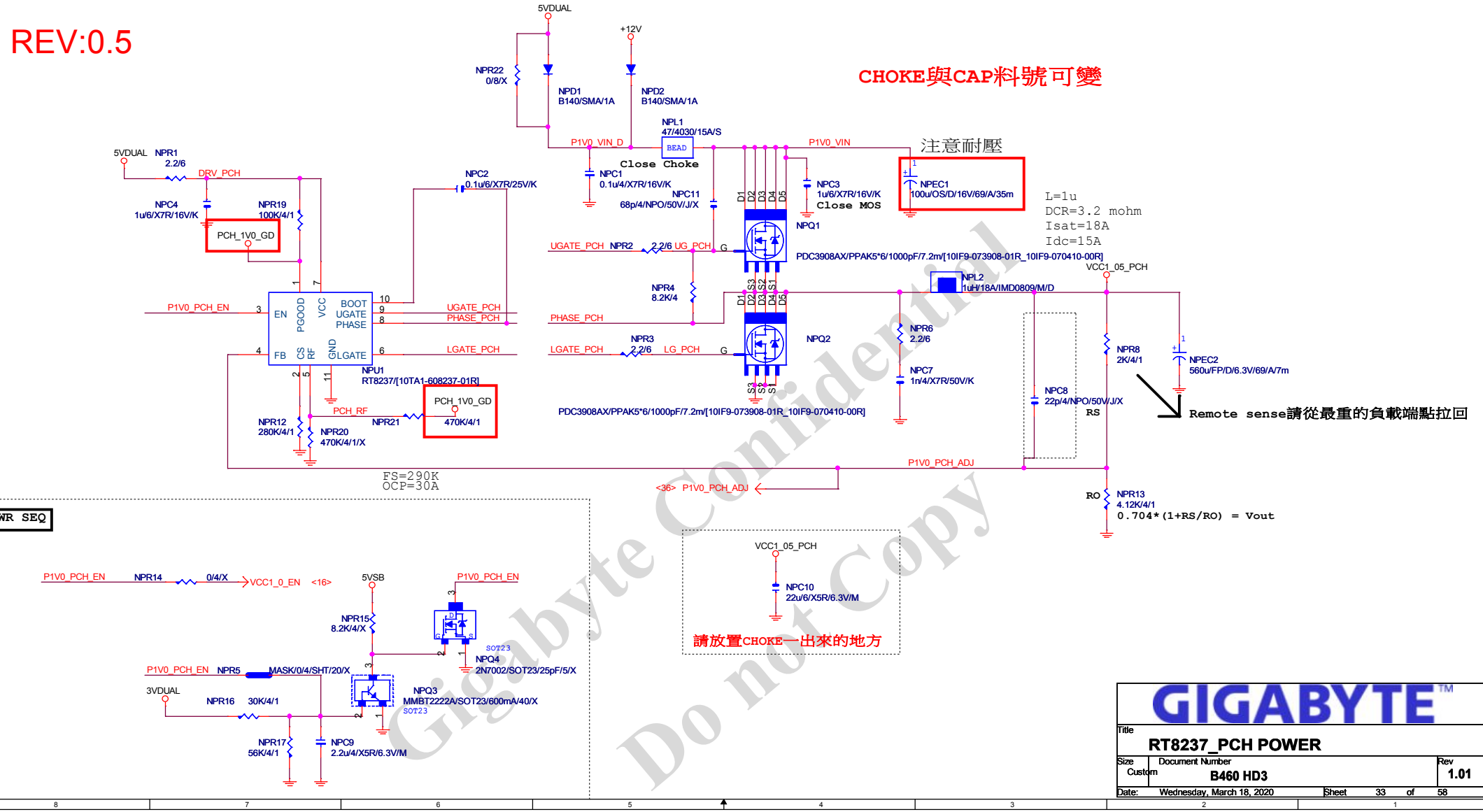
REV:0.5



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Title	RT8237_PCH POWER	
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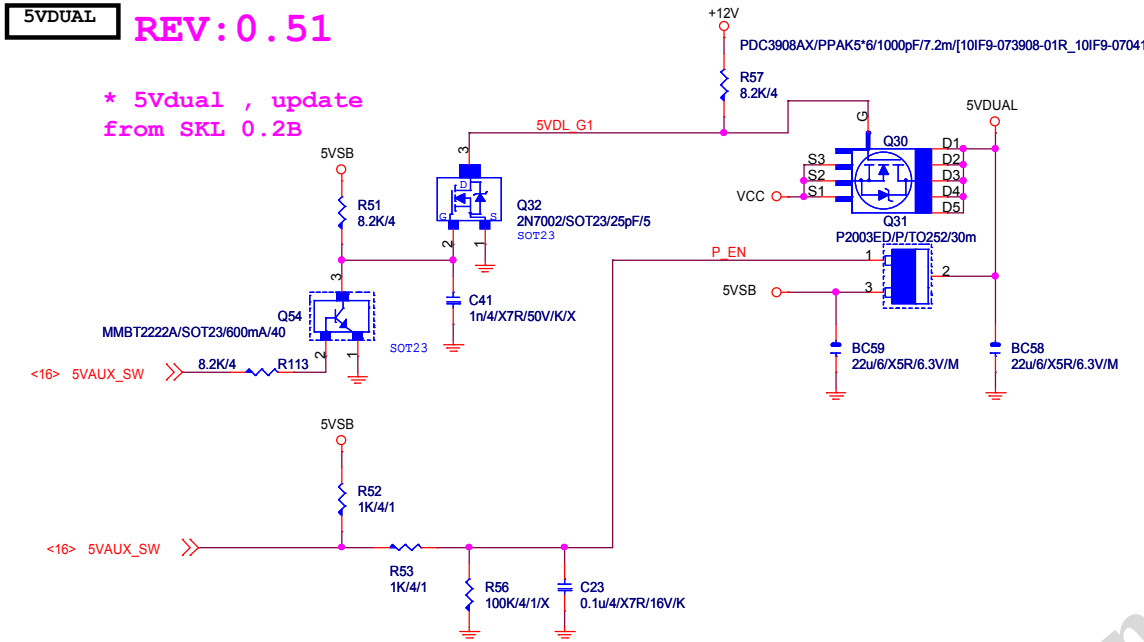
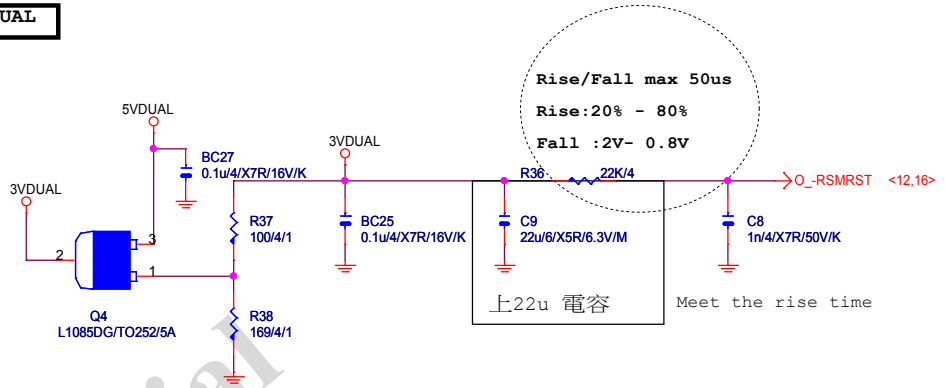
5VDUAL

REV:0.51

* 5Vdual , update from SKL 0.2B



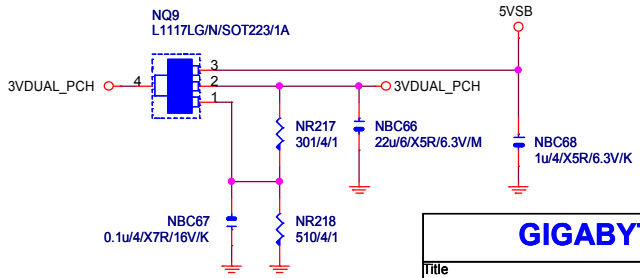
3VDUAL



O_-RSMRST （不上件）

20191014 Removed ,ref B460M-D2V

3VDUAL_PCH



GIGABYTE Technology

Title: DISCRETE POWER

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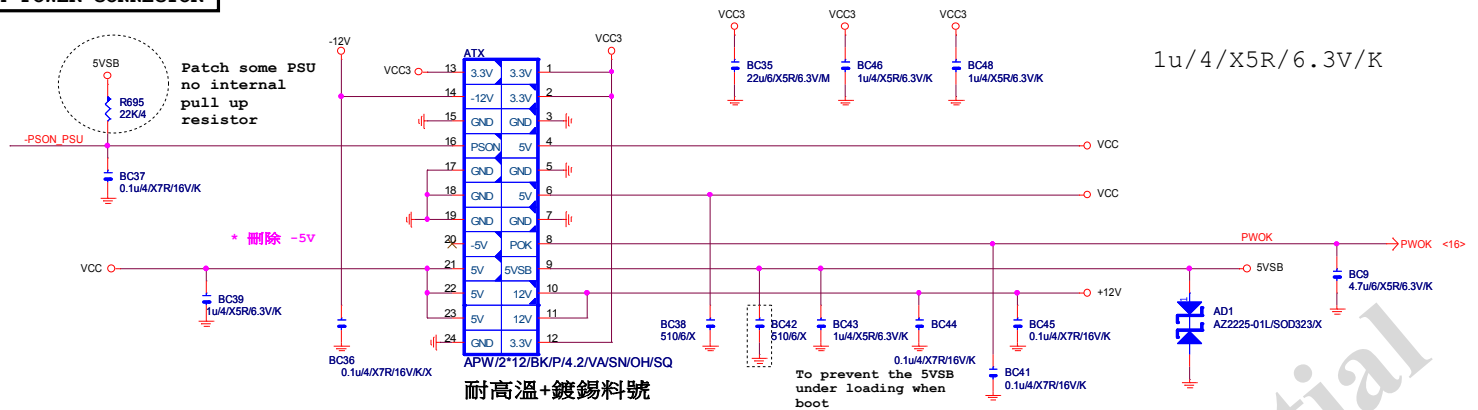
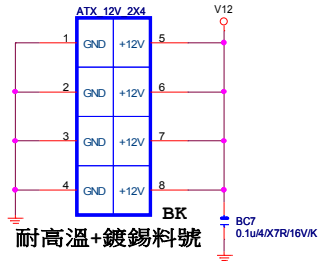
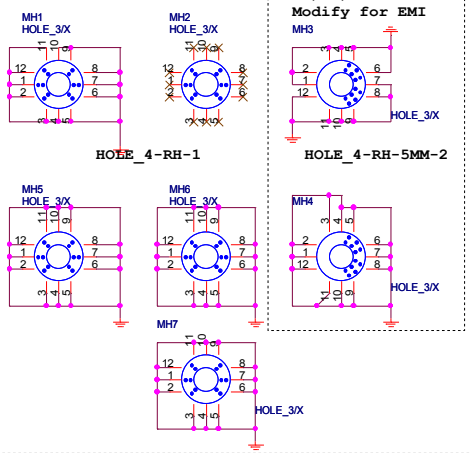
ATXX24 POWER CONNECTOR



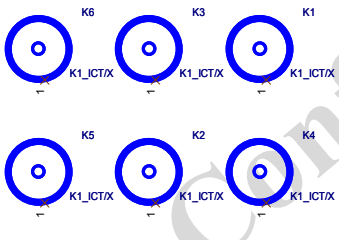
ATXX4 POWER CONNECTOR

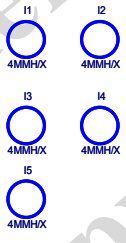


螺絲孔

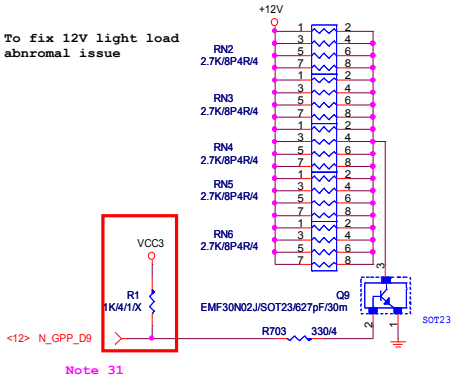


固定孔/光學點



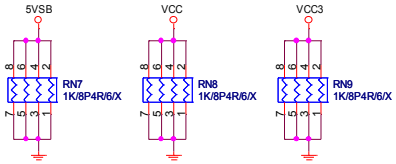


+12V DUMMY LOAD

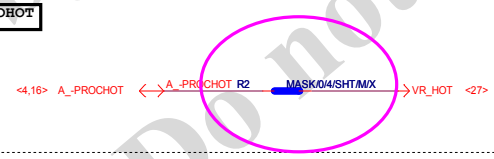


【技術通報R&D技術通報153】

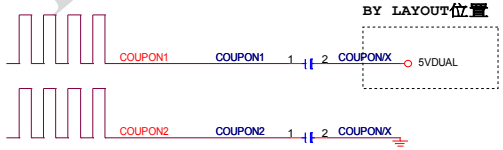
DUMMY LOAD

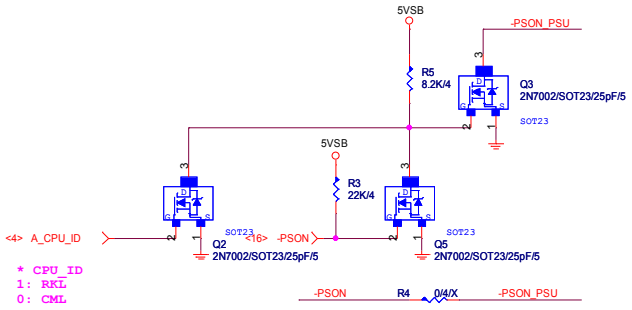


-PROHOT



COUPON





GIGABYTE Technology		
Title: ATX POWER CONNECTOR		
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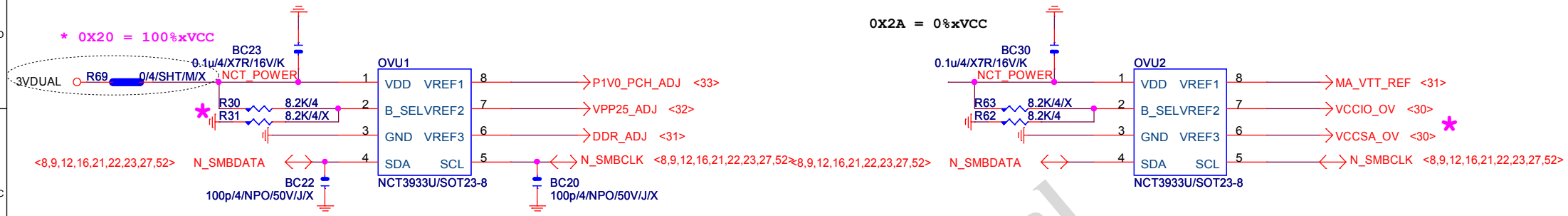
OVER VOLTAGE



NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

GIGABYTE Technology

Title: CPU CORE VR-2

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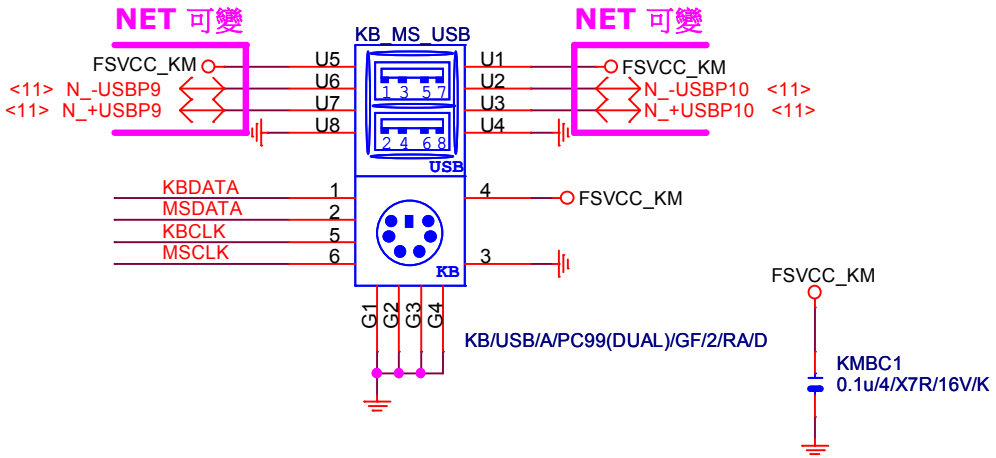
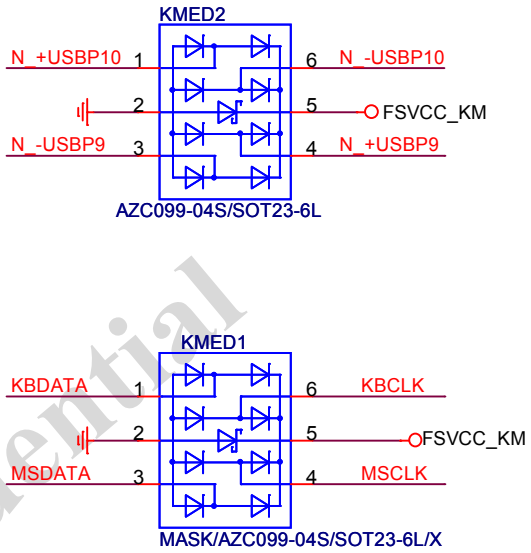
KB_MS_USB

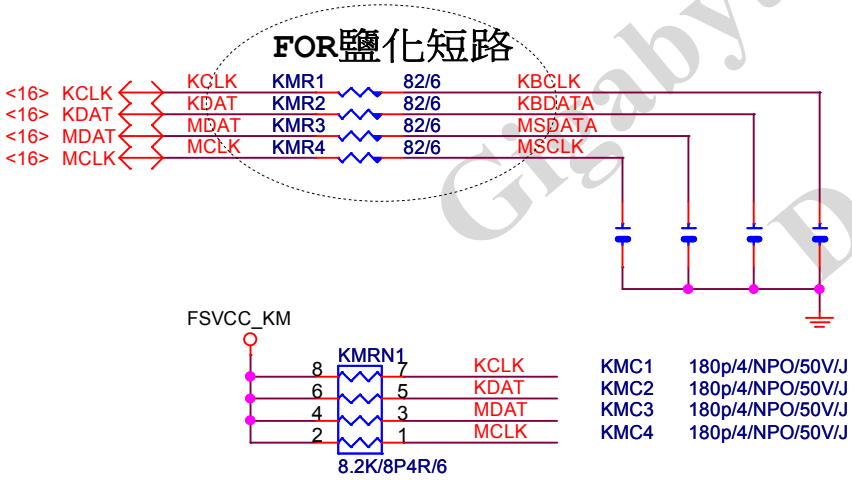
Rev: 0.7



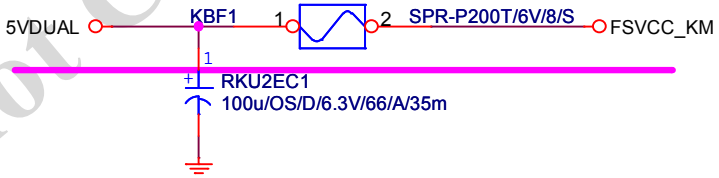
ESD



KB_MS_USB DAMPING/PU



KB_MS_USB PWR



USB OC PROTECT

GIGABYTE Technology		
Title: KB_MS_USB		
Size: A	Document Number: B460 HD3	Rev: 1.01
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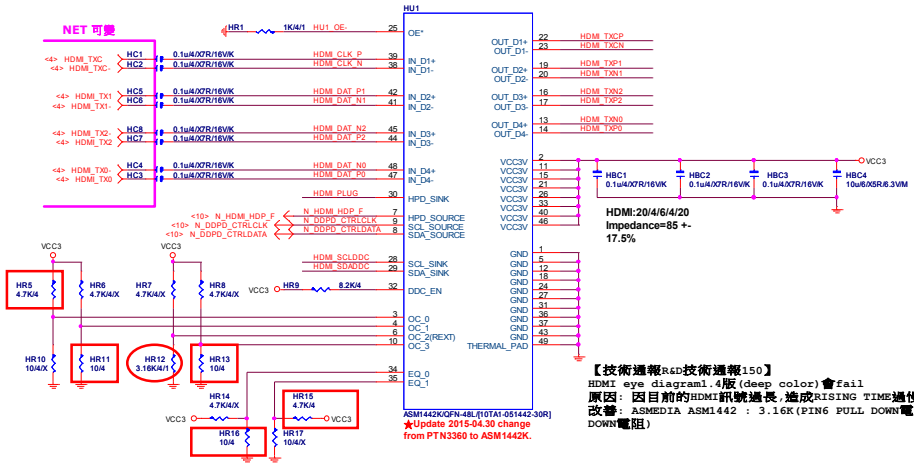
HDMI LEVEL SHIFT

Rev: 0.7



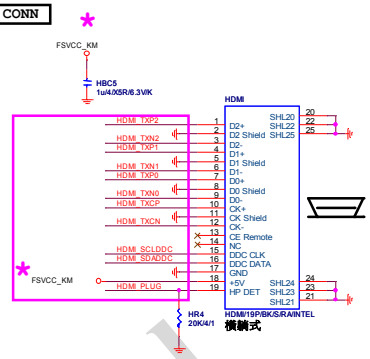
【技術通報R&D技術通報150】
HDMI eye diagram1.4版(deep color)會fail
原因：因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善：ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K

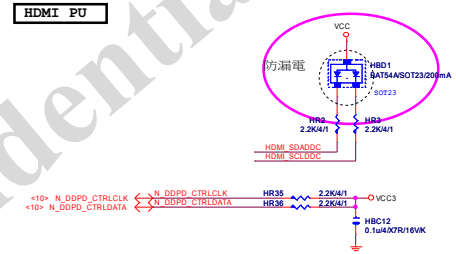
ASM1442:紅色框要上,HR12:3.16K

【技術通報R&D技術通報150】
HDMI eye diagram1.4版(deep color)會fail
原因：因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善：ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

HDMI CONN

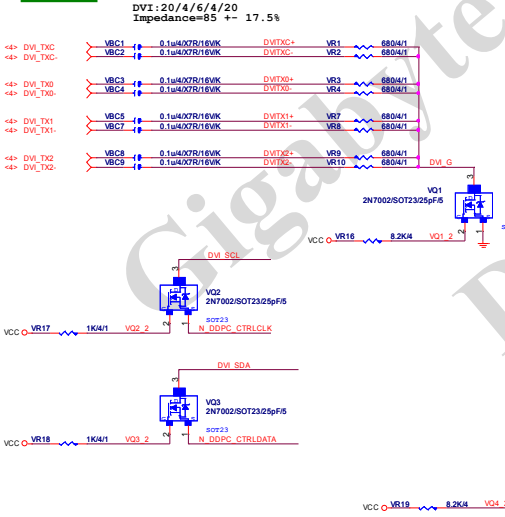


HDMI PU

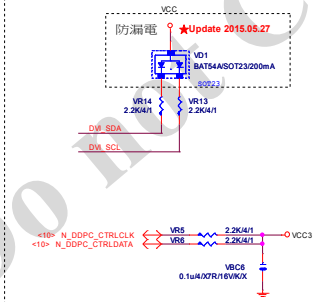


DVI

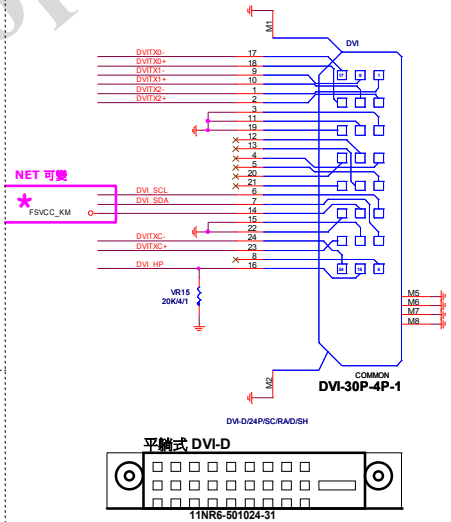
Rev: 0.8



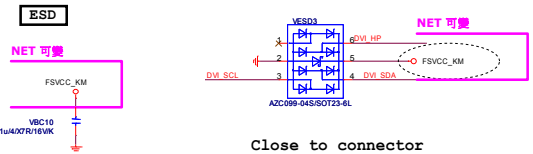
DVI PU



DVI CONN

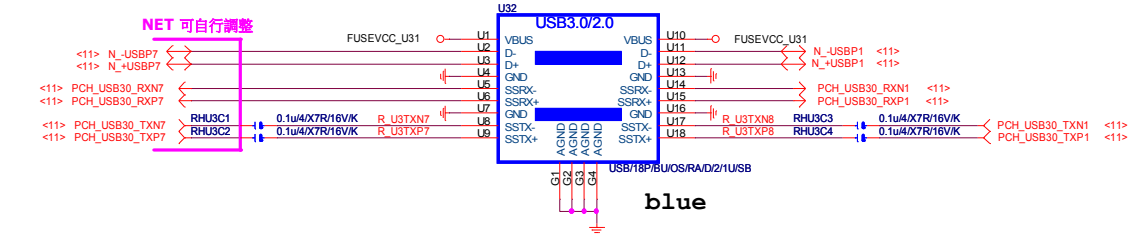


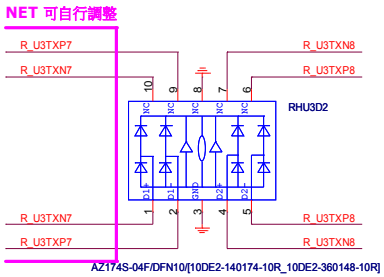
ESD

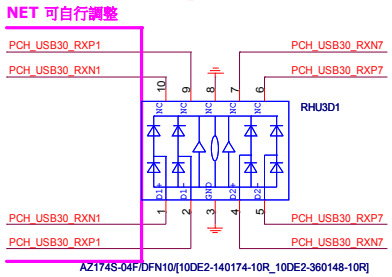


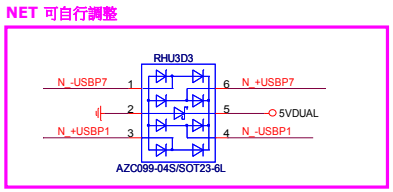
Title	GIGABYTE Technology		
	HDMI		
Size	Document Number		Rev
Custom	B460 HD3		1.01
Date:	Friday, March 27, 2020	Sheet 38 of 58	

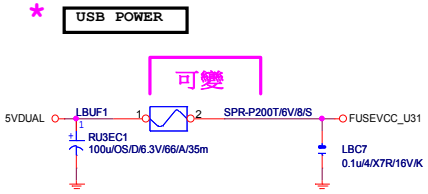
GIGABYTE Technology		
Title: DVI		
Size: Custom	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 39 of 58	

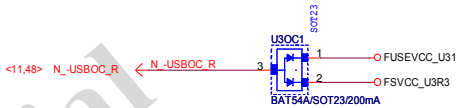










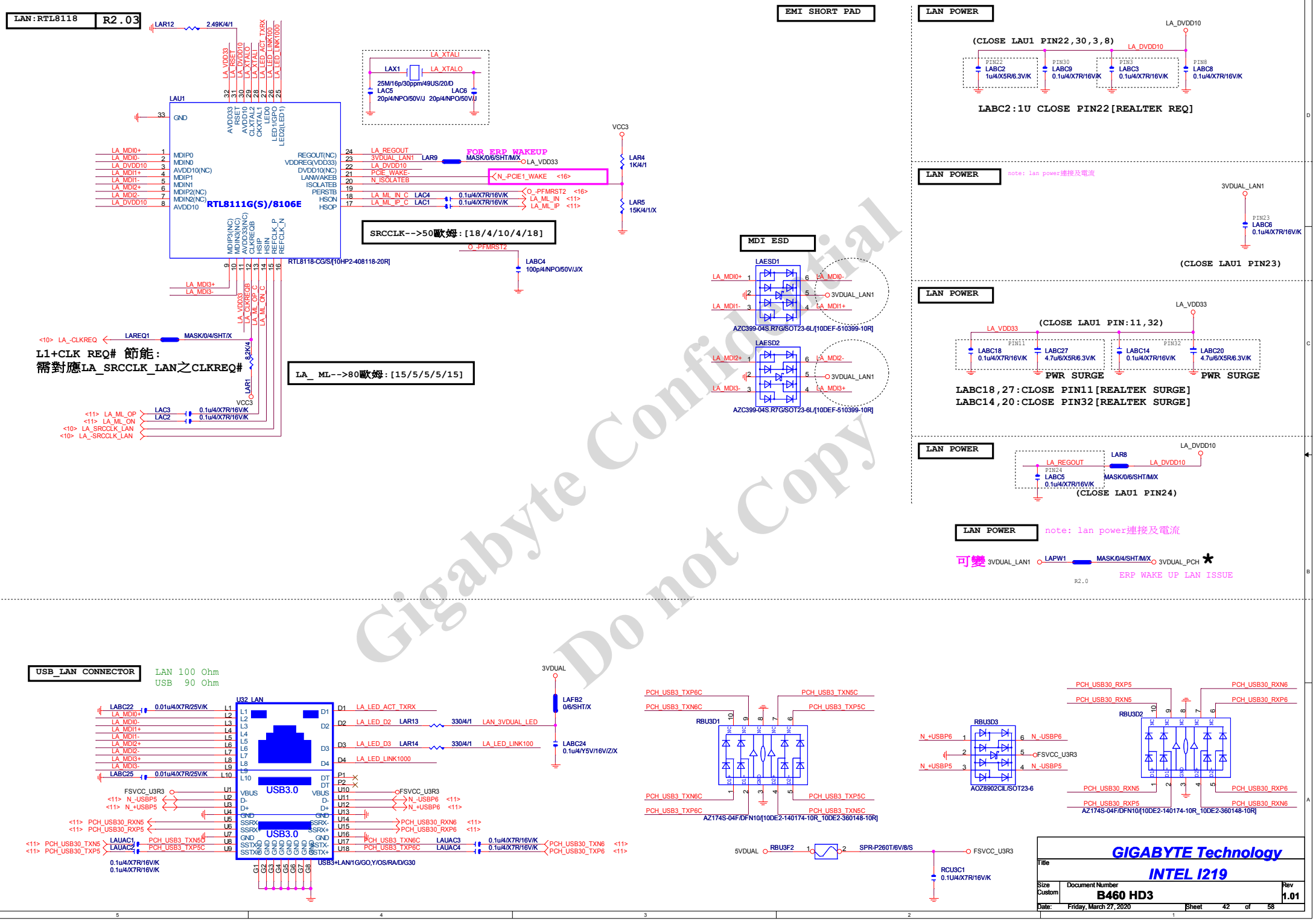


GIGABYTE Technology

Title	R_USB30,USB_OC		
Size: Custom	Document Number: B460 HD3		Rev: 1.01
Date: Friday, March 27, 2020	Sheet 40 of 58		

GIGABYTE™

Title	TUSB321_Front	
Size: C	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 41 of 58	



GIGABYTE Technology		
Title: LAN CONNECTOR-I219		
Size: Custom	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 43 of 58	

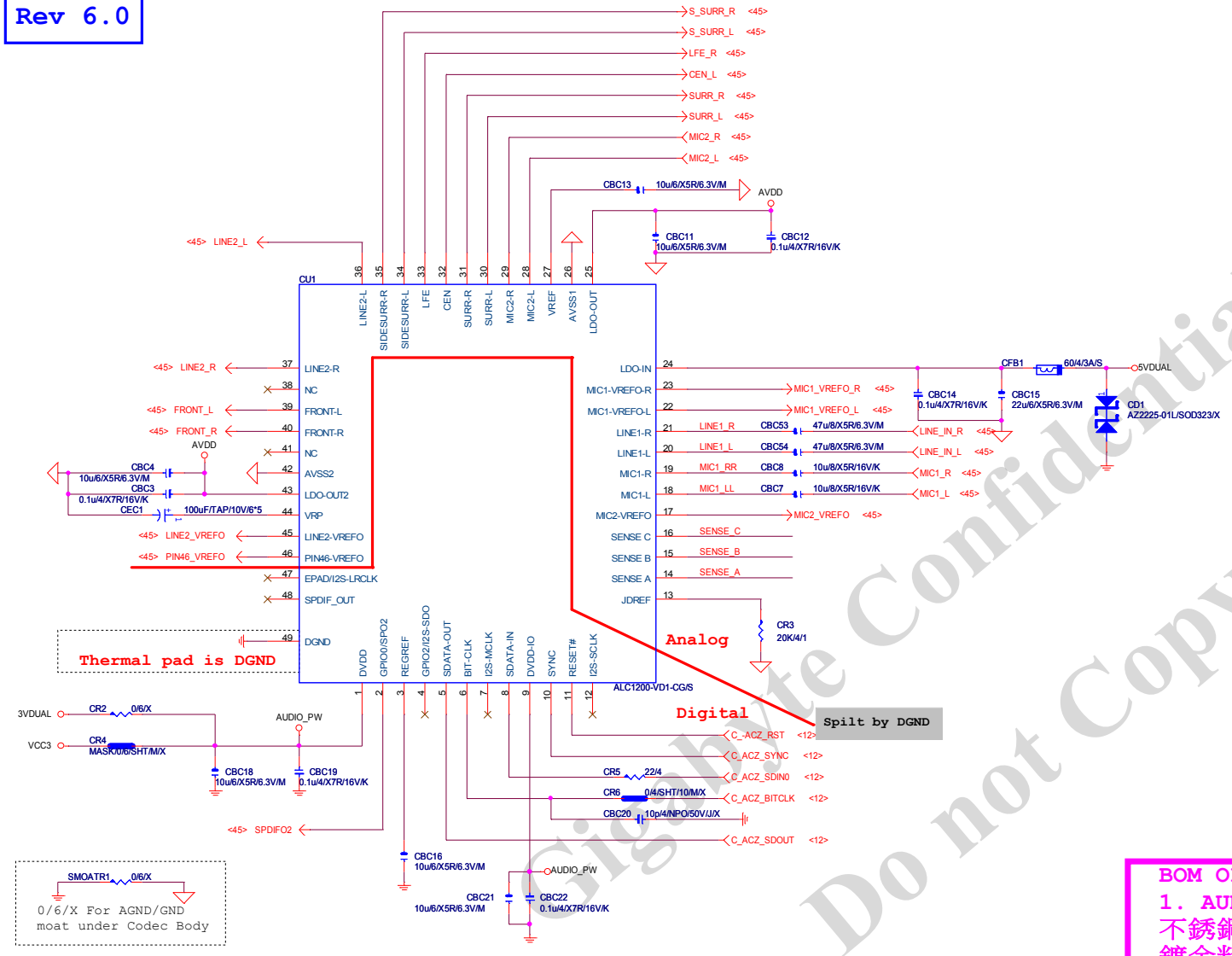
Rev 6.0

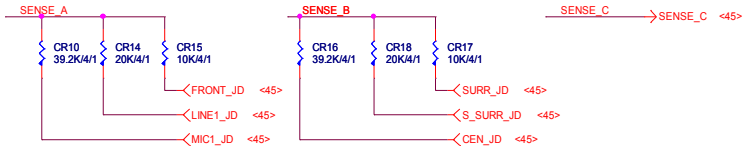
LAYOUT注意:螺絲孔下GND方式
1. MH1下DGND
2. MH2一律改為Isolate

MH1	MH2
DGND	Isolate

LAYOUT注意:是否要加?
AGND切割線

音效區域印刷





BOM OPTION :
1. AUDIO CONNECT
不銹鋼料號:11NR6-403025-A3R
鍍金料號:11NR6-403025-92R
全黑料號:11NR6-403025-B1R
2. AUDIO CAP
Nichicon MW音效電容 : 100u/TAP/6.3V/65
Chemicon音效電容 : 100uF/TAP/10V/6*5

GIGABYTE

Title	ALC1220	
Size: Custom	Document Number: B460 HD3	Rev: 1.01
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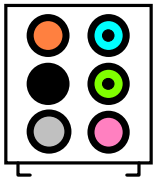
Rev 6.0

AZALIA JACK

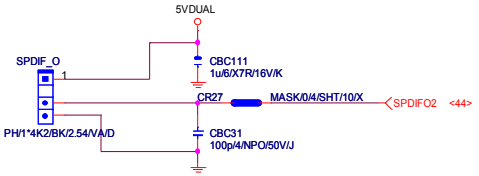


MOATR1 0/4
MOATC1 0.1u/4/X7R/16V/K → Near F_AUDIO

MOATR2 0/4/X
MOATC2 0.1u/4/X7R/16V/K → Near Codec

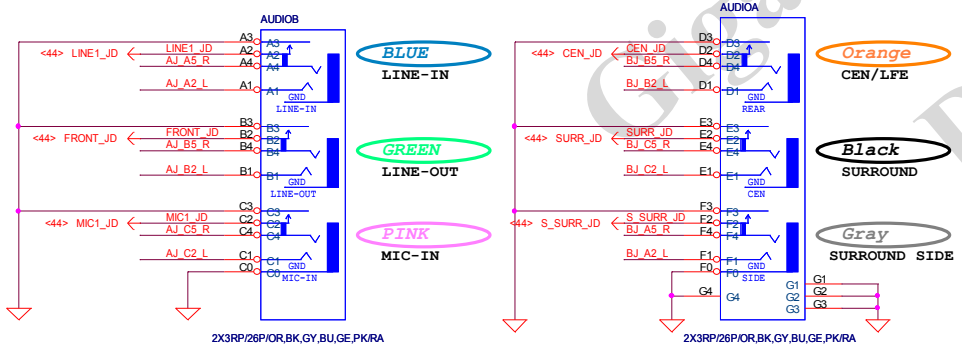
MOATR3 0/4/X
MOATC3 0.1u/4/X7R/16V/K → Under Audio Jack

MOATR4 2.2/6 → Audio Jack - LAN



For HDMI SPDIF （依SPEC保留或移除）

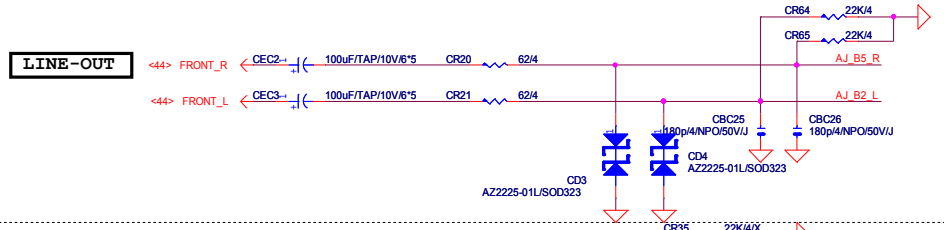
AZALIA JACK



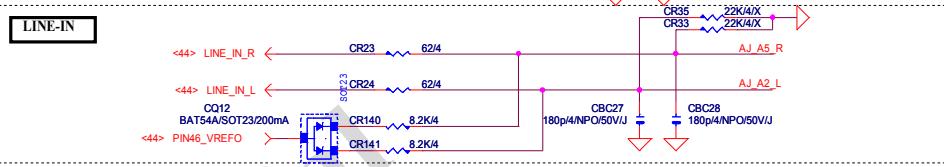
2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

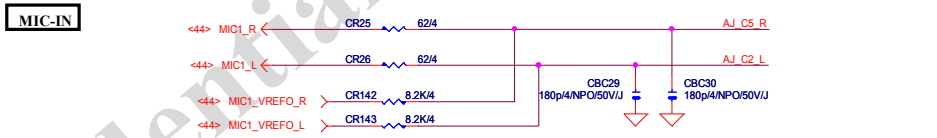
LINE-OUT



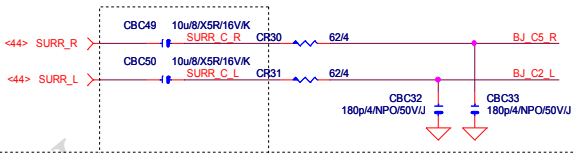
LINE-IN



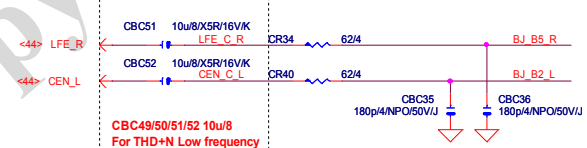
MIC-IN



SURROUND

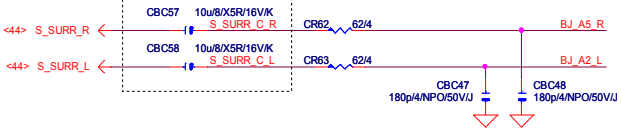


CEN/LFE

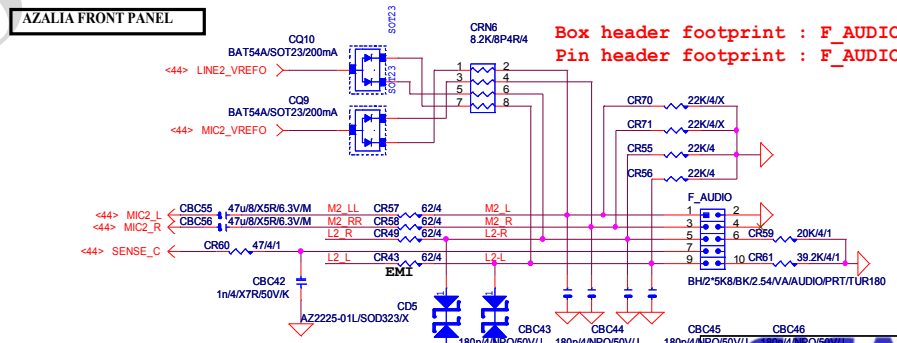


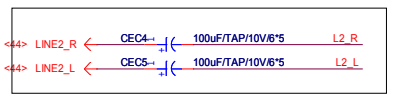
CBC49/50/51/52 10u/8
For THD+N Low frequency

SURR BACK



AZALIA FRONT PANEL





GIGABYTE

Title	AUDIO JACK	
Size: Custom	Document Number: B460 HD3	Rev: 1.01
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GIGABYTE™

Title: IT5702		
Size: C	Document Number: B460 HD3	Rev: 1.01
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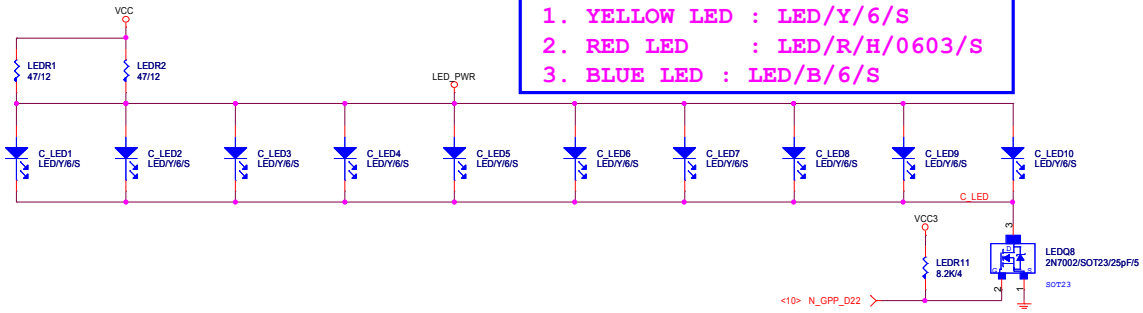
BOM OPTION :
1. YELLOW LED : LED/Y/6/S
2. RED LED : LED/R/H/0603/S
3. BLUE LED : LED/B/6/S



Ambient LED Control

	N_GPP_D22
Still Mode	H
OFF Mode	L

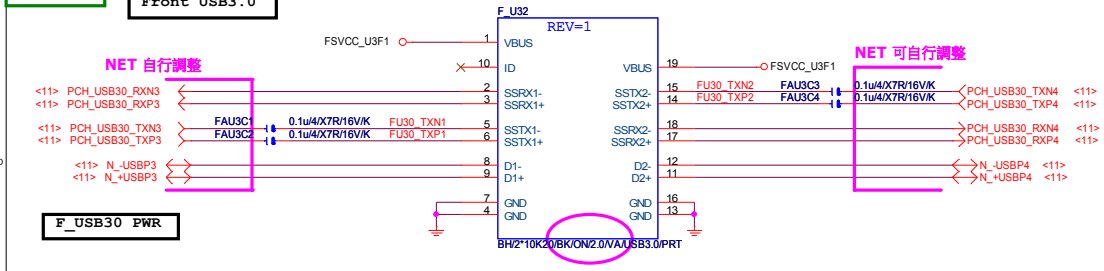
GIGABYTE™

Title: Amient Single LED		
Size: Custom	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 47 of 58	

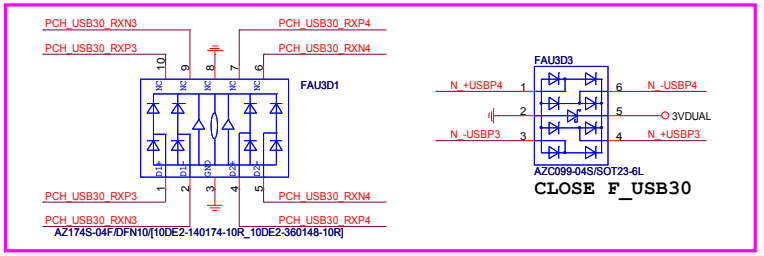
Rev: 0.7

Front USB3.0

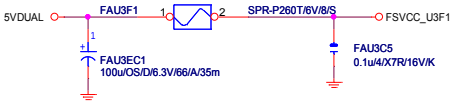
NET 自行調整

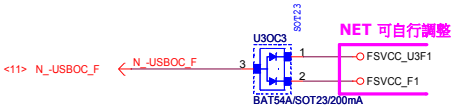


NET 可自行調整

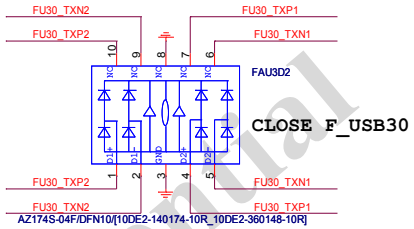


F_USB30 PWR





NET 可自行調整

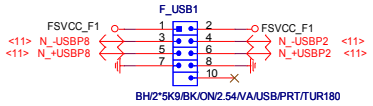


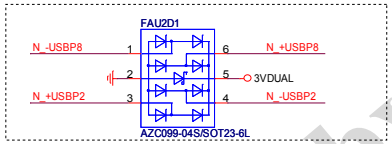
Rev: 0.7

FRONT USB1

NET 可變

FUSB2X5-HS



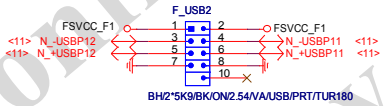


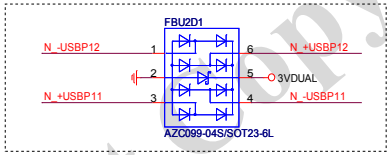
Close to connector

FUSE 2 Port 1 Fuse 2A

FRONT USB2

FUSB2X5-HS



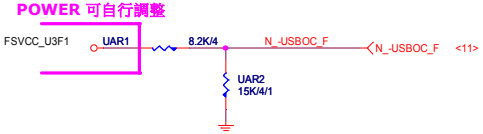


Close to connector

FUSE 2 Port 1 Fuse 2A

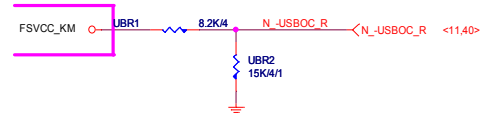
-USBOC_F

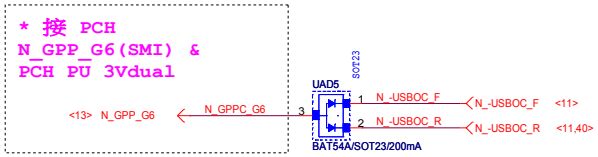
POWER 可自行調整



-USBOC_R

POWER 可自行調整





GIGABYTE Technology

Title: R_USB30,F_USB30, USB_OC

Size: Custom | Document Number: B460 HD3 | Rev: 1.01

Date: Wednesday, March 18, 2020 | Sheet 48 of 58

GIGABYTE Technology

Title: USB2.0

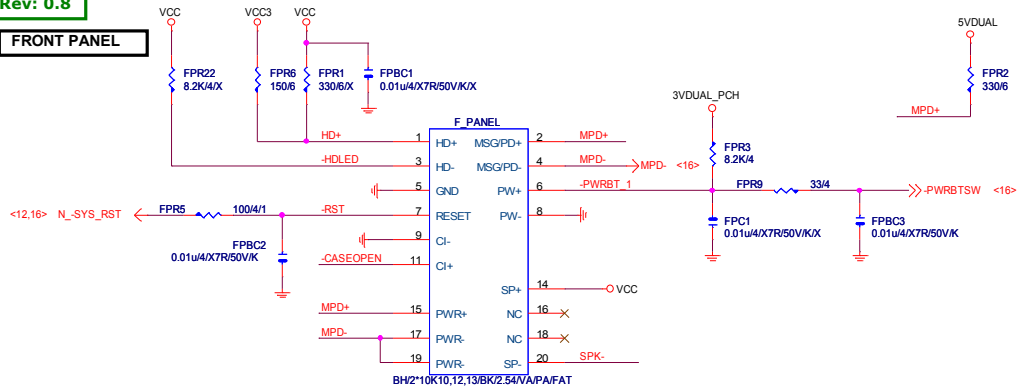
Size	Document Number	Rev
A	B460 HD3	1.01

Date: Wednesday, March 18, 2020 Sheet 49 of 58

Rev: 0.8

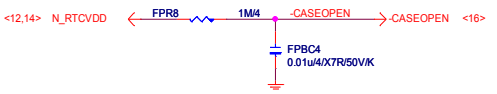
FRONT PANEL

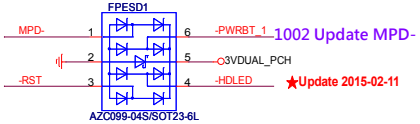
★Update 2016.06.15



Update 2015.01.08
Footprint=F_PANEL-100

CASE OPEN



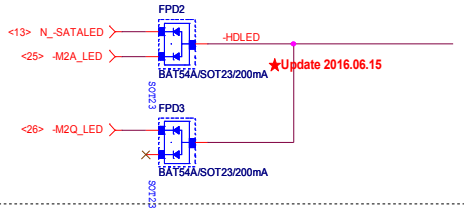


1002 Update MPD-

★Update 2015-02-11

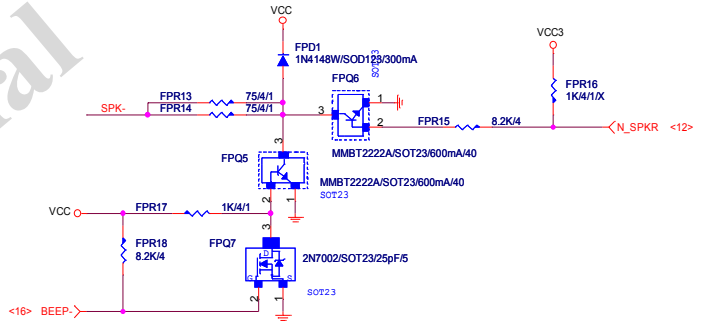
SATA/M.2 LED

Fix some M.2 cause HD_LED always on.



★Update 2016.06.15

SPKR

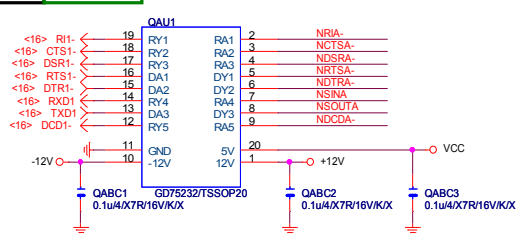


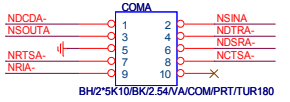
For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

GIGABYTE Technology		
Title: FRONT PANEL		
Size: Custom	Document Number: B460 HD3	Rev: 1.01
Date: Wednesday, March 18, 2020	Sheet 50 of 58	

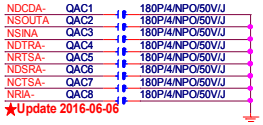
COM PORT

Rev: 0.7



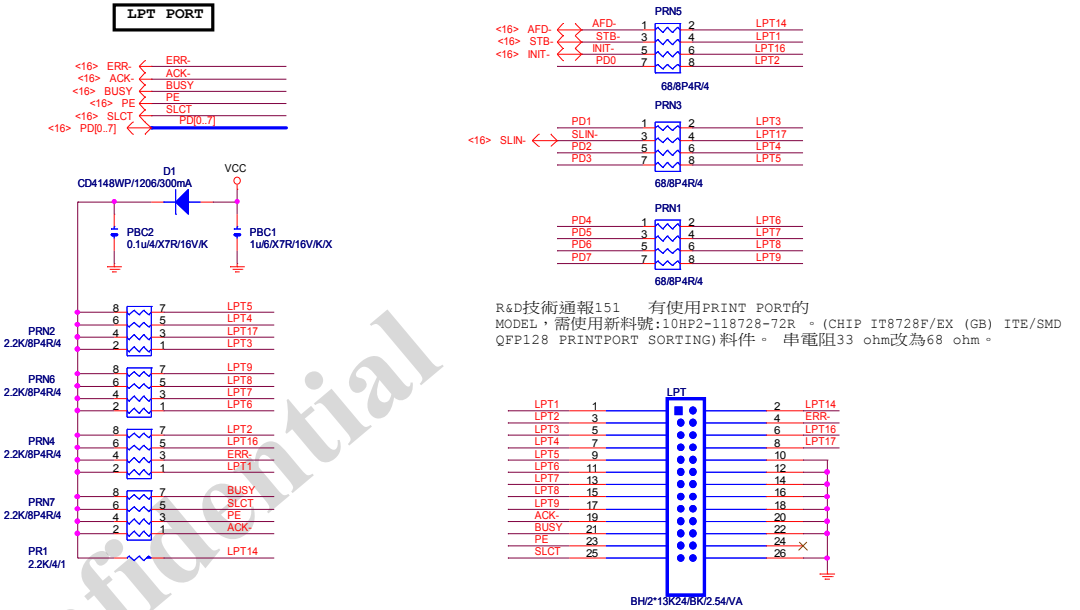


F_COM-HS



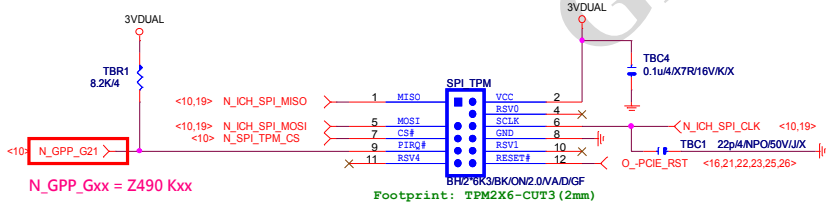
★Update 2016-06-06

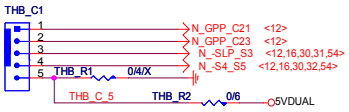
LPT PORT



R&D技術通報151　有使用PRINT PORT的MODEL，需使用新料號:10HP2-118728-72R 。(CHIP IT8728F/EX (GB) ITE/SMD QFP128 PRINTPORT SORTING)料件。 串電阻33 ohm改為68 ohm。

TPM CONNECT

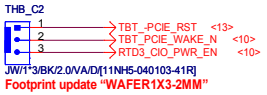




Footprint update "WAFER-1X5P"

Thunderbolt

★Update 2015-12-29



Footprint update "WAFER1X3-2MM"

FOR TBT RTD3

Z490系列使用

TBT_PCIE_RST : CFL connector to GPP_F_2
TBT_PCIE_WAKE_N : CFL connector to GPP_H_15
RTD3_CIO_PWR_EN : CFL connector to GPP_K_23

GIGABYTE Technology		
Title: FP,F_USB,USB PWR,BZ		
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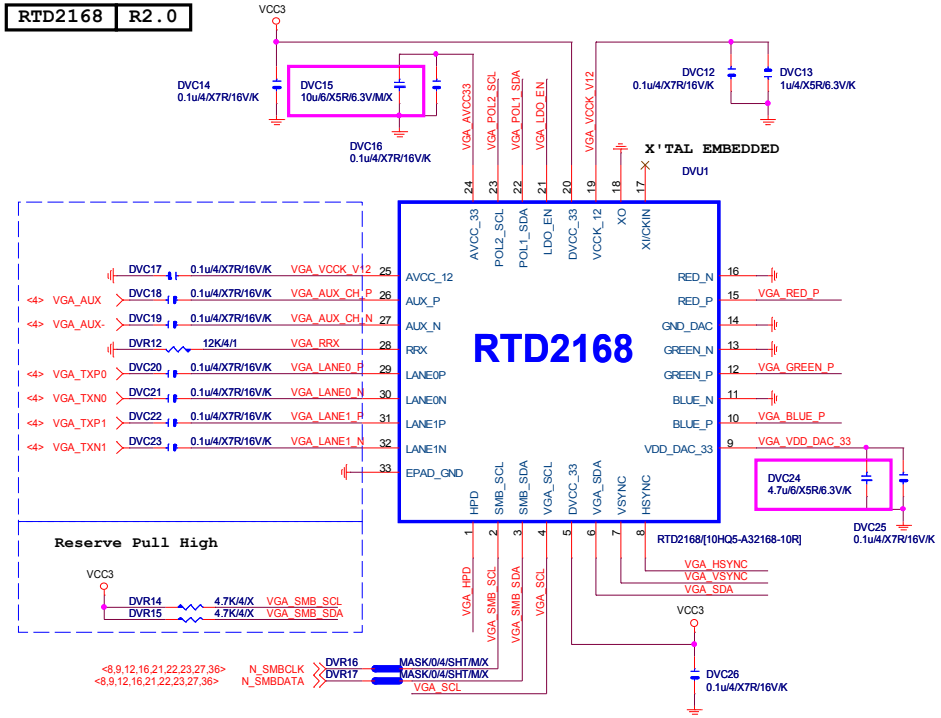
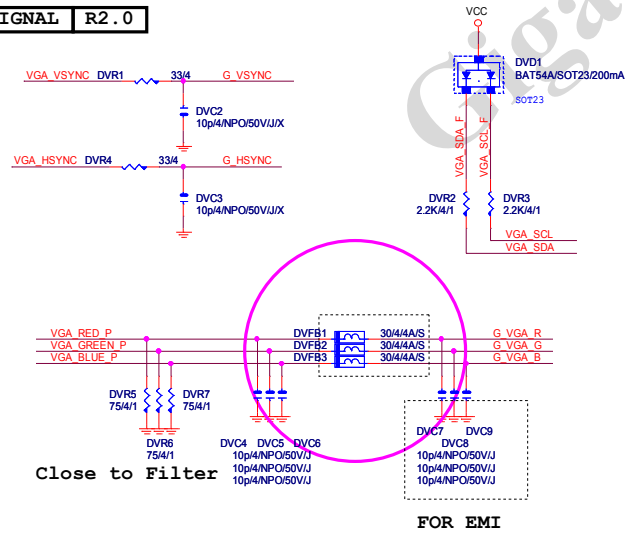
RTD2168 R2.0

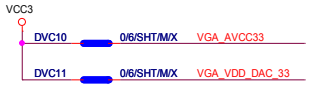


放置PCH端

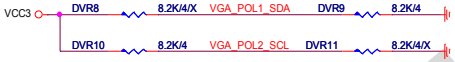
VGA SIGNAL R2.0



POWER



Power on latch



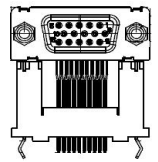
POL2_SCL (PIN23)	POL1_SDA(PIN22) = 0	POL1_SDA(PIN22) = 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

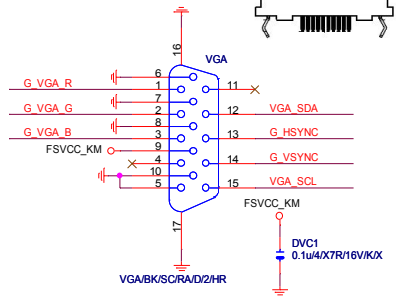
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

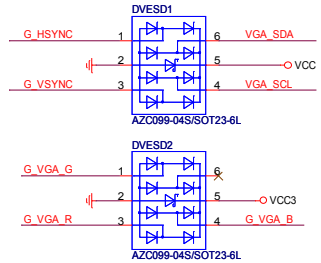
DP HPD

VGA CONN. 架高型VGA(BLACK)





VGA ESD



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EMI/ESD R0.1

CLOSE SIO

EMIC1
100p/4/NPO/50V/J/X

<12,16,30,31,51> N_-SLP_S3

EMIC2
100p/4/NPO/50V/J/X

<12,16,30,32,51> N_-S4_S5

CLOSE PCH

EMIC4
100p/4/NPO/50V/J/X

<4,12> N_CPUPWROK

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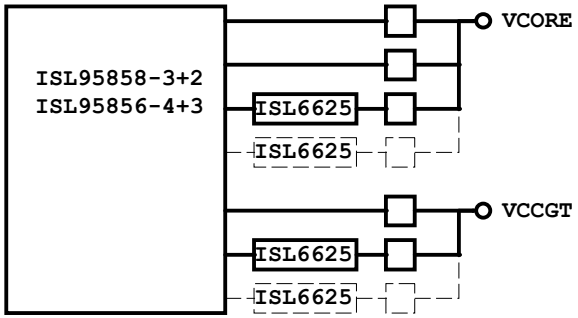
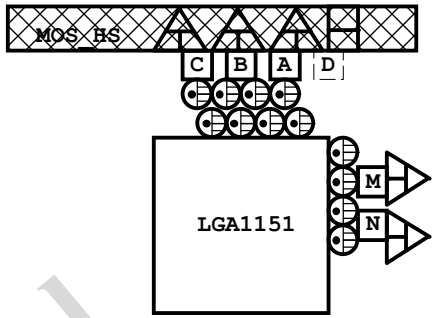
POWER BLOCK MAP

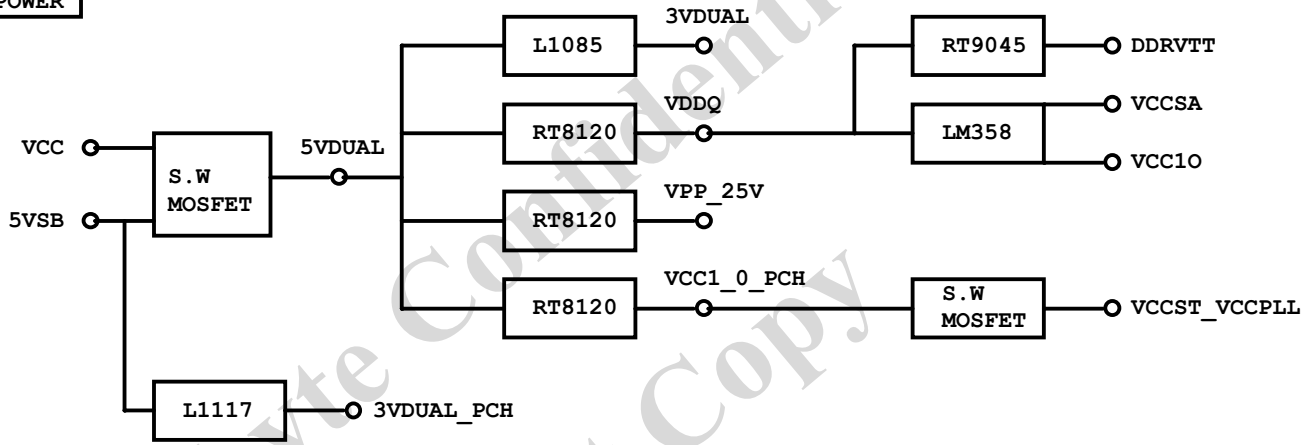
- CPU
  - VCORE
  - VCCGT
  - VCCSA
  - VCCIO
  - VDDQ
  - VCCST_VCCPLL
  - VCCSFUSEPRG
- DDR4
  - VDDQ
  - DDRVTT
  - VPP_25V
  - VDDSPD(VCC3)
- PCH
  - VCC1_0_PCH
  - VCC1_0_PCH_DSW
  - VCC10_VCCF24_1P0
  - VCC10_VCCAMPHYPLL
  - VCC10_VCCAPLL
  - VCC3_PCH
  - 3VDUAL_PCH
  - VCC3
  - N_RTCVDD
- IT8628
  - IT_VCCH
  - IT_AVCC
  - 2_5LEVEL
- HM
  - +12V
  - VCC
  - VCC3
  - VCORE
  - VCCGT(IMON_VCCGT)
  - VDDQ
  - VCCSA(IMON_VCORE)

VCORE/VCCGT

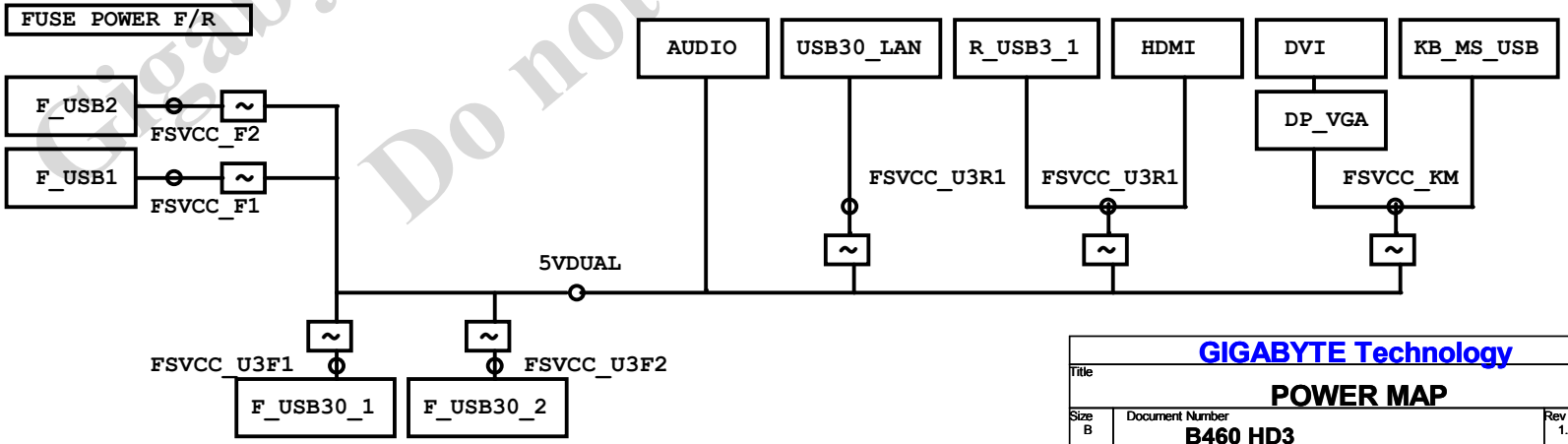




POWER



FUSE POWER F/R



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Title: POWER MAP

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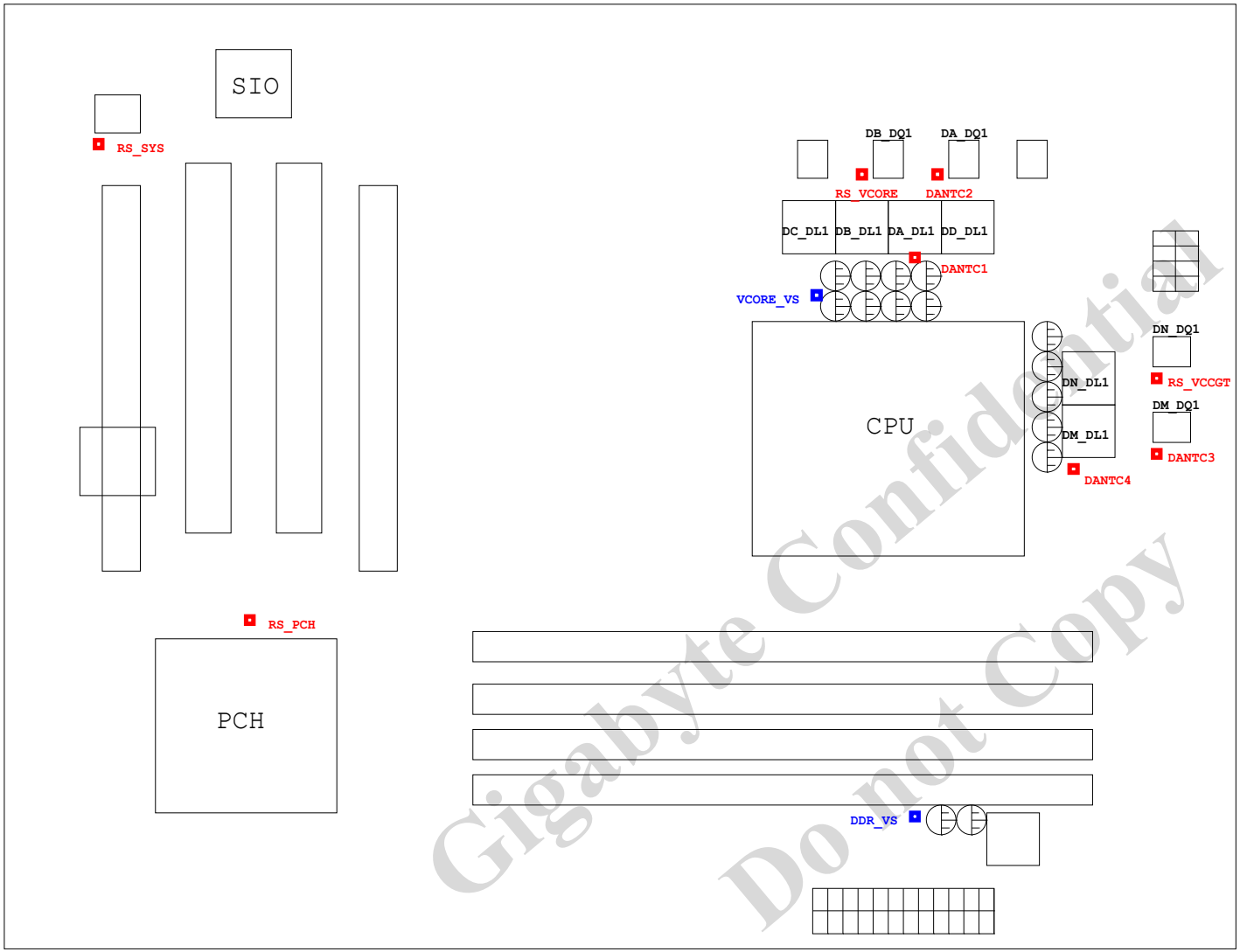

熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL1	N/A
DANTC2	DA_DQ1	Differential
DANTC3	DM_DQ1	N/A
DANTC4	DM_DL1	Differential
RS_VCORE	DB_DQ1	N/A
RS_VCCGT	DN_DQ1	N/A
RS_PCH	PCH	N/A
RS_SYS	CU1	N/A

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Title
D_LED1/D_LED2

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