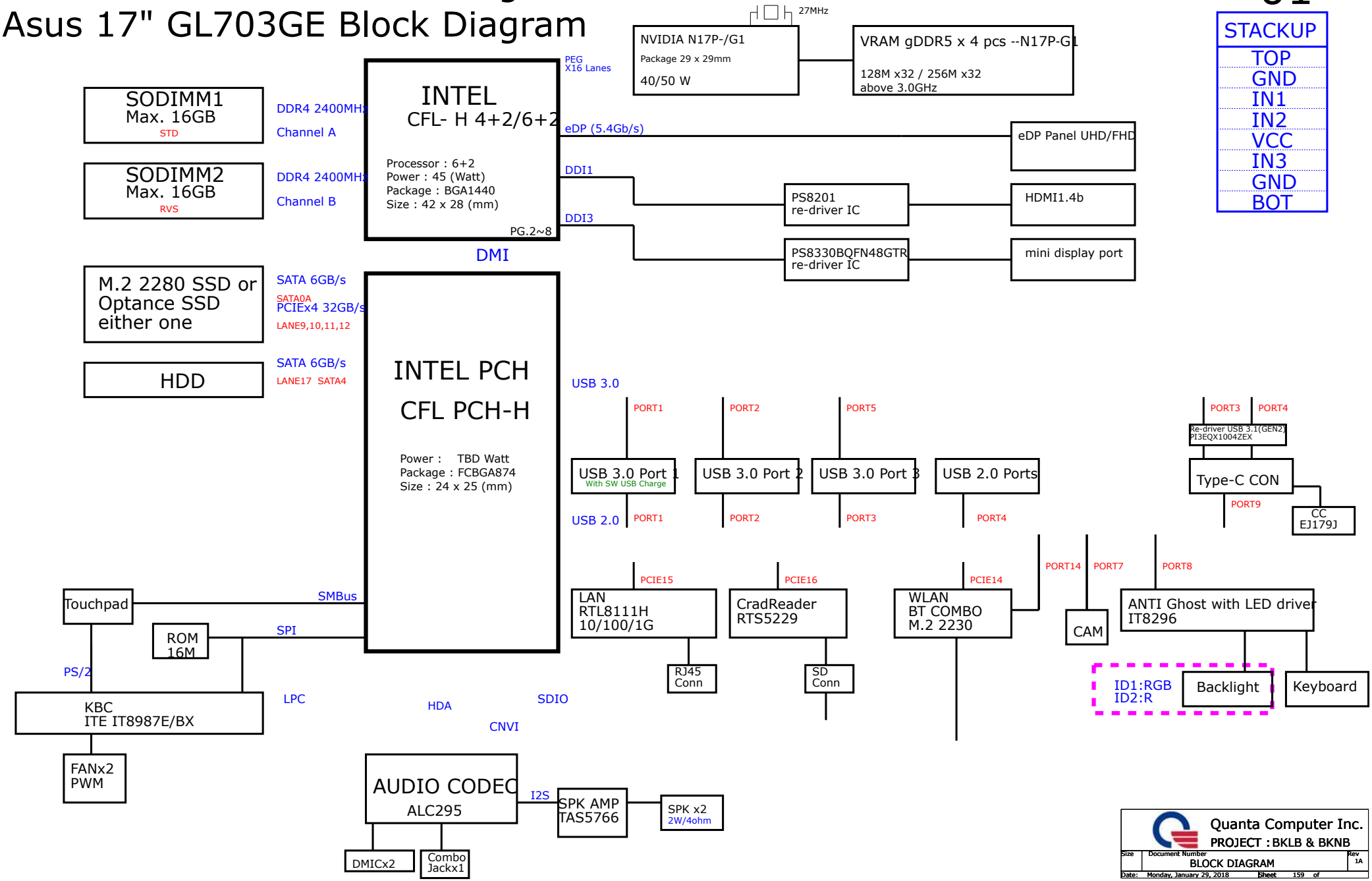
Asus 15" GL503GE Block Diagram
Asus 17" GL703GE Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, January 29, 2018 Sheet 159 of

Model
BKLB
BKNB

REV	CHANGE LIST
PR	Page 11 -- Change R1027 pull high from +3V to +3V_S5 for SYS_RESET,Follow CRB request Page 11 -- ADD RTC battery detect for ASSY line request. Page 13 -- ADD R1220 pull high to +3V_S5 for PCH_SPI1_SI and no mount. Page 14 -- ADD GL703GD for 1050 MBID. Page 16 -- DEL R1181,R1179,R1182,R1180,R1183,R1184 Series for PCH SD signal for EMI verify Page 17 -- Modify H12 layout for Thermal issue and add 0ohm for EMI request Page 23 -- Change VR67 from 100K to 150K for solve power off timing for GPU Page 23 -- Add VR174,VQ15,VC486 for solve power off timing for GPU. Re-work ok and verify on latest report Page 23 -- Add VR173,VQ14,VC485 for solve power off timing for GPU. Re-work ok and verify on latest report Page 32 -- Change C320 ,C338,C339 size from 0201 to 0402 for SMT line request. Page 34 -- Change R231 10K from mount to no mount. There is pull high on PCH side. Page 34 -- Change TR3 from 10K to 18.7K. To define GPU thermal OT on 120 degree. Page 35 -- Add AR126 and AR127 Bead for solve ESD and Change AC45 AC42 from 100p to 680P And Change TVS on SLEEVE and RING2 Page 36 -- Add RTC_DET# at GPA0 for Assy line request. Page 36 -- Change KR72 form 100K to 200K for PR stage. Page 50 -- Change KC85 size form 0201 to 0402 for SMT line request. Page 51 -- Add MR28 10K to pull down on PCIE_CLKREQ_CR#, Realtek request to alwayes pull down.
MP	

DOC NO.	PROJECT MODEL :	BKLB/BKNB	APPROVED BY:		DATE:	2018/01/29
	PART NUMBER:		DRAWING BY:		REVISON:	3A

Quanta Computer Inc.
PROJECT : BKLB & BKNB
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KABY LAKE Processor (CLK,MISC,JTAG)

03

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

Please remove to CPU side

PROCHOT# (50ohm)
Trace Length <11 inches

Close to U1

Mount 220P for ESD

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

Close to CPU

SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID DATA

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

For DCI debug

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;

Mark eDP mode Enabled

Mark PCIE port reserved
N17P used port 8~15

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

CPU VDDQ

Placement close to CPU.

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

Close to U1

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Size	Document Number	Rev
	CFL 1/7 (JTAG/MISC)	1A
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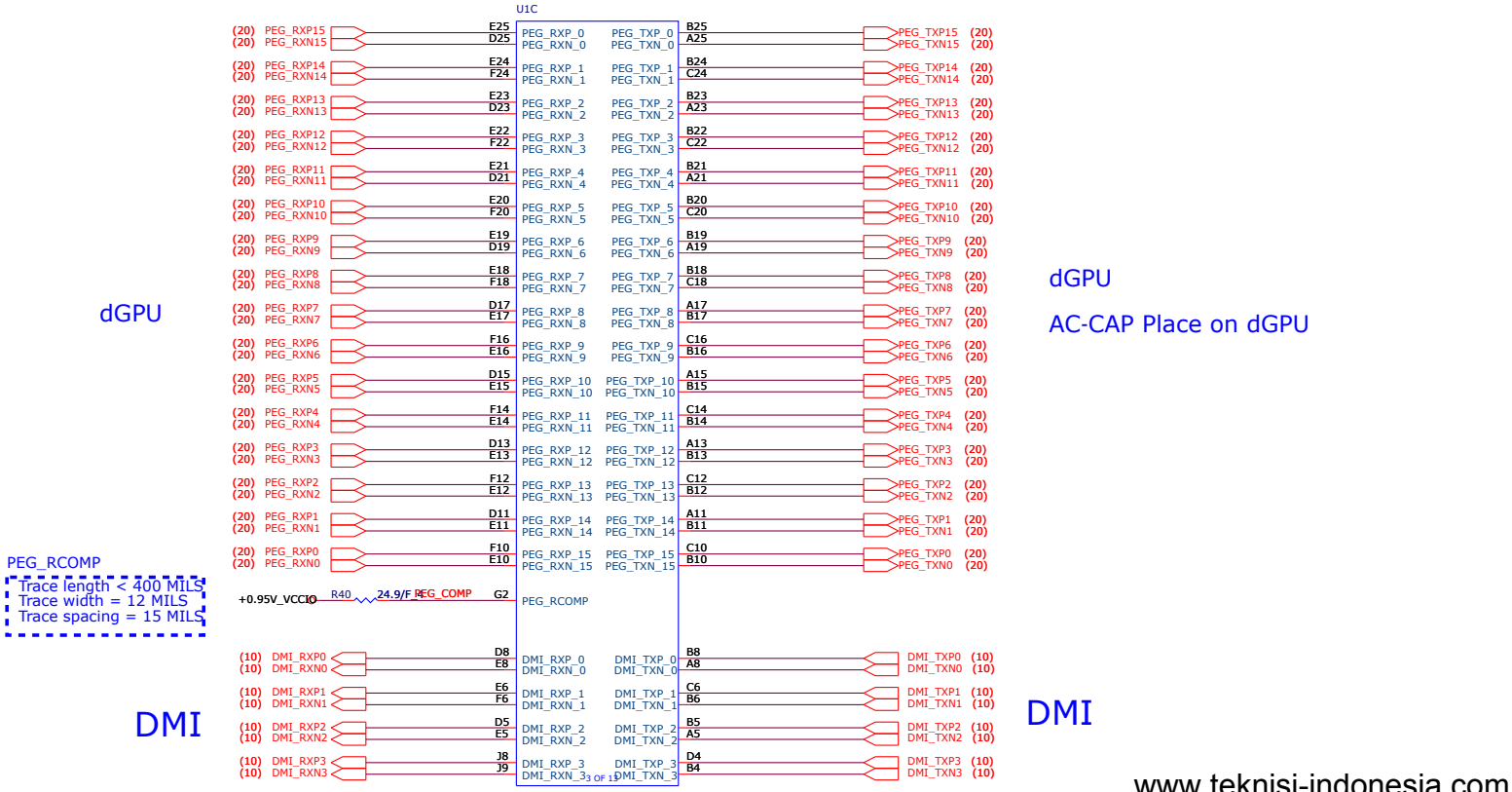
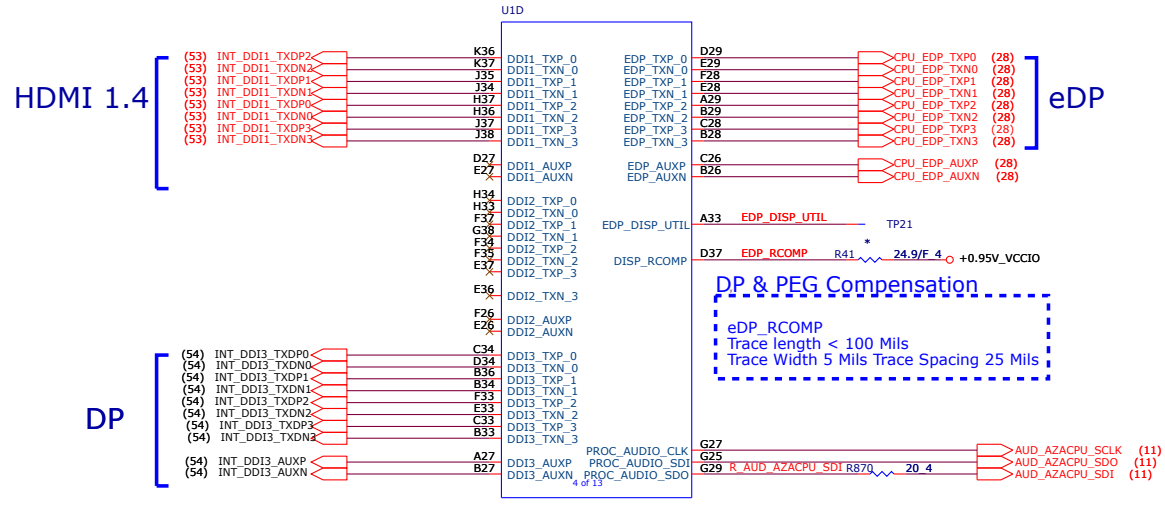
KABY LAKE Processor (DMI,PEG,FDI)





Quanta Computer Inc.		
PROJECT : BKLB & BKNB		
Size	Document Number: CFL 2/7 (DMI/EDP/PEG)	Rev: 1A
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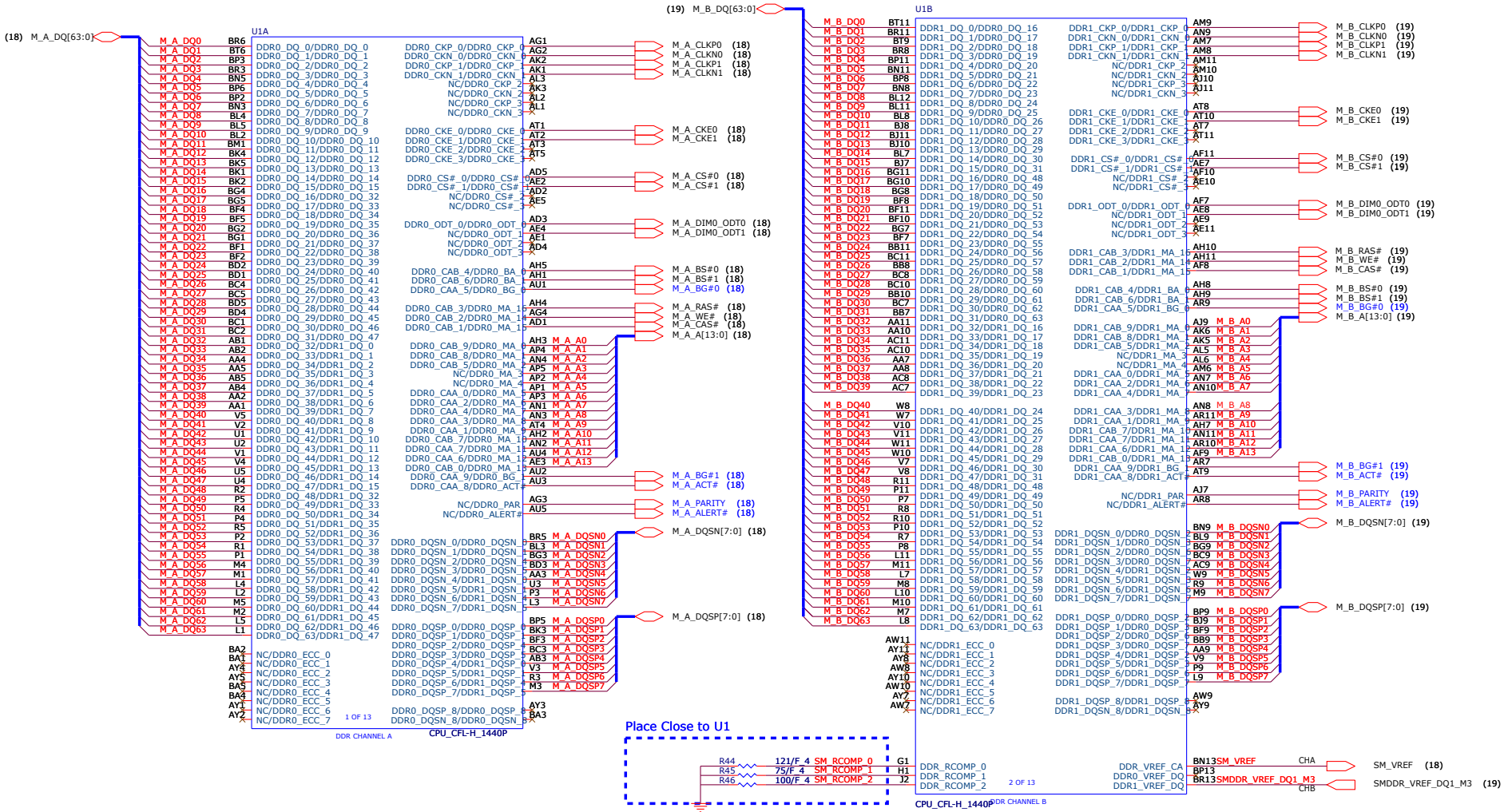
KABY LAKE Processor (DDR4)



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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 3/7 (DDR4 I/F)	1A

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CFL Processor (POWER)

Follow CFL H page 133 to 45W(GT2): +VCCGT=32A

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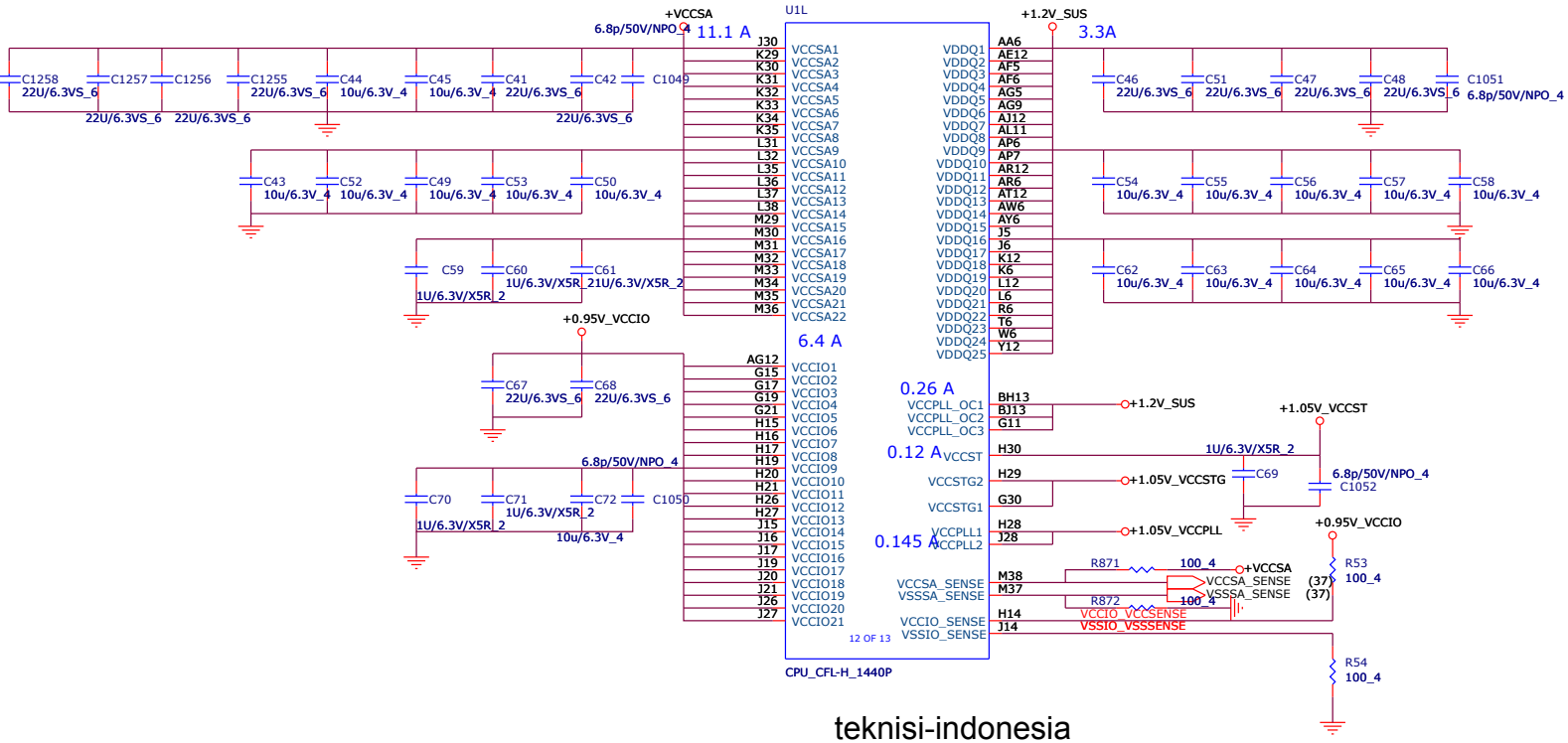
PROJECT : BKLB & BKNB	
Size	Document Number: CFL 4/7 (POWER) — Rev: 2A
Date: Monday, January 29, 2018	Sheet 659 of



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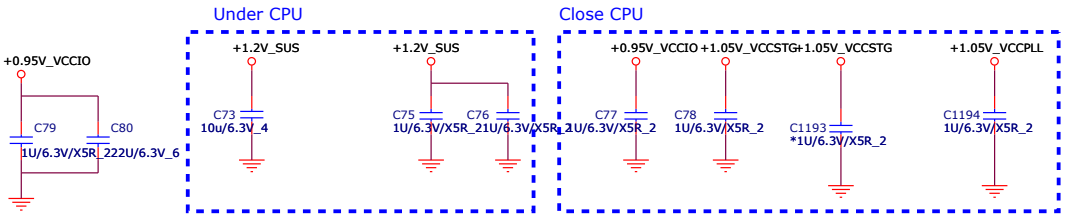

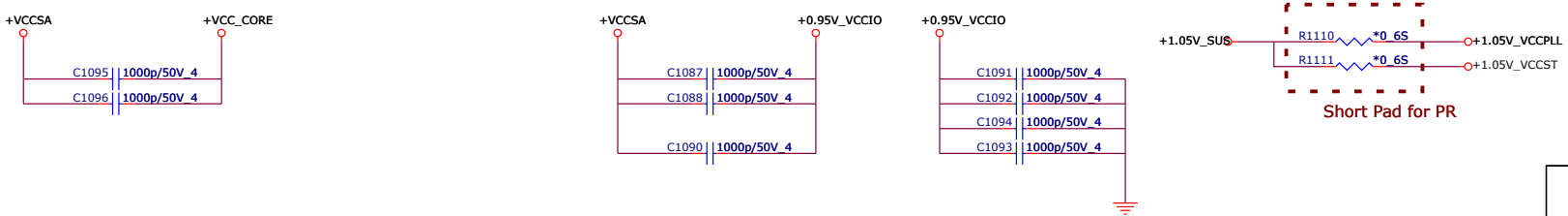

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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 5/7 (POWER&GND)	2A

Date: Monday, January 29, 2018 Sheet 759 of

Follow CFL H EDS page 130 to 45W(GT2): VCC_CORE=128A for 6 code
Follow CFL H EDS page 130 to 45W(GT2): VCC_CORE=86A for 4 code

08

+VCC_CORE

U1I

CPU_CFL-H_1440P

9 OF 13

VCC_SENSE
VSS_SENSE

R65 100_4

R66 100_4

Add 22u and 1u for 6 core CPU

U1J

CPU_CFL-H_1440P

10 OF 13

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impendence 50 ohm

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 6/7 (POWER&GND)	1A
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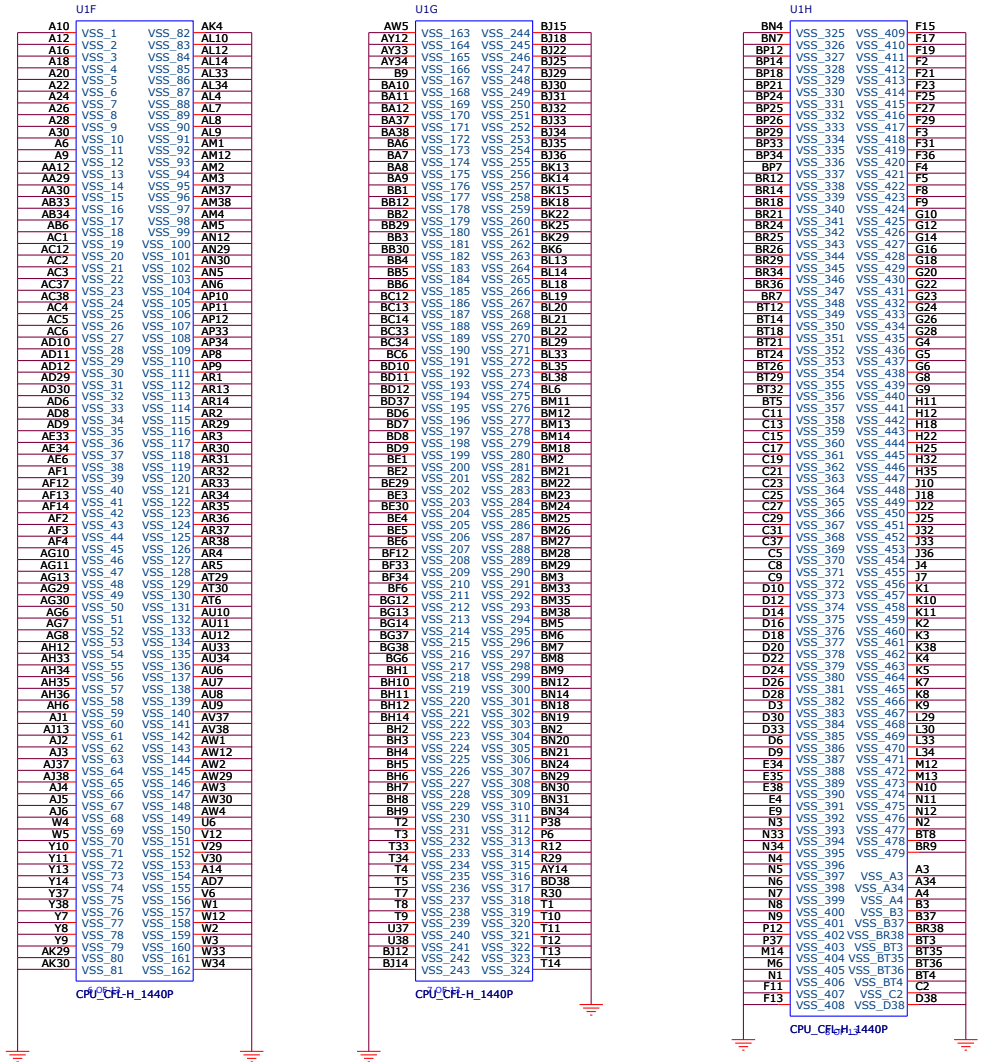
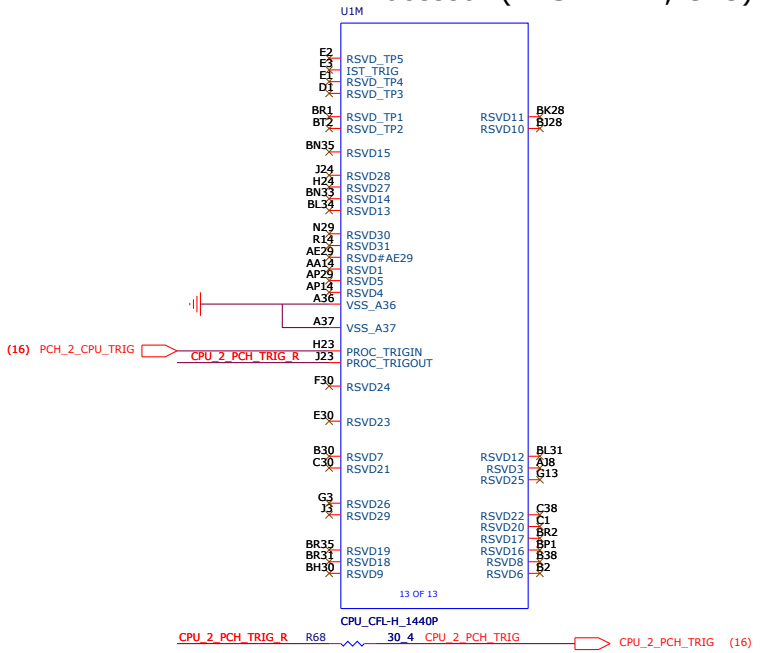
KBL-HProcessor (GND)



09

KBL-H Processor (RESERVED, CFG)

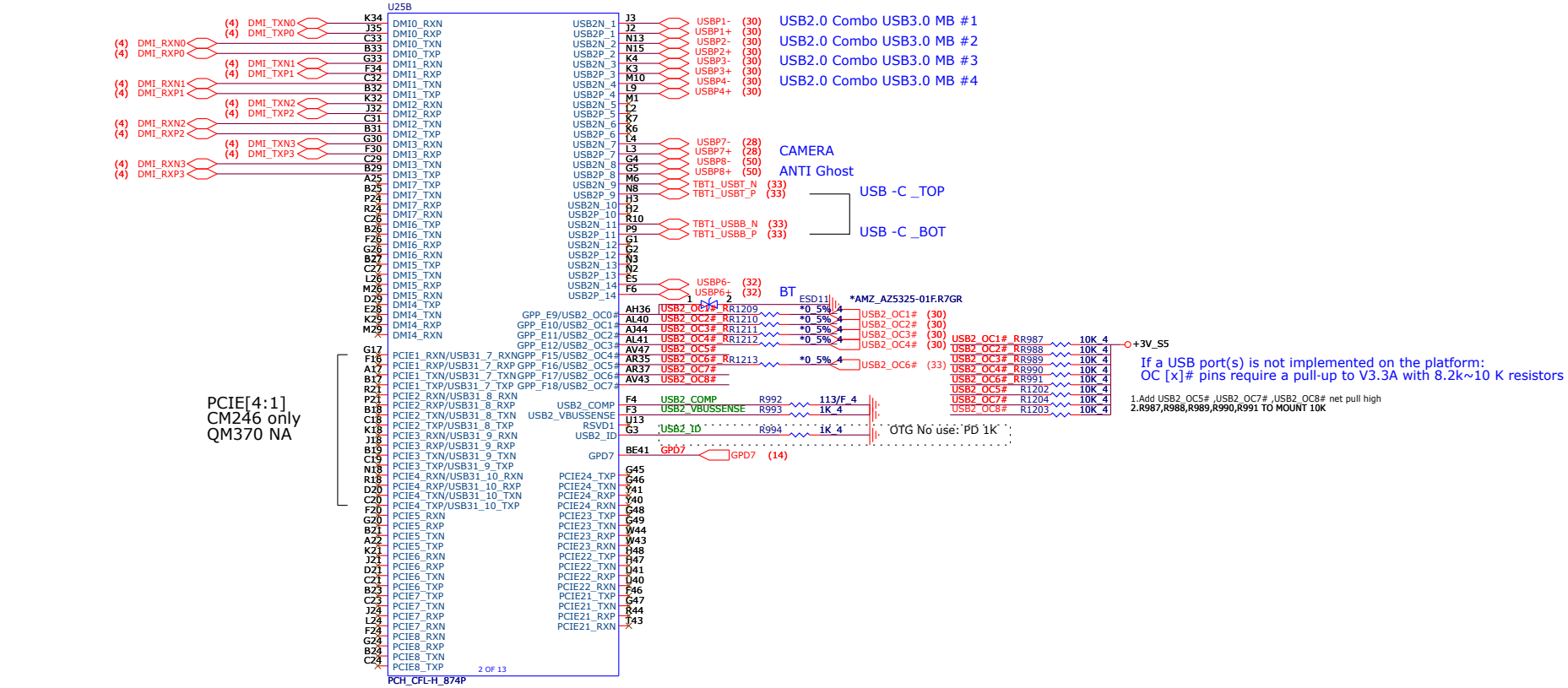


Quanta Computer Inc.

PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 7/7 (GND)	1A

Date: Monday, January 29, 2018 Sheet 959 of



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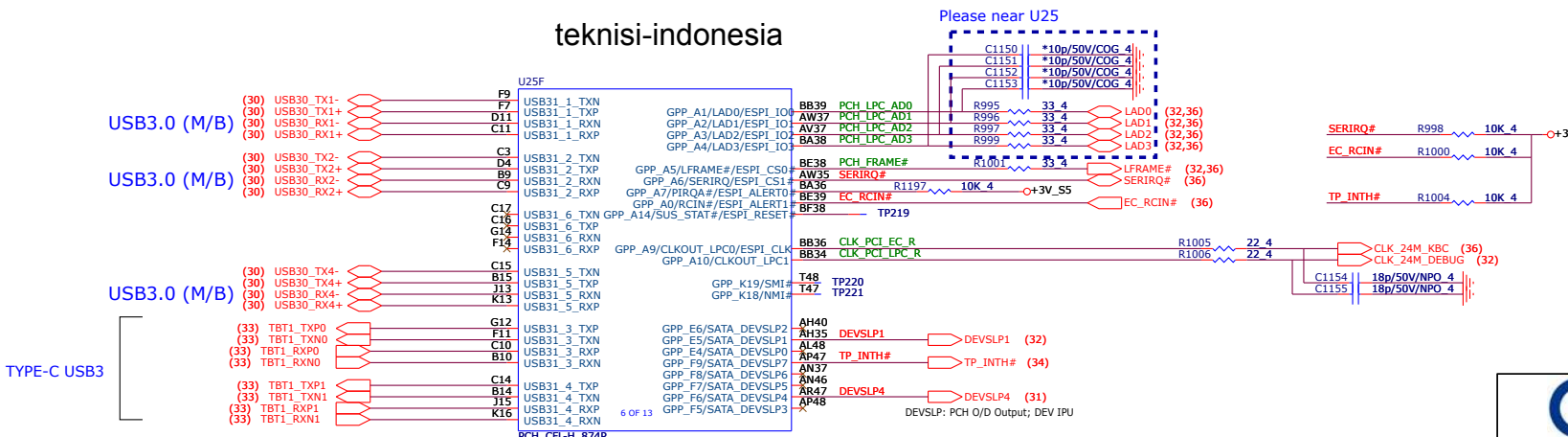

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	2A
Date: Monday, January 29, 2018	Sheet 10 of 59	

Please near U25

EC152 *33p/50V/NPO_4
EC153 *33p/50V/NPO_4
EC154 33p/50V/NPO_4

(36) GPIO33_EC — R1011 1K_4 — ACZ_SDOUT

(35) BIT_CLK_AUDIO — R1008 22_4 — ACZ_BCLK
(35) ACZ_SDIN0
(35) ACZ_SDOUT_AUDIO — R1009 22_4 — ACZ_SDOUT
(35) ACZ_SYNC_AUDIO — R1012 22_4 — HDA_SYNC_R

EC Drive High for OVERRIDE

TP182 *

R1010 *22_4 ACZ_RST#

Please near U25

(4) AUD_AZACPU_SDO — R1015 30_4 — HDACPU_SDO_R
(4) AUD_AZACPU_SDI
(4) AUD_AZACPU_SCLK — R1017 30_4 — HDACPU_SCLK_R

EC155 *33p/50V/NPO_4
EC156 *33p/50V/NPO_4

(32) CNV_WR_CLKREQ0
(32) CNV_RF_RST#

+3V_S5
R1018 2.2K_4 SML0CLK
R1019 2.2K_4 SML0DATA
R1206 1K_4 SML1CLK
R1207 1K_4 SML1DATA
R1022 10K_4 PCH_BATLOW#

+3V
R1024 2.2K_4 SMB_RUN_CLK
R1025 2.2K_4 SMB_RUN_DAT
+3V_S5
R1027 10K_4 SYS_RESET#

DDR4 SPD

U25D

HDA_BCLK/I2S0_SCLK	BD11	GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#	BF36
HDA_SDI0/I2S0_RXD	BE11	GPP_A8/CLKRUN#	AV32
HDA_SDO/I2S0_TXD	BF12		
HDA_SYNC/I2S0_SFRM	BG13	GPD11/LANPHYPC	BF41
HDA_RST#/I2S1_SCLK	BE10	GPD9/SLP_WLAN#	BD42
HDA_SDI1/I2S1_RXD	BF10		
I2S1_TXD/SNDW2_DATA	BE12	DRAM_RESET#	BB46
I2S1_SFRM/SNDW2_CLK	BD12	GPP_B2/VRALERT#	BE32
		GPP_B1/GSPI1_CS1#/TIME_SYNC1	BF33
		GPP_B0/GSPI0_CS1#	BE29
		GPP_K17/ADR_COMPLETE	R47
HDACPU_SDO	AM2	GPP_B11/I2S_MCLK	AP29
HDACPU_SDI	AN3	SYS_PWROK	AU3
HDACPU_SCLK	AM3		
		WAKE#	BB47
GPP_D8/I2S2_SCLK	AV18	GPD6/SLP_A#	BE40
GPP_D7/I2S2_RXD	AW18	SLP_LAN#	BF40
GPP_D6/I2S2_TXD/MODEM_CLKREQ	BA17	GPP_B12/SLP_S0#	BC28
GPP_D5/I2S2_SFRM/CNV_RF_RESET#	BE16	GPD4/SLP_S3#	BF42
GPP_D20/DMIC_DATA0/SNDW4_DATA	BF15	GPD5/SLP_S4#	BE42
GPP_D19/DMIC_CLK0/SNDW4_CLK	BD16	GPD10/SLP_S5#	BC42
GPP_D18/DMIC_DATA1/SNDW3_DATA	AV16		
GPP_D17/DMIC_CLK1/SNDW3_CLK	AW15	GPD8/SUSCLK	BE45
		GPD0/BATLOW#	BF44
		GPP_A15/SUSACK#	BE35
RTCRST#	BE47	GPP_A13/SUSWARN#/SUSPWRDNACK	BC37
SRTCRST#	BD46		
PCH_PWROK	AY42	GPD2/LAN_WAKE#	BG44
RSMRST#	BA47	GPD1/ACPRESENT	BG42
		SLP_SUS#	BD39
		GPD3/PWRBTN#	BE46
DSW_PWROK	AW41	SYS_RESET#	AU2
GPP_C2/SMBALERT#	BE25	GPP_B14/SPKR	AW29
GPP_C0/SMBCLK	BE26	CPUPWRGD	AE3
GPP_C1/SMBDATA	BF26		
GPP_C5/SML0ALERT#	BF24	ITP_PMODE	AL3
GPP_C3/SML0CLK	BF25	PCH_JTAGX	AH4
GPP_C4/SML0DATA	BE24	PCH_JTAG_TMS	AJ4
GPP_B23/SML1ALERT#/PCHHOT#	BD33	PCH_JTAG_TDO	AH3
GPP_C6/SML1CLK	BF27	PCH_JTAG_TDI	AH2
GPP_C7/SML1DATA	BE27	PCH_JTAG_TCK	AJ3

4 OF 13

PCH_CFL-H_874P

(36) PCH_PWROK
(36) RSMRST#
(14) SMBALERT#
(18,19) SMB_RUN_CLK
(18,19) SMB_RUN_DAT
(14) SML0ALERT#
(14) SML1ALERT#

ESD12 — *AMZ_AZ5325-01F.R7GR

DDR4_DRAMRST# (18,19)

PCIE_WAKE# — R1014 1K_4 — +3V_S5
PCH_SUSPWRDNACK# — R1016 10K_4 — +3V_S5

SYSPWROK (36)
PCIE_WAKE# (32,55)
SUSB# (36)
SUSC# (36)
TP185
SUSCLK (32)

PCH_SUSPWRDNACK#, O/D
Output High: No require PCH Primary well
SUSACK#: Need for DeepSx only

R1023 *10_4

R1198 10K_4 — +3V_S5
AC_PRESENT_EC (36)
DNBSWON# (36)
SYS_RESET#
ACZ_SPKR (14)
PROCPWRGD (3)
R1026 1K_4 — +1.05V_S5
XDP_TCK#_CPU (3)
XDP_TMS_CPU (3)
XDP_TDO_CPU (3)
XDP_TDI_CPU (3)
TP193

SUSB# — TP187
SUSC# — TP188

ACPRESENT PCH IPD 20K
AC_PRESENT_EC — TP190
DNBSWON# — TP191
PROCPWRGD — TP192

1003 Default GPI PIN, no need termination
DEL MBCLK1 and MBDATA1 to U25

1213 PR Change

RTC Circuitry(RTC)

RTC Power trace width 20mils.

+3VPCU — R1175 1K/F_4 — 20MIL — D4 (BAT54CW) — 30mils — +3V_RTC
20MIL — R1176 45.3K/F_4
20MIL — +3V_RTC_0 — R1033 1K/F_4
20MIL — R1219 0_4 — Q50 PJA138K — RTC_3V
CN19 — AAA-BAT-054-K01_RTC Battery
R1216 10M_4
R1218 1K_4
R1217 100K_4 — RTC_DET# (36)
+3V_RTC — R1029 30.1K/F_4 — RTC_RST#
+3VPCU — R1032 30.1K/F_4 — SRTC_RST#
C1156 1U/6.3V/X5R_2
C1158 1U/6.3V/X5R_2
J1 *SOLDERJUMPER-2

1/4 PR Change

RTC Detect for EC Check

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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	1A

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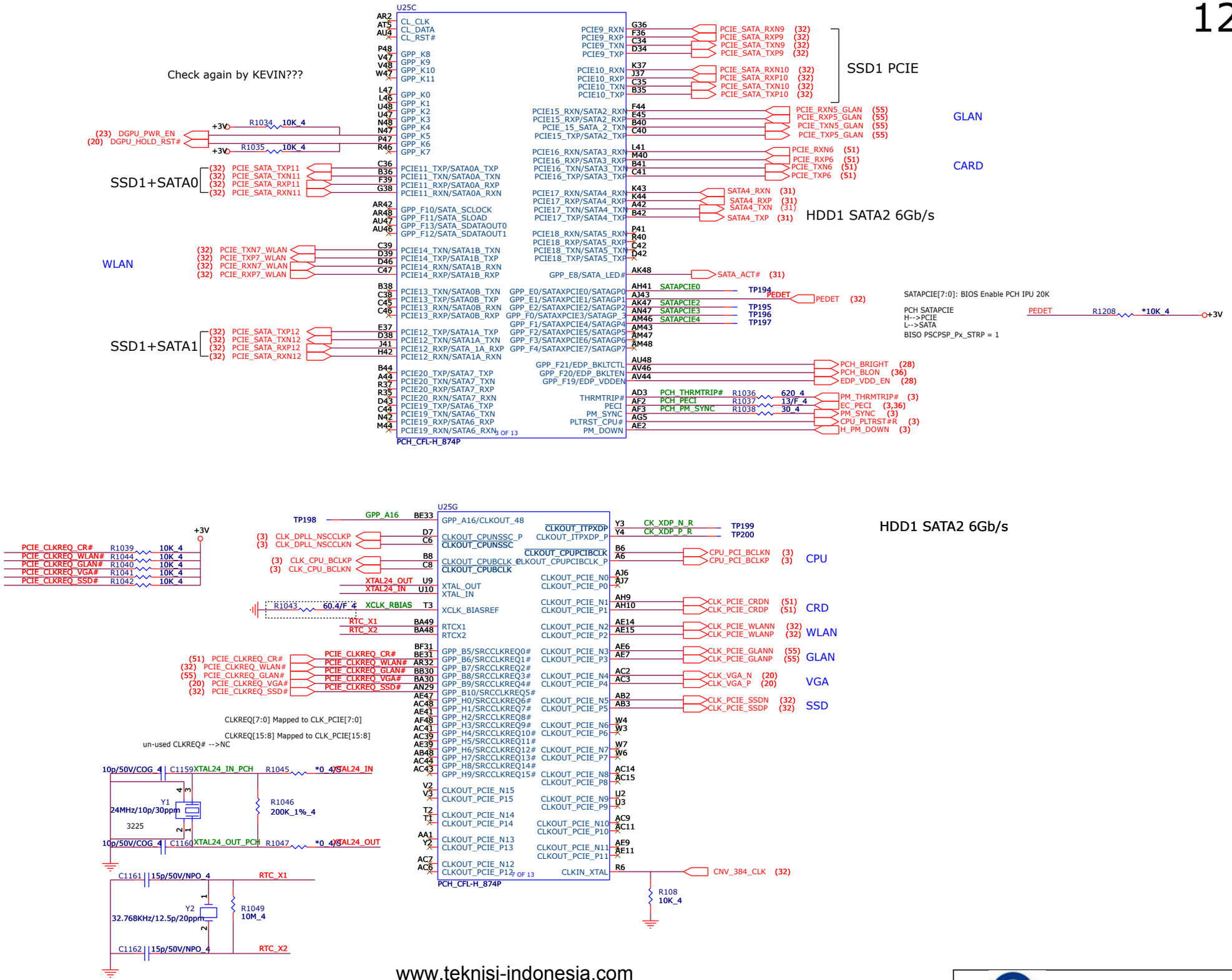
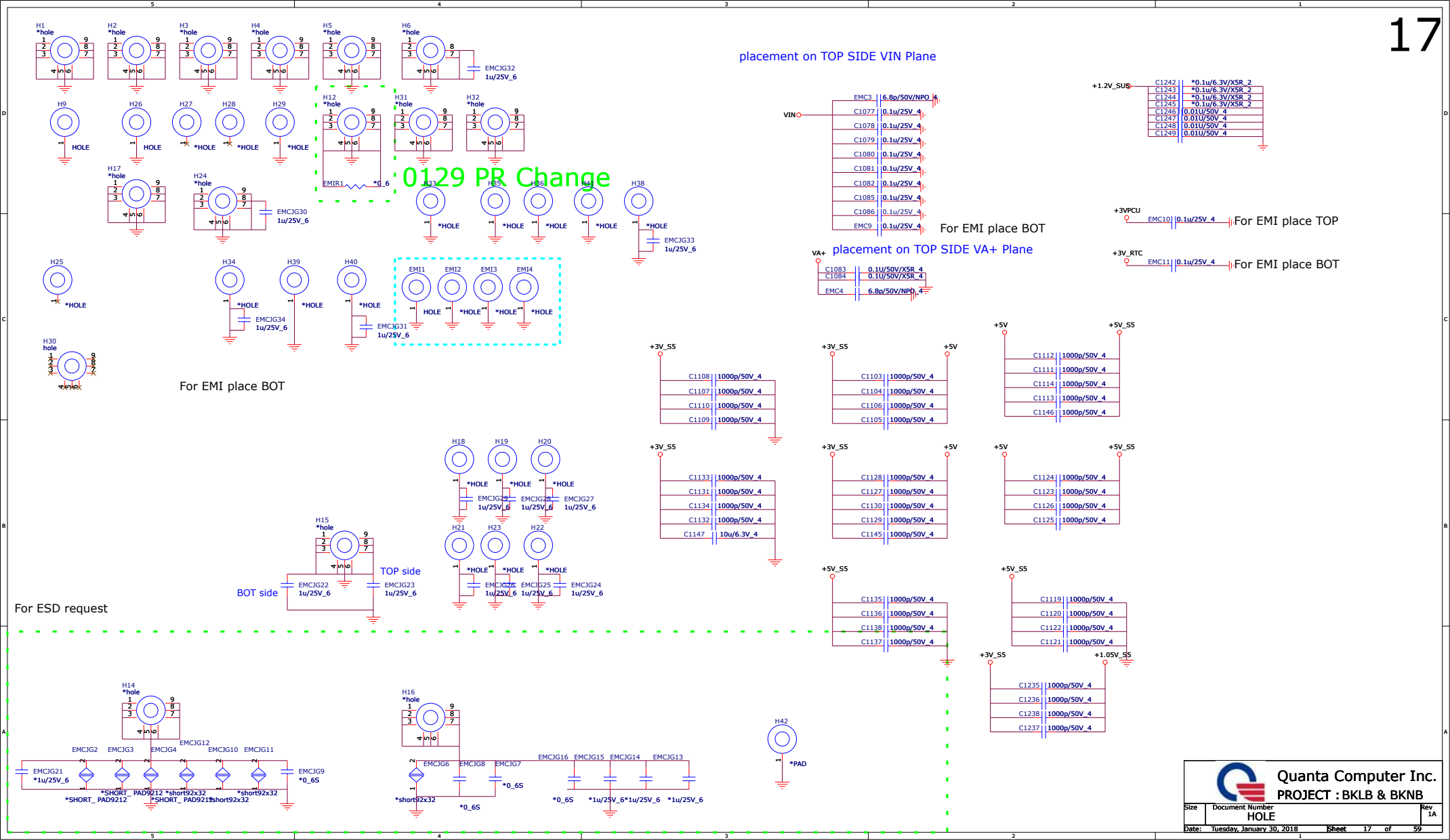


Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 3/7 (SATA/LPC/CLK)	1A
Date: Monday, January 29, 2018	Sheet 12 of 59	


placement on TOP SIDE VIN Plane
0129 PR Change
For EMI place BOT
placement on TOP SIDE VA+ Plane
For EMI place BOT
For EMI place TOP
For EMI place BOT
TOP side
BOT side
For ESD request
Quanta Computer Inc.
PROJECT : BKLB & BKNB
Size
Document Number
HOLE
Rev
1A
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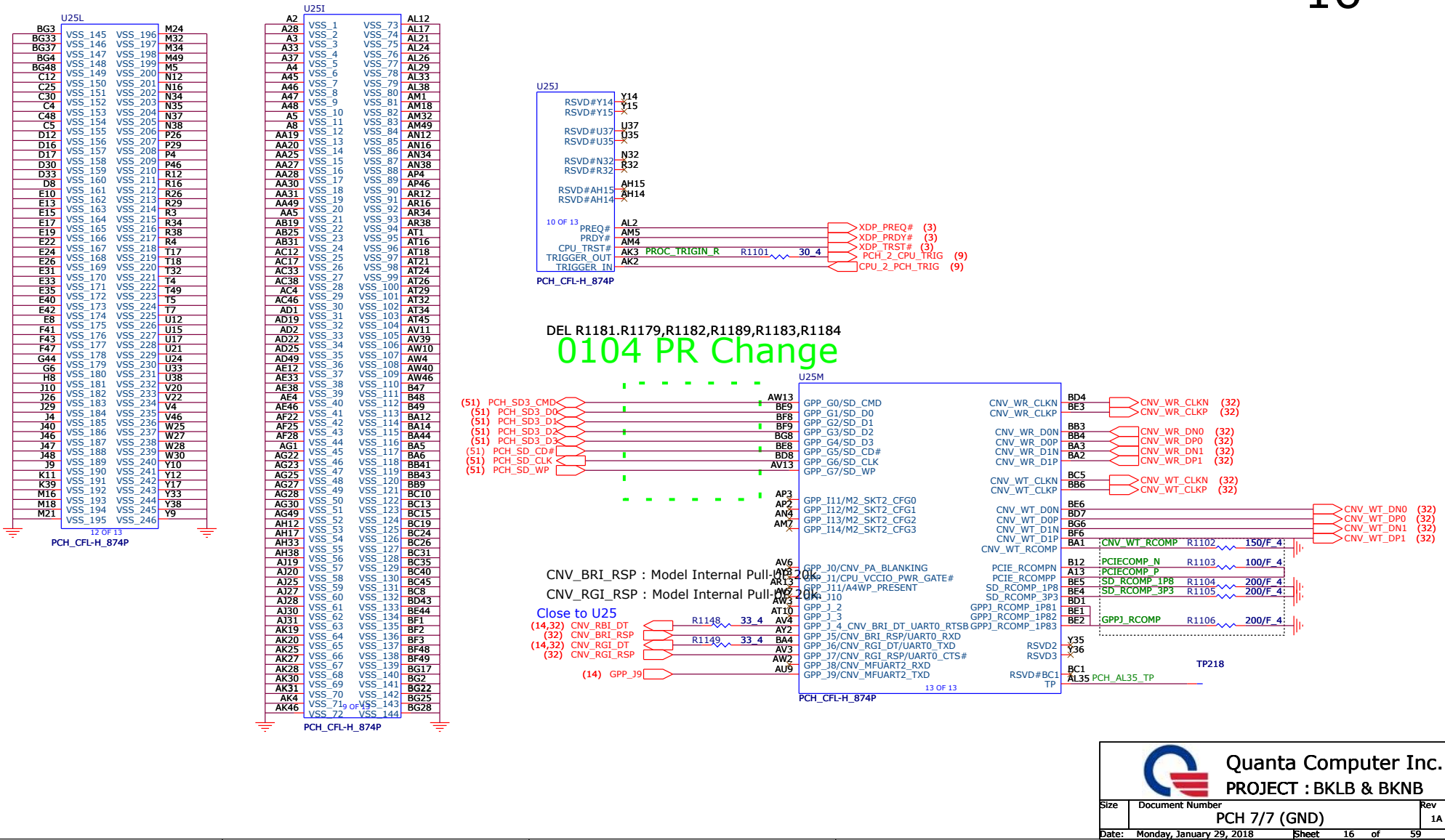

Quanta Computer Inc.		
PROJECT : BKLB & BKNB		
Size	Document Number	Rev
	PCH 7/7 (GND)	1A
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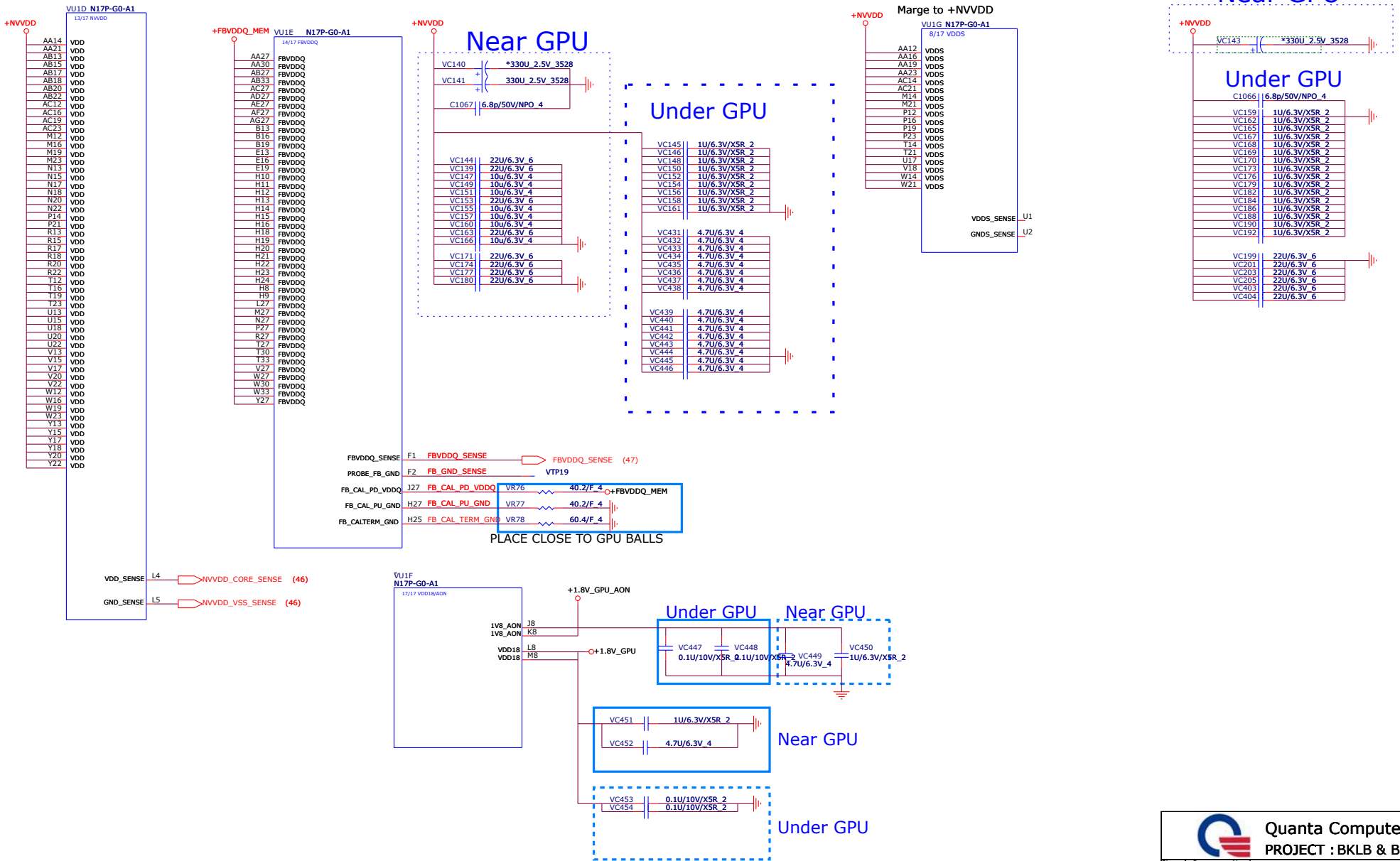

Quanta Computer Inc.		
PROJECT : BKLB & BKNB		
Size	Document Number	Rev
	N17P-G1-POWER 5/7	1A
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Under GPU

Near GPU

NVVDD POWER GOOD LOOPBACK

DEL NVVDDSPG

0110 PR Change

Change VR67 from 100K to 150K

Overt temp ckt for NVVDD

for GC6

GPU All power good

For Power off sequence

0.4A

90 ohms +/- 15% Differential Impedance

0110 PR Change

Add power off timing

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PROJECT : BKLB & BKNB

Size | Document Number: N17P-G1-MISC 4/9 | Rev: 1A

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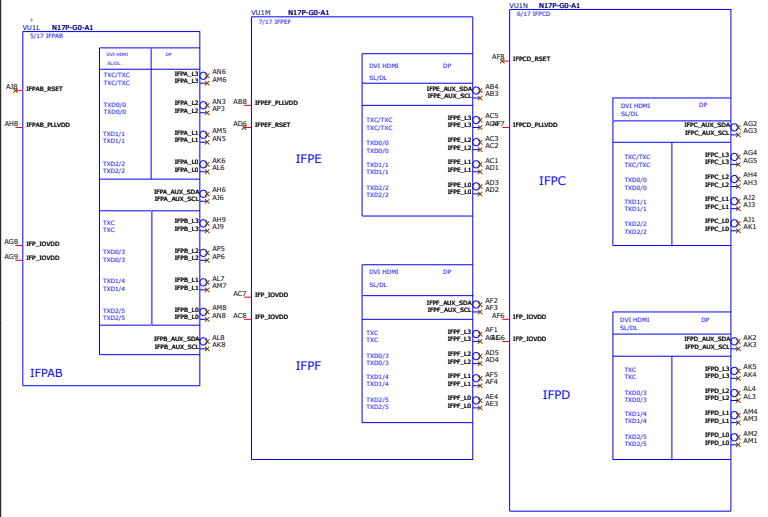


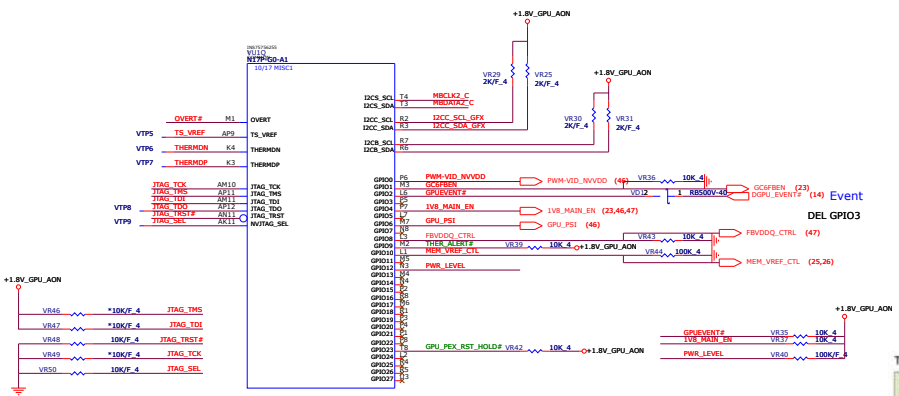


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/ WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDQ power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.5
GPIO16	GC6M: GPU_PEX_RST_HOLD#	O	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted Input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted Input. See Figure 14.5
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	PCS_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

STRAP[2:0] VRAM Table for N17P-G0/G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	Quanta P/N	FBVDD/Q	
0x0	GDDR5 256Mx32 7 GHz	Samsung	SAMSUNG/K4G80325FB-HC28	AKG5QGDT515	1.5V	Default
0x1	GDDR5 256Mx32 7 GHz	Micron MICRON/MT51J256M32HF-70:A		AKG5QGUTL10	1.5V	
0x7	GDDR5 128Mx32 7 GHz	Samsung	SAMSUNG/K4G41325FE-HC28	AKG5PGUT508	1.5V	
0x8	GDDR5 128Mx32 7 GHz	ELPIDA ELPIDA/EDW4032BABG-70-F-D		AKG5PW0TL12	1.55V	

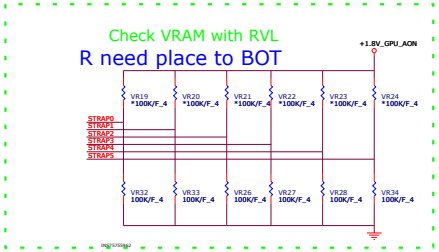
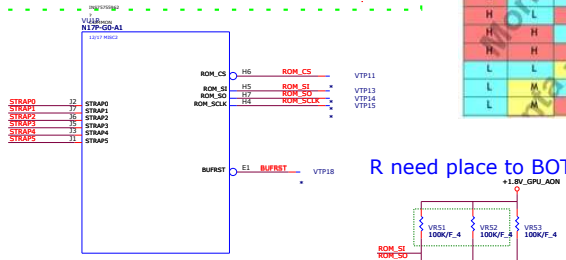
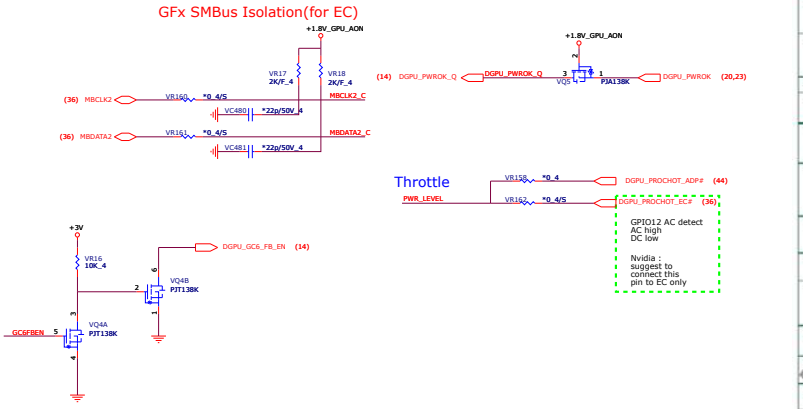
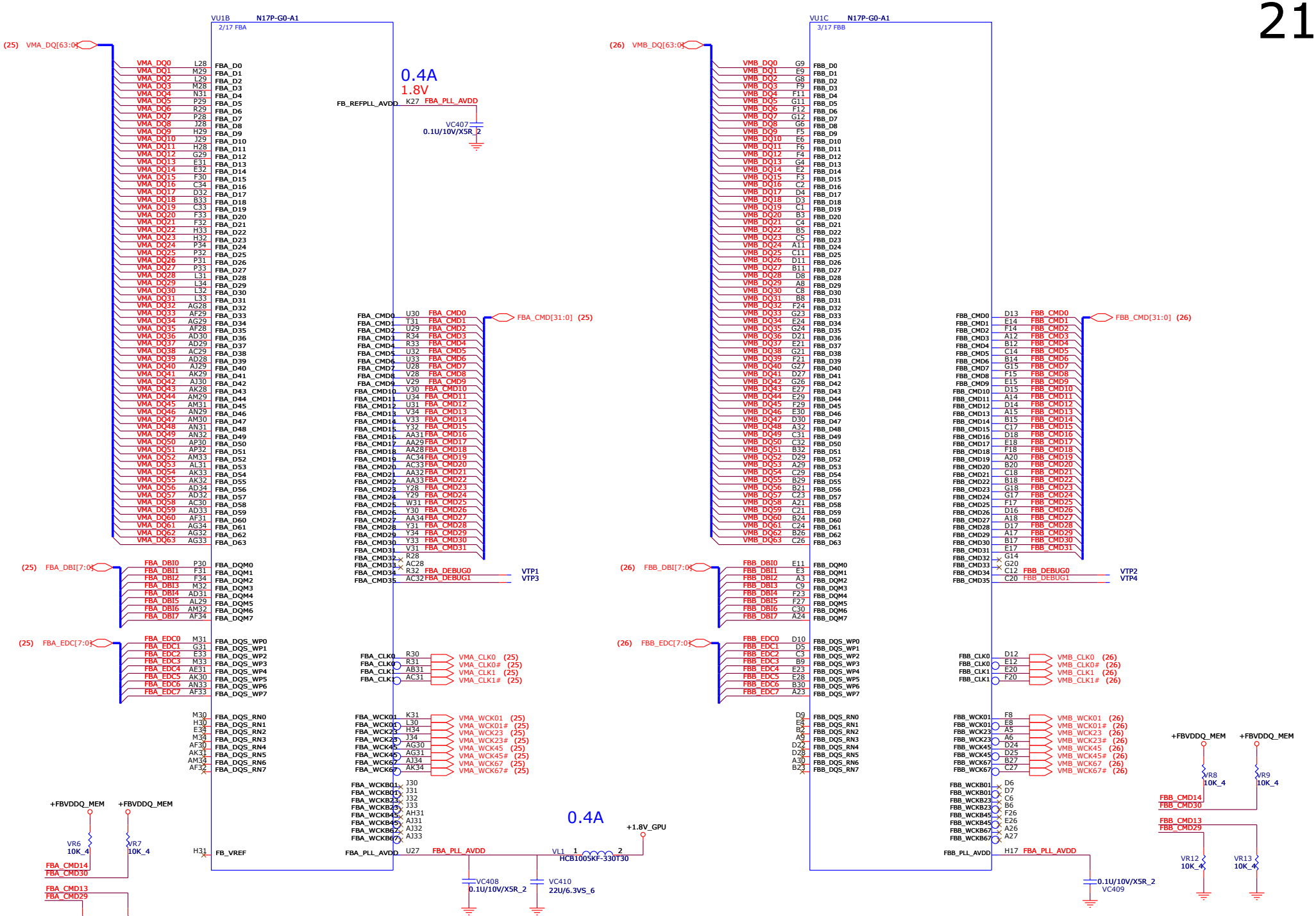


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)



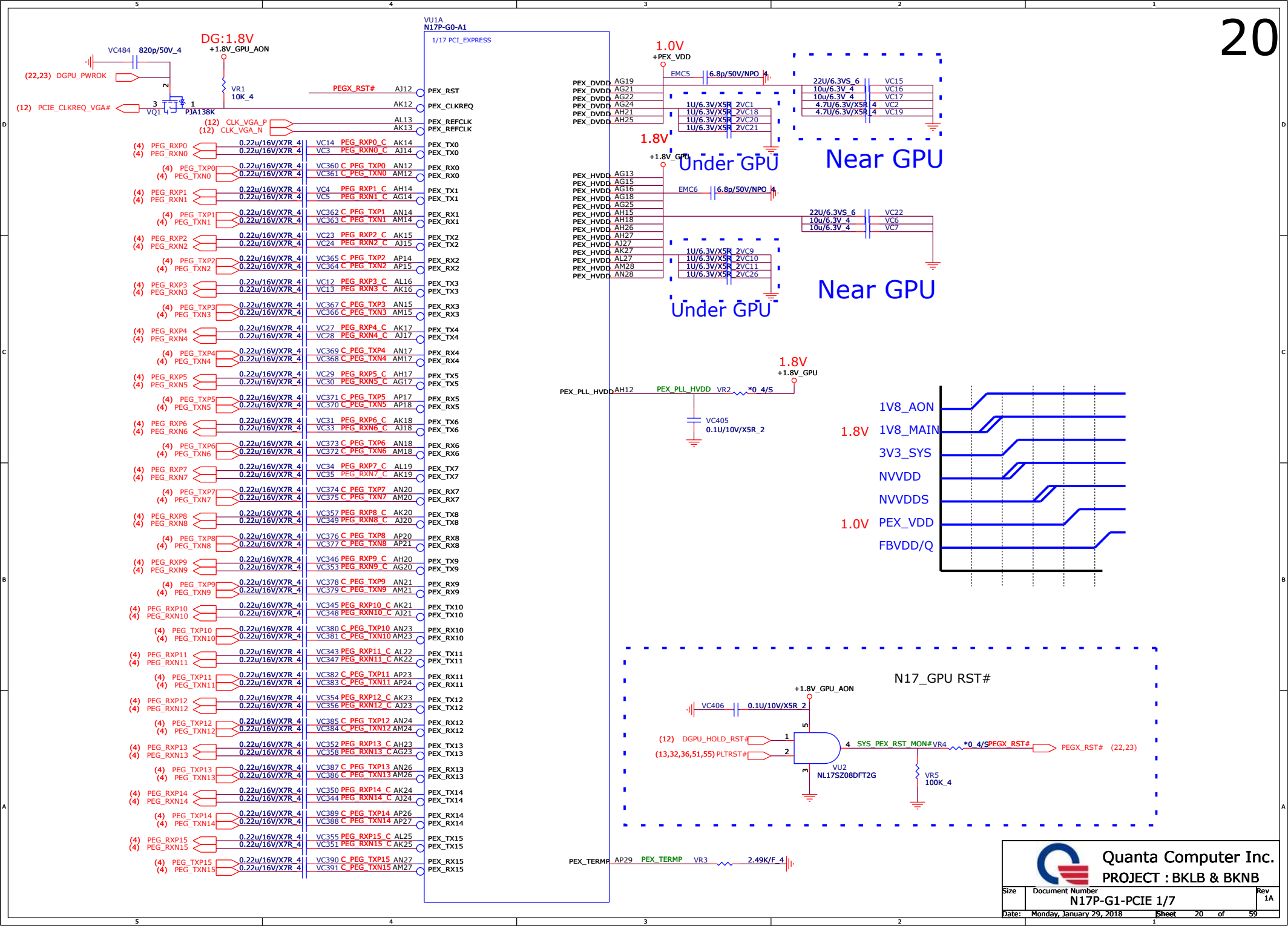




Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	N17P-G1-MEMORY 1/7	1A

Date: Monday, January 29, 2018 Sheet 21 of 59



Quanta Computer Inc.			
PROJECT : BKLB & BKNB			
Size	Document Number		Rev
	N17P-G1-PCIE 1/7		1A
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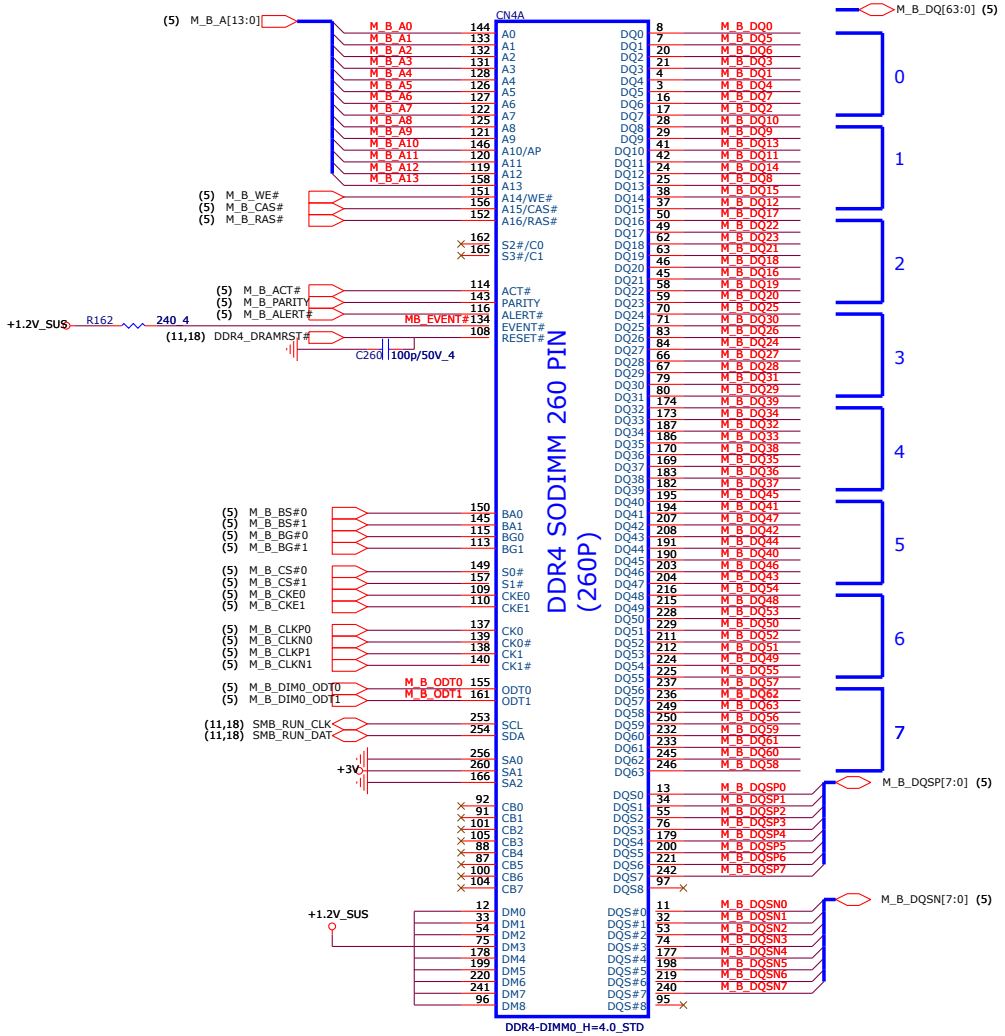
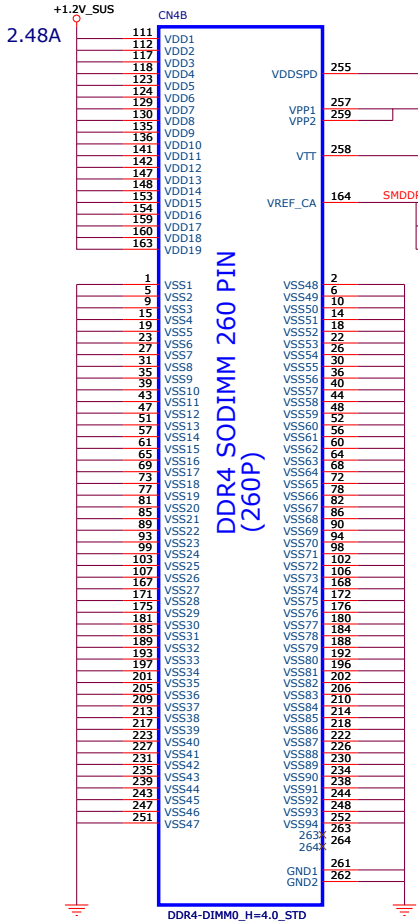
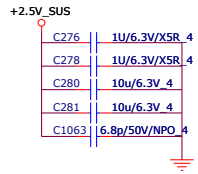
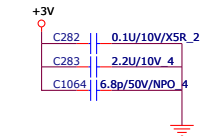
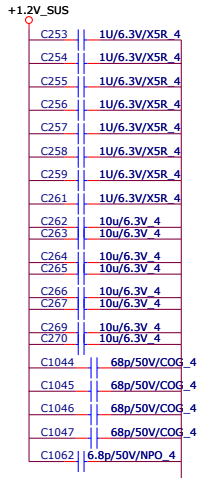
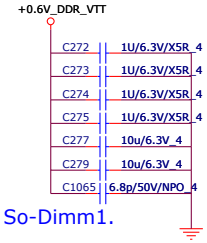








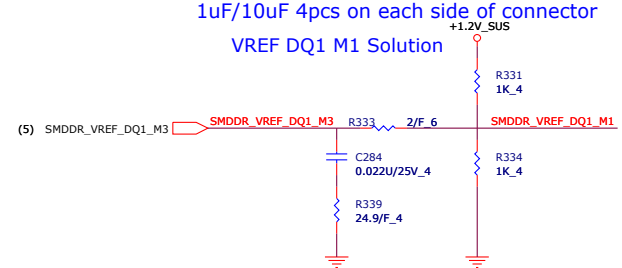




Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

VREF DQ1 M1 Solution



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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	DDR4 DIMM1-RVS(4.0H)	1A

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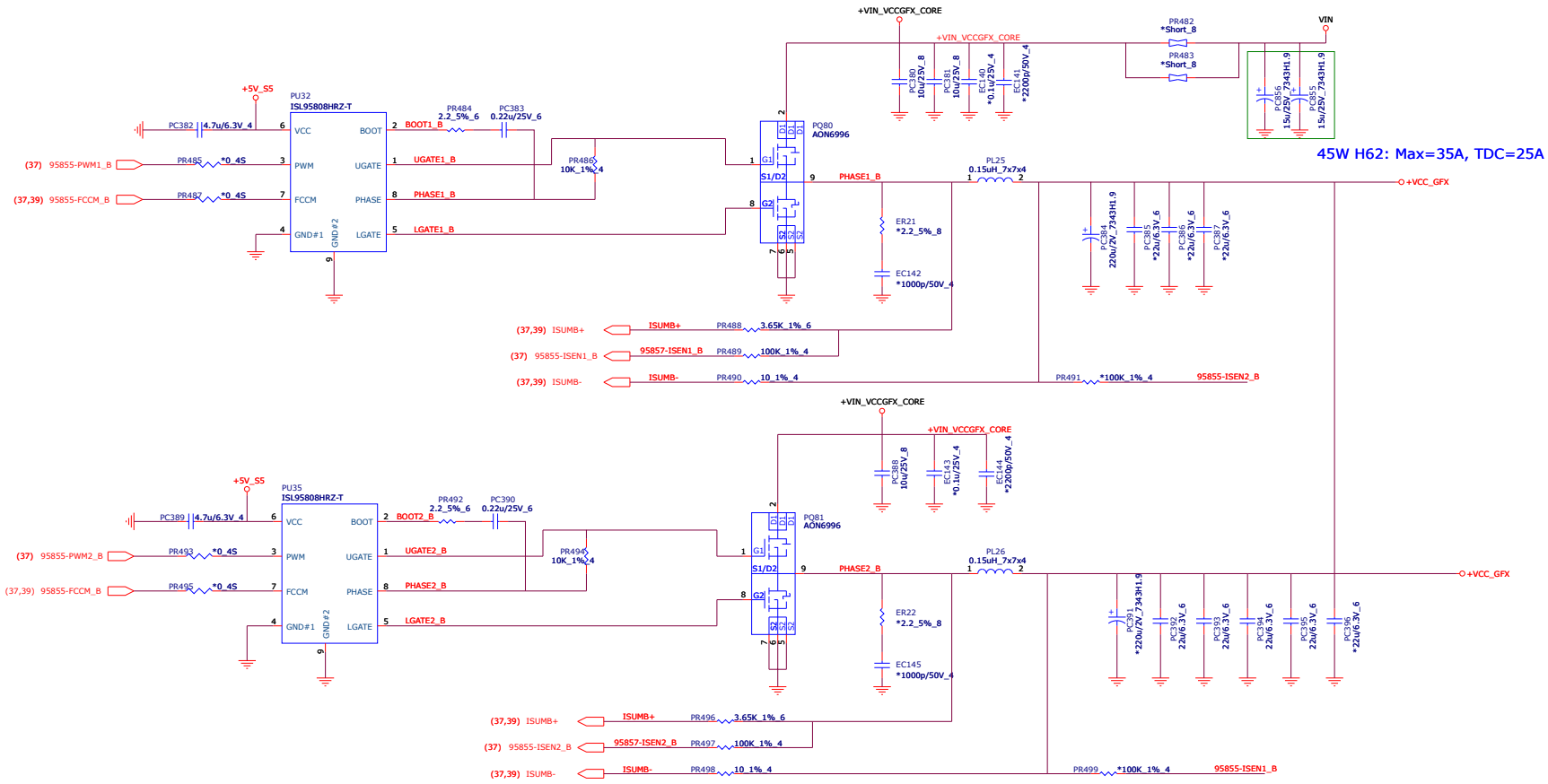
GFX_CORE



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	GTCORE (ISL95829A)	1A

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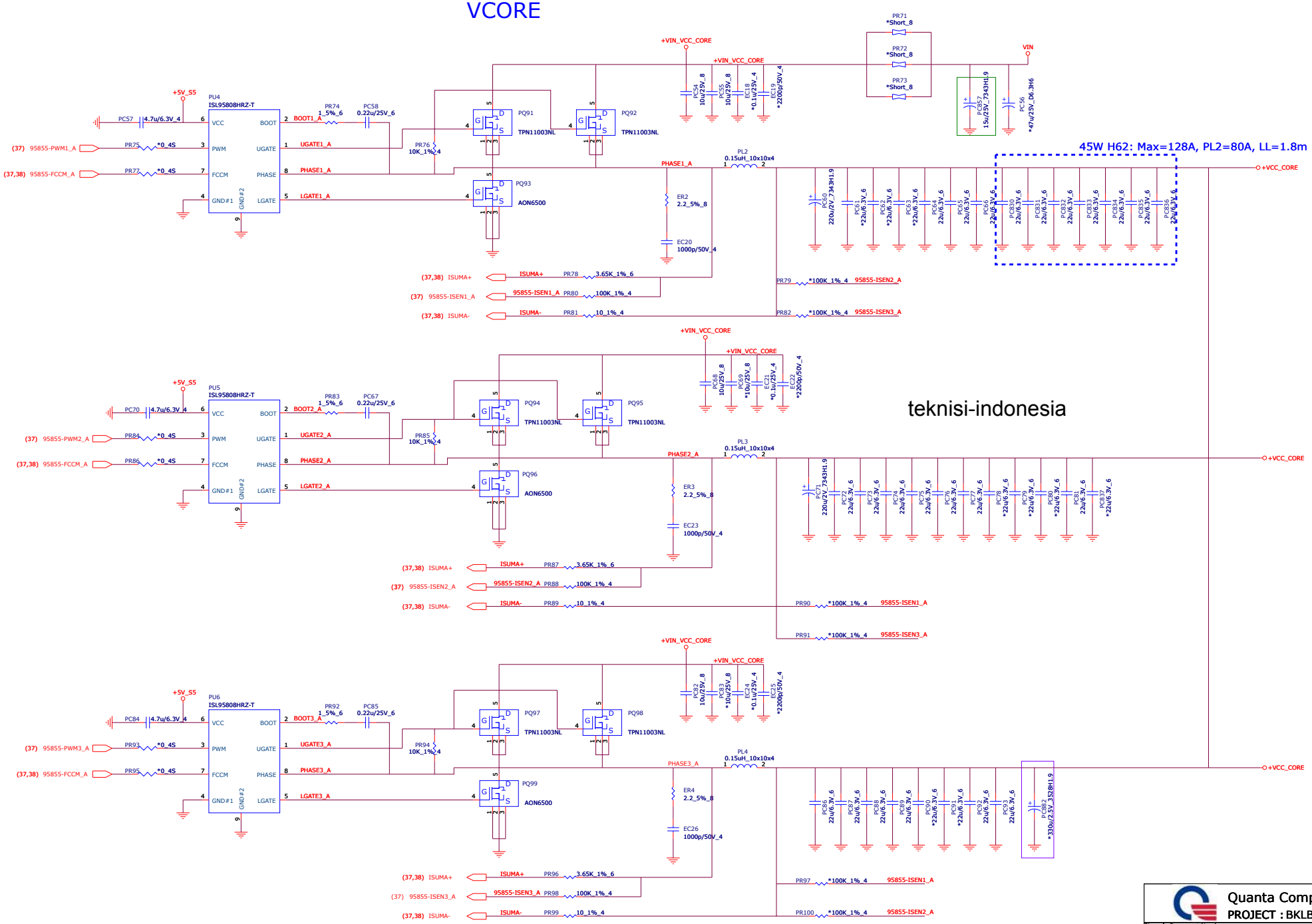
VCORE



Quanta Computer Inc.	
PROJECT : BKLB & BKNB	
Size	Document Number: VCCORE/GTCORE/VCCSA (ISL95829A) Rev: 1A
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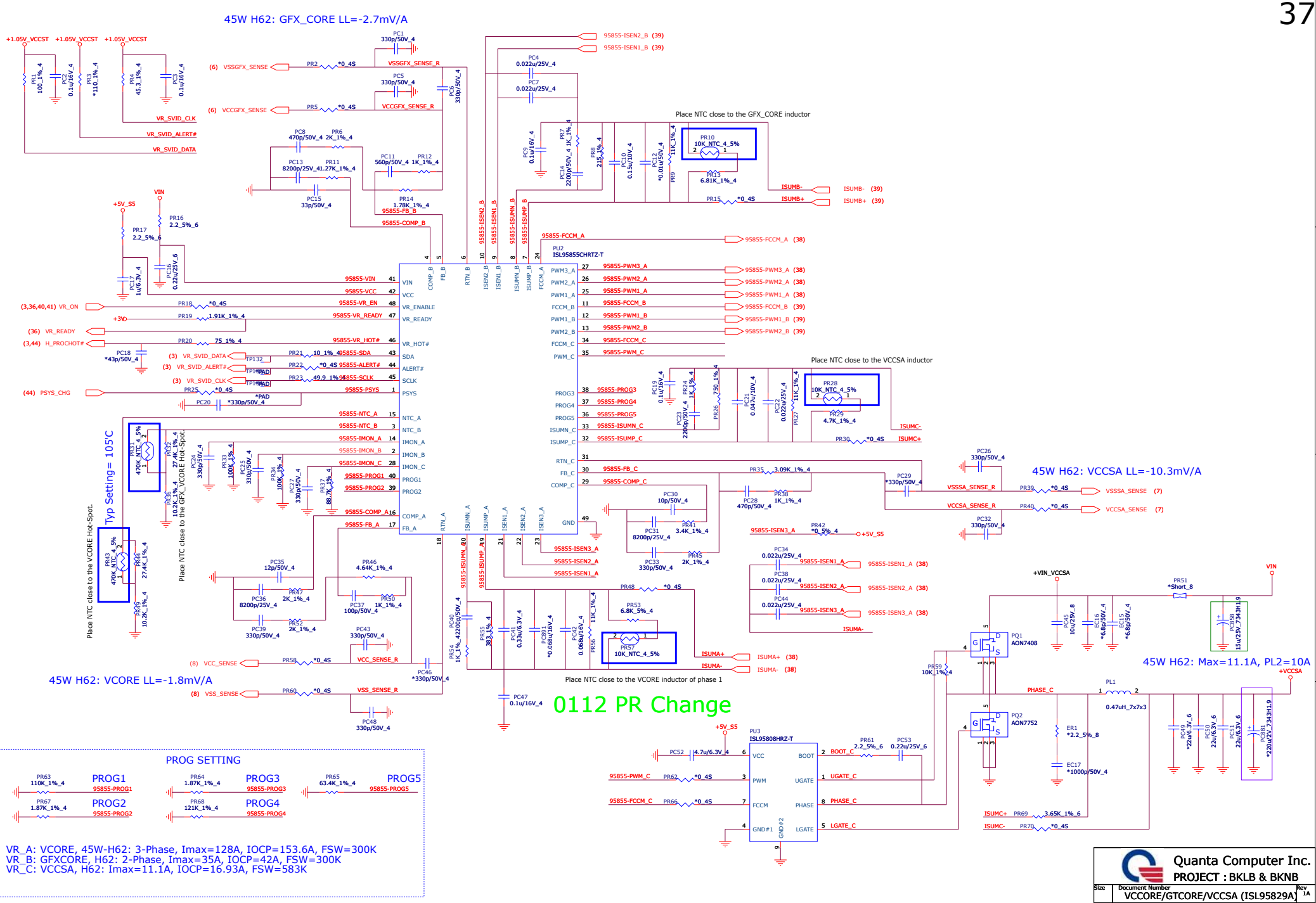

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	VCCORE/GTCORE/VCCSA (ISL95829A)	1A

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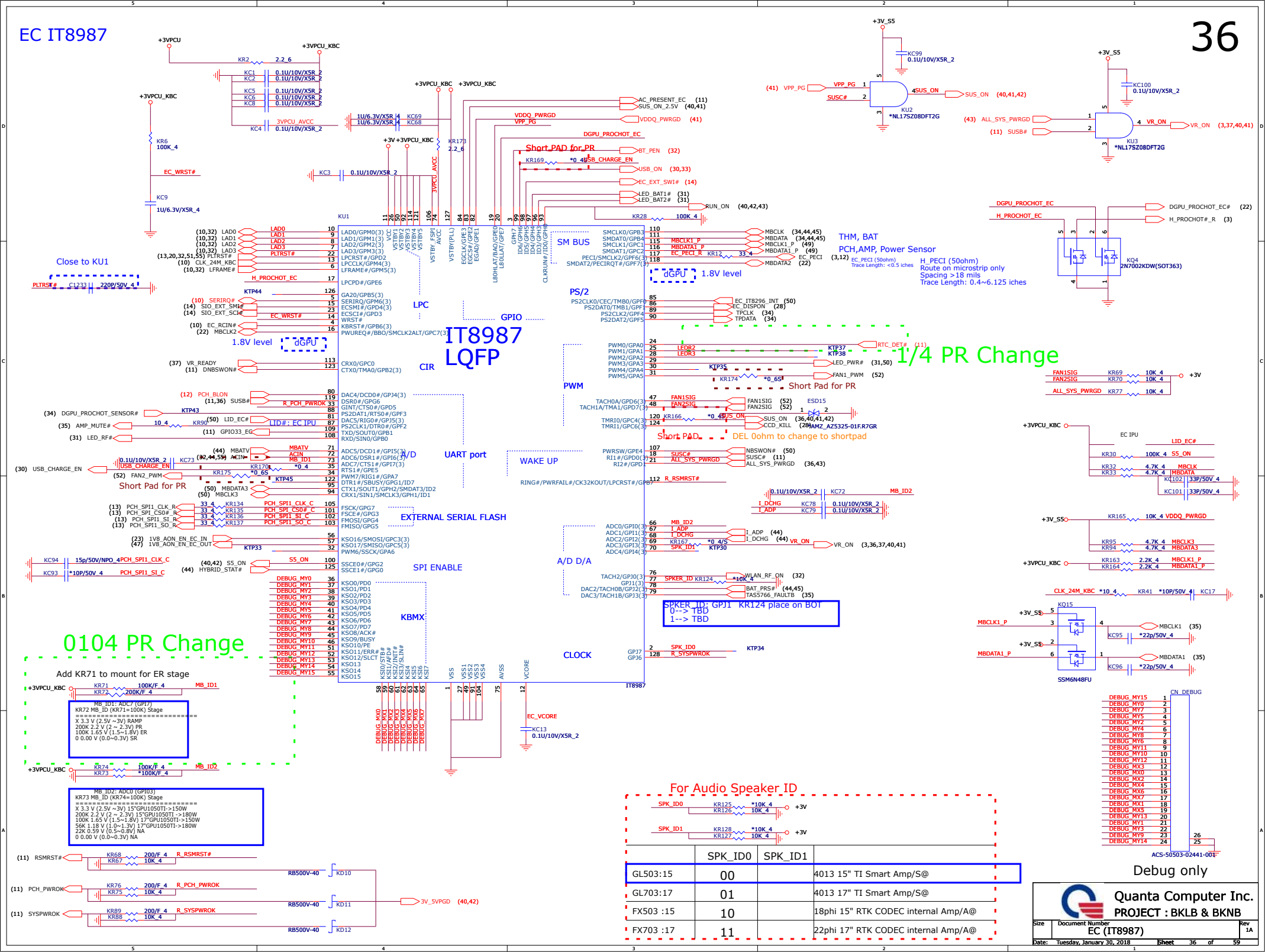
EC IT8987



	SPK_ID0	SPK_ID1	
GL503:15	00		4013 15" TI Smart Amp/S@
GL703:17	01		4013 17" TI Smart Amp/S@
FX503 :15	10		18phi 15" RTK CODEC internal Amp/A@
FX703 :17	11		22phi 17" RTK CODEC internal Amp/A@

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	EC (IT8987)	1A
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Audio Code (ALC295)

0130 PR Change FOR ESD

Universal Jack

0110 PR Change FOR ESD

ALC295

QFN48(6*6)

Thermal pad=DGND

Linear regulator +1.8VA

AGND

DGND

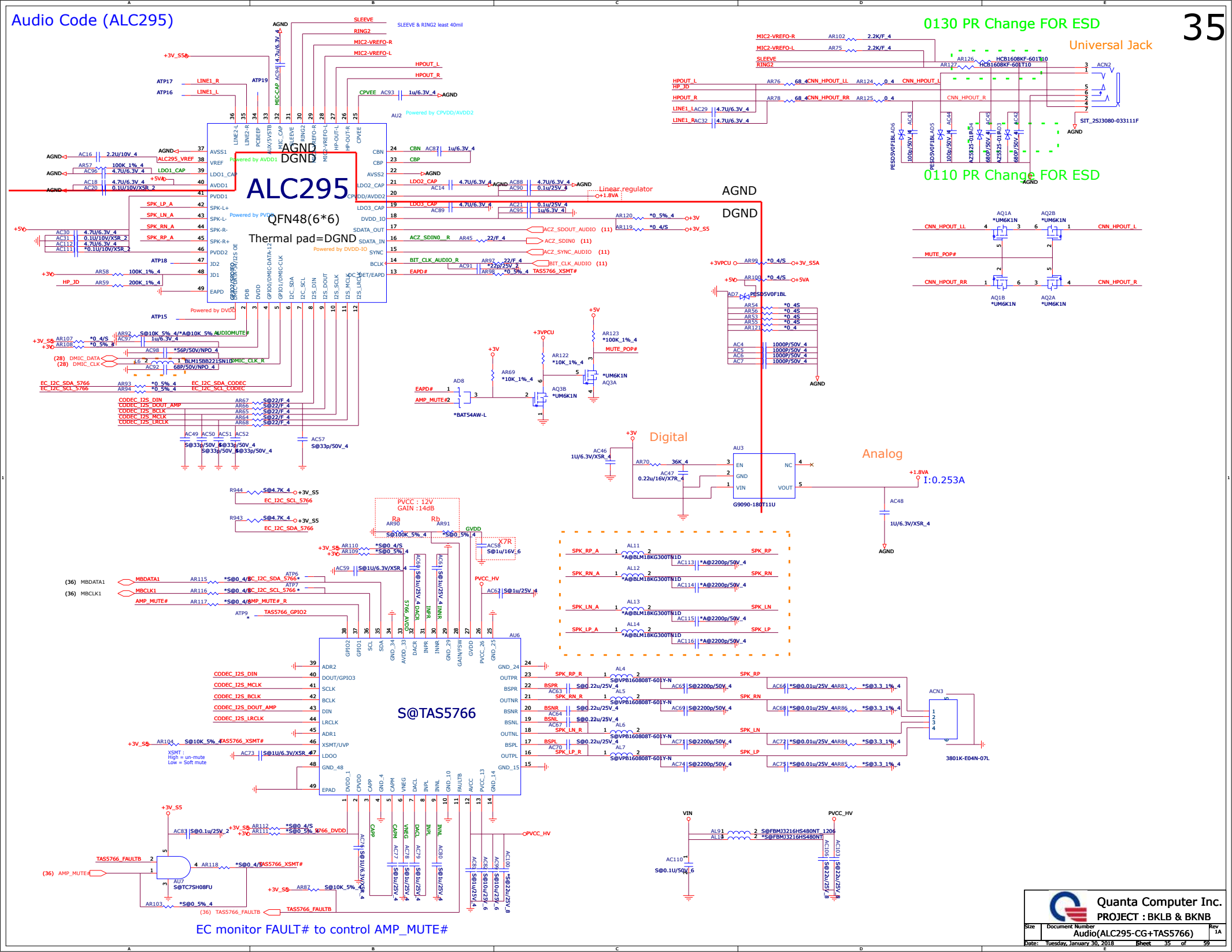
Digital

Analog

I:0.253A

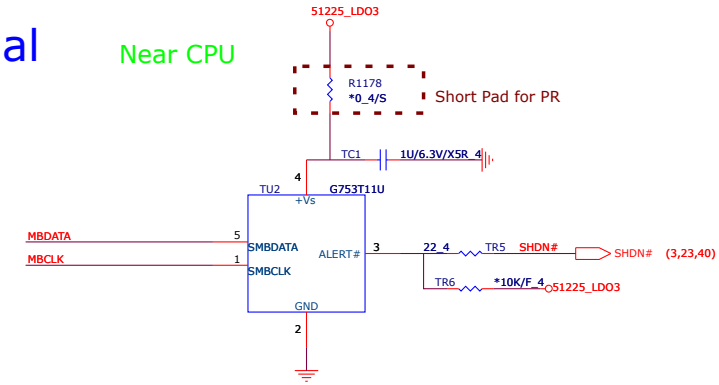
S@TAS5766

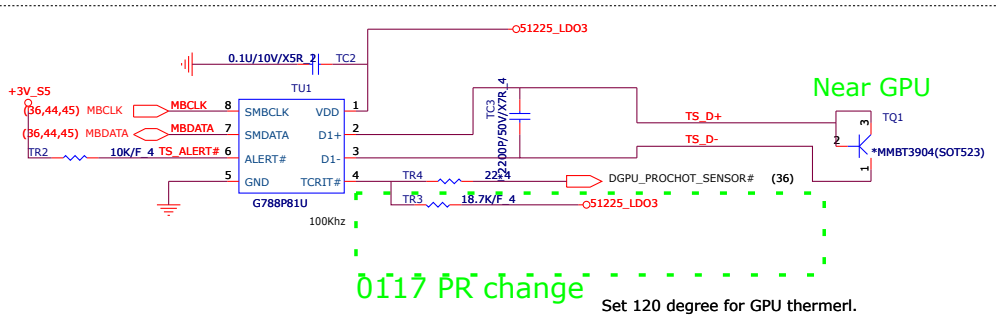
EC monitor FAULT# to control AMP_MUTE#



Thermal

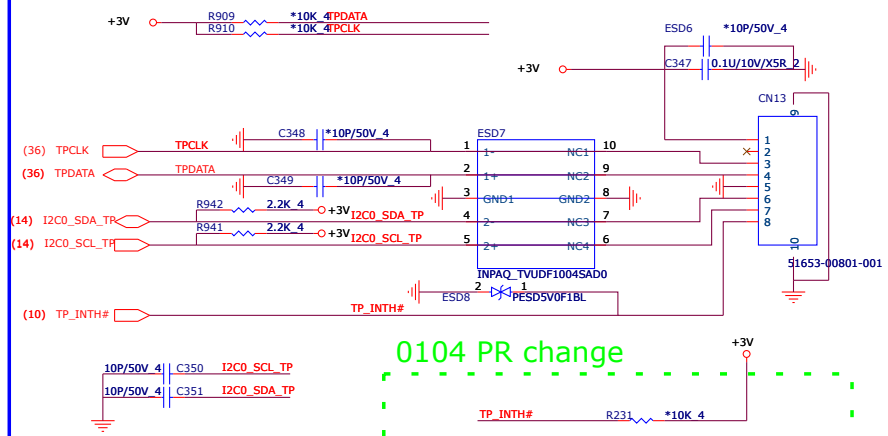
Near CPU





www.teknisi-indonesia.com

Touch Pad Connector AA type



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	THM/TP	1A
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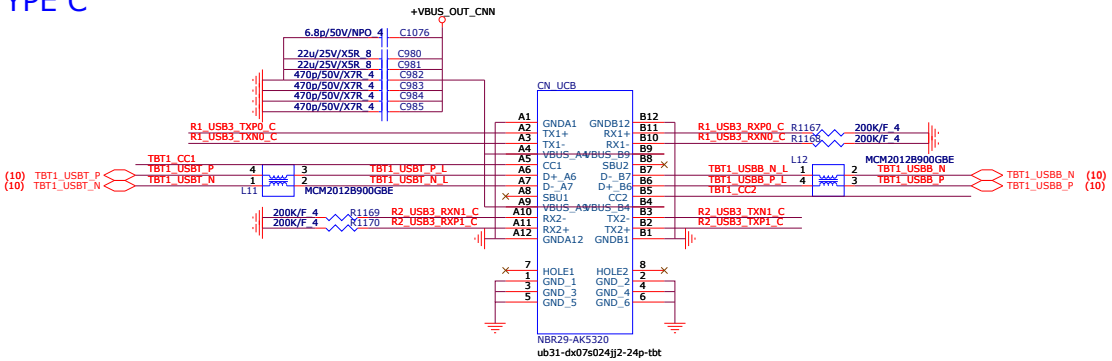
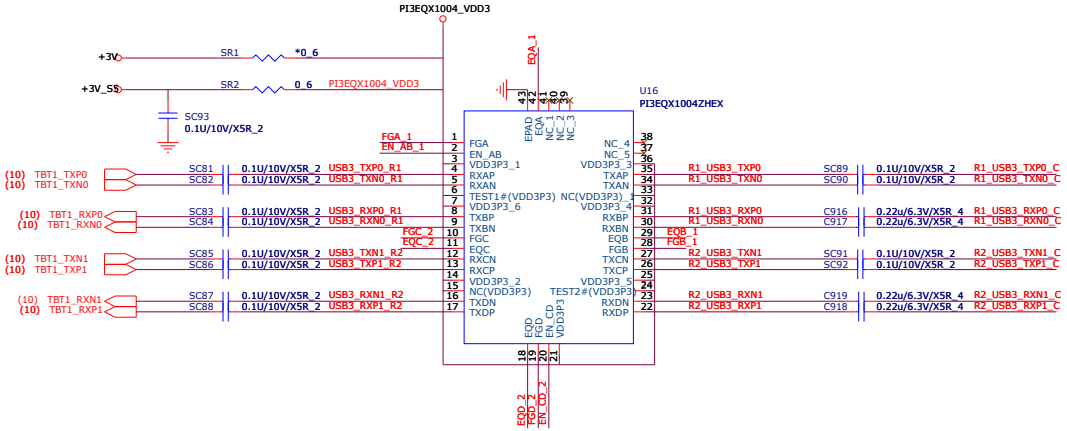
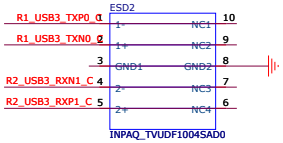
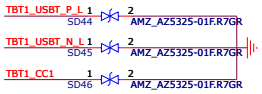
TYPE C

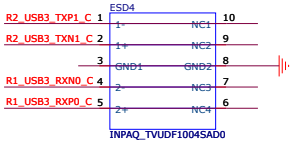
VBUS:5V

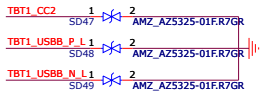


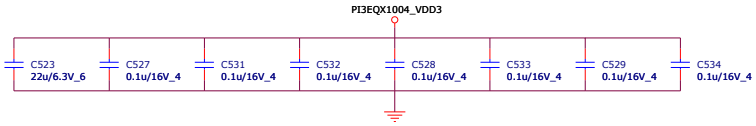












Channel Enable Setting:

EN_AB/EN_CD are the channel enable pins for channels A&B and C&D respectively

	Channel Enable Setting
EN	*Setting*
0	Disabled
1	Enabled (Default)

Equalization Setting:

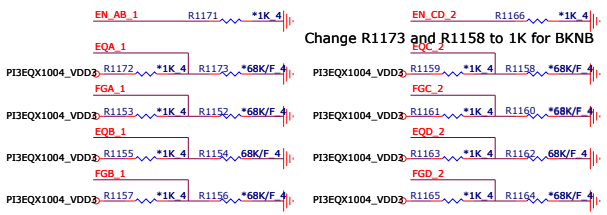
EQA/B/C/D are the selection pins for the equalization selection

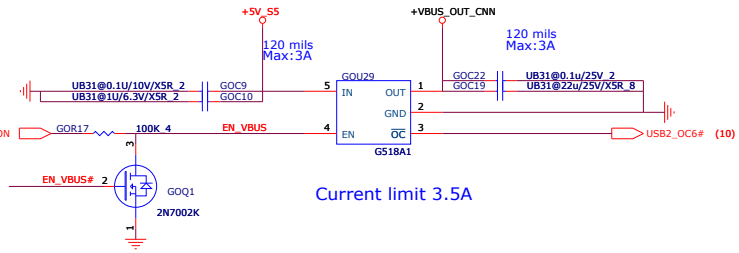
	Equalizer setting (dB)	
EQA/B/C/D	*@2.5GHz*	*@5GHz*
0 (Tie 0Ω to GND)	5.1	10.9
R (Tie Rext to GND)	1.9	6.7
F (Leave Open)	3.5	8.9 (Default)
1 (Tie 0Ω to VDD)	6.8	13.1

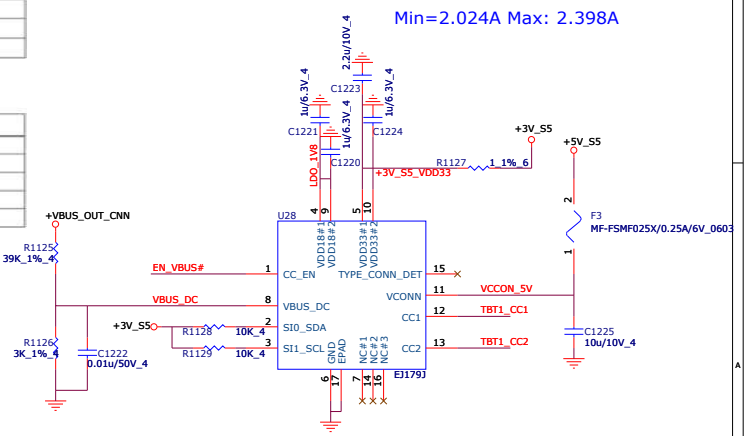
Flat Gain Setting:

FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-3
R (Tie Rext to GND)	-1.5
F (Leave Open)	0 (Default)
1 (Tie 0Ω to VDD)	+2







Quanta Computer Inc.

PROJECT : BKLB & BKNB

Size	Document Number	Rev
	USB-C(USB/PD/DP-OUT)	1A

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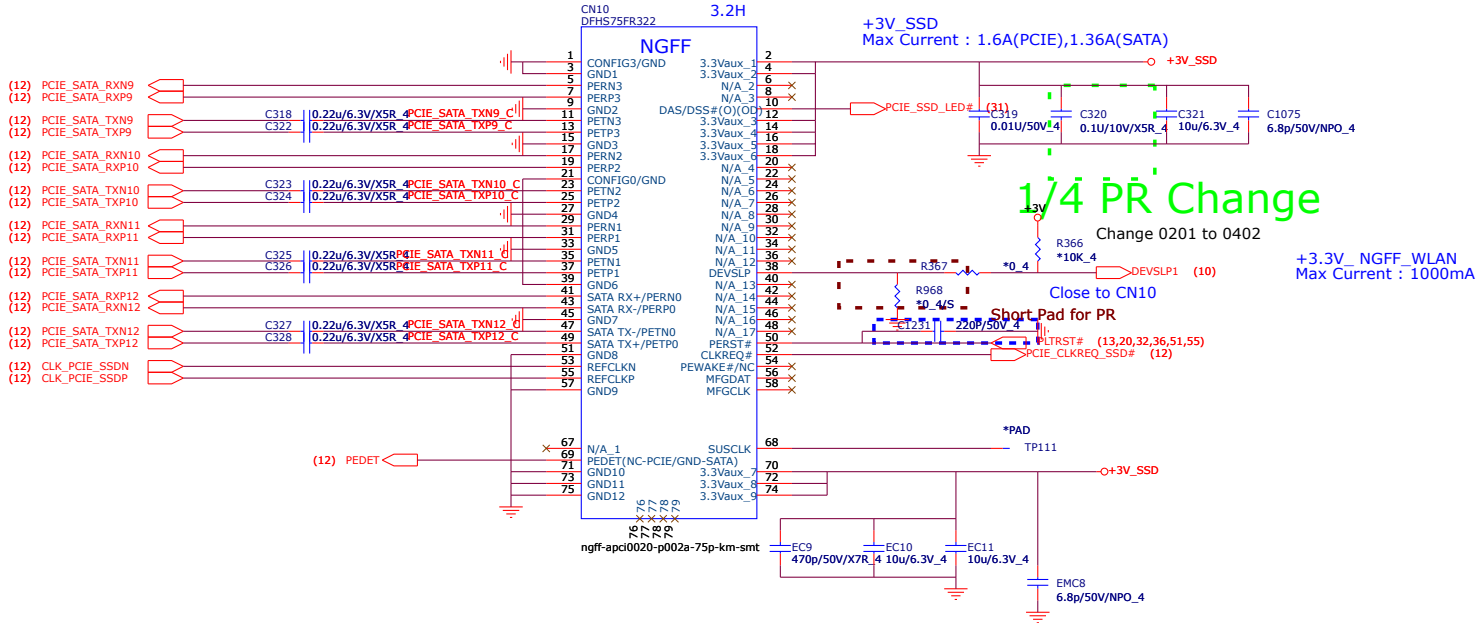
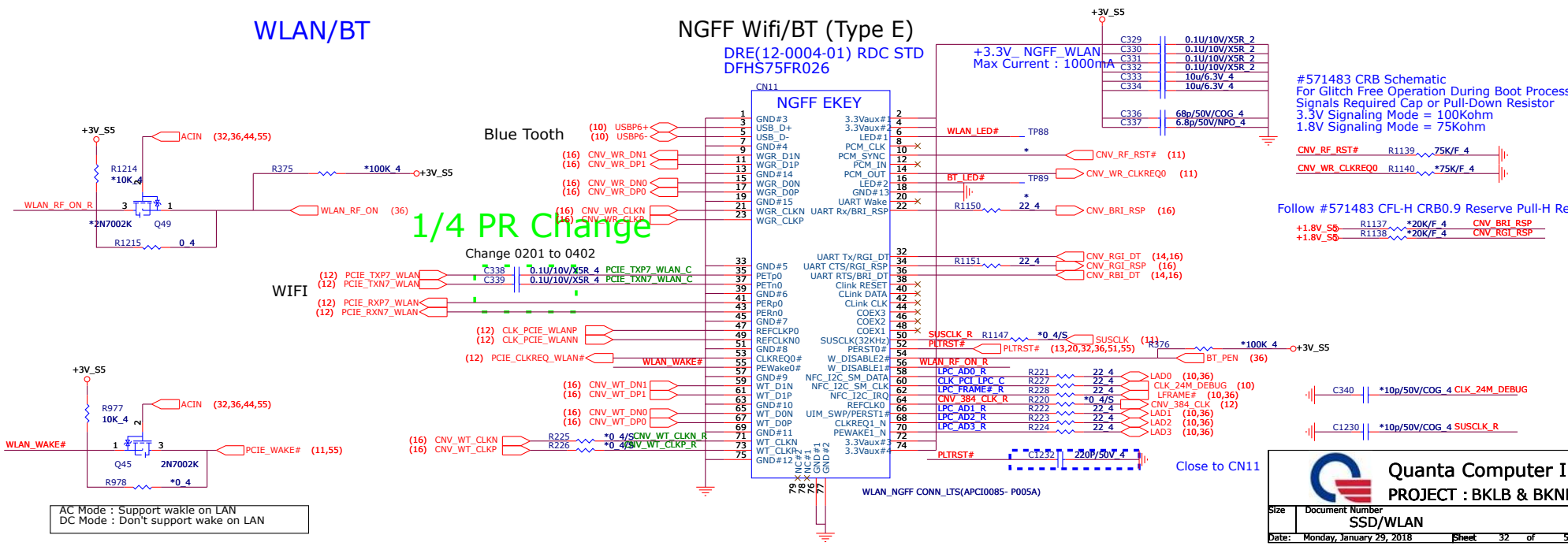
SSD



WLAN/BT



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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	SSD/WLAN	1A

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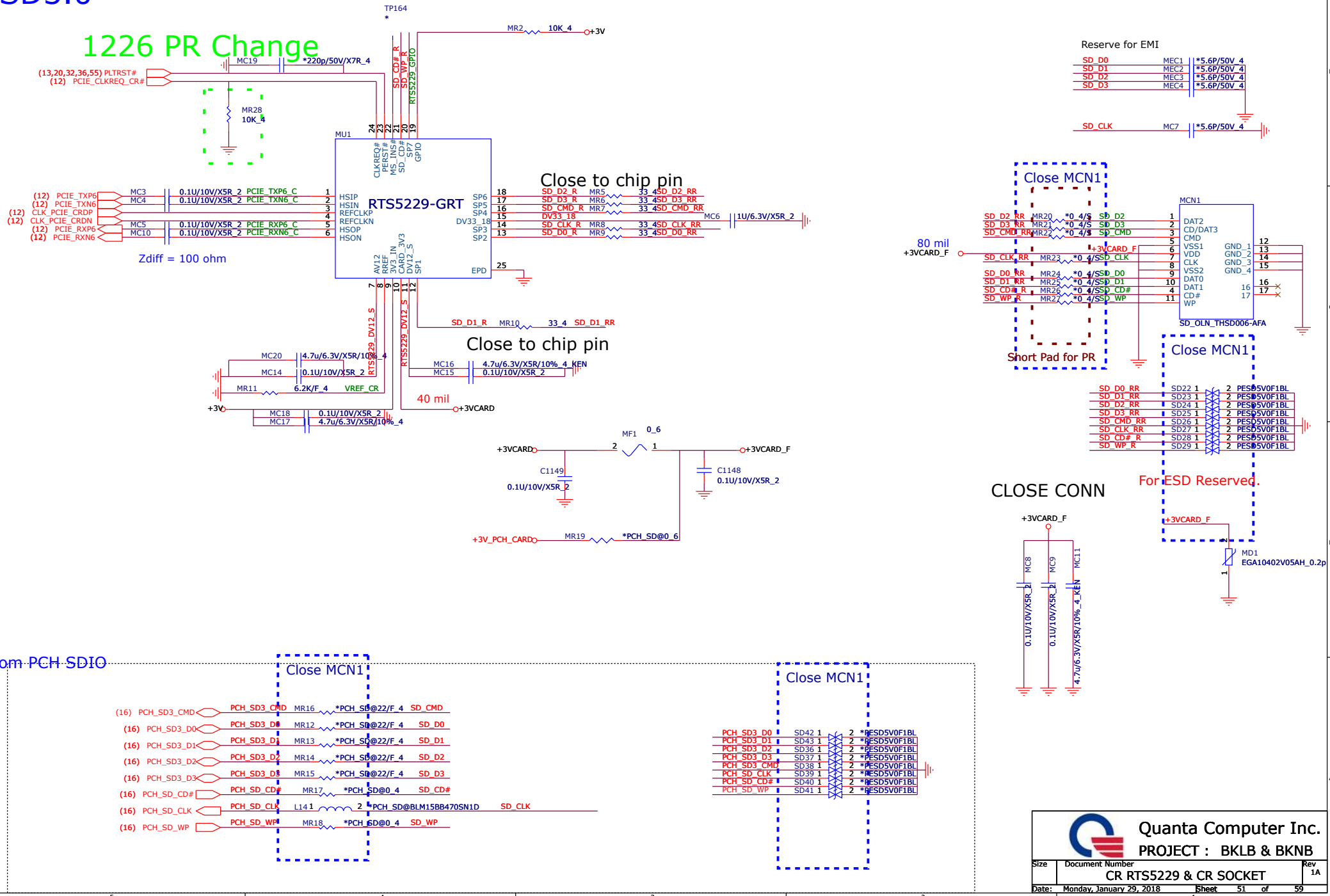
SD3.0

1226 PR Change



Quanta Computer Inc.

PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CR RTS5229 & CR SOCKET	1A
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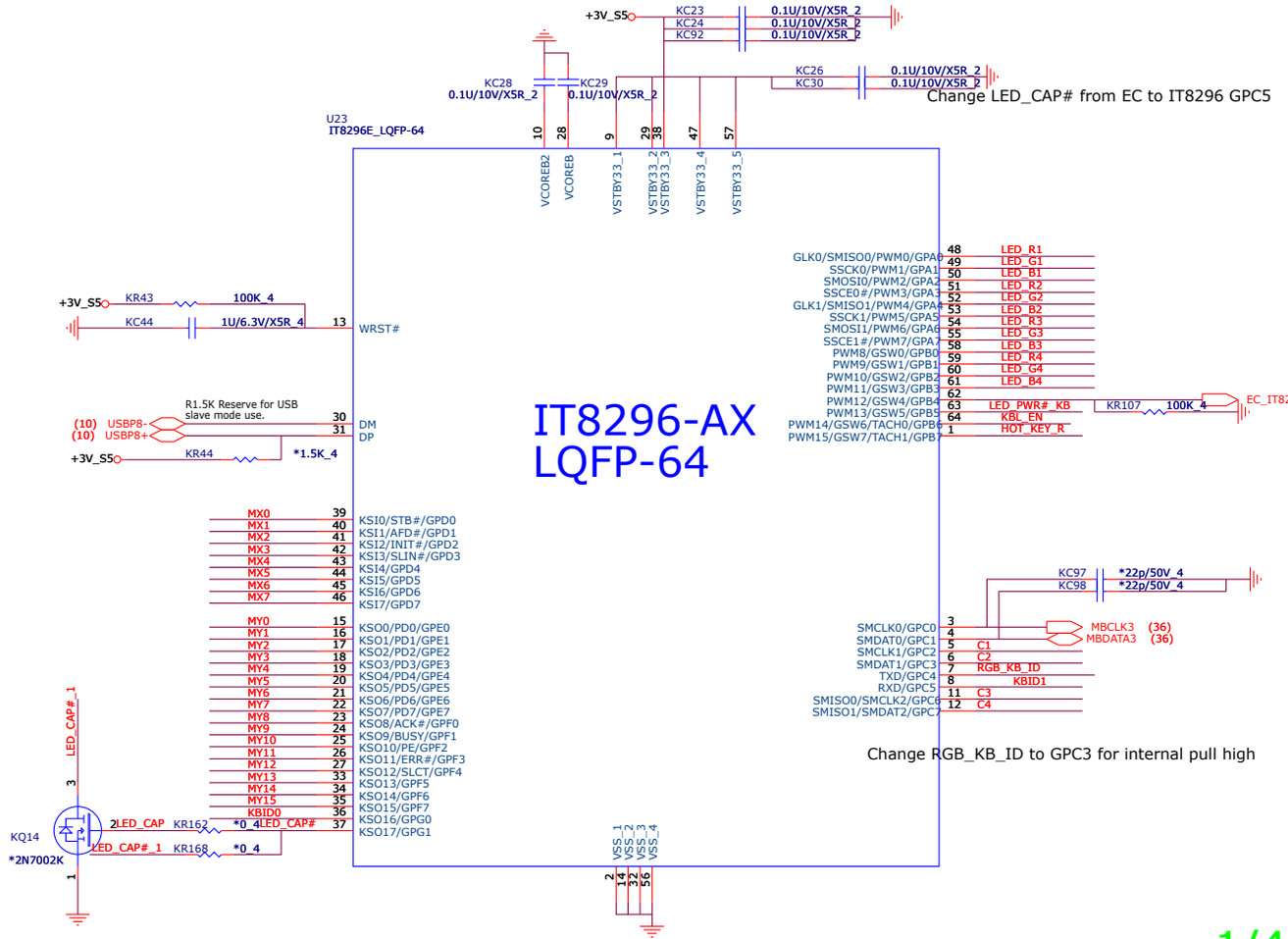
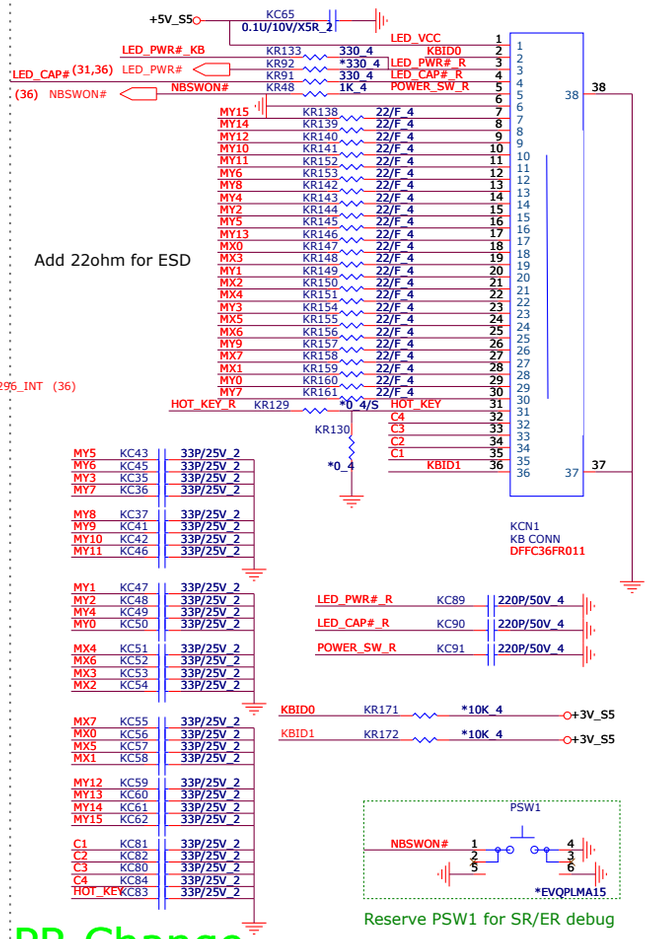
ANTI Ghost with LED driver



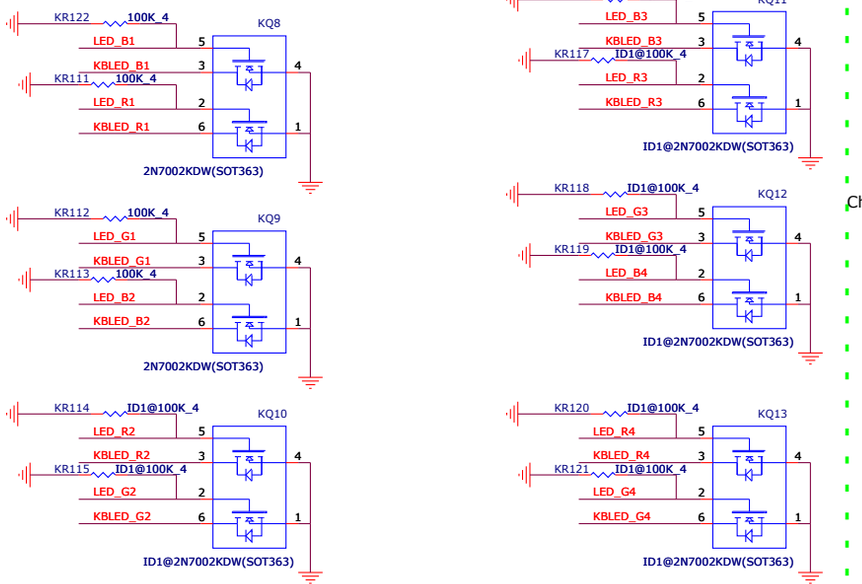
KEYBOARD Con.

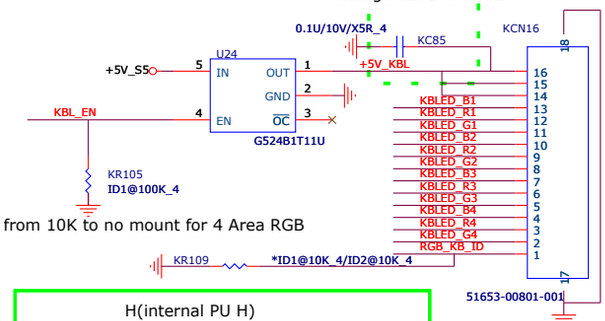


1/4 PR Change

Change 0201 to 0402

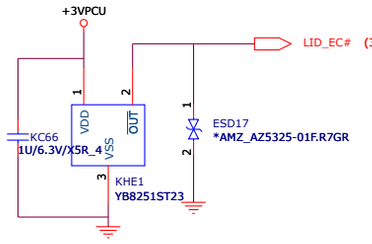
RGB KB LED Driver





Change KR109 from 10K to no mount for 4 Area RGB

H(internal PU H)		
	4 Area RGB	1 Area R
KR109	No mount	Mount



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	EC(IT8296)	1A
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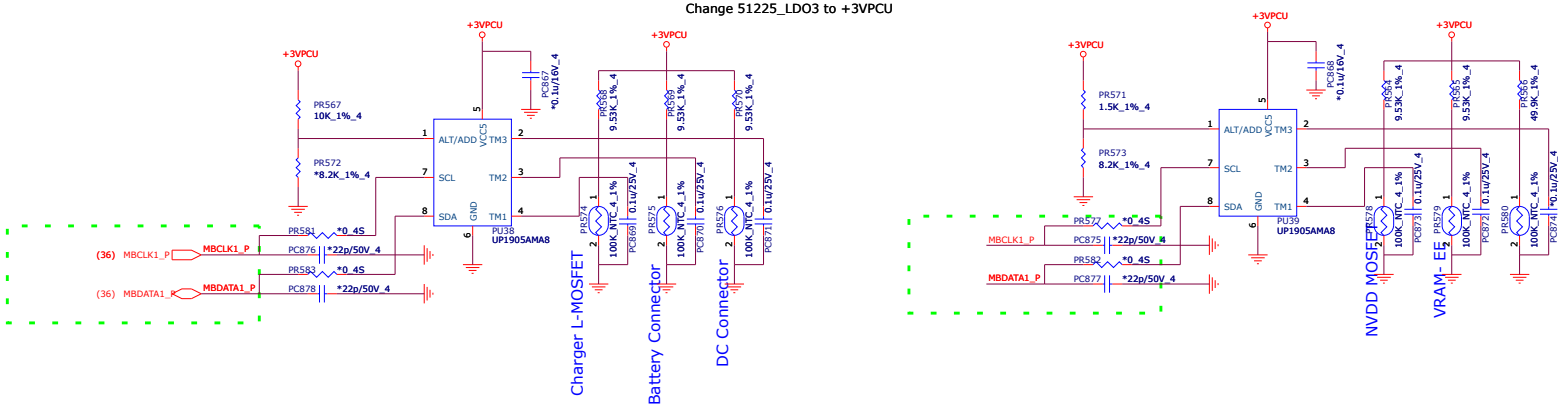
Change 51225_LDO3 to +3VPCU



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
		1A

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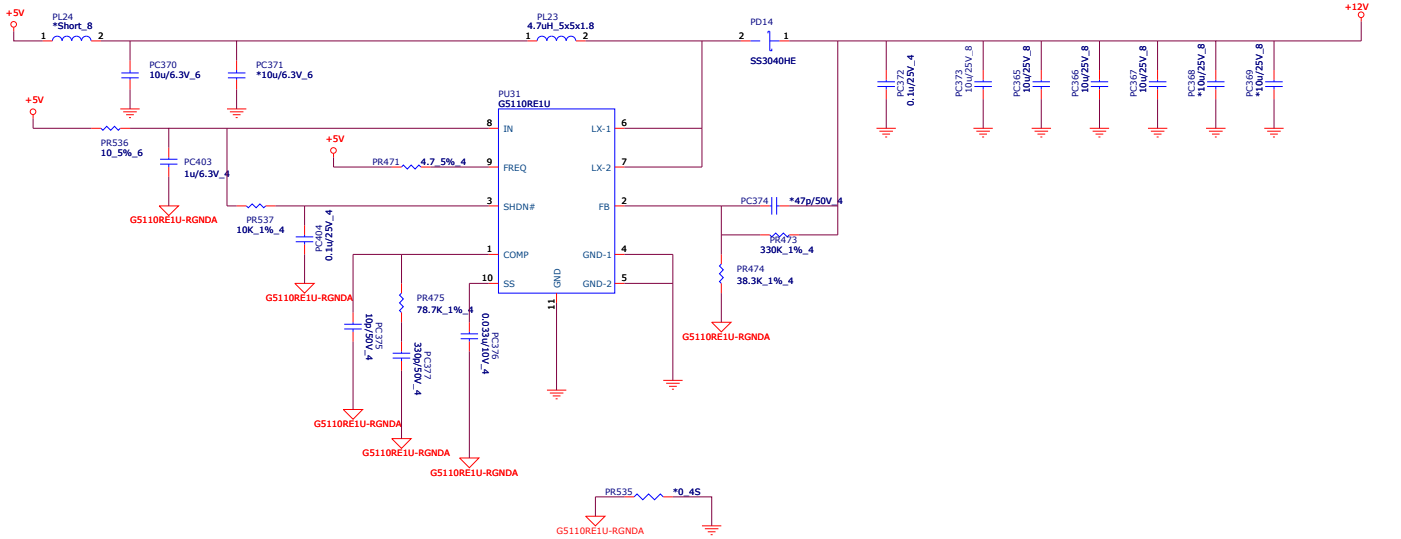
+12V for FAN

Max 1.4A



Quanta Computer Inc.

PROJECT : BKLB & BKNB

Size	Document Number	Rev
	+1.0V_VCCEDRAM / +12V	1A

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FBVDDQ - 1.5V_GPU

0112 PR Change

Fsw Setting=430KHz

OC Setting

1.35V / 1.55V
MAX: 20A, TDC:11A

FBVDDQ Voltage Setting: 1.55V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12K	3.57K	1.55V
0	12K	3.57K	1.35V

FBVDDQ Voltage Setting: 1.50V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	2.94K	1.35V

R1

R2

VOUT=(1+R1/R2)*0.7

Load Switch for GPU

0112 PR Change

1.6A

1.0V
Max: 1.1A

Discharge

+1.0V_GPU

1.0V
Max: 1.1A

Rg

Rh

Vout1 = (1+Rg/Rh)*0.8

+1.8V_GPU_AON

Max: 1.8A
TDC: 1.0A

Rg

Rh

Vout1 = (1+Rg/Rh)*0.8

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PROJECT : BKLB & BKNB
Size | Document Number: +FBVDDQ (G5318) | Rev 1A
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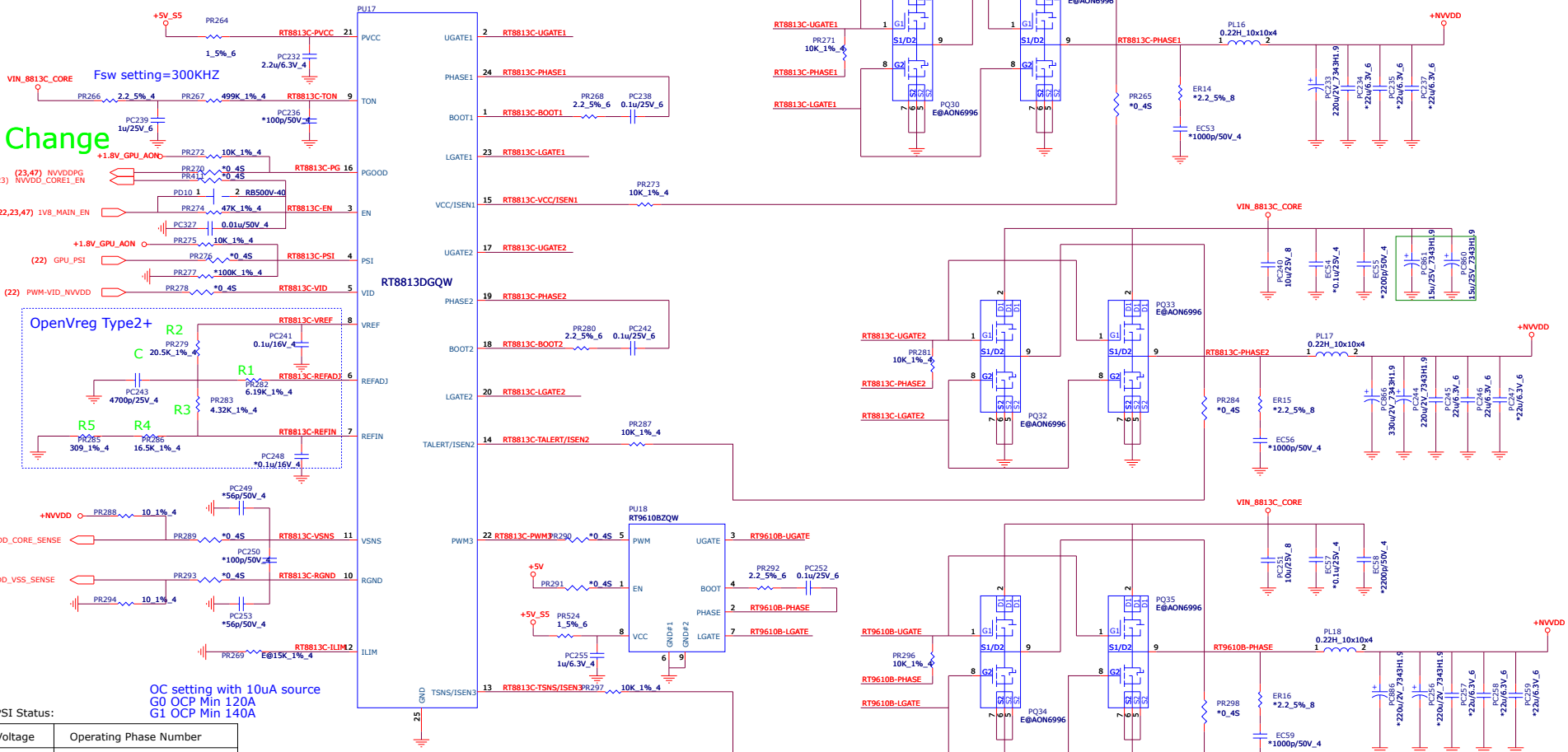
+NVVDD

N17P-G0 (TDP=40W)
Max=100A, TDC=50A
N17P-G1 (TDP=50W)
Max=124A, TDC=59A

0112 PR Change



GPU_PSI Status:

PSI Voltage	Operating Phase Number
0V~0.4V	1 phase with DEM
0.8V~1V	1 phase with CCM
1.4V~5.5V	Active phase with CCM (Only for 2 or 3 hases)

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	dGPU CORE (RT8813D)	A
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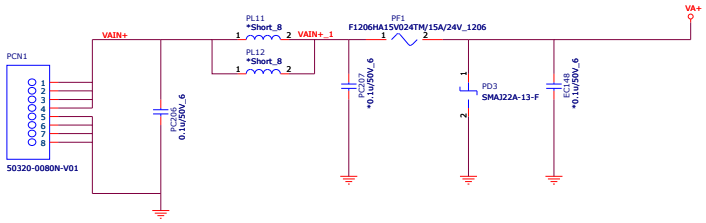
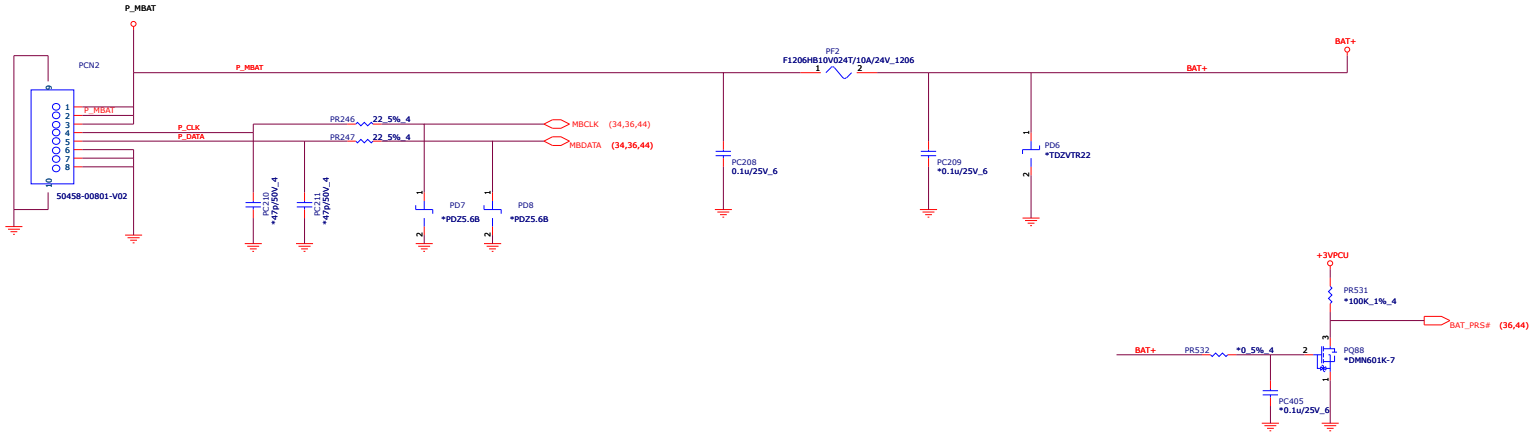
AC IN

AC ADAPTOR IN CONN



BAT IN



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Size	Document Number	Rev
	ADP IN / BAT IN / Thermal Protection	1A

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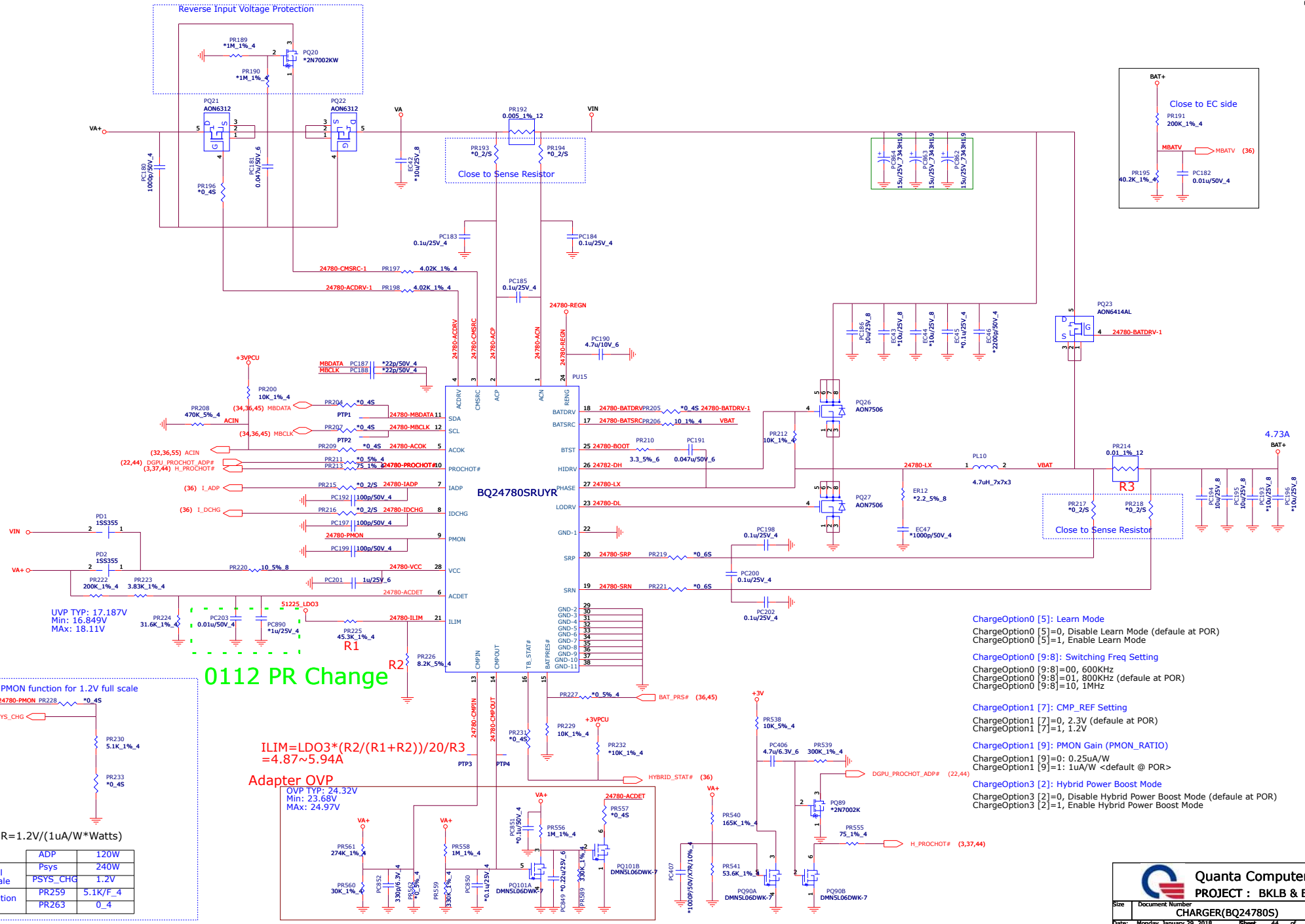
Reverse Input Voltage Protection
PR189 *1M_1%_4
PQ20 *2N7002KW
PR190 *1M_1%_4
PQ21 AON6312
PQ22 AON6312
VA+
VA
VIN
PR192 0.005_1%_12
PR193 *0_2/S
PR194 *0_2/S
Close to Sense Resistor
PC180 1000p/50V_4
PC181 0.047u/50V_6
PR196 *0_4S
EC42 *10u/25V_8
PC183 0.1u/25V_4
PC184 0.1u/25V_4
PC185 0.1u/25V_4
PC190 4.7u/10V_6
24780-CMSRC-1
24780-ACDRV-1
PR197 4.02K_1%_4
PR198 4.02K_1%_4
24780-REGN
+3VPCU
MBDATA PC187 *22p/50V_4
MBCLK PC188 *22p/50V_4
PR200 10K_1%_4
PR208 470K_5%_4
ACIN
(34,36,45) MBDATA
(34,36,45) MBCLK
PR204 *0_4S
PR207 *0_4S
PTP1
PTP2
PR209 *0_4S 24780-ACOK
PR211 *0_5%_4
PR213 75_1%_4 24780-PROCHOT#
(32,36,55) ACIN
(22,44) DGPU_PROCHOT_ADP#
(3,37,44) H_PROCHOT#
(36) I_ADP
PR215 *0_2/S 24780-IADP
PC192 100p/50V_4
(36) I_DCHG
PR216 *0_2/S 24780-IDCHG
PC197 100p/50V_4
24780-PMON
PC199 100p/50V_4
PD1 1SS355
PD2 1SS355
VIN
VA+
PR220 10_5%_8
24780-VCC
PC201 1u/25V_6
24780-ACDET
PR222 200K_1%_4
PR223 3.83K_1%_4
UVP TYP: 17.187V
Min: 16.849V
MAx: 18.11V
PR224 31.6K_1%_4
PC203 0.01u/50V_4
PC890 *1u/25V_4
51225_LDO3
PR225 45.3K_1%_4
24780-ILIM
R1
R2
PR226 8.2K_5%_4
0112 PR Change
PU15
BQ24780SRUYR
ACDRV
CMSRC
ACP
ACN
REGN
SDA
SCL
ACOK
PROCHOT#
IADP
IDCHG
PMON
VCC
ACDET
ILIM
CMPIN
CMPOUT
TB_STAT#
BATPRES#
BATDRV
BATSRC
BTST
HIDRV
PHASE
LODRV
GND-1
SRP
SRN
GND-2
GND-3
GND-4
GND-5
GND-6
GND-7
GND-8
GND-9
GND-10
GND-11
24780-BATDRV
PR205 *0_4S 24780-BATDRV-1
24780-BATSRC
PR206 10_1%_4 VBAT
24780-BOOT
PR210 3.3_5%_6
PR191 0.047u/50V_6
24782-DH
24780-LX
24780-DL
24780-SRP
PR219 *0_6S
24780-SRN
PR221 *0_6S
PC198 0.1u/25V_4
PC200 0.1u/25V_4
PC202 0.1u/25V_4
PR227 *0_5%_4
BAT_PRS# (36,45)
PR229 10K_1%_4
PR231 *0_4S
PR232 *10K_1%_4
+3VPCU
HYBRID_STAT# (36)
24780-CMPIN
24780-CMPOUT
PTP3
PTP4
ILIM=LDO3*(R2/(R1+R2))/20/R3
=4.87~5.94A
Adapter OVP
OVP TYP: 24.32V
Min: 23.68V
MAx: 24.97V
PC851 *0.1u/50V_4
PR556 1M_1%_4
PR557 *0_4S
PR561 274K_1%_4
PR560 30K_1%_4
PC852 330p/6.3V_4
PR558 1M_1%_4
PR559 330K_1%_4
PC850 *0.1u/25V_4
PQ101A DMN5L06DWK-7
PQ101B DMN5L06DWK-7
PC849 *0.22u/25V_6
PR569 330K_1%_4
PR538 10K_5%_4
PC406 4.7u/6.3V_6
PR539 300K_1%_4
DGPU_PROCHOT_ADP# (22,44)
PQ89 *2N7002K
PR555 75_1%_4
H_PROCHOT# (3,37,44)
PR540 165K_1%_4
PR541 53.6K_1%_4
PC407 *1000P/50V/X7R/10%_4
PQ90A DMN5L06DWK-7
PQ90B DMN5L06DWK-7
PC186 10u/25V_8
EC43 *10u/25V_8
EC44 *10u/25V_8
EC45 *0.1u/25V_4
EC46 *2200p/50V_4
PQ23 AON6414AL
24780-BATDRV-1
PQ26 AON7506
PQ27 AON7506
PR212 10K_1%_4
PL10 4.7uH_7x7x3
VBAT
PR214 0.01_1%_12
R3
ER12 *2.2_5%_8
EC47 *1000p/50V_4
PR217 *0_2/S
PR218 *0_2/S
Close to Sense Resistor
4.73A
BAT+
PC194 10u/25V_8
PC195 10u/25V_8
PC193 *10u/25V_8
PC196 *10u/25V_8
BAT+
Close to EC side
PR191 200K_1%_4
MBATV
MBATV (36)
PR195 40.2K_1%_4
PC182 0.01u/50V_4
PC864 150u/25V_7343H19
PC863 150u/25V_7343H19
PC862 150u/25V_7343H19
PMON function for 1.2V full scale
24780-PMON PR228 *0_4S
(37) PSYS_CHG
PR230 5.1K_1%_4
PR233 *0_4S
R=1.2V/(1uA/W*Watts)
Full Scale
ADP 120W
Psys 240W
Location
PSYS_CHG 1.2V
PR259 5.1K/F_4
PR263 0_4
ChargeOption0 [5]: Learn Mode
ChargeOption0 [5]=0, Disable Learn Mode (defaule at POR)
ChargeOption0 [5]=1, Enable Learn Mode
ChargeOption0 [9:8]: Switching Freq Setting
ChargeOption0 [9:8]=00, 600KHz
ChargeOption0 [9:8]=01, 800KHz (defaule at POR)
ChargeOption0 [9:8]=10, 1MHz
ChargeOption1 [7]: CMP_REF Setting
ChargeOption1 [7]=0, 2.3V (defaule at POR)
ChargeOption1 [7]=1, 1.2V
ChargeOption1 [9]: PMON Gain (PMON_RATIO)
ChargeOption1 [9]=0: 0.25uA/W
ChargeOption1 [9]=1: 1uA/W <default @ POR>
ChargeOption3 [2]: Hybrid Power Boost Mode
ChargeOption3 [2]=0, Disable Hybrid Power Boost Mode (defaule at POR)
ChargeOption3 [2]=1, Enable Hybrid Power Boost Mode
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CHARGER(BQ24780S)
Rev 1A
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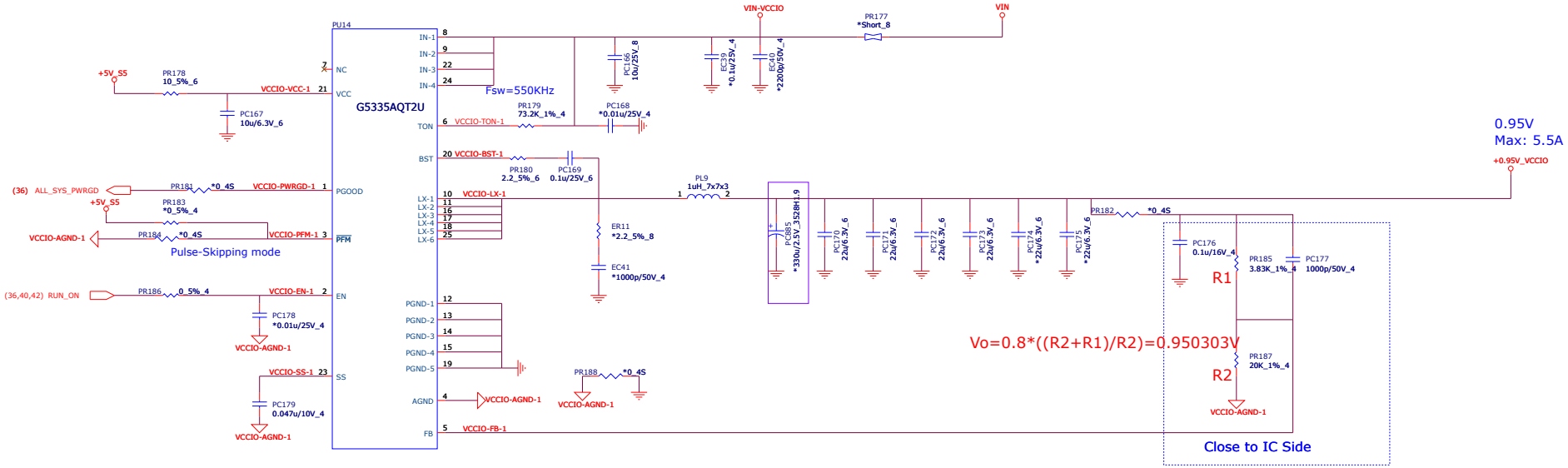
+VCCIO (Fix VCCIO=0.95V)



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	+0.95V_VCCIO	1A

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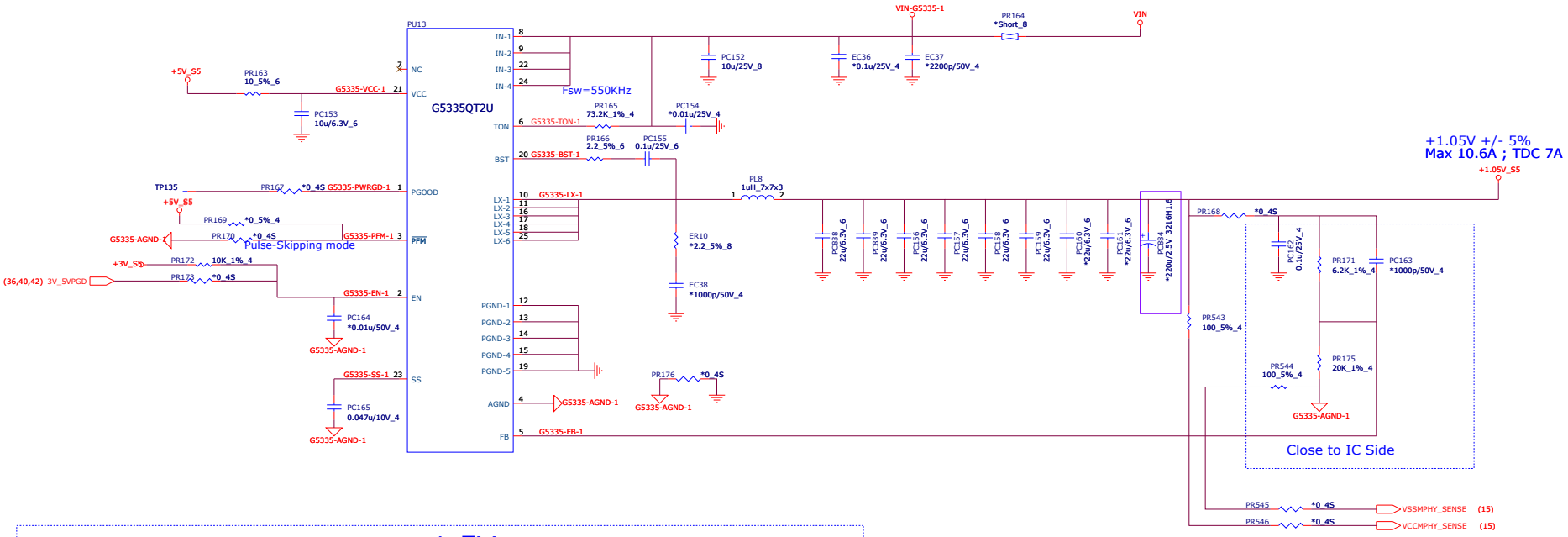
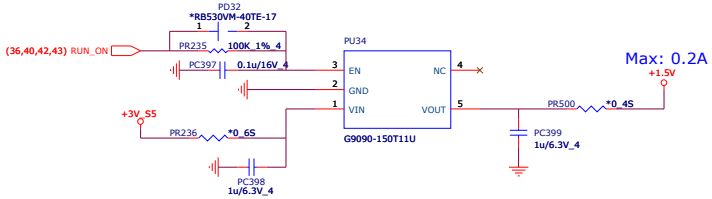
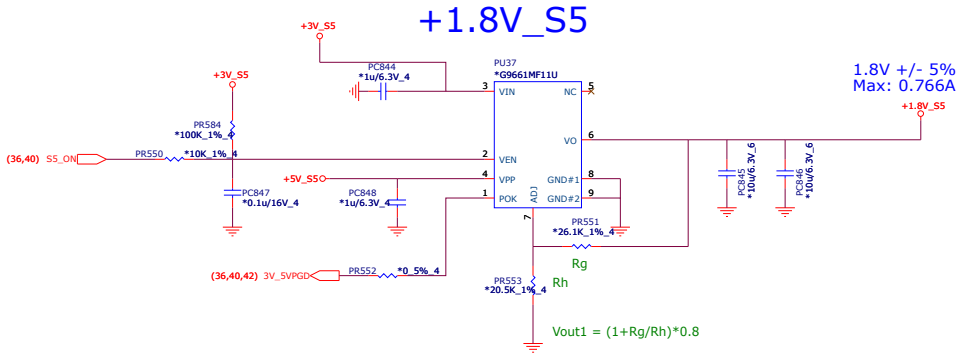
+1.05V_S5

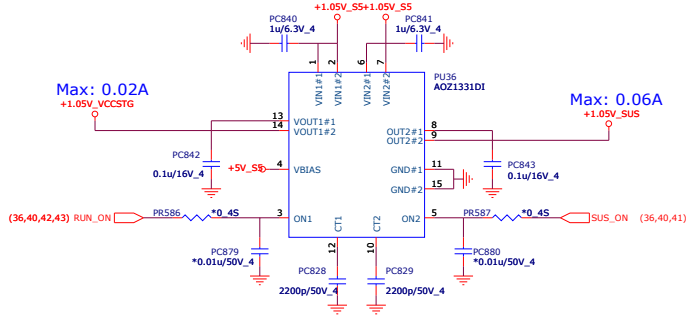


+1.5V



+1.8V_S5





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Size	Document Number	Rev
	+1.0V_S5 / +1.5V	1A
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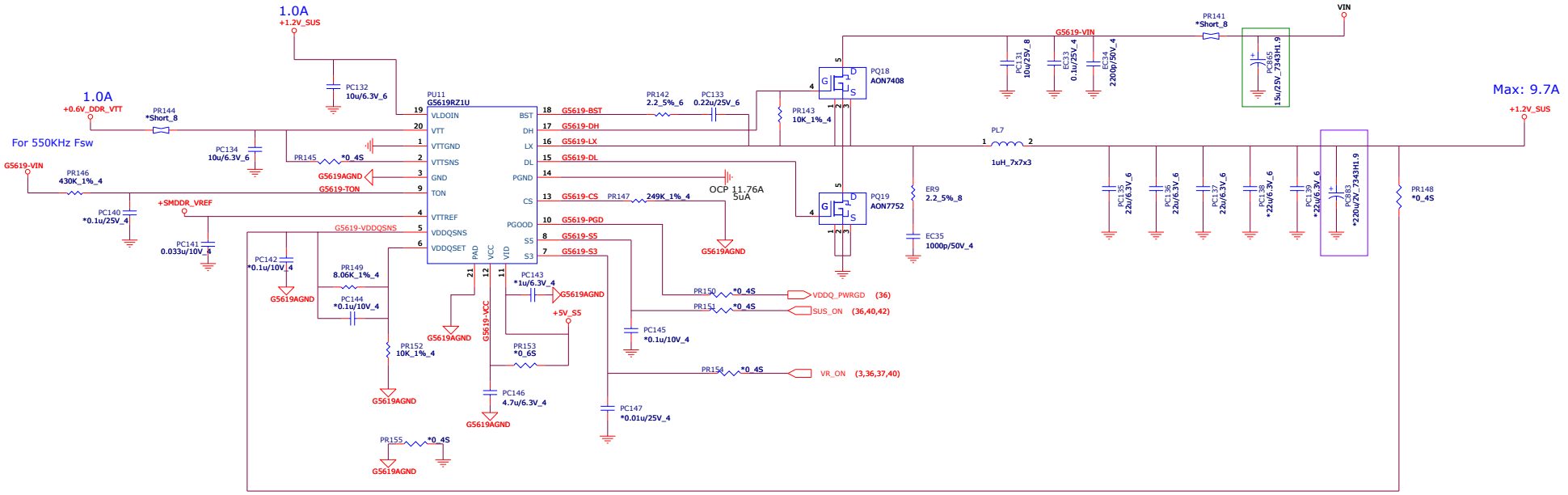
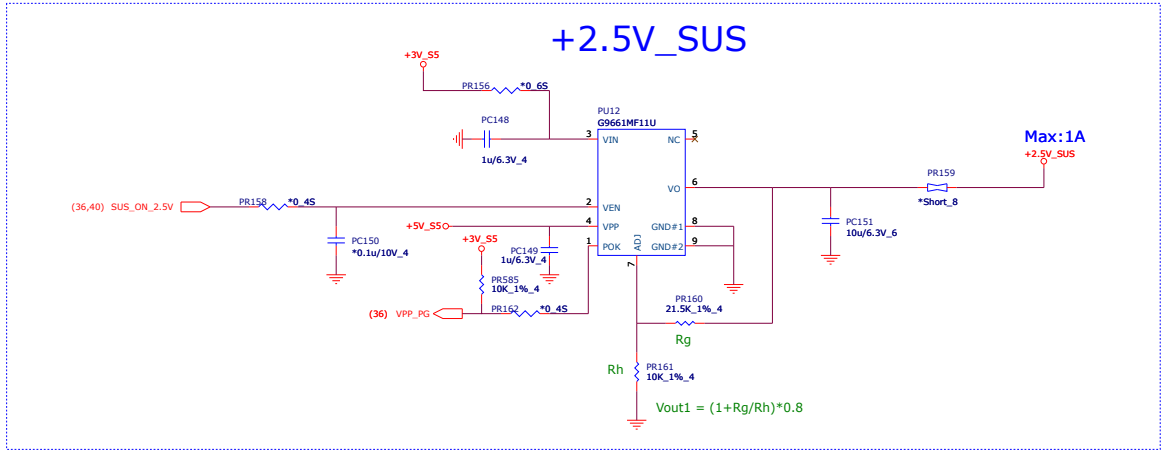
1.2VSUS & VTT_MEM



STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	00		Off	Off	Off

+2.5V_SUS



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	1.2VSUS/VTT_MEM	1A
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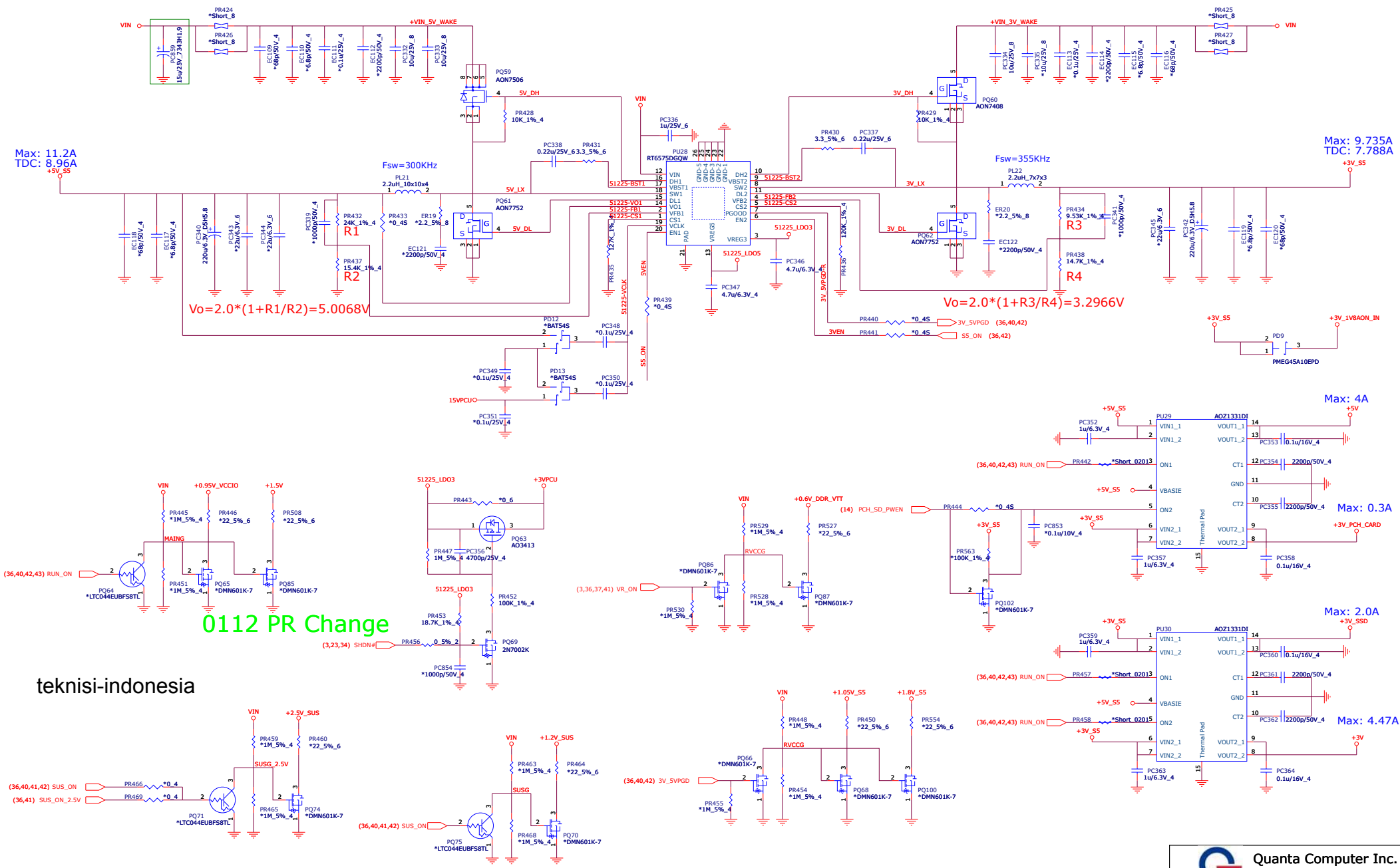

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PROJECT : BKLB & BKNB			
Size	Document Number		Rev
	1.2VSUS/VTT_MEM		1A
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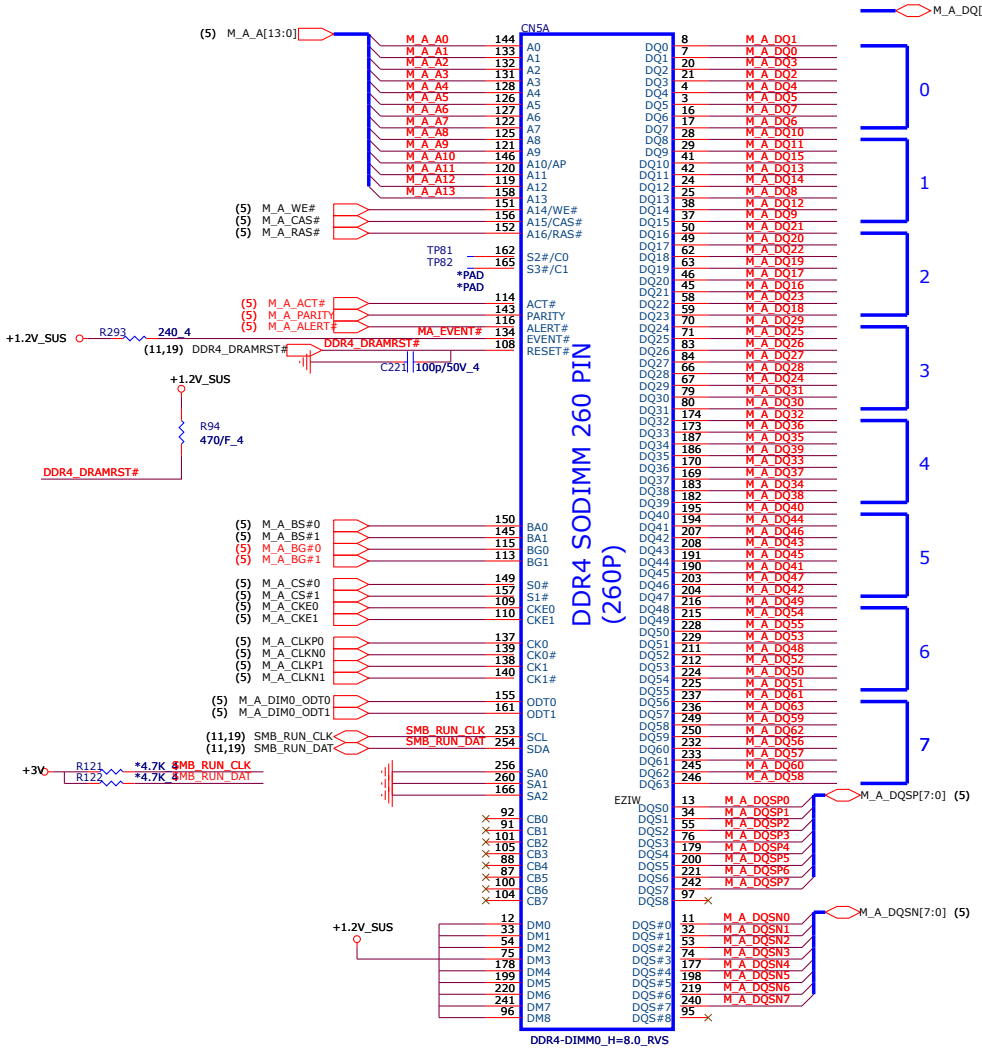
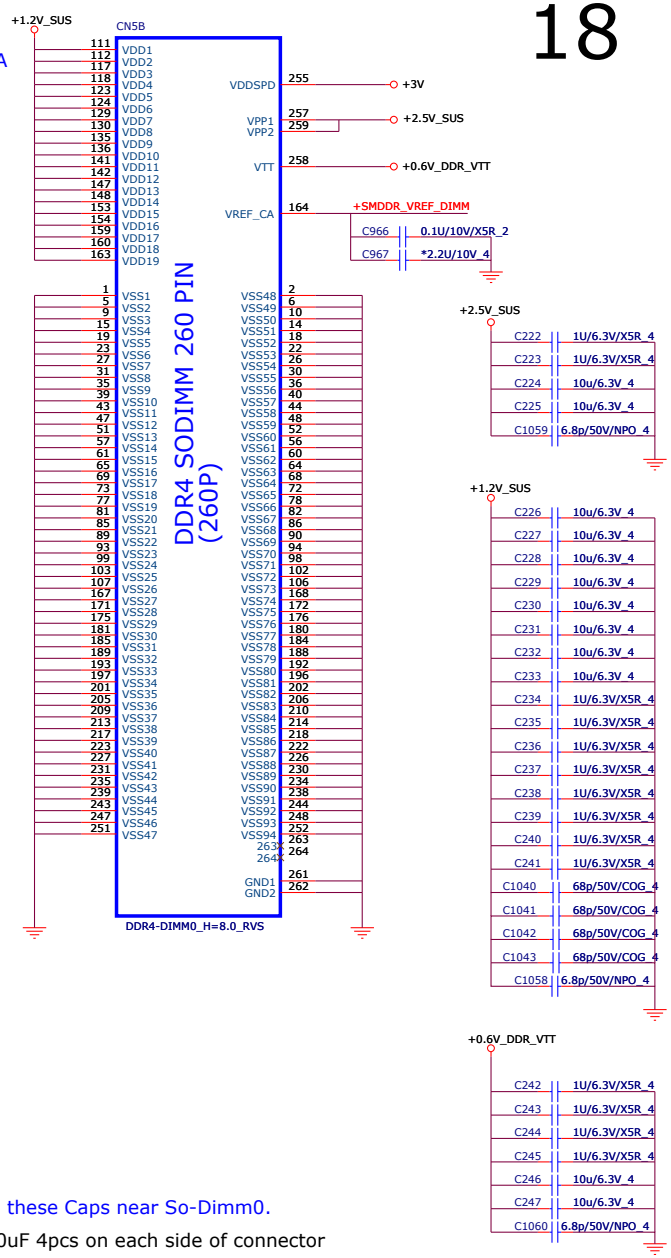
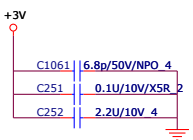
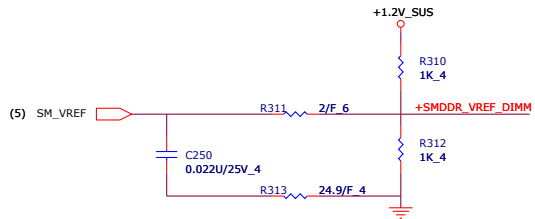




Place these Caps near So-Dimm0.





Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

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	DDR4 DIMM0-STD(4.0H)	1A

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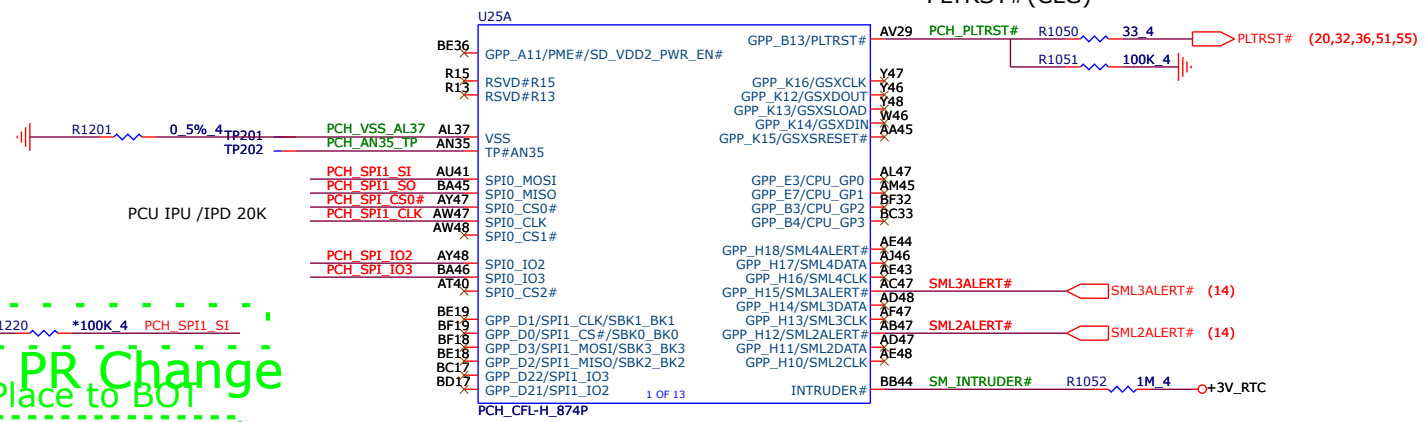
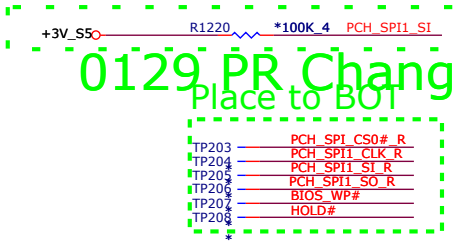
PLTRST#(CLG)

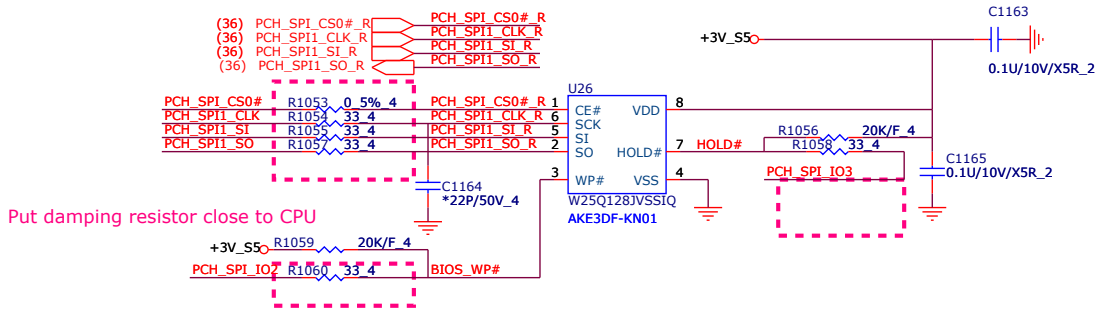


0129 PR Change

Place to BOT



PCH SPI ROM(CLG)



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Size	Document Number	Rev
	PCH 4/7 (GPIO/MISC)	1A

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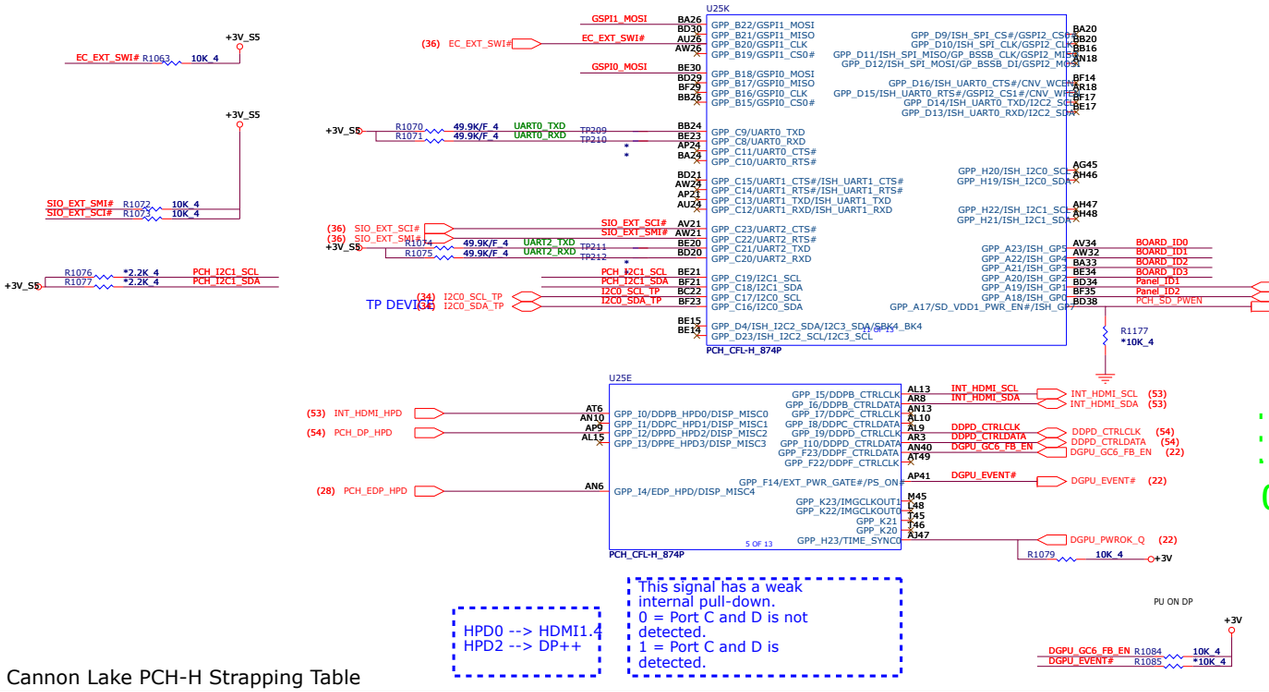


	Panel ID1	Panel ID2
FHD	11	
4K2K	1	0
HD	0	1

	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
GE15 1050TI ID1 ROG	00	0	0	
GE17 1050TI ID1 ROG	00	0	0	1
GD17 1050 ID1 ROG	0	0	10	
	0	0	11	
	1	0	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	11	

Cannon Lake PCH-H Strapping Table

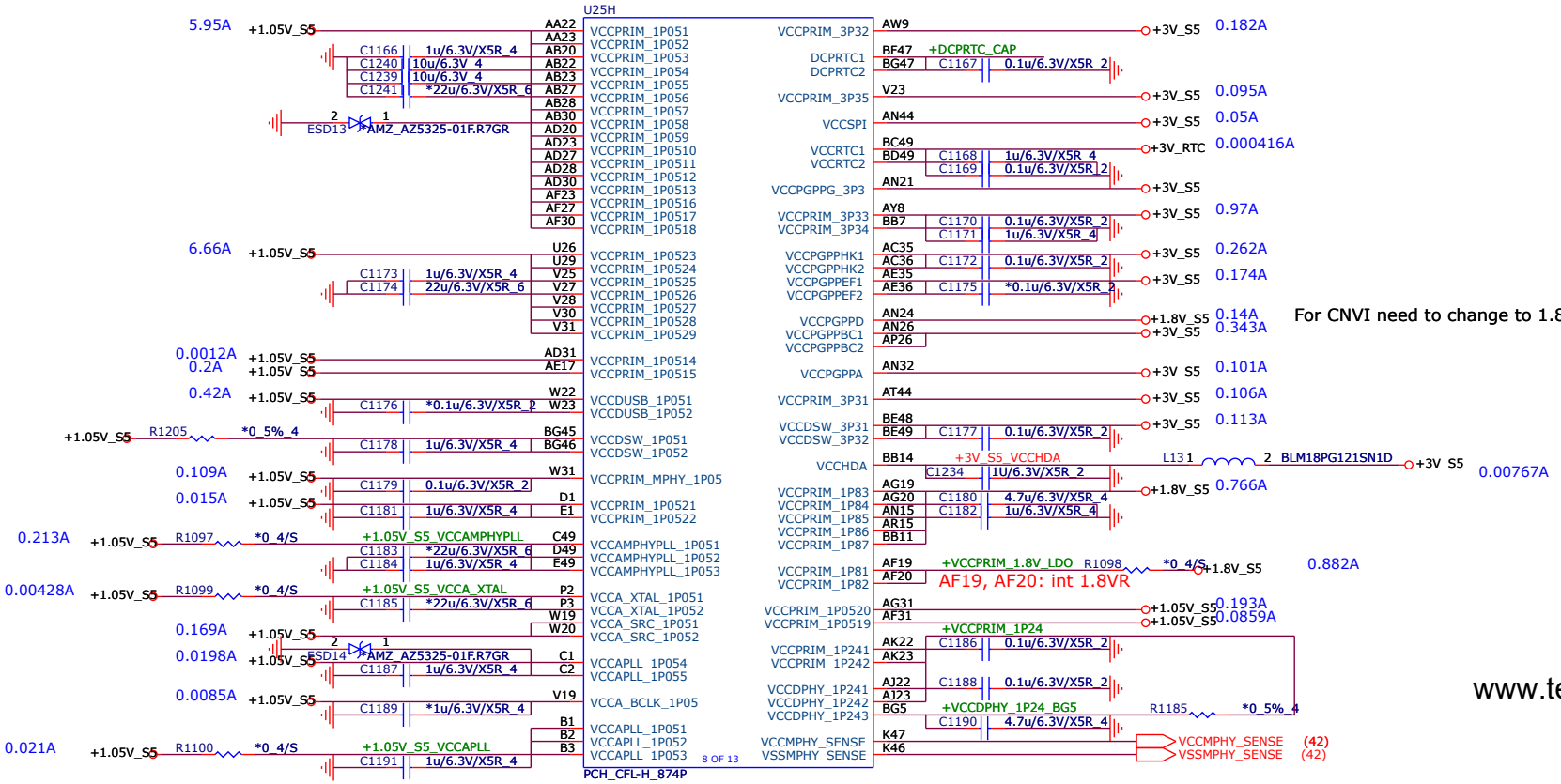
Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) Default 1 = Enable Top Swap Mode	+3V_S5 R1086 *1K_4 ACZ_SPKR (11)
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default 1 = Enable No Reboot Mode	+3V_S5 R1087 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) Default 1 = Enable Intel ME Cryp to TLS PU to support AMT TLS	+3V_S5 R1088 *1K_4 SMBALERT# (11)
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	0 = *SPI (iPD 20K) Default 1 = LPC	+3V_S5 R1089 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) Default 1 = eSPI selected for EC	TP213 SML0ALERT# (11)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP214 SML3ALERT# (13)
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP215 SML1ALERT# (11)
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSMRST#	0 = *Master Attached Flash Sharing (MAFS) enabled (iPD 20K)Default 1 = Slave Attached Flash Sharing (SAFS) enabled.	TP216 SML2ALERT# (13)
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) (Default) 1 =Port B is detected	INT_HDMI_SCL R1090 2.2K_4 +3V INT_HDMI_SDA R1091 2.2K_4
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) (Default) 1 =Port C is detected	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	PCH_PWROK	0 = *Port D is not detected (iPD 20K) (Default) 1 =Port D is detected	DDPD_CTRLCLK R1094 2.2K_4 +3V DDPD_CTRLDATA R1095 2.2K_4
GPP_F23	Display Port F Detected	PCH_PWROK	0 = *Port F is not detected (iPD 20K) (Default) 1 =Port F is detected	CFL - H CPU Not Support DDI Port F
GPP_J4 CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	RSMRST#	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. 0 = *38.4MHz XTAL frequency selected. (iPD 20K) (Default) 1 = 24MHz XTAL frequency selected.	CNV_RBI_DT (16,32) +1.8V_S5 R1141 4.7K_4 R1142 *20K/F_4
GPP_J6 CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. (Default) 1 = Integrated CNVi disable.	CNV_RGI_DT (16,32) +1.8V_S5 R1143 20K/F_4 R1144 *20K/F_4
GPP_J9	1.8V VCCPSPI	RSMRST#	0 = *VCCSPI is connected to 3.3V rail. (iPD 20K) (Default) 1 = VCCSPI is connected to 1.8V rail	R1145 TP217 *10K_4 GPP_J9 (16)
GPD7	Reserved	DSW_PWROK	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	External pull-up is required. Recommend 100K. +3V_S5 R1196 10K_4 GPD7 (10) R1146 *10K_4

Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

PCH Strap: GPP_J4 = XTAL SELECT-1
HIGH -> 24 MHZ / LOW -> 38.4 MHZ

PCH Strap: GPP_J6 = M.2 CNVI STRAP
HIGH -> DISABLE / LOW -> ENABLE

Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os



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CHANNEL A: 2G/4G GDDR5

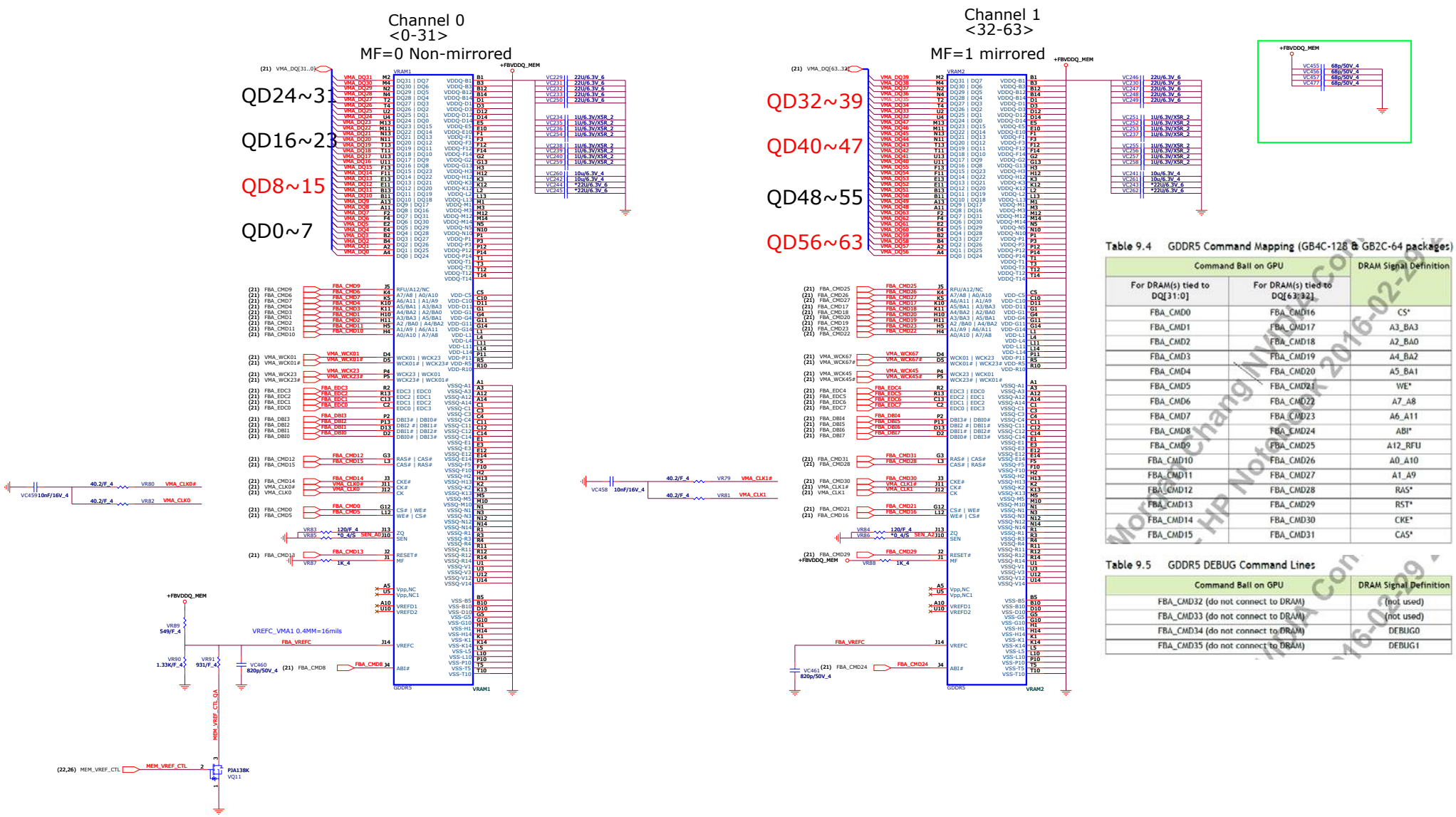


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

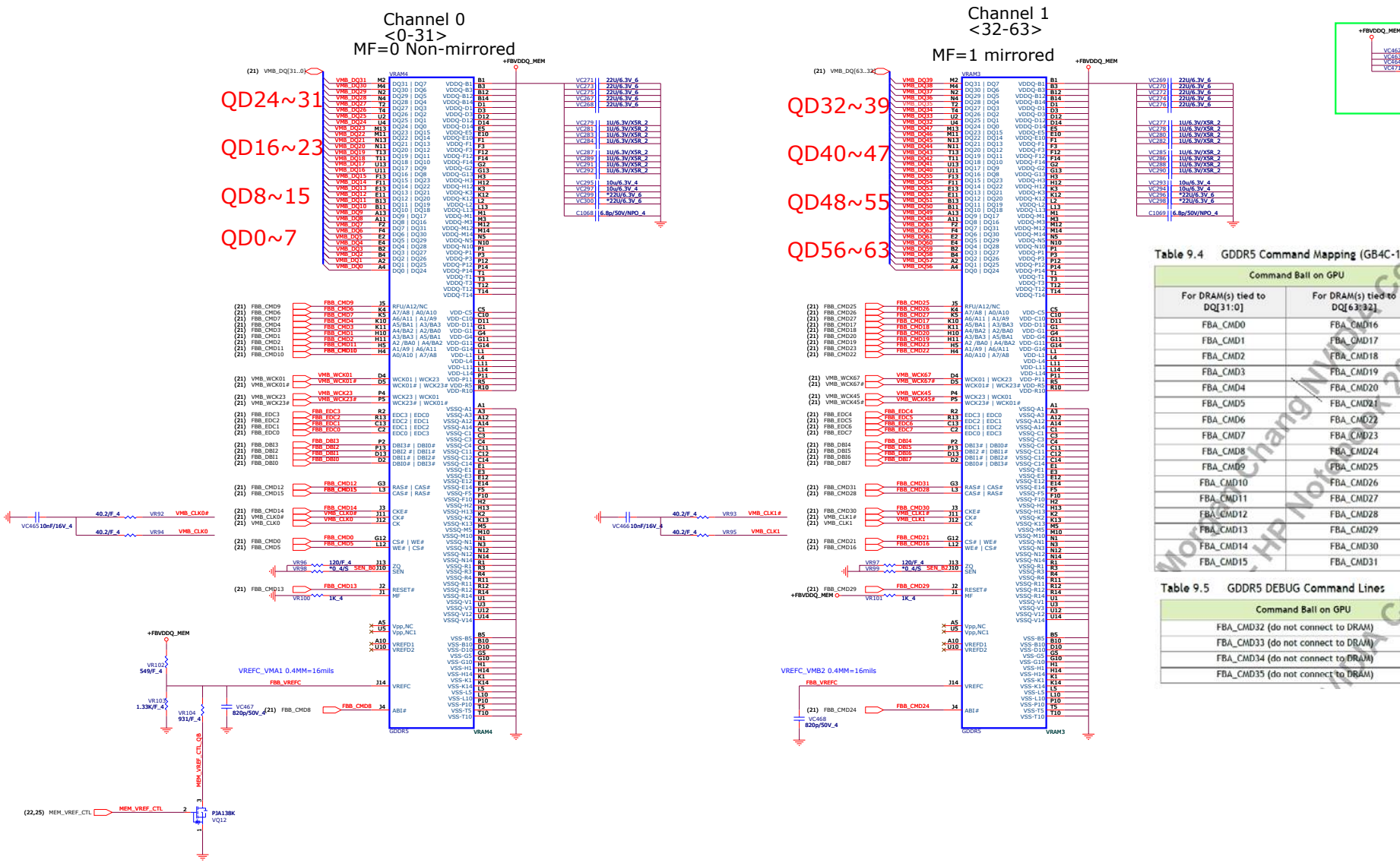


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

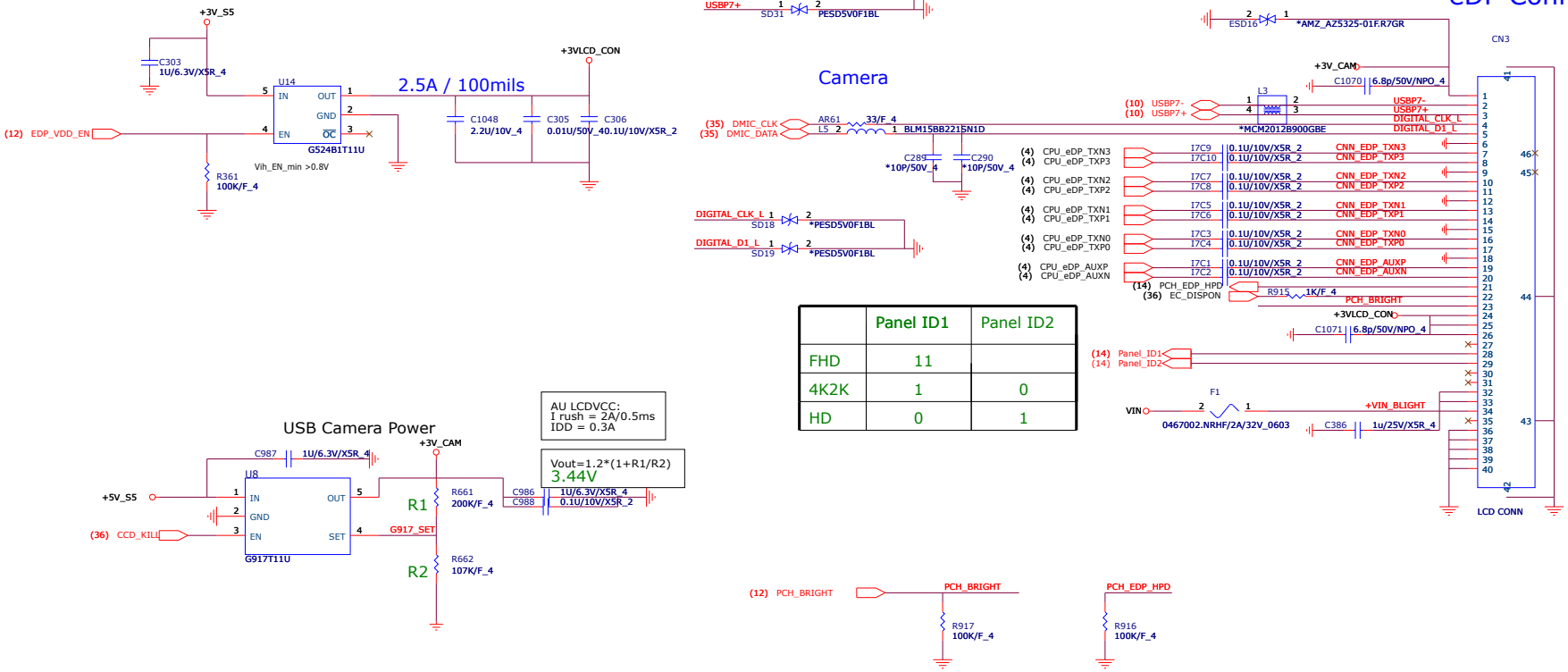
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

eDP & Camera

eDP Conn.



	Panel ID1	Panel ID2
FHD	11	
4K2K	1	0
HD	0	1

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	eDP CONN/CAM/D-MIC	1A

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Size C	Document Number NA	Rev 1A
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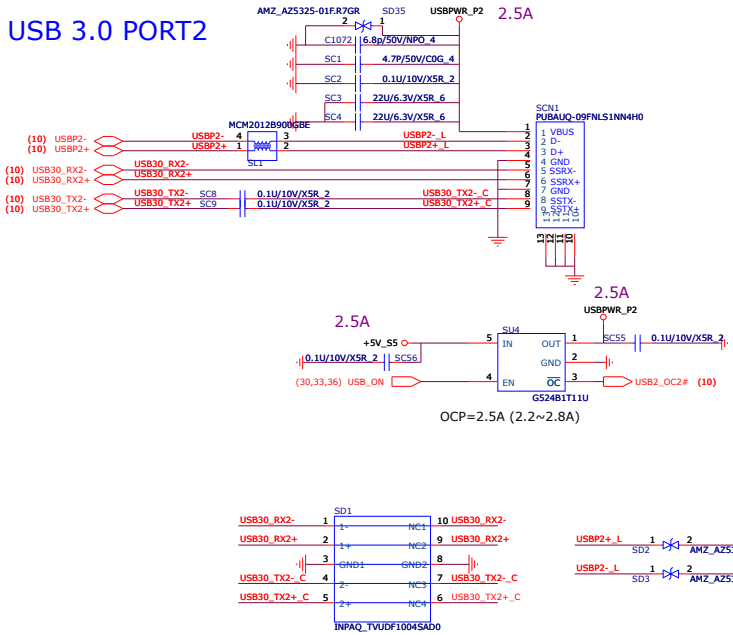
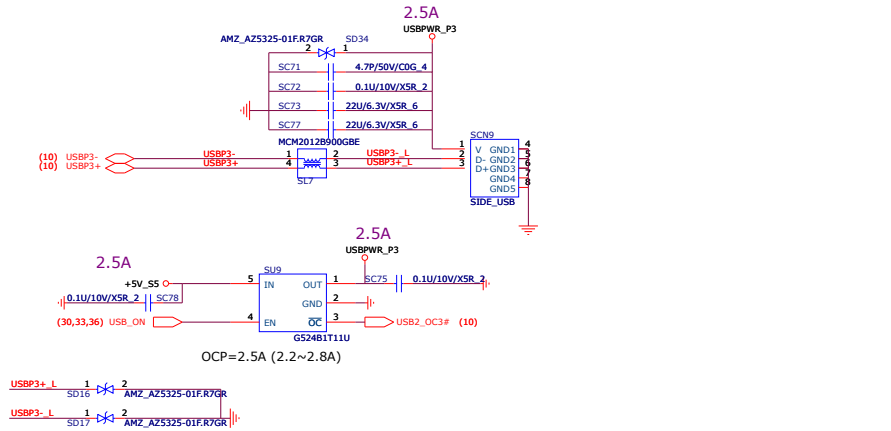
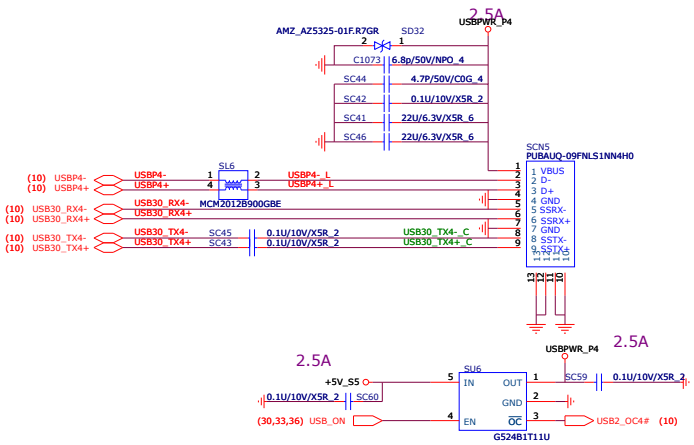
USB 3.0 PORT2



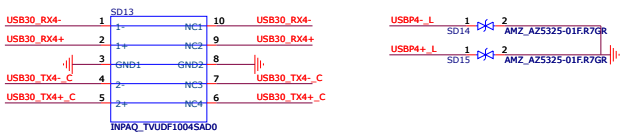
USB 2.0 PORT3



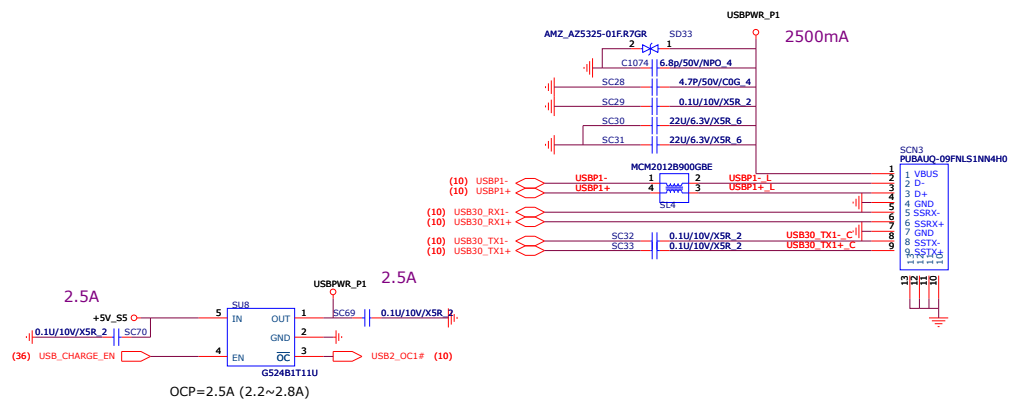
USB 3.0 PORT4



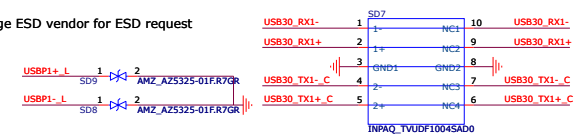
Change ESD vendor for ESD request



USB 3.0 PORT1



Change ESD vendor for ESD request



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	USB3.0	1A

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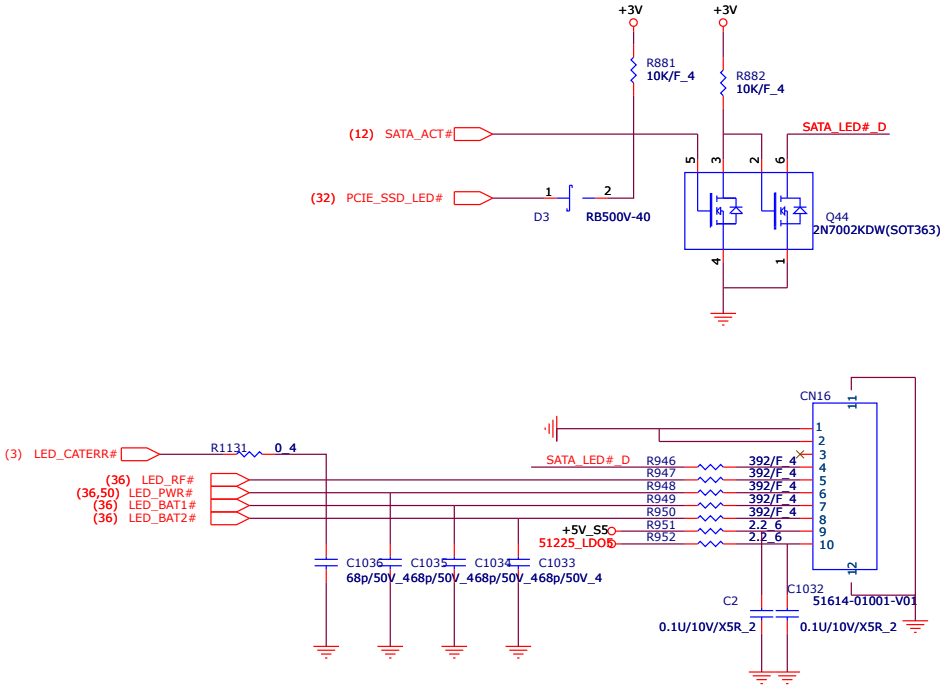
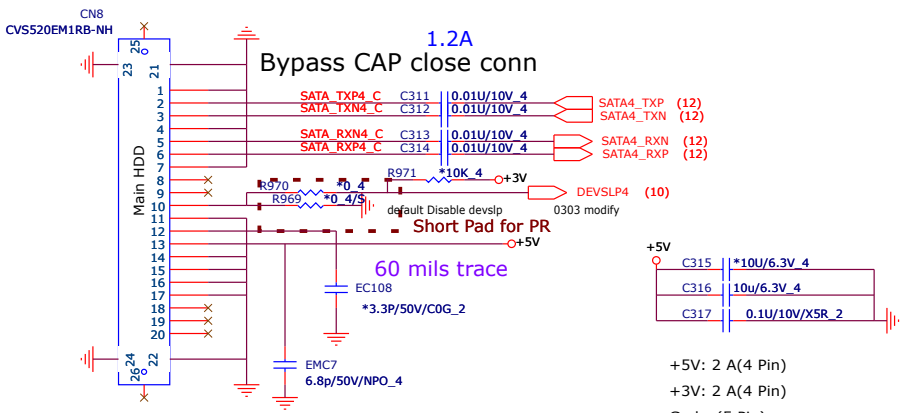
LED



SATA HDD Connector(Cable type)



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	HDD/LED	1A
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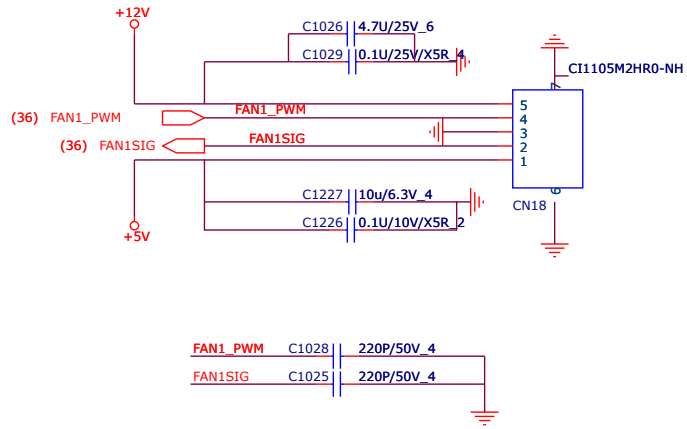
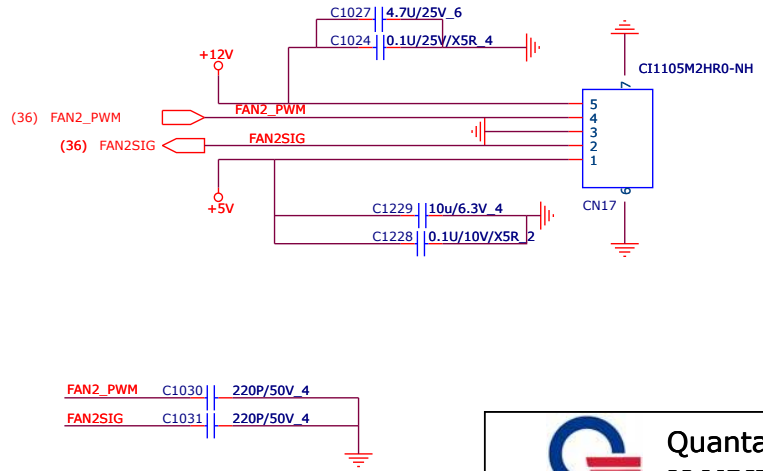
FAN1 for GPU



FAN2 for CPU



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	FAN	1A
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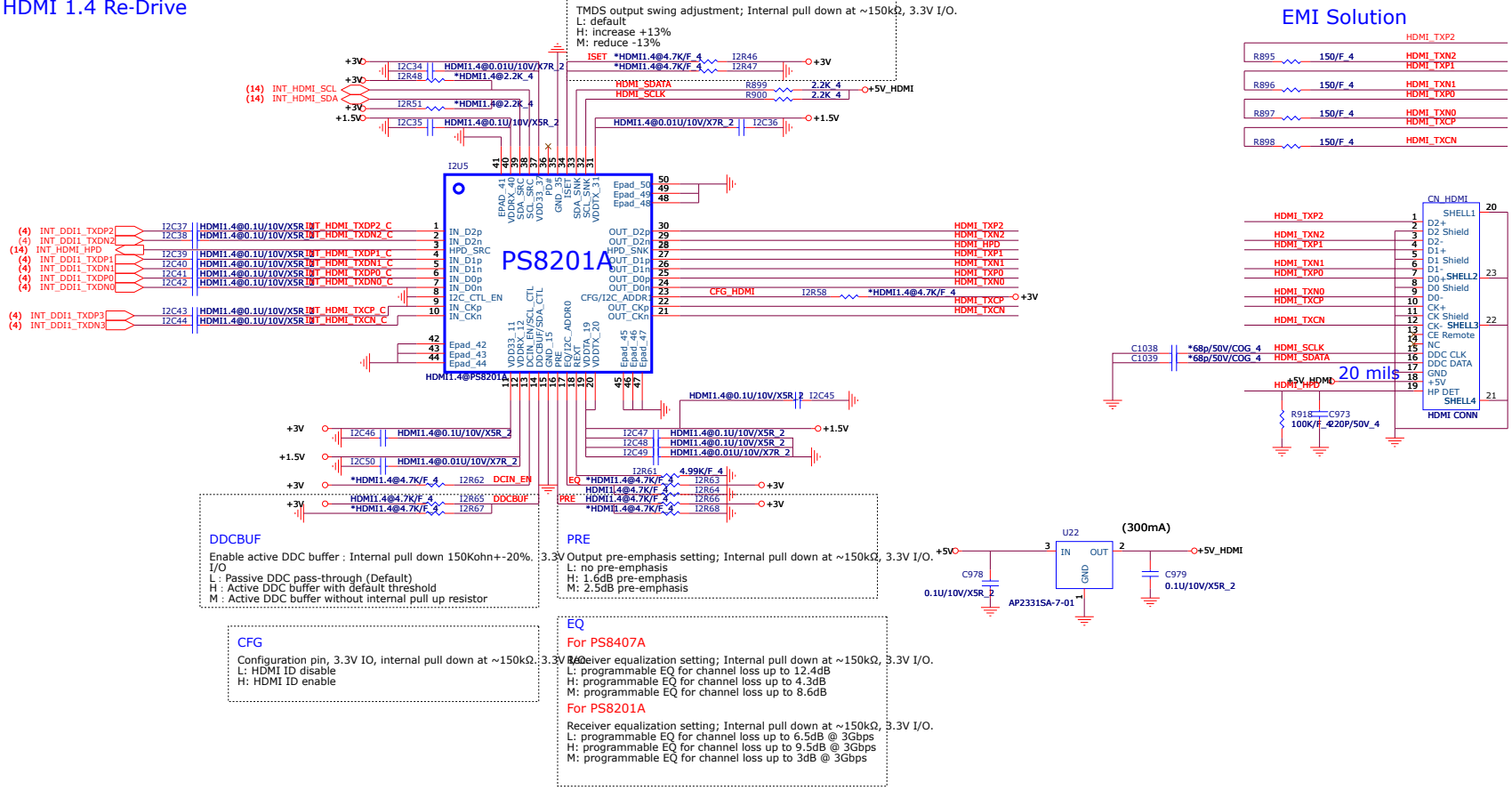
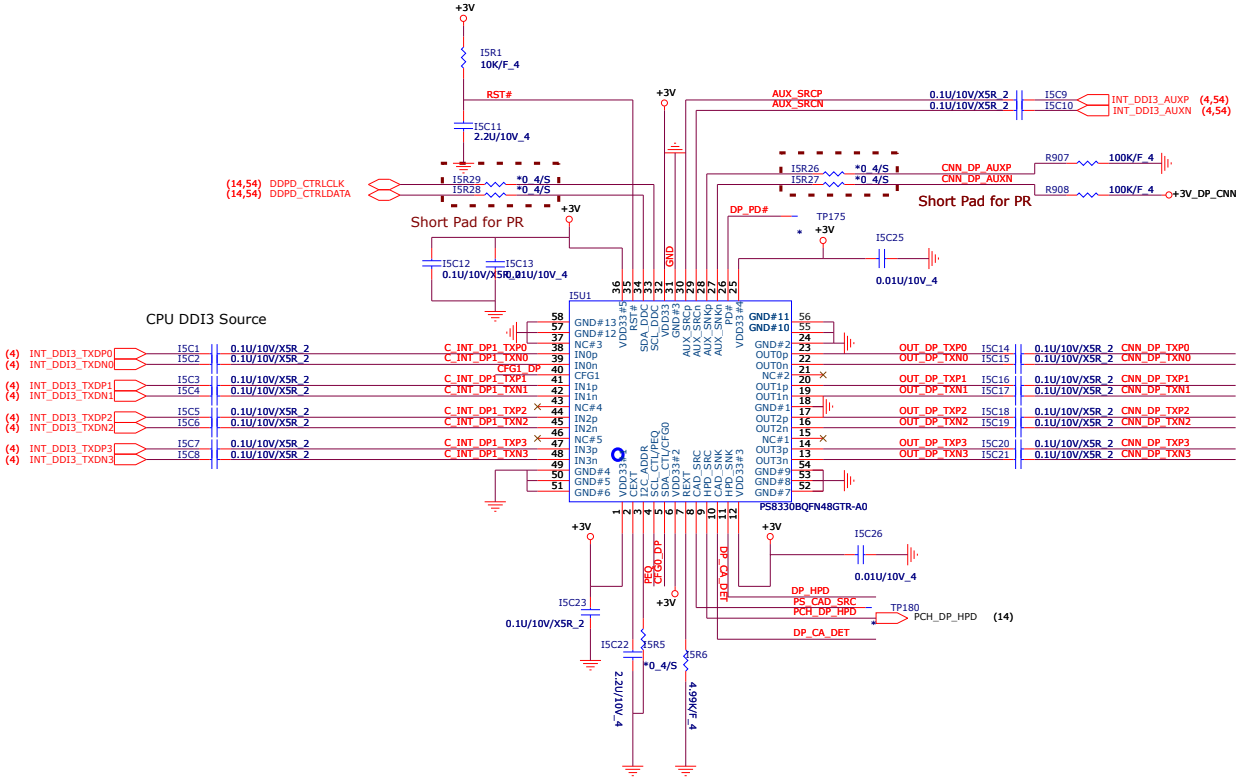
HDMI 1.4 Re-Drive

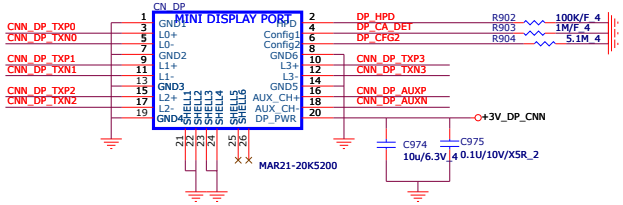


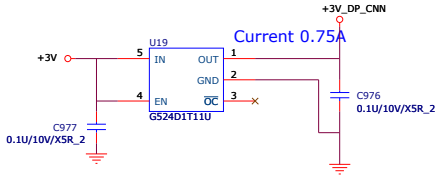
EMI Solution

Dual-Mode DisplayPort (DP++)

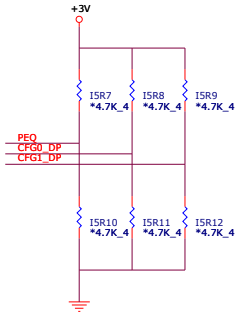


Mini-DP





PS8330 strap pin



PEQ
Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

CFG0_DP
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

CFG1_DP
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

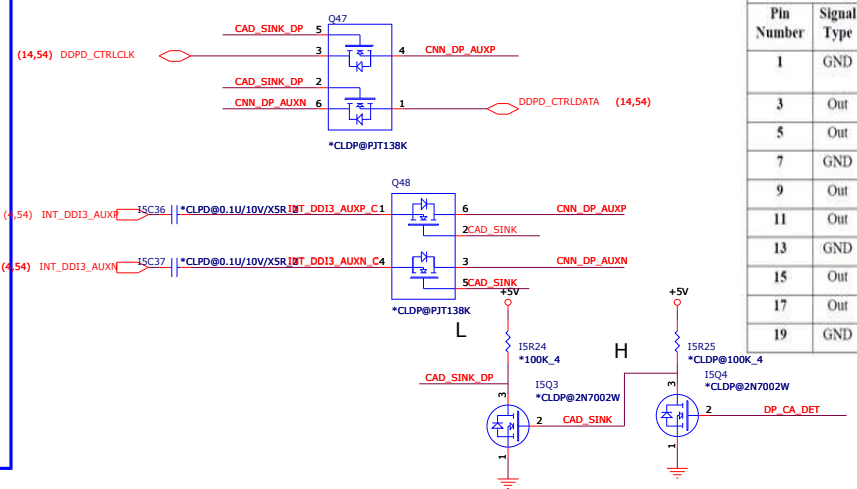


Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

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	Mini-DP/Re-driver	1A
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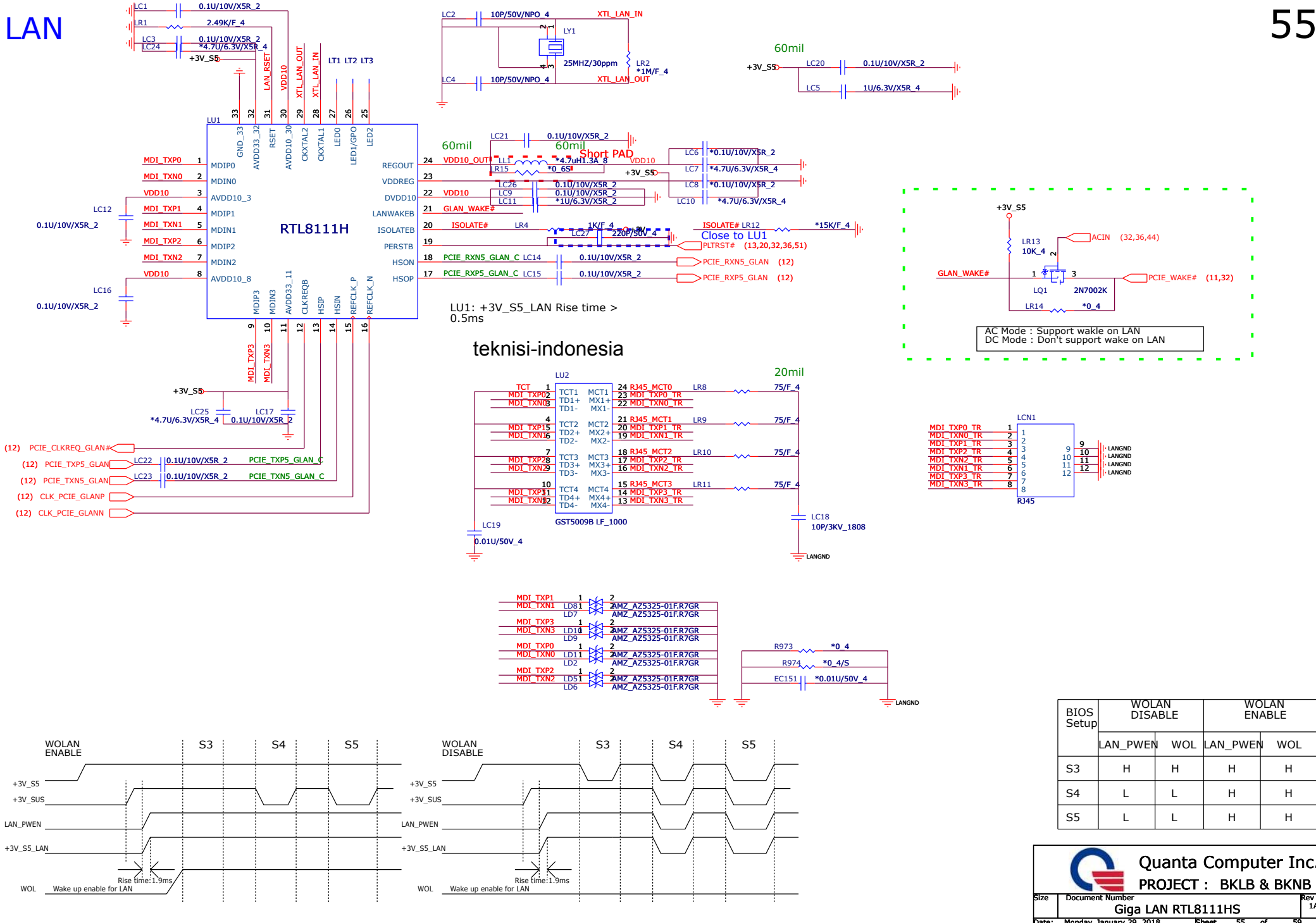
LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

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	Giga LAN RTL8111HS	1A
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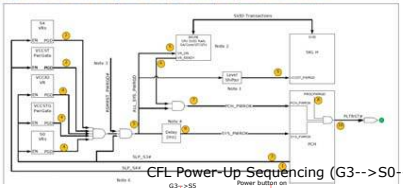
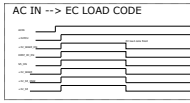
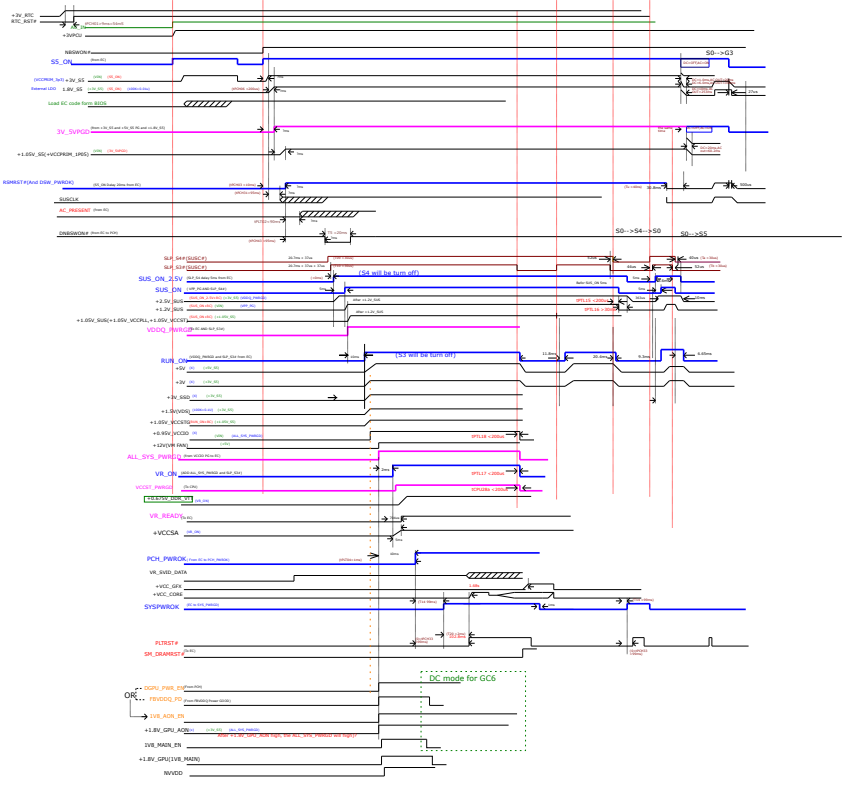
Figure 45-1. CFL Flow Diagram for SYS_PWROK/PCH_PWROK Generation





CFL Power-Up Sequencing (G3-->S0+->S3-->S4-->S5)



OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")	
RUN_ON	HL			L	L	L	L	
+3V	HL			L	L	L	L	
+5V	HL			L	L	L	L	
+0.675V_DDR_VTT	HL			L	L	L	L	
+12V	HL			L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	HL			L	L	L	L	
+1.05V_VCCSTG	HL			L	L	L	L	
+VCCSA	HL			L	L	L	L	
+VCC_GFX	HL			L	L	L	L	
+VCC_CORE	HL			L	L	L	L	
+0.95V_VCCIO	HL			L	L	L	L	
SUS_ON	HH			L	LL	L		
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	HH			L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	HL	H		H	L		L	
+1.8V_S5	H	H		HL	L		L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	HH	H		H	L		L	

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	POWER MAP	1A

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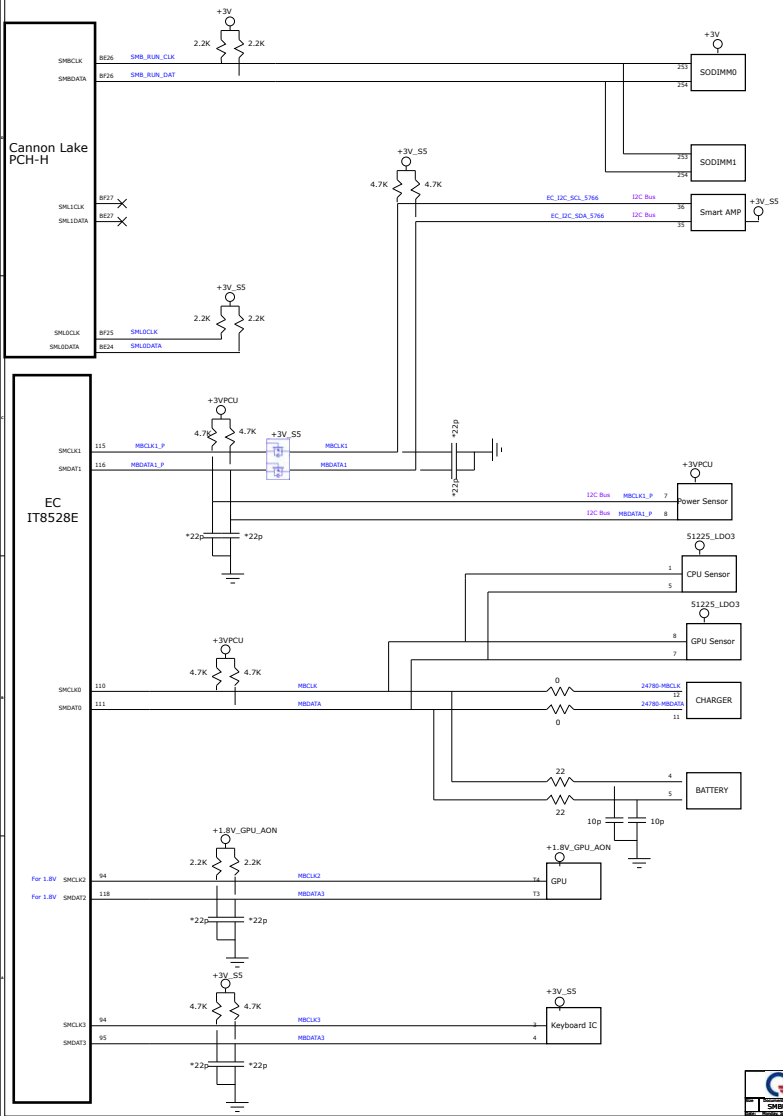
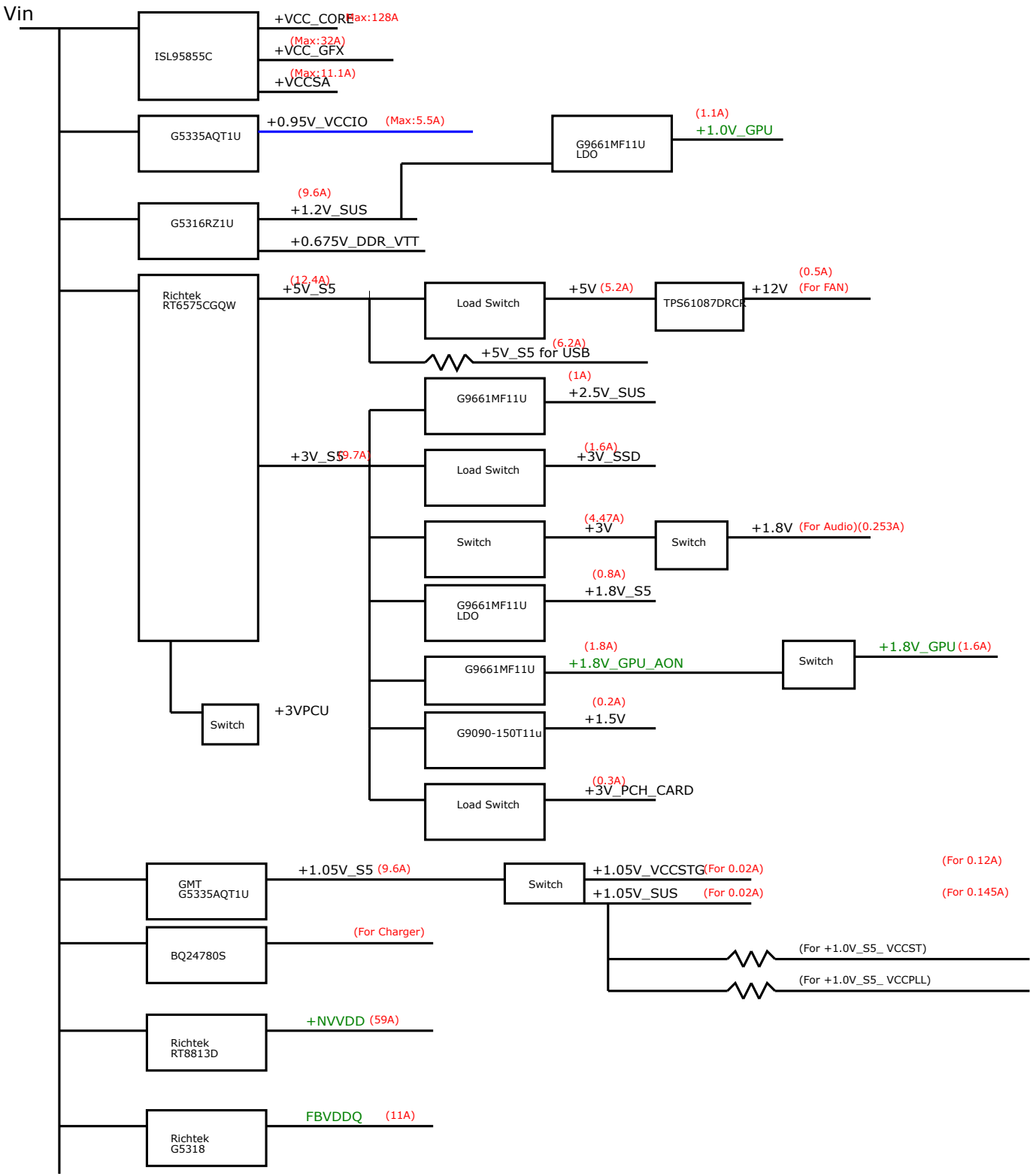

Cannon Lake
PCH-H
SMBCLK
SMBDATA
BE26
SMB_RUN_CLK
BF26
SMB_RUN_DAT
SML1CLK
SML1DATA
BF27
BE27
SML0CLK
SML0DATA
BF25
SML0CLK
BE24
SML0DATA
+3V
2.2K
2.2K
+3V_S5
4.7K
4.7K
SODIMM0
SODIMM1
253
254
257
254
Smart AMP
EC_I2C_SCL_5766
EC_I2C_SDA_5766
I2C Bus
36
35
EC
IT8528E
+3VPCU
SMCLK1
SMDAT1
115
MBCLK1_P
116
MBDATA1_P
MBCLK1
MBDATA1
*22p
Power Sensor
7
8
51225_LDO3
CPU Sensor
1
5
GPU Sensor
9
7
SMCLK0
SMDAT0
110
111
MBCLK
MBDATA
0
24780-MBCLK
24780-MBDATA
12
11
CHARGER
22
4
5
BATTERY
10p
+1.8V_GPU_AON
For 1.8V
SMCLK2
SMDAT2
94
118
MBCLK2
MBDATA3
T4
T3
GPU
SMCLK3
SMDAT3
95
MBCLK3
3
4
Keyboard IC



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	Power Diagram	1A
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