Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

BOM DISTRIBUTION RULE
Frodo, SamWise
(BOM,BOM)

DO NOT DISTRIBUTE

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

	Frodo	Samwise
PCH	Q87	Q85

PCB AND SILKSCREEN COLOR

Program Phase	Color of PCB	Silkscreen
EVT1	RED	YELLOW
EVT2	RED	WHITE
DVT1	LIGHT BLUE	YELLOW
DVT2+	LIGHT BLUE	WHITE
PVT1	GREEN	YELLOW
PVT2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE

PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

DELL INC.

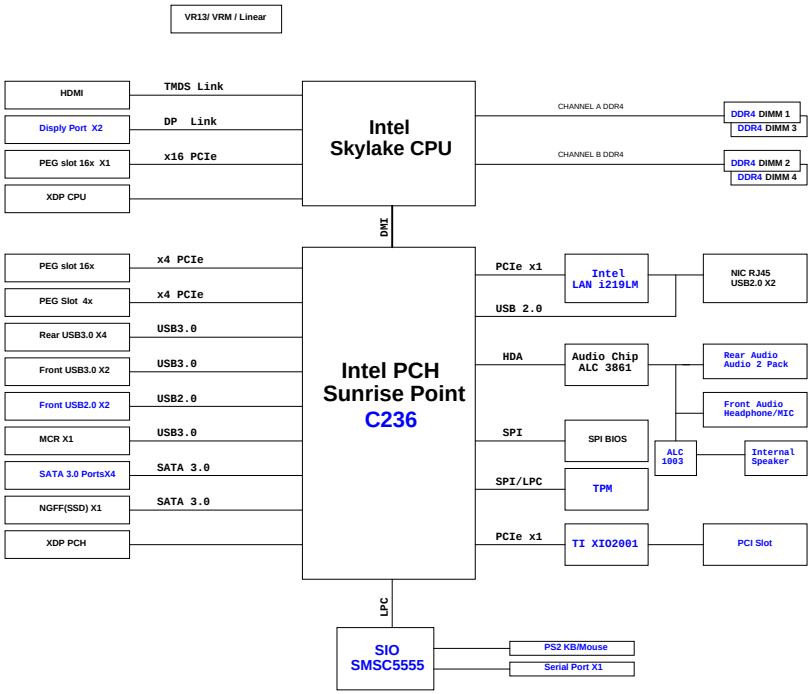
Title: **INDEX**

DWG NO: *GY SKL/ Farallon MT*

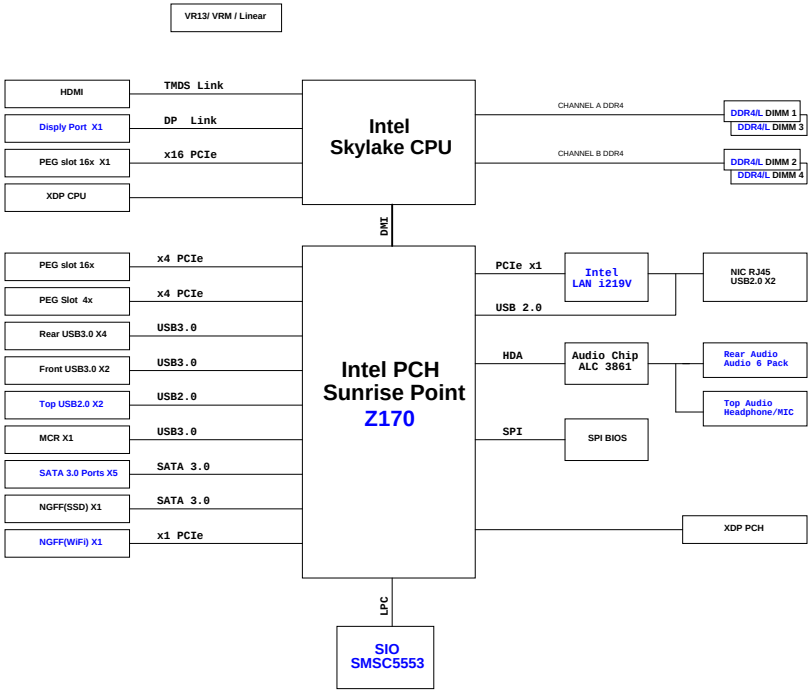
Rev: A00

Date: Tuesday, July 07, 2015 Sheet 1 of 71

Faralon MT



Goodyear SKL



DELL INC.

Title: BLOCK DIAGRAM

DWG NO: GY SKL/ Farallon MT

Rev: A00

Date: Tuesday, July 07, 2015

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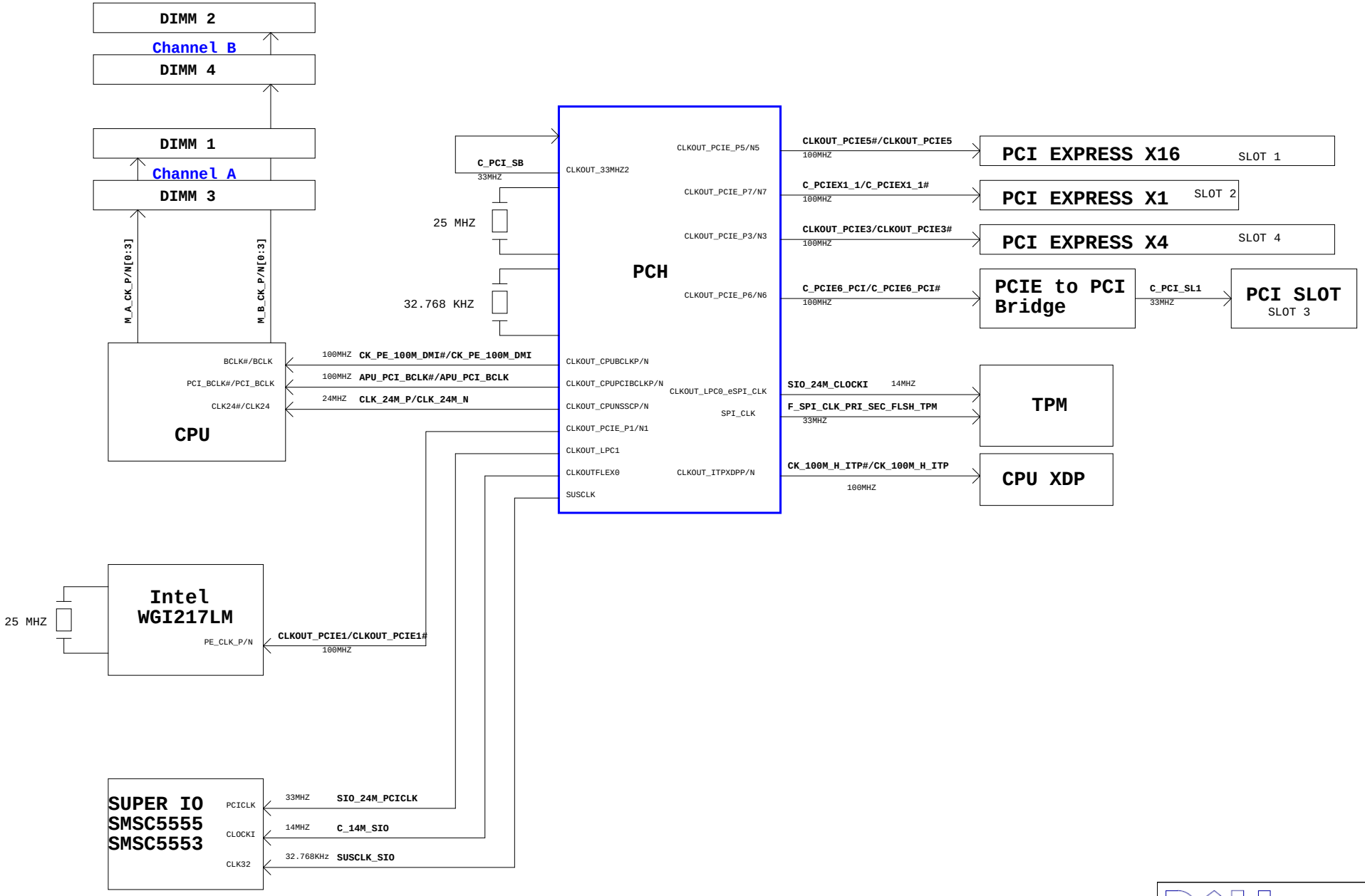


DELL INC.

Title

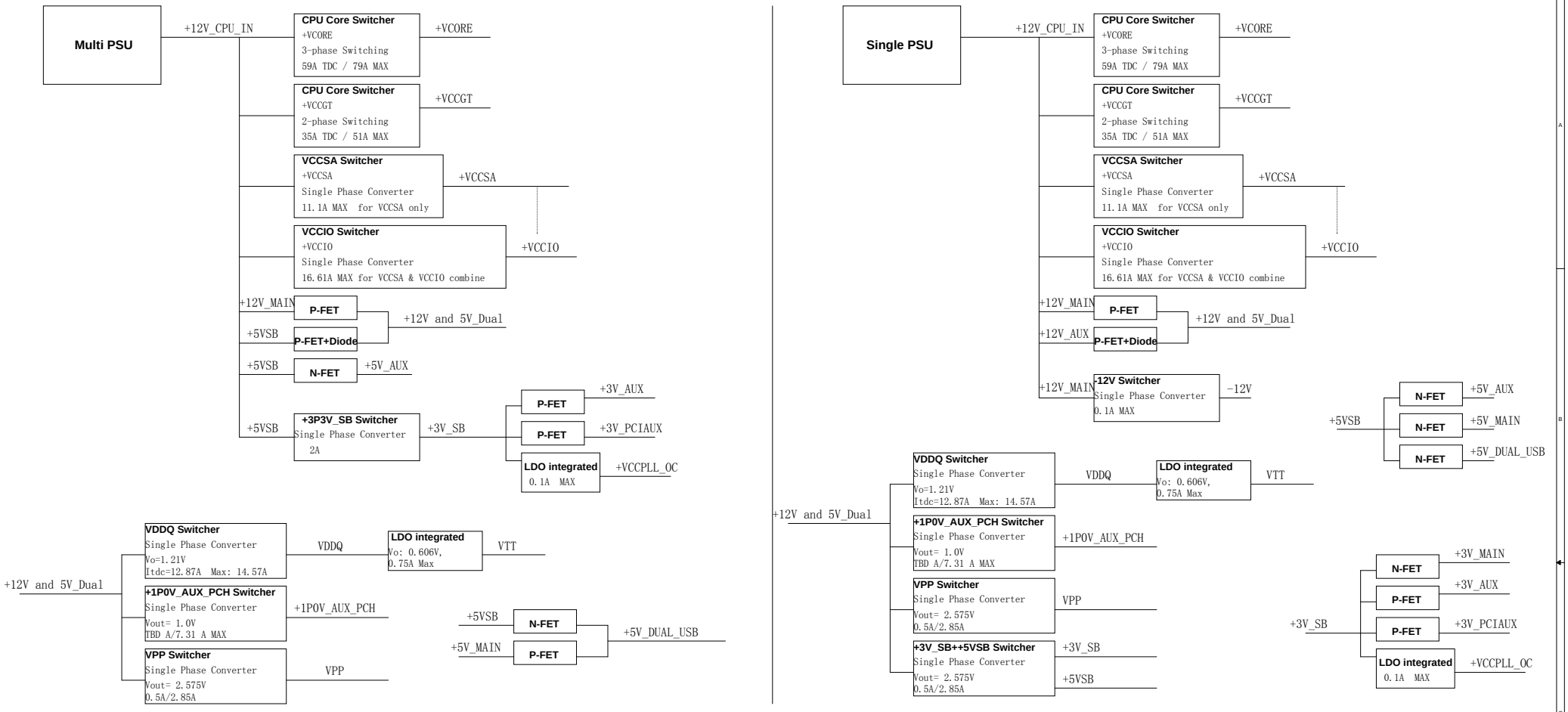
BLOCK DIAGRAM

DWG NO

GY SKL/ Farallon MT

Rev A00

Date: Tuesday, July 07, 2015 Sheet 3 of 71



DELL INC.

Title

POWER DISTRIBUTION

DWG NO

GY SKL/ Farallon MT

Rev **A00**

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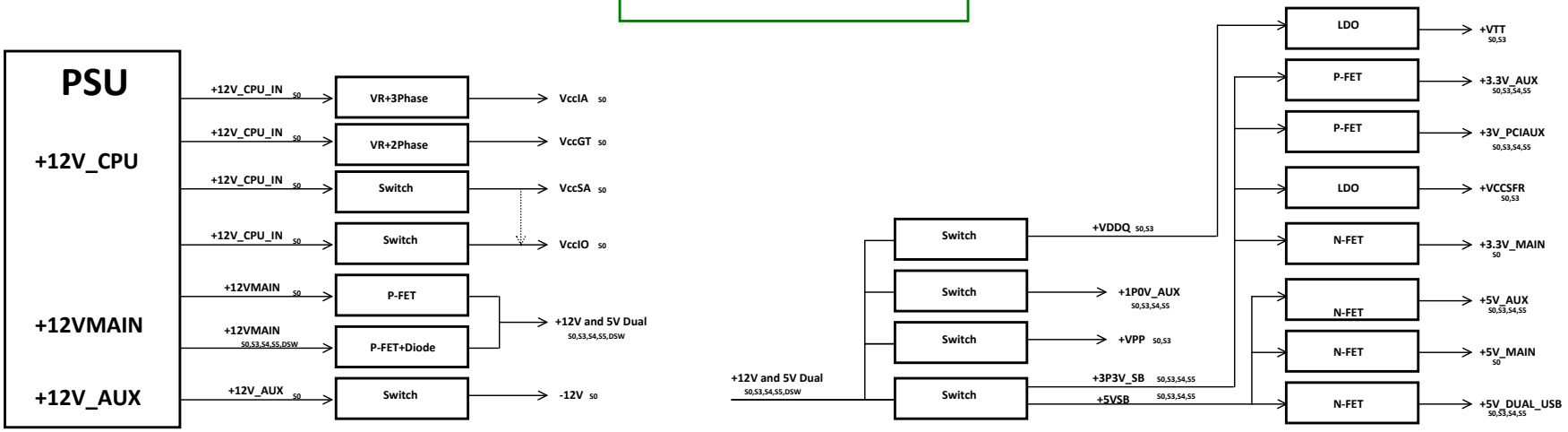
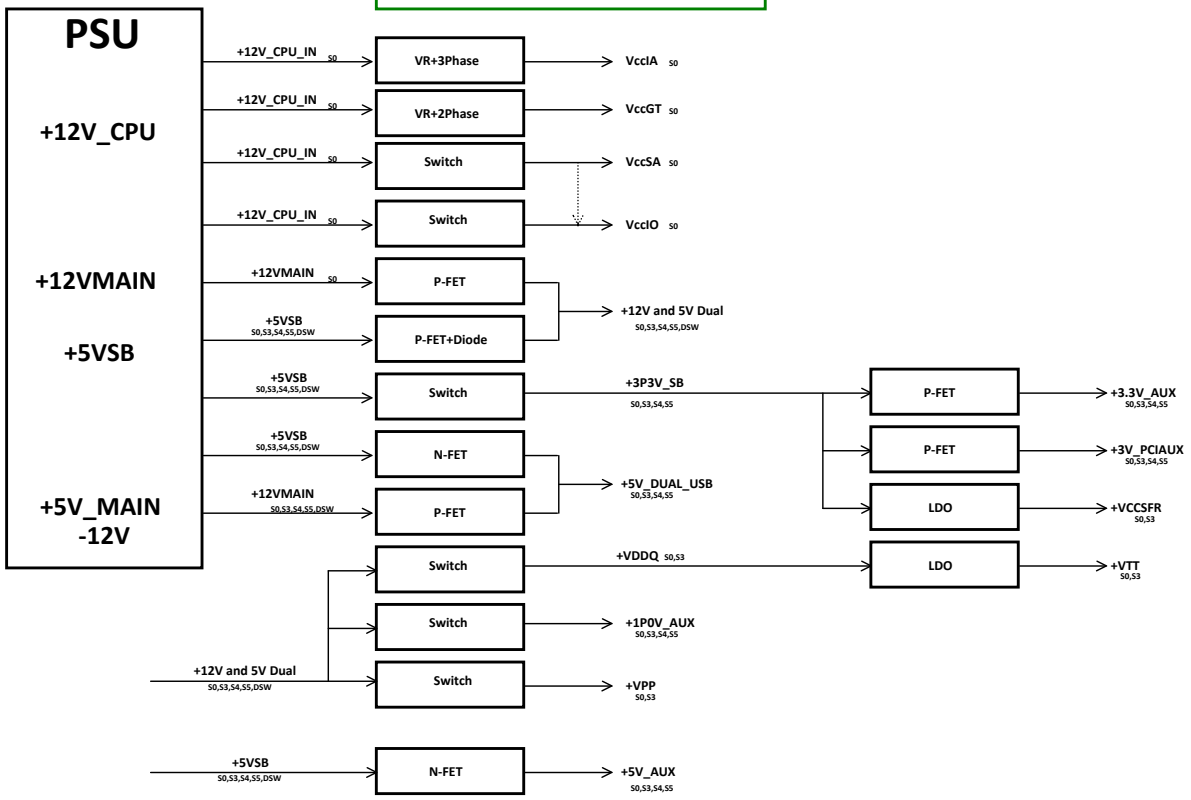
Faralon MT



Goodyear SKL



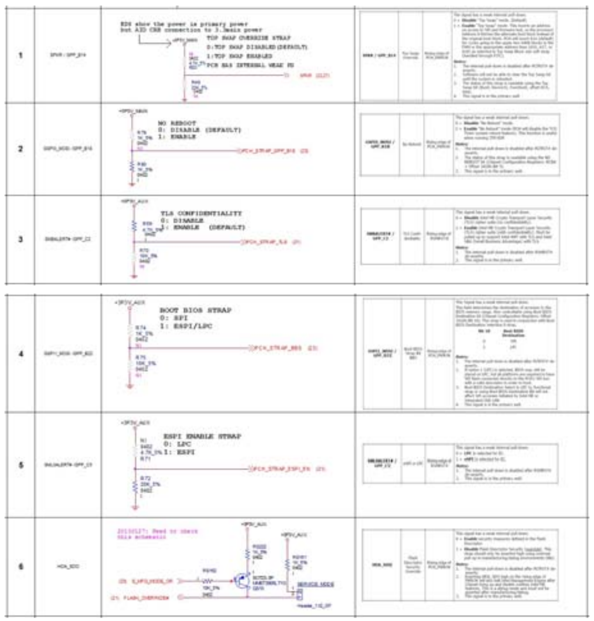
DELL INC.

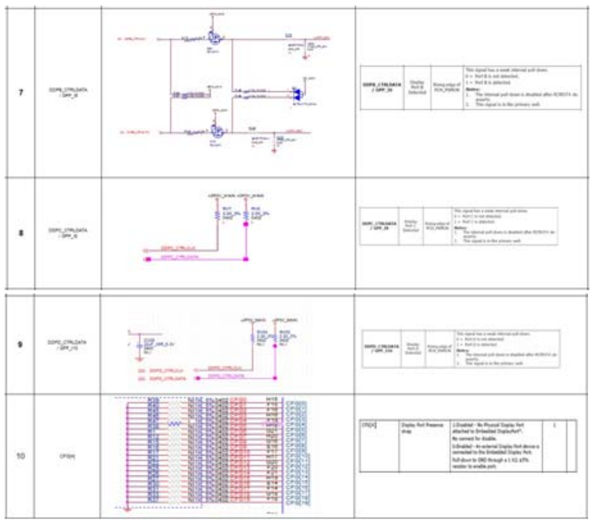
Power Flow

GY SKL/ Faralon MT

A00

1	SPKR / GPP_B14	EDS show the power is primary power but AIO CRB connection to 3.3main power TOP SWAP OVERRIDE STRAP 0:TOP SWAP DISABLED(DEFAULT) 1:TOP SWAP ENABLED PCH HAS INTERNAL WEAK PD	
2		NO REBOOT 0: DISABLE (DEFAULT) 1: ENABLE	
3		TLS CONFIDENTIALITY 0: DISABLE 1: ENABLE (DEFAULT)	
4		BOOT BIOS STRAP 0: SPI 1: ESPI/LPC	
5		ESPI ENABLE STRAP 0: LPC 1: ESPI	
6		SERVICE MODE	
7			
8			
9			
10			





DELL INC.

Title: **STRAP & GPIO**

DWG NO: *GY SKL/ Farallon MT* — Rev: A00

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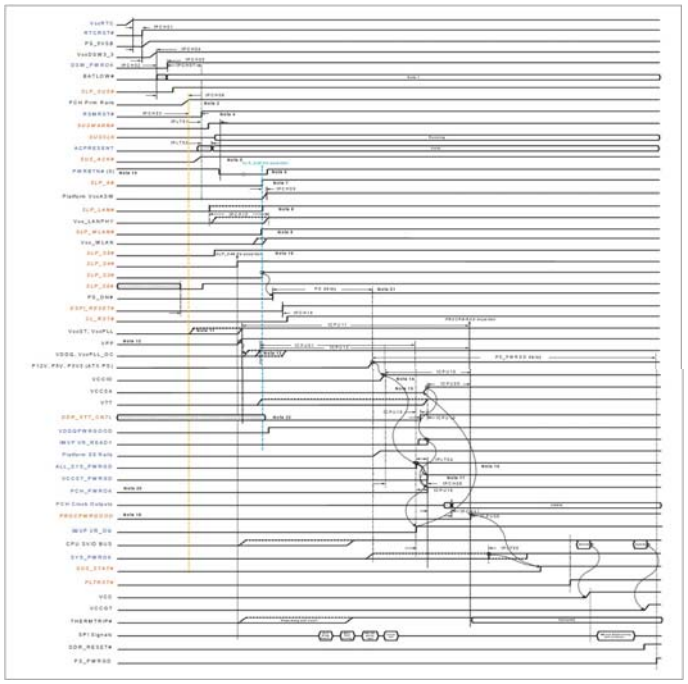
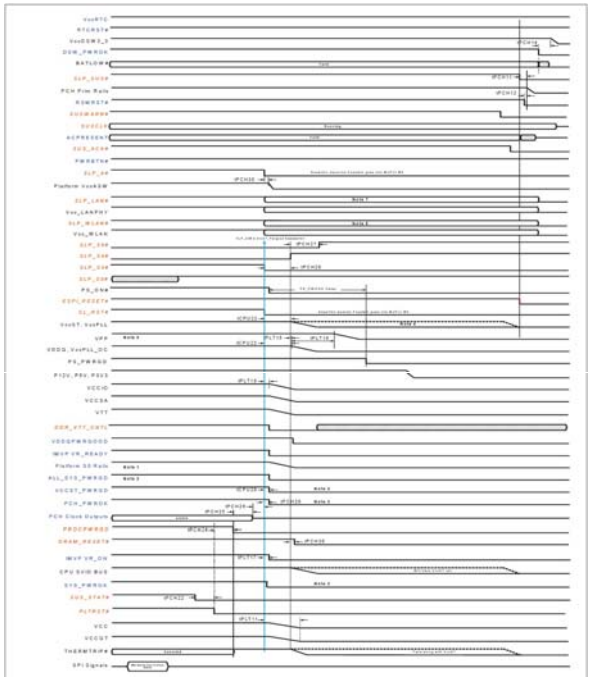
POWER SEQUENCE DIAGRAM

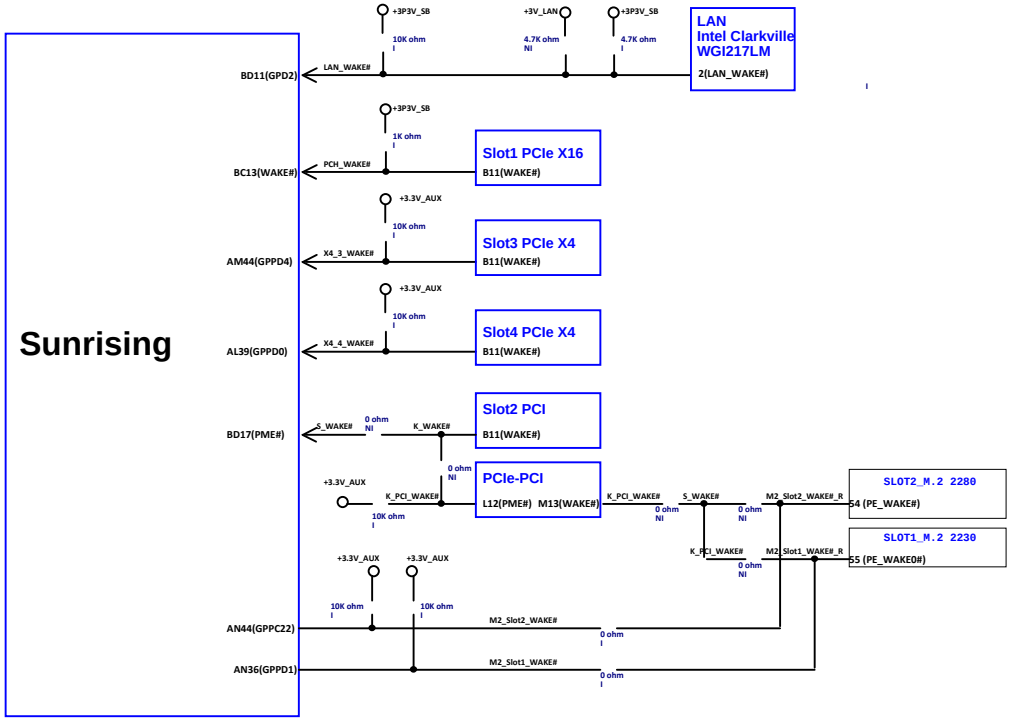
SKL-S Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



SKL-S Timing Diagram for S0/M0 to G3 [Deep Sx Platform]



DELL INC.		
TITLE	POWER SEQUENCE DIAGRAM	
DWG NO	GY SKL/ Farallon MT	REV A00
DATE	Tuesday, July 07, 2015	SHEET 1 of 1



DELL INC.

Title: INTERRUPT & PME DIAGRAM

DWG NO: GY SKI/ Farallon MT

Rev: A00

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20140520 Need check Debug port PDG, CRB 0.5 and PDG 0.7 is different

20140519 Follow CRB0.5 and PDG0.7

20140617 Follow CRB0.5

Need to check.

Intel MCP XDP Debug Connector

PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.

place R148,R149 clost to CPU

20140520 Follow CRB0.5 and PDG0.7

CRB is dummy R148, R149

PDG is Pop R148, R149

20140520 Follow CRB0.5 and PDG0.7

20140519 Follow CRB0.5 and PDG0.7

Note :
VCCST Power Gating (Q1) implemented : XDP_PRESENT# need connect to Q1.G with a inverse logic.

Place near CPU within 500mils

Place near CPU within 500mils

20140617 Follow CRB0.5

Title	SIO-SCH5555-1
DWG NO	GY SKL/ Farallon MT
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APU - VID,CTRL, MSIC

Need to check VR control power level. Level Shift?

20140516 SKL-S EDS0.75:It should be connected to VCCIO with pull-up resistor of xx

PEI-E CONFIG TABLE

CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

XU1E — Socket_LGA 1151_15u_Black — 5 OF 10

XU1_1

XU1_2

COOLER
COOLER

CL_LGA1151_FARALLON_MT

DELL INC.

Title: CLK/ CTRL/ MISC/DEBUG

DWG NO: GY SKL/ Farallon MT

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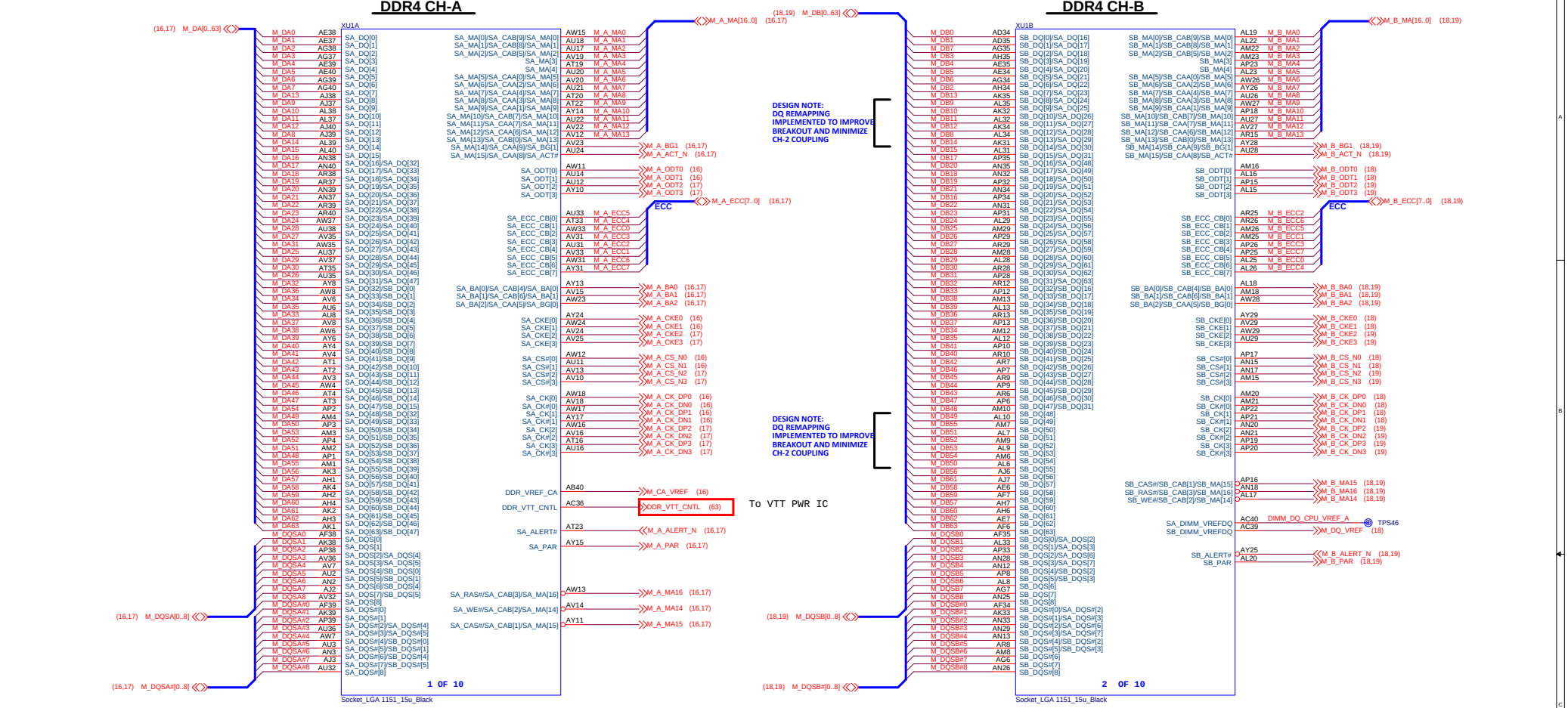
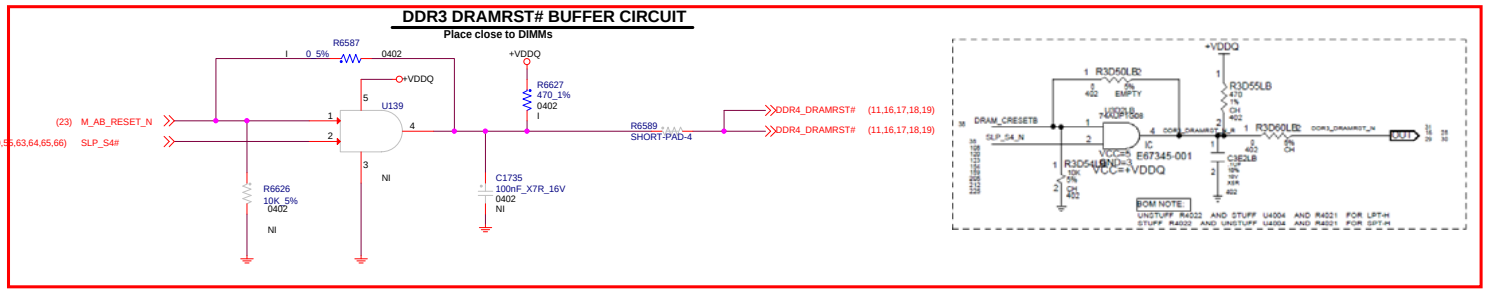




DELL INC.

Title: **DDR4 CHANEL A/B**

DWG NO: ***GY SKL/ Farallon MT***

Rev: **A00**

Date: Tuesday, July 07, 2015 Sheet 11 of 71

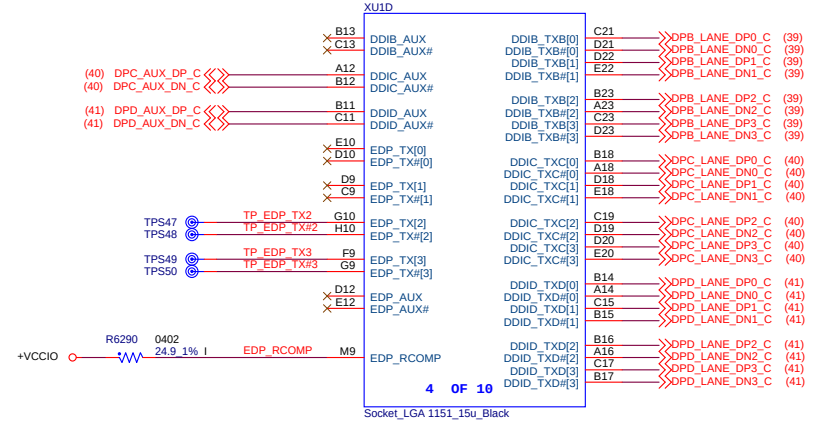
MCP - PCIE,DMI,FDI,DDI

PEG AC Cap Value	
Gen1/Gen2	75nf~265nf
Gen3	180nf~265nf

PEG x16 & DMI - Refer to PDG page45
Breakout
MS = 10/4/4/4/10
DSL = 10/3/3.5/3/10

Main
12/3.5/4.5/3.5/12 (Group)
15/3.5/4.5/3.5/15 (Other)

PEG_RCOMP:
Trace Width = 12 mils
Spacing = 15 mils
Length = 400mils



Processor PCI Express* Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9+-1%

2014-03-07-J

DELL INC.

Title: **PCIE/ DMI/ DDI**

DWG NO: ***GY SKL/ Farallon MT***

Rev: **A00**

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+VCCGT

Intel PDG 0.7: Request 11x47uF

XU1I

H36 AB34 AB33 AA37 AA36 AA35 G38 Y38 G37 Y36 AA38 Y34 Y33 W38 W37 W35 AA34 V40 W36 W34 V36 V38 V34 V33 U40 U39 U38 U37 U36 U35

VCCGT[0] VCCGT[1] VCCGT[2] VCCGT[3] VCCGT[4] VCCGT[5] VCCGT[6] VCCGT[7] VCCGT[8] VCCGT[9] VCCGT[10] VCCGT[11] VCCGT[12] VCCGT[13] VCCGT[14] VCCGT[15] VCCGT[16] VCCGT[17] VCCGT[18] VCCGT[19] VCCGT[20] VCCGT[21] VCCGT[22] VCCGT[23] VCCGT[24] VCCGT[25] VCCGT[26] VCCGT[27] VCCGT[28] VCCGT[29]

F35 G34 G35 H33 H34 J33 J35 K32 K34 L31 L33 M32

VCCGTX[11] VCCGTX[10] VCCGTX[9] VCCGTX[8] VCCGTX[7] VCCGTX[6] VCCGTX[5] VCCGTX[4] VCCGTX[3] VCCGTX[2] VCCGTX[1] VCCGTX[0]

AC7 AB8 AB7 AB6 AA7 Y7 Y6 Y8 U7 T7 R7 P7 N7 AC8 W7 V7 AA6

VCCSA[0] VCCSA[1] VCCSA[2] VCCSA[3] VCCSA[4] VCCSA[5] VCCSA[6] VCCSA[7] VCCSA[8] VCCSA[9] VCCSA[10] VCCSA[11] VCCSA[12] VCCSA[13] VCCSA[14] VCCSA[15] VCCSA[16]

U34 T40 T36 T38 R38 R34 T34 T33 R40 R39 R37 R36 R35 N36 P40 N34 P38 M38 P36 K36 P34 P33 N40 N39 N38 N37 N35 J38 M40 G36 M36 M34 M33 L40 L39 L38 L37 L36 L35 L34 K40 K38 J40 J39 J37 J36 H40 H38 G40 G39

VCCGT[30] VCCGT[31] VCCGT[32] VCCGT[33] VCCGT[34] VCCGT[35] VCCGT[36] VCCGT[37] VCCGT[38] VCCGT[39] VCCGT[40] VCCGT[41] VCCGT[42] VCCGT[43] VCCGT[44] VCCGT[45] VCCGT[46] VCCGT[47] VCCGT[48] VCCGT[49] VCCGT[50] VCCGT[51] VCCGT[52] VCCGT[53] VCCGT[54] VCCGT[55] VCCGT[56] VCCGT[57] VCCGT[58] VCCGT[59] VCCGT[60] VCCGT[61] VCCGT[62] VCCGT[63] VCCGT[64] VCCGT[65] VCCGT[66] VCCGT[67] VCCGT[68] VCCGT[69] VCCGT[70] VCCGT[71] VCCGT[72] VCCGT[73] VCCGT[74] VCCGT[75] VCCGT[76] VCCGT[77] VCCGT[78] VCCGT[79]

VCCGT_SENSE VSSGT_SENSE

F39 F38

VCCGT_SENSE (68)
VSSGT_SENSE (68)

VCCGTX_SENSE VSSGTX_SENSE

F37 F36

TPS109
TPS110

VCCSA_SENSE VSS_SAIO_SENSE

AD5 AE4

VCCSA_SENSE (71)
VSSSAIO_SENSE (71)

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Socket_LGA 1151_15u_Black

+VCCGT

+VCORE

XU1F

M30 L28 M28 L26 M26 L24 M24 L22 M22 L20 M20 L18 M18 L16 M16 J28 M14 M13 L30 L29 L27 L25 L23 L21 L19 L17 L15 L14 K31 J26 K29 J24 K27 H32 K25 G28 K23 G26 K21 K20 F34 F31 K18 K16 E28 J31 J30 J29 J27 J25 J23 J22 J21 H31 E26 H29 D35 H27 D32 H25 C29 H23 H22 C27 G32 G30 G29 G27 G25 G24 G23 F33 F32 F27 F25 F24

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75

VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110 VCC_111 VCC_112 VCC_113 VCC_114 VCC_115 VCC_116 VCC_117 VCC_118 VCC_119 VCC_120 VCC_121 VCC_122 VCC_123 VCC_124 VCC_125 VCC_126 VCC_127

F23 E36 E34 E32 E30 E27 E25 E24 D36 D34 D33 D31 D29 D27 D25 C36 C34 C32 C30 C28 C26 C25 B37 B36 B35 B34 B33 B32 B31 B29 B27 B25 A30 A29 A28 A27 A26 A25 E29 F29 AJ17 AJ19 AJ15 AJ11 AJ13 AJ21 AJ22 AJ20 AJ18 AJ16 AJ14 AJ12

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Socket_LGA 1151_15u_Black

+VCORE

Intel PDG 0.7: Request 20x22uF

Intel PDG 0.7: Request 4x22uF

+VDDQ

VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16

AY18 AY16 AV12 AW25 AW14 AW10 AV21 AV17 AV11 AU23 AU19 AU15 AU13 AT21 AT18 AY23

R6638 SHORT-PAD-15 0603_15Mil

+VCCSA

Intel PDG 0.7: Request 2x22uF

XU1J

D40 C2 B38 A4

VSS_NCTF_1 VSS_NCTF_2 VSS_NCTF_3 VSS_NCTF_4

+VCCIO

AK24 AK14 AK11 AJ23 W8 U8 P8 M8 T8

VCCIO[0] VCCIO[1] VCCIO[2] VCCIO[3] VCCIO[4] VCCIO[5] VCCIO[6] VCCIO[7] VCCIO[8]

(71) VCCIO_SENSE

AF4

VCCIO_SENSE

SHORT-PAD-15 R6641 0603_15Mil

AB38 AB37

VCC_OPC_1P8[0] VCC_OPC_1P8[1]

AK27 AJ30 AJ29 AJ28 AJ27

VCCOPC[0] VCCOPC[1] VCCOPC[2] VCCOPC[3] VCCOPC[4]

R6639 SHORT-PAD-15 0603_15Mil

20140430 Intel feedback 4+2e CPU can leave these pin floating

AK21 AK22

VCCOPC_SENSE VSSOPC_EOPIO_SENSE

TPS8 TPS9

20140430 Need double check with Intel

AJ25 AJ26 AJ24

VCCEOPIO[0] VCCEOPIO[1] VCCEOPIO_SENSE

SHORT-PAD-15 R6640 0603_15Mil

TPS72

V4 AJ9 V5 V6 U2

VCCPLL VCCPLL_OC VCCST[0] VCCST[1] VCCST_PWRGD

+1P0V_VCCST

VCCST_PWRGD_1V

R6499 0_5% 0402 NI +VCCPLL_OC
R6500 0_5% 0402 I +VDDQ

R6296 10.5K_1% 0402 NI
R6298 2.67K_1% 0402 NI

+DDR_PGOOD (63)

R6546 0_5% 0402 I +VCCST_PWRGD (59)

PU 5V_DUAL in Power page, change the R6296 to 10k-11k

10 OF 10

Socket_LGA 1151_15u_Black

20140430 Intel feedback 4+2e CPU can leave these pin floating

+1P0V_PCH_AUX +1P0V_VCCST +1P0V_VCCST

R6513 0603 0_5% NI

C1722 22uF_X5R_6.3V 0805 I

C1728 1uF_X5R_6.3V 0402 I

DELL INC.

Title: VCC/VDDDQ

DWG NO: GY SKL/ Farallon MT

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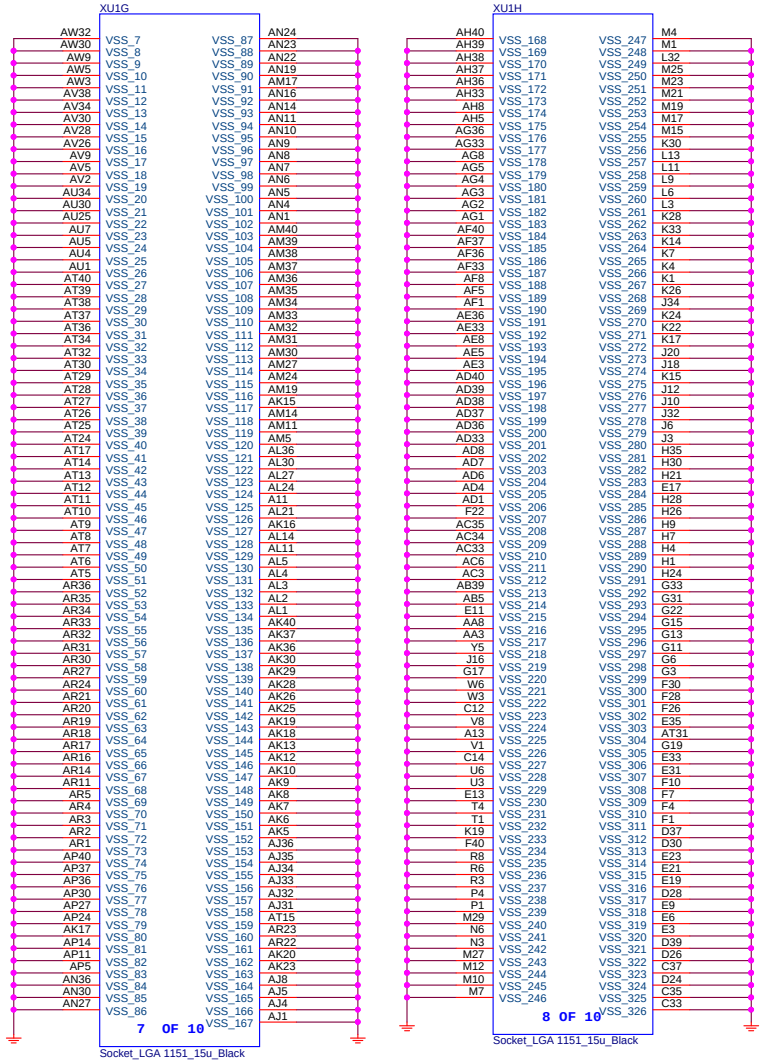

DELL INC.

Title

VSS

DWG NO

GY SKL/ Farallon MT

Rev

A00

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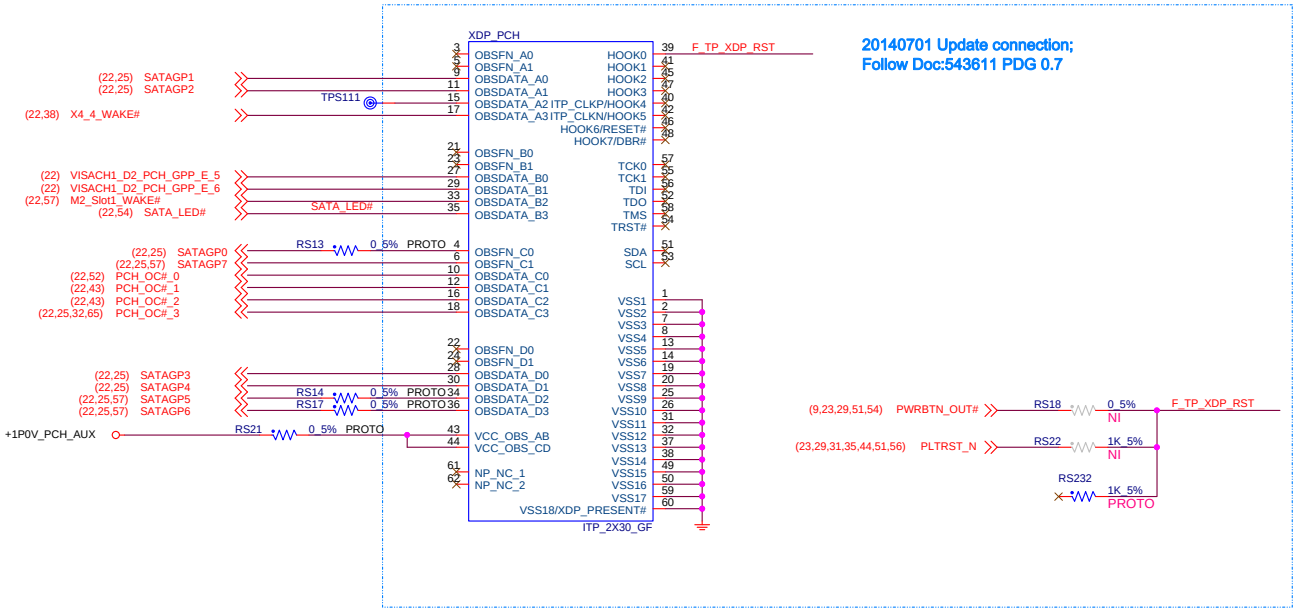
XDP Connector - PCH

Intel PCH XDP Debug Connector



Title	.PCH DEBUG PORT
DWG NO	GY SKL/ Farallon MT
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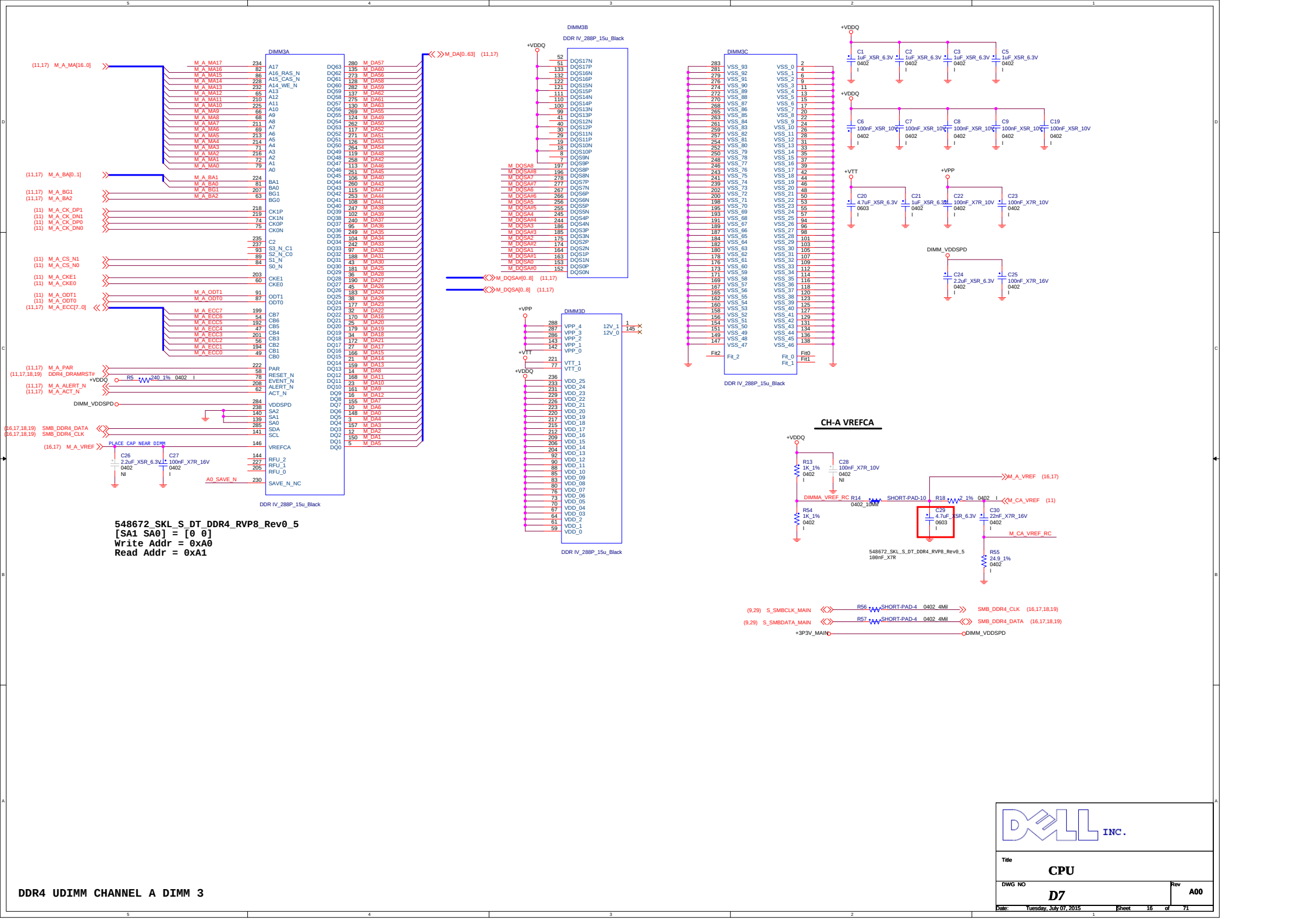
DIMM3A
DDR IV_288P_15u_Black
DIMM3B
DDR IV_288P_15u_Black
DIMM3C
DDR IV_288P_15u_Black
DIMM3D
DDR IV_288P_15u_Black
M_A_MA[16..0]
M_A_BA[0..1]
M_A_BG1
M_A_BA2
M_A_CK_DP1
M_A_CK_DN1
M_A_CK_DP0
M_A_CK_DN0
M_A_CS_N1
M_A_CS_N0
M_A_CKE1
M_A_CKE0
M_A_ODT1
M_A_ODT0
M_A_ECC[7..0]
M_A_PAR
DDR4_DRAMRST#
M_A_ALERT_N
M_A_ACT_N
DIMM_VDDSPD
SMB_DDR4_DATA
SMB_DDR4_CLK
M_A_VREF
PLACE CAP NEAR DIMM
A0_SAVE_N
M_DA[0..63]
M_DQSA#[0..8]
M_DQSA[0..8]
548672_SKL_S_DT_DDR4_RVP8_Rev0_5
[SA1 SA0] = [0 0]
Write Addr = 0xA0
Read Addr = 0xA1
DDR4 UDIMM CHANNEL A DIMM 3
CH-A VREFCA
548672_SKL_S_DT_DDR4_RVP8_Rev0_5
100nF_X7R
S_SMBCLK_MAIN
S_SMBDATA_MAIN
+3P3V_MAIN
SMB_DDR4_CLK
SMB_DDR4_DATA
DIMM_VDDSPD
DELL INC.
Title
CPU
DWG NO
D7
Rev
A00
Date: Tuesday, July 07, 2015
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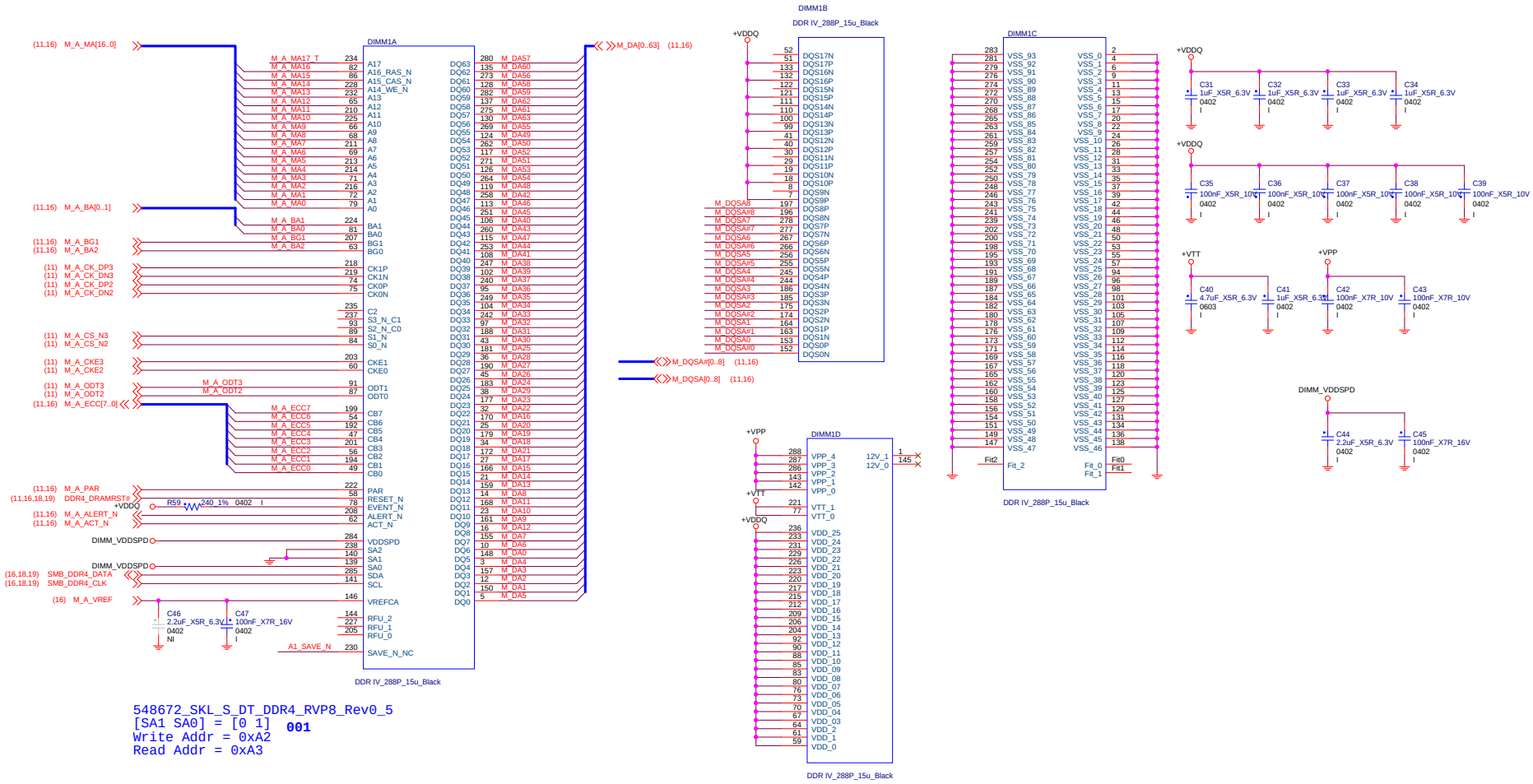

548672_SKL_S_DT_DDR4_RVP8_Rev0_5
[SA1 SA0] = [0 1] **001**
Write Addr = 0xA2
Read Addr = 0xA3

DELL INC.

Title
CPU

DWG NO
D7

Rev
A00

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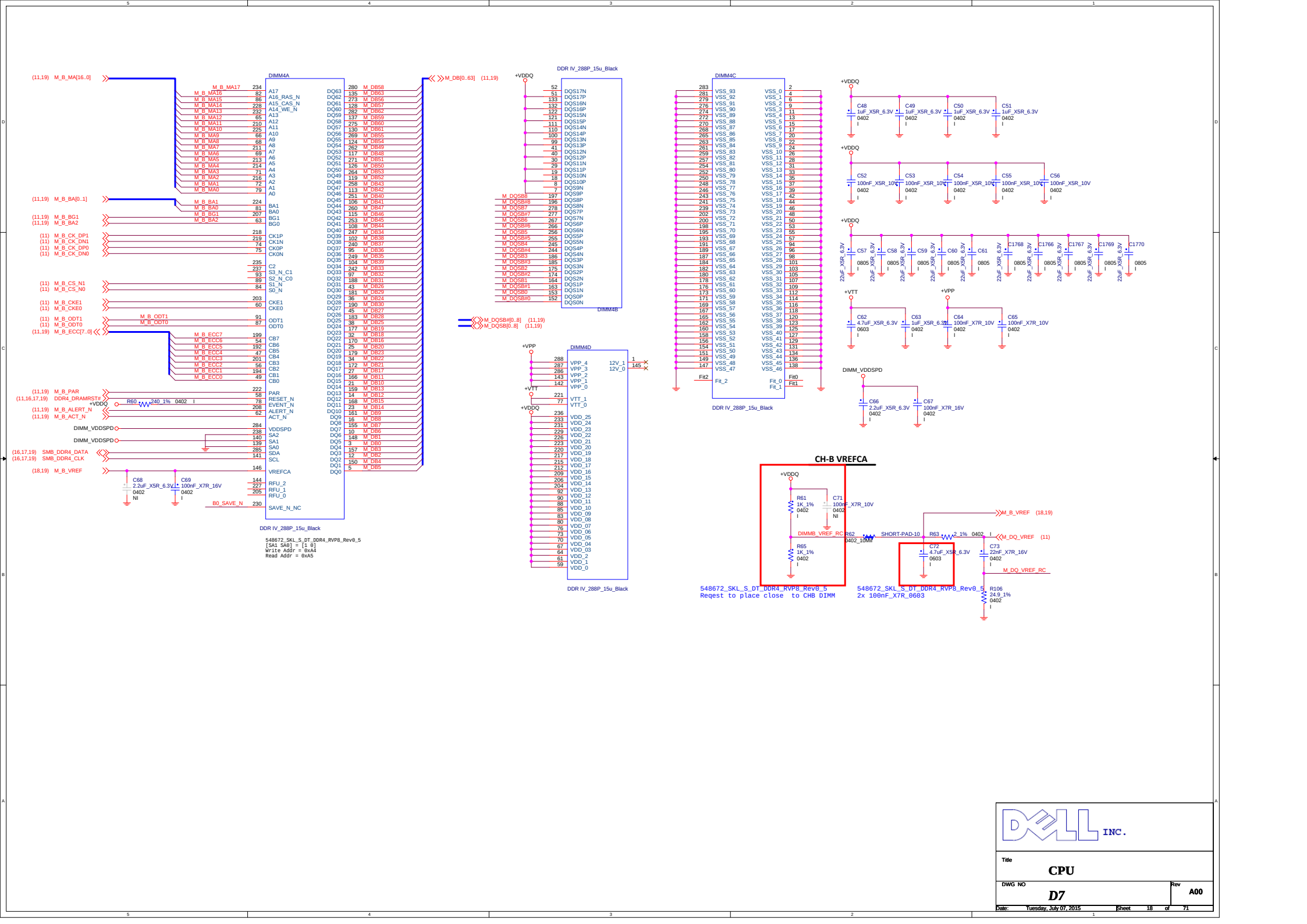
DIMM4A
DDR IV_288P_15u_Black
DIMM4B
DIMM4C
DIMM4D
M_B_MA[16..0]
M_B_BA[0..1]
M_B_BG1
M_B_BA2
M_B_CK_DP1
M_B_CK_DN1
M_B_CK_DP0
M_B_CK_DN0
M_B_CS_N1
M_B_CS_N0
M_B_CKE1
M_B_CKE0
M_B_ODT1
M_B_ODT0
M_B_ECC[7..0]
M_B_PAR
DDR4_DRAMRST#
M_B_ALERT_N
M_B_ACT_N
DIMM_VDDSPD
SMB_DDR4_DATA
SMB_DDR4_CLK
M_B_VREF
M_DB[0..63]
M_DQSB#[0..8]
M_DQSB[0..8]
+VDDQ
+VPP
+VTT
DIMM_VDDSPD
CH-B VREFCA
DIMMB_VREF_RC
SHORT-PAD-10
M_B_VREF
M_DQ_VREF
M_DQ_VREF_RC
548672_SKL_S_DT_DDR4_RVP8_Rev0_5
[SA1 SA0] = [1 0]
Write Addr = 0xA4
Read Addr = 0xA5
548672_SKL_S_DT_DDR4_RVP8_Rev0_5
Reqest to place close to CHB DIMM
548672_SKL_S_DT_DDR4_RVP8_Rev0_5
2x 100nF_X7R_0603
DELL INC.
Title
CPU
DWG NO
D7
Rev
A00
Date: Tuesday, July 07, 2015
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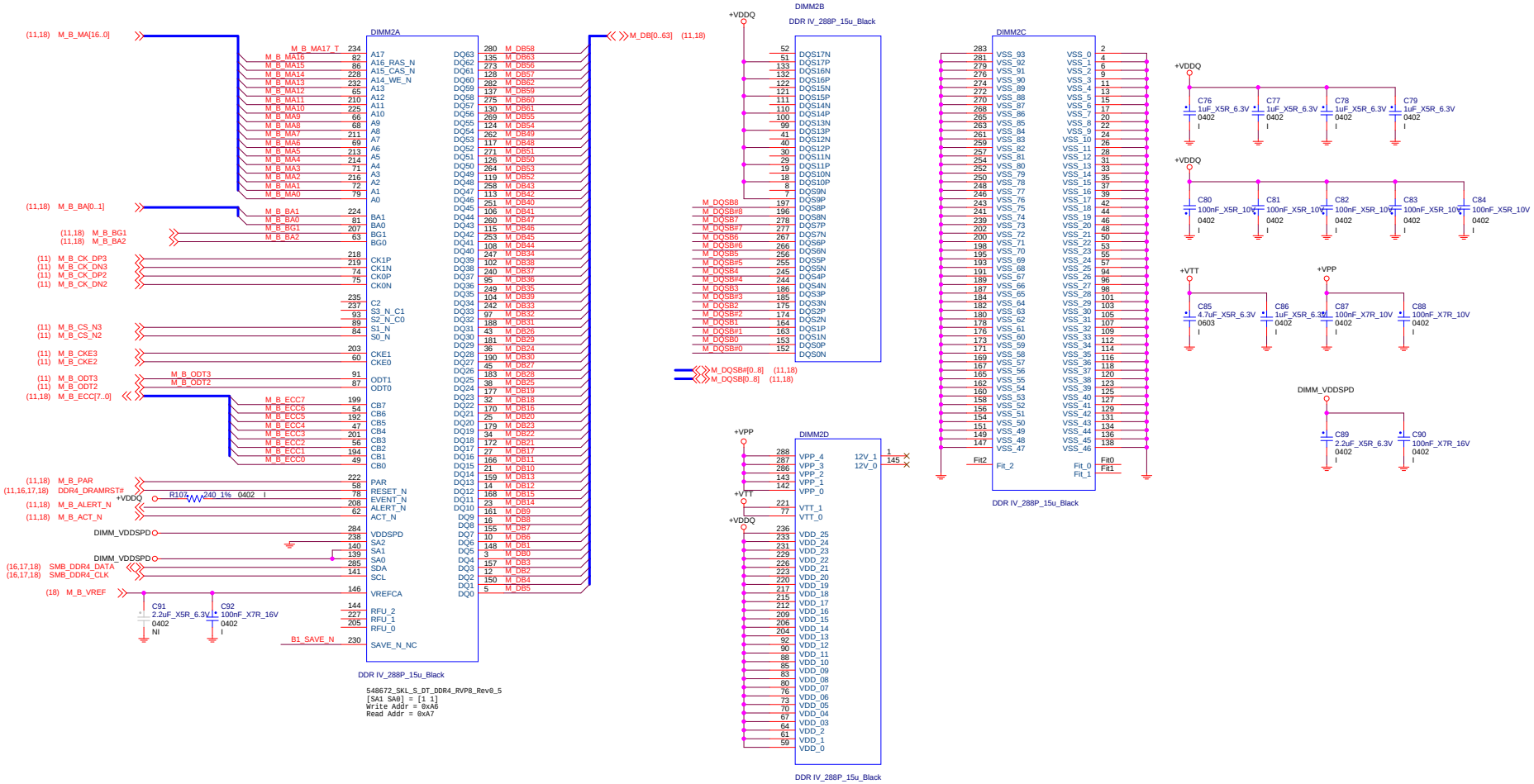

Title	CPU
DWG NO	D7
Rev	A00
Date:	Tuesday, July 07, 2015
Sheet	19 of 71

It is highly recommended to have DMI on surfaced vias (not buried).

U4A

(12) DMI_CPU_PCH_RXN0 → L27 DMI_RXN0
(12) DMI_CPU_PCH_RXP0 → N27 DMI_RXP0
(12) DMI_PCH_CPU_RXN0 → C27 DMI_TXN0
(12) DMI_PCH_CPU_RXP0 → B27 DMI_TXP0
(12) DMI_CPU_PCH_RXN1 → E24 DMI_RXN1
(12) DMI_CPU_PCH_RXP1 → G24 DMI_RXP1
(12) DMI_PCH_CPU_RXN1 → B28 DMI_TXN1
(12) DMI_PCH_CPU_RXP1 → A28 DMI_TXP1
(12) DMI_CPU_PCH_RXN2 → G27 DMI_RXN2
(12) DMI_CPU_PCH_RXP2 → E26 DMI_RXP2
(12) DMI_PCH_CPU_RXN2 → B29 DMI_TXN2
(12) DMI_PCH_CPU_RXP2 → C29 DMI_TXP2
(12) DMI_CPU_PCH_RXN3 → L29 DMI_RXN3
(12) DMI_CPU_PCH_RXP3 → K29 DMI_RXP3
(12) DMI_PCH_CPU_RXN3 → B30 DMI_TXN3
(12) DMI_PCH_CPU_RXP3 → A30 DMI_TXP3

DMI

PCH_PERN1 → H15 PERN1 / USB3RN7
PCH_PERP1 → G15 PERP1 / USB3RP7
PCH_PETN1 → A16 PETN1 / USB3TN7
PCH_PETP1 → B16 PETP1 / USB3TP7
TPS125 → E17 PERN2 / USB3RN8
TPS124 → G17 PERP2 / USB3RP8
TPS127 → B19 PETN2 / USB3TN8
TPS126 → C19 PETP2 / USB3TP8
TPS121 → L17 PERN3 / USB3RN9
TPS120 → K17 PERP3 / USB3RP9
TPS123 → B20 PETN3 / USBTN9
TPS122 → C20 PETP3 / USBTP9

PCI-E

M.2 WLAN

LAN
(31) X_L1X1_RXN → E20 PERN4 / USBRN10
(31) X_L1X1_RXP → G19 PERP4 / USBRP10
(31) X_L1X1_TXN → B21 PETN4 / USBTN10
(31) X_L1X1_TXP → A21 PETP4 / USBTP10

PCIE Slot4(PCIEx4)
(38) X_2X4_RXN0 → K19 PERN5
(38) X_2X4_RXP0 → L19 PERP5
(38) X_2X4_TXN0 → D22 PETN5
(38) X_2X4_TXP0 → C22 PETP5
(38) X_2X4_RXN1 → G22 PERN6
(38) X_2X4_RXP1 → E22 PERP6
(38) X_2X4_TXN1 → B22 PETN6
(38) X_2X4_TXP1 → A23 PETP6
(38) X_2X4_RXN2 → L22 PERN7
(38) X_2X4_RXP2 → K22 PERP7
(38) X_2X4_TXN2 → C23 PETN7
(38) X_2X4_TXP2 → B23 PETP7
(38) X_2X4_RXN3 → K24 PERN8
(38) X_2X4_RXP3 → L24 PERP8
(38) X_2X4_TXN3 → C24 PETN8
(38) X_2X4_TXP3 → B24 PETP8

PCIE Slot3(PCIEx4)
(37) X_1X4_RXN0 → G31 PERN9 / SATA0A_RN
(37) X_1X4_RXP0 → H31 PERP9 / SATA0A_RP
(37) X_1X4_TXN0 → C31 PETN9 / SATA0A_TN
(37) X_1X4_TXP0 → B31 PETP9 / SATA0A_TP
(37) X_1X4_RXN1 → G29 PERN10 / SATA1A_RN
(37) X_1X4_RXP1 → E29 PERP10 / SATA1A_RP
(37) X_1X4_TXN1 → C32 PETN10 / SATA1A_TN
(37) X_1X4_TXP1 → B32 PETP10 / SATA1A_TP
(37) X_1X4_RXN2 → L31 PERN11
(37) X_1X4_RXP2 → K31 PERP11
(37) X_1X4_TXN2 → C33 PETN11
(37) X_1X4_TXP2 → B33 PETP11
(37) X_1X4_RXN3 → G33 PERN12
(37) X_1X4_RXP3 → H33 PERP12
(37) X_1X4_TXN3 → B35 PETN12
(37) X_1X4_TXP3 → A35 PETP12

1 OF 10

GLZ170_D1,SR2C9

Change BOM option.

USB

USB2N1 → AF5 → USB_N1 (52) — Front USB3
USB2P1 → AG7 → USB_P1 (52) — Front USB3
USB2N2 → AD5 → USB_N2 (52) — Front USB3
USB2P2 → AD7 → USB_P2 (52) — Front USB3
USB2N3 → AG8 → USB_N3 (43) — REAR USB3x4
USB2P3 → AG10 → USB_P3 (43) — REAR USB3x4
USB2N4 → AE1 → USB_N4 (43) — REAR USB3x4
USB2P4 → AE2 → USB_P4 (43) — REAR USB3x4
USB2N5 → AC2 → USB_N5 (43) — REAR USB3x4
USB2P5 → AC3 → USB_P5 (43) — REAR USB3x4
USB2N6 → AF2 → USB_N6 (32) — LAN+USB (J9)
USB2P6 → AF3 → USB_P6 (32) — LAN+USB (J9)
USB2N7 → AB3 → USB_N7 (43) — REAR USB3x4
USB2P7 → AB2 → USB_P7 (43) — REAR USB3x4
USB2N8 → AL8 → USB_N8 (32) — LAN+USB (J9)
USB2P8 → AL7 → USB_P8 (32) — LAN+USB (J9)
USB2N9 → AA1 → USB_N9 (54,55) — FRONT USB2x2
USB2P9 → AA2 → USB_P9 (54,55) — FRONT USB2x2
USB2N10 → AJ8 → USB_N10 (55) — FRONT USB2x2
USB2P10 → AJ7 → USB_P10 (55) — FRONT USB2x2
USB2N11 → W2 → USB_N11 (57) — M.2 NGFF
USB2P11 → W3 → USB_P11 (57) — M.2 NGFF
USB2N12 → AD3 → USB_N12 (50) — Internal USB2
USB2P12 → AD2 → USB_P12 (50) — Internal USB2
USB2N13 → V2 → USB_N13 (50) — Internal USB2
USB2P13 → V1 → USB_P13 (50) — Internal USB2
USB2N14 → AJ11
USB2P14 → AJ13

USB2_ID → AG2
USB2_VBUSSENSE → AD10
USB2_ID — R6602 1K_5% 0402 I
PD_USB2_VBUSSENSE — R6331 1K_5% 0402 I

USB3RN1 → B7 → USB3_RXDN1 (52) — Front USB3
USB3RP1 → A7 → USB3_RXDP1 (52) — Front USB3
USB3TN1 → C11 → USB3_TXDN1 (52) — Front USB3
USB3TP1 → B11 → USB3_TXDP1 (52) — Front USB3
USB3RN2 → C8 → USB3_RXDN2 (52) — Front USB3
USB3RP2 → B8 → USB3_RXDP2 (52) — Front USB3
USB3TN2 → B12 → USB3_TXDN2 (52) — Front USB3
USB3TP2 → A12 → USB3_TXDP2 (52) — Front USB3
USB3RN3 → B10 → USB3_RXDN3 (43) — REAR USB3x4
USB3RP3 → A9 → USB3_RXDP3 (43) — REAR USB3x4
USB3TN3 → C13 → USB3_TXDN3 (43) — REAR USB3x4
USB3TP3 → D13 → USB3_TXDP3 (43) — REAR USB3x4
USB3RN4 → E11 → USB3_RXDN4 (43) — REAR USB3x4
USB3RP4 → G11 → USB3_RXDP4 (43) — REAR USB3x4
USB3TN4 → A14 → USB3_TXDN4 (43) — REAR USB3x4
USB3TP4 → B13 → USB3_TXDP4 (43) — REAR USB3x4
USB3RN5 → G13 → USB3_RXDN5 (43) — REAR USB3x4
USB3RP5 → H13 → USB3_RXDP5 (43) — REAR USB3x4
USB3TN5 → B14 → USB3_TXDN5 (43) — REAR USB3x4
USB3TP5 → C14 → USB3_TXDP5 (43) — REAR USB3x4
USB3RN6 → K15 → USB3_RXDN6 (43) — REAR USB3x4
USB3RP6 → K13 → USB3_RXDP6 (43) — REAR USB3x4
USB3TN6 → B15 → USB3_TXDN6 (43) — REAR USB3x4
USB3TP6 → C15 → USB3_TXDP6 (43) — REAR USB3x4

USB3 and USB2 port mapping is not clear in PDG.
Have to check again if Intel releases new PDG.

PCIe to PCI bridge
(56) PCH_HSIN2 → RU188 0_5% NI,I → PCH_PERN1
(56) PCH_HSIP2 → RU189 0_5% NI,I → PCH_PERP1
(56) PCH_HSON2 → RU192 0_5% NI,I → PCH_PETN1
(56) PCH_HSOP2 → RU193 0_5% NI,I → PCH_PETP1

M.2 WLAN
(57) PCH_HSIN3 → RU190 0_5% I,NI
(57) PCH_HSIP3 → RU191 0_5% I,NI
(57) PCH_HSON3 → RU194 0_5% I,NI
(57) PCH_HSOP3 → RU195 0_5% I,NI

DELL INC.

Title: PCH - DMI/ PCIE/ USB2/3

DWG NO: GY SKL/ Farallon MT

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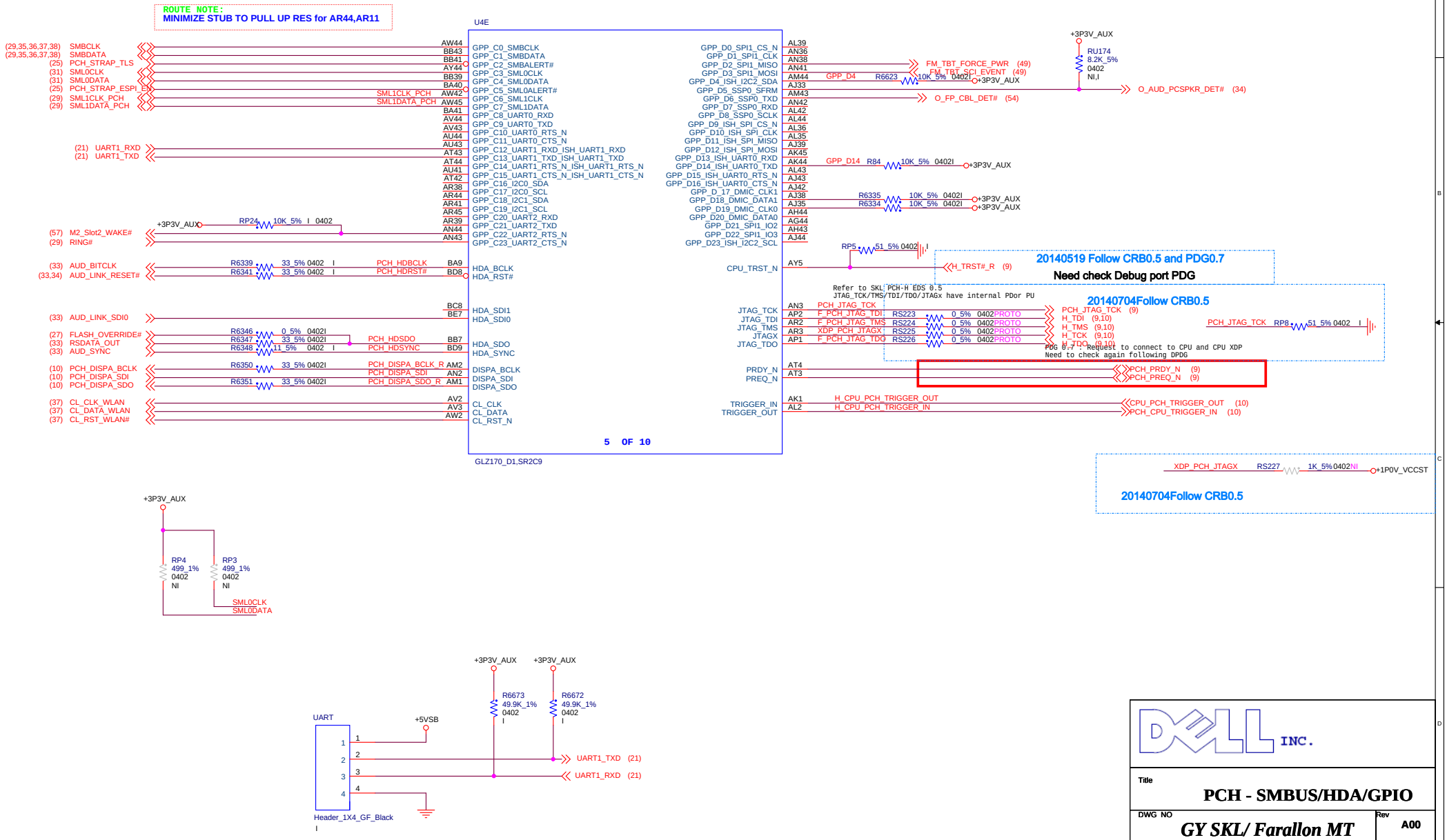
Date: Tuesday, July 07, 2015 Sheet 20 of 71


ROUTE NOTE:
MINIMIZE STUB TO PULL UP RES for AR44,AR11
U4E
5 OF 10
GLZ170_D1,SR2C9
20140519 Follow CRB0.5 and PDG0.7
Need check Debug port PDG
20140704Follow CRB0.5
Refer to SKL PCH-H EDS 0.5
JTAG_TCK/TMS/TDI/TDO/JTAGx have internal PDor PU
PDG 0.7 - Request to connect to CPU and CPU XDP
Need to check again following DPDG
20140704Follow CRB0.5
UART
Header_1X4_GF_Black
DELL INC.
Title
PCH - SMBUS/HDA/GPIO
DWG NO
GY SKL/ Farallon MT
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U4B
SATA_RXN0B / PERN13
SATA_RXP0B / PERP13
SATA_TXN0B / PETN13
SATA_TXP0B / PETP13
SATA_RXN1B / PERN14
SATA_RXP1B / PERP14
SATA_TXN1B / PETN14
SATA_TXP1B / PETP14
SATA_RXN2 / PERN15
SATA_RXP2 / PERP15
SATA_TXN2 / PETN15
SATA_TXP2 / PETP15
SATA_RXN3 / PERN16
SATA_RXP3 / PERP16
SATA_TXN3 / PETN16
SATA_TXP3 / PETP16
SATA_RXN4 / PERN17
SATA_RXP4 / PERP17
SATA_TXN4 / PETN17
SATA_TXP4 / PETP17
SATA_RXN5 / PERN18
SATA_RXP5 / PERN18
SATA_TXN5 / PERN18
SATA_TXP5 / PERN18
PERN19
PERP19
PETN19
PETP19
PERN20
PERP20
PETN20
PETP20
GPP_E3_CPU_GP0
GPP_E7_CPU_GP1
GPP_E4_DEVSLP0
GPP_E5_DEVSLP1
GPP_E6_DEVSLP2
GPP_F5_DEVSLP3
GPP_F6_DEVSLP4
GPP_F7_DEVSLP5
GPP_F8_DEVSLP6
GPP_F9_DEVSLP7
GPP_I0_DDPB_HPD0
GPP_I1_DDPC_HPD1
GPP_I2_DDPD_HPD2
GPP_I3_DDPE_HPD3
GPP_I4_EDP_HPD
GPP_I5_DDPB_CTRLCLK
GPP_I6_DDPB_CTRLDATA
GPP_I7_DDPC_CTRLCLK
GPP_I8_DDPC_CTRLDATA
GPP_I9_DDPD_CTRLCLK
GPP_I10_DDPD_CTRLDATA
2 OF 10
GLZ170_D1,SR2C9
GPP_E0_SATAXPCIE0_SATAGP0
GPP_E1_SATAXPCIE1_SATAGP1
GPP_E2_SATAXPCIE2_SATAGP2
GPP_F0_SATAXPCIE3_SATAGP3
GPP_F1_SATAXPCIE4_SATAGP4
GPP_F2_SATAXPCIE5_SATAGP5
GPP_F3_SATAXPCIE6_SATAGP6
GPP_F4_SATAXPCIE7_SATAGP7
GPP_E8_SATALED_N
GPP_F10_SCLOCK
GPP_F11_SLOAD
GPP_F12_SDATAOUT1
GPP_F13_SDATAOUT0
GPP_F19_EDP_VDDEN
GPP_F20_EDP_BKLTEN
GPP_F21_EDP_BKLTCTL
GPP_F14
GPP_F22
GPP_F23
GPP_E9_USB2_OC0_N
GPP_E10_USB2_OC1_N
GPP_E11_USB2_OC2_N
GPP_E12_USB2_OC3_N
GPP_F15_USB2_OCB_4
GPP_F16_USB2_OCB_5
GPP_F17_USB2_OCB_6
GPP_F18_USB2_OCB_7
SATAGP0
SATAGP1
SATAGP2
SATAGP3
SATAGP4
SATAGP5
SATAGP6
SATAGP7
SATA_LED#
H_SKTOCC#
GPIO_PEG SLOT_RESET
S_PCIAUX_GATE
PCH_OC#_0
PCH_OC#_1
PCH_OC#_2
PCH_OC#_3
PCH_OC#_4
PCH_OC#_5
PCH_OC#_6
+3P3V_AUX
SHORT-PAD-4
M.2_SSD_PEDET
20140519 Follow CRB0.5
Need to check Intel design guide for OC# port mapping
U4F
GPP_A0_RCIN_N_ESPI_ALERT1_N
GPP_A1_LAD0_ESPI_IO0
GPP_A2_LAD1_ESPI_IO1
GPP_A3_LAD2_ESPI_IO2
GPP_A4_LAD3_ESPI_IO3
GPP_A5_LFRAME_N_ESPI_CS_N
GPP_A6_SERIRQ
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N
GPP_A13_SUSWARN_N_SUSPWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RST_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5
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GLZ170_D1,SR2C9
GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23
SPI0_CLK
SPI0_CS0#
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_MISO
SPI0_MOSI
SPI0_CS2#
PM_DOWN
PM_SYNC
PECI
MB_SERIES_ID0
MB_SERIES_ID1
FORM_FACTOR_ID0
FORM_FACTOR_ID1
S_GPI_BRD_REV0
S_GPI_BRD_REV1
S_USB2_HDR_DET#
DPC_HPD_R
DPD_HPD_R
MB_SERIES_ID2
S_PSWD_CLR
S_USB3_HDR_DET#
INT_USB_DET2#
A_FP_PRES#
S_INTRUD_CBL_DET#
Charge_CTL3
Charge_power
5V_SMART_USB_EN
UEFI_S
CPU_FAN_OFF
SYS_FAN_OFF
CL_SENCE#
SER_SENCE#
PCH_FVS
SPI_SCK
SPI_CS#
SPI_IO2
SPI_IO3
SPI_MISO
SPI_MOSI
SPI_TPM_CS2#
PMDOWN
PMSYNC#
H_PECI
UEFI
FVS
Dummy
TEST POINT
20140516 Folow CRB0.5
EPSI Interface
ESPI_IO[3:0]
ESPI_CLK
ESPI_CS#
ESPI_RESET#
LPC
RES place close to
PCH within 2inch
P1V8_P3V3_PCH_GPPA
LPC : 3.3V
ESPI : 1.8V
DELL INC.
Title
PCH - SATA/SPI/GPIO
DWG NO
GY SKL/ Farallon MT
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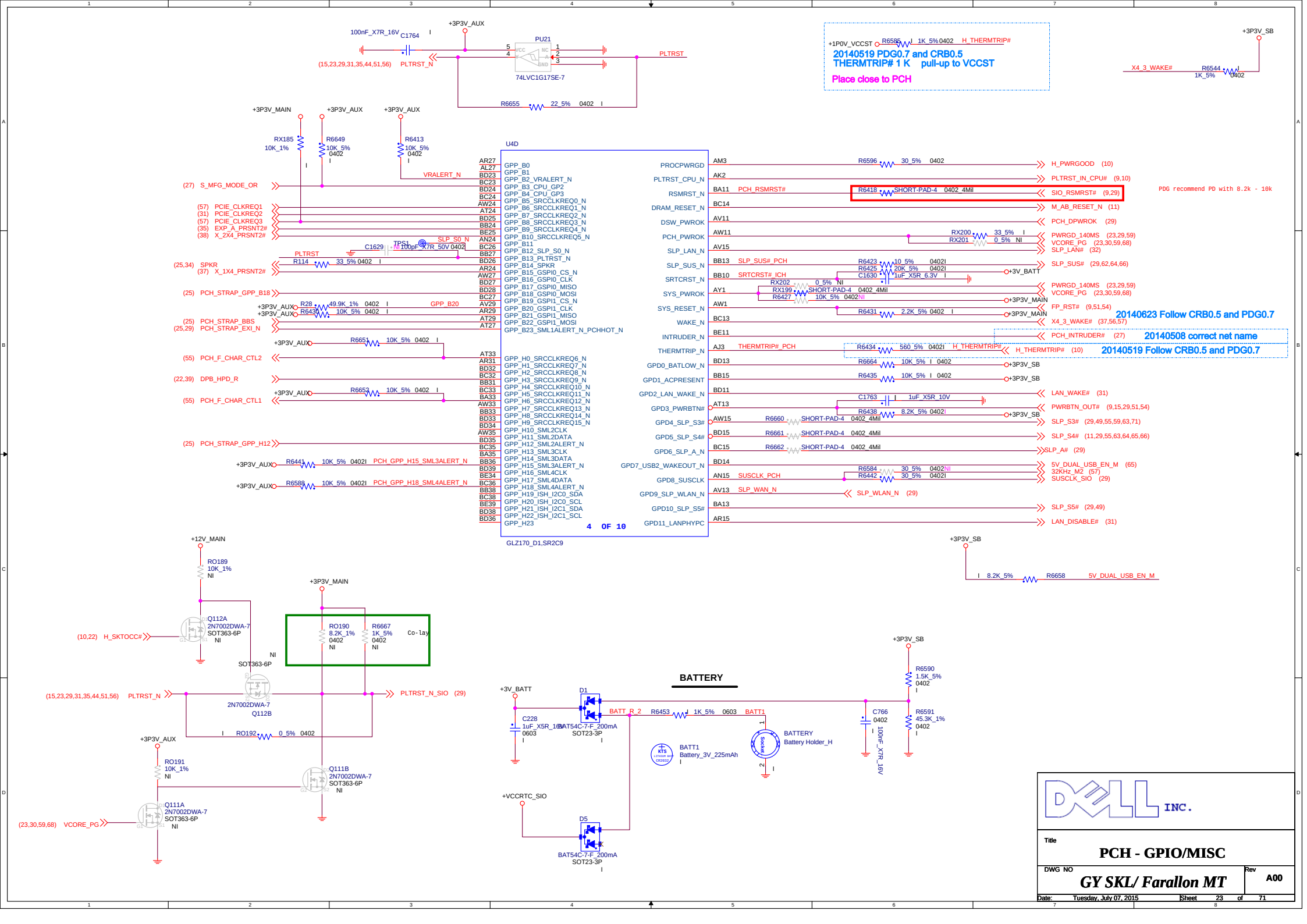
+3P3V_AUX
100nF_X7R_16V
C1764
PU21
74LVC1G17SE-7
PLTRST_N
PLTRST
R6655 22_5% 0402
+1P0V_VCCST
R6585 1K_5% 0402 H_THERMTRIP#
20140519 PDG0.7 and CRB0.5
THERMTRIP# 1 K pull-up to VCCST
Place close to PCH
+3P3V_SB
X4_3_WAKE#
R6544 1K_5% 0402
+3P3V_MAIN
RX185 10K_1%
R6649 10K_5% 0402
R6413 10K_5% 0402
VRALERT_N
U4D
GPP_B0
GPP_B1
GPP_B2_VRALERT_N
GPP_B3_CPU_GP2
GPP_B4_CPU_GP3
GPP_B5_SRCCLKREQ0_N
GPP_B6_SRCCLKREQ1_N
GPP_B7_SRCCLKREQ2_N
GPP_B8_SRCCLKREQ3_N
GPP_B9_SRCCLKREQ4_N
GPP_B10_SRCCLKREQ5_N
GPP_B11
GPP_B12_SLP_S0_N
GPP_B13_PLTRST_N
GPP_B14_SPKR
GPP_B15_GSPI0_CS_N
GPP_B16_GSPI0_CLK
GPP_B17_GSPI0_MISO
GPP_B18_GSPI0_MOSI
GPP_B19_GSPI1_CS_N
GPP_B20_GSPI1_CLK
GPP_B21_GSPI1_MISO
GPP_B22_GSPI1_MOSI
GPP_B23_SML1ALERT_N_PCHHOT_N
GPP_H0_SRCCLKREQ6_N
GPP_H1_SRCCLKREQ7_N
GPP_H2_SRCCLKREQ8_N
GPP_H3_SRCCLKREQ9_N
GPP_H4_SRCCLKREQ10_N
GPP_H5_SRCCLKREQ11_N
GPP_H6_SRCCLKREQ12_N
GPP_H7_SRCCLKREQ13_N
GPP_H8_SRCCLKREQ14_N
GPP_H9_SRCCLKREQ15_N
GPP_H10_SML2CLK
GPP_H11_SML2DATA
GPP_H12_SML2ALERT_N
GPP_H13_SML3CLK
GPP_H14_SML3DATA
GPP_H15_SML3ALERT_N
GPP_H16_SML4CLK
GPP_H17_SML4DATA
GPP_H18_SML4ALERT_N
GPP_H19_ISH_I2C0_SDA
GPP_H20_ISH_I2C0_SCL
GPP_H21_ISH_I2C1_SDA
GPP_H22_ISH_I2C1_SCL
GPP_H23
4 OF 10
GLZ170_D1,SR2C9
PROCPWRGD
PLTRST_CPU_N
RSMRST_N
DRAM_RESET_N
DSW_PWROK
PCH_PWROK
SLP_LAN_N
SLP_SUS_N
SRTCRST_N
SYS_PWROK
SYS_RESET_N
WAKE_N
INTRUDER_N
THERMTRIP_N
GPD0_BATLOW_N
GPD1_ACPRESENT
GPD2_LAN_WAKE_N
GPD3_PWRBTN#
GPD4_SLP_S3#
GPD5_SLP_S4#
GPD6_SLP_A_N
GPD7_USB2_WAKEOUT_N
GPD8_SUSCLK
GPD9_SLP_WLAN_N
GPD10_SLP_S5#
GPD11_LANPHYPC
(27) S_MFG_MODE_OR
(57) PCIE_CLKREQ1
(31) PCIE_CLKREQ2
(57) PCIE_CLKREQ3
(35) EXP_A_PRSNT2#
(38) X_2X4_PRSNT2#
TPS1
C1629 100pF_X7R_50V 0402
SLP_S0_N
PLTRST
(25,34) SPKR
(37) X_1X4_PRSNT2#
R114 33_5% 0402
(25) PCH_STRAP_GPP_B18
R28 49.9K_1% 0402
R643 10K_5% 0402
GPP_B20
(25) PCH_STRAP_BBS
(25,29) PCH_STRAP_EXI_N
R6651 10K_5% 0402
(55) PCH_F_CHAR_CTL2
(22,39) DPB_HPD_R
R6652 10K_5% 0402
(55) PCH_F_CHAR_CTL1
(25) PCH_STRAP_GPP_H12
R6441 10K_5% 0402I PCH_GPP_H15_SML3ALERT_N
R6588 10K_5% 0402I PCH_GPP_H18_SML4ALERT_N
AM3 PROCPWRGD
AK2 PLTRST_CPU_N
BA11 PCH_RSMRST#
BC14 DRAM_RESET_N
AV11 DSW_PWROK
AW11 PCH_PWROK
AV15 SLP_LAN_N
BB13 SLP_SUS#_PCH
BB10 SRTCRST#_ICH
AY1 SYS_PWROK
AW1 SYS_RESET_N
BC13 WAKE_N
BE11 INTRUDER_N
AJ3 THERMTRIP#_PCH
BD13 GPD0_BATLOW_N
BB15 GPD1_ACPRESENT
BD11 GPD2_LAN_WAKE_N
AT13 GPD3_PWRBTN#
AW15 GPD4_SLP_S3#
BD15 GPD5_SLP_S4#
BC15 GPD6_SLP_A_N
BD14 GPD7_USB2_WAKEOUT_N
AN15 SUSCLK_PCH
AV13 SLP_WAN_N
BA13 GPD10_SLP_S5#
AR15 GPD11_LANPHYPC
R6596 30_5% 0402
R6418 SHORT-PAD-4 0402_4Mil
RX200 33_5%
RX201 0_5% NI
R6423 10_5% 0402I
R6425 20K_5% 0402I
C1630 1uF_X5R_6.3V
+3V_BATT
RX202 0_5% NI
RX199 SHORT-PAD-4 0402_4Mil
R6427 10K_5% 0402NI
R6431 2.2K_5% 0402
R6434 560_5% 0402I H_THERMTRIP#
R6664 10K_5% 0402
R6435 10K_5% 0402
C1763 1uF_X5R_10V
R6438 8.2K_5% 0402I
R6660 SHORT-PAD-4 0402_4Mil
R6661 SHORT-PAD-4 0402_4Mil
R6662 SHORT-PAD-4 0402_4Mil
R6584 30_5% 0402NI
R6442 30_5% 0402I
SLP_WLAN_N (29)
H_PWRGOOD (10)
PLTRST_IN_CPU# (9,10)
SIO_RSMRST# (9,29)
PDG recommend PD with 8.2k - 10k
M_AB_RESET_N (11)
PCH_DPWROK (29)
PWRGD_140MS (23,29,59)
VCORE_PG (23,30,59,68)
SLP_LAN# (32)
SLP_SUS# (29,62,64,66)
PWRGD_140MS (23,29,59)
VCORE_PG (23,30,59,68)
FP_RST# (9,51,54)
20140623 Follow CRB0.5 and PDG0.7
X4_3_WAKE# (37,56,57)
PCH_INTRUDER# (27)
20140508 correct net name
H_THERMTRIP# (10)
20140519 Follow CRB0.5 and PDG0.7
LAN_WAKE# (31)
PWRBTN_OUT# (9,15,29,51,54)
SLP_S3# (29,49,55,59,63,71)
SLP_S4# (11,29,55,63,64,65,66)
SLP_A# (29)
5V_DUAL_USB_EN_M (65)
32KHz_M2 (57)
SUSCLK_SIO (29)
SLP_S5# (29,49)
LAN_DISABLE# (31)
+3P3V_SB
8.2K_5% R6658 5V_DUAL_USB_EN_M
+12V_MAIN
RO189 10K_1% NI
Q112A 2N7002DWA-7 SOT363-6P NI
(10,22) H_SKTOCC#
RO190 8.2K_1% 0402 NI
R6667 1K_5% 0402 NI
Co-lay
SOT363-6P NI
2N7002DWA-7 Q112B
(15,23,29,31,35,44,51,56) PLTRST_N
PLTRST_N_SIO (29)
RO192 0_5% 0402
RO191 10K_1% NI
Q111A 2N7002DWA-7 SOT363-6P NI
Q111B 2N7002DWA-7 SOT363-6P NI
(23,30,59,68) VCORE_PG
BATTERY
+3V_BATT
D1
C228 1uF_X5R_16V 0603
BAT54C-7-F_200mA SOT23-3P
BATT_R_2
R6453 1K_5% 0603
BATT1
BATT1 Battery_3V_225mAh
BATTERY Battery Holder_H
C766 0402 100nF_X7R_16V
R6590 1.5K_5% 0402
R6591 45.3K_1% 0402
+VCCRTC_SIO
D5
BAT54C-7-F_200mA SOT23-3P
DELL INC.
Title
PCH - GPIO/MISC
DWG NO
GY SKL/ Farallon MT
Rev
A00
Date: Tuesday, July 07, 2015
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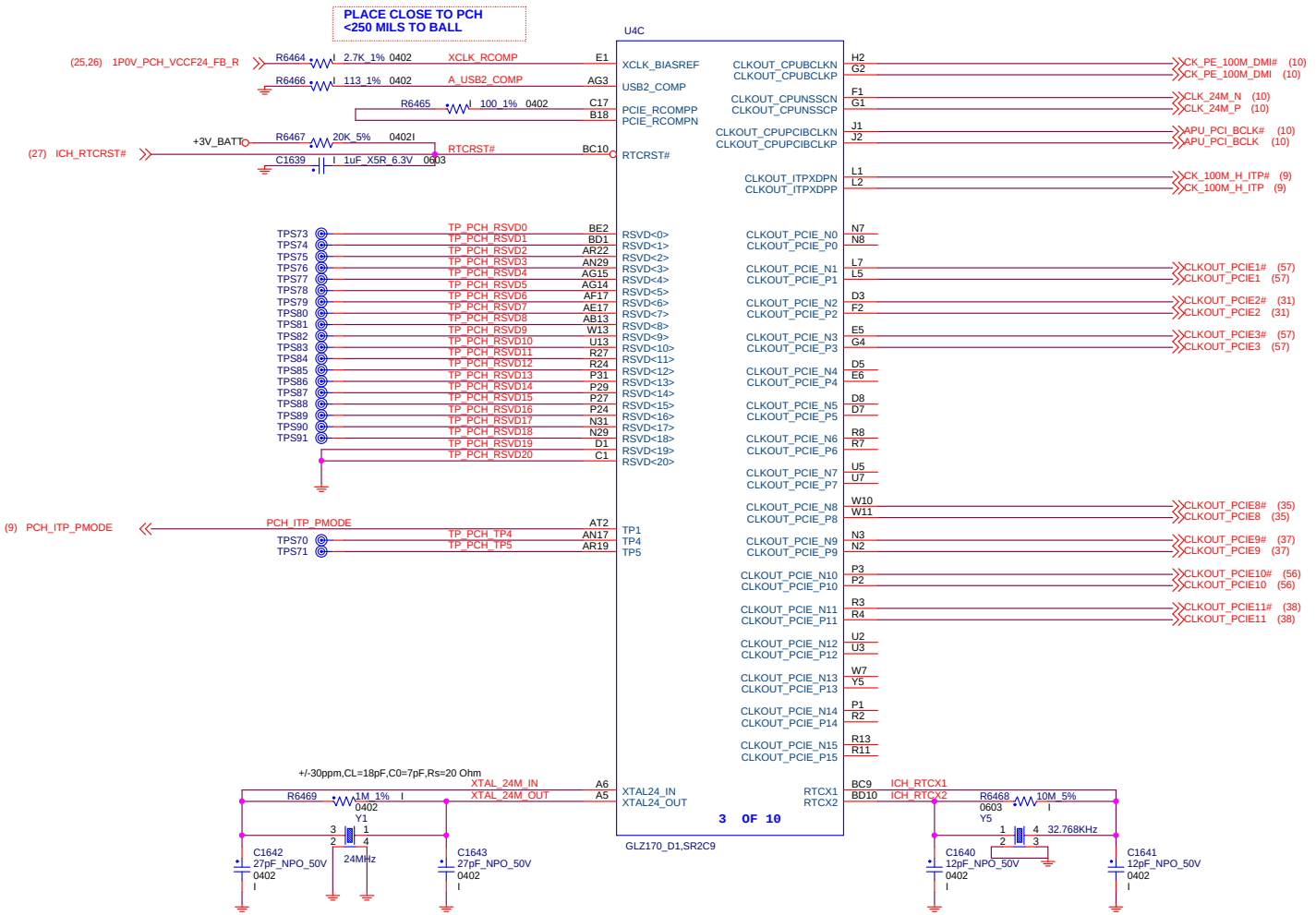
PCH - CLOCK DISTRIBUTION



DELL INC.

Title

PCH - CLOCK

DWG NO *GY SKL/ Farallon MT*

Rev A00

Date: Tuesday, July 07, 2015 Sheet 24 of 71

P1V8_P3V3_PCH_GPPA
1.8V for ESPI mode
3.3 for LPC mode

20140506 ARD0.92 : Follow CRB0.5

20140506 ARD0.92 : Follow CRB0.5

TLS CONFIDENTIALITY
0: DISABLE
1: ENABLE (DEFAULT)

NO REBOOT
0: DISABLE (DEFAULT)
1: ENABLE

ESPI ENABLE STRAP
0: LPC
1: ESPI

BOOT BIOS STRAP
0: SPI
1: ESPI/LPC

BOOT HALF STRAP(DFX)
0: ENABLE
1: DISABLE (PCH INT PULL-UP)

HI: SATA
LO: PCIE

SATA0 PCIE13
SATA1 PCIE14
SATA2 PCIE15
SATA3 PCIE16
SATA4 PCIE17
SATA5 PCIE18

20140626 add pull down reister, Follow CRB0.5

EXI BOOT STALLBYPASS STRAP
0: DISABLE (DEFAULT)
1: ENABLE

20140626 add pull down reister, Follow CRB0.5

ESPI FLASH SHARING MODE STRAP
0: DISABLE (DEFAULT)
1: SLAVE ATTACHED FLASH SHARING

20140626 add pull high reister, Follow CRB0.5

JTAG ODT DISABLE STRAP(DFX)
0: DISABLE
1: ENABLE

20140626 add pull high reister, Follow CRB0.5

BOOT HALF STRAP(DFX)
0: ENABLE
1: DISABLE (PCH INT PULL-UP)

EDS show the power is primary power
but AIO CRB connection to 3.3main power

TOP SWAP OVERRIDE STRAP
0:TOP SWAP DISABLED(DEFAULT)
1:TOP SWAP ENABLED
PCH HAS INTERNAL WEAK PD

20140626 add pull high reister, Follow CRB0.5

CONSENT ADN PERSONALITY STRAP(DXF)
0: ENABLE
1: DISABLE

20140626 add pull high reister, Follow CRB0.5

PESONALITY STRAP
0: ENABLE
1: DISABLE

20140626 add this strap pin, Follow CRB0.5

DFX TEST MODE
0: XTAL INPUT IS SINGLE ENDED
1: XTAL INPUT IS DIFFERENTIAL

2014.5.26: Need to link to GPIO

Title	PCH - POWER & GND
DWG NO	GY SKL/ Farallon MT
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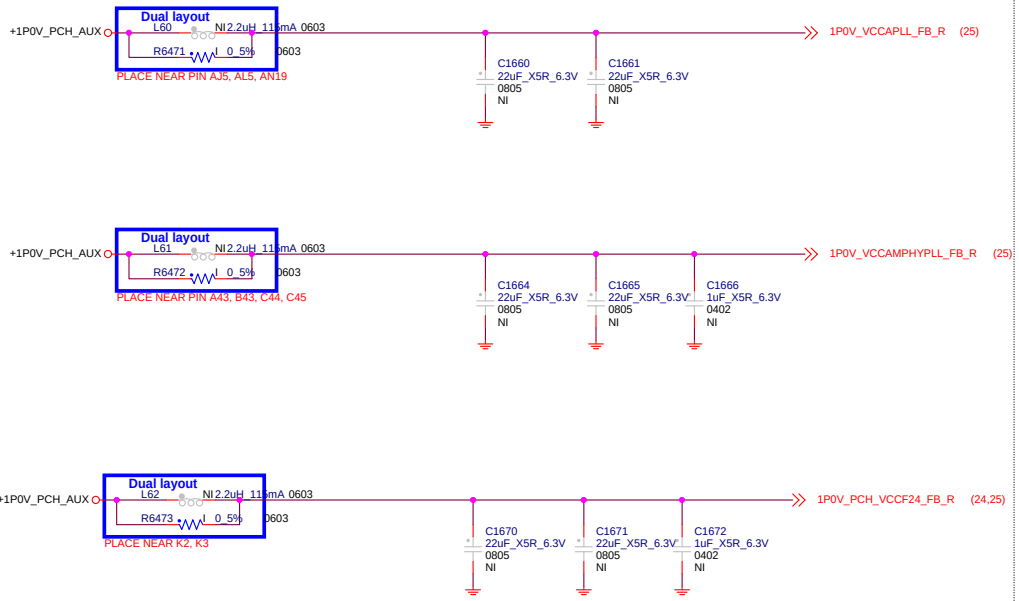
FILTER

SKYLAKE Decoupling & filter

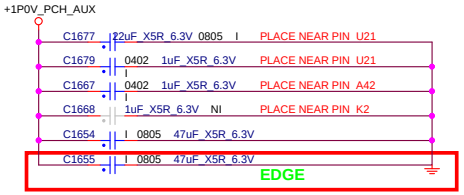


Power Plane Isolation

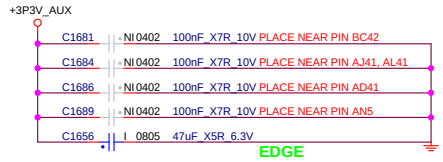
Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

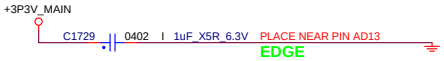
V1.0A



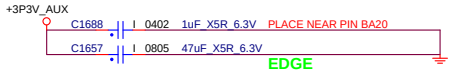
V1.8A / V3.3A



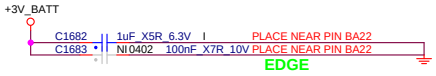
V1.8A / V1.8S / V3.3S



V3.3A

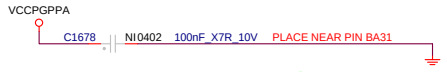


VCCRTC



V3.3 DSW

VccPGPPA



DELL INC.

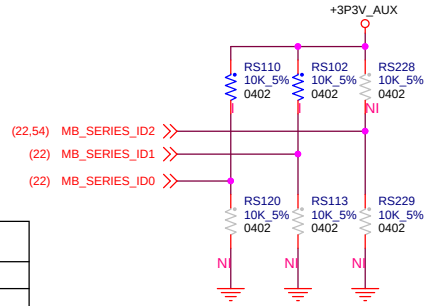
Title: PCH-PLL FILTER & DECOUPLING

DWG NO: GY SKL/ Farallon MT

Rev: A00

Date: Tuesday, July 07, 2015 Sheet 26 of 71

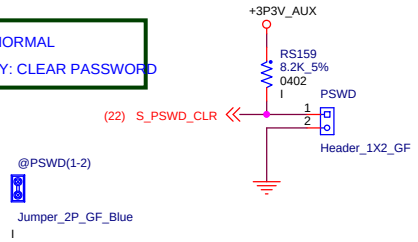
MB series ID



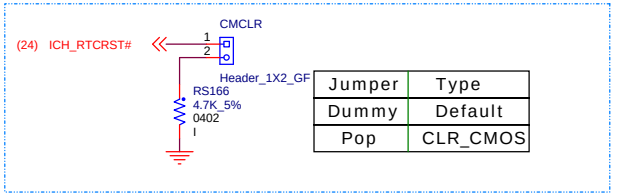
ID1	ID0	Type
0	0	SFF3
0	1	SFF7
1	0	SFF9
1	1	Farallon

Clear Password

1-2: NORMAL
EMPTY: CLEAR PASSWORD

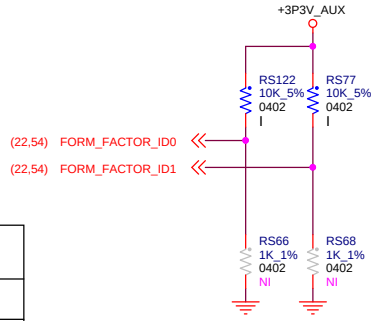


CLR_CMOS



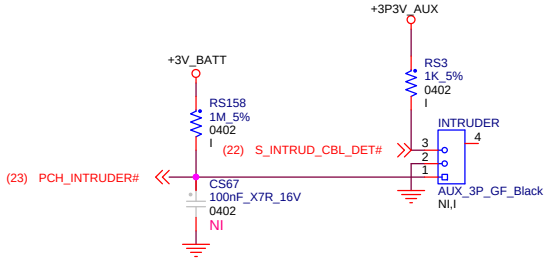
Jumper	Type
Dummy	Default
Pop	CLR_CMOS

Form Factor ID



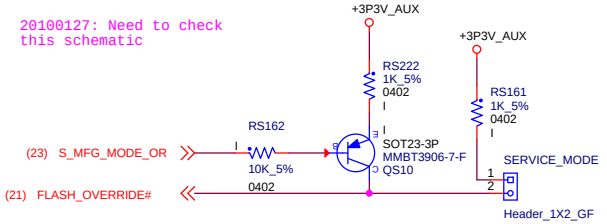
ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro

Chassis Intruder

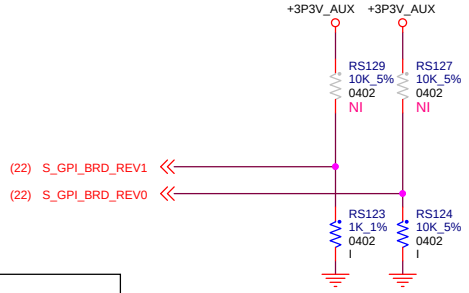


ME Disable (Flash overide)

20100127: Need to check this schematic



BOARD ID



ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00

BEEP

DELL INC.

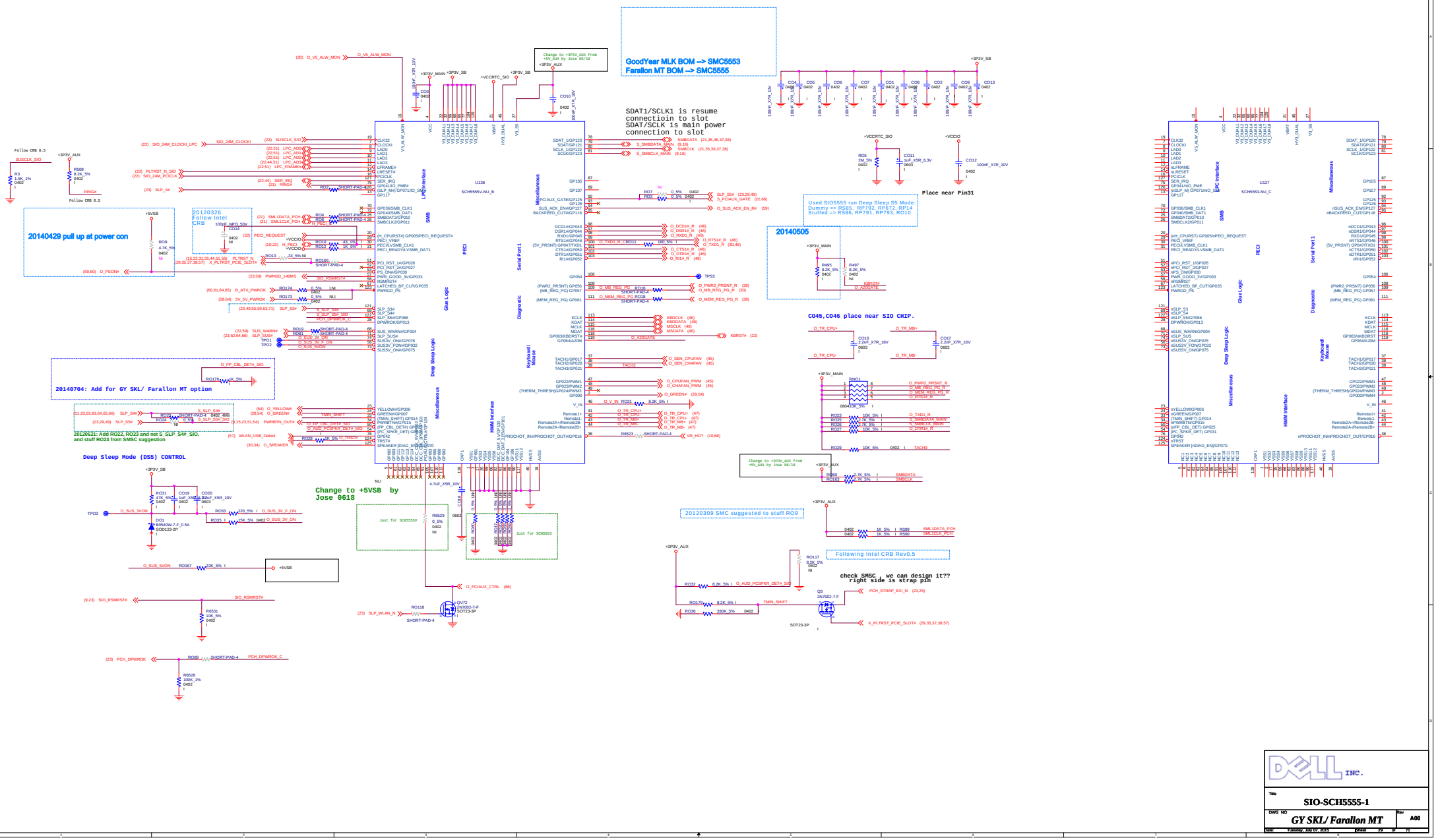
Title: **PCH-8:MISC CONN/BEEP/ID**

DWG NO: ***GY SKL/ Farallon MT***

Rev: **A00**

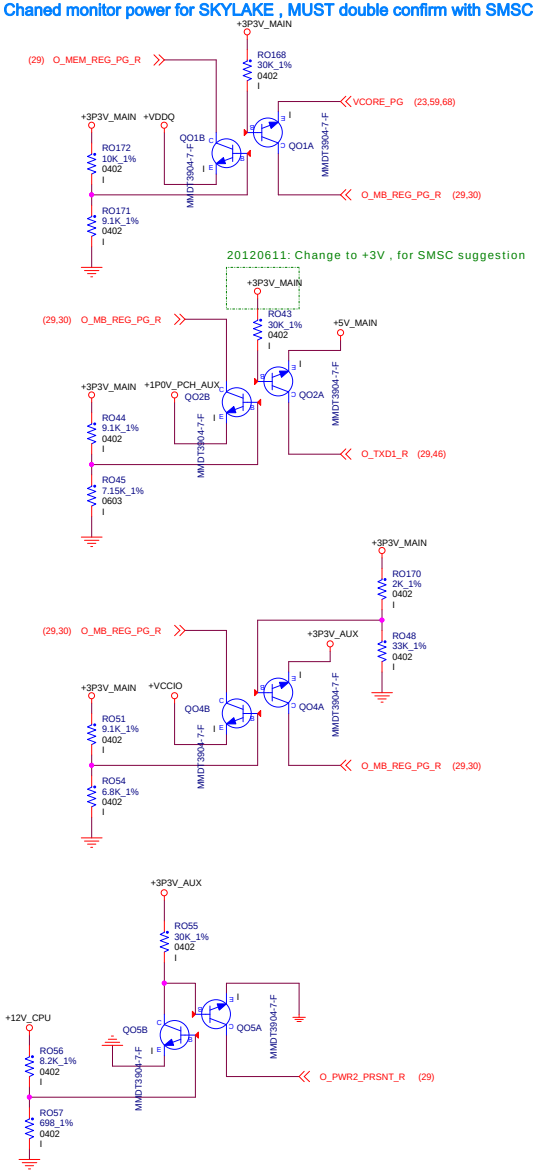
Date: Tuesday, July 07, 2015 Sheet 27 of 71

TBM	LABEL		
SYMS NO	GY SKL/ Farallon MT	Rev	A00
Date	Tuesday, July 07, 2015	Sheet	48 of 76

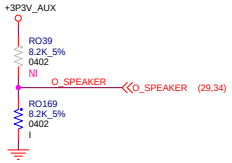

GoodYear MLK BOM --> SMC5553
Farallon MT BOM --> SMC5555
SDAT1/SCLK1 is resume connection to slot
SDAT/SCLK is main power connection to slot
Change to +3V_AUX from +5V_AUX by Jose 06/18
Change to +5VSB by Jose 0618
Used SIO5555 run Deep Sleep S5 Mode:
Dummy => RS85 , RP792, RP672, RP14
Stuffed => RS86, RP791, RP793, RO10
Place near Pin31
C045,C046 place near SIO CHIP.
20140429 pull up at power con
20140704: Add for GY SKL/ Farallon MT option
20120621: Add RO22, RO23 and net S_SLP_S4#_SIO, and stuff RO23 from SMSC suggestion
Deep Sleep Mode (DS5) CONTROL
20120309 SMC suggested to stuff RO9
Following Intel CRB Rev0.5
check SMSC we can design it?? right side is strap pin
Just for SCH5555
Just for SCH5553
SCH5555V-NU_B
SCH5553-NU_C
LPC Interface
SMB
PECI
Serial Port1
Miscellaneous
Glue Logic
Deep Sleep Logic
Diagnostic
Keyboard/ Mouse
HWM Interface
SIO-SCH5555-1
GY SKL/ Farallon MT
A00
Tuesday, July 07, 2015

5555 PRE-POST DIAG Monitor

20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC



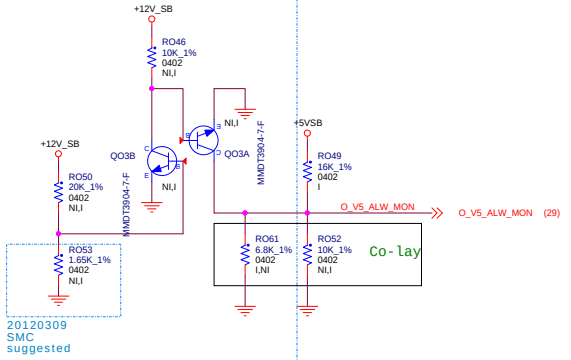
SIO STRAPING



SIO_STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

SIO5555 V5_ALW Monitor



For single Power ONLY

DELL INC.

Title: SIO-SCH5555-2

DWG NO: GY SKL/ Farallon MT

Rev: A00

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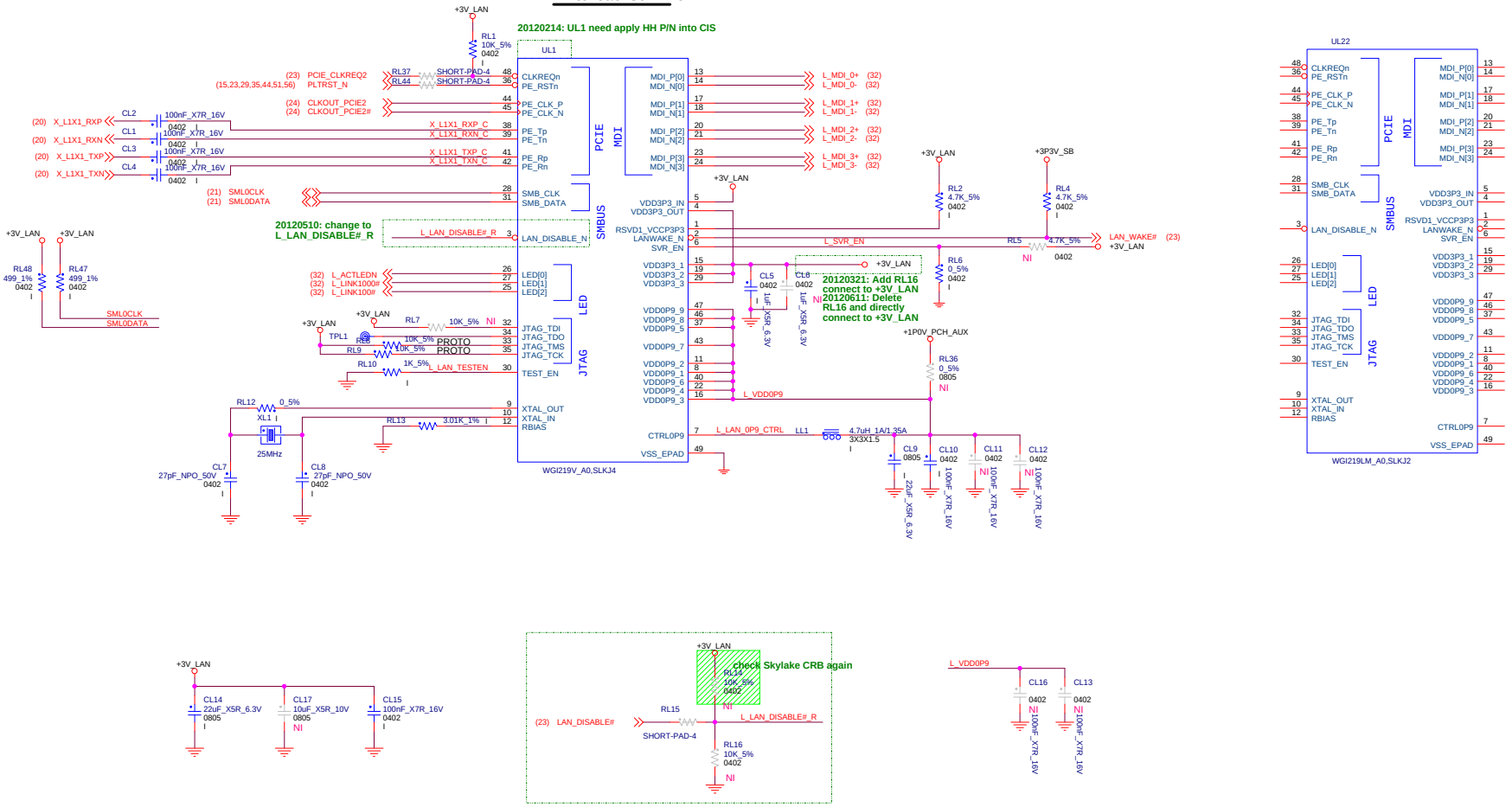
Jacksonville need applied CIS.

Intel Jacksonville



Title	LAN:Intel Clarkville
DWG NO	GY SKL/ Farallon MT
Rev	A00
Date:	Tuesday, July 07, 2015
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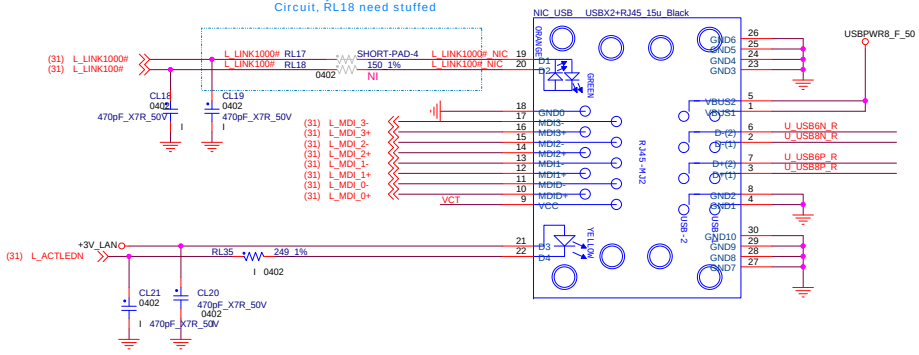
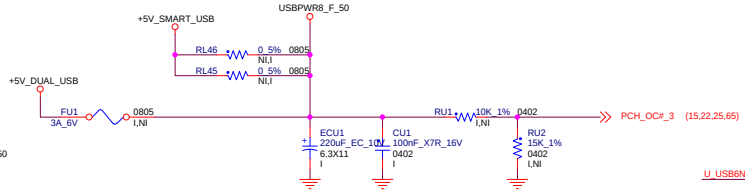
REAR LAN + USB
Ports 12 & 13

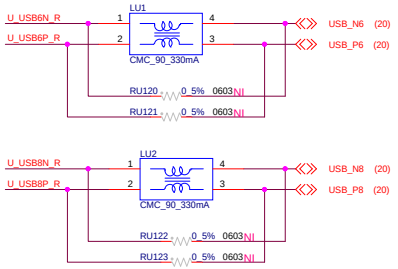
LED's:
10MHz : OFF
100MHz: Yellow
1GHz : Green

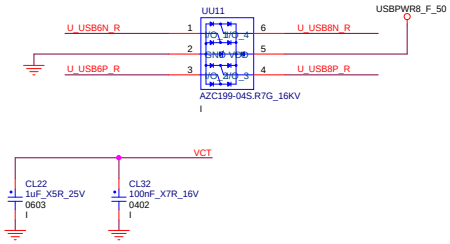
20120528: Dummy RL18

if Dummy LAN LED Control Circuit, RL18 need stuffed

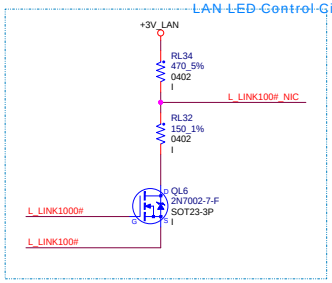




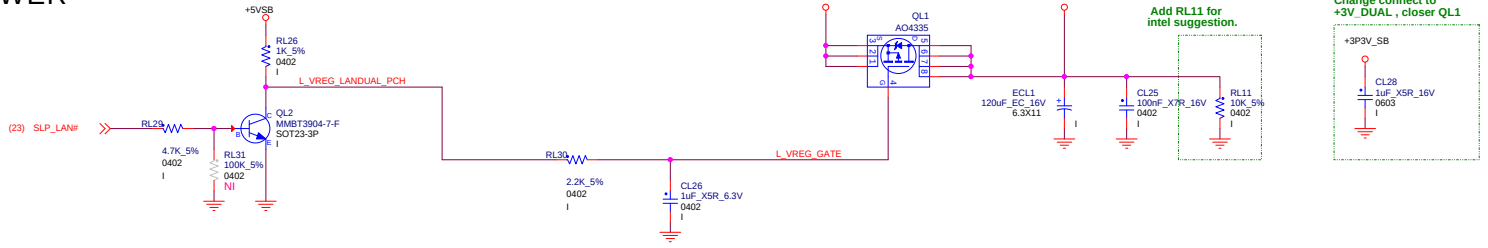




LAN LED Control Circuit



LAN POWER



DELL INC.

Title: **LAN Power & LAN/USB Conn**

DWG NO: ***GY SKL/ Farallon MT***

Rev: **A00**

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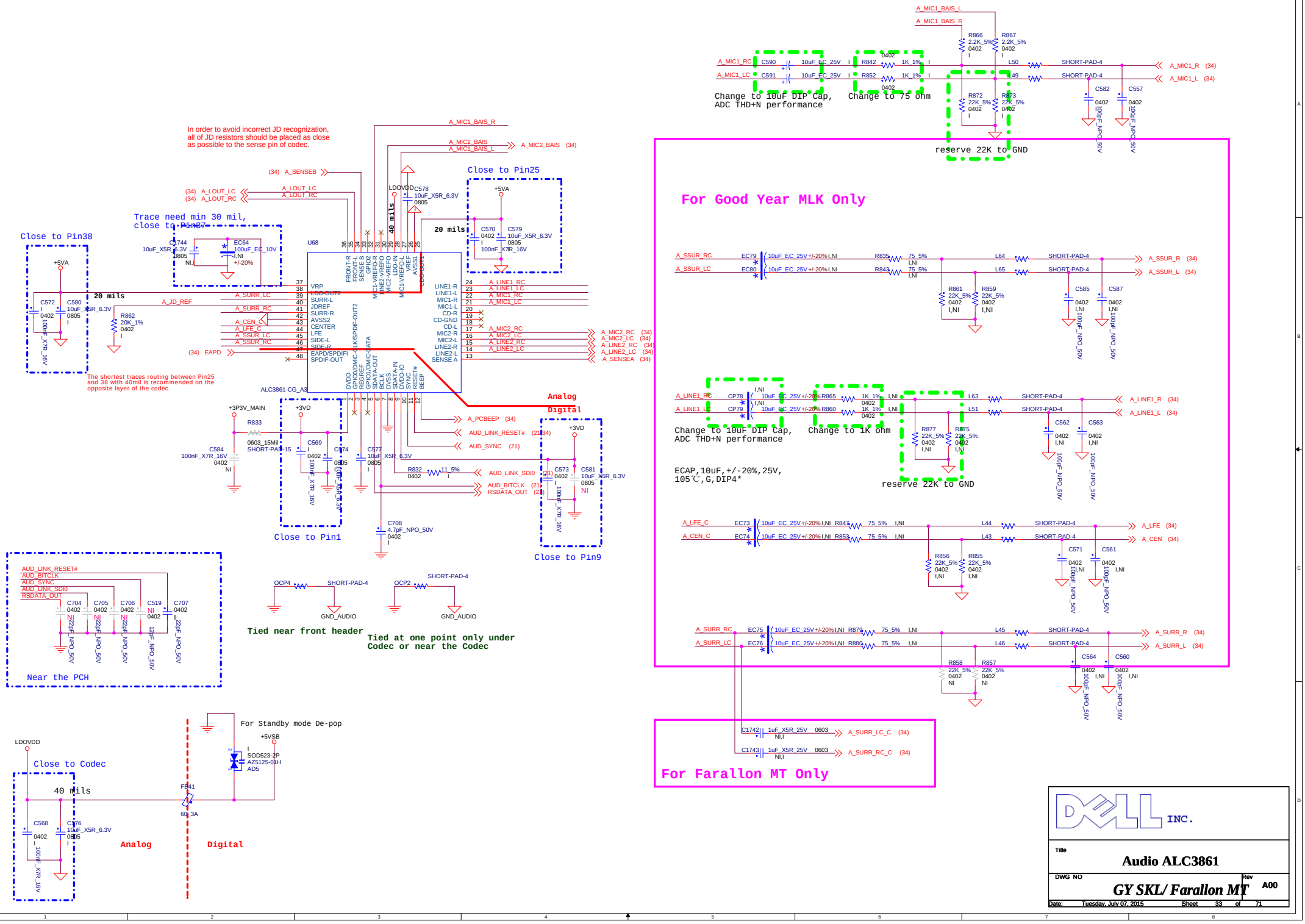

Title	Audio ALC3861
DWG NO	GY SKL/ Farallon MT
Rev	A00
Date:	Tuesday, July 07, 2015
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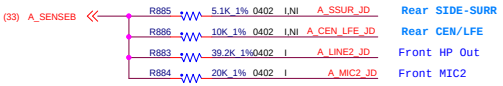
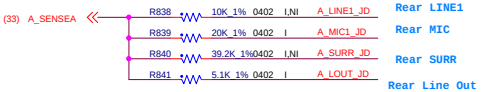
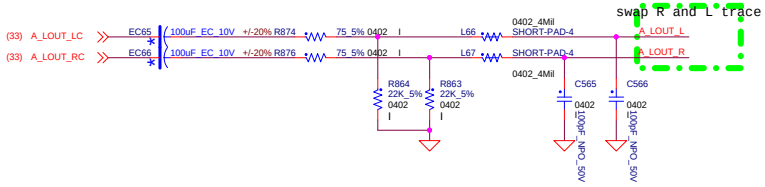
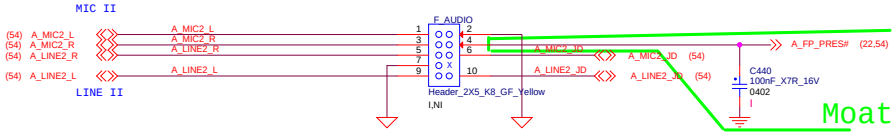
JACK SENSE

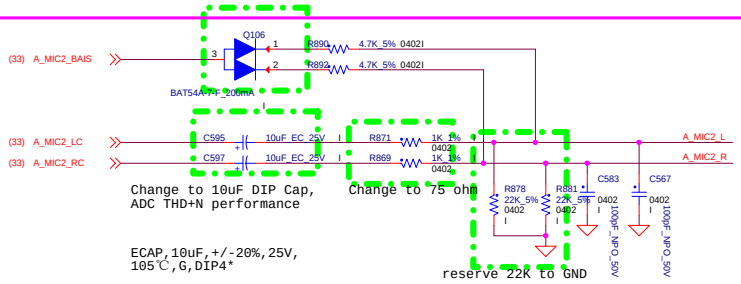


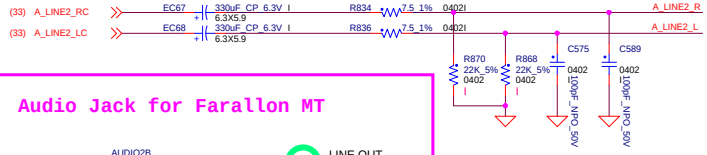




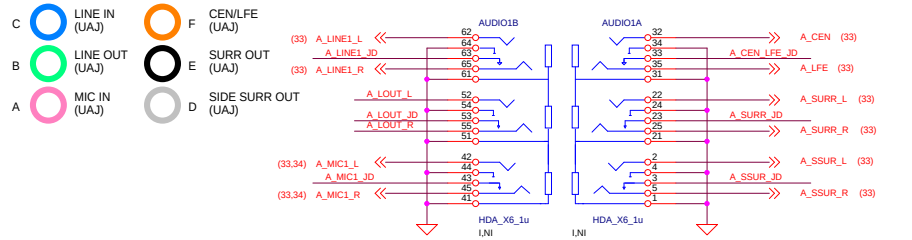
Front_Audio for Good Year SKL



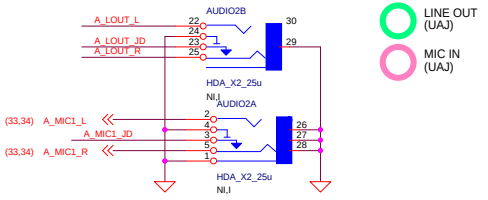




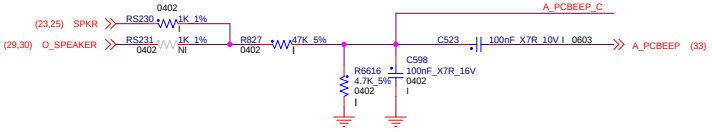
Audio Jack for GOODYEAR SKL



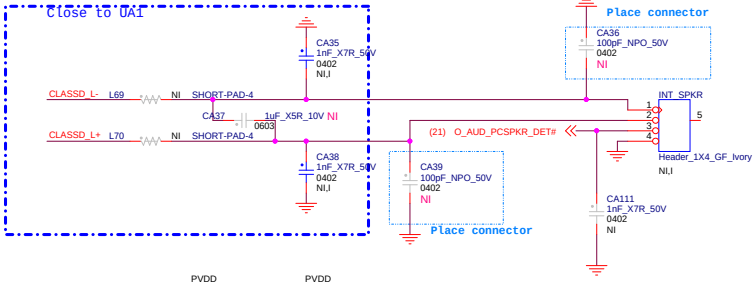
Audio Jack for Farallon MT

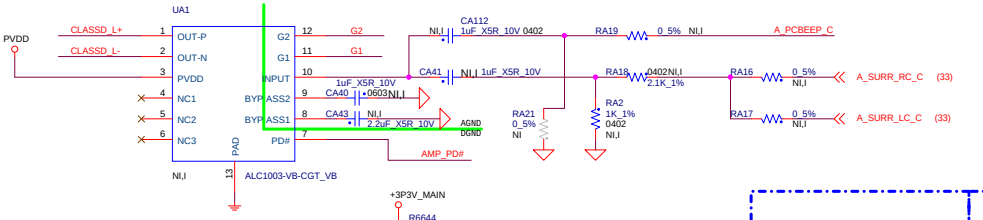


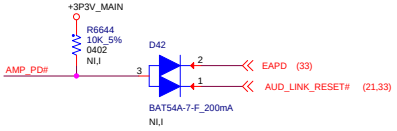
PC BEEP

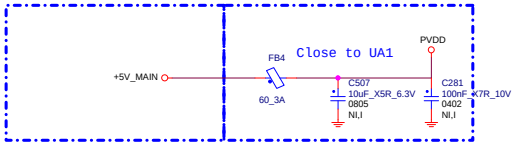


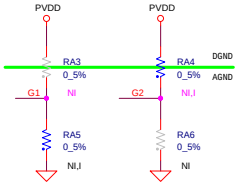
CHASSIS SPEAKER for Farallon MT











DELL INC.

Title: **Audio Conn**

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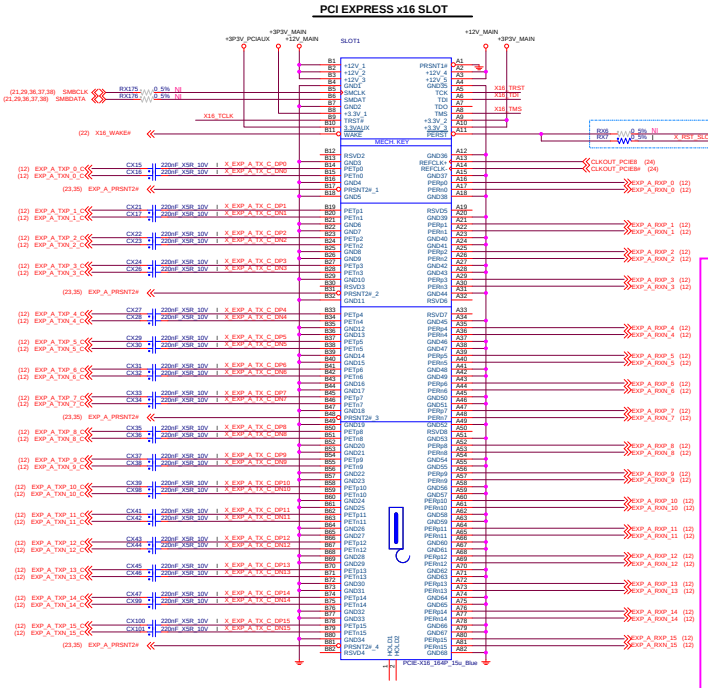
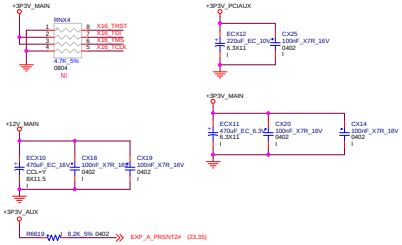
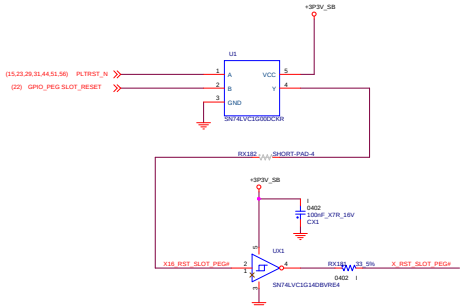
PCI EXPRESS x16 SLOT





PCIE RESET LOGIC CIRCUIT

Used PCH GPIO13 PCIE RESET Mode.
Stuffed => RX12, RX20, RS225



Title	PCIe 16X
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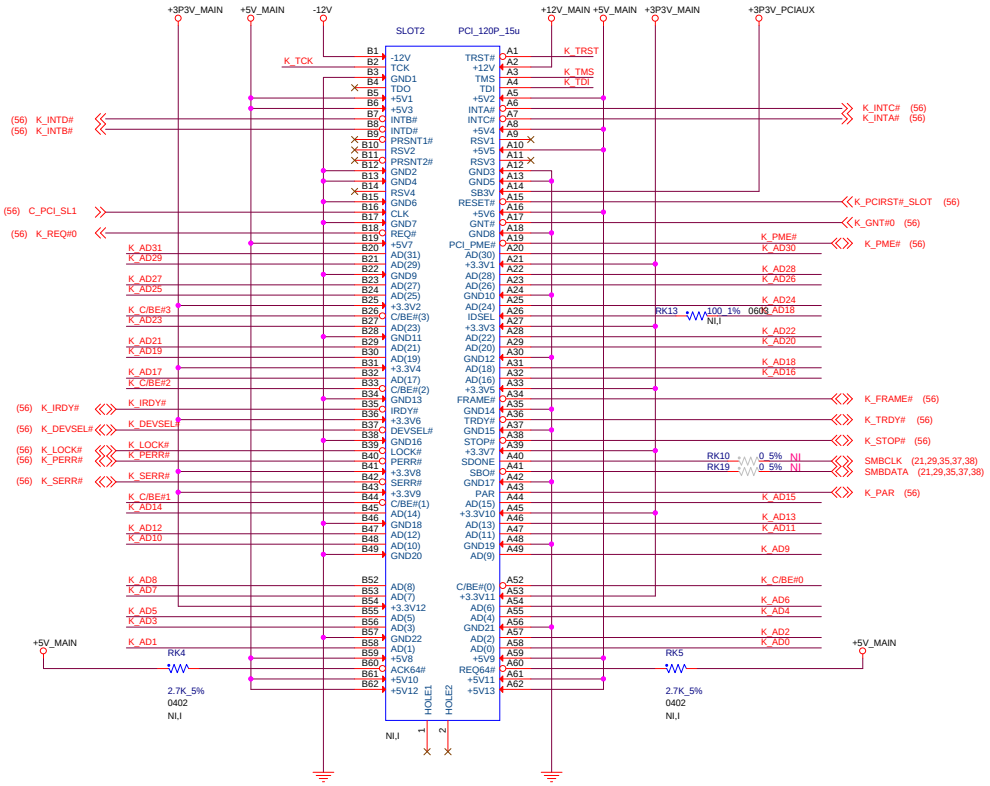

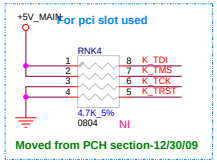

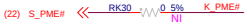

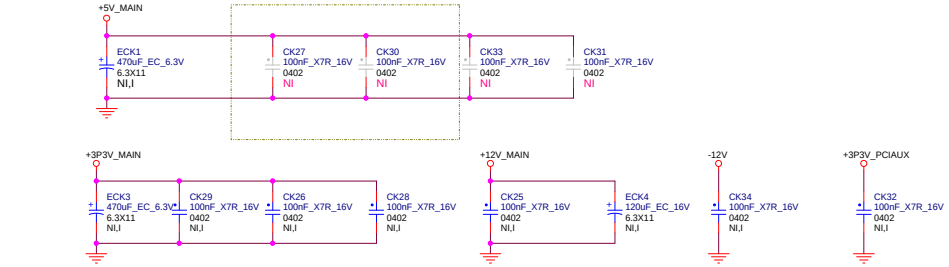

DELL INC.

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Slot2 PCI

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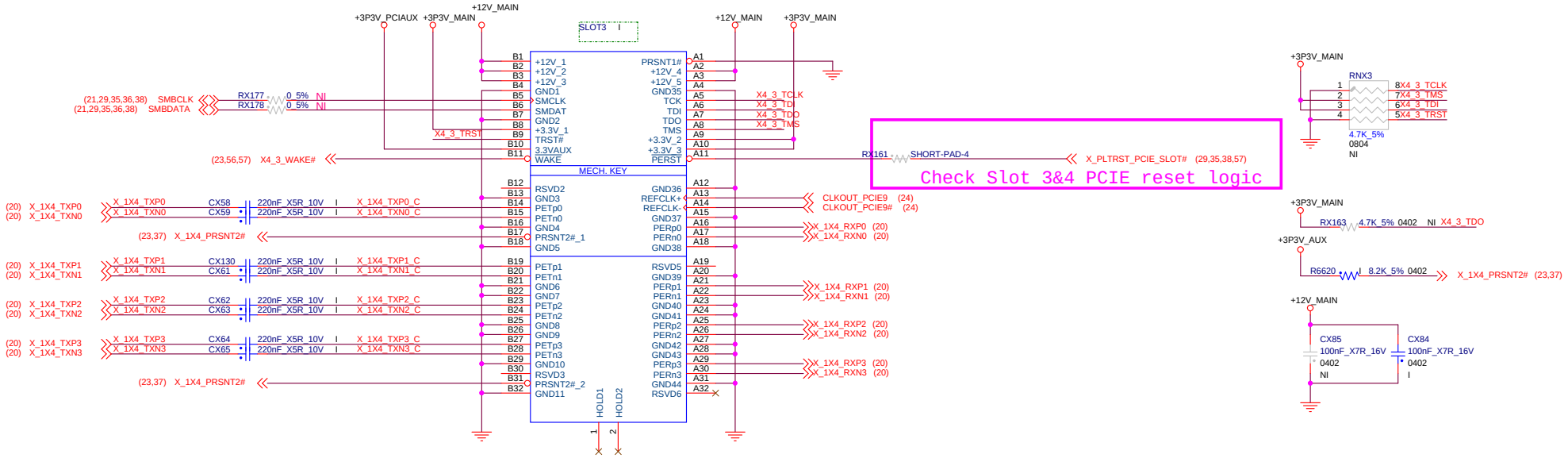
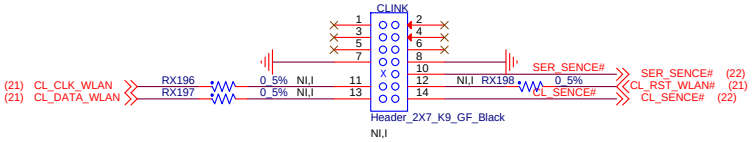
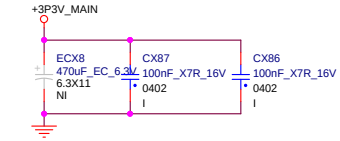
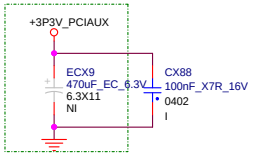
20120315: SLOT1 change to 15u" parts
FOXCONN_2EG03217-22DB-DF









20120409: Dummy ECX4

DELL INC.

Title
PCIe 4x

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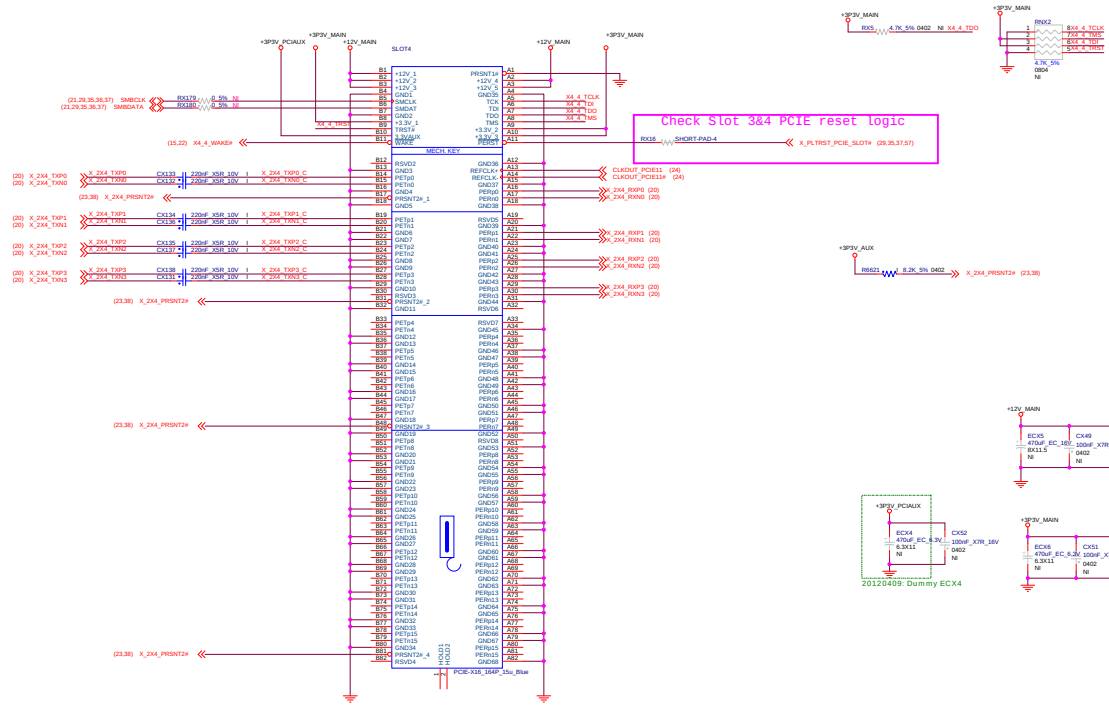

Title	Slot4 PCIE 4x SLOT
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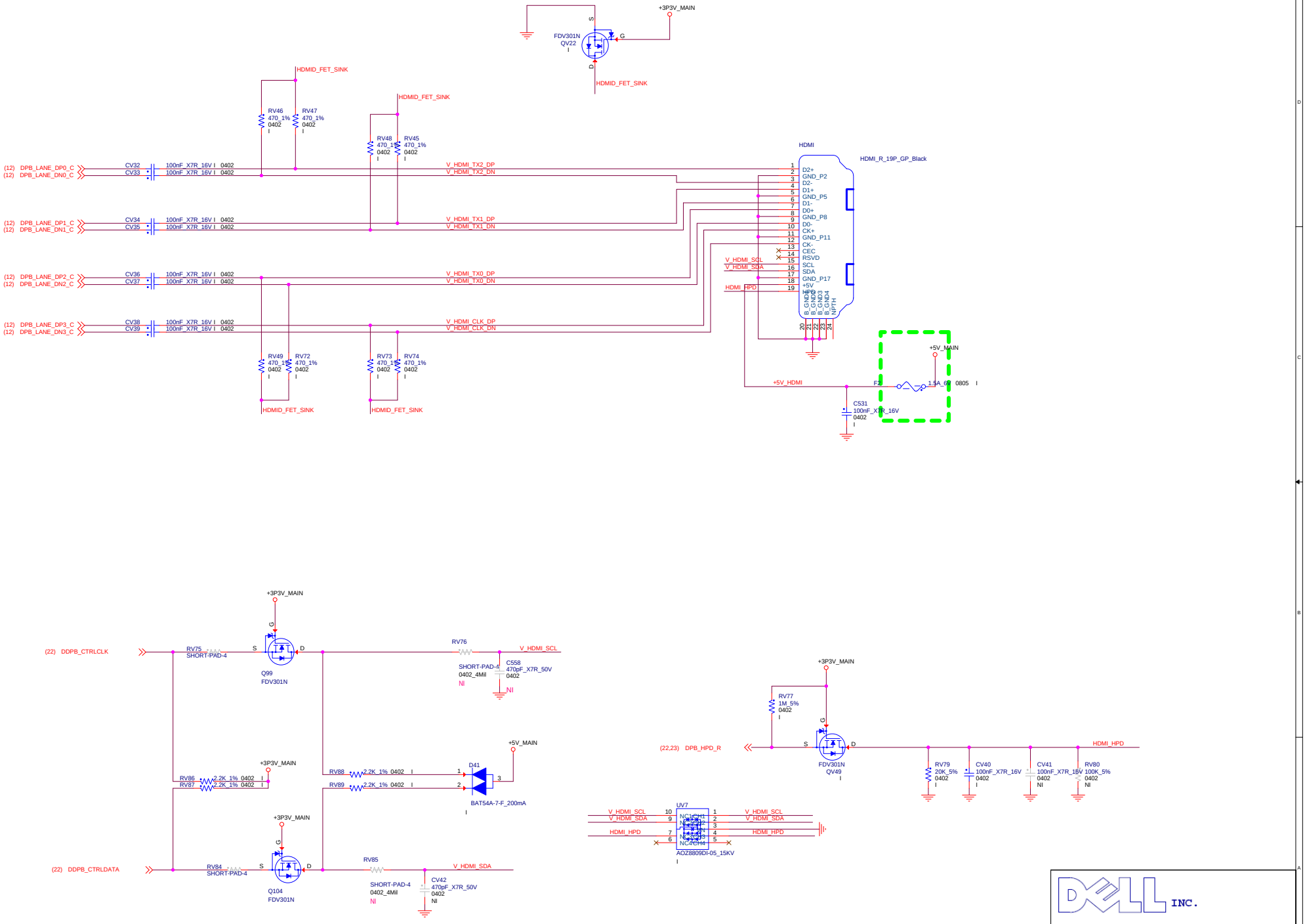

Title	HDMI
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20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC

UV1 AOZ8809DI-05_15KV

(12) DPC_LANE_DP0_C — CV2 100nF_X7R_16V 0402 NI,I — DPC_LANE_DP0 — 10 NC1/CH1 — 1 — DPC_LANE_DP0
(12) DPC_LANE_DN0_C — CV6 100nF_X7R_16V 0402 NI,I — DPC_LANE_DN0 — 9 NC2/CH2 — 2 — DPC_LANE_DN0
(12) DPC_LANE_DP1_C — CV4 100nF_X7R_16V 0402 NI,I — DPC_LANE_DP1 — 7 VN — 3
(12) DPC_LANE_DN1_C — CV5 100nF_X7R_16V 0402 NI,I — DPC_LANE_DN1 — 6 NC3/CH3 — 4 — DPC_LANE_DP1
NC4/CH4 — 5 — DPC_LANE_DN1

UV2 AOZ8809DI-05_15KV

(12) DPC_LANE_DP2_C — CV6 100nF_X7R_16V 0402 NI,I — DPC_LANE_DP2 — 10 NC1/CH1 — 1 — DPC_LANE_DP2
(12) DPC_LANE_DN2_C — CV7 100nF_X7R_16V 0402 NI,I — DPC_LANE_DN2 — 9 NC2/CH2 — 2 — DPC_LANE_DN2
(12) DPC_LANE_DP3_C — CV8 100nF_X7R_16V 0402 NI,I — DPC_LANE_DP3 — 7 VN — 3
(12) DPC_LANE_DN3_C — CV9 100nF_X7R_16V 0402 NI,I — DPC_LANE_DN3 — 6 NC3/CH3 — 4 — DPC_LANE_DP3
NC4/CH4 — 5 — DPC_LANE_DN3

UV3 AOZ8809DI-05_15KV

DPC_AUX_DN — 10 NC1/CH1 — 1 — DPC_AUX_DN
DPC_AUX_DP — 9 NC2/CH2 — 2 — DPC_AUX_DP
3
DPC_HPD — 7 VN — 4 — DPC_HPD
DPC_P13 — 6 NC3/CH3 — 5 — DPC_P13
NC4/CH4

(12) DPC_AUX_DN_C — CV10 100nF_X7R_16V 0402 NI,I — V_DDSP_C_AUX_DN_C
(12) DPC_AUX_DP_C — CV11 100nF_X7R_16V 0402 NI,I — V_DDSP_C_AUX_DP_C

DP_PORT2 DP

DPC_LANE_DP0 — 1 ML_LANE_0P
2 GND
DPC_LANE_DN0 — 3 ML_LANE_0N
DPC_LANE_DP1 — 4 ML_LANE_1P
5 GND
DPC_LANE_DN1 — 6 ML_LANE_1N
DPC_LANE_DP2 — 7 ML_LANE_2P
8 GND
DPC_LANE_DN2 — 9 ML_LANE_2N
DPC_LANE_DP3 — 10 ML_LANE_3P
11 GND
DPC_LANE_DN3 — 12 ML_LANE_3N
DPC_P13 — 13 CONFIG1
DPC_P14 — 14 CONFIG2
DPC_AUX_DP — 15 AUX_CH_P
16 GND
DPC_AUX_DN — 17 AUX_CH_N
DPC_HPD — 18 HP_DET
19 PWR_RTN
V_DPC_PWR — 20 DP_PWR
NI,I — 24 — 23 — 22 — 21 — DISPLAYPORT_15u_Black

RV3 1M_5% 0402 NI,I
RV4 100K_5% 0402 NI,I

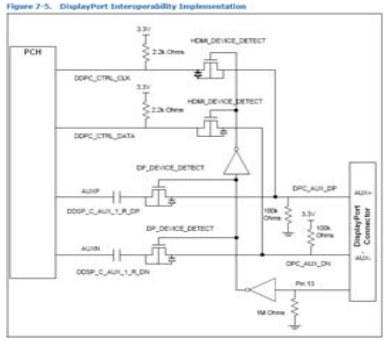
+3P3V_MAIN — FV1 NI,I 1.5A_6V_0805 — V_DPC_PWR
CV12 1uF_X5R_16V 0603 NI,I
CV13 10uF_X5R_10V 0805 NI
CV14 470pF_X7R_50V 0402 NI,I
CV15 22uF_X5R_6.3V 0805 NI,I

+3P3V_MAIN +3P3V_MAIN
RV7 2.2K_5% 0402 NI,I
RV8 2.2K_5% 0402 NI,I
(22) DDPC_CTRLCLK — DDPC_CTRLCLK
(22) DDPC_CTRLDATA — DDPC_CTRLDATA

DDPC_CTRLCLK — DPC_P13_POS — Q107A 2N7002DWA-7 SOT363-6P NI,I — DPC_AUX_DP
DPC_AUX_DN — DPC_P13_POS — Q107B 2N7002DWA-7 SOT363-6P NI,I — DDPC_CTRLDATA

DPC_AUX_DP — DPC_P13_INV — Q108A 2N7002DWA-7 SOT363-6P NI,I — V_DDSP_C_AUX_DP_C
DPC_AUX_DN — DPC_P13_INV — Q108B 2N7002DWA-7 SOT363-6P NI,I — V_DDSP_C_AUX_DN_C

Figure 2-5. DisplayPort Interoperability Implementation



Display Port Hotplug Detect

+5V_MAIN
RV12 1K_5% 0402 NI
DPC_HPD
+5V_MAIN
FDV301N QV5 NI,I
RV19 100K_5% 0402 NI,I
DPC_HPD_R (22)

+3P3V_MAIN +3P3V_AUX +3P3V_MAIN
RV13 100K_1% 0402 NI,I
RV14 100K_1% 0402 NI
RV15 100K_1% 0402 NI,I
DPC_AUX_DN
DPC_AUX_DP
RV21 100K_1% 0402 NI
RV22 100K_1% 0402 NI,I

+12V_MAIN
RV11 4.7K_5% 0402 NI,I
+5V_MAIN
RV16 4.7K_5% 0402 NI
DPC_P13
RV18
RV20 1M_5% 0402 NI,I
8.2K_5% 0402 NI,I
DPC_P13_INV
QV38A 2N7002DWA-7 SOT363-6P
CV16 100nF_X7R_16V 0402 NI,I
QV38B SOT363-6P 2N7002DWA-7
20110211:change 2N7002DW for cost down.
+12V_MAIN
RV17 8.2K_5% 0402 NI,I
DPC_P13_POS
Change location name.

DELL INC.

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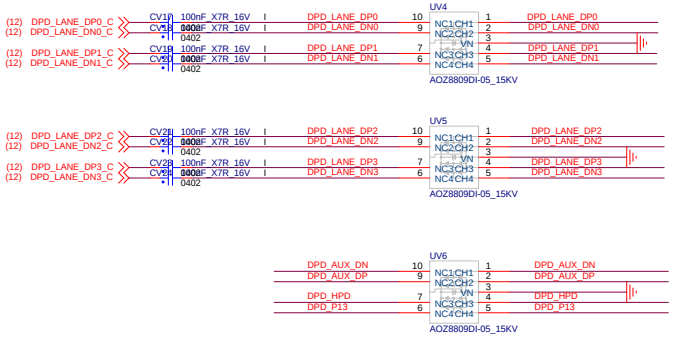
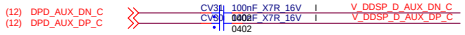
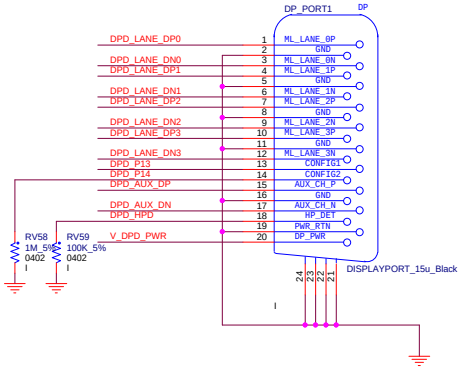
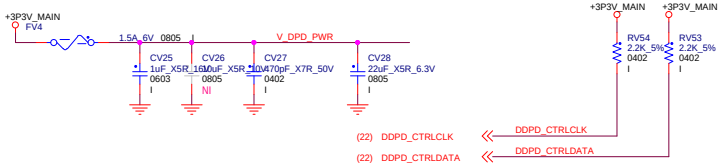
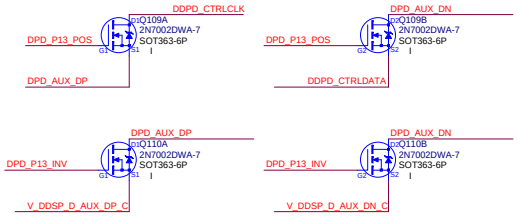
20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC

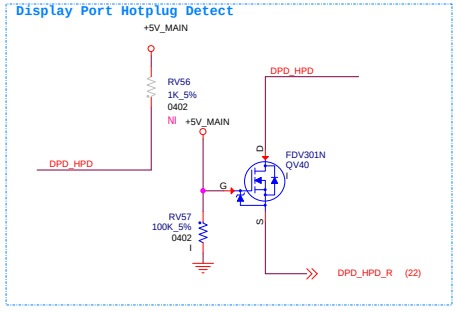


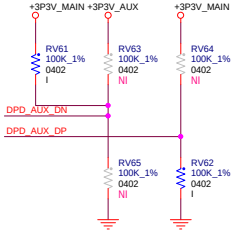


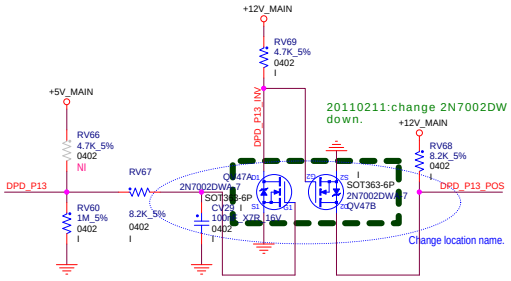












Title	Display Port 2		
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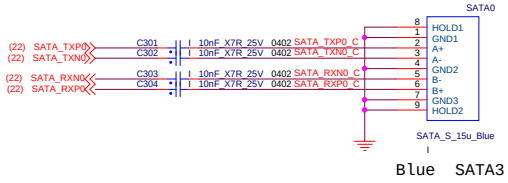
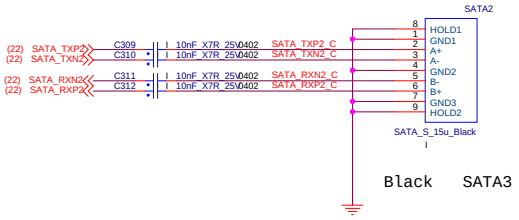
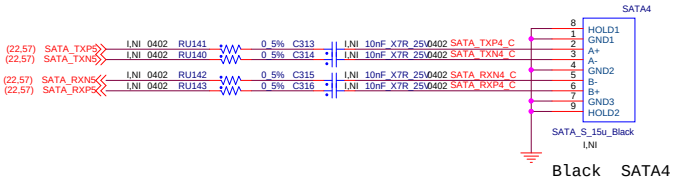
DARK BLUE



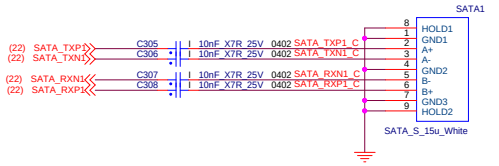
Blue SATA3



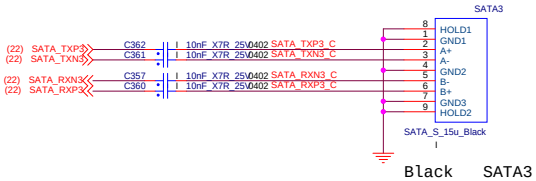
Black SATA3



Black SATA4



White SATA3



Black SATA3

INC.

Title

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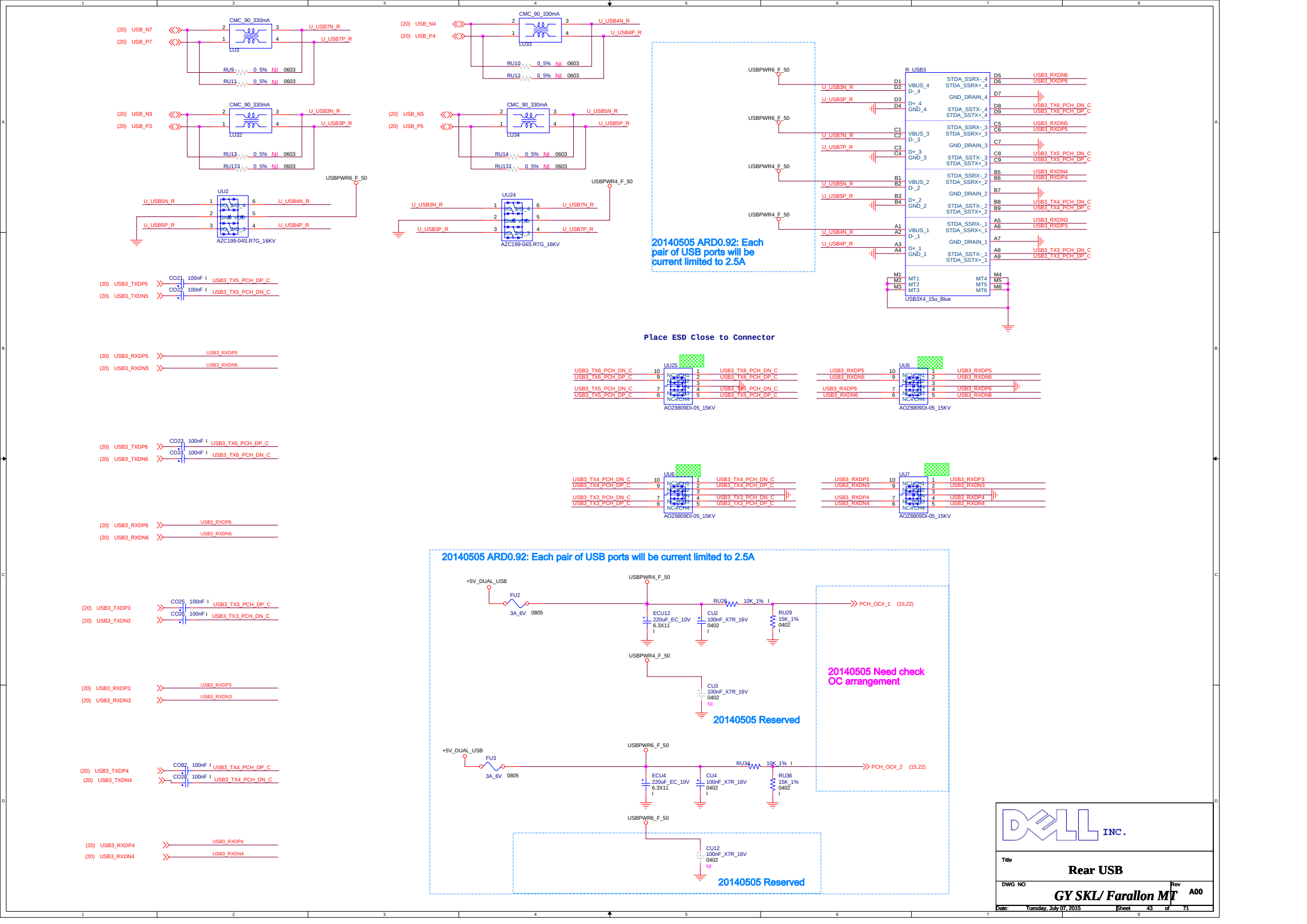
CMC_90_330mA
U_USB7N_R
U_USB7P_R
U_USB4N_R
U_USB4P_R
U_USB3N_R
U_USB3P_R
U_USB5N_R
U_USB5P_R
USBPWR6_F_50
USBPWR4_F_50
R_USB3
USB3X4_15u_Blue
AZC199-04S.R7G_16KV
AOZ8809DI-05_15KV
20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A
Place ESD Close to Connector
20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A
+5V_DUAL_USB
PCH_OC#_1 (15,22)
PCH_OC#_2 (15,22)
20140505 Need check OC arrangement
20140505 Reserved
20140505 Reserved
INC.
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Rear USB
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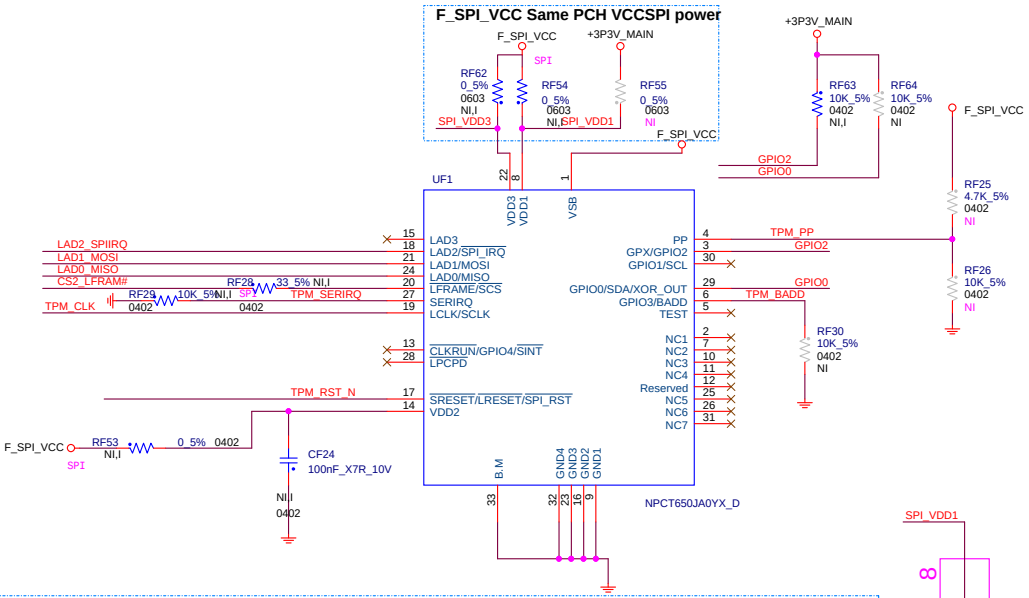
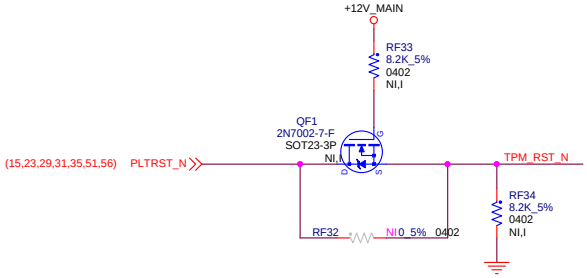
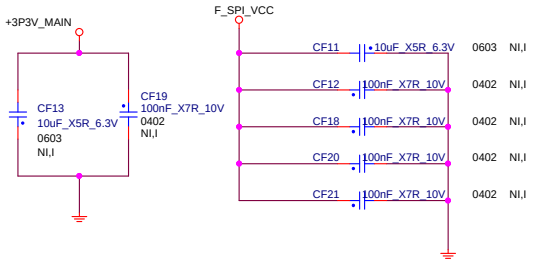
Nuvoton NPCT650JAAYX



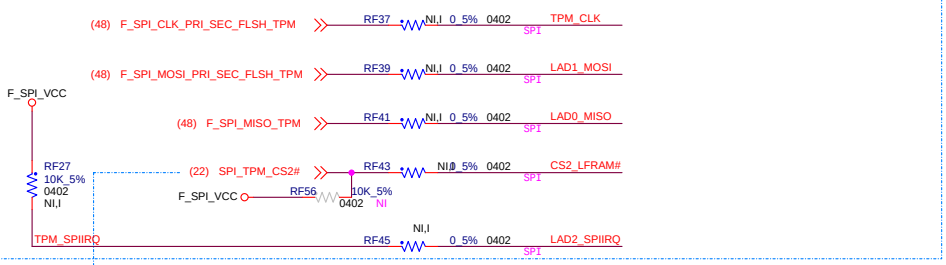
20140508 Follow Dell D serials design



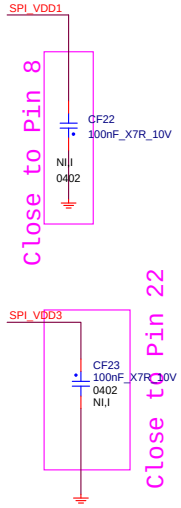
Decoupling Capacitors



20140515 Co-layout with LPC TPM



20140509 Changed net name to SPI__TPM__CS2#



NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

DELL INC.

Title: TPM

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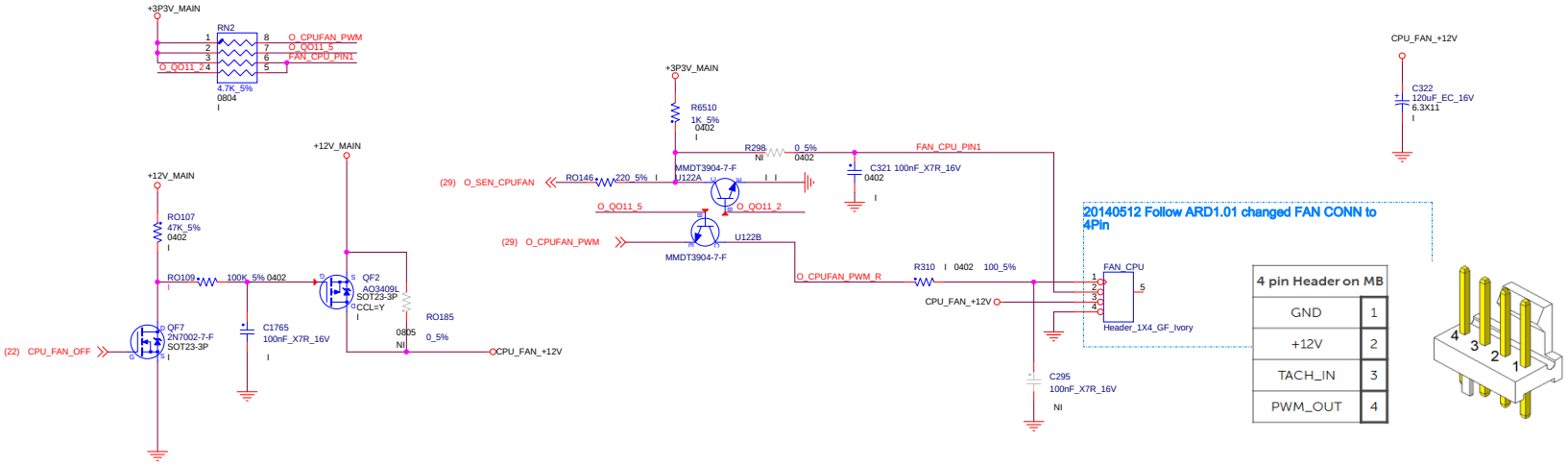
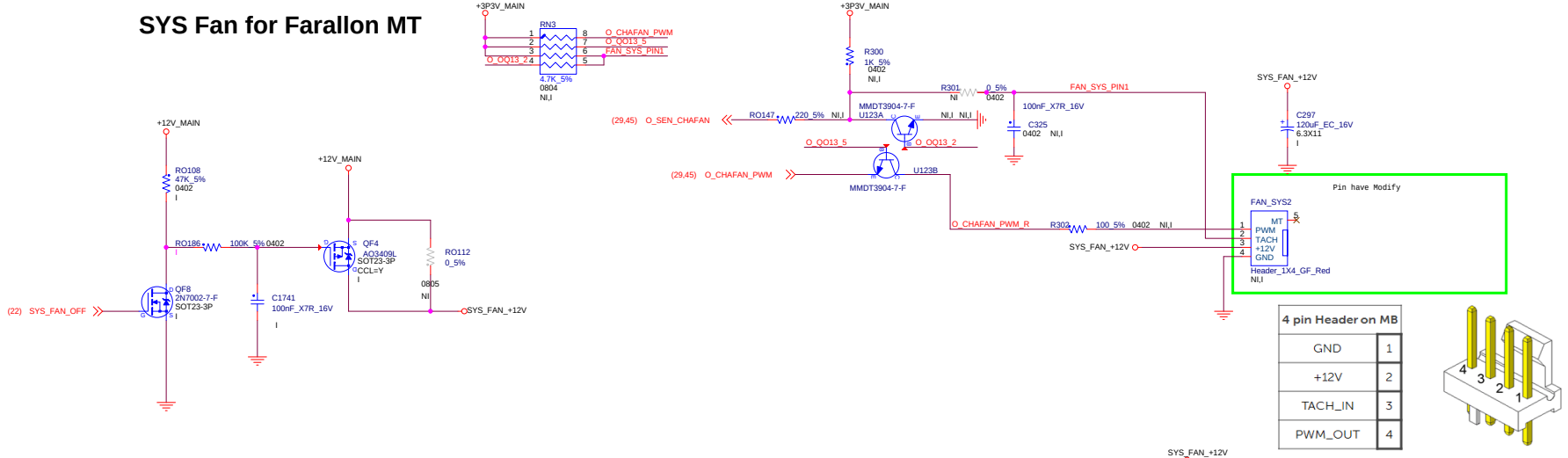
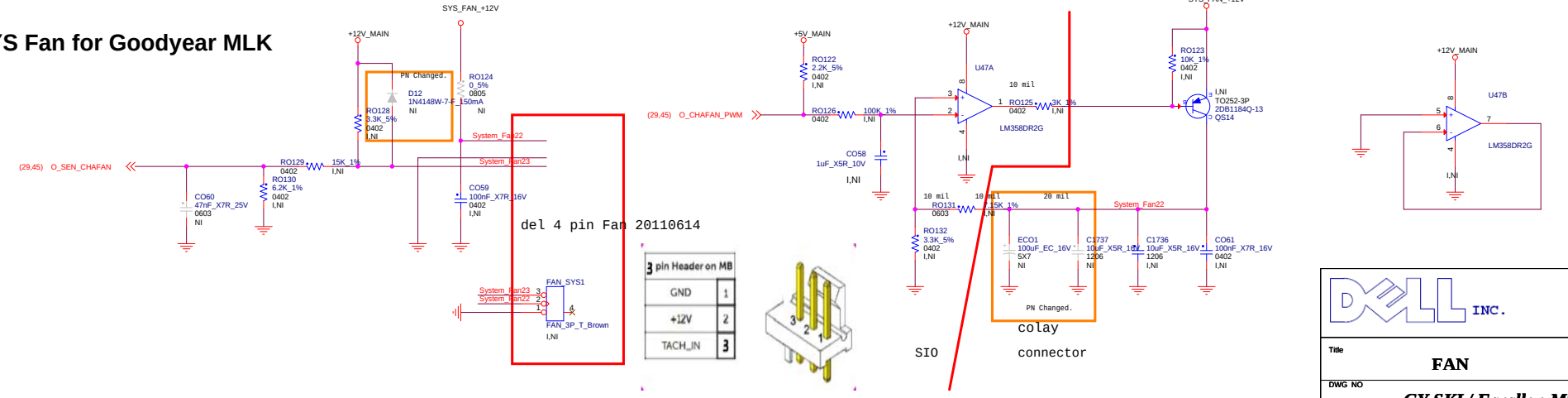
CPU Fan



SYS Fan for Farallon MT



SYS Fan for Goodyear MLK



Title	FAN
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SERIAL A

12V solution

U29
GD75232DBRE4

SERIAL B

RS232_GF_Teal

PS2 KEYBOARD / MOUSE

EMI SOLUTION

The +5V_PS2 power trace width must be 40 mils or greater

Change BOM option.

KYBD_MOUSE
PS2-KBMS-2_GF

AZC199-04S.R7G_16KV

Title	COM/PS2
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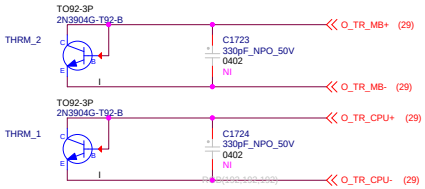
Thermal Header



Title	TBD
DWG NO	GY SKL/ Farallon MT
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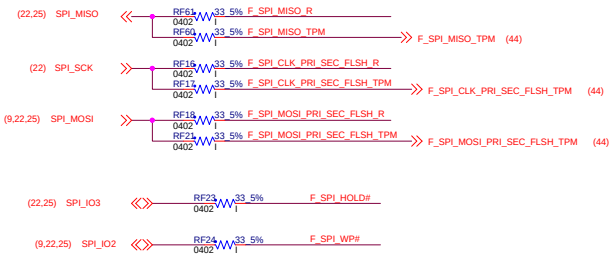
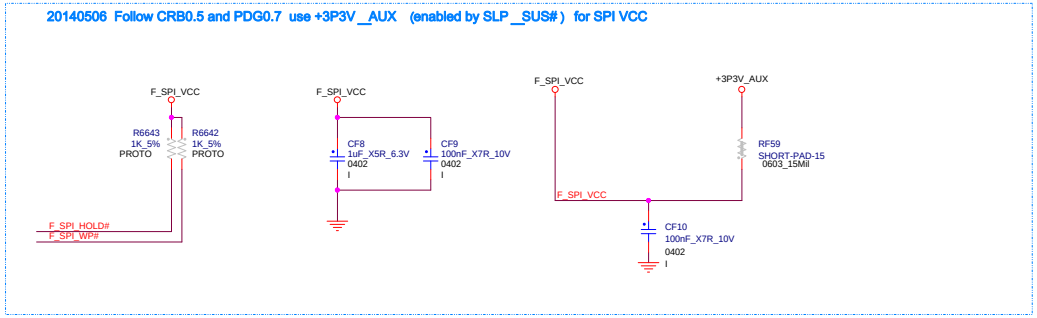
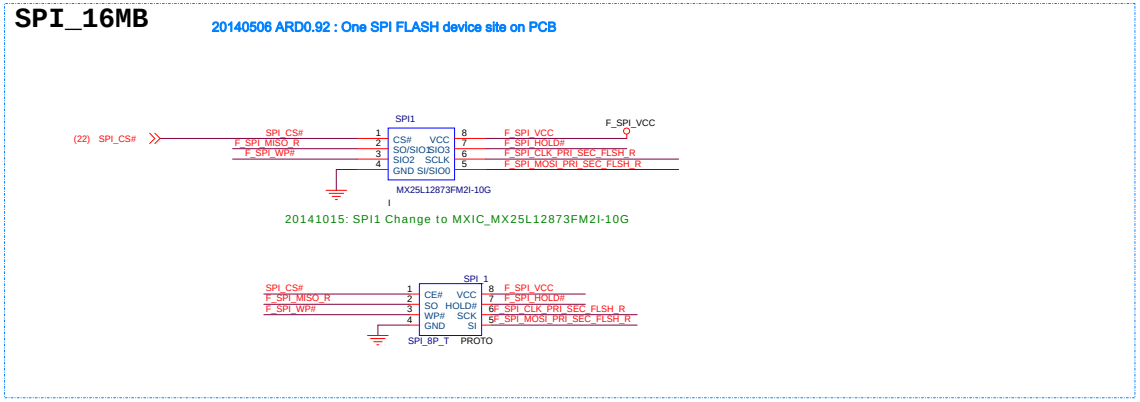
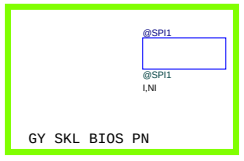
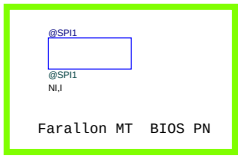










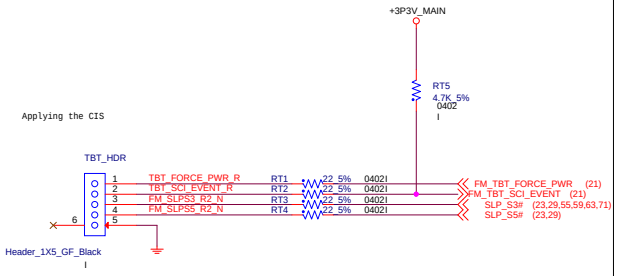
DELL INC.

Title: **SPI**

DWG NO: ***GY SKL/ Farallon MT*** Rev: **A00**

Date: Tuesday, July 07, 2015 Sheet 48 of 71

TBT



DELL INC.

Title

TBT_HDR

DWG NO

GY SKL/ Farallon MT

Rev A00

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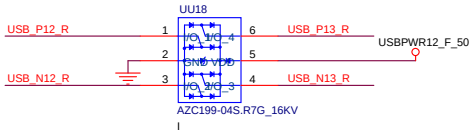
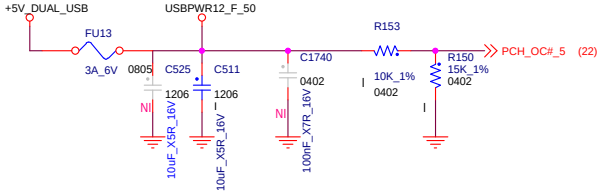
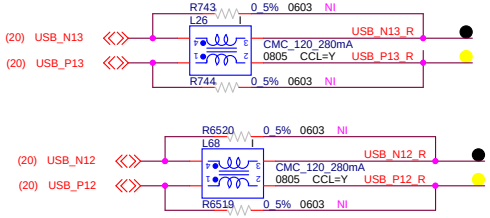


Place ESD Close to Header

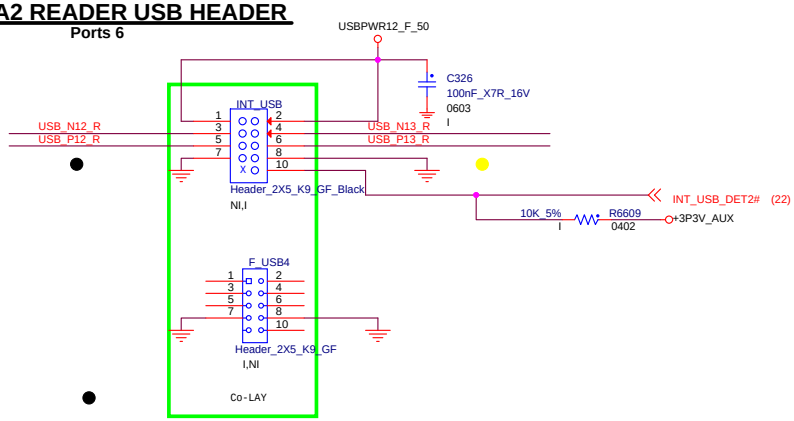
USB2.0





MEDIA2 READER USB HEADER

Ports 6



GY SKL F_USB4 Card reader Black color

DELL INC.

Title: **BLANK**

DWG NO: ***GY SKL/ Farallon MT***

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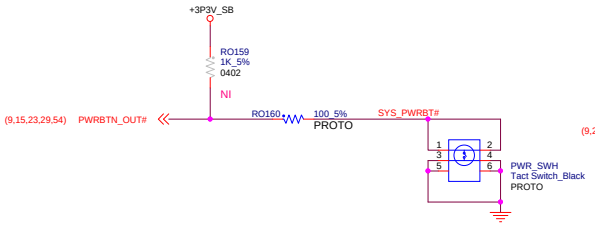
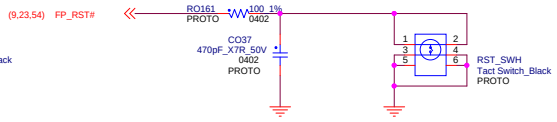
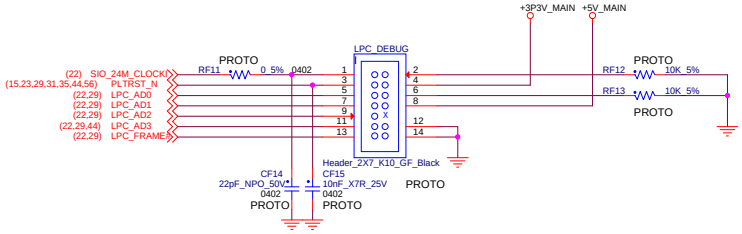
Power Bottom

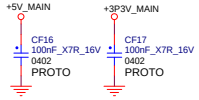


Reset Bottom



LPC DEBUG





APS Debug

Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RTCRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

DELL INC.

Title: **Pilot Run Conn**

DWG NO: *GY SKL/ Farallon MT* Rev: A00

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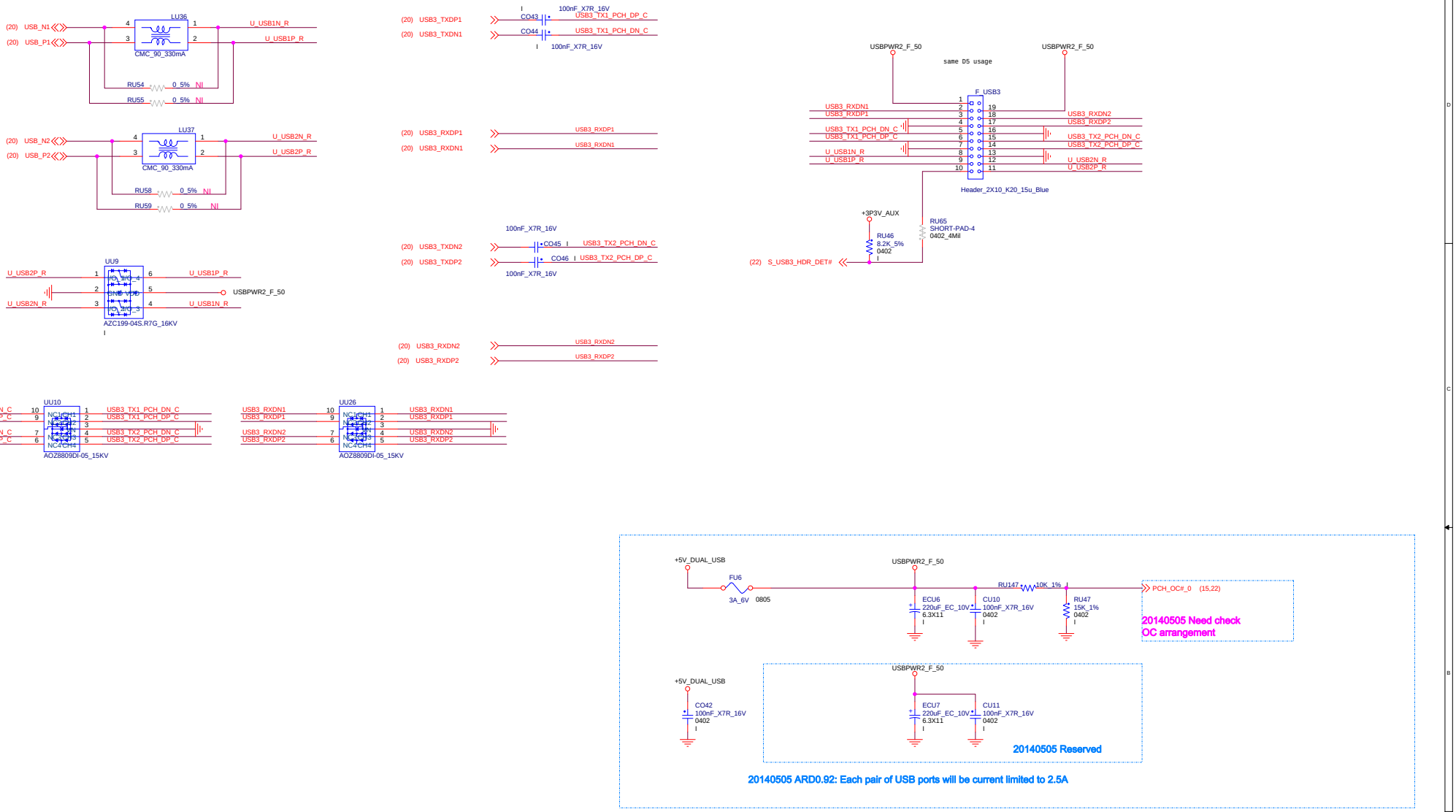

DELL INC.

Title: **BLANK**

DWG NO: *GY SKL/ Farallon MT*

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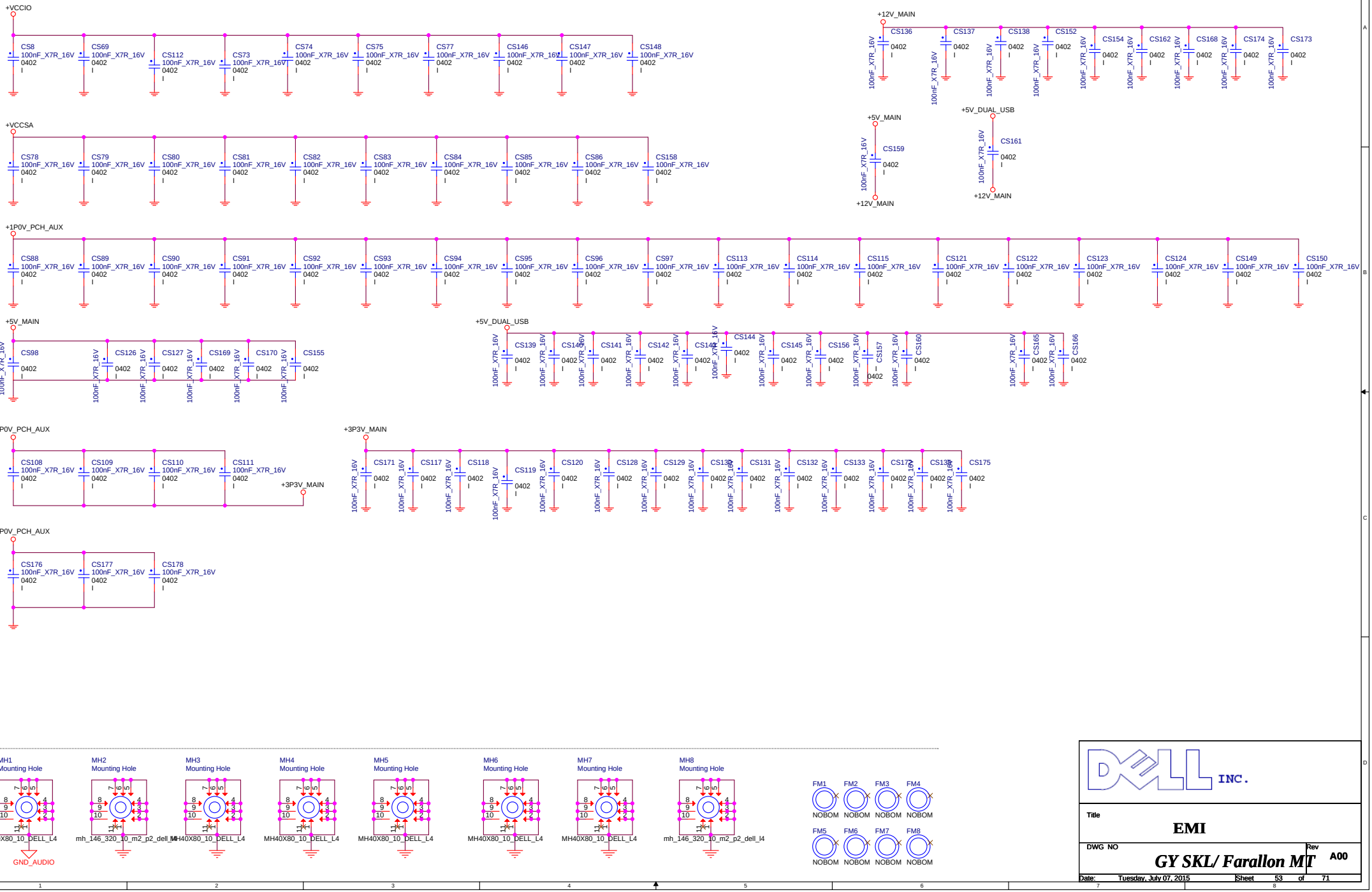
EMI CAP



DELL INC.

Title: EMI

DWG NO: GY SKL/ Farallon MT

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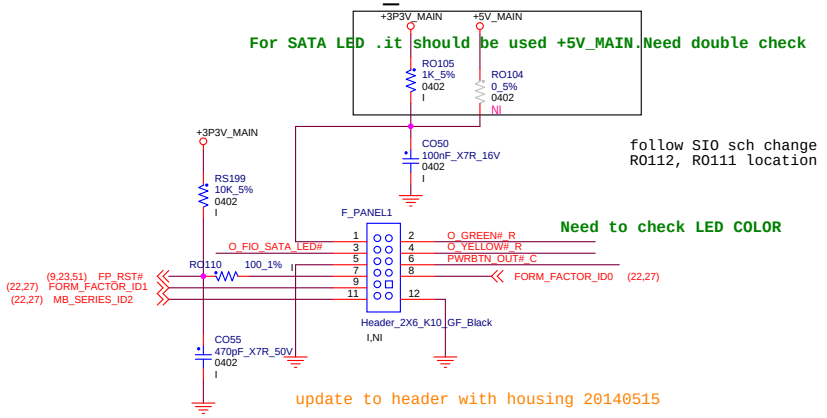
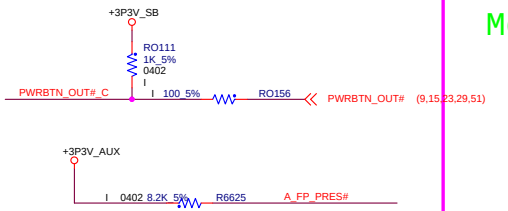
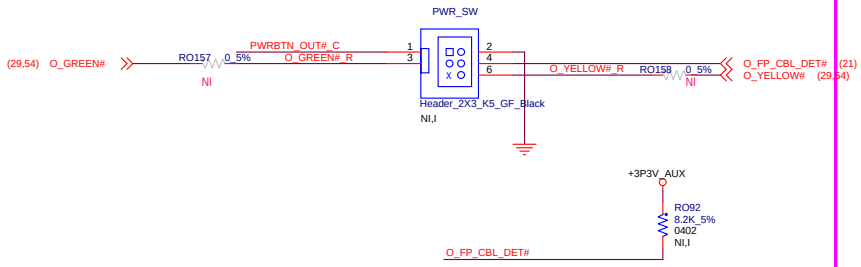
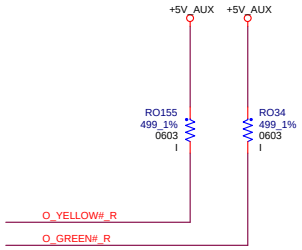
GOODYEAR SKL Front_IO Header



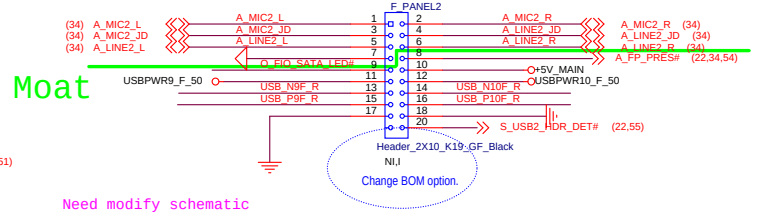


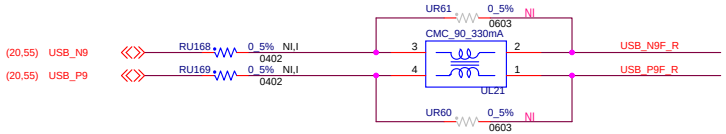
FARALLON MT POWER SWITCH Header

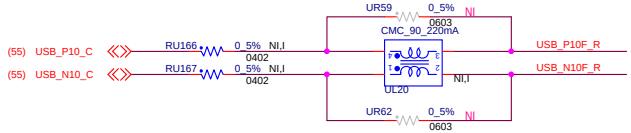


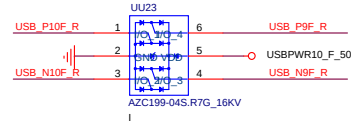


FARALLON MT Front_IO Header







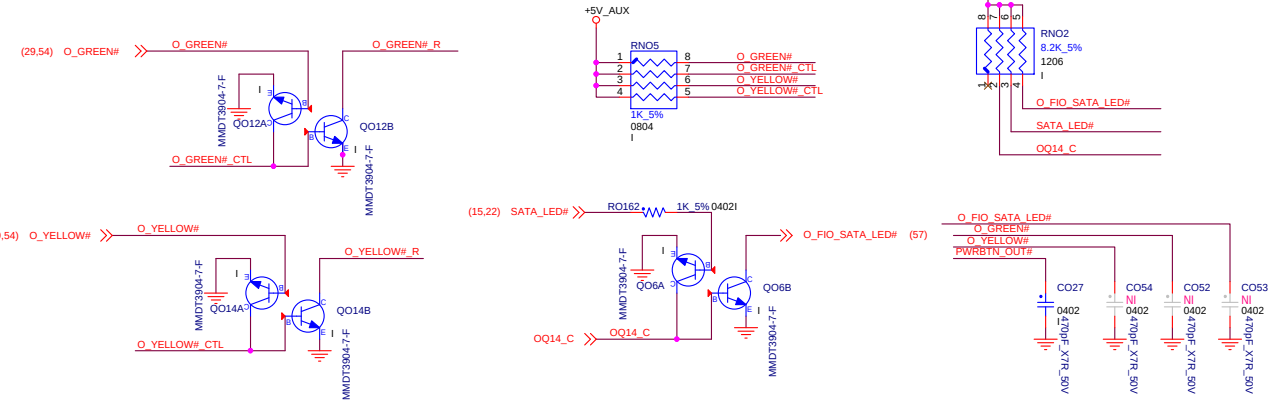


YELLOW TOP_USB

20120521: Add QO12, QO14, RN04, RO84, RO86 for Power LED control

If stuffed RO84, RO86 ; Dummy QO12, QO14, RN04

Pitch 2.0mm



DELL INC.

Title: **Front Panel**

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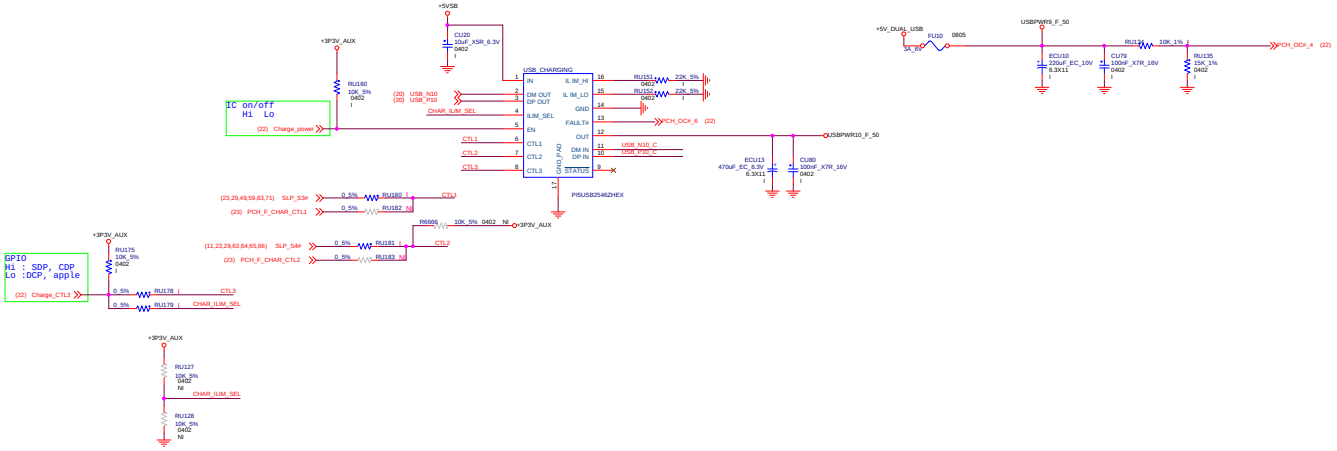
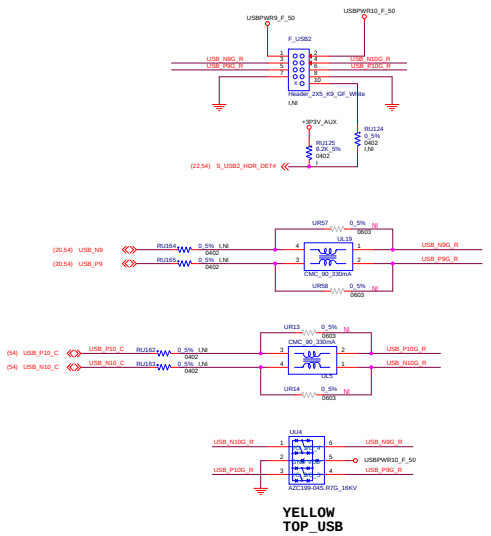
INT USB



Goodyear SKL Front USB

GY SKL F_USB2 Top IO White color



YELLOW
TOP_USB

Title	Front USB
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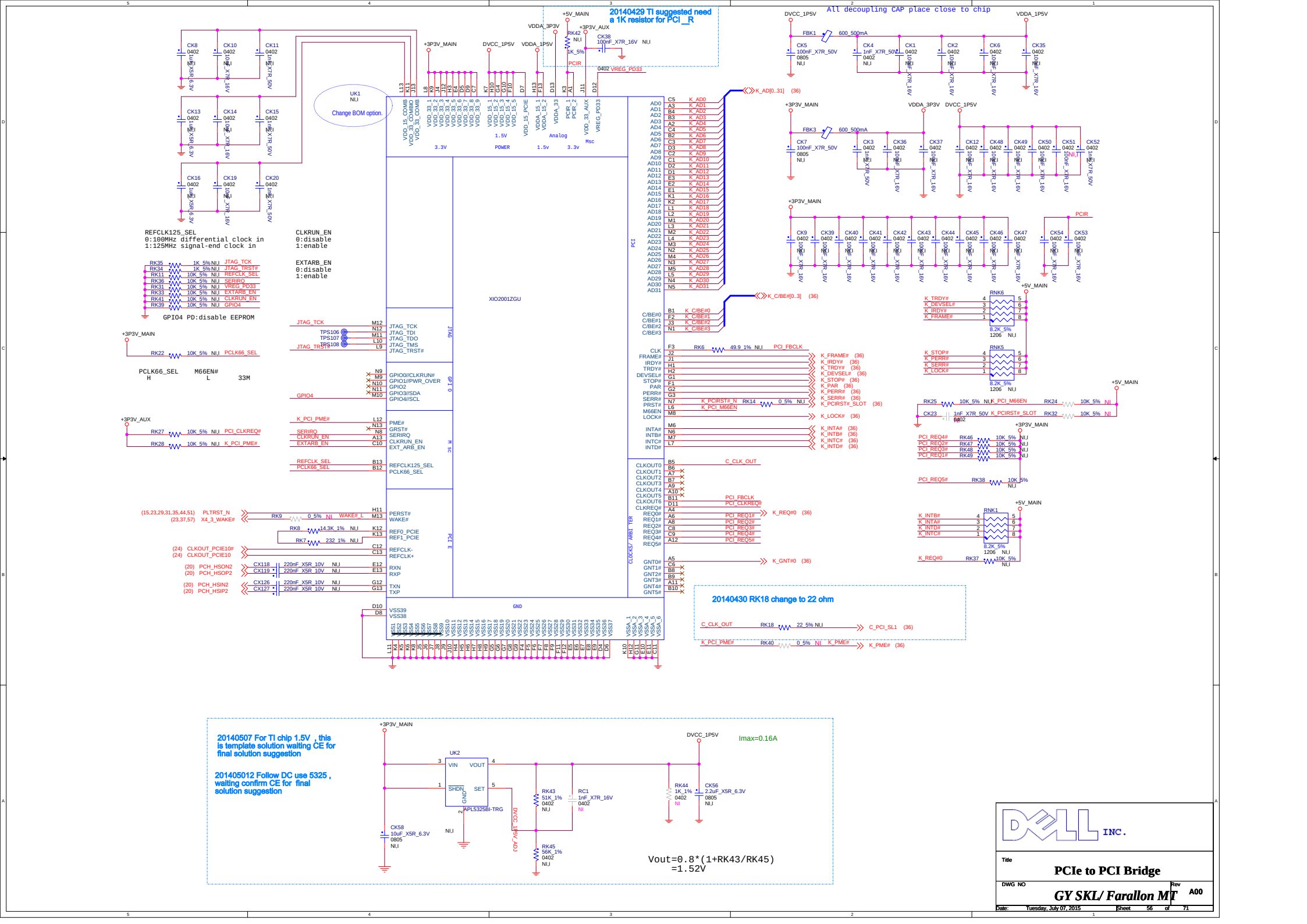
20140429 TI suggested need a 1K resistor for PCI_R
All decoupling CAP place close to chip
XIO2001ZGU
UK1
Change BOM option.
REFCLK125_SEL
0:100MHz differential clock in
1:125MHz signal-end clock in
CLKRUN_EN
0:disable
1:enable
EXTARB_EN
0:disable
1:enable
GPIO4 PD:disable EEPROM
PCLK66_SEL M66EN# 33M
H L
20140430 RK18 change to 22 ohm
20140507 For TI chip 1.5V , this is template solution waiting CE for final solution suggestion
201405012 Follow DC use 5325 , waiting confirm CE for final solution suggestion
Imax=0.16A
Vout=0.8*(1+RK43/RK45)
=1.52V
DELL INC.
Title
PCIe to PCI Bridge
DWG NO
GY SKL/ Farallon MT
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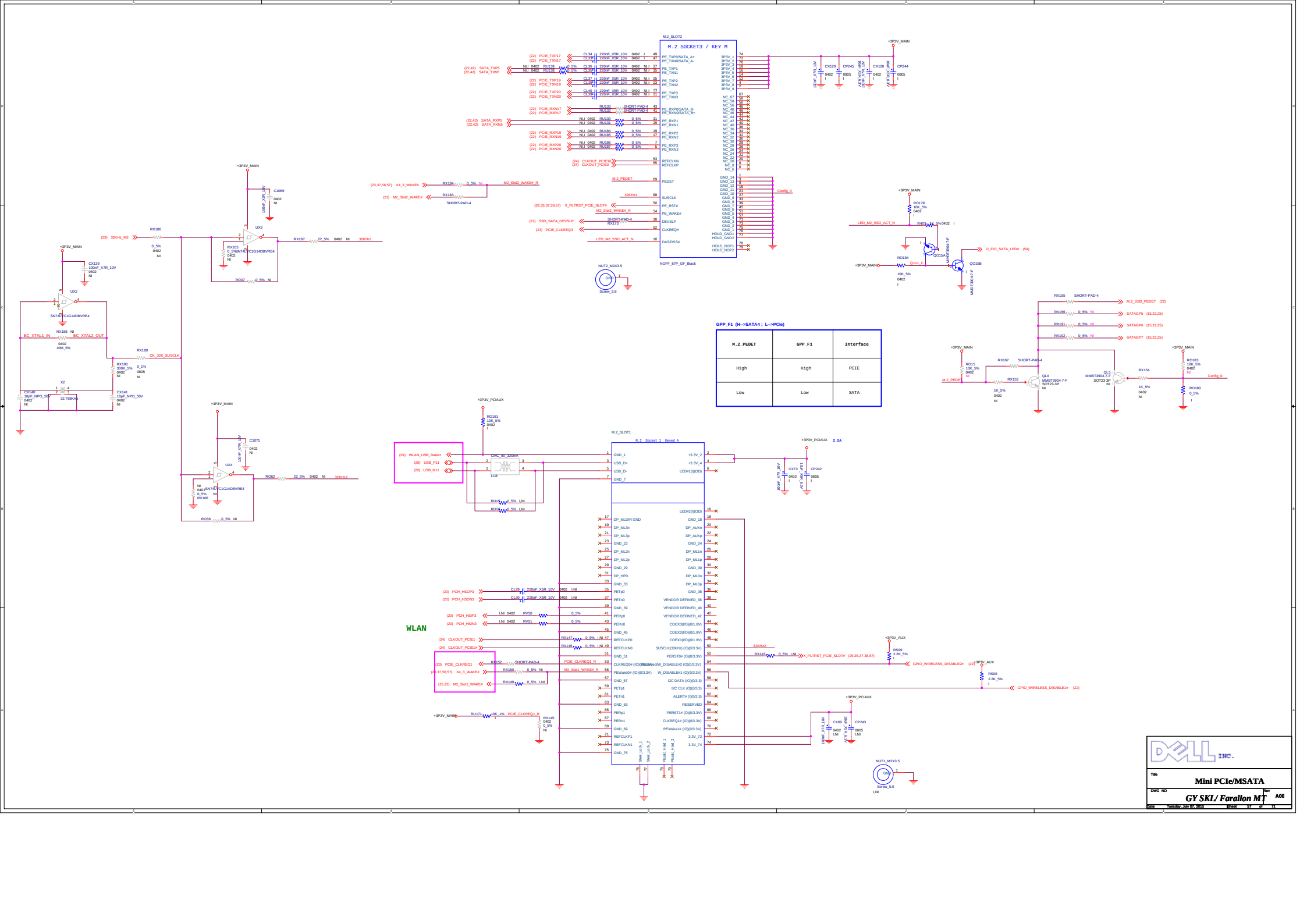
M.2_SLOT2
M.2 SOCKET3 / KEY M
NGFF_67P_GF_Black
M.2_SLOT1
M.2_Socket_1_Keyed_A
GPP_F1 (H->SATA4 ; L->PCIe)
M.2_PEDET | GPP_F1 | Interface
High | High | PCIE
Low | Low | SATA
WLAN
Mini PCIe/MSATA
GY SKL/ Farallon MT
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DELL INC.

Title

TBD

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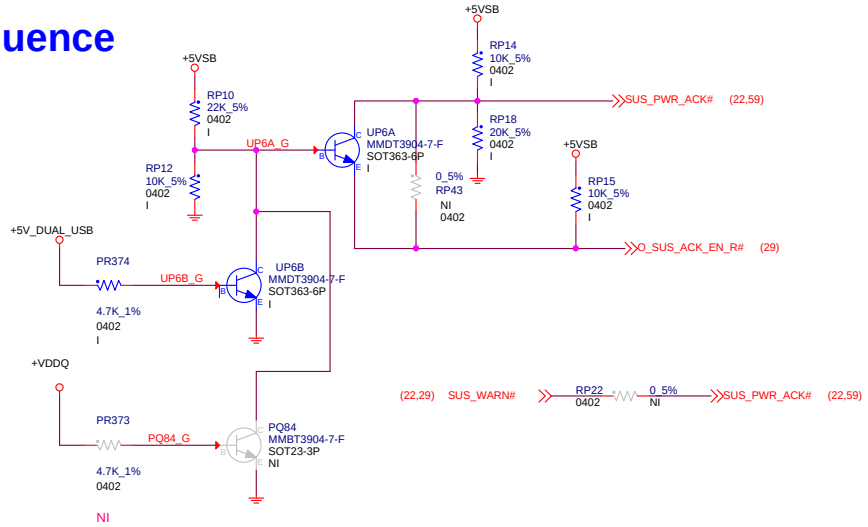
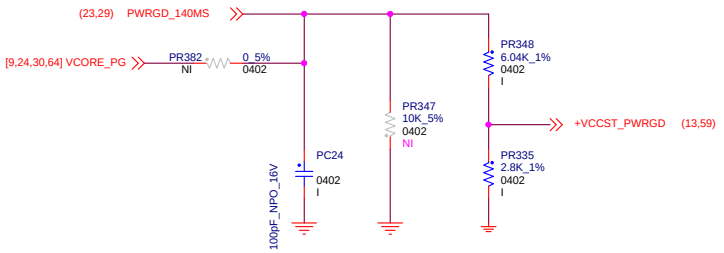
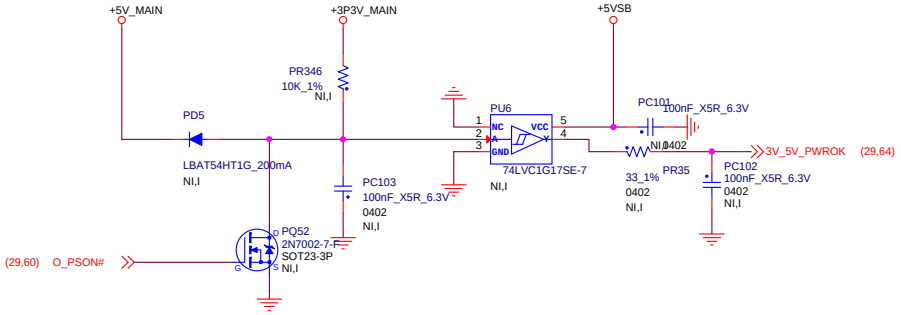
Power Sequence

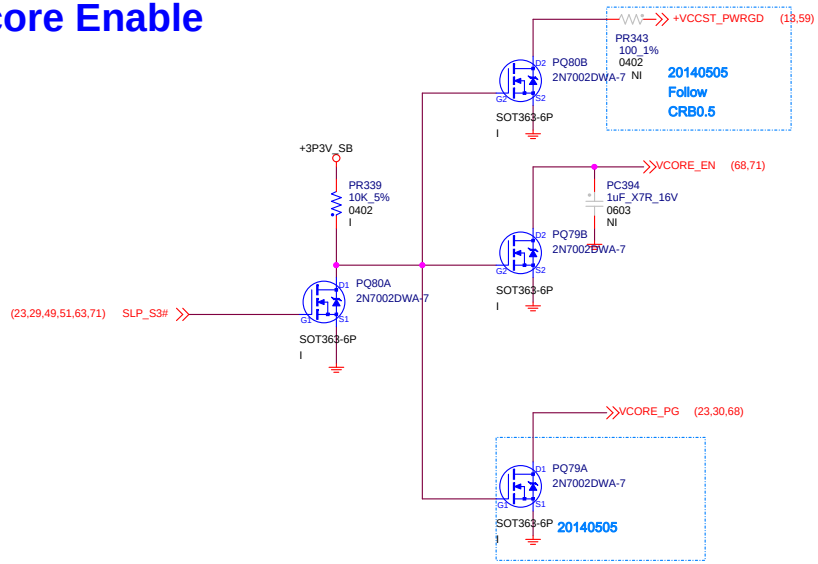






New ATXPWROK

Vcore Enable



DELL INC.

Title
Power Sequence

DWG NO
GY SKL/ Farallon MT

Rev
A00

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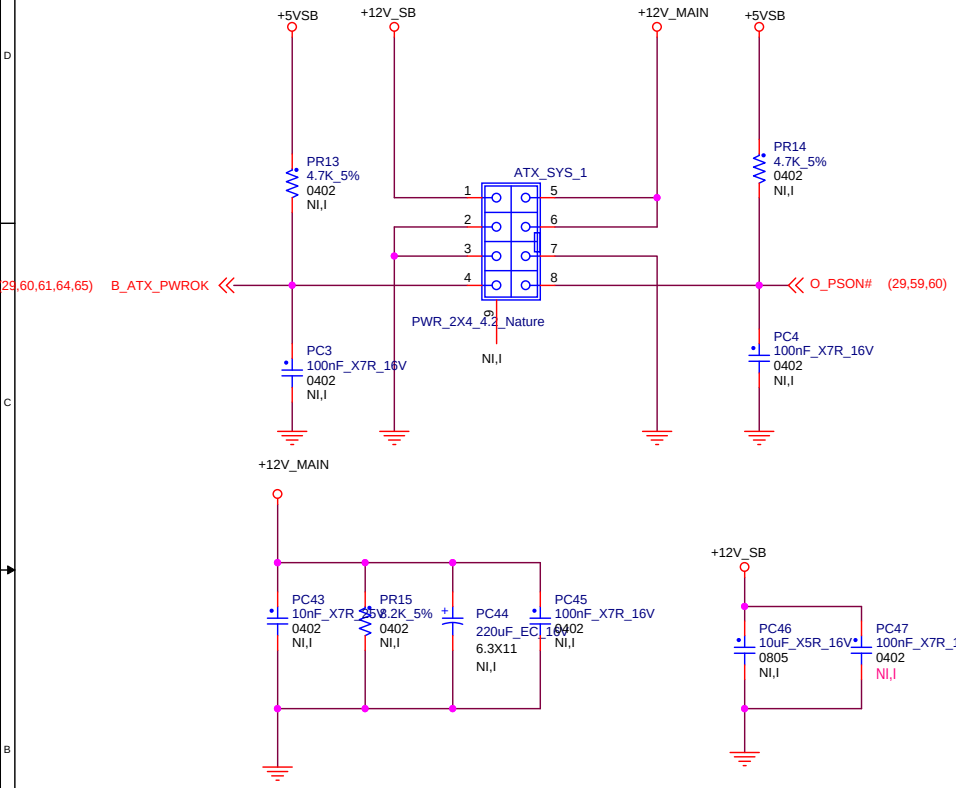
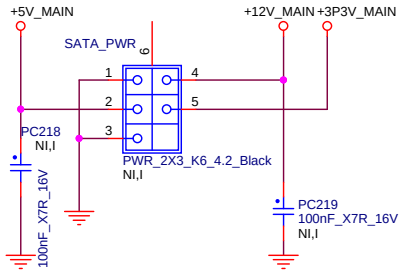
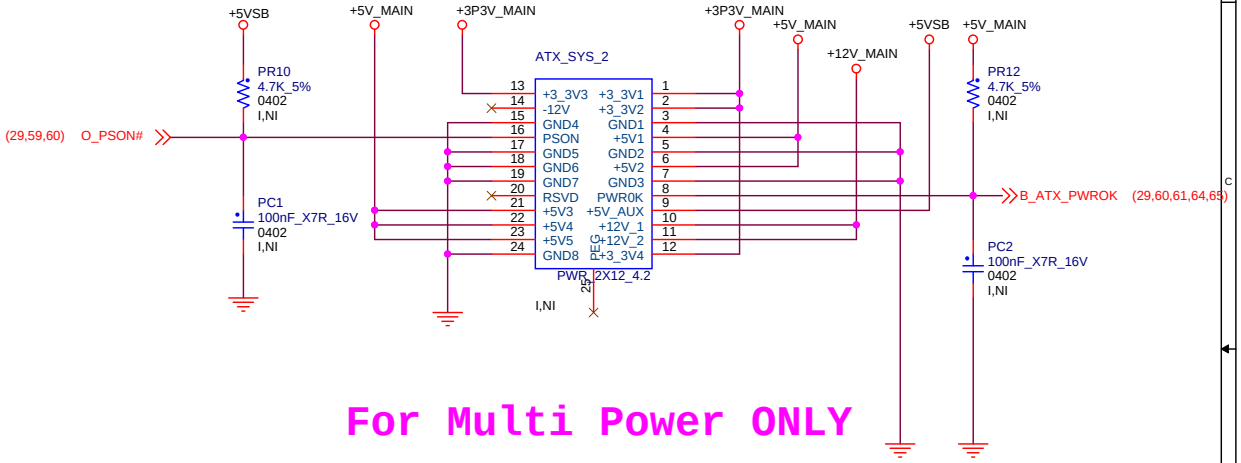
ATX POWER CONNECTOR



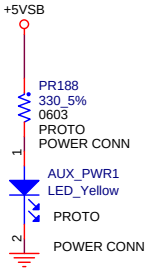
For ODD
and HDD



For single Power ONLY



For Multi Power ONLY



Title	<Title>	
Size B	Document Number <Doc>	Rev A00
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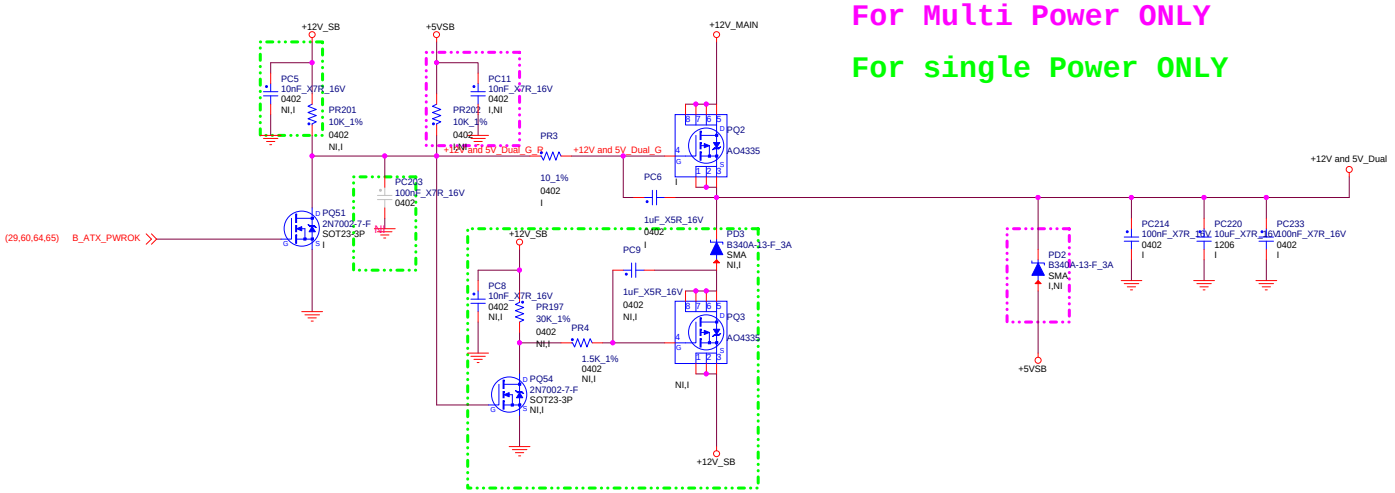
+12V and 5V_Dual



For Multi Power ONLY

For single Power ONLY

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Size C	Document Number <Doc>		Rev A00
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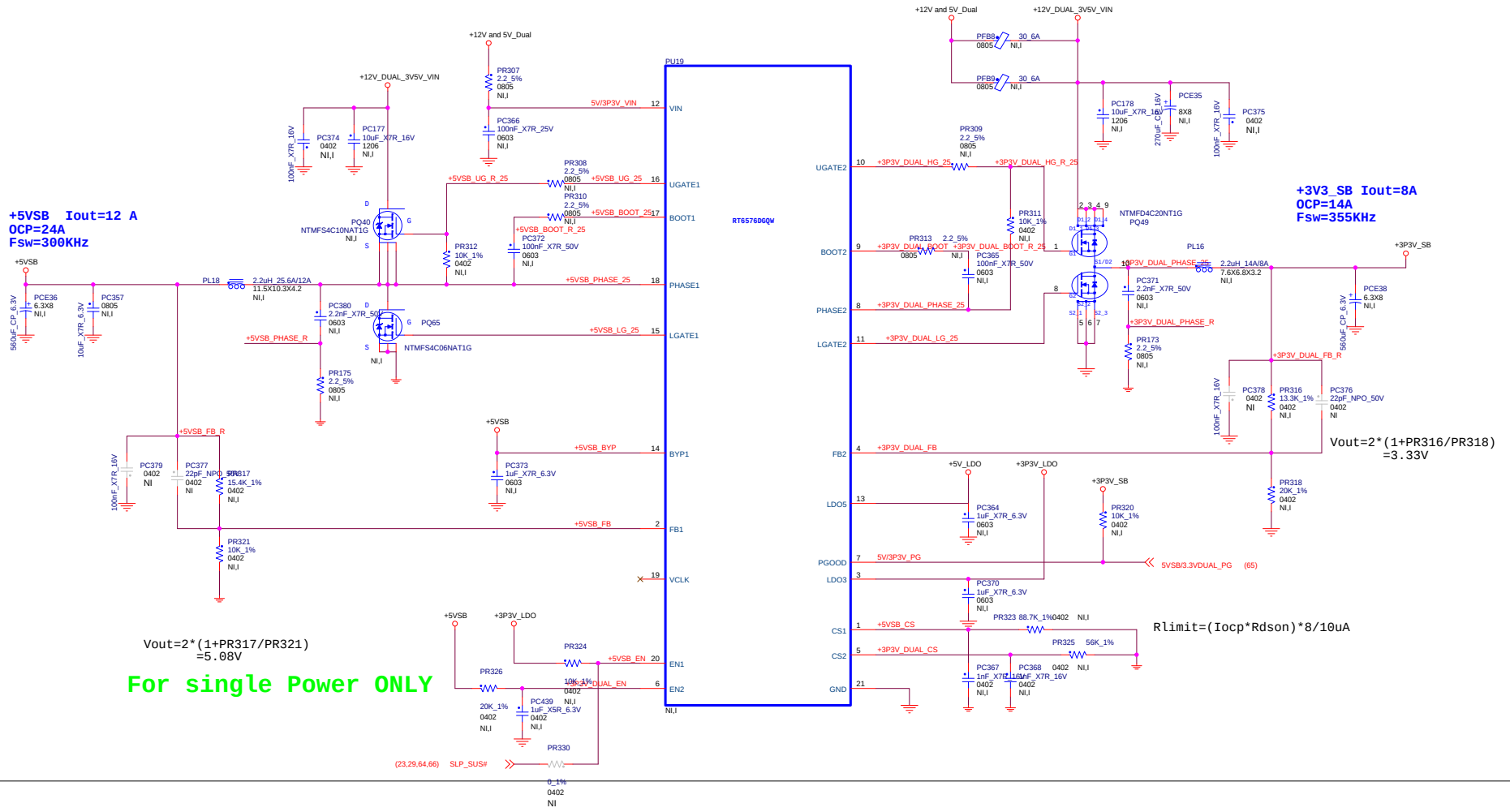

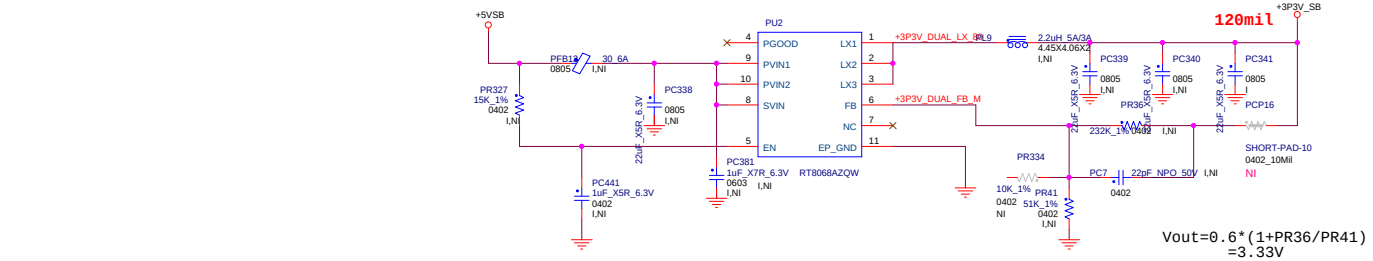

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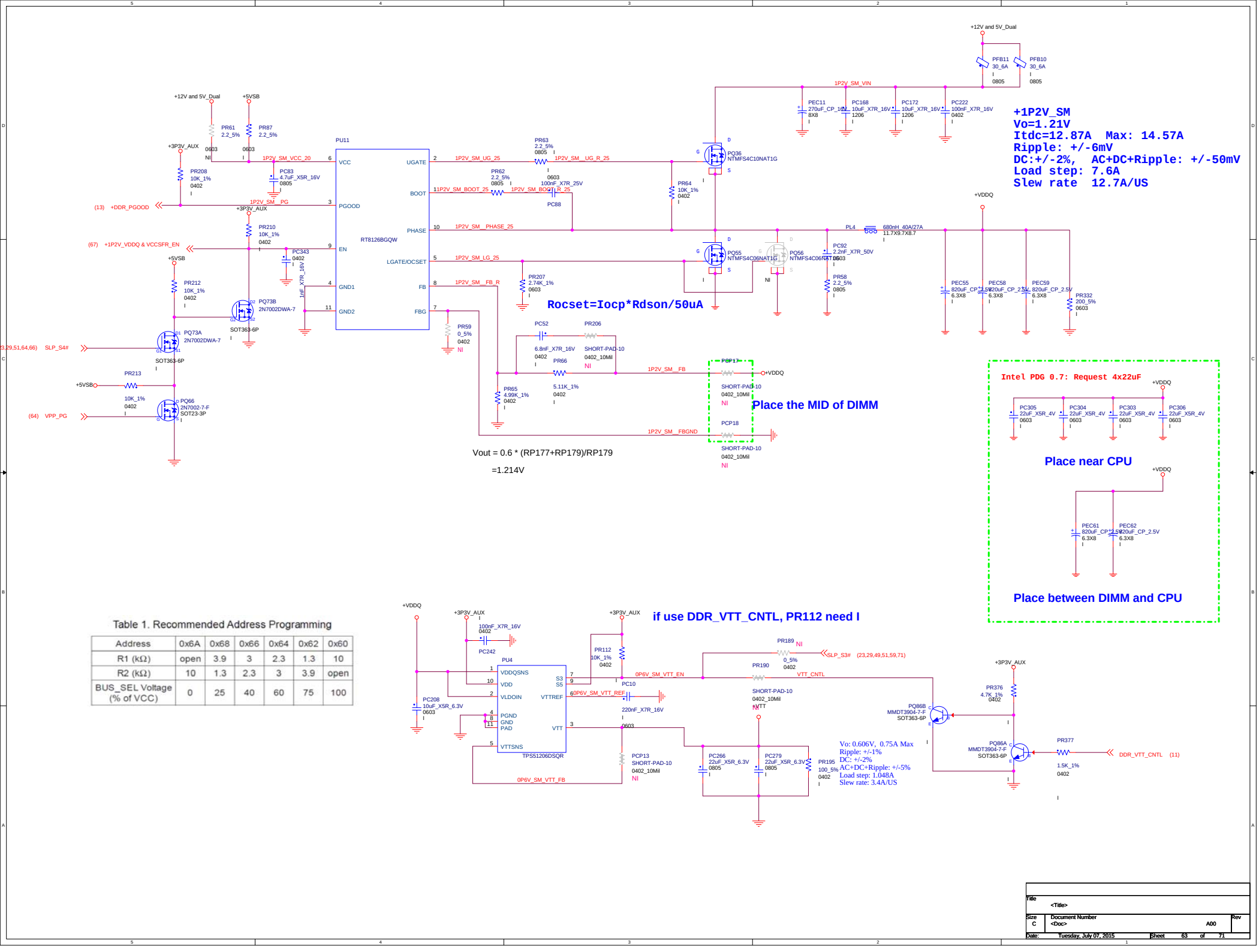

Table 1. Recommended Address Programming

Address	0x6A	0x68	0x66	0x64	0x62	0x60
R1 (kΩ)	open	3.9	3	2.3	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100

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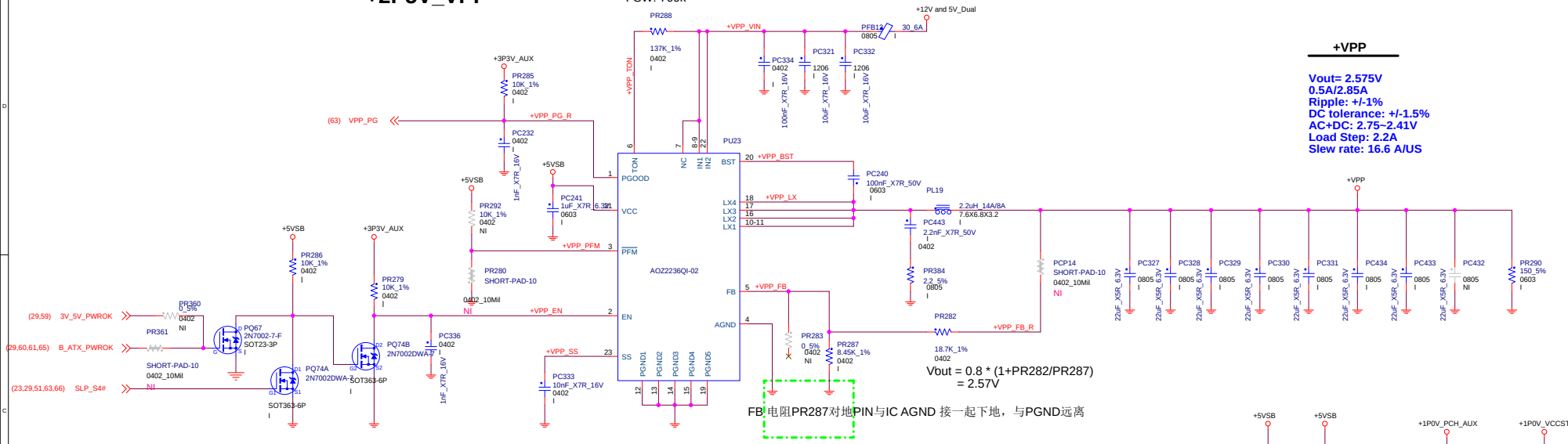
+2P5V_VPP

Fsw_khz=38000*Vout/Rton_kohm

FSW: 700k

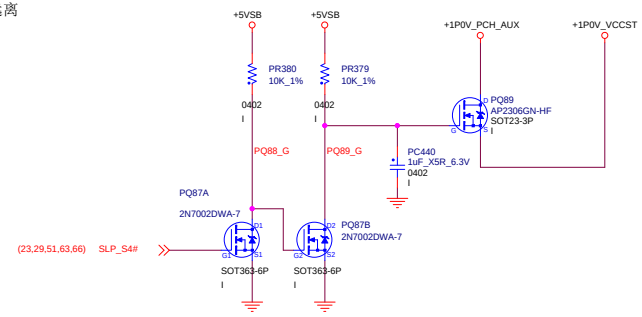


+VPP

Vout= 2.575V
0.5A/2.85A
Ripple: +/-1%
DC tolerance: +/-1.5%
AC+DC: 2.75~2.41V
Load Step: 2.2A
Slew rate: 16.6 A/US

Vout = 0.8 * (1+PR282/PR287)
= 2.57V

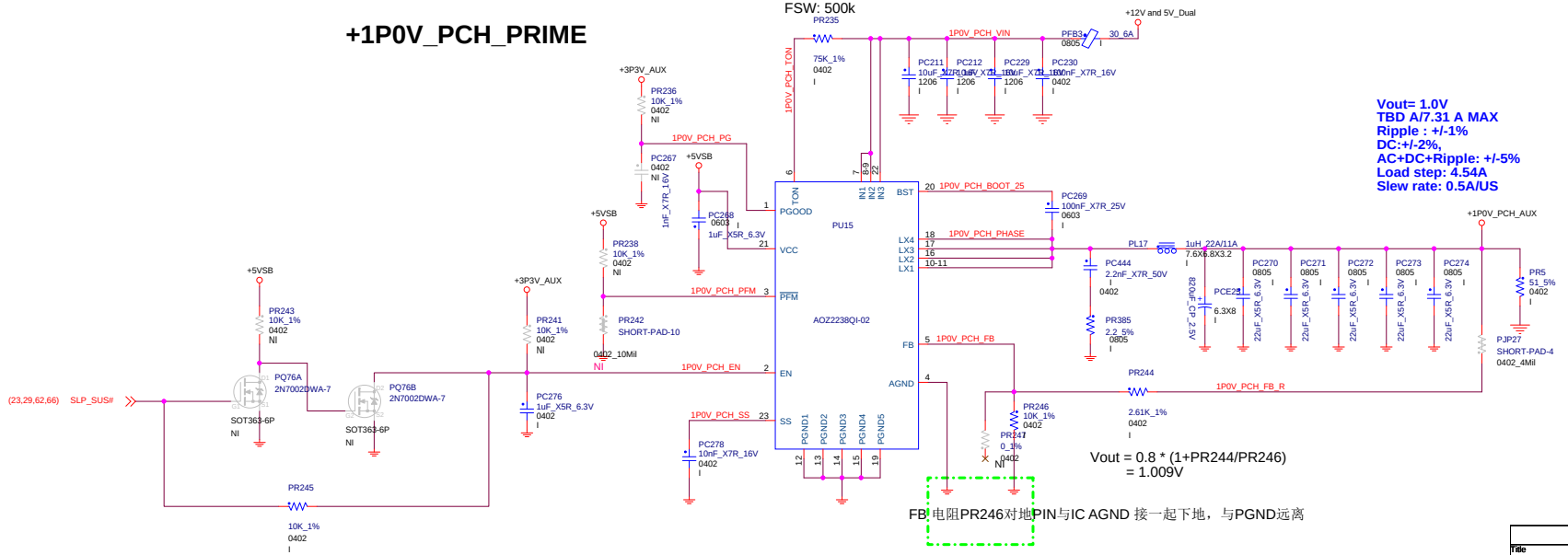
FB 电阻PR287对地PIN与IC AGND 接一起下地，与PGND远离



+1P0V_PCH_PRIME

Fsw_khz=38000*Vout/Rton_kohm

FSW: 500k



Vout= 1.0V
TBD A/7.31 A MAX
Ripple : +/-1%
DC:+/-2%,
AC+DC+Ripple: +/-5%
Load step: 4.54A
Slew rate: 0.5A/US

Vout = 0.8 * (1+PR244/PR246)
= 1.009V

FB 电阻PR246对地PIN与IC AGND 接一起下地，与PGND远离

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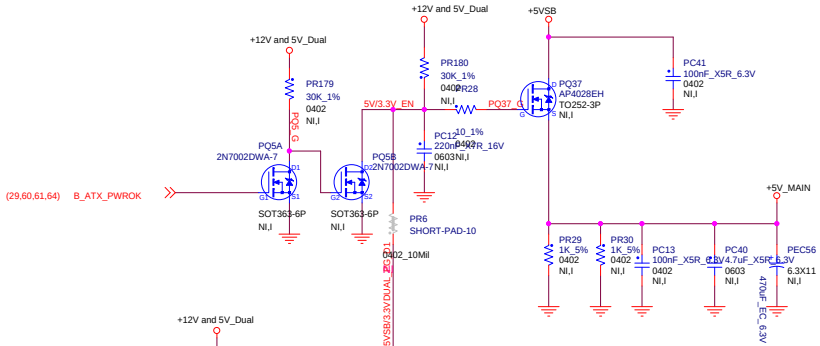
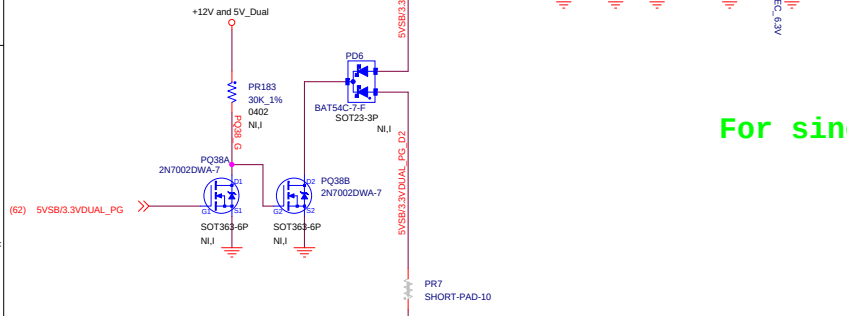
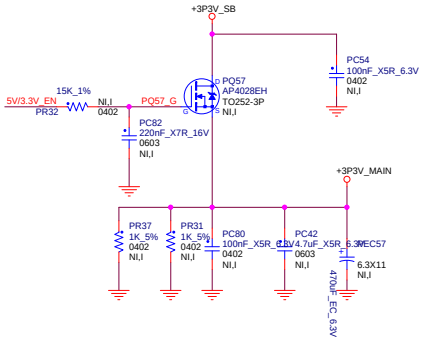
+5V MAIN



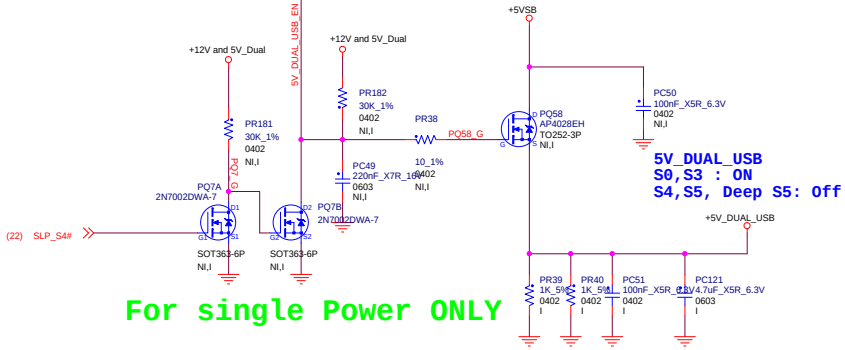


+3V MAIN



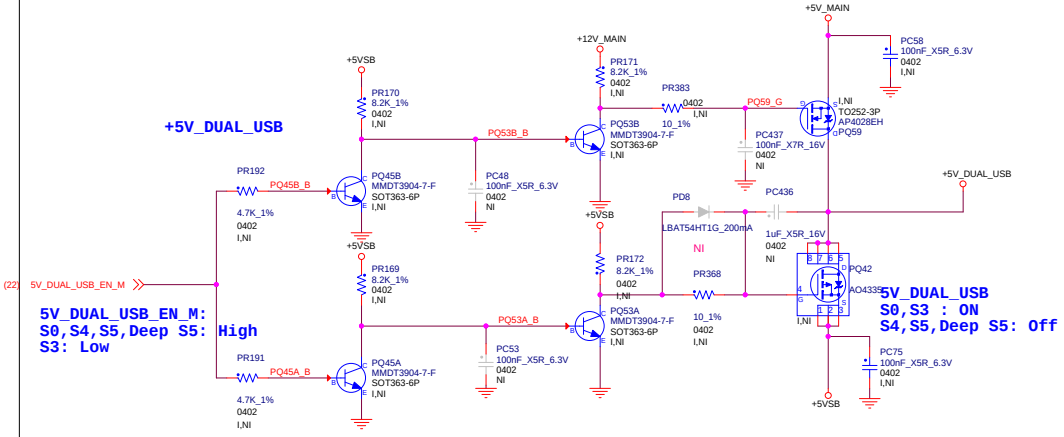
For single Power ONLY

+5V DUAL_USB



5V_DUAL_USB
S0,S3 : ON
S4,S5, Deep S5: Off

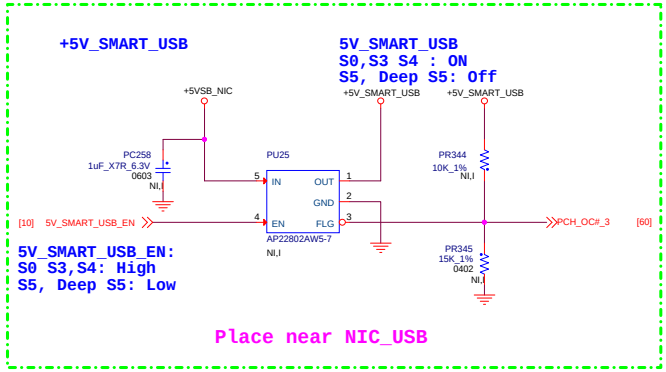
For single Power ONLY

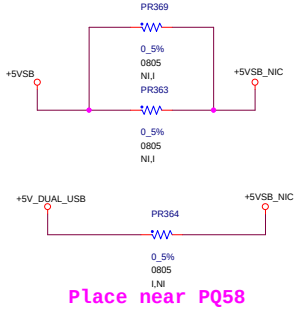


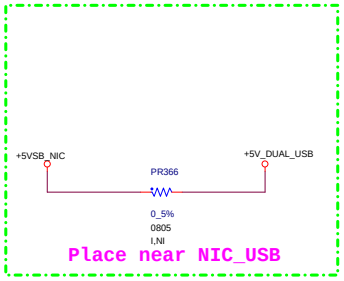
5V_DUAL_USB_EN_M:
S0,S4,S5,Deep S5: High
S3: Low

5V_DUAL_USB
S0,S3 : ON
S4,S5,Deep S5: Off

For Multi Power ONLY







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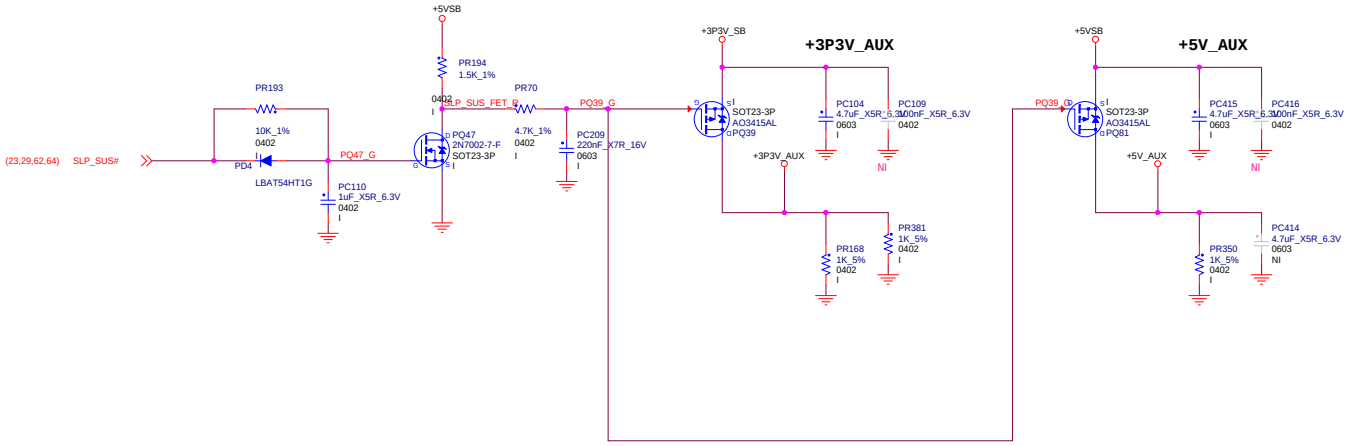
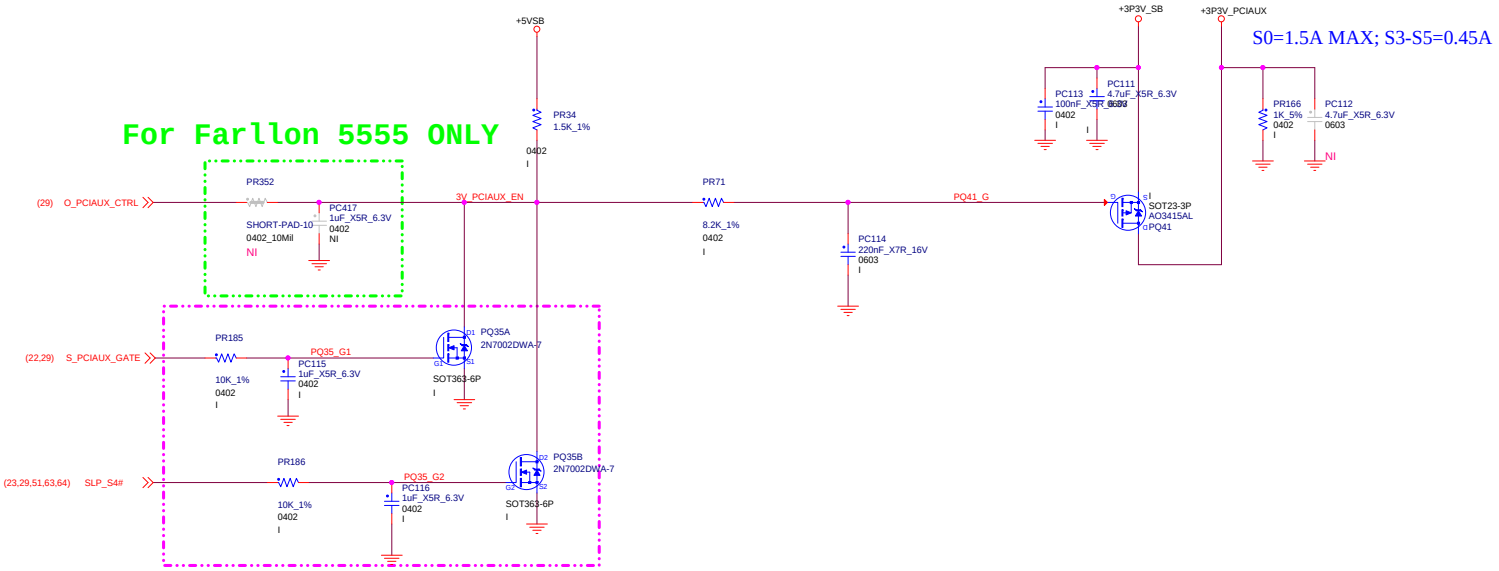


+3V_PCIAUX(FOR PCI/PCIE SLOT)

S0=1.5A MAX; S3-S5=0.45A



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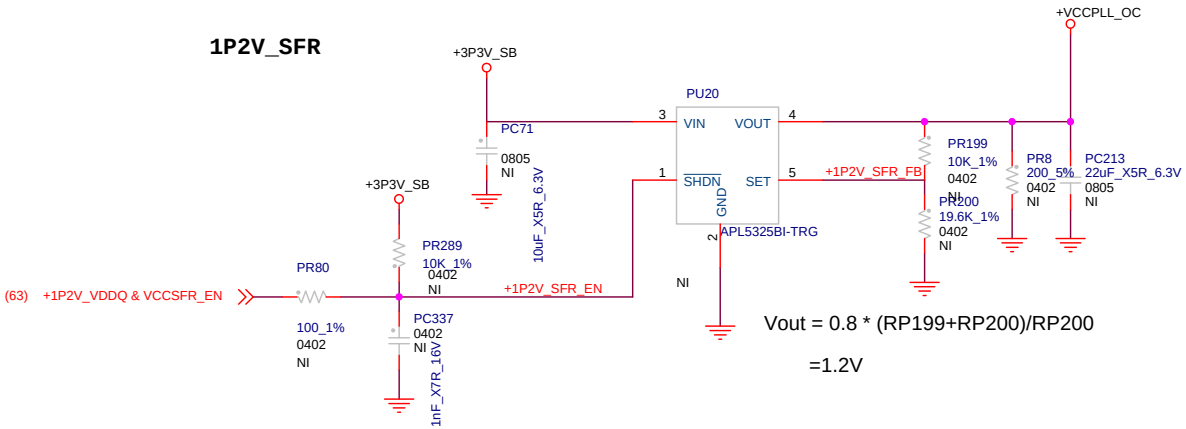
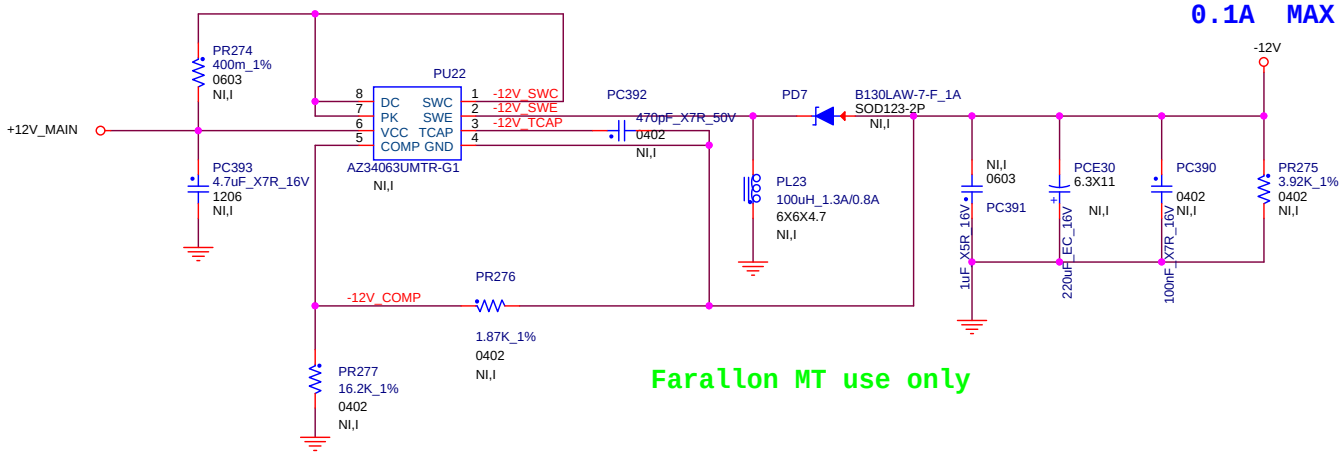
1P2V_SFR

0.1A MAX



-12V

0.1A MAX



Farallon MT use only

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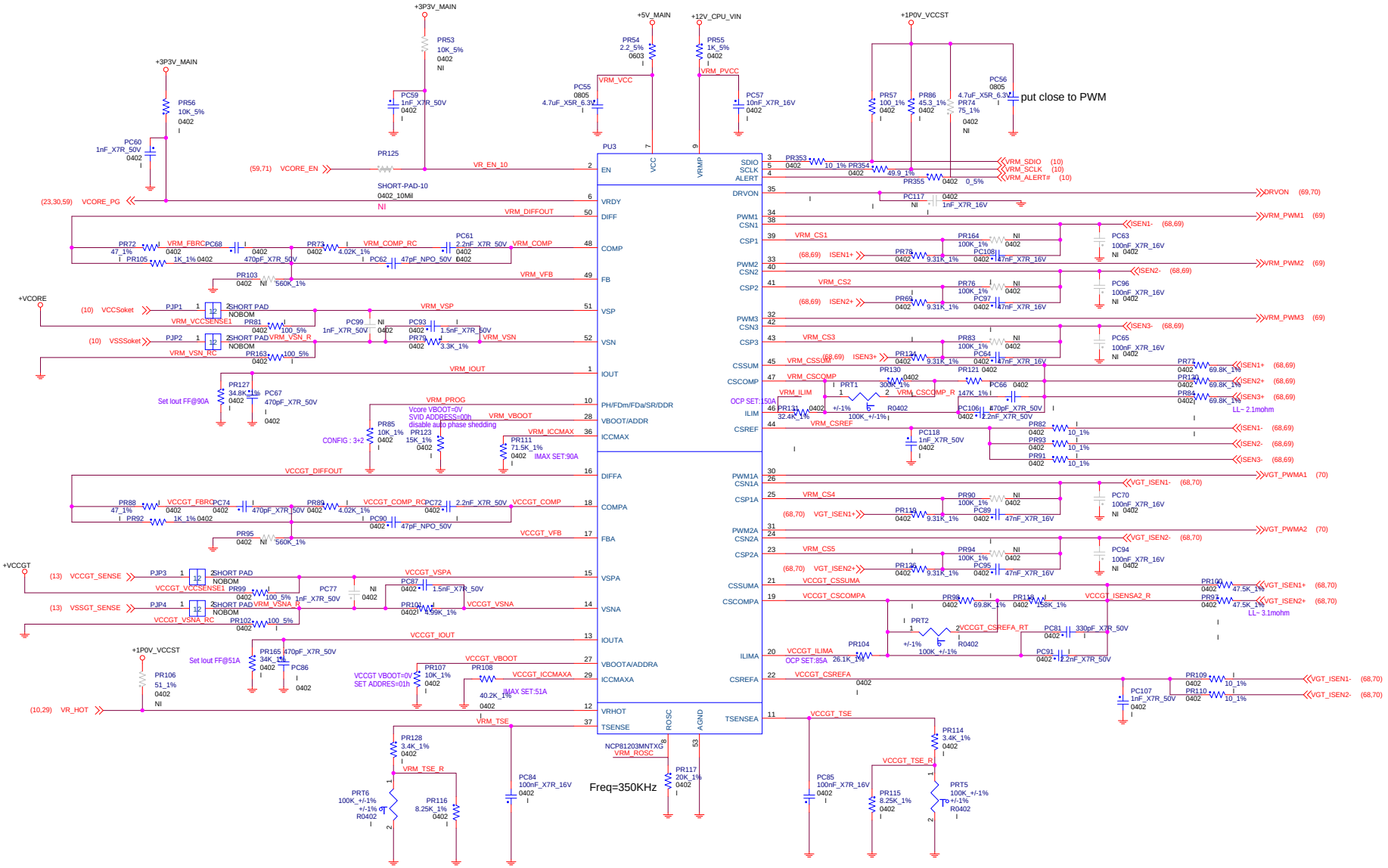

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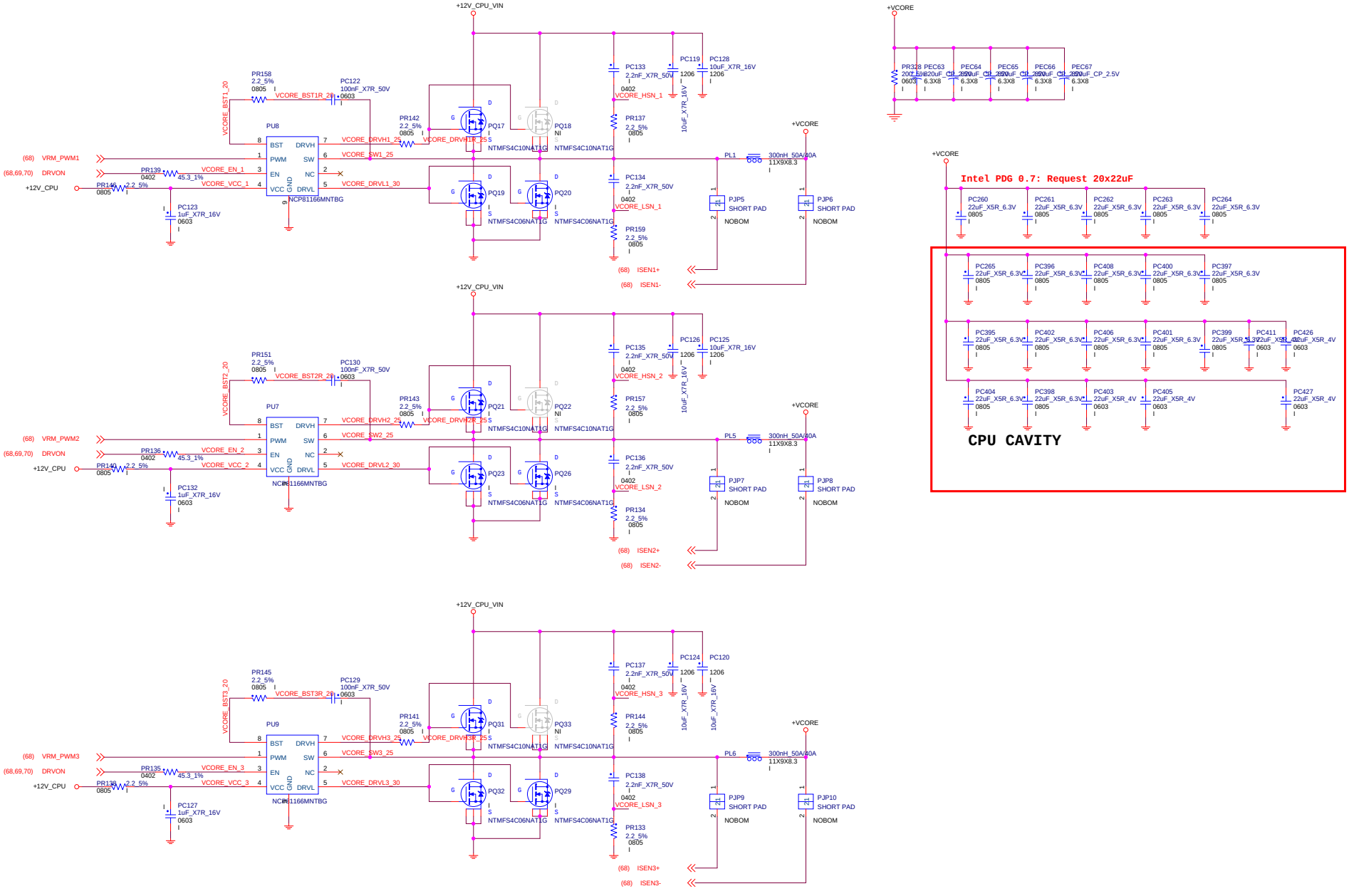
VCORE PHASE1~3

67A TDC / 90A MAX



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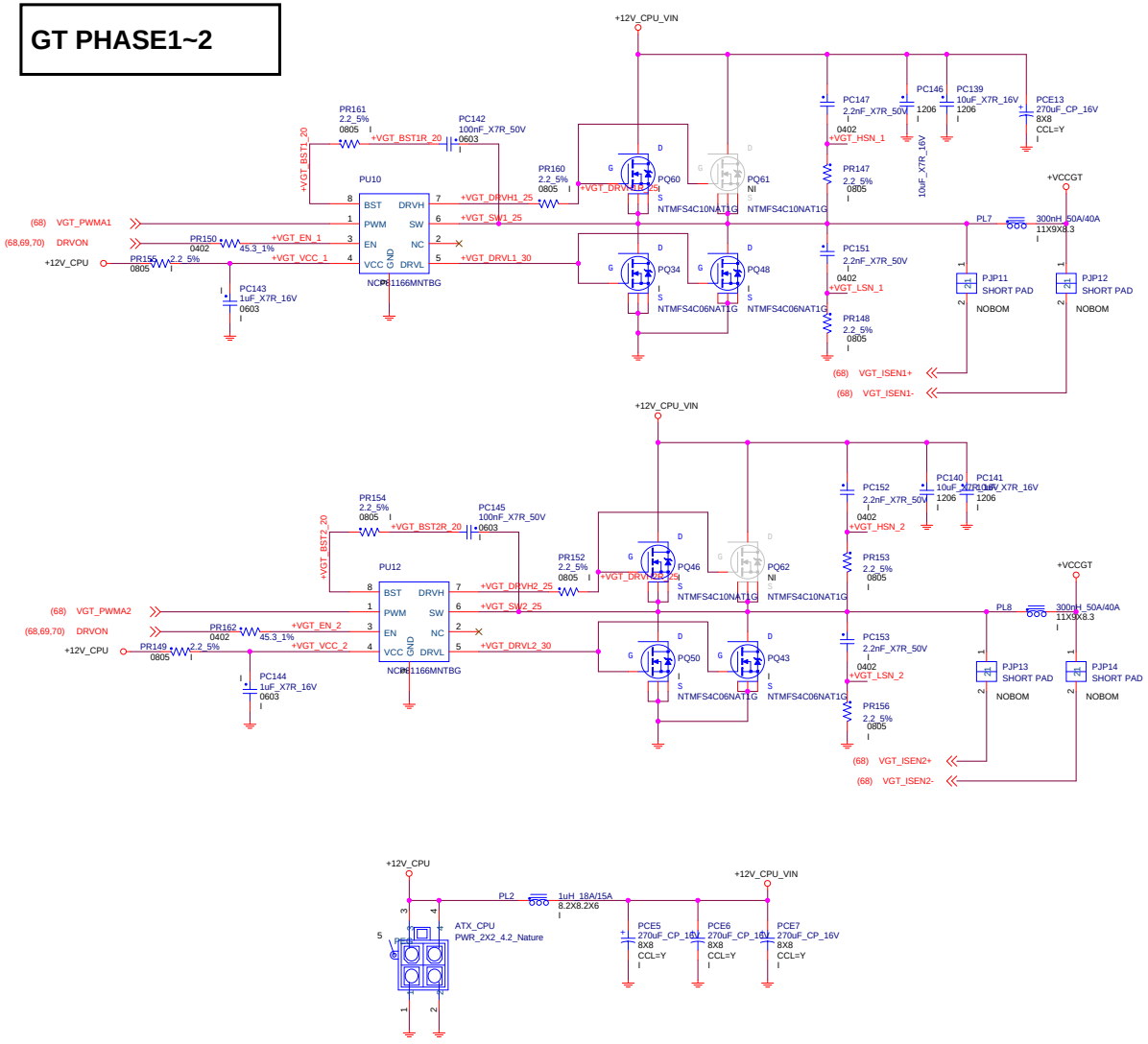
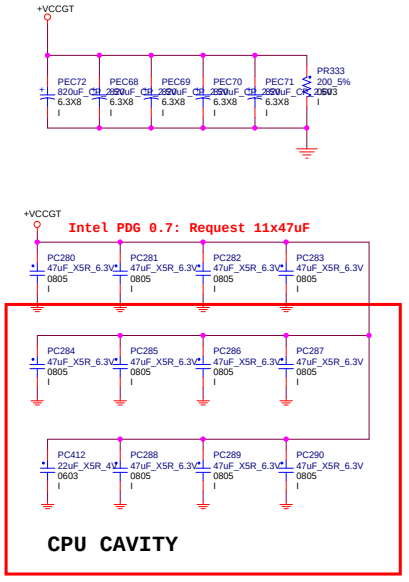
GT PHASE1~2



35A TDC / 51A MAX



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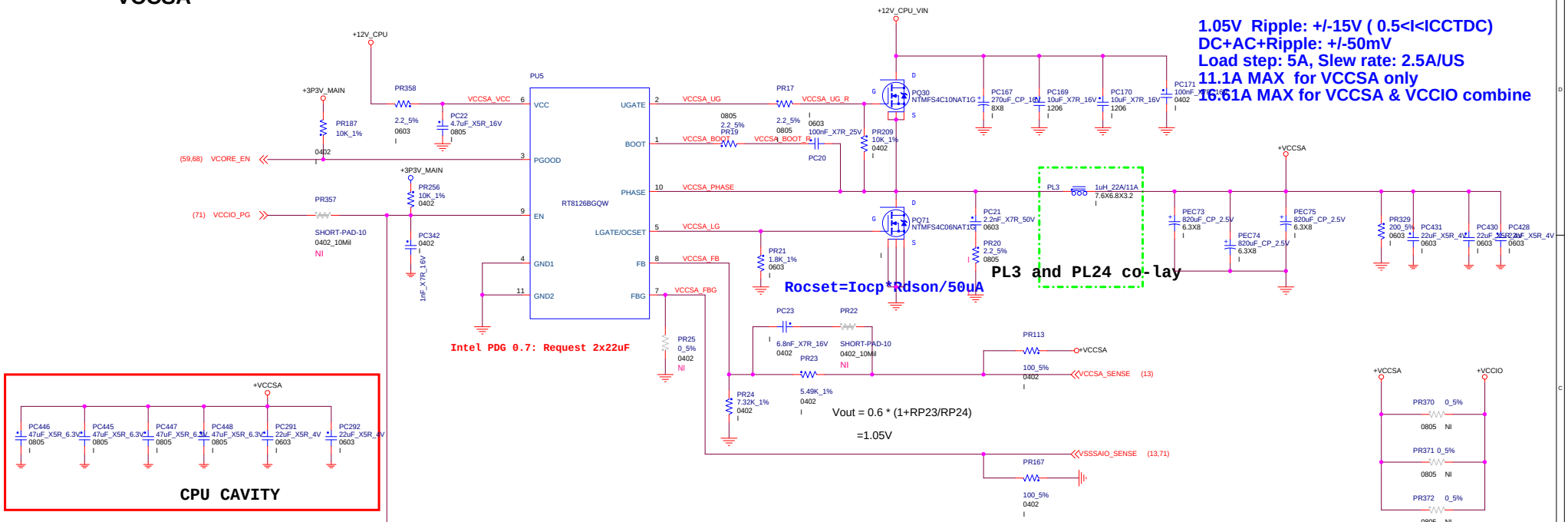
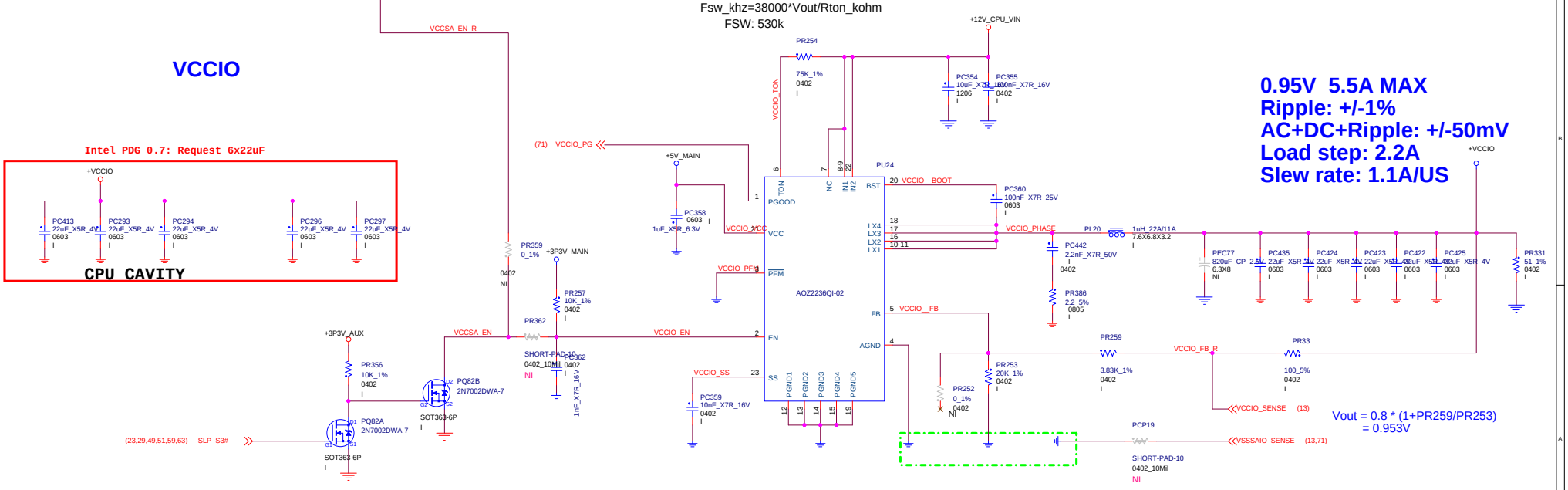
VCCSA



VCCIO



FB 电阻PR253,PCP19对地PIN与IC AGND 接一起下地，与PGND远离

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