Hellcat 14/15_ ICL
Schematics DIAGRAM

2019-09-17

REV : SA

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

<Core Design>

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Title	Cover Page	
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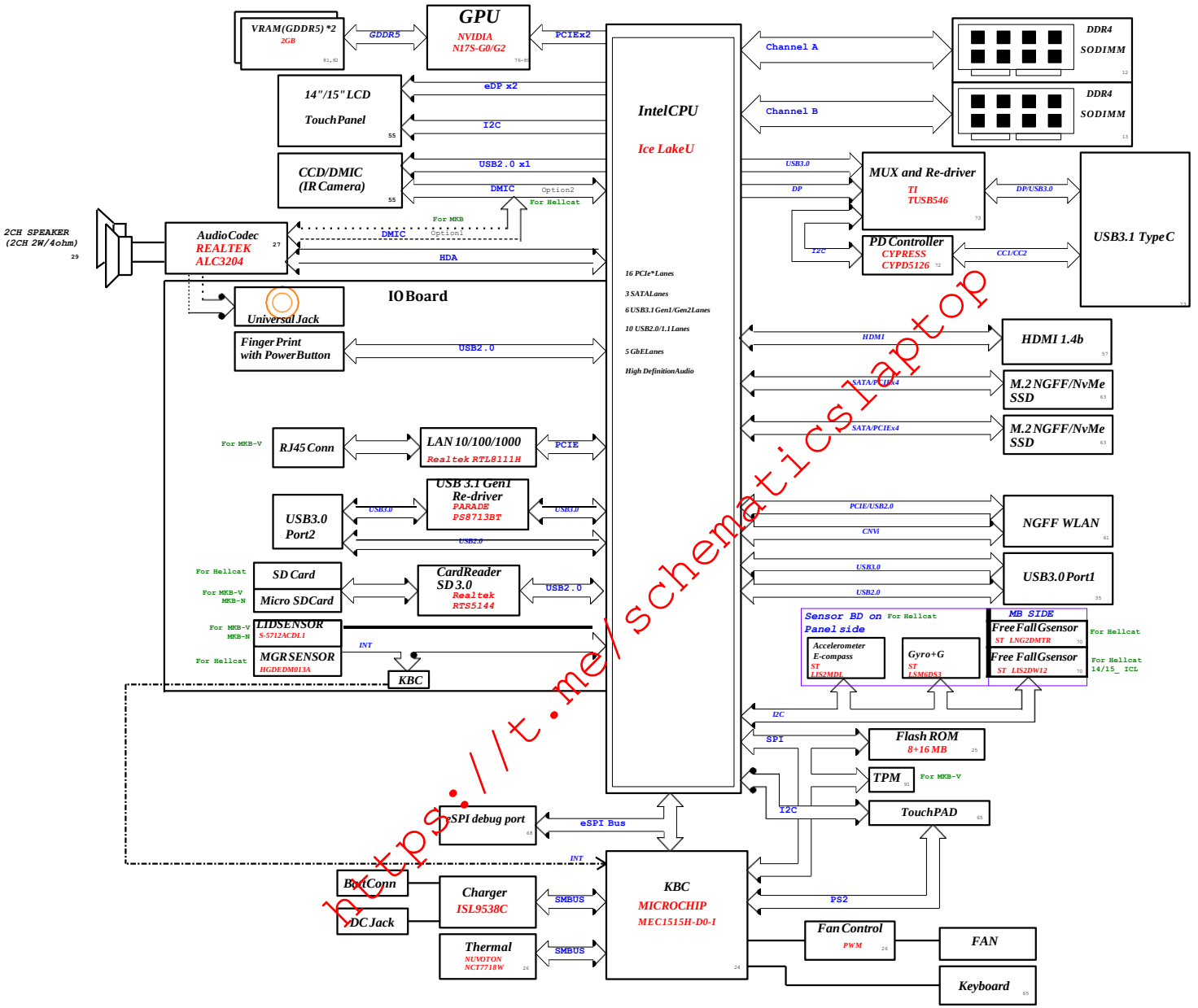
Date: Tuesday, September 17, 2019	Sheet 1 of 106	

HellCat CML Block Diagram



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Title: BlockDiagram
Size: Document Number: Hellcat 14/15_ ICL
Rev: SA
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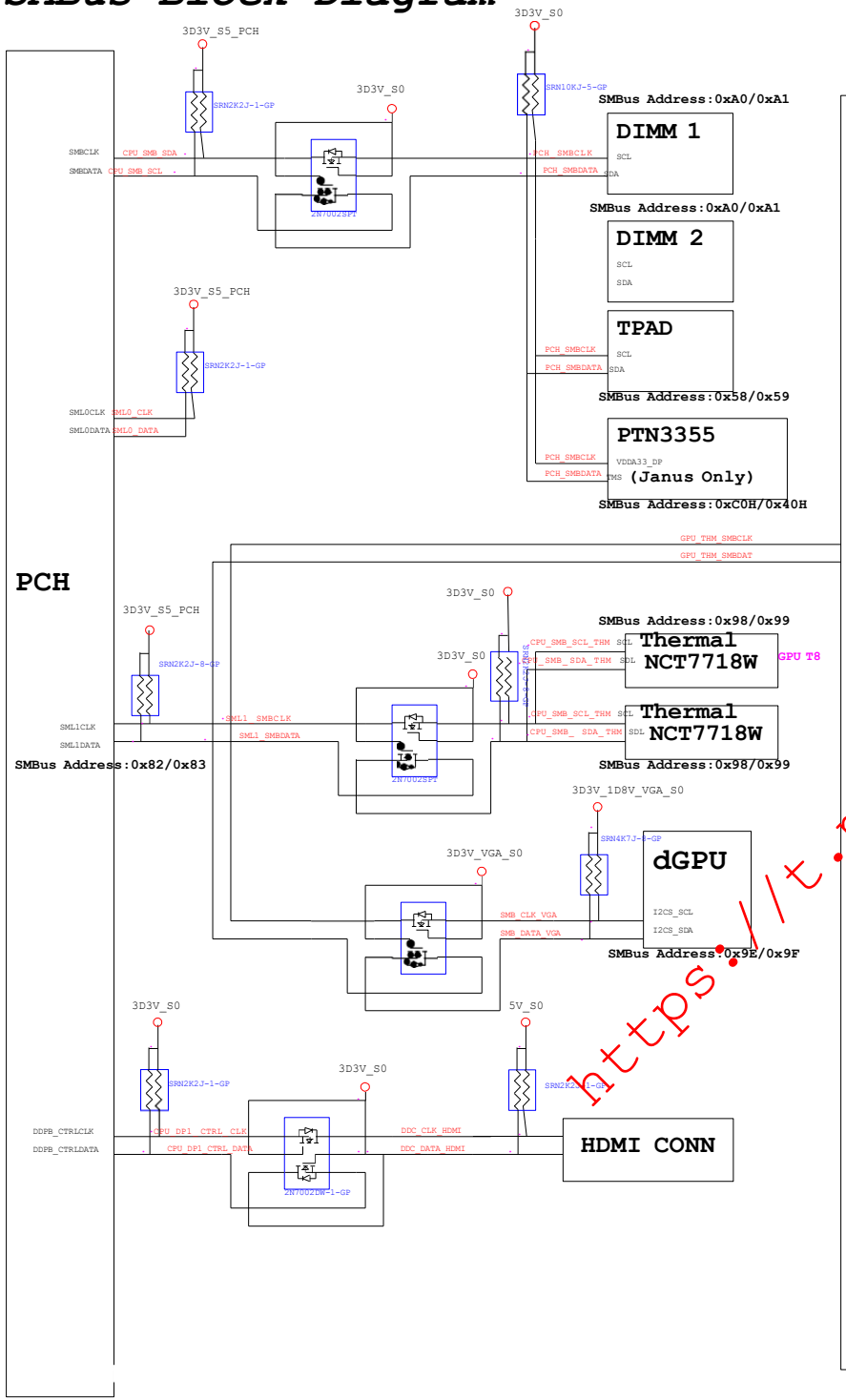
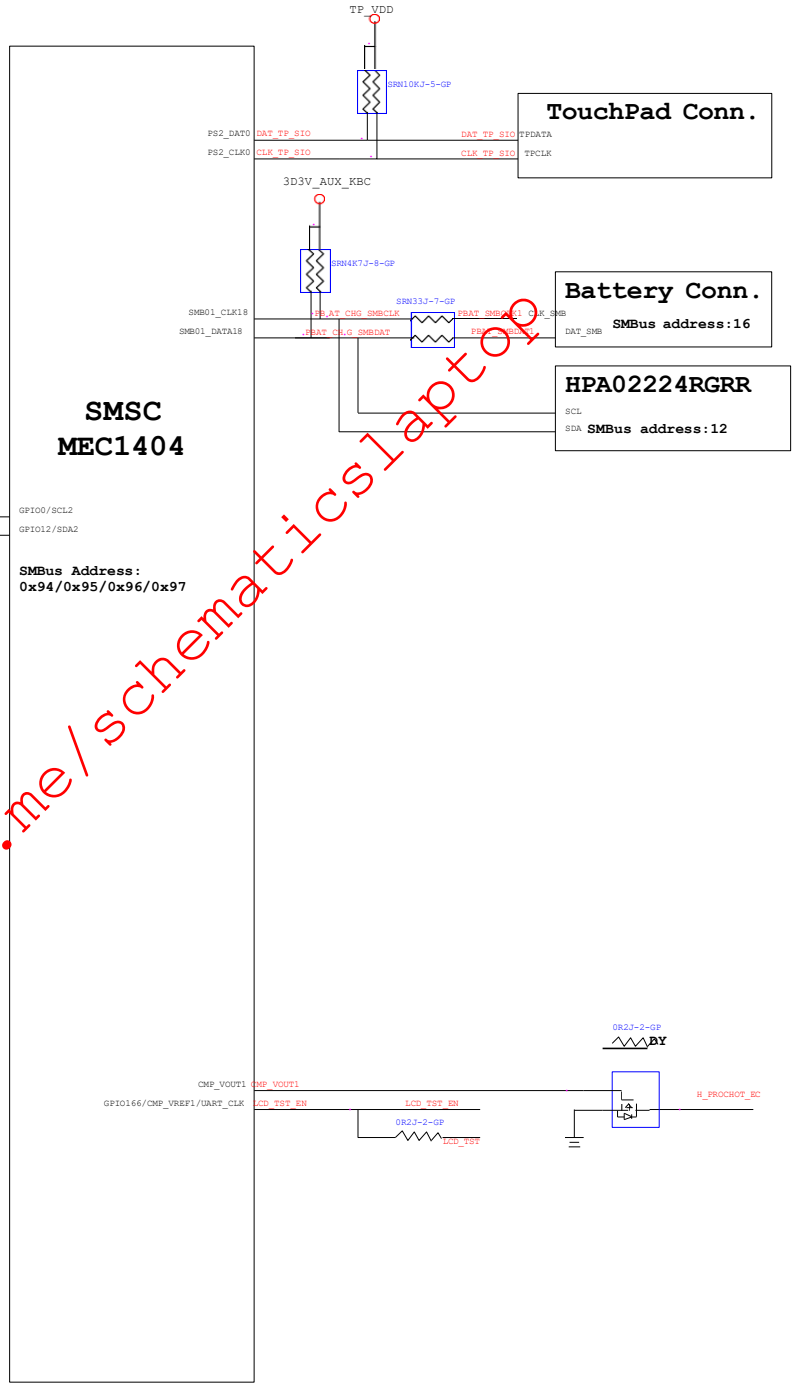
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram
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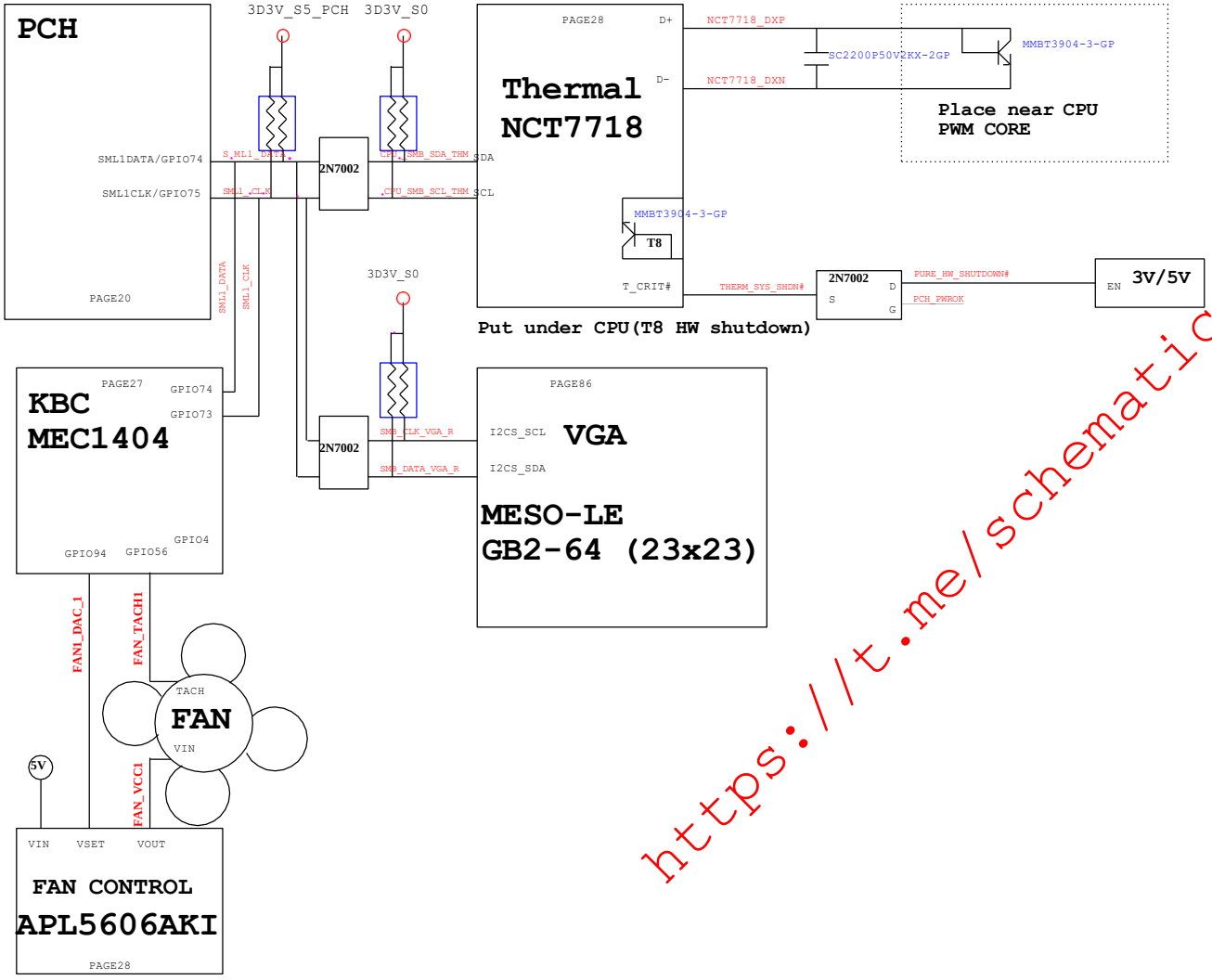
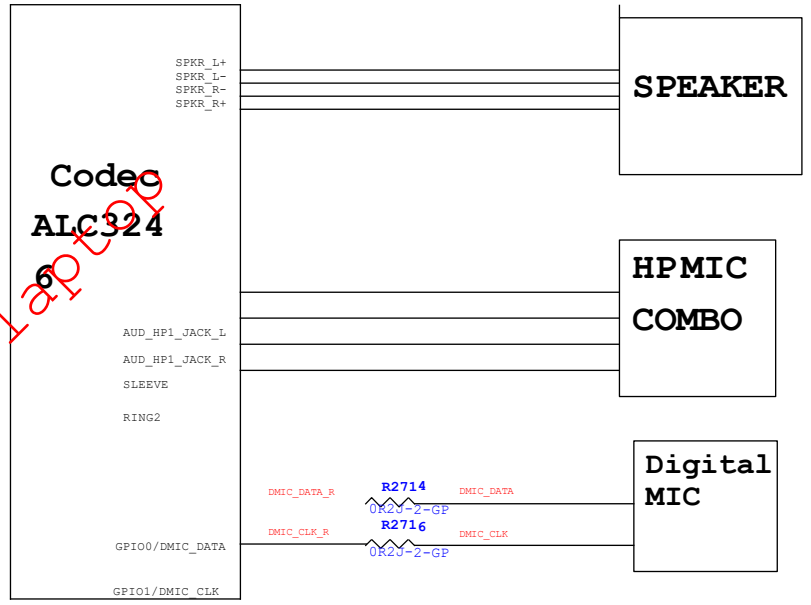
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio BlockDiagram

Size: Custom | Document Number: Hellcat 14/15_ ICL | Rev: SA

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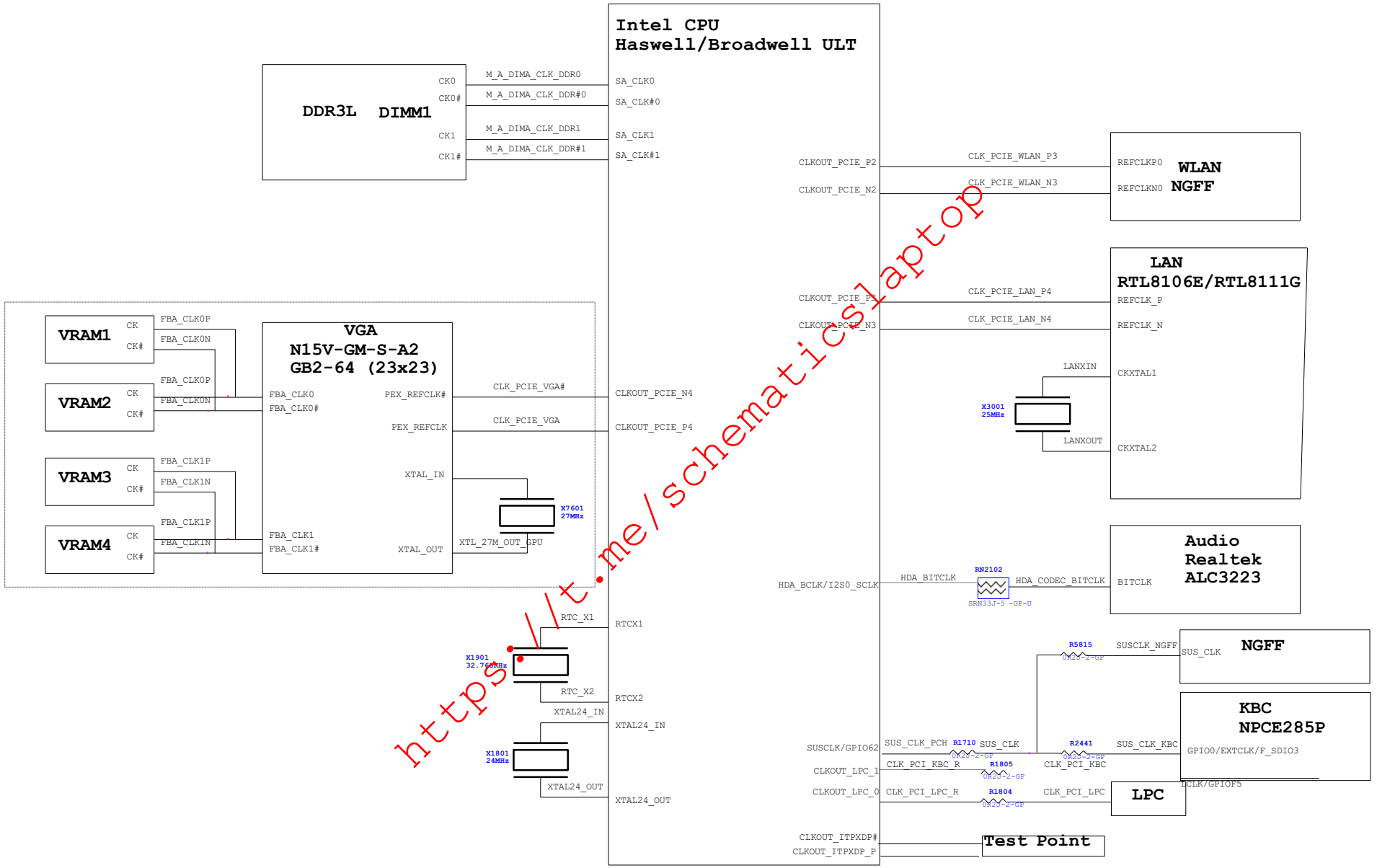
CLK Block Diagram



<CoreDesign>
Wistron Corporation
CLK Block Diagram
Size: A2
Document Number: Hellcat 14/15_ICL
Rev: SA
Date: Tuesday, September 17, 2019
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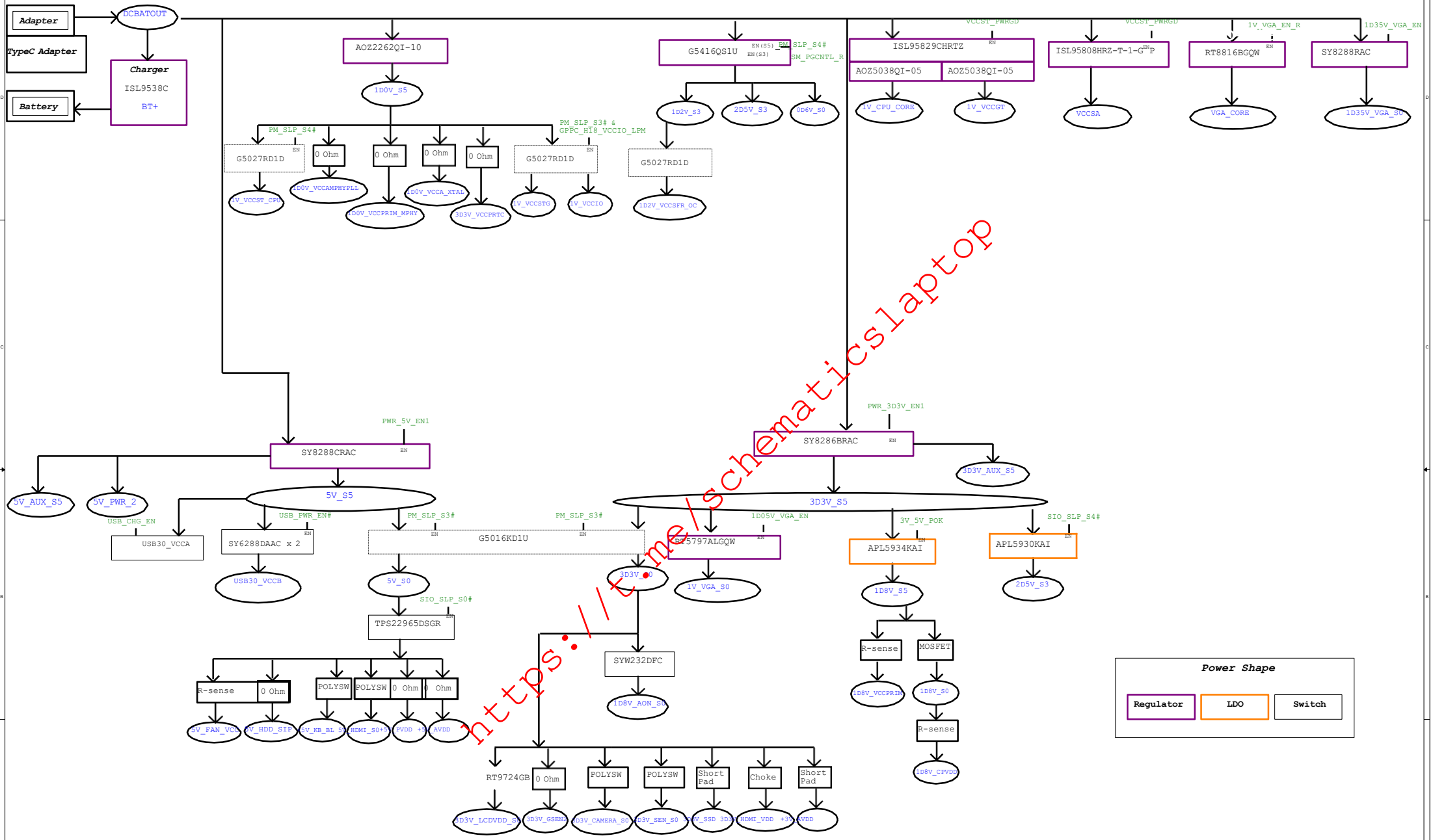

Title: Power Block Diagram

Size	Document Number	Rev
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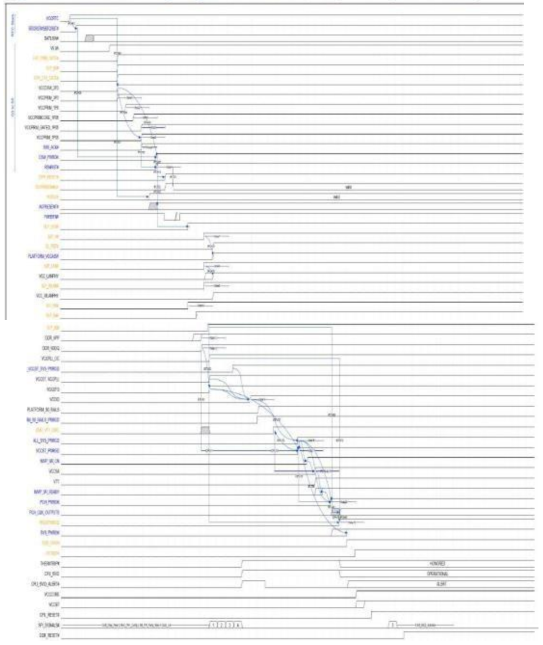
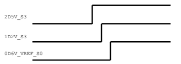
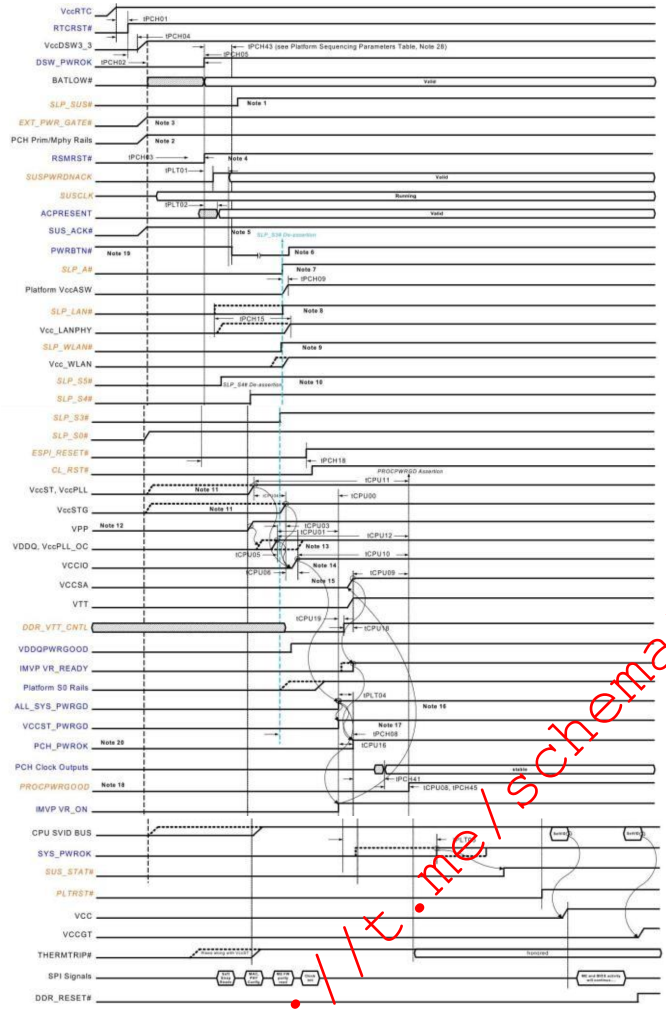
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



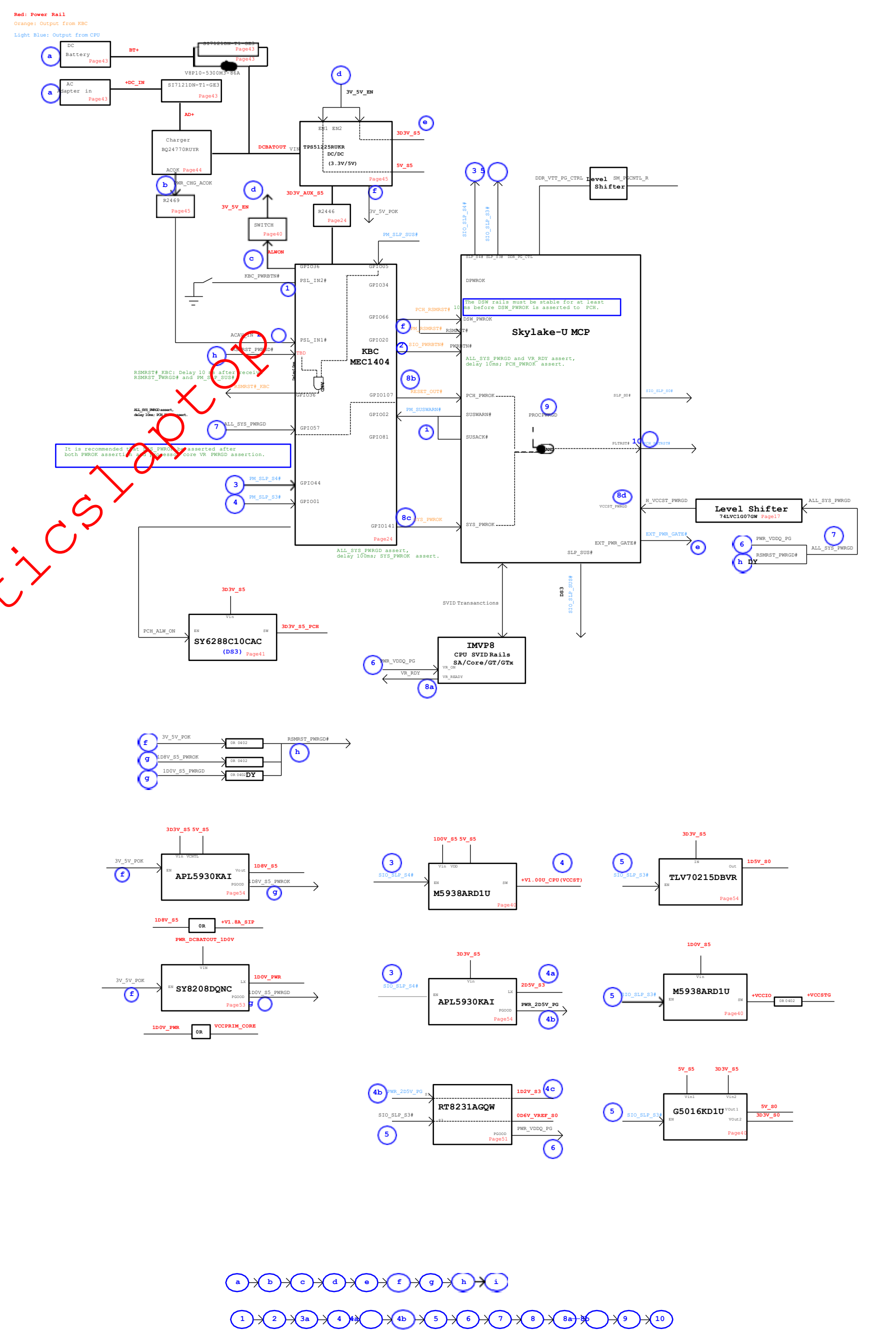
For DDR4 power sequence



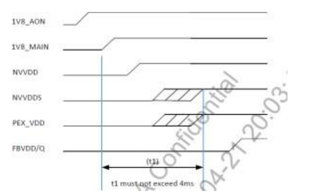
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



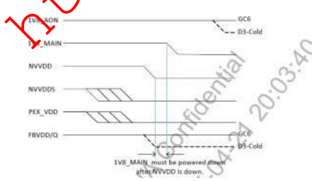
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence



DELL Wistron Corporation
Power Sequence
MOCKINGBIRD BCL

Main Func = CPU

[24] PECI_CPU
[22,24,44,46] PROCHOT#_CPU

[99] CPU_JTAG_TCK
[99] CPU_JTAG_TDI
[99] CPU_JTAG_TDO
[99] CPU_JTAG_TMS
[99] CPU_JTAG_TRST#
[99] PCH_JTAG_TCK
[99] CPU_JTAG_PRDY#
[99] CPU_JTAG_PREQ#
[15,99] DBG_PMODE

[15] GPP_E6
[15] GPP_H2

[55] TOUCH_PANEL_PD#
[55] TOUCH_PANEL_DET#

[24,65] TOUCHPAD_INTR#

1D05V_VCCSTG_TERM
R313 51R2J-2-GP CPU_JTAG_TDO
DY
R311 51R2J-2-GP CPU_JTAG_PREQ#
R314 51R2J-2-GP
R315 51R2J-2-GP CPU_JTAG_TDI
CPU_JTAG_TMS

TPAD14-OP-GP
TP301

R312 51R2J-2-GP CPU_JTAG_TCK
DY
RN304 SRN51J-GP
1 CPU_JTAG_TRST#
2 PCH_JTAG_TCK
R305 49D9R2F-GP CPU_POPI_RCOMP
R306 49D9R2F-GP PCH_OPI_RCOMP
DY
RN306 SRN49D9F-GP
1 EDRAM_OPIO_RCOMP
2 CPU_EOPIO_RCOMP

R307 0R2J-2-GP
TOUCHPAD_INTR# TOUCH_PAD_INTR#

3D3V_S0
R301 100KR2J-1-GP
TOUCH_PANEL_DET#

1 : non touch
0 : touch

CPU1D 4 OF19
ICE-LAKE-U-GP-U

H_CATERR# J4
PECI_CPU CD5
PROCHOT#_CPU_R C3
THERMTRIP#_CPU E3
PROC_POPIRCOMP
PCH_OPIRCOMP
RSVD_25
RSVD_26
DBG_PMODE DL15
GPP_E3 DV11
TOUCH_PANEL_PD# DT11
TOUCH_PAD_INTR# CR38
TOUCH_PANEL_DET# CR39
GPP_E6 DT12
GPP_H2 DJ38 DL38

CATERR#
PECI
PROCHOT#
THRMTRIP#
DBG_PMODE
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_E6
GPP_H2/CNV_BT_I2S_SDO
GPP_H19/TIME_SYNC0

PROC_TCK P3 CPU_JTAG_TCK
PROC_TDI K5 CPU_JTAG_TDI
PROC_TDO K3 CPU_JTAG_TDO
PROC_TMS P4 CPU_JTAG_TMS
PROC_TRST# N1 CPU_JTAG_TRST#
PCH_TRST# N5
PCH_TCK R5 PCH_JTAG_TCK
PCH_TDI K1
PCH_TDO K2
PCH_TMS N3
PCH_JTAGX N2
PROC_PRDY# P6 CPU_JTAG_PRDY# M6
PROC_PREQ# CPU_JTAG_PREQ#

1D05V_VCCSTG_TERM
R302 1KR2F-3-GP
PROCHOT#_CPU
R303 499R2F-2-GP PROCHOT#_CPU_R

1D05V_VCCST
R304 1KR2F-3-GP THERMTRIP#_CPU
R309 49D9R2F-GP H_CATERR#

<CoreDesign>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THML/JTAG)

Size	Document Number	Rev
A4	Hellcat 14/15_ ICL	SA

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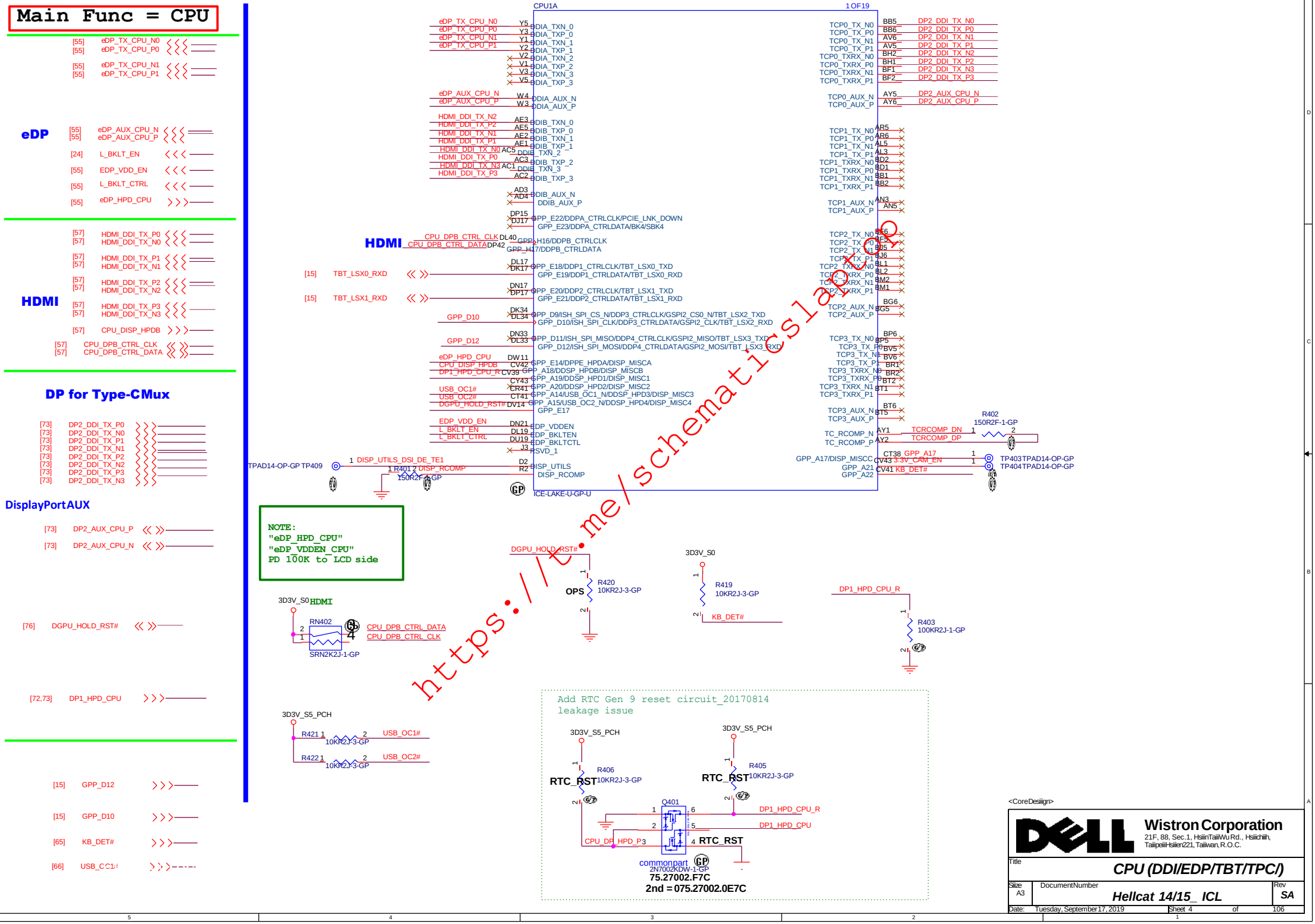
Main Func = CPU



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Wistron Corporation
21F, 88, Sec.1, HsiihTaiiWu Rd., Hsiichih,
TaiipeiiHsiien221, Taiiwan, R.O.C.

Title: CPU (DDI/EDP/TBT/TPC/)

Size	DocumentNumber	Rev
A3	Hellcat 14/15_ ICL	SA

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DDR4 ball type: Non-Interleaved Type

Channel A

M_A_DQ0 [12] … M_A_DQ63 [12]

M_A_A0 [12] … M_A_A16 [12]

M_A_DQS_DP0 … M_A_DQS_DP7 [12]

M_A_DQS_DN0 … M_A_DQS_DN7 [12]

[12] M_A_CLK#0 [12] M_A_DIMA_ODT0

[12] M_A_CLK0 [12] M_A_DIMA_ODT1

[12] M_A_CKE0 [12] M_A_ACT_N

[12] M_A_CKE1 [12] M_A_PARITY

[12] M_A_ALERT_N

[12] M_A_CS#0 M_A_CLK1 [12]

M_A_CLK#1 [12]

M_A_CS#1 [12]

[12] M_A_BA0

[12] M_A_BA1

[12] M_A_BG0

[12] M_A_BG1

Channel B

M_B_DQ0 [13] … M_B_DQ63 [13]

M_B_A0 [13] … M_B_A16 [13]

M_B_DQS_DP0 … M_B_DQS_DP7 [13]

M_B_DQS_DN0 … M_B_DQS_DN7 [13]

[13] M_B_CLK#0 [13] M_B_DIMB_ODT0

[13] M_B_CLK0 [13] M_B_DIMB_ODT1

[13] M_B_ACT_N

[13] M_B_CKE1 [13] M_B_PARITY

[13] M_B_CKE0 [13] M_B_ALERT_N

[13] M_B_CS#0 M_B_CLK1 [13]

M_B_CLK#1 [13]

[13] M_B_CS#1 [13]

[13] M_B_BA0

[13] M_B_BA1

[13] M_B_BG0

[13] M_B_BG1

[12] V_SM_VREF_CNTA

[13] V_SM_VREF_CNTB

[12,13] DDR4_DRAMRST#

CPU1B (2OF 19)

M_A_DQ0 … M_A_DQ63 → DDRA_DQ0_0/DDR0_DQ0_0 … DDRB_DQ3_7/DDR0_DQ7_7

DDRA_CLK_N/DDR0_CLK_N_0 BL48 M_A_CLK#0

DDRA_CLK_P/DDR0_CLK_P_0 BL47 M_A_CLK0

DDRB_CLK_N/DDR0_CLK_N_1 BF42 M_A_CLK1

DDRB_CLK_P/DDR0_CLK_P_1 BF43

DDRA_CKE0/DDR0_CKE0 BG49 M_A_CKE0

DDRA_CKE1/NC BG47

DDRB_CKE0/NC BF38

DDRB_CKE1/DDR0_CKE1 BF41 M_A_CKE1

DDRA_CS_0/DDR0_CS_N_0 BM38 M_A_CS#0

DDRA_CS_1/NC BM42

DDRB_CS_0/NC BP42

DDRB_CS_1/DDR0_CS_N_1 BG42 M_A_CS#1

DDRB_CA4/DDR0_BA0 BM43 M_A_BA0

NC/DDR0_BA1 BG39 M_A_BA1

NC/DDR0_BG1 BM49 M_A_BG0

DDRA_CA5/DDR0_BG0 BD47 M_A_BG1

NC/DDR0_MA0 BB48 M_A_A0

NC/DDR0_MA1 BL49 M_A_A1

DDRB_CA5/DDR0_MA2 BG38 M_A_A2

NC/DDR0_MA3 BL45 M_A_A3

NC/DDR0_MA4 BJ46 M_A_A4

DDRA_CA0/DDR0_MA5 BE48 M_A_A5

DDRA_CA2/DDR0_MA6 BL44 M_A_A6

DDRA_CA4/DDR0_MA7 BG45 M_A_A7

DDRA_CA3/DDR0_MA8 BG47 M_A_A8

DDRA_CA1/DDR0_MA9 BE47 M_A_A9

NC/DDR0_MA10 BJ38 M_A_A10

NC/DDR0_MA11 BB47 M_A_A11

NC/DDR0_MA12 BE48 M_A_A12

DDRB_CA0/DDR0_MA13 BG39 M_A_A13

DDRB_CA2/DDR0_MA14W E# BG43 M_A_A14

DDRB_CA1/DDR0_MA15CAS# BH42 M_A_A15

DDRB_CA3/DDR0_MA16RAS# BH31 M_A_A16

NC/DDR0_ODT_0 BJ39 M_A_DIMA_ODT0

NC/DDR0_ODT_1 BB45 M_A_DIMA_ODT1

DDRA_DQSN_0/DDR0_DQSN_0 BY47 M_A_DQS_DN0

DDRA_DQSP_0/DDR0_DQSP_0 BY46 M_A_DQS_DP0

DDRA_DQSN_1/DDR0_DQSN_1 CC51 M_A_DQS_DN1

DDRA_DQSP_1/DDR0_DQSP_1 CE51 M_A_DQS_DP1

DDRA_DQSN_2/DDR0_DQSN_2 BR47 M_A_DQS_DN2

DDRA_DQSP_2/DDR0_DQSP_2 BR46 M_A_DQS_DP2

DDRA_DQSN_3/DDR0_DQSN_3 BV51 M_A_DQS_DN3

DDRA_DQSP_3/DDR0_DQSP_3 BW 41 M_A_DQS_DP3

DDRB_DQSN_0/DDR0_DQSN_4 AV46 M_A_DQS_DN4

DDRB_DQSP_0/DDR0_DQSP_4 AV47 M_A_DQS_DP4

DDRB_DQSN_1/DDR0_DQSN_5 AY51 M_A_DQS_DN5

DDRB_DQSP_1/DDR0_DQSP_5 BB41 M_A_DQS_DP5

DDRB_DQSN_2/DDR0_DQSN_6 AN46 M_A_DQS_DN6

DDRB_DQSP_2/DDR0_DQSP_6 AN47 M_A_DQS_DP6

DDRB_DQSN_3/DDR0_DQSN_7 AR41 M_A_DQS_DN7

DDRB_DQSP_3/DDR0_DQSP_7 AT41 M_A_DQS_DP7

NC/DDR0_PAR BF39 M_A_PARITY

NC/DDR0_ACT# BE49 M_A_ACT_N

NC/DDR0_ALERT# BD46 M_A_ALERT_N

RSVD_73 M38

DDR0_VREF_CA C44 V_SM_VREF_CNTA

DDR1_VREF_CA B45 V_SM_VREF_CNTB

DDR_VTT_CTL M39 VTT_CNTL

DRAM_RESET# AV47 SM_DRAMRST#_CPU

R506 2 … R508 2 → 100R2F-L1-GP-U → SM_RCOMP_0/1/2

SM_RCOMP_0 D47

DDR_RCOMP_0 E46

DDR_RCOMP_1 C47

DDR_RCOMP_2

ICE-LAKE-U-GP-U

CPU1C (3OF 19)

M_B_DQ0 … M_B_DQ63 → DDRC_DQ0_0/DDR1_DQ0_0 … DDRD_DQ3_7/DDR1_DQ7_7

DDRC_CLK_N/DDR1_CLK_N_1 Y47 M_B_CLK#0

DDRC_CLK_P/DDR1_CLK_P_1 M45 M_B_CLK0

DDRD_CLK_N/DDR1_CLK_N_1 M42 M_B_CLK#1

DDRD_CLK_P/DDR1_CLK_P_1 V51 M_B_CLK1

DDRC_CKE0/DDR1_CKE0 U45 M_B_CKE0

DDRC_CKE1/NC M41

DDRD_CKE0/NC P43 M_B_CKE1

DDRD_CKE1/DDR1_CKE1

DDRC_CS_0/DDR1_CS_N_0 V42 M_B_CS#0

DDRC_CS_1/NC V39

DDRD_CS_0/NC Y39

DDRD_CS_1/DDR1_CS_N_1 T39 M_B_CS#1

DDRD_CA4/DDR1_BA0 T42 M_B_BA0

NC/DDR1_BA1 R45 M_B_BG0

DDRC_CA5/DDR1_BG0 N47 M_B_BG1

NC/DDR1_BG1

NC/DDR1_MA0 Y49 M_B_A0

NC/DDR1_MA1 U49 M_B_A1

DDRD_CA5/DDR1_MA2 Y45 M_B_A2

NC/DDR1_MA3 U47 M_B_A3

NC/DDR1_MA4 R49 M_B_A4

DDRC_CA0/DDR1_MA5 U43 M_B_A5

DDRC_CA2/DDR1_MA6 M47 M_B_A6

DDRC_CA4/DDR1_MA7 M45 M_B_A7

DDRC_CA3/DDR1_MA8 R47 M_B_A8

DDRC_CA1/DDR1_MA9 P51 M_B_A9

NC/DDR1_MA10 N49 M_B_A10

NC/DDR1_MA11 R49 M_B_A11

NC/DDR1_MA12 Y41 M_B_A12

DDRD_CA0/DDR1_MA13 V41 M_B_A13

DDRD_CA2/DDR1_MA14W E# P42 M_B_A14

DDRD_CA1/DDR1_MA15CAS# V43 M_B_A15

DDRD_CA3/DDR1_MA16RAS# M_B_A16

NC/DDR1_ODT_0 V38 M_B_DIMB_ODT0

NC/DDR1_ODT_1 M_B_DIMB_ODT1

DDRC_DQSN_0/DDR1_DQSN_0 AH47 M_B_DQS_DN0

DDRC_DQSP_0/DDR1_DQSP_0 AJ47 M_B_DQS_DP0

DDRC_DQSN_1/DDR1_DQSN_1 AL47 M_B_DQS_DN1

DDRC_DQSP_1/DDR1_DQSP_1 AC47 M_B_DQS_DP1

DDRC_DQSN_2/DDR1_DQSN_2 AC45 M_B_DQS_DN2

DDRC_DQSP_2/DDR1_DQSP_2 AE51 M_B_DQS_DP2

DDRC_DQSN_3/DDR1_DQSN_3 AD51 M_B_DQS_DN3

DDRC_DQSP_3/DDR1_DQSP_3 AH47 M_B_DQS_DP3

DDRD_DQSN_0/DDR1_DQSN_4 H46 M_B_DQS_DN4

DDRD_DQSP_0/DDR1_DQSP_4 G47 M_B_DQS_DP4

DDRD_DQSN_1/DDR1_DQSN_5 J47 M_B_DQS_DN5

DDRD_DQSP_1/DDR1_DQSP_5 C42 M_B_DQS_DP5

DDRD_DQSN_2/DDR1_DQSN_6 D47 M_B_DQS_DN6

DDRD_DQSP_2/DDR1_DQSP_6 D36 M_B_DQS_DP6

DDRD_DQSN_3/DDR1_DQSN_7 C36 M_B_DQS_DN7

DDRD_DQSP_3/DDR1_DQSP_7 M_B_DQS_DP7

NC/DDR1_PAR P38 M_B_PARITY

NC/DDR1_ACT# M48 M_B_ACT_N

NC/DDR1_ALERT# M49 M_B_ALERT_N

ICE-LAKE-U-GP-U

VTT_CNTL circuit

3D3V_S5 → R508 10KR2J-3-GP → Q501 (G/D/S) → VTT_CNTL_CPU_G

Q502_G → Q502 2N7002K-2-GP → VTT_CNTL

3D3V_S0 → R520 10KR2J-3-GP → Q502 D

PJA138KA-GP

084.00138.0A31

2nd =84.05067.031

84.2N702.J31

1D2V_S3

1D2V_S3 → R510 470R2F-GP → SM_DRAMRST#_CPU

R511 0R2J-2-GP → 2 DDR4_DRAMRST#

C501 SCD1U16V2KX-3GP

DY

<CoreDesign>

緯創資通 Wistron Corporation

21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

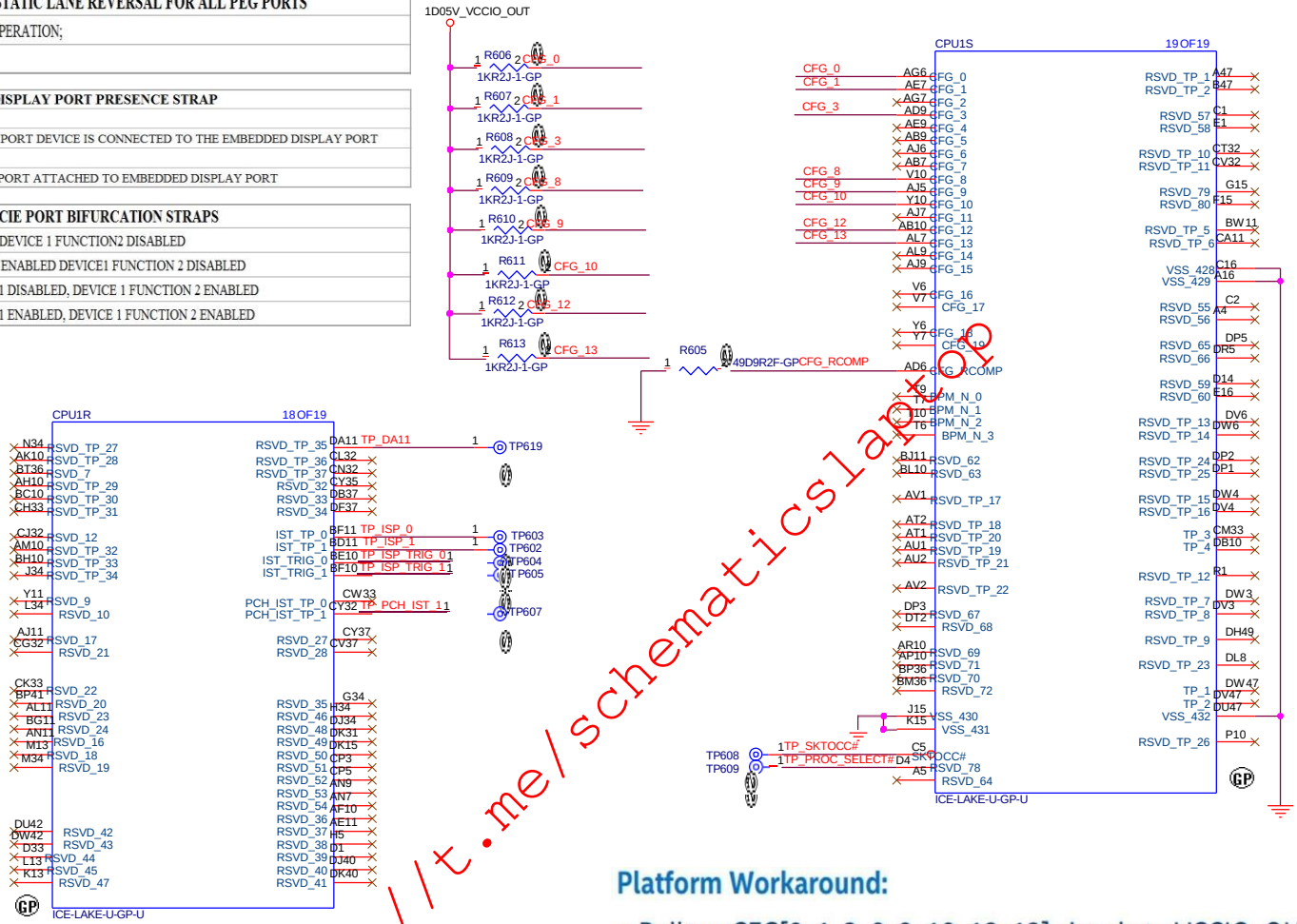
Size: A2 | Document Number: Hellcat 14/15_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 5 of 108

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED



Platform Workaround:

- Pull-up CFG[0, 1, 3, 8, 9, 10, 12, 13] signals to VCCIO_OUT
- Different configuration options:
  1. Add 1K Ohm pull-up resistors to each of the CFG[0, 1, 3, 8, 9, 10, 12, 13] signals
  2. Tie all eight CFG[0, 1, 3, 8, 9, 10, 12, 13] signals together with a single 100 Ohm pull-up resistor; only use this option when CFG signals are not routed to MIPI60 debug connector
  3. Use 270 Ohm resistor to pull up 3 or 4 CFG signals together through a single resistor, and/or 470 Ohm resistor to pull up 2 CFG signals through a single resistor; only use this option when CFG signals are not routed to MIPI60 debug connector

Table 5-76. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall.	Pull Up	1K Ohm
CFG1,8,9,10,12,13	RSVD	Pull Up	1K Ohm
CFG2,3,5,6,7,11,14,15	RSVD	No termination	N/A
CFG4	CFG[4]: eDP enable: – 1 = Disabled. – 0 = Enabled.	Pull Down	1K Ohm
Note: Refer Chapter 13, "Platform Debug and Test Hooks" for debug connectivity guidelines.			

<CoreDesiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih, TaiipeiiHsiien221, Taiiwan, R.O.C.

Title: CPU (CFG/IST)

Size: A3 | DocumentNumber: Hellcat 14/15_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 6 of 106

Main Func = CPU

[46] SVID_ALERT#_CPU
[46] SVID_CLK_CPU
[46] SVID_DATA_CPU

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE

1V_CPU_CORE

CPU1L 12 OF19

A19	VCCIN_1	VCCIN_52	CJ35
AC12	VCCIN_2	VCCIN_53	CK10
V13	VCCIN_3	VCCIN_54	J32
W12	VCCIN_4	VCCIN_55	CL34
Y13	VCCIN_5	VCCIN_56	CL35
K29	VCCIN_6	VCCIN_57	CN34
K31	VCCIN_7	VCCIN_58	CN35
B19	VCCIN_8	VCCIN_59	CP33
B23	VCCIN_9	VCCIN_60	CR34
B27	VCCIN_10	VCCIN_61	A29
B29	VCCIN_11	VCCIN_62	CR35
BN10	VCCIN_12	VCCIN_63	CT33
BP11	VCCIN_13	VCCIN_64	CT34
BP9	VCCIN_14	VCCIN_65	CT35
BR10	VCCIN_15	VCCIN_66	CU33
BT11	VCCIN_16	VCCIN_67	D19
A21	VCCIN_17	VCCIN_68	D21
BT9	VCCIN_18	VCCIN_69	D23
BU10	VCCIN_19	VCCIN_70	D24
BV36	VCCIN_20	VCCIN_71	D27
BV9	VCCIN_21	VCCIN_72	AA12
BW 10	VCCIN_22	VCCIN_73	D29
BW 36	VCCIN_23	VCCIN_74	F19
BW 9	VCCIN_24	VCCIN_75	F21
BY10	VCCIN_25	VCCIN_76	F23
C19			F24
C23	VCCIN_26	VCCIN_77	F27
A23	VCCIN_27	VCCIN_78	F29
C27	VCCIN_28	VCCIN_79	G1
C29	VCCIN_29	VCCIN_80	G19
CA36	VCCIN_30	VCCIN_81	G23
CA9	VCCIN_31	VCCIN_82	AB1
CB10	VCCIN_32	VCCIN_83	G27
CC11	VCCIN_33	VCCIN_84	G29
CC36	VCCIN_34	VCCIN_85	H19
CC9	VCCIN_35	VCCIN_86	H23
CD10	VCCIN_36	VCCIN_87	H27
CE11	VCCIN_37	VCCIN_88	H29
A24	VCCIN_38	VCCIN_89	J18
CE34	VCCIN_39	VCCIN_90	J20
CE35	VCCIN_40	VCCIN_91	J22
CF10	VCCIN_41	VCCIN_92	J23
CF33	VCCIN_42	VCCIN_93	AB13
CG11	VCCIN_43	VCCIN_94	J26
CG34	VCCIN_44	VCCIN_95	J28
CG35	VCCIN_45	VCCIN_96	K17
CH10	VCCIN_46	VCCIN_97	K19
J30	VCCIN_47	VCCIN_98	K21
CJ11	VCCIN_48	VCCIN_99	K23
A27	VCCIN_49	VCCIN_100	K24
CJ34	VCCIN_50	VCCIN_101	K27
	VCCIN_51	VCCIN_102	M1
		VCCIN_103	U1
		VCCIN_104	

SVID_ALERT#_CPU_R H1 — VIDALERT#
SVID_CLK_CPU_R H2 — VIDSCK
SVID_DATA_CPU_R H3 — VIDSOUT

VCCIN_SENSE F17 VCCCORE_SENSE
VSSIN_SENSE G17 VSSCORE_SENSE

ICE-LAKE-U-GP-U

SVID DATA

1D05V_VCCST
R703 100R2F-L1-GP-U
R708 0R2J-2-GP
SVID_DATA_CPU_R — SVID_DATA_CPU

SVID ALERT

1D05V_VCCST
R701 56R2J-4-GP
R706 0R2J-2-GP
SVID_ALERT#_CPU_R — SVID_ALERT#_CPU

SVID CLOCK

1D05V_VCCST
R702 DY 43R2F-2-GP
R709 0R2J-2-GP
SVID_CLK_CPU_R — SVID_CLK_CPU

Layout note:

3.Length matchin 25mil, and close SOC in 2inch "

1V_CPU_CORE
R704 100R2F-L1-GP-U — VCCCORE_SENSE
R705 100R2F-L1-GP-U — VSSCORE_SENSE

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<CoreDesign>

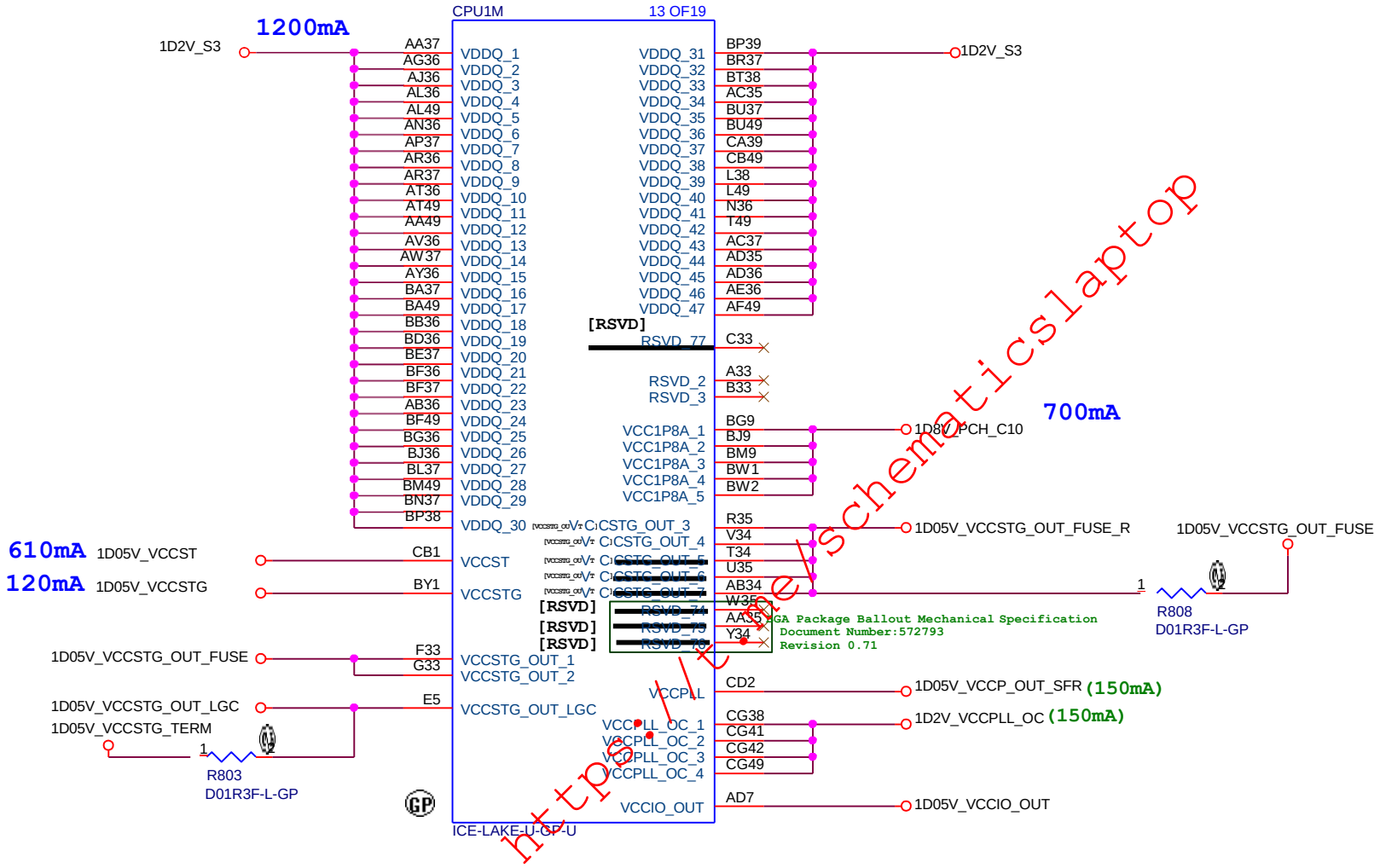
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN/VID)

Size	Document Number	Rev
A4	Hellcat 14/15_ ICL	SA

Date: Tuesday, September 17, 2019 Sheet 7 of 106

Main Func = CPU



<Core Design>

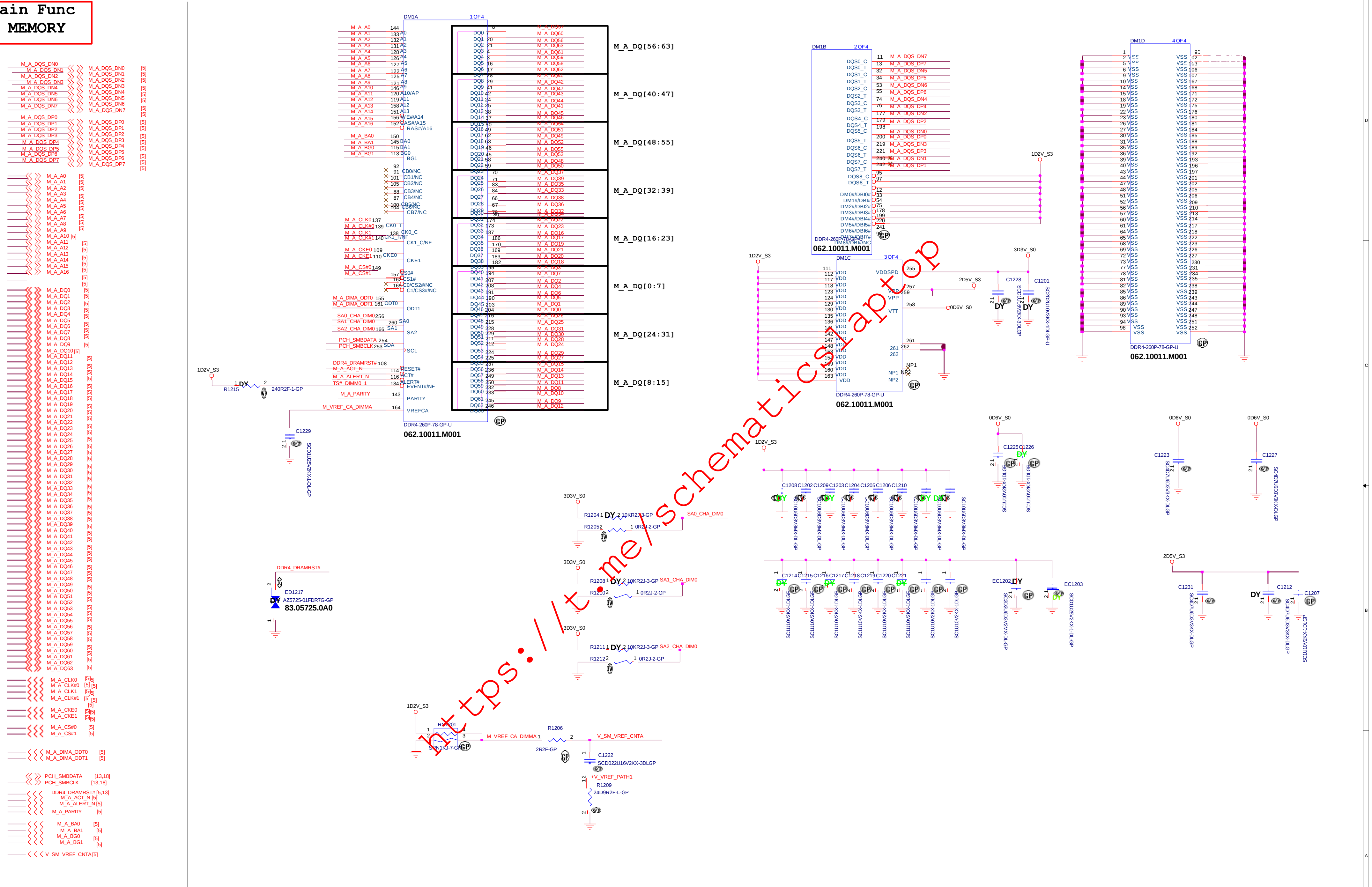
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VDDQ/VCC/VCCST/VCCSTG)**

Size	Document Number	Rev
A4	Hellcat 14/15_ ICL	SA

Date: Tuesday, September 17, 2019 Sheet 8 of 106

Main Func = MEMORY



<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

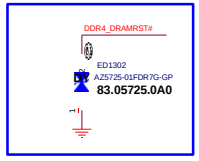
Title: **DDR3-SODIMM1**

Size	Document Number	Rev
A2	Hellcat 14/15_ ICL	SA

Date: Tuesday, September 17, 2019 — Sheet 12 of 106

Main Func
= MEMORY

0614 Layout HT

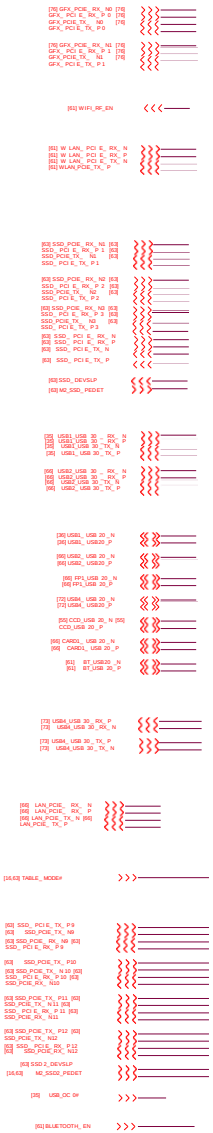


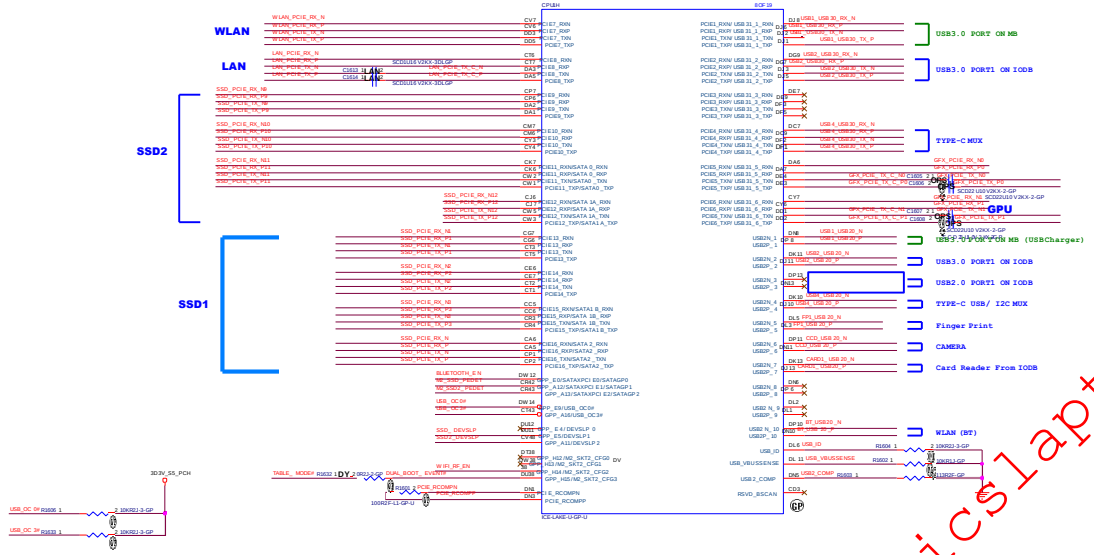
<Core Design>
Wistron Corporation
2F., 88., Sec.1., HsinTaiWu Rd., Hsichih,
Taipei Hsien221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Hellcat 14/15_ ICL	SA

Date: Tuesday, September17, 2019 Sheet 13 of 106





High Speed I/O (HSIO) Lane Multiplexing in Ice Lake U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1 / Gen2 #1	USB3.1 Gen1 / Gen2 #2	USB3.1 Gen1 / Gen2 #3	USB3.1 Gen1 / Gen2 #4	USB3.1 Gen1 / Gen2 #5	USB3.1 Gen1 / Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GBE	GBE	GBE		SATA #0	SATA #1	GBE	GBE	SATA #2	SATA #3
PCIe*Remap Support	No Support				No Support				Yes							

CY20 Port Mapping											
Mockingbird N	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	M.2 SSD2	M.2 SSD1		
Mockingbird V	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	LAN	M.2 SSD2	M.2 SSD1		
Hellcat 14	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	NC	M.2 SSD1		
Hellcat 15	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	NC	M.2 SSD1		

USB2.0 (10 Ports)

USB2 #1	USB2 #2	USB2 #3	USB2 #4	USB2 #5	USB2 #6	USB2 #7	USB2 #8	USB2 #9	USB2 #10
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT

DDI Ports Availability for U-Processor Lines

DDI A [eDP]	DDI B [DP / HDMI]	TCP0 (DDI C) [DP / HDMI]	TCP1 (DDI D) [DP / HDMI]	TCP2 (DDI E) [DP / HDMI]	TCP3 (DDI F) [DP / HDMI]
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC

緯創資通 WistronCorporation
CPU (PCIE/SATA/USB)
Hellcat 14/15 ICL
SA
Tuesday, September 17, 2019

Main Func = PCH

[40,54,55,81] PM_SLP_S3#
[40,51,66] PM_SLP_S4#
[40] SIO_SLP_S0#
[17,24] SYS_PWROK
[24] SIO_PWRBTN#
[24,26] IMVP_VR_ON
[18,64] PM_RSMRST#
[44] AC_IN#
[40] CPU_C10_GATE#
[53] SIO_SLP_SUS#
[15] GPD7
[15] PCH_DPWROK
[17,24] SYS_PWROK
[61,63,66,76,91] PLT_RST#
[24,40,44,46] VCCST_PWRGD
[44,46] PWR_IMVP_PWRGD
[25,53] 3V_5V_PWRGD

CPU1K — 11 OF 19 — ICE-LAKE-U-GP-U

3V SELECT STRAP
LOW → 3.3V +/-5%
HIGH → 3.0V +/-5%

20190424(EVT)
Reverse R1705, R1739 by Dell Andy

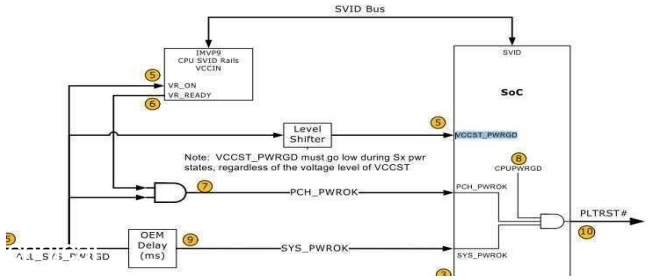
Q1701 PJT138KA-GP — 075.00138.0A7C

Q1702 common part — 2N7002KDW-1-GP — 75.27002.F7C

D1701 RB520S30-GP — 83.R2003.A8M — 2nd =083.52030.008F

SPI Voltage Configu-ration

SVID Bus



Wistron Corporation

CPU (PMU)

Hellcat 14/15_ ICL

SA

Main Func = PCH

SPI ROM
[24,25,91] SPI_CLK_ROM
[24,25,91] SPI_SI_ROM
[24,25,91] SPI_SO_ROM
[24,25] SPI_WP_ROM
[24,25] SPI_HOLD_ROM
[24,25] SPI_CS_ROM_N0
[24,25] SPI_CS_ROM_N1
[15] SPI_HOLD_CPU

TPM
[91] SPI_CS_CPU_N2
[91] TPM_SPI_IRQ#

WLAN
[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] WLAN_CLKREQ_CPU_N

ESPI
[24,68] ESPI_IO0
[24,68] ESPI_IO1
[24,68] ESPI_IO2
[24,68] ESPI_IO3
[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK

OTHER
[12,13] PCH_SMBCLK
[12,13] PCH_SMBDATA
[12,13] SML0_SMBCLK
[12,13] SML0_SMBDATA
[15] GPP_C2
[15] GPP_C5
[24,61] SUS_CLK
[66] LAN_CLK_CPU_N
[66] LAN_CLK_CPU_P
[66] LAN_CLKREQ_CPU_N
[64] SATA_LED#
[24,25] RTCRST_ON
[15] SPI_SI_CPU
[15] SPI_WP_CPU

GPU
[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#

SSD
[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N
[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD2_CLKREQ_CPU_N

[17,64] PM_RSMRST#
[24] EC_PCH_SPI_EN

CPU1E 5OF19
SPI_CLK_CPU_R R18201 49D9R2F-GP SPI_CLK_CPU DB42 SPI0_CLK
SPI_SI_CPU_R R18211 49D9R2F-GP SPI_SI_CPU DD43 SPI0_MOSI
SPI_SO_CPU_R R18221 49D9R2F-GP SPI_SO_CPU DF43 SPI0_MISO
SPI_WP_CPU_R R18251 49D9R2F-GP SPI_WP_CPU DF42 SPI0_IO2
SPI_HOLD_CPU_R R18261 49D9R2F-GP SPI_HOLD_CPU DD41 SPI0_IO3
SPI_CS_CPU_N1 DB43 SPI0_CS0#
SPI_CS_CPU_N2 DB41 SPI0_CS1#
SPI0_CS2#
SPI0
Strap Pin GPP_C2/SMBALERT#
GPP_C0/SMBCLK DK27 CPU_SMB_SCL
GPP_C1/SMBDATA DK24 GPP_C2
SMBUS
GPP_C3/SML0CLK DK24 SML0_SMBCLK
GPP_C4/SML0DATA DK22 GPP_C5
SML0
Strap Pin GPP_C5/SML0ALERT#
GPP_C6/SML1CLK/SUSW ARN_N/SUSPW RDNACK DK22 CPU_SMB_SDA_P1
GPP_C7/SML1DATA/SUSACK# DN22 CPU_SMB_SCL_P1
SML1
TPM_SPI_IRQ# DV16 GPP_E11/SPI1_CLK/BK1/SBK1
DU18 GPP_E13/SPI1_MOSI/BK3/SBK3
DT18 GPP_E12/SPI1_MISO/BK2/SBK2
SATA_LED# DW 18 GPP_E1/SPI1_IO2
DW 16 GPP_E2/SPI1_IO3
DU16 GPP_E10/SPI1_CS_N/BK0/SBK0
GPP_E8/SATALED#/SPI1_CS1#
SPI1
TPAD14-OP-GP TP1809 1 CL_CLK DV19 CL_CLK
TPAD14-OP-GP TP1810 1 CL_DATA DW 19 CL_DATA
TPAD14-OP-GP TP1811 1 CL_RST# DT19 CL_RST#
MISC
GPP_A5/ESPI_CLK CN45 PCH_ESPI_CLK
GPP_A0/ESPI_IO0 CN48 PCH_ESPI_IO1
GPP_A1/ESPI_IO1 CN49 PCH_ESPI_IO2
GPP_A2/ESPI_IO2 CN47 PCH_ESPI_IO3
GPP_A3/ESPI_IO3 CT45 ESPI_CS#
GPP_A4/ESPI_CS# CN46 ESPI_RESET#
GPP_A6/ESPI_RESET#
ESPI
ICE-LAKE-U-GP-U

3D3V_S5_PCH
CPU_SMB_SCL R18041 2 1KR2J-1-GP
CPU_SMB_SDA R18051 2 1KR2J-1-GP
SML0_SMBCLK R18061 2 499R2F-2-GP
SML0_SMBDATA R18071 2 499R2F-2-GP
CPU_SMB_SCL_P1 R18101 2 1KR2J-1-GP
CPU_SMB_SDA_P1 R18111 2 1KR2J-1-GP
SPI_CLK_CPU R181 2 10KR2J-1-GP

3D3V_S0 R1808 1 2 SATA_LED# 10KR2J-3-GP

If support TPM change to 5R

3D3V_S0 RN1802 SRN1KJ-7-GP
CPU_SMB_SDA Q1802 PCH_SMBDATA
2N7002KDW-1-GP
CPU_SMB_SCL PCH_SMBCLK
75.27002.F7C

PCH_ESPI_CLK R1834 33R2F-3-GP ESPI_CLK
PCH_ESPI_IO0 R1835 0R2J-2-GP ESPI_IO0
PCH_ESPI_IO1 R1836 0R2J-2-GP ESPI_IO1
PCH_ESPI_IO2 R1837 0R2J-2-GP ESPI_IO2
PCH_ESPI_IO3 R1839 0R2J-2-GP ESPI_IO3
Intel requst set as PDG .

ESPI_CLK RC18011 2 33P50V2JN-2-GP
DY
RF Reserve

XTL_32K_X1_CPU R1847 0R2J-2-GP XTL_32K_X1_CPU_R
XTL_32K_X2_CPU R1849 0R2J-2-GP XTL_32K_X2_CPU_R
R1844 2 10MR2J-2-GP
X1803 XTAL-32768KHZ-88-GP
C1810 SC15P50V2JN-DL-GP C1809 SC12P50V2JN-DL-GP
082.30003.0191

	C1810(Cg)	C1809(Cd)
EPSON 082.30003.0191	15pF	12pF
SEIKO 082.30003.0301	12pF	15pF
NDK 082.30003.0221	15pF	12pF

CPU1J 10OF19
GPU
WLAN
LAN
SSD1
GFX_CLK_CPU_N CJ33 CLKOUT_PCIE_N0 GPP_D5/SRCCLKREQ0#
GFX_CLK_CPU_P CJ35 CLKOUT_PCIE_P0
CLK_PCIE_PEG_REQ# DK33
WLAN_CLK_CPU_N CL2 CLKOUT_PCIE_N1
WLAN_CLK_CPU_P CL1 CLKOUT_PCIE_P1 GPP_D6/SRCCLKREQ1#
WLAN_CLKREQ_CPU_N DN34
LAN_CLK_CPU_N CL3 CLKOUT_PCIE_N2
LAN_CLK_CPU_P CL5 CLKOUT_PCIE_P2 GPP_D7/SRCCLKREQ2#
LAN_CLKREQ_CPU_N DP34
CK3 CLKOUT_PCIE_N3
CP36 CLKOUT_PCIE_P3 GPP_D8/SRCCLKREQ3#
SSD_CLK_CPU_N CJ2 CLKOUT_PCIE_N4
SSD_CLK_CPU_P CJ1 CLKOUT_PCIE_P4 GPP_R10/SRCCLKREQ4#
SSD_CLKREQ_CPU_N DN40
ICE-LAKE-U-GP-U
CLKOUT_PCIE_N5 CF5 SSD2_CLK_CPU_N
CLKOUT_PCIE_P5 CF3 SSD2_CLK_CPU_P
GPP_H11/SRCCLKREQ5# CF40 SSD2_CLKREQ_CPU_N
SSD2
RTCX1 DL48 XTL_32K_X1_CPU
RTCX2 DL49 XTL_32K_X2_CPU
RTCRST# DT47 RTC_RST#
SRTCRST# DK46 SRTC_RST#
GPD8/SUSCLK DF49 SUS_CLK
XTAL_IN DW 1 XTL_38D4M_X1_CPU
XTAL_OUT DU8 XTL_38D4M_X2_CPU
XCLK_BIASREF DP36 XCLK_BIASREF R1823 1 2 60D4R2F-GP
SUS_CLK R1812 1 DY 2 100KR2J-1-GP

3D3V_S0 RN1805 SRN10KJ-6-GP
LAN_CLKREQ_CPU_N
CLK_PCIE_PEG_REQ#
WLAN_CLKREQ_CPU_N
SSD2_CLKREQ_CPU_N
R18011 2 SSD_CLKREQ_CPU_N 10KR2J-3-GP

XTL_38D4M_X1_CPU R1850 2 0R2J-2-GP XTL_38D4M_X1_CPU_R
C1805 SC15P50V2JN-DL-GP
X1802 XTAL-38D4MHZ-18-GP
082.30040.0091
2nd = 082.30040.0161
3rd = 082.30040.0171
R1824 200KR2F-L-GP
XTL_38D4M_X2_CPU R1851 2 0R2J-2-GP XTL_38D4M_X2_CPU_R
C1806 SC15P50V2JN-DL-GP

RTC_AUX_S5
RN1801 SRN20KJ-1-GP
RTCRST_ON
EC1804 SCD1U16V3KX-3GP
RTC_RST R1816 20K2F-3-GP
Q1803 RTC_RST 2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.D31
3rd = 84.07002.I31
C1808 SC1U10V2KX-1GLGP
G1801 GAP-OPEN
C1807 SC1U10V2KX-1DLGP
SRTC_RST#
RTC_RST#
(#514849)
Layout: Place at the open door area.

PCH_SPI_EN_Q
SPI_CLK_ROM Q1804 SPI_CLK_CPU_R
PJE8408-R1-00001-GP
084.08408.0031

PCH_SPI_EN_Q
SPI_SI_ROM Q1805 SPI_SI_CPU_R
PJE8408-R1-00001-GP
084.08408.0031

PCH_SPI_EN_Q
SPI_WP_ROM Q1807 SPI_WP_CPU_R
PJE8408-R1-00001-GP
084.08408.0031

PCH_SPI_EN_Q
SPI_CS_ROM_N0 Q1809 SPI_CS_CPU_N0
PJE8408-R1-00001-GP
084.08408.0031

PM_RSMRST# R1802 1 DY 2 0R1J-GP
EC_PCH_SPI_EN R1803 2 0R1J-GP
PCH_SPI_EN R1814 1 2 100KR2J-1-GP

5V_S5 R1817 100KR2J-1-GP
3D3V_S5 R1815 100KR2J-1-GP
Q1811 Q1811_D_G
PCH_SPI_EN
PCH_SPI_EN_Q
2N7002KDW-1-GP
75.27002.F7C

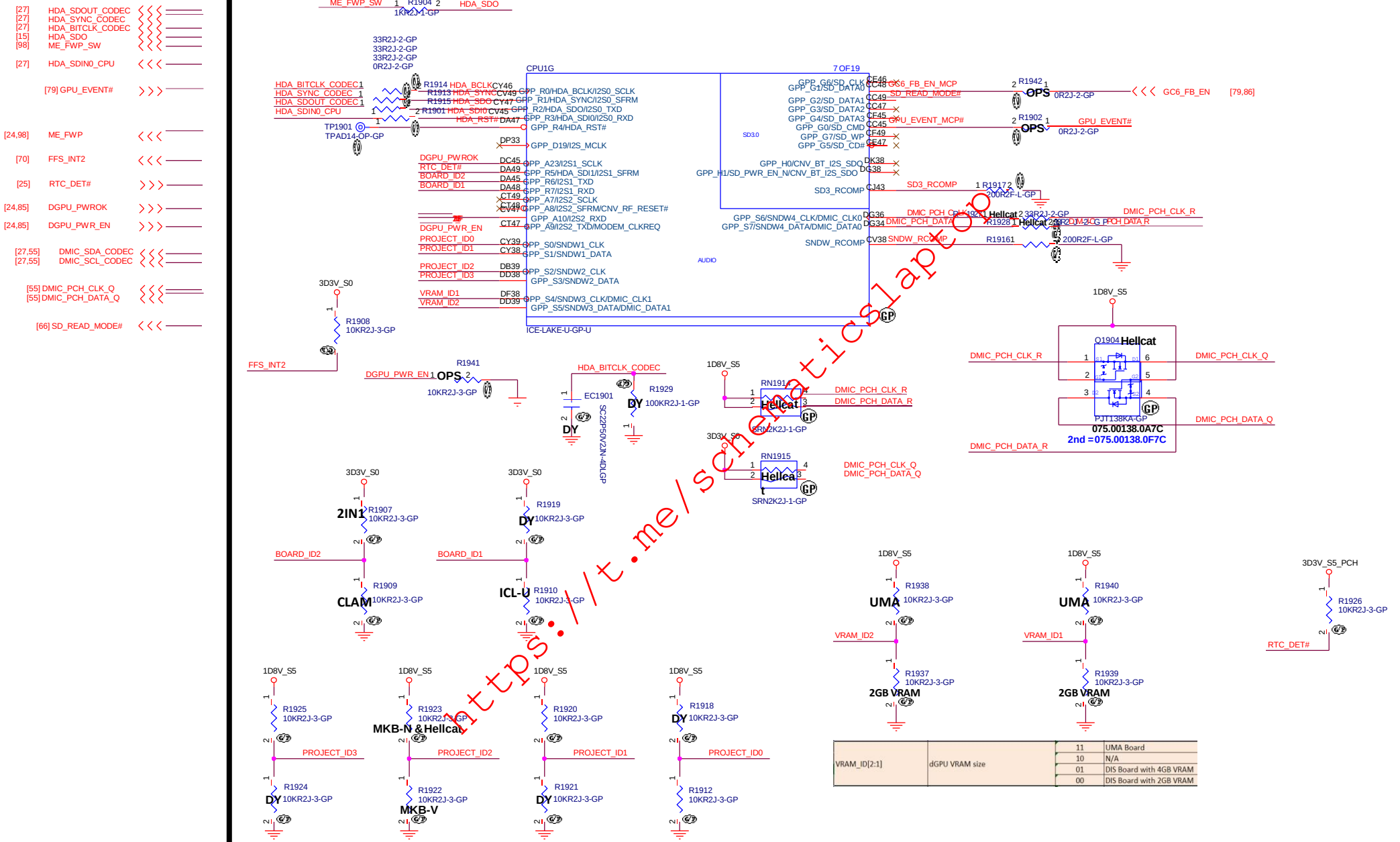
PCH_SPI_EN_Q
SPI_SO_ROM Q1806 SPI_SO_CPU_R
PJE8408-R1-00001-GP
084.08408.0031

PCH_SPI_EN_Q
SPI_HOLD_ROM Q1808 SPI_HOLD_CPU_R
PJE8408-R1-00001-GP
084.08408.0031

PCH_SPI_EN_Q
SPI_CS_ROM_N1 Q1810 SPI_CS_CPU_N1
PJE8408-R1-00001-GP
084.08408.0031

<CoreDesign>
WistronCorporation
2SF., 88, Sec. 1, HsinTaiWu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: Document Number: A2
Rev: SA
Hellcat 14/15_ ICL
Date: Tuesday, September 17, 2019
Sheet 18 of 106

Main Func = PCH



<CoreDesiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, TaiipeiiHsiien221, Taiiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size: A3 | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September17, 2019 | Sheet 19 of 106

Main Func = PCH

[91] TPM_PIRQ#
[15] GPP_B23

[65,66] CPU_I2C_SDA_P0
[65,66] CPU_I2C_SCL_P0

[55,70] SENSOR_I2C_SDA
[55,70] SENSOR_I2C_SCL

[15] NRB_BIT

[15,27] SPKR

[24,66] LID_CL_SIO#

[55] CPU_I2C_SDA_TS
[55] CPU_I2C_SCL_TS

[65] KB_LED_BL_DET

[70] FFS_INT1

[24,66] LID_CL_SIO_TAB#

[55] DBC_PANEL_EN

[70] GSEN2_INT1_C
[55] GSEN_INT1_C

[15,27] TOUCH_PANEL_INTR#

[24] NB_MODE

[24,64] MASK_SATA_LED#

[64] SATA_LED#_D

[24,64] BATT_WHITE_LED#

[68] UART_2_CRXD_DTXD
[68] UART_2_CTXD_DRXD

[24] TABLE_MODE#

CPU1F — 6 OF 19 — ICE-LAKE-U-GP-U

NRB_BIT — GPP_B16/GSPI0_CLK, GPP_B18/GSPI0_MOSI, GPP_B17/GSPI0_MISO, GPP_B15/GSPI0_CS0#
SPKR — GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
TPM_PIRQ# — GPP_B20/GSPI1_CLK, GPP_B22/GSPI1_MOSI, GPP_B21/GSPI1_MISO, GPP_B19/GSPI1_CS0#
GPP_B23 — GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#
FFS_INT1 — SBIOS_TX — TPAD14-OP-GPTP2026
UART_2_CRXD_DTXD — GPP_C20/UART2_RXD
UART_2_CTXD_DRXD — GPP_C21/UART2_TXD
TOUCH_PANEL_INTR# — GPP_C22/UART2_RTS#, GPP_C23/UART2_CTS#
Touch Screen: CPU_I2C_SDA_TS — GPP_C16/I2C0_SDA; CPU_I2C_SCL_TS — GPP_C17/I2C0_SCL
Touch Pad: CPU_I2C_SDA_P0 — GPP_C18/I2C1_SDA; CPU_I2C_SCL_P0 — GPP_C19/I2C1_SCL
GPP_H4/I2C2_SDA, GPP_H5/I2C2_SCL
DBC_PANEL_EN — GPP_H6/I2C3_SDA, GPP_H7/I2C3_SCL
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD, GPP_H9/I2C4_SCL/CNV_MFUART2_TXD

GPP_D13/ISH_UART0_RXD, GPP_D14/ISH_UART0_TXD
GPP_D15/ISH_UART0_RTS_N/GSPI2_CS1_N/IMGCLKOUT5
GPP_D16/ISH_UART0_CTS_N/CNV_WCEN
KB_LED_BL_DET
GPP_C12/UART1_RXD/ISH_UART1_RXD — SIO_EXT_WAKE#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_B5/ISH_I2C0_SDA — CN43 CPU_I2C_SDA_ISH0 — R20511
GPP_B6/ISH_I2C0_SCL — CN42 CPU_I2C_SCL_ISH0 — R20521
GPP_B7/ISH_I2C1_SDA — CN41
GPP_B8/ISH_I2C1_SCL — CL43
GPP_B9/I2C5_SDA/ISH_I2C2_SDA — CL41
GPP_B10/I2C5_SCL/ISH_I2C2_SCL — CJ39
ISH_GP0, ISH_GP1, ISH_TABLE_MODE#, ISH_KB_DISABLE, LID_CL_SIO#, LID_CL_SIO_TAB#
GPP_D0/ISH_GP0, GPP_D1/ISH_GP1, GPP_D2/ISH_GP2, GPP_D3/ISH_GP3
GPP_D17/ISH_GP4, GPP_D18/ISH_GP5, GPP_E15/ISH_GP6, GPP_E16/ISH_GP7

3D3V_S0 — RN2005 — SRN1KJ-7-GP
CPU_I2C_SDA_ISH0 — 0R2J-2-GP — SENSOR_I2C_SDA — ISH
CPU_I2C_SCL_ISH0 — 0R2J-2-GP — SENSOR_I2C_SCL

R2039 2IN1 0R2J-2-GP GSEN_INT1_C
R2037 2IN1 0R2J-2-GP GSEN2_INT1_C
R2053 2IN1 0R2J-2-GP TABLE_MODE#
R2056 2IN1 100KR2J-1-GP

For Gyro+G

3D3V_S0 — R2002 DEBUG 51KR2J-1-GP — UART_2_CRXD_DTXD
R2003 DEBUG 51KR2J-1-GP — UART_2_CTXD_DRXD

Q2001 2N7002KDW-1-GP
ISH_KB_DISABLE — NB_MODE
BATT_WHITE_LED# — MASK_SATA_LED#
SATA_LED#_D

3D3V_S5_PCH — R2001 DY 10KR2J-3-GP — SIO_EXT_WAKE#

3D3V_S5 — R2050 2IN1 10KR2J-3-GP — NB_MODE

	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
Clam Shell Mode	0	1	KB鎖住

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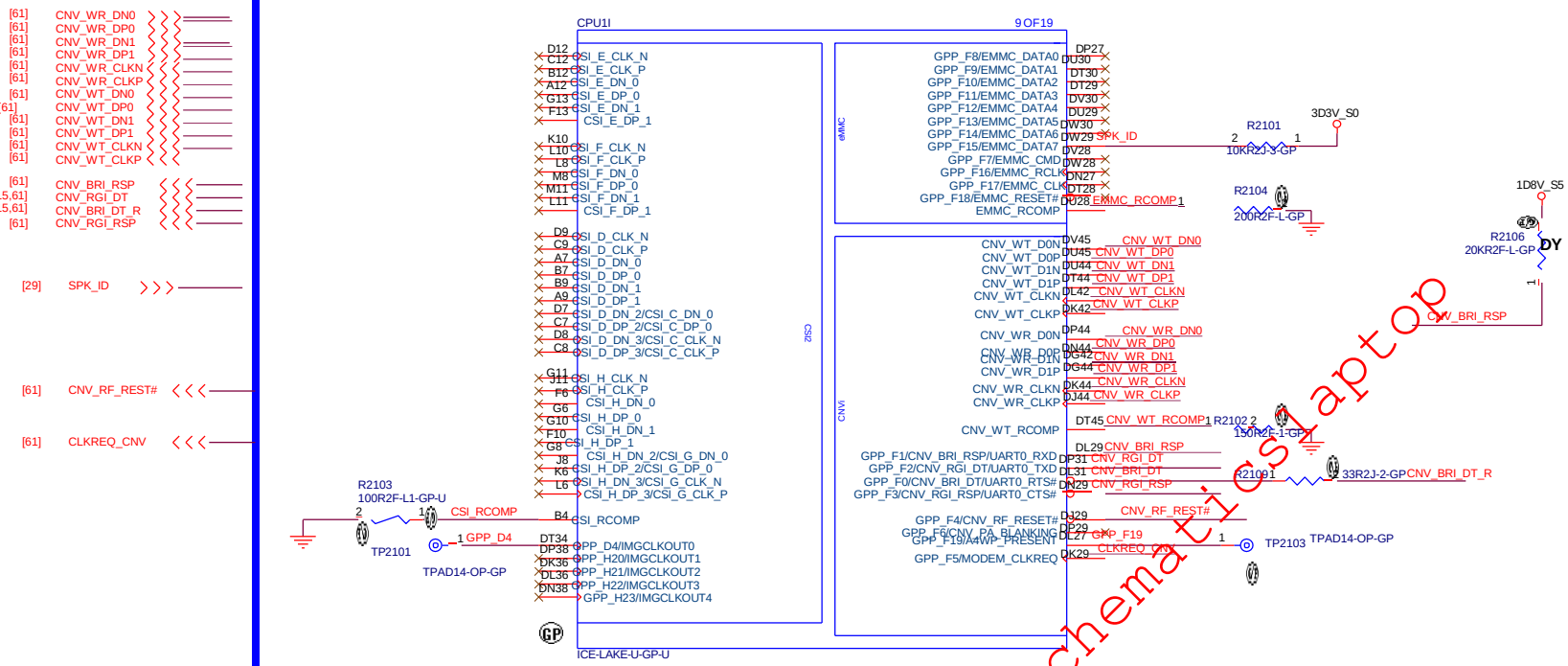
Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih, TaiipeiiHsiien221, Taiiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size	Document Number	Rev
A3	Hellcat 14/15_ ICL	SA

Date: Tuesday, September 17, 2019 Sheet 20 of 106

Main Func = PCH



<Core Design>

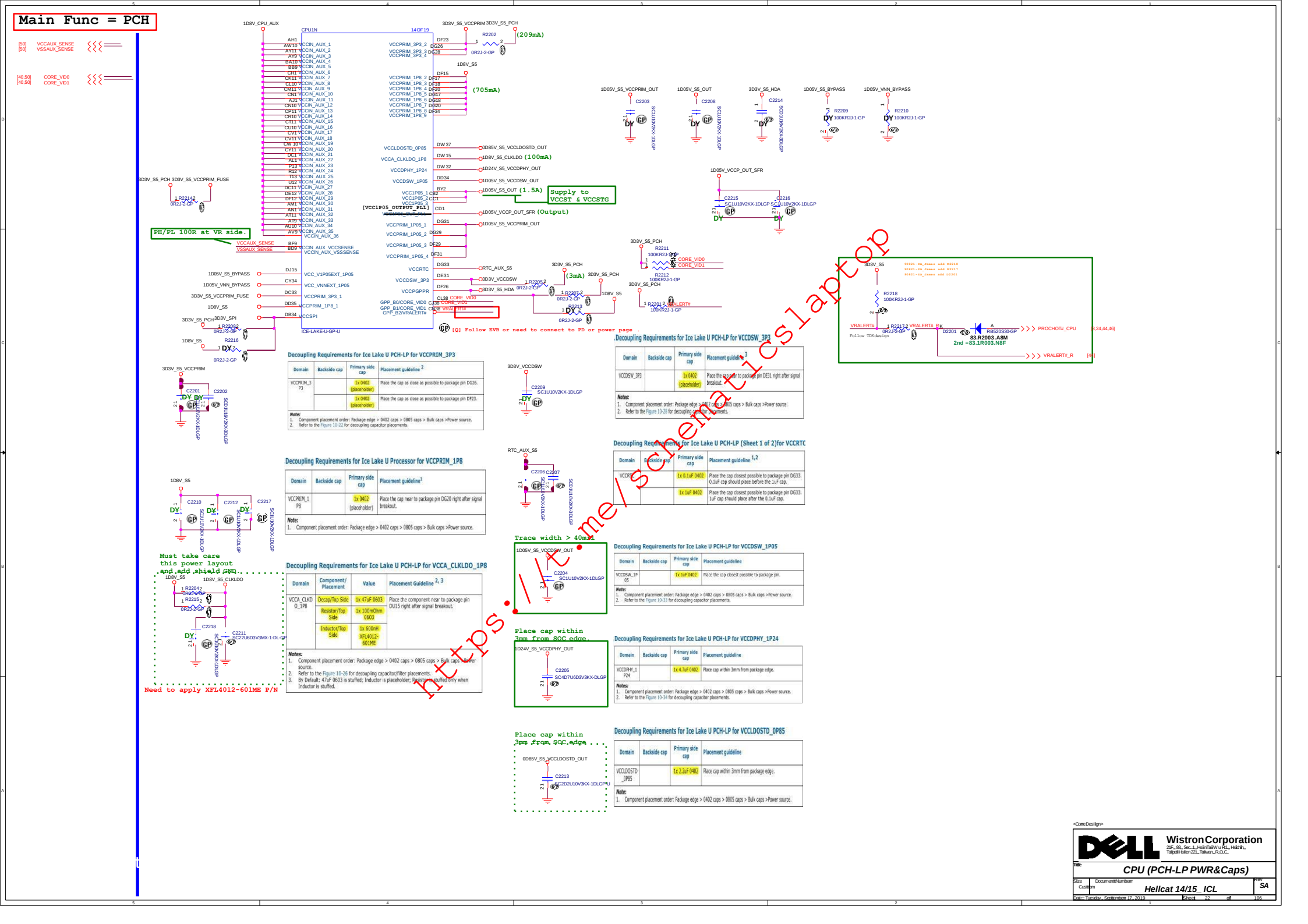
Wistron Corporation
21F, 88, Sec.1, HsiihTaiiWu Rd., Hsiichiih, TaiipeiiiHsiien221, Taiiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)

Size: A3 | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 21 of 106

Main Func = PCH



Decoupling Requirements for Ice Lake U PCH-LP for VCCPRIM_3P3

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPRIM_3P3		1x 0402 (placeholder)	Place the cap as close as possible to package pin DG26.
		1x 0402 (placeholder)	Place the cap as close as possible to package pin DF23.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-22 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPRIM_1P8

Domain	Backside cap	Primary side cap	Placement guideline [1]
VCCPRIM_1P8		1x 0402 (placeholder)	Place the cap near to package pin DG20 right after signal breakout.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.

Decoupling Requirements for Ice Lake U PCH-LP for VCCA_CLKLDO_1P8

Domain	Component/ Placement	Value	Placement Guideline [2, 3]
VCCA_CLKDO_1P8	Decap/Top Side	1x 47uF 0603	Place the component near to package pin DU15 right after signal breakout.
	Resistor/Top Side	1x 100mOhm 0603	
	Inductor/Top Side	1x 600nH XFL4012-601ME	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-26 for decoupling capacitor/filter placements.
3. By Default: 47uF 0603 is stuffed; Inductor is placeholder; Resistor is stuffed only when Inductor is stuffed.

Must take care this power layout and add shield GND.

Need to apply XFL4012-601ME P/N

Trace width > 40mil

Place cap within 3mm from SOC edge.

Place cap within 3mm from SOC edge.

Decoupling Requirements for Ice Lake U PCH-LP for VCCDSW_3P3

Domain	Backside cap	Primary side cap	Placement guideline [3]
VCCDSW_3P3		1x 0402 (placeholder)	Place the cap near to package pin DE31 right after signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-28 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U PCH-LP (Sheet 1 of 2)for VCCRTC

Domain	Backside cap	Primary side cap	Placement guideline [1,2]
VCCRTC		1x 0.1uF 0402	Place the cap closest possible to package pin DG33. 0.1uF cap should place before the 1uF cap.
		1x 1uF 0402	Place the cap closest possible to package pin DG33. 1uF cap should place after the 0.1uF cap.

Decoupling Requirements for Ice Lake U PCH-LP for VCCDSW_1P05

Domain	Backside cap	Primary side cap	Placement guideline
VCCDSW_1P05		1x 1uF 0402	Place the cap closest possible to package pin.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-33 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U PCH-LP for VCCDPHY_1P24

Domain	Backside cap	Primary side cap	Placement guideline
VCCDPHY_1P24		1x 4.7uF 0402	Place cap within 3mm from package edge.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-34 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U PCH-LP for VCCLDOSTD_0P85

Domain	Backside cap	Primary side cap	Placement guideline
VCCLDOSTD_0P85		1x 2.2uF 0402	Place cap within 3mm from package edge.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.

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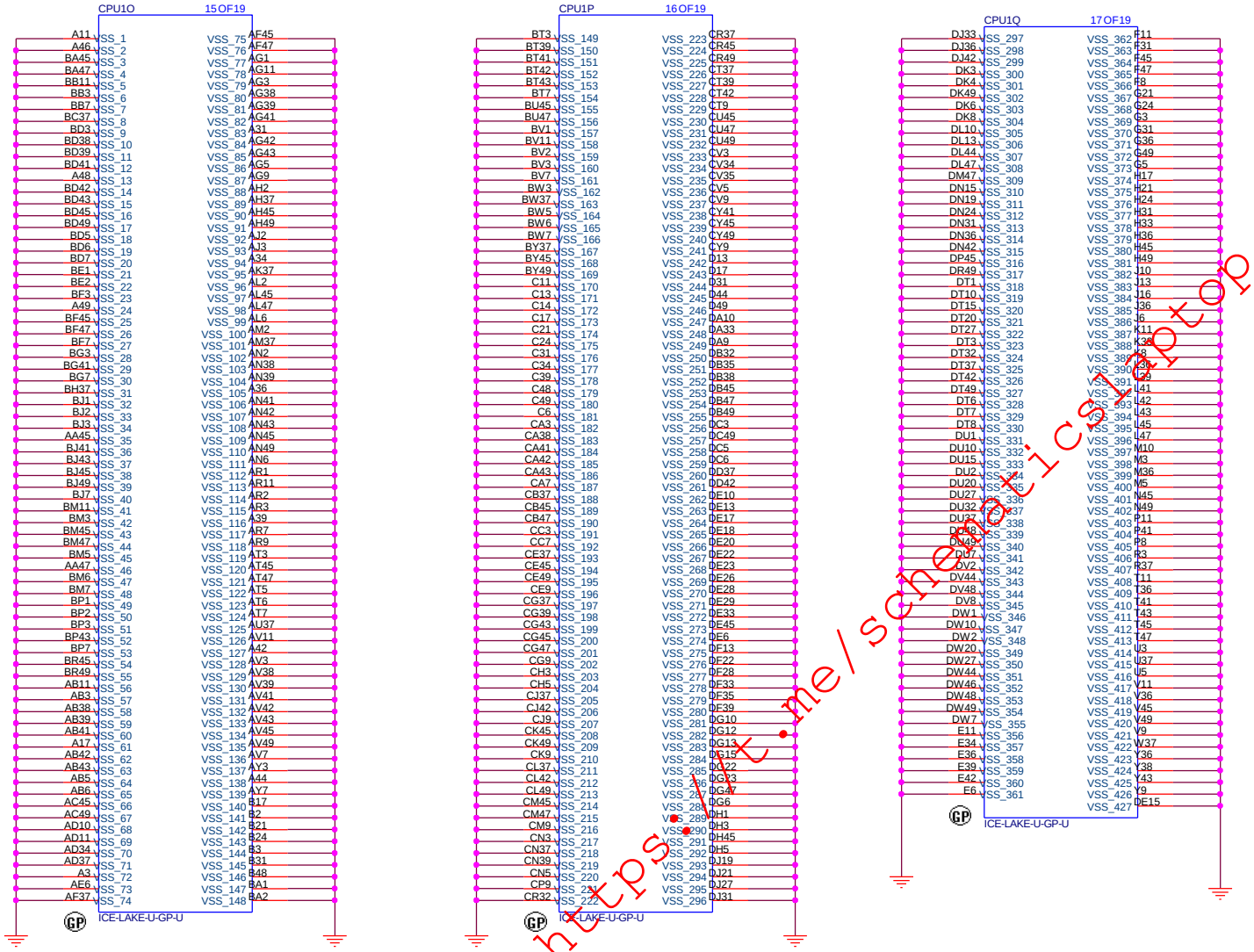
Title: CPU (PCH-LP PWR&Caps)

Size: Custom | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 22 of 106

Main Func = PCH



<CoreDesiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
TaiipeiiHsiien221, Taiiwan, R.O.C.

Title: CPU(VSS)

Size	DocumentNumber	Rev
A3	Hellcat 14/15_ ICL	SA

Date: Tuesday, September17, 2019 Sheet 23 of 106

Main Func = KBC

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	100.0K	10.0K	3
2	15" Upsell UMA	100.0K	17.8K	2.801
3	13" M6/15" M5 UMA	100.0K	27.0K	2.598
4	15" CS UMA	100.0K	37.4K	2.402
5	15" Upsell UMA	100.0K	49.9K	2.201
6	17" 2in1 UMA	100.0K	64.9K	2.001
7	14"/15" M5 DIS	100.0K	82.5K	1.806
8	17" CS DIS	100.0K	107K	1.594
9	15" Upsell DIS	100.0K	154K	1.299
10	17" 2in1 DIS	100.0K	200K	1.1

64.82525.6DL

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	N5 14"/15" UMA	100.0K	10.0K	3
2	V5 14"/15" UMA	100.0K	17.8K	2.801
3	L 14"/15" UMA(CML&KBL-R)	100.0K	27.0K	2.598
4	N7/V7 UMA	100.0K	37.4K	2.402
5	N5 14"/15" DIS	100.0K	49.9K	2.201
6	V5 14"/15" DIS	100.0K	64.9K	2.001
7	L 14"/15" DIS(CML)	100.0K	82.5K	1.806
8	N7/V7 DIS	100.0K	107K	1.594

64.49925.6DL
64.64925.6DL
64.82525.6DL

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	3000	100.0K	10.0K	3
2	3001	100.0K	17.8K	2.801
3	3002	100.0K	27.0K	2.598
4	3003(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.806
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

XTechnical

MODEL ID

Hellcat

83.R2003.ABM
2ND=083.52030.008F

eDP backlight control from ec

eDP backlight control from pch

BOARD ID

For eSPI

LayoutNote: PlacecloseIoMec1515

Need very close to EC, PSU - 0.5 inches.

For Charge(confirm level shift 1.8V to 3.3V)

M_BIT

GPIO45 (CR_STRAP)

EC G3 Flash Share

NON_JTAG

For eSPI

GPIO55 (BSS_STRAP)

Already pull low on CPU side

Non-G3 Again

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS#/	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

2.14 MEC1618 / DEC1618 Shared SPI Flash Isolation Requirement

EC G3 Flash Share

JTAG DEBUG CONN

ECDEBUG

20.K0400.010

For USBTypeC

75.27002.F7C

PowerSwitchLogic(PSL)

pull high on CPD side

071.01515.0A03

KBC Nuvoton NPCE285PA0D

MOCKINGBIRD_BCL

SA

Main Func = SPI Flash

Socket for 16M

Layout : SKT251 and U2503 co-lay

SKT251
EVT
62.10089.011

8M
072.25Q64.0H01
2nd =072.25647.000D
3rd =072.25B64.0C01

16M
072.25128.0B51
2nd =072.25127.0001
3rd =072.25128.0D61

Figure 6-85. SPI0 3-Load(2 Flash and 1 TPM) EC G3 Flash Fharing with Wire-OR Topology

Main Func = RTC

D2501
BAT54C-12-GP
75.00054.A7D
2nd =75.00054.T7D

Q2501
2N7002KDW-1-GP
75.27002.F7C

Q2507
P1A3413-1-GP
084.03413.0031
2nd =084.02301.0031

D2503
BAT54A-1-GP

U2502
RT9742CGJ5-GP
074.09742.0A9F
2nd =074.00524.0B9F

<Core Design>

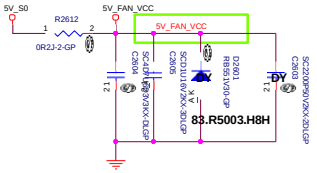
Wistron Corporation
2F., 88., Sec.1., HsinTaiWu Rd., Hsichih,
Taipei Hsien221, Taiwan, R.O.C.

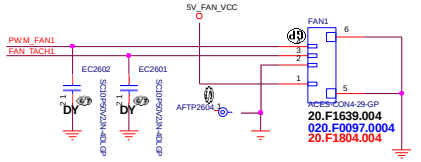
Title: Flash
Size: A2
DocumentNumber: Hellcat 14/15_ ICL
Rev: SA
Date: Tuesday., September17, 2019
Sheet 25 of 105

Main Func = Thermal Sensor

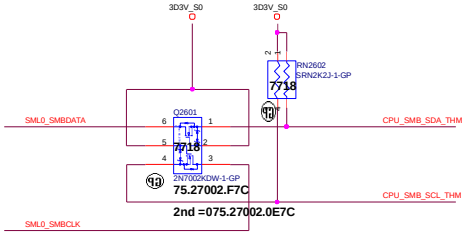
PWM FAN1

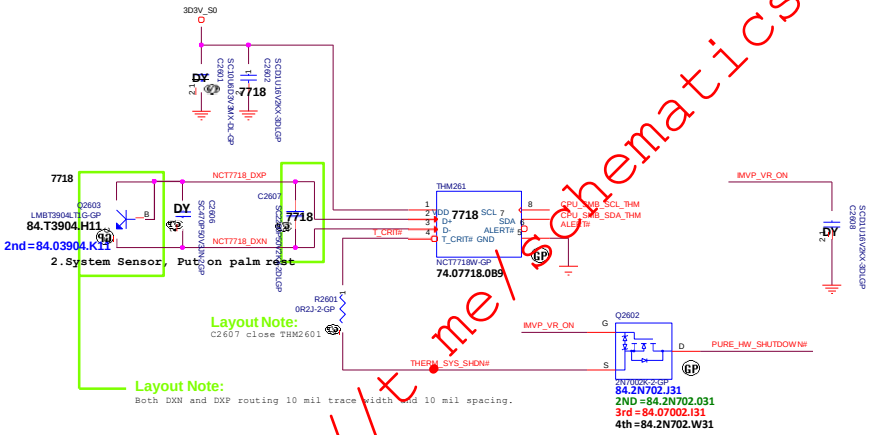
Layout Note:
Signal Routing Guideline:
Trace width = 15mil





[18,24,79]SML0_SMBDATA
[18,24,79]SML0_SMBCLK
[17,24]IMVP_VR_ON
[40] PURE_HW_SHUTDOWN#
[24] PWM_FAN1
[24] FAN_TACH1

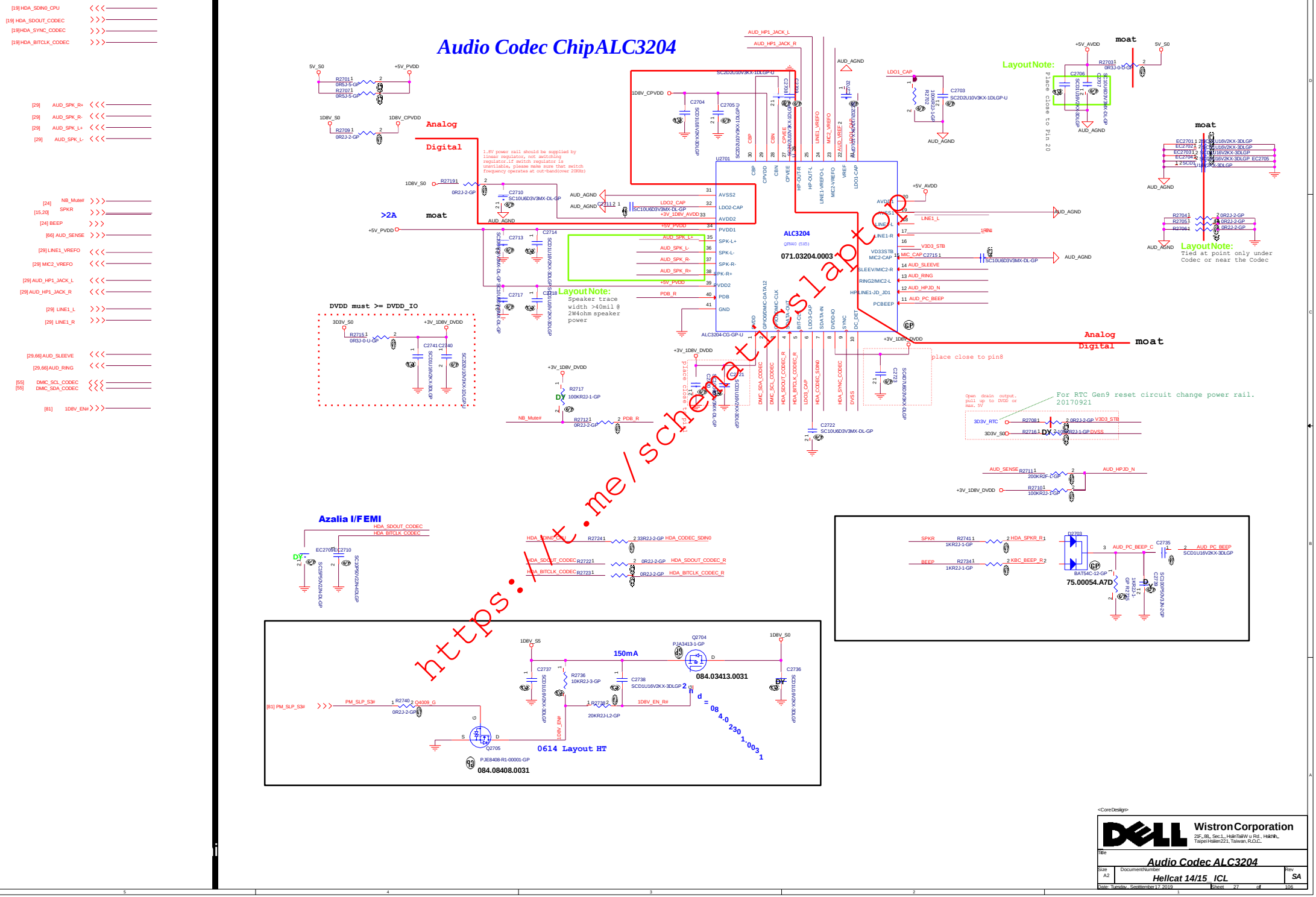




TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<CoreDesign>
Wistron Corporation
2F., 88, Sec. 1, HsinTaiWu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: THERMAL NCT7718W/Fan
Size: A2
Document Number:
Hellcat 14/15 ICL
Rev: SA
Date: Tuesday, September 17, 2019
Sheet 26 of 106

Main Func = Audio



Title: Audio Codec ALC3204

Size	Document Number	Rev
A2	Hellcat 14/15_ICL	SA

Date: Tuesday, September 17, 2019 Sheet 27 of 106

Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[20] SPK_ID

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

AUD_SPK_L+ R29021 2 0R3J-0-U-GP
AUD_SPK_L- R29011 0R3J-0-U-GP
AUD_SPK_R- R29031 0R3J-0-U-GP
AUD_SPK_R+ R29041 0R3J-0-U-GP

Follow CML_DIS
AUD_SPK_R+_C
AUD_SPK_R-_C
AUD_SPK_L-_C
AUD_SPK_L+_C
SPK_ID
ED2901 ED2902 ED2903 ED2904 ED2905
AZ5725-01FDR7G-GP
83.05725.0A0 83.05725.0A0 83.05725.0A0
83.05725.0A0 83.05725.0A0

EC2902 EC2901 EC2903 EC2904
SC1K950V2KX-1DLGP

SPK1
AUD_SPK_L+_C 1
AUD_SPK_L-_C 2
AUD_SPK_R-_C 3
AUD_SPK_R+_C 4
SPK_ID 5
6
8
MKB
ACES-CON6-20-GP-U
20.F1639.006
2nd =20.F1804.006

SPK2
1
2
3
4
5
6
Hellcat
ACES-CON4-29-GP
20.F1639.004
020.F0097.0004
20.F1804.004

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci

AUD_SPK_L- C 1
AUD_SPK_L+ C 1
AUD_SPK_R- C 1
AUD_SPK_R+ C 1
SPK_ID 1
AFTP2901
AFTP2902
AFTP2903
AFTP2904
AFTP2911

From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)

MIC2_VREFO 2 RN2901 4 SRN2K2J-1-GP
AUD_HP1_JACK_L
LINE1_L C29071
LINE1_L_C SC10U6D3V3MX-DL-GP R29221 2 1KR2J-1-GP
LINE1_R C29081
AUD_HP1_JACK_R
LINE1_L_R SC10U6D3V3MX-DL-GP R29211 1KR2J-1-GP
R29081 2 10R2F-L-GP AUD_RING AUD_HP1_JACK_L1
R29101 2 10R2F-L-GP AUD_HP1_JACK_R1 AUD_SLEEVE

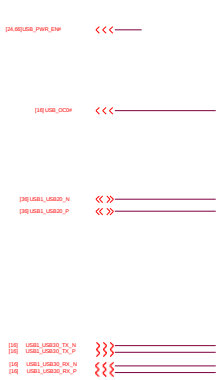
LINE1_VREFO
D2901 A RB520S30-GP
LINE1_VREFO_D1 R29121 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F
D2902 A RB520S30-GP
LINE1_VREFO_D2 R29131 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F

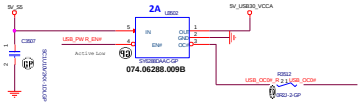
<CoreDesiign>

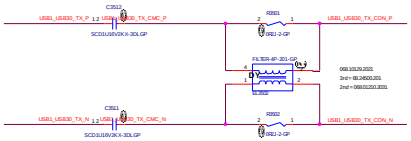
Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
TaiipeiiHsiien221, Taiiwan, R.O.C.

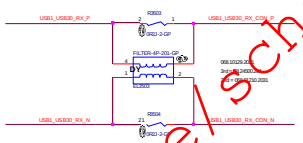
Title: Audio IO
Size: A3
DocumentNumber: Hellcat 14/15 ICL
Rev: SA
Date: Tuesday, September 17, 2019
Sheet 29 of 106

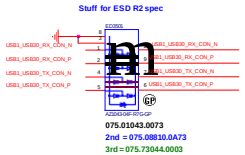
Main Func = USB3.0 Port1

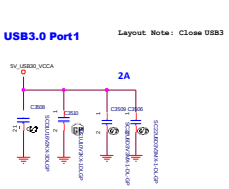


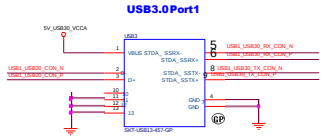












Main Func = USB3.0 Port2

<Core Design>

Wistron Corporation

USB3.0CONN

Hellcat 14/15_ICL

SA

SSID = Power Plane & Sequence

5V_S0 & 3D3V_S0

[5] 1D2V_VTT_PWRGD
[17,54,55,63]PM_SLP_S3#
[45] 3V_5V_EN
[28] PURE_HW_SHUTDOWN#
[24] ALWON
[17] SIO_SLP_S0#
[17,51,63] PM_SLP_S4#
[22,50] CORE_VID0
[22,50] CORE_VID1
[17] CPU_C10_GATE#
[17,24,44,48] VCCST_PWRGD

ROSA RunPower

5V_S0

5V_S0 Consumption
Peak current 5A

3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A

83.R2003.A8M
2nd = 083.52030.008F

074.02898.0093

PowerGood

All_SYS_PWRGD

1D05V_VCCSTG_EN

73.01G08.EHG

1D05V_VCCST/1D05V_VCCSTG

650mA

074.05027.0B93
2nd = 074.05201.0A93

150mA

074.05027.0B93
2nd = 074.05201.0A93

1D2V_VCCPLL_OC

1D05V_VCCST_EN

75.00054.A7D

If VCCPLL_OC is powered directly from VDDQ with no power gate, then SLP_3# should be replaced with SLP_S4# in the VCCST enable logic.

75.27002.F7C

Note 1: Vpullup voltage may be V1.8VA or V3.3A as set by the OEM for the GPIOs that CORE_VID[1:0] reside on. See the ICL-LP SPI Programming Guide for details.

Note 2: If VCCIN_AUX is on at a non-0V, VCCST must also be powered on.

Note 3: If VCCPLL_OC is powered directly from VDDQ with no power gate, then SLP_3# should be replaced with SLP_S4# in the VCCST enable logic.

See Note2 and Note3

V-tree_VCCIO

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.3	0.64	0.9	V

ICL no VCCIO

084.08408.0031

1D8V_PCH_C10/1D8V_S0

700mA

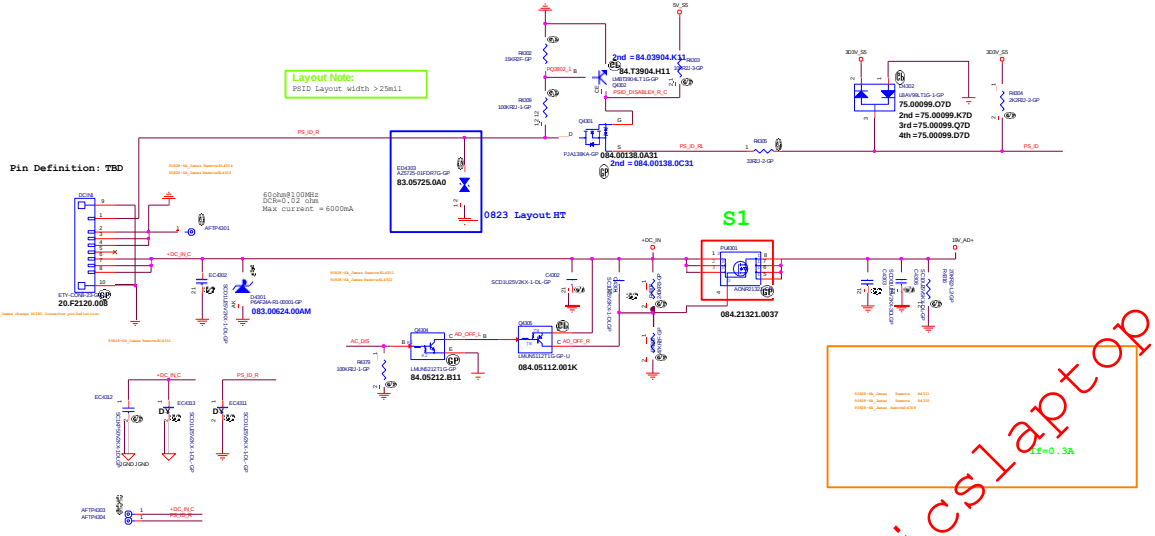
Premium

Volume

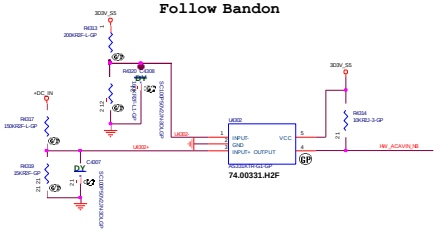
500mA

074.02898.0093

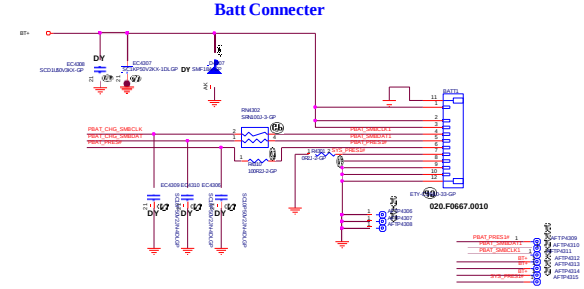
Main Func = ADT Input

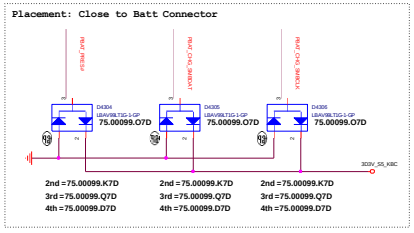


Barrel Adapter Piug-in Detect Follow Bandon



Main Func = M-BAT Input





Wistron Corporation	
DCIN	
Hellcat 14/15_ ICL	SA

ISL9538C For Charger

Main Func = Charger

OFFPAGE

S2

+3D3V_VDD_DCIN

Vcore_OVP

CHECK EE
follow custormer circuits.

TypeC Prochot
Follow custormer circuits.

PU 3V3 _AON_S0 on GPU side

PU +VCCSTG = 1.0 V on CPU side

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLim(1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	No	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

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Power (Charger_ISL9538)

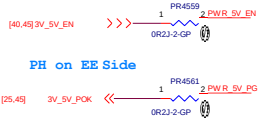
MOCKINGBIRD_MCL

SA

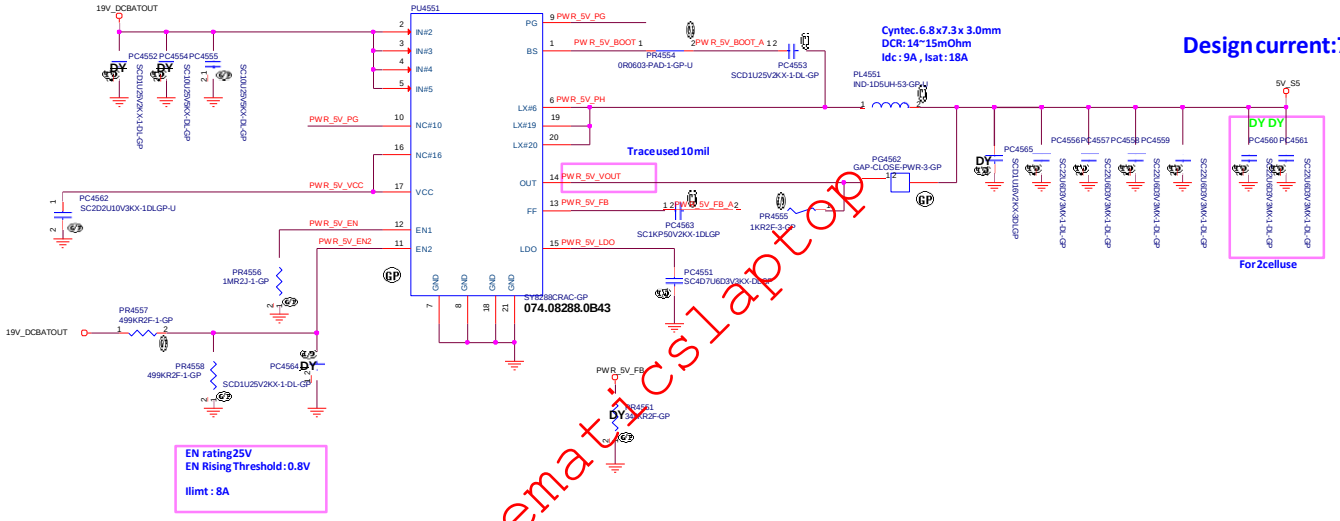
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP



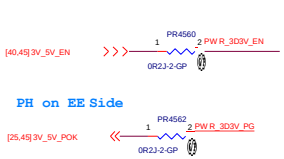
SY8288C For 5V

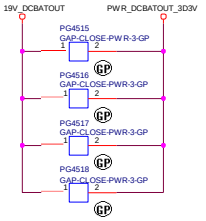


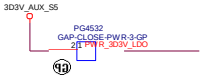
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

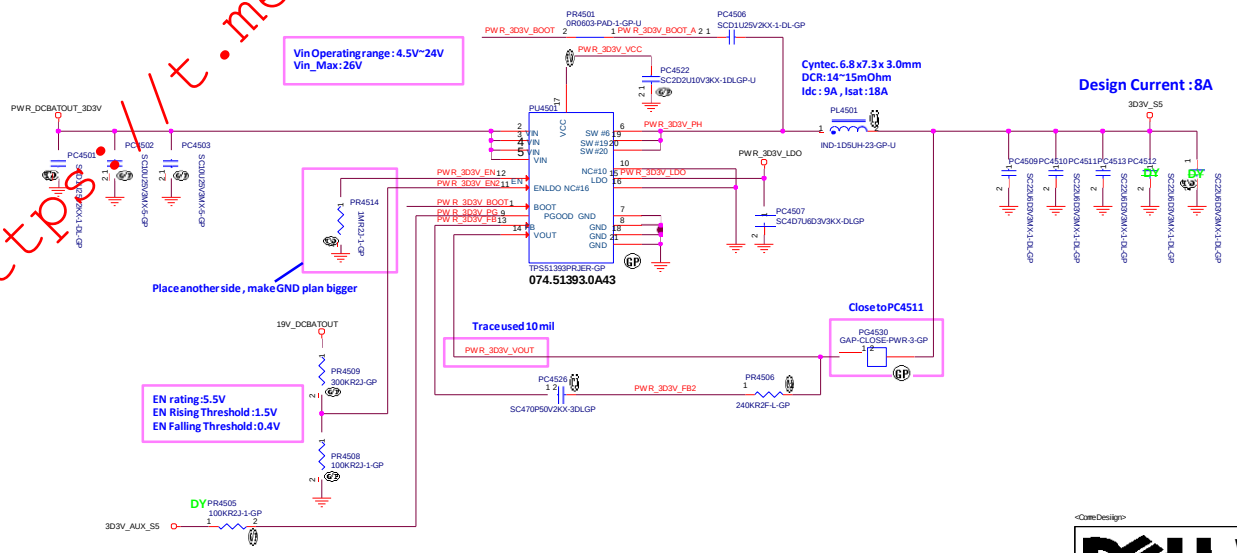
OFFPAGE-GAP







TPS 51393For 3D3V



<CoreDesilign>

Wistron Corporation
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Title: POWER (SY8288_5V/3D3V)

Size: A2 | Document Number: Hellcat 14/15_ICL | Rev: SA

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Main Func = CPU_CORE

OFFPAGE

SVID

- [7] SVID_CLK_CPU — PR4632 0R0402-PAD-1-GP — PWR_VCORE_SCLK_R
- [7] SVID_DATA_CPU — PR4633 0R0402-PAD-1-GP — PWR_VCORE_SDIO_R
- [7] SVID_ALERT#_CPU — PR4634 0R0402-PAD-1-GP — PWR_VCORE_ALERT#_R

- [3,22,24,44]PROCHOT#_CPU — PR4631 0R0402-PAD-1-GP — PWR_VCORE_VRHOT_R
- [44] CHGR_PSYS_IMVP — CHGR_PSYS_IMVP
- [7,44] PWR_IMVP_PWRGD — PR4636 0R0402-PAD-1-GP — PWR_VCORE_VR_READY
- [4,40,44]VCCST_PWRGD — PR4635 0R0402-PAD-1-GP — PWR_VCORE_VR_EN

VCORE SENSE

- [7] VSSCORE_SENSE — VSSCORE_SENSE
- [7] VCCCORE_SENSE — VCCCORE_SENSE

- [47] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
- [47] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
- [47] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

- [47] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
- [47] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
- [47] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

- [47] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
- [47] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
- [47] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
- [47] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

1D05V_VCCST
1D05V_VCCSTG_TERM
3D3V_S0
5V_S5
19V_DCBATOUT
1V_CPU_CORE
PWR_VCORE_VRHOT_R
PWR_VCORE_SCLK_R
PWR_VCORE_ALERT#_R
PWR_VCORE_SDIO_R
PWR_VCORE_VR_READY
PWR_VCORE_VR_EN
CHGR_PSYS_IMVP
PWR_VCORE_NTC_N
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_VCORE_LGATE1
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_VCORE_LGATE2
PWR_VCORE_ISEN2
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN
PWR_VCORE_ISUMN_N
PWR_VCORE_ISUMP_N
PWR_VCORE_ISUMP_2
PWR_VCORE_FB
PWR_VCORE_FB2
VCCCORE_SENSE
VSSCORE_SENSE
PWR_VCORE_PROG1
PWR_VCORE_PROG2
PWR_VCORE_BOOT1
PWR_VCORE_BOOT1_N
PWR_VCORE_BOOT2_N
PWR_VCORE_VDDP

PR4603 1K1R2F-3-GP
PR4607 100R2F-L1-GP-U
PR4609 10KR2J-3-GP
PR4617 0R2J-2-GP
PR4601 0R2J-2-GP
PC4613 SC01U10V2KX-1DLGP
PC4601 SCD22U25V2KX-4-GP
PC4612 SC4700P50V2KX-1DLGP
PR4602 12K1R2F-L1-GP
PC4609 SC330P50V2KX-3-DL-GP
PR4608 93K1R2F-L-GP
PR4619 9K31R2F-GP
PR4620 9K31R2F-GP
PR4621 0R3F-1-GP-U
PC4610 SCD22U25V2KX-4-GP
PR4625 0R2J-2-GP
PC4625 SC1U10V2KX-1DLGP
PR4616 10KR2F-2-GP
PR4618 NTC-47K-17-GP 069.60012.0001
B=4500
PR4655 27K4R2F-GP
PR4615 1K3R2F-1-GP
PR4611 0R3F-1-GP-U
PC4611 SCD22U25V2KX-4-GP
PC4608 SC330P50V2KX-3-DL-GP
PR4614 2KR2F-3-GP
PR4613 2KR2F-3-GP
PR4612 2R2F-GP
PC4607 SC2200P50V2KX-2DLGP
PC4606 SC330P50V2KX-3-DL-GP
PC4604 SC820P50V2KX-1-DL-GP
PR4665 0R2J-2-GP
PR4667 0R0402-PAD-1-GP
PR4640 100R2F-L1-GP-U
PC4615 SCD01U25V2KX-3DLGP
PC4605 SC330P50V2KX-3-DL-GP
PC4638 SC2200P50V2KX-2DLGP
PR4626 100R2F-L1-GP-U
PC4623 SC2200P50V2KX-2DLGP
PR4628 3K48R2F-GP
PR4627 511R2F-2-GP
PR4666 0R0402-PAD-1-GP
PC4614 SCD22U25V2KX-4-GP
PC4618 SCD22U25V2KX-4-GP
PR4629 0R2J-2-GP
PC4616 SCD01U16V2KX-3DLGP
PC4602 SCD01U16V2KX-3DLGP
PR4630 11KR2F-L-GP
PR4653 2K61R2F-1-GP
PR4650 NTC-10K-29-GP-U 69.60011.201
B=3370
PC4603 SCD01U16V2KX-3DLGP

U4601 074.95869.0073
PROG1
VBOOT: 1.8V
F=750kHz

<ComteDesign>

Wistron Corporation
21F., 88, Sec. 1, HsinTaiWu Rd., HsiChih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(1/3))

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Main Func = VCCIN

OFFPAGE

[46] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

[46] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

[46] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

19V_DCBATOUT — PWR_DCBATOUT_VCOREA

PL4703 IHLP4532CZ-01-GP 68.00084.831
PL4704 IHLP4532CZ-01-GP 68.00084.831

PC4702 PC4703 PC4704 PC4705 PC4706 SCD10U25V3KX-5-GP

PWR_DCBATOUT_VCOREA

PU4701 AOE6932-GP 075.06932.0A73

PWR_VCORE_LGATE1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_DCBATOUT_VCOREA

PR4705 202R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP

PL4701 IND-D15UH-33-GP 068.R1510.1171

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP

1V_CPU_CORE
PT4701 SE230L02DSVDM-2GP 79.3371V.2PL

PWR_VCORE_ISUMN_GA
PWR_VCORE_ISUMP_GA

PWR_VCORE_ISEN1 — PR4721 100KR2F-L1-GP
PWR_VCORE_ISUMP — PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN — PR4709 10R2F-L-GP
PWR_VCORE_ISEN2 — PR4722 100KR2F-L1-GP

PWR_DCBATOUT_VCOREA

PC4717 PC4714 PC4716 PC4715 PC4718 SCD10U25V3KX-5-GP

PU4702 AOE6932-GP 075.06932.0A73

PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_DCBATOUT_VCOREA

PR4714 202R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP

PL4702 IND-D15UH-33-GP 068.R1510.1171

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP

1V_CPU_CORE

PWR_VCORE_ISUMN_GB
PWR_VCORE_ISUMP_GB

PWR_VCORE_ISEN2 — PR4723 100KR2F-L1-GP
PWR_VCORE_ISUMP — PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN — PR4715 10R2F-L-GP
PWR_VCORE_ISEN1 — PR4724 100KR2F-L1-GP

ICL_U42 15W
Performance
TDC=39A
ICCMAX=70A

<CoreDesign>

Wistron Corporation
21F, 88, Sec. 1, HsinTaiWu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))
Size: A2 | Document Number: Hellcat 14/15_ICL | Rev: SA
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Main Func = VCCIN_AUX

OFFPAGE

VID

[22.40]CORE_VID0 — PR5014 2-GP — PWR_VCCIN_AUX_VID0 — 0R2J-2-GP

[22.40]CORE_VID1 — PR5016 2-GP — PWR_VCCIN_AUX_VID1 — 0R2J-2-GP

[53]1D8V_S5_PWROK — PR5012 — PWR_VCCIN_AUX_EN_R — 0R2J-2-GP

[54]1D8V_CPU_AUX_PG — PR5013 — PWR_VCCIN_AUX_PG — 0R2J-2-GP

VCCIN_AUX SENSE

[22]VCCAUX_SENSE — PR5017 — PWR_VCCIN_AUX_FB_O — 0R2J-2-GP

[22]VSSAUX_SENSE — PR5018 — PWR_VCCIN_AUX_RGND — 0R2J-2-GP

19V_DCBATOUT — PL5003 BLM21PG220SN1DGP 68.00084.831

PWR_VCCIN_AUX_IN — PL5004 BLM21PG220SN1DGP 68.00084.831

PWR_VCCIN_AUX_IN — PC5006 PC5007 PC8638 PC8639 — SCD1Z0Z5VBMX6-GP

PWR_VCCIN_AUX_BOOT — PC5009 SC1U10V2KX-1DLGP

PU5001 RT6543ACQW-GP 074.06543.0073

1	CS_DIS	BOOT	10
2	PWR_VCCIN_AUX_ISENP	VSYS	20 PWR_VCCIN_AUX_IN
3	PWR_VCCIN_AUX_ISENN	UG	11 PWR_VCCIN_AUX_UG
4	PG	PH	12 PWR_VCCIN_AUX_LX
5	PWR_VCCIN_AUX_COMP	LG	13 PWR_VCCIN_AUX_LG
6	PWR_VCCIN_AUX_FB	PGND	14
7	PWR_VCCIN_AUX_RGND	ISENSEP	2 PWR_VCCIN_AUX_ISENP
8	1D8V_CPU_AUX	ISENSEN	3 PWR_VCCIN_AUX_ISENN
9	PWR_VCCIN_AUX_FSW	VOUT	8 1D8V_CPU_AUX
15	PWR_VCCIN_AUX_VCC	COMP	5 PWR_VCCIN_AUX_COMP
16	VCC	FB	6 PWR_VCCIN_AUX_FB
17	PWR_VCCIN_AUX_VID1	RGND	7 PWR_VCCIN_AUX_RGND
18	PWR_VCCIN_AUX_VID0	AGND	21
19	PWR_VCCIN_AUX_EN		

3D3V_S0 — PR5004 10KR2J-3-GP

5V_S5 — PR5002 124KR2F-GP — PWR_VCCIN_AUX_CS

PR5001 2D2R2J-GP — PWR_VCCIN_AUX_VCC — PC5008 SC1U10V2KX-1DLGP

PWR_VCCIN_AUX_EN_R — PR5006 2D2R2J-GP — PC5010 SC1U10V2KX-1DLGP

PR5003 DY 10KR2J-3-GP

PWR_VCCIN_AUX_BOOT — PU5002 / PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073

PWR_VCCIN_AUX_IN — PU5002 / PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073

ICL_U4215W
Performance
TDC=14A
ICCMAX=32A

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

1D8V_CPU_AUX — PL5001 IND-D22UH-37-GP — PR5021 17K8R2F-GP — PR5016 0R2J-2-GP — PR5007 100R2F-L1-GP-U — PT5001 SE330U2D6VDM-2GP 79.3371V.2PL

PC5011 SCD1U25V2KX-1-DL-GP

PR5008 332R2F-1-GP — PWR_VCCIN_AUX_RC — PR5022 634R2F-1-GP

PR5023 NTC-10K-29-GP-U B=3370K

PC5003 SC2200P50V2KX-2DLGP — PWR_VCCIN_AUX_COMP_R — PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP — PWR_VCCIN_AUX_FB_R — PR5009 1K6R2F-GP DY

PC5004 SC220P50V2JN-4DLGP — PR5010 5K62R2F-GP

PWR_VCCIN_AUX_FB_O

PR5006 100R2F-L1-GP-U

PR5020 0R2J-2-GP

<ComeDesign>

Wistron Corporation
2F., 88., Sec. 1, HsinTaiWu Rd., HsiChih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX

Size: A2 | DocumentNumber | Rev: SA

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OFFPAGE

S5

[17,40,68] PM_SLP_S4#

PM_SLP_S 4#

S3

[3]VTT_CNTL

VTT_CNTL

PH on EE Side

[40] 1D2V_VTT_PW RGD

1D2V_VTT_PW RGD

OFFPAGE_GAP

19V_DCBATO UT

PR5146 0.01/REF-3-GP

PWR_DCBATOUT_ VDDQ

1D2V_S3

PG5115 GAP_CLOSE- PW R-3-GP

PWR_VDDQ_ VLDOIN

VTT

0D6V_S0

PG5111 GAP-CLOSE- PWR-3-GP

PWR_VDDQVTT

2D5V

2D5V_S3

PG5118 GAP-CLOSE-PWR-3-GP

PWR_VDDQ_ V2P5

PWR_DCBATOUT_ VDDQ

PC5102 PC5104 PC5101

5V_S5

PR5117 0R0402-PAD-1-GP

3D3V_S5

PWR_VDDQ_VLDOIN

PC5134 SC10U6D3V3MX-DL-GP

PR5116 100KR02/-1-GP

PC5135 PC5136

PWR_DCBATOUT_ VDDQ

PWR_VDDQ_VCC

PU5101

PVIN PVIN_VPP VCC_5V VLDOIN PGOOD SLP_S4 VTT_CNTL AGND SW_VPP VPPSNS BST SW VDDQSNS VTI VTISNS VTTREF PGND_VPP PGND

1D2V_VTT_PW RGD

PM_SLP_S 4#

VTT_CNTL

PWR_VDDQVPP_PH

PWR_VDDQVPP_SENSE

PWR_VDDQ_BOOT

PWR_VDDQ_PH

PWR_VDDQ_SENSE

PWR_VDDQ_VTTREF

PWR_VDDQ_BOOTA

PR5111 0R0J-0-U-GP

PR5118 0R0402-PAD-1- GP

PC5112 SC0.1U25V 2KX-1-DL- GP

PWR_VDDQVTT

PC5127 SC10U6D3V3MX-DL-GP

PC5130 SC10U6D 3V3MX-DL-GP

PC5128 SC10U6D 3V3MX-DL-GP

put as close as PU5101 pin1

put as close as PU5101 pin2

074.51486.0043

murata.2.5 x 2.0 x 1.2mm
DCR:240mOhm
Idc : 1.3A , Isat : 1.5 A

PL5102 0884R7101111

2D5V
Design Current : 0.105A

PC5137 SC22U6D3V6MX-1-GP

PC5126 SC22U6D3V6MX-1-GP

Cyntec. 6.6 x 7.3 x 3.0mm
DCR:4.8m~5.3mOhm
Idc : 16 A , Isat : 17A

PL5101 CYN-060H-3-GP 68.R6810.20J

1D2V_S3
Design Current : 5.65A

PR5110 1D29BJ-3-GP

PR5115 SC 1500P50V2KX-2-DL- GP

PR5113 0R0402-PAD-1- GP

PC5106 PC5107 PC5109 PC5108

SC 22U6D 3 V3 MX-1-DL- GP
SC 22U6D 3 V3 MX-1-DL- GP
SC 22U6D 3 V3 MX-1-DL- GP
SC 22U6D 3 V3MX-1-DL- GP
SC 22U6D 3V3MX-1-DL- GP

VTT
Design Current : 0.42A

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

Table 1. VTT_CNTL and SLP_S4 Control for Output State

<CoreDesign>

Wistron Corporation

051_POWER (TPS51486R_VDDQ/VTT)

Size: Custom | Document Number: Hellcat 14/15_ ICL | Rev: SA

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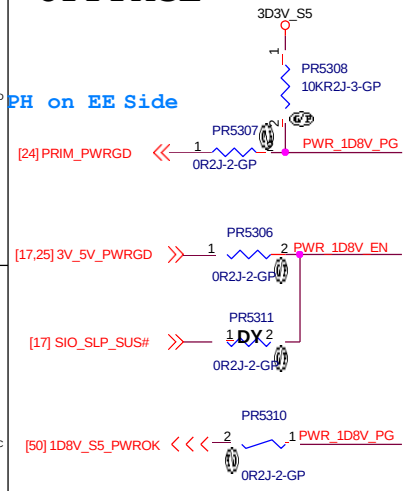
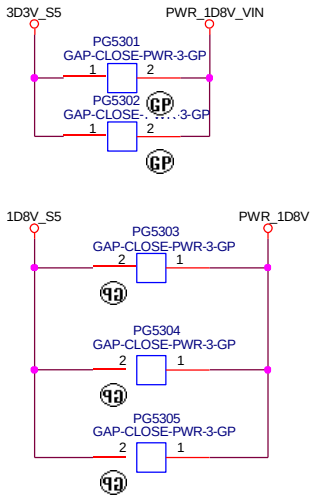
Main Func = 1D8V/1D2V

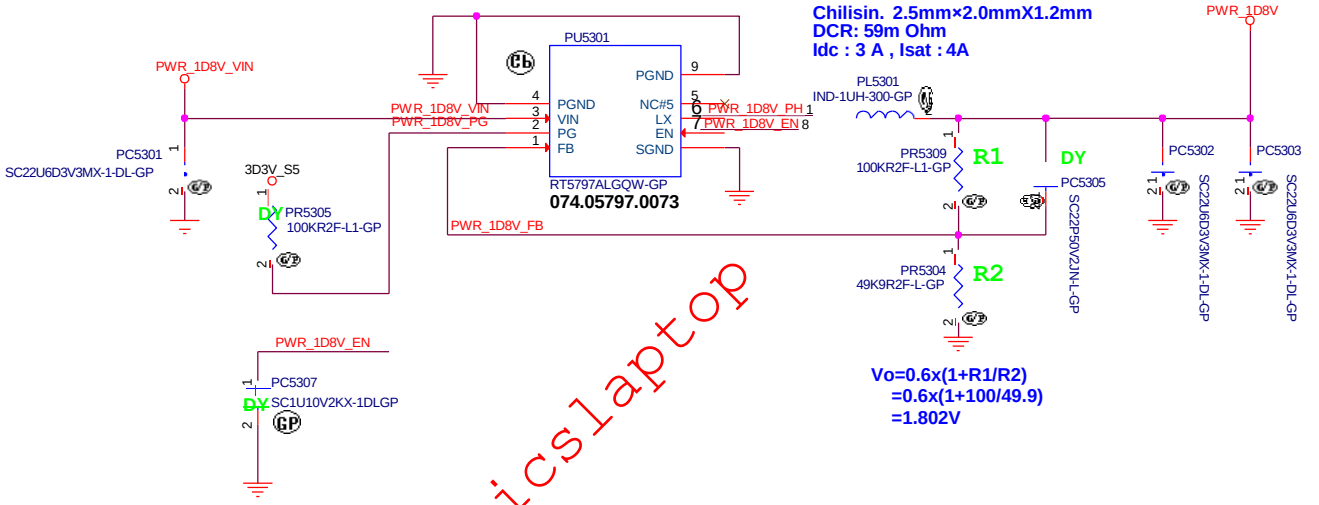
OFFPAGE



OFFPAGE_GAP



Design Current=1.7A



<CoreDesign>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&CAM&DMC&Touch	
Size: B	Document Number: Hellcat 14/15_ ICL	Rev: SA
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Main Func = 1D05V

OFFPAGE

[50]1D8V_CPU_AUX_PG — PR5450 1 — 2 PWR_VNN_EN
0R2J-2-GP

PWR_1D05A_EN — PR5454 1 — 2 PWR_VNN1D05_POK1
0R2J-2-GP

[17,40,55,81]PM_SLP_S3# — PR5452 1 — 2 PWR_VNN1D05_VID
0R2J-2-GP

OFFPAGE-GAP

PWR_VNN — R5499 1 DY 2 D01R2J-L-GP — 1D05V_VNN_BYPASS

PWR_1D05V — R5498 1 DY 2 D01R2J-L-GP — 1D05V_S5_BYPASS

3D3V_S5
PR5420 1 — 100KR2J-1-GP — 2 PWR_VNN1D05_POK1
PR5421 1 — 100KR2J-1-GP — 2 PWR_VNN1D05_POK2

Design Current=0.2A
DFE252012F-1R0M=P2

PU5401
APW8738AQBI-TRG-1 GP
074.08738.0073

PC5401 1 2 SC1U10V2KX-1DLGP
PR5413 2D2R2J-GP
PC5402 1 2 SC10U6D3V3MX-DL-GP
PR5422 2 0R0402-PAD-1-GP
PR5410 2 0R0402-PAD-1-GP
PC5403 1 2 SC10U6D3V3MX-DL-GP
PC5404 1 2 SCD1U25V2KX-2DLGP
PC5405 1 2 SCD1U25V2KX-1-DL-GP
PC5406 2 DY 1 SCD1U16V2KX-3DLGP
PC5407 2 DY 1 SCD1U16V2KX-3DLGP
PR5423 1 2 0R2J-2-GP
PR5401 1 2 0R2J-2-GP

PWR_VNN1D05_VCC 8
PWR_VNN1D05_VIN1 11
PWR_VNN1D05_VIN2 10
PWR_VNN1D05_VID 13
PWR_VNN1D05_BOOT1R
PWR_VNN1D05_BOOT2R
PWR_VNN1D05_BT1 2
PWR_VNN1D05_BT2 3
PWR_VNN1D05_POK1 14
PWR_VNN1D05_POK2 7
PWR_VNN1D05_LX2
PWR_VNN1D05_LX1

VCC, VIN1, VIN2, VID, BOOT1, BOOT2, POK1, POK2, EN1, EN2, LX1, LX2, FB2, VOUT1, AGND, PGND, PGND

15 PWR_VNN_EN
6 PWR_1D05A_EN
1 PWR_VNN1D05_LX1
4 PWR_VNN1D05_LX2
5 PWR_VNN1D05_FB2
16 PWR_VNN1D05V_VOUT1
17
9
12

2 PR5419 1 PWR_VNN
0R0402-PAD-1-GP

PWR_VNN
PL5401 IND-1UH-363-GP
PC5411 SC10U6D3V3MX-DL-GP
PC5412 SC10U6D3V3MX-DL-GP

Design Current=0.2A
1239AS-H-100N=P2

PWR_1D05V
PL5402 IND-10UH-271-GP
PR5408 7K5R2F-1-GP
PR5407 10KR2F-2-GP
PC5410 SC10U6D3V3MX-DL-GP

<CoreDesiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih, TaiipeiiHsiien221, Taiiwan, R.O.C.

Tiitle: POWER(APW8738A_VNN1D05)

Siize	Document Number	Rev
A3	Hellcat 14/15_ ICL	SA

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Main Func = LCD

From CPU

[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P1
[4] eDP_AUX_CPU_P
[4] eDP_AUX_CPU_N
[4] eDP_HPD_CPU
[4] EDP_VDD_EN
[4] L_BKLT_CTRL

From EC

[24,55] PANEL_BKEN
[17,40,54,81] PM_SLP_S3#

FOR TESTING

[20] DRC_PANEL_EN
[24] LCD_VCC_TEST_EN
[24] LCD_TST
[24] CABLE2_OCP#
[24] PANEL_MONITOR
[66] 3D3V_LCDVDD_R
[20,70] SENSOR_I2C_SDA
[20,70] SENSOR_I2C_SCL
[20] GSEN_INT1_C
[24,55] PANEL_BKEN

Main Func = Touch panel

[20] CPU_I2C_SDA_TS
[20] CPU_I2C_SCL_TS
[3] TOUCH_PANEL_INTR#
[24] TOUCH_REPORT_SW
[3] TOUCH_PANEL_DET#
[20] TOUCH_PANEL_PDI#

Main Func = CAMERA

[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK_Q
[19] DMIC_PCH_DATA_Q

INVERTER POWER

Hinge up cable protection

MIC POWER

CAMERA POWER

SENSOR POWER

TOUCH PANEL POWER

Touch Panel
CCD& CAM
Sensor Board
Display
eDP

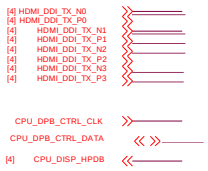
PANEL_PWRGD CIRCUIT

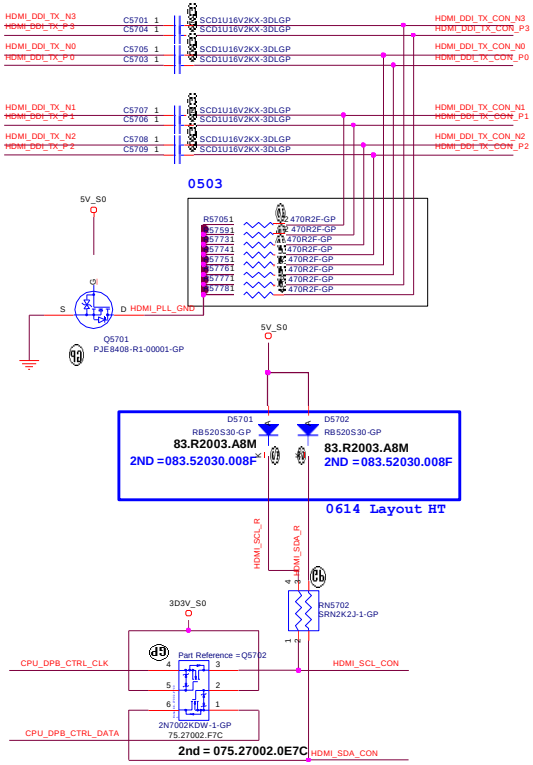
Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.

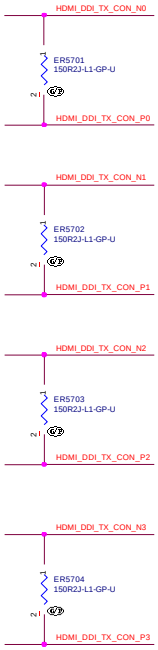
Brightness
EC (BIST MODE)

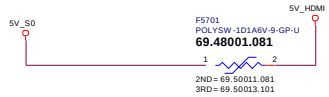
WistronCorporation
LCD&CAM&DMC&Touch
Hellcat 14/15_ICL
SA

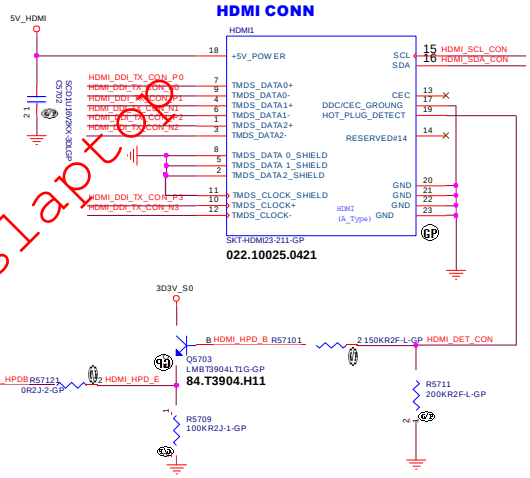
SSID = HDMI Level Shifter/Connector











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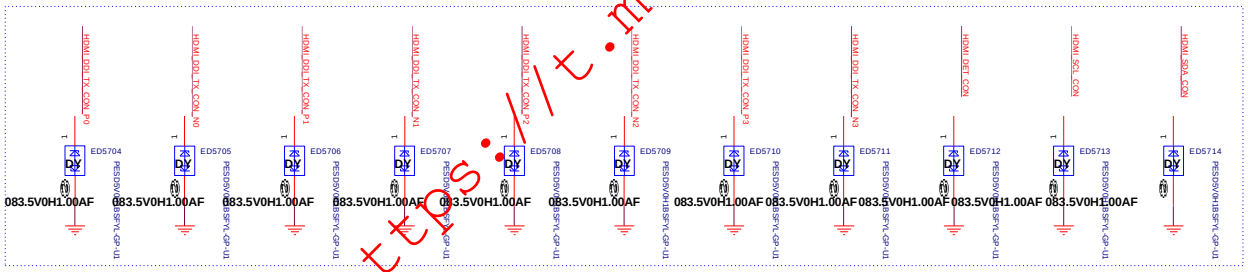

<Core Design>

Wistron Corporation
21F., 88., Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size: Custom | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 57 of 106

Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] WLAN_CLKREQ_CPU_N

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[3] BLUETOOTH_EN
[21] WIFI_RF_EN
[17,63,66,76,91] PLT_RST#
[18,24] SUS_CLK

Debug

Power EN (Madesimo)

[15,21] CNV_BRI_DT_R
[15,21] CNV_RGI_DT
[19] CLKREQ_CNV
[19] CNV_RF_REST#
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_BRI_RSP
[21] CNV_RGI_RSP
[24] JIO3_PCIE_WAKE#

3D3V_S5 R6140 D01R5F-GP 3D3V_WLAN

1.1A

C6110 SCD1U16V2KX-3DLGP
C6106 SC100D03V3MX-DL-GP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6101 1 3D3V_WLAN
AFTE14P-GP AFTP6105 1 WLAN_CLKREQ_CPU_N
AFTE14P-GP AFTP6106 1 WIFI_RF_EN_R
AFTE14P-GP AFTP6107 1 BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 1 PLT_RST#
AFTE14P-GP AFTP6109 1 BT_USB20_CON_N
AFTE14P-GP AFTP6110 1 BT_USB20_CON_P
AFTE14P-GP AFTP6111 1 JIO3_PCIE_WAKE#

3D3V_WLAN R6145 10KR2J-3-GP DY
WIFI_RF_EN R6144 0R2J-2-GP DY WIFI_RF_EN_R

3D3V_WLAN R6146 10KR2J-3-GP DY
BLUETOOTH_EN R6143 0R2J-2-GP DY BLUETOOTH_EN_R

3D3V_WLAN

WLAN1

76	76		
74	74		
72	3_3VAUX		
70	3_3VAUX		
68	RESERVED#70		
66	RESERVED#68		
64	RESERVED#66		
62	GPIO0_NFC_RESET#/MGPIO7		
60	NFC_I2C_IRQ/MGPIO5		
58	NFC_I2C_SM_CLK		
56	NFC_I2C_SM_DATA		
54	W_DISABLE#1		
52	RESERVED#54/W_DISABLE#2		
50	PERST0#		
48	SUSCLK_32KHZ		
46	COEX1		
44	COEX2		
42	COEX3		
40	CLINK_CLK		
38	CLINK_DATA		
36	CLINK_RESET		
34	UART_CTS		
32	UART_RTS		
	UART_TX		
22			
20	UART_RX		
18	UART_WAKE		
16	GND		
14	LED#2		
12	PCM_OUT		
10	PCM_IN		
8	PCM_SYNC		
6	PCM_CLK		
4	LED#1		
2	3_3VAUX		
	3_3VAUX		
NP2	NP2		
		77	77
		75	GND
		73	RESERVED#73
		71	RESERVED#71
		69	GND
		67	RESERVED#67/2ND_LANE_PERN1
		65	RESERVED#65/2ND_LANE_PERP1
		63	GND
		61	RESERVED#61/2ND_LANE_PETN1
		59	RESERVED#59/2ND_LANE_PETP1
		57	GND
		55	PEWAKE0#
		53	CLKREQ0#
		51	GND
		49	REFCLKN0
		47	REFCLKP0
		45	GND
		43	PERN0
		41	PERP0
		39	GND
		37	PETN0
		35	PETP0
		33	GND
		23	
		21	SDIO_RESET
		19	SDIO_WAKE
		17	SDIO_DAT3
		15	SDIO_DAT2
		13	SDIO_DAT1
		11	SDIO_DAT0
		9	SDIO_CMD
		7	SDIO_CLK
		5	GND
		3	USB_D-
		1	USB_D+
			GND
		NP1	NP1

NGFF_KEY_E_75P

SKT-NGFF75P-164-GP
062.10003.0B11

3D3V_WLAN R6106 10KR2J-3-GP CLKIN_XTAL_LCP_R

WIFI_RF_EN_R
BLUETOOTH_EN_R
PLT_RST#
SUS_CLK R61351 33R2J-2-GP SUSCLK_WLAN

CNV_RGI_RSP R61091 22R2J-2-GP CNV_BRI_DT_R / CNV_RGI_RSP_R / CNV_RGI_DT
CNV_BRI_RSP R61181 22R2J-2-GP CNV_BRI_RSP_R

CLKREQ_CNV R6141 33R2J-2-GP BT_PCMOUT_CLKREQ0_R
CNV_RF_REST# R6142 33R2J-2-GP BT_PCMFRM_CRF_RST_N

3D3V_WLAN R6134 75KR2F-GP R6133 71K5R2F-1-GP

CNV_WT_CLKP
CNV_WT_CLKN
CNV_WT_DP0
CNV_WT_DN0
CNV_WT_DP1
CNV_WT_DN1
JIO3_PCIE_WAKE#
WLAN_CLKREQ_CPU_N
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_CON_N
WLAN_PCIE_TX_CON_P
C61071 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_N
C61081 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_P
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WR_DP0
CNV_WR_DN0
CNV_WR_DP1
CNV_WR_DN1
BT_USB20_CON_N
BT_USB20_CON_P

BT_USB20_CON_P R61111 0R2J-2-GP BT_USB20_P
BT_USB20_CON_N R61101 0R2J-2-GP BT_USB20_N

<CoreDesiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, TaiipeiiiHsiien221, Taiiiwan, R.O.C.

Title: NGFF_WLAN CONN
Size: A3
Document Number: Hellcat 14/15_ ICL
Rev: SA
Date: Tuesday, September 17, 2019
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Main Func = M.2 SSD

[18] SSD_CLKREQ_CPU_N
[17,61,63,66,76,91] PLT_RST#

[16] SSD_DEVSLP
[18] SSD_CLK_CPU_P
[18] SSD_CLK_CPU_N
[16] SSD_PCIE_TX_P
[16] SSD_PCIE_TX_N
[16] SSD_PCIE_RX_N
[16] SSD_PCIE_RX_P
[16] SSD_PCIE_TX_P3
[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_TX_P2
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_RX_N2
[16] SSD_PCIE_TX_P1
[16] SSD_PCIE_TX_N1
[16] SSD_PCIE_RX_P1
[16] SSD_PCIE_RX_N1
[16] M2_SSD_PEDET
[64] M2_PCIE_LED#
[24] SSD_SCP#

3D3V_S0
R6355
D01R5F-1-GP
3D3V_SSD1

SSD M.2 CONN

SSD1
SKT-NGFF75P-224-GP
NGFF_KEY_M 75P

062.10003.0F31
2nd =062.10003.0481
3rd =062.10003.0F21

SSD_CLKREQ_CPU_N
PLT_RST#
SSD_DEVSLP
R6352
MSATA_DEVSLP_R
0R2J-2-GP
M2_PCIE_LED#
SSD_SCP#
R6354
R6356
M2_PCIE_LED#_R
SSD_SCP1#

PCIE:1 SATA:0

R6353
100KR2J-1-GP
M2_SSD_PEDET
SSD_CLK_CPU_P
SSD_CLK_CPU_N
SSD_SATA_TX_CON_P
SSD_SATA_TX_CON_N
SSD_PCIE_TX_CON_P3
SSD_PCIE_TX_CON_N3
SSD_PCIE_TX_CON_P2
SSD_PCIE_TX_CON_N2
SSD_PCIE_TX_CON_P1
SSD_PCIE_TX_CON_N1
C6343
C6345
C6346
C6339
C6342
C6335
C6337
SCD22U10V2KX-2-GP
SSD_PCIE_TX_P
SSD_PCIE_TX_N
SSD_PCIE_RX_N
SSD_PCIE_RX_P
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_TX_P1
SSD_PCIE_TX_N1
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

M.2 SSD2

[16] SSD_PCIE_TX_P9
[16] SSD_PCIE_TX_N9
[16] SSD_PCIE_RX_N9
[16] SSD_PCIE_RX_P9
[16] SSD_PCIE_TX_P10
[16] SSD_PCIE_TX_N10
[16] SSD_PCIE_RX_P10
[16] SSD_PCIE_RX_N10
[16] SSD_PCIE_TX_P11
[16] SSD_PCIE_TX_N11
[16] SSD_PCIE_RX_P11
[16] SSD_PCIE_RX_N11
[16] SSD_PCIE_TX_P12
[16] SSD_PCIE_TX_N12
[16] SSD_PCIE_RX_P12
[16] SSD_PCIE_RX_N12
[18] SSD2_CLK_CPU_P
[18] SSD2_CLK_CPU_N
[18] SSD2_CLKREQ_CPU_N
[16] SSD2_DEVSLP
[16] M2_SSD2_PEDET

3D3V_S0
R6351
D01R5F-1-GP
MKB
3D3V_SSD2

SSD M.2 CONN

SSD2
SKT-NGFF75P-224-GP
NGFF_KEY_M 75P

062.10003.0F31
2nd =062.10003.0481
3rd=062.10003.0F21
MKB

SSD2_CLKREQ_CPU_N
PLT_RST#
SSD2_DEVSLP
R6350
MSATA_DEVSLP2_R
0R2J-2-GP
SSD_SCP#
R6357
M2_PCIE_LED#
SSD_SCP2#

PCIE:1 SATA:0

R6349
MKB
100KR2J-1-GP
M2_SSD2_PEDET
SSD2_CLK_CPU_P
SSD2_CLK_CPU_N
SSD_SATA_TX_CON_P12
SSD_SATA_TX_CON_N12
SSD_PCIE_TX_CON_P11
SSD_PCIE_TX_CON_N11
SSD_PCIE_TX_CON_P10
SSD_PCIE_TX_CON_N10
SSD_PCIE_TX_CON_P9
SSD_PCIE_TX_CON_N9
C6324 MKB
C6325 MKB
C6326 MKB
C6327 MKB
C6328 MKB
C6329 MKB
C6330 MKB
C6331 MKB
SCD22U10V2KX-2-GP
SSD_PCIE_TX_P12
SSD_PCIE_TX_N12
SSD_PCIE_RX_N12
SSD_PCIE_RX_P12
SSD_PCIE_TX_P11
SSD_PCIE_TX_N11
SSD_PCIE_RX_P11
SSD_PCIE_RX_N11
SSD_PCIE_TX_P10
SSD_PCIE_TX_N10
SSD_PCIE_RX_P10
SSD_PCIE_RX_N10
SSD_PCIE_TX_P9
SSD_PCIE_TX_N9
SSD_PCIE_RX_P9
SSD_PCIE_RX_N9

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Title: mSATA
Size: A2
DocumentNumber: Hellcat 14/15_ ICL
Rev: SA
Date: Tuesday, September 17, 2019
Sheet 63 of 105

CML

Main Func = Power BTN

NONE FINGER PRINT オオオオ

Power button

[24] KBC_PWRBTN#

[66] KBC_PWRBTN#_R

Layout note:
G6401 place to buttom
G6402 place to top

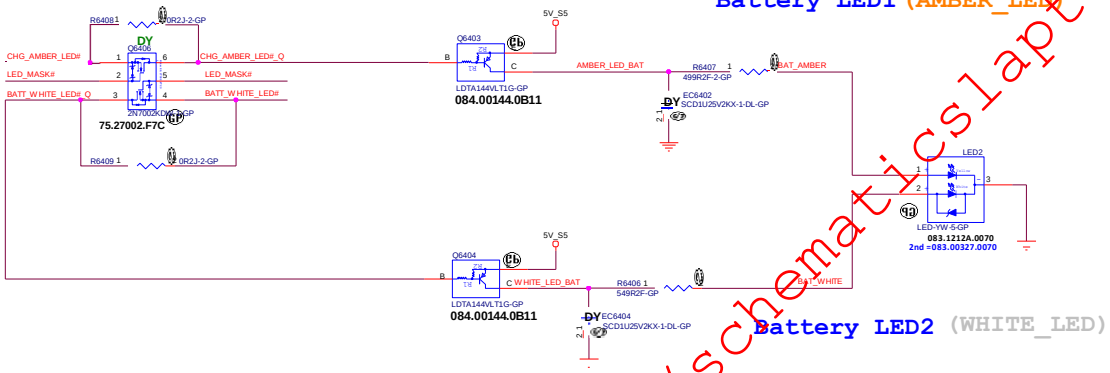
Main Func = Battery LED

Low actived from KBC GPIO

[24]LED_MASK#

[24] CHG_AMBER_LED#

[24] BATT_WHITE_LED#



Battery LED1 (AMBER_LED)

Battery LED2 (WHITE_LED)

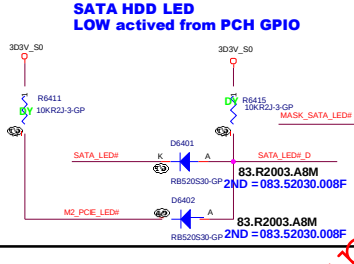
Main Func = HDD LED

[20,24] MASK_SATA_LED#

[18] SATA_LED#

[63] M2_PCIE_LED#

[63] SATA_LED#_D

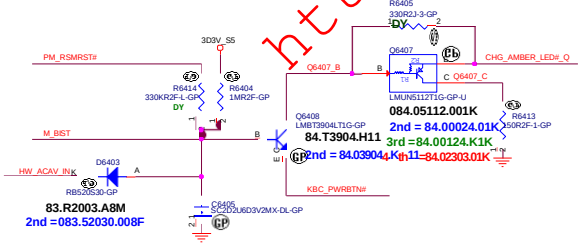


Main Func = M-BIST

[17,18]PM_RSMRST#

[24] M_BIST

[24,44] HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

<CoreDesign>

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Title: LED Board&Power Button

Size: A2 | Document Number: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 64 of 106

Main Func = KB

0513

[24] CAP_LED#_R

[4] KB_DET#

[20] KB_LED_BL_DET

[24] KB_LED_PWM

[24] KSO00 KSO01 KSO02 KSO03 KSO04 KSO05 KSO06 KSO07 KSO08 KSO09 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16

[24] KSI[0..7] KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

Keyboard Backlight (Reserved)

5V_S0 → F6502 KBBL POLYSW-1D1A6V3-GP-U 69.48001.081

+5V_KB_BL

C6501 SCD1U16V2KX-3DLGP

KBBL1 KBBL

KB_LED_BL_DET → R6503 51KR2J-1-GP

KB_LED_DET_C

KB_BL_CTRL# → R6507 100KR2J-1-GP

ACES-CON6-GP-U 020.K0298.0004 → AFTP6565

KB Backlight Power Consumption: 285mA max.

KB_LED_PWM → R6505 100KR2J-1-GP

Q6501 PJA3402-R1-00001-GP 084.03402.0031 KBBL

+5V_KB_BL → AFTP6506

KB_LED_DET_C → AFTP6566

KB_BL_CTRL# → AFTP6567

KB_LED_DET_C → EC6501 SCD1U16V2KX-3DLGP

KB_BL_CTRL# → EC6503 SCD1U16V2KX-3DLGP

CAP LED Control

LOW actived from KBC GPIO

CAP_LED#_R → Q6502 LDTA144VLT1G-GP 084.00144.0B11

5V_S0 → R6506 1KR2J-1-GP → CAP_LED

CAP_LED_Q

Internal Keyboard Connector

KB1 ACES-CON30-29-GP 020.K0254.0030

CAP_LED KSO10 KSO11 KSO09 KSO14 KSO13 KSO15 KSO16 KSO12 KSO00 KSO02 KSO01 KSO03 KSO08 KSO06 KSO07 KSO04 KSO05 KSI3 KSI0 KSI5 KSI2 KSI4 KSI7 KB_DET#

Main Func = TPAD

0513

[24] CLK_TP_SIO_I2C_DAT

[24] DAT_TP_SIO_I2C_CLK

[20,66] CPU_I2C_SCL_P0

[20,66] CPU_I2C_SDA_P0

[3,24] TOUCHPAD_INTR#

[24] PTP_DIS#

3D3V_S0 → R6502 0R2J-2-GP → TP_VDD

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TP_VDD

TP side has pull high

TOUCHPAD_INTR# → R6511 10KR2J-3-GP

Support PTP

PS2

DAT_TP_SIO_I2C_CLK

CLK_TP_SIO_I2C_DAT

RN6502 SRN0J-6-GP

I2C

CPU_I2C_SCL_P0

CPU_I2C_SDA_P0

R6513 0R2J-2-GP

R6514 0R2J-2-GP

I2C1_SCL_R

I2C1_SDA_R

EC6504 SCD1U16V2KX-3DLGP

EC6505 SCD1U16V2KX-3DLGP

DY DY

TP_VDD

RN6503 SRN2K2J-1-GP

I2C1_SCL_R

I2C1_SDA_R

Precision Touch Pad Connector

TP_VDD → C6505 SCD1U16V2KX-3DLGP

TP1 PTWO-CON8-16-GP 020.K0255.0008 2nd =020.K0151.0008 → AFTP6531

I2C1_SDA_R

I2C1_SCL_R

TOUCHPAD_INTR#

PTP_DIS#

TP_VDD → AFTP6529

I2C1_SCL_R → AFTP6528

I2C1_SDA_R → AFTP6527

TOUCHPAD_INTR# → AFTP6525

PTP_DIS# → AFTP6526

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

Wistron Corporation

21F., 88, Sec.1, HsinTaiWu Rd., Hsichih, Taipei Hsien221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

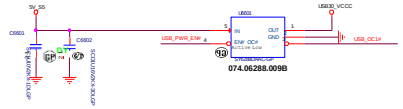
Size: A2 | Document Number: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September17, 2019 | Sheet 65 of 106

Main Func = IO Connector

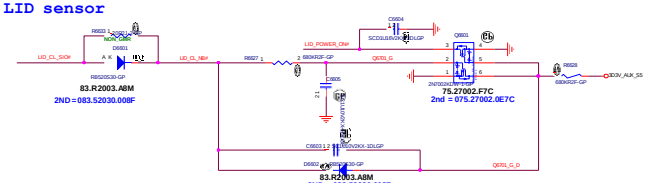
USB2.0 Power

Pin define by follow layout routing



074.06288.009B

LID sensor

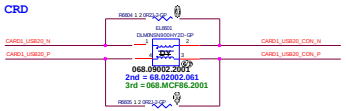


83.R2003.A8M
2ND = 083.52030.008F

75.Z7002.F7C
2nd = 075.27002.0E7C

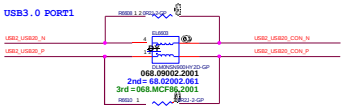
83.R2003.A8M
2ND = 083.52030.008F

CRD



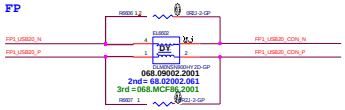
068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001

USB3.0 PORT1



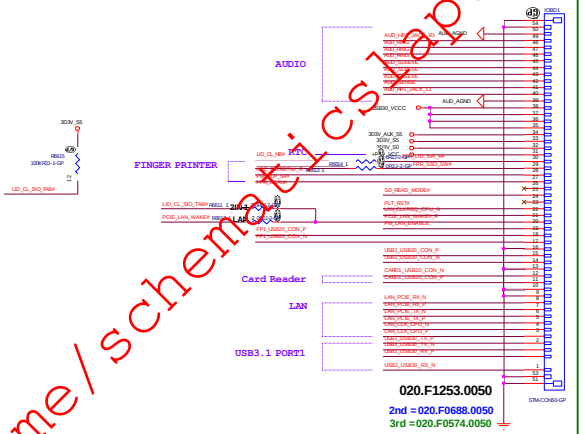
068.09002.2001
2nd= 68.02002.061
3rd =068.MCF86.2001

FP

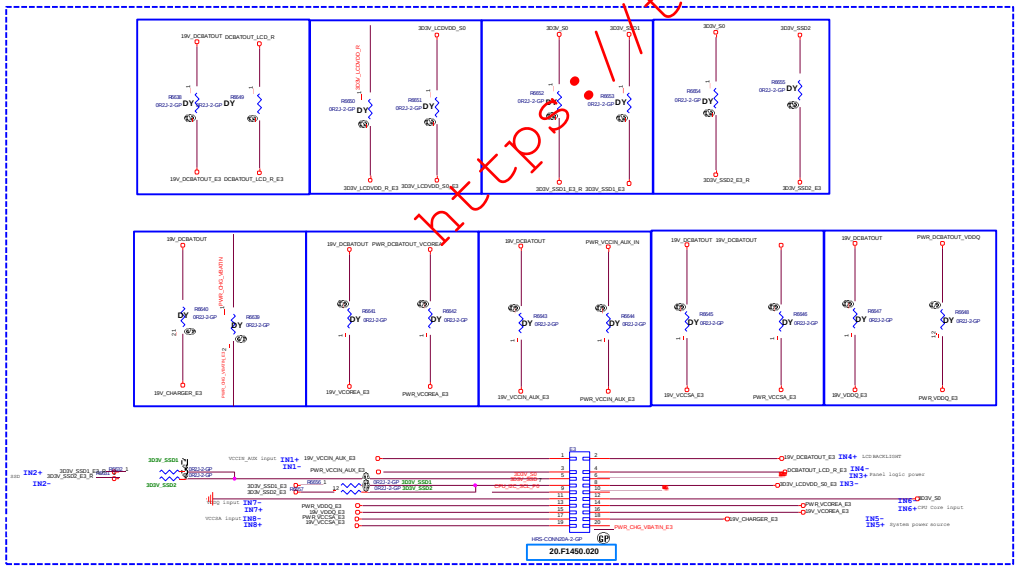


068.09002.2001
2nd= 68.02002.061
3rd =068.MCF86.2001

I/O Board Connector



020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050



20.F1450.020

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IO Board Connector

Hellcat 14/15 ICL

SA

Main Func = Debug

ESPI

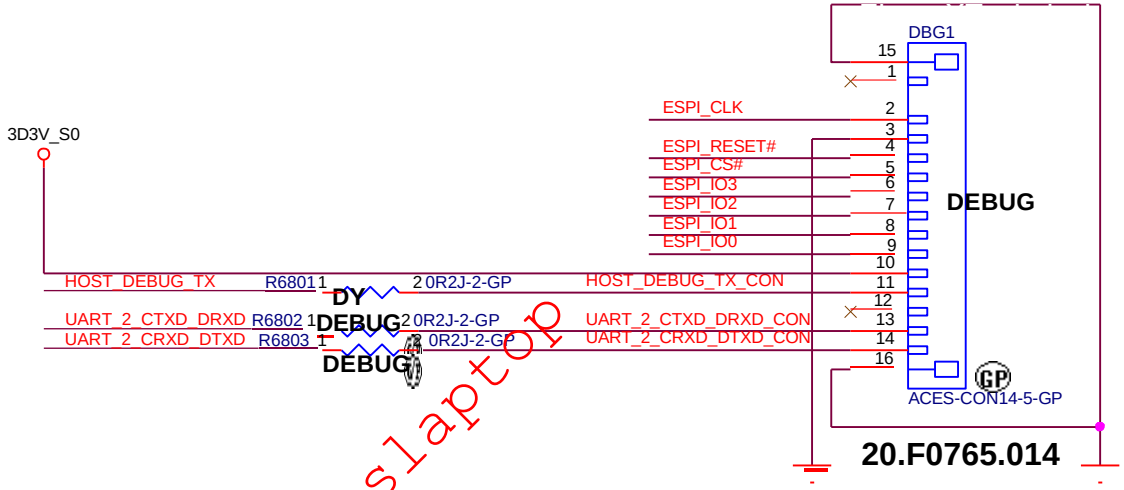
[18,24] ESPI_CLK
[18,24] ESPI_RESET#
[18,24] ESPI_CS#

[18,24] ESPI_IO[3..0]
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0

UART

[24] HOST_DEBUG_TX
[20] UART_2_CTXD_DRXD
[20] UART_2_CRXD_DTXD

ESPI Debug Connector



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Title: *Dubug connector*

Size	Document Number	Rev
A4	*Hellcat 14/15_ ICL*	*SA*

Date: Tuesday, September 17, 2019 Sheet 68 of 106

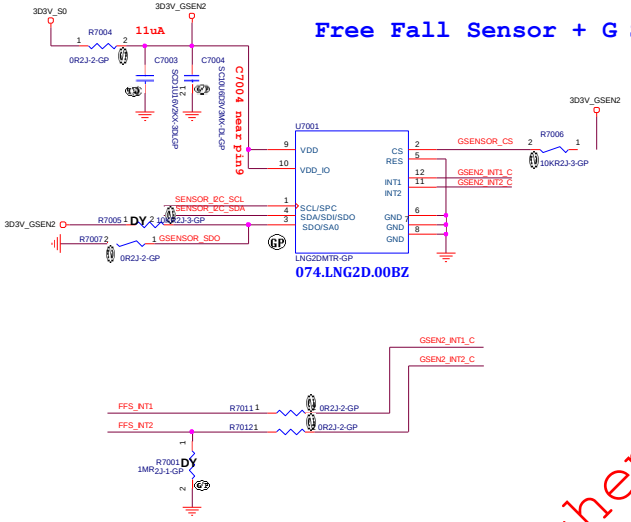
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

[20] GSEN2_INT1_C
[20,55] SENSOR_I2C_SCL
[20,55] SENSOR_I2C_SDA
[20] FFS_INT1
[19] FFS_INT2

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<CoreDesign>

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Title: Free FallSensor

Size	Document Number	Rev
A2	Hellcat 14/15_ICL	SA

Date: Tuesday, September 17, 2019 Sheet 70 of 106

Main Func =TI

[74] PD_VBUS_C_CTRL1

EC

[24] UPD1_SMBCLK
[24] UPD1_SMBDAT

[74] VBUS_P_CTRL

[24] CCG5C_I2C_INT#

0513

MUX TUSB546

[73] I2C_DATA_PD
[73] I2C_CLK_PD

[4,73] DP1_HPD_CPU

[73] CCG5_SBU1
[73] CCG5_SBU2

[74] NX5P3363_FO

TYPE-CCONNECTOR

[73] USB1_CC1
[73] USB1_CC2
[73] TOP_MUX_P_L
[73] TOP_MUX_N_L
[73] BOT_MUX_P_L
[73] BOT_MUX_N_L
[73] USB1_SBU1
[73] USB1_SBU2

PCH

[16] USB4_USB20_P
[16] USB4_USB20_N

From System

3D3V_S5
VCC3PD_1
D7202
SBA0520Q-R1-00001-GP-U

D7203
SBA0520Q-R1-00001-GP-U
083.00520.0F8F

2nd =083.05S40.001F

VCC3PD
R7211
0R2J-2-GP
VDDD

For debattery

Power

VDDD
C7203
C7204
C7207
SCD1U16V2KX-3DLGP
SCD1U10V2KX-1DLGP
VCC3PD_1
C7210
C7212

MOD ID Settings

RN7202
I2C_CLK_PD
I2C_DATA_PD
SRN2K2J-1-GP
R7202
100KR2J-1-GP
CCG5C_I2C_INT#

R7201
51KR2J-1-GP
CCG5_MOD_ID1
R7213
150KR2J-GP

MOD ID Settings

R7212
100KR2J-1-GP
CCG5_MOD_ID2
R7214
100KR2J-1-GP

R7215
10KR2F-3-GP
CCG5_SWD_CLK/CCG5_I2C_CFG_EC
R7220
10KR2F-3-GP

VCC3PD_1
R7217
100KR2J-1-GP
R7223
100KR2J-1-GP
PD_VBUS_C_CTRL
VBUS_P_CTRL_C
Q7201
2N7002KDW-1-GP
PD_VBUS_C_CTRL1_C
VBUS_P_CTRL
R7218
10JKR2J-1-GP
R7222
100KR2J-1-GP

2nd =075.27002.0E7C
75.27002.F7C

U7201
VDDD
VDDIO
VSYS
VCCD
V5V
VBUS
ISP
CSN
I2C_INT_EC
I2C_SCL_SCB1_EC
I2C_SDA_SCB1_EC
I2C_INT_AR
I2C_SCL_SCB2_AR
I2C_SDA_SCB2_AR
SCL3/VSEL_1
SDA3/VSEL_2
OV_OCP_TRIP/SCL_4
OVP_TRIP/SDA_4
SWD_IO/AR_RST
SWD_CLK/I2C_CFG
VBUS_P_CTRL
VBUS_C_CTRL
CC1
CC2
DPLUS_SYS
DMINUS_SYS
UART_TX
UART_RX
DPLUS_TOP
DMINUS_TOP
DPLUS_BOT
DMINUS_BOT
SBU1
SBU2
AUX_P
AUX_N
LSTX
LSRX
XRES#
HPD
GND
CYPD5126-40LQXIT-12-GP
071.05126.0P03

SCD1U16V2KX-3DLGP
PD_VCCD
5V_S5
20V_VCCPD_VBUS
CCG5C_I2C_INT#
UPD1_SMBCLK
UPD1_SMBDAT
CCG5_MOD_ID2
I2C_CLK_PD
I2C_DATA_PD
CCG5_MOD_ID1
CCG5_ILIM
NX5P3363_FO
CCG5_PROCHOT#
CCG5_SWD_CLK/CCG5_I2C_CFG_EC
SWD_CLK/I2C_CFG
R7225
R7226
10KR2J-3-GP
R7224
0R2J-2-GP
R7216
10KR2J-3-GP
VBUS_P_CTRL_C
PD_VBUS_C_CTRL1_C
USB1_CC1
USB1_CC2
C7221 C7220
SCP39P50V2KX-3-DL-GP
SC330P50V2KX-3-DL-GP
USB4_USB20_P
USB4_USB20_N
UPD1_SMBCLK
UPD1_SMBDAT
TOP_MUX_P_L
TOP_MUX_N_L
BOT_MUX_P_L
BOT_MUX_N_L
USB1_SBU1
USB1_SBU2
CCG5_SBU1
CCG5_SBU2
PD_XRES
CPU_DP_HPD_MUX
R72081
2 0R2J-2-GP
R7207
10KR2J-3-GP
DP1_HPD_CPU
R7209
100KR2J-1-GP
R7221
4K7R2J-2-GP
C7219
SCD1U16V2KX-3DLGP

<CoreDesign>

Wistron Corporation
2F., 88, Sec. 1, HsinTaiWu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB PD(CYPD5126)

Size: A2
Document Number: Hellcat 14/15_ ICL
Rev: SA

Date: Tuesday, September 17, 2019
Sheet 72 of 106

Main Func = TYPEC MUX

DisplayPortSource

USB HOST

DisplayPortAUX

MUX I2C

DisplayPortHPD

I2C/USBMUX

TypeCCC

For displayport function at dead batterycondition

Slave address : 0X44

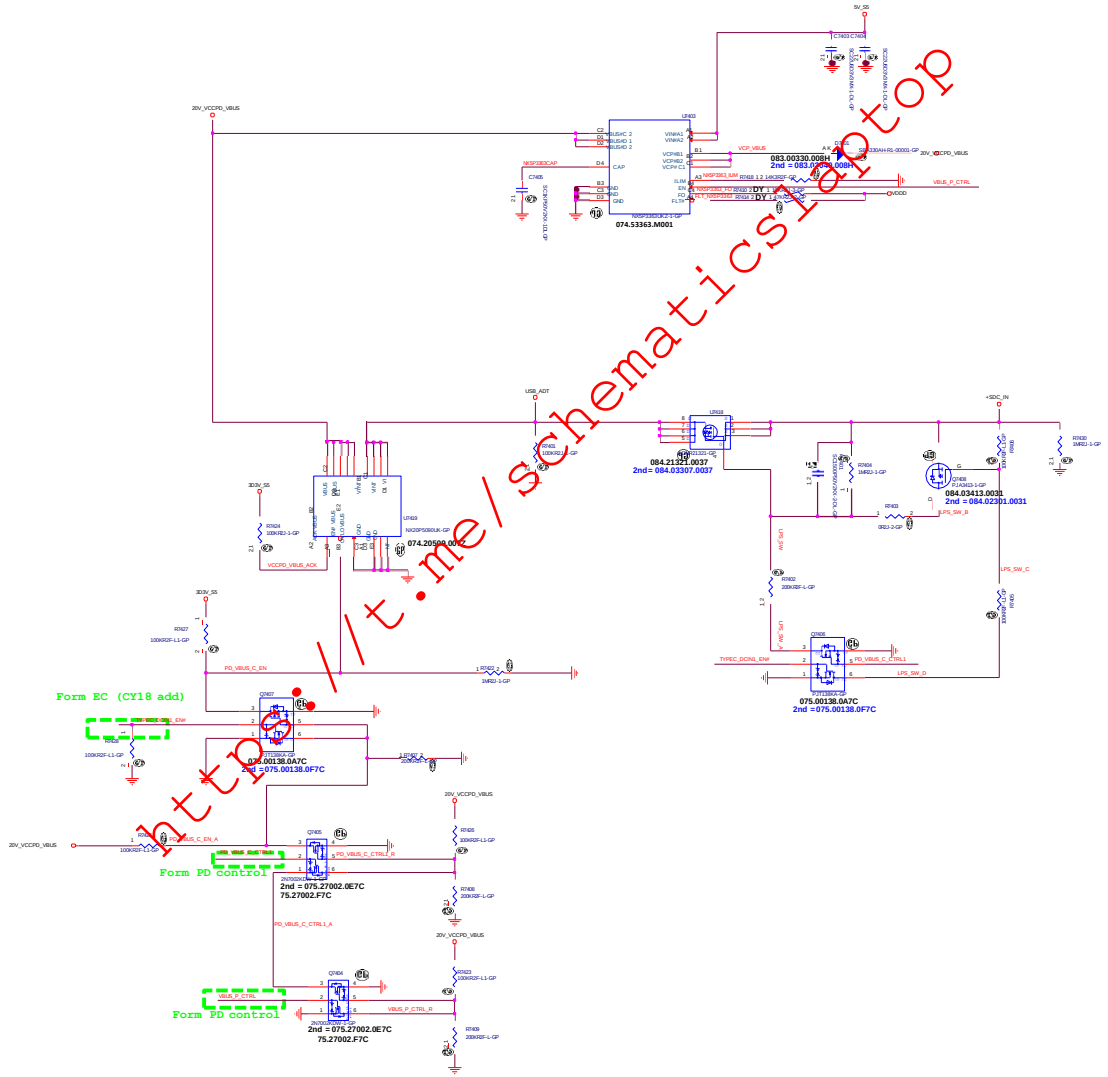
3A

0614 Layout HT

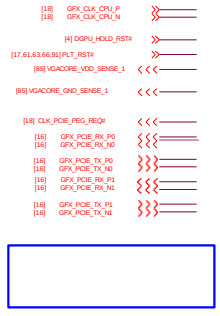
Wistron Corporation

USB Type-C&MUX(TUSB546)

Hellcat 14/15_ICL



Main Func = dGPU



0508

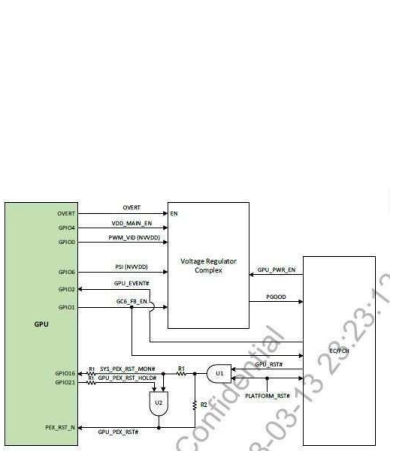


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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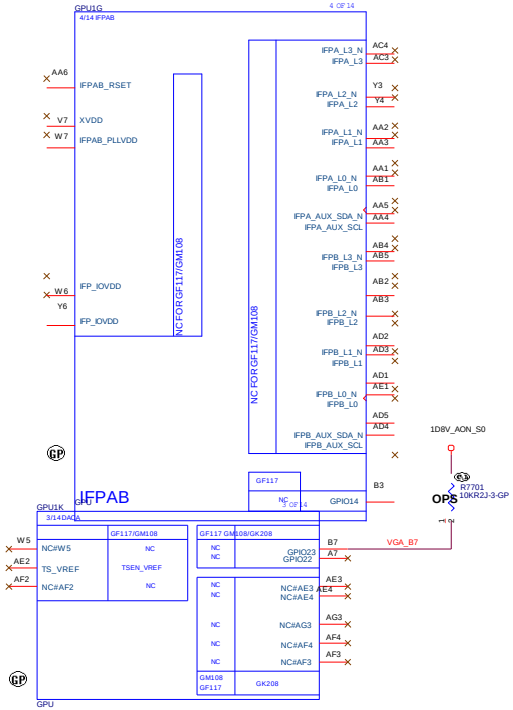
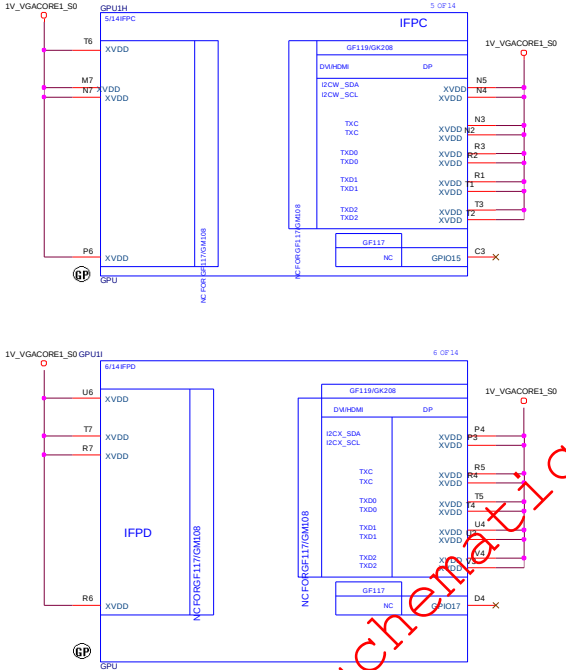
GPU(1/5)PEG

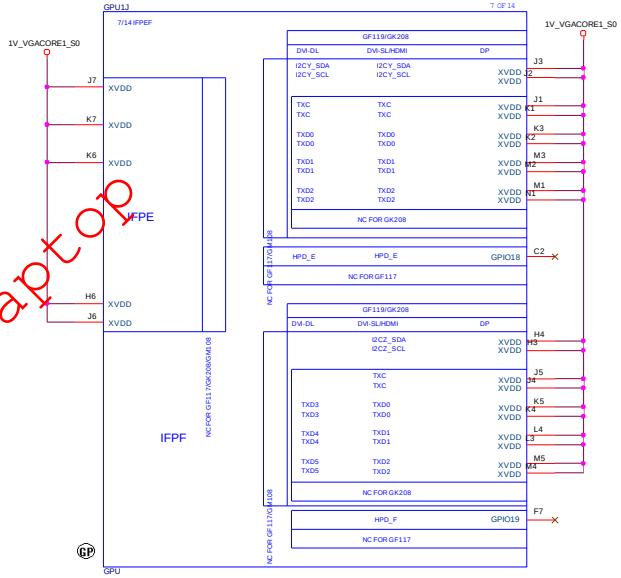
Hellcat 14/15_ ICL

SA

Main Func = dGPU







<CoreDesign>
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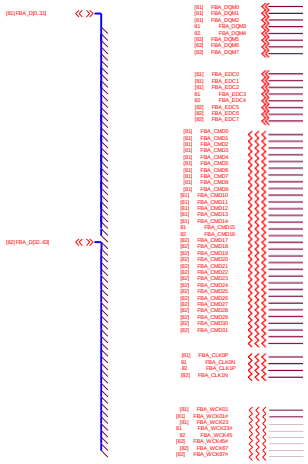
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsi-chih,
Taipei Hsien 221, Taiwan, R.O.C.

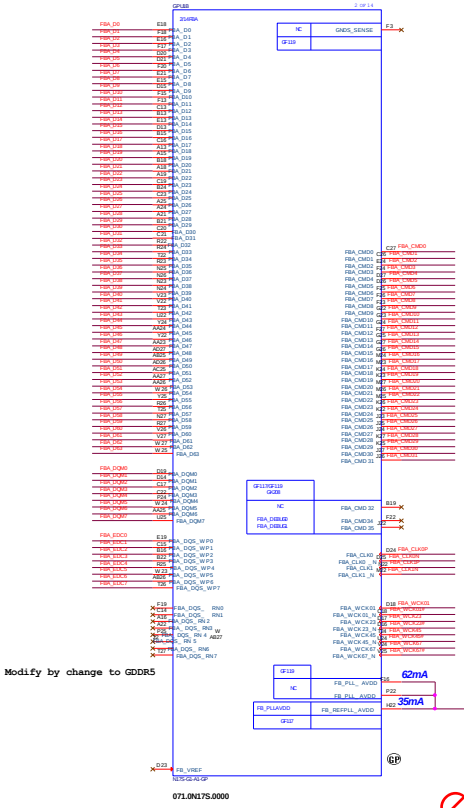
Title: GPU(2/5)DIGITALOUT

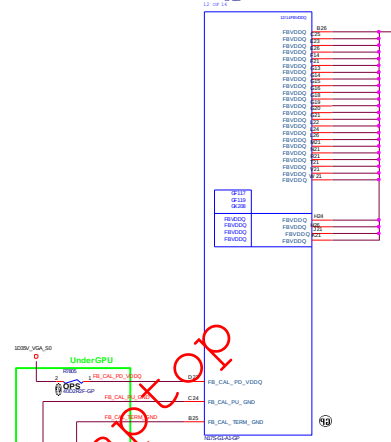
Size	Document Number	Rev
A2	Hellcat 14/15_ ICL	SA

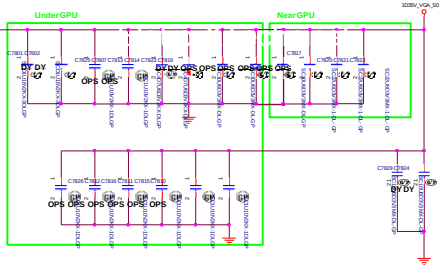
Date: Tuesday, September 17, 2019 Sheet 77 of 106

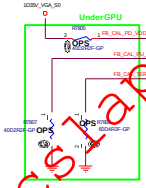
Main Func = dGPU

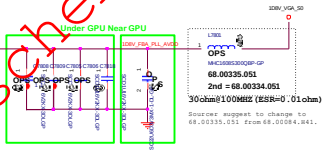


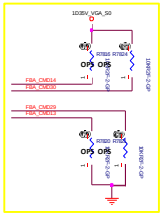












Modify by change to GDDR5

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

GDDR5:60.4R

GDDR3:51.1R

071.0N17S.0000

1.35V +/- 3%
4.88A

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

Main Func = dGPU

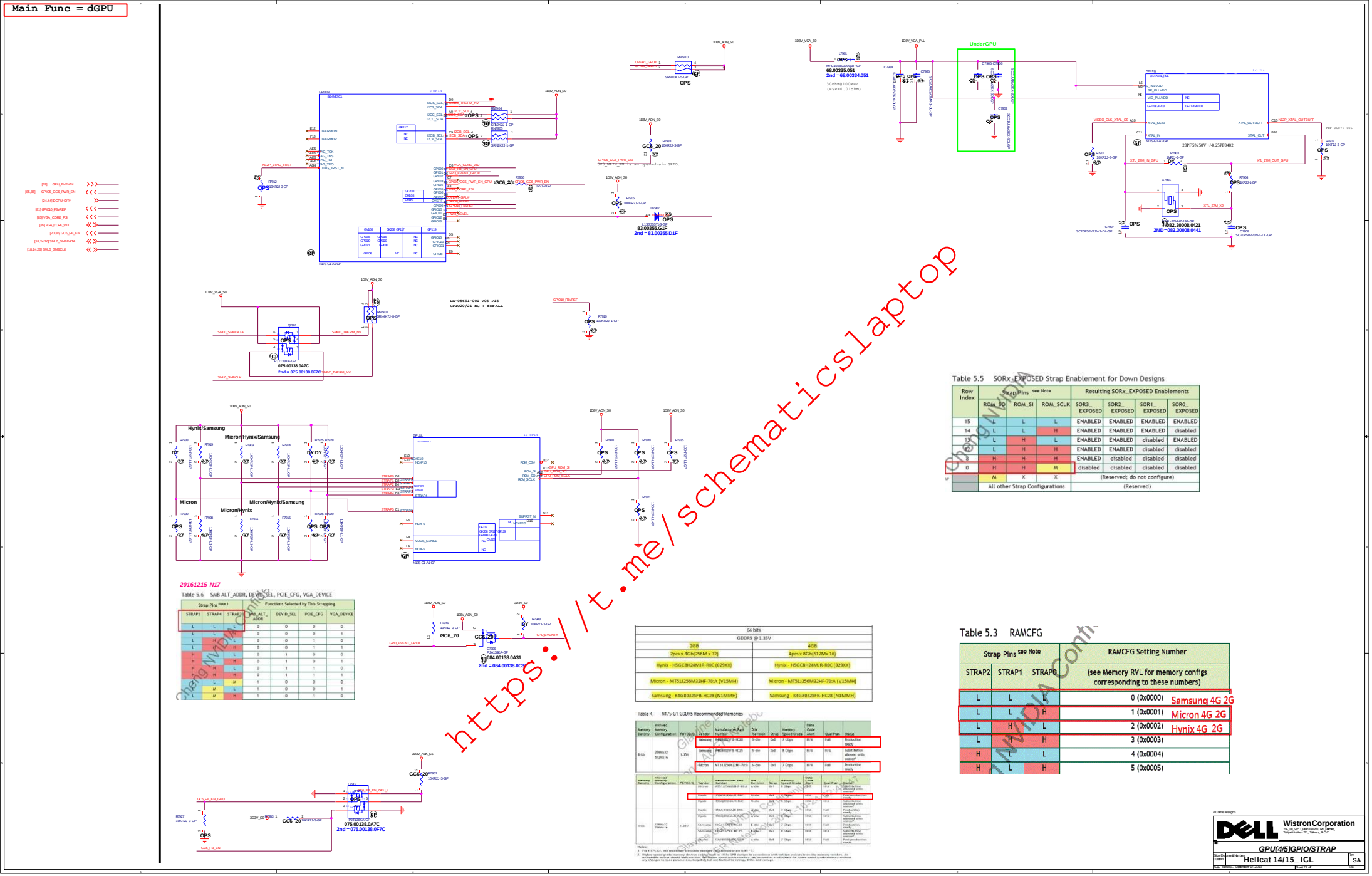


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)	
STRAP2	STRAP1	STRAP0		
L	L	L	0 (0x0000)	Samsung 4G 2G
L	L	H	1 (0x0001)	Micron 4G 2G
L	H	L	2 (0x0002)	Hynix 4G 2G
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	

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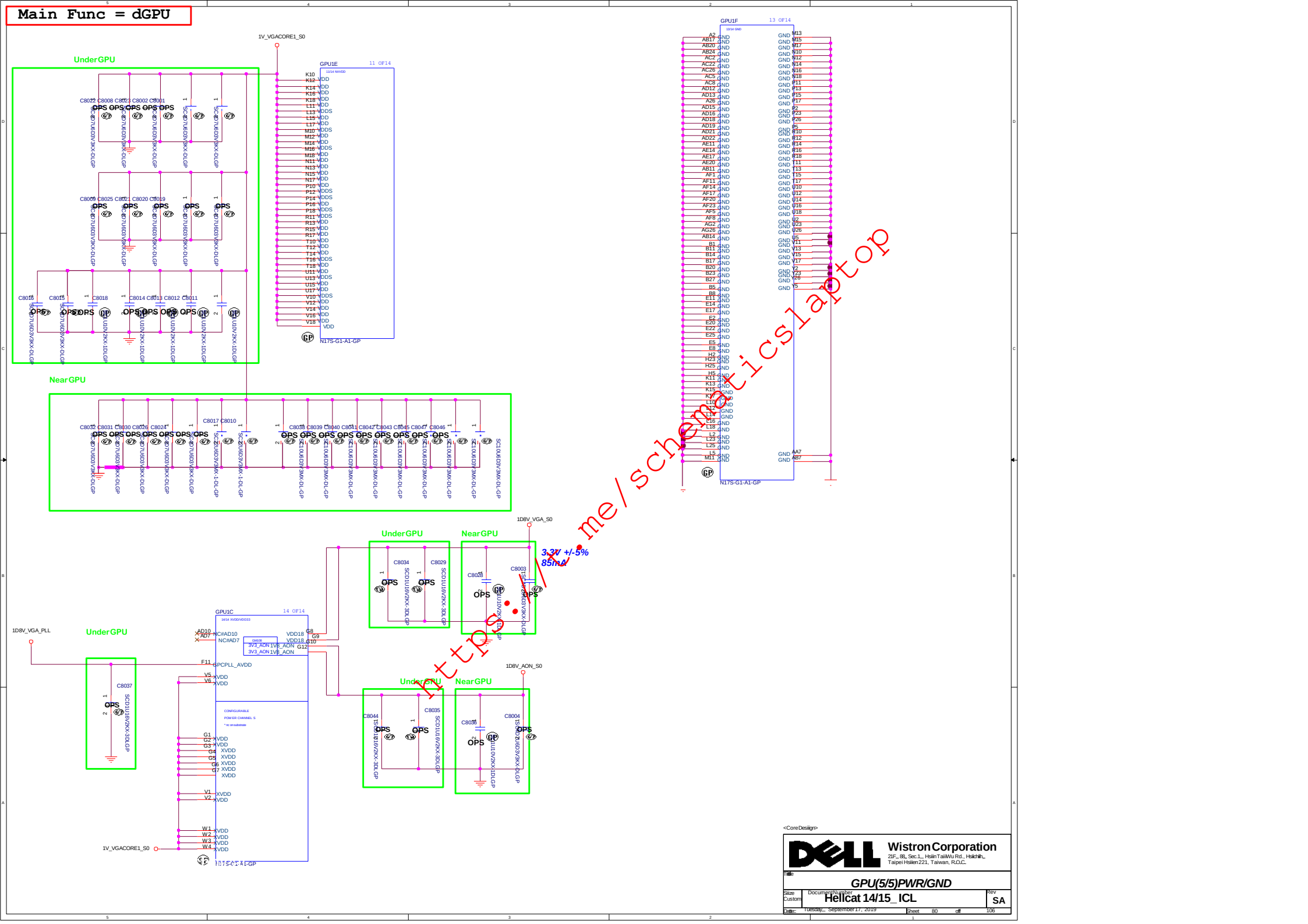
GPU(4/5)GPIO/STRAP

Hellcat 14/15_ICL

SA



<CoreDesign>

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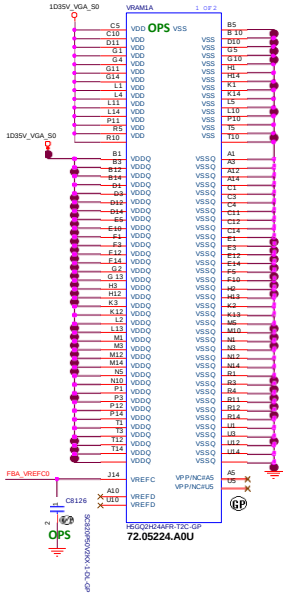
21F., 88, Sec.1, HsinTaiWu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(5/5)PWR/GND

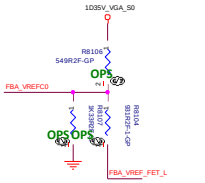
Size	Document Number	Rev
Custom	Hellcat 14/15_ ICL	SA

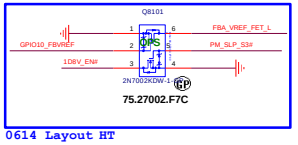
Date: Tuesday, September 17, 2019 Sheet 80 of 106

SSID = VRAM



Frame Buffer Patition A-Lower Half

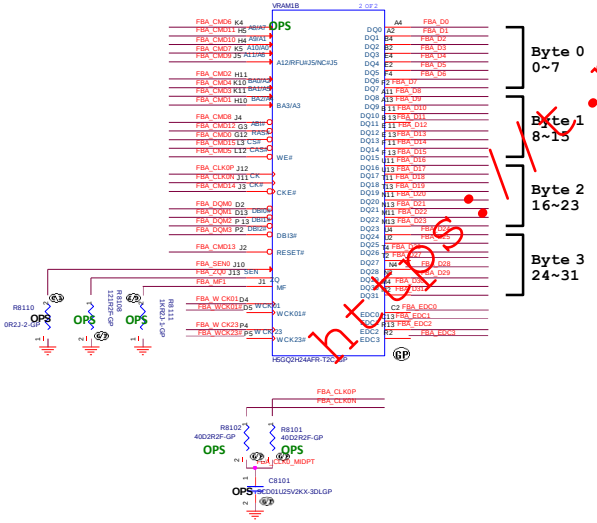




FBVREF Termination

Type	FBVREF%	Voltage	GPU_GIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Normal(MF=0)



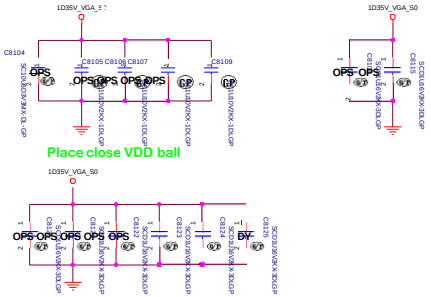
Byte 0
0~7

Byte 1
8~15

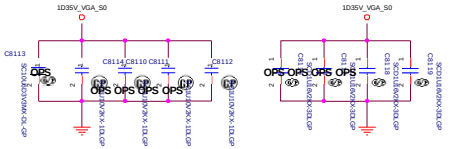
Byte 2
16~23

Byte 3
24~31

Place close VDD ball



Place close VDDQ ball



SSID = VRAM

Frame Buffer Patition A-Upper Half

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Mirrored(MF=1)

Byte 7 56~63

Byte 6 48~55

Byte 5 40~47

Byte 4 32~39

Place close VDD ball

Place close VDDQ ball

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GPU-VRAM3,4 (2/4)

Hellcat 14/15_ICL

SA

Date: Tuesday, September 17, 2019 Sheet 82 of 106

OFFPAGE-Signal

PH on EE side

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

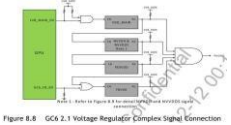

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

For VGA_CORE sequence
EE need check

075.00138.0A7C
2nd =075.00138.0F7C

84.2N702.J31
2nd =084.27002.0N31

OFFPAGE-GAP

RT8816B For NVVDDS

VGA : N17S-G1
EDP-Continuous : 30A
EDP-Peak : 60.1A

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

874.08816.0A73

VGA : N17S-G0/G2
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

ID:31/54A ,
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)
1st = 075.07321.0073

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

OCP setting
160K ohm for OCP around 96.2A setting

SS setting

Place Near GPU (NVVDDS)
1X330uF(Poscap) - PT8511 (Page85)

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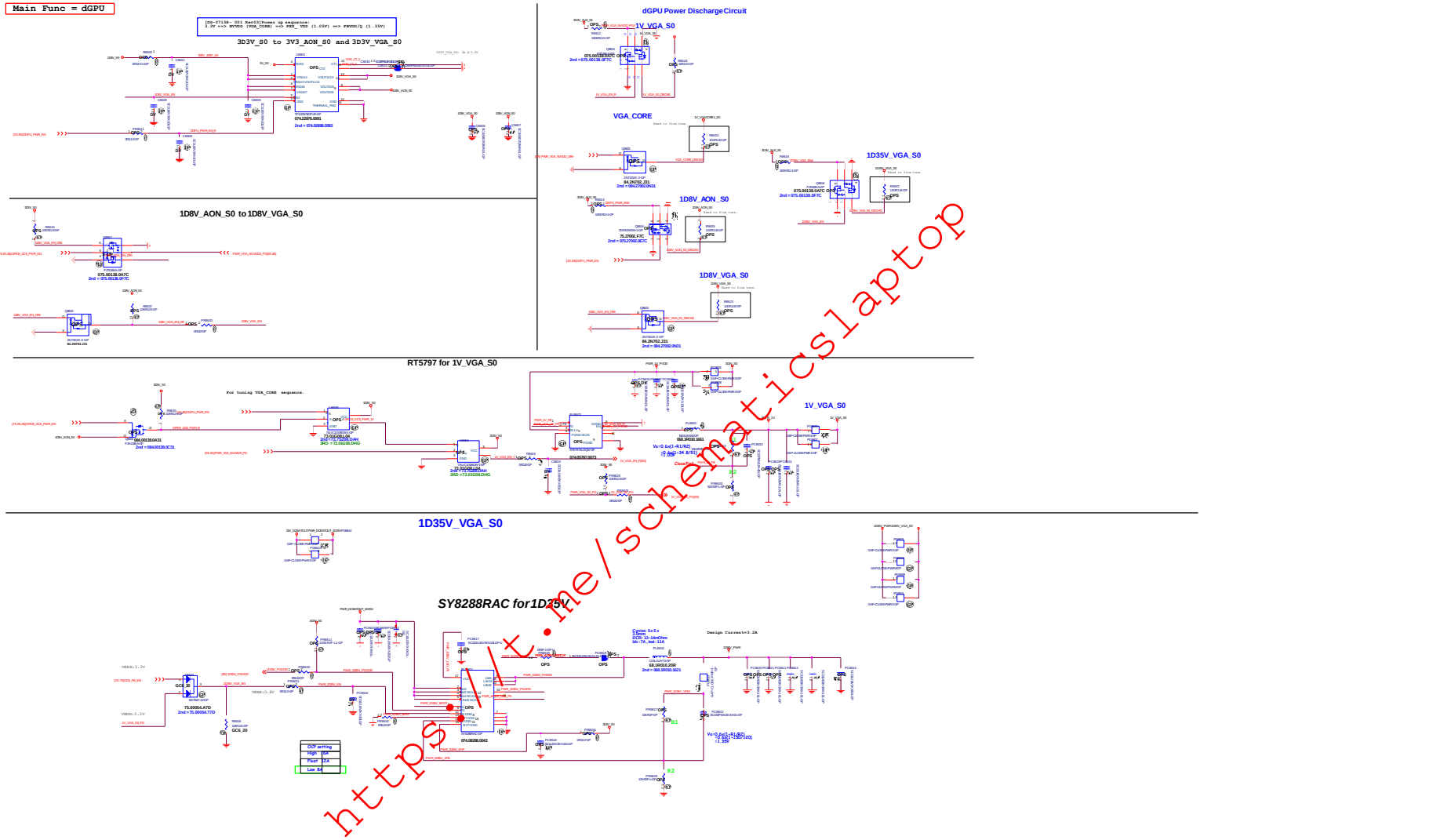
Taipei Hsien 221, Taiwan., R.O.C.

Title: GPU(RT8816A_VGA)
Size: A1
Document Number: Hellcat 14/15_ICL
Rev: SA
Date: Tuesday, September 17, 2013
Sheet 85 of 105

Main Func = dGPU



Wistron Corporation	DISCRETE VGA POWER	
MODEL NAME		SA

Main Func = TPM

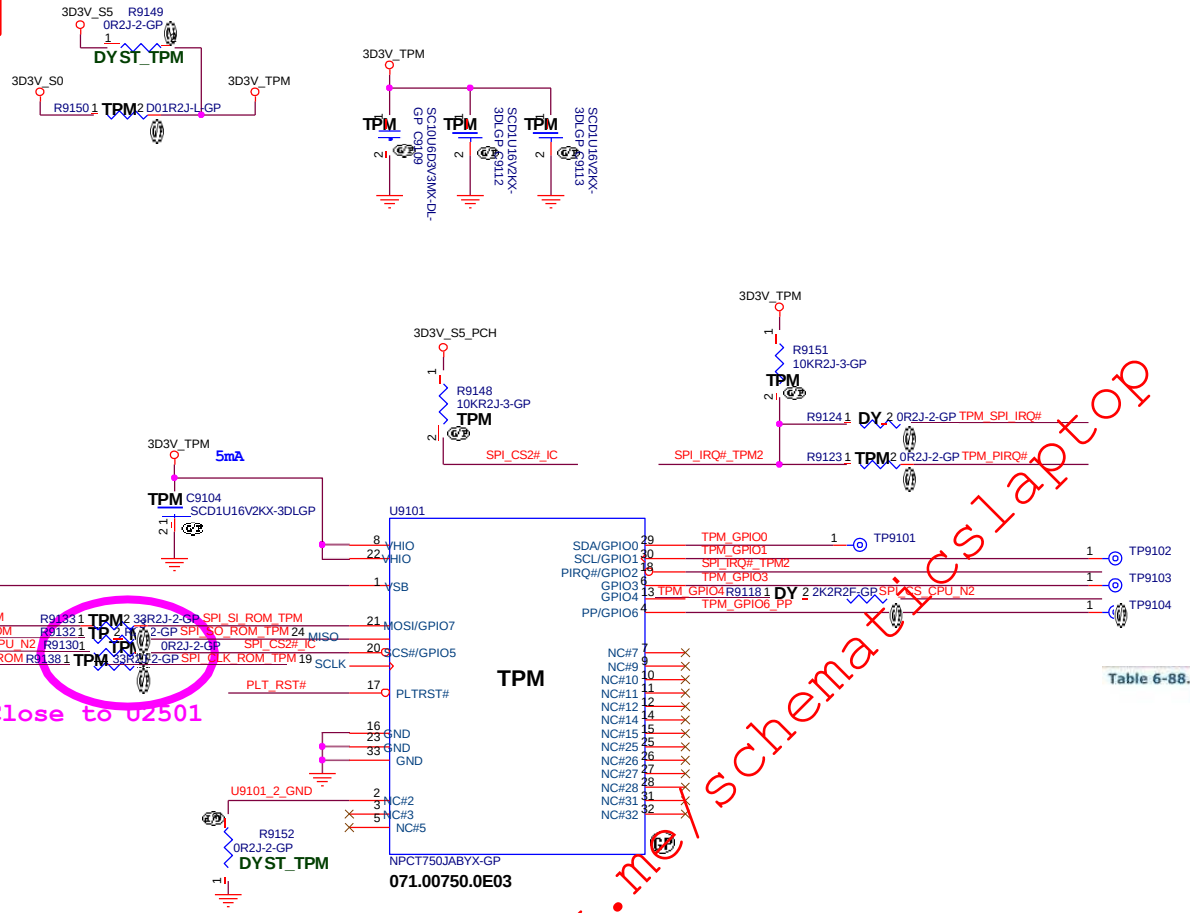
[17,61,63,66,76] PLT_RST#

[18,24,25] SPI_CLK_ROM
[18,24,25] SPI_SI_ROM
[18,24,25] SPI_SO_ROM

[18] TPM_SPI_IRQ#

[20] TPM_PIRQ#

[18] SPI_CS_CPU_N2



SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology

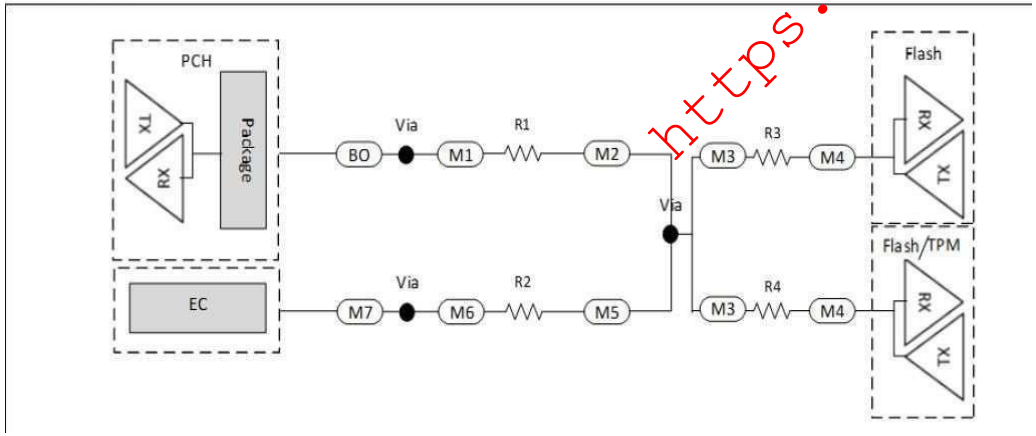


Table 6-88. SPI0 2-Load(1 Flash and 1 TPM) EC G3 Flash Sharing with Wire-OR Topology Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
B0/ M7	MS/SL	VSS	1	12.7	152.4
M1/ M6	MS/SL/DSL	VSS	1	76.2	
M2/ M5	MS	VSS	0	25.4	
M3	MS	VSS	0	12.7	
M4	MS	VSS	0	25.4	

Notes:

1. EC and PCH branch requirement: Delta between M1+M2 and M5+M6 shall not exceed 50.8mm (2inch).
2. R1 resistor should be stuffed with 0 ohm placeholder for 3.3V and 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
3. R2 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If topology uses two flash then R2 for SPI0_IO2 and SPI0_IO3 shall be same as MISO and MOSI recommendation.
4. R2 resistor should be stuffed with 75 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO2 and SPI0_IO3, if topology uses 1 flash and 1 TPM.If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
5. R3 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If topology uses two flash then R3 for SPI0_IO2 and SPI0_IO3 shall be same as MISO and MOSI recommendation.
6. R3 resistor should be stuffed with 22 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO2 and SPI0_IO3, if topology uses 1 flash and 1 TPM.If TPM use these signals, R3 value shall follow MISO and MOSI recommendation.
7. If topology uses two flash, R4 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3. If TPM use SPI0_IO2 and SPI0_IO3, R4 value shall follow MISO and MOSI recommendation
8. Minimum length for M1, M2, M4, M5 and M6: 12.7mm

<CoreDesiign>

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21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
TaipeiiHsiien221, Taiiwan, R.O.C.

Title: INT IO(TPM)

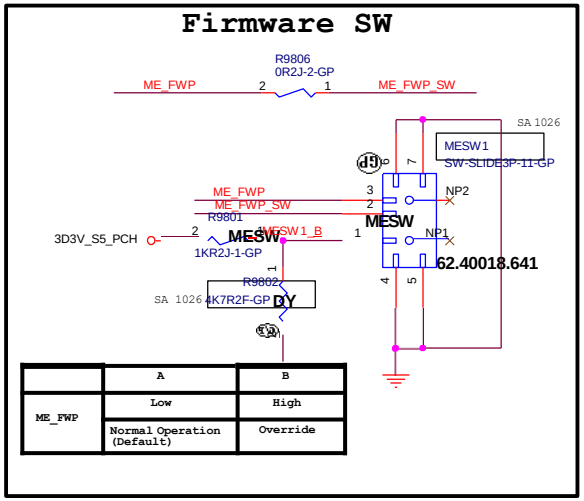
Size: A3 | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September17, 2019 | Sheet 91 of 106

Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

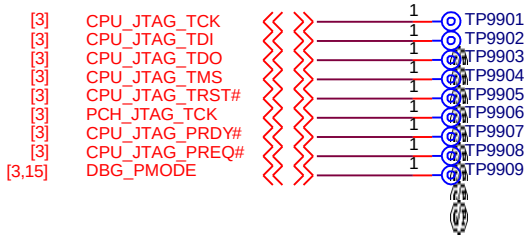
<CoreDesiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, TaiipeiiiHsiien221, Taiiiwan, R.O.C.

Title: CRT_Switch

Size: A3 | Document Number: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 98 of 106



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug (XDPdebug)***

Size	Document Number	Rev
A4	***Hellcat 14/15_ ICL***	***SA***

Date: Tuesday, September 17, 2019 Sheet 99 of 106

Main Func = CPU

1D8V_PCH_C10

C1101 DY SC47U4V3MX-3-GP C1108 SC10U6D3V3MX-

1D2V_VCCPLL_OC

C1114 SC1U10V2KX-1DLGP C1115 SC1U10V2KX-1DLGP

1D05V_VCCP_OUT_SFR

C1119 SC1U10V2KX-1DLGP C1120 SC1U10V2KX-1DLGP

1D05V_VCCST

C1121 SC1U10V2KX-1DLGP C1122 SC1U10V2KX-1DLGP

1D05V_VCCSTG

C1126 SC1U10V2KX-1DLGP C1127 SC1U10V2KX-1DLGP

Decoupling Requirements for Ice Lake U Processor for VCC1P8A

Domain	Backside cap	Primary side cap	Placement guideline[2]
VCC1P8A		1x 10uF 0402	Place as close to BGA as possible.
		1x 0603 (placeholder)	Place this post power gate path to BGAs.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-8 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPLL_OC

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPLL_OC		1x 1uF 0402	Place as close as possible to the package.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-12 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPLL

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPLL		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-14 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCST

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCST		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-16 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCSTG

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCSTG		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-18 for decoupling capacitor placements.

1D2V_S3

C1102 SC1U10V2KX-1DLGP C1103 SC1U10V2KX-1DLGP C1104 SC1U10V2KX-1DLGP C1105 SC1U10V2KX-1DLGP C1106 SC1U10V2KX-1DLGP C1107

C1109 SC10U6D3V3MX-DL-GP C1110 SC10U6D3V3MX-DL-GP C1123 SC12P50V2JN-DL-GP C1124 SC12P50V2JN-DL-GP C1128 SC12P50V2JN-DL-GP

C1111 DY C1112 DY C1113 SC10U6D3V2MX-6-GP DY C1129 SC4D7P50V2BN-2-GP C1130 SC4D7P50V2BN-2-GP C1131 SC4D7P50V2BN-2-GP

Decoupling capacitors of 12 pF (0402) and 2.2 pF (0402)
are required to suppress the broadband noise at RF frequency

C1116 SC22U6D3V3MX-1-DL-GP C1117 SC22U6D3V3MX-1-DL-GP

DY C1118 SC22U6D3V3MX-1-DL-GP

1D05V_VCCSTG_OUT_FUSE_R

C1125 SC1U10V2KX-1DLGP

Decoupling Requirements for Ice Lake U Processor for VDDQ

Domain	Backside cap	Primary side cap	Placement guideline [3]
VDDQ	6x 1uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 10uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	3x 0402 (placeholder)		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 22uF 0603		Place after the TOP DDR signal breakout. These should not be omitted on SODIMM designs, and can be removed only in Memory Down designs when the following conditions are met: 1) DRAM's are soldered down, so their decoupling is shared with the SoC. 2) DRAM's and SoC VDDQ plane copper is shared between both directly (no shorting resistors, pads or similar in the middle). 3) DRAM's are placed close to the SoC allowing that at least 5x10uF capacitors of the DRAM decoupling is within a 30mm radius from SoC Edge.
	1x 0603 (placeholder)		Place after the TOP DDR signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-10 for decoupling capacitor placements.

<CoreDesiiign>

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21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih,
TaiipeiiiHsiien221, Taiiwan, R.O.C.

Title: CPU (PowerCap2)

Size: A3 | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

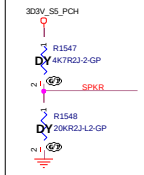
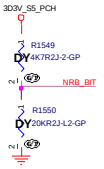
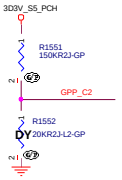
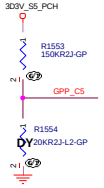
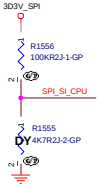
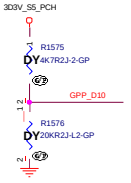
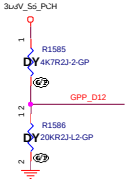
Date: Tuesday, September17, 2019 | Sheet 11 of 106

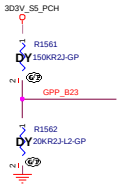
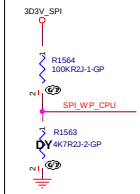
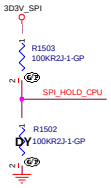
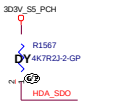
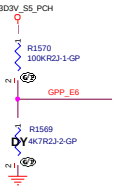
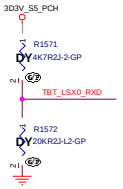
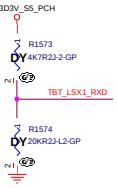
Main Func = PCH

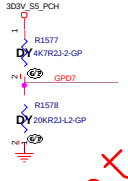
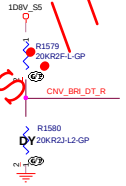
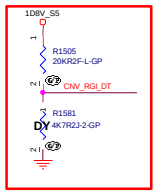
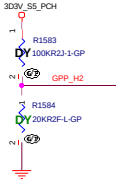
[20,27] SPKR
[20] NRB_BIT
[18] GPP_C2
[18] GPP_C5
[18] SPI_SI_CPU

[20] GPP_B23
[18] SPI_WP_CPU
[18] SPI_HOLD_CPU
[19] HDA_SDO
[3] GPP_E6
[4] TBT_LSX0_RXD
[4] TBT_LSX1_RXD

[17] GPD7
[21,61] CNV_BRI_DT_R
[21,61] CNV_RGI_DT
[3] GPP_H2
[4] GPP_D10
[4] GPP_D12

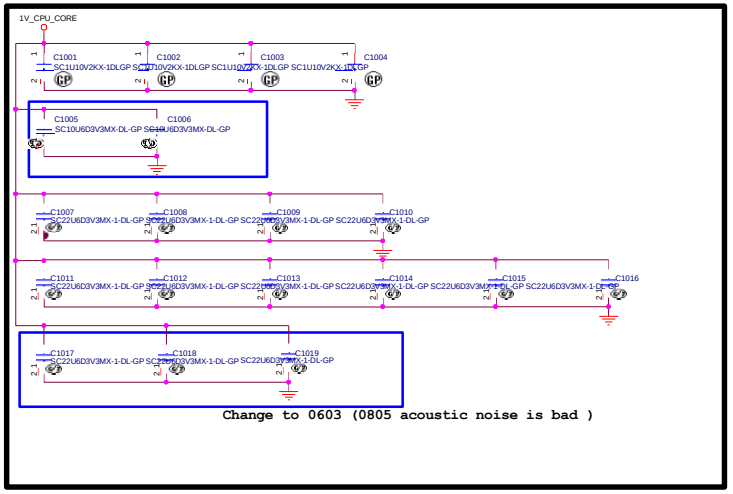
Description	Top Swap Override	No Reboot	TLS Confi-dentiality	eSPI Disable	Reserved	DDP3 I2C/TBT LSX #2/ BSSB-LS #2 pins VCC configuration	DDP4 I2C/TBT LSX #3/ BSSB-LS #3 pins VCC configuration
GPIO	GPP_B14 / SPKR / TIME_SYNC1 / GSPI0_CS#	GPP_B18	GPP_C2	GPP_C5	SPI0_MOSI	GPP_D10	GPP_D12
							
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	Enable eSPI. (Default)		DDP3 I2C/TBT LSX #2/BSSB_LS #2 pins at 1.8V	DDP4 I2C/TBT LSX #3/BSSB_LS #3 pins at 1.8V
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	Disable eSPI.	This strap should sample HIGH.	DDP3 I2C/TBT LSX #2/BSSB_LS #2 pins at 3.3V	DDP4 I2C/TBT LSX #3/BSSB_LS #3 pins at 3.3V
	20 Kt 30% internal pull-down.						

Description	CPUNSSC Clock Frequency	Reserved	Reserved	Flash Descriptor Security Override	Reserved	DDP1 I2C /TBT LSX #0 / BSSB-LS #0 pins VCC configuration	DDP2 I2C/TBT LSX #1/ BSSB-LS #1 pins VCC configuration
GPIO	GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#	SPI0_IO2	SPI0_IO3	GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO	GPP_E6	GPP_E19 / DDP1_CTRLDATA / CNV_BT_IF_SELECT / BSSB_LS0_RX	GPP_E21 / D DP2_CTRLDATA / BSSB_LS1_TX
							
LOW	38.4 MHz clock (direct from crystal) (default)			Enable security measures defined in the Flash Descriptor. (default)		1.8V	1.8V
HIGH	19.2 MHz clock (from internal divider)	This strap should sample HIGH	This strap should sample HIGH	Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	This strap should sample HIGH.	3.3V	3.3V
	20 Kt 30% internal pull-down.			20 Kt 30% internal pull-down.			20 Kt 30% internal pull-down.

Description	Reserved	Reserved	XTAL Frequency Selection	M.2 CNVi Mode Select	eSPI Flash Sharing Mode	ITP_PMODE
GPIO	ITP_PMODE	GPD7	GPP_F0 / CNV_BRI_DT / UART0_RTS#	GPP_F2 / CNV_RGI_DT / UART0_TXD	GPP_H2 / CNV_BT_I2S_SDI/ MODEM_CLKREQ	
						
LOW		This strap should sample LOW.	38.4 MHz (default)	Integrated CNVi enabled.	Master Attached Flash Sharing (MAFS) is enabled. (Default)	Reserved
HIGH	This strap should sample high.		24MHz	Integrated CNVi disabled.	Slave Attached Flash Sharing (SAFS) is enabled.	Reserved
	20 Kt 30% internal pull-up	20 Kt 30% internal pull-down.	20 Kt 30% internal pull-down.		20 Kt 30% internal pull-down.	

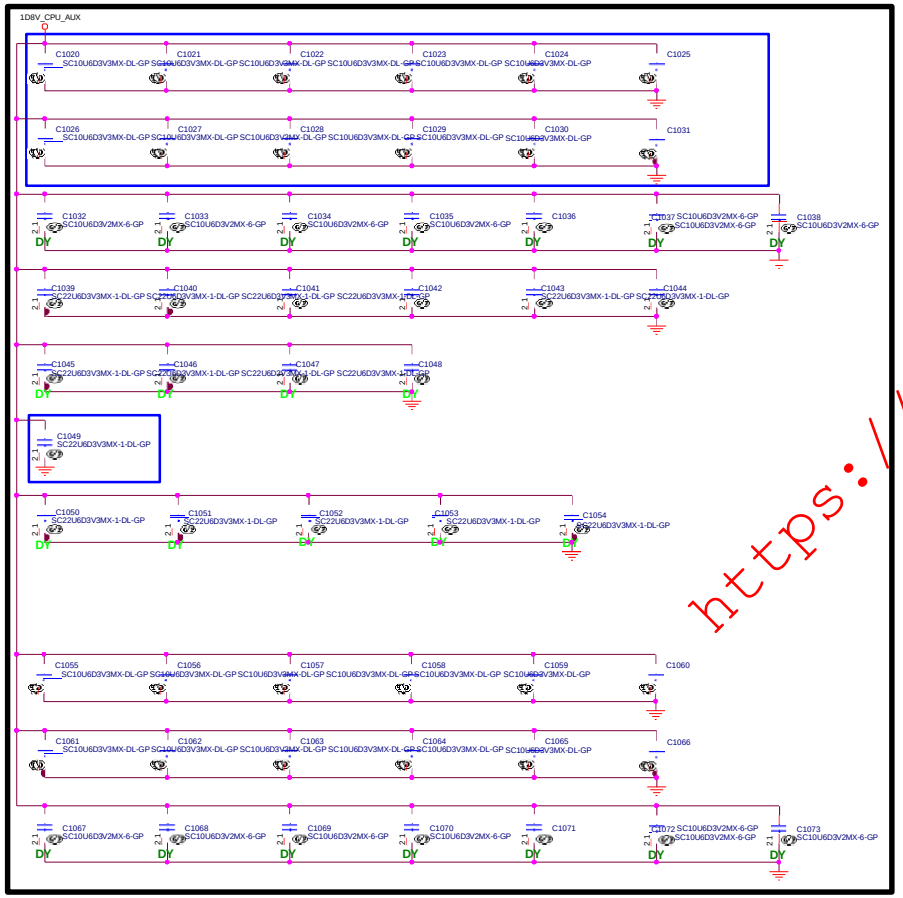
<CoreDesign>
Wistron Corporation
2F., 88, Sec. 1, HsinTaiWu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (STRAP)
Size: Document Number: A2
Hellcat 14/15_ ICL
Rev: SA
Date: Tuesday, September 17, 2019
Sheet: 15 of 106

Main Func = CPU



Decoupling Requirements for Ice Lake U Processor for VCCIN

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCIN	4x 1uF 0402		Place as close as possible to CP33, and CT33.
	2x 1uF 0402		Place closest possible to CA36 *Place for ICL U43e only.*
	1x 1uF 0402		Place as close as possible to BU10 *Place for ICL U43e only.*
		2x 10uF 0402	Place as close as possible to each U1 and AB1.
		4x 22uF 0603	Place closest possible to package near heat sink mounting hole.
		6x 22uF 0603	Place closest possible to package along the plane breakout as in Figure 10-5.
		2x 22uF 0603	Place closest possible to package along the plane breakout as in Figure 10-5. *Place for ICL U43e only.*
		1x 47uF 0805	Place closest possible to package along the plane breakout. *Place for ICL U43e only.*
		3x 47uF 0805	Place closest possible to package near heat sink mounting hole.
		1x 47uF 0805	Place closest possible to package near heat sink mounting hole. *Place for ICL U43e only.*
		2x 330uF 7343	Refer to the placement guideline in Figure 10-5.



Decoupling Requirements for Ice Lake U Processor for VCCIN_AUX

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCIN_AUX	12x 10uF 0402		Place them as directly below the BGAs as possible .
	7x 0402 (placeholder)		
		6x 22uF 0603	Place them close to VR.
		4x 0603 (placeholder)	
		1x 47uF 0805	Place them as close to the VR as possible.
		5x 0805 (placeholder)	
		2x 330uF 7343	Place them close to VR.
		12x 10uF 0402	Place them close to the BGAs on the primary side.
		7x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-6 for decoupling capacitor placements.

<CoreDesign>

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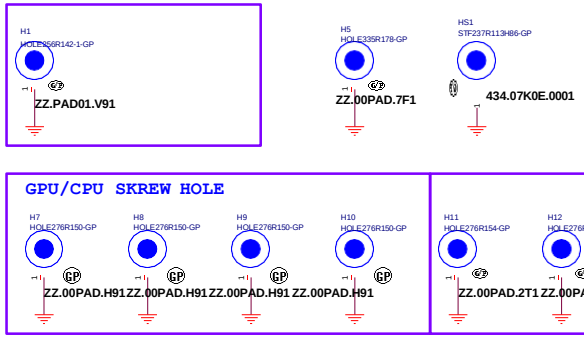
Title: CPU (CORE Power Cap1)

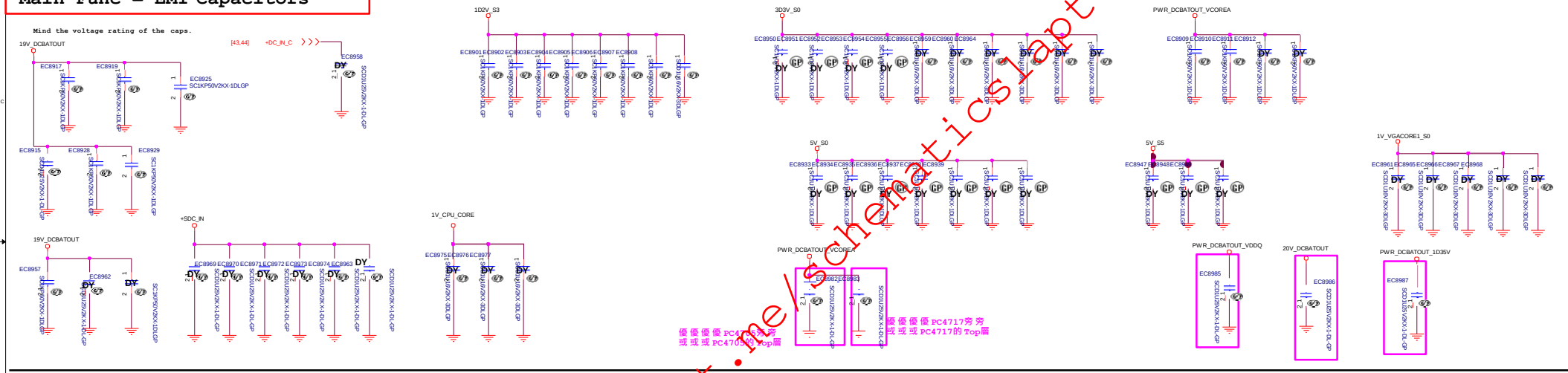
Size: A2 | DocumentNumber: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 10 of 106

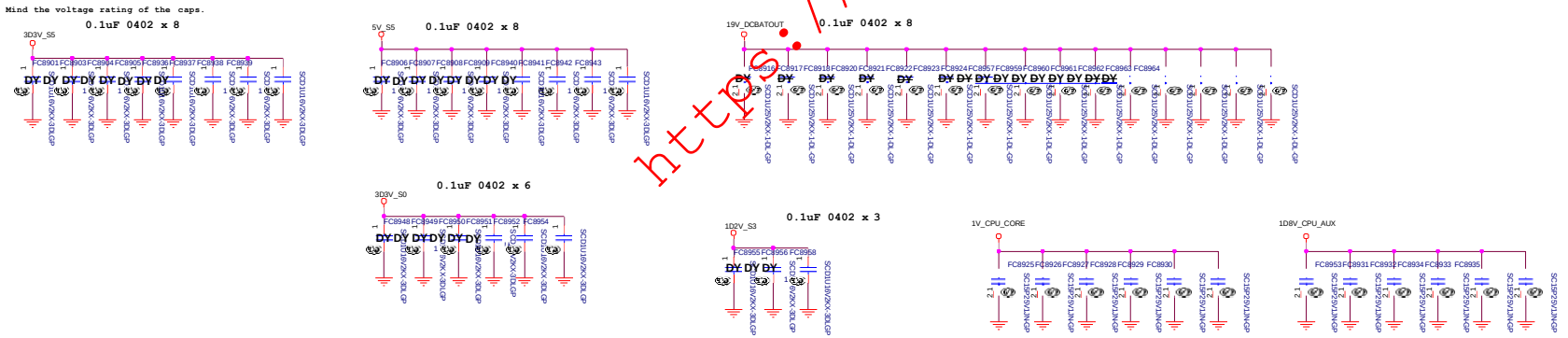
Main Func = UnusedParts



Main Func = EMI Capacitors



Main Func = RF Capacitors



<CoreDesign>
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21F., 88, Sec. 1, HsinTaiWu Rd., Hsichih,
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Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Hellcat 14/15_ ICL | Rev: SA
Date: Tuesday, September 17, 2019 | Sheet 89 of 106

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
TaiipeiiiHsiien221, Taiiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: Hellcat 14/15_ ICL | Rev: SA

Date: Tuesday, September17, 2019 | Sheet 101 of 106

Hellcat 15_MS IO Board Schematics

2020/01/30

REV : -1

DY :None Installed

HellCat15

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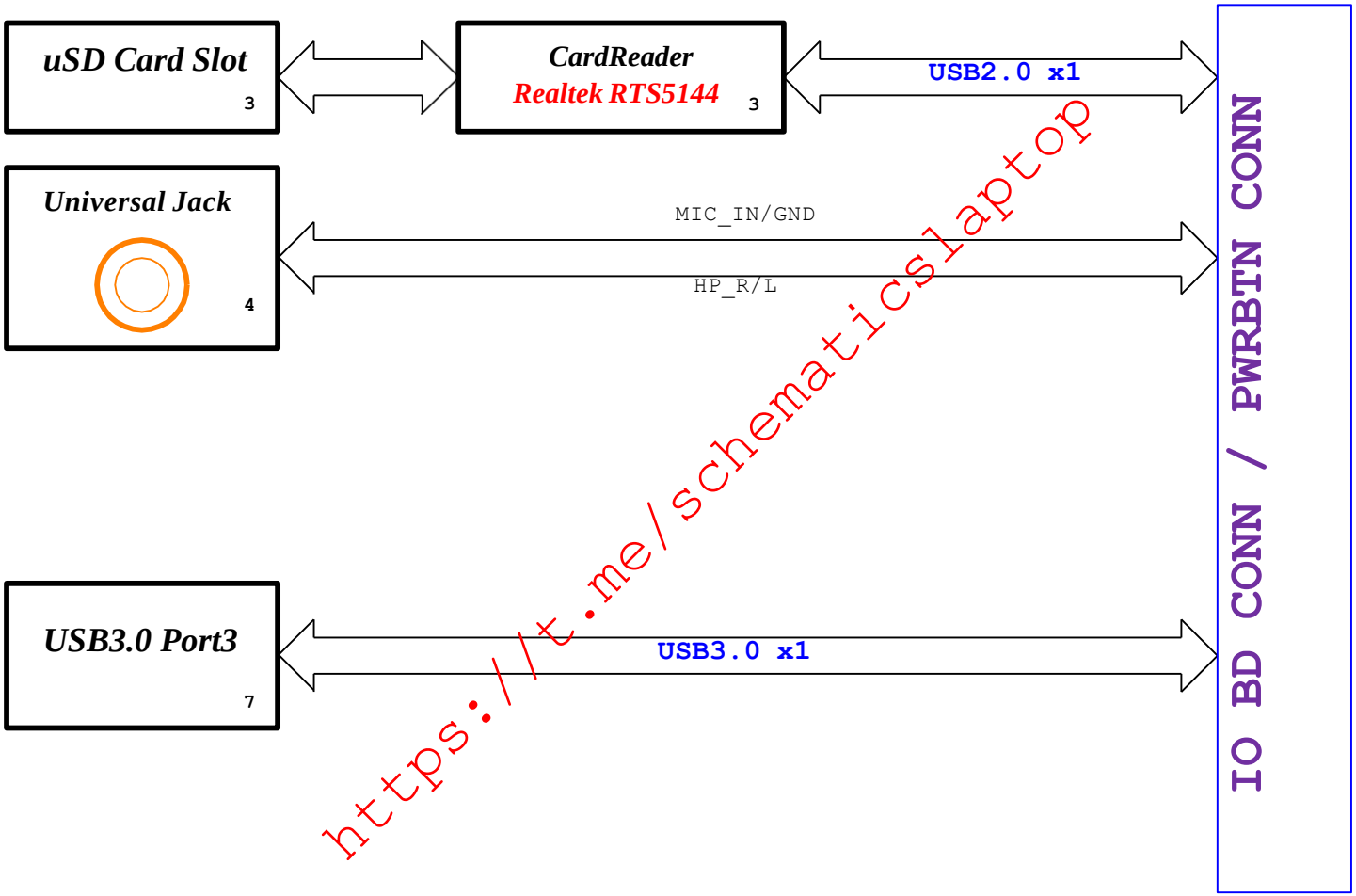
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: A4	Document Number: Hellcat15 MS IO	Rev: -1
Date: Wednesday, February 05, 2020	Sheet 1 of 10	

Hellcat 15_Mainstrin IO board Block Diagram

Project code : 4PD0JV010001
PCB P/N : 19A97
Revision : SC



HellCat15

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Block Diagram	
Size: A4	Document Number: Hellcat15 MS IO	Rev: -1
Date: Wednesday, February 05, 2020	Sheet 2 of 10	

SSID = Card Reader

8 CARD1_USB20_N
8 CARD1_USB20_P

The maximum range of the PMOS output current in RTS5144 (Card Reader TX) is 400mA

3D3V_S0
R309 0R3J-0-U-GP
3D3V_CARDREADER_S0
EC301 DY Do Not Stuff
C301 SCD47U6D3V3KX-DLGP
C302 SCD1U16V2KX-3DLGP

Remove R305、R306

EL301
CARD1_USB20_N
CARD1_USB20_P
CARD1_USB20_CON_N_R
CARD1_USB20_CON_P_R
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061

Layout note:
3D3V_CARD_S0 30mils

U301
3V3_IN
3V3_IN
3V3_IN
CARD_3V3
DP
DM
SD_CD#
SD_DAT1
RREF
IS_INS#
48MHZ_IN
AV18
GPIO
SDREG
SP1
SP2
SP3
SP4
SP5
SP6
SP7
SP8
SP9
SP10
GND
RTS5144-GR-GP
071.05144.0003

Layout note:
V18 12mils
V18
SDREFG
C303 SC1U10V2KX-1DLGP
C304 SC1U10V2KX-1DLGP
Layout note:
SDREFG 12mils
SD_WP
SD_DATA0
SD_CLK_5170
SD_CMD
SD_DATA3
SD_DATA2
R302 0R2J-2-GP
SD_CLK

3D3V_CARD_S0
R303 6K2R2F-GP
RREF
Layout note:
RREF 12mils

3D3V_CARD_S0
C305 SCD1U16V2KX-3DLGP
EC302 DY Do Not Stuff
C306 SCA47U6D3V3KX-DLGP
C307 DY Do Not Stuff

Do Not Stuff AFTP301
3D3V_CARD_S0
400mA
SD1
VDD
CD
W/P
DAT0
DAT1
DAT2
DAT3
VSS1
VSS2
GND
GND
GND
GND
CLK
CMD
SD_CD#
SD_WP_CON
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
SD_CLK
SD_CMD
SKT-SDCARD-88-GP
022.S0013.0011
AFTP309 Do Not Stuff

Do Not Stuff AFTP302
Do Not Stuff AFTP303
Do Not Stuff AFTP304
Do Not Stuff AFTP305
Do Not Stuff AFTP306
Do Not Stuff AFTP307
Do Not Stuff AFTP308
SD_CLK
SD_CD#
SD_WP_CON
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3

3D3V_S0
R301 10KR2J-3-GP
Q301
G
D
S
SD_WP
SD_WP_CON
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0N31

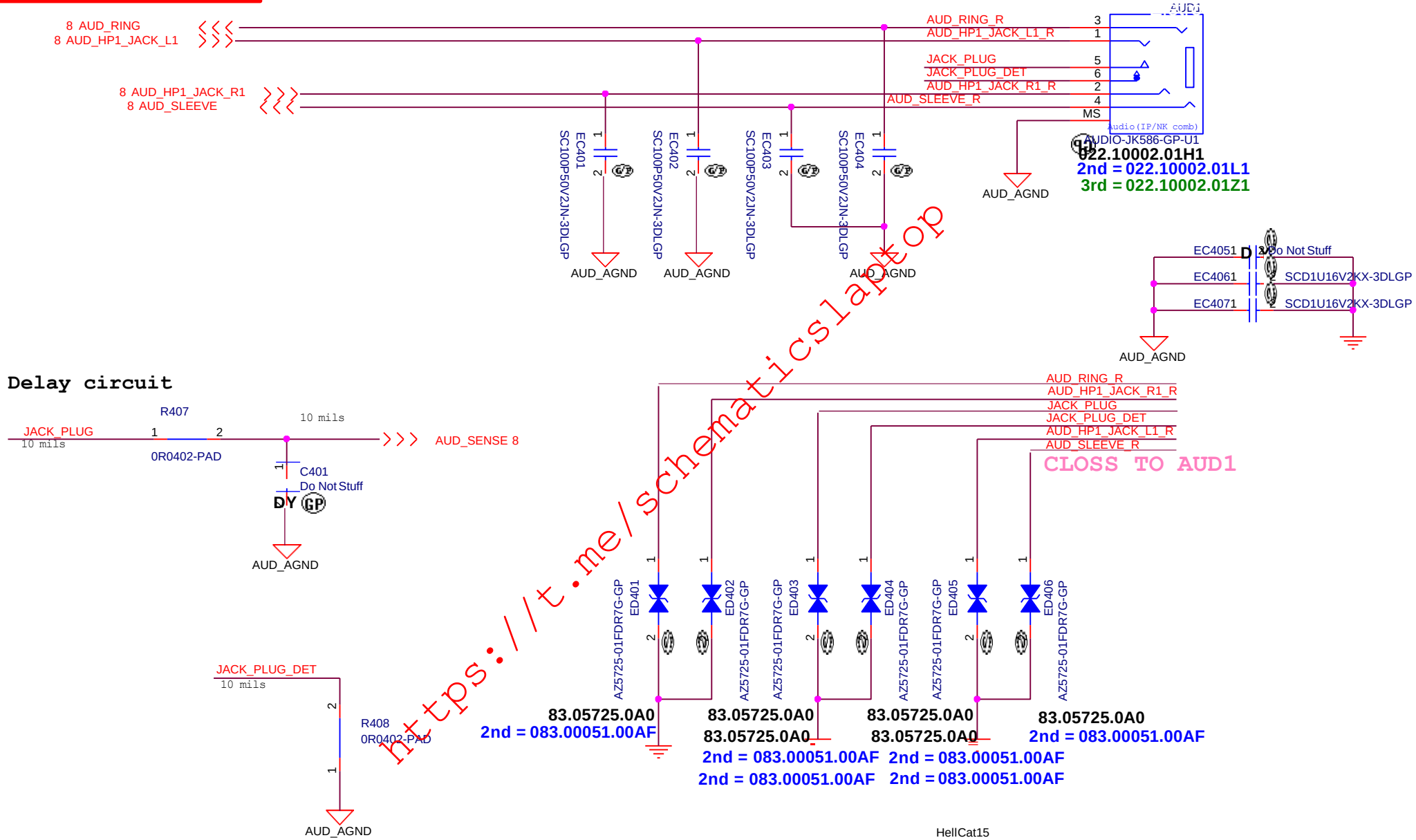
For EMI reserve
SD_WP_CON
SD_CD#
SD_CMD
SD_DATA3
SD_DATA2
SD_DATA1
SD_DATA0
SD_CLK
EC303 EC304 EC305 EC306 EC307 EC308 EC309 EC310
SCD6B8P50V2CN-DL-GP

HellllCat15

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih,
TaiipeiiHsiien221, Taiiiwan, R.O.C.

Tiitle: Card Reader-RTS5144
Size: A3
Document Number: Hellcat15 MS IO
Rev: -1
Date: Wednesday, February 05, 2020
Sheet 3 of 10

SSID = Audio IO



HellCat15

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUD IO**		
Size: A4	Document Number: **Hellcat 15MS IO**	Rev: -1
Date: Wednesday, February 05, 2020	Sheet 4 of 10	

SSID = USB3.0

Remove R704、R705

8 USB2_USB30_TX_N
8 USB2_USB30_TX_P
8 USB2_USB30_RX_N
8 USB2_USB30_RX_P
8 USB2_USB20_N
8 USB2_USB20_P

EL701
USB2_USB20_P 1 — 2 USB2_USB20_CON_P
USB2_USB20_N 4 — 3 USB2_USB20_CON_N
DLM0NSN900HY2L-GP
068.09002.2001
2nd = 68.02002.061

3D3V_RE_S5
C702 SC1U10V2KX-1DLGP
C701 SC01U10V2KX-3DLGP

PCH (TX, RX) — Redriver (RX1, TX1, TX2, RX2) — Connector

3D3V_S5 3D3V_RE_S5
R715 1 — 2 0R2J-2-GP

U701
PS8719BTQFN24GTR2-A0-GP
071.08719.0A03

From Host
USB2_USB30_TX_P / USB2_USB30_TX_N — SCD1U16V1KX-5-GP — USB2_USB30_TX_C_P / USB2_USB30_TX_C_N
USB2_USB30_TX_CON_P / USB2_USB30_TX_CON_N — SCD1U16V1KX-5-GP — USB2_USB30_TX_RE_P / USB2_USB30_TX_RE_N
to USB3.0 conn

USB2_USB30_RX_RE_P / USB2_USB30_RX_RE_N — R723 / R724 0R1J-GP — USB2_USB30_RX_C_P / USB2_USB30_RX_C_N — C706 / C705 SCD1U16V1KX-5-GP — USB2_USB30_RX_CON_P / USB2_USB30_RX_CON_N
to USB3.0 conn
From Host

A_DE0_1, A_DE1_1, A_EQ0_1, A_EQ1_1
Do Not Stuff
TP701 1 U3_PD#_EC
I2C_EN
R701 4K99R1F-GP
REXT
TST

B_DE0_1, B_DE1_1, B_EQ0_1, B_EQ1_1
R706 R707 R708 R709 R710 Do NotStuff
R711 4K7R1J-GP
R712 4K7R1J-GP
R713 Do NotStuff
R714 Do NotStuff

ED701
USB2_USB20_CON_P
USB2_USB20_CON_N
83.05315.0A0
AZ5315-02F-GP
2nd = 075.5V0X2.0070

ED702
USB2_USB30_TX_CON_P / USB2_USB30_TX_CON_N / USB2_USB30_RX_CON_P / USB2_USB30_RX_CON_N
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

USB30_VCCC
USB3
VBUS, D-, D+, GND
STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+
USB2_USB30_RX_CON_N / USB2_USB30_RX_CON_P
USB2_USB30_TX_CON_N / USB2_USB30_TX_CON_P
USB2_USB20_CON_N / USB2_USB20_CON_P
SKT-USB13-457-GP
022.10005.0ZE1
2nd = 022.10005.0GR1
NB要要1st、2nd對對

USB3.0 Port1

USB30_VCCC
C711 SCD1U10V2KX-3DLGP
C712 SC1U10V2KX-1DLGP
C713 SC22UE820V3MX-1DL-GP
C714 Do NotStuff
FC701 FC702 Do NotStuff Do NotStuff

USB 3.0 Re-driver Pull High / Low

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~150K
[A_DE1, A_DE0]==
- LL: 3.5dB de-emphasis (default)
- LH: No de-emphasis
- HL: 2.7dB de-emphasis
- HH: 5dB de-emphasis

Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~150K
[B_DE1, B_DE0]==
- LL: 3.5dB de-emphasis (default)
- LH: No de-emphasis
- HL: 2.7dB de-emphasis
- HH: 5dB de-emphasis

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~150K
[A_EQ1, A_EQ0] ==
- LL: program EQ for channel loss up to 9.5dB (default)
- LH: program EQ for channel loss up to 13dB

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~150K
[B_EQ1, B_EQ0] ==
- LL: program EQ for channel loss up to 9.5dB (default)
- LH: program EQ for channel loss up to 13dB
- HL: program EQ for channel loss up to 4.5dB
- HH: program EQ for channel loss up to 7.5dB

LFPS swing adjust. 3.3V tolerant. Internally pulled down at ~150K .
TST ==
- L: Normal LFPS swing (default)
- H: Tune down LFPS swing

HellCat15

Wistron Corporation
2F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 HUB / CONN

Size	Document Number	Rev
A2	Hellcat15 MS IO	-1

Date: Wednesday, February 05, 2020 Sheet 7 of 10

SSID:IO connect

Pin define by follow layout routing

Card Reader

3 CARD1_USB20_N
3 CARD1_USB20_P

Audio

4 AUD_HP1_JACK_L1
4 AUD_HP1_JACK_R1
4 AUD_SENSE
4 AUD_RING
4 AUD_SLEEVE

USB3.0

7 USB2_USB20_N
7 USB2_USB20_P
7 USB2_USB30_TX_N
7 USB2_USB30_TX_P
7 USB2_USB30_RX_N
7 USB2_USB30_RX_P

Finger Print

9 FPR_SCAN#
9 PM_SLP_S4#
9 KBC_PWRBTN#_R
9 LID_CL_NB#
9 FP1_USB20_P
9 FP1_USB20_N

34AWG

AUDIO
AUD_HP1_JACK_L1
AUD_SENSE
AUD_SLEEVE
AUD_SLEEVE
AUD_SLEEVE
AUD_RING
AUD_RING
AUD_RING
AUD_HP1_JACK_R1
AUD_AGND

USB3.1 PORT1
Coaxial
USB2_USB30_RX_N
USB2_USB30_RX_P
USB2_USB30_TX_N
USB2_USB30_TX_P

Card Reader
CARD1_USB20_P
CARD1_USB20_N

USB3.1 PORT1
USB2_USB20_N
USB2_USB20_P

FINGER PRINTER
FP1_USB20_N
FP1_USB20_P
LID_CL_SIO_TAB#
FPR_SCAN#
PM_SLP_S4#
KBC_PWRBTN#_R
LID_CL_NB#

RTC
+RTC_VCC
3D3V_S0
3D3V_S5
3D3V_AUX_S5
USB30_VCCC

IOBD1
STAR-CON40-8-GP
020.F0847.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040

+RTC_VCC
R801
1KR2J-1-GP
+RTC_VCC_CON
RTC1
ETY-CON2-22-GP-U
20.F1841.002
2nd = 20.F1639.002
AFTP801
AFTP802

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff

GMR Sensor

3D3V_S5
3D3V_AUX_S5
R910 Do Not Stuff DY
R909 100KR2J-1-GP
R912 Do Not Stuff DY
R911 100KR2J-1-GP
GMR1
HGDEDM013A-GP
074.00013.00BJ
D902
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
LID_CL_SIO_TAB#_A
LID_CL_TAB#
LID_CL_NB#
GMR_VDD_R
NON LID_WAKE
R913 Do Not Stuff
R914 0R2J-2-GP
C902 SCD1U16V2KX-3DLGP
20180118 Change part number

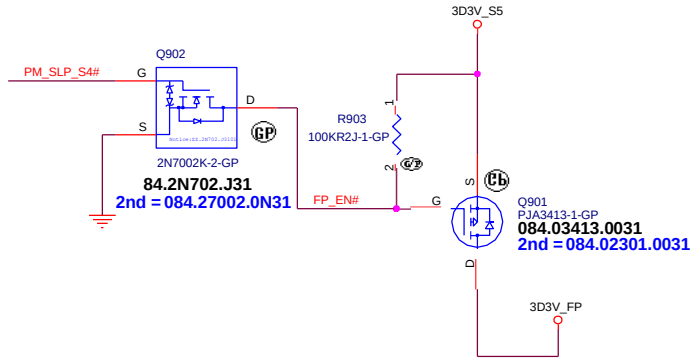
HellllCat15

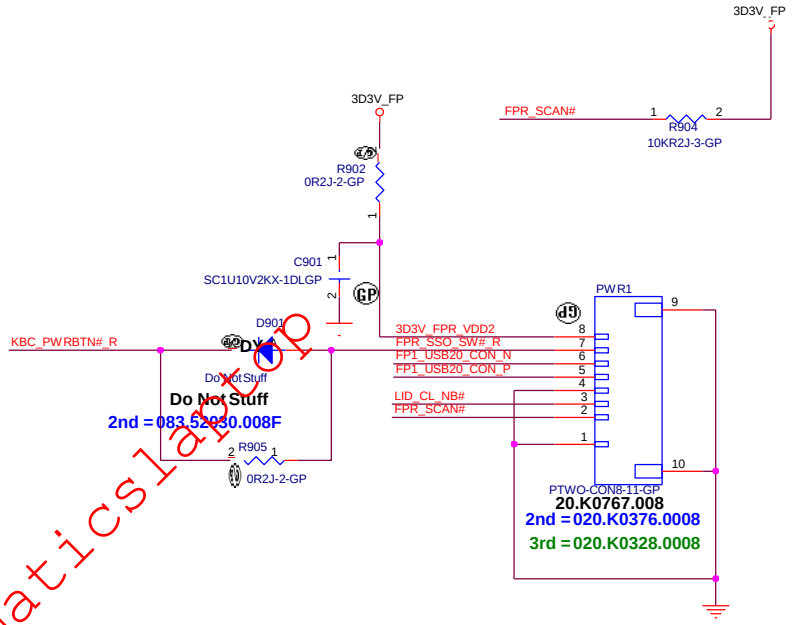
Wistron Corporation
21F, 88, Sec.1, HsinTaiiWu Rd., Hsiichiih, Taiipeiii-Hsiien221, Taiiiwan, R.O.C.

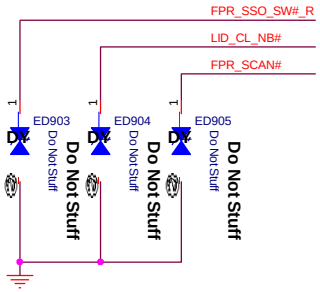
Title: IO Connector
Size: A3
Document Number: Hellcat15 MS IO
Rev: -1
Date: Wednesday, February 05, 2020
Sheet 8 of 10

SSID = Finger Print

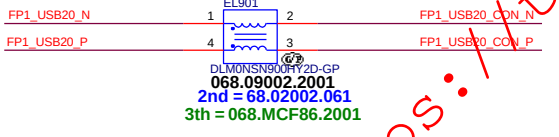
8 FPR_SCAN#
8 FP1_USB20_P
8 FP1_USB20_N
8 PM_SLP_S4#
8 LID_CL_NB#
8 KBC_PWRBTN#_R

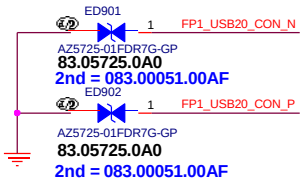






Remove R907、R908





FP_Pin_define

PIN 序号	PIN 名	说明
1	VBUS	AVDD(3.3V)
2	Power button	Power button signal
3	USB_DN	USB_N
4	USB_DP	USB_P
5	GND	系统地
6	LID closed	LID closed signal
7	GPIO_key	GPIO
8	ID(GND)	ID 检测脚

HelllllCat15

Wistron Corporation
21F, 88, Sec.1, HsinTaiiWu Rd., Hsichih,
Taipeiii-Hsiien221, Taiiwan, R.O.C.

Title: Finger Print

Size	Document Number	Rev
A3	Hellcat15 MS IO	-1

Date: Wednesday, February 05, 2020 Sheet 9 of 10

Change History

Version	Date	Page	Change Description

HellCat15

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change Note

Size	Document Number	Rev
A4	Hellcat15 Mainstrin IO	-1

Date: Wednesday, February 05, 2020 Sheet 10 of 10

Hellcat MS 14 AMD IO Board Schematics

Hellcat MS 14 ICL IO Board Schematics

2020/01/31

REV : A00

DY :None Installed

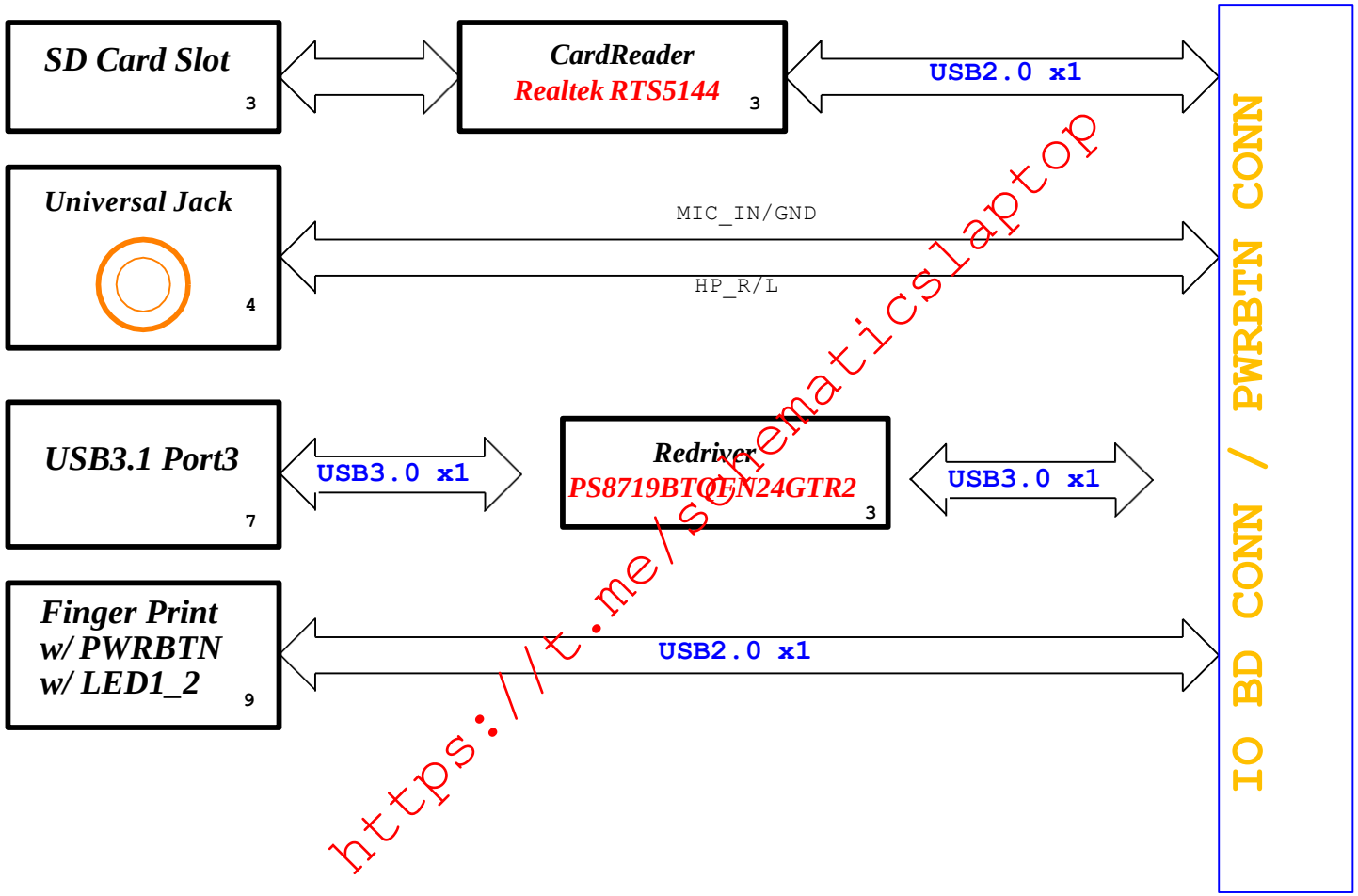
Hellcat 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: Hellcat MS 14 AMD	Rev: A00
Date: Friday, January 31, 2020	Sheet 1 of 10	

Hellcat MS 14 AMD IO board Block Diagram

Project code : 4PD0JV010001
PCB P/N : 19A89
Revision : SC



Hellcat 14

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Title: Block Diagram		
Size: A4	Document Number: Hellcat MS 14 AMD	Rev: A00
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SSID = Card Reader

[8] CARD1_USB20_N
[8] CARD1_USB20_P

The maximum range of the PMOS output current in RTS5144 (Card Reader TQ) is 400mA

3D3V_S0
R309 D01R3F-L-GP
EC301 DY SCD1U16V2KX-3DLGP
C301 SC47U6D3V3KX-DLGP
C302 SCD1U16V2KX-3DLGP
3D3V_CARDREADER_S0

U301 RTS5144-GR-GP
071.05144.0003
3V3_IN 3V3_IN 3V3_IN
CARD_3V3
DP DM
SD_CD# SD_DAT1
RREF
XS_INS# 48MHZ_IN
AV18 GPIO SDREG
SP1 SP2 SP3 SP4 SP5 SP6 SP7 SP8 SP9 SP10
GND

Layout note:
V18 12mils
V18
C303 SC1U10V2KX-1DLGP
C304 SC1U10V2KX-1DLGP
SDREFG
Layout note:
SDREFG 12mils
SD_WP
SD_DATA0
SD_CLK_5170
SD_CMD
SD_DATA3
SD_DATA2
R302 0R2J-2-GP
SD_CLK

EL301 DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001
CARD1_USB20_N
CARD1_USB20_P
CARD1_USB20_CON_N_R
CARD1_USB20_CON_P_R

Layout note:
3D3V_CARD_S0 30mils
3D3V_CARD_S0
CARD1_USB20_CON_P_R
CARD1_USB20_CON_N_R
SD_CD#
SD_DATA1
R303 6K2R2F-GP
RREF
Layout note:
RREF 12mils

3D3V_CARD_S0
C305 SCD1U16V2KX-3DLGP
EC302 DY SCD1U16V2KX-3DLGP
C306 SC47U6D3V3KX-DLGP
C307 DY SC10U6D3V3MX-11-GP

3D3V_CARD_S0
400mA
AFTE14P-GP AFTP301
SD1 SKT-SDCARD-85-GP
062.10002.0941
2nd = 062.10002.0741
VDD
DAT0 DAT1 DAT2 DAT3
CMD CD CLK WP
VSS1 VSS2
NP1 NP2
GND GND
SD_DATA0 SD_DATA1 SD_DATA2 SD_DATA3
SD_CMD SD_CD# SD_CLK SD_WP_CON
AFTP309 AFTE14P-GP

AFTE14P-GP AFTP302 SD_CLK
AFTE14P-GP AFTP303 SD_CD#
AFTE14P-GP AFTP304 SD_WP_CON
AFTE14P-GP AFTP305 SD_DATA0
AFTE14P-GP AFTP306 SD_DATA1
AFTE14P-GP AFTP307 SD_DATA2
AFTE14P-GP AFTP308 SD_DATA3

3D3V_S0
R301 10KR2J-3-GP
Q301 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0N31
SD_WP
SD_WP_CON
G D S

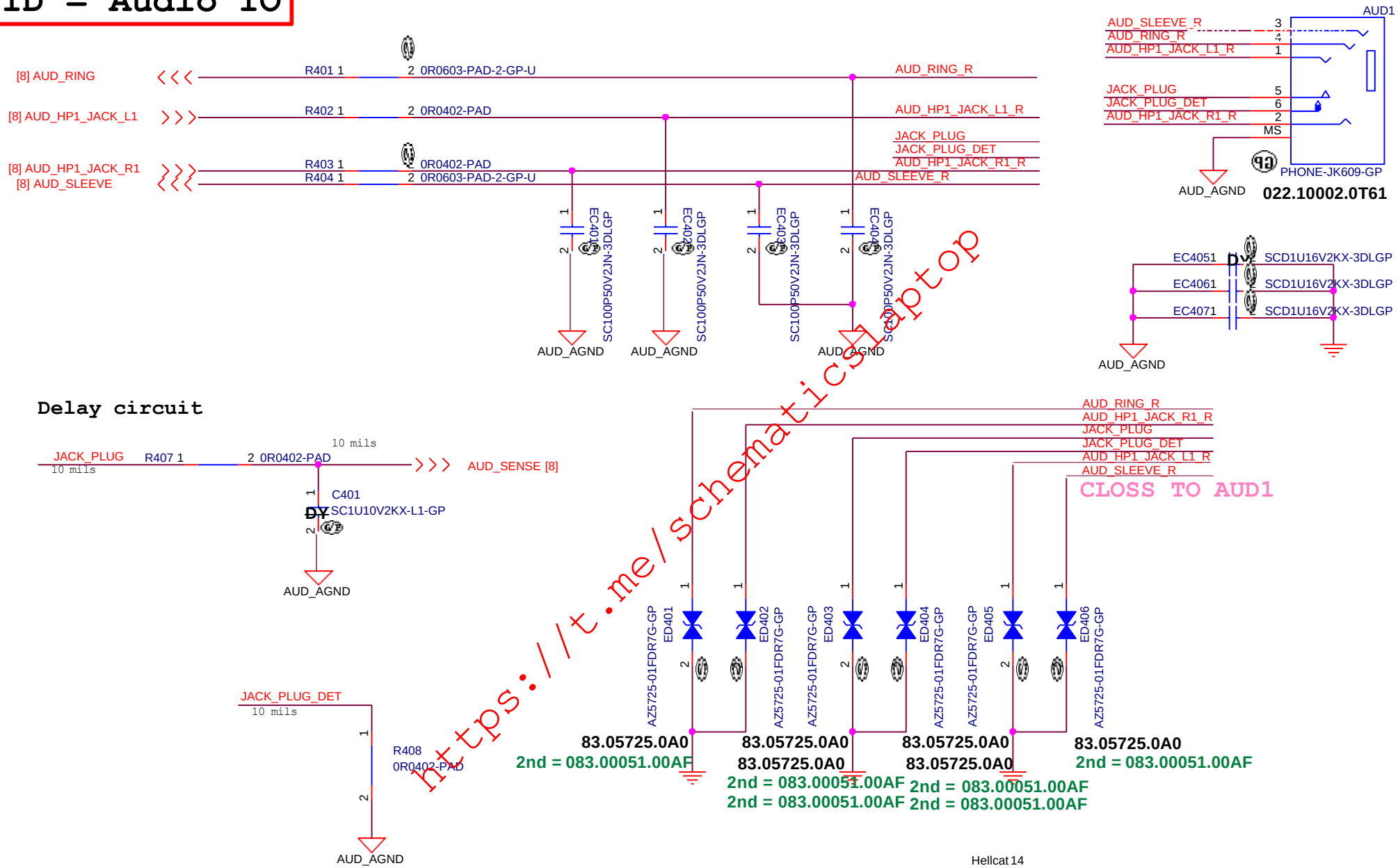
For EMI reserve
SD_WP_CON
SD_CD#
SD_CMD
SD_DATA3
SD_DATA2
SD_DATA1
SD_DATA0
SD_CLK
EC303 EC304 EC305 EC306 EC307 EC308 EC309 EC310
SCD6D8P50V2CN-DL-GP

Hellllcat14

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, TaiipeiiHsiien221, Taiiiwan, R.O.C.

Tiitle: Card Reader-RTS5144
Size: A3
Document Number: Hellcat MS 14 AMD
Rev: A00
Date: Friday, January 31, 2020
Sheet 3 of 10

SSID = Audio IO



Hellcat 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUD IO**

Size	Document Number	Rev
A4	Hellcat MS 14 AMD	A00

Date: Friday, January 31, 2020 Sheet 4 of 10

SSID = USB3.0

[8] USB2_USB30_TX_N
[8] USB2_USB30_TX_P
[8] USB2_USB30_RX_N
[8] USB2_USB30_RX_P
[8] USB2_USB20_N
[8] USB2_USB20_P

EL701
USB2_USB20_P
USB2_USB20_N
USB2_USB20_CON_P
USB2_USB20_CON_N
DLM0NSN900HY2GP
068.09002.2001
2nd = 068.09002.2001 3rd = 068.MCF86.2001

3D3V_RE_S5
C702 SC1U10V2KX-1DLGP
C701 SC1U10V2KX-3DLGP

PCH TX RX
Redriver RX1 TX1 TX2 RX2
Connector

3D3V_S5 3D3V_RE_S5
R715 D01R2J-L-GP

U701
VDD VDD
A_INP A_INN
A_OUTP A_OUTN
A_DE0/SCL_CTL
A_DE1/NC#18
A_EQ0/NC#17
A_EQ1/SDA_CTL
PD#
I2C_EN
B_INP B_INN
B_OUTP B_OUTN
B_DE0/I2C_ADDR0
B_DE1/NC#6
B_EQ0/NC#2
B_EQ1/I2C_ADDR1
REXT TST/NC#14
GND GND GND
PS8719BTQFN24GTR2-A0-GP
071.08719.0A03

From Host
to USB3.0 conn
USB2_USB30_TX_P
USB2_USB30_TX_N
USB2_USB30_TX_CON_P
USB2_USB30_TX_CON_N
SCD1U16V1KX-5-GP
C708 C707 C703 C704
USB2_USB30_TX_C_P
USB2_USB30_TX_C_N
USB2_USB30_TX_RE_P
USB2_USB30_TX_RE_N
A_DE0_1 A_DE1_1 A_EQ0_1 A_EQ1_1
TPAD14-OP-GP TP701 U3_PDe_EC
R701 4K99R1F-GP

USB2_USB30_RX_RE_P
USB2_USB30_RX_RE_N
R723 R724 0R1J-GP
USB2_USB30_RX_CON_P
USB2_USB30_RX_CON_N
to USB3.0 conn
From Host
USB2_USB30_RX_C_P
USB2_USB30_RX_C_N
C706 C705 SCD1U16V1KX-5-GP
USB2_USB30_RX_P
USB2_USB30_RX_N
B_DE0_1 B_DE1_1 B_EQ0_1 B_EQ1_1

3D3V_S5
A_DE0_1 A_DE1_1 B_DE0_1 B_DE1_1 A_EQ0_1 A_EQ1_1 B_EQ0_1 B_EQ1_1 TST
R706 R707 R708 R709 R710 R711 R712 R713 R714 4K7R1J-GP

ED701
USB2_USB20_CON_P
USB2_USB20_CON_N
83.05315.0A0
AZ5315-02F-GP
2nd = 075.5V0X2.0070

ED702
USB2_USB30_TX_CON_P
USB2_USB30_TX_CON_N
USB2_USB30_RX_CON_P
USB2_USB30_RX_CON_N
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

USB30_VCCC
USB3
VBUS
D- D+
STDA_SSRX- STDA_SSRX+
STDA_SSTX- STDA_SSTX+
GND GND
SKT-USB13-457-GP
022.10005.0ZE1
2nd = 022.10005.0GR1

USB3.0 Port1
USB30_VCCC
C711 SC1U10V2KX-3DGP
C712 SC1U10V2KX-1DLGP
C713 SC1U20V6KX-1DLGP
C714 SC2X2U20V6KX-1DLGP

USB 3.0 Re-driver Pull High / Low

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~150K
[A_DE1, A_DE0]==
LL: 3.5dB de-emphasis (default)
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~150K
[B_DE1, B_DE0]==
LL: 3.5dB de-emphasis (default)
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~150K
[A_EQ1, A_EQ0] ==
LL: program EQ for channel loss up to 9.5dB (default)
LH: program EQ for channel loss up to 13dB

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~150K
[B_EQ1, B_EQ0] ==
LL: program EQ for channel loss up to 9.5dB (default)
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

LFPS swing adjust. 3.3V tolerant. Internally pulled down at ~150K .
TST ==
L: Normal LFPS swing (default)
H: Tune down LFPS swing

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 HUB / CONN
Size: A2 | Document Number: Hellcat MS 14 AMD | Rev: A00
Date: Friday, January 31, 2020 | Sheet 7 of 10

SSID:IO connect

Pin define by follow layout routing

Card Reader

[3] CARD1_USB20_N
[3] CARD1_USB20_P

Audio

[4] AUD_HP1_JACK_L1
[4] AUD_HP1_JACK_R1
[4] AUD_SENSE
[4] AUD_RING
[4] AUD_SLEEVE

USB3.0

[7] USB2_USB20_N
[7] USB2_USB20_P
[7] USB2_USB30_TX_N
[7] USB2_USB30_TX_P
[7] USB2_USB30_RX_N
[7] USB2_USB30_RX_P

Finger Print

[9] FPR_SCAN#
[9] KBC_PWRBTN#_R
[9] LID_CL_NB#
[9] FP1_USB20_P
[9] FP1_USB20_N
[8] APU_SLP_S5#

20191205

RTC CONN

+RTC_VCC
R901 1KR2J-1-GP
+RTC_VCC_CON
RTC1 ETY-CON2-22-GP-U
20.F1841.002
2nd = 20.F1639.002
AFTP901
AFTP902

H1 HOLE256R142-1-GP
ZZ.PAD01.V91
H2 HOLE256R119-GP
ZZ.PAD01.V61

GMR Sensor

3D3V_S5
3D3V_AUX_S5
R910 100KR2J-1-GP DY
R909 100KR2J-1-GP
R912 100KR2J-1-GP DY
R911 100KR2J-1-GP
LID_CL_SIO_TAB#
D902 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
GMR1 HGDEDM013A-GP
074.00013.00BJ
LID_CL_NB#
NON LID_WAKE
R913 D01R2J-L-GP
R914 D01R2J-L-GP
GMR_VDD_R
C902 SCD1U16V2KX-3DLGP
20180118 Change part number

IOBD1

USB2_USB30_RX_N
USB2_USB30_RX_P
USB2_USB30_TX_N
USB2_USB30_TX_P
CARD1_USB20_P
CARD1_USB20_N
USB2_USB20_N
USB2_USB20_P
FP1_USB20_N
FP1_USB20_P
20191205
FINGER PRINTER
LID_CL_SIO_TAB#
FPR_SCAN#
APU_SLP_S5#
KBC_PWRBTN#_R
LID_CL_NB#
RTC
+RTC_VCC
3D3V_S0
3D3V_S5
3D3V_AUX_S5
USB30_VCCC
34AWG
AUDIO
AUD_HP1_JACK_L1
AUD_SENSE
AUD_SLEEVE
AUD_SLEEVE
AUD_SLEEVE
AUD_RING
AUD_RING
AUD_RING
AUD_HP1_JACK_R1
AUD_AGND
STAR-CON40-8-GP
020.F0847.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040

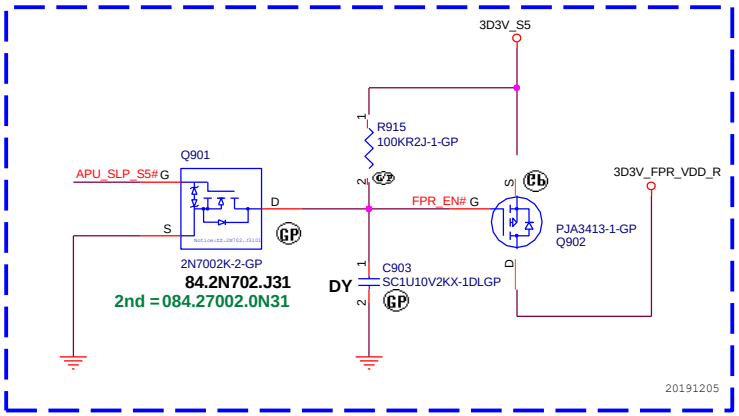
Hellcat14

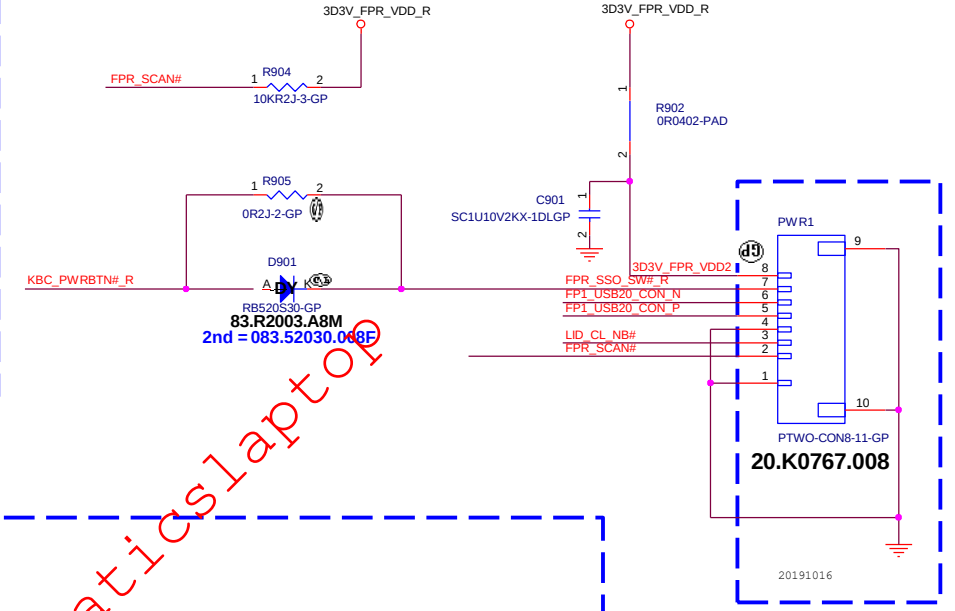
Wistron Corporation
21F, 88, Sec.1, HsinTaiiWu Rd., Hsiichiih, Taiipeiii-Hsiien221, Taiiwan, R.O.C.

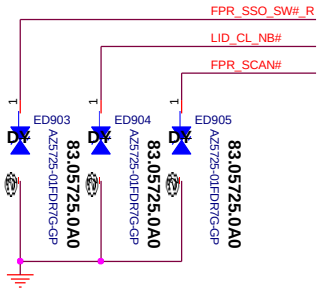
Title: IO Connector
Size: A3
Document Number: Hellcat MS 14 AMD
Rev: A00
Date: Friday, January 31, 2020
Sheet 8 of 10

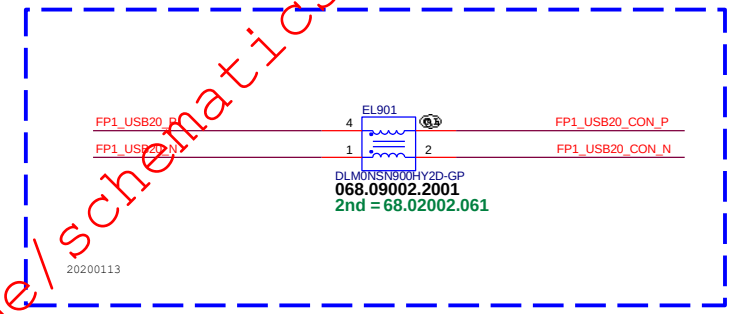
SSID = Finger Print

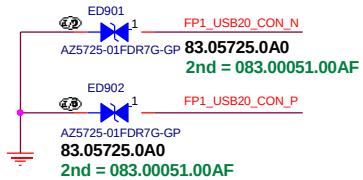
[8] FPR_SCAN#
[8] FP1_USB20_P
[8] FP1_USB20_N
[8] LID_CL_NB#
[8] KBC_PWRBTN#_R
[8] APU_SLP_S5#











teknisi indonesia

FP_8Pin_define

PIN 序号	PIN 名	说明
1	VBUS	AVDD(3.3V)
2	Power button	Power button signal
3	USB_DN	USB_N
4	USB_DP	USB_P
5	GND	系统地
6	LID closed	LID closed signal
7	GPIO_key	GPIO
8	ID(GND)	ID 检测脚

Hellllcat14

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, Taiipeiii-Hsiien221, Taiiwan, R.O.C.

Title: **Finger Print**

Size	Document Number	Rev
A3	Hellcat MS 14 AMD	A00

Date: Friday, January 31, 2020 Sheet 9 of 10

Change History

Version	Date	Page	Change Description

Hellcat 14

Wistron Corporation
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