MS-7A32 Ver:10

CPU:
AMD AM4

System Chipset:
Promontory X370/B350
(Performance gaming)

Main Memory:
DDR IV * 4 MAX:64 GB

VRM
RT8894A 4+2

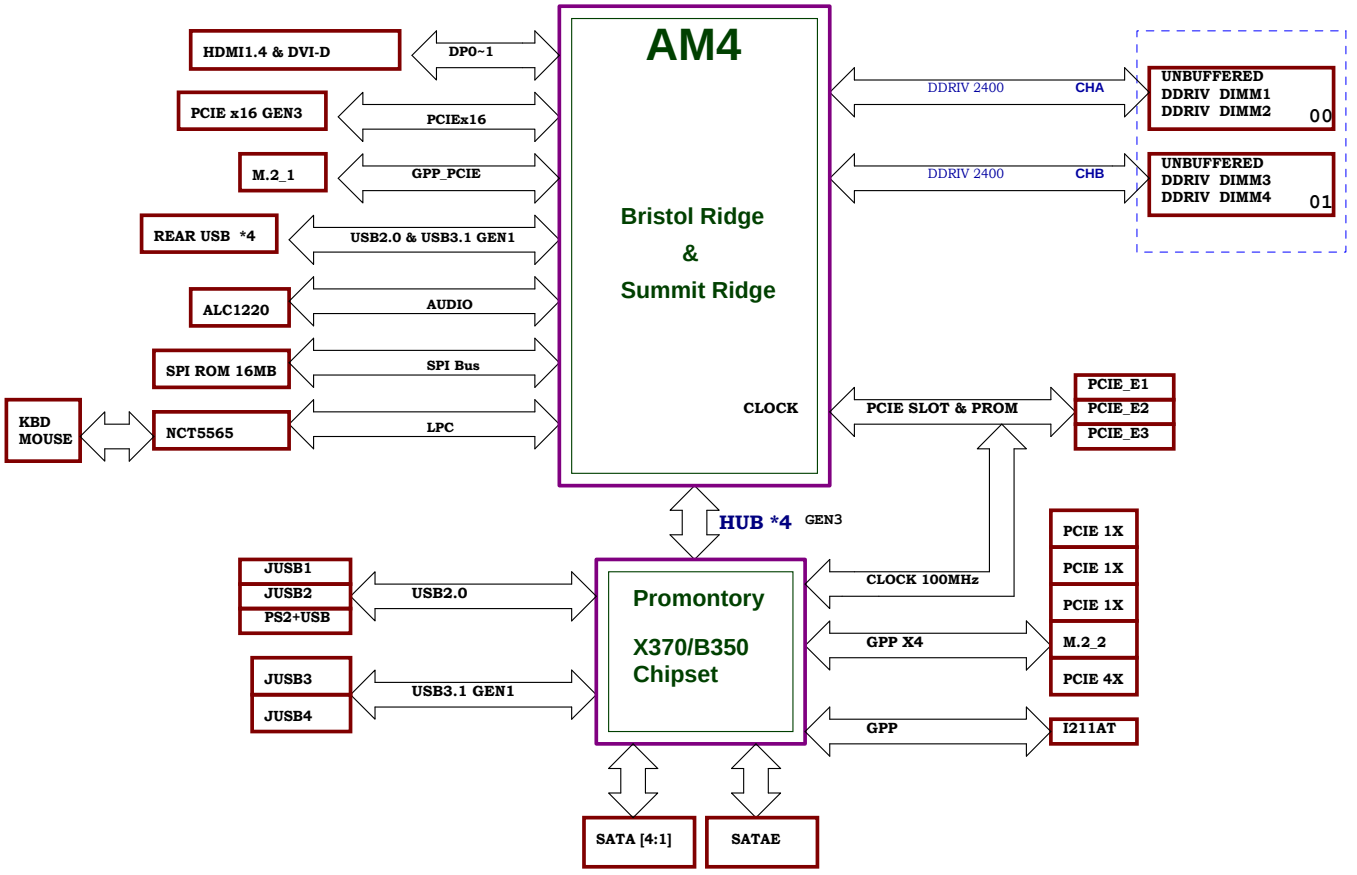
On Board Chipset:
LPC Super I/O --NCT6795D
LAN I211AT
Azalia CODEC - Realtek ALC1220
ASM2142 USB3.1 Gen2

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X8 Slot * 1

From FCH
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X4 Slot * 1

OCP IC:
UP6273

FUSION BLOCK DIAGRAM



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MS-7A32

Size	Document Description	Rev
Custom	Block Diagram	10

Date: Friday, January 20, 2017 | Sheet 1 of 65

AMD AM4

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MS-7A32

Size: Custom | Document Description: Cover Sheet | Rev: 10

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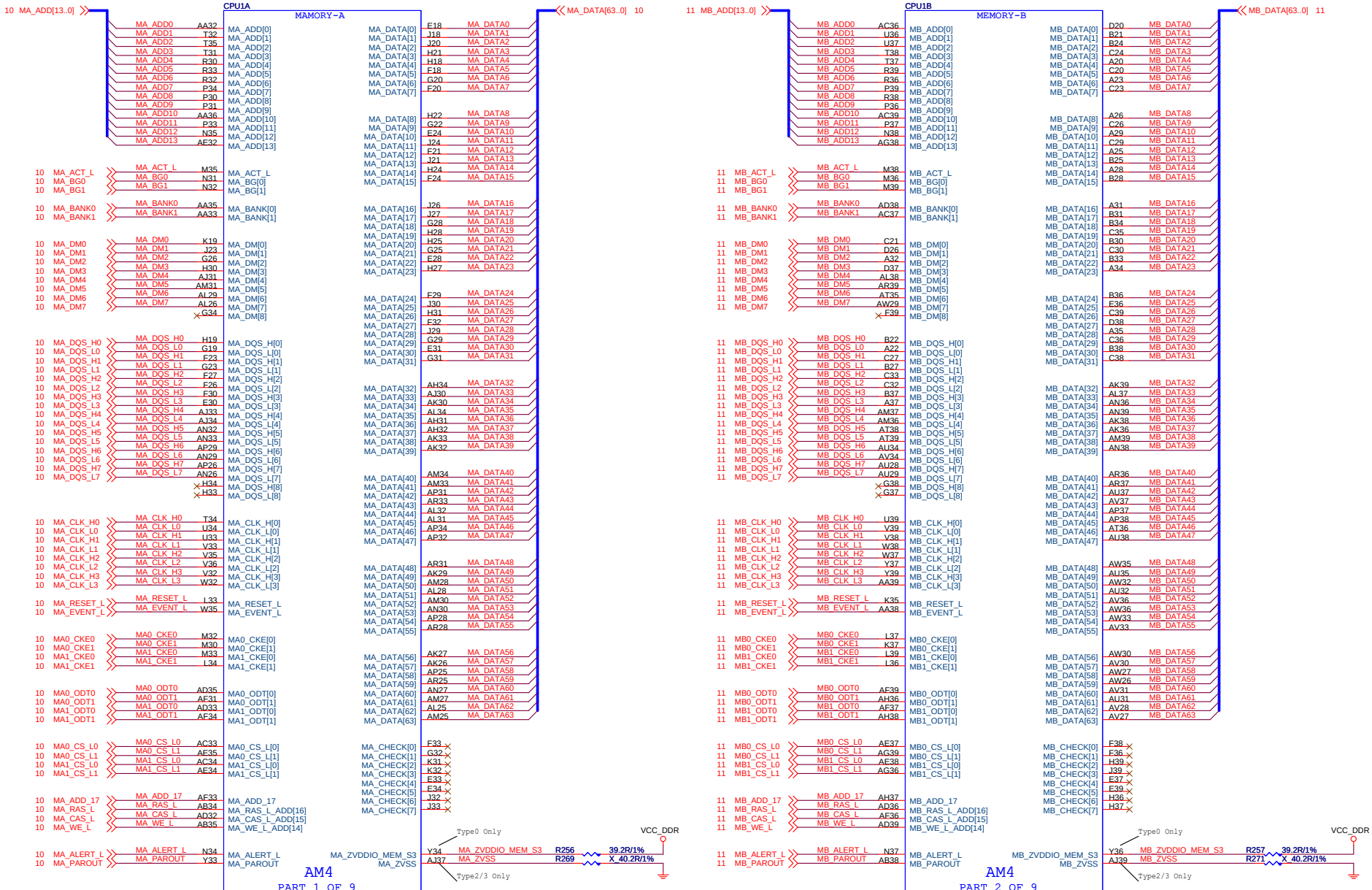
CPU1A
MAMORY-A
10 MA_ADD[13..0]
MA_ADD0 AA32
MA_ADD1 T32
MA_ADD2 T35
MA_ADD3 T31
MA_ADD4 R30
MA_ADD5 R33
MA_ADD6 R32
MA_ADD7 P34
MA_ADD8 P30
MA_ADD9 P31
MA_ADD10 AA36
MA_ADD11 P33
MA_ADD12 N35
MA_ADD13 AE32
MA_ACT_L M35
MA_BG0 N31
MA_BG1 N32
MA_BANK0 AA35
MA_BANK1 AA33
MA_DM0 K19
MA_DM1 J23
MA_DM2 G26
MA_DM3 H30
MA_DM4 AJ31
MA_DM5 AM31
MA_DM6 AL29
MA_DM7 AL26
G34
MA_DQS_H0 H19
MA_DQS_L0 G19
MA_DQS_H1 F23
MA_DQS_L1 G23
MA_DQS_H2 F27
MA_DQS_L2 F26
MA_DQS_H3 F30
MA_DQS_L3 E30
MA_DQS_H4 AJ33
MA_DQS_L4 AJ34
MA_DQS_H5 AN32
MA_DQS_L5 AN33
MA_DQS_H6 AP29
MA_DQS_L6 AN29
MA_DQS_H7 AP26
MA_DQS_L7 AN26
H34
H33
MA_CLK_H0 T34
MA_CLK_L0 U34
MA_CLK_H1 U33
MA_CLK_L1 V33
MA_CLK_H2 V35
MA_CLK_L2 V36
MA_CLK_H3 V32
MA_CLK_L3 W32
MA_RESET_L L33
MA_EVENT_L W35
MA0_CKE0 M32
MA0_CKE1 M30
MA1_CKE0 M33
MA1_CKE1 L34
MA0_ODT0 AD35
MA0_ODT1 AF31
MA1_ODT0 AD33
MA1_ODT1 AF34
MA0_CS_L0 AC33
MA0_CS_L1 AE35
MA1_CS_L0 AC34
MA1_CS_L1 AE34
MA_ADD_17 AF33
MA_RAS_L AB34
MA_CAS_L AD32
MA_WE_L AB35
MA_ALERT_L N34
MA_PAROUT Y33
MA_ADD[0]
MA_ADD[1]
MA_ADD[2]
MA_ADD[3]
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MA_RAS_L_ADD[16]
MA_CAS_L_ADD[15]
MA_WE_L_ADD[14]
MA_ALERT_L
MA_PAROUT
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MA_ZVDDIO_MEM_S3
MA_ZVSS
F18 MA_DATA0
J18 MA_DATA1
J20 MA_DATA2
H21 MA_DATA3
H18 MA_DATA4
F18 MA_DATA5
G20 MA_DATA6
F20 MA_DATA7
H22 MA_DATA8
G22 MA_DATA9
E24 MA_DATA10
J24 MA_DATA11
F21 MA_DATA12
J21 MA_DATA13
H24 MA_DATA14
F24 MA_DATA15
J26 MA_DATA16
J27 MA_DATA17
G28 MA_DATA18
H28 MA_DATA19
H25 MA_DATA20
G25 MA_DATA21
E28 MA_DATA22
H27 MA_DATA23
F29 MA_DATA24
J30 MA_DATA25
H31 MA_DATA26
F32 MA_DATA27
J29 MA_DATA28
G29 MA_DATA29
E31 MA_DATA30
G31 MA_DATA31
AH34 MA_DATA32
AJ30 MA_DATA33
AK30 MA_DATA34
AL34 MA_DATA35
AH31 MA_DATA36
AH32 MA_DATA37
AK33 MA_DATA38
AK32 MA_DATA39
AM34 MA_DATA40
AM33 MA_DATA41
AP31 MA_DATA42
AR33 MA_DATA43
AL32 MA_DATA44
AL31 MA_DATA45
AP34 MA_DATA46
AP32 MA_DATA47
AR31 MA_DATA48
AK29 MA_DATA49
AM28 MA_DATA50
AL28 MA_DATA51
AM30 MA_DATA52
AN30 MA_DATA53
AP28 MA_DATA54
AR28 MA_DATA55
AK27 MA_DATA56
AK26 MA_DATA57
AP25 MA_DATA58
AR25 MA_DATA59
AN27 MA_DATA60
AM27 MA_DATA61
AL25 MA_DATA62
AM25 MA_DATA63
F33
G32
K31
K32
E33
E34
J32
J33
Y34 MA_ZVDDIO_MEM_S3 R256 39.2R/1%
AJ37 MA_ZVSS R269 X_40.2R/1%
Type0 Only
Type2/3 Only
VCC_DDR
MA_DATA[63..0] 10
AM4
PART 1 OF 9
ZIF-SOCKET1331-HF
CPU1B
MEMORY-B
11 MB_ADD[13..0]
MB_ADD0 AC36
MB_ADD1 U36
MB_ADD2 U37
MB_ADD3 T38
MB_ADD4 T37
MB_ADD5 R39
MB_ADD6 R36
MB_ADD7 P39
MB_ADD8 R38
MB_ADD9 P36
MB_ADD10 AC39
MB_ADD11 P37
MB_ADD12 N38
MB_ADD13 AG38
MB_ACT_L M38
MB_BG0 M36
MB_BG1 M39
MB_BANK0 AD38
MB_BANK1 AC37
MB_DM0 C21
MB_DM1 D26
MB_DM2 A32
MB_DM3 D37
MB_DM4 AL38
MB_DM5 AR39
MB_DM6 AT35
MB_DM7 AW29
F39
MB_DQS_H0 B22
MB_DQS_L0 A22
MB_DQS_H1 C27
MB_DQS_L1 B27
MB_DQS_H2 C33
MB_DQS_L2 C32
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MB_DQS_L3 A37
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MB_DQS_L6 AV34
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MB_CHECK[7]
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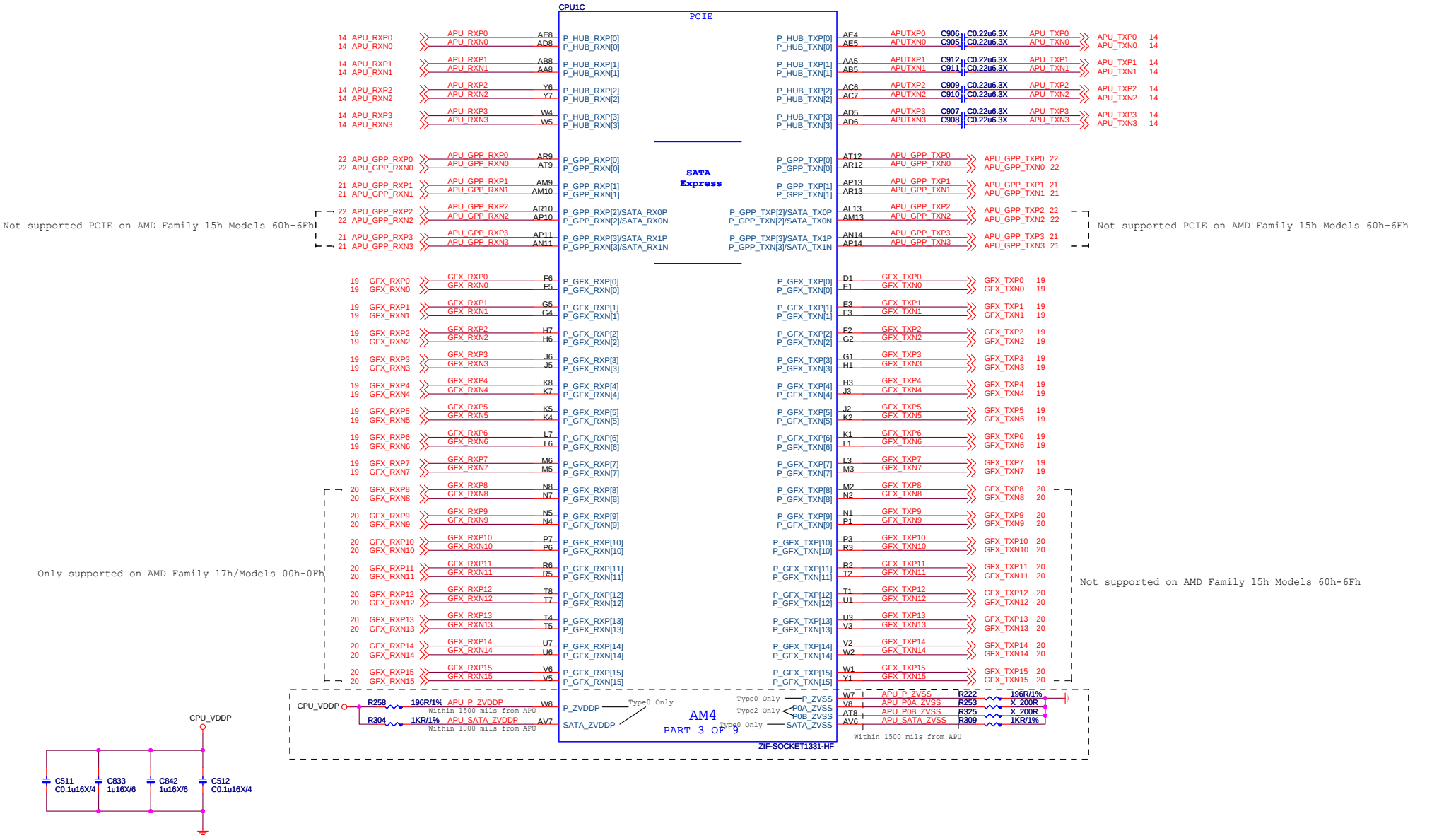
MB_ZVSS
D20 MB_DATA0
B21 MB_DATA1
B24 MB_DATA2
C24 MB_DATA3
A20 MB_DATA4
C20 MB_DATA5
A23 MB_DATA6
C23 MB_DATA7
A26 MB_DATA8
C26 MB_DATA9
A29 MB_DATA10
C29 MB_DATA11
A25 MB_DATA12
B25 MB_DATA13
A28 MB_DATA14
B28 MB_DATA15
A31 MB_DATA16
B31 MB_DATA17
B34 MB_DATA18
C35 MB_DATA19
B30 MB_DATA20
C30 MB_DATA21
B33 MB_DATA22
A34 MB_DATA23
B36 MB_DATA24
E36 MB_DATA25
C39 MB_DATA26
D38 MB_DATA27
A35 MB_DATA28
C36 MB_DATA29
B38 MB_DATA30
C38 MB_DATA31
AK39 MB_DATA32
AL37 MB_DATA33
AN36 MB_DATA34
AN39 MB_DATA35
AK38 MB_DATA36
AK36 MB_DATA37
AM39 MB_DATA38
AN38 MB_DATA39
AR36 MB_DATA40
AR37 MB_DATA41
AU37 MB_DATA42
AV37 MB_DATA43
AP37 MB_DATA44
AP38 MB_DATA45
AT36 MB_DATA46
AU38 MB_DATA47
AW35 MB_DATA48
AU35 MB_DATA49
AW32 MB_DATA50
AU32 MB_DATA51
AV36 MB_DATA52
AW36 MB_DATA53
AW33 MB_DATA54
AV33 MB_DATA55
AW30 MB_DATA56
AV30 MB_DATA57
AW27 MB_DATA58
AW26 MB_DATA59
AV31 MB_DATA60
AU31 MB_DATA61
AV28 MB_DATA62
AV27 MB_DATA63
F38
F36
H39
J39
E37
E39
H36
H37
Y36 MB_ZVDDIO_MEM_S3 R257 39.2R/1%
AJ39 MB_ZVSS R271 X_40.2R/1%
Type0 Only
Type2/3 Only
VCC_DDR
MB_DATA[63..0] 11
AM4
PART 2 OF 9
ZIF-SOCKET1331-HF
MICRO-STAR INT'L CO.,LTD
MS-7A32
Size
Custom
Document Description
AM4 DDR4 I/F
Rev
10
Date: Tuesday, January 24, 2017
Sheet 3 of 65



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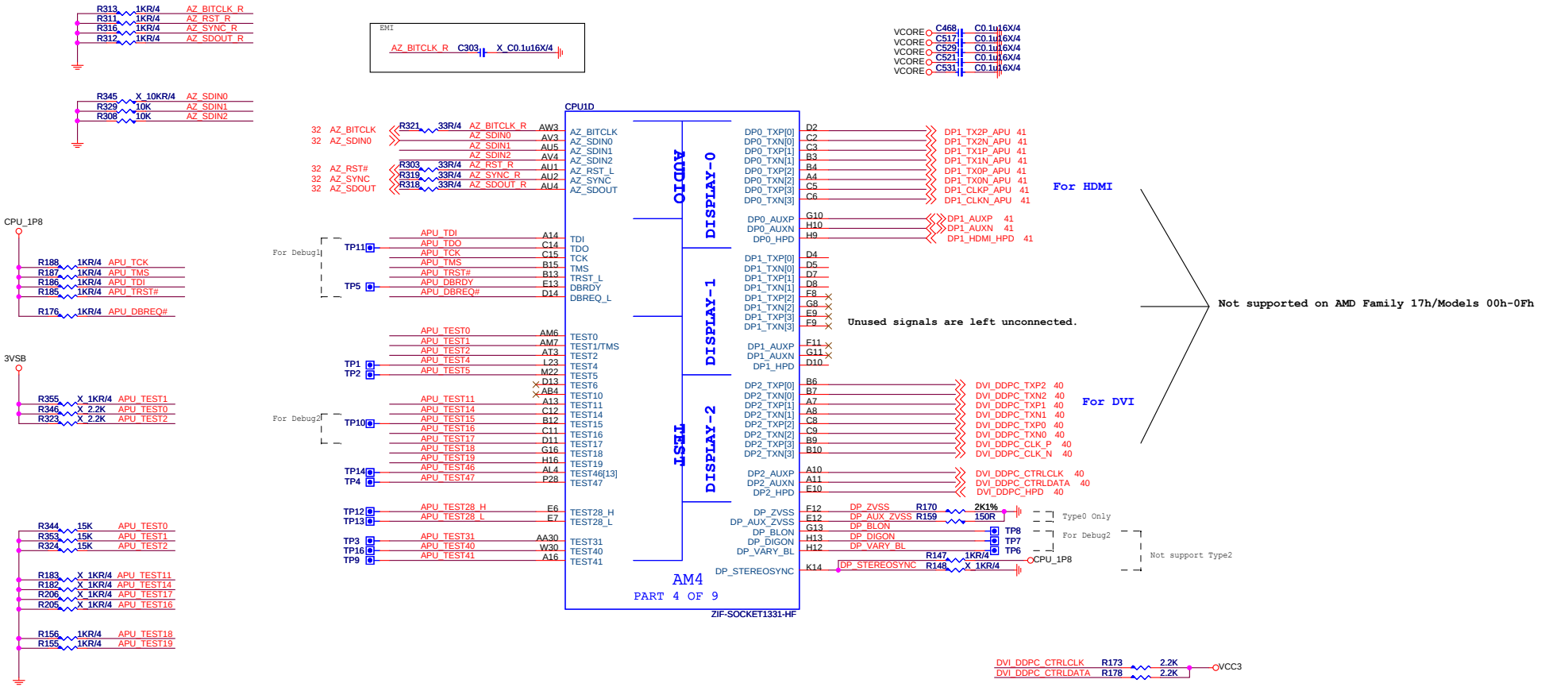
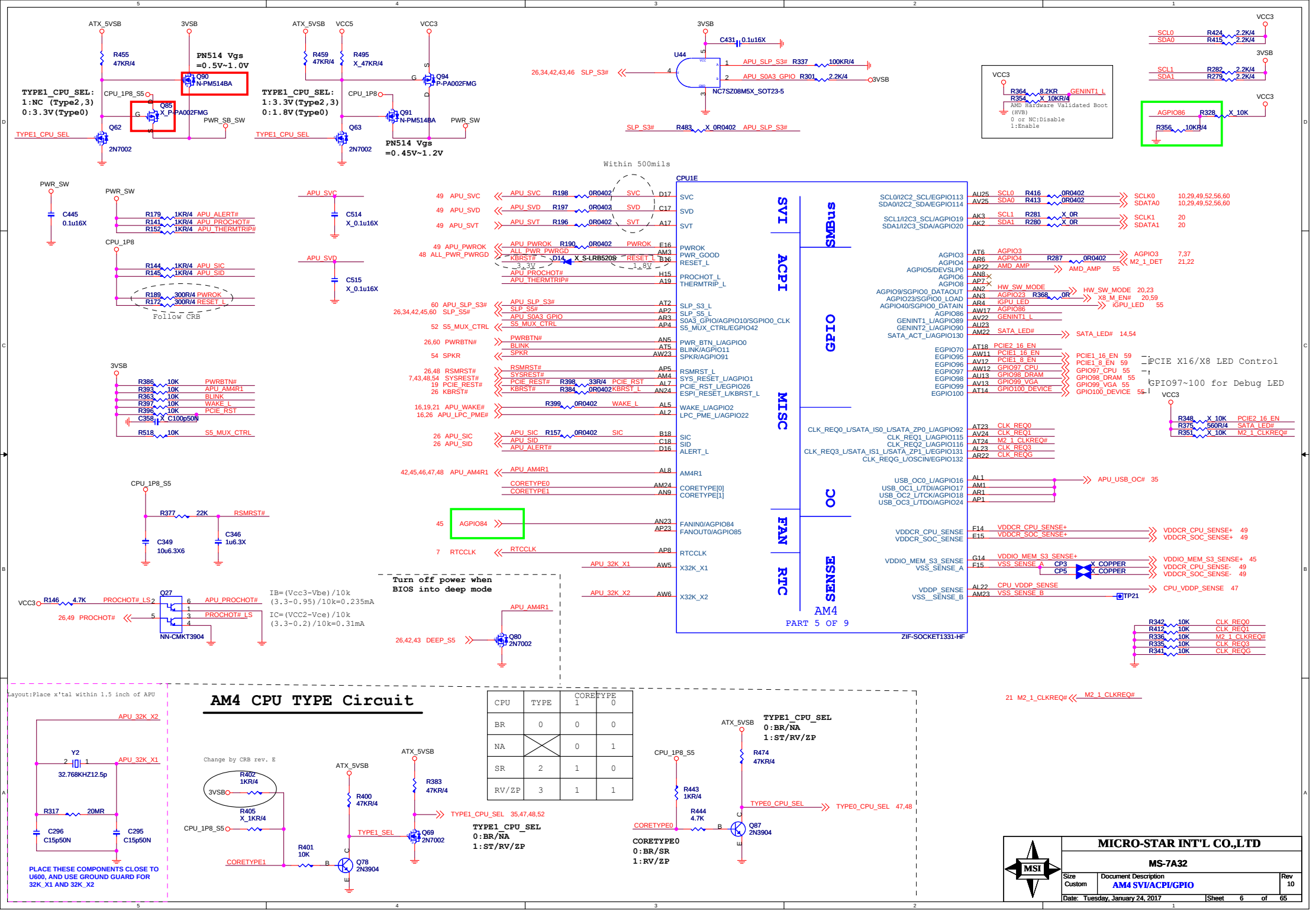
Rev: 10	
Date: Tuesday, January 24, 2017	Sheet 4 of 65



MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: AM4 Display/Audio	Rev: 10
Date: Tuesday, January 24, 2017	Sheet 5 of 65	


ATX_5VSB
3VSB
R455 47KR/4
PN514 Vgs =0.5V~1.0V
Q90 N-PM514BA
TYPE1_CPU_SEL: 1:NC (Type2,3) 0:3.3V(Type0)
CPU_1P8_S5
Q85 X_P-PA002FMG
PWR_SB_SW
Q62
TYPE1_CPU_SEL
2N7002
VCC5
VCC3
R459 47KR/4
R495 X_47KR/4
Q94 P-PA002FMG
CPU_1P8
Q91 N-PM514BA
PWR_SW
TYPE1_CPU_SEL: 1:3.3V(Type2,3) 0:1.8V(Type0)
Q63
2N7002
PN514 Vgs =0.45V~1.2V
C431 0.1u16X
U44
NC7SZ08M5X_SOT23-5
APU_SLP_S3# R337 100KR/4
APU_S0A3_GPIO R301 2.2K/4
26,34,42,43,46 SLP_S3#
SLP_S3# R483 X_0R0402 APU_SLP_S3#
SCL0 R424 2.2K/4
SDA0 R415 2.2K/4
SCL1 R282 2.2K/4
SDA1 R279 2.2K/4
R364 8.2KR GENINT1_L
R354 X_10KR/4
AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable
AGPIO86 R328 X_10K
R356 10KR/4
PWR_SW
C445 0.1u16X
R179 1KR/4 APU_ALERT#
R141 1KR/4 APU_PROCHOT#
R152 1KR/4 APU_THERMTRIP#
CPU_1P8
R144 1KR/4 APU_SIC
R145 1KR/4 APU_SID
R189 300R/4 PWROK
R172 300R/4 RESET_L
Follow CRB
APU_SVC
C514 X_0.1u16X
APU_SVD
C515 X_0.1u16X
Within 500mils
CPU1E
SVC
SVD
SVT
PWROK
PWR_GOOD
RESET_L
PROCHOT_L
THERMTRIP_L
SLP_S3_L
SLP_S5_L
S0A3_GPIO/AGPIO10/SGPIO0_CLK
S5_MUX_CTRL/EGPIO42
PWR_BTN_L/AGPIO0
BLINK/AGPIO11
SPKR/AGPIO91
RSMRST_L
SYS_RESET_L/AGPIO1
PCIE_RST_L/EGPIO26
ESPI_RESET_L/KBRST_L
WAKE_L/AGPIO2
LPC_PME_L/AGPIO22
SIC
SID
ALERT_L
AM4R1
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CORETYPE[1]
FANIN0/AGPIO84
FANOUT0/AGPIO85
RTCCLK
X32K_X1
X32K_X2
SVI
ACPI
MISC
OC
FAN
RTC
SMBus
GPIO
SENSE
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQG_L/OSCIN/EGPIO132
USB_OC0_L/AGPIO16
USB_OC1_L/TDI/AGPIO17
USB_OC2_L/TCK/AGPIO18
USB_OC3_L/TDO/AGPIO24
VDDCR_CPU_SENSE
VDDCR_SOC_SENSE
VDDIO_MEM_S3_SENSE
VSS_SENSE_A
VDDP_SENSE
VSS_SENSE_B
AM4
PART 5 OF 9
ZIF-SOCKET1331-HF
SCL0/I2C2_SCL/EGPIO113
SDA0/I2C2_SDA/EGPIO114
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20
AGPIO3
AGPIO4
AGPIO5/DEVSLP0
AGPIO6
AGPIO8
AGPIO9/SGPIO0_DATAOUT
AGPIO23/SGPIO0_LOAD
AGPIO40/SGPIO0_DATAIN
AGPIO86
GENINT1_L/AGPIO89
GENINT2_L/AGPIO90
SATA_ACT_L/AGPIO130
EGPIO70
EGPIO95
EGPIO96
EGPIO97
EGPIO98
EGPIO99
EGPIO100
PCIE X16/X8 LED Control
GPIO97~100 for Debug LED
R348 X_10K PCIE2_16_EN
R375 560R/4 SATA_LED#
R351 X_10K M2_1_CLKREQ#
R342 10K CLK_REQ0
R412 10K CLK_REQ1
R336 10K M2_1_CLKREQ#
R335 10K CLK_REQ3
R341 10K CLK_REQG
21 M2_1_CLKREQ#
M2_1_CLKREQ#
3VSB
R386 10K PWRBTN#
R393 10K APU_AM4R1
R363 10K BLINK
R397 10K WAKE_L
R396 10K PCIE_RST
C358 X_C100p50N
R518 10K S5_MUX_CTRL
CPU_1P8_S5
R377 22K RSMRST#
C349 10u6.3X6
C346 1u6.3X
VCC3
R146 4.7K PROCHOT_LS
Q27
APU_PROCHOT#
26,49 PROCHOT#
PROCHOT# LS
NN-CMKT3904
IB=(Vcc3-Vbe)/10k (3.3-0.95)/10k=0.235mA
IC=(VCC2-Vce)/10k (3.3-0.2)/10k=0.31mA
Turn off power when BIOS into deep mode
APU_AM4R1
26,42,43 DEEP_S5
Q80 2N7002
45 AGPIO84
7 RTCCLK
APU_32K_X1
APU_32K_X2
APU_SVC R198 0R0402 SVC
APU_SVD R197 0R0402 SVD
APU_SVT R196 0R0402 SVT
APU_PWROK R190 0R0402 PWROK
ALL_PWR_PWRGD
KBRST# D14 X_S-LRB5208 RESET_L
3.3V
1.8V
APU_PROCHOT#
APU_THERMTRIP#
APU_SLP_S3#
SLP_S5#
APU_S0A3_GPIO
S5_MUX_CTRL
PWRBTN#
BLINK
SPKR
RSMRST#
SYSRESET#
PCIE_RST# R398 33R/4 PCIE_RST
KBRST# R384 0R0402 KBRST_L
R399 0R0402 WAKE_L
APU_SIC R157 0R0402 SIC
APU_SID
APU_ALERT#
APU_AM4R1
CORETYPE0
CORETYPE1
SCLK0 10,29,49,52,56,60
SDATA0 10,29,49,52,56,60
SCLK1 20
SDATA1 20
AGPIO3 7,37
M2_1_DET 21,22
AMD_AMP 55
HW_SW_MODE 20,23
X8_M_EN# 20,59
iGPU_LED 55
SATA_LED# 14,54
PCIE1_16_EN 59
PCIE1_8_EN 59
GPIO97_CPU 55
GPIO98_DRAM 55
GPIO99_VGA 55
GPIO100_DEVICE 55
CLK_REQ0
CLK_REQ1
M2_1_CLKREQ#
CLK_REQ3
CLK_REQG
APU_USB_OC# 35
VDDCR_CPU_SENSE+ 49
VDDCR_SOC_SENSE+ 49
VDDIO_MEM_S3_SENSE+ 45
VDDCR_CPU_SENSE- 49
VDDCR_SOC_SENSE- 49
CPU_VDDP_SENSE 47
TP21
Layout:Place x'tal within 1.5 inch of APU
Y2
32.768KHZ12.5p
R317 20MR
C296 C15p50N
C295 C15p50N
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
AM4 CPU TYPE Circuit
Change by CRB rev. E
R402 1KR/4
R405 X_1KR/4
R400 47KR/4
R383 47KR/4
TYPE1_SEL
Q69 2N7002
TYPE1_CPU_SEL 35,47,48,52
R401 10K
Q78 2N3904
CORETYPE1
TYPE1_CPU_SEL 0:BR/NA 1:ST/RV/ZP
CPU TYPE TYPE CORETYPE 1 0
BR 0 0 0
NA X 0 1
SR 2 1 0
RV/ZP 3 1 1
R474 47KR/4
R443 1KR/4
R444 4.7K
Q87 2N3904
TYPE0_CPU_SEL
TYPE0_CPU_SEL 47,48
CORETYPE0
CORETYPE0 0:BR/SR 1:RV/ZP
MICRO-STAR INT'L CO.,LTD
MS-7A32
Size Custom
Document Description AM4 SVI/ACPI/GPIO
Rev 10
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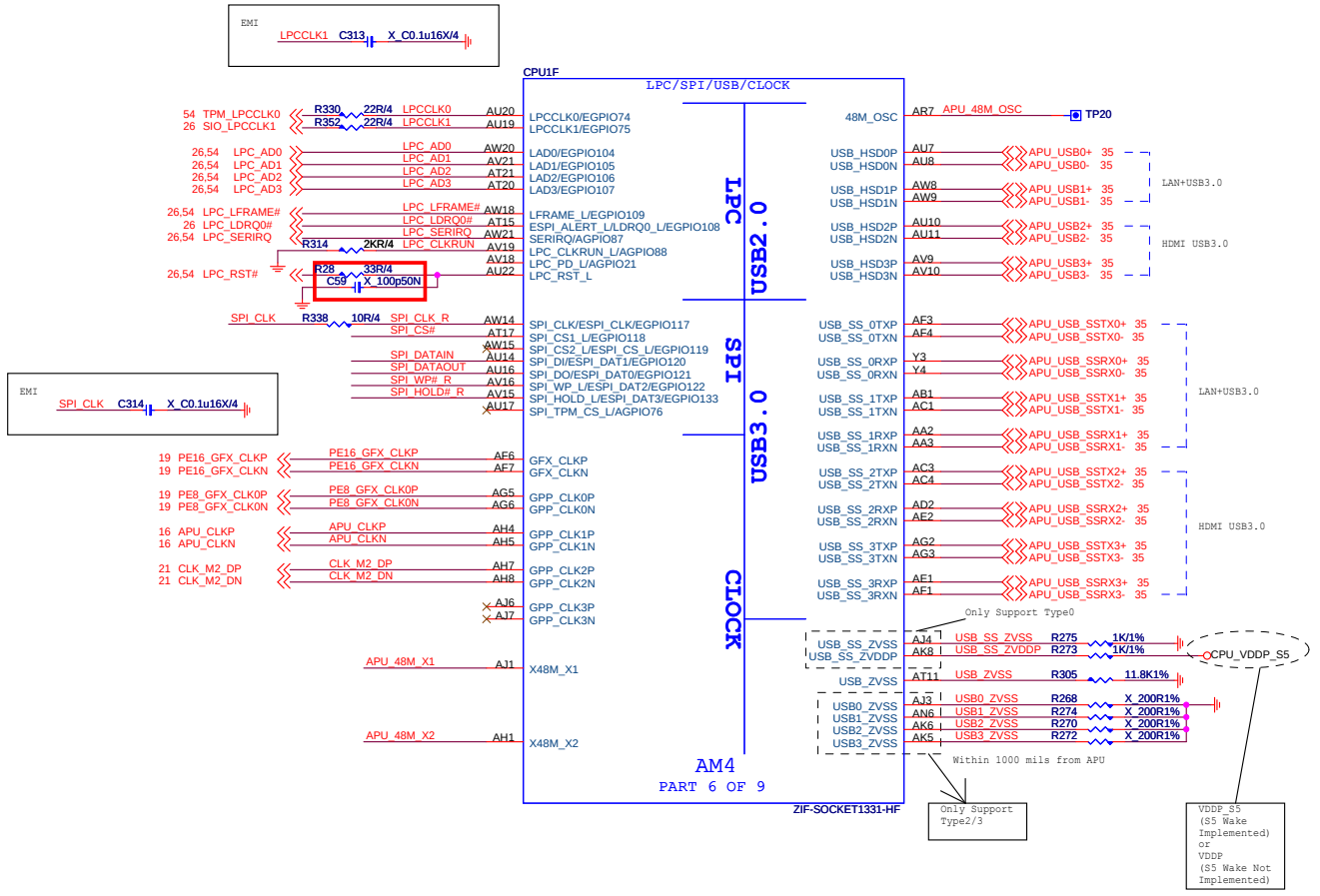
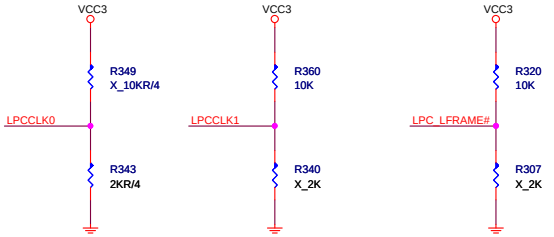
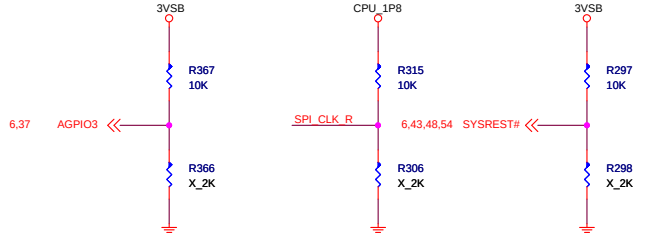
Sheet 6 of 65



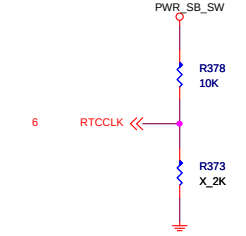
Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM

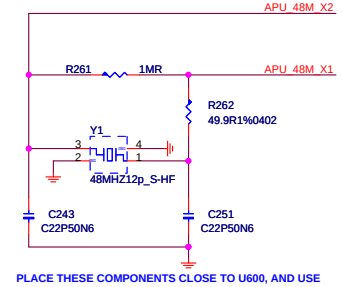


	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



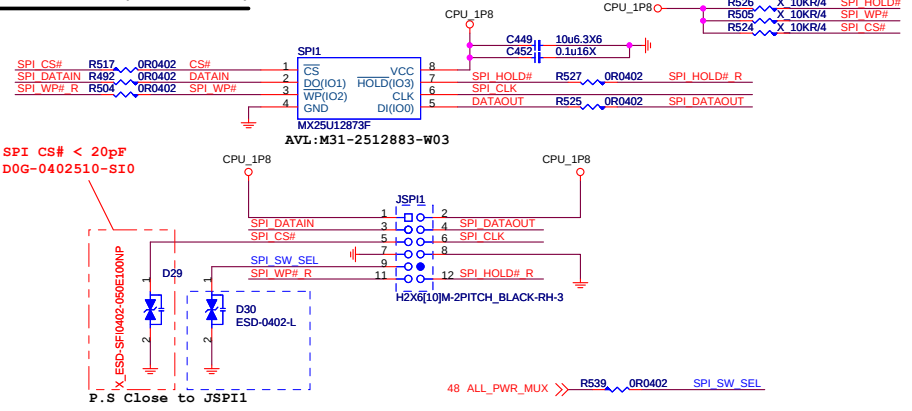
	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

Layout:Place x'tal within 1.5 inch of APU

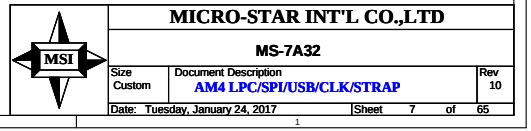


PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

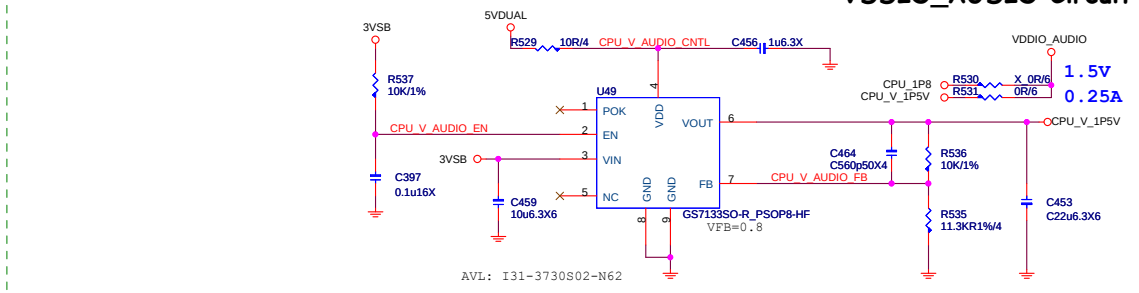
SPI ROM(1.8V)

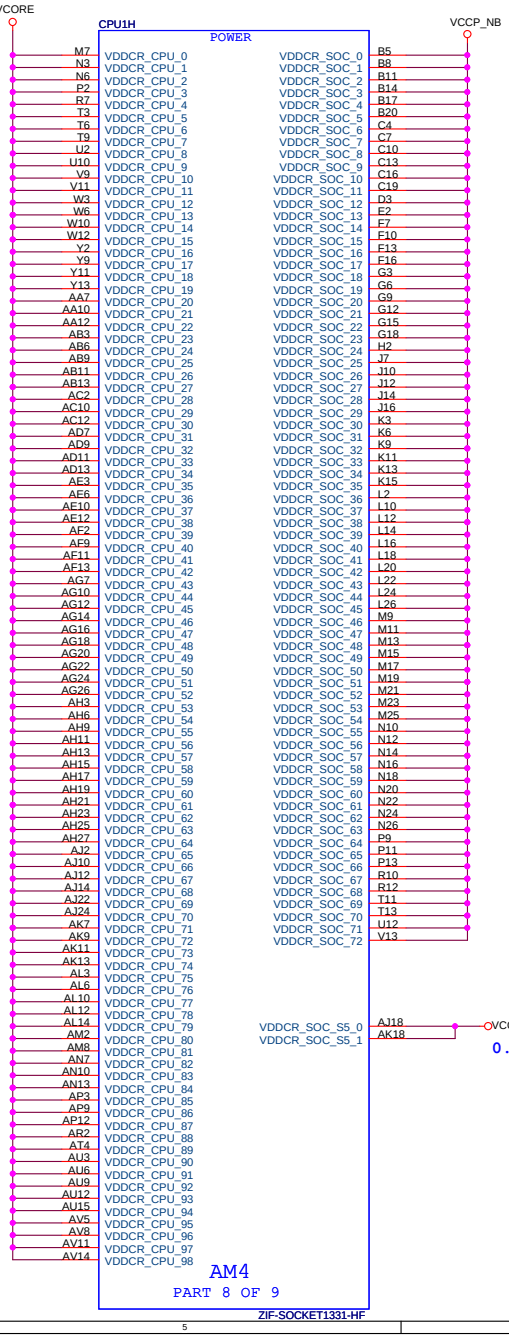


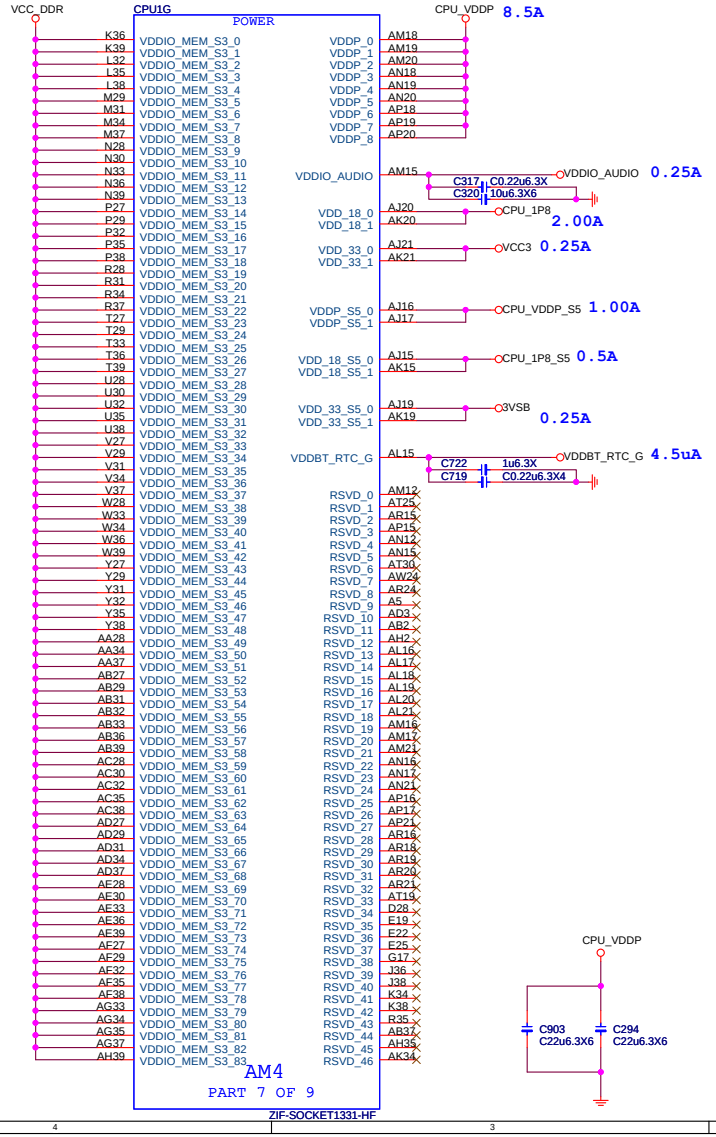
P.S Close to JSPI1



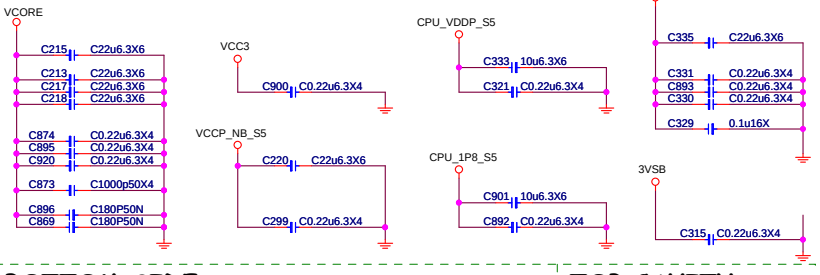
VDDIO_AUDIO Circuit



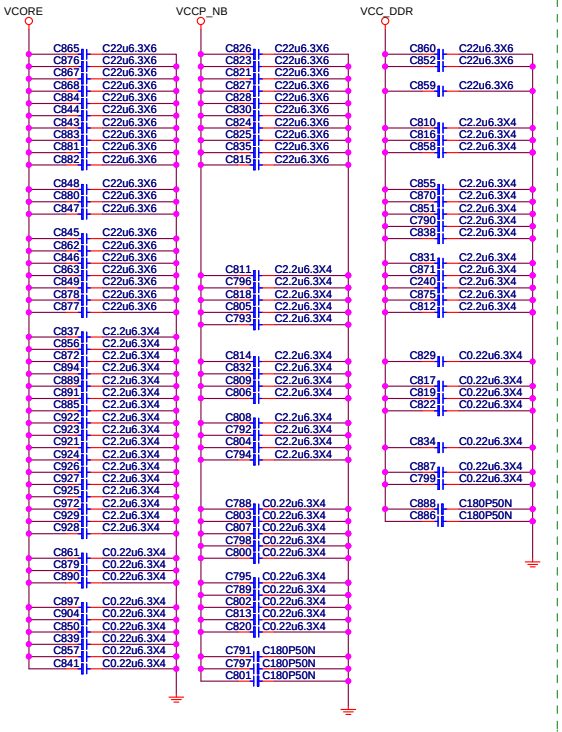




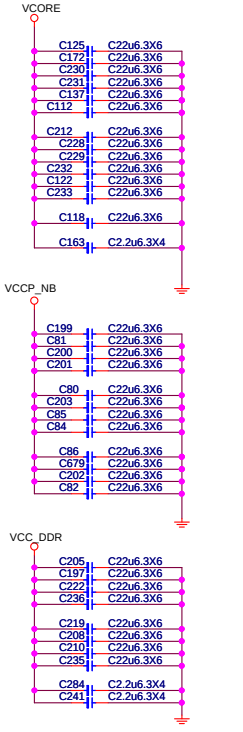
TOP SIDE



BOTTOM SIDE



TOP CAVITY



MICRO-STAR INT'L CO.,LTD

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Custom	AM4 Power/RTC Power	10

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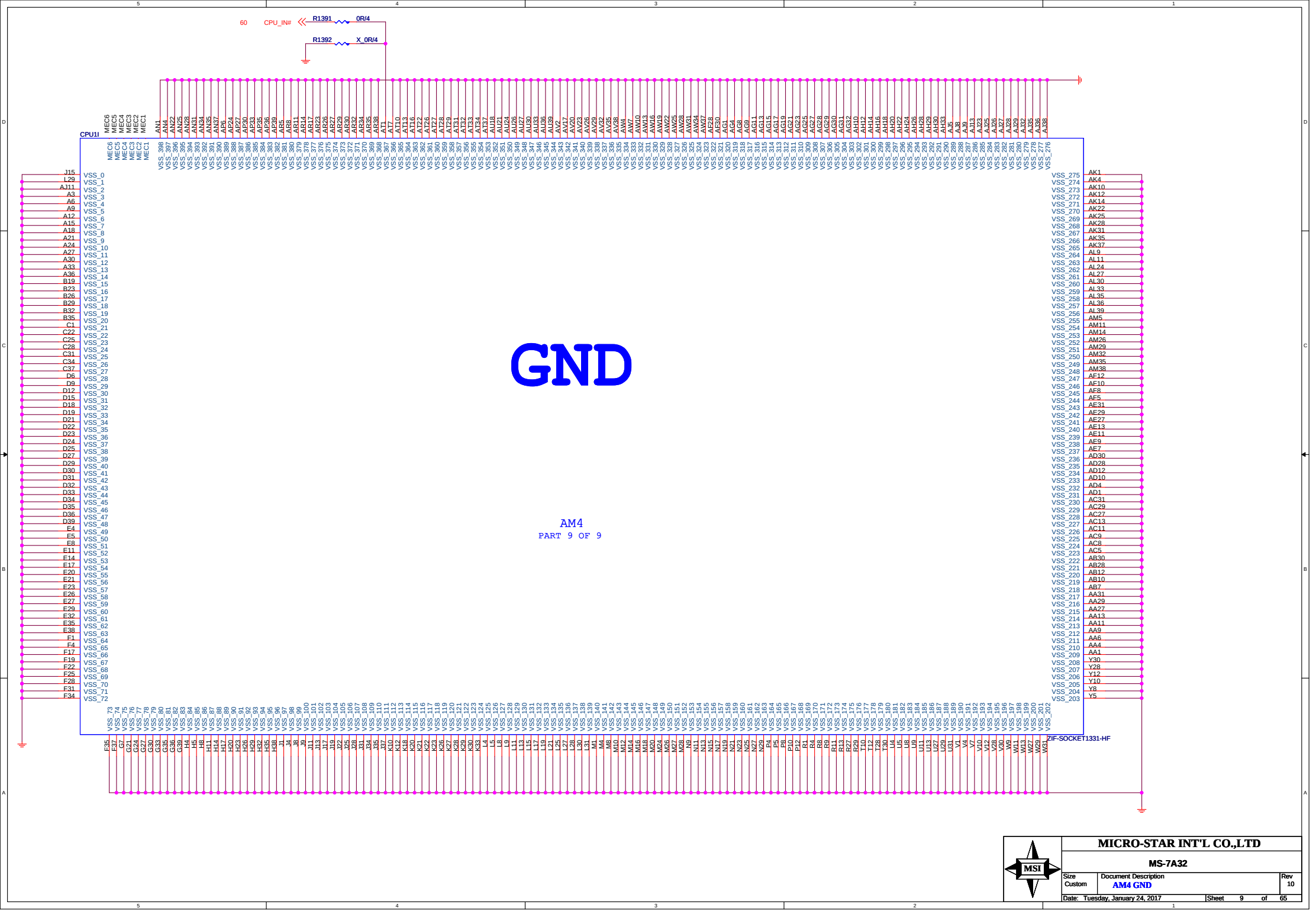

MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: AM4 GND
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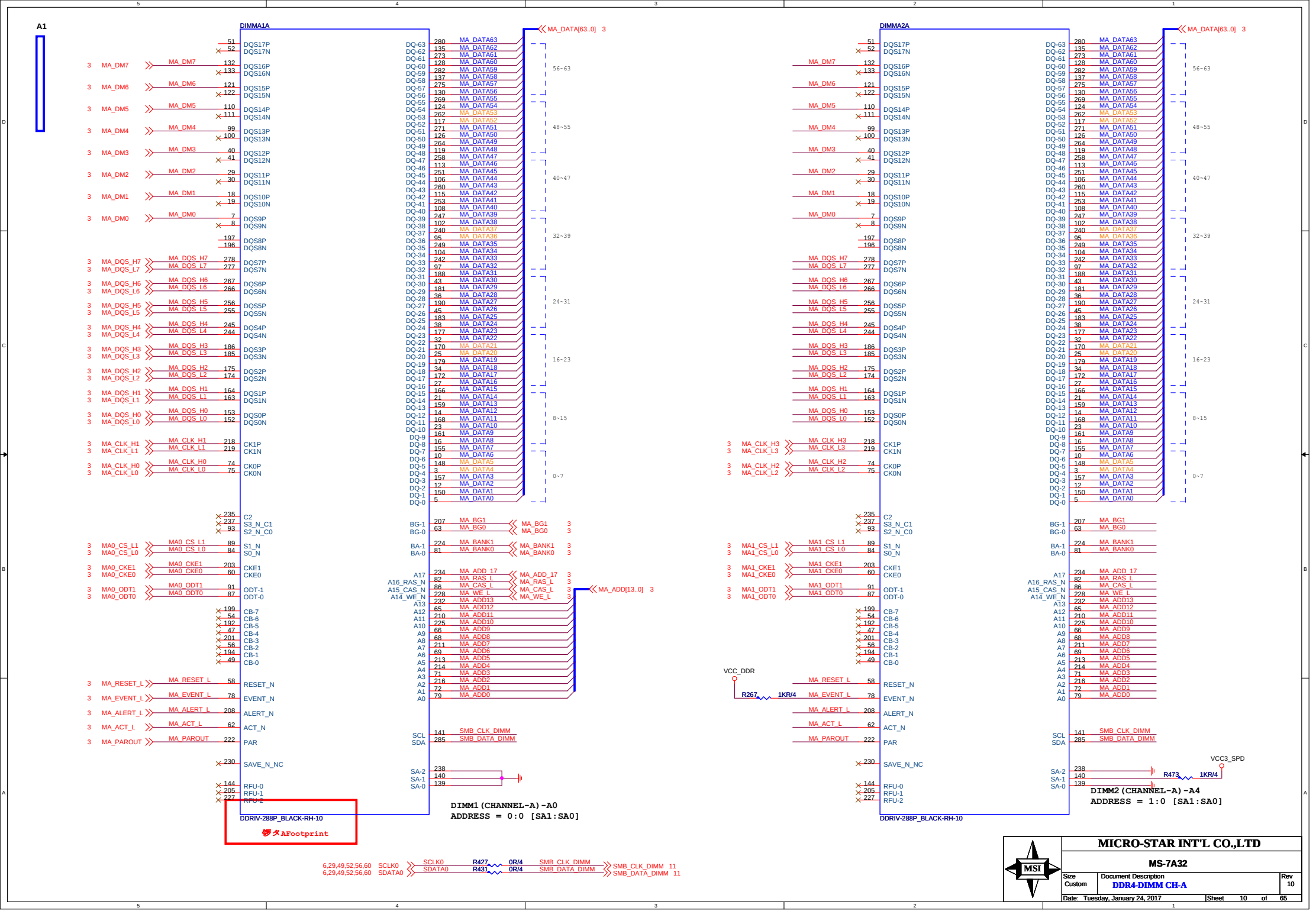
A1
DIMMA1A
DIMMA2A
MA_DATA[63..0] 3
MA_ADD[13..0] 3
DDRIV-288P_BLACK-RH-10
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
DIMM2(CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]
VCC_DDR
R267 1KR/4
VCC3_SPD
R473 1KR/4
AFootprint
SCLK0
SDATA0
R427 0R/4
R431 0R/4
SMB_CLK_DIMM
SMB_DATA_DIMM
MICRO-STAR INT'L CO.,LTD
MS-7A32
Size Custom
Document Description DDR4-DIMM CH-A
Rev 10
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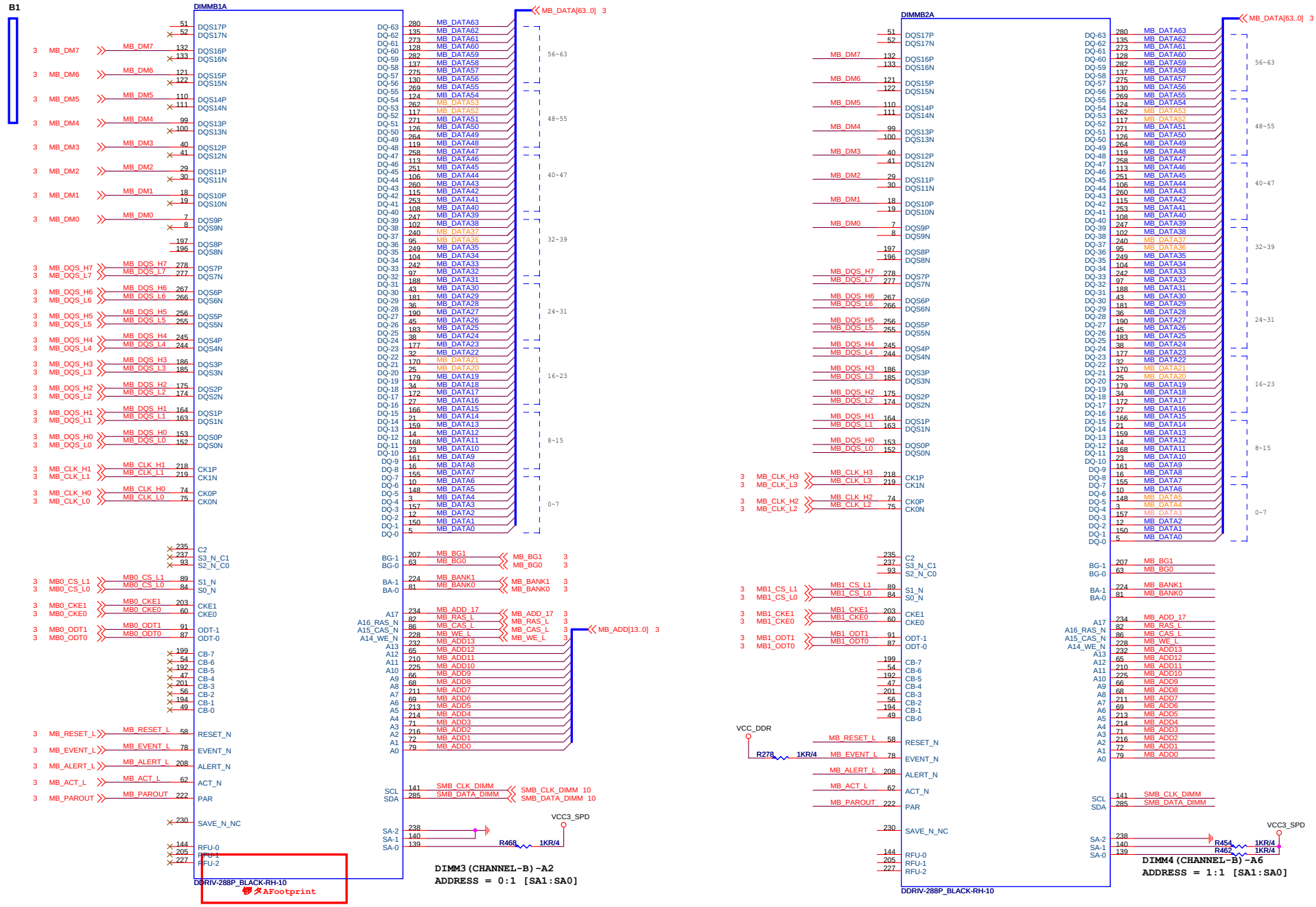
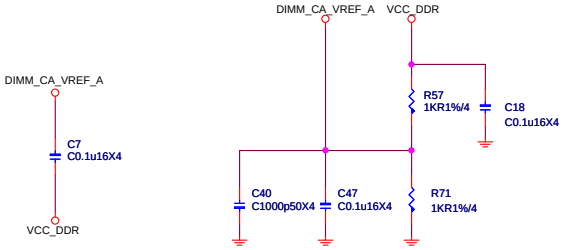


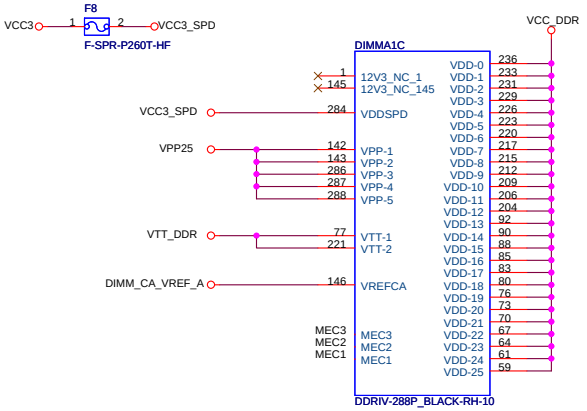
MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: DDR4-DIMM CH-B
Rev: 10	
Date: Tuesday, January 24, 2017	Sheet 11 of 65

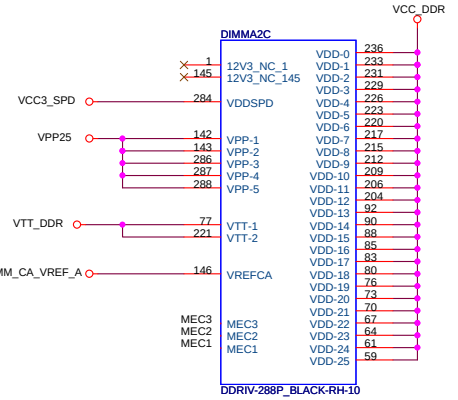
DDR VREF

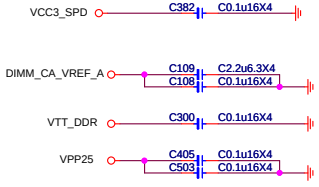
(place resistors close to DIMMs)

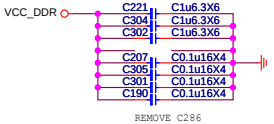


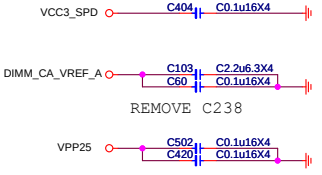
DIMM SLOT PN BY SPEC

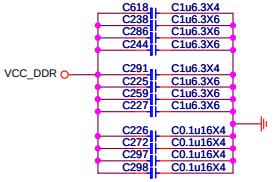


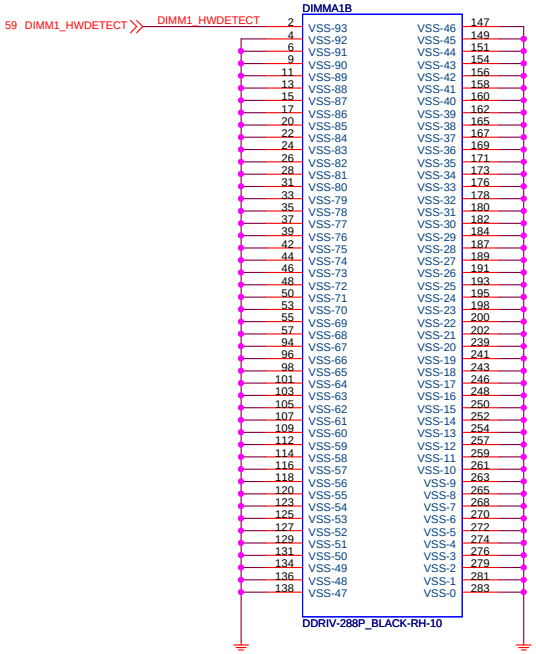


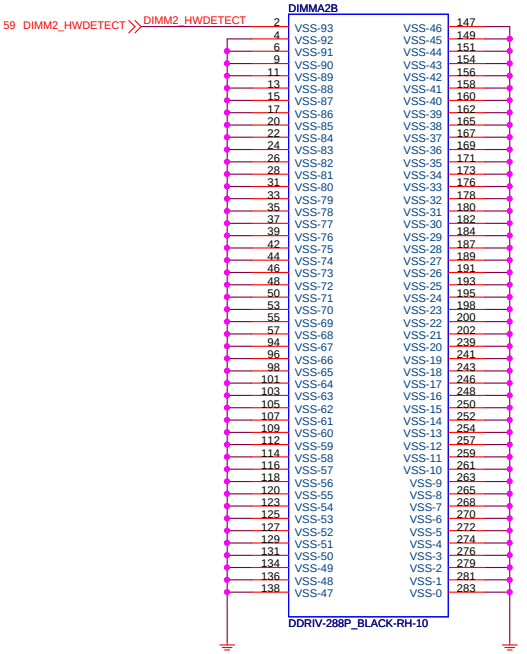








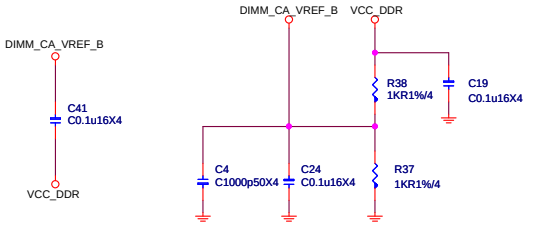


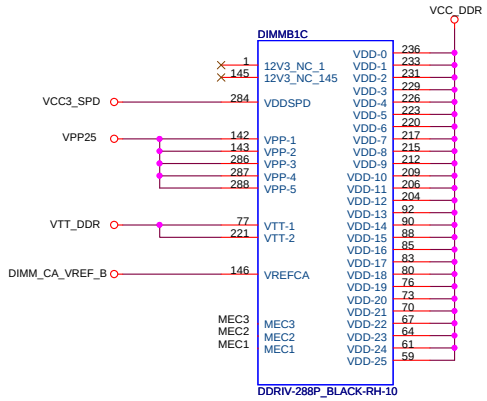


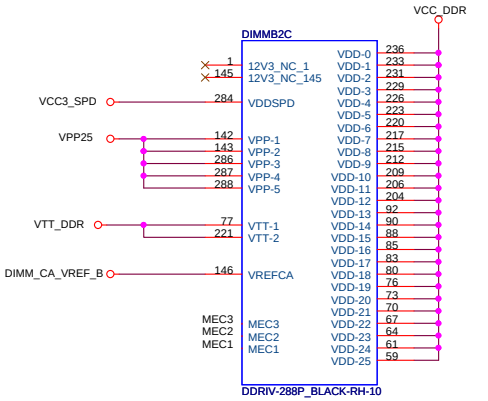
MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 10
Date: Tuesday, January 24, 2017	Sheet 12 of 65	

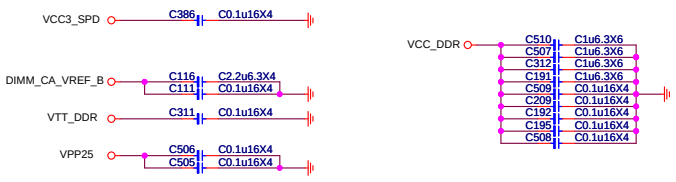
DDR VREF

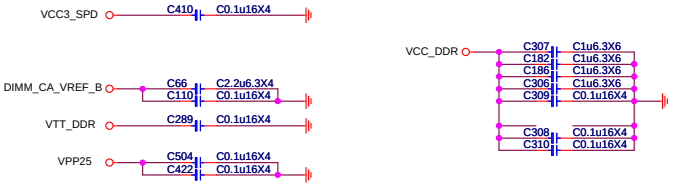
(place resistors close to DIMMs)

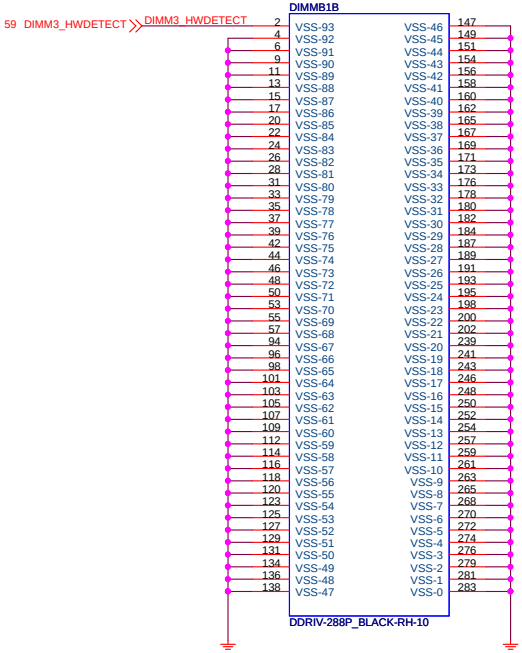


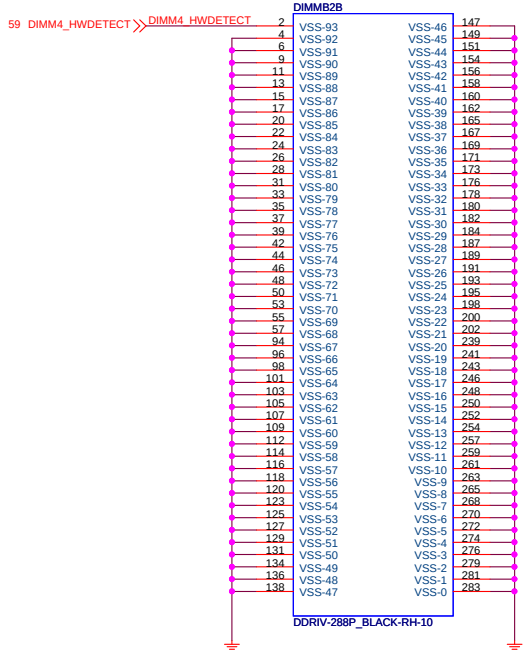












MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	10

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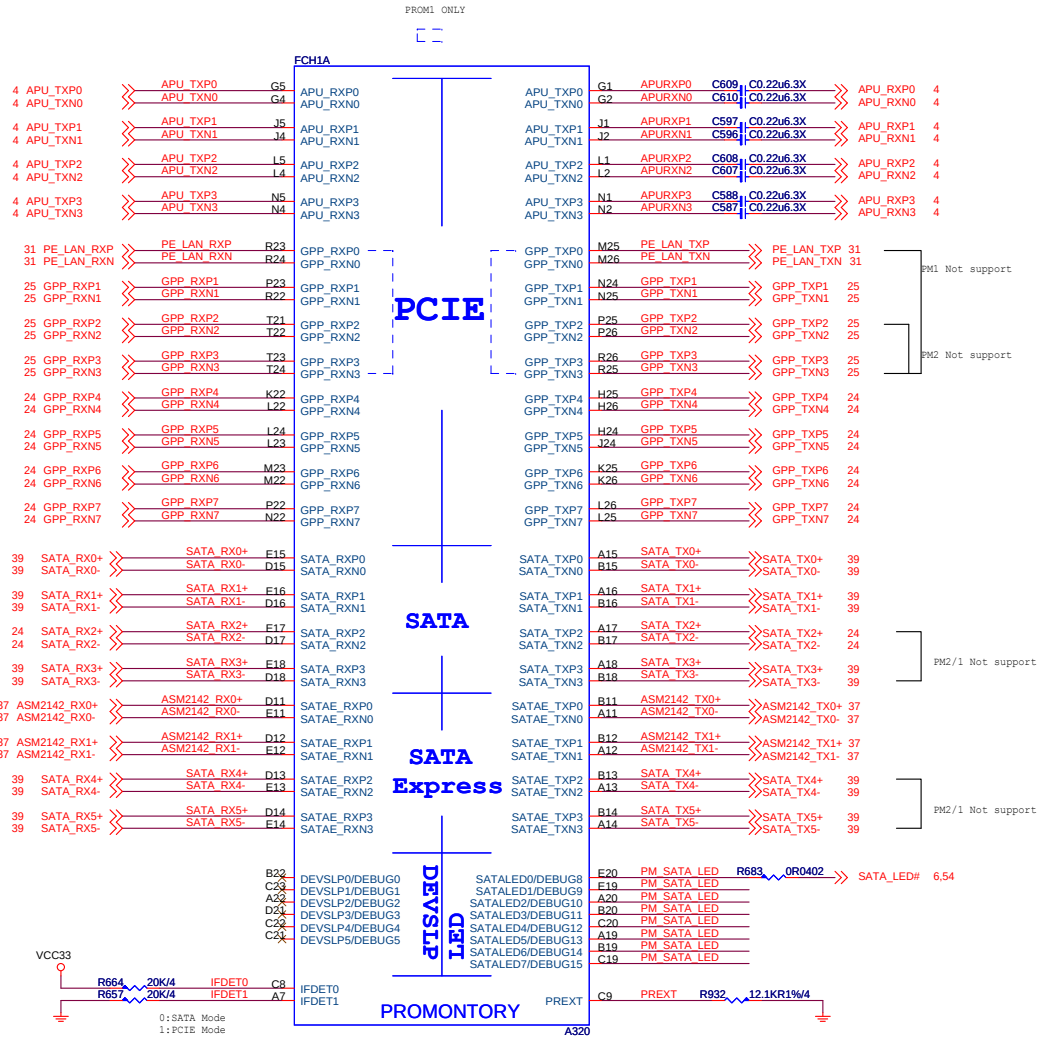
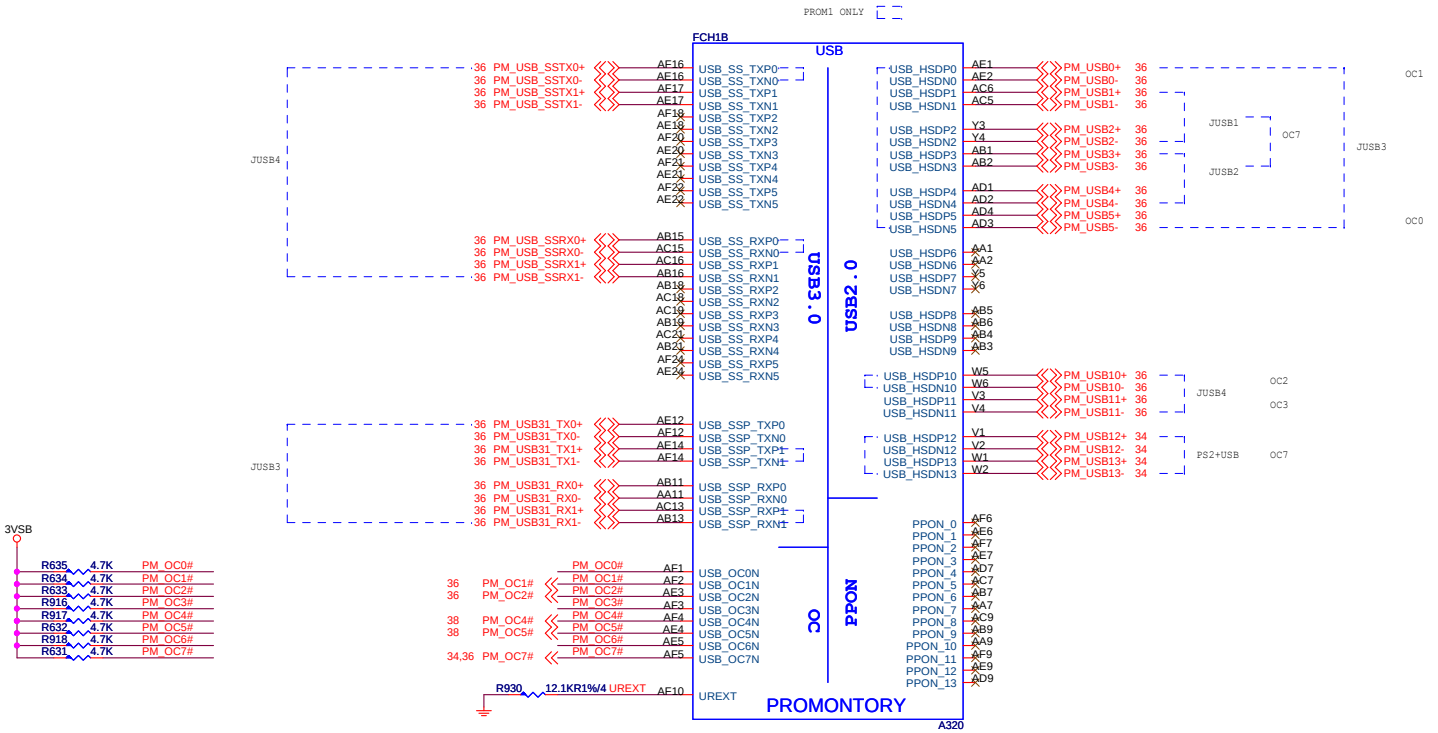


MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: Promontory-PCIE/SATA/SATAE
Rev: 10	
Date: Tuesday, January 24, 2017	Sheet 14 of 65



MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: Promontory-USB/OC	Rev: 10
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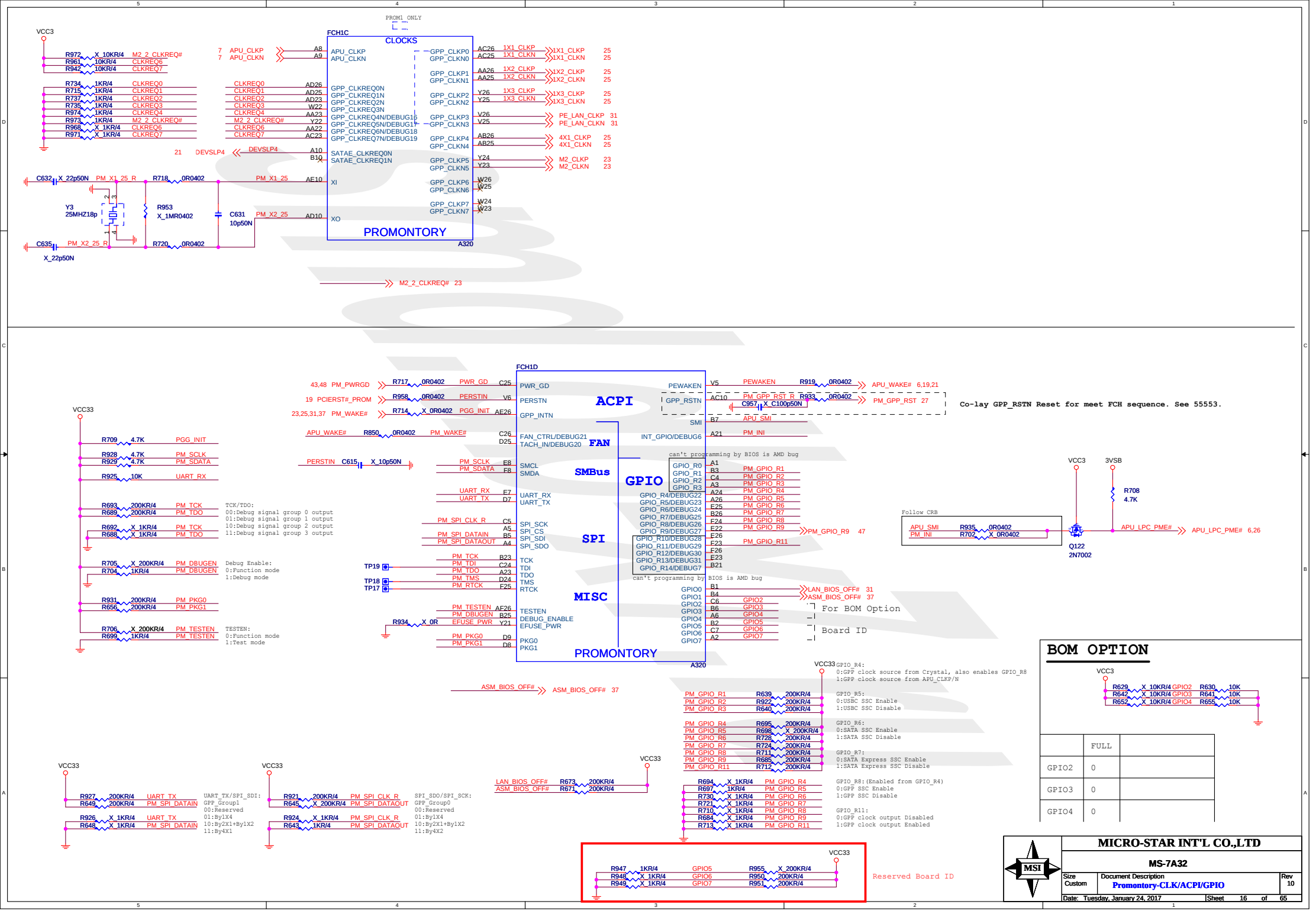
FCH1C
CLOCKS
PROMONTORY
A320
FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
PROMONTORY
A320
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
BOM OPTION
MICRO-STAR INT'L CO.,LTD
MS-7A32
Promontory-CLK/ACPI/GPIO
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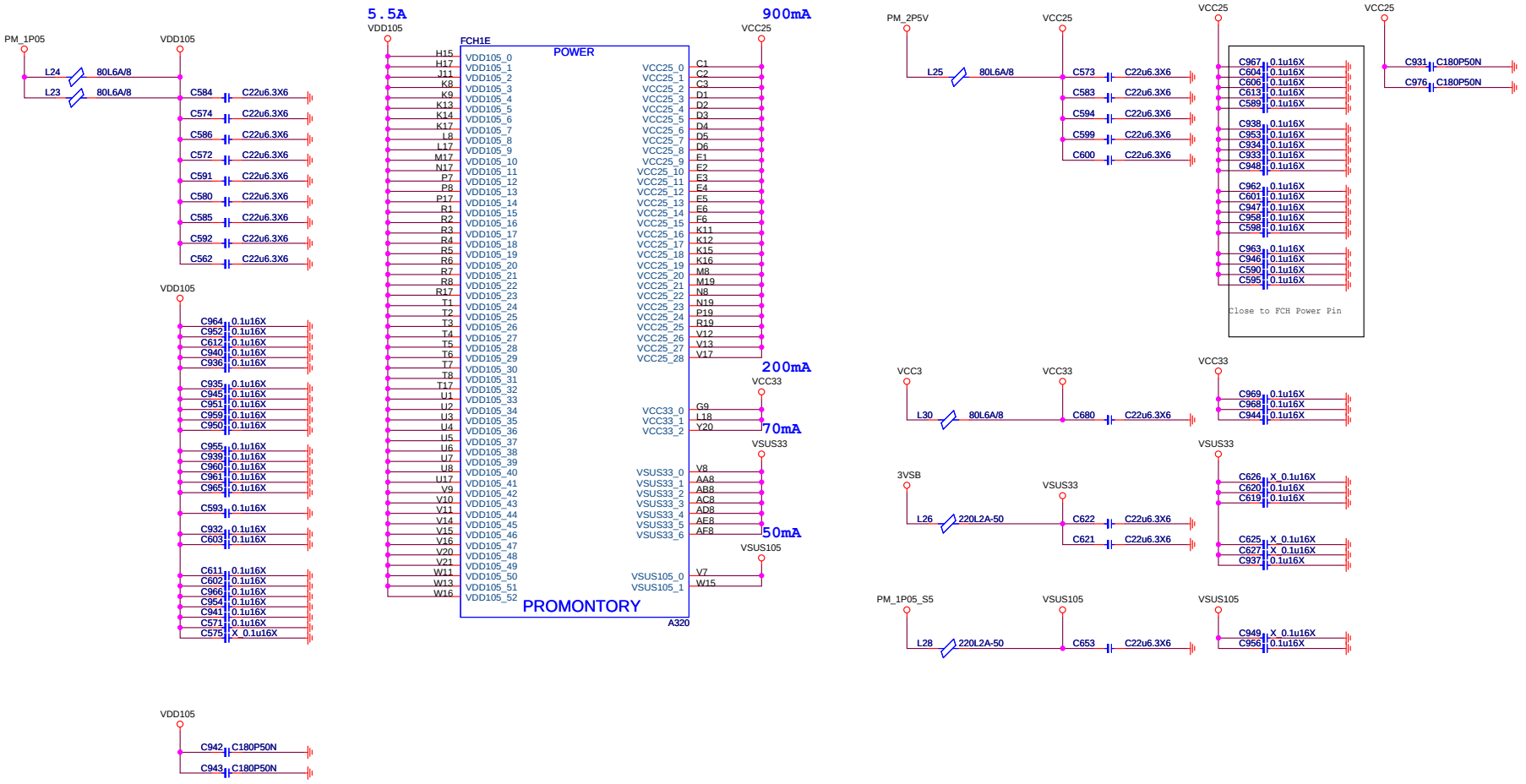

MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: Promontory-Power	Rev: 10
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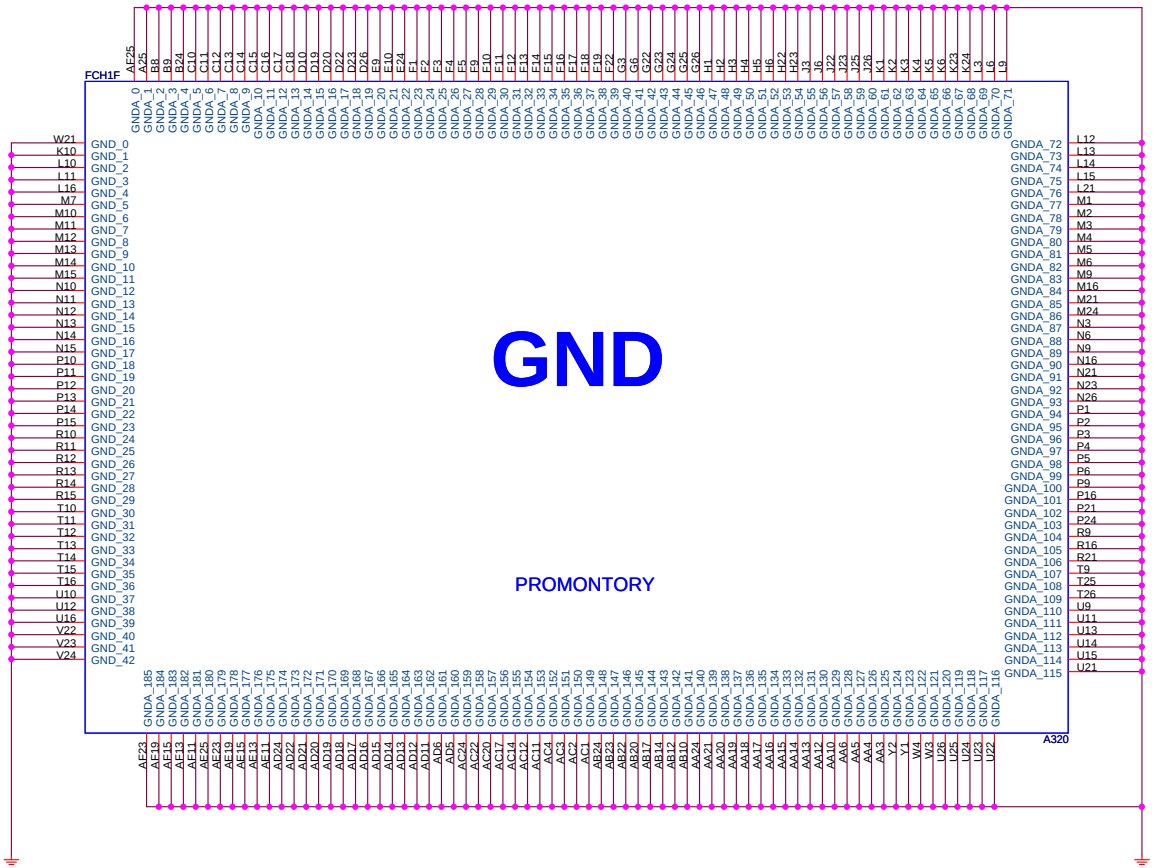

MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: Promontory-GND
Rev: 10	
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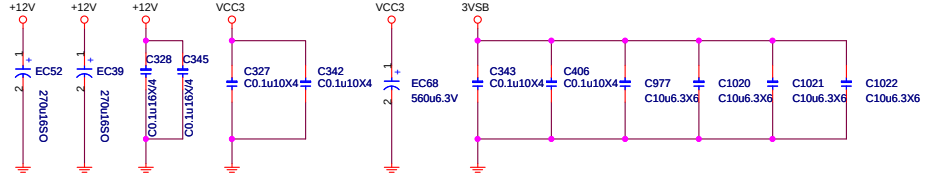
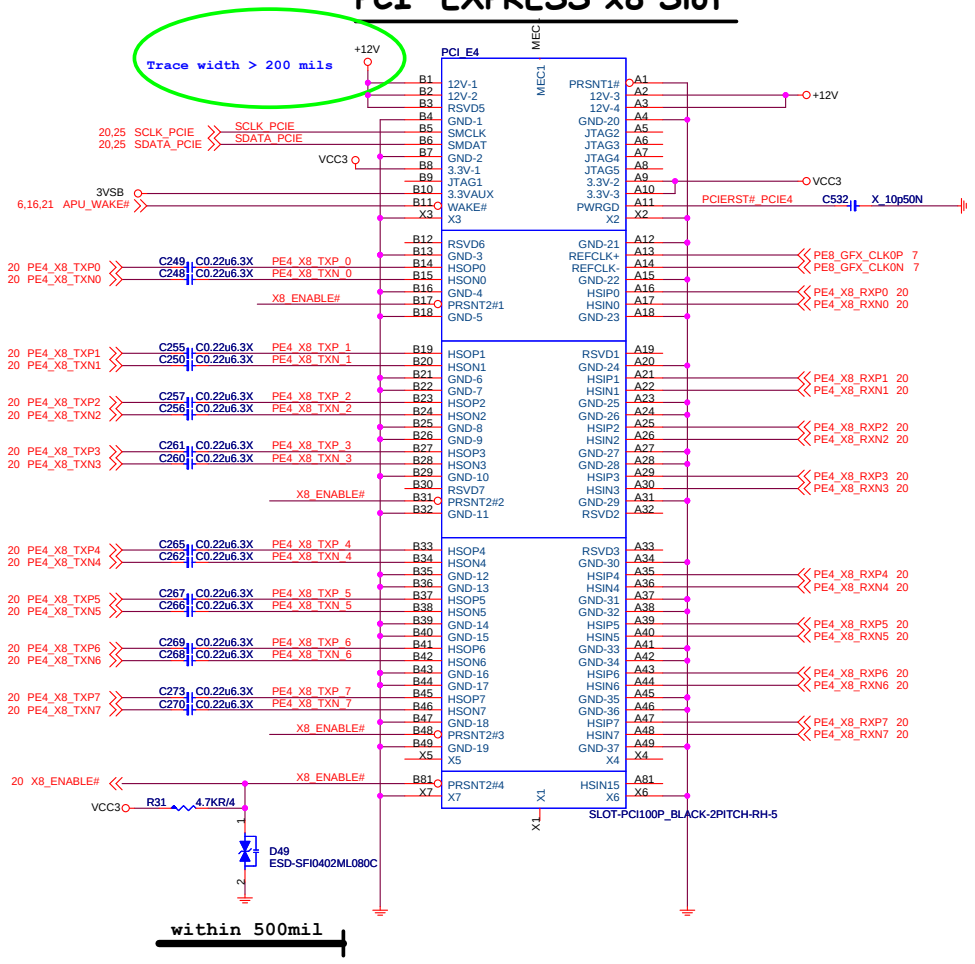
PCI EXPRESS x16 Slot

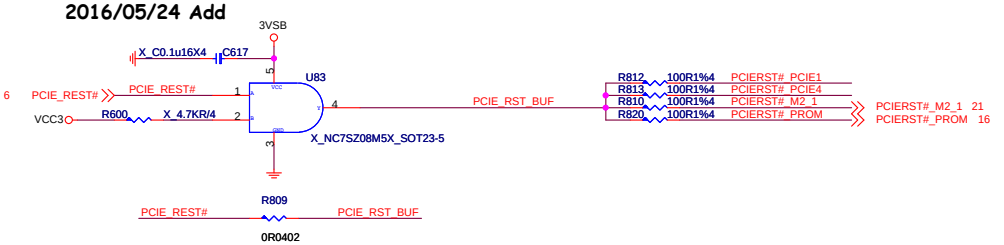
3.3V 3.0A
12V 5.5A



PCI EXPRESS x8 Slot



2016/05/24 Add



MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: PCIE X16(X8*2) SLOT
Rev: 10	
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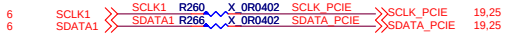
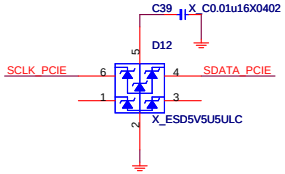
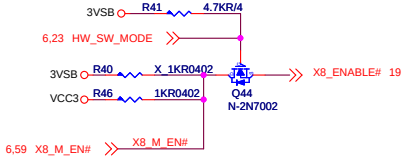
SMBus separate circuit

SMB_SEL
GPIO Default High





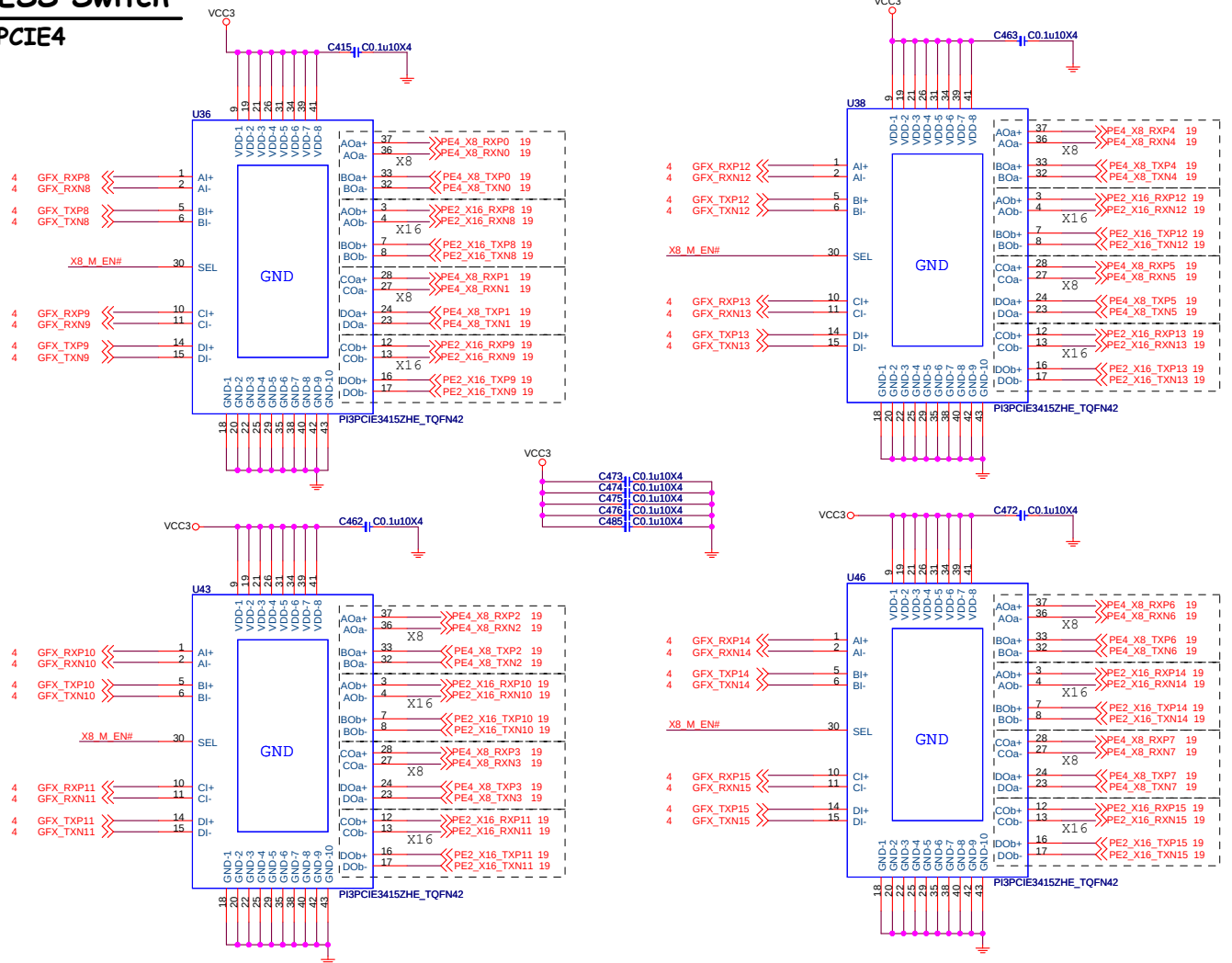
PCIE Lanes control circuit



	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

PCI EXPRESS Switch

For PCIE2 & PCIE4



MICRO-STAR INT'L CO.,LTD		
MS-7A32		
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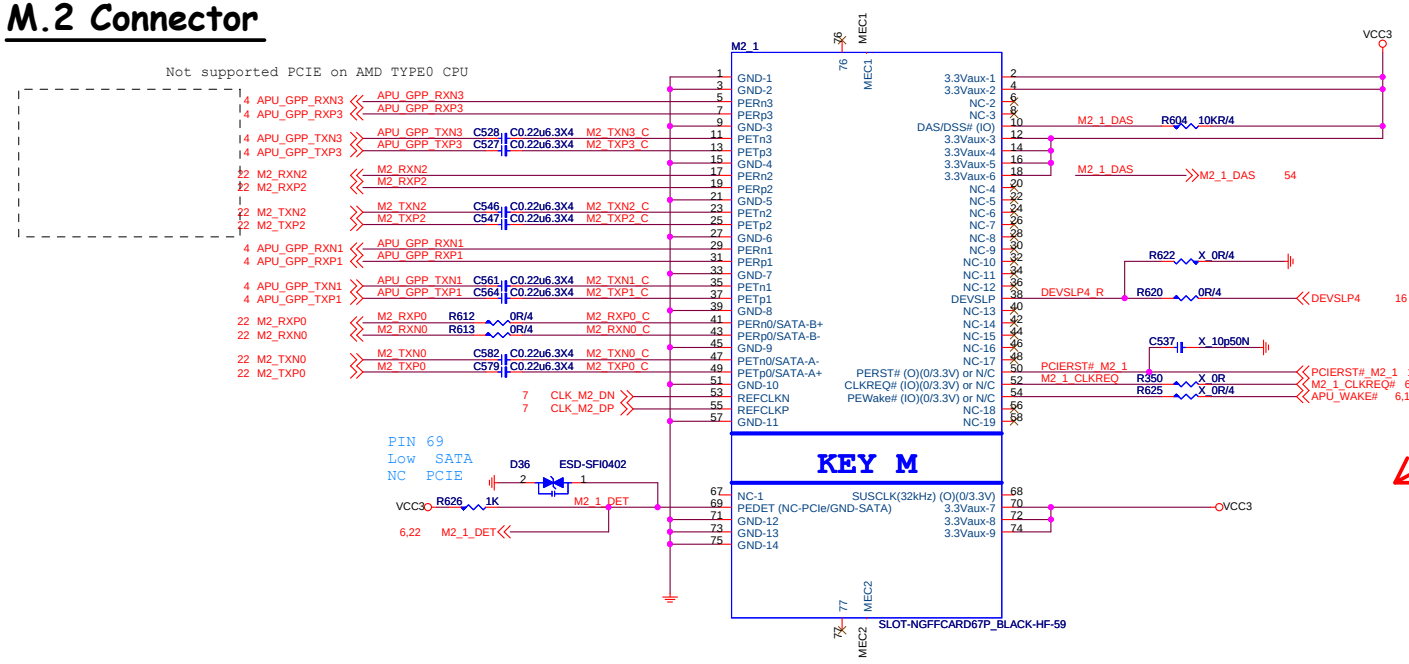
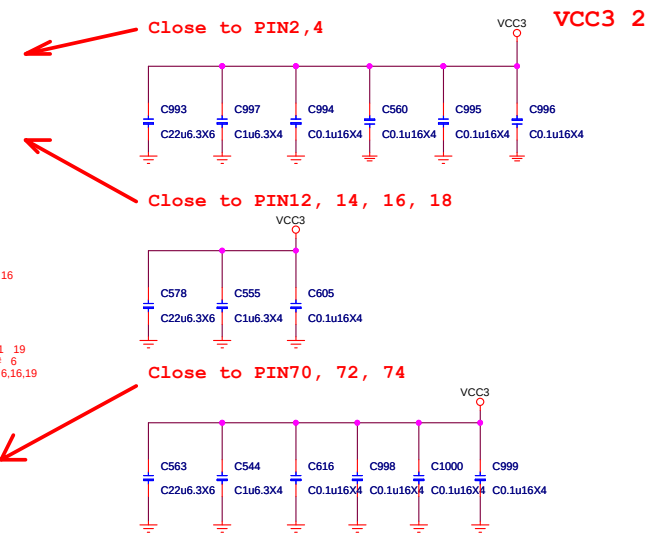
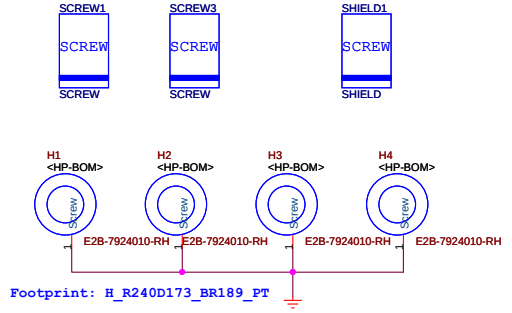
M.2 Connector





2016.05.31 Update M.2 PartNumber & Footprint
ON1-7A58001-L06
SLOT_NGFFCARD67_31



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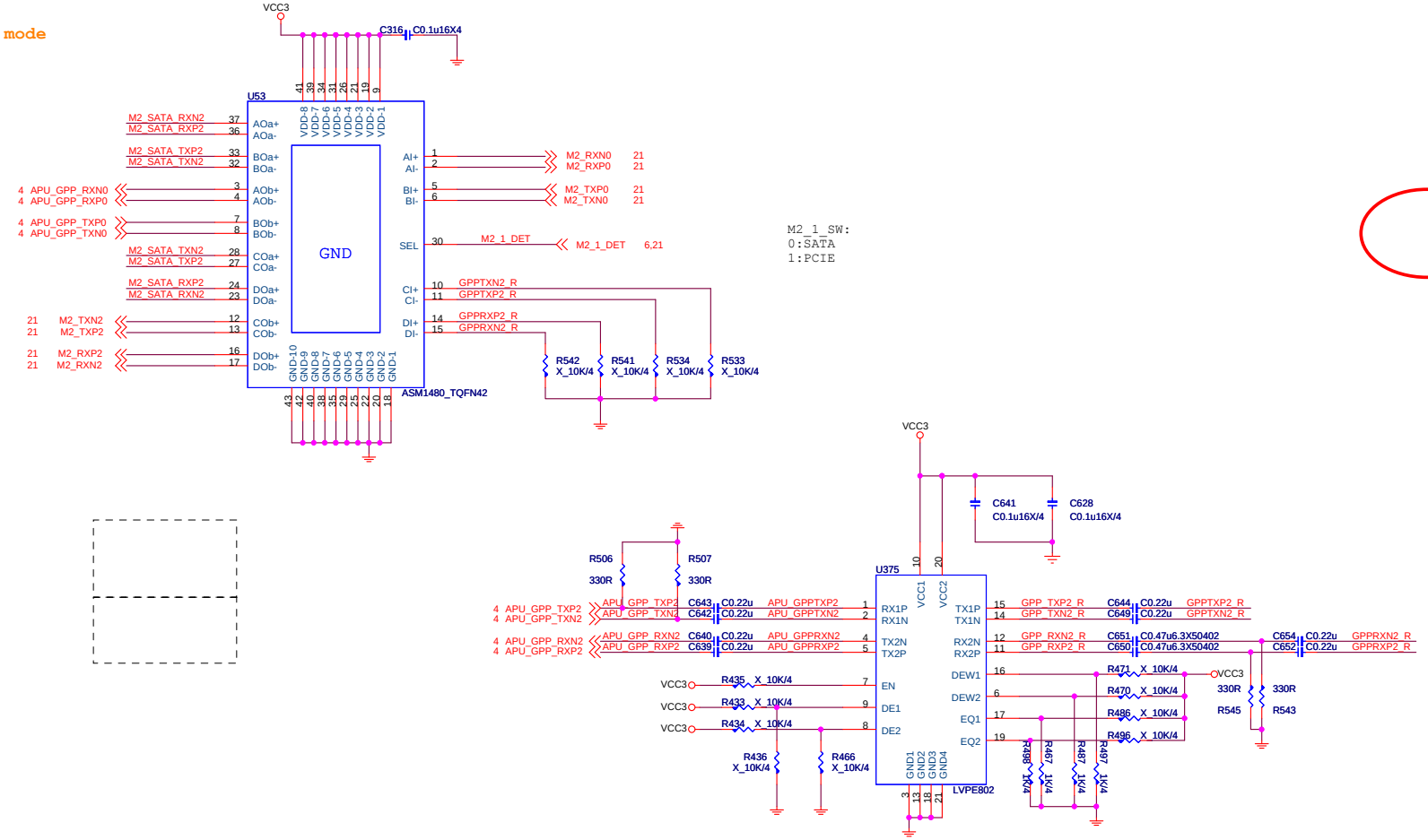
Select M2 PCIE or SATA mode



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Size: Custom	Document Description: M.2_1 Switch	Rev: 10
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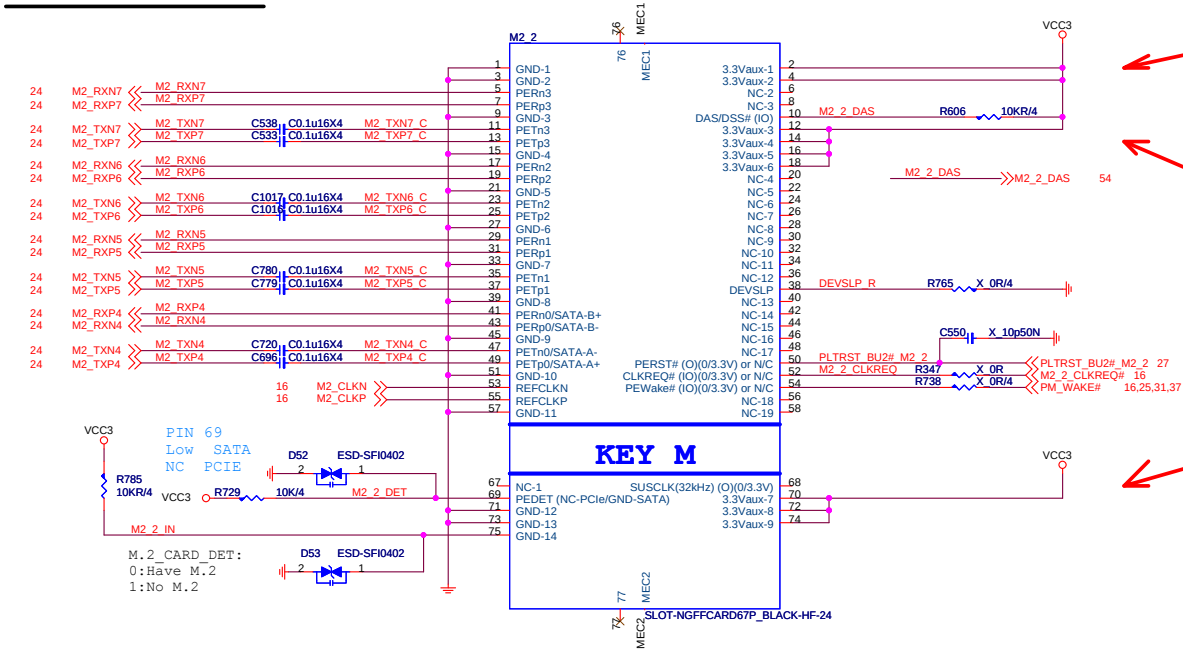
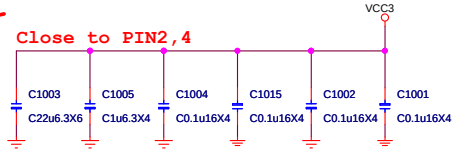
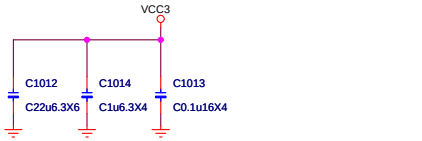
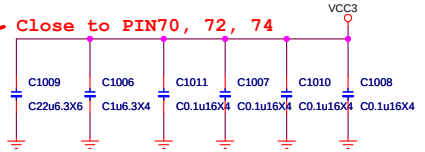
M.2 Connector

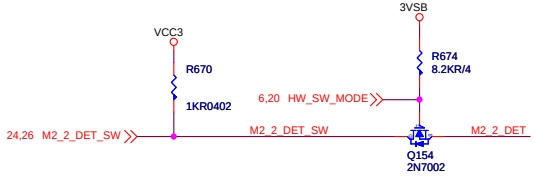


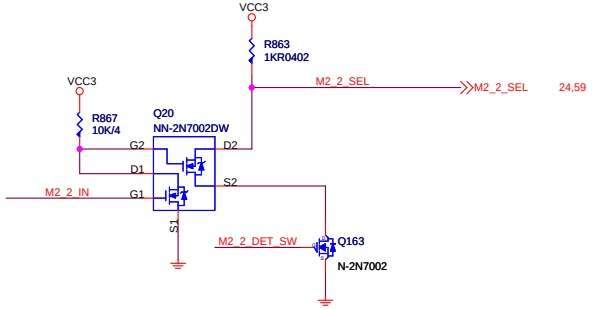
VCC3 2.5A

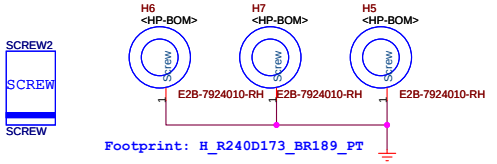












	M2	SATA	PCIEX4	M2_2_DET_SW	M2_2_IN	M2_2_SEL
M2 NOT IN	NO	YES	YES	1	1	1
M2 IN SATA	SATA	NO	YES	0	0	1
M2 IN PCIE	PCIE	YES	NO	1	0	0

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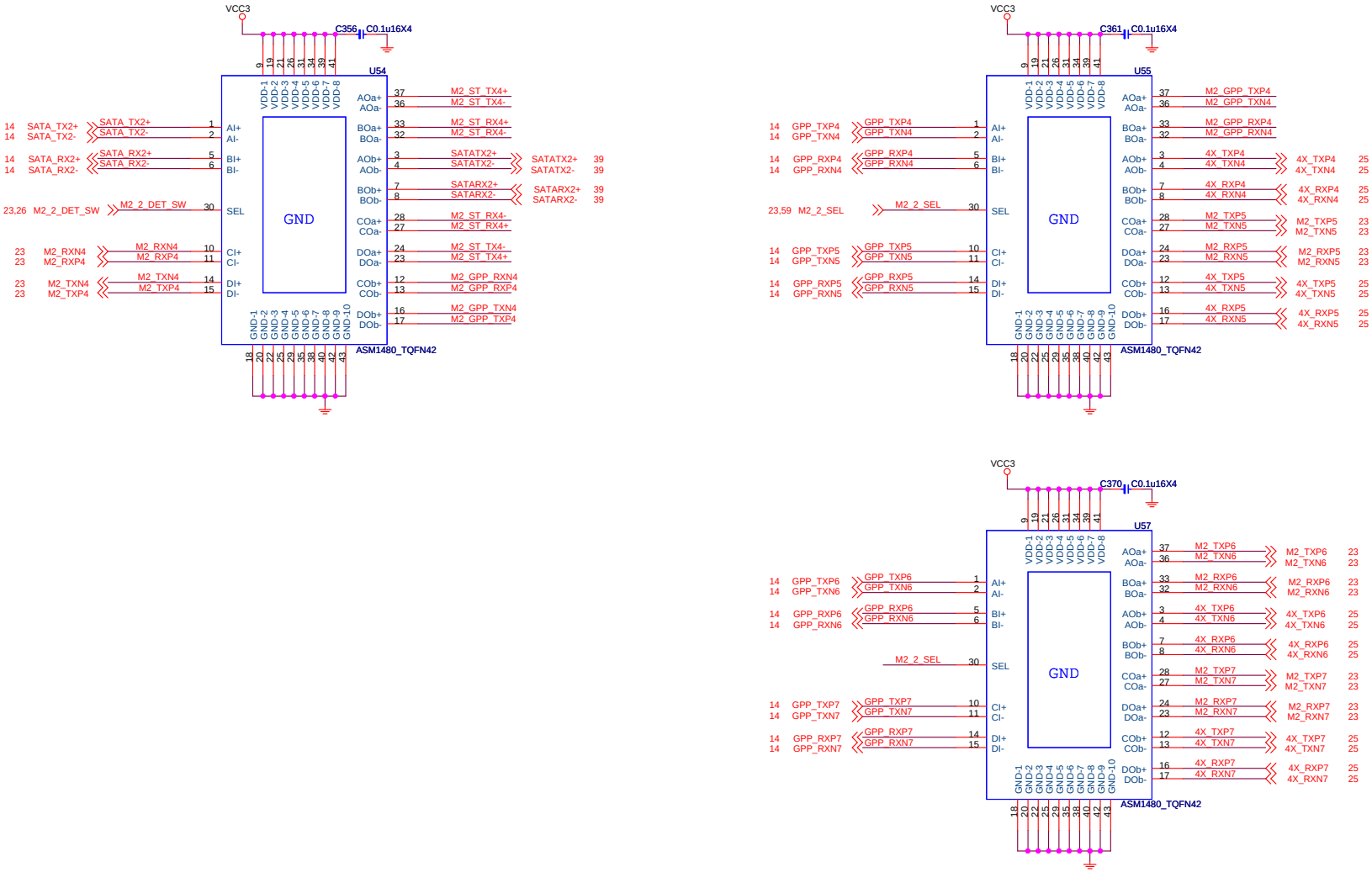

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Size: Custom	Document Description: M2_2 Switch	Rev: 10
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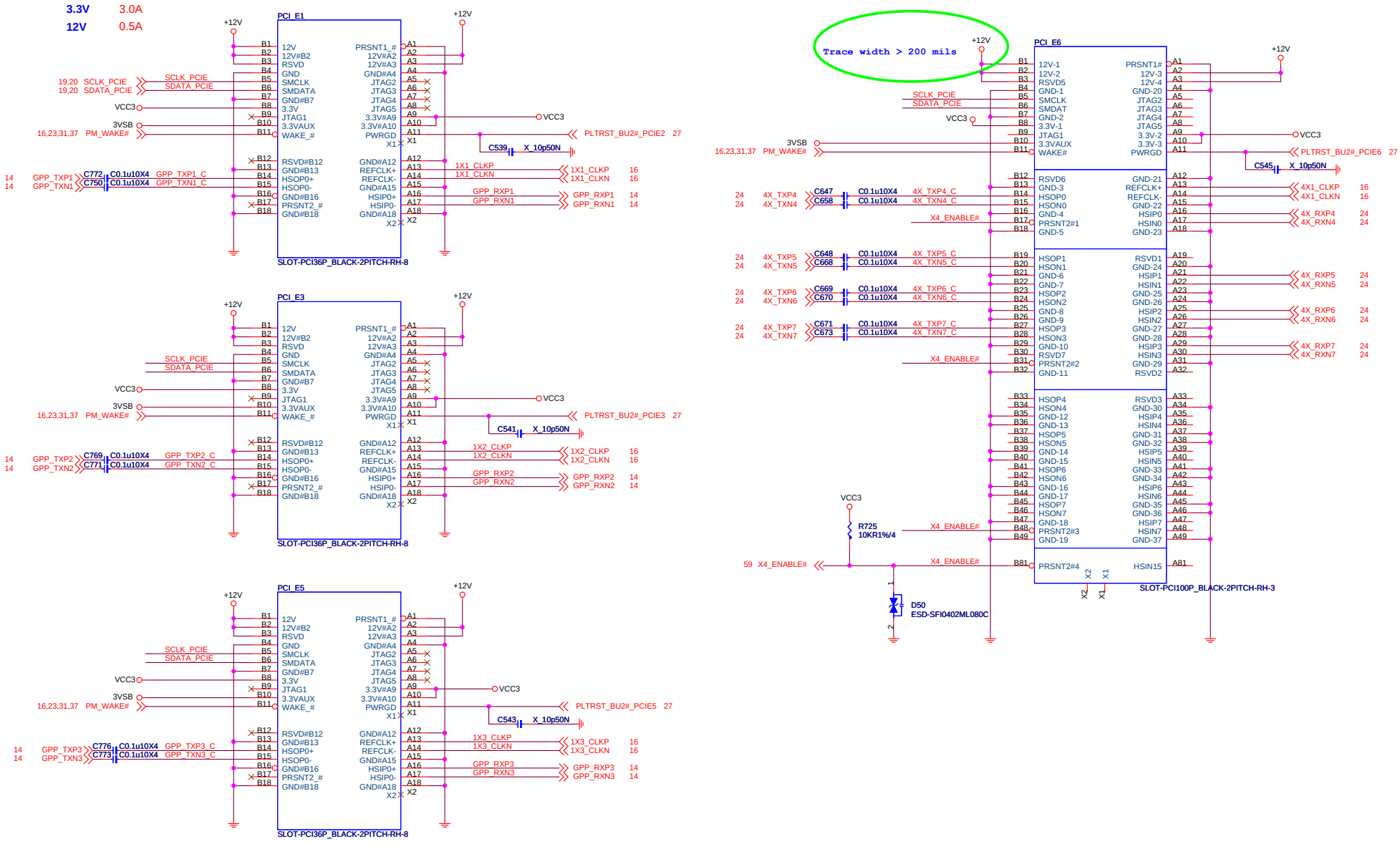
PCIEX1 12V 0.5A
3.3V weak 375mA



PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

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Size	Document Description	Rev
Custom	PCIE 1X 4X	10

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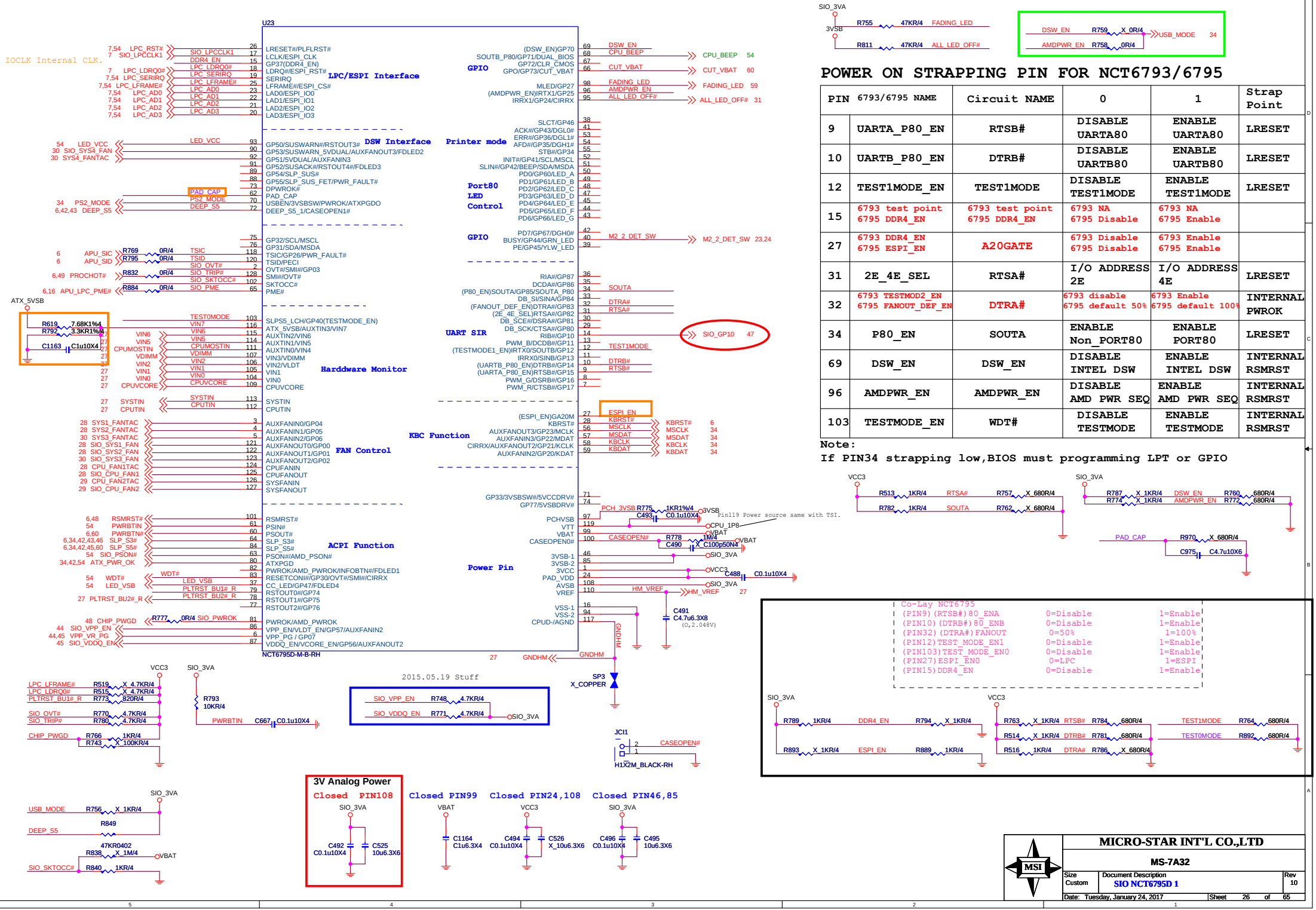

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

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HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

VCC_DDR — R701 10KR1%/4 — VDIMM — VDIMM 26
R716 10KR1%/4
C678 C10u6.3X6

VCORE — R719 10KR1%/4 — CPUVCORE 26
R732 X_10KR1%/4
C687 C10u6.3X6

+12V — R733 220K/1%/4 — VIN0 — VIN0 26
R736 20KR1%/4
C705 C0.1u16X4

VCC5 — R723 12K/1%/4 — VIN1 — VIN1 26
R727 3K/1%/4
C688 C0.1u16X4

Power Fault detect through VIN0,VIN1

VCCP_NB — R722 10KR1%/4 — VIN2 — VIN2 26
R741 X_10KR1%/4
C697 C10u6.3X6

Inform BIOS disable VIN2 with Power Fault

2016/05/24 Remove VIN4

CPU_VDDP — R726 10KR1%/4 — VIN5 — VIN5 26
C702 C10u6.3X6

TEMP SENSOR

For CPU

HM_VREF — HM_VREF 26
R731 10KR1%/4

CPUTIN — CPUTIN 26
RT5 10KRT1%0402
C684 C2200p50X

GNDHM — GNDHM 26

Under Socket

For System

SYSTIN — SYSTIN 26
Q123 P-3906 (E, B, C)
C689 2.2n50X
GNDHM

For CPU

HM_VREF — HM_VREF 26
R796 10KR1%/4

2016/05/24 Add

CPUMOSTIN — CPUMOSTIN 26
RT6 10KRT1%0402
C1018 C2200p50X

GNDHM

Close to CPU MOS

For PM

HM_VREF — HM_VREF 26
R739 10KR1%/4

VIN6 — VIN6 26
RT7 10KRT1%0402
C692 C2200p50X

GNDHM — GNDHM 26

Under PM BOT

RESET

26 PLTRST_BU2#_R — PLTRST_BU2#_R — R827 X_22R1%/4 — PLTRST_BU2#

R839	100R1%4	PLTRST_BU2#_PCIE2	PLTRST_BU2#_PCIE2	25
R833	100R1%4	PLTRST_BU2#_PCIE5	PLTRST_BU2#_PCIE5	25
R826	100R1%4	PLTRST_BU2#_PCIE3	PLTRST_BU2#_PCIE3	25
R834	100R1%4	PLTRST_BU2#_PCIE6	PLTRST_BU2#_PCIE6	25
R819	100R1%4	PLTRST_BU2#_LAN	PLTRST_BU2#_LAN	31
R943	100R1%4	PLTRST_BU2#_ASM2142	PLTRST_BU2#_ASM2142	37
R959	100R1%4	PLTRST_BU2#_M2_2	PLTRST_BU2#_M2_2	23

16 PM_GPP_RST — PM_GPP_RST — R936 0R0402 — PLTRST_BU2#

Co-lay FCH Reset for meet FCH sequence. See 55553.

MICRO-STAR INT'L CO.,LTD

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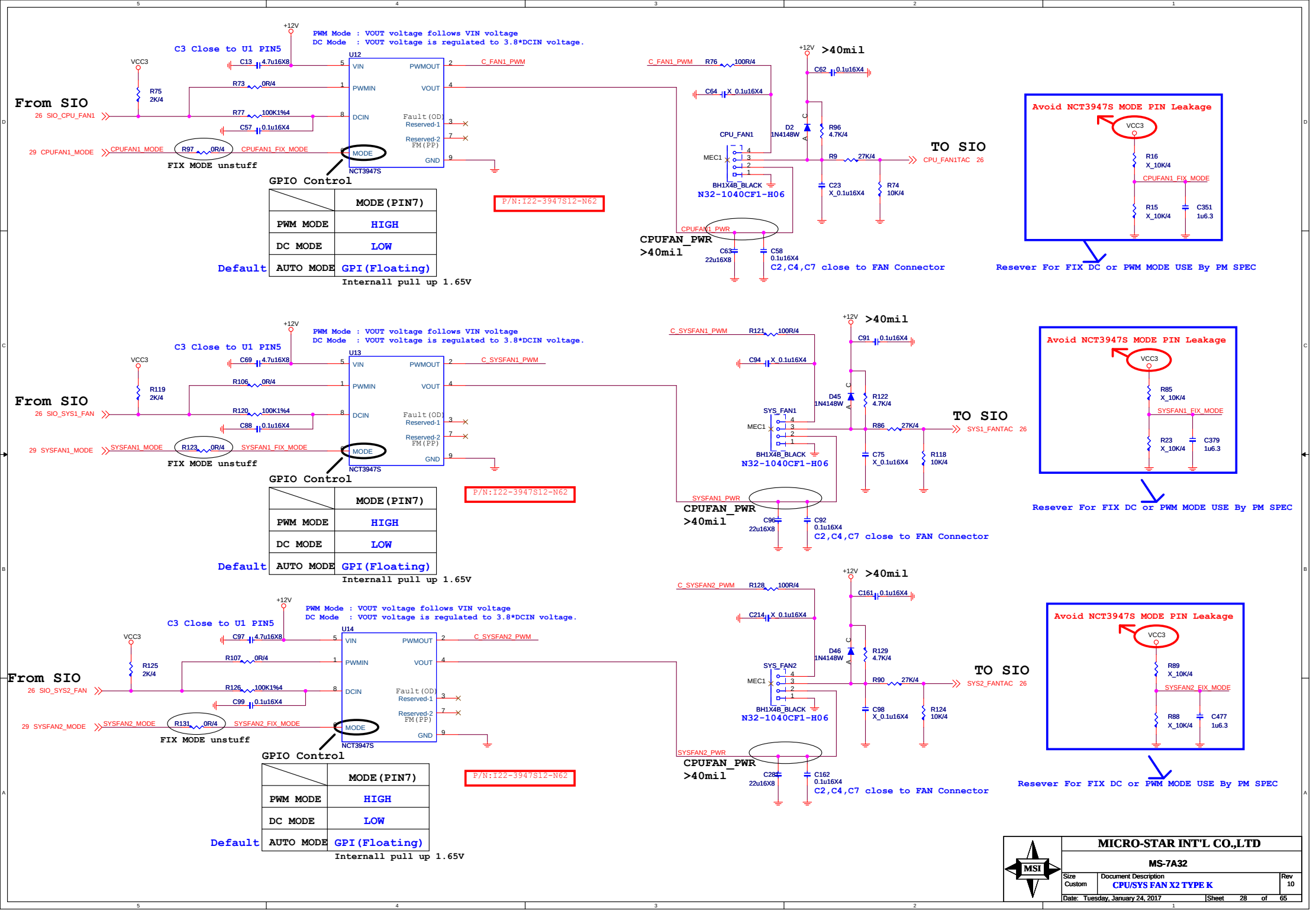

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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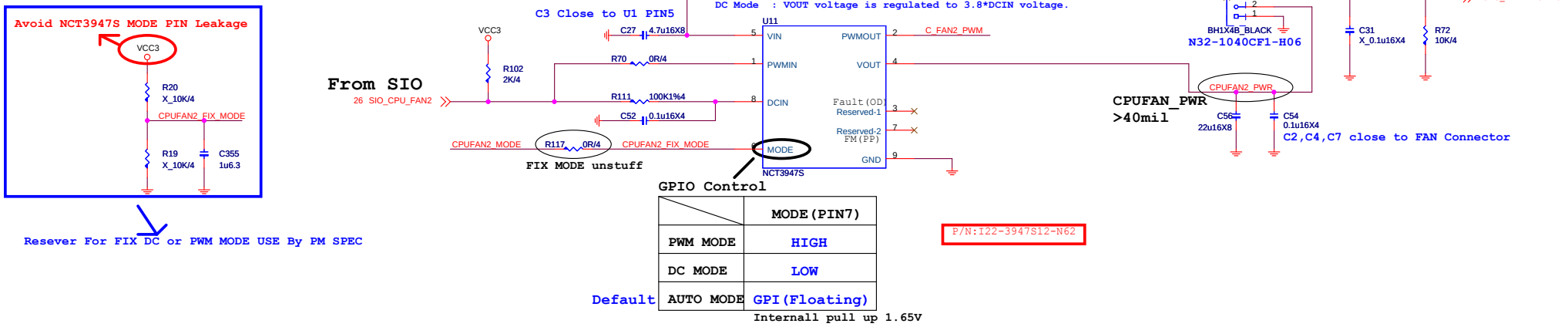
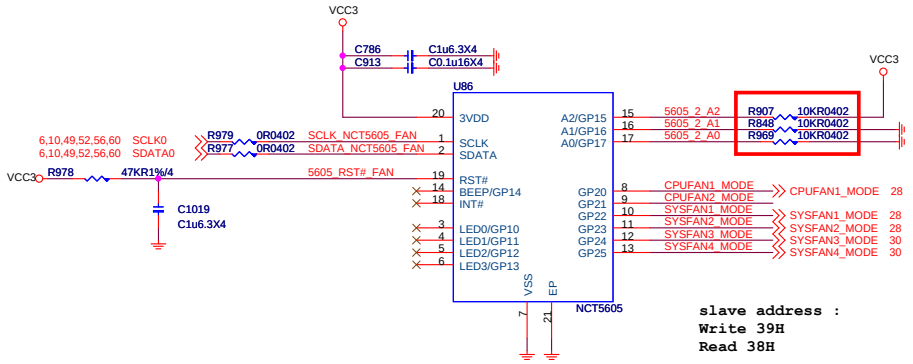
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE





1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

R/W: 0 = Write, 1 = Read

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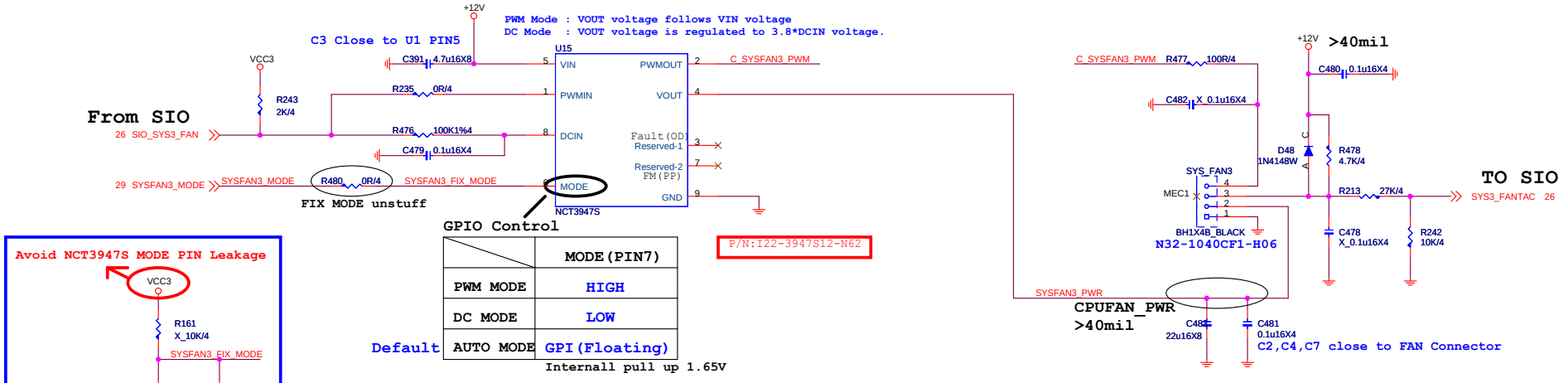
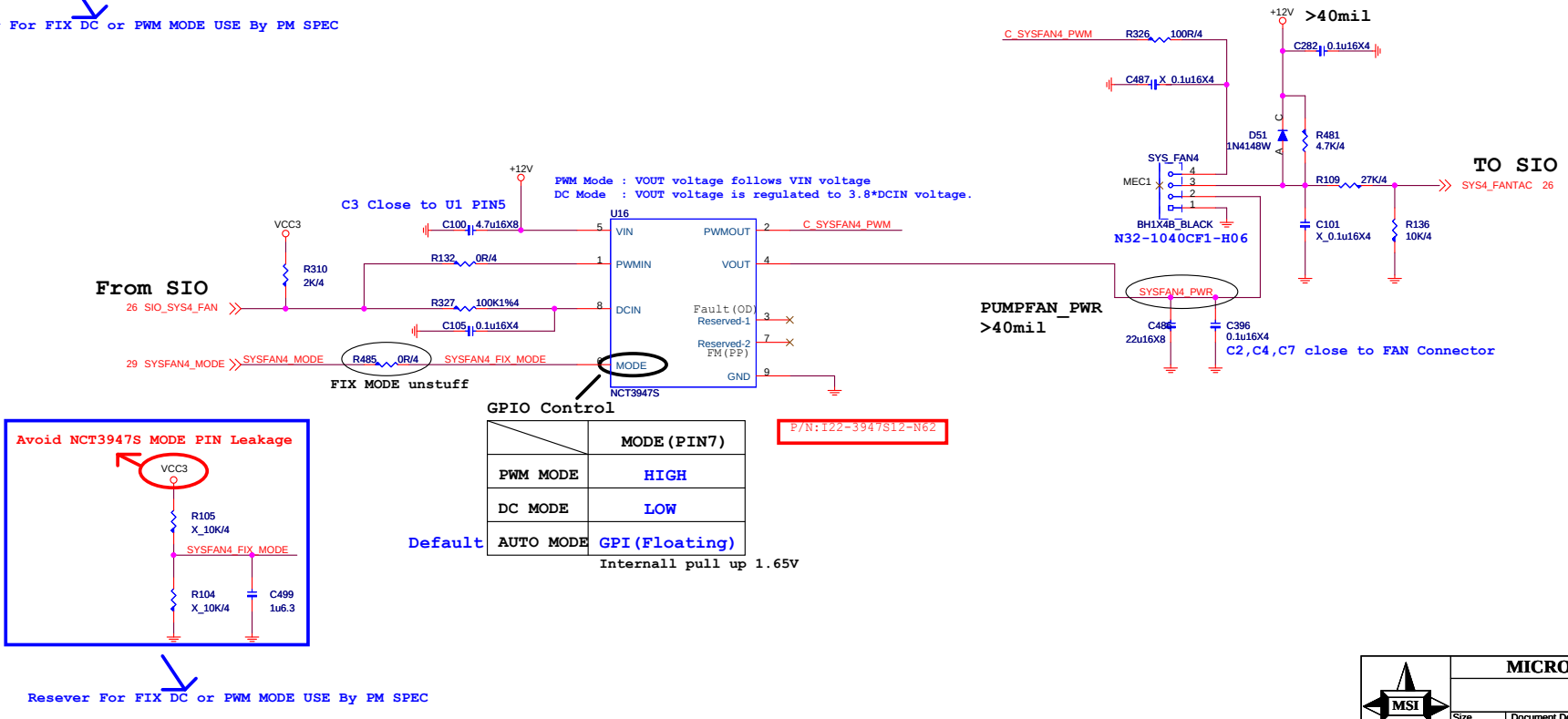
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち伝 PWM/DC MODE





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Model	MS-7A32
Size	Custom
Document Description	SYS FAN X2 TYPE K
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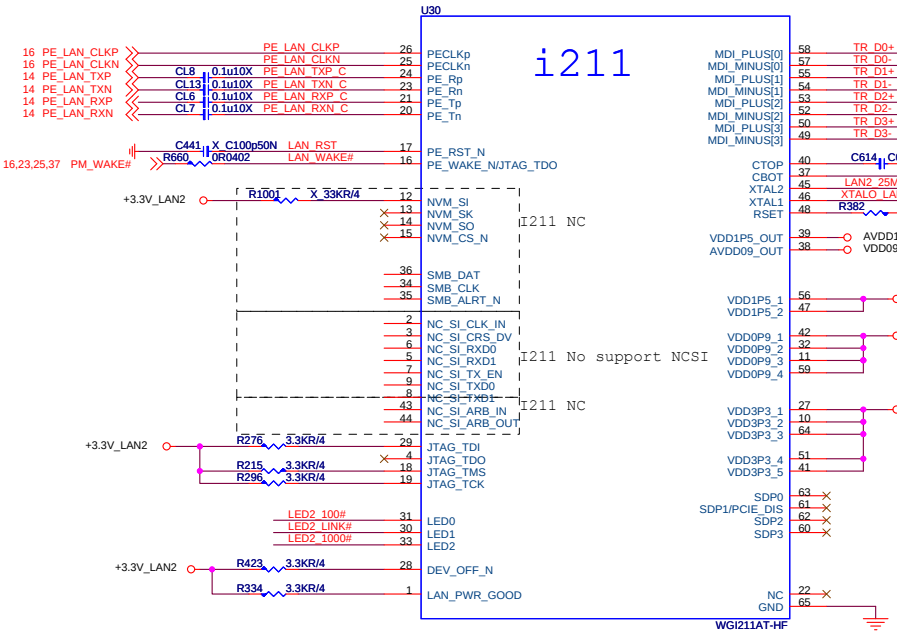
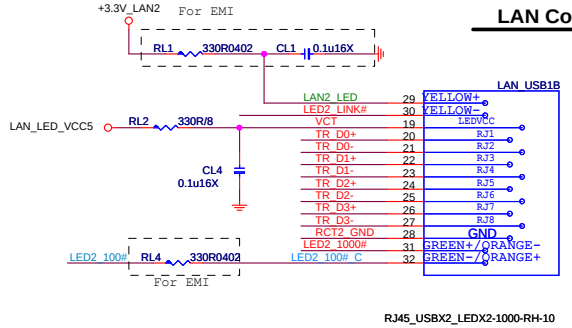
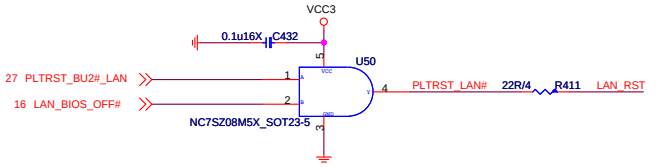
LAN2-- I211AT

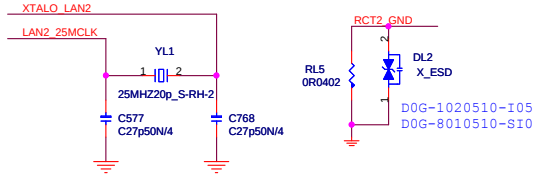


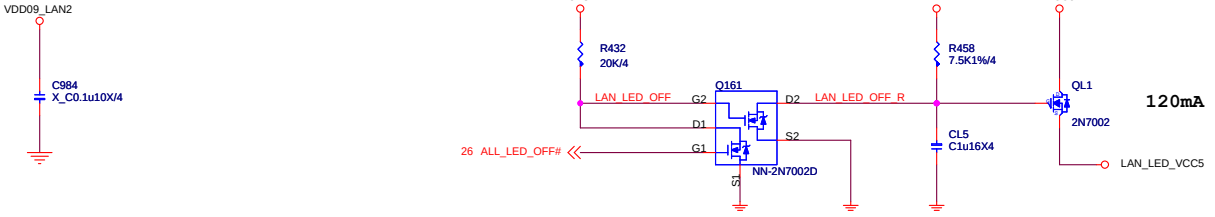
LAN Connector

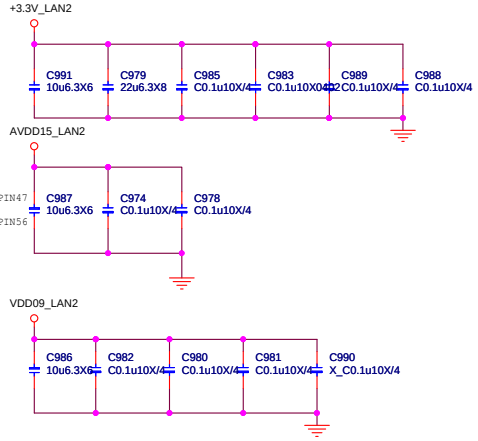


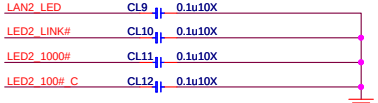
RJ45_USBX2_LEDX2-1000-RH-10

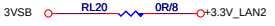


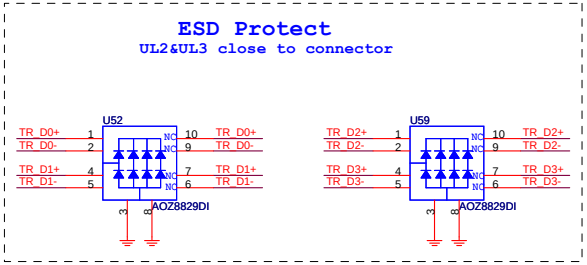












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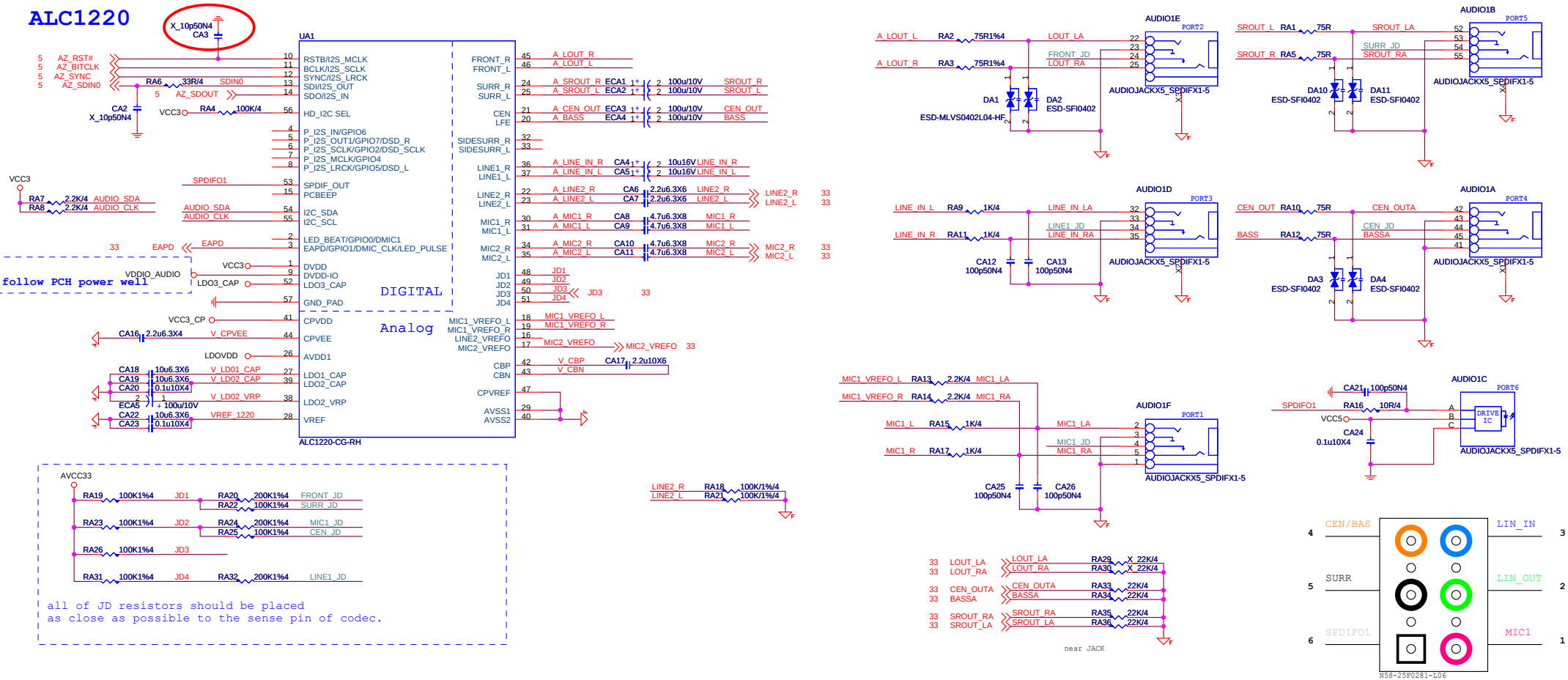
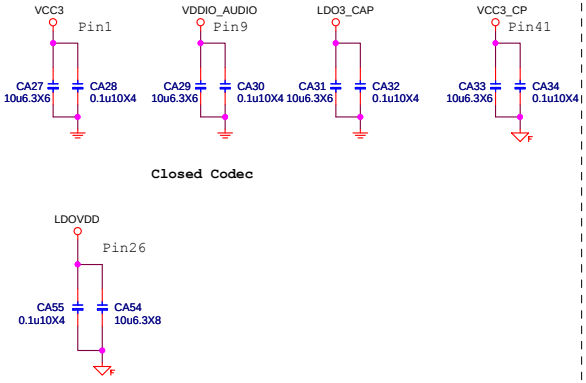
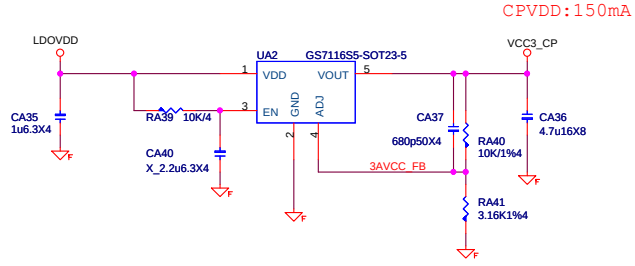
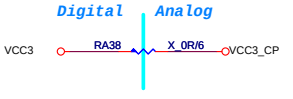
ALC1220

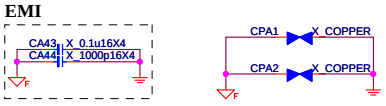




CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V







MICRO-STAR INT'L CO.,LTD

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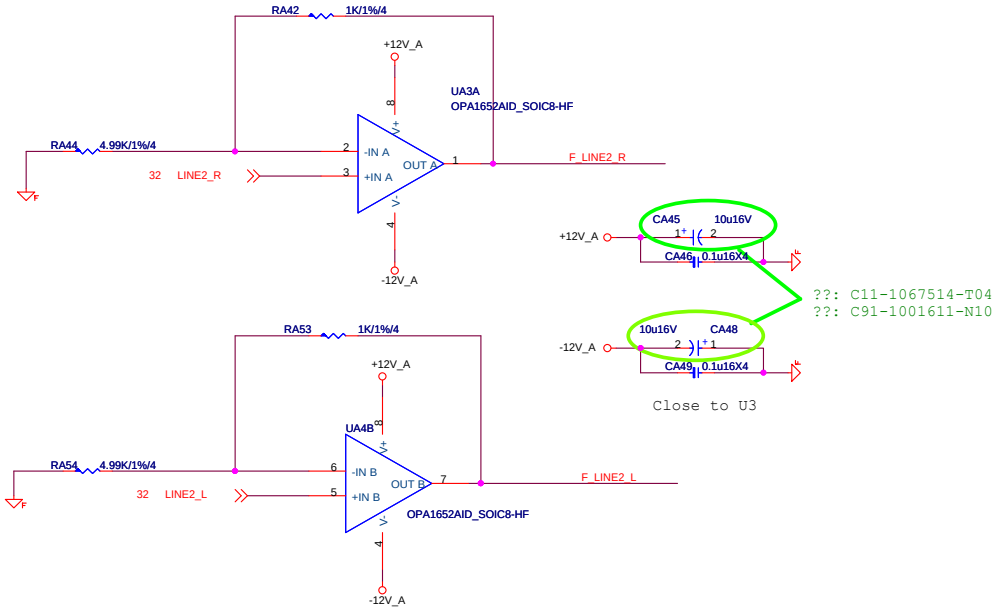
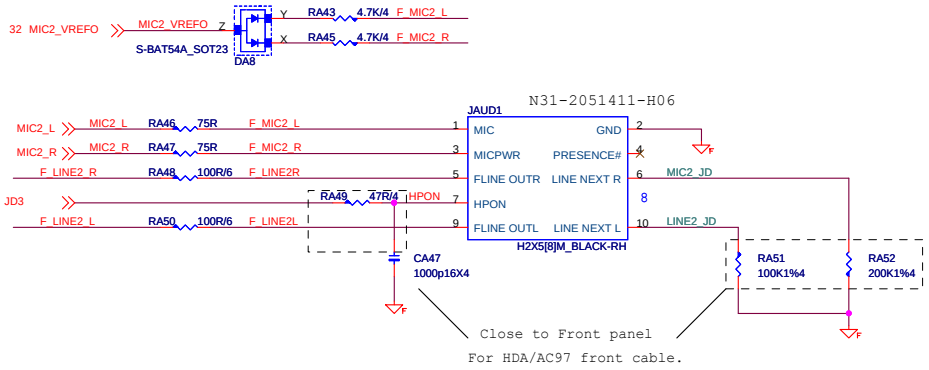


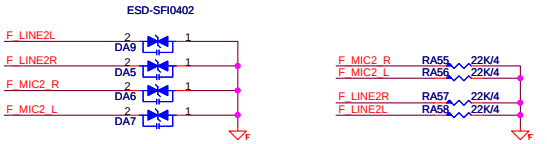


Close to Jack

ESD protect

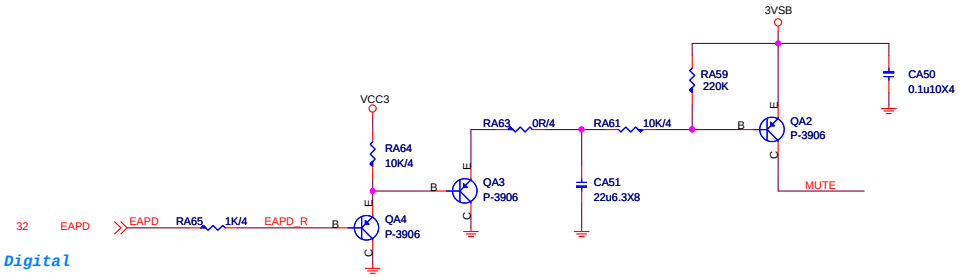
D0G-2950500-SI0

D0G-2710510-I05



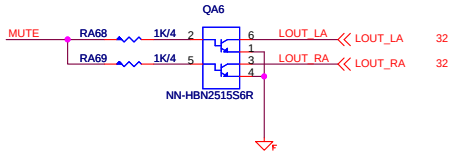
Rear Line OUT De-POP circuit

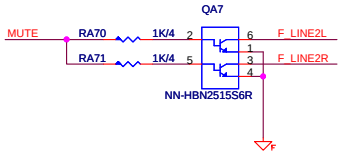
(De-pop circuit for Rear Line out & Front Headphone out)

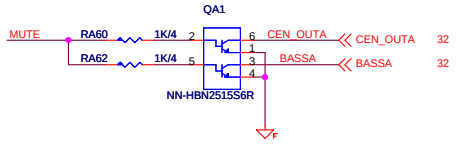


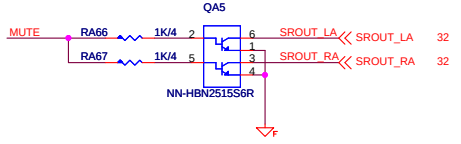
Digital

Analog









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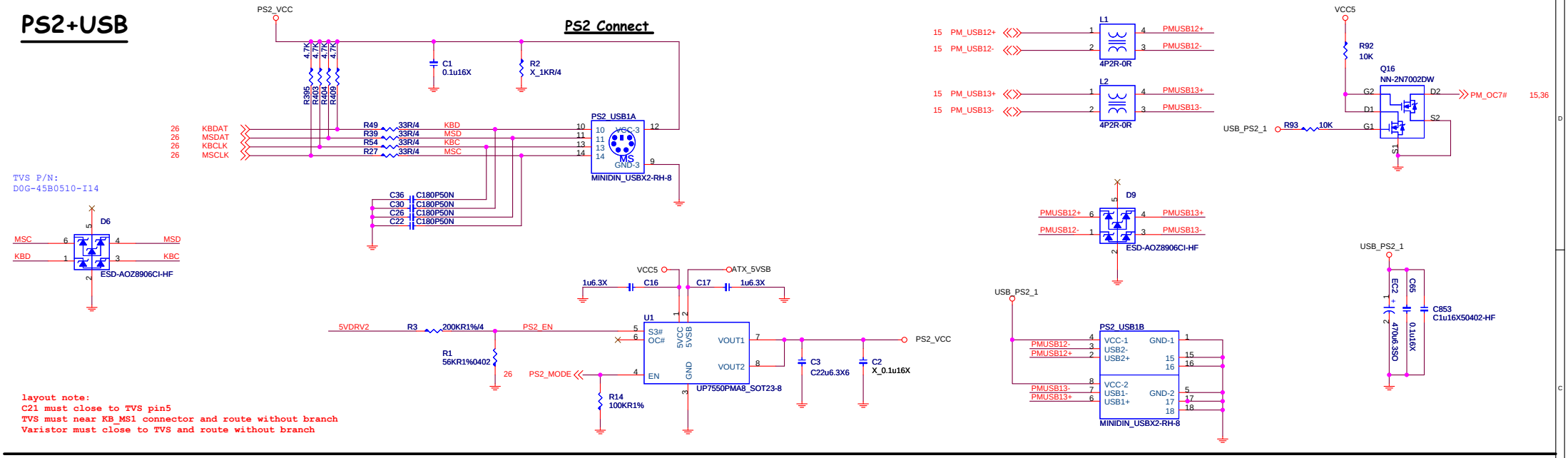
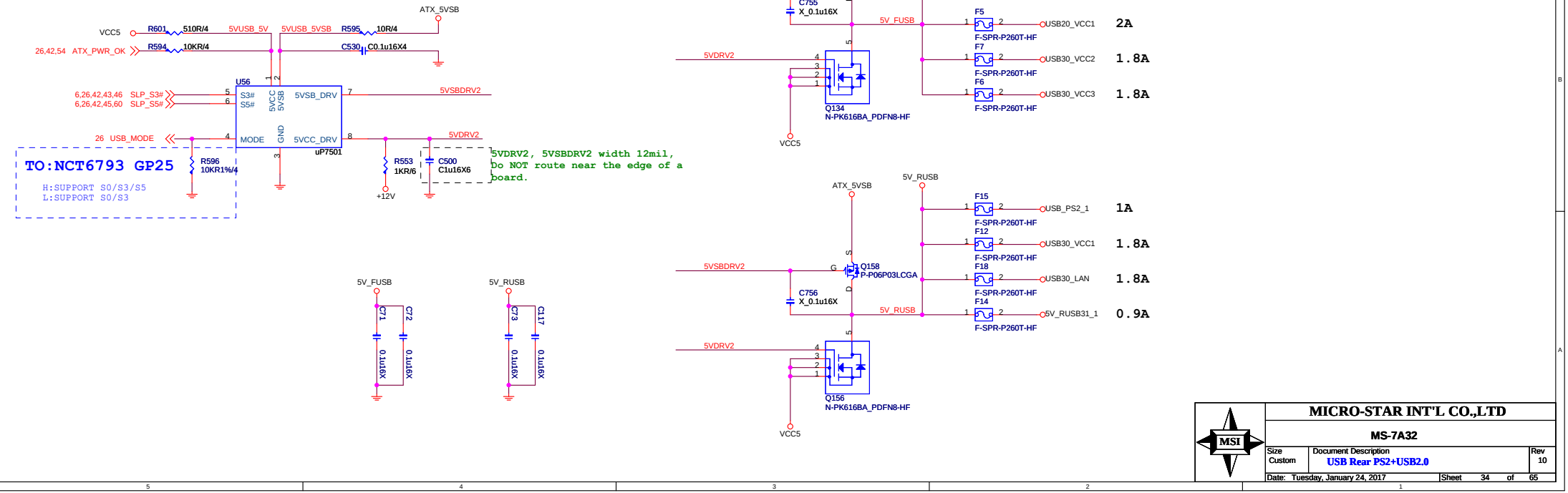
PS2+USB



USB Power



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Custom	USB Rear PS2+USB2.0	10

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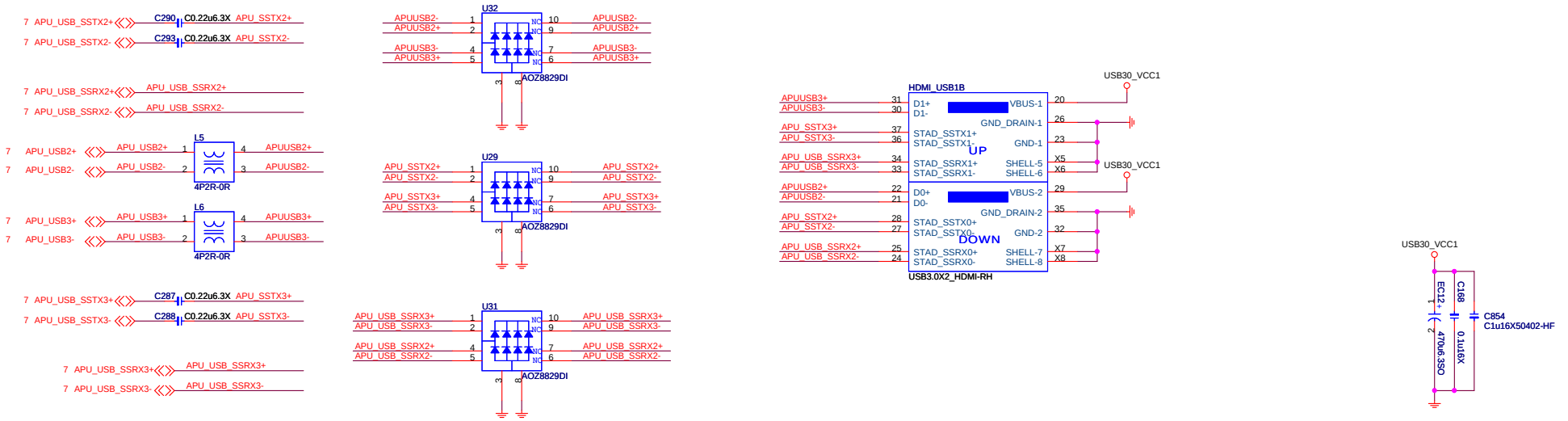
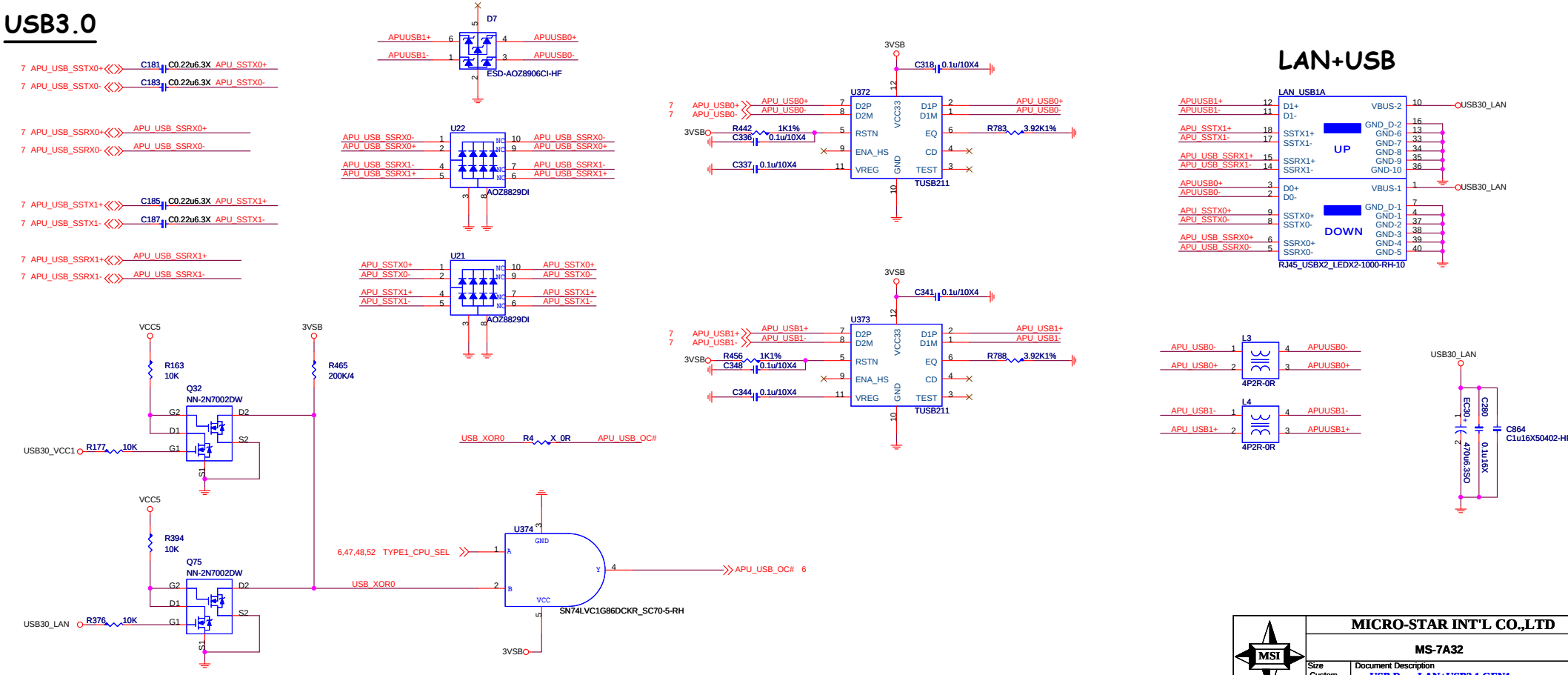
USB 3.0



USB3.0



LAN+USB

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MS-7A32	
Size: Custom	Document Description: USB Rear LAN+USB3.1 GEN1
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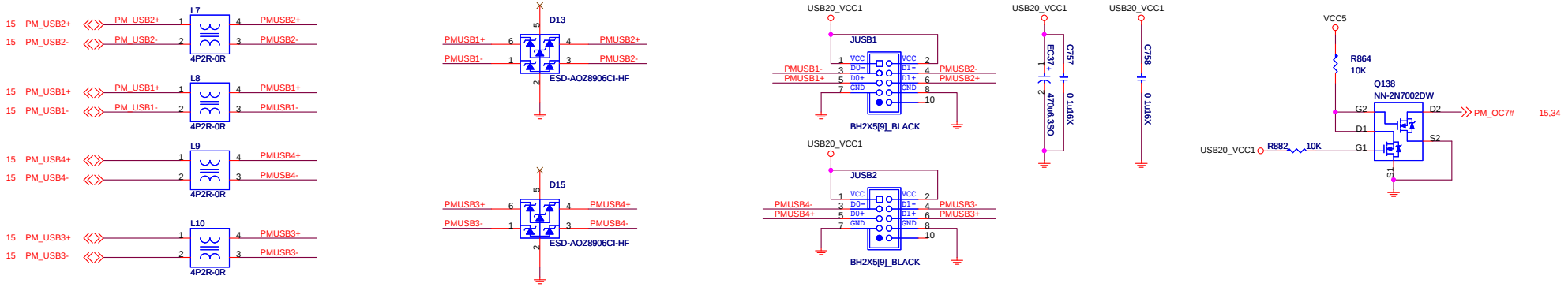
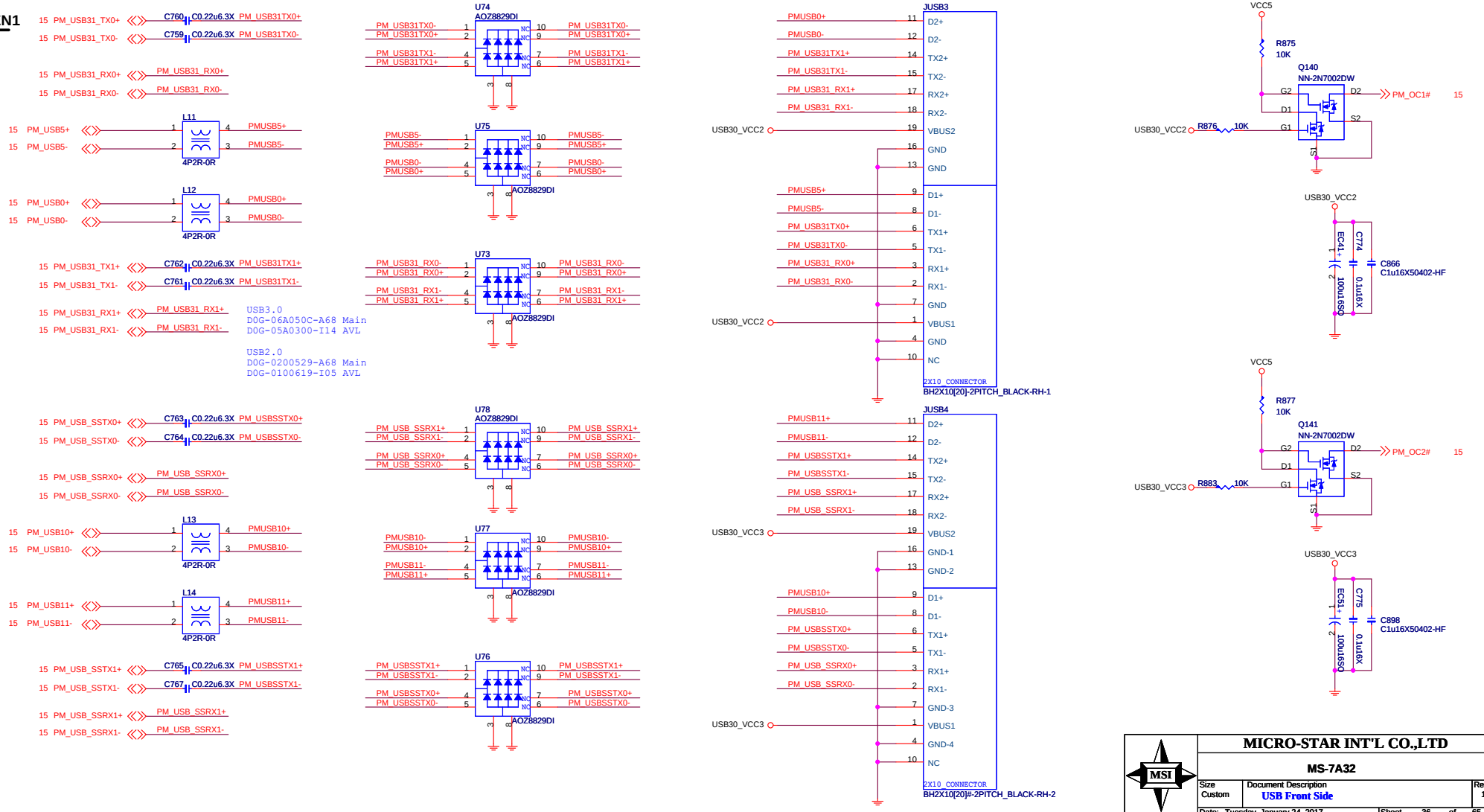
Front USB2.0



Front USB3.1 GEN1



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Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

Minimun gap should be greater of >15mil with other signal.

Chip to Connector <1.5 inch.

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

ASM1142 RU29 stuff RU28 unstuff
ASM2142 RU29 unstuff RU28 stuff

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to 3VS

RX/TX Internal Pull-up

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

YU1
D04-0901200-F07
D04-0901100-T16

ASM1142 RU14 stuff RU16 unstuff
ASM2142 RU14 unstuff RU16 stuff

P/N:B02-021421C-AD0

ASM2142 UU8 stuff RU6 unstuff
ASM1142 UU8 unstuff RU6 stuff

Reset control for ASM2142 only.

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

ASM1142 RU1/RU2 200K/187K 1.24V
ASM2142 RU1/RU2 196K/261K 1.05V

ASM1142 1.2 VSB Power

ASM1142 RU31 18K 1.24V
ASM2142 RU31 31.6K 1.05V

EEPROM

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25L1022-M24(1M bit)

ASM1142/ASM1042 unstuff
ASM2142 stuff

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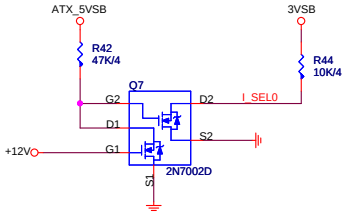
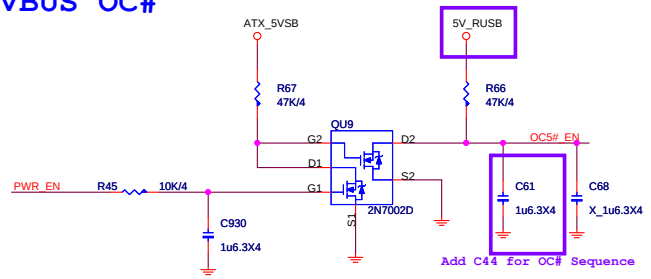
Current Mode

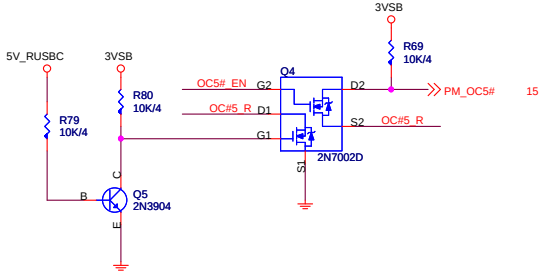


I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

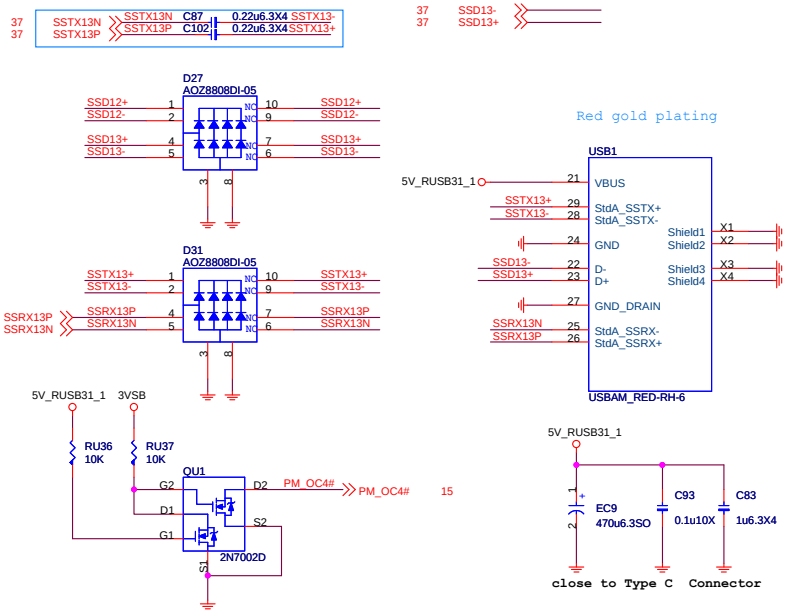
1.5A under S3 mode
3A under S0 mode

VBUS OC#

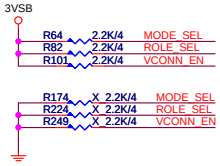




TYPE-A



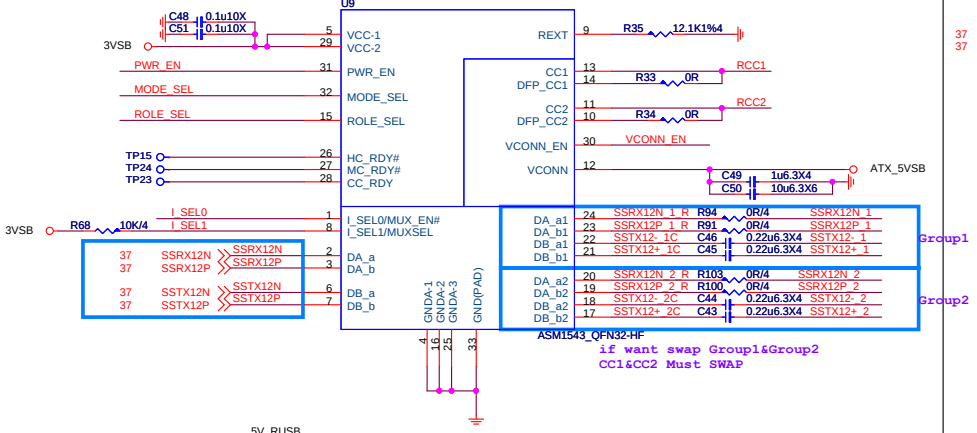
USB Type-C MUX with Configuration Channel (CC)

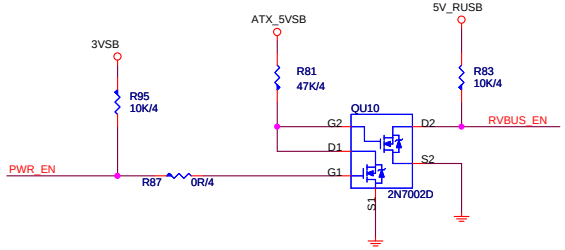


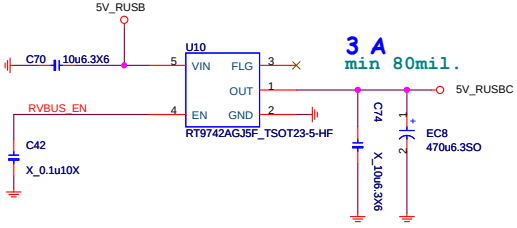
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

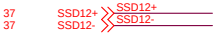
VCONN_EN	
1	enable
0	disable

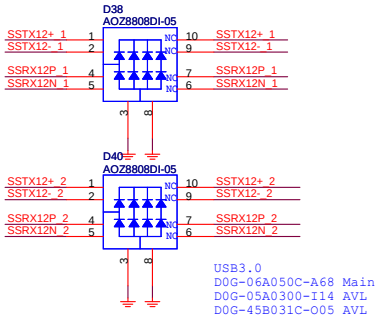


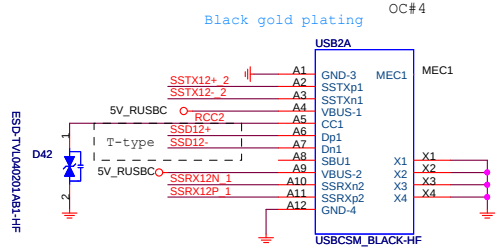




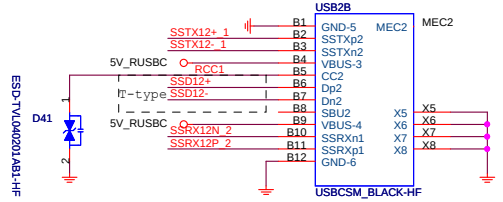
TYPE-C



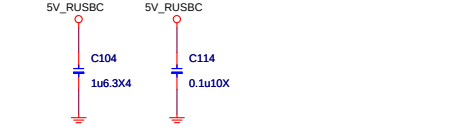




T-type だや惠 140mils



close to Type C Connector



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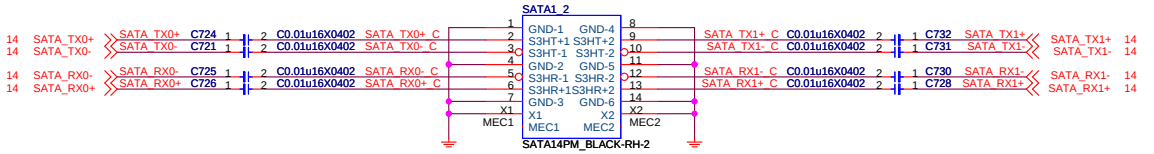
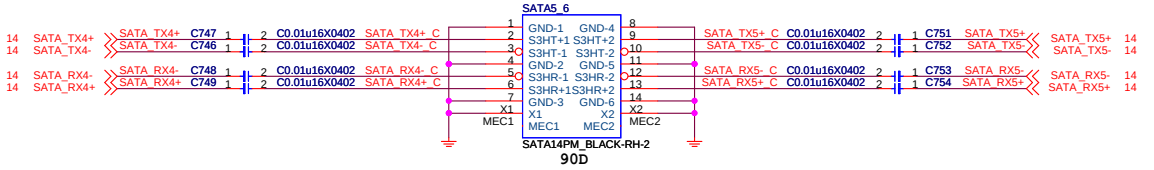
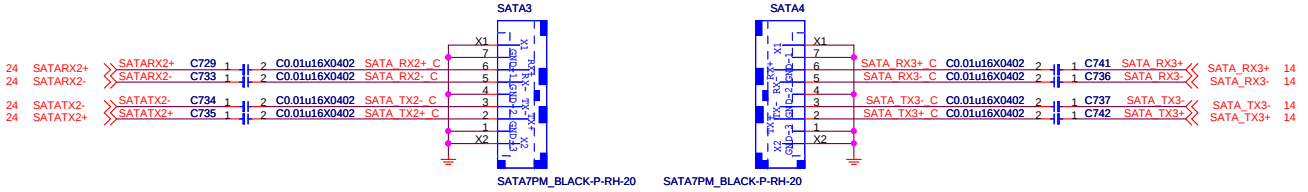
SATA Connector





180D



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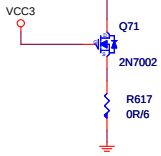
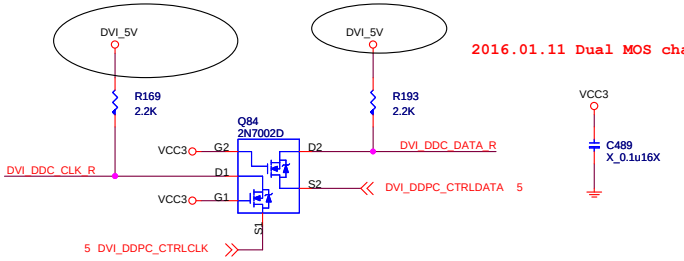
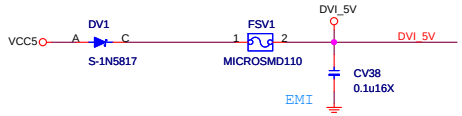
DVI level shifter

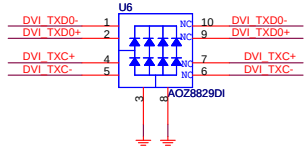
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

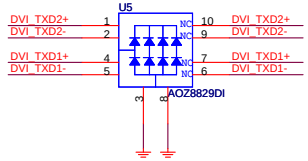


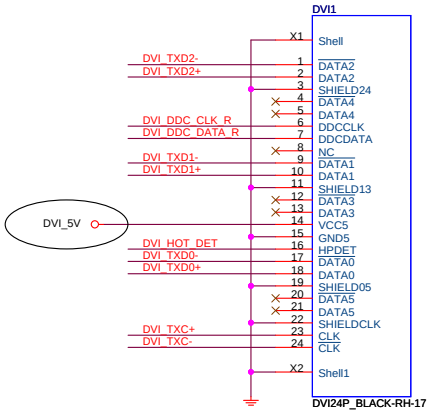


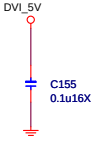
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

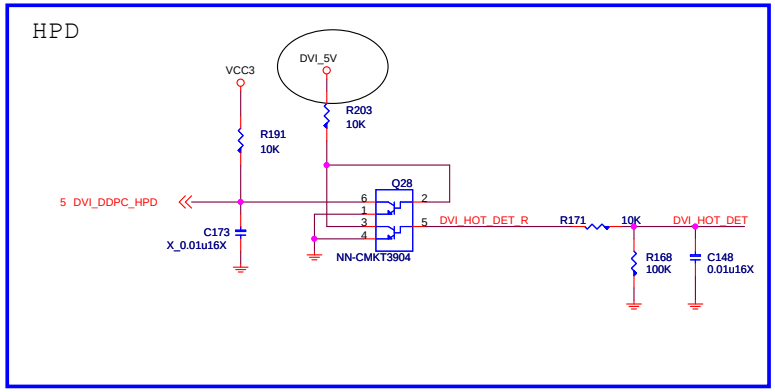


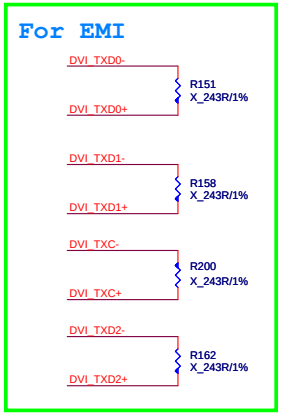


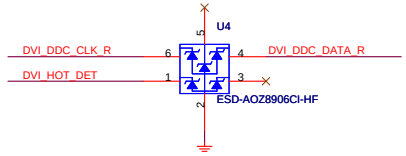


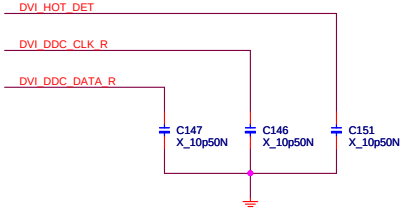












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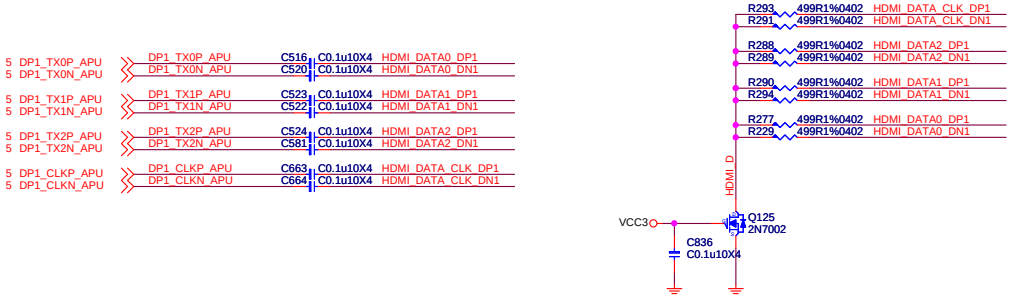
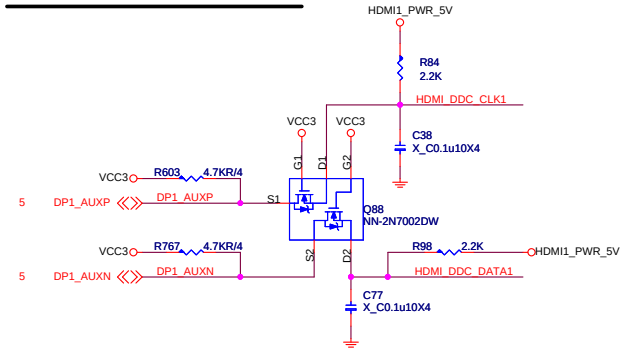
HDMI CONNECTOR

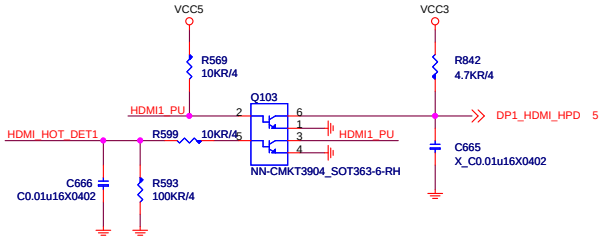
For HDMI 1.4



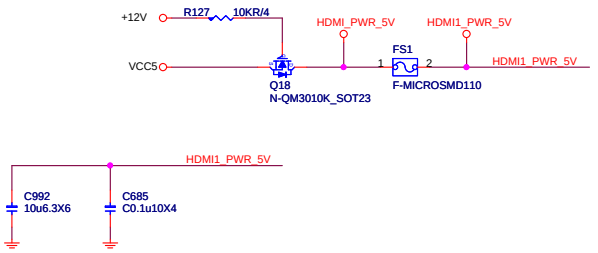
AUX Level Shifter



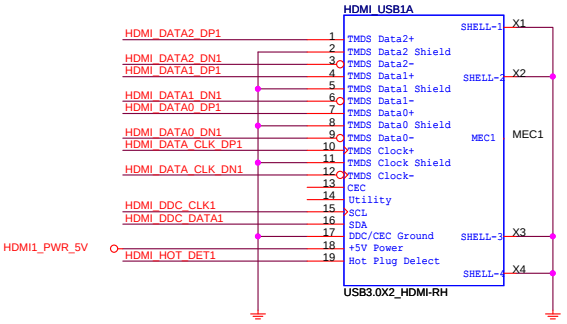
HPD Circuit



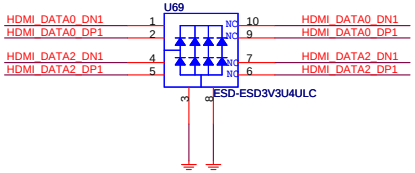
Connector Power

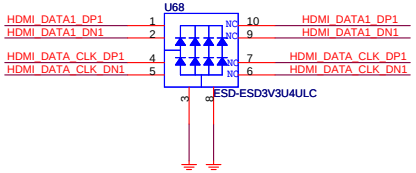


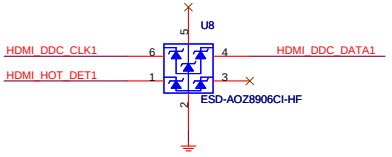
Connector

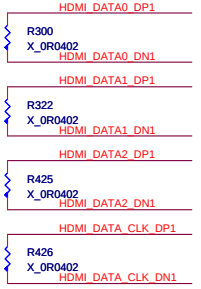


For EMI









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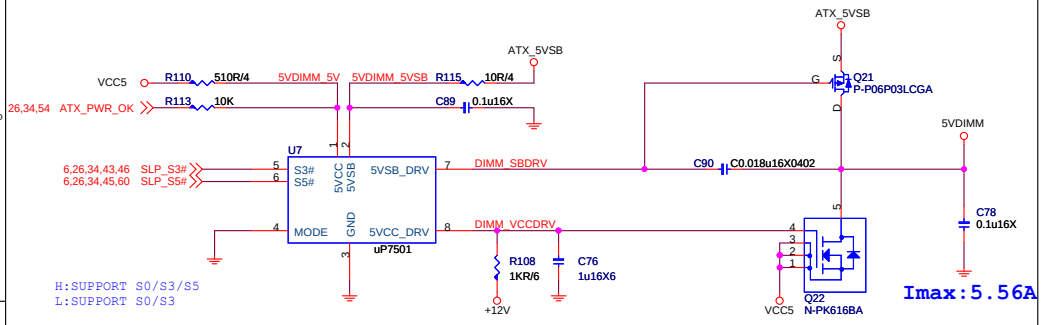
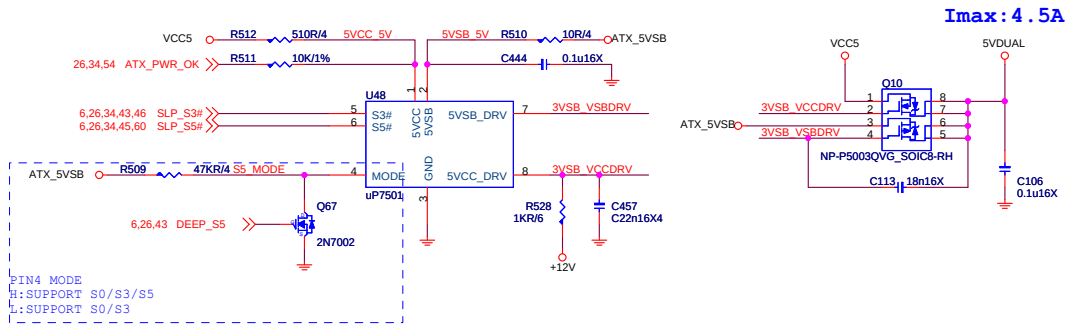
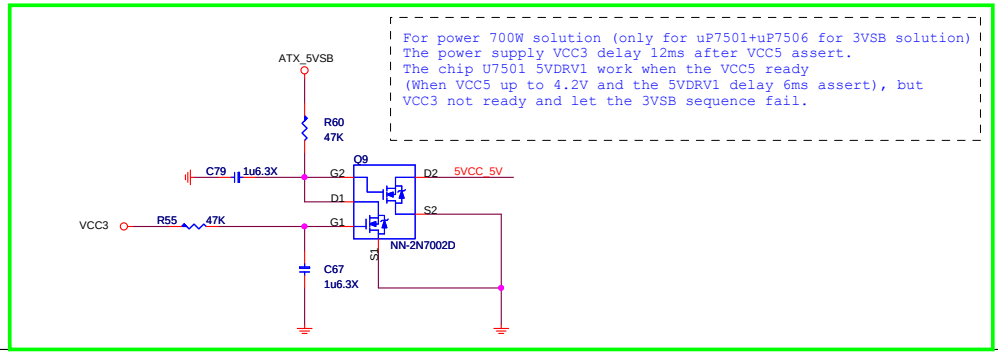
5VDIMM FOR DDR

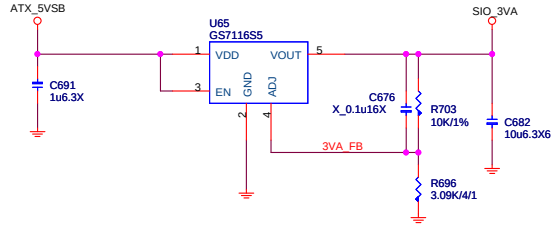


5VDUAL For 3VSB CPU 1.8V VDDP

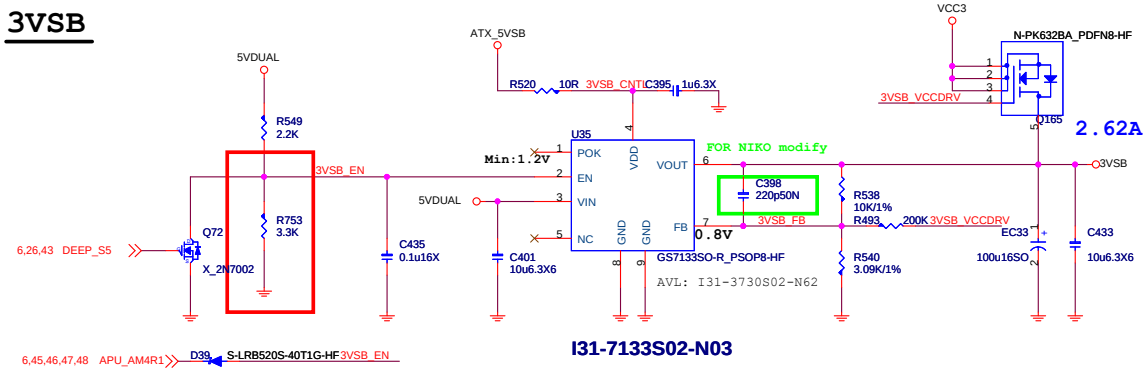


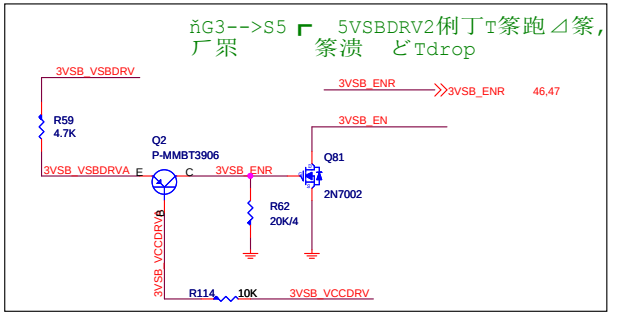


SIO_3VA



3VSB





MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: ACPI uPI-5VDIMM&3VSB	Rev: 10
Date: Tuesday, January 24, 2017	Sheet 42 of 65	

FOR Promontory 1.05V_S0

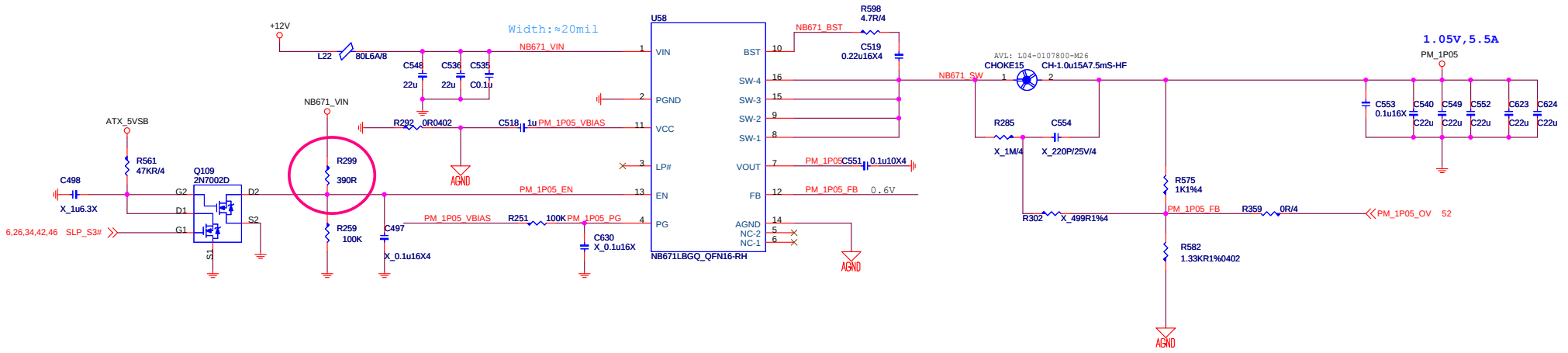
1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

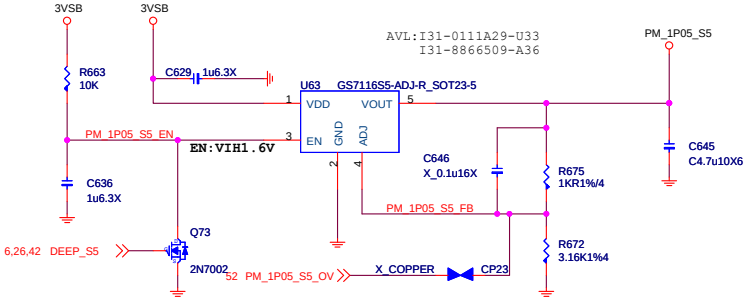
0.7776uH≦L≦1.1664uH

F:500K



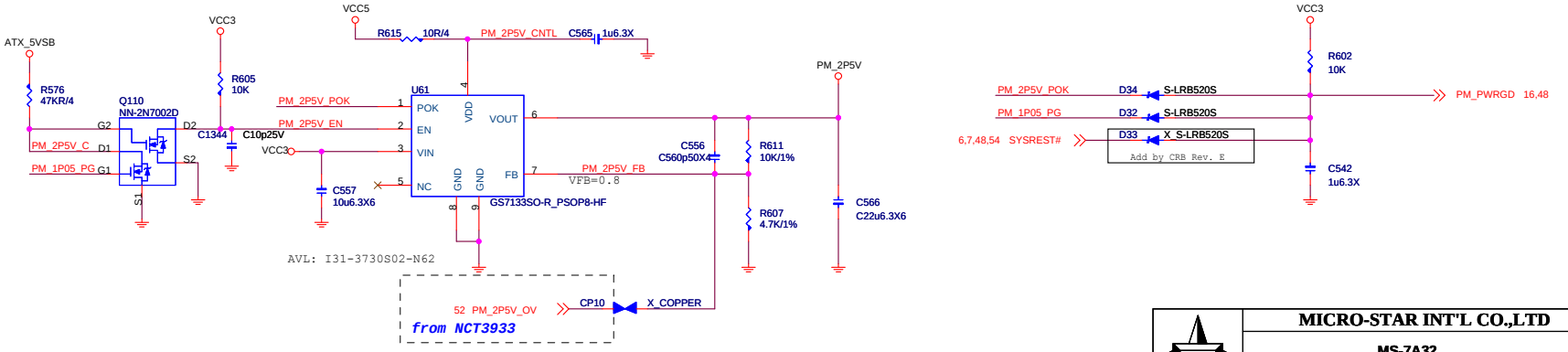
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA



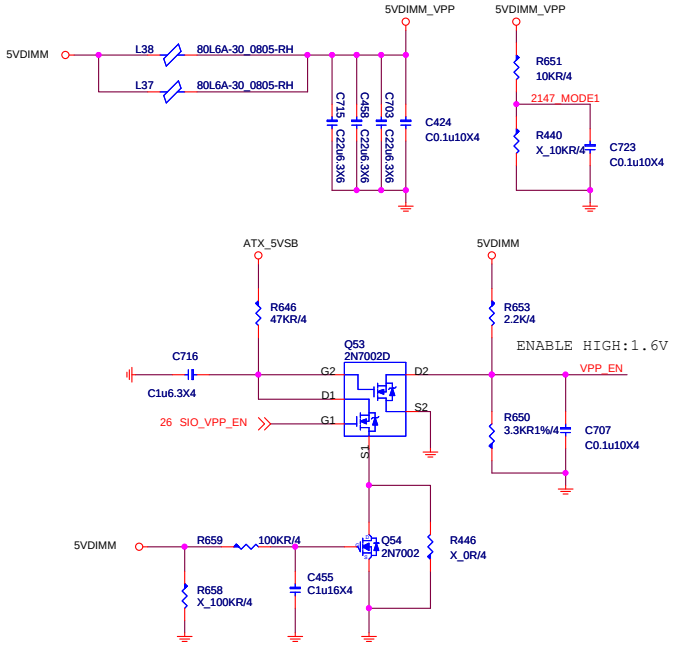
MICRO-STAR INT'L CO.,LTD

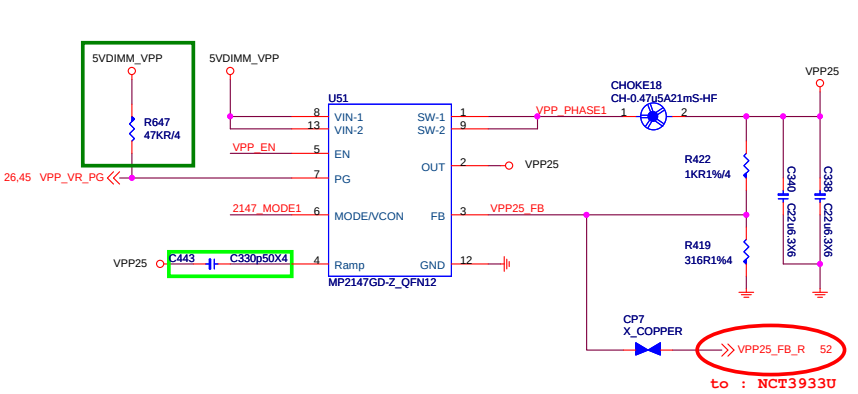
MS-7A32

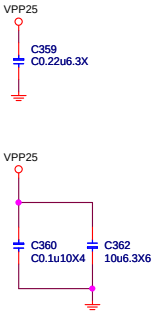
Size	Document Description	Rev
Custom	PM-NB681GD-1.05V/GS7133-2.5V	10

Date: Tuesday, January 24, 2017 Sheet 43 of 65

4DIMM :2.24A FOR DDR VPP2.5V

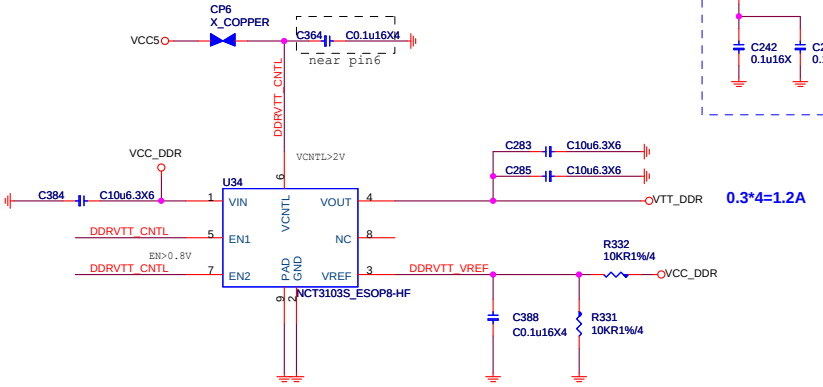


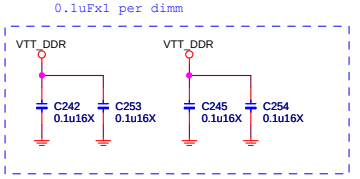


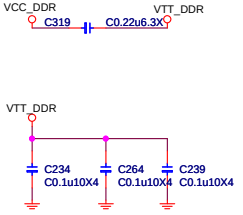


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .







MICRO-STAR INT'L CO.,LTD	
MS-7A32	
Size: Custom	Document Description: DDR PWR VPP25/VTT-MP2147
Rev: 10	
Date: Tuesday, January 24, 2017	Sheet 44 of 65

DDR4_1.2V 15.5A+9.5A+1.2A=26.2A

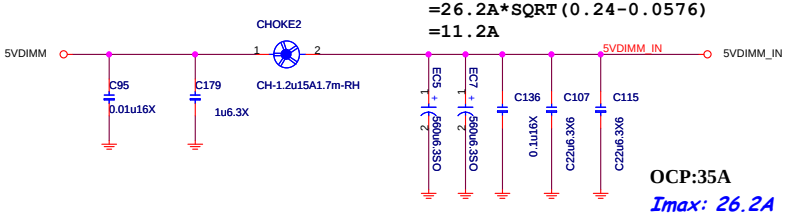
15.5A FOR CPU

9.5A FOR 2DIMM

1.2A FOR DDR VTT

VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=26.2A*SQRT(0.24-0.0576)
=11.2A



OCP:35A

Imax: 26.2A

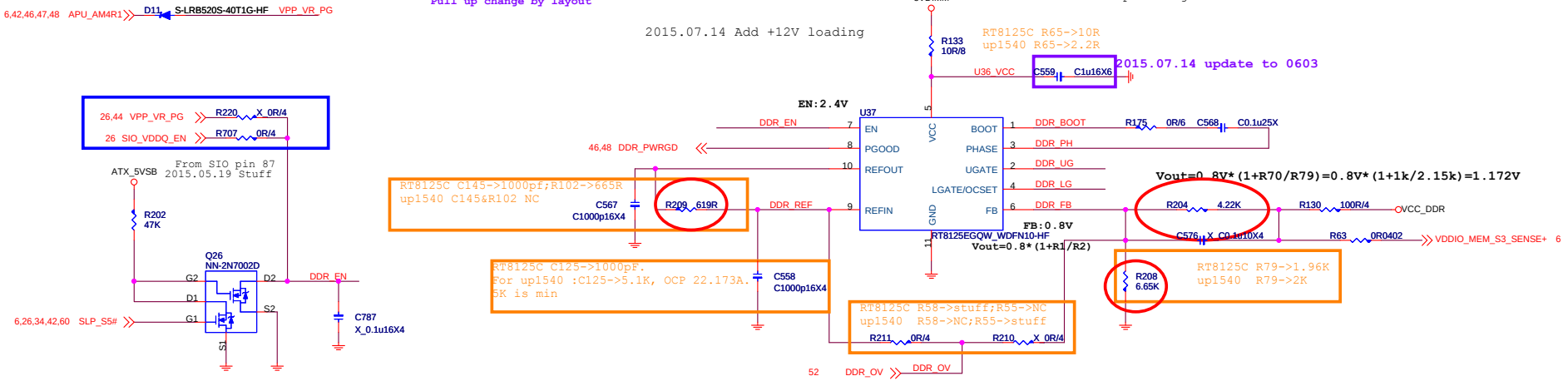
20151230 Update

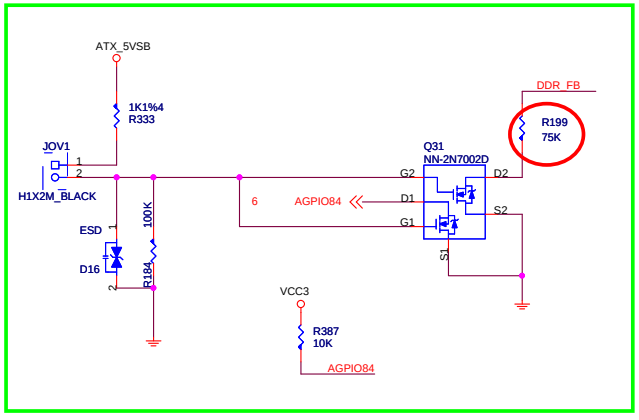
uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

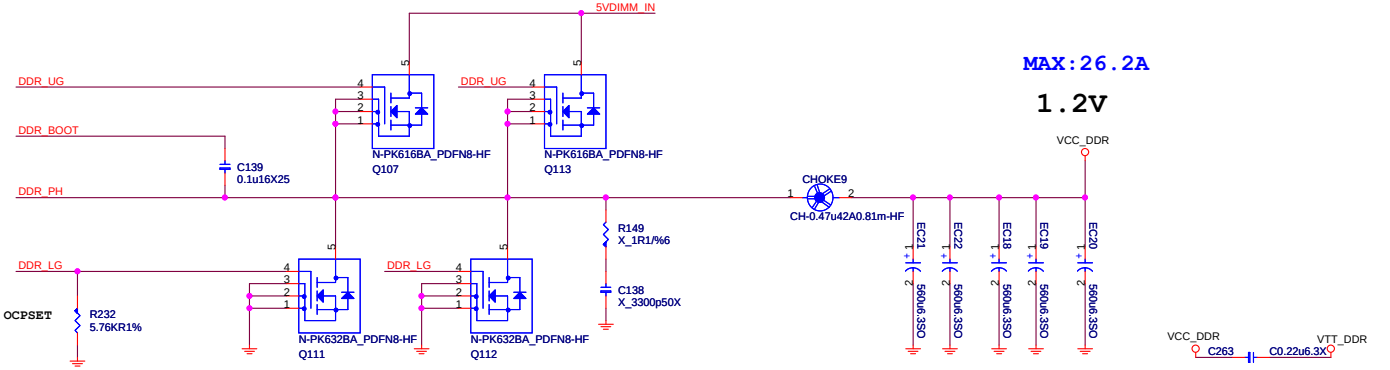
Pull up change by layout

2015.07.14 Add +12V loading

2015.07.14 update to 0603







MAX:26.2A

1.2V

OCP=35A
OCPSET:min 5Kohm
OCP
=(R232*10uA)/Rdson
=R232*10uA)/3.3m/2
=35A

R232=5.775k

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

MICRO-STAR INT'L CO.,LTD

MS-7A32

Size	Document Description	Rev
Custom	DDR Power-RT8125E	10

Date: Tuesday, January 24, 2017 Sheet 45 of 65

FOR CPU 1.8V S5

0.5A

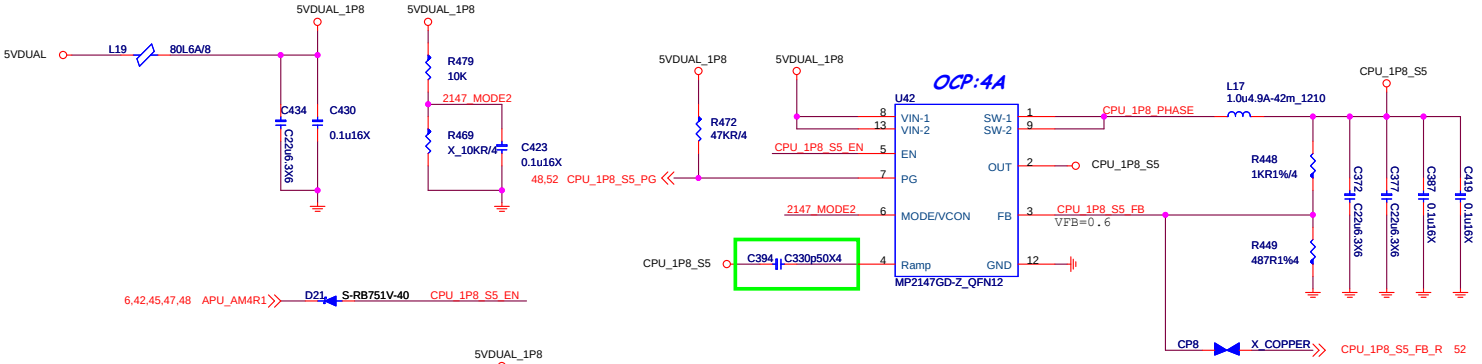
FOR VCCP_SOC_S5

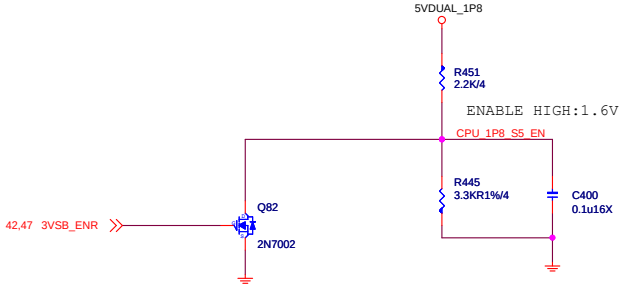
0.9A

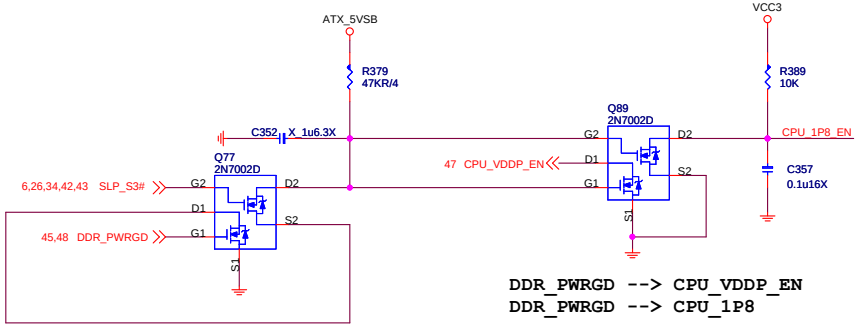
FOR CPU 1.8V S0

2.0A

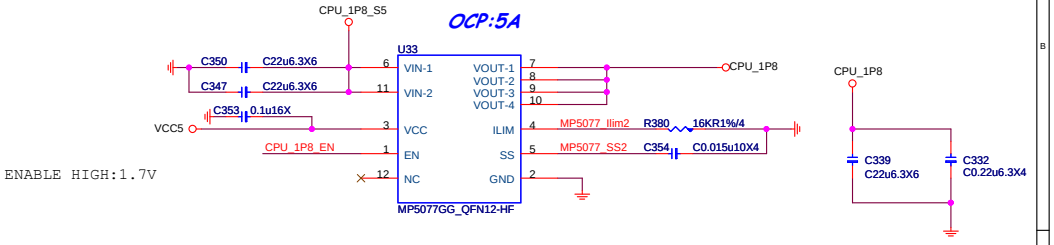
0.5A + 2.0A + 0.9A =3.4A







DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS

MICRO-STAR INT'L CO.,LTD		
MS-7A32		
Size: Custom	Document Description: CPU Power 1P8V-MP2147	Rev: 10
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CPU_VDDP_S0

1.05V/0.9
S0:8.5A

by layout

+12V

R406 100K1%4 EN:VIH1.6V

CPU_VDDP_EN

R418 33K/1%

C389 0.1u16X

VCC5

R437 10K

48 CPU_VDDP_PG

6,42,45,46,48 APU_AM4R1

D20 S-LRB520S

CPU_VDDP_EN

EN:VIH1.6V
EN pin Maximum:6.5V

U41

EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB

RT8125EGQW_WDFN10-HF

CPU_VDDP_REFOUT

C426 C1000p50X4

R453 768R1%4

CPU_VDDP_REFIN

C374 C1000p50X4

0.8V
0.684V

R463 4.53KR1%4

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

Q86 NN-2N7002DW

6,35,48,52 TYPE1_CPU_SEL

16 PM_GPIO_R9

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

52 CPU_VDDP_OV

CP25 X_COPPER

by layout

+12V

R494 10R/8

U6_VCC C429 C1u16X6

CPU_VDDP_BOOT1 R484 0R/6 C440 0.1u16X25

CPU_VDDP_PH1

CPU_VDDP_UG1

CPU_VDDP_LG1

CPU_VDDP_FB

FB:0.8V

CPU_VDDP

R420 10R1%0402

R438 1KR1%/4

CPU_VDDP_SENSE_R R421 0R/4 CPU_VDDP_SENSE 6

C399 X_0.1u16X

R450 3.16K/1%

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 8.5*0.2823
= 2.4A

3VSB

1K1%4 R339

R212 2.26KR1%0402

JOV2 H1X2M_BLACK

26 SIO_GP10

Q149 2N7002

ESD D17

R195 100K

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2

CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

Q92 NN-2N7002DW

6,48 TYPE0_CPU_SEL

VDDP_SEL

6,35,48,52 TYPE1_CPU_SEL

CPU_VDDP_EN CPU_VDDP_EN 46

VDDP_SEL

TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

12VCC_IN

CHOKE14 CH-0.47u5A21mS-HF

+12V

C461 C1u16X6

C460 22u16X8

EC11 270u16SO

C446 0.1u16X

CPU_VDDP_UG1 R508 0R/6 CPU_VDDP_UG1_R

R500 X_10KR/4

N-PK616BA_PDFN8-HF Q97

CPU_VDDP_PH1

CPU_VDDP_LG1

N-PK632BA_PDFN8-HF Q96

OCP=12A

OCPSET:min 5Kohm
OCP
=(R475*10uA)/Rdson
=(5.1k*10uA)/3.3m
=15.45A

R475 5.1K/1%/4

R482 X_2.2R/8

snubber

C437 X_C3300p50X4

CHOKE13 1.0u15A7.5mS-HF

CPU_VDDP

C334 1u6.3X

C425 C22u6.3X6

EC31 560u6.3SO

EC32 560u6.3SO

OCP=12A
1.05v,8.5A

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

3VSB 3VSB

5VDUAL

L20 80L6A/8

R501 X_10KR/4

R502 10K

C439 C22u6.3X6

U45

VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PG

VIN
EN
PG
PGND
AGND
SW
OUT
FB

MP2143DJ

48 VDDP_VSB_PG

Internal Pull-Up 500K

VDDP_VSB_PHASE

L18 1.0u5.5A-35_1210-HF

CPU_VDDP_S5

R489 1KR1%/4

R488 2KR1%/4

C412 C22u6.3X6

C421 C22u6.3X6

C427 C0.22u6.3X4

VDDP_VSB_FB

6,42,45,46,48 APU_AM4R1

D28 S-LRB520S

VDDP_VSB_EN

C390 X_0.1u16X

42,46 3VSB_ENR

Q98 2N7002

ATX_5VSB

R490 47KR/4

Q95 NN-2N7002DW

C436 0.1u16X

6,35,48,52 TYPE1_CPU_SEL

AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

R464 3.83KR1%4

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

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MS-7A32

Size: Custom

Document Description: CPU Power VDDP-RT8125E

Rev: 10

Date: Tuesday, January 24, 2017

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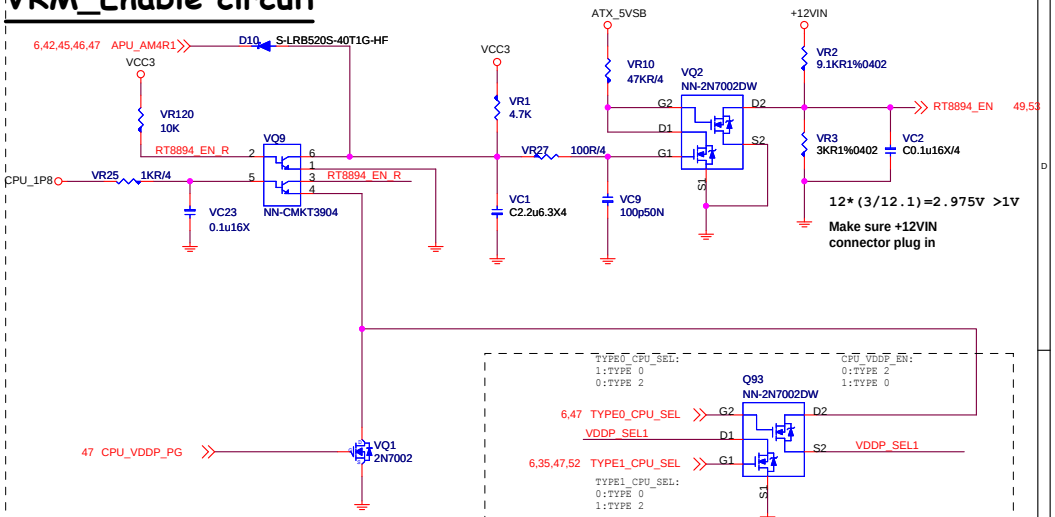
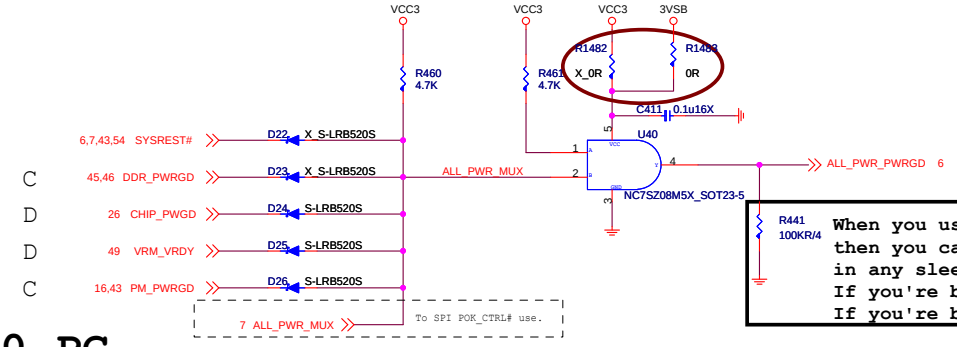
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

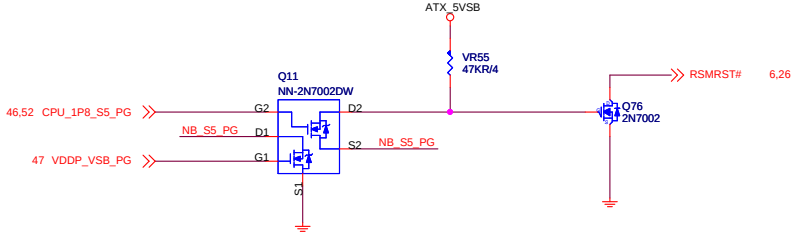


R441 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MICRO-STAR INT'L CO.,LTD

MS-7A32

Size	Document Description	Rev
Custom	CPU Power Connector/PWRGD	10

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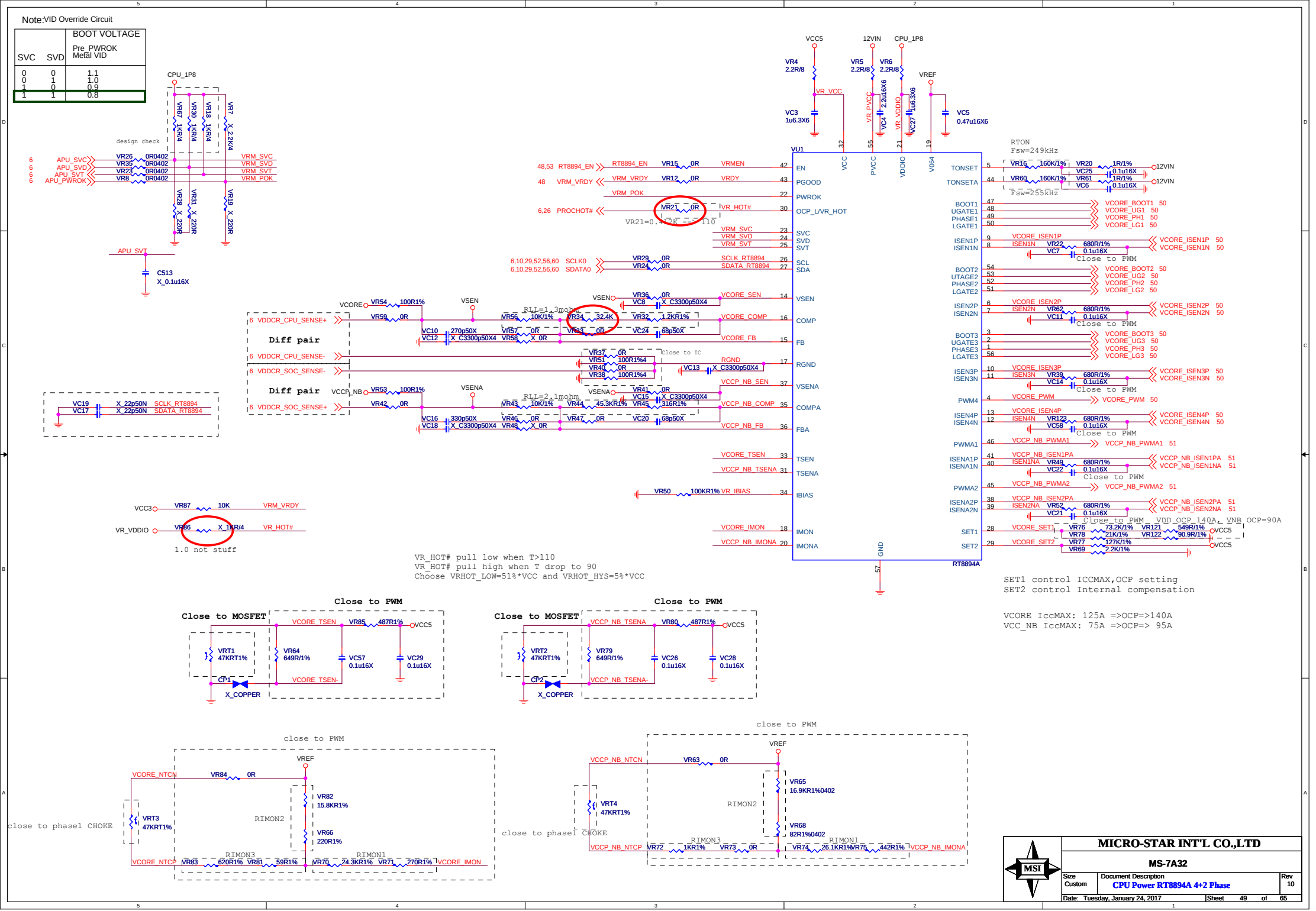
Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



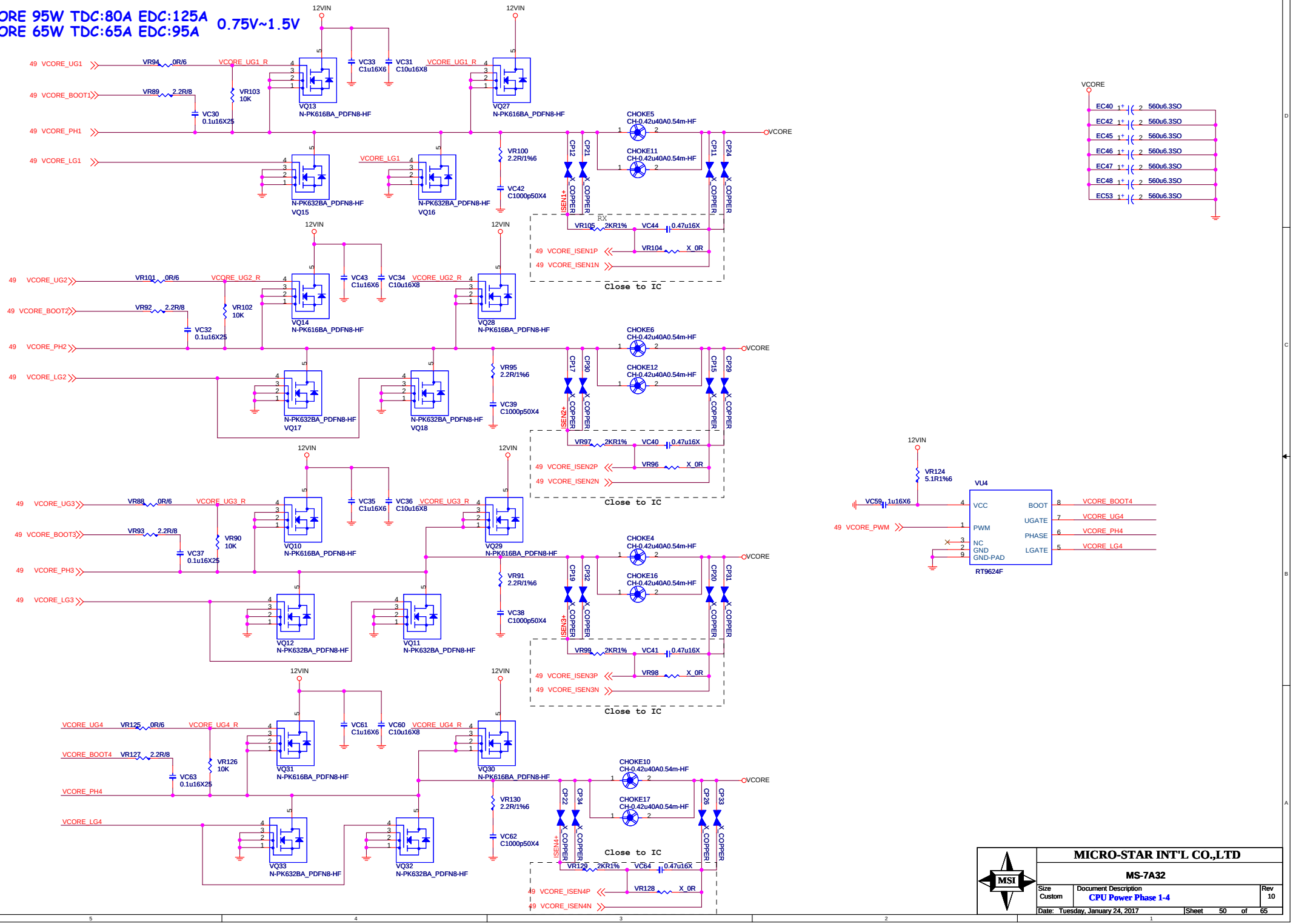
MICRO-STAR INT'L CO.,LTD

MS-7A32

Size	Document Description	Rev
Custom	CPU Power RT8894A 4+2 Phase	10

Date: Tuesday, January 24, 2017 Sheet 49 of 65

VCORE 95W TDC:80A EDC:125A 0.75V~1.5V
VCORE 65W TDC:65A EDC:95A



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power Phase 1-4	10

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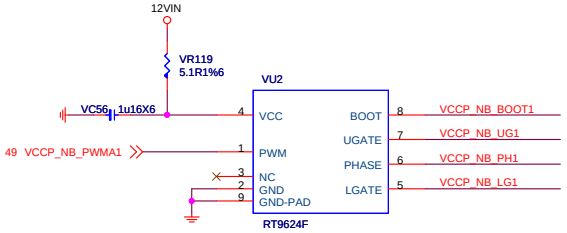
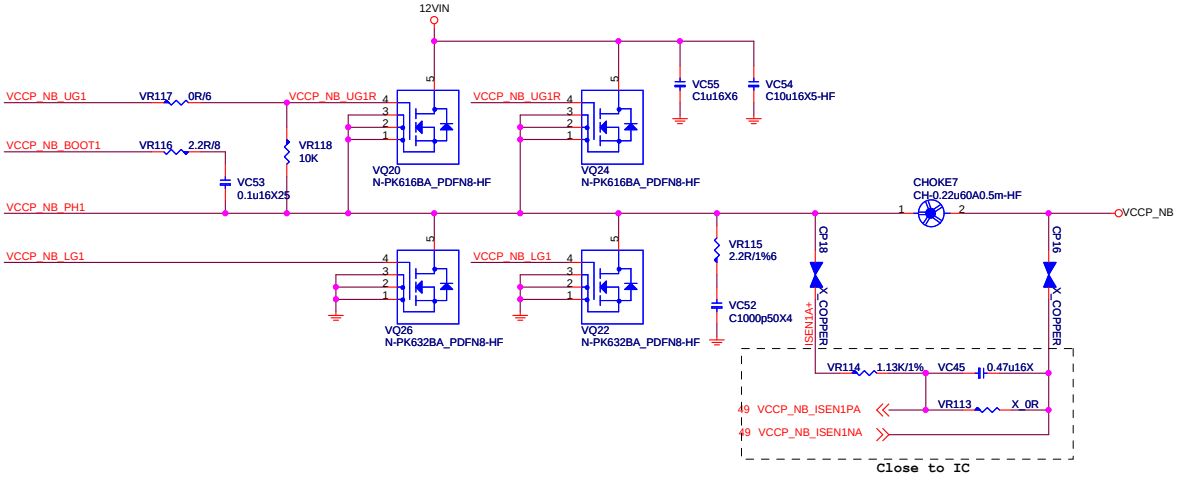
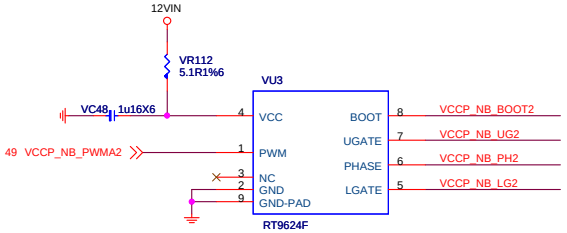
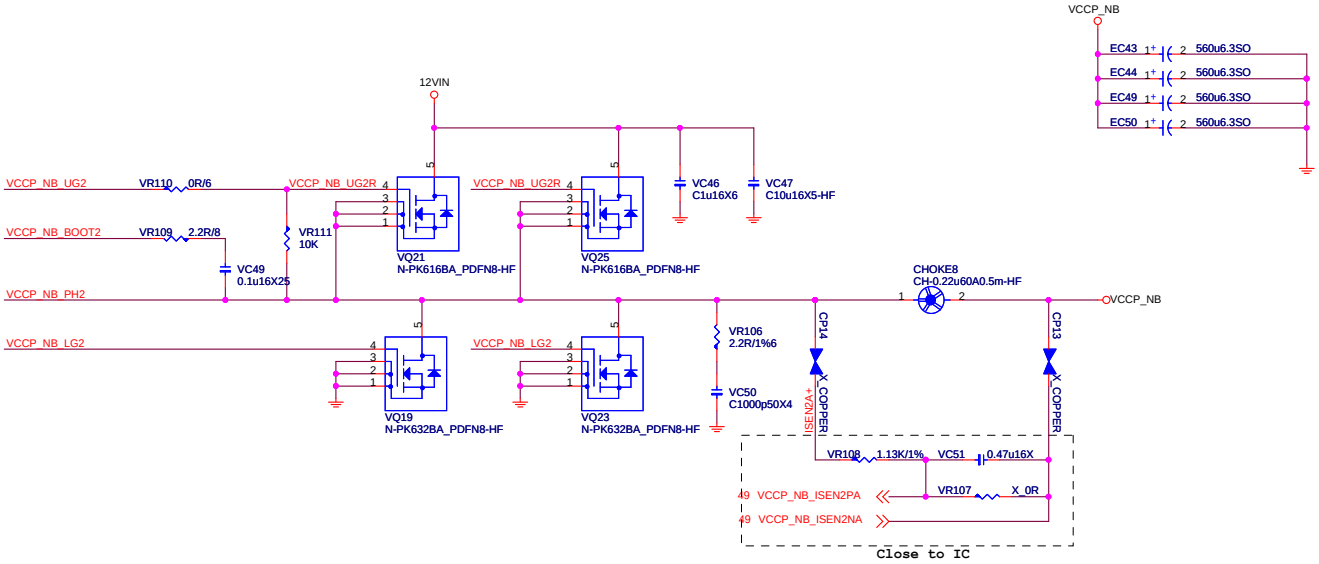
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

0.75V~1..2V









MICRO-STAR INT'L CO.,LTD

MS-7A32

Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	10

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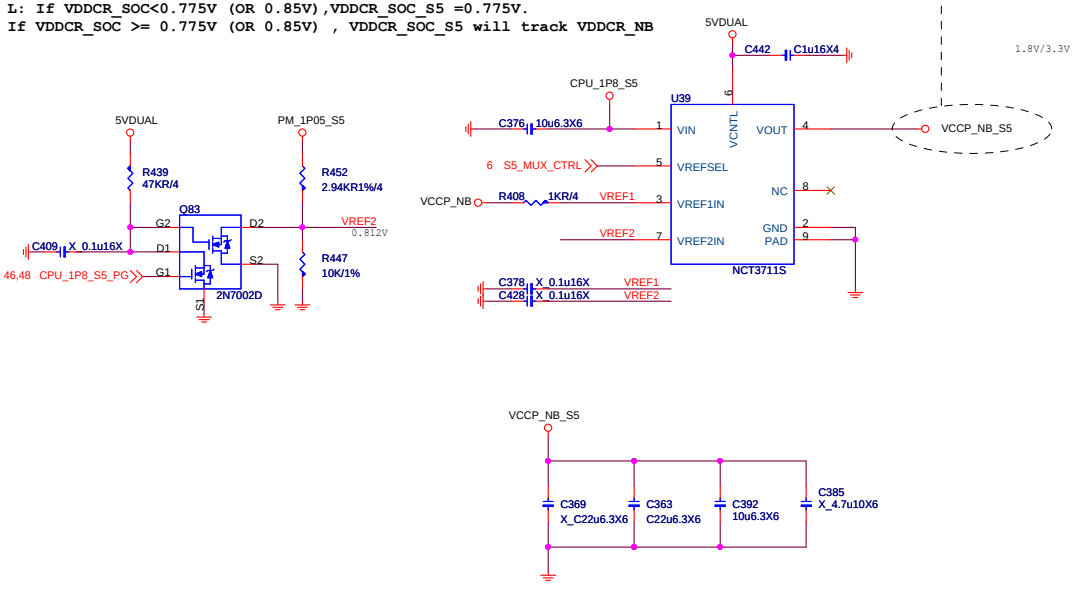
FOR VCCP_SOC_s5
0.9A

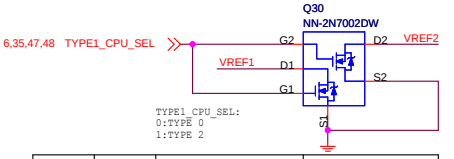
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0





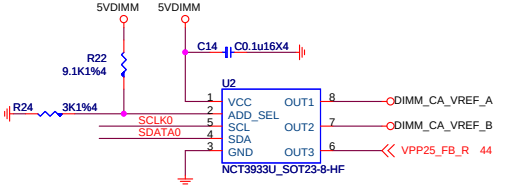
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

埃獲禡溃癸　　Tヴ：腊　，　玥ぃ　NCT3933籔秤禡溃匡兜

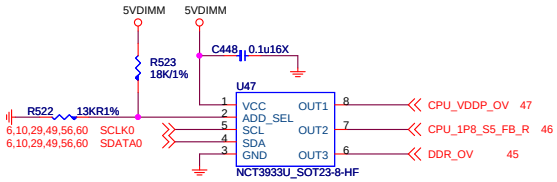
0x28:RH=9.1K,RL=3K



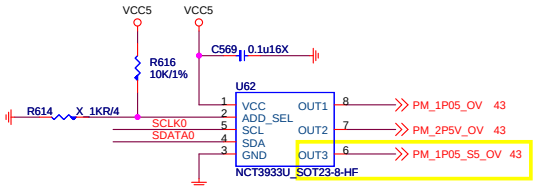
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

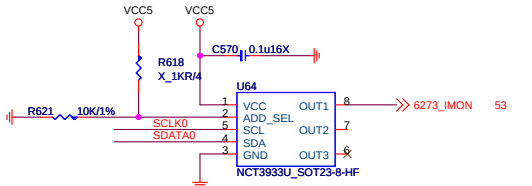
0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



0x2A:RH=OPEN,RL=10K



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power NB Switch/NCT3933	10

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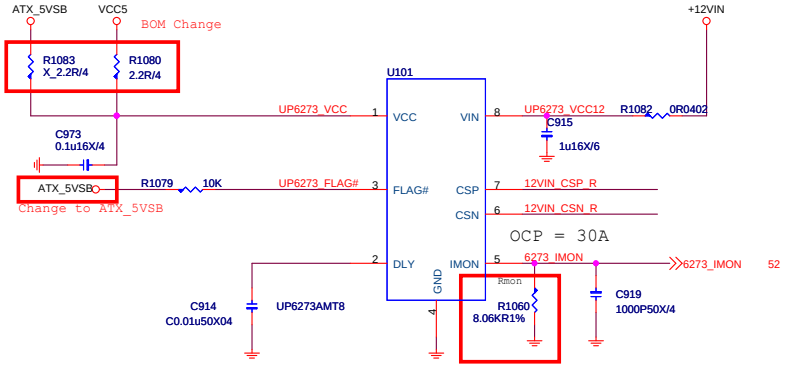
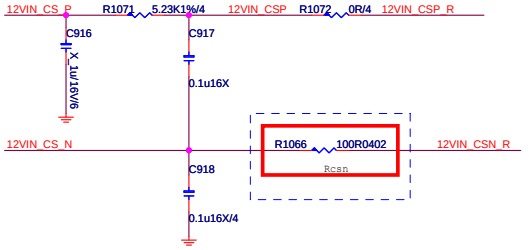
uP6273 CURRENT SENSE

VCORE EDC MAC 125A

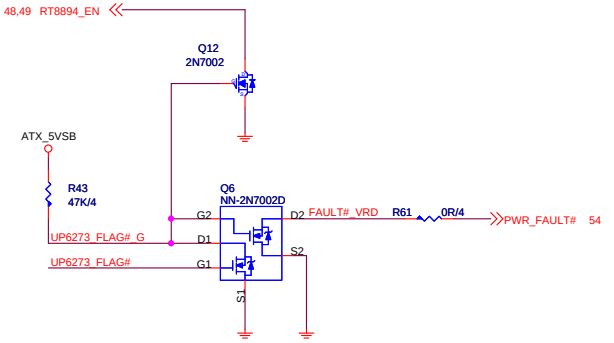
NB EDC MAX75A



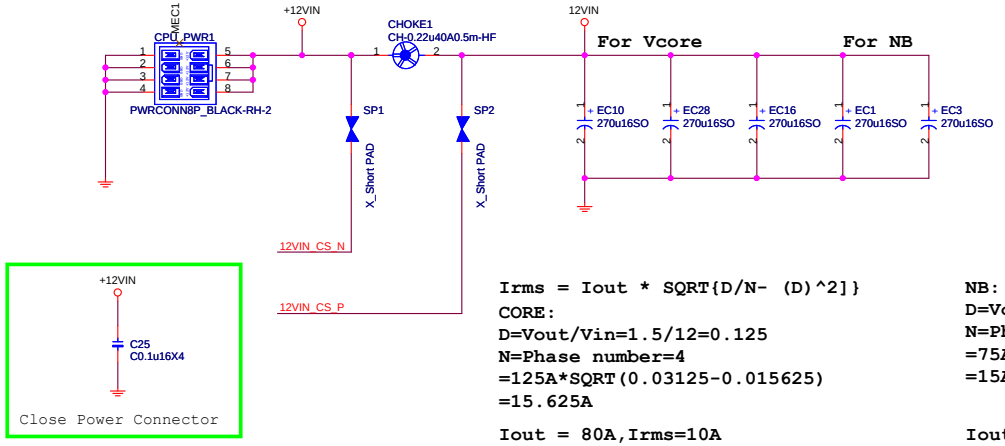
Vmon = 1.2V觸發ocp
Vmon=(Iin x Rdc / Rcsn) x Rmon
1.2V=30 x 0.5m /100 x Rmon
Rmon=8K



Imon= 10uA = Vin 2A (NCT3933一階做2A拓展)
Iin x Rdc /Rcsn = Imon
2A x 0.5m / Rcsn = 10uA
Rcsn=100 ohm



CPU POWER CONNECTOR



Irms = Iout * SQRT{D/N- (D)^2]}
CORE:
D=Vout/Vin=1.5/12=0.125
N=Phase number=4
=125A*SQRT(0.03125-0.015625)
=15.625A

Iout = 80A,Irms=10A

NB:
D=Vout/Vin=1.2/12=0.1
N=Phase number=2
=75A*SQRT(0.05-0.01)
=15A

Iout = 50A,Irms=10A

uP6273 CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	UP6273 CURRENT SENSE	10

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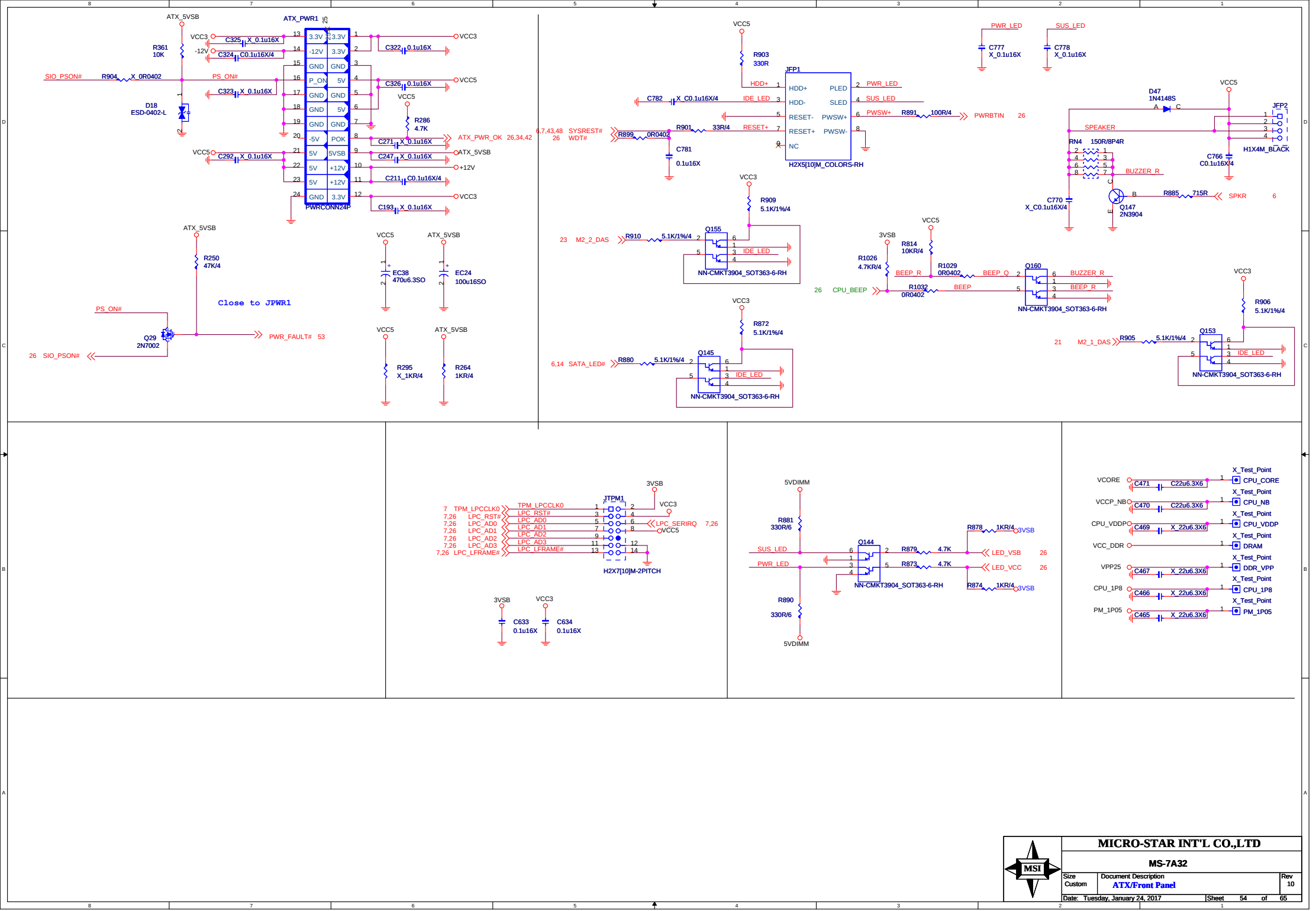

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ATX/Front Panel	10

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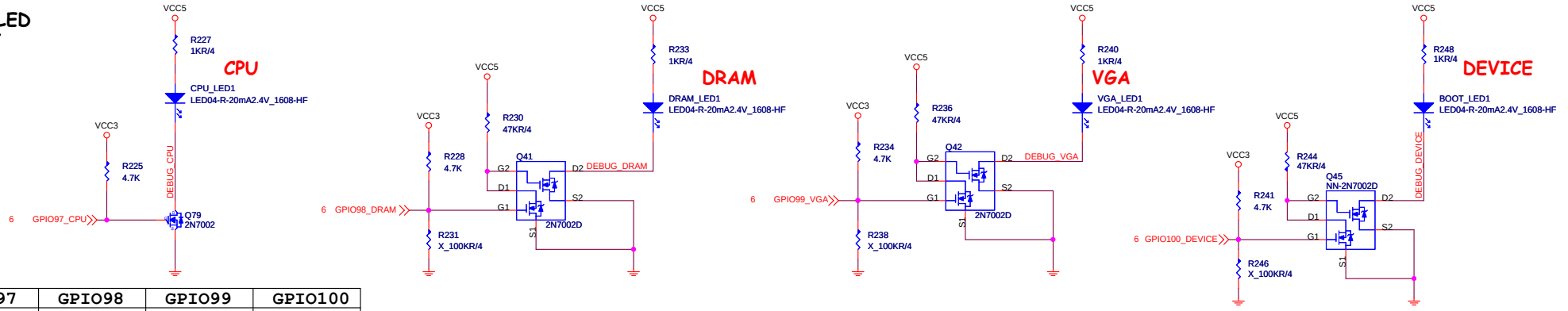
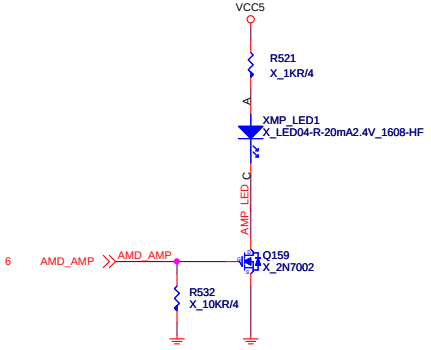
EZ Debug LED



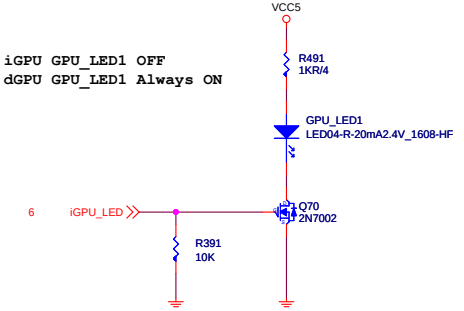
LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獨	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED



AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
獨	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

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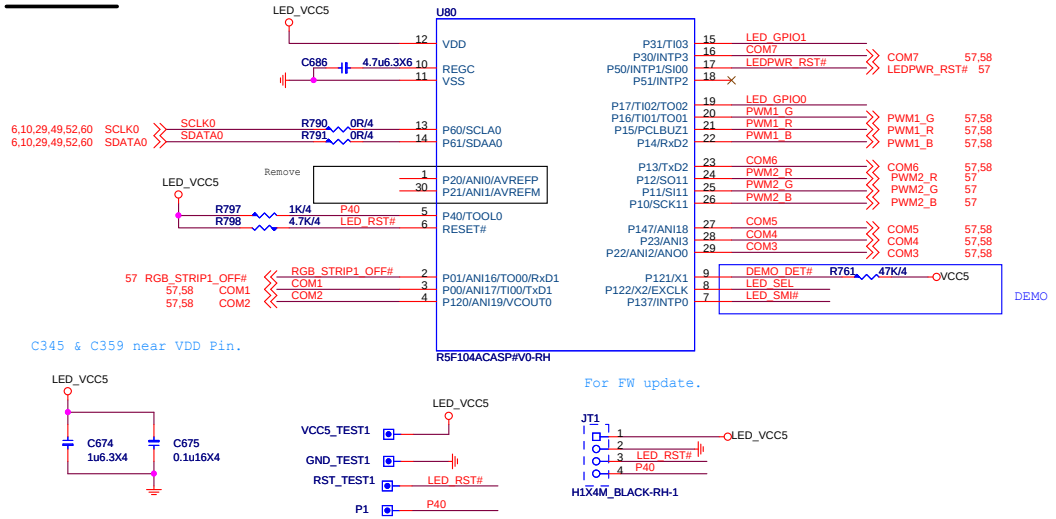
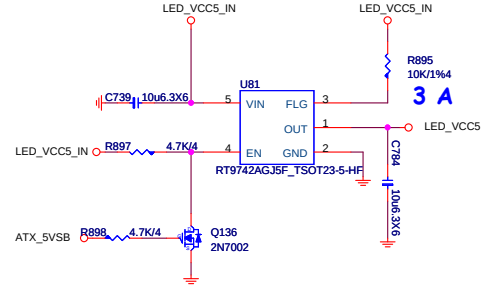
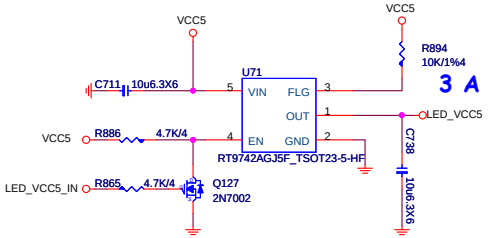
LED MCU



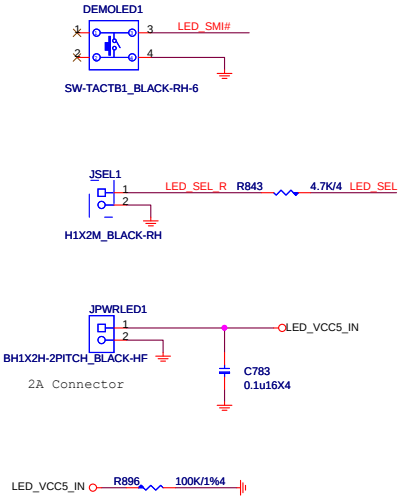
Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~7	PWM1	RGB LED
Board Side LED	COM1~7	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
IO Cover	LED_GPIO0	No Use	JPIPE_LED1

EXTERNAL POWER INPUT



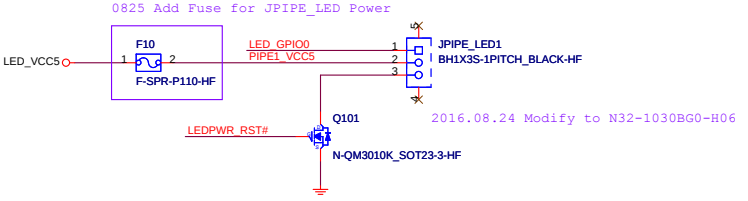


LED Demo Button



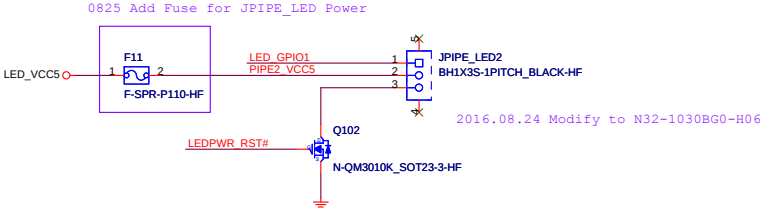
Cover LED

6PCS LED*0.16W=0.96W



HEATSINK LED

9PCS LED*0.16W=1.44W



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Custom	LED MCU Control	10

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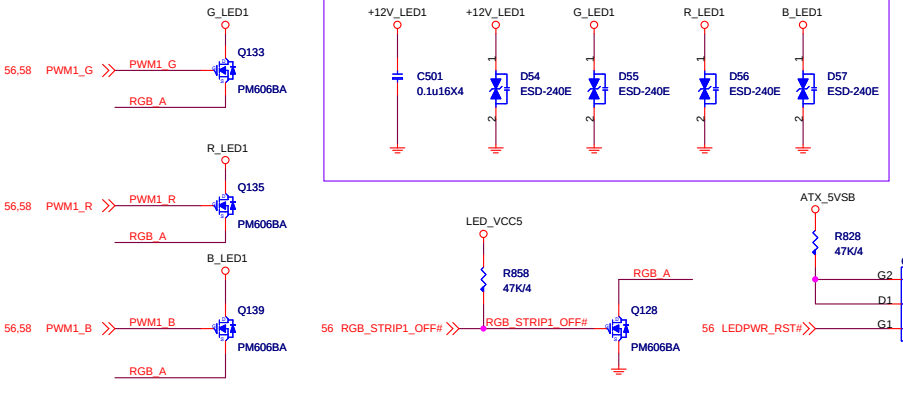
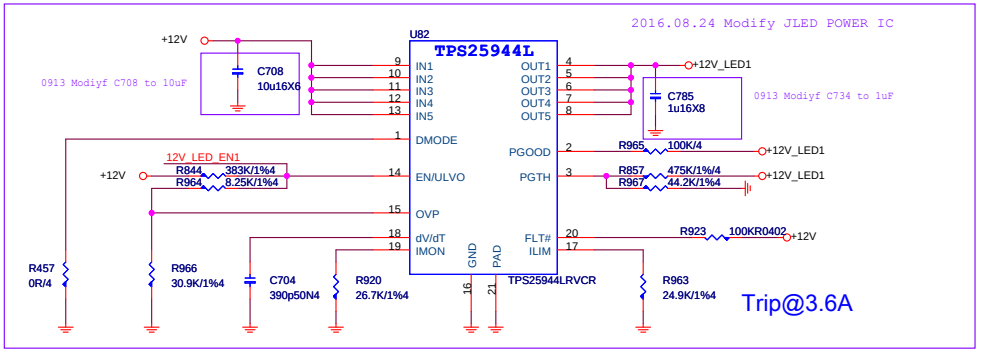
LED STRIPLINE(LEFT)

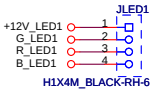
2016.08.24 Add,Close to JLED1



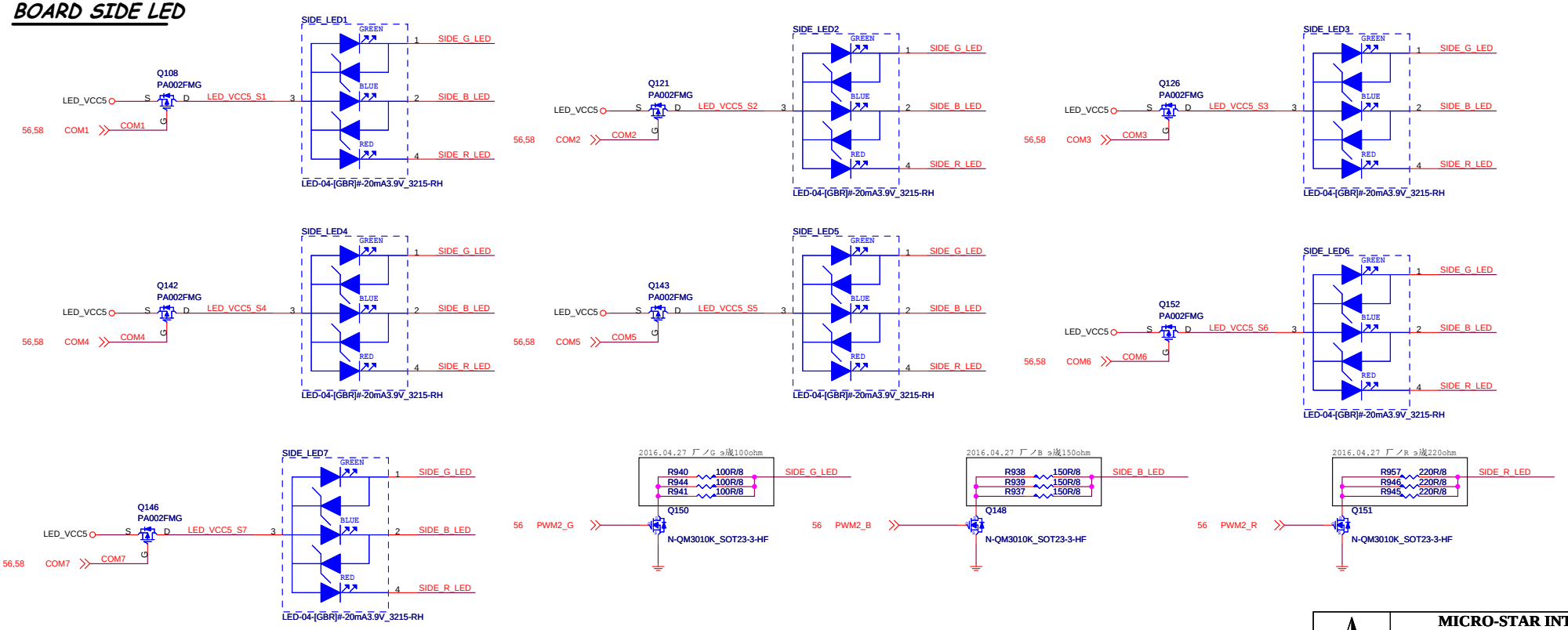
2016.08.24 Modify JLED POWER IC



钡LED 縊兵 （RGB ）
---- PCB ゅ 瑛 (JLED1)
---- も 爹 RGB 钡纔や穿夹非 5050 RGB LED 縊兵 (12V/G/R/B) , 縊兵罷块 篆琛綜 成3 蚌 (12 ヱ疢) , 塌芊綜 成2そへ (沅7A20喷靡)



BOARD SIDE LED



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Size: Custom	Document Description: LED STRIPLINE
Rev: 10	
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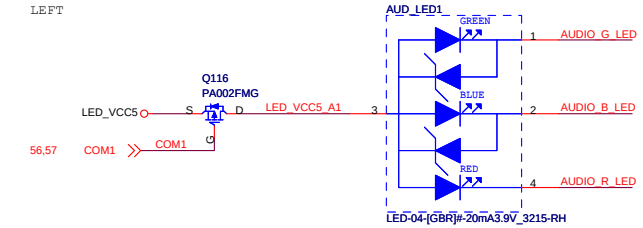
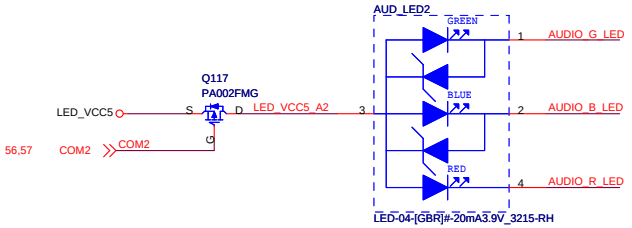
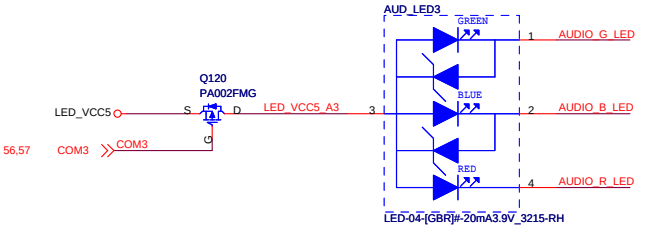
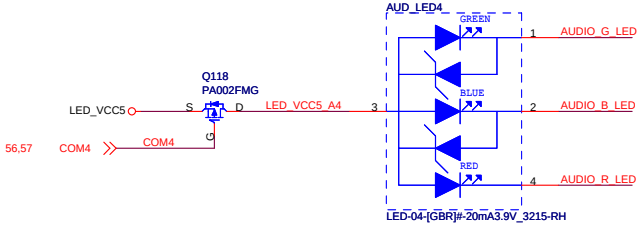
AUDIO_MOAT LED

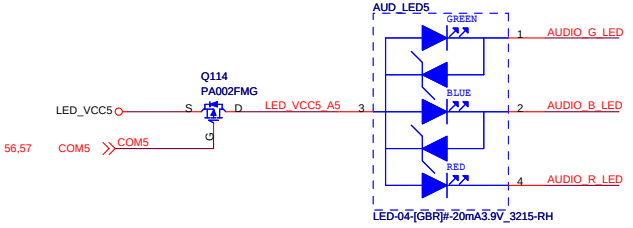
LEFT

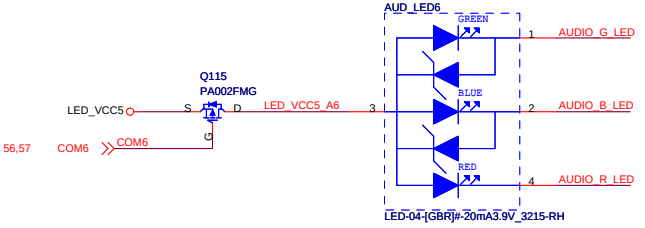


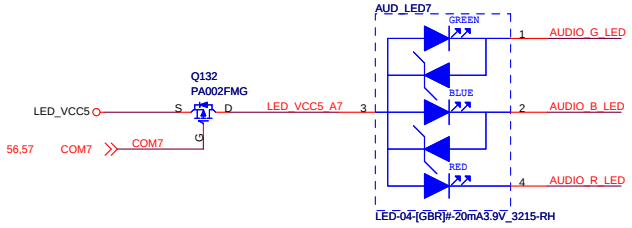


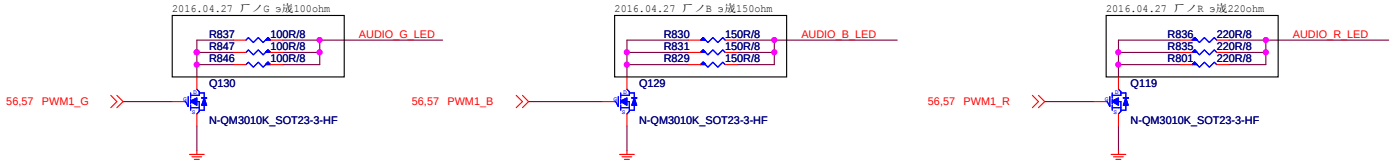












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Custom	LED AUDIO	10

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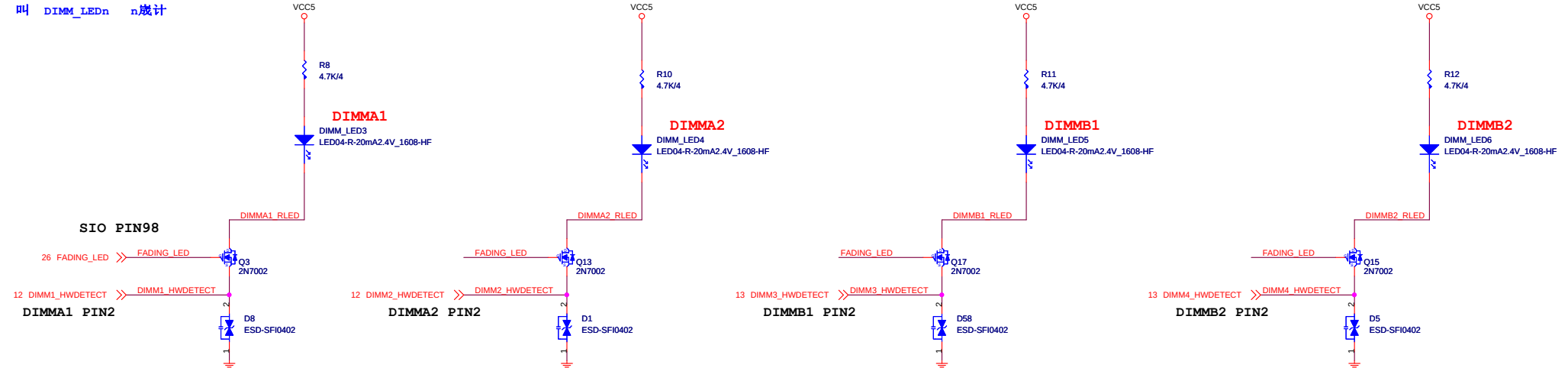
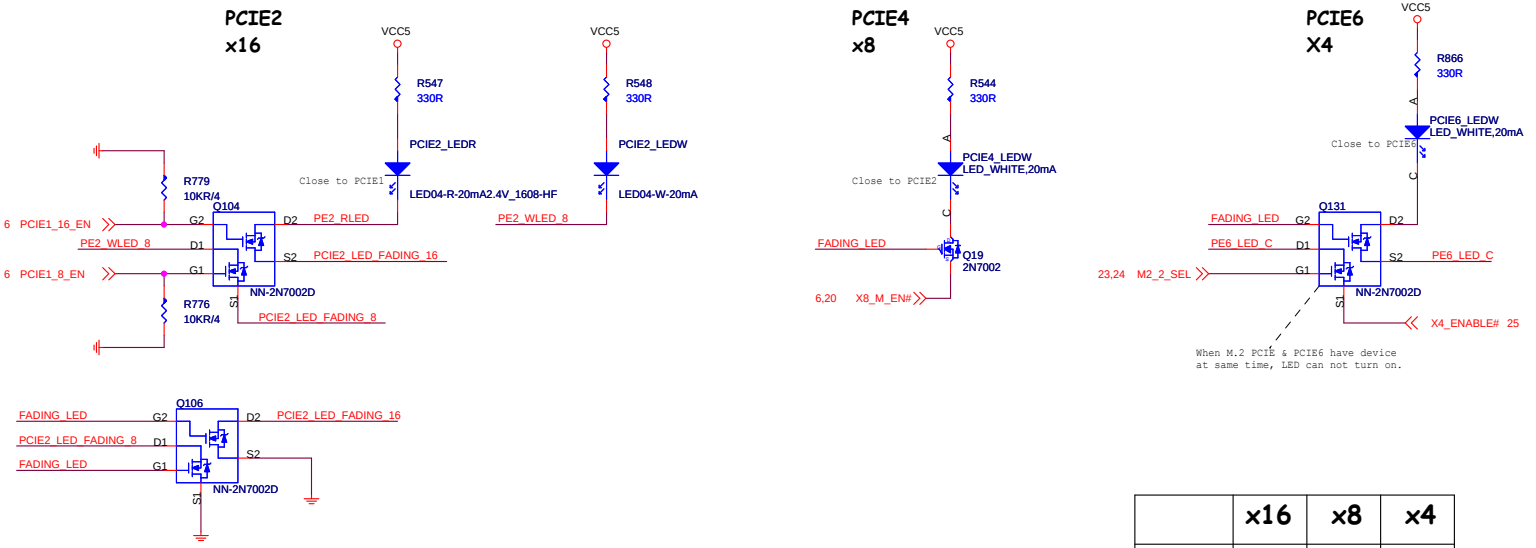
DIMM_SLOT

朗 ： D0C-040S500-E07

LED ln 叫 DIMM_LEDn n成计



PCIE SLOT LED



	x16	x8	x4
PCIE1	Red	X	X
PCIE4	X	White	X
PCIE6	X	X	White

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Custom	LED DIMM/PCIE	10

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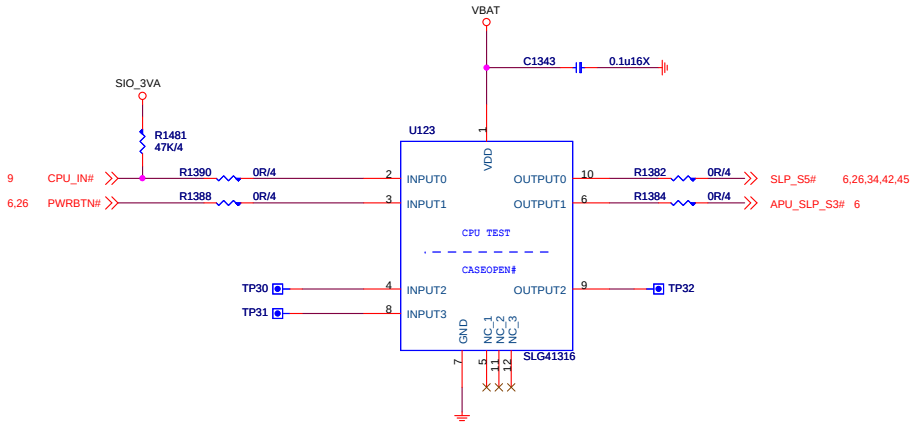
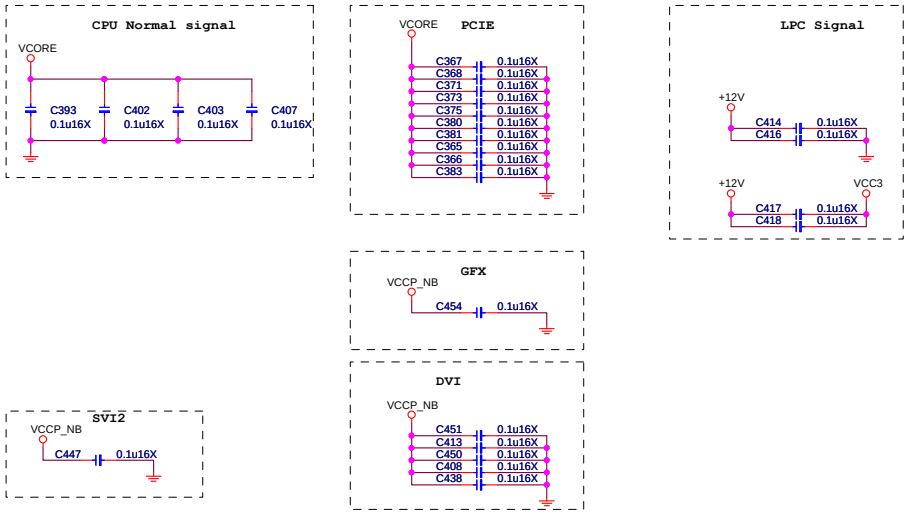
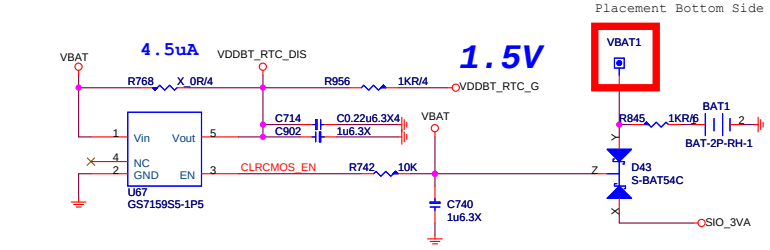
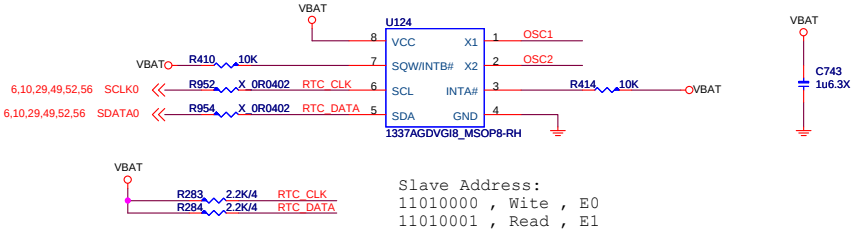


Moat Cap

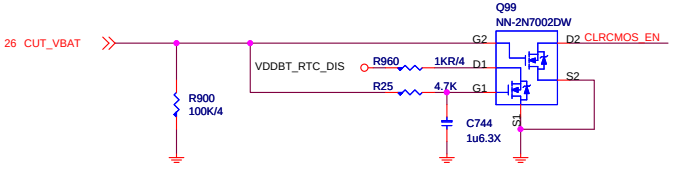


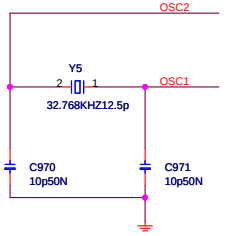
RTC & Clear CMOS Circuit

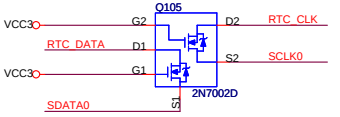


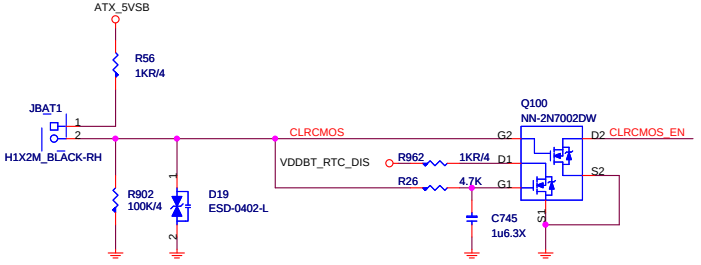


Slave Address:
11010000 , Wite , E0
11010001 , Read , E1









MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	RTC Circuit/Moat Cap	10

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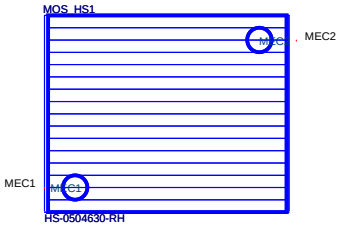
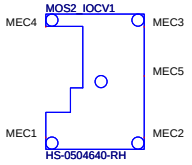
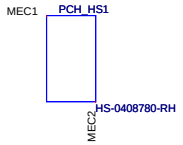
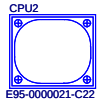
HEAT SINK





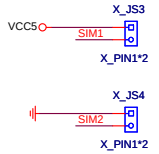


CPU Socket



RETENTION MODULE

Simulation



MANUAL PART

UEFI1
[redacted]
G51-M1SPXXA-A09

MKT1
[redacted]
G51-M1SPK31-Q13

VIRTUAL1
[redacted]
Y01-RHDMI03-000

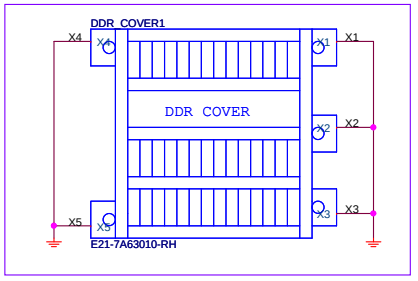
VIRTUAL2
[redacted]
Y02-MA00101-SSE

VIRTUAL3
[redacted]
Y02-MU00100-NAH

VIRTUAL4
[redacted]
Y02-MU00170-CFO

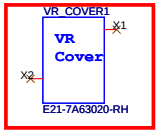
VIRTUAL5
[redacted]
Y02-MA00401-XSP

VIRTUAL6
[redacted]
Y01-RNVIDIH-000

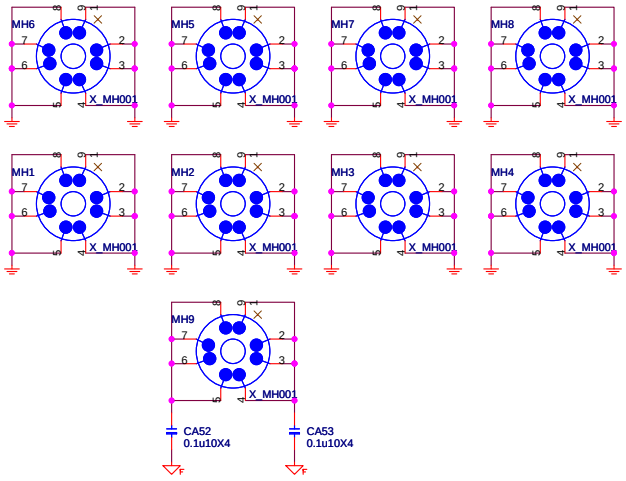


0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

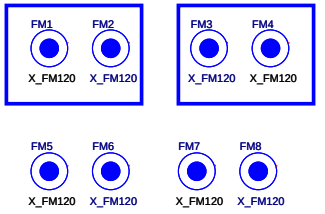
VR Cover



Optics Orientation Holes



5010 5020



OPT	Configure	BOM	Function
		601-7A32-010	XXXX

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