HuaQin Confidential

Aspire5_NB8513_M/B Schematics Document

Intel Whiskey Lake U-Processor with DDR4

REV3.0

2019-03-14

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Approver	Lobo_Fan

Huaqin Telecom Technology Com.,Ltd.

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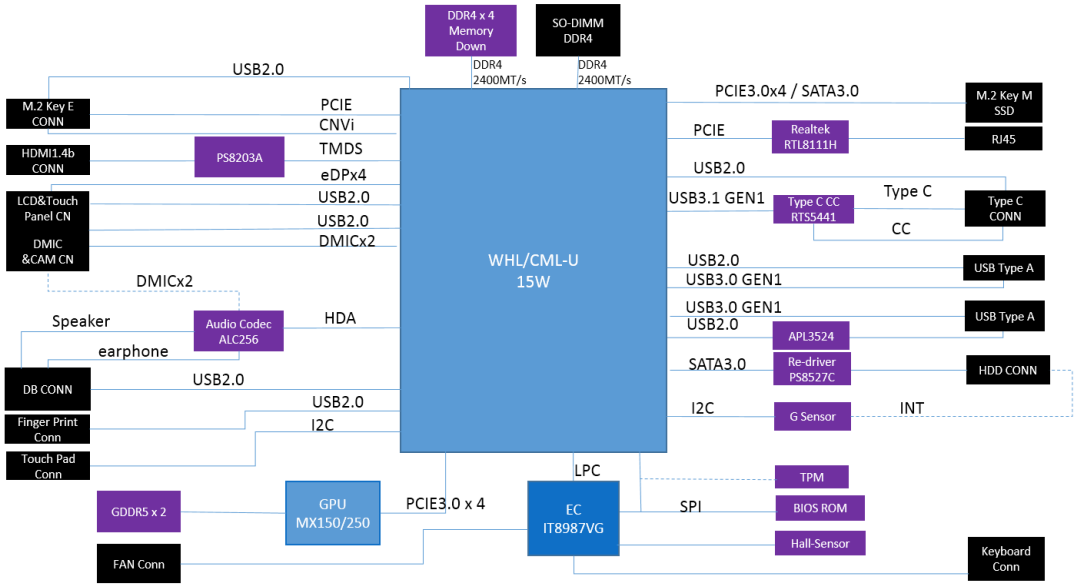
EE MB Block Diagram



Huaqin Telecom Technology Com.,Ltd.			
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MEM ID

HW_ID0	HW_ID1	HW_ID2	Description	Total
0	0	0	4x Micron 8Gbx16 MT40A512M16TB-062E:J	4GB
1	0	0	4x Micron 8Gbx16 MT40A512M16LY-075:E	4GB
0	1	0	4x Hynix 8Gbx16 H5AN8G6NCJR-VKC	4GB
1	1	0	NA	NA
0	0	1	4x 16Gb(reserve)	8GB
1	0	1	4x 16Gb(reserve)	8GB
0	1	1	4x 16Gb(reserve)	8GB

GPU ID

HW_ID3	HW_ID4		Description
0	0		UMA
1	0		N17-G0
0	1		N17-G1
1	1		N17-G2

G-sensor ID

HW_ID5	Description
0	no g-sensor
1	G-sensor on board

FP ID

HW_ID6	Description
0	no FP
1	FP on board

TPM and fTPM ID

HW_ID7	Description
0	fTPM
1	TPM

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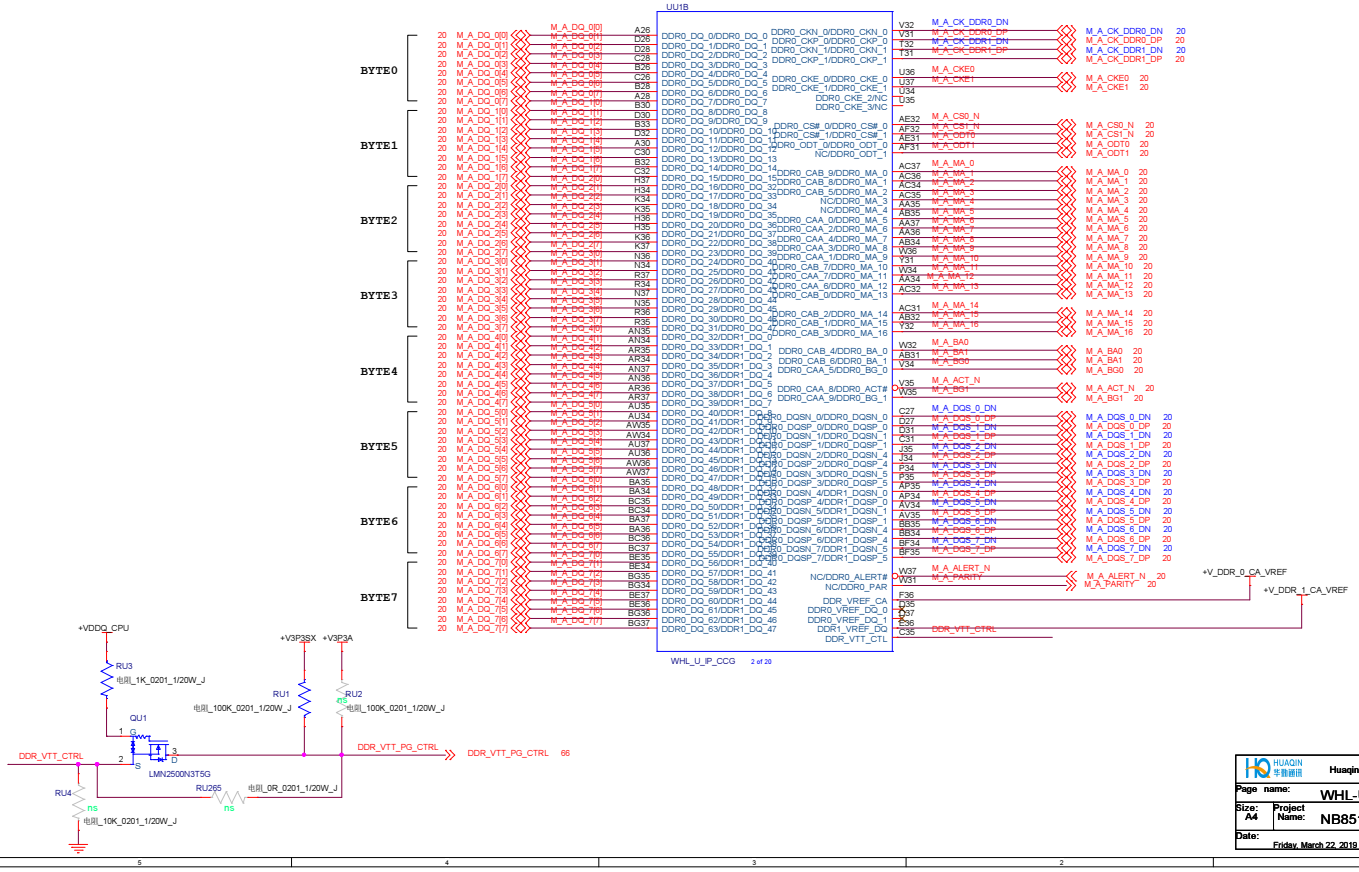
CHA_SODIMM



Huaqin Telecom Technology Com.,Ltd.	
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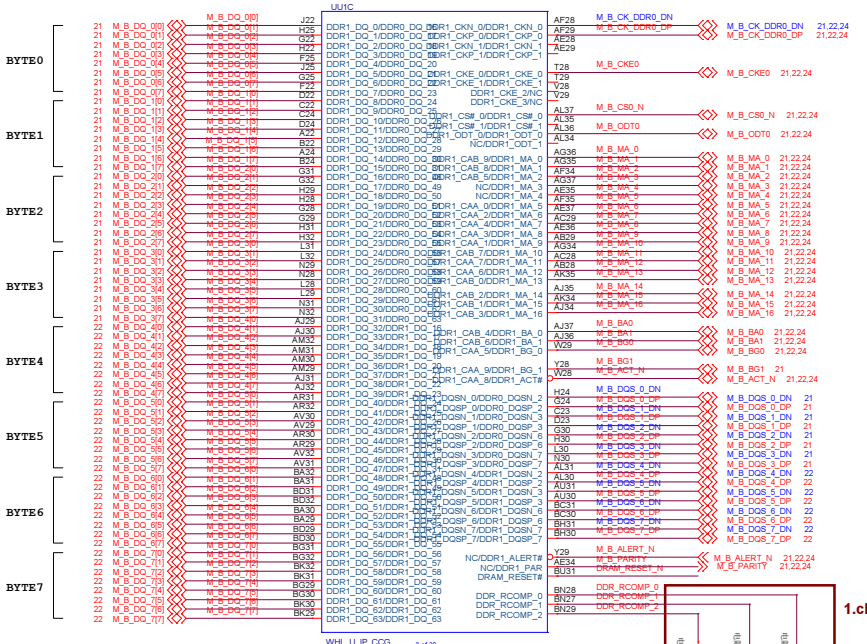
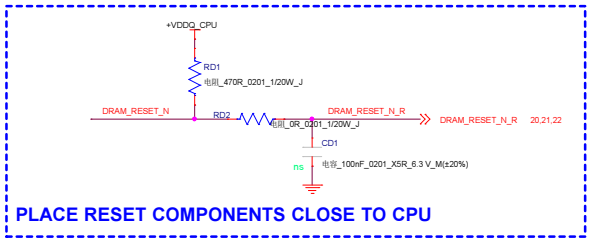
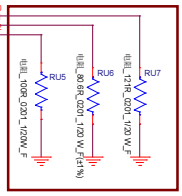
CHB_MD







1.change RU7 to 121Ω 2018 06 06

BOM NOTE

CFL-U43e/WHLU42:
[0]:121
[1]:80.6
[2]:100
CNL-U22:
100/100/100

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Page name:	WHL-U42(CHB)		
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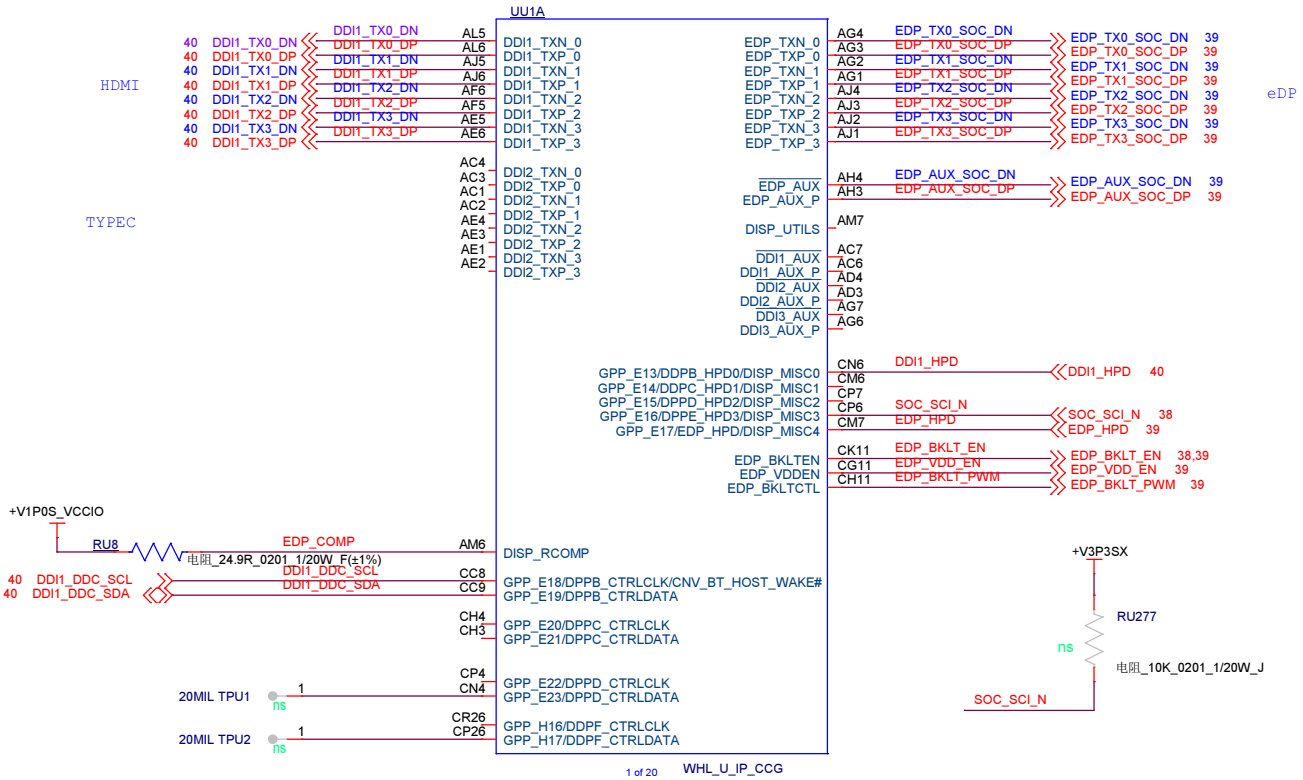

DISPLAY PORT STRAP

	Strap	How to Enable Port	How to Disable Port
DDI Port 1	DDPB_CTRLDATA(L12)	Pull up to 3.3 V	No Connect
DDI Port 2	DDPC_CTRLDATA(N8)	Pull up to 3.3 V	No Connect

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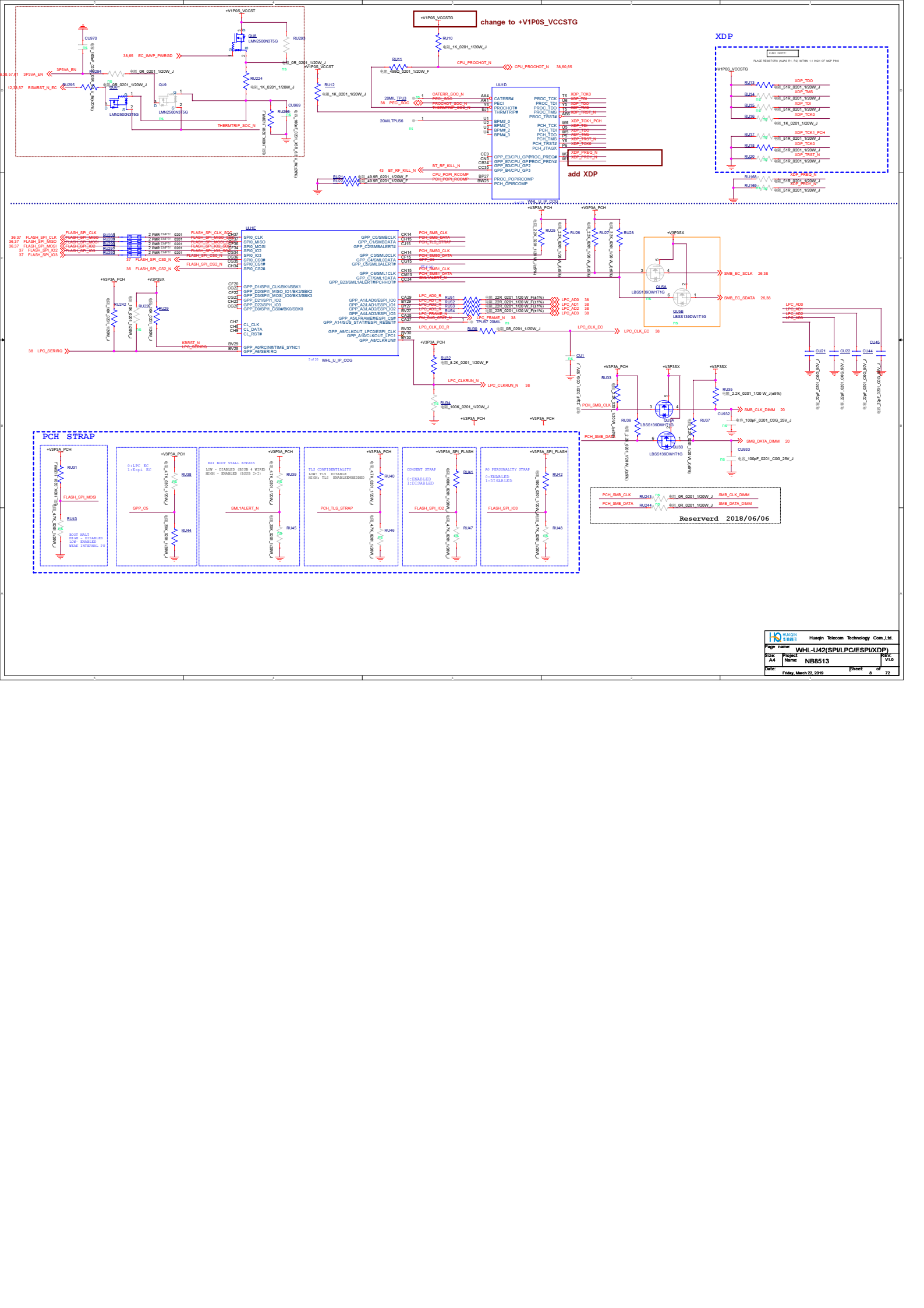
+V1P0S_VCCST
+V1P0S_VCCSTG
change to +V1P0S_VCCSTG
XDP
add XDP
PCH STRAP
Reserverd 2018/06/06
Huaqin Telecom Technology Com.,Ltd.
Page name: WHL-U42(SPI/LPC/ESPI/XDP)
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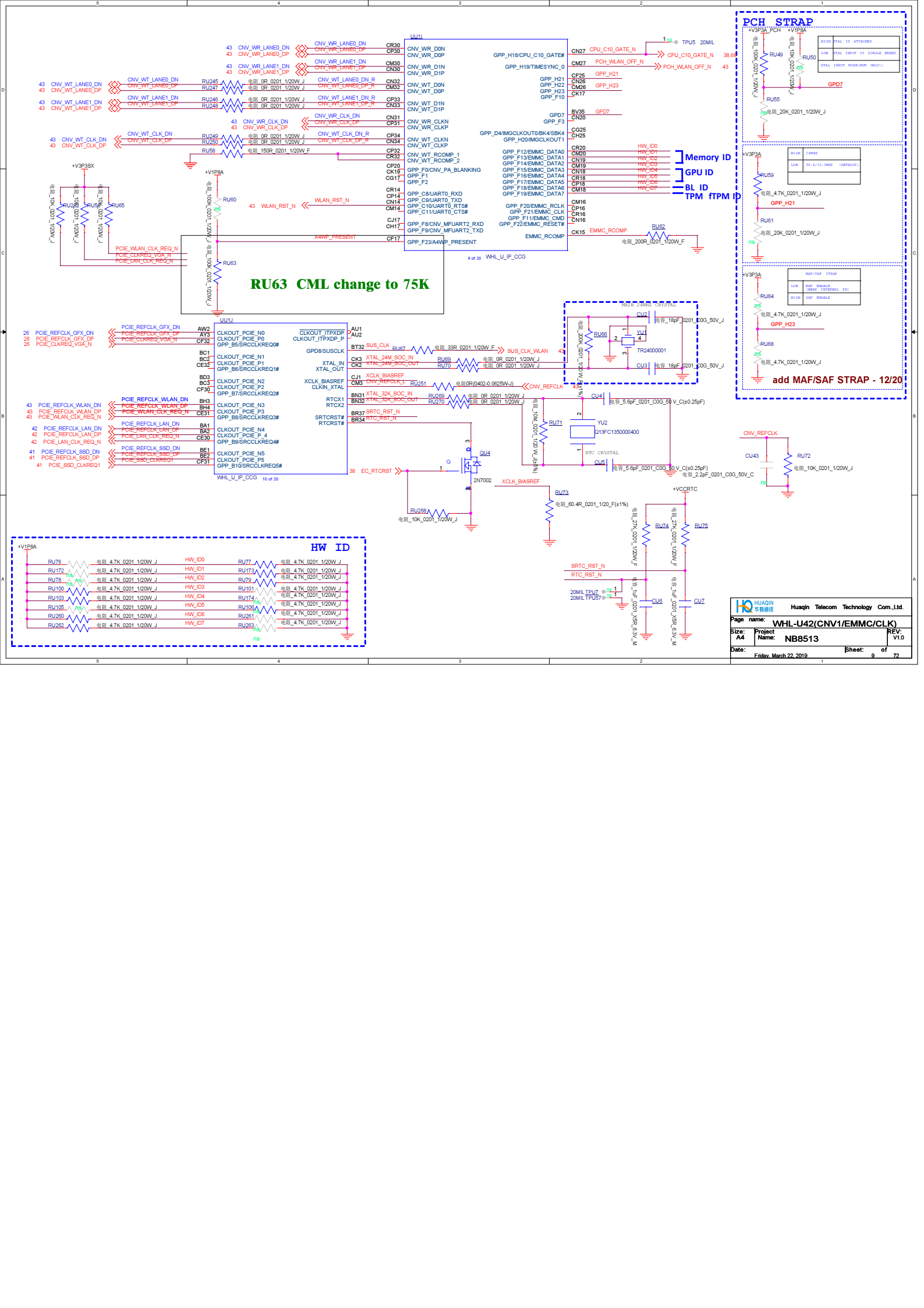
PCH STRAP
RU63 CML change to 75K
add MAF/SAF STRAP - 12/20
HW ID
Memory ID
GPU ID
BL ID
TPM fTPM ID
Huaqin Telecom Technology Com.,Ltd.
Page name: WHL-U42(CNV1/EMMC/CLK)
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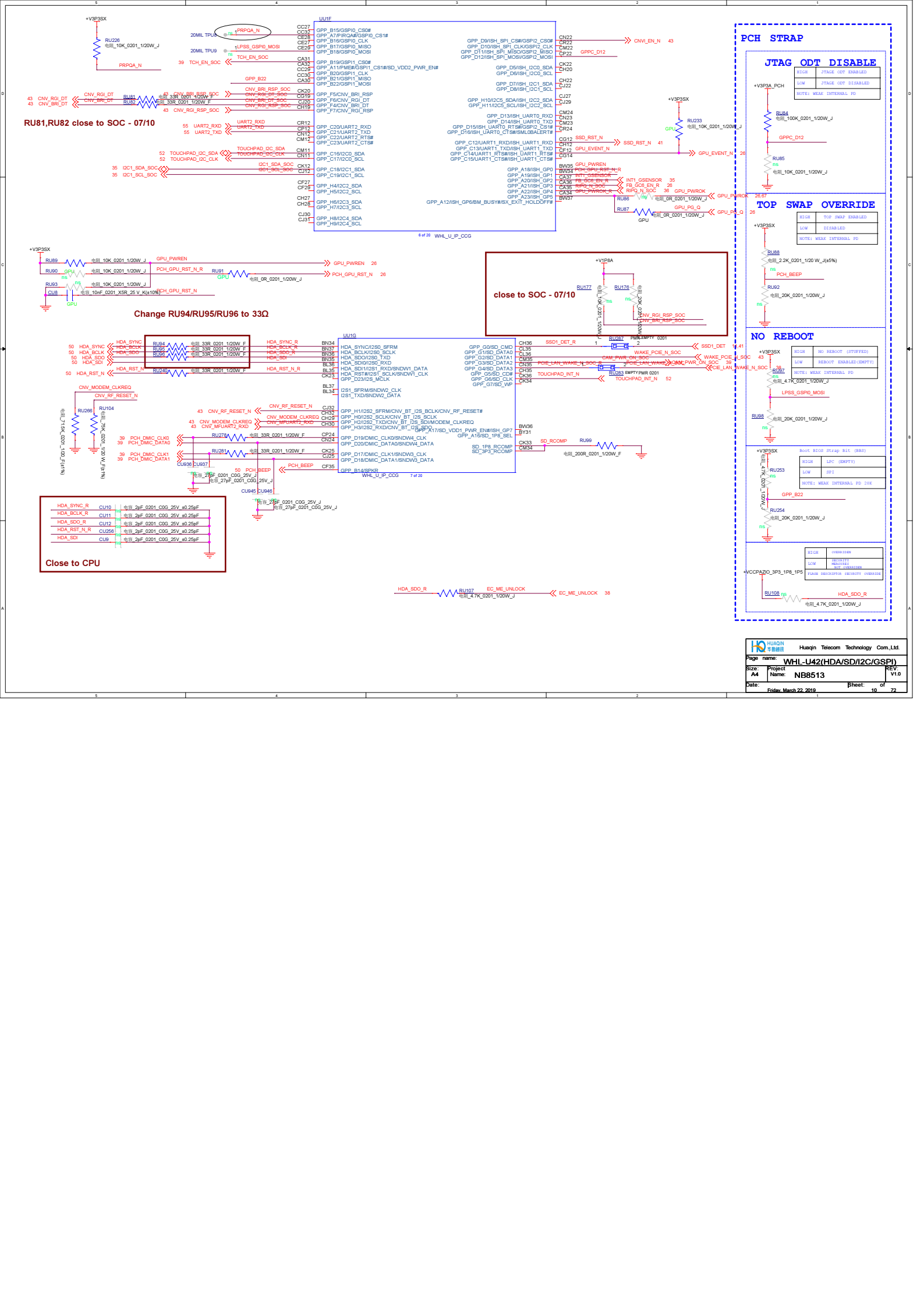
PCH STRAP
JTAG ODT DISABLE
HIGH JTAGC ODT ENABLED
LOW JTAGC ODT DISABLED
NOTE: WEAK INTERNAL PD
TOP SWAP OVERRIDE
HIGH TOP SWAP ENABLED
LOW DISABLED
NOTE: WEAK INTERNAL PD
NO REBOOT
HIGH NO REBOOT (STUFFED)
LOW REBOOT ENABLED(EMPTY)
NOTE: WEAK INTERNAL PD
Boot BIOS Strap Bit (BBS)
HIGH LPC (EMPTY)
LOW SPI
NOTE: WEAK INTERNAL PD 20K
HIGH OVERRIDEN
LOW SECURITY MEASURES NOT OVERRIDEN
FLASH DESCRIPTOR SECURITY OVERRIDE
RU81,RU82 close to SOC - 07/10
Change RU94/RU95/RU96 to 33Ω
close to SOC - 07/10
Close to CPU
UU1F
UU1G
WHL_U_IP_CCG
Huaqin Telecom Technology Com.,Ltd.
Page name: WHL-U42(HDA/SD/I2C/GSPI)
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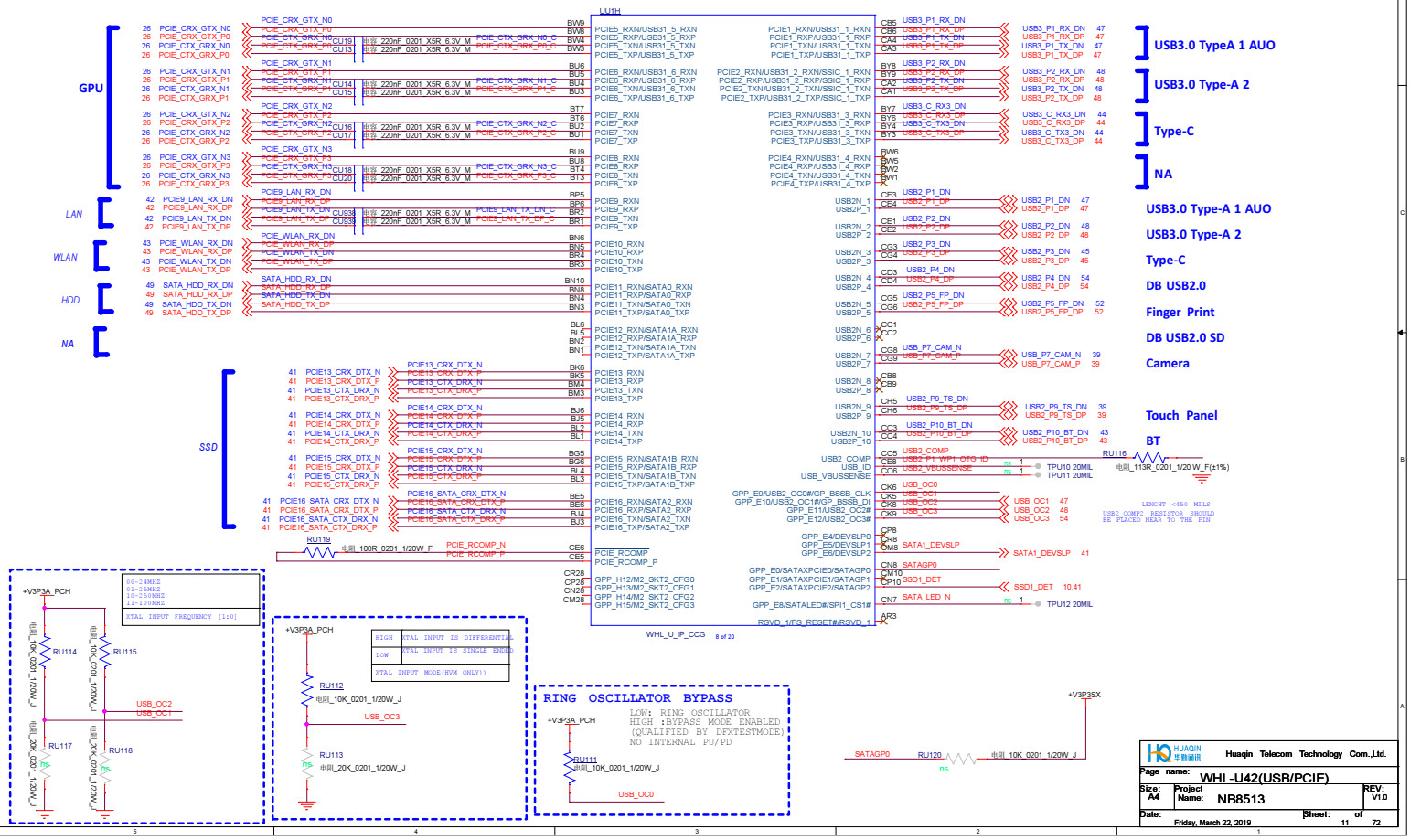

Huaqin Telecom Technology Com.,Ltd.	
Page name:	WHL-U42(USB/PCIE)
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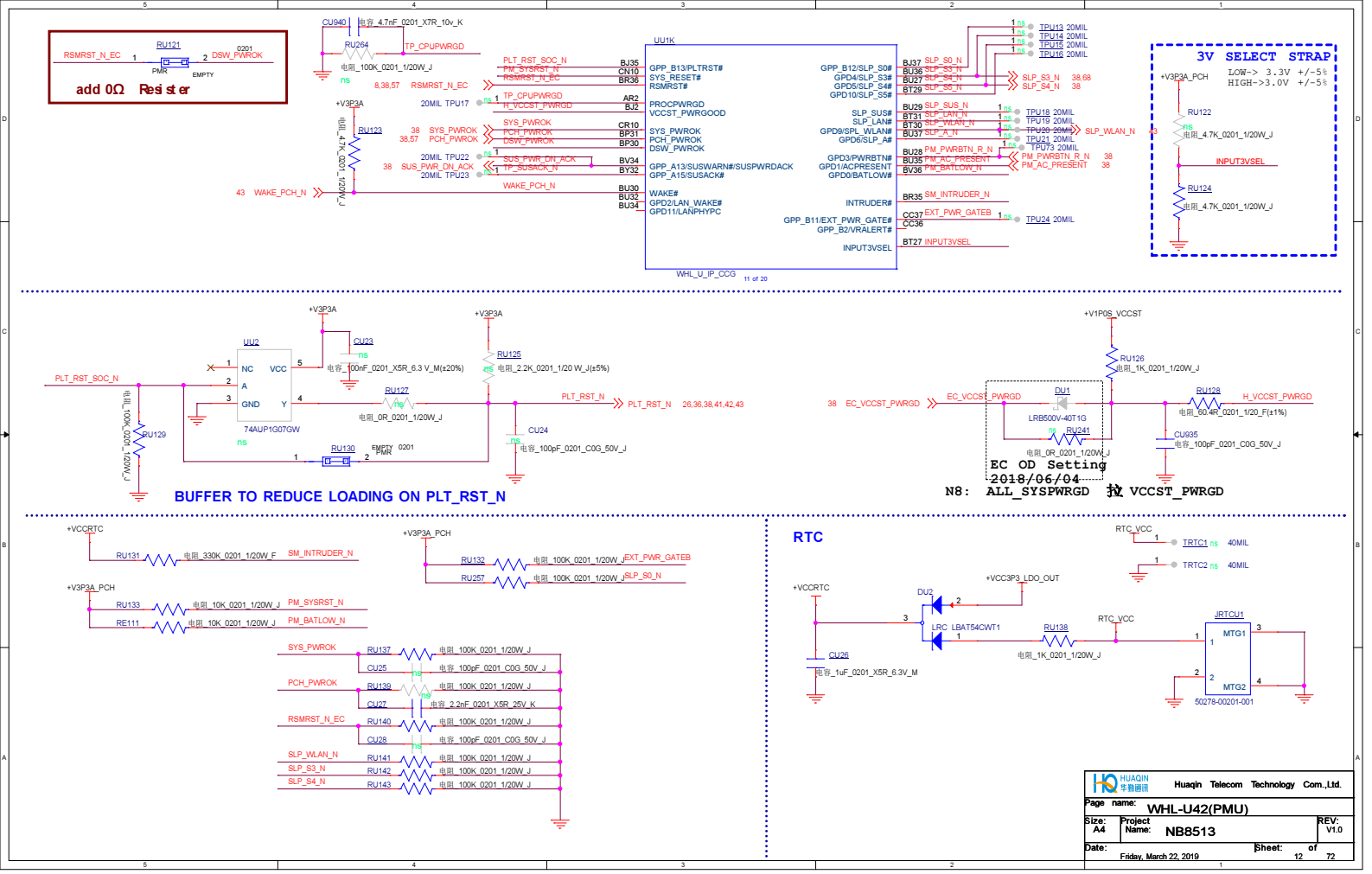

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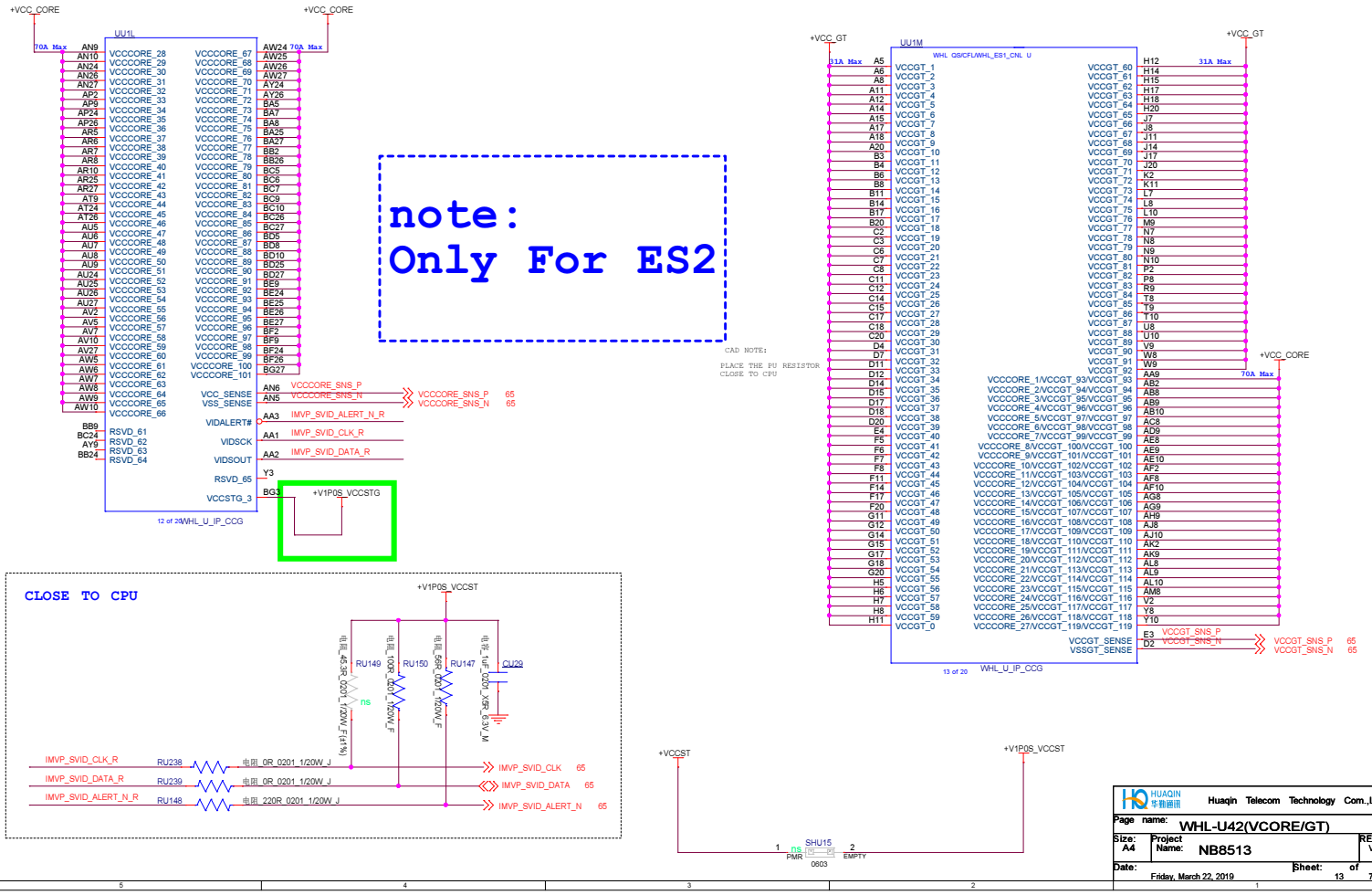
+VCC_CORE
+VCC_CORE
UU1L
70A Max
AN9
AN10
AN24
AN26
AN27
AP2
AP9
AP24
AP26
AR5
AR6
AR7
AR8
AR10
AR25
AR27
AT9
AT24
AT26
AU5
AU6
AU7
AU8
AU9
AU24
AU25
AU26
AU27
AV2
AV5
AV7
AV10
AV27
AW5
AW6
AW7
AW8
AW9
AW10
VCCCORE_28
VCCCORE_29
VCCCORE_30
VCCCORE_31
VCCCORE_32
VCCCORE_33
VCCCORE_34
VCCCORE_35
VCCCORE_36
VCCCORE_37
VCCCORE_38
VCCCORE_39
VCCCORE_40
VCCCORE_41
VCCCORE_42
VCCCORE_43
VCCCORE_44
VCCCORE_45
VCCCORE_46
VCCCORE_47
VCCCORE_48
VCCCORE_49
VCCCORE_50
VCCCORE_51
VCCCORE_52
VCCCORE_53
VCCCORE_54
VCCCORE_55
VCCCORE_56
VCCCORE_57
VCCCORE_58
VCCCORE_59
VCCCORE_60
VCCCORE_66
VCCCORE_67
VCCCORE_68
VCCCORE_69
VCCCORE_70
VCCCORE_71
VCCCORE_72
VCCCORE_73
VCCCORE_74
VCCCORE_75
VCCCORE_76
VCCCORE_77
VCCCORE_78
VCCCORE_79
VCCCORE_80
VCCCORE_81
VCCCORE_82
VCCCORE_83
VCCCORE_84
VCCCORE_85
VCCCORE_86
VCCCORE_87
VCCCORE_88
VCCCORE_89
VCCCORE_90
VCCCORE_91
VCCCORE_92
VCCCORE_93
VCCCORE_94
VCCCORE_95
VCCCORE_96
VCCCORE_97
VCCCORE_98
VCCCORE_99
VCCCORE_100
VCCCORE_101
AW24
AW25
AW26
AW27
AY24
AY26
BA5
BA7
BA8
BA25
BA27
BB2
BB26
BC5
BC6
BC7
BC9
BC10
BC26
BC27
BD5
BD8
BD10
BD25
BD27
BE9
BE24
BE25
BE26
BE27
BF2
BF9
BF24
BF26
BG27
AN6
AN5
VCCORE_SNS_P
VCCORE_SNS_N
VCC_SENSE
VSS_SENSE
VCCORE_SNS_P
VCCORE_SNS_N
65
65
AA3
VIDALERT#
IMVP_SVID_ALERT_N_R
AA1
VIDSCK
IMVP_SVID_CLK_R
AA2
VIDSOUT
IMVP_SVID_DATA_R
Y3
RSVD_65
BG3
VCCSTG_3
+V1P0S_VCCSTG
BB9
BC24
AY9
BB24
RSVD_61
RSVD_62
RSVD_63
RSVD_64
12 of 20
WHL_U_IP_CCG
note:
Only For ES2
CAD NOTE:
PLACE THE PU RESISTOR
CLOSE TO CPU
+VCC_GT
+VCC_GT
UU1M
WHL QS/CFL/WHL_ES1_CNL U
31A Max
A5
A6
A8
A11
A12
A14
A15
A17
A18
A20
B3
B4
B6
B8
B11
B14
B16
B17
B20
C2
C3
C6
C7
C8
C11
C12
C14
C15
C17
C18
C20
D4
E4
F5
F6
F7
F8
F11
F14
F17
F20
G11
G12
G14
G15
G17
G18
G20
H5
H6
H7
H8
H11
VCCGT_1
VCCGT_2
VCCGT_3
VCCGT_4
VCCGT_5
VCCGT_6
VCCGT_7
VCCGT_8
VCCGT_9
VCCGT_10
VCCGT_11
VCCGT_12
VCCGT_13
VCCGT_14
VCCGT_15
VCCGT_16
VCCGT_17
VCCGT_18
VCCGT_19
VCCGT_20
VCCGT_21
VCCGT_22
VCCGT_23
VCCGT_24
VCCGT_25
VCCGT_26
VCCGT_27
VCCGT_28
VCCGT_29
VCCGT_30
VCCGT_31
VCCGT_32
VCCGT_33
VCCGT_34
VCCGT_35
VCCGT_36
VCCGT_37
VCCGT_38
VCCGT_39
VCCGT_40
VCCGT_41
VCCGT_42
VCCGT_43
VCCGT_44
VCCGT_45
VCCGT_46
VCCGT_47
VCCGT_48
VCCGT_49
VCCGT_50
VCCGT_51
VCCGT_52
VCCGT_53
VCCGT_54
VCCGT_55
VCCGT_56
VCCGT_57
VCCGT_58
VCCGT_59
VCCGT_0
VCCGT_60
VCCGT_61
VCCGT_62
VCCGT_63
VCCGT_64
VCCGT_65
VCCGT_66
VCCGT_67
VCCGT_68
VCCGT_69
VCCGT_70
VCCGT_71
VCCGT_72
VCCGT_73
VCCGT_74
VCCGT_75
VCCGT_76
VCCGT_77
VCCGT_78
VCCGT_79
VCCGT_80
VCCGT_81
VCCGT_82
VCCGT_83
VCCGT_84
VCCGT_85
VCCGT_86
VCCGT_87
VCCGT_88
VCCGT_89
VCCGT_90
VCCGT_91
VCCGT_92
VCCGT_93
VCCGT_94
VCCGT_95
VCCGT_96
VCCGT_97
VCCGT_98
VCCGT_99
VCCGT_100
VCCGT_101
VCCGT_102
VCCGT_103
VCCGT_104
VCCGT_105
VCCGT_106
VCCGT_107
VCCGT_108
VCCGT_109
VCCGT_110
VCCGT_111
VCCGT_112
VCCGT_113
VCCGT_114
VCCGT_115
VCCGT_116
VCCGT_117
VCCGT_118
VCCGT_119
VCCGT_SENSE
VSSGT_SENSE
H12
H14
H15
H17
H18
H20
J7
J8
J11
J14
J17
J20
K2
K11
L7
L8
L10
M9
N7
N8
N9
N10
P2
P8
R9
T8
T9
T10
U8
U10
V9
W8
W9
AA9
AB2
AB8
AB9
AB10
AC8
AD9
AE8
AE9
AE10
AF2
AF8
AF10
AG8
AG9
AH9
AJ8
AJ10
AK2
AK9
AL8
AL9
AL10
AM8
V2
Y8
Y10
31A Max
+VCC_CORE
70A Max
E3
D2
VCCGT_SNS_P
VCCGT_SNS_N
VCCGT_SNS_P
VCCGT_SNS_N
65
65
13 of 20
WHL_U_IP_CCG
CLOSE TO CPU
+V1P0S_VCCST
RU149
RU150
RU147
CU29
ns
IMVP_SVID_CLK_R
RU238
电阻_0R_0201_1/20W_J
IMVP_SVID_CLK
65
IMVP_SVID_DATA_R
RU239
电阻_0R_0201_1/20W_J
IMVP_SVID_DATA
65
IMVP_SVID_ALERT_N_R
RU148
电阻_220R_0201_1/20W_J
IMVP_SVID_ALERT_N
65
+VCCST
+V1P0S_VCCST
SHU15
PMR
0603
EMPTY
HUAQIN
华勤通讯
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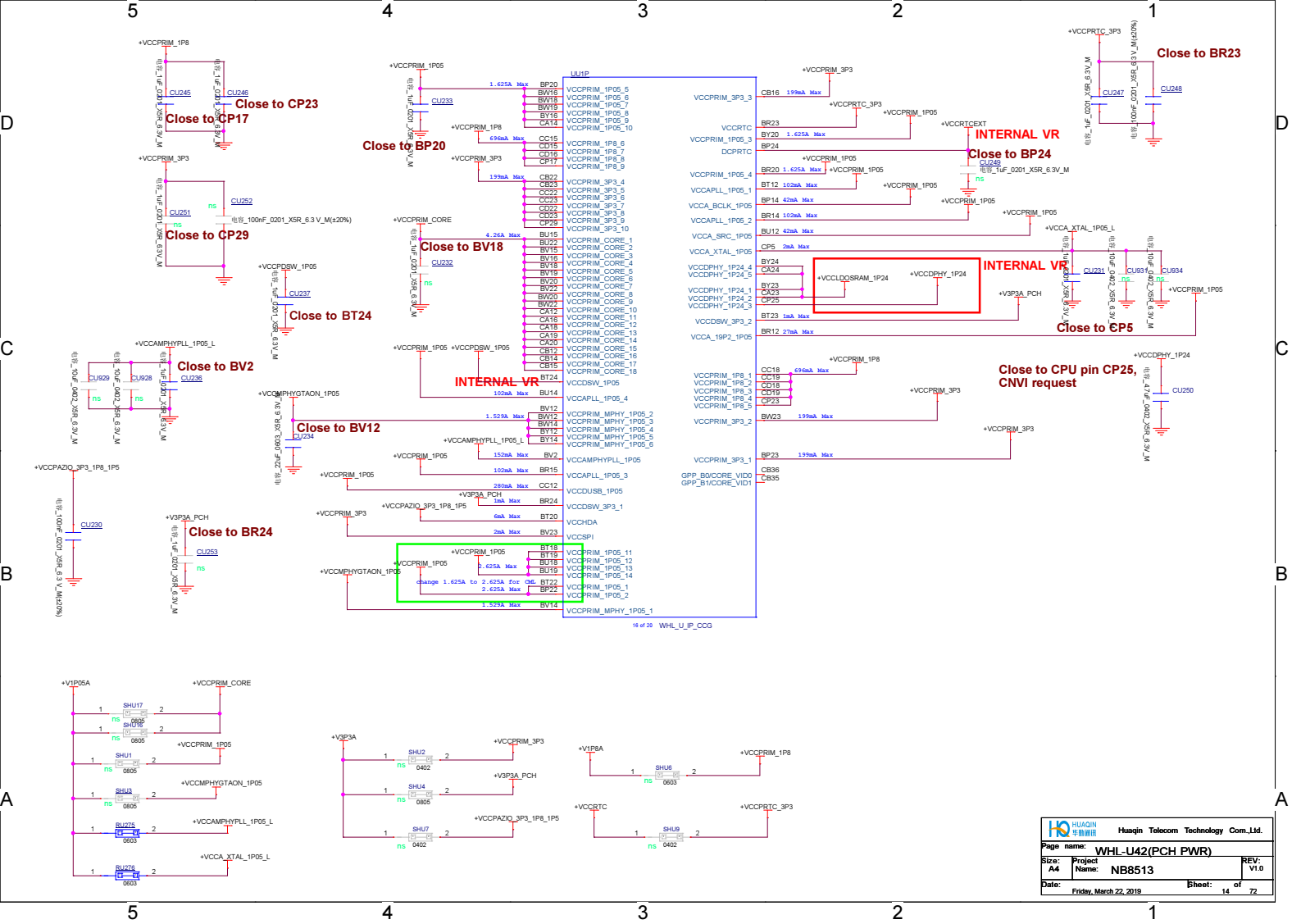

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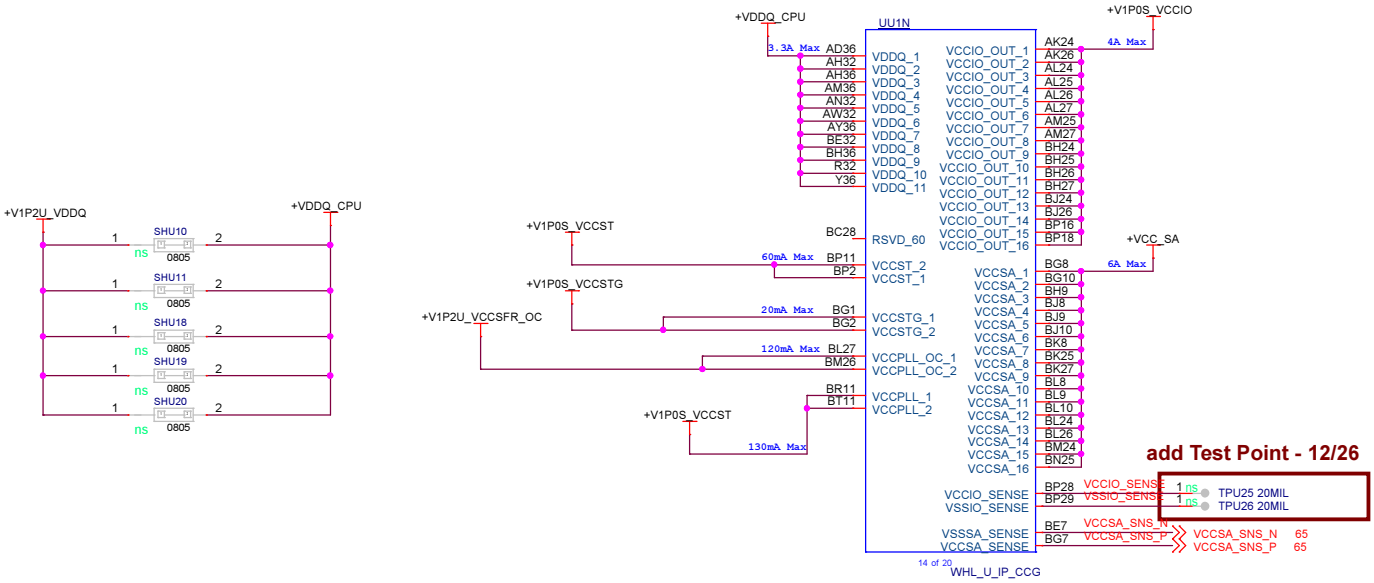

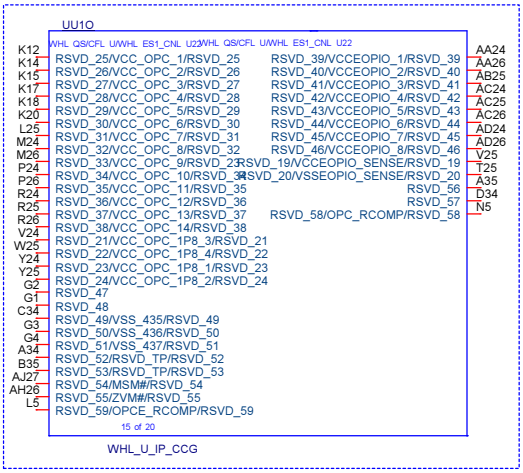

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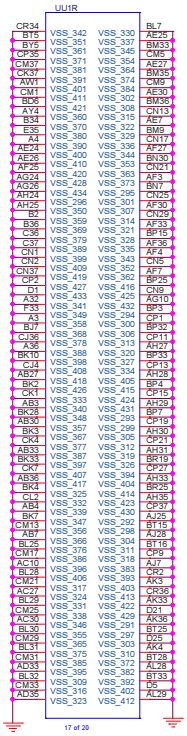

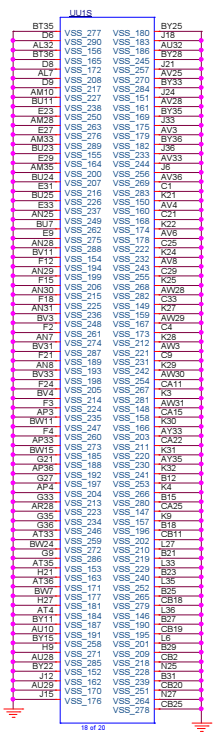

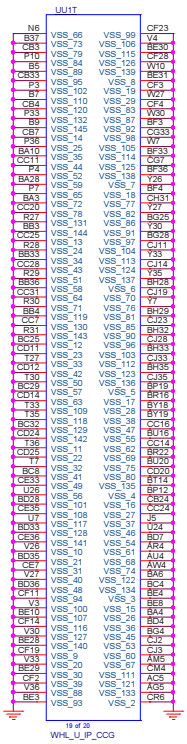

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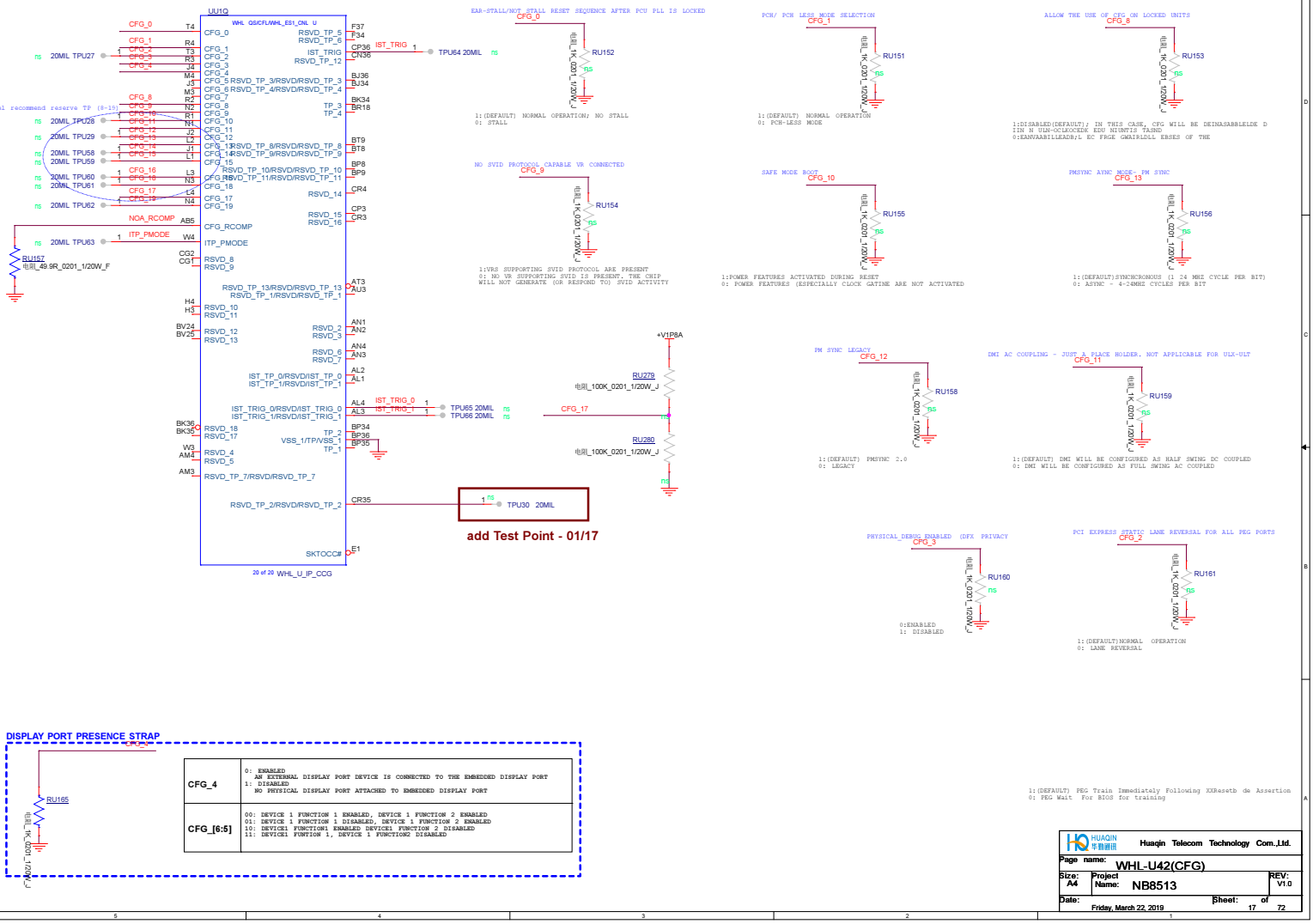

DISPLAY PORT PRESENCE STRAP

CFG_4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
CFG_[6:5]	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED 10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED 11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

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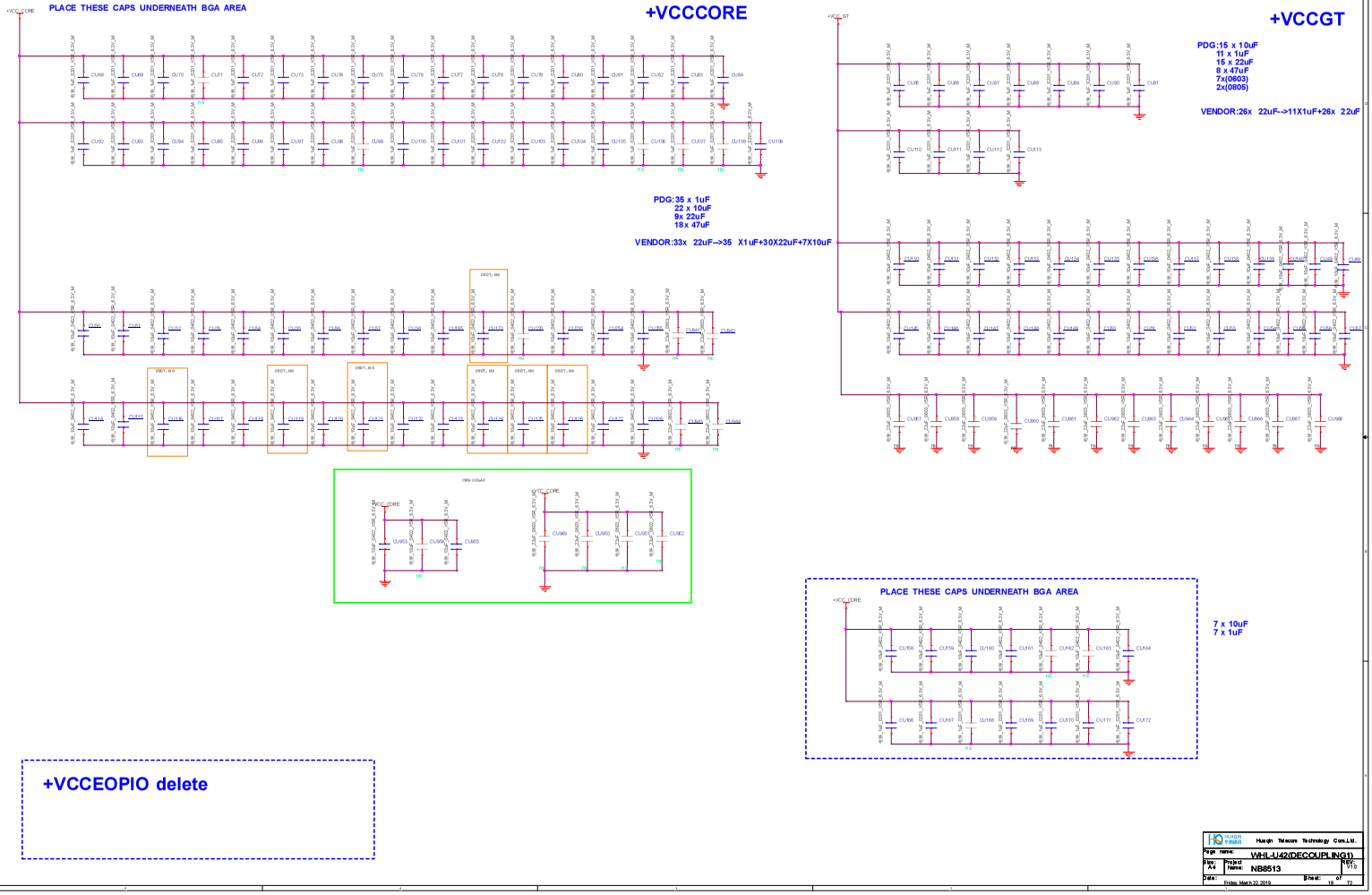

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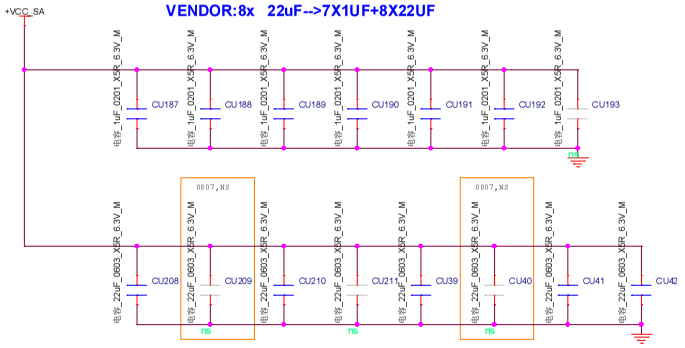
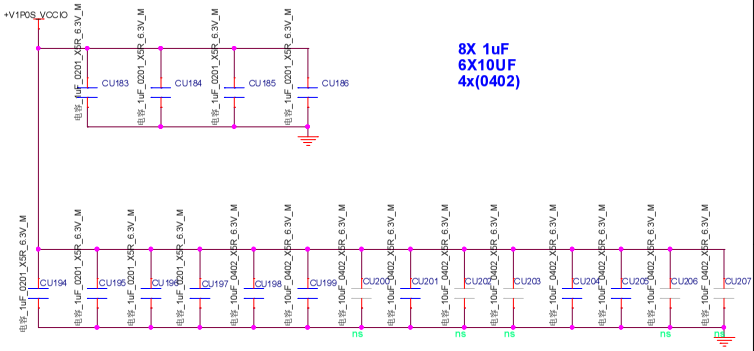
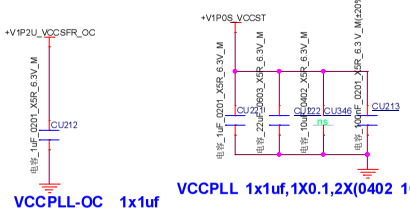
PDG:7x 1uF
15X 10uF
2 x 47 uF
2 x (0805)

VENDOR:8x 22uF-->7X1UF+8X22UF

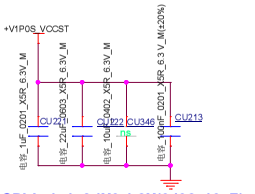


8X 1uF
6X10UF
4x(0402)

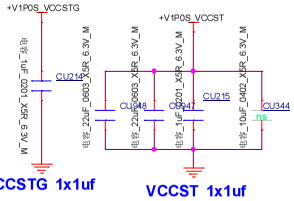




VCCPLL-OC 1x1uf

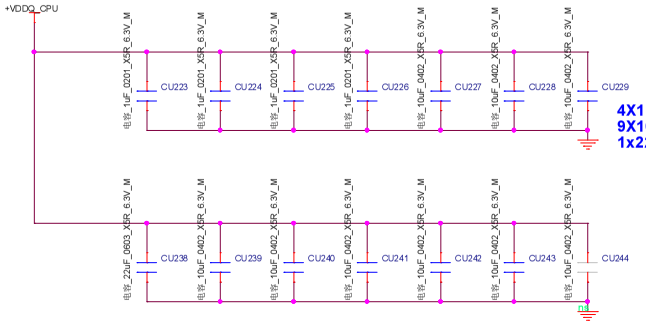


VCCPLL 1x1uf,1X0.1,2X(0402 10uF)



VCCSTG 1x1uf

VCCST 1x1uf



4X1UF
9X10UF
1x22UF

HUAQIN 华勤通讯	Husqin Telecom Technology Com.,Ltd.	
Page name:	WHL-U42(DECOUPLING2)	
Size: A4	Project Name: NB8513	REV: V1.0
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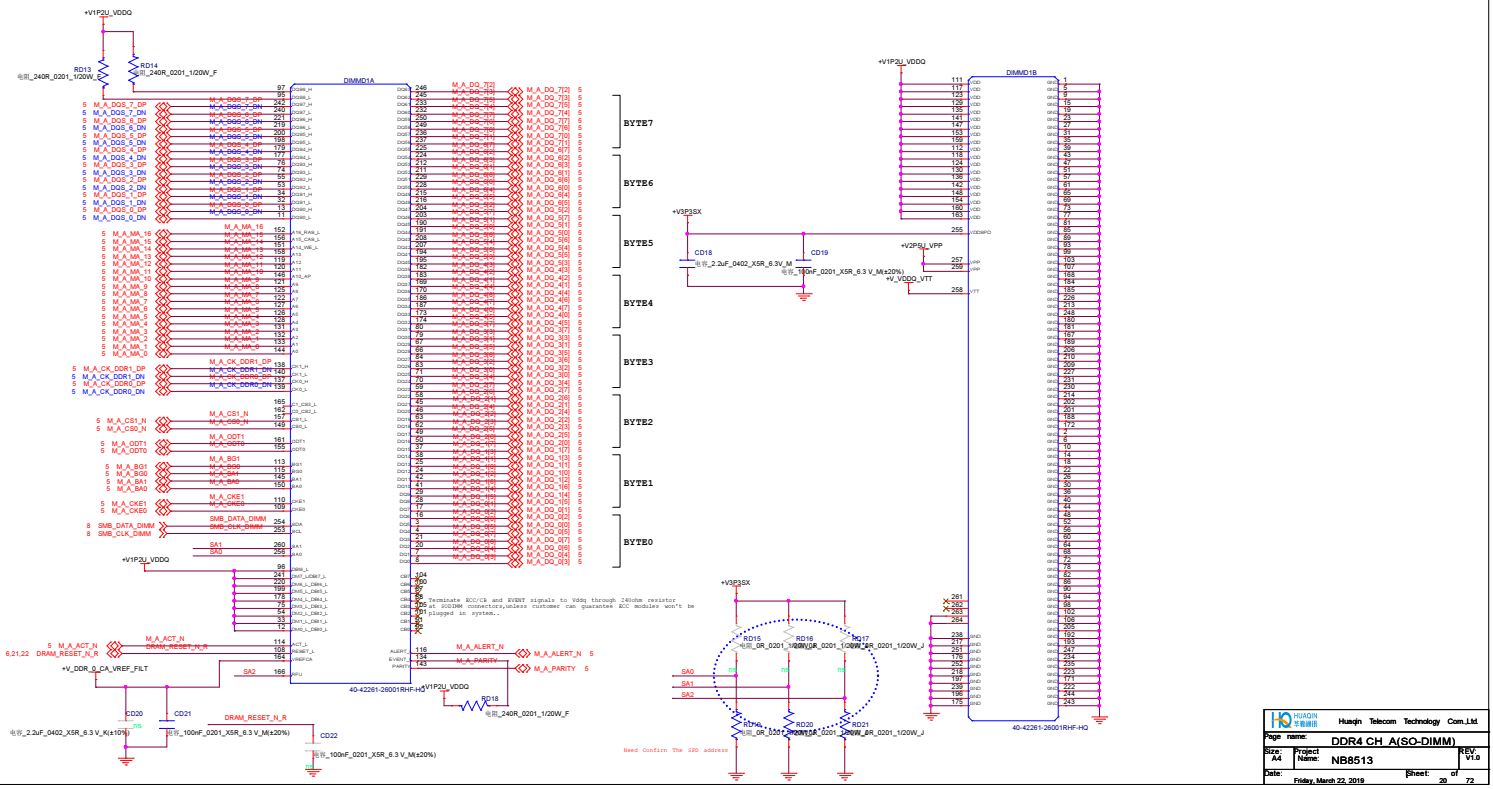
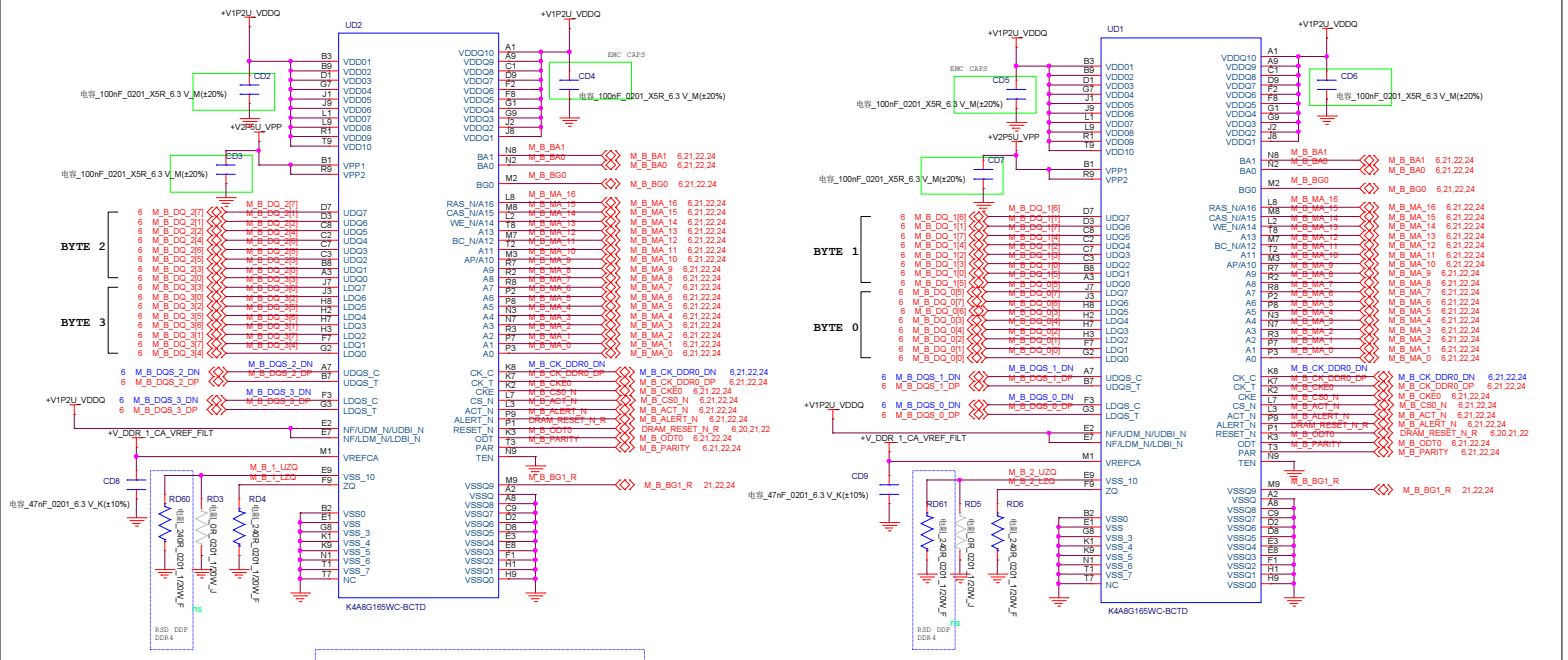


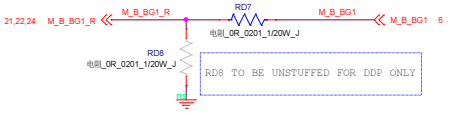
Page name:	DDR4 CH_A(SO-DIMM)		
Size: A4	Project Name: NB8513		REV: V1.0
Date: Friday, March 22, 2019		Sheet: 20	of 72

Huaqin Telecom Technology Com.,Ltd.



NOTE: TO BE STUFF FOR DUAL ZQ PARTS

RD7 TO BE STUFFED FOR DDP ONLY



RD8 TO BE UNSTUFFED FOR DDP ONLY

BOM NOTE

DDR PINS	SDP	DDP
E9 UZQ	GND	240E PD
M9 BG1	GND	BG1 SIG FROM CONTROLLER

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Page name:	DDR4 CH-B(DEVICE0)
Size: A4	Project Name: NB8513 REV: V1.0
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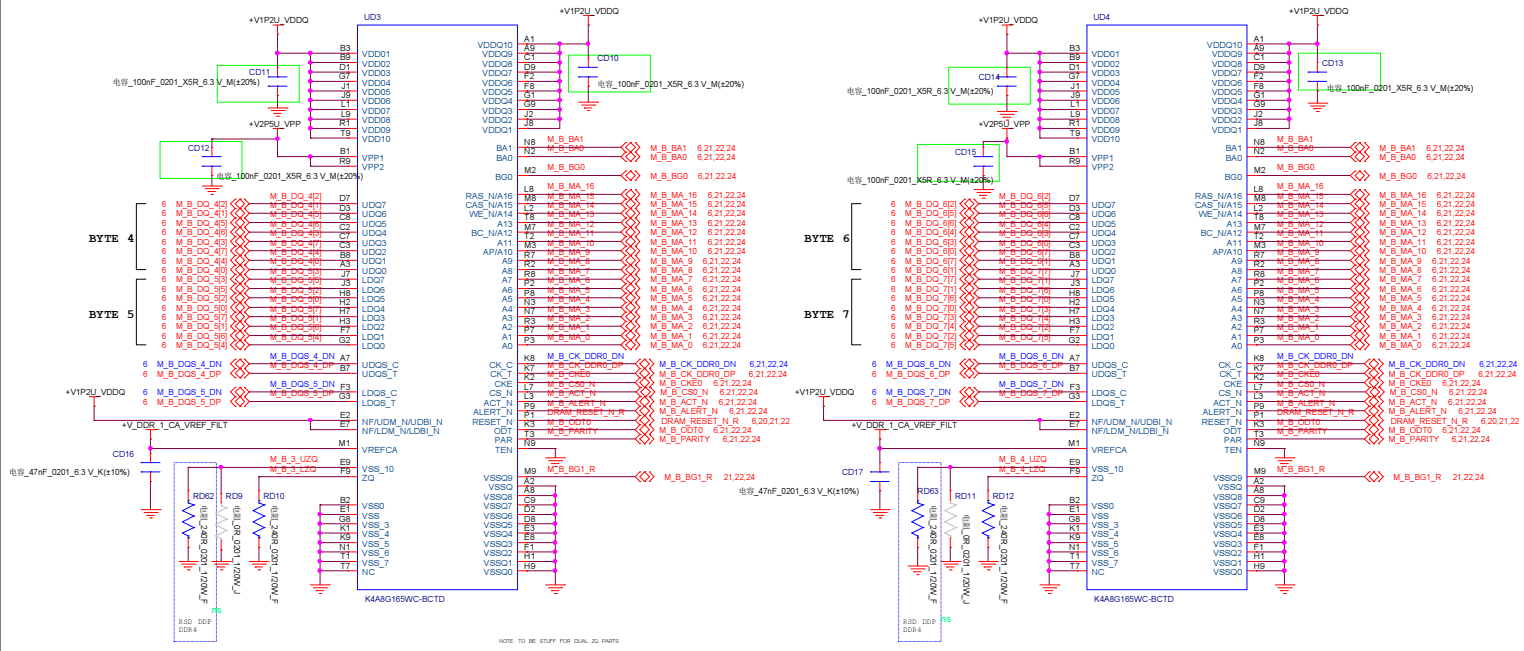

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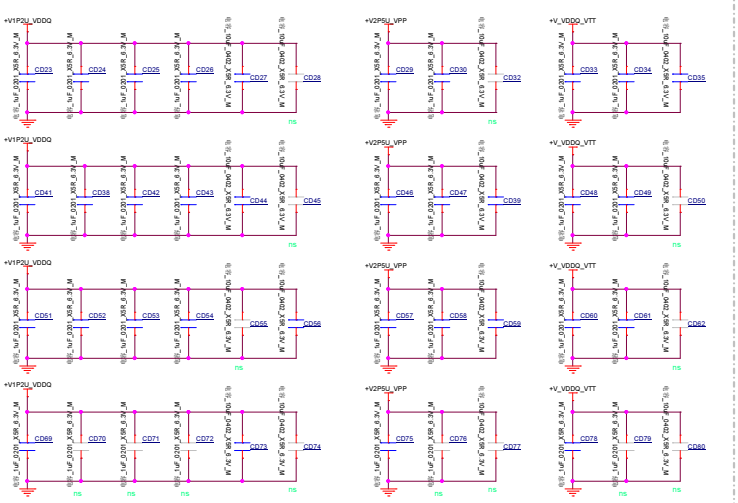
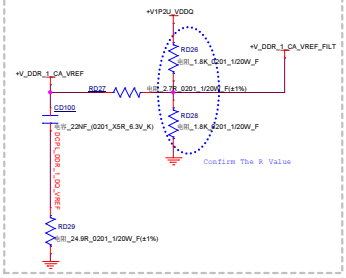
Page name:	DDR4 CH_B(DEVICE1)		
Size: A4	Project Name: NB8513	REV: V1.0	
Date: Friday, March 22, 2019	Sheet: 22 of 72		

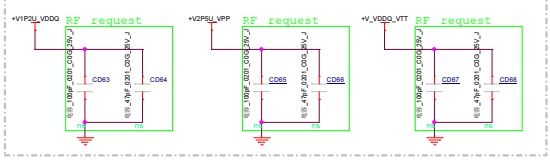
DECOUPLING CAPACITORS FOR DDR CHANNEL B MD



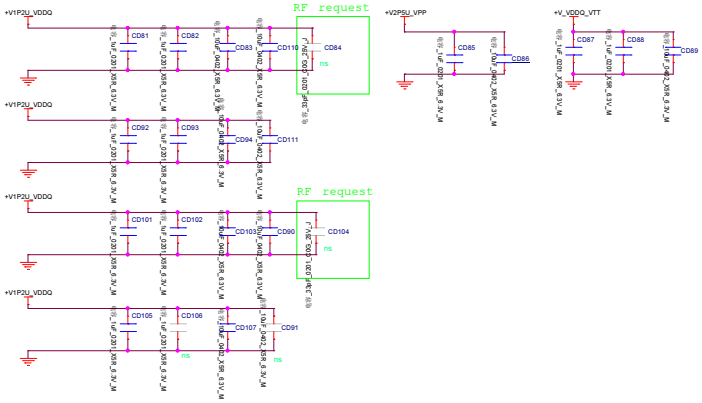
DDR4 CH B MD REF GENERATION



CHB MD

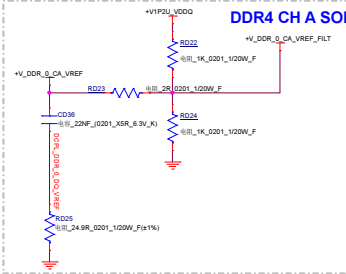


DECOUPLING CAPACITORS FOR DDR CHANNEL A SODIMM



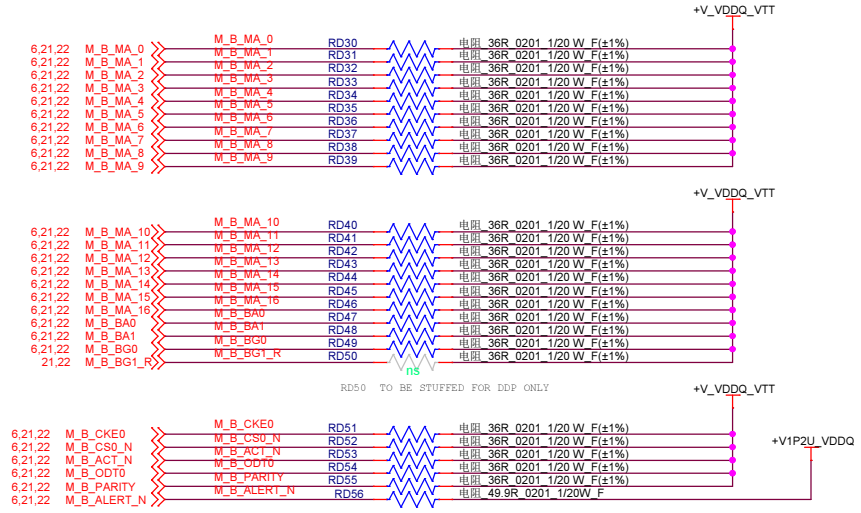
Close to SODIMM

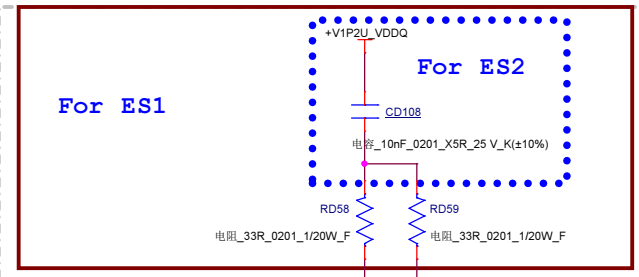
DDR4 CH A SODIMM REF GENERATION



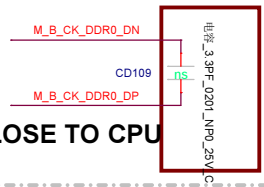
Huaqin Telecom Technology Com.,Ltd.			
Page name:	DDR4(DECAPS)		
Size: A4	Project Name:	NB8513	REV: V1.0
Date: Friday, March 22, 2019	Sheet: 23	of 72	

MEMORY TERMINATIONS CHANNEL B MD





PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP



PLACE CLOSE TO CPU

1.change +V_VDDQ_VTT to +V1P2U_VDDQ
2. add CAP CD155 for ES2 sample - 01/04
3. add RD89 for ES1 sample -01/23

change CD146 to 3.3pF - 01/04

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Page name:	DDR4 TERMINATIONS	
Size: A4	Project Name: NB8513	REV: V1.0
Date: Friday, March 22, 2019	Sheet: 24 of 72	

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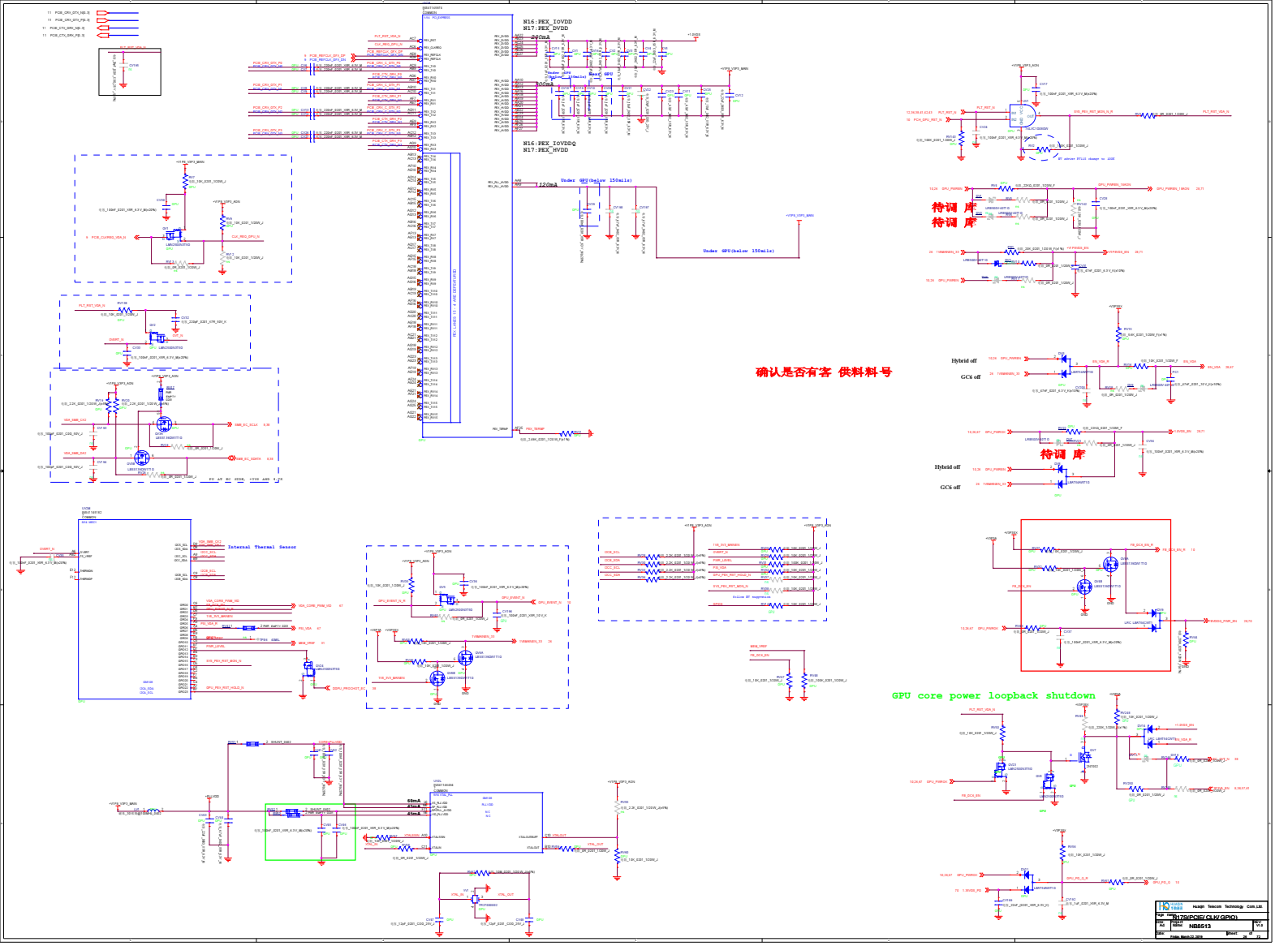
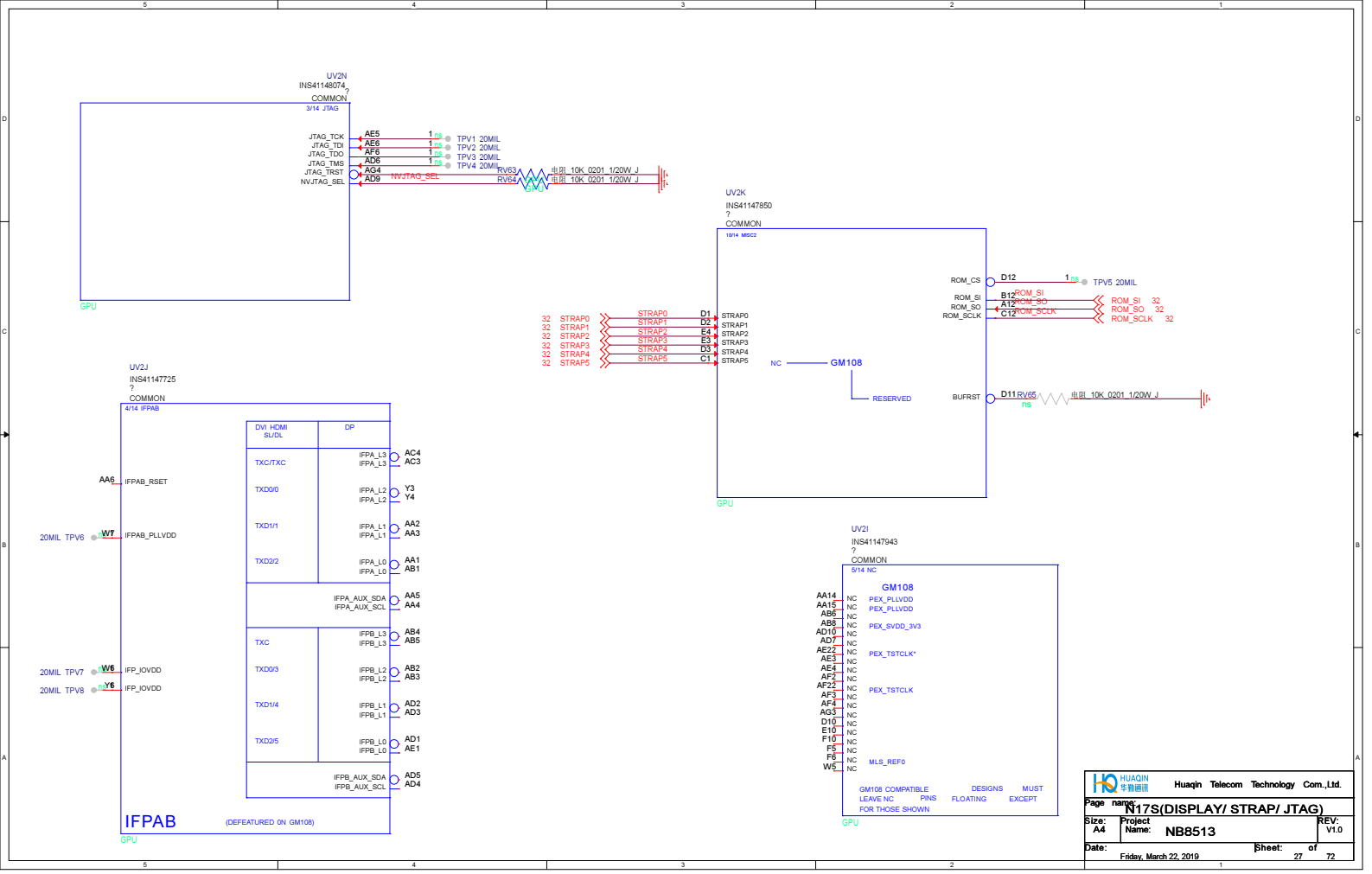
Date: Friday, March 22, 2019	Sheet: 25 of 72	


N16:PEX_IOVDD
N17:PEX_DVDD
290mA
Under GPU(below 150mils)
N16:PEX_IOVDDQ
N17:PEX_HVDD
120mA
Under GPU(below 150mils)
特调 库
特调 库
确认是否有客 供料料号
Hybrid off
GC6 off
特调 库
Hybrid off
GC6 off
Internal Thermal Sensor
GPU core power loopback shutdown
N17S(PCIE/CLK/GPIO)
NB8513



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Size: A4	Project Name: NB8513	REV: V1.0
Date: Friday, March 22, 2019	Sheet: 27 of 72	

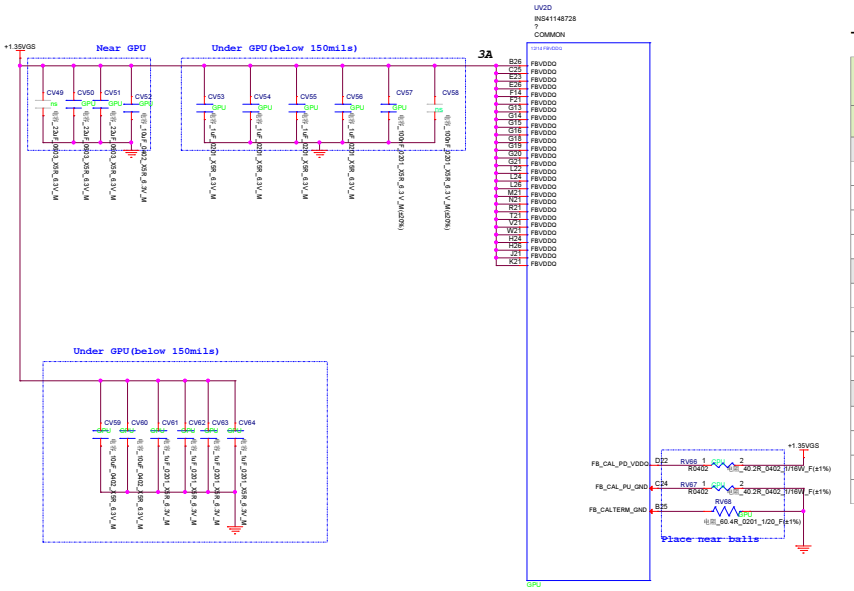
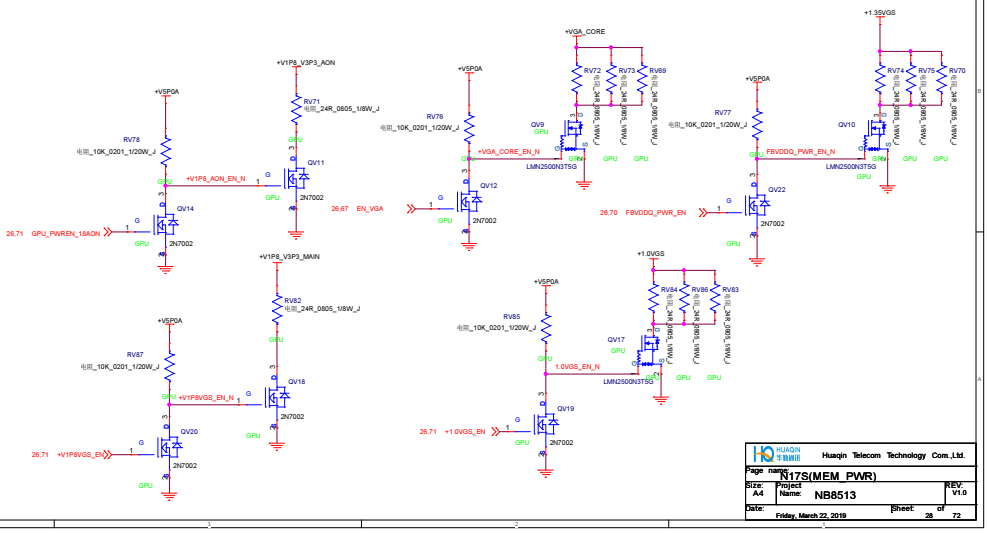


Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: GB2C-64 (preliminary)			
1.0 uF	X6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	X6S [0603]	2	
10 uF	X6S [0603]	1	Near GPU device
22 uF	X6S [0603]	3	
For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	
For N17x GPU Package: GB4-256			
1.0 uF	X6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	5	
10 uF	X6S [0603]	7	Near GPU device
22 uF	X6S [0603]	9	

+V1P8A TO +V1P8_AON

Move to Power Page 2018/06/07



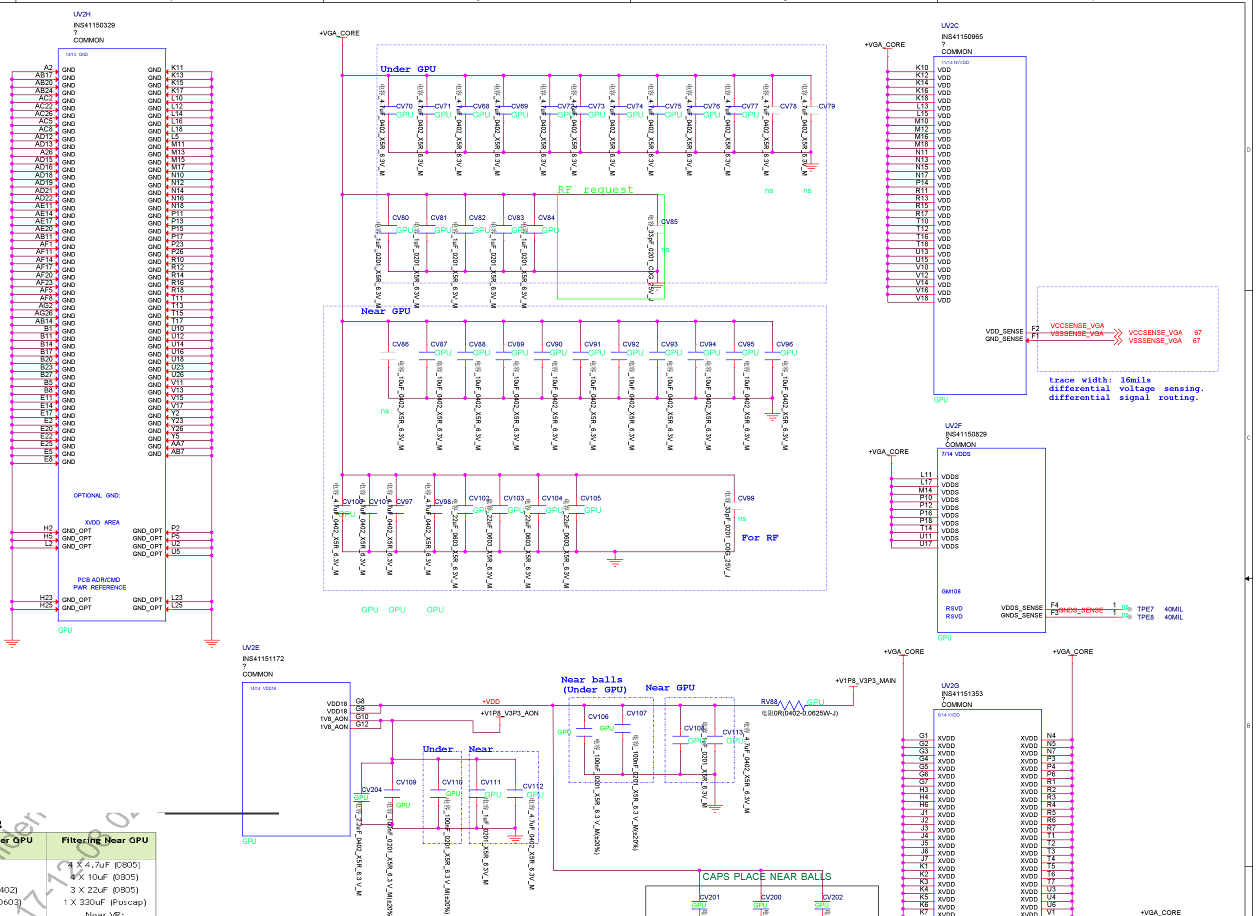


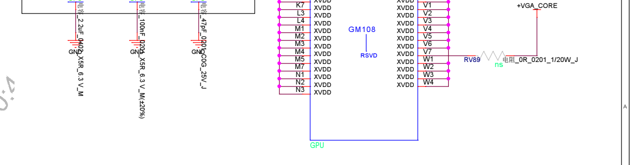
Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	4 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Poscap) Near VR: 2 X 10uF (0805)
NVVDDS	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Ω bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	
IFPAB_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
GPCPLL_AVDDx XS_PLLVDD	2		2 X 0.1uF (0402 X5R)	
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	
IFP_IOVDD	2	1.0V	2 X 0.1uF (0402 X6S)	1 X 4.7uF (0603) 1 X 1uF (0402)

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

Note:
1. Also see Section 9.2.2.1.10.1



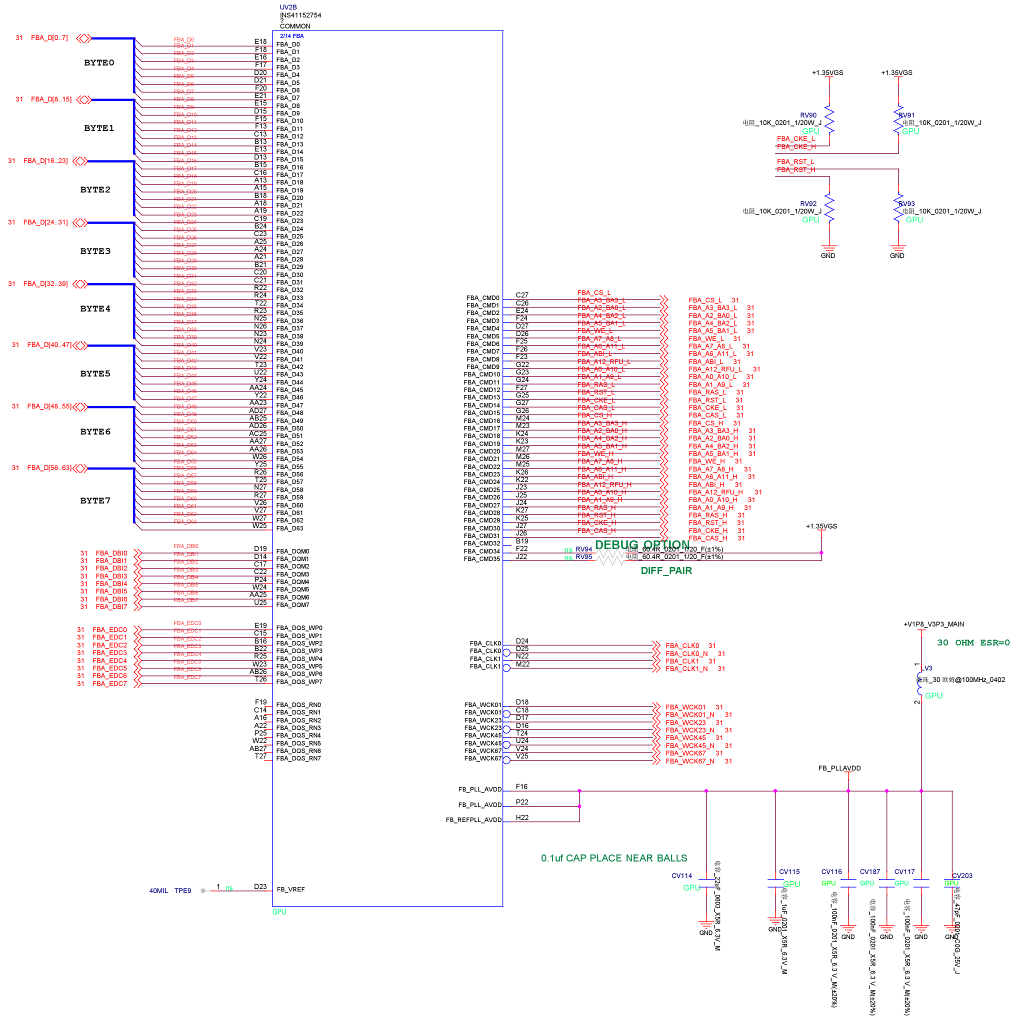
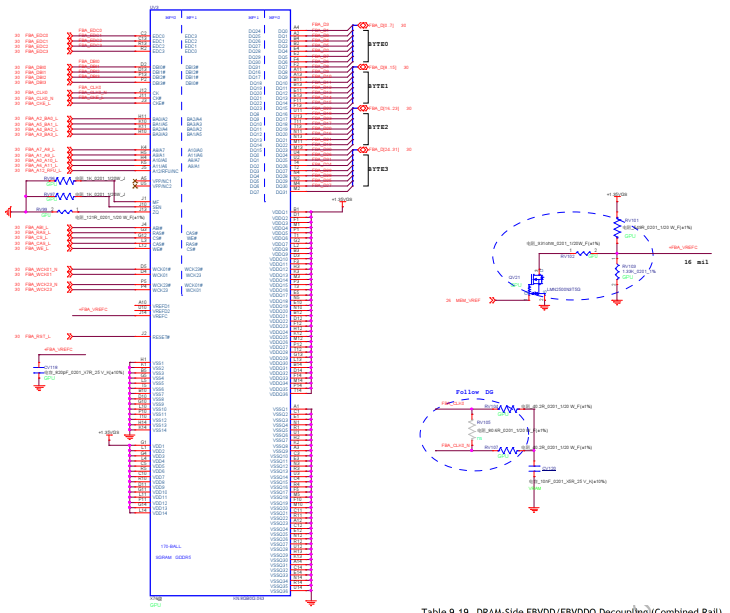


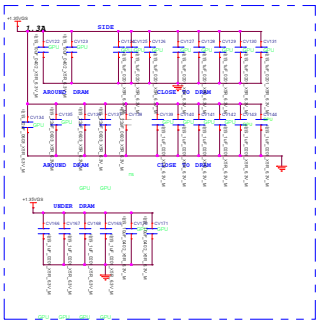
Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	**Channel 0 & 1**		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

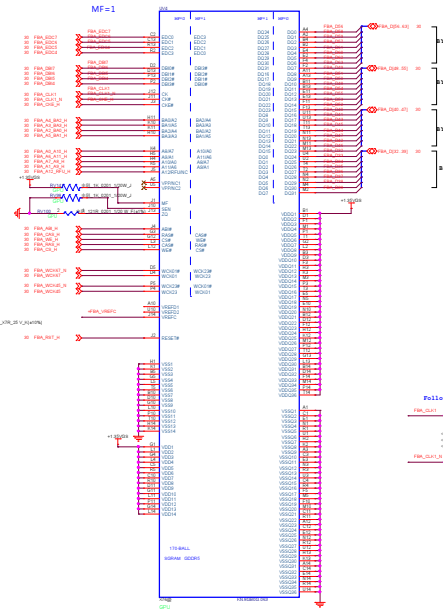
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

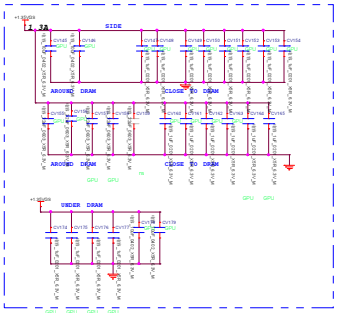
Memory - Lower 32 bits





Memory - Upper 32 bits





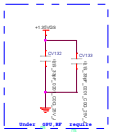
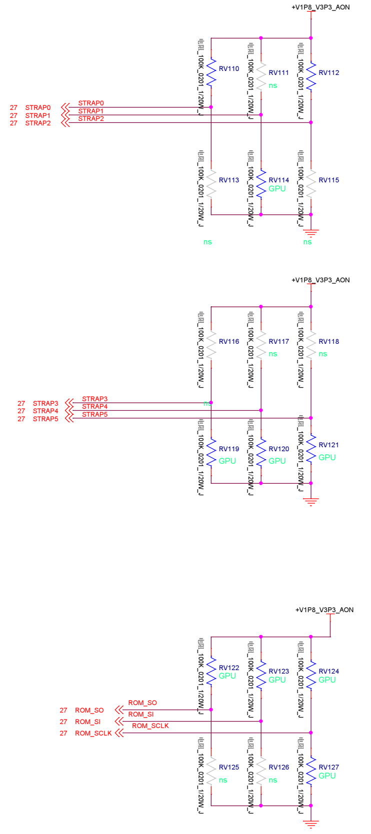


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X6S [0402]	10	**For x32 DRAM:** Under the DRAM FBVDD or FBVDDQ ball. **For x16 DRAM in a "clamshell" PCB configuration:** As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
10 uF	X6S [0603]	4	
1.0 uF	X6S [0402]	8 additional	**For x32 DRAM:** Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X6S [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.



For N17

GPU	Vendor	Manufacturer	Strap	Strap2	Strap1	Strap0
N17S-G1	Samsung	K4G80325FB-HC25	0x0	L	L	L
	Micron	MT51J256M32HF-70:A	0x1	L	L	H
	Hynix	H5GC8H24MJR-ROC	0x2	L	H	L
	Micron	MT51J256M32HF-70:B	0x4	H	L	L
	Hynix	H5GC8H24AJR-ROC	0x5	H	L	H
N17S_G0/G2	Micron	MT51J256M32HF-80:B	0x9	L	M	L
	Hynix	H5GC8H24AJR-R2C	0xA	L	M	H

N17S_G0/G2 follow N17S_G1 with NV confirm

PN	MPN	STRAP	Vendor
HQ11121854000	MT51J256M32HF-70:B	0x4	Micron
HQ11121852000	H5GC8H24AJR-R0C	0x5	Hynix
HQ11121870000	K4G80325FB-HC28	0x0	Samsung

Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[1]	RAM_CFG[0x00]
STRAP0			L		L
STRAP1			H		L
STRAP2			L		L

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M	Disable	Disable	Disable	Disable
ROM_SI	H				
ROM_SO	H				

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:
1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

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ODD

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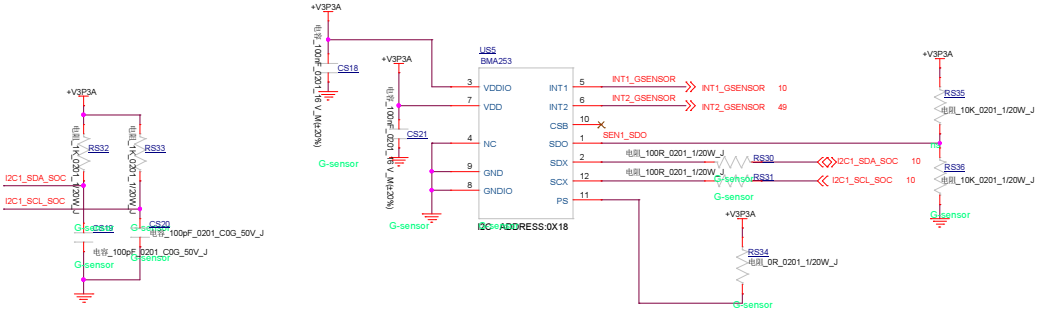

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Size: A4	Project Name: NB8513	REV: V1.0
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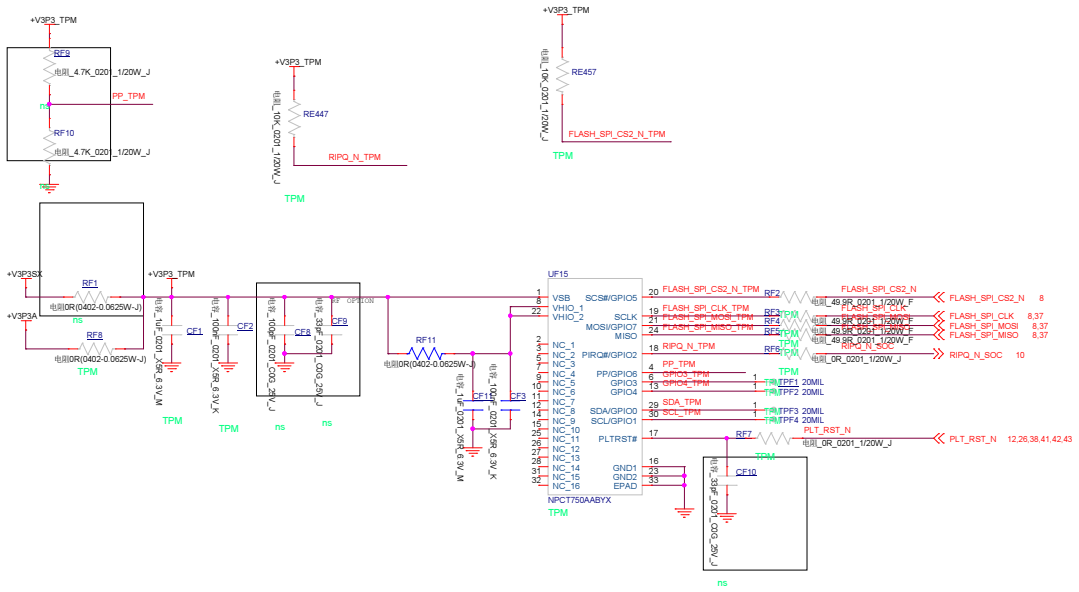

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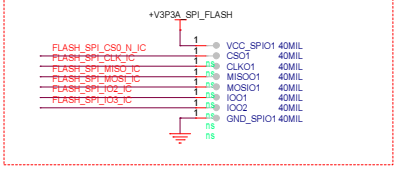
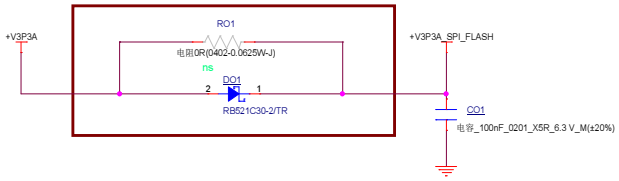
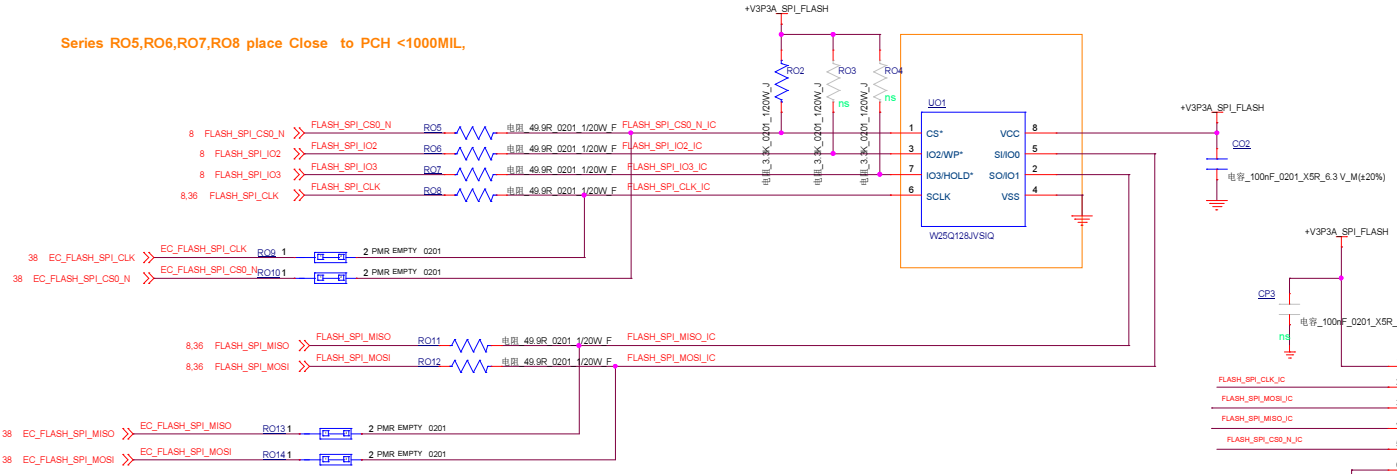
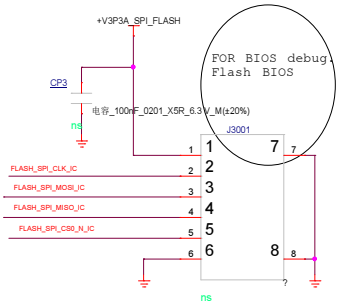
FOR product line





Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,





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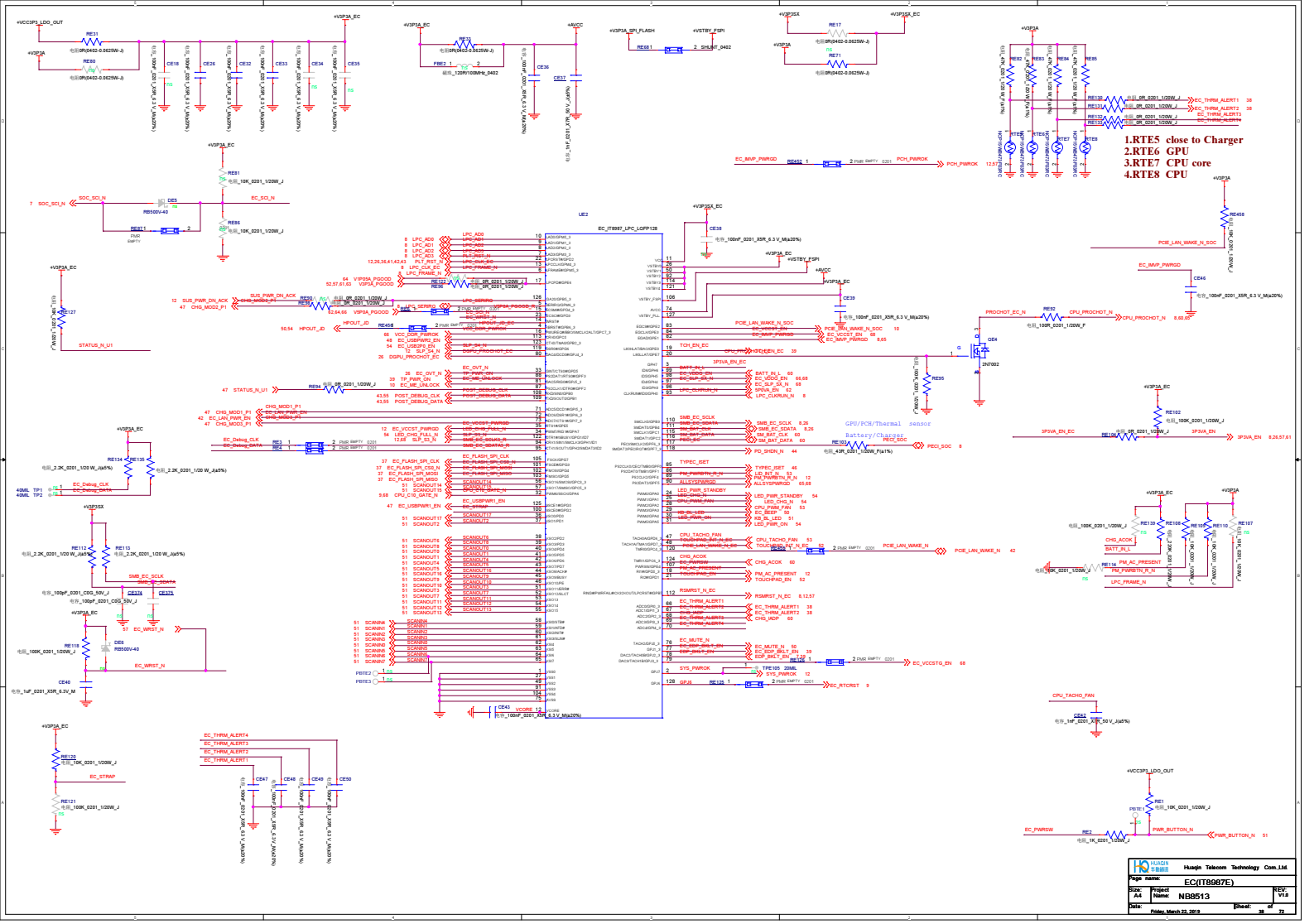

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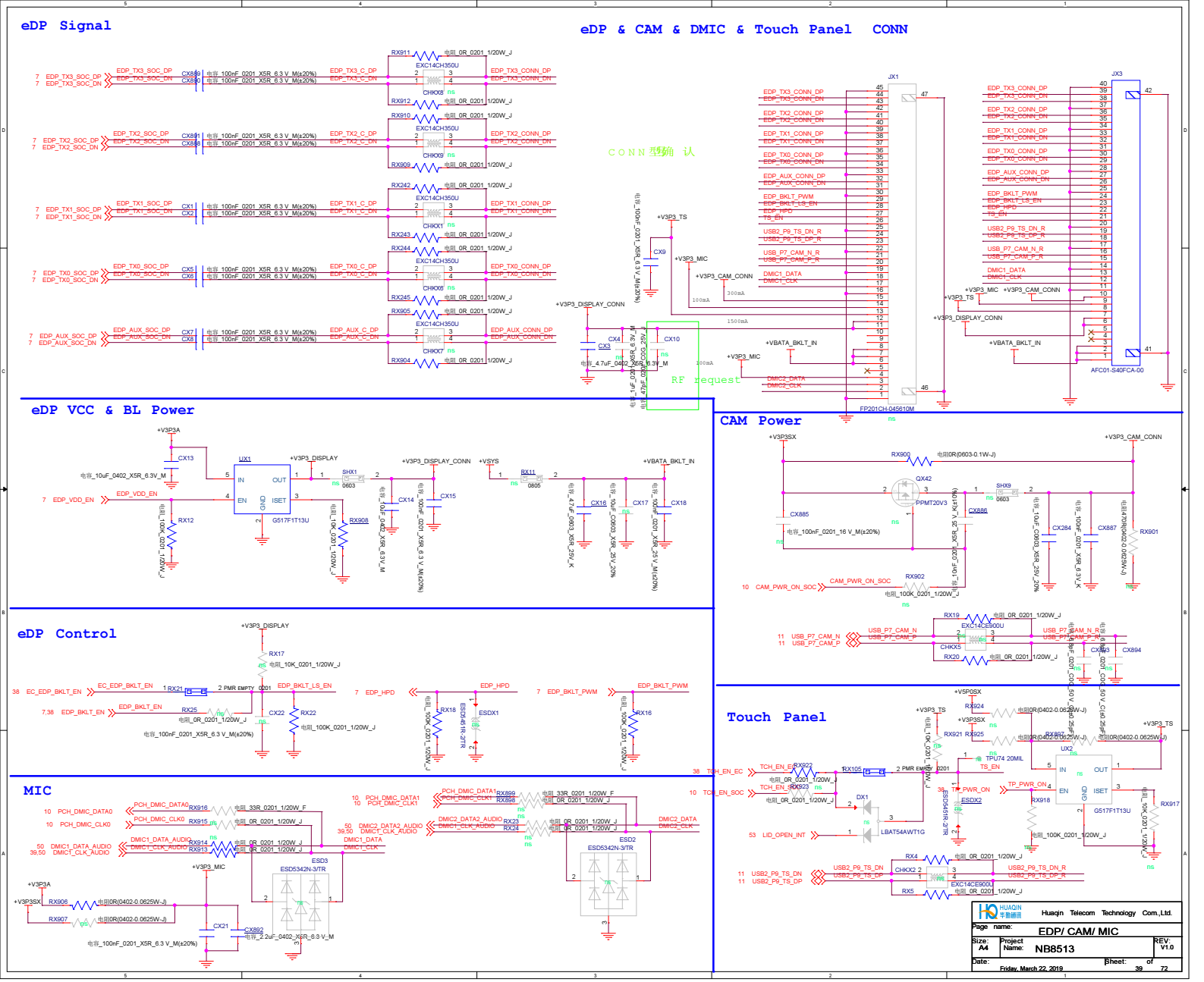
eDP Signal
eDP & CAM & DMIC & Touch Panel CONN
eDP VCC & BL Power
CAM Power
eDP Control
Touch Panel
MIC
CONN型确认
RF request
Huaqin Telecom Technology Com.,Ltd.
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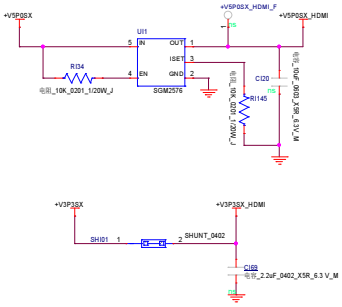
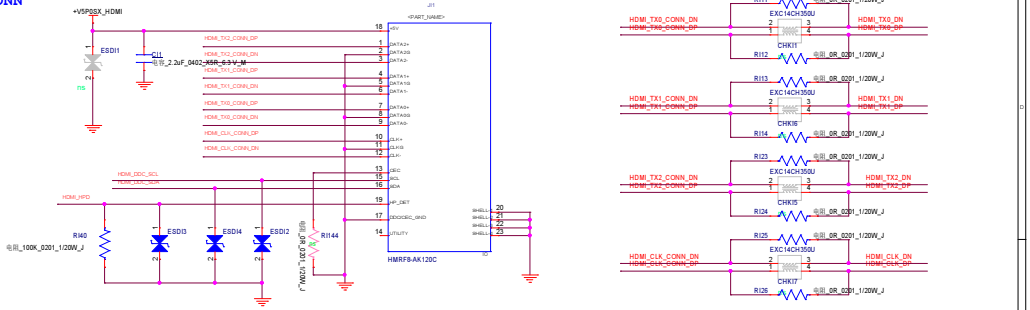
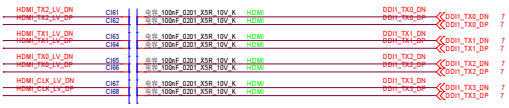
Power 1



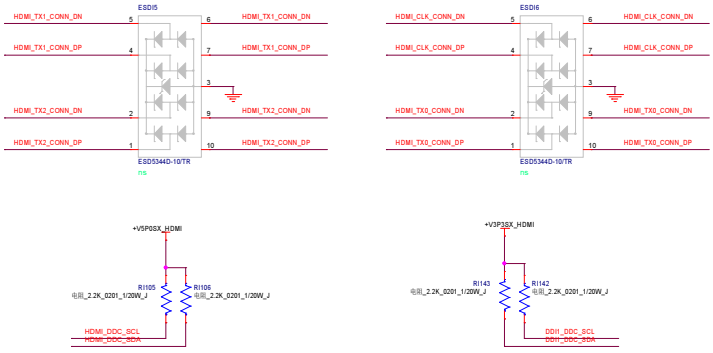
HDMI CONN

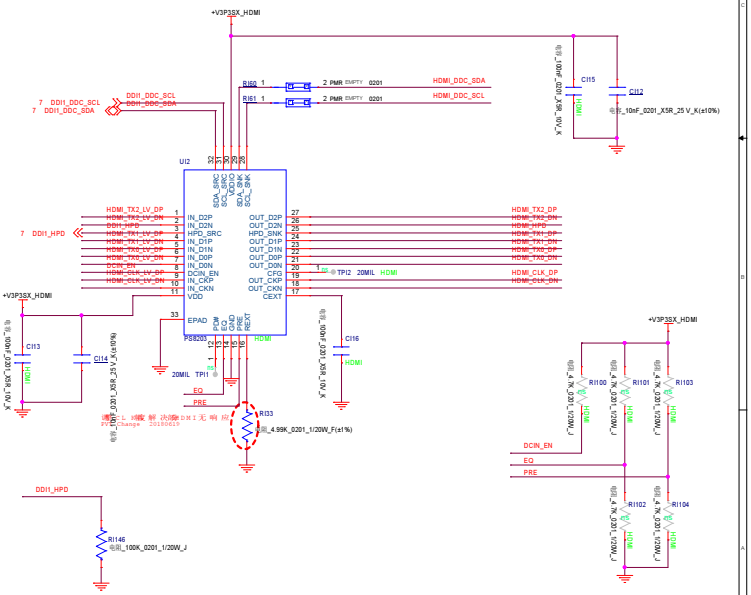


Signal



ESD





Huaqin Telecom Technology Com.,Ltd.			
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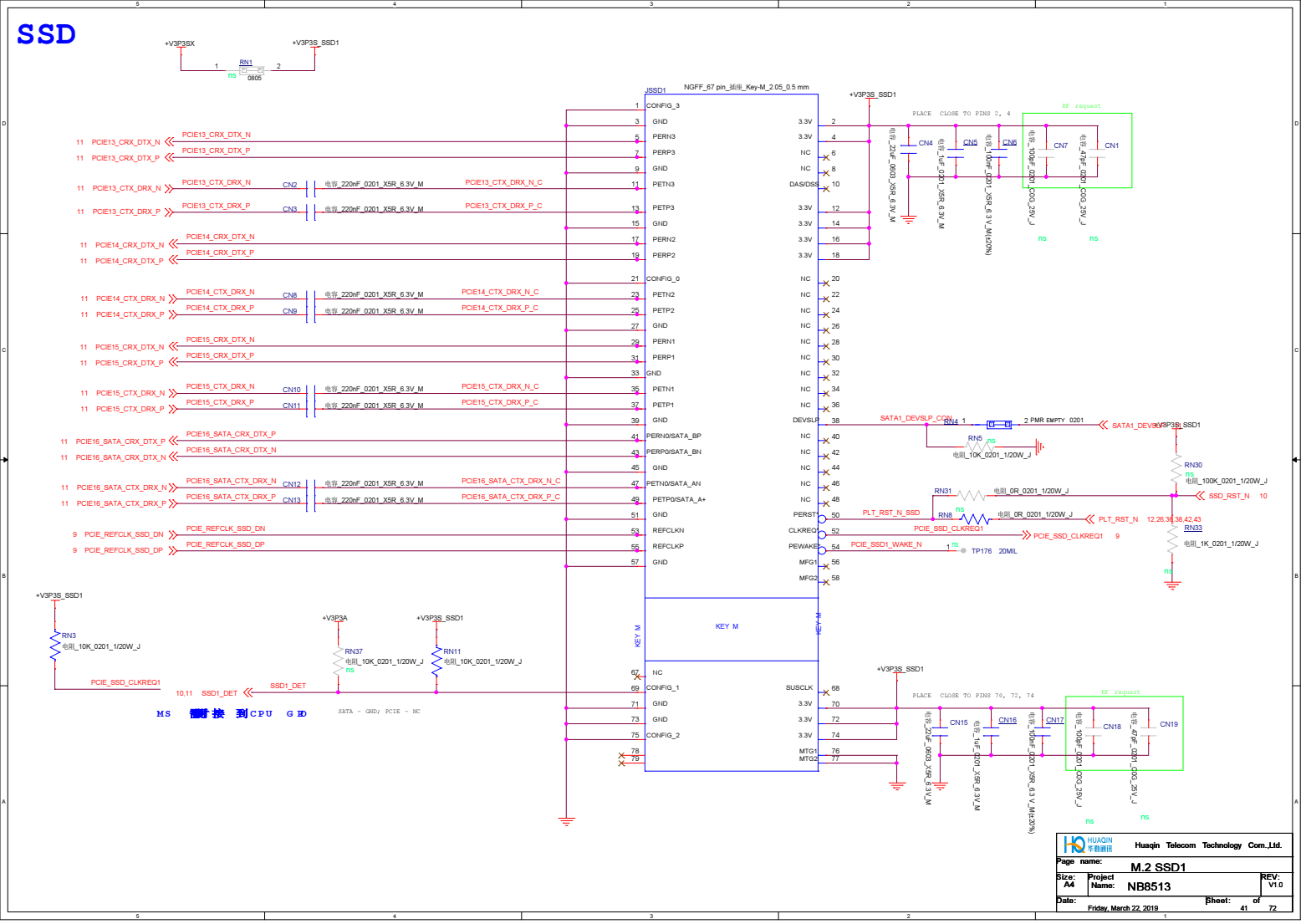
SSD



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Page name:	M.2 SSD1	
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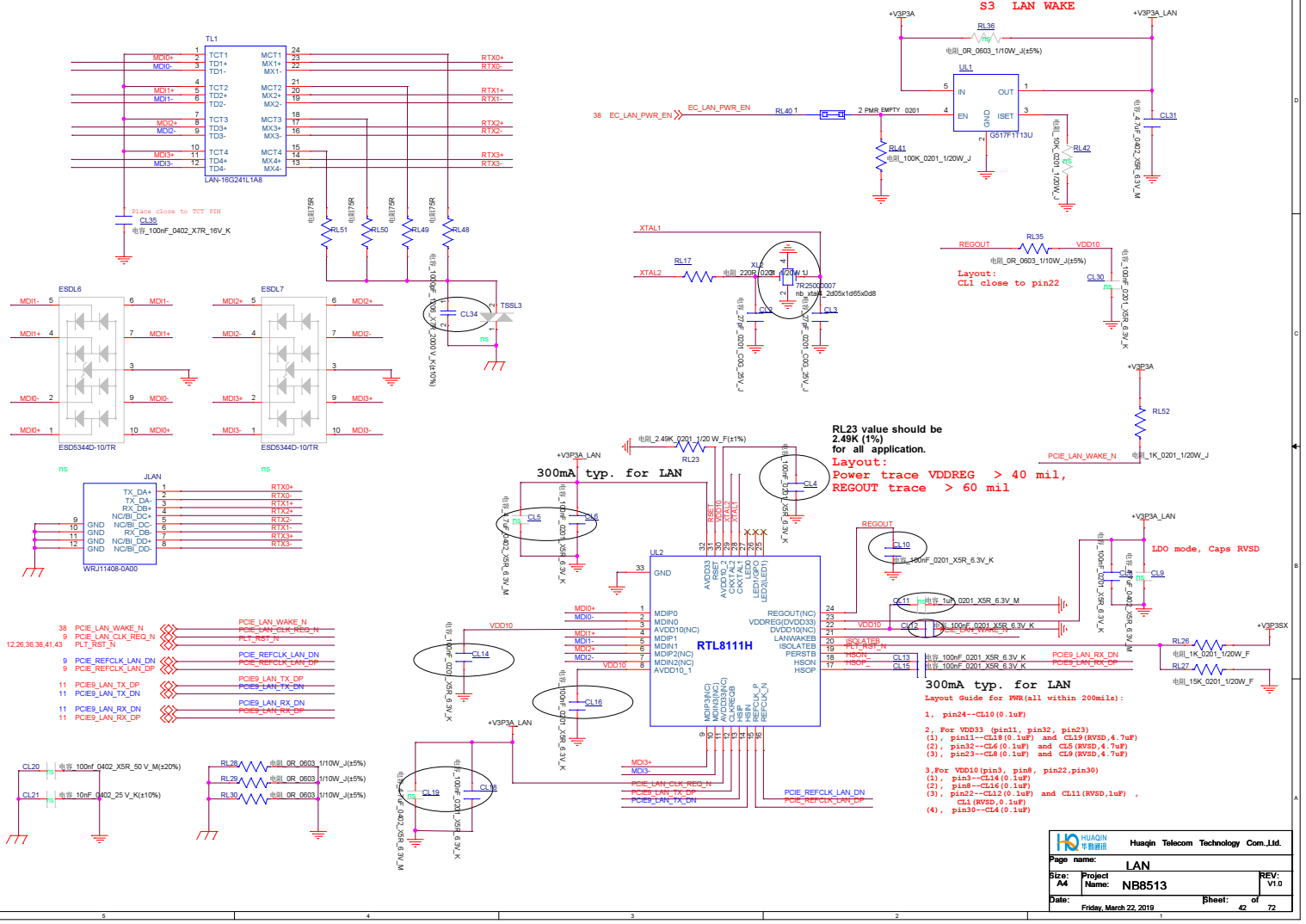
Suport AC S5 S4 LAN WAKE
S3 LAN WAKE



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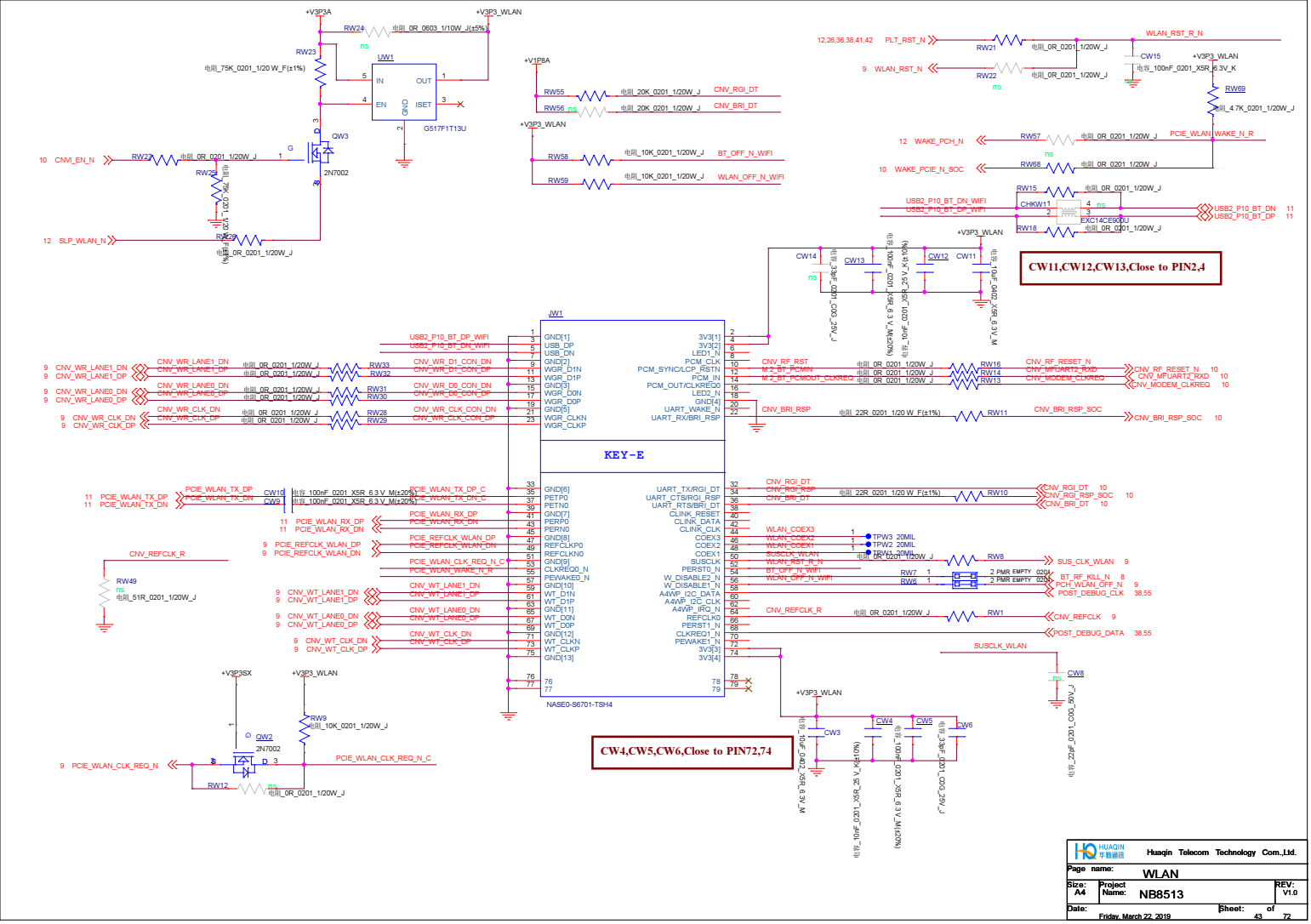
CW11,CW12,CW13,Close to PIN2,4
CW4,CW5,CW6,Close to PIN72,74
KEY-E
NASE0-S6701-TSH4
Husqin Telecom Technology Com.,Ltd.
Page name: WLAN
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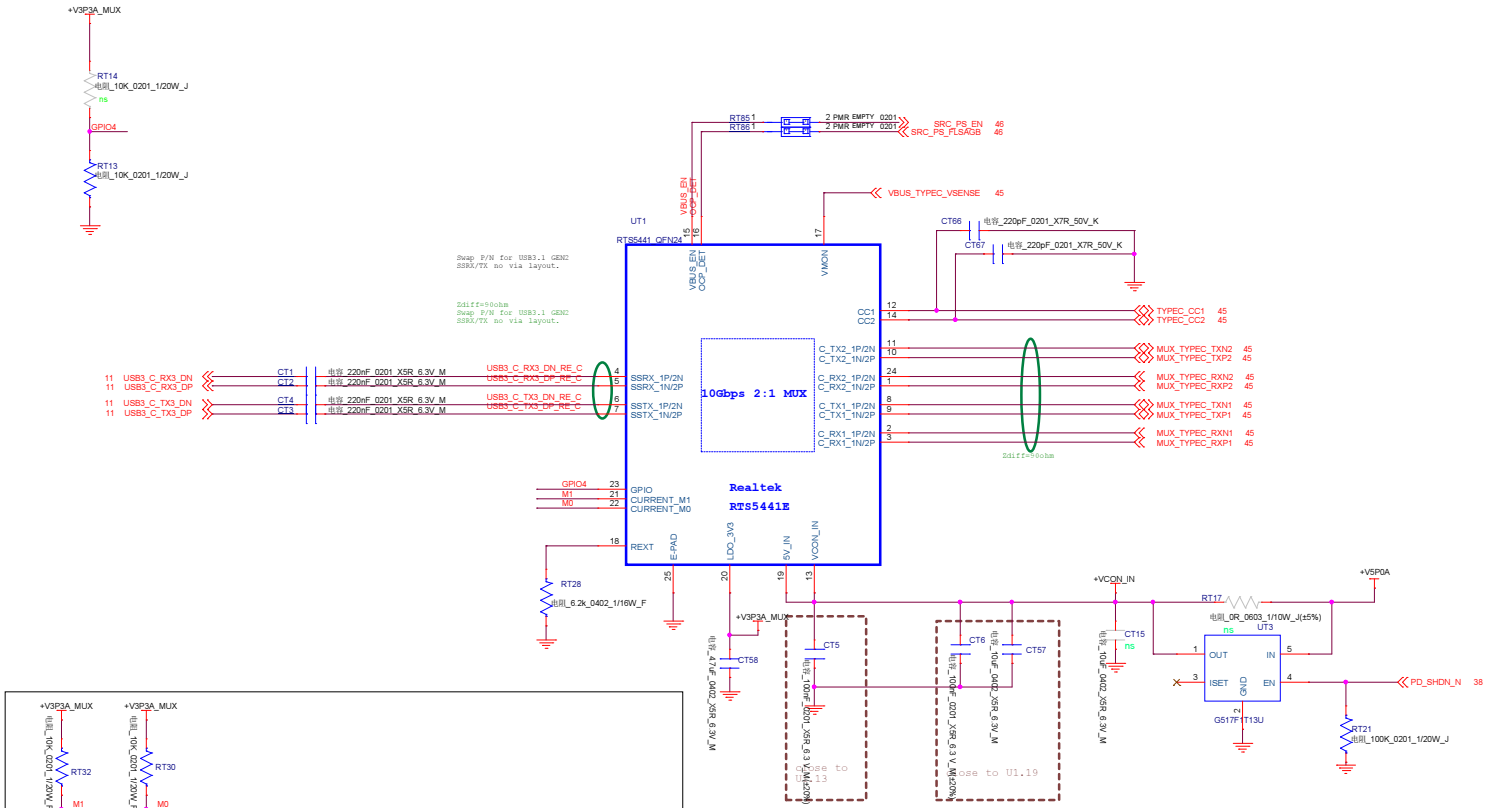

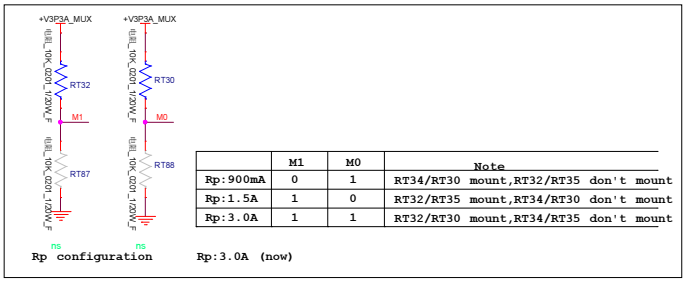

	M1	M0	Note
Rp:900mA	0	1	RT34/RT30 mount,RT32/RT35 don't mount
Rp:1.5A	1	0	RT32/RT35 mount,RT34/RT30 don't mount
Rp:3.0A	1	1	RT32/RT30 mount,RT34/RT35 don't mount

HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	Type C Controller	
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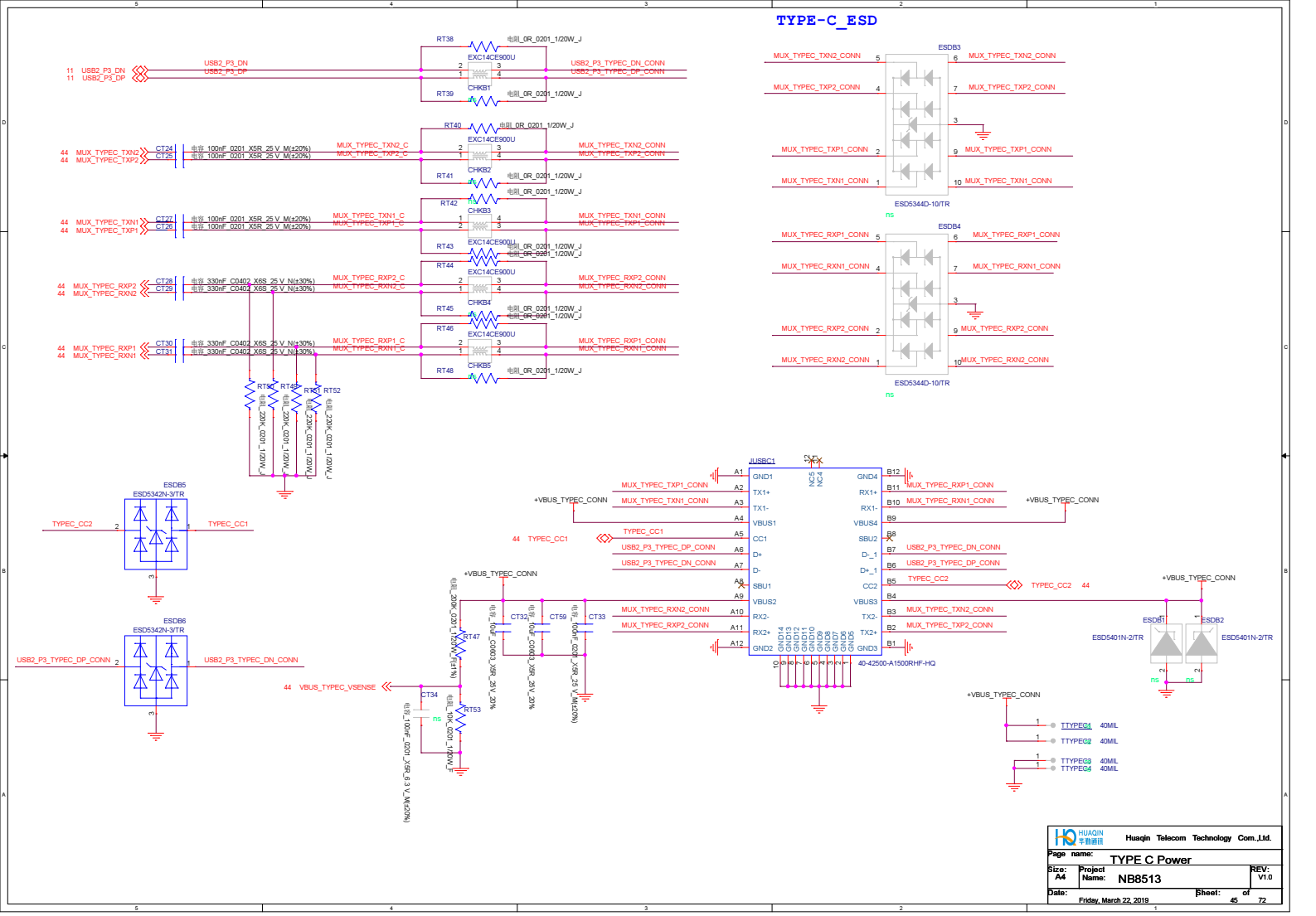
TYPE-C_ESD



Huaqin Telecom Technology Com.,Ltd.	
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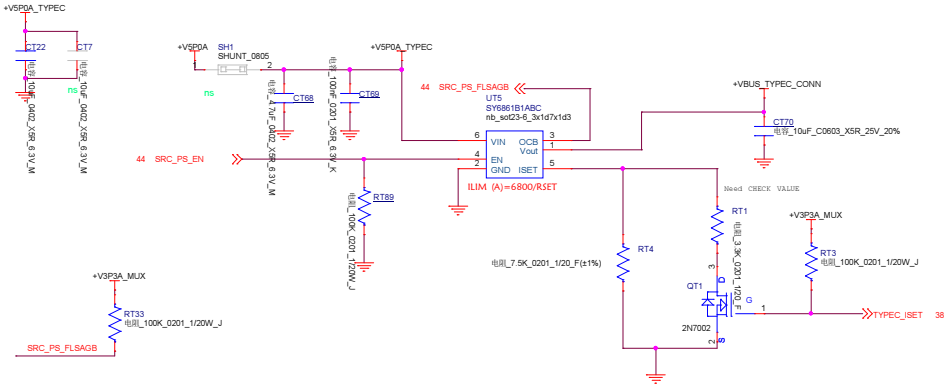

HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
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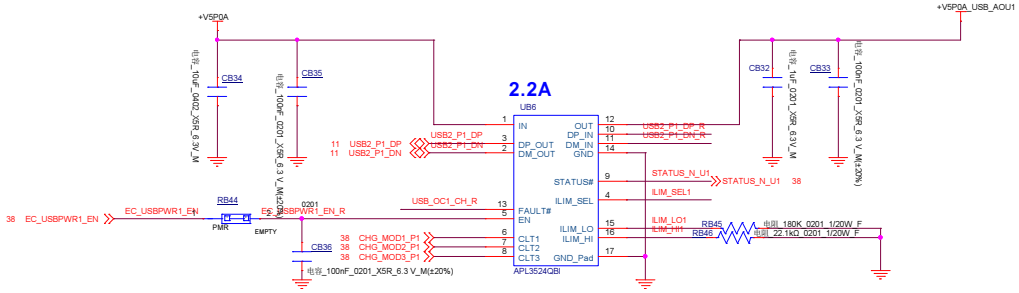
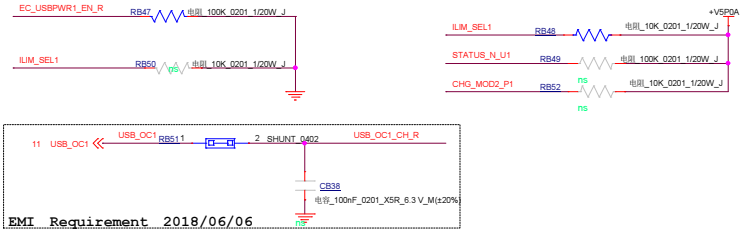
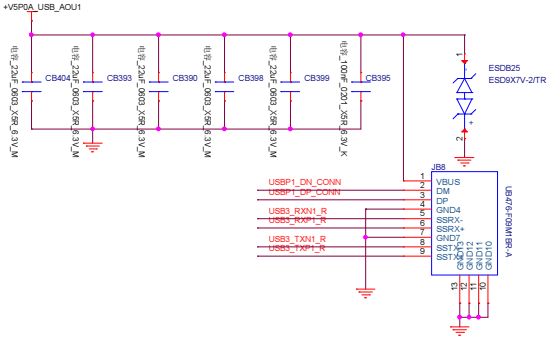
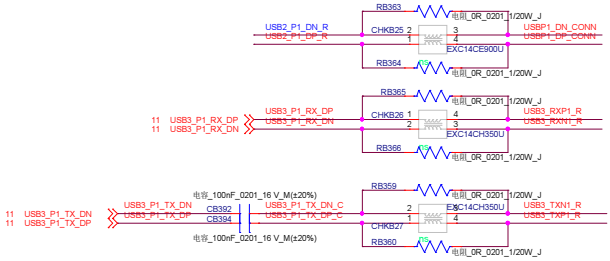
USB3.1 POWER Port1



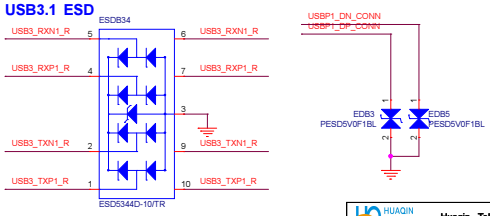




USB3.1 Signal



USB3.1 ESD



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	TYPE-C PD & MUX	
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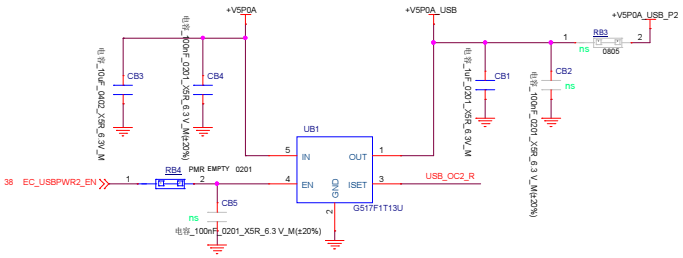
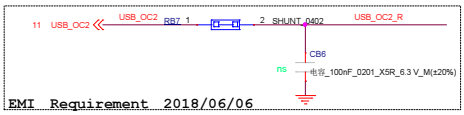
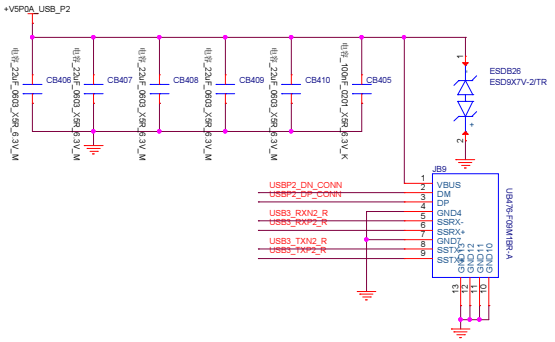
USB3.1 POWER Port2

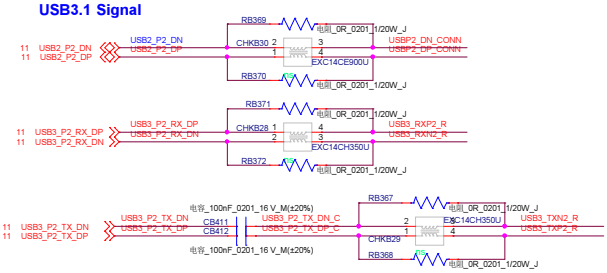




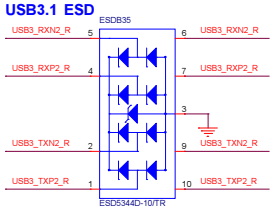
HUANWULIAO

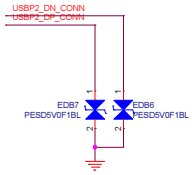


USB3.1 Signal



USB3.1 ESD





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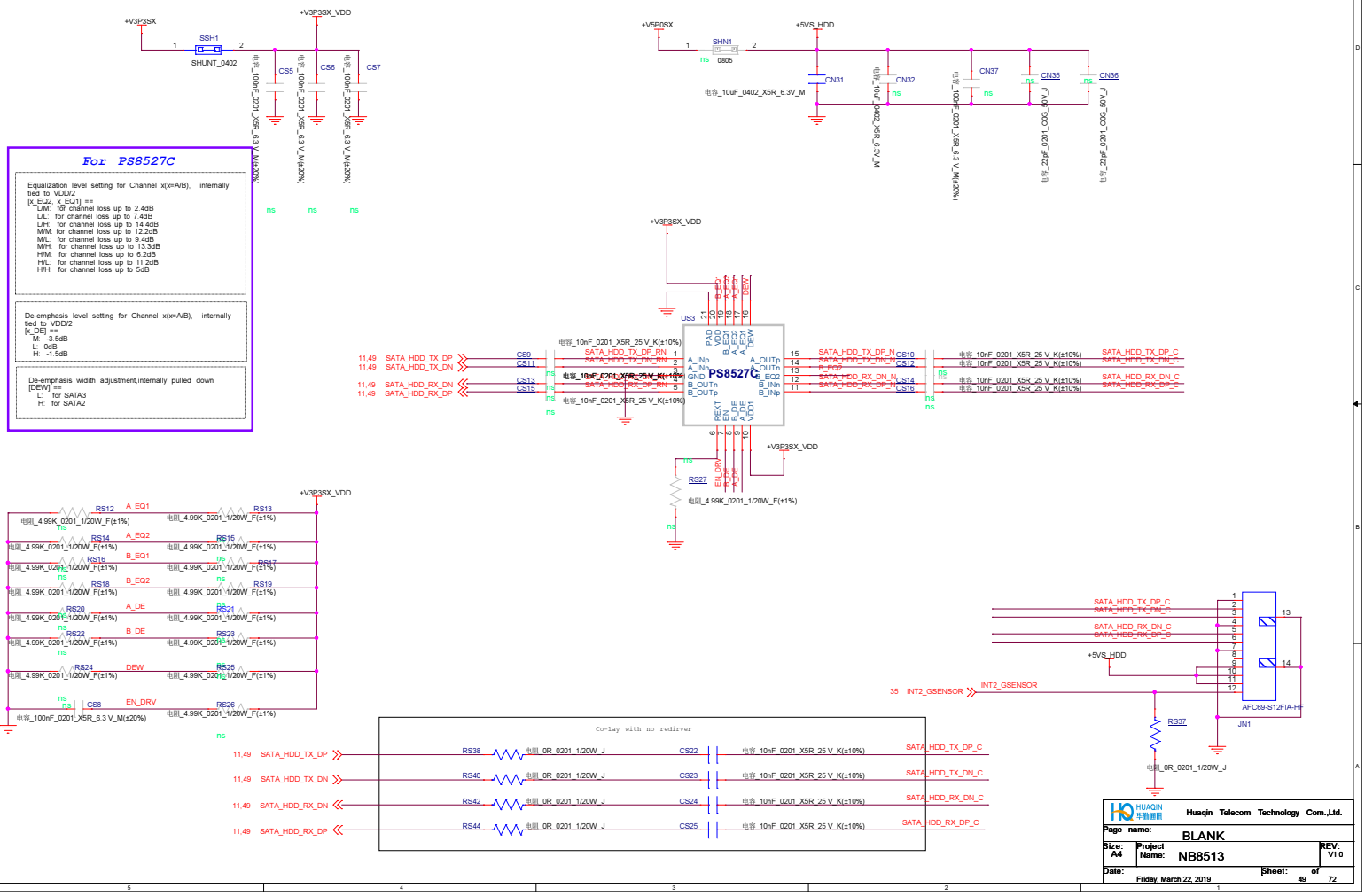
HDD


For PS8527C
Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2 ,x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB
L: 0dB
H: -1.5dB
De-emphasis width adjustment,internally pulled down
[DEW] ==
L: for SATA3
H: for SATA2
+V3P3SX
+V3P3SX_VDD
SSH1
SHUNT_0402
CS5
CS6
CS7
+V5P0SX
+5VS_HDD
SHN1
CN31
CN32
CN37
CN35
CN36
US3
PS8527C
SATA_HDD_TX_DP
SATA_HDD_TX_DN
SATA_HDD_RX_DN
SATA_HDD_RX_DP
SATA_HDD_TX_DP_C
SATA_HDD_TX_DN_C
SATA_HDD_RX_DN_C
SATA_HDD_RX_DP_C
RS27
RS12
RS13
RS14
RS15
RS16
RS17
RS18
RS19
RS20
RS21
RS22
RS23
RS24
RS25
RS26
CS8
A_EQ1
A_EQ2
B_EQ1
B_EQ2
A_DE
B_DE
DEW
EN_DRV
Co-lay with no redirver
RS38
RS40
RS42
RS44
CS22
CS23
CS24
CS25
SATA_HDD_TX_DP_C
SATA_HDD_TX_DN_C
SATA_HDD_RX_DN_C
SATA_HDD_RX_DP_C
INT2_GSENSOR
RS37
AFC69-S12FIA-HF
JN1
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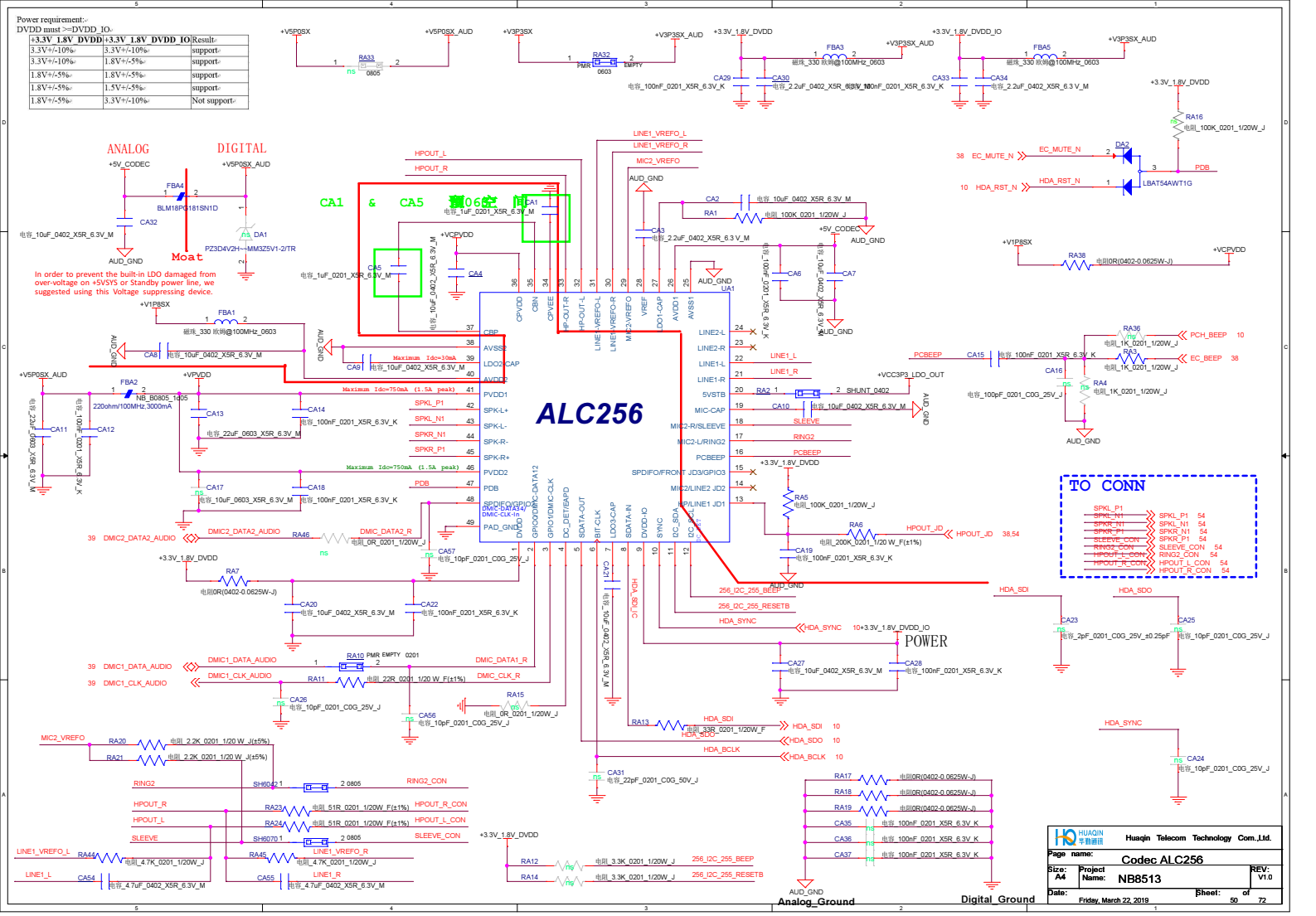
Power requirement:

DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support



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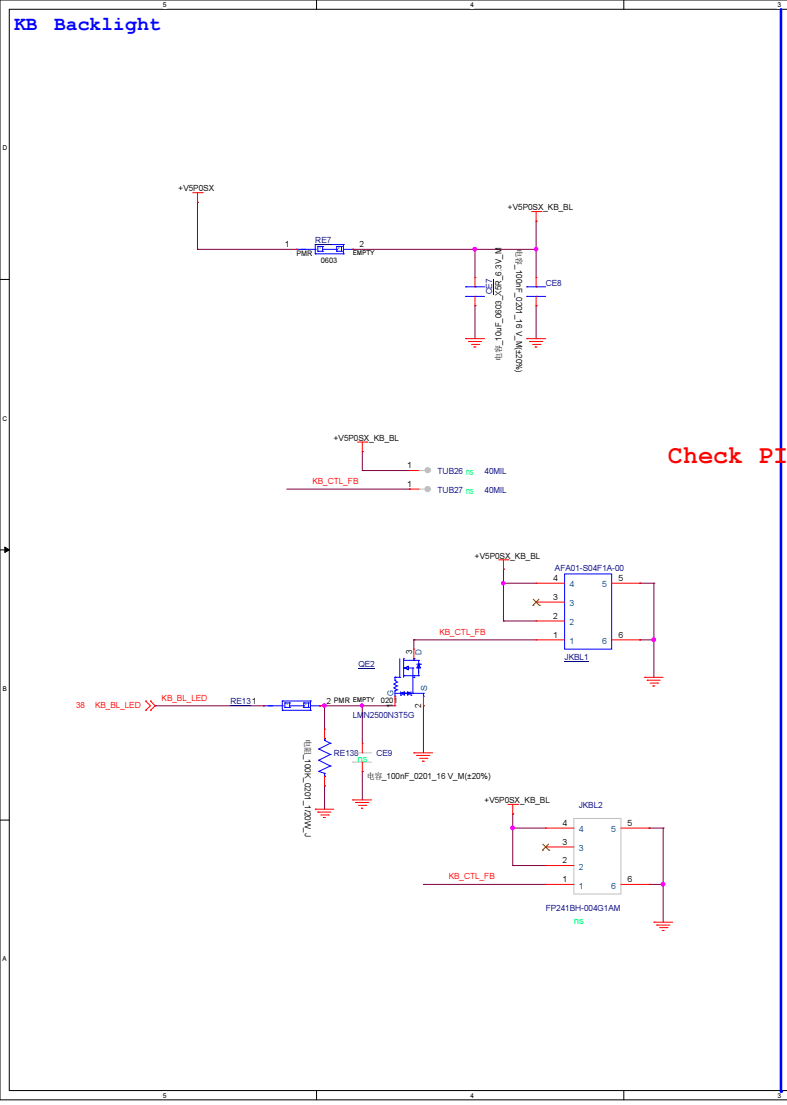
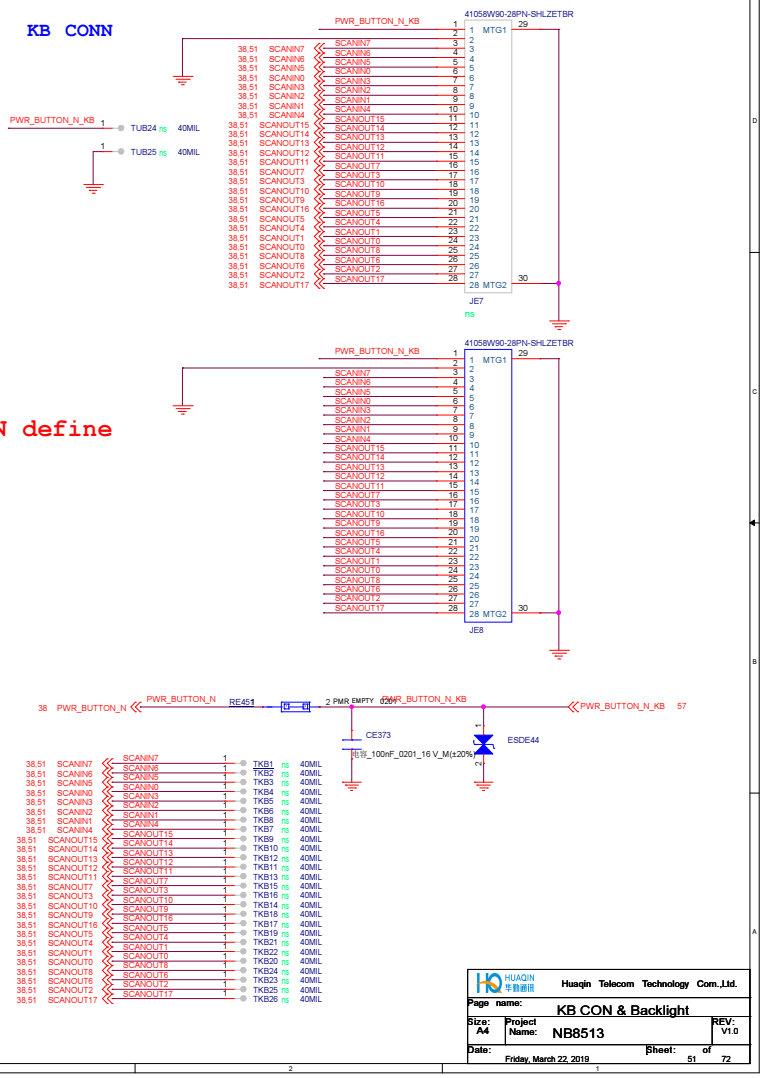


Check PIN define



38,51	SCANIN7	SCANIN7	1	TKB1	ns	40MIL			
38,51	SCANIN6	SCANIN6	1	TKB2	ns	40MIL			
38,51	SCANIN5	SCANIN5	1	TKB3	ns	40MIL			
38,51	SCANIN0	SCANIN0	1	TKB4	ns	40MIL			
38,51	SCANIN3	SCANIN3	1	TKB5	ns	40MIL			
38,51	SCANIN2	SCANIN2	1	TKB6	ns	40MIL			
38,51	SCANIN1	SCANIN1	1	TKB8	ns	40MIL			
38,51	SCANIN4	SCANIN4	1	TKB7	ns	40MIL			
38,51	SCANOUT15	SCANOUT15	1	TKB9	ns	40MIL			
38,51	SCANOUT14	SCANOUT14	1	TKB10	ns	40MIL			
38,51	SCANOUT13	SCANOUT13	1	TKB12	ns	40MIL			
38,51	SCANOUT12	SCANOUT12	1	TKB11	ns	40MIL			
38,51	SCANOUT11	SCANOUT11	1	TKB13	ns	40MIL			
38,51	SCANOUT7	SCANOUT7	1	TKB15	ns	40MIL			
38,51	SCANOUT3	SCANOUT3	1	TKB16	ns	40MIL			
38,51	SCANOUT10	SCANOUT10	1	TKB14	ns	40MIL			
38,51	SCANOUT9	SCANOUT9	1	TKB18	ns	40MIL			
38,51	SCANOUT16	SCANOUT16	1	TKB17	ns	40MIL			
38,51	SCANOUT5	SCANOUT5	1	TKB19	ns	40MIL			
38,51	SCANOUT4	SCANOUT4	1	TKB21	ns	40MIL			
38,51	SCANOUT1	SCANOUT1	1	TKB22	ns	40MIL			
38,51	SCANOUT0	SCANOUT0	1	TKB20	ns	40MIL			
38,51	SCANOUT8	SCANOUT8	1	TKB24	ns	40MIL			
38,51	SCANOUT6	SCANOUT6	1	TKB23	ns	40MIL			
38,51	SCANOUT2	SCANOUT2	1	TKB25	ns	40MIL			
38,51	SCANOUT17	SCANOUT17	1	TKB26	ns	40MIL			

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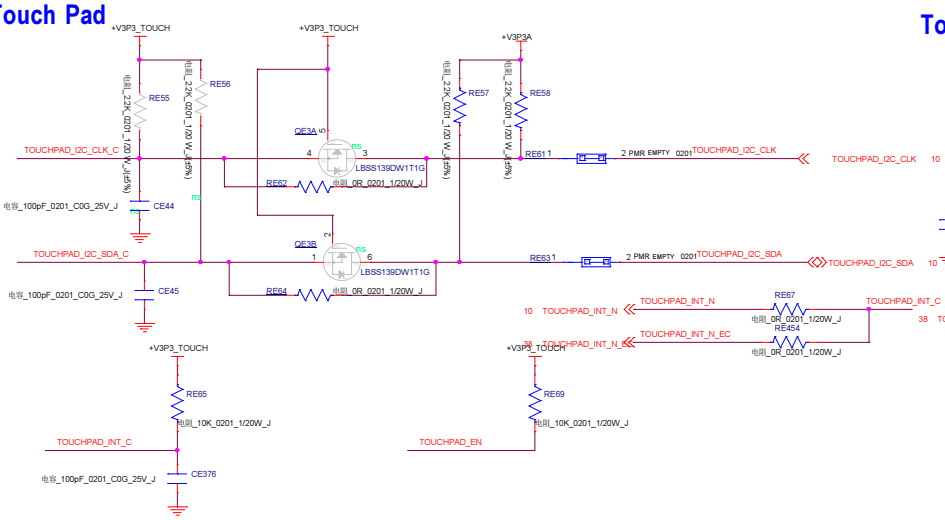
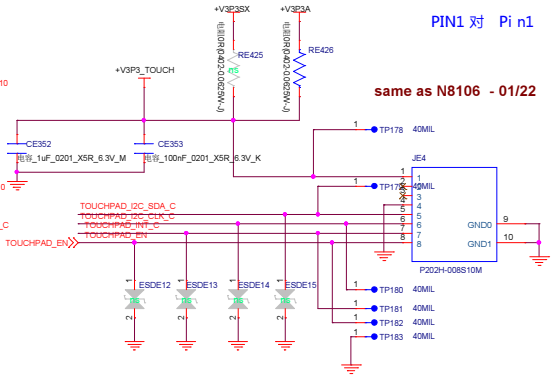
Touch Pad



Touch Pad CONN

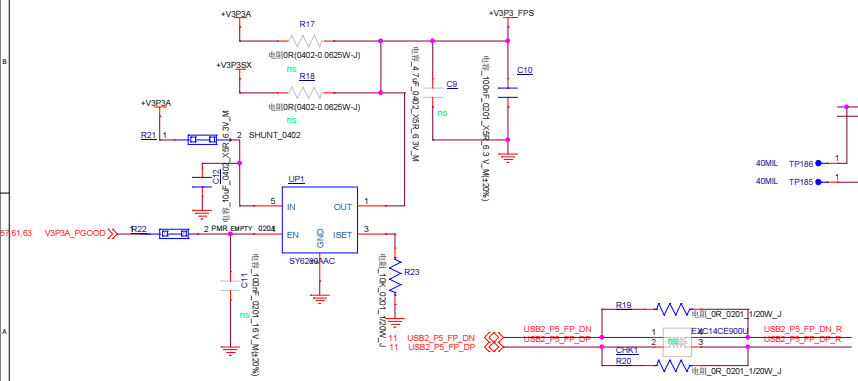
PIN1 对 Pi n1

same as N8106 - 01/22

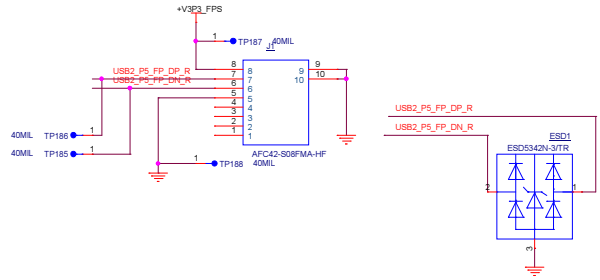


目 前 按 照 同 面 线定 义 ，待 ME u pde最 同面线

Finger Print



Finger Print CONN



Huaqin Telecom Technology Com.,Ltd.		
Page name:	TouchPad/ Finger Print	
Size: A4	Project Name: NB8513	REV: V1.0
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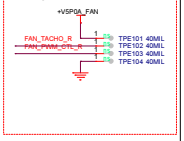
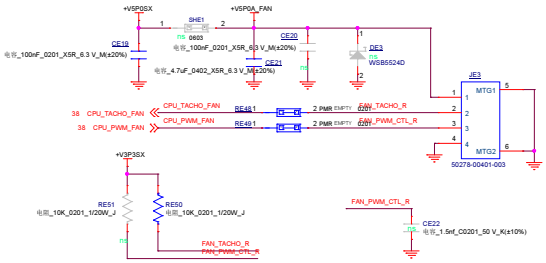
Voice input with LED

FAN CONN

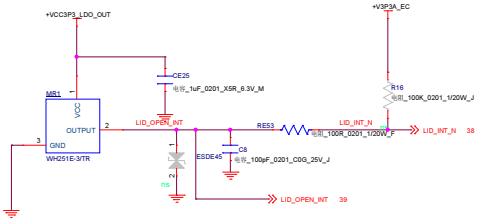
FOR product line



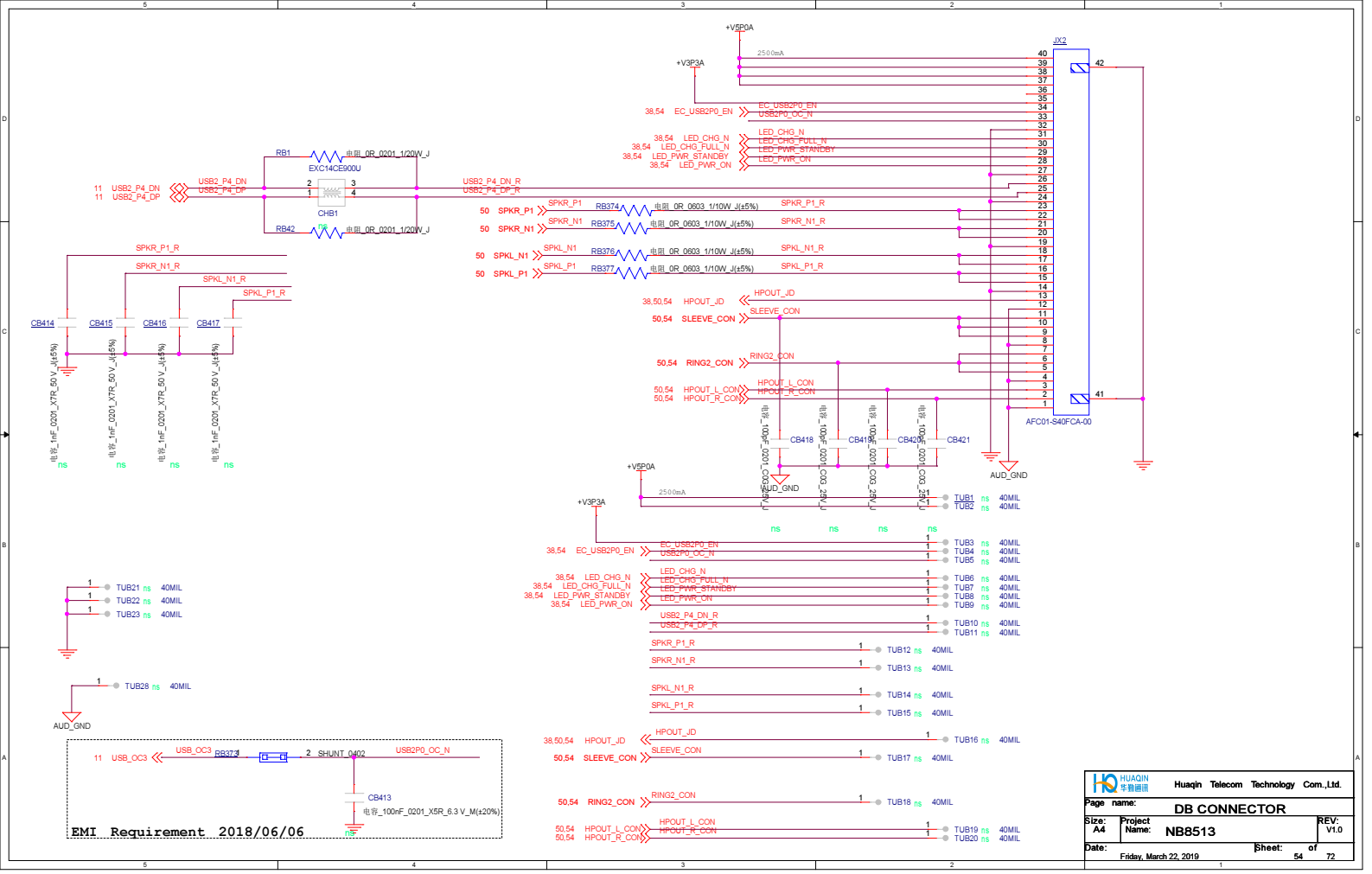


确认 PIN顺序

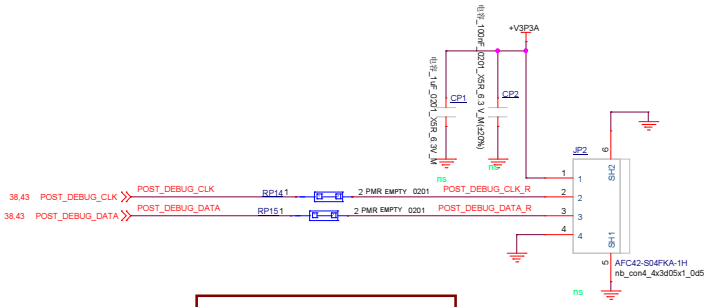
HALL



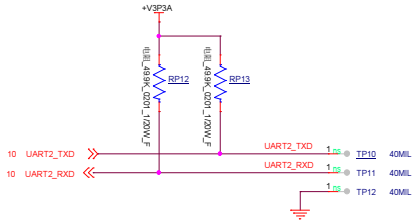
Huaqin Telecom Technology Com.,Ltd.		
Page name:	G-SENSOR/FAN/LED/Hall	
Size: A4	Project Name: NB8513	REV: V1.0
Date: Friday, March 22, 2019	Sheet: 53 of 72	



Huaqin Telecom Technology Com.,Ltd.	
Page name:	DB CONNECTOR
Size: A4	Project Name: NB8513
REV: V1.0	
Date: Friday, March 22, 2019	Sheet: 54 of 72



add test point - 01/18



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	Debug Conn	
Size: A4	Project Name: NB8513	REV: V1.0
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HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.		
Page name:	Thermal sensor		
Size: A4	Project Name:	NB8513	REV: V1.0
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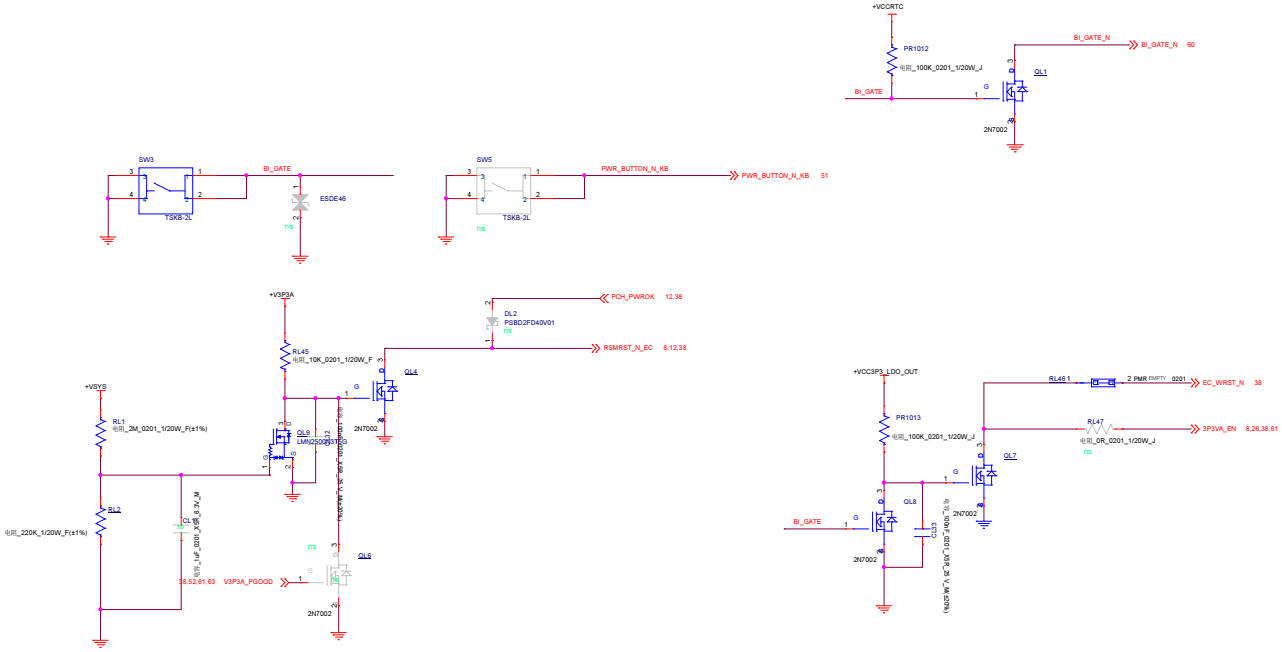
Reset BUTTON



Huaqin Telecom Technology Com.,Ltd.			
Page name:	Hole/ Mark		
Size: A4	Project Name:	NB8513	REV: V1.0
Date: Friday, March 22, 2019		Sheet: 57 of 72	

Need add HQ CODE and Stuff

螺母元件

HS1 HOLE_3D5_6_P HOLE_3D5_6_P
HS2 HOLE_3D5_6_P HOLE_3D5_6_P
HS3 HOLE_3D5_6_P HOLE_3D5_6_P
HS4 HOLE_3D5_6_P HOLE_3D5_6_P
HS5 HOLE_3D5_6_P HOLE_3D5_6_P
HS6 HOLE_3D5_6_P HOLE_3D5_6_P

Thermal

H1 hole_4_6_7 HOLE276R142
H2 hole_4_6_7 HOLE276R142
H4 hole_4_6_7 HOLE276R142
H3 hole_4_6_7 HOLE276R142
H5 hole_4_6_7 HOLE276R142
H6 hole_4_6_7 HOLE276R162
H7 hole_4_6_7 HOLE315R221

ns

HOLE *14

HS1+ 贴片弹片_3.4*D4.2_3.4 mm <PCB Footprint>
Part Reference = HS2+ 贴片弹片_3.4*D4.2_3.4 mm <PCB Footprint>
HS3+ 贴片弹片_3.4*D4.2_3.4 mm <PCB Footprint>
HS4+ 贴片弹片_3.4*D4.2_3.4 mm <PCB Footprint>
HS5+ 贴片弹片_3.4*D4.2_3.4 mm <PCB Footprint>

CPU & GPU Boss

HS6+ 贴片弹片_3.3*D4.5_3.3 mm <PCB Footprint>

WLAN Boss

PCB
PCB
ZNB8513_主板PCB_V3_融宁博德

PCB

RTCBATT
PCB
CR2025-LH20106
ns

HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	BLANK	
Size: A4	Project Name: NB8513	REV: V1.0
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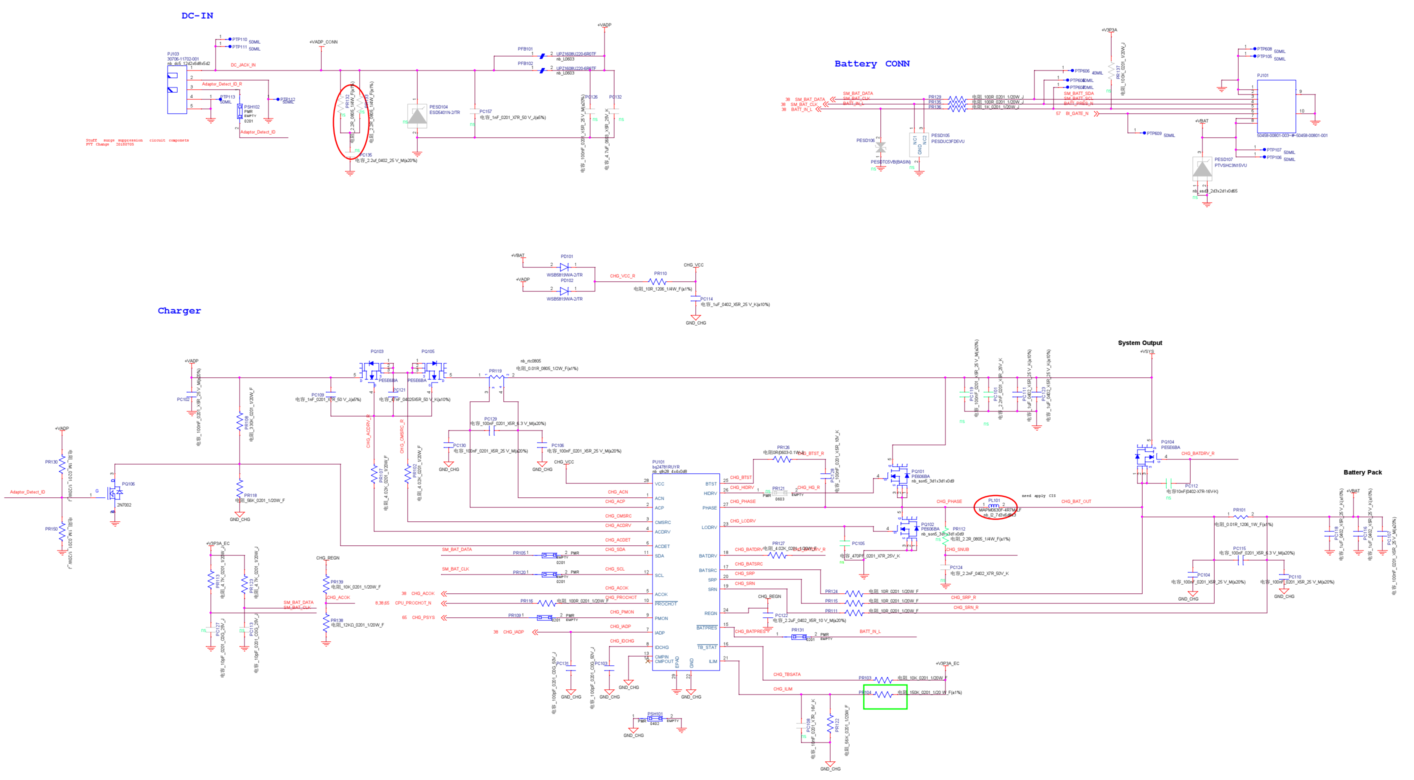
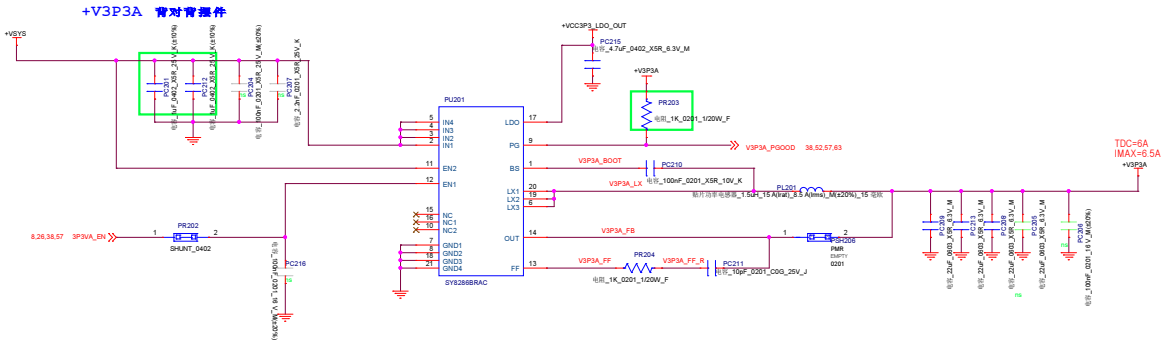
HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.		
Page name:	Power Map		
Size: A4	Project Name: NB8513		REV: V1.0
Date: Friday, March 22, 2019		Sheet: 59 of 72	



Huaqin Telecom Technology Com.,Ltd.		
Page name	BATTERY CHARGER	
Size: A4	Project Name: NB8513	REV V1.0
Date: Friday, March 22, 2019	Sheet 60 of 72	



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	POWER DELIVERY 3.3V	
Size: A4	Project Name: NB8513	REV: V1.0
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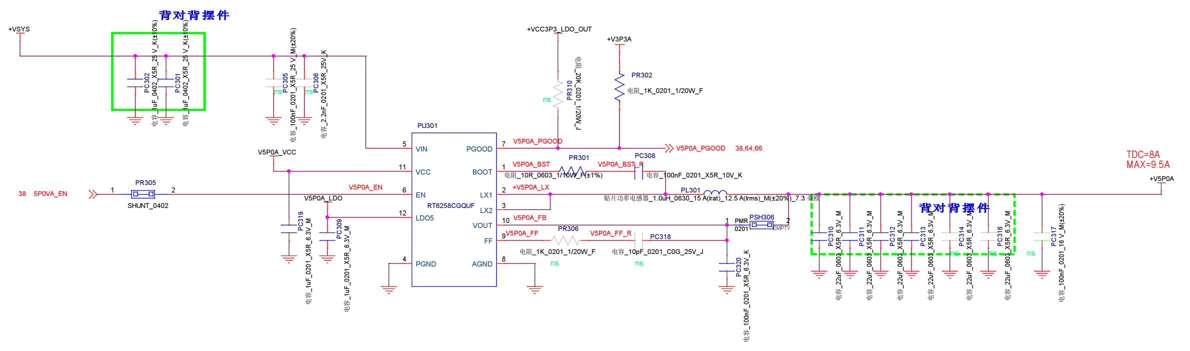

HUAQIN 华勤通讯 Huaqin Telecom Technology Com.,Ltd.

Page name:	POWER DELIVERY 5V	
Size: A4	Project Name: NB8513	REV: V1.0
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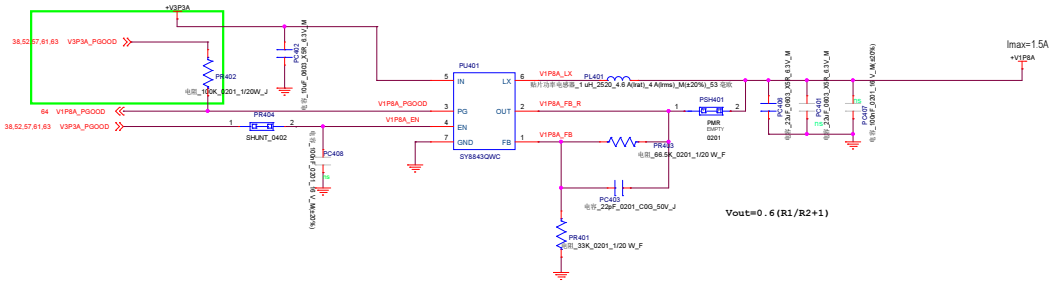
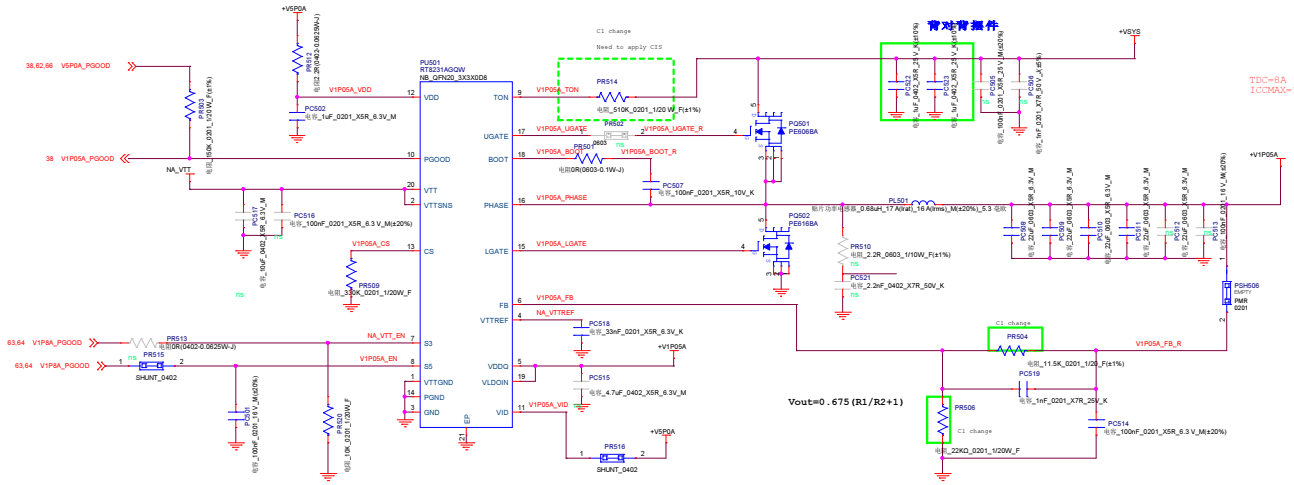
+V1P8A



Huaqin Telecom Technology Com.,Ltd.		
Page name:	POWER DELIVERY 1.8V	
Size: A4	Project Name: NB8513	REV: V1.0
Date: Friday, March 22, 2019	Sheet: 63 of 72	



Huaqin Telecom Technology Com.,Ltd.		
Page name:	POWER DELIVERY 1.0V	
Size: A4	Project Name: NB8513	REV: V1.0
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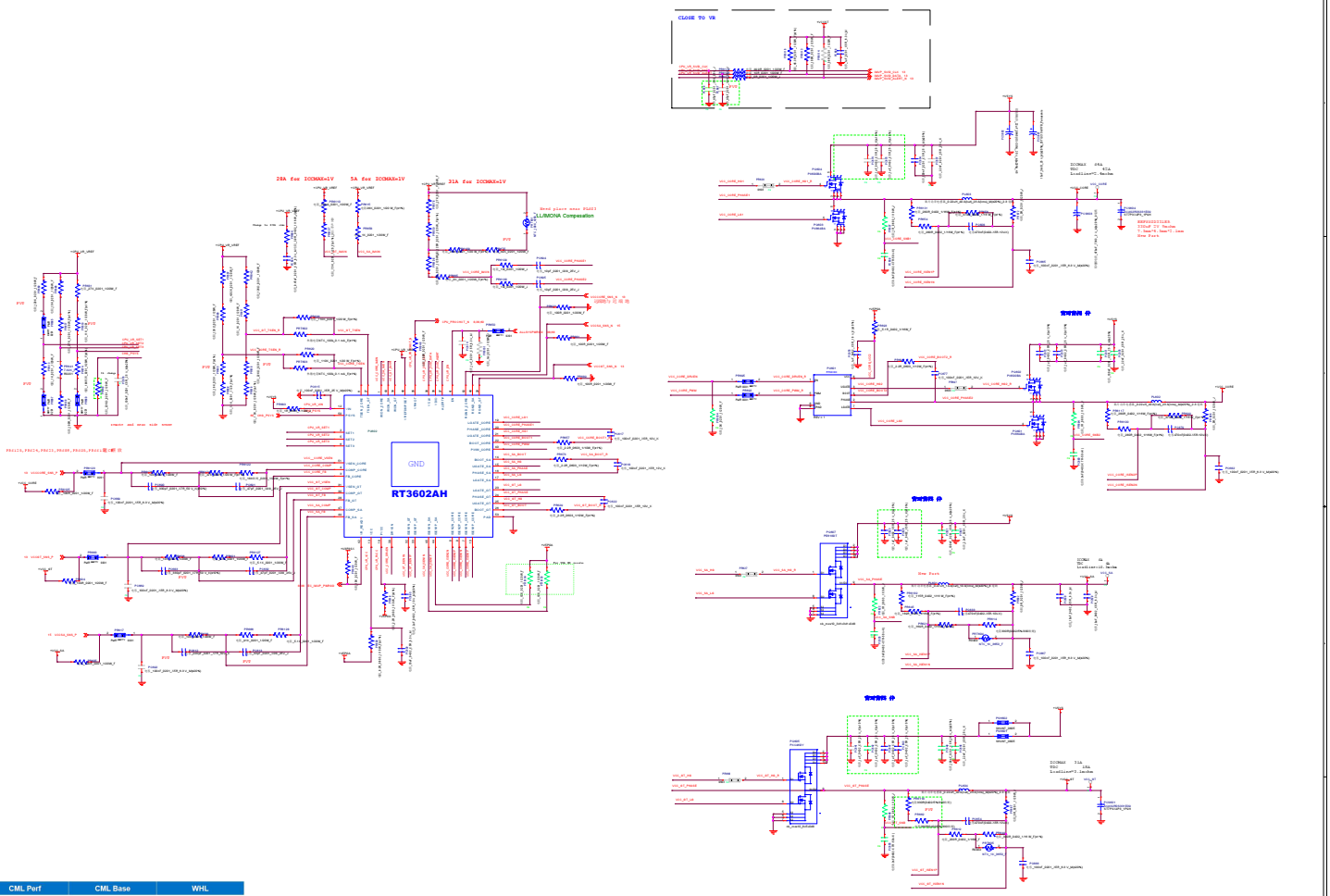
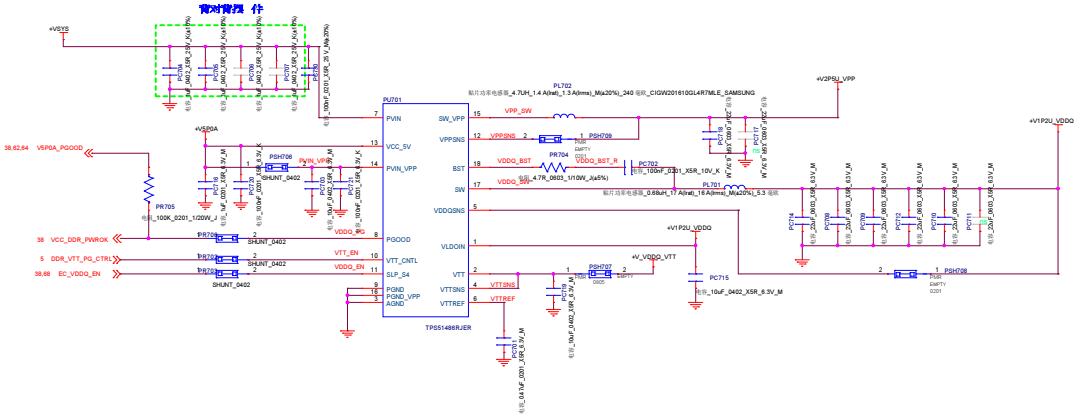


	CML Perf	CML Base	WHL
ICCMAX[A]	85	70	70
IPL2[A]	58	48	48
DC/AC LL[mΩ]	1.8	1.8	1.8
GT ICCMAX [A]	31	31	31
GT IPL2[A]	18	18	18
GT DC/AC LL[mΩ]	3.1	3.1	3.1
SA ICCMAX[A]	6	6	6
SA DC/AC LL[mΩ]	10.3	10.3	10.3
PL2 [W]	64	51	51
PL4 [W]	90	82	71
Tau [sec]	--	--	--



Huaqin Telecom Technology Com.,Ltd.			
Page name: POWER DELIVERY IMVP1			
Size: A4	Project Name: NB8513		REV: V1.0
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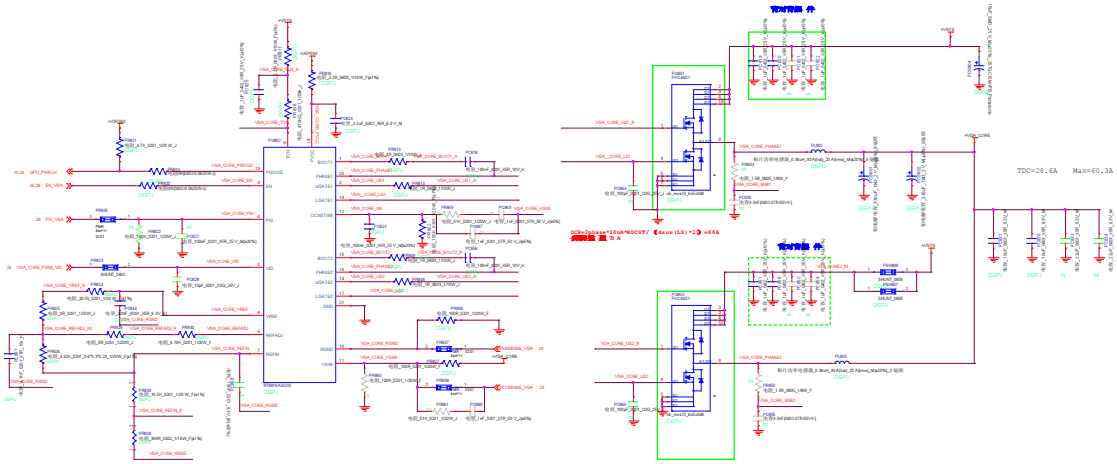


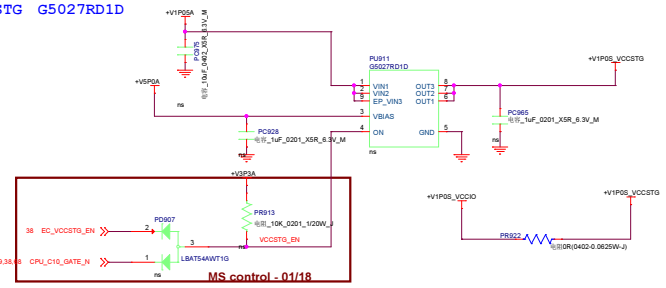
Table 7. Output EDP-Continuous

Product	NVVDD — (A)	GPU FBIO 1.35V[4] (A)	FB Total[4] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0[6]	27.8	3.2	5.8	0.2	0.5
N17S-G2[6]	28.6	3.2	5.8	0.2	0.5

Table 8. Output EDP-Peak

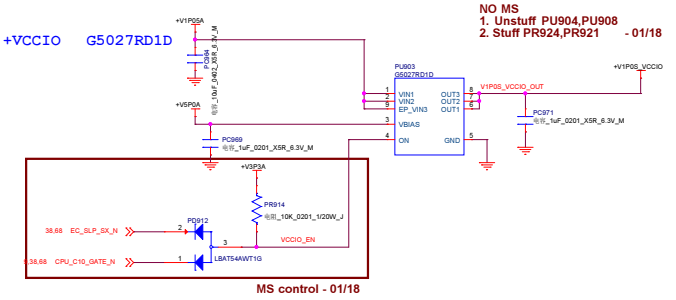
Product	NVVDD — (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-LG	48.3	2.8	5.8	0.2
N17S-G1	60.1	3.4	6.9	0.2
N17S-G0[5]	42.0	3.9	7.4	0.3
N17S-G2[5]	60.3	3.9	7.4	0.3

+VCCSTG G5027RD1D

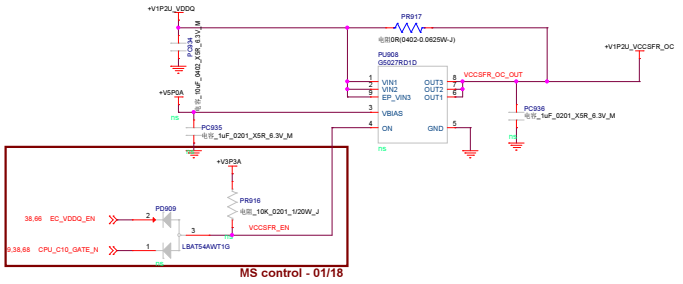


+VCCIO G5027RD1D

NO MS
1. Unstuff PU904,PU908
2. Stuff PR924,PR921 - 01/18



+V1P2U_VCCSFR_OC G5027RD1D

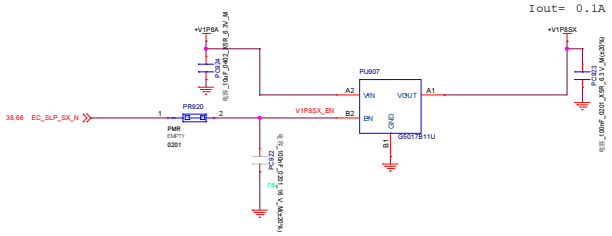


								VCCEOPIO ramp
tCPU33	All	CPU	PLT		240		us	11	CPU_C10_GATE# de-assertion to VCCPLL_OC stable

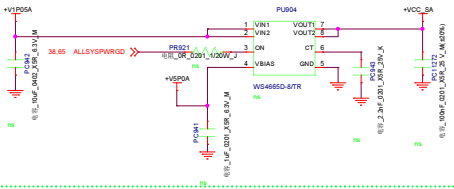
									Sx transitions
tCPU26	All	CPU	PLT	10	65		us	11	CPU_C10_GATE# de-assertion to VCCSTG stable Note: CPU_C10_GATE# de-assertion to VCCST also needs to meet max 65us on cold boot
tCPU27	All	CPU	PLT	10	240		us	11	CPU_C10_GATE# de-assertion to VCCIO stable
tCPU28a	All	CPU	PLT		200		us	36	SLP_S3# assertion to VCCST_PWRGD de-assertion
tCPU28b	All	CPU	PLT	0			us	37, 38	VCCST_PWRGD low to VCCST

+V1P8SX

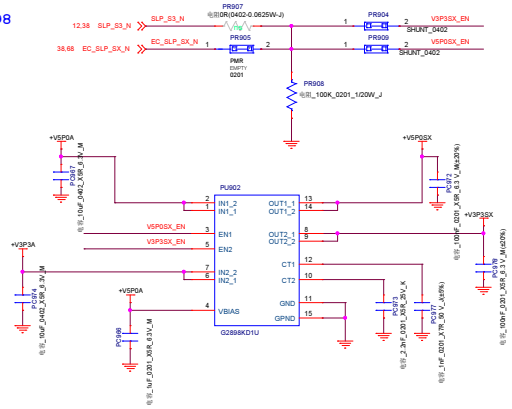
Iout= 0.1A



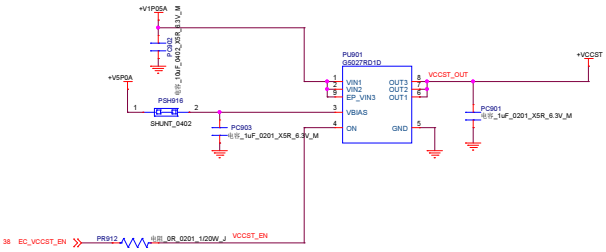
+VSA



+V3P3SX,+V5P0SX G2898



+VCCST G5027RD1D



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.		
Page name: POWER DELIVERY_Load switch			
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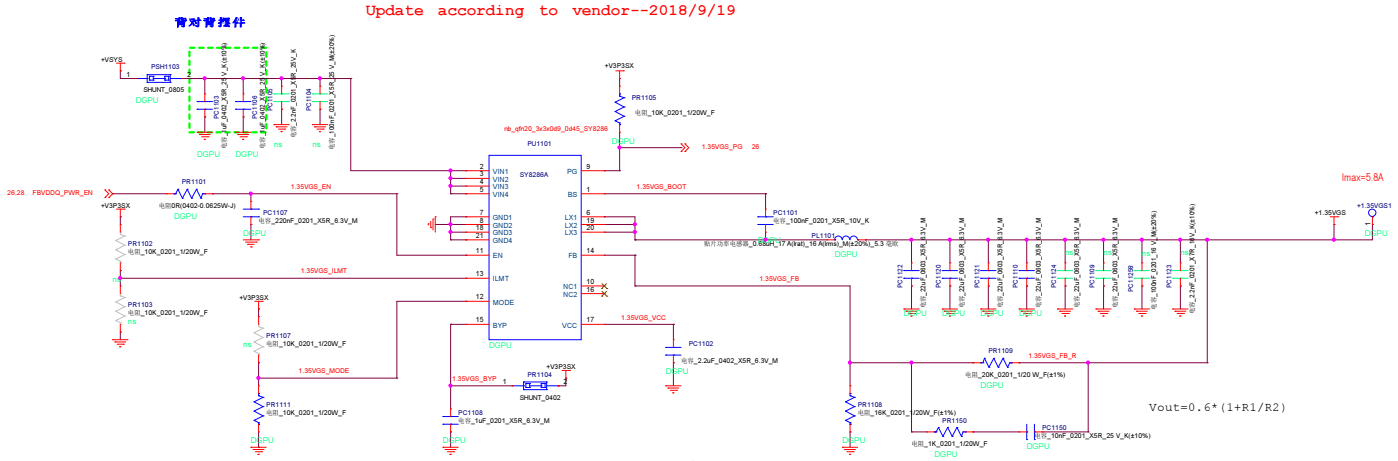
Update according to vendor--2018/9/19



stuff reduce S0 power consumption 11/5

ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

PR1150:0Ω -10kΩ
PC1150:100pF-1nF 11/5

Huaqin Telecom Technology Com.,Ltd.			
Page name:	POWER DELIVERY_1.35VGS		
Size: A4	Project Name: NB8513		REV: V1.0
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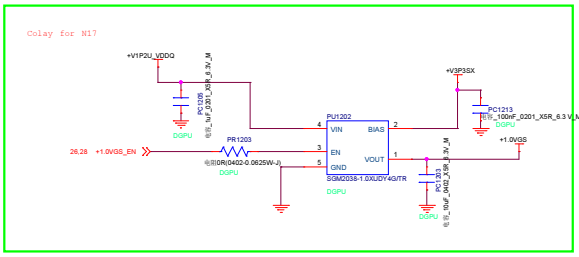

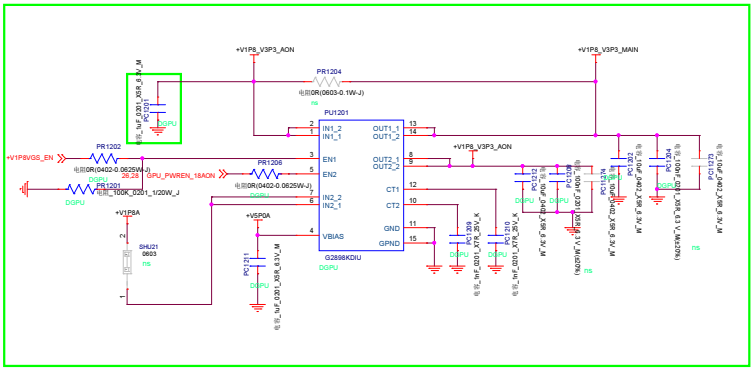

Page name:	POWER DELIVERY_1.0VGS&1.8VGS		
Size: A4	Project Name: NB8513		REV: V1.0
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Huaqin Telecom Technology Com.,Ltd.

HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	BLANK	
Size: A4	Project Name: NB8513	REV: V1.0
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