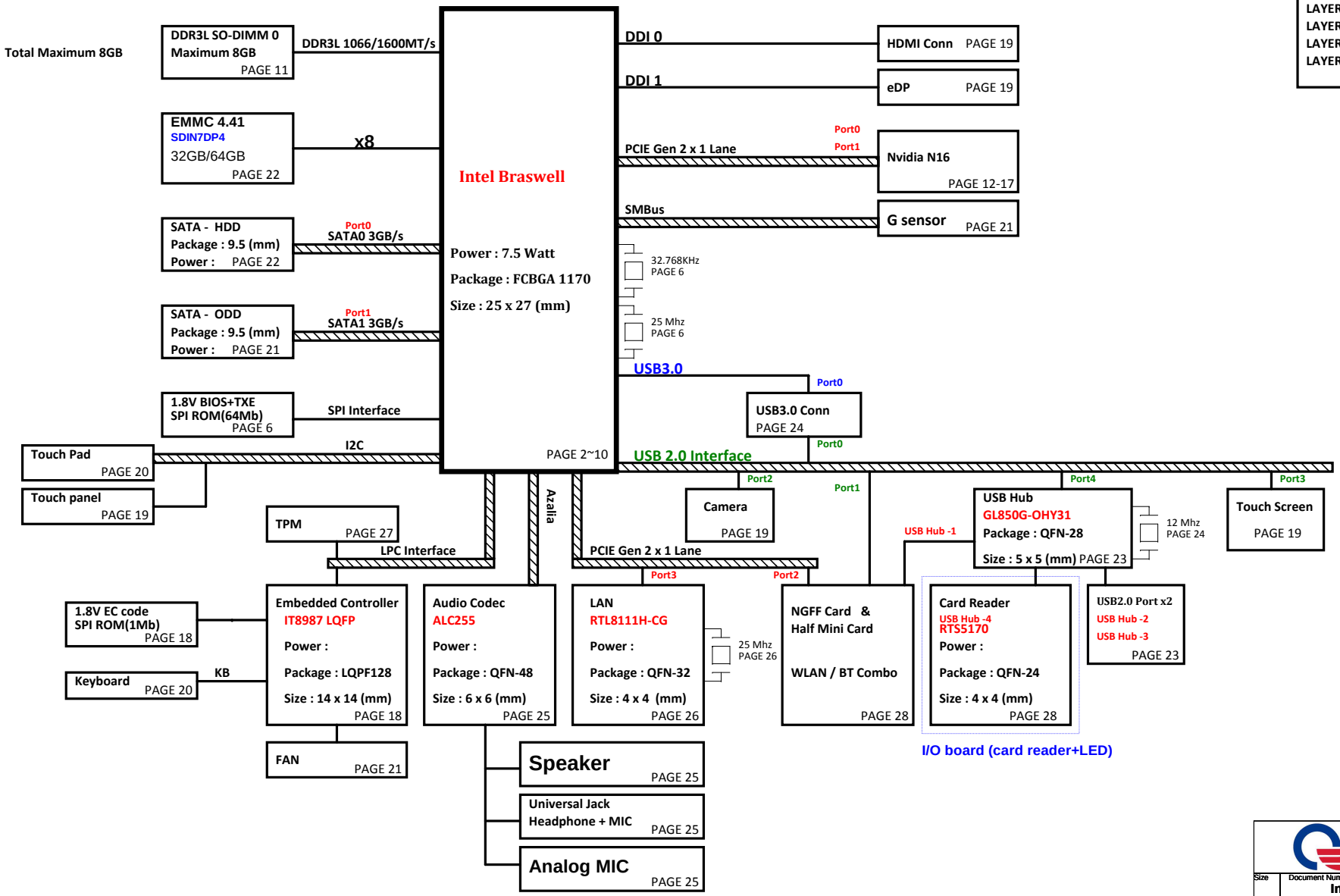
ZYLB/ZYLC (17")
Intel Braswell Platform Block Diagram

01

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND
LAYER 6 : BOT



BOM option	Note
EV@	Discrete
TPS@	Touch Screen
KBL@	KB light
GS@	G-Sensor
EVG@	CG6 2.0 (N16S)
EVNG@	Non-CG6 2.0
AC@	IOAC
NAC@	Non-IOAC
EM@	EMMC

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Friday, April 10, 2015 Sheet 1 of 42

+1.35VSUS 3,9,11,34
+3V_S5 3,5,9,17,18,20,23,26,27,29,33,38

11 M_A_A[15:0]

U27A

M_A_A0 BB47 DDR3_M0_MA_0
M_A_A1 BC42 DDR3_M0_MA_1
M_A_A2 BJ48 DDR3_M0_MA_2
M_A_A3 BH47 DDR3_M0_MA_3
M_A_A4 BD42 DDR3_M0_MA_4
M_A_A5 BH48 DDR3_M0_MA_5
M_A_A6 BB46 DDR3_M0_MA_6
M_A_A7 BE46 DDR3_M0_MA_7
M_A_A8 BD44 DDR3_M0_MA_8
M_A_A9 BE52 DDR3_M0_MA_9
M_A_A10 BJ45 DDR3_M0_MA_10
M_A_A11 BB49 DDR3_M0_MA_11
M_A_A12 BF48 DDR3_M0_MA_12
M_A_A13 BF44 DDR3_M0_MA_13
M_A_A14 BD47 DDR3_M0_MA_14
M_A_A15 BD49 DDR3_M0_MA_15

11 M_A_DM0 M_A_DM0 AP52 DDR3_M0_DM_0
11 M_A_DM1 M_A_DM1 AT48 DDR3_M0_DM_1
11 M_A_DM2 M_A_DM2 AP44 DDR3_M0_DM_2
11 M_A_DM3 M_A_DM3 BA53 DDR3_M0_DM_3
11 M_A_DM4 M_A_DM4 BG41 DDR3_M0_DM_4
11 M_A_DM5 M_A_DM5 AY36 DDR3_M0_DM_5
11 M_A_DM6 M_A_DM6 BD32 DDR3_M0_DM_6
11 M_A_DM7 M_A_DM7 BH30 DDR3_M0_DM_7

11 M_A_RAS# M_A_RAS# BA40 DDR3_M0_RASB
11 M_A_CAS# M_A_CAS# BG45 DDR3_M0_CASB
11 M_A_WE# M_A_WE# BH44 DDR3_M0_WEB

11 M_A_BS#0 M_A_BS#0 BH46 DDR3_M0_BS_0
11 M_A_BS#1 M_A_BS#1 AY40 DDR3_M0_BS_1
11 M_A_BS#2 M_A_BS#2 BF52 DDR3_M0_BS_2

11 M_A_CS#0 M_A_CS#0 AY38 DDR3_M0_CSB_0
11 M_A_CS#1 M_A_CS#1 AU38 DDR3_M0_CSB_1

11 M_A_CKE0 M_A_CKE0 BB44 DDR3_M0_CKE_0
11 M_A_CKE1 M_A_CKE1 AY42 DDR3_M0_CKE_1

11 M_A_ODT0 M_A_ODT0 AV36 DDR3_M0_ODT_0
11 M_A_ODT1 M_A_ODT1 BA38 DDR3_M0_ODT_1

11 M_A_CLK0 M_A_CLK0 BD40 DDR3_M0_CK_0
11 M_A_CLK0# M_A_CLK0# BF40 DDR3_M0_CKB_0

11 M_A_CLK1 M_A_CLK1 BD38 DDR3_M0_CK_1
11 M_A_CLK1# M_A_CLK1# BF38 DDR3_M0_CKB_1

11 M_A_DRAMRST# M_A_DRAMRST# BA42 DDR3_M0_DRAMRSTB

M_A_VREF_CA AT28 DRAM_M0_OCAVREF
M_A_VREF_DQ AU28 DRAM_M0_ODQVREF

AT30 RSVD_AT30
AU30 RSVD_AU30

SOC_DRAM_PWROK AV28 DDR3_DRAM_PWROK

GND R262 182/F_4 DRAM_RCOMP0 BA28 DDR3_M0_RCOMPPD

1 OF 12

VLV_M_D/BGA
REV = 1.15

M_A_DQ[63:0] 11

DDR3_M0_DQ_0 AK51 M_A_DQ0
DDR3_M0_DQ_1 AL51 M_A_DQ1
DDR3_M0_DQ_2 AT52 M_A_DQ2
DDR3_M0_DQ_3 AR51 M_A_DQ3
DDR3_M0_DQ_4 AL53 M_A_DQ4
DDR3_M0_DQ_5 AK52 M_A_DQ5
DDR3_M0_DQ_6 AR53 M_A_DQ6
DDR3_M0_DQ_7 AP51 M_A_DQ7
DDR3_M0_DQ_8 AP48 M_A_DQ8
DDR3_M0_DQ_9 AT47 M_A_DQ9
DDR3_M0_DQ_10 AY48 M_A_DQ10
DDR3_M0_DQ_11 AV50 M_A_DQ11
DDR3_M0_DQ_12 AP47 M_A_DQ12
DDR3_M0_DQ_13 AT50 M_A_DQ13
DDR3_M0_DQ_14 AY50 M_A_DQ14
DDR3_M0_DQ_15 AV45 M_A_DQ15
DDR3_M0_DQ_16 AT40 M_A_DQ16
DDR3_M0_DQ_17 AP42 M_A_DQ17
DDR3_M0_DQ_18 AT38 M_A_DQ18
DDR3_M0_DQ_19 AP40 M_A_DQ19
DDR3_M0_DQ_20 AT44 M_A_DQ20
DDR3_M0_DQ_21 AV41 M_A_DQ21
DDR3_M0_DQ_22 AP41 M_A_DQ22
DDR3_M0_DQ_23 AV42 M_A_DQ23
DDR3_M0_DQ_24 BD52 M_A_DQ24
DDR3_M0_DQ_25 AV52 M_A_DQ25
DDR3_M0_DQ_26 BC53 M_A_DQ26
DDR3_M0_DQ_27 AV51 M_A_DQ27
DDR3_M0_DQ_28 AW51 M_A_DQ28
DDR3_M0_DQ_29 BC52 M_A_DQ29
DDR3_M0_DQ_30 AW53 M_A_DQ30
DDR3_M0_DQ_31 BB51 M_A_DQ31
DDR3_M0_DQ_32 BG42 M_A_DQ32
DDR3_M0_DQ_33 BG43 M_A_DQ33
DDR3_M0_DQ_34 BG37 M_A_DQ34
DDR3_M0_DQ_35 BJ37 M_A_DQ35
DDR3_M0_DQ_36 BH42 M_A_DQ36
DDR3_M0_DQ_37 BJ41 M_A_DQ37
DDR3_M0_DQ_38 BH36 M_A_DQ38
DDR3_M0_DQ_39 BH38 M_A_DQ39
DDR3_M0_DQ_40 BC36 M_A_DQ40
DDR3_M0_DQ_41 BA36 M_A_DQ41
DDR3_M0_DQ_42 AU34 M_A_DQ42
DDR3_M0_DQ_43 AU32 M_A_DQ43
DDR3_M0_DQ_44 BF36 M_A_DQ44
DDR3_M0_DQ_45 BD36 M_A_DQ45
DDR3_M0_DQ_46 AV34 M_A_DQ46
DDR3_M0_DQ_47 AV32 M_A_DQ47
DDR3_M0_DQ_48 BF34 M_A_DQ48
DDR3_M0_DQ_49 BC34 M_A_DQ49
DDR3_M0_DQ_50 BA32 M_A_DQ50
DDR3_M0_DQ_51 BD30 M_A_DQ51
DDR3_M0_DQ_52 BD34 M_A_DQ52
DDR3_M0_DQ_53 BA34 M_A_DQ53
DDR3_M0_DQ_54 BF30 M_A_DQ54
DDR3_M0_DQ_55 BD28 M_A_DQ55
DDR3_M0_DQ_56 BJ33 M_A_DQ56
DDR3_M0_DQ_57 BG29 M_A_DQ57
DDR3_M0_DQ_58 BH34 M_A_DQ58
DDR3_M0_DQ_59 BG32 M_A_DQ59
DDR3_M0_DQ_60 BG28 M_A_DQ60
DDR3_M0_DQ_61 BJ29 M_A_DQ61
DDR3_M0_DQ_62 BH28 M_A_DQ62
DDR3_M0_DQ_63 BG33 M_A_DQ63

DDR3_M0_DQSP_0 AM52 M_A_DQS0 M_A_DQS0 11
DDR3_M0_DQSN_0 AM51 M_A_DQS#0 M_A_DQS#0 11
DDR3_M0_DQSP_1 AV47 M_A_DQS1 M_A_DQS1 11
DDR3_M0_DQSN_1 AV48 M_A_DQS#1 M_A_DQS#1 11
DDR3_M0_DQSP_2 AT42 M_A_DQS2 M_A_DQS2 11
DDR3_M0_DQSN_2 AT41 M_A_DQS#2 M_A_DQS#2 11
DDR3_M0_DQSP_3 AY52 M_A_DQS3 M_A_DQS3 11
DDR3_M0_DQSN_3 BA51 M_A_DQS#3 M_A_DQS#3 11
DDR3_M0_DQSP_4 BH40 M_A_DQS4 M_A_DQS4 11
DDR3_M0_DQSN_4 BG39 M_A_DQS#4 M_A_DQS#4 11
DDR3_M0_DQSP_5 AT32 M_A_DQS5 M_A_DQS5 11
DDR3_M0_DQSN_5 AT34 M_A_DQS#5 M_A_DQS#5 11
DDR3_M0_DQSP_6 BC30 M_A_DQS6 M_A_DQS6 11
DDR3_M0_DQSN_6 BC32 M_A_DQS#6 M_A_DQS#6 11
DDR3_M0_DQSP_7 BH32 M_A_DQS7 M_A_DQS7 11
DDR3_M0_DQSN_7 BG31 M_A_DQS#7 M_A_DQS#7 11

ROUTE ALL VREF POWER SIGNALS AS THICK TRACES
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

VREF signals are not used for DDR3L designs.

+1.35VSUS
R559 *4.7K/F_4
M_A_VREF_CA
R564 *4.7K/F_4
C417 *0.1U/16V_4
GND GND

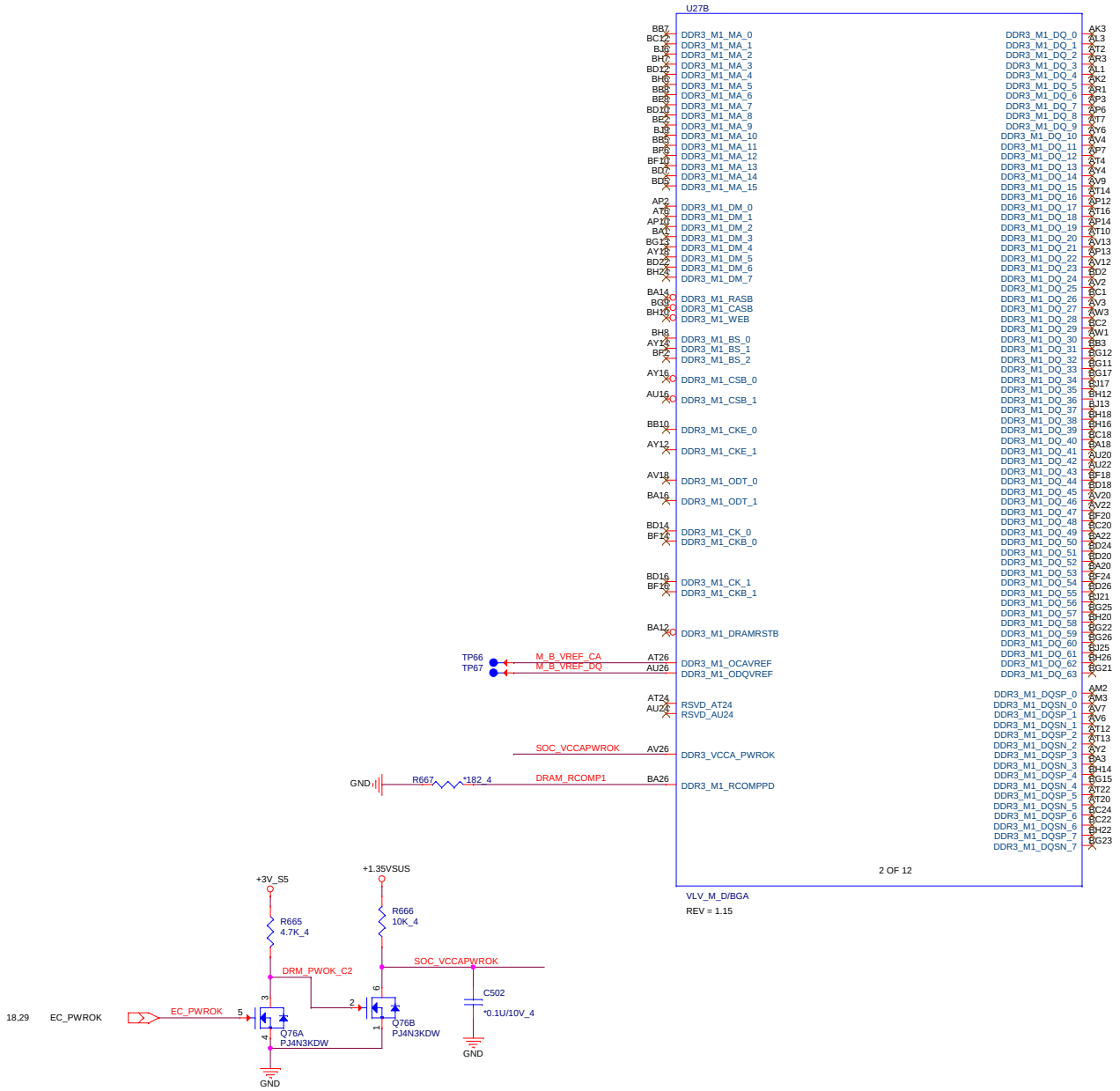
+1.35VSUS
PLACE 0.1UF CAP CLOSE TO CPU
R560 *4.7K/F_4
M_A_VREF_DQ
R565 *4.7K/F_4
C418 *0.1U/16V_4
GND GND

Channel 0	Channel 1	SoC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

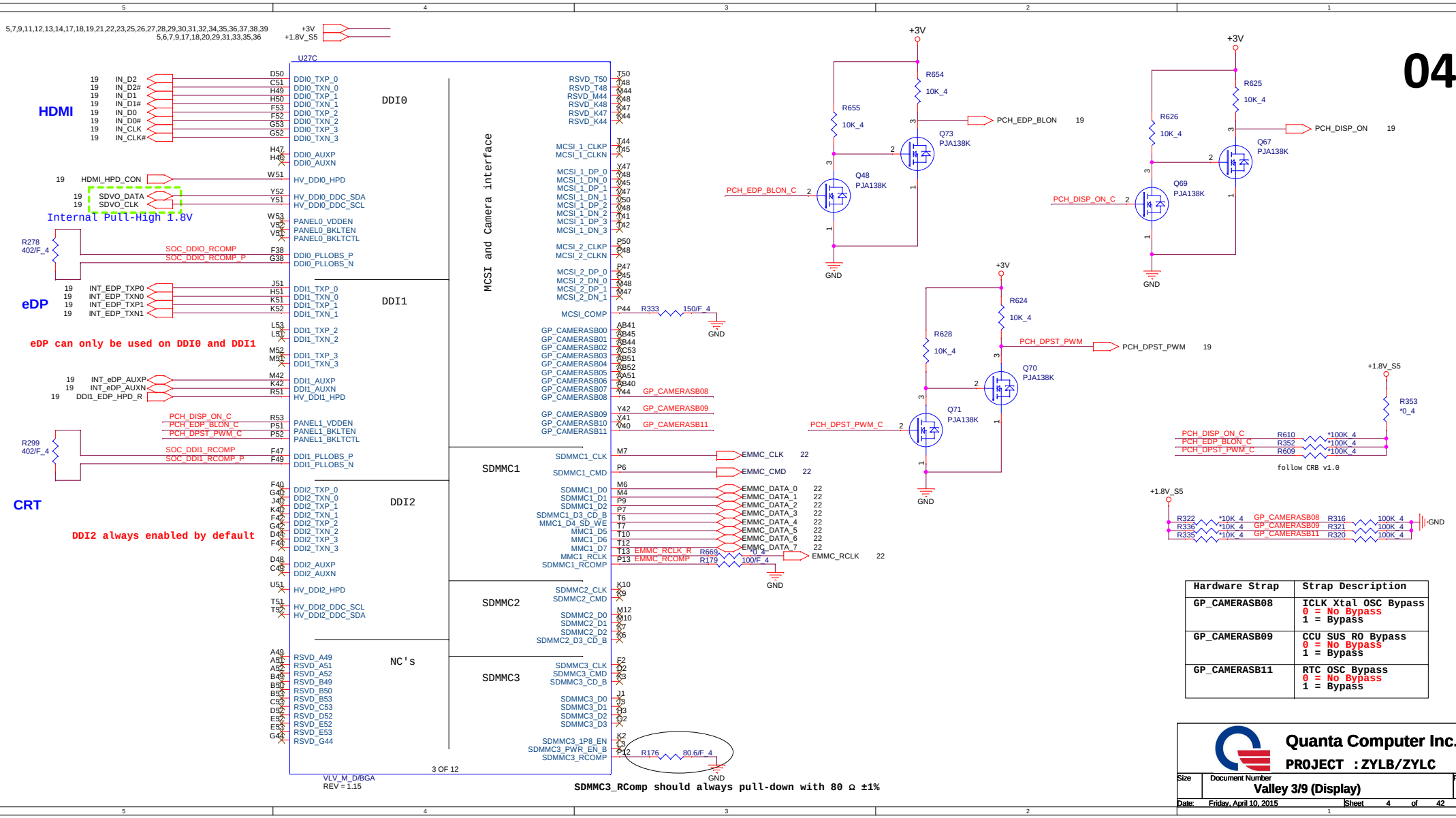
Channel 0 need to
be populated first for the platform to power on

+3V_S5
R152 4.7K_4
DRM_PWOK_C1
+1.35VSUS
R145 10K_4
HWPG_1.35V *0/short_4 R144 SOC_DRAM_PWROK
C139 *0.1U/16V_4
GND
6,29 SLP_S4# SLP_S4# 5
Q27A PJ4N3KDW
Q27B PJ4N3KDW
GND
HWPG_1.35V 34

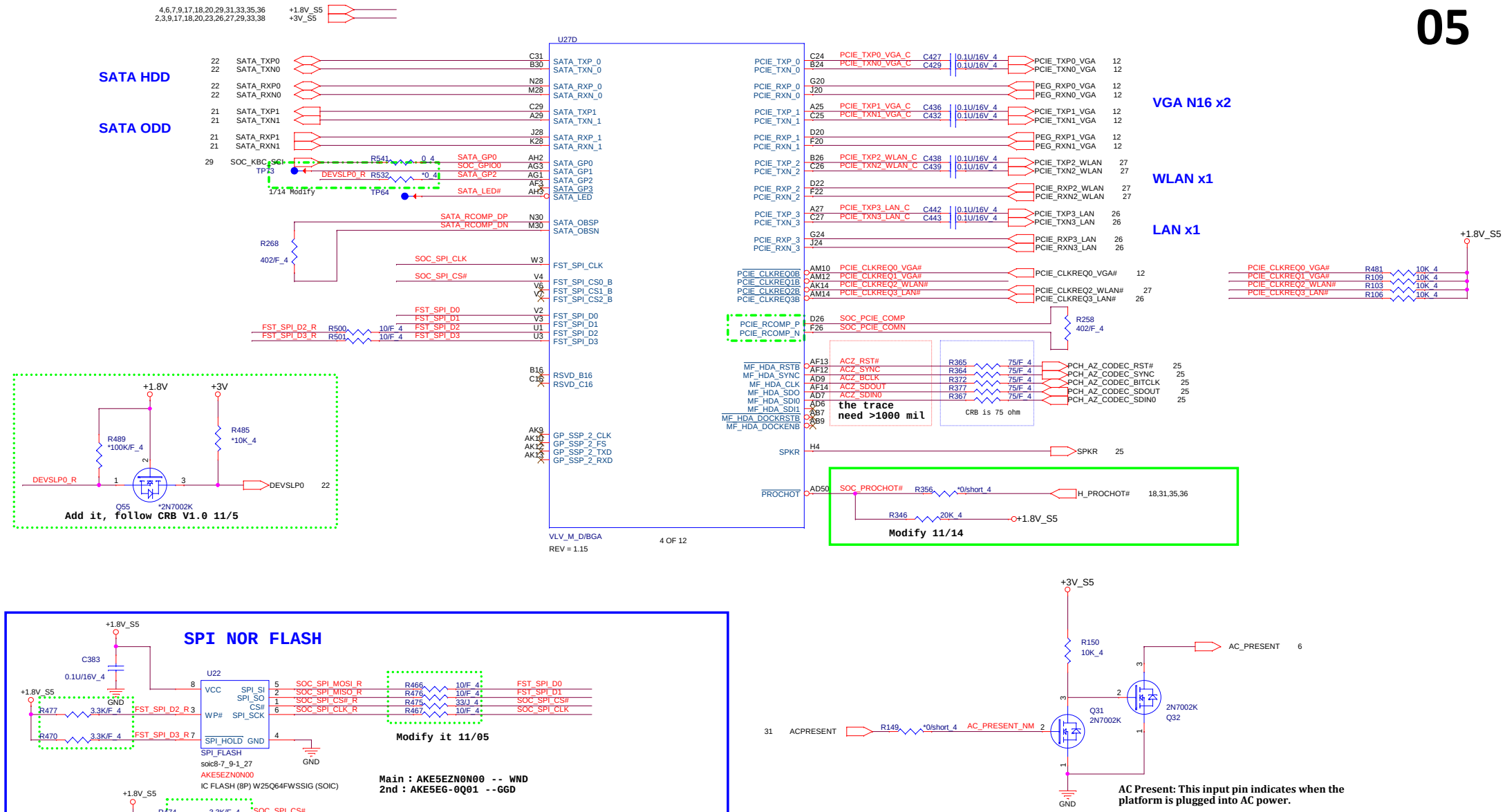
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
Size
Document Number
Valley 1/9 (DDRA)
Rev 1A
Date: Friday, April 10, 2015 Sheet 2 of 42



Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
Date: Friday, April 10, 2015	Sheet 3 of 42	



Hardware Strap	Strap Description
GP_CAMERASB08	ICLK Xtal OSC Bypass 0 = No Bypass 1 = Bypass
GP_CAMERASB09	CCU SUS RO Bypass 0 = No Bypass 1 = Bypass
GP_CAMERASB11	RTC OSC Bypass 0 = No Bypass 1 = Bypass



Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A

Date: Friday, April 10, 2015 Sheet 5 of 42

2/5 Change from 18P to 15P

C416 15P/50V_4 — XTAL25_OUT — GND

Y5 19.2MHZ +-20PPM — PR217 200K/F_4

XTAL25_IN — C419 15P/50V_4 — GND

2nd source:BG619200014 (TXC)

4,5,7,9,17,18,20,29,31,33,35,36 +1.8V_S5
9,18 +3V_RTC
8,33,35,36 +1.05V_S5

U27E

XTAL25_IN P24 — XTAL25_OUT M22 — ICLK_OSCIN / ICLK_OSCOUT

R249 2.49K/F_4 — R255 49.9/F_4 — GND — ICLK_ICOMP / ICLK_RCOMP

J26 RSVD_J26
N26 RSVD_N26
P20 ICLK_ICOMP
N20 ICLK_RCOMP
P26 RSVD_P26
K26 RSVD_K26
M26 RSVD_M26
AH45 RSVD_AH45

VGA N16

12 CLK_PCIE_VGAN — C21 A21 — PCIE_CLK_DIFF_N_0 / PCIE_CLK_DIFF_P_0
12 CLK_PCIE_VGAP — B20 C19 — PCIE_CLK_DIFF_N_1 / PCIE_CLK_DIFF_P_1

WLAN

27 CLK_PCIE_WLANN — B18 C18 — PCIE_CLK_DIFF_N_2 / PCIE_CLK_DIFF_P_2
27 CLK_PCIE_WLANP

LAN

26 CLK_PCIE_LANN — A17 C17 — PCIE_CLK_DIFF_N_3 / PCIE_CLK_DIFF_P_3
26 CLK_PCIE_LANP

All straps are sampled on the rising edge of PMU_RSMRST_N

Hardware Strap	Strap Description
GPIO_SUS[0]	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap(A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	BIOS Boot Selection 0 = - - 1 = SPI
GPIO_SUS[5]	Security Flash Descriptors 0 = Overrride 1 = Normal Operation
GPIO_SUS[8]	ICLK,USB 2.0,DDI SFR supply select 0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK,USB 2.0,DDI SFR Bypass 0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[3]	MIPI-DSI Display Detect 0 = DSI Port not detected 1= DSI Port detected
GPIO_SUS[6]	Halt Boot Strap 1= Normal Operation
GPIO_SUS[10]	POSM Select 0 = Fuse Controller 1 = PMC

BOARD_ID0 A9 — BOARD_ID1 C9 — BOARD_ID2 B8 — BOARD_ID3 B7 — BOARD_ID4 B5 — BOARD_ID5 B4 — MF_PLT_CLK0 / MF_PLT_CLK1 / MF_PLT_CLK2 / MF_PLT_CLK3 / MF_PLT_CLK4 / MF_PLT_CLK5

Y13 SPI1_CS0_B — Y12 SPI1_CS1_B — V13 SPI1_MISO — V12 SPI1_MOSI — V14 SPI1_CLK

AM40 GPIO_DFX0 — AM41 GPIO_DFX1 — AM43 GPIO_DFX2 — AM45 GPIO_DFX3 — AM47 GPIO_DFX4 — AK45 GPIO_DFX5 — AM49 GPIO_DFX6 — AK41 GPIO_DFX7 — AK42 GPIO_DFX8

GPIO_SUS0 AD51 — GPIO_SUS1 AD52 — GPIO_SUS2 AH50 — GPIO_SUS3 AH48 — GPIO_SUS4 AH51 — GPIO_SUS5 AH52 — GPIO_SUS6 AG51 — GPIO_SUS7 AG53 — GPIO_SUS8 AF52 — GPIO_SUS9 AF51 — GPIO_SUS10 AE51 — SEC_GPIO_SUS9 / SEC_GPIO_SUS8 / SEC_GPIO_SUS10 / SEC_GPIO_SUS11 — AC51

R644 100/F_4 — SOC_GPIO_RCOMP — AH40 GPIO0_RCOMP — Y3 GPIO0_ALERT — GND

5 OF 12

VLV_M_D/BGA
REV = 1.15

UART1_RXD AD12 — UART1_TXD AD10 — DGPU_EVENT#_Q AD14 — UART1_RTS_B AD13 — UART1_CTS_B
TP29 / TP28 / DGPU_EVENT#_Q 17
1/22 Delete TP33

VGPU_EN_Q T7 — DGPU_HOLD_RST#_Q Y6 — DGPU_PWR_EN_Q V10 — DGPU_PWROK_Q V9 — UART2_RXD / UART2_TXD / UART2_RTS_B / UART2_CTS_B
VGPU_EN_Q 17
DGPU_HOLD_RST#_Q 17
DGPU_PWR_EN_Q 17
DGPU_PWROK_Q 17

SUSPWRDNACK AE3 — PMU_SUSCLK C15 — PMU_SLP_S0IX_B A13 — PMU_SLP_S4_B C12 — PMU_SLP_S3_B B14
SUS_PWRDOWNACK — 1/14 Modify R503 *0_4 — TP75 — PCH_SUSPWRDANCK 18,33
SLP_S0IX# 33 / SLP_S4# 2,29 / SLP_S3# 29,33

PMU_AC_PRESENT C13 — PMU_WAKE_B N16 — PMU_BATLOW_B C14 — PMU_PWRBTN_B M16 — PMU_RESETBUTTON_B AF2 — PMU_PLTRST_B F14 — SUS_STAT_B D14 — PMU_SLP_LAN_B B12 — PMU_WAKE_LAN_B B18
AC_PRESENT — SOC_PMC_WAKE — PMU_BATLOW# — SOC_PWRBTN# — SOC_REST_BTN# — SOC_PLTRST# — PCH_SUS_STAT#
AC_PRESENT 5
SOC_PMC_WAKE 29
SOC_PWRBTN# 29
SOC_PLTRST# 22,29
PCH_SUS_STAT# 29

RTEST_B J16 — SRTCRST_B D18
SOC_RTEST# / SRT_CRST#

RSMRST_B F18 — COREPWROK G16
SOC_RSMRST# 29
CORE_PWROK 29

BRTCX1_PAD M18 — BRTCX2_PAD K18 — BVCCRTC_EXTPAD F16 — RSVD_VSS G18
RTC_X1 / RTC_X2 / BRTC_EXTPAD
C406 0.1U/16V_4 — R246 10K/F_4 — GND

SVID0_ALERT_B AD40 — SVID0_DATA AD41 — SVID0_CLK AD42
VR_SVID_ALERT# / VR_SVID_DATA / VR_SVID_CLK
VR_SVID_ALERT# 35,36
VR_SVID_DATA 35,36
VR_SVID_CLK 35,36

RSVD_C11 C11 — RSVD_B10 B10 — RSVD_F12 C12 — RSVD_F10 F10 — RSVD_D12 D12

RSVD_E8 E8 — RSVD_C7 C7 — RSVD_D6 D6
TP_INT# — Gsensor_INT
TP_INT# 20
Gsensor_INT 29

RSVD_J12 J12 — RSVD_F7 F7 — RSVD_J14 J14 — RSVD_L13 L13
TP_INT_C / TP_RST#_Q / PCH_ODD_EN
TP_INT_C 29
TP_RST#_Q 29
PCH_ODD_EN 21

Touch pad

Touch panel

+1.8V_S5
TP_INT# 10K_4 R199
TP_INT_C 10K_4 R169
TP_RST#_Q 10K_4 R530
Gsensor_INT 10K_4 R529

Default NC No Pull High / Low
R139 *EV@10K_4 — VGPU_EN_Q — R138 *EV@10K_4 — GND
Default Pull High 10K(+1.8V_S5)
R136 EV@10K_4 — DGPU_HOLD_RST#_Q — R137 *EV@10K_4 — GND
Default NC No Pull High / Low
R128 *EV@10K_4 — DGPU_PWR_EN_Q — R162 *EV@10K_4 — GND
Default Pull Low 10K(GND)
R134 *EV@10K_4 — DGPU_PWROK_Q — R164 EV@100K/F_4 — GND
Default NC No Pull High / Low
R107 *EV@10K_4 — DGPU_EVENT#_Q — R108 *EV@10K_4 — GND

+1.8V_S5
PCH_SUS_STAT# R196 *10K_4
PMU_BATLOW# R562 10K_4
SUS_PWRDOWNACK R498 *10K_4
SOC_PMC_WAKE R129 10K_4
AC_PRESENT R561 10K_4
SLP_S4# R198 *10K_4
SLP_S3# R566 *10K_4
SLP_S0IX# R563 *10K_4
1/27 Modify
SOC_REST_BTN# R521 2.7K/J_4
SOC_PLTRST# R197 1K/J_4
AC_PRESENT R175 *10K_4 — GND

Change from +1.0V to +1.05V
+1.05V_S5
C462 *0.1u/16V_4 — GND
C464 *10p/50V_4 — VR_SVID_DATA — R604 *301/F_4
C465 *10p/50V_4 — VR_SVID_ALERT# — R605 200/F_4
C466 *10p/50V_4 — VR_SVID_CLK — R606 *301/F_4
GND
Add 10P to GND for layout length too long 11/26

RTC Clock 32.768KHz
RTC_X1 — R558 10M_4 — Y4 32.768KHZ — RTC_X2
15P/50V_4 C413 — 15P/50V_4 C408 — GND
2013/07/25
change package , P/N change
from BG332768224 to
BG332768453

+1.8V_S5
R631 4.7K_4 GPIO_SUS0 R614 *10K_4
R632 4.7K_4 GPIO_SUS1 R615 *10K_4
R340 10K_4 GPIO_SUS2 R348 *10K_4
R621 100K_4 GPIO_SUS4 R638 *10K_4
R637 100K_4 GPIO_SUS5
R634 *10K_4 GPIO_SUS8 R617 4.7K_4
R635 *1K/J_4 GPIO_SUS9 R618 *10K_4
R341 *10K_4 GPIO_SUS3 R349 *10K_4
R636 4.7K_4 GPIO_SUS6
R619 *10K_4 GPIO_SUS7
R633 *10K_4 GPIO_SUS10 R616 *10K_4 — GND

Modify it 11/14

29 TPS_SEL — *0_4 R202 — BOARD_ID1

1/27 Modify
11/28 Add it
R620 4.7K_4 — GPIO_SUS5
18 EC_Override — R652 *0/short_4 — SOC_Override_NM — 2N7002K Q72 — GND

BOARD ID

+1.8V_S5
R695 *GS@10K_4 BOARD_ID0 R696 10K_4
R556 *10K_4 BOARD_ID1 R557 10K_4
R551 *10K_4 BOARD_ID2 R552 *EV@10K_4
R550 *TPM@10K_4 BOARD_ID3 R549 10K_4
R542 10K_4 BOARD_ID4 R543 *10K_4
R536 *10K_4 BOARD_ID5 R534 10K_4

BOARD_ID0 :"H" W/ G-Sensor; "Low " W/O G-Sensor
BOARD_ID1 :"H" W/ touch panel; "Low " W/O touch panel
BOARD_ID2 : "H" is UMA ; "Low " is Dis
BOARD_ID3 : TPM HIGH=TPM, LOW=W/O TPM
BOARD_ID4 :"H" is for ZYLB,MB ID
BOARD_ID5 : Reserve for UMA and GPU

RTC Circuitry(RTC)

+3V_RTC_0 — 20mils — +3VPCU — R180 1K/J_4 — VCCRTC_1 — D7 BAT54CW — 20MIL
CN6 BAT_CONN — GND

+3V_RTC
R174 20K/J_4 — C161 1u/6.3V_4 — G1 — SOC_RTEST# — *SHORT_PAD1
30mils
R170 20K/J_4 — C155 1u/6.3V_4 — C164 1u/6.3V_4 — G2 — SRT_CRST# — *SHORT_PAD1
20MIL
Change G1、G2 footprint from "SOLDERJUMPER-2" to "RC0603-C" for SMT request

20MIL

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A

Date: Friday, April 10, 2015 Sheet 6 of 42

+1.8V_S5 4,5,6,9,17,18,20,29,31,33,35,36
+3V_S5 2,3,5,9,17,18,20,23,26,27,29,33,38

All USB 3.0 ports support xHCI debug port functionality.

U27F

24 USB30_TX0+ → B32 USB3_TXP0
24 USB30_TX0- → C32 USB3_TXN0
24 USB30_RX0+ → F28 USB3_RXP0
24 USB30_RX0- → D28 USB3_RXN0

A33 USB3_TXP1
C33 USB3_TXN1
F30 USB3_RXP1
D30 USB3_RXN1

C34 USB3_TXP2
B34 USB3_TXN2
G32 USB3_RXP2
J32 USB3_RXN2

C35 USB3_TX3
A35 USB3_TXN3
G34 USB3_RXP3
J34 USB3_RXN3

R277 402/F_4 — USB3_OBSP / USB3_OBSN
D34 USB3_OBSP
F34 USB3_OBSN

C37 RSVD_C37
A37 RSVD_A37
F36 RSVD_F36
D36 RSVD_D36
M34 RSVD_M34
M32 RSVD_M32

C38 RSVD_C38
B38 RSVD_B38
G36 RSVD_G36
J36 RSVD_J36

N34 RSVD_N34
P34 RSVD_P34

18 CLK_24M_KBC — R516 22_4 — SOC_CLKOUT_0 — P2 MF_LPC_CLKOUT0
27 CLK_TPM — R515 *TPM@22_4 — SOC_CLKOUT_1 — R3 MF_LPC_CLKOUT1
27 CLK_24M_DEBUG — R517 22_4
18,27 CLKRUN# — R533 22_4 — SOC_CLKRUN# — T3 LPC_CLKRUNB

18,27 LFRAME# — LFRAME# — P3 LPC_FRAMEB
18,27 LAD0 — LAD0 — M3 MF_LPC_AD0
18,27 LAD1 — LAD1 — M2 MF_LPC_AD1
18,27 LAD2 — LAD2 — N3 MF_LPC_AD2
18,27 LAD3 — LAD3 — N1 MF_LPC_AD3

27,29 SOC_SERIRQ — SOC_SERIRQ — T2 ILB_SERIRQ

GND — R172 100/F_4 — LPC_RCOMP — T4 LPC_HVT_RCOMP

+1.8V_S5
R339 51/F_4 XDP_H_TDO
R347 51/F_4 XDP_H_TMS
R323 51/F_4 XDP_H_TDI
R342 51/F_4 XDP_H_PREQ#
R334 51/F_4 XDP_H_TRST#
R622 51/F_4 XDP_H_TCK
GND

XDP_H_TCK AF42 TCK
XDP_H_TDI AD47 TDI
XDP_H_TDO AF40 TDO
XDP_H_TMS AD48 TMS
XDP_H_TRST# AB48 TRST_B
TP43 XDP_H_PRDY# AD45 CX_PRDY_B
XDP_H_PREQ# AF41 CX_PREQ_B
EDM_SOC M13 RSVD_M13

+1.8V_S5
R96 1K/J_4 SMB_SOC_DATA AM7 MF_SMB_DATA
R105 1K/J_4 SMB_SOC_CLK AM6 MF_SMB_CLK
R115 1K/J_4 SMB_SOC_ALERTB AM9 MF_SMB_ALERTB

6 OF 12

VLV_M_D/BGA
REV = 1.15

USB_OTG_ID B48

USB_DP0 C42 USBP0+ 24
USB_DN0 B42 USBP0- 24
USB_DP1 C43 USB_BT_P 27
USB_DN1 B44 USB_BT_N 27
USB_DP2 C41 USBP2+ 19
USB_DN2 A41 USBP2- 19
USB_DP3 C45 USBP3+ 19
USB_DN3 A45 USBP3- 19
USB_DP4 B40 USB_H4_P 23
USB_DN4 C40 USB_H4_N 23

USB_OC_00 P14 — 10K_4 R167 — SOC_USB_OC0 24
USB_OC_11 P16 — 10K_4 R568 — +1.8V_S5
RSVD_B46 B46 — USB2_OBSP R256 *49.9/F_4 — SOC_USB_OC1 23
USB_VBUSSNS B47 — USB_VBUSSNS — R596 0_4 — GND
USB_RCOMP A48 — USB_RCOMP — R600 113/F_4 — GND

USB_HSIC_0_STROBE M36
USB_HSIC_0_DATA N36
USB_HSIC_1_STROBE K38
USB_HSIC_1_DATA M38
USB_HSIC_RCOMP N38 — USB_HSIC_RCOMP — 45.3/F_4 R297 — GND

RSVD_H5 H5
RSVD_H7 H7

RSVD_P28 P28
RSVD_P30 C30
RSVD_AF50 AF50
RSVD_AF48 AF48
RSVD_AF44 AF44
RSVD_AF45 AF45

I2C0_SDA AH7 I2C_0_SDA_R — R524 0_4 — I2C_0_SDA 20
I2C0_SCL AK6 I2C_0_SCL_R — R523 0_4 — I2C_0_SCL 20 — **Touch pad**

I2C1_SDA AH6 I2C_1_SDA — R528 *0_4 — I2C1_SDA_GPIO6 19
I2C1_SCL AF6 I2C_1_SCL — R527 *0_4 — I2C1_SCL_GPIO7 19 — **Touch panel**

I2C2_SDA AF7 I2C_2_SDA
I2C2_SCL AF9 I2C_2_SCL

I2C3_SDA AD2 I2C_3_SDA
I2C3_SCL AE4 I2C_3_SCL

I2C4_SDA AD3 I2C_4_SDA
I2C4_SCL AC1 I2C_4_SCL

I2C5_SDA AC3 I2C_5_SDA
I2C5_SCL AB2 I2C_5_SCL

I2C6_SDA AB3 I2C_6_SDA
I2C6_SCL AA1 I2C_6_SCL

RSVD_Y2 Y2
RSVD_AA3 AA3
I2C_NFC_SOC_SDA — T4
I2C_NFC_SOC_SCL — T5

USB3.0

Bluetooth

CAMERA

TouchPanel

USB 2.0 HUB

+1.8V_S5
R597 *40.2K/F_4
R599 *10K/F_4
GND
Follow Intel suggest 12/05

3/19 Modify it

+1.8V_S5
I2C_0_SDA_R — R513 1K/J_4
I2C_0_SCL_R — R512 1K/J_4
I2C_1_SDA — R540 *1K/J_4
I2C_1_SCL — R539 *1K/J_4
I2C_2_SDA — R147 *1K/J_4
I2C_2_SCL — R146 *1K/J_4
I2C_3_SDA — R495 *1K/J_4
I2C_3_SCL — R526 *1K/J_4
I2C_4_SDA — R525 *1K/J_4
I2C_4_SCL — R518 *1K/J_4
I2C_5_SDA — R514 *1K/J_4
I2C_5_SCL — R504 *1K/J_4
I2C_6_SDA — R499 *1K/J_4
I2C_6_SCL — R494 *1K/J_4
I2C_NFC_SOC_SDA — R488 *1K/J_4
I2C_NFC_SOC_SCL — R492 *1K/J_4

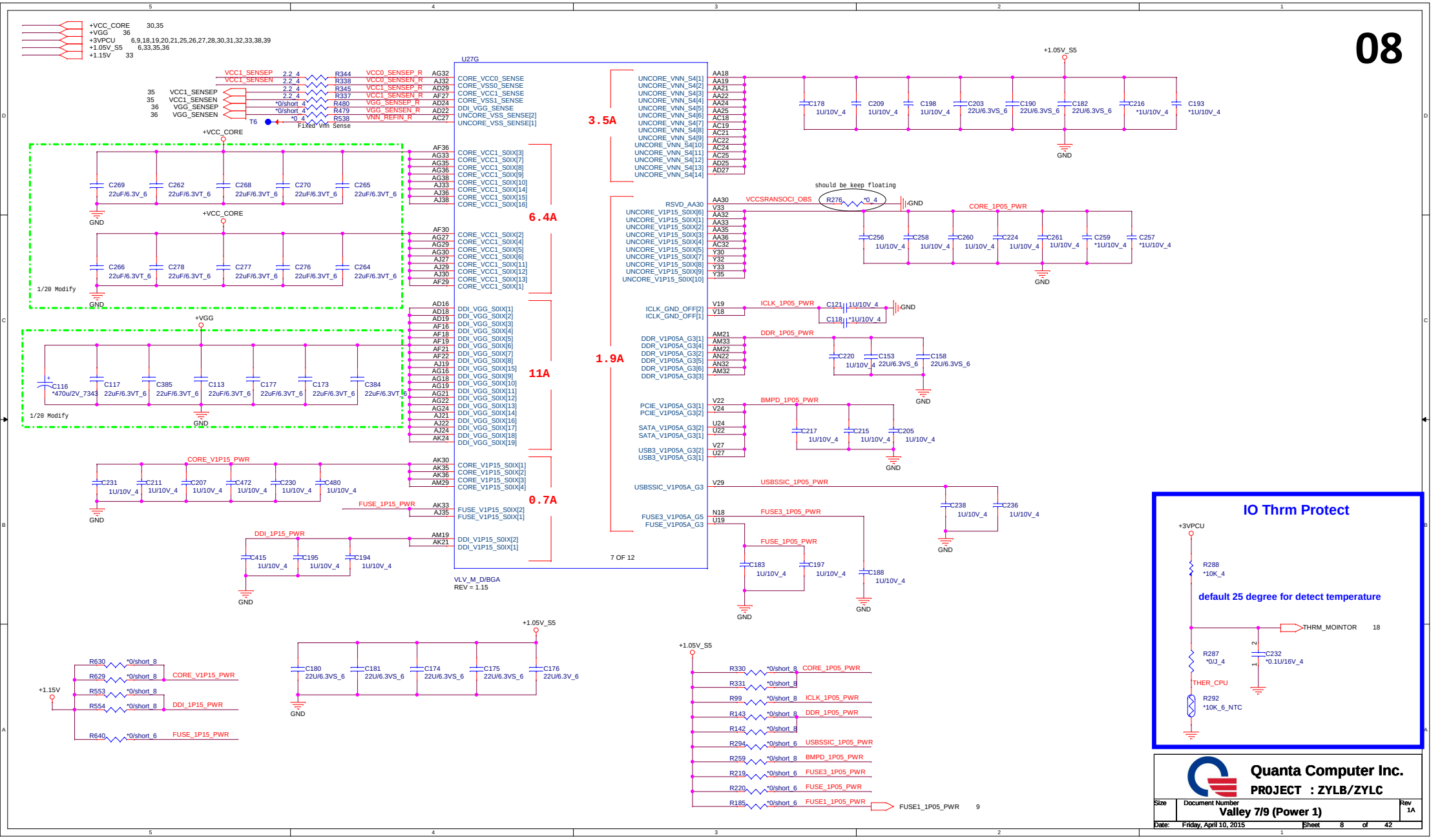
change to 1K as CRB

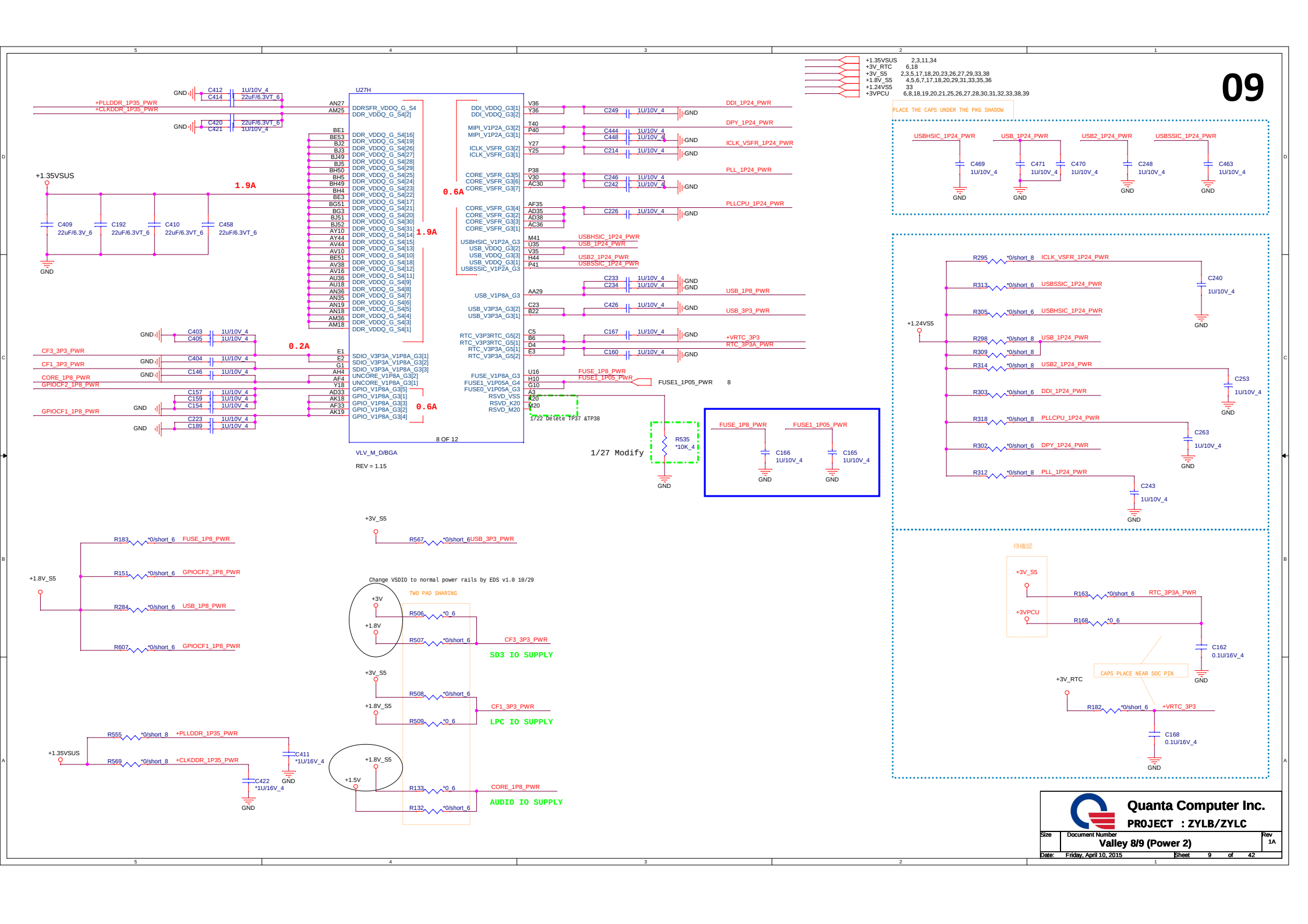
1/27 Modify

+3V
+1.8V_S5
R686 200K_4
3/4 Modify to 4.7K
R687 4.7K_4
R688 4.7K_4
U30 PCA9306
GND — C505 0.1U/25V_4 — C504 0.1U/25V_4 — GND
SMB_SOC_DATA — SDA1 / SDA2 — SMB_RUN_DAT
SMB_SOC_CLK — SCL1 / SCL2 — SMB_RUN_CLK
SMB_RUN_DAT 11,21,27
SMB_RUN_CLK 11,21,27

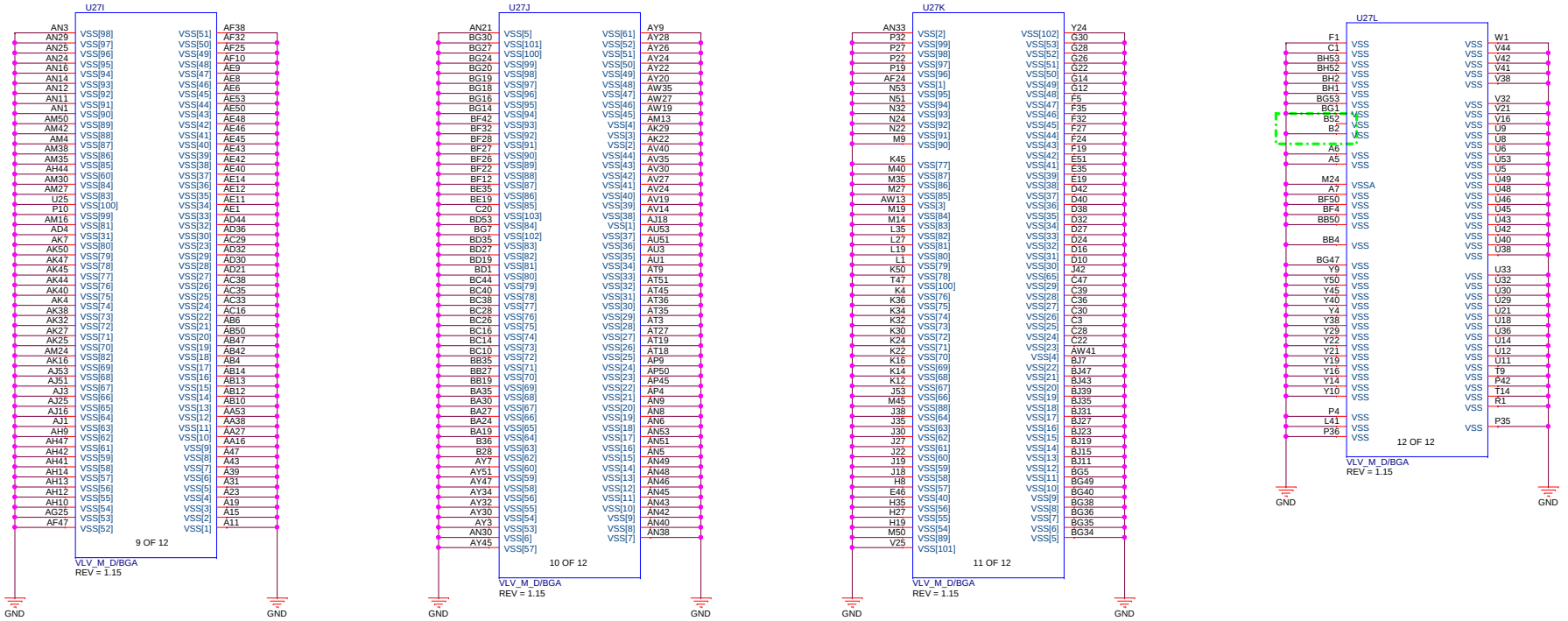
*10K_4 R537 EDM_SOC
GND
Add it 10/29 for CRB v1.0

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
Size | Document Number: Valley 6/9 (USB/LPC/I2C) | Rev 1A
Date: Friday, April 10, 2015 | Sheet 7 of 42

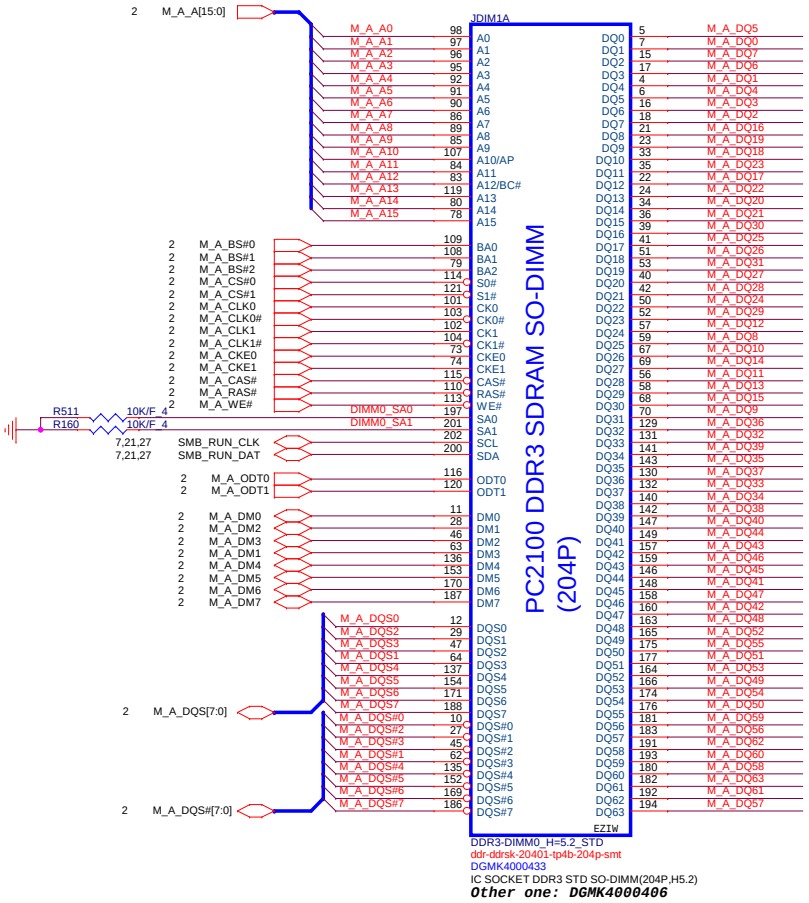

08
+VCC_CORE 30,35
+VGG 36
+3VPCU 6,9,18,19,20,21,25,26,27,28,30,31,32,33,38,39
+1.05V_S5 6,33,35,36
+1.15V 33
U27G
CORE_VCC0_SENSE
CORE_VSS0_SENSE
CORE_VCC1_SENSE
CORE_VSS1_SENSE
DDI_VGG_SENSE
UNCORE_VSS_SENSE[2]
UNCORE_VSS_SENSE[1]
3.5A
6.4A
11A
1.9A
0.7A
7 OF 12
VLV_M_D/BGA
REV = 1.15
VCC1_SENSEP
VCC1_SENSEN
VGG_SENSEP
VGG_SENSEN
Fixed Vnn Sense
+VCC_CORE
+VGG
1/20 Modify
CORE_V1P15_PWR
FUSE_1P15_PWR
DDI_1P15_PWR
+1.15V
+1.05V_S5
should be keep floating
VCCSRANSOCI_OBS
CORE_1P05_PWR
ICLK_1P05_PWR
DDR_1P05_PWR
BMPD_1P05_PWR
USBSSIC_1P05_PWR
FUSE3_1P05_PWR
FUSE_1P05_PWR
GND
IO Thrm Protect
default 25 degree for detect temperature
THRM_MOINTOR 18
THER_CPU
R288 *10K_4
R287 *0/J_4
C232 *0.1U/16V_4
R292 *10K_6_NTC
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
Size
Document Number
Valley 7/9 (Power 1)
Rev 1A
Date: Friday, April 10, 2015
Sheet 8 of 42

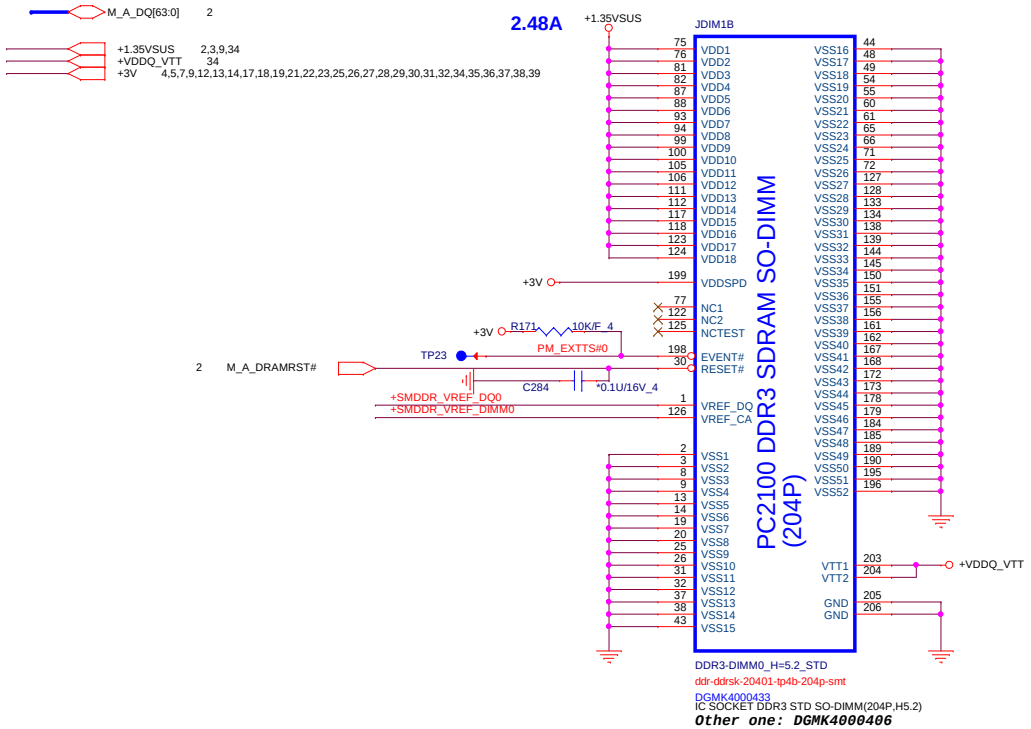

09
U27H
8 OF 12
VLV_M_D/BGA
REV = 1.15
+1.35VSUS
1.9A
0.6A
0.2A
1/27 Modify
Change VSDIO to normal power rails by EDS v1.0 10/29
TWO PAD SHARING
SD3 IO SUPPLY
LPC IO SUPPLY
AUDIO IO SUPPLY
PLACE THE CAPS UNDER THE PKG SHADOW
CAPS PLACE NEAR SOC PIN
待確認
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
Valley 8/9 (Power 2)
Friday, April 10, 2015

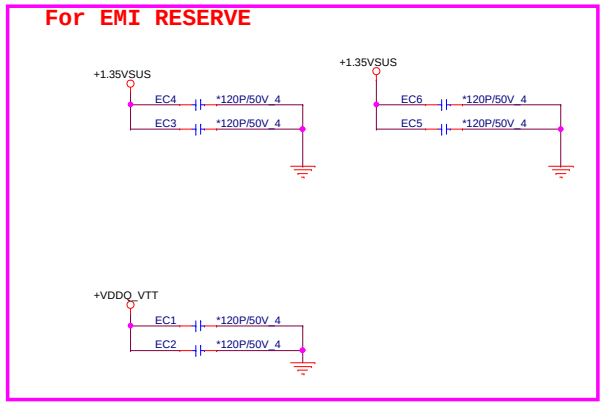
B52 is NC for layout issue

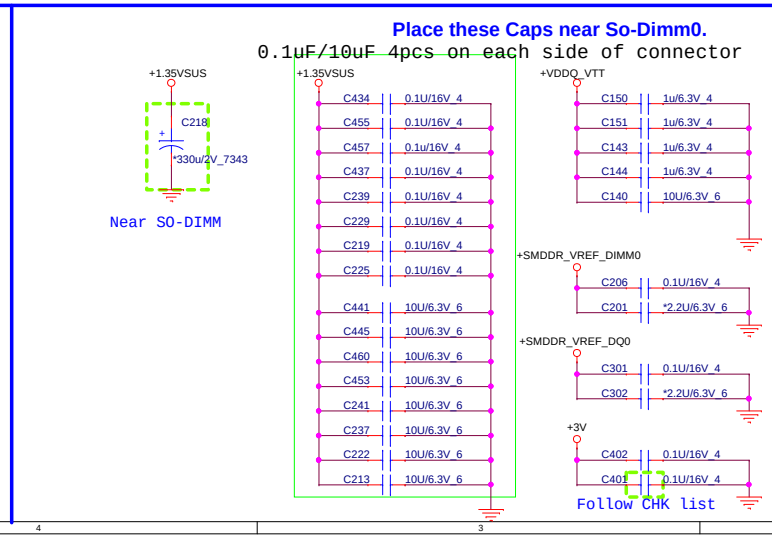


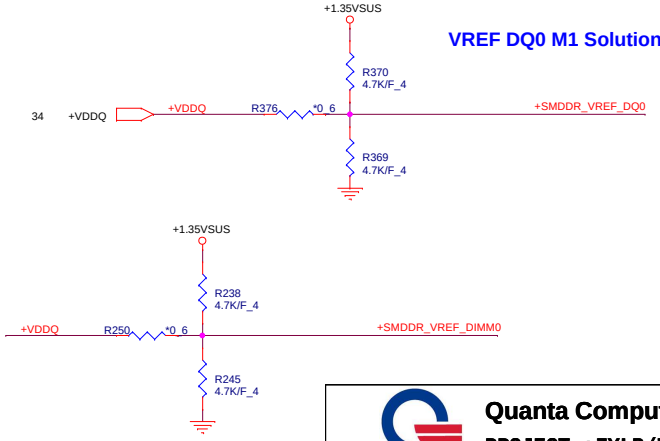
Quanta Computer Inc.	
PROJECT : ZYLB/ZYLC	
Size	Document Number: Valley 9/9 (GND) — Rev: 1A
Date: Friday, April 10, 2015	Sheet 10 of 42











Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	DDR3 DIMM0-STD(5.2H)	1A
Date: Friday, April 10, 2015	Sheet 11 of 42	

+1.05V_GFX 13,14,30,39
+3V_GFX 14,15,18,39
+3V 4,5,7,9,11,13,14,17,18,19,21,22,23,25,26,27,28,29,30,31,32,34,35,36,37,38,39
+3V_MAIN 14,15
+VGPU_CORE 38

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

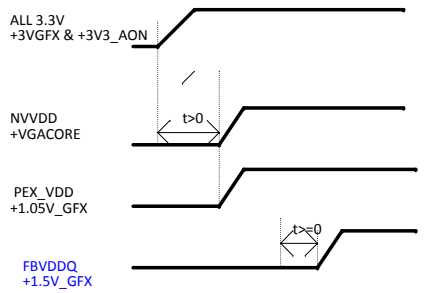
NVDD = 32.22 ~ 26.66 A

VDD33 = 56mA

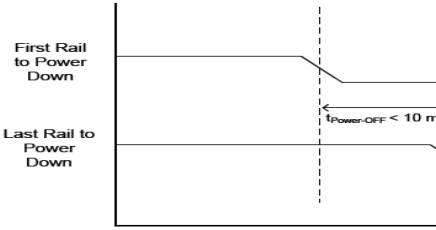
N16V stuff it, not support GC6 2.0

Modify 12/25

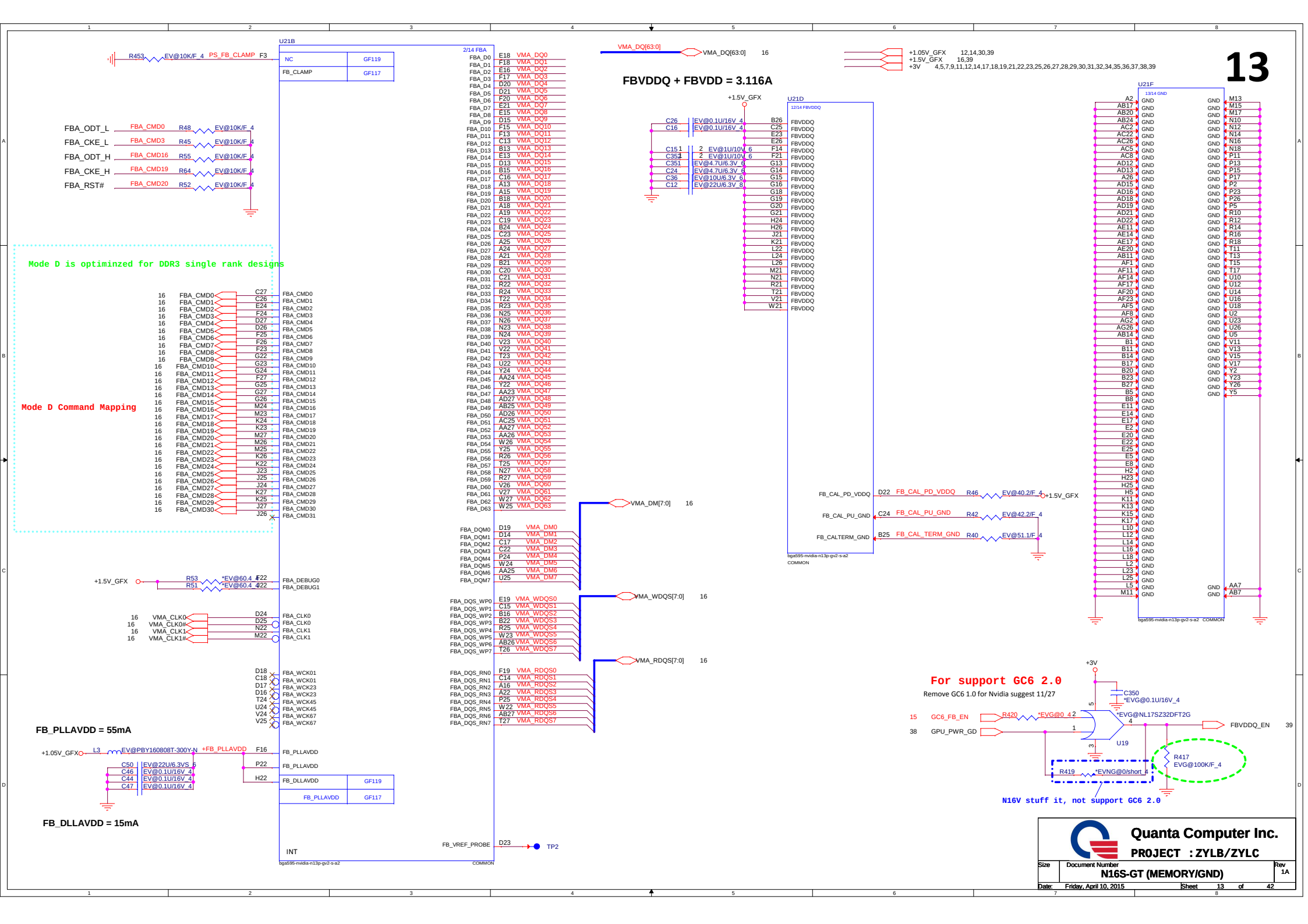
Power up sequence



Power down sequence



Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: N16S-GT (PCIE I/F) /NVDD	Rev: 1A
Date: Friday, April 10, 2015	Sheet 12 of 42	



Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	N16S-GT (MEMORY/GND)	1A

Date: Friday, April 10, 2015 Sheet 13 of 42

U21G
4/14 IFPAB
IFPAB
bga595-nvidia-n13p-gv2-s-a2
COMMON

U21J
7/14 IFPEF
IFPE
IFPF
bga595-nvidia-n13p-gv2-s-a2
COMMON

U21K
3/14 DACA
bga595-nvidia-n13p-gv2-s-a2
COMMON

U21H
5/14 IFPC
IFPC
bga595-nvidia-n13p-gv2-s-a2
COMMON

U21I
6/14 IFPD
IFPD
bga595-nvidia-n13p-gv2-s-a2
COMMON

GC6 Power control

3V MAIN POWER

N16V stuff it, not support GC6 2.0

PLLVDD = 38mA

SP_PLLVDD = 17mA

VID_PLLVDD = 41mA

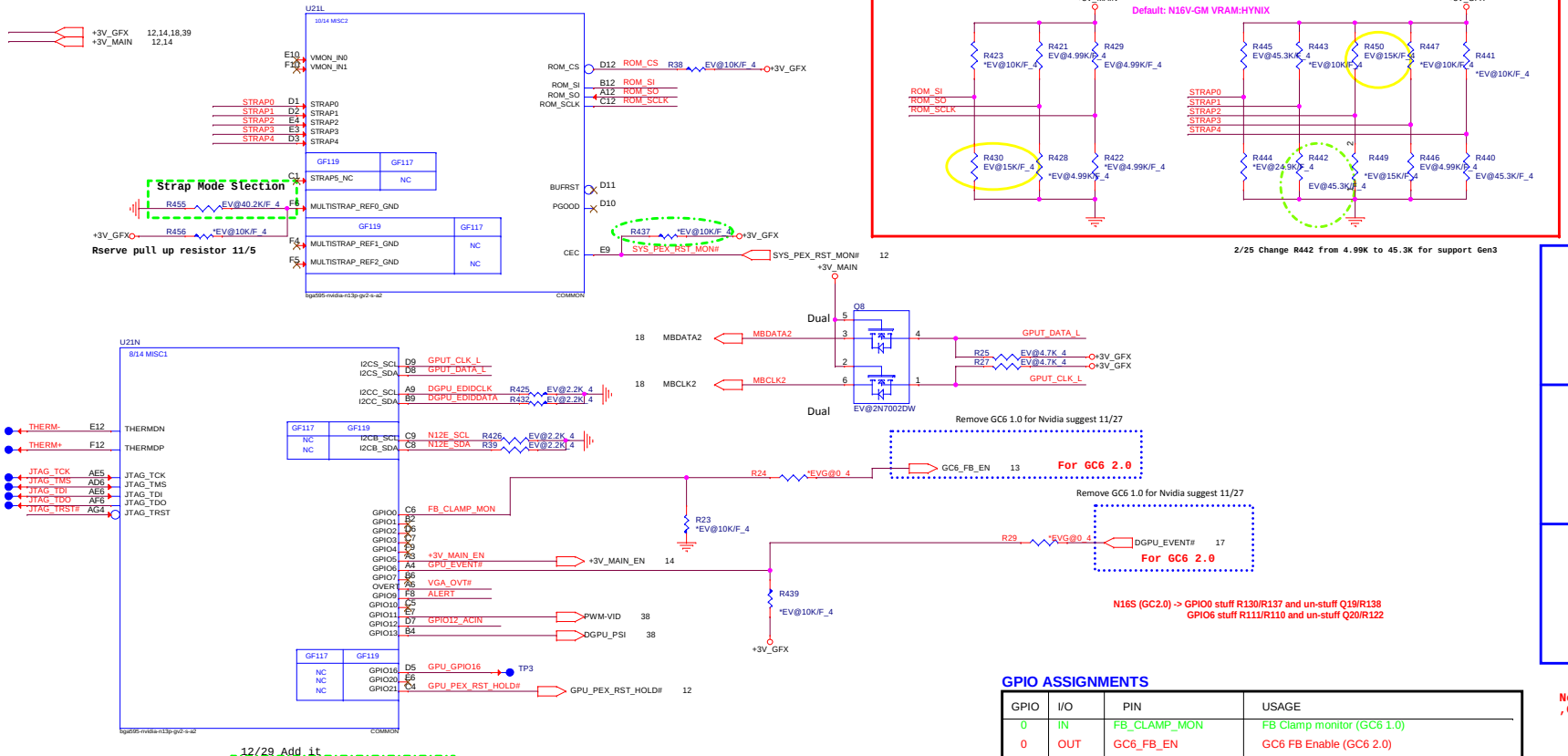
U21M
9/14 XTAL_PLL

+1.05V_GFX and GPU core power EN

+3V 4,5,7,9,11,12,13,17,18,19,21,22,23,25,26,27,28,29,30,31,32,34,35,36,37,38,39
+1.05V_GFX 12,13,30,39
+3V_GFX 12,15,18,39
+3V_MAIN 12,15

2/5 Change from 10pF to 12pF

Quanta Computer Inc.	
PROJECT : ZYLB/ZYLC	
Size	Document Number: N16S-GT (DISPLAY) — Rev: 1A
Date: Friday, April 10, 2015	Sheet 14 of 42



N16S-GT DID=0x1347 GB2B-64

```
ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table
```

N16V-GM DID=0x1299 GB2-64

```
ROM_SCLK = Stuff 4.99K pull up
ROM_SO   = Stuff 4.99K pull up.
STRAP0   = Stuff 45.3k pull up. (EDID Panel)
STRAP1   = Stuff 4.99k pull down.(Gen3 support)
STRAP2   = Stuff 10k pull up.(DID 0x1299)
STRAP3   = Stuff 4.99k pull down.(No display out)
STRAP4   = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI   = VRAM Configuration follow below table
```

N16V-GL DID=0x129A GB2-64

```
ROM_SCLK = Stuff 4.99K pull up
ROM_SO   = Stuff 4.99K pull up.
STRAP0   = Stuff 45.3k pull up. (EDID Panel)
STRAP1   = Stuff 4.99k pull down.(Gen3 support)
STRAP2   = Stuff 15k pull up.(DID 0x129A)
STRAP3   = Stuff 4.99k pull down.(No display out)
STRAP4   = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI   = VRAM Configuration follow below table
```

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.

N16S-GM/-GT/-LP VRAM Configuration Table — ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					
0000	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63AFR-11C	PD 4.9K ohm	AKD5PGWTW13	Single Rank or Single Rank stuffing for Dual Rank
0001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	
0010	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG	K4W4G1646D-BC1A	PD 15K ohm	AKD5PGWT504	Dual Rank

N16V-GM/GL VRAM Configuration Table — ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					
0001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank or Single Rank stuffing for Dual Rank
0010	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63AFR-11C	PD 15K ohm	AKD5PGWTW13	
0100	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG	K4W4G1646D-BC1A	PD 24.9K ohm	AKD5PGWT504	
1001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63CFR-N0C	PU 10K ohm	AKD5PZDTW03	

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev 1A
Date: Friday, April 10, 2015 | Sheet 15 of 42

HYU 256Mx16, H5TC4G63AFR-11C STN B/S PN : AKD5PGWTW13
MIC 256Mx16, MT41J256M16HA-093G:E STN B/S PN : AKD5PZSTL05
SAM 256Mx16, K4W4G1646D-BC1A STN B/S PN : AKD5PGWT504

CHANNEL A: 2048MB DDR3X16

16

13 VMA_DQ[63..0]
13 VMA_DM[7..0]
13 VMA_WDQS[7..0]
13 VMA_RDQS[7..0]

+1.05V_GFX 12,13,14,30,39
+1.5V_GFX 13,39

VRAM1 / VRAM3 / VRAM2 / VRAM4

EV@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1%

R49 / R448 / R62 / R60 EV@243/F_4

VMA_CLK0 — R43 EV@162/F_4 — VMA_CLK0#

162_1% ohm
CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

R451 / R32 EV@1.33K/F_4 — VREFC_VMA1 / VREFD_VMA1 — R452 / R37 EV@1.33K/F_4 — C362 / C22 EV@0.1u/16V_4

13 FBA_CMD17 — FBA_CMD17 — TP8
13 FBA_CMD1 — FBA_CMD1 — TP51
10/14 modify

VMA_CLK1 — R70 EV@162/F_4 — VMA_CLK1#

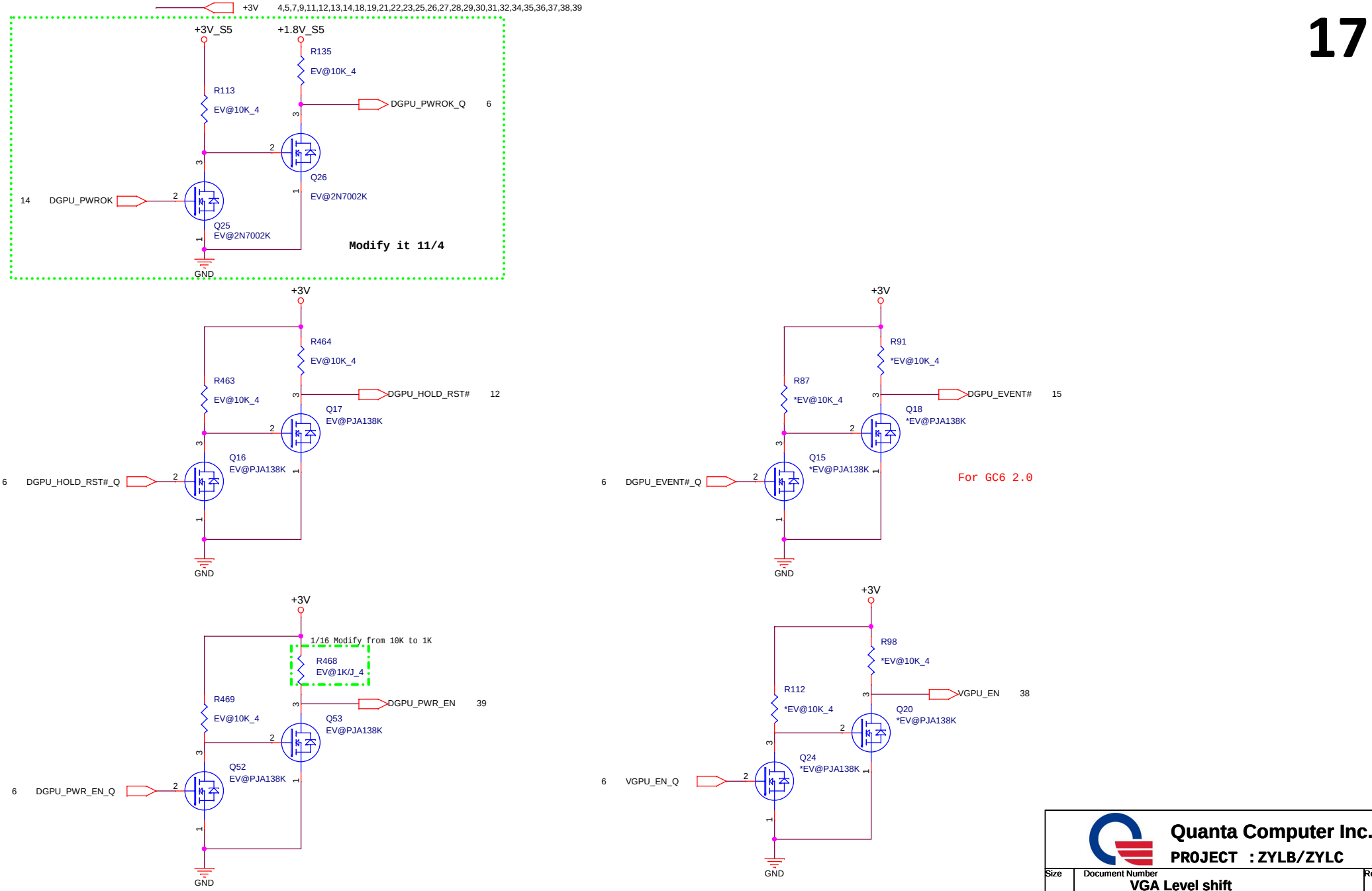
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R59 / R457 EV@1.33K/F_4 — VREFC_VMA3 / VREFD_VMA3 — R58 / R458 EV@1.33K/F_4 — C70 / C370 EV@0.1u/16V_4

+1.5V_GFX
C371 C353 C30 C359 EV@1u/10V_4
C13 C367 C366 C354 C17 C360 EV@10u/6.3V_6 / EV@1u/10V_4
C105 C372 C355 C368 C381 C106 C358 C361 EV@10u/6.3V_6 / EV@1u/10V_4
C379 C31 C97 C99 C20 C87 C93 EV@10u/6.3V_6 / EV@0.1u/16V_4
C34 C103 EV@10u/6.3V_6
C19 C380 C85 EV@0.1u/16V_4

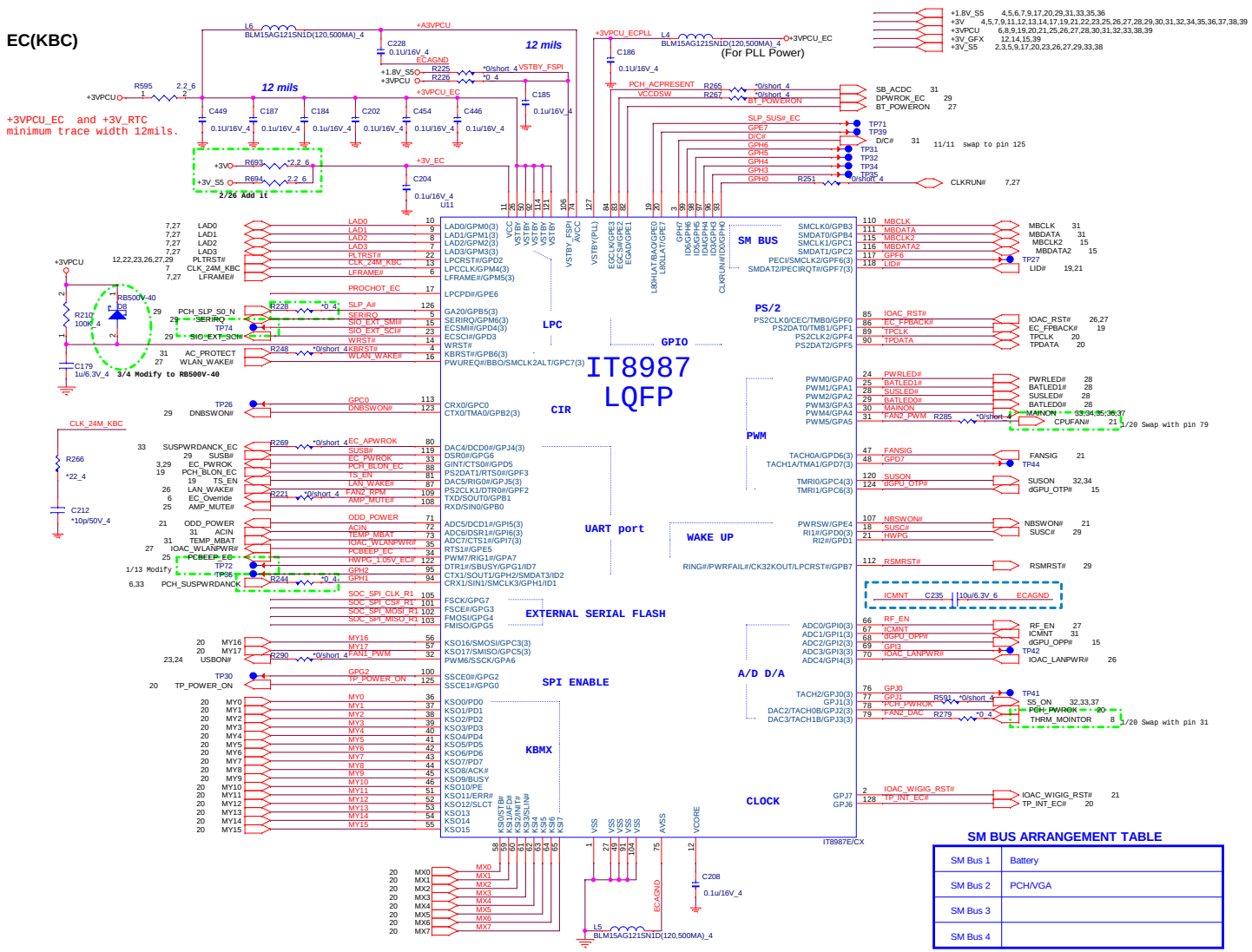
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	N15P- DDR3 VRAM	1A
Date: Friday, April 10, 2015	Sheet 16 of 42	



Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: VGA Level shift	Rev: 1A
Date: Friday, April 10, 2015	Sheet 17 of 42	

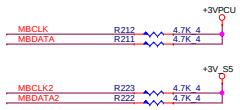
EC(KBC)

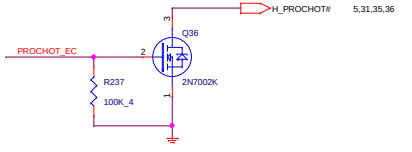


SM BUS ARRANGEMENT TABLE

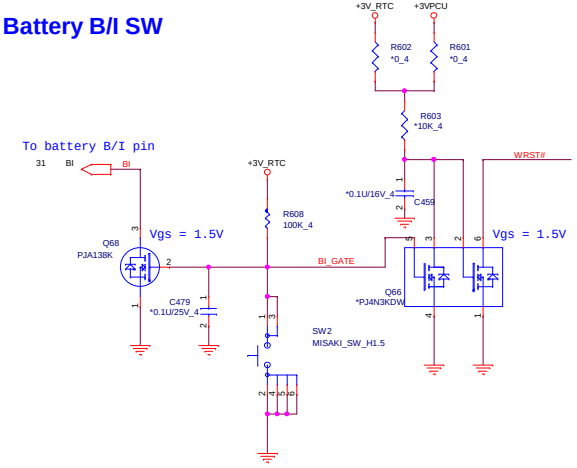
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

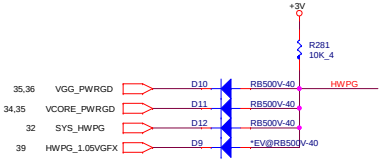




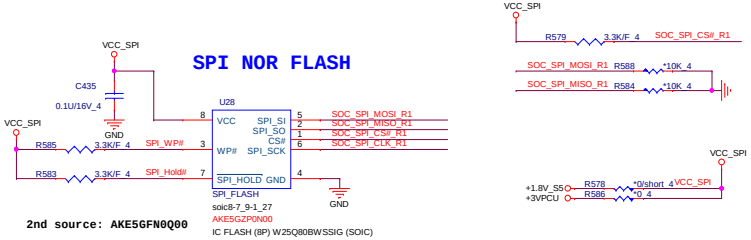
Battery B/I SW

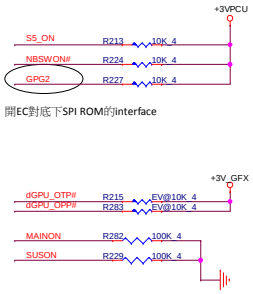


HWPG(KBC)



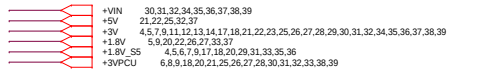
SPI NOR FLASH

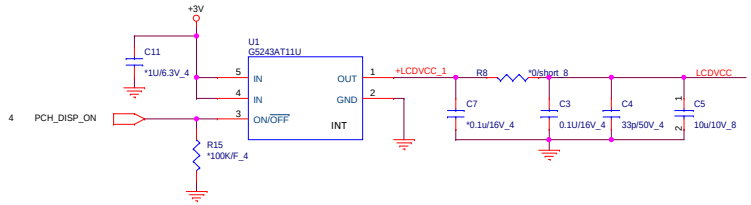


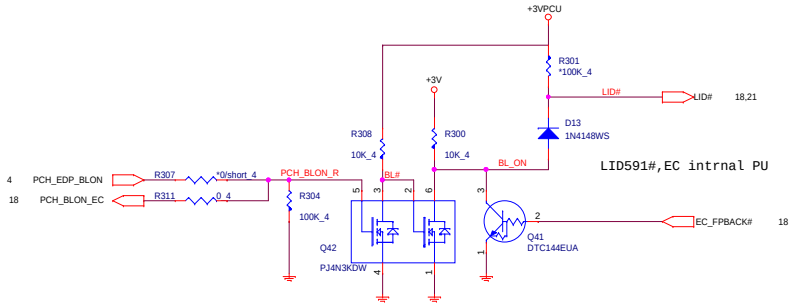


Quanta Computer Inc.	
PROJECT : ZYLB/ZYLC	
Size	Document Number: KBC IT8987 — Rev: 1A
Date: Friday, April 10, 2015	Sheet 18 of 42

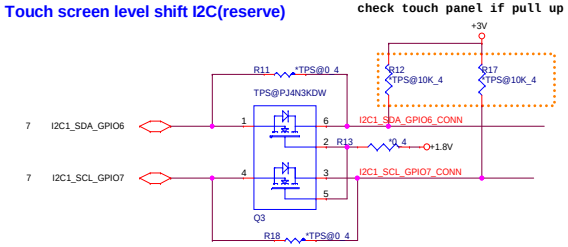
EDP Conn.

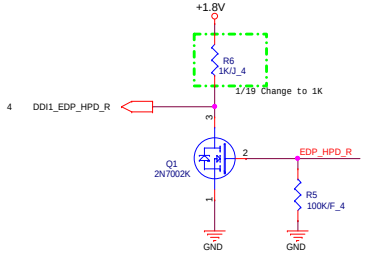


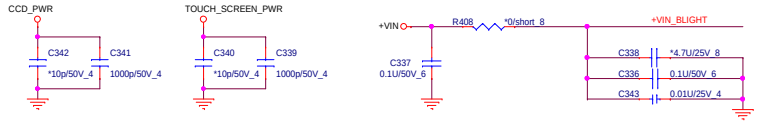




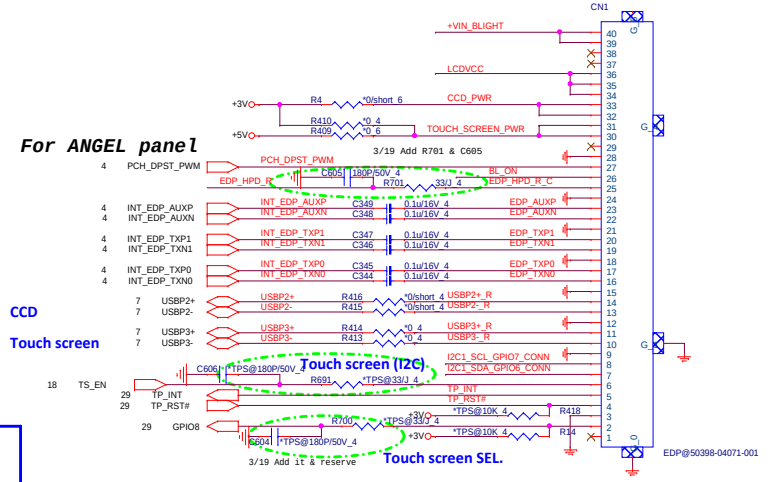
Touch screen level shift I2C(reserve)

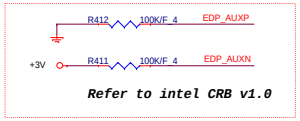






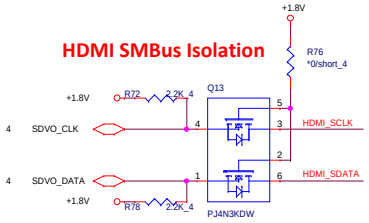
For ANGEL panel



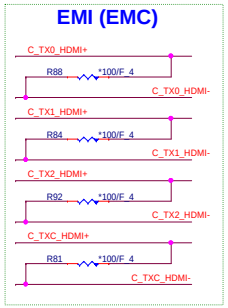


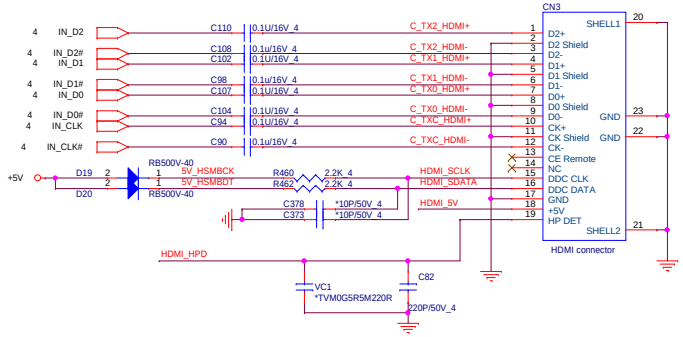
HDMI Conn.

HDMI SMBus Isolation



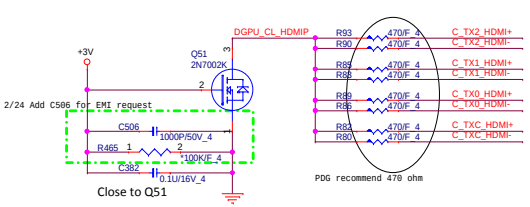
EMI (EMC)



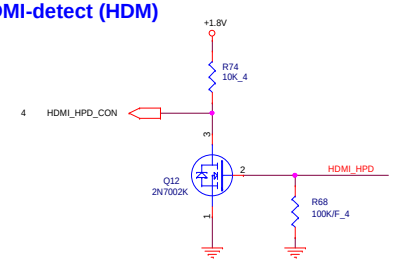


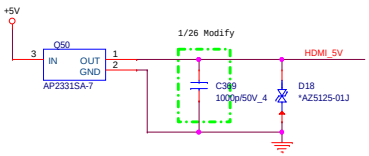
HDMI-Level shift (HDM)

Close to HDMI connector



HDMI-detect (HDM)

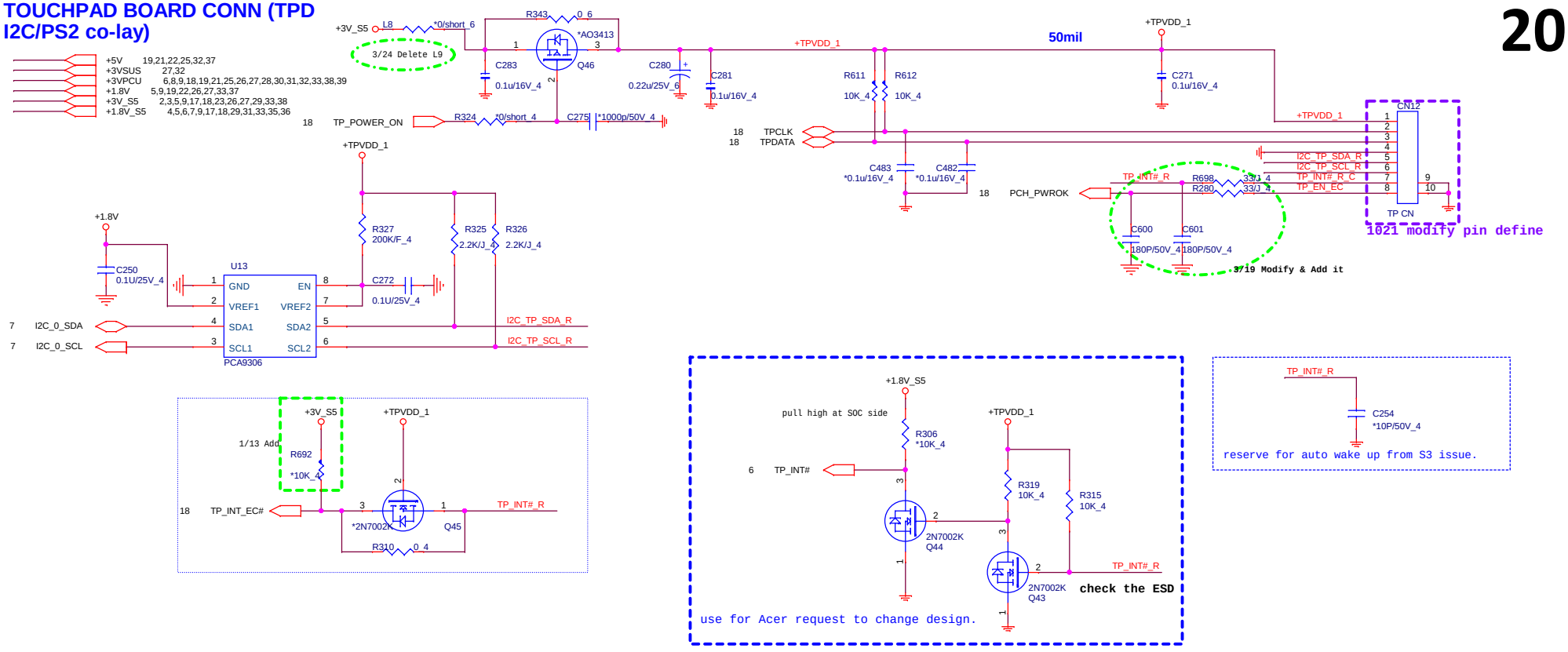




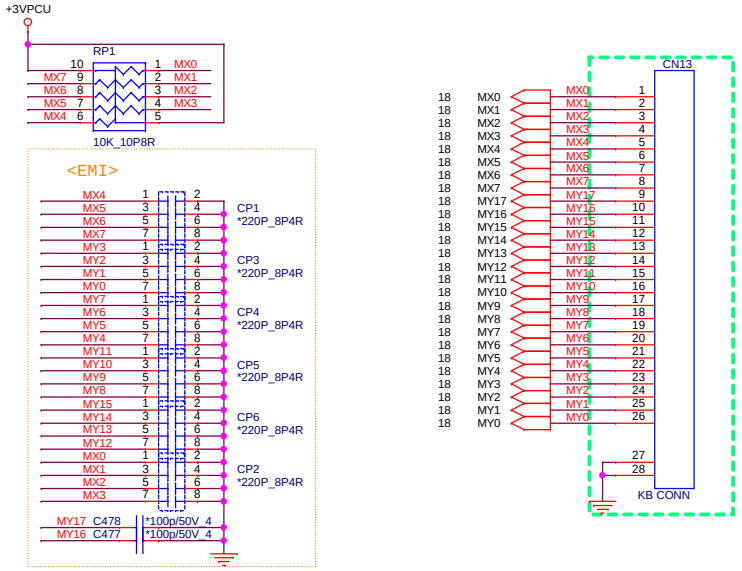
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	LCD/HDMI/Camera	1A
Date: Friday, April 10, 2015	Sheet 19 of 42	

TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



KEYBOARD (KBC)

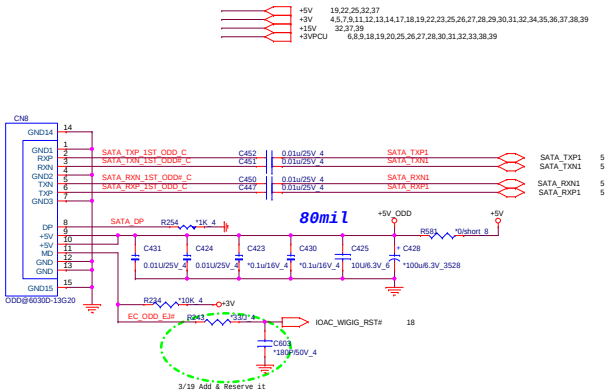


SWAP KB nets 10/21

KB_BL LED (KBC)

Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: KB/BT/TP/LED/Power Connector	Rev: 1A
Date: Monday, April 13, 2015	Sheet 20 of 42	

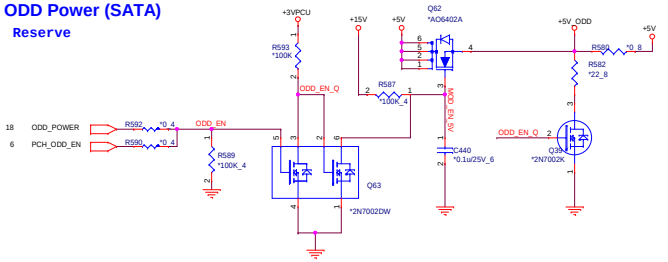
SATA ODD Connector



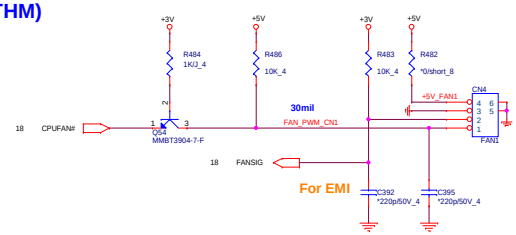
SATA ODD Re-driver

ODD Power (SATA)

Reserve



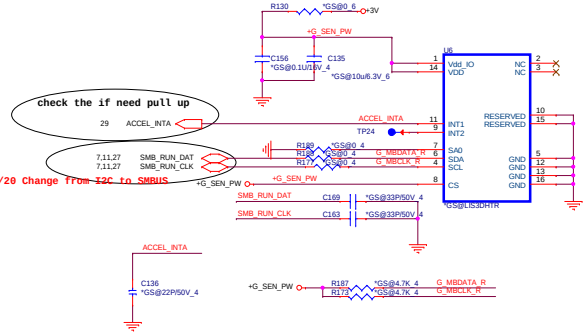
CPU FAN CTRL(THM)



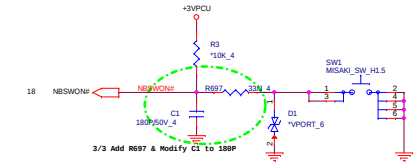
CPU Thermal sensor(THS) / MB Local TEMP

Reserve

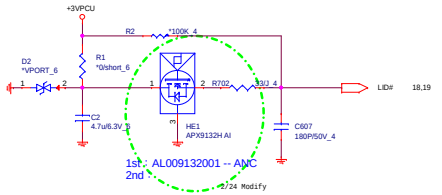
G-sensor



Power Switch. (FSW)



Hall Sensor (HSR)

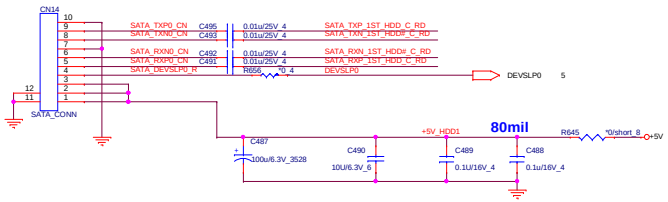


Quanta Computer Inc.
PROJECT ZYLB/ZYLC

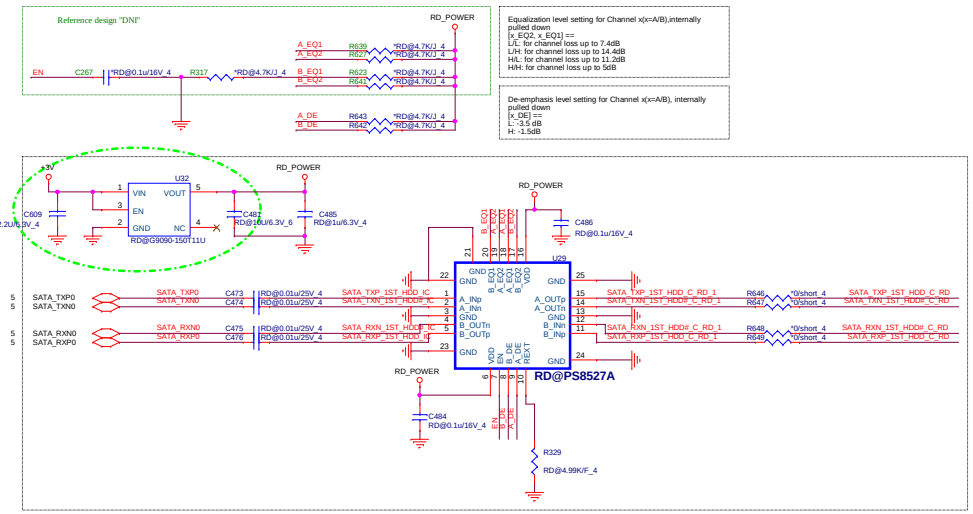
Size	Document Number	Rev
	ODD/FAN/Hall/PSW	1A
Date: Friday, April 10, 2015	Sheet 21 of 42	

SATA HDD1

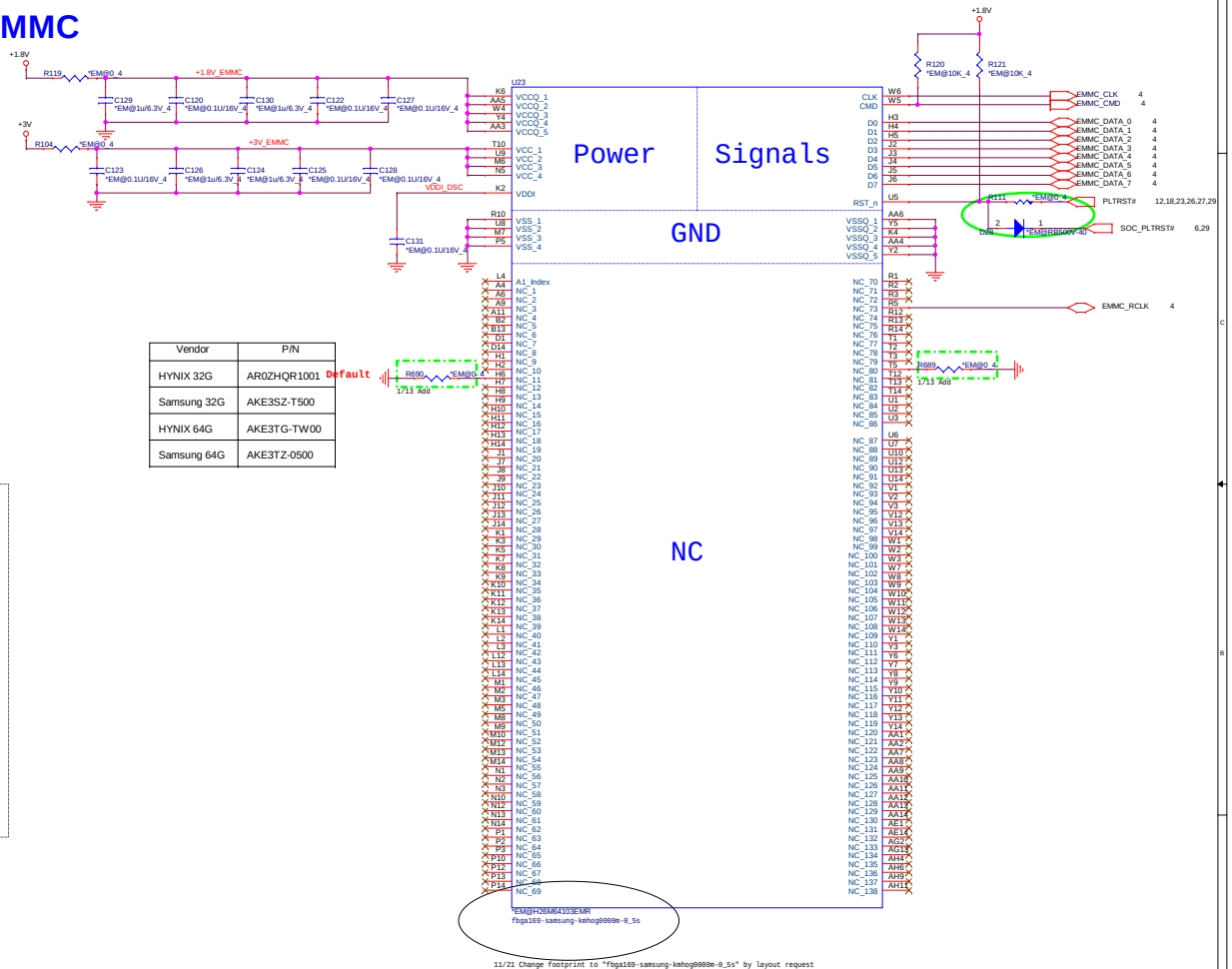
HDD1



HDD1 SATA Re-driver



eMMC

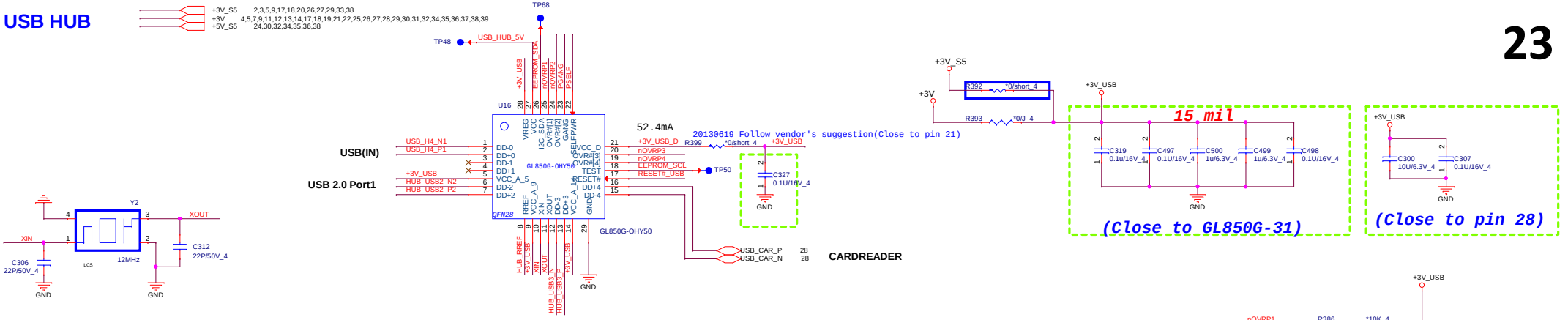


Vendor	P/N
HYNIX 32G	AR0ZHQR1001 Default
Samsung 32G	AKE3SZ-T500
HYNIX 64G	AKE3TG-TW00
Samsung 64G	AKE3TZ-0500

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

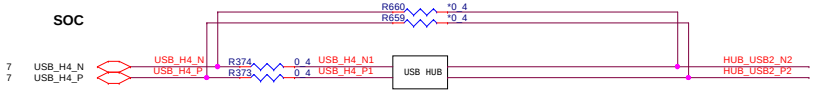
Size	Document Number	Rev
	SATA HDD/SATA REDRIVER	1A
Date: Friday, April 10, 2015	Sheet 22 of 42	

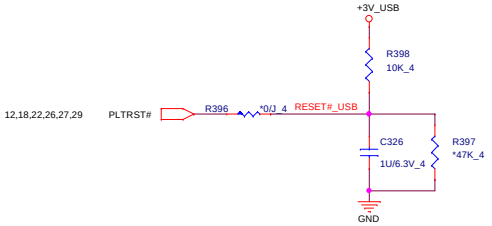
USB HUB

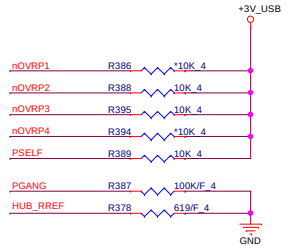


Reserve for debug

SOC

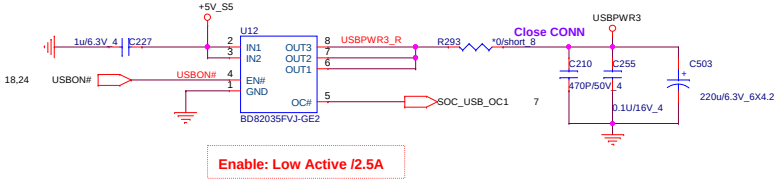




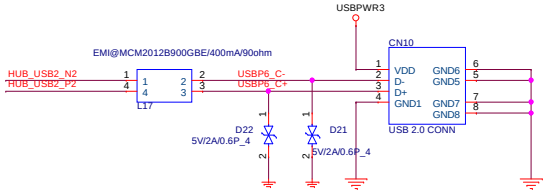


OVCURn#	Non-Removable Configuration of Portn
Floating	Non-removable
Pull high	Removable

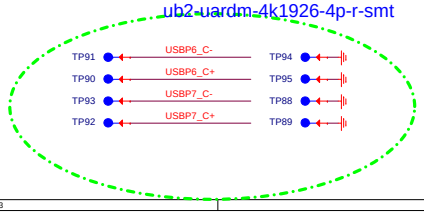
USB 2.0 CONNECTOR X2



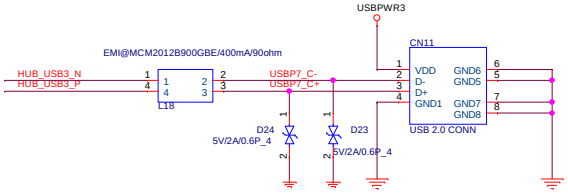
USB 2.0 Port1



Main: DFHD04MR377
ub2-uardm-4k1926-4p-r-smt



USB 2.0 Port2



Main: DFHD04MR377
ub2-uardm-4k1926-4p-r-smt

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	USB CONN/USB HUB	1A

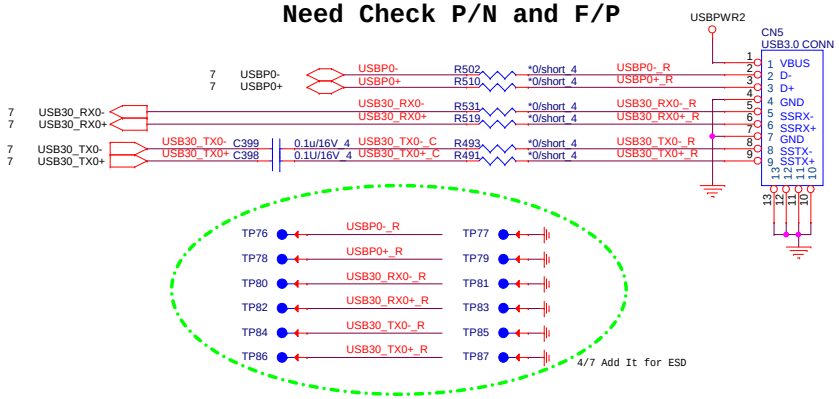
Date: Friday, April 10, 2015 Sheet 23 of 42

USB 3.0 Connector

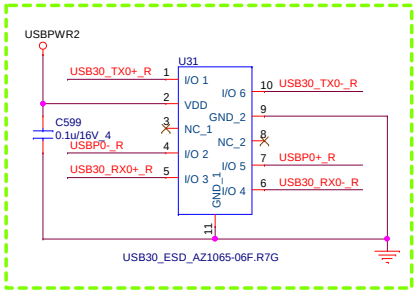
USB 3.0 Port1

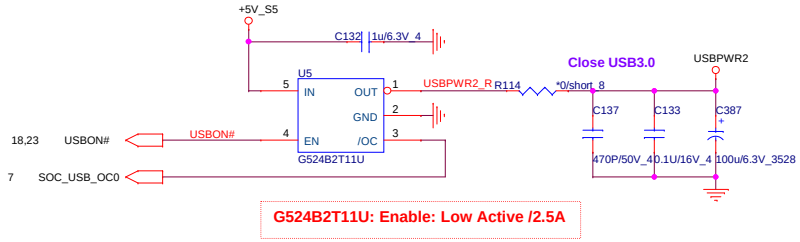
+5V_S5 23,30,32,34,35,36,38

Need Check P/N and F/P



2/26 add

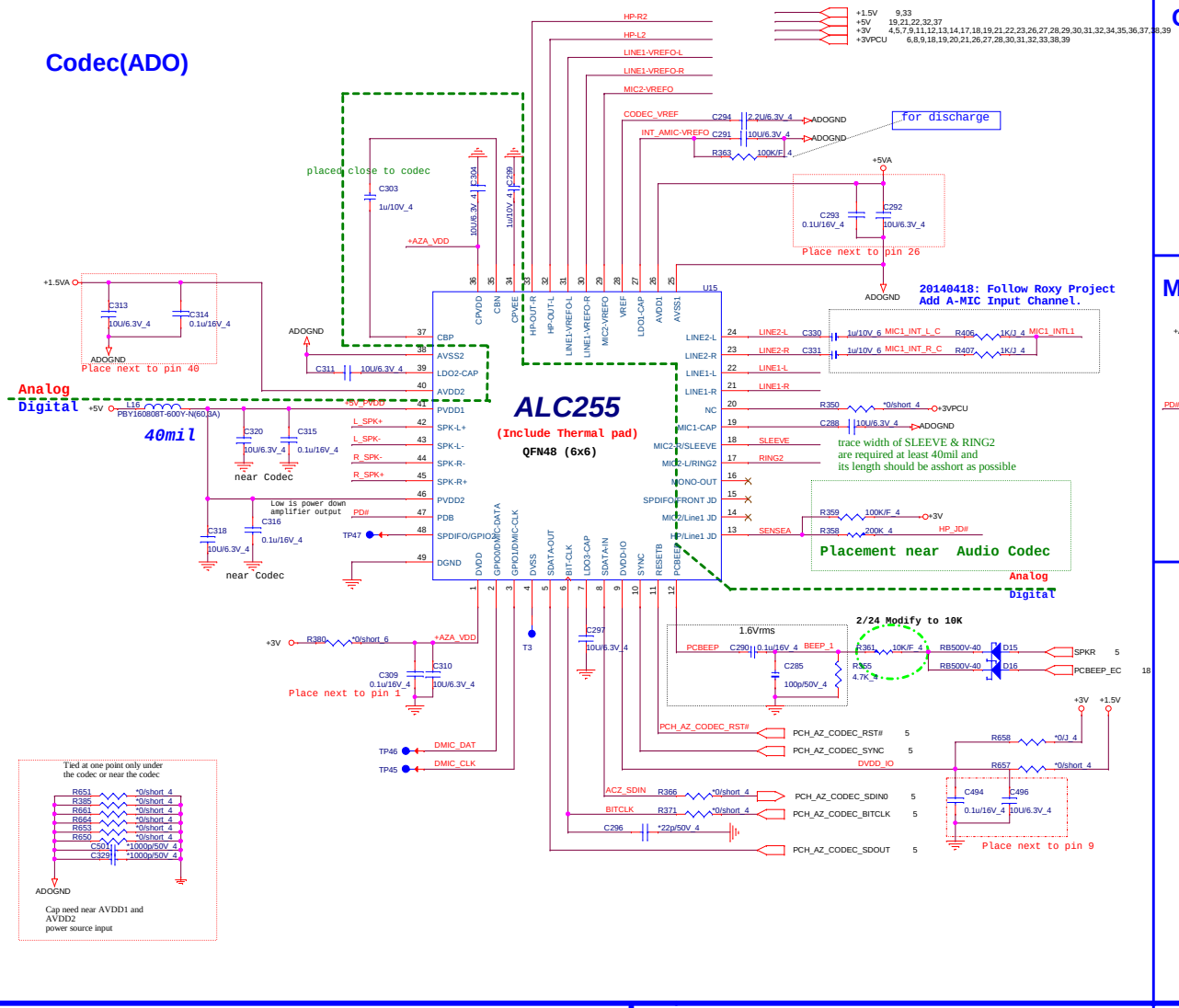




G524B2T11U: Enable: Low Active /2.5A

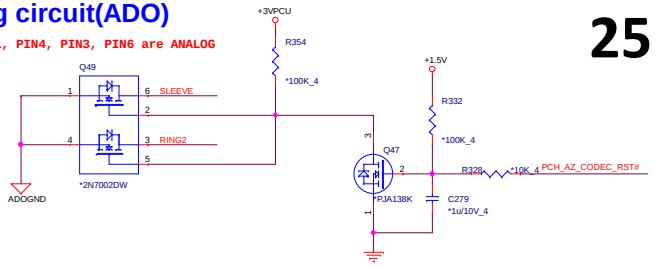
Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: USB 3.0	Rev: 1A
Date: Friday, April 10, 2015	Sheet 24 of 42	

Codec(ADO)

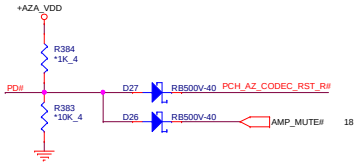


Grounding circuit(ADO)

PIN1, PIN4, PIN3, PIN6 are ANALOG

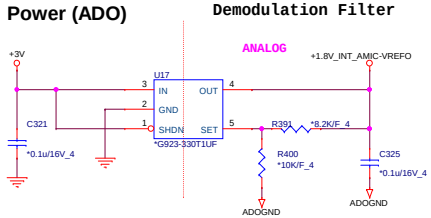


Mute(ADO)



Power (ADO)

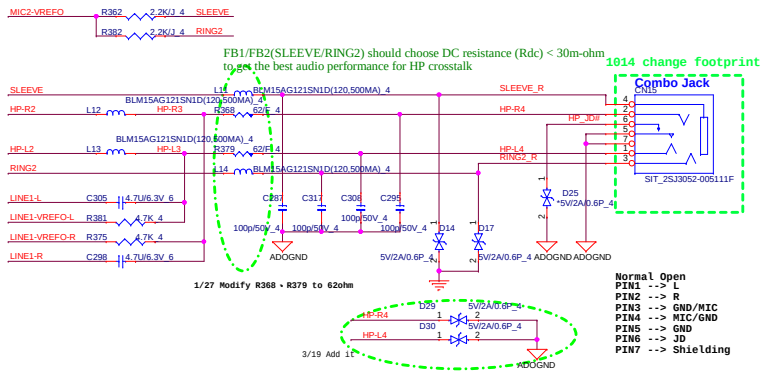
Demodulation Filter



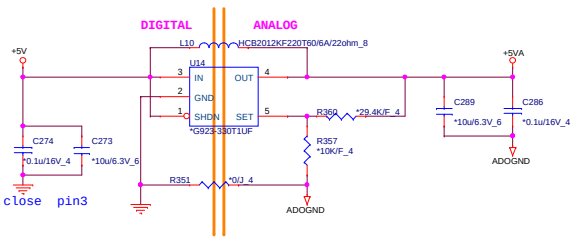
Vset =1.25V

Vout =Vset[1+AR(1,2)/AR(2,GND)]

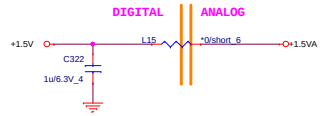
HEADPHONE/MIC/LINE combo (ADO)



Codec PWR 5V(ADO)



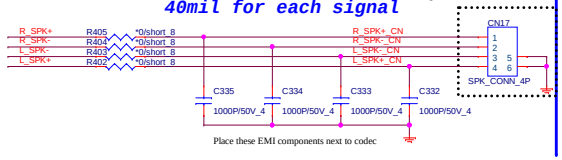
Codec PWR 1.5V(ADO)



Internal Speaker

40mil for each signal

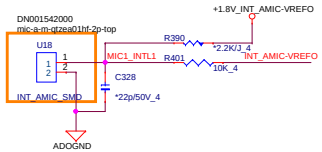
change connector 10/30



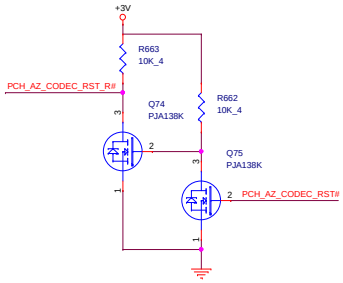
A-Mic

Analog-MIC

8/1 Change CN1 footprint to mic-a-m-qtzea01hf-2p-top .



Level shift



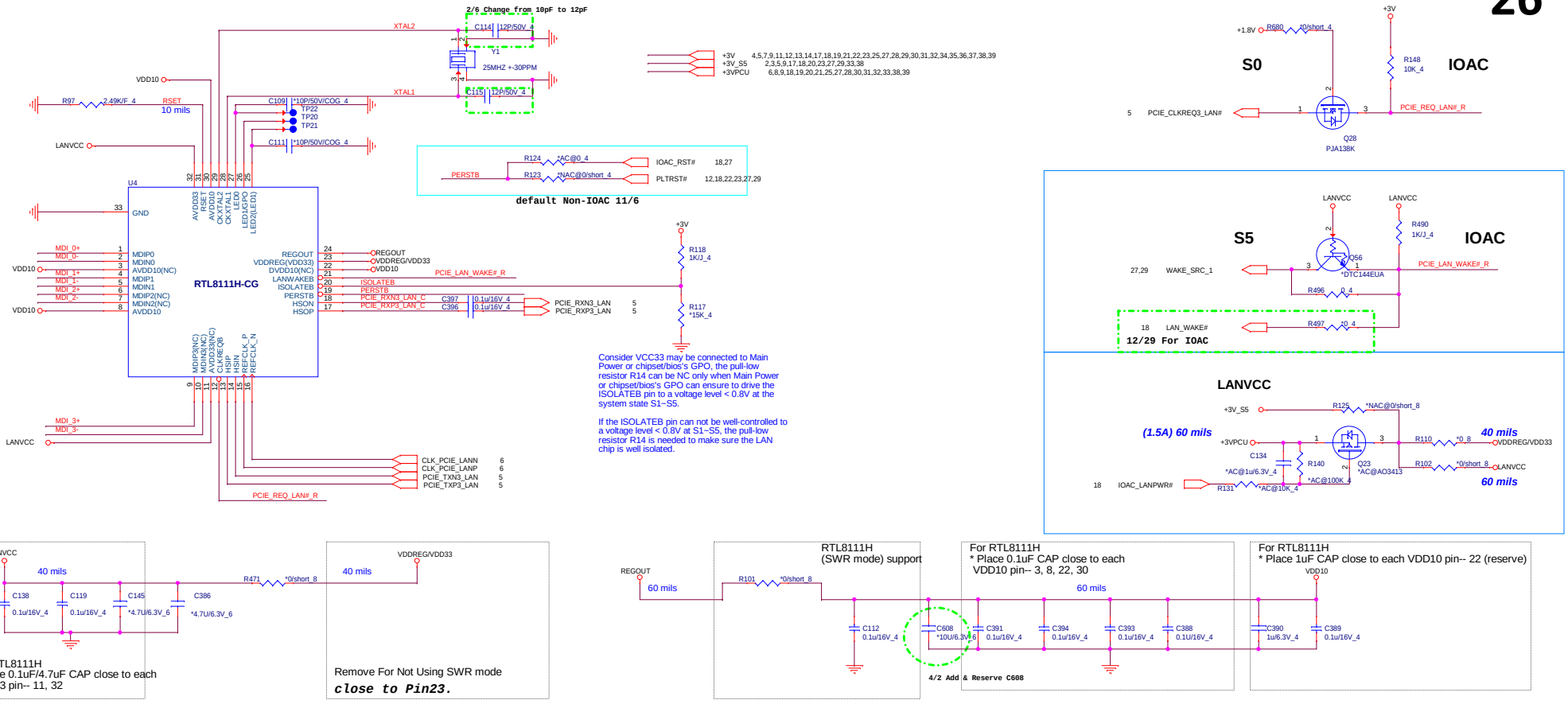
Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Codec ALC3225	1A

Date: Friday, April 10, 2015 Sheet 25 of 42

LAN



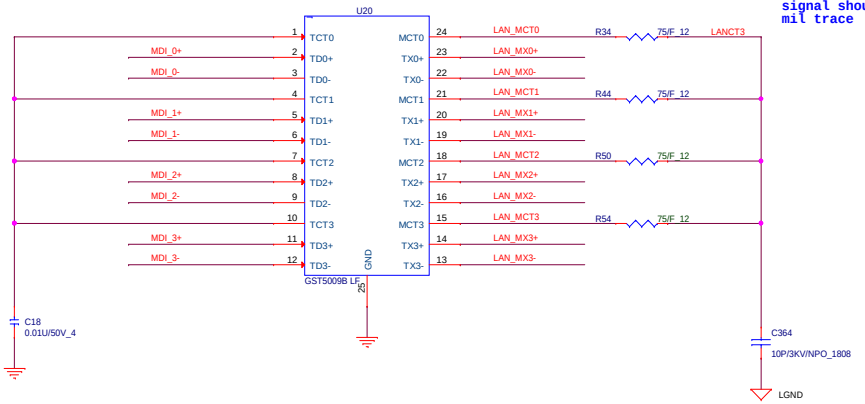
Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

Tramsformer

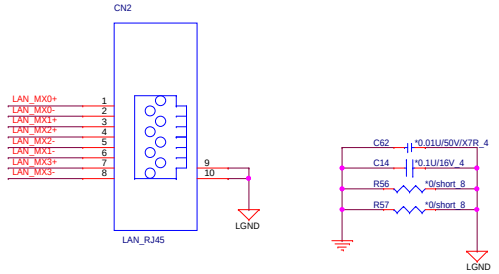
Change footprint from "ssop24-11-1" to "trf-n1010g-25p" 11/21

Layout:All termination signal should have 30 mil trace



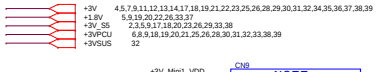
RJ45 Connector

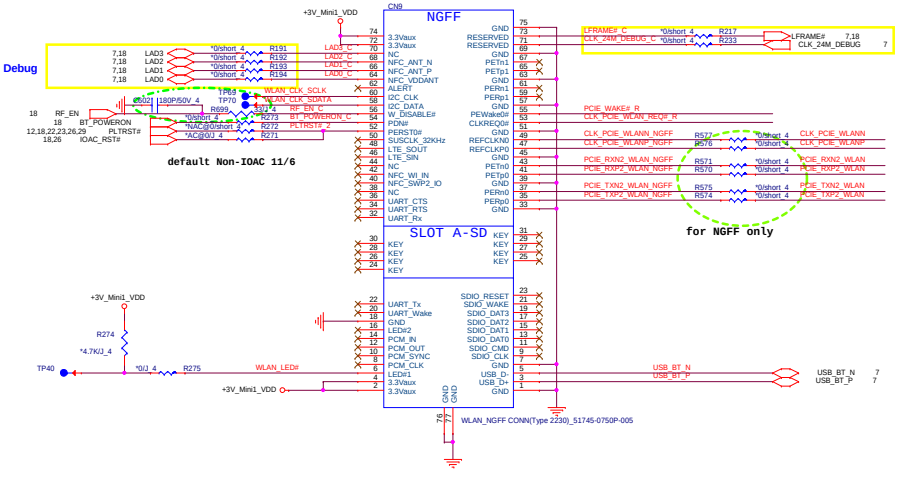
Need Check P/N and F/P



Quanta Computer Inc.			
PROJECT : ZYLB/ZYLC			
Size	Document Number: LAN		Rev: 1A
Date: Friday, April 10, 2015	Sheet 26 of 42		

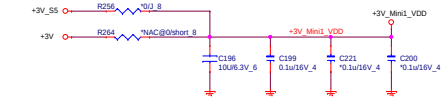
WLAN

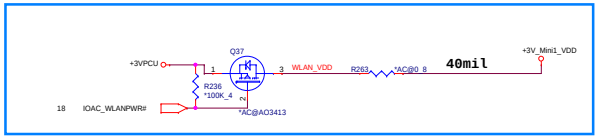


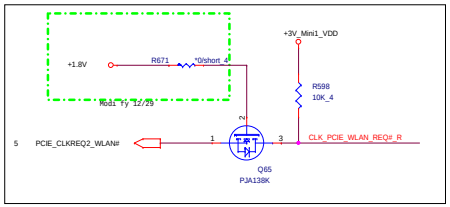


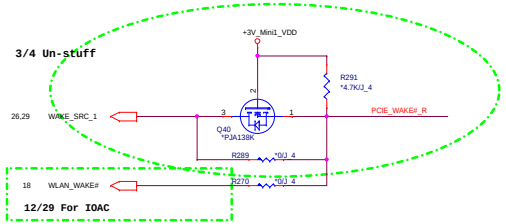
	NGFF	mPCIE
R577 R576 R571 R570 R575 R574	Stuff	Un-Stuff
R572 R573	Un-Stuff	Stuff

Default

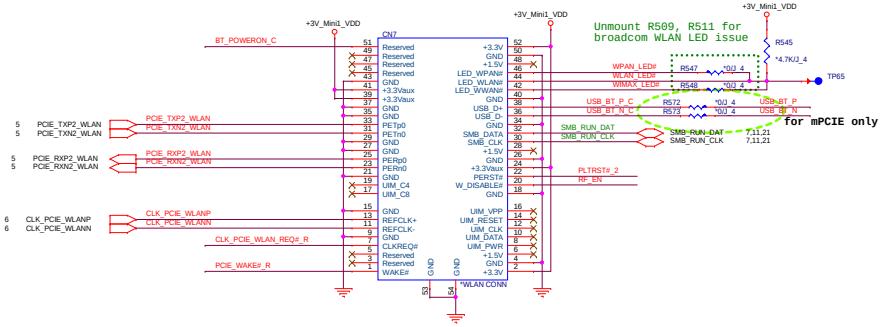






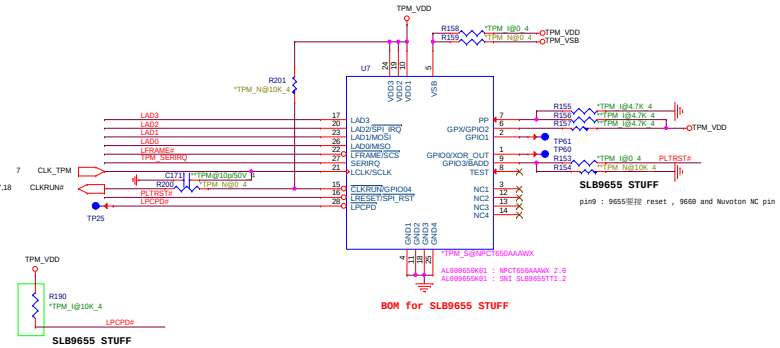


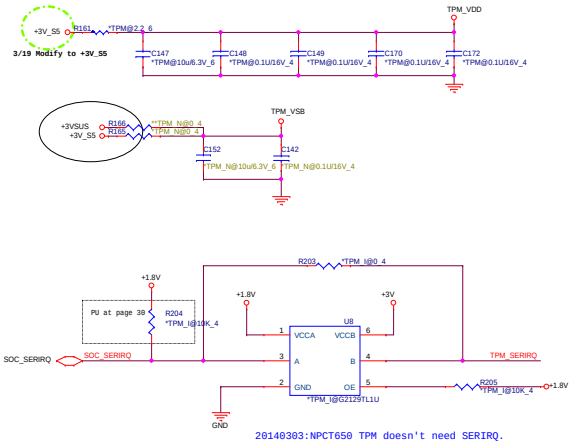
MINI PCI-E



TPM (TPM)

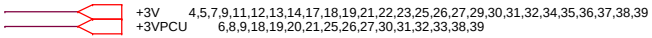
BOM default for NPCT650AAWX

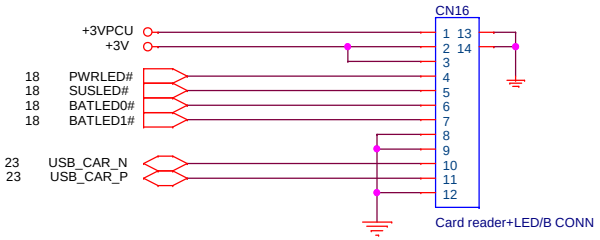


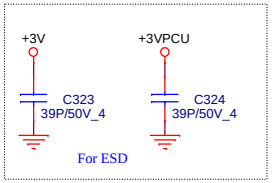


Quanta Computer Inc.			
PROJECT : ZYLB/ZYLC			
Size	Document Number		Rev
	WiFi & BT & TPM		1A
Date: Friday, April 10, 2015		Sheet 27 of 42	

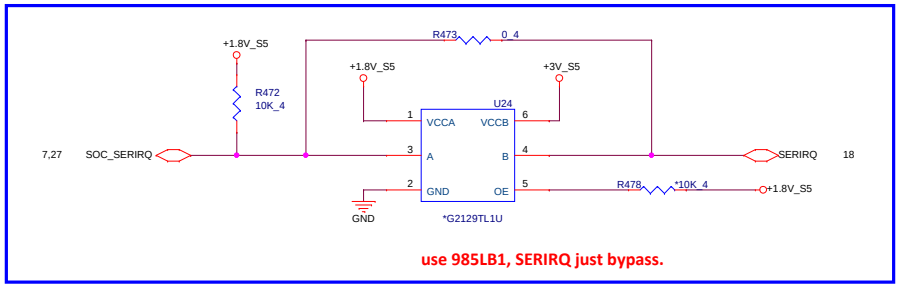
Card Reader+ LED/B Connector

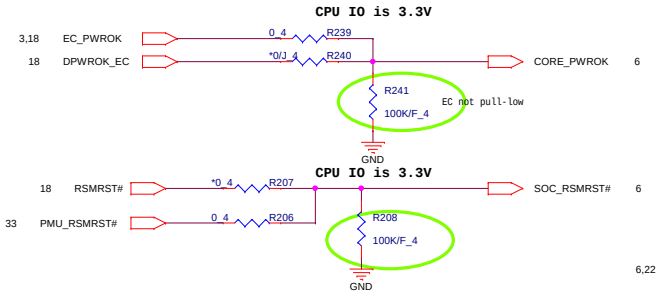


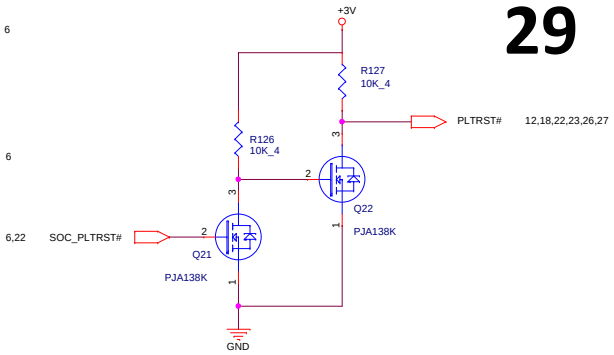


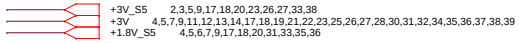


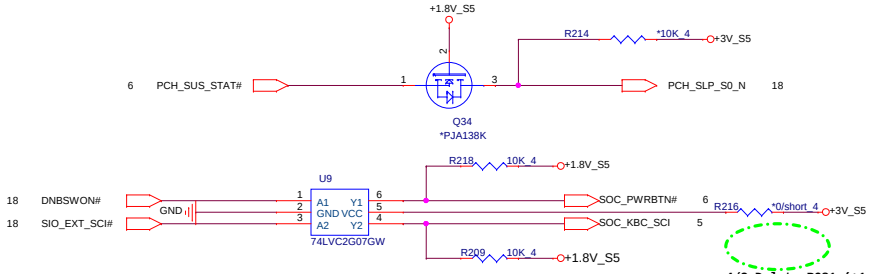
Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: Card Reader+ LED/B Connector	Rev: 1A
Date: Friday, April 10, 2015	Sheet 28 of 42	

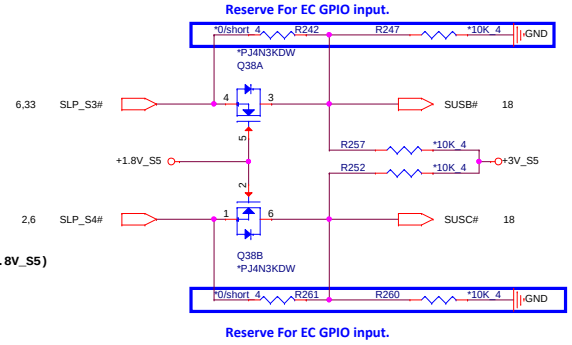


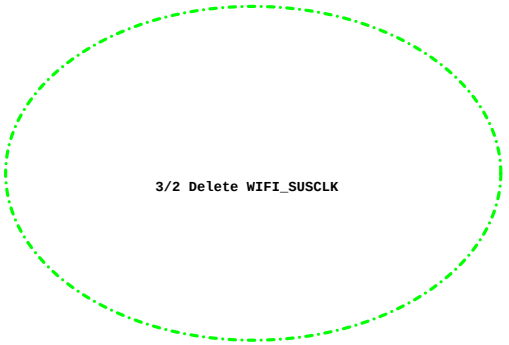


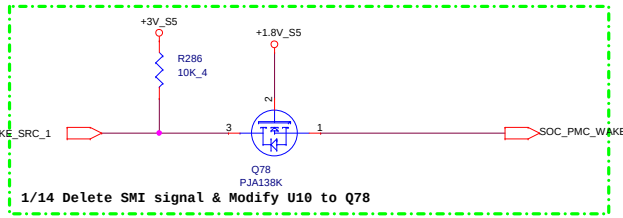


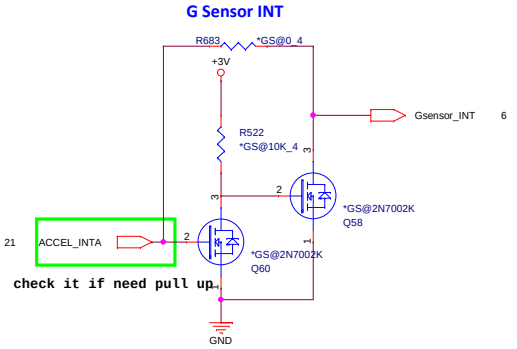


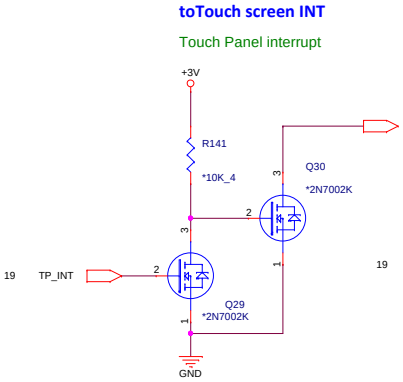


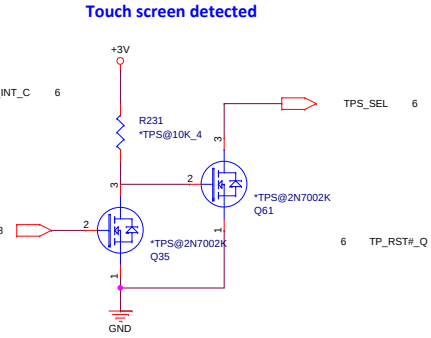


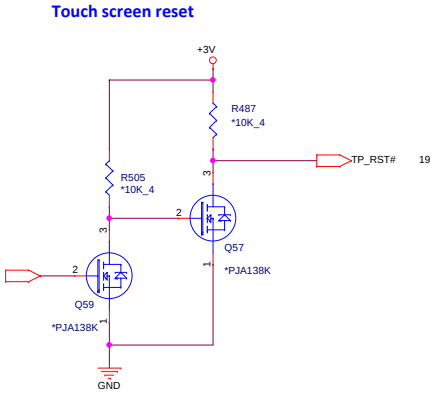












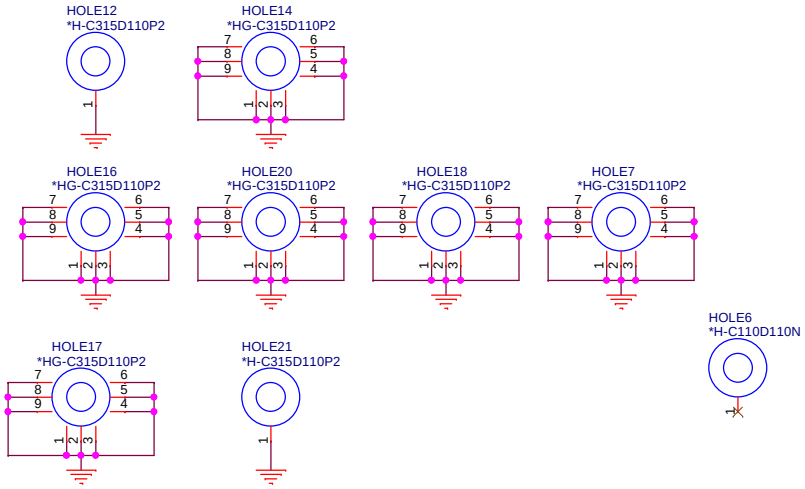
Quanta Computer Inc.

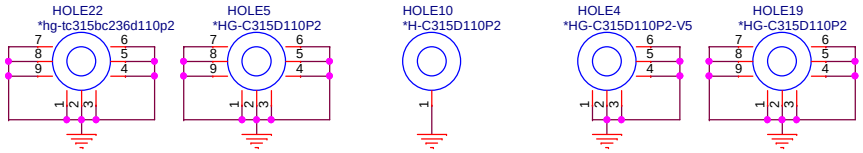
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Level Shift	1A

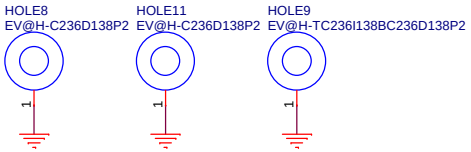
Date: Friday, April 10, 2015 Sheet 29 of 42

HOLE(OTH)

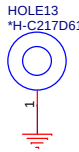




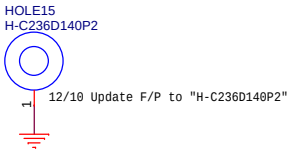
GPU nuts



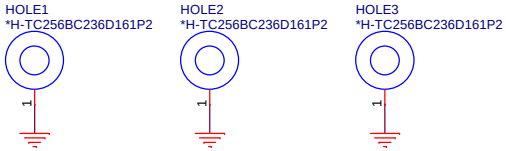
Mini card nuts

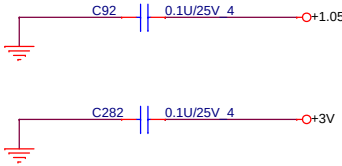


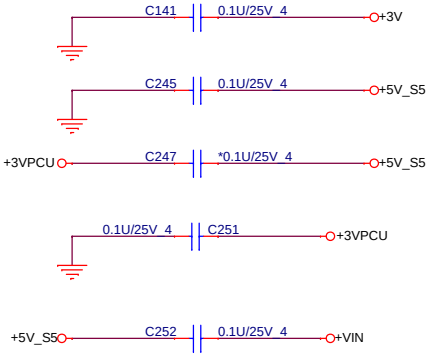
M.2 (NGFF)nuts

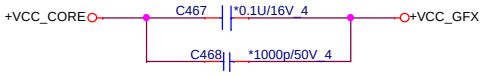


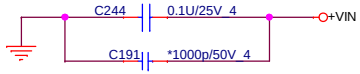
CPU nuts











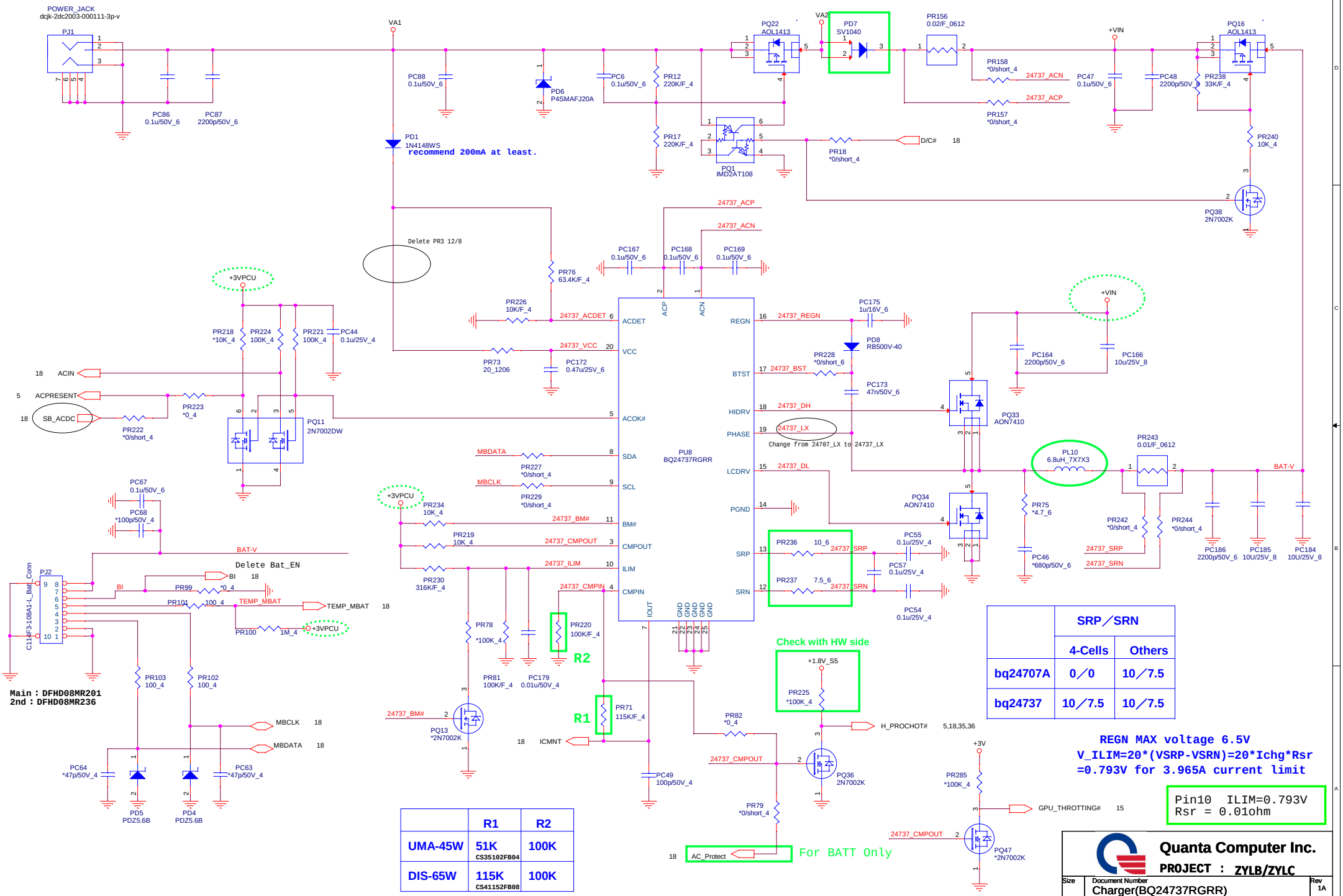
Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	USB BOARD CONN	1A

Date: Friday, April 10, 2015 Sheet 30 of 42

DFPJ06MR015-- 65W
DFPJ03MR043--- 45W



	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

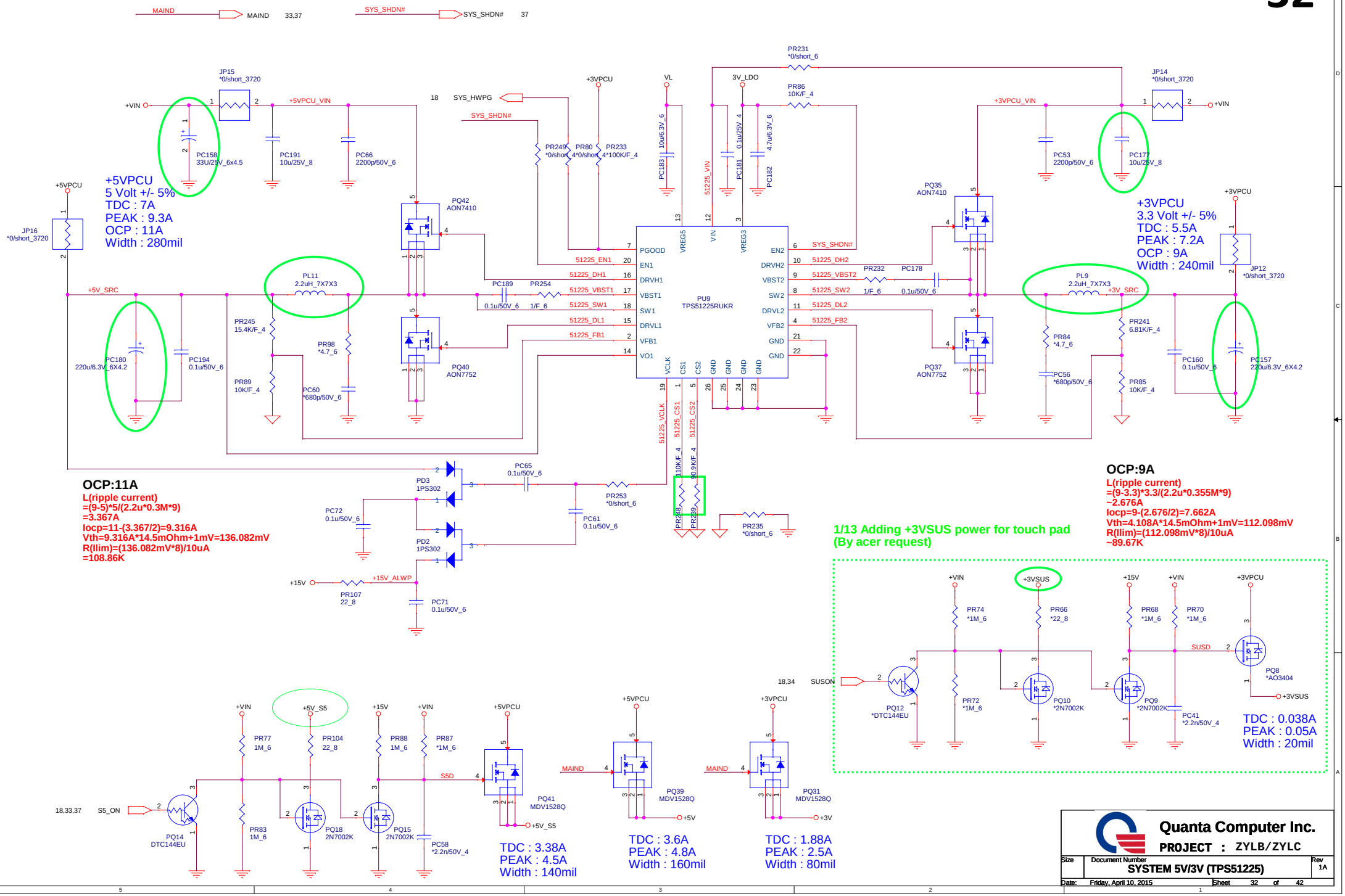
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

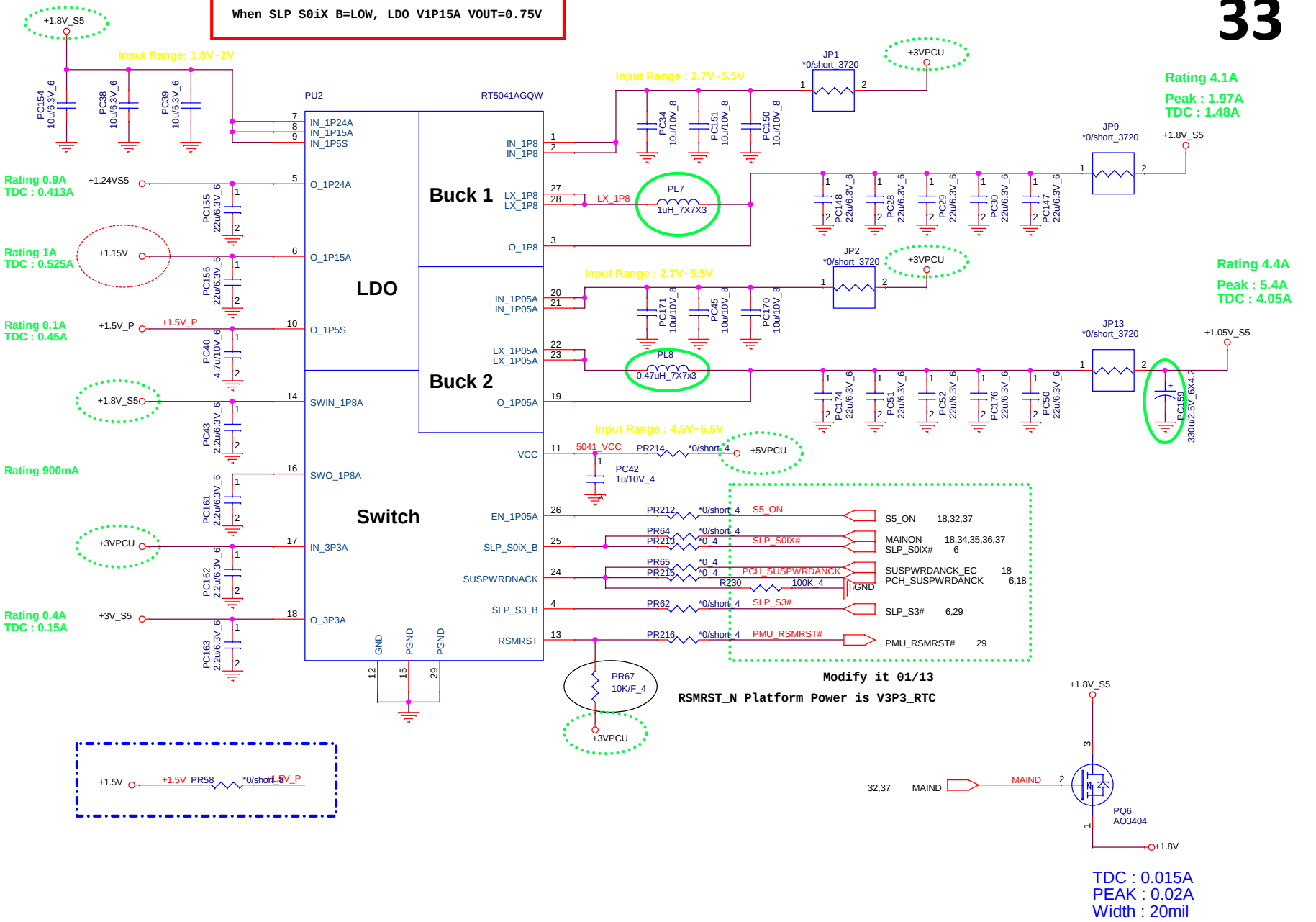
	R1	R2
UMA-45W	51K CS35102FB04	100K
DIS-65W	115K CS41152FB08	100K

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

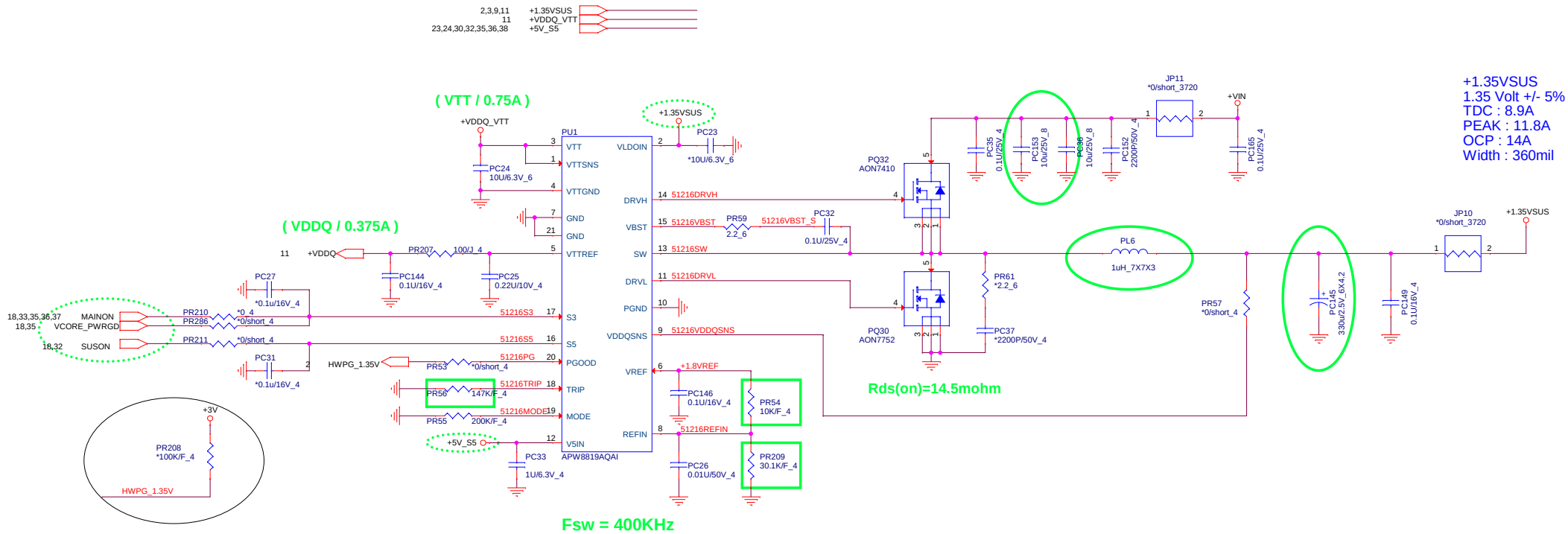
Size	Document Number	Rev
	Charger(BQ24737RGRR)	1A
Date: Friday, April 10, 2015	Sheet 31 of 42	


MAIND
MAIND 33,37
SYS_SHDN#
SYS_SHDN# 37
+5VPCU
5 Volt +/- 5%
TDC : 7A
PEAK : 9.3A
OCP : 11A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 5.5A
PEAK : 7.2A
OCP : 9A
Width : 240mil
OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14.5mOhm+1mV=136.082mV
R(Ilim)=(136.082mV*8)/10uA
=108.86K
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.662A
Vth=4.108A*14.5mOhm+1mV=112.098mV
R(Ilim)=(112.098mV*8)/10uA
~89.67K
1/13 Adding +3VSUS power for touch pad
(By acer request)
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
TDC : 3.38A
PEAK : 4.5A
Width : 140mil
TDC : 3.6A
PEAK : 4.8A
Width : 160mil
TDC : 1.88A
PEAK : 2.5A
Width : 80mil
PU9
TPS51225RUKR
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
SYSTEM 5V/3V (TPS51225)
Size
Document Number
Rev
1A
Date: Friday, April 10, 2015
Sheet 32 of 42

When SLP_S0iX_B=High,LDO_V1P15A_VOUT=1.15V
When SLP_S0iX_B=LOW, LDO_V1P15A_VOUT=0.75V



Quanta Computer Inc.			
PROJECT : ZYLB/ZYLC			
Size: Custom	Document Number: PMIC (RT5041AGQW)		Rev: 1A
Date: Friday, April 10, 2015		Sheet 33 of 42	



+1.35VSUS
1.35 Volt +/- 5%
TDC : 8.9A
PEAK : 11.8A
OCP : 14A
Width : 360mil

OCP=14A
L ripple current
=(19-1.35)*1.35/(1u*400k*19)
=3.135A
Vtrip=14-(3.135/2)*14.5mohm
=180.269mV
Rlimit=180.269mV/10uA*8=144.21Kohm

DDR=1.35V
PR104=10K/F_4
PR106=30.1K/F_4

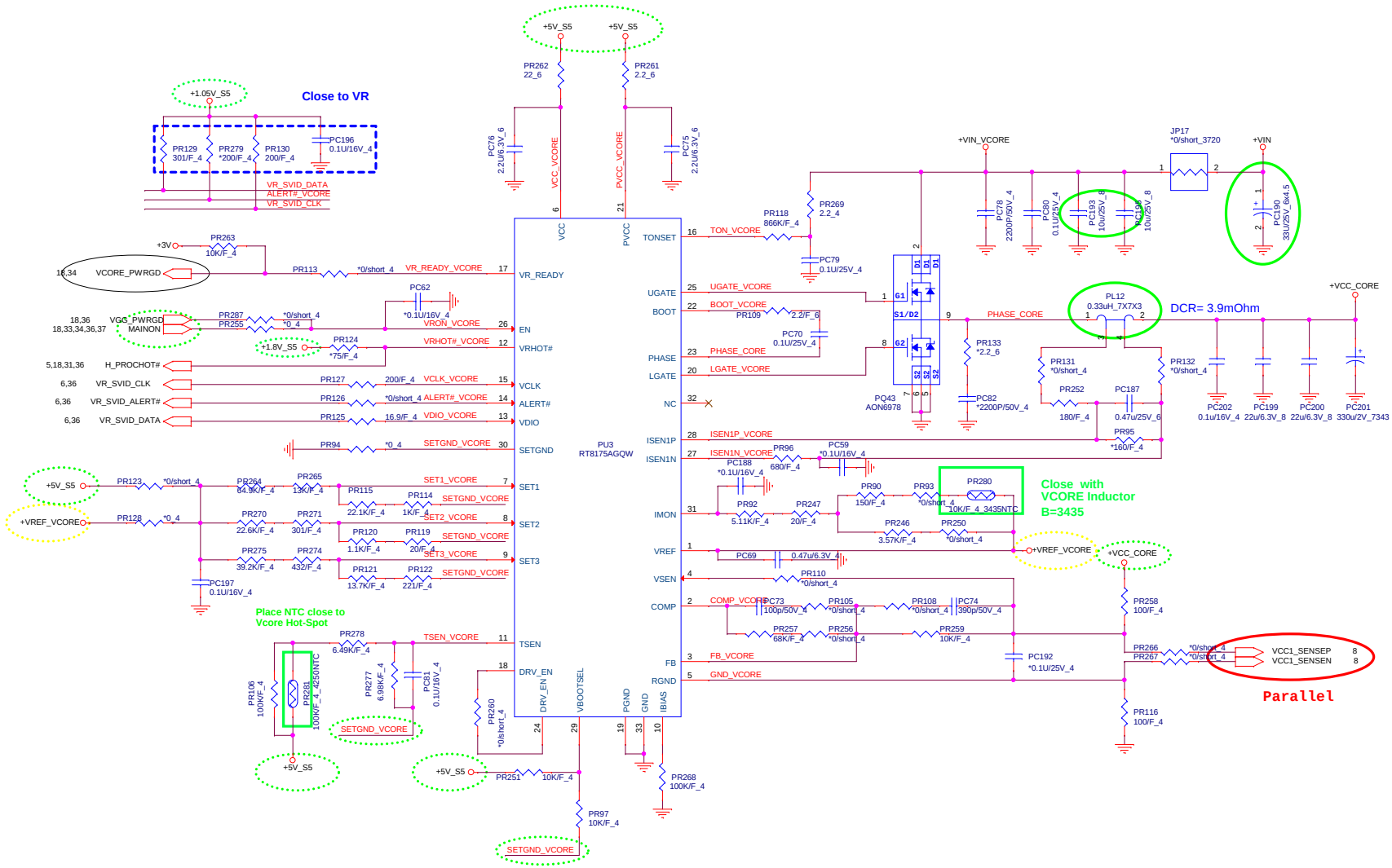
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT LC

Size	Document Number	Rev
	DDR3L (APW8819)	1A

Date: Friday, April 10, 2015 Sheet 34 of 42



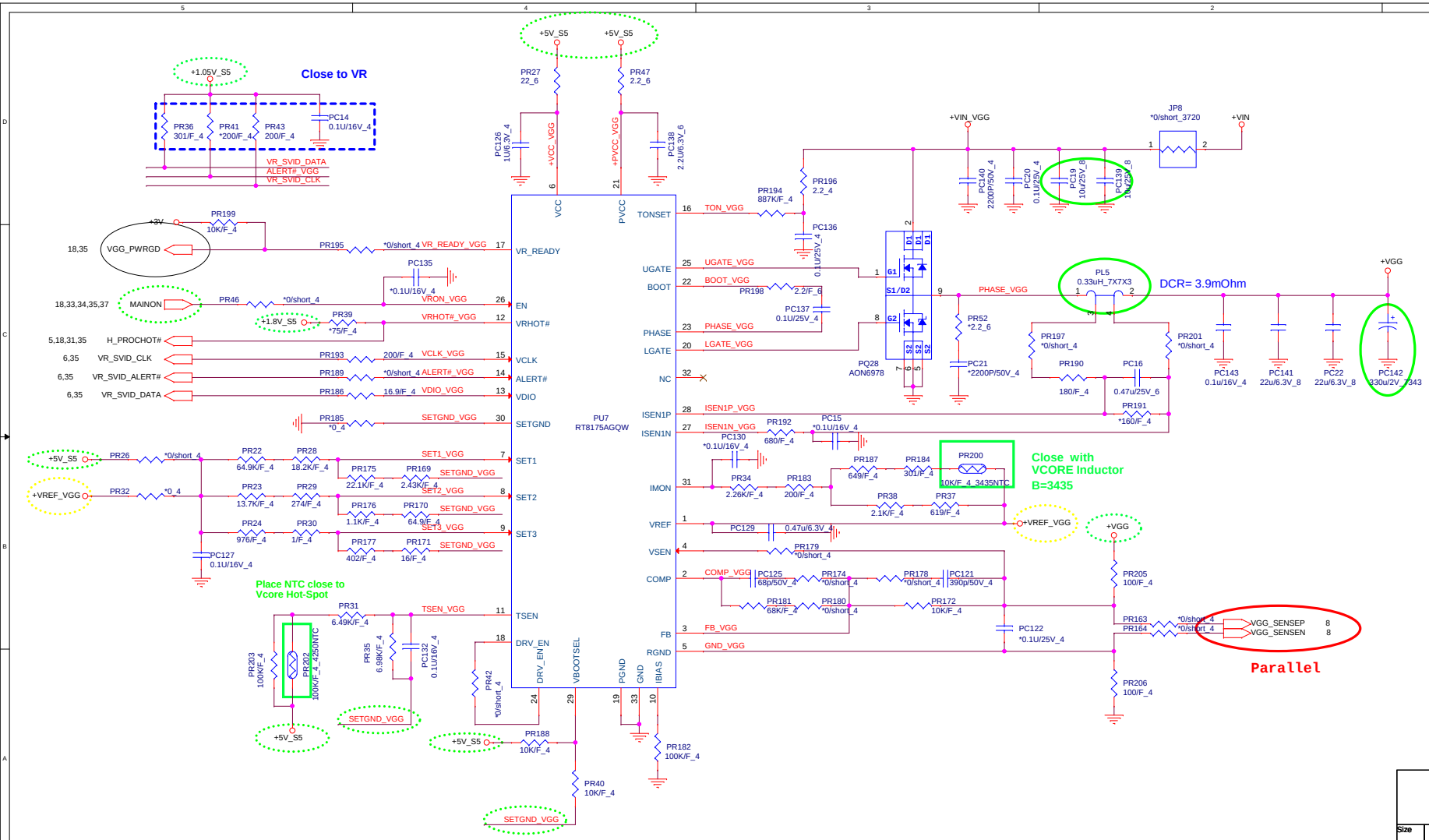
VR 12.1

Braswell - VCC0+1 (1 Phase)

Icc TDC PL2：TBD
Icc Max：7A
OCP：12.4A
Fsw：800KHz
Vboot：1V
VR address：0

VCC0+1 L/L：
R_DC_LL：0 mV/A
R_AC_LL：0 mV/A

Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number: VCC0+1 (RT8171BGQW)	Rev: 1A
Date: Friday, April 10, 2015	Sheet 35 of 42	



VR 12.1

Braswell - VGG (1 Phase)

Icc TDC PL2：TBD

Icc Max：15A

OCP：20.7A

Fsw：800KHz

VR Address：5

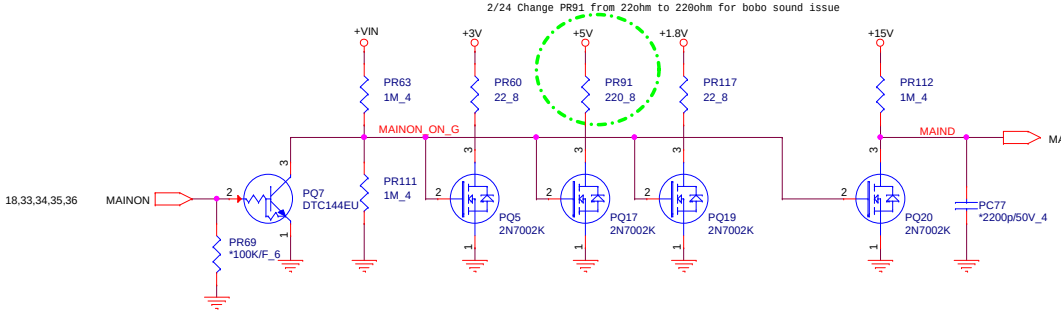
VCORE L/L：

R_DC_LL：0 mV/A

R_AC_LL：0 mV/A

Quanta Computer Inc.		
PROJECT ：ZYLB/ZYLC		
Size	Document Number +VGG (RT8171BGQW)	Rev 1A
Date: Friday, April 10, 2015	Sheet 36 of 42	

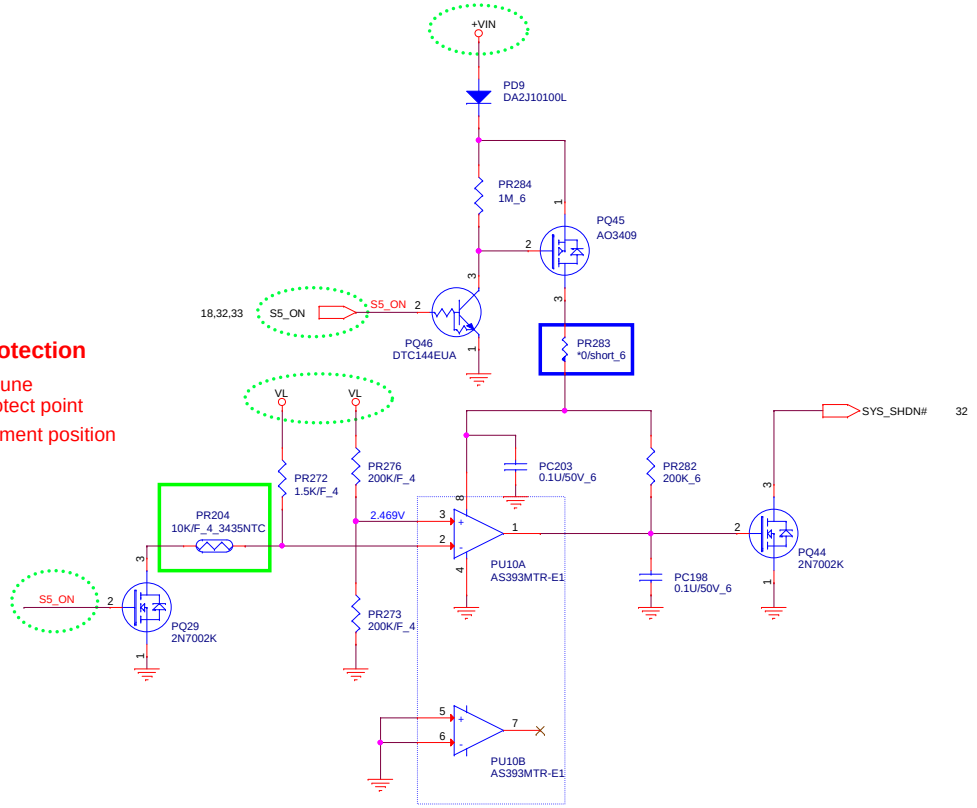
2/24 Change PR91 from 22ohm to 220ohm for bobo sound issue



Thermal Protection

(1) Need fine tune
for thermal protect point

(2) Note placement position



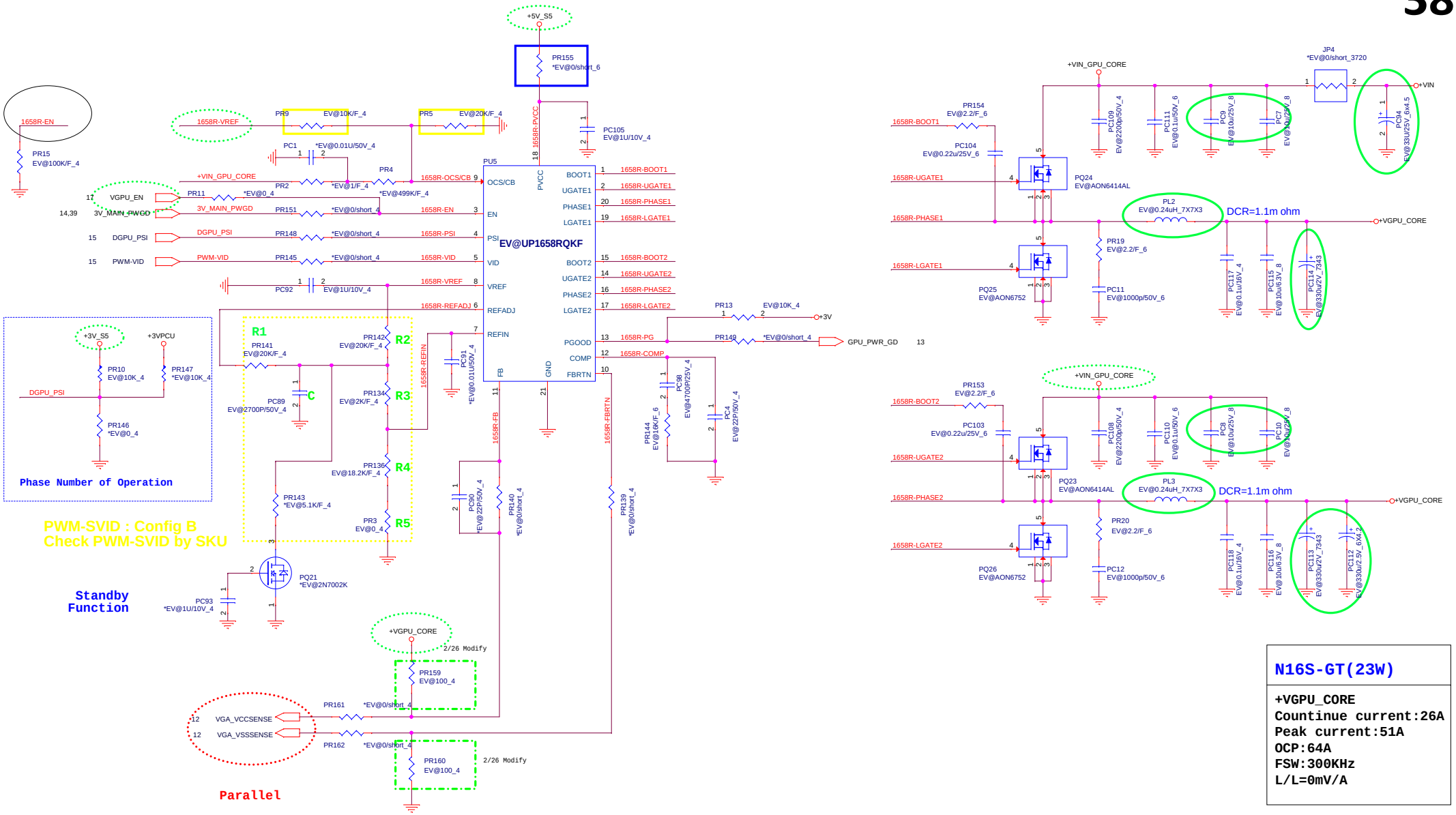
For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Thermal / Discharge	1A

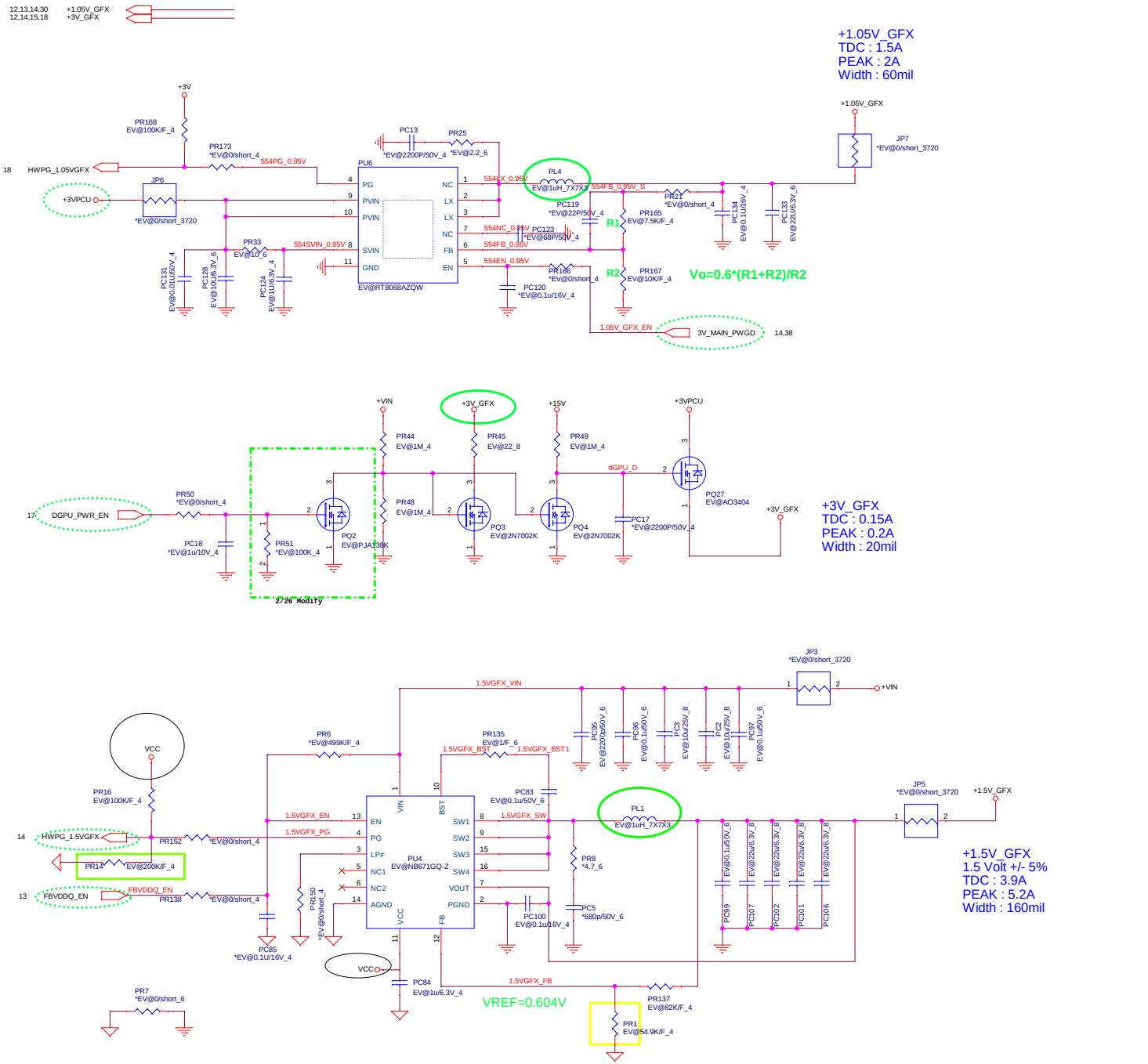
Date: Friday, April 10, 2015 Sheet 37 of 42



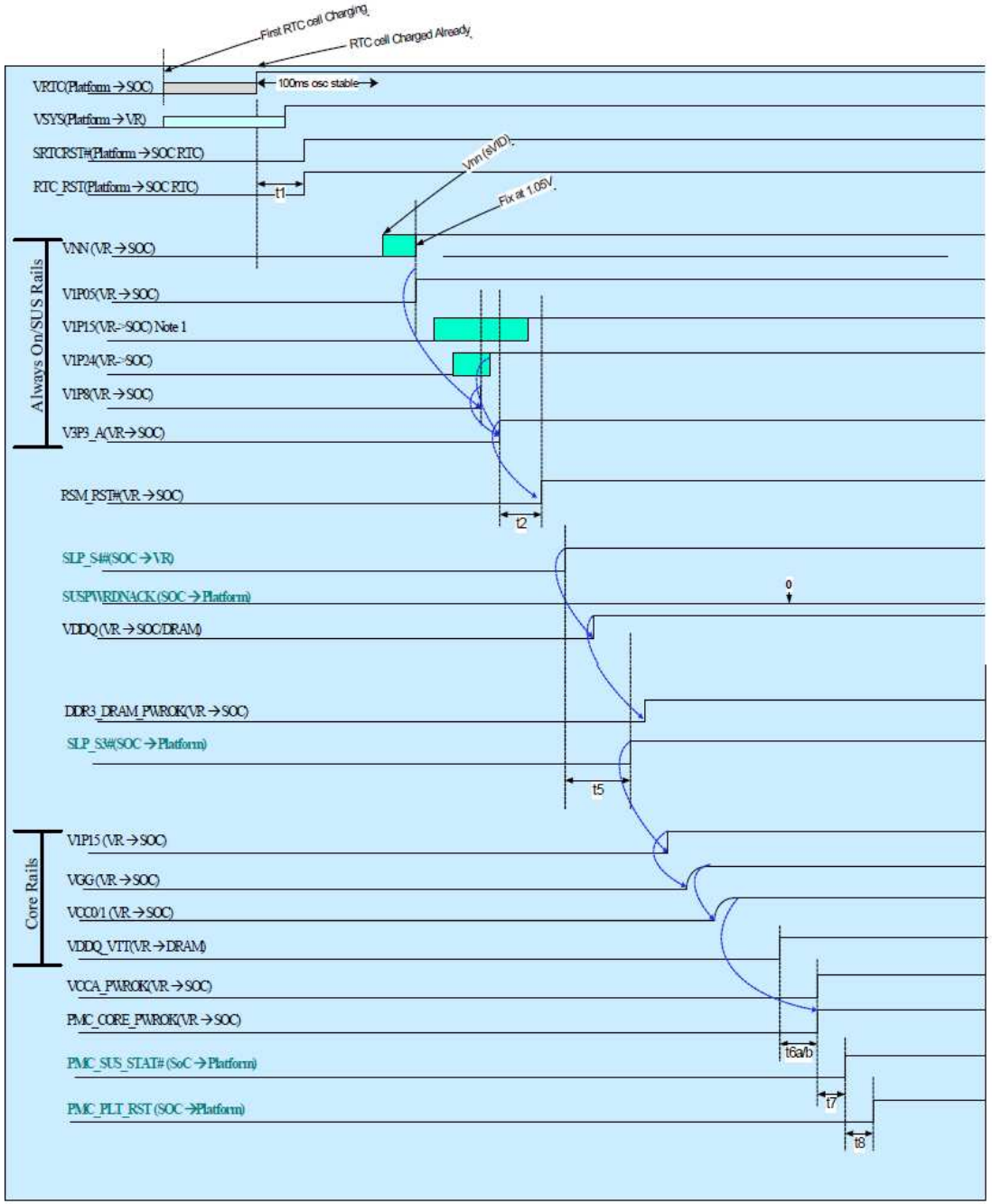
N16S-GT(23W)

+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:64A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.		
PROJECT : ZYLB/ZYLC		
Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	1A
Date: Friday, April 10, 2015	Sheet 38 of 42	


12,13,14,30 +1.05V_GFX
12,14,15,18 +3V_GFX
+1.05V_GFX
TDC : 1.5A
PEAK : 2A
Width : 60mil
Vo=0.6*(R1+R2)/R2
+3V_GFX
TDC : 0.15A
PEAK : 0.2A
Width : 20mil
+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.9A
PEAK : 5.2A
Width : 160mil
VREF=0.604V
EV@RT8068AZQW
EV@NB671GQ-Z
2726 Modify
Quanta Computer Inc.
PROJECT : ZYLB/ZYLC
+1.5V_GFX/+1.05V_GFX/+3V_GFX
Friday, April 10, 2015
Sheet 39 of 42

Braswell S4/S5 to S0 (Power Up) Sequence



Platform Power Up Timing (G3 to S0)

Parameter	Description	Minimum	Maximum	Units
t1	RTC_VCC to RTC_RST# de-assertion	9	-	ms
t2	V3P3A (SUS Rails) valid to RSMRST# de-assertion (t1 still applies in applications without RTC battery)	10		µS
t3	RSMRST# to Internal RTC Clock stable2	95		ms
t4	Internal RTC Clock stable to PMC_SUSCLK[0] toggling	5		ms
t5	PMU_SLP_S4# de-assertion to PMU_SLP_S3# de-assertion	26		µs
t6a	Core well stable to DDR3_DRAM_PWROK and PMC_CORE_PWROK assertion (NO PCIe* devices)	10		ms
t6b	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by PCIe* devices)	99		ms
t7	PMC_CORE_PWROK to PMC_SUS_STAT#	1		ms
t8	PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion	60		us

Model	REV	CHANGE LIST	ZYLB/ZYLC MB

ZYLB MB

REV.A

1 2014/11/28 Add R4213 & delete R689 to follow Intel circuit (page 6)

1 2014/12/03 Change Hole30 footprint to "H-C236D142P2" (page 30)

2 2014/12/03 Change R4192 & R350 from short0402 to RC0402 (page 22)

1 2014/12/04 Delete M_A_MON1P & M_A_MON1N (page 2)

1 2014/12/08 Delete PR3 (page 31)

1 2014/12/10 Change Hole30 footprint to "H-C236D140P2" (page 30)

1 2014/12/16 Change R361 from 47K to 22K (CS32202FB18) & R290 from 1u to 0.1uF(CH4103K1B08) (page 25)

REV.B

1 2014/12/29 Reserve R669 for EMMC 5.0 device (page 4)

2 2014/12/29 Change Q65 pin2 to +1.8V (page 4)

3 2014/12/29 Add Q77 for "PCIE_CLKREQ0_VGA#" (page 12)

4 2014/12/29 Add "SOC_VCCAPWROK" Schematic (page 3)

5 2014/12/29 Change U6 pin1 & pin14 to +3V (page 21)

6 2014/12/29 Change Q28 pin2 to +1.8V (page 26)

7 2014/12/29 Change U9 pin5 to +3V_S5 (page 26)

8 2014/12/29 Add R683 for reserve (page 26)

9 2014/12/29 Stuff R477、R470 & Change R470 to 3.3K (page 26)

10 2014/12/29 Change debug port to NGFF CONN(CN9) (page 27)

11 2014/12/29 Delete C456、C433、C461 & Add C503 (page 23)

12 2014/12/29 Delete "BIOS_STRAP" (page 5)

13 2014/12/29 Add "GPU_THROTTING#" Schematic (page 15、31)

1 2015/01/07 Add Hynix H5TC4G63CFR-N0C strap (page 15)

REV.C

1 2015/01/27 Un-stuff Q55、R489、R485、R532、R656 (page 5)

2 2015/01/27 Un-stuff R563、R498、R196、R503 & delete R178 (page 6)

3 2015/01/27 Change Board ID4 to M/B ID strap pin (Stuff R542 & Un-stuff R543) (page 6)

4 2015/01/27 Un-stuff R296 (page 7)

5 2015/01/27 Change SMB_SOC_DATA& CLK design (Delete Q19、R94、R95、R100、D4、D5，Add U30、C505、C504、R686、R687、R688) (page 7)

6 2015/01/27 Un-stuff R535 (page 9)

7 2015/01/27 Un-stuff R171 (page 11)

8 2015/01/27 Un-stuff GC6 parts (U2、C21、R77、R79、R26、R30、R24、R29、Q15、Q18、R87、R91、R23、R439、R437) (page 12、15、17)

9 2015/01/27 Swap CPUFAN# & THRM_MOINTOR ， Un-stuff R243、R244、R228、R279 ，Change R280 to 10ohm (page 18)

10 2015/01/27 Un-stuff Touch Screen parts (R413、R414、R14) ，Change R6 to 1K ohm (page 19)

11 2015/01/27 Delete L7 、Stuff Q46、R324 & Un-stuff R343 for Touchpad power control (page 20)

12 2015/01/27 Un-Stuff IOAC parts (R131、R140、R134、Q23、Q37、R263) (page 26、27)

13 2015/01/27 Un-Stuff R496、R289 & Stuff Q56、Q40 for leakage current issue (page 26、27)

14 2015/01/27 delete S0IX level-shift (Q64、R594) & un-stuff Q34、R214 for unuse (page 29)

15 2015/01/27 delete SMI signal (U10、R235、R232) & modify level-shift to Q78 (page 29)

16 2015/01/27 Un-stuff touch-screen level-shift Q29、Q30、Q35、Q61、Q57、Q59、R141、R231、R487、R505 (page 29)

17 2015/01/27 Un-stuff PR215 & stuff R230 for powe design (page 33)

18 2015/01/27 Un-stuff PR210、PR255、stuff PR286、PR287 to follow Intel power-on sequence (page 34、35)

19 2015/01/27 Un-stuff U26、C407、R546 for unuse (page 29)

20 2015/01/27 Stuff Q72、R652、R620 for EC request (page 6)

21 2015/01/27 Stuff R465、C369 for EMI request (page 19)

22 2015/01/27 Stuff C117 & change C268、C270、C265、C277、C276、C264、C385、C113、C177、C173、C384 to 22u/6.3V for Intel suggest (page 8)

23 2015/01/27 Change R468 to 10K to 1K (page 17)

24 2015/01/27 Change PU3/PU7 to RT8175AGQW 、 change PR262/PR27 to 22ohm、PR265 to 13K、PR114 to 1K 、PC73 to 100P、PL1 to 1uH、un-stuff PR94/PR185 for power requesr (page 35、36)

25 2015/01/27 Change R368/379 to 62ohm for vendor suggest (page 25)

REV.D

1 2015/02/05 Change C416/C419 from 18pF to 15pF for vendor suggest (page 6)

2 2015/02/05 Change C356/C357 from 10pF to 12pF for vendor suggest (page 14)

1 2015/02/24 Stuff D14、D17、D25 for ESD (page 25)

2 2015/02/24 Change HE1 source to AL009132001 (page 21)

3 2015/02/24 Change R361 from 22K to 10K for noise issue (page 25)

4 2015/02/24 Add C506 & change R465 to *100K/F_4 for EMI requset (page 19)

5 2015/02/24 Stuff D21、D22、D23、D24 for ESD (page 23)

6 2015/02/24 Change PR91 from 22ohm to 220ohm for Bobo sound issue (page 37)

Page	From	To
1		3A
2		3A
3		3A
4		3A
5		3A
6		3A
7		3A
8		3A
9		3A
10		3A
11		3A
12		3A
13		3A
14		3A
15		3A
16		3A
17		3A
18		3A
19		3A
20		3A
21		3A
22		3A
23		3A
24		3A
25		3A
26		3A
27		3A
28		3A
29		3A
30		3A
31		3A
32		3A
33		3A
34		3A
35		3A
36		3A
37		3A
38		3A
39		3A

Quanta Computer Inc.

PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Change List-1	1A

Date: Friday, April 10, 2015 Sheet 41 of 42

Model	REV	CHANGE LIST	ZYLB/ZYLC MB
ZYLB MB	REV.D	1 2015/02/25 Change R442 from 4.99K to 45.3K for vendor suggest(support Gen 3) (page 15)	
		1 2015/02/26 Change C114/C115 from 10pF to 12pF for vendor suggest (page 26) 2 2015/02/26 Add USB3.0 ESD component U31 & C599 (page 24) 3 2015/02/26 Modify PQ2 to PJA138K(BAM138K0001) & un-stuff PR51 (page 39) 4 2015/02/26 Modify PR159/PR160 from 0ohm to 100ohm (page 38) 5 2015/02/26 Add R693(reserve) & R694 for current leakage issue (page 18)	
		1 2015/03/2 Delete Wifi_SUSCLK schematic(U26、R544、C407、R546) & add TP75 for vendor requset (page 6、27、29)	
		1 2015/03/3 Add Board ID0 strap (R695、R696) (page 6) 2 2015/03/3 Add R697 & Change C1 to 180P/50V for ESD (page 21) 3 2015/03/03 Un-Stuff Q56 & Stuff R496 (page 26)	
		1 2015/03/04 Un-Stuff R528、R527、R540、R539 (page 7) 2 2015/03/04 Un-Stuff Q40、R291 (page 27) 3 2015/03/04 Change R687、R688 from 2.2K to 4.7K (page 7) 4 2015/03/04 Change D8 to RB500V-40 (BCRB500VZ29) (page 18)	
		1 2015/03/06 Change PU9 P/N from AL051225000 to AL051225003 for PDC request (page 32)	
		1 2015/03/06 Change L11、L12、L13、L14 to CX5AG121002 for PDC requset (page 25)	
	REV.E	1 2015/03/19 Modify R280 to close CN12 & add C600、R698、C601 for ESD (page 20) 2 2015/03/19 Add R699 & C602 for ESD (page 27) 3 2015/03/19 Modify R243 to close CN8 & add C603、R702、C607 for ESD (page 21) 4 2015/03/19 Add R700、R701、C604、C605、C606 for ESD (page 19) 5 2015/03/19 Delete R253 (page 18) 6 2015/03/19 Add SPAD1~SPAD10 for ESD (page 30) 7 2015/03/19 Add D29、D30 & Change D14、D17、D25 to BCPJSD05Z06 for ESD (page 25) 8 2015/03/19 Change D21~D24 to BCPJSD05Z06 for ESD (page 23) 9 2015/03/19 Change R161 connect from +3V to +3V_S5 for current leakage issue (page 23) 10 2015/03/19 Change some parts from 0 ohm to shortpad	
		1 2015/03/24 Delete L9 (page 20)	
		1 2015/04/2 Add & Reserve C608 for vendor suggest (page 26) 2 2015/04/2 Delete R681 (+1.8V_S5) (page 29)	
		1 2015/04/07 Delete SPAD1~SPAD10 (page 30) & Add TP76~TP95 for ESD (page 23 &24)	

Page	From	To
1		3A
2		3A
3		3A
4		3A
5		3A
6		3A
7		3A
8		3A
9		3A
10		3A
11		3A
12		3A
13		3A
14		3A
15		3A
16		3A
17		3A
18		3A
19		3A
20		3A
21		3A
22		3A
23		3A
24		3A
25		3A
26		3A
27		3A
28		3A
29		3A
30		3A
31		3A
32		3A
33		3A
34		3A
35		3A
36		3A
37		3A
38		3A
39		3A

Quanta Computer Inc.
PROJECT : ZYLB/ZYLC

Size	Document Number	Rev
	Change List-2	1A
Date: Friday, April 10, 2015	Sheet 42 of 42	