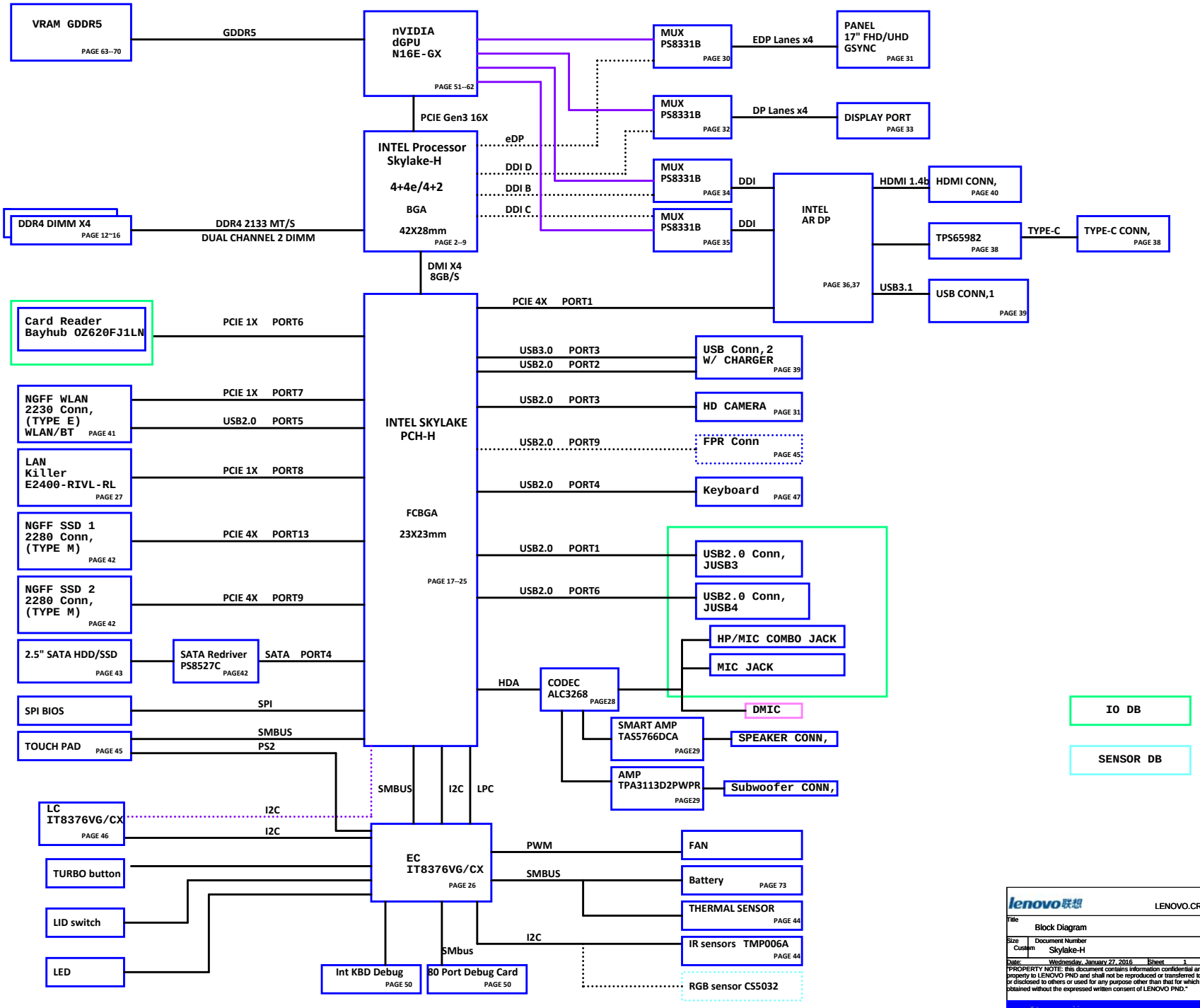
Schematic Block Diagram



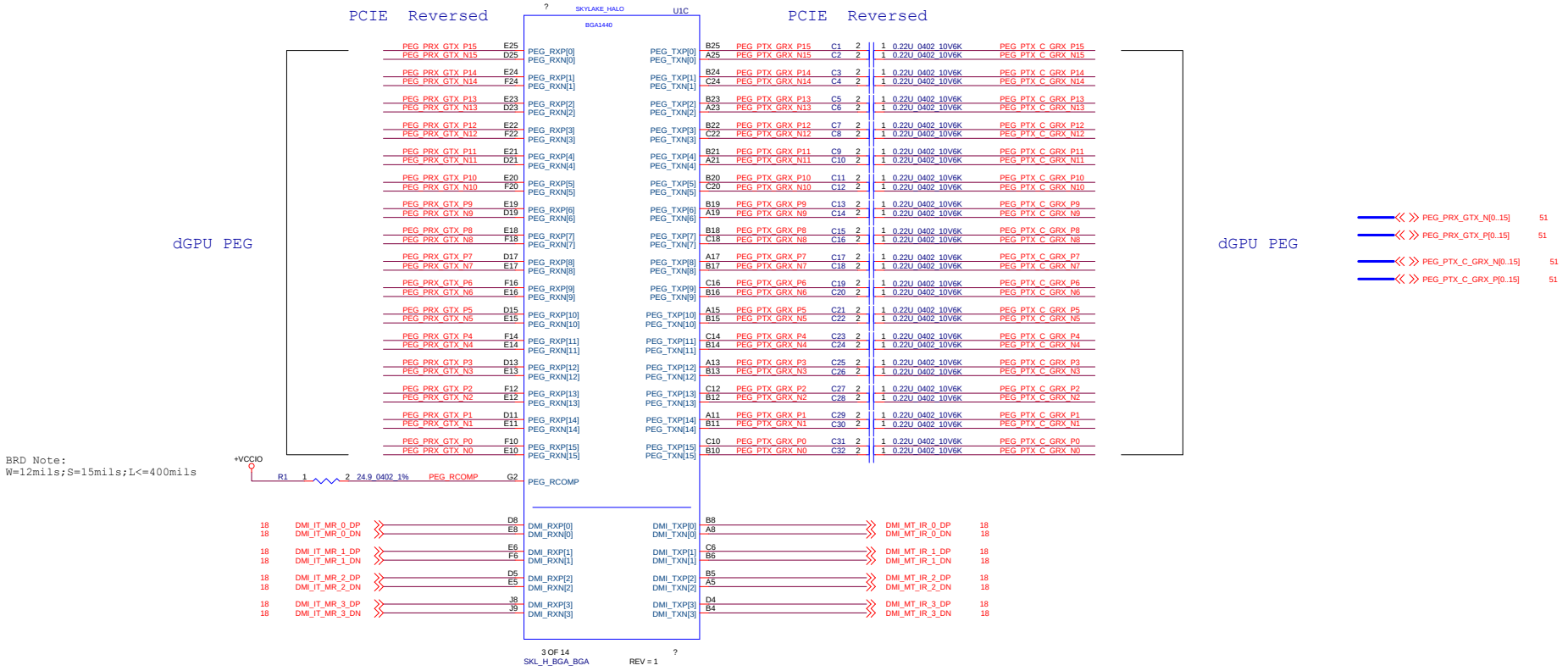
lenovo联想 LENOVO.CRDN

Title: Block Diagram

Size: Custom | Document Number: Skylake-H | Rev: V0.3

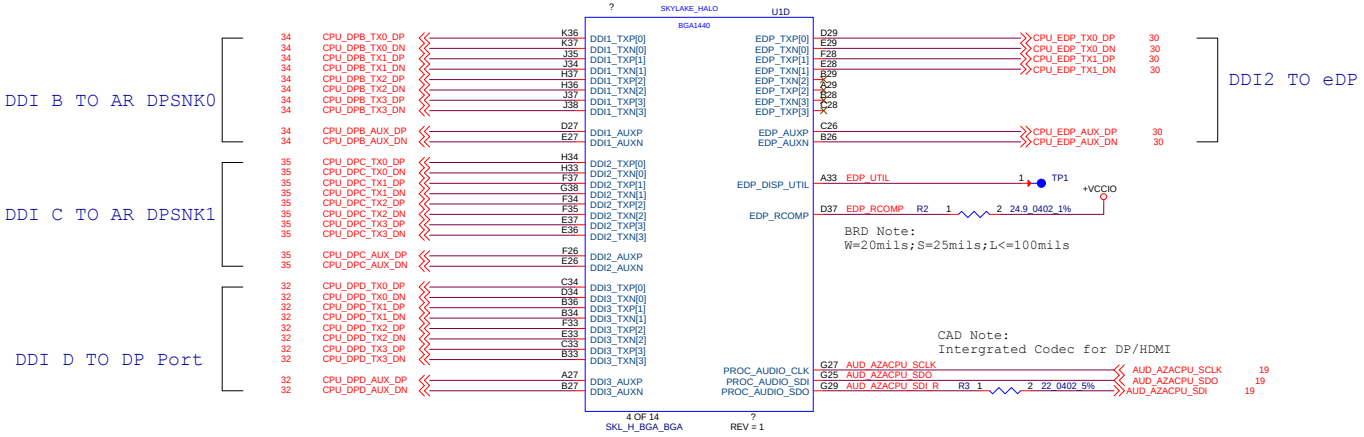
Date: Wednesday, January 27, 2016 | Sheet 1 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



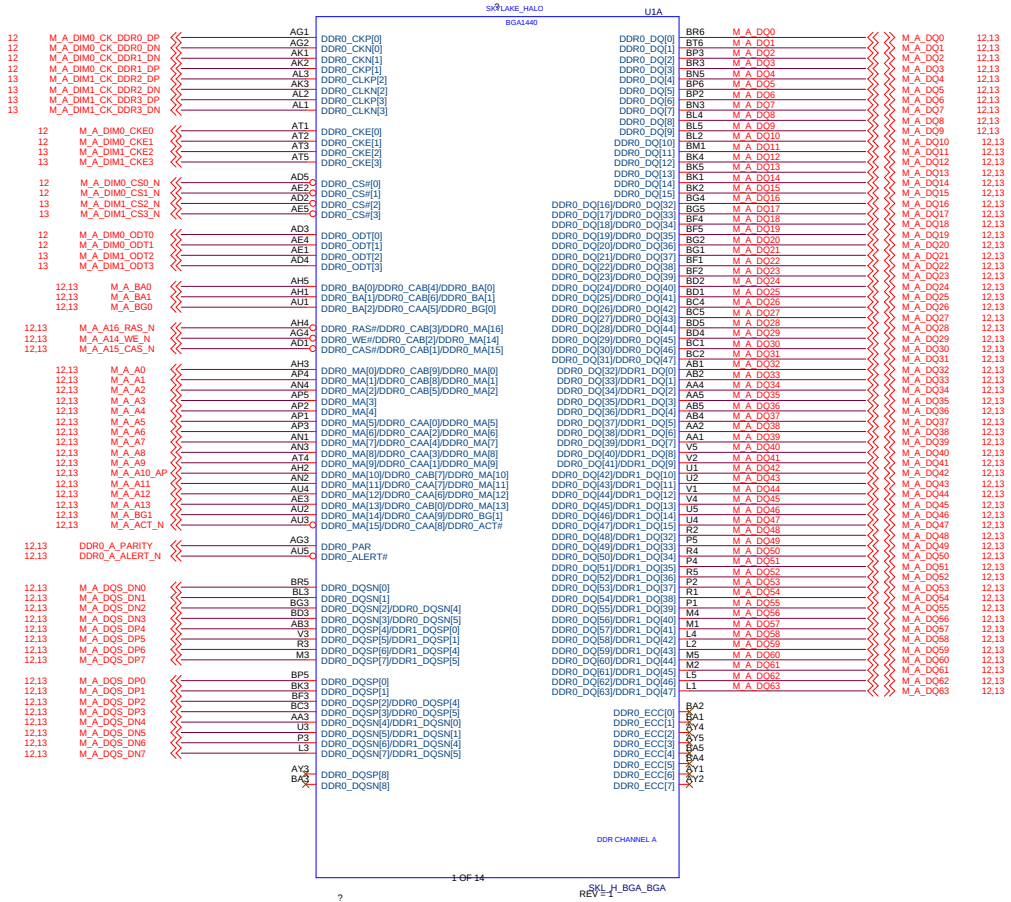
lenovo联想	LENOVO.CRDN		
Title: PROCESSOR-PEG/DMI			
Size: C	Document Number: Skylake-H		Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 2 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN		
Title: Processor--eDP/TBT/DP			
Size: C	Document Number: Skylake-H		Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 3 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



12	M_A_DIM0_CK_DDR0_DP	AG1	DDR0_CKP[0]	DDR0_DQ[0]	BR6	M_A_DQ0	M_A_DQ0 12,13
12	M_A_DIM0_CK_DDR0_DN	AG2	DDR0_CKN[0]	DDR0_DQ[1]	BT6	M_A_DQ1	M_A_DQ1 12,13
12	M_A_DIM0_CK_DDR1_DN	AK1	DDR0_CKN[1]	DDR0_DQ[2]	BP3	M_A_DQ2	M_A_DQ2 12,13
12	M_A_DIM0_CK_DDR1_DP	AK2	DDR0_CKP[1]	DDR0_DQ[3]	BR3	M_A_DQ3	M_A_DQ3 12,13
13	M_A_DIM1_CK_DDR2_DP	AL3	DDR0_CLKP[2]	DDR0_DQ[4]	BN5	M_A_DQ4	M_A_DQ4 12,13
13	M_A_DIM1_CK_DDR2_DN	AK3	DDR0_CLKN[2]	DDR0_DQ[5]	BP6	M_A_DQ5	M_A_DQ5 12,13
13	M_A_DIM1_CK_DDR3_DP	AL2	DDR0_CLKP[3]	DDR0_DQ[6]	BP2	M_A_DQ6	M_A_DQ6 12,13
13	M_A_DIM1_CK_DDR3_DN	AL1	DDR0_CLKN[3]	DDR0_DQ[7]	BN3	M_A_DQ7	M_A_DQ7 12,13
				DDR0_DQ[8]	BL4	M_A_DQ8	M_A_DQ8 12,13
				DDR0_DQ[9]	BL5	M_A_DQ9	M_A_DQ9 12,13
12	M_A_DIM0_CKE0	AT1	DDR0_CKE[0]	DDR0_DQ[10]	BL2	M_A_DQ10	M_A_DQ10 12,13
12	M_A_DIM0_CKE1	AT2	DDR0_CKE[1]	DDR0_DQ[11]	BM1	M_A_DQ11	M_A_DQ11 12,13
13	M_A_DIM1_CKE2	AT3	DDR0_CKE[2]	DDR0_DQ[12]	BK4	M_A_DQ12	M_A_DQ12 12,13
13	M_A_DIM1_CKE3	AT5	DDR0_CKE[3]	DDR0_DQ[13]	BK5	M_A_DQ13	M_A_DQ13 12,13
12	M_A_DIM0_CS0_N	AD5	DDR0_CS#[0]	DDR0_DQ[14]	BK1	M_A_DQ14	M_A_DQ14 12,13
12	M_A_DIM0_CS1_N	AE2	DDR0_CS#[1]	DDR0_DQ[15]	BK2	M_A_DQ15	M_A_DQ15 12,13
13	M_A_DIM1_CS2_N	AD2	DDR0_CS#[2]	DDR0_DQ[16]/DDR0_DQ[32]	BG4	M_A_DQ16	M_A_DQ16 12,13
13	M_A_DIM1_CS3_N	AE5	DDR0_CS#[3]	DDR0_DQ[17]/DDR0_DQ[33]	BG5	M_A_DQ17	M_A_DQ17 12,13
				DDR0_DQ[18]/DDR0_DQ[34]	BF4	M_A_DQ18	M_A_DQ18 12,13
12	M_A_DIM0_ODT0	AD3	DDR0_ODT[0]	DDR0_DQ[19]/DDR0_DQ[35]	BF5	M_A_DQ19	M_A_DQ19 12,13
12	M_A_DIM0_ODT1	AE4	DDR0_ODT[1]	DDR0_DQ[20]/DDR0_DQ[36]	BG2	M_A_DQ20	M_A_DQ20 12,13
13	M_A_DIM1_ODT2	AE1	DDR0_ODT[2]	DDR0_DQ[21]/DDR0_DQ[37]	BG1	M_A_DQ21	M_A_DQ21 12,13
13	M_A_DIM1_ODT3	AD4	DDR0_ODT[3]	DDR0_DQ[22]/DDR0_DQ[38]	BF1	M_A_DQ22	M_A_DQ22 12,13
				DDR0_DQ[23]/DDR0_DQ[39]	BF2	M_A_DQ23	M_A_DQ23 12,13
12,13	M_A_BA0	AH5	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	DDR0_DQ[24]/DDR0_DQ[40]	BD2	M_A_DQ24	M_A_DQ24 12,13
12,13	M_A_BA1	AH1	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	DDR0_DQ[25]/DDR0_DQ[41]	BD1	M_A_DQ25	M_A_DQ25 12,13
12,13	M_A_BG0	AU1	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	DDR0_DQ[26]/DDR0_DQ[42]	BC4	M_A_DQ26	M_A_DQ26 12,13
				DDR0_DQ[27]/DDR0_DQ[43]	BC5	M_A_DQ27	M_A_DQ27 12,13
12,13	M_A_A16_RAS_N	AH4	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	DDR0_DQ[28]/DDR0_DQ[44]	BD5	M_A_DQ28	M_A_DQ28 12,13
12,13	M_A_A14_WE_N	AG4	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	DDR0_DQ[29]/DDR0_DQ[45]	BD4	M_A_DQ29	M_A_DQ29 12,13
12,13	M_A_A15_CAS_N	AD1	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	DDR0_DQ[30]/DDR0_DQ[46]	BC1	M_A_DQ30	M_A_DQ30 12,13
				DDR0_DQ[31]/DDR0_DQ[47]	BC2	M_A_DQ31	M_A_DQ31 12,13
12,13	M_A_A0	AH3	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	DDR0_DQ[32]/DDR1_DQ[0]	AB1	M_A_DQ32	M_A_DQ32 12,13
12,13	M_A_A1	AP4	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	DDR0_DQ[33]/DDR1_DQ[1]	AB2	M_A_DQ33	M_A_DQ33 12,13
12,13	M_A_A2	AN4	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	DDR0_DQ[34]/DDR1_DQ[2]	AA4	M_A_DQ34	M_A_DQ34 12,13
12,13	M_A_A3	AP5	DDR0_MA[3]	DDR0_DQ[35]/DDR1_DQ[3]	AA5	M_A_DQ35	M_A_DQ35 12,13
12,13	M_A_A4	AP2	DDR0_MA[4]	DDR0_DQ[36]/DDR1_DQ[4]	AB5	M_A_DQ36	M_A_DQ36 12,13
12,13	M_A_A5	AP1	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	DDR0_DQ[37]/DDR1_DQ[5]	AB4	M_A_DQ37	M_A_DQ37 12,13
12,13	M_A_A6	AP3	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	DDR0_DQ[38]/DDR1_DQ[6]	AA2	M_A_DQ38	M_A_DQ38 12,13
12,13	M_A_A7	AN1	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	DDR0_DQ[39]/DDR1_DQ[7]	AA1	M_A_DQ39	M_A_DQ39 12,13
12,13	M_A_A8	AN3	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	DDR0_DQ[40]/DDR1_DQ[8]	V5	M_A_DQ40	M_A_DQ40 12,13
12,13	M_A_A9	AT4	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	DDR0_DQ[41]/DDR1_DQ[9]	V2	M_A_DQ41	M_A_DQ41 12,13
12,13	M_A_A10_AP	AH2	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	DDR0_DQ[42]/DDR1_DQ[10]	U1	M_A_DQ42	M_A_DQ42 12,13
12,13	M_A_A11	AN2	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	DDR0_DQ[43]/DDR1_DQ[11]	U2	M_A_DQ43	M_A_DQ43 12,13
12,13	M_A_A12	AU4	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	DDR0_DQ[44]/DDR1_DQ[12]	V1	M_A_DQ44	M_A_DQ44 12,13
12,13	M_A_A13	AE3	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	DDR0_DQ[45]/DDR1_DQ[13]	V4	M_A_DQ45	M_A_DQ45 12,13
12,13	M_A_BG1	AU2	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	DDR0_DQ[46]/DDR1_DQ[14]	U5	M_A_DQ46	M_A_DQ46 12,13
12,13	M_A_ACT_N	AU3	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	DDR0_DQ[47]/DDR1_DQ[15]	U4	M_A_DQ47	M_A_DQ47 12,13
				DDR0_DQ[48]/DDR1_DQ[32]	R2	M_A_DQ48	M_A_DQ48 12,13
12,13	DDR0_A_PARITY	AG3	DDR0_PAR	DDR0_DQ[49]/DDR1_DQ[33]	P5	M_A_DQ49	M_A_DQ49 12,13
12,13	DDR0_A_ALERT_N	AU5	DDR0_ALERT#	DDR0_DQ[50]/DDR1_DQ[34]	R4	M_A_DQ50	M_A_DQ50 12,13
				DDR0_DQ[51]/DDR1_DQ[35]	P4	M_A_DQ51	M_A_DQ51 12,13
12,13	M_A_DQS_DN0	BR5	DDR0_DQSN[0]	DDR0_DQ[52]/DDR1_DQ[36]	R5	M_A_DQ52	M_A_DQ52 12,13
12,13	M_A_DQS_DN1	BL3	DDR0_DQSN[1]	DDR0_DQ[53]/DDR1_DQ[37]	P2	M_A_DQ53	M_A_DQ53 12,13
12,13	M_A_DQS_DN2	BG3	DDR0_DQSN[2]/DDR0_DQSN[4]	DDR0_DQ[54]/DDR1_DQ[38]	R1	M_A_DQ54	M_A_DQ54 12,13
12,13	M_A_DQS_DN3	BD3	DDR0_DQSN[3]/DDR0_DQSN[5]	DDR0_DQ[55]/DDR1_DQ[39]	P1	M_A_DQ55	M_A_DQ55 12,13
12,13	M_A_DQS_DP4	AB3	DDR0_DQSP[4]/DDR1_DQSP[0]	DDR0_DQ[56]/DDR1_DQ[40]	M4	M_A_DQ56	M_A_DQ56 12,13
12,13	M_A_DQS_DP5	V3	DDR0_DQSP[5]/DDR1_DQSP[1]	DDR0_DQ[57]/DDR1_DQ[41]	M1	M_A_DQ57	M_A_DQ57 12,13
12,13	M_A_DQS_DP6	R3	DDR0_DQSP[6]/DDR1_DQSP[4]	DDR0_DQ[58]/DDR1_DQ[42]	L4	M_A_DQ58	M_A_DQ58 12,13
12,13	M_A_DQS_DP7	M3	DDR0_DQSP[7]/DDR1_DQSP[5]	DDR0_DQ[59]/DDR1_DQ[43]	L2	M_A_DQ59	M_A_DQ59 12,13
				DDR0_DQ[60]/DDR1_DQ[44]	M5	M_A_DQ60	M_A_DQ60 12,13
12,13	M_A_DQS_DP0	BP5	DDR0_DQSP[0]	DDR0_DQ[61]/DDR1_DQ[45]	M2	M_A_DQ61	M_A_DQ61 12,13
12,13	M_A_DQS_DP1	BK3	DDR0_DQSP[1]	DDR0_DQ[62]/DDR1_DQ[46]	L5	M_A_DQ62	M_A_DQ62 12,13
12,13	M_A_DQS_DP2	BF3	DDR0_DQSP[2]/DDR0_DQSP[4]	DDR0_DQ[63]/DDR1_DQ[47]	L1	M_A_DQ63	M_A_DQ63 12,13
12,13	M_A_DQS_DP3	BC3	DDR0_DQSP[3]/DDR0_DQSP[5]				
12,13	M_A_DQS_DN4	AA3	DDR0_DQSN[4]/DDR1_DQSN[0]	DDR0_ECC[0]	BA2		
12,13	M_A_DQS_DN5	U3	DDR0_DQSN[5]/DDR1_DQSN[1]	DDR0_ECC[1]	BA1		
12,13	M_A_DQS_DN6	P3	DDR0_DQSN[6]/DDR1_DQSN[4]	DDR0_ECC[2]	AY4		
12,13	M_A_DQS_DN7	L3	DDR0_DQSN[7]/DDR1_DQSN[5]	DDR0_ECC[3]	AY5		
				DDR0_ECC[4]	BA5		
		AY3	DDR0_DQSP[8]	DDR0_ECC[5]	BA4		
		BA3	DDR0_DQSN[8]	DDR0_ECC[6]	AY1		
				DDR0_ECC[7]	AY2		

?

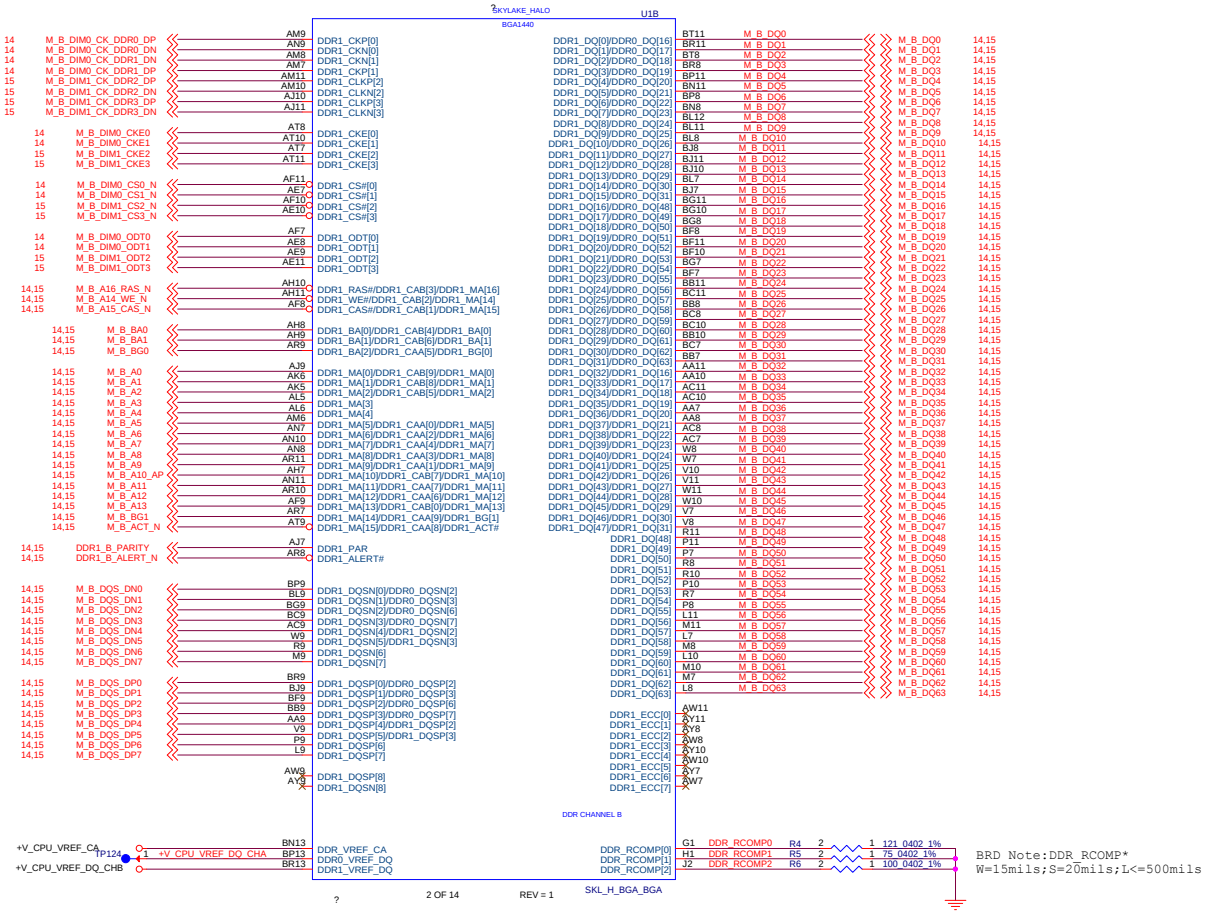
lenovo联想 LENOVO.CRDN

Title: PROCESSOR-MEM_CH A

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 4 of 99

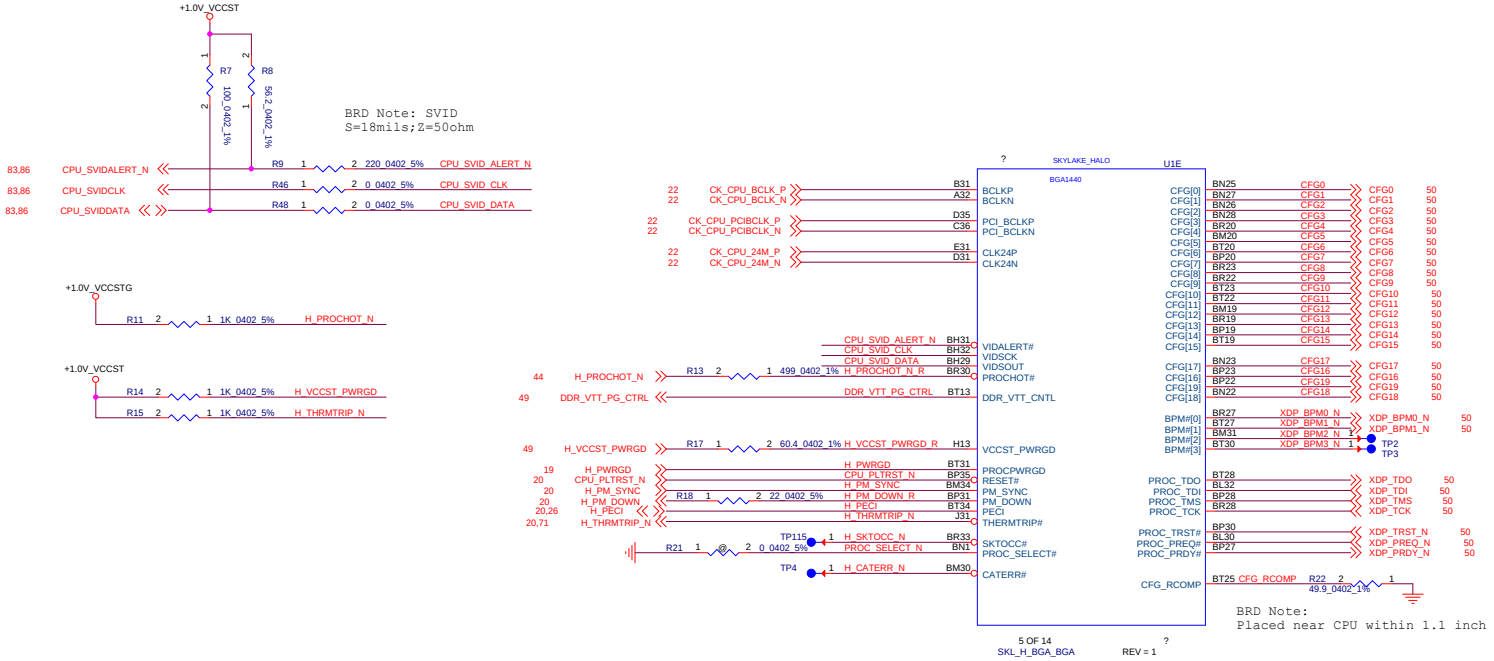
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

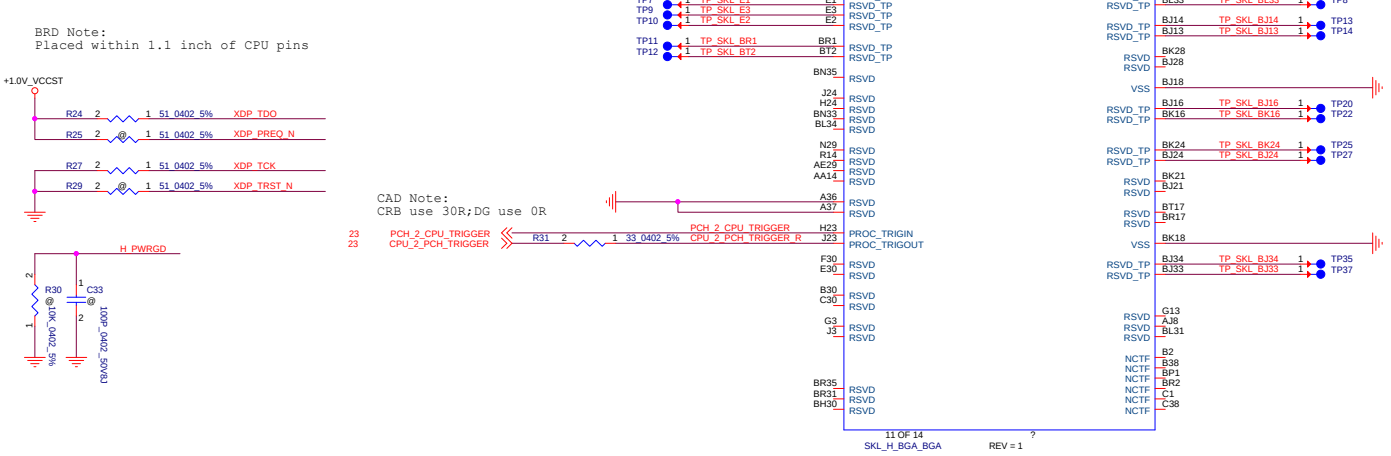


Title	PROCESSOR-MEM_CH B
Size	C
Document Number	Skylake-H
Rev	V0.3
Date:	Wednesday, January 27, 2016
Sheet	5 of 99

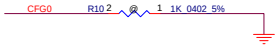
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

LENOVO.CRDN



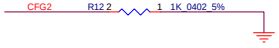


PROCESSOR CFG STRAPS



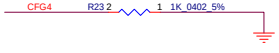
Stall reset sequence after PCU PLL lock until de-asserted

CFG0	1:Normal(Default) *
	0:Stall



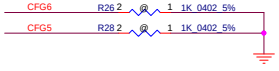
PEG16x Static Lane Reversal Strap

CFG2	1:Normal
	0:Reversed(Default) *



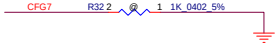
Embedded Display Port Presence Strap

CFG4	1:Disable
	0:Enable(Default) *



PEG CONFIG Straps

CFG[6:5]	11: x16 (Default)) *
	10: x8, x8
	01: Reserved
	00: x8,x4,x4



PEG TRAINNING

CFG7	1: follow RESET# deassertion *
	0: Wait for BIOS for training

lenovo联想 LENOVO.CRDN

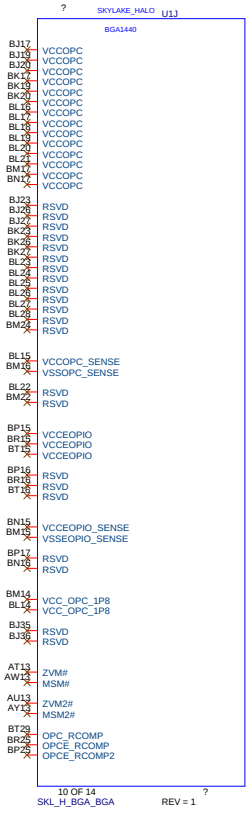
Title: PROCESSOR-CLK/PM/STRAP/TP

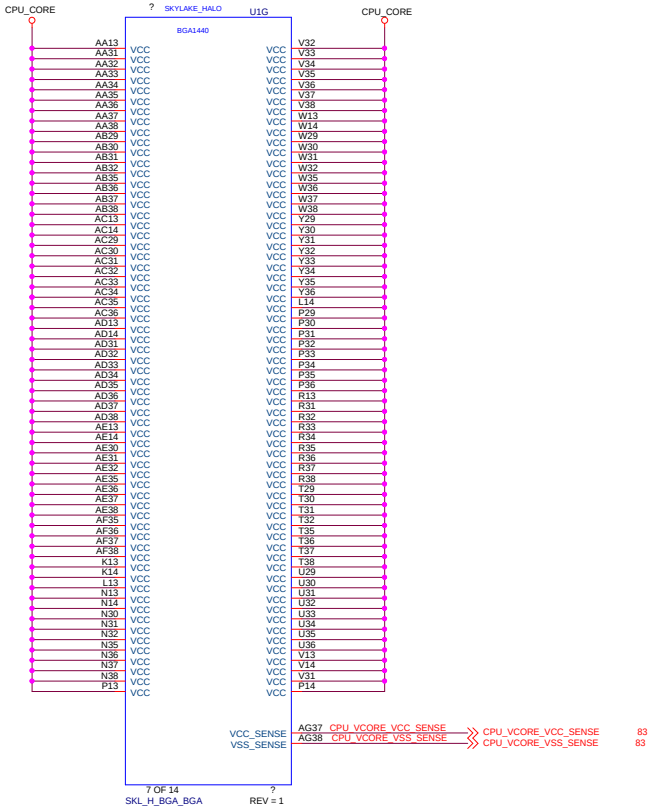
Size: C | Document Number: Skylake-H | Rev V0.3

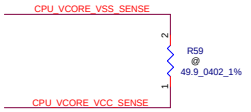
Date: Wednesday, January 27, 2016 | Sheet 6 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

FOR H4+4e







lenovo联想 LENOVO.CRDN

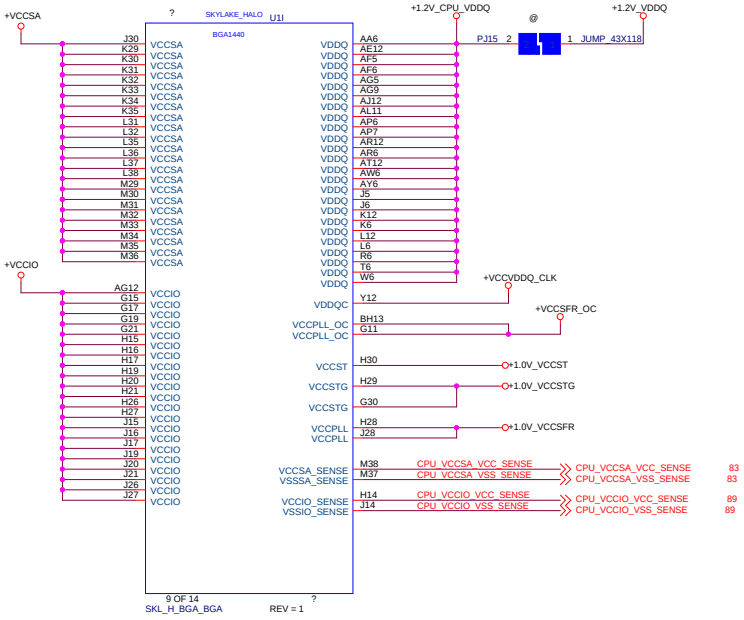
Title: PROCESSOR-POWER

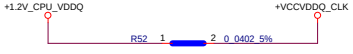
Size	Document Number	Rev
C	Skylake-H	V0.3

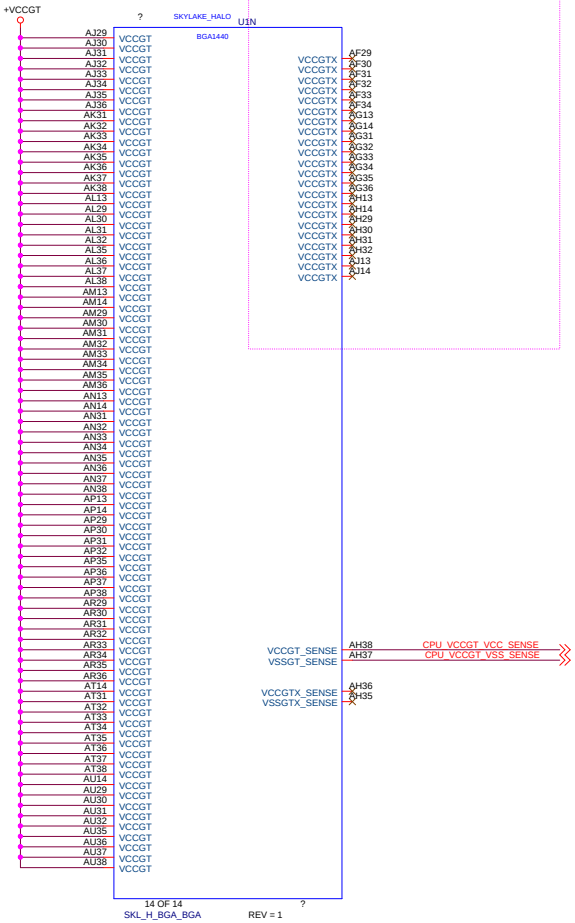
Date: Wednesday, January 27, 2016 Sheet 7 of 99

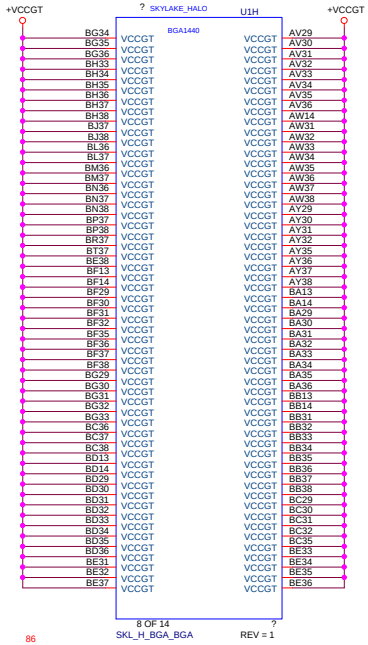
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

FOR H4+4e



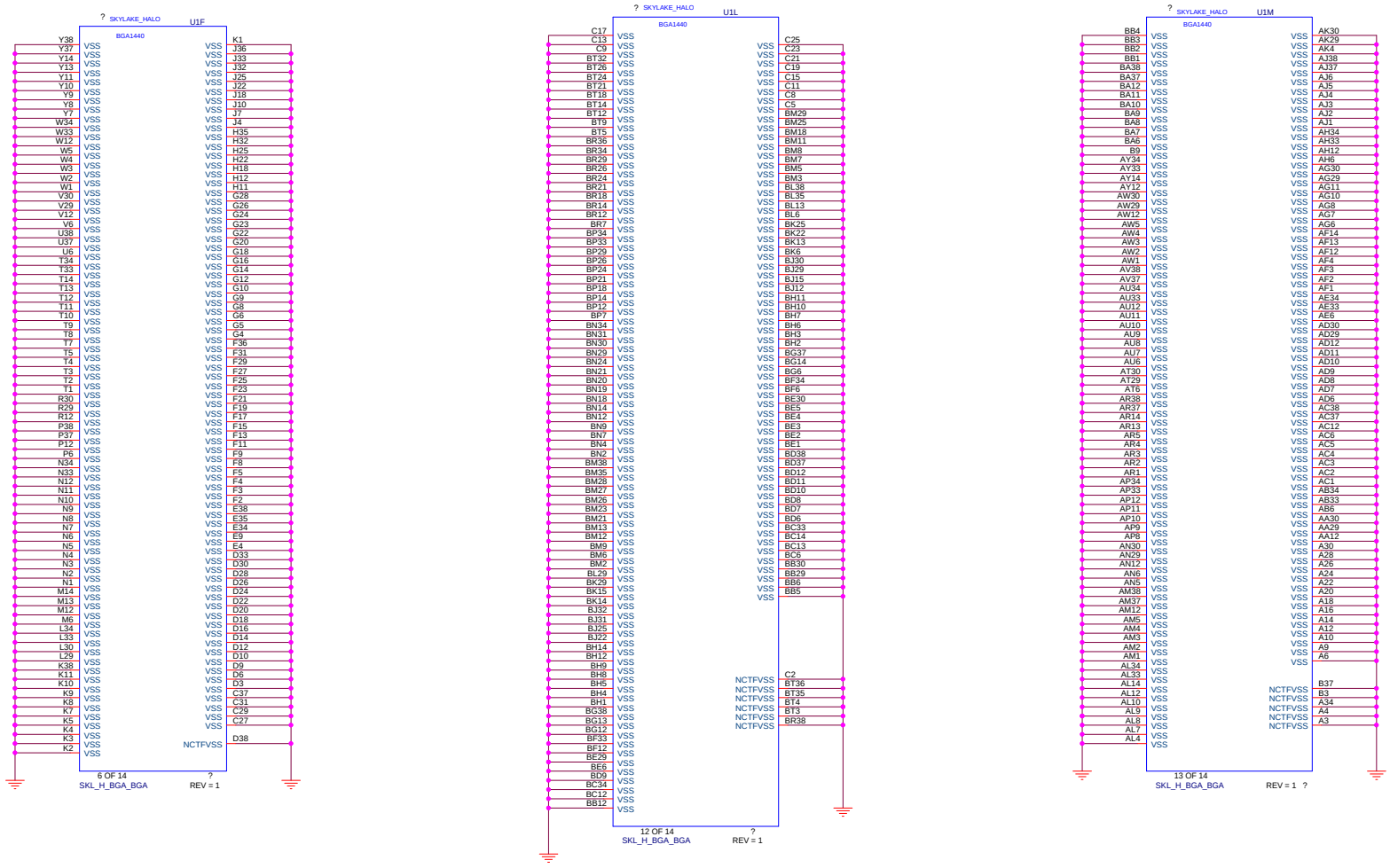






lenovo联想	LENOVO.CRDN
Title	PROCESSOR-POWER
Size C	Document Number Skylake-H
Rev	V0.3
Date:	Wednesday, January 27, 2016 Sheet 8 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

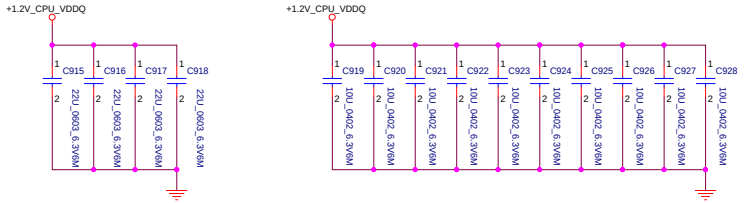


lenovo联想	LENOVO.CRDN
Title	PROCESSOR-VSS
Size C	Document Number: Skylake-H
Rev	V0.3
Date:	Wednesday, January 27, 2016 Sheet 9 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

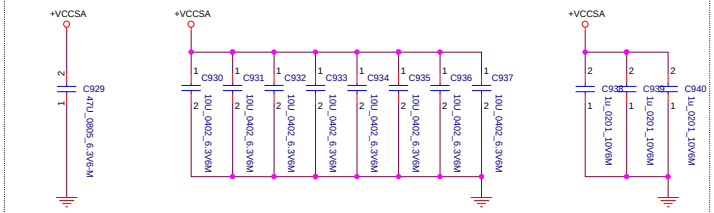
+1.2V_CPU_VDDQ 4X0603(22UF) 10X0402(10UF)

BRD Note:
Placed backside

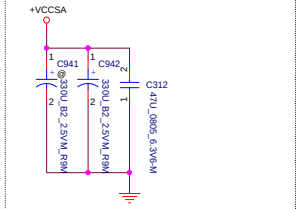


+VCCSA
BOTTOM:1X0805(47UF), 8X0402(10UF), 3X0201(1UF);
TOP:2XBULK(220UF),1X0805(22UF)

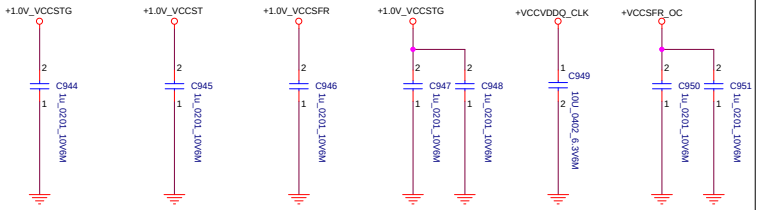
BRD Note:
Placed backside



BRD Note:
Placed TOP BGA EDGE



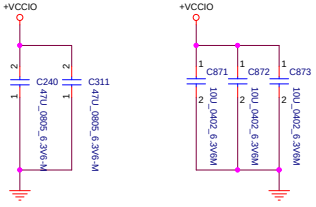
BRD Note:
Placed backside



+VCCIO 2x0805(47UF) 3X0402(10UF)

BRD Note:
Placed TOP BGA EDGE

BRD Note:
Placed backside



lenovo联想 LENOVO.CRDN

Title: PROCESSOR Decoupling 1/2

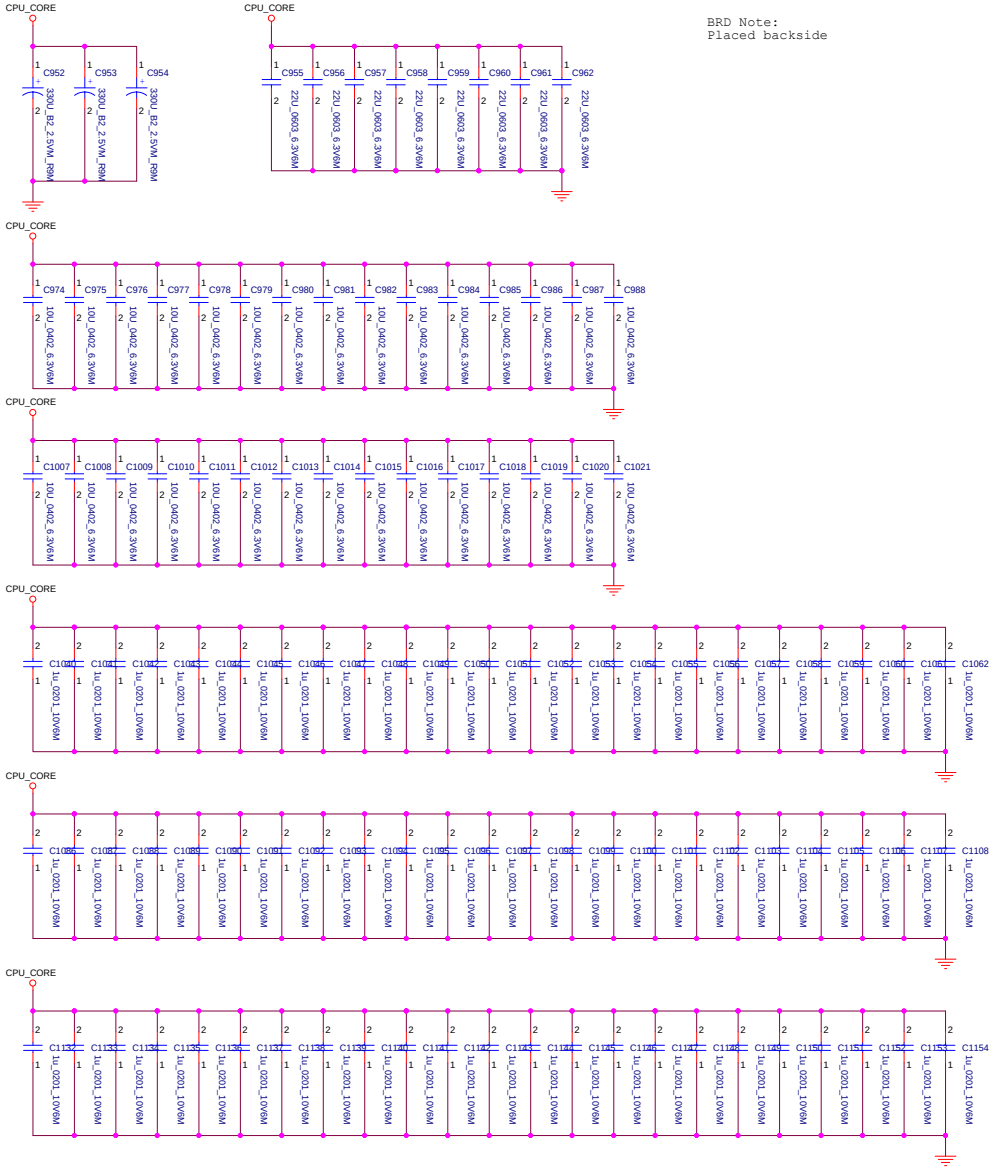
Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 10 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

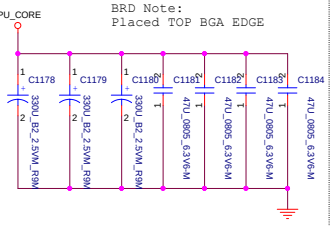
CPU_CORE
BOTTOM:3XBULK(220UF),8x0603(22U),30X0402(10UF), 69X0201(1UF);
TOP:3XBULK(220UF),4X0805(47UF)

BRD Note:
Placed backside



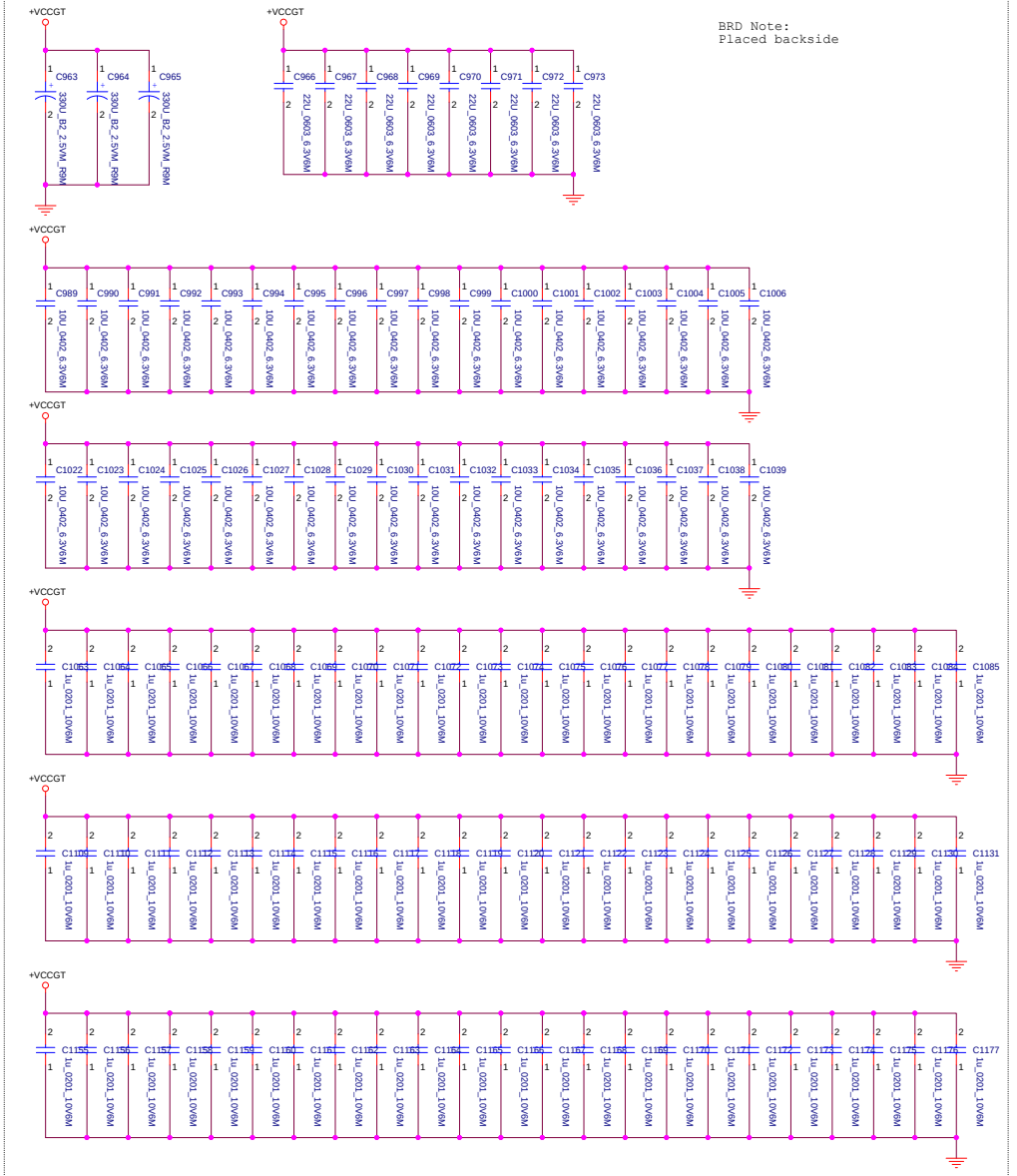
CPU_CORE

BRD Note:
Placed TOP BGA EDGE



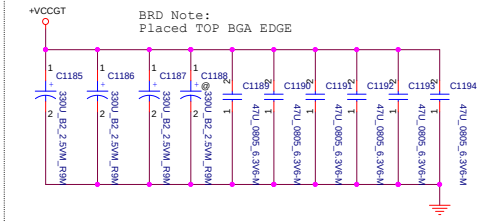
+VCCGT
BOTTOM:4XBULK(220UF),8X0603(22U),36X0402(10UF), 69X0201(1UF);
TOP:4XBULK(220UF),6X0805(47UF)

BRD Note:
Placed backside



+VCCGT

BRD Note:
Placed TOP BGA EDGE



lenovo联想 LENOVO.CRDN

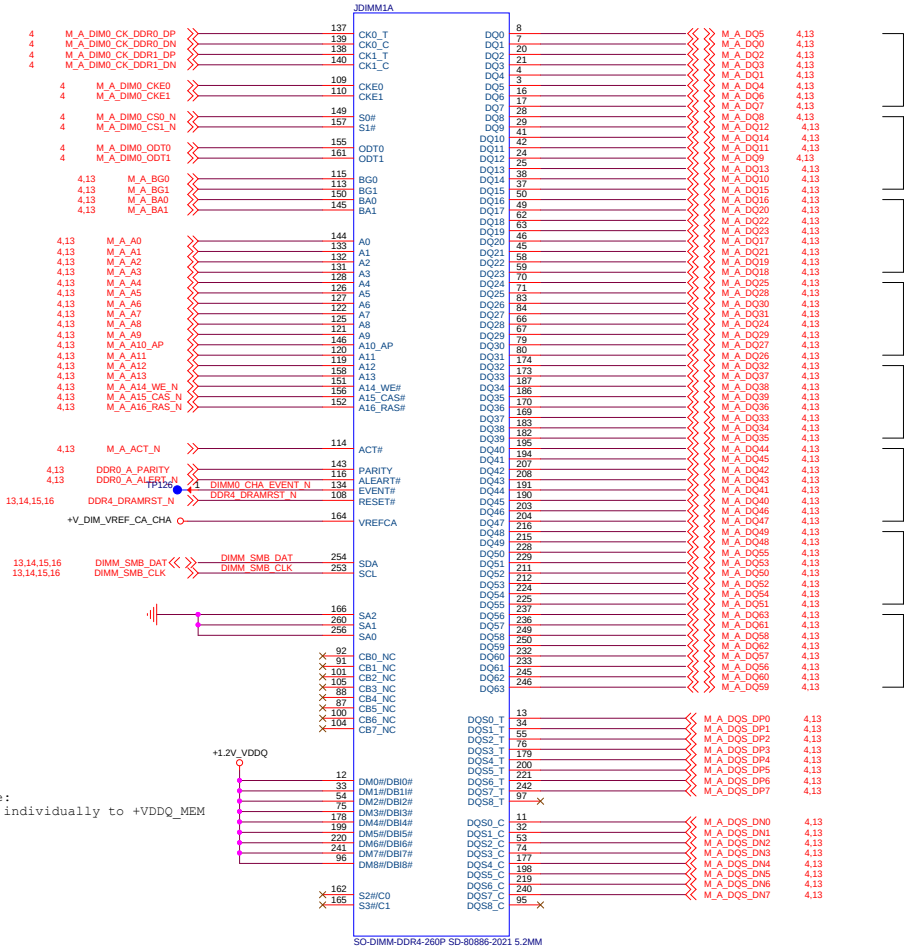
Title: PROCESSOR Decoupling 2/2

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 11 of 99

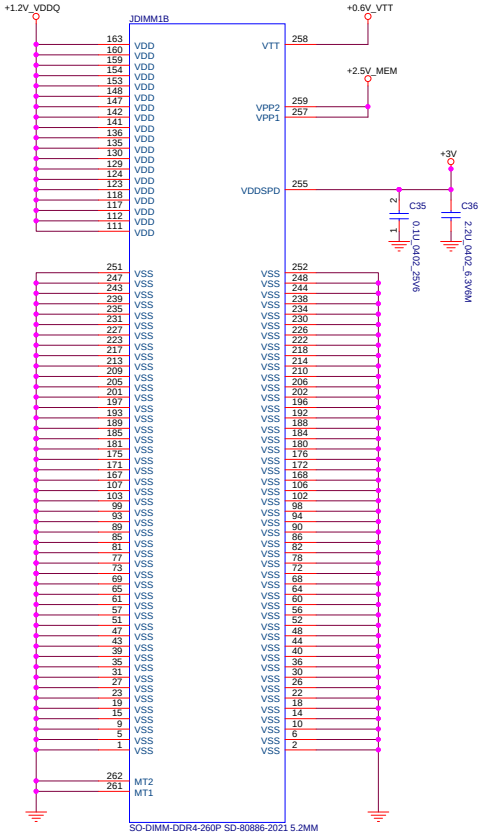
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

DDR4 SODIMM CHANNEL - A BOTTOM REV DIMM0 (5.2 MM HEIGHT CONNECTOR)



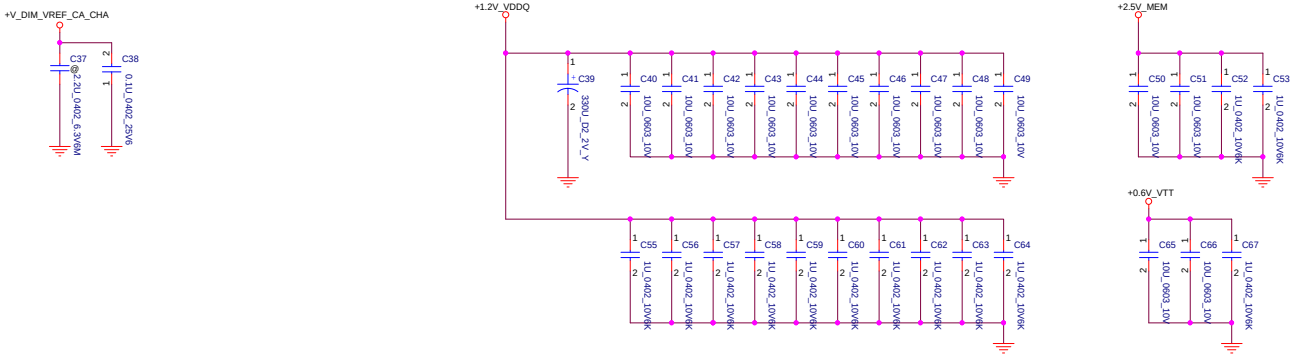
SPD ADDRESS:0xA0

BRD Note:
Connect individually to +VDDQ_MEM



Decoupling Caps

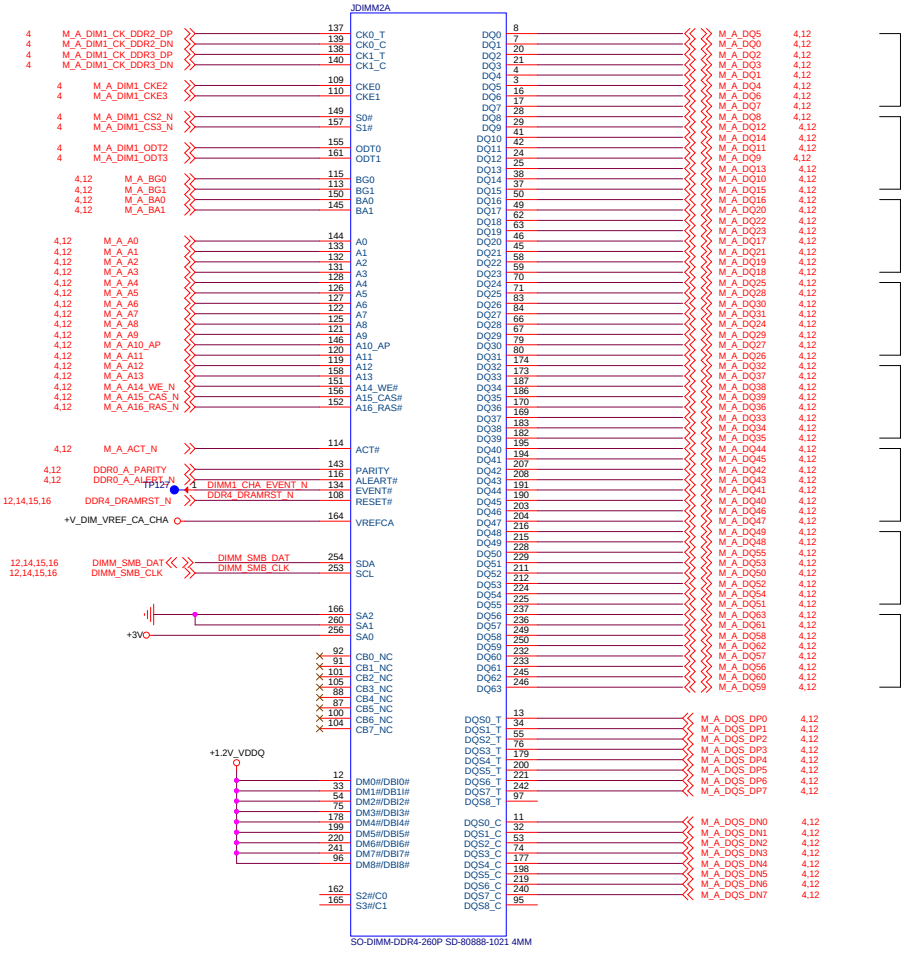
BRD Note:
placed close to CHA DIMM0



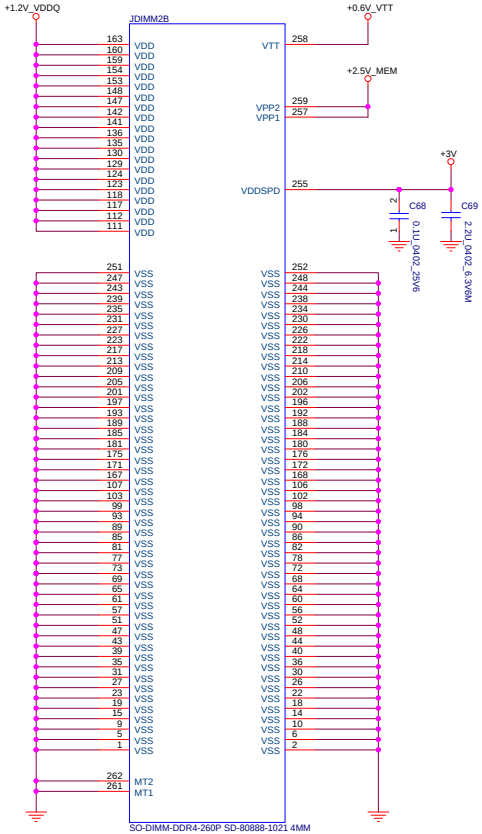
lenovo联想	LENOVO.CRDN	
Title: DDR4 CHA DIMM0		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 12 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

DDR4 SODIMM CHANNEL - A TOP STD DIMM1 (4 MM HEIGHT CONNECTOR)

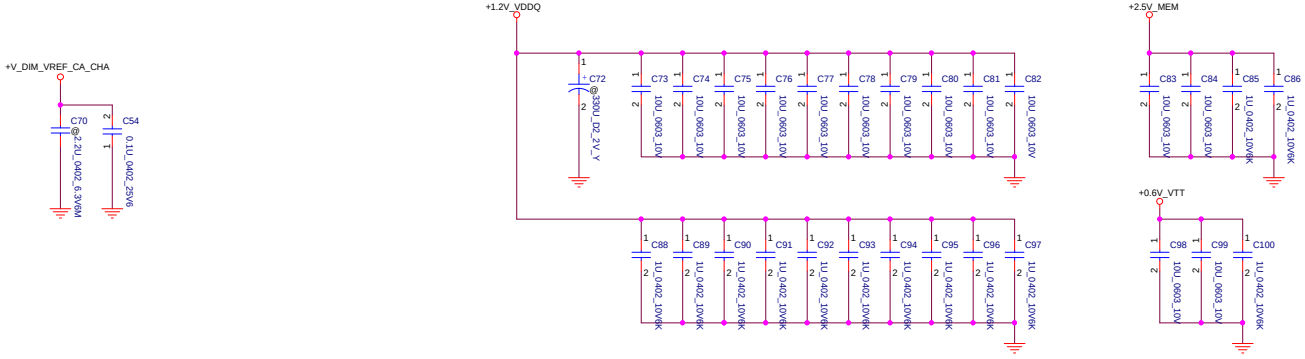


SPD ADDRESS:0xA2



Decoupling Caps

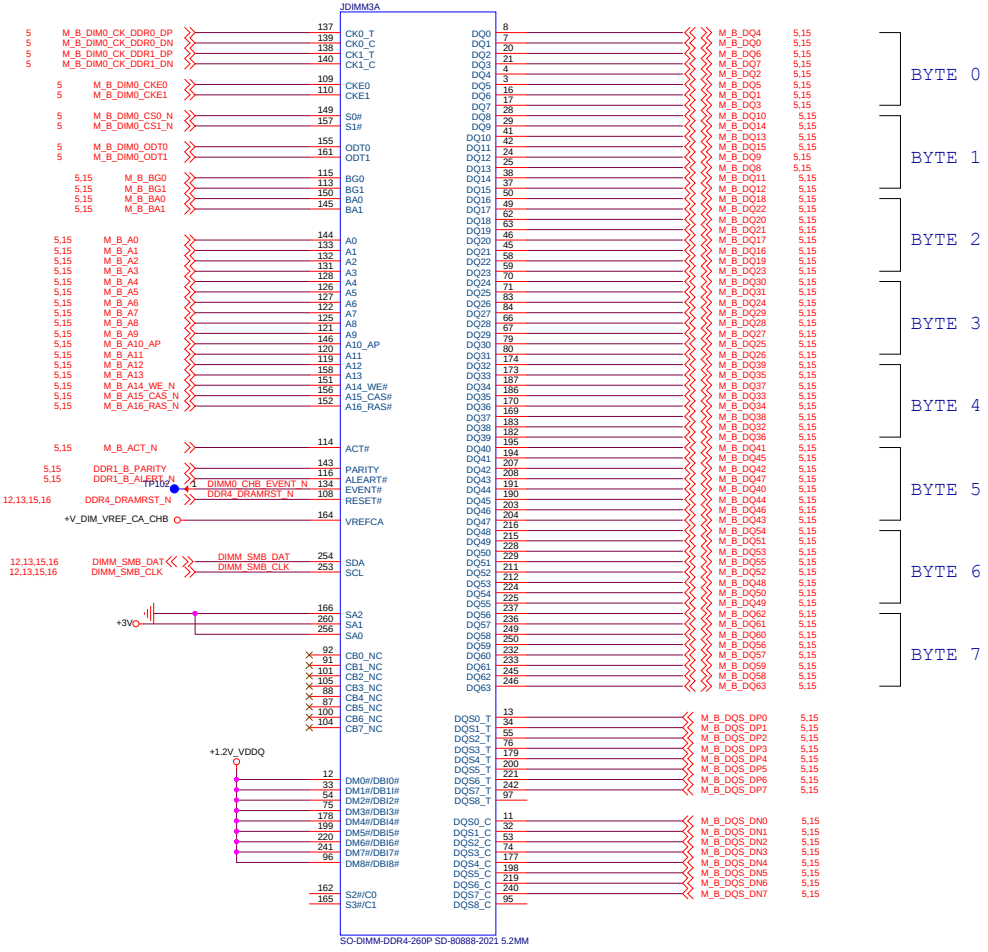
BRD Note:
placed close to CHA DIMM0



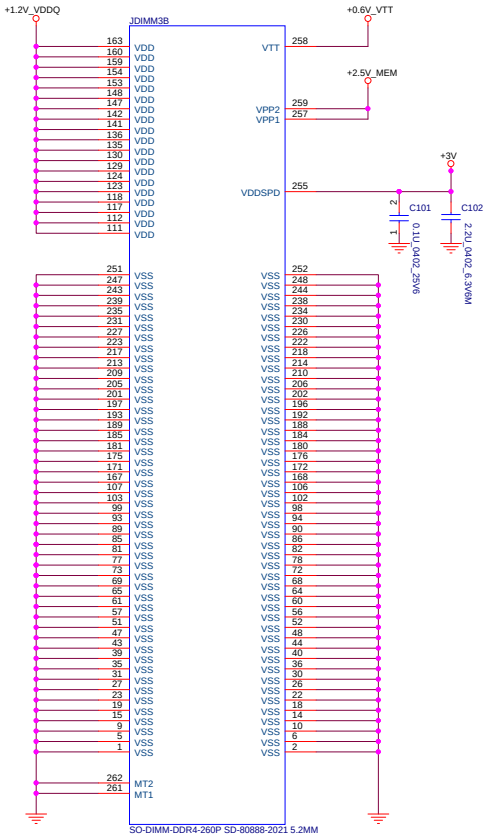
lenovo联想	LENOVO.CRDN
Title	DDR4 CHA DIMM1
Size C	Document Number Skylake-H
Rev	V0.3
Date: Wednesday, January 27, 2016	Sheet 13 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

DDR4 SODIMM CHANNEL - B BOTTOM STD DIMM0 (5.2 MM HEIGHT CONNECTOR)

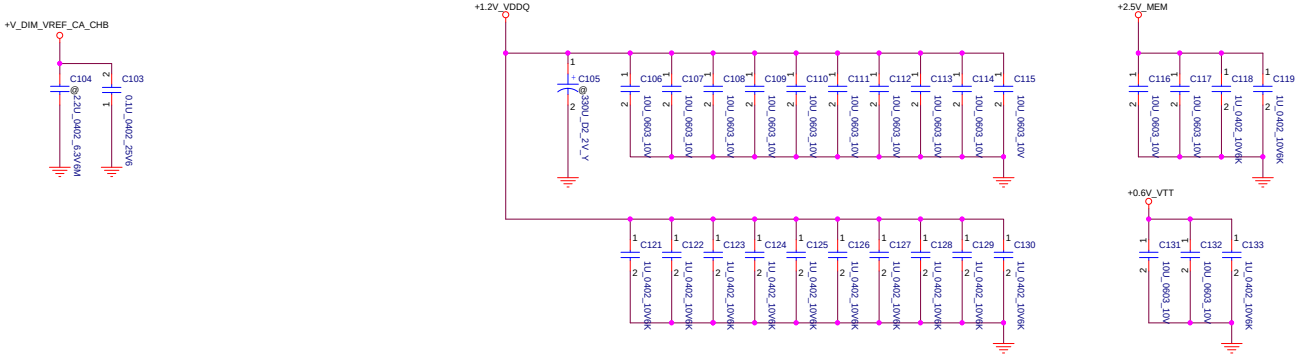


SPD ADDRESS:0xA4



Decoupling Caps

BRD Note:
placed close to CHA DIMM0



lenovo联想 LENOVO.CRDN

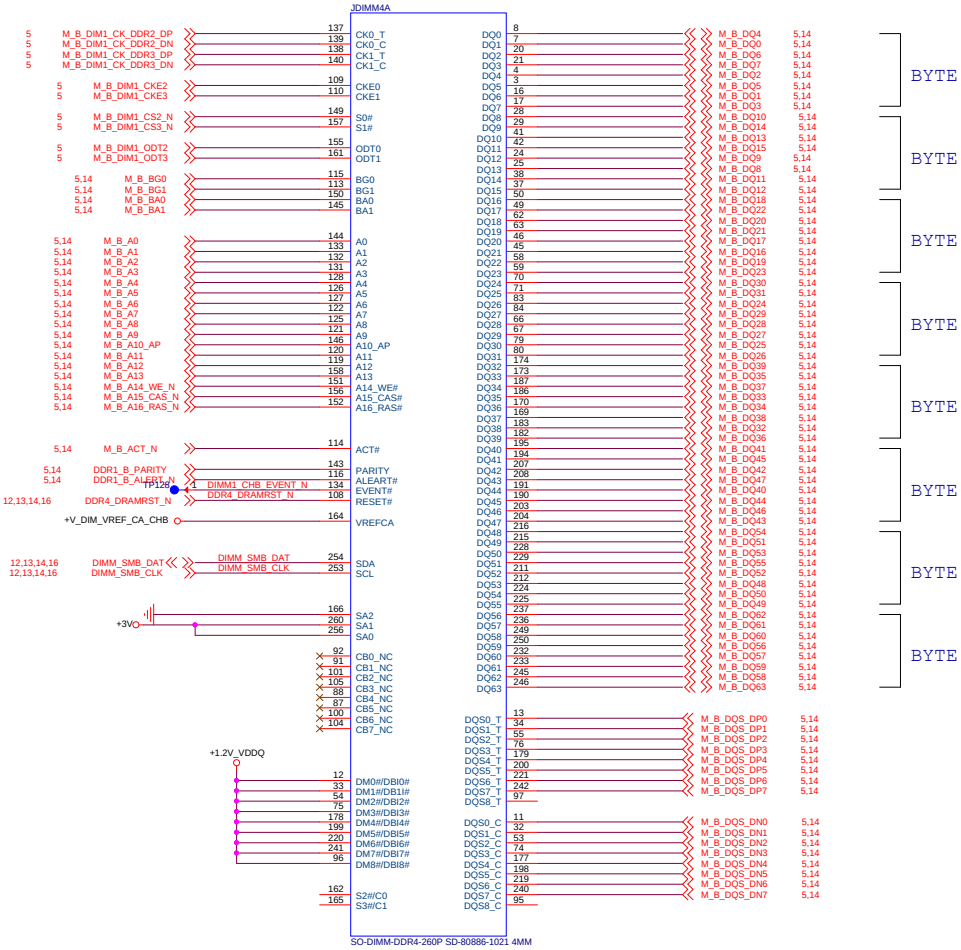
Title: DDR4 CHB DIMM0

Size	Document Number	Rev
C	Skylake-H	V0.3

Date: Wednesday, January 27, 2016 Sheet 14 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

DDR4 SODIMM CHANNEL - B TOP REV DIMM1 (4.0 MM HEIGHT CONNECTOR)



BYTE 0

BYTE 1

BYTE 2

BYTE 3

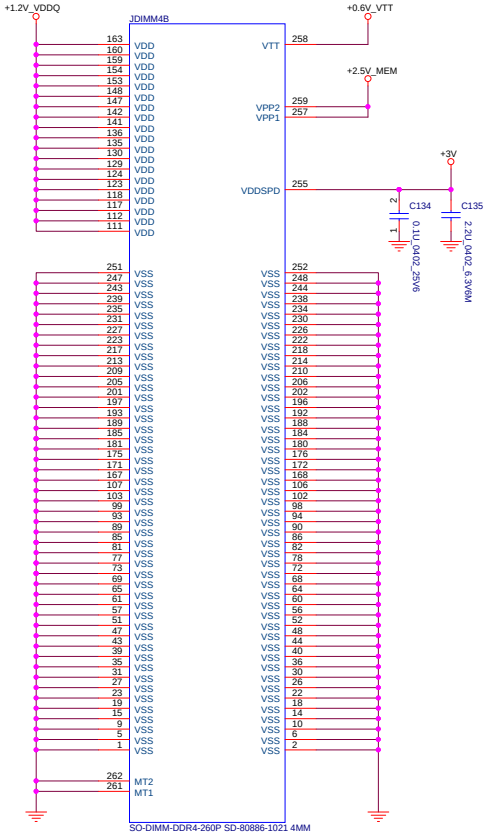
BYTE 4

BYTE 5

BYTE 6

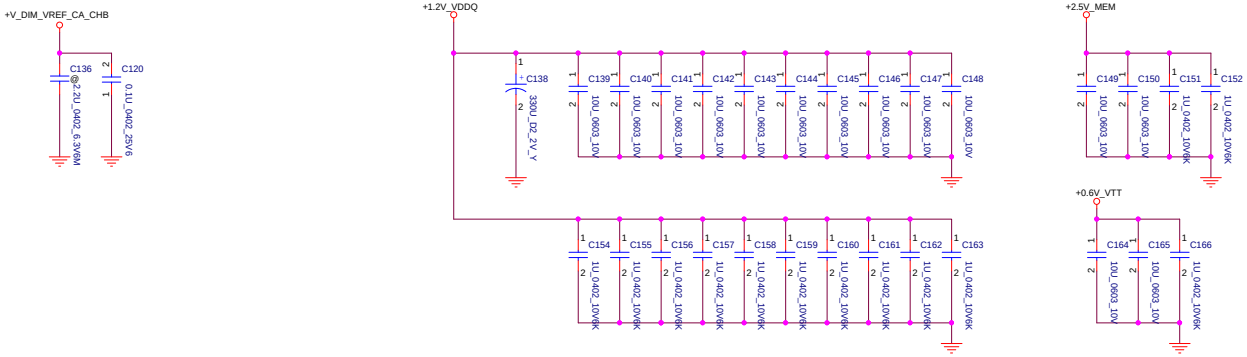
BYTE 7

SPD ADDRESS:0xA6



Decoupling Caps

BRD Note:
placed close to CHA DIMM0



lenovo联想 LENOVO.CRDN

Title: DDR4 CHB DIMM1

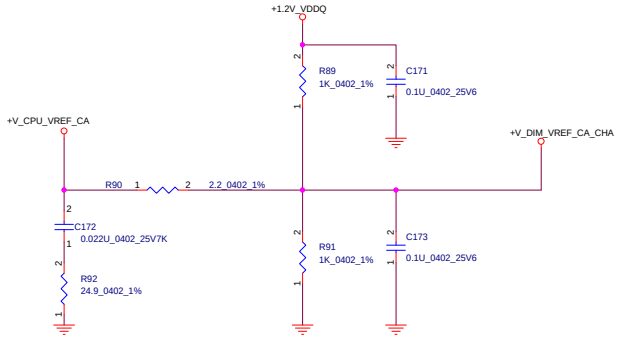
Size	Document Number	Rev
C	Skylake-H	V0.3

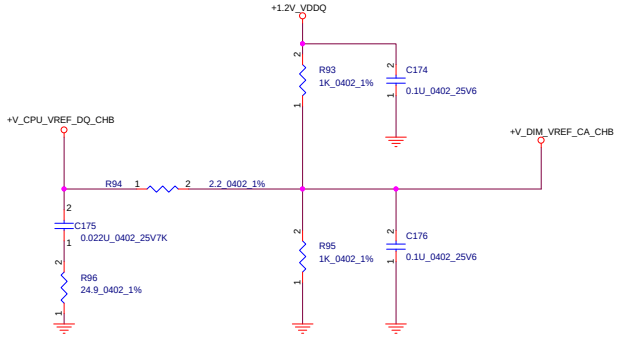
Date: Wednesday, January 27, 2016 Sheet 15 of 99

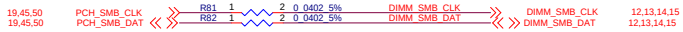
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

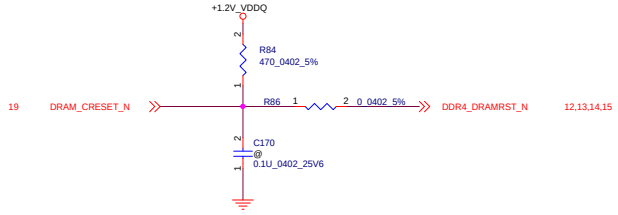
DDR VREF

BRD Note:
VREF trace width 20mils;spacing 20 mils to other signal/planes



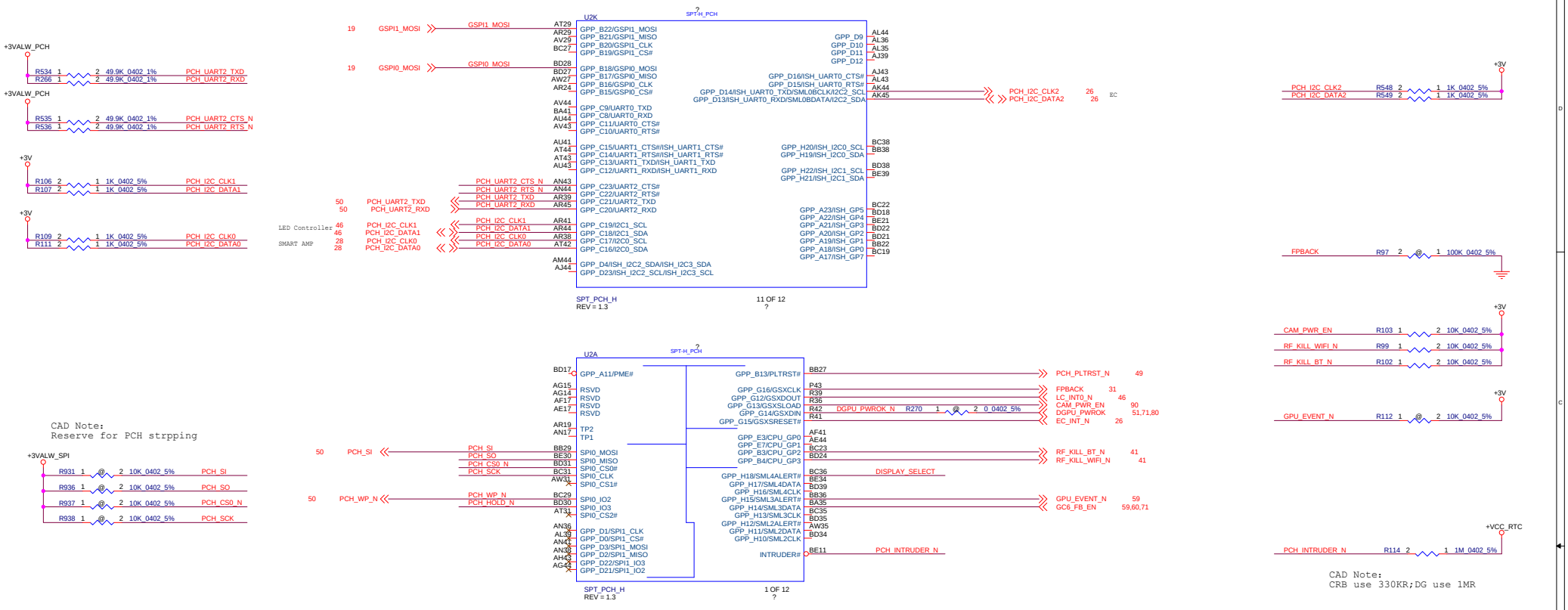




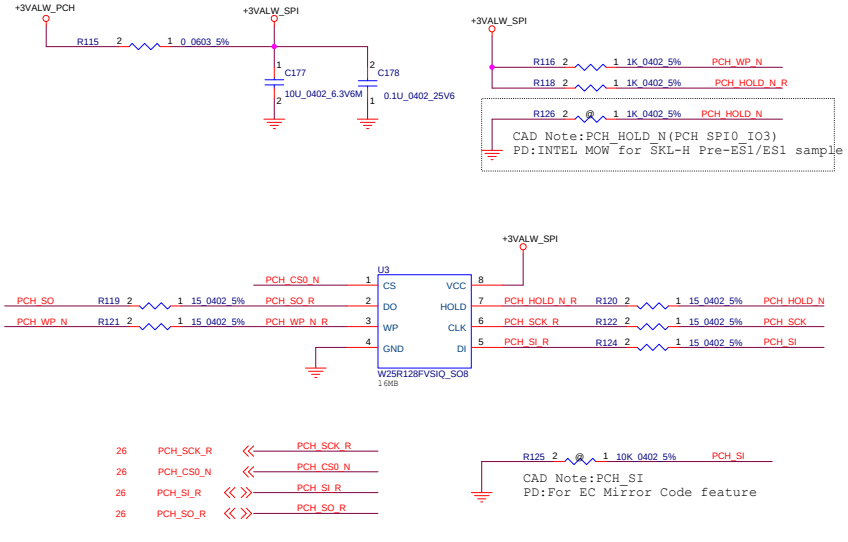


lenovo联想	LENOVO.CRDN	
Title: DDR4-VREF		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 16 of 99	

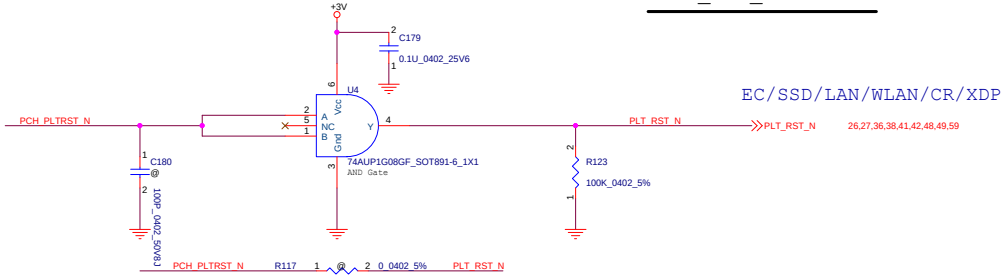
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



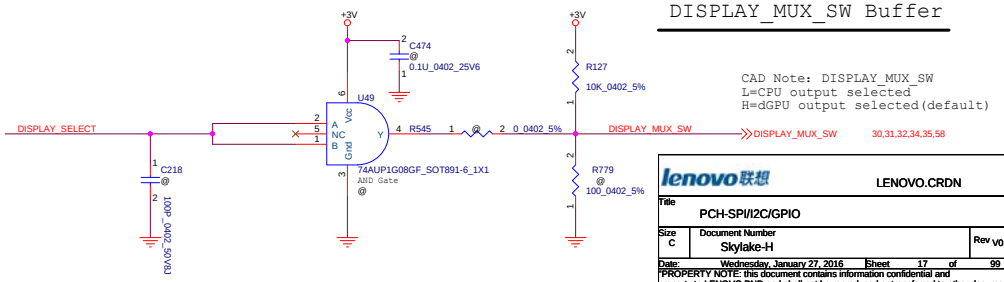
SPI ROM



PLT_RST_N Buffer



DISPLAY_MUX_SW Buffer



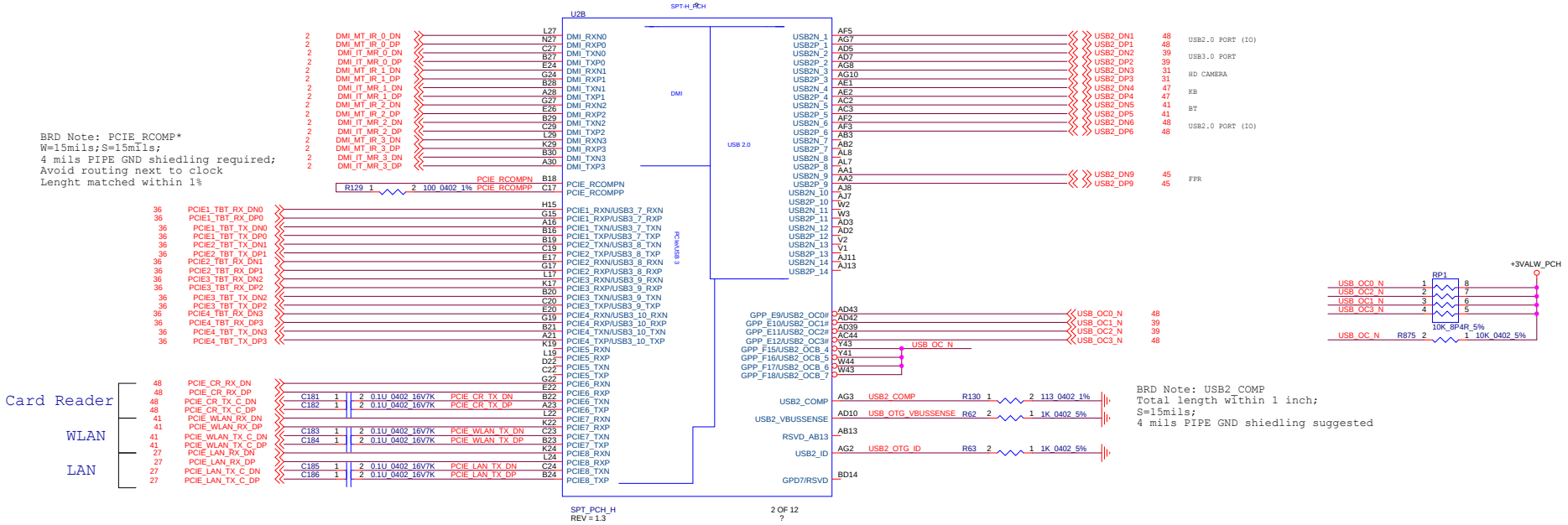
Title	PCH-SPI/I2C/GPIO
Size	C
Document Number	Skylake-H
Rev	V0.3
Date	Wednesday, January 27, 2016
Sheet	17 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

LENOVO.CRDN

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 7	USB3_7 / PCIE 1	AR (L0)	U2005 (Intel AR DP)	
Port 8	USB3_8 / PCIE 2	AR (L1)		
Port 9	USB3_9 / PCIE 3	AR (L2)		
Port 10	USB3_10 / PCIE 4	AR (L3)		
Port 11	PCIE 5	NC		
Port 12	PCIE 6	Card Reader	U3001	PCIE 1x Gen2
Port 13	PCIE 7	WLAN	JWLAN1	PCIE 1x Gen2
Port 14	PCIE 8	LAN	U6	PCIE1x Gen1

USB2.0 Configuration		
USB2 #	Assignment	OCx #
USB2 1	JUSB3(IO DB)	USB_OC0_N
USB2 2	JUSB2	USB_OC1_N
USB2 3	HD camera	
USB2 4	KB	
USB2 5	BT	
USB2 6	JUSB4(IO DB)	USB_OC3_N
USB2 7	NC	
USB2 8	NC	
USB2 9	Finger print	
USB2 10	NC	
USB2 11	NC	
USB2 12	NC	
USB2 13	NC	
USB2 14	NC	



BRD Note: USB2_COMP
Total length within 1 inch;
S=15mils;
4 mils PIPE GND shiedling suggested

BRD Note: PCIE BUS
All the AC-coupling caps placed close to device down or connector;
Non-interleaved breakout is required

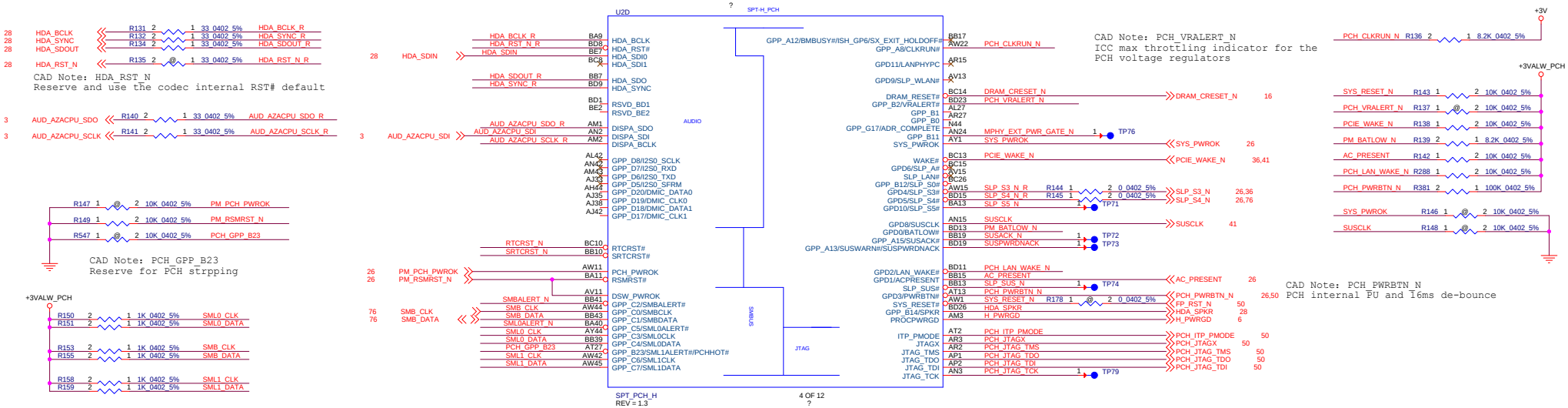
lenovo联想 LENOVO.CRDN

Title: PCH-DMI/PCIE/USB2.0

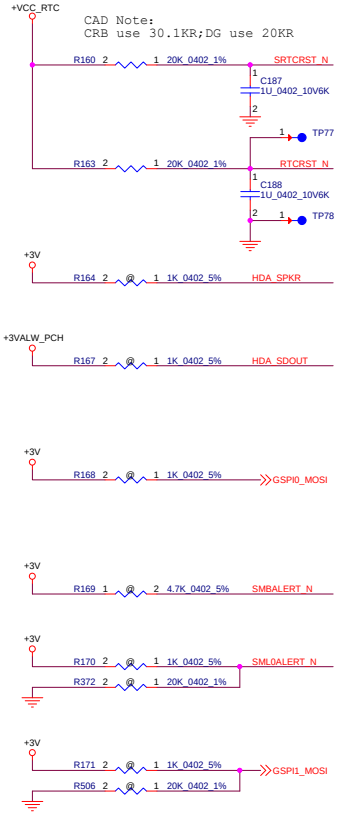
Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 18 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



PCH Straps



ME RESET

SRTCRST_N	1:SAVE ME (Default) *
	0:CLEAR ME

CMOS RESET

RTCRST_N	1:SAVE CMOS (Default) *
	0:CLEAR CMOS

Top Swap MODE

HDA_SPKR	1:Enabled
	0:Disabled(Default),Internal PD *

Flash Descriptor Security Override

HDA_SDOUT	1:Disabled
	0:Enabled(Default),Internal PD *

TCO Timer System No Reboot mode

GSPI0_MOSI	1:Enable "No reboot" mode
	0:Disable (Default),Internal PD *

Intel ME TLS cipher suite

SMBALERT_N	1:Enabled
	0:Disabled(Default),Internal PD *

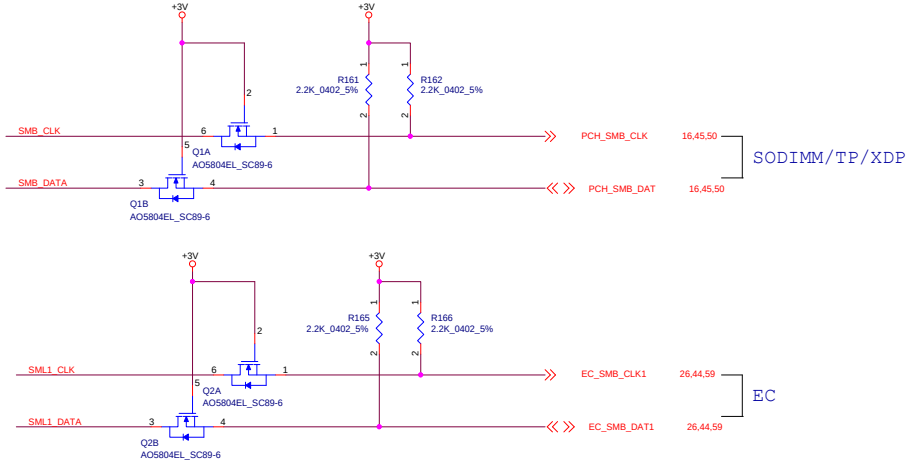
eSPI or LPC bus for EC

SML0ALERT_N	1:eSPI
	0:LPC(Default),Internal PD *

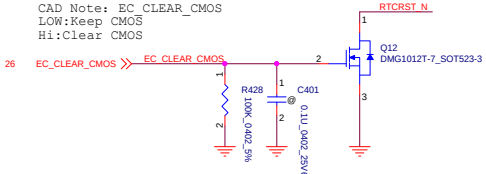
Boot BIOS Destination Bit 10

GSPI1_MOSI	1:LPC
	0:SPI(Default),Internal PD *

SMBus Isolation



EC Clear CMOS

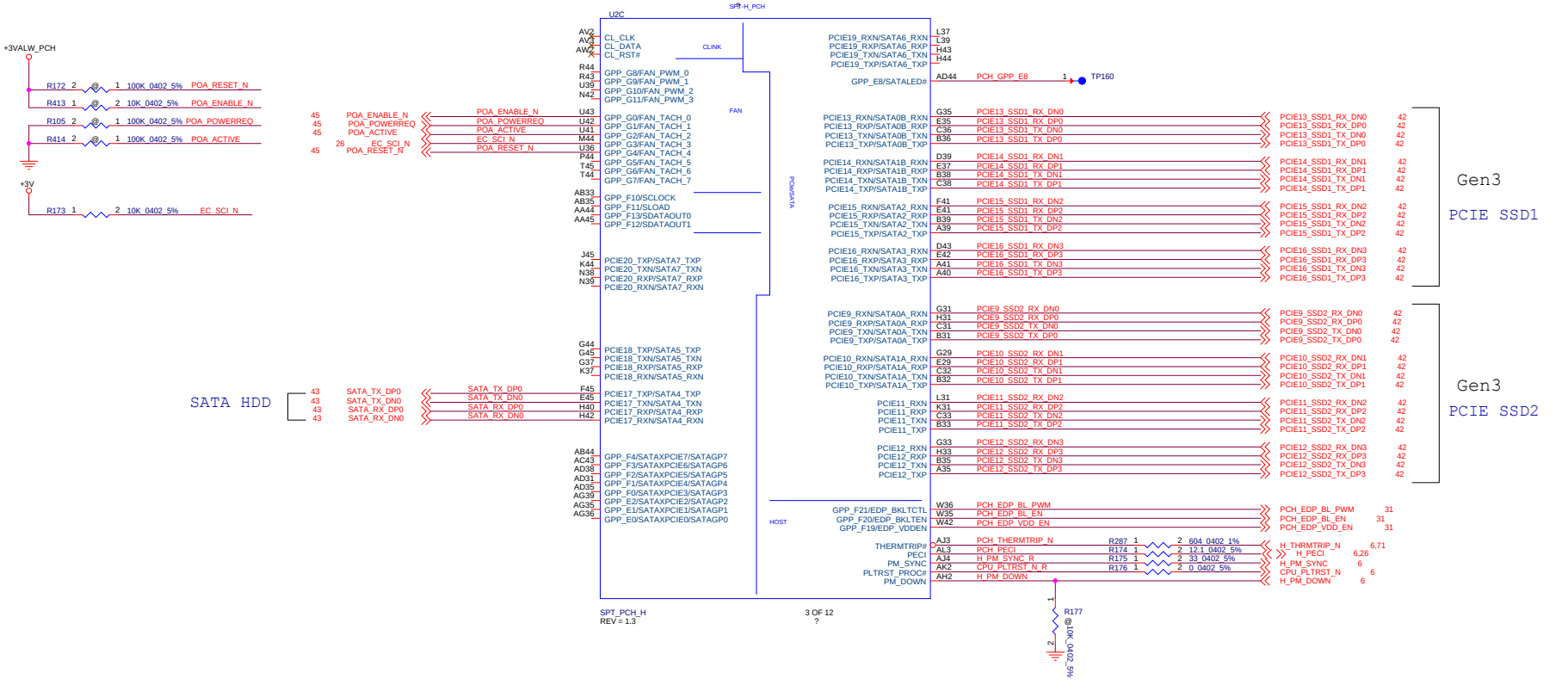


lenovo联想	LENOVO.CRDN		
Title	PCH-HDA/PM/SMBUS/STRAP		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 19 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

Flexible I/O Configuration

I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 15	SATA 0A / PCIE 9	M.2 SSD2 (L0) / SATA0	JSSD2	PCIE 4x Gen 3 /SATA Gen 3
Port 16	SATA 1A / PCIE 10	M.2 SSD2 (L1)		
Port 17	/ PCIE 11	M.2 SSD2 (L2)		
Port 18	/ PCIE 12	M.2 SSD2 (L3)		
Port 19	SATA 0B / PCIE 13	M.2 SSD12(L0)	JSSD1	PCIE 4 x Gen 3
Port 20	SATA 1B / PCIE 14	M.2 SSD1 (L1)		
Port 21	SATA 2 / PCIE 15	M.2 SSD1 (L2)		
Port 22	SATA 3 / PCIE 16	M.2 SSD1 (L3)		
Port 23	SATA 4 / PCIE 17	SATA HDD	U14	SATA Gen 3
Port 24	SATA 5 / PCIE 18	NC		
Port 25	SATA6 / PCIE 19	NC		
Port 26	SATA7 / PCIE 20	NC		

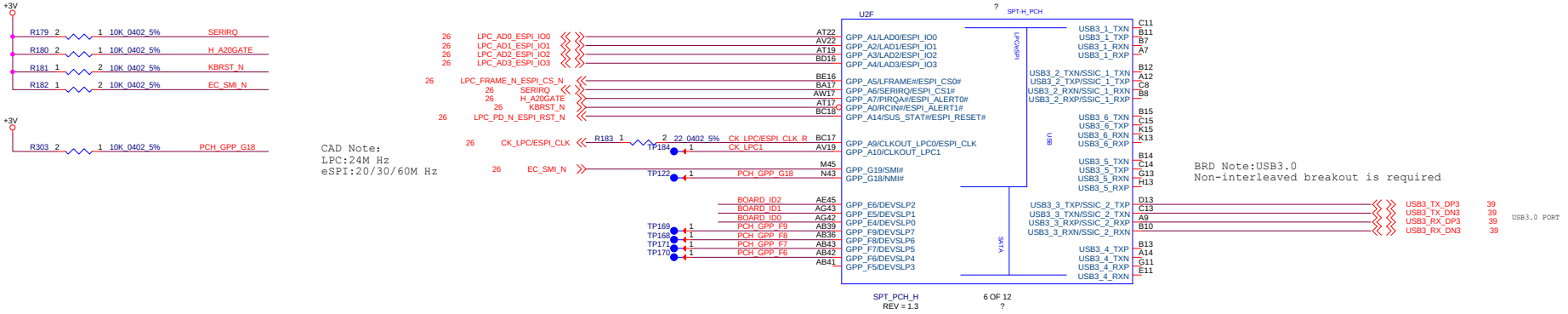


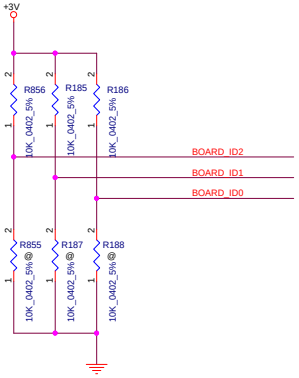
BRD Note: PCIE BUS
All the AC-coupling caps placed close to connector side;
Non-interleaved breakout is required

lenovo联想	LENOVO.CRDN	
Title: PCH-PCIE/SATA/HOST		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 20 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	OCx #
Port 1	USB3 1 Capable of OTG	NC		
Port 2	USB2 3 / SSIC 1	NC		
Port 3	USB3 3 / SSIC 2	USB3.0	JUSB2	USB_OC1_N
Port 4	USB3 4	NC		
Port 5	USB3 5	NC		
Port 6	USB3 6	NC		





BOARD_ID2	BOARD_ID1	BOARD_ID0	Description
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

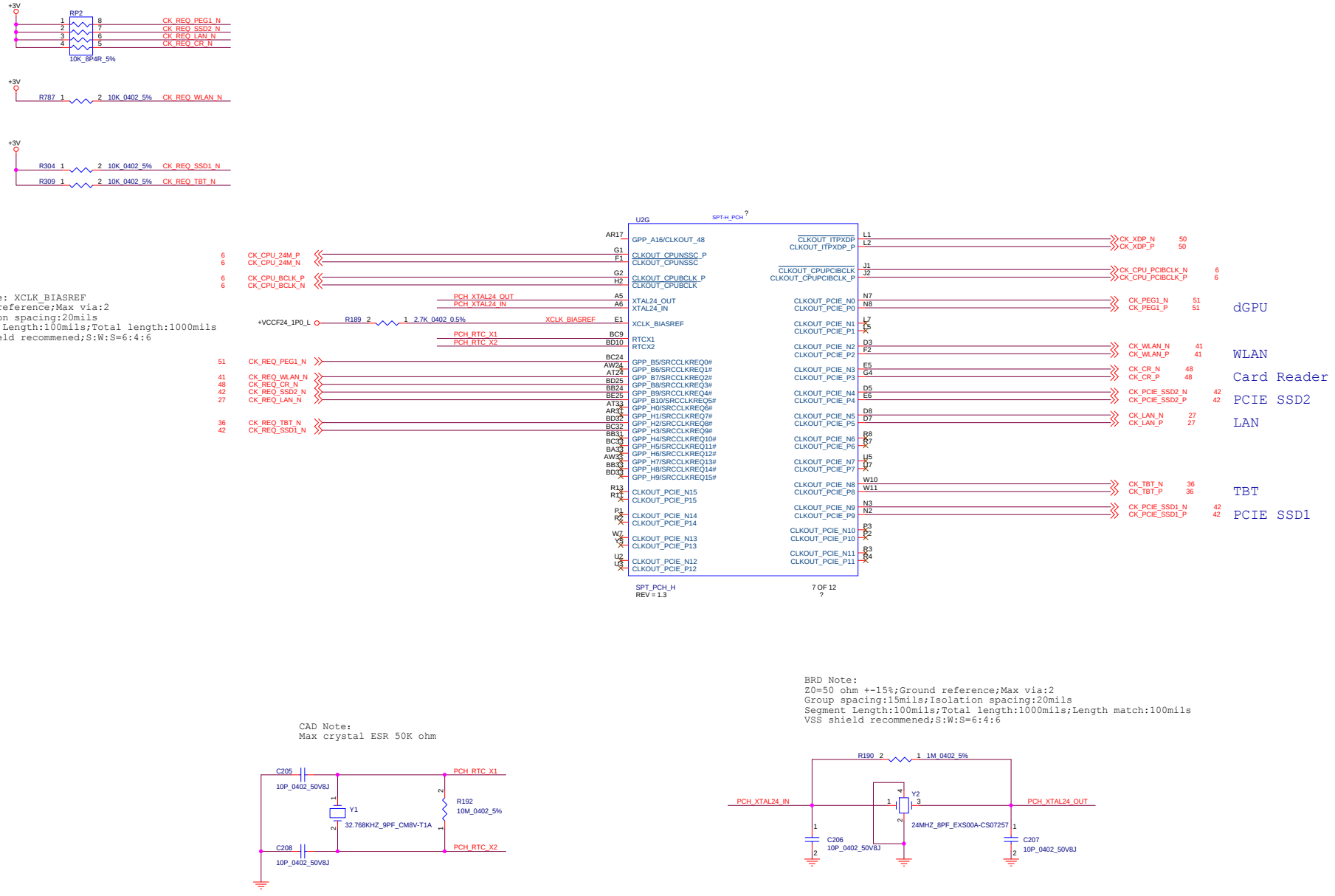
lenovo联想 LENOVO.CRDN

Title: PCH-USB3.0/LPC

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 21 of 99

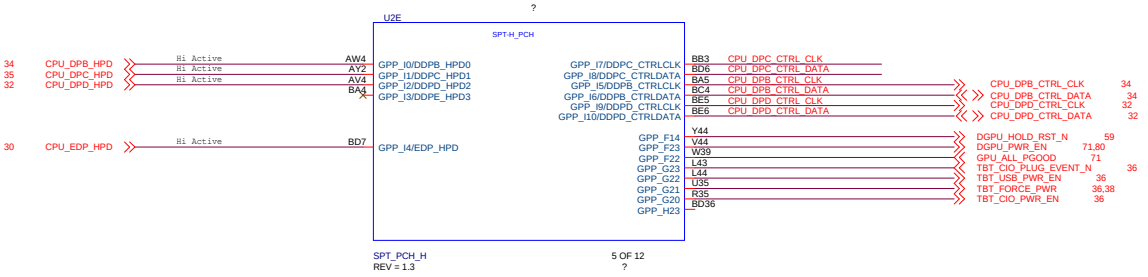
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

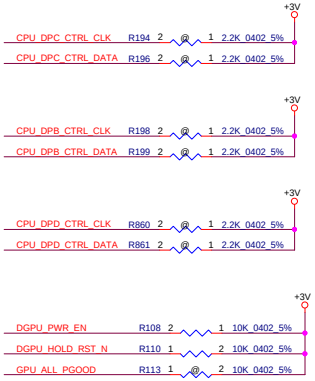


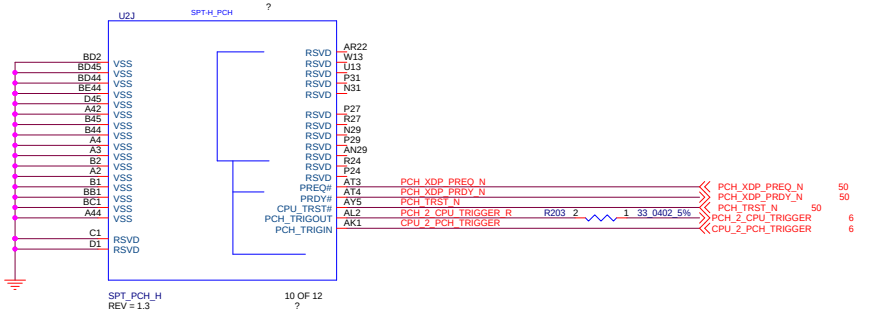
lenovo联想	LENOVO.CRDN	
Title: PCH-CLOCK		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 22 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

CAD Note: DP*_CTRL_DATA(Internal 20K PD)
NC:Disable DP Port



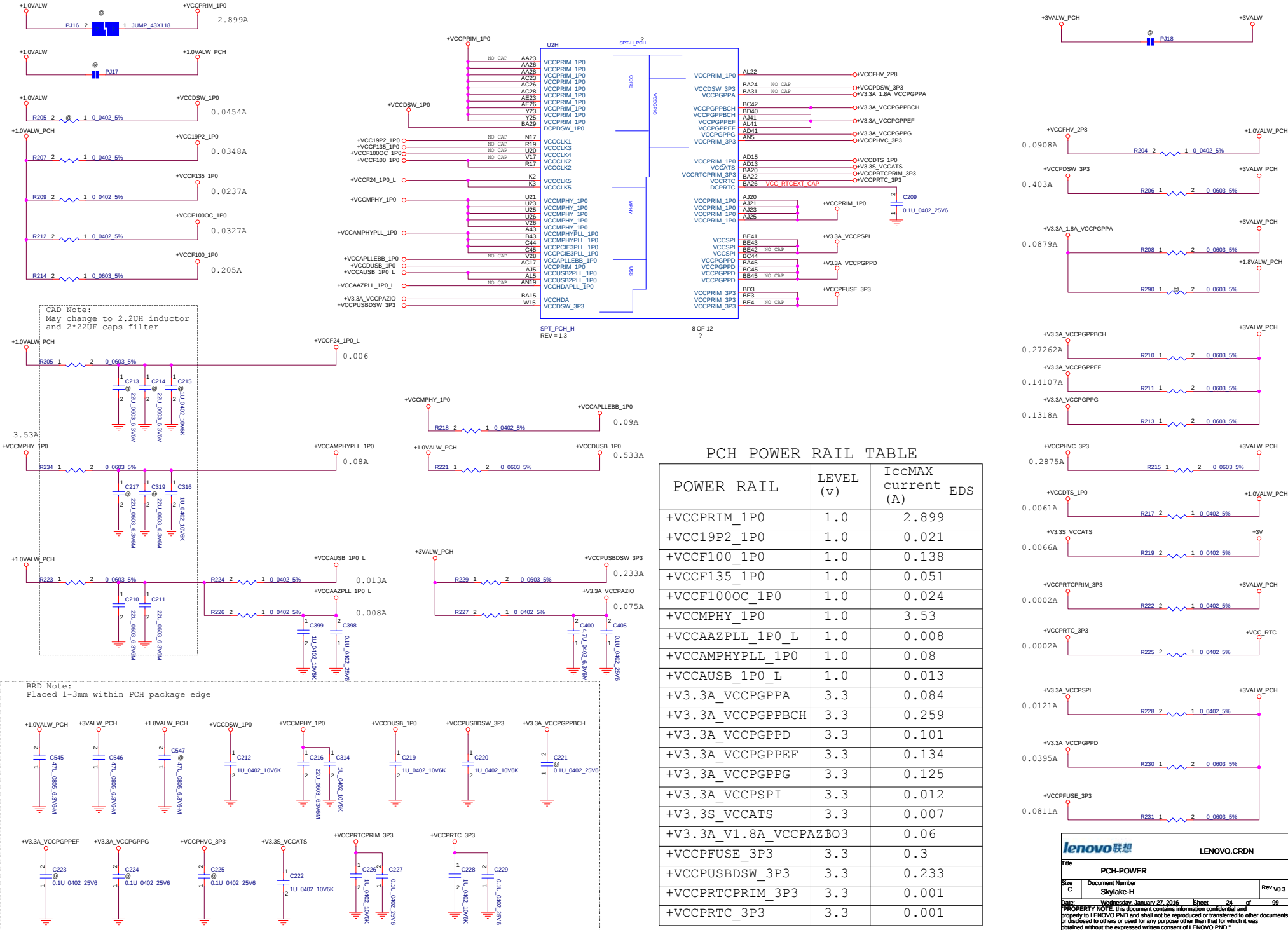




CAD Note:
CRB use 30R;DG use 0R

lenovo联想	LENOVO.CRDN	
Title: PCH-DISPLAY/RSVD		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 23 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



PCH POWER RAIL TABLE

POWER RAIL	LEVEL (v)	IccMAX current (A) EDS
+VCCPRIM_1P0	1.0	2.899
+VCC19P2_1P0	1.0	0.021
+VCCF100_1P0	1.0	0.138
+VCCF135_1P0	1.0	0.051
+VCCF100OC_1P0	1.0	0.024
+VCCMPHY_1P0	1.0	3.53
+VCCAAZPLL_1P0_L	1.0	0.008
+VCCAMPHYPLL_1P0	1.0	0.08
+VCCAUSB_1P0_L	1.0	0.013
+V3.3A_VCCPGPPA	3.3	0.084
+V3.3A_VCCPGPPBCH	3.3	0.259
+V3.3A_VCCPGPPD	3.3	0.101
+V3.3A_VCCPGPPEF	3.3	0.134
+V3.3A_VCCPGPPG	3.3	0.125
+V3.3A_VCCPSPI	3.3	0.012
+V3.3S_VCCATS	3.3	0.007
+V3.3A_V1.8A_VCCPAZ303	3.3	0.06
+VCCPFUSE_3P3	3.3	0.3
+VCCPUSBDSW_3P3	3.3	0.233
+VCCPRTCPRIM_3P3	3.3	0.001
+VCCPRTC_3P3	3.3	0.001

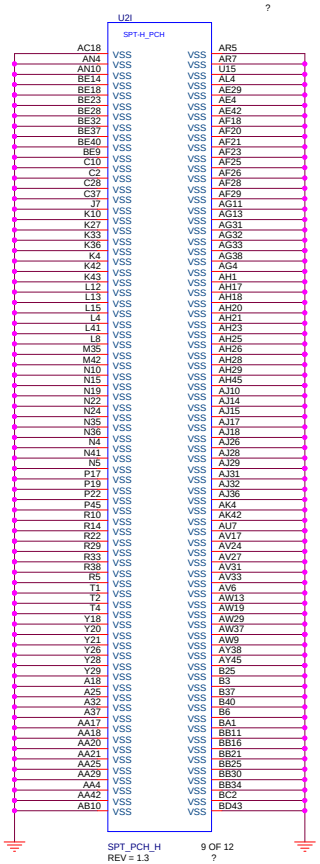
LENOVO.CRDN

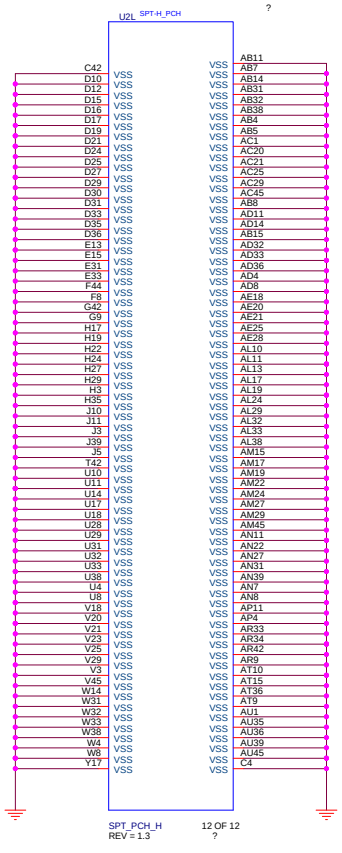
Title: PCH-POWER

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 24 of 99

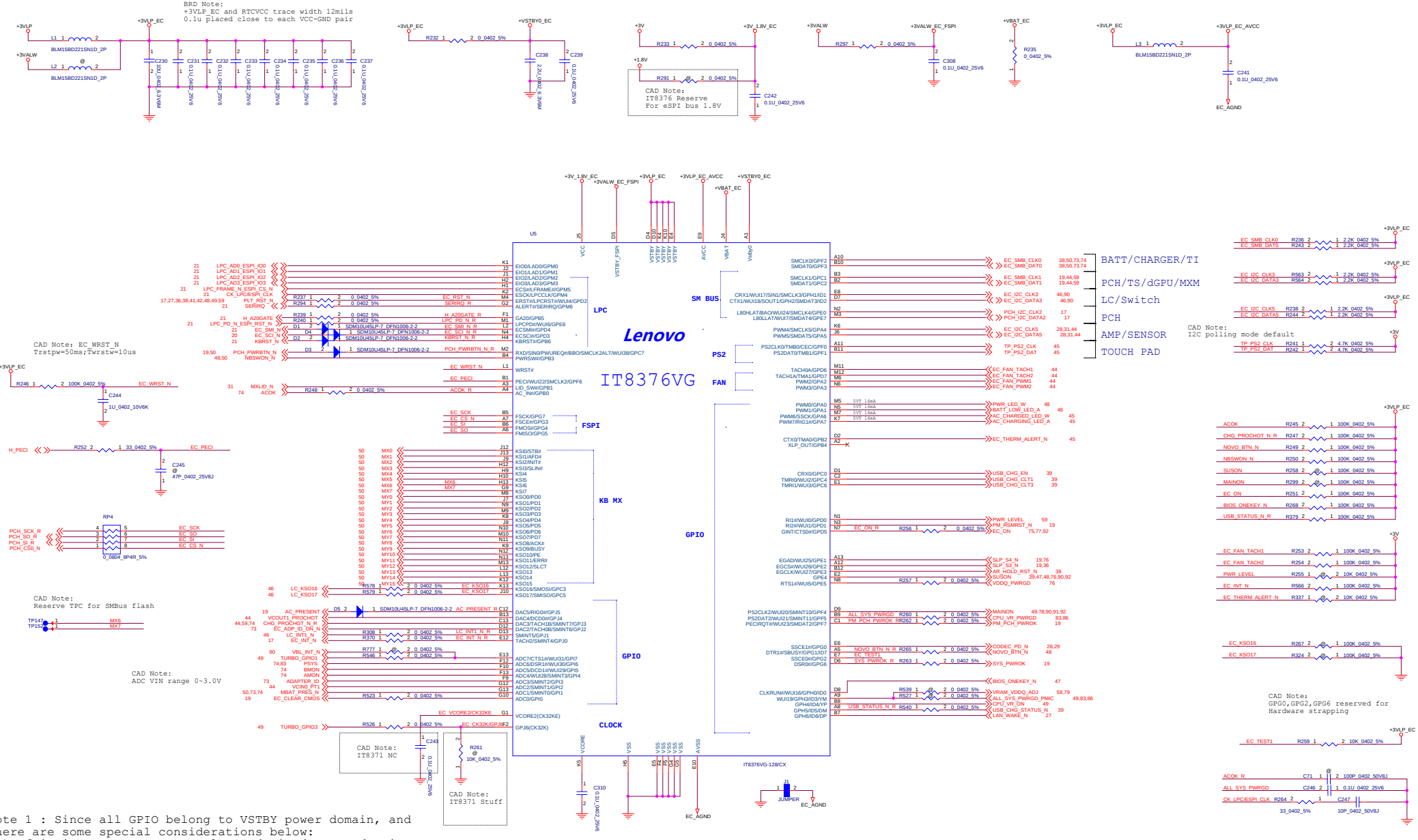
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."





lenovo联想	LENOVO.CRDN	
Title: PCH-VSS		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 25 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

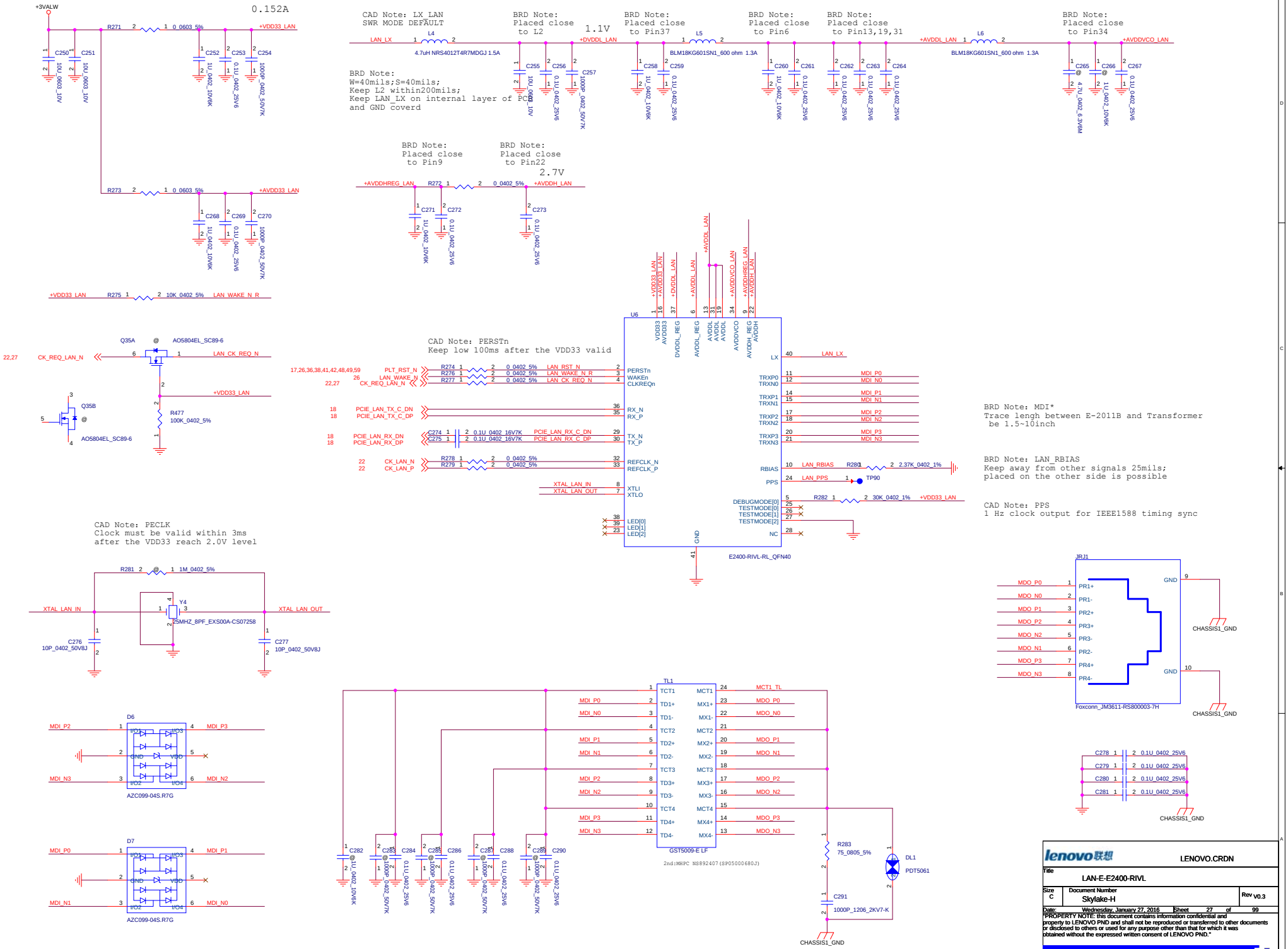


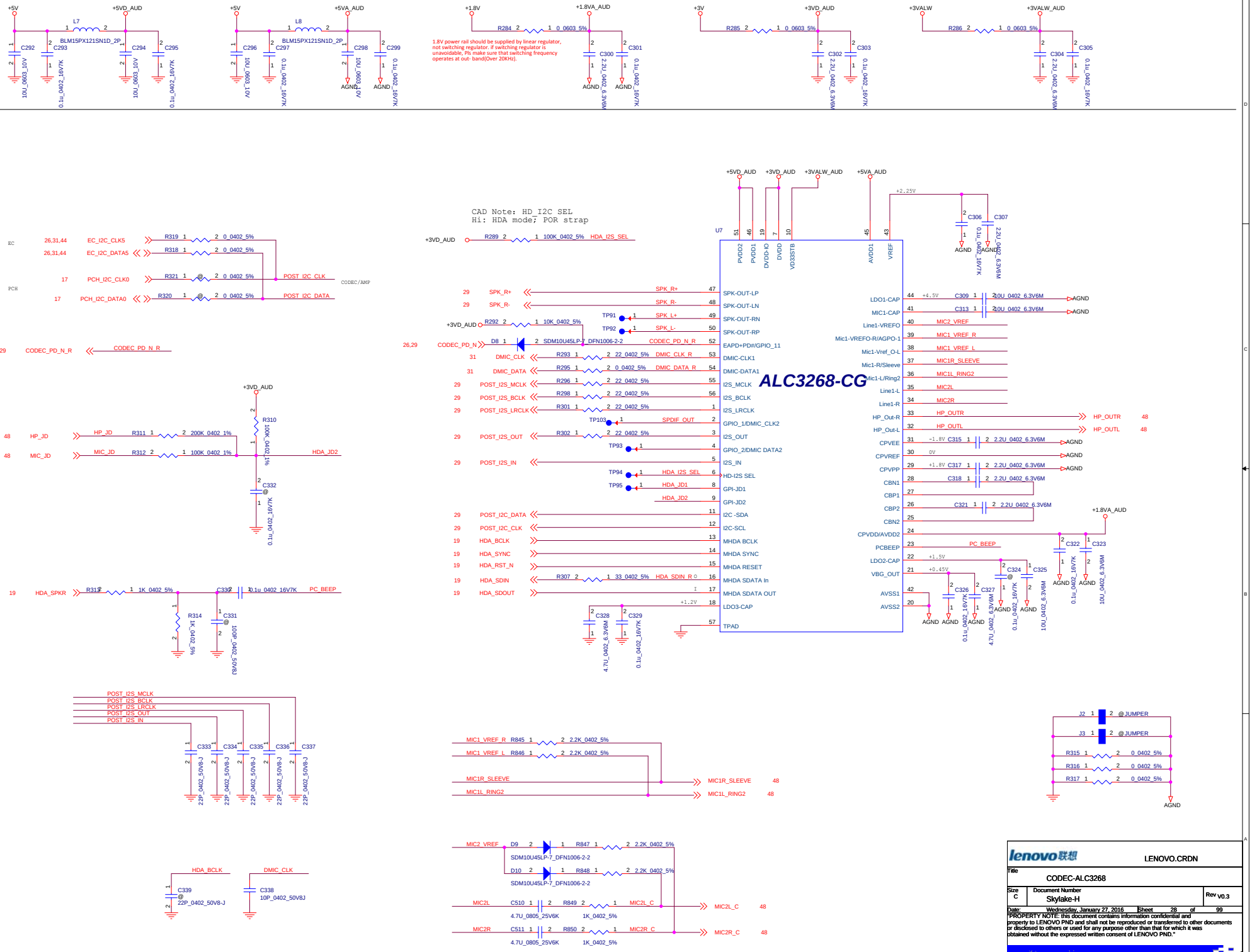
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

lenovo联想	LENOVO.CRDN	
Title	EC IT8376VG	
Size: Custom	Document Number: Skylake-H	Rev: v0.3
Date: Wednesday, January 27, 2016	Sheet 26 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


0.152A
+3VALW
R271 0 0603 5%
+VDD33_LAN
C250 10U_0603_10V
C251 10U_0603_10V
C252 1U_0402_10V6K
C253 0.1U_0402_25V6
C254 1000P_0402_50V7K
R273 0 0603 5%
+AVDD33_LAN
C268 1U_0402_10V6K
C269 0.1U_0402_25V6
C270 1000P_0402_50V7K
+VDD33_LAN
R275 10K_0402_5%
LAN_WAKE_N_R
CAD Note: LX_LAN
SWR MODE DEFAULT
BRD Note:
Placed close
to L2
1.1V
LAN_LX
L4
4.7uH NRS4012T4R7MDGJ 1.5A
+DVDDL_LAN
C255 10U_0603_10V
C256 0.1U_0402_25V6
C257 1000P_0402_50V7K
BRD Note:
Placed close
to Pin37
L5
BLM18KG601SN1_600 ohm 1.3A
C258 1U_0402_10V6K
C259 0.1U_0402_25V6
BRD Note:
Placed close
to Pin6
C260 1U_0402_10V6K
C261 0.1U_0402_25V6
BRD Note:
Placed close
to Pin13,19,31
C262 0.1U_0402_25V6
C263 0.1U_0402_25V6
C264 0.1U_0402_25V6
+AVDDL_LAN
L6
BLM18KG601SN1_600 ohm 1.3A
BRD Note:
Placed close
to Pin34
+AVDDVCO_LAN
C265 4.7U_0402_6.3V6M
C266 1U_0402_10V6K
C267 0.1U_0402_25V6
BRD Note:
W=40mils;S=40mils;
Keep L2 within200mils;
Keep LAN_LX on internal layer of PCB
and GND coverd
BRD Note:
Placed close
to Pin9
BRD Note:
Placed close
to Pin22
2.7V
+AVDDHREG_LAN
R272 0_0402_5%
+AVDDH_LAN
C271 1U_0402_10V6K
C272 0.1U_0402_25V6
C273 0.1U_0402_25V6
Q35A AO5804EL_SC89-6
22,27 CK_REQ_LAN_N
LAN_CK_REQ_N
Q35B
+VDD33_LAN
R477 100K_0402_5%
CAD Note: PERSTn
Keep low 100ms after the VDD33 valid
U6
+VDD33_LAN
+AVDD33_LAN
+DVDDL_LAN
+AVDDL_LAN
+AVDDVCO_LAN
+AVDDHREG_LAN
VDD33
AVDD33
DVDDL_3E
AVDDL_3E
AVDDL
AVDDL
AVDDL
AVDDVCO
AVDDH_3E
AVDDH
LX
LAN_LX
17,26,36,38,41,42,48,49,59 PLT_RST_N
26 LAN_WAKE_N
22,27 CK_REQ_LAN_N
R274 0_0402_5% LAN_RST_N
R276 0_0402_5% LAN_WAKE_N_R
R277 0_0402_5% LAN_CK_REQ_N
PERSTn
WAKEn
CLKREQn
18 PCIE_LAN_TX_C_DN
18 PCIE_LAN_TX_C_DP
RX_N
RX_P
18 PCIE_LAN_RX_DN
18 PCIE_LAN_RX_DP
C274 0.1U_0402_16V7K PCIE_LAN_RX_C_DN
C275 0.1U_0402_16V7K PCIE_LAN_RX_C_DP
TX_N
TX_P
22 CK_LAN_N
22 CK_LAN_P
R278 0_0402_5%
R279 0_0402_5%
REFCLK_N
REFCLK_P
XTAL_LAN_IN
XTAL_LAN_OUT
XTLI
XTLO
LED[0]
LED[1]
LED[2]
GND
E2400-RIVL-RL_QFN40
TRXP0 TRXN0 MDI_P0 MDI_N0
TRXP1 TRXN1 MDI_P1 MDI_N1
TRXP2 TRXN2 MDI_P2 MDI_N2
TRXP3 TRXN3 MDI_P3 MDI_N3
RBIAS LAN_RBIAS R281 2.37K_0402_1%
PPS LAN_PPS TP90
DEBUGMODE[0]
TESTMODE[0]
TESTMODE[1]
TESTMODE[2]
NC
R282 30K_0402_1% +VDD33_LAN
BRD Note: MDI*
Trace lengh between E-2011B and Transformer
be 1.5~10inch
BRD Note: LAN_RBIAS
Keep away from other signals 25mils;
placed on the other side is possible
CAD Note: PPS
1 Hz clock output for IEEE1588 timing sync
CAD Note: PECLK
Clock must be valid within 3ms
after the VDD33 reach 2.0V level
R281 1M_0402_5%
XTAL_LAN_IN
XTAL_LAN_OUT
Y4
25MHZ_8PF_EXS00A-CS07258
C276 10P_0402_50V8J
C277 10P_0402_50V8J
D6
MDI_P2
MDI_P3
MDI_N3
MDI_N2
AZC099-04S.R7G
D7
MDI_P0
MDI_P1
MDI_N1
MDI_N0
AZC099-04S.R7G
TL1
MCT1_TL
MDI_P0
MDO_P0
MDI_N0
MDO_N0
MDI_P1
MDO_P1
MDI_N1
MDO_N1
MDI_P2
MDO_P2
MDI_N2
MDO_N2
MDI_P3
MDO_P3
MDI_N3
MDO_N3
GST5009-E LF
2nd:MHPC NS892407(SP05000680J)
C282 1U_0402_10V6K
C283 1000P_0402_50V7K
C284 0.1U_0402_25V6
C285 1000P_0402_50V7K
C286 0.1U_0402_25V6
C287 1000P_0402_50V7K
C288 0.1U_0402_25V6
C289 1000P_0402_50V7K
C290 0.1U_0402_25V6
R283 75_0805_5%
DL1
PDT5061
C291 1000P_1206_2KV7-K
CHASSIS1_GND
JRJ1
MDO_P0
MDO_N0
MDO_P1
MDO_P2
MDO_N2
MDO_N1
MDO_P3
MDO_N3
PR1+
PR1-
PR2+
PR3+
PR3-
PR2-
PR4+
PR4-
GND
Foxconn_JM3611-RS800003-7H
CHASSIS1_GND
C278 0.1U_0402_25V6
C279 0.1U_0402_25V6
C280 0.1U_0402_25V6
C281 0.1U_0402_25V6
CHASSIS1_GND
lenovo联想
LENOVO.CRDN
Title
LAN-E-E2400-RIVL
Size C
Document Number
Skylake-H
Rev V0.3
Date: Wednesday, January 27, 2016
Sheet 27 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



Title	CODEC-ALC3268
Size	C
Document Number	Skylake-H
Rev	V0.3
Date:	Wednesday, January 27, 2016
Sheet	28 of 99

LENOVO.CRDN

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

CAD Note: POST_I2C*
connect to PCH default and reserve to EC
PU at PCH or EC side

BRD Note:
placed near to Pin6&7
and Pin41&42&43 seperately

BRD Note:
Route 40 mils width and As short as possible

Internal Speaker

CAD Note: POST_I2S_MCLK
Use TAS5766M internal MCLK default

TAS5766M

I2C ADDRESS:0x 1001_100x

CAD Note: AMP_PD_R_N
Low active to mute,
Tr/Tf less than 20ns

TPA3113D2PWPR

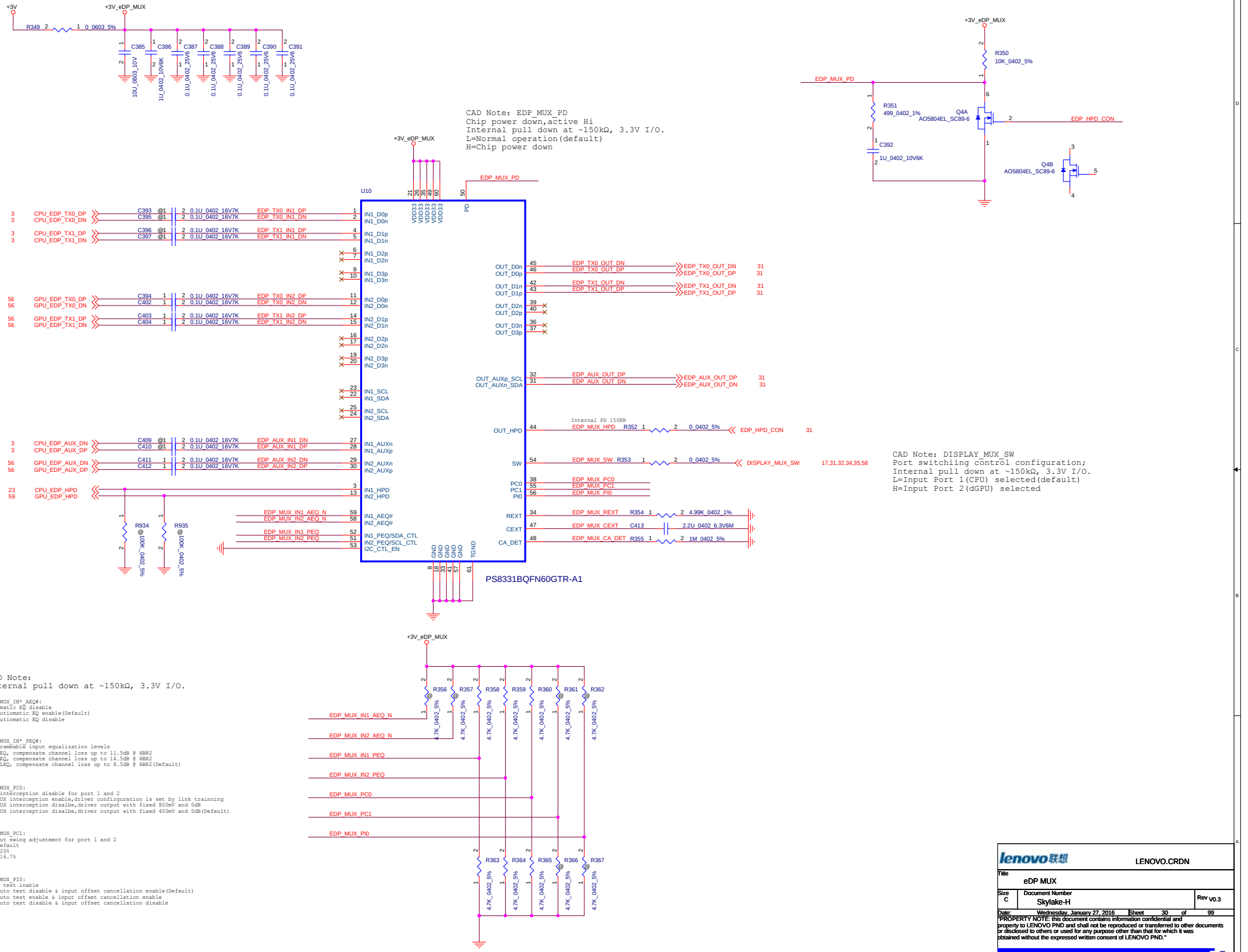
BRD Note:
Route 40 mils width

Sub Woofer

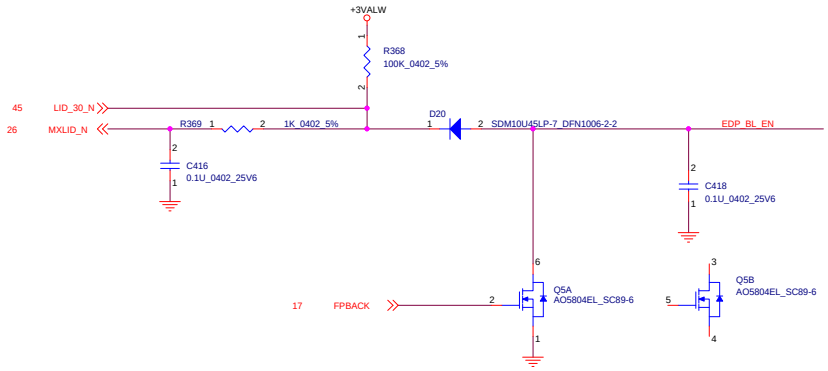
CAD Note: SWF_GAIN[1::0]
00:Gain=20dB,RI=60k ohm(Default)
01:Gain=26dB,RI=30k ohm
00:Gain=32dB,RI=15k ohm
00:Gain=38dB,RI=9k ohm

lenovo联想	LENOVO.CRDN	
Title: AMP		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 29 of 99	

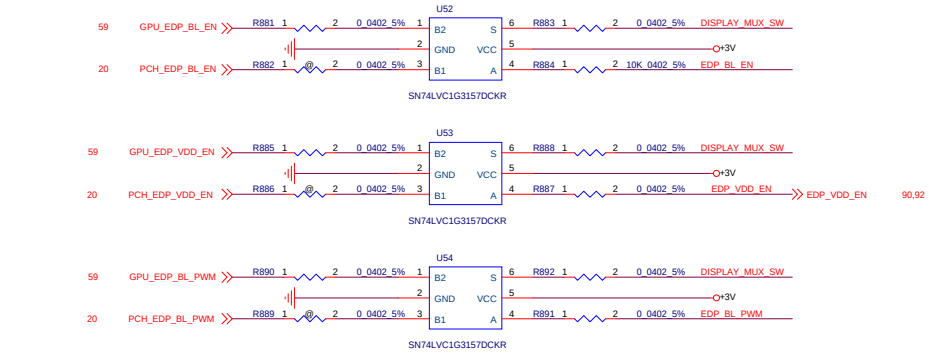
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


210mA
+3V
+3V_eDP_MUX
R349 2 1 0 0603 5%
C385 10U_0603_10V
C386 1U_0402_10V6K
C387 0.1U_0402_25V6
C388 0.1U_0402_25V6
C389 0.1U_0402_25V6
C390 0.1U_0402_25V6
C391 0.1U_0402_25V6
CAD Note: EDP_MUX_PD
Chip power down,active Hi
Internal pull down at ~150kΩ, 3.3V I/O.
L=Normal operation(default)
H=Chip power down
U10
EDP_MUX_PD
VDD33
PD
CPU_EDP_TX0_DP
CPU_EDP_TX0_DN
CPU_EDP_TX1_DP
CPU_EDP_TX1_DN
GPU_EDP_TX0_DP
GPU_EDP_TX0_DN
GPU_EDP_TX1_DP
GPU_EDP_TX1_DN
0.1U_0402_16V7K
EDP_TX0_IN1_DP
EDP_TX0_IN1_DN
EDP_TX1_IN1_DP
EDP_TX1_IN1_DN
EDP_TX0_IN2_DP
EDP_TX0_IN2_DN
EDP_TX1_IN2_DP
EDP_TX1_IN2_DN
IN1_D0p
IN1_D0n
IN1_D1p
IN1_D1n
IN1_D2p
IN1_D2n
IN1_D3p
IN1_D3n
IN2_D0p
IN2_D0n
IN2_D1p
IN2_D1n
IN2_D2p
IN2_D2n
IN2_D3p
IN2_D3n
OUT_D0n
OUT_D0p
OUT_D1n
OUT_D1p
OUT_D2n
OUT_D2p
OUT_D3n
OUT_D3p
EDP_TX0_OUT_DN
EDP_TX0_OUT_DP
EDP_TX1_OUT_DN
EDP_TX1_OUT_DP
EDP_TX0_OUT_DN 31
EDP_TX0_OUT_DP 31
EDP_TX1_OUT_DN 31
EDP_TX1_OUT_DP 31
IN1_SCL
IN1_SDA
IN2_SCL
IN2_SDA
OUT_AUXp_SCL
OUT_AUXn_SDA
EDP_AUX_OUT_DP
EDP_AUX_OUT_DN
EDP_AUX_OUT_DP 31
EDP_AUX_OUT_DN 31
CPU_EDP_AUX_DN
CPU_EDP_AUX_DP
GPU_EDP_AUX_DN
GPU_EDP_AUX_DP
EDP_AUX_IN1_DN
EDP_AUX_IN1_DP
EDP_AUX_IN2_DN
EDP_AUX_IN2_DP
IN1_AUXn
IN1_AUXp
IN2_AUXn
IN2_AUXp
OUT_HPD
Internal PD 150KR
EDP_MUX_HPD R352 0 0402 5%
EDP_HPD_CON 31
CPU_EDP_HPD
GPU_EDP_HPD
IN1_HPD
IN2_HPD
SW
EDP_MUX_SW R353 0 0402 5%
DISPLAY_MUX_SW 17,31,32,34,35,58
PC0
PC1
PI0
EDP_MUX_PC0
EDP_MUX_PC1
EDP_MUX_PI0
R934 @ 100K_0402_5%
R935 @ 100K_0402_5%
EDP_MUX_IN1_AEQ_N
EDP_MUX_IN2_AEQ_N
IN1_AEQ#
IN2_AEQ#
EDP_MUX_IN1_PEQ
EDP_MUX_IN2_PEQ
IN1_PEQ/SDA_CTL
IN2_PEQ/SCL_CTL
I2C_CTL_EN
REXT
CEXT
CA_DET
EDP_MUX_REXT R354 4.99K 0402 1%
EDP_MUX_CEXT C413 2.2U 0402 6.3V6M
EDP_MUX_CA_DET R355 1M 0402 5%
GND
TGND
PS8331BQFN60GTR-A1
+3V_eDP_MUX
R350 10K_0402_5%
EDP_MUX_PD
R351 499_0402_1%
C392 1U_0402_10V6K
Q4A AO5804EL_SC89-6
Q4B AO5804EL_SC89-6
EDP_HPD_CON
CAD Note: DISPLAY_MUX_SW
Port switchiing control configuration;
Internal pull down at ~150kΩ, 3.3V I/O.
L=Input Port 1(CPU) selected(default)
H=Input Port 2(dGPU) selected
CAD Note:
Internal pull down at ~150kΩ, 3.3V I/O.
EDP_MUX_IN*_AEQ#:
Automatic EQ disable
L:Autiomatic EQ enable(Default)
H:Autiomatic EQ disable
EDP_MUX_IN*_PEQ#:
Programmable input equalization levels
L:LEQ, compensate channel loss up to 11.5dB @ HBR2
H:HEQ, compensate channel loss up to 14.5dB @ HBR2
M:LLEQ, compensate channel loss up to 8.5dB @ HBR2(Default)
EDP_MUX_PC0:
AUX interception disable for port 1 and 2
L:AUX interception enable,driver configuration is set by link trainning
H:AUX interception disalbe,driver output with fixed 800mV and 0dB
M:AUX interception disalbe,driver output with fixed 400mV and 0dB(Default)
EDP_MUX_PC1:
Output swing adjustment for port 1 and 2
L:Default
H:+20%
M:-16.7%
EDP_MUX_PI0:
Auto test inable
L:Auto test disable & input offset cancellation enable(Default)
H:Auto test enable & input offset cancellation enable
M:Auto test disable & input offset cancellation disable
R356 R357 R358 R359 R360 R361 R362
R363 R364 R365 R366 R367
4.7K_0402_5%
lenovo联想
LENOVO.CRDN
Title
eDP MUX
Size C
Document Number
Skylake-H
Rev V0.3
Date: Wednesday, January 27, 2016
Sheet 30 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

Panel Backlight Control



PANLE Contrl switch

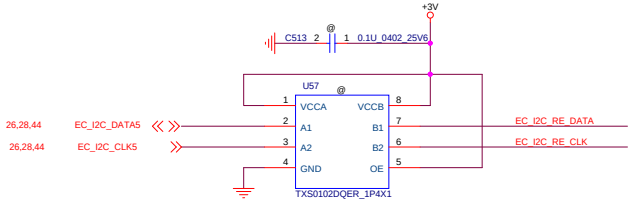


17,30,32,34,35,58 DISPLAY_MUX_SW → DISPLAY_MUX_SW

CAD Note: DISPLAY_MUX_SW
L=CPU output selected(default)
H=dGPU output selected

S control input	ON CHANNEL
L	B1
H	B2

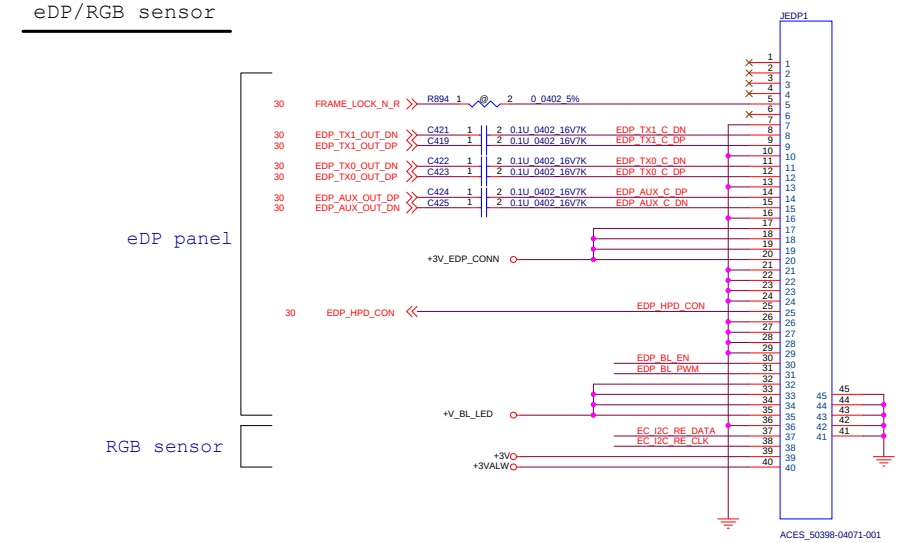
I2C Repeater

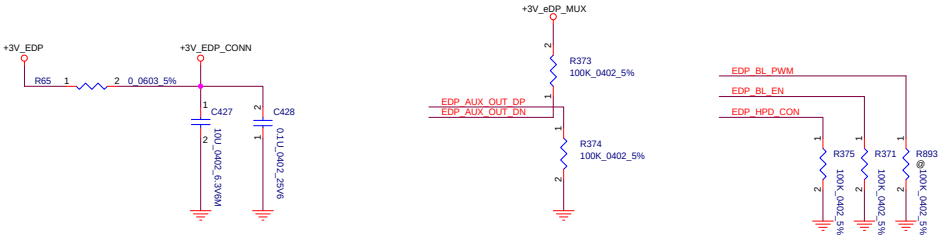


eDP/RGB sensor

eDP panel

RGB sensor

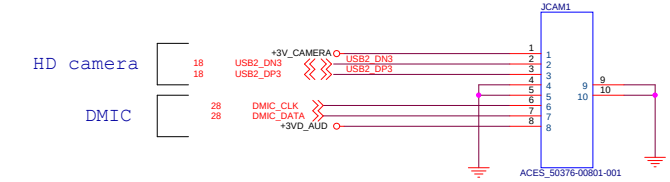


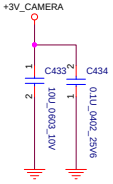


Camera/DMIC

HD camera

DMIC





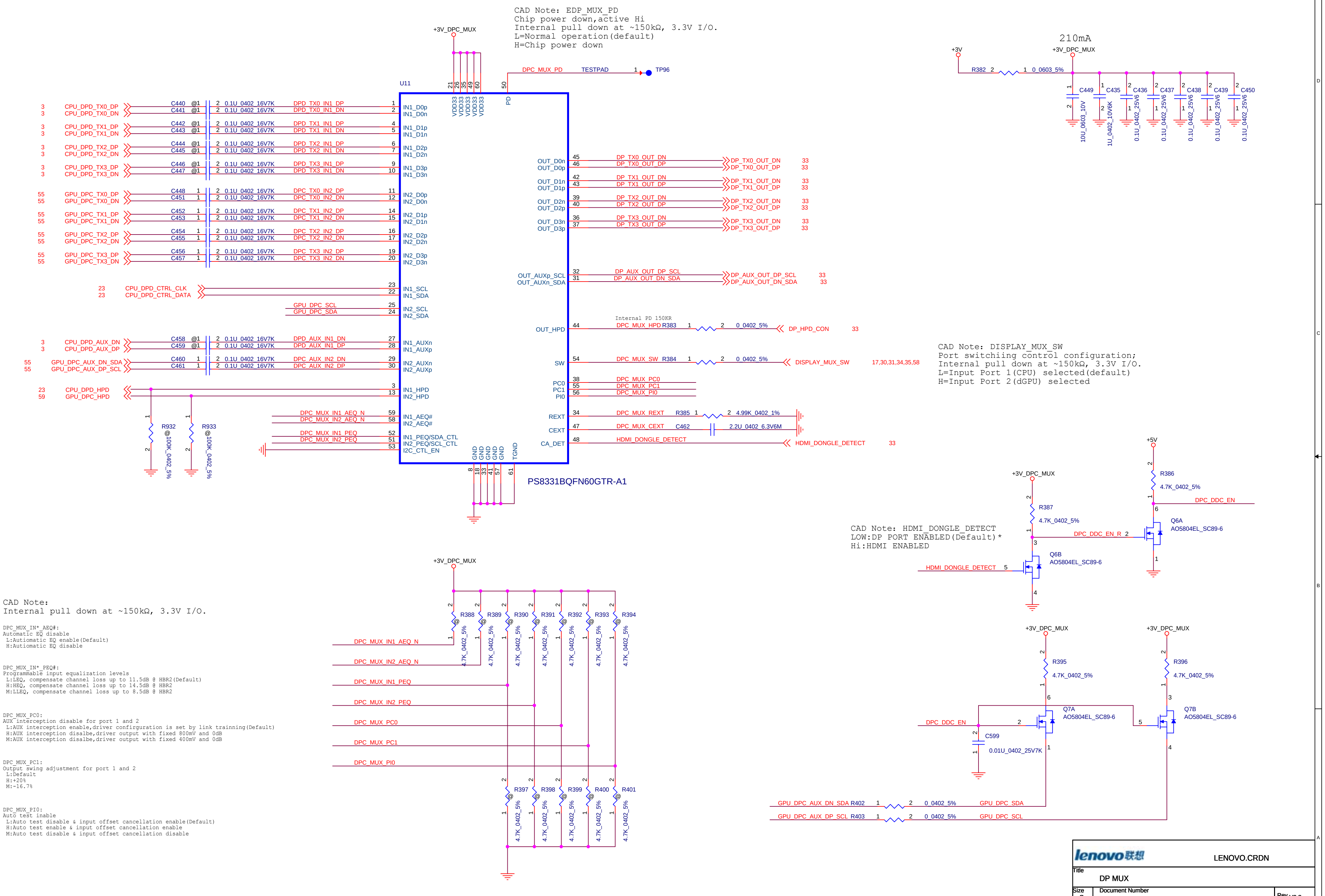
lenovo联想 LENOVO.CRDN

Title: eDP/RGB/CAMERA/DMIC

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 31 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


U11
PS8331BQFN60GTR-A1
+3V_DPC_MUX
DPC_MUX_PD
TESTPAD
TP96
IN1_D0p
IN1_D0n
IN1_D1p
IN1_D1n
IN1_D2p
IN1_D2n
IN1_D3p
IN1_D3n
IN2_D0p
IN2_D0n
IN2_D1p
IN2_D1n
IN2_D2p
IN2_D2n
IN2_D3p
IN2_D3n
IN1_SCL
IN1_SDA
IN2_SCL
IN2_SDA
IN1_AUXn
IN1_AUXp
IN2_AUXn
IN2_AUXp
IN1_HPD
IN2_HPD
IN1_AEQ#
IN2_AEQ#
IN1_PEQ/SDA_CTL
IN2_PEQ/SCL_CTL
I2C_CTL_EN
OUT_D0n
OUT_D0p
OUT_D1n
OUT_D1p
OUT_D2n
OUT_D2p
OUT_D3n
OUT_D3p
OUT_AUXp_SCL
OUT_AUXn_SDA
OUT_HPD
SW
PC0
PC1
PI0
REXT
CEXT
CA_DET
VDD33
GND
TGND
PD
CPU_DPD_TX0_DP
CPU_DPD_TX0_DN
CPU_DPD_TX1_DP
CPU_DPD_TX1_DN
CPU_DPD_TX2_DP
CPU_DPD_TX2_DN
CPU_DPD_TX3_DP
CPU_DPD_TX3_DN
GPU_DPC_TX0_DP
GPU_DPC_TX0_DN
GPU_DPC_TX1_DP
GPU_DPC_TX1_DN
GPU_DPC_TX2_DP
GPU_DPC_TX2_DN
GPU_DPC_TX3_DP
GPU_DPC_TX3_DN
CPU_DPD_CTRL_CLK
CPU_DPD_CTRL_DATA
GPU_DPC_SCL
GPU_DPC_SDA
CPU_DPD_AUX_DN
CPU_DPD_AUX_DP
GPU_DPC_AUX_DN_SDA
GPU_DPC_AUX_DP_SCL
CPU_DPD_HPD
GPU_DPC_HPD
0.1U_0402_16V7K
R932
R933
100K_0402_5%
DPC_MUX_IN1_AEQ_N
DPC_MUX_IN2_AEQ_N
DPC_MUX_IN1_PEQ
DPC_MUX_IN2_PEQ
DP_TX0_OUT_DN
DP_TX0_OUT_DP
DP_TX1_OUT_DN
DP_TX1_OUT_DP
DP_TX2_OUT_DN
DP_TX2_OUT_DP
DP_TX3_OUT_DN
DP_TX3_OUT_DP
DP_AUX_OUT_DP_SCL
DP_AUX_OUT_DN_SDA
Internal PD 150KR
DPC_MUX_HPD
R383
0_0402_5%
DP_HPD_CON
DPC_MUX_SW
R384
DISPLAY_MUX_SW
17,30,31,34,35,58
DPC_MUX_PC0
DPC_MUX_PC1
DPC_MUX_PI0
DPC_MUX_REXT
R385
4.99K_0402_1%
DPC_MUX_CEXT
C462
2.2U_0402_6.3V6M
HDMI_DONGLE_DETECT
210mA
+3V
R382
0_0603_5%
C449
C435
C436
C437
C438
C439
C450
10U_0603_10V
1U_0402_10V6K
0.1U_0402_25V6
+5V
R386
R387
4.7K_0402_5%
DPC_DDC_EN
DPC_DDC_EN_R
Q6A
Q6B
AO5804EL_SC89-6
R388
R389
R390
R391
R392
R393
R394
R397
R398
R399
R400
R401
R395
R396
Q7A
Q7B
C599
0.01U_0402_25V7K
GPU_DPC_AUX_DN_SDA
GPU_DPC_AUX_DP_SCL
R402
R403
GPU_DPC_SDA
GPU_DPC_SCL

CAD Note: EDP_MUX_PD
Chip power down,active Hi
Internal pull down at ~150kΩ, 3.3V I/O.
L=Normal operation(default)
H=Chip power down

CAD Note: DISPLAY_MUX_SW
Port switchiing control configuration;
Internal pull down at ~150kΩ, 3.3V I/O.
L=Input Port 1(CPU) selected(default)
H=Input Port 2(dGPU) selected

CAD Note: HDMI_DONGLE_DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED

CAD Note:
Internal pull down at ~150kΩ, 3.3V I/O.

DPC_MUX_IN*_AEQ#:
Automatic EQ disable
L:Automatic EQ enable(Default)
H:Automatic EQ disable

DPC_MUX_IN*_PEQ#:
Programmable input equalization levels
L:LEQ, compensate channel loss up to 11.5dB @ HBR2(Default)
H:HEQ, compensate channel loss up to 14.5dB @ HBR2
M:LLEQ, compensate channel loss up to 8.5dB @ HBR2

DPC_MUX_PC0:
AUX interception disable for port 1 and 2
L:AUX interception enable,driver confirguration is set by link trainning(Default)
H:AUX interception disalbe,driver output with fixed 800mV and 0dB
M:AUX interception disalbe,driver output with fixed 400mV and 0dB

DPC_MUX_PC1:
Output swing adjustment for port 1 and 2
L:Default
H:+20%
M:-16.7%

DPC_MUX_PI0:
Auto test inable
L:Auto test disable & input offset cancellation enable(Default)
H:Auto test enable & input offset cancellation enable
M:Auto test disable & input offset cancellation disable

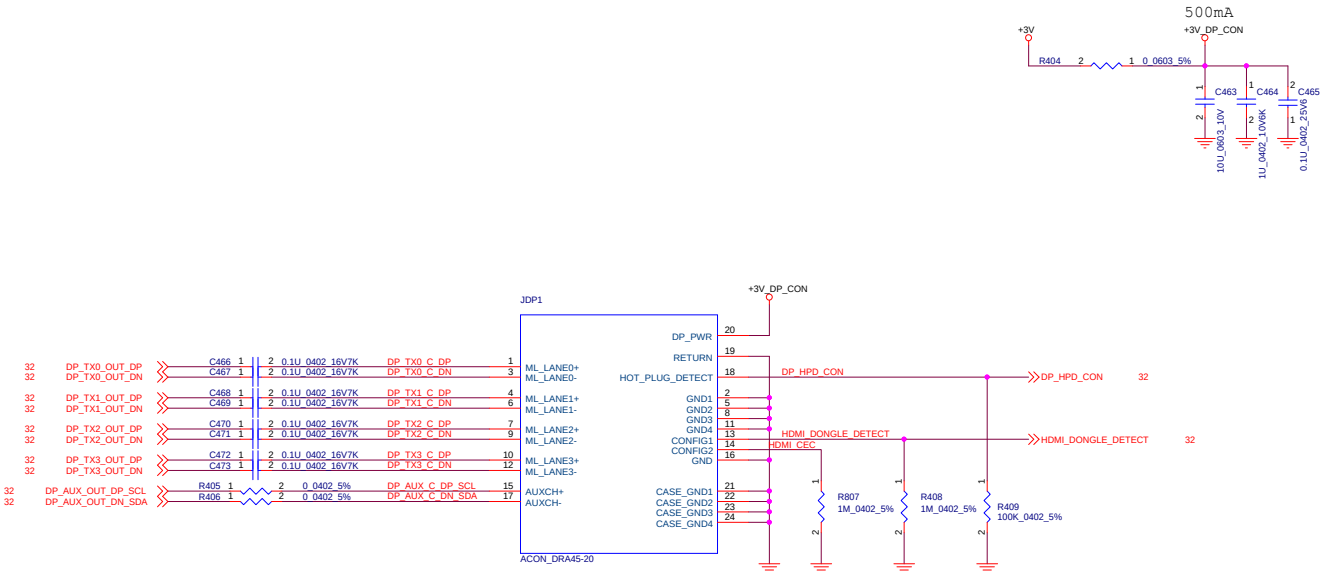
lenovo联想 LENOVO.CRDN

Title: DP MUX

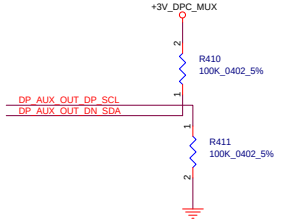
Size: C | Document Number: Skylake-H | Rev: V0.3

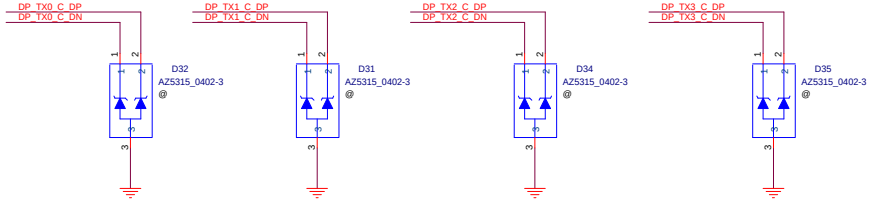
Date: Wednesday, January 27, 2016 | Sheet 32 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

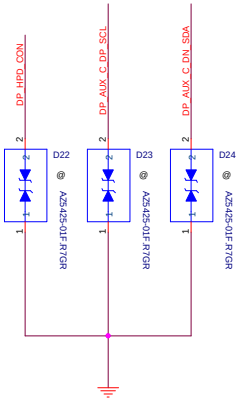


CAD Note: HDMI_DONGLE_DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED





CAD Note: Reserve for ESD



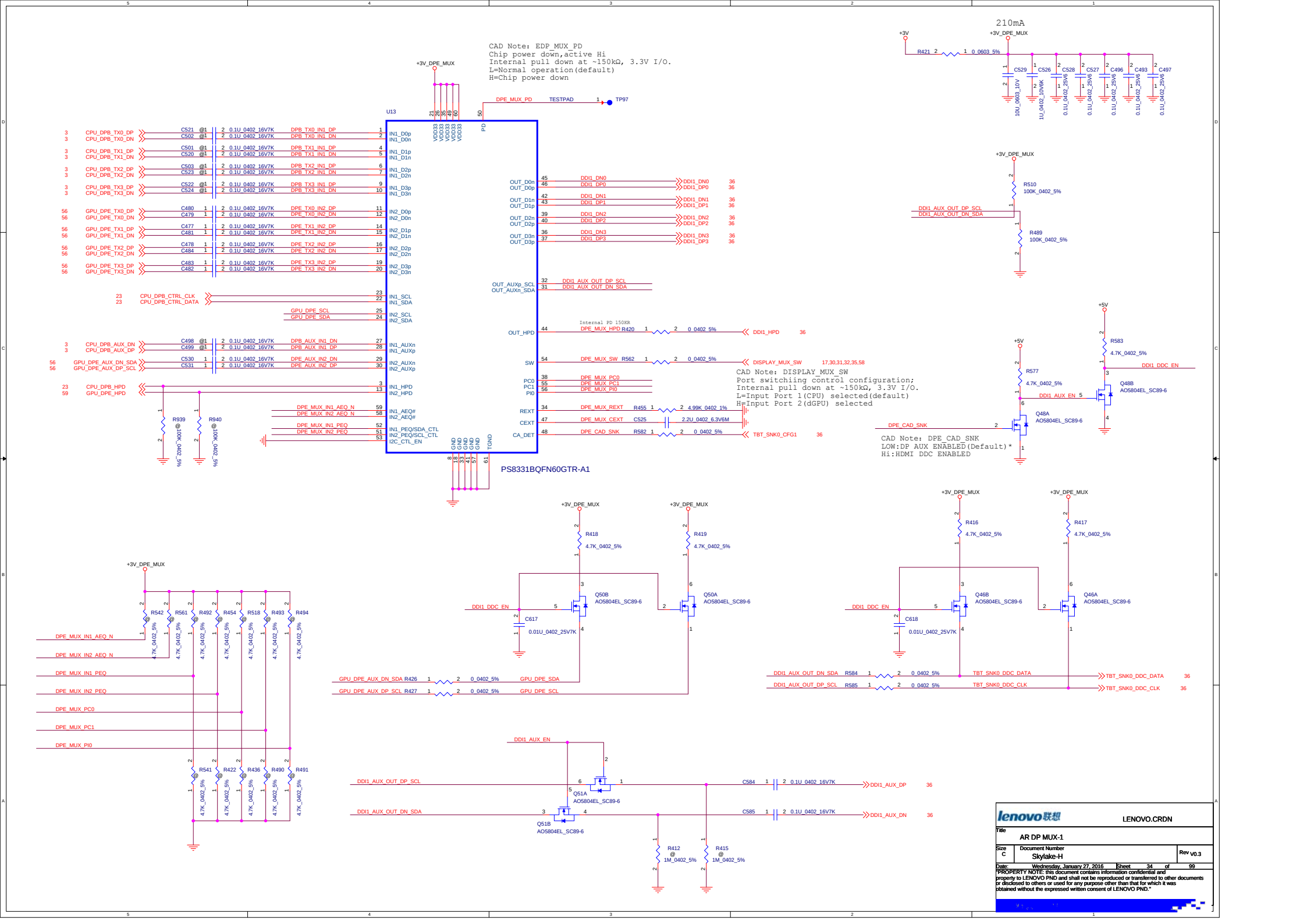
lenovo联想 LENOVO.CRDN

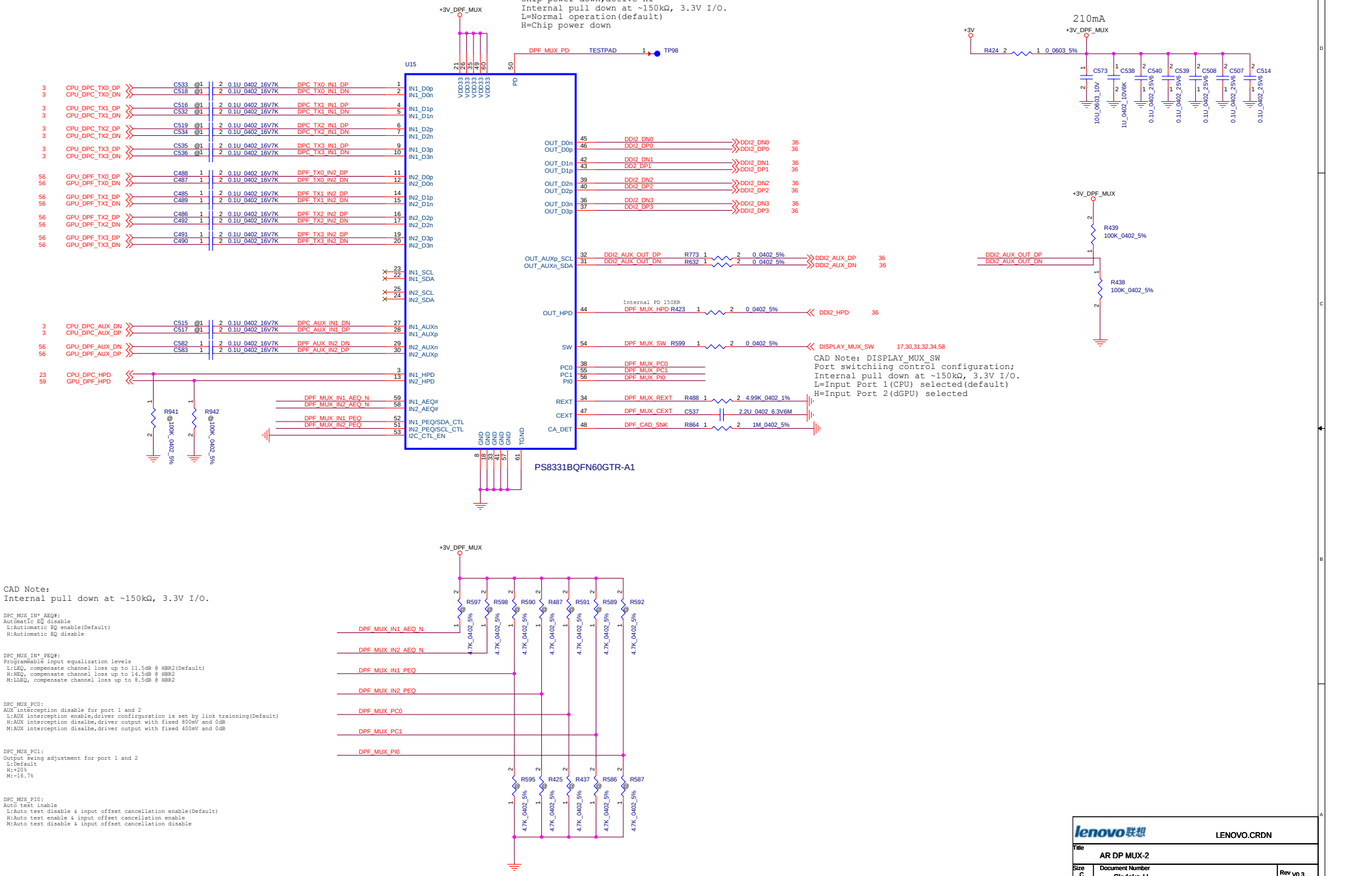
Title: DISPLAY PORT

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 33 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


210mA
CAD Note: EDP_MUX_PD
Chip power down,active Hi
Internal pull down at ~150kΩ, 3.3V I/O.
L=Normal operation(default)
H=Chip power down
U13
PS8331BQFN60GTR-A1
CAD Note: DISPLAY_MUX_SW
Port switchiing control configuration;
Internal pull down at ~150kΩ, 3.3V I/O.
L=Input Port 1(CPU) selected(default)
H=Input Port 2(dGPU) selected
CAD Note: DPE_CAD_SNK
LOW:DP AUX ENABLED(Default)*
Hi:HDMI DDC ENABLED
lenovo联想
LENOVO.CRDN
AR DP MUX-1
Skylake-H
Rev V0.3
Wednesday, January 27, 2016
Sheet 34 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

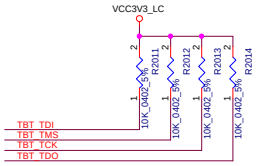


lenovo联想		LENOVO.CRDN	
Title	AR DP MUX-2		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 35 of 99		

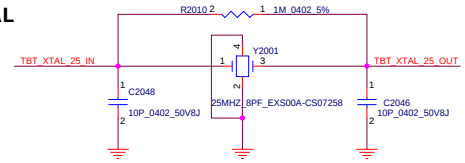
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

AR-DP TYPE C +USB 3.1 (3.0)

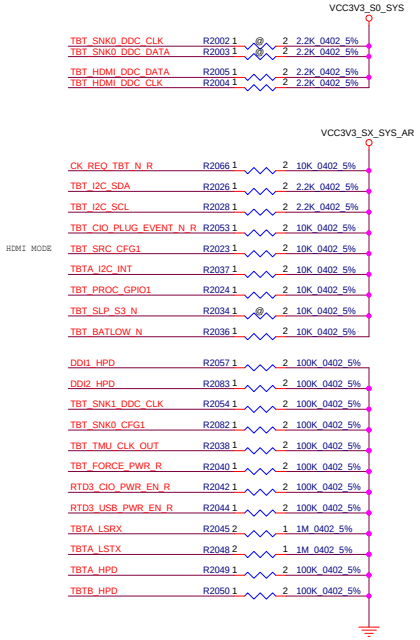
JTAG



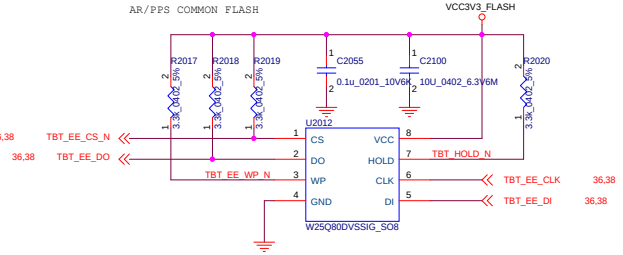
XTAL

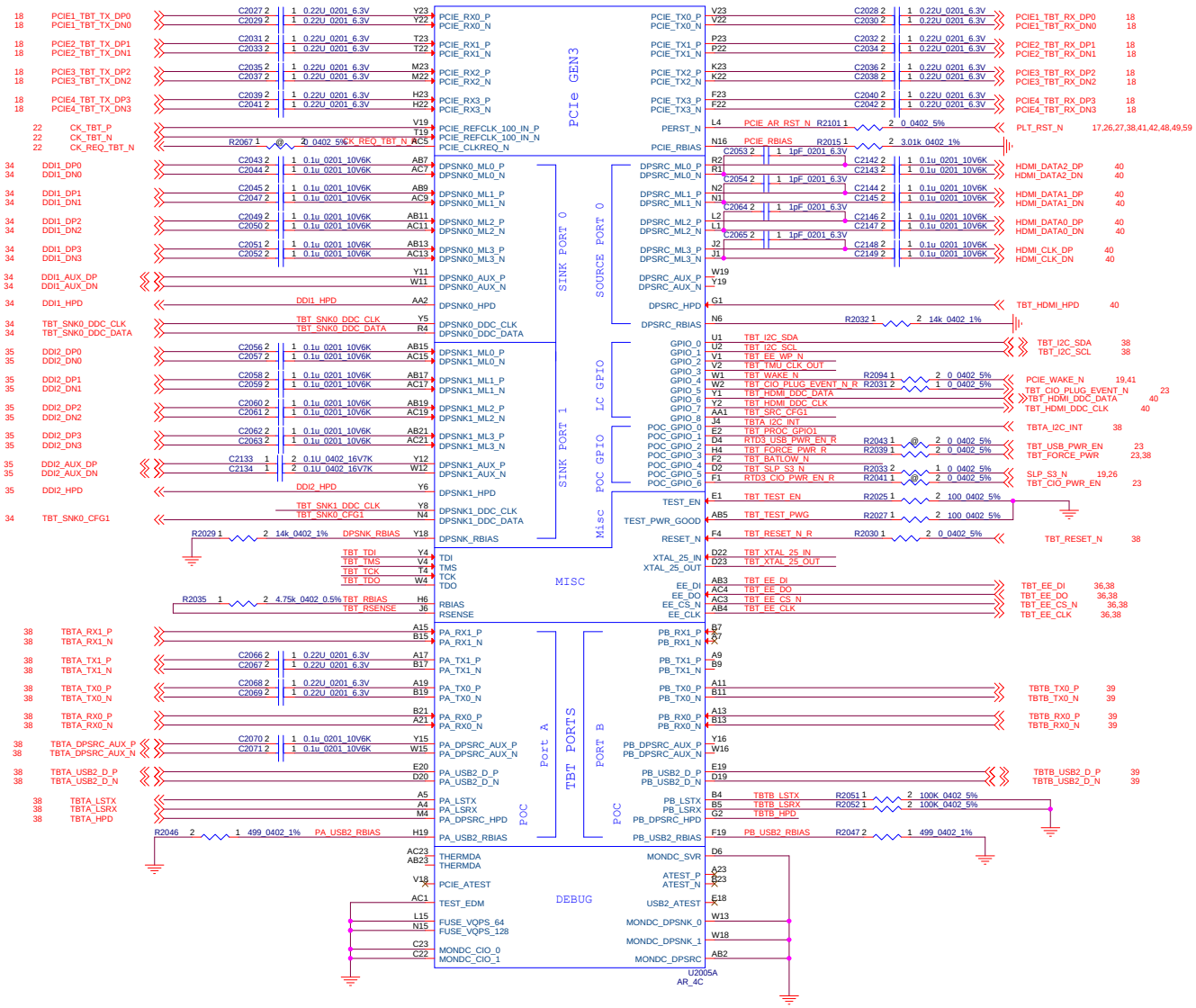


GPIO



ROM





IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

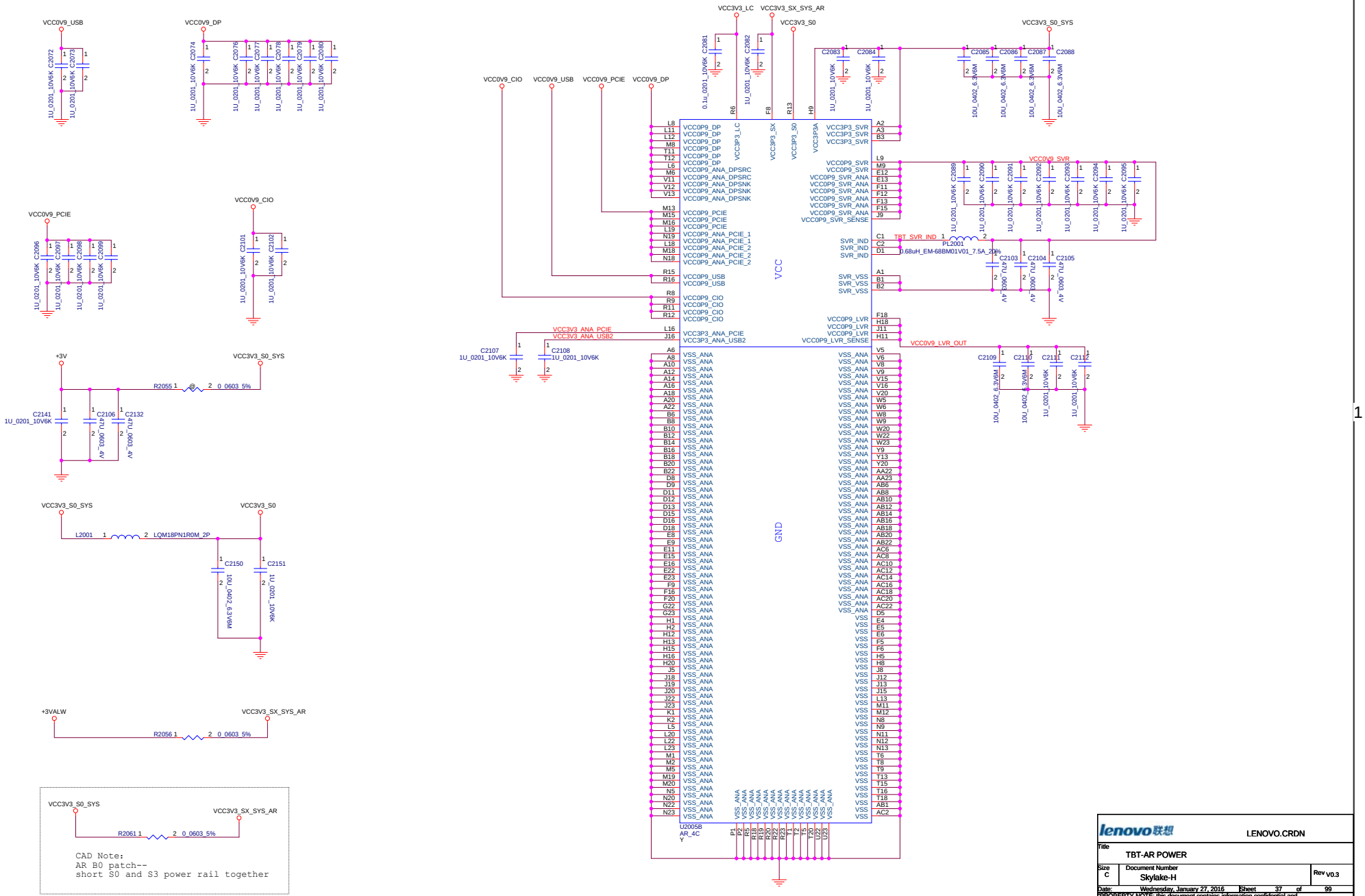
lenovo联想 LENOVO.CRDN

Title: DDI redriver PS8330

Size: C | Document Number: Skylake-H | Rev V0.3

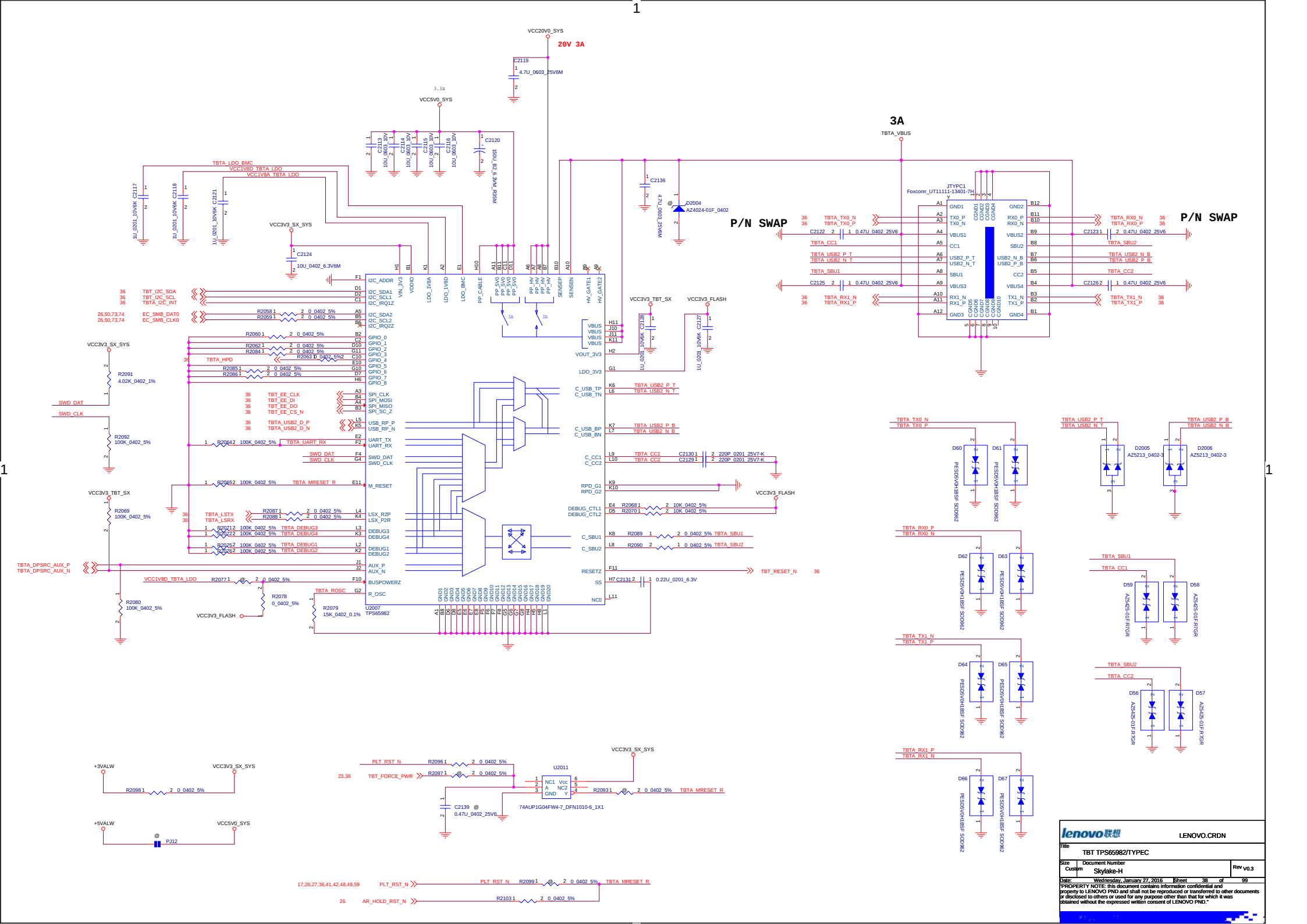
Date: Wednesday, January 27, 2016 | Sheet 36 of 99

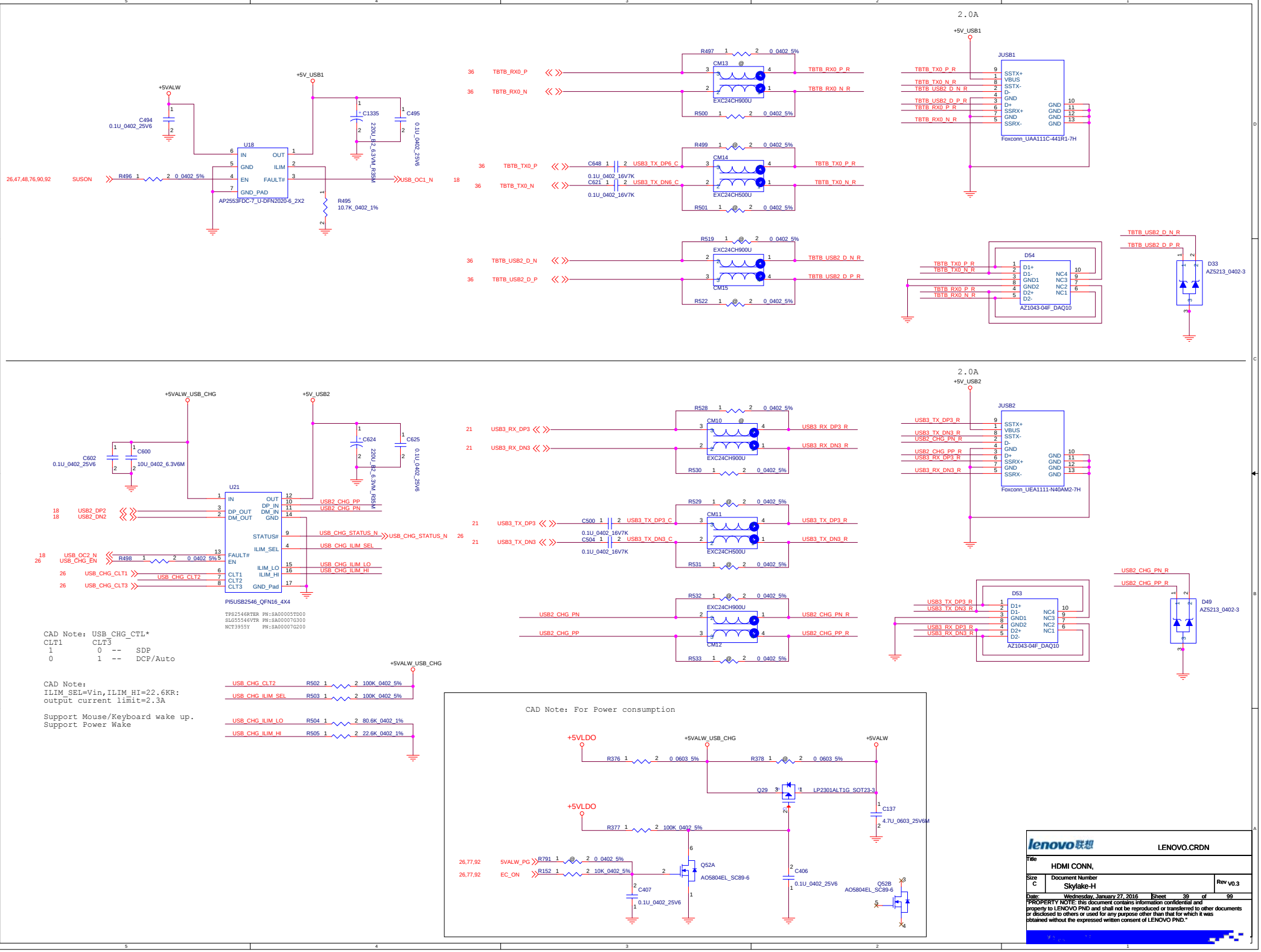
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

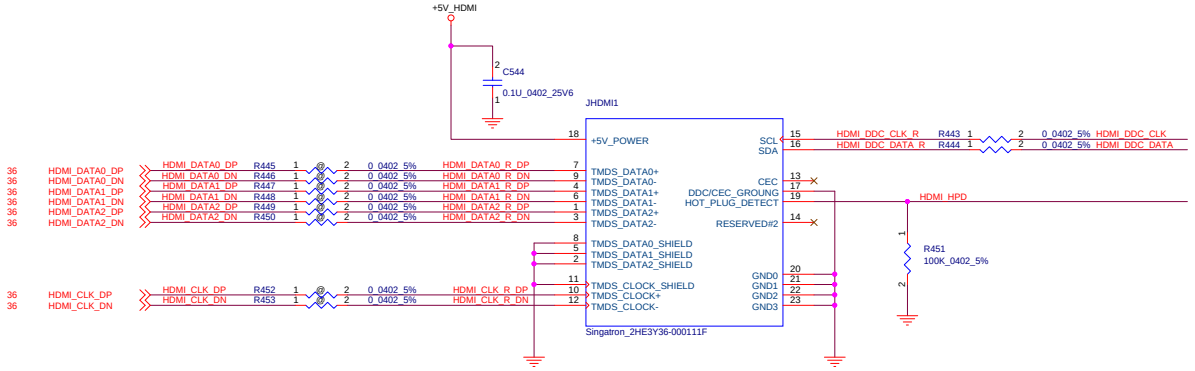


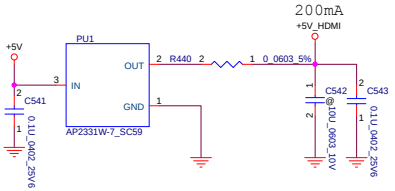
lenovo联想	LENOVO.CRDN	
Title: TBT-AR POWER		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 37 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


VCC20V0_SYS
20V 3A
C2119
4.7U_0603_25V6M
VCC5V0_SYS
3.3A
C2113 10U_0603_10V
C2114 10U_0603_10V
C2115 10U_0603_10V
C2116 10U_0603_10V
C2120 150U_D2_6.3VM_R45M
C2136 4.7U_0603_25V6M
D2004 AZ4024-01F_0402
3A
TBTA_VBUS
P/N SWAP
P/N SWAP
JTYPC1
Foxconn_UT11111-13401-7H
TBTA_LDO_BMC
VCC1V8D_TBTA_LDO
VCC1V8A_TBTA_LDO
C2117 1U_0201_10V6K
C2118 1U_0201_10V6K
C2121 1U_0201_10V6K
VCC3V3_SX_SYS
C2124 10U_0402_6.3V6M
I2C_ADDR
I2C_SDA1
I2C_SCL1
I2C_IRQ1Z
I2C_SDA2
I2C_SCL2
I2C_IRQ2Z
TBT_I2C_SDA
TBT_I2C_SCL
TBTA_I2C_INT
EC_SMB_DAT0
EC_SMB_CLK0
R2058 R2059 2_0_0402_5%
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
TBTA_HPD
R2060 R2062 R2084 R2063 R2085 R2086
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SC_Z
TBT_EE_CLK
TBT_EE_DI
TBT_EE_DO
TBT_EE_CS_N
USB_RP_P
USB_RP_N
TBTA_USB2_D_P
TBTA_USB2_D_N
UART_TX
UART_RX
TBTA_UART_RX
R20642 100K_0402_5%
SWD_DAT
SWD_CLK
M_RESET
TBTA_MRESET_R
R20652 100K_0402_5%
LSX_R2P
LSX_P2R
TBTA_LSTX
TBTA_LSRX
R20871 R20881 2_0_0402_5%
DEBUG3
DEBUG4
DEBUG1
DEBUG2
TBTA_DEBUG3
TBTA_DEBUG4
TBTA_DEBUG1
TBTA_DEBUG2
R20712 R20722 R20752 R20762 100K_0402_5%
AUX_P
AUX_N
TBTA_DPSRC_AUX_P
TBTA_DPSRC_AUX_N
BUSPOWERZ
R20771 @ 2_0_0402_5%
R2078 0_0402_5%
R2080 100K_0402_5%
R2069 100K_0402_5%
R2091 4.02K_0402_1%
R2092 100K_0402_5%
R_OSC
TBTA_ROSC
R2079 15K_0402_0.1%
U2007 TPS65982
VOUT_3V3
LDO_3V3
C2128 1U_0201_10V6K
C2127 1U_0201_10V6K
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
TBTA_USB2_P_T
TBTA_USB2_N_T
TBTA_USB2_P_B
TBTA_USB2_N_B
C_CC1
C_CC2
TBTA_CC1
TBTA_CC2
C2130 C2129 2_220P_0201_25V7-K
RPD_G1
RPD_G2
DEBUG_CTL1
DEBUG_CTL2
R2068 R2070 2_10K_0402_5%
C_SBU1
C_SBU2
TBTA_SBU1
TBTA_SBU2
R2089 R2090 2_0_0402_5%
RESETZ
TBT_RESET_N
SS
C2131 0.22U_0201_6.3V
NC0
TBTA_TX0_N
TBTA_TX0_P
TBTA_RX0_N
TBTA_RX0_P
TBTA_CC1
TBTA_SBU2
TBTA_USB2_N_B
TBTA_USB2_P_B
TBTA_CC2
TBTA_RX1_N
TBTA_RX1_P
TBTA_TX1_N
TBTA_TX1_P
C2122 C2123 C2125 C2126 2_1_0.47U_0402_25V6
D60 D61 D62 D63 D64 D65 D66 D67
PESD5V0H1BSF SOD962
D2005 D2006
AZ5213_0402-3
D58 D59
AZ5425-01F.R7GR
D56 D57
AZ5425-01F.R7GR
+3VALW
+5VALW
VCC3V3_SX_SYS
VCC5V0_SYS
R2098 2_0_0402_5%
PJ12
PLT_RST_N
TBT_FORCE_PWR
R2096 R2097 2_0_0402_5%
U2011
74AUP1G04FW4-7_DFN1010-6_1X1
C2139 @ 0.47U_0402_25V6
R2093 @ 2_0_0402_5%
TBTA_MRESET_R
17,26,27,36,41,42,48,49,59
PLT_RST_N
R2099 @ 2_0_0402_5%
26
AR_HOLD_RST_N
R2103 2_0_0402_5%
LENOVO.CRDN
TBT TPS65982/TYPEC
Custom
Skylake-H
Rev v0.3
Wednesday, January 27, 2016
Sheet 38 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


2.0A
+5V_USB1
+5VALW
U18
AP2553FDC-7_U-DFN2020-6_2X2
JUSB1
Foxconn_UAA111C-441R1-7H
D54
AZ1043-04F_DAQ10
D33
AZ5213_0402-3
+5VALW_USB_CHG
+5V_USB2
U21
PI5USB2546_QFN16_4X4
JUSB2
Foxconn_UEA1111-N40AM2-7H
D53
D49
CAD Note: USB_CHG_CTL*
CLT1 CLT3
1 0 -- SDP
0 1 -- DCP/Auto
CAD Note:
ILIM_SEL=Vin,ILIM_HI=22.6KR:
output current limit=2.3A
Support Mouse/Keyboard wake up.
Support Power Wake
CAD Note: For Power consumption
+5VLDO
Q52A
AO5804EL_SC89-6
Q52B
Q29
LP2301ALT1G_SOT23-3
LENOVO.CRDN
HDMI CONN,
Skylake-H
Rev V0.3
Wednesday, January 27, 2016
Sheet 39 of 99

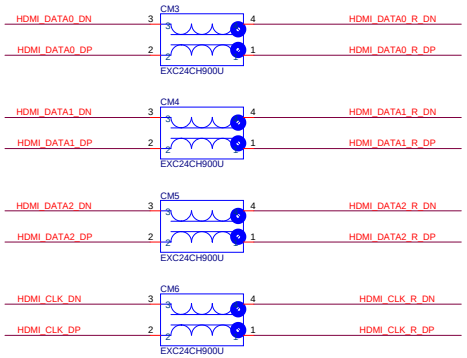




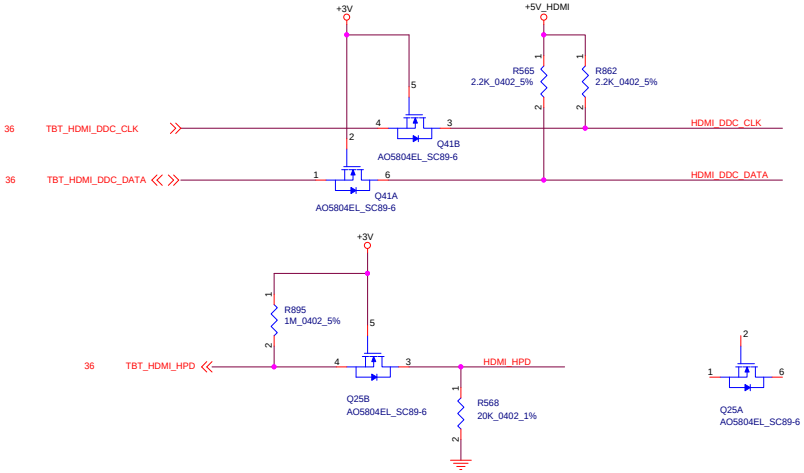
CM

BRD Note: Co-lay with R

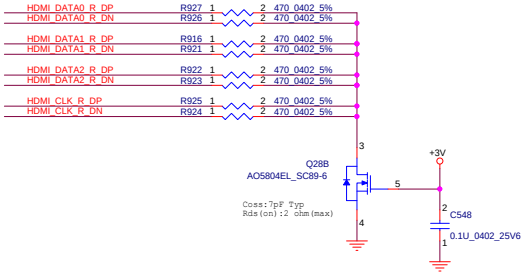
CAD Note: Reserve for EMI



LS

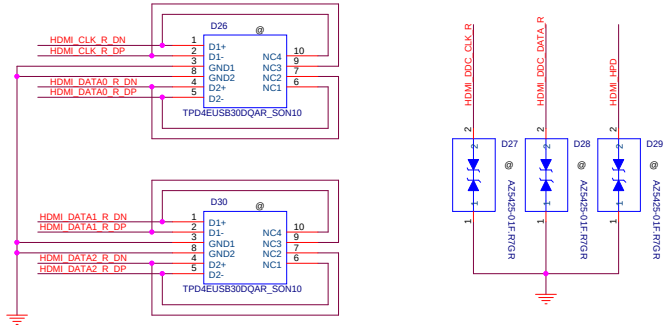


CRLS



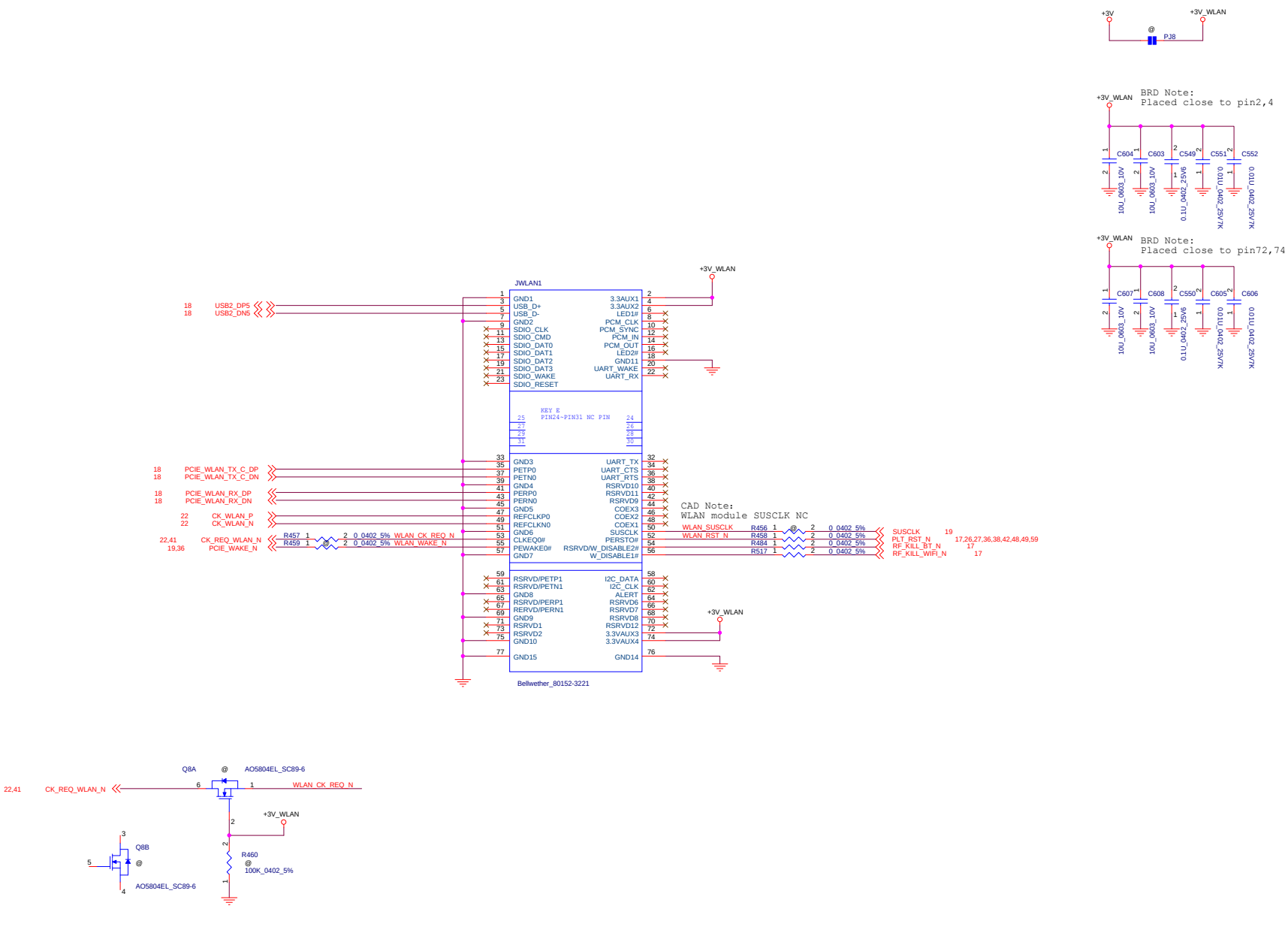
ESD

CAD Note: Reserve for ESD



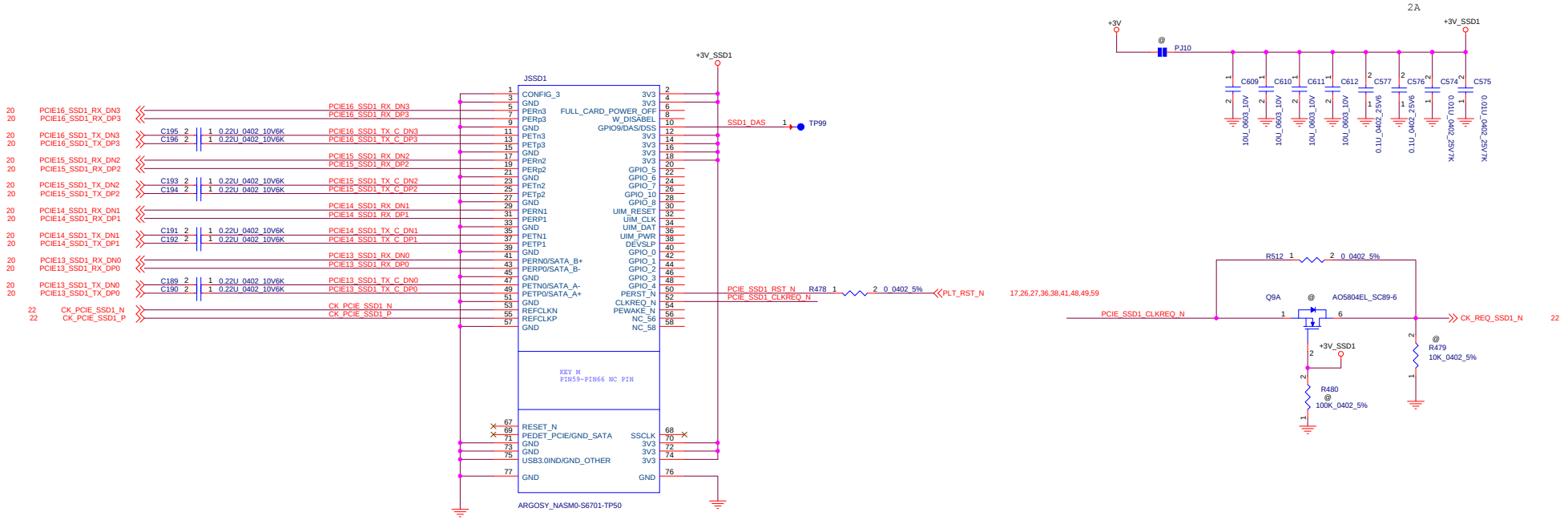
lenovo联想	LENOVO.CRDN	
Title: HDMI CONN,		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 40 of 99	

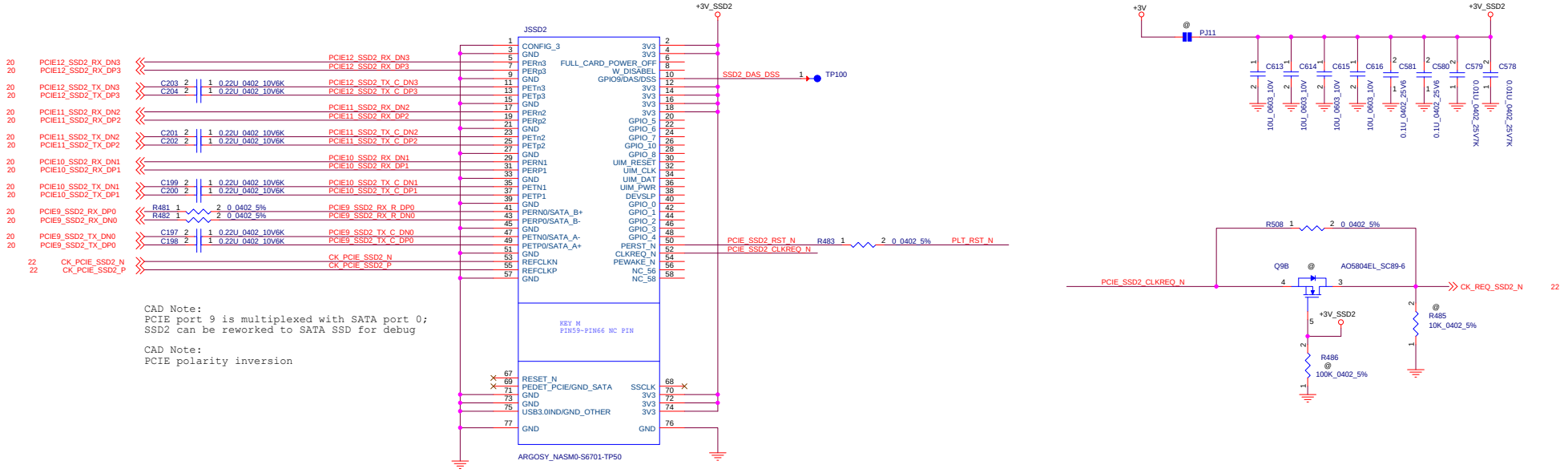
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN	
Title: NGFF WLAN		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 41 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."





CAD Note:
PCIE port 9 is multiplexed with SATA port 0;
SSD2 can be reworked to SATA SSD for debug

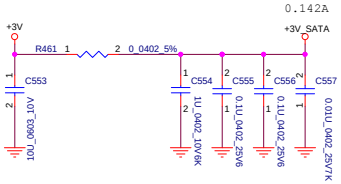
CAD Note:
PCIE polarity inversion

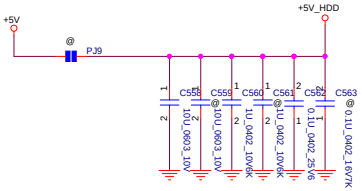
Title	NGFF SSD
Size	C
Document Number	Skylake-H
Rev	V0.3
Date:	Wednesday, January 27, 2016
Sheet	42 of 99

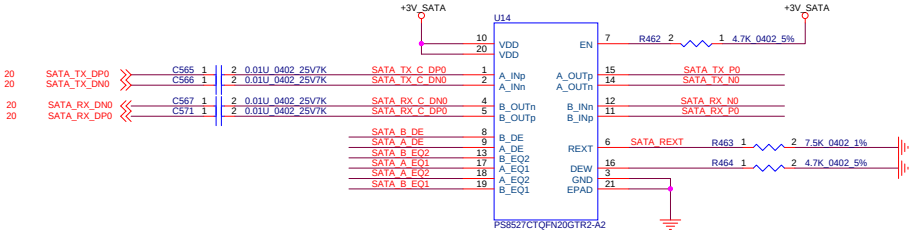
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

CAD Note: PS8527A VDD
1.2V/1.35V/1.5V

0.142A



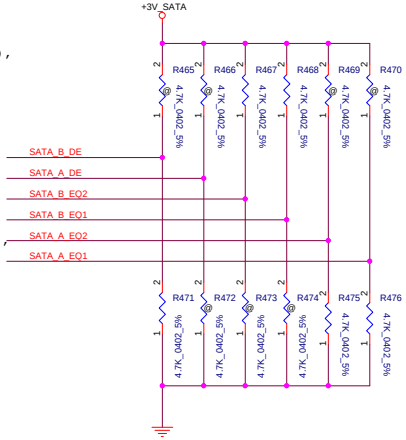




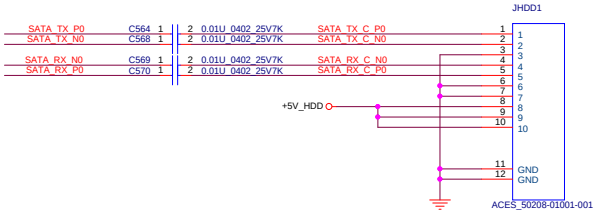
CAD Note:
SATA_REXT=7.5KR:
Vtx_diff=700 mV

CAD Note: SATA_DEW
L:For SATA Gen3
H:For SATA Gen2

CAD Note: SATA_x_DE
De-emphasis level setting for channel x(x=A,B),
internally tied to VDD/2
[A_DE,B_DE]=M,L
M:-3.5dB
L: 0dB
H: -6dB



CAD Note: SATA_x_EQ
Equalization level setting for channel x(x=A,B),
internally tied to VDD/2
[x_EQ2,x_EQ1]=
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB(CH A)
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB(CH B)



lenovo联想 LENOVO.CRDN

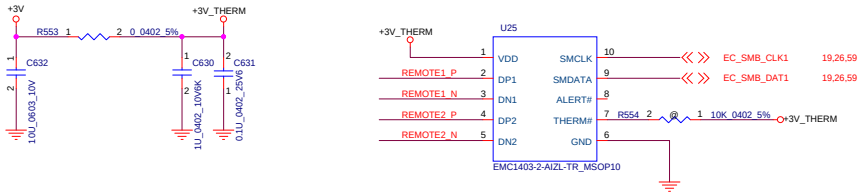
Title: SATA HDD

Size	Document Number	Rev
C	Skylake-H	V0.3

Date: Wednesday, January 27, 2016 Sheet 43 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

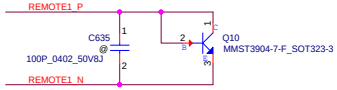
Theamal Sensor



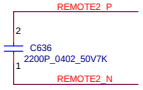
SMBus ADDRESS:0x 1001_101x

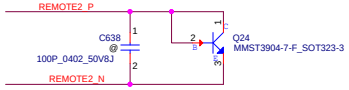
BRD Note:
Placed close to EMC1403

BRD Note:
Placed close to DDR
W/S=10:10



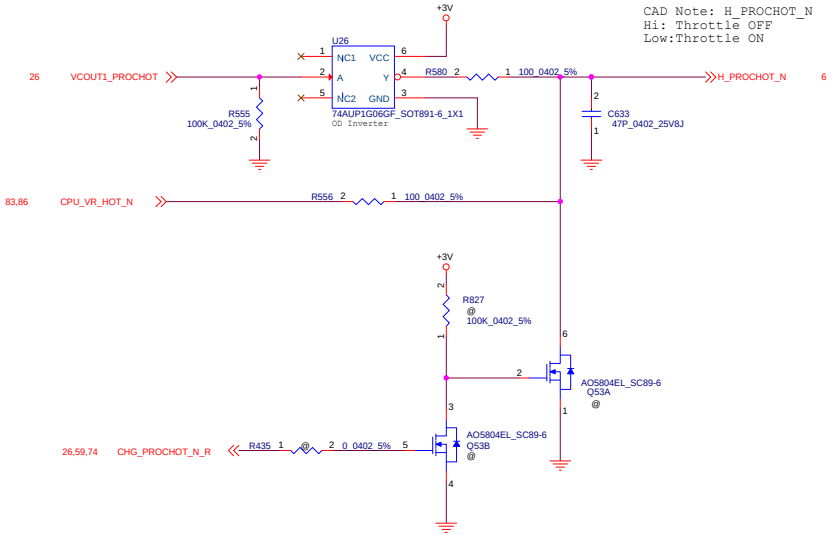
BRD Note:
Placed close to FAN



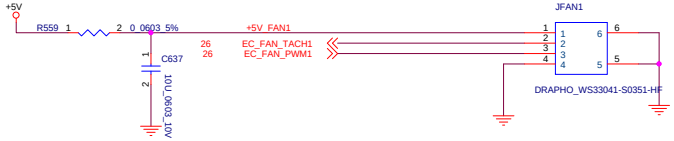


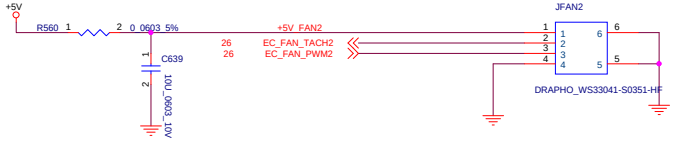
PROCHOT_N Logic

CAD Note: H_PROCHOT_N
Hi: Throttle OFF
Low:Throttle ON

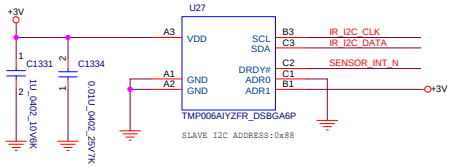


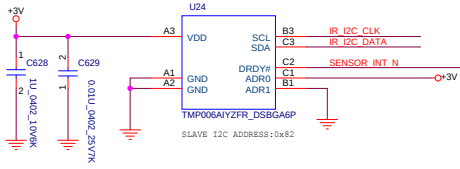
FAN CONN.

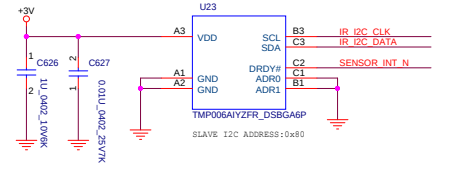


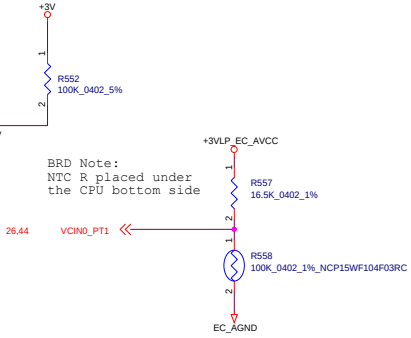


IR Sensor

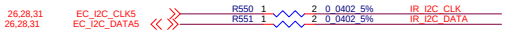








BRD Note:
NTC R placed under
the CPU bottom side



lenovo联想 LENOVO.CRDN

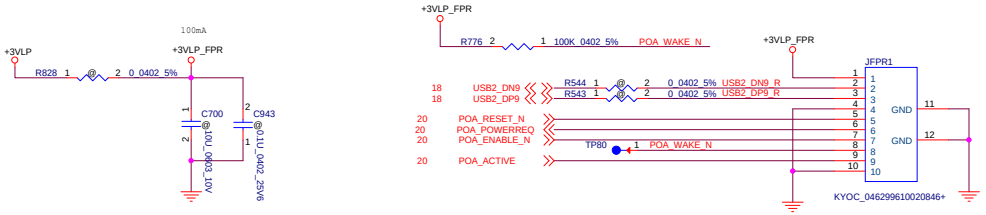
Title: Thermal/IR Sensor/FAN

Size	Document Number	Rev
C	Skylake-H	V0.3

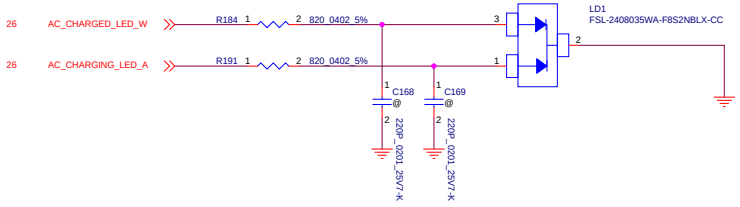
Date: Wednesday, January 27, 2016 Sheet 44 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

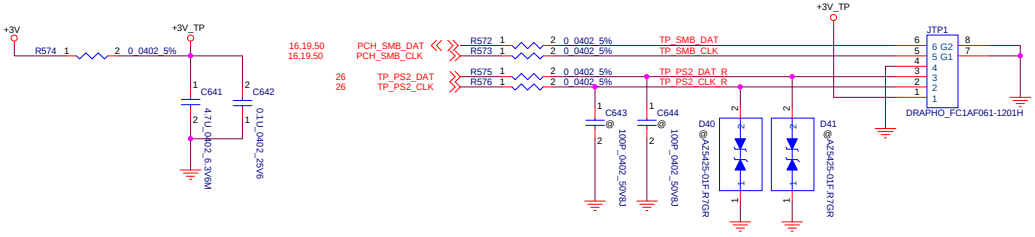
FPR CONN.



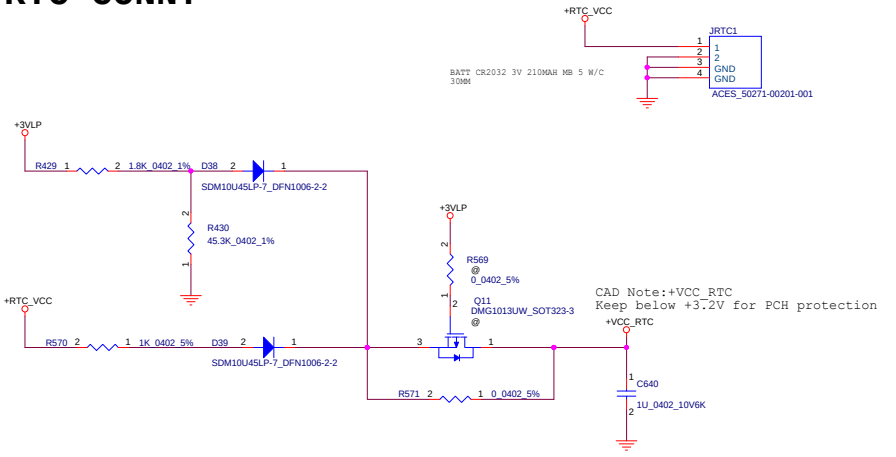
AC Charge LED



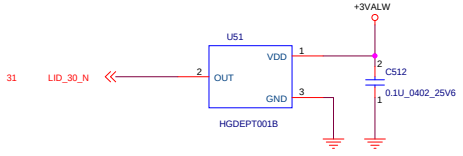
Touch Pad



RTC CONN.

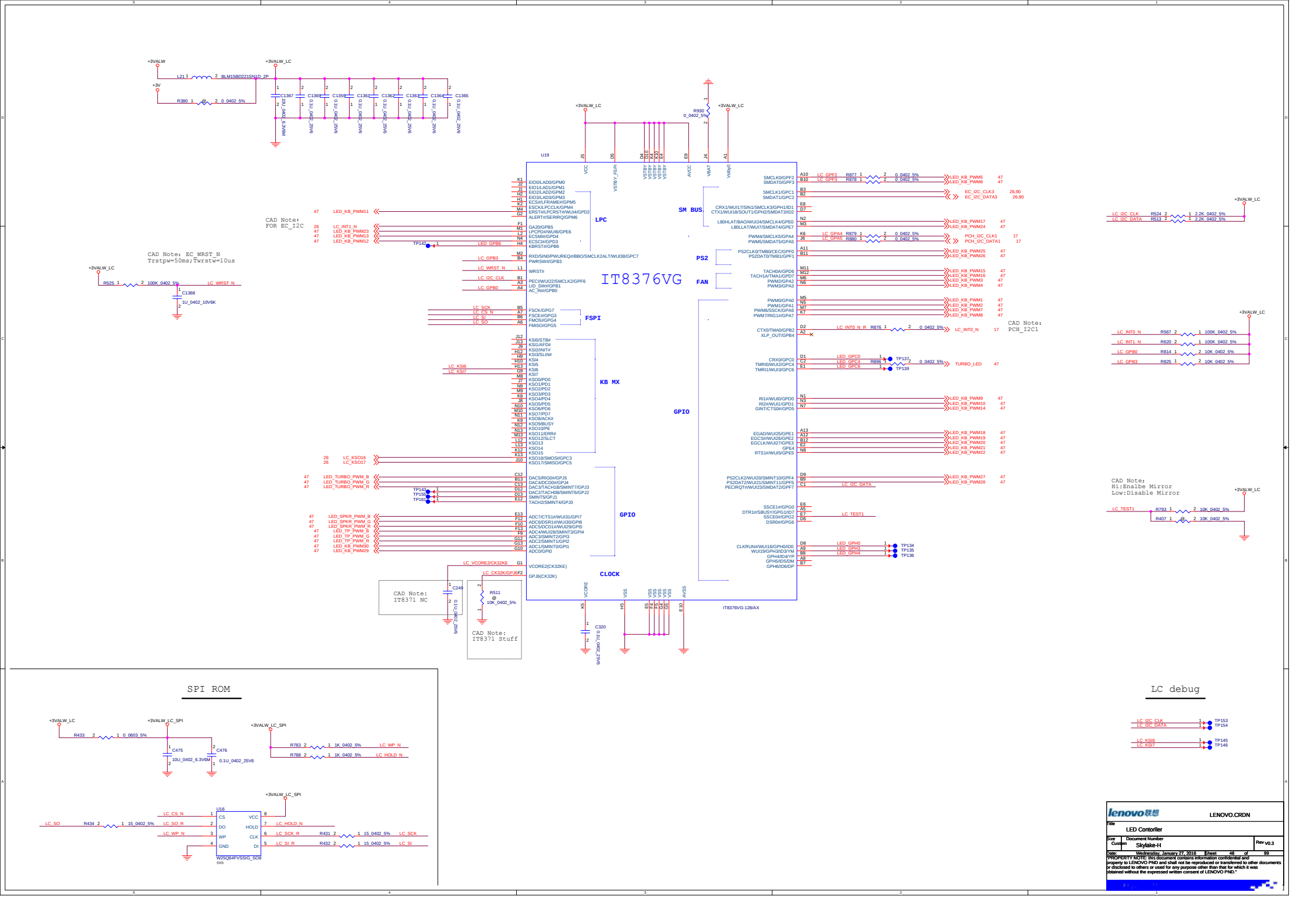


LID

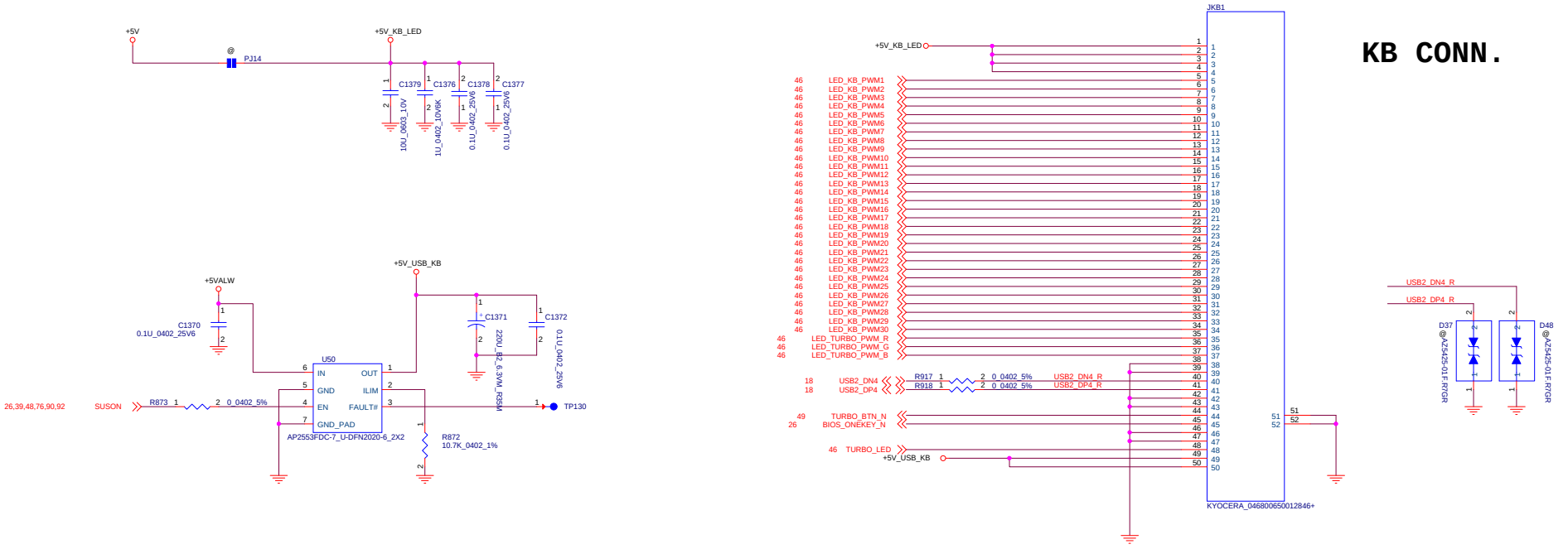


lenovo联想	LENOVO.CRDN	
Title	TP/FPR/RTC/LED CONN	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 45 of 99	

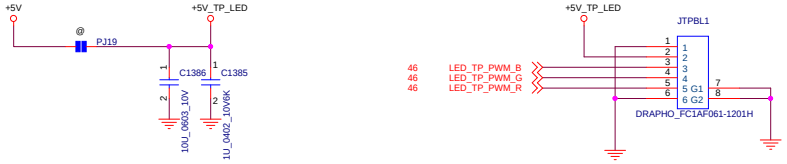
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


IT8376VG
U19
IT8376VG-128/AX
LPC
SM BUS
PS2
FAN
FSPI
KB MX
GPIO
GPIO
CLOCK
CAD Note:
FOR EC_I2C
CAD Note: EC_WRST_N
Trstpw=50ms;Twrstw=10us
CAD Note:
IT8371 NC
CAD Note:
IT8371 Stuff
CAD Note:
PCH_I2C1
CAD Note:
Hi:Enalbe Mirror
Low:Disable Mirror
SPI ROM
LC debug
W25Q64FVSSIG_SO8
LENOVO.CRDN
LED Contorller
Skylake-H
Rev V0.3
Wednesday, January 27, 2016
46
99

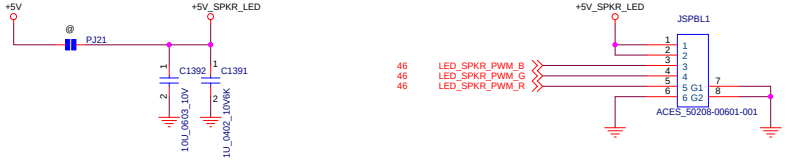
KB CONN.



TP LED CONN.

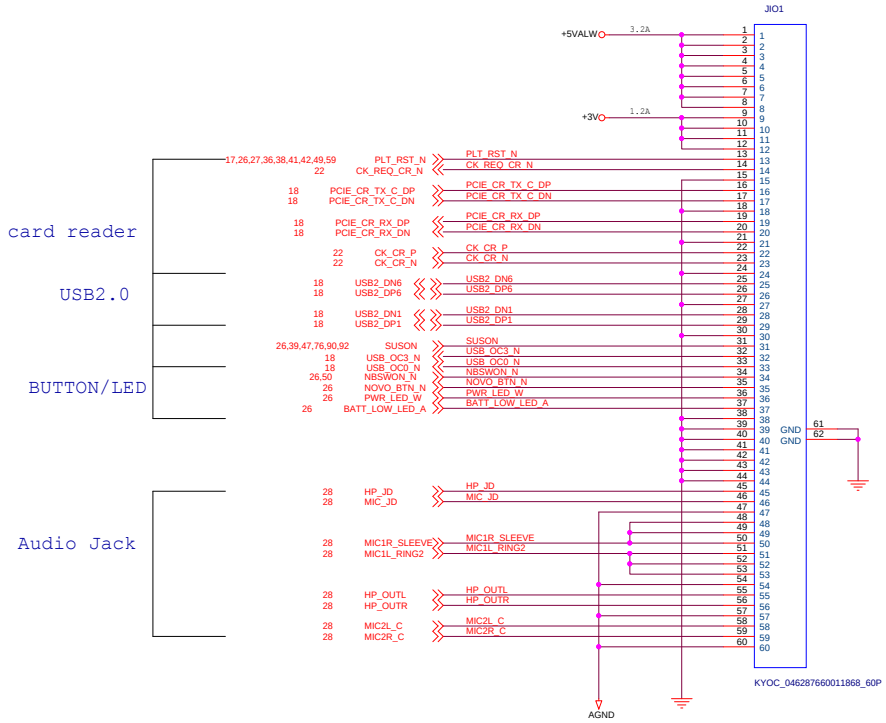


SPKR LED CONN.



lenovo联想	LENOVO.CRDN	
Title: KB/BACKLIGHT LED		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 47 of 99	

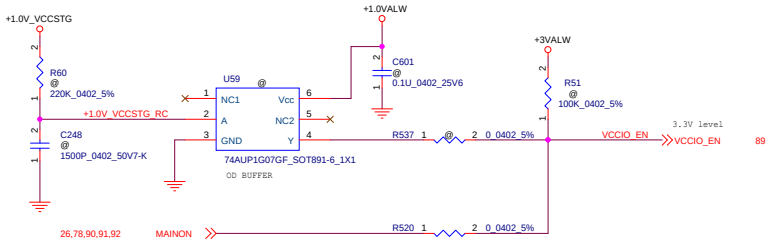
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



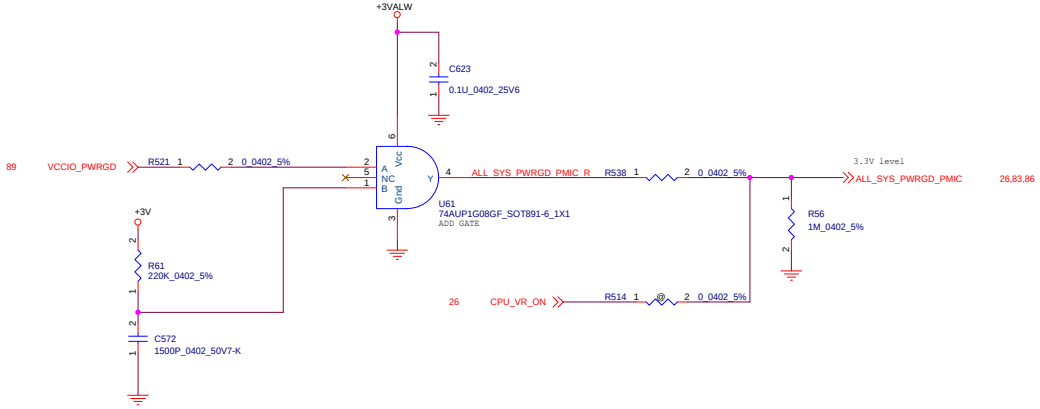
lenovo联想	LENOVO.CRDN	
Title: IO BTB Conn		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 48 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

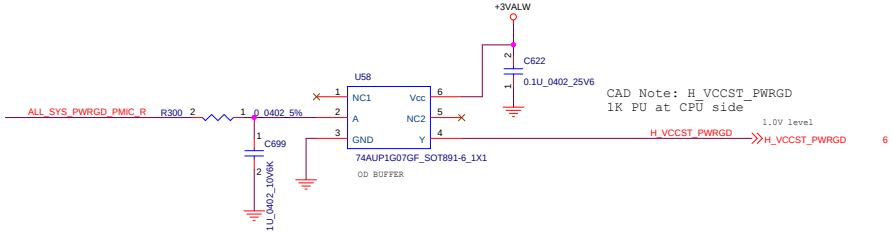
VCCIO_EN



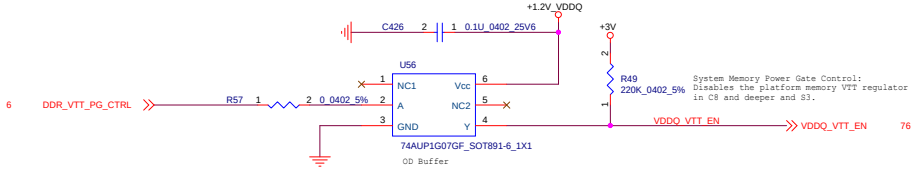
ALL_SYS_PWRGD_PMIC



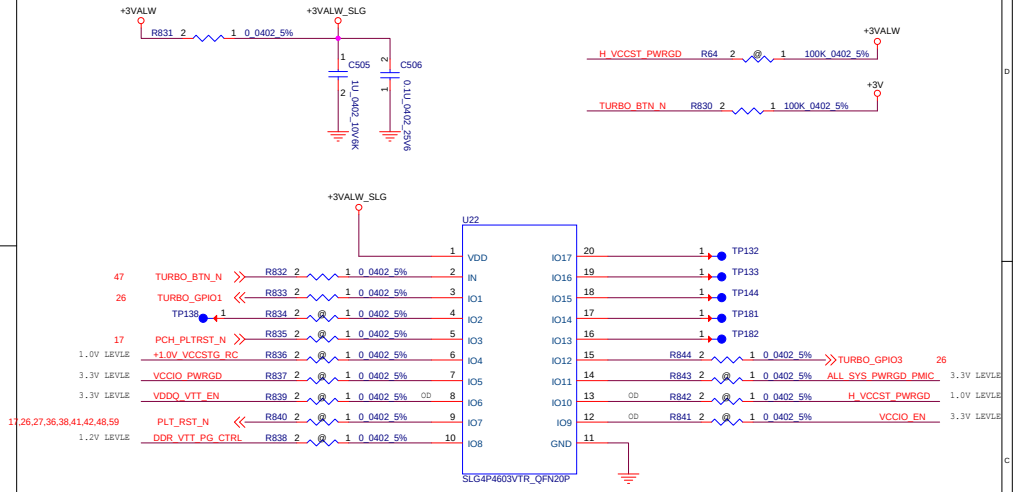
H_VCCST_PWRGD



VDDQ_VTT_EN



SLG4P4603VTR



lenovo联想 LENOVO.CRDN

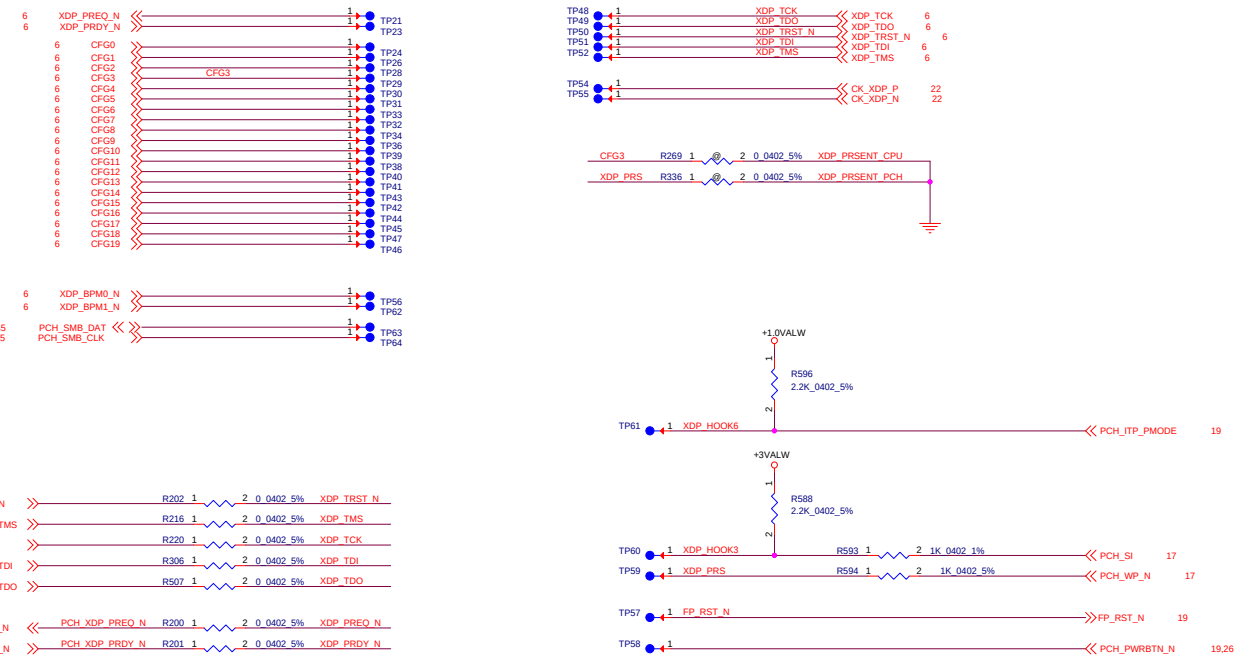
Title: PWRGD CONTROL

Size	Document Number	Rev
C	Skylake-H	V0.3

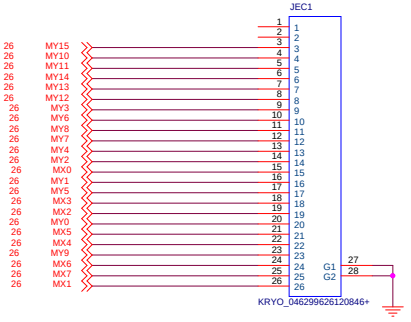
Date: Wednesday, January 27, 2016 Sheet 49 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

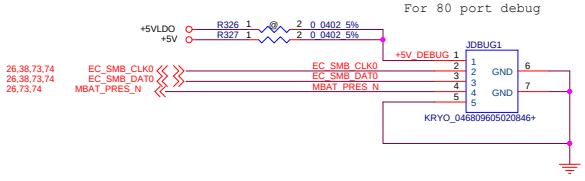
XDP CONN.



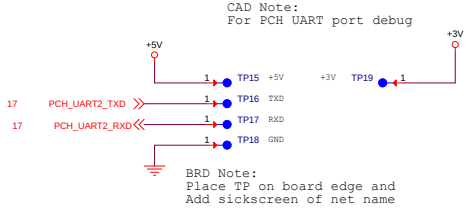
EC Debug CONN.



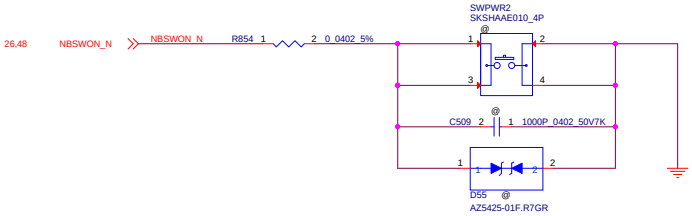
80 Port Debug CONN.



PCH UART Debug CONN.

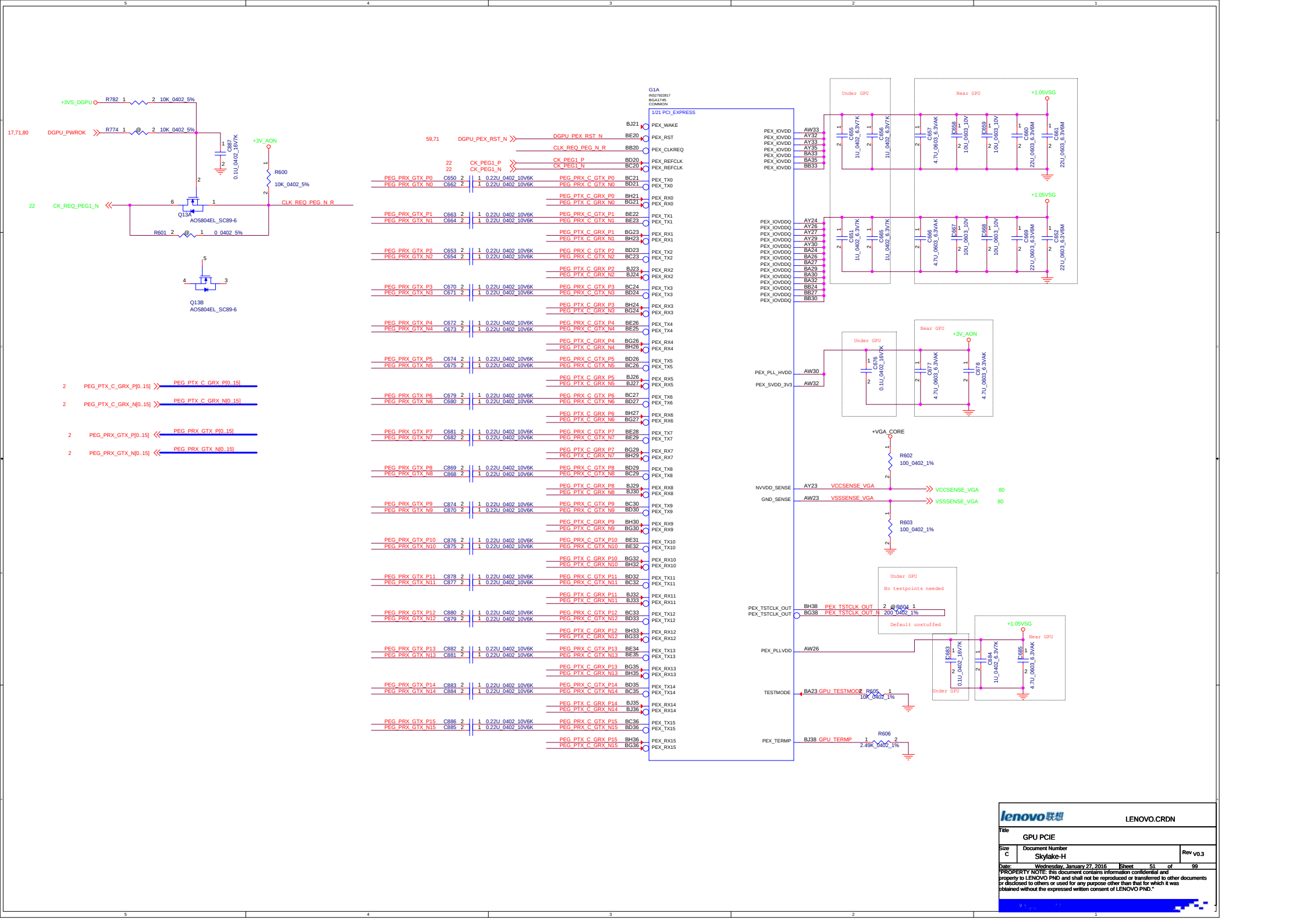


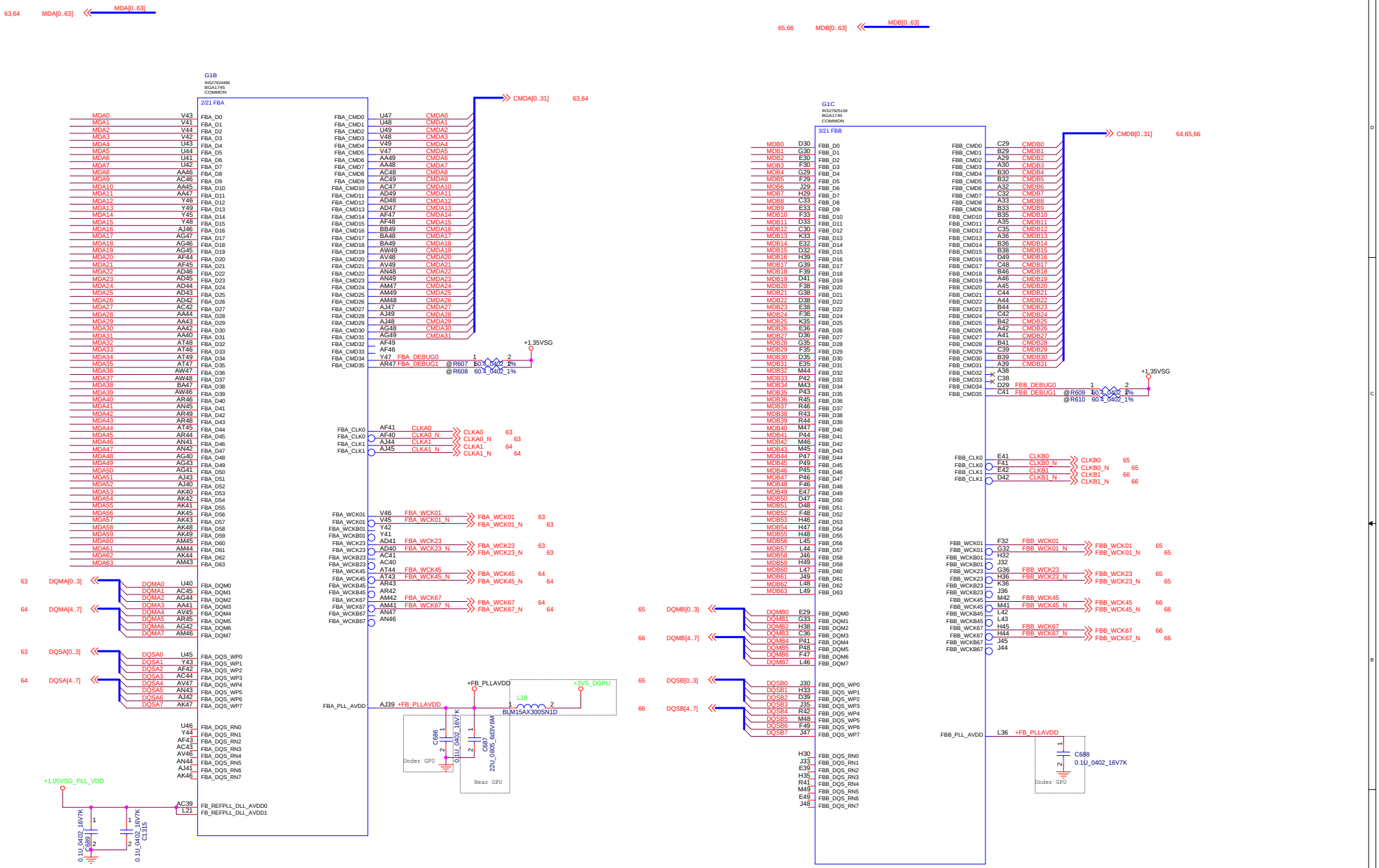
MB PWRBTN



lenovo联想	LENOVO.CRDN	
Title	XDP/DEBUG	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 50 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


+3VS_DGPU
R782 1 2 10K_0402_5%
17,71,80 DGPU_PWROK
R774 1 @ 2 10K_0402_5%
C887 0.1U_0402_16V7K
+3V_AON
R600 10K_0402_5%
22 CK_REQ_PEG1_N
Q13A AO5804EL_SC89-6
CLK_REQ_PEG_N_R
R601 2 @ 1 0_0402_5%
Q13B AO5804EL_SC89-6
2 PEG_PTX_C_GRX_P[0..15]
PEG_PTX_C_GRX_P[0..15]
2 PEG_PTX_C_GRX_N[0..15]
PEG_PTX_C_GRX_N[0..15]
2 PEG_PRX_GTX_P[0..15]
PEG_PRX_GTX_P[0..15]
2 PEG_PRX_GTX_N[0..15]
PEG_PRX_GTX_N[0..15]
G1A
IN527922817
BGA1745
COMMON
1/21 PCI_EXPRESS
59,71 DGPU_PEX_RST_N
22 CK_PEG1_P
22 CK_PEG1_N
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEX_TX0
PEX_RX0
PEX_TX1
PEX_RX1
PEX_TX2
PEX_RX2
PEX_TX3
PEX_RX3
PEX_TX4
PEX_RX4
PEX_TX5
PEX_RX5
PEX_TX6
PEX_RX6
PEX_TX7
PEX_RX7
PEX_TX8
PEX_RX8
PEX_TX9
PEX_RX9
PEX_TX10
PEX_RX10
PEX_TX11
PEX_RX11
PEX_TX12
PEX_RX12
PEX_TX13
PEX_RX13
PEX_TX14
PEX_RX14
PEX_TX15
PEX_RX15
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
NVVDD_SENSE
GND_SENSE
PEX_TSTCLK_OUT
PEX_PLLVDD
TESTMODE
PEX_TERMP
+VGA_CORE
VCCSENSE_VGA
VSSSENSE_VGA
Under GPU
Near GPU
+1.05VSG
+3V_AON
No testpoints needed
Default unstuffed
GPU_TESTMODE
GPU_TERMP
2.49K_0402_1%
LENOVO.CRDN
GPU PCIE
Skylake-H
Rev v0.3
Wednesday, January 27, 2016
Sheet 51 of 99



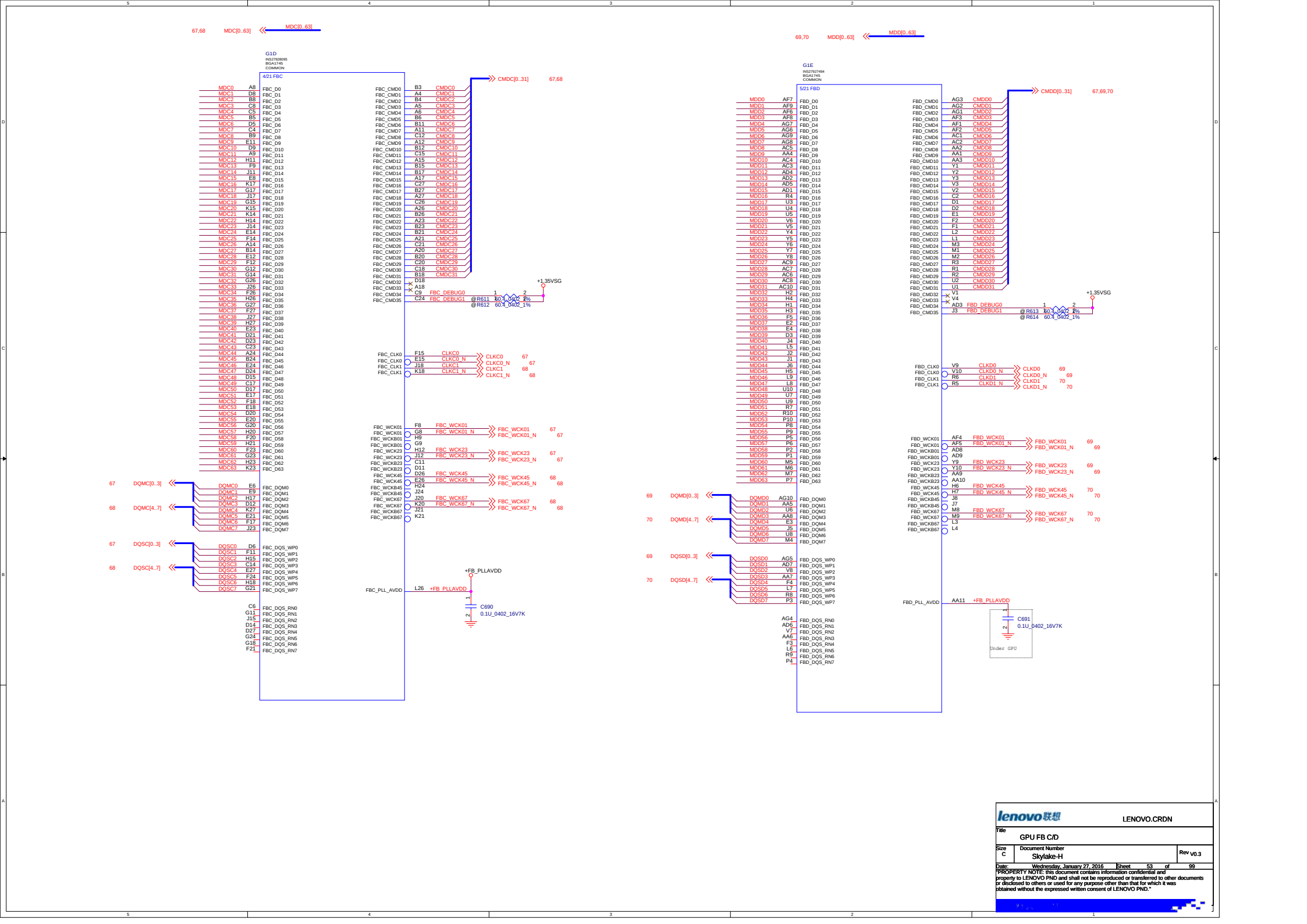
lenovo联想 LENOVO.CRDN

Title: GPU FB A/B

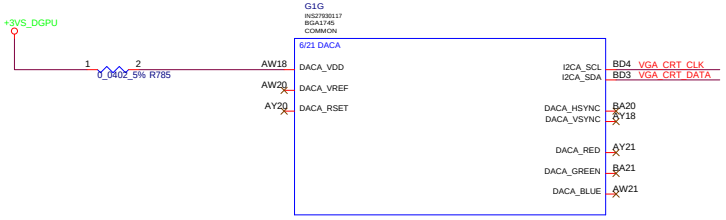
Size: C | Document Number: Skylake-H | Rev: V0.3

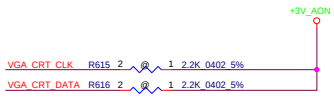
Date: Wednesday, January 27, 2016 | Sheet 52 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


67,68 MDC[0..63]
MDC[0..63]
G1D
INS27928095
BGA1745
COMMON
4/21 FBC
FBC_D0
FBC_D1
FBC_D2
FBC_D3
FBC_D4
FBC_D5
FBC_D6
FBC_D7
FBC_D8
FBC_D9
FBC_D10
FBC_D11
FBC_D12
FBC_D13
FBC_D14
FBC_D15
FBC_D16
FBC_D17
FBC_D18
FBC_D19
FBC_D20
FBC_D21
FBC_D22
FBC_D23
FBC_D24
FBC_D25
FBC_D26
FBC_D27
FBC_D28
FBC_D29
FBC_D30
FBC_D31
FBC_D32
FBC_D33
FBC_D34
FBC_D35
FBC_D36
FBC_D37
FBC_D38
FBC_D39
FBC_D40
FBC_D41
FBC_D42
FBC_D43
FBC_D44
FBC_D45
FBC_D46
FBC_D47
FBC_D48
FBC_D49
FBC_D50
FBC_D51
FBC_D52
FBC_D53
FBC_D54
FBC_D55
FBC_D56
FBC_D57
FBC_D58
FBC_D59
FBC_D60
FBC_D61
FBC_D62
FBC_D63
FBC_CMD0
FBC_CMD1
FBC_CMD2
FBC_CMD3
FBC_CMD4
FBC_CMD5
FBC_CMD6
FBC_CMD7
FBC_CMD8
FBC_CMD9
FBC_CMD10
FBC_CMD11
FBC_CMD12
FBC_CMD13
FBC_CMD14
FBC_CMD15
FBC_CMD16
FBC_CMD17
FBC_CMD18
FBC_CMD19
FBC_CMD20
FBC_CMD21
FBC_CMD22
FBC_CMD23
FBC_CMD24
FBC_CMD25
FBC_CMD26
FBC_CMD27
FBC_CMD28
FBC_CMD29
FBC_CMD30
FBC_CMD31
FBC_CMD32
FBC_CMD33
FBC_CMD34
FBC_CMD35
CMDC[0..31] 67,68
FBC_DEBUG0
FBC_DEBUG1
+1.35VSG
@R611 60.4_0402_1%
@R612 60.4_0402_1%
FBC_CLK0
FBC_CLK0
FBC_CLK1
FBC_CLK1
CLKC0
CLKC0_N
CLKC1
CLKC1_N
FBC_WCK01
FBC_WCK01_N
FBC_WCKB01
FBC_WCK23
FBC_WCK23_N
FBC_WCKB23
FBC_WCK45
FBC_WCK45_N
FBC_WCKB45
FBC_WCK67
FBC_WCK67_N
FBC_WCKB67
67 DQMC[0..3]
68 DQMC[4..7]
DQMC0
DQMC1
DQMC2
DQMC3
DQMC4
DQMC5
DQMC6
DQMC7
FBC_DQM0
FBC_DQM1
FBC_DQM2
FBC_DQM3
FBC_DQM4
FBC_DQM5
FBC_DQM6
FBC_DQM7
67 DQSC[0..3]
68 DQSC[4..7]
DQSC0
DQSC1
DQSC2
DQSC3
DQSC4
DQSC5
DQSC6
DQSC7
FBC_DQS_WP0
FBC_DQS_WP1
FBC_DQS_WP2
FBC_DQS_WP3
FBC_DQS_WP4
FBC_DQS_WP5
FBC_DQS_WP6
FBC_DQS_WP7
FBC_DQS_RN0
FBC_DQS_RN1
FBC_DQS_RN2
FBC_DQS_RN3
FBC_DQS_RN4
FBC_DQS_RN5
FBC_DQS_RN6
FBC_DQS_RN7
FBC_PLL_AVDD
+FB_PLLAVDD
C690
0.1U_0402_16V7K
69,70 MDD[0..63]
MDD[0..63]
G1E
INS27927494
BGA1745
COMMON
5/21 FBD
FBD_D0
FBD_D1
FBD_D2
FBD_D3
FBD_D4
FBD_D5
FBD_D6
FBD_D7
FBD_D8
FBD_D9
FBD_D10
FBD_D11
FBD_D12
FBD_D13
FBD_D14
FBD_D15
FBD_D16
FBD_D17
FBD_D18
FBD_D19
FBD_D20
FBD_D21
FBD_D22
FBD_D23
FBD_D24
FBD_D25
FBD_D26
FBD_D27
FBD_D28
FBD_D29
FBD_D30
FBD_D31
FBD_D32
FBD_D33
FBD_D34
FBD_D35
FBD_D36
FBD_D37
FBD_D38
FBD_D39
FBD_D40
FBD_D41
FBD_D42
FBD_D43
FBD_D44
FBD_D45
FBD_D46
FBD_D47
FBD_D48
FBD_D49
FBD_D50
FBD_D51
FBD_D52
FBD_D53
FBD_D54
FBD_D55
FBD_D56
FBD_D57
FBD_D58
FBD_D59
FBD_D60
FBD_D61
FBD_D62
FBD_D63
FBD_CMD0
FBD_CMD1
FBD_CMD2
FBD_CMD3
FBD_CMD4
FBD_CMD5
FBD_CMD6
FBD_CMD7
FBD_CMD8
FBD_CMD9
FBD_CMD10
FBD_CMD11
FBD_CMD12
FBD_CMD13
FBD_CMD14
FBD_CMD15
FBD_CMD16
FBD_CMD17
FBD_CMD18
FBD_CMD19
FBD_CMD20
FBD_CMD21
FBD_CMD22
FBD_CMD23
FBD_CMD24
FBD_CMD25
FBD_CMD26
FBD_CMD27
FBD_CMD28
FBD_CMD29
FBD_CMD30
FBD_CMD31
FBD_CMD32
FBD_CMD33
FBD_CMD34
FBD_CMD35
CMDD[0..31] 67,69,70
FBD_DEBUG0
FBD_DEBUG1
+1.35VSG
@R613 60.4_0402_1%
@R614 60.4_0402_1%
FBD_CLK0
FBD_CLK0
FBD_CLK1
FBD_CLK1
CLKD0
CLKD0_N
CLKD1
CLKD1_N
FBD_WCK01
FBD_WCK01_N
FBD_WCKB01
FBD_WCK23
FBD_WCK23_N
FBD_WCKB23
FBD_WCK45
FBD_WCK45_N
FBD_WCKB45
FBD_WCK67
FBD_WCK67_N
FBD_WCKB67
69 DQMD[0..3]
70 DQMD[4..7]
DQMD0
DQMD1
DQMD2
DQMD3
DQMD4
DQMD5
DQMD6
DQMD7
FBD_DQM0
FBD_DQM1
FBD_DQM2
FBD_DQM3
FBD_DQM4
FBD_DQM5
FBD_DQM6
FBD_DQM7
69 DQSD[0..3]
70 DQSD[4..7]
DQSD0
DQSD1
DQSD2
DQSD3
DQSD4
DQSD5
DQSD6
DQSD7
FBD_DQS_WP0
FBD_DQS_WP1
FBD_DQS_WP2
FBD_DQS_WP3
FBD_DQS_WP4
FBD_DQS_WP5
FBD_DQS_WP6
FBD_DQS_WP7
FBD_DQS_RN0
FBD_DQS_RN1
FBD_DQS_RN2
FBD_DQS_RN3
FBD_DQS_RN4
FBD_DQS_RN5
FBD_DQS_RN6
FBD_DQS_RN7
FBD_PLL_AVDD
+FB_PLLAVDD
C691
0.1U_0402_16V7K
Under GPU
lenovo联想
LENOVO.CRDN
Title
GPU FB C/D
Size C
Document Number
Skylake-H
Rev V0.3
Date: Wednesday, January 27, 2016
Sheet 53 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

Need confirm with NV if follow PDG to Capacitor/Bead, or only need connect 3V_MAIN to DACA_VDD?





Need double confirm with NV

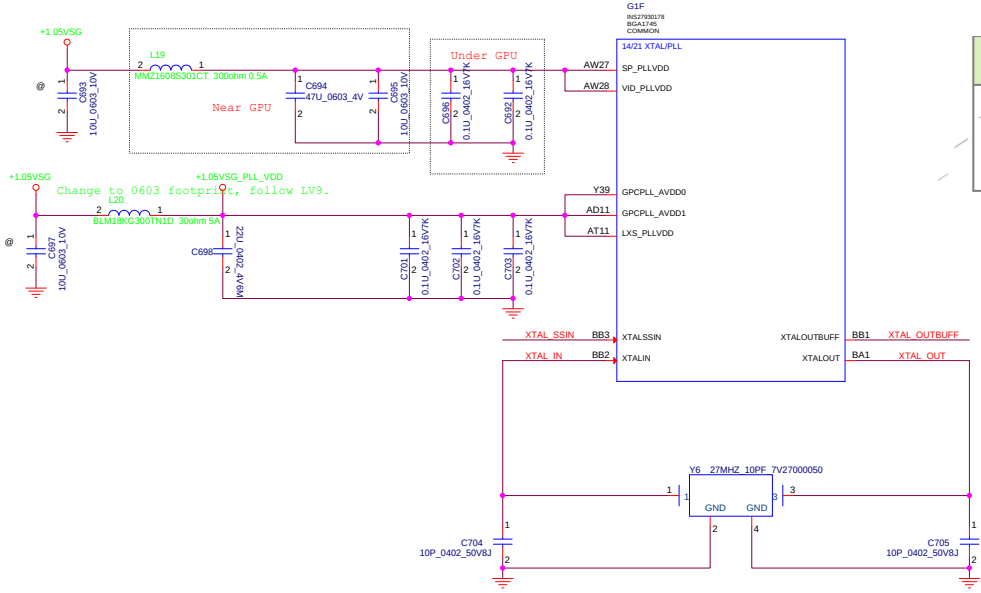
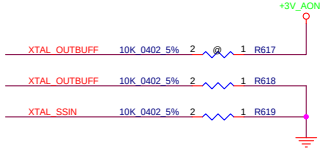


Table 3-36. GPCPLL_AVDD0/1, LXS_PLLVDD, and FB_PLL_DLL_AVDD0/1 Power Rail Filter Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB3B:256	GPCPLL_AVDD0/1 +	0.1 µF	X7R	0402	5	Under GPU
	LXS_PLLVDD +	22 µF	X5R	0805	1	Near GPU
	FB_PLL_DLL_AVDD0/1	**Bead Type**				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

NVIDIA Confidential



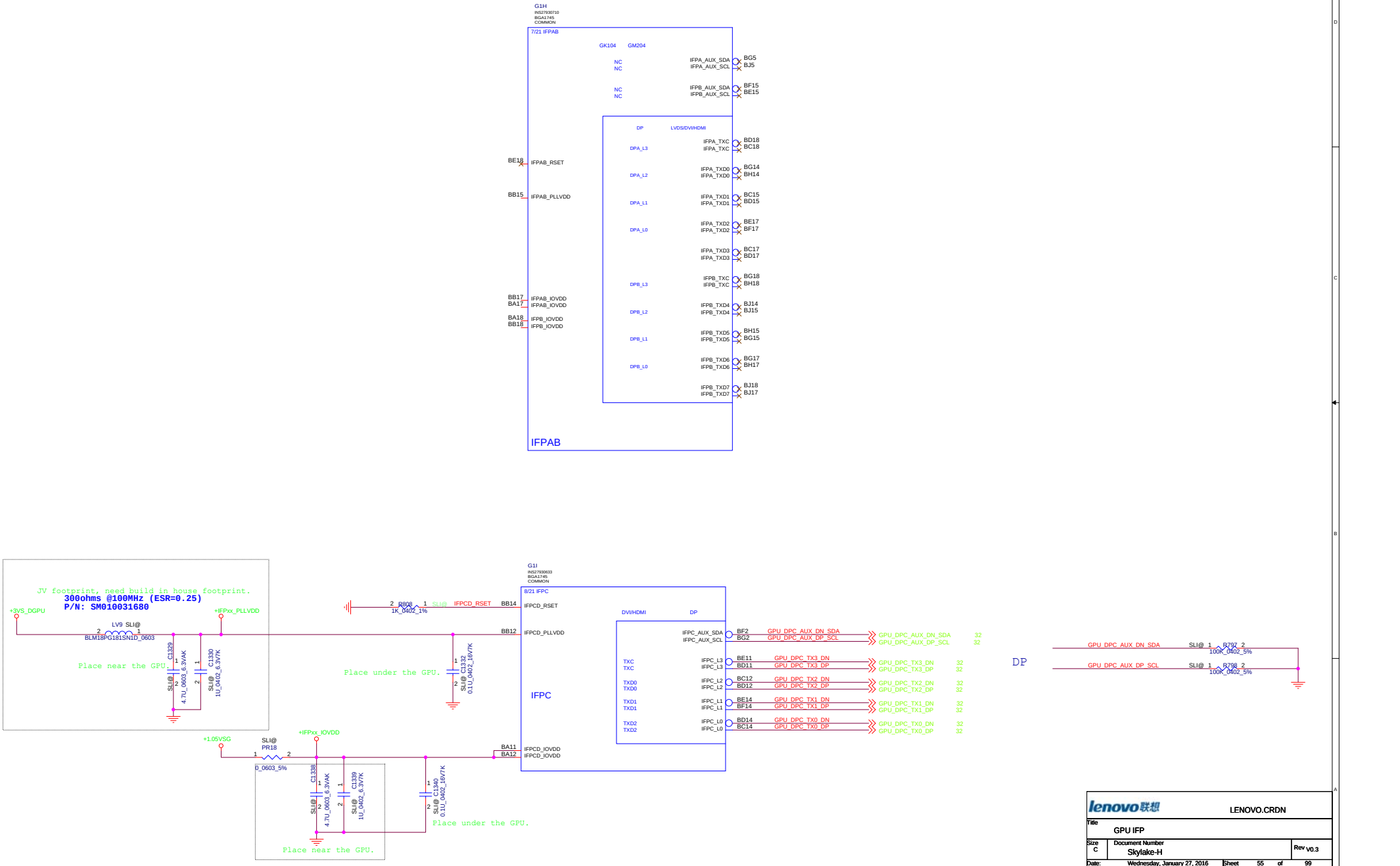
lenovo联想 LENOVO.CRDN

Title: GPU PLL/XTAL

Size: C | Document Number: Skylake-H | Rev: V0.3

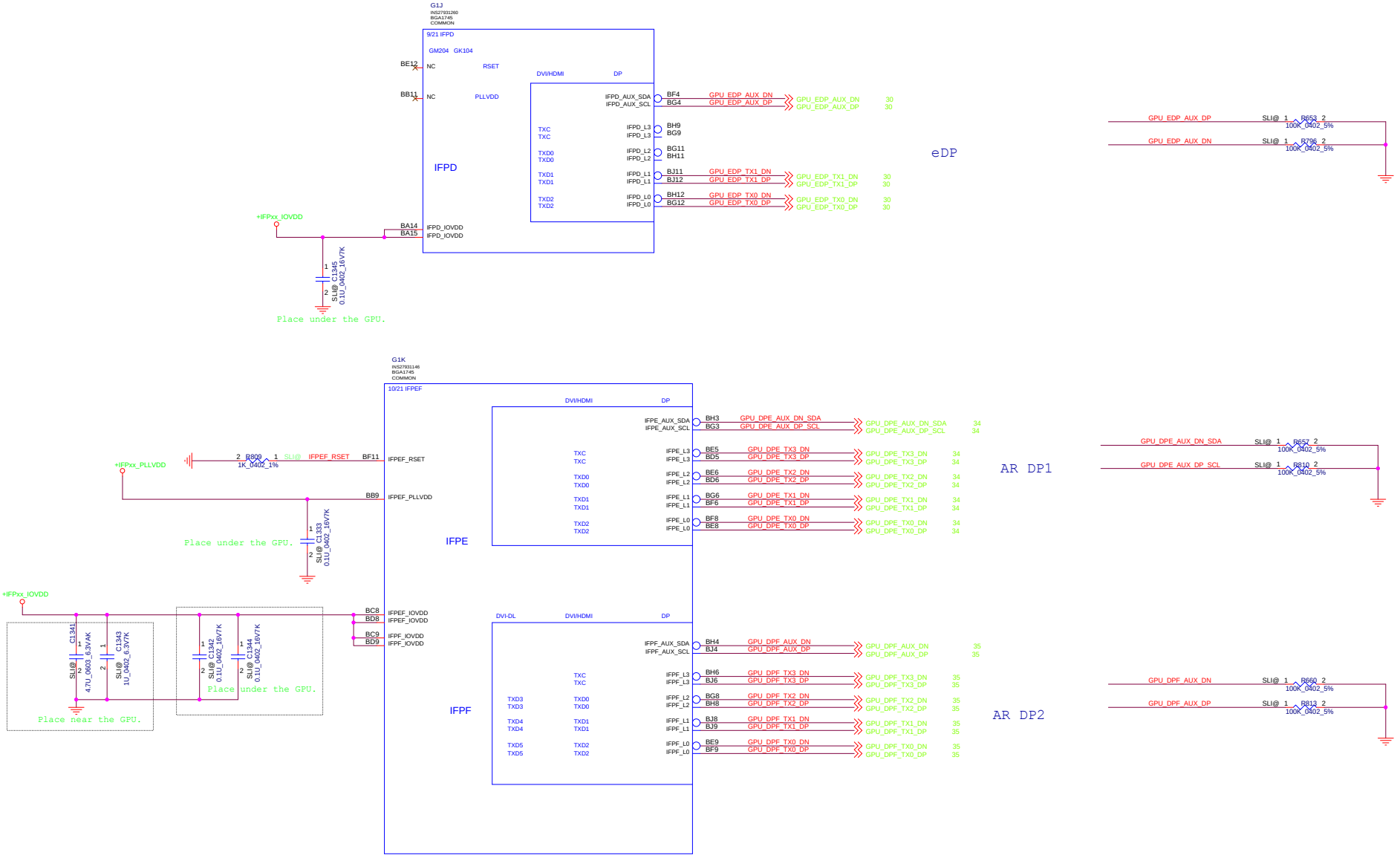
Date: Wednesday, January 27, 2016 | Sheet 54 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



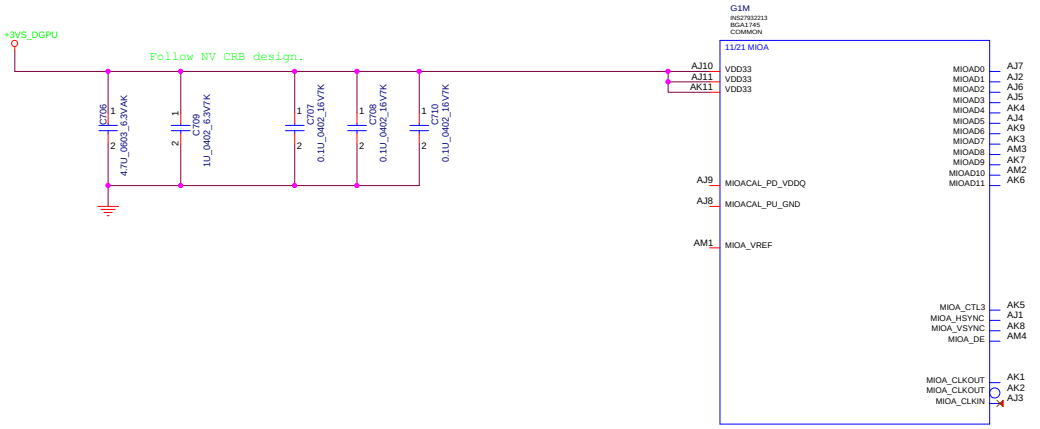
lenovo联想	LENOVO.CRDN	
Title	GPU IFP	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 55 of 99	

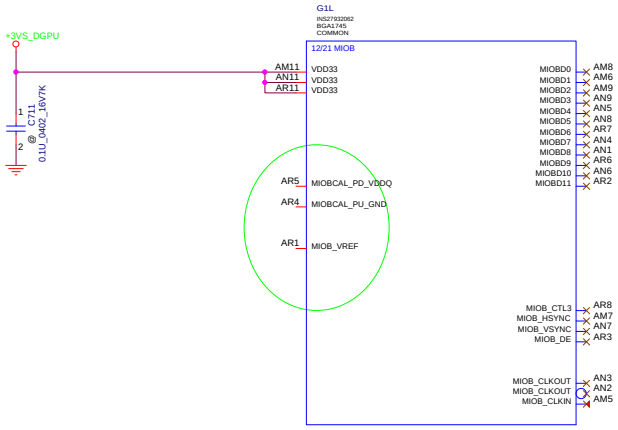
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN	
Title	GPU IFP	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 56 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."





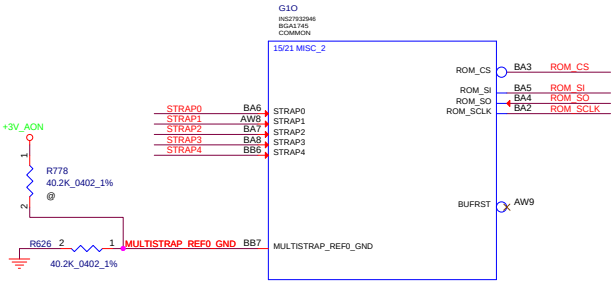
lenovo联想 LENOVO.CRDN

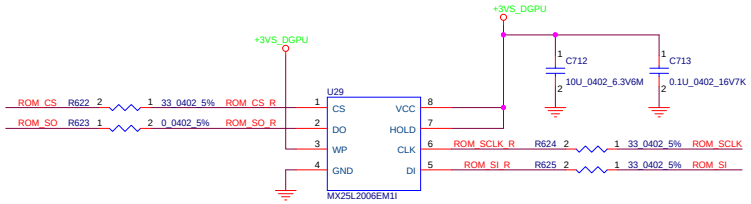
Title: GPU MIO

Size	Document Number	Rev
C	Skylake-H	V0.3

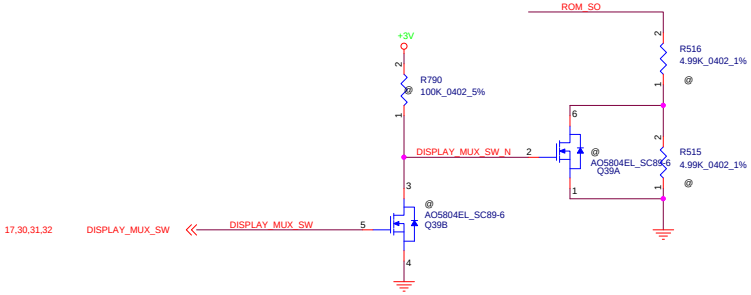
Date: Wednesday, January 27, 2016 Sheet 57 of 99

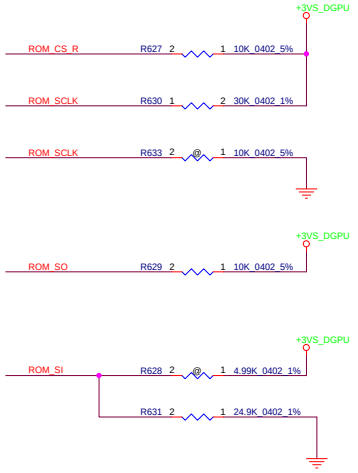
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

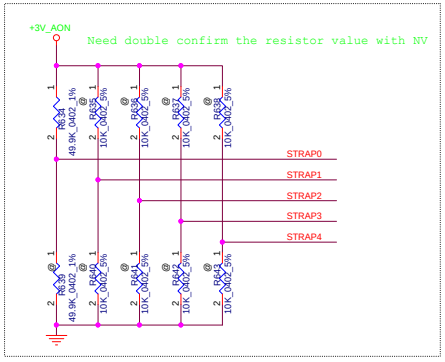




Follow NV's suggestion, change the ROM to SA00005LP00(MX25L2006EM1I-12G SOP 8P, A.2)







GPU	VRAM Vendor	Memory Density	VRAM P/N	Die-Revision	Lenovo P/N	Rom_SI	Bom stuff	
N16E-GX	Hynix	128M*16	H5GC2H24BFR-T2C	B-Die	1101020	PD 10K	R631=10KR_1%	NC
		256M*16	H5GC4H24AJR-T2C	A-Die	SV20H30108	PU 4.99K	NC	R628=4.99K_1%
	Samsung	128M*16	K4G20325FD-FC03	D-Die	1100893	PD 4.99K	R631=4.99KR_1%	NC
		256M*16	K4G41325FC-HC03	C-Die	1101023	PD 20K	R631=20KR_1%	NC
	Micron	128M*16	EDW2032BBBG-6A-F	B-Die	SV20G59954	PD 30.1K	R631=30.1KR_1%	NC
		256M*16	EDW4032BABG-60-F	A-Die	SV20G59955	PD 24.9K	R631=24.9KR_1%	NC

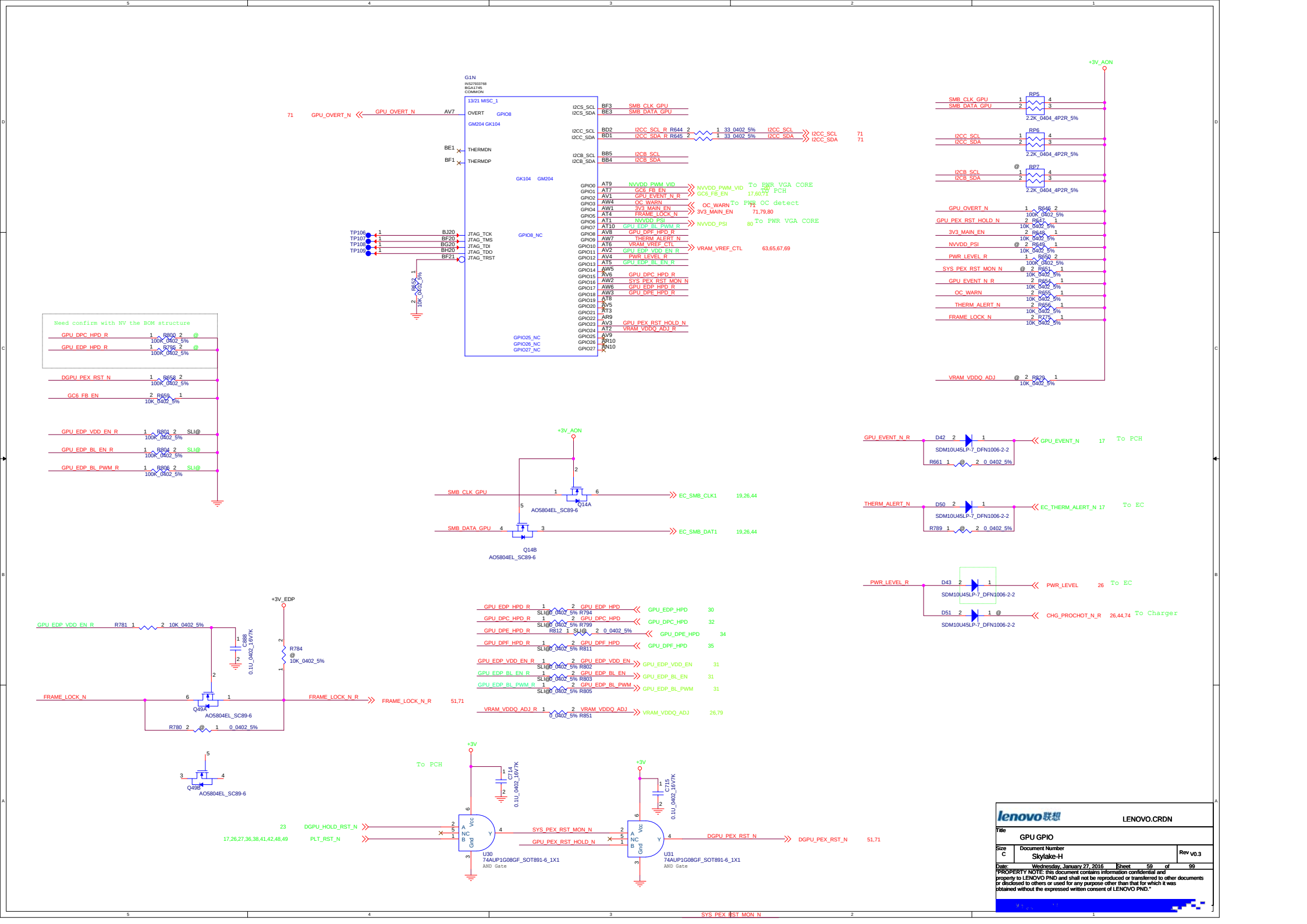
lenovo联想 LENOVO.CRDN

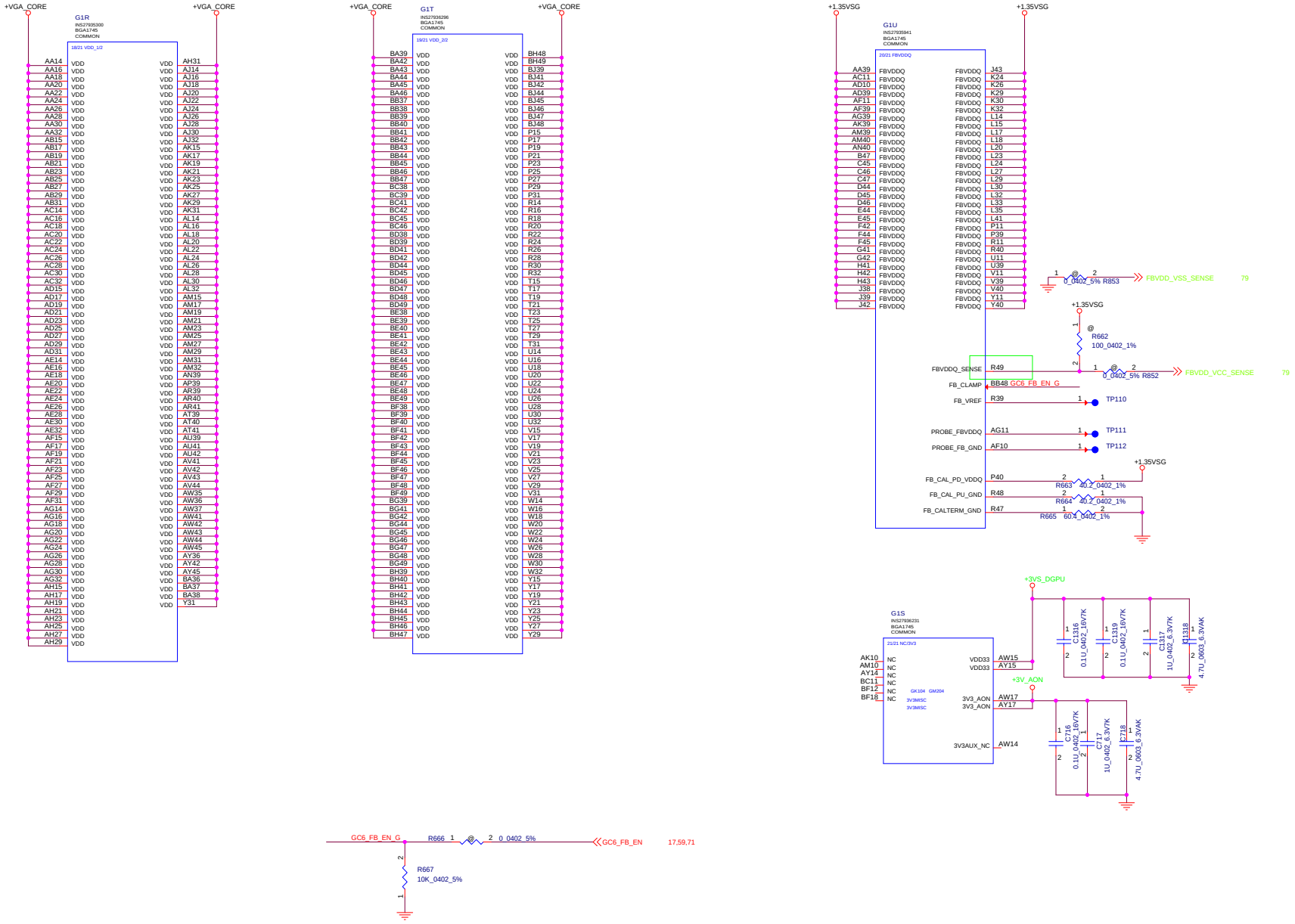
Title: GPU ROM/STRAP

Size: C | Document Number: Skylake-H | Rev V0.3

Date: Wednesday, January 27, 2016 | Sheet 58 of 99

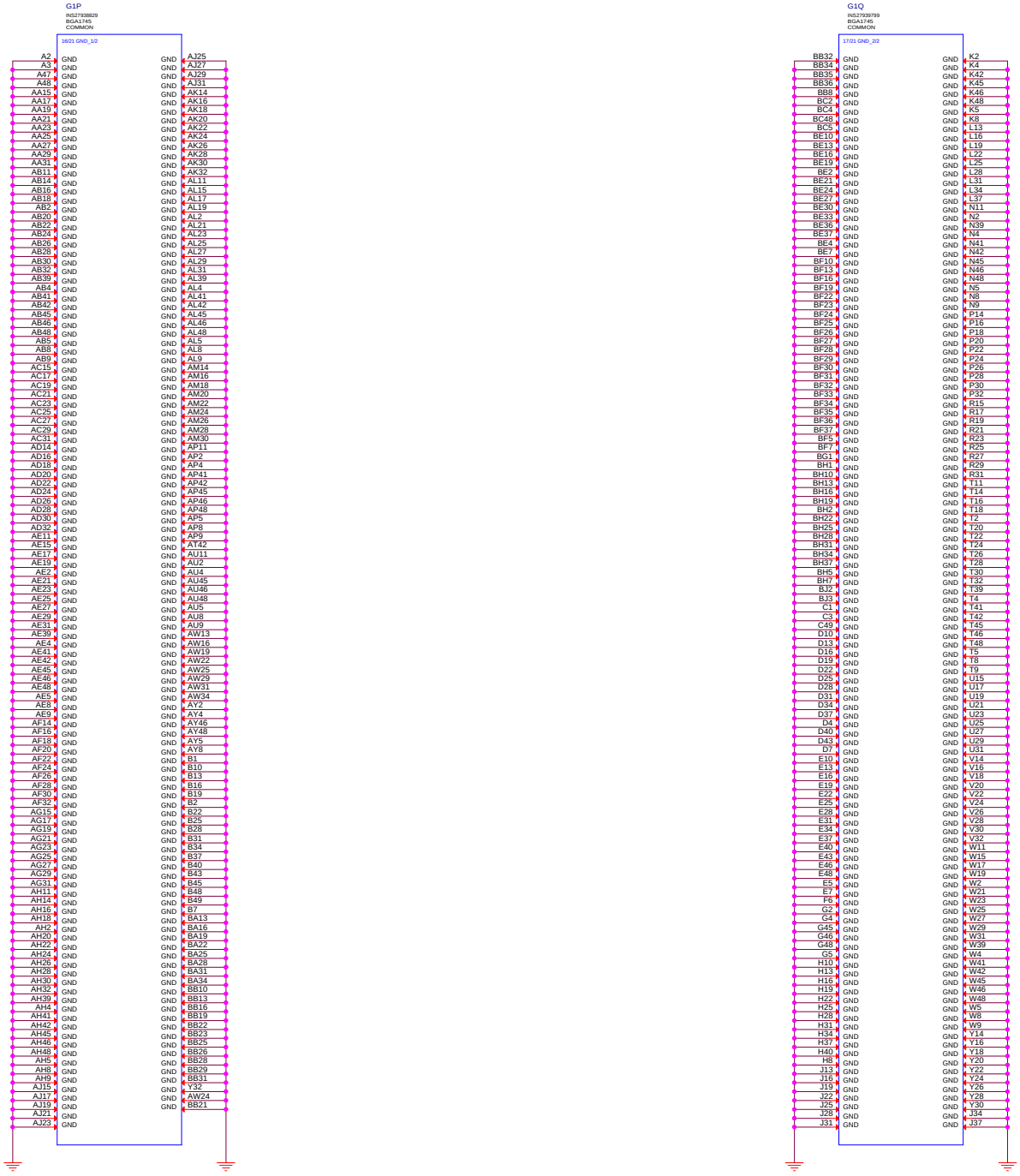
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


G1N
13/21 MISC_1
GM204 GK104
GK104 GM204
GPIO8_NC
GPIO25_NC
GPIO26_NC
GPIO27_NC
GPU_OVERT_N
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
SMB_CLK_GPU
SMB_DATA_GPU
I2CC_SCL_R
I2CC_SDA_R
I2CB_SCL
I2CB_SDA
NVVDD_PWM_VID
GC6_FB_EN
GPU_EVENT_N_R
OC_WARN
3V3_MAIN_EN
FRAME_LOCK_N
NVVDD_PSI
GPU_EDP_BL_PWM_R
GPU_DPF_HPD_R
THERM_ALERT_N
VRAM_VREF_CTL
GPU_EDP_VDD_EN_R
PWR_LEVEL_R
GPU_EDP_BL_EN_R
GPU_DPC_HPD_R
SYS_PEX_RST_MON_N
GPU_EDP_HPD_R
GPU_PEX_RST_HOLD_N
VRAM_VDDQ_ADJ_R
To PWR VGA CORE
To PCH
To PWR OC detect
To PWR VGA CORE
+3V_AON
SMB_CLK_GPU
SMB_DATA_GPU
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
GPU_OVERT_N
GPU_PEX_RST_HOLD_N
3V3_MAIN_EN
NVVDD_PSI
PWR_LEVEL_R
SYS_PEX_RST_MON_N
GPU_EVENT_N_R
OC_WARN
THERM_ALERT_N
FRAME_LOCK_N
VRAM_VDDQ_ADJ
Need confirm with NV the BOM structure
GPU_DPC_HPD_R
GPU_EDP_HPD_R
DGPU_PEX_RST_N
GC6_FB_EN
GPU_EDP_VDD_EN_R
GPU_EDP_BL_EN_R
GPU_EDP_BL_PWM_R
Q14A
Q14B
AO5804EL_SC89-6
EC_SMB_CLK1
EC_SMB_DAT1
GPU_EVENT_N
THERM_ALERT_N
EC_THERM_ALERT_N
PWR_LEVEL
CHG_PROCHOT_N_R
To EC
To Charger
SDM10U45LP-7_DFN1006-2-2
+3V_EDP
Q49A
Q49B
R784
R781
R780
FRAME_LOCK_N_R
GPU_EDP_HPD
GPU_DPC_HPD
GPU_DPE_HPD
GPU_DPF_HPD
GPU_EDP_VDD_EN
GPU_EDP_BL_EN
GPU_EDP_BL_PWM
VRAM_VDDQ_ADJ
To PCH
+3V
C714
C715
U30
U31
74AUP1G08GF_SOT891-6_1X1
AND Gate
DGPU_HOLD_RST_N
PLT_RST_N
SYS_PEX_RST_MON_N
GPU_PEX_RST_HOLD_N
DGPU_PEX_RST_N
LENOVO.CRDN
GPU GPIO
Skylake-H
Rev V0.3
Wednesday, January 27, 2016
Sheet 59 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想		LENOVO.CRDN	
Title	GPU PWR		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 60 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



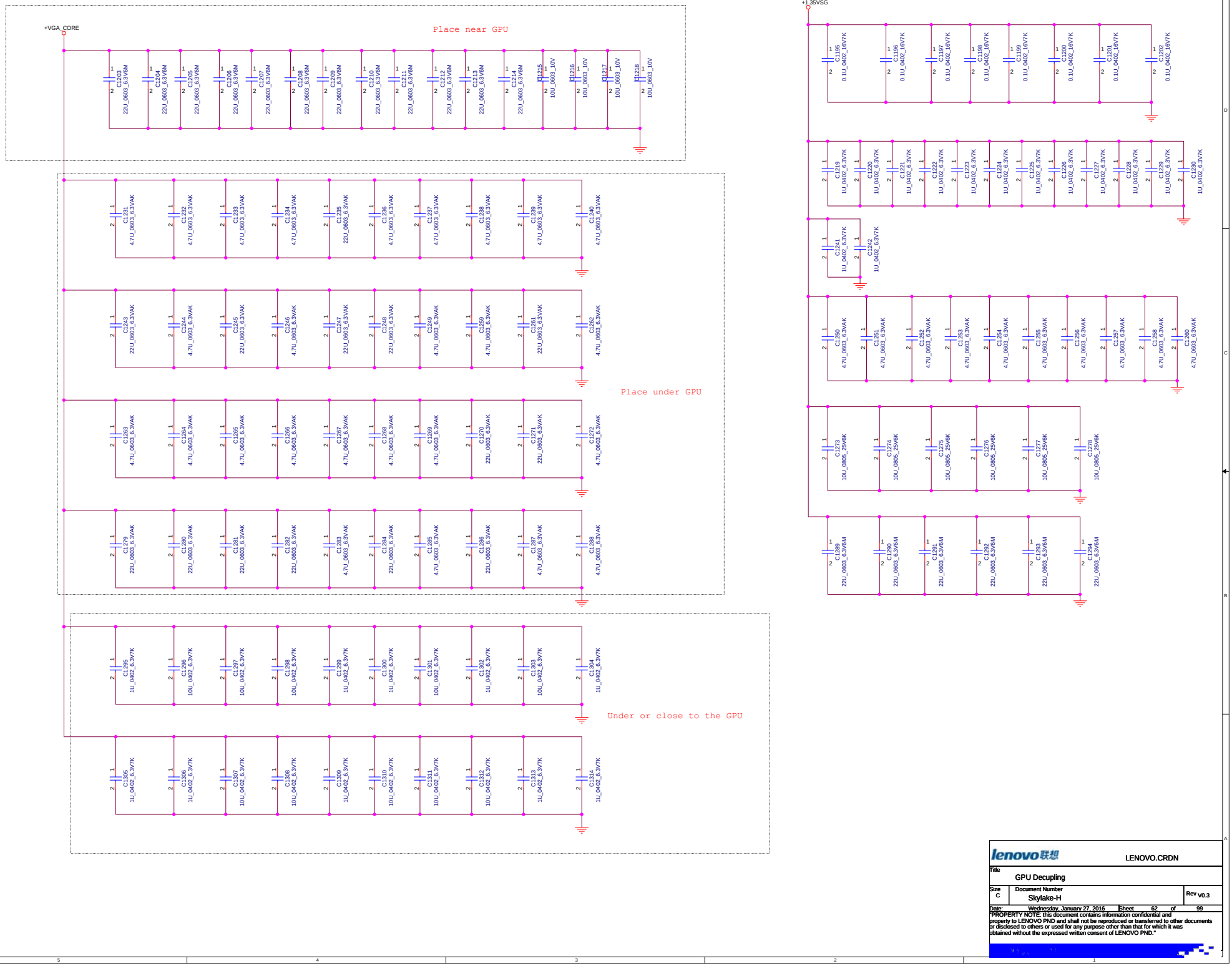
lenovo联想 LENOVO.CRDN

Title: GPU GND

Size	Document Number	Rev
C	Skylake-H	V0.3

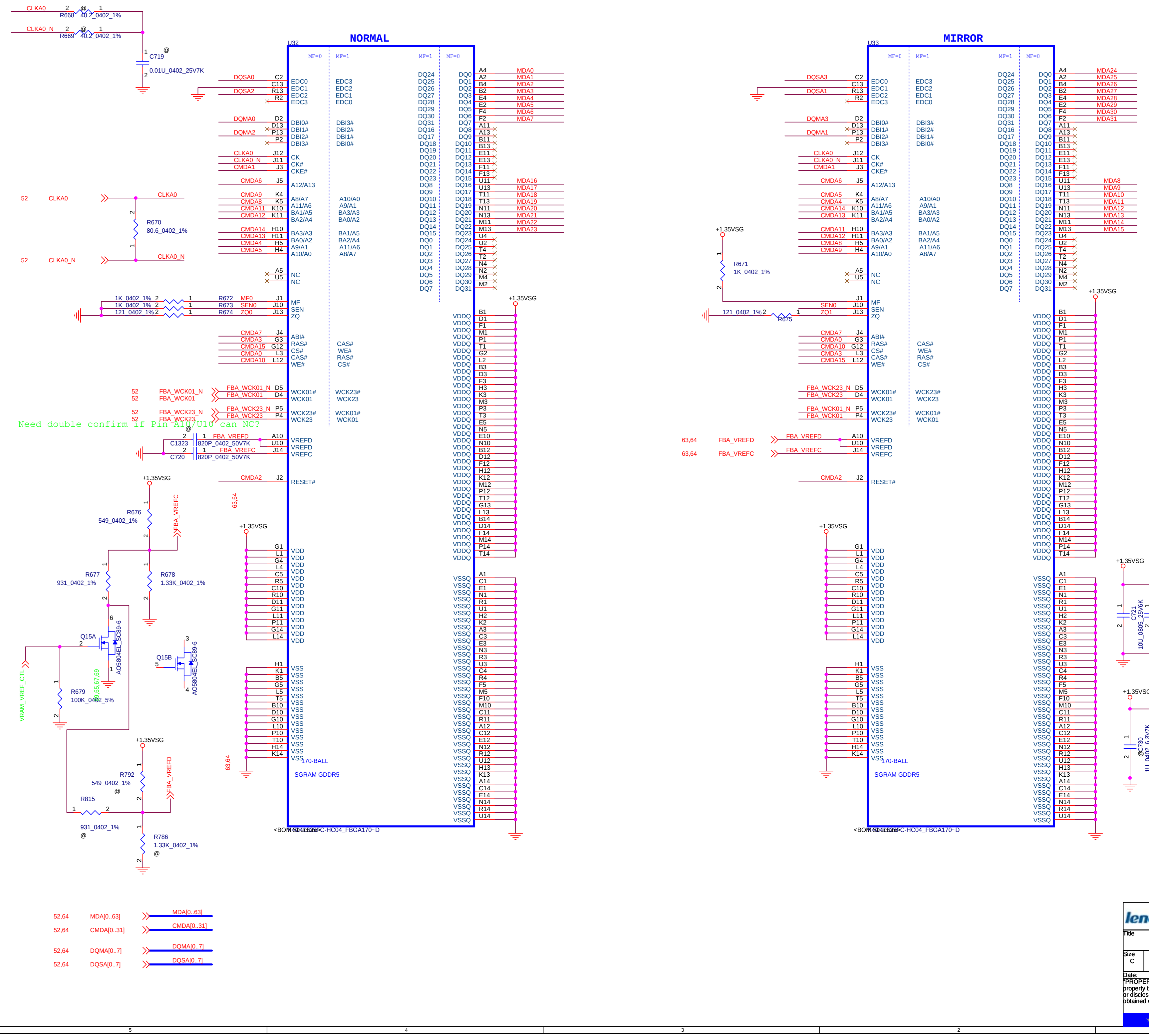
Date: Wednesday, January 27, 2016 Sheet 61 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN	
Title: GPU Decupling		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 62 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



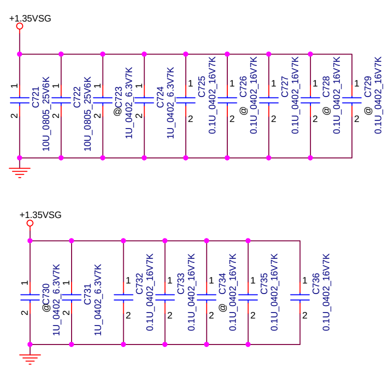


Table 7-5. GDDR5 Mode F Mapping

GB3B-256	Channel 0 0..31	GB3B-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3B-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See Section 7.1.13.

Confidential - 2014.06.

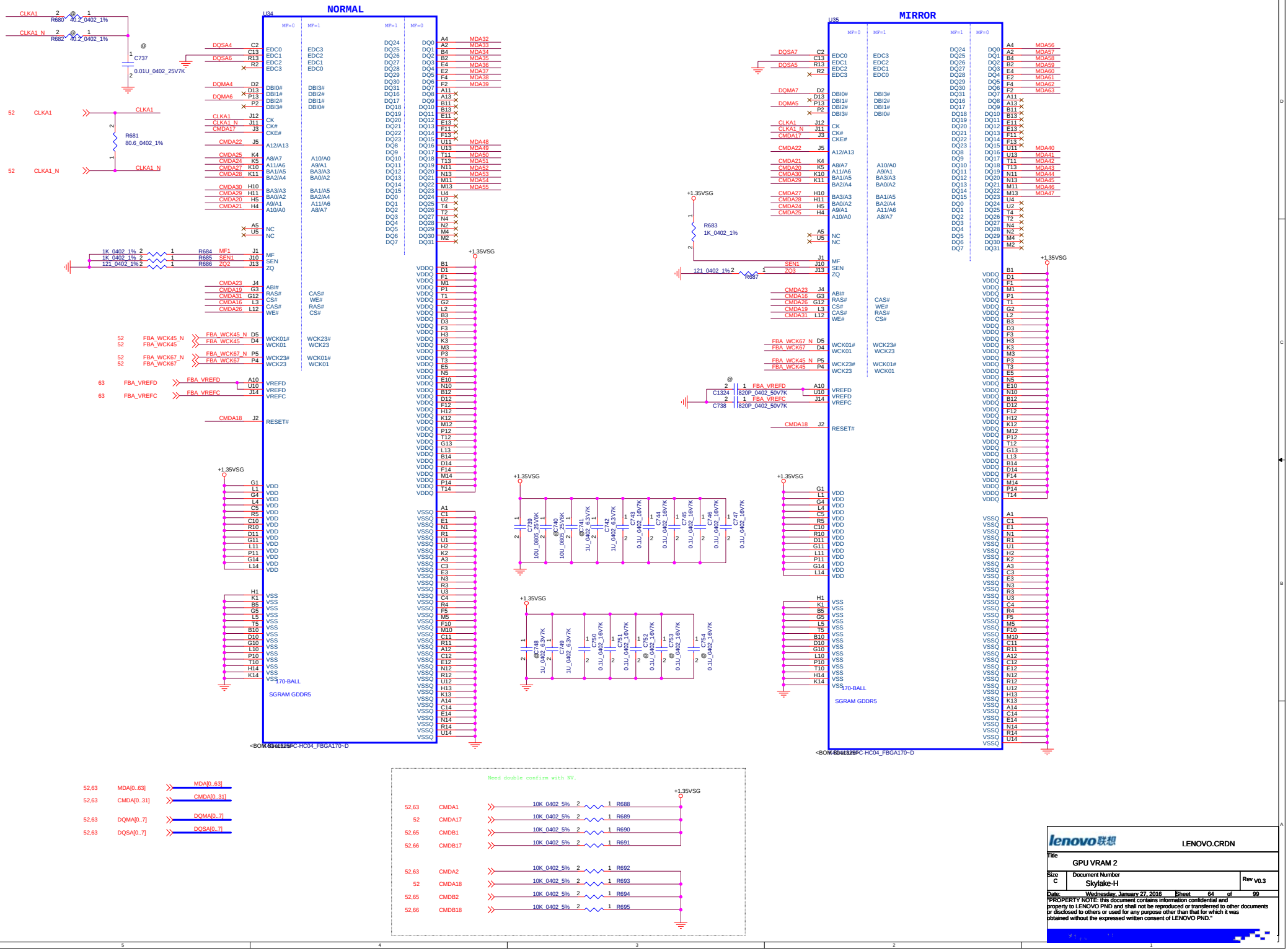
lenovo联想 LENOVO.CRDN

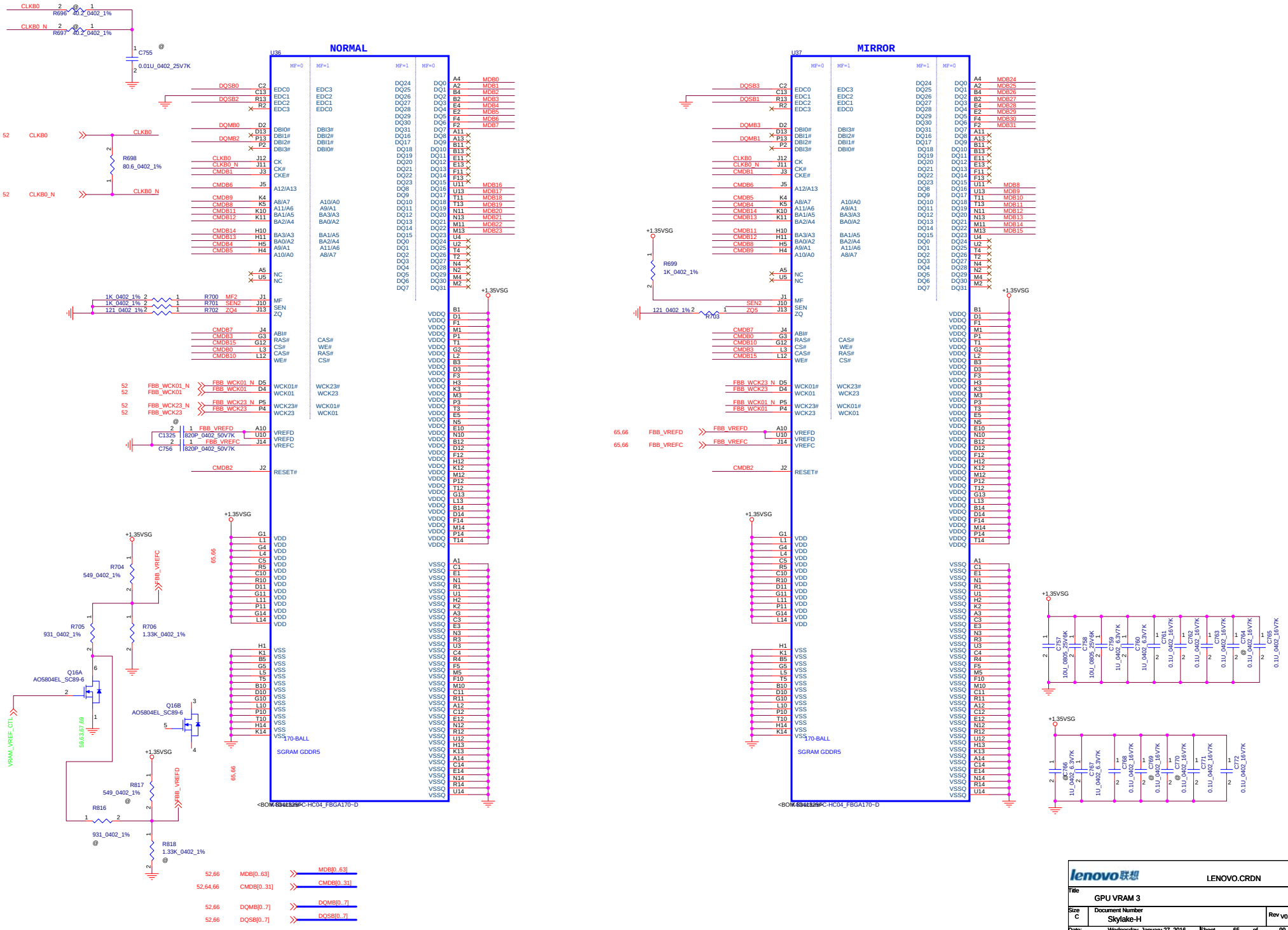
Title: GPU VRAM 1

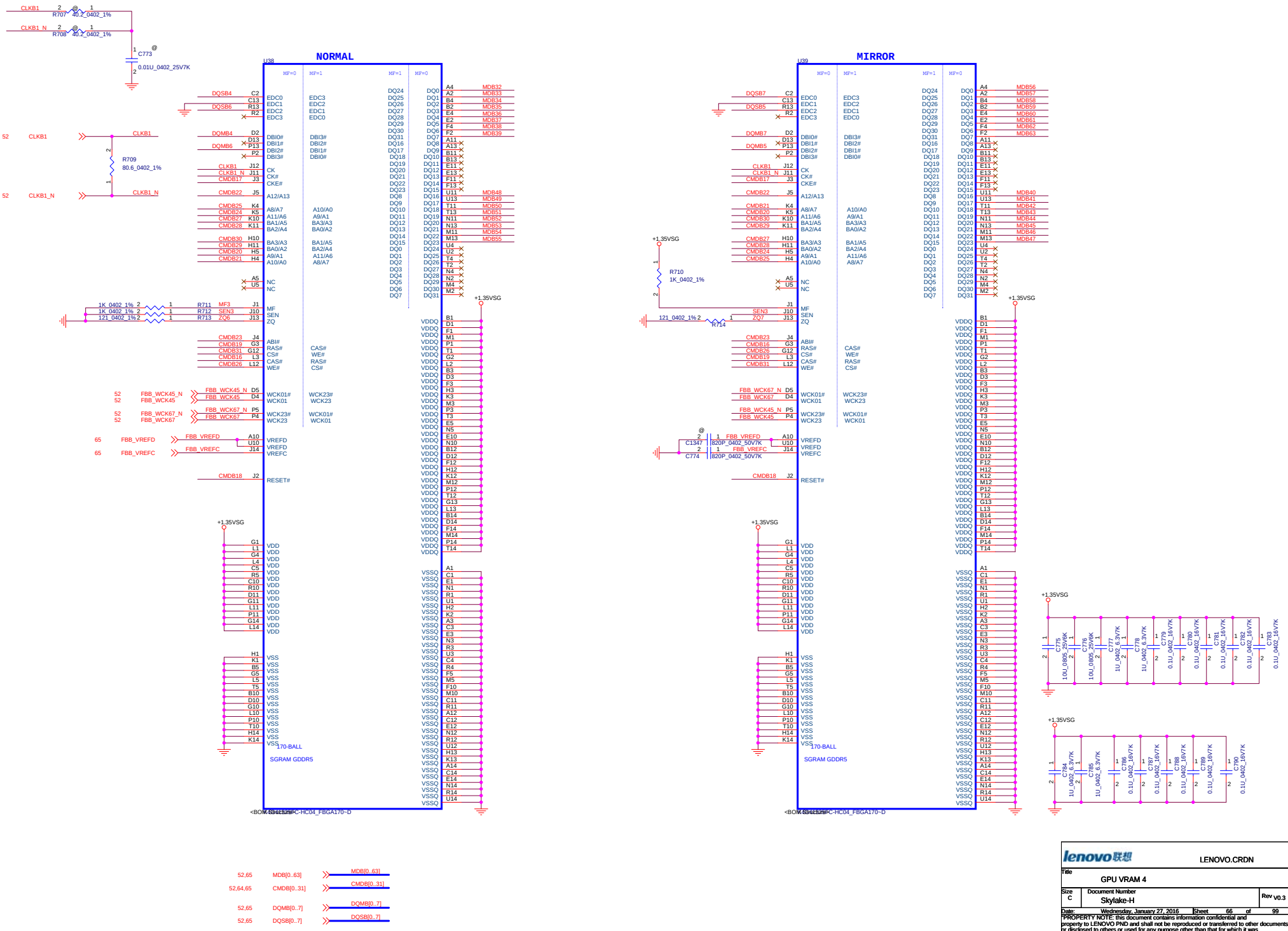
Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 63 of 99

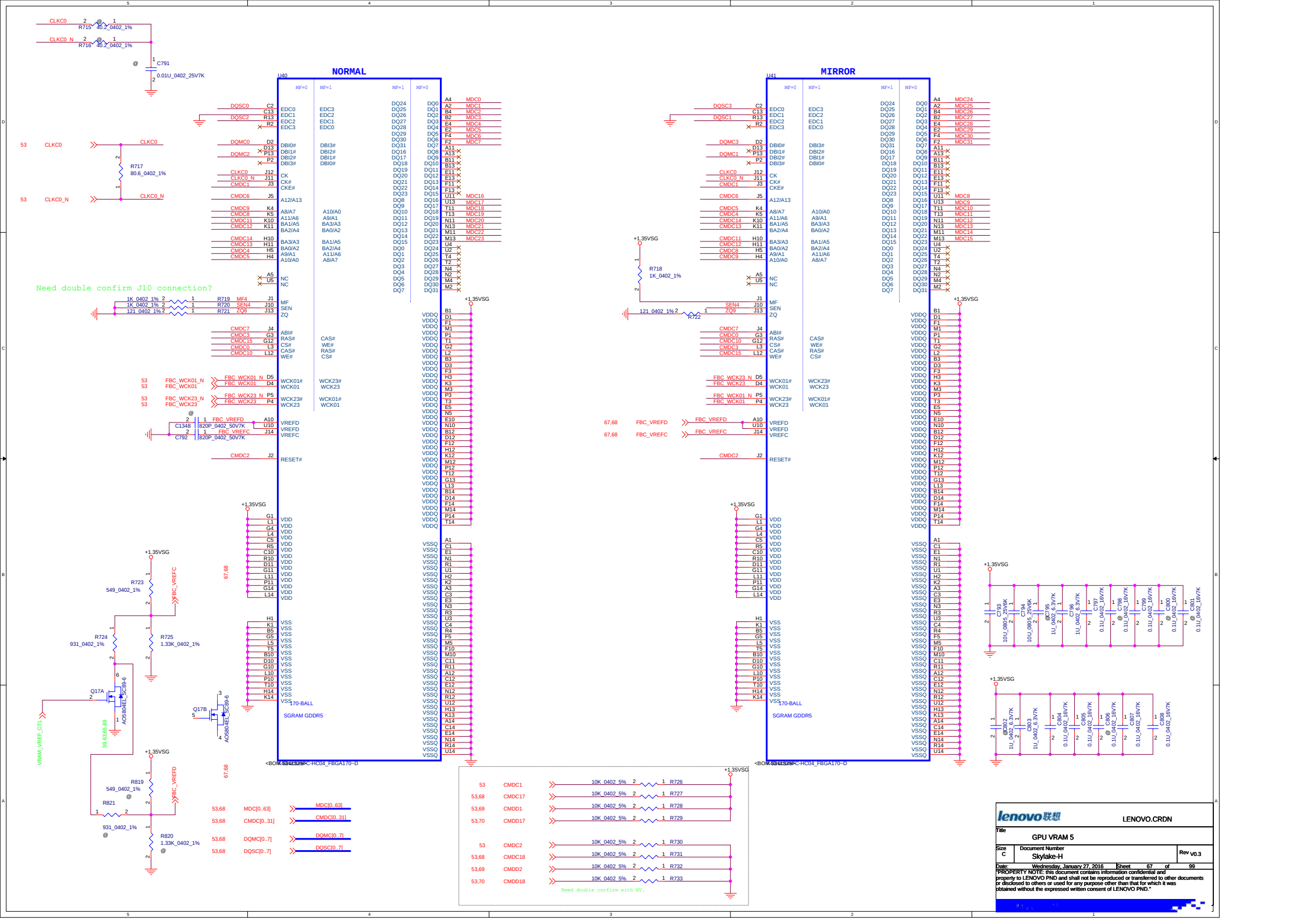
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

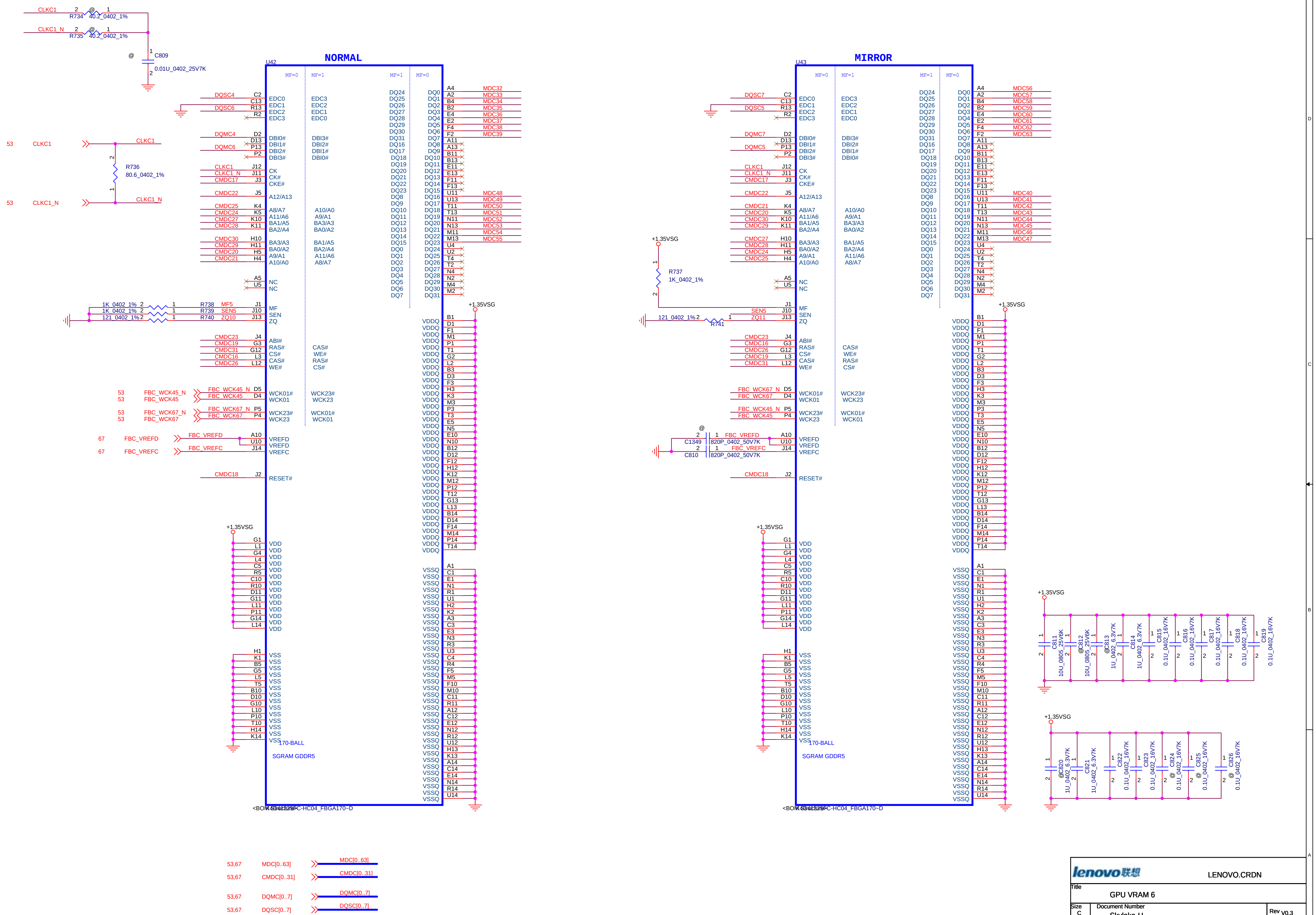

NORMAL
MIRROR
U34
U35
SGRAM GDDR5
170-BALL
+1.35VSG
Need double confirm with NV.
LENOVO.CRDN
GPU VRAM 2
Skylake-H
Wednesday, January 27, 2016
PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND.


NORMAL
MIRROR
U36
U37
CLKB0
CLKB0_N
R696
R697
40.2_0402_1%
C755
0.01U_0402_25V7K
R698
80.6_0402_1%
R699
1K_0402_1%
R700
R701
R702
1K_0402_1%
121_0402_1%
R703
+1.35VSG
FBB_VREFD
FBB_VREFC
C1325
C756
820P_0402_50V7K
R704
549_0402_1%
R705
931_0402_1%
R706
1.33K_0402_1%
Q16A
AO5804EL_SC89-6
Q16B
AO5804EL_SC89-6
VRAM_VREF_CTL
R817
R816
R818
1.33K_0402_1%
170-BALL
SGRAM GDDR5
MDB[0..63]
CMDB[0..31]
DQMB[0..7]
DQSB[0..7]
C757
C758
C759
C760
C761
C762
C763
C764
C765
C766
C767
C768
C769
C770
C771
C772
10U_0805_25V6K
1U_0402_6.3V7K
0.1U_0402_16V7K
LENOVO.CRDN
GPU VRAM 3
Skylake-H
V0.3
Wednesday, January 27, 2016
65
99



"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


NORMAL
MIRROR
U40
U41
Need double confirm J10 connection?
SGRAM GDDR5
170-BALL
Need double confirm with NV.
LENOVO.CRDN
GPU VRAM 5
Skylake-H
Rev V0.3
Wednesday, January 27, 2016
Sheet 67 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



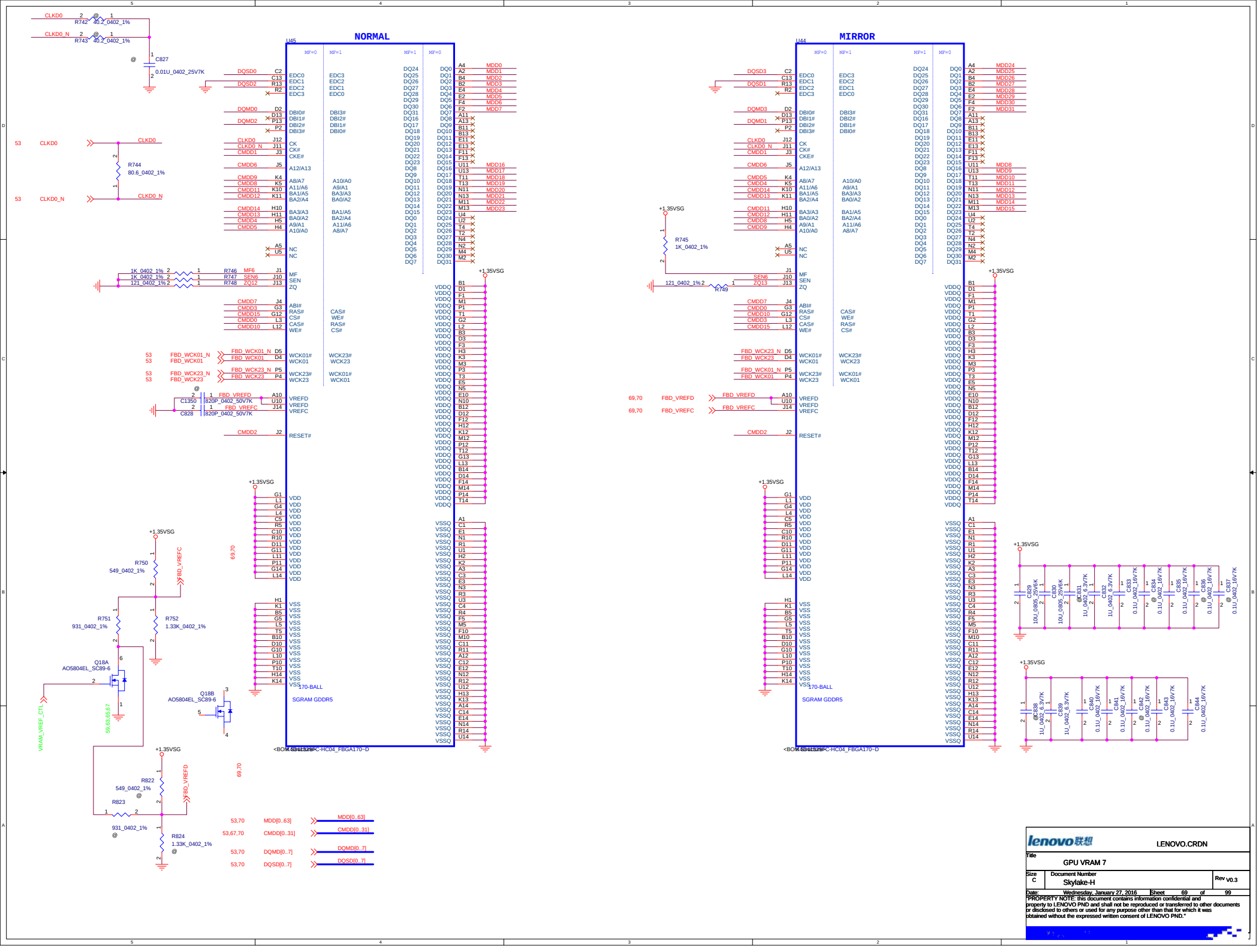
lenovo联想 LENOVO.CRDN

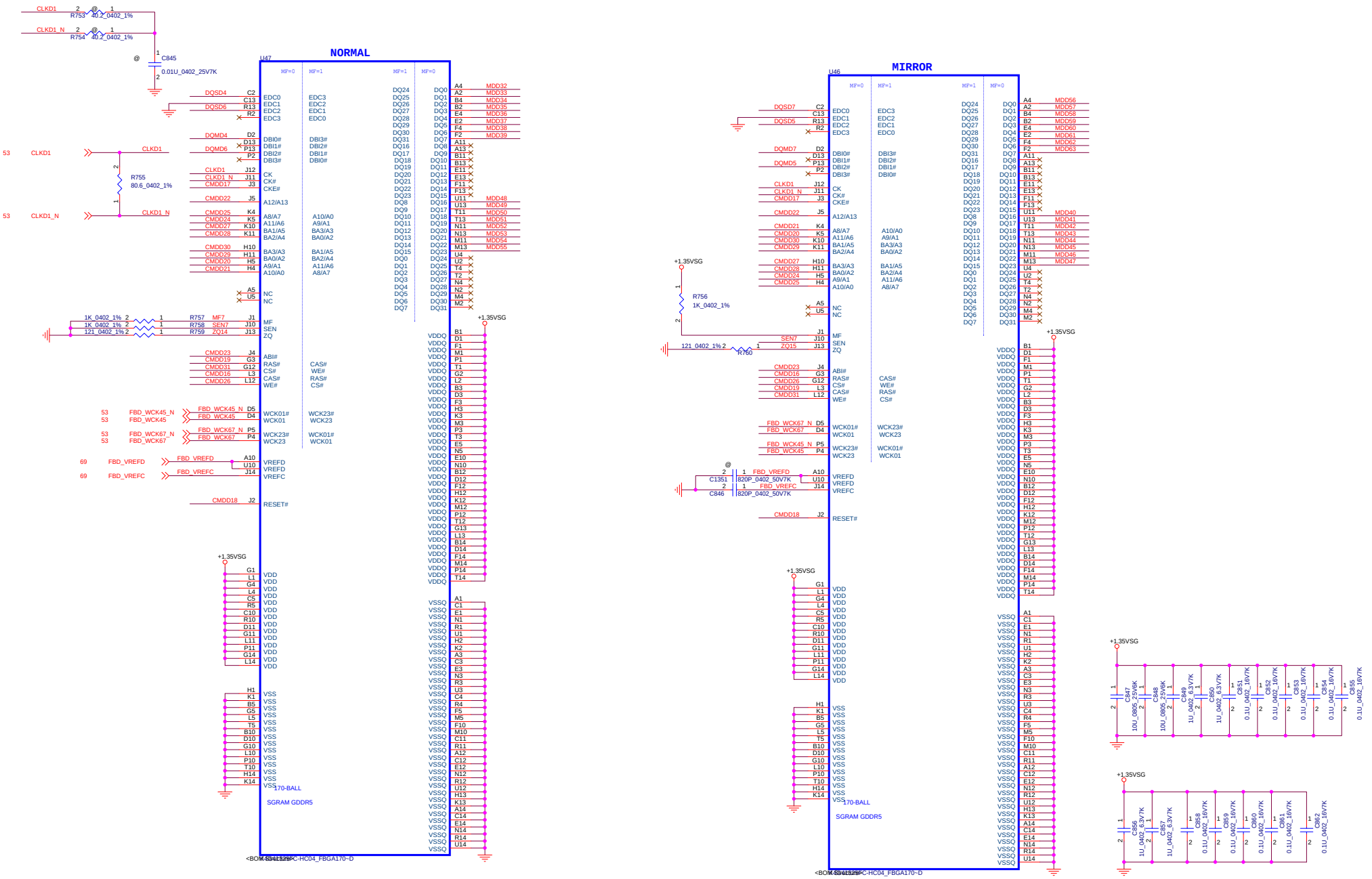
Title: GPU VRAM 6

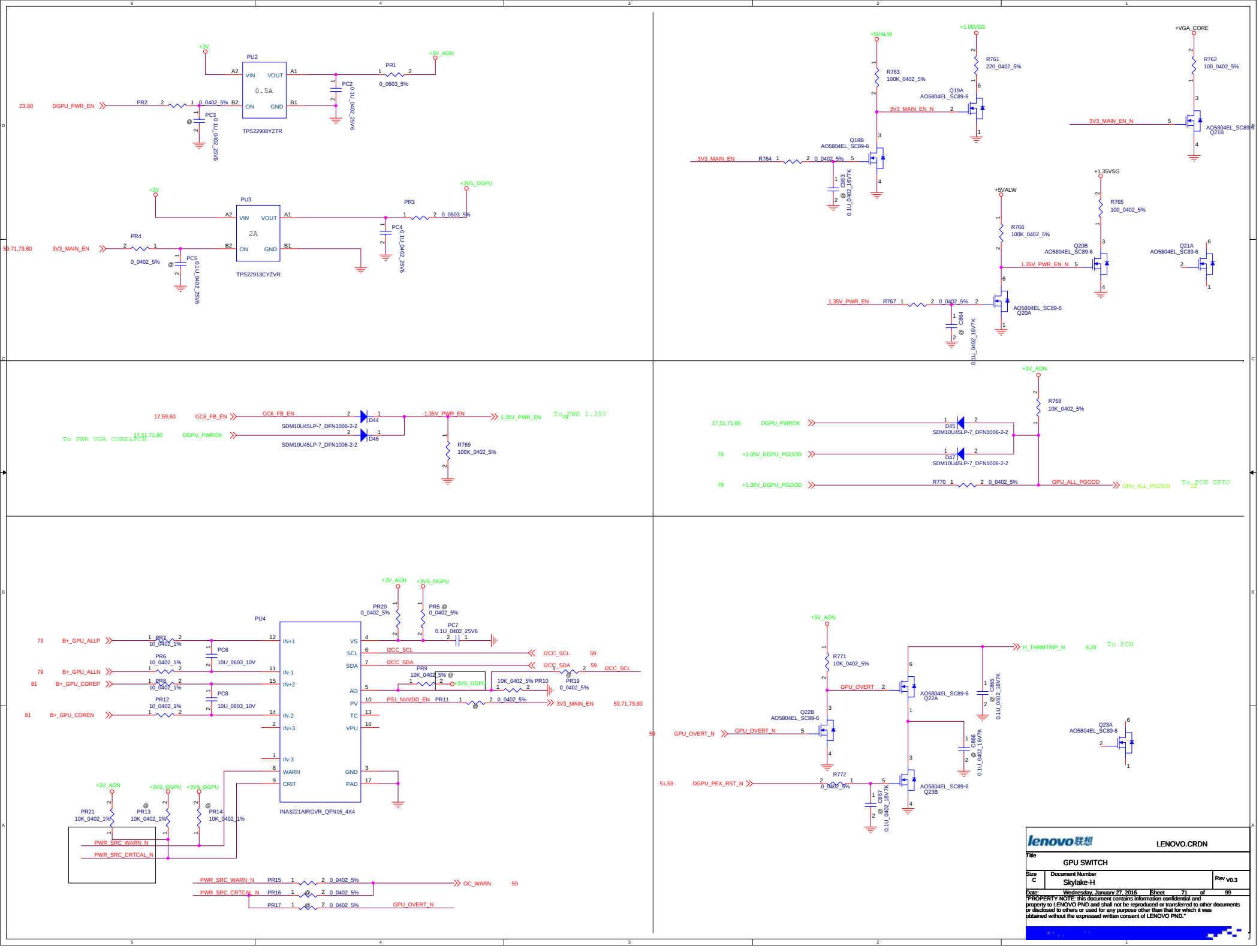
Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 68 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


NORMAL
MIRROR
U45
U44
SGRAM GDDR5
170-BALL
LENOVO.CRDN
GPU VRAM 7
Skylake-H
Wednesday, January 27, 2016
PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND.


NORMAL
MIRROR
U47
U46
MF=0
MF=1
CLKD1
CLKD1_N
R753 40.2_0402_1%
R754 40.2_0402_1%
C845 0.01U_0402_25V7K
R755 80.6_0402_1%
R756 1K_0402_1%
R757 MF7
R758 SEN7
R759 ZQ14
R760 121_0402_1%
ZQ15
CMDD18 RESET#
+1.35VSG
FBD_VREFD
FBD_VREFC
FBD_WCK45
FBD_WCK45_N
FBD_WCK67
FBD_WCK67_N
170-BALL
SGRAM GDDR5
MDD[0..63]
CMDD[0..31]
DQMD[0..7]
DQSD[0..7]
LENOVO.CRDN
GPU VRAM 8
Skylake-H
Wednesday, January 27, 2016
70
99
V0.3


PU2
TPS22908YZTR
PU3
TPS22913CYZVR
PU4
INA3221AIRGVR_QFN16_4X4
Q19A AO5804EL_SC89-6
Q19B AO5804EL_SC89-6
Q20A AO5804EL_SC89-6
Q20B AO5804EL_SC89-6
Q21A AO5804EL_SC89-6
Q21B AO5804EL_SC89-6
Q22A AO5804EL_SC89-6
Q22B AO5804EL_SC89-6
Q23A AO5804EL_SC89-6
Q23B AO5804EL_SC89-6
D44 SDM10U45LP-7_DFN1006-2-2
D45 SDM10U45LP-7_DFN1006-2-2
D46 SDM10U45LP-7_DFN1006-2-2
D47 SDM10U45LP-7_DFN1006-2-2
DGPU_PWR_EN
3V3_MAIN_EN
GC6_FB_EN
DGPU_PWROK
1.35V_PWR_EN
1.05V_DGPU_PGOOD
1.35V_PWR_EN_N
3V3_MAIN_EN_N
GPU_ALL_PGOOD
GPU_OVERT
GPU_OVERT_N
DGPU_PEX_RST_N
H_THRMTRIP_N
PS1_NVDD_EN
I2CC_SCL
I2CC_SDA
PWR_SRC_WARN_N
PWR_SRC_CRTCAL_N
OC_WARN
B+_GPU_ALLP
B+_GPU_ALLN
B+_GPU_COREP
B+_GPU_COREN
To PWR 1.35V
To PWR VGA CORE&PCH
To PCH GPIO
To PCH
LENOVO.CRDN
GPU SWITCH
Skylake-H
Wednesday, January 27, 2016

lenovo联想 LENOVO.CRDN

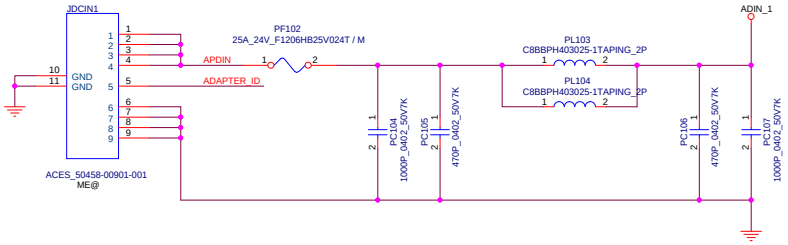
Title: BLANK

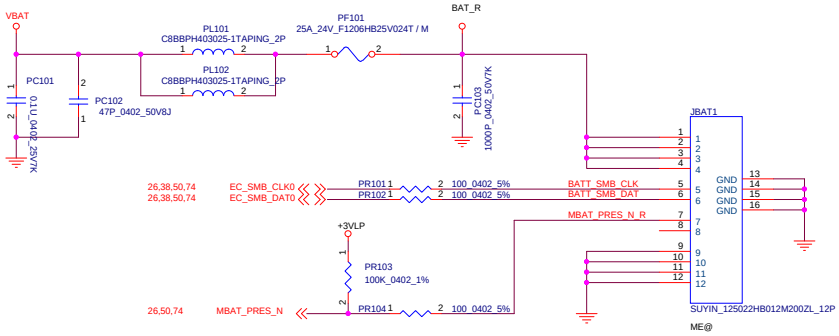
Size	Document Number	Rev
C	Skylake-H	V0.3

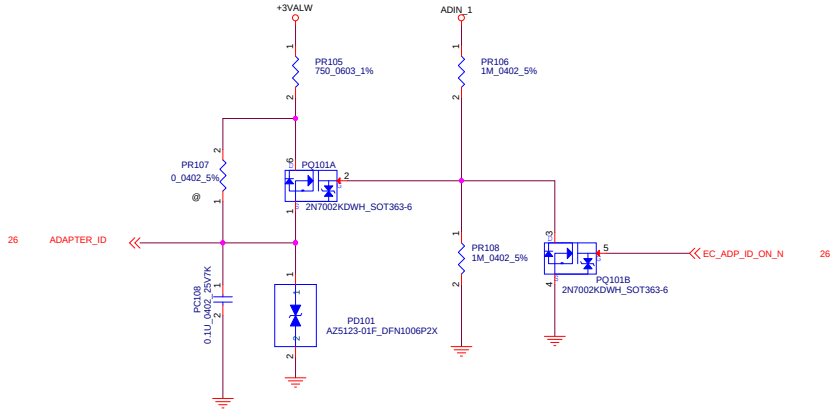
Date: Wednesday, January 27, 2016 Sheet 72 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

BATT CONN.

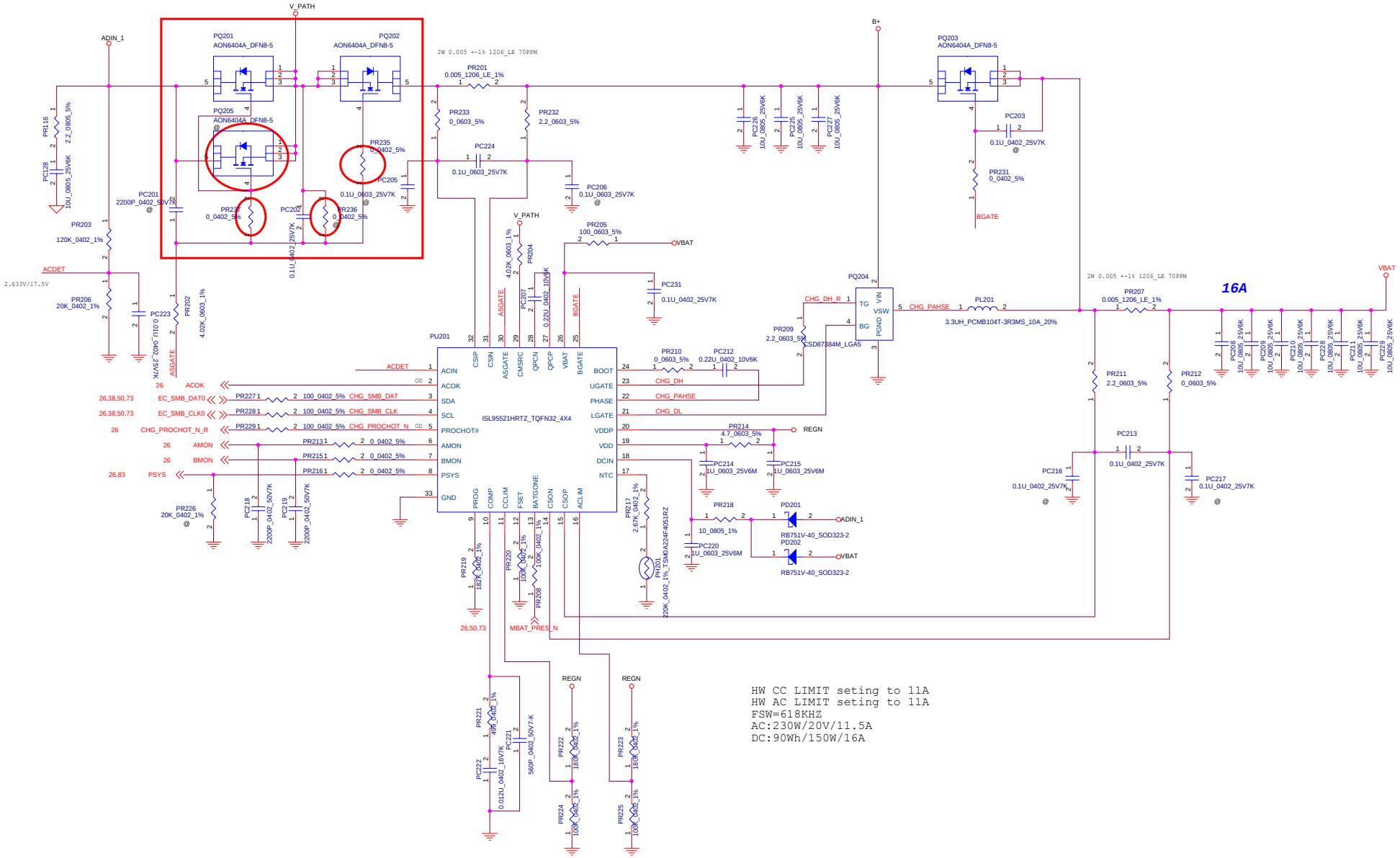






lenovo联想	LENOVO.CRDN	
Title: DCIN/BATT		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 73 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



HW CC LIMIT seting to 11A
HW AC LIMIT seting to 11A
FSW=618KHZ
AC:230W/20V/11.5A
DC:90Wh/150W/16A

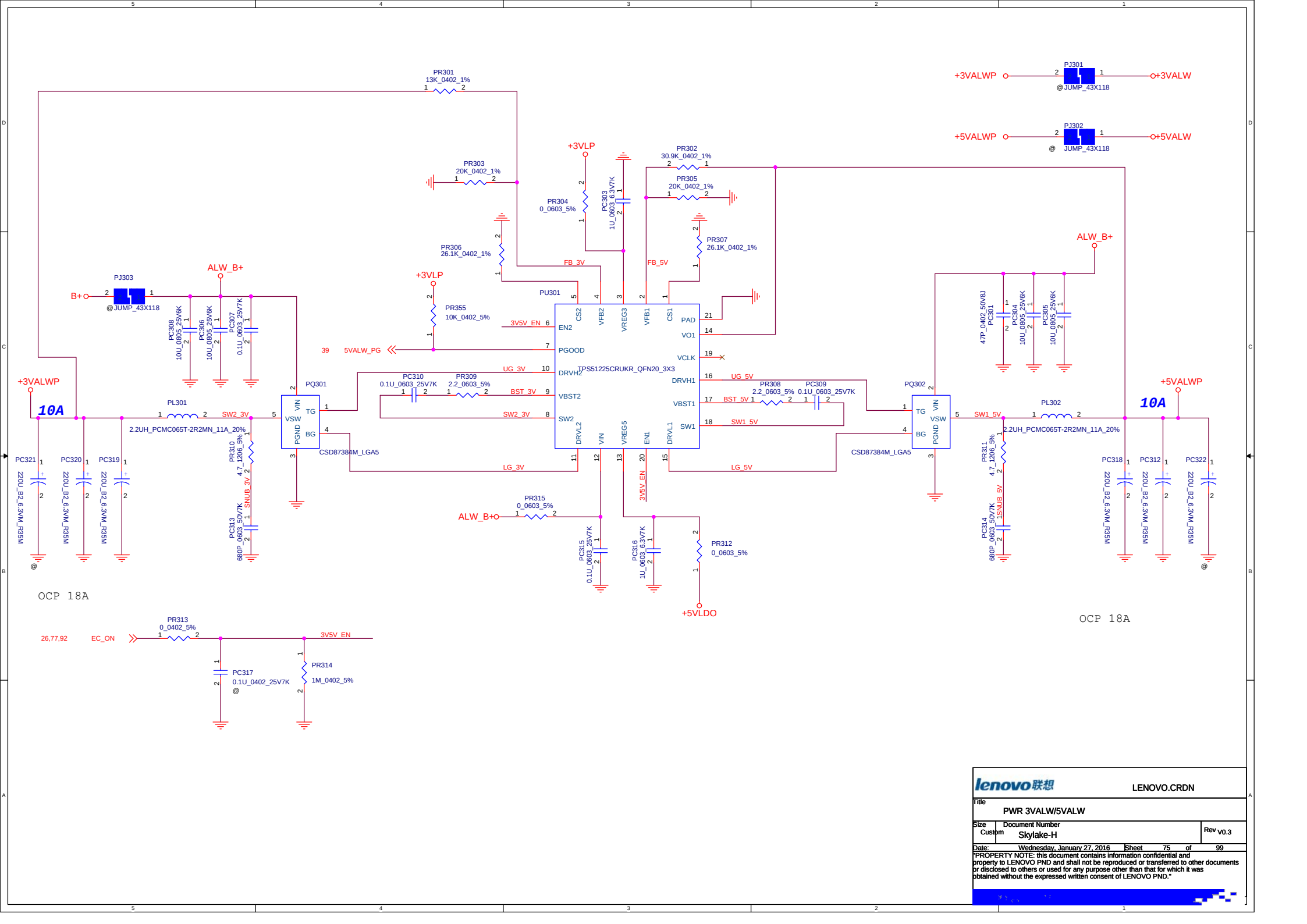
lenovo联想 LENOVO.CRDN

Title: PWR Trubo charger ISL95520

Size	Document Number	Rev
C	Skylake-H	V0.3

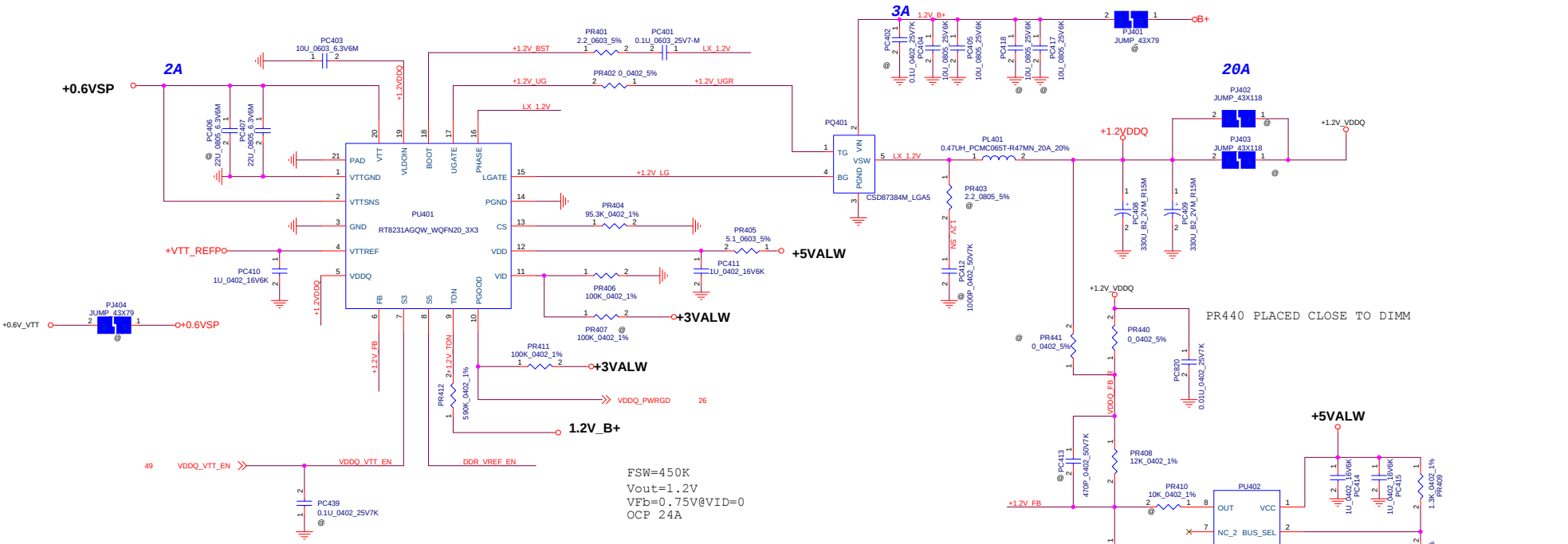
Date: Wednesday, January 27, 2016 Sheet 74 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



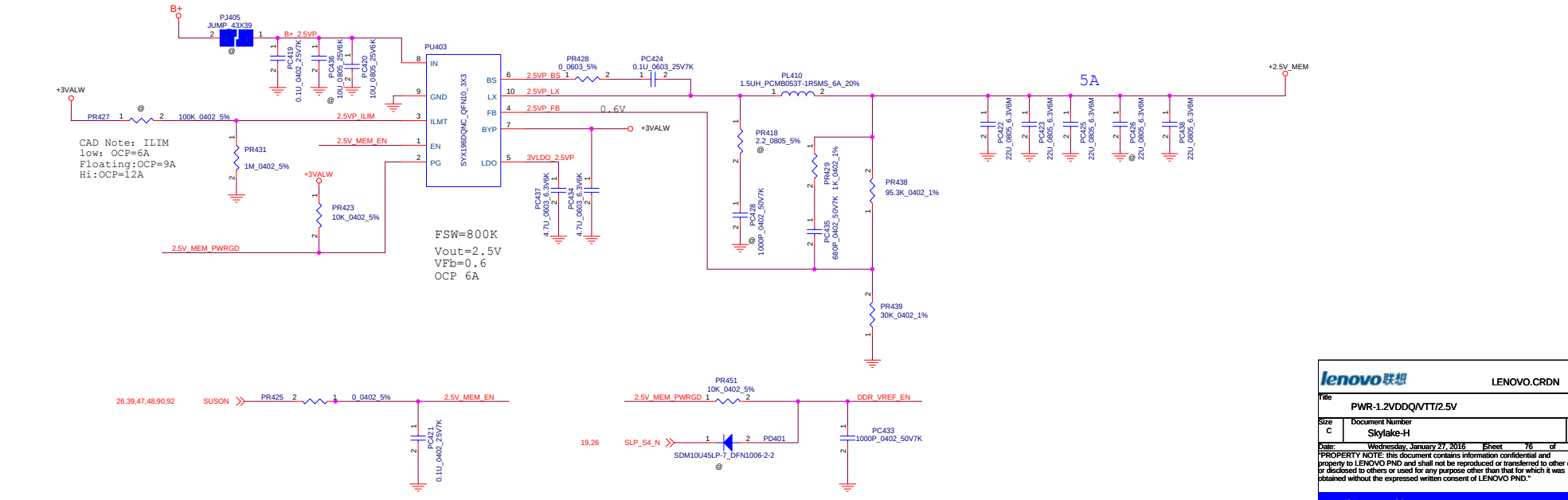
lenovo 联想	LENOVO.CRDN		
Title: PWR 3VALW/5VALW			
Size: Custom	Document Number: Skylake-H		Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 75 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



STATE	SUSON	MAINON	+1.2V_VDDQ	+0.6V_VTT
S0	HI	HI	ON	ON
S3	HI	LOW	ON	OFF(HighI-Z)
S5	LOW	LOW	OFF(Discharge)	OFF(Discharge)

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%



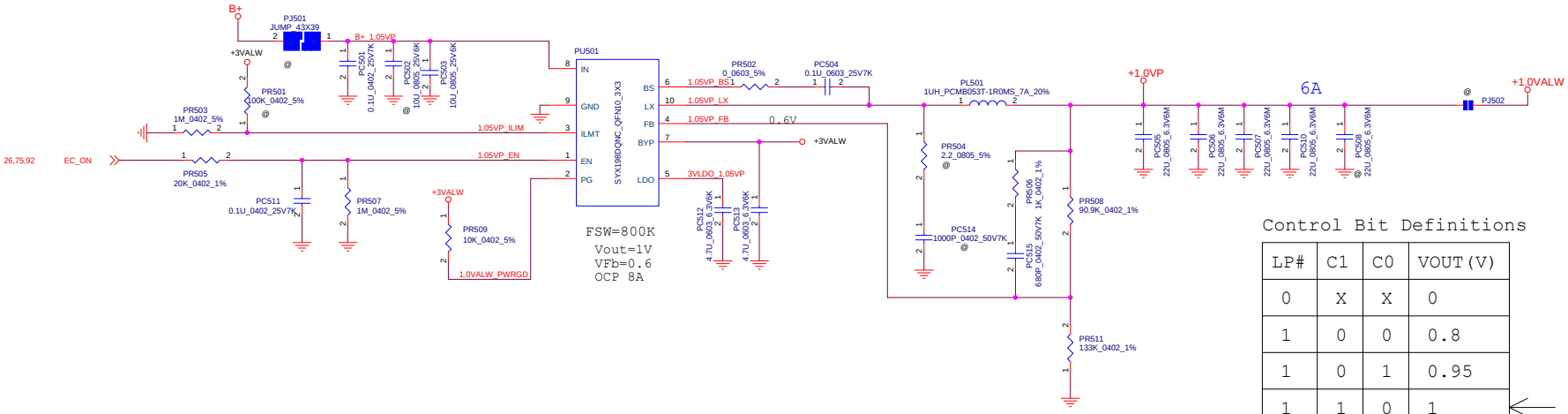
lenovo联想 LENOVO.CRDN

Title: PWR-1.2VDDQ/VTT/2.5V

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 76 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1
1	1	1	1.05

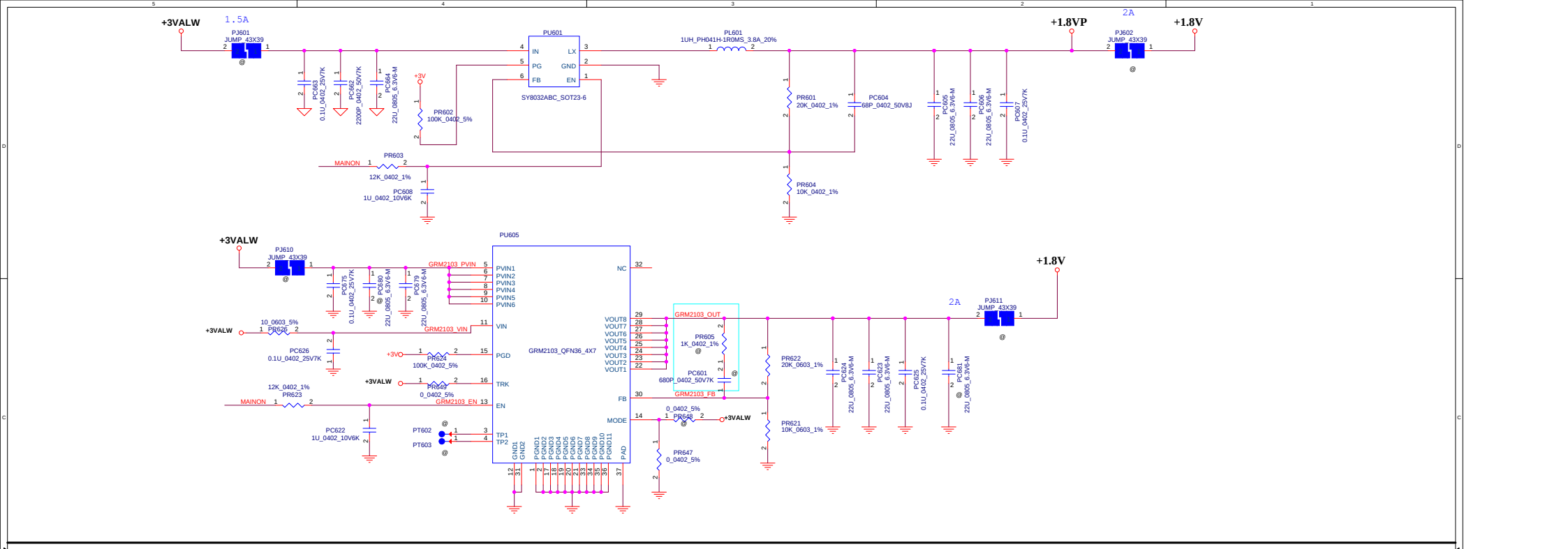
lenovo联想 LENOVO.CRDN

Title: PWR 1.0V/VCCEDRAM/EPIO

Size: C | Document Number: Skylake-H | Rev: V0.3

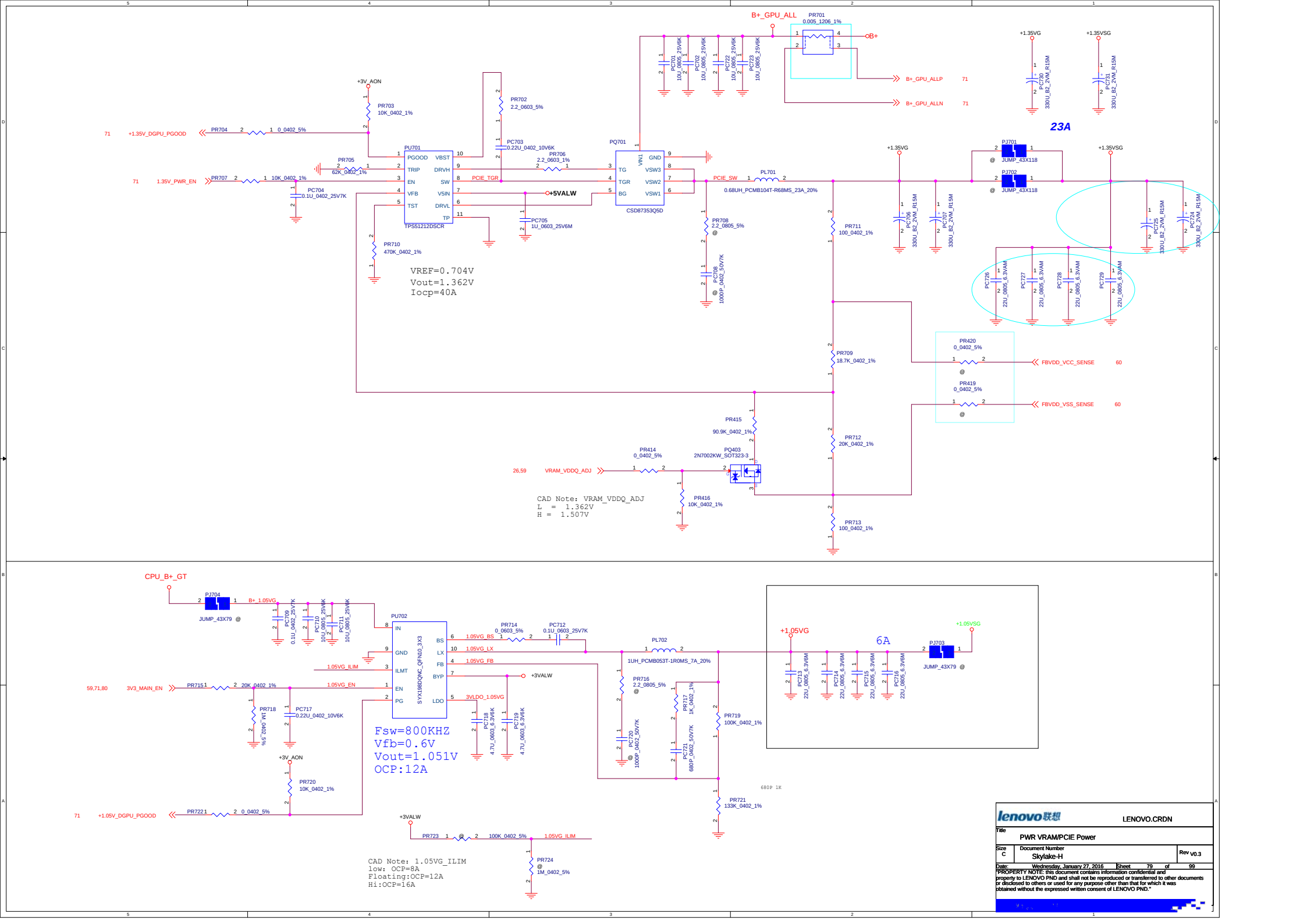
Date: Wednesday, January 27, 2016 | Sheet 77 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



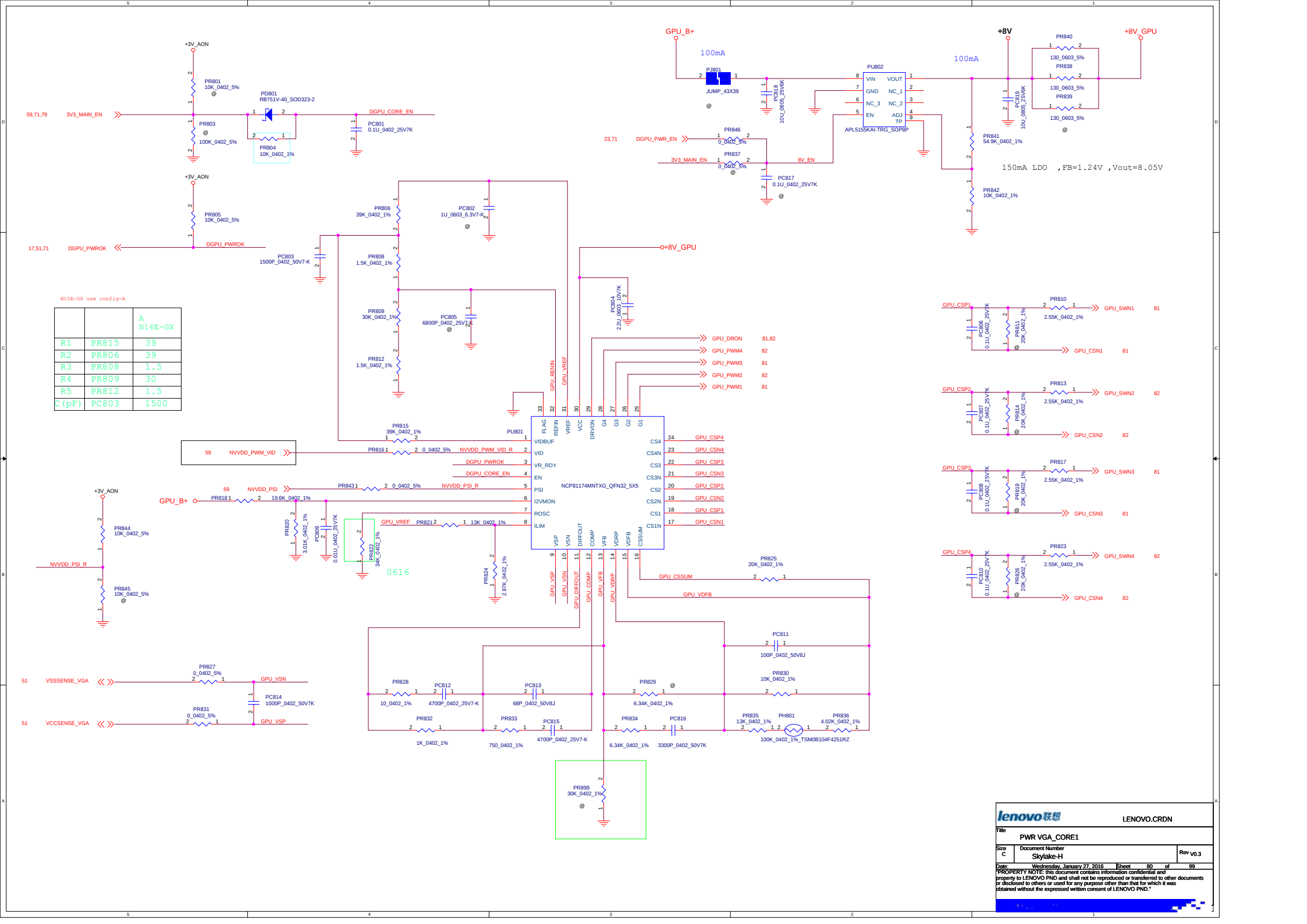
lenovo联想		LENOVO.CRDN	
Title	PWR 1.8V/1.2V/12V Boost		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 78 of 99		

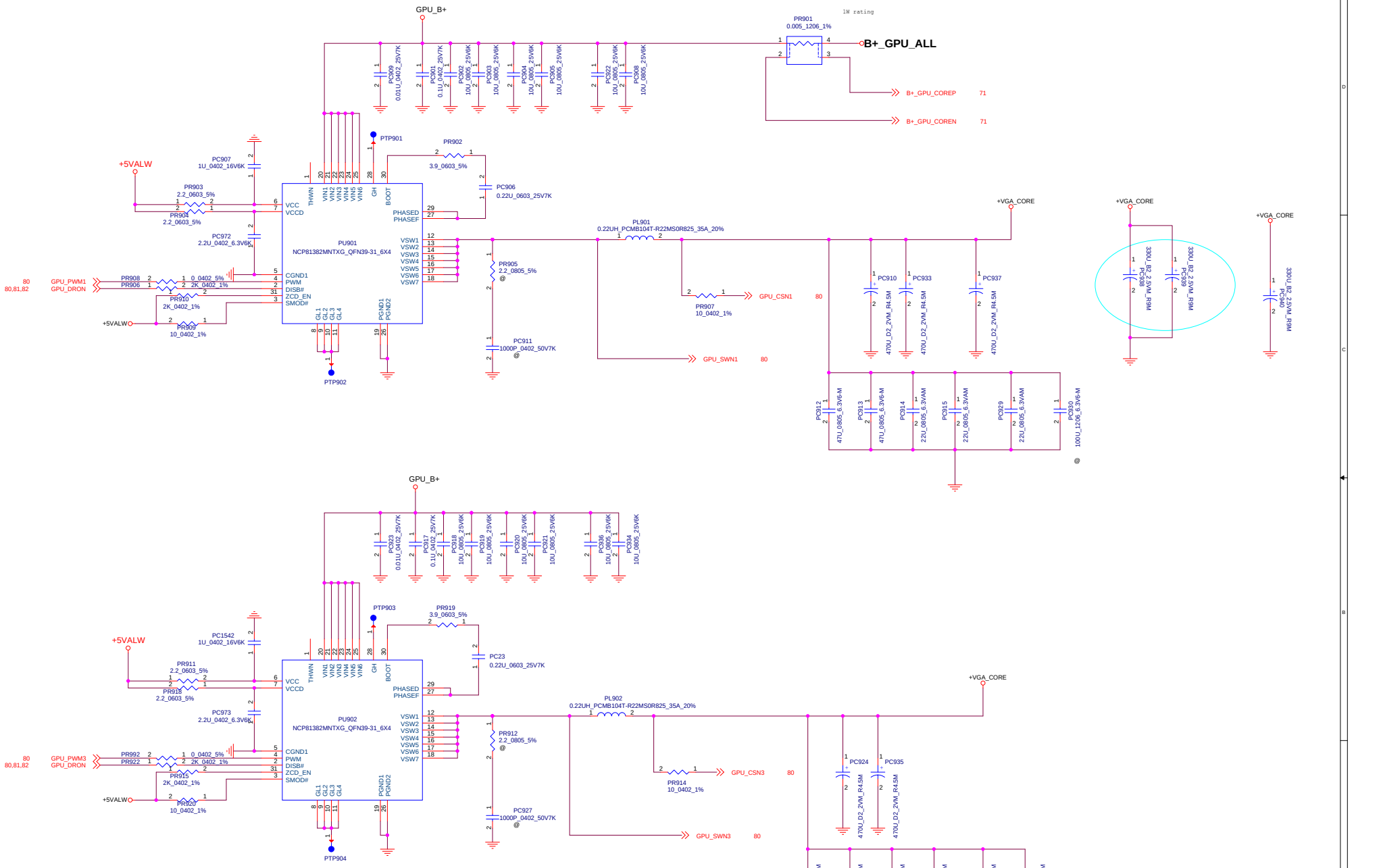
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想		LENOVO.CRDN	
Title	PWR VRAM/PCIE Power		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 79 of 99		

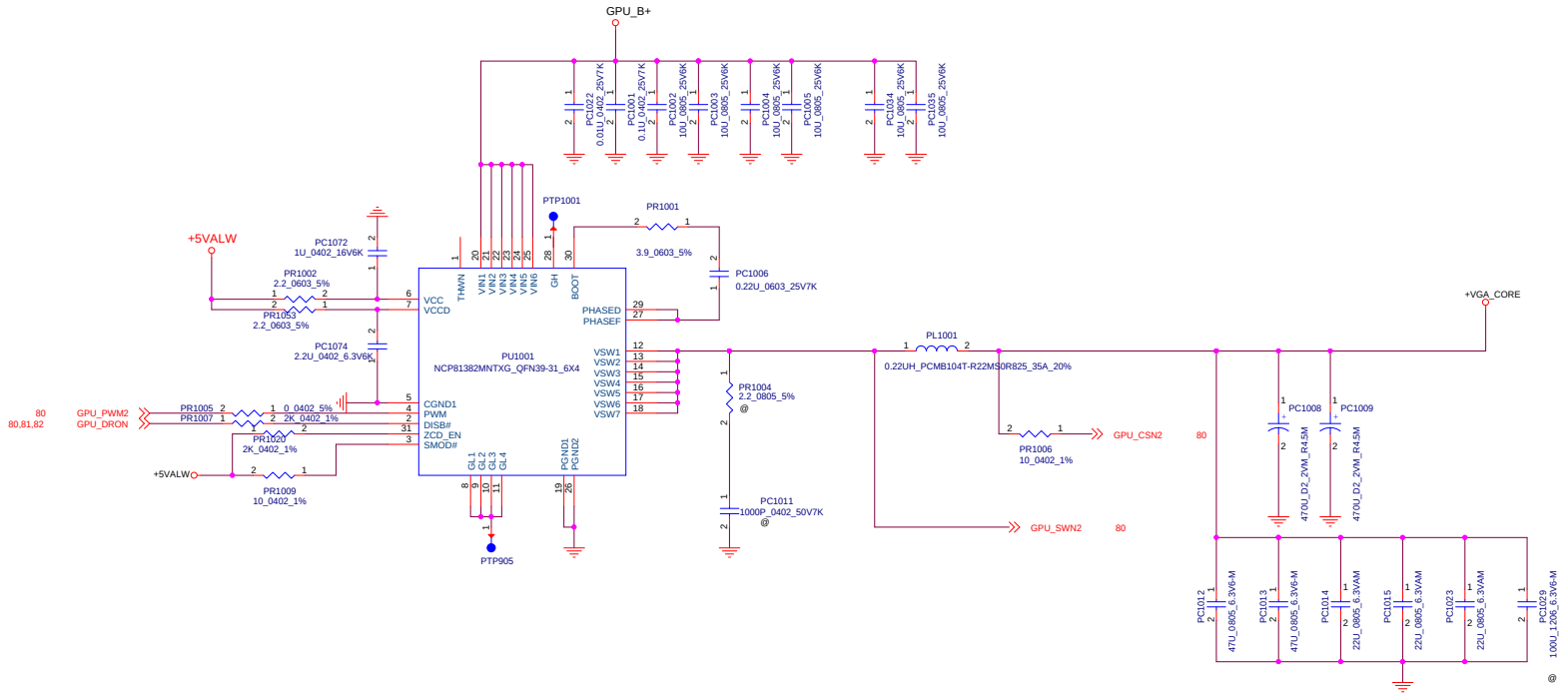
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

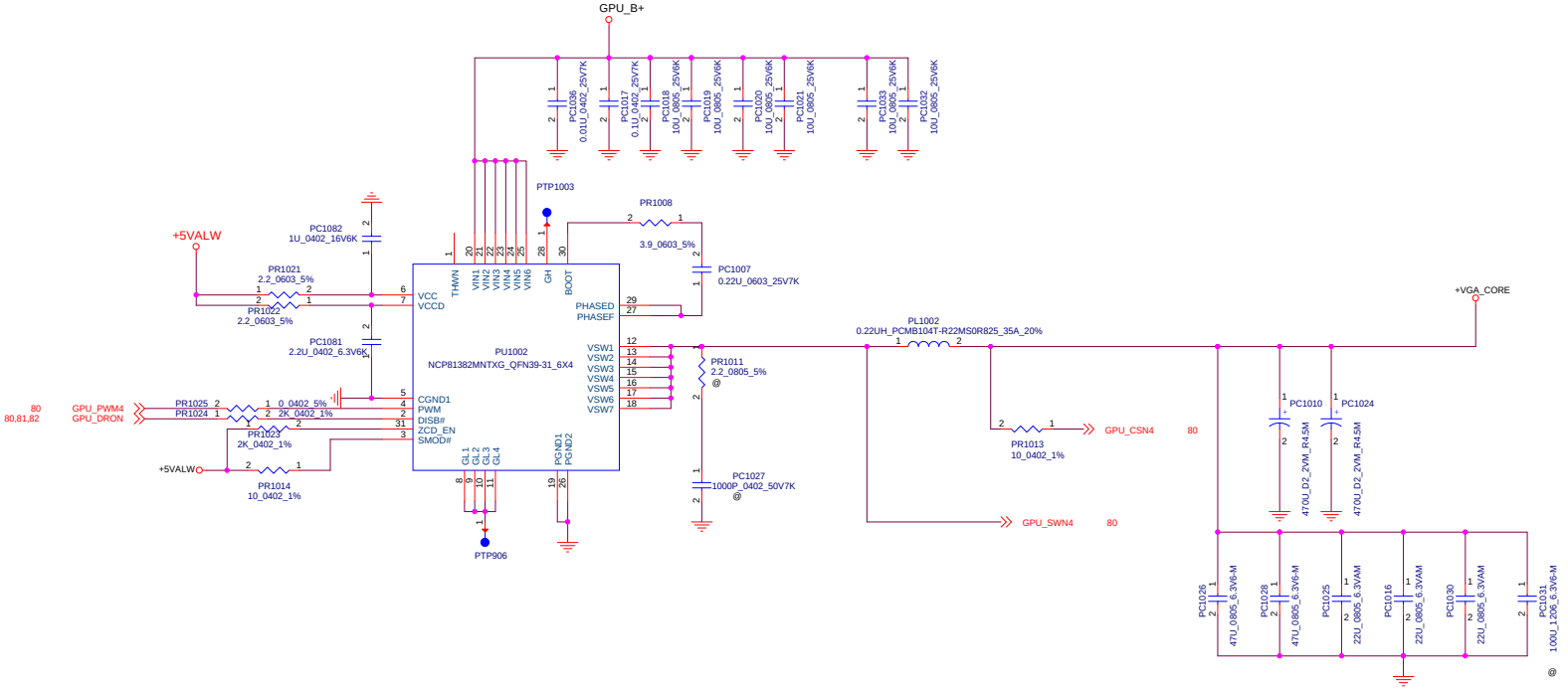

GPU_B+
100mA
PJ801
JUMP_43X39
PC818
10U_0805_25V6K
PU802
VIN
VOUT
GND
NC_1
NC_3
NC_2
EN
ADJ
TP
APL5155KAI-TRG_SOP8P
+8V
100mA
PR840
130_0603_5%
PR838
130_0603_5%
PR839
130_0603_5%
+8V_GPU
PC819
10U_0805_25V6K
PR841
54.9K_0402_1%
PR842
10K_0402_1%
150mA LDO ,FB=1.24V ,Vout=8.05V
23,71
DGPU_PWR_EN
PR846
0_0402_5%
3V3_MAIN_EN
PR837
0_0402_5%
8V_EN
PC817
0.1U_0402_25V7K
+3V_AON
PR801
10K_0402_5%
59,71,79
3V3_MAIN_EN
PD801
RB751V-40_SOD323-2
DGPU_CORE_EN
PR803
100K_0402_5%
PR804
10K_0402_1%
PC801
0.1U_0402_25V7K
+3V_AON
PR805
10K_0402_5%
17,51,71
DGPU_PWROK
PC803
1500P_0402_50V7-K
PR806
39K_0402_1%
PC802
1U_0603_6.3V7-K
PR808
1.5K_0402_1%
PR809
30K_0402_1%
PC805
6800P_0402_25V7-K
PR812
1.5K_0402_1%
+8V_GPU
PC804
2.2U_0603_10V7K
N15E-GX use config-A
A
N16E-GX
R1 PR815 39
R2 PR806 39
R3 PR808 1.5
R4 PR809 30
R5 PR812 1.5
C(pF) PC803 1500
PR815
39K_0402_1%
59
NVVDD_PWM_VID
PR816
0_0402_5%
NVVDD_PWM_VID_R
PU801
VIDBUF
VID
VR_RDY
EN
PSI
I2VMON
ROSC
ILIM
FLAG
REFIN
VREF
VCC
DRVON
G4
G3
G2
G1
NCP81174MNTXG_QFN32_5X5
CS4
CS4N
CS3
CS3N
CS2
CS2N
CS1
CS1N
VSP
VSN
DIFFOUT
COMP
VFB
VDRP
VDFB
CSSUM
GPU_RENIN
GPU_VREF
GPU_DRON 81,82
GPU_PWM4 82
GPU_PWM3 81
GPU_PWM2 82
GPU_PWM1 81
GPU_CSP4
GPU_CSN4
GPU_CSP3
GPU_CSN3
GPU_CSP2
GPU_CSN2
GPU_CSP1
GPU_CSN1
DGPU_PWROK
DGPU_CORE_EN
59
NVVDD_PSI
PR843
0_0402_5%
NVVDD_PSI_R
GPU_B+
PR818
19.6K_0402_1%
PR820
3.01K_0402_1%
PC809
0.01U_0402_25V7K
GPU_VREF
PR821
13K_0402_1%
PR822
34K_0402_1%
0616
PR824
2.87K_0402_1%
+3V_AON
PR844
10K_0402_5%
NVVDD_PSI_R
PR845
10K_0402_5%
GPU_VSP
GPU_VSN
GPU_DIFFOUT
GPU_COMP
GPU_VFB
GPU_VDRP
GPU_CSSUM
GPU_VDFB
PR825
20K_0402_1%
PC811
100P_0402_50V8J
PR830
10K_0402_1%
PR827
0_0402_5%
51
VSSSENSE_VGA
GPU_VSN
PC814
1000P_0402_50V7K
PR831
0_0402_5%
51
VCCSENSE_VGA
GPU_VSP
PR828
10_0402_1%
PC812
4700P_0402_25V7-K
PC813
68P_0402_50V8J
PR829
6.34K_0402_1%
PR832
1K_0402_1%
PR833
750_0402_1%
PC815
4700P_0402_25V7-K
PR834
6.34K_0402_1%
PC816
3300P_0402_50V7K
PR835
13K_0402_1%
PH801
100K_0402_1%_TSM0B104F4251RZ
PR836
4.02K_0402_1%
PR899
30K_0402_1%
PR810
2.55K_0402_1%
PC806
0.1U_0402_25V7K
PR811
20K_0402_1%
GPU_SWN1 81
GPU_CSN1 81
PR813
2.55K_0402_1%
PC807
0.1U_0402_25V7K
PR814
20K_0402_1%
GPU_SWN2 82
GPU_CSN2 82
PR817
2.55K_0402_1%
PC808
0.1U_0402_25V7K
PR819
20K_0402_1%
GPU_SWN3 81
GPU_CSN3 81
PR823
2.55K_0402_1%
PC810
0.1U_0402_25V7K
PR826
20K_0402_1%
GPU_SWN4 82
GPU_CSN4 82
lenovo联想
LENOVO.CRDN
Title
PWR VGA_CORE1
Size C
Document Number
Skylake-H
Rev V0.3
Date: Wednesday, January 27, 2016
Sheet 80 of 99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN	
Title	PWR VGA_CORE2	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 81 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."





lenovo联想 LENOVO.CRDN

Title: PWR VGA_CORE3

Size: C | Document Number: Skylake-H | Rev: V0.3

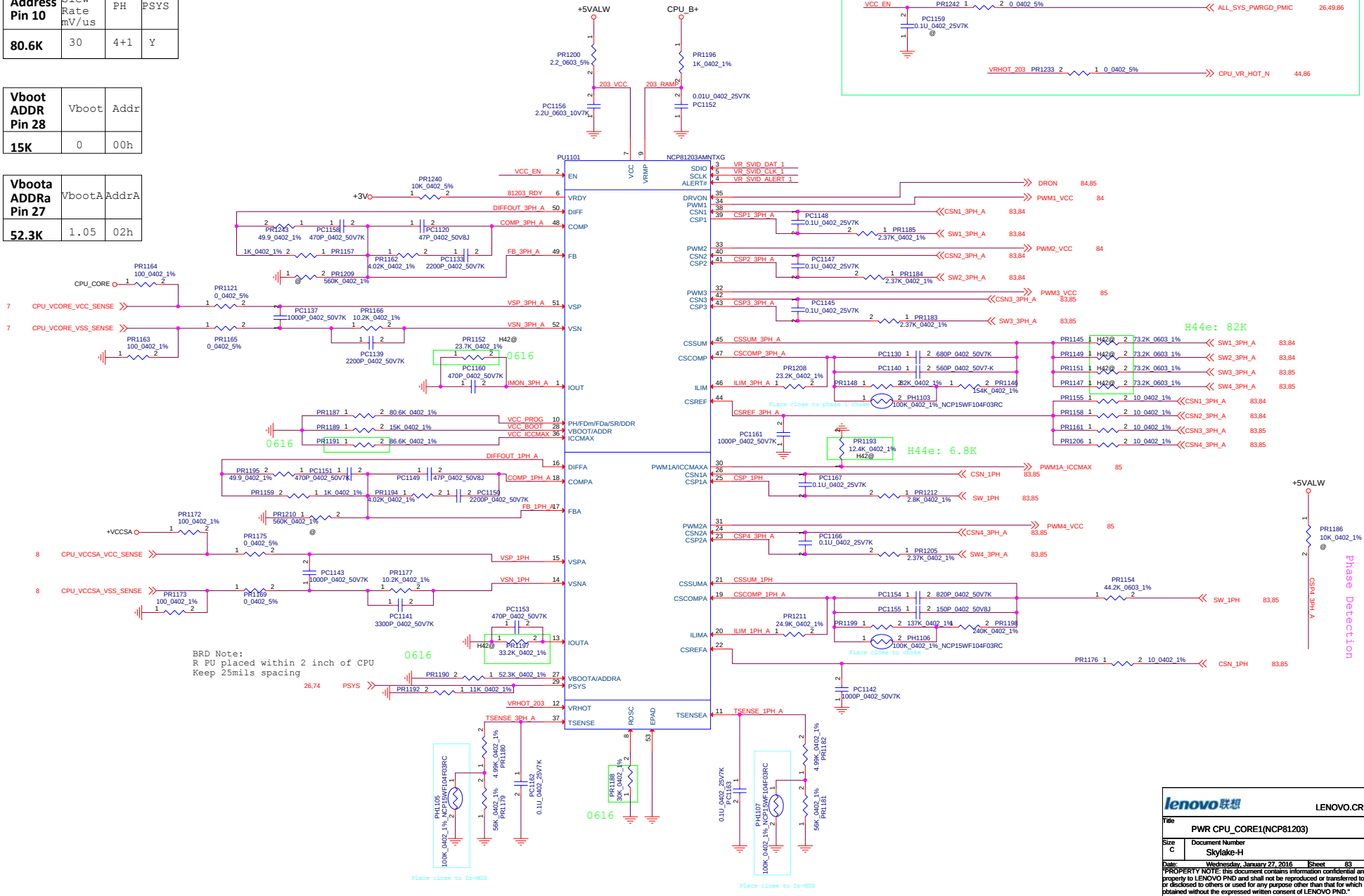
Date: Wednesday, January 27, 2016 | Sheet 82 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

Address Pin 10	Slew Rate mV/us	PH	PSYS
80.6K	30	4+1	Y

Vboot ADDR Pin 28	Vboot	Addr
15K	0	00h

Vboota ADDRa Pin 27	VbootA	AddrA
52.3K	1.05	02h



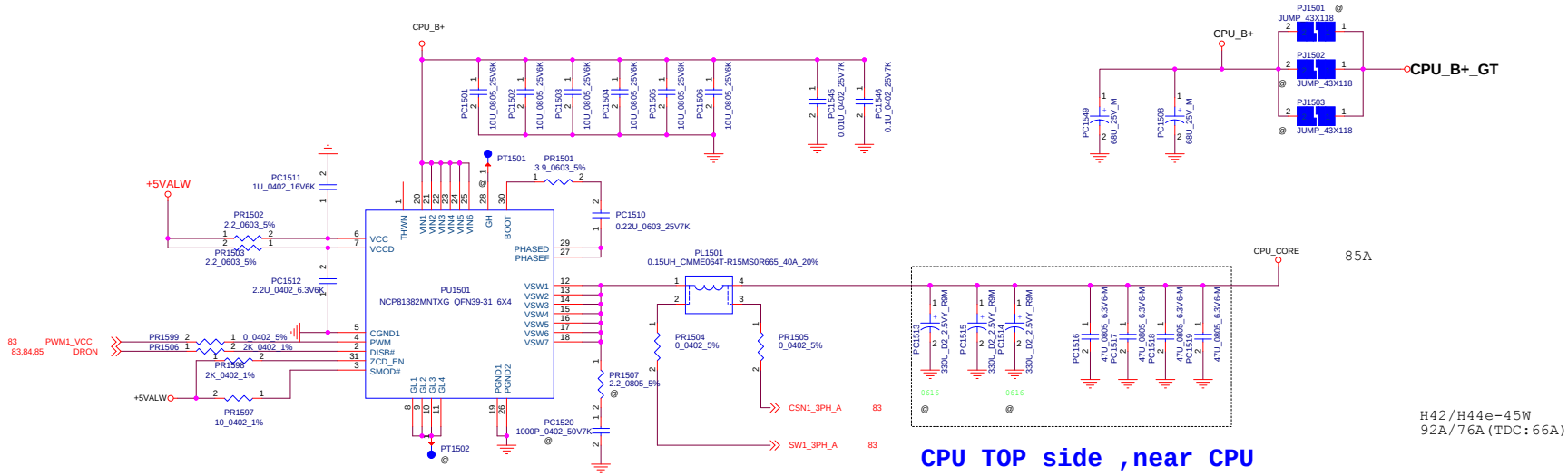
lenovo联想 LENOVO.CRDN

Title: PWR CPU_CORE1(NCP81203)

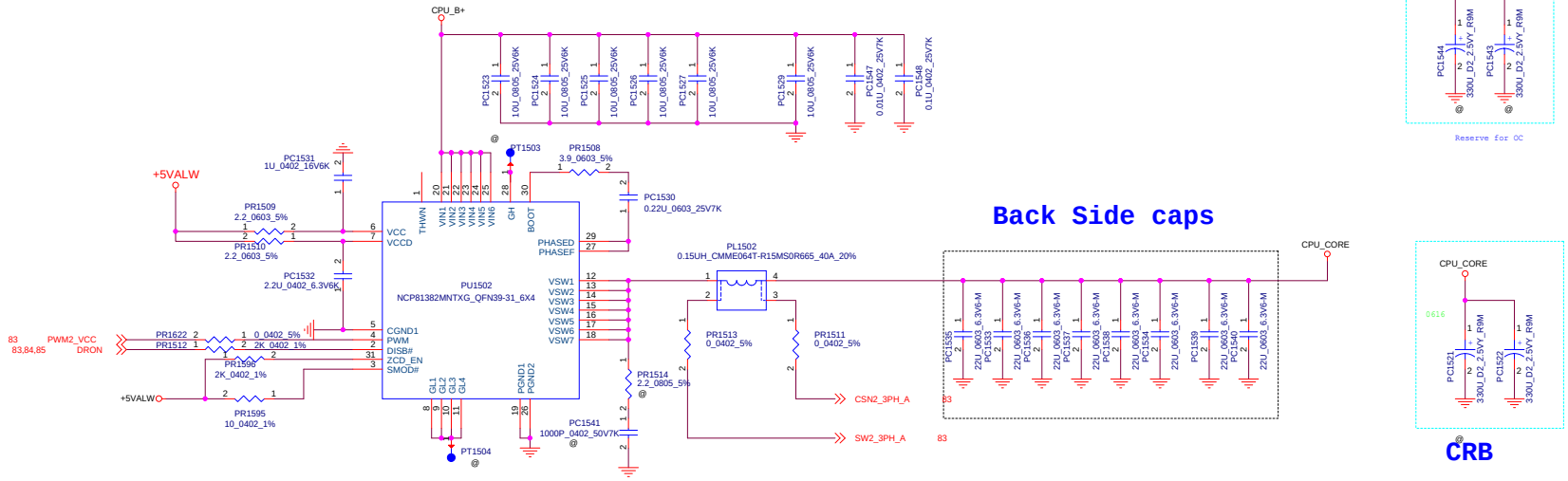
Size	Document Number	Rev
C	Skylake-H	V0.3

Date: Wednesday, January 27, 2016 Sheet 83 of 99

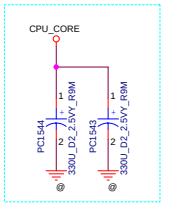
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



CPU TOP side ,near CPU



Back Side caps



CRB

	CPU BACK				CPU TOP	
CRB	220	22	10	1	220	47
	2V	0603	0402	0201	2V	0805
pcs	3	8	28	63	2	4

1,PDG 3*220uF TOP ,no Back; follow CRB/PDG;
2,47uF,22uF follow CRB;
3,Reserve 16pcs 22uF for OC;
4,10uF/1uF double check EE side
5,Total Cap double check with Vendor

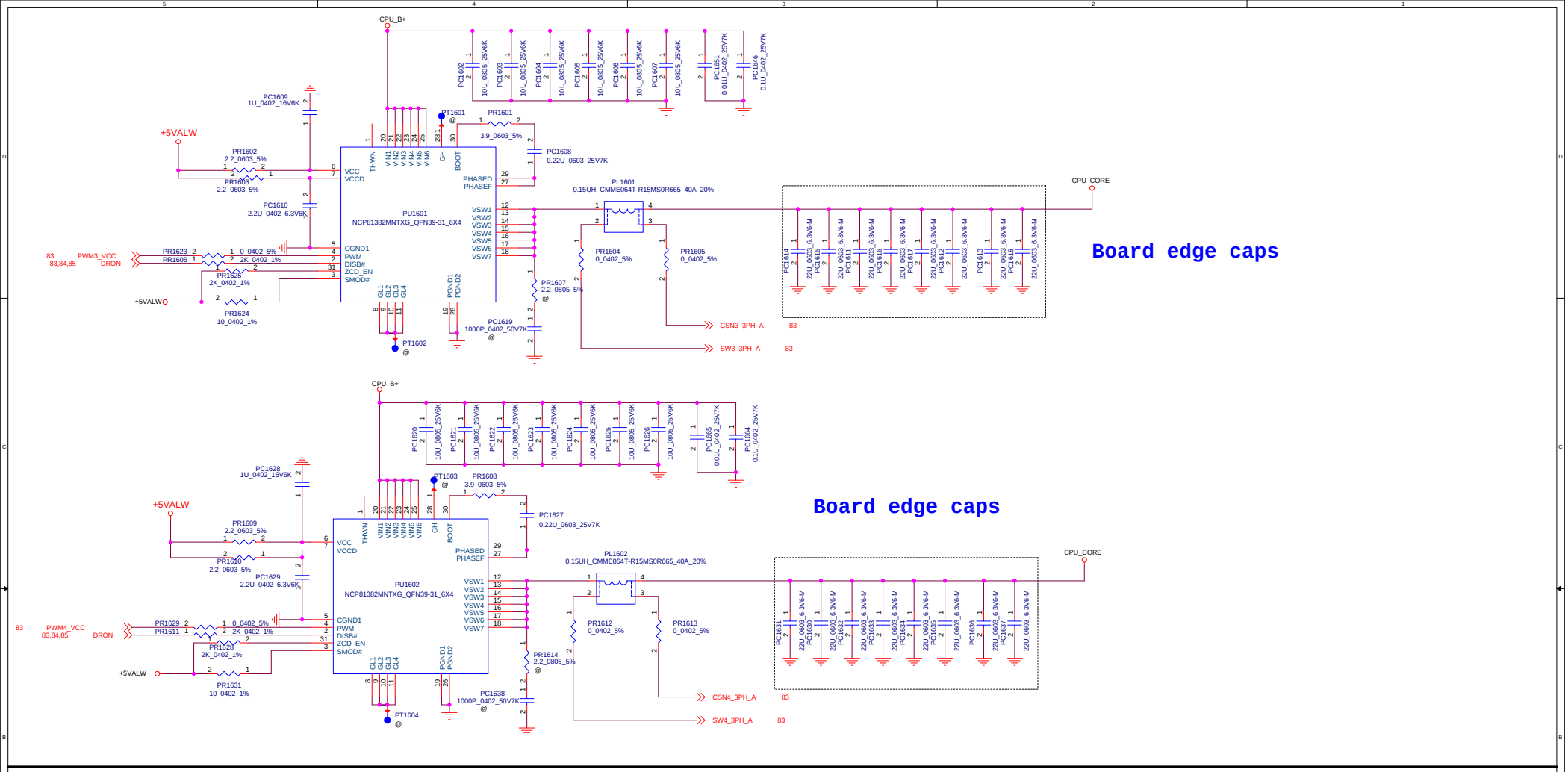
lenovo联想 LENOVO.CRDN

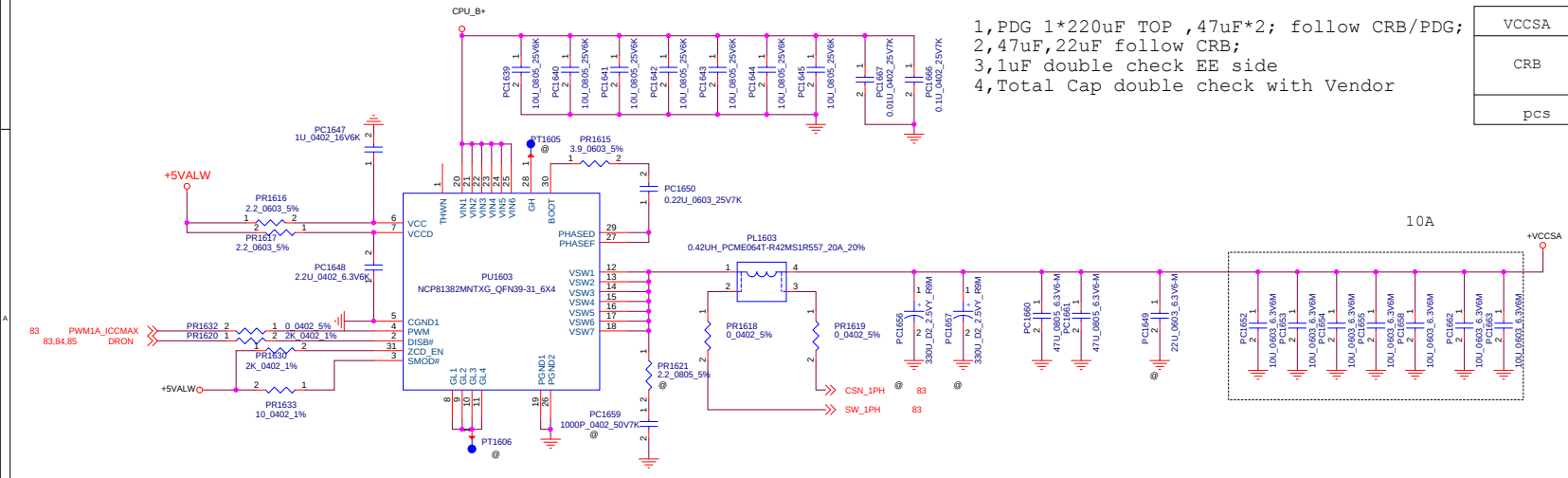
Title: PWR CPU_CORE2(NCP81382)

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 84 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."





1,PDG 1*220uF TOP ,47uF*2; follow CRB/PDG;
2,47uF,22uF follow CRB;
3,1uF double check EE side
4,Total Cap double check with Vendor

VCCSA	CPU BACK				CPU TOP	
CRB	220	47	10	1	220	22
	2V	0805	0402	0201	2V	0603
pcs	0	1	7	3	2	1

lenovo联想	LENOVO.CRDN		
Title	PWR CPU_CORE3(NCP81382)		
Size C	Document Number Skylake-H		Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 85 of 99		

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

SKL H42

Address Pin 10	Slew Rate mV/us	PH	PSYS
19.1K	30	2+0	N

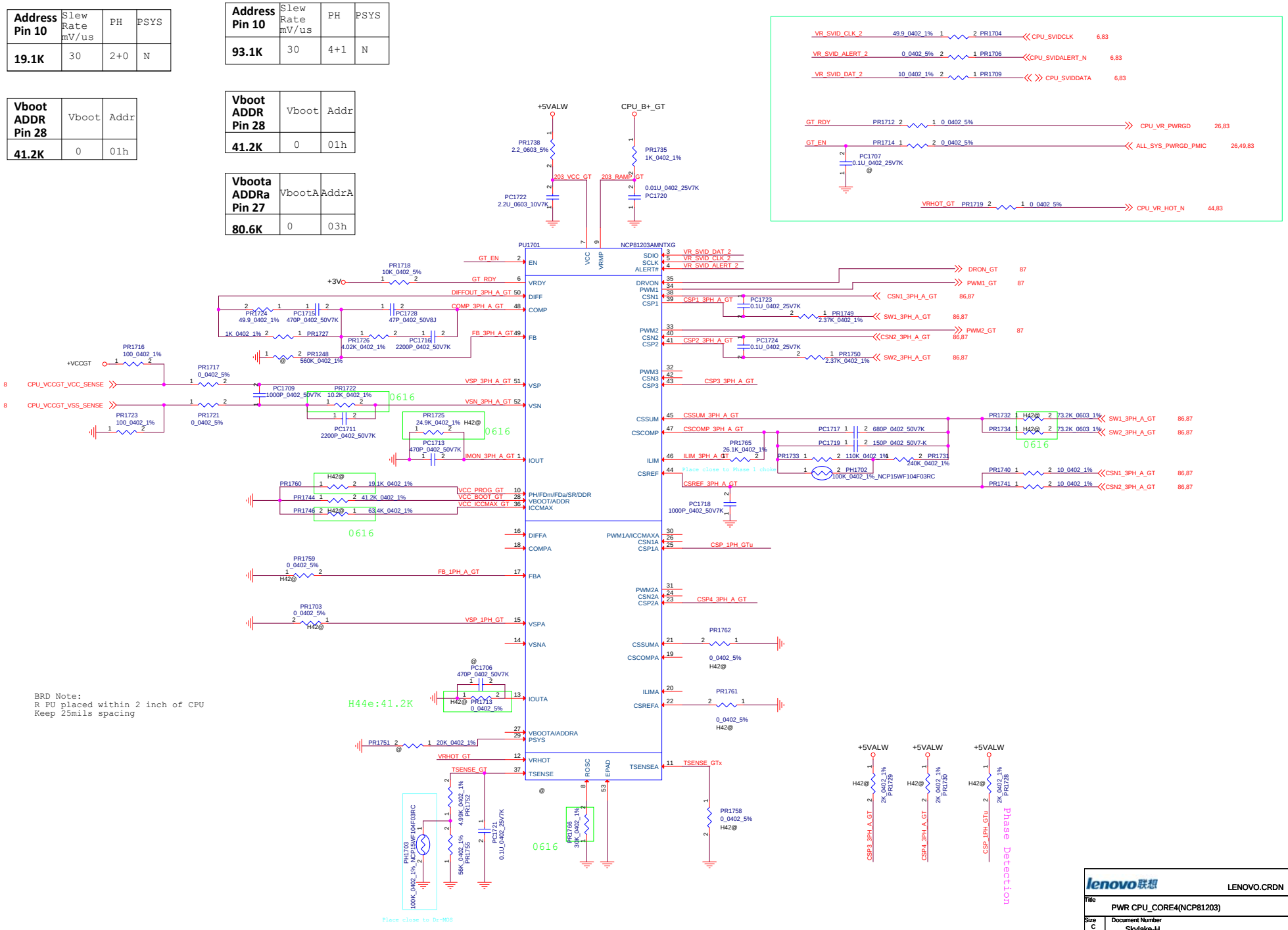
Vboot ADDR Pin 28	Vboot	Addr
41.2K	0	01h

SKL H44e

Address Pin 10	Slew Rate mV/us	PH	PSYS
93.1K	30	4+1	N

Vboot ADDR Pin 28	Vboot	Addr
41.2K	0	01h

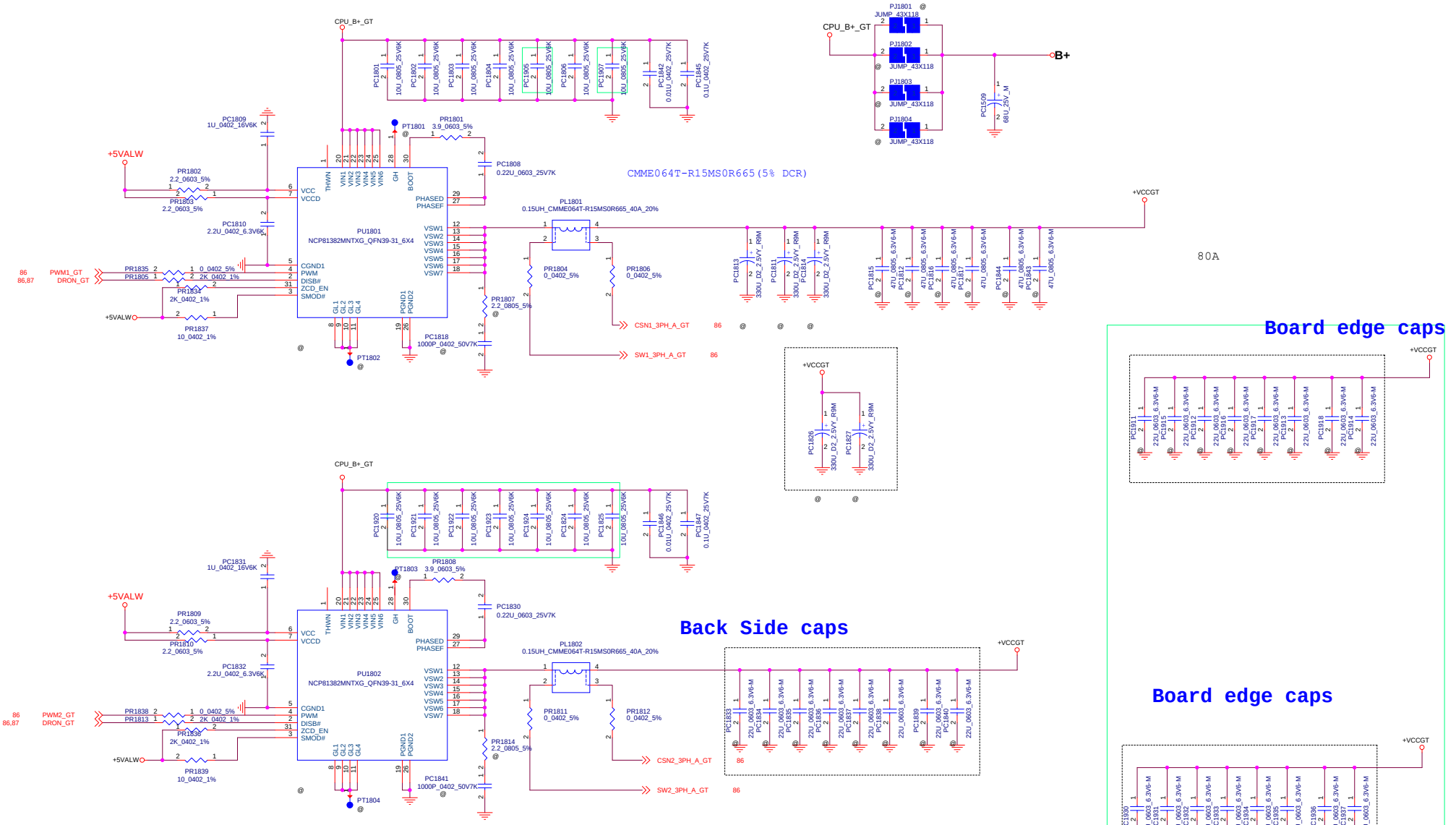
Vboota ADDRa Pin 27	VbootA	AddrA
80.6K	0	03h



Title	PWR CPU_CORE4(NCP81203)
Size	C
Document Number	Skylake-H
Rev	V0.3
Date	Wednesday, January 27, 2016
Sheet	86 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

LENOVO.CRDN



	CPU BACK				CPU TOP	
CRB	220	22	10	1	220	47
	2V	0603	0402	0201	2V	0805
pcs	3	8	35	6	4	6

1,PDG 4*220uF TOP ,no Back; follow CRB/PDG;
2,47uF,22uF follow CRB;
3,Reserve more 16pcs 22uF;
4,10uF/1uF double check EE side
5,Total Cap double check with Vendor

lenovo联想 LENOVO.CRDN

Title: PWR CPU_CORE5(NCP81382)

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 87 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

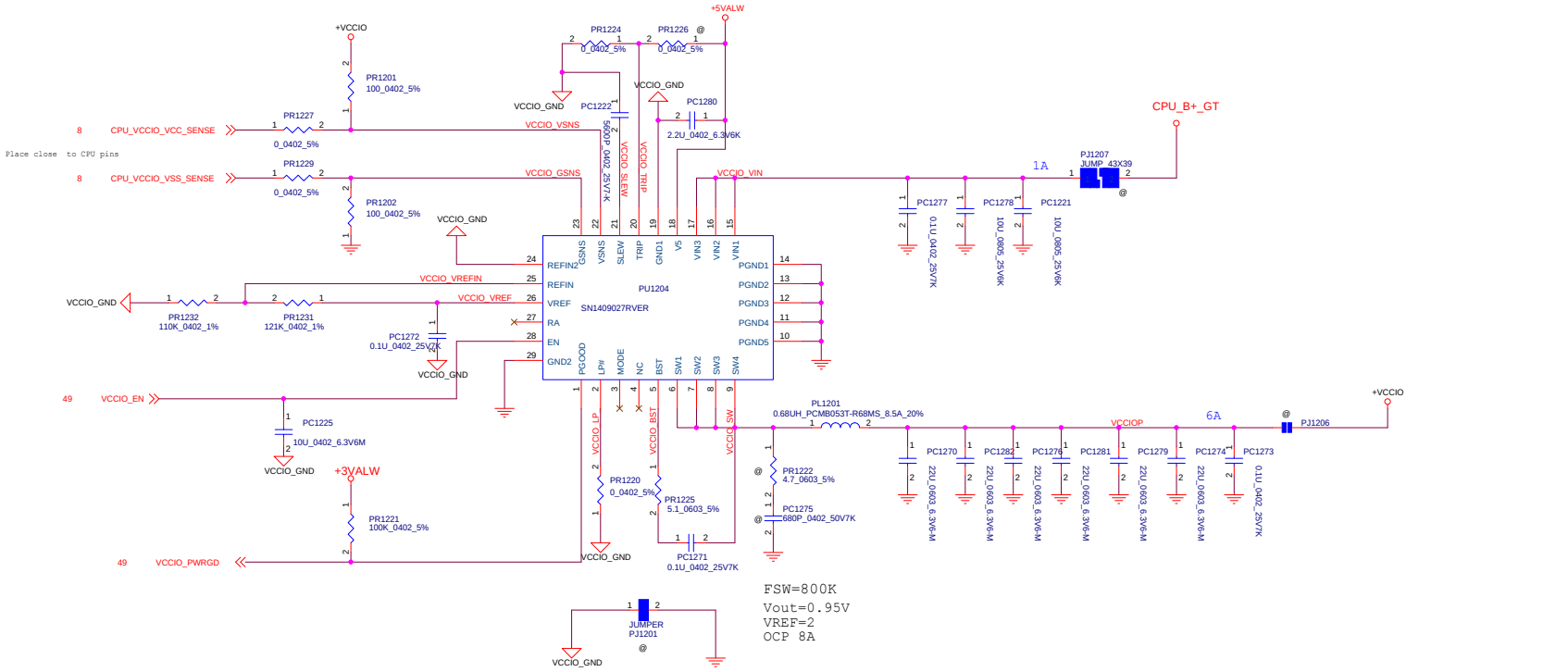
LENOVO.CRDN

Title: PWR CPU_CORE6(NCP81382)

Size: C | Document Number: Skylake-H | Rev: V0.3

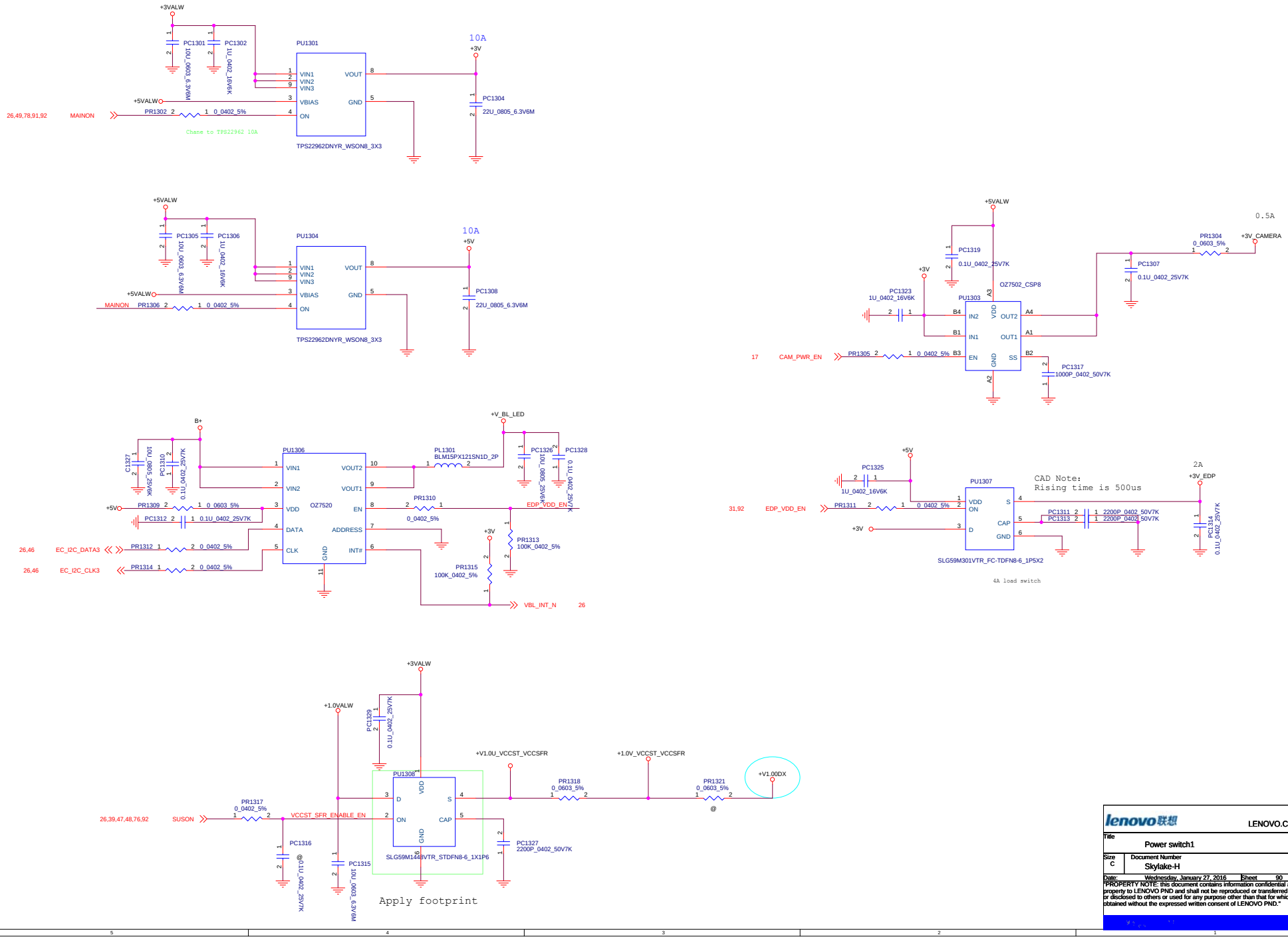
Date: Wednesday, January 27, 2016 | Sheet 88 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



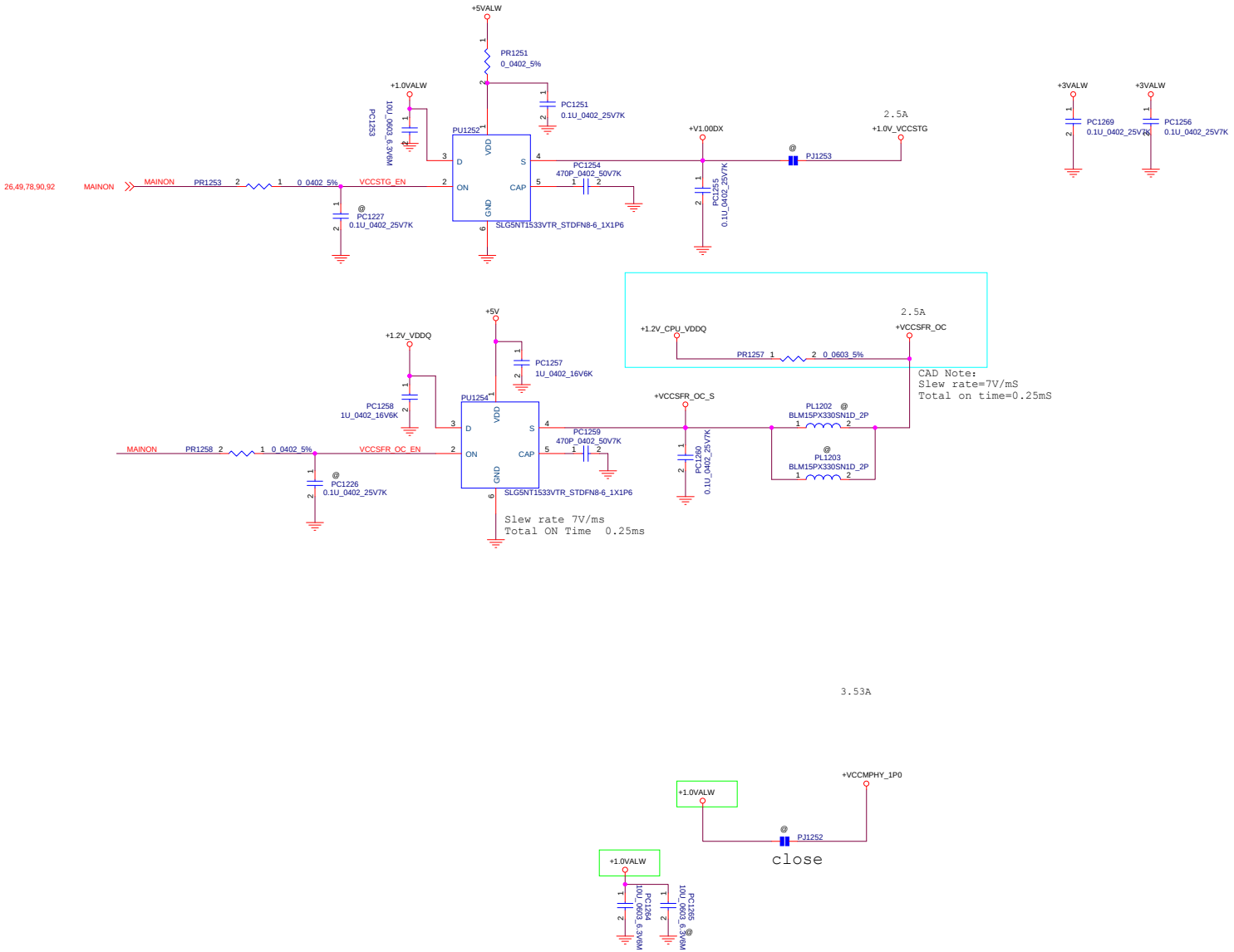
lenovo联想	LENOVO.CRDN	
Title: PWR VCCIO		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 89 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



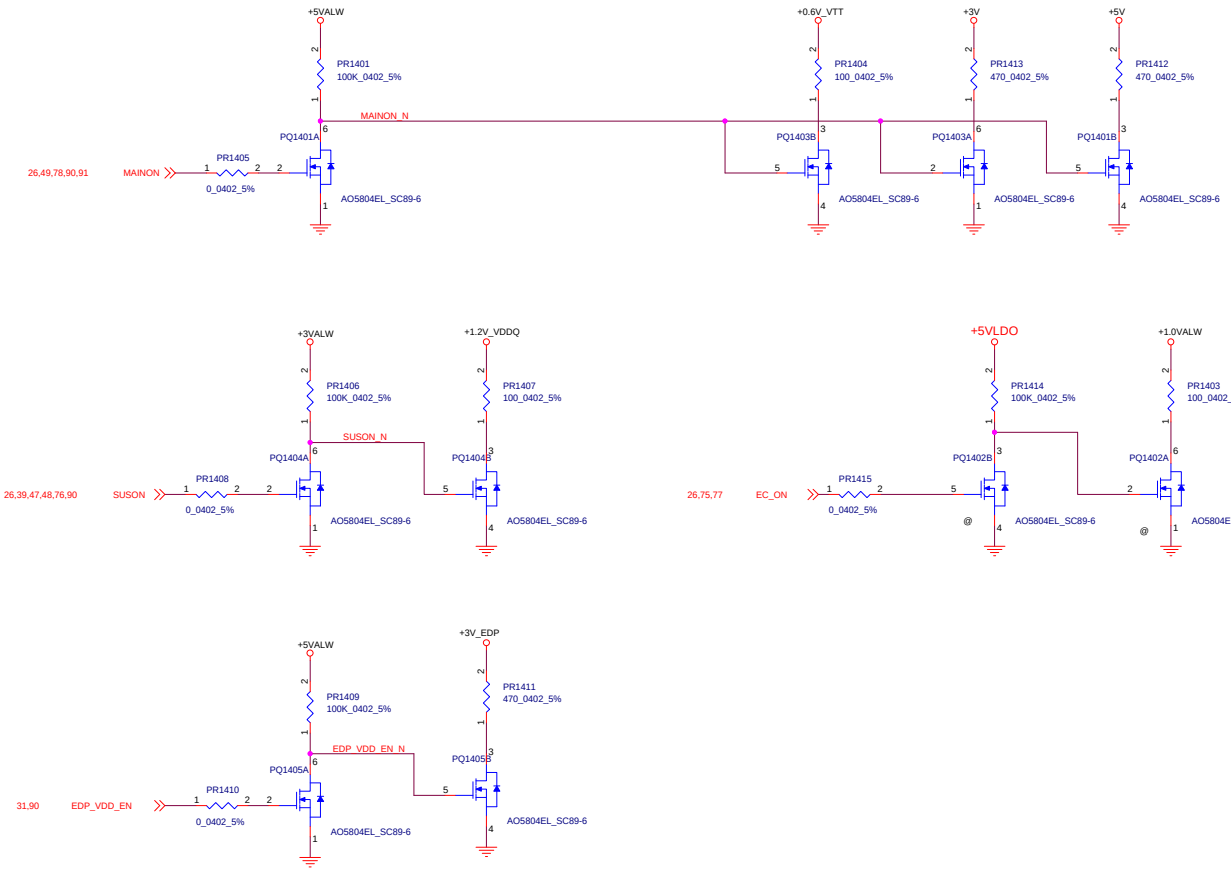
lenovo联想	LENOVO.CRDN	
Title	Power switch1	
Size C	Document Number Skylake-H	Rev V0.3
Date: Wednesday, January 27, 2016	Sheet 90 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



lenovo联想	LENOVO.CRDN	
Title: Power switch2		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 91 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."



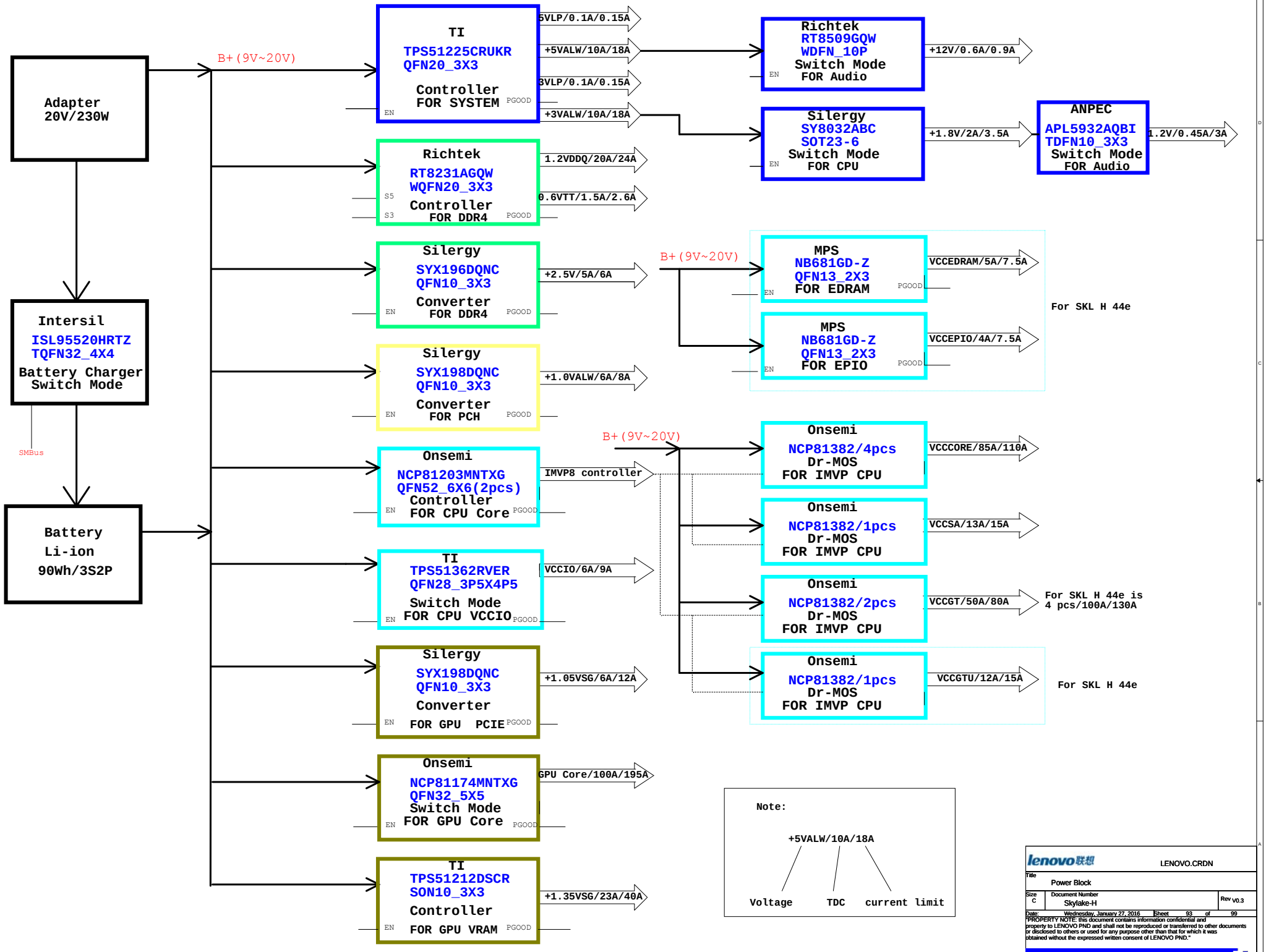
lenovo联想 LENOVO.CRDN

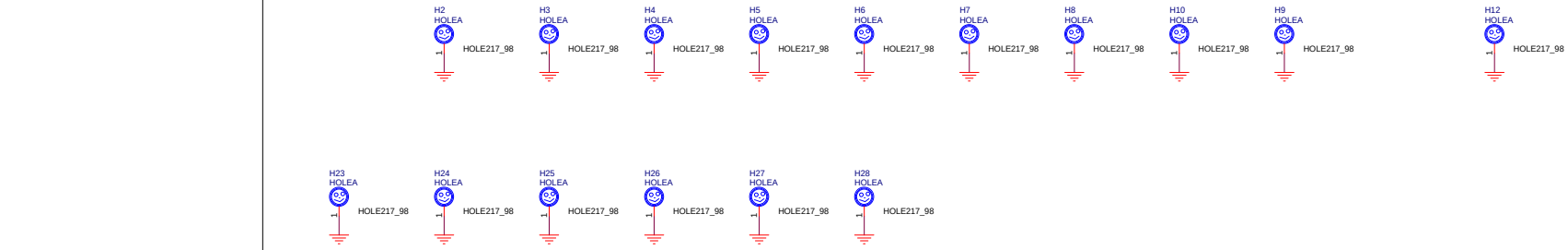
Title: KB/TP/RTC

Size	Document Number	Rev
C	Skylake-H	V0.3

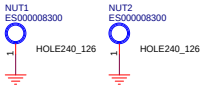
Date: Wednesday, January 27, 2016 Sheet 92 of 99

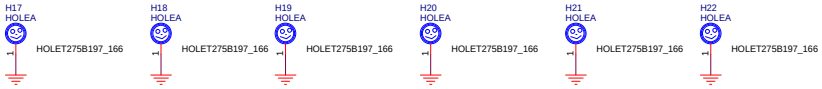
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."


Adapter
20V/230W
B+(9V~20V)
Intersil
ISL95520HRTZ
TQFN32_4X4
Battery Charger
Switch Mode
SMBus
Battery
Li-ion
90Wh/3S2P
TI
TPS51225CRUKR
QFN20_3X3
Controller
FOR SYSTEM
EN
PGOOD
5VLP/0.1A/0.15A
+5VALW/10A/18A
3VLP/0.1A/0.15A
+3VALW/10A/18A
Richtek
RT8509GQW
WDFN_10P
Switch Mode
FOR Audio
EN
+12V/0.6A/0.9A
Silergy
SY8032ABC
SOT23-6
Switch Mode
FOR CPU
EN
+1.8V/2A/3.5A
ANPEC
APL5932AQBI
TDFN10_3X3
Switch Mode
FOR Audio
1.2V/0.45A/3A
Richtek
RT8231AGQW
WQFN20_3X3
Controller
FOR DDR4
S5
S3
PGOOD
1.2VDDQ/20A/24A
0.6VTT/1.5A/2.6A
Silergy
SYX196DQNC
QFN10_3X3
Converter
FOR DDR4
EN
PGOOD
+2.5V/5A/6A
B+(9V~20V)
MPS
NB681GD-Z
QFN13_2X3
FOR EDRAM
EN
PGOOD
VCCEDRAM/5A/7.5A
MPS
NB681GD-Z
QFN13_2X3
FOR EPIO
EN
PGOOD
VCCEPIO/4A/7.5A
For SKL H 44e
Silergy
SYX198DQNC
QFN10_3X3
Converter
FOR PCH
EN
PGOOD
+1.0VALW/6A/8A
B+(9V~20V)
Onsemi
NCP81203MNTXG
QFN52_6X6(2pcs)
Controller
FOR CPU Core
EN
PGOOD
IMVP8 controller
Onsemi
NCP81382/4pcs
Dr-MOS
FOR IMVP CPU
VCCCORE/85A/110A
Onsemi
NCP81382/1pcs
Dr-MOS
FOR IMVP CPU
VCCSA/13A/15A
TI
TPS51362RVER
QFN28_3P5X4P5
Switch Mode
FOR CPU VCCIO
EN
PGOOD
VCCIO/6A/9A
Onsemi
NCP81382/2pcs
Dr-MOS
FOR IMVP CPU
VCCGT/50A/80A
For SKL H 44e is
4 pcs/100A/130A
Onsemi
NCP81382/1pcs
Dr-MOS
FOR IMVP CPU
VCCGTU/12A/15A
For SKL H 44e
Silergy
SYX198DQNC
QFN10_3X3
Converter
FOR GPU PCIE
EN
PGOOD
+1.05VSG/6A/12A
Onsemi
NCP81174MNTXG
QFN32_5X5
Switch Mode
FOR GPU Core
EN
PGOOD
GPU Core/100A/195A
TI
TPS51212DSCR
SON10_3X3
Controller
FOR GPU VRAM
EN
PGOOD
+1.35VSG/23A/40A
Note:
+5VALW/10A/18A
Voltage
TDC
current limit
lenovo联想
LENOVO.CRDN
Title
Power Block
Size
C
Document Number
Skylake-H
Rev V0.3
Date:
Wednesday, January 27, 2016
Sheet
93
of
99
"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

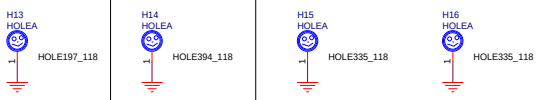


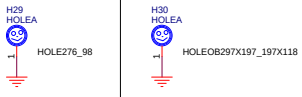
SSD





WLAN





lenovo联想	LENOVO.CRDN	
Title: ME		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Wednesday, January 27, 2016	Sheet 94 of 99	

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."

lenovo联想 LENOVO.CRDN

Title: ME

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Wednesday, January 27, 2016 | Sheet 95 of 99

"PROPERTY NOTE: this document contains information confidential and property to LENOVO PND and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of LENOVO PND."