GIGABYTE GA-M57SLI-S4 Schematics

Revision:1.1

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05	PROCESSOR DDR INTERFACE
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27	KB_MS/FUSEVCC
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32	ATX POWER CONNCTOR,VCC15
33	DUAL BIOS
34	FRONT PANEL
35	ITE 8716F (GB)
36	FAN/HW MONITOR
37	F_USB1/F_USB2/F_USB3 CONNECTOR
38	COMA , LPT , TPM , R_USB
39	MARVELL 1116 RGMII PHY -A
40	TI TSB43AB23 1394A
41	
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GIGABYTE CORP.

Title: BLOCK DIAGRAM

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Model Name: GA-M57SLI-S4

Version: 1.1

Component value change history

Date	Change Item	Reason
REV0.1 2006/03/27	First release.	
	REV1.0A	
2006/05/10	First PVT	
	REV1.1A	
2006/05/16	Update M2 CPU 風扇新機構	
	REV1.1B	
2006/05/25	R182 建新料時料號規則錯誤,修正	
	REV1.1C	
2006/06/01	改 VCC15 & CPU 機構	
	REV1.1D	
2006/06/26	EC9 1000U (low temperature 3D hang up)	
	remove R13 (VCC current leakage issue)	
	R451 12K/4/1 for STR margin	

Circuit or PCB layout change for next version

Date	Change Item	Reason
REV0.1 2006/03/27		
	First release.	
	REV1.1	
2006/06/01	改 VCC15 & CPU 機構	

GIGABYTE CORP.		
Title: BOM & PCB MODIFY HISTORY		
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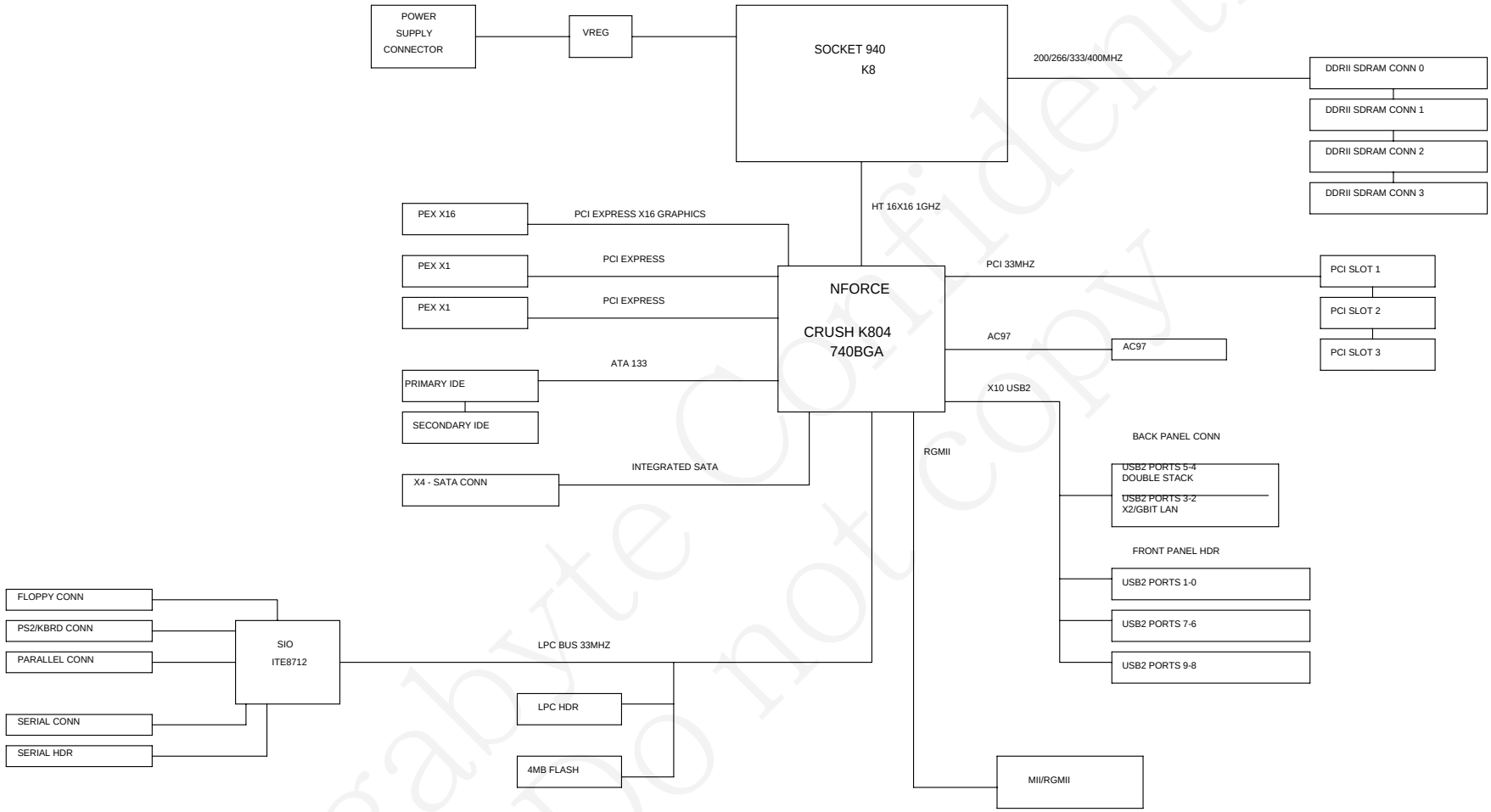
BLOCK DIAGRAM



GIGABYTE CORP.		
Title: BLOCK DIAGRAM		
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] [11]
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [11]
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] [11]
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] [11]
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] [11]
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] [11]
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] [11]
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] [11]

CPU_VDDA_RUN = VDDA25
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

VLDT_A = VCC12_HT
VLDT_B = HT12B

U12A

HYPERTRANSPORT

VCC12_HT R156 49.9/6/1 R163 49.9/6/1 GND
[11] L0_CTLIN_H0 [11] L0_CTLIN_L0

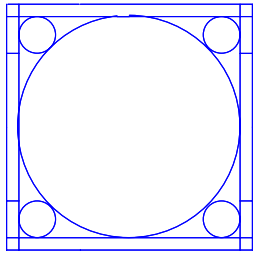
L0_CLKIN_H1 N6 L0_CLKIN_L1 P6 L0_CLKIN_H0 N3 L0_CLKIN_L0 N2
L0_CTLIN_H0 U1 L0_CTLIN_L0 V1
L0_CADIN_H15 U6 L0_CADIN_L15 V6 L0_CADIN_H14 T4 L0_CADIN_L14 T5 L0_CADIN_H13 R6 L0_CADIN_L13 T6 L0_CADIN_H12 P4 L0_CADIN_L12 P5 L0_CADIN_H11 M4 L0_CADIN_L11 M5 L0_CADIN_H10 L6 L0_CADIN_L10 M6 L0_CADIN_H9 K4 L0_CADIN_L9 K5 L0_CADIN_H8 J6 L0_CADIN_L8 K6
L0_CADIN_H7 U3 L0_CADIN_L7 U2 L0_CADIN_H6 R1 L0_CADIN_L6 T1 L0_CADIN_H5 R3 L0_CADIN_L5 R2 L0_CADIN_H4 N1 L0_CADIN_L4 P1 L0_CADIN_H3 L1 L0_CADIN_L3 M1 L0_CADIN_H2 L3 L0_CADIN_L2 L2 L0_CADIN_H1 J1 L0_CADIN_L1 K1 L0_CADIN_H0 J3 L0_CADIN_L0 J2

L0_CLKOUT_H(1) L0_CLKOUT_L(1) L0_CLKOUT_H(0) L0_CLKOUT_L(0)
L0_CTLOUT_H(1) L0_CTLOUT_L(1) L0_CTLOUT_H(0) L0_CTLOUT_L(0)
L0_CADOUT_H(15) L0_CADOUT_L(15) L0_CADOUT_H(14) L0_CADOUT_L(14) L0_CADOUT_H(13) L0_CADOUT_L(13) L0_CADOUT_H(12) L0_CADOUT_L(12) L0_CADOUT_H(11) L0_CADOUT_L(11) L0_CADOUT_H(10) L0_CADOUT_L(10) L0_CADOUT_H(9) L0_CADOUT_L(9) L0_CADOUT_H(8) L0_CADOUT_L(8)
L0_CADOUT_H(7) L0_CADOUT_L(7) L0_CADOUT_H(6) L0_CADOUT_L(6) L0_CADOUT_H(5) L0_CADOUT_L(5) L0_CADOUT_H(4) L0_CADOUT_L(4) L0_CADOUT_H(3) L0_CADOUT_L(3) L0_CADOUT_H(2) L0_CADOUT_L(2) L0_CADOUT_H(1) L0_CADOUT_L(1) L0_CADOUT_H(0) L0_CADOUT_L(0)

AD5 L0_CLKOUT_H1 AD4 L0_CLKOUT_L1 AD1 L0_CLKOUT_H0 AC1 L0_CLKOUT_L0
Y6 1 TP3 W6 1 TP4 W2 L0_CTLOUT_H0 W3 L0_CTLOUT_L0
L0_CTLOUT_H0 [11] L0_CTLOUT_L0 [11]
Y5 L0_CADOUT_H15 Y4 L0_CADOUT_L15 AB6 L0_CADOUT_H14 AA6 L0_CADOUT_L14 AB5 L0_CADOUT_H13 AB4 L0_CADOUT_L13 AD6 L0_CADOUT_H12 AC6 L0_CADOUT_L12 AE6 L0_CADOUT_H11 AE6 L0_CADOUT_L11 AF5 L0_CADOUT_H10 AE4 L0_CADOUT_L10 AH6 L0_CADOUT_H9 AG6 L0_CADOUT_L9 AH5 L0_CADOUT_H8 AH4 L0_CADOUT_L8
Y1 L0_CADOUT_H7 W1 L0_CADOUT_L7 AA2 L0_CADOUT_H6 AA3 L0_CADOUT_L6 AB1 L0_CADOUT_H5 AA1 L0_CADOUT_L5 AC2 L0_CADOUT_H4 AC3 L0_CADOUT_L4 AE2 L0_CADOUT_H3 AE3 L0_CADOUT_L3 AF1 L0_CADOUT_H2 AE1 L0_CADOUT_L2 AG2 L0_CADOUT_H1 AG3 L0_CADOUT_L1 AH1 L0_CADOUT_H0 AG1 L0_CADOUT_L0

VCORE
SC24 0.01U/4/Y5V/25V/Z
SC23 0.01U/4/Y5V/25V/Z
SC18 0.01U/4/Y5V/25V/Z
CLOSE CHIPSET & CROSSING BOUNDARY

SOCKET_M2
M2_RM/PLASTICS/[12KRC-04K807-41R]



GIGABYTE CORP.

Title: CPU HYPER TRANSPORT

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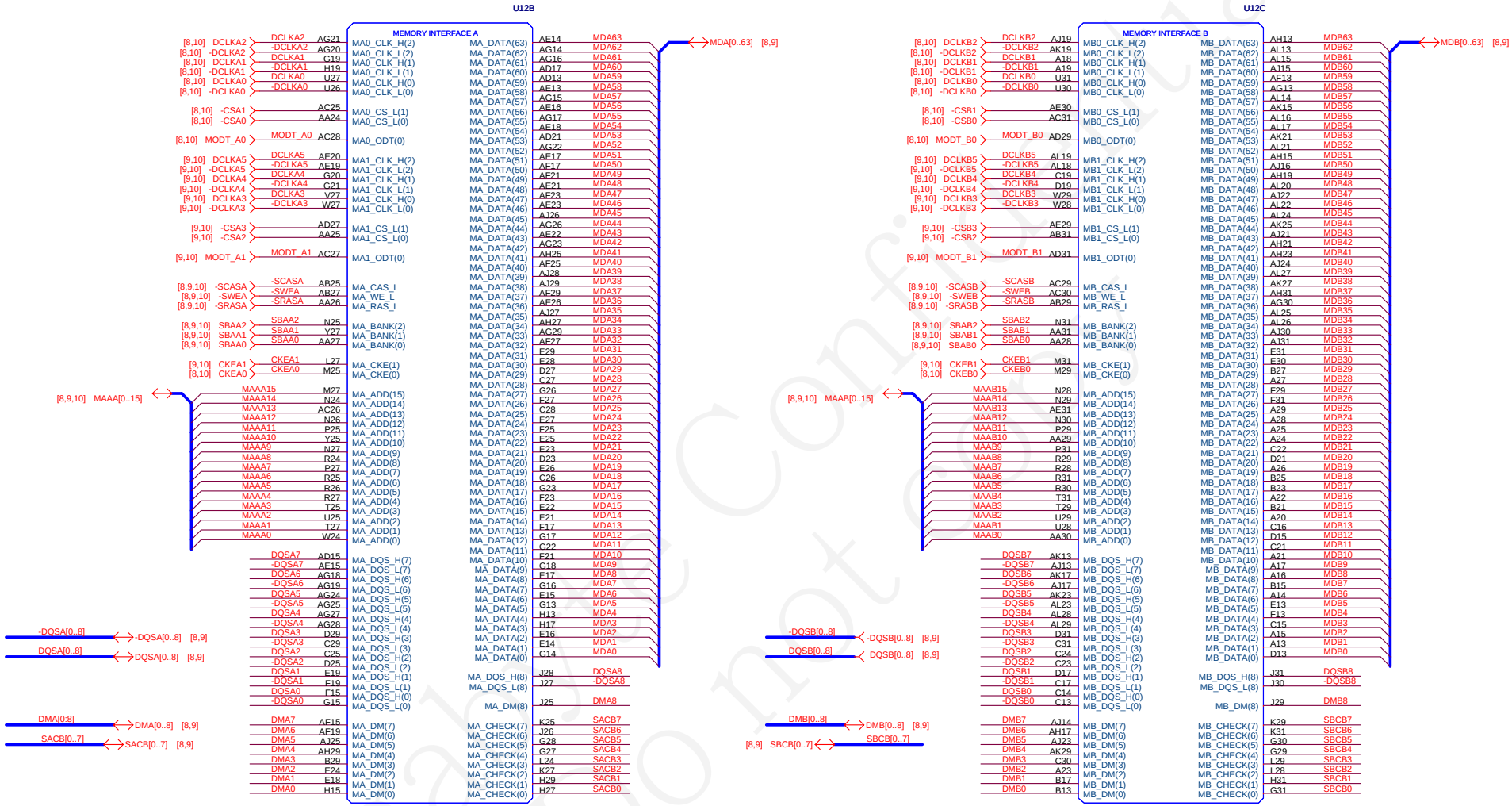

GIGABYTE CORP.	
Title	CPU DDRII MEMORY
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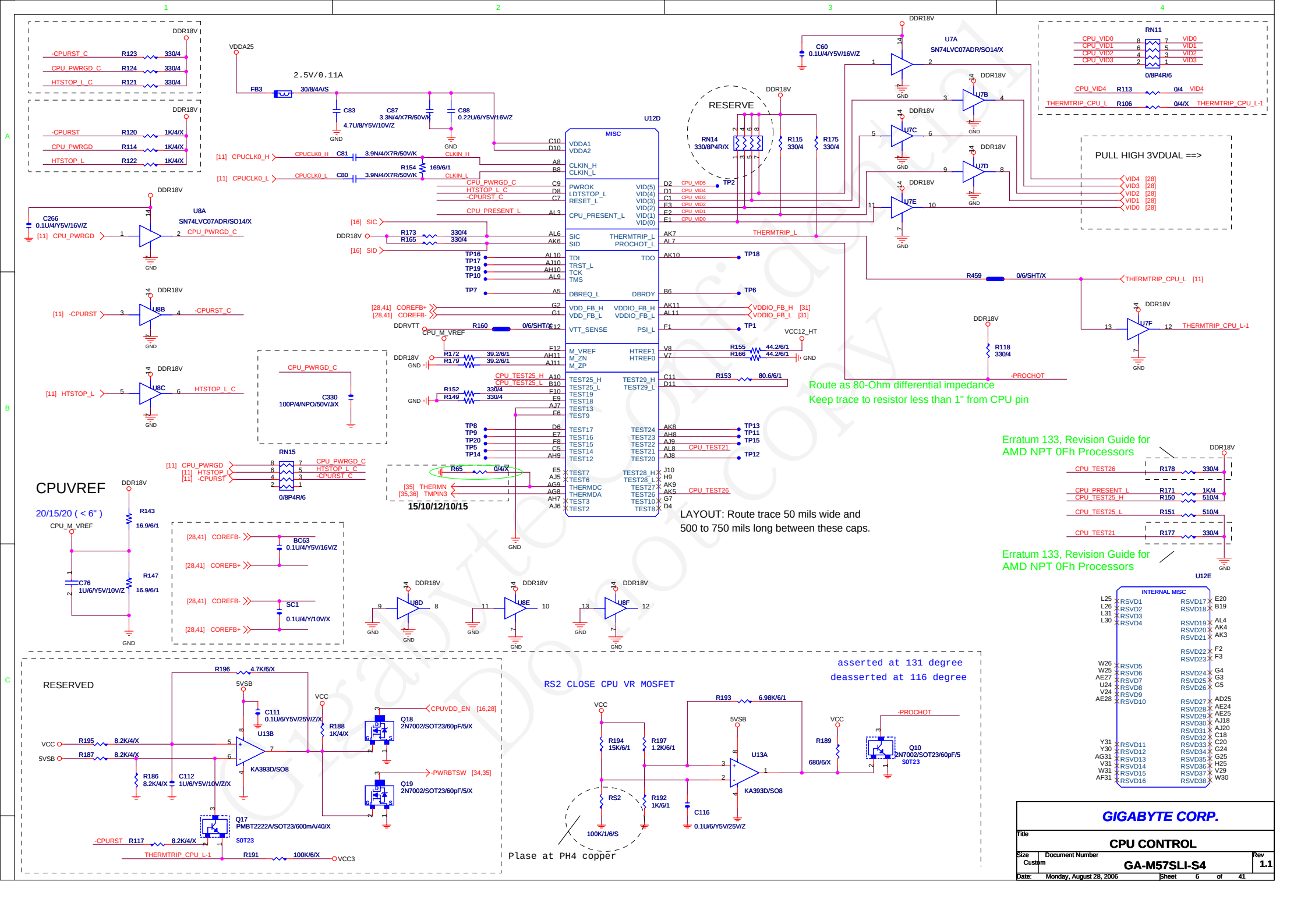
DDR18V
-CPURST_C R123 330/4
CPU_PWRGD_C R124 330/4
HTSTOP_L_C R121 330/4
-CPURST R120 1K/4/X
CPU_PWRGD R114 1K/4/X
HTSTOP_L R122 1K/4/X
VDDA25
2.5V/0.11A
FB3 30/8/4A/S
C83 4.7U/8/Y5V/10V/Z
C87 3.3N/4/X7R/50V/K
C88 0.22U/6/Y5V16V/Z
GND
[11] CPUCLK0_H
CPUCLK0_H C81 3.9N/4/X7R/50V/K
CLKIN_H
R154 169/6/1
[11] CPUCLK0_L
CPUCLK0_L C80 3.9N/4/X7R/50V/K
CLKIN_L
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
CPU_PRESENT_L
U12D
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
SIC
SID
THERMTRIP_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VTT_SENSE
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
CPU_VID5
CPU_VID4
CPU_VID3
CPU_VID2
CPU_VID1
CPU_VID0
TP2
THERMTRIP_L
TP18
TP6
TP1
VCC12_HT
VDDIO_FB_H [31]
VDDIO_FB_L [31]
TP13
TP11
TP15
TP12
CPU_TEST21
CPU_TEST26
RESERVE
RN14 330/8P4R/X
R115 330/4
R175 330/4
U7A SN74LVC07ADR/SO14/X
U7B
U7C
U7D
U7E
U7F
C60 0.1U/4/Y5V/16V/Z
RN11
CPU_VID0 VID0
CPU_VID1 VID1
CPU_VID2 VID2
CPU_VID3 VID3
0/8P4R/6
CPU_VID4 R113 0/4 VID4
THERMTRIP_CPU_L R106 0/4/X THERMTRIP_CPU_L-1
PULL HIGH 3VDUAL ==>
VID4 [28]
VID3 [28]
VID2 [28]
VID1 [28]
VID0 [28]
R459 0/6/SHT/X
THERMTRIP_CPU_L [11]
R118 330/4
-PROCHOT
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
U8A SN74LVC07ADR/SO14/X
C266 0.1U/4/Y5V/16V/Z
[11] CPU_PWRGD
CPU_PWRGD_C
U8B
[11] -CPURST
-CPURST_C
U8C
[11] HTSTOP_L
HTSTOP_L_C
[16] SIC
[16] SID
R173 330/4
R165 330/4
TP16
TP17
TP19
TP10
TP7
[28,41] COREFB+
[28,41] COREFB-
DDRVTT
R160 0/6/SHT/X
CPU_M_VREF
R172 39.2/6/1
R179 39.2/6/1
R152 330/4
R149 330/4
CPU_TEST25_H
CPU_TEST25_L
TP8
TP9
TP20
TP5
TP14
R65 0/4/X
[35] THERMN
[35,36] TMPIN3
15/10/12/10/15
CPU_PWRGD_C
C330 100P/4/NPO/50V/J/X
RN15
[11] CPU_PWRGD
[11] HTSTOP
[11] -CPURST
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
0/8P4R/6
R155 44.2/6/1
R166 44.2/6/1
R153 80.6/6/1
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
CPUVREF
20/15/20 (< 6")
R143 16.9/6/1
R147 16.9/6/1
C76 1U/6/Y5V/10V/Z
BC63 0.1U/4/Y5V/16V/Z
SC1 0.1U/4/Y/10V/X
U8D
U8E
U8F
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
CPU_TEST26 R178 330/4
CPU_PRESENT_L R171 1K/4
CPU_TEST25_H R150 510/4
CPU_TEST25_L R151 510/4
CPU_TEST21 R177 330/4
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
U12E
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
RESERVED
R196 4.7K/6/X
5VSB
C111 0.1U/6/Y5V/25V/Z/X
VCC
R188 1K/4/X
R195 8.2K/4/X
R187 8.2K/4/X
U13B
KA393D/SO8
R186 8.2K/4/X
C112 1U/6/Y5V/10V/Z/X
Q17 PMBT2222A/SOT23/600mA/40/X
S0T23
-CPURST R117 8.2K/4/X
THERMTRIP_CPU_L-1
R191 100K/6/X
VCC3
CPUVDD_EN [16,28]
Q18 2N7002/SOT23/60pF/5/X
-PWRBTSW [34,35]
Q19 2N7002/SOT23/60pF/5/X
RS2 CLOSE CPU VR MOSFET
asserted at 131 degree
deasserted at 116 degree
R193 6.98K/6/1
R194 15K/6/1
R197 1.2K/6/1
R192 1K/6/1
C116 0.1U/6/Y5V/25V/Z
U13A
R189 680/6/X
Q10 2N7002/SOT23/60pF/5
S0T23
100K/1/6/S
Plase at PH4 copper
GIGABYTE CORP.
Title
CPU CONTROL
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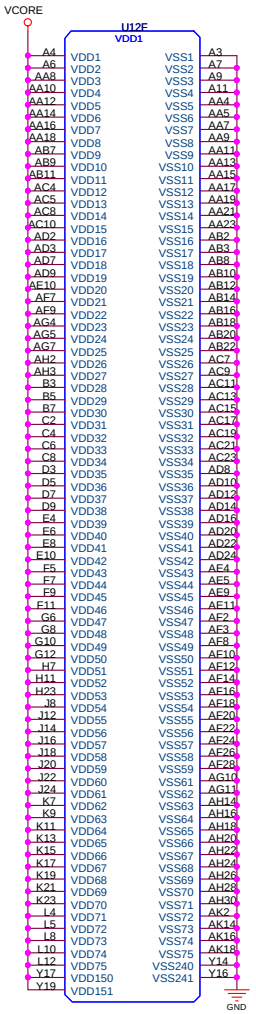
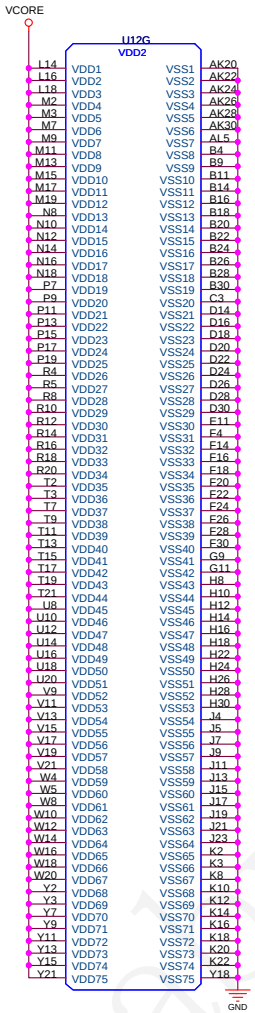
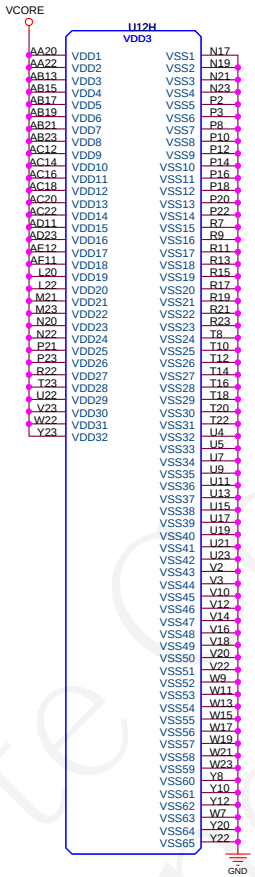
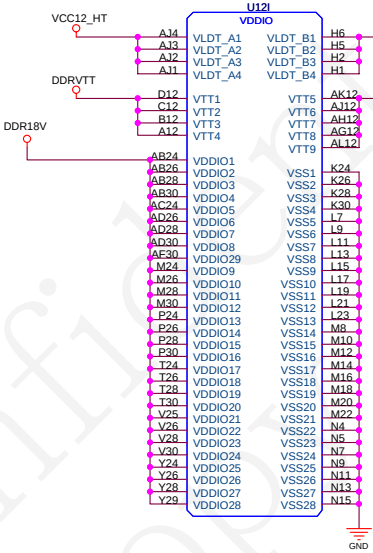
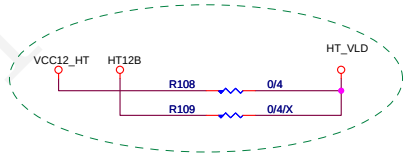
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

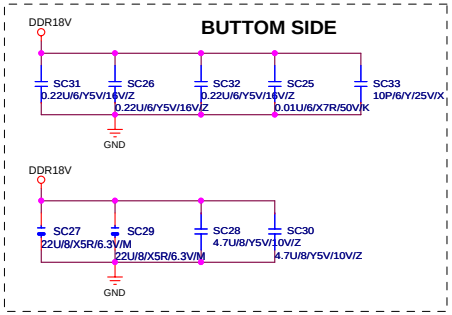


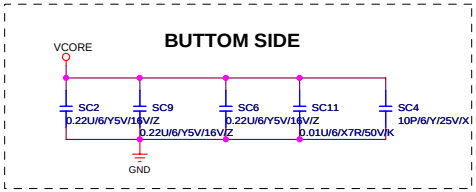


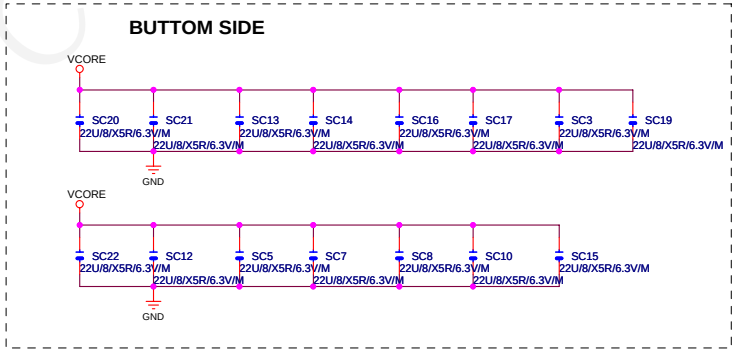


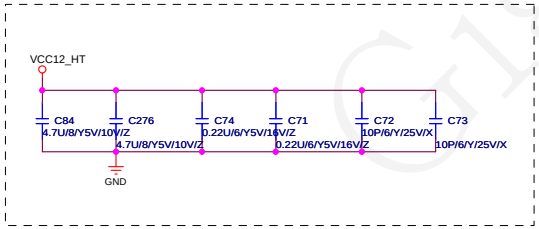


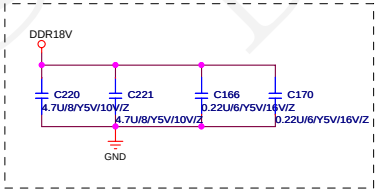


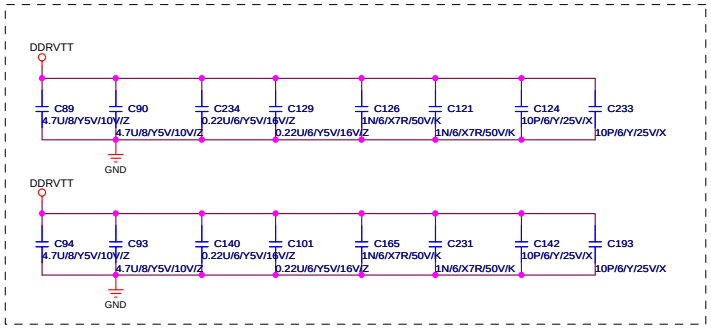


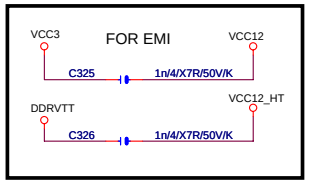












GIGABYTE CORP.			
Title: CPU POWER & GND			
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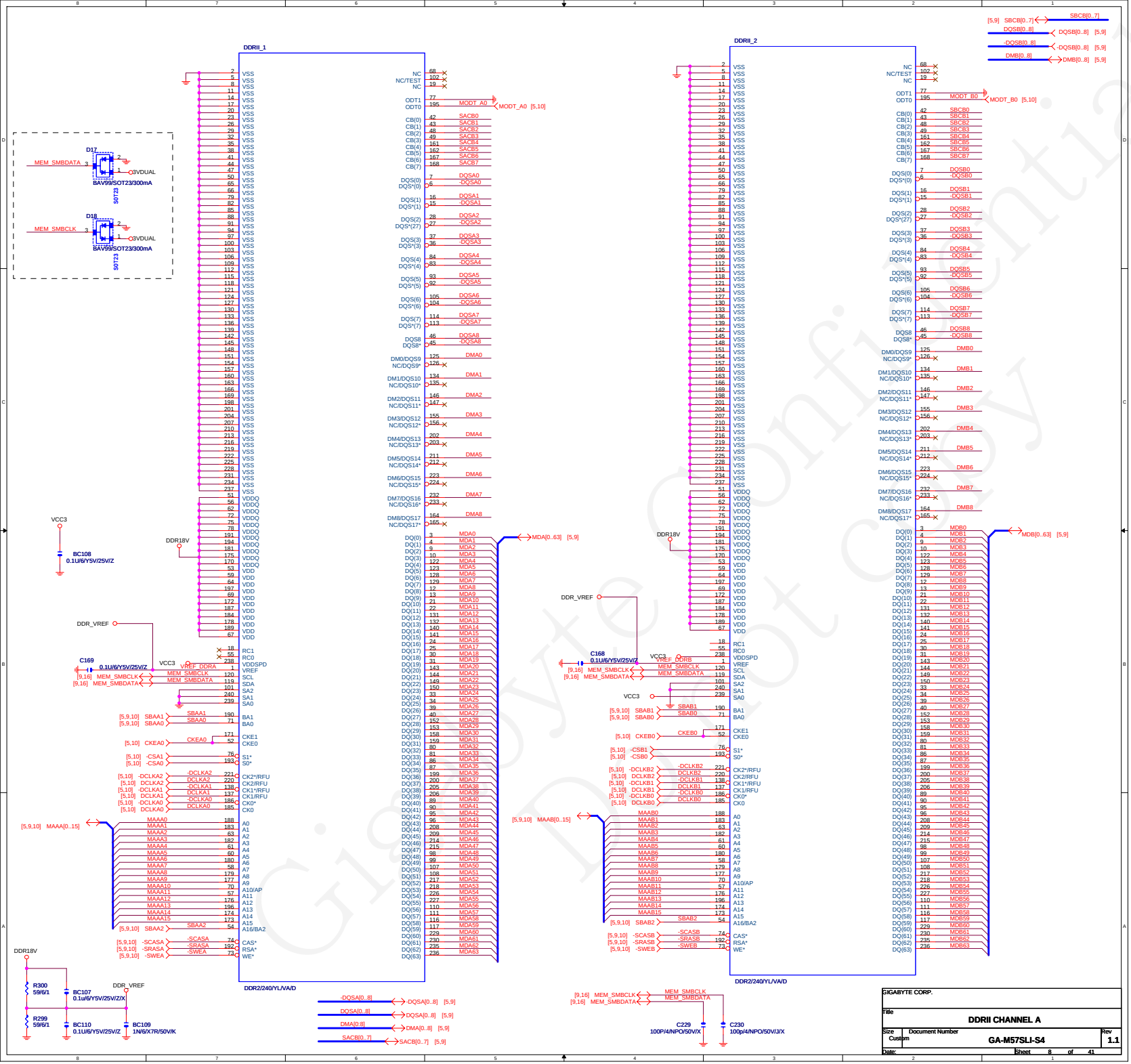
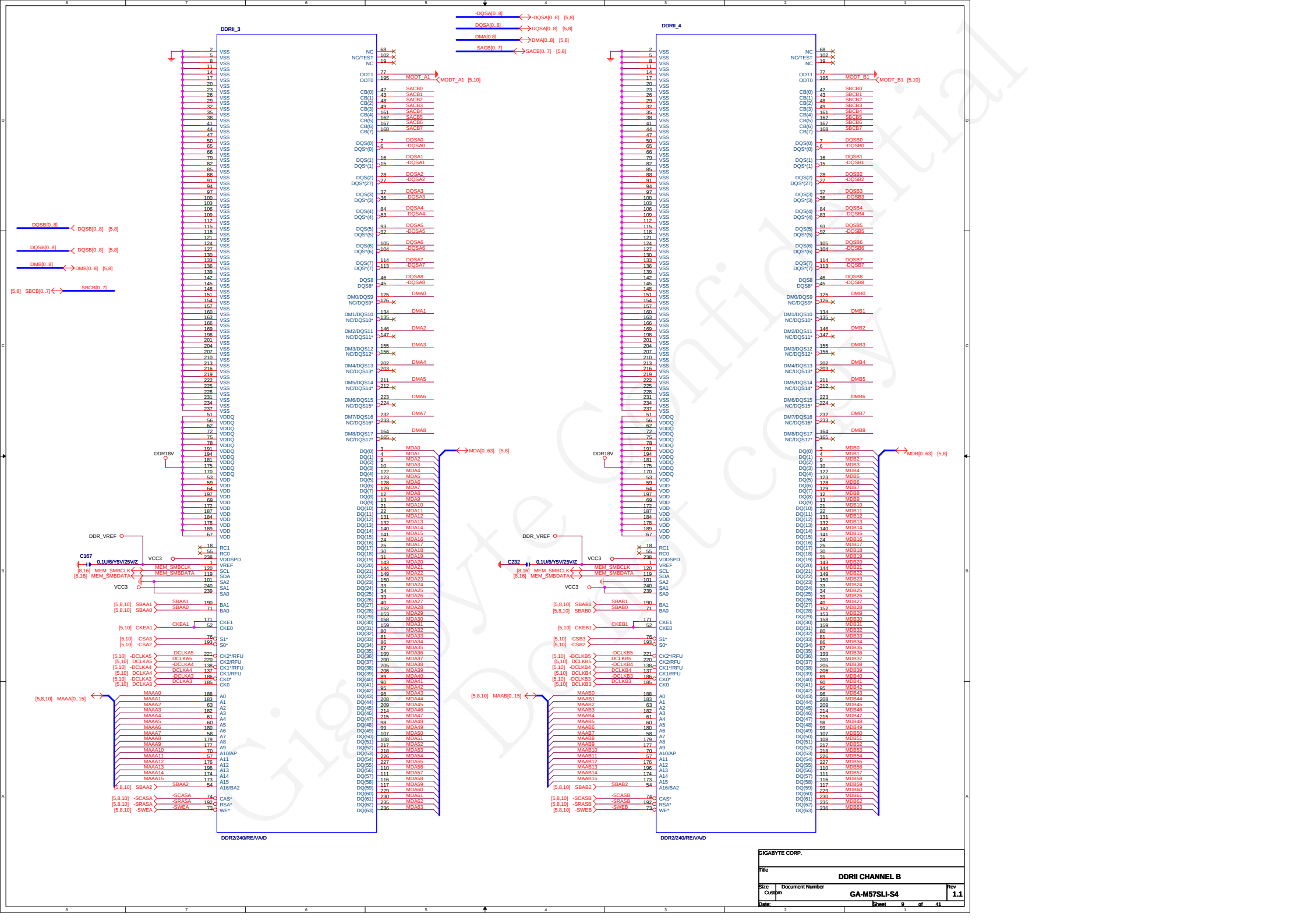


GIGABYTE CORP.		
Title	DDRII CHANNEL A	
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date:	Sheet 8 of 41	



GIGABYTE CORP.	
Title	DDRII CHANNEL B
Size: Custom	Document Number: GA-M57SLI-S4
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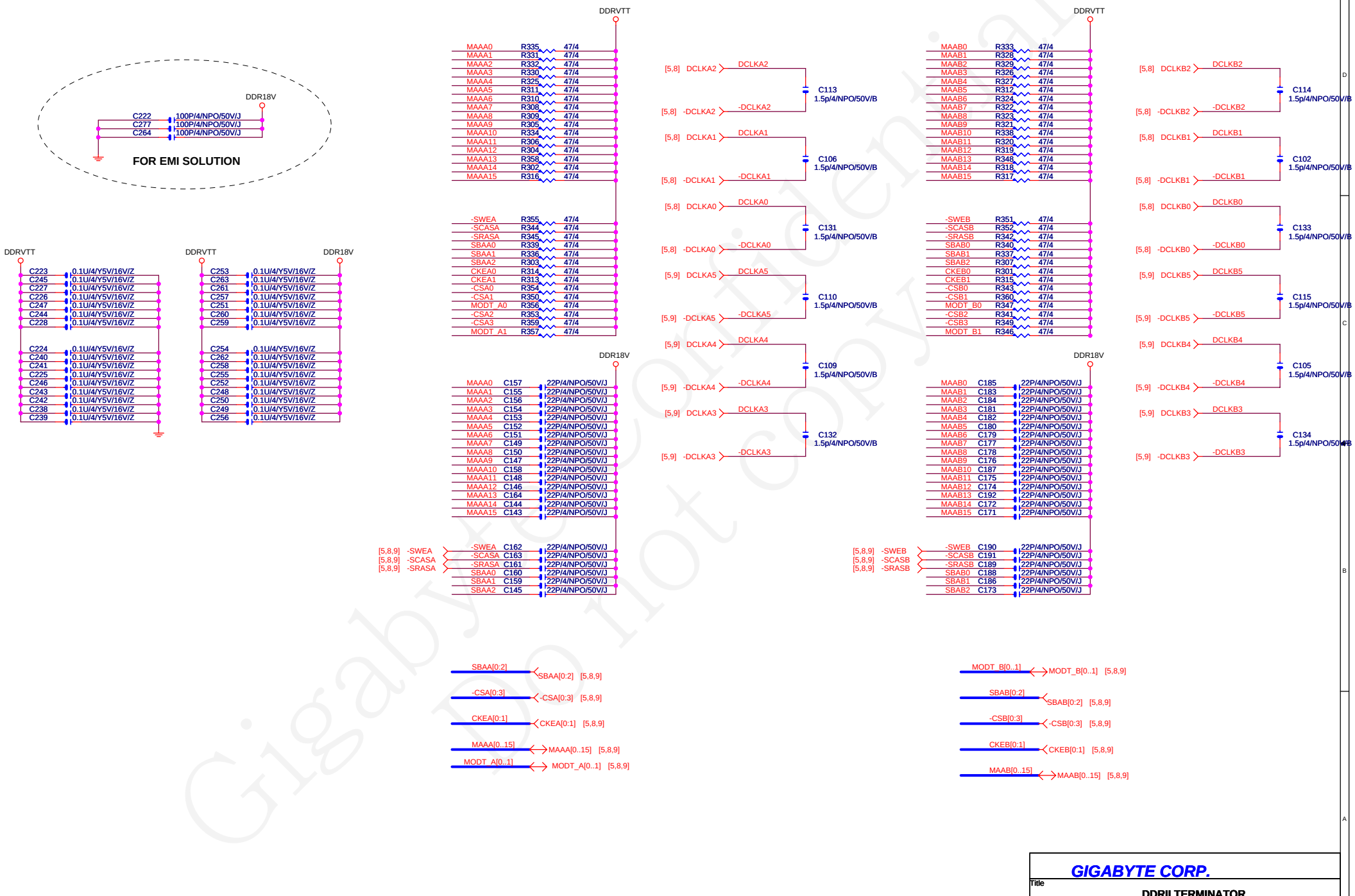
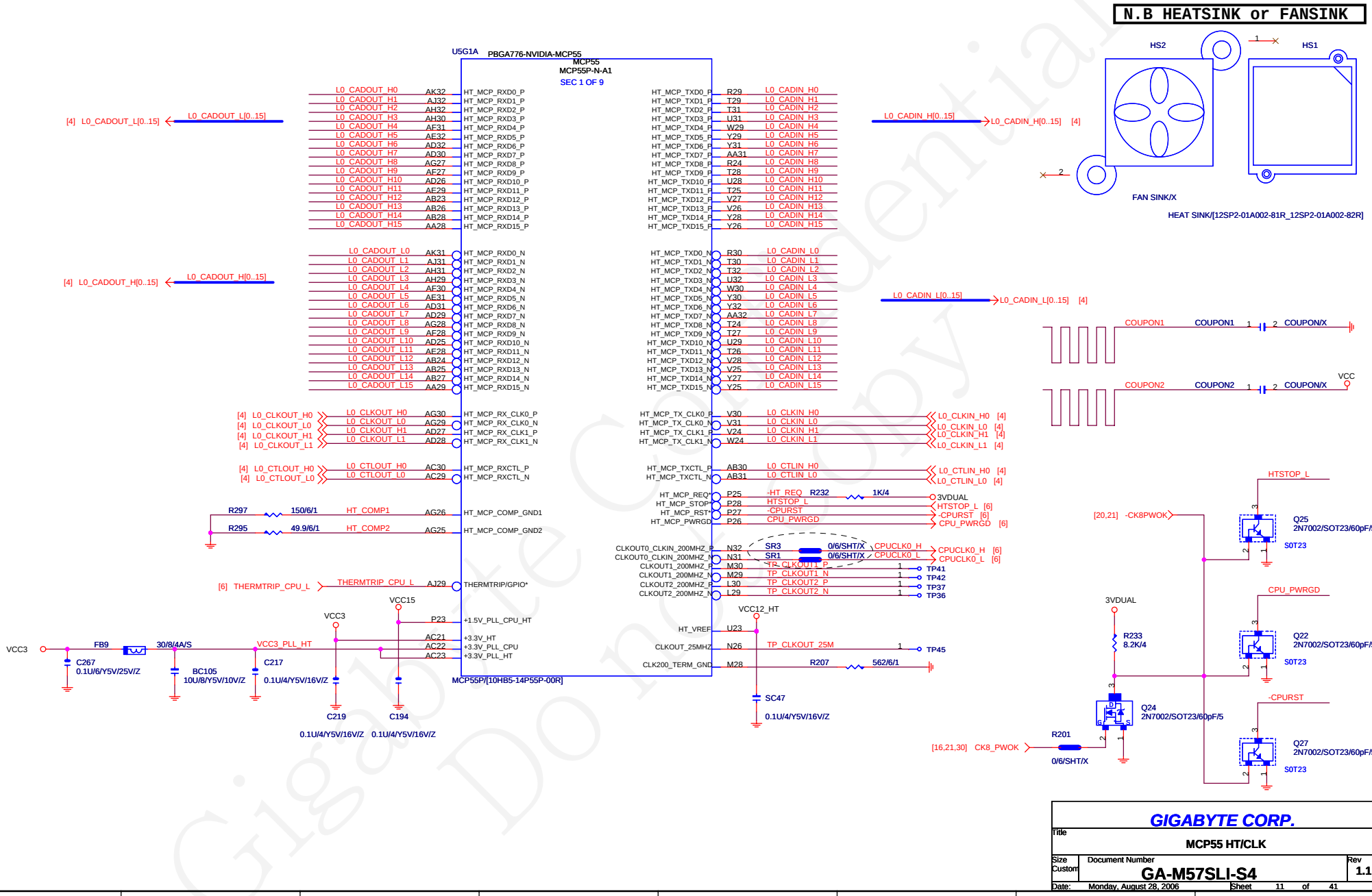
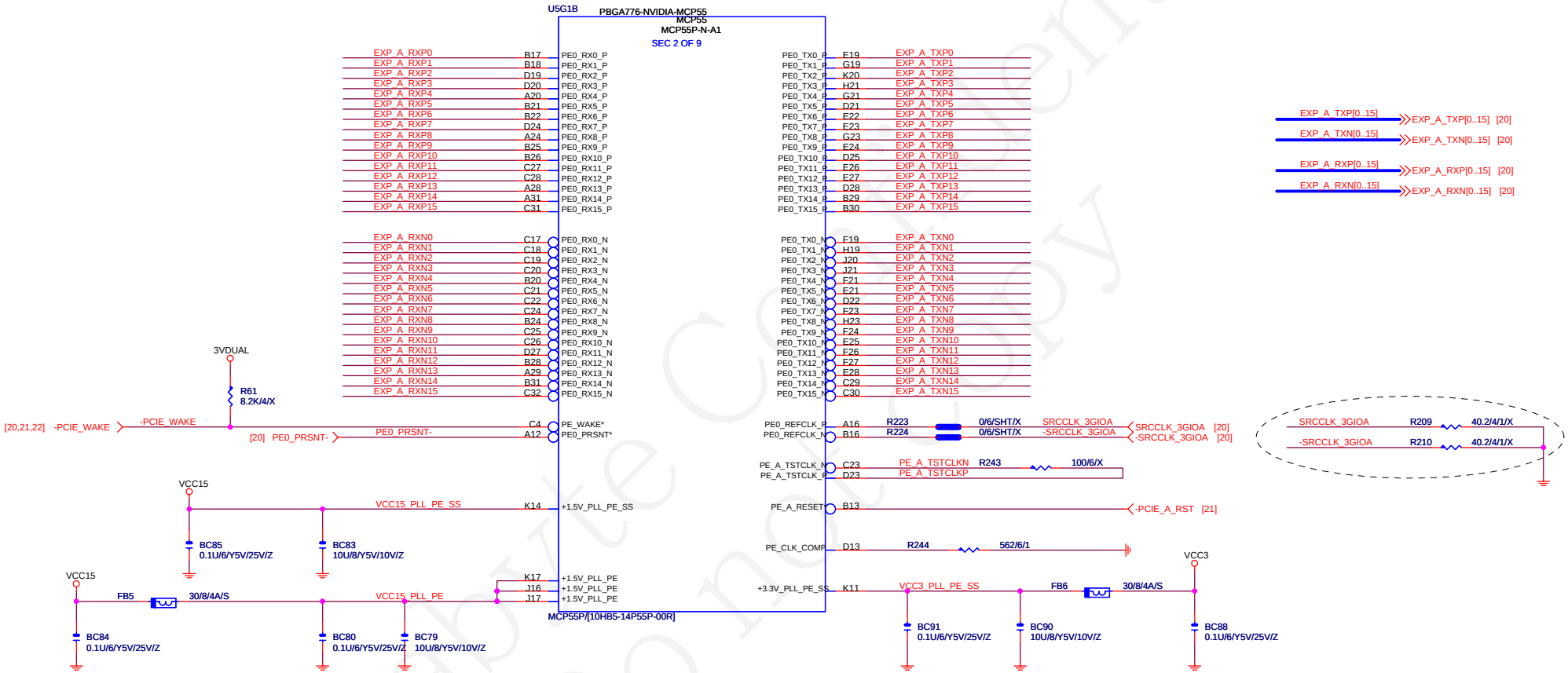
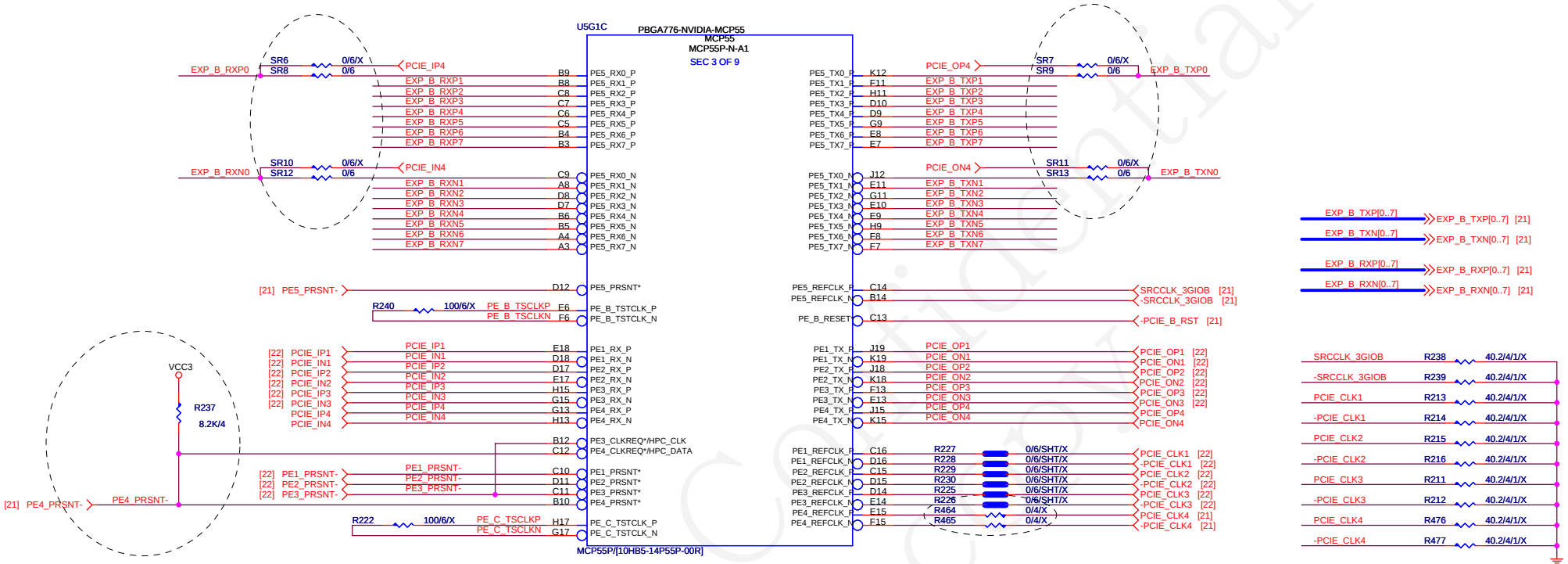


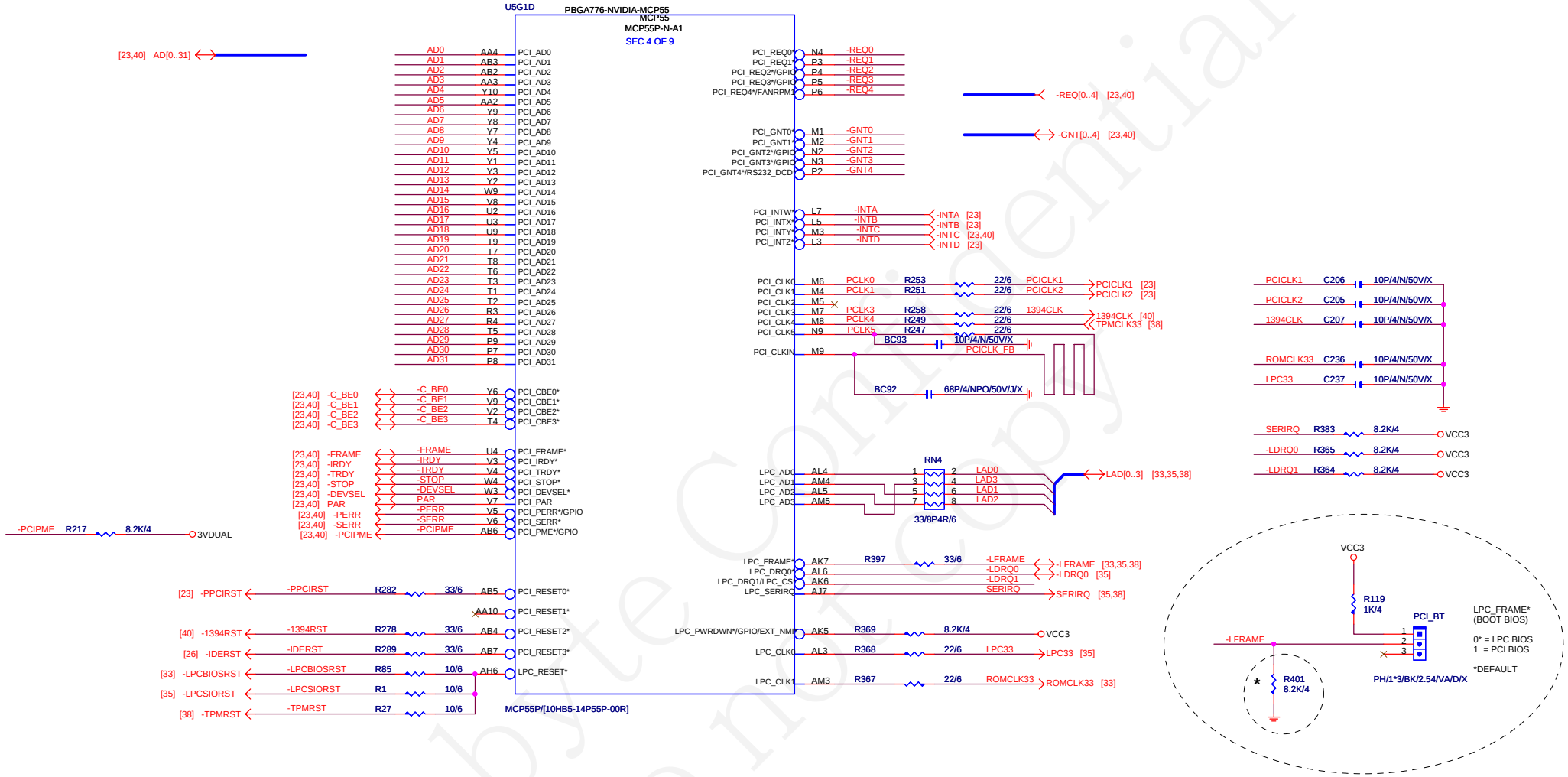




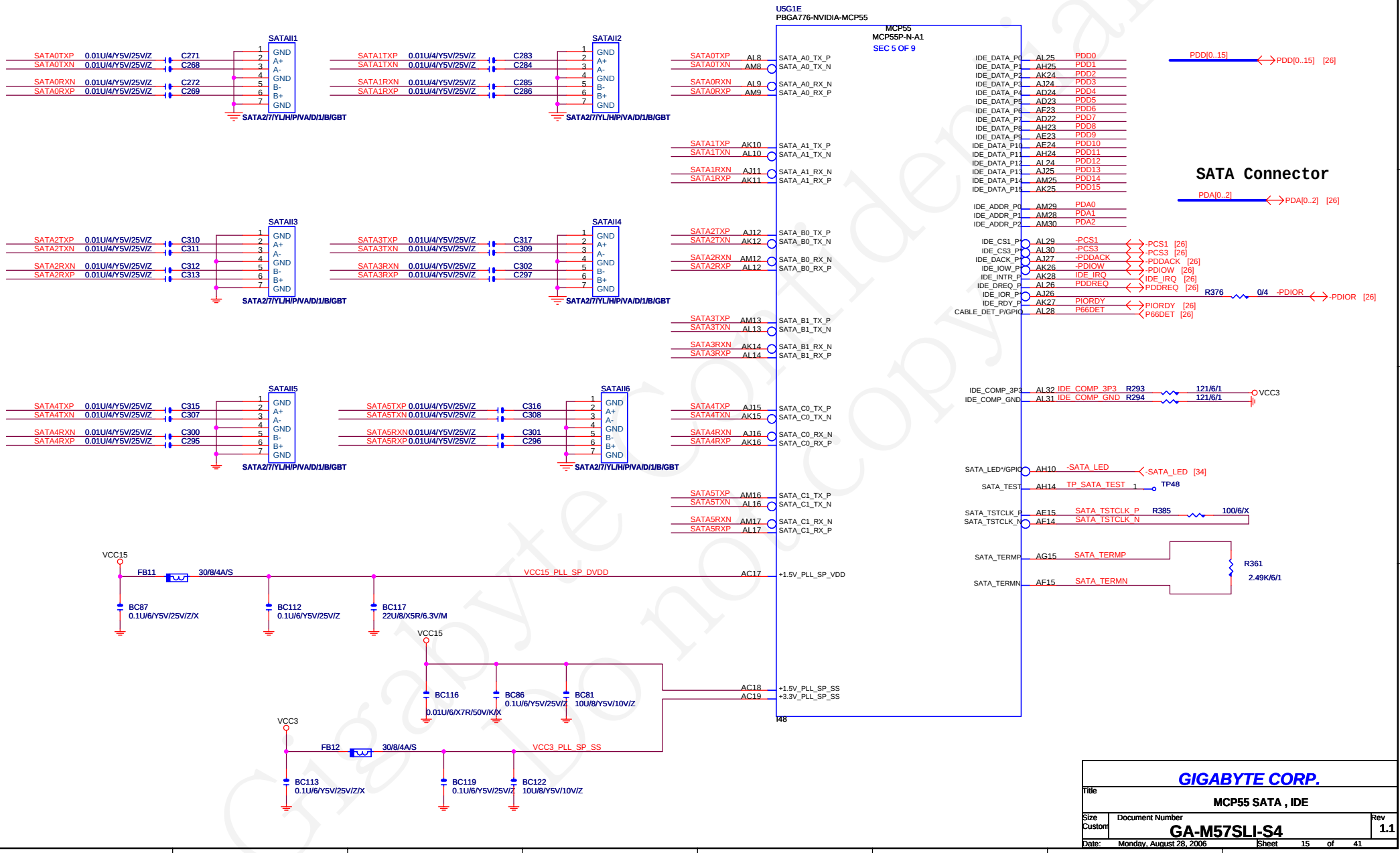
GIGABYTE CORP.		
Title: MCP55 PCIE X16		
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 12 of 41	

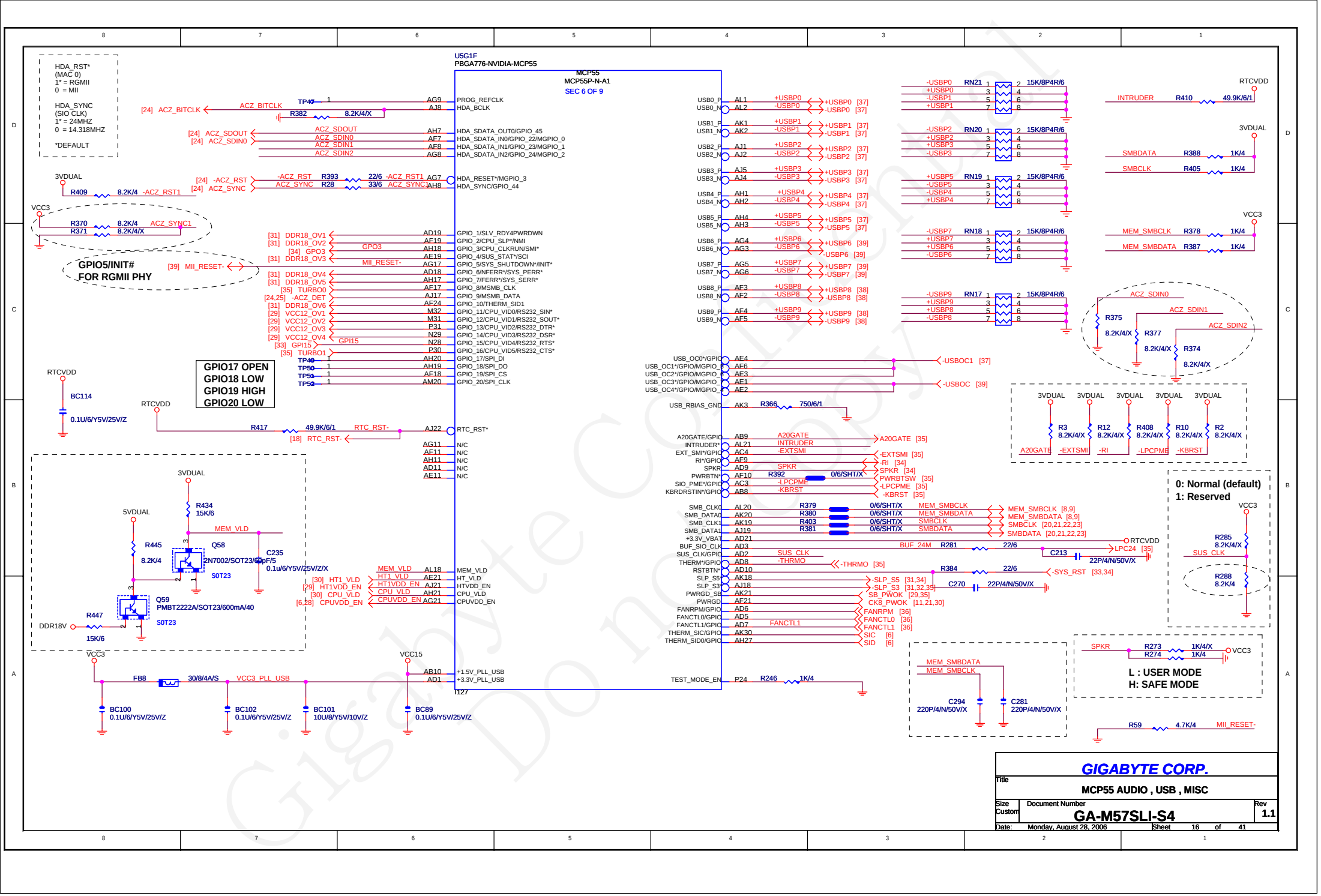


GIGABYTE CORP.		
Title: MCP55 PCIE X8 , X1		
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 13 of 41	



GIGABYTE CORP.		
Title: MCP55 PCI		
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 14 of 41	




HDA_RST*
(MAC 0)
1* = RGMII
0 = MII
HDA_SYNC
(SIO CLK)
1* = 24MHZ
0 = 14.318MHZ
*DEFAULT
U5G1F
PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 6 OF 9
GPIO5/INIT#
FOR RGMII PHY
GPIO17 OPEN
GPIO18 LOW
GPIO19 HIGH
GPIO20 LOW
0: Normal (default)
1: Reserved
L : USER MODE
H: SAFE MODE
GIGABYTE CORP.
MCP55 AUDIO , USB , MISC
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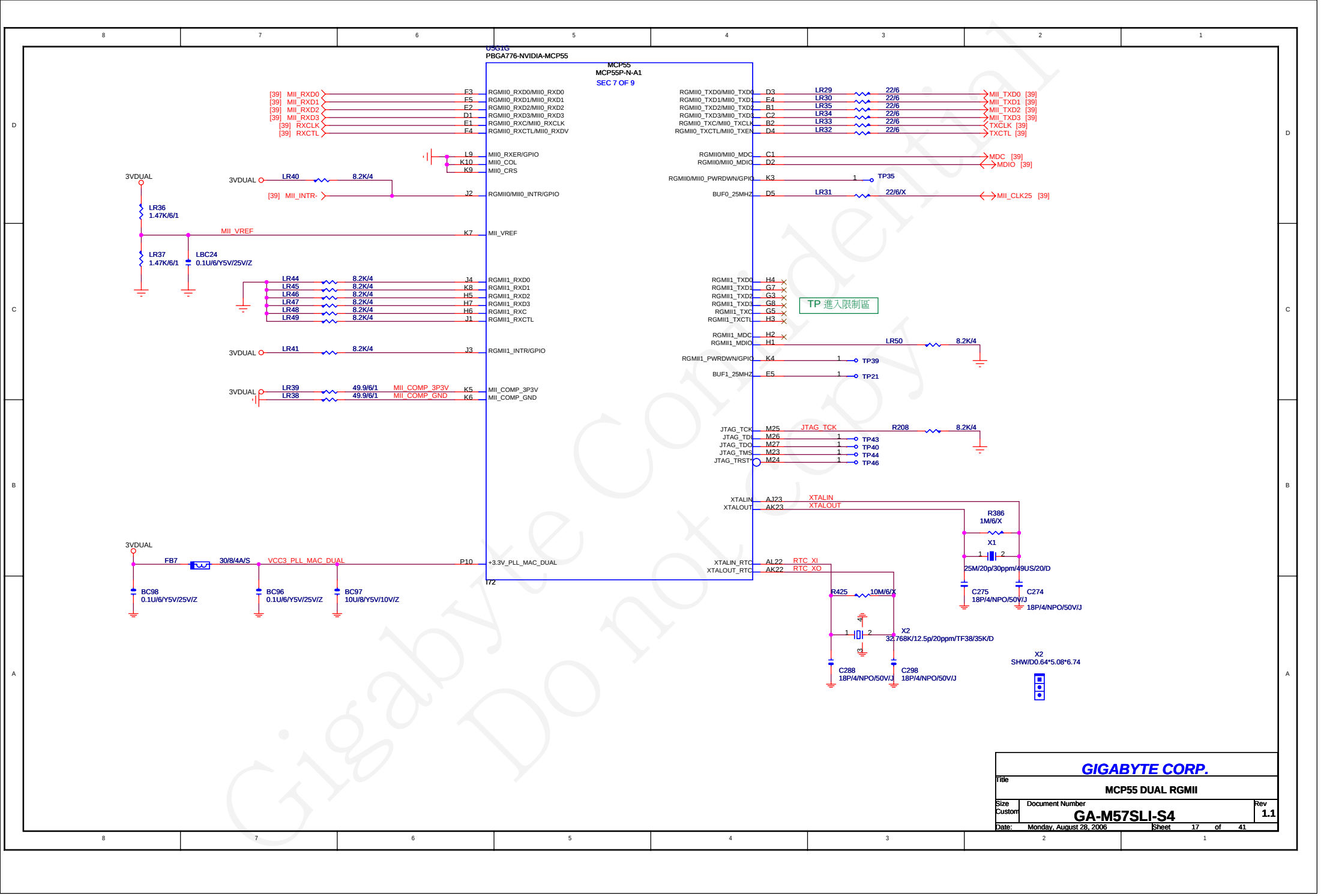
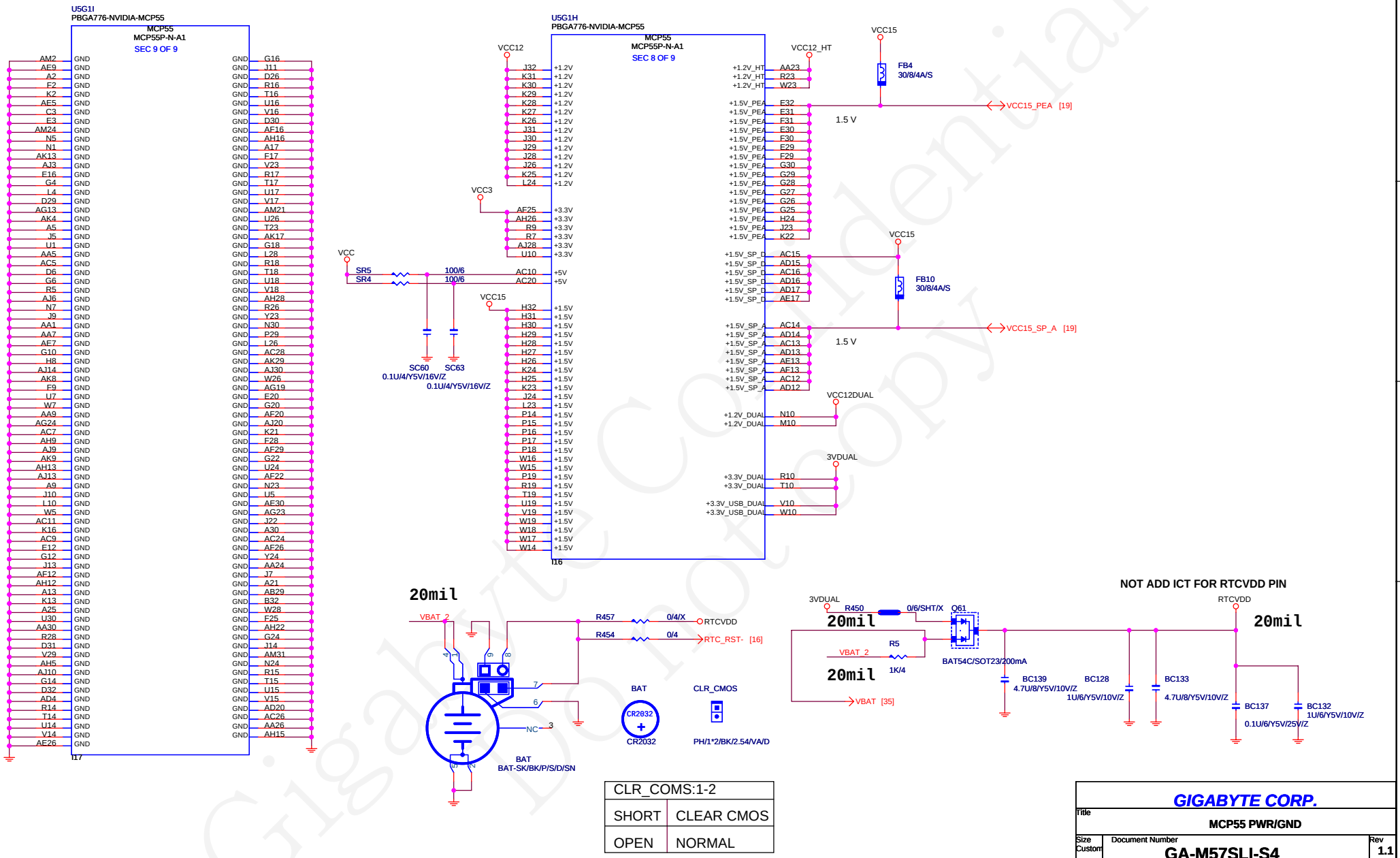
Monday, August 28, 2006
Sheet 16 of 41





CLR_COMS:1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL

GIGABYTE CORP.

Title: MCP55 PWR/GND

Size: Custom | Document Number: GA-M57SLI-S4 | Rev: 1.1

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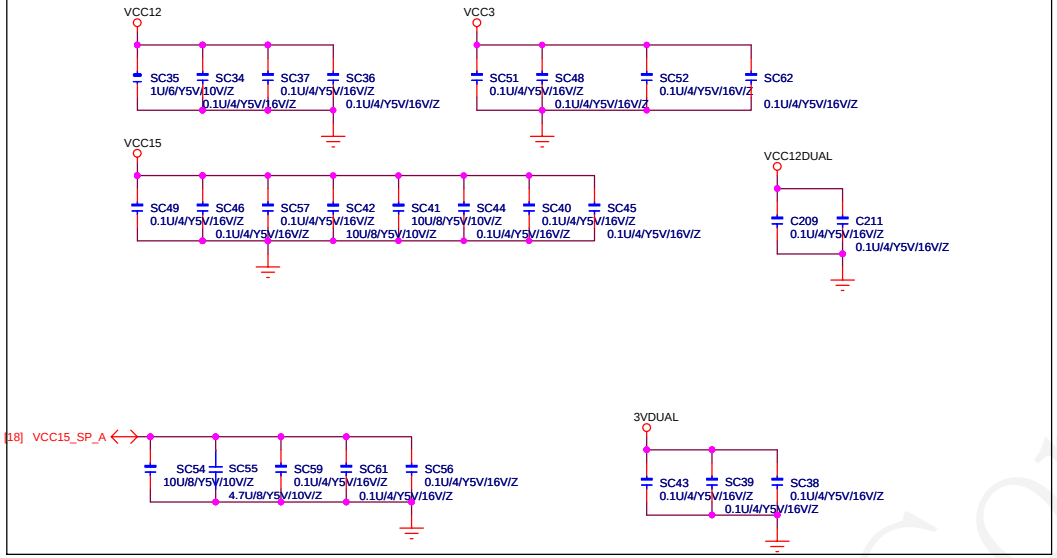
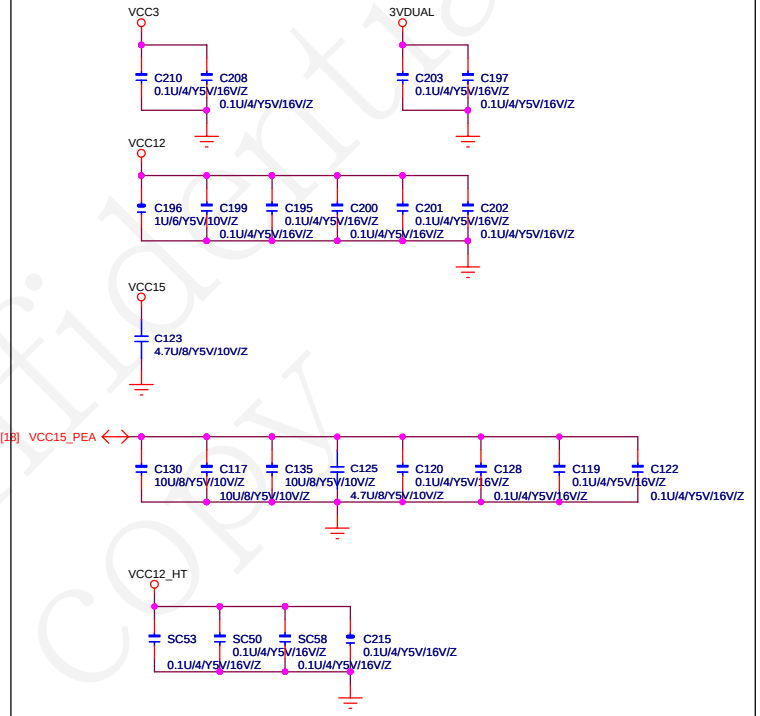
MCP55 BACK SIDE DECOUPLING



MCP55 TOP SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

GIGABYTE CORP.

Title: MCP55 DECOUPLING

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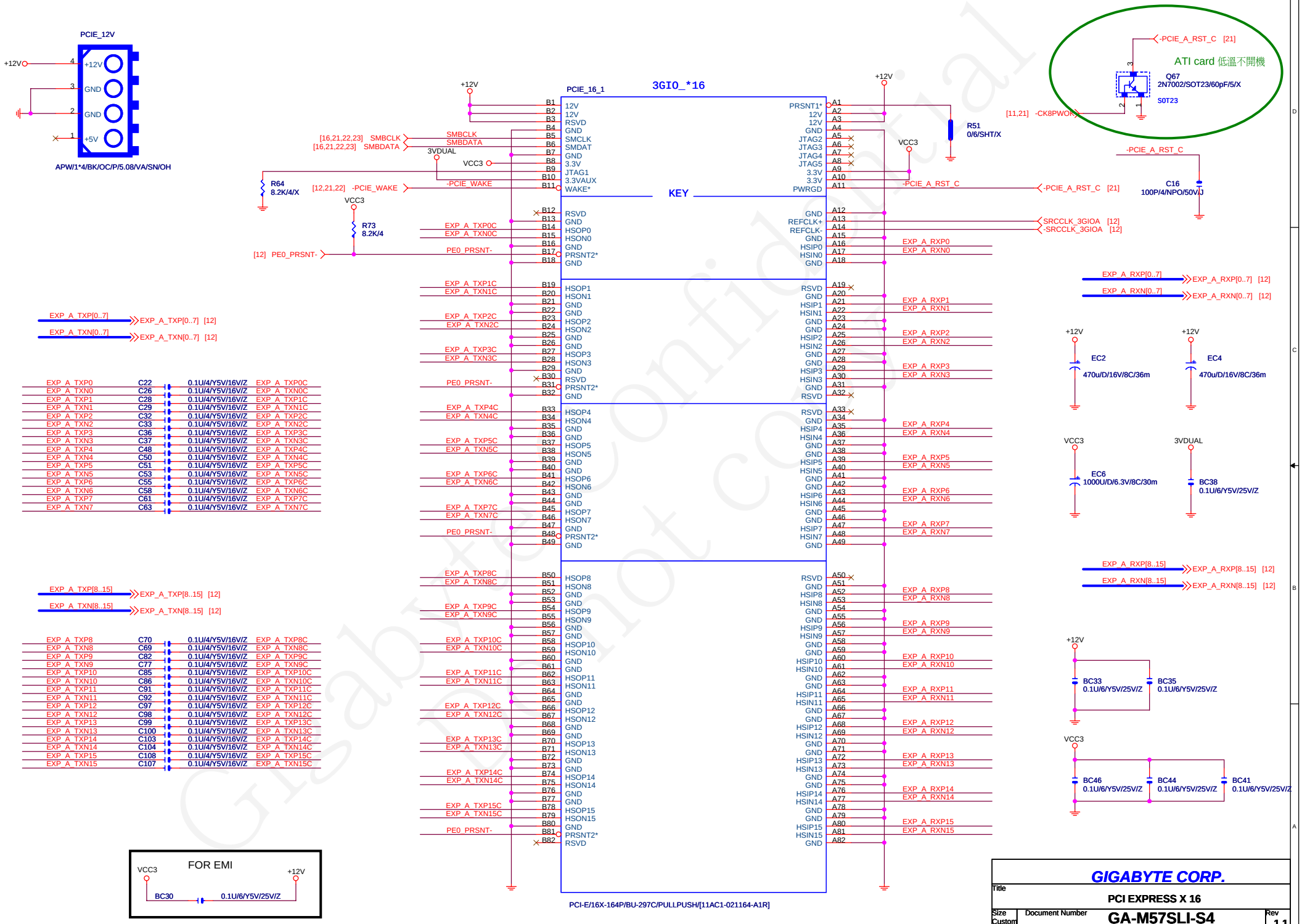
PCIE_12V
APW/1*4/BK/OC/P/5.08/VA/SN/OH
PCIE_16_1
3GIO_*16
KEY
PCI-E/16X-164P/BU-297C/PULLPUSH/[11AC1-021164-A1R]
ATI card 低溫不開機
Q67
2N7002/SOT23/60pF/5/X
S0T23
R51
0/6/SHT/X
R64
8.2K/4/X
R73
8.2K/4
C16
100P/4/NPO/50V/J
EC2
470u/D/16V/8C/36m
EC4
470u/D/16V/8C/36m
EC6
1000U/D/6.3V/8C/30m
BC38
0.1U/6/Y5V/25V/Z
BC33
0.1U/6/Y5V/25V/Z
BC35
0.1U/6/Y5V/25V/Z
BC46
0.1U/6/Y5V/25V/Z
BC44
0.1U/6/Y5V/25V/Z
BC41
0.1U/6/Y5V/25V/Z
FOR EMI
BC30
0.1U/6/Y5V/25V/Z
GIGABYTE CORP.
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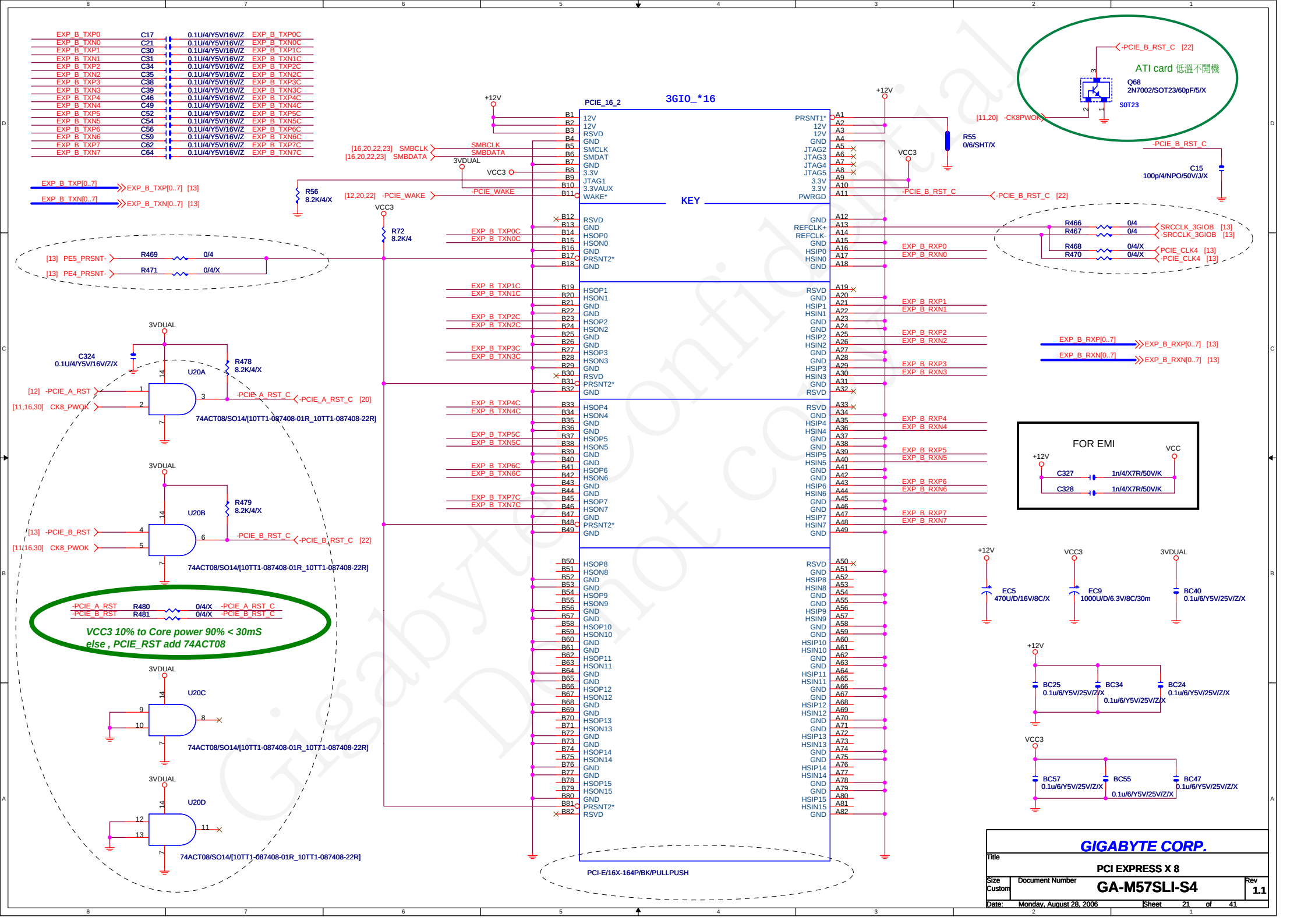
EXP_B_TXP0 C17 0.1U/4/Y5V/16V/Z EXP_B_TXP0C
EXP_B_TXN0 C21 0.1U/4/Y5V/16V/Z EXP_B_TXN0C
EXP_B_TXP1 C30 0.1U/4/Y5V/16V/Z EXP_B_TXP1C
EXP_B_TXN1 C31 0.1U/4/Y5V/16V/Z EXP_B_TXN1C
EXP_B_TXP2 C34 0.1U/4/Y5V/16V/Z EXP_B_TXP2C
EXP_B_TXN2 C35 0.1U/4/Y5V/16V/Z EXP_B_TXN2C
EXP_B_TXP3 C38 0.1U/4/Y5V/16V/Z EXP_B_TXP3C
EXP_B_TXN3 C39 0.1U/4/Y5V/16V/Z EXP_B_TXN3C
EXP_B_TXP4 C46 0.1U/4/Y5V/16V/Z EXP_B_TXP4C
EXP_B_TXN4 C49 0.1U/4/Y5V/16V/Z EXP_B_TXN4C
EXP_B_TXP5 C52 0.1U/4/Y5V/16V/Z EXP_B_TXP5C
EXP_B_TXN5 C54 0.1U/4/Y5V/16V/Z EXP_B_TXN5C
EXP_B_TXP6 C56 0.1U/4/Y5V/16V/Z EXP_B_TXP6C
EXP_B_TXN6 C59 0.1U/4/Y5V/16V/Z EXP_B_TXN6C
EXP_B_TXP7 C62 0.1U/4/Y5V/16V/Z EXP_B_TXP7C
EXP_B_TXN7 C64 0.1U/4/Y5V/16V/Z EXP_B_TXN7C
EXP_B_TXP[0..7] EXP_B_TXP[0..7] [13]
EXP_B_TXN[0..7] EXP_B_TXN[0..7] [13]
R56 8.2K/4/X
[12,20,22] -PCIE_WAKE -PCIE_WAKE
[16,20,22,23] SMBCLK SMBCLK
[16,20,22,23] SMBDATA SMBDATA
3VDUAL
VCC3
R72 8.2K/4
[13] PE5_PRSNT- R469 0/4
[13] PE4_PRSNT- R471 0/4/X
PCIE_16_2
3GIO_*16
KEY
+12V
B1 12V
B2 12V
B3 RSVD
B4 GND
B5 SMCLK
B6 SMDAT
B7 GND
B8 3.3V
B9 JTAG1
B10 3.3VAUX
B11 WAKE*
B12 RSVD
B13 GND
B14 HSOP0
B15 HSON0
B16 GND
B17 PRSNT2*
B18 GND
B19 HSOP1
B20 HSON1
B21 GND
B22 GND
B23 HSOP2
B24 HSON2
B25 GND
B26 GND
B27 HSOP3
B28 HSON3
B29 GND
B30 RSVD
B31 PRSNT2*
B32 GND
B33 HSOP4
B34 HSON4
B35 GND
B36 GND
B37 HSOP5
B38 HSON5
B39 GND
B40 GND
B41 HSOP6
B42 HSON6
B43 GND
B44 GND
B45 HSOP7
B46 HSON7
B47 GND
B48 PRSNT2*
B49 GND
B50 HSOP8
B51 HSON8
B52 GND
B53 GND
B54 HSOP9
B55 HSON9
B56 GND
B57 GND
B58 HSOP10
B59 HSON10
B60 GND
B61 GND
B62 HSOP11
B63 HSON11
B64 GND
B65 GND
B66 HSOP12
B67 HSON12
B68 GND
B69 GND
B70 HSOP13
B71 HSON13
B72 GND
B73 GND
B74 HSOP14
B75 HSON14
B76 GND
B77 GND
B78 HSOP15
B79 HSON15
B80 GND
B81 PRSNT2*
B82 RSVD
PRSNT1* A1
12V A2
12V A3
GND A4
JTAG2 A5
JTAG3 A6
JTAG4 A7
JTAG5 A8
3.3V A9
3.3V A10
PWRGD A11
GND A12
REFCLK+ A13
REFCLK- A14
GND A15
HSIP0 A16
HSIN0 A17
GND A18
RSVD A19
GND A20
HSIP1 A21
HSIN1 A22
GND A23
GND A24
HSIP2 A25
HSIN2 A26
GND A27
GND A28
HSIP3 A29
HSIN3 A30
GND A31
RSVD A32
RSVD A33
GND A34
HSIP4 A35
HSIN4 A36
GND A37
GND A38
HSIP5 A39
HSIN5 A40
GND A41
GND A42
HSIP6 A43
HSIN6 A44
GND A45
GND A46
HSIP7 A47
HSIN7 A48
GND A49
RSVD A50
GND A51
HSIP8 A52
HSIN8 A53
GND A54
GND A55
HSIP9 A56
HSIN9 A57
GND A58
GND A59
HSIP10 A60
HSIN10 A61
GND A62
GND A63
HSIP11 A64
HSIN11 A65
GND A66
GND A67
HSIP12 A68
HSIN12 A69
GND A70
GND A71
HSIP13 A72
HSIN13 A73
GND A74
GND A75
HSIP14 A76
HSIN14 A77
GND A78
GND A79
HSIP15 A80
HSIN15 A81
GND A82
PCI-E/16X-164P/BK/PULLPUSH
R55 0/6/SHT/X
[11,20] -CK8PWOK
-PCIE_B_RST_C [22]
ATI card 低溫不開機
Q68 2N7002/SOT23/60pF/5/X
S0T23
C15 100p/4/NPO/50V/J/X
R466 0/4 SRCCLK_3GIOB [13]
R467 0/4 -SRCCLK_3GIOB [13]
R468 0/4/X PCIE_CLK4 [13]
R470 0/4/X -PCIE_CLK4 [13]
EXP_B_RXP0
EXP_B_RXN0
EXP_B_RXP1
EXP_B_RXN1
EXP_B_RXP2
EXP_B_RXN2
EXP_B_RXP3
EXP_B_RXN3
EXP_B_RXP4
EXP_B_RXN4
EXP_B_RXP5
EXP_B_RXN5
EXP_B_RXP6
EXP_B_RXN6
EXP_B_RXP7
EXP_B_RXN7
EXP_B_RXP[0..7] EXP_B_RXP[0..7] [13]
EXP_B_RXN[0..7] EXP_B_RXN[0..7] [13]
FOR EMI
+12V
VCC
C327 1n/4/X7R/50V/K
C328 1n/4/X7R/50V/K
EC5 470U/D/16V/8C/X
EC9 1000U/D/6.3V/8C/30m
BC40 0.1u/6/Y5V/25V/Z/X
BC25 0.1u/6/Y5V/25V/Z/X
BC34 0.1u/6/Y5V/25V/Z/X
BC24 0.1u/6/Y5V/25V/Z/X
BC57 0.1u/6/Y5V/25V/Z/X
BC55 0.1u/6/Y5V/25V/Z/X
BC47 0.1u/6/Y5V/25V/Z/X
C324 0.1U/4/Y5V/16V/Z/X
R478 8.2K/4/X
U20A
[12] -PCIE_A_RST
[11,16,30] CK8_PWOK
-PCIE_A_RST_C
-PCIE_A_RST_C [20]
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
R479 8.2K/4/X
U20B
[13] -PCIE_B_RST
[11,16,30] CK8_PWOK
-PCIE_B_RST_C
-PCIE_B_RST_C [22]
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
-PCIE_A_RST R480 0/4/X -PCIE_A_RST_C
-PCIE_B_RST R481 0/4/X -PCIE_B_RST_C
VCC3 10% to Core power 90% < 30mS
else , PCIE_RST add 74ACT08
U20C
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
U20D
74ACT08/SO14/[10TT1-087408-01R_10TT1-087408-22R]
GIGABYTE CORP.
Title
PCI EXPRESS X 8
Size Custom
Document Number
GA-M57SLI-S4
Rev 1.1
Date: Monday, August 28, 2006
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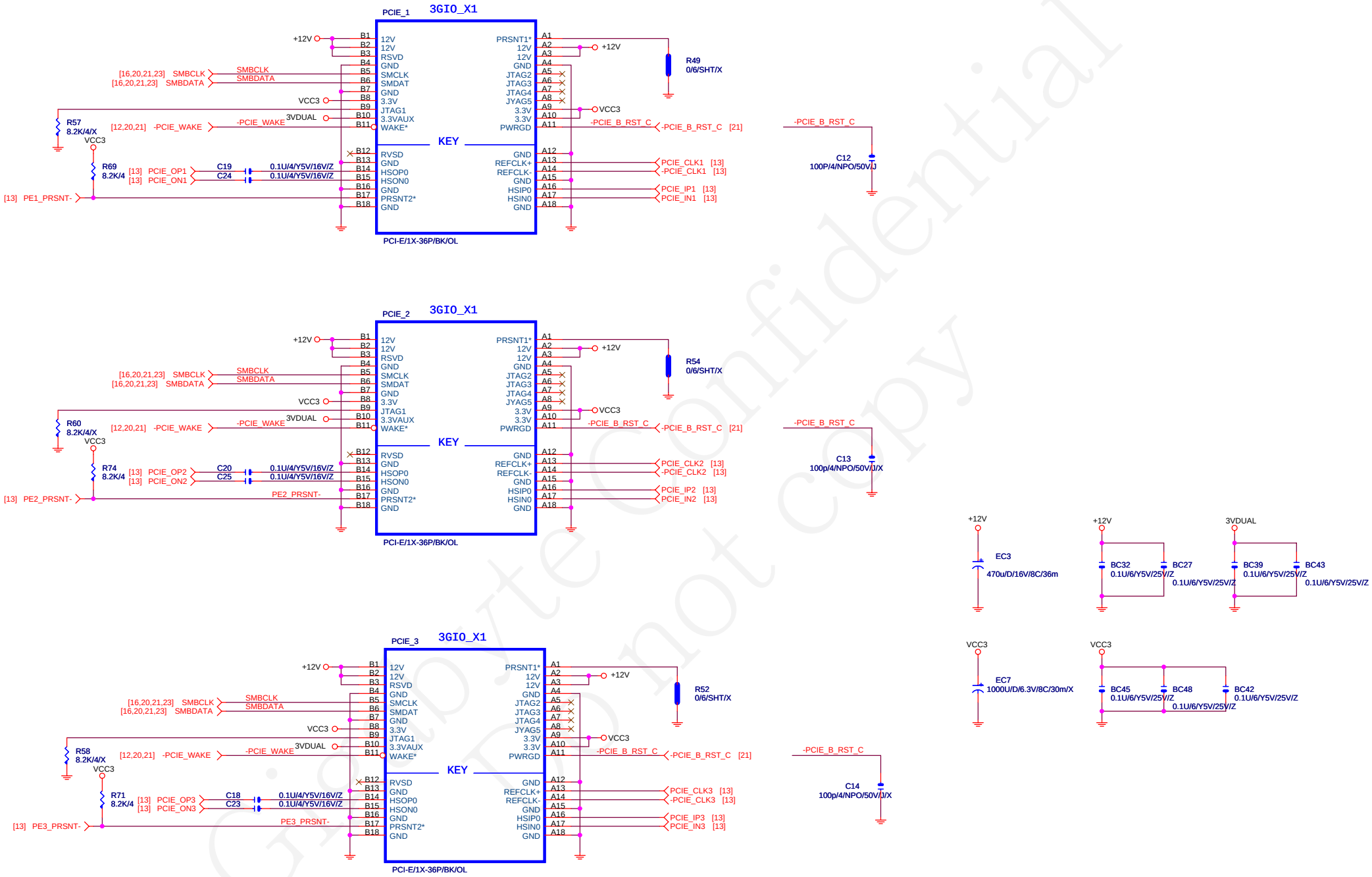
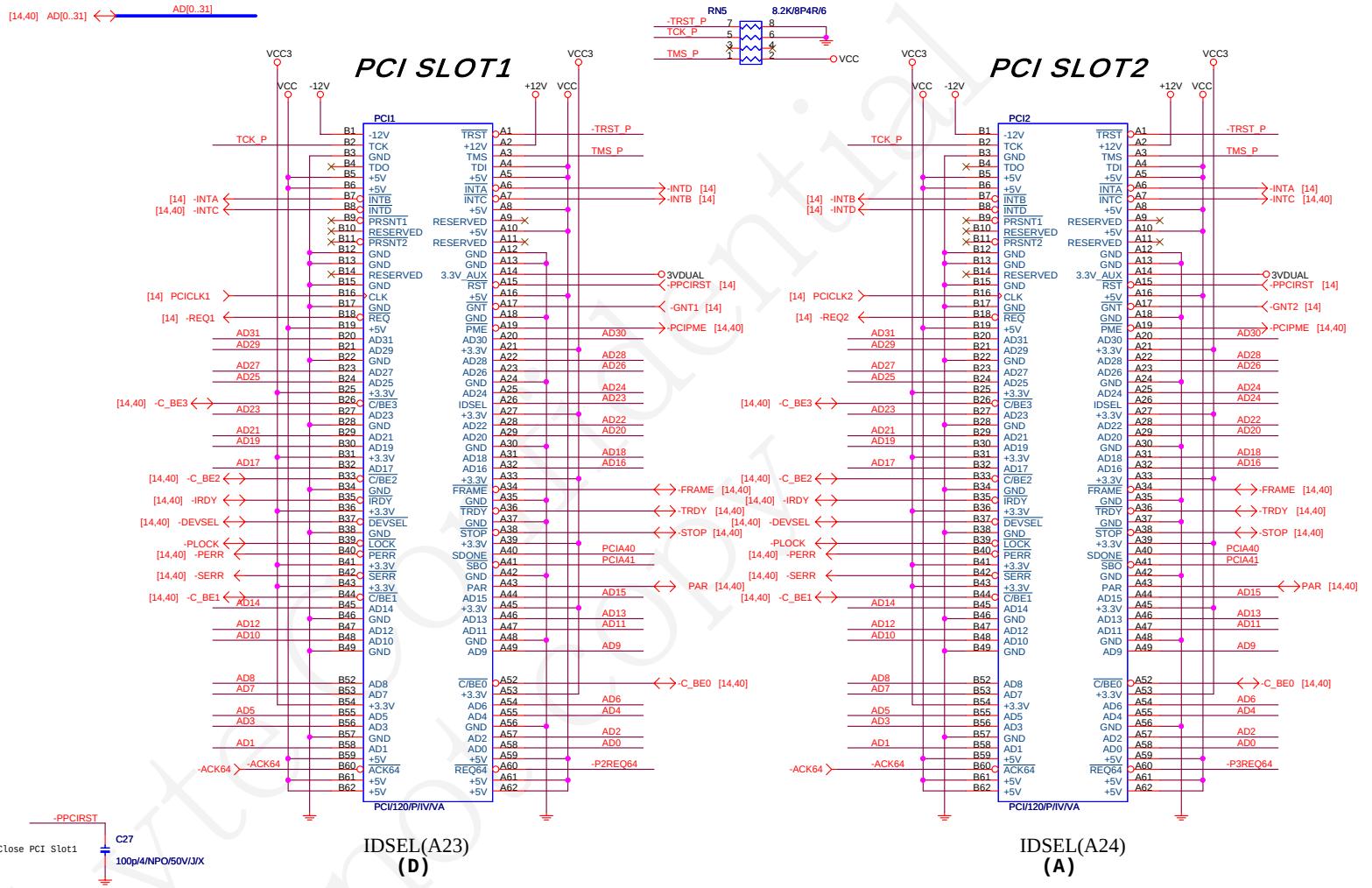
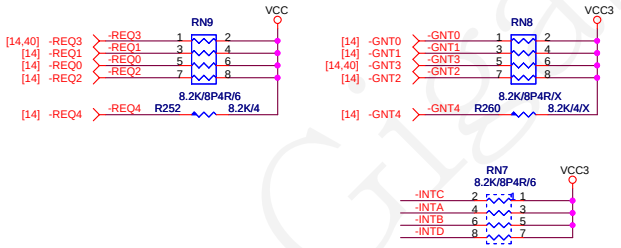
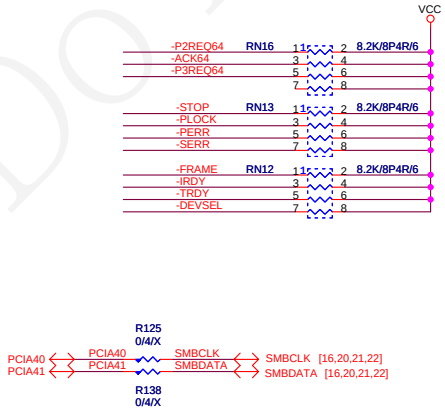


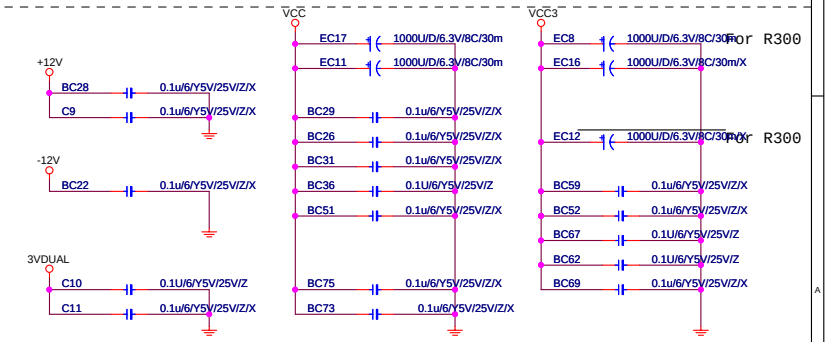
GIGABYTE CORP.		
Title: PCI E SLOT 1, 2		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 22 of 41	

PCI SLOT 1,2



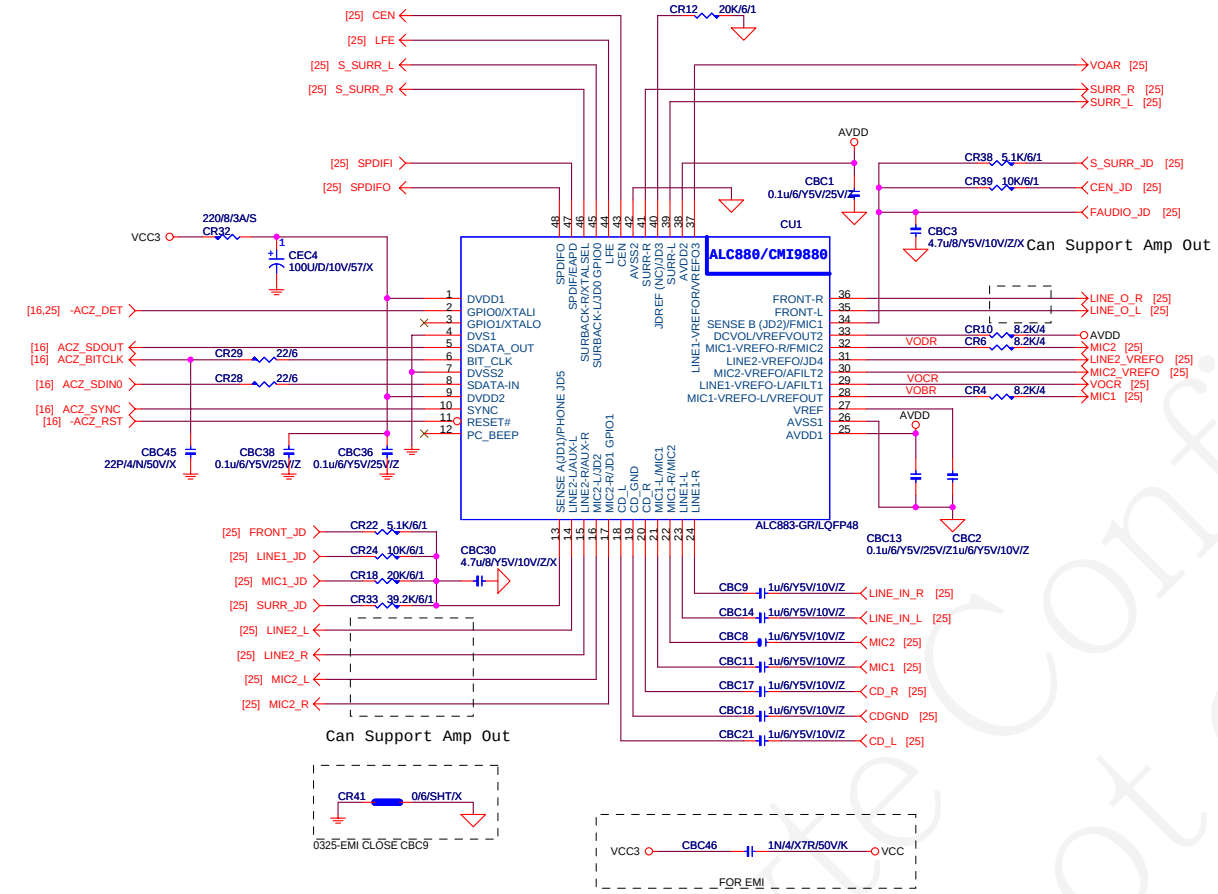






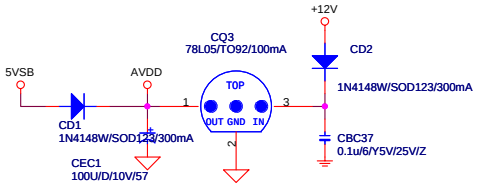
GIGABYTE CORP.		
Title: PCI SLOT 1,2		
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 23 of 41	

AZALIA CODEC

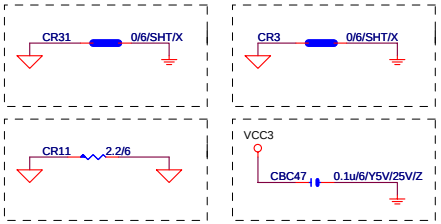


GIGABYTE CORP.		
Title: AZALIA-ALC883		
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 24 of 41	

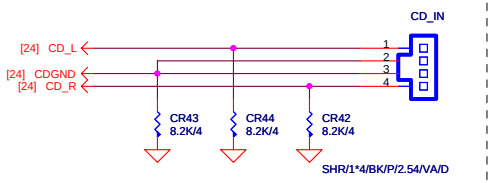
CODEC POWER/EMI PAD

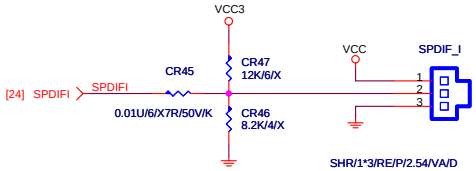


FOR EMI

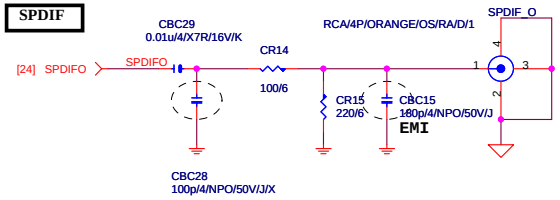


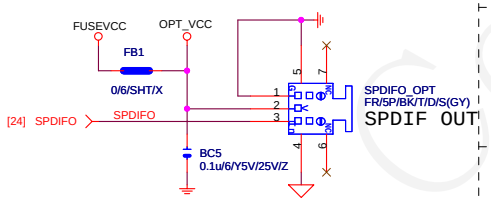
CD IN





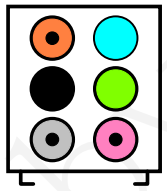
SPDIF



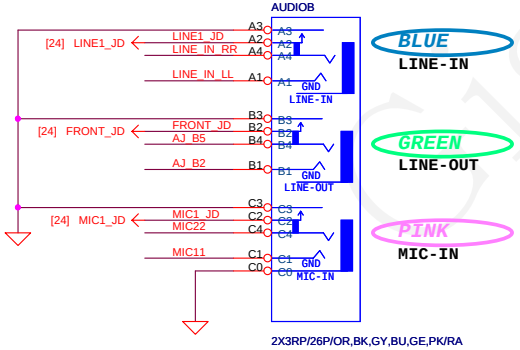


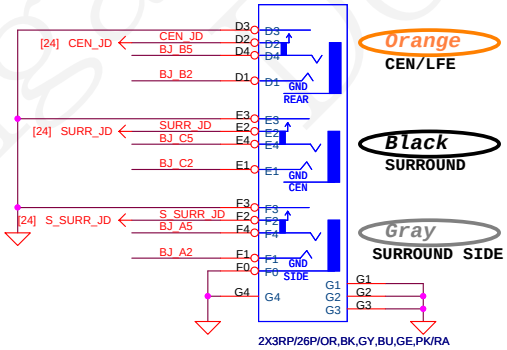
AZALIA JACK

BTX AZALIA CONNECTOR

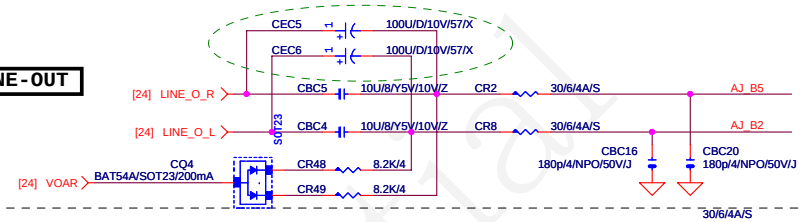


11NR6-403007-21

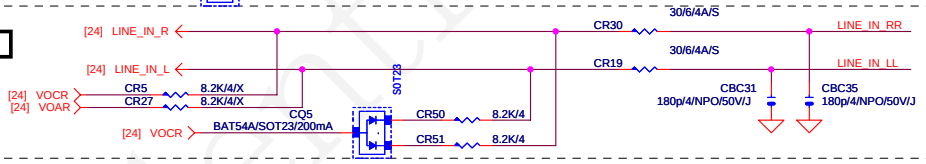




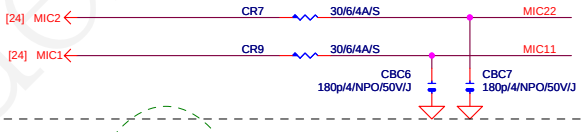
LINE-OUT



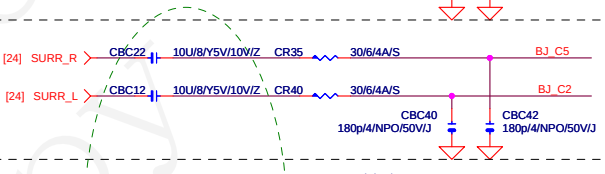
LINE-IN



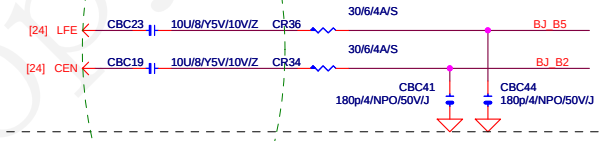
MIC-IN



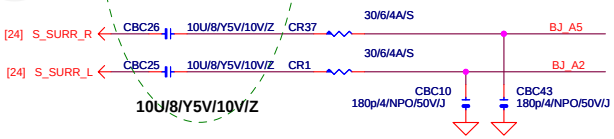
SURROUND



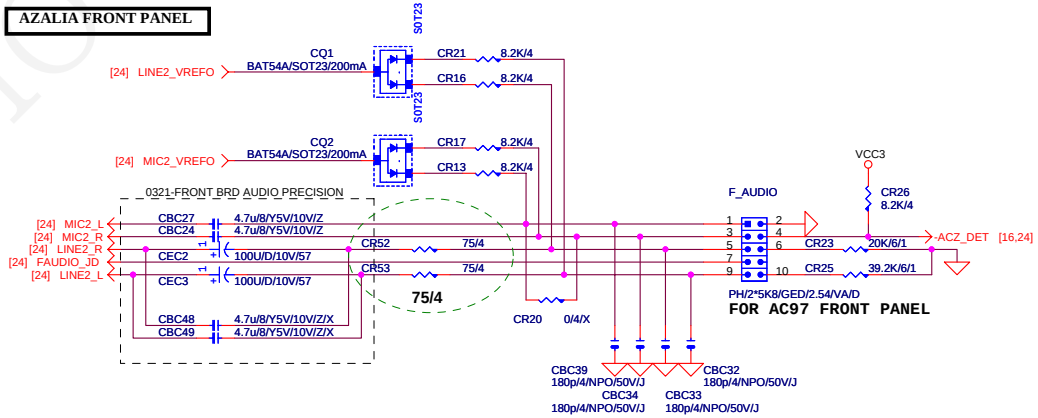
CEN/LFE



SURR BACK

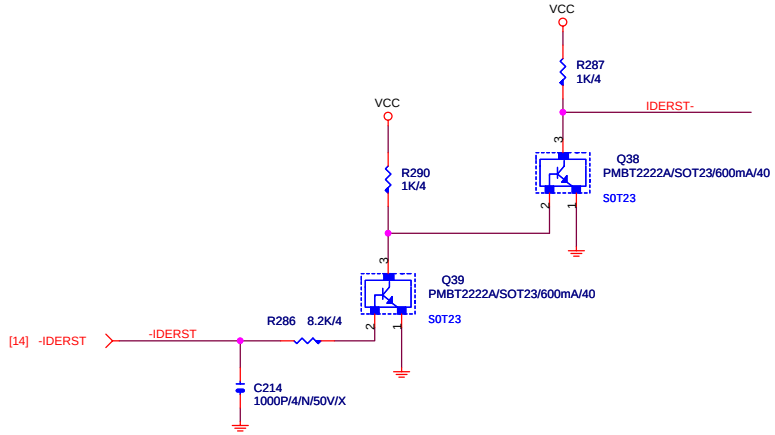


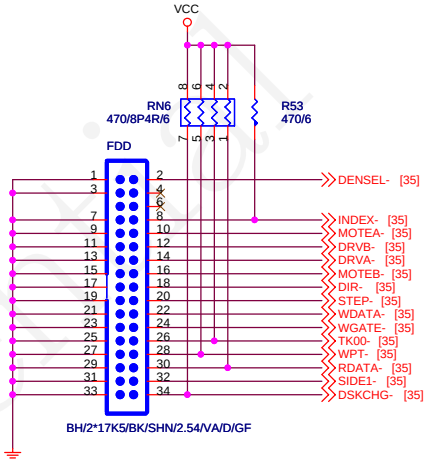
AZALIA FRONT PANEL

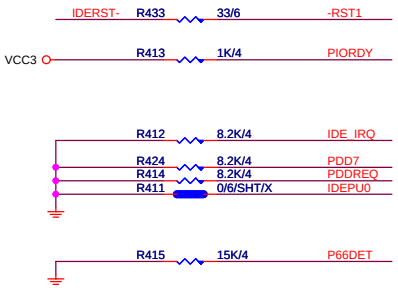


GIGABYTE CORP.

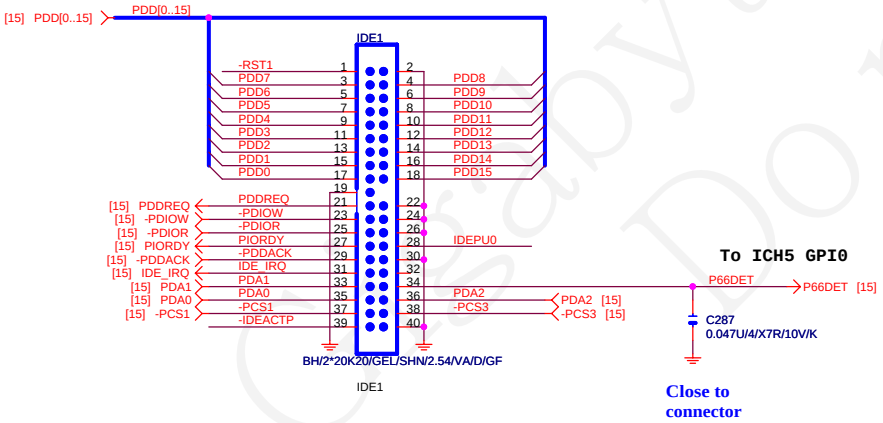
Title	AUDIO JACK	
Size: Custom	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 25 of 41	

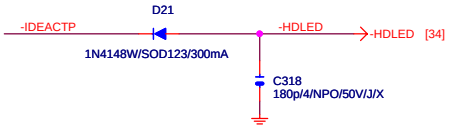




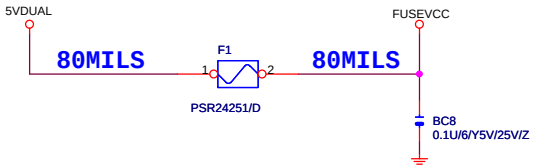


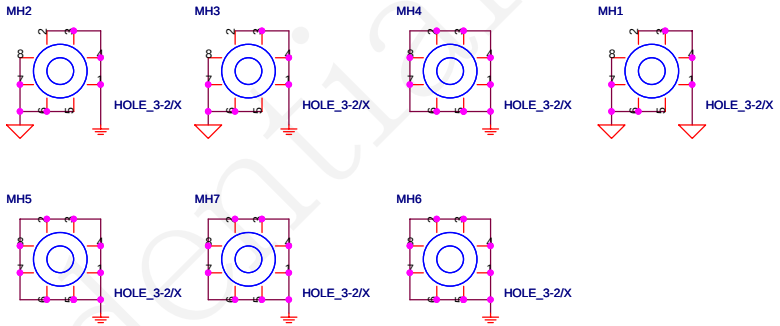
PRIMARY IDE CONNECTOR

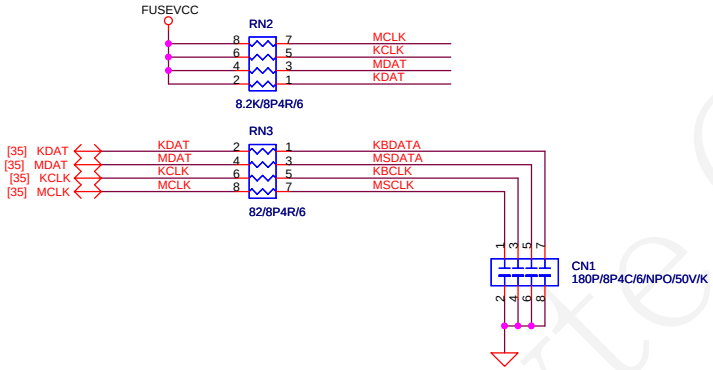


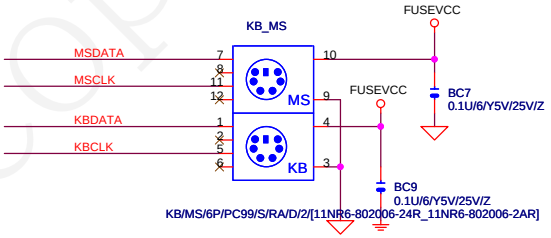


GIGABYTE CORP.		
Title: IDE CONNECTOR		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.1
Date:	Sheet 26 of 41	









GIGABYTE CORP.

Title	KB & PS2 MOUSE & IR	
Size B	Document Number GA-M57SLI-S4	Rev 1.1
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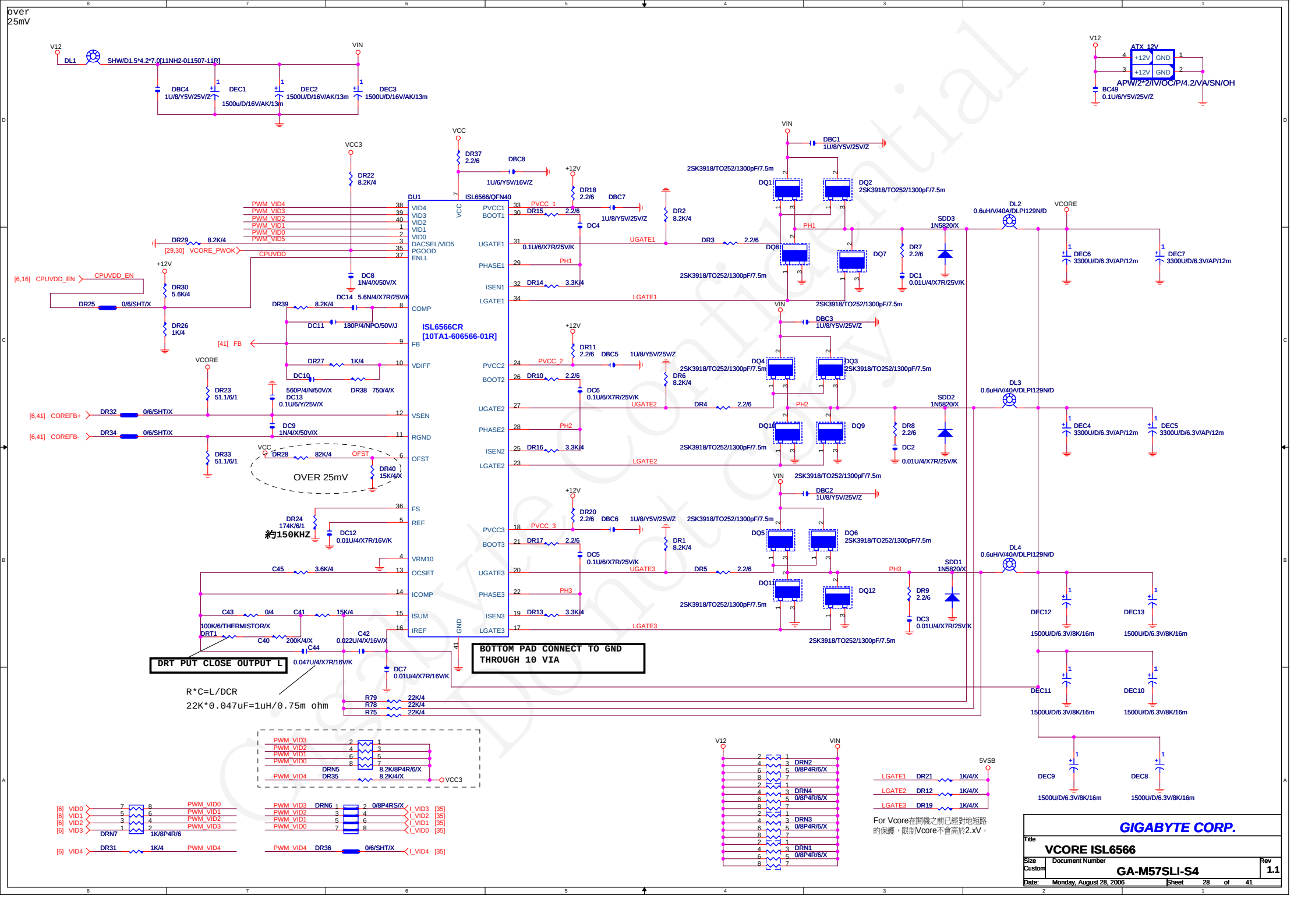
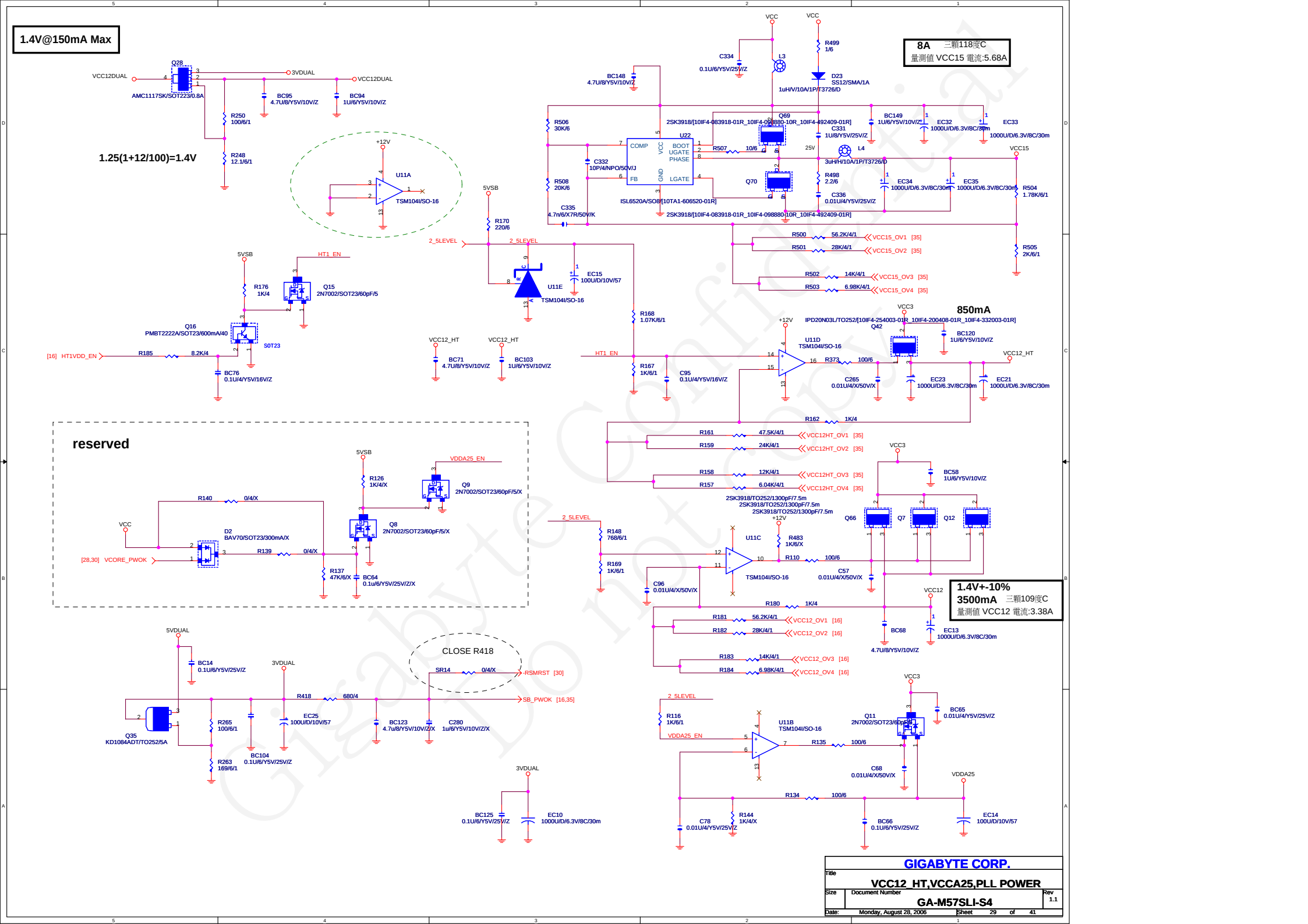
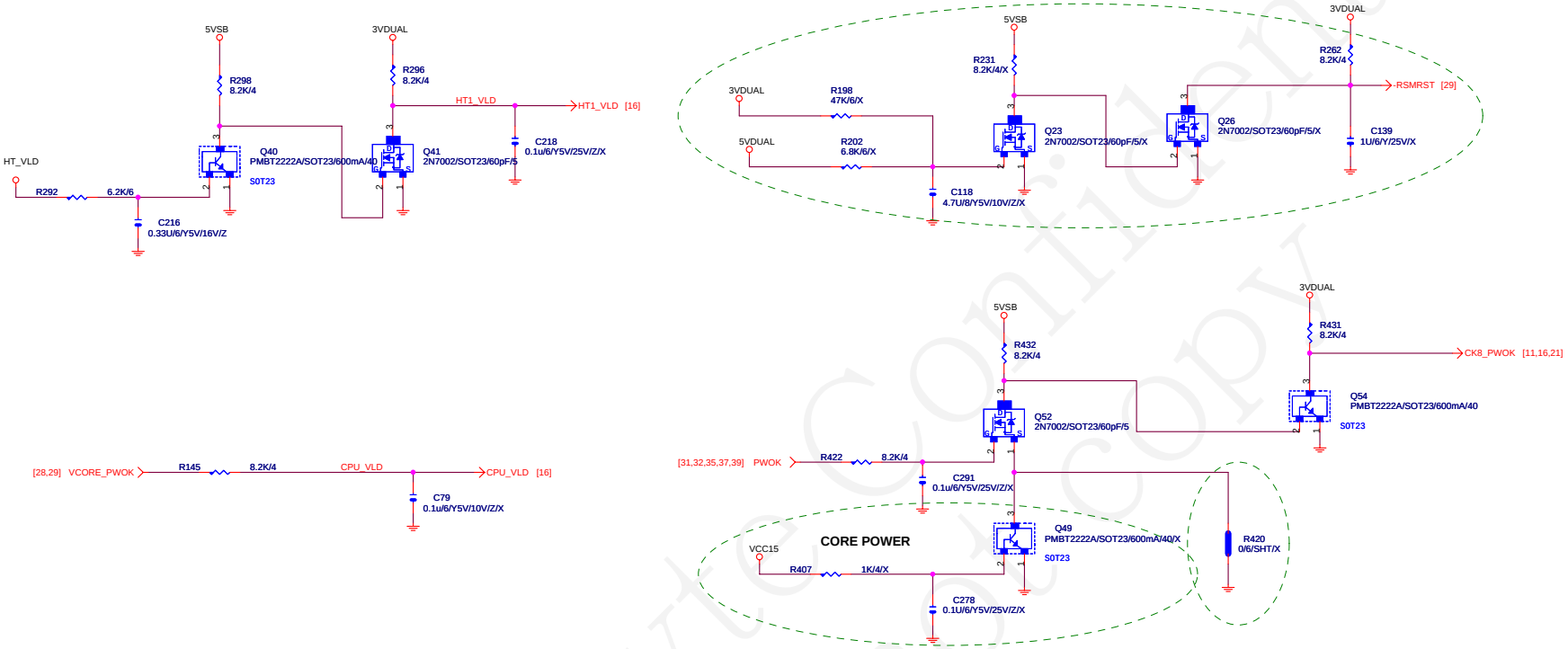
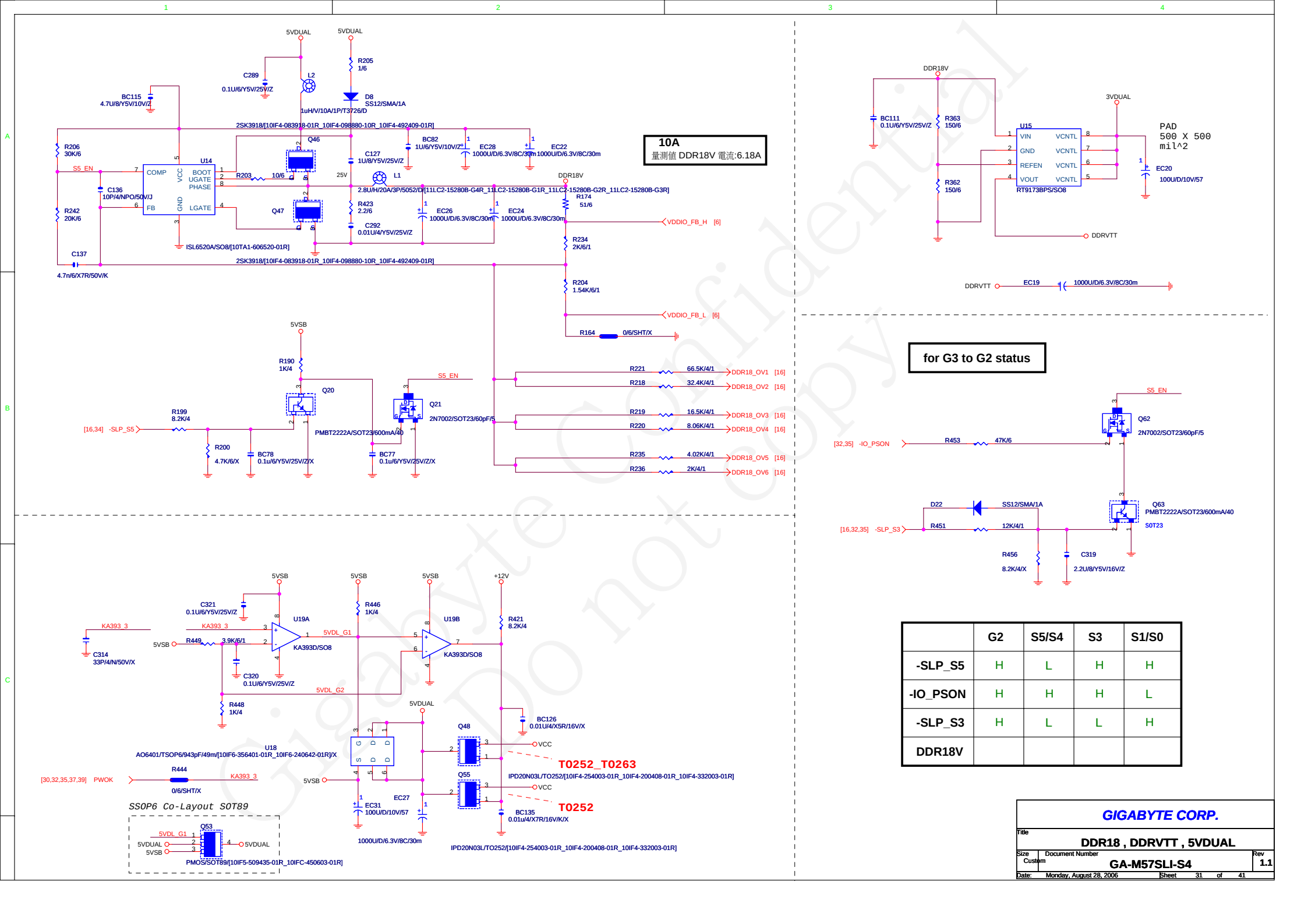

over
25mV
ISL6566CR
[10TA1-606566-01R]
ISL6566/QFN40
OVER 25mV
BOTTOM PAD CONNECT TO GND
THROUGH 10 VIA
DRT PUT CLOSE OUTPUT L
約150KHZ
R*C=L/DCR
22K*0.047uF=1uH/0.75m ohm
APW/2*2/IV/OC/P/4.2/VA/SN/OH
For Vcore在開機之前已經對地短路
的保護，限制Vcore不會高於2.xV。
GIGABYTE CORP.
VCORE ISL6566
GA-M57SLI-S4
Rev 1.1
Monday, August 28, 2006
Sheet 28 of 41
Gigabyte Confidential
Do not copy



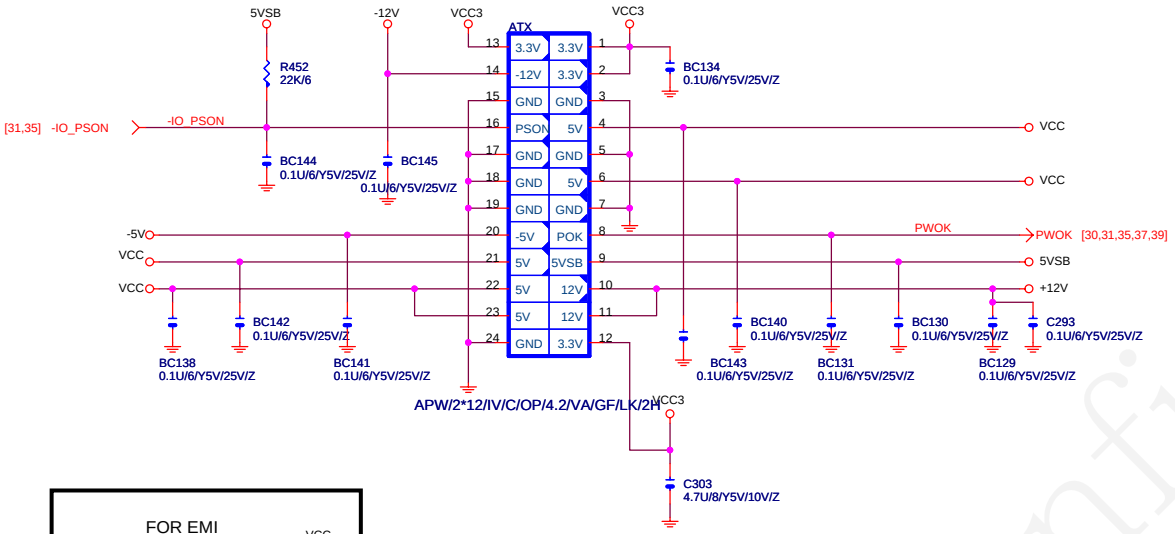


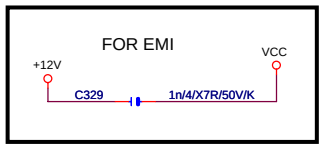
GIGABYTE CORP.		
Title: POWER SEQUENCE POWER		
Size	Document Number: GA-M57SLI-S4	Rev: 1.1
Date: Monday, August 28, 2006	Sheet 30 of 41	

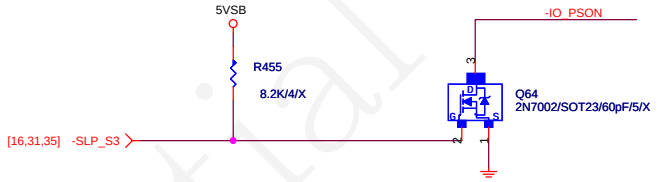


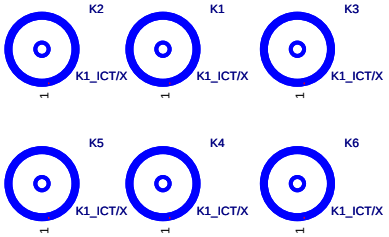
	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

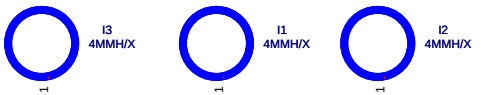
ATX POWER CONNECTOR



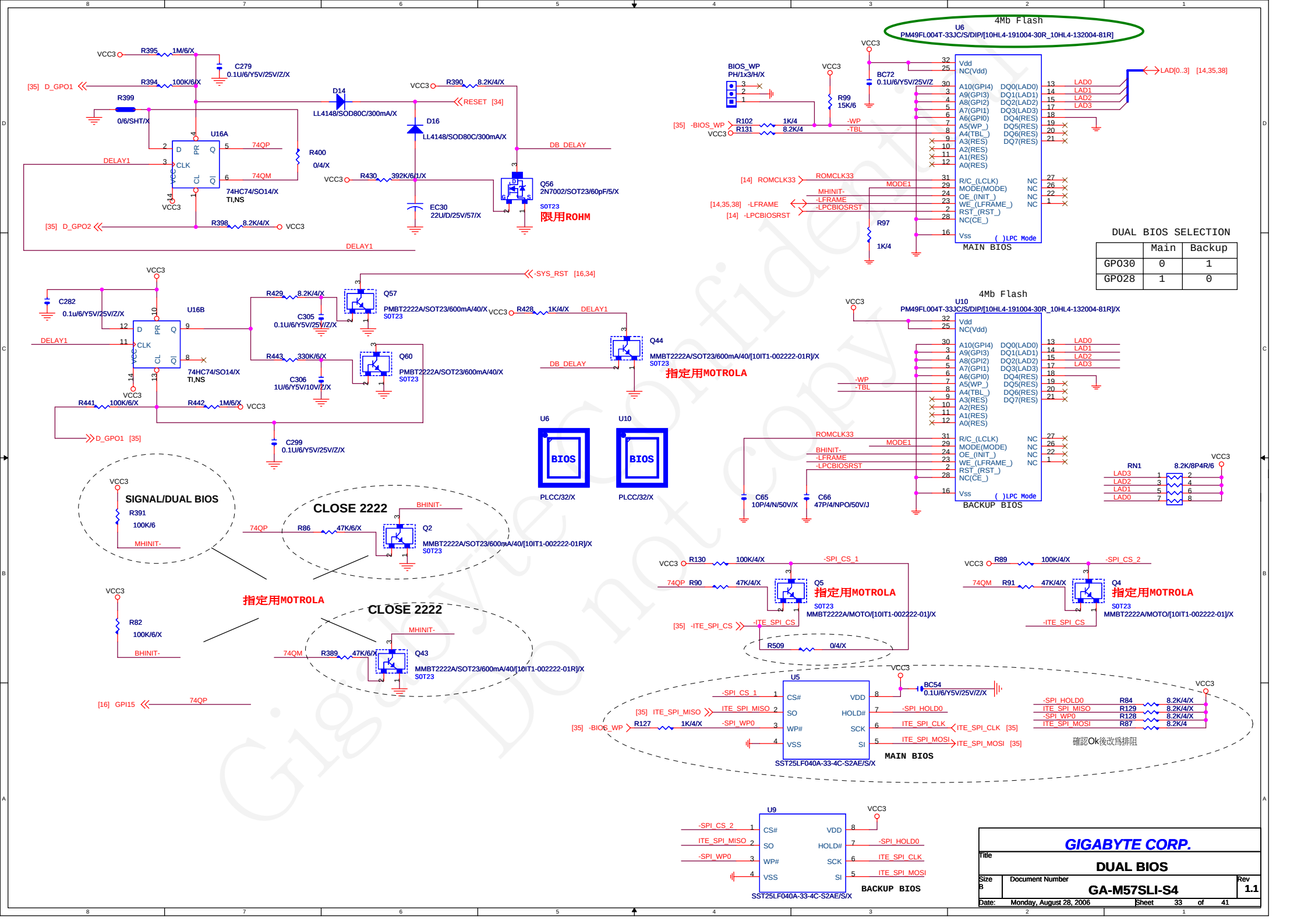


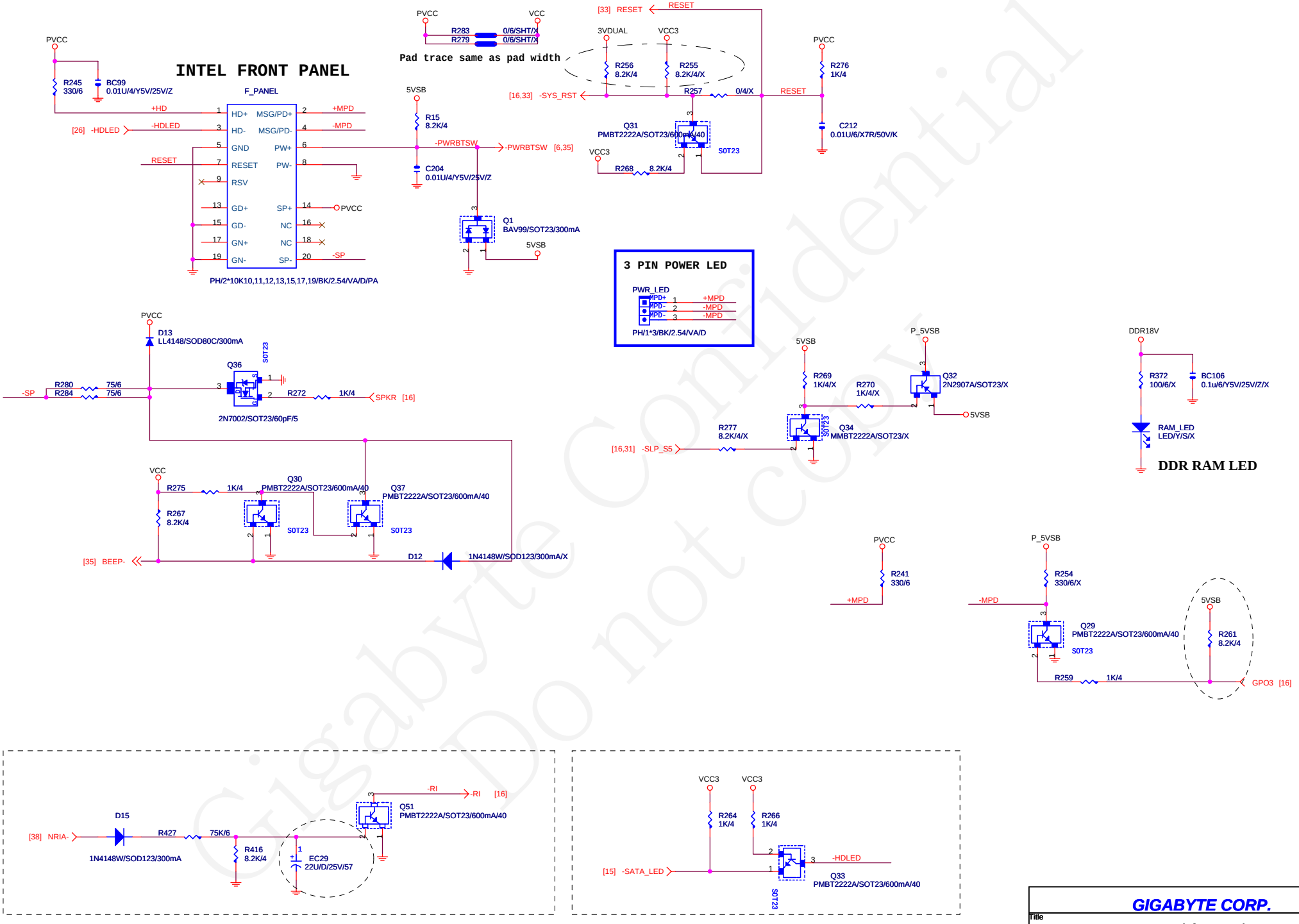






GIGABYTE CORP.		
Title: Misc. PWR & ATX CONN.		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.1
Date:	Sheet 32 of 41	


4Mb Flash
U6
PM49FL004T-33JC/S/DIP/[10HL4-191004-30R_10HL4-132004-81R]
MAIN BIOS
DUAL BIOS SELECTION
Main
Backup
GPO30
GPO28
4Mb Flash
U10
PM49FL004T-33JC/S/DIP/[10HL4-191004-30R_10HL4-132004-81R]/X
BACKUP BIOS
SIGNAL/DUAL BIOS
CLOSE 2222
CLOSE 2222
指定用MOTROLA
指定用MOTROLA
指定用MOTROLA
指定用MOTROLA
限用ROHM
MAIN BIOS
BACKUP BIOS
SST25LF040A-33-4C-S2AE/S/X
GIGABYTE CORP.
DUAL BIOS
GA-M57SLI-S4
1.1
Monday, August 28, 2006
33
41



GIGABYTE CORP.

Title	PANEL & STR LED & RI
Size	B
Document Number	GA-M57SLI-S4
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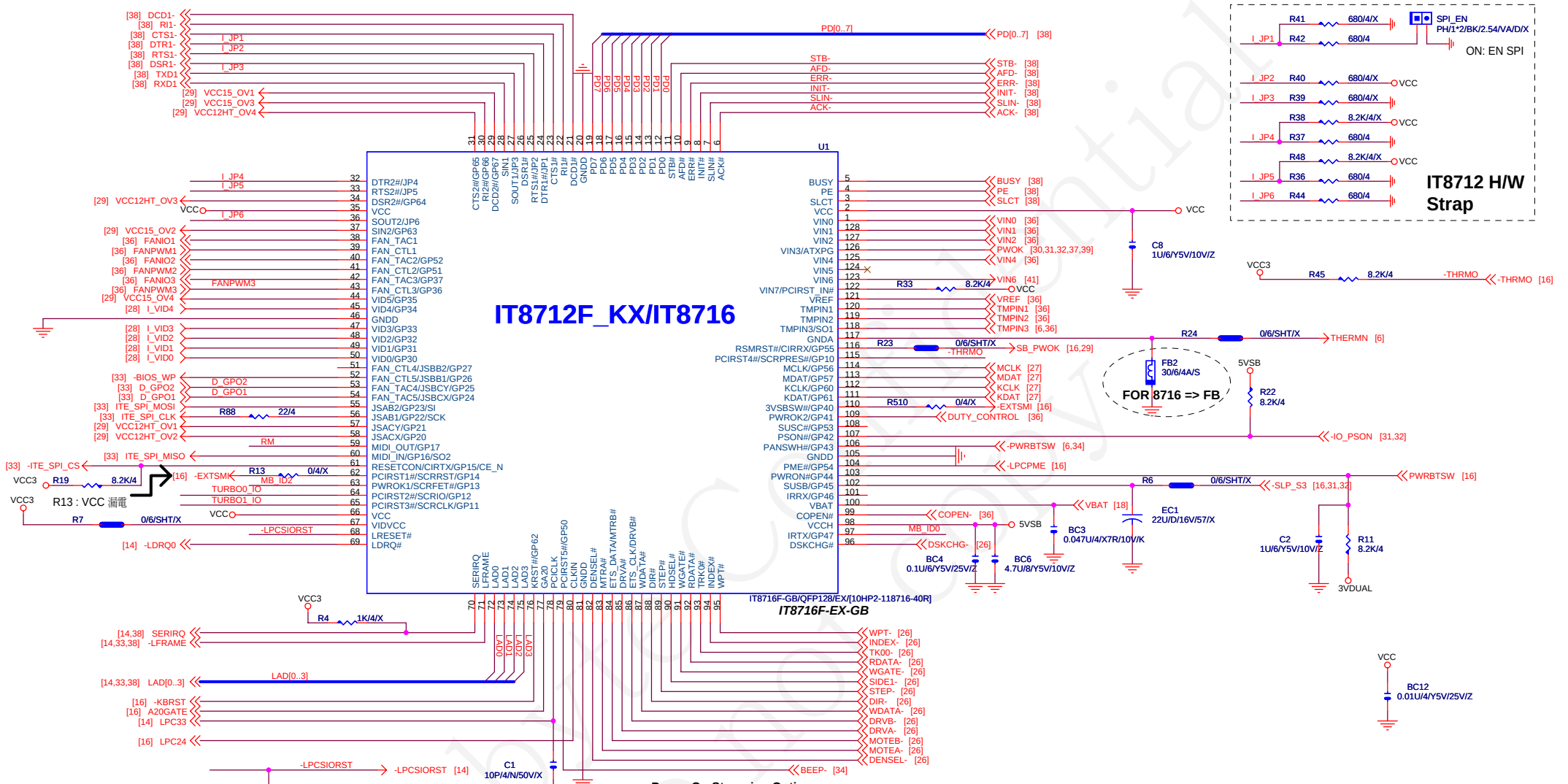

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled En SPI Flash
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h (Duty=100%)
		0	The default value of EC Index 15h / 16h / 17h is 40h (Duty=50%)
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

GIGABYTE CORP.

Title	ITE 8712 LPC IO
Size	B
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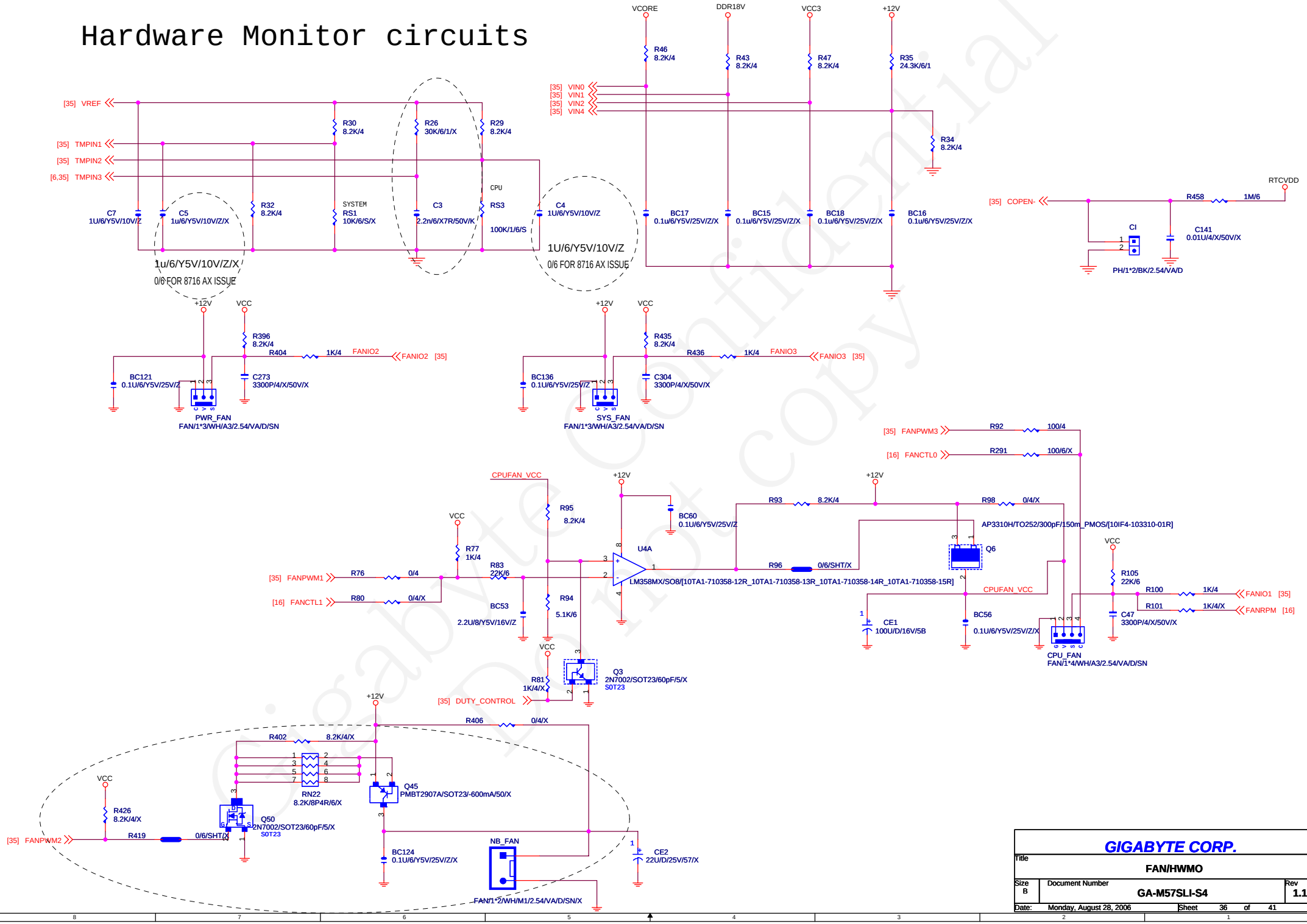
Hardware Monitor circuits



GIGABYTE CORP.		
Title: FAN/HWMO		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.1
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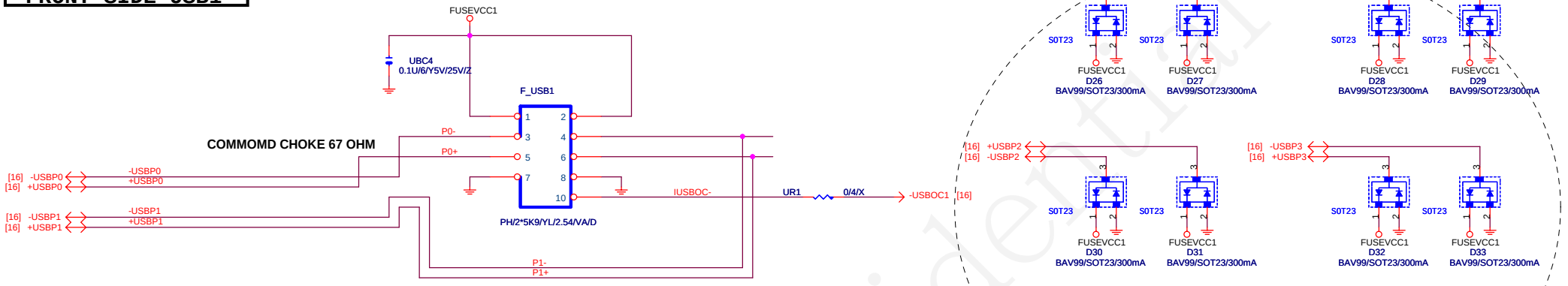
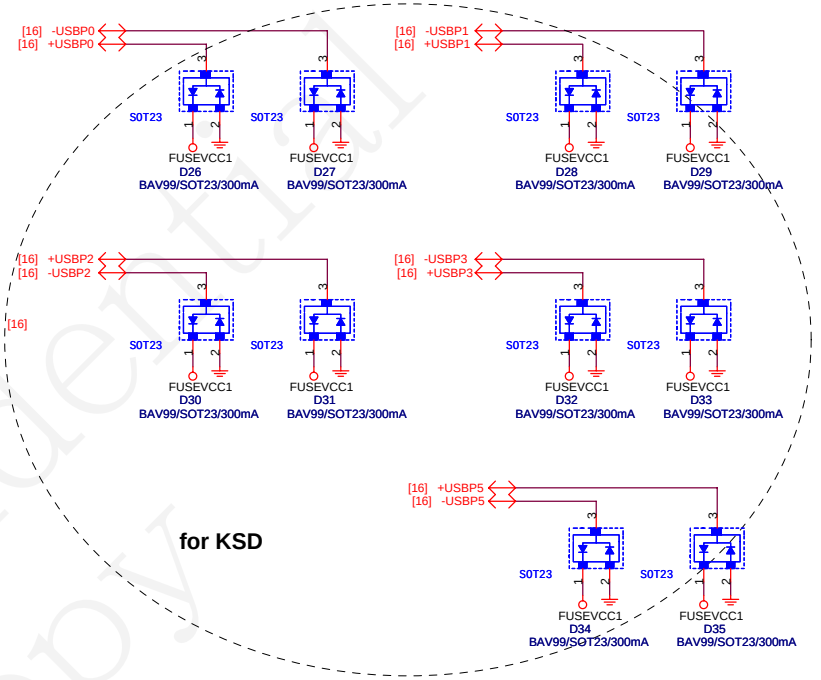
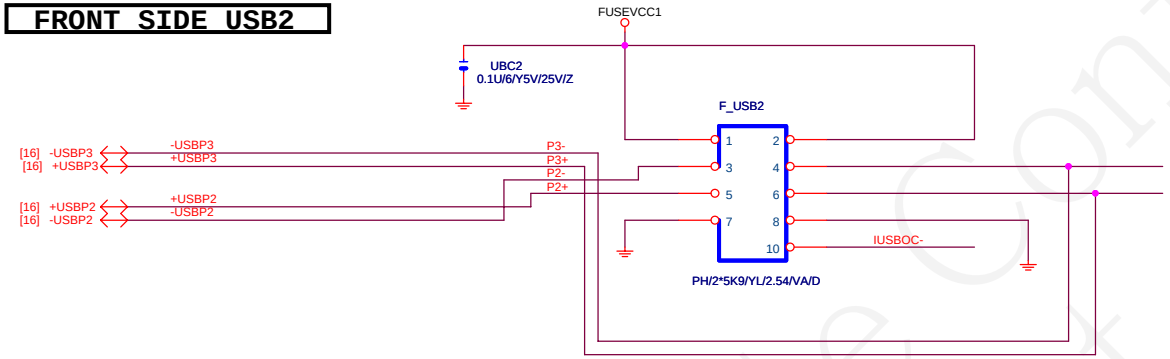
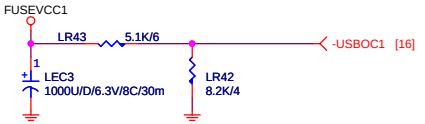
FRONT SIDE USB1



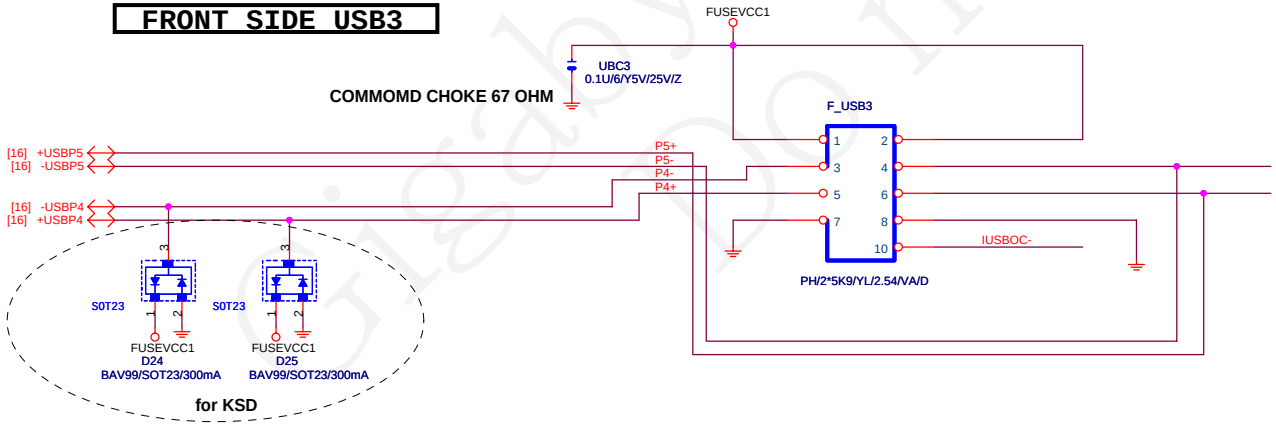


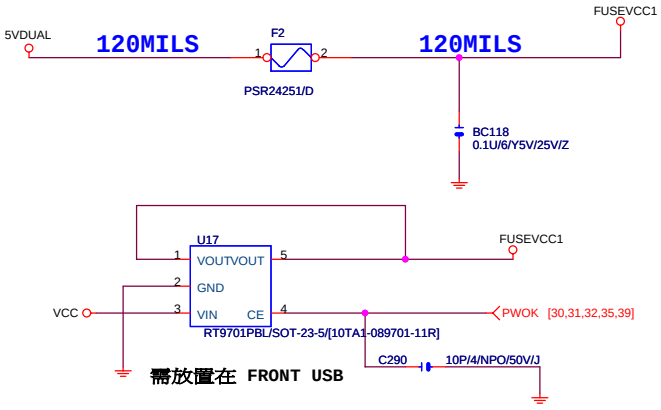
FRONT SIDE USB2



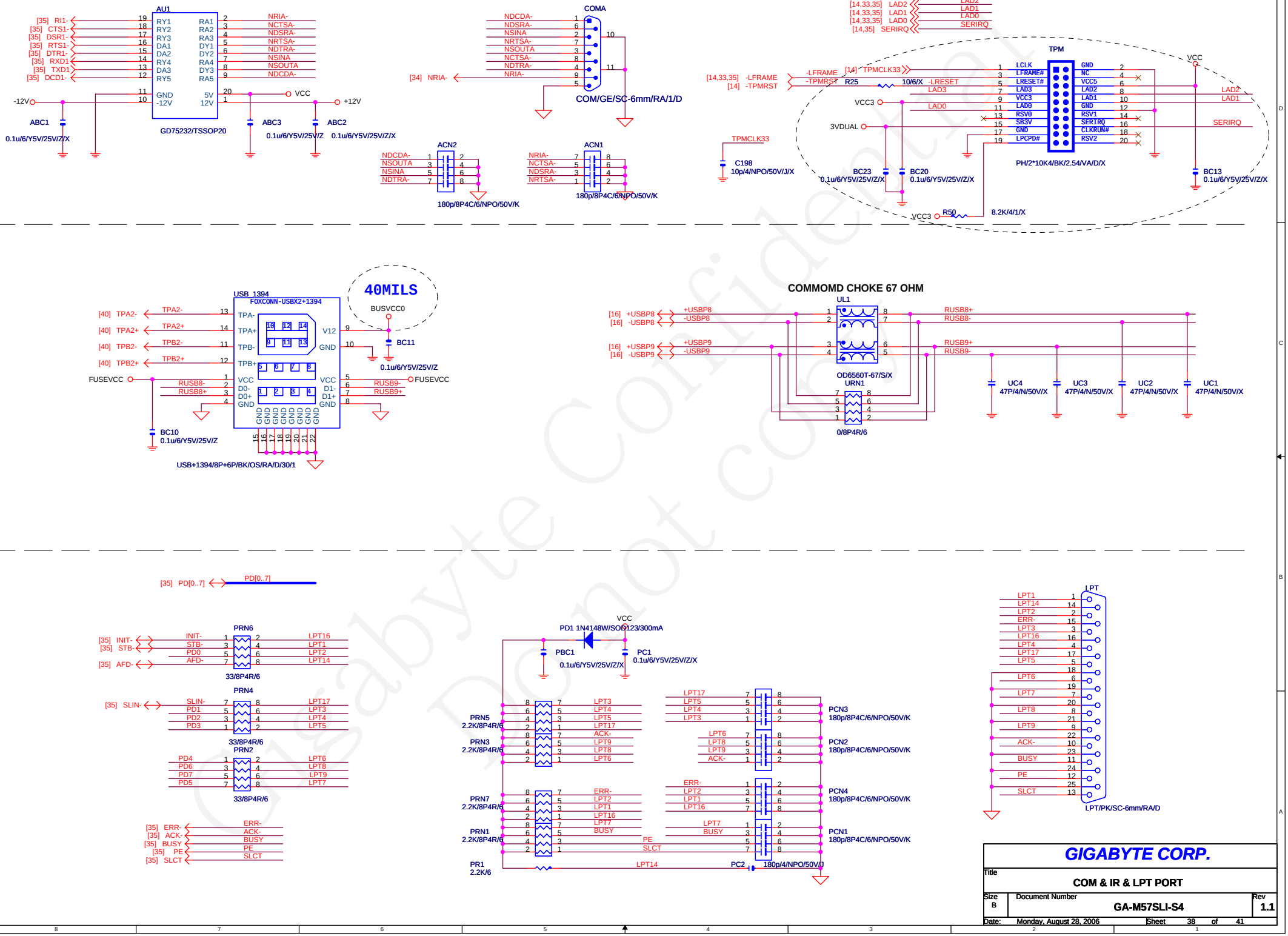


FRONT SIDE USB3





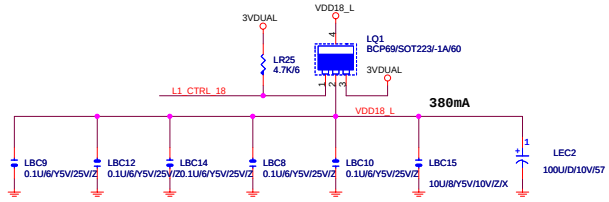
GIGABYTE CORP.		
Title: USB PORT		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.1
Date:	Sheet 37 of 41	

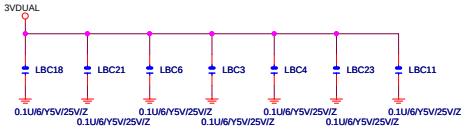


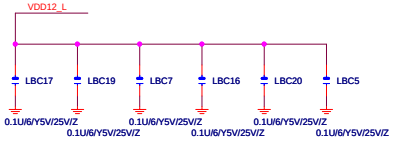
E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

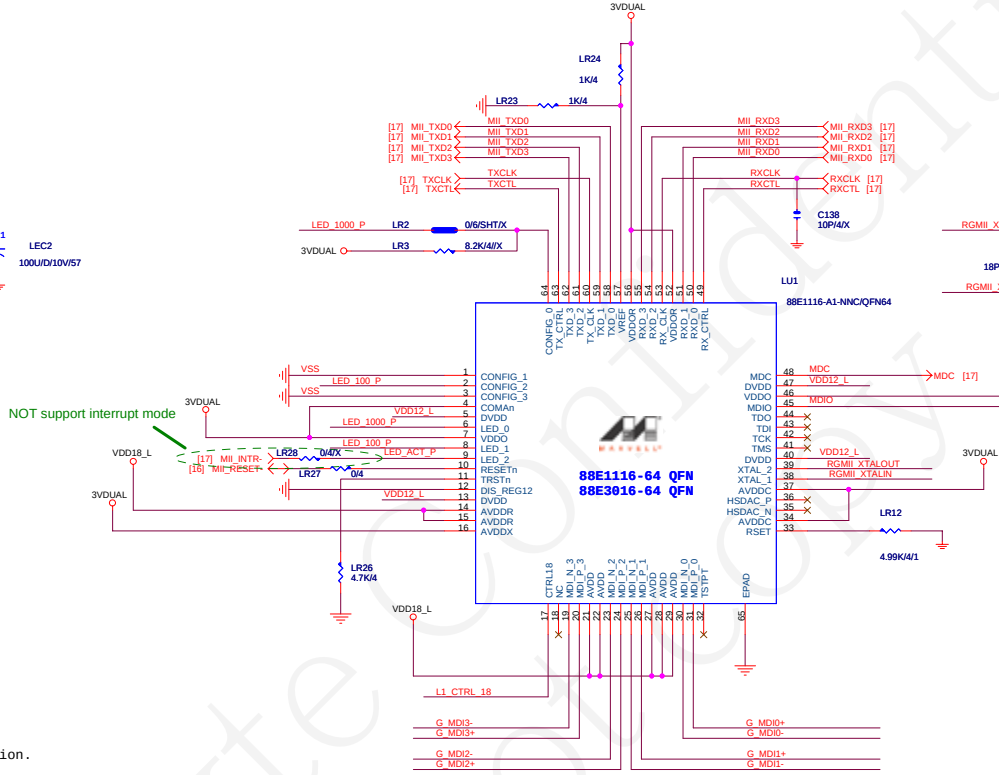
Hardware Configuration: See config _0:4

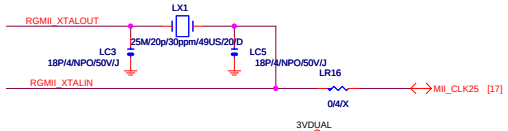
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



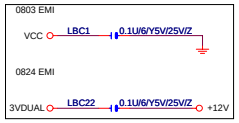


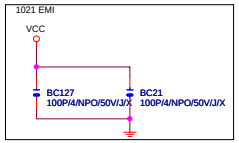




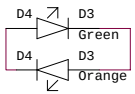


Bypass cap can share. User check it by layout consideration.

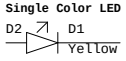


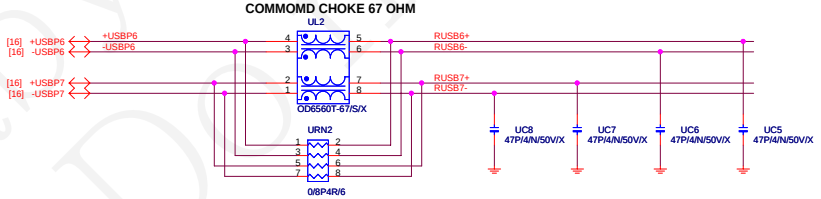


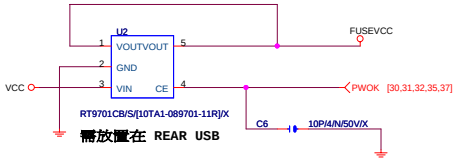
Dual Color LED

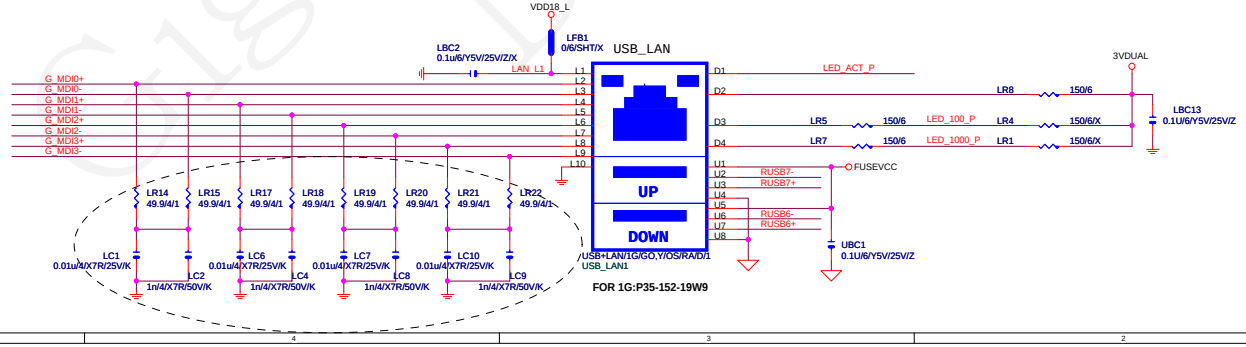


Single Color LED

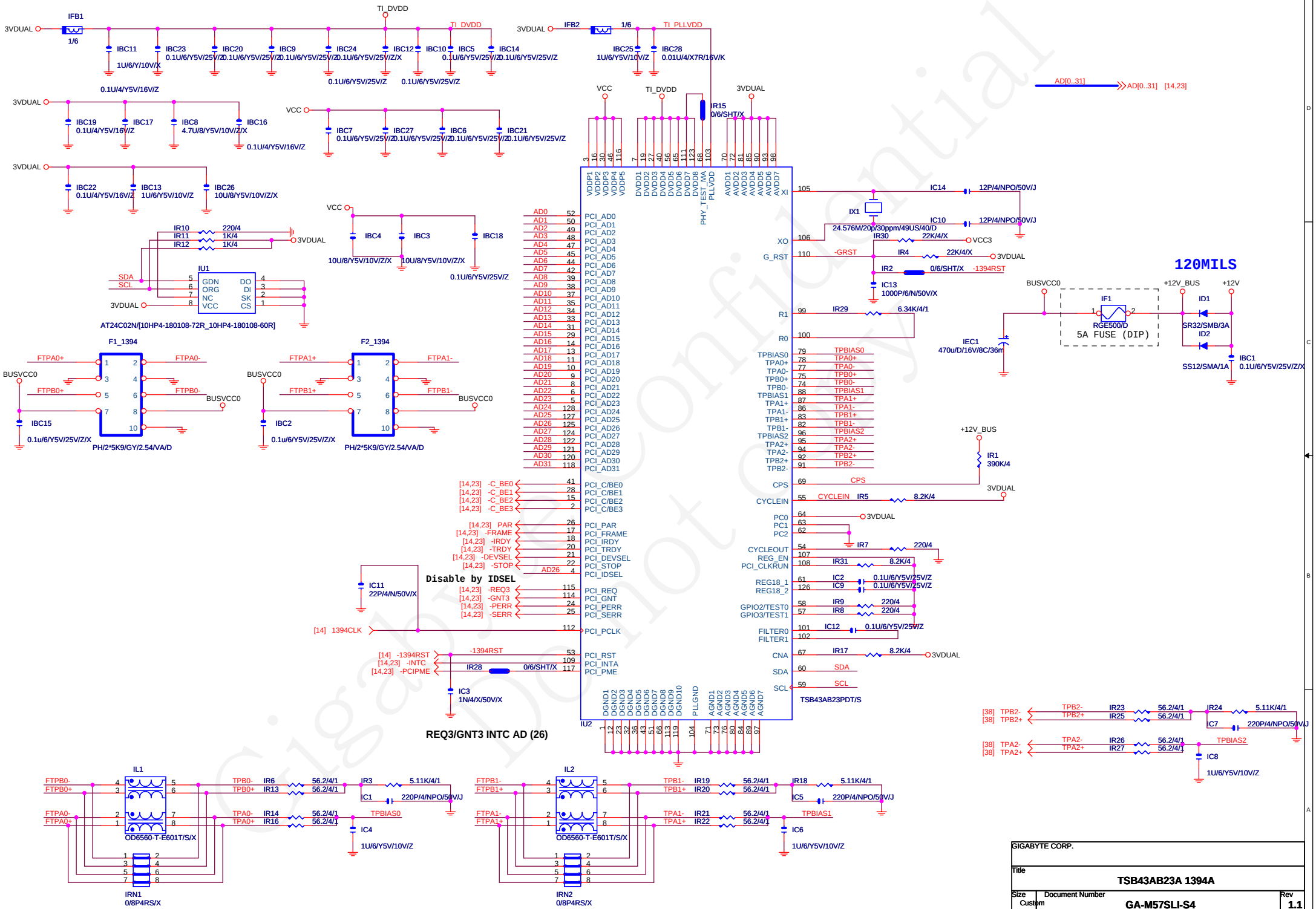


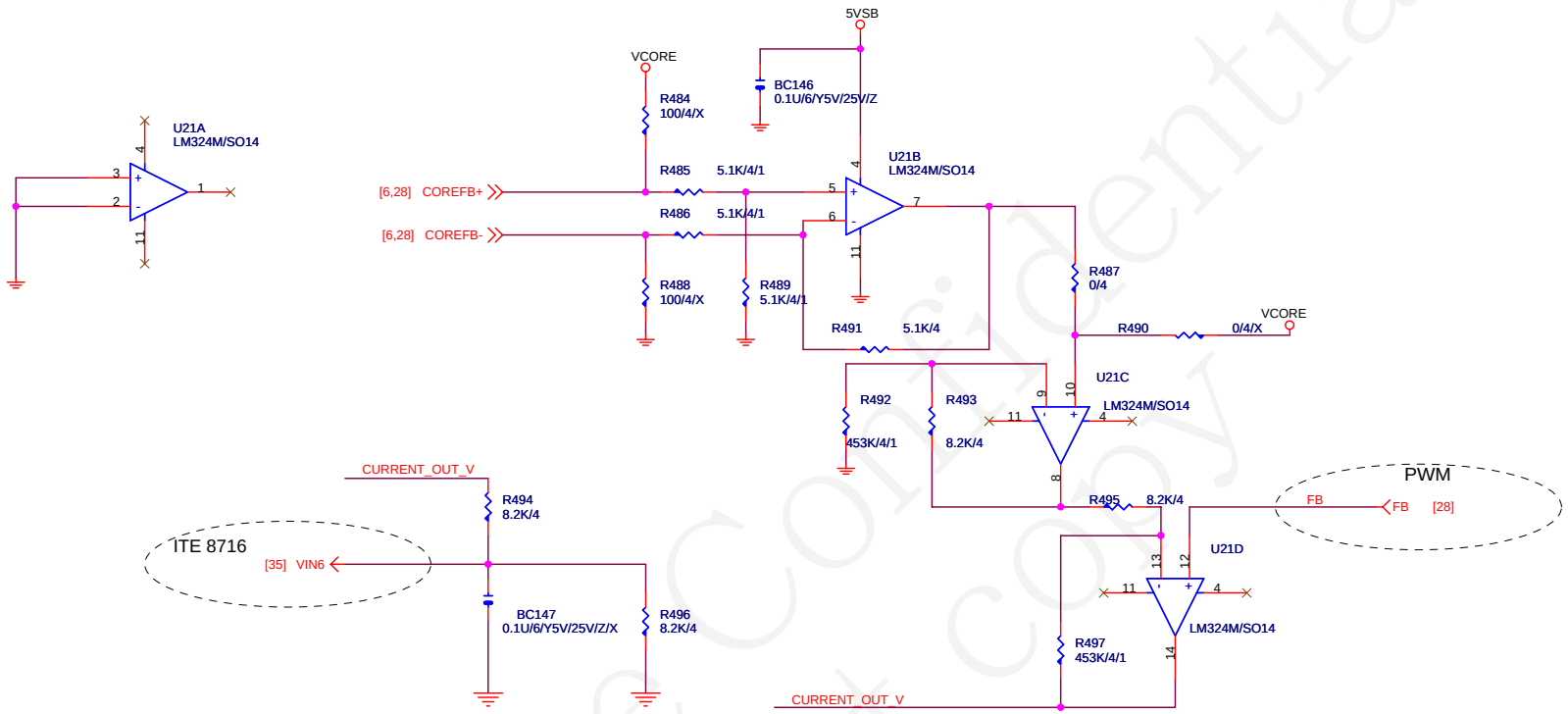






Title	Marvell_88E1115_88E1116_88E3016	
Size C	Document Number GA-M57SLI-S4	Rev 1.1
Date: Monday, August 28, 2006	Sheet 39 of 41	


IU2
TSB43AB23PDT/S
IU1
AT24C02N/[10HP4-180108-72R_10HP4-180108-60R]
IL1
IL2
OD6560-T-E601T/S/X
IRN1
IRN2
0/8P4RS/X
F1_1394
F2_1394
PH/2*5K9/GY/2.54/VA/D
IF1
RGE500/D
5A FUSE (DIP)
120MILS
Disable by IDSEL
REQ3/GNT3 INTC AD (26)
GIGABYTE CORP.
Title
TSB43AB23A 1394A
Size
Custom
Document Number
GA-M57SLI-S4
Rev
1.1
Date:
Thursday, November 22, 2007
Sheet
40
of
41



GIGABYTE CORP.		
Title: CURRENT_OUT		
Size: B	Document Number: GA-M57SLI-S4	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 41 of 41	