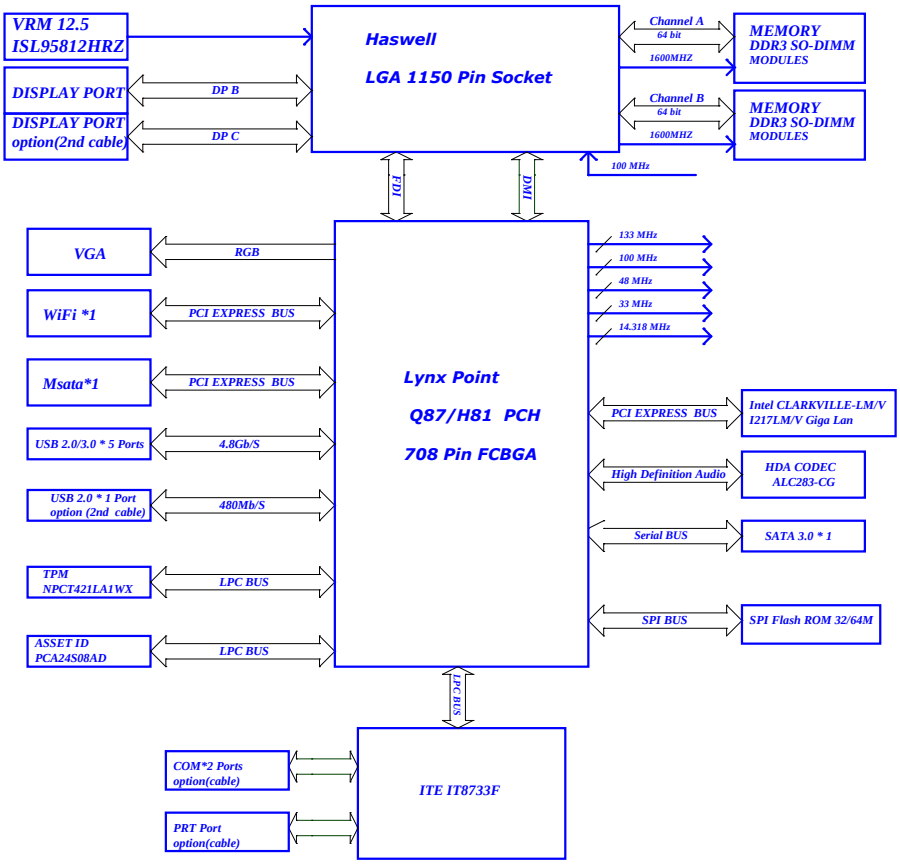
JC184/JC186

Project JC184/JC186

Document No : A116/A1232

A04: 2014/09/19

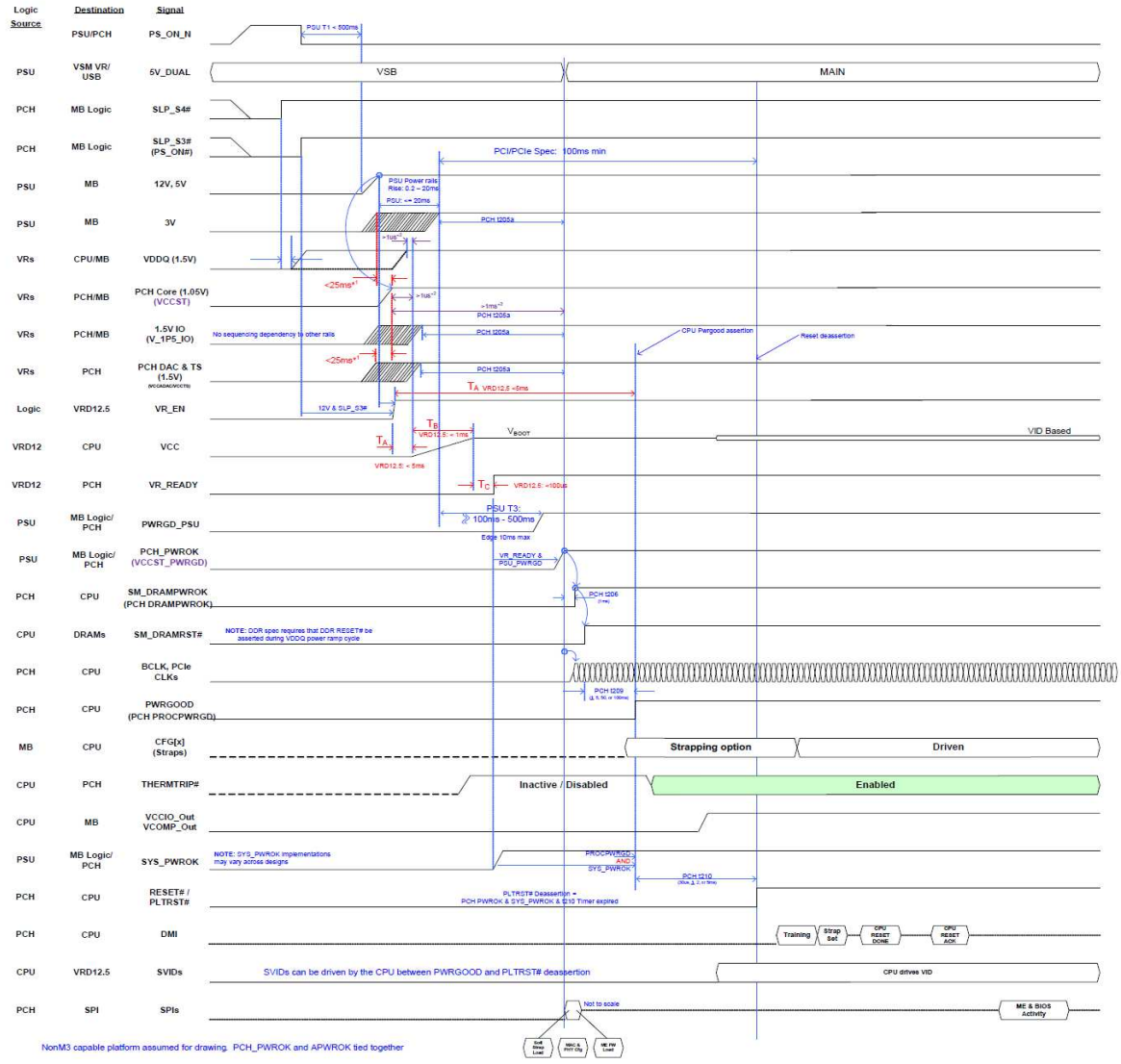


LITE-ON TECHNOLOGY CORP.	LITEON
Title	01. Block Diagram
Size: C	Document Number: JC184/JC186
Rev: A04	
Date: Tuesday, October 21, 2014	Sheet 1 of 62

50 -----

51 -----

52 -----



LITE-ON TECHNOLOGY CORP.	LITEON
Title	02. Power Sequence
Size: C	Document Number: JC184/JC186
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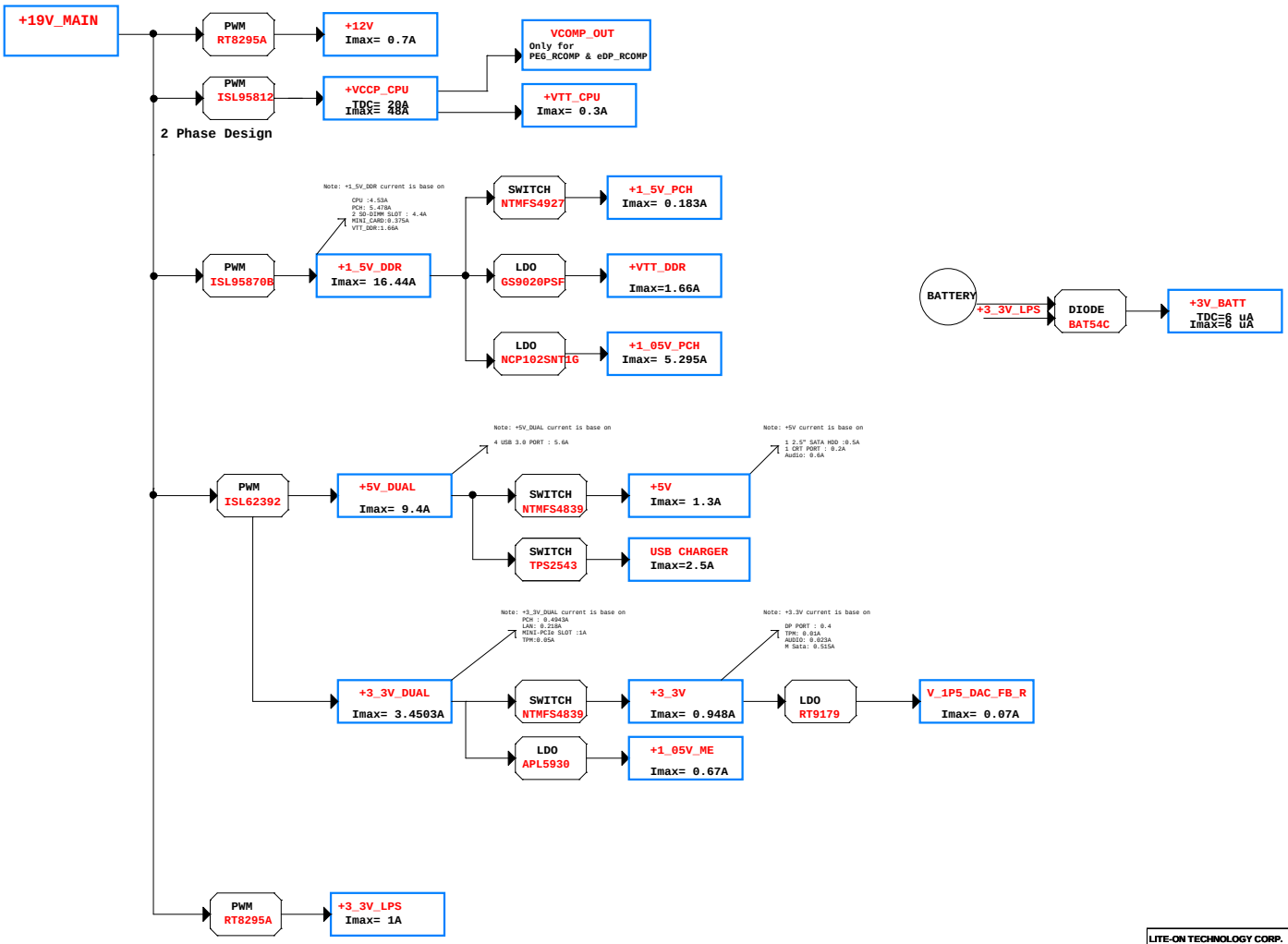
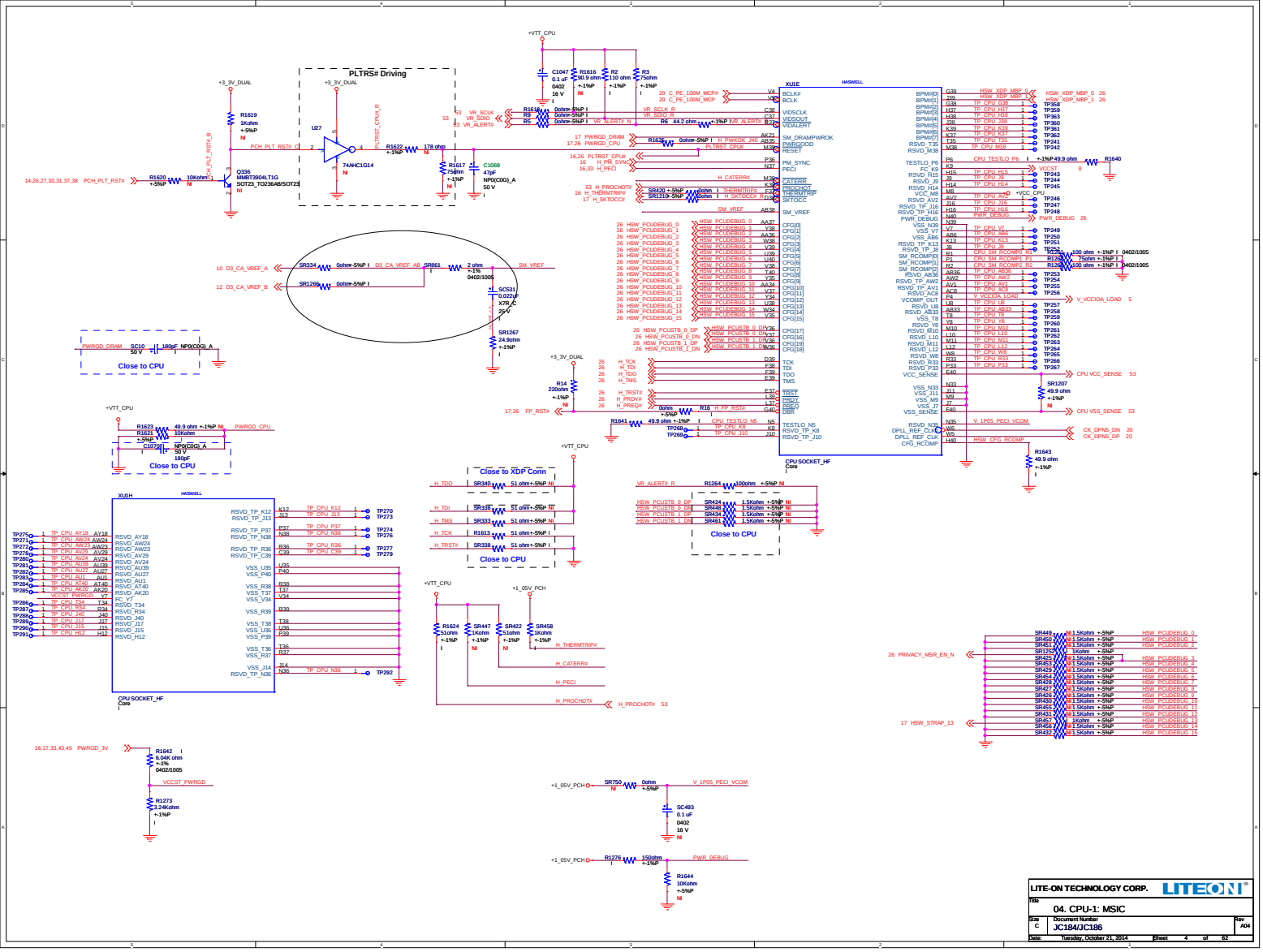
POWER CONN



LITE-ON TECHNOLOGY CORP.		
Title	03. Power Delivery Map	
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 3 of 62	


PLTRS# Driving
Close to CPU
Close to XDP Conn
Close to CPU
Close to CPU
Close to CPU
CPU SOCKET_HF
Core
LITE-ON TECHNOLOGY CORP.
LITEON
Title
04_CPU-1: MSIC
Size
C
Document Number
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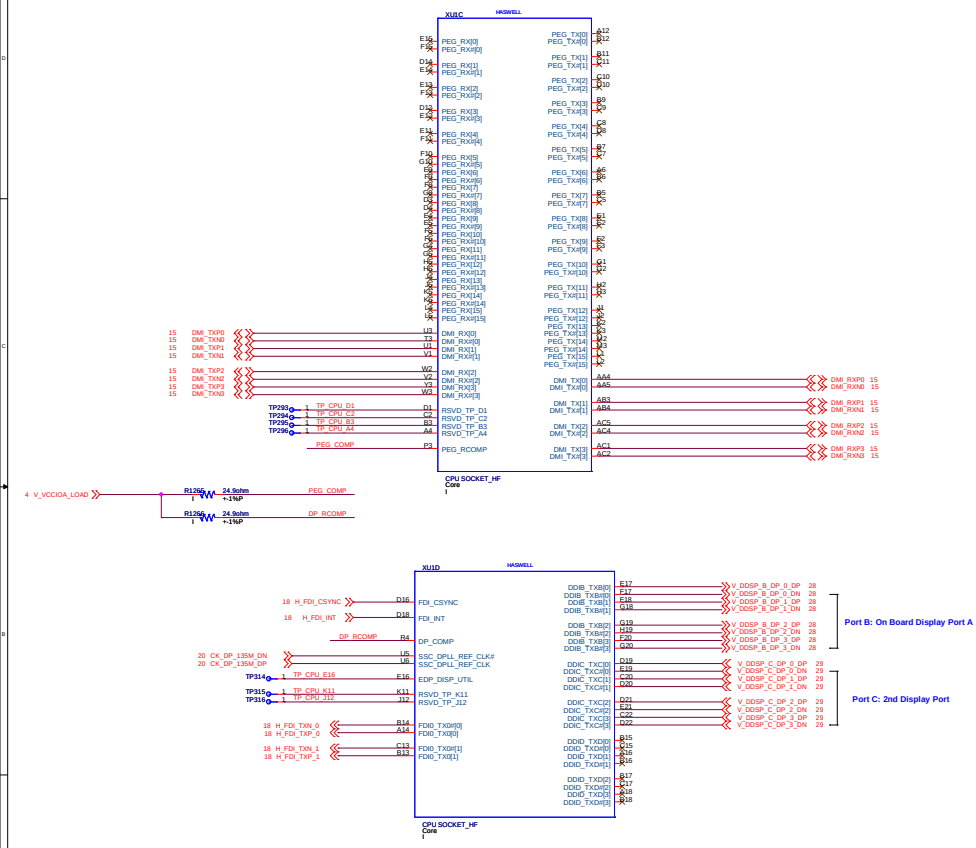
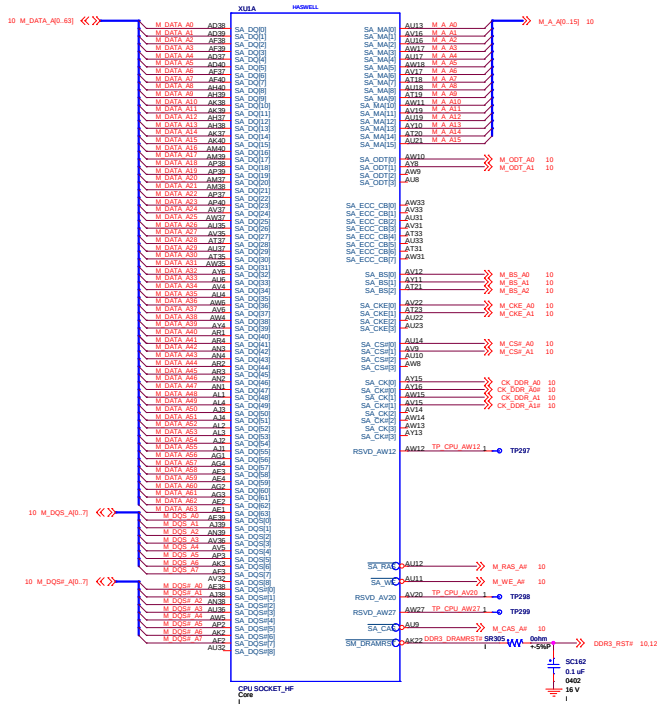
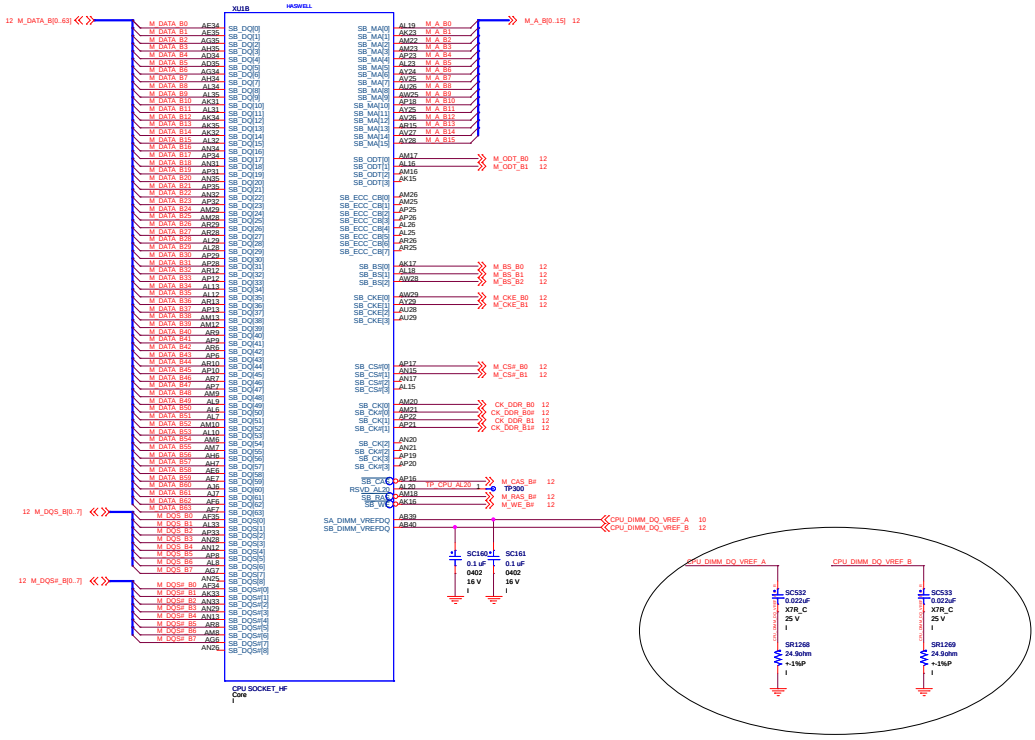
62



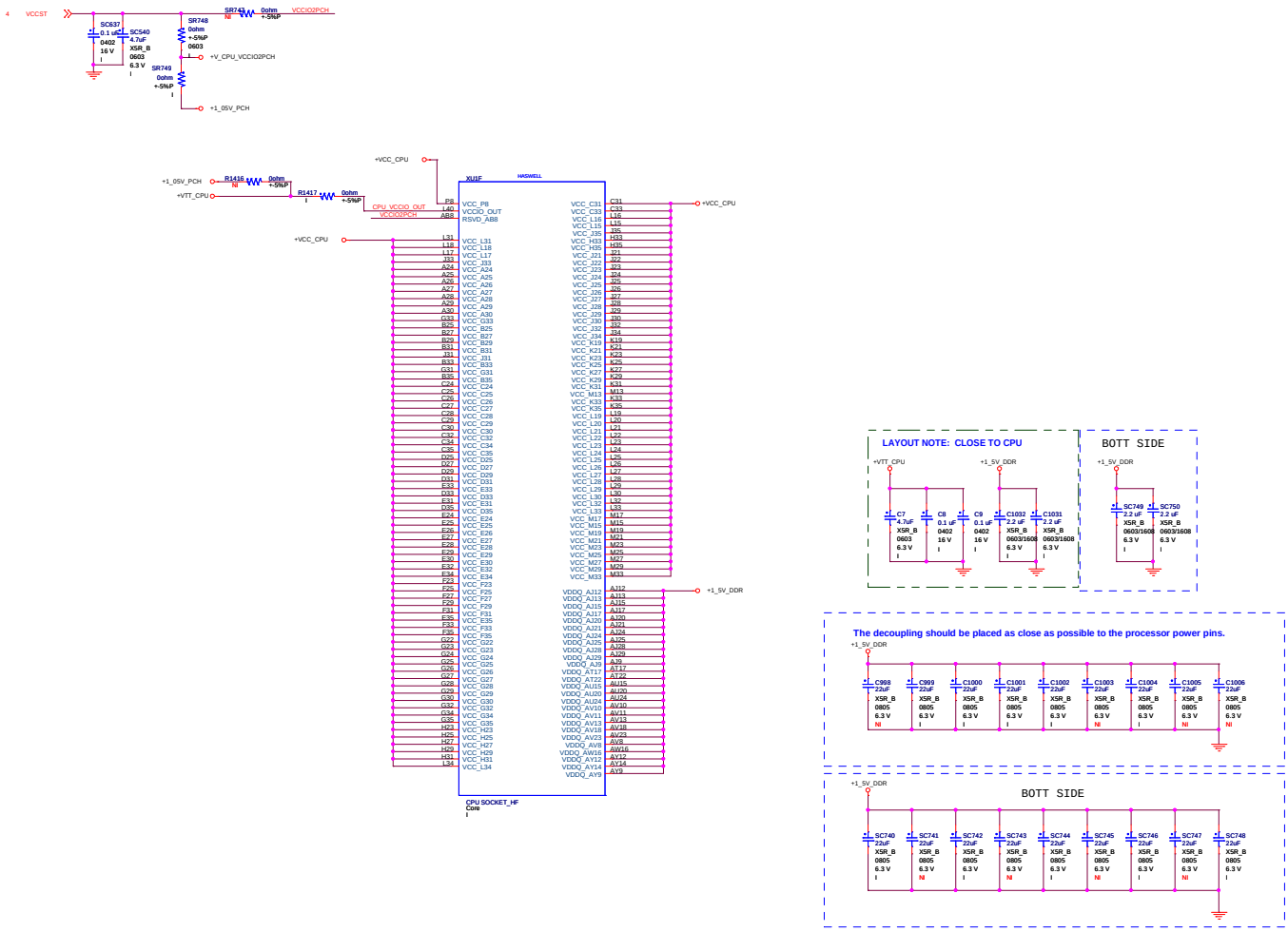
LITE-ON TECHNOLOGY CORP.			
Title	05. CPU-2: FDI/PCIe/DMI		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 5	of 62	



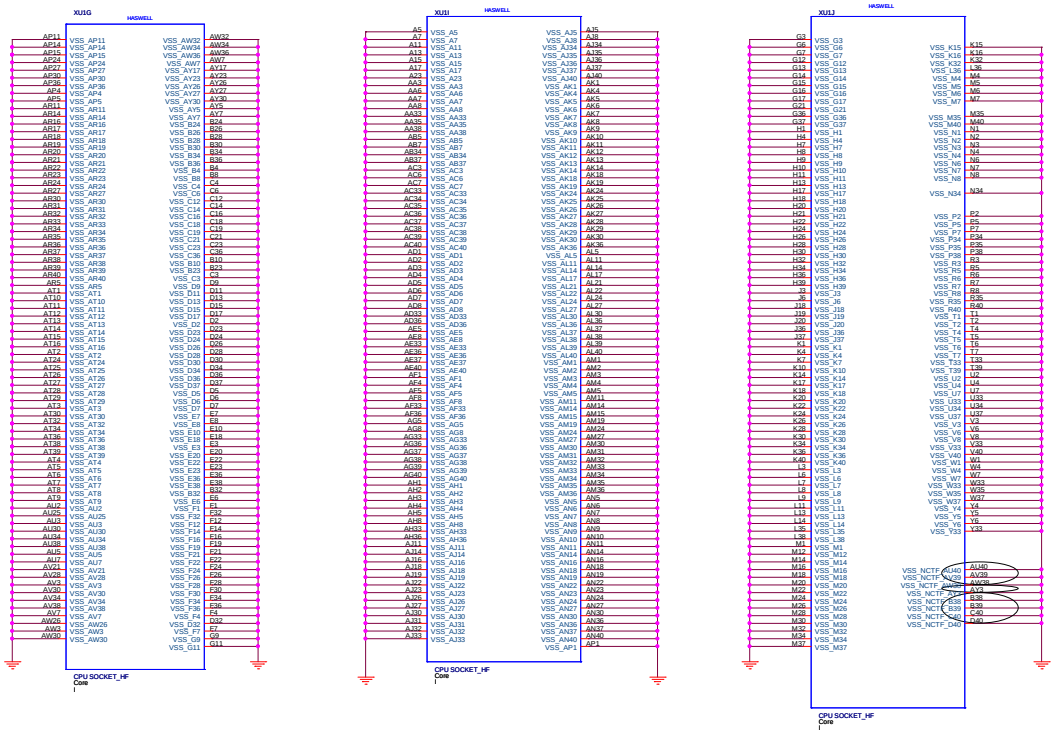
LITE-ON TECHNOLOGY CORP.			
Title	06. CPU-3: DDR3_CHA		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 6 of 62		



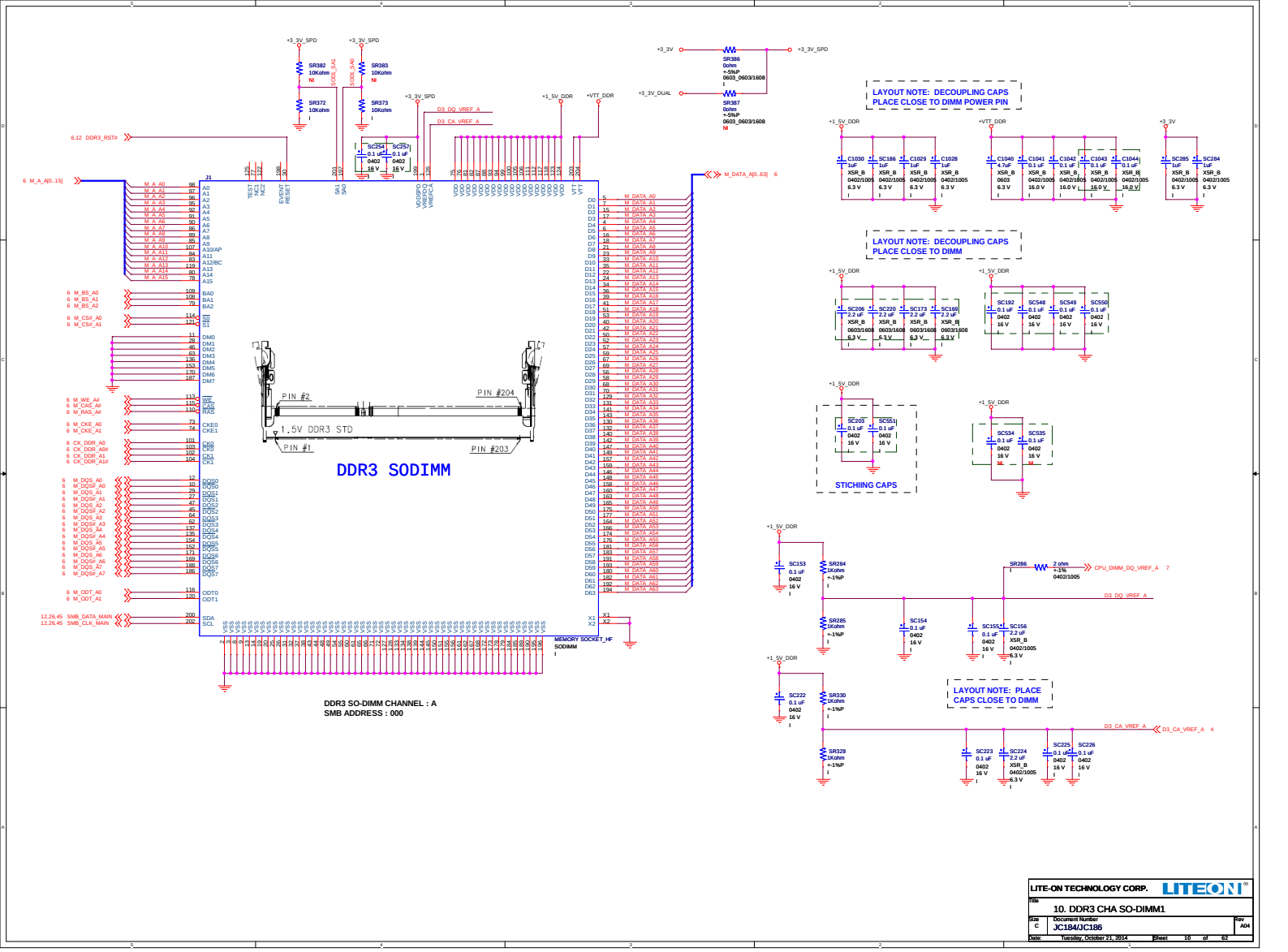
LITE-ON TECHNOLOGY CORP.			
Title	07. CPU-4: DDR3_CHB		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 7	of 62	



LITE-ON TECHNOLOGY CORP.			
Title	08. CPU-5: Power		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 8	of	62



LITE-ON TECHNOLOGY CORP.		LITEON
Title	09. CPU-6: GND	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 9 of 62	



LITE-ON TECHNOLOGY CORP.	LITEON
Title	10. DDR3 CHA SO-DIMM1
Size: C	Document Number: JC184/JC186
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LITE-ON TECHNOLOGY CORP.

Title: 11. Blank

Size: C | Document Number: JC184/JC186 | Rev: A04

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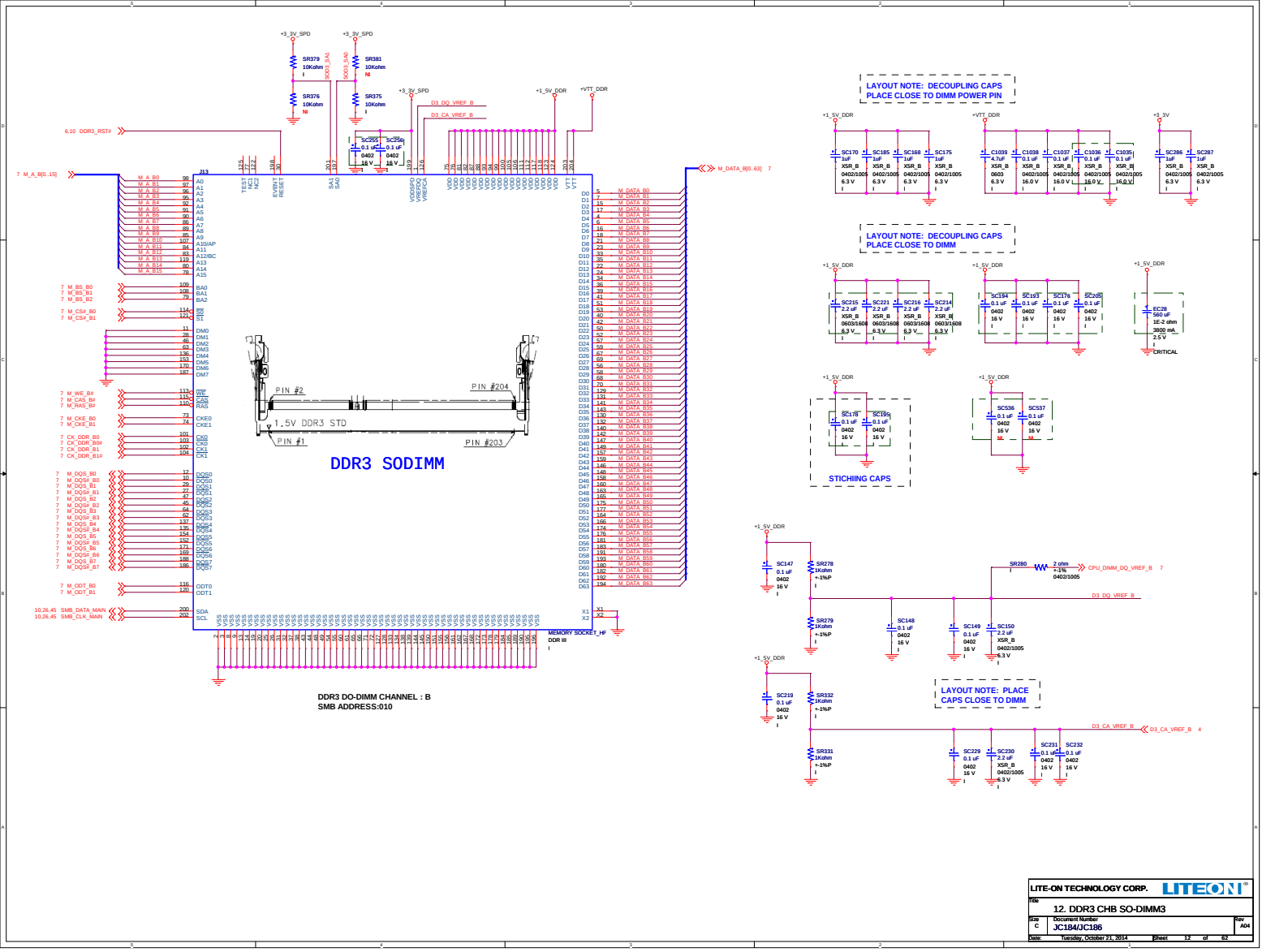

LITE-ON TECHNOLOGY CORP.	LITEON
Title	12_DDR3 CHB SO-DIMM3
Size: C	Document Number: JC184/JC186
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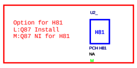
LITE-ON TECHNOLOGY CORP.

Title: 13. Blank

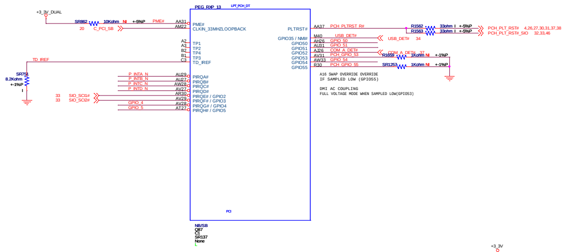
Size: C | Document Number: JC184/JC186 | Rev: A04

Date: Tuesday, October 21, 2014 | Sheet 13 of 62

Specital PCH PN for Lenovo Project



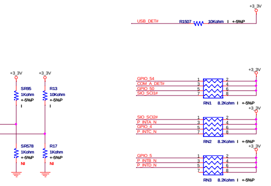
No PCI Device



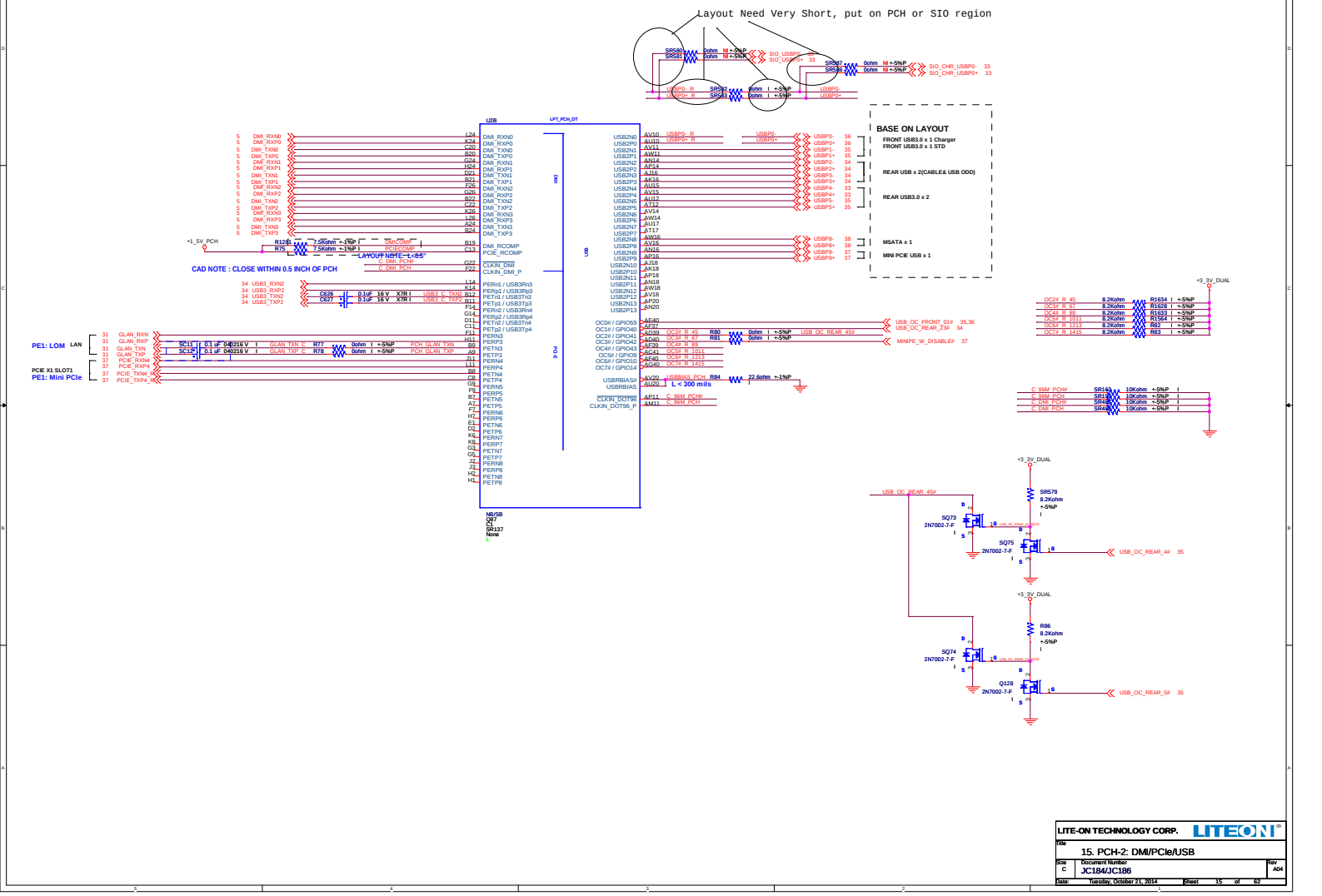
Boot BIOS Select

Boot Device	GPIO51	SATA1GP
LPC	0	0
RSVD	1	0
Reserved	0	1
SPI	1	1

16 SATA1GP



LITE-ON TECHNOLOGY CORP.		
Title: 14. PCH-1: PCI		
Size: D	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 14 of 62	



LITE-ON TECHNOLOGY CORP.	LITEON
Title	15. PCH-2: DMI/PCIe/USB
Size: C	Document Number: JC184/JC186
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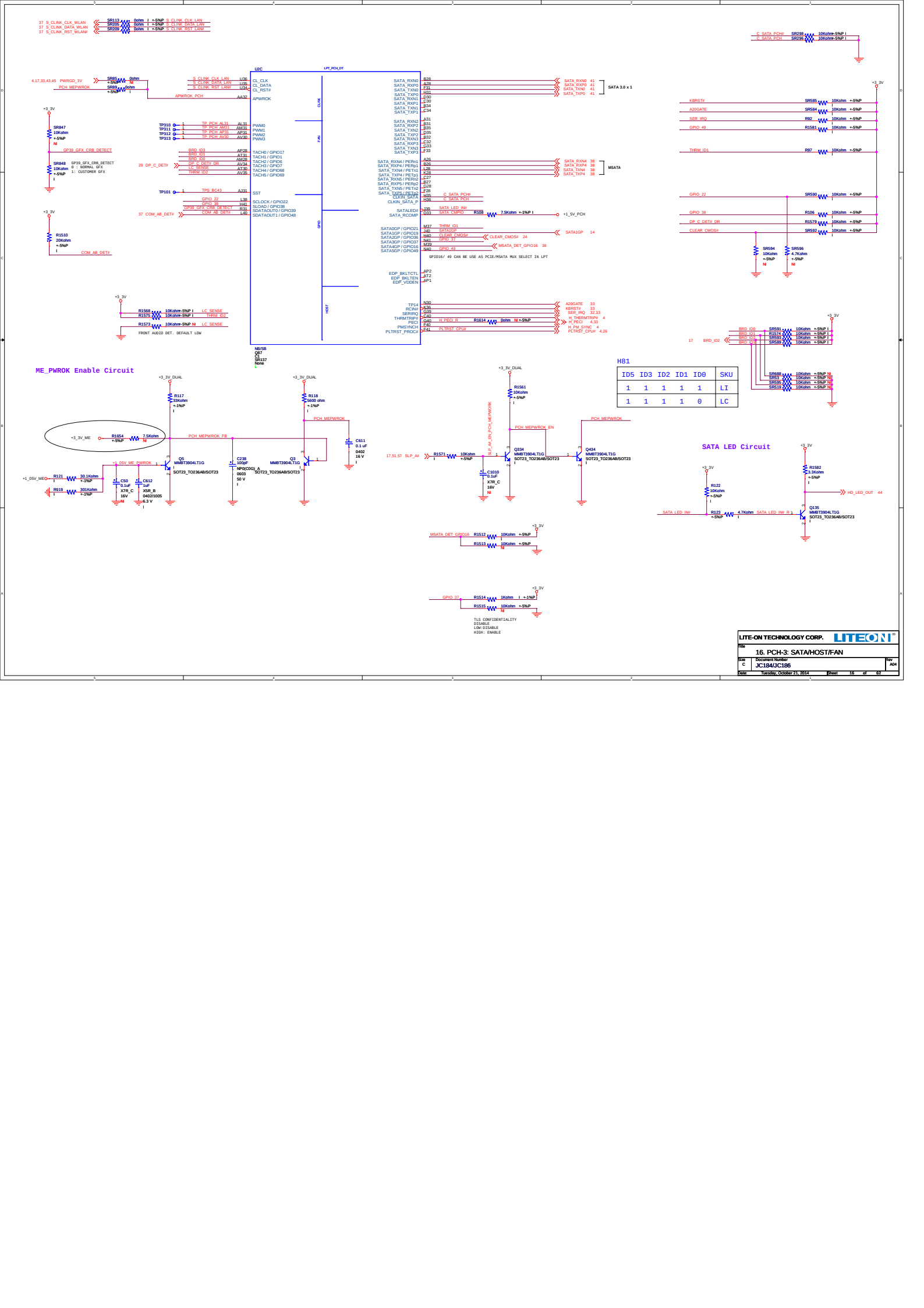
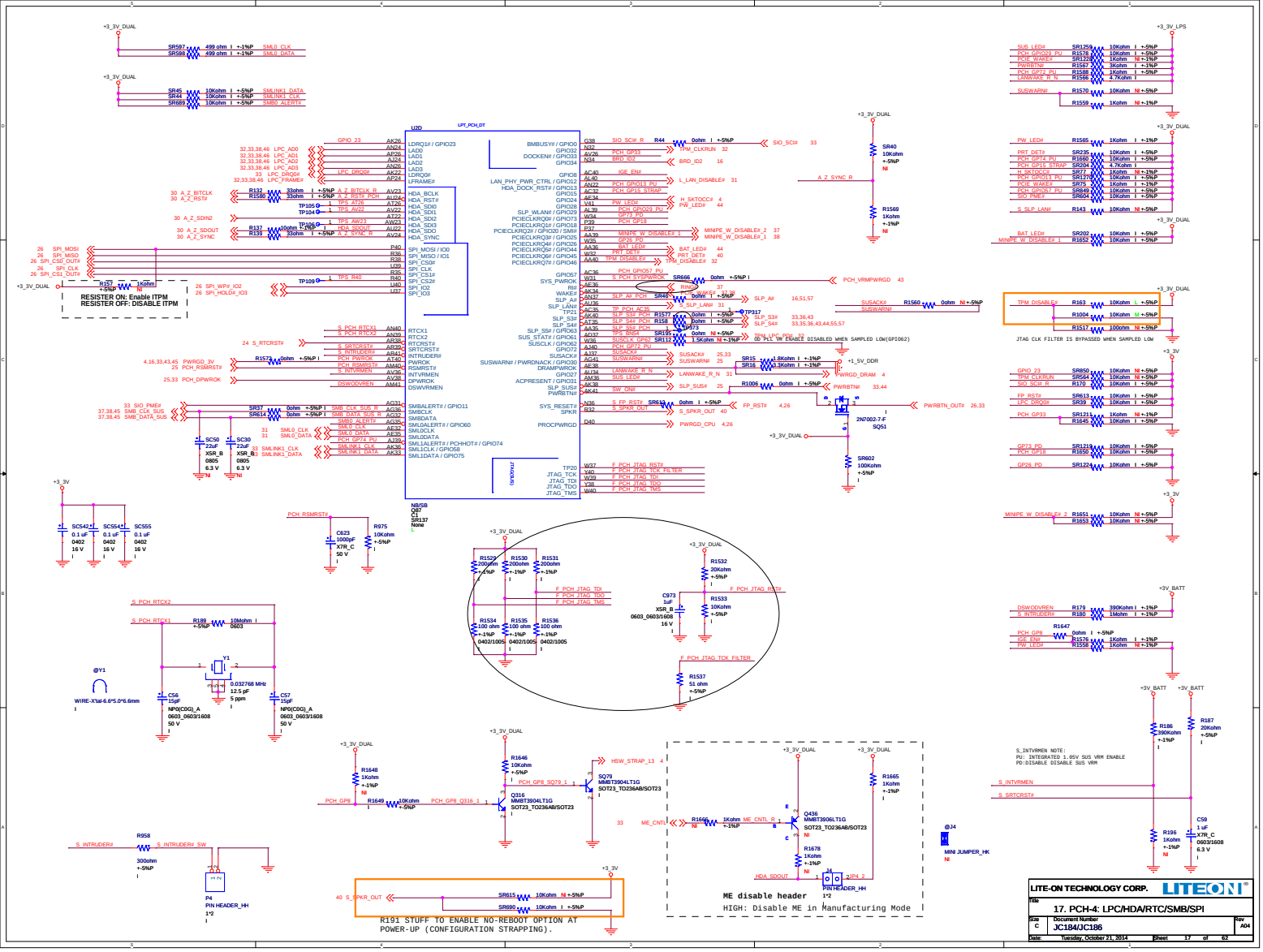
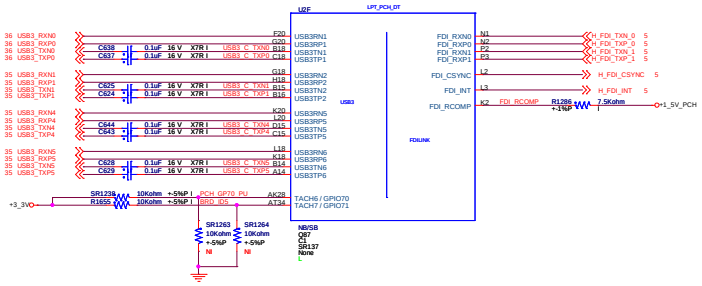
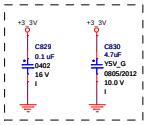
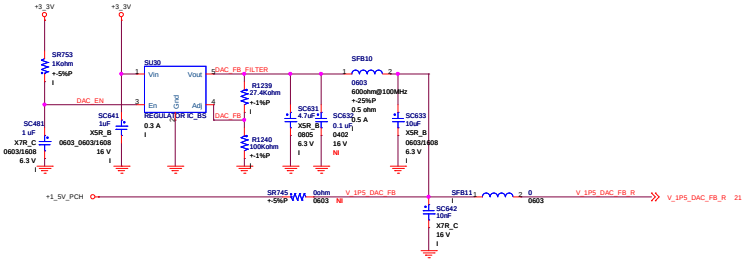
Date: Tuesday, October 21, 2014	Sheet 15 of 62


ME_PWROK Enable Circuit
SATA LED Circuit
H81
ID5 ID3 ID2 ID1 ID0 SKU
1 1 1 1 1 LI
1 1 1 1 0 LC
LITE-ON TECHNOLOGY CORP.
16. PCH-3: SATA/HOST/FAN
JC184/JC186
Tuesday, October 21, 2014


RESISTER ON: Enable ITPM
RESISTER OFF: DISABLE ITPM
R191 STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).
ME disable header
HIGH: Disable ME in Manufacturing Mode
JTAG CLK FILTER IS BYPASSED WHEN SAMPLED LOW
S_INTVRMEN NOTE:
PU: INTEGRATED 1.05V SUS VRM ENABLE
PD:DISABLE DISABLE SUS VRM
LITE-ON TECHNOLOGY CORP.
17. PCH-4: LPC/HDA/RTC/SMB/SPI
JC184/JC186
Tuesday, October 21, 2014







LITE-ON TECHNOLOGY CORP.		LITEON
Title	18. PCH-5/7: NVRAM/FDI	
Size C	Document Number JC184/JC186	Rev A04
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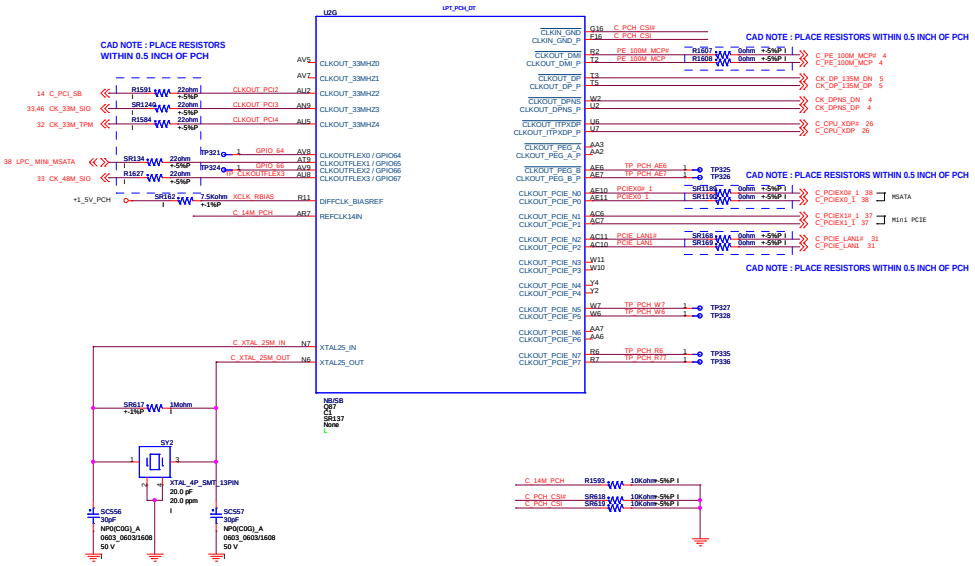
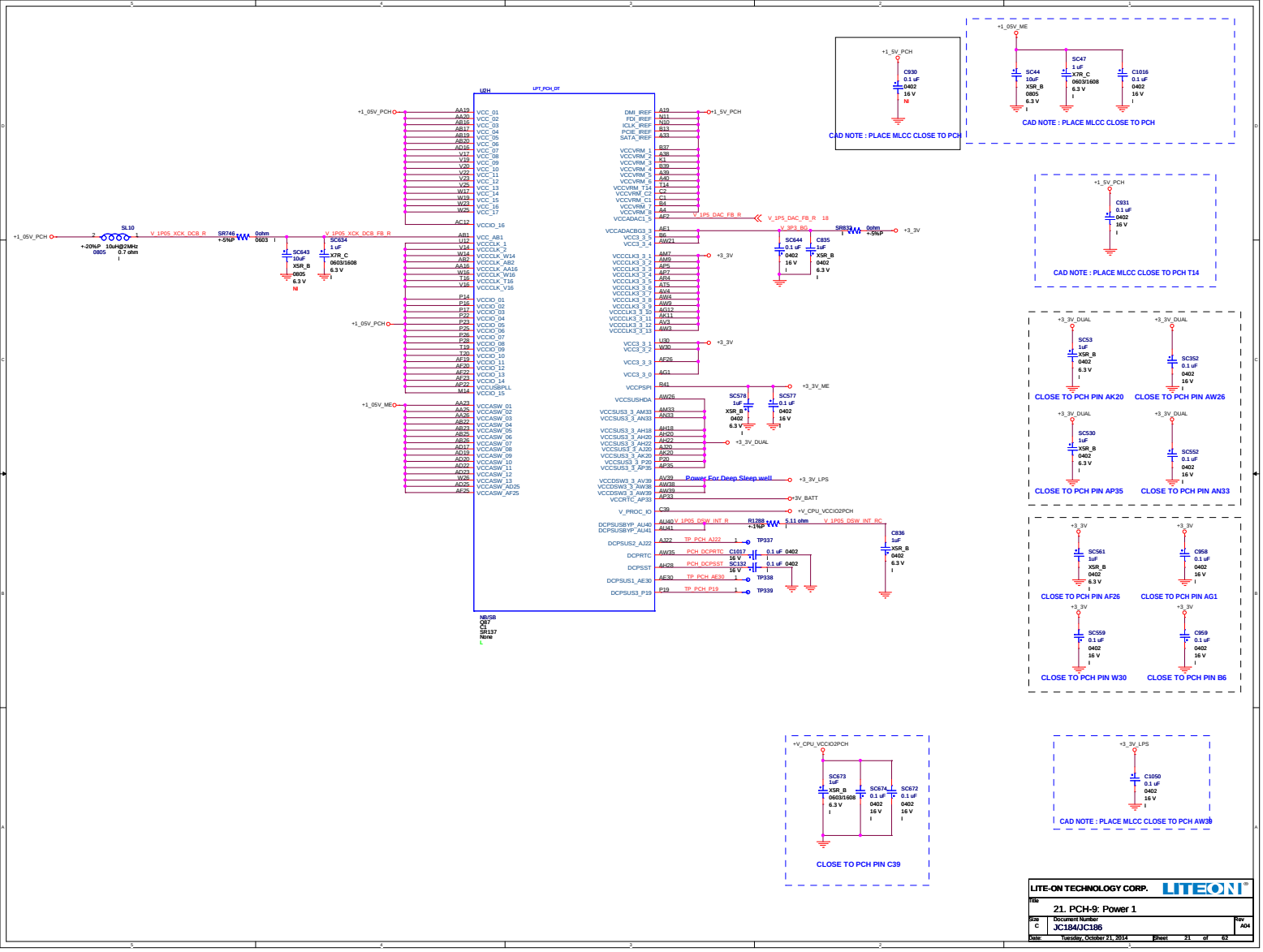
LITE-ON TECHNOLOGY CORP.			
Title	19. PCH-6: Display		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 19 of 62		



LITE-ON TECHNOLOGY CORP.			
Title	20. PCH-8: Clock		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 20 of 62		



LITE-ON TECHNOLOGY CORP.	LITEON
Title	21. PCH-9: Power 1
Size: C	Document Number: JC184/JC186
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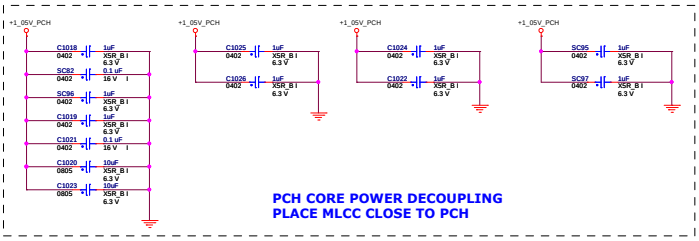
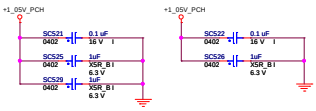
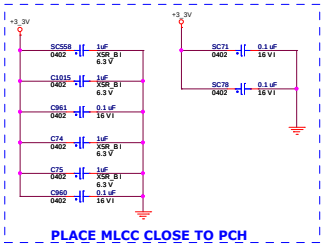
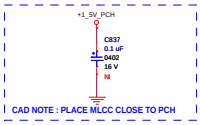
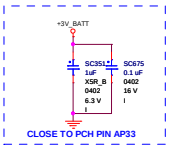
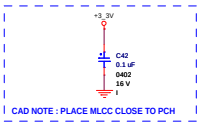




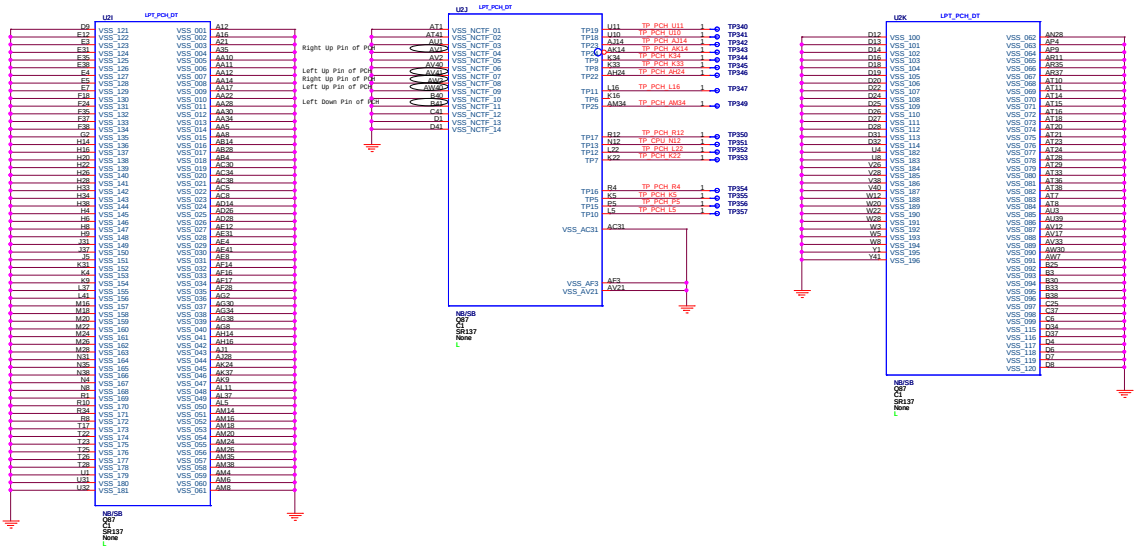








LITE-ON TECHNOLOGY CORP.		LITEON
Title: 22_PCH-10: Power 2		
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 22 of 62	



LITE-ON TECHNOLOGY CORP.	LITEON
Title	23. PCH-11: GND
Size: C	Document Number: JC184/JC186
Rev: A04	
Date: Tuesday, October 21, 2014	Sheet 23 of 62

CLEAR CMOS

16 CLEAR_CMOS#

E1_R_GND

E1
PIN HEADER_HH
1*3

R256
1Kohm
+-5%P

E2_R_GND

E2
PIN HEADER_HH
1*2
NI

R257
1Kohm
+-5%P
NI

S_RTCRST# 17

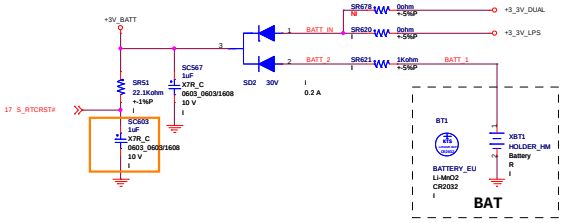
FOR SPI BOOT BLOCK JMP

@E1(1-2)
M
MINI JUMPER_HK

Jumper	Type
Dummy	Default
Pop	CLR_CMOS

@E2(2-3)
M
MINI JUMPER_HK
NI

BATTERY CIRCUIT



LITE-ON TECHNOLOGY CORP.			
Title: 24. CMOS Clear / Battery			
Size: C	Document Number: JC184/JC186		Rev: A04
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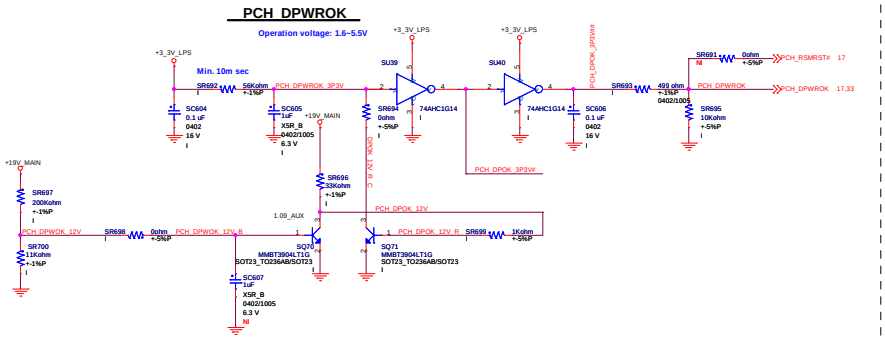
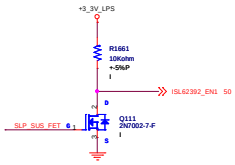
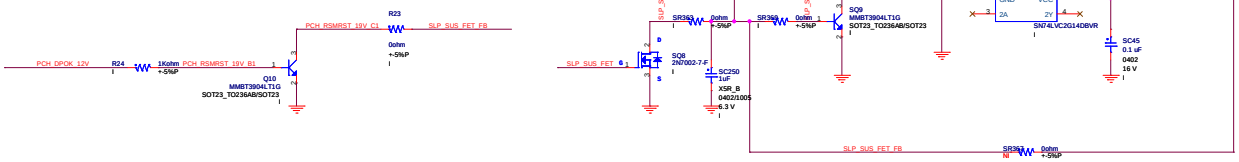
PCH_DPWROK

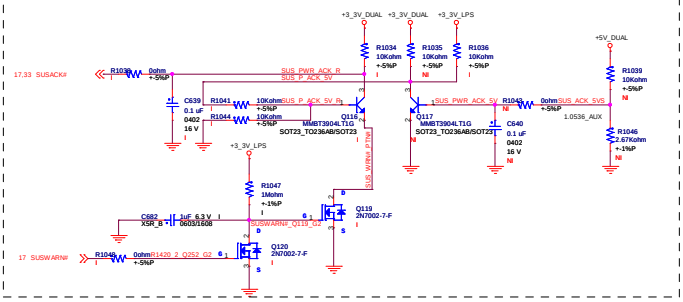
Operation voltage: 1.6~5.5V



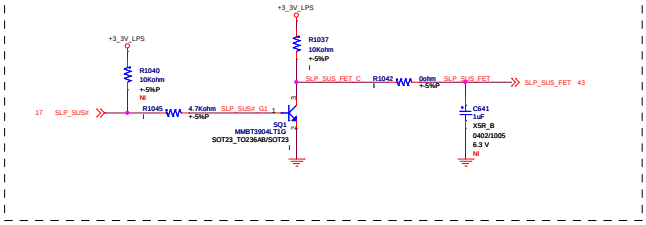




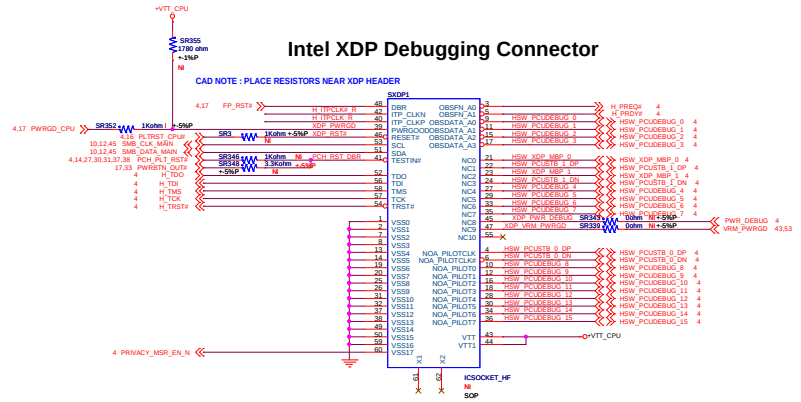
+5V_DUAL SUS ACK

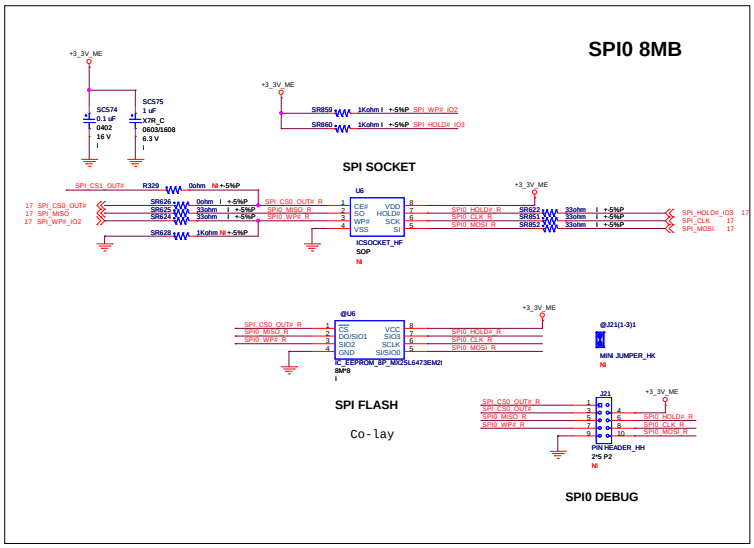


DSW CONTROL SIGNAL

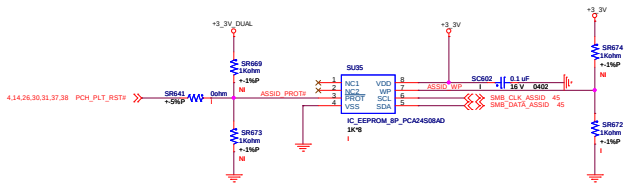


LITE-ON TECHNOLOGY CORP.		
Title	25. DSW	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 25 of 62	





LITE-ON TECHNOLOGY CORP.		
Title	26. SPI/XDP	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 26 of 62	



LITE-ON TECHNOLOGY CORP.			
Title	27. Asset ID - PCA24S08AD		
Size C	Document Number JC184/JC186		Rev A04
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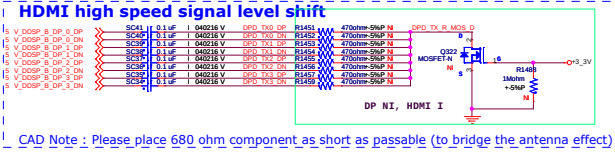
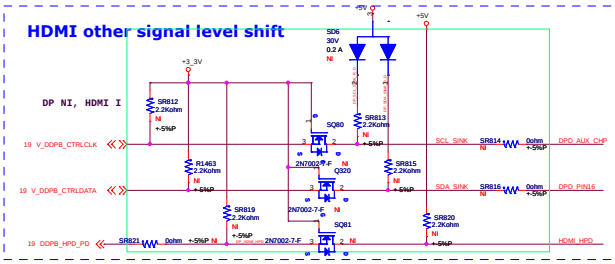
HDMI high speed signal level shift

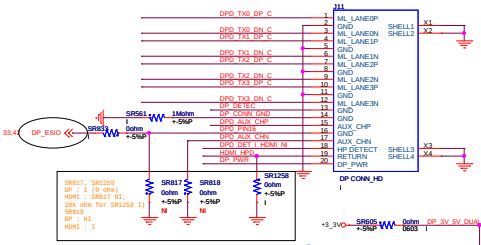


CAD Note : Please place 680 ohm component as short as passable (to bridge the antenna effect)

HDMI other signal level shift

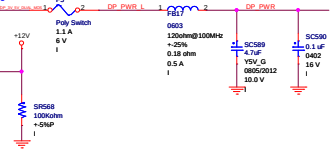


DP & HDMI co-lay Connector

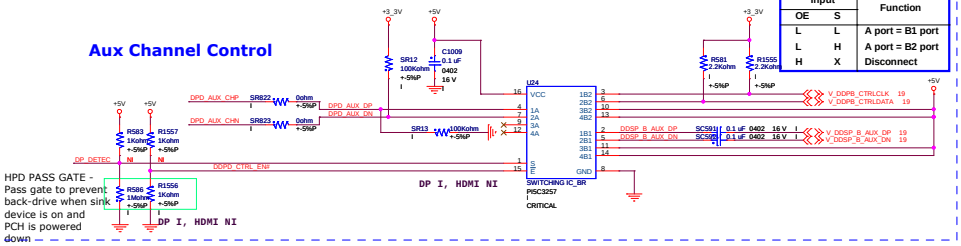


DP SR605 I, SR606 NI
HDMI SR606 I,SR605 NI

DisplayPort Interoperability

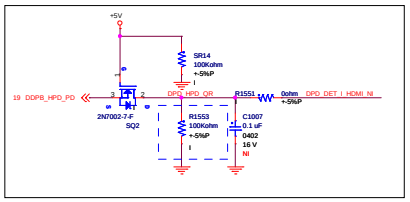


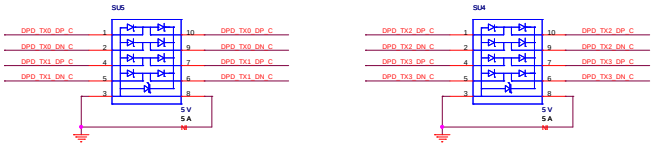
Aux Channel Control



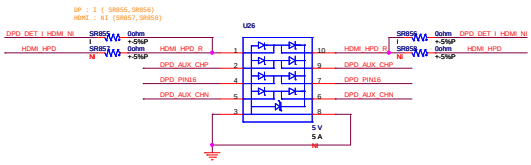
Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

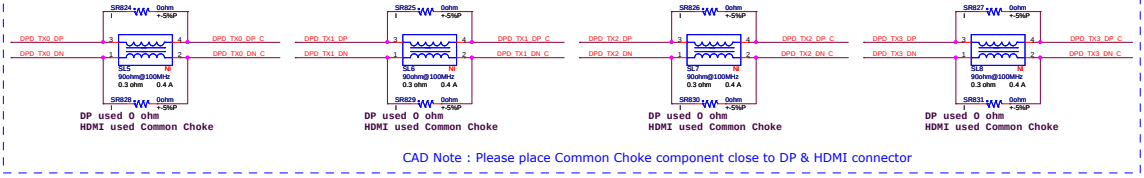
HPD PASS GATE - Pass gate to prevent back-drive when sink device is on and PCH is powered down





CAD Note : Please place ESD component close to DP connector

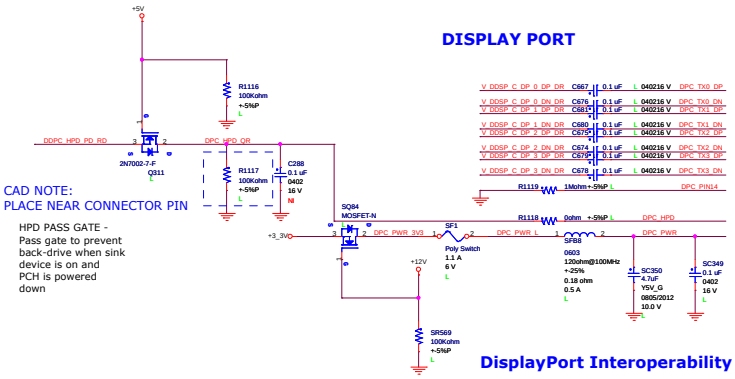




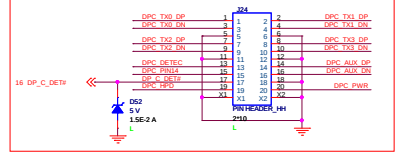
CAD Note : Please place Common Choke component close to DP & HDMI connector

LITE-ON TECHNOLOGY CORP.			
Title	28. Display Port B		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 28 of 62		

DISPLAY PORT



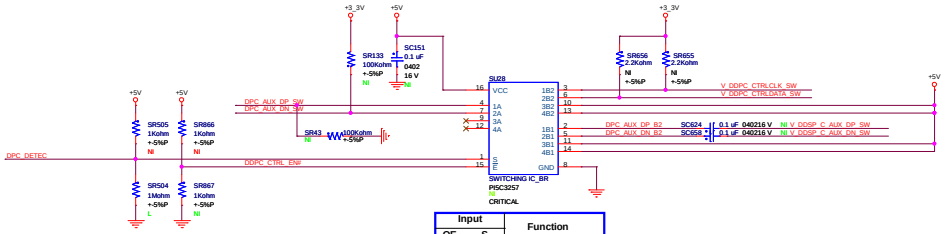
J24 Footprint is special ,for Tiny II only use, other project don't use.



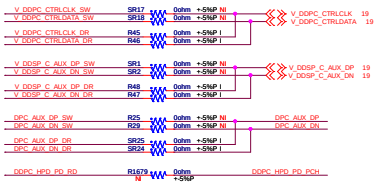
On Cable side Pin17 & Pin 18 need short

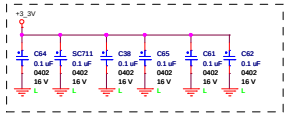
DPC_DETEC
L : Connect to Display Port or No Connection
H : Connect to Doungle

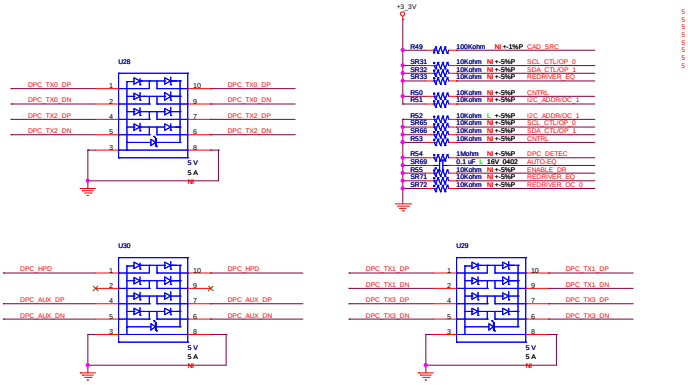
DisplayPort Interoperability

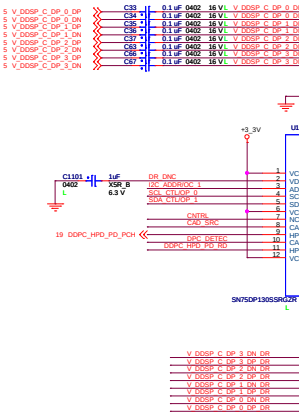


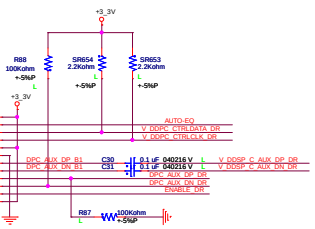
Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect





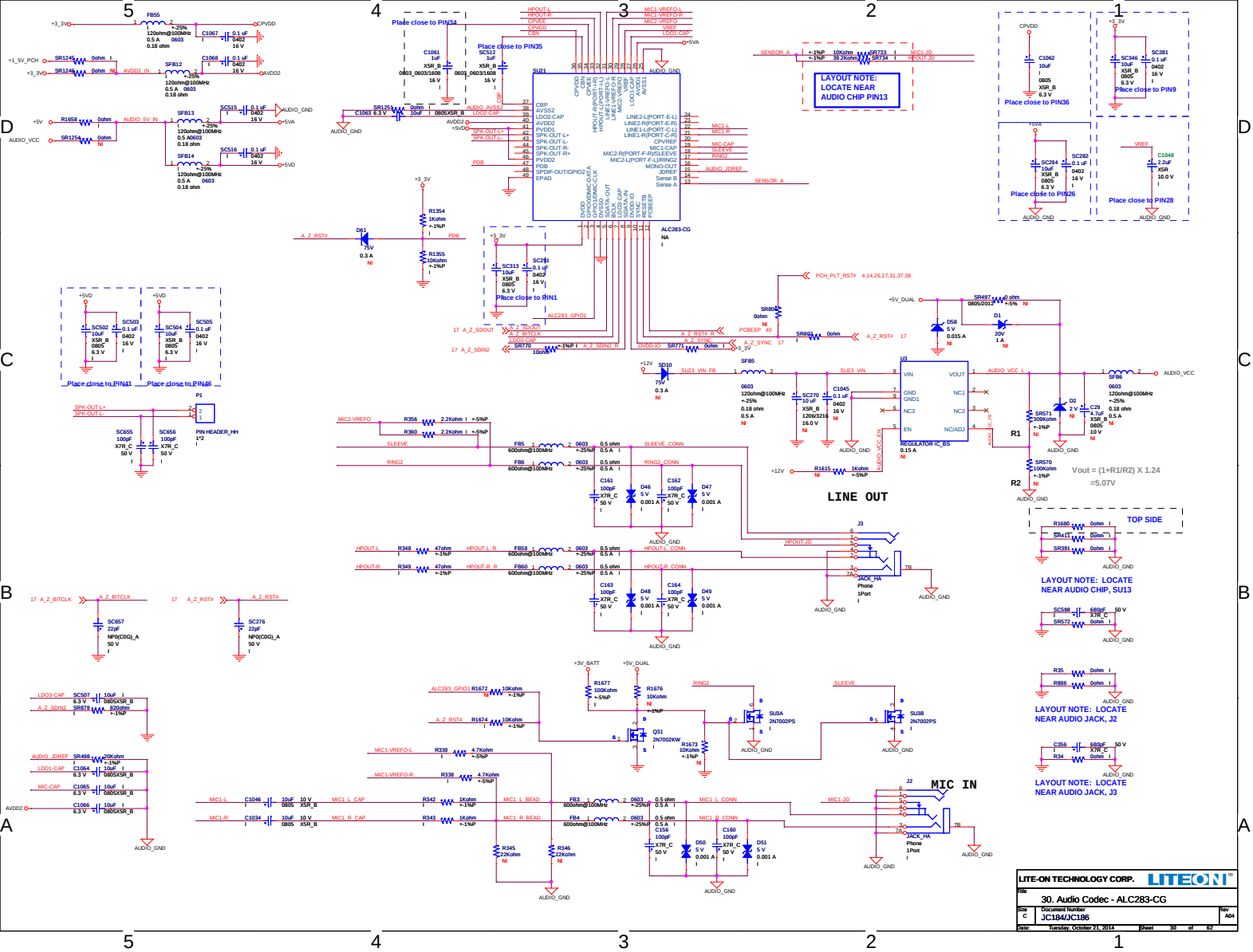






CAD Note : Please place ESD component close to DP connector

LITE-ON TECHNOLOGY CORP.			
Title	29. Display Port C / Redriver		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 29 of 62		


LAYOUT NOTE:
LOCATE NEAR
AUDIO CHIP PIN13
LINE OUT
MIC IN
TOP SIDE
LAYOUT NOTE: LOCATE
NEAR AUDIO CHIP, SU13
LAYOUT NOTE: LOCATE
NEAR AUDIO JACK, J2
LAYOUT NOTE: LOCATE
NEAR AUDIO JACK, J3
Vout = (1+R1/R2) X 1.24
=5.07V
Place close to PIN34
Place close to PIN35
Place close to PIN36
Place close to PIN9
Place close to PIN26
Place close to PIN28
Place close to PIN1
Place close to PIN41
Place close to PIN46
ALC283-CG
NA
REGULATOR IC_BS
PIN HEADER_HH
1*2
JACK_HA
Phone
1Port
LITE-ON TECHNOLOGY CORP.
30. Audio Codec - ALC283-CG
JC184/JC186
Tuesday, October 21, 2014
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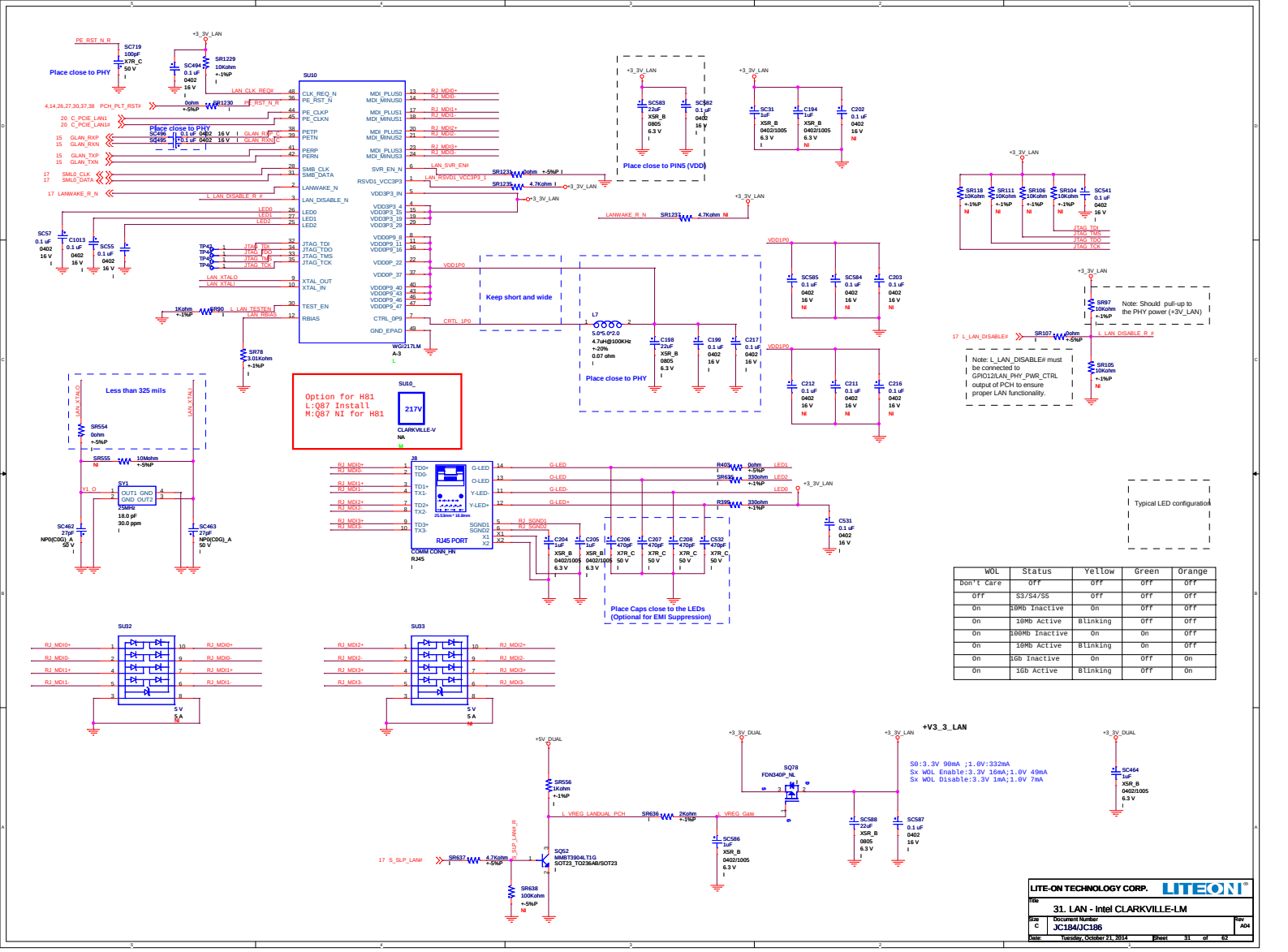

WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On

LITE-ON TECHNOLOGY CORP.

Title: 31. LAN - Intel CLARKVILLE-LM

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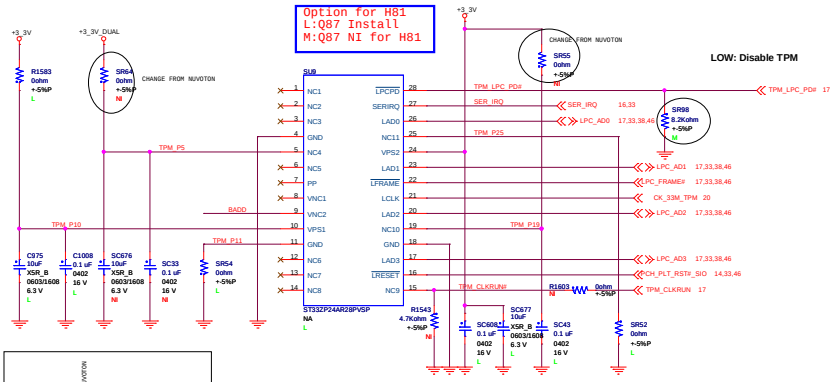
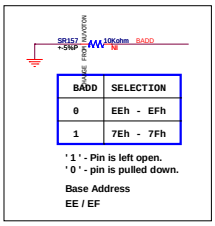
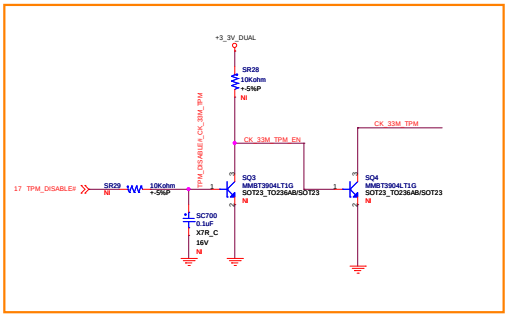
NUVOTON:
SR64,SC676,SC33,SR55-->I
R1583,C975,C1008,SR54-->NI

ST:
SR64,SC676,SC33,SR55-->NI
R1583,C975,C1008,SR54-->I

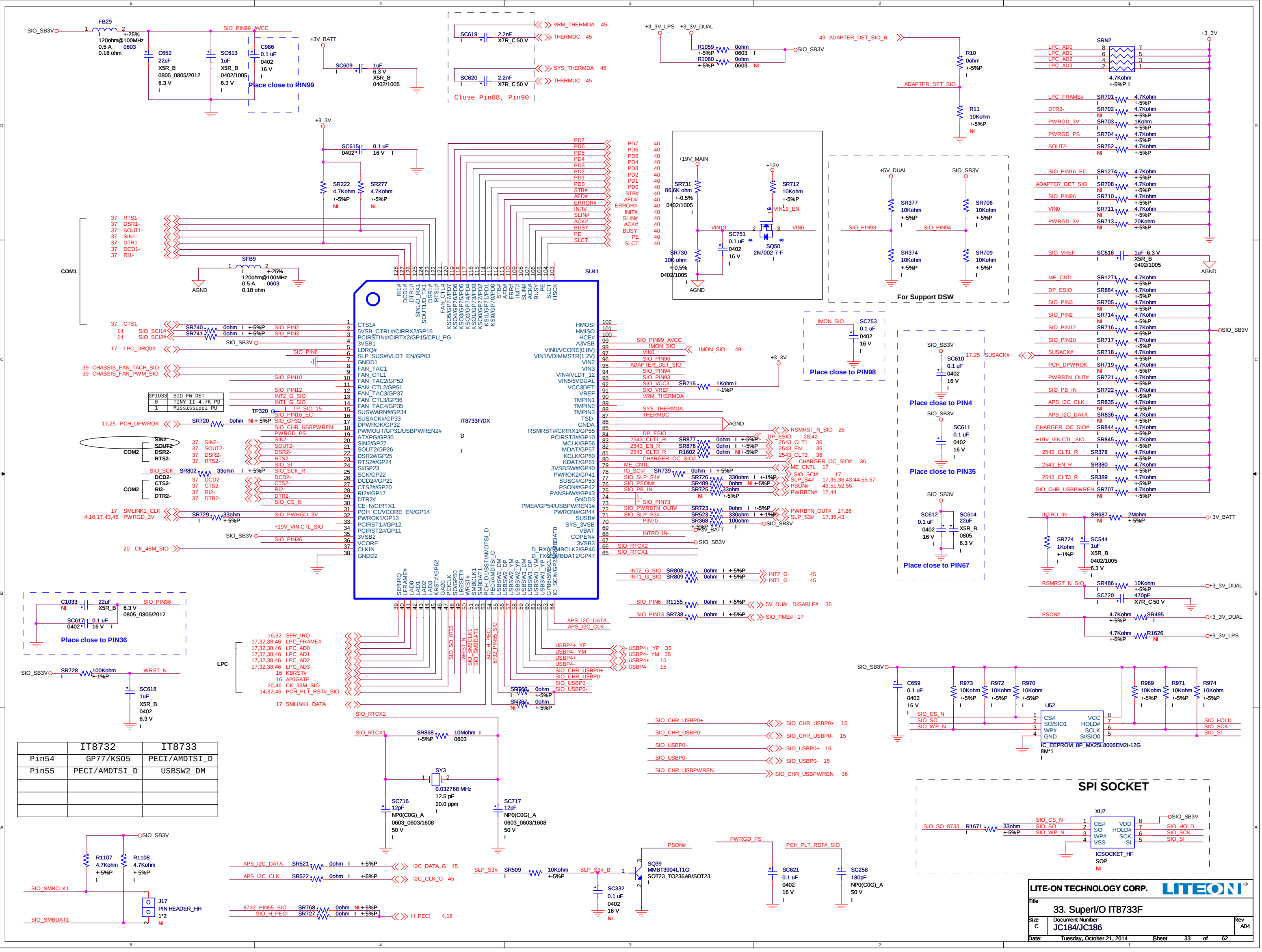
TPM







LITE-ON TECHNOLOGY CORP.			
Title: 32_TPM - ST ST33ZP24AR28PVSH			
Size: C	Document Number: JC184/JC186		Rev: A04
Date: Tuesday, October 21, 2014	Sheet 32 of 62		



	IT8732	IT8733
Pin54	GP77/KSO5	PECI/AMDTSI_D
Pin55	PECI/AMDTSI_D	USBSW2_DM

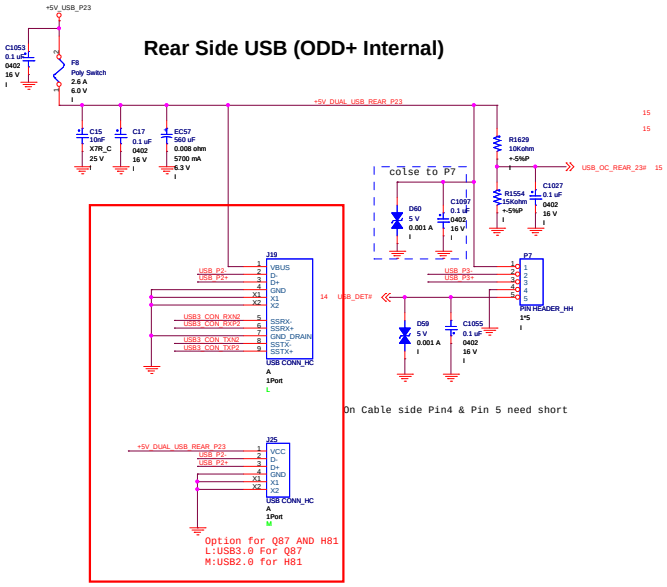
LITE-ON TECHNOLOGY CORP.

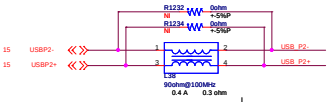
Title: 33. SuperI/O IT8733F

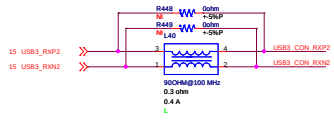
Size: C | Document Number: JC184/JC186 | Rev: A04

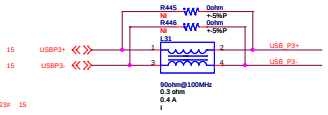
Date: Tuesday, October 21, 2014 | Sheet 33 of 62

Rear Side USB (ODD+ Internal)

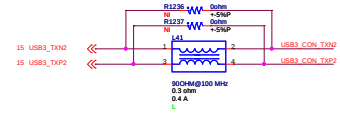


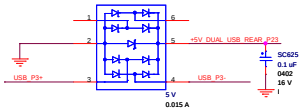


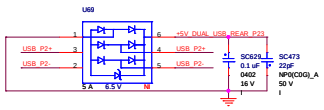


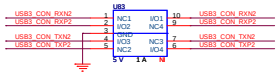


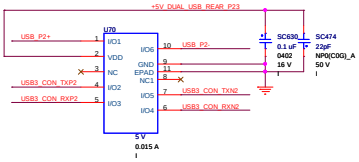
NOTE:
L:Q87 Install ,H81 NI



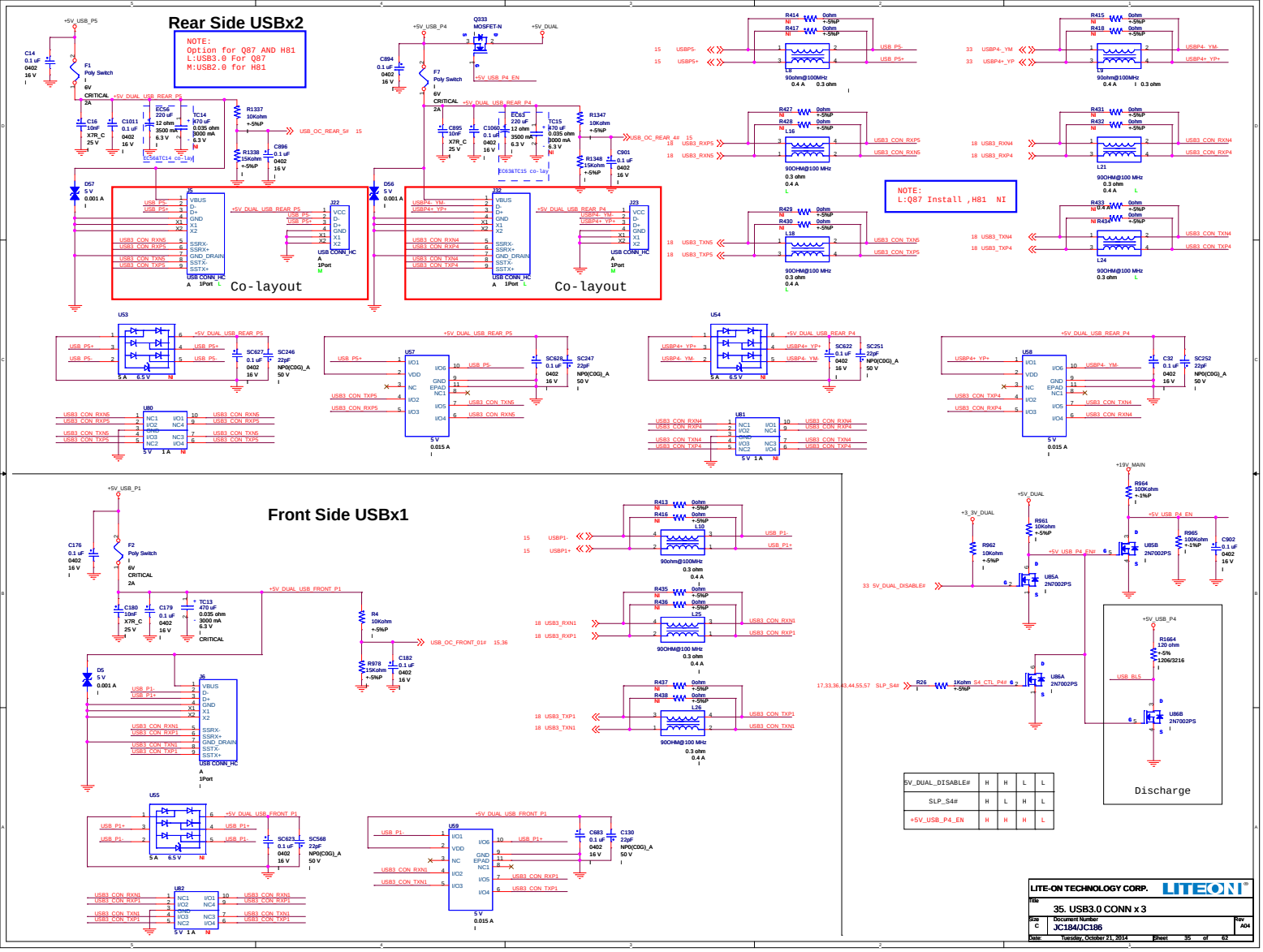








LITE-ON TECHNOLOGY CORP.		LITEON
Title	34. USB3.0 ODD CONN / Int USB	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 34 of 62	


Rear Side USBx2
NOTE:
Option for Q87 AND H81
L:USB3.0 For Q87
M:USB2.0 for H81
Co-layout
Co-layout
NOTE:
L:Q87 Install ,H81 NI
Front Side USBx1
Discharge
5V_DUAL_DISABLE#
SLP_S4#
+5V_USB_P4_EN
LITE-ON TECHNOLOGY CORP.
35. USB3.0 CONN x 3
Document Number
JC184/JC186
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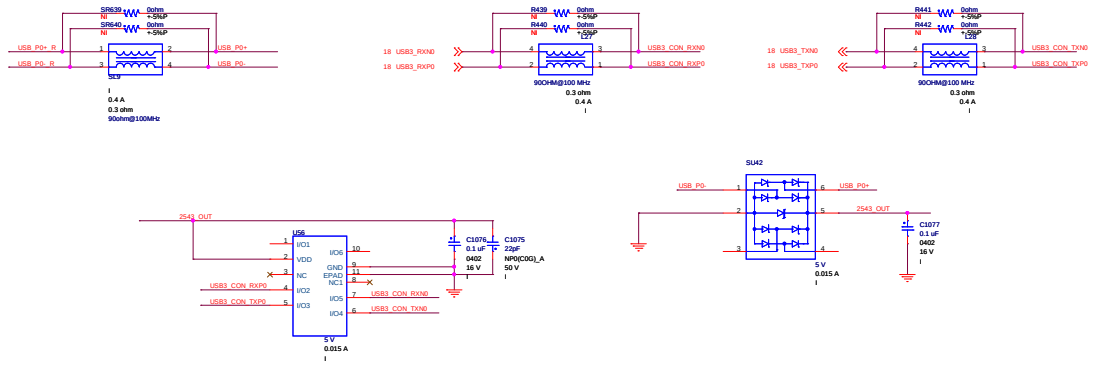
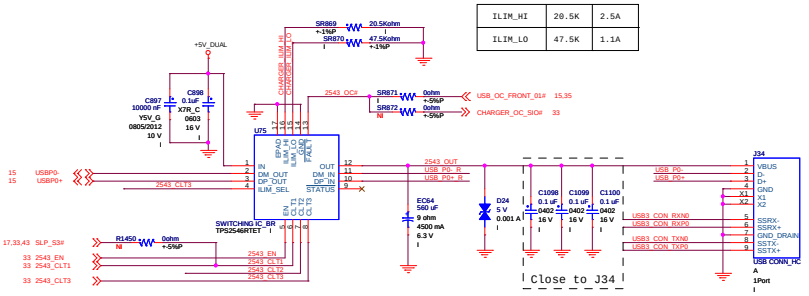
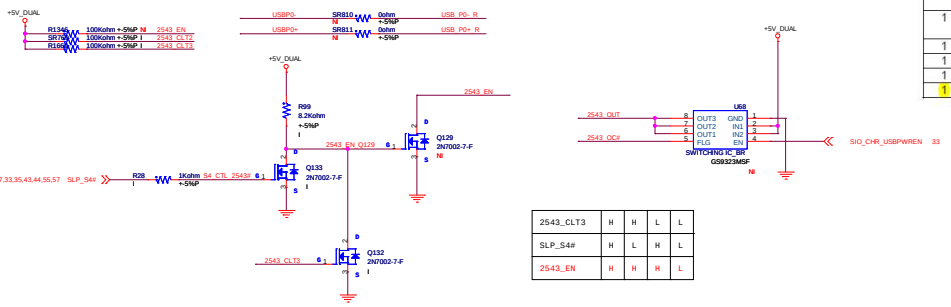
FRONT USB3.0 Charger x 1



ILIM_HI	20.5K	2.5A
ILIM_LO	47.5K	1.1A



CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
						off
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{OS_PW} & ILIM_HI (1)	DCP load present (2)
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present (3)
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP (4)	ILIM_LO	off
1	1	1	1	CDP (4)	ILIM_HI	CDP load present (5)



2543_CLT3	H	H	L	L
SLP_S4#	H	L	H	L
2543_EN	H	H	H	L

LITE-ON TECHNOLOGY CORP.			LITEON
Title	36. USB3.0 x1/ USB CHARGER		
Size C	Document Number JC184/JC186		Rev A04
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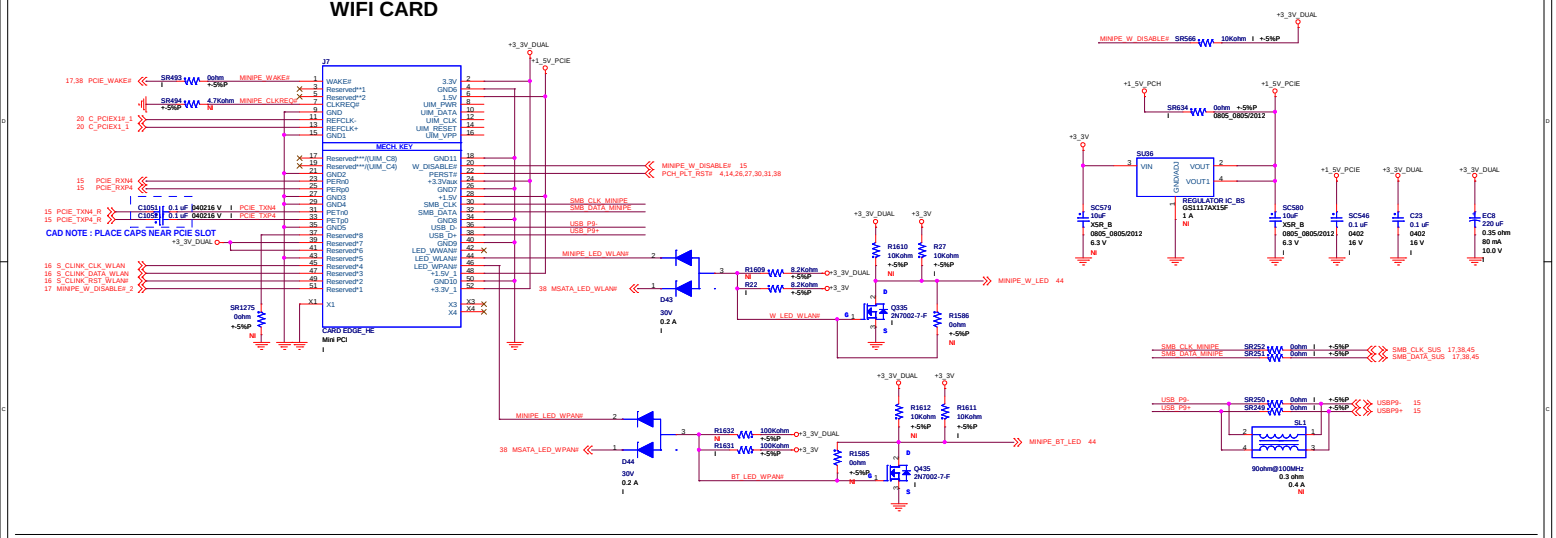
WIFI CARD

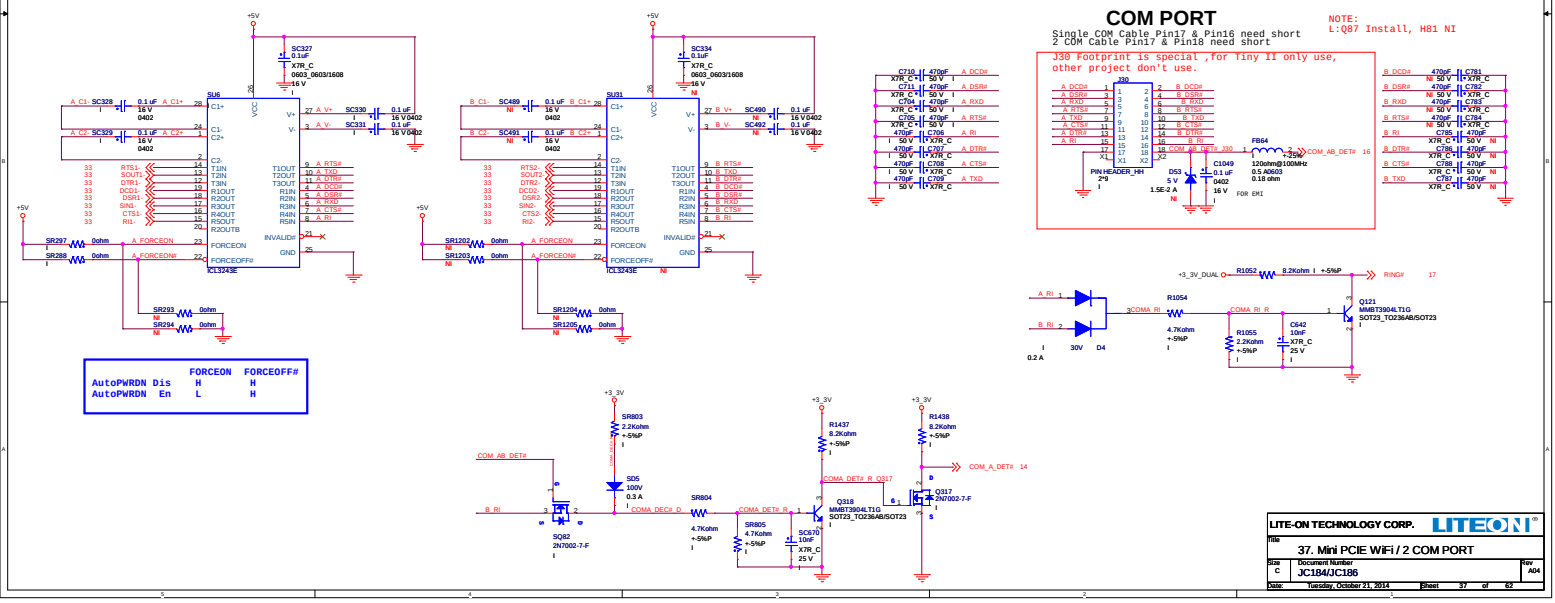


COM PORT

Single COM Cable Pin17 & Pin16 need short
2 COM Cable Pin17 & Pin18 need short

NOTE:
L:Q87 Install, H81 NI

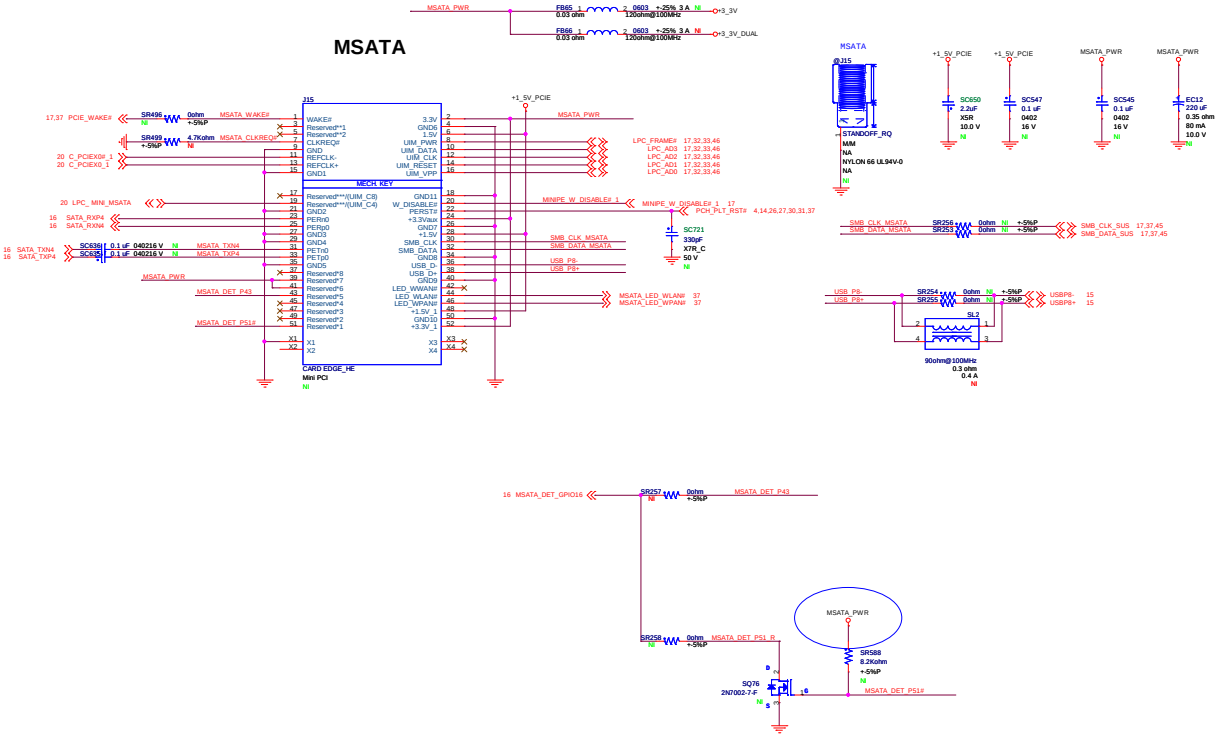
J30 Footprint is special ,for Tiny II only use, other project don't use.



	FORCEON	FORCEOFF#
AutoPWRDN Dis	H	H
AutoPWRDN En	L	H

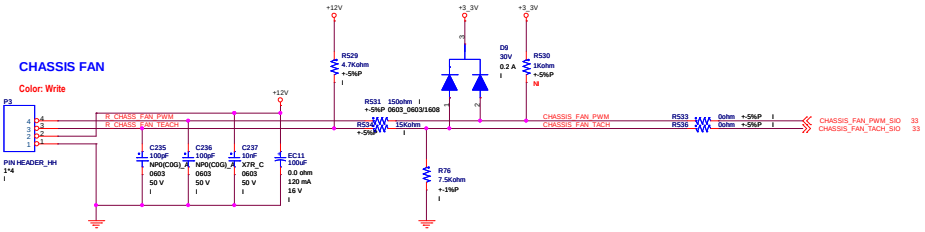
LITE-ON TECHNOLOGY CORP.	LITEON
Title	37. Mini PCIE WiFi / 2 COM PORT
Size C	Document Number JC184/JC186
Rev A04	
Date: Tuesday, October 21, 2014	Sheet 37 of 62

MSATA



LITE-ON TECHNOLOGY CORP.			
Title	38. MSATA		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 38 of 62		

CHASSIS/CPU/PSU FAN



LITE-ON TECHNOLOGY CORP.		
Title: 39. FAN CRTL		
Size: C	Document Number: JC184/JC186	Rev: A04
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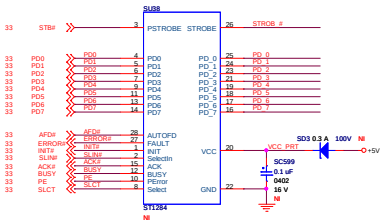
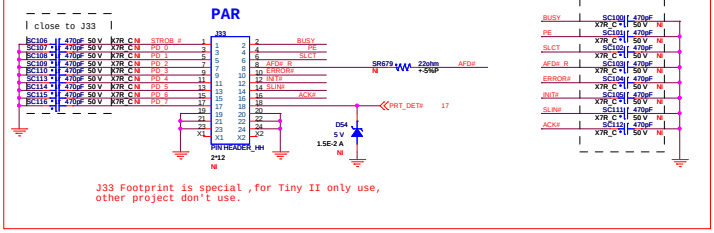
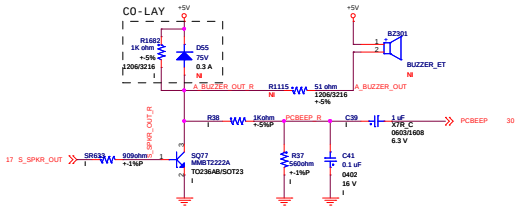


PARALLEL PORT

NOTE:
L:Q87 Install, H81 NI



J33 Footprint is special ,for Tiny II only use,
other project don't use.



LITE-ON TECHNOLOGY CORP.

Title	40. Buzzer/Parallel Port/BATT	
Size C	Document Number JC184/JC186	Rev A04
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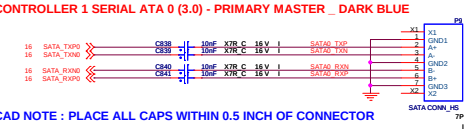
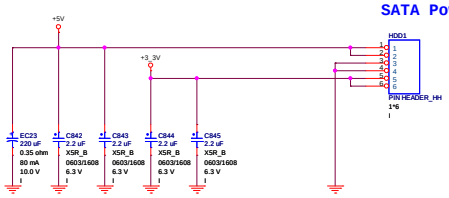
SATA SATA0

CONTROLLER 1 SERIAL ATA 0 (3.0) - PRIMARY MASTER _ DARK BLUE

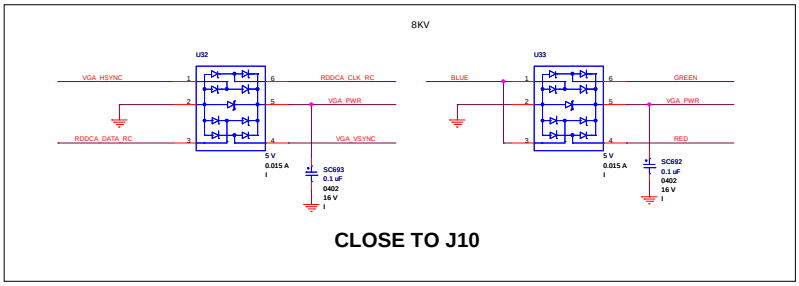


CAD NOTE : PLACE ALL CAPS WITHIN 0.5 INCH OF CONNECTOR

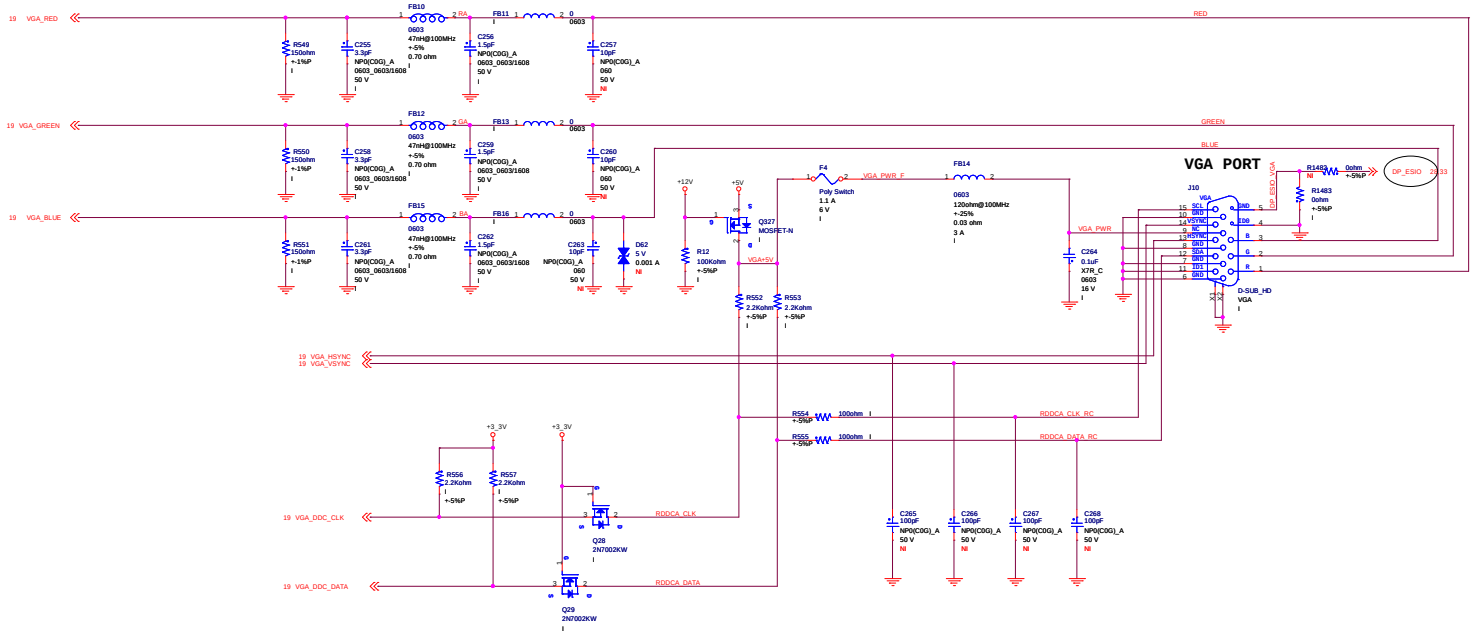
SATA Power



LITE-ON TECHNOLOGY CORP.		LITEON
Title: 41. SATA HDD		
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 41 of 62	

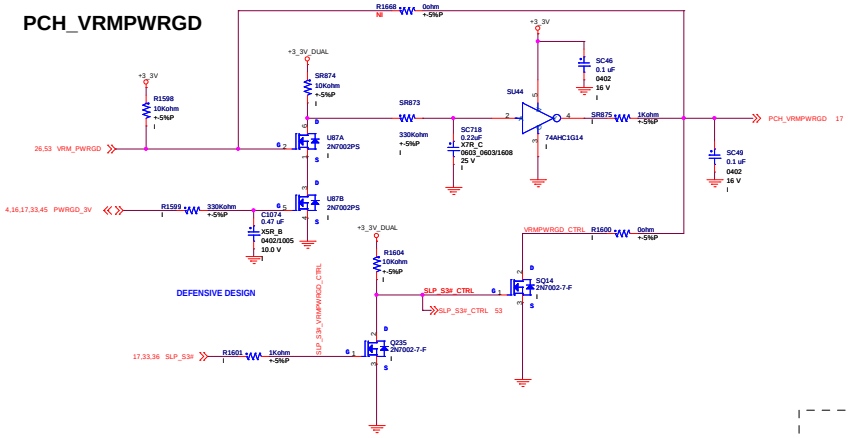


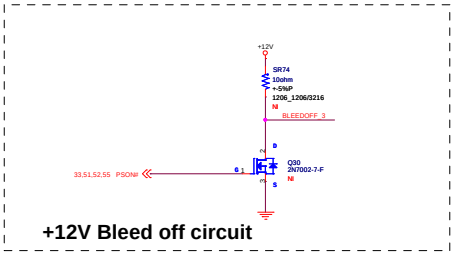
CLOSE TO J10



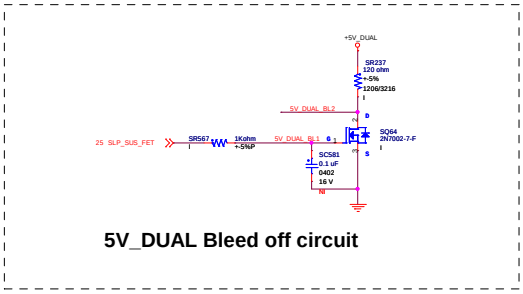
LITE-ON TECHNOLOGY CORP.		
Title	42. VGA	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 42 of 62	

PCH_VRMPWRGD

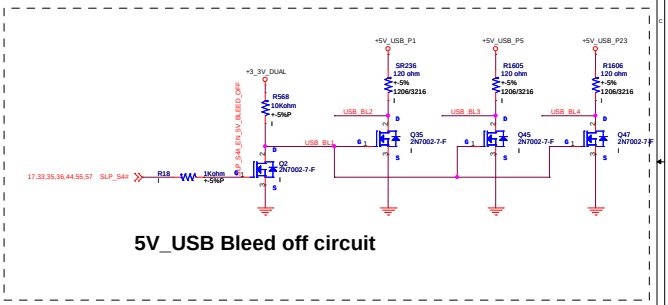




+12V Bleed off circuit

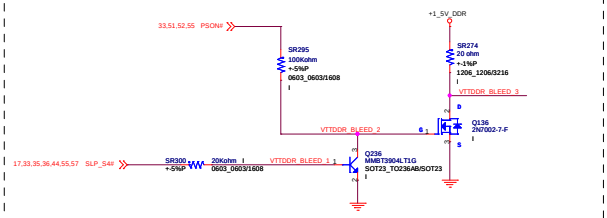


5V_DUAL Bleed off circuit

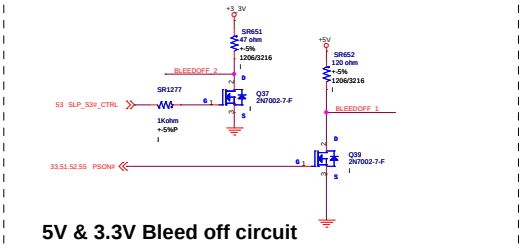


5V_USB Bleed off circuit

DESIGN NOTE:THESE CIRCUITS ARE USED TO BLEED OFF 1.5V DDR



+1_5V_DDR Bleed off circuit

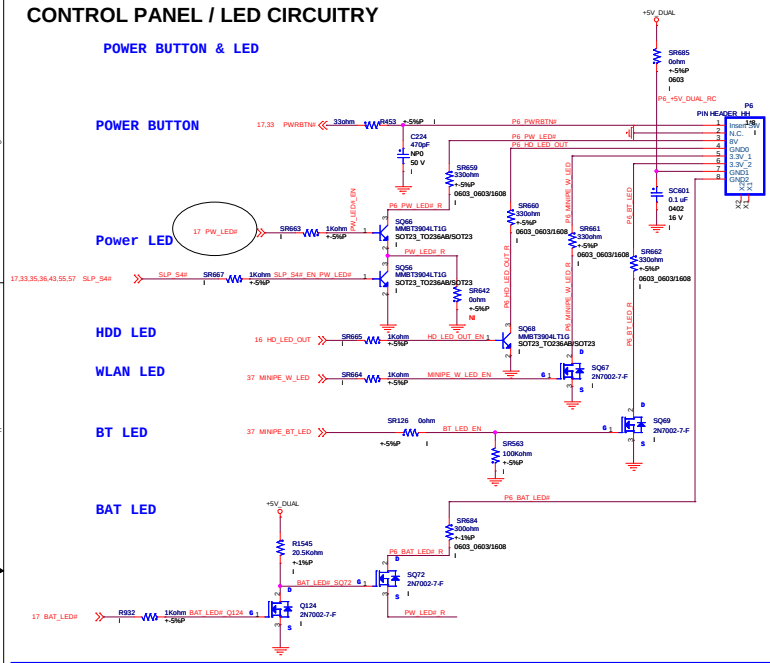


5V & 3.3V Bleed off circuit

LITE-ON TECHNOLOGY CORP.		
Title: 43_PWRGD & BLEED OFF		
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 43 of 62	

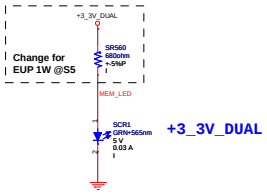
CONTROL PANEL / LED CIRCUITRY

POWER BUTTON & LED



P6 HEADER	Color	Functoin
3 PIN	G	PWR
4 PIN	G	HDD
5 PIN	G	WIFI
6 PIN	G	BT

Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 100ohm = 22mA
0.1W (For Current limit R)

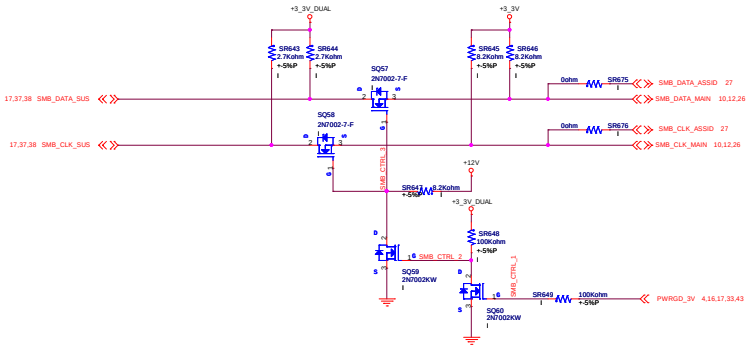


PCA LED CIRCUITS

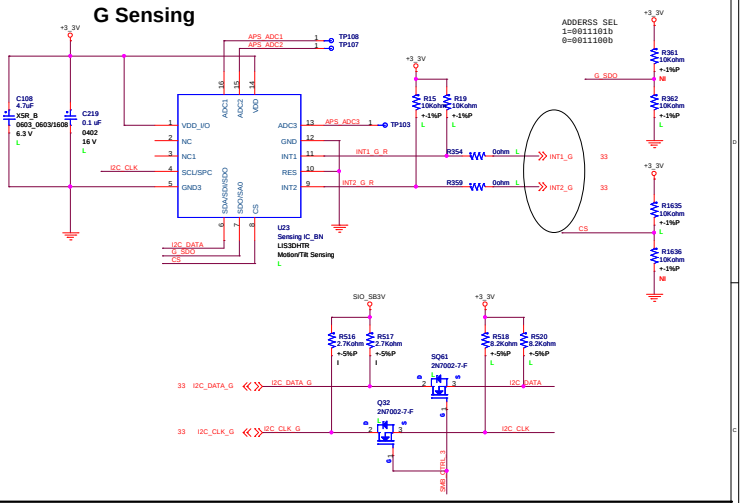
ALL PARTS ON THIS SHEET ARE NI FOR PRODUCTION.

LITE-ON TECHNOLOGY CORP.			
Title	44. Button/LED		
Size C	Document Number JC184/JC186		Rev A04
Date: Tuesday, October 21, 2014	Sheet 44 of 62		

SM Bus

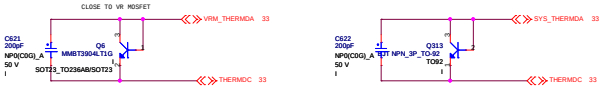


G Sensing



Temperature Sensing

Current Mode

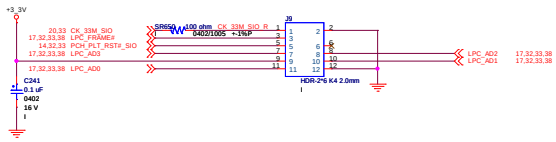


CAD NOTE : Place MLCC Close to Thermal Diode

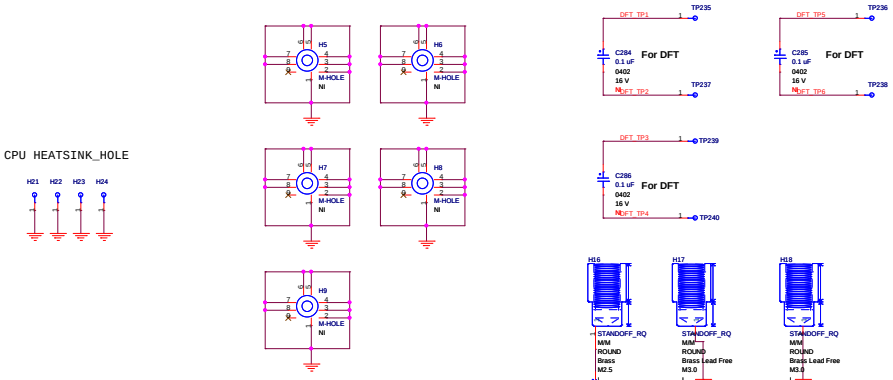
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

LITE-ON TECHNOLOGY CORP.		
Title	45. SM BUS/Thermal Sensing/APS	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 45 of 62	

Debug port

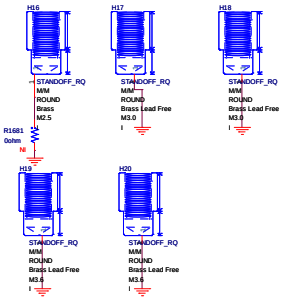


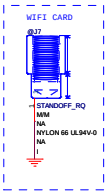
LITE-ON TECHNOLOGY CORP.		
Title: 46. Debug Port		
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 46 of 62	

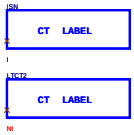


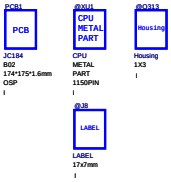
CPU HEATSINK_HOLE

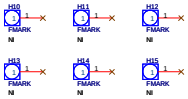
FAN DUCT



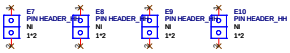




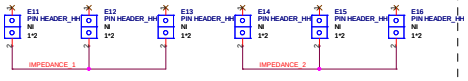




For Impedance Test



E7 differential 5/7 (85ohm) for USB2.0,USB3.0 for Layer1
E8 differential 4/5 (85ohm) for DMI , FDI ,SATA,USB for Layer4
E9 differential 6.5/4 (68ohm) for MEMORY for Layer4
E10 differential 4/10 (100ohm) for LAN for Layer6



E11 single 4 for Layer 1
E12 single 4 for Layer 4
E13 single 9.5 (34ohm) for Layer 4
E14 single 6.5 (42ohm) for Layer 4

LITE-ON TECHNOLOGY CORP.

Title: 47. Mounting Hole

Size	Document Number	Rev
C	JC184/JC186	A04

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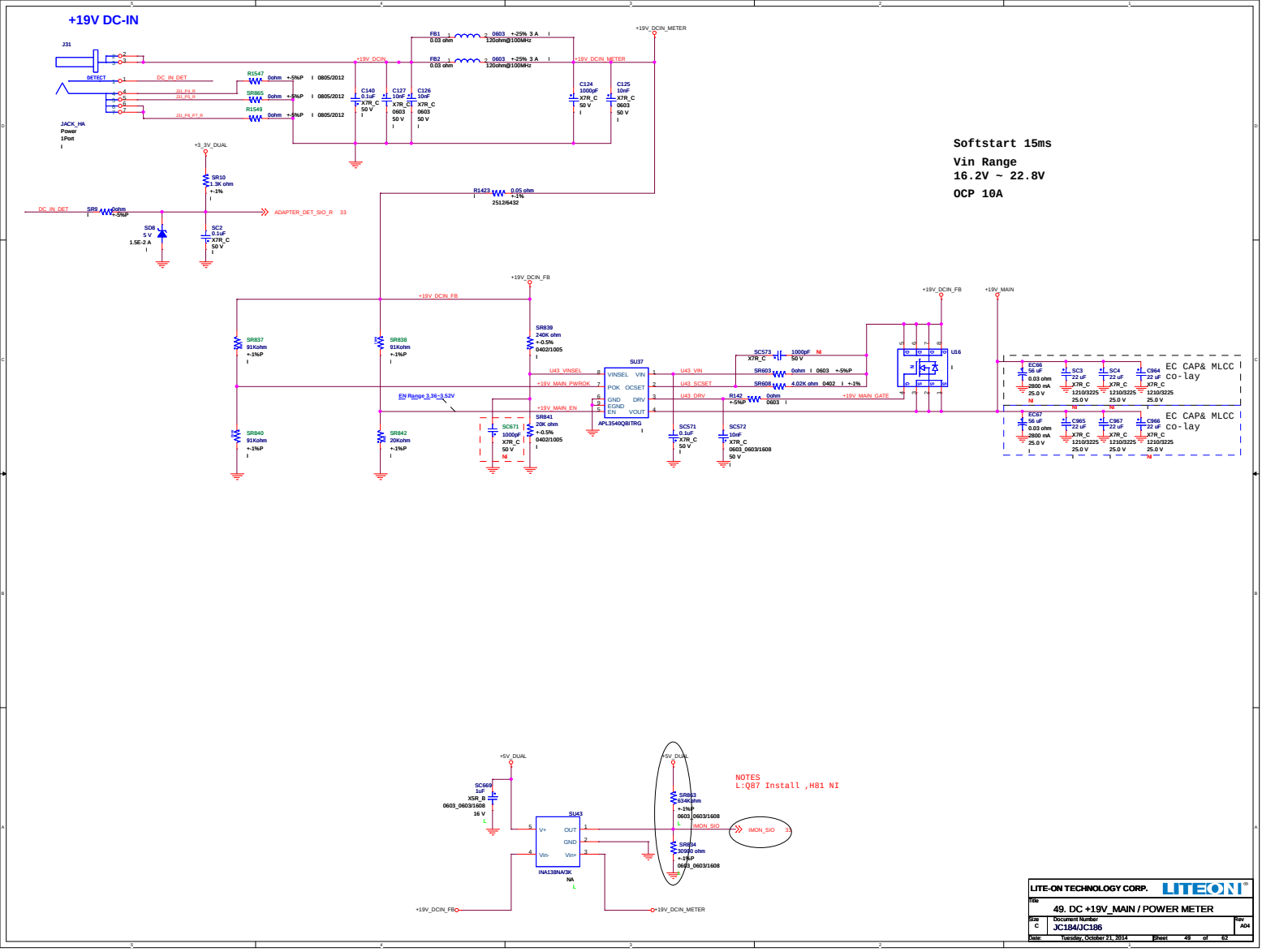
LITE-ON TECHNOLOGY CORP.

Title: 48. Blank

Size: C | Document Number: JC184/JC186 | Rev: A04

Date: Tuesday, October 21, 2014 | Sheet 48 of 62



LITE-ON TECHNOLOGY CORP.

Title	49. DC +19V_MAIN / POWER METER	
Size C	Document Number JC184/JC186	Rev A04
Date: Tuesday, October 21, 2014	Sheet 49 of 62	

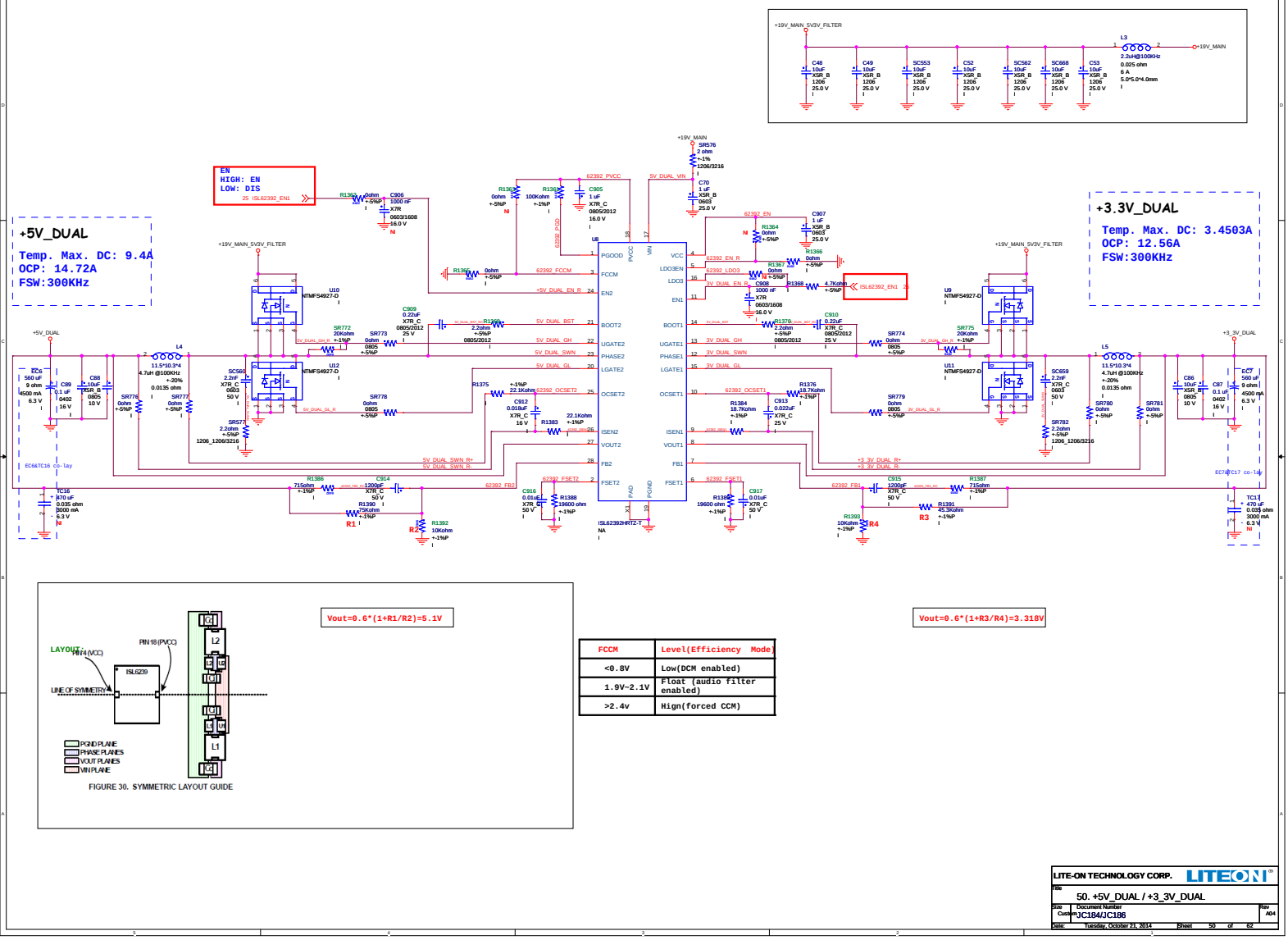


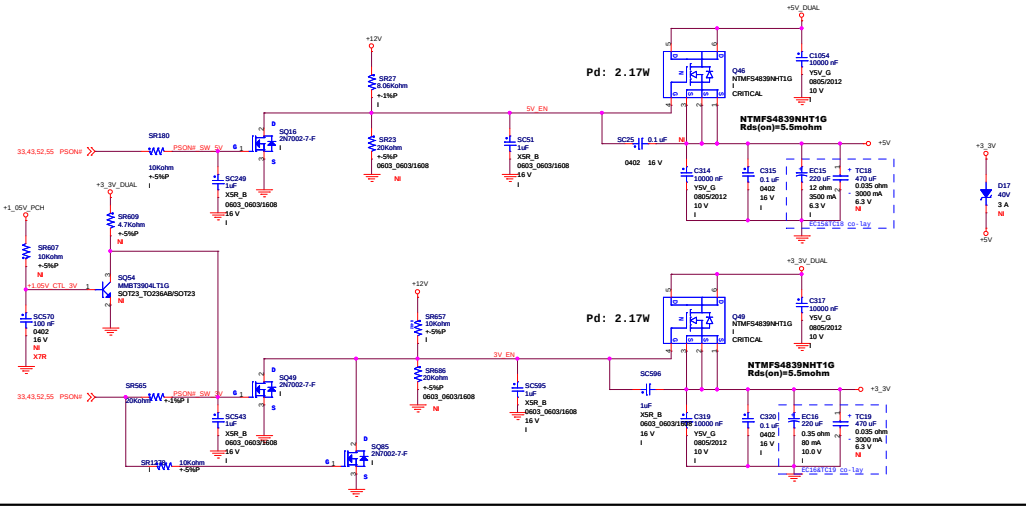
FIGURE 30. SYMMETRIC LAYOUT GUIDE

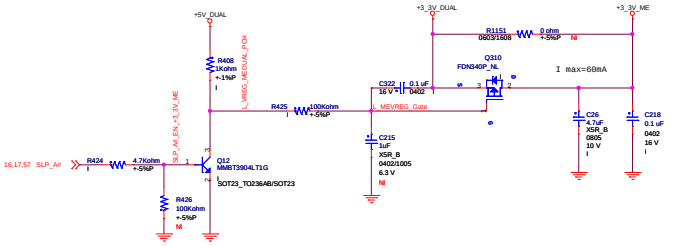
Vout=0.6*(1+R1/R2)=5.1V

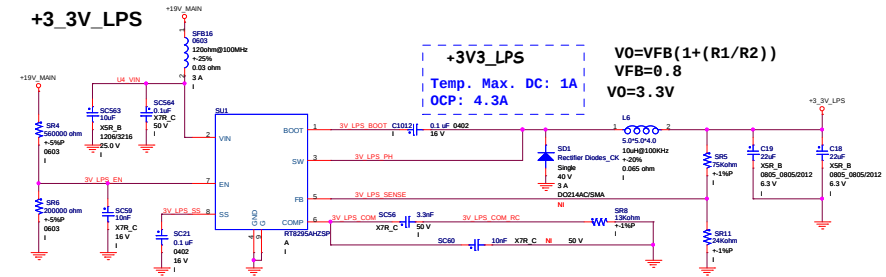
Vout=0.6*(1+R3/R4)=3.318V

FCCM	Level(Efficiency Mode)
<0.8V	Low(DCM enabled)
1.9V~2.1V	Float (audio filter enabled)
>2.4v	High(forced CCM)

LITE-ON TECHNOLOGY CORP.		
Title: 50. +5V_DUAL / +3_3V_DUAL		
Size: Custom	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 50 of 62	







LITE-ON TECHNOLOGY CORP.		
Title	51_ +5V/ +3.3V/ +3_3V_LPS/ ME	
Size C	Document Number JC184/JC186	Rev A04
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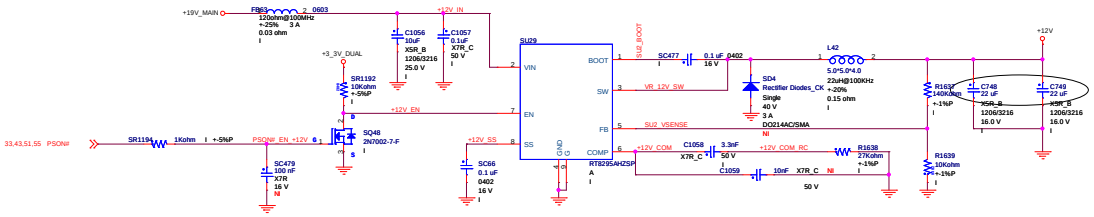
+12V

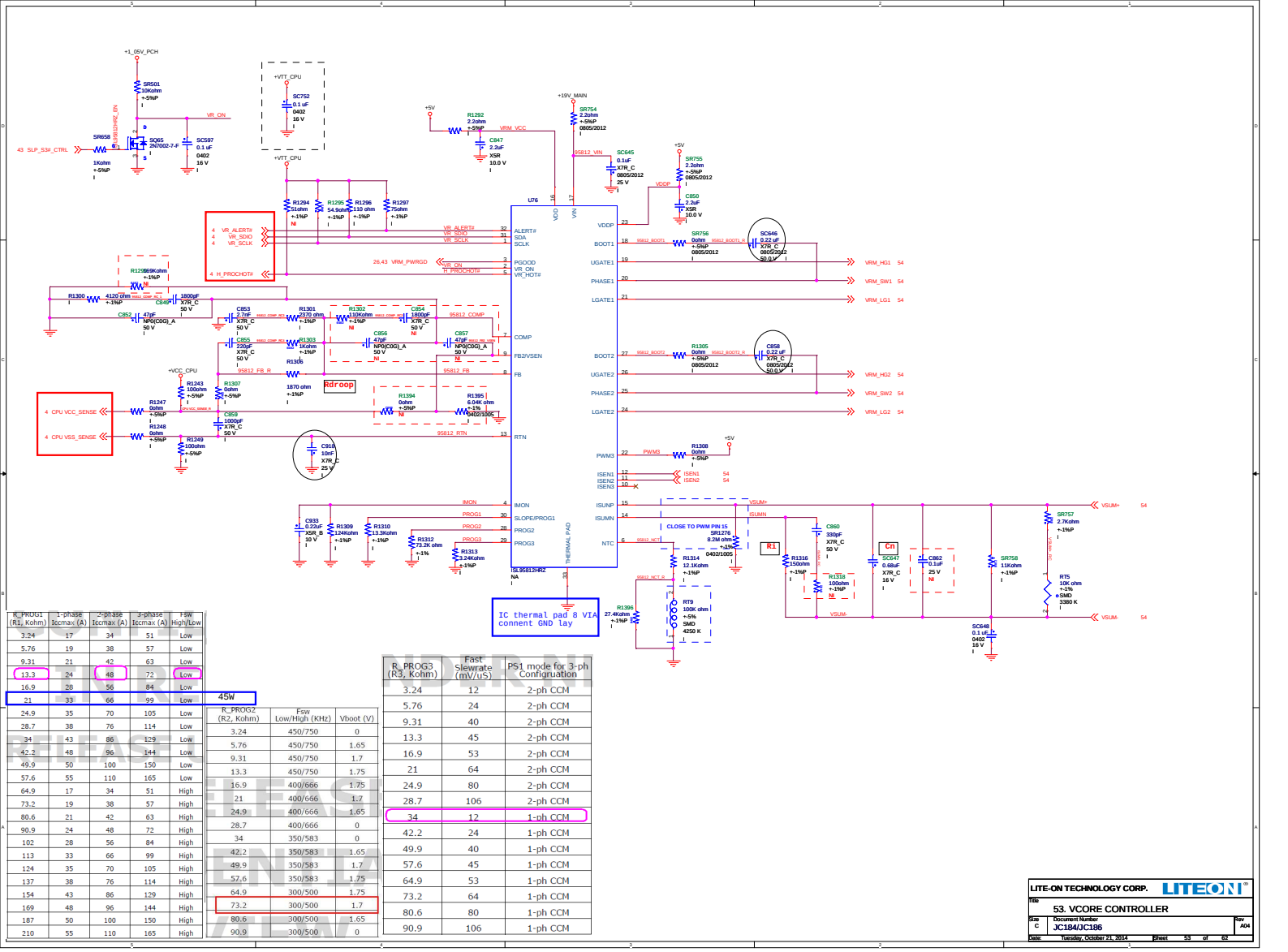


+12V

Temp. Max. DC: 0.7A
OCP: 4.3A

VO=VFB(1+(R1/R2))
VFB=0.8
VO=12.05V

LITE-ON TECHNOLOGY CORP.		
Title: 52. +12V		
Size: C	Document Number: JC184/JC186	Rev: A04
Date: Tuesday, October 21, 2014	Sheet 52 of 62	



R_PROG1 (R1, Kohm)	1-phase Iccmax (A)	2-phase Iccmax (A)	3-phase Iccmax (A)	Fsw High/Low
3.24	17	34	51	Low
5.76	19	38	57	Low
9.31	21	42	63	Low
13.3	24	48	72	Low
16.9	28	56	84	Low
21	33	66	99	Low
24.9	35	70	105	Low
28.7	38	76	114	Low
34	43	86	129	Low
42.2	48	96	144	Low
49.9	50	100	150	Low
57.6	55	110	165	Low
64.9	17	34	51	High
73.2	19	38	57	High
80.6	21	42	63	High
90.9	24	48	72	High
102	28	56	84	High
113	33	66	99	High
124	35	70	105	High
137	38	76	114	High
154	43	86	129	High
169	48	96	144	High
187	50	100	150	High
210	55	110	165	High

45W

R_PROG2 (R2, Kohm)	Fsw Low/High (KHz)	Vboot (V)
3.24	450/750	0
5.76	450/750	1.65
9.31	450/750	1.7
13.3	450/750	1.75
16.9	400/666	1.75
21	400/666	1.7
24.9	400/666	1.65
28.7	400/666	0
34	350/583	0
42.2	350/583	1.65
49.9	350/583	1.7
57.6	350/583	1.75
64.9	300/500	1.75
73.2	300/500	1.7
80.6	300/500	1.65
90.9	300/500	0

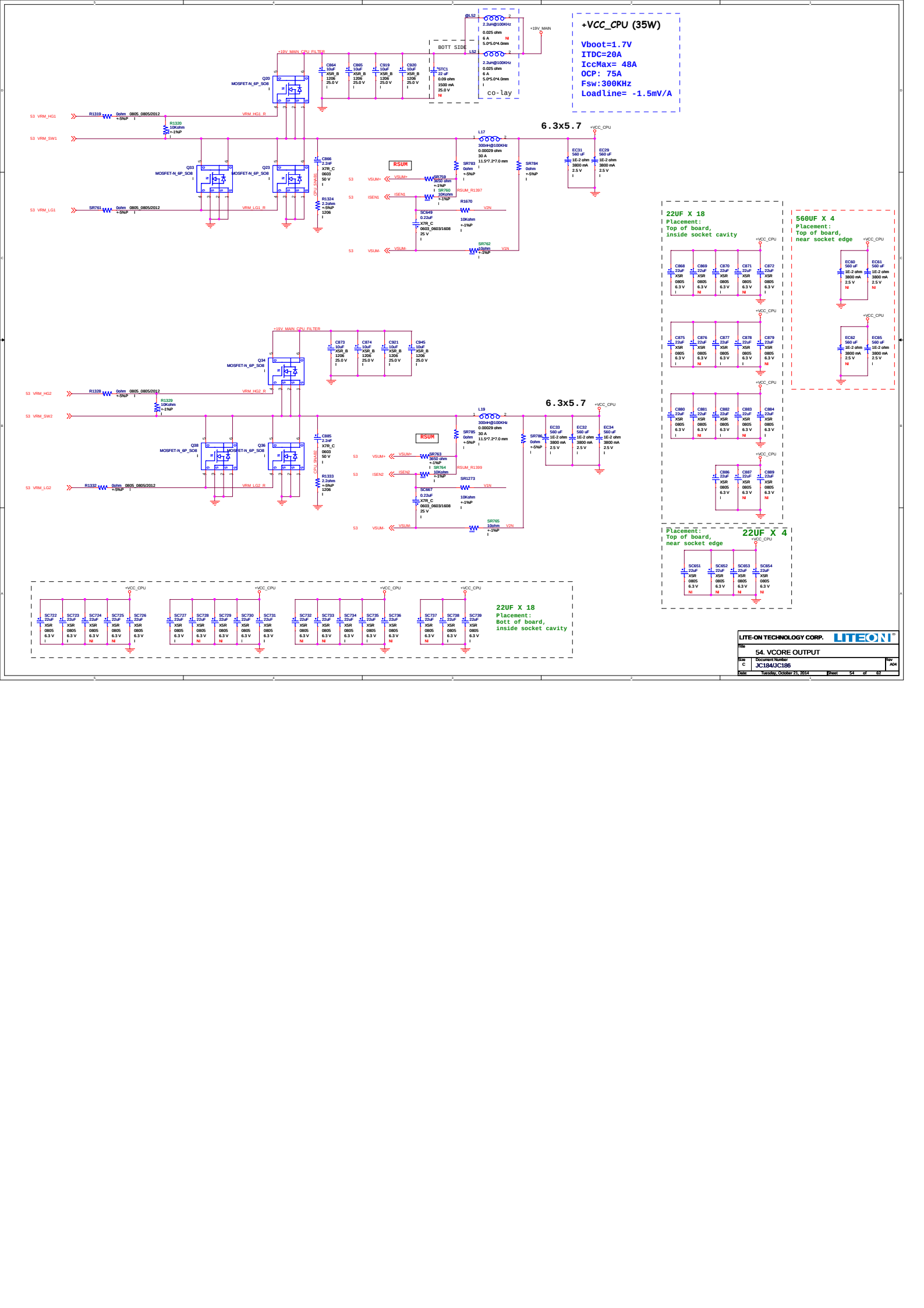
R_PROG3 (R3, Kohm)	Fast Slewrate (mV/uS)	PS1 mode for 3-ph Configruation
3.24	12	2-ph CCM
5.76	24	2-ph CCM
9.31	40	2-ph CCM
13.3	45	2-ph CCM
16.9	53	2-ph CCM
21	64	2-ph CCM
24.9	80	2-ph CCM
28.7	106	2-ph CCM
34	12	1-ph CCM
42.2	24	1-ph CCM
49.9	40	1-ph CCM
57.6	45	1-ph CCM
64.9	53	1-ph CCM
73.2	64	1-ph CCM
80.6	80	1-ph CCM
90.9	106	1-ph CCM

LITE-ON TECHNOLOGY CORP.

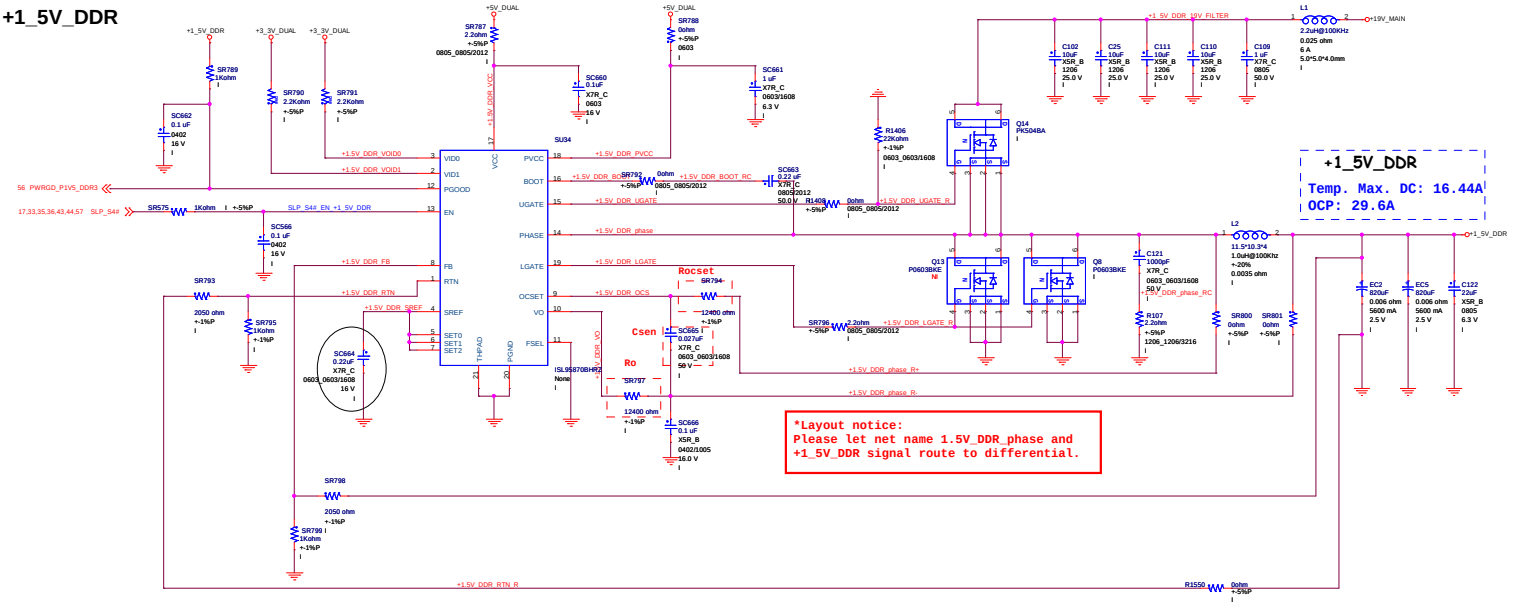
Title: 53. VCORE CONTROLLER

Size: C | Document Number: JC184/JC186 | Rev: A04

Date: Tuesday, October 21, 2014 | Sheet 53 of 62


+VCC_CPU (35W)
Vboot=1.7V
ITDC=20A
IccMax= 48A
OCP: 75A
Fsw:300KHz
Loadline= -1.5mV/A
BOTT SIDE
co-lay
6.3x5.7
RSUM
22UF X 18
Placement:
Top of board,
inside socket cavity
560UF X 4
Placement:
Top of board,
near socket edge
22UF X 4
Placement:
Top of board,
near socket edge
22UF X 18
Placement:
Bott of board,
inside socket cavity
LITE-ON TECHNOLOGY CORP.
54. VCORE OUTPUT
JC184/JC186
Tuesday, October 21, 2014

+1_5V_DDR



OCP

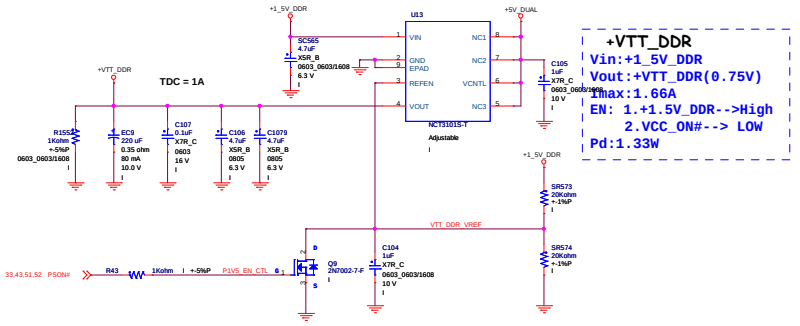
L=	1	uH
DCR=	3.5	m ohm
Ioc=	30	A
Csen=	27.21088	nF
Rocset=	10.5	K ohm
Ro=	10.5	K ohm

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{I_{OCSET}}$$

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR}$$

FSEL=>Pull this pin directly to GND for 300kHz.

check TINY SCH



LITE-ON TECHNOLOGY CORP.	LITEON
Title	55. +1.5V_DDR / +VTT_DDR
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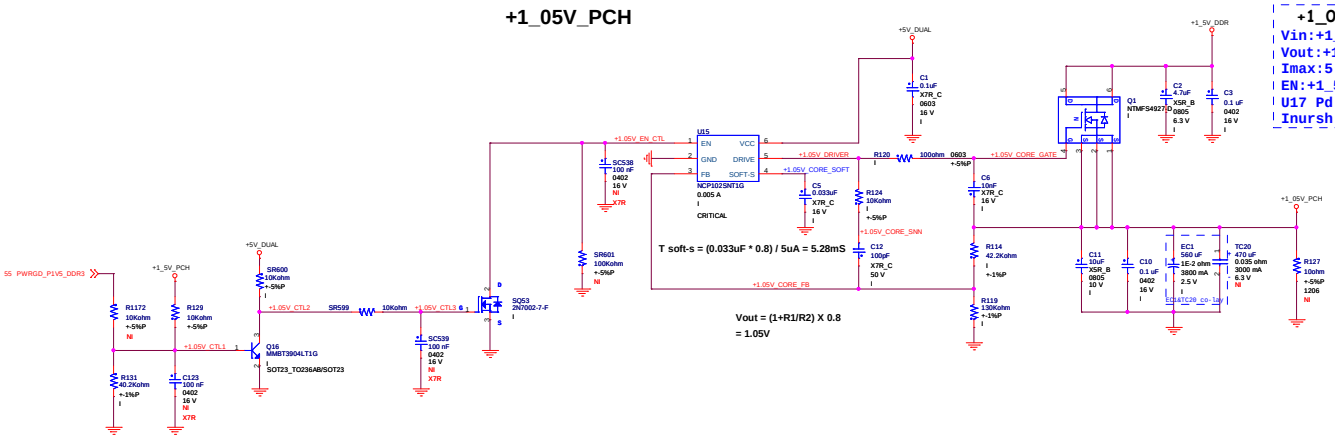
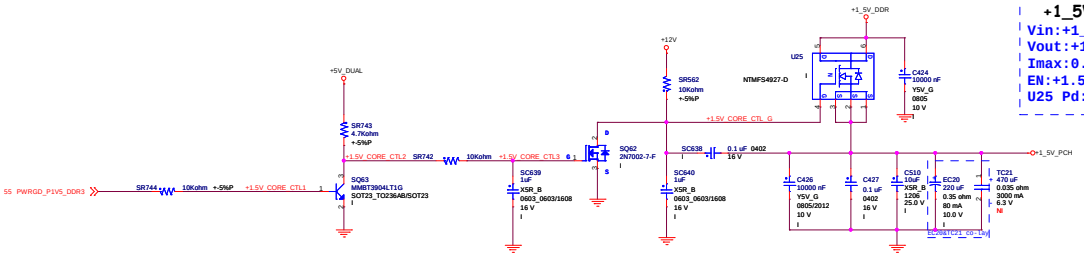
+1_05V_PCH



+1_05V_PCH
Vin:+1_5V_DDR
Vout:+1_05V_PCH(1.05V)
Imax:5.295A
EN:+1_5V_CORE High
U17 Pd:2.7W
Inursh_current:0.163A

+1_5V_PCH



+1_5V_PCH
Vin:+1_5V_DDR
Vout:+1_5V_PCH(+1.5V)
Imax:0.183A
EN:+1.5V_CORE_CTL_G High
U25 Pd:2.7W

LITE-ON TECHNOLOGY CORP.		
Title	56. +1_5V_PCH /+1_05V_PCH	
Size C	Document Number JC184/JC186	Rev A04
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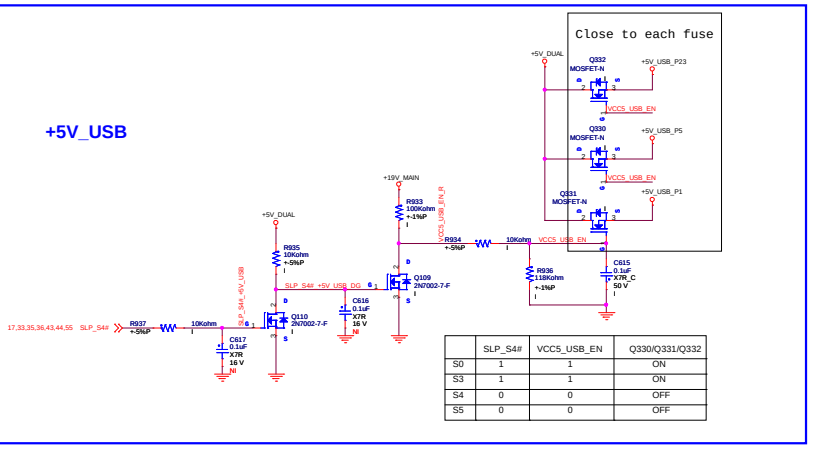
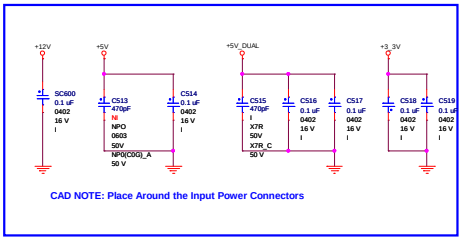
+5V_USB

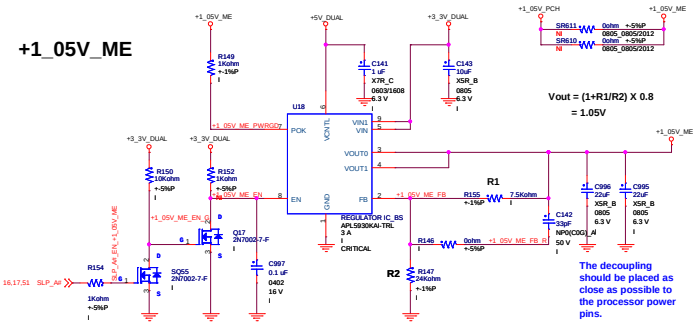


	SLP_S4#	VCC5_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF



CAD NOTE: Place Around the Input Power Connectors

+1_05V_ME



Vout = (1+R1/R2) X 0.8
= 1.05V

The decoupling should be placed as close as possible to the processor power pins.

+1_05V_ME
Vin:+3_3V_DUAL
Vout:+1_05V_ME (+1.05V)
Imax:0.67A
Pd:2W

LITE-ON TECHNOLOGY CORP.		LITEON
Title	57. +1_05V_ME / +5V_USB	
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PCH STRAPPING PIN

Signal	Usage	When Sampled	Comment
SPKR (S_SPKR_OUT)	No Reboot	Rising edge of PWROK	Set pull down. The signal has weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
GPIO62 / SUSCLK (SUSCLK_GP62)	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	Set pull high. THis has a weak internal pull-up Note: The internal pull-up is disabled after RSMRST#
GPIO55	Top-Block Swap Override	Rising edge of PWROK	Set pull high. The signal has weak internal pull-up . If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
INTVRMEN (S_INTVRMEN)	Integrated V VRM Enable / Disable	Always	Set pull high. Integrated VRMs is enabled when INTVRMEN is sampled high
GPIO51	Boot BIOS Strap Bit[1] BBS[1]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO19 / SATA1GP	Boot BIOS Strap Bit[0] BBS[0]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO53	ESI Strap (Server/Workstation Only)	Rising edge of PWROK	Set pull high. This Signal has a weak internal pull-up.Tying this strap low configures DMI for ESI compatible operation.
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	reserve pull up If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPIO36 (CLEAR_CMOS#)	RSVD	Rising edge of PWROK	Set pull high. This signal has a weak internal pull-down.
GPIO37 / SATA3GP (GPIO_37)	TLS Confidentiality	Rising edge of PWROK	Set pull high. This signal has a weak internal pull down. TLS CONFIDENTIALITY DISABLE LOW:DISABLE
DDPB_CTRLDATA (V_DDPB_CTRLCLK)	PORT B Detected	Rising edge of PWROK	When ‘1’- Port B is detected; When ‘0’- Port B is not detected. This signal has a weak internal pull-down.
DDPC_CTRLDATA (V_DDPC_CTRLDATA)	PORT C Detected	Rising edge of PWROK	When ‘1’- Port C is detected; When ‘0’- Port C is not detected. This signal has a weak internal pull-down.
DDPD_CTRLDATA (V_DDPD_CTRLDATA)	PORT D Detected	Rising edge of PWROK	When ‘1’- Port D is detected; When ‘0’- Port D is not detected. This signal has a weak internal pull-down.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep Sx Well (DSW) On-Die VR mode is enabled.
GPIO36 / SATA2GP (CLEAR_CMOS#)	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
GPIO8 (IGE_EN#)	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal should not be pulled low when strap is sampled.

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Title: 58. STRAPPING PIN

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PCH GPIO TABLE

GPIO	Signal Name	Power Well	In/Out	Tiny II
GPIO_0	BMBUSY-_GPIO0	VCC3	IN	SIO_SCI#
GPIO_1	TACH1_GPIO1	VCC3	IN	BRD_ID1
GPIO_2	PIRQE-_GPIO2	VCC3	IN	SIO_SCI1#
GPIO_3	PIRQF-_GPIO3	VCC3	IN	SIO_SCI2#
GPIO_4	PIRQG-_GPIO4	VCC3	NATIVE	GPIO_4(NO USE 8K2 PU)
GPIO_5	PIRQH-_GPIO5	VCC3	NATIVE	GPIO_5(NO USE 8K2 PU)
GPIO_6	TACH2_GPIO6	VCC3	IN	BRD_ID0
GPIO_7	TACH3_GPIO7	VCC3	IN	DP_C_DET#
GPIO_8	GPIO8	SB3V	IN	IGE_EN#
GPIO_9	OC5-_GPIO9	SB3V	NATIVE	OC5#_R_1011(NO USE 8K2 PU)
GPIO_10	OC6-_GPIO10	SB3V	OUT	OC6#_R_1213 (NO USE 8K2 PU)
GPIO_11	SMBALERT-_GPIO11	SB3V	IN	SIO_PME#
GPIO_12	LAN_PHY_PWR_CTRL_GPIO12	DSW	NATIVE	L_LAN_DISABLE#
GPIO_13	DA_DOCK_RST-_GPIO13	SB3V	OUT	PCH_GPIO13_PU(NO USE 10K PU)
GPIO_14	OC7-_GPIO14	SB3V	IN	OC7#_R_1415 (NO USE 8K2 PU)
GPIO_15	GPIO15	SB3V	IN	PCH_GP15_STRAP(NO USE 4.7K PU)
GPIO_16	SATA4GP_GPIO16	VCC3	NATIVE	MSATA_DET_GPIO16
GPIO_17	TACH0_GPIO17	VCC3	IN	BRD_ID3
GPIO_18	PCIECLKRQ1-_GPIO18	VCC3	IN	PCH_GP18 (NON USE 10K PD)
GPIO_19	SATA1GP_GPIO19	VCC3	IN	SATA1GP (10K PU/STRAP PIN)
GPIO_20	PCIECLKRQ2-_GPIO20_SMI-	VCC3	OUT	MINIPE_W_DISABLE#_2
GPIO_21	SATA0GP_GPIO21	VCC3	IN	THRM_ID1
GPIO_22	SCLOCK_GPIO22	VCC3	IN	GPIO_22 (NON USE 10K PU)
GPIO_23	LDRQ1-_GPIO23	VCC3	NATIVE	GPIO_23(NON USE)
GPIO_24	GPIO24	SB3V	IN	H_SKTOCC#
GPIO_25	PCIECLKRQ3-_GPIO25	SB3V	OUT	MINIPE_W_DISABLE#_1
GPIO_26	PCIECLKRQ4-_GPIO26	SB3V	IN	GP26_PD (NON USE 10K PD)
GPIO_27	GPIO27	DSW	IN	LANWAKE_R_N
GPIO_28	GPIO28	SB3V	OUT	PW_LED#
GPIO_29	SLP_WLAN-_GPIO29	DSW	NATIVE	PCH_GPIO29_PU(NON USE 10K PU)
GPIO_30	SUSWARN-_SUSPWRNACK_GPIO30	SB3V	NATIVE	SUSWARN#
GPIO_31	ACPRESENT_GPIO31	DSW	OUT	SUS_LED#
GPIO_32	GPIO32	VCC3	OUT	TPM_CLKRUN (NON USE)
GPIO_33	DOCKEN-_GPIO33	VCC3	IN	PCH_GP33 (NON USE 10K PD)
GPIO_34	GPIO34	VCC3	IN	BRD_ID2
GPIO_35	GPIO35_NMI-	VCC3	IN	USB_DET#
GPIO_36	SATA2GP_GPIO36	VCC3	IN	CLEAR_CMOS#(STRAP PIN)
GPIO_37	SATA3GP_GPIO37	VCC3	IN	GPIO_37 (STRAP PIN)
GPIO_38	SLOAD_GPIO38	VCC3	IN	GPIO_38(NON USE 10K PU)
GPIO_39	SDATAOUT0_GPIO39	VCC3	IN	GP39_GFX_CRB_DETECT
GPIO_40	OC1-_GPIO40	SB3V	NATIVE	USB_OC_REAR_23#
GPIO_41	OC2-_GPIO41	SB3V	NATIVE	USB_OC_REAR_45#
GPIO_42	OC3-_GPIO42	SB3V	OUT	MINIPE_W_DISABLE#
GPIO_43	OC4-_GPIO43	SB3V	NATIVE	USB_OC_REAR_89# (NON USE 8.2K PU)
GPIO_44	PCIECLKRQ5-_GPIO44	SB3V	OUT	BAT_LED#
GPIO_45	PCIECLKRQ6-_GPIO45	SB3V	IN	PRT_DET#
GPIO_46	PCIECLKRQ7-_GPIO46	SB3V	OUT	TPM_DISABLE#
GPIO_48	SDATAOUT1_GPIO48	VCC3	IN	COM_AB_DET#
GPIO_49	SATA5GP_GPIO49	VCC3	IN	NON USE 10K PU
GPIO_50	GPIO50	VCC3	OUT	GPIO_50
GPIO_51	GPIO51	VCC3	NATIVE	GPIO_51 (STRAP PIN)
GPIO_52	GPIO52	VCC3	IN	COM_A_DET#
GPIO_53	GPIO53	VCC3	IN	NON USE (STRAP PIN)
GPIO_54	GPIO54	VCC3	IN	GPIO_54 (NON USE 8.2K PU)
GPIO_55	GPIO55	VCC3	NATIVE	NON USE (STRAP PIN)
GPIO_57	GPIO57	SB3V	IN	NON USE 10K PU
GPIO_58	SML1CLK_GPIO58	SB3V	NATIVE	SMLINK1_CLK
GPIO_59	OC0-_GPIO59	SB3V	NATIVE	USB_OC_FRONT_01#
GPIO_60	SML0ALERT-_GPIO60	SB3V	IN	SMB0_ALERT#
GPIO_61	SUS_STAT-_GPIO61	SB3V	NATIVE	TPM_LPC_PD#
GPIO_62	SUSCLK_GPIO62	SB3V	NATIVE	SUSCLK_GP62 (STRAP PIN)
GPIO_63	SLP_S5-_GPIO63	SB3V	NATIVE	TP (NO USE)
GPIO_64	CLKOUTFLEX0_GPIO64	VCC3	NATIVE	TP (NO USE)
GPIO_65	CLKOUTFLEX1_GPIO65	VCC3	NATIVE	LPC_MINI_MSATA
GPIO_66	CLKOUTFLEX2_GPIO66	VCC3	NATIVE	TP (NO USE)
GPIO_67	CLKOUTFLEX3_GPIO67	VCC3	NATIVE(ITE) GPO(nuvoton)	CK_48M_SIO
GPIO_68	TACH4_GPIO68	VCC3	IN	LC_SENSE
GPIO_69	TACH5_GPIO69	VCC3	IN	THRM_ID2
GPIO_70	TACH6_GPIO70	VCC3	IN	PCH_GP70_PU
GPIO_71	TACH7_GPIO71	VCC3	IN	BRD_ID5
GPIO_72	GPIO72	DSW	OUT	PCH_GP72_PU (NON USE 1K PU)
GPIO_73	PCIECLKRQ0-_GPIO73	SB3V	IN	GP73_PD(NON USE 10K PD)
GPIO_74	SML1ALERT-_PCHHOT-_GPIO74	SB3V	NATIVE	PCH_GP74_PU(NON USE 10K PU)
GPIO_75	SML1DATA_GPIO75	SB3V	NATIVE	SMLINK1_DATA

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SIO IT8733F GPIO TABLE

GPIO	Signal Name	Tiny II
GPIO_10(PIN84)	PCIRST3#/GP10	DP_ESIO (PU SB3V)
GPIO_11(PIN34)	PCIRST2#/GP11	+19V_VIN CTL_SIO (PU SB3V)
GPIO_12(PIN33)	PCIRST1#/GP12	(NO USE)
GPIO_13(PIN32)	PWROK1/GP13	SIO_PWRGD_3V
GPIO_14(PIN31)	VCORE_EN/PCH_C1/GP14	SMLINK1_CLK
GPIO_15(PIN3)	PCIRSTIN#/CIRTX2/GP15/CPU_PG	SIO_SCI2# (PU +3.3V)
GPIO_16(PIN2)	5VSB_CTRL#/CIRRX2/GP16	SIO_SCI1# (PU +3.3V)
GPIO_17(PIN28)	RI2#/GP17	RI2-
GPIO_20(PIN27)	CTS2#/GP20	CTS2-
GPIO_21(PIN26)	DCD2#/GP21	DCD2-
GPIO_22(PIN25)	SCK/GP22	SIO_SCK
GPIO_23(PIN24)	SI/GP23	SIO_SI
GPIO_24(PIN23)	RTS2#/GP24	RTS2-
GPIO_25(PIN22)	DSR2#/GP25	DSR2-
GPIO_26(PIN21)	SOUT2/GP26	SOUT2-
GPIO_27(PIN20)	SIN2/GP27	SIN2-
GPIO_30(PIN19)	ATXPG/GP30	PWRGD_PS
GPIO_31(PIN18)	PWMOUT / GP31 / USBPWREN2#	SIO_CHR_USBPWREN (PU SB3V)
GPIO_32(PIN17)	DPWROK/GP32	SIO_GP32(NO USE)
GPIO_33(PIN16)	SUSACK#/GP33	SIO_PIN16_EC(4.7K PD)
GPIO_34(PIN15)	SUSWARN#/GP34	(NO USE)
GPIO_35(PIN14)	FAN_TAC4/GP35	INT1_G_SIO
GPIO_36(PIN13)	FAN_CTL3/GP36	INT2_G_SIO
GPIO_37(PIN12)	FAN_TAC3/GP37	SIO_PIN12(NO USE 4.7K PU)
GPIO_40(PIN79)	3VSBSW#/GP40	ME_CNTL
GPIO_41(PIN78)	PWROK2/GP41	SIO_SCI#
GPIO_42(PIN76)	PSON#/GP42	SIO_PSON#
GPIO_43(PIN75)	PANSWH#/GP43	SIO_PB_IN
GPIO_44(PIN72)	PWRON#/GP44	PWRBTN_OUT#
GPIO_46(PIN66)	D_RX0/SMBCLK2/GP46/IRRX	SIO_RTCX2
GPIO_47(PIN65)	D_TX0/SMDAT2/GP47	SIO_RTCX1
GPIO_50(PIN48)	SO/GP50	SIO_SO
GPIO_51(PIN11)	FAN_CTL2/GP51	(NO USE)
GPIO_52(PIN10)	FAN_TAC2/GP52	SIO_PIN10(NO USE 4.7K PU)
GPIO_53(PIN77)	SUSC#/GP53	SLP_S4#
GPIO_54(PIN73)	PME#/GP54/USBPWREN1#	SIO_PME#
GPIO_55(PIN85)	RSMRST#/CIRRX1/GP55	RSMRST_N_SIO
GPIO_56(PIN83)	MCLK/GP56	2543_CLT1 (PU SB3V)
GPIO_57(PIN82)	MDAT/GP57	2543_EN (PU SB3V)
GPIO_60(PIN81)	KCLK/GP60	2543_CLT3 (PU SB3V)
GPIO_61(PIN80)	KDAT/GP61	CHARGER_OC_SIO# (PU SB3V)
GPIO_62(PIN45)	KRST#/GP62	KBRST#
GPIO_63(PIN6)	SLP_SUS#/VLDT_EN/GP63	5V_DUAL_DISABLE#
GPIO_70(PIN113)	KSI0/GP70/PD0	PD0
GPIO_71(PIN114)	KSI1/GP71/PD1	PD1
GPIO_72(PIN115)	JP1/KSO0/GP72/PD2	PD2
GPIO_73(PIN116)	KSO1/GP73/PD3	PD3
GPIO_74(PIN117)	KSO2/GP74/PD4	PD4
GPIO_75(PIN118)	KSO3/GP75/PD5	PD5
GPIO_76(PIN119)	KSO4/GP76/PD6	PD6
GPIO_77(PIN120)	KSO5/GP77/PD7	PD7
GPIO_85(PIN64)	IO_SCI#/GP85/SMBDAT0	APS_I2C_DATA
GPIO_86(PIN63)	GP86/SMBCLK0	APS_I2C_CLK

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Title: 60. SIO GPIO TABLE

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JC186 A01 LI_3BTA1232AA-R to JC186 A01A LI_3BTA1232AA-R

Page28 NI SR817 and install SR833 for Monitor Power on
Page49 Change SR10 form 10K to 1.3K for DC IN detect

A01 TO A03 FOR HEAD CODE CHANGE(3BTA1232bA-R,3BTA1232CA-R)

JC186 A03A(3BTA1232CA-R)-0709

Page17 NI R1651 for Lenovo request and follow Mini PCi-e SPEC Pin define

JC186 A03B(3BTA1232CA-R)

Page55 Due Quility issues to remove GLOBALTECH Symbol in the Schematic and replace with NUVOTON

JC186 A04(3BTA1232DA-R) HEAD CODE CHANGE

Base on lenovo request , Lotes Audio JACK have Inset /pull issues so cahnge MFG PN and need update Lenovo Head code

JC186 A04A(3BTA1232DA-R)

Remove J17 for Lenovo request

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