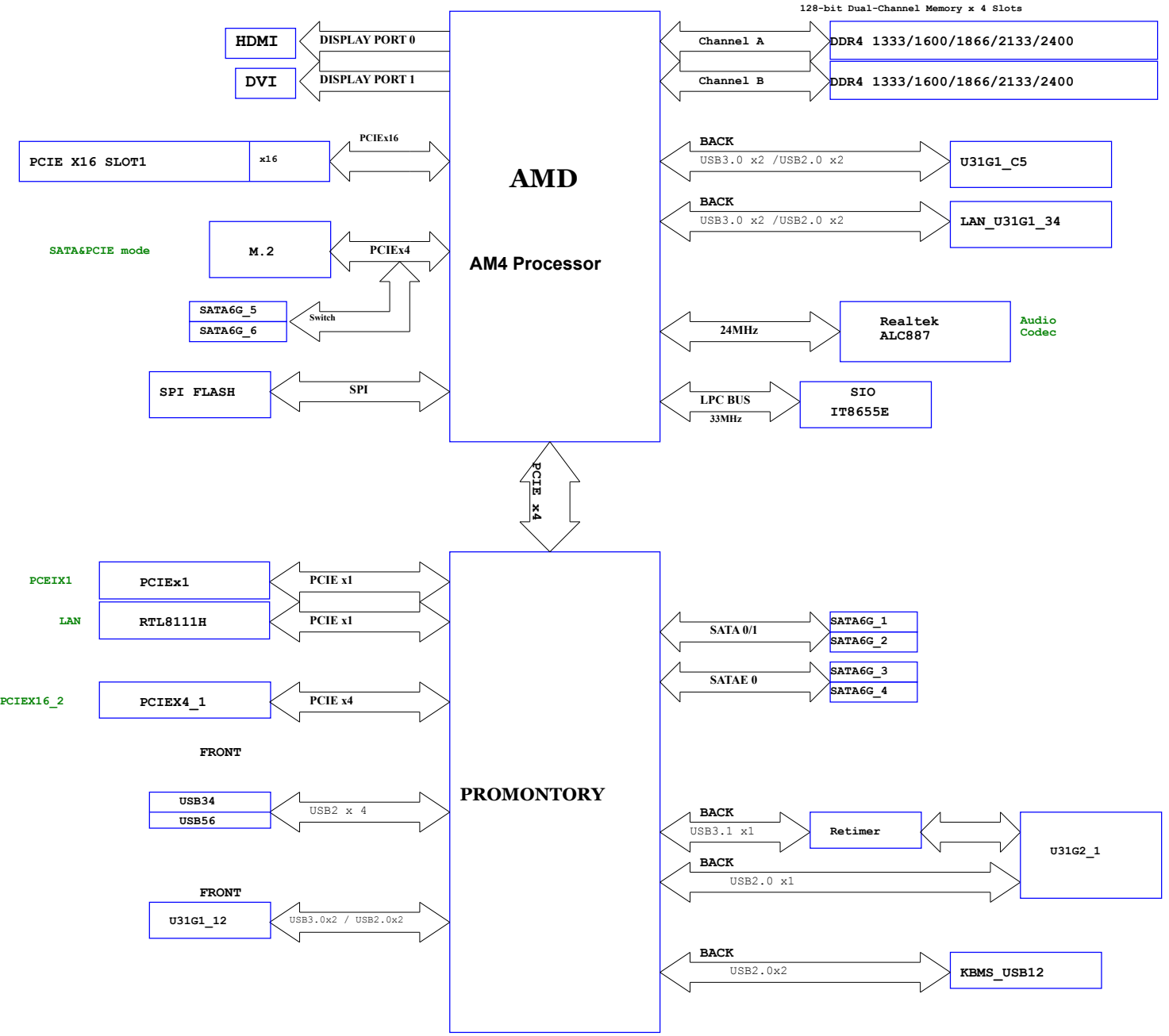
TUF B450M-PLUS GAMING

Rev 1.03 2018.6.4



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03	POWER Sequence
05	P-Power Flow
06-09	VCore
10-30	Other Power
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32	AM4-02(PCIE/HUB)
33	AM4-03(DISPLAY/MISC)
34	AM4-04(GPIO/ACPI/AUDIO)
35	AM4-05(USB/SPI/CLK/LPC)
36	AM4-06(PWR)
37	AM4-07(GND)
38	AM4-08(STRAPS)
39	AM4-09(LPC RC)
40	AM4-10(DDR4 Channel A)
41	AM4-11(DDR4 Channel B)
42	AM4-12(DDR4 PWR)
43	AM4-13(DDR4 PWR CAP)
44	AM4-14(RTC)
45	AM4-15(DP)
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54	PROM-01(HUB/PCIE/SATA)
55	PROM-02(USB)
56	PROM-03(CLK)
57	PROM-04(GPIO/MISC)
58	PROM-05(PWR)
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88-98	USB
103-111	Other
113-114	AURA

ASUSTek Computer Inc.

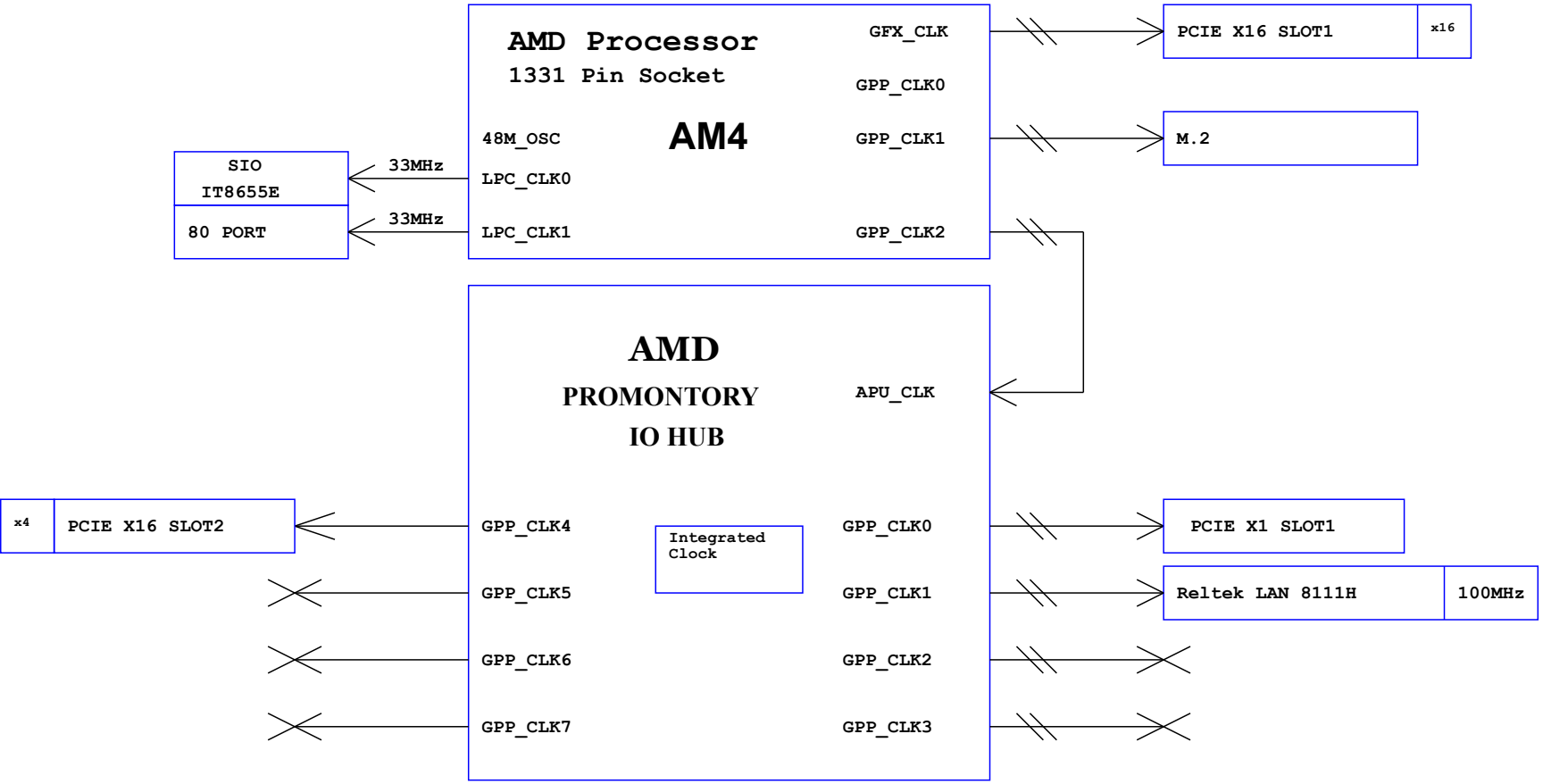
Title : Block Diagram

Engineer: Elainelx_Li

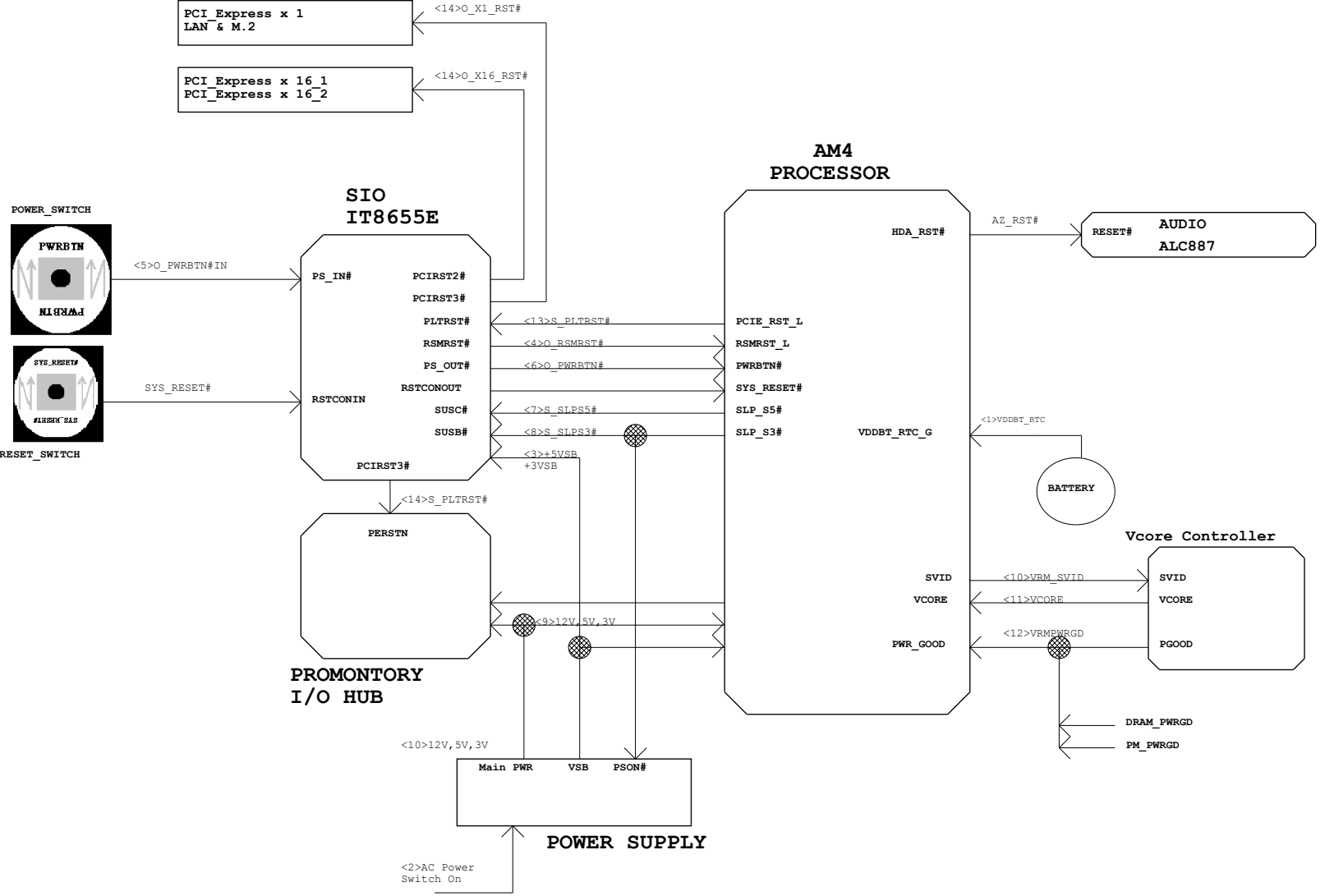
Size	Project Name	Rev
A3	AM4	R1.00

Date: Friday, August 17, 2018 Sheet 1 of 117

ICG : Integrated Clock Gen.



ASUSTek Computer Inc.	Title : CLOCK DISTRIBUTION	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: R1.00
Date: Friday, August 17, 2018	Sheet 2 of 117	



ASUSTek Computer Inc.	Title :	
	Engineer:	Elainelx_Li
Size: A3	Project Name: AM4	Rev: R1.00
Date: Friday, August 17, 2018	Sheet 3 of 117	

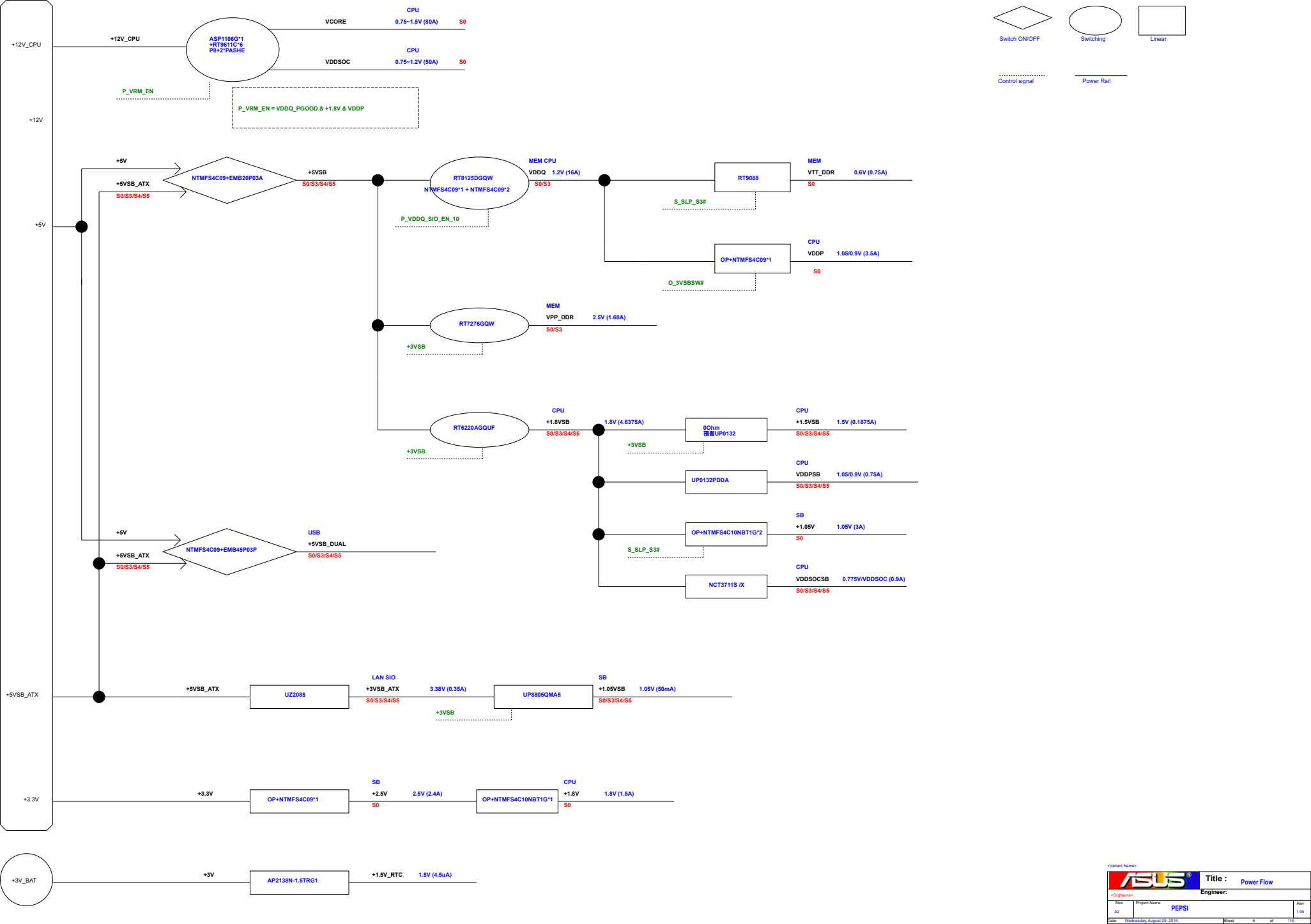
Title :

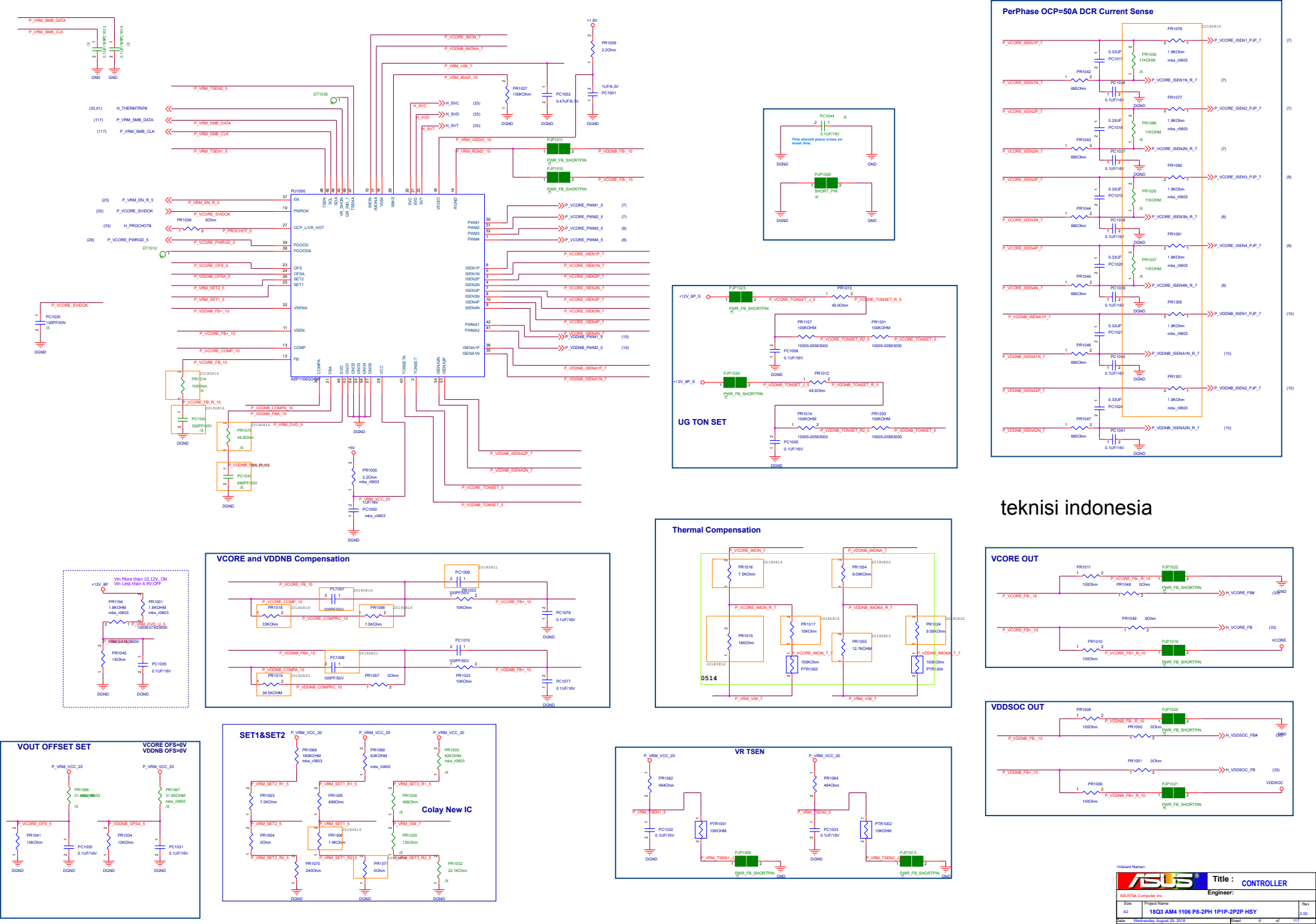
ASUSTek Computer Inc.

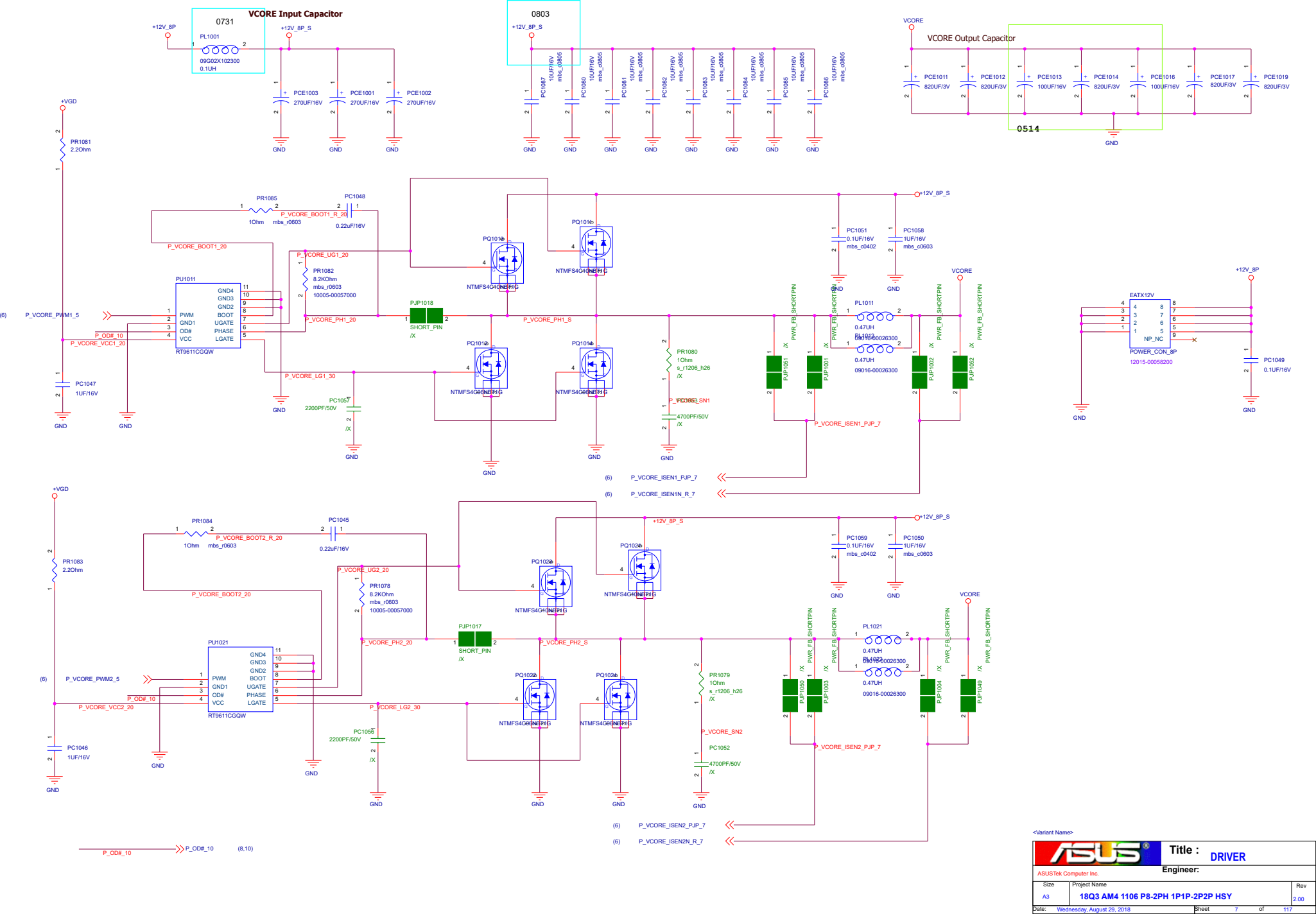
Engineer: ElaineIx_Li

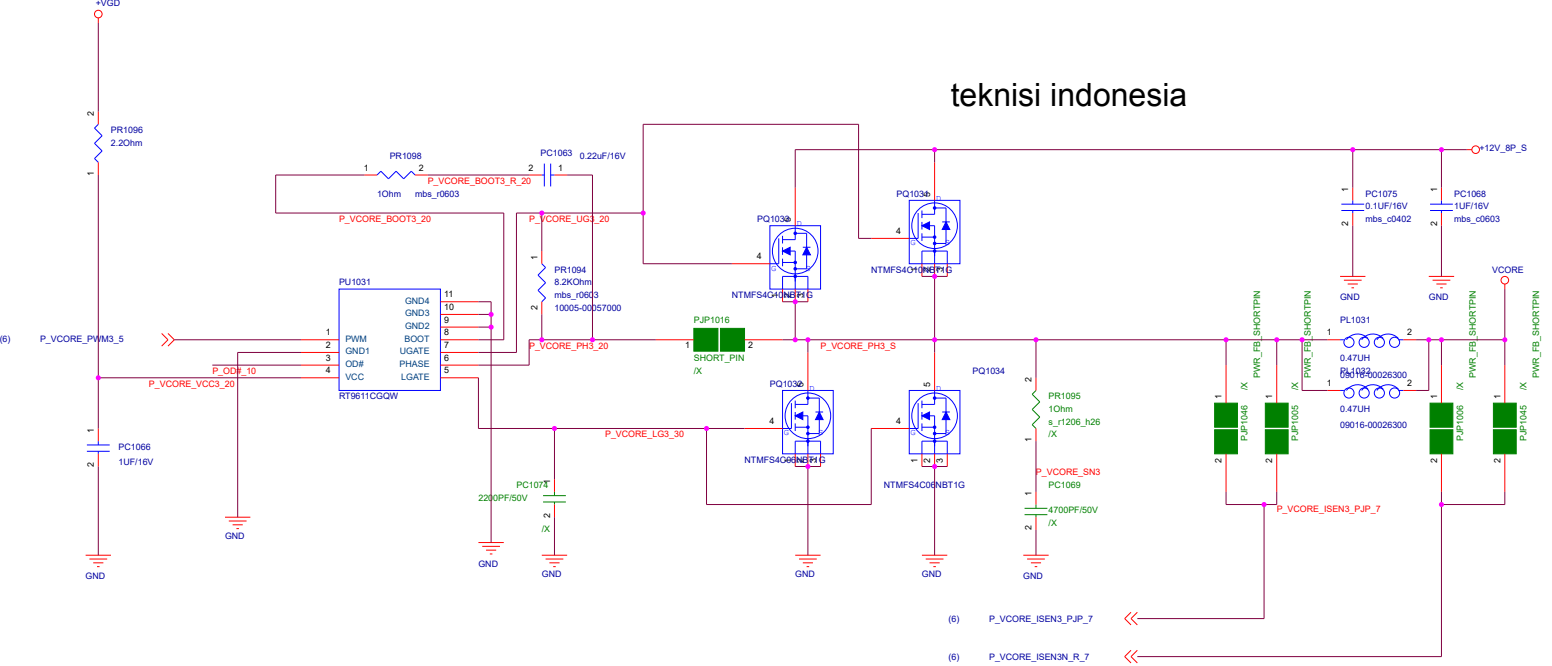
Size	Project Name	Rev
A3	AM4	R1.00

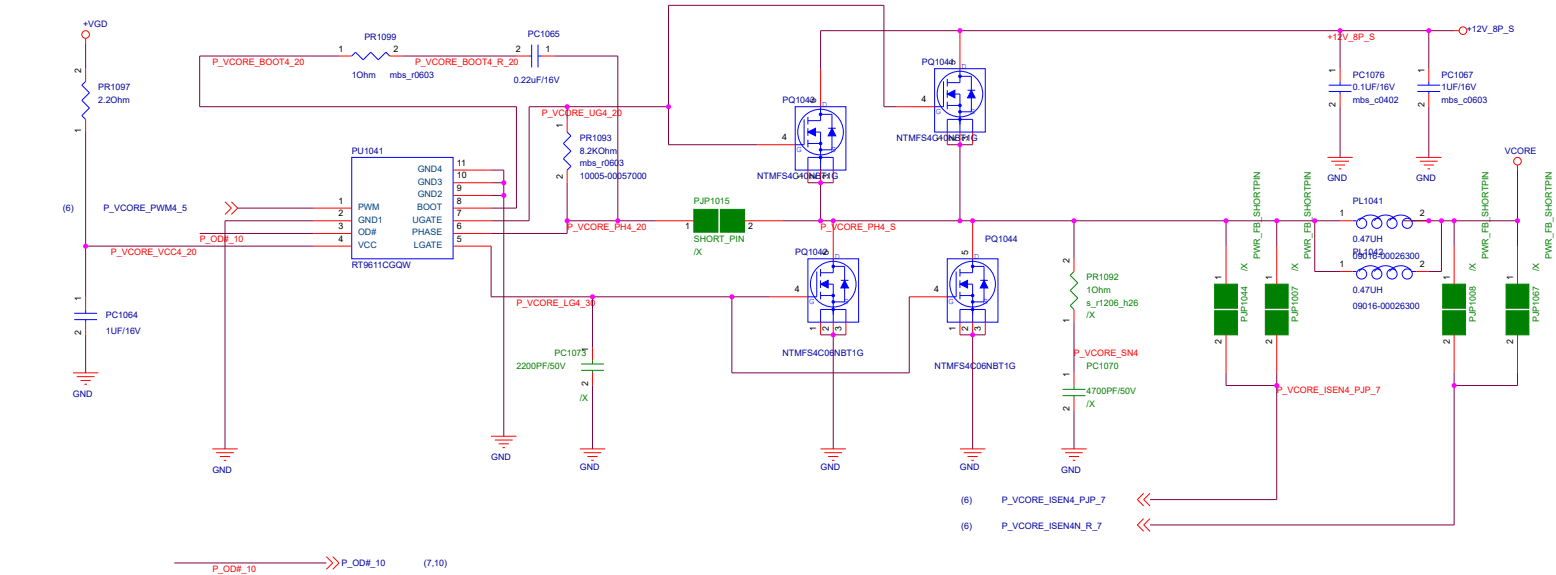
Date: Friday, August 17, 2018


Switch ON/OFF
Switching
Linear
Control signal
Power Rail
+12V_CPU
+12V_CPU
ASP1106G*1
+RT9611C*S
P8+2*PASHE
CPU
VCORE
0.75~1.5V (80A)
S0
CPU
VDDSOC
0.75~1.2V (50A)
S0
P_VRM_EN
P_VRM_EN = VDDQ_PGOOD & +1.8V & VDDP
+12V
+5V
+5V
+5VSB_ATX
S0/S3/S4/S5
NTMFS4C09+EMB20P03A
+5VSB
S0/S3/S4/S5
RT8125DGQW
NTMFS4C09*1 + NTMFS4C09*2
MEM CPU
VDDQ 1.2V (16A)
S0/S3
P_VDDQ_SIO_EN_10
RT9088
MEM
VTT_DDR 0.6V (0.75A)
S0
S_SLP_S3#
OP+NTMFS4C09*1
CPU
VDDP 1.05/0.9V (3.5A)
S0
O_3VSBSW#
RT7276GQW
MEM
VPP_DDR 2.5V (1.68A)
S0/S3
+3VSB
RT6220AGQUF
CPU
+1.8VSB
1.8V (4.6375A)
S0/S3/S4/S5
+3VSB
0Ohm
預留UP0132
CPU
+1.5VSB 1.5V (0.1875A)
S0/S3/S4/S5
+3VSB
UP0132PDDA
CPU
VDDPSB 1.05/0.9V (0.75A)
S0/S3/S4/S5
+5V
+5VSB_ATX
S0/S3/S4/S5
NTMFS4C09+EMB45P03P
USB
+5VSB_DUAL
S0/S3/S4/S5
OP+NTMFS4C10NBT1G*2
SB
+1.05V 1.05V (3A)
S0
S_SLP_S3#
NCT3711S /X
CPU
VDDSOCSB 0.775V/VDDSOC (0.9A)
S0/S3/S4/S5
+5VSB_ATX
+5VSB_ATX
UZ2085
LAN SIO
+3VSB_ATX 3.38V (0.35A)
S0/S3/S4/S5
+3VSB
UP8805QMA5
SB
+1.05VSB 1.05V (50mA)
S0/S3/S4/S5
+3.3V
+3.3V
OP+NTMFS4C09*1
SB
+2.5V 2.5V (2.4A)
S0
OP+NTMFS4C10NBT1G*1
CPU
+1.8V 1.8V (1.5A)
S0
+3V_BAT
+3V
AP2138N-1.5TRG1
+1.5V_RTC 1.5V (4.5uA)
<Variant Name>
Title : Power Flow
Engineer:
<OrgName>
Size A2
Project Name PEPSI
Rev 1.00
Date: Wednesday, August 29, 2018
Sheet 5 of 115


PerPhase OCP=50A DCR Current Sense
UG TON SET
Thermal Compensation
VCORE and VDDNB Compensation
SET1&SET2
Colay New IC
VOUT OFFSET SET
VCORE OFS=0V
VDDNB OFS=0V
VR TSEN
VCORE OUT
VDDSOC OUT
teknisi indonesia
Title : CONTROLLER
Engineer:
ASUSTeK Computer Inc.
Project Name
18Q3 AM4 1106 P8-2PH 1P1P-2P2P HSY
Wednesday, August 29, 2018


VCORE Input Capacitor
0731
+12V_8P
PL1001
09G02X102300
0.1UH
+12V_8P_S
PCE1003
270UF/16V
PCE1001
270UF/16V
PCE1002
270UF/16V
GND
0803
+12V_8P_S
PC1087
PC1080
PC1081
PC1082
PC1083
PC1084
PC1085
PC1086
10UF/16V
mbs_c0805
VCORE
VCORE Output Capacitor
PCE1011
PCE1012
PCE1013
PCE1014
PCE1016
PCE1017
PCE1019
820UF/3V
100UF/16V
100UF/16V
0514
+VGD
PR1081
2.2Ohm
PR1085
1Ohm
mbs_r0603
P_VCORE_BOOT1_R_20
PC1048
0.22uF/16V
P_VCORE_BOOT1_20
P_VCORE_UG1_20
PR1082
8.2KOhm
mbs_r0603
10005-00057000
PU1011
RT9611CGQW
PWM
GND1
OD#
VCC
GND2
GND3
GND4
BOOT
UGATE
PHASE
LGATE
(6) P_VCORE_PWM1_5
P_OD#_10
P_VCORE_VCC1_20
P_VCORE_LG1_30
P_VCORE_PH1_20
PJP1018
SHORT_PIN
/X
P_VCORE_PH1_S
PQ1014
PQ1015
PQ1016
PQ1017
NTMFS4C40NEPHG
PC1047
1UF/16V
PC1057
2200PF/50V
PR1080
1Ohm
s_r1206_h26
P_VCORE_SN1
PC1053
4700PF/50V
PC1051
0.1UF/16V
mbs_c0402
PC1058
1UF/16V
mbs_c0603
PWR_FB_SHORTPIN
PJP1051
PJP1031
PJP1032
PJP1052
PL1011
PL1012
0.47UH
09016-00026300
P_VCORE_ISEN1_PJP_7
P_VCORE_ISEN1N_R_7
(6) P_VCORE_ISEN1_PJP_7
(6) P_VCORE_ISEN1N_R_7
EATX12V
POWER_CON_8P
12015-00058200
NP_NC
PC1049
0.1UF/16V
+VGD
PR1083
2.2Ohm
PR1084
1Ohm
mbs_r0603
P_VCORE_BOOT2_R_20
PC1045
0.22uF/16V
P_VCORE_BOOT2_20
P_VCORE_UG2_20
PR1078
8.2KOhm
mbs_r0603
10005-00057000
PU1021
RT9611CGQW
(6) P_VCORE_PWM2_5
P_OD#_10
P_VCORE_VCC2_20
P_VCORE_LG2_30
P_VCORE_PH2_20
PJP1017
SHORT_PIN
/X
P_VCORE_PH2_S
PQ1022
PQ1023
PQ1024
PQ1025
NTMFS4C40NEPHG
PC1046
1UF/16V
PC1055
2200PF/50V
PR1079
1Ohm
s_r1206_h26
P_VCORE_SN2
PC1052
4700PF/50V
PC1059
0.1UF/16V
mbs_c0402
PC1050
1UF/16V
mbs_c0603
PJP1050
PJP1003
PJP1004
PJP1049
PL1021
PL1022
0.47UH
09016-00026300
P_VCORE_ISEN2_PJP_7
P_VCORE_ISEN2N_R_7
(6) P_VCORE_ISEN2_PJP_7
(6) P_VCORE_ISEN2N_R_7
P_OD#_10
(8,10)
<Variant Name>
Title : DRIVER
Engineer:
ASUSTek Computer Inc.
Size A3
Project Name 18Q3 AM4 1106 P8-2PH 1P1P-2P2P HSY
Rev 2.00
Date: Wednesday, August 29, 2018
Sheet 7 of 117





<Variant Name>

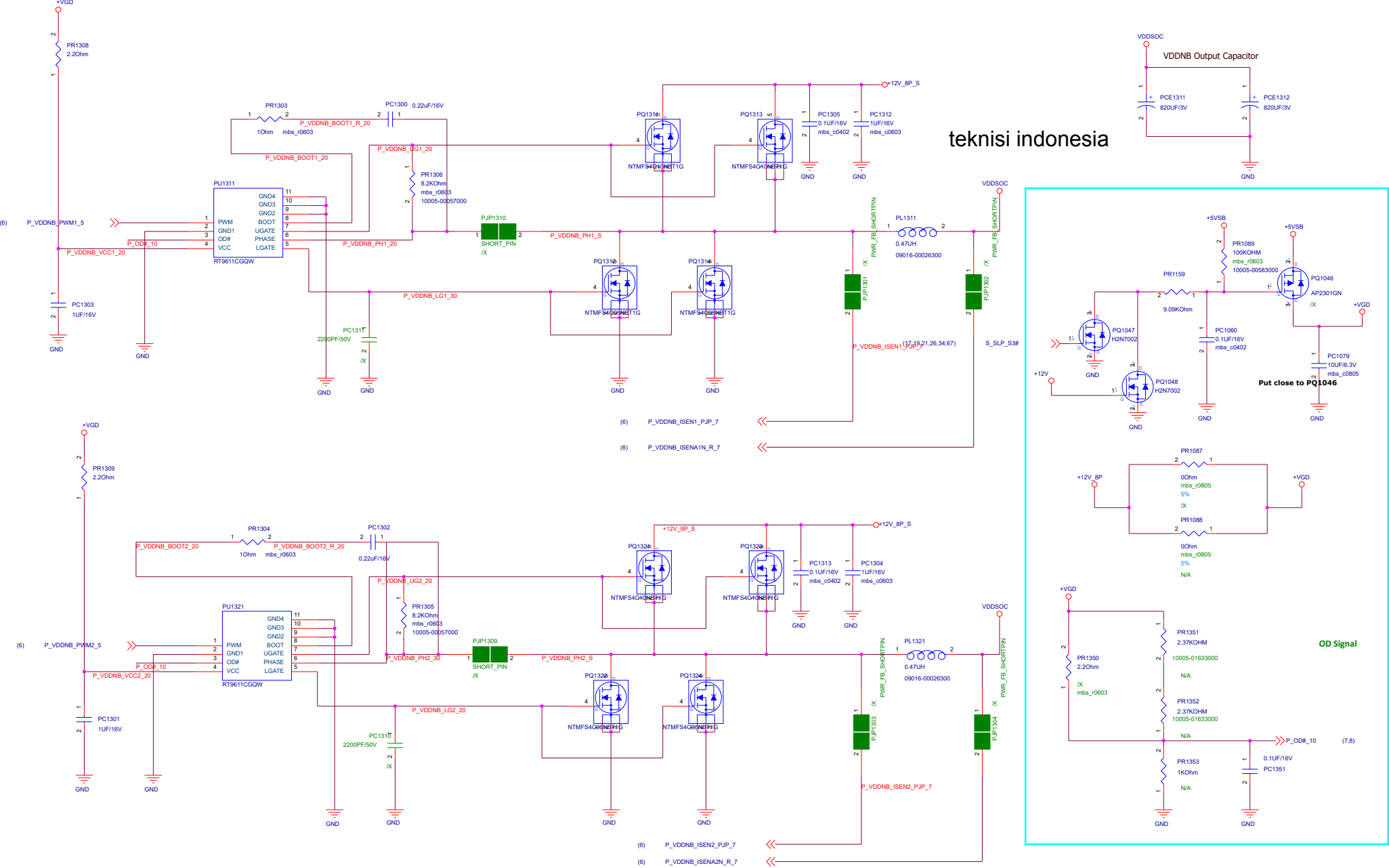
ASUSTek Computer Inc.	Title : DRIVER	
	Engineer:	
Size: A3	Project Name: 18Q3 AM4 1106 P8-2PH 1P1P-2P2P HSY	Rev: 2.00
Date: Wednesday, August 29, 2018	Sheet 8 of 117	

Title : VDDSOC Controller

Engineer:

ASUSTek Computer Inc.

Size	Project Name	Rev
A3	18Q2 AM4 1106 4-2PH 1P2P-2P2P?HSY?100	2.00



<Variant Name>

ASUSTek Computer Inc.

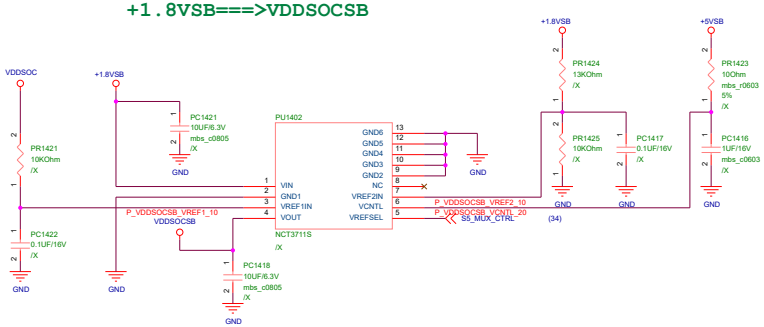
Title : DRIVER

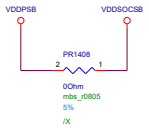
Engineer:

Size	Project Name	Rev
A3	18Q3 AM4 1106 P8-2PH 1P1P-2P2P HSY	2.00

Date: Wednesday, August 29, 2018 Sheet 10 of 117

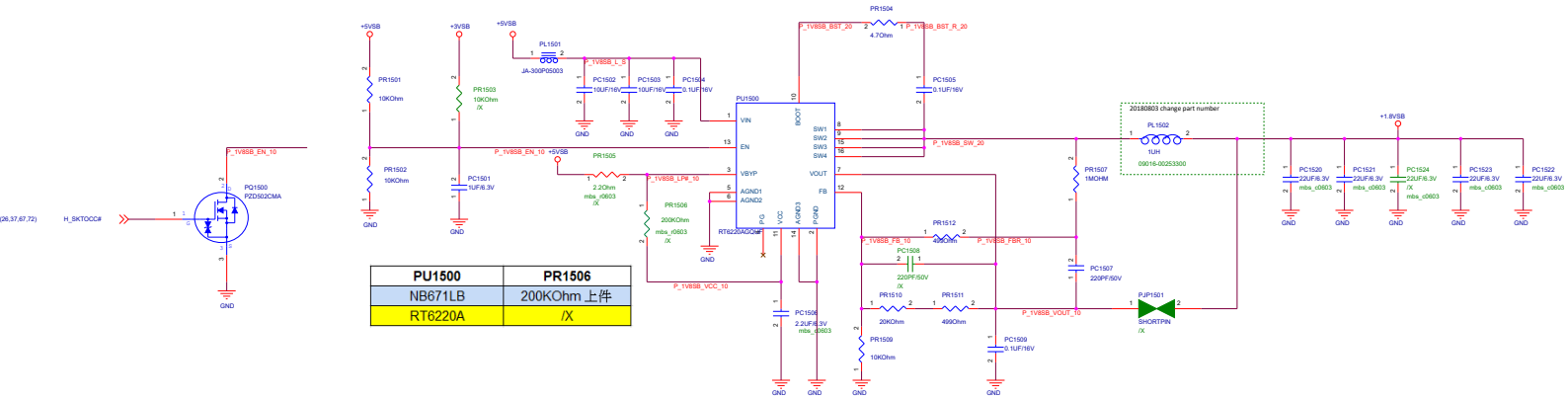
+1.8VSB===>VDDSOCSB





ASUSTek Computer Inc.	Title : VDDSOCSB	
	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 11 of 109	

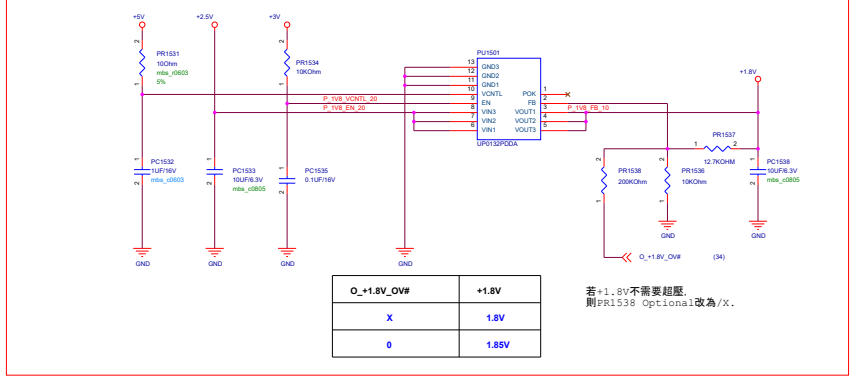
+5VSB====>+1.8VSB /3.735+0.9A



PU1500	PR1506
NB671LB	200KOhm 上件
RT6220A	/X

tek

+2.5V====>+1.8V 1A

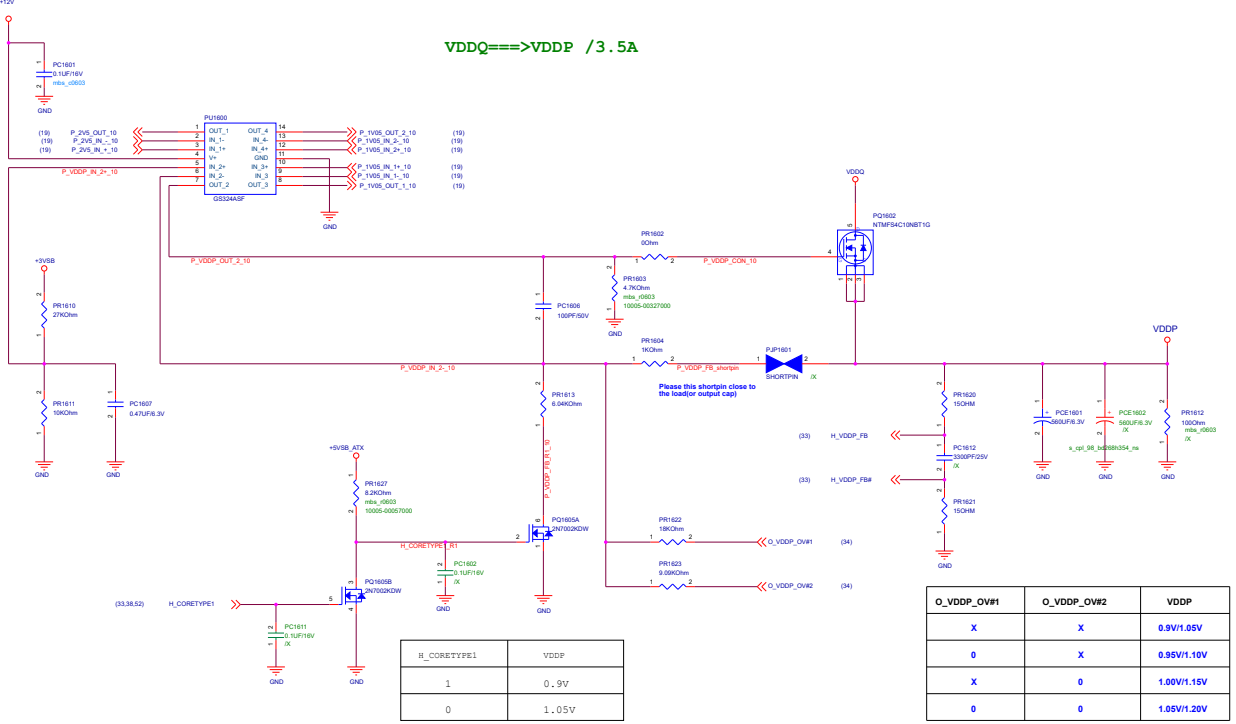


O_+1.8V_OV#	+1.8V
X	1.8V
0	1.85V

若+1.8V不需要超壓,
則PR1538 Optional改為/X.

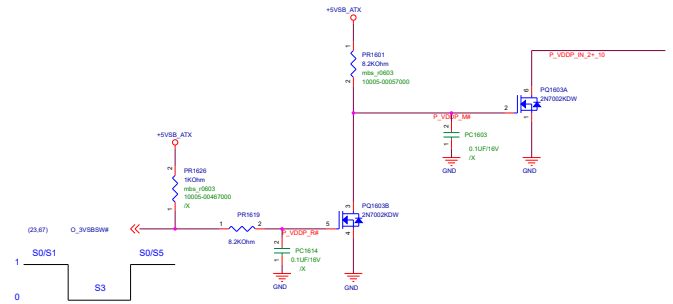
ASUSTek Computer Inc.	Title : +1.8VSB&+1.8V		
	Engineer:		
Size: A2	Project Name: AM4		Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 12 of 100		

VDDQ===>VDDP /3.5A

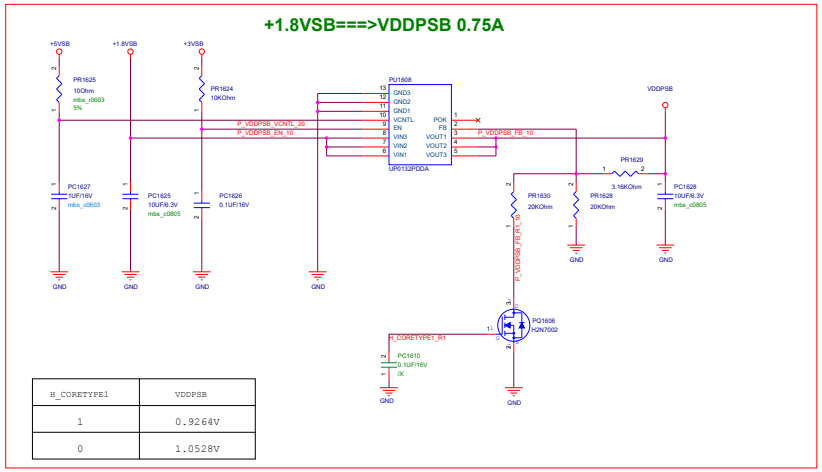


H_CORETYPE1	VDDP
1	0.9V
0	1.05V

O_VDDP_OV#1	O_VDDP_OV#2	VDDP
X	X	0.9V/1.05V
0	X	0.95V/1.10V
X	0	1.00V/1.15V
0	0	1.05V/1.20V



+1.8VSB===>VDDPSB 0.75A



H_CORETYPE1	VDDPSB
1	0.9264V
0	1.0528V

ASUSTek Computer Inc.	Title : VDDP&VDDPSB	
	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 13 of 109	

Title : NA

Engineer:

ASUSTek Computer Inc.

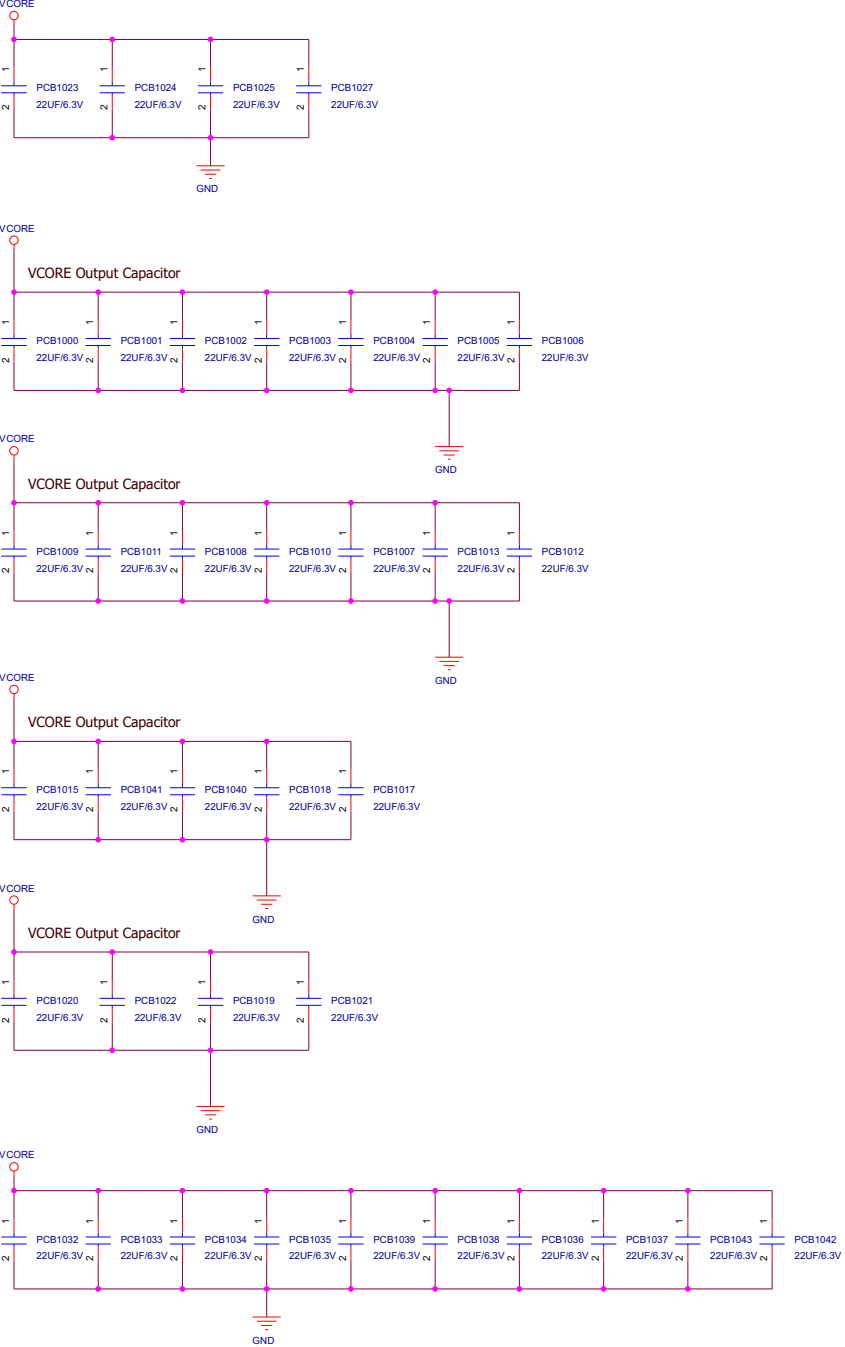
Size	Project Name	Rev
A2	**AM4**	1.00

Title : NA

Engineer:

ASUSTek Computer Inc.

Size	Project Name	Rev
A3	**AM4**	1.00



<Variant Name>

ASUSTek Computer Inc.

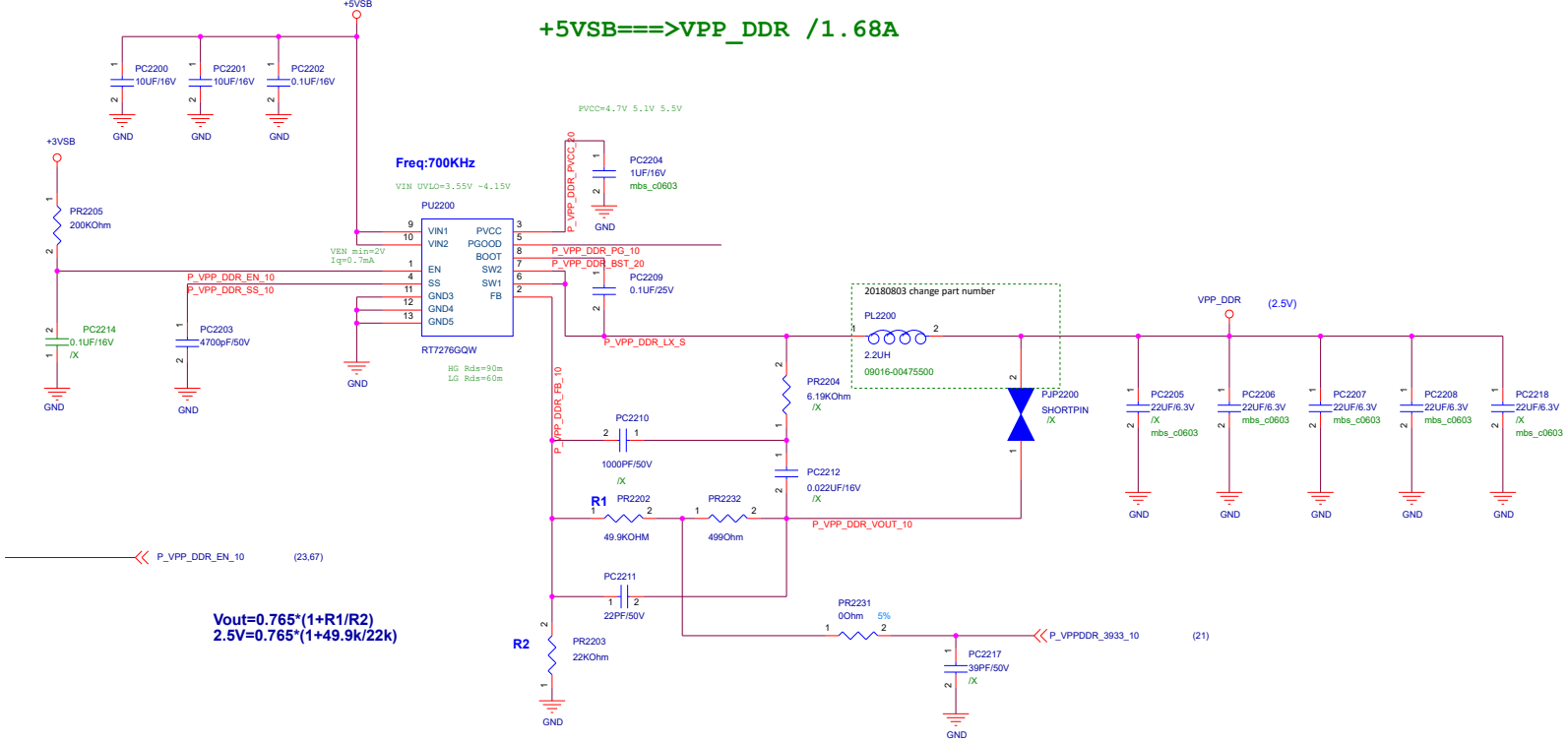
Title : Socket MLCC

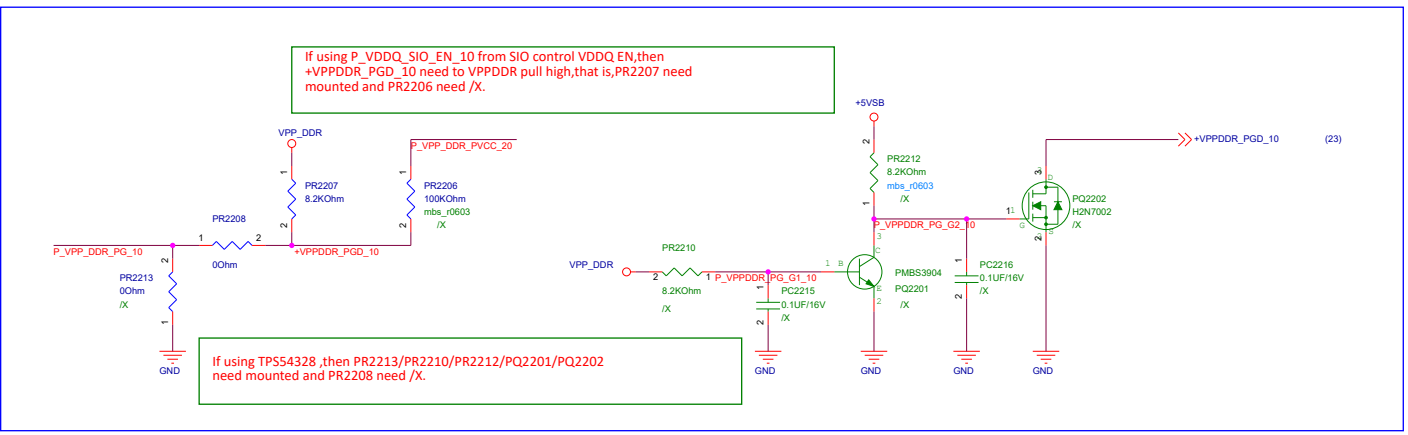
Engineer:

Size	Project Name	Rev
A3	18Q3 AM4 1106 P8-2PH 1P1P-2P2P HSY	2.00

Date: Wednesday, August 29, 2018 Sheet 16 of 117

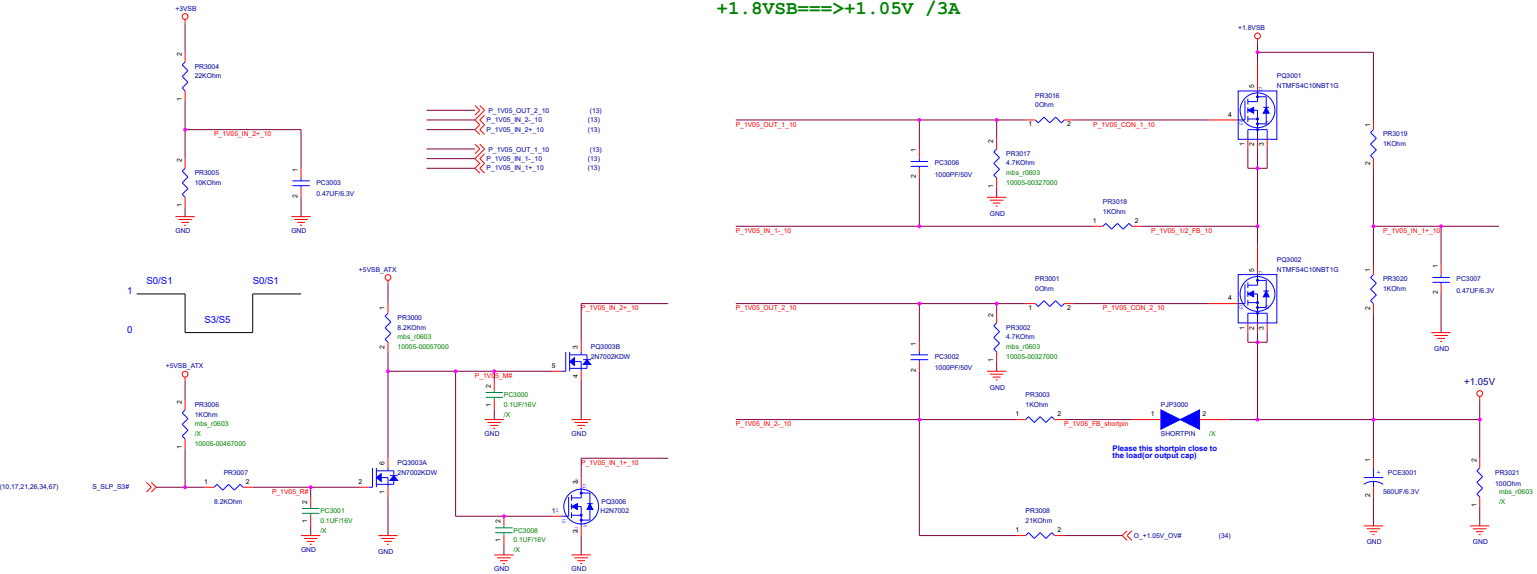
+5VSB===>VPP_DDR /1.68A





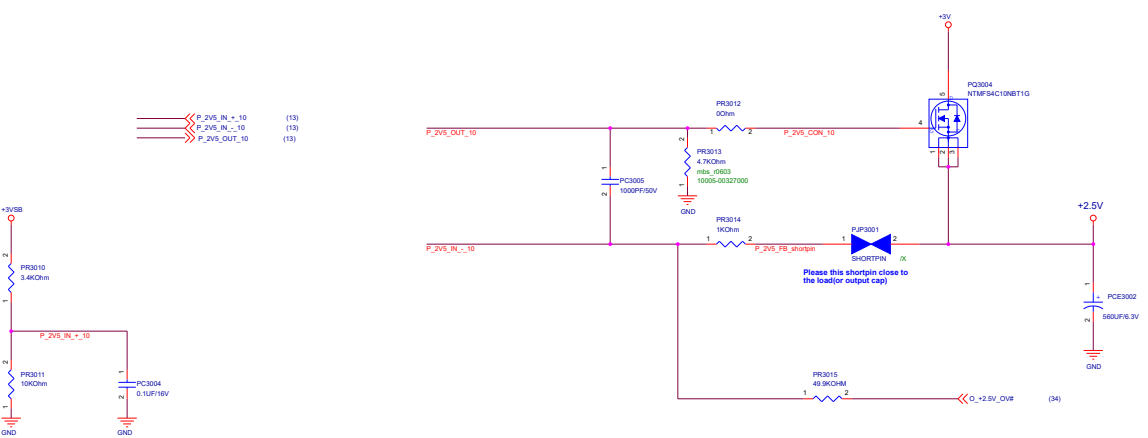
ASUSTek Computer Inc.	Title : VPP_DDR	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 18 of 109	

+1.8VSB===>+1.05V /3A



O_+1.05V_OV#	+1.05V
X	1.05V
0	1.10V

+3V===>+2.5V /2.4A

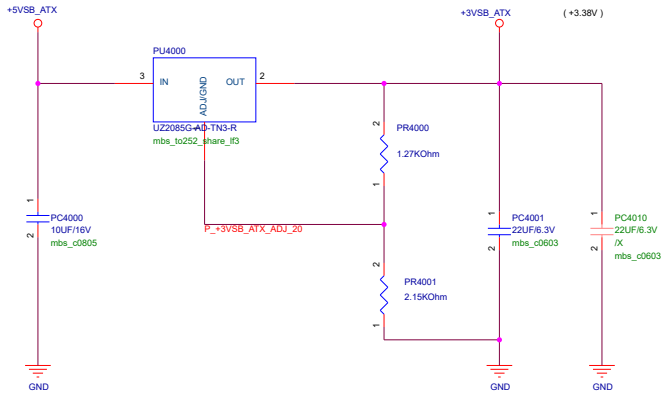


O_+2.5V_OV#	+2.5V
X	2.50V
0	2.55V

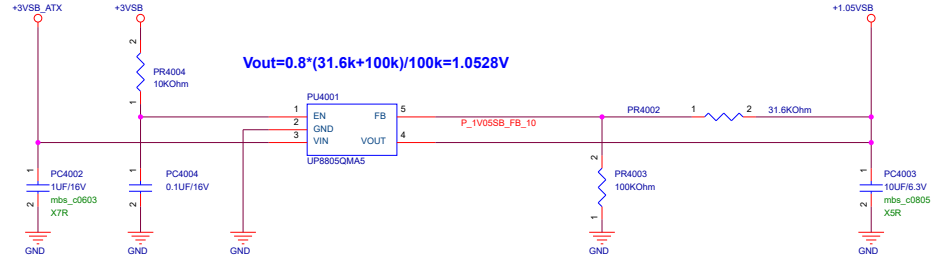
ASUSTek Computer Inc.	Title : +1.05V & +2.5V	
	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 19 of 109	

+5VSB_ATX ====>+3VSB_ATX

Io:1.5A

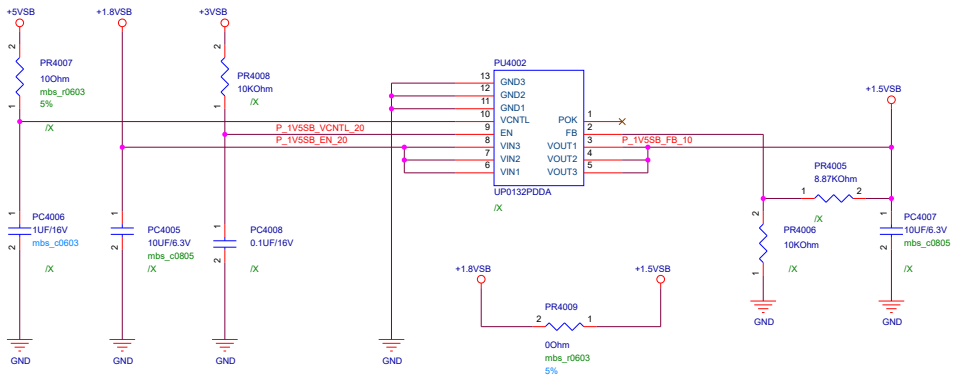


+3VSB_ATX ====>+1.05VSB /50mA



Power Component place near each other!

+1.8VSB==>+1.5VSB /0.75A



ASUSTek Computer Inc.	Title : +3VSB_ATX	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 20 of 109	

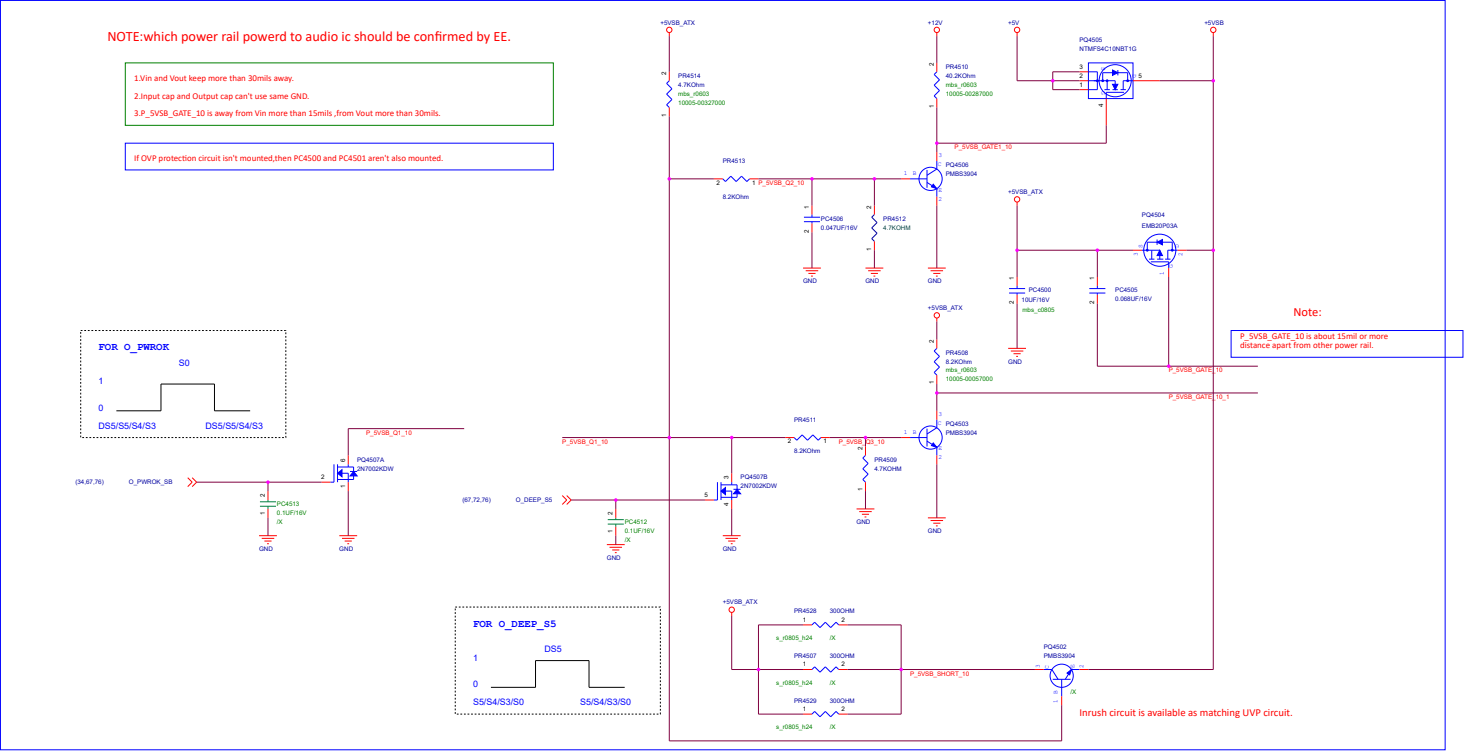
NOTE:which power rail powerd to audio ic should be confirmed by EE.

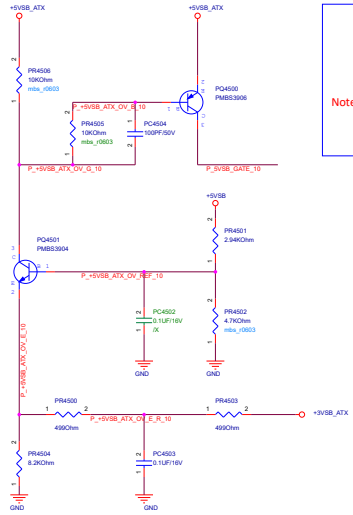
1.Vin and Vout keep more than 30mils away.

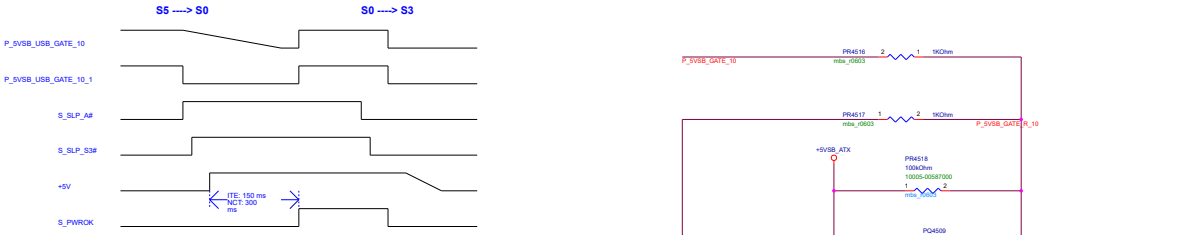
2.Input cap and Output cap can't use same GND.

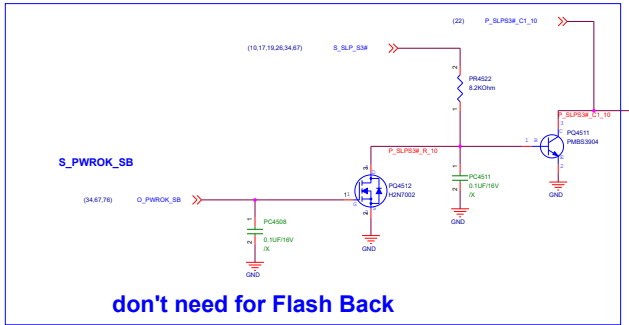
3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

If OVP protection circuit isn't mounted,then PC4500 and PC4501 aren't also mounted.









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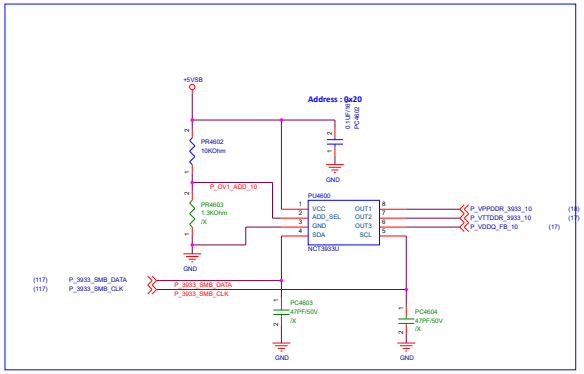


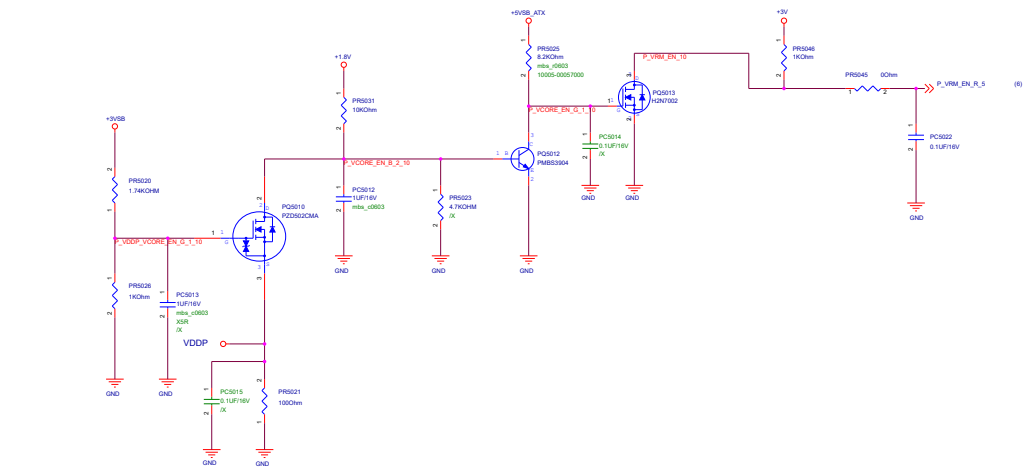
ASUSTeK Computer Inc.

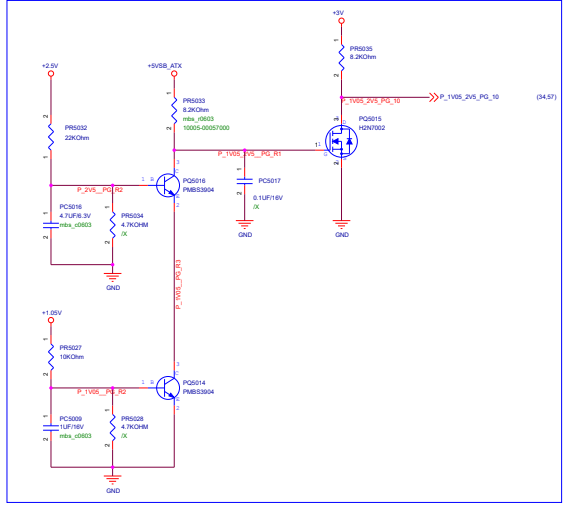
Title : +5VSB&+5VSB Inrush

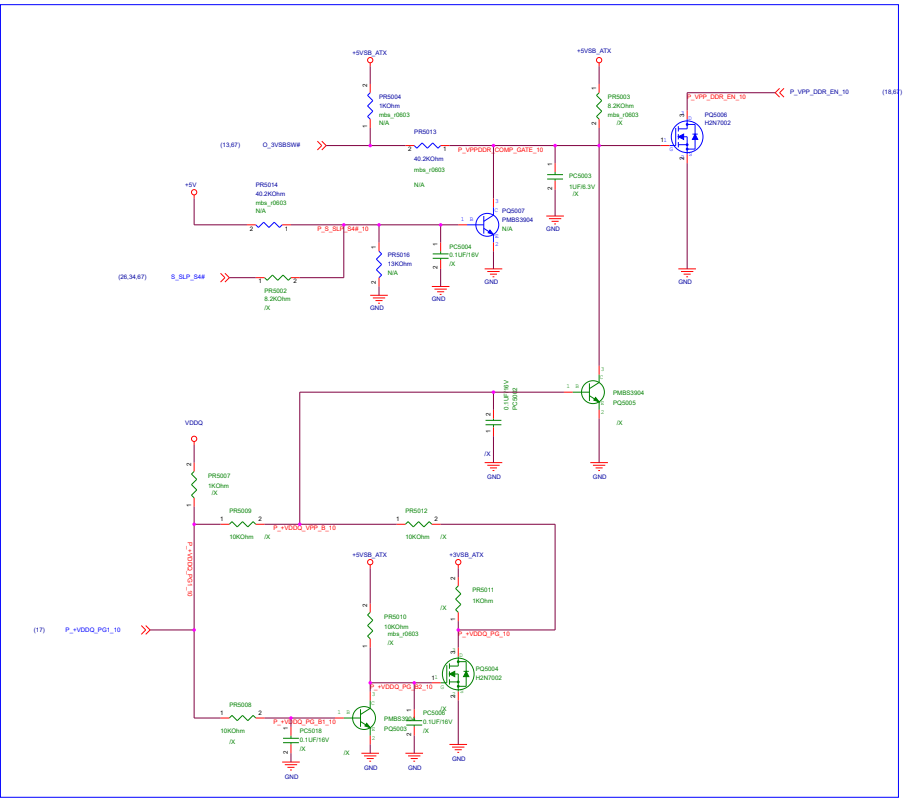
Engineer:

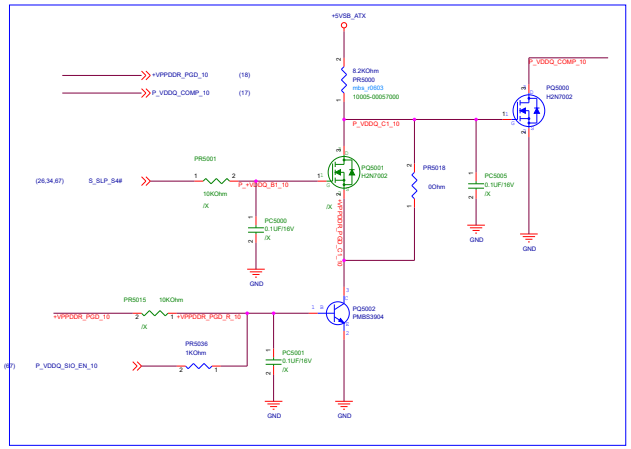
Size	Project Name	Rev
A2	AM4	1.00

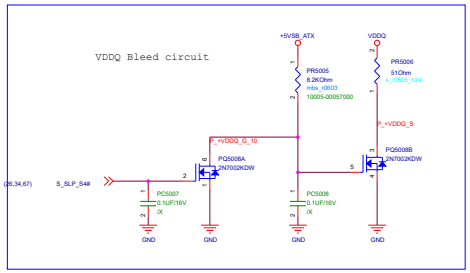
Date: Wednesday, August 29, 2018 Sheet 21 of 189











ASUSTek Computer Inc.	Title :		
	Engineer:		
Size: A2	Project Name:		Rev:
Date: Wednesday, August 29, 2018	Sheet: 23	of: 103	

Title : +3V_OVP

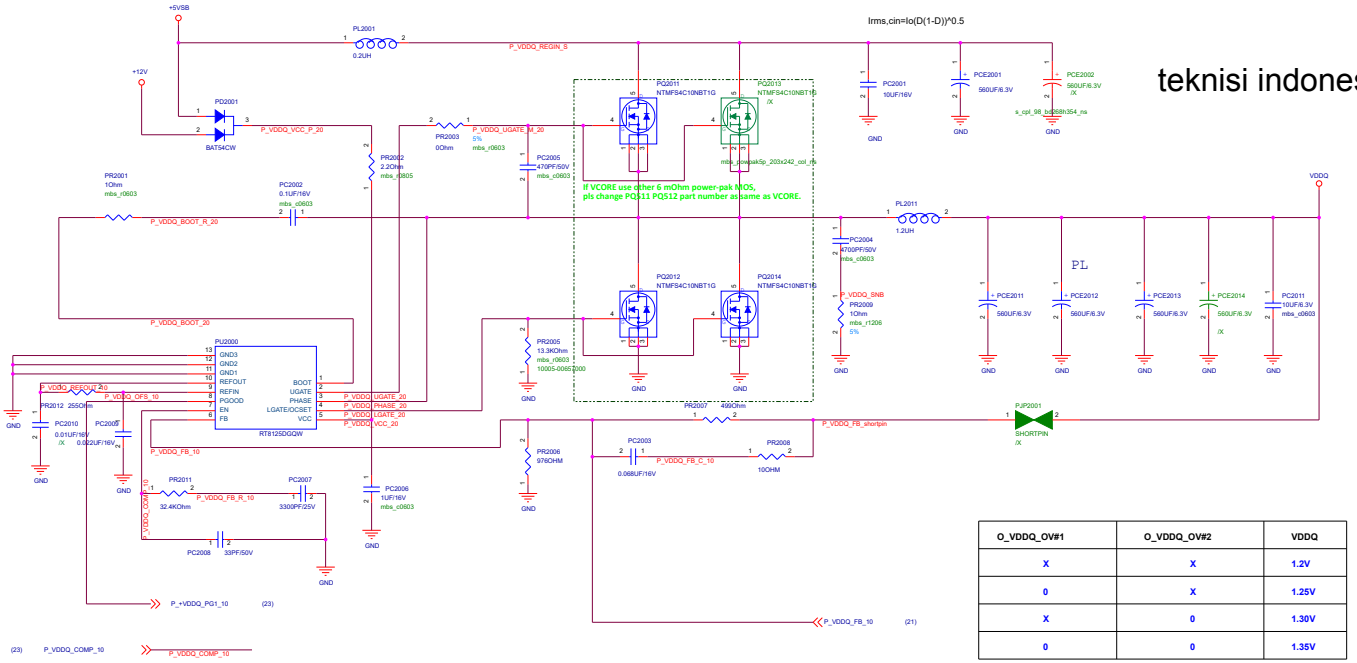
Engineer:

ASUSTek Computer Inc.

Size	Project Name	Rev
A2	FM2 PLUS	1.00

Date:	Wednesday, August 29, 2018	Sheet	24	of	109

+5VSB====>VDDQ Io:16A



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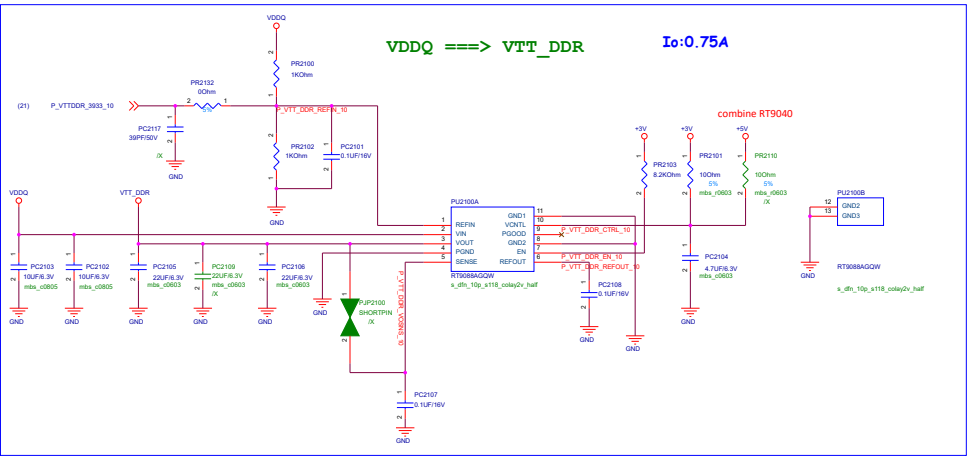
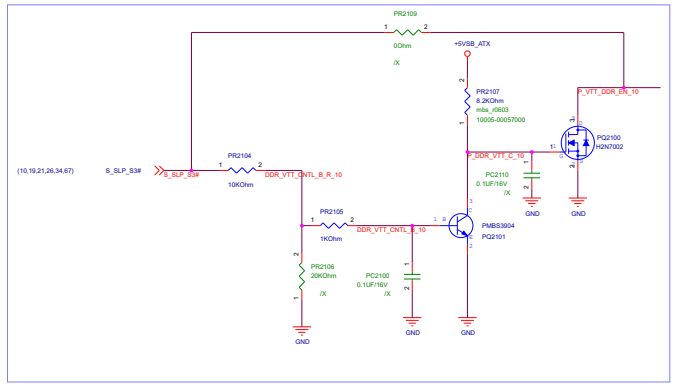
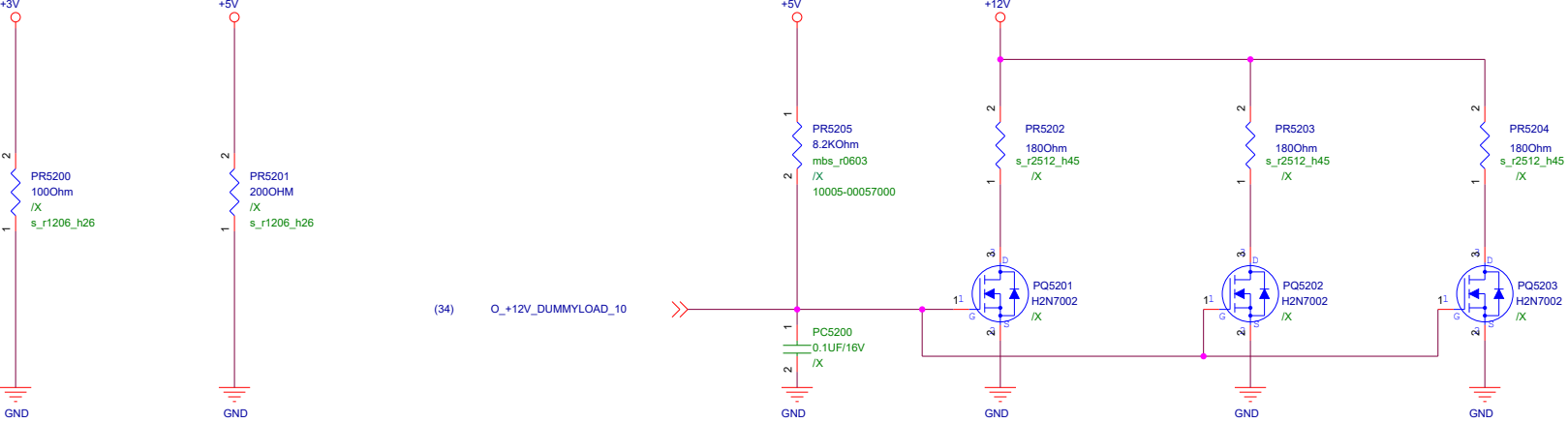
O_VDDQ_OV#1	O_VDDQ_OV#2	VDDQ
X	X	1.2V
0	X	1.25V
X	0	1.30V
0	0	1.35V



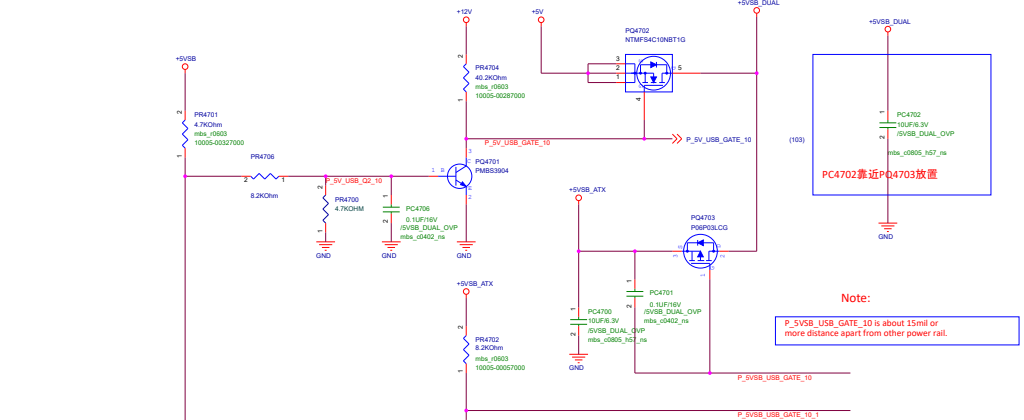


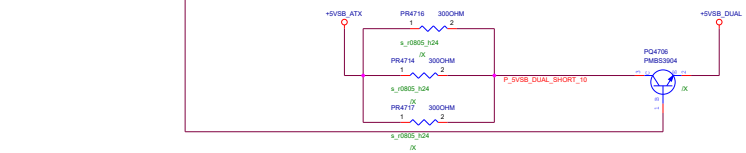
ASUSTek Computer Inc.	Title : VDDQ&VTT_DDR		
	Engineer:		
Size: A2	Project Name: AM4		Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 17 of 109		

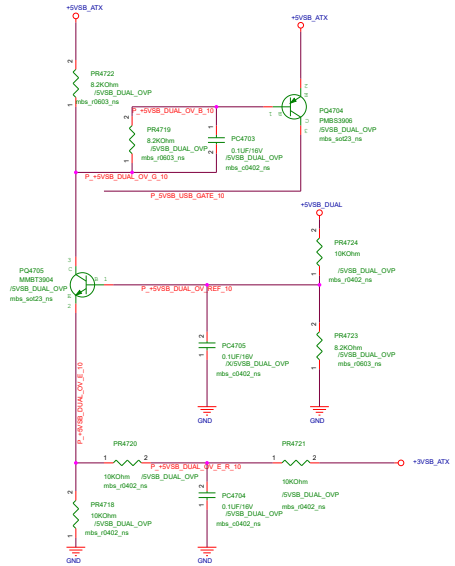


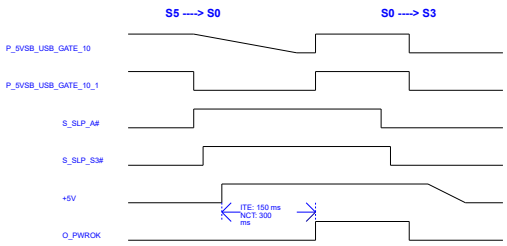
ASUSTek Computer Inc.	Title :	
	Engineer:	
Size: A3	Project Name	Rev
Date: Wednesday, August 29, 2018	Sheet 25 of 109	

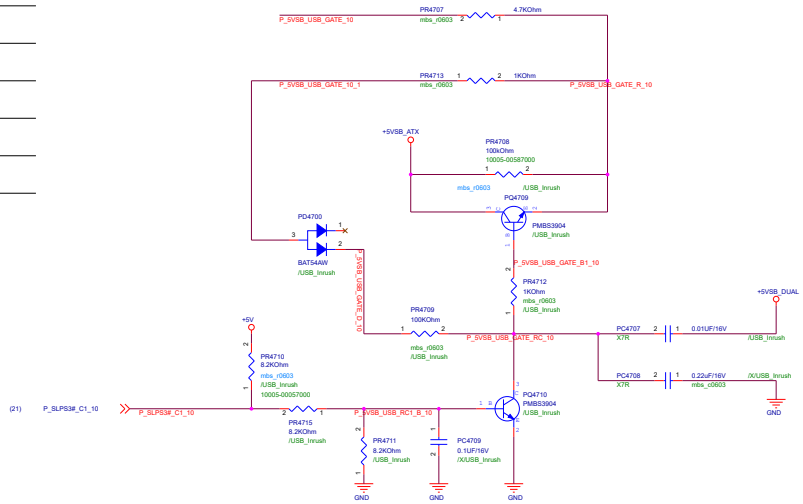
BOM	主板上+5VSB_DUAL 上有接不耐 12V 高壓的元件且上件，例如用在 Type-C 上的 Power Switch G517 06016-01100500	主板上+5VSB_DUAL 上沒有接不耐 12V 高壓的元件或者主板上+5VSB_DUAL 上有接不耐 12V 高壓的元件但不上件
/5VSB_DUAL_OVP	mount	unmount



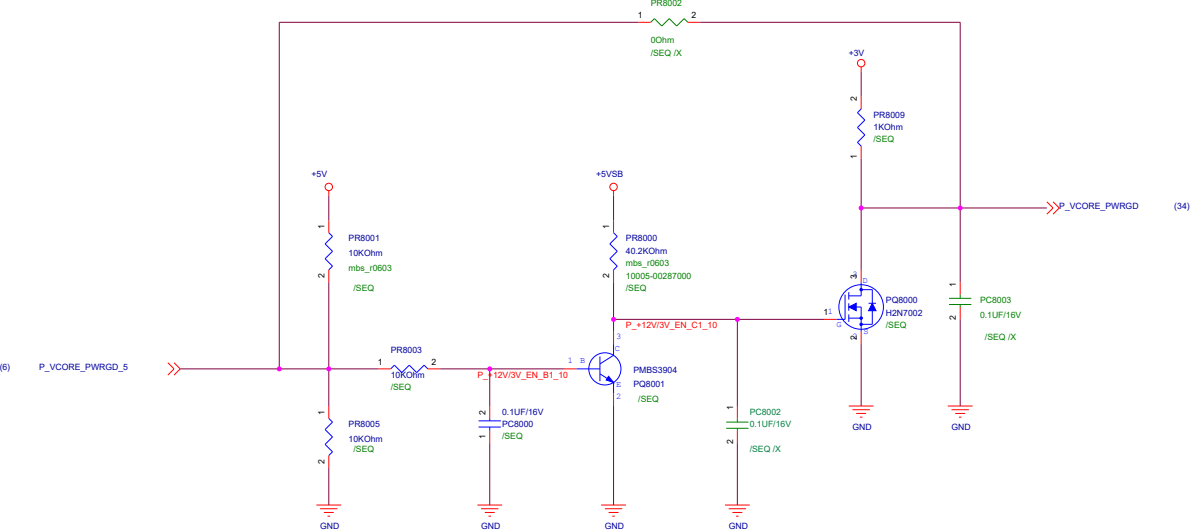




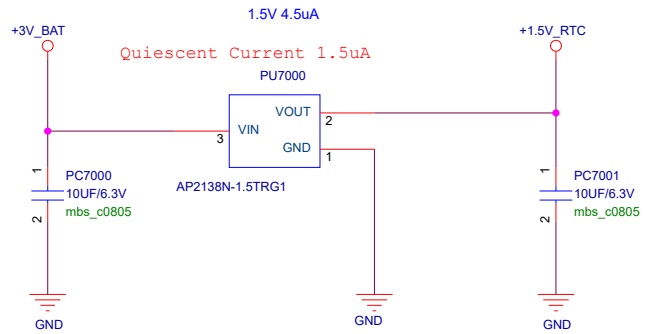




Title :	+5VSB_DUAL		
ASUSTek Computer Inc.	Engineer:		
Size	Project Name		Rev
A2	AM4		1.00
Date:	Wednesday, August 29, 2018	Sheet 22 of 118	



ASUSTek Computer Inc.	Title : VCORE PWRGD Glitch	
	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 28 of 109	



Modify 20170613

ASUSTek Computer Inc.	Title : +1.5V_RTC	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 27 of 109	

Title : NA

Engineer:

ASUSTek Computer Inc.

Size	Project Name	Rev
A3	**AM4**	1.00

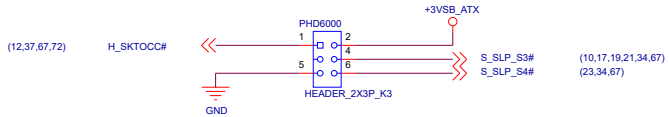
Date:	Wednesday, August 29, 2018	Sheet	30	of	110

Title : NA

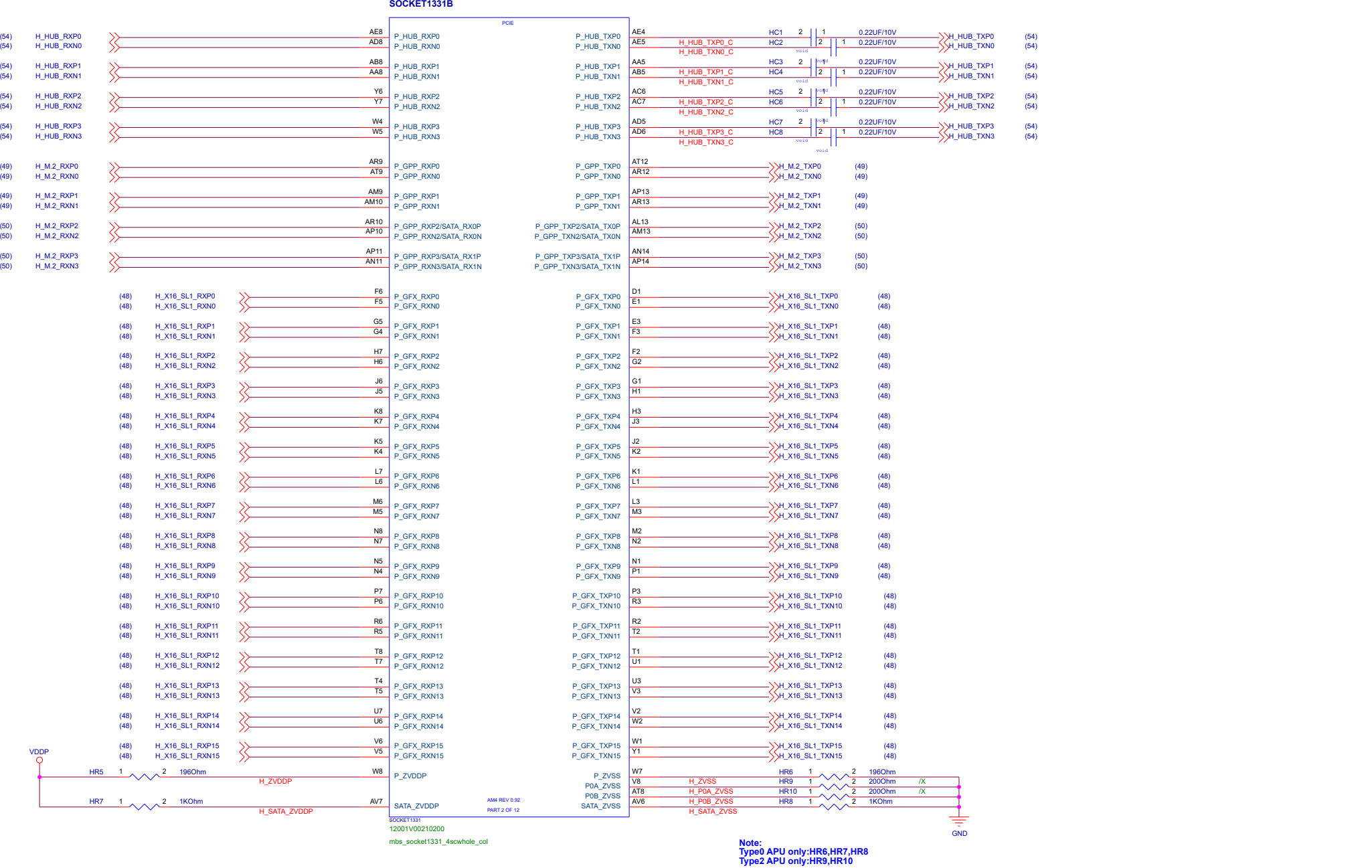
Engineer:

ASUSTek Computer Inc.

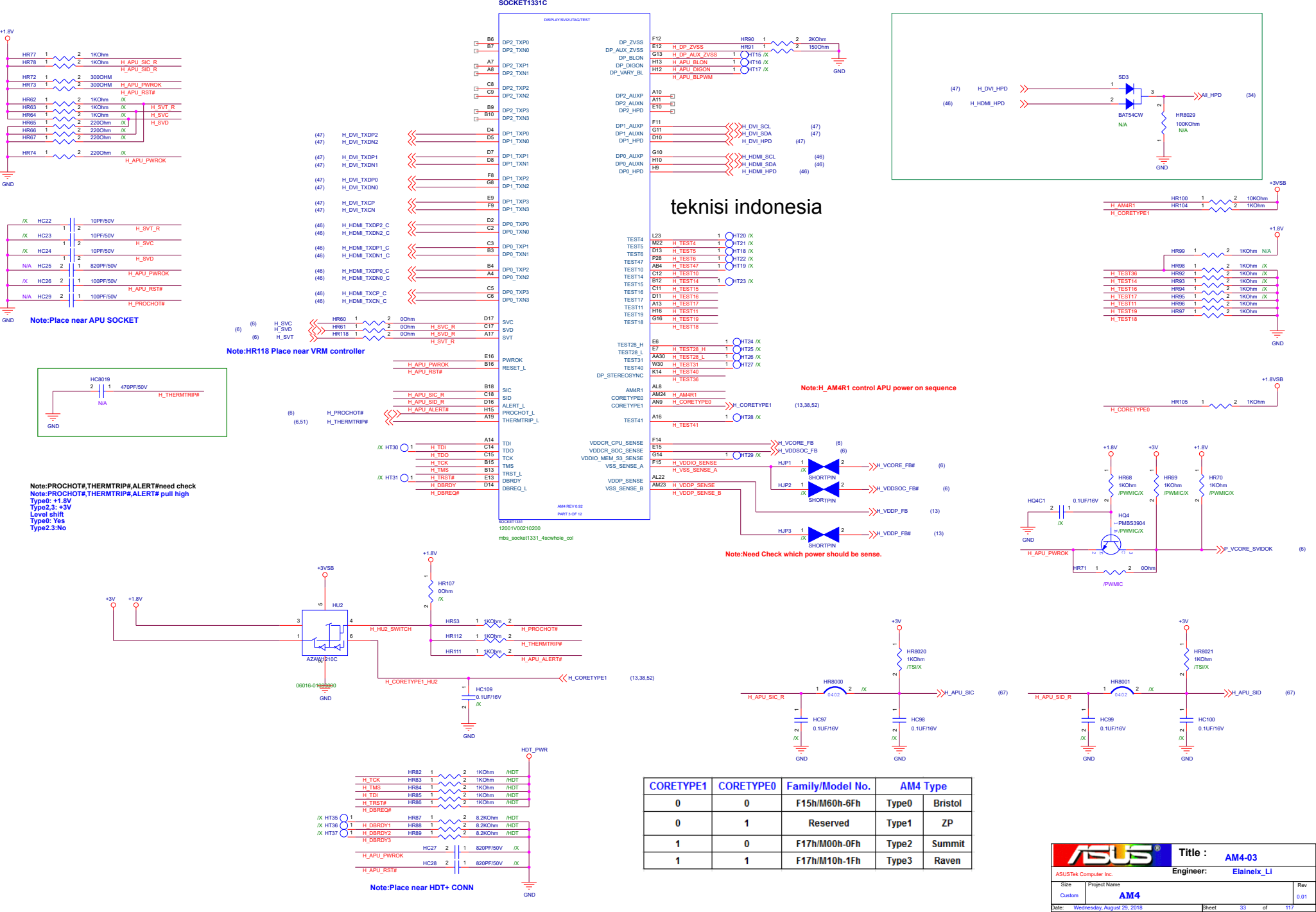
Size	Project Name	Rev
A3	**AM4**	1.00

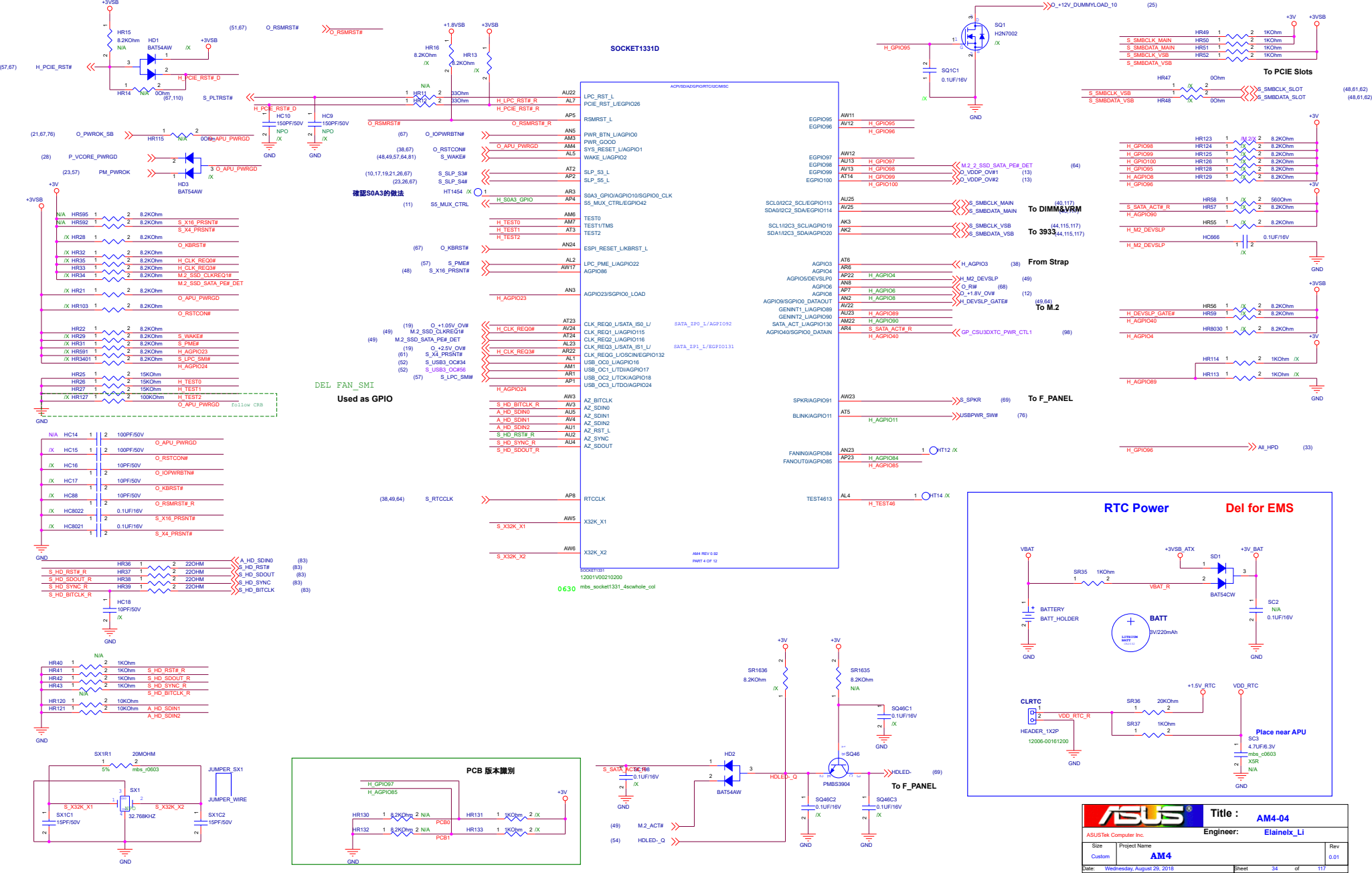


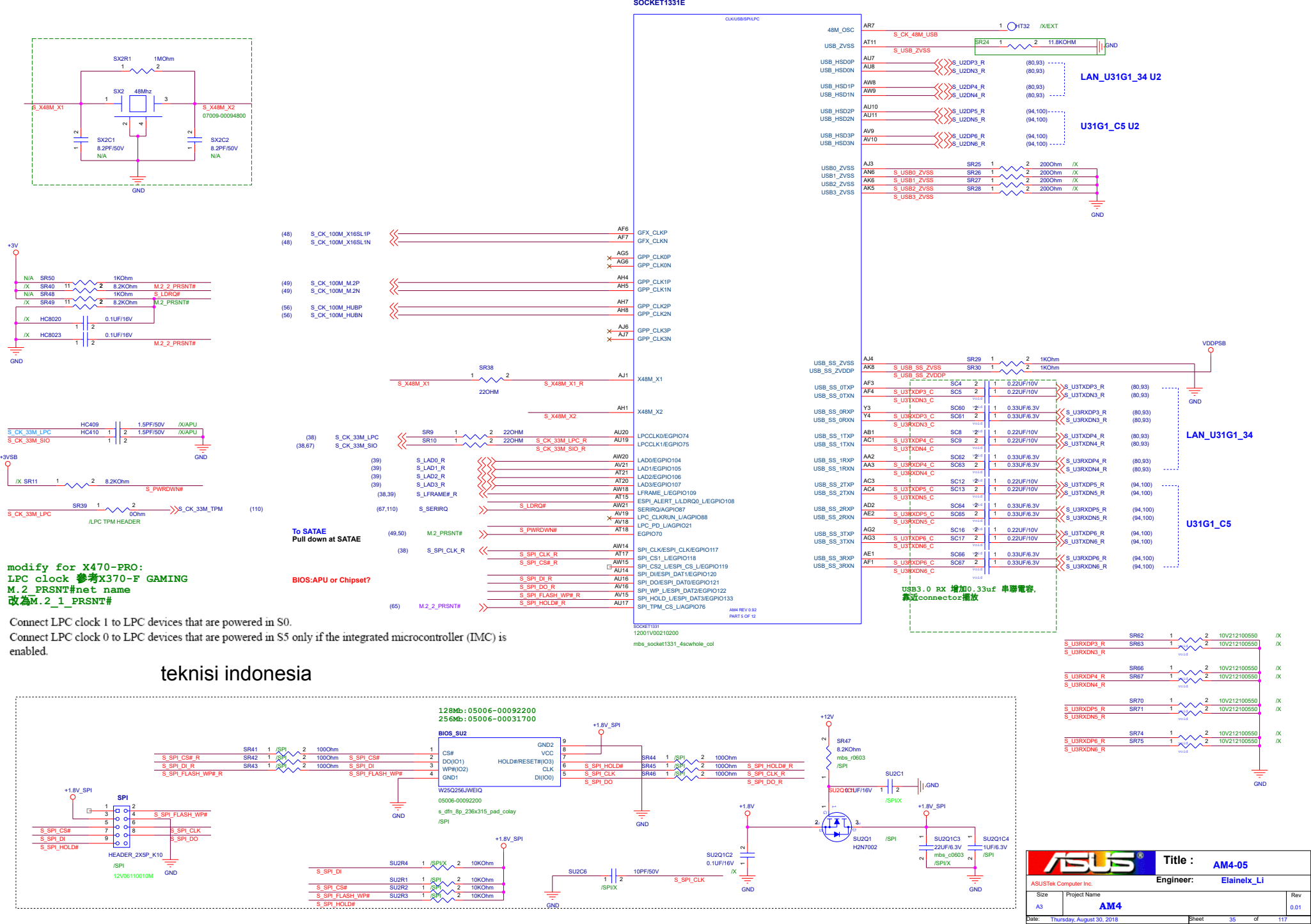
ASUSTek Computer Inc.	Title : NA Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Wednesday, August 29, 2018	Sheet 26 of 109	

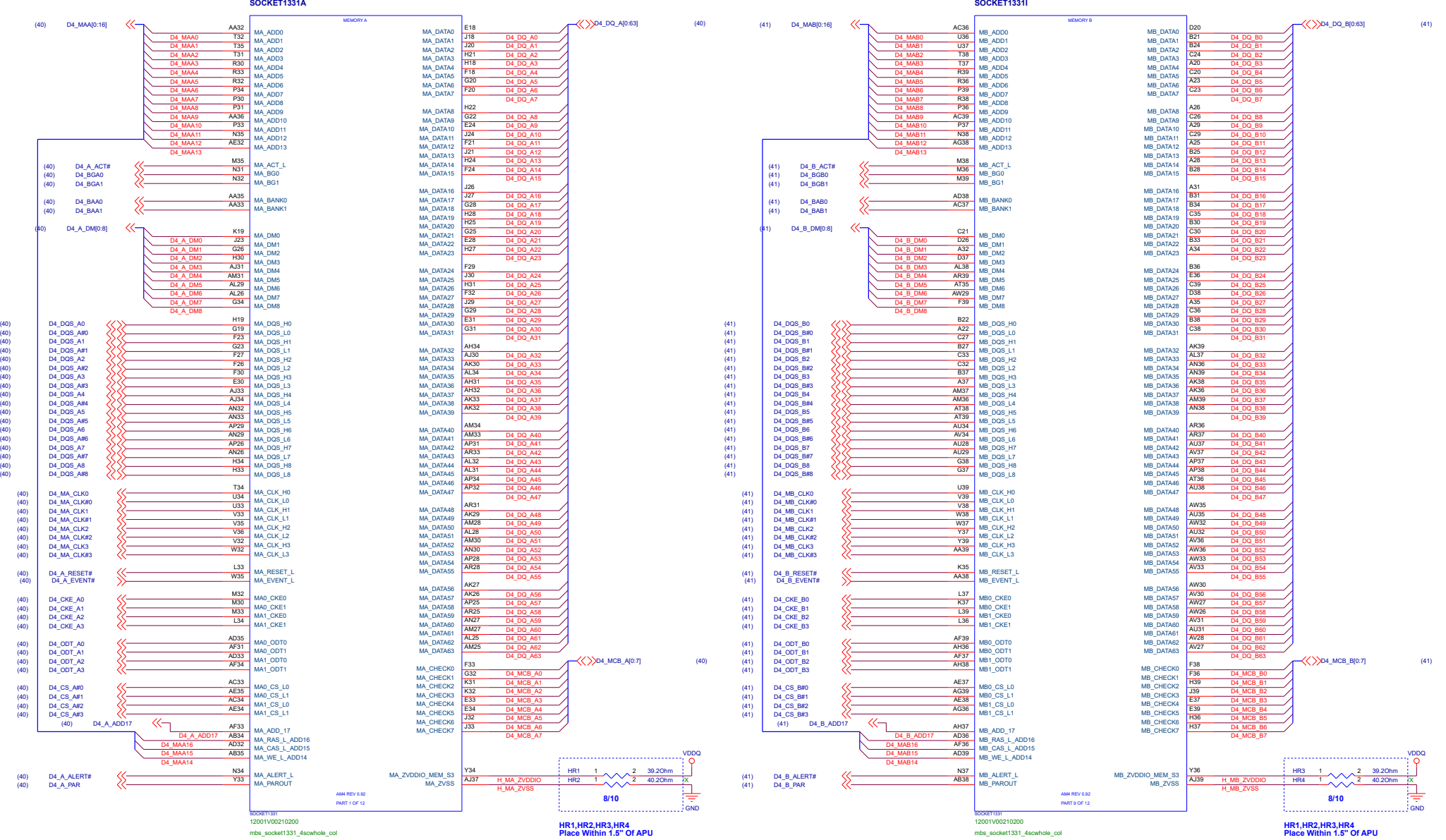


ASUSTek Computer Inc.	Title :	AM4-02	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 32 of 117		


SOCKET1331C
teknisi indonesia
Note:Place near APU SOCKET
Note:HR118 Place near VRM controller
Note:H_AM4R1 control APU power on sequence
Note:Need Check which power should be sense.
Note:PROCHOT#,THERMTRIP#,ALERT#need check
Note:PROCHOT#,THERMTRIP#,ALERT# pull high
Type0: +1.8V
Type2,3: +3V
Level shift
Type0: Yes
Type2.3:No
Note:Place near HDT+ CONN
CORETYPE1 CORETYPE0 Family/Model No. AM4 Type
0 0 F15h/M60h-6Fh Type0 Bristol
0 1 Reserved Type1 ZP
1 0 F17h/M00h-0Fh Type2 Summit
1 1 F17h/M10h-1Fh Type3 Raven
Title : AM4-03
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Project Name AM4
Date: Wednesday, August 29, 2018
Sheet 33 of 117


SOCKET1331D
To PCIE Slots
To DIMM&VRM
To 3933
From Strap
To M.2
To F_PANEL
DEL FAN_SMI
Used as GPIO
確認S0A3的做法
PCB 版本識別
RTC Power
Del for EMS
Place near APU
To F_PANEL
Title : AM4-04
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Project Name AM4
Size Custom
Rev 0.01
Date: Wednesday, August 29, 2018
Sheet 34 of 117


SOCKET1331E
CLK/USB/SPI/LPC
SX2R1 1MOhm
SX2 48Mhz
S_X48M_X1
S_X48M_X2
07009-00094800
SX2C1 8.2PF/50V N/A
SX2C2 8.2PF/50V N/A
GND
48M_OSC
USB_ZVSS
S_CK_48M_USB
S_USB_ZVSS
SR24 11.8KOHM
USB_HSD0P
USB_HSD0N
S_U2DP3_R
S_U2DN3_R
USB_HSD1P
USB_HSD1N
S_U2DP4_R
S_U2DN4_R
USB_HSD2P
USB_HSD2N
S_U2DP5_R
S_U2DN5_R
USB_HSD3P
USB_HSD3N
S_U2DP6_R
S_U2DN6_R
LAN_U31G1_34 U2
U31G1_C5 U2
USB0_ZVSS
USB1_ZVSS
USB2_ZVSS
USB3_ZVSS
S_USB0_ZVSS
S_USB1_ZVSS
S_USB2_ZVSS
S_USB3_ZVSS
SR25 SR26 SR27 SR28 200Ohm
+3V
SR50 1KOhm
SR40 8.2KOhm M.2_2_PRSNT#
SR48 1KOhm S_LDRQ#
SR49 8.2KOhm M.2_PRSNT#
HC8020 0.1UF/16V
HC8023 0.1UF/16V
M.2_2_PRSNT#
S_CK_100M_X16SL1P
S_CK_100M_X16SL1N
S_CK_100M_M.2P
S_CK_100M_M.2N
S_CK_100M_HUBP
S_CK_100M_HUBN
GFX_CLKP
GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
SR38 22OHM
S_X48M_X1
S_X48M_X1_R
X48M_X1
S_X48M_X2
X48M_X2
VDDPSB
USB_SS_ZVSS
USB_SS_ZVDDP
S_USB_SS_ZVSS
S_USB_SS_ZVDDP
SR29 SR30 1KOhm
USB_SS_0TXP
USB_SS_0TXN
USB_SS_0RXP
USB_SS_0RXN
USB_SS_1TXP
USB_SS_1TXN
USB_SS_1RXP
USB_SS_1RXN
USB_SS_2TXP
USB_SS_2TXN
USB_SS_2RXP
USB_SS_2RXN
USB_SS_3TXP
USB_SS_3TXN
USB_SS_3RXP
USB_SS_3RXN
SC4 SC5 SC60 SC61 SC8 SC9 SC62 SC63 SC12 SC13 SC64 SC65 SC16 SC17 SC66 SC67 0.22UF/10V 0.33UF/6.3V
S_U3TXDP3_R
S_U3TXDN3_R
S_U3RXDP3_R
S_U3RXDN3_R
S_U3TXDP4_R
S_U3TXDN4_R
S_U3RXDP4_R
S_U3RXDN4_R
S_U3TXDP5_R
S_U3TXDN5_R
S_U3RXDP5_R
S_U3RXDN5_R
S_U3TXDP6_R
S_U3TXDN6_R
S_U3RXDP6_R
S_U3RXDN6_R
LAN_U31G1_34
U31G1_C5
USB3.0 RX 增加0.33uf 串聯電容,
靠近connector擺放
HC409 HC410 1.5PF/50V /X/APU
S_CK_33M_LPC
S_CK_33M_SIO
+3VSB
SR11 8.2KOhm
S_PWRDWN#
SR39 0Ohm
S_CK_33M_TPM
/LPC TPM HEADER
SR9 SR10 22OHM
S_CK_33M_LPC_R
S_CK_33M_SIO_R
LPCCLK0/EGPIO74
LPCCLK1/EGPIO75
S_LAD0_R
S_LAD1_R
S_LAD2_R
S_LAD3_R
S_LFRAME#_R
S_SERIRQ
S_LDRQ#
S_PWRDWN#
S_SPI_CLK_R
S_SPI_CS#_R
S_SPI_DI_R
S_SPI_DO_R
S_SPI_FLASH_WP#_R
S_SPI_HOLD#_R
LAD0/EGPIO104
LAD1/EGPIO105
LAD2/EGPIO106
LAD3/EGPIO107
LFRAME_L/EGPIO109
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SERIRQ/AGPIO87
LPC_CLKRUN_L/AGPIO88
LPC_PD_L/AGPIO21
EGPIO70
SPI_CLK/ESPI_CLK/EGPIO117
SPI_CS1_L/EGPIO118
SPI_CS2_L/ESPI_CS_L/EGPIO119
SPI_DI/ESPI_DAT1/EGPIO120
SPI_DO/ESPI_DAT0/EGPIO121
SPI_WP_L/ESPI_DAT2/EGPIO122
SPI_HOLD_L/ESPI_DAT3/EGPIO133
SPI_TPM_CS_L/AGPIO76
AM4 REV 0.02
PART 5 OF 12
SOCKET1331
120015V00210200
mbs_socket1331_4scwhole_col
To SATAE
Pull down at SATAE
BIOS:APU or Chipset?
M.2_PRSNT#
M.2_2_PRSNT#
modify for X470-PRO:
LPC clock 參考X370-F GAMING
M.2_PRSNT#net name
改為M.2_1_PRSNT#
Connect LPC clock 1 to LPC devices that are powered in S0.
Connect LPC clock 0 to LPC devices that are powered in S5 only if the integrated microcontroller (IMC) is enabled.
teknisi indonesia
128Mb:05006-00092200
256Mb:05006-00031700
BIOS_SU2
CS#
DO(IO1)
WP#(IO2)
GND1
VCC
HOLD#/RESET#(IO3)
CLK
DI(IO0)
GND2
W25Q256JWEIQ
05006-00092200
s_dfn_8p_236x315_pad_colay
/SPI
SR41 SR42 SR43 100Ohm
SR44 SR45 SR46 100Ohm
+1.8V_SPI
+12V
SR47 8.2KOhm mbs_r0603 /SPI
SU2C1 0.1UF/16V /SPI/X
SU2Q1 H2N7002
SU2Q1C2 0.1UF/16V /X
SU2Q1C3 22UF/6.3V mbs_c0603 /SPI/X
SU2Q1C4 1UF/6.3V /SPI
SU2C6 10PF/50V /SPI/X
SU2R4 SU2R1 SU2R2 SU2R3 10KOhm
SPI
HEADER_2X5P_K10
12V06110010M
SR62 SR63 SR66 SR67 SR70 SR71 SR74 SR75 10V212100550
Title : AM4-05
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Size A3
Project Name AM4
Rev 0.01
Date: Thursday, August 30, 2018
Sheet 35 of 117



Note:
Type0 APU only:HR1,HR3

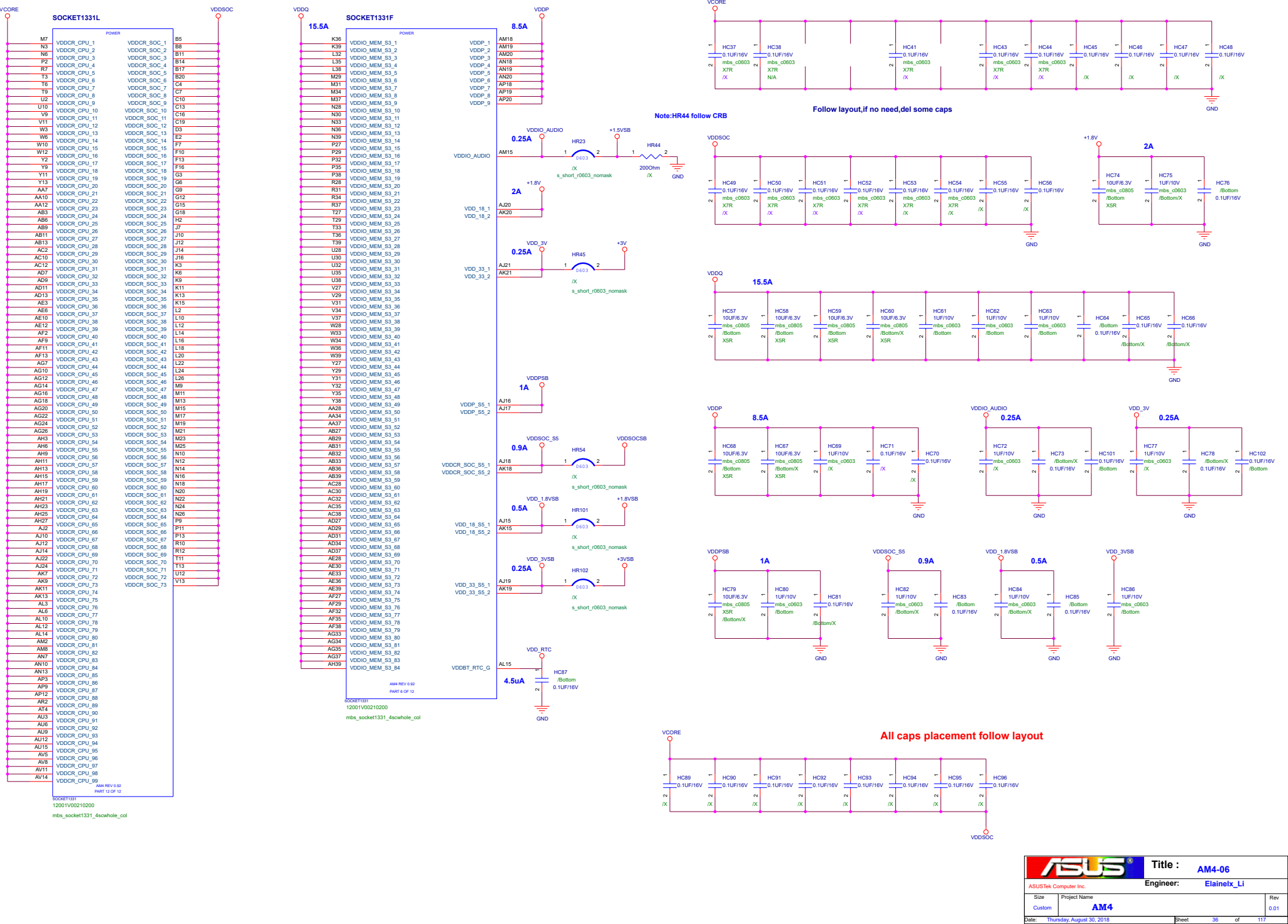
ASUSTek Computer Inc.

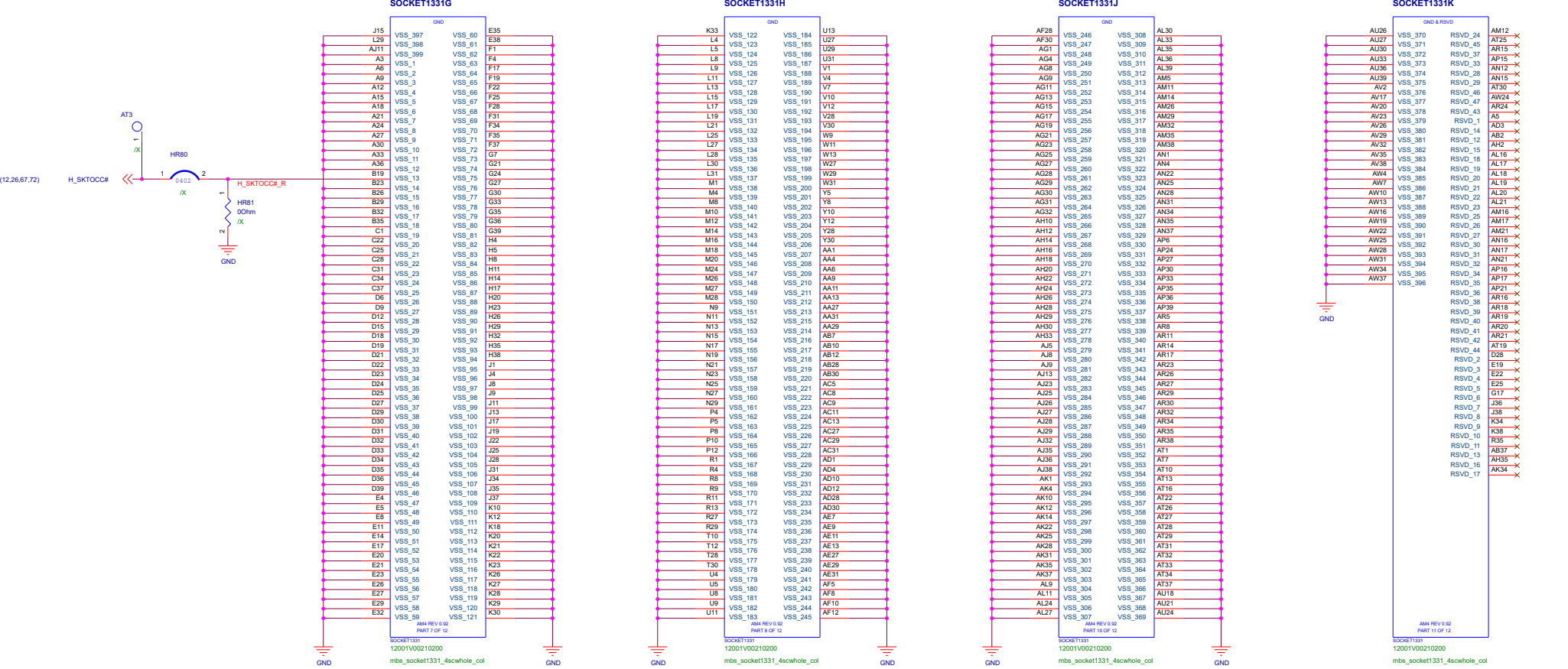
Title : AM4-01

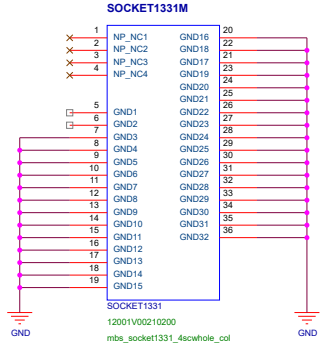
Engineer: Elainelx_Li

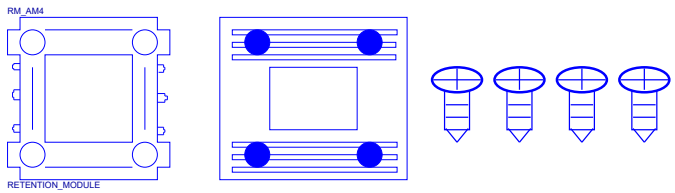
Size	Project Name	Rev
A3	AM4	0.01

Date: Wednesday, August 29, 2018 Sheet 31 of 117

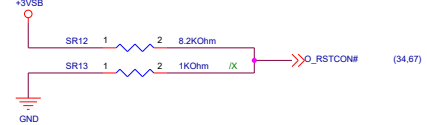

SOCKET1331L
POWER
VCORE
VDDSOC
M7 VDDCR_CPU_1
N3 VDDCR_CPU_2
N6 VDDCR_CPU_3
P2 VDDCR_CPU_4
R7 VDDCR_CPU_5
T3 VDDCR_CPU_6
T6 VDDCR_CPU_7
T9 VDDCR_CPU_8
U2 VDDCR_CPU_9
U10 VDDCR_CPU_10
V9 VDDCR_CPU_11
V11 VDDCR_CPU_12
W3 VDDCR_CPU_13
W6 VDDCR_CPU_14
W10 VDDCR_CPU_15
W12 VDDCR_CPU_16
Y2 VDDCR_CPU_17
Y9 VDDCR_CPU_18
Y11 VDDCR_CPU_19
Y13 VDDCR_CPU_20
AA7 VDDCR_CPU_21
AA10 VDDCR_CPU_22
AA12 VDDCR_CPU_23
AB3 VDDCR_CPU_24
AB6 VDDCR_CPU_25
AB9 VDDCR_CPU_26
AB11 VDDCR_CPU_27
AB13 VDDCR_CPU_28
AC2 VDDCR_CPU_29
AC10 VDDCR_CPU_30
AC12 VDDCR_CPU_31
AD7 VDDCR_CPU_32
AD9 VDDCR_CPU_33
AD11 VDDCR_CPU_34
AD13 VDDCR_CPU_35
AE3 VDDCR_CPU_36
AE6 VDDCR_CPU_37
AE10 VDDCR_CPU_38
AE12 VDDCR_CPU_39
AF2 VDDCR_CPU_40
AF9 VDDCR_CPU_41
AF11 VDDCR_CPU_42
AF13 VDDCR_CPU_43
AG7 VDDCR_CPU_44
AG10 VDDCR_CPU_45
AG12 VDDCR_CPU_46
AG14 VDDCR_CPU_47
AG16 VDDCR_CPU_48
AG18 VDDCR_CPU_49
AG20 VDDCR_CPU_50
AG22 VDDCR_CPU_51
AG24 VDDCR_CPU_52
AG26 VDDCR_CPU_53
AH3 VDDCR_CPU_54
AH6 VDDCR_CPU_55
AH9 VDDCR_CPU_56
AH11 VDDCR_CPU_57
AH13 VDDCR_CPU_58
AH15 VDDCR_CPU_59
AH17 VDDCR_CPU_60
AH19 VDDCR_CPU_61
AH21 VDDCR_CPU_62
AH23 VDDCR_CPU_63
AH25 VDDCR_CPU_64
AH27 VDDCR_CPU_65
AJ2 VDDCR_CPU_66
AJ10 VDDCR_CPU_67
AJ12 VDDCR_CPU_68
AJ14 VDDCR_CPU_69
AJ22 VDDCR_CPU_70
AJ24 VDDCR_CPU_71
AK7 VDDCR_CPU_72
AK9 VDDCR_CPU_73
AK11 VDDCR_CPU_74
AK13 VDDCR_CPU_75
AL3 VDDCR_CPU_76
AL6 VDDCR_CPU_77
AL10 VDDCR_CPU_78
AL12 VDDCR_CPU_79
AL14 VDDCR_CPU_80
AM2 VDDCR_CPU_81
AM6 VDDCR_CPU_82
AN7 VDDCR_CPU_83
AN10 VDDCR_CPU_84
AN13 VDDCR_CPU_85
AP3 VDDCR_CPU_86
AP9 VDDCR_CPU_87
AP12 VDDCR_CPU_88
AR2 VDDCR_CPU_89
AT4 VDDCR_CPU_90
AU3 VDDCR_CPU_91
AU6 VDDCR_CPU_92
AU9 VDDCR_CPU_93
AU12 VDDCR_CPU_94
AU15 VDDCR_CPU_95
AV5 VDDCR_CPU_96
AV8 VDDCR_CPU_97
AV11 VDDCR_CPU_98
AV14 VDDCR_CPU_99
VDDCR_SOC_1 B5
VDDCR_SOC_2 B8
VDDCR_SOC_3 B11
VDDCR_SOC_4 B14
VDDCR_SOC_5 B17
VDDCR_SOC_6 B20
VDDCR_SOC_7 C4
VDDCR_SOC_8 C7
VDDCR_SOC_9 C10
VDDCR_SOC_10 C13
VDDCR_SOC_11 C16
VDDCR_SOC_12 C19
VDDCR_SOC_13 D3
VDDCR_SOC_14 E2
VDDCR_SOC_15 F7
VDDCR_SOC_16 F10
VDDCR_SOC_17 F13
VDDCR_SOC_18 F16
VDDCR_SOC_19 G3
VDDCR_SOC_20 G6
VDDCR_SOC_21 G9
VDDCR_SOC_22 G12
VDDCR_SOC_23 G15
VDDCR_SOC_24 G18
VDDCR_SOC_25 H2
VDDCR_SOC_26 J7
VDDCR_SOC_27 J10
VDDCR_SOC_28 J12
VDDCR_SOC_29 J14
VDDCR_SOC_30 J16
VDDCR_SOC_31 K3
VDDCR_SOC_32 K6
VDDCR_SOC_33 K9
VDDCR_SOC_34 K11
VDDCR_SOC_35 K13
VDDCR_SOC_36 K15
VDDCR_SOC_37 L2
VDDCR_SOC_38 L10
VDDCR_SOC_39 L12
VDDCR_SOC_40 L14
VDDCR_SOC_41 L16
VDDCR_SOC_42 L18
VDDCR_SOC_43 L20
VDDCR_SOC_44 L22
VDDCR_SOC_45 L24
VDDCR_SOC_46 L26
VDDCR_SOC_47 M9
VDDCR_SOC_48 M11
VDDCR_SOC_49 M13
VDDCR_SOC_50 M15
VDDCR_SOC_51 M17
VDDCR_SOC_52 M19
VDDCR_SOC_53 M21
VDDCR_SOC_54 M23
VDDCR_SOC_55 M25
VDDCR_SOC_56 N10
VDDCR_SOC_57 N12
VDDCR_SOC_58 N14
VDDCR_SOC_59 N16
VDDCR_SOC_60 N18
VDDCR_SOC_61 N20
VDDCR_SOC_62 N22
VDDCR_SOC_63 N24
VDDCR_SOC_64 N26
VDDCR_SOC_65 P9
VDDCR_SOC_66 P11
VDDCR_SOC_67 P13
VDDCR_SOC_68 R10
VDDCR_SOC_69 R12
VDDCR_SOC_70 T11
VDDCR_SOC_71 T13
VDDCR_SOC_72 U12
VDDCR_SOC_73 V13
AM4 REV 0.92
PART 12 OF 12
SOCKET1331
12001V00210200
mbs_socket1331_4scwhole_col
VDDQ
15.5A
SOCKET1331F
POWER
K36 VDDIO_MEM_S3_1
K39 VDDIO_MEM_S3_2
L32 VDDIO_MEM_S3_3
L35 VDDIO_MEM_S3_4
L38 VDDIO_MEM_S3_5
M29 VDDIO_MEM_S3_6
M31 VDDIO_MEM_S3_7
M34 VDDIO_MEM_S3_8
M37 VDDIO_MEM_S3_9
N28 VDDIO_MEM_S3_10
N30 VDDIO_MEM_S3_11
N33 VDDIO_MEM_S3_12
N36 VDDIO_MEM_S3_13
N39 VDDIO_MEM_S3_14
P27 VDDIO_MEM_S3_15
P29 VDDIO_MEM_S3_16
P32 VDDIO_MEM_S3_17
P35 VDDIO_MEM_S3_18
P38 VDDIO_MEM_S3_19
R28 VDDIO_MEM_S3_20
R31 VDDIO_MEM_S3_21
R34 VDDIO_MEM_S3_22
R37 VDDIO_MEM_S3_23
T27 VDDIO_MEM_S3_24
T29 VDDIO_MEM_S3_25
T33 VDDIO_MEM_S3_26
T36 VDDIO_MEM_S3_27
T39 VDDIO_MEM_S3_28
U28 VDDIO_MEM_S3_29
U30 VDDIO_MEM_S3_30
U32 VDDIO_MEM_S3_31
U35 VDDIO_MEM_S3_32
U38 VDDIO_MEM_S3_33
V27 VDDIO_MEM_S3_34
V29 VDDIO_MEM_S3_35
V31 VDDIO_MEM_S3_36
V34 VDDIO_MEM_S3_37
V37 VDDIO_MEM_S3_38
W28 VDDIO_MEM_S3_39
W33 VDDIO_MEM_S3_40
W34 VDDIO_MEM_S3_41
W36 VDDIO_MEM_S3_42
W39 VDDIO_MEM_S3_43
Y27 VDDIO_MEM_S3_44
Y29 VDDIO_MEM_S3_45
Y31 VDDIO_MEM_S3_46
Y32 VDDIO_MEM_S3_47
Y35 VDDIO_MEM_S3_48
Y38 VDDIO_MEM_S3_49
AA28 VDDIO_MEM_S3_50
AA34 VDDIO_MEM_S3_51
AA37 VDDIO_MEM_S3_52
AB27 VDDIO_MEM_S3_53
AB29 VDDIO_MEM_S3_54
AB31 VDDIO_MEM_S3_55
AB32 VDDIO_MEM_S3_56
AB33 VDDIO_MEM_S3_57
AB36 VDDIO_MEM_S3_58
AB39 VDDIO_MEM_S3_59
AC28 VDDIO_MEM_S3_60
AC30 VDDIO_MEM_S3_61
AC32 VDDIO_MEM_S3_62
AC35 VDDIO_MEM_S3_63
AC38 VDDIO_MEM_S3_64
AD27 VDDIO_MEM_S3_65
AD29 VDDIO_MEM_S3_66
AD31 VDDIO_MEM_S3_67
AD34 VDDIO_MEM_S3_68
AD37 VDDIO_MEM_S3_69
AE28 VDDIO_MEM_S3_70
AE30 VDDIO_MEM_S3_71
AE33 VDDIO_MEM_S3_72
AE36 VDDIO_MEM_S3_73
AE39 VDDIO_MEM_S3_74
AF27 VDDIO_MEM_S3_75
AF29 VDDIO_MEM_S3_76
AF32 VDDIO_MEM_S3_77
AF35 VDDIO_MEM_S3_78
AF38 VDDIO_MEM_S3_79
AG33 VDDIO_MEM_S3_80
AG34 VDDIO_MEM_S3_81
AG35 VDDIO_MEM_S3_82
AG37 VDDIO_MEM_S3_83
AH39 VDDIO_MEM_S3_84
VDDP_1 AM18
VDDP_2 AM19
VDDP_3 AM20
VDDP_4 AN18
VDDP_5 AN19
VDDP_6 AN20
VDDP_7 AP18
VDDP_8 AP19
VDDP_9 AP20
AM4 REV 0.92
PART 6 OF 12
SOCKET1331
12001V00210200
mbs_socket1331_4scwhole_col
VDDP
8.5A
VDDIO_AUDIO
0.25A
AM15
HR23
0603
/X
s_short_r0603_nomask
+1.5VSB
HR44
200Ohm
/X
GND
VDD_18_1
VDD_18_2
+1.8V
2A
AJ20
AK20
VDD_3V
0.25A
AJ21
AK21
HR45
+3V
VDD_33_1
VDD_33_2
VDDPSB
1A
AJ16
AJ17
VDDP_S5_1
VDDP_S5_2
VDDSOC_S5
0.9A
AJ18
AK18
HR54
VDDSOCSB
VDDCR_SOC_S5_1
VDDCR_SOC_S5_2
VDD_1.8VSB
0.5A
AJ15
AK15
HR101
+1.8VSB
VDD_18_S5_1
VDD_18_S5_2
VDD_3VSB
0.25A
AJ19
AK19
HR102
+3VSB
VDD_33_S5_1
VDD_33_S5_2
VDD_RTC
AL15
VDDBT_RTC_G
4.5uA
HC87
/Bottom
0.1UF/16V
GND
Note:HR44 follow CRB
VCORE
HC37 HC38 HC41 HC43 HC44 HC45 HC46 HC47 HC48
0.1UF/16V
mbs_c0603
X7R
/X
N/A
GND
Follow layout,if no need,del some caps
VDDSOC
HC49 HC50 HC51 HC52 HC53 HC54 HC55 HC56
0.1UF/16V
mbs_c0603
X7R
/X
+1.8V
2A
HC74
10UF/6.3V
mbs_c0805
/Bottom
X5R
HC75
1UF/10V
mbs_c0603
/Bottom/X
HC76
/Bottom
0.1UF/16V
VDDQ
15.5A
HC57 HC58 HC59 HC60 HC61 HC62 HC63 HC64 HC65 HC66
10UF/6.3V
mbs_c0805
/Bottom
X5R
1UF/10V
mbs_c0603
/Bottom
0.1UF/16V
/Bottom/X
VDDP
8.5A
HC68 HC67 HC69 HC71 HC70
10UF/6.3V
mbs_c0805
/Bottom
/Bottom/X
X5R
1UF/10V
mbs_c0603
/X
0.1UF/16V
VDDIO_AUDIO
0.25A
HC72 HC73 HC101
1UF/10V
mbs_c0603
/X
/Bottom/X
0.1UF/16V
/Bottom
VDD_3V
0.25A
HC77 HC78 HC102
1UF/10V
mbs_c0603
/X
/Bottom/X
0.1UF/16V
VDDPSB
1A
HC79
10UF/6.3V
mbs_c0805
X5R
/Bottom/X
HC80
1UF/10V
mbs_c0603
/Bottom
HC81
0.1UF/16V
/Bottom/X
VDDSOC_S5
0.9A
HC82
1UF/10V
mbs_c0603
/Bottom/X
HC83
/Bottom
0.1UF/16V
VDD_1.8VSB
0.5A
HC84
1UF/10V
mbs_c0603
/Bottom/X
HC85
/Bottom
0.1UF/16V
VDD_3VSB
HC86
1UF/10V
mbs_c0603
/Bottom
All caps placement follow layout
VCORE
HC89 HC90 HC91 HC92 HC93 HC94 HC95 HC96
0.1UF/16V
/X
VDDSOC
Title : AM4-06
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Size Custom
Project Name AM4
Rev 0.01
Date: Thursday, August 30, 2018
Sheet 36 of 117

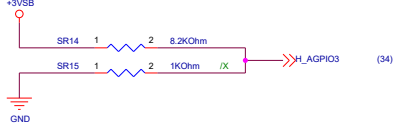


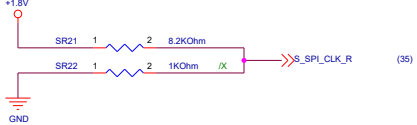


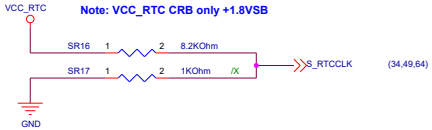


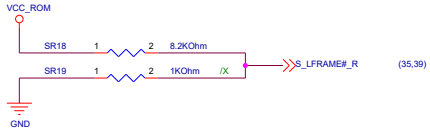
ASUSTek Computer Inc.	Title : AM4-07	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 37 of 117	

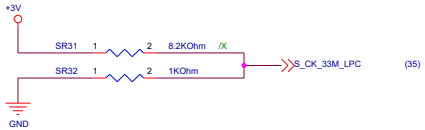


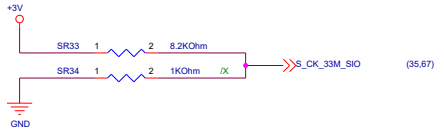






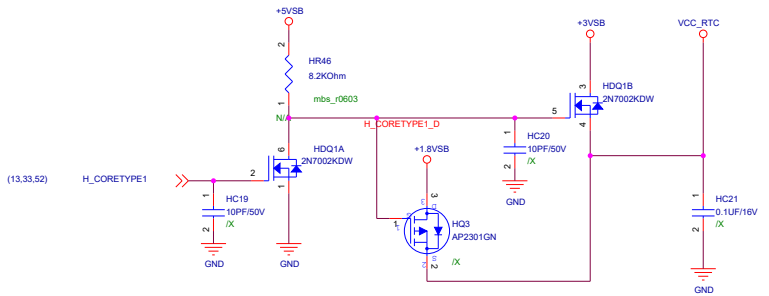


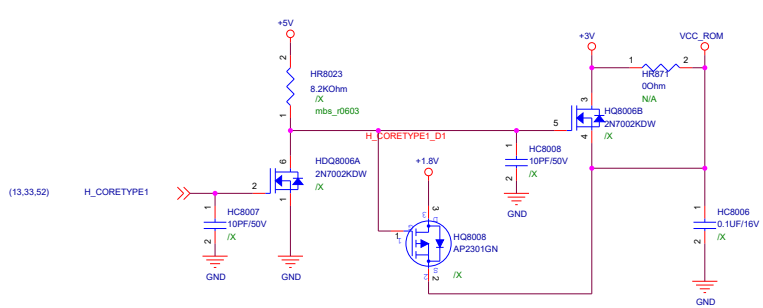




	TYPE0 2	TYPE0	TYPE0	TYPE0		TYPE0	TYPE1 2 3
PIN	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK	SYS_RESET_L	AGPIO3	SPI_CLK(ZP)
NET	S_LFRAME#_R	C_LPC_TPM	C_LPC_SIO_R	S_RTCCLK	O_RSTCON#	H_AGPIO3	S_SPI_CLK
PULL HIGH	SPI ROM Default	48M source and generate both internal andexternal clocks Default	Boot Fail Timer Enabled	Coin Battery is onboard Default	Normal Reset Mode Default	Enhanced Reset logic for faster resume from S5 Default	48M source and generate both internal andexternal clocks Default
PULL LOW	LPC ROM	100M source and generate internal clock only	Boot Fail Timer Disabled Default	Coin Battery is onboard	Short Reset Mode	Traditional Reset logic	100M source and generate internal clock only

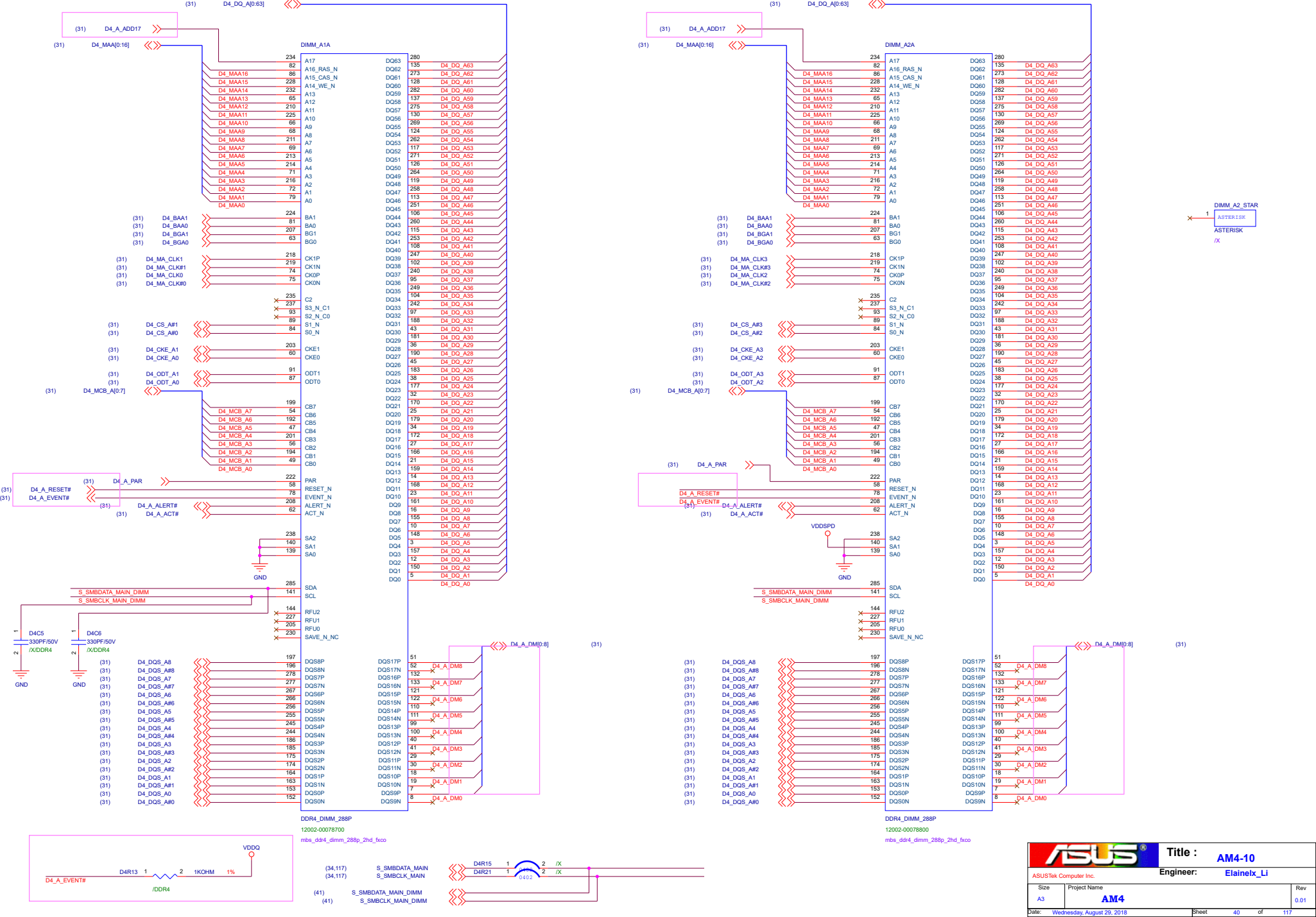
CORETYPE1	CORETYPE0	Family/Model NO.	AM4 Type	
0	0	Family 15h/Models 60h-6Fh	Type 0	Bristol
0	1	Reserved	Reserved	
1	1	Family 17h/Models 20h-2Fh	Type 1	Raven-2
1	0	Family 17h/Models 00h-0Fh	Type 2	Summit/Pinnacle
1	1	Family 17h/Models 10h-1Fh	Type 3	Raven-1





APU TYPE	H_CORETYPE1	VCC_RTC
Type0	0	+3VSB
Type2,3	1	+1.8VSB

ASUSTek Computer Inc.	Title : <Title>	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 38 of 117	


DIMM_A1A
DIMM_A2A
DDR4_DIMM_288P
12002-00078700
12002-00078800
mbs_ddr4_dimm_288p_2hd_fxco
D4_DQ_A[0:63]
D4_A_ADD17
D4_MAA[0:16]
D4_BAA1
D4_BAA0
D4_BGA1
D4_BGA0
D4_MA_CLK1
D4_MA_CLK#1
D4_MA_CLK0
D4_MA_CLK#0
D4_MA_CLK3
D4_MA_CLK#3
D4_MA_CLK2
D4_MA_CLK#2
D4_CS_A#1
D4_CS_A#0
D4_CS_A#3
D4_CS_A#2
D4_CKE_A1
D4_CKE_A0
D4_CKE_A3
D4_CKE_A2
D4_ODT_A1
D4_ODT_A0
D4_ODT_A3
D4_ODT_A2
D4_MCB_A[0:7]
D4_A_PAR
D4_A_RESET#
D4_A_EVENT#
D4_A_ALERT#
D4_A_ACT#
VDDSPD
GND
S_SMBDATA_MAIN_DIMM
S_SMBCLK_MAIN_DIMM
D4C5
330PF/50V
/X/DDR4
D4C6
330PF/50V
/X/DDR4
D4_DQS_A8
D4_DQS_A#8
D4_DQS_A7
D4_DQS_A#7
D4_DQS_A6
D4_DQS_A#6
D4_DQS_A5
D4_DQS_A#5
D4_DQS_A4
D4_DQS_A#4
D4_DQS_A3
D4_DQS_A#3
D4_DQS_A2
D4_DQS_A#2
D4_DQS_A1
D4_DQS_A#1
D4_DQS_A0
D4_DQS_A#0
D4_A_DM[0:8]
D4_A_DM8
D4_A_DM7
D4_A_DM6
D4_A_DM5
D4_A_DM4
D4_A_DM3
D4_A_DM2
D4_A_DM1
D4_A_DM0
DIMM_A2_STAR
ASTERISK
/X
VDDQ
D4R13
1KOHM
1%
/DDR4
S_SMBDATA_MAIN
S_SMBCLK_MAIN
S_SMBDATA_MAIN_DIMM
S_SMBCLK_MAIN_DIMM
D4R15
D4R21
0402
/X
Title :
AM4-10
ASUSTek Computer Inc.
Engineer:
Elainelx_Li
Size
A3
Project Name
AM4
Rev
0.01
Date:
Wednesday, August 29, 2018
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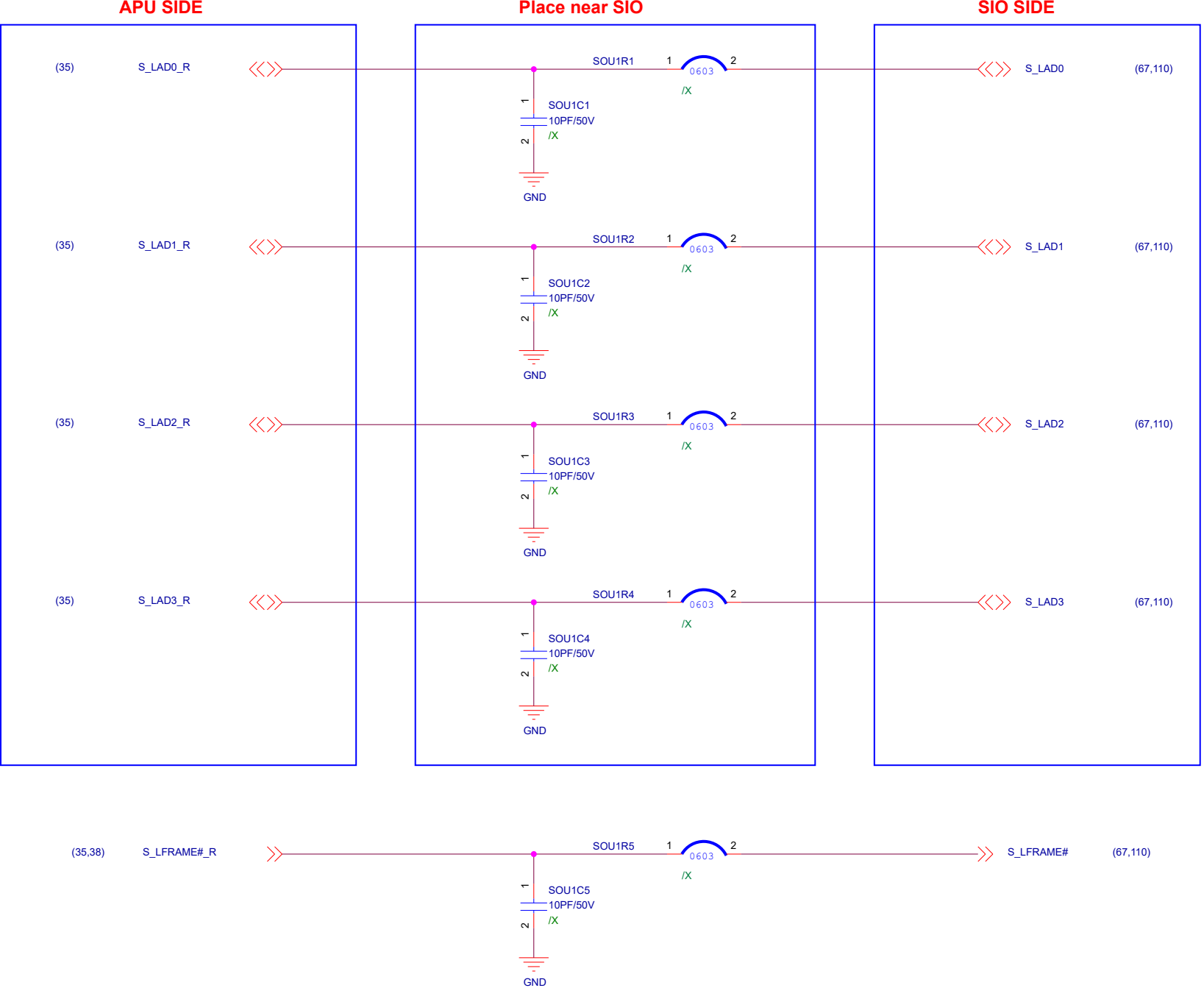
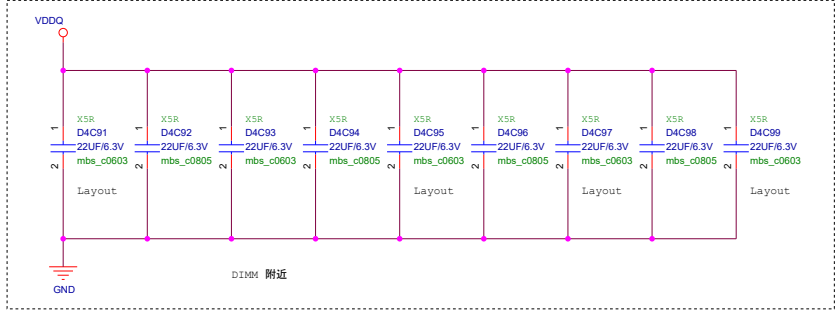
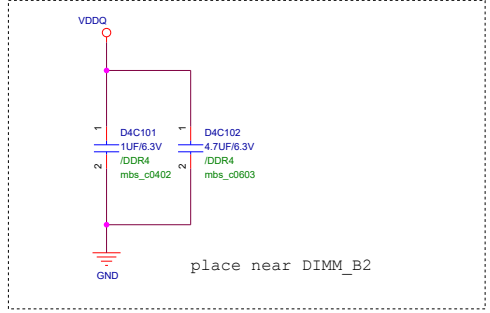
117

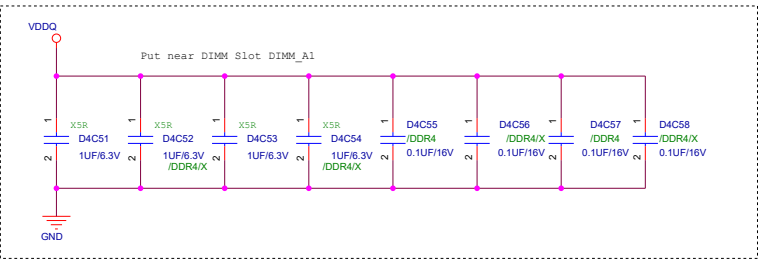


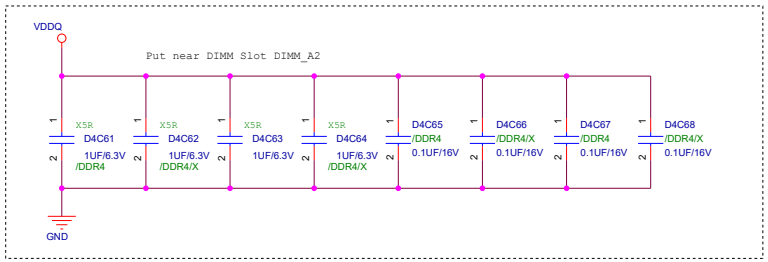
ASUSTek Computer Inc.	Title : AM4-09		
	Engineer: Elainelx_Li		
Size: A4	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 39 of 117		

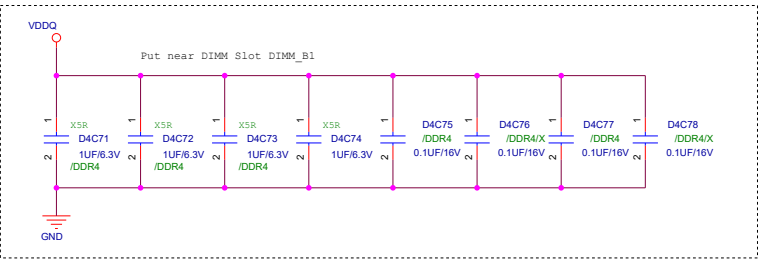
Layout to 0603

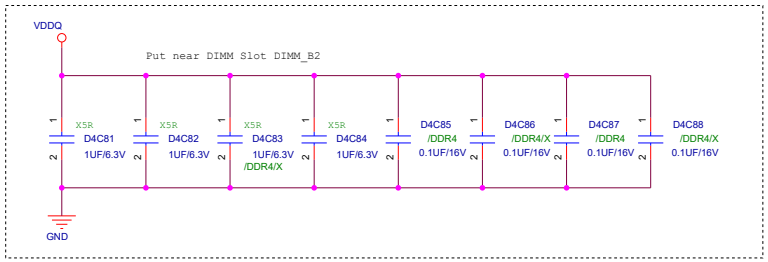


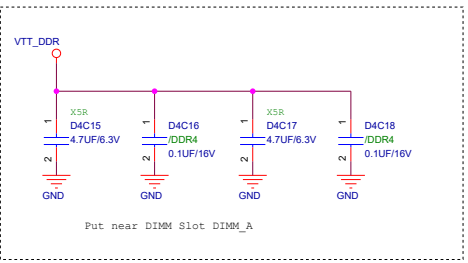


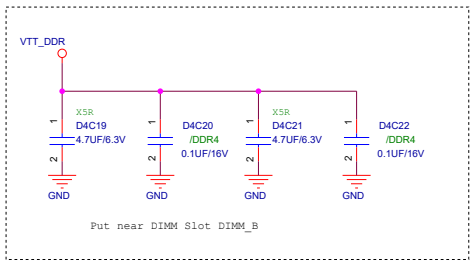


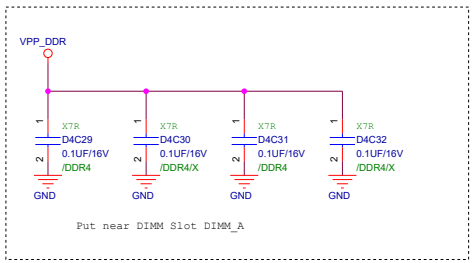


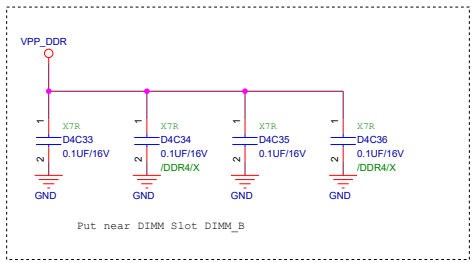




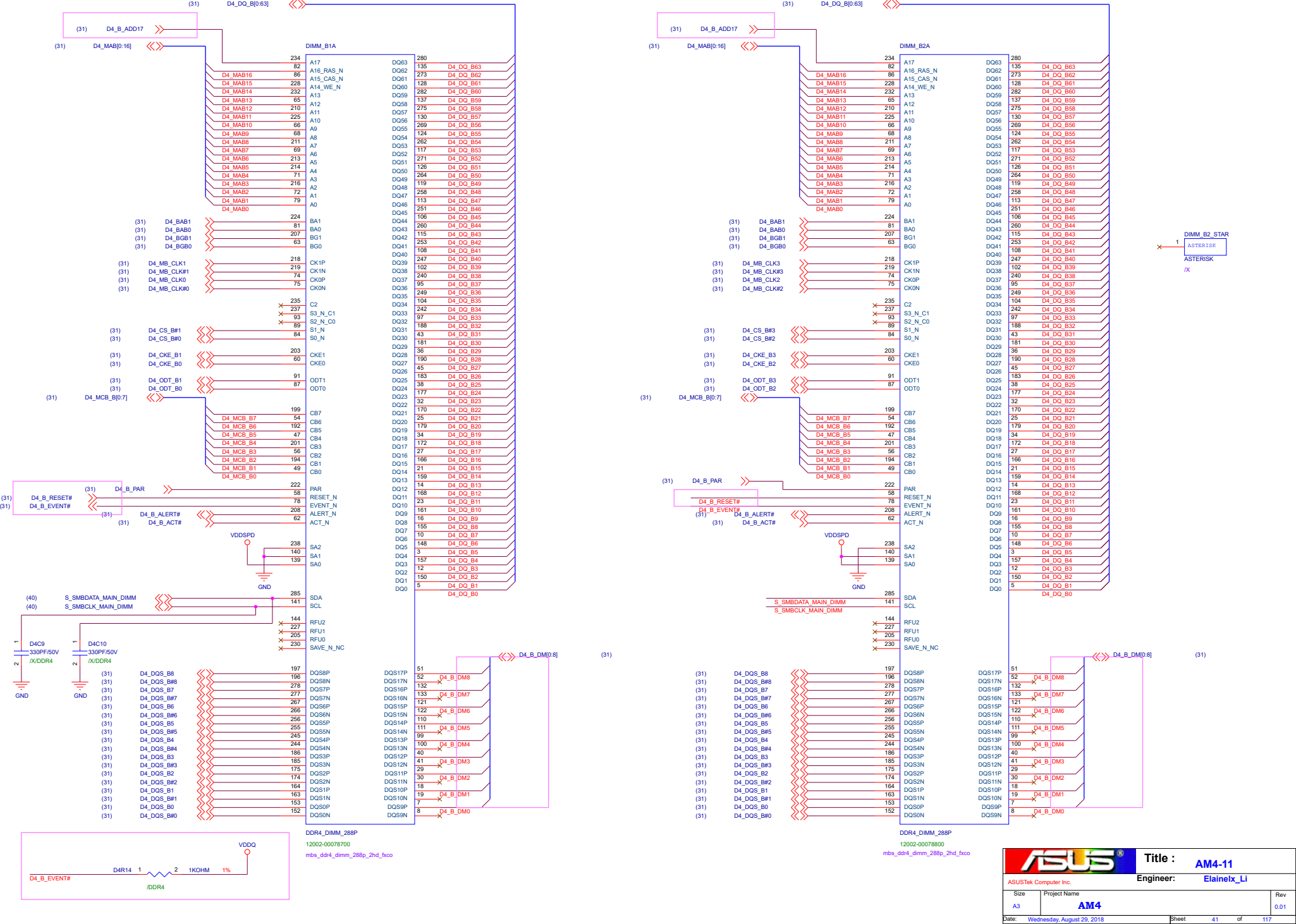




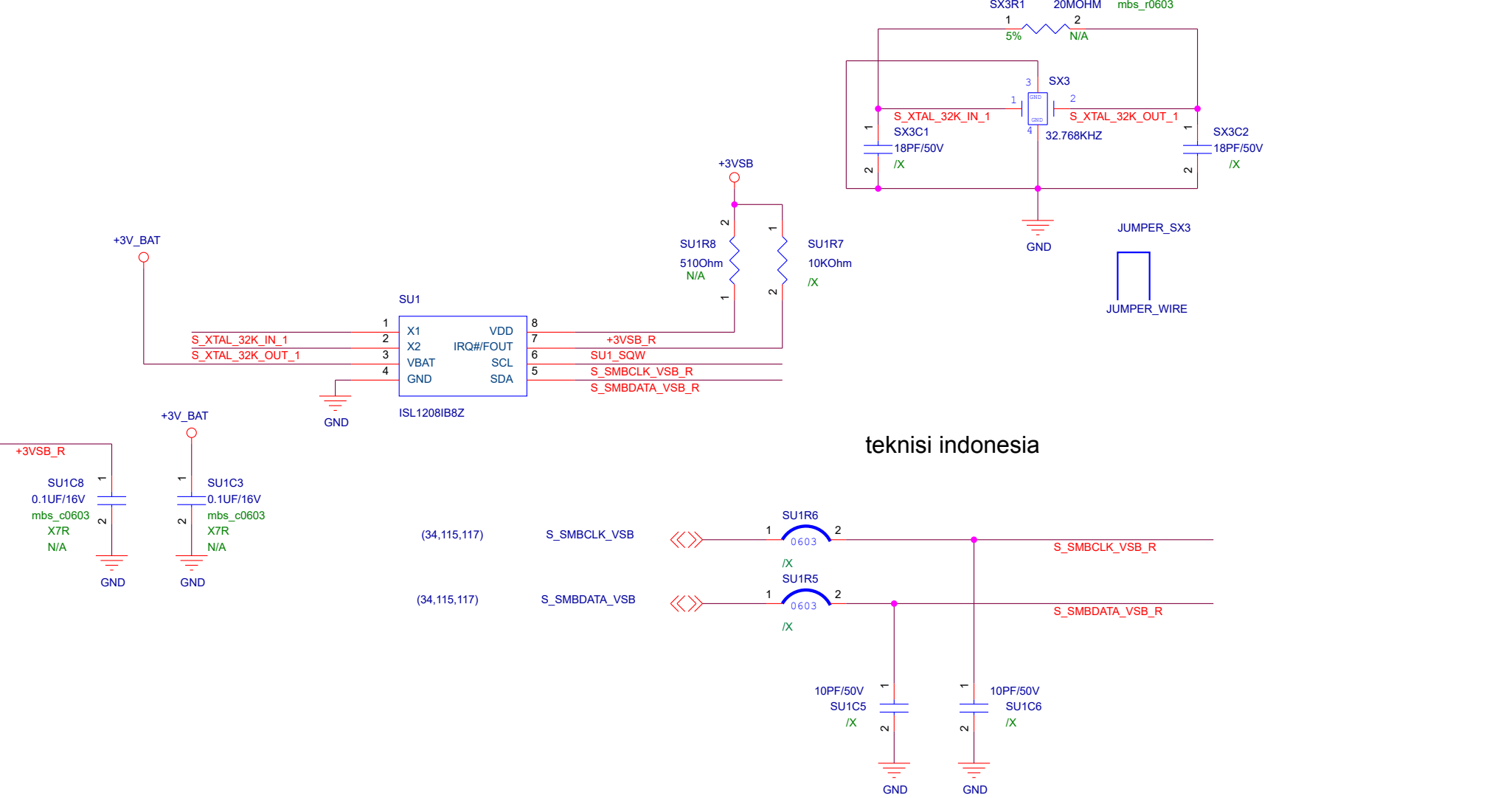




ASUSTek Computer Inc.	Title : AM4-13		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Friday, August 17, 2018	Sheet 43 of 117		



ASUSTek Computer Inc.	Title :	AM4-11	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 41 of 117		



Title	<Title>	
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date: Wednesday, August 29, 2018	Sheet 44 of 117	

0719

<Variant Name>

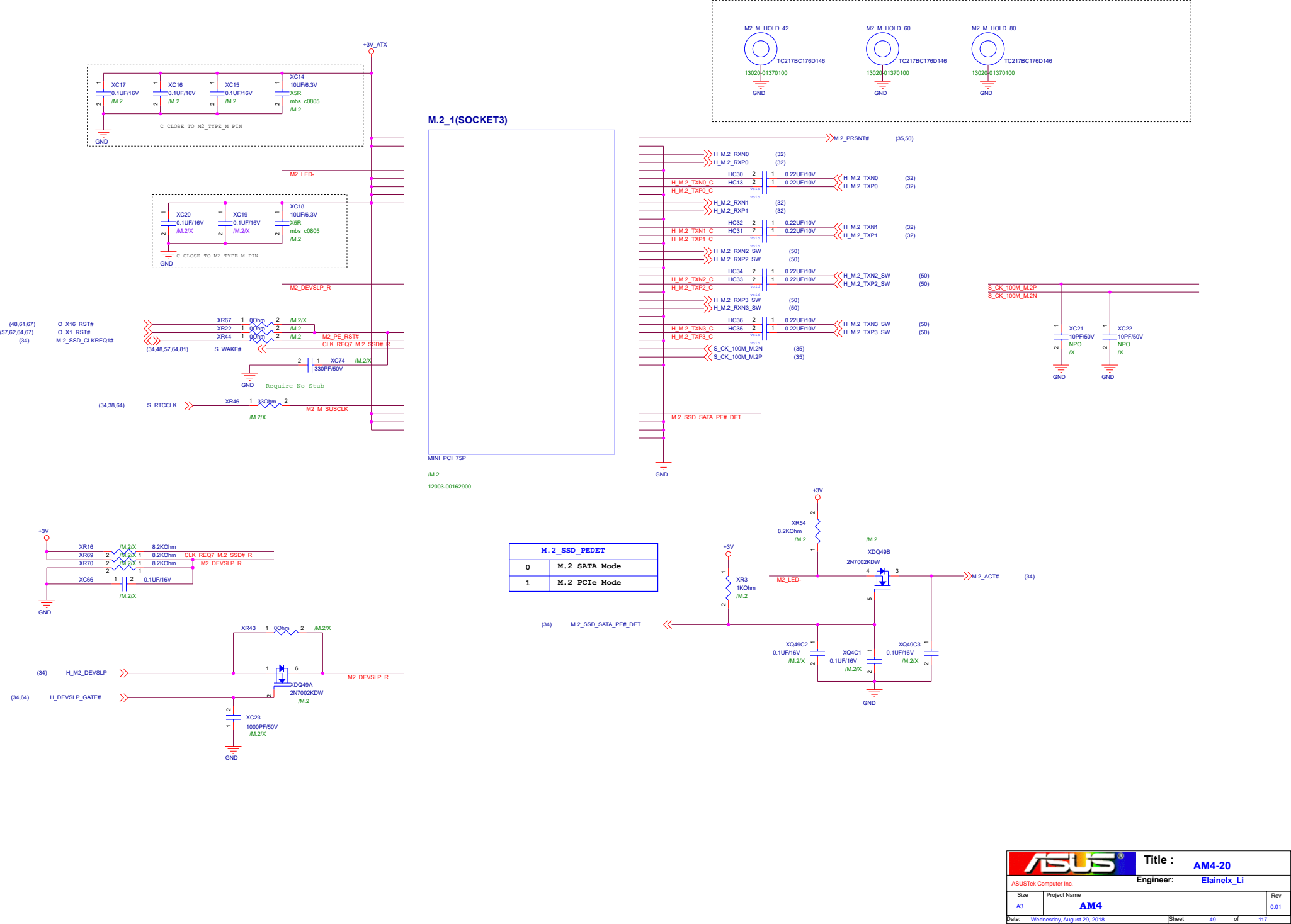
Title : DP_MUX_PS8331

ASUSTeK COMPUTER INC

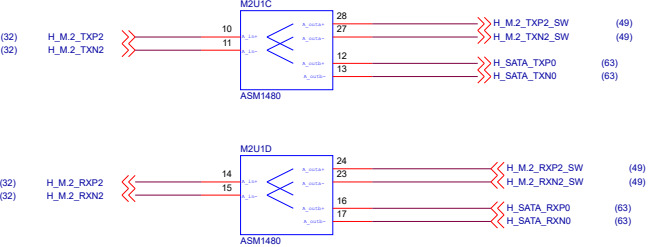
Engineer: Morse_Peng

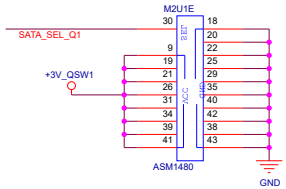
Size	Project Name	Rev
A2	SkyLake VC	R1.00

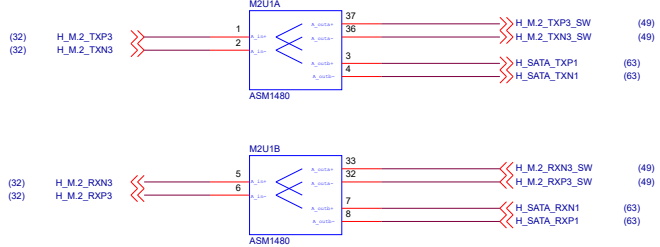
Date:	Friday, August 17, 2018	Sheet	45	of	117



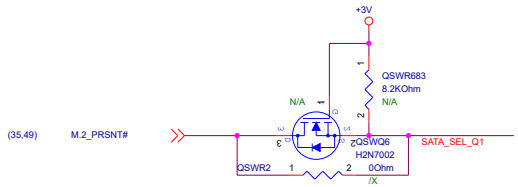
ASUSTek Computer Inc.	Title : AM4-20	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 49 of 117	

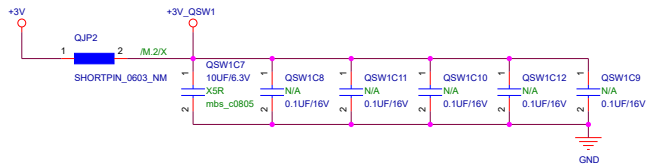






M.2_PRSNT#	Function	
L	N_in to N_outa	M.2
H	N_in to N_outb	SATA





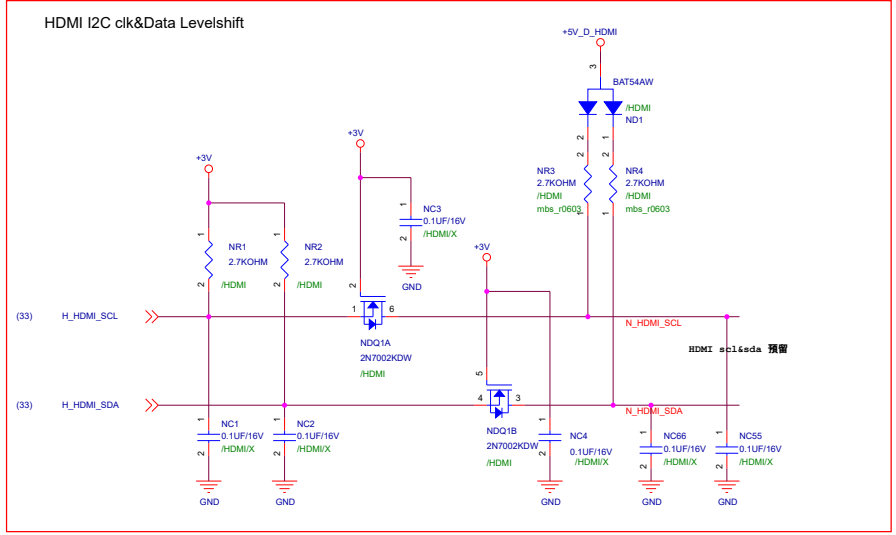
ASUSTek Computer Inc.

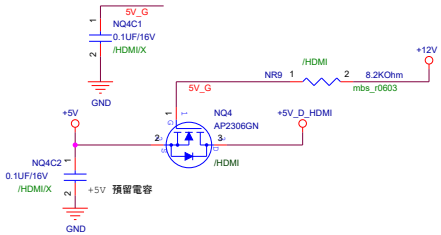
Title : M.2 SW

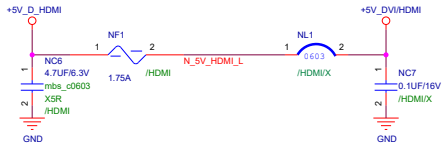
Engineer: Elainelx_Li

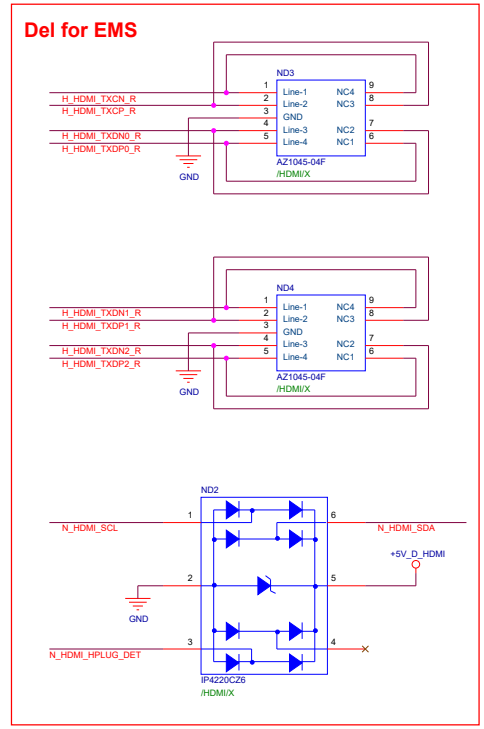
Size	Project Name	Rev
A3	AM4	0.01

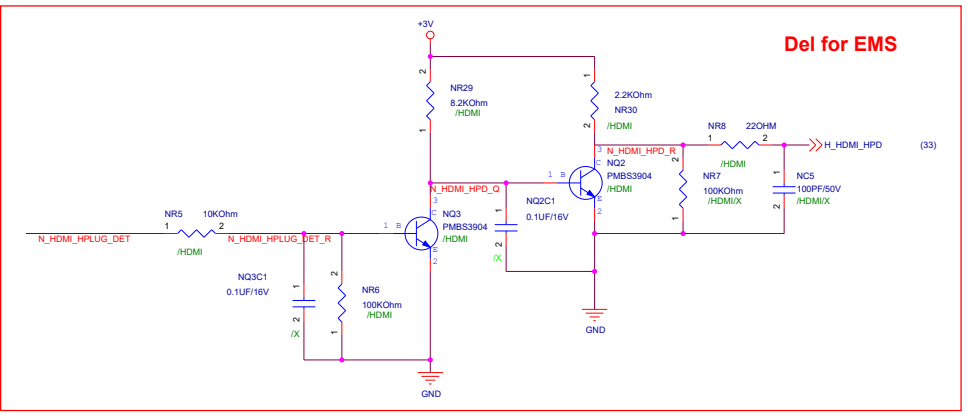
Date: Wednesday, August 29, 2018 Sheet 50 of 117

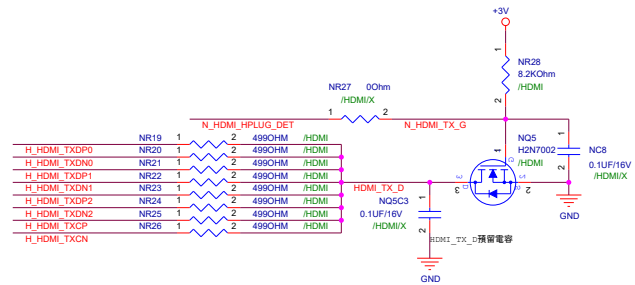












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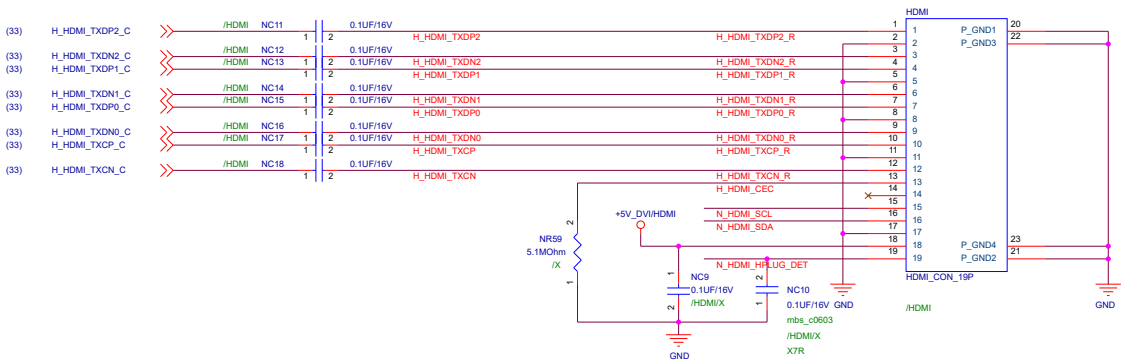
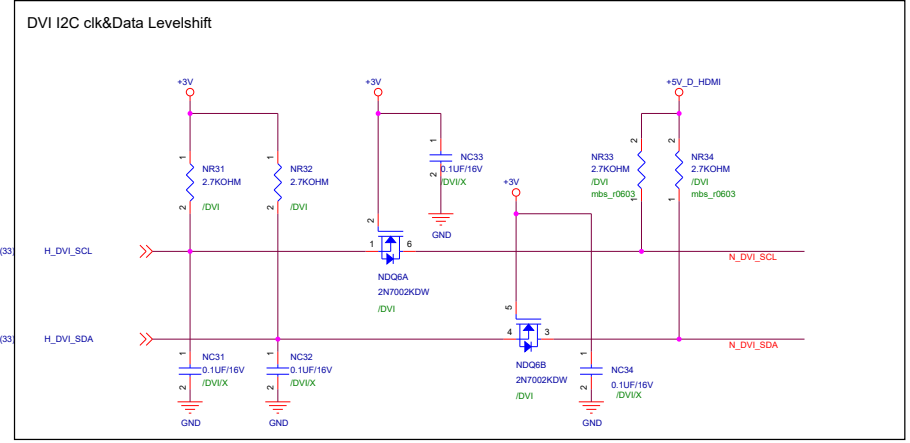
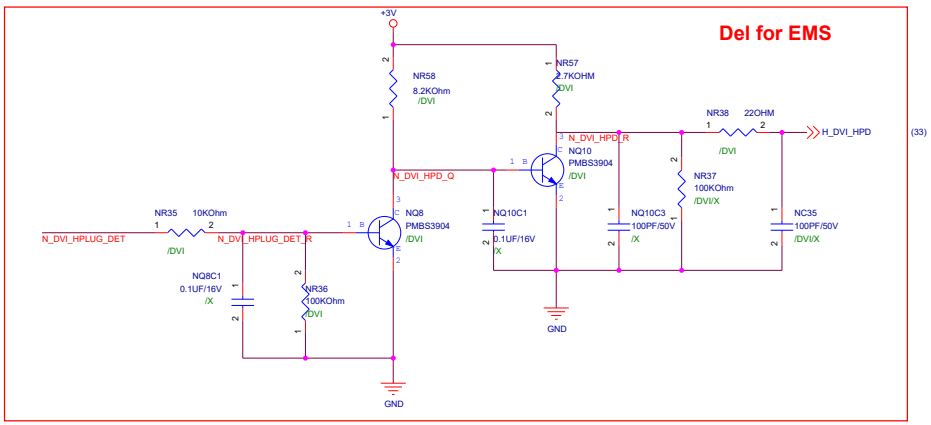
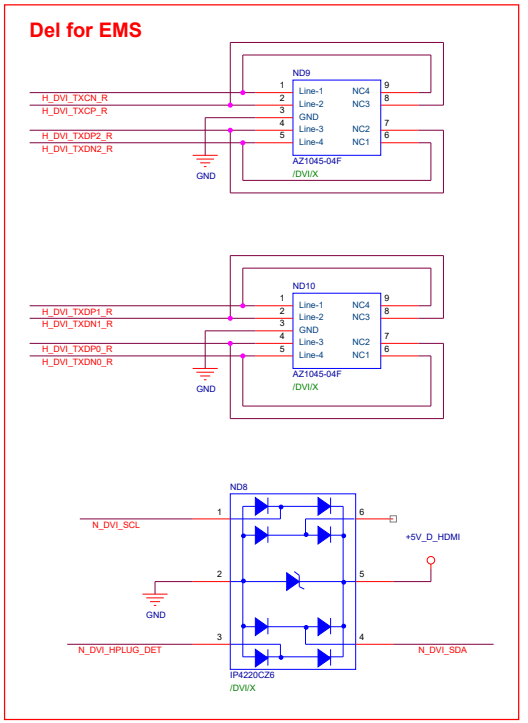
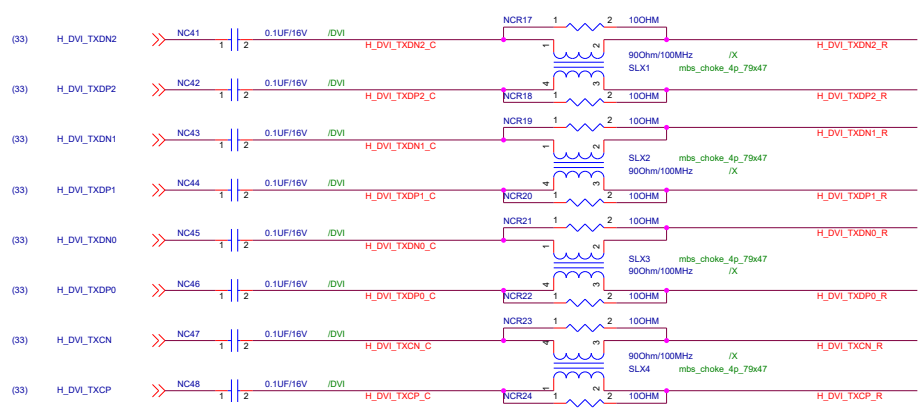


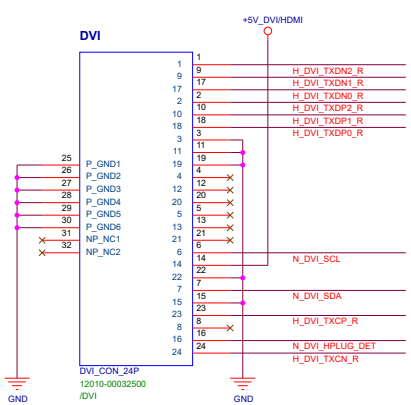
ASUSTek Computer Inc.	Title :	AM4-16	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 46 of 117		

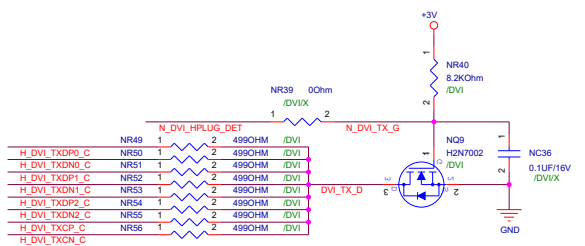




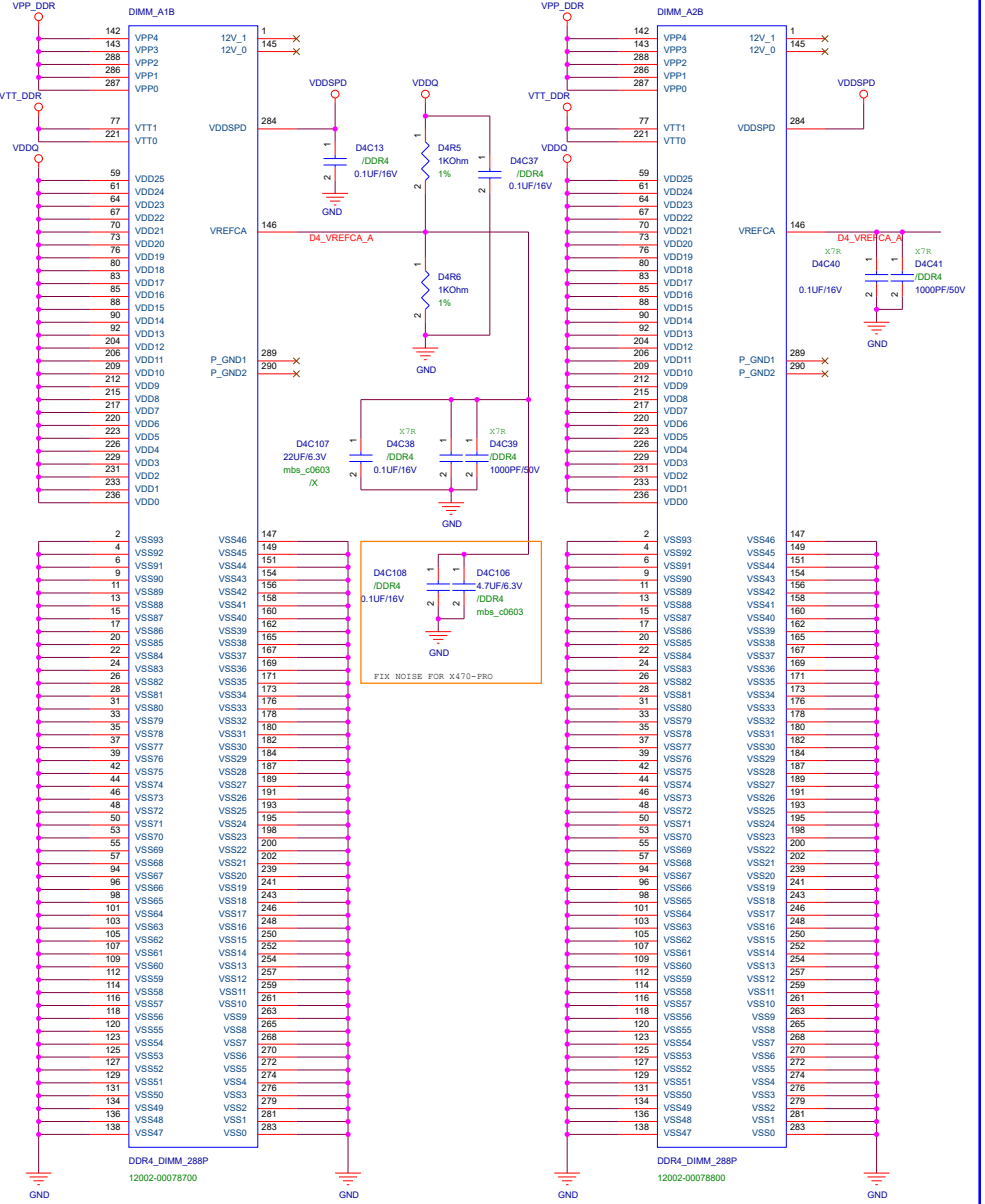


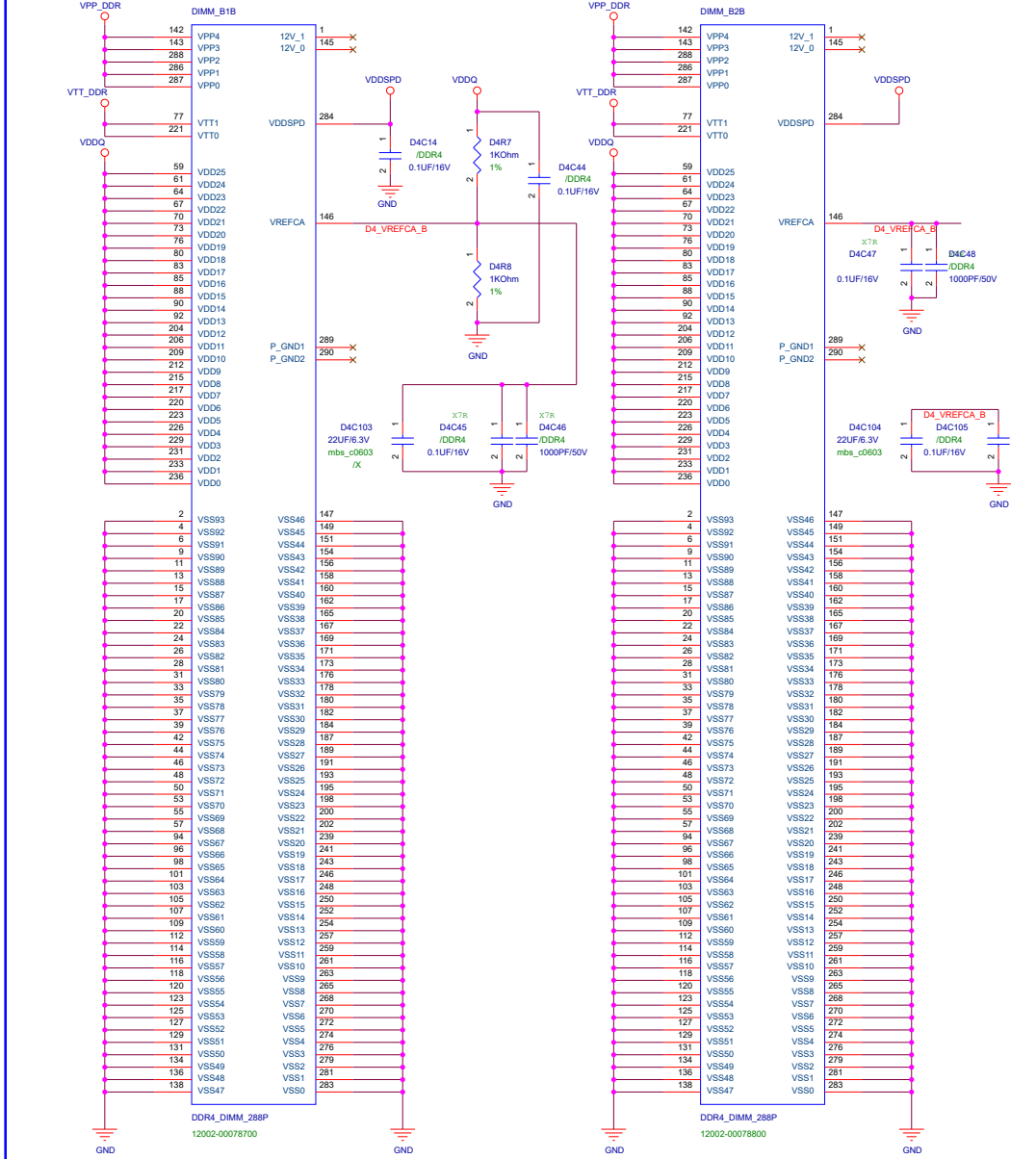


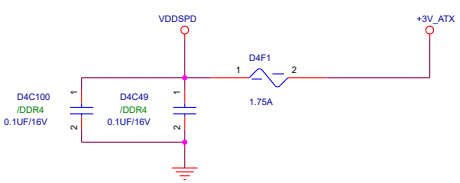




ASUSTek Computer Inc.	Title :	AM4-17	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 47 of 117		

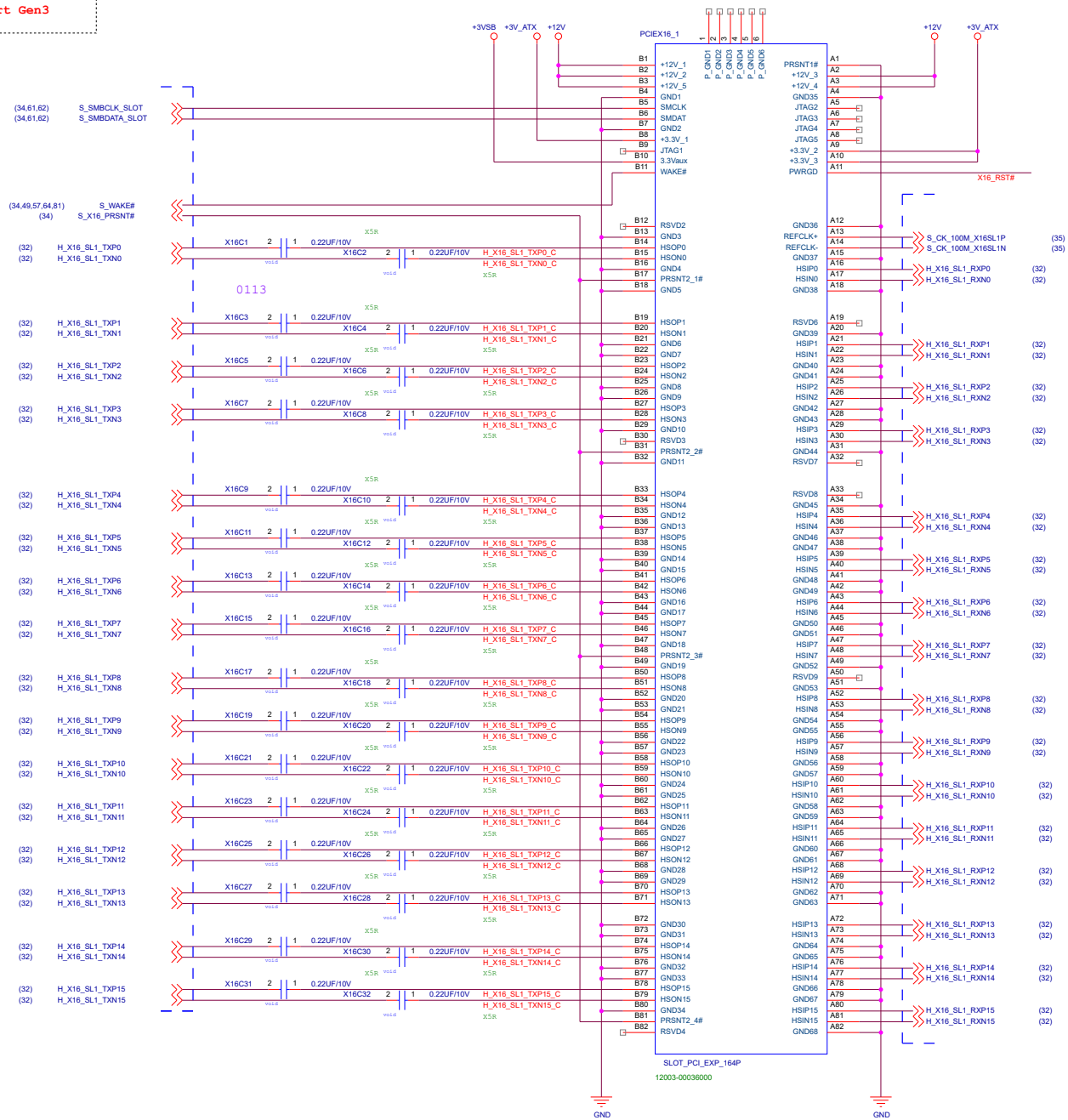






ASUSTek Computer Inc.	Title :	AM4-12	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Friday, August 17, 2018	Sheet 42 of 117		

Support Gen3



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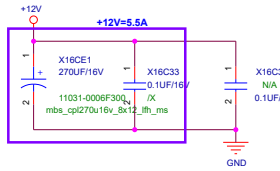
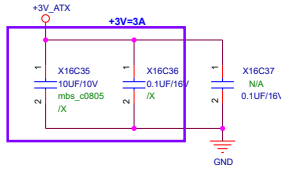
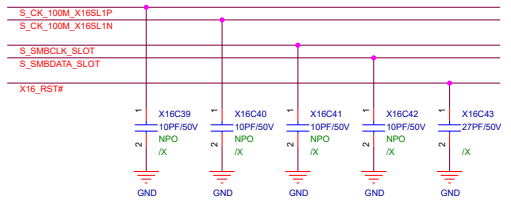
12003-00036000
Symbol:s_pci_exp_164p_6hod_fox_lf3

X16CE1	P/N	11V090277339
	Footprint	mbs_cpl270u16v_8x12_lfh_ms Taping并剪腳H



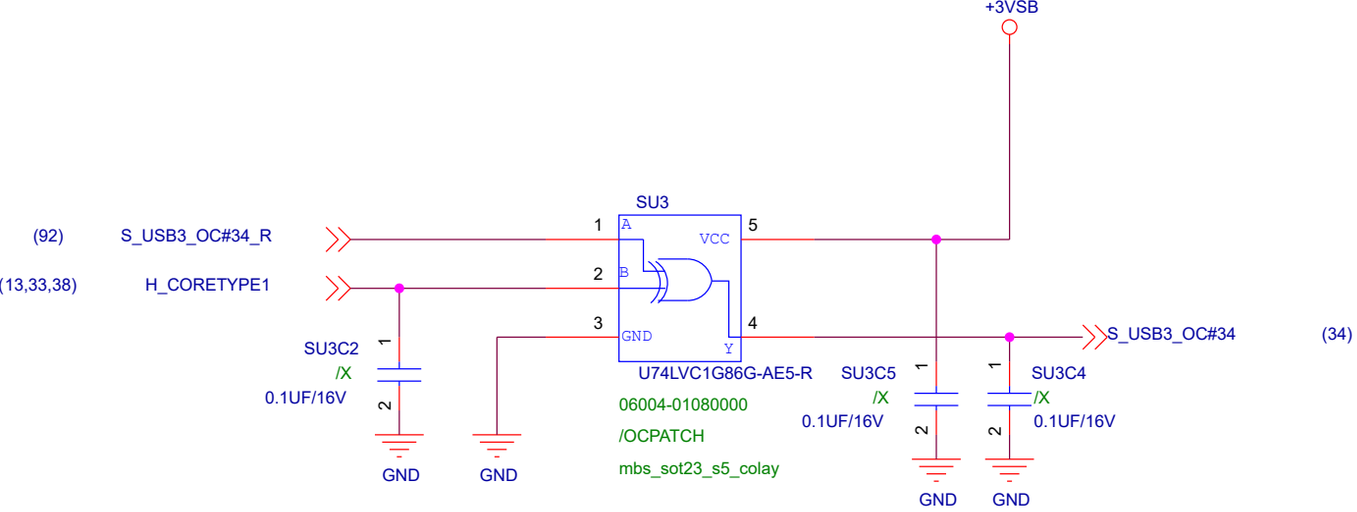


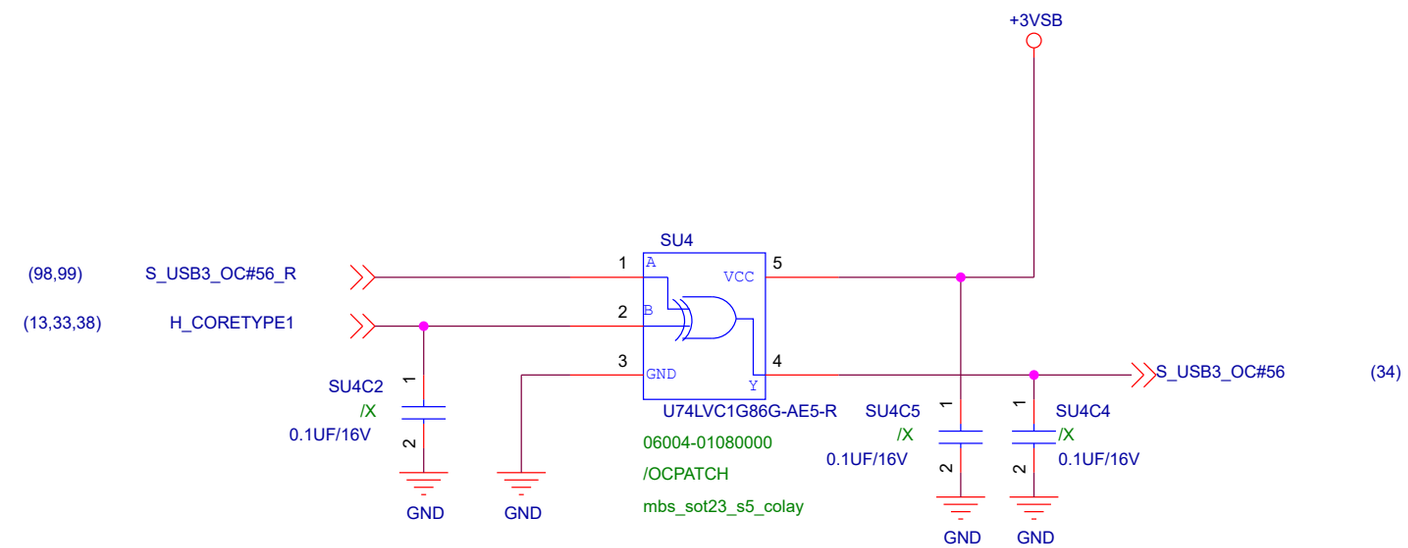
Place near slot



(49,61,67) O_X16_RST# → X16_RST# → X16_RST# (49,67)

ASUSTek Computer Inc.	Title :	AM4-15	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 48 of 117		





<Variant Name>

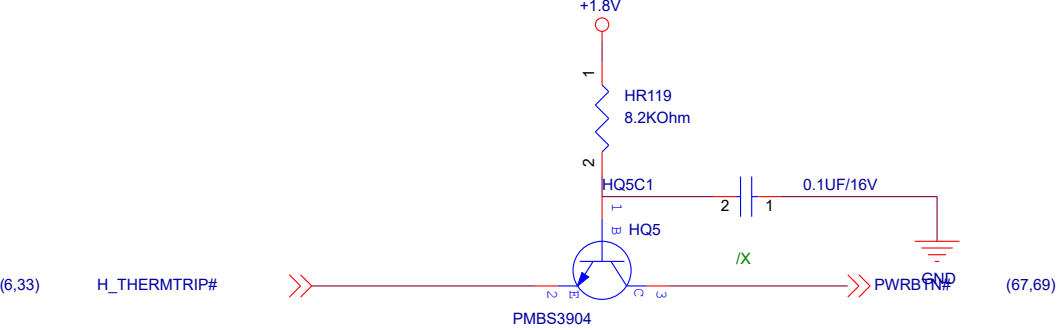
ASUSTEK COMPUTER INC

Title : Patch For USBOC

Engineer:

Size	Project Name	Rev
A4		0.0

Date: Wednesday, August 29, 2018 Sheet 52 of 117



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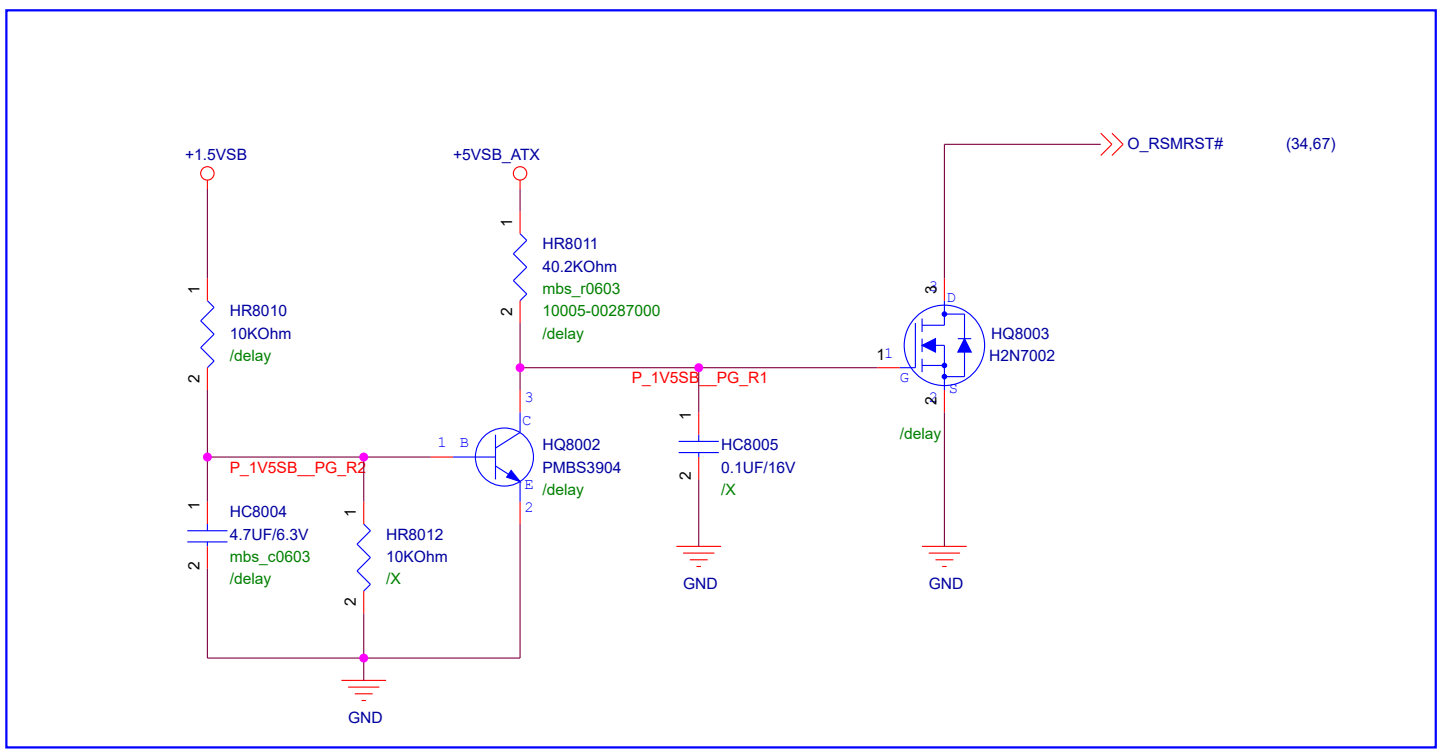

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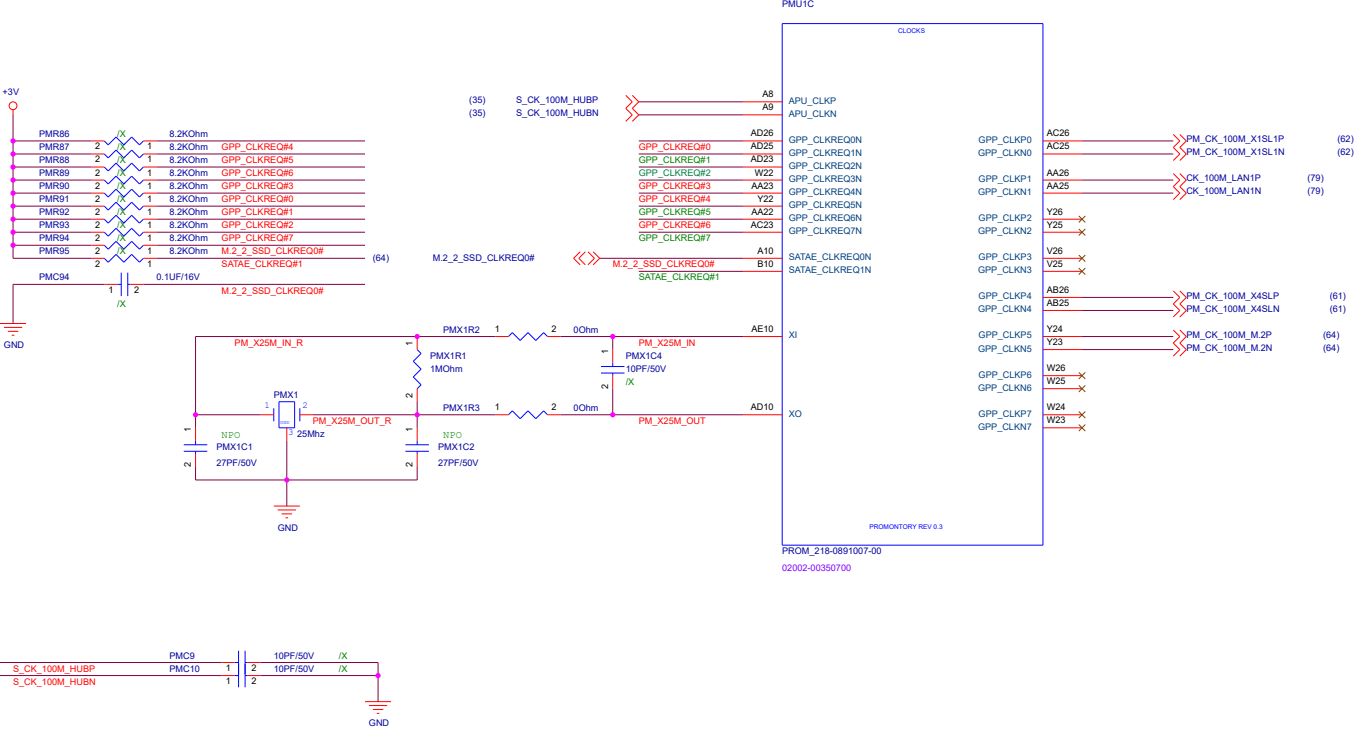
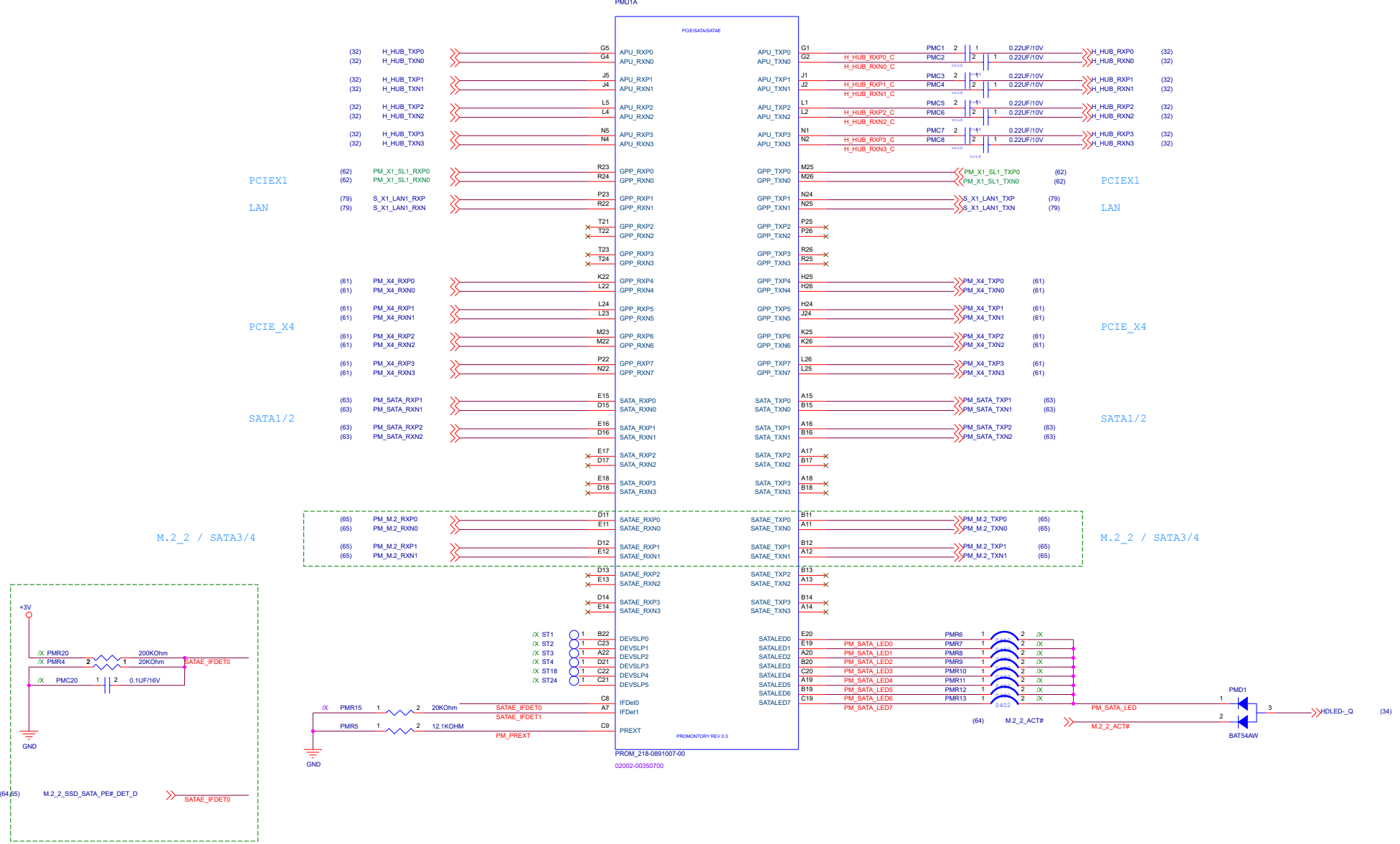
Size A	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, August 29, 2018	Sheet 51 of 117		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 53 of 117	



ASUSTek Computer Inc.	Title : PROM-03		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 56 of 117		



M.2_SSD_PEDET	
0	M.2 SATA Mode
1	M.2 PCIe Mode

IFDET1	SATA Express port1 1: PCIe mode; 0: SATA mode
IFDET0	SATA Express port0 1: PCIe mode; 0: SATA mode

BUS Model	USB				SATA3.0	SATA Express	PCIeG2GPP	PCIeCLK
	3.1Gen2 10Gbps	3.1Gen1 5Gbps	2.0	Debug Port				
PROM28.A	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	All USB3.1 port	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM26.A	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	All USB3.1 port	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7

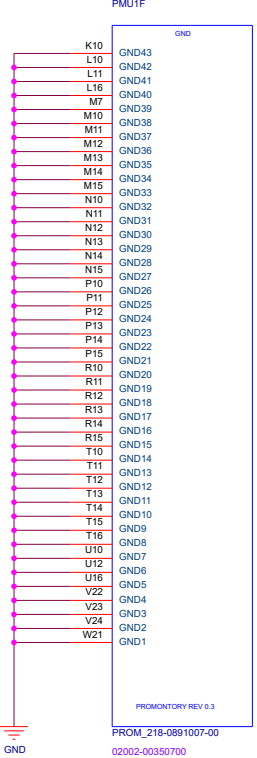
ASUSTek Computer Inc.

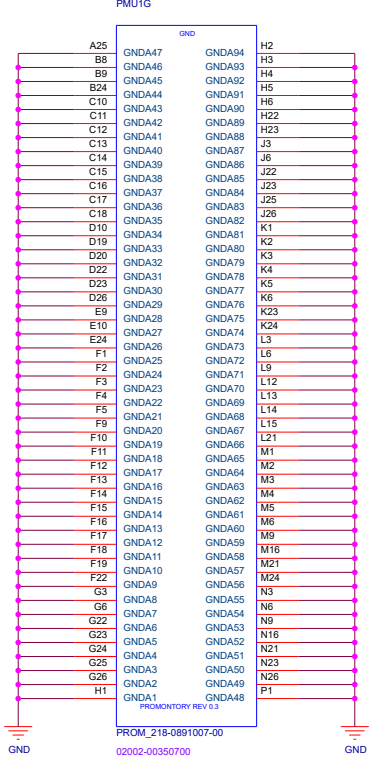
Title : PROM-01

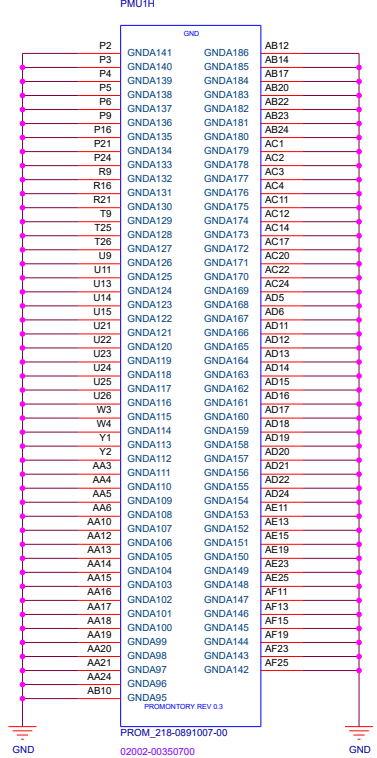
Engineer: Elainelx_Li

Size	Project Name	Rev
A3	AM4	0.01

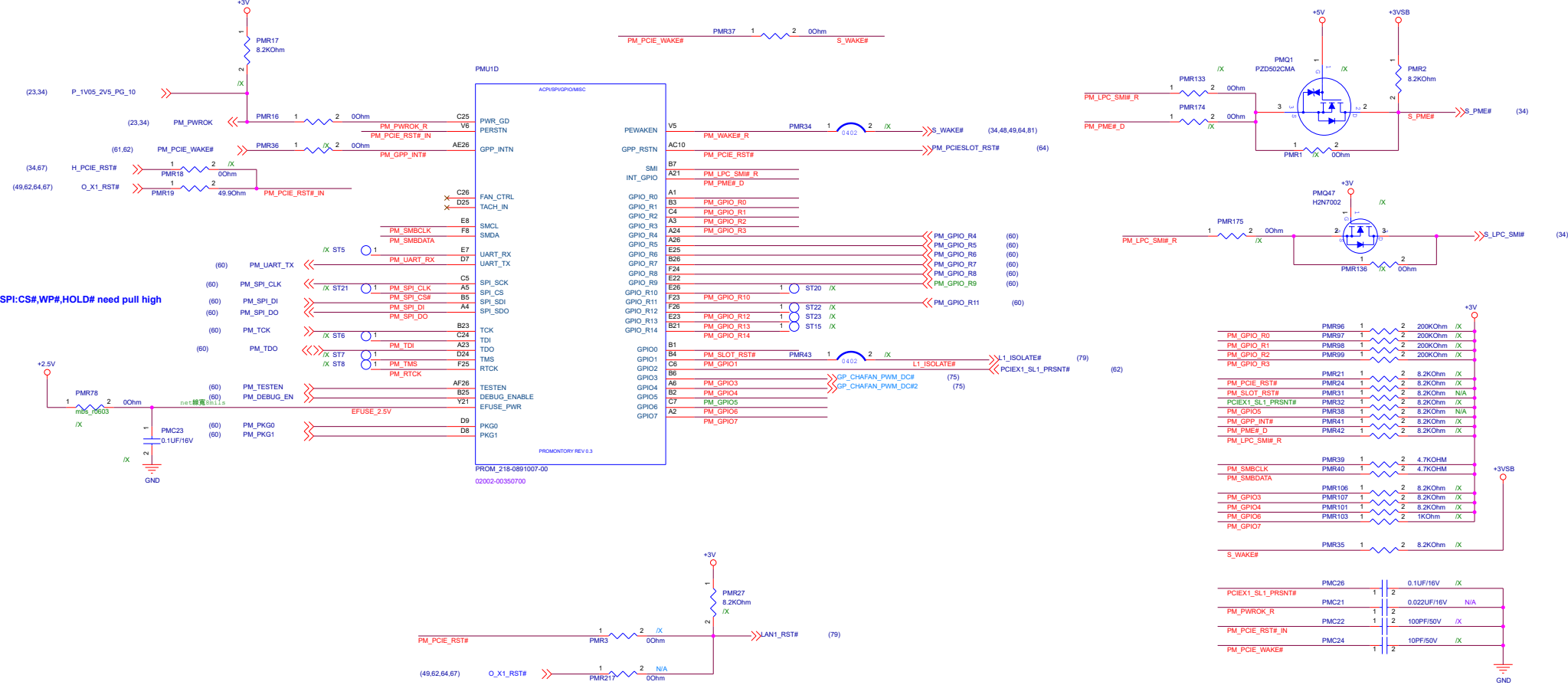
Date: Wednesday, August 29, 2018 Sheet 54 of 117







ASUSTek Computer Inc.	Title : PROM-06	
	Engineer: Elainelx_Li	
Size: A3	Project Name: ME175KG	Rev: 1.00
Date: Friday, August 17, 2018	Sheet 59 of 117	



ASUSTek Computer Inc.	Title :	PROM-04	
	Engineer:	Elaineix_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 57 of 117		

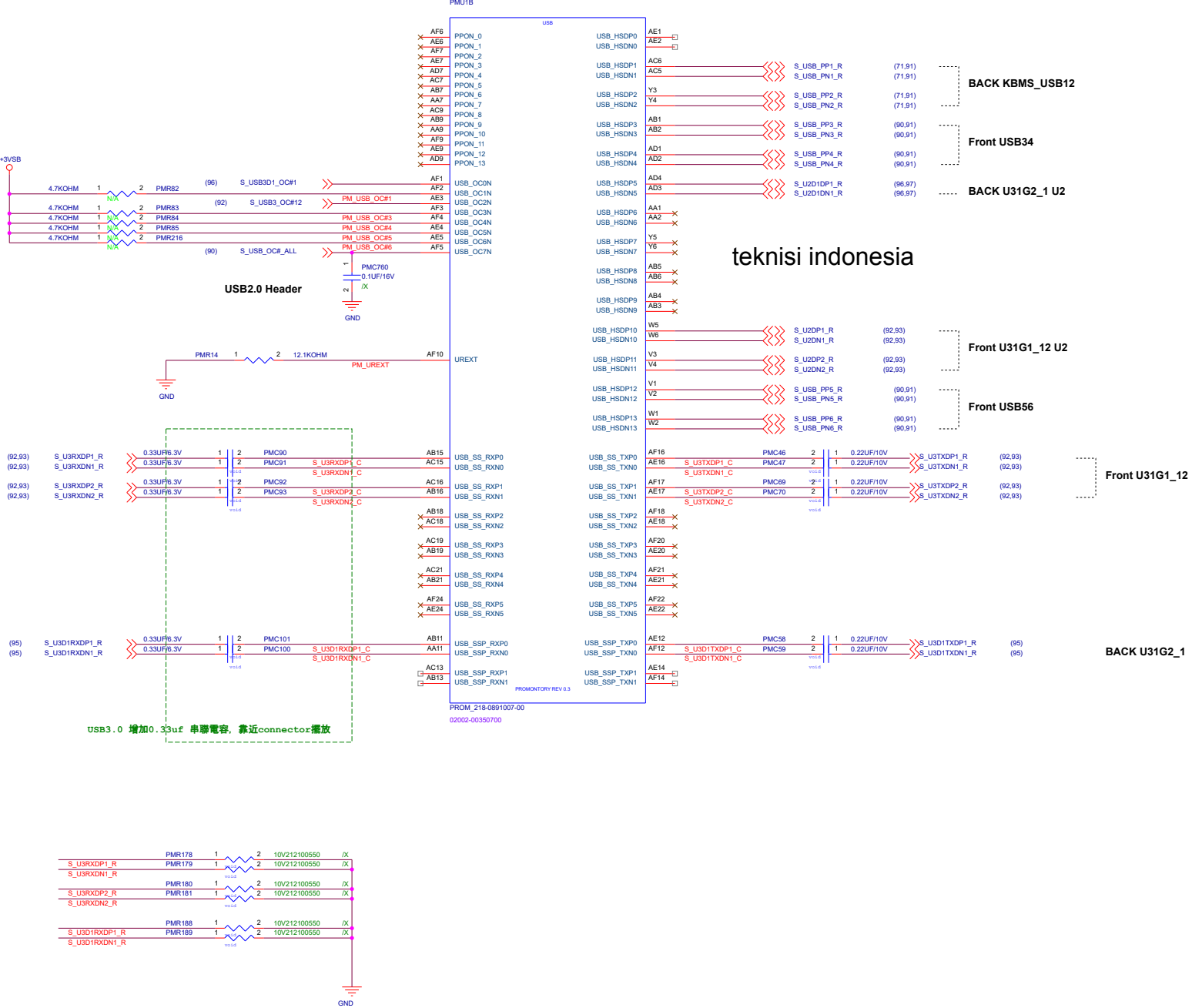
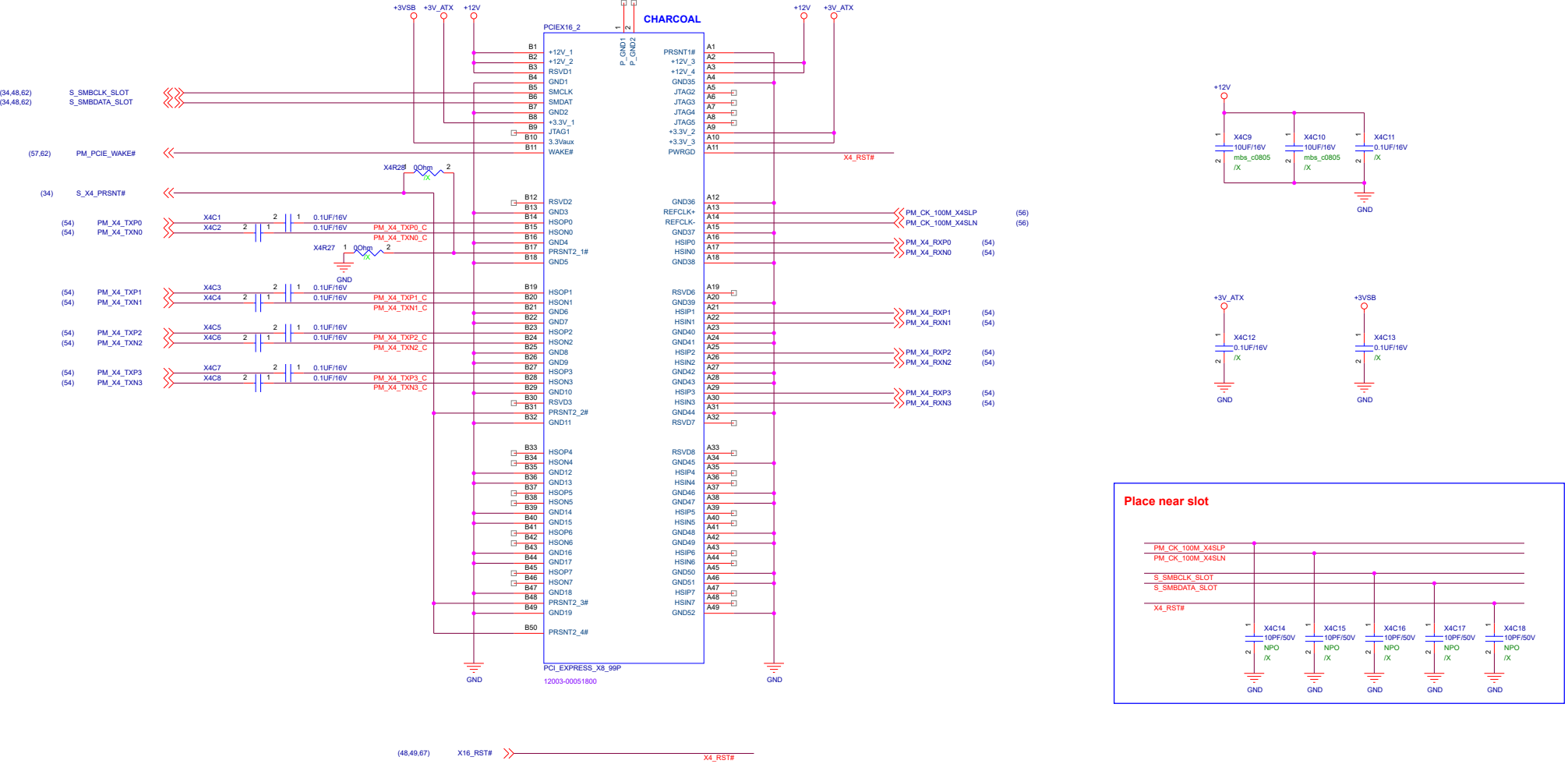


Table 10. USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RX[0]	USB_HSD[5]	USB_OC0N
USB_SSP_TX/RX[1]	USB_HSD[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RX[0]	USB_HSD[10]	USB_OC2N
USB_SS_TX/RX[1]	USB_HSD[11]	USB_OC3N
USB_SS_TX/RX[2]	USB_HSD[6]	USB_OC4N
USB_SS_TX/RX[3]	USB_HSD[7]	USB_OC5N
USB_SS_TX/RX[4]	USB_HSD[8]	USB_OC6N
USB_SS_TX/RX[5]	USB_HSD[9]	USB_OC7N
	USB_HSD[1]	USB_OC7N
	USB_HSD[2]	USB_OC7N
	USB_HSD[3]	USB_OC7N
	USB_HSD[4]	USB_OC7N
	USB_HSD[12]	USB_OC7N
	USB_HSD[13]	USB_OC7N

ASUSTek Computer Inc.	Title : PROM-02		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Thursday, August 30, 2018	Sheet 55 of 117		



ASUSTek Computer Inc.

Title : PROM-08

Engineer: Elainelx_Li

Size	Project Name	Rev
A3	AM4	0.01

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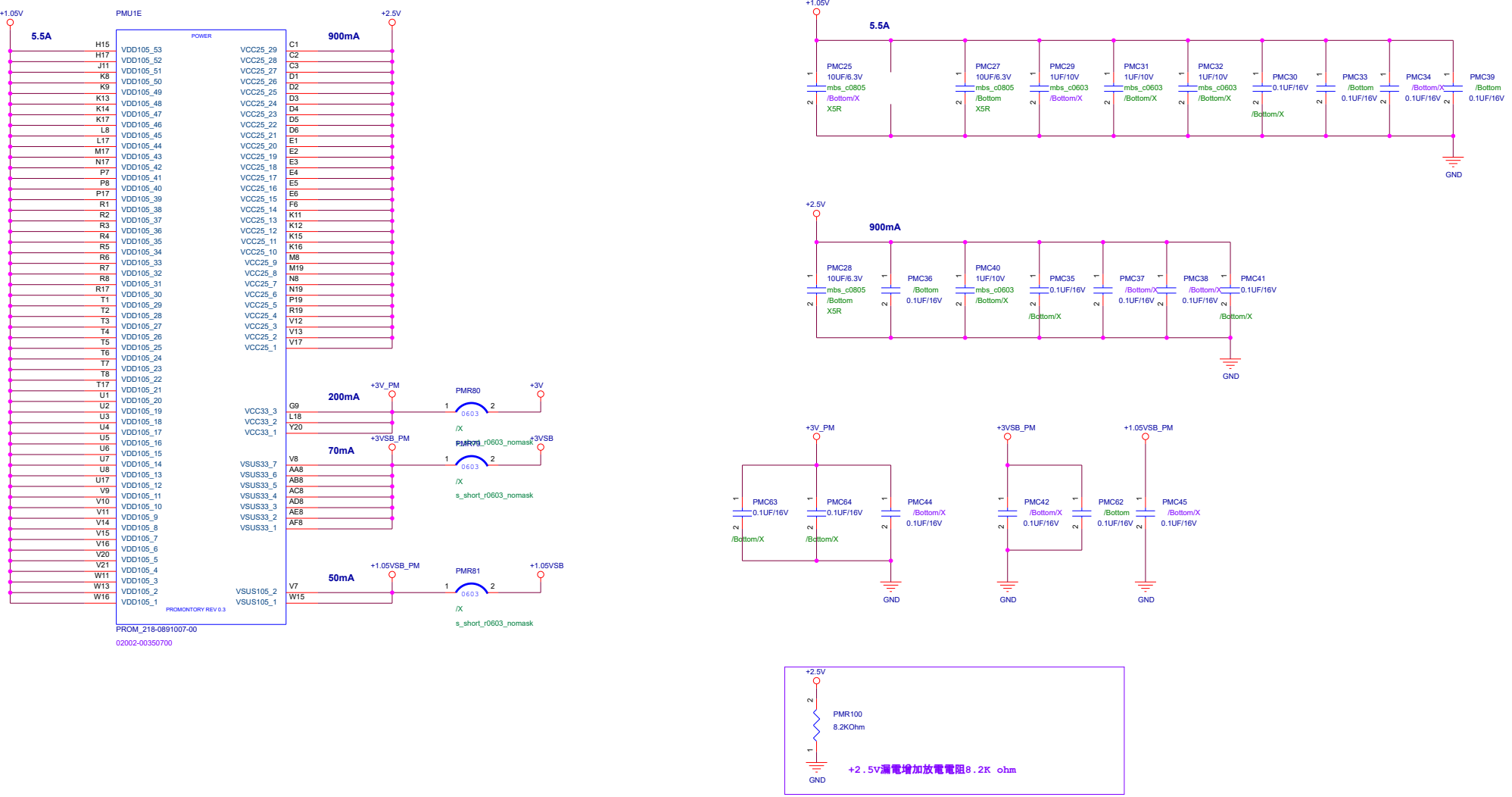
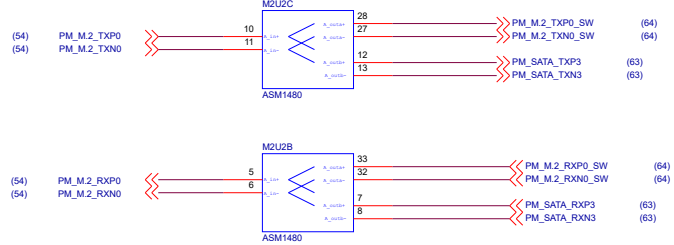
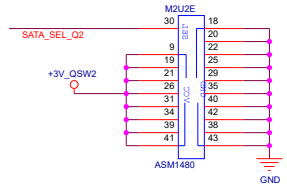
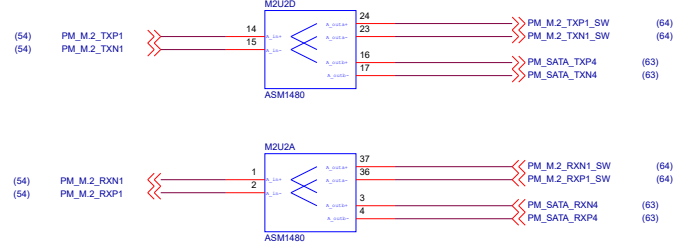


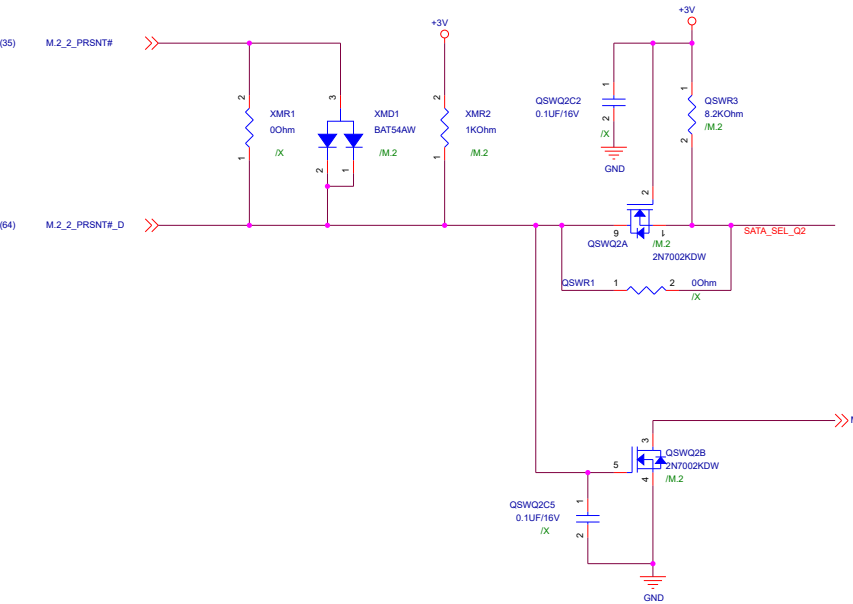
ASUSTek Computer Inc.	Title :	PROM-05	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Friday, August 17, 2018	Sheet 58 of 117		

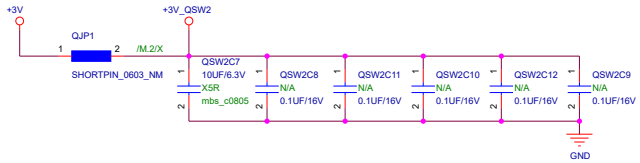




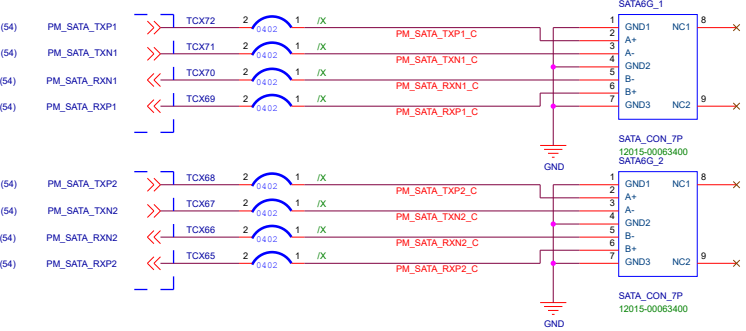


M.2_PRSNT#	Function	
L	N_in to N_outa	M.2
H	N_in to N_outb	SATA

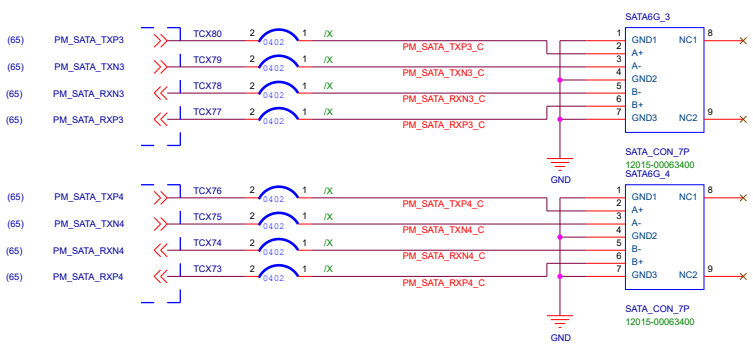


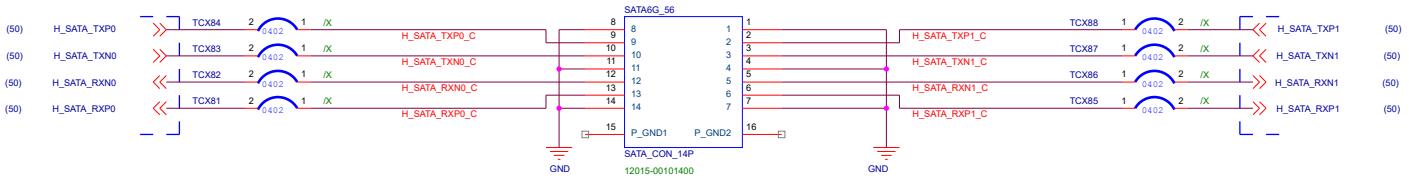


ASUSTek Computer Inc.	Title :	M.2 SW	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 65 of 117		

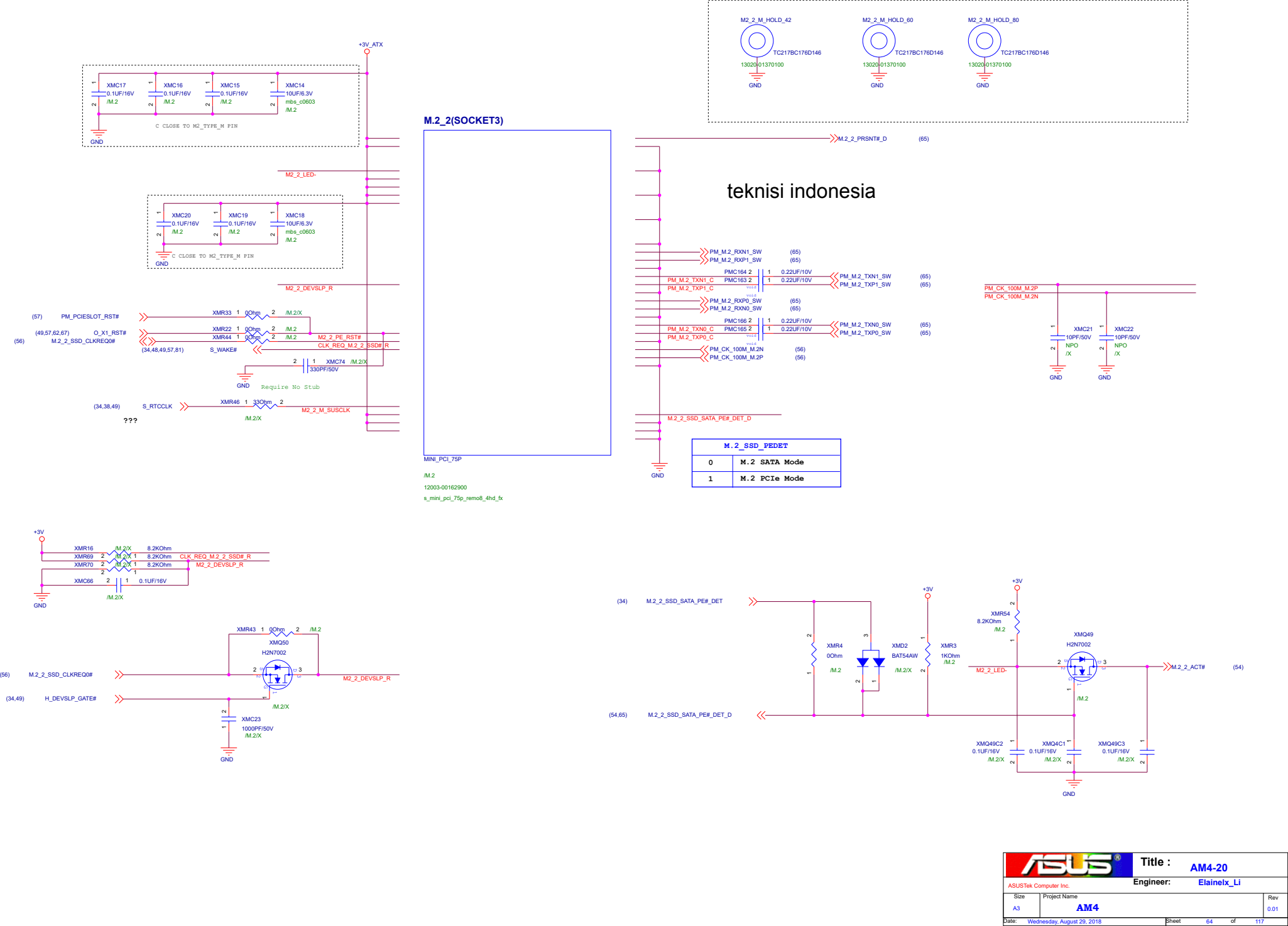


for Pad reference層挖空

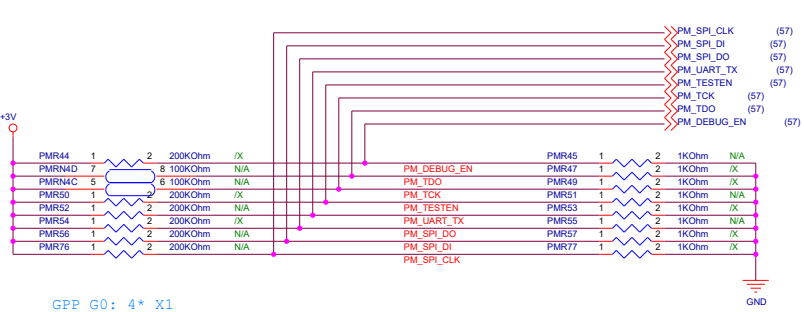




ASUSTek Computer Inc.	Title : PROM-09		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 63 of 117		

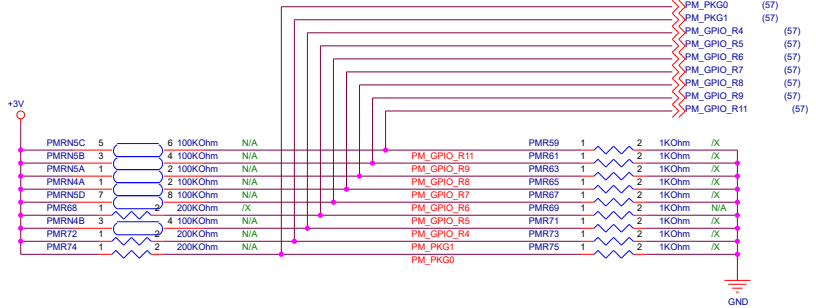

M2_2_M_HOLD_42
M2_2_M_HOLD_60
M2_2_M_HOLD_80
TC217BC176D146
13020-01370100
GND
+3V_ATX
XMC17 0.1UF/16V /M.2
XMC16 0.1UF/16V /M.2
XMC15 0.1UF/16V /M.2
XMC14 10UF/6.3V mbs_c0603 /M.2
C CLOSE TO M2_TYPE_M PIN
M2_2_LED-
XMC20 0.1UF/16V /M.2
XMC19 0.1UF/16V /M.2
XMC18 10UF/6.3V mbs_c0603 /M.2
M2_2_DEVSLP_R
(57) PM_PCIESLOT_RST#
XMR33 0Ohm /M.2/X
(49,57,62,67) O_X1_RST#
XMR22 0Ohm /M.2
(56) M.2_2_SSD_CLKREQ0#
XMR44 0Ohm /M.2
M2_2_PE_RST#
(34,48,49,57,81) S_WAKE#
CLK_REQ_M.2_2_SSD#_R
XMC74 330PF/50V /M.2/X
Require No Stub
(34,38,49) S_RTCCLK
XMR46 33Ohm /M.2/X
M2_2_M_SUSCLK
???
M.2_2(SOCKET3)
MINI_PCI_75P
/M.2
12003-00162900
s_mini_pci_75p_remo8_4hd_fx
M.2_2_PRSNT#_D (65)
teknisi indonesia
PM_M.2_RXN1_SW (65)
PM_M.2_RXP1_SW (65)
PMC164 0.22UF/10V
PM_M.2_TXN1_C PMC163 0.22UF/10V
PM_M.2_TXP1_C
PM_M.2_TXN1_SW (65)
PM_M.2_TXP1_SW (65)
PM_M.2_RXP0_SW (65)
PM_M.2_RXN0_SW (65)
PMC166 0.22UF/10V
PM_M.2_TXN0_C PMC165 0.22UF/10V
PM_M.2_TXP0_C
PM_M.2_TXN0_SW (65)
PM_M.2_TXP0_SW (65)
PM_CK_100M_M.2N (56)
PM_CK_100M_M.2P (56)
M.2_2_SSD_SATA_PE#_DET_D
PM_CK_100M_M.2P
PM_CK_100M_M.2N
XMC21 10PF/50V NPO /X
XMC22 10PF/50V NPO /X
M.2_SSD_PEDET
0 M.2 SATA Mode
1 M.2 PCIe Mode
+3V
XMR16 /M.2/X 8.2KOhm
XMR69 /M.2/X 8.2KOhm CLK_REQ_M.2_2_SSD#_R
XMR70 /M.2/X 8.2KOhm M2_2_DEVSLP_R
XMC66 0.1UF/16V /M.2/X
XMR43 0Ohm /M.2
XMQ50 H2N7002
(56) M.2_2_SSD_CLKREQ0#
M2_2_DEVSLP_R
(34,49) H_DEVSLP_GATE#
XMC23 1000PF/50V /M.2/X
(34) M.2_2_SSD_SATA_PE#_DET
XMR4 0Ohm /M.2
XMD2 BAT54AW /M.2/X
XMR3 1KOhm /M.2
XMR54 8.2KOhm /M.2
XMQ49 H2N7002
M2_2_LED-
M.2_2_ACT# (54)
(54,65) M.2_2_SSD_SATA_PE#_DET_D
XMQ49C2 0.1UF/16V /M.2/X
XMQ4C1 0.1UF/16V /M.2/X
XMQ49C3 0.1UF/16V /M.2/X
ASUSTek Computer Inc.
Title : AM4-20
Engineer: Elainelx_Li
Size A3
Project Name AM4
Rev 0.01
Date: Wednesday, August 29, 2018
Sheet 64 of 117

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 66 of 117	



GPP_G0: 4* X1

GPP_G1: 1*X4

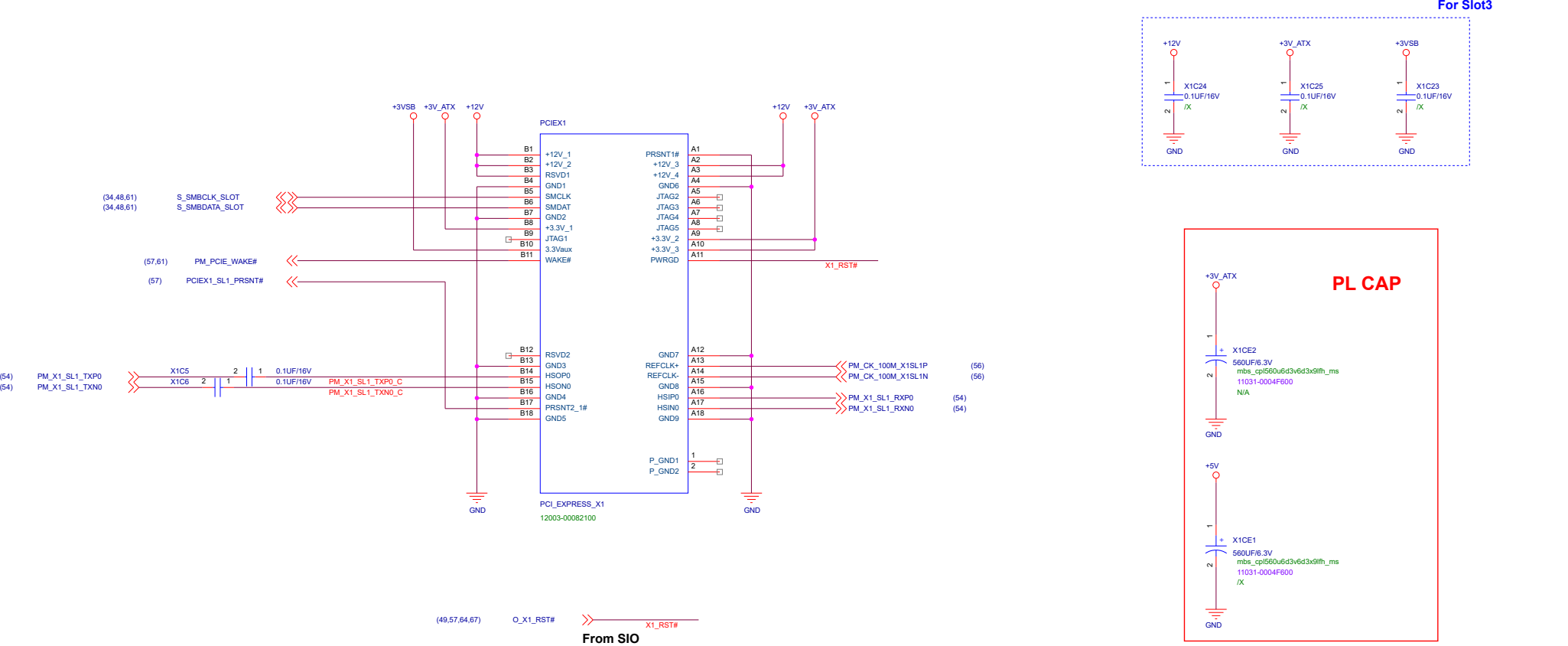


TESTEN	Test mode enable 1: Test mode 0: Function mode
IFDET1	SATA Express port1 1: PCIe mode; 0: SATA mode
IFDET0	SATA Express port0 1: PCIe mode; 0: SATA mode
DEBUG_ENABLE	1:; Debug mode 0: Function mode
TCK (DEBUG_SEL1) TDO (DEBUG_SEL0)	11: Debug signal group 3 output 10: Debug signal group 2 output 01: Debug signal group 1 output 00: Debug signal group 0 output
UART_TX (GPP_G1_SET1) SPI_SDI (GPP_G1_SET0)	GPP Group1 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved
SPI_SDO (GPP_G0_SET1) SPI_SCK (GPP_G0_SET0)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved

GPIO_R4	1: GPP clock source from APU_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO_R8
GPIO_R5	1: USBC SSC disable 0: USBC SSC enable
GPIO_R6	1: SATA SSC disable 0: SATA SSC enable
GPIO_R7	1: SATA Express SSC disable 0: SATA Express SSC enable
GPIO_R8 (enabled from GPIO_R4)	1: GPP SSC disable 0: GPP SSC enable
GPIO_R11	1: GPP clock output enabled 0: GPP clock output disabled

UART_TX	PCIe Group 1 configuration: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	PCIe Group 1 configuration: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
SPI_SDI	PCIe Group 1 configuration: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	PCIe Group 1 configuration: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
SPI_SDO	PCIe Group 0 configuration: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	PCIe Group 0 configuration: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
SPI_SCK	PCIe Group 0 configuration: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	PCIe Group 0 configuration: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
DEBUG_ENABLE	Debug Mode: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	Function Mode (default): Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
TESTEN	TEST mode enable: Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	Function Mode (default): Pull-down resistor to VSS is implemented of value:	1	1 k	Ω

GPIO_R[4]	GPP clock source from APUCLK implemented (default): Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	GPP clock source from Crystal Implemented: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[5]	USB SSC disable implemented (default): Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	USB SSC enable Implemented: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[6]	SATA SSC disable implemented (default): Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	SATA SSC enable Implemented: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[7]	SATA Express SSC disable implemented (default): Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	SATA Express SSC enable Implemented: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[8]	GPP SSC disable implemented (default): Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	GPP SSC enable Implemented: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[9]	Whole Chip SSC disable implemented (default). Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	Whole Chip SSC enable implemented. Pull-down resistor to VSS is implemented of value:	1	1 k	Ω
GPIO_R[11]	GPP Clock Output enable: (default). Pull-up resistor to VCC33 is implemented of value:	1	200 k	Ω
	GPP Clock Output disable: Pull-down resistor to VSS is implemented of value:	1	1 k	Ω



ASUSTek Computer Inc.	Title : PROM-09	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Wednesday, August 29, 2018	Sheet 62 of 117	

COM PORT

COM Circuit

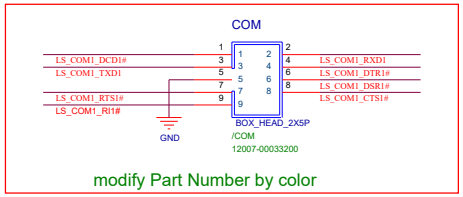
A. Choose COM Port Connector/Header Type

B. Choose use RI# to do Deep S4/S5 wake-up or not by Project

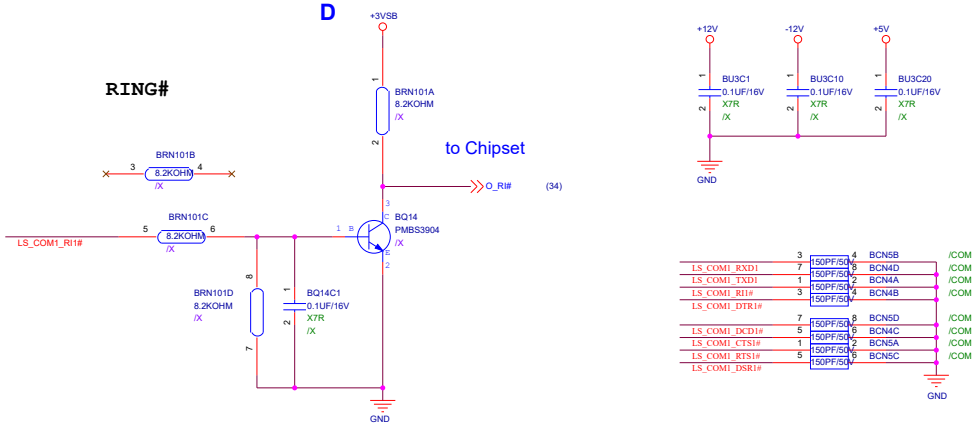
C. Modify Part Number of COM Connector/Header by Color

D. Modify O_RI# pill-high power by Project

A.1 COM Box Header

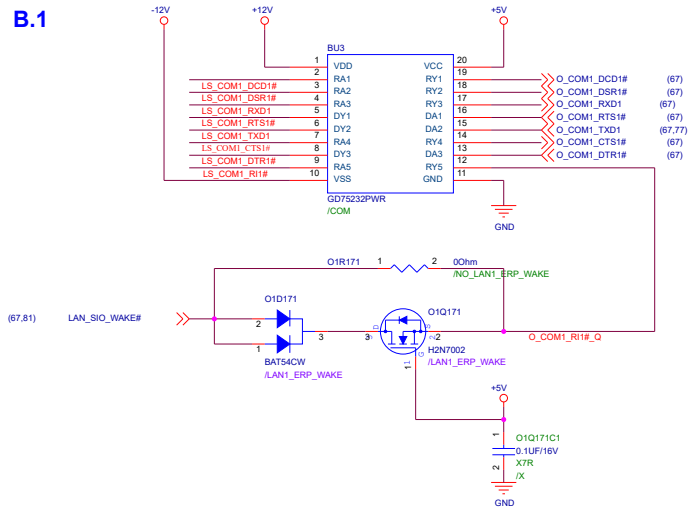


D



for use COM Port RI# to do Deep S4/S5 wake-up function
modify SIO RI# Pin net name to LAN_SIO_WAKE#

B.1



When mount /COM

LAN Deep S4/S5 wake-up	O1R171	O1Q171 & O1D171
support	unmount	mount
not support	mount	unmount

When unmount /COM

LAN Deep S4/S5 wake-up	O1R171	O1Q171 & O1D171
support	unmount	unmount
not support	unmount	unmount

BOM	need COM Port	no COM Port
/COM	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : COM

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 68 of 117

EATX Power Circuit

A. Choose EATX Power Circuit by Project

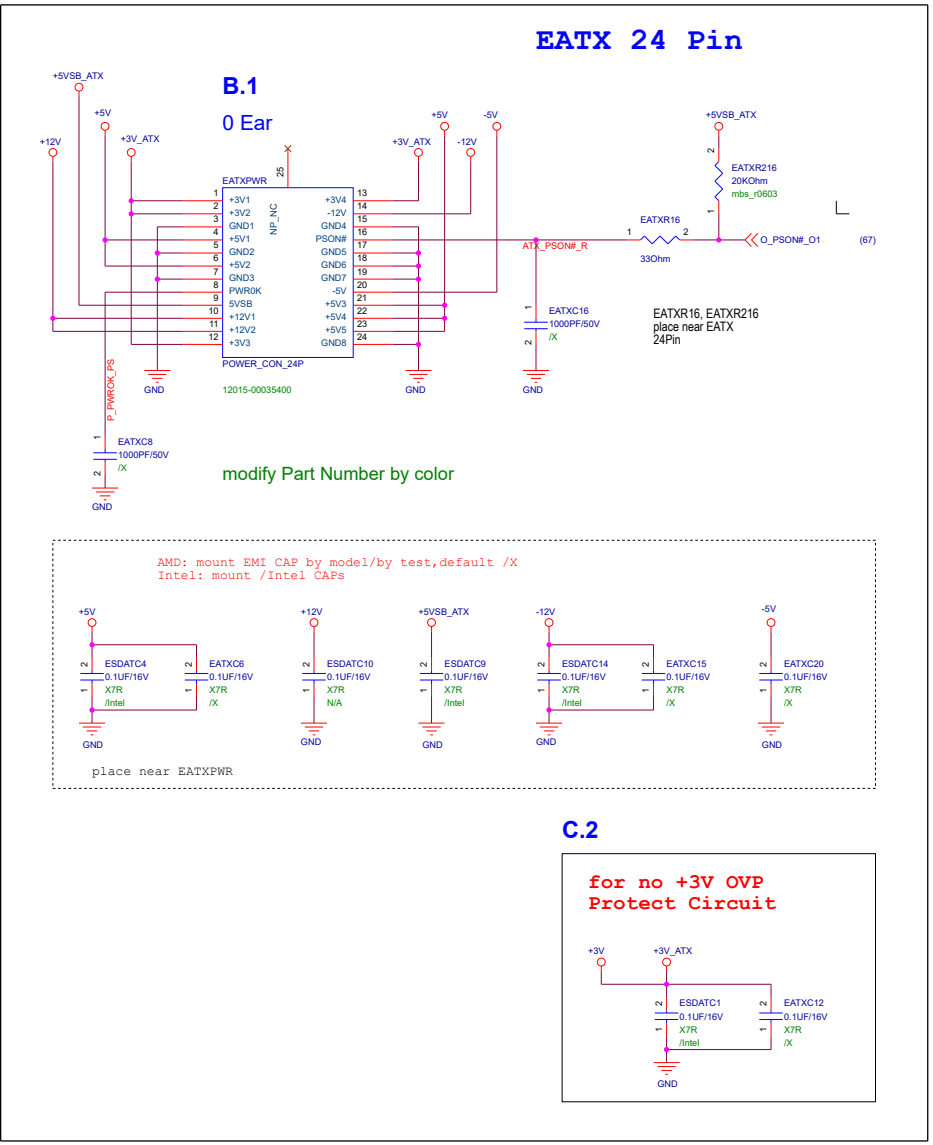
B. If choose EATX 24Pin Circuit, choose EATX Connector with 0 Ear, 1 Ear or 2 Ears by Project

C. If choose EATX 24Pin Circuit, choose +3V_ATX & +3V Circuit by Project

D. If support Intel S0ix, add SC945, SC946 & Off-Page Net O_PSON#_O1 change to ATX_PSON#

E. Modify Part Number of EATX Connector by Color

A.1



<Variant Name>

ASUSTEK COMPUTER INC	Title : EATX	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 70 of 117	

IT8655E Circuit

A. Delete LPC Bus Signal Pull High Resistor if don't need

B. Delete Pin 20 KBRST# Circuit if not connect KBRST# to Chipset

C. Delete O_CASEOPEN# off-page if not used

D. Delete COM1 Port Signal if don't need, but keep Strapping Pin Signal

E. Modify FAN IN/PWM Signal by Project

F. If use COM Port RI# do Deep S4/S5 wake-up, modify Pin 60 net name to LAN_SIO_WAKE#

G. Delete AUDIO_LED_PWM Signal if don't need

H. If SIO Breathing LED is reserved, unmount AUDIO_LED_PWM pull high resistor

I. Add COM Debug Signal by Project, choose GPIO by mapping table

J. Add OVT#/SMI# Signal by Project, choose GPIO by mapping table

K. Add BEEP Signal by Project, choose GPIO by mapping table

L. If use MS as FAN or GPIO, remove pull high resistor ORN404A/ORN404D

M. If use SIO Anti Surge Function, mount O1C32, O1C34

N. Choose RSMRST# Circuit by Project

IT8655E FAN Header Pin Table for AMD AM4

SIO FAN	FAN IN	FAN PWM	FAN Header
FAN1	Pin 64	Pin 1	CPU_FAN
FAN2	Pin 2	Pin 3	CHA_FAN/CHA_FAN1
FAN3	Pin 4	Pin 5	CHA_FAN2
FAN4	Pin 40	Pin 39	CHA_FAN3

FAN Net Name Table

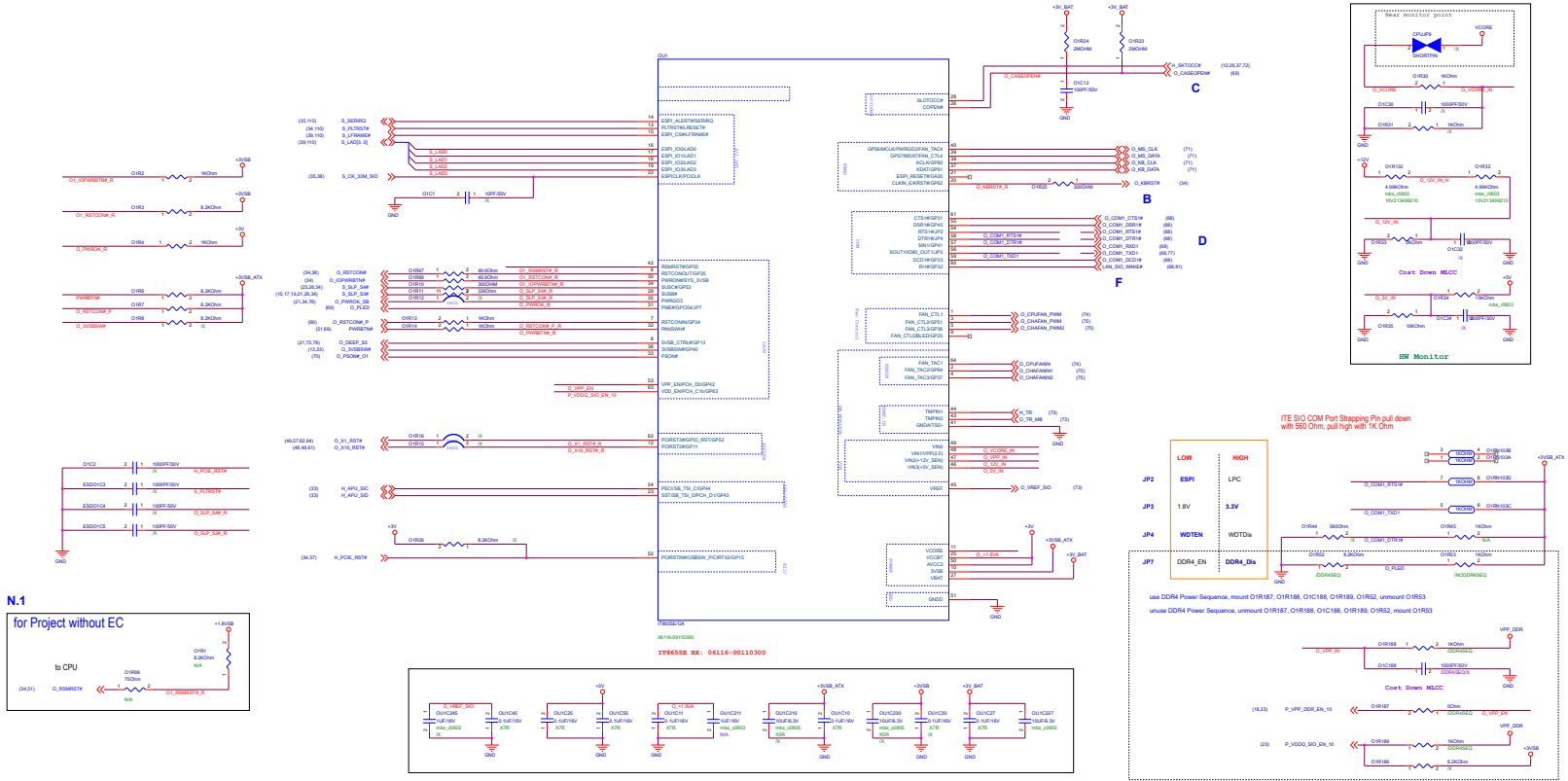
FAN	FAN IN	FAN PWM
CPU_FAN	O_CPUFANIN	O_CPUFAN_PWM
CPU_OPT	O_CPUOPTIN	
CHA_FAN/CHA_FAN1	O_CHAFANIN1	O_CHAFAN_PWM
CHA_FAN2	O_CHAFANIN2	O_CHAFAN_PWM2
CHA_FAN3	O_CHAFANIN3	O_CHAFAN_PWM3
CHA_FAN4	O_CHAFANIN4	O_CHAFAN_PWM4
AIO_PUMP	O_AIO_PUMP_FANIN	O_PUMP_PWM
W_PUMP+	O_PUMP_FANIN	
M.2_FAN	O_M2_FANIN	O_M2_FAN_PWM

IT8655E VIN Table

SIO VIN	VIN0	VIN1	VIN2	VIN3
VIN IN	VCORE	VPP_DDR	+12V	+5V

IT8655E TIN Table

SIO TIN	TMPIN1	TMPIN2
TIN IN	CPU	MB



BOM	use SIO DDR4 Sequence	unuse SIO DDR4 Sequence
/DDR4SEQ	mount	unmount
/NODDR4SEQ	unmount	mount

BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT

Title :	IT8655E_AMD	
ASUSTeK COMPUTER INC	Engineer:	SZ Design IP
Size: Custom	Project Name:	Super I/O Demo Circuit
Date: Wednesday, August 29, 2018	Sheet: 67 of 100	Rev: 0.0

KBMS Circuit

A. Choose KBMS Power Source by Project

B. If KBMS share power with USB Port, modify Share Power Net Name by Project

C. Choose KBMS Port Connector by Project

D. If choose KBMS Connector, KBMS Signal to-GND Cap choose Single Capacitor or RES Cap by Project

E. If choose KB & USB 2.0 Connector, check USB 2.0 Port D+/D- Signal begin with 0 or 1, then modify USB 2.0 Port D+/D- Signal Net Name by Project

F. If choose KB & USB 3.0 Connector, modify USB Port TX/RX/D+/D- Signal Net Name by Project

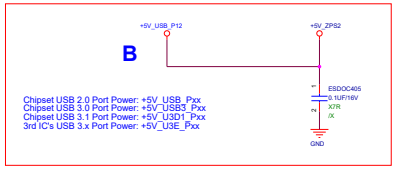
G. If choose KB & USB Connector, modify USB Port Power Net Name by Project

H. If choose KB & USB Connector, modify Connector Part Reference by Project

I. If choose KB & USB Connector, for ITE SIO, ORN404 could /X for cost down

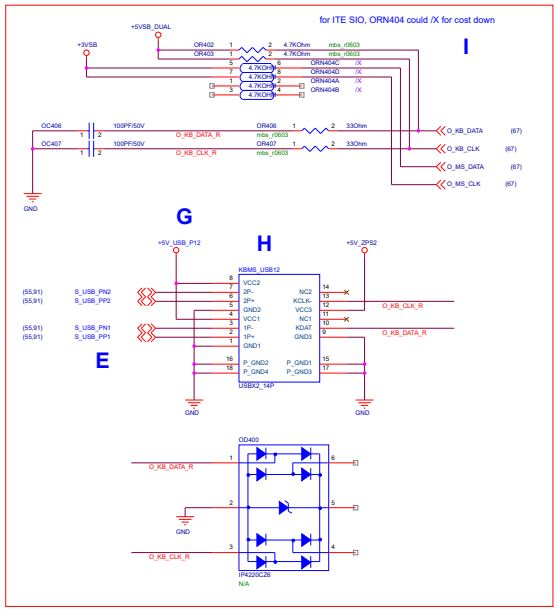
A.1

share USB Port Power



C.3

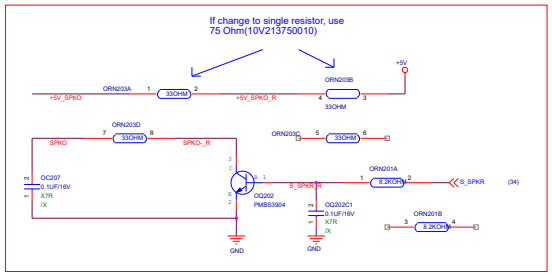
KBMS_USB910



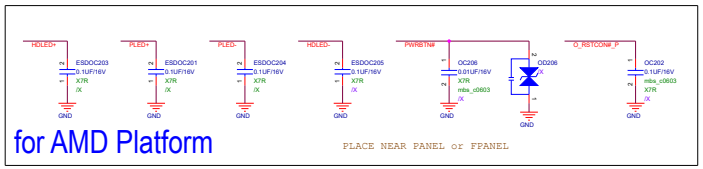
Panel Circuit

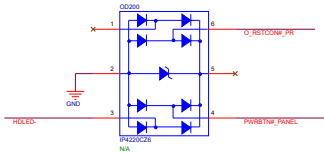
A. Choose PANEL/F_PANEL Signal ESD Solution by Project
B. Choose PANEL/F_PANEL Circuit + Chassis Inturder Circuit by Project
C. Choose Chassis Inturder Signal connect to SIO or Chipset by Project
D. Choose SPEAKER Header Circuit + BUZZER Circuit by Project
E. Choose PLED Circuit by Project
F. Choose PLED control by SIO or Chipset
G. If use Memory Power control PLED, check Memory Power Net Name
H. Modify Part Number of PANEL/F_PANEL/SPEAKER Header by Color

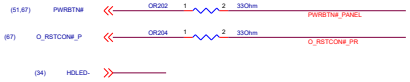
D.1



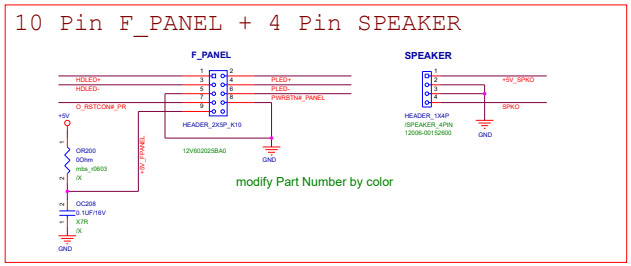
A.2

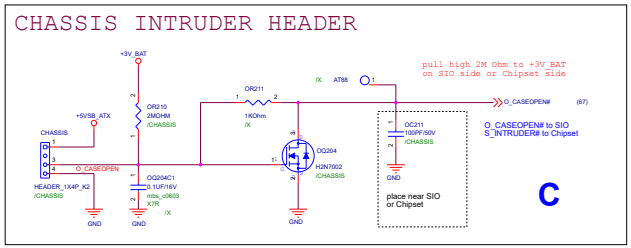






B.1





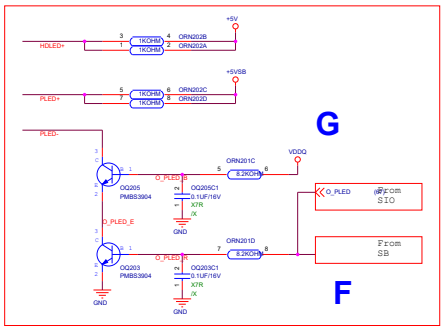
BOM	need SPEAKER	no SPEAKER
/SPEAKER_4PIN	mount	unmount

BOM	need BUZZER	no BUZZER
/BUZZER	mount	unmount

BOM	need CHASSIS	no CHASSIS
/CHASSIS	mount	unmount

E.1

Power LED power source use +5VSB



O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI(no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. Porting Guide: default keep GPI, enable blink 0.5Hz or 1Hz function when enter S3, disable blink function and back to GPI when resume from S3

<Variant Name>

ASUSTEK COMPUTER INC	Title : PANEL	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet: 69 of 117	

Debug Header Circuit

A. Choose Debug Header by Project

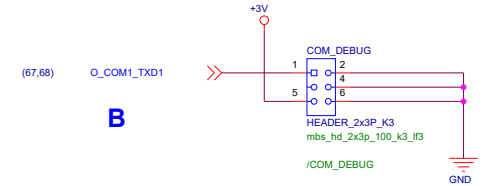
B. If choose COM Debug Header, take care Debug Signal Net Name is different by Project

C. If choose LPC Debug Header, modify Clock Signal Net Name by Project

A.1

Delete it for EMS

COM Debug Header



COM Debug Signal share Nuvoton & ITE SIO COM1 TX Signal

BOM	need COM Debug Header	no COM Debug Header
/COM_DEBUG	mount	unmount

BOM	need LPC Debug Header	no LPC Debug Header
/LPC_DEBUG	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : Debug Header

Engineer: SZ Design IP

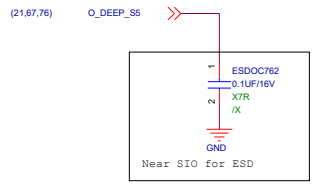
Size	Project Name	Rev
B	Super I/O Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 77 of 117

ERP Circuit

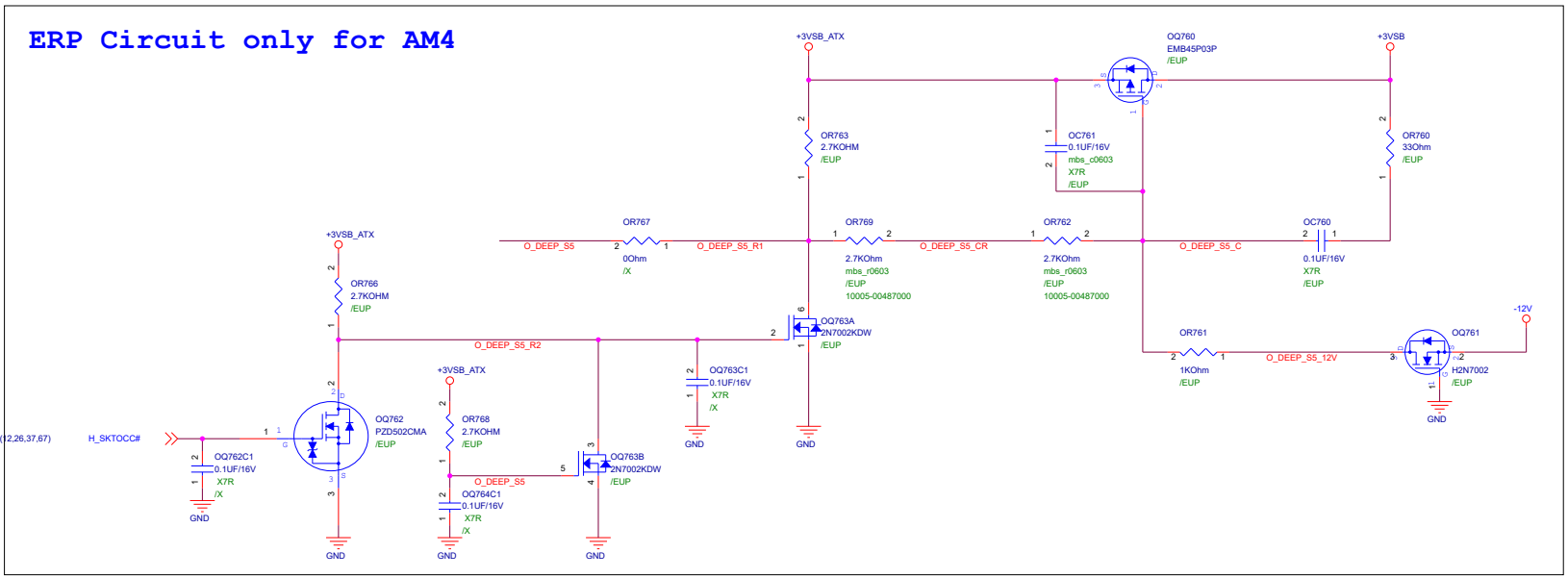
A. Choose ERP Circuit by Project

B. OR764, OR765 choose Short-Pin, Resistor or delete by Project

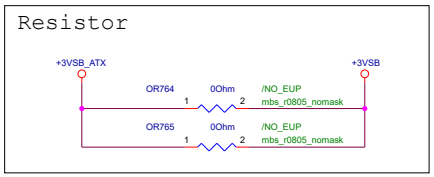


BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
/NO_EUP	mount	unmount	unmount
/EUP	unmount	mount	mount
/NO_SIODSW	mount	mount	unmount
/SIODSW	unmount	unmount	mount

A.3



B.2



<Variant Name>

ASUSTEK COMPUTER INC

Title : ERP

Engineer: SZ Design IP

Size	Project Name	Rev
Custom	Super I/O Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 72 of 117

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 78 of 117	

CHA_FAN Circuit use Single Resistor

A. Choose QFAN Mode Type by Project

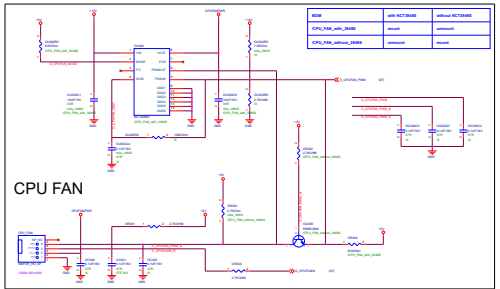
B. If choose PWM Mode, choose with FAN RGB Header or not by Project

C. Remove CPU_OPT if don't need

D. Choose O_PWROK or O_PWROK_SB by Platform for FAN Expert 3 and above Mode

E. Modify Part Number of CPU_FAN & CPU_OPT by Color

PWM Mode with FAN RGB Header for AM4 **B.2**



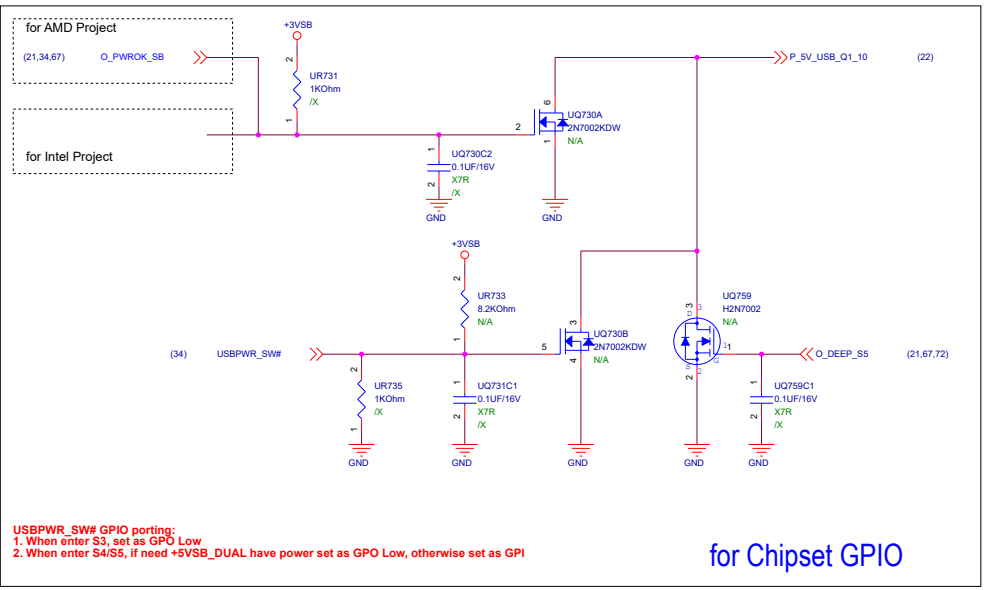
USBPWR_SW# Circuit for ITE SIO GPIO

A. Choose USBPWR_SW# Circuit by Project

USBPWR_SW# GPIO select:
1. could be GPI & GPOD both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance

A.1

+5VSB_DUAL default no power, reserve USB Inrush Circuit



USBPWR_SW# GPIO porting:
1. When enter S3, set as GPO Low
2. When enter S4/S5, if need +5VSB_DUAL have power set as GPO Low, otherwise set as GPI

for Chipset GPIO

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB Power Control

Engineer: SZ Design IP

Size	Project Name	Rev
Custom	Super I/O Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 76 of 117

Stand By LED & HW Monitor Circuit

A. Choose Stand By LED Circuit by Project

B. Keep or delete TR_PCH Circuit by Project

C. Keep or delete T_SENSOR Circuit by Project

D. Keep or delete VCORE Power Controller TEMP Detect Circuit by Project

E. Keep or delete GFX Power Controller TEMP Detect Circuit by Project

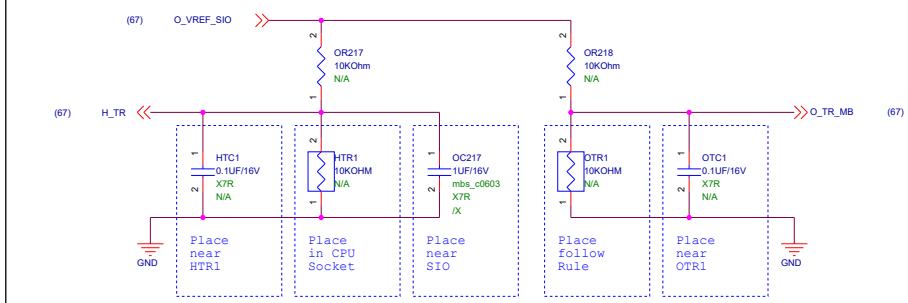
F. Modify Part Number of T_SENSOR Header by Color

BOM	need Stand By LED	no Stand By LED
/StandByLED	mount	unmount

BOM	need TR_PCH	no TR_PCH
/TR_PCH	mount	unmount

BOM	need T_SENSOR	no T_SENSOR
/T_SENSOR	mount	unmount

HW Monitor



If no CPU thermistor, unmount components HTR1, HTC1, OR217

If no MB thermistor, unmount components OTR1, OTC1, OR218

<Variant Name>

ASUSTEK COMPUTER INC

Title : SBLED_HWM

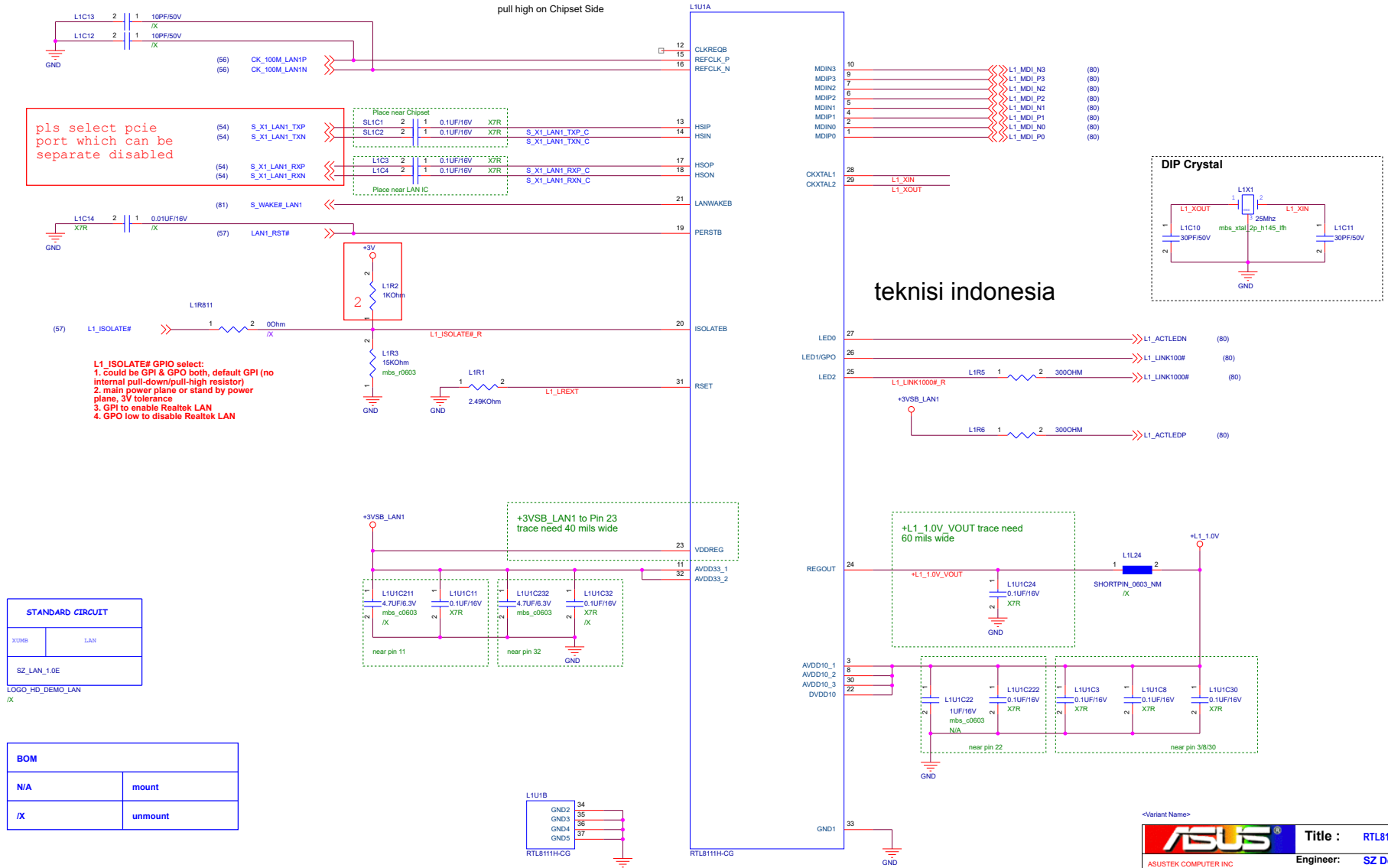
Engineer: SZ Design IP

Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 73 of 117

RTL8111H Circuit

1. If support Deep S4/S5 wake-up, rename S_WAKE# to S_WAKE#_LAN1
2. Modify PCIE Reset Signal Net Name by Project
3. Choose Crystal Type by Project
4. Check +3VSB_LAN1 Power Source by Project,
5. Delete CLKREQ#_LAN1 if not need
6. select block 1 or 2 according to if you support S0IX



STANDARD CIRCUIT	
XUMB	LAN
SZ_LAN_1.0E	

LOGO_HD_DEMO_LAN
/X

BOM	
N/A	mount
/X	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : RTL8111H

Engineer: SZ Design IP

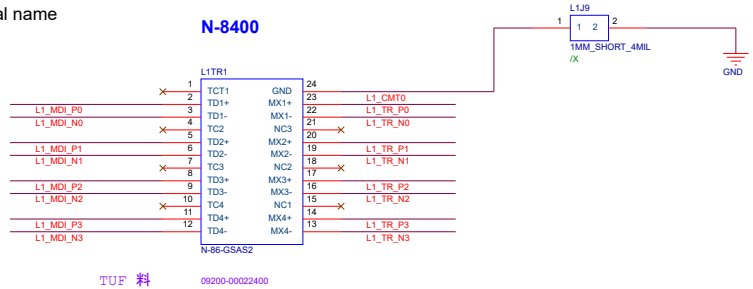
Size	Project Name	Rev
A3	LAN Demo Circuit	0.0

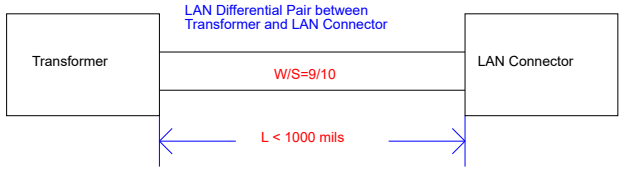
Date: Wednesday, August 29, 2018 Sheet 79 of 117

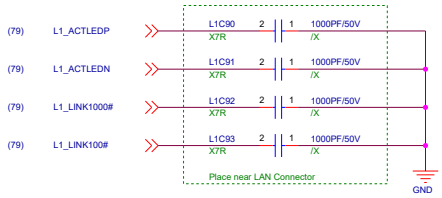
1. change LAN_USB12 name ,part, partnumber to what you want,copy from page24

2. change vbus source name

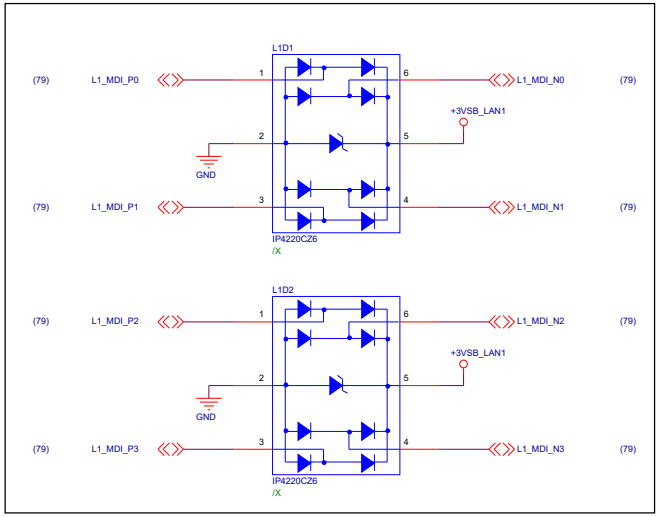
3. change usb signal name





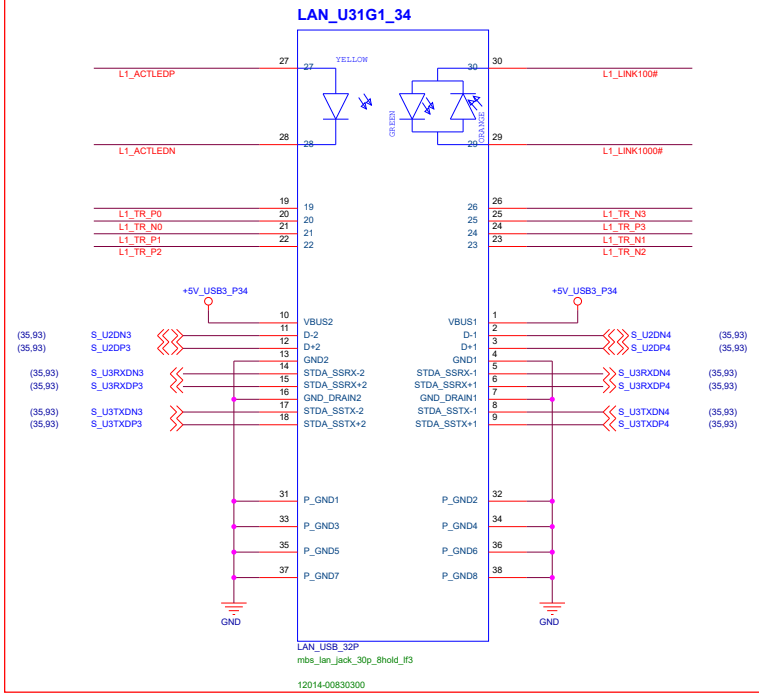


Delete it for EMS



GLAN + USB31G1 *2 Connector without Transformer

single LAN named LAN_USB31G1_xx
dual LAN named LAN1_USB31G1_xx



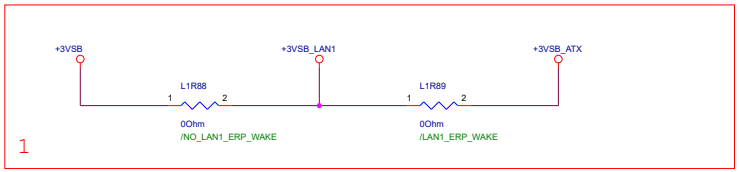
<variant_name>

ASUSTEK COMPUTER INC	Title :	LAN Connector	
	Engineer:	SZ Design IP	
Size: A3	Project Name: LAN Demo Circuit		Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 80 of 117		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 82 of 117	

LAN1 Deep S4/S5 Wake-up Circuit

1. Remove Short-Pin L1R88 in LAN1 IC Page



for Intel PHY

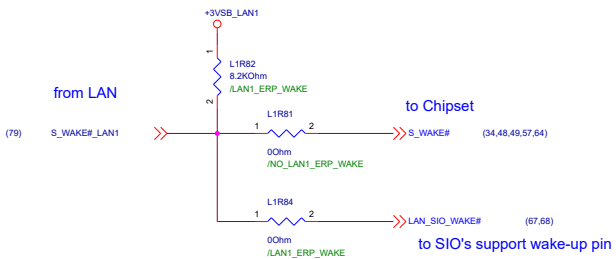
2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN1 IC Page

3. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN1 IC Page

for PCIE LAN1

4. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN1 IC Page

5. for Intel PCIE LAN, make sure L1_DEV_OFF# choose +3VSB_ATX power plane GPIO



<Variant Name>

ASUSTEK COMPUTER INC

Title : Deep S4/S5 Wake

Engineer: SZ Design IP

Size	Project Name	Rev
A3	LAN Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 81 of 117

CHA_FAN PWM Mode & DC Mode QFAN Circuit use Single Resistor

A. Choose QFAN Mode Type by Project

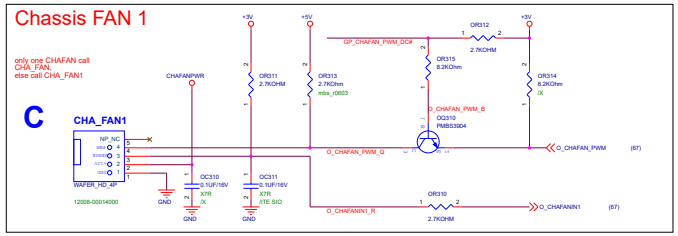
B. Remove the CHA_FAN which don't need

C. If only one CHA_FAN, rename CHA_FAN1 to CHA_FAN

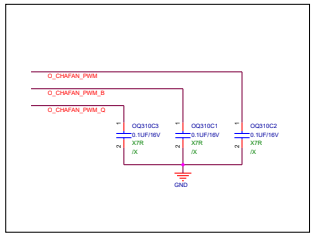
D. Modify Part Number of CHA FAN Header by Color

A.1

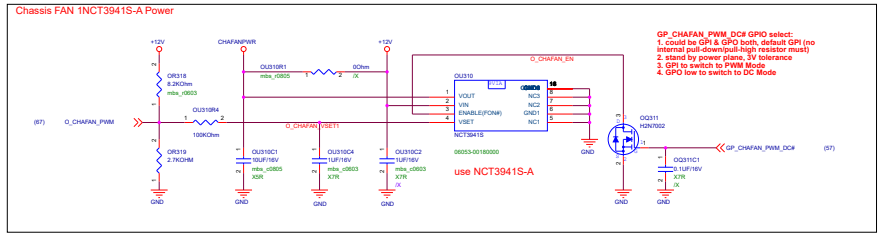
4 Pin PWM Mode & DC Mode

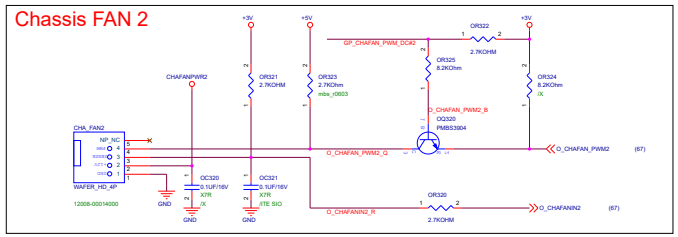


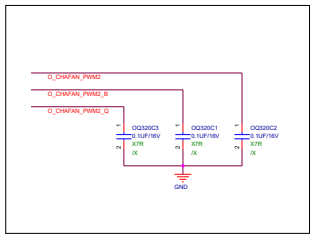
BJT Cap

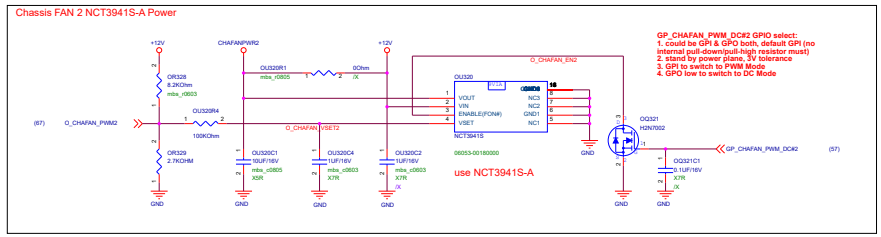


PWM Mode & DC Mode Power Solution





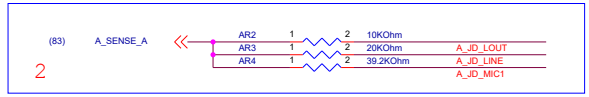




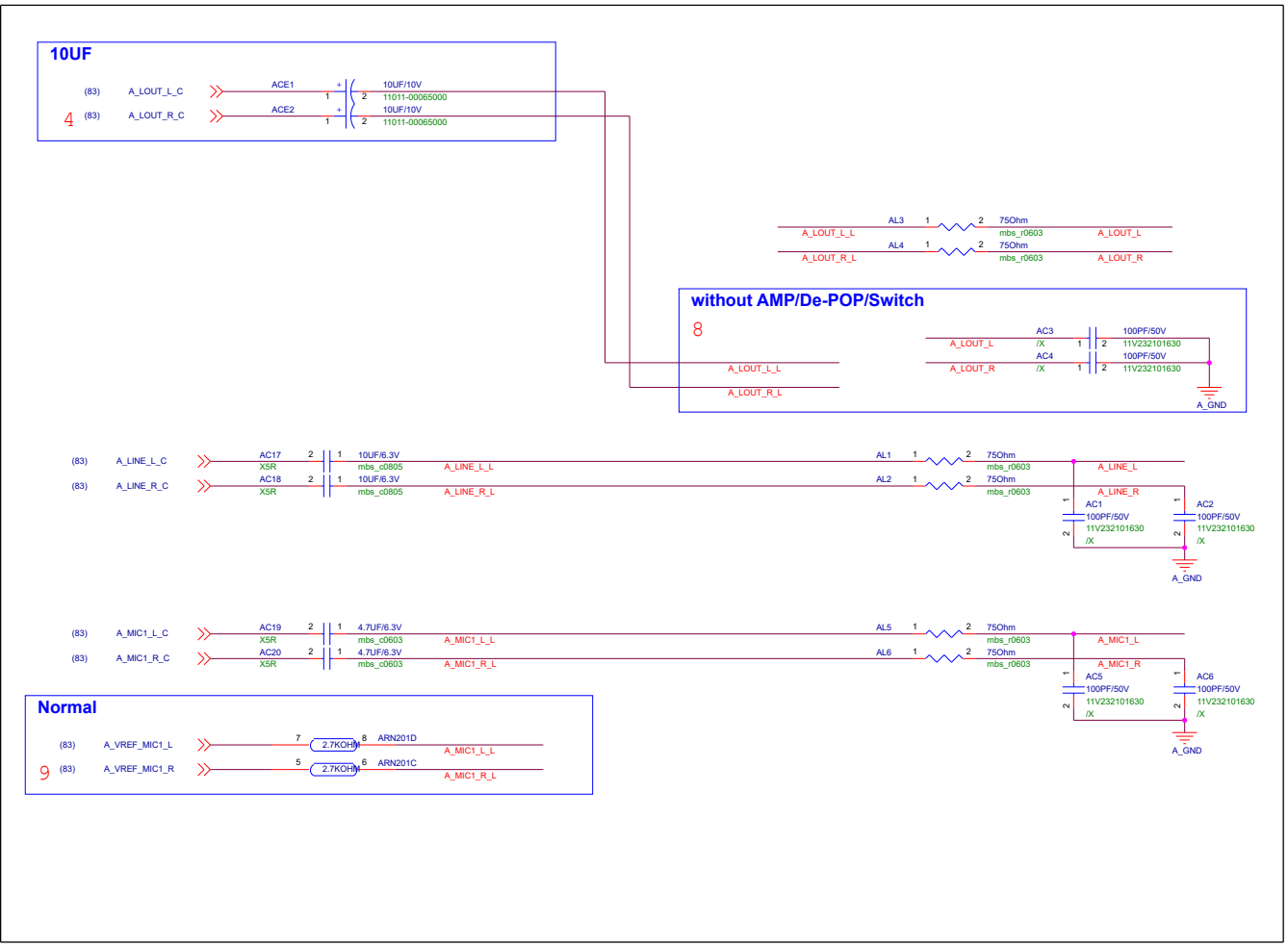
Rear 3Jacks Circuit

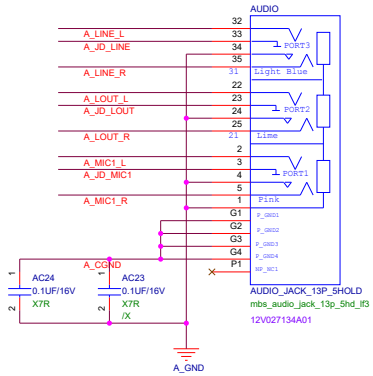
1. Choose Jack Detect Circuit by Codec,block 1,2,3
2. Choose LOUT DIP CAP Type by Codec & Project,block 4,5,6
3. Choose LOUT Circuit with or without De-POP/Switch by Project,block 7,8
4. Modify ACE1, ACE2 Part Number by Project
5. Choose Rear MIC VREF Circuit by Project ,block9,10
6. For Gamer/Gaming modity AC17, AC18 part by request
7 if you use 1220 ,Modify AC1,AC2,AC3, AC4, ,AC5,AC6, Part Number to varistor and Optional to N/A

for ALC1150



Delete it for EMS





Audio CAP using rule,pls change all dip caps partnumber according bellow rule

Z390,B450 ROG / Strix series	Nichicon
Z390,B450 PRIME / TUF Series	ELNA
Intel H310,H310C,H110&AMD A320 series	Chemicon
other chipsets except above series	Nichicon

DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207

Taping DIP CAP
Chemicon 10U T: 11011-00064100
Elan 10U:11011-00065000
Nichicon 10U T: 11011-00066200

DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

AC1, AC2, AC3, AC4, AC5, AC6
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
PL 100U T:11031V0001F400

<Variant Name>

ASUSTEK COMPUTER INC

Title : 3 Jacks

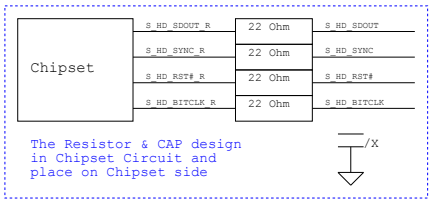
Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 85 of 100

ALC1150 Circuit

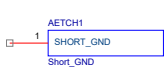
1. Modify IO Power by Project
2. Delete A_SELET_AMP if not need
3. Delete A_EAPD if not need
4. Delete A_SPDIFO_HEADER if not need
5. Delete A_SPDIFO_OPTICAL if not need
6. Delete Side Surround for Rear 3 Jacks or 5Jacks
7. Delete CEN/LFE & Surround for Rear 3 Jacks
8. Modify AU1CE44 Part Number by Project
9. Block 8,9, select one of them according if support s0ix



DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

Taping DIP CAP
PL 100U T:11031V0001F400

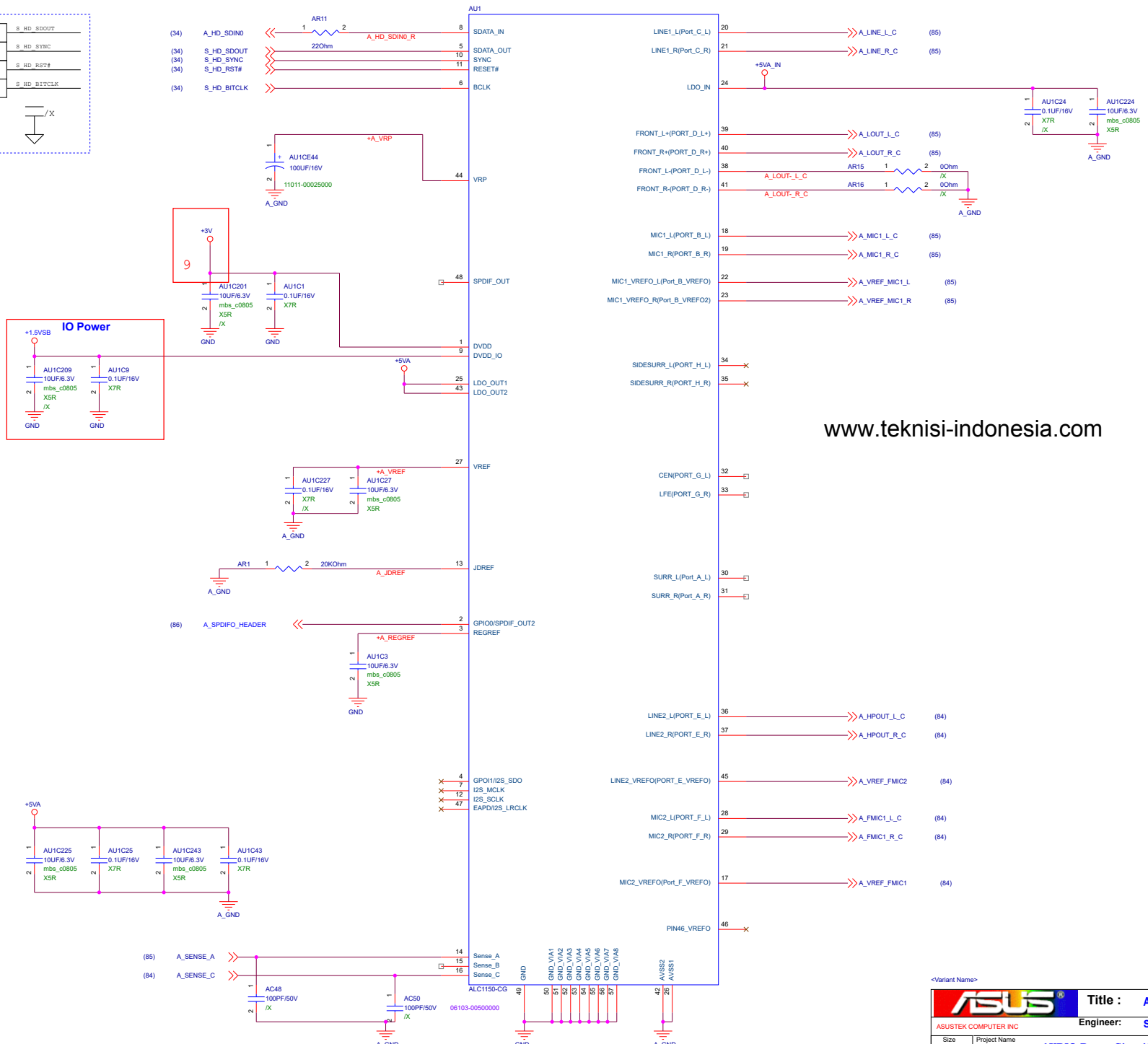
Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200



BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	Audio
SZ_Audio_1.0F	

HD_STANDARD_AUDIO
/X



<Variant Name>

ASUSTEK COMPUTER INC	Title :	ALC1150	
	Engineer:	SZ Design IP	
Size: Custom	Project Name: AUDIO Demo Circuit		Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 83 of 100		

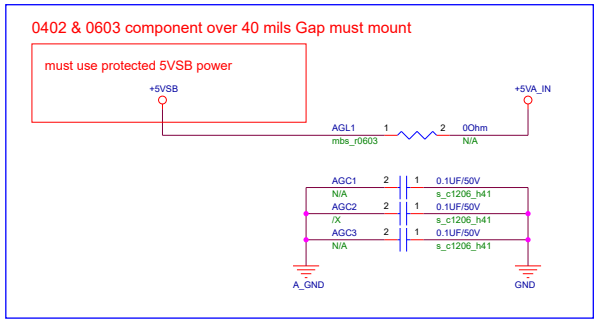
Audio GAP & Power Circuit

1. Choose Resistor & Capacitor over GAP Circuit by Project

2. Keep or delete Audio Power LDO Circuit by Project

3. Modify APCE4 Part Number by Project

40 mils Gap for XU



BOM	Audio Power from 5VSB	Audio Power from 12V LDO 5V
/AUDIO_PWR_5VSB	mount	unmount
/AUDIO_PWR_LDO	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : GAP_Power

Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

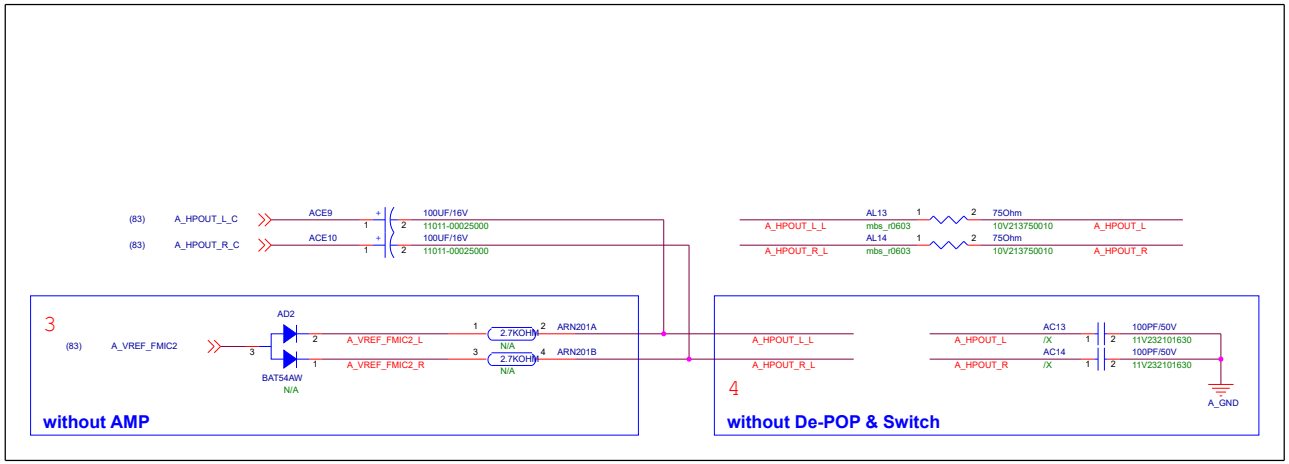
Date: Friday, August 17, 2018 Sheet 87 of 117

AAFP Circuit

1. Choose AAFP Header Circuit by Codec,and change AAFP part number by your request,block 6,7, or 8
2. Choose HP Circuit with or without AMP/De-POP/Switch by Project,block 1,2,3,4
3. Modify ACE9, ACE10 Part Number by Project
4. IF you use 1220, AC13,AC14,AC15,AC16 option must change to N/A and change part number to varistor
5. Modify ARN202 value to 4.7k if you use 887,block 5
6. For Gamer Project with ALC1150, AL13, AL14 change to 47Ohm
7. change AC37,AC38 part number if you have AMP,block 6

AAFP

for ALC887-VD2/ALC892/ALC1150/ALC1220X



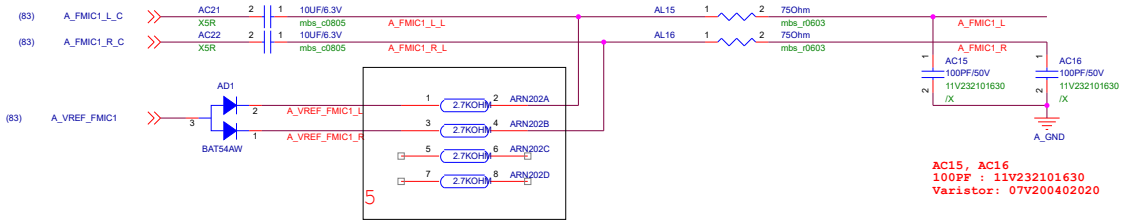
DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010

AC13, AC14
100PF : 11V232101630
Varistor: 07V200402020

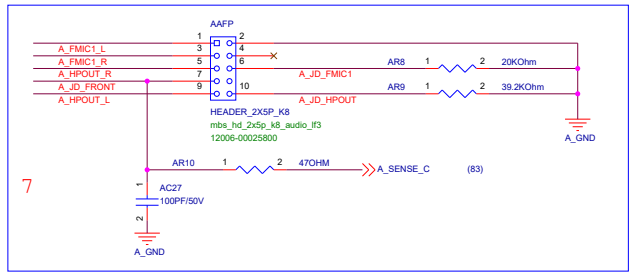
Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

Taping DIP CAP
PL 100U T:11031V0001F400



AC15, AC16
100PF : 11V232101630
Varistor: 07V200402020

for ALC1150



Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : AAFP

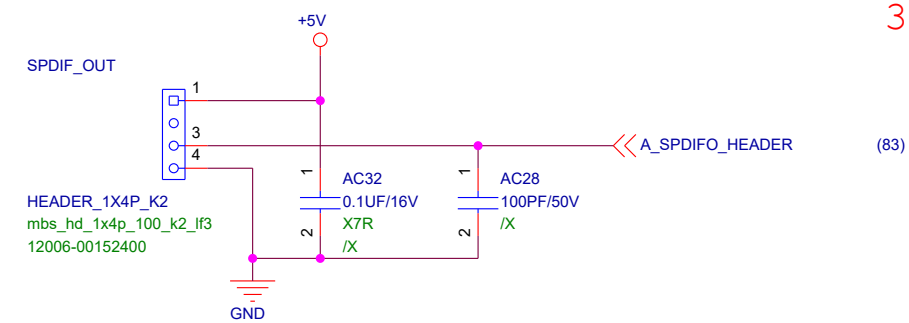
Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 84 of 100

SPDIF

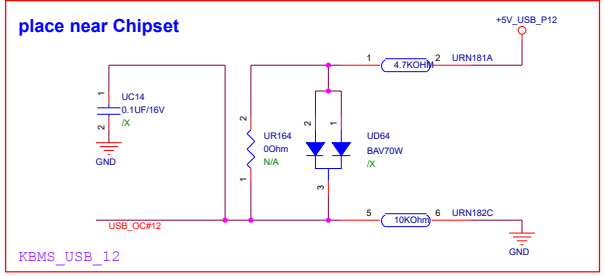
SPDIF Header

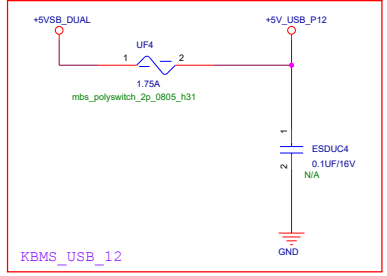


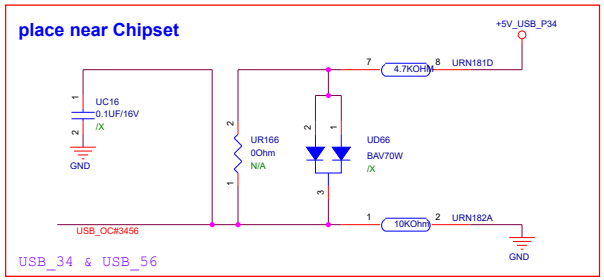
<Variant Name>

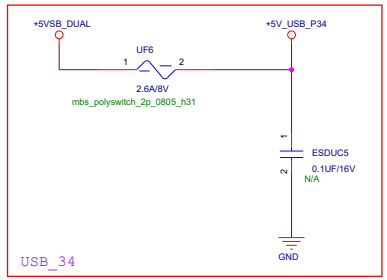
ASUSTEK COMPUTER INC	Title : SPDIF	
	Engineer: SZ Design IP	
Size: A	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 86 of 117	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 89 of 117	

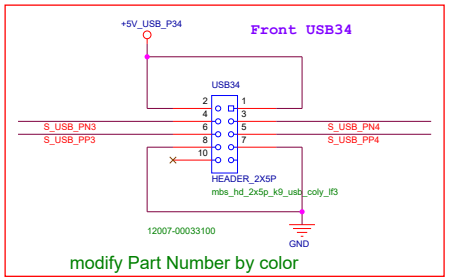




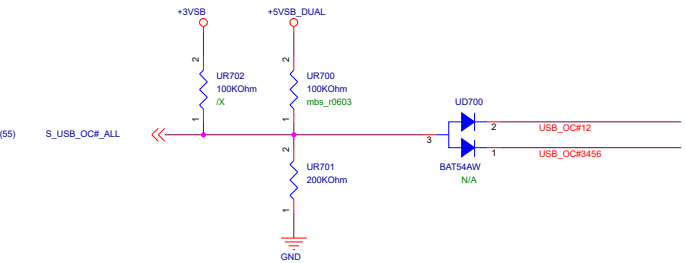


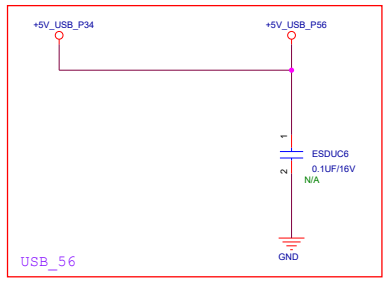


USB2 Header

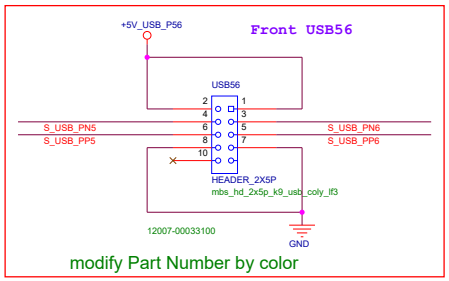


(55,91) S_USB_PN3
(55,91) S_USB_PP3
(55,91) S_USB_PN4
(55,91) S_USB_PP4





USB2 Header



(55,91) S_USB_PN5
(55,91) S_USB_PP5
(55,91) S_USB_PN6
(55,91) S_USB_PP6

<Variant Name>

ASUSTEK COMPUTER INC	Title :	USB2 Port
	Engineer:	Kell_Huang
Size: A3	Project Name:	Chipset USB Demo Circuit
Rev: 0.0		
Date: Wednesday, August 29, 2018	Sheet 90 of 117	

AUDIO COVER

TUF Cover

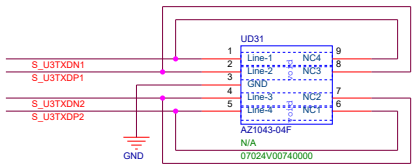
Codec Cover LED

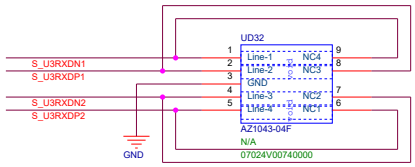
<Variant Name>

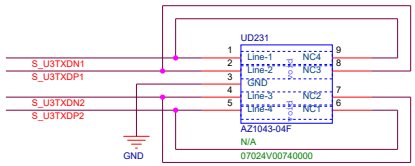
ASUSTEK COMPUTER INC		Title : Cover_LED	
		Engineer: SZ Design IP	
Size: A3	Project Name: AUDIO Demo Circuit		Rev: 0.0
Date: Friday, August 17, 2018		Sheet 88 of 117	

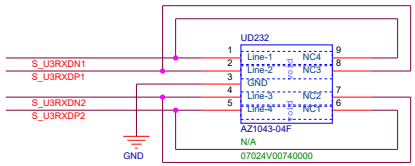
Delete it for EMS

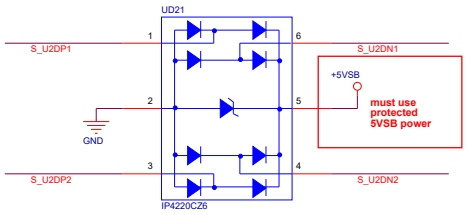
ESD Diode





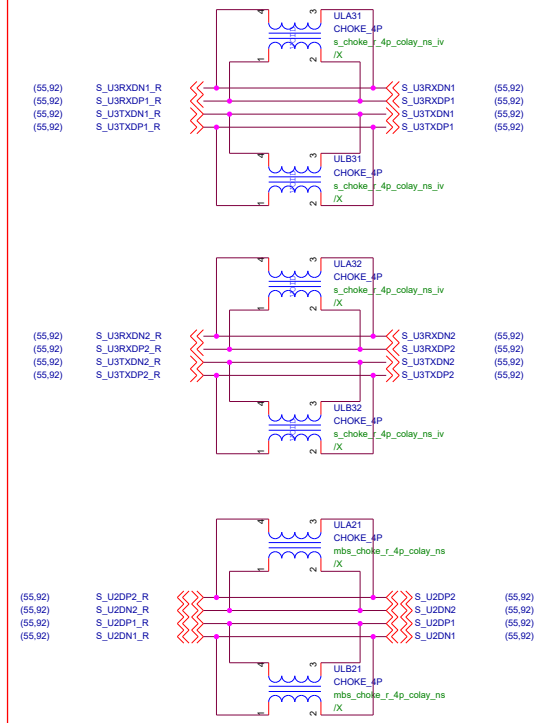






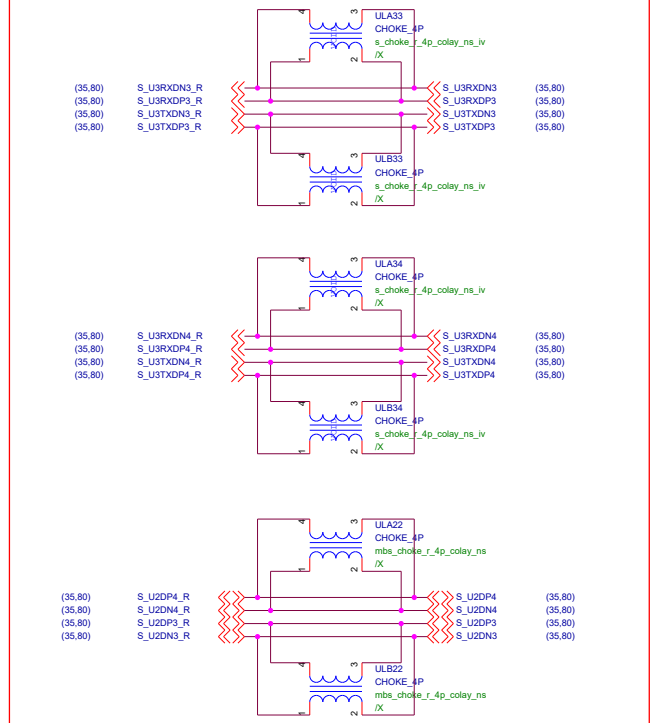
Front U31G1_12

Reserve Location (RES A)



Front U31G1_12

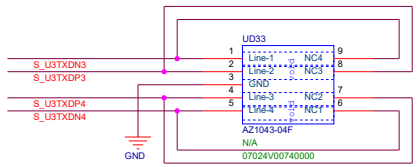
Reserve Location (Single RES)

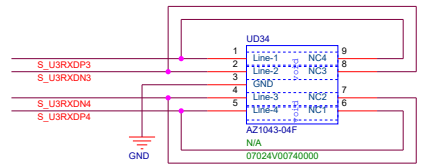


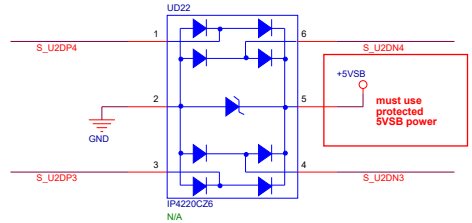
BACK LAN_U31G1_34

Delete it for EMS

ESD Diode







BACK LAN_U31G1_34

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB3 Port

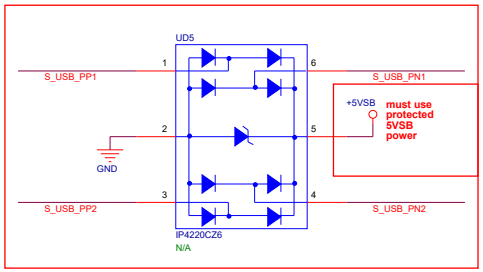
Engineer: Kell_Huang

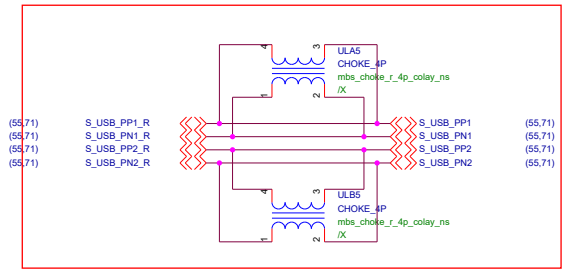
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

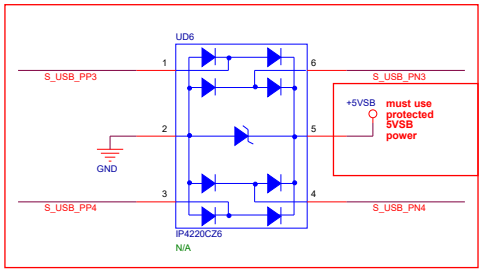
Date: Wednesday, August 29, 2018 Sheet 93 of 117

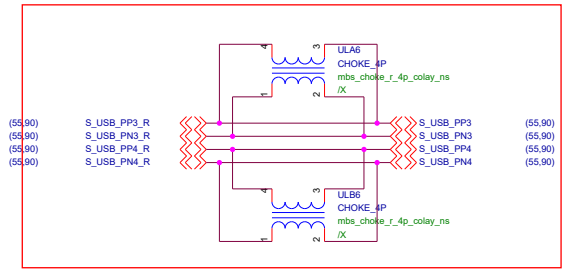
Delete it for EMS

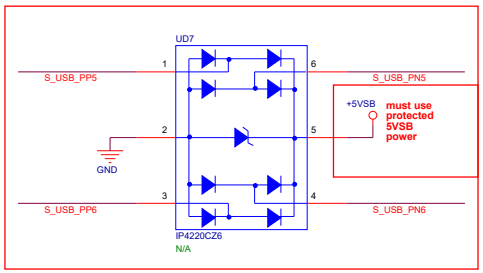
Reserve Location (RES A)

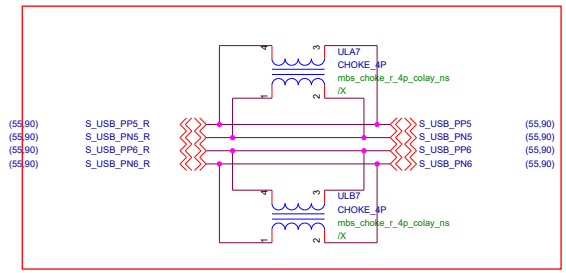












<Variant Name>

ASUSTEK COMPUTER INC

Title : USB2 Port

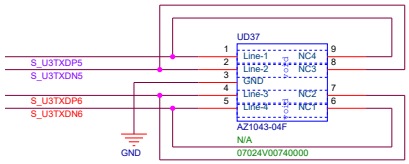
Engineer: Kell_Huang

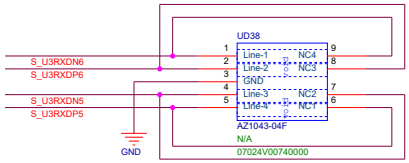
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

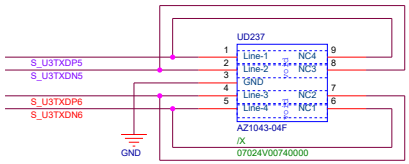
Date: Wednesday, August 29, 2018 Sheet 91 of 117

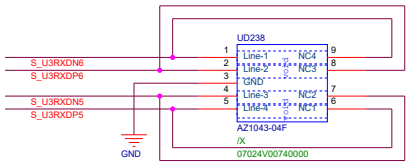
Delete it for EMS

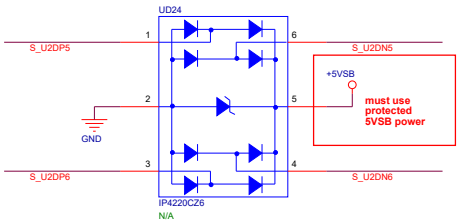
ESD Diode





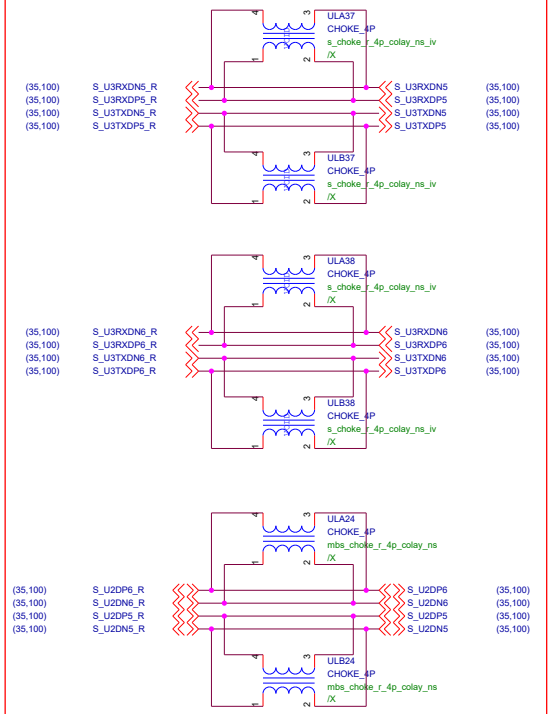






BACK U31G1_C5

Reserve Location (RES A)



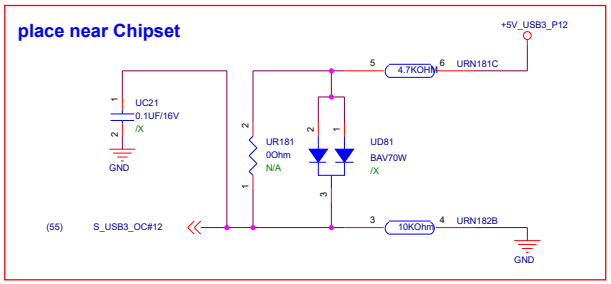
BACK U31G1_C5

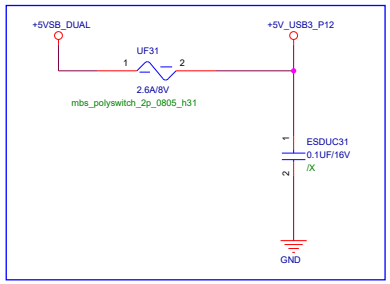
<Variant Name>

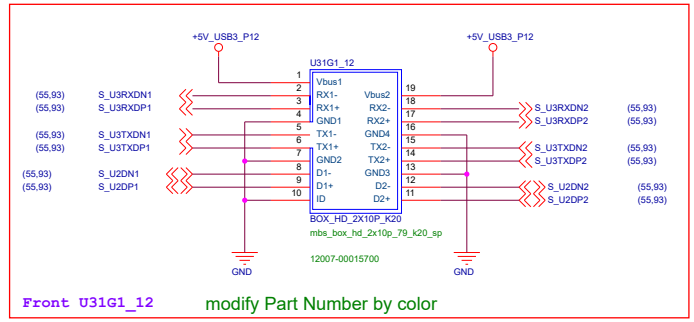
ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 94 of 117	

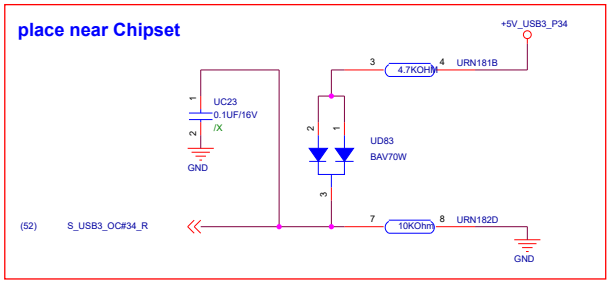
Delete it for EMS

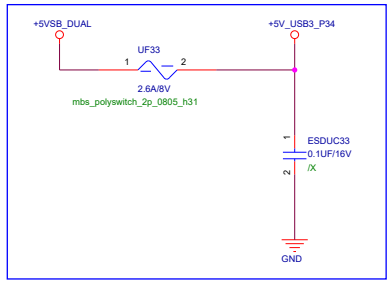
OC# circuit for AMD











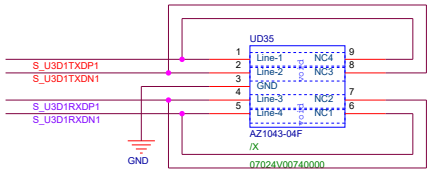
<variant_name>

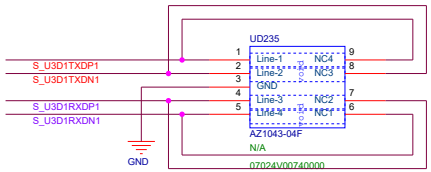
ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 92 of 117	

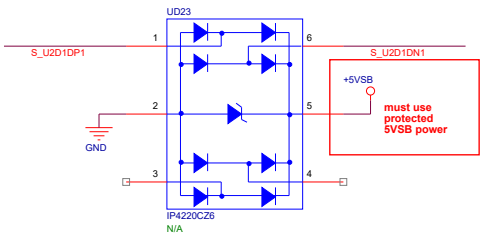
USB3.1Port 12

Delete it for EMS

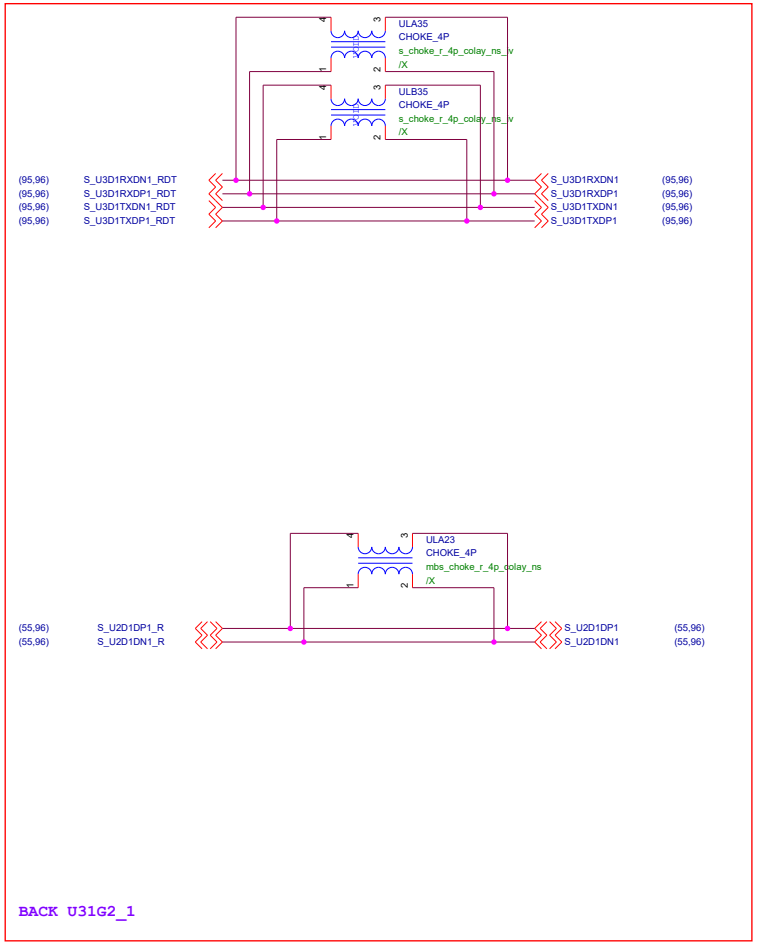
ESD Diode





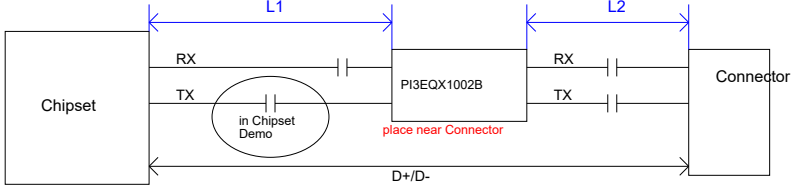


Reserve Location (Single RES)



<variant_name>

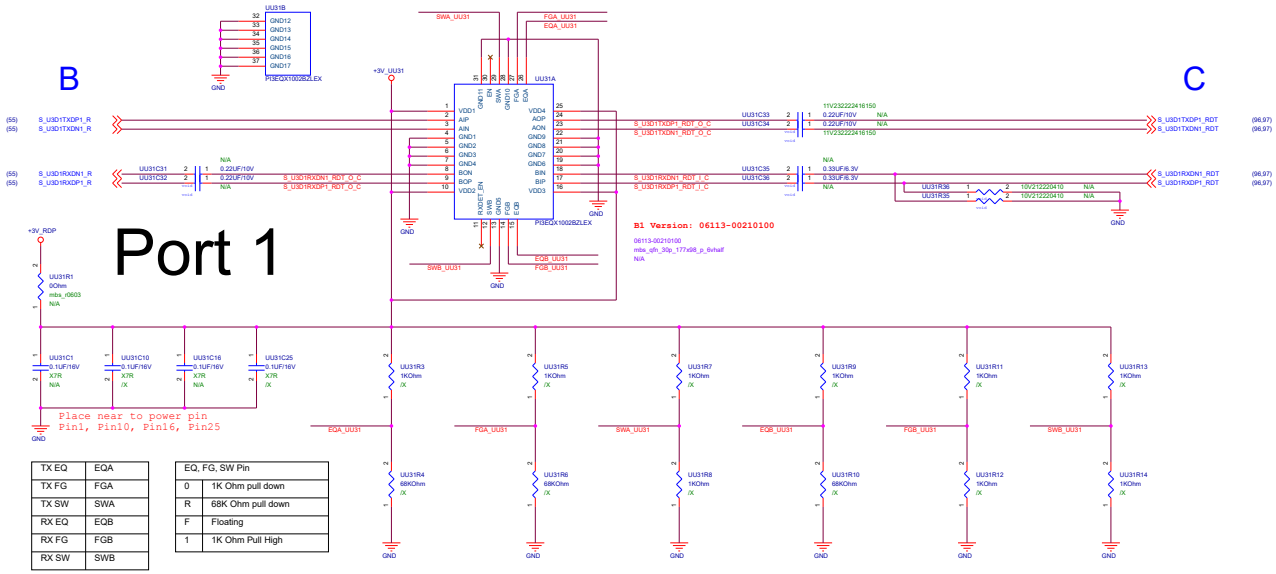
ASUSTEK COMPUTER INC	Title : USB3.1 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 97 of 117	



Net	Impedance/Width	Space	Length
TX/RX L1	follow USB 3.1 Controller Rule	30 mils	< 10", prefer 5" - 9"
TX/RX L2		30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP	>= 20 mils		

EQ/FG Setting Table for Intel Platform	L2 < 2.5"					
	EQA	FGA	SWA	EQB	FGB	SWB
L1 < 7"	R	R	F	R	0	F
7" <= L1 <= 9" (demo default)	F	R	F	R	F	F
9" < L1 < 10"	1	R	F	R	1	F

EQ/FG Setting Table for AMD Platform	L2 < 2.5"					
	EQA	FGA	SWA	EQB	FGB	SWB
L1 < 7"	F	F	F	F	F	F
7" <= L1 <= 9"	F	F	F	F	F	F
9" < L1 < 10"	F	F	F	0	1	F



TX EQ	EQA
TX FG	FGA
TX SW	SWA
RX EQ	EQB
RX FG	FGB
RX SW	SWB

EQ, FG, SW Pin	
0	1K Ohm pull down
R	68K Ohm pull down
F	Floating
1	1K Ohm Pull High

USB 3.1 Re-Driver PI3EQX1002B Circuit

A. Delete the Re-Driver IC which is not needed by Project

B. Modify Input USB 3.1 TX/RX Signal Net Name by Project

C. Modify Output USB 3.1 TX/RX Signal Net Name by Project

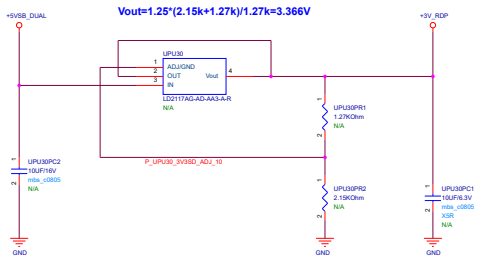
D. If UU31 TX output signals send to ASM1543, UU31C33, UU31C34 change Part Number from 11V232222416150 to 11V232334150 & mount UU31R33, UU31R34, otherwise could delete UU31R33, UU31R34

E. If UU32 TX output signals send to ASM1543, UU32C33, UU32C34 change Part Number from 11V232222416150 to 11V232334150 & mount UU32R33, UU32R34 otherwise could delete UU32R33, UU32R34

F. Modify EQ/FG/SW Pins' pull high/pull down BOM by layout

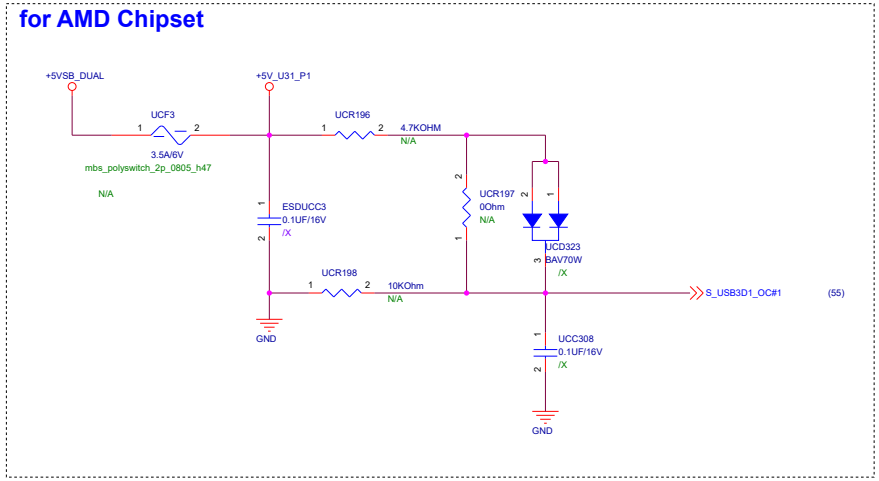
Power Solution for PI3EQX1002B *1/2pcs

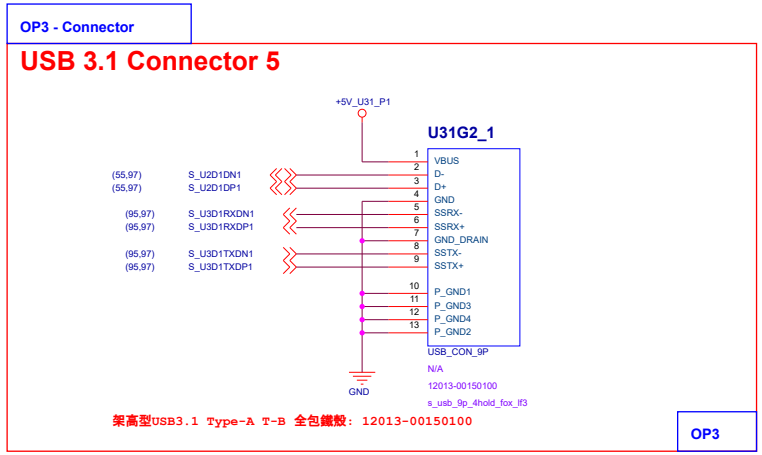
3.3V for PI3EQX1002B, 170mA/pcs@S0



Power Component place near each other!

3.1 Port 12





<variant_name>

ASUSTEK COMPUTER INC

Title : USB3.1 Port

Engineer: Kell_Huang

Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Wednesday, August 29, 2018 Sheet 96 of 117

Two USB 3.x Ports to One Type-C Connector/USB 3.1 Front Header Circuit_1

A. If don't need use or reserve Power Switch to control Type-C Connector Power, delete this block

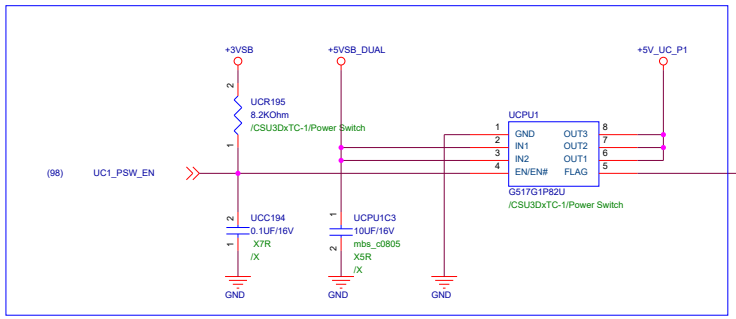
B. Choose OC# Signal Circuit Type

C. Modify OC# Signal Net Name by Project

D. Choose DIP CAP Type

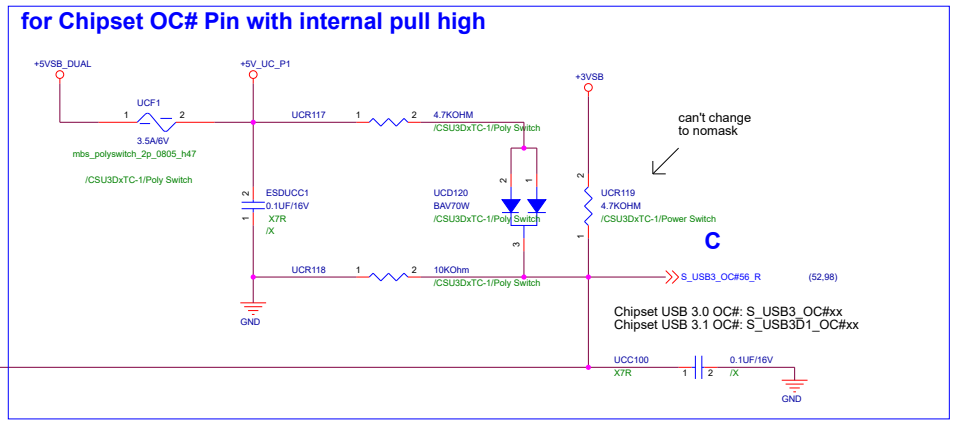
E. Modify Part Number of UCCE1 by Project

A

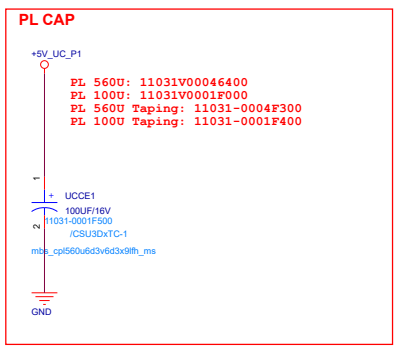


B.2

for Chipset OC# Pin with internal pull high



D.1



BOM	Type-C with Power Switch	Type-C with Poly Switch
/CSU3DxTC-1	mount	mount
/CSU3DxTC-1/Power Switch	mount	unmount
/CSU3DxTC-1/Poly Switch	unmount	mount

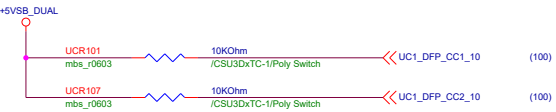
<Variant Name>

ASUSTEK COMPUTER INC	Title :	CS U3.x Type-C
	Engineer:	SZ Design IP
Size: A3	Project Name: Chipset USB Type-C Port	Rev: 1.0D
Date: Wednesday, August 29, 2018	Sheet 99 of 117	

Two USB 3.x Ports to One Type-C Connector/USB 3.1 Front Header Circuit_1

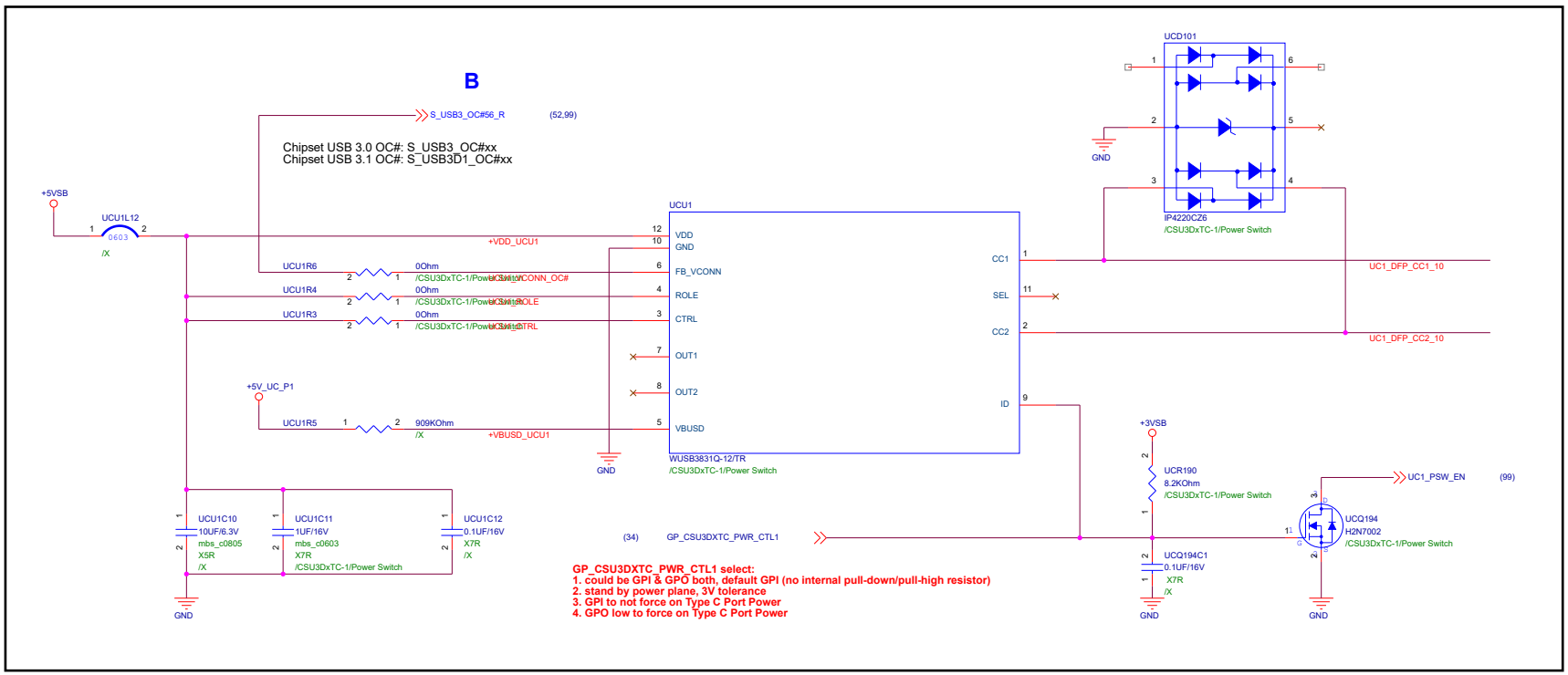
A. If don't need use or reserve Power Switch to control Type-C Connector Power, delete this block

B. Modify OC# Signal Net Name by Project



BOM	Type-C with Power Switch	Type-C with Poly Switch
/CSU3DxTC-1	mount	mount
/CSU3DxTC-1/Power Switch	mount	unmount
/CSU3DxTC-1/Poly Switch	unmount	mount

A



<Variant Name>

ASUSTEK COMPUTER INC

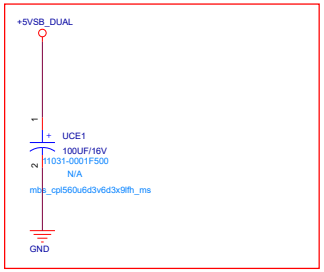
Title : CS U3.x Type-C

Engineer: SZ Design IP

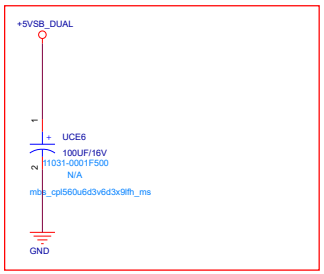
Size	Project Name	Rev
A3	Chipset USB Type-C Port	1.0D

Date: Wednesday, August 29, 2018 Sheet 98 of 117

PL CAP



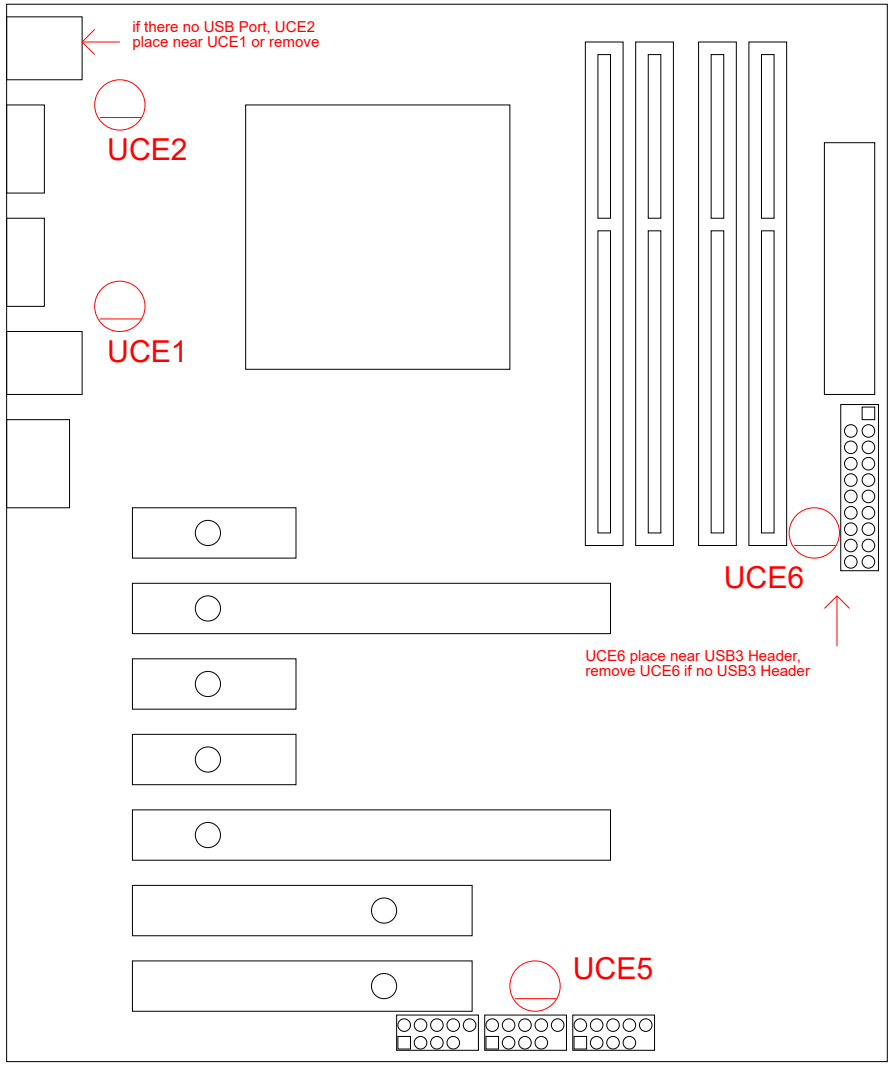
PL CAP



CAP PL 100UF/16V 6.3*9 DIP 20%

GAMING :黑色11031-0001F500

USB Power CAP recommend placement



BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	USB
CS_USB_0.2E	

HD_DEMO_USB
/X

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB Power CAP

Engineer: Kell_Huang

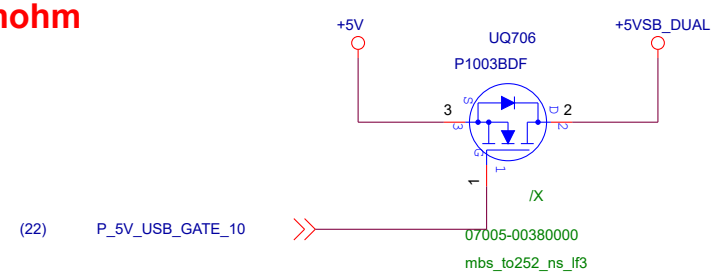
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Friday, August 17, 2018 Sheet 102 of 117

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 104 of 117	

+5VSB_DUAL current:
DIMM*4=7A, DIMM*2=5A
USB 2.0=0.5A/port
USB 3.x=1A/port
USB Type C=3A/port
if +5VSB_DUAL current (DIMM+USB 2.0 Port+USB 3.x Port) > 15A, add UQ706

DPAK MOS 9 mohm



NIKO DPAK 9mohm: 07005-00380000

Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, August 29, 2018		Sheet 103 of 117	

ASUS PCB Logo Circuit

A. Choose ASUS Logo by Project

B. Choose KCC Logo by Project

C. Keep or remove NEED_COMP_SILK by Project

A

LOGO2
FCC
FCC
/X

LOGO7
PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

PCB MADE IN CHINA

LOGO3
RCM
RCM
/X

LOGO9
CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

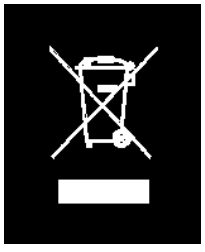
CAN ICES-3 (B)/NMB-3(B)

LOGO1
EMI_D33005_H
EMI_D33005_H
/X

D33005
RoHS

LOGO8
VCCI
VCCI
/X

LOGO5
WEEE_LOGO
WEEE_LOGO
/X



LOGO6
CE
CE
/X

LOGO11
SFIS LABEL
SFIS_LABEL
/X

SFIS

B

10mm without Wifi

LOGO10
KC_R-REM-MSQ-XXXXXXXXXXXXX
KC_R_REM_LOGO
/X
s_kc_r_r_logo_10mm

KCC Logo without Wifi

KCC Logo with Wifi

C

LOGO12
UKRAINE LOGO
UKRAINE LOGO
/X

UKRAINE Logo without Wifi

<Variant Name>

ASUSTEK COMPUTER INC	Title : PCB Logo	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Silkscreen Demo Circuit	Rev: 1.0C
Date: Friday, August 17, 2018	Sheet 105 of 117	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 101 of 117	

Two USB 3.x Ports to One Type-C Connector/USB 3.1 Front Header Circuit_1

A. Choose Type-C Connector/USB 3.1 Front Header by Project

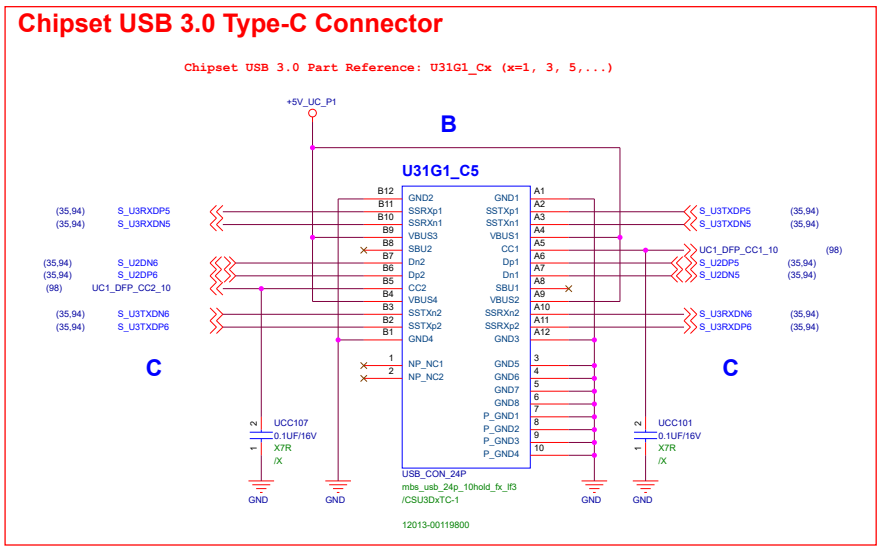
B. Modify Type-C Connector/USB 3.1 Front Header Part Reference by Project

C. Modify USB 3.x Port TX/RX/D+/D- Signal Net Name by Project

BOM	Type-C with Power Switch	Type-C with Poly Switch
/CSU3DxTC-1	mount	mount
/CSU3DxTC-1/Power Switch	mount	unmount
/CSU3DxTC-1/Poly Switch	unmount	mount

A.1

Chipset USB 3.0 Type-C Connector



<Variant Name>

ASUSTEK COMPUTER INC

Title : CS U3.x Type-C

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Chipset USB Type-C Port	1.0D

Date: Wednesday, August 29, 2018 Sheet 100 of 117

AMD Platform

You can only choose **8** pcs PCB Impedance point for your project

0 (must choose if use ASM1142/1143/2142/3142)

ASMedia USB 3.1 TX/RX

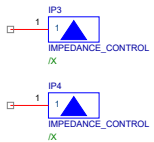
80 Ohm +/- 10%

1

DRAM CMD

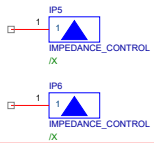
2

DRAM Clock



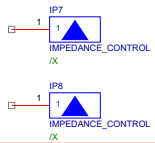
3

PCIE



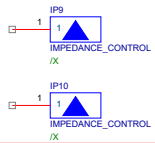
4

USB2.0



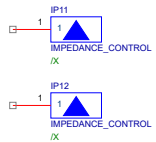
5

DRAM DQS



6

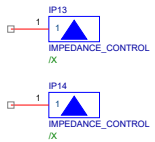
LAN



*** You can only choose 1 function to place point follow table ***

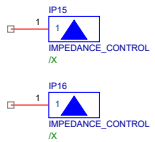
7

SATA



8

USB3.1



Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : PCB Impedance Point

Engineer: SZ Design IP

Size: A3 | Project Name: Silkscreen Demo Circuit | Rev: 1.0C

Date: Friday, August 17, 2018 | Sheet 108 of 117

Fiducial Mask (光學點)

Delete it for EMS

圓形光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

大顆光學點

小顆光學點

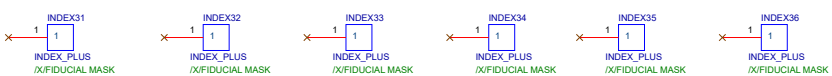
Delete it for EMS

十字光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

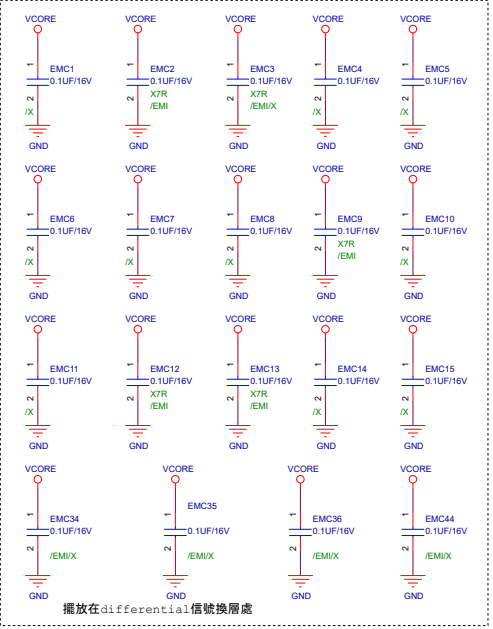
大顆光學點

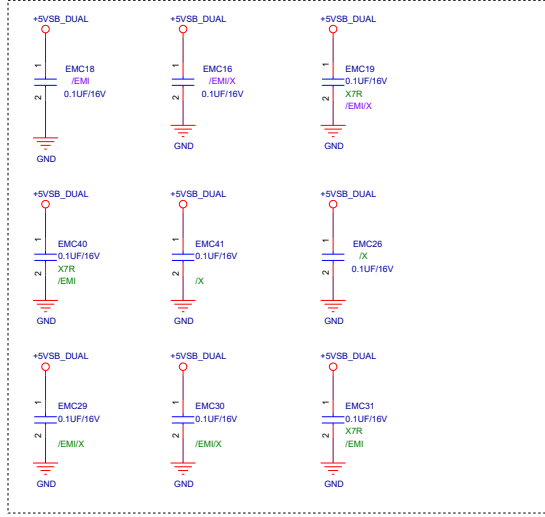
小顆光學點

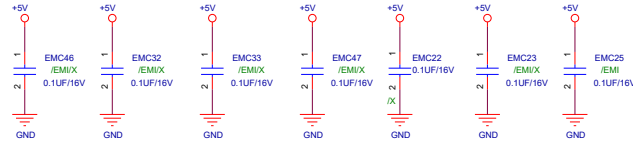


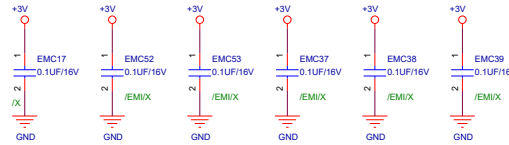
<Variant Name>

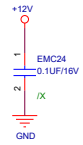
ASUSTEK COMPUTER INC	Title : Fiducial Mask		
	Engineer: SZ Design IP		
Size: A3	Project Name: Silkscreen Demo Circuit		Rev: 1.0C
Date: Friday, August 17, 2018	Sheet 107 of 117		

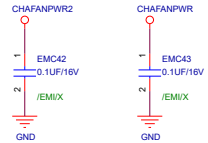


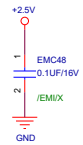












Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, August 21, 2018		Sheet 113 of 117	

IO Cover

H26
1
C118D118N
/X
mbs_hole_c118d118n_sp

H31
1
C138D138N
/X
s_hole_c138d138n

H32
1
C157D157N
/X
mbs_hole_c157d157n

H27
1
C118D118N
/X
mbs_hole_c118d118n_sp

H26_1

SPI ROM

DIP 64M

13050-B5D04000

H27_1

SPI ROM

DIP 64M

13050-B5D04000

IO_COVER

SPI ROM

DIP 64M

13MB0Y11P01011

Heatsink

Heatsink follow Intel TUF B360M-PLUS GAMING

HEATSINK_PCH
1
2
HEATSINK
s_hsk_2p_1516x2008
N/A
13071-02781300

PCH Heatsink

HEATSINK_MOSW
1
2
HEATSINK
N/A
13071-02781800
s_hsk_2p_1949x3952

MOSW Heatsink

HEATSINK_MOSN
1
2
HEATSINK
N/A
temp_T_002702
s_hsk_2p_3210x1103

MOSN Heatsink

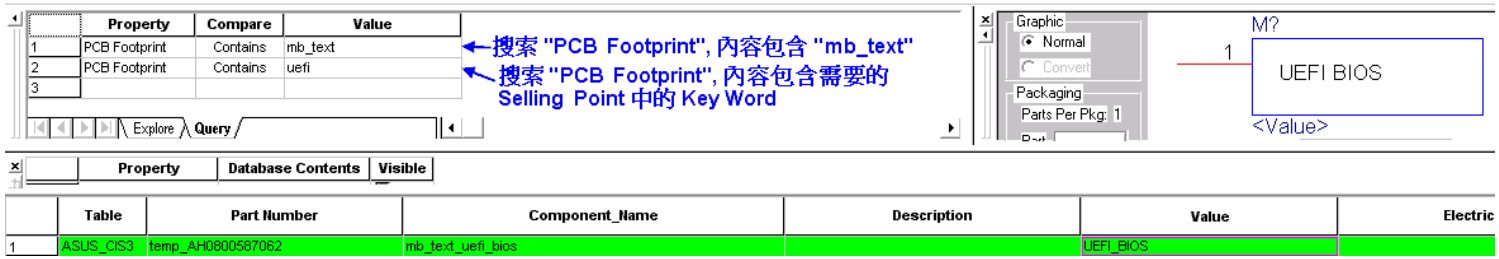
<Variant Name>

ASUSTeK COMPUTER INC	Title : HEAT SINK	
	Engineer: KENNY_CHEN	
Size: A3	Project Name: Z87-PRO	Rev: R1.02A
Date: Friday, August 31, 2018	Sheet 112 of 117	

Selling Point

1. Selling Point 新增流程及窗口人員

2. 如何抓取 Selling Point Part, 如下圖



3. Example

layout request

Note:
1. PWM(Server/ WS only)
2. TACH(Server/ WS only)

0613
swap by layout
Alex

RN change to R

RN change to R

0530
swap by layout
Alex

0522

0706

GPIO \ CORETYPE1	Bristol (0)	Summit (1)
GPI	S_LED1	O_MEMOKLED#
GPO L	O_MEMOKLED#	S_LED1

<Variant Name>

ASUSTeK COMPUTER INC

Title: SPTH EUP/LED Control

Engineer: Eason

Size	Project Name	Rev
A3	Z270-STRIX	R1.00

Date: Friday, August 17, 2018 Sheet 114 of 117

LPC TPM Circuit

A. Del LPC TPM Header if don't need

B. Modify LPC TPM Header Clock Net Name by Project

C. Modify Part Number of LPC TPM Header by Color

D. Del Onboard LPC TPM IC if don't need

E. Modify Onboard LPC TPM IC Clock Net Name by Project

F. Modify Onboard LPC TPM IC's Part Number by Project

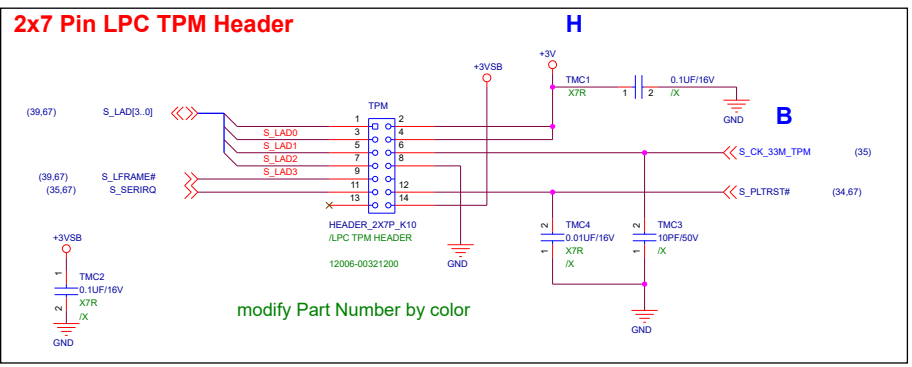
G. Modify Optional of TMR13, TMR14, TMR15 by Onboard LPC TPM IC

H. Modify +3V to +3V_S0IX if support Intel S0ix

I. Choose TPM_CLKRUN# Circuit by Project

BOM	LPC TPM Header	Onboard LPC TPM
N/A	mount	mount
/X	unmount	unmount
/LPC TPM HEADER	mount	unmount
/LPC TPM IC	unmount	mount

A



<Variant Name>

ASUSTEK COMPUTER INC

Title : LPC TPM

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Other Demo Circuit	1.0C

Date: Wednesday, August 29, 2018 Sheet 110 of 117

0.1A Beta

IC Power (Iop=4.5mA、Isink=320mA)

+3VSB_ATX → LED1JP24 (SHORTPIN_0603_NM /X/8K41) → LED1_VCC

線寬=30mil

請將電容擺放至VDD旁邊(避免power-on時的電源凸波)

LED1C221 0.1UF/16V
LED1C257 10UF/6.3V /X/8K41
LED1C258 1UF/6.3V
LED1_VCC
GND

Cost考量，改上1uF，待實測確認是否更換10uF

SMBUS 請依平台選擇SMBUS

Intel：接SIO

AMD：接CPU S5 SMB

(34,44,117) S_SMBCLK_VSB
(34,44,117) S_SMBDATA_VSB

SMBUS net 命名，請自行修改或刪除

SMBUS 請放置在IC的SMBUS附近

+3VSB

LED1R1601 4.7KOhm /X/8K41 S_SMBCLK_VSB
LED1R1602 4.7KOhm /X/8K41 S_SMBDATA_VSB
LED1C219 33PF/50V /X/8K41 S_SMBCLK_VSB
LED1C218 33PF/50V /X/8K41 S_SMBDATA_VSB
GND

SMBUS net 命名，請自行修改或刪除

ACPI 請選擇APCI Pin的Power，請依需求自行刪除

支援開/關機特效

+3V
LED1R1990 8.2KOhm
LED1_ACPI
/8K41

LED1U1

LED1_VCC
GND
12 VDD
13 VSS
21 GND
Power

10 PB7/RXD0/ICK/SCL/SCK/PWM2/ GPW2/AD4
11 PC0/TXD0/IDA/SDA/DIO/PWM3/ INT1/AD5
SMBUS

UR
TX1
RX1
1 PA6/GPW1/INT0/SEG6/TXD1/TK6
2 PA7/SEG7/RXD1/TK7
UR

ACPI
LED1_ACPI
19 PA4/SEG4/TK4
ACPI

GPIO
14 PC1/GPW0/CEXT
9 PB6/AD3/TK14
8 PB5/AD2/TK13
7 PB4/COM4/AD1/TK12
6 PB3/COM3/AD0/TK11
5 PB2/COM2/TK10
4 PB1/COM1/TK9
3 PB0/COM0/TK8 LED1_SMBSTRAP2
20 PA5/SEG5/TK5 LED1_SMBSTRAP1

PWM
18 PA3/SEG3/TK3
17 PA2/SEG2/TK2
16 PA1/PWM1/SEG1/TK1
15 PA0/STB/PWM0/SEG0/TK0
PWM

PWM：Sink 10mA
LED1A_B (116)
LED1A_G (116)
LED1A_R (116)

AURA41UA0

SMBUS Address：80

請註明是否有外接MOS

? LED (MOS)

請註明亮燈的區域 EX：CPU LED(MOS)

0: CPU
1: VRM
2: NB
3: PCH
4: Audio
5: Back IO
6: Back Plate
7: PCIE
8: PCB Surround
9: M.2
10:Start/retry Button
11:Light Bar
12:RGB Header

SMBUS Address:(預留)
請將零件放置在IC的SMBUS附近

+3VSB_ATX
LED1R1997 8.2KOhm /X/8K41
LED1R1998 8.2KOhm /X/8K41
LED1_SMBSTRAP2
LED1_SMBSTRAP1
LED1R1999 8.2KOhm /X/8K41
LED1R2000 8.2KOhm /X/8K41
GND GND

<Variant Name>

ASUSTek Computer Inc.
Title : ENE_8K41
Engineer: Kazier_Luo
Size: Custom
Project Name: LED Standard Circiut
Rev: 1.0
Date: Wednesday, August 29, 2018
Sheet 115 of 117

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, August 17, 2018	Sheet 111 of 117	

m-ATX Screw Hole Circuit

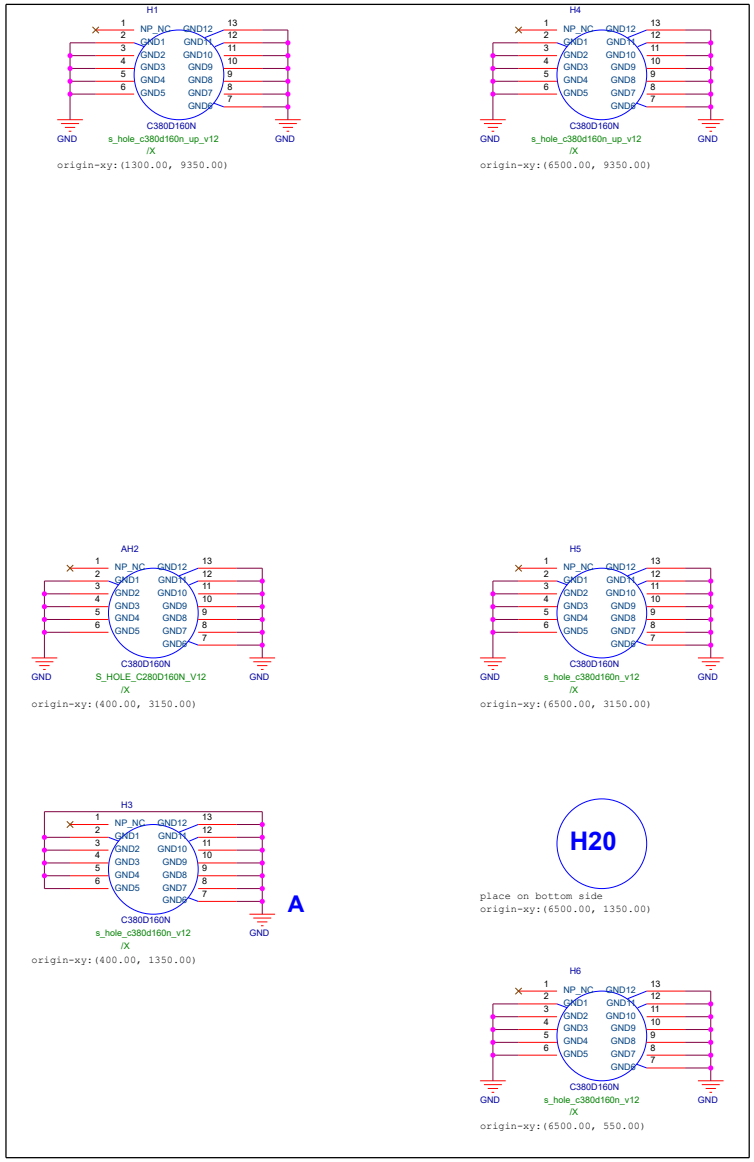
A. Connect H3 to GND or A_GND by Project

B. Choose Bottom Side Silkscreen of H20 by Project

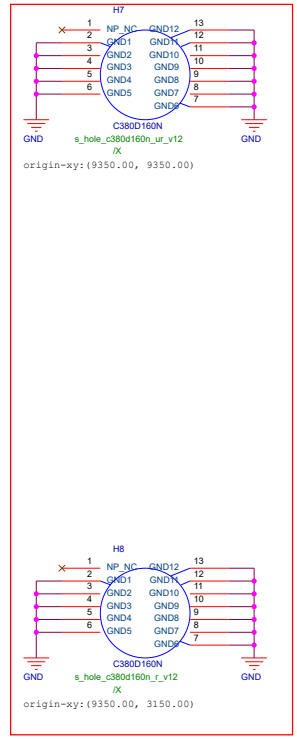
C. Choose H7, H8 by Project

Delete it for EMS

m-ATX Screw Hole

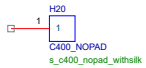


C.1

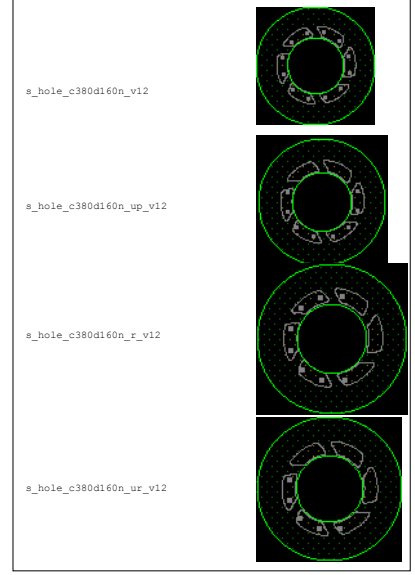


B.2

H20 with Bottom Side Silkscreen



MB SCREW FOOTPRINT



m-ATX Screw Select

	Standard (9.6 x 9.6)	Scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H20	V	V

<Variant Name>

ASUSTEK COMPUTER INC

Title : Screw Hole

Engineer: SZ Design IP

Size	Project Name	Rev
Custom	Other Demo Circuit	1.0C

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1.LED控制 < 20颗

LED驱动器简单介绍及使用

LED驱动 Driver

Code View

LED程序命名

外接模块 （跳线cc或接地表示此脚是否要外接模块，若不需要，跳自行锁脚）

3.只有一颗模块的情况

PWM Function

Micro Seconds

Milli Seconds

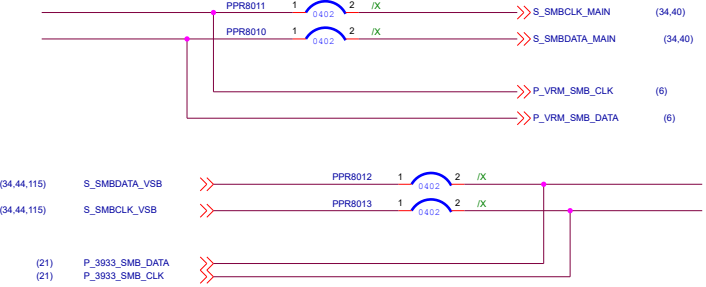
Seconds

PWM Function 2

Micro Seconds

Milli Seconds

Seconds



<Variant Name>

ASUSTEK COMPUTER INC	Title : PWRCUT	
	Engineer: Kell_Huang	
Size: A3	Project Name: ASM1142 Demo Circuit	Rev: 0.0
Date: Wednesday, August 29, 2018	Sheet 117 of 117	