1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
3	0007084962	ENGINEERING RELEASED	2016-09-14

Kristie MLB

LAST_MODIFICATION=Wed Sep 14 23:01:20 2016

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-01477	1	SCH,MLB,X647	SCH	CRITICAL	
820-00597	1	PCBF,MLB,X647	PCB	CRITICAL	
685-00101	1	PCBA,MLB,COMMON PARTS,X647	CMNPTS		MLB_CMNPTS

FAB#KG159

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SYNC_MASTER=yeungr SYNC_DATE=12/09/2015

DRAWING TITLE: SCHEM,MLB,X647

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

BRANCH:

PAGE: 1 OF 119

SHEET: 1 OF 87

BOM Groups

BOM GROUP	BOM OPTIONS
X647_COMMON	COMMON,ALTERNATE,ALT_CMN,X647_PROGPARTS,XDP,RTCRST:Y,GPUCLK:OSC,1V8_AUDIO_DLY:Y
X647_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
X647_DEVEL	XDP_CONN,SAMCONN

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00659	1	IC,EFI,V0055,Proto1,X647	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,SERIAL FLASH,64MBIT,3V,8P,WSON,QE=1	U5210	CRITICAL	BOOTROM:BLANK
341S00567	1	IC,SMC-B1,EXTERNAL,VSMC2,36A6,X647	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/560MIPS,MCU,157BGA	U5000	CRITICAL	SMC:BLANK
341S00660	1	IC,CAMERA,FLASH,VTBD,Proto1,x647	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00706	1	IC,AR,V10.2.EVT,X647	U2890	CRITICAL	TBTROM:PROG
335S00133	1	IC,SPI FLASH,8MBIT,3.0V,USON8	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET ROM,NYMONYX,V1.15	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00341	1	CPU,KBL,QKZQ,B0,QS,3.0,65W,1.0,LGA1151	CPU	CRITICAL	CPU:KBL_3.0
337S00340	1	CPU,KBL,QKHA,B0,QS,3.4,65W,1.1,LGA1151	CPU	CRITICAL	CPU:KBL_3.4
337S00342	1	CPU,KBL,QKHA,B0,QS,3.6,65W,1.15,LGA1151	CPU	CRITICAL	CPU:KBL_3.6

GPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00307	1	IC,GPU,AMD,BAFFIN,LEA,A1,LF,QS,BGA769	U8800	CRITICAL	GPU:BF_LEA
337S00306	1	IC,GPU,AMD,BAFFIN,PROA,A1,LF,QS,BGA769	U8800	CRITICAL	GPU:BF_PROA
337S00321	1	IC,GPU,AMD,BAFFIN,XLA,A1,LF,QS,BGA769	U8800	CRITICAL	GPU:BF_XLA

Sockets & Connectors

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S00002	1	CONN,CPU,SOCKET,LGA1151,SKYLAKE,HF	U0500	CRITICAL	
514-00053	1	CONN,RCPT,USB-C,DUAL,X648	J3300	CRITICAL	
998-04867	1	INTERPOSER,AMD,CS88,BGA769,VDDC	U8800	CRITICAL	GPU:SKT_VCORE
998-04866	1	INTERPOSER,AMD,CS89,BGA769,VDDCI/MVDD	U8800	CRITICAL	GPU:SKT_VDDCI

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00298	1	IC,PCH,SKL,SSKU,Q3SD,D1,ES,BGA837	U1100	CRITICAL	
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	

FB VDRAM Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S00044	4	VRAM,MICRON,4GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:2GB_MICRON
333S00078	4	VRAM,SAMSUNG,4GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:2GB_SAMSUNG
333S00043	4	VRAM,HYNIX,4GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:2GB_HYNIX
333S00075	4	VRAM,MICRON,8GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:4GB_MICRON
333S00074	4	VRAM,SAMSUNG,8GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:4GB_SAMSUNG
333S00100	4	VRAM,HYNIX,8GBIT,7GBPS,BGA170	U9200,U9250,U9300,U9350	CRITICAL	FB:4GB_HYNIX

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0124	377S0057	ALT_CMN	ALL	TVS
155S0578	155S0367	ALT_CMN	ALL	120OHM EMI BEAD
138S0681	138S0638	ALT_CMN	ALL	Taiyo 10uf 805 alt
197S0479	197S0478	ALT_CMN	ALL	12 MHz Cam. Xtal
197S0486	197S0478	ALT_CMN	ALL	12 MHz Cam. Xtal
107S0251	107S0249	ALT_CMN	ALL	2mOhm Sense resistor
107S0255	107S0240	ALT_CMN	ALL	1mOhm Sense resistor
197S0481	197S0480	ALT_CMN	ALL	25MHz Xtal
197S0343	197S0480	ALT_CMN	ALL	25MHz Xtal
197S0369	197S0392	ALT_CMN	ALL	32 KHz PCH Xtal
197S0399	197S0392	ALT_CMN	ALL	32 KHz PCH Xtal
138S0860	138S0775	ALT_CMN	ALL	Single-source 1uF 402
378S0391	378S0390	ALT_CMN	ALL	Debug LEDs
341S00016	341S3912	ALT_CMN	ALL	ENET ROM,ADESTO,V1.15
376S0572	376S0659	ALT_CMN	ALL	Single P-Ch FET
128S00042	128S0329	ALT_CMN	ALL	CAP,220uF,6.3V,35mOhm
128S0311	128S0329	ALT_CMN	ALL	CAP,220uF,6.3V,35mOhm
371S00095	371S0567	ALT_CMN	ALL	Diode,100V,0.25A
138S00084	138S00060	ALT_CMN	ALL	Cap,47uF,6.3V,0603
152S00403	152S00322	ALT_CMN	ALL	Ind,0.68uH,20%,6.1A,20mOhm
138S0676	138S0691	ALT_CMN	ALL	Cap,Cer,22uF,20%,6.3V
155S00007	155S0667	ALT_CMN	ALL	Fltr,Common Mode,90Ohm,100mA
155S0935	155S0667	ALT_CMN	ALL	Fltr,Common Mode,90Ohm,100mA
353S00769	353S4398	ALT_CMN	ALL	IC,TPS22966,LOADSW,6A
353S00993	353S2541	ALT_CMN	ALL	IC,NCS20081,OP-AMP,R-R
132S0401	132S00012	ALT_CMN	ALL	CAP,0.22UF,10%,25V,X7R,0402
371S0684	371S0495	ALT_CMN	ALL	DIODE,DUAL SCHOTTKY,30V
376S00015	376S0610	ALT_CMN	ALL	XSTR,FET,DL NCH,60V
138S0933	138S0931	ALT_CMN	ALL	CAP,22UF,20%,4V,X6S,0603
128S00008	128S0380	ALT_CMN	ALL	CAP,TANT,210UF,20%,2.5V
152S00368	152S00269	ALT_CMN	ALL	Ind,1.0uH,20%,14A,10.7mOhm
128S0412	128S0237	ALT_CMN	ALL	CAP,TANT,330UF,20%,6.3V

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00189	08	CPU,SKL,4C+2,65W,3.2GHZ
337S00187	08	PCH,SSDKUZ170,SR2C9
338S00229	08	TBT,Alpine Ridge-4c
337S00225	09	GPU,BAFFIN_M,BGA769
333S00044	09	VRAM,MICRON,4GBIT,7GBPS
333S00078	09	VRAM,SAMSUNG,4GBIT,7GBPS
333S00075	09	VRAM,MICRON,8GBIT,7GBPS
333S00074	09	VRAM,SAMSUNG,8GBIT,7GBPS
353S00422	09	ACE, USB-C port power ctlr
353S4442	09	TPS2559, USB load switch
353S00875	09	TAS5764L, Audio amp

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0830	155S0316	ALT_CMN	ALL	FER BD,600 OHM,0.5A,0603
155S00076	155S0546	ALT_CMN	ALL	FER BD,600 OHM,300mA,0402
152S1876	152S1373	ALT_CMN	ALL	IND,PWR,7.8 mohm,13A,7.1x6.5x3mm
376S1089	376S1128	ALT_CMN	ALL	Single N-Ch FET
155S0660	155S0513	ALT_CMN	ALL	22OHM EMI BEAD
155S0694	155S0387	ALT_CMN	ALL	470OHM EMI BEAD
376S1129	376S00074	ALT_CMN	ALL	Dual N-Ch FET
376S0855	376S00074	ALT_CMN	ALL	Dual N-Ch FET
311S0649	311S0541	ALT_CMN	ALL	Single AND Gate
353S4376	353S3384	ALT_CMN	ALL	HDD OOBv1 comparator
371S00019	371S0463	ALT_CMN	ALL	Rohm Schottky Barrier Diode
138S0746	138S0705	ALT_CMN	ALL	CAP,CER,X5R,10uF,20%,10V,402
311S00004	311S0370	ALT_CMN	ALL	SPI Quad I/O Mux
376S00001	376S0659	ALT_CMN	ALL	Single P-Ch FET
376S0972	376S00075	ALT_CMN	ALL	Single N-Ch FET
376S00124	376S00200	ALT_CMN	ALL	NFET,30V,22A,8P DFN
371S00043	371S0463	ALT_CMN	ALL	Diode,Schottky,30V,100mA
152S00358	152S00208	ALT_CMN	ALL	Ind,1uH,2.1A,128mOhm
138S0714	138S0713	ALT_CMN	ALL	Cap,10uF,6.3V,0402
116S00007	116S00006	ALT_CMN	ALL	Res,0Ohm,3A,0402
152S1499	152S0864	ALT_CMN	ALL	Ind,47uH,0.58mOhm,0402
353S00854	353S4342	ALT_CMN	ALL	ICREF3330,V-Ref,3V,5mA
155S0659	155S0382	ALT_CMN	ALL	Fltr,EMI,Ferr,8O,30Ohms,1.7A
197S00047	197S00036	ALT_CMN	ALL	Xtal,25Mhz,15ppm,20pF,50Ohm
107S00030	107S00029	ALT_CMN	ALL	RES,DCDC SENSE,0.005OHM,1%
107S00087	107S00029	ALT_CMN	ALL	RES,DCDC SENSE,0.005OHM,1%
107S00015	107S00011	ALT_CMN	ALL	RES,DCDC SENSE,0.75MOHM,1%
152S00388	152S00182	ALT_CMN	ALL	IND,2.2UH,20%,43MOHM,4.5A
155S00155	155S0441	ALT_CMN	ALL	FLTR,EMI,FER BD,220OHM,1.4A
371S0718	371S0531	ALT_CMN	ALL	DIODE,BAT54,SHOTTKY,30V
155S00115	155S00114	ALT_CMN	ALL	FERR BD,10 OHM,25%,8A
197S0588	197S0591	ALT_CMN	ALL	XTAL,24.000MHZ,20PPM,9.5PF
197S0590	197S0591	ALT_CMN	ALL	XTAL,24.000MHZ,20PPM,9.5PF
353S00711	353S2073	ALT_CMN	ALL	IC,INA210,CURRENT SENSE
376S0977	376S00078	ALT_CMN	ALL	XSTR,FET,N-CH,DUAL,20V
311S00116	311S0324	ALT_CMN	ALL	74LVC2G34GF/S500
106S00017	106S4171	ALT_CMN	ALL	RES,MF,30.1OHM,0.125W,1,80S
132S00086	132S00045	ALT_CMN	ALL	CAP,X6S,0.022UF,6.3V,0201
132S00057	132S0668	ALT_CMN	ALL	CAP,2200PF,10%,25V,X7R,0201
138S0758	138S0742	ALT_CMN	ALL	CAP,X5R,22UF,MURATA
138S0759	138S0762	ALT_CMN	ALL	CAP,1UF,20%,16V,X6S,0603
138S00015	138S0777	ALT_CMN	ALL	CAP,10UF,20%,16V,X6S,0603
128S0444	128S0323	ALT_CMN	ALL	CAP,330UF,6.3V,D2E
311S00008	311S0271	ALT_CMN	ALL	AND GATE
353S00519	353S00831	ALT_CMN	ALL	IC,FDMF5804,DR MOS
376S00016	376S0644	ALT_CMN	ALL	MOSFET,P-CH,20V,1A
138S0641	138S0700	ALT_CMN	ALL	CAP,2.2UF,10%,10V,X5R,0402
138S0739	138S0706	ALT_CMN	ALL	CAP,1UF,20%,10V,X5R,0201
155S00204	155S0731	ALT_CMN	ALL	FERR BD,120 OHM,25%,0402
152S00543	152S00484	ALT_CMN	ALL	IND,0.24UH,20%,10A,12MOHM

SYNC_MASTER=andres SYNC_DATE=08/05/2016

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

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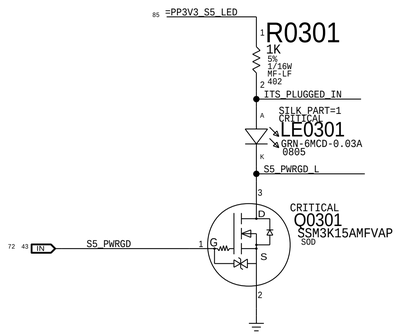
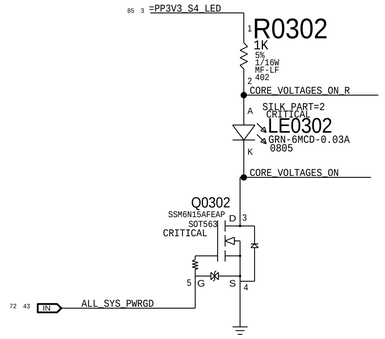
S5 Led



ALL_SYS_PWRGD Led



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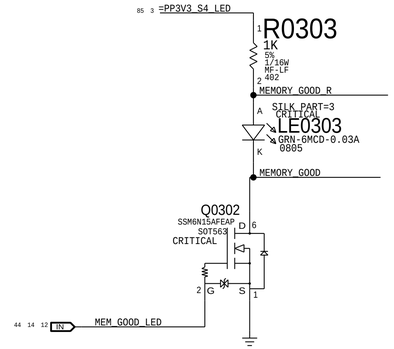
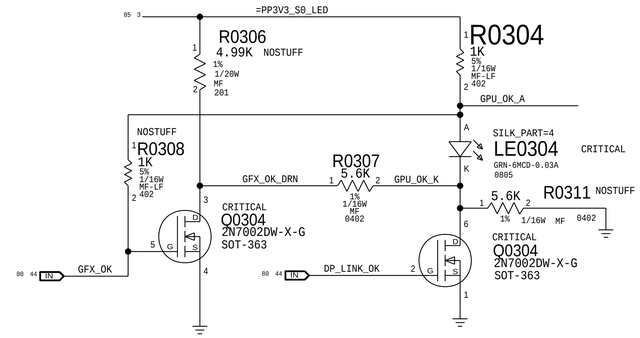
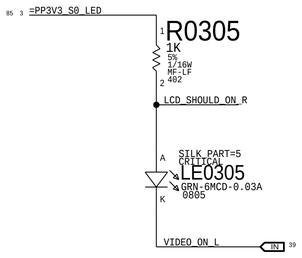


GPU OK Led



THIS LED IS DRIVEN BY GPU:
GFX_OK HIGH LIGHTS THE LED DIMLY
DP_LINK_OK HIGH LIGHTS THE LED FULLY

VIDEO ON Led



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SYNC_MASTER=J94_ROSSANA SYNC_DATE=02/02/2015

PAGE TITLE: Debug LEDS

Apple Inc.

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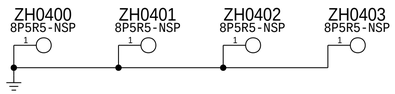
CPU HEATSINK

4mm Plated Holes (APN 998-4158)

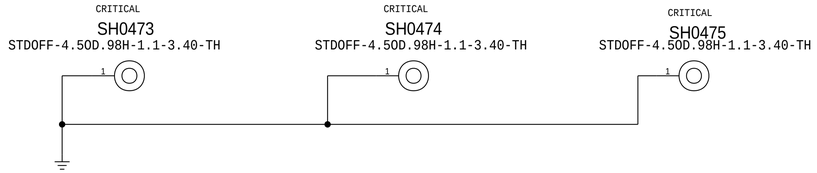


WIRELESS CARD MTG HOLES

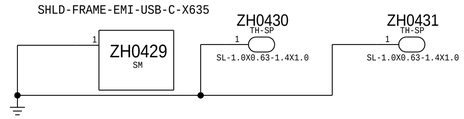
998-06186 (PLATED HOLES, 3.3mm INNER DIAMETER, 5.5mm pad)

GPU HEATSINK MOUNTING FEATURES

APN:860-1532



USB-C EMI Can



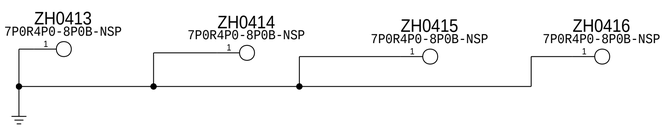
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-07339	1	COVER,EMI SHIELD,USB-C,X635	EMI_SHIELD	CRITICAL	

HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

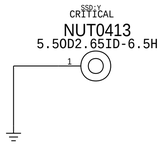
Rear Cover

APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



SSD STANDOFF

APN: 860-00314



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PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-01477
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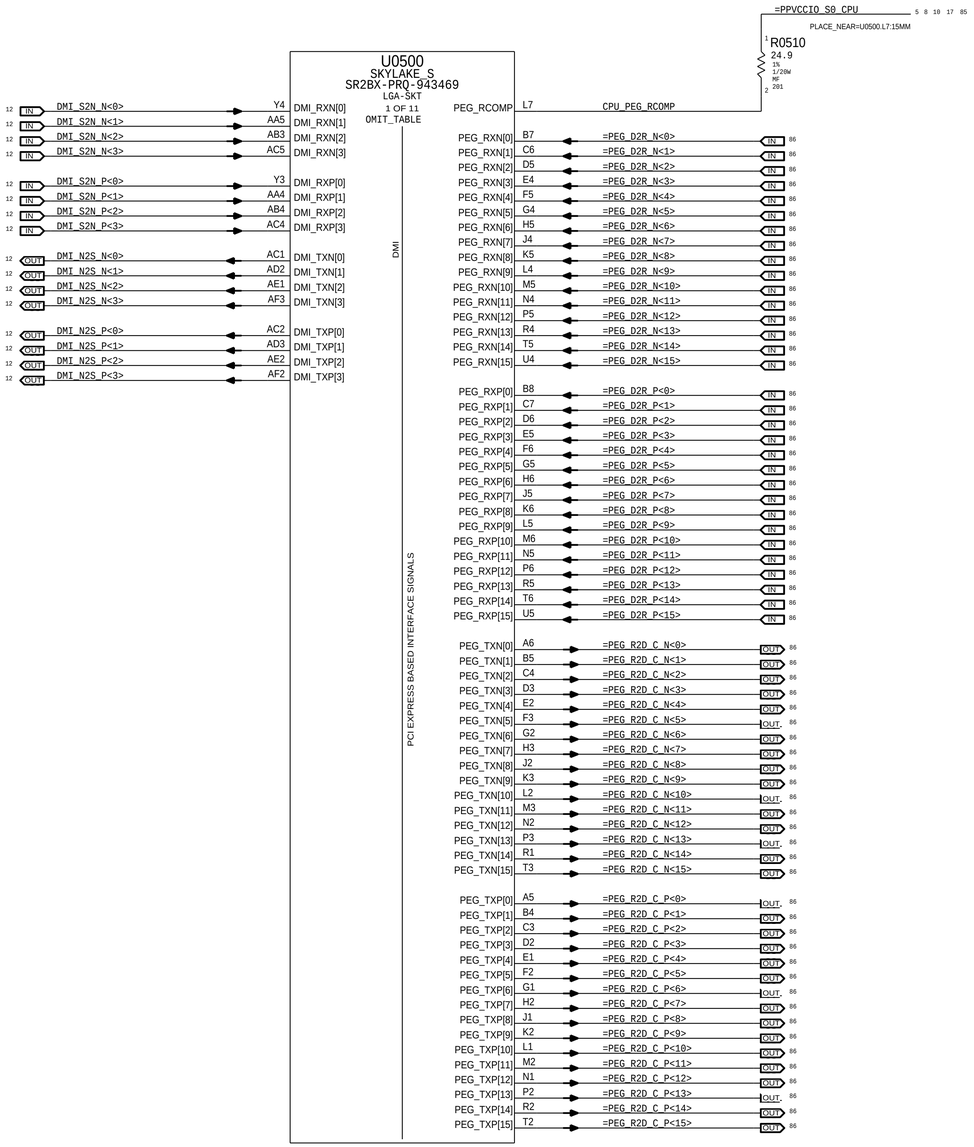

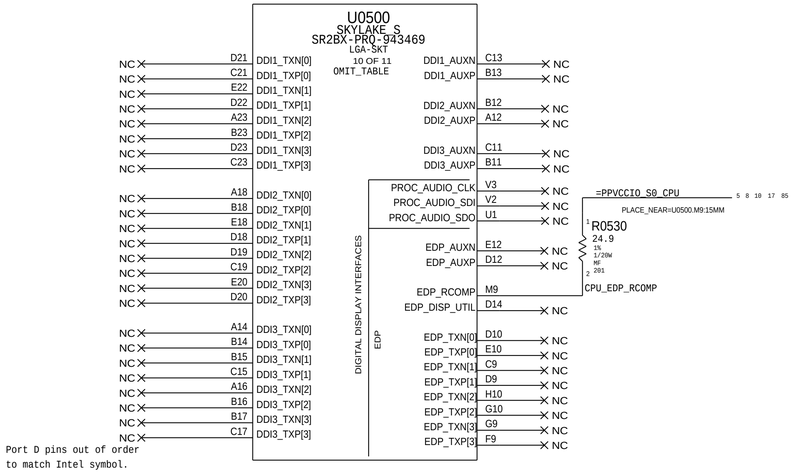

Port D pins out of order
to match Intel symbol.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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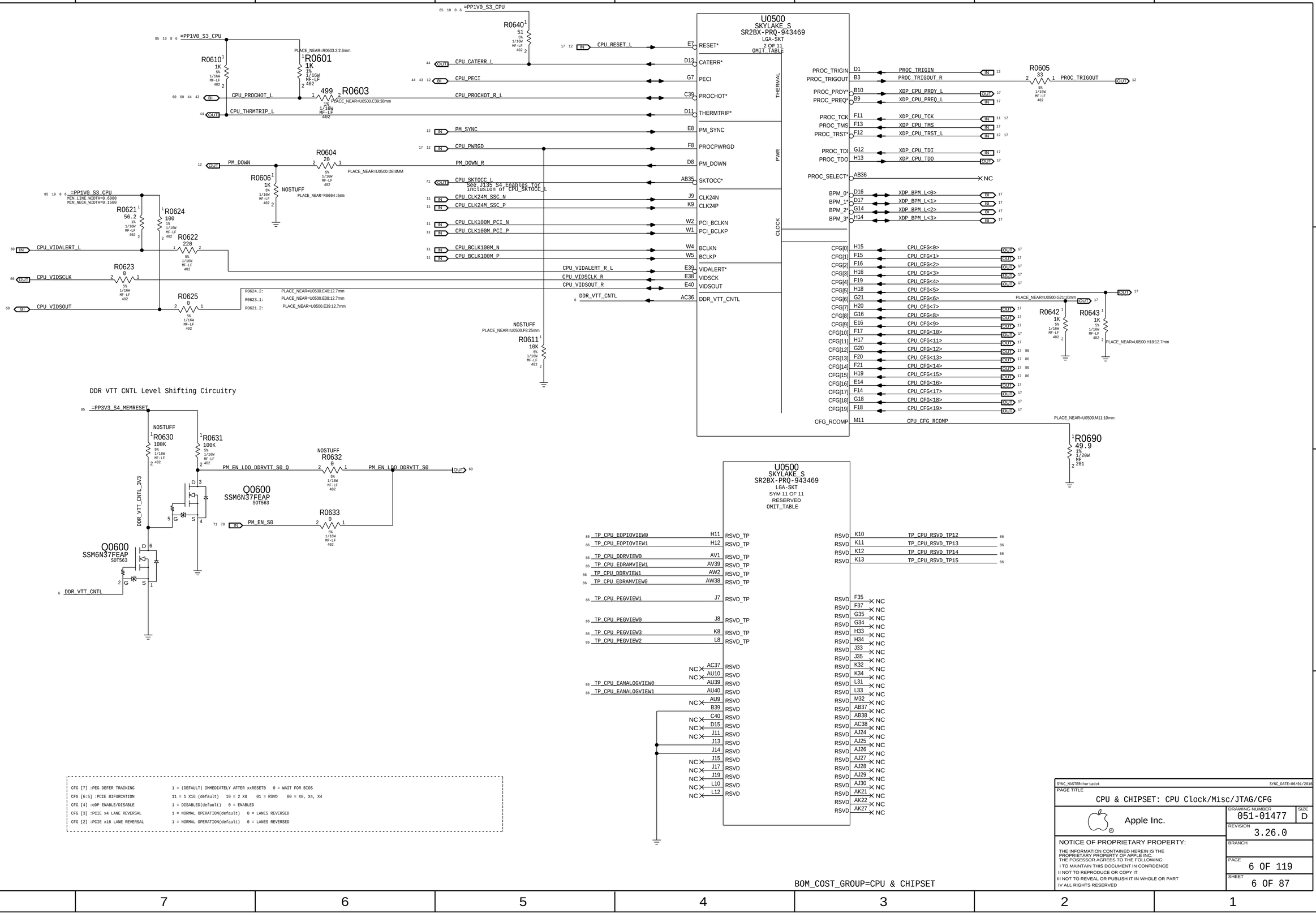
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U0500
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LGA-SKT
2 OF 11
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RESET*
CPU_CATERR_L
CATERR*
CPU_PECI
PECI
CPU_PROCHOT_L
CPU_PROCHOT_R_L
PROCHOT*
CPU_THRMTRIP_L
THERMTRIP*
THERMAL
PM_SYNC
PM_SYNC
CPU_PWRGD
PROCPWRGD
PM_DOWN
PM_DOWN_R
SKTOCC*
CPU_SKTOCC_L
See j125 S4 Enables for inclusion of CPU_SKTOCC_L
PWR
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CPU_CLK24M_SSC_P
CLK24N
CLK24P
CPU_CLK100M_PCI_N
CPU_CLK100M_PCI_P
PCI_BCLKN
PCI_BCLKP
CPU_BCLK100M_N
CPU_BCLK100M_P
BCLKN
BCLKP
CLOCK
CPU_VIDALERT_R_L
CPU_VIDSCK_R
CPU_VIDSOUT_R
VIDALERT*
VIDSCK
VIDSOUT
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DDR_VTT_CNTL
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PROC_TRIGOUT
PROC_TRIGOUT_R
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PROC_PREQ*
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XDP_CPU_PREQ_L
PROC_TCK
PROC_TMS
PROC_TRST*
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XDP_CPU_TMS
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PROC_TDO
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CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
CPU_CFG<16>
CPU_CFG<17>
CPU_CFG<18>
CPU_CFG<19>
R0642 1K
R0643 1K
PLACE_NEAR=U0500.H18:12.7mm
CFG_RCOMP
CPU_CFG_RCOMP
R0690 49.9 1% 1/20W MF 201
R0610 1K
R0601 1K
R0603 499
PLACE_NEAR=R0603.2:2.6mm
PLACE_NEAR=U0500.C39:38mm
R0604 20
PLACE_NEAR=U0500.D8:8MM
R0606 1K NOSTUFF
PLACE_NEAR=R0604:5mm
R0621 56.2
R0624 100
R0622 220
R0623 0
R0625 0
R0624.2: PLACE_NEAR=U0500.E40:12.7mm
R0623.1: PLACE_NEAR=U0500.E38:12.7mm
R0621.2: PLACE_NEAR=U0500.E39:12.7mm
NOSTUFF
PLACE_NEAR=U0500.F8:25mm
R0611 10K
DDR VTT CNTL Level Shifting Circuitry
=PP3V3_S4_MEMRESET
R0630 100K NOSTUFF
R0631 100K
R0632 0 NOSTUFF
R0633 0
PM_EN_LDO_DDRVTT_S0_Q
PM_EN_LDO_DDRVTT_S0
PM_EN_S0
DDR_VTT_CNTL_3V3
Q0600 SSM6N37FEAP SOT563
Q0600 SSM6N37FEAP SOT563
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (default) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eOP ENABLE/DISABLE 1 = DISABLED(default) 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION(default) 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION(default) 0 = LANES REVERSED
U0500
SKYLAKE_S
SR2BX-PRQ-943469
LGA-SKT
SYM 11 OF 11
RESERVED
OMIT_TABLE
TP_CPU_EOPIOVIEW0
TP_CPU_EOPIOVIEW1
TP_CPU_DDRVIEW0
TP_CPU_EDRAMVIEW1
TP_CPU_DDRVIEW1
TP_CPU_EDRAMVIEW0
TP_CPU_PEGVIEW1
TP_CPU_PEGVIEW0
TP_CPU_PEGVIEW3
TP_CPU_PEGVIEW2
TP_CPU_EANALOGVIEW0
TP_CPU_EANALOGVIEW1
RSVD_TP
RSVD
NC
TP_CPU_RSVD_TP12
TP_CPU_RSVD_TP13
TP_CPU_RSVD_TP14
TP_CPU_RSVD_TP15
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=hurtadot
SYNC_DATE=06/01/2016
PAGE TITLE
CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
BRANCH
PAGE 6 OF 119
SHEET 6 OF 87
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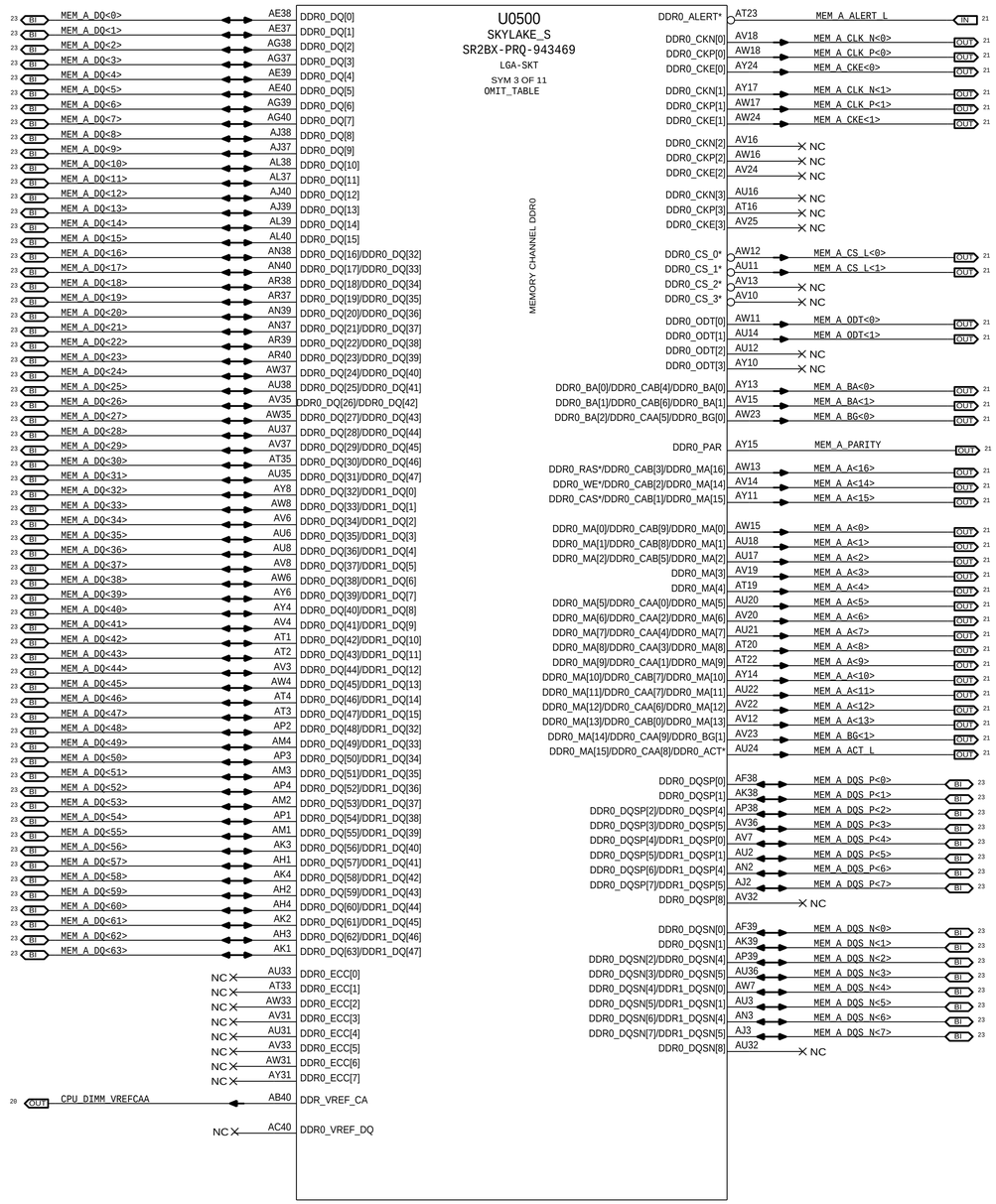

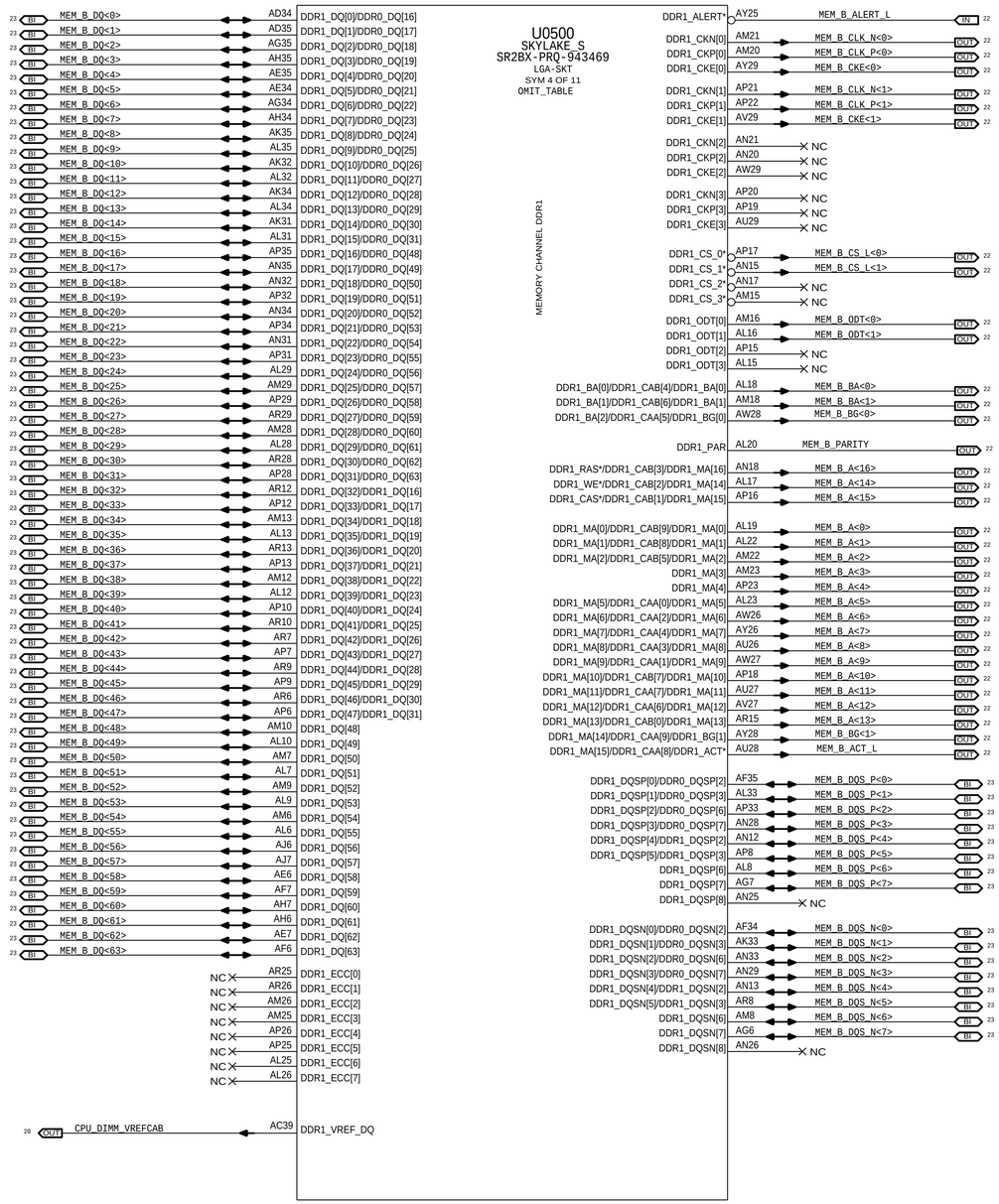

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=ddressler SYNC_DATE=11/09/2015

PAGE TITLE

CPU & CHIPSET: DDR4 Interface

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

BRANCH

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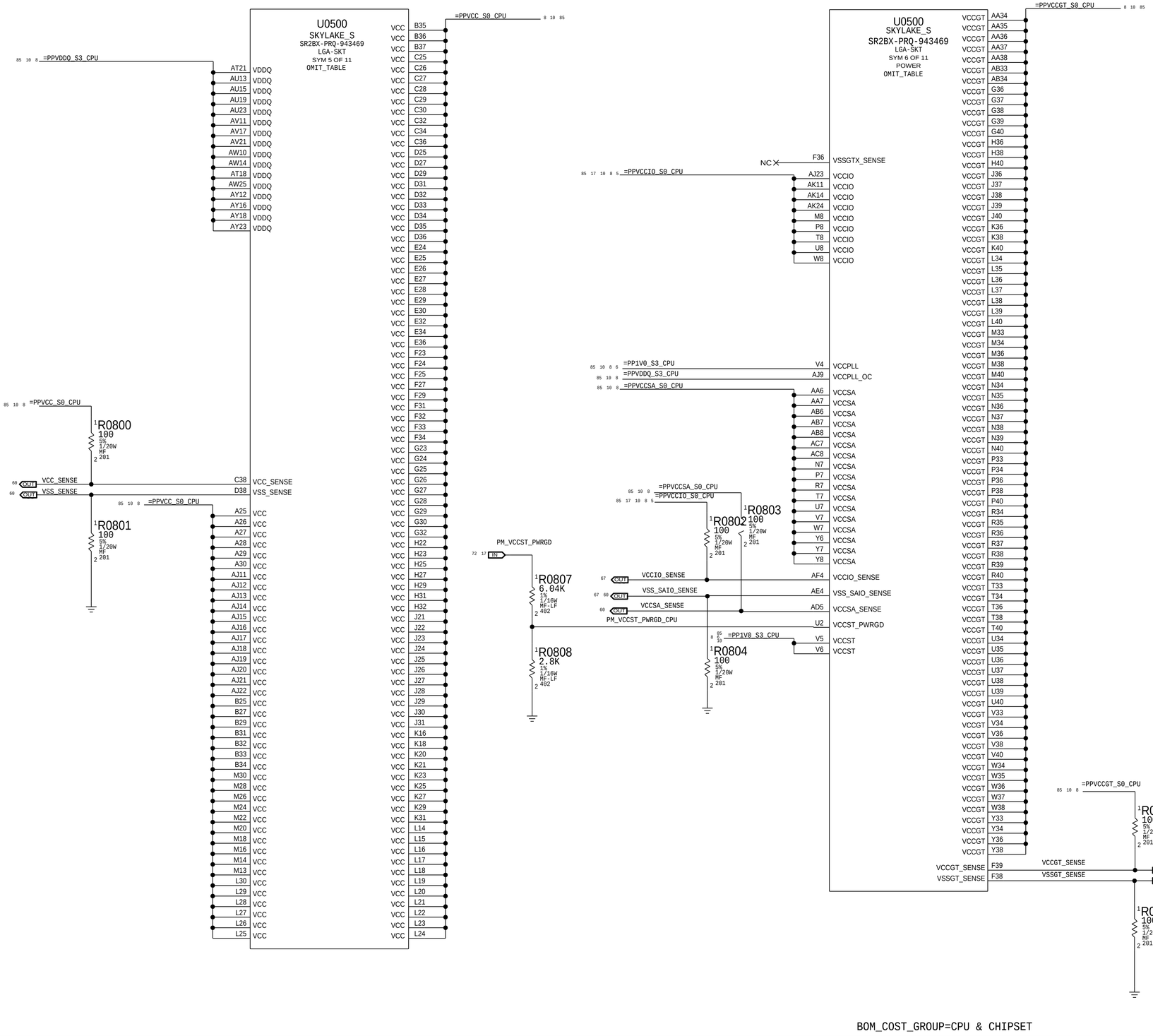
SHEET 7 OF 87


U0500
SKYLAKE_S
SR2BX-PRQ-943469
LGA-SKT
SYM 5 OF 11
OMIT_TABLE
=PPVDDQ_S3_CPU
AT21 VDDQ
AU13 VDDQ
AU15 VDDQ
AU19 VDDQ
AU23 VDDQ
AV11 VDDQ
AV17 VDDQ
AV21 VDDQ
AW10 VDDQ
AW14 VDDQ
AT18 VDDQ
AW25 VDDQ
AY12 VDDQ
AY16 VDDQ
AY18 VDDQ
AY23 VDDQ
=PPVCC_S0_CPU
B35 VCC
B36 VCC
B37 VCC
C25 VCC
C26 VCC
C27 VCC
C28 VCC
C29 VCC
C30 VCC
C32 VCC
C34 VCC
C36 VCC
D25 VCC
D27 VCC
D29 VCC
D31 VCC
D32 VCC
D33 VCC
D34 VCC
D35 VCC
D36 VCC
E24 VCC
E25 VCC
E26 VCC
E27 VCC
E28 VCC
E29 VCC
E30 VCC
E32 VCC
E34 VCC
E36 VCC
F23 VCC
F24 VCC
F25 VCC
F27 VCC
F29 VCC
F31 VCC
F32 VCC
F33 VCC
F34 VCC
G23 VCC
G24 VCC
G25 VCC
G26 VCC
G27 VCC
G28 VCC
G29 VCC
G30 VCC
G32 VCC
H22 VCC
H23 VCC
H25 VCC
H27 VCC
H29 VCC
H31 VCC
H32 VCC
J21 VCC
J22 VCC
J23 VCC
J24 VCC
J25 VCC
J26 VCC
J27 VCC
J28 VCC
J29 VCC
J30 VCC
J31 VCC
K16 VCC
K18 VCC
K20 VCC
K21 VCC
K23 VCC
K25 VCC
K27 VCC
K29 VCC
K31 VCC
L14 VCC
L15 VCC
L16 VCC
L17 VCC
L18 VCC
L19 VCC
L20 VCC
L21 VCC
L22 VCC
L23 VCC
L24 VCC
A25 VCC
A26 VCC
A27 VCC
A28 VCC
A29 VCC
A30 VCC
AJ11 VCC
AJ12 VCC
AJ13 VCC
AJ14 VCC
AJ15 VCC
AJ16 VCC
AJ17 VCC
AJ18 VCC
AJ19 VCC
AJ20 VCC
AJ21 VCC
AJ22 VCC
B25 VCC
B27 VCC
B29 VCC
B31 VCC
B32 VCC
B33 VCC
B34 VCC
M30 VCC
M28 VCC
M26 VCC
M24 VCC
M22 VCC
M20 VCC
M18 VCC
M16 VCC
M14 VCC
M13 VCC
L30 VCC
L29 VCC
L28 VCC
L27 VCC
L26 VCC
L25 VCC
=PPVCC_S0_CPU
R0800 100 5% 1/20W MF 201
VCC_SENSE
VSS_SENSE
C38 VCC_SENSE
D38 VSS_SENSE
R0801 100 5% 1/20W MF 201
U0500
SKYLAKE_S
SR2BX-PRQ-943469
LGA-SKT
SYM 6 OF 11
POWER
OMIT_TABLE
=PPVCCGT_S0_CPU
AA34 VCCGT
AA35 VCCGT
AA36 VCCGT
AA37 VCCGT
AA38 VCCGT
AB33 VCCGT
AB34 VCCGT
G36 VCCGT
G37 VCCGT
G38 VCCGT
G39 VCCGT
G40 VCCGT
H36 VCCGT
H38 VCCGT
H40 VCCGT
J36 VCCGT
J37 VCCGT
J38 VCCGT
J39 VCCGT
J40 VCCGT
K36 VCCGT
K38 VCCGT
K40 VCCGT
L34 VCCGT
L35 VCCGT
L36 VCCGT
L37 VCCGT
L38 VCCGT
L39 VCCGT
L40 VCCGT
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M34 VCCGT
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M38 VCCGT
M40 VCCGT
N34 VCCGT
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N36 VCCGT
N37 VCCGT
N38 VCCGT
N39 VCCGT
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P34 VCCGT
P36 VCCGT
P38 VCCGT
P40 VCCGT
R34 VCCGT
R35 VCCGT
R36 VCCGT
R37 VCCGT
R38 VCCGT
R39 VCCGT
R40 VCCGT
T33 VCCGT
T34 VCCGT
T36 VCCGT
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T40 VCCGT
U34 VCCGT
U35 VCCGT
U36 VCCGT
U37 VCCGT
U38 VCCGT
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U40 VCCGT
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V34 VCCGT
V36 VCCGT
V38 VCCGT
V40 VCCGT
W34 VCCGT
W35 VCCGT
W36 VCCGT
W37 VCCGT
W38 VCCGT
Y33 VCCGT
Y34 VCCGT
Y36 VCCGT
Y38 VCCGT
F36 VSSGTX_SENSE
NC
=PPVCCIO_S0_CPU
AJ23 VCCIO
AK11 VCCIO
AK14 VCCIO
AK24 VCCIO
M8 VCCIO
P8 VCCIO
T8 VCCIO
U8 VCCIO
W8 VCCIO
=PP1V0_S3_CPU
=PPVDDQ_S3_CPU
=PPVCCSA_S0_CPU
V4 VCCPLL
AJ9 VCCPLL_OC
AA6 VCCSA
AA7 VCCSA
AB6 VCCSA
AB7 VCCSA
AB8 VCCSA
AC7 VCCSA
AC8 VCCSA
N7 VCCSA
P7 VCCSA
R7 VCCSA
T7 VCCSA
U7 VCCSA
V7 VCCSA
W7 VCCSA
Y6 VCCSA
Y7 VCCSA
Y8 VCCSA
=PPVCCSA_S0_CPU
=PPVCCIO_S0_CPU
R0802 100 5% 1/20W MF 201
R0803 100 5% 1/20W MF 201
PM_VCCST_PWRGD
R0807 6.04K 1% 1/10W MF-LF 402
R0808 2.8K 1% 1/10W MF-LF 402
VCCIO_SENSE
VSS_SAIO_SENSE
VCCSA_SENSE
PM_VCCST_PWRGD_CPU
AF4 VCCIO_SENSE
AE4 VSS_SAIO_SENSE
AD5 VCCSA_SENSE
U2 VCCST_PWRGD
=PP1V0_S3_CPU
R0804 100 5% 1/20W MF 201
V5 VCCST
V6 VCCST
=PPVCCGT_S0_CPU
R0805 100 5% 1/20W MF 201
VCCGT_SENSE
VSSGT_SENSE
R0806 100 5% 1/20W MF 201
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=J78_MLB
SYNC_DATE=06/30/2014
PAGE TITLE
CPU & CHIPSET: CPU Power
Apple Inc.
DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
BRANCH
PAGE 8 OF 119
SHEET 8 OF 87
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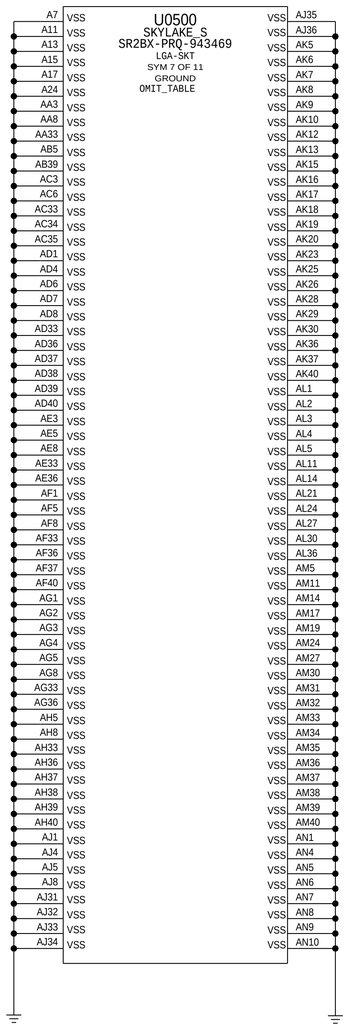

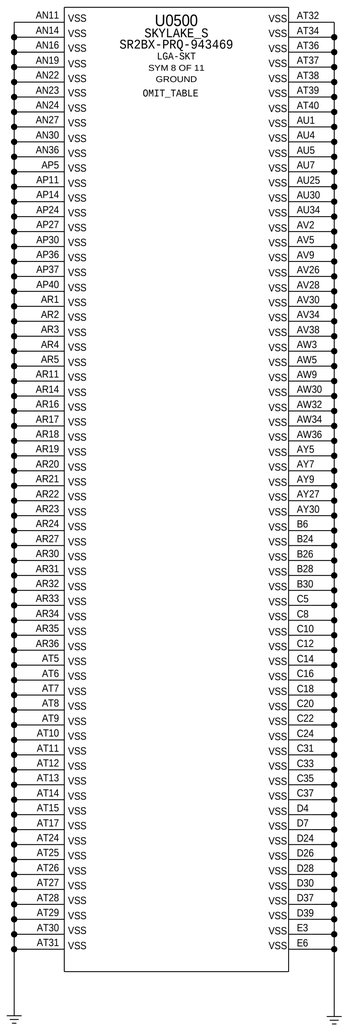

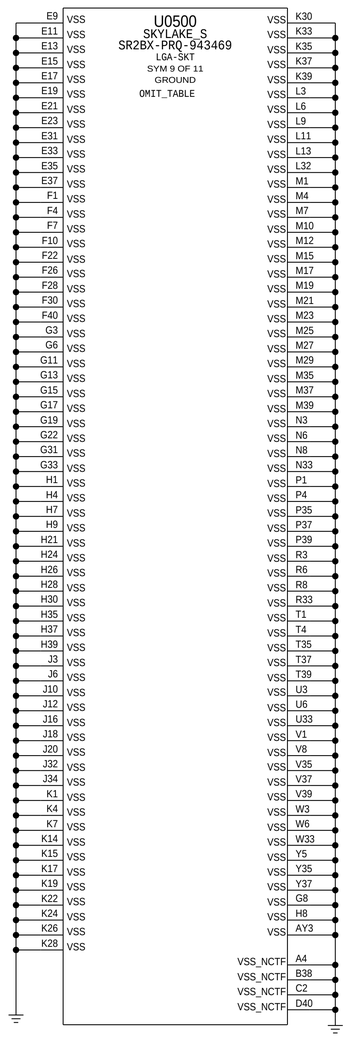

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU Ground

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

BRANCH

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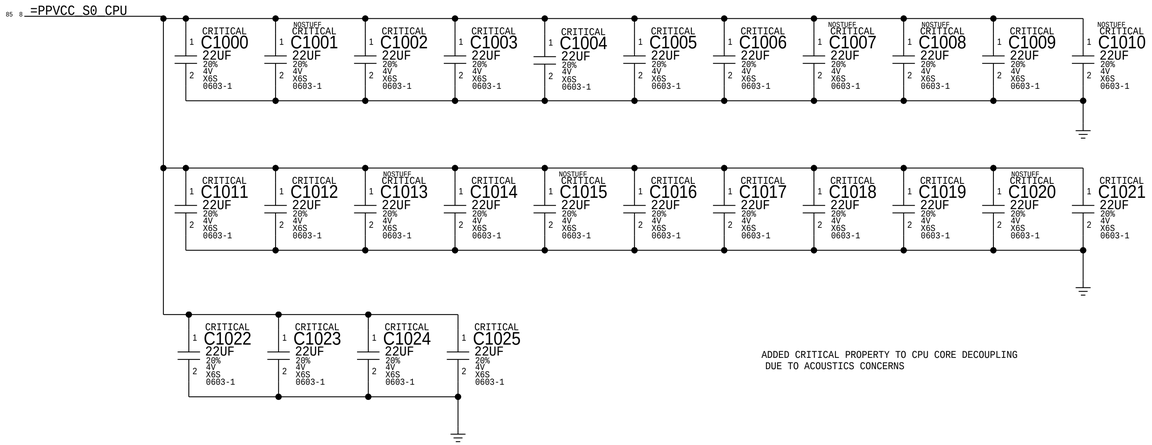
CPU VCORE DECOUPLING

Intel Recommendation:12x 22UF 0805 (top side cavity)
6x 22UF 0603 (top side cavity)
5x 22UF 0805 (top side outside cavity)

Apple Implementation:26x 22UF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71



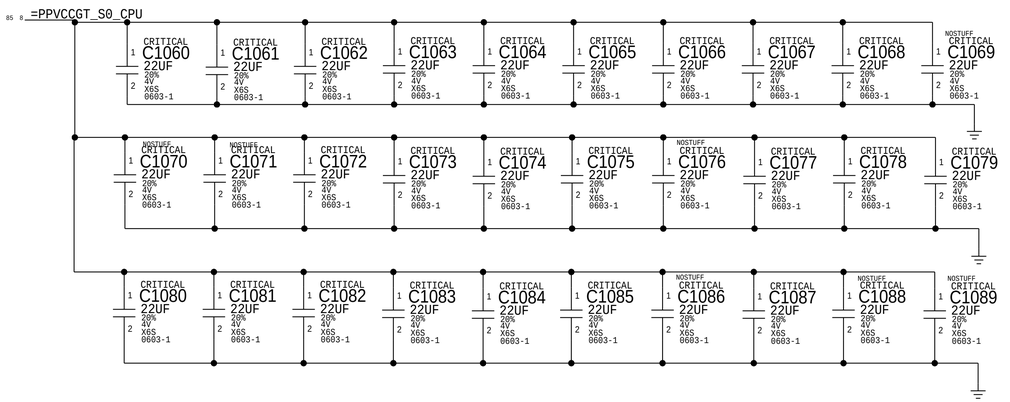
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

Intel Recommendation:9x 47UF 0805 (top side cavity)
4x 47UF 0805 (top side outside cavity)

Apple Implementation: 30x 22uF 0603

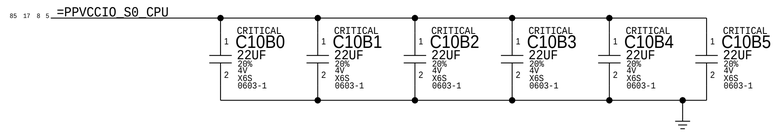
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:5x 22UF 0603 (top side cavity)
1x 22UF 0805 (top side cavity)

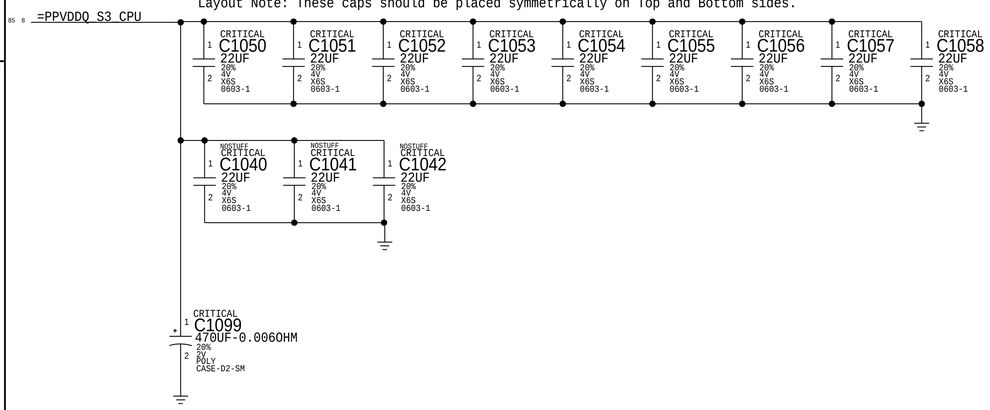
Apple Implementation:(following Intel recommendation w/ 0603)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:4x 22UF 0603 (top side outside cavity)

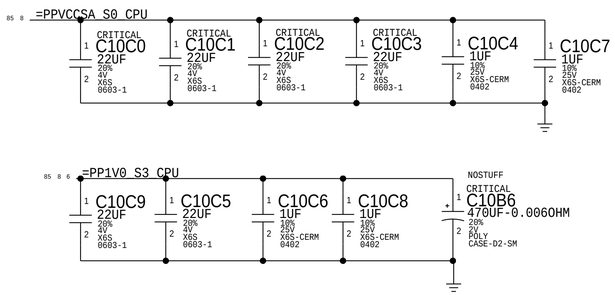
Apple Implementation:9x 22UF 0603 (J78 carry over)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCSA / VCCST+VCCPLL DECOUPLING

Intel Recommendation:2x 22UF 0603 near top side cavity

Apple Implementation: VCCST/VCCPLL: 1X 22UF 0603/2X 1UF 0402
Layout Note: These caps should be placed on top side cavity.



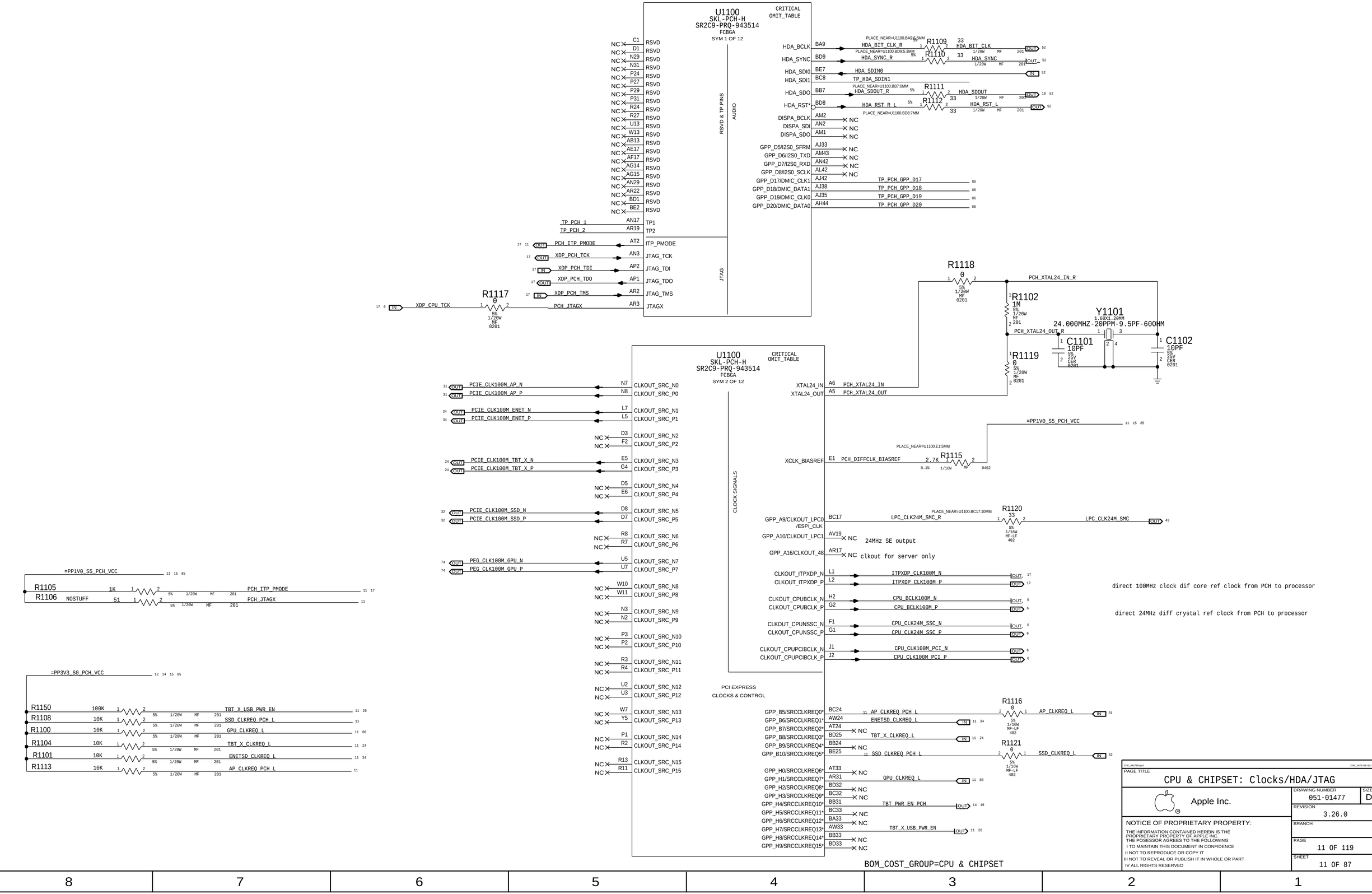
BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=harper SYNC_DATE=06/08/2016

PAGE TITLE
CPU & CHIPSET: CPU Decoupling

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D
REVISION 3.26.0
BRANCH
PAGE 10 OF 119
SHEET 10 OF 87


U1100
SKL-PCH-H
SR2C9-PRQ-943514
FCBGA
SYM 1 OF 12
CRITICAL
OMIT_TABLE
RSVD & TP PINS
AUDIO
JTAG
HDA_BCLK
HDA_SYNC
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_RST*
R1109
R1110
R1111
R1112
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_SDOUT_R
HDA_RST_R_L
HDA_BIT_CLK
HDA_SYNC
HDA_SDOUT
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
DISPA_BCLK
DISPA_SDI
DISPA_SDO
GPP_D5/I2S0_SFRM
GPP_D6/I2S0_TXD
GPP_D7/I2S0_RXD
GPP_D8/I2S0_SCLK
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
TP_PCH_GPP_D17
TP_PCH_GPP_D18
TP_PCH_GPP_D19
TP_PCH_GPP_D20
TP_PCH_1
TP_PCH_2
PCH_ITP_PMODE
XDP_PCH_TCK
XDP_PCH_TDI
XDP_PCH_TDO
XDP_PCH_TMS
PCH_JTAGX
XDP_CPU_TCK
R1117
R1118
R1102
R1119
Y1101
24.000MHZ-20PPM-9.5PF-60OHM
C1101
C1102
PCH_XTAL24_IN_R
PCH_XTAL24_OUT_R
U1100
SKL-PCH-H
SR2C9-PRQ-943514
FCBGA
SYM 2 OF 12
CRITICAL
OMIT_TABLE
CLOCK SIGNALS
PCI EXPRESS
CLOCKS & CONTROL
CLKOUT_SRC_N0
CLKOUT_SRC_P0
CLKOUT_SRC_N1
CLKOUT_SRC_P1
CLKOUT_SRC_N2
CLKOUT_SRC_P2
CLKOUT_SRC_N3
CLKOUT_SRC_P3
CLKOUT_SRC_N4
CLKOUT_SRC_P4
CLKOUT_SRC_N5
CLKOUT_SRC_P5
CLKOUT_SRC_N6
CLKOUT_SRC_P6
CLKOUT_SRC_N7
CLKOUT_SRC_P7
CLKOUT_SRC_N8
CLKOUT_SRC_P8
CLKOUT_SRC_N9
CLKOUT_SRC_P9
CLKOUT_SRC_N10
CLKOUT_SRC_P10
CLKOUT_SRC_N11
CLKOUT_SRC_P11
CLKOUT_SRC_N12
CLKOUT_SRC_P12
CLKOUT_SRC_N13
CLKOUT_SRC_P13
CLKOUT_SRC_N14
CLKOUT_SRC_P14
CLKOUT_SRC_N15
CLKOUT_SRC_P15
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_TBT_X_N
PCIE_CLK100M_TBT_X_P
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
PEG_CLK100M_GPU_N
PEG_CLK100M_GPU_P
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
PCH_DIFFCLK_BIASREF
R1115
=PP1V0_S5_PCH_VCC
LPC_CLK24M_SMC_R
LPC_CLK24M_SMC
R1120
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A16/CLKOUT_48
24MHz SE output
clkout for server only
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUBCLK_P
CPU_BCLK100M_N
CPU_BCLK100M_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUNSSC_P
CPU_CLK24M_SSC_N
CPU_CLK24M_SSC_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
CPU_CLK100M_PCI_N
CPU_CLK100M_PCI_P
direct 100MHz clock dif core ref clock from PCH to processor
direct 24MHz diff crystal ref clock from PCH to processor
GPP_B5/SRCCLKREQ0*
GPP_B6/SRCCLKREQ1*
GPP_B7/SRCCLKREQ2*
GPP_B8/SRCCLKREQ3*
GPP_B9/SRCCLKREQ4*
GPP_B10/SRCCLKREQ5*
GPP_H0/SRCCLKREQ6*
GPP_H1/SRCCLKREQ7*
GPP_H2/SRCCLKREQ8*
GPP_H3/SRCCLKREQ9*
GPP_H4/SRCCLKREQ10*
GPP_H5/SRCCLKREQ11*
GPP_H6/SRCCLKREQ12*
GPP_H7/SRCCLKREQ13*
GPP_H8/SRCCLKREQ14*
GPP_H9/SRCCLKREQ15*
AP_CLKREQ_PCH_L
ENETSD_CLKREQ_L
TBT_X_CLKREQ_L
SSD_CLKREQ_PCH_L
GPU_CLKREQ_L
TBT_PWR_EN_PCH
TBT_X_USB_PWR_EN
AP_CLKREQ_L
SSD_CLKREQ_L
R1116
R1121
BOM_COST_GROUP=CPU & CHIPSET
=PP1V0_S5_PCH_VCC
R1105
R1106
NOSTUFF
PCH_ITP_PMODE
PCH_JTAGX
=PP3V3_S0_PCH_VCC
R1150
R1108
R1100
R1104
R1101
R1113
TBT_X_USB_PWR_EN
SSD_CLKREQ_PCH_L
GPU_CLKREQ_L
TBT_X_CLKREQ_L
ENETSD_CLKREQ_L
AP_CLKREQ_PCH_L
PAGE TITLE
CPU & CHIPSET: Clocks/HDA/JTAG
Apple Inc.
DRAWING NUMBER
051-01477
SIZE
D
REVISION
3.26.0
BRANCH
PAGE
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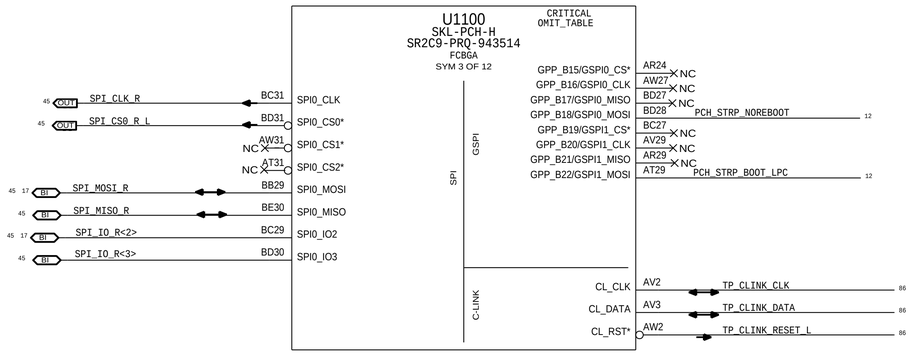

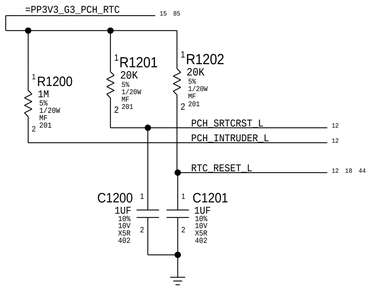

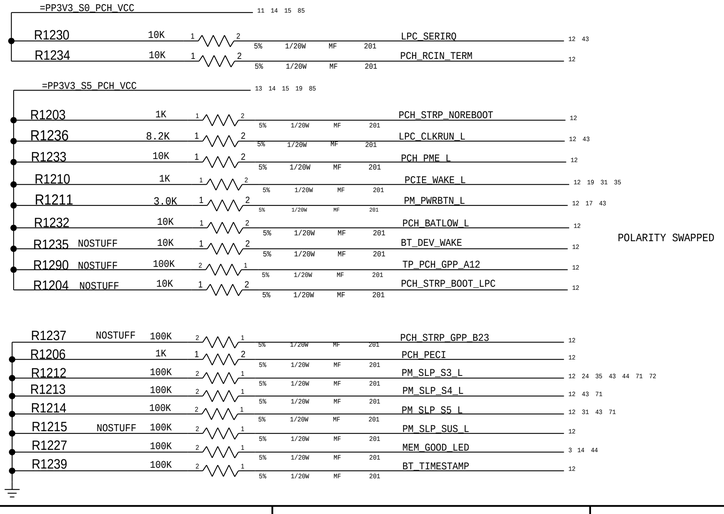

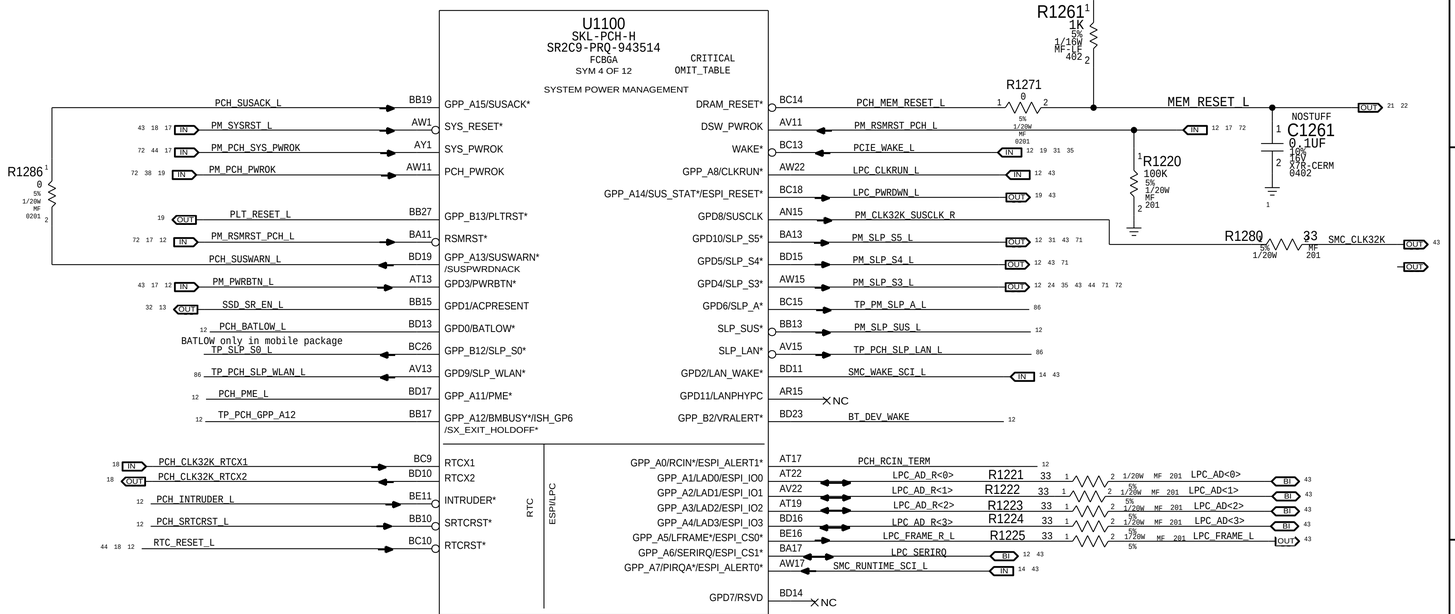

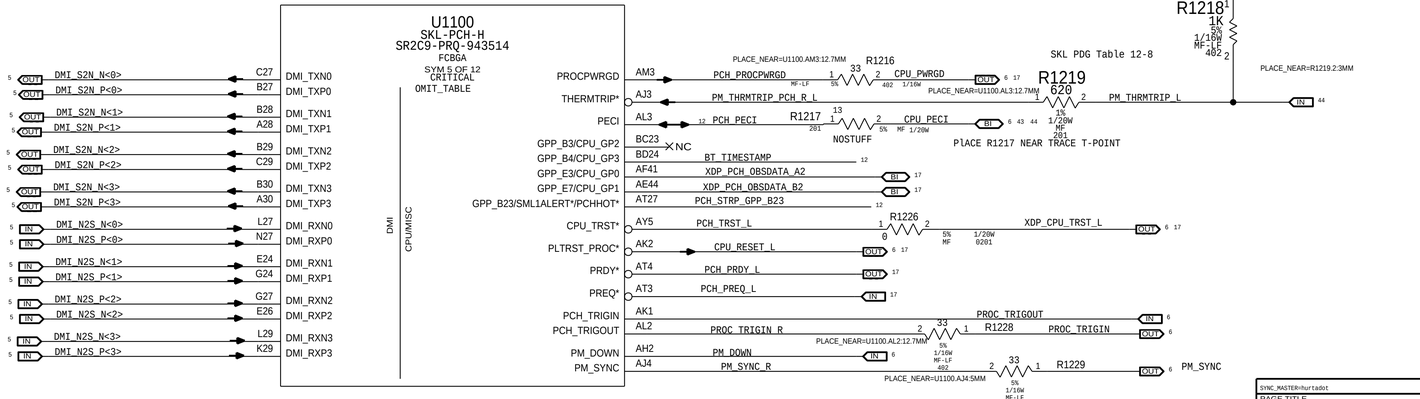

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=hurtadot SYNC_DATE=02/17/2016

PAGE TITLE

CPU & CHIPSET: PCH RTC/DMI/PM/CPU_Misc

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

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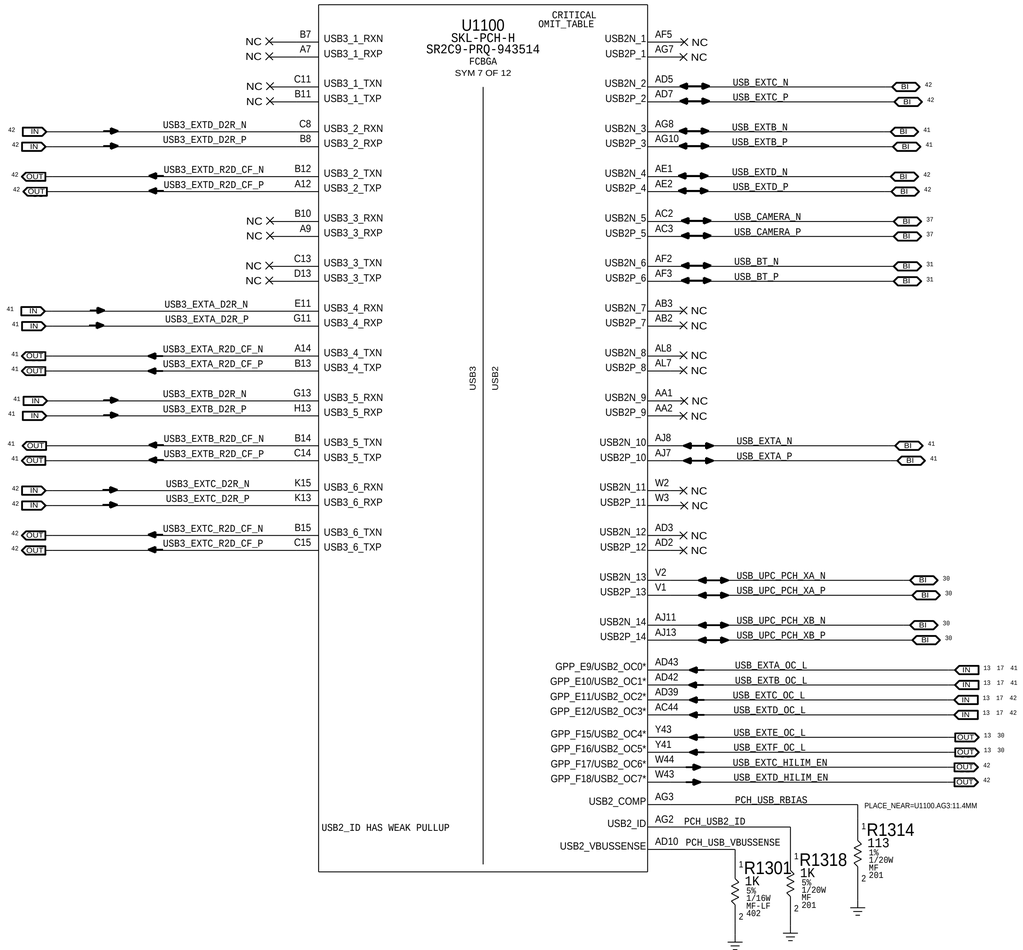
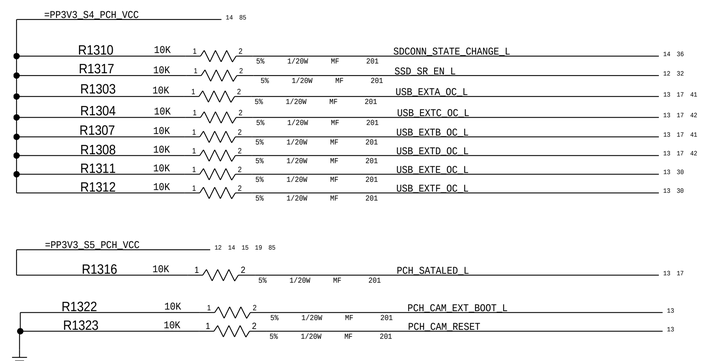
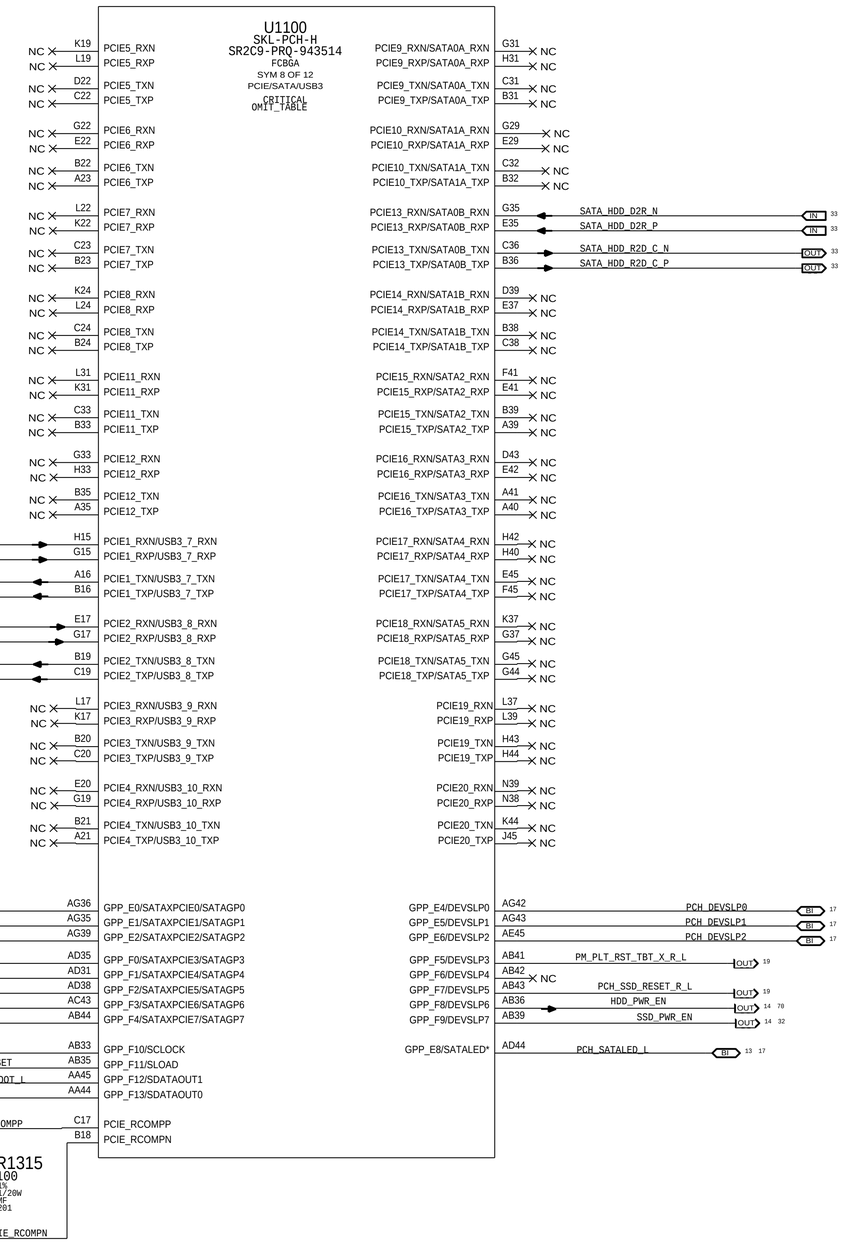
SHEET 12 OF 87







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=David SYNC_DATE=08/22/2013

PAGE TITLE

CPU & CHIPSET: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER 051-01477

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Board Rev[4:0]

POC: 11111
Proto0: 11110
Proto1: 11101
EVT: 11100 <<

U1100
SKL-PCH-H
SR2C9-PRQ-943514
FCBGA
SYM 6 OF 12

CRITICAL
OMIT_TABLE

GPP_A17/ISH_GP7 BC19 ENET_SD_RESET_R_L (19 OUT)
GPP_A18/ISH_GP0 BB22 AP_RESET_R_L (19 OUT)
GPP_A19/ISH_GP1 BD21 NC
GPP_A20/ISH_GP2 BD22 NC
GPP_A21/ISH_GP3 BE21 NC
GPP_A22/ISH_GP4 BD18 NC
GPP_A23/ISH_GP5 BC22 NC
GPPA/ INTEGRATED SENSOR

GPP_B0 AR27 NC
GPP_B1 AL27 NC
GPP_B11 AN24 MEM_GOOD_LED (44 12 3 OUT)
GPP_B14/SPKR BD26 PCH_STRP_TOPBLK_SWP_L (44 IN)
GPPB
GPPC/SMLINK/I2C/UART

GPP_D0 AL39 PCH_GPU_PWR_EN (14)
GPP_D1 AN36 PCH_GPU_RESET_R_L (19 OUT)
GPP_D2 AN38 USB_EXTA_HILIM_EN (41 OUT)
GPP_D3 AN41 USB_EXTB_HILIM_EN (41 OUT)
GPP_D9 AL44 NC
GPP_D10 AL36 GPU_ID (14)
GPP_D11 AL35 NC
GPP_D12 AJ39 NC
GPPD/INTEGRATED SENSOR/UART/I2C

GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA AK45 PCH_BOARD_REV<0>
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL AK44 PCH_BOARD_REV<1>
GPP_D15/ISH_UART0_RTS* AL43 PCH_BOARD_REV<2>
GPP_D16/ISH_UART0_CTS* AJ43 PCH_BOARD_REV<3>
GPP_D21 AG44 PCH_BOARD_REV<4>
GPP_D22 AH43 NC
GPP_D4/ISH_I2C2_SDA/I2C3_SDA AM44 NC
GPP_D23/ISH_I2C2_SCL/I2C3_SCL AJ44 TP_PCH_GPP_D23 (86)

GPP_C0/SMBCLK AW44 SMBUS_PCH_CLK (OUT 46)
GPP_C1/SMBDATA BB43 SMBUS_PCH_DATA (BI 46)
GPP_C2/SMBALERT* BB41 PCH_SMBALERT_L (14)
GPP_C3/SML0CLK AY44 SML_PCH_0_CLK (OUT 46)
GPP_C4/SML0DATA BB39 SML_PCH_0_DATA (BI 46)
GPP_C5/SML0ALERT* BA40 PCH_STRP_LPC_L (14)
GPP_C6/SML1CLK AW42 SML_PCH_1_CLK (IN 46)
GPP_C7/SML1DATA AW45 SML_PCH_1_DATA (BI 46)
GPP_C8/UART0_RXD BA41 NC
GPP_C9/UART0_TXD AV44 NC
GPP_C10/UART0_RTS* AV43 NC
GPP_C11/UART0_CTS* AU44 NC
GPP_C12/UART1_RXD/ISH_UART1_RXD AU43 NC
GPP_C13/UART1_TXD/ISH_UART1_TXD AT43 NC
GPP_C14/UART1_RTS*/ISH_UART1_RTS* AT44 NC
GPP_C15/UART1_CTS*/ISH_UART1_CTS* AU41 NC
GPP_C16/I2C0_SDA AT42 NC
GPP_C17/I2C0_SCL AR38 NC
GPP_C18/I2C1_SDA AR44 NC
GPP_C19/I2C1_SCL AR41 NC
GPP_C20/UART2_RXD AR45 NC
GPP_C21/UART2_TXD AR39 NC
GPP_C22/UART2_RTS* AN44 NC
GPP_C23/UART2_CTS* AN43 NC

R1447 1K 5% 1/20W MF 201 (PCH_BOARD_REV<0>)
R1446 1K 5% 1/20W MF 201 (PCH_BOARD_REV<1>)
NOSTUFF R1445 1K 5% 1/20W MF 201 (PCH_BOARD_REV<2>)
NOSTUFF R1444 1K 5% 1/20W MF 201 (PCH_BOARD_REV<3>)
NOSTUFF R1449 1K 5% 1/20W MF 201 (PCH_BOARD_REV<4>)

U1100
SKL-PCH-H
SR2C9-PRQ-943514
FCBGA
SYM 9 OF 12

CRITICAL
OMIT_TABLE

GPP_F14 Y44 ENET_LOW_PWR_PCH (19 14 OUT)
GPP_F19/EDP_VDDEN W42 NC
GPP_F20/EDP_BKLTEN W35 NC
GPP_F21/EDP_BKLTCTL W36 NC
GPP_F22 W39 NC
GPP_F23 V44 SPIROM_USE_MLB (45 BI)
GPPF/ BACKLIGHT

GPP_I0/DDPB_HPD0 AW4 NC
GPP_I1/DDPC_HPD1 AY2 NC
GPP_I2/DDPD_HPD2 AV4 NC
GPP_I3/DDPE_HPD3 BA4 NC
GPP_I4/EDP_HPD BD7 PCH_EDP_HPD_PD
GPP_I5/DDPB_CTRLCLK BA5 NC
GPP_I6/DDPB_CTRLDATA BC4 NC
GPP_I7/DDPC_CTRLCLK BB3 NC
GPP_I8/DDPC_CTRLDATA BD6 NC
GPP_I9/DDPD_CTRLCLK BE5 NC
GPP_I10/DDPD_CTRLDATA BE6 NC
GPPI/DISPLAY
GPPG

GPP_H10/SML2CLK BD34 JTAG_ISP_TDO_PCH (19 14 IN)
GPP_H11/SML2DATA AW35 JTAG_ISP_TDI_PCH (19 14 OUT)
GPP_H12/SML2ALERT* BD35 JTAG_ISP_TCK (19 14 OUT)
GPP_H13/SML3CLK BC35 JTAG_TBT_TMS_PCH (19 14 OUT)
GPP_H14/SML3DATA BA35 NC
GPP_H15/SML3ALERT* BB36 NC
GPP_H16/SML4CLK BD39 PCH_DP_TBT_SEL (14)
GPP_H17/SML4DATA BE34 ENET_MEDIA_SENSE (34 14 IN)
GPP_H18/SML4ALERT* BC36 BKLT_FAULT_INT_L (68 IN)
GPP_H19/ISH_I2C0_SDA BB38 SDCONN_STATE_CHANGE_L (36 13 IN)
GPP_H20/ISH_I2C0_SCL BC38 SDCONN_OC_L (36 14 IN)
GPP_H21/ISH_I2C1_SDA BE39 TBT_X_CIO_PLUG_EVENT_L (26 24 19 IN)
GPP_H22/ISH_I2C1_SCL BD38 NC
GPP_H23 BD36 NC
GPPH/I2C/INTEGRATED SENSOR /SMLINK

GPP_G0/FAN_TACH_0 U43 SSD_BFH_L (OUT 14 32)
GPP_G1/FAN_TACH_1 U42 NC
GPP_G2/FAN_TACH_2 U41 NC
GPP_G3/FAN_TACH_3 M44 NC
GPP_G4/FAN_TACH_4 U36 NC
GPP_G5/FAN_TACH_5 P44 NC
GPP_G6/FAN_TACH_6 T45 NC
GPP_G7/FAN_TACH_7 T44 NC
GPP_G8/FAN_PWM_0 R44 NC
GPP_G9/FAN_PWM_1 R43 PCH_BT_ROM_BOOT (OUT 31)
GPP_G10/FAN_PWM_2 U39 NC
GPP_G11/FAN_PWM_3 N42 NC
GPP_G12/GSXDOUT R39 NC
GPP_G13/GSXSLOAD R36 NC
GPP_G14/GSXDIN R42 NC
GPP_G15/GSXSRESET* R41 NC
GPP_G16/GSXCLK P43 NC
GPP_G17/ADR_COMPLETE N44 NC
GPP_G18/NMI* N43 NC
GPP_G19/SMI* M45 NC
GPP_G20 R35 NC
GPP_G21 U35 AUD_IPHS_SWITCH_EN_PCH (14)
GPP_G22 L44 TP_AUD_IP_PERIPHERAL_DET
GPP_G23 L43 TP_AUD_I2C_INT_L

R1426 100K 5% 1/20W MF 201 (PCH_EDP_HPD_PD)
GPPI IS ON VCC3V3_PRIM

NOSTUFF R1491 0 5% 1/20W MF 201 (DP_TBT_SEL (44 49 OUT) ↔ PCH_DP_TBT_SEL)

PLACE_NEAR=U1100.M45:10MM
R1405 33 1/16W MF-LF 402 (TCON_RESET_L (39 OUT) ↔ TCON_RESET_R_L (14))

=PP3V3_S5_PCH_VCC (12 13 15 19 85)
R1406 10K SMC_RUNTIME_SCI_L (12 43)
R1412 10K SMC_WAKE_SCI_L (12 43)
R1427 10K HDD_PWR_EN (13 70)
R1404 100K PCH_SMBALERT_L (14)

=PP3V3_S4_PCH_VCC (13 85)
R1489 NOSTUFF 10K SSD_BFH_L (14 32)
R1429 10K SSD_PWR_EN (13 32)

=PP3V3_S0_PCH_VCC (11 12 15 85)
R1403 10K TBT_PWR_EN_PCH (11 19)
R1421 10K SDCONN_OC_L (14 36)
R1411 10K JTAG_TBT_TMS_PCH (14 19)
R1415 10K JTAG_ISP_TDO_PCH (14 19)
R1416 100K NOSTUFF JTAG_ISP_TDI_PCH (14 19)
R1425 10K TCON_RESET_R_L (14)
R1494 100K PCH_GPU_PWR_EN (14)

R1495 100K JTAG_ISP_TDI_PCH (14 19)
R1492 100K TBT_POC_RESET (13 26)
R1453 NOSTUFF 10K PCH_STRP_LPC_L (14)
R1490 100K AUD_IPHS_SWITCH_EN_PCH (14)
R1407 10K WOL_EN (13 35)
R1414 10K JTAG_ISP_TCK (14 19)
R1417 10K ENET_LOW_PWR_PCH (14 19)
R1451 10K ENET_MEDIA_SENSE (14 34)
R1424 10K PCH_DP_TBT_SEL (14)
R1454 10K GPU_ID (14)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU & CHIPSET: PCH GPIO/Misc

Apple Inc.

DRAWING NUMBER 051-01477
SIZE D
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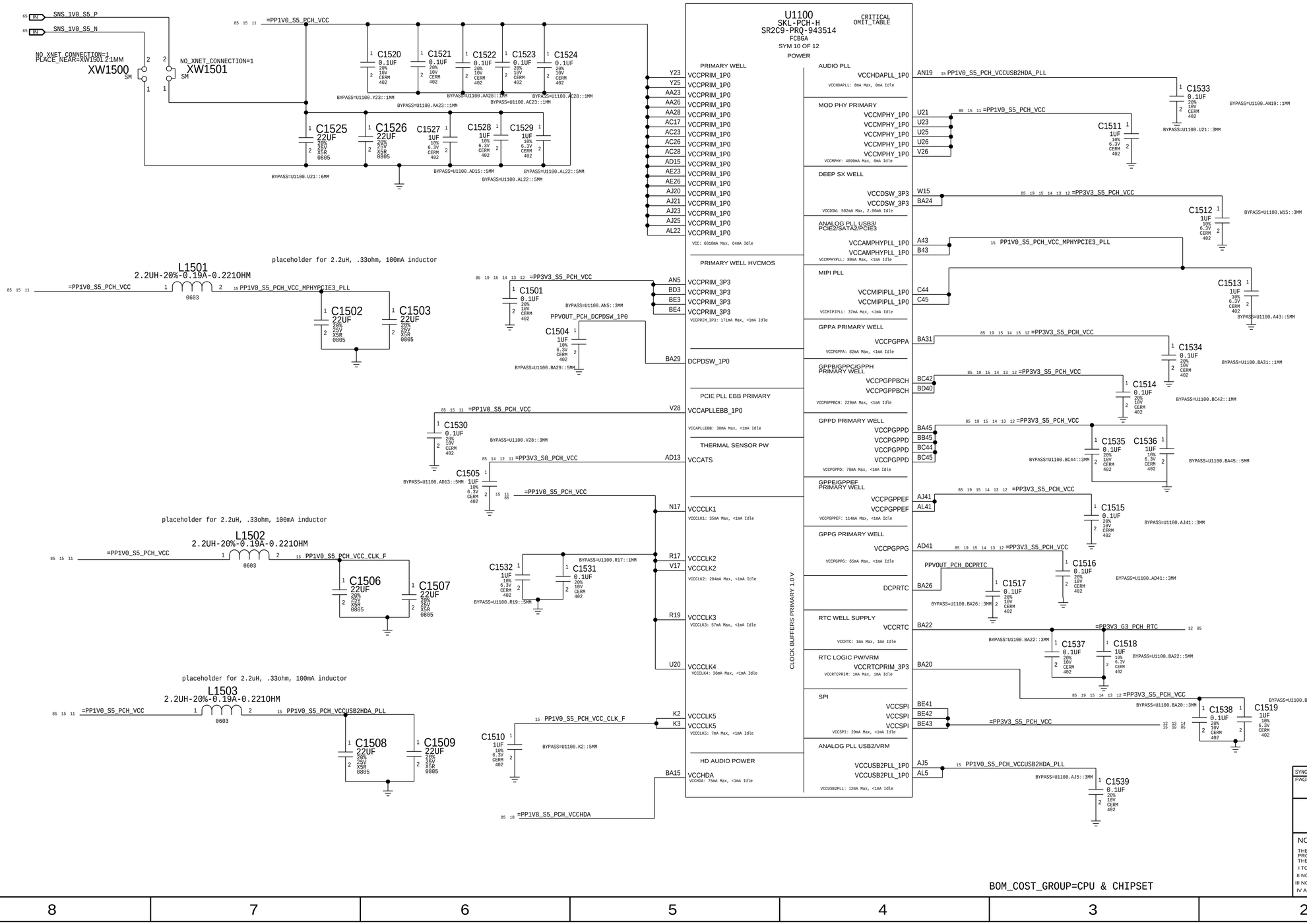

SYNC_MASTER=yeungr SYNC_DATE=03/14/2016

PAGE TITLE

CPU & CHIPSET: PCH Power/Decoupling

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

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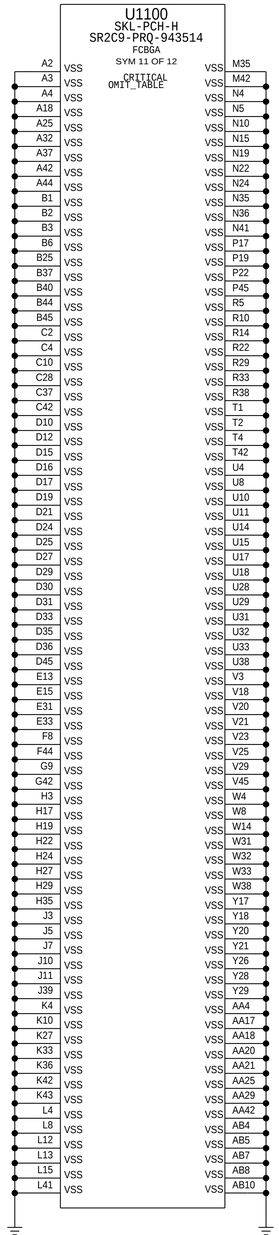

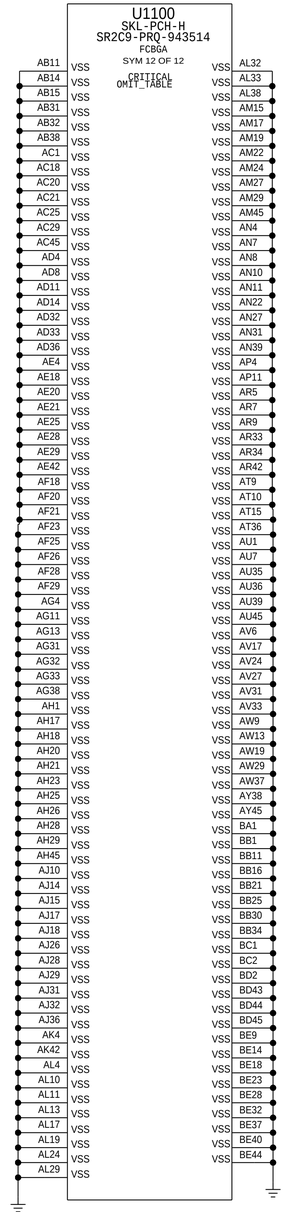

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J95_DEBORAH SYNC_DATE=10/20/2014

PAGE TITLE

CPU & CHIPSET: PCH Grounds

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

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Primary Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803

CRB has no-stuff S3 pull-up on PREQ_L
PDG allows any value from 51 to 3K

Connect Hook2 to CFG<0>
and pull-up to S0
(as in CRB)

Review PLACE_NEAR for these components:
R1800, R1820, R1838, R1861, R1891
<rdar://problem/24860021>

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

ICT CPU & PCH JTAG Test-Points:

TP1840 = TMS
TP1841 = TDI
TP1842 = TDO
TP1843 = TCK0
(TP1844 = TCK1)
TP1845 = DAISY
TP1846 = DAISY_L
TP1847 = TRST_L

NOTE: TDI and TMS are terminated in CPU.

ICT CPU & PCH JTAG Daisy-Chain Support (S0):

To configure CPU and PCH JTAG in an ICT Daisy-Chain:
Drive ICT_JTAG_DAISY to 5V and
drive ICT_JTAG_DAISY_L to Ground.

Secondary (PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

PCH SIGNALS / XDP SIGNALS

PCH SIGNALS		XDP SIGNALS
PCH_PREQ_L	R1890	XDP_PCH_PREQ_L
PCH_PRDY_L	R1893	XDP_PCH_PRDY_L
PCH_SATAXPCIE0_SATAGP0	R1894	XDP_PCH_SATAXPCIE0_SATAGP0
PCH_SATAXPCIE1_SATAGP1	R1895	XDP_PCH_SATAXPCIE1_SATAGP1
PCH_SATAXPCIE2_SATAGP2	R1880	XDP_PCH_SATAXPCIE2_SATAGP2
PCH_SATAXPCIE3_SATAGP3	R1881	XDP_PCH_SATAXPCIE3_SATAGP3
PCH_SATAXPCIE4_SATAGP4	R1896	XDP_PCH_SATAXPCIE4_SATAGP4
PCH_SATAXPCIE5_SATAGP5	R1897	XDP_PCH_SATAXPCIE5_SATAGP5
PCH_SATAXPCIE6_SATAGP6	R1872	XDP_PCH_SATAXPCIE6_SATAGP6
PCH_SATAXPCIE7_SATAGP7	R1873	XDP_PCH_SATAXPCIE7_SATAGP7
XDP_PCH_OBSDATA_A2	R1874	XDP_PCH_CPU_GP0
PCH_DEVSLP0	R1875	XDP_PCH_DEVSLP0
PCH_ITP_PMODE	R1878	XDP_PCH_ITP_PMODE
PCH_DEVSLP1	R1879	XDP_PCH_DEVSLP1
PCH_DEVSLP2	R1882	XDP_PCH_DEVSLP2
XDP_PCH_OBSDATA_B2	R1883	XDP_PCH_CPU_GP1
PCH_SATALED_L	R1886	XDP_PCH_SATALED_L
PM_RSMRST_PCH_L	R1887	XDP_PCH_RSMRST_L
PM_SYSRST_L	R1884	XDP_PM_SYSRST_L
USB_EXTA_OC_L	R1833	XDP_PCH_USB2_0C0_L
USB_EXTB_OC_L	R1835	XDP_PCH_USB2_0C1_L
USB_EXTC_OC_L	R1832	XDP_PCH_USB2_0C2_L
USB_EXTD_OC_L	R1834	XDP_PCH_USB2_0C3_L

PCH/XDP Signal Isolation Notes:

R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU & CHIPSET: XDP
Apple Inc.	DRAWING NUMBER 051-01477
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	REVISION 3.26.0
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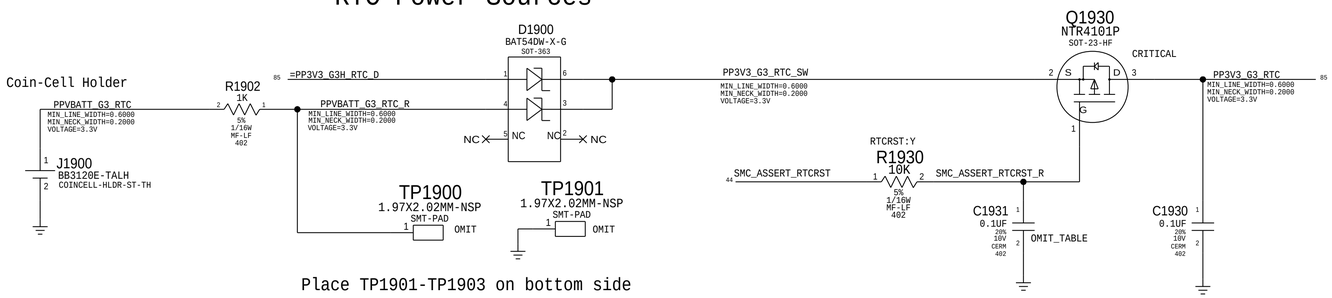
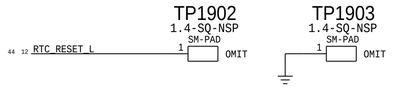
RTC Power Sources

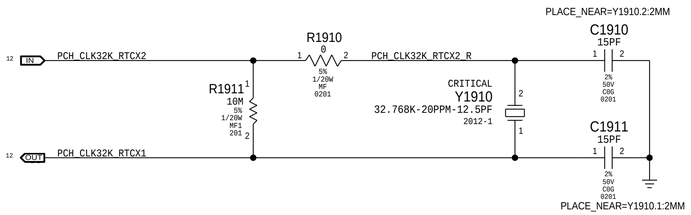


Place TP1901-TP1903 on bottom side

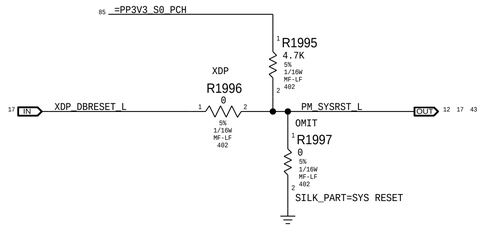


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K ohm,402	C1931	RTCRST:N

PCH RTC Crystal

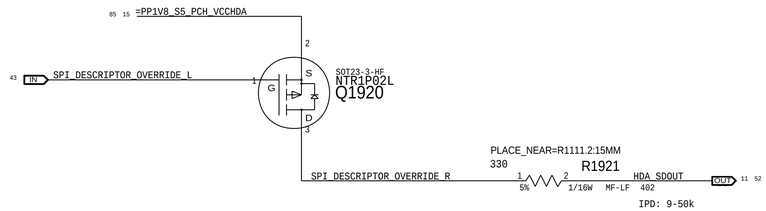


PCH Reset Button



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=hurtadot SYNC_DATE=12/09/2015

PAGE TITLE

Chipset Support

Apple Inc.

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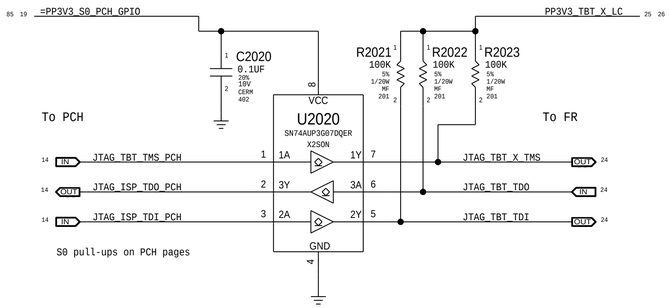
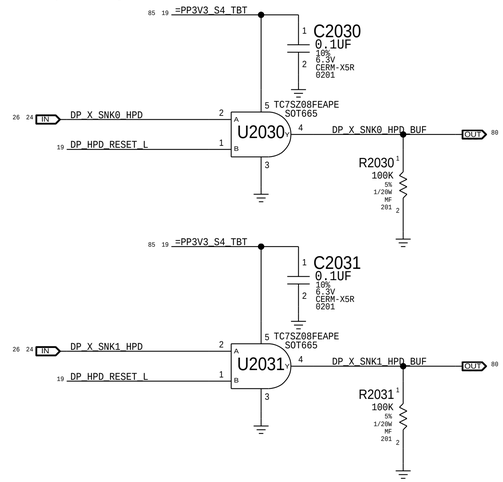
Alpine Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH



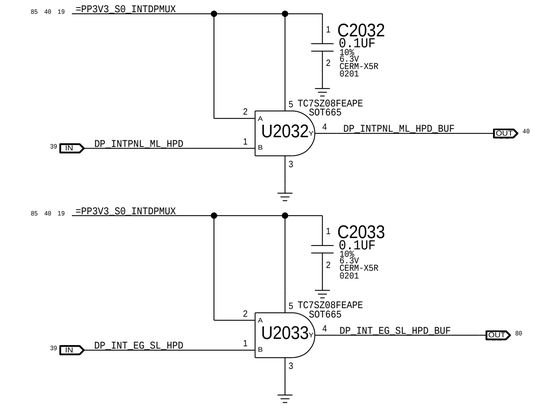
Alpine Ridge HPD Isolation

NOTE: PLT_RESET_L used as other input to the AND gate so that HPD
is only driven high to the PCH in S0.

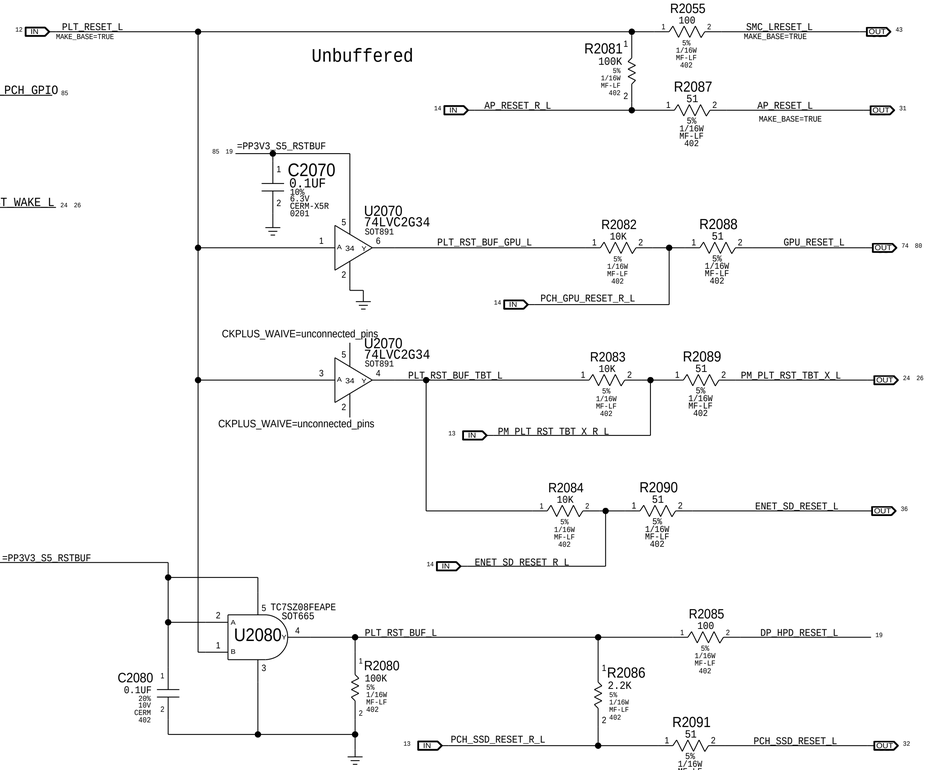


Internal Display HPD Isolation

NOTE: PP3V3_S0 used as other input to the AND gate so that HPD
is only driven high when PCH 3V3_S0 is up.

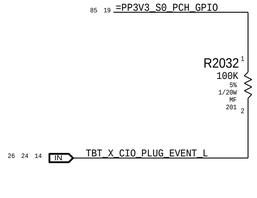


Platform Reset Connections

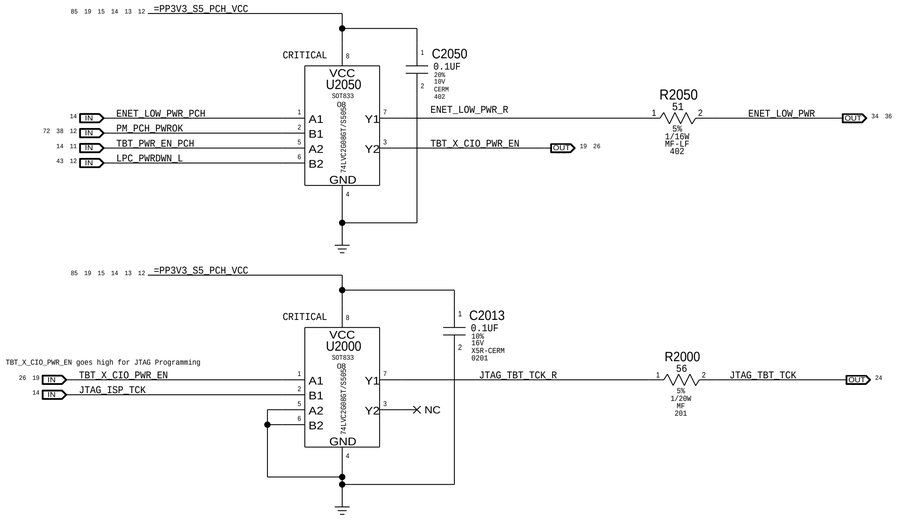


Alpine Ridge Support

FR output is open-drain, no isolation necessary



GPIO Glitch Prevention



Add series resistor to reduce over/undershoot <rdar://problem/26333074>

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=davidd
SYNC_DATE=03/22/2016

PAGE TITLE
Project-Specific Chipset Support

Apple Inc.

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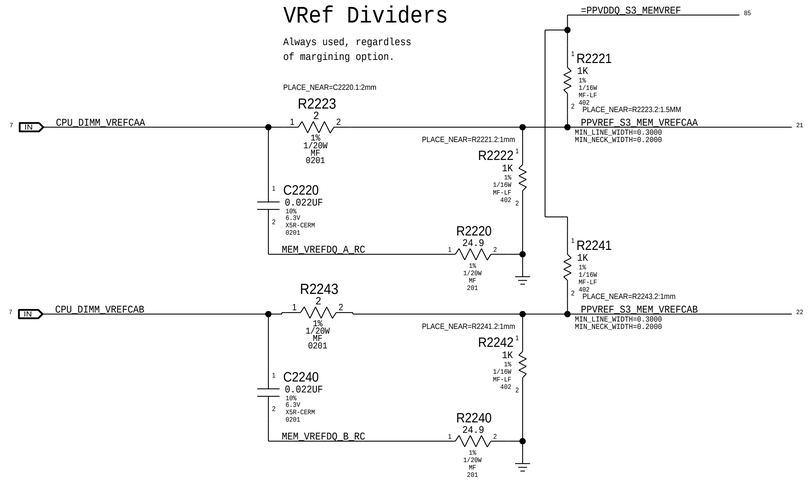
VRef Dividers

Always used, regardless
of margining option.



BOM_COST_GROUP=DRAM

SYNC_MASTER=mlb_skl_am SYNC_DATE=07/09/2015

PAGE TITLE

DRAM: VREF/VTT EN

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

BRANCH

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Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVTT_S0_MEM_A

C2350 1UF 10% 10V X5S 402
C2351 1UF 10% 10V X5S 402
C2352 1UF 10% 10V X5S 402
C2353 1UF 10% 10V X5S 402
C2354 10UF 20% 6.3V CERM-X6S 0402

=PPDDRVPP_S3_MEM_A

C2330 10UF 20% 6.3V CERM-X6S 0402
C2331 1UF 10% 10V X5R 402
BYPASS=J2300.257::2MM

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C2310 1UF 20% 6.3V X6S-CERM 0201
C2311 1UF 20% 6.3V X6S-CERM 0201
C2312 1UF 20% 6.3V X6S-CERM 0201
C2313 1UF 20% 6.3V X6S-CERM 0201
C2314 1UF 20% 6.3V X6S-CERM 0201
C2315 1UF 20% 6.3V X6S-CERM 0201
C2316 1UF 20% 6.3V X6S-CERM 0201
C2317 1UF 20% 6.3V X6S-CERM 0201

C2300 10UF 20% 6.3V CERM-X6S 0402
C2301 10UF 20% 6.3V CERM-X6S 0402
C2318 10UF 20% 6.3V CERM-X6S 0402
C2319 10UF 20% 6.3V CERM-X6S 0402
C2320 10UF 20% 6.3V CERM-X6S 0402
C2321 10UF 20% 6.3V CERM-X6S 0402
C2322 10UF 20% 6.3V CERM-X6S 0402
C2323 10UF 20% 6.3V CERM-X6S 0402

CRITICAL C2324 470UF-0.0060HM 20% 20V CASE-D2-SM
NOSTUFF CRITICAL C2325 470UF-0.0060HM 20% 20V CASE-D2-SM

PPVREF_S3_MEM_VREFCAA

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 10% 10V CERM 402

=PP3V3_S0_MEM_A_SPD
MEM_DIMMA_SA<2>
MEM_DIMMA_SA<1>
MEM_DIMMA_SA<0>

R2340 10K 5% 1/16W ME-LF 402
R2341 10K 5% 1/16W ME-LF 402
R2342 10K 5% 1/16W ME-LF 402
C2340 2.2UF 20% 6.3V CERM 402-LF
C2341 0.1UF 20% 10V CERM 402

P/N: 998-05061

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 1 OF 3

MEM_A_A<16>	152	RAS*/A16	
MEM_A_A<15>	156	CAS*/A15	
MEM_A_A<14>	151	WE*/A14	
MEM_A_A<13>	158	A13	
MEM_A_A<12>	119	A12	
MEM_A_A<11>	120	A11	
MEM_A_A<10>	146	A10/AP	
MEM_A_A<9>	121	A9	
MEM_A_A<8>	125	A8	
MEM_A_A<7>	122	A7	
MEM_A_A<6>	127	A6	
MEM_A_A<5>	126	A5	
MEM_A_A<4>	128	A4	
MEM_A_A<3>	131	A3	
MEM_A_A<2>	132	A2	
MEM_A_A<1>	133	A1	
MEM_A_A<0>	144	A0	
MEM_A_BA<1>	145	BA1	
MEM_A_BA<0>	150	BA0	
MEM_A_CLK_P<1>	138	CK1_T/NF	
MEM_A_CLK_N<1>	140	CK1_C/NF	
MEM_A_CLK_P<0>	137	CK0_T	
MEM_A_CLK_N<0>	139	CK0_C	
NC	165	C1/CS3*/NC	
NC	162	C0/CS2*/NC	
MEM_A_CS_L<1>	157	CS1*/NC	
MEM_A_CS_L<0>	149	CS0*	
MEM_A_CKE<1>	110	CKE1/NC	
MEM_A_CKE<0>	109	CKE0	
MEM_A_BG<1>	113	BG1	
MEM_A_BG<0>	115	BG0	
MEM_A_ODT<1>	161	ODT1/NC	
MEM_A_ODT<0>	155	ODT0	
MEM_A_PARITY	143	PARITY	
NC	104	CB7/NC	
NC	100	CB6/NC	
NC	87	CB5/NC	
NC	88	CB4/NC	
NC	105	CB3/NC	
NC	101	CB2/NC	
NC	91	CB1/NC	
NC	92	CB0/NC	
MEM_RESET_L	108	RESET*	
=PP3V3_S0_MEM_A_SPD	255	VDDSPD	
MEM_DIMMA_SA<2>	166	SA2	
MEM_DIMMA_SA<1>	260	SA1	
MEM_DIMMA_SA<0>	256	SA0	
=I2C_SODIMMA_SDA	254	SDA	
=I2C_SODIMMA_SCL	253	SCL	
PPVREF_S3_MEM_VREFCAA	164	VREFCA	
=PPDDRVPP_S3_MEM_A	257	VPP	
	259	VPP	
MEM_A_ACT_L	114	ACT*	
MEM_A_ALERT_L	116	ALERT*	

DQ63	246	=MEM_A_DQ<63>	
DQ62	245	=MEM_A_DQ<62>	
DQ61	233	=MEM_A_DQ<61>	
DQ60	232	=MEM_A_DQ<60>	
DQ59	250	=MEM_A_DQ<59>	
DQ58	249	=MEM_A_DQ<58>	
DQ57	236	=MEM_A_DQ<57>	
DQ56	237	=MEM_A_DQ<56>	
DQ55	225	=MEM_A_DQ<55>	
DQ54	224	=MEM_A_DQ<54>	
DQ53	212	=MEM_A_DQ<53>	
DQ52	211	=MEM_A_DQ<52>	
DQ51	229	=MEM_A_DQ<51>	
DQ50	228	=MEM_A_DQ<50>	
DQ49	215	=MEM_A_DQ<49>	
DQ48	216	=MEM_A_DQ<48>	
DQ47	204	=MEM_A_DQ<47>	
DQ46	203	=MEM_A_DQ<46>	
DQ45	190	=MEM_A_DQ<45>	
DQ44	191	=MEM_A_DQ<44>	
DQ43	208	=MEM_A_DQ<43>	
DQ42	207	=MEM_A_DQ<42>	
DQ41	194	=MEM_A_DQ<41>	
DQ40	195	=MEM_A_DQ<40>	
DQ39	182	=MEM_A_DQ<39>	
DQ38	183	=MEM_A_DQ<38>	
DQ37	169	=MEM_A_DQ<37>	
DQ36	170	=MEM_A_DQ<36>	
DQ35	186	=MEM_A_DQ<35>	
DQ34	187	=MEM_A_DQ<34>	
DQ33	173	=MEM_A_DQ<33>	
DQ32	174	=MEM_A_DQ<32>	
DQ31	80	=MEM_A_DQ<31>	
DQ30	79	=MEM_A_DQ<30>	
DQ29	67	=MEM_A_DQ<29>	
DQ28	66	=MEM_A_DQ<28>	
DQ27	84	=MEM_A_DQ<27>	
DQ26	83	=MEM_A_DQ<26>	
DQ25	71	=MEM_A_DQ<25>	
DQ24	70	=MEM_A_DQ<24>	
DQ23	59	=MEM_A_DQ<23>	
DQ22	58	=MEM_A_DQ<22>	
DQ21	45	=MEM_A_DQ<21>	
DQ20	46	=MEM_A_DQ<20>	
DQ19	63	=MEM_A_DQ<19>	
DQ18	62	=MEM_A_DQ<18>	
DQ17	49	=MEM_A_DQ<17>	
DQ16	50	=MEM_A_DQ<16>	
DQ15	37	=MEM_A_DQ<15>	
DQ14	38	=MEM_A_DQ<14>	
DQ13	25	=MEM_A_DQ<13>	
DQ12	24	=MEM_A_DQ<12>	
DQ11	42	=MEM_A_DQ<11>	
DQ10	41	=MEM_A_DQ<10>	
DQ9	29	=MEM_A_DQ<9>	
DQ8	28	=MEM_A_DQ<8>	
DQ7	17	=MEM_A_DQ<7>	
DQ6	16	=MEM_A_DQ<6>	
DQ5	3	=MEM_A_DQ<5>	
DQ4	4	=MEM_A_DQ<4>	
DQ3	21	=MEM_A_DQ<3>	
DQ2	20	=MEM_A_DQ<2>	
DQ1	7	=MEM_A_DQ<1>	
DQ0	8	=MEM_A_DQ<0>	
EVENT*/NF	134	MEM_EVENT_L	

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 2 OF 3

DM8*/DBI*/NC	96	=PPVDDQ_S3_MEM_A
DM7*/DBI7*	241	
DM6*/DBI6*	220	
DM5*/DBI5*	199	
DM4*/DBI4*	178	
DM3*/DBI3*	75	
DM2*/DBI2*	54	
DM1*/DBI*	33	
DM0*/DBI0*	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	=MEM_A_DQS_P<7>
DQS7_C	240	=MEM_A_DQS_N<7>
DQS6_T	221	=MEM_A_DQS_P<6>
DQS6_C	219	=MEM_A_DQS_N<6>
DQS5_T	200	=MEM_A_DQS_P<5>
DQS5_C	198	=MEM_A_DQS_N<5>
DQS4_T	179	=MEM_A_DQS_P<4>
DQS4_C	177	=MEM_A_DQS_N<4>
DQS3_T	76	=MEM_A_DQS_P<3>
DQS3_C	74	=MEM_A_DQS_N<3>
DQS2_T	55	=MEM_A_DQS_P<2>
DQS2_C	53	=MEM_A_DQS_N<2>
DQS1_T	34	=MEM_A_DQS_P<1>
DQS1_C	32	=MEM_A_DQS_N<1>
DQS0_T	13	=MEM_A_DQS_P<0>
DQS0_C	11	=MEM_A_DQS_N<0>

Memory desense caps

=PPVDDQ_S3_MEM_A

C23A0 12PF 5% 25V NP0-C0G 0201
C23A1 12PF 5% 25V NP0-C0G 0201

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 3 OF 3

251	VSS	VDD	163
247	VSS	VDD	159
243	VSS	VDD	153
239	VSS	VDD	147
235	VSS	VDD	141
231	VSS	VDD	135
227	VSS	VDD	129
223	VSS	VDD	123
217	VSS	VDD	117
213	VSS	VDD	111
209	VSS	VDD	112
205	VSS	VDD	118
201	VSS	VDD	124
197	VSS	VDD	130
193	VSS	VDD	136
189	VSS	VDD	142
185	VSS	VDD	148
181	VSS	VDD	154
175	VSS	VDD	160
171	VSS		
167	VSS	VTT	258
107	VSS		
103	VSS	IO261	261
99	VSS	IO262	262
93	VSS		
89	VSS		
85	VSS		
81	VSS		
77	VSS	VSS	60
73	VSS	VSS	64
69	VSS	VSS	68
65	VSS	VSS	72
61	VSS	VSS	78
57	VSS	VSS	82
51	VSS	VSS	86
47	VSS	VSS	90
43	VSS	VSS	94
39	VSS	VSS	98
35	VSS	VSS	102
31	VSS	VSS	106
27	VSS	VSS	168
23	VSS	VSS	172
19	VSS	VSS	176
15	VSS	VSS	180
9	VSS	VSS	184
5	VSS	VSS	188
1	VSS	VSS	192
2	VSS	VSS	196
6	VSS	VSS	202
10	VSS	VSS	206
14	VSS	VSS	210
18	VSS	VSS	214
22	VSS	VSS	218
26	VSS	VSS	222
30	VSS	VSS	226
36	VSS	VSS	230
40	VSS	VSS	234
44	VSS	VSS	238
48	VSS	VSS	244
52	VSS	VSS	248
56	VSS	VSS	252

=PPVDDQ_S3_MEM_A

=PPDDRVTT_S0_MEM_A

BOM_COST_GROUP=DRAM

PAGE TITLE	DRAM: SO-DIMM Connector A
Apple Inc.	DRAWING NUMBER 051-01477
	SIZE D
	REVISION 3.26.0
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Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP3V3_S0_MEM_B_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM8_SCL
- =I2C_SODIMM8_SDA

BOM options provided by this page:
(NONE)

=PPDDRVTT_S0_MEM_B

C2550 1UF 10% 6.3V CERM 402
C2551 1UF 10% 6.3V CERM 402
C2552 1UF 10% 6.3V CERM 402
C2553 1UF 10% 6.3V CERM 402
C2554 10UF 20% 6.3V CERM-X6S 0402

=PPDDRVPP_S3_MEM_B

C2530 10UF 20% 6.3V CERM-X6S 0402
C2531 1UF 10% 10V CERM 402
BYPASS=I2500.257::2MM

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C2510 1UF 20% 6.3V X6S-CERM 0201
C2511 1UF 20% 6.3V X6S-CERM 0201
C2512 1UF 20% 6.3V X6S-CERM 0201
C2513 1UF 20% 6.3V X6S-CERM 0201
C2514 1UF 20% 6.3V X6S-CERM 0201
C2515 1UF 20% 6.3V X6S-CERM 0201
C2516 1UF 20% 6.3V X6S-CERM 0201
C2517 1UF 20% 6.3V X6S-CERM 0201

C2500 10UF 20% 6.3V CERM-X6S 0402
C2501 10UF 20% 6.3V CERM-X6S 0402
C2518 10UF 20% 6.3V CERM-X6S 0402
C2519 10UF 20% 6.3V CERM-X6S 0402
C2520 10UF 20% 6.3V CERM-X6S 0402
C2521 10UF 20% 6.3V CERM-X6S 0402
C2522 10UF 20% 6.3V CERM-X6S 0402
C2523 10UF 20% 6.3V CERM-X6S 0402

CRITICAL C2524 470UF-0.0060HM 20% 2V POLY CASE-D2-SM
NOSTUFF CRITICAL C2525 470UF-0.0060HM 20% 2V POLY CASE-D2-SM

PPVREF_S3_MEM_VREFCAB

C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 10% 10V CERM 402

R2541 10K 5% 1/16W MF-LF 402
=PP3V3_S0_MEM_B_SPD
MEM_DIMMB_SA<2>
MEM_DIMMB_SA<1>
MEM_DIMMB_SA<0>
R2540 10K 5% 1/16W MF-LF 402
R2542 10K 5% 1/16W MF-LF 402
C2540 2.2UF 20% 6.3V CERM 402-LF
C2541 0.1UF 20% 10V CERM 402

P/N: 998-05060

J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 1 OF 3

MEM_B_A<16>	152	RAS*/A16	
MEM_B_A<15>	156	CAS*/A15	
MEM_B_A<14>	151	WE*/A14	
MEM_B_A<13>	158	A13	
MEM_B_A<12>	119	A12	
MEM_B_A<11>	120	A11	
MEM_B_A<10>	146	A10/AP	
MEM_B_A<9>	121	A9	
MEM_B_A<8>	125	A8	
MEM_B_A<7>	122	A7	
MEM_B_A<6>	127	A6	
MEM_B_A<5>	126	A5	
MEM_B_A<4>	128	A4	
MEM_B_A<3>	131	A3	
MEM_B_A<2>	132	A2	
MEM_B_A<1>	133	A1	
MEM_B_A<0>	144	A0	
MEM_B_BA<1>	145	BA1	
MEM_B_BA<0>	150	BA0	
MEM_B_CLK_P<1>	138	CK1_T/NF	
MEM_B_CLK_N<1>	140	CK1_C/NF	
MEM_B_CLK_P<0>	137	CK0_T	
MEM_B_CLK_N<0>	139	CK0_C	
NC	165	C1/CS3*/NC	
NC	162	C0/CS2*/NC	
MEM_B_CS_L<1>	157	CS1*/NC	
MEM_B_CS_L<0>	149	CS0*	
MEM_B_CKE<1>	110	CKE1/NC	
MEM_B_CKE<0>	109	CKE0	
MEM_B_BG<1>	113	BG1	
MEM_B_BG<0>	115	BG0	
MEM_B_ODT<1>	161	ODT1/NC	
MEM_B_ODT<0>	155	ODT0	
MEM_B_PARITY	143	PARITY	
NC	104	CB7/NC	
NC	100	CB6/NC	
NC	87	CB5/NC	
NC	88	CB4/NC	
NC	105	CB3/NC	
NC	101	CB2/NC	
NC	91	CB1/NC	
NC	92	CB0/NC	
MEM_RESET_L	108	RESET*	
=PP3V3_S0_MEM_B_SPD	255	VDDSPD	
MEM_DIMMB_SA<2>	166	SA2	
MEM_DIMMB_SA<1>	260	SA1	
MEM_DIMMB_SA<0>	256	SA0	
=I2C_SODIMMB_SDA	254	SDA	
=I2C_SODIMMB_SCL	253	SCL	
PPVREF_S3_MEM_VREFCAB	164	VREFCA	
=PPDDRVPP_S3_MEM_B	257	VPP	
	259	VPP	
MEM_B_ACT_L	114	ACT*	
MEM_B_ALERT_L	116	ALERT*	

J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 2 OF 3

DM8*/BDI*/NC	96	=PPVDDQ_S3_MEM_B
DM7*/DBI7*	241	
DM6*/DBI6*	220	
DM5*/DBI5*	199	
DM4*/DBI4*	178	
DM3*/DBI3*	75	
DM2*/DBI2*	54	
DM1*/DBI*	33	
DM0*/DBI0*	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	=MEM_B_DQS_P<7>
DQS7_C	240	=MEM_B_DQS_N<7>
DQS6_T	221	=MEM_B_DQS_P<6>
DQS6_C	219	=MEM_B_DQS_N<6>
DQS5_T	200	=MEM_B_DQS_P<5>
DQS5_C	198	=MEM_B_DQS_N<5>
DQS4_T	179	=MEM_B_DQS_P<4>
DQS4_C	177	=MEM_B_DQS_N<4>
DQS3_T	76	=MEM_B_DQS_P<3>
DQS3_C	74	=MEM_B_DQS_N<3>
DQS2_T	55	=MEM_B_DQS_P<2>
DQS2_C	53	=MEM_B_DQS_N<2>
DQS1_T	34	=MEM_B_DQS_P<1>
DQS1_C	32	=MEM_B_DQS_N<1>
DQS0_T	13	=MEM_B_DQS_P<0>
DQS0_C	11	=MEM_B_DQS_N<0>

DQ63	246	=MEM_B_DQ<63>
DQ62	245	=MEM_B_DQ<62>
DQ61	233	=MEM_B_DQ<61>
DQ60	232	=MEM_B_DQ<60>
DQ59	250	=MEM_B_DQ<59>
DQ58	249	=MEM_B_DQ<58>
DQ57	236	=MEM_B_DQ<57>
DQ56	237	=MEM_B_DQ<56>
DQ55	225	=MEM_B_DQ<55>
DQ54	224	=MEM_B_DQ<54>
DQ53	212	=MEM_B_DQ<53>
DQ52	211	=MEM_B_DQ<52>
DQ51	229	=MEM_B_DQ<51>
DQ50	228	=MEM_B_DQ<50>
DQ49	215	=MEM_B_DQ<49>
DQ48	216	=MEM_B_DQ<48>
DQ47	204	=MEM_B_DQ<47>
DQ46	203	=MEM_B_DQ<46>
DQ45	190	=MEM_B_DQ<45>
DQ44	191	=MEM_B_DQ<44>
DQ43	208	=MEM_B_DQ<43>
DQ42	207	=MEM_B_DQ<42>
DQ41	194	=MEM_B_DQ<41>
DQ40	195	=MEM_B_DQ<40>
DQ39	182	=MEM_B_DQ<39>
DQ38	183	=MEM_B_DQ<38>
DQ37	169	=MEM_B_DQ<37>
DQ36	170	=MEM_B_DQ<36>
DQ35	186	=MEM_B_DQ<35>
DQ34	187	=MEM_B_DQ<34>
DQ33	173	=MEM_B_DQ<33>
DQ32	174	=MEM_B_DQ<32>
DQ31	80	=MEM_B_DQ<31>
DQ30	79	=MEM_B_DQ<30>
DQ29	67	=MEM_B_DQ<29>
DQ28	66	=MEM_B_DQ<28>
DQ27	84	=MEM_B_DQ<27>
DQ26	83	=MEM_B_DQ<26>
DQ25	71	=MEM_B_DQ<25>
DQ24	70	=MEM_B_DQ<24>
DQ23	59	=MEM_B_DQ<23>
DQ22	58	=MEM_B_DQ<22>
DQ21	45	=MEM_B_DQ<21>
DQ20	46	=MEM_B_DQ<20>
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J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 3 OF 3

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VSS	235	
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VDD	160	
VTT	258	=PPDDRVTT_S0_MEM_B
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IO262	262	
VSS	60	
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VSS	252	

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C25A0 12PF 5% 25V NP0-C0G 0201
C25A1 12PF 5% 25V NP0-C0G 0201

BOM_COST_GROUP=DRAM

SYNC_MASTER=L103 SYNC_DATE=01/29/2018

PAGE TITLE
DRAM: SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
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PAGE 25 OF 119
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THERE ARE NO PIN SWAPS

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SYNC_MASTER=ddressler SYNC_DATE=11/09/2015

PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

BRANCH

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R2891 3.3K
R2893 3.3K
R2892 3.3K
C2890 1UF
U2890
8MBIT-3.0V
W25Q80DVUXIE
USON
OMIT_TABLE
CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
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SNK1 AC Coupling
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10K PU ON CLOCKS PAGE
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TBT_X_PCIE_BIAS
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R2851 3.01K
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
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DP_X_SNK1_HPD
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=DP_X_SNK0_DDC_DATA
=DP_X_SNK1_DDC_CLK
=DP_X_SNK1_DDC_DATA
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R2830 100K
R2831 100K
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DP_X_SRC_AUX_N
DP_X_SRC_HPD
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=PP3V3_TBT_X_SX
R2834 2.2K
R2835 2.2K
R2836 2.2K
R2837 2.2K
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I2C_TBT_X_SCL
TBT_X_ROM_WP_L
=TBT_X_TMU_CLK_OUT
TBT_WAKE_L
TBT_X_CIO_PLUG_EVENT_L
TBT_X_HDMI_DDC_DATA
TBT_X_HDMI_DDC_CLK
=TBT_X_GPIO_8
I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L
TBT_X_RTD3_USB_PWR_EN
TBT_X_FORCE_PWR
=TBT_X_BATLOW_L
PM_SLP_S3_L
TBT_X_RTD3_CIO_PWR_EN
PU at PCH
not used
R2827 100K
TBT_X_TEST_EN
TBT_X_TEST_PWR_GOOD
R2825 100
USBC_X_RESET_L
R2829 100
TBT_X_XTAL25M_IN
TBT_X_XTAL25M_OUT
=UPC_X_SPI_MOSI
=UPC_X_SPI_MISO
=UPC_X_SPI_CS_L
=UPC_X_SPI_CLK
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JTAG_TBT_X_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_X_RBIAS
TBT_X_RSENSE
R2855 4.75K
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PORT B
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DP_XB_AUXCH_C_P
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C2813 0.1UF
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DP_XB_AUXCH_N
USB_AR_XA_P
USB_AR_XA_N
USB_AR_XB_P
USB_AR_XB_N
TBT_XA_LSTX
TBT_XA_LSRX
DP_XA_HPD
TBT_XB_LSTX
TBT_XB_LSRX
DP_XB_HPD
TBT_XA_USB2_RBIAS
TBT_XB_USB2_RBIAS
PLACE_NEAR=U2800.H19:2MM
R2854 499
PLACE_NEAR=U2800.F19:2MM
R2853 499
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R2862 100K
R2872 100K
R2860 1M
R2861 1M
R2870 1M
R2871 1M
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LAST_MODIFIED=Wed Sep 14 23:01:24 2016

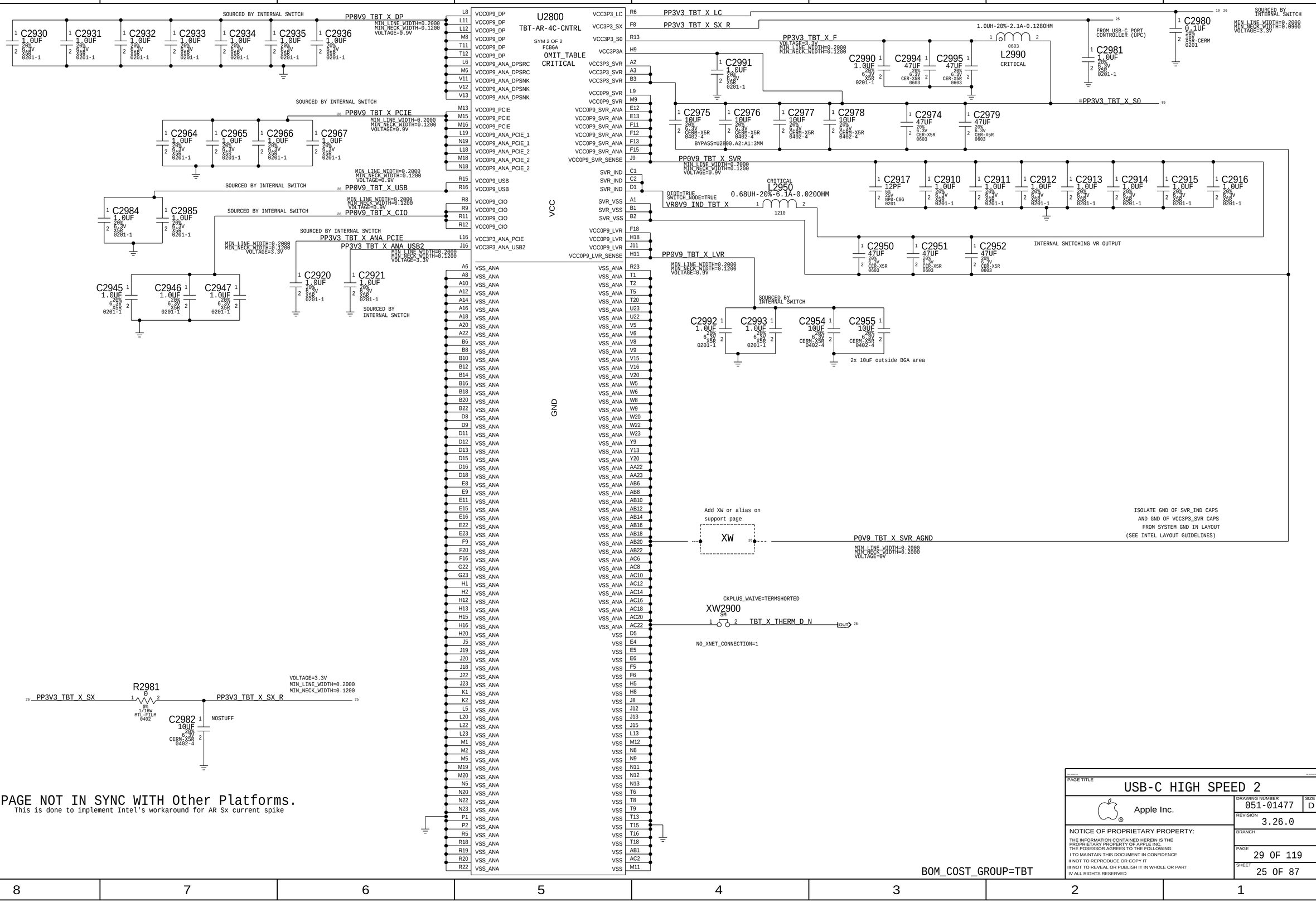
PAGE TITLE: USB-C HIGH SPEED 1

DRAWING NUMBER: 051-01477 SIZE: D

Apple Inc.

REVISION: 3.26.0

NOTICE OF PROPRIETARY PROPERTY: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C2931 1.0UF 20% 6.3V X5R 0201-1
C2932 1.0UF 20% 6.3V X5R 0201-1
C2933 1.0UF 20% 6.3V X5R 0201-1
C2934 1.0UF 20% 6.3V X5R 0201-1
C2935 1.0UF 20% 6.3V X5R 0201-1
C2936 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_PCIE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
C2964 1.0UF 20% 6.3V X5R 0201-1
C2965 1.0UF 20% 6.3V X5R 0201-1
C2966 1.0UF 20% 6.3V X5R 0201-1
C2967 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_USB
C2984 1.0UF 20% 6.3V X5R 0201-1
C2985 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_CIO
C2945 1.0UF 20% 6.3V X5R 0201-1
C2946 1.0UF 20% 6.3V X5R 0201-1
C2947 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
PP3V3_TBT_X_ANA_PCIE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
C2920 1.0UF 20% 6.3V X5R 0201-1
PP3V3_TBT_X_ANA_USB2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
C2921 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
U2800
TBT-AR-4C-CNTRL
SYM 2 OF 2
FCBGA
OMIT_TABLE
CRITICAL
VCC
GND
VCC0P9_DP
VCC0P9_ANA_DPSRC
VCC0P9_ANA_DPSNK
VCC0P9_PCIE
VCC0P9_ANA_PCIE_1
VCC0P9_ANA_PCIE_2
VCC0P9_USB
VCC0P9_CIO
VCC3P3_ANA_PCIE
VCC3P3_ANA_USB2
VSS_ANA
VCC3P3_LC
VCC3P3_SX
VCC3P3_S0
VCC3P3A
VCC3P3_SVR
VCC0P9_SVR
VCC0P9_SVR_ANA
VCC0P9_SVR_SENSE
SVR_IND
SVR_VSS
VCC0P9_LVR
VCC0P9_LVR_SENSE
VSS
PP3V3_TBT_X_LC
PP3V3_TBT_X_SX_R
PP3V3_TBT_X_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
C2991 1.0UF 20% 6.3V X5R 0201-1
C2990 1.0UF 20% 6.3V X5R 0201-1
C2994 47UF 20% 6.3V CER-X5R 0603
C2995 47UF 20% 6.3V CER-X5R 0603
1.0UH-20%-2.1A-0.128OHM
0603
L2990
CRITICAL
FROM USB-C PORT CONTROLLER (UPC)
C2981 1.0UF 20% 6.3V X5R 0201-1
C2980 0.1UF 10% 16V X5R-CERM 0201
SOURCED BY INTERNAL SWITCH
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0900
VOLTAGE=3.3V
=PP3V3_TBT_X_S0
C2975 10UF 20% 6.3V CERM-X5R 0402-4
C2976 10UF 20% 6.3V CERM-X5R 0402-4
C2977 10UF 20% 6.3V CERM-X5R 0402-4
C2978 10UF 20% 6.3V CERM-X5R 0402-4
BYPASS=U2800.A2:A1:3MM
C2974 47UF 20% 6.3V CER-X5R 0603
C2979 47UF 20% 6.3V CER-X5R 0603
PP0V9_TBT_X_SVR
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
C2917 12PF 5% 25V NP0-C0G 0201
C2910 1.0UF 20% 6.3V X5R 0201-1
C2911 1.0UF 20% 6.3V X5R 0201-1
C2912 1.0UF 20% 6.3V X5R 0201-1
C2913 1.0UF 20% 6.3V X5R 0201-1
C2914 1.0UF 20% 6.3V X5R 0201-1
C2915 1.0UF 20% 6.3V X5R 0201-1
C2916 1.0UF 20% 6.3V X5R 0201-1
DIDT=TRUE
SWITCH_NODE=TRUE
VR0V9_IND_TBT_X
CRITICAL
L2950
0.68UH-20%-6.1A-0.020OHM
1210
C2950 47UF 20% 6.3V CER-X5R 0603
C2951 47UF 20% 6.3V CER-X5R 0603
C2952 47UF 20% 6.3V CER-X5R 0603
INTERNAL SWITCHING VR OUTPUT
PP0V9_TBT_X_LVR
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
C2992 1.0UF 20% 6.3V X5R 0201-1
C2993 1.0UF 20% 6.3V X5R 0201-1
C2954 10UF 20% 6.3V CERM-X5R 0402-4
C2955 10UF 20% 6.3V CERM-X5R 0402-4
2x 10uF outside BGA area
Add XW or alias on support page
XW
P0V9_TBT_X_SVR_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V
ISOLATE GND OF SVR_IND CAPS
AND GND OF VCC3P3_SVR CAPS
FROM SYSTEM GND IN LAYOUT
(SEE INTEL LAYOUT GUIDELINES)
CKPLUS_WAIVE=TERMSHORTED
XW2900
SM
TBT_X_THERM_D_N
OUT
NO_XNET_CONNECTION=1
R2981
0
0%
1/16W
MTL-FILM
0402
PP3V3_TBT_X_SX
PP3V3_TBT_X_SX_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
C2982 10UF 20% 6.3V CERM-X5R 0402-4
NOSTUFF
PAGE NOT IN SYNC WITH Other Platforms.
This is done to implement Intel's workaround for AR Sx current spike
BOM_COST_GROUP=TBT
PAGE TITLE
USB-C HIGH SPEED 2
Apple Inc.
DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
BRANCH
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Ridge PUs

=TBT_X_BATLOW_L → MAKE_BASE=TRUE PM_BATLOW_L → R3075 100K 1/20W 5% MF 201 → PP3V3_TBT_X_SX

R3074 100K 1/20W 5% MF 201: TBT_X_HDMI_DDC_CLK → PP3V3_TBT_X_LC

USBC 5V EN PD

UPC_XA_5V_EN, UPC_XB_5V_EN → MAKE_BASE=TRUE UPC_X_5V_EN → R3032 100K 1/20W 5% MF 201

ACE Debug Support

R3089 NOSTUFF NONE NONE NONE 402: TP_UPC_XA_DBG_UART_TX → TP_UPC_XA_DBG_UART_RX

R3088 NOSTUFF NONE NONE NONE 402: TP_UPC_XB_DBG_UART_TX → TP_UPC_XB_DBG_UART_RX

Ridge PDs

=DP_X_SNK0_DDC_CLK	MAKE_BASE=TRUE DP_X_SNK0_DDC_CLK	R3067 100K 5% 1/20W MF 201
=DP_X_SNK0_DDC_DATA	MAKE_BASE=TRUE DP_X_SNK0_DDC_DATA	R3068 100K 5% 1/20W MF 201
=DP_X_SNK1_DDC_CLK	MAKE_BASE=TRUE DP_X_SNK1_DDC_CLK	R3069 100K 5% 1/20W MF 201
=DP_X_SNK1_DDC_DATA	MAKE_BASE=TRUE DP_X_SNK1_DDC_DATA	R3070 100K 5% 1/20W MF 201
=TBT_X_GPIO_8	MAKE_BASE=TRUE PD_TBT_X_GPIO_8	R3071 100K 5% 1/20W MF 201
=TBT_X_TMU_CLK_OUT	MAKE_BASE=TRUE PD_TBT_X_TMU_CLK_OUT	R3072 100K 5% 1/20W MF 201
DP_X_SRC_HPD		R3073 100K 1/20W MF 201 5%
TBT_X_HDMI_DDC_DATA		R3076 100K 5% 1/20W MF 201

SMC RESET Connection

UPC_XA_HPD_RX → R3033 100K 5% 1/20W MF 201 → R3024 MF 0201 NOSTUFF 0 5% 1/20W

UPC_XB_HPD_RX → R3034 MF 0201 NOSTUFF 0 5% 1/20W → SMC_RESET_L

R3025 100K 5% 1/20W MF 201

GND ALIASES

MAKE_BASE=TRUE

USBC_XB_RPD_G2, USBC_XB_RPD_G1, USBC_XA_RPD_G2, USBC_XA_RPD_G1, UPC_XB_SPI_CLK, UPC_XB_SPI_MOSI, UPC_XB_SPI_MISO, UPC_XB_SPI_CS_L, UPC_XA_RESET, UPC_XB_RESET, TBT_X_THERM_D_P, TBT_X_THERM_D_N

POWER ALIASES

=PP5V_USBC_XA, =PP5V_USBC_XB → =PP5V_S4_USBC

=PPHV_TBT_XA, =PPHV_TBT_XB → =PPHV_SW_TBT_X

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=3.3V

=PP3V3_TBT_X_SX, =PP3V3_UPC_XA_SX, =PP3V3_UPC_XB_SX → MAKE_BASE=TRUE PP3V3_TBT_X_SX

=PP3V3R1V8_UPC_XB, =PP3V3_UPC_XB_LDO → MAKE_BASE=TRUE PP3V3_UPC_XB_LDO (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=3.3V)

=PP3V3_TBT_X_FLASH, =PP3V3R1V8_UPC_XA, =PP3V3_UPC_XA_LDO → MAKE_BASE=TRUE PP3V3_UPC_XA_LDO (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=3.3V)

SIGNAL ALIASES

TBT_X_RTD3_CIO_PWR_EN → MAKE_BASE=TRUE TBT_X_CIO_PWR_EN; UPC_XB_GPIO2

TBT_X_RTD3_USB_PWR_EN → MAKE_BASE=TRUE TBT_X_USB_PWR_EN; UPC_XB_GPIO3

=UPC_WAKE_L → MAKE_BASE=TRUE TBT_WAKE_L

=UPC_X_SPI_CLK	MAKE_BASE=TRUE UPC_X_SPI_CLK
=UPC_X_SPI_CS_L	MAKE_BASE=TRUE UPC_X_SPI_CS_L
=UPC_X_SPI_MOSI	MAKE_BASE=TRUE UPC_X_SPI_MOSI
=UPC_X_SPI_MISO	MAKE_BASE=TRUE UPC_X_SPI_MISO

USBC_X_POC_RESET → MAKE_BASE=TRUE TBT_POC_RESET

I2C SERIES R'S

PLACE_NEAR=U5000:5mm

R3041 33 5% 1/20W MF 201: =I2C_UPC_XA_SDA2 → =I2C_UPC_XA_SDA2_R; =I2C_UPC_XB_SDA2 → =I2C_UPC_XB_SDA2_R; I2C_UPC_X_SDA2

PLACE_NEAR=U5000:5mm

R3042 33 5% 1/20W MF 201: =I2C_UPC_XA_SCL2 → =I2C_UPC_XA_SCL2_R; =I2C_UPC_XB_SCL2 → =I2C_UPC_XB_SCL2_R; I2C_UPC_X_SCL2

RIDGE 0.9V SVR XW

XW3000 SM

P0V9_TBT_X_SVR_AGND → NO_XNET_CONNECTION=1

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

I2C_TBT_X_SCL	=I2C_UPC_XA_SCL1
I2C_TBT_X_SDA	=I2C_UPC_XA_SDA1
I2C_TBT_XA_INT_L	=I2C_UPC_XA_INT1_L
I2C_TBT_XB_INT_L	

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

=I2C_UPC_XB_SCL1	
=I2C_UPC_XB_SDA1	
=I2C_UPC_XB_INT1_L	

Ridge PCIE Caps

PCIE_TBT_X_R2D_C_P<0>	GND_VOID=TRUE	C3040 0.22UF
PCIE_TBT_X_R2D_C_N<0>	GND_VOID=TRUE	C3041 0.22UF
PCIE_TBT_X_R2D_C_P<1>	GND_VOID=TRUE	C3042 0.22UF
PCIE_TBT_X_R2D_C_N<1>	GND_VOID=TRUE	C3043 0.22UF
PCIE_TBT_X_R2D_C_P<2>	GND_VOID=TRUE	C3044 0.22UF
PCIE_TBT_X_R2D_C_N<2>	GND_VOID=TRUE	C3045 0.22UF
PCIE_TBT_X_R2D_C_P<3>	GND_VOID=TRUE	C3046 0.22UF
PCIE_TBT_X_R2D_C_N<3>	GND_VOID=TRUE	C3047 0.22UF
PCIE_TBT_X_D2R_C_P<0>	GND_VOID=TRUE	C3050 0.22UF
PCIE_TBT_X_D2R_C_N<0>	GND_VOID=TRUE	C3051 0.22UF
PCIE_TBT_X_D2R_C_P<1>	GND_VOID=TRUE	C3052 0.22UF
PCIE_TBT_X_D2R_C_N<1>	GND_VOID=TRUE	C3053 0.22UF
PCIE_TBT_X_D2R_C_P<2>	GND_VOID=TRUE	C3054 0.22UF
PCIE_TBT_X_D2R_C_N<2>	GND_VOID=TRUE	C3055 0.22UF
PCIE_TBT_X_D2R_C_P<3>	GND_VOID=TRUE	C3056 0.22UF
PCIE_TBT_X_D2R_C_N<3>	GND_VOID=TRUE	C3057 0.22UF

All: 0201 X5R 6.3V 20%

RIDGE DEBUG CONN

Place on bottom

BOM OPTION Removed, No Stuff at PVT

J3099 505070-1220 M-ST-SM DEVELOPMENT

TBT_X_CIO_PLUG_EVENT_L	PM_PLT_RST_TBT_X_L	
DP_X_SNK0_HPD	USBC_X_RESET_L	
ARKANOID_P5	PP3V3_TBT_X_SX	
ARKANOID_P7	PP0V9_TBT_X_PCIE	
TBT_POC_RESET	PP0V9_TBT_X_USB	
PP3V3_TBT_X_LC	PP0V9_TBT_X_CIO	

516S00115

ACE DEBUG CONN

Place on bottom

BOM OPTION Removed, No Stuff at PVT

J3000 505070-1220 M-ST-SM DEVELOPMENT

I2C_TBT_XB_INT_L	I2C_TBT_XA_INT_L	
I2C_UPC_X_SCL2	I2C_TBT_X_SDA	
I2C_UPC_X_SDA2	I2C_TBT_X_SCL	
SMC_USBC_INT_L	I2C_UPC_XB_DBG_CTL_SDA	
TBT_X_SPI_CLK_DBG	I2C_UPC_XB_DBG_CTL_SCL	
UPC_XA_UART_TX	UPC_XA_UART_RX	

AR/ACE SPI BUS SERIES R'S

TBT_X_SPI_CLK	R3094 100	TBT_X_SPI_CLK_DBG
TBT_X_SPI_CS_L	R3095 15	UPC_XA_SPI_CLK
TBT_X_SPI_MOSI	R3096 15	UPC_XA_SPI_CS_L
TBT_X_SPI_MISO	R3097 15	UPC_XA_SPI_MOSI
	R3098 15	UPC_XA_SPI_MISO
	R3090 15	=UPC_X_SPI_CLK
	R3091 15	=UPC_X_SPI_CS_L
	R3092 15	=UPC_X_SPI_MOSI
	R3093 15	=UPC_X_SPI_MISO

All: 5% 1/20W MF 201

ROM — Ace — AR

USBC DEBUG CONN

=PP5V_S4_USBC → C3089 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

ACE XA DEBUG PORTS

SMC SWD

MAKE_BASE=TRUE	SMC_TCK	=	UPC_XA_DBG1
MAKE_BASE=TRUE	SMC_TMS	=	UPC_XA_DBG2
MAKE_BASE=TRUE	SMC_TX_L	=	UPC_XA_DBG3
MAKE_BASE=TRUE	SMC_RX_L	=	UPC_XA_DBG4

ACE XB DEBUG PORTS

R3062 100K: UPC_XB_DBG1

R3063 100K: UPC_XB_DBG2

SMC_DEBUGPRT_TX_L → R3080 0 MF 0201 NOSTUFF 5% 1/20W → UPC_XB_DBG3

R3015 100K MF 201 5% 1/20W

R3016 100K MF 201 5% 1/20W

SMC MOJO — SMC_DEBUGPRT_RX_L → R3081 0 MF 0201 NOSTUFF 5% 1/20W → UPC_XB_DBG4

Place Resistors close to USB-A Mojo Mux resistors.

ARKANOID_P5	R3082 0 5% 1/20W MF 0201	DP_X_SNK1_HPD
	R3083 NOSTUFF 0 5% 1/20W MF 0201	SMC_DEBUGPRT_RX_L
ARKANOID_P7	R3084 0 5% 1/20W MF 0201	DP_XA_HPD
	R3085 NOSTUFF 0 5% 1/20W MF 0201	SMC_DEBUGPRT_TX_L

TP_UPC_XA_SWD_DATA → TP3001

TP_UPC_XA_SWD_CLK → TP3002

TP_UPC_XB_SWD_DATA → TP3003

TP_UPC_XB_SWD_CLK → TP3004

=USBC_XB_RESET_L → MAKE_BASE=TRUE TP_USBC_XB_RESET_L → TP3014

(TP-P5)

=USBC_XA_RESET_L

R3031 10K 1/20W MF 201 5% → D3000 SM-201 RB521ZS-30 → MAKE_BASE=TRUE USBC_X_RESET_L → C3031 1.0UF 20% 6.3V X5R 0201-1

MAKE_BASE=TRUE USBC_X_RESET_L_R

25MHz xtal

TBT_X_XTAL25M_OUT → R3007 0 5% 1/20W MF 201 → TBT_X_XTAL25M_OUT_R

R3006 NOSTUFF 1M 5% 1/20W MF 201

Y3000 25MHZ-25PPM-20PF-500HM 2.00X1.60-SM (CRITICAL)

C3002 20PF 5% 25V C0G 0201 (PLACE_NEAR=Y3000.3:2MM, PLACE_NEAR=Y3000.3:2MM)

C3003 20PF 5% 25V C0G 0201 (PLACE_NEAR=Y3000.1:2MM)

TBT_X_XTAL25M_IN

to/from Ridge

BOM_COST_GROUP=USB-C

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Apple Inc.	DRAWING NUMBER 051-01477
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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

=PP3V3_G3H_UPC_XA — R3189 0 5% 1/16W MF-LP 402 — VOLTAGE=3.3V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200

PPVBUS_USBC_XA — C3101 1UF 10% 35V X5R 0402

=PP3V3R1V8_UPC_XA — C3198 1UF 10% 35V X6S-CERM 0402

PP3V3_G3H_UPC_XA_R — C3199 1UF 10% 35V X5R 0402

=PPHV_TBT_XA — C3100 10UF 20% 6.3V CERM-X5R 0402-1

=PP5V_USBC_XA

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

=PP3V3_UPC_XA_LDO
- R3109 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SCL
- R3108 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SDA
- R3105 1M 5% 1/20W MF 201 — UPC_XA_UART_RX

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

USE GPIOs for SMC RESET after boot.

GND_I2C_ADDR PRIMARY ONLY
- R3102 0 5% 1/20W MF 201
- CRITICAL R3103 15K 0.1% 1/20W TF-LF 0201 — NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

RIDGE USB2
- L3100 90-OHM-0.1A EXCX4CE
- USB_UPC_XA_P
- USB_UPC_XA_N
- PLACE_NEAR=U3100:5mm

=PP3V3_UPC_XA_AUX
- PU to PP3V3_S4 if convenient for layout.
- Otherwise PU to PP3V3_UPC_XA_LDO
- NO_XNET_CONNECTION=1
- R3110 100K 5% 1/20W MF 201
- R3111 100K 5% 1/20W MF 201
- NO_XNET_CONNECTION=1

U3100 CD3215A BGA

	USBC_X_POC_RESET	E11	MRESET — PRIMARY ONLY
OUT	=USBC_XA_RESET_L	F11	RESET* — PRIMARY ONLY
	TP_UPC_XA_DBG_UART_TX	B2	GPIO0
	TP_UPC_XA_DBG_UART_RX	C2	GPIO1
BI	TBT_X_RTD3_CIO_PWR_EN	D10	GPIO2
BI	TBT_X_RTD3_USB_PWR_EN	G11	GPIO3
OUT	DP_XA_HPD	C10	GPIO4
OUT	UPC_XA_HPD_RX	E10	GPIO5
OUT	UPC_XA_5V_EN	G10	GPIO6
OUT	=UPC_WAKE_L	D7	GPIO7
OUT	UPC_XA_FAULT_L	H6	GPIO8
	=PP3V3_UPC_XA_LDO	F10	BUSPOWERZ
	UPC_XA_I2C_ADDR	F1	I2C_ADDR
	UPC_XA_R_OSC	G2	R_OSC
	I2C_UPC_XA_DBG_CTL_SCL	E4	DEBUG_CTL1
	I2C_UPC_XA_DBG_CTL_SDA	D5	DEBUG_CTL2
BI	=I2C_UPC_XA_SDA1	D1	I2C_SDA1
BI	=I2C_UPC_XA_SCL1	D2	I2C_SCL1
OUT	=I2C_UPC_XA_INT1_L	C1	I2C_IRQ1*
BI	=I2C_UPC_XA_SDA2	A5	I2C_SDA2
BI	=I2C_UPC_XA_SCL2	B5	I2C_SCL2
OUT	=I2C_UPC_XA_INT2_L	B6	I2C_IRQ2*
OUT	UPC_XA_SPI_CLK	A3	SPI_CLK
OUT	UPC_XA_SPI_MOSI	B4	SPI_MOSI
IN	UPC_XA_SPI_MISO	A4	SPI_MISO
OUT	UPC_XA_SPI_CS_L	B3	SPI_SSZ
	TP_UPC_XA_SWD_DATA	F4	SWD_DATA
	TP_UPC_XA_SWD_CLK	G4	SWD_CLK
	UPC_XA_UART_RX	F2	UART_RX
OUT	UPC_XA_UART_TX	E2	UART_TX
IN	TBT_XA_LSTX	L4	LSX_R2P
OUT	TBT_XA_LSRX	K4	LSX_P2R
	USB_UPC_XA_F_P	L5	USB_RP_P
	USB_UPC_XA_F_N	K5	USB_RP_N
	DP_XA_AUXCH_P	J1	AUX_P
	DP_XA_AUXCH_N	J2	AUX_N
BI	UPC_XA_DBG1	L2	DEBUG1
BI	UPC_XA_DBG2	K2	DEBUG2
BI	UPC_XA_DBG3	L3	DEBUG3
BI	UPC_XA_DBG4	K3	DEBUG4

PP_5V0 A11, B11, C11, D11 — PP_HV A6, A7, A8, B7 — PP_HV H10 — VBUS H11, J10, J11, K11 — VIN_3V3 H1 — VDDIO B1 — LDO_3V3 G1 — VOUT_3V3 H2 — LDO_1V8A K1 — LDO_1V8D A2 — LDO_BMC E1

OMIT_TABLE
CRITICAL

=PP3V3_UPC_XA_LDO — C3105 1.0UF 20% 6.3V X5R 0201-1 — C3108 10UF 20% 6.3V CERM-X5R 0402-1

PP1V1_UPC_XA_LDO_BMC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.1V — C3104 2.2UF 20% 6.3V X5R-CERM 0201

=PP3V3_UPC_XA_SX — VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED

PP1V8_UPC_XA_LDOA — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V

PP1V8_UPC_XA_LDOD — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V — C3106 0.47UF 10% 6.3V CERM-X5R 0201

HV FET/SENSE

SS	H7	UPC_XA_SS
SENSEP	B10	
SENSEN	A10	
HV_GATE1	B9	NC_UPC_XA_HV_GATE1
HV_GATE2	A9	NC_UPC_XA_HV_GATE2

C3109 0.47UF 10% 6.3V CERM-X5R 0201

DIGITAL CORE I/O AND CONTROL

TYPE-C

C_CC1	L9	USBC_XA_CC1
C_CC2	L10	USBC_XA_CC2
RPD_G1	K9	USBC_XA_RPD_G1
RPD_G2	K10	USBC_XA_RPD_G2
C_USB_TP	K6	USBC_XA_USB_TOP_P
C_USB_TN	L6	USBC_XA_USB_TOP_N
C_USB_BP	K7	USBC_XA_USB_BOT_P
C_USB_BN	L7	USBC_XA_USB_BOT_N
C_SBU1	K8	USBC_XA_SBU1
C_SBU2	L8	USBC_XA_SBU2

MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200

C3114 220PF 10% 16V C-ER-X7R 0201 — C3113 220PF 10% 16V C-ER-X7R 0201

GROUND
- NC — L11 — NC or GND to dissipate heat

PORT MUX

GND: A1, D6, E5, E6, E7, F5, G5, H4, H5, G8, H8, L1, B8, D8, E8, F6, F7, F8, G6, G7

UPC_XA_RESET

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER: 051-01477 — SIZE: D
REVISION: 3.26.0
BRANCH:
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SECONDARY ACE USB-C PORT CONTROLLER (UPC)

29 PPVBUS_USBC_XB

C3201 1UF 10% 25V X5R 0402

MAX 100uF TOTAL ON RAIL

85 =PP3V3_G3H_UPC_XB — R3289 0 5% 1/16W MF-LF 402 — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V — PP3V3_G3H_UPC_XB_R

26 =PP3V3R1V8_UPC_XB

26 =PPHV_TBT_XB

26 =PP5V_USBC_XB

C3298 1UF 10% 25V X6S-CERM 0402

C3299 1UF 10% 35V X5R 0402

C3200 10UF 20% 6.3V CERM-X5R 0402-1

PP_5V0 A11 B11 C11 D11 — PP_HV A6 A7 A8 B7 — PP_CABLE H10 — VBUS H11 J10 J11 K11 — VIN_3V3 H1 — VDDIO B1 — LDO_3V3 G1 — VOUT_3V3 H2 — LDO_1V8A K1 — LDO_1V8D A2 — LDO_BMC E1

OMIT_TABLE
CRITICAL

U3200
CD3215A
BGA

=PP3V3_UPC_XB_LDO 26 28

=PP3V3_UPC_XB_SX 26

PP1V8_UPC_XB_LDOA — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V — VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED

PP1V8_UPC_XB_LDOD

PP1V1_UPC_XB_LDO_BMC — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.1V

C3205 1.0UF 20% 6.3V X6S 0201-1

C3208 10UF 20% 6.3V CERM-X5R 0402-1

C3204 2.2UF 20% 4V X5R-CERM 0201

C3206 0.47UF 10% 6.3V CERM-X5R 0201 — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V

PULL R3209 AND R3208 UP TO ACES LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

=PP3V3_UPC_XB_LDO 26 28

R3209 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SCL 26 28

R3208 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SDA 26 28

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

R3205 1M 5% 1/20W MF 201 — UPC_XA_UART_TX 26 27 28

27 26 IN	USBC_X_POC_RESET	E11	MRESET
26 OUT	=USBC_XB_RESET_L	F11	RESET*
26	TP_UPC_XB_DBG_UART_TX	B2	GPIO0
26	TP_UPC_XB_DBG_UART_RX	C2	GPIO1
26	UPC_XB_GPIO2	D10	GPIO2
26	UPC_XB_GPIO3	G11	GPIO3
24 OUT	DP_XB_HPD	C10	GPIO4
26 OUT	UPC_XB_HPD_RX	E10	GPIO5
26 OUT	UPC_XB_5V_EN	G10	GPIO6
27 26 OUT	=UPC_WAKE_L	D7	GPIO7
30 OUT	UPC_XB_FAULT_L	H6	GPIO8
28 26	=PP3V3_UPC_XB_LDO	F10	BUSPOWERZ
	NC_UPC_XB_I2C_ADDR	F1	I2C_ADDR
	UPC_XB_R_OSC	G2	R_OSC
28 26	I2C_UPC_XB_DBG_CTL_SCL	E4	DEBUG_CTL1
28 26	I2C_UPC_XB_DBG_CTL_SDA	D5	DEBUG_CTL2
26 BI	=I2C_UPC_XB_SDA1	D1	I2C_SDA1
26 BI	=I2C_UPC_XB_SCL1	D2	I2C_SCL1
24 OUT	=I2C_UPC_XB_INT1_L	C1	I2C_IRQ1*
26 BI	=I2C_UPC_XB_SDA2	A5	I2C_SDA2
26 BI	=I2C_UPC_XB_SCL2	B5	I2C_SCL2
46 OUT	=I2C_UPC_XB_INT2_L	B6	I2C_IRQ2*
25 OUT	UPC_XB_SPI_CLK	A3	SPI_CLK
25 OUT	UPC_XB_SPI_MOSI	B4	SPI_MOSI
25 IN	UPC_XB_SPI_MISO	A4	SPI_MISO
25 OUT	UPC_XB_SPI_CS_L	B3	SPI_SSZ
26	TP_UPC_XB_SWD_DATA	F4	SWD_DATA
26	TP_UPC_XB_SWD_CLK	G4	SWD_CLK
28 27 26	UPC_XA_UART_TX	F2	UART_RX
27 26 OUT	UPC_XA_UART_RX	E2	UART_TX
24 IN	TBT_XB_LSTX	L4	LSX_R2P
24 OUT	TBT_XB_LSRX	K4	LSX_P2R
	USB_UPC_XB_F_P	L5	USB_RP_P
	USB_UPC_XB_F_N	K5	USB_RP_N
	DP_XB_AUXCH_P	J1	AUX_P
	DP_XB_AUXCH_N	J2	AUX_N
26 BI	UPC_XB_DBG1	L2	DEBUG1
26 BI	UPC_XB_DBG2	K2	DEBUG2
26 BI	UPC_XB_DBG3	L3	DEBUG3
26 BI	UPC_XB_DBG4	K3	DEBUG4

CRITICAL
R3203 15K 0.1% 1/20W TF-LF 0201 — NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

L3200 90-OHM-0.1A EXCX4CE SYM_VER_1

30 BI USB_UPC_XB_P — PLACE_NEAR=U3200.L5:5mm

30 BI USB_UPC_XB_N — PLACE_NEAR=U3200.K5:5mm

RIDGE/PCH USB2

85 =PP3V3_UPC_XB_AUX

PU to PP3V3_S4 if convenient for layout
OTHERWISE PU TO PP3V3_UPC_XB_LDO

R3210 100K 5% 1/20W MF 201 — NO_XNET_CONNECTION=1

24 BI
24 BI

R3211 100K 5% 1/20W MF 201 — NO_XNET_CONNECTION=1

HV FET/SENSE

DIGITAL CORE I/O AND CONTROL

TYPE-C

PORT MUX

SS	H7	UPC_XB_SS	
SENSEP	B10		
SENSEN	A10		
HV_GATE1	B9	NC_UPC_XB_HV_GATE1	
HV_GATE2	A9	NC_UPC_XB_HV_GATE2	
C_CC1	L9	USBC_XB_CC1	BI 29
C_CC2	L10	USBC_XB_CC2	BI 29
RPD_G1	K9	USBC_XB_RPD_G1	BI 26
RPD_G2	K10	USBC_XB_RPD_G2	BI 26
C_USB_TP	K6	USBC_XB_USB_TOP_P	BI 29
C_USB_TN	L6	USBC_XB_USB_TOP_N	BI 29
C_USB_BP	K7	USBC_XB_USB_BOT_P	BI 29
C_USB_BN	L7	USBC_XB_USB_BOT_N	BI 29
C_SBU1	K8	USBC_XB_SBU1	BI 29
C_SBU2	L8	USBC_XB_SBU2	BI 29
NC	L11	GROUND	

NC or GND to dissipate heat

C3209 0.47UF 10% 6.3V CERM-X5R 0201

C3214 220PF 10% 16V CER-X7R 0201

C3213 220PF 10% 16V CER-X7R 0201 — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200

GND — A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7

UPC_XB_RESET 26

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0201	8	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	C3374-C3377,C3394-C3397	CRITICAL	

Second IO from right (Between USB-C and USBA Ports) is used for Mojo.

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR

Apple Inc.

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REVISION 3.26.0
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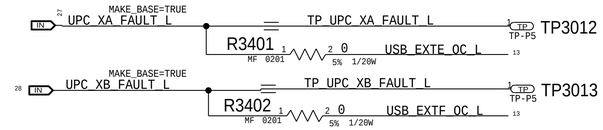
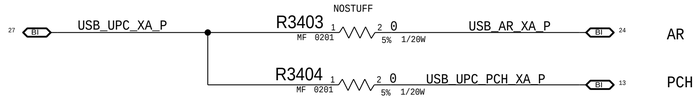
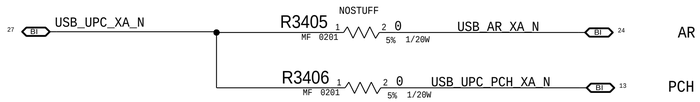
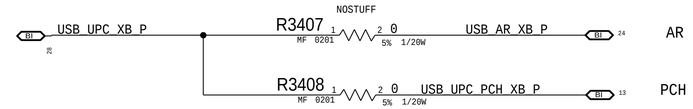


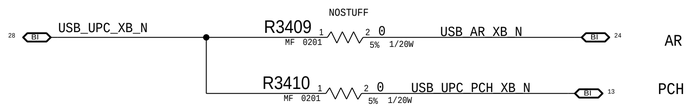


ACE A





ACE B



BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C Support 2

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

BRANCH

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22966
AP SLEW RATE	1185 us
BT SLEW RATE	1185 us
Equation	0.32*Ct + 13.7

Wireless desense caps

PP3V3_S4_AP_FLT (31) — C35A0 12PF 5% 25V NP0-C0G 0201

PP3V3_G3H_BT_FLT (31) — C35A1 12PF 5% 25V NP0-C0G 0201

U3500 TPS22966

CRITICAL
U3500
TPS22966
DPU-THICKSTNCL

1	VIN1	VOUT1	13
3	ON1		
12	CT1		
4	VBIAS		
6	VIN2	VOUT2	8
5	ON2		
10	CT2		
11	GND		
15	THRM PAD		

- 1 =PP3V3_G3H_BT (85, 31)
- 3 SMC_BT_PWR_EN (IN, 44)
- 12 BT_PWR_RAMP
- 4 =PP3V3_G3H_BT (85, 31)
- 6 =PP3V3_S4_AP (85, 44, 31)
- 5 AP_PWR_EN (IN, 44, 31)
- 10 AP_PWR_RAMP

C3541 0.001UF 10% 50V X7R-CERM 0402 (1–2)

C3542 0.1UF 10% 16V X7R-CERM 0402 (1–2)

C3543 0.001UF 10% 50V X7R-CERM 0402 (1–2)

PP3V3_S4_AP_FET

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V

CRITICAL
L3502
FERR-220-OHM-2.5A
0603 (1–2)

PP3V3_S4_AP_FLT (31)

C3502 0.1UF 10% 16V X7R-CERM 0402 (1–2)

C3503 0.1UF 10% 16V X7R-CERM 0402 (1–2)

C3504 10UF 20% 6.3V X5R 603 (1–2)

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V

PP3V3_G3H_BT_FET

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000

CRITICAL
L3501
FERR-220-OHM-2.5A
0603 (1–2)

PP3V3_G3H_BT_FLT (31)

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000

C3507 0.1UF 10% 16V X7R-CERM 0402 (1–2)

C3508 10UF 20% 6.3V X5R 603 (1–2)

J3500 SSD-K99

514S0335
CRITICAL
J3500
SSD-K99
F-RT-SM1

1			
2	PCH_BT_ROM_BOOT_L_R (31)		
3			
4	PCIE_AP_R2D_N		
5	PCIE_AP_R2D_P		
6			
7	PCIE_CLK100M_AP_N (IN, 11)		
8	PCIE_CLK100M_AP_P (IN, 11)		
9			
10	PCIE_AP_D2R_N (OUT, 13)		
11	PCIE_AP_D2R_P (OUT, 13)		
12			
13	AP_WAKE_L (31)		
14	AP_RESET_CONN_L (31)		
15	AP_CLKREQ_Q_L (31)		
16	USB_BT_MUX_N (31)		
17	USB_BT_MUX_P (31)		
18			
19			
20			
21			

PCIE_AP_R2D_C_N (IN, 13) — C3505 0.1UF 0201 CERM-X5R 6.3V 10% — PCIE_AP_R2D_N
PLACE_NEAR=J3500.4:7mm

PCIE_AP_R2D_C_P (IN, 13) — C3506 0.1UF 0201 CERM-X5R 6.3V 10% — PCIE_AP_R2D_P
PLACE_NEAR=J3500.5:7mm

PCH_BT_ROM_BOOT_L

=PP3V3_G3H_BT (85, 31)

R3502 10K 5% 1/20W MF 201 (1–2)

R3503 10K 5% 1/20W MF 201 NOSTUFF (1–2)

R3504 0 5% 1/10W MF-LF 603 (1–2) — PCH_BT_ROM_BOOT_L → PCH_BT_ROM_BOOT_L_R (31)

CRITICAL
Q3502
SSM3K15AMFVAP
SOD
(D=3, G=1, S=2)

PCH_BT_ROM_BOOT (IN, 14) → G

R3505 100K 5% 1/20W MF 201 (1–2)

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT (31)

R3530 100K 1% 1/10W MF-LF 402 (1–2)

R3531 232K 1% 1/10W MF-LF 402 (1–2)

=PP3V3_S4_AP (85, 44, 31)

CRITICAL
U3530
SLG4AP041V
TDFN

C3530 0.1UF 10% 16V CERM-X5R 0201 (1–2)

P3V3AP_VMON → SENSE (2)

VREF

DLY

AP_RESET_CONN_L (31) → R3533 0 5% 1/20W MF 201 (1–2) → AP_RESET_CONN_R_L → RESET* (4)

MR* (3) → AP_RESET_L (IN, 19)

EN (6) ← AP_PWR_EN (IN, 31, 44)

AP_CLKREQ_Q_L (31) → IN (7)

OUT (8, OD) → AP_CLKREQ_L (OUT, 11)

THRM PAD, GND

R3532 100K 1% 1/10W MF-LF 402 (1–2)

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L (OUT, 44, 43)

CRITICAL
Q3501
SSM3K15AMFVAP
SOD
(D=3, G=1, S=2)

R3501 15K 5% 1/20W MF 201 (1–2)

=PP3V3_G3H_BT (85, 31)

C3500 0.1UF 10% 10V X5R-CERM 0201 (1–2)

USB_BT_WAKEN

CRITICAL
U3501
PI3USB102EZLE
TQFN

NC		Y+	1 USB_BT_MUX_P (31)
5	M+	Y-	2 USB_BT_MUX_N (31)
4	M-		
7	D+		USB_BT_P (BI, 13)
6	D-		USB_BT_N (BI, 13)
8	OE*	SEL	10 PM_SLP_S5_L (IN, 12, 43, 71)
	GND		

PCIE_WAKE_L

PP3V3_S4_AP_FLT (31)

CRITICAL
Q3570
SOD
(D=3, G=1, S=2)

R3570 10K 5% 1/10W MF-LF 402 (1–2)

PCIE_WAKE_L (OUT, 35, 19, 12) → AP_WAKE_L (31)

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIRELESS: Airport/Bluetooth

Apple Inc.

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3V3 S0 SSD

85 72 71 70 =PP3V3_S5_PWRCTL

C3750 0.1UF 10% 16V X7R-CERM 0402 (SSD:Y)

U3750 SLG5AP1445V TDFN8 CRITICAL

VDD, CAP, ON, GND

P3V3_S0_SSD_FET_RAMP

14 13 12 IN SSD_PWR_EN

VIH = 0.85V MIN
VIL = 0.30V MAX

D 3 =PP3V3_S5_FET_P3V3_S0 70 85

S 5 PP3V3_S0_SSD_FET 85

Polaris SSD only needs to be powered in S0

C3751 0.0047UF 10% 25V CERM 0402 (SSD:Y)

4nF corresponds to
2.2V / ms ramp rate

GS3 SSD

155S00114
L3700
CRITICAL
PLACE_NEAR=J3700.1:10MM
FERR-10-OHM-8A
0603

85 =PPVSSD_S0_CONN

PP3V3_S0_SSD_FLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V

C3701 0.1UF 20% 10V CERM 402 (SSD:Y)

C3700 0.1UF 20% 10V CERM 402 (SSD:Y)

J3700
SSD:Y
SILK_PART=SSD
CRITICAL
SSD-J90
F-RT-SM

85 44 =PP3V3_S5_SMC

R3713 100K 5% 1/16W MF-LF 402

R3712 100K 5% 1/16W MF-LF 402

IN 44
OUT 44

Polaris SSD does not support LPSR

13 12 IN SSD_SR_EN_L
PCH GPD1

R3719 0 5% 1/16W MF-LF 402 NOSTUFF

SSD_SR_EN_R_L

19 IN PCH_SSD_RESET_L
PCH GPP_F7

R3718 0 5% 1/16W MF-LF 402 (SSD:Y)

SSD_RESET_R_L

Polaris SSD has PU on BFH

14 IN SSD_BFH_L
PCH GPP_G0

R3720 0 5% 1/16W MF-LF 402 (SSD:Y)

SSD_BFH_R_L

For PCH GPIO leakage issue

R3722 249K 1% 1/20W MF 201 (SSD:Y)

SMC_OOB2_R2D_L
SMC_OOB2_D2R_L

Pin 50: SSD_V_SEL (S3X)
Pin 49: EFI_L (S3X)
Pin 48: STORAGE_LATCH (S3X)

NC
NC
NC

SSD_PWR_EN_R

R3721 0 5% 1/16W MF-LF 402 NOSTUFF

Polaris SSD does not currently use pin 47

SSD_PWR_EN IN 13 14 32

PCIE TX3

86 IN PCIE_SSD_R2D_C_N<3>
IN PCIE_SSD_R2D_C_P<3>

C3717 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.11:5MM

C3716 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.12:5MM

PCIE_SSD_R2D_N<3>
PCIE_SSD_R2D_P<3>
PCIE_SSD_R2D_N<2>
PCIE_SSD_R2D_P<2>
PCIE_SSD_R2D_N<1>
PCIE_SSD_R2D_P<1>
PCIE_SSD_R2D_N<0>
PCIE_SSD_R2D_P<0>
(GND_VOID=TRUE)

PCIE_SSD_D2R_N<3> OUT 86
PCIE_SSD_D2R_P<3> OUT 86
PCIE_SSD_D2R_N<2> OUT 86
PCIE_SSD_D2R_P<2> OUT 86
PCIE_SSD_D2R_N<1> OUT 86
PCIE_SSD_D2R_P<1> OUT 86
PCIE_SSD_D2R_N<0> OUT 86
PCIE_SSD_D2R_P<0> OUT 86
(GND_VOID=TRUE)

PCIE RX3
PCIE RX2
PCIE RX1
PCIE RX0

PCIE TX2
POLARITY SWAPPED

86 IN PCIE_SSD_R2D_C_P<2>
86 IN PCIE_SSD_R2D_C_N<2>

C3715 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.14:5MM

C3714 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.15:5MM

PCIE TX1

86 IN PCIE_SSD_R2D_C_N<1>
86 IN PCIE_SSD_R2D_C_P<1>

C3711 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.19:5MM

C3710 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.19:5MM

PCIE TX0

86 IN PCIE_SSD_R2D_C_N<0>
86 IN PCIE_SSD_R2D_C_P<0>

C3713 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.21:5MM

C3712 0.22UF 20% 6.3V X5R 0201 (SSD:Y) GND_VOID=TRUE PLACE_NEAR=J3700.22:5MM

11 OUT SSD_CLKREQ_L

PCIE_CLK100M_SSD_N IN 11
PCIE_CLK100M_SSD_P IN 11

POR:514S0457 (tall)

BOM_COST_GROUP=SSD

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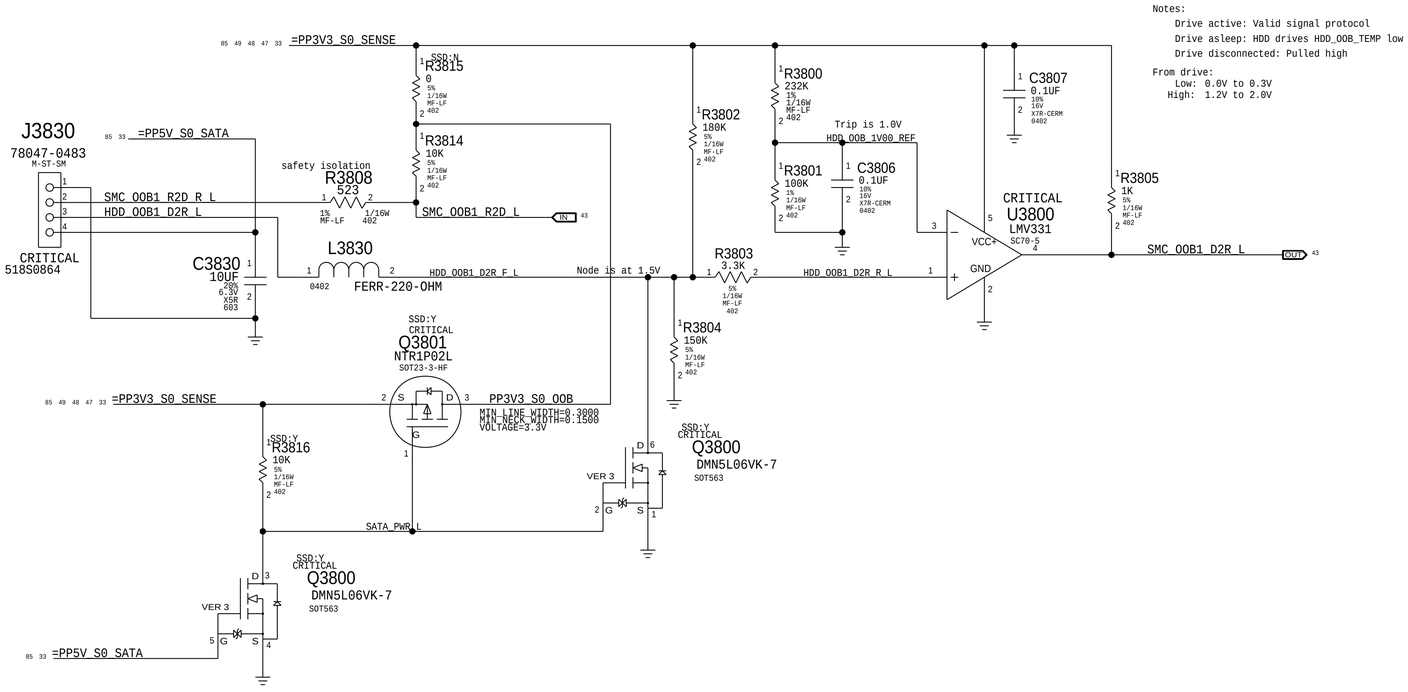
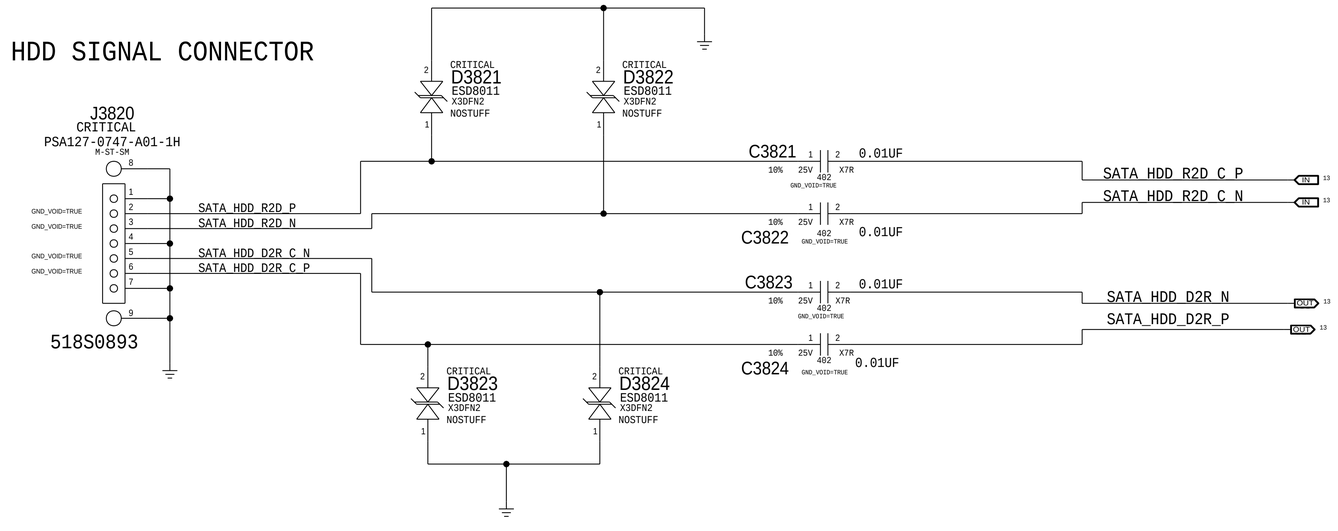
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing



HDD SIGNAL CONNECTOR



BOM_COST_GROUP=HDD

SYNC_MASTER=andres	SYNC_DATE=08/05/2016
PAGE TITLE	HDD Connector
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

85 35 34 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
34 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 35

=ENET_SR_VFB 35

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 35

396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201

ENET_XTALVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R3910 4.7K 5% 1/10W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/10W MF-LF 402
R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM 402
C3916 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

85 =PP3V3_S0_ENET

R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

13 OUT PCIE_ENET_D2R_N
13 OUT PCIE_ENET_D2R_P
13 IN PCIE_ENET_R2D_C_P
13 IN PCIE_ENET_R2D_C_N
35 OUT =ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

42	AVDDH		
48	BIASVDDH		
37	XTALVDDH		
17	VDDO		
7	SR_VDD		
20	SR_VDDP		
56	SR_LX		
62	SR_VFB		
14	AVDDL		
39	PCIE_PLLVDDL		
45	GPHY_PLLVDDL		
51	VDDC		
29	VMAIN_PRSNT	(IPD-ENET)	ENETCONN_MDI_P<0> BI 35
32	PCIE_TXD_N		ENETCONN_MDI_N<0> BI 35
36	PCIE_TXD_P		ENETCONN_MDI_P<1> BI 35
35	PCIE_RXD_P		ENETCONN_MDI_N<1> BI 35
61	PCIE_RXD_N		ENETCONN_MDI_P<2> BI 35
	PCIE_REFCLK_P		ENETCONN_MDI_N<2> BI 35
	PCIE_REFCLK_N		ENETCONN_MDI_P<3> BI 35
	PERST*	(IPD)	ENETCONN_MDI_N<3> BI 35
	CLKREQ*	(OD)	
	WAKE*	(OD)	
	LOW_PWR	(IPD)	
	SMB_CLK		
	SMB_DATA	(IPD-ENETM)	
	SCLK_SPD1000LED*		
	SI/EEDATA		
	SO_LINKLED*		
	CS*/EECLK		
	SPD100LED*/SERIAL_DO	(OD)	
	TRAFFICLED*/SERIAL_DI	(OD)	
	XTALI		
	XTALO		
	RDAC		
69	THRM_PAD		

TRD0_P 40 ENETCONN_MDI_P<0> BI 35
TRD0_N 41 ENETCONN_MDI_N<0> BI 35
TRD1_P 44 ENETCONN_MDI_P<1> BI 35
TRD1_N 43 ENETCONN_MDI_N<1> BI 35
TRD2_P 46 ENETCONN_MDI_P<2> BI 35
TRD2_N 47 ENETCONN_MDI_N<2> BI 35
TRD3_P 50 ENETCONN_MDI_P<3> BI 35
TRD3_N 49 ENETCONN_MDI_N<3> BI 35

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3R1V8_CR_VDDIO 34
C3980 4.7UF 20% 6.3V X5R-CERM1 402
C3981 0.1UF 10% 16V X5R-CERM 0201
C3982 0.1UF 10% 16V X5R-CERM 0201

(IPD) GPIO_0/CR_ACT_LED* 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 ENET_MEDIA_SENSE OUT 14

(IPx-ENET) SD_DETECT 0 1 ENET_SD_DETECT_L IN 36

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

(IPU-ENET)	CR_CMD	26	ENET_SD_CMD	R3961	33	5%	1/20W	MF	201	SDCONN_CMD IN 36
	CR_CLK	21	ENET_SD_CLK	R3979	33	5%	1/20W	MF	201	SDCONN_CLK OUT 36
(IPU-ENET)	CR_DATA0	25	ENET_CR_DATA<0>	R3971	33	5%	1/20W	MF	201	SDCONN_DATA<0> BI 36
	CR_DATA1	24	ENET_CR_DATA<1>	R3972	33	5%	1/20W	MF	201	SDCONN_DATA<1> BI 36
	CR_DATA2	23	ENET_CR_DATA<2>	R3973	33	5%	1/20W	MF	201	SDCONN_DATA<2> BI 36
	CR_DATA3	22	ENET_CR_DATA<3>	R3974	33	5%	1/20W	MF	201	SDCONN_DATA<3> BI 36
	CR_DATA4	52	ENET_CR_DATA<4>	R3975	33	5%	1/20W	MF	201	SDCONN_DATA<4> BI 36
	CR_DATA5	53	ENET_CR_DATA<5>	R3976	33	5%	1/20W	MF	201	SDCONN_DATA<5> BI 36
	CR_DATA6	54	ENET_CR_DATA<6>	R3977	33	5%	1/20W	MF	201	SDCONN_DATA<6> BI 36
	CR_DATA7	55	ENET_CR_DATA<7>	R3978	33	5%	1/20W	MF	201	SDCONN_DATA<7> BI 36

NO MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

(IPU-ENET) MS_INS* 59 NC
(IPU-ENET) CR_LED*/CR_BUS_PWR 60 ENET_CR_PWREN OUT 36
(IPU-ENET) CR_WP* 57 SDCONN_WP IN 36
(NO IPU OR IPD-ENET) SR_DISABLE 68 ENET_SR_DISABLE R3981 1K 5% 1/16W MF-LF 402
(See note)

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

85 35 34 =PP3V3_ENET_PHY

C3990 0.1UF 10% 16V X5R-CERM 0201

U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE

34	ENET_SCLK	SCK	2
34	ENET_CS_L	CS*	4
		WP*	5
		RESET*	3
		SI	1
		SO	8
		VCC	6
		GND	7

ENET_MOSI 34
ENET_MISO 34

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

C3940 15PF 5% 50V CERM 0402
C3941 15PF 5% 50V CERM 0402
CRITICAL Y3940 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM
ENET_XTAL_OUT_R
R3943 0 5% 1/16W MF-LF 402
ENET_XTAL_OUT 34
NOSTUFF R3944 1M 5% 1/16W MF-LF 402
ENET_XTAL_IN 34

NOTE: 30 PPM crystal required

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=hurtadot SYNC_DATE=11/17/2015
PAGE TITLE
Ethernet PHY (CAESAR IV)
Apple Inc.
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CAESAR IV 1.2V INT.VR CMPTS

=PP3V3_ENET_PHY

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402

C4011 0.1UF 10% 16V X7R-CERM 0402

CRITICAL

L4010 4.7UH-0.8A PCAA031B-SM

ENET_SR_LX

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

C4012 10UF 20% 6.3V X5R 603

C4013 0.1UF 10% 16V X7R-CERM 0402

PP1V2_ENET_INTREG

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

Feedback loop

PP1V2_ENET_INTREG
MAKE_BASE=TRUE

=PP1V2_ENET_PHY

=ENET_SR_VFB

ENET Enable Generation

ENET is enabled when in S0 or when (S4 & WOL_EN) is present

3.3V ENET FET

CRITICAL

Q4020 NTR4101P SOT-23-HF

=PP3V3_S4_FET_ENET

R4020 10K 5% 1/16W MF-LF 402

C4020 0.033UF 10% 16V X5R 402

PP3V3_ENET_FET

PM_EN_ENET_L

R4021 100K 5% 1/16W MF-LF 402

P3V3ENET_SS

C4021 0.01UF 10% 25V X7R 402

Q4021 SSM6N15AFEAP SOT563 CRITICAL

Q4021 SSM6N15AFEAP SOT563 CRITICAL

WOL_EN

PM_SLP_S3_L

CAESAR IV ACTIVITY LED

=PP3V3_ENET_PHY

DEVELOPMENT R4050 330 5% 1/16W MF-LF 402

ENET_ACT

DEVELOPMENT LED4050 GRN-6MCD-0.03A 0805

ENET_TRAFFICLED_L

CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY

R4070 10K 5% 1/16W MF-LF 402

PCIE_WAKE_L

ENET_WAKE_L
MAKE_BASE=TRUE

=ENET_WAKE_L

Q4070 SSM3K15AMFVAP SOD

157S00005

T4000 LC607-AP-AFT453220M-171-T001 SM-COMBO VER 1

ENETCONN_MDI_P<2>

ENETCONN_MDI_N<2>

ENETCONN_MCT2

ENETCONN_MDI_X_P<2>

ENETCONN_MDI_X_N<2>

ENETCONN_MDI_T_P<2>

ENETCONN_MDI_T_N<2>

L4000 HCMC0805-4SM 370-OHM 155S00056

T4005 LC607-AP-AFT453220M-171-T001 SM-COMBO VER 1

ENETCONN_MDI_P<0>

ENETCONN_MDI_N<0>

ENETCONN_MCT0

ENETCONN_MDI_X_P<0>

ENETCONN_MDI_X_N<0>

ENETCONN_MDI_T_P<0>

ENETCONN_MDI_T_N<0>

L4005 HCMC0805-4SM 370-OHM

T4020 LC607-AP-AFT453220M-171-T001 SM-COMBO VER 1

ENETCONN_MDI_N<1>

ENETCONN_MDI_P<1>

ENETCONN_MCT1

ENETCONN_MDI_X_N<1>

ENETCONN_MDI_X_P<1>

ENETCONN_MDI_T_N<1>

ENETCONN_MDI_T_P<1>

L4020 HCMC0805-4SM 370-OHM

T4025 LC607-AP-AFT453220M-171-T001 SM-COMBO VER 1

ENETCONN_MDI_N<3>

ENETCONN_MDI_P<3>

ENETCONN_MCT3

ENETCONN_MDI_X_N<3>

ENETCONN_MDI_X_P<3>

ENETCONN_MDI_T_N<3>

ENETCONN_MDI_T_P<3>

L4025 HCMC0805-4SM 370-OHM

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402

C4002 0.1UF 20% 10V CERM 402

C4003 0.1UF 20% 10V CERM 402

C4004 0.1UF 20% 10V CERM 402

514-0822
CRITICAL
J4000 K70-K72 F-ANG-TH

ENET_MDI

ENETCONN_MDI_T_N<3> — ENET_MDI_TRAN3-
ENETCONN_MDI_T_P<3> — ENET_MDI_TRAN3+
ENETCONN_MDI_T_N<1> — ENET_MDI_TRAN1-
ENETCONN_MDI_T_N<2> — ENET_MDI_TRAN2-
ENETCONN_MDI_T_P<2> — ENET_MDI_TRAN2+
ENETCONN_MDI_T_P<1> — ENET_MDI_TRAN1+
ENETCONN_MDI_T_N<0> — ENET_MDI_TRAN0-
ENETCONN_MDI_T_P<0> — ENET_MDI_TRAN0+

SHIELD PINS

ENETCONN_MCT2
ENETCONN_MCT0
ENETCONN_MCT1
ENETCONN_MCT3

R4000 75 5% 1/20W MF 201

R4001 75 5% 1/20W MF 201

R4002 75 5% 1/20W MF 201

R4003 75 5% 1/20W MF 201

ENETCONN_MCT_RS
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000

C4000 1000PF 10% 3KV X7R 1808

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=yeungr SYNC_DATE=03/30/2016

PAGE TITLE: Ethernet Support & Connector

Apple Inc.

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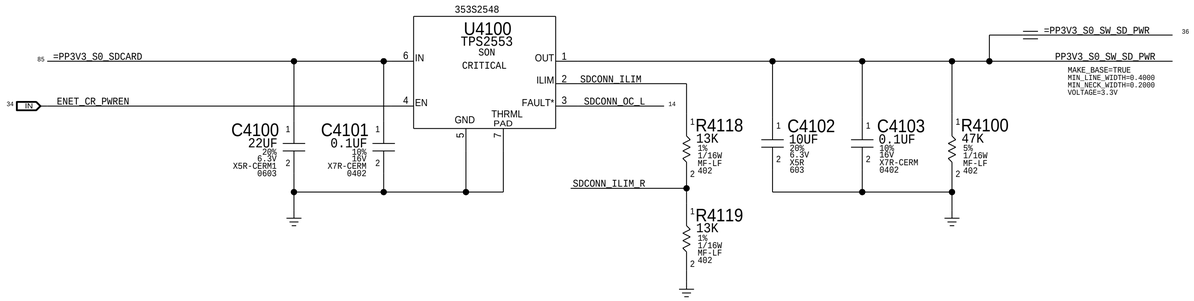
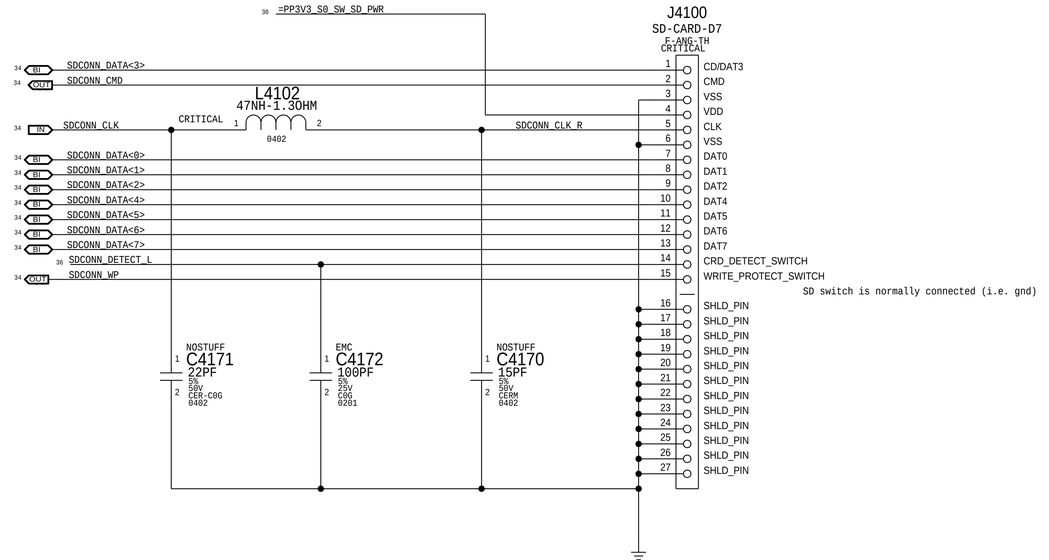
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

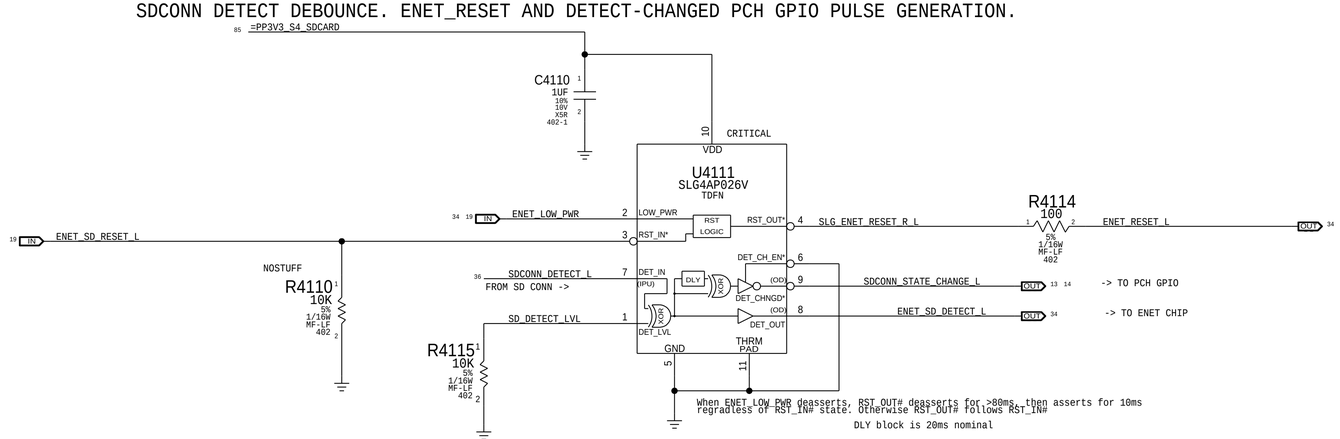


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



BOM_COST_GROUP=SD CARD

SYNC_MASTER=J117_MLB	SYNC_DATE=08/18/2014
PAGE TITLE: SD Reader Connector	
Apple Inc.	DRAWING NUMBER: 051-01477 SIZE: D
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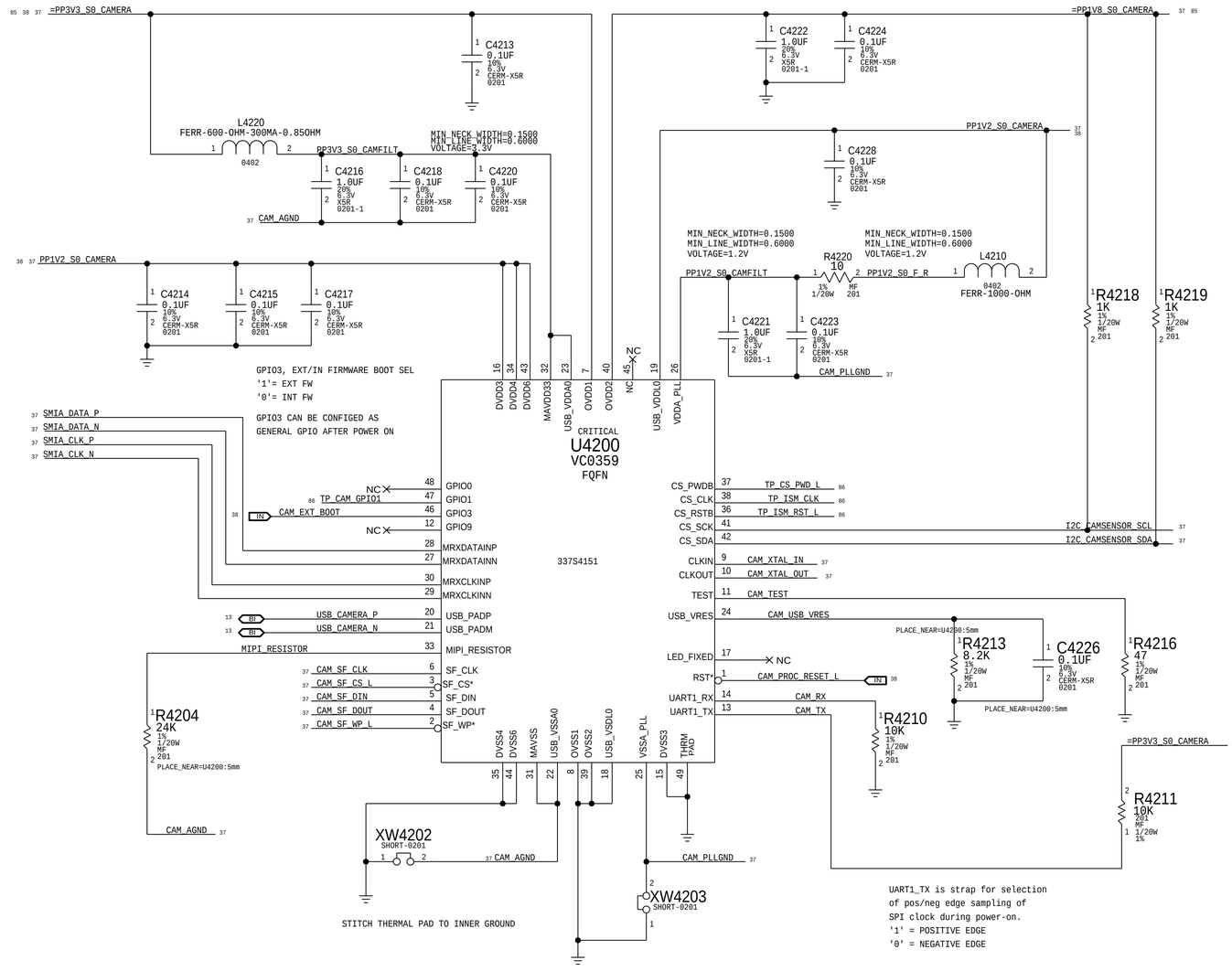
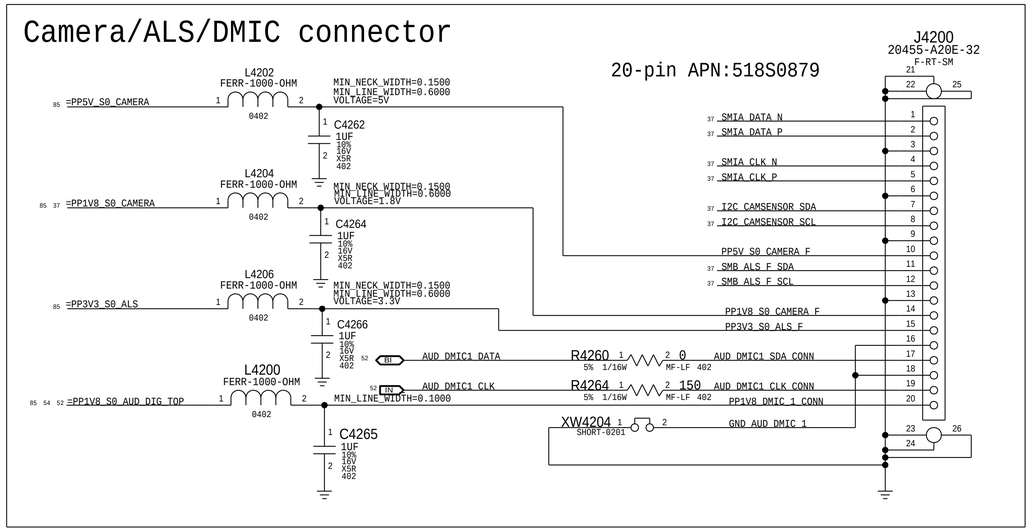
USB CAMERA CONTROLLER

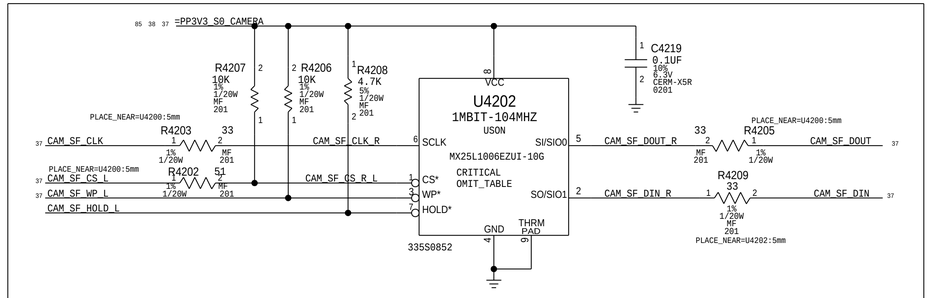


Camera/ALS/DMIC connector

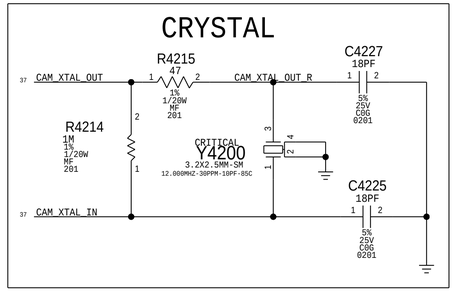


Use 100 ohms and 150pF for 10MHz filter

SERIAL FLASH



CRYSTAL



BOM_COST_GROUP=CAMERA

SYNC_MASTER=J117_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	Camera Controller
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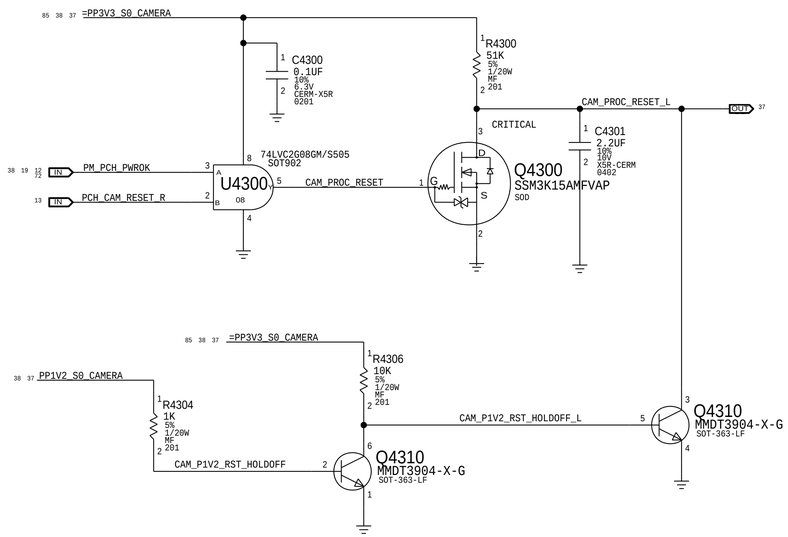
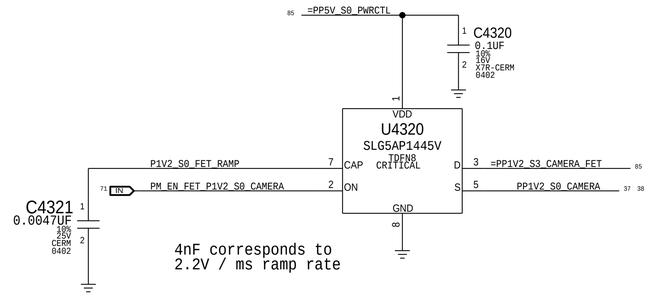
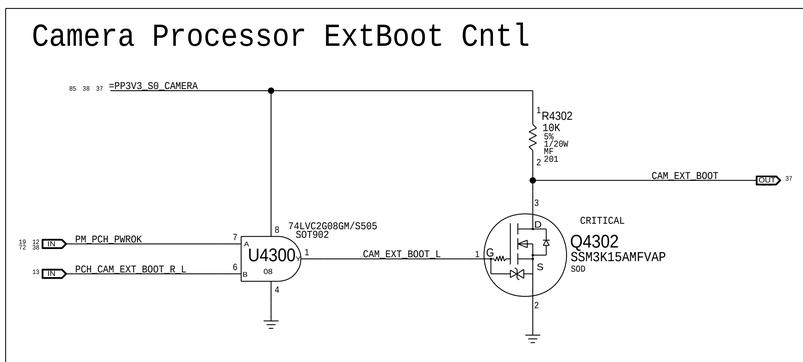
Camera Processor Reset



1.2V S0 Camera Pass FET



Camera Processor ExtBoot Cntl



BOM_COST_GROUP=CAMERA

SYNC_MASTER=J117_MLB SYNC_DATE=08/18/2014

PAGE TITLE

Camera Controller Support

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

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Internal DP Connector

518S0886

J4400
20525-160E-01
F-RT-SM

F4400
3AMP-32V-467
603-HF

L4400
FERR-120-OHM-3A
0603

=PP12V_S0_LCD
PP12V_LCD_F
VOLTAGE=12V
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1000
PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1000

C4420 10UF 10% 16V X5R-CERM 0805
C4401 0.001UF 20% 50V CERM 0402
C4421 0.1UF 10% 16V X7R-CERM 0402

NC
SMB_DP_MLB_MSR_SDA
SMB_DP_MLB_MSR_SCL
DP_INTPNL_ML_HPD
DP_INT_EG_SL_HPD
DP_INTPNL_ML_AUX_C_P
DP_INTPNL_ML_AUX_C_N
DP_INTPNL_ML_C_P<0>
DP_INTPNL_ML_C_N<0>
DP_INTPNL_ML_C_P<1>
DP_INTPNL_ML_C_N<1>
DP_INTPNL_ML_C_P<2>
DP_INTPNL_ML_C_N<2>
DP_INTPNL_ML_C_P<3>
DP_INTPNL_ML_C_N<3>
DP_INT_EG_SL_C_P<0>
DP_INT_EG_SL_C_N<0>
DP_INT_EG_SL_C_P<1>
DP_INT_EG_SL_C_N<1>
DP_INT_EG_SL_C_P<2>
DP_INT_EG_SL_C_N<2>
DP_INT_EG_SL_C_P<3>
DP_INT_EG_SL_C_N<3>
DP_INT_EG_SL_AUX_C_P
DP_INT_EG_SL_AUX_C_N
DP_TCON_RESET_L
PANEL_PGOOD
BLC_VSYNC
BLC_LSYNC
BLC_EN

DP Link AC Decoupling

GND_VOID=TRUE

DP_INT_EG_SL_P<0>	C4470	0.1UF
DP_INT_EG_SL_N<0>	C4471	0.1UF
DP_INT_EG_SL_P<1>	C4472	0.1UF
DP_INT_EG_SL_N<1>	C4473	0.1UF
DP_INT_EG_SL_P<2>	C4474	0.1UF
DP_INT_EG_SL_N<2>	C4475	0.1UF
DP_INT_EG_SL_P<3>	C4476	0.1UF
DP_INT_EG_SL_N<3>	C4477	0.1UF
DP_INT_EG_SL_AUX_P	C4478	0.1UF
DP_INT_EG_SL_AUX_N	C4479	0.1UF

10% 16V X5R-CERM 0201

=PP3V3_S0_GPU
R4430 100K 5% 1/20W MF 201
R4431 100K 5% 1/20W MF 201

TCON_RESET_L
NOSTUFF
R4402 0 5% 1/20W MF 201

=PP3V3_S4_PWRCTL
C4410 0.1UF 10% 16V X7R-CERM 0402

U4410
74LVC1G125DBVG4
SOT23-5
PM_PGOOD_FET_P12V_S0
PANEL_PGOOD_R
BUF_OE_L
R4411 100 5% 1/16W MF-LF 402
R4410 10K 5% 1/16W MF-LF 402

R4420 0 5% 1/20W MF 201
VIDEO_ON_L
Q4420
SSM3K15AMFVAP
SOD
TCON_BLC_EN

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=andres
SYNC_DATE=08/16/2016
PAGE TITLE: Internal DP Support

Apple Inc.

DRAWING NUMBER: 051-01477
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TP to DP aliases

IN	DP_X_SRC_ML_P<0>	DP_TBTSRC_ML_P<0>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_N<0>	DP_TBTSRC_ML_N<0>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_P<1>	DP_TBTSRC_ML_P<1>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_N<1>	DP_TBTSRC_ML_N<1>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_P<2>	DP_TBTSRC_ML_P<2>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_N<2>	DP_TBTSRC_ML_N<2>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_P<3>	DP_TBTSRC_ML_P<3>	MAKE_BASE=TRUE
IN	DP_X_SRC_ML_N<3>	DP_TBTSRC_ML_N<3>	MAKE_BASE=TRUE
BI	DP_X_SRC_AUX_P	DP_TBTSRC_AUXCH_P	MAKE_BASE=TRUE
BI	DP_X_SRC_AUX_N	DP_TBTSRC_AUXCH_N	MAKE_BASE=TRUE

=PP1V8_S0_DP

R4510 470K 5% 1/20W MF 201

R4511 470K 5% 1/20W MF 201

DP_INT_EG_ML_AUX_P — C4508 0.1UF — DP_INT_EG_ML_AUX_C_P

DP_INT_EG_ML_AUX_N — C4509 0.1UF — DP_INT_EG_ML_AUX_C_N

=PP1V8_S0_DP

R4512 470K 5% 1/20W MF 201

R4513 470K 5% 1/20W MF 201

DP_TBTSRC_AUXCH_P — C4510 0.1UF — DP_TBTSRC_AUX_C_P

DP_TBTSRC_AUXCH_N — C4511 0.1UF — DP_TBTSRC_AUX_C_N

DP_INT_EG_ML_HPD_BUF

R4500 200K 1% 1/20W MF 201

=PP3V3_S0_INTDPMUX

R4504 10K 5% 1/20W MF 201

DP_GPU_MUX_EN

R4501 10K 5% 1/20W MF 201

U4500.A1:8MM

=PP3V3_S0_INTDPMUX

C4568 0.1UF 10% 6.3V CERM-X5R 0201

C4569 0.1UF 10% 6.3V CERM-X5R 0201

U4500 CBTL06142EEE TFBGA CRITICAL

DP_INT_EG_ML_P<0>	B4	DIN1_0+	
DP_INT_EG_ML_N<0>	A4	DIN1_0-	
DP_INT_EG_ML_P<1>	B5	DIN1_1+	
DP_INT_EG_ML_N<1>	A5	DIN1_1-	
DP_INT_EG_ML_P<2>	B6	DIN1_2+	
DP_INT_EG_ML_N<2>	A6	DIN1_2-	
DP_INT_EG_ML_P<3>	A8	DIN1_3+	
DP_INT_EG_ML_N<3>	A9	DIN1_3-	
	H9	DAUX1+	
	J9	DAUX1-	
NC	H8	DDC_CLK1	
NC	J8	DDC_DAT1	
	J2	HPD_1	
DP_TBTSRC_ML_C_P<0>	B8	DIN2_0+	
DP_TBTSRC_ML_C_N<0>	B9	DIN2_0-	
DP_TBTSRC_ML_C_P<1>	D8	DIN2_1+	
DP_TBTSRC_ML_C_N<1>	D9	DIN2_1-	
DP_TBTSRC_ML_C_P<2>	E8	DIN2_2+	
DP_TBTSRC_ML_C_N<2>	E9	DIN2_2-	
DP_TBTSRC_ML_C_P<3>	F8	DIN2_3+	
DP_TBTSRC_ML_C_N<3>	F9	DIN2_3-	
	H6	DAUX2+	
	J6	DAUX2-	
NC	H5	DDC_CLK2	
NC	J5	DDC_DAT2	
DP_X_SRC_HPD	H3	HPD_2	
DP_TBT_SEL	A1	GPU_SEL	
	B7	XSD*	
	C2	DDC_AUX_SEL	
	B3	GND	
	C8	GND	
	G8	GND	
	H4	GND	
	H7	GND	
	G2	GND	

PD is on the LR page

DOUT_0+	B2	DP_INTPNL_ML_P<0>	C4500 0.1UF
DOUT_0-	B1	DP_INTPNL_ML_N<0>	C4501 0.1UF
DOUT_1+	D2	DP_INTPNL_ML_P<1>	C4502 0.1UF
DOUT_1-	D1	DP_INTPNL_ML_N<1>	C4503 0.1UF
DOUT_2+	E2	DP_INTPNL_ML_P<2>	C4504 0.1UF
DOUT_2-	E1	DP_INTPNL_ML_N<2>	C4505 0.1UF
DOUT_3+	F2	DP_INTPNL_ML_P<3>	C4506 0.1UF
DOUT_3-	F1	DP_INTPNL_ML_N<3>	C4507 0.1UF

0201 10% 6.3V CERM-X5R 6.3V

DP_INTPNL_ML_C_P<0> … DP_INTPNL_ML_C_P<3>

DP_INTPNL_ML_C_N<0> … DP_INTPNL_ML_C_N<3>

AUX+	H2	DP_INTPNL_ML_AUX_P	R4558 0 5% 1/20W MF 0201 — DP_INTPNL_ML_AUX_C_P
AUX-	H1	DP_INTPNL_ML_AUX_N	R4559 0 5% 1/20W MF 0201 — DP_INTPNL_ML_AUX_C_N
HPDIN	J1	DP_INTPNL_ML_HPD_BUF	

R4502 100K 5% 1/20W MF 201

R4503 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

IN	DP_TBTSRC_ML_P<0>	DP_TBTSRC_ML_C_P<0>
IN	DP_TBTSRC_ML_N<0>	DP_TBTSRC_ML_C_N<0>
IN	DP_TBTSRC_ML_P<1>	DP_TBTSRC_ML_C_P<1>
IN	DP_TBTSRC_ML_N<1>	DP_TBTSRC_ML_C_N<1>
IN	DP_TBTSRC_ML_P<2>	DP_TBTSRC_ML_C_P<2>
IN	DP_TBTSRC_ML_N<2>	DP_TBTSRC_ML_C_N<2>
IN	DP_TBTSRC_ML_P<3>	DP_TBTSRC_ML_C_P<3>
IN	DP_TBTSRC_ML_N<3>	DP_TBTSRC_ML_C_N<3>

MAKE_BASE=TRUE

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=armin SYNC_DATE=11/03/2015

PAGE TITLE: DISPLAY: MUXing

Apple Inc.

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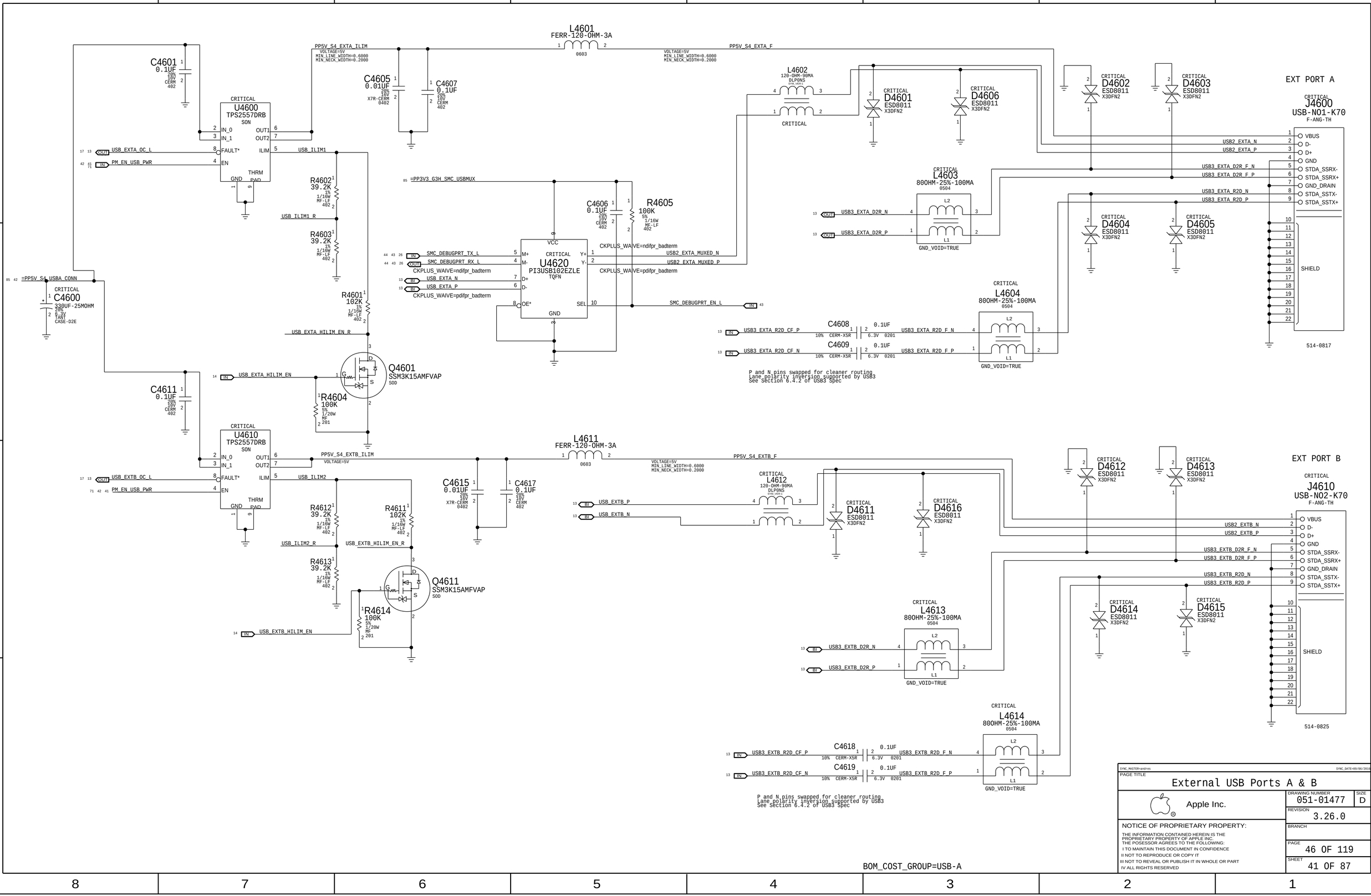
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTA_F
C4601 0.1UF 20% 10V CERM 402
C4605 0.01UF 20% 10V X7R-CERM 0402
C4607 0.1UF 20% 10V CERM 402
CRITICAL
U4600
TPS2557DRB
SON
IN_0
IN_1
OUT1
OUT2
FAULT*
EN
ILIM
THRM PAD
GND
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602 39.2K 1% 1/10W MF-LF 402
R4603 39.2K 1% 1/10W MF-LF 402
USB_ILIM1_R
R4601 102K 1% 1/16W MF-LF 402
USB_EXTA_HILIM_EN_R
=PP5V_S4_USBA_CONN
CRITICAL
C4600 330UF-25MOHM 20% 6.3V TANT CASE-D2E
C4611 0.1UF 20% 10V CERM 402
USB_EXTA_HILIM_EN
Q4601
SSM3K15AMFVAP
SOD
R4604 100K 5% 1/20W MF 201
CRITICAL
U4610
TPS2557DRB
SON
PP5V_S4_EXTB_ILIM
VOLTAGE=5V
USB_EXTB_OC_L
PM_EN_USB_PWR
USB_ILIM2
R4612 39.2K 1% 1/10W MF-LF 402
R4611 102K 1% 1/10W MF-LF 402
USB_ILIM2_R
USB_EXTB_HILIM_EN_R
R4613 39.2K 1% 1/10W MF-LF 402
Q4611
SSM3K15AMFVAP
SOD
R4614 100K 5% 1/20W MF 201
USB_EXTB_HILIM_EN
=PP3V3_G3H_SMC_USBMUX
C4606 0.1UF 20% 10V CERM 402
R4605 100K 5% 1/16W MF-LF 402
CRITICAL
U4620
PI3USB102EZLE
TQFN
VCC
GND
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_N
USB_EXTA_P
M+
M-
D+
D-
OE*
SEL
Y+
Y-
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601 ESD8011 X3DFN2
D4606 ESD8011 X3DFN2
D4602 ESD8011 X3DFN2
D4603 ESD8011 X3DFN2
D4604 ESD8011 X3DFN2
D4605 ESD8011 X3DFN2
EXT PORT A
CRITICAL
J4600
USB-NO1-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_D2R_F_N
USB3_EXTA_D2R_F_P
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_N
USB3_EXTA_R2D_P
CRITICAL
L4603
80OHM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
CRITICAL
L4604
80OHM-25%-100MA
0504
C4608 0.1UF 10% CERM-X5R 6.3V 0201
C4609 0.1UF 10% CERM-X5R 6.3V 0201
USB3_EXTA_R2D_CF_P
USB3_EXTA_R2D_CF_N
USB3_EXTA_R2D_F_N
USB3_EXTA_R2D_F_P
P and N pins swapped for cleaner routing
Lane polarity inversion supported by USB3
See Section 6.4.2 of USB3 Spec
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_F
C4615 0.01UF 20% 10V X7R-CERM 0402
C4617 0.1UF 20% 10V CERM 402
USB_EXTB_P
USB_EXTB_N
CRITICAL
L4612
120-OHM-90MA
DLP0NS
CRITICAL
D4611 ESD8011 X3DFN2
D4616 ESD8011 X3DFN2
D4612 ESD8011 X3DFN2
D4613 ESD8011 X3DFN2
D4614 ESD8011 X3DFN2
D4615 ESD8011 X3DFN2
EXT PORT B
CRITICAL
J4610
USB-NO2-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0825
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_D2R_F_N
USB3_EXTB_D2R_F_P
USB3_EXTB_R2D_N
USB3_EXTB_R2D_P
CRITICAL
L4613
80OHM-25%-100MA
0504
GND_VOID=TRUE
CRITICAL
L4614
80OHM-25%-100MA
0504
C4618 0.1UF 10% CERM-X5R 6.3V 0201
C4619 0.1UF 10% CERM-X5R 6.3V 0201
USB3_EXTB_R2D_CF_P
USB3_EXTB_R2D_CF_N
USB3_EXTB_R2D_F_N
USB3_EXTB_R2D_F_P
P and N pins swapped for cleaner routing
Lane polarity inversion supported by USB3
See Section 6.4.2 of USB3 Spec
BOM_COST_GROUP=USB-A
SYNC_MASTER=andres
SYNC_DATE=09/06/2016
PAGE TITLE
External USB Ports A & B
Apple Inc.
DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
BRANCH
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SHEET 41 OF 87
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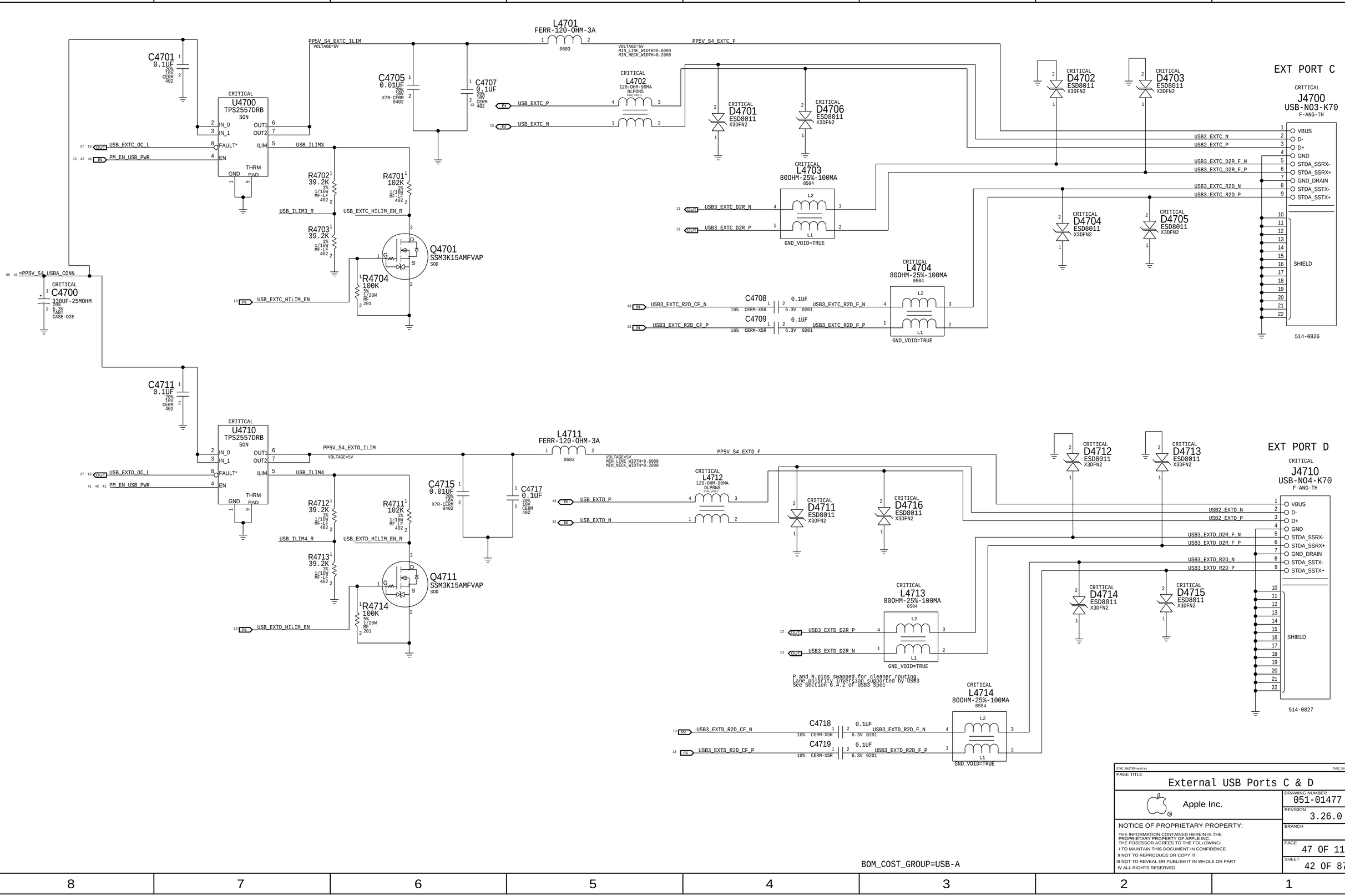

SYNC_MASTER=andres SYNC_DATE=09/06/2016

PAGE TITLE

External USB Ports C & D

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

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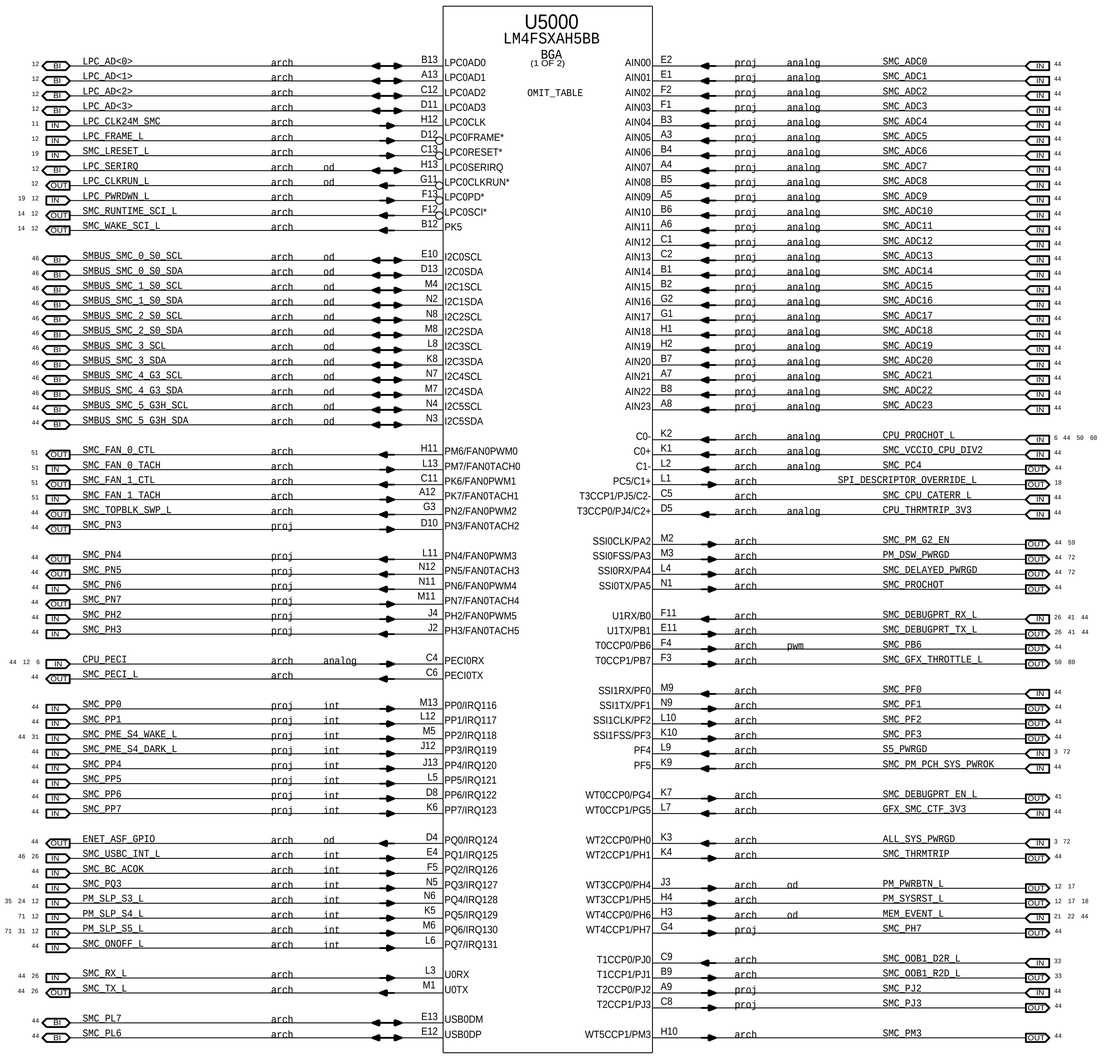
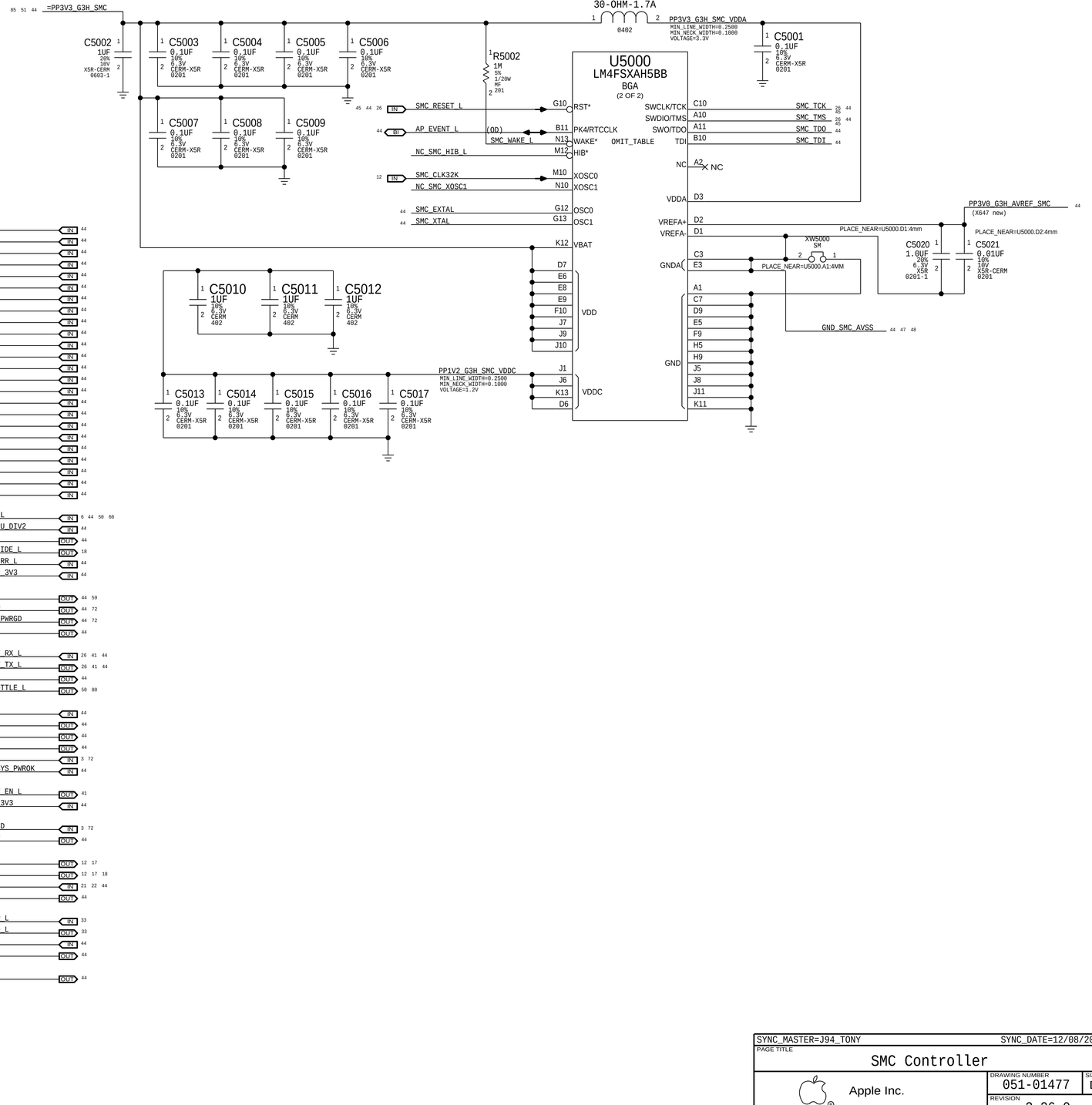
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





BOM_COST_GROUP=SMC

SYNC_MASTER=J94_TONY SYNC_DATE=12/08/2014

PAGE TITLE: SMC Controller

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D
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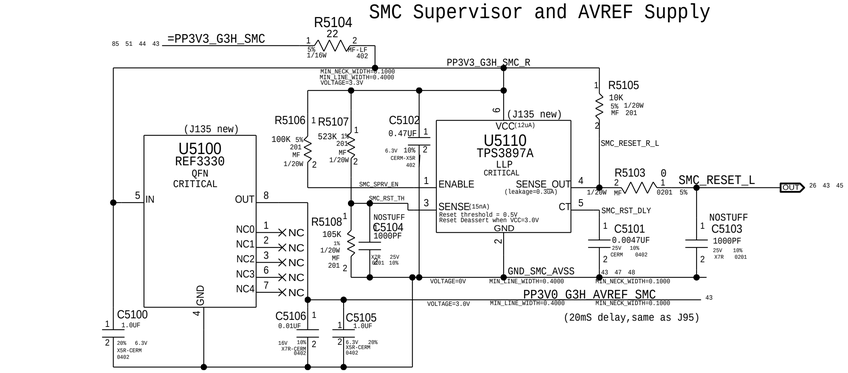
SMC Supervisor and AVREF Supply



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	VD2R
SMC_ADC1	ISNS_P12VG3H	ID2R
SMC_ADC2	ISNS_P12VS0_GPU	IG20
SMC_ADC3	ISNS_P12VS0_CPUCORE	IC20
SMC_ADC4	VSNS_CPUVCC	VC0C
SMC_ADC5	ISNS_CPUVCC	IC0C
SMC_ADC6	VSNS_CPUVCC_GT	VC0G
SMC_ADC7	ISNS_CPUVCC_GT	IC0G
SMC_ADC8	VSNS_FBVDDQ	VG0F
SMC_ADC9	ISNS_FBVDDQ	IG0F
SMC_ADC10	ISNS_CPUVCC_SA	IC0S
SMC_ADC11	ISNS_CPUVCC_IO	IC0I
SMC_ADC12	VSNS_GPUCORE_ALT	VG0C
SMC_ADC13	ISNS_GPUCORE_ALT	IG0C
SMC_ADC14	VSNS_GPU_VDDCI	VG0I
SMC_ADC15	ISNS_GPU_VDDCI	IG0I
SMC_ADC16	VSNS_P5VS4	VR54
SMC_ADC17	ISNS_P5VS4	IR54
SMC_ADC18	VSNS_P3V3S5	VR35
SMC_ADC19	ISNS_P3V3S5	IR35
SMC_ADC20	ISNS_P5VS4_USB	IU54
SMC_ADC21	ISNS_SSD_S4	IH1R
SMC_ADC22	VSNS_VDDQS3_DDR	VM0R
SMC_ADC23	ISNS_VDDQS3_DDR	IR13

Project-specific Aliases

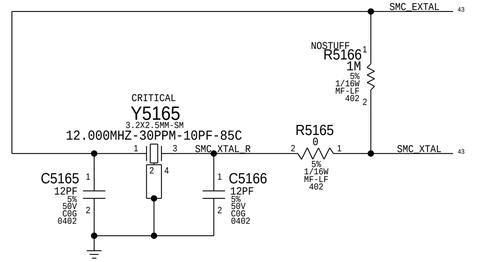
SMC_PN5	ACDC_BURST_EN_L
SMC_PJ3	SMC_OOB2_R2D_L
SMC_PJ2	SMC_OOB2_D2R_L
SMC_PP0	SMC_ACDC_ID
SMC_PH2	SMC_ASSERT_RTCRST
SMC_PL6	SMC_WIFI_PWR_EN
SMC_PC4	MEM_GOOD_LED
SMC_PN3	TCON_BLC_EN
SMC_PH7	GFX_OK
SMC_PL7	SMC_BT_PWR_EN
SMC_PM3	PSU_OCP_ACTIVE
SMC_PP1	PM_EPO_SMC_L
SMC_PN7	DP_LINK_OK
SMC_PN4	GFX_SMC_ALERT_R
SMC_PB6	SMC_EXT_VIDEO_SEL

Unused Project-specific

SMC_PP5	NC_SMC_PP5
SMC_PP4	NC_SMC_S4_WAKESRC_EN
SMC_PP6	NC_SMC_PP6
SMC_PP7	NC_SMC_PP7
SMC_PN6	NC_SMC_PN6
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA
SMC_PF0	NC_SPI_SMC_MISO
SMC_PF1	NC_SPI_SMC_MOSI
SMC_PF2	NC_SPI_SMC_CLK
SMC_PF3	NC_SPI_SMC_CS_L
SMC_PH3	NC_SMC_PH3
SMC_PO3	NC_G3_POWERON_L

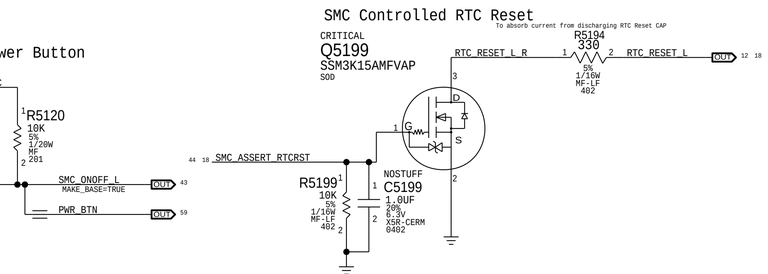
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal

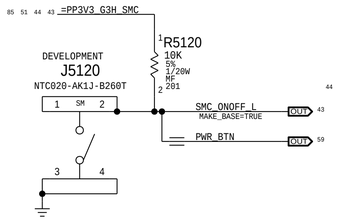


SMC Controlled RTC Reset

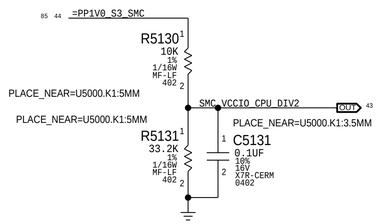
To absorb current from discharging RTC Reset CAP



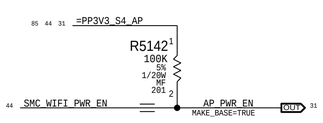
Power Button



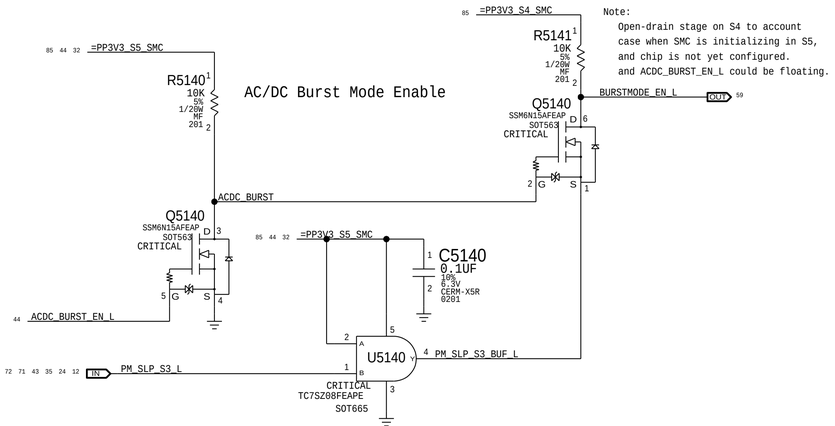
Comparator Reference



SMC control for AirPort power

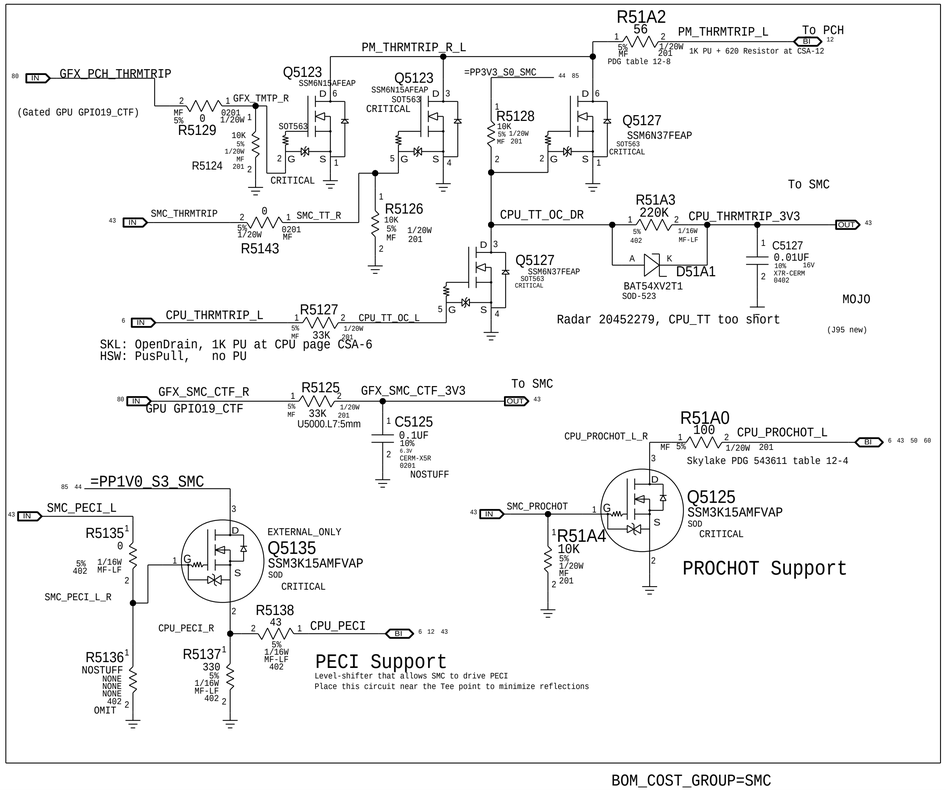


AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

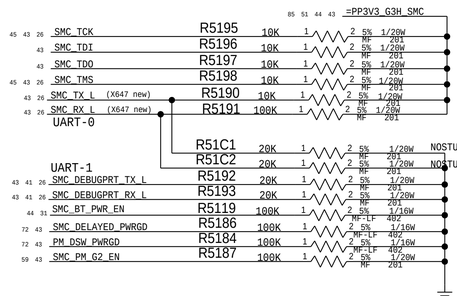
Platform Thermal Control



BOM_COST_GROUP=SMC

Arch Pull-Up/Down

Serial/JTAG Interface Pull-Up/Down



SYNC_MASTER=dtuzman SYNC_DATE=03/29/2016

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

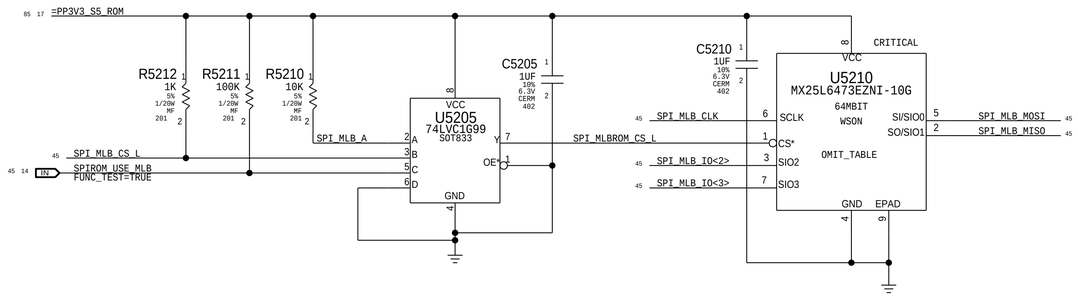
BRANCH:

PAGE: 51 OF 119

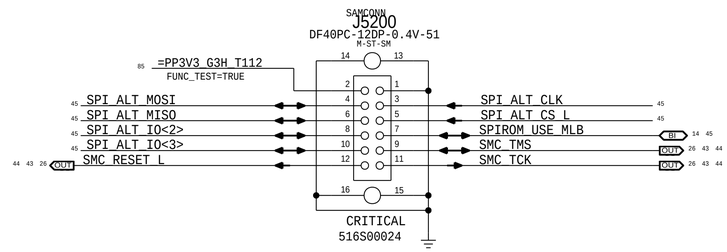
SHEET: 44 OF 87

SPI BootROM

Quad_IO Mode (Mode 0 & 3) supported
SPI Freq: 50MHz for PCH, 20 MHz for SMC

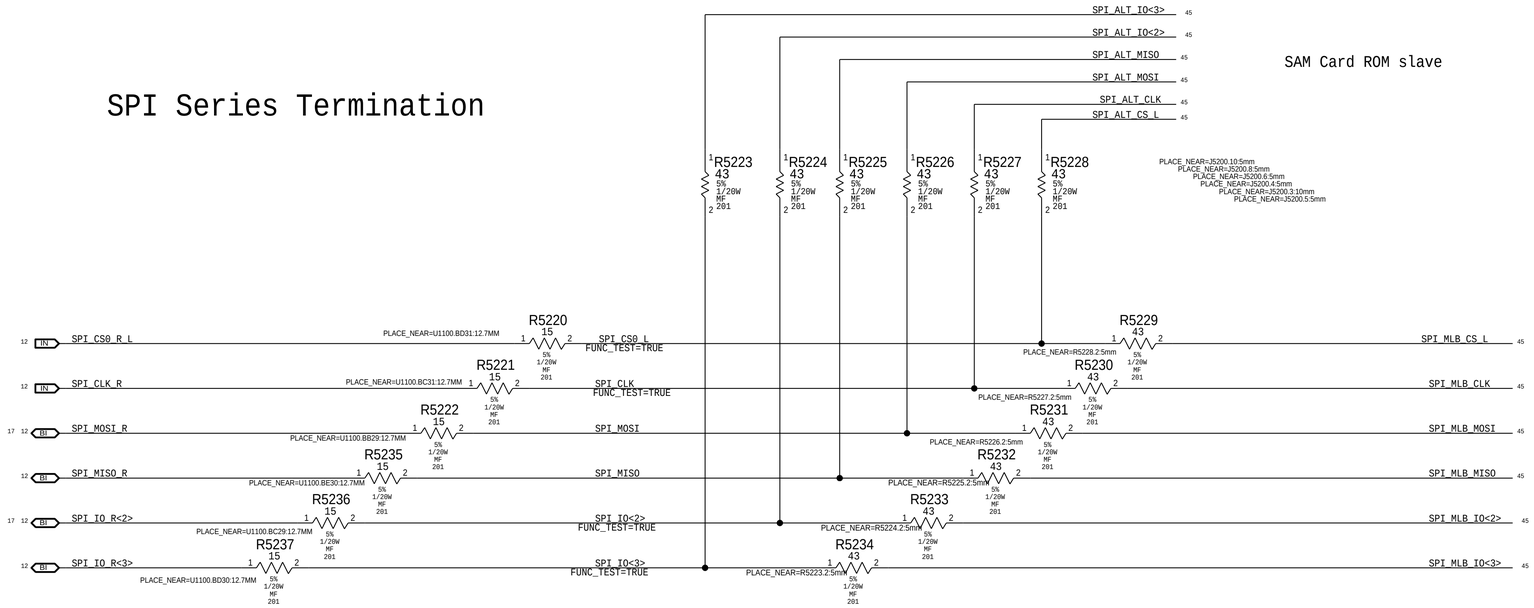


SPI+SWD SAM Connector



SPI Series Termination

SAM Card ROM slave



BOM_COST_GROUP=DEBUG

SYNC_MASTER=J94_TONY SYNC_DATE=10/02/2014

PAGE TITLE
SPI and Debug Connector

Apple Inc.

DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
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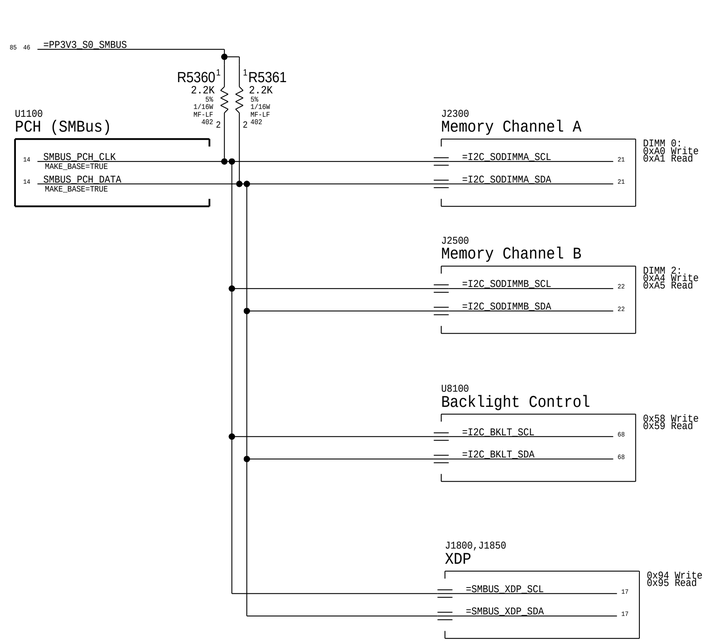

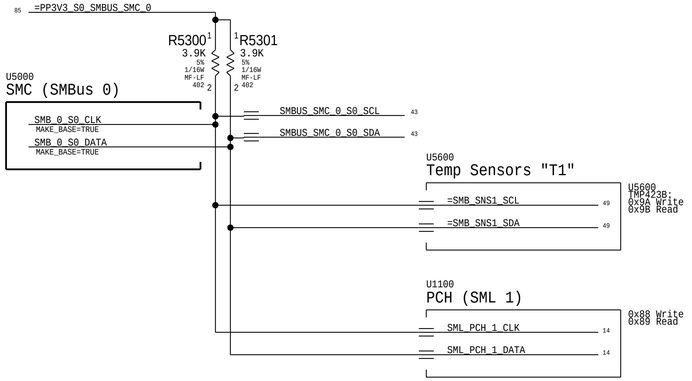

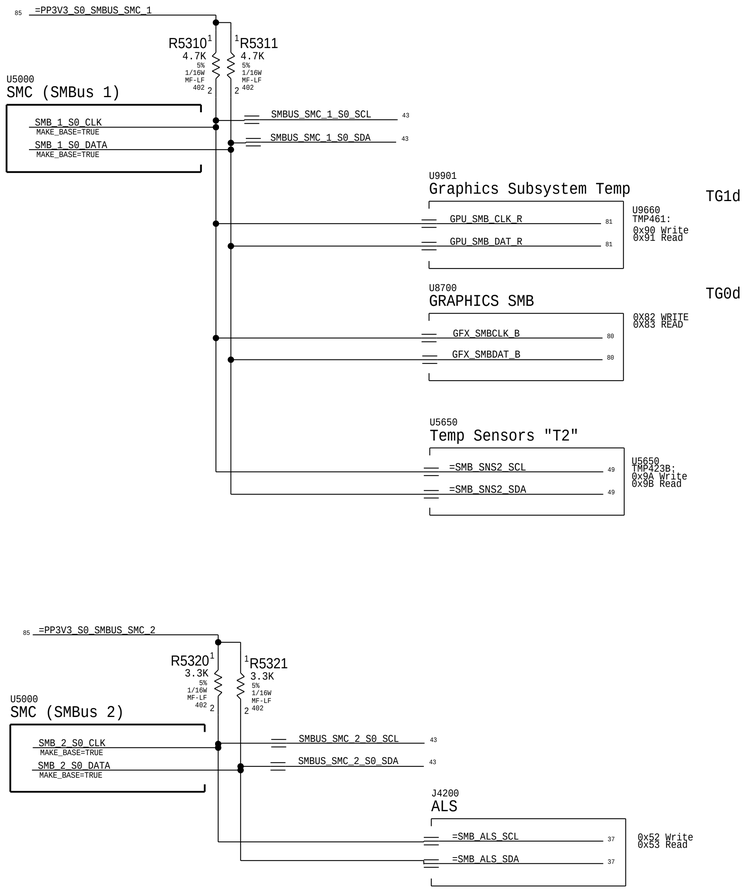

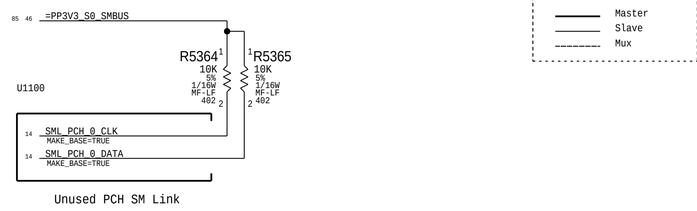

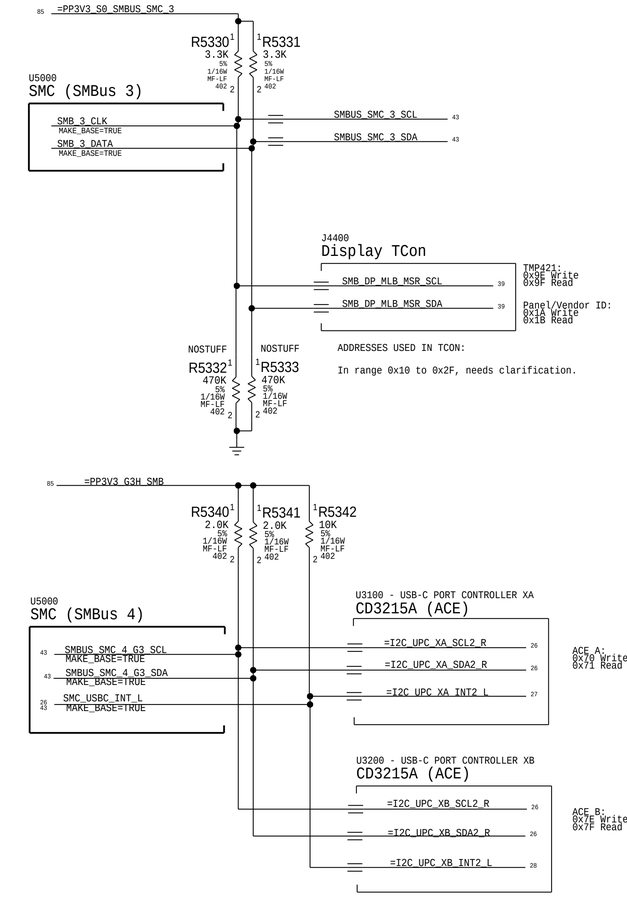

Line Legend
- Master
- Slave
- Mux

BOM_COST_GROUP=SMC

SYNC_MASTER=j135 SYNC_DATE=12/16/2015

PAGE TITLE
SMC: SMBus Connections

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D
REVISION 3.26.0
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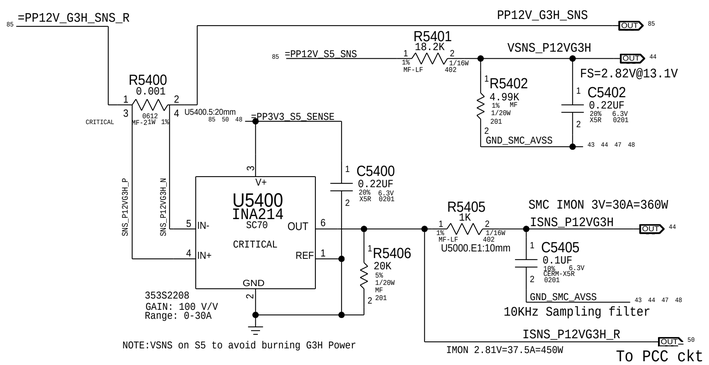
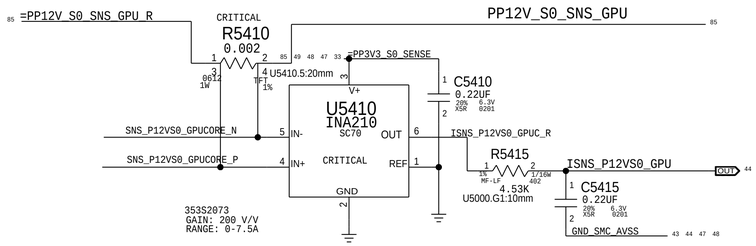
PP12V_G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



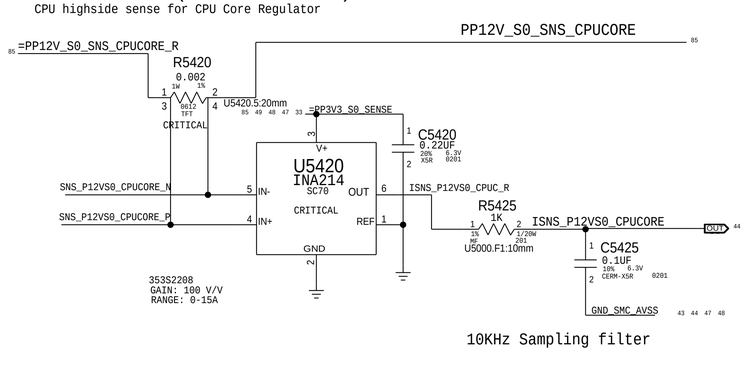
PP12V_S0_GPU (VD2R/IG20:ADC2)

GPU highside sense for GPU Core Regulator



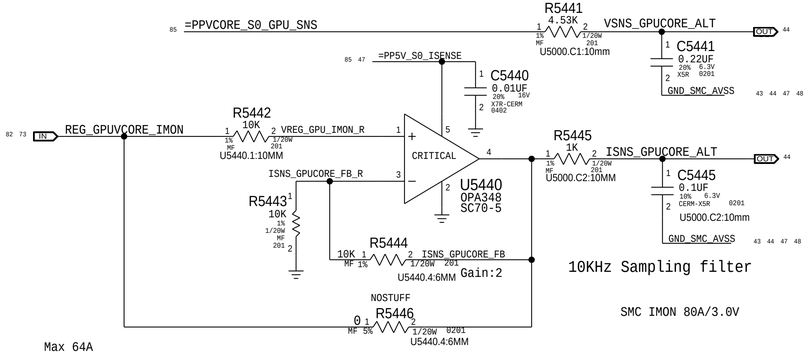
PP12V_S0_CPU (VD2R/IC20:ADC3)

CPU highside sense for CPU Core Regulator



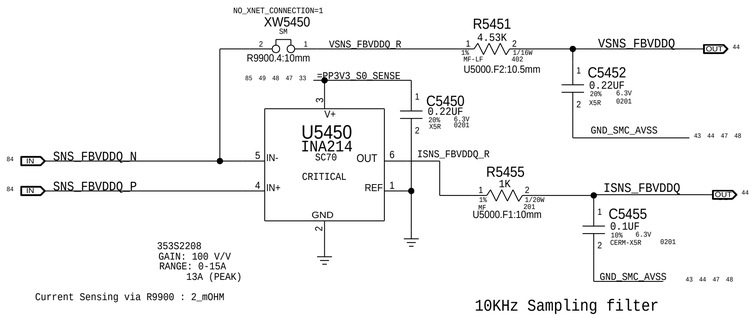
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp

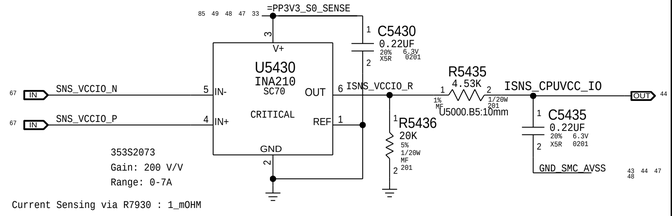


GPU FB (VG0F:ADC8/IG0F:ADC9)

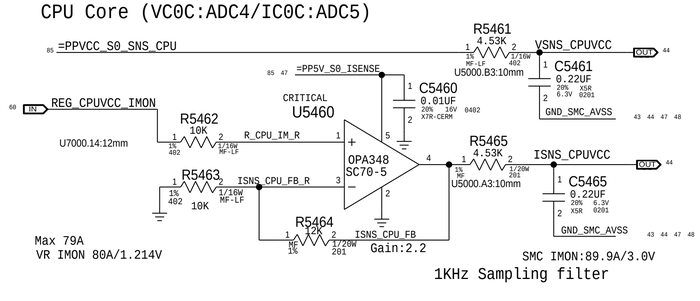
GPU lowside sense for Frame Buffer 1.5V/1.35V VDDQ



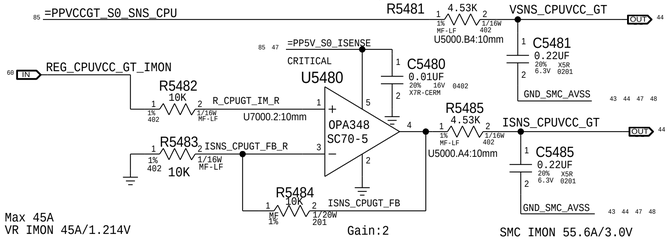
CPU VCCIO (0.95V/IC0I:ADC11)



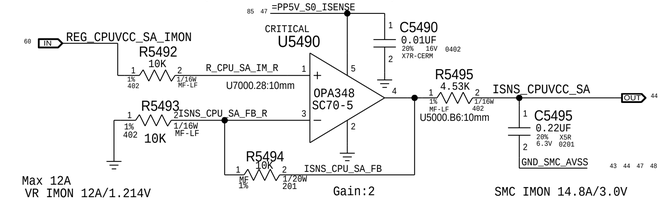
CPU Core (VC0C:ADC4/IC0C:ADC5)



CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU Core VCC_SA (1.05V/IC0S:ADC10)



BOM_COST_GROUP=SENSORS

PAGE TITLE

SENSORS: I and V Sense 1

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

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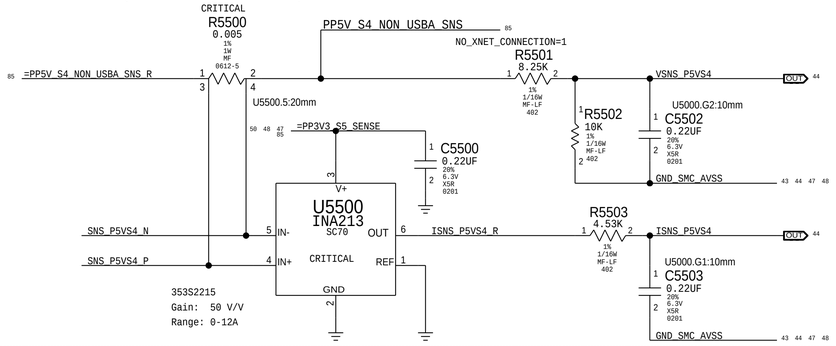
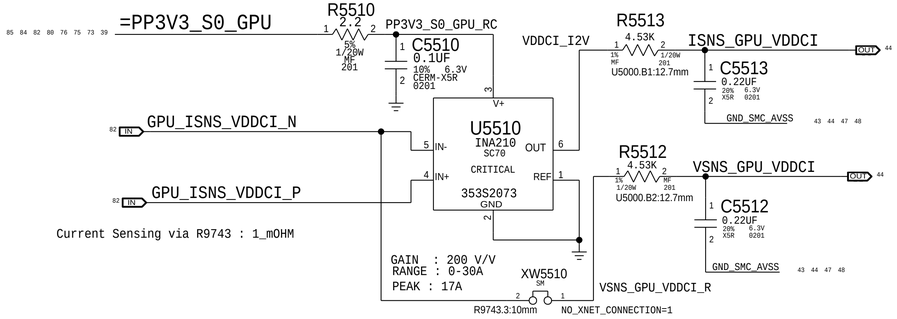
PP5V_S4 (VR54:ADC16/IR54:ADC17)

PP5V S4 (Non-USB-A)low side power distribution

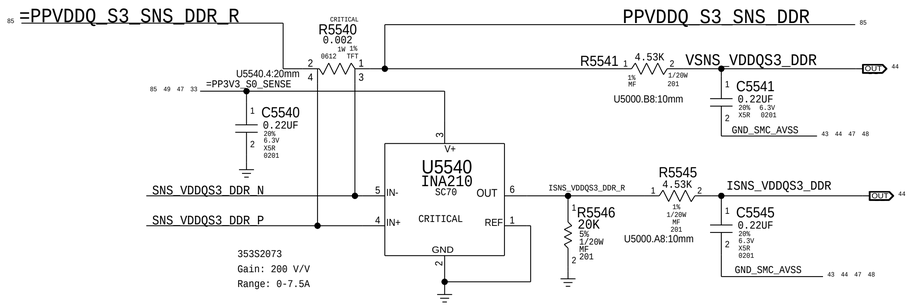


GPU_VDDCI S0 (VG0I:ADC14/IG0I:ADC15)



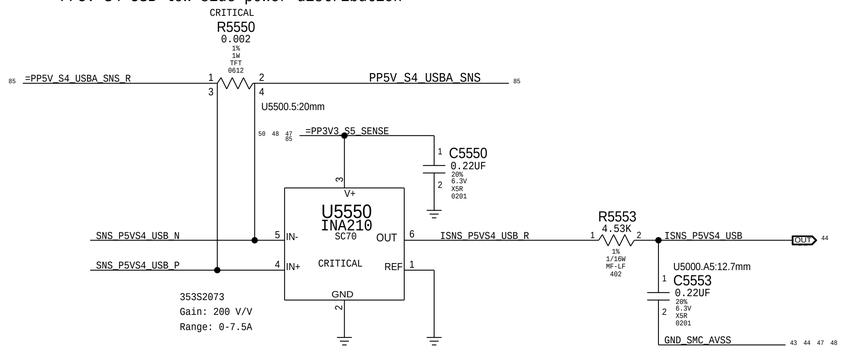
VDDQ S3 (VM0R:ADC22/IR13:ADC23)

VDDQ lowside sense for CPU Mem Controller (IC0M) and SO-DIMM modules



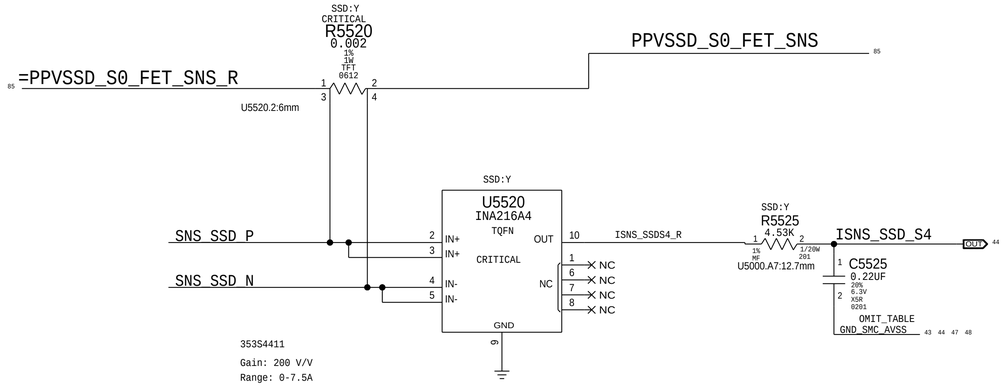
PP5V_S4_USB (VR54/IU54:ADC20)

PP5V S4 USB low side power distribution



SSD S0 (VR35/IH1R:ADC21)

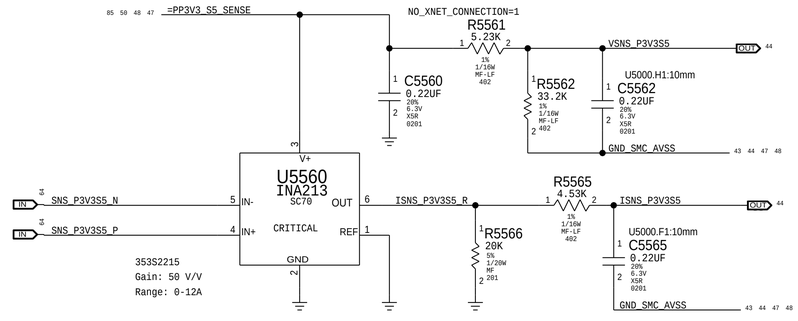
I-SENSE FOR SSD / V-SENSE FOR PPSSD_S0)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5525	SSD:Y
117S0201	1	RES,0 OHM,201	C5525	SSD:N

PP3V3_S5 (VR35:ADC18/IR35:ADC19)

PP3V3 S5 low side power distribution



BOM_COST_GROUP=SENSORS

SYNC_MASTER=VEAGH SYNC_DATE=03/16/2016

PAGE TITLE

SENSORS: I and V Sense 2

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

REVISION 3.26.0

BRANCH

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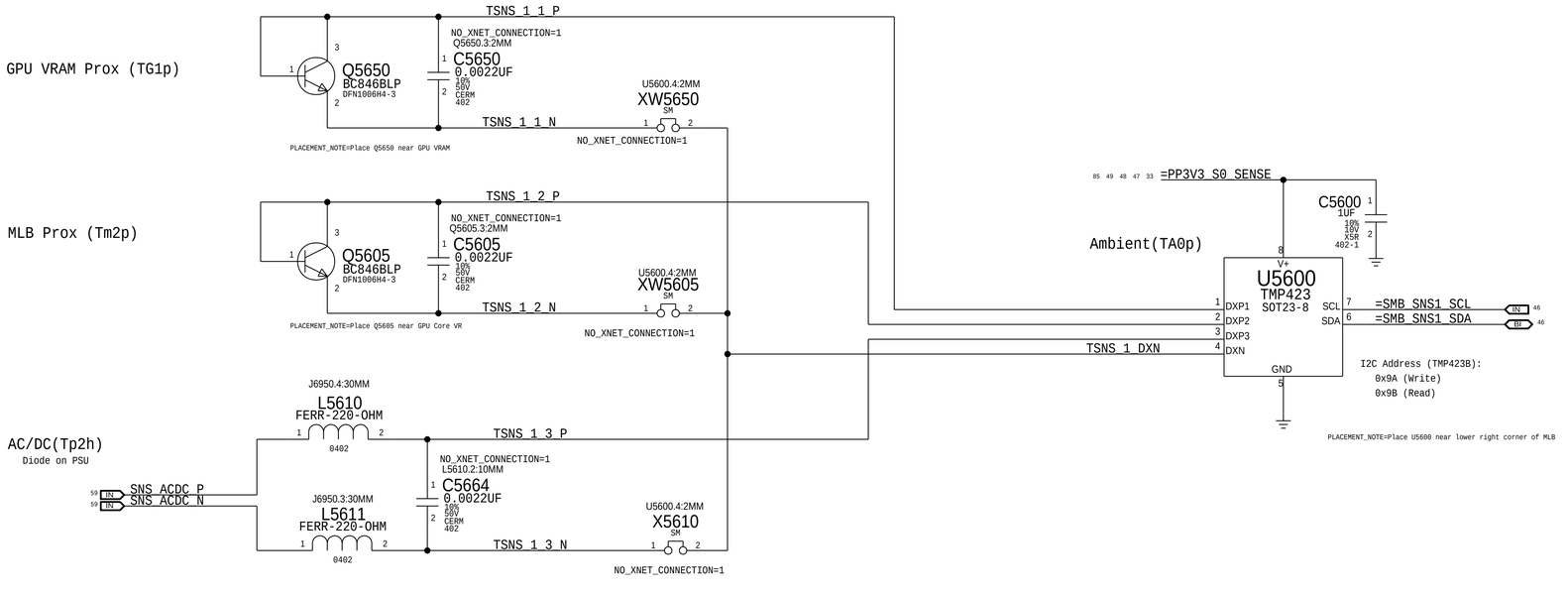
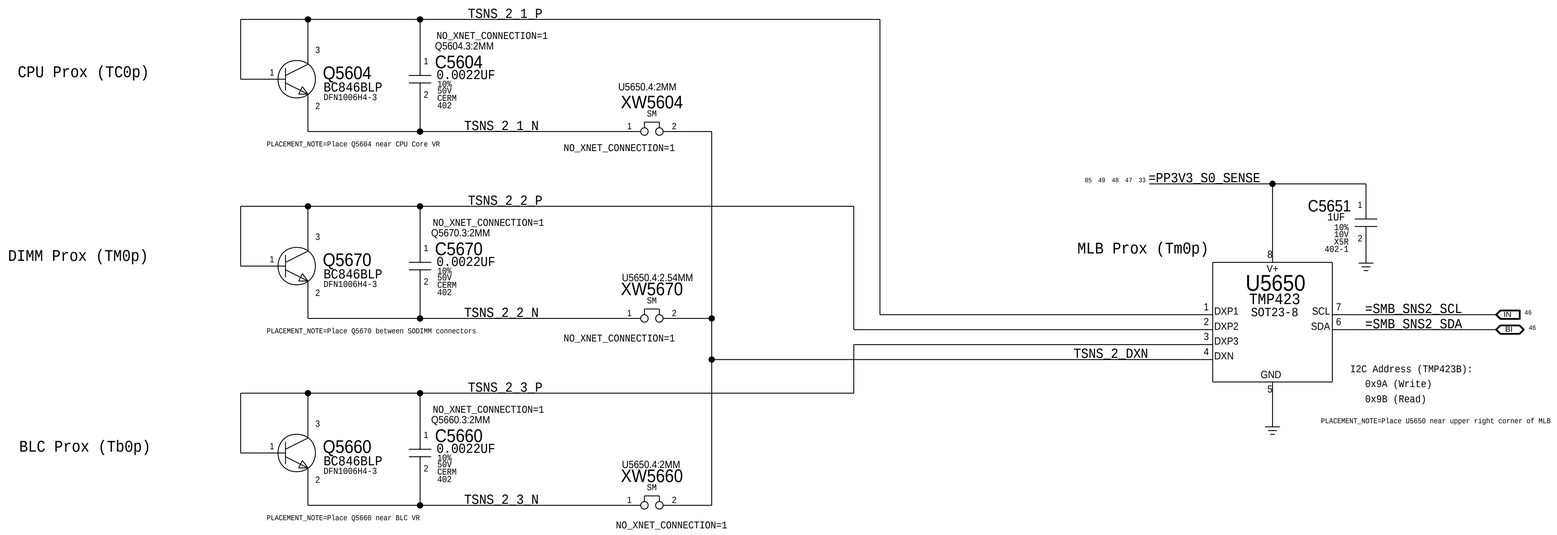
TEMPERATURE SENSOR T1

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



TEMPERATURE SENSOR T2



BOM_COST_GROUP=SENSORS

SYNC_MASTER=YEUNGR SYNC_DATE=03/16/2016

PAGE TITLE

SENSORS: Temperature Sensors

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D

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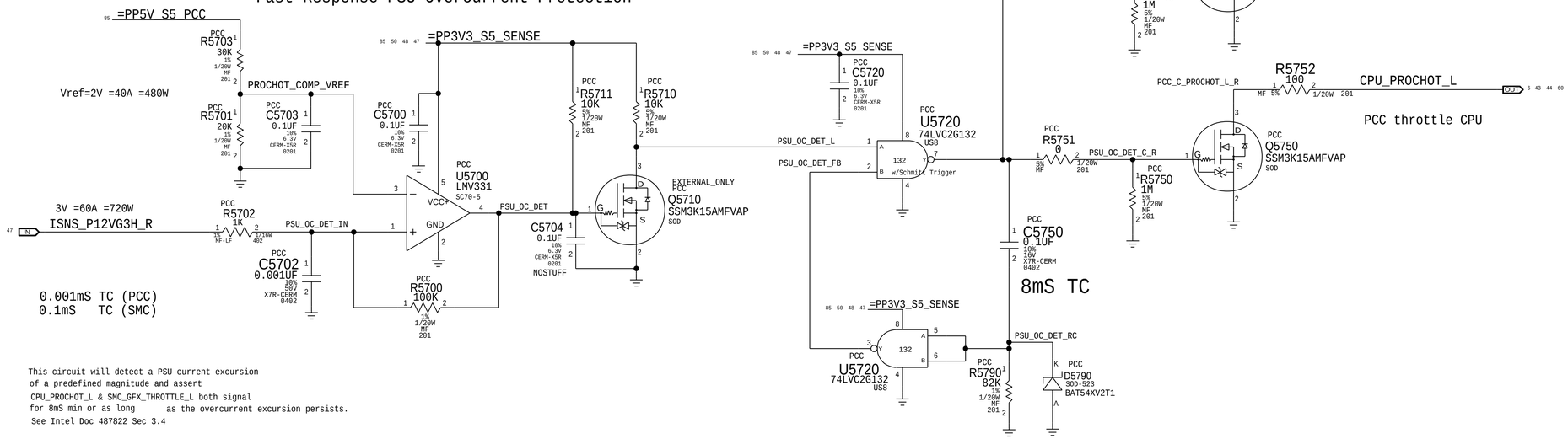
Fast Response PSU Overcurrent Protection



This circuit will detect a PSU current excursion
of a predefined magnitude and assert
CPU_PROCHOT_L & SMC_GFX_THROTTLE_L both signal
for 8mS min or as long as the overcurrent excursion persists.
See Intel Doc 487822 Sec 3.4

BOM_COST_GROUP=SENSORS

SYNC_MASTER=jerry SYNC_DATE=11/20/2015

PAGE TITLE: SENSORS: PSU/PCC

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

BRANCH:

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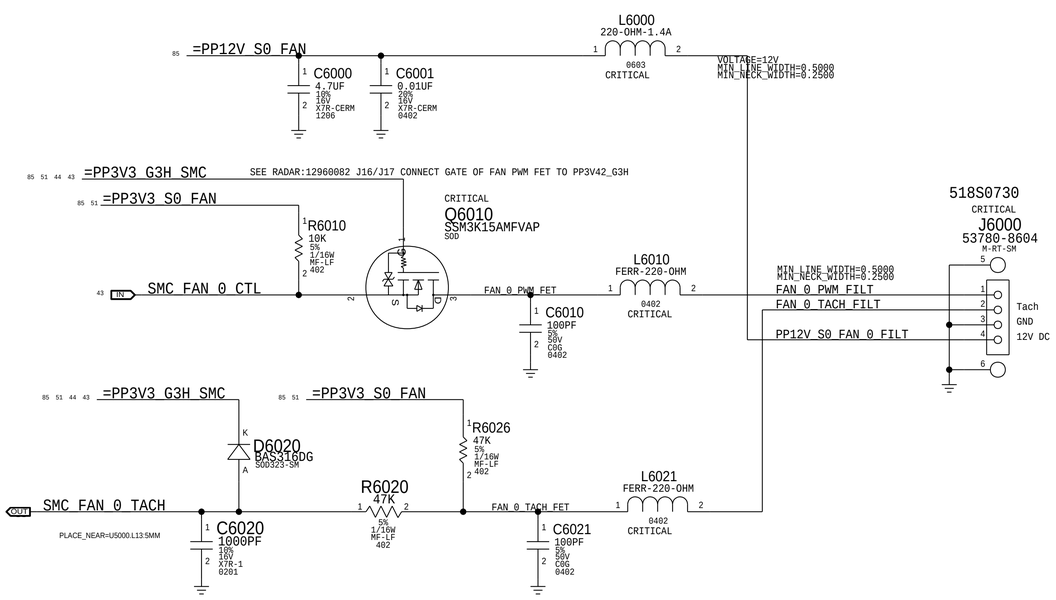
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

BOM_COST_GROUP=FAN

SYNC_MASTER=J117_MLB SYNC_DATE=08/01/2014

PAGE TITLE
System Fan Connector

Apple Inc.

DRAWING NUMBER 051-01477 SIZE D
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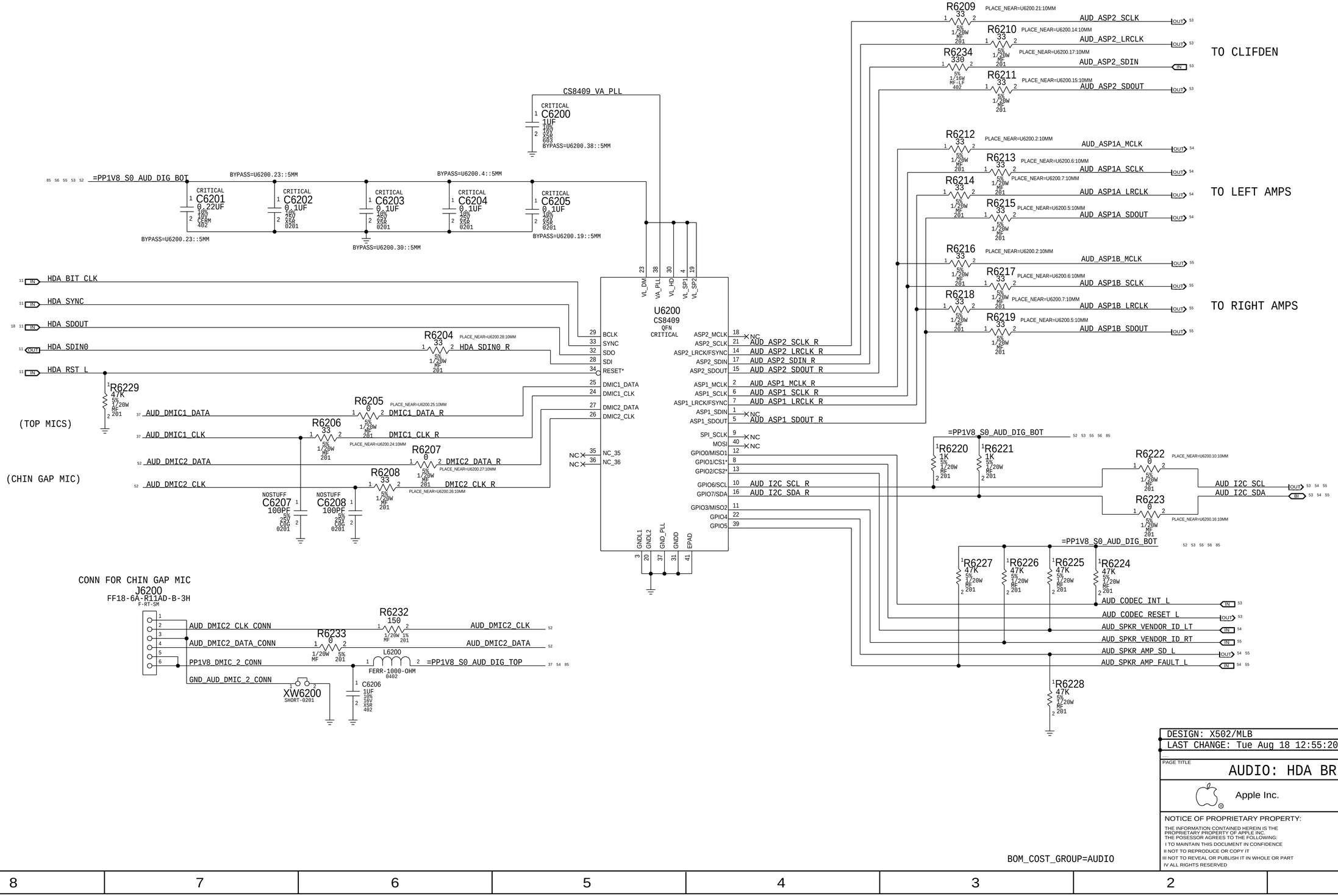

DESIGN: X502/MLB

LAST CHANGE: Tue Aug 18 12:55:20 2015

PAGE TITLE

AUDIO: HDA BRIDGE

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

BRANCH

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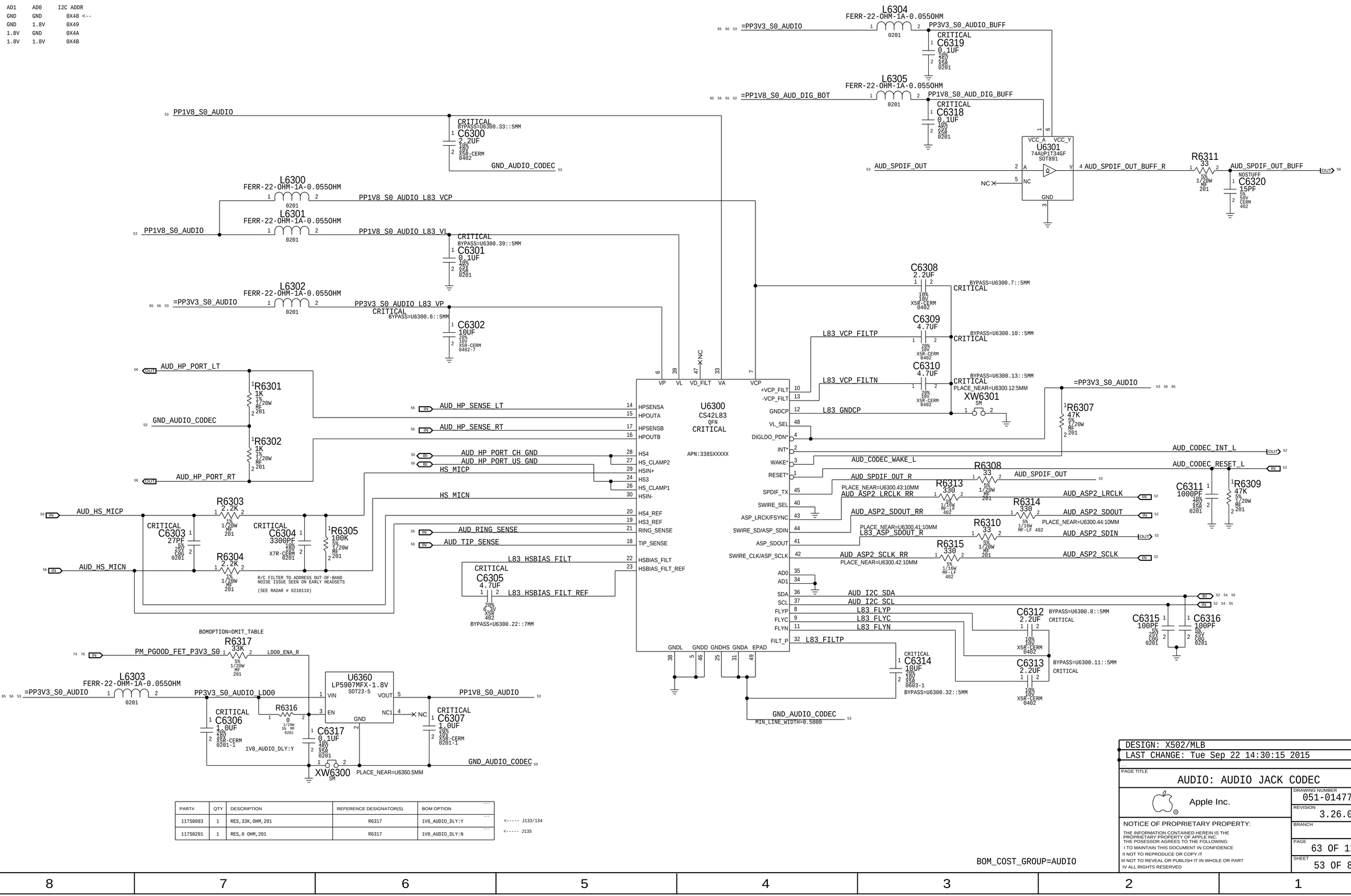
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0083	1	RES,33K,OHM,201	R6317	1V8_AUDIO_DLY:Y	<----- J133/134
117S0201	1	RES,0 OHM,201	R6317	1V8_AUDIO_DLY:N	<----- J135

DESIGN: X502/MLB
LAST CHANGE: Tue Sep 22 14:30:15 2015

PAGE TITLE
AUDIO: AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER 051-01477
SIZE D
REVISION 3.26.0
BRANCH
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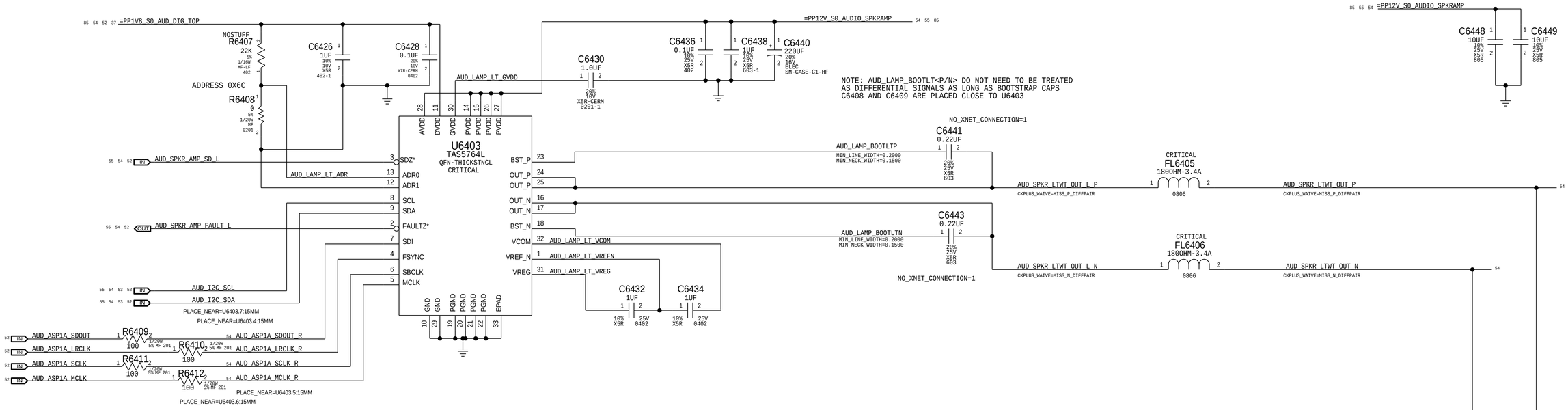
SHEET 53 OF 87

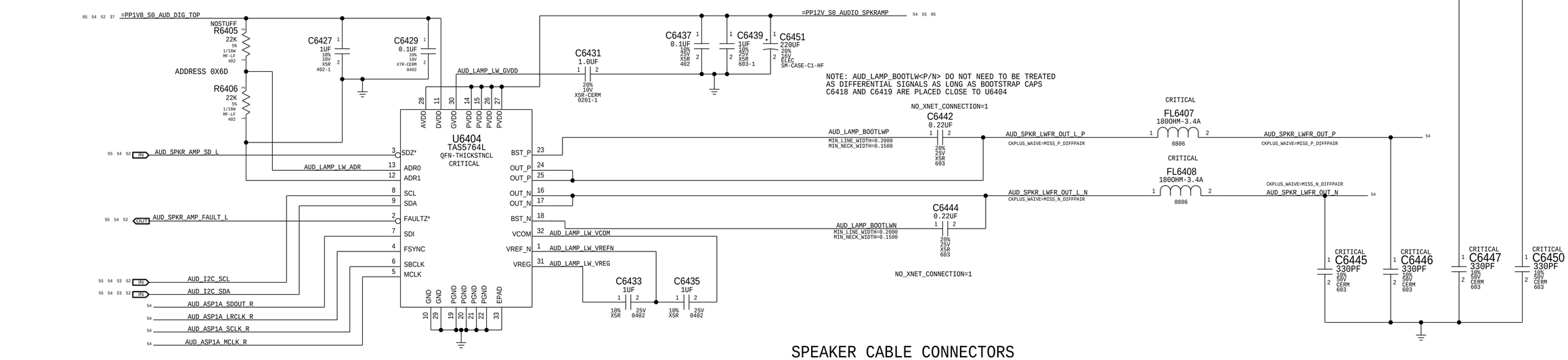
2X MONO SPEAKER AMPLIFIERS (TAS5764L)

APN:353S00875

GAIN = TBD

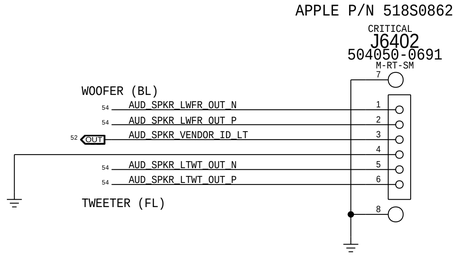
SPEAKER AMPLIFIERS - LEFT CHANNEL





SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE: AUDIO: LEFT SPKR AMP

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

BRANCH:

PAGE: 64 OF 119

SHEET: 54 OF 87

2X MONO SPEAKER AMPLIFIERS (TAS5764L)

APN:353S00875

GAIN = TBD

SPEAKER AMPLIFIERS - RIGHT CHANNEL

=PP1V8_S0_AUD_DIG_BOT

ADDRESS 0X6E

R6501 22K 5% 1/16W MF-LF 402

NOSTUFF R6502 22K 5% 1/16W MF-LF 402

C6501 1UF 10% 10V X5R 402-1

C6503 0.1UF 20% 10V X7R-CERM 0402

=PP12V_S0_AUDIO_SPKRAMP

C6505 1.0UF 20% 10V X5R-CERM 0201-1

C6511 0.1UF 10% 25V X5R 402

C6513 1UF 10% 25V X5R 603-1

C6515 220UF 20% 16V ELEC SM-CASE-C1-HF

AUD_RAMP_RT_GVDD

NOTE: AUD_LAMP_BOOTRT<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6408 AND C6409 ARE PLACED CLOSE TO U6501

U6501 TAS5764L QFN-THICKSTNCL CRITICAL

28	AVDD	BST_P	23
11	DVDD	OUT_P	24
30	GVDD	OUT_P	25
14	PVDD	OUT_N	16
15	PVDD	OUT_N	17
26	PVDD	BST_N	18
27	PVDD	VCOM	32
3	SDZ*	VREF_N	1
13	ADR0	VREG	31
12	ADR1		
8	SCL		
9	SDA		
2	FAULTZ*		
7	SDI		
4	FSYNC		
6	SBCLK		
5	MCLK		
10	GND		
29	GND		
19	PGND		
20	PGND		
21	PGND		
22	PGND		
33	EPAD		

AUD_SPKR_AMP_SD_L

AUD_RAMP_RT_ADR

AUD_SPKR_AMP_FAULT_L

AUD_I2C_SCL

AUD_I2C_SDA

PLACE_NEAR=U6501.7:15MM

PLACE_NEAR=U6501.4:15MM

R6509 100 1/20W 5% MF 201

R6510 100 1/20W 5% MF 201

R6511 100 1/20W 5% MF 201

R6512 100 1/20W 5% MF 201

AUD_ASP1B_SDOUT

AUD_ASP1B_LRCLK

AUD_ASP1B_SCLK

AUD_ASP1B_MCLK

AUD_ASP1B_SDOUT_R

AUD_ASP1B_LRCLK_R

AUD_ASP1B_SCLK_R

AUD_ASP1B_MCLK_R

PLACE_NEAR=U6501.5:15MM

PLACE_NEAR=U6501.6:15MM

C6507 1UF 10% 25V X5R 0402

C6509 1UF 10% 25V X5R 0402

AUD_RAMP_BOOTRTP

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6516 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_RAMP_BOOTRTN

C6518 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_SPKR_RTWT_OUT_L_P

AUD_SPKR_RTWT_OUT_L_N

CKPLUS_WAIVE=MISS_P_DIFFPAIR

CKPLUS_WAIVE=MISS_N_DIFFPAIR

CRITICAL FL6501 180OHM-3.4A 0806

CRITICAL FL6502 180OHM-3.4A 0806

AUD_SPKR_RTWT_OUT_P

AUD_SPKR_RTWT_OUT_N

C6523 10UF 10% 25V X5R 805

C6524 10UF 10% 25V X5R 805

SPEAKER AMPLIFIERS - LEFT CHANNEL

=PP1V8_S0_AUD_DIG_BOT

ADDRESS 0X6F

R6503 0 5% 1/20W MF 0201

NOSTUFF R6504 22K 5% 1/16W MF-LF 402

C6502 1UF 10% 10V X5R 402-1

C6504 0.1UF 20% 10V X7R-CERM 0402

=PP12V_S0_AUDIO_SPKRAMP

C6506 1.0UF 20% 10V X5R-CERM 0201-1

C6512 0.1UF 10% 25V X5R 402

C6514 1UF 10% 25V X5R 603-1

C6526 220UF 20% 16V ELEC SM-CASE-C1-HF

AUD_RAMP_RW_GVDD

NOTE: AUD_LAMP_BOOTRW<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6418 AND C6419 ARE PLACED CLOSE TO U6502

U6502 TAS5764L QFN-THICKSTNCL CRITICAL

28	AVDD	BST_P	23
11	DVDD	OUT_P	24
30	GVDD	OUT_P	25
14	PVDD	OUT_N	16
15	PVDD	OUT_N	17
26	PVDD	BST_N	18
27	PVDD	VCOM	32
3	SDZ*	VREF_N	1
13	ADR0	VREG	31
12	ADR1		
8	SCL		
9	SDA		
2	FAULTZ*		
7	SDI		
4	FSYNC		
6	SBCLK		
5	MCLK		
10	GND		
29	GND		
19	PGND		
20	PGND		
21	PGND		
22	PGND		
33	EPAD		

AUD_SPKR_AMP_SD_L

AUD_RAMP_RW_ADR

AUD_SPKR_AMP_FAULT_L

AUD_I2C_SCL

AUD_I2C_SDA

AUD_ASP1B_SDOUT_R

AUD_ASP1B_LRCLK_R

AUD_ASP1B_SCLK_R

AUD_ASP1B_MCLK_R

C6508 1UF 10% 25V X5R 0402

C6510 1UF 10% 25V X5R 0402

AUD_RAMP_BOOTRWP

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6517 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_RAMP_BOOTRWN

C6519 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_SPKR_RWFR_OUT_L_P

AUD_SPKR_RWFR_OUT_L_N

CKPLUS_WAIVE=MISS_P_DIFFPAIR

CKPLUS_WAIVE=MISS_N_DIFFPAIR

CRITICAL FL6503 180OHM-3.4A 0806

CRITICAL FL6504 180OHM-3.4A 0806

AUD_SPKR_RWFR_OUT_P

AUD_SPKR_RWFR_OUT_N

CRITICAL C6520 330PF 10% 50V CERM 603

CRITICAL C6521 330PF 10% 50V CERM 603

CRITICAL C6522 330PF 10% 50V CERM 603

CRITICAL C6525 330PF 10% 50V CERM 603

SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862

CRITICAL J6502 504050-0691 M-RT-SM

WOOFER (BR)

1	AUD_SPKR_RWFR_OUT_N
2	AUD_SPKR_RWFR_OUT_P
3	AUD_SPKR_VENDOR_ID_RT
4	
5	AUD_SPKR_RTWT_OUT_N
6	AUD_SPKR_RTWT_OUT_P

TWEETER (FR)

7, 8

BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE: AUDIO: RIGHT SPKR AMP

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SIZE D

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BRANCH

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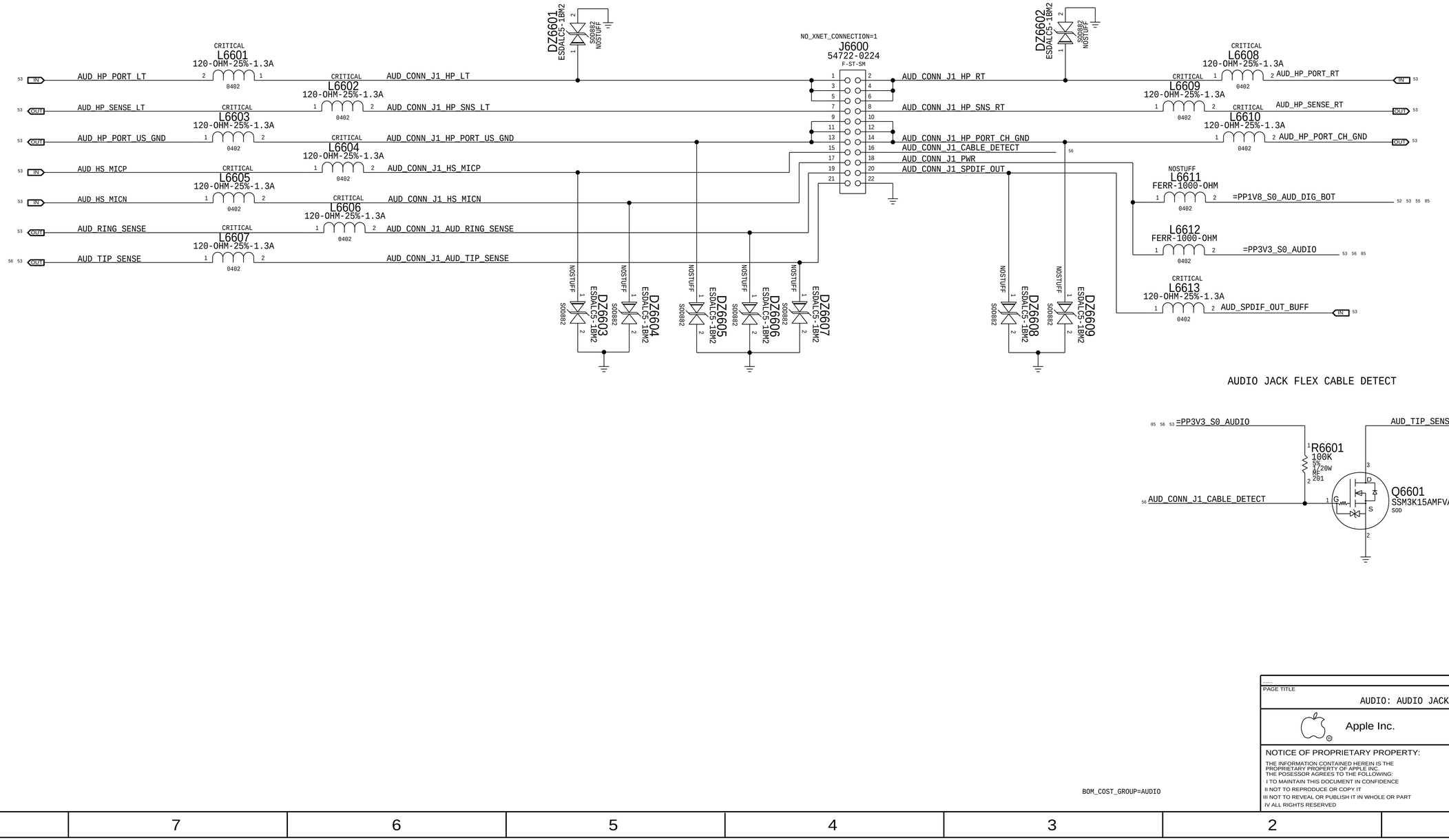

PAGE TITLE

AUDIO: AUDIO JACK CONN

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SYNC_MASTER:1135 SYNC_DATE:04/04/2007

PAGE TITLE

AUDIO: EMPTY

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

SYNC_MASTER=1135 SYNC_DATE=04/04/2013

PAGE TITLE

AUDIO: EMPTY

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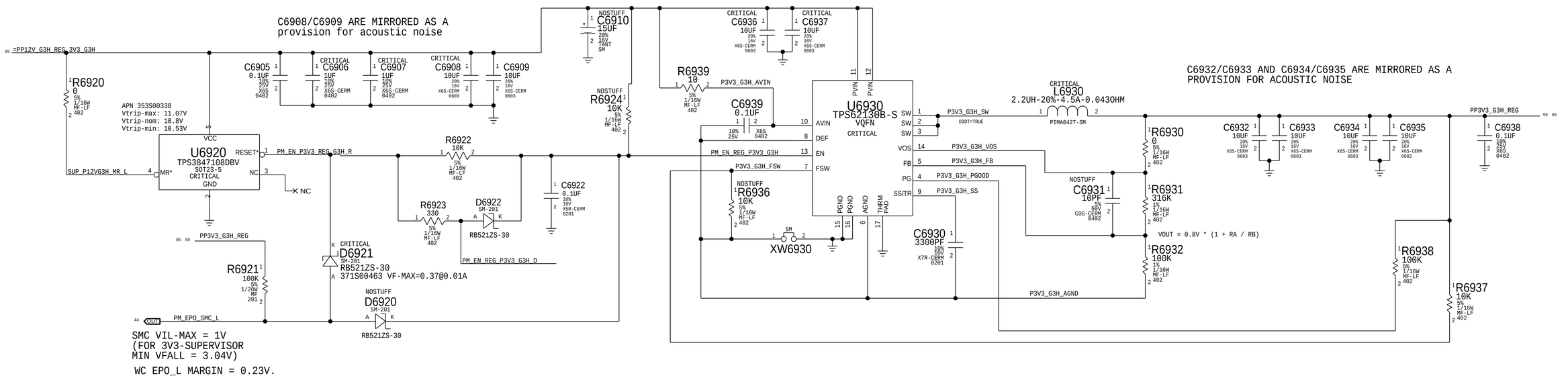
3.3V "G3HOT" REGULATOR

1.25MHZ SWITCHING FREQ

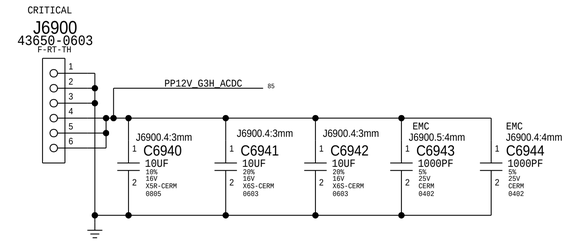
C6936/C6937 ARE MIRRORED AS A provision for acoustic noise

C6908/C6909 ARE MIRRORED AS A provision for acoustic noise

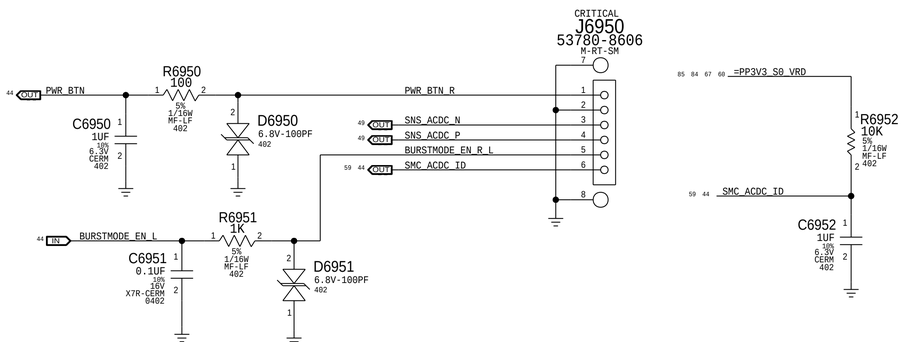
C6932/C6933 AND C6934/C6935 ARE MIRRORED AS A PROVISION FOR ACOUSTIC NOISE



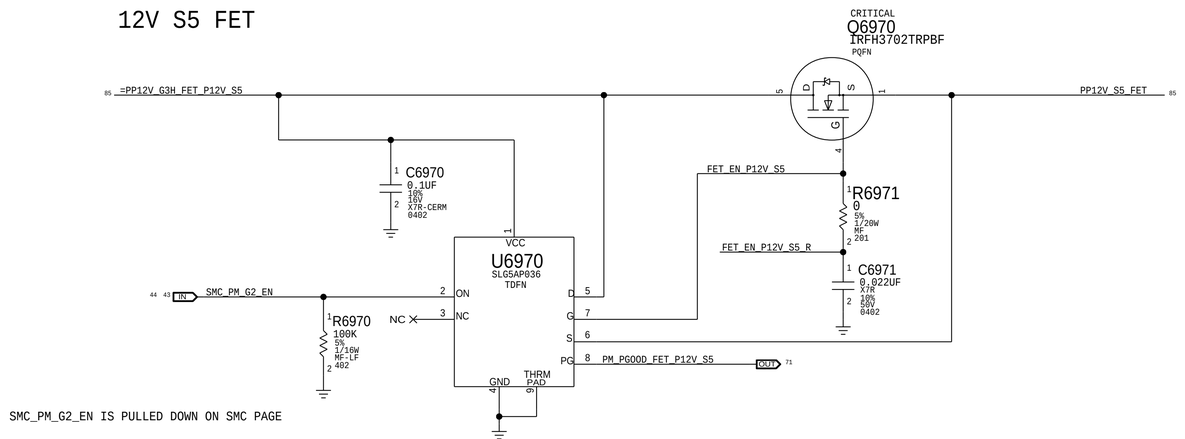
MLB to AC-DC Connector



MLB to AC-DC Supplemental Signal Connector



12V S5 FET



SMC_PM_G2_EN IS PULLED DOWN ON SMC PAGE

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	Connectors / VReg G3Hot
Apple Inc.	DRAWING NUMBER 051-01477 SIZE D
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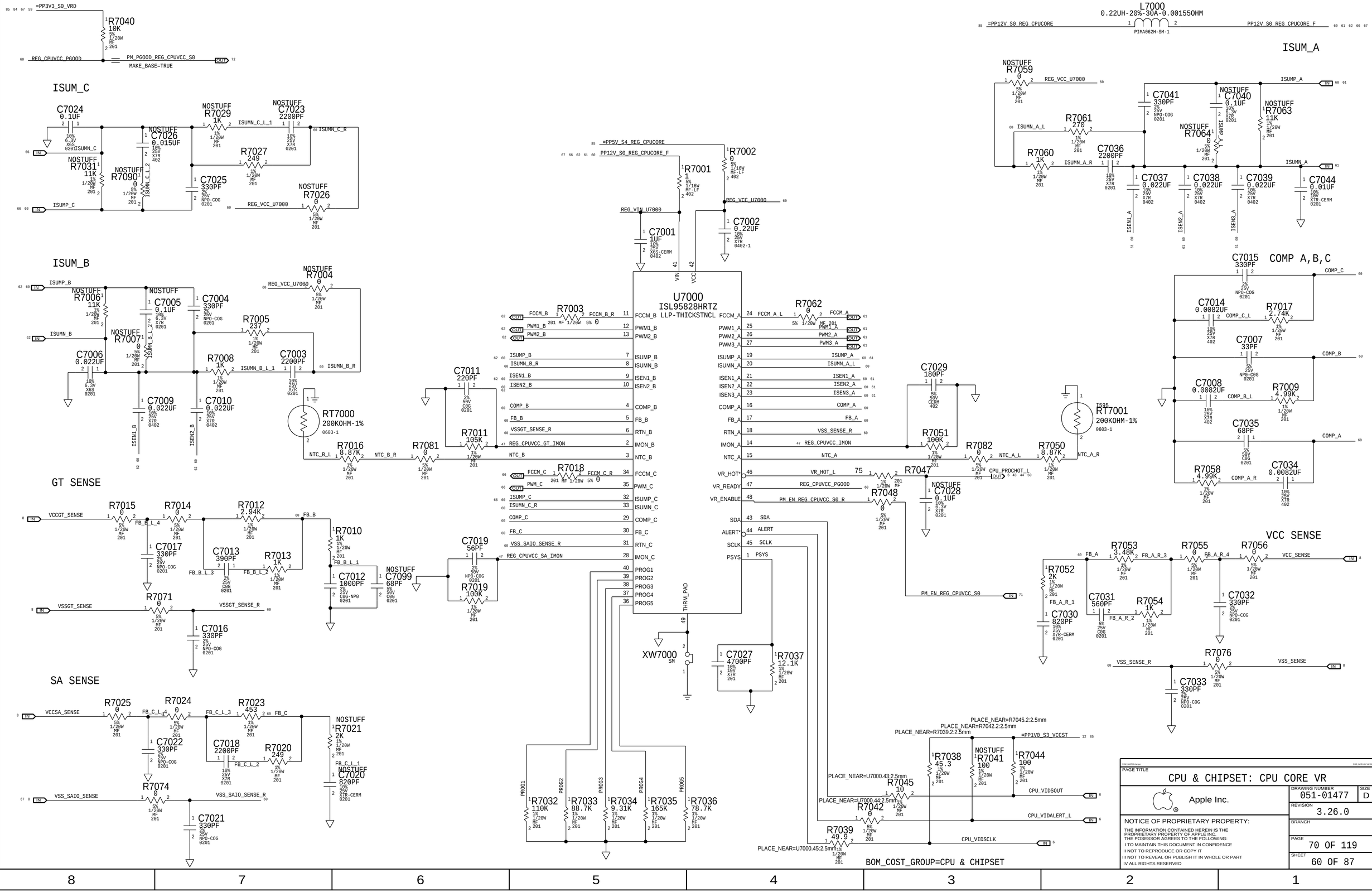

PAGE TITLE

CPU & CHIPSET: CPU CORE VR

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CPU VCC Regulator
EDC = 79A
TDC = 61A

CPU VCORE Phase 1

CPU VCORE Phase 2

CPU Phase 3

CPU VCORE OUTPUT DECOUPLING

BOM_COST_GROUP=CPU & CHIPSET

DRAWING	LAST_MODIFIED=Wed Sep 14 23:01:32 2016
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCC)
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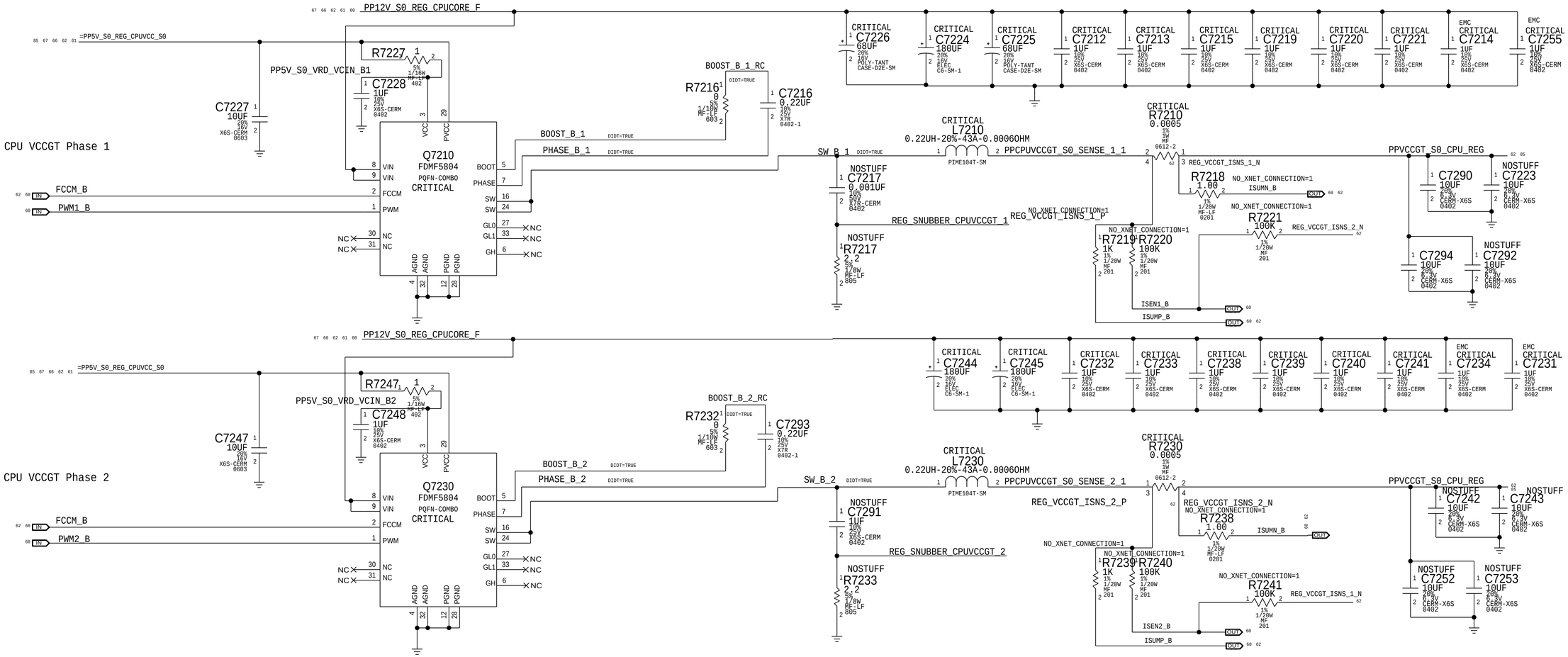
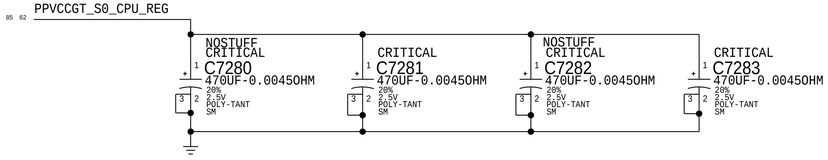
CPU VCCGT Regulator

EDC = 45A

TDC = 30A



CPU VCCGT OUTPUT DECOUPLING



BOM_COST_GROUP=CPU & CHIPSET

DRAWING	LAST_MODIFIED=Wed Sep 14 23:01:32 2016
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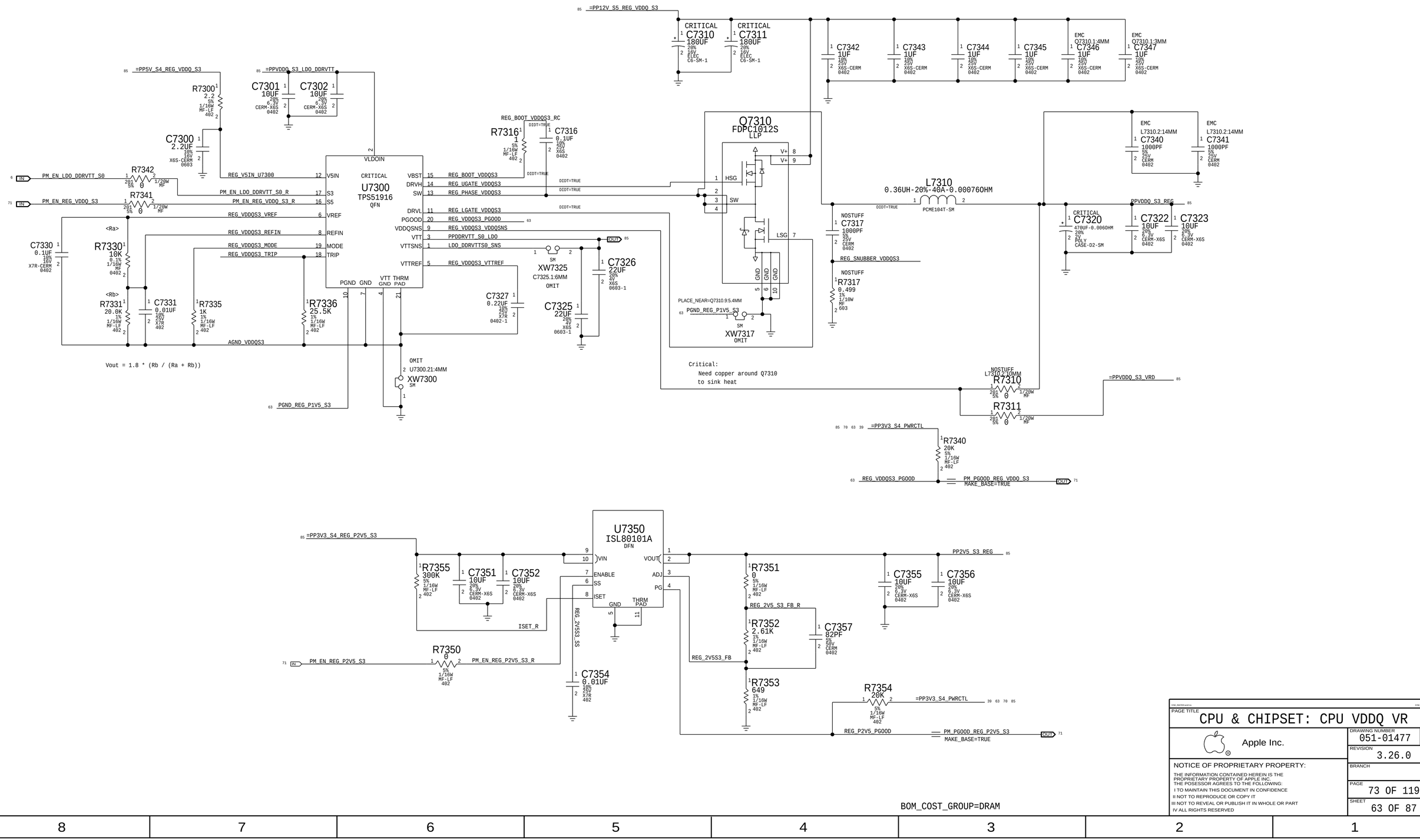
VDDQ S3 REGULATOR



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3.3V S5 Regulator

Switching freq: 356 kHz = 1 / (170 E-12 * R7633)

5V S4 Regulator

OC trip point: 31.25 A = R7658 * 10 E-6 / DCR(L7650)

Switching freq: 356 kHz = 1 / (170 E-12 * R7673)

=PP12V_S5_REG_P3V3_S5_P5V_S4

C7610 CRITICAL 180UF 20% 16V ELEC C6-SM-1

C7650 CRITICAL 180UF 20% 16V ELEC C6-SM-1

C7651 CRITICAL 180UF 20% 16V ELEC C6-SM-1

R7603 1 5% 1/16W MF-LF 402 2

REG_VIN_U7600

C7640 EMC L7610.1:8MM 1000PF 5% 25V CERM 0402

C7641 EMC L7610.1:8MM 1000PF 5% 25V CERM 0402

C7642 EMC CRITICAL Q7610.1:4.2MM 1UF 10% 25V X6S-CERM 0402

C7643 EMC CRITICAL Q7610.1:3MM 1UF 10% 25V X6S-CERM 0402

C7682 EMC CRITICAL Q7650.1:5MM 1UF 10% 25V X6S-CERM 0402

C7683 EMC CRITICAL Q7650.1:5MM 1UF 10% 25V X6S-CERM 0402

PP3V3_S5_REG

C7621 CRITICAL 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7620 CRITICAL 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

R7690 CRITICAL 0.005 1% 1W MF 0612-5

L7610 CRITICAL 1.0UH-20A-2.64M-OHM PIMB103E-SM-1

PP3V3_S5_REG_R

PP5V_S5_LDO

C7601 4.7UF 20% 6.3V CERM 603

R7602 2.2 5% 1/16W MF-LF 402

C7602 1UF 10% 25V X6S-CERM 0402

C7603 1UF 10% 25V X6S-CERM 0402

C7600 1UF 10% 25V X6S-CERM 0402

REG_VCC2_U7600

REG_VCC1_U7600

Q7610 FDPC1012S LLP

DIDT=TRUE

REG_BOOT_P3V3S5_RC

C7616 0.1UF 10% 25V X6S 0402

R7616 2.2 5% 1/16W MF-LF 402

HSG

SW

LSG

GND

C7617 NOSTUFF 0.001UF 10% 50V CERM 402

REG_LGATE_P3V3S5_R

R7610 0 5% 1/10W MF-LF 603

U7600 ISL62383CRTZ QFN CRITICAL

REG_P3V3S5_PGOOD	7 PGOOD1	PGOOD2 1	REG_P5VS4_PGOOD
REG_UGATE_P3V3S5	14 UGATE1	UGATE2 22	REG_UGATE_P5VS4
REG_BOOT_P3V3S5	15 BOOT1	BOOT2 21	REG_BOOT_P5VS4
REG_PHASE_P3V3S5	13 PHASE1	PHASE2 23	REG_PHASE_P5VS4
REG_LGATE_P3V3S5	16 LGATE1	LGATE2 20	REG_LGATE_P5VS4
REG_P3V3S5_ISEN	10 ISEN1	ISEN2 26	REG_P5VS4_ISEN
REG_P3V3S5_OCSET	11 OCSET1	OCSET2 25	REG_P5VS4_OCSET
REG_P3V3S5_VOUT	9 VOUT1	VOUT2 27	REG_P5VS4_VOUT
REG_P3V3S5_FB	8 FB1	FB2 28	REG_P5VS4_FB
REG_P3V3S5_FSET	6 FSET1	FSET2 2	REG_P5VS4_FSET
	12 EN1	EN2 24	
	18 LDO5	VIN 17	
	VCC1 5	VCC2 4	
	FCCM 3	NC	
	THRM PAD 29	PGND 19	

Q7650 FDPC1012S LLP

REG_BOOT_P5VS4_RC

R7656 2.2 5% 1/16W MF-LF 402

C7656 0.1UF 10% 25V X6S 0402

REG_LGATE_P5VS4_R

R7650 0 5% 1/10W MF-LF 603

C7657 NOSTUFF 0.001UF 10% 50V X7R-CERM 0402

R7657 NOSTUFF 0.499 1% 1/10W MF 603

REG_SNUBBER_P5VS4

L7650 CRITICAL 1.0UH-20A-2.64M-OHM PIMB103E-SM-1

PP5V_S4_REG

XW7650 OMIT SM NO_XNET_CONNECTION=1

XW7651 OMIT SM NO_XNET_CONNECTION=1

REG_P5VS4_PHASE_SNS_P

REG_P5VS4_PHASE_SNS_N

R7658 8.25K 1% 1/16W MF-LF 402

C7658 0.047UF 10% 16V X7R-CERM 0402

R7659 8.25K 1% 1/16W MF-LF 402

R7665 0 5% 1/16W MF-LF 402

C7660 CRITICAL 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7661 CRITICAL 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7680 EMC L7650.2:5MM 1000PF 5% 25V CERM 0402

C7681 EMC L7650.2:5MM 1000PF 5% 25V CERM 0402

C7663 NOSTUFF 10UF 20% 10V X5R-CERM 0402-1

C7664 NOSTUFF 10UF 20% 10V X5R-CERM 0402-1

C7663/C7664 are mirrored as a provision for acoustic noise

SNS_P3V3S5_P

SNS_P3V3S5_N

XW7610 OMIT SM NO_XNET_CONNECTION=1

XW7611 OMIT SM NO_XNET_CONNECTION=1

REG_P3V3S5_SNS_P

REG_P3V3S5_SNS_N

C7618 0.082UF 10% 16V CERM-X7R 402

R7618 6.81K 1% 1/16W MF-LF 402

R7619 6.81K 1% 1/16W MF-LF 402

REG_SNUBBER_P3V3S5

R7617 0.499 1% 1/10W MF 603 NOSTUFF

R7666 0 5% 1/16W MF-LF 402

(reg_p3v3s4_isen)

(reg_p3v3s4_ocset)

(reg_p3v3s4_vout)

(reg_p5vs4_isen)

(reg_p5vs4_ocset)

(reg_p5vs4_vout)

Vout = 0.6 * (1 + Ra / Rb)

<Ra> R7630 45.3K 1% 1/16W MF-LF 402

<Rb> R7631 10K 0.1% 1/16W MF 0402

R7632 976 1% 1/16W MF-LF 402

C7632 1000PF 5% 25V CERM 0402

REG_P3V3S5_VOUT_R

Vout = 0.6*(1+Ra/Rb)

C7633 0.01UF 10% 16V X7R-CERM 0402

R7633 16.5K 1% 1/16W MF-LF 402

PM_EN_REG_P3V3_S5_R

R7688 0 5% 1/16W MF-LF 402

PM_EN_REG_P3V3_S5

PM_EN_REG_P5V_S4

R7689 0 5% 1/16W MF-LF 402

PM_EN_REG_P5V_S4_R

C7673 0.01UF 10% 16V X7R-CERM 0402

R7673 16.5K 1% 1/16W MF-LF 402

R7672 976 1% 1/16W MF-LF 402

C7672 1000PF 5% 25V CERM 0402

REG_P5VS4_VOUT_R

R7670 75K 1% 1/16W MF-LF 402

R7671 10K 0.1% 1/16W MF 0402

Vout = 0.6 * (1 + Ra / Rb)

=PP3V3_S5_VRD

R7680 20K 5% 1/16W MF-LF 402

REG_P5VS4_PGOOD

PM_PGOOD_REG_P5V_S4 MAKE_BASE=TRUE

R7640 20K 5% 1/16W MF-LF 402

REG_P3V3S5_PGOOD

PM_PGOOD_REG_P3V3_S5 MAKE_BASE=TRUE

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: VReg 3.3V S5/5V S4

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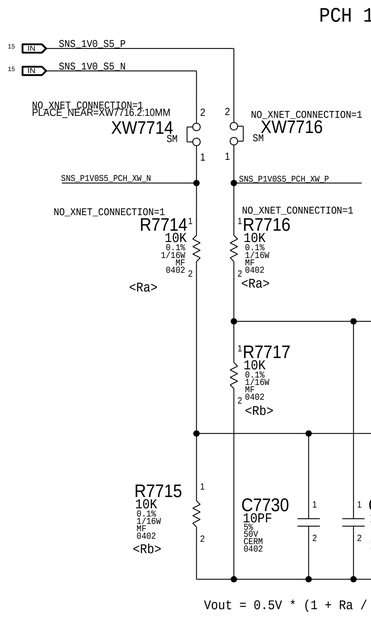
PCH 1V0 SUPPLY



PAGE TITLE	CPU & CHIPSET: PCH 1V0 VR
Apple Inc.	DRAWING NUMBER 051-01477 · SIZE D
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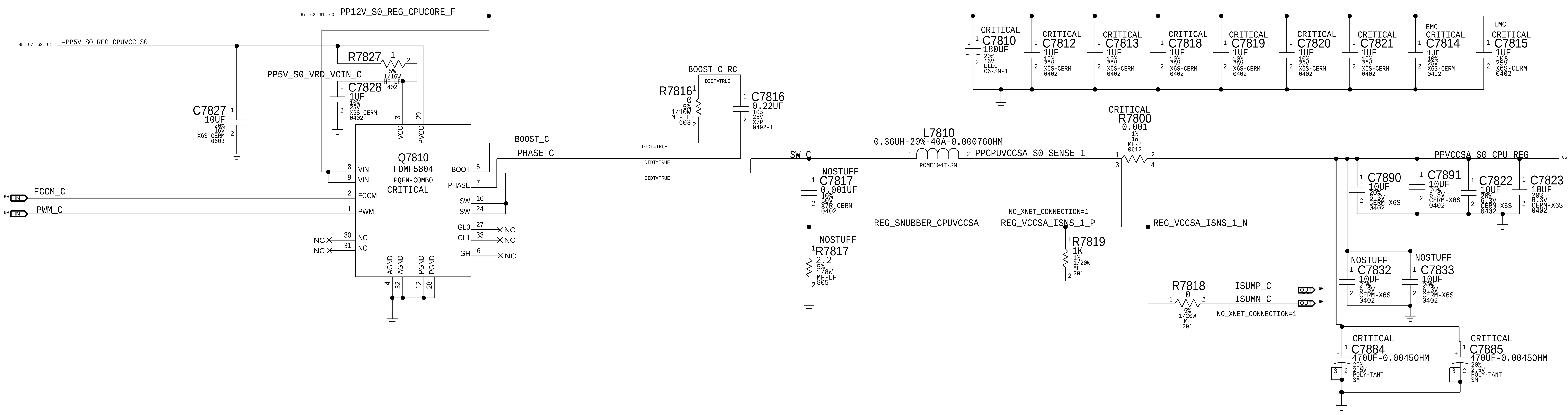
CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A



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LAST_MODIFIED=Wed Sep 14 23:01:33 2016

PAGE TITLE

CPU & CHIPSET: CPU CORE VR (VCCSA)

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

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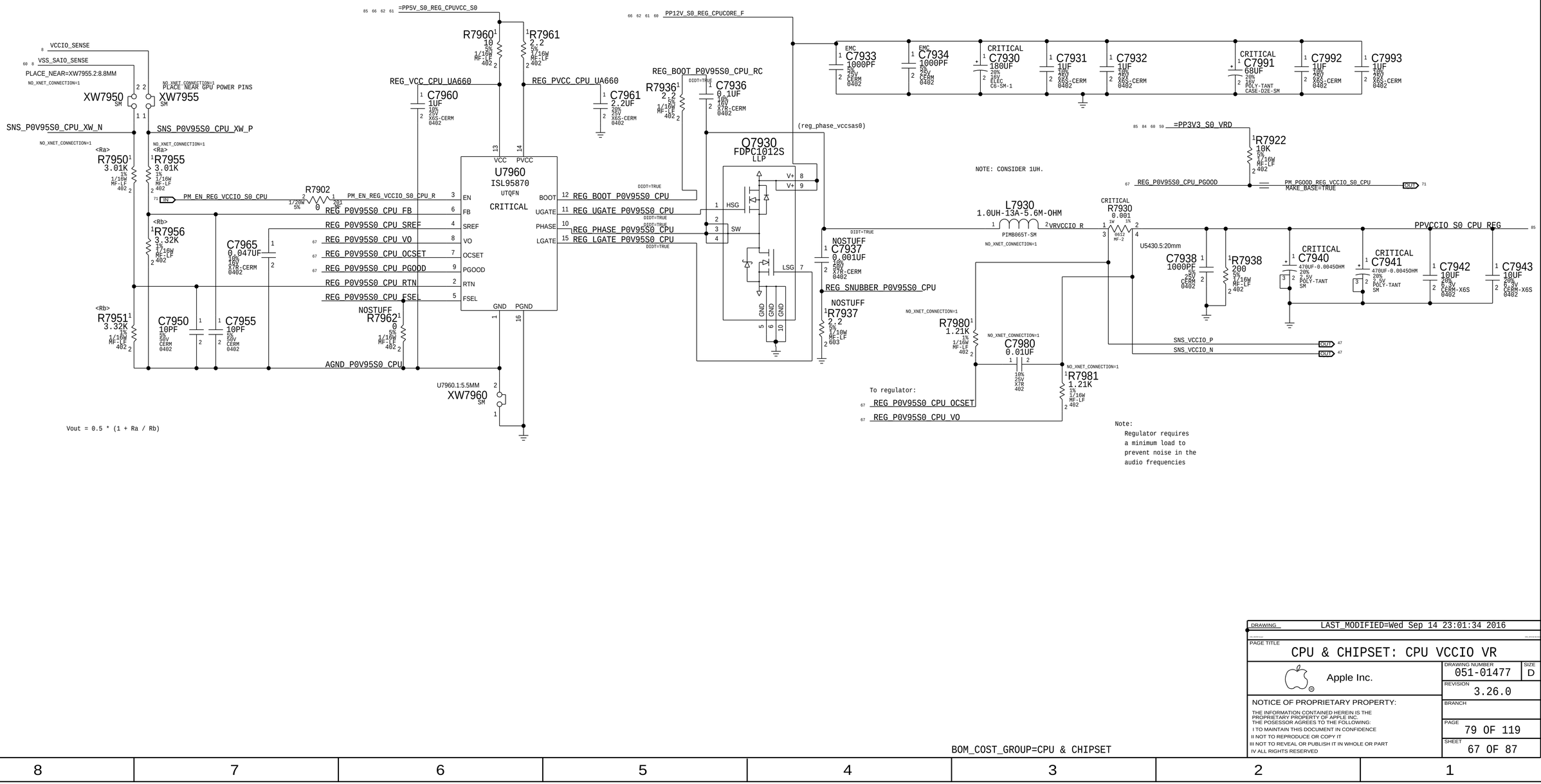
BOM_COST_GROUP=CPU & CHIPSET

VCCIO S0 REGULATOR



BOM_COST_GROUP=CPU & CHIPSET

DRAWING	LAST_MODIFIED=Wed Sep 14 23:01:34 2016
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OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

PP12V_S0_BKLT_PWR
D8103 SOD-323 SBR130S3
C8140 1000PF 5% 25V CERM 0402
C8141 1000PF 5% 25V CERM 0402
C8102 10UF 10% 25V X7R-CERM 1206-1 CRITICAL
C8103 10UF 10% 25V X7R-CERM 1206-1 CRITICAL
C8114 100UF 20% 35V ELEC 6.3X11-TH CRITICAL
PLACE C8114 NEAR HIGHER FREQUENCY CAPS

OMIT_TABLE
L8100 33UH-20%-10A-0.0351OHM
IHLP6767GZ-IHLP4040DZ11-SM

BKLT_PHASE
D8101 POWERDI5-TO277A PDS5100H
NOSTUFF R8123 4.7 5% 1/10W MF-LF 603
BKLT_SNUBBER
NOSTUFF C8113 100PF 5% 100V C0G-CERM 0603

Q8120 FDMC86102LZ MLP-3.3X3.3-PWRPK-12128-COMBO
BKLT_GATE_R

C8119 100PF 5% 100V C0G-CERM 0603
C8106 2.2UF 10% 100V X7S-CERM 1206
C8108 2.2UF 10% 100V X7S-CERM 1206
C8109 15UF 20% 100V ELEC TH-COMBO OMIT_TABLE CRITICAL
C8118 15UF 20% 100V ELEC TH-COMBO OMIT_TABLE CRITICAL
C8120 100PF 5% 100V C0G-CERM 0603
BKLT_BOOST

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1078	138S0810		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0648	371S0694		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211 TO Q8216	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR
126-00012	126-0306		C8114	BLC INPUT CAP
376S1184	376S1183		Q8120	BLC POWER FET

PP3V3_S0_BKLT_VDDIO
PP5V_S0_BKLT_VDDD
PP5V_S0_BKLT_VDDA
PP12V_S0_BKLT_FILT

R8119 30.1 1% 1/8W MF-LF 805
BKLT_SNSP_R
R8102 0.03 1% 2W MF 2512-LF
BKLT_SNSN_R
R8114 20 5% 1/8W MF-LF 805
R8104 887K 1% 1/16W MF-LF 402
R8103 330K 1% 1/8W MF 0402
C8111 1000PF 10% 100V X7R-CERM 0603
BKLT_BST_FB_R
R8113 887K 1% 1/16W MF-LF 402
C8110 1000PF 10% 100V X7R-CERM 0603
R8112 330K 1% 1/8W MF 0402
XW8109 SHORT-1206 BKLT_SNSN_R

U8100 LP8565A13RWC WQFN-THICKSTNCL OMIT_TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
126-00013	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	
353S01125	1	IC,P8565A128,LED BCKLGHT CTRL,7X7 QFN56	U8100	CRITICAL	

BKLT_SHUTDOWN	39	SD	
	40	UVLO_OVP	
=I2C_BKLT_SDA	9	SDA	IN
=I2C_BKLT_SCL	8	SCL	IN
DP_INT_EG_ML_HPD_BUF_R	2	HPD	
TCON_BLC_EN	3	BL_EN	IN
BKLT_FAULT_INT_R_L	12	INT	
BLC_VSYNC_R	10	BRT_SYNC	
BKLT_PWM_IN	7	PWM	
BLC_LSYNC_R	11	SYNC	
BKLT_PLL_FILT	43	FILTER	
BKLT_ANG_TEST	32	ANALOG_TEST	
BKLT_DIG_TEST	1	DIGITAL_TEST	
PP12V_S0_BKLT_PWR_R	38	VING	
BKLT_GD_RAIL	37	BST_GD_RAIL	
BKLT_NC_TEST	13	NC	

BST_GD	36	BKLT_GATE	
BST_ISENSE_P	34	BKLT_SNSP	
BST_ISENSE_N	33	BKLT_SNSN	
BST_FB	31	BKLT_BST_FB	
BST_SHORT_FB	30	BKLT_BST_SHORT_FB	
LED1_HDR	14	BKLT_VSEN1	
LED1_GD	15	BKLT_GD1	OUT
LED1_R	16	BKLT_ISEN1_Q	IN
LED2_HDR	17	BKLT_VSEN2	
LED2_GD	18	BKLT_GD2	OUT
LED2_R	19	BKLT_ISEN2_Q	IN
LED3_HDR	20	BKLT_VSEN3	
LED3_GD	21	BKLT_GD3	OUT
LED3_R	22	BKLT_ISEN3_Q	IN
LED4_HDR	24	NC	
LED4_GD	25	NC	
LED4_R	26	NC	
LED5_HDR	29	NC	
LED5_GD	27	NC	
LED5_R	28	NC	
LED6_HDR	44	NC	
LED6_GD	45	NC	
LED6_R	46	NC	
LED7_HDR	47	BKLT_VSEN4	
LED7_GD	48	BKLT_GD4	OUT
LED7_R	49	BKLT_ISEN4_Q	IN
LED8_HDR	51	BKLT_VSEN5	
LED8_GD	52	BKLT_GD5	OUT
LED8_R	53	BKLT_ISEN5_Q	IN
LED9_HDR	54	BKLT_VSEN6	
LED9_GD	55	BKLT_GD6	OUT
LED9_R	56	BKLT_ISEN6_Q	IN

GNDA	41		
GNDD	6		
LED_GND1	23		
LED_GND2	50		
GND_BST_GD	35		
THRM PAD	57		

BKLT_PLL_FILT
C8115 330PF 5% 50V NPO-C0G-CERM 0402
R8111 270K 5% 1/16W MF-LF 402
NOSTUFF D8102 SOD-523 BAT54XV2T1
BKLT_PLL_FILT_R
C8116 4700PF 10% 25V X7R-CERM 0402
BKLT_GNDA

BKLT_GD_RAIL
C8145 0.1UF 10% 25V X6S 0402 NOSTUFF
C8117 0.1UF 10% 25V X6S 0402
BKLT_GND_BST_GD

R8138 1 5% 1/16W MF-LF 402
PP12V_S0_BKLT_PWR
PP12V_S0_BKLT_PWR_R
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8142 1UF 10% 25V X7R 0603
C8143 0.01UF 10% 16V X7R-CERM 0402
C8144 0.1UF 10% 16V X7R-CERM 0402
BKLT_GND_BST_GD

XW8105 BKLT_GNDA
XW8106 BKLT_GNDD

R8137 1 5% 1/16W MF-LF 402
=PP5V_S0_BKLT
PP5V_S0_BKLT_VDDA
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8137 22UF 20% 10V X5R-CERM 0603
C8138 0.01UF 10% 16V X7R-CERM 0402
C8139 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDA

R8131 1 5% 1/16W MF-LF 402
=PP5V_S0_BKLT
PP5V_S0_BKLT_VDDD
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8131 22UF 20% 10V X5R-CERM 0603
C8132 0.01UF 10% 16V X7R-CERM 0402
C8133 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

R8134 1 5% 1/16W MF-LF 402
=PP3V3_S0_BKLT
PP3V3_S0_BKLT_VDDIO
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8134 1UF 10% 25V X7R 0603
C8135 0.01UF 10% 16V X7R-CERM 0402
C8136 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

XW8108 BKLT_GND_BST_GD

R8172 0 5% 1/16W MF-LF 402
BKLT_FAULT_INT_R_L
=PP3V3_S0_BKLT
R8124 4.7K 5%
BKLT_FAULT_INT_L

R8106 200K 1% DP_INT_EG_ML_HPD_BUF_R
R8105 100K 5% TCON_BLC_EN
R8107 10K 5% BKLT_PWM_IN
R8121 10K 5% BLC_VSYNC_R
R8120 10K 5% NOSTUFF BLC_LSYNC_R
BKLT_GNDD

R8173 0 5% 402 DP_INT_EG_ML_HPD_BUF
R8170 NOSTUFF 0 5% 402 BLC_VSYNC
R8171 0 5% 402 BLC_LSYNC

R8180 10K 5% BKLT_ANG_TEST
R8181 10K 5% BKLT_DIG_TEST
R8182 10K 5% BKLT_NC_TEST
BKLT_GNDA

R8125 0 5% 1/16W MF-LF 402
BKLT_SNSP — BKLT_SNSP_R
C8130 1000PF 10% 100V X7R 603 NO_XNET_CONNECTION=1 NOSTUFF
R8191 0 5% 1/10W MF-LF 402
BKLT_SNSN — BKLT_SNSN_R

F8100 6AMP-32V 0603-1
=PP12V_S0_BKLT — PP12V_BKLT_SNS
R8132 CRITICAL 0.005 1% 1/4W MF 1206-1
PP12V_BKLT_FUSED
FB8108 CRITICAL 160-OHM-6A 1206
PP12V_S0_BKLT_FILT
C8171 NOSTUFF 0.1UF 10% 25V X6S 0402
R8101 NOSTUFF 330K 1% 1/8W MF 0402
Q8119 FDMS6681Z POWER56
C8101 0.01UF 10% 16V X7R-CERM 0402
PP12V_S0_BKLT_PWR
BKLT_EN_DIV

Q8101 SSM3K15AMFVAP SOD NOSTUFF
BKLT_EN_L
R8133 NOSTUFF 147K 1% 1/16W MF-LF 402
R8122 0 5% 1/16W MF-LF 402
TCON_BLC_EN
BKLT_SHUTDOWN

BKLT_BOOST
C8121 470PF 5% 100V CER-C0G 0603
C8122 470PF 5% 100V CER-C0G 0603
C8123 470PF 5% 100V CER-C0G 0603
C8124 470PF 5% 100V CER-C0G 0603
C8125 470PF 5% 100V CER-C0G 0603
C8126 470PF 5% 100V CER-C0G 0603
LED_RETURN_1_FB
LED_RETURN_2_FB
LED_RETURN_3_FB
LED_RETURN_4_FB
LED_RETURN_5_FB
LED_RETURN_6_FB

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=hurtadot SYNC_DATE=12/15/2015
PAGE TITLE: LCD Backlight Driver 1
Apple Inc.
DRAWING NUMBER: 051-01477 SIZE: D
REVISION: 3.26.0
BRANCH:
PAGE: 81 OF 119
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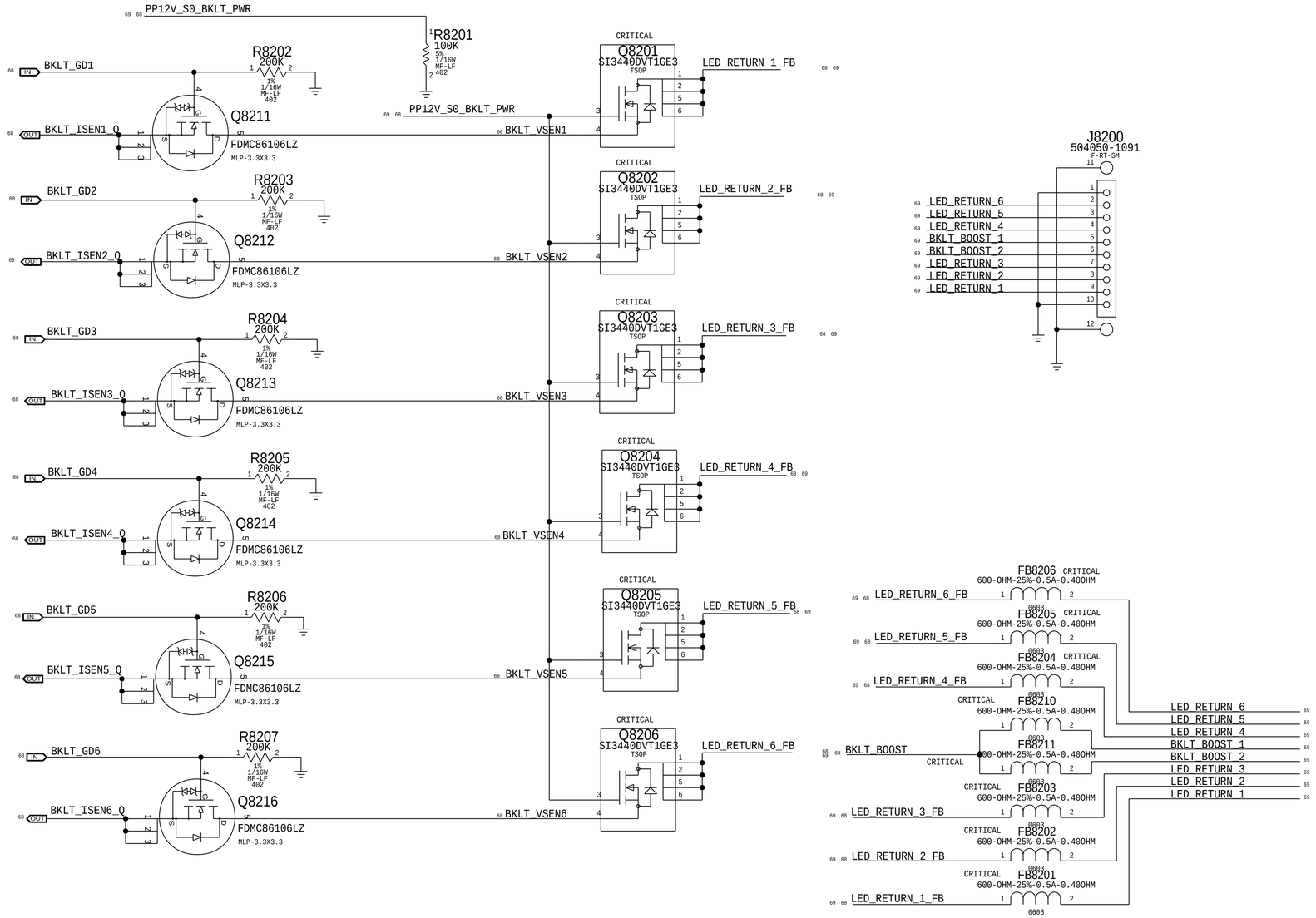
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



BOM_COST_GROUP=DISPLAY

SYNC_MASTER=J94_JINGDONG SYNC_DATE=08/21/2014

PAGE TITLE: LCD Backlight Driver 2

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

BRANCH:

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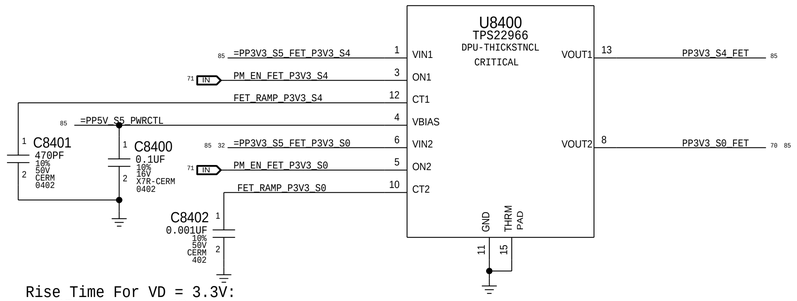
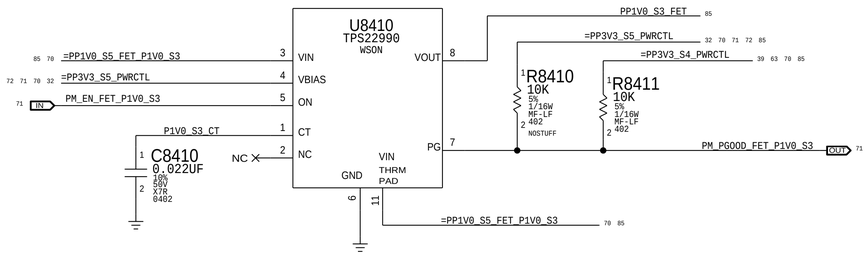
3.3V S4/S0 FET

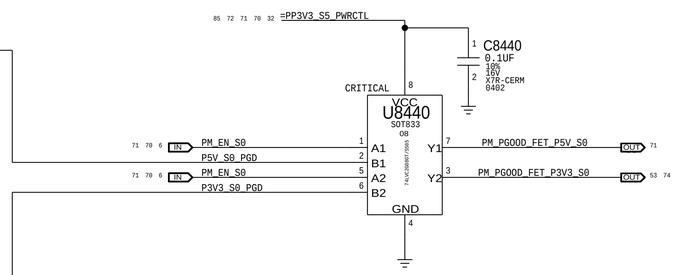


Rise Time For VD = 3.3V:
470 pF -- 603 us
1000 pF -- 1185 us

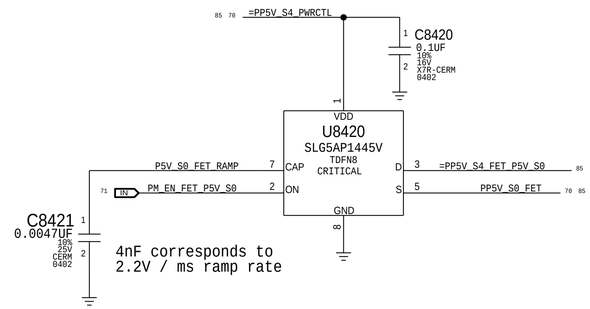
1.0V S3 FET



5V / 3V3 S0 PGOODs

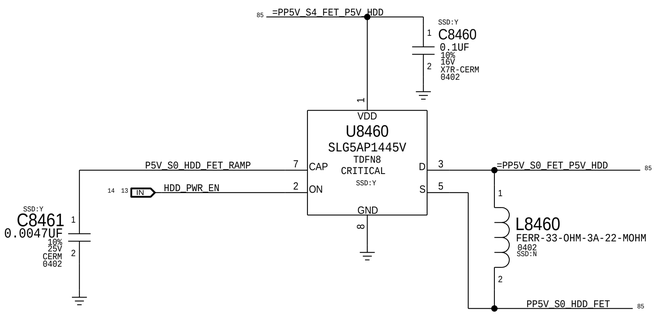


5V S0 FET

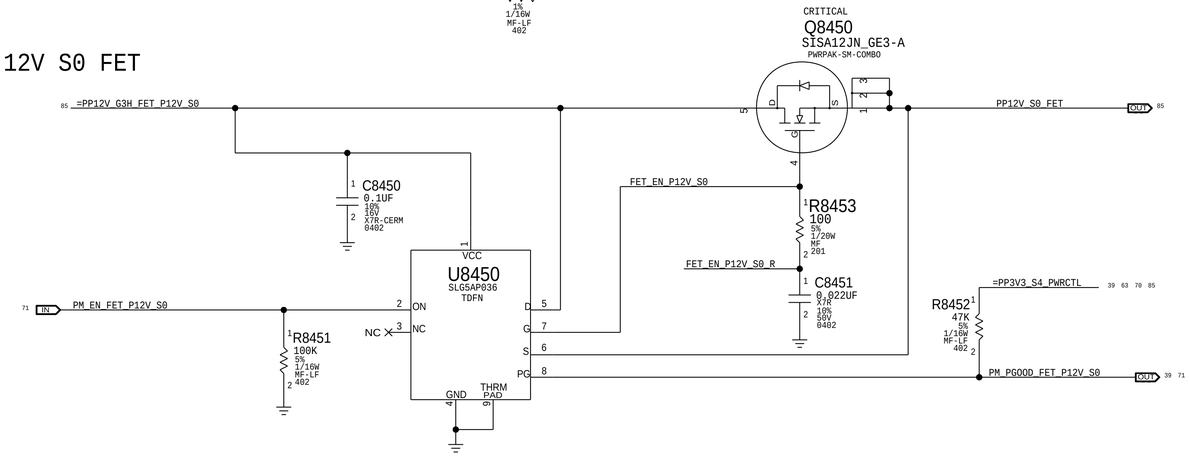


4nF corresponds to
2.2V / ms ramp rate

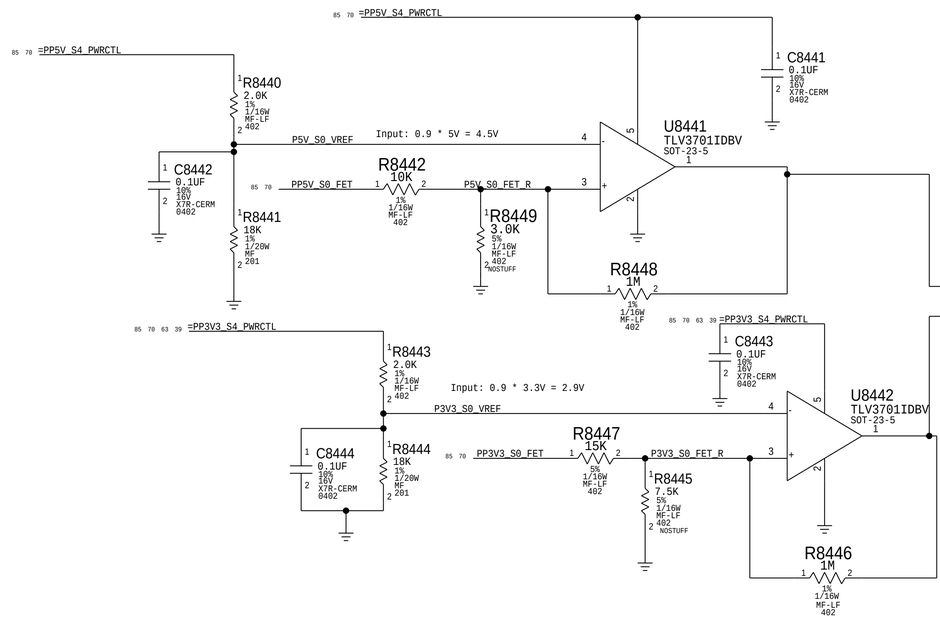
5V HDD FET



12V S0 FET



Input: 0.9 * 5V = 4.5V



Input: 0.9 * 3.3V = 2.9V

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=david	SYNC_DATE=09/01/2016
PAGE TITLE	PM FETs/LDOs
Apple Inc.	DRAWING NUMBER 051-01477 · SIZE D
	REVISION 3.26.0
	BRANCH
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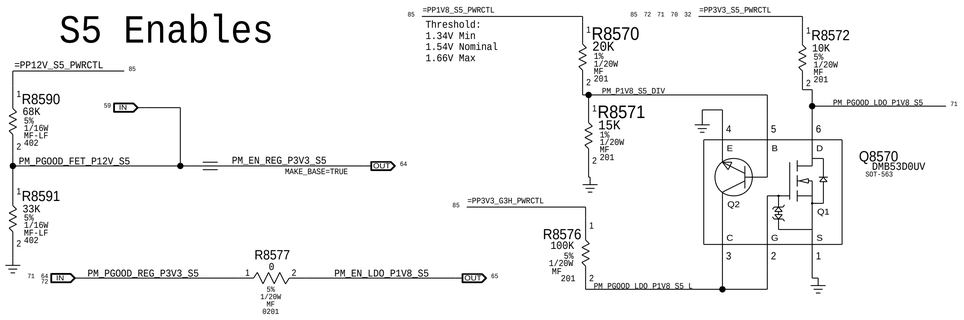
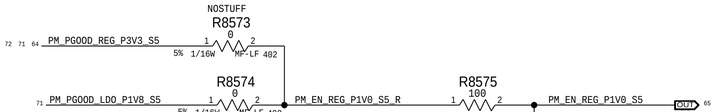
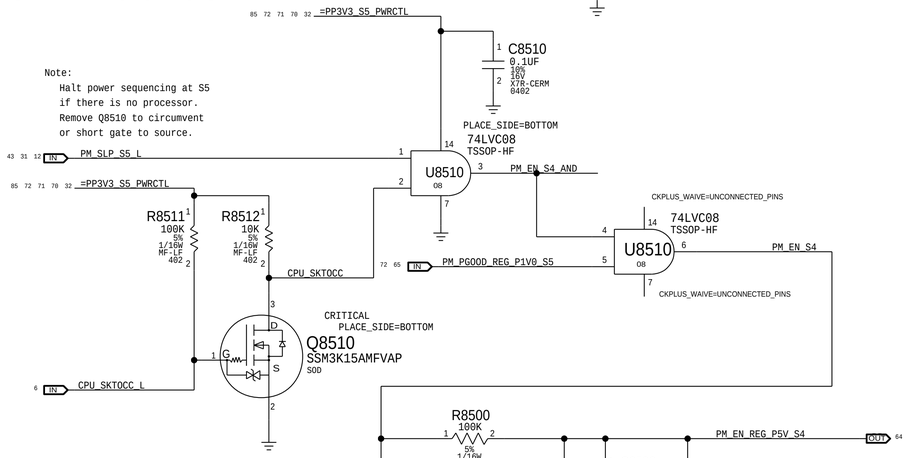
S5 Enables



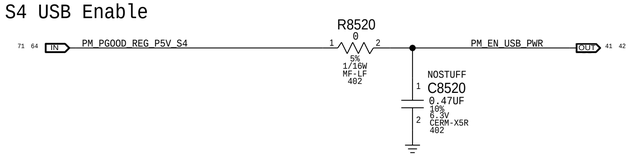


S4 Enables

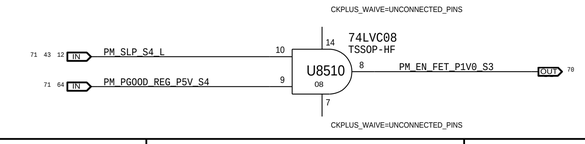


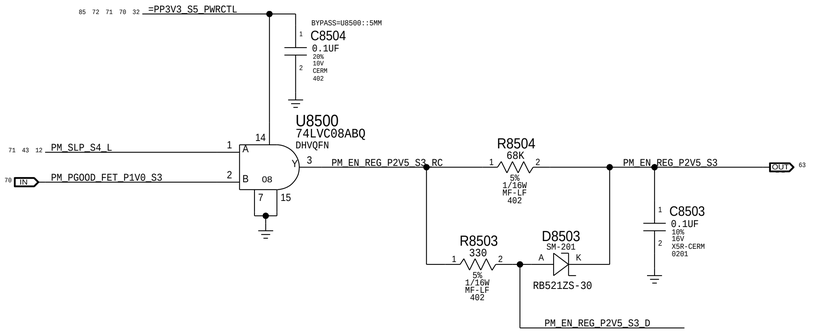
~40 ms RC delay added to ensure that 5V S4 rail stays up at least as long as the S0 sequencing holds in order to keep 5V S0 powered.

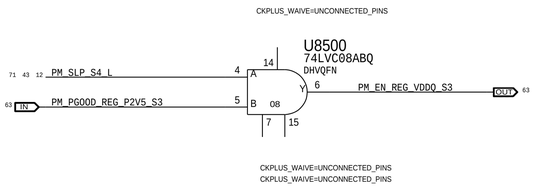
S4 USB Enable



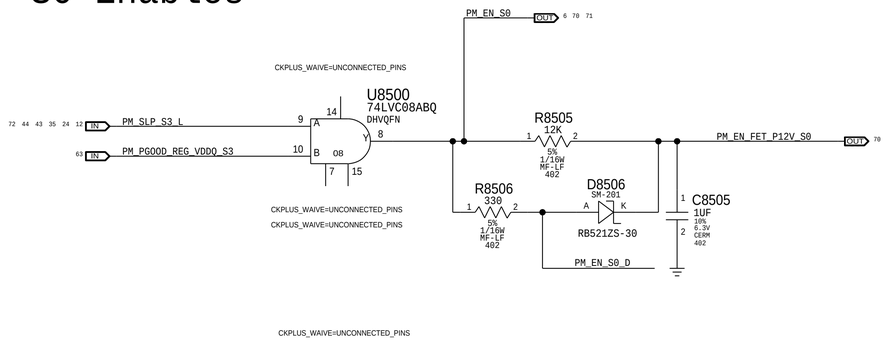
S3 Enables

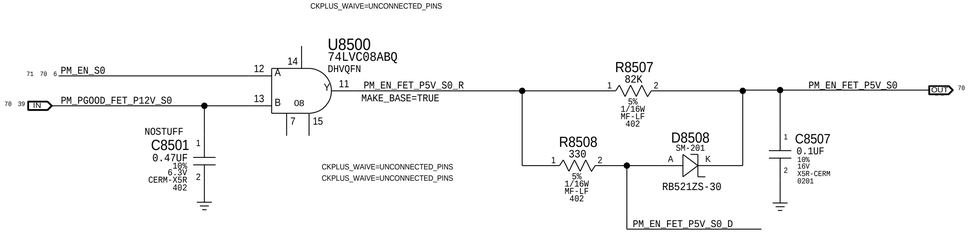


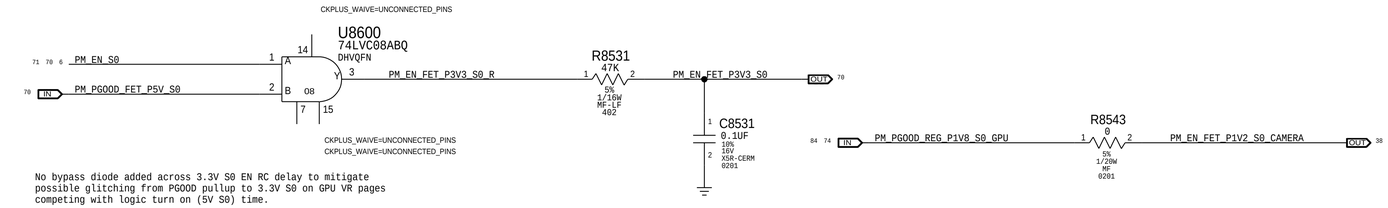




S0 Enables

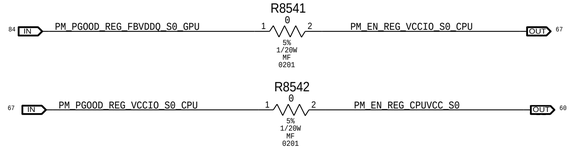






No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 3.3V S0 on GPU VR pages competing with logic turn on (5V S0) time.

S0 CPU Sequencing



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=dtuzman	SYNC_DATE=04/01/2016
PAGE TITLE	PM Regulator Enables
Apple Inc.	DRAWING NUMBER 051-01477 SIZE D
	REVISION 3.26.0
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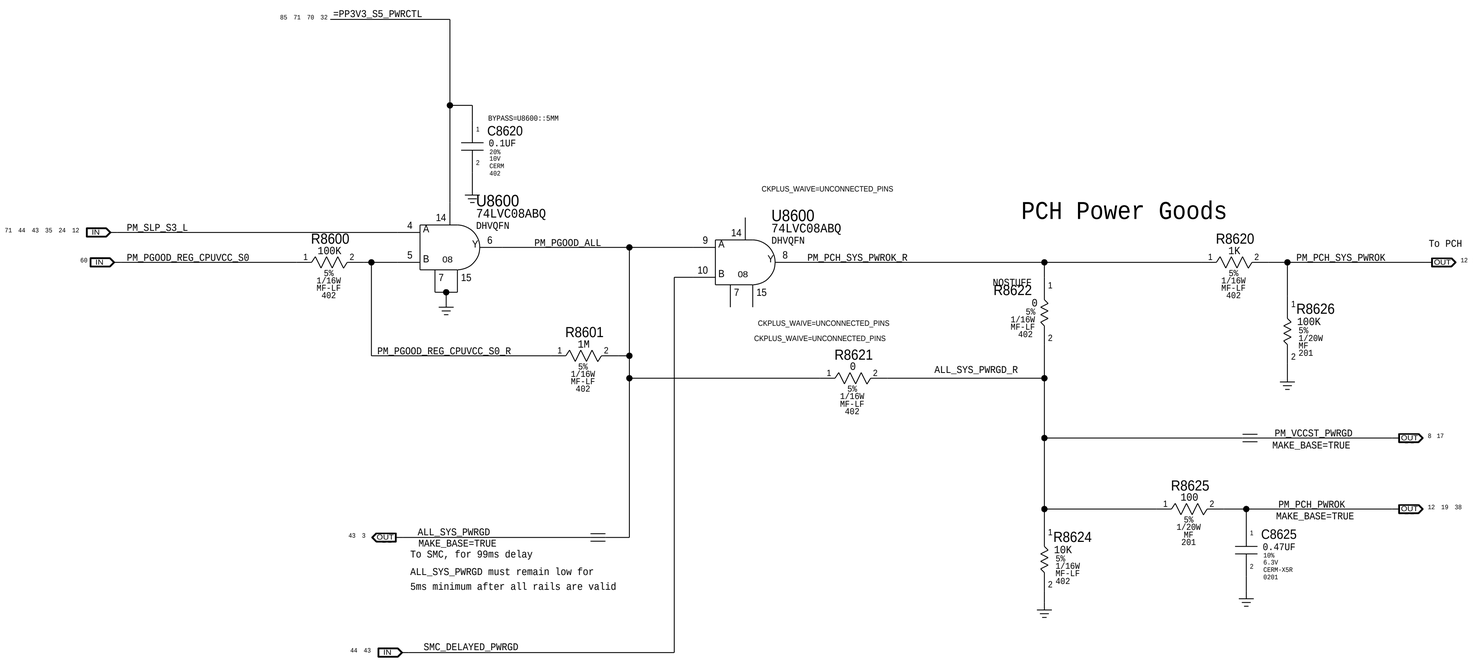
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 2.5V and 1.2V for DDR4

Notes on sequencing requirements

Intel:

1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

PCH Power Goods

Resume Reset

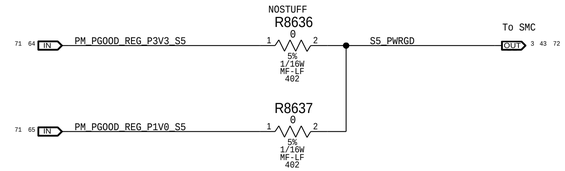
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

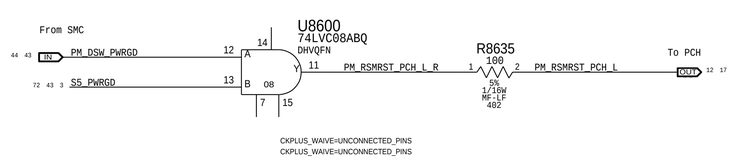
Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.





BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=hurtadot SYNC_DATE=06/01/2016

PAGE TITLE
PM Power Good

Apple Inc.

DRAWING NUMBER 051-01477
SIZE D
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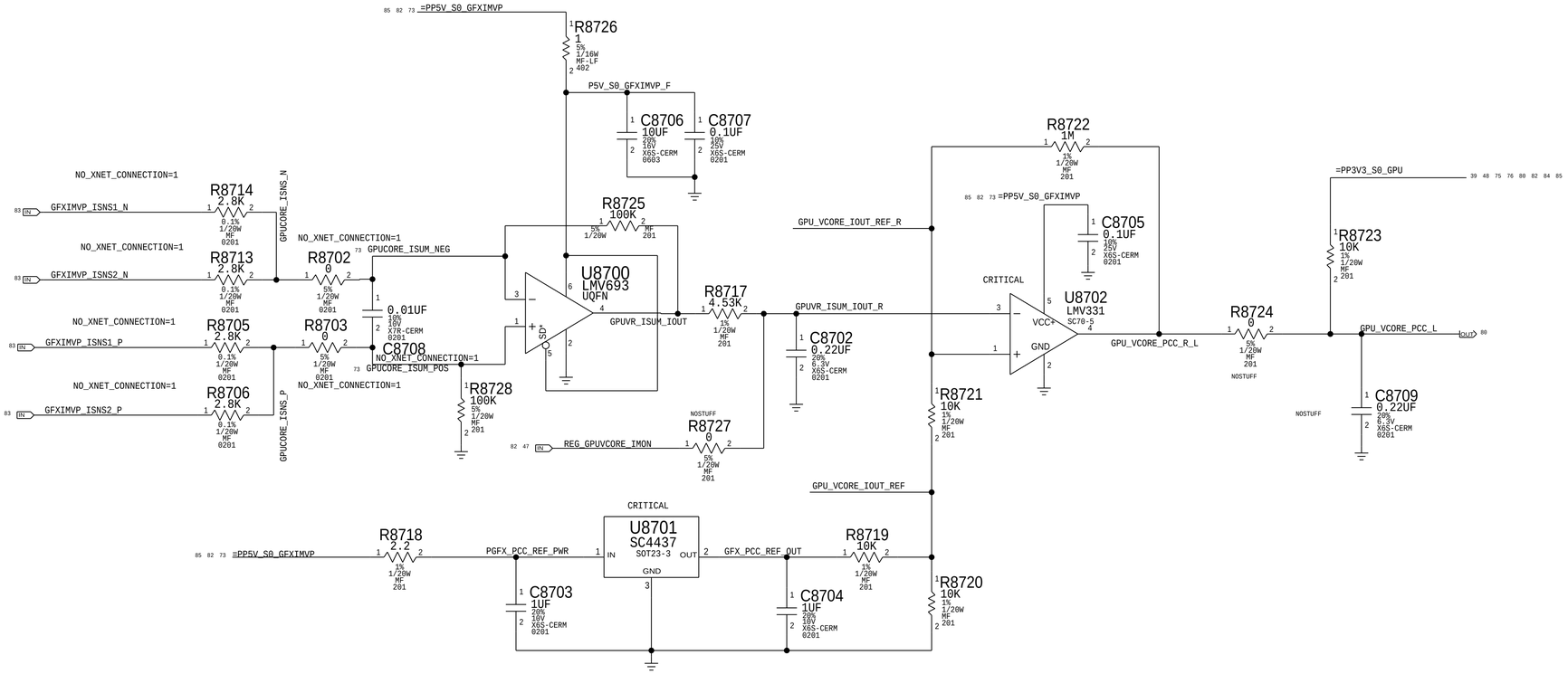
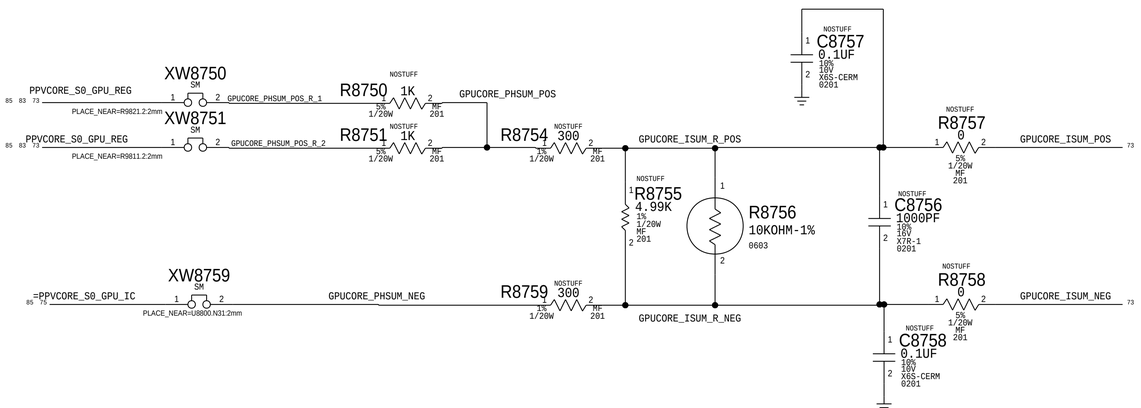


Copper sense apparatus



BOM_COST_GROUP=GRAPHICS

PAGE TITLE

GPU PCC

Apple Inc.

DRAWING NUMBER 051-01477

SIZE D

REVISION 3.26.0

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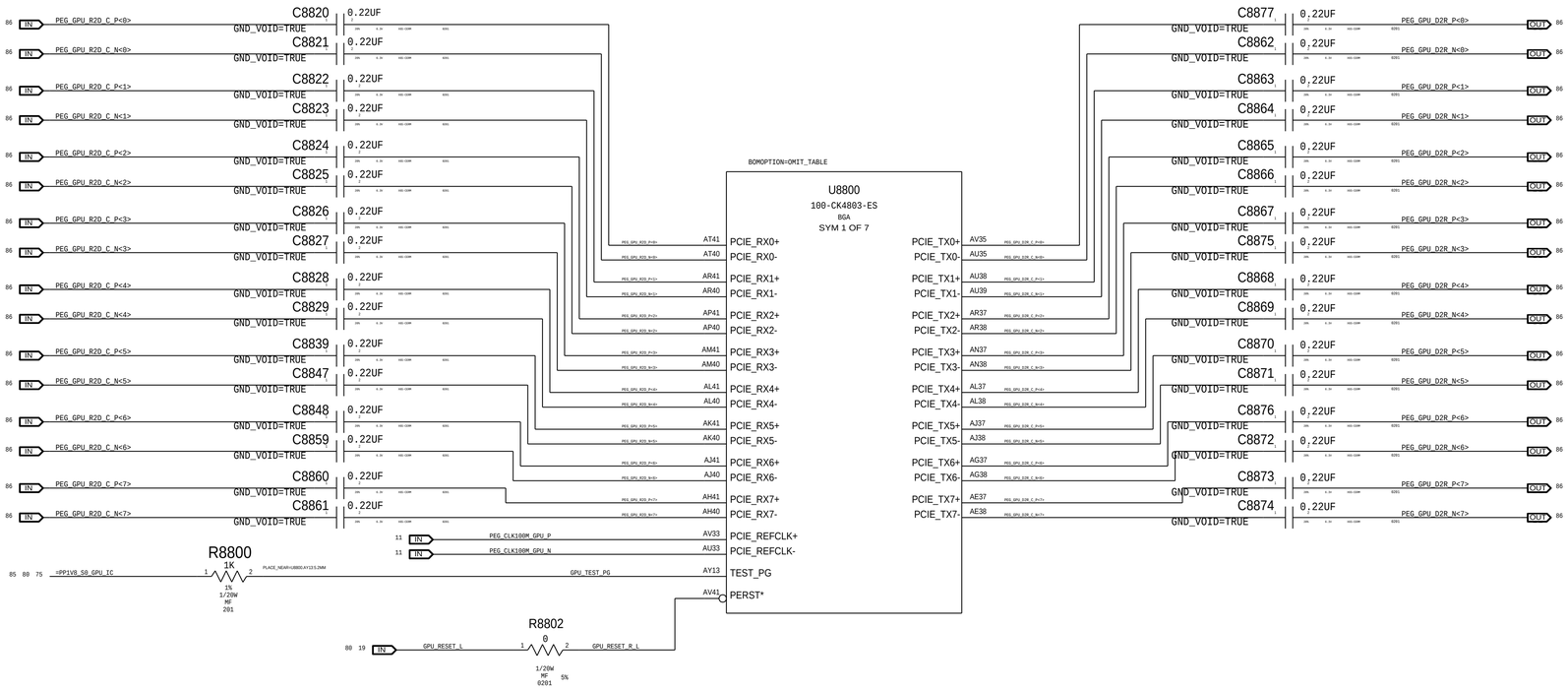
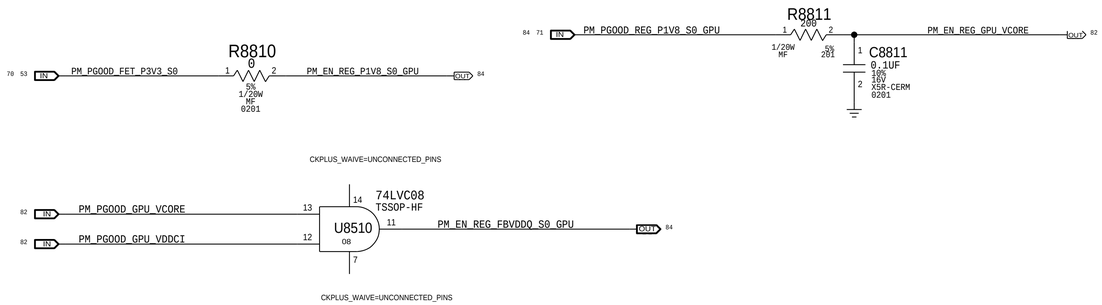
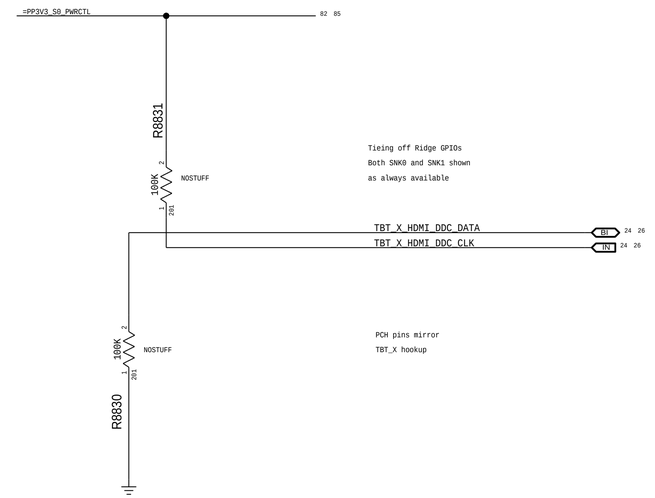


GPU Power Sequencing





Power Sequencing - to be replaced by cascading enables.

Baffin reqs:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/\u03bcs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10us before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: Baffin PEG & Power Seq

Apple Inc.

DRAWING NUMBER: 051-01477 SIZE: D

REVISION: 3.26.0

BRANCH:

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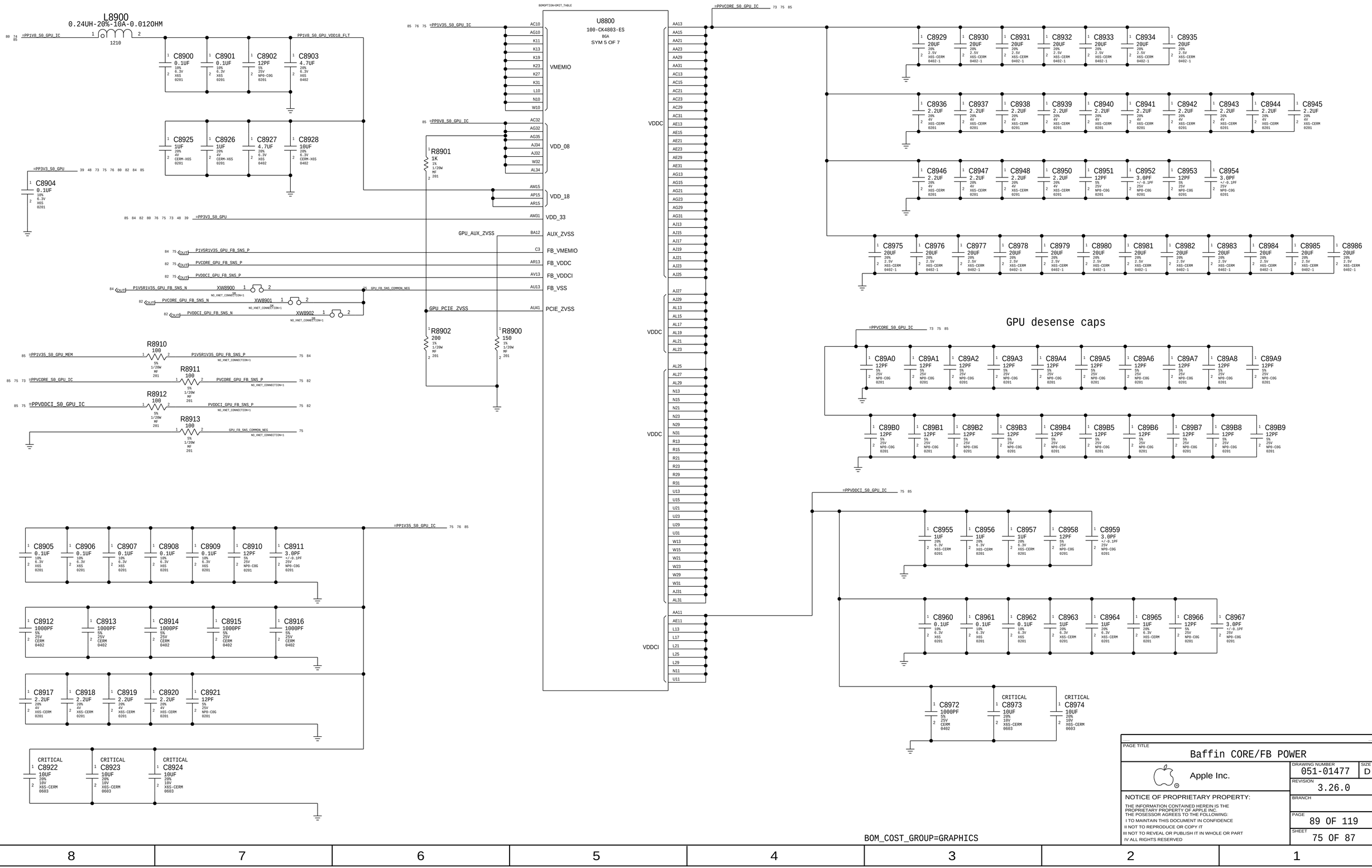

PAGE TITLE

Baffin CORE/FB POWER

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REVISION 3.26.0

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BOMOPTION=OMIT_TABLE

U8800
100-CK4803-ES
BGA
SYM 3 OF 7

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100-CK4803-ES
BGA
SYM 4 OF 7

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R9002 120 1% 1/20W MF 201 — PLACE_NEAR=U8800.K15:2.54MM — FB_A_CALR
R9003 120 1% 1/20W MF 201 — PLACE_NEAR=U8800.R10:2.54MM — FB_B_CALR

R9091 10 1% 1/20W MF 201 — FB_A_RESET_PIN_L
R9093 49.9 1% 1/20W MF 201 — FB_A_RESET_R_L — FB_A_RESET_L — OUT 77
R9090 5.1K 1% 1/20W MF 201
C9090 120PF 10% 25V X7R 0201

R9096 10 1% 1/20W MF 201 — FB_B_RESET_PIN_L
R9097 49.9 1% 1/20W MF 201 — FB_B_RESET_R_L — FB_B_RESET_L — OUT 78
R9095 5.1K 1% 1/20W MF 201
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85 76 75 =PP1V35_S0_GPU_IC

R9004 40.2 1% 1/20W MF 201 — NOSTUFF — PLACE_NEAR=U8800.K17:3MM
note: to be unstuffed after initial baffin bringup
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C9000 1UF 20% 6.3V X5S-CERM 0201 — PLACE_NEAR=U8800.K17:3.2MM

R9005 40.2 1% 1/20W MF 201 — NOSTUFF — PLACE_NEAR=U8800.U10:2.54MM
note: to be unstuffed after initial baffin bringup
R9007 100 1% 1/20W MF 201 — PLACE_NEAR=U8800.U10:2.54MM
C9001 1UF 20% 6.3V X5S-CERM 0201 — PLACE_NEAR=U8800.U10:2.54MM

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
Baffin FRAME BUFFER I/F

Apple Inc.

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U9200
32MX32-1.25GHZ-MFL
(1 OF 2)
OMIT_TABLE
BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
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CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
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DBI0*
DBI1*
DBI2*
DBI3*
DQ0
DQ31
NC
CK TERMINATION - A0
CK TERMINATION - A1
U9200
(2 OF 2)
VDD
VSS
VDDQ
VSSQ
VREFC
VREFD
U9250
(1 OF 2)
(2 OF 2)
VRAM desense caps
C92A0
C92A1
C92A2
C92A3
12PF
BOM_COST_GROUP=GRAPHICS

PAGE TITLE

GDDR5 Frame Buffer A

Apple Inc.

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8 7 6 5 4 3 2 1

D C B A

U9300
32MX32-1.25GHZ-MFL
86A
MT62F1G32D4AFR-72C
(1 OF 2)
OMIT_TABLE

U9350
32MX32-1.25GHZ-MFL
86A
MT62F1G32D4AFR-72C
(1 OF 2)
OMIT_TABLE

U9300
32MX32-1.25GHZ-MFL
86A
MT62F1G32D4AFR-72C
(2 OF 2)
OMIT_TABLE

U9350
32MX32-1.25GHZ-MFL
86A
MT62F1G32D4AFR-72C
(2 OF 2)
OMIT_TABLE

VRAM desense caps

BOM_COST_GROUP=GRAPHICS

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SPEED MLPS STRAPS

PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled
All power audio-capable display output
256MB FB Aperture Size

PS_0:	01001	82nF	8.45k	2k
PS_1:	10001	10nF	8.45k	2k
PS_2:	10000	10nF	NC	4.75k
PS_3:	00000	680nF	NC	4.75k

NOT REQUIRED FOR BAFFIN

NOTICE THE ANNOYING MIX OF 3.3V AND 1.8V PULL-UPS

85 =PP3V3_S0_GPU_STRAPS
85 =PP1V8_S0_GPU_STRAPS

R9470 10K 5% 1/20W MF 201 — NOSTUFF
R9471 10K 5% 1/20W MF 201 — NOSTUFF
R9472 10K 5% 1/20W MF 201 — NOSTUFF
R9473 10K 5% 1/20W MF 201 — NOSTUFF
R9474 10K 5% 1/20W MF 201
R9475 10K 5% 1/20W MF 201 — NOSTUFF
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R9478 10K 5% 1/20W MF 201 — NOSTUFF
R9479 10K 5% 1/20W MF 201 — NOSTUFF
R947E 10K 5% 1/20W MF 201 — NOSTUFF

R947A 10K 5% 1/20W MF 201 — NOSTUFF
R947B 10K 5% 1/20W MF 201
R947C 10K 5% 1/20W MF 201 — NOSTUFF
R947D 10K 5% 1/20W MF 201
R947F 10K 5% 1/20W MF 201
R9480 10K 5% 1/20W MF 201 — NOSTUFF
R9481 10K 5% 1/20W MF 201
R9482 10K 5% 1/20W MF 201 — NOSTUFF
R9483 10K 5% 1/20W MF 201 — NOSTUFF
R9484 10K 5% 1/20W MF 201

80	GPU_ROM_CONFIG<2>	0
80	GPU_ROM_CONFIG<1>	0
80	GPU_ROM_CONFIG<0>	1
80	GPU_AUD_PORT_CONN<2>	0
80	GPU_AUD_PORT_CONN<1>	0
80	GPU_AUD_PORT_CONN<0>	0
80	GPU_BIF_GEN3_EN_A	1
80	GPU_TX_HALF_SWING	0
80	GPU_TX_DEEMPH_EN	1
80 79	GPU_ROM_SO (strap_BIF_CLK_PM_EN)	1
80 79	GPU_ROM_CS_L_R (strap_BTOS_ROM_EN)	0
80	GPU_VGA_DIS	0
80	GPU_AUD<1>	1
80	GPU_AUD<0>	0
80	GPU_BRD_CFG<2>	0
80	GPU_BRD_CFG<1>	0
80	GPU_BRD_CFG<0>	0
80	GPU_SMBUS_ADDR<1>	0
80	GPU_SMBUS_ADDR<0>	1

R9485 10K 5% 1/20W MF 201
R9486 10K 5% 1/20W MF 201 — NOSTUFF
R9487 10K 5% 1/20W MF 201
R9488 10K 5% 1/20W MF 201 — NOSTUFF
R9489 10K 5% 1/20W MF 201 — NOSTUFF
R948A 10K 5% 1/20W MF 201
R948B 10K 5% 1/20W MF 201 — NOSTUFF
R948C 10K 5% 1/20W MF 201
R948D 10K 5% 1/20W MF 201
R948E 10K 5% 1/20W MF 201 — NOSTUFF

GPU_ROM_SI_R (strap_reserved) 79 80
GPU_RESERVED 80

R948F 10K 5% 1/20W MF 201
R9490 10K 5% 1/20W MF 201
R9491 10K 5% 1/20W MF 201
R9492 10K 5% 1/20W MF 201
R9493 10K 5% 1/20W MF 201 — NOSTUFF
R9494 10K 5% 1/20W MF 201
R9495 10K 5% 1/20W MF 201
R9496 10K 5% 1/20W MF 201
R9497 10K 5% 1/20W MF 201
R9498 10K 5% 1/20W MF 201
R9499 10K 5% 1/20W MF 201 — NOSTUFF

BAFFIN STRAPS

PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

GPU SVI2 VOLTAGE TRANSLATION
SPEED ONLY

NOT REQUIRED FOR BAFFIN

GPU CLKREQ GATING

NOT REQUIRED FOR BAFFIN

GPU ROM

85 =PP3V3_S0_GPU_ROM

R9423 33 5% 1/20W MF 201 — GPU_ROM:YES
R9424 33 5% 1/20W MF 201 — GPU_ROM:YES
R9425 33 5% 1/20W MF 201 — GPU_ROM:YES
R9421 15K 1% 1/20W MF 201 — GPU_ROM:YES
R9420 10K 1% 1/20W MF 201 — GPU_ROM:YES
R9422 0 5% 1/20W MF 201 — NO STUFF
R9426 33 5% 1/20W MF 201 — GPU_ROM:YES
C9421 0.1UF 10% 6.3V X5S 0201 — GPU_ROM:YES

79 80 GPU_ROM_SI_R — GPU_ROM_SI
80 GPU_ROM_SCLK_R — GPU_ROM_SCLK
79 80 GPU_ROM_CS_L_R — GPU_ROM_CS_L
GPU_ROM_WP_L

U9401 M25P10A UFDFPN8
VCC 8
D 5 — GPU_ROM_SO_R — 79 80 GPU_ROM_SO
C 6 — GPU_ROM_SCLK
S* 1 — GPU_ROM_CS_L
W* 3 — GPU_ROM_WP_L
HOLD* 7
VSS 4
THRM PAD 9

GPU JTAG

85 =PP3V3_S0_GPU_JTAG

R9431 10K 5% 1/10W MF-LF 402 — NOSTUFF
R9432 10K 5% 1/10W MF-LF 402 — NOSTUFF
R9433 10K 5% 1/10W MF-LF 402 — NOSTUFF
R9434 10K 5% 1/10W MF-LF 402 — NOSTUFF
R9430 10K 5% 1/10W MF-LF 402 — NOSTUFF

GPU_JTAG_TDI 80
GPU_JTAG_TRST_L 80
GPU_JTAG_TMS 80
GPU_JTAG_TDO 80
GPU_JTAG_TCK 80

85 =PP1V8_S0_GPU_XTAL

R9440 0 5% 1/20W MF 0201 — OMIT_TABLE
R9441 10K 5% 1/20W MF 201 — GPUCLK:OSC
C9440 18PF 5% 25V C0G 0201 — GPUCLK:XTAL
GPU_XTAL_XTAL_OR_CLK
R9443 0 5% 1/20W MF 0201 — OMIT_TABLE
GPU_XTAL_XTAL_OR_CLK_IN 80
R9445 1M 5% 1/20W MF 201 — GPUCLK:XTAL
Y9440 27MHZ-30PPM-18PF-60OHM 2.50X2.00MM-SM — OMIT_TABLE
GPU_XTAL_PWR_OR_GND
R9442 0 5% 1/20W MF 0201 — OMIT_TABLE
R9444 0 5% 1/20W MF 0201 — GPUCLK:XTAL
GPU_XTAL_OUT 80
GPU_XTAL_PU_OR_CAP
C9441 18PF 5% 25V C0G 0201 — GPUCLK:XTAL

GPU XTAL 27 MHZ
OR
GPU OSC 100 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0499	1	XTAL,27.000MHZ,30PPM,12PF,2.5X2.0MM	Y9440	CRITICAL	GPUCLK:XTAL
197S0056	1	OSC,MEMS,100MHZ,+/-20PPM,1.8V,2520	Y9440	CRITICAL	GPUCLK:OSC
155S0387	1	FERRITE BEAD, 470OHM,0.1A,1.5MOHM DCR,060	R9440	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	R9442	CRITICAL	GPUCLK:XTAL
132S0444	1	CAP,CER,X5R,0.1UF,10%,6.3V,0201	R9442	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	R9443	CRITICAL	GPUCLK:XTAL
117S0080	1	RES,33 OHM,5%,0201	R9443	CRITICAL	GPUCLK:OSC

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
Baffin GPIOs,CLK & Straps

Apple Inc.

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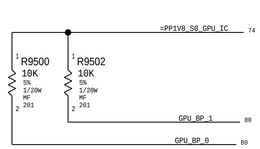
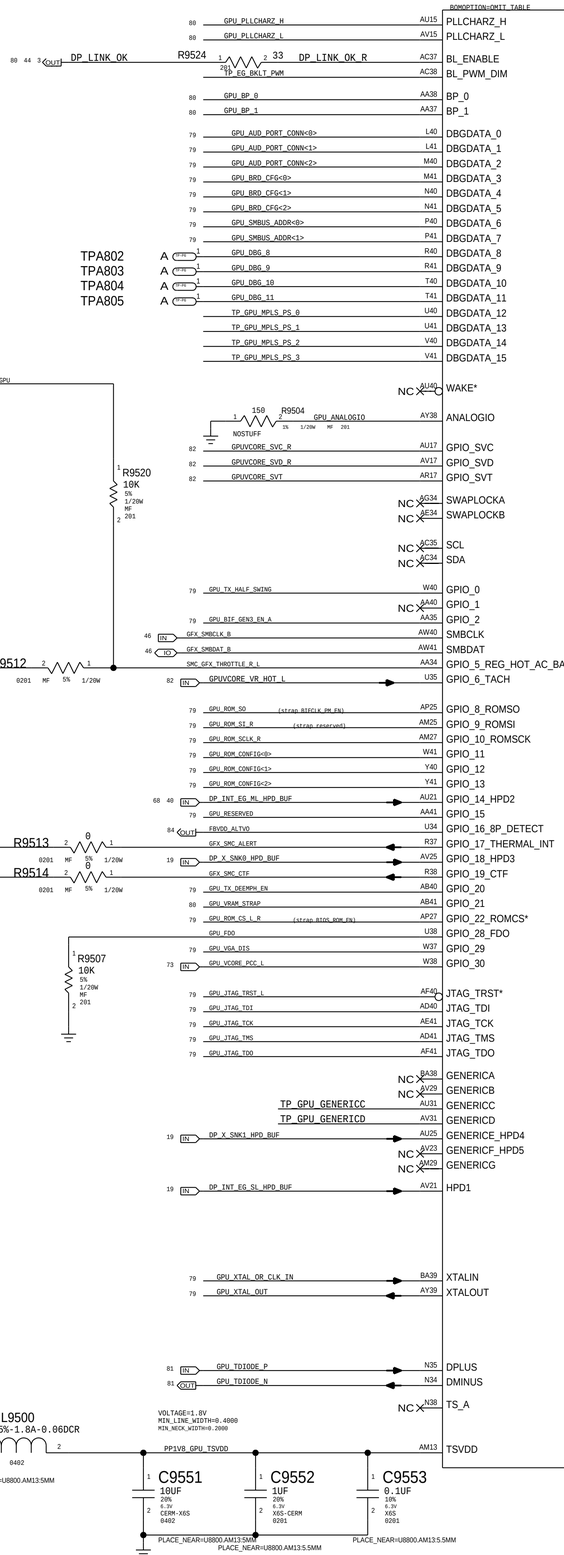
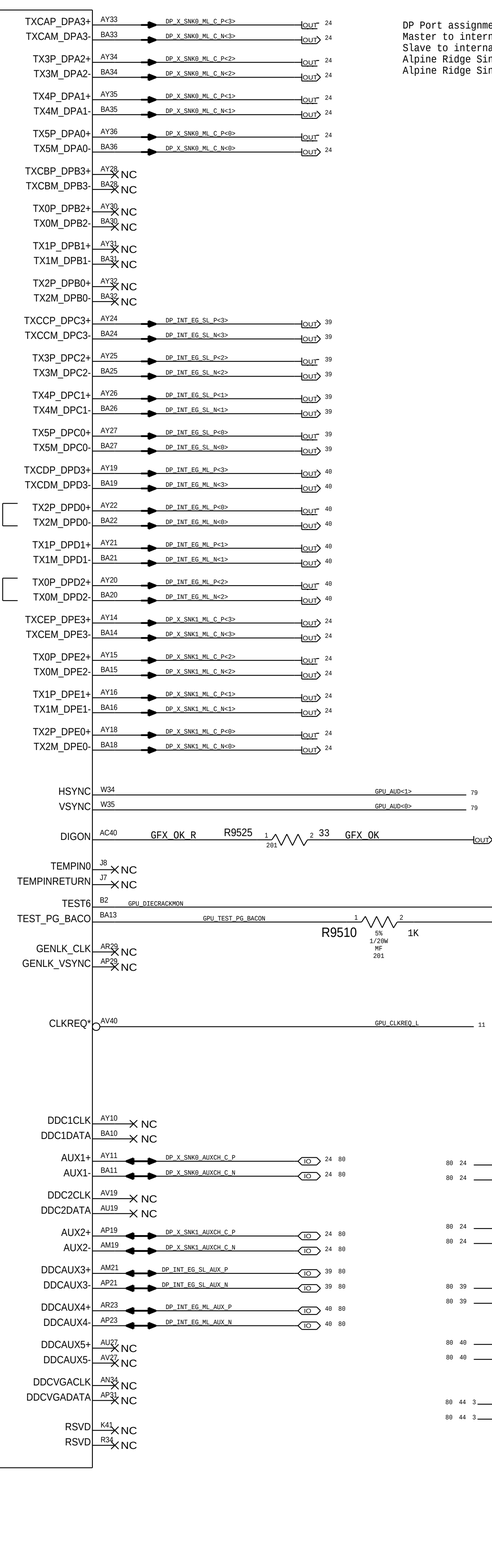
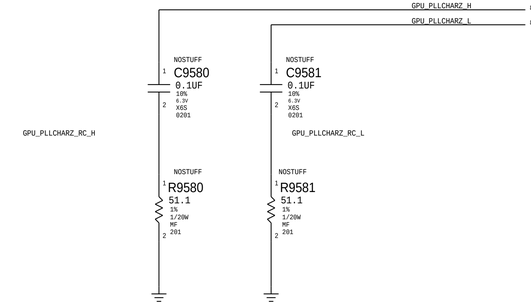


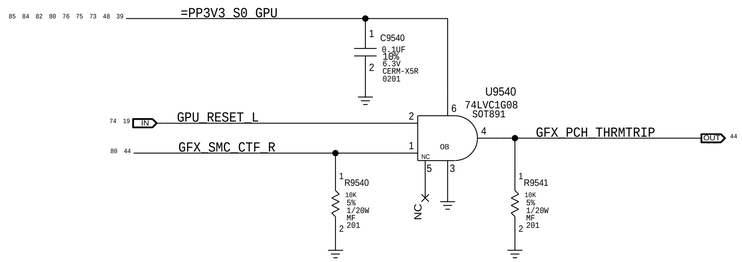


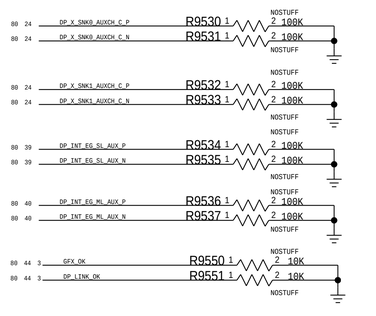


DP Port assignments:
Master to internal display: DP Port D
Slave to internal display: DP Port C
Alpine Ridge Sink0: DP Port A
Alpine Ridge Sink1: DP Port E



GPU OVERTEMP MASKING





BOM_COST_GROUP=GRAPHICS

PAGE TITLE
Baffin DP/GPIO

Apple Inc.

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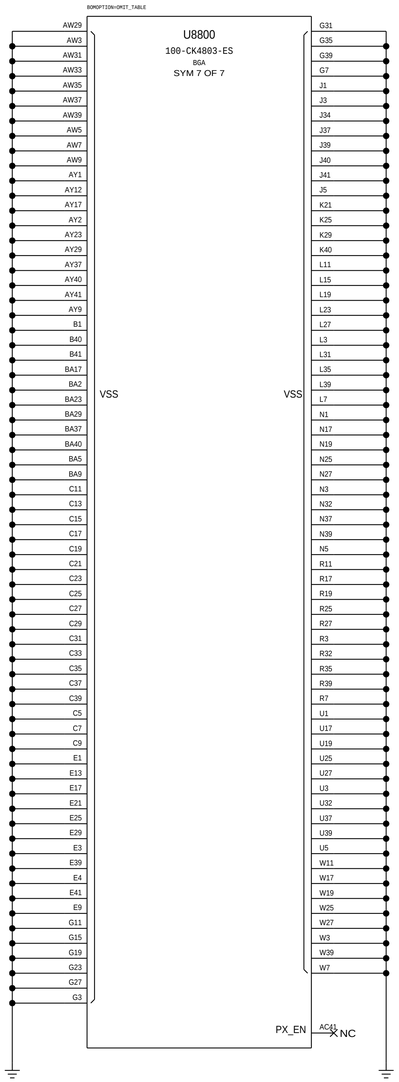
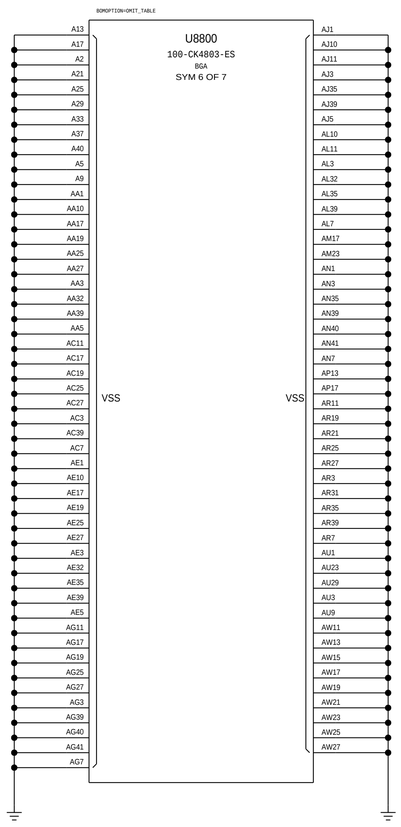
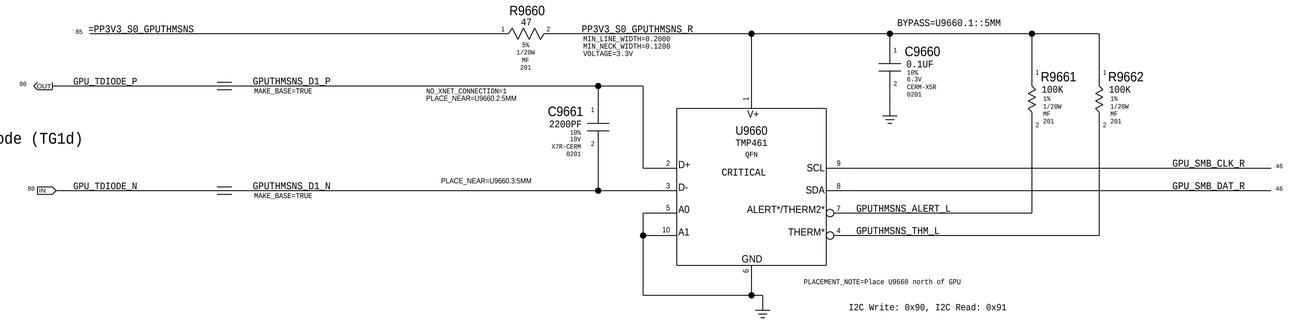




GPU proximity (TG0p)

GPU TDiode (TG1d)



BOM_COST_GROUP=GRAPHICS

PAGE TITLE
Baffin VSS & MISC

Apple Inc.

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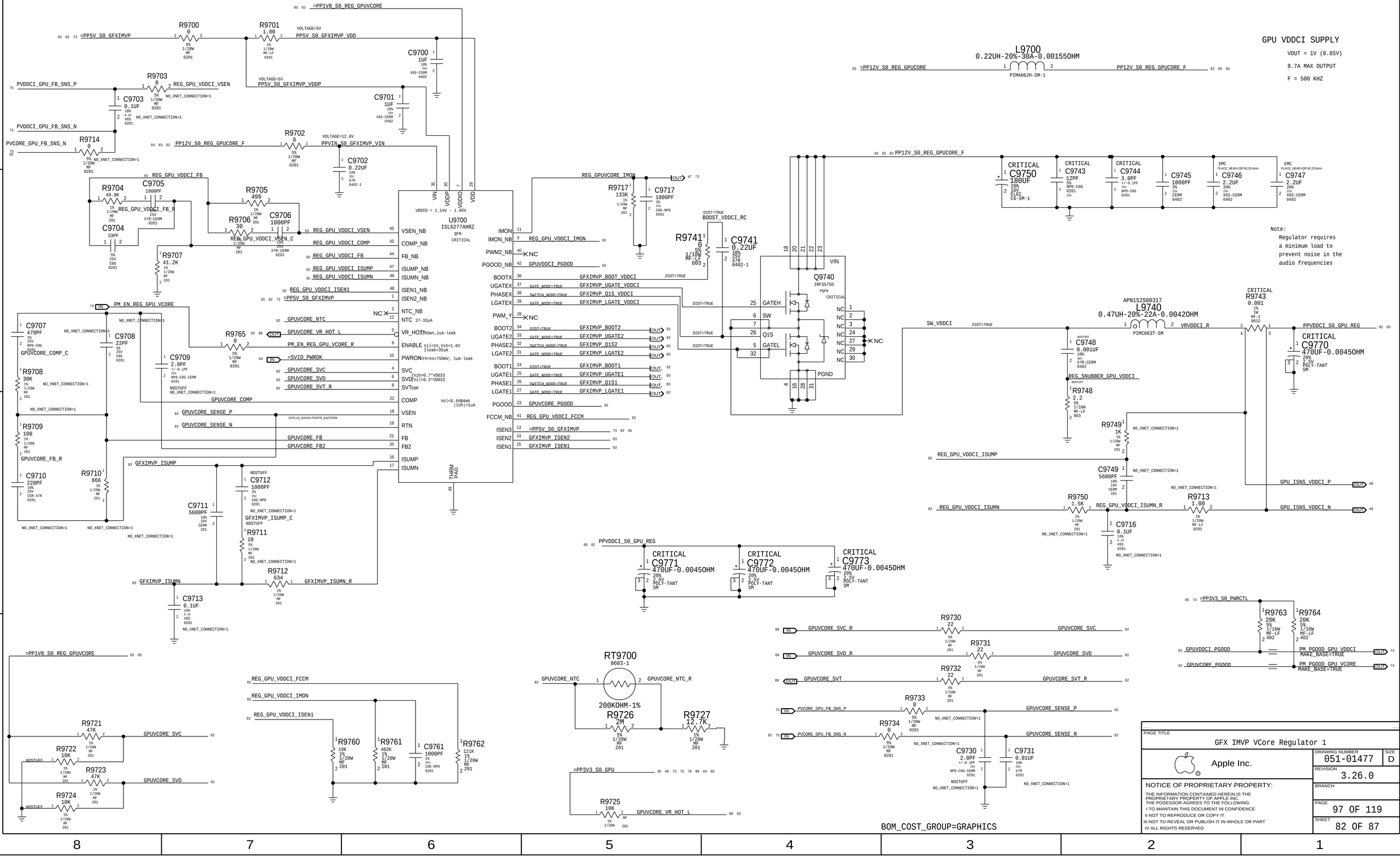
GPU VDDCI SUPPLY
VOUT = 1V (0.85V)
8.7A MAX OUTPUT
F = 500 KHZ
L9700
0.22UH-20%-30A-0.00155OHM
PIMA062H-SM-1
=PP12V_S0_REG_GPUCORE
PP12V_S0_REG_GPUCORE_F
Note:
Regulator requires
a minimum load to
prevent noise in the
audio frequencies
L9740
APN152S00317
0.47UH-20%-22A-0.0042OHM
PIMC063T-SM
VRVDDCI_R
PPVDDCI_S0_GPU_REG
REG_SNUBBER_GPU_VDDCI
=PP1V8_S0_REG_GPUVCORE
=PP3V3_S0_PWRCTL
=PP3V3_S0_GPU
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
GFX IMVP VCore Regulator 1
Apple Inc.
DRAWING NUMBER
051-01477
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D
REVISION
3.26.0
BRANCH
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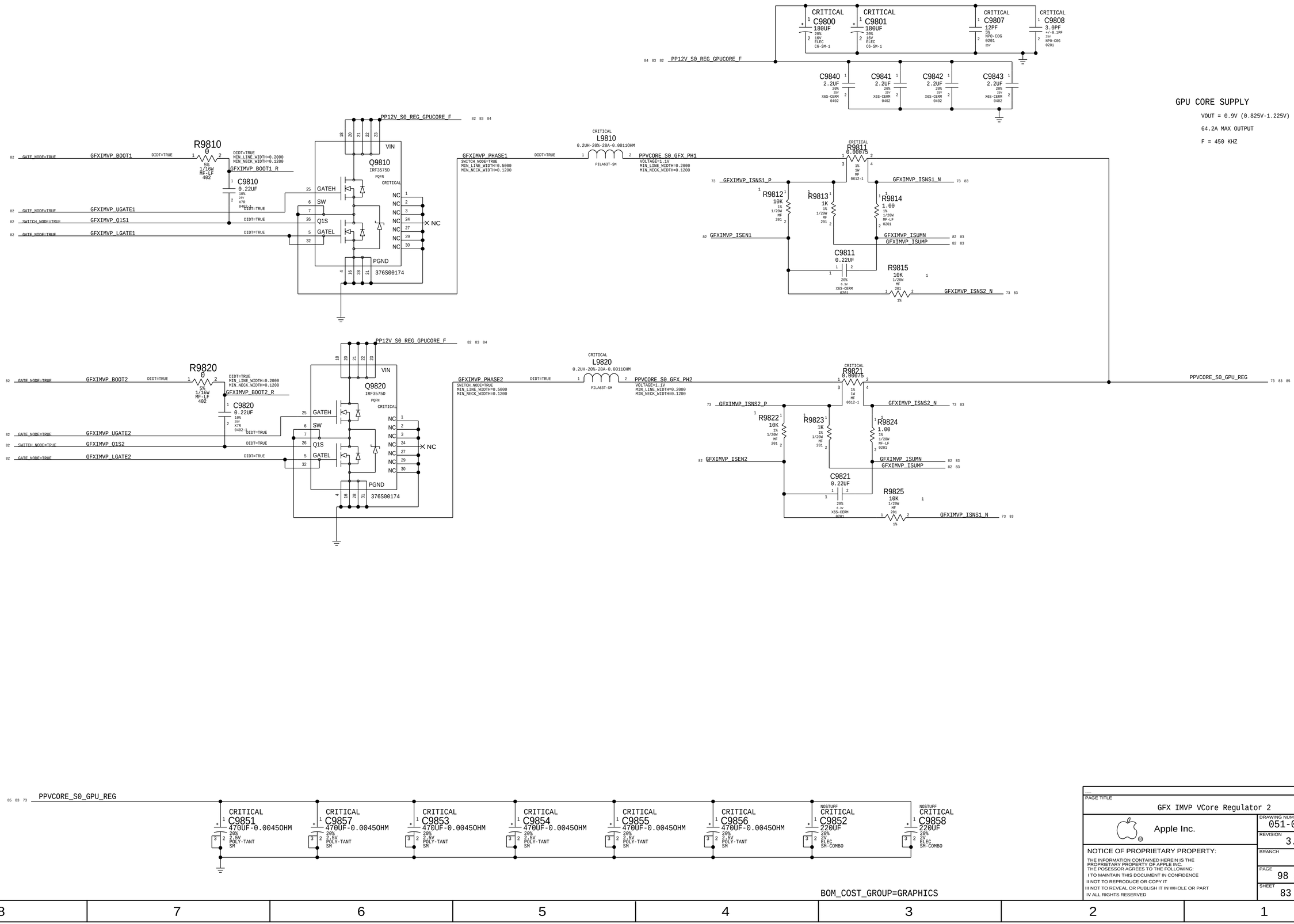

PAGE TITLE

GFX IMVP VCore Regulator 2

Apple Inc.

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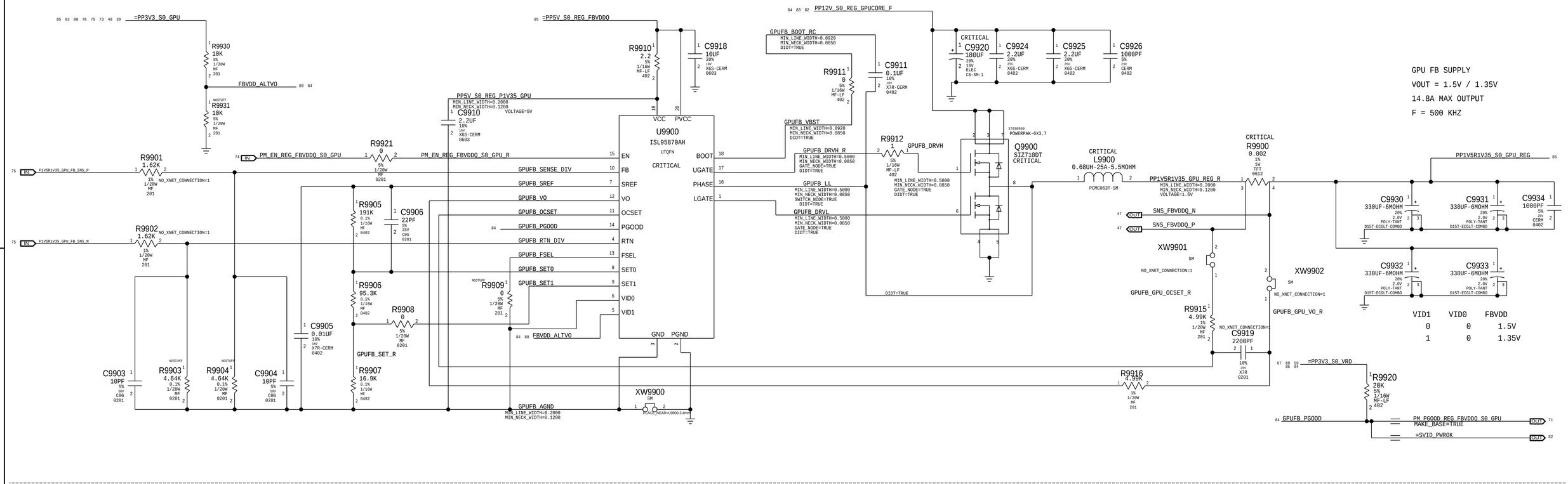

PAGE TITLE	BAFFIN 1V35 FB/1V8 Power Supplies
Apple Inc.	DRAWING NUMBER 051-01477 · SIZE D
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G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3
MAKE_BASE=TRUE
- PP3V3_G3_RTC 18
- =PP3V3_G3_PCH_RTC 12 15

G3H Rails

PP12V_ACDC
MAKE_BASE=TRUE
- PP12V_G3H_ACDC 59
- =PP12V_G3H_SNS_R 47

PP12V_G3H
MAKE_BASE=TRUE
- PP12V_G3H_SNS 47
- =PP12V_G3H_REG_3V3_G3H 59
- =PP12V_G3H_FET_P12V_S5 59
- =PP12V_G3H_FET_P12V_S0 70

PP3V3_G3H
MAKE_BASE=TRUE
- PP3V3_G3H_REG 59
- =PP3V3_G3H_BT 31
- =PP3V3_G3H_SMC 43 44 51
- =PP3V3_G3H_RTC_D 18
- =PP3V3_G3H_SMC_USBMUX 41
- =PP3V3_G3H_T112 45
- =PP3V3_G3H_SMB 46
- =PP3V3_G3H_UPC_XA 27
- =PP3V3_G3H_UPC_XB 28
- =PP3V3_G3H_PWRCTL 71

Ground/Common

GND\G
MAKE_BASE=TRUE

S5 Rails

Enabled when system has AC and is in S5

PP12V_S5
MAKE_BASE=TRUE
- PP12V_S5_FET 59
- =PP12V_S5_REG_VDDQ_S3 63
- =PP12V_S5_PWRCTL 71
- =PP12V_S5_SNS 47
- =PP12V_S5_REG_P1V8_S5 65
- =PP12V_S5_REG_P3V3_S5_P5V_S4 64
- =PPHV_SW_TBT_X 26

PP5V_S5
MAKE_BASE=TRUE
- PP5V_S5_LDO 64
- =PP5V_S5_PWRCTL 70
- =PP5V_S5_REG_P1V0 65
- =PP5V_S5_XDP 17
- =PP5V_S5_PCC 50

PP3V3_S5
MAKE_BASE=TRUE
- PP3V3_S5_REG 64
- =PP3V3_S5_FET_P3V3_S0 32 70
- =PP3V3_S5_FET_P3V3_S4 70
- =PP3V3_S5_SMC 32 44
- =PP3V3_S5_LED 3
- =PP3V3_S5_PCH_VCC 12 13 14 15 19
- =PP3V3_S5_PWRCTL 32 70 71 72
- =PP3V3_S5_ROM 17 45
- =PP3V3_S5_VRD 64 65
- =PP3V3_S5_SENSE 47 48 50
- =PP3V3_S5_RSTBUF 19
- =PP3V3_S5_LDO_P1V8_S5 65

PP1V8_S5
MAKE_BASE=TRUE
- PP1V8_S5_LDO 65
- =PP1V8_S5_PCH_VCCHDA 15 18
- =PP1V8_S5_PWRCTL 71

PP1V0_S5
MAKE_BASE=TRUE
- PP1V0_S5_REG 65
- =PP1V0_S5_PCH_VCC 11 15
- =PP1V0_S5_XDP 17
- =PP1V0_S5_FET_P1V0_S3 70

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4_SRC
MAKE_BASE=TRUE
- PP5V_S4_REG 64
- =PP5V_S4_NON_USBA_SNS_R 48
- =PP5V_S4_USBA_SNS_R 48

PP5V_S4_NONUSBA
MAKE_BASE=TRUE
- PP5V_S4_NON_USBA_SNS 48
- =PP5V_S4_FET_P5V_S0 70
- =PP5V_S4_PWRCTL 70
- =PP5V_S4_USBC 26
- =PP5V_S4_FET_P5V_HDD 70
- =PP5V_S4_REG_VDDQ_S3 63
- =PP5V_S4_REG_CPUCORE 60

PP5V_S4_USBA
MAKE_BASE=TRUE
- PP5V_S4_USBA_SNS 48
- =PP5V_S4_USBA_CONN 41 42

PP3V3_S4
MAKE_BASE=TRUE
- PP3V3_S4_FET 70
- =PP3V3_S4_FET_ENET 35
- =PP3V3_S4_PWRCTL 39 63 70
- =PP3V3_S4_LED 3
- =PP3V3_S4_PCH_GPIO 19
- =PP3V3_S4_SDCARD 36
- =PP3V3_S4_SMC 44
- =PP3V3_S4_TBT 19
- =PP3V3_S4_AP 31 44
- =PP3V3_S4_REG_P2V5_S3 63
- =PP3V3_S4_MEMRESET 6
- =PP3V3_S4_PCH_VCC 13 14
- =PP3V3_UPC_XA_AUX 27
- =PP3V3_UPC_XB_AUX 28

PP3V3_ENET
MAKE_BASE=TRUE
- PP3V3_ENET_FET 35
- =PP3V3_ENET_PHY 34 35

S3 Rails

Enabled when system is in run or sleep

PPVDDQ_S3
MAKE_BASE=TRUE
- PPVDDQ_S3_REG 63
- =PPVDDQ_S3_SNS_DDR_R 48
- =PP1V2_S3_CAMERA_FET 38

PPVDDQ_S3_DDR
MAKE_BASE=TRUE
- PPVDDQ_S3_SNS_DDR 48
- =PPVDDQ_S3_MEMVREF 20
- =PPVDDQ_S3_MEM_A 21
- =PPVDDQ_S3_MEM_B 22
- =PPVDDQ_S3_MEMRESET 12
- =PPVDDQ_S3_LDO_DDRVTT 63
- =PPVDDQ_S3_CPU 8 10
- =PPVDDQ_S3_VRD 63

PP2V5_S3
MAKE_BASE=TRUE
- PP2V5_S3_REG 63
- =PPDDRVPP_S3_MEM_A 21
- =PPDDRVPP_S3_MEM_B 22

PP1V0_S3_CPU_VCCST
MAKE_BASE=TRUE
- PP1V0_S3_FET 70
- =PP1V0_S3_VCCST 12 60
- =PP1V0_S3_SMC 44
- =PP1V0_S3_XDP 17
- =PP1V0_S3_CPU 6 8 10

S0 Rails

Enabled when system is in run

PP12V_S0
MAKE_BASE=TRUE
- PP12V_S0_FET 70
- =PP12V_S0_AUDIO_SPKRAMP 54 55
- =PP12V_S0_BKLT 68
- =PP12V_S0_FAN 51
- =PP12V_S0_LCD 39
- =PP12V_S0_SNS_GPU_R 47
- =PP12V_S0_SNS_CPUCORE_R 47

PP12V_S0_CPUCORE
MAKE_BASE=TRUE
- PP12V_S0_SNS_CPUCORE 47
- =PP12V_S0_REG_CPUCORE 60

PP12V_S0_GPU
MAKE_BASE=TRUE
- PP12V_S0_SNS_GPU 47
- =PP12V_S0_REG_GPUCORE 82

PP3V3_S0
MAKE_BASE=TRUE
- PP3V3_S0_FET 70
- =PP3V3_S0_VRD 59 60 67 84
- =PP3V3_S0_AUDIO 53 56
- =PP3V3_S0_ENET 34
- =PP3V3_S0_FAN 51
- =PP3V3_S0_INTDPMUX 19 40
- =PP3V3_S0_LED 3
- =PP3V3_S0_PCH 18
- =PP3V3_S0_GPU 39 48 73 75 76 80 82 84 85
- =PP3V3_S0_SDCARD 36
- =PP3V3_S0_SENSE 33 47 48 49
- =PP3V3_S0_SMBUS 46
- =PP3V3_S0_SMBUS_SMC_0 46
- =PP3V3_S0_SMBUS_SMC_1 46
- =PP3V3_S0_SMBUS_SMC_2 46
- =PP3V3_S0_SMBUS_SMC_3 46
- =PP3V3_S0_SMC 44
- =PP3V3_S0_BKLT 68
- =PP3V3_S0_PCH_GPIO 19
- =PP3V3_S0_CAMERA 37 38
- =PP3V3_S0_ALS 37
- =PP3V3_S0_PWRCTL 74 82
- =PP3V3_S0_PCH_VCC 11 12 14 15
- =PP3V3_S0_MEM_A_SPD 21
- =PP3V3_S0_MEM_B_SPD 22
- =PP3V3_S0_GPU 39 48 73 75 76 80 82 84 85
- =PP3V3_S0_GPU_STRAPS 79
- =PP3V3_S0_GPU_ROM 79
- =PP3V3_S0_GPU_JTAG 79
- =PP3V3_S0_GPUTHMSNS 81
- =PP3V3_TBT_X_S0 25

PP3V3_S0_SSD
MAKE_BASE=TRUE
- PP3V3_S0_SSD_FET 32
- =PPVSSD_S0_FET_SNS_R 48

PPVSSD_S0
MAKE_BASE=TRUE
- PPVSSD_S0_FET_SNS 48
- =PPVSSD_S0_CONN 32

PP5V_S0
MAKE_BASE=TRUE
- PP5V_S0_FET 70
- =PP5V_S0_REG_CPUVCC_S0 61 62 66 67
- =PP5V_S0_BKLT 68
- =PP5V_S0_FET_P5V_HDD 70
- =PP5V_S0_CAMERA 37
- =PP5V_S0_PWRCTL 38
- =PP5V_S0_ISENSE 47
- =PP5V_S0_REG_FBVDDQ 84
- =PP5V_S0_GFXIMVP 73 82

PP5V_S0_HDD
MAKE_BASE=TRUE
- PP5V_S0_HDD_FET 70
- =PP5V_S0_SATA 33

PPVCC_S0_CPU
MAKE_BASE=TRUE
- PPVCC_S0_CPU_REG 61
- =PPVCC_S0_CPU 8 10
- =PPVCC_S0_SNS_CPU 47

PPVCCGT_S0_CPU
MAKE_BASE=TRUE
- PPVCCGT_S0_CPU_REG 62
- =PPVCCGT_S0_CPU 8 10
- =PPVCCGT_S0_SNS_CPU 47

PPVCCSA_S0_CPU
MAKE_BASE=TRUE
- PPVCCSA_S0_CPU_REG 66
- =PPVCCSA_S0_CPU 8 10

PPVCCIO_S0
MAKE_BASE=TRUE
- PPVCCIO_S0_CPU_REG 67
- =PPVCCIO_S0_CPU 5 8 10 17

PPVCORE_S0_GPU
MAKE_BASE=TRUE
- PPVCORE_S0_GPU_REG 73 83
- =PPVCORE_S0_GPU_IC 73 75
- =PPVCORE_S0_GPU_SNS 47

PP1V5R1V35_S0_GPU
MAKE_BASE=TRUE
- PP1V5R1V35_S0_GPU_REG 84
- =PP1V35_S0_GPU_FBVDDQ 77 78
- =PP1V35_S0_GPU_IC 75 76
- =PP1V35_S0_GPU_MEM 75

PPVDDCI_S0_GPU
MAKE_BASE=TRUE
- PPVDDCI_S0_GPU_REG 82
- =PPVDDCI_S0_GPU_IC 75
- =PP0V8_S0_GPU_IC 75

PP1V8_S0_GPU
MAKE_BASE=TRUE
- PP1V8_S0_GPU_REG 84
- =PP1V8_S0_GPU_STRAPS 79
- =PP1V8_S0_GPU_IC 74 75 80
- =PP1V8_S0_GPU_XTAL 79
- =PP1V8_S0_GPU_TS 80
- =PP1V8_S0_CAMERA 37
- =PP1V8_S0_REG_GPUVCORE 82
- =PP1V8_S0_DP 40
- =PP1V8_S0_AUD_DIG_TOP 37 52 54
- =PP1V8_S0_AUD_DIG_BOT 52 53 55 56

PPDDRVTT_S0
MAKE_BASE=TRUE
- PPDDRVTT_S0_LDO 63
- =PPDDRVTT_S0_MEM_A 21
- =PPDDRVTT_S0_MEM_B 22

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Power Aliases

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CPU Reserved

17 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12> (MAKE_BASE=TRUE)

Unused Display Aliases

40 24 DP_X_SRC_ML_P<3..0> — NC_DP_X_SRC_ML_P<3..0> (MAKE_BASE=TRUE)
40 24 DP_X_SRC_ML_N<3..0> — NC_DP_X_SRC_ML_N<3..0> (MAKE_BASE=TRUE)
40 24 DP_X_SRC_AUX_P — NC_DP_X_SRC_AUX_P (MAKE_BASE=TRUE)
40 24 DP_X_SRC_AUX_N — NC_DP_X_SRC_AUX_N (MAKE_BASE=TRUE)

GPU PEG Lanes

5 =PEG_D2R_P<7..0> — PEG_GPU_D2R_P<7..0> 74 (MAKE_BASE=TRUE)
5 =PEG_D2R_N<7..0> — PEG_GPU_D2R_N<7..0> 74 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_P<7..0> — PEG_GPU_R2D_C_P<7..0> 74 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_N<7..0> — PEG_GPU_R2D_C_N<7..0> 74 (MAKE_BASE=TRUE)

Thunderbolt Signals Through PEG

5 =PEG_D2R_P<11..8> — PCIE_TBT_X_D2R_P<3..0> 26 (MAKE_BASE=TRUE)
5 =PEG_D2R_N<11..8> — PCIE_TBT_X_D2R_N<3..0> 26 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_P<11..8> — PCIE_TBT_X_R2D_C_P<3..0> 26 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_N<11..8> — PCIE_TBT_X_R2D_C_N<3..0> 26 (MAKE_BASE=TRUE)

SSD Signals Through PEG

5 =PEG_D2R_P<15..12> — PCIE_SSD_D2R_P<3..0> 32 (MAKE_BASE=TRUE)
5 =PEG_D2R_N<15..12> — PCIE_SSD_D2R_N<3..0> 32 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_P<15..12> — PCIE_SSD_R2D_C_P<3..0> 32 (MAKE_BASE=TRUE)
5 =PEG_R2D_C_N<15..12> — PCIE_SSD_R2D_C_N<3..0> 32 (MAKE_BASE=TRUE)

Unrouted Testpoints

12 TP_PM_SLP_A_L — NC_PM_SLP_A_L (MAKE_BASE=TRUE)

12 TP_PCH_SLP_WLAN_L — NC_PCH_SLP_WLAN_L (MAKE_BASE=TRUE)
12 TP_PCH_SLP_LAN_L — NC_PCH_SLP_LAN_L (MAKE_BASE=TRUE)

37 TP_ISM_RST_L — NC_ISM_RST_L (MAKE_BASE=TRUE)
37 TP_ISM_CLK — NC_ISM_CLK (MAKE_BASE=TRUE)

37 TP_CS_PWD_L — NC_CS_PWD_L (MAKE_BASE=TRUE)
6 TP_CPU_EOPIOVIEW0 — NC_CPU_RSVD_TP1 (MAKE_BASE=TRUE)
6 TP_CPU_EOPIOVIEW1 — NC_CPU_RSVD_TP2 (MAKE_BASE=TRUE)
6 TP_CPU_DDRVIEW0 — NC_CPU_RSVD_TP3 (MAKE_BASE=TRUE)
6 TP_CPU_EDRAMVIEW1 — NC_CPU_RSVD_TP4 (MAKE_BASE=TRUE)
6 TP_CPU_DDRVIEW1 — NC_CPU_RSVD_TP5 (MAKE_BASE=TRUE)
6 TP_CPU_EDRAMVIEW0 — NC_CPU_RSVD_TP6 (MAKE_BASE=TRUE)
6 TP_CPU_PEGVIEW1 — NC_CPU_RSVD_TP7 (MAKE_BASE=TRUE)
6 TP_CPU_PEGVIEW0 — NC_CPU_RSVD_TP8 (MAKE_BASE=TRUE)
6 TP_CPU_PEGVIEW3 — NC_CPU_RSVD_TP9 (MAKE_BASE=TRUE)
6 TP_CPU_PEGVIEW2 — NC_CPU_RSVD_TP10 (MAKE_BASE=TRUE)
6 TP_CPU_EANALOGVIEW0 — NC_CPU_RSVD1 (MAKE_BASE=TRUE)
6 TP_CPU_EANALOGVIEW1 — NC_CPU_RSVD2 (MAKE_BASE=TRUE)

6 TP_CPU_RSVD_TP12 — NC_CPU_RSVD_TP12 (MAKE_BASE=TRUE)
6 TP_CPU_RSVD_TP13 — NC_CPU_RSVD_TP13 (MAKE_BASE=TRUE)
6 TP_CPU_RSVD_TP14 — NC_CPU_RSVD_TP14 (MAKE_BASE=TRUE)
6 TP_CPU_RSVD_TP15 — NC_CPU_RSVD_TP15 (MAKE_BASE=TRUE)

11 TP_PCH_GPP_D17 — NC_PCH_GPP_D17 (MAKE_BASE=TRUE)
11 TP_PCH_GPP_D18 — NC_PCH_GPP_D18 (MAKE_BASE=TRUE)
11 TP_PCH_GPP_D19 — NC_PCH_GPP_D19 (MAKE_BASE=TRUE)
11 TP_PCH_GPP_D20 — NC_PCH_GPP_D20 (MAKE_BASE=TRUE)
14 TP_PCH_GPP_D23 — NC_PCH_GPP_D23 (MAKE_BASE=TRUE)

12 TP_CLINK_RESET_L — NC_CLINK_RESET_L (MAKE_BASE=TRUE)
12 TP_CLINK_DATA — NC_CLINK_DATA (MAKE_BASE=TRUE)
12 TP_CLINK_CLK — NC_CLINK_CLK (MAKE_BASE=TRUE)
37 TP_CAM_GPIO1 — NC_CAM_GPIO1 (MAKE_BASE=TRUE)

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Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00154	PCBA,MLB,DEV,X647	DEVELOPMENT,X647_DEVEL
685-00101	PCBA,MLB,COMMON PARTS,X647	X647_COMMON
639-03385	PCBA,MLB,3.0G,HDD,BF_LEA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:N,GPU:BF_LEA,FB:2GB_HYNIX
639-03386	PCBA,MLB,3.0G,HDD,BF_LEA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:N,GPU:BF_LEA,FB:2GB_SAMSUNG
639-03387	PCBA,MLB,3.0G,SSD,BF_LEA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:Y,GPU:BF_LEA,FB:2GB_HYNIX
639-03388	PCBA,MLB,3.0G,SSD,BF_LEA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:Y,GPU:BF_LEA,FB:2GB_SAMSUNG
639-03389	PCBA,MLB,3.6G,HDD,BF_LEA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:N,GPU:BF_LEA,FB:2GB_HYNIX
639-03390	PCBA,MLB,3.6G,HDD,BF_LEA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:N,GPU:BF_LEA,FB:2GB_SAMSUNG
639-03391	PCBA,MLB,3.6G,SSD,BF_LEA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_LEA,FB:2GB_HYNIX
639-03392	PCBA,MLB,3.6G,SSD,BF_LEA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_LEA,FB:2GB_SAMSUNG
639-03393	PCBA,MLB,3.4G,SSD,BF_PROA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.4,SSD:Y,GPU:BF_PROA,FB:2GB_HYNIX
639-03394	PCBA,MLB,3.4G,SSD,BF_PROA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.4,SSD:Y,GPU:BF_PROA,FB:2GB_SAMSUNG
639-03395	PCBA,MLB,3.4G,SSD,BF_XLA,FB_4GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.4,SSD:Y,GPU:BF_XLA,FB:4GB_HYNIX
639-03396	PCBA,MLB,3.4G,SSD,BF_XLA,FB_4GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.4,SSD:Y,GPU:BF_XLA,FB:4GB_SAMSUNG
639-03397	PCBA,MLB,3.6G,SSD,BF_PROA,FB_2GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_PROA,FB:2GB_HYNIX
639-03398	PCBA,MLB,3.6G,SSD,BF_PROA,FB_2GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_PROA,FB:2GB_SAMSUNG
639-03399	PCBA,MLB,3.6G,SSD,BF_XLA,FB_4GB_HY,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_XLA,FB:4GB_HYNIX
639-03400	PCBA,MLB,3.6G,SSD,BF_XLA,FB_4GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.6,SSD:Y,GPU:BF_XLA,FB:4GB_SAMSUNG

BOM Variants, Socket Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-03164	PCBA,MLB,3.0G,SSD,BF_SKT_VCORE,FB_4GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:Y,GPU:SKT_VCORE,FB:4GB_SAMSUNG
639-03165	PCBA,MLB,3.0G,SSD,BF_SKT_VDDCI,FB_4GB_SA,X647	MLB_CMNPTS,ALTERNATE,ALT_CMN,CPU:KBL_3.0,SSD:Y,GPU:SKT_VDDCI,FB:4GB_SAMSUNG

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