Compal Confidential

Model Name : C4PB1/C5PB1
File Name : TBD
BOM P/N:43

ZZZ
LA-E591P MB
DAA000DD000
DA2@

ZZZ1
LS-D303P FUN/B
DA400299000
DAS@

ZZZ2
LS-D302P USB/B
DA6001HX000
DAS@

ZZZ3
LS-A133P
DA600101010
DAS@

ZZZ4
LS-D301P LID/B
DA400272000
DAS@

ZZZ5
LS-B734P
DA6001B8010
DAS@

ZZZ5
HDMI LOGO
RO0000003HM
HDMI@

ZZZ
LS-B732P
DA4001YF010
DAS@

ZZZ
DAZ PCB
DAZ1IB00100
DAZ@

Compal Confidential

C4PB1/C5PB1
M/B Schematics Document

Kabylake U Processor + DDR4 + Nvidia N16X

2016-12-15

Rev:1.0

UC1
S IC FJ8067702739738 SR2ZW H0 2.4G ABO!
CPU_3860@
SA0000A3860

UC1
S IC FJ8067702739738 QLDP H0 2.4G BGA
CPU_3820@
SA0000A3820

UC1
S IC FJ8067702739739 SR2ZU H0 2.5G ABO!
CPU_3760@
SA0000A3760

UC1
S IC FJ8067702739739 QLDM H0 2.5G BGA
CPU_3720@
SA0000A3720

UC1
S IC FJ8066201924931 SR2F0 D1 2.4G ABO!
CPU_2T80@
SA000092T80

UC1
S IC FJ8067702739741 QLDU H0 2.6G BGA
CPU_3L20@
SA0000A3L20

UC1
S IC FJ8067702739740 SR2ZV H0 2.7G ABO!
CPU_3450@
SA0000A3450

UC1
S IC FJ8067702739633 QLYG H0 2.6G BGA
CPU_DO10@
SA0000ADO10

UC1
S IC FJ8067702739628 QLYF H0 2.8G BGA
CPU_DP10@
SA0000ADP10

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

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Title: Cover Page

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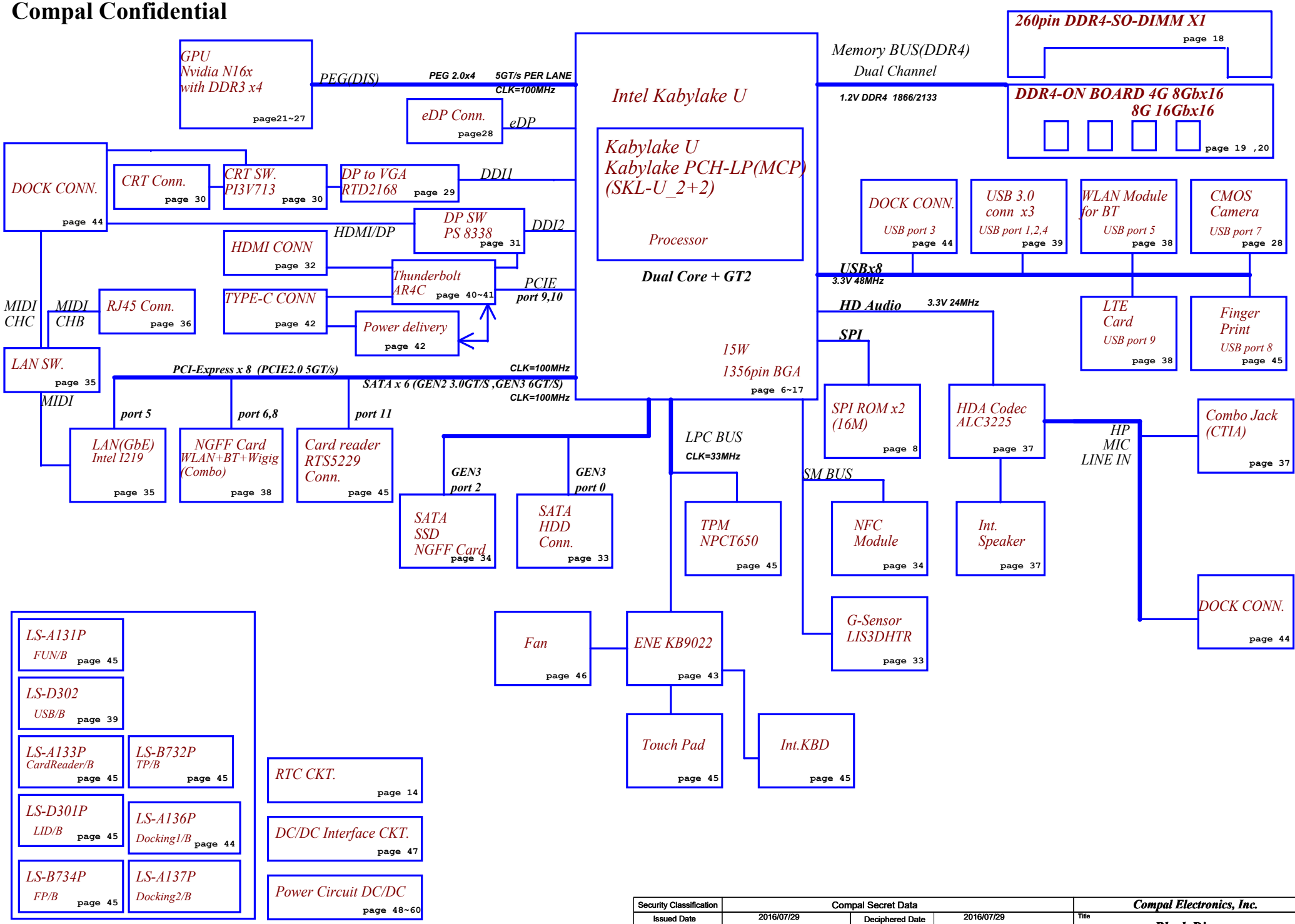

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Title: **Block Diagrams**

Size	Document Number	Rev
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	Res	Vbrd	PCB version	Project	Note
EVT	0K	0v	0.1	P6	
PVT	12k	0.345V	0.2		
PreMP	15k	0.430V	1		

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
EMI requirement	@EMC@/EMI@
Thunderbolt Function	TBT@
RF requirement	@RF@/RF@
LTE Function	3G@
UMA only	UMA@
VPRO Function	VPRO@/NOVPRO@
VGA EMI Requirement	@VGA_EMI@/VGA_EMI@
VGA UNPOP	@VGA@
VGA RF Requirement	@RF@_VGA@
VGA Power	22@/23E@
GC6 Function	GC6@/NOGC6@/NGC6
INTEL CMC	CMC@
ESPI	ESPI @

BOM Option Table	
Item	BOM Structure
dGPU	VGA@
ON Board DDR4	X76OBRAM@
N16S-GT	SGT@
Without WiGi Function	NOWG@
HDD Redriver	X76TI@/X76PAR@
GPU CG6 function	VGM@
VRAM BOM Select	X76@
Single/Dual Rank	SR@/DR@ (DR@ is not been used in this project)
PD Function	PD@
CPU Code	QH7Y@
CPU Code	QH7Y@

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON	OFF	OFF
+2.5V	DDR4 +2.5V Power Rail	ON	ON	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

I2C Address Table

BUS	Device	8Bit Read/Write
SOC_SMBCLK_1 +3VS	JDIMM1	A4/A5
SOC_SMBCLK_1 +3VS	Gsensor U26	30/31
SOC_SML0CLK +3VS	JNFC1	52/53
SOC_SML0CLK +3V_LAN	LAN UL1	C8/C9
SOC_SML1CLK_1 +3VSDGPU_MAIN	UGPU1	9E/9F
SOC_SML1CLK_1 +3VS	Thermal Sensor UU24	98/99
SOC_SML1CLK_1 +3VS	PCH_LP	90/91
EC_SMB_CK1 +3VLP_EC	PD U5007	70/71
EC_SMB_CK1 +3VLP_EC	Battery PJP201	16/17
EC_SMB_CK1 +3VLP_EC	Charger PU301	12/13

Vinafix

43 level BOM table

43 Level	Description	BOM Structure
431A0NBOL01	SMT MB AD301 B4DBG QJFC 2.3G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL02	SMT MB AD301 B4DBG QJ8M 2.4G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL03	SMT MB AD301 B4DBG QJKP 2.3G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@
431A0NBOL04	SMT MB AD301 B4DBG QJKK 2.5G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@

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Issued Date	2016/07/29	Deciphered Date 2016/07/29	Title: Notes List

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		Document Number	C4PB1/C5PB1 LA-E591P
		Rev	1A
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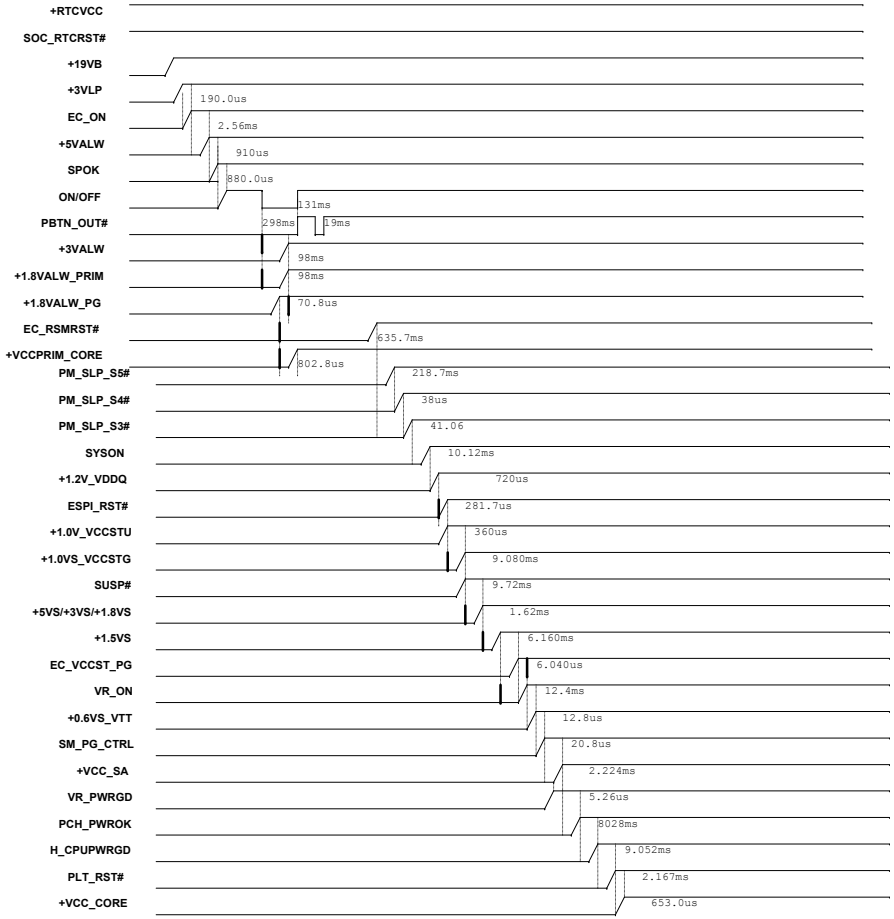
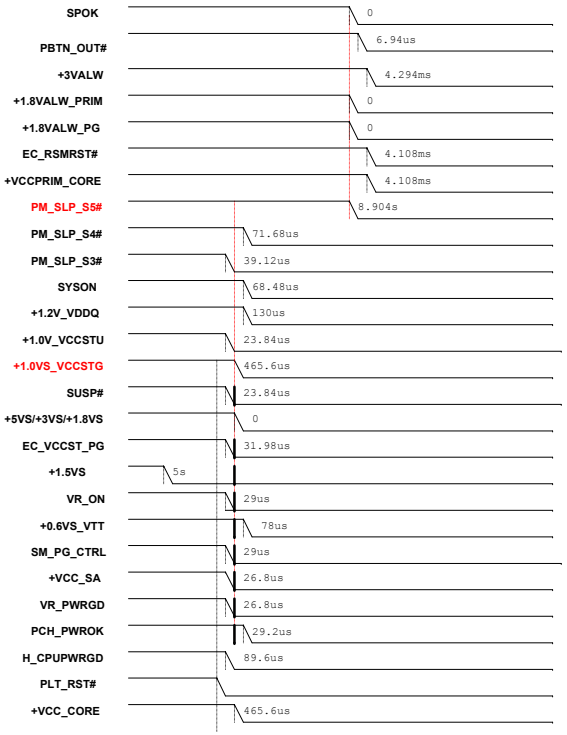
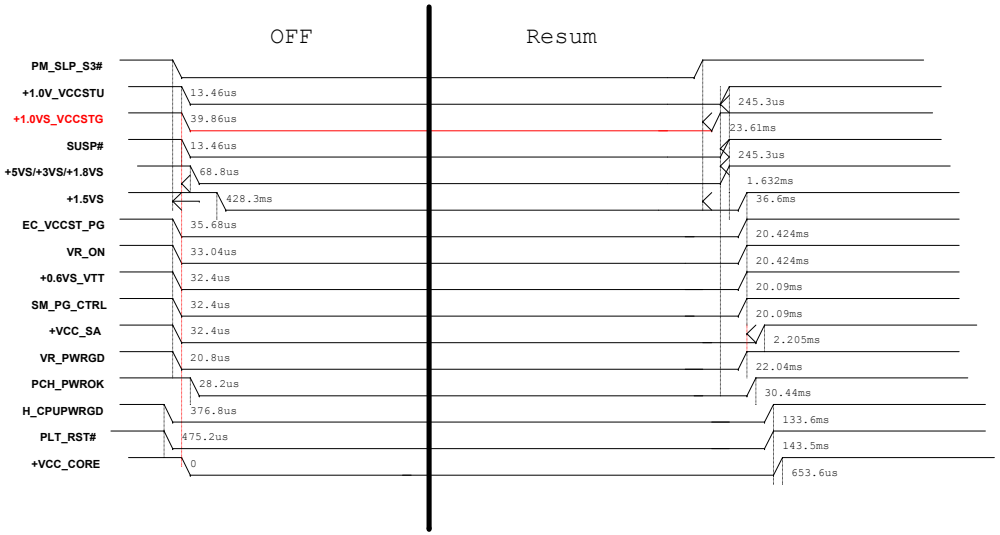
C4PB1/C5PB1 Power on sequence



C4PB1/C5PB1 Power OFF sequence



C4PB1/C5PB1 S3 sequence



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Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: Power Sequence			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
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Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.

<DP to VGA>

< PS8338 >
Docking HDMI+TBT

UC1A SKL-U Rev_0.53

DDI1_TXN[0] E55
DDI1_TXP[0] F55
DDI1_TXN[1] E58
DDI1_TXP[1] F58
DDI1_TXN[2] F53
DDI1_TXP[2] G53
DDI1_TXN[3] F56
DDI1_TXP[3] G56
DDI2_TXN[0] C50
DDI2_TXP[0] D50
DDI2_TXN[1] C52
DDI2_TXP[1] D52
DDI2_TXN[2] A50
DDI2_TXP[2] B50
DDI2_TXN[3] D51
DDI2_TXP[3] C51

DDI

EDP_TXN[0] C47
EDP_TXP[0] C46
EDP_TXN[1] D46
EDP_TXP[1] C45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47
EDP_AUXN E45
EDP_AUXP F45
EDP_DISP_UTIL B52

EDP

DISPLAY SIDEBANDS

GPP_E18/DDPB_CTRLCLK L13
GPP_E19/DDPB_CTRLDATA L12
GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N8
GPP_E22/DDPD_CTRLCLK N11
GPP_E23/DDPD_CTRLDATA N12
EDP_RCOMP E52

1 OF 20

SKL-U_BGA1356

@

EDP_TXN0 <28>
EDP_TXP0 <28>
EDP_TXN1 <28>
EDP_TXP1 <28>
EDP_TXN2 <28>
EDP_TXP2 <28>
EDP_TXN3 <28>
EDP_TXP3 <28>

<eDP>

EDP_AUXN <28>
EDP_AUXP <28>

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP G46

SOC_DP1_AUXN
SOC_DP1_AUXP
SOC_DP2_AUXN
SOC_DP2_AUXP

SOC_DP1_AUXN <29>
SOC_DP1_AUXP <29>
DDI2_AUX_DN <31>
DDI2_AUX_DP <31>

DP Aux (Port B for VGA)
PS8338

GPP_E13/DDPB_HPD0 L9
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10

SOC_DP1_HPD
CPU_HDMI_HPD
EC_SCI#
CPU_EDP_HPD

SOC_DP1_HPD <29>
CPU_HDMI_HPD <31>
EC_SCI# <43>
CPU_EDP_HPD <28>

From VGA Trans.
From DP MUX
From eDP

EDP_BKLTEN R12
EDP_BKLTCTL R11
EDP_VDDEN U13

ENBKL
SOC_BKL_PWM
SOC_ENVDD

ENBKL <43>
SOC_BKL_PWM <28>
SOC_ENVDD <28>

+3VS

RC212 10K_0402_5%
EC_SCI# 1 @ 2

EC_SCI# SOC internal PU

COMPENSATION PU FOR eDP

+VCCIO
RC1 1 2 EDP_COMP 24.9_0402_1%

#543016 PDG0.9 P.186
Trace width=20 mils,Spacing=25mil,Max length=100mils

+1.0V_VCCST

#543016 PDG0.9 P.753
PH 1K to VCCST
CPU over 130 degree will output low force S0->S5

RC2 1 2 THERMTRIP# 1K_0402_5%

+1.0VS_VCCSTG

RC3 1K_0402_5% follow INTEL check list to reserve D63 test point

<43,50> H_PROCHOT# RC4 499_0402_1%

@ T167 CATERR# D63
H_PECI A54
H_PROCHOT#_R C65
H_THERMTRIP# C63
A65

@ T160 XDP_BPM#0 C55
@ T161 XDP_BPM#1 D55
B54
C56

@ T170 I2C_TS_INT# A6
A7
@ T169 B45
AY5

<35,44> DET_SIG#_R

RC5 49.9_0402_1% CPU_POPIRCOMP AT16
RC6 49.9_0402_1% PCH_OPIRCOMP AU16
RC7 49.9_0402_1% EDRAM_OPIO_RCOMP H66
RC8 49.9_0402_1% EOPIO_RCOMP H65

UC1D SKL-U Rev_0.53

CATERR# B61
PECI A61
PROCHOT# C60
THERMTRIP# B59
SKTOCC#

CPU MISC

BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

4 OF 20

SKL-U_BGA1356

@

JTAG

PROC_TCK B56
PROC_TDI D59
PROC_TDO A56
PROC_TMS C59
PROC_TRST# C61
JTAGX A59

CPU_XDP_TCK0
SOC_XDP_TDI
SOC_XDP_TDO
SOC_XDP_TMS
SOC_XDP_TRST#
PCH_JTAG_TCK1
SOC_XDP_TDI
SOC_XDP_TDO
SOC_XDP_TMS
SOC_XDP_TRST#
CPU_XDP_TCK0

#545659 PCH EDS 0.7 P.108
SCI capability is available on all GPIOs,
while NMI and SMI capability is available on selected GPIOs only.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0], GPP_E[16:13]

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
59	GND	GND	NA		60	GND[2] (XDP_PRESENT#)	See XDP_PRESENT# routing guidelines	NA	system

Notes:
1. These signals are optional, can be left as OPEN/No-Connect.
2. See XDP_PRESENT# section for additional routing guidelines.
3. Routing of this signal to CFG[2] is OPTIONAL.

9	OBSDATA_A0	CFG[0]	I/O	Skylake	10	OBSDATA_C0	CFG[8]	I/O	Skylake
11	OBSDATA_A1	CFG[1]	I/O	Skylake	12	OBSDATA_C1	CFG[9]	I/O	Skylake
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	CFG[2]	I/O	Skylake	16	OBSDATA_C2	CFG[10]	I/O	Skylake
17	OBSDATA_A3	CFG[3]	I/O	Skylake	18	OBSDATA_C3	CFG[11]	I/O	Skylake
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	BPM#[0]	I/O	Skylake	22	OBSFN_D0	CFG[19]	I	Skylake
23	OBSFN_B1	BPM#[1]	I/O	Skylake	24	OBSFN_D1	CFG[18]	I	Skylake
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	CFG[4]	I/O	Skylake	28	OBSDATA_D0	CFG[12]	I/O	Skylake
29	OBSDATA_B1	CFG[5]	I/O	Skylake	30	OBSDATA_D1	CFG[13]	I/O	Skylake
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	CFG[6]	I/O	Skylake	34	OBSDATA_D2	CFG[14]	I/O	Skylake
35	OBSDATA_B3	CFG[7]	I/O	Skylake	36	OBSDATA_D3	CFG[15]	I/O	Skylake
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	ASMRST#	I	Skylake	40	ITPCLK/HOOK4	CLKOUT_ITPX_DP_P	I	Skylake
41	HOOK1	PWRBTN#	O	Skylake	42	ITPCLK#/HOOK5	CLKOUT_ITPX_DP_N	I	Skylake
43	VCC_OBS_AB	PCH V1.0A	NA		44	VCC_OBS_CD	PCH V1.0A	NA	
45	HOOK2[3]	Open	NA		46	HOOKE/RESET#	ITP_PMODE	I	Skylake
47	HOOK3[3]	SPIO_MOSI	O	Skylake	48	HOOK7/OBS#4	SYS_RESET#4	O	Skylake
49	GND	GND	NA		50	GND	GND	NA	
51	XDP_SDA[3]	SDA	I/O	system	52	XDP_TDO	PROC_TDO / PCH_JTAG_TDO	I	Skylake
53	XDP_SCL[3]	SCL	I/O	system	54	XDP_TRSTn	PROC_TRST#/ PCH_TRST#	O	Skylake
55	XDP_TCK1	PCH_JTAG_TCK	O	Skylake	56	XDP_TDI	PROC_TDI / PCH_JTAG_TDI	O	Skylake
57	XDP_TCK0	PROC_TCK / JTAGX	O	Skylake	58	XDP_THS	PROC_THS / PCH_JTAG_TMS	O	Skylake

CC52 @EMC@ .1U_0402_16V7K H_PECI
CC53 @EMC@ .1U_0402_16V7K H_PROCHOT#_R
Reserved for ESD 2014/9/17

PDG0.9 P.771
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB RVP7 1.0
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD50ohm

APS CONN

+3VALW +3VALW_PRIM

JAPS1
ACES_50506-01841-P01
CONN@

<10,43,47> PM_SLP_S3#
<10> PM_SLP_S5#
<10,43,47> PM_SLP_S4#
<10,43> PM_SLP_A#
<10> SOC_RTCRST#
PBTN_OUT#_R2
<10> SYS_RESET#
<10> PM_SLP_S0#

Place to CPU side

+1.0V_XDP

RC31 1 CMC@ 2 1K_0402_5% XDP_ITP_PMODE
RC43 2 @ 1 0_0402_5% XDP_PRSENT_CPU
RC46 2 @ 1 0_0402_5% XDP_PRSENT_PCH
RC35 2 CMC@ 1 51_0402_1% CPU_XDP_TCK0
RC37 2 @ 1 51_0402_5% PCH_JTAG_TCK1
RC151 2 @ 1 1K_0402_5% CFG0

Follow 544924_Skylake_EDS_Vol_1_Rev_0.93

+3VALW_PRIM
RC9 1 CMC@ 2 1K_0402_5% XDP_SPI_SI

+1.0VS_VCCSTG

RC11 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC13 2 CMC@ 1 51_0402_5% SOC_XDP_TDI
RC15 2 CMC@ 1 51_0402_5% SOC_XDP_TDO

Place to CPU side

CMC@ RPC2
SOC_XDP_TMS 1 8 XDP_TMS
SOC_XDP_TDI 2 7 XDP_TDI
SOC_XDP_TRST# 3 6 XDP_TRST#
SOC_XDP_TDO 4 5 XDP_TDO
0_0804_8P4R_5%

<17> XDP_ITP_PMODE
CFG3 XDP_ITP_PMODE
RC55 1 @ 2 0_0402_5% XDP_PRSENT_CPU
RC56 1 @ 2 0_0402_5% XDP_HOOK6

<8> XDP_SPI_SI
<8> XDP_SPI_IO2

CMC@ RPC15
XDP_SPI_SI 1 8 XDP_HOOK3
PCH_JTAG_TCK1 2 7 XDP_TCK1
CPU_XDP_TCK0 3 6 XDP_TCK0
XDP_SPI_IO2 4 5 XDP_PRSENT_PCH
0_0804_8P4R_5%

<10,43> EC_RSMRST#
EC_RSMRST# RC23 1 CMC@ 2 1K_0402_5% XDP_HOOK0

XDP CONN

+1.0VALW_PRIM +1.0V_XDP
RC12 1 @ 2 0_0603_5%

JPCMC1 CMC_DEBUG_36P
INTEL_CMC_PRIMARY
CONN@

OBS DATA
JTAG/RC/HOOKS

<17> CFG0 CFG0 1 DATA_0
<17> CFG1 CFG1 3 DATA_1
<17> CFG2 CFG2 5 DATA_2
<17> CFG3 CFG3 7 DATA_3
<17> CFG4 CFG4 9 DATA_4
<17> CFG5 CFG5 11 DATA_5
<17> CFG6 CFG6 13 DATA_6
<17> CFG7 CFG7 15 DATA_7
DATA_CLK_1P
DATA_CLK_1N
DATA_8
DATA_9
<17> CFG10 DATA_10
<17> CFG11 DATA_11
<17> CFG12 DATA_12
<17> CFG13 DATA_13
<17> CFG14 DATA_14
<17> CFG15 DATA_15
<17> CFG17 CFG17 17
<17> CFG16 CFG16 21
DATA_CLK_2P
DATA_CLK_2N
<17> CFG8 CFG8 2
<17> CFG9 CFG9 4
<17> CFG19 CFG19 18
<17> CFG18 CFG18 20

+1.0V_XDP
VCCOBS_AB 22

XDP_TRST* 28 XDP_TRST#
XDP_TDI 29 XDP_TDI
XDP_TMS 30 XDP_TMS
XDP_TCK0 32 XDP_TCK0
XDP_TCK1 31 XDP_TCK1
XDP_TDO 35 XDP_TDO
XDP_PREQ* 33 XDP_PREQ#
XDP_PRDY* 34 XDP_PRDY#
HOOK_0 27 XDP_HOOK0
HOOK_3 25 XDP_HOOK3
HOOK_6 26 XDP_HOOK6
XDP_PRSNT_PCH* 24 XDP_PRSENT_PCH
XDP_PRSNT_CPU* 23 XDP_PRSENT_CPU
GND 19
<MT> GND 36

XDP_PREQ# <12>
XDP_PRDY# <12>

<10,43> PBTN_OUT#
<43,45> ON/OFF#
RC53 2 @ 1 0_0402_5% PBTN_OUT#_R
RC54 2 @ 1 0_0402_5%
use for iAMT Test

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

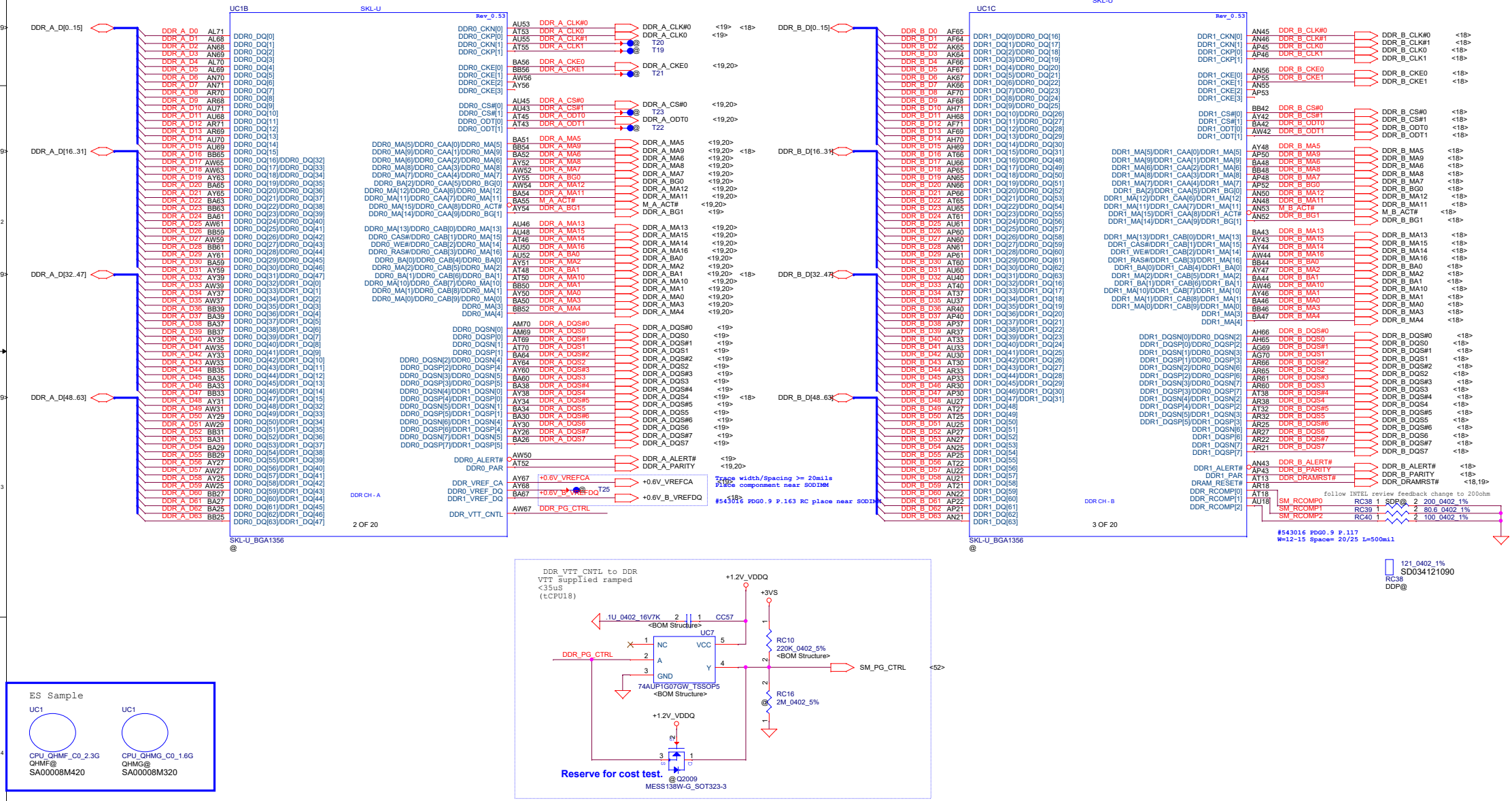
Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

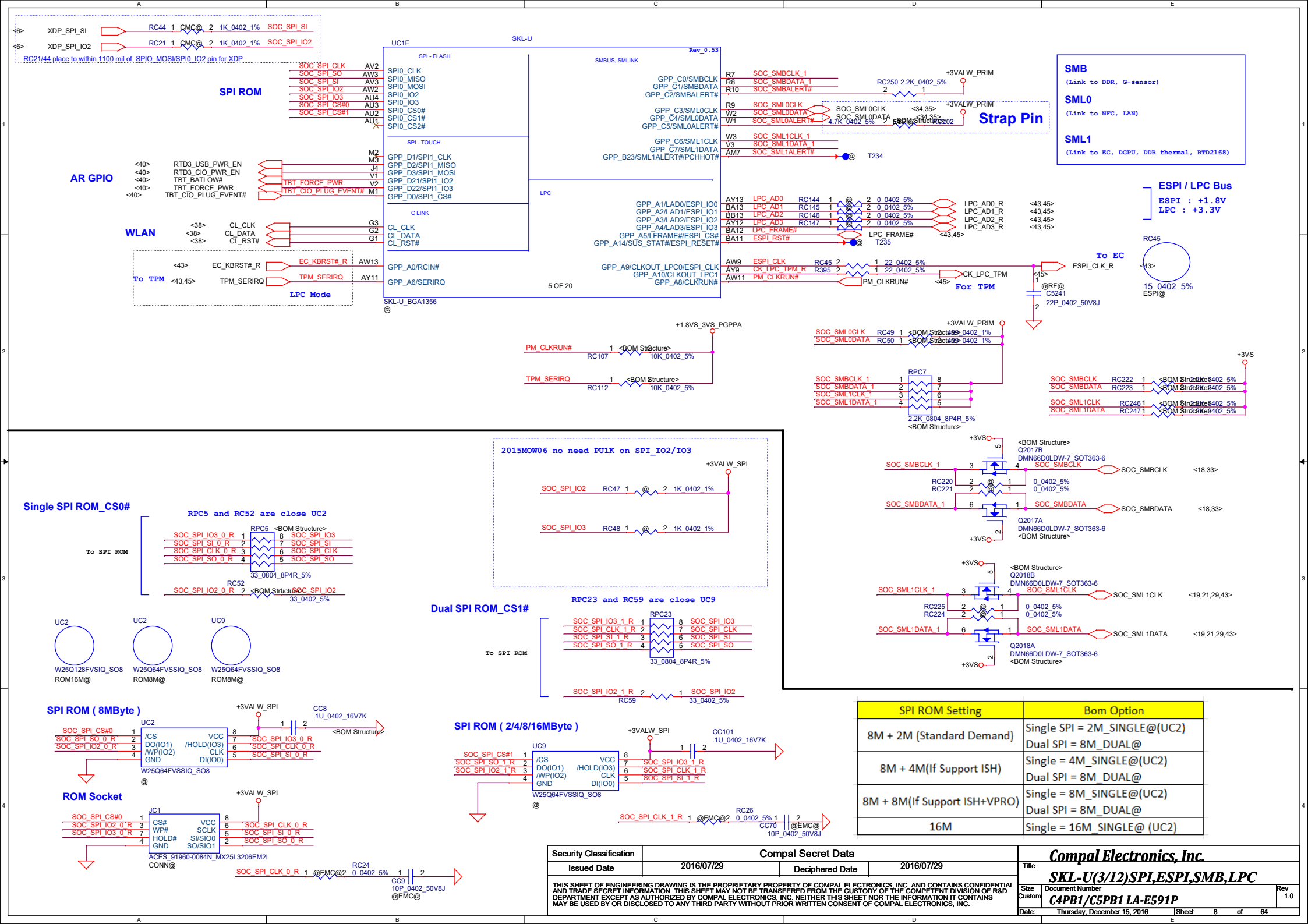
Date: Thursday, December 15, 2016 Sheet 6 of 64

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: SKL-U(2/12)DDR			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 7 of 64		



SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.	
Title	SKL-U(3/12)SPI,ESPI,SMB,LPC
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P
Rev	1.0
Date: Thursday, December 15, 2016	Sheet 8 of 64

#545659 SKL_PCH_EDS_R0.7 P.84

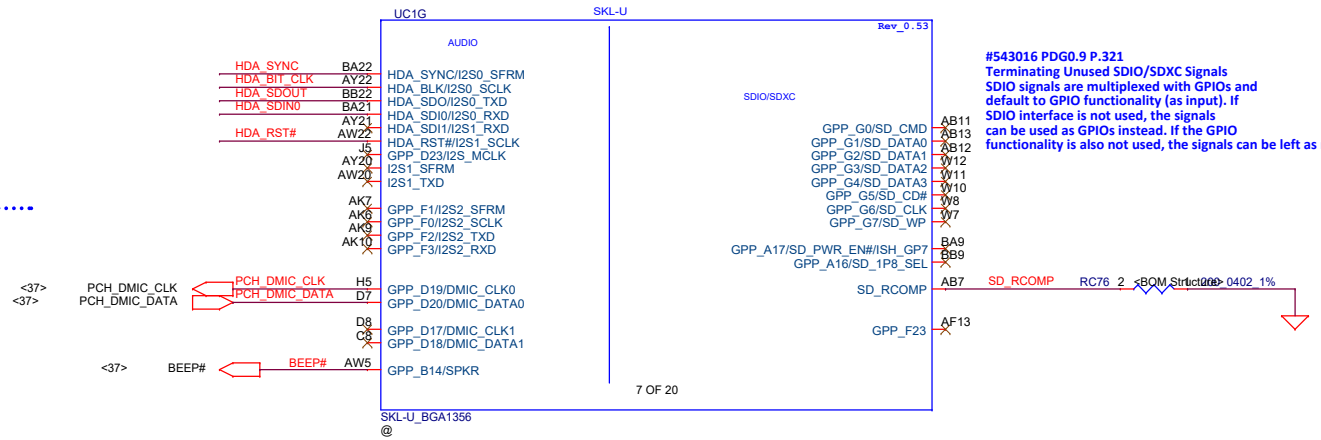
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.



#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

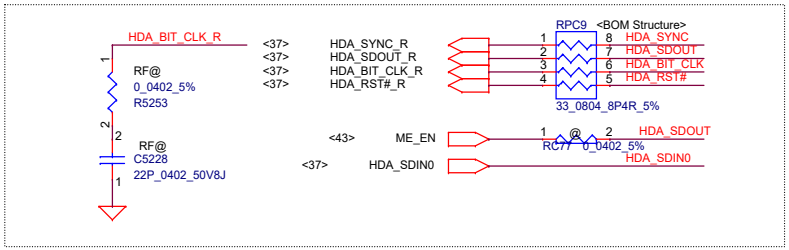
62.3.38 RCOMP Checklist

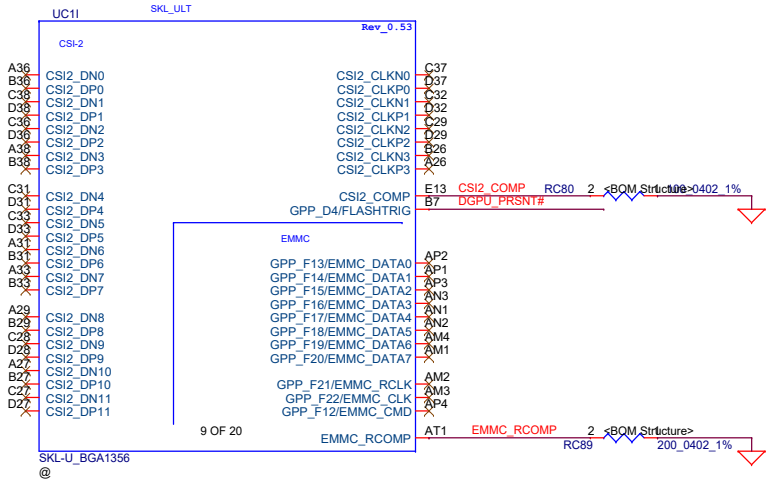
Table 62-48. RCOMP Checklist

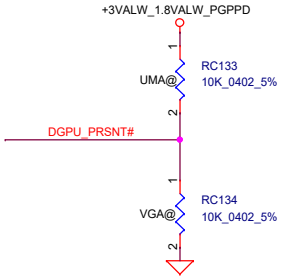
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

HDA for AUDIO

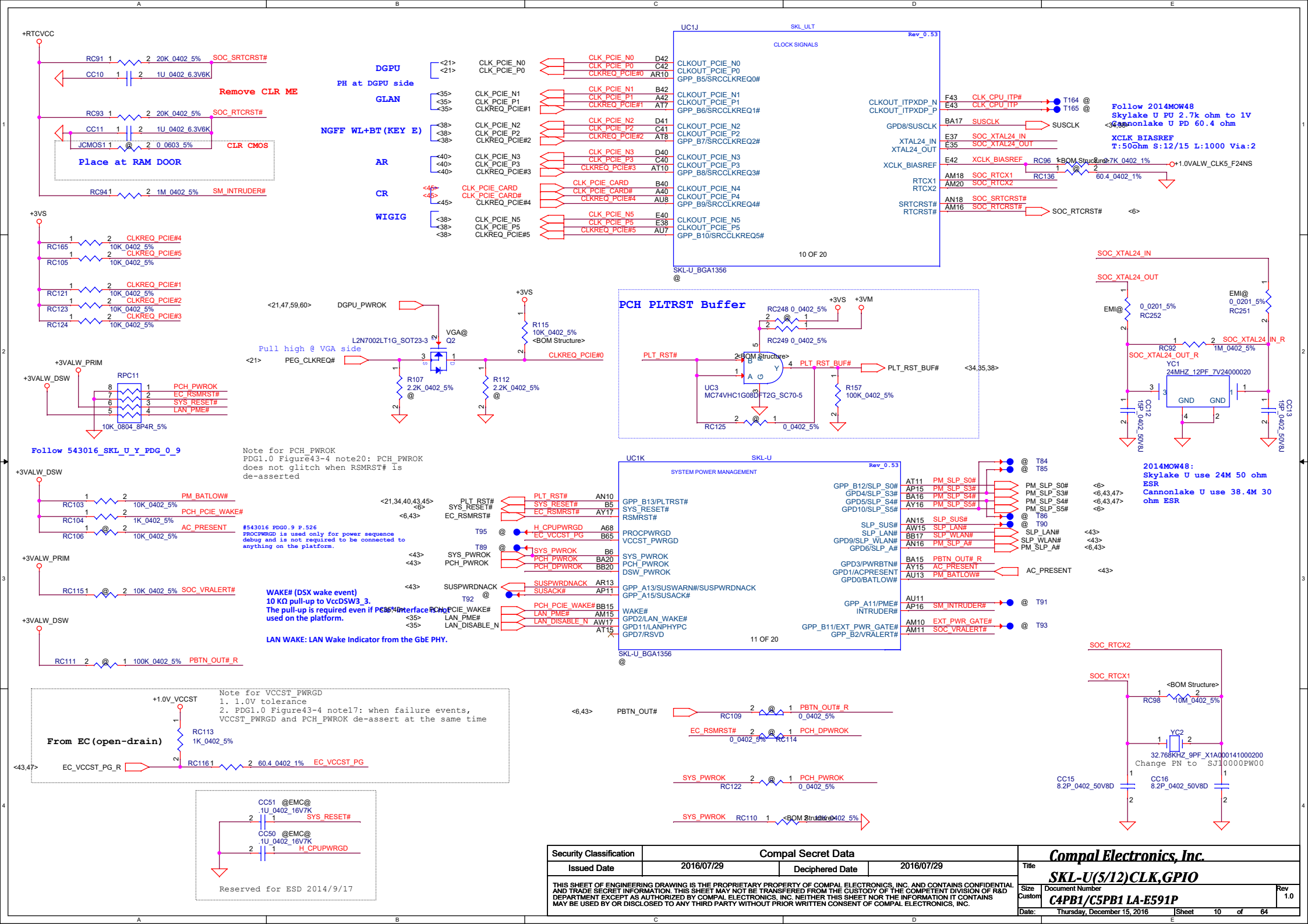






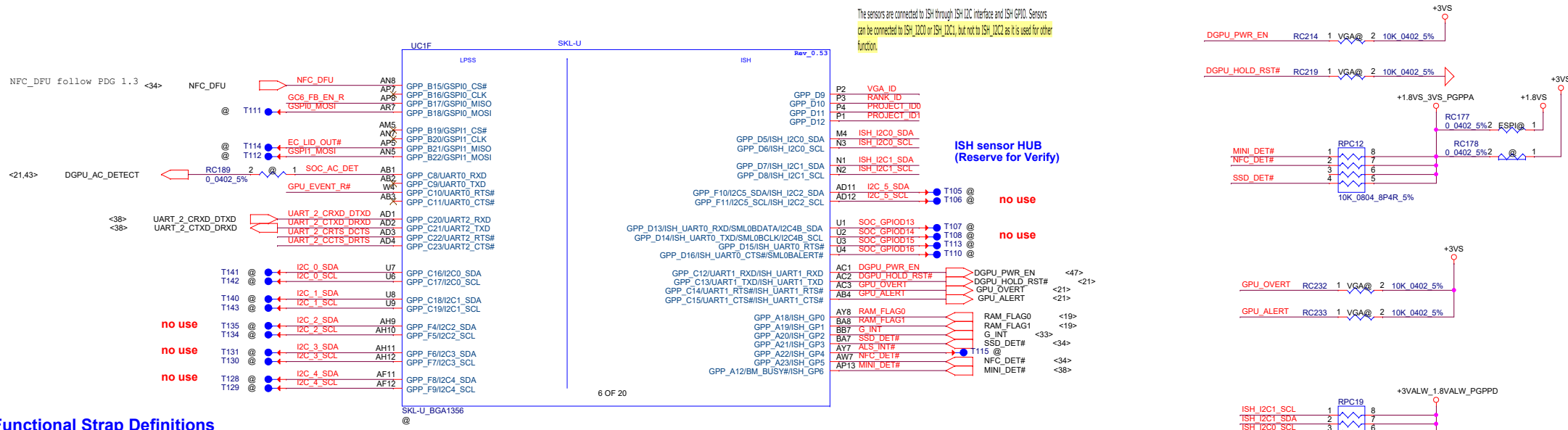
	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

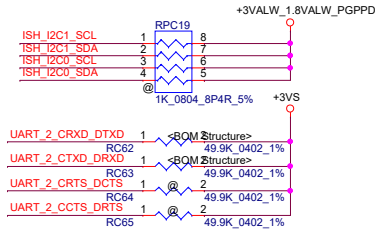
Compal Electronics, Inc.			
Title	SKL-U(4/12)HDA,EMMC,SDIO,CSI2		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 9 of 64		

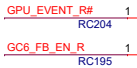


Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

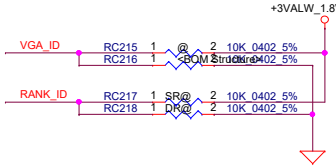
Compal Electronics, Inc.			
Title: SKL-U(5/12)CLK,GPIO			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 10 of 64		

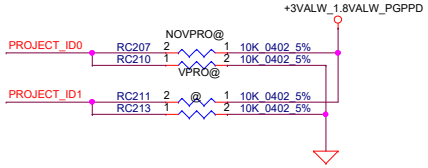






TO DGPU





Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
*** 0 = Disable TOP Swap mode.---> AAX05 Use**
1 = Enable TOP Swap Mode.

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*** 0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*** 0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
*** 0 = LPC is selected for EC --> For KB9022/9032 Use**
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
*** 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).**
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

VGA_ID	GPP_D9
GL	0
GM	1

RANK_ID	GPP_D10
DR	0
SR	1

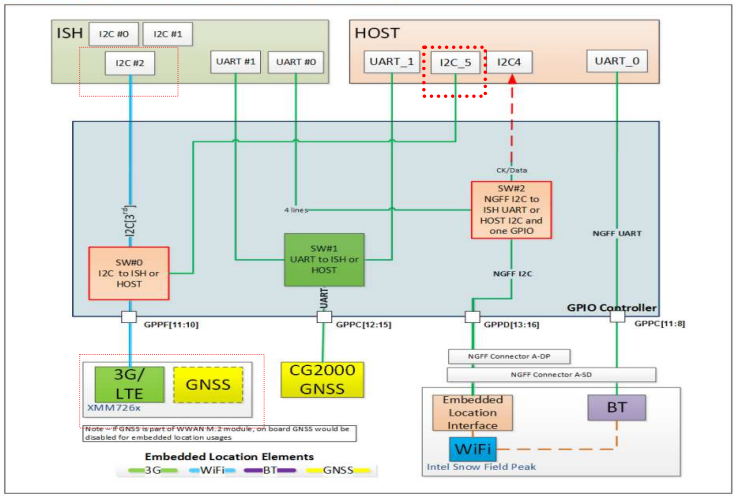
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*B4DBU+VPRO	0	0
B4DBU+NVPRO	0	1
Reserved	1	0
Reserved	1	1

HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port D is not detected.
1 =Port D is detected.

I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.	
Title	SKL-U(6/12)GPIO
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P
Rev	1.0
Date: Thursday, December 15, 2016	Sheet 11 of 64

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC / USB3

USB2

8 OF 20

SKL-U_BGA1356

@

DGPU

GLAN

NGFF WLAN+BT(Key E)

HDD

Wigig

Thunderbolt

CR

SSD

#543016 P.239 PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12 S=12 R=100ohm

RC120 1K_0402_1%

RC135 10K_0402_5%

+3VALW_PRIM

PIRQA#

XDP_PRDY#

XDP_PREQ#

PCH_USB3_RX1 IO/B

PCH_USB3_TX1 IO/B

PCH_USB3_RX2 / PCH_USB3_TX2 USB3 MB

PCH_USB3_RX3 / PCH_USB3_TX3 DOCKING

PCH_USB3_RX4 IO/B

PCH_USB3_TX4 IO/B

USB20_N1 IO/B

USB20_P1 IO/B

USB20_N2 USB3 MB

USB20_P2 USB3 MB

USB20_N3 DOCKING

USB20_P3 DOCKING

USB20_N4 IO/B

USB20_P4 IO/B

USB20_N5 BT

USB20_P5 BT

T26

T27

USB20_N7 Camera

USB20_P7 Camera

USB20_N8 FP

USB20_P8 FP

USB20_N9 LTE

USB20_P9 LTE

AG3,AG4 PD1K for DCI warm boot fail issue (follow PCH EDS1.2)
2015MOW10, USB2_ID connected to GND

USB_OC0# <39>

T166 @

NFC_IRQ <34>

NFC_IRQ,RST# follow PDG 1.3

NFC_RST# <34>

DEVSLP2 <34>

PCH_SATALED# <45>

+3VALW_PRIM

USB_OC0# RC1321 2 10K_0402_5%

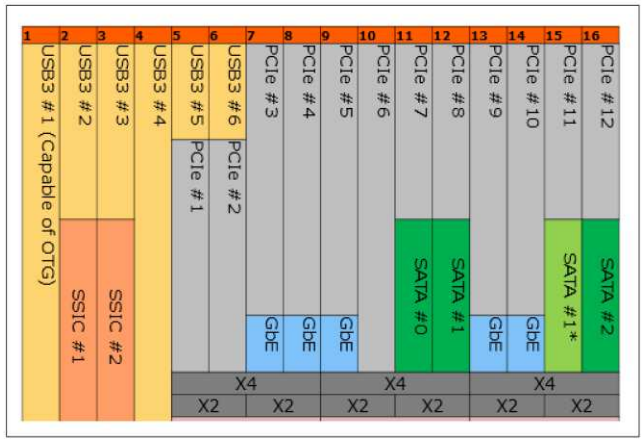
+3VS

PCH_SATALED# RC1391 2 10K_0402_5%

NFC_RST# RC1381 2 10K_0402_5%

DEVSLP2 RC2011 2 10K_0402_5%

High Speed I/O (HSIO) Lane Multiplexing in SKL U



Acer HSIO define

3.3 Intel SKYLAKE one chip.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1,2,4
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	SSD
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
• When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
• When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
• The processor provides three SATA general purpose input signals,SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
• When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
• If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

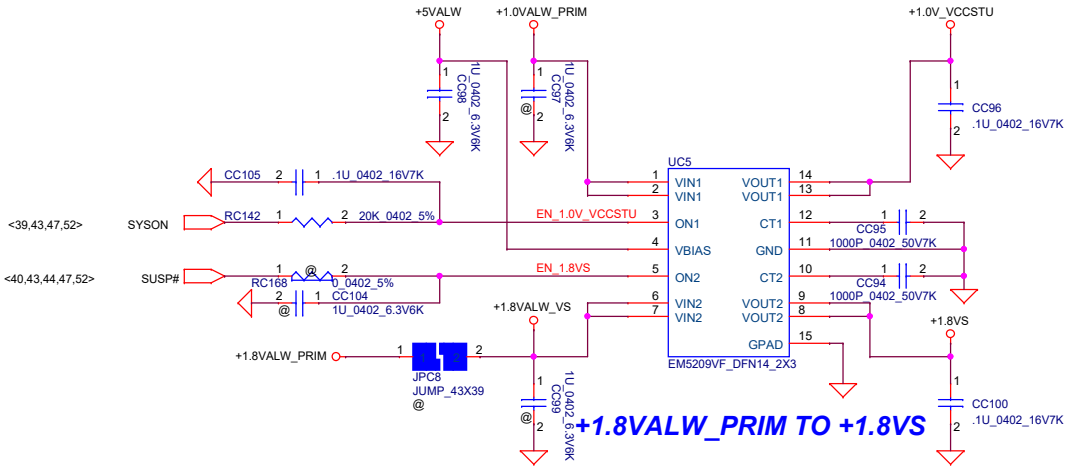
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

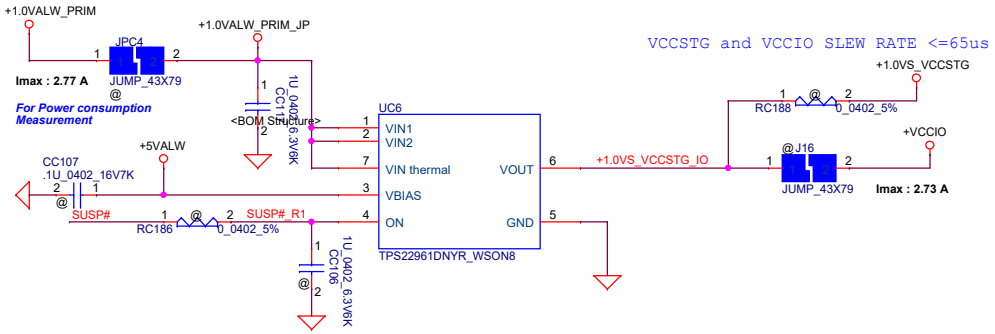
Date: Thursday, December 15, 2016 | Sheet 12 of 64

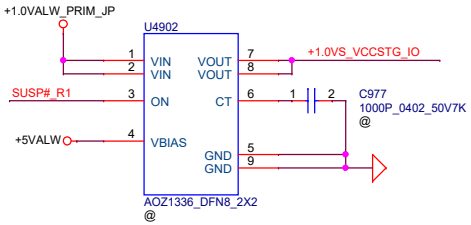
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

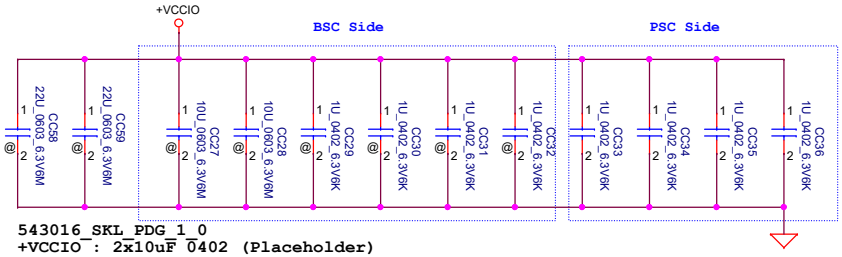


+1.8VALW_PRIM TO +1.8VS

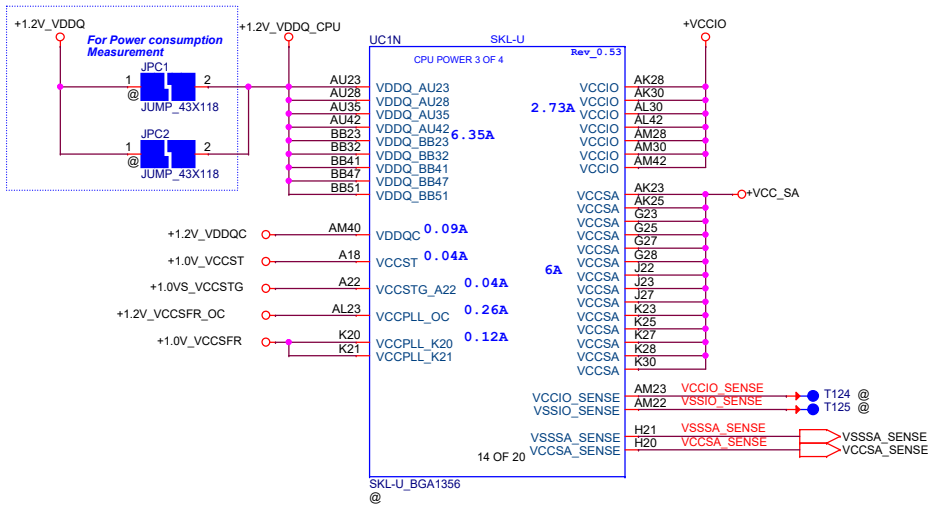
+1.0VALW_PRIM TO +1.0VS_VCCSTG

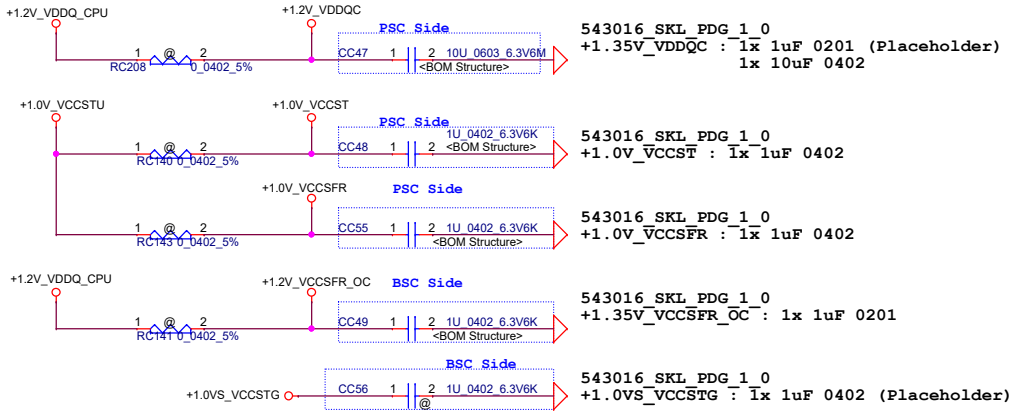


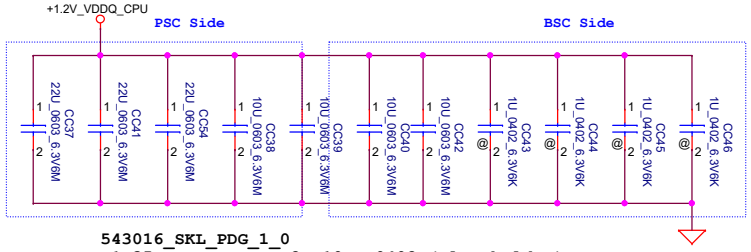




543016_SKL_PDG_1_0
+VCCIO : 2x10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 1uF 0402



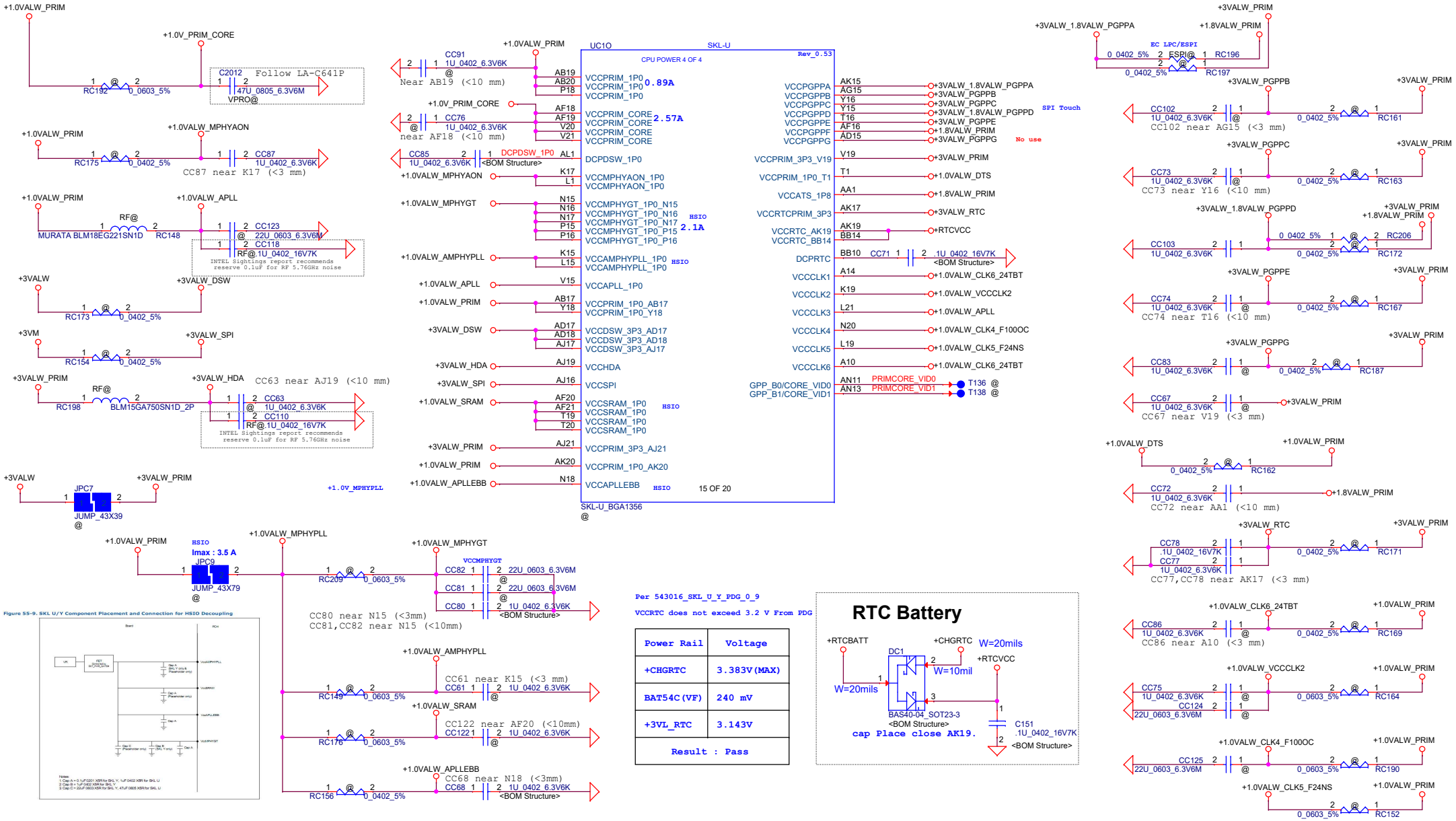




543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402
3x 22uF 0603

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Title	Compal Electronics, Inc.		
	SKL-U(8/12)Power		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 13 of 64		



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Friday, December 16, 2016	Sheet 14 of 64		

VCC 27A (U 15W Dual Core GT2)

#544924 Skylake EDS P.125

7.2.1.6 VCC_{OPC} DC Specifications

VCC_{OPC} is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

Table 7-7. VCC_{OPC} Voltage levels

ZVM# state	VCC_{OPC}	Units
0	0	V
1	1	V

VCC_{EOPIO} Voltage levels (separate VR)

ZVM# state	HSM# state	VCC_{EOPIO}	Units
0	x	0	V
1	0	0.8	V
1	1	1.0	V

Notes:
1. If processor line doesn't support HSM# signal.

#544924 Skylake EDS P.125
VCCOPC 1V 2.8A
VCC_OPC_1P8 1.8V 50mA
VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

+VCC_CORE

UC1L SKL-U Rev_0.53
CPU POWER 1 OF 4

A30	VCC_A30	
A34	VCC_A34	
A39	VCC_A39	
A44	VCC_A44	
AK33	VCC_AK33	
AK35	VCC_AK35	
AK37	VCC_AK37	
AK38	VCC_AK38	
AK40	VCC_AK40	
AL33	VCC_AL33	
AL37	VCC_AL37	
AL40	VCC_AL40	
AM32	VCC_AM32	
AM33	VCC_AM33	
AM35	VCC_AM35	
AM37	VCC_AM37	
AM38	VCC_AM38	
G30	VCC_G30	
K32	RSVD_K32	
AK32	RSVD_AK32	
AB62	VCCOPC_AB62	
P62	VCCOPC_P62	
V62	VCCOPC_V62	
H63	VCC_OPC_1P8_H63	
G61	VCC_OPC_1P8_G61	
AC63	VCCOPC_SENSE	
AE63	VSSOPC_SENSE	
AE62	VCCEOPIO	
AG62	VCCEOPIO	
AL63	VCCEOPIO_SENSE	
AJ62	VSSEOPIO_SENSE	

T132 @ VCCOPC_SENSE
T133 @ VSSOPC_SENSE
T137 @ VCCEOPIO_SENSE
T139 @ VSSEOPIO_SENSE

12 OF 20

SKL-U_BGA1356
@

+VCC_CORE

#544924 Skylake EDS P.120
VCC U(15W)-dual core GT2 27A(Typ)-33A(MAX)
0.55-1.15V

G32	VCC_G32
G33	VCC_G33
G35	VCC_G35
G37	VCC_G37
G38	VCC_G38
G40	VCC_G40
G42	VCC_G42
J30	VCC_J30
J33	VCC_J33
J37	VCC_J37
J40	VCC_J40
K33	VCC_K33
K35	VCC_K35
K37	VCC_K37
K38	VCC_K38
K40	VCC_K40
K42	VCC_K42
K43	VCC_K43
E32	VCC_SENSE
E33	VSS_SENSE
B63	VIDALERT#
A63	VIDSCK
D64	VIDSOUT
G20	VCCSTG_G20

Trace Length < 25 mils

VCCSENSE <55>
VSSSENSE <55>
SOC_SVID_ALERT#
SOC_SVID_CLK
SOC_SVID_DAT
SOC_SVID_CLK <55>
+1.0VS_VCCSTG
+1.0VS (SUSP#)

Table 2-1. Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{GTX}_SENSE / Vss_{GTX}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE		NA	
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]			

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines
- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals

VCCGT / VCCGTX(2+3e only) 40A(need confirm)

+VCC_GT

#544924 Skylake EDS P.121
VCCGT U(15W)-dual core GT2 40A(MAX)
0.55-1.15V

UC1M SKL-U Rev_0.53
CPU POWER 2 OF 4

A48	VCCGT
A53	VCCGT
A58	VCCGT
A62	VCCGT
A66	VCCGT
AA63	VCCGT
AA64	VCCGT
AA66	VCCGT
AA67	VCCGT
AA69	VCCGT
AA70	VCCGT
AA71	VCCGT
AC64	VCCGT
AC65	VCCGT
AC66	VCCGT
AC67	VCCGT
AC68	VCCGT
AC69	VCCGT
AC70	VCCGT
AC71	VCCGT
J43	VCCGT
J45	VCCGT
J46	VCCGT
J48	VCCGT
J50	VCCGT
J52	VCCGT
J53	VCCGT
J55	VCCGT
J56	VCCGT
J58	VCCGT
J60	VCCGT
K48	VCCGT
K50	VCCGT
K52	VCCGT
K53	VCCGT
K55	VCCGT
K56	VCCGT
K58	VCCGT
K60	VCCGT
L62	VCCGT
L63	VCCGT
L64	VCCGT
L65	VCCGT
L66	VCCGT
L67	VCCGT
L68	VCCGT
L69	VCCGT
L70	VCCGT
L71	VCCGT
M62	VCCGT
N63	VCCGT
N64	VCCGT
N66	VCCGT
N67	VCCGT
N69	VCCGT
J70	VCCGT_SENSE
J69	VSSGT_SENSE

N70	VCCGT
N71	VCCGT
R63	VCCGT
R64	VCCGT
R65	VCCGT
R66	VCCGT
R67	VCCGT
R68	VCCGT
R69	VCCGT
R70	VCCGT
R71	VCCGT
T62	VCCGT
U65	VCCGT
U68	VCCGT
U71	VCCGT
W63	VCCGT
W64	VCCGT
W65	VCCGT
W66	VCCGT
W67	VCCGT
W68	VCCGT
W69	VCCGT
W70	VCCGT
W71	VCCGT
Y62	VCCGT
VCCGTX_AK42	AK42
VCCGTX_AK43	AK43
VCCGTX_AK45	AK45
VCCGTX_AK46	AK46
VCCGTX_AK48	AK48
VCCGTX_AK50	AK50
VCCGTX_AK52	AK52
VCCGTX_AK53	AK53
VCCGTX_AK55	AK55
VCCGTX_AK56	AK56
VCCGTX_AK58	AK58
VCCGTX_AK60	AK60
VCCGTX_AK70	AK70
VCCGTX_AL43	AL43
VCCGTX_AL46	AL46
VCCGTX_AL50	AL50
VCCGTX_AL53	AL53
VCCGTX_AL56	AL56
VCCGTX_AL60	AL60
VCCGTX_AM48	AM48
VCCGTX_AM50	AM50
VCCGTX_AM52	AM52
VCCGTX_AM53	AM53
VCCGTX_AM56	AM56
VCCGTX_AM58	AM58
VCCGTX_AU58	AU58
VCCGTX_AU63	AU63
VCCGTX_BB57	BB57
VCCGTX_BB66	BB66
VCCGTX_SENSE	AK62 VCCGTX_SENSE
VSSGTX_SENSE	AL61 VSSGTX_SENSE

For CPU2+3e SKU

T155 @
T219 @

13 OF 20

SKL-U_BGA1356
@

<55> VCCGT_SENSE
<55> VSSGT_SENSE

Trace Length < 25 mils

SVID ALERT

+1.0V_VCCST
Place the PU resistors close to CPU
RC179 56_0402_5%
<BOM Structure>
SOC_SVID_ALERT#
RC180 220_0402_5%
SOC_SVID_ALERT#_R <55> (To VR)

SVID DATA

+1.0V_VCCST
Place the PU resistors close to CPU
RC181 100_0402_1%
<BOM Structure>
SOC_SVID_DAT
SOC_SVID_DAT <55> (To VR)

543016 PDG0.9 P.189 Need check

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCCST [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDSCK							100	100	0	10	
VIDALERT#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

Date: Thursday, December 15, 2016 Sheet 15 of 64

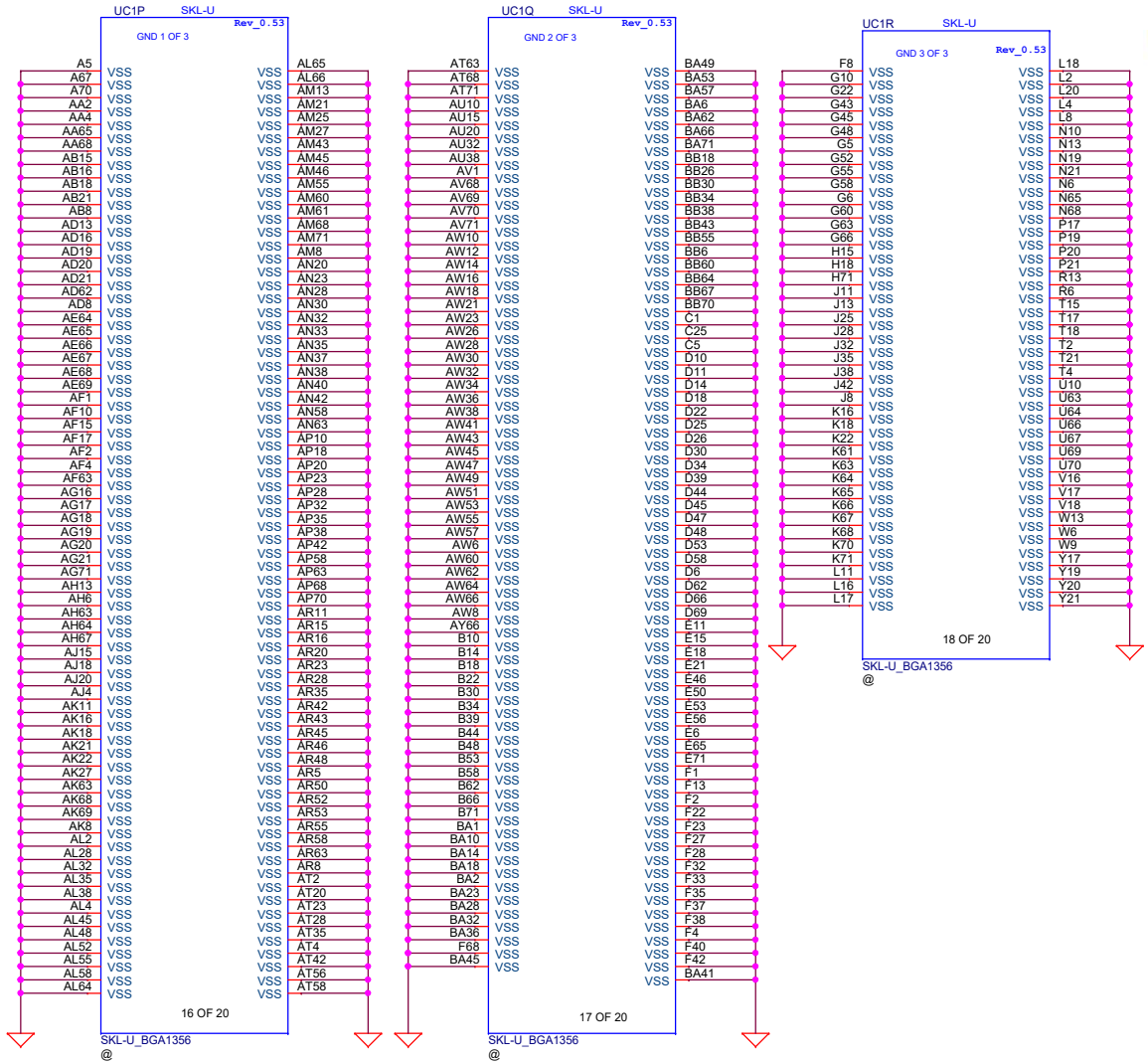
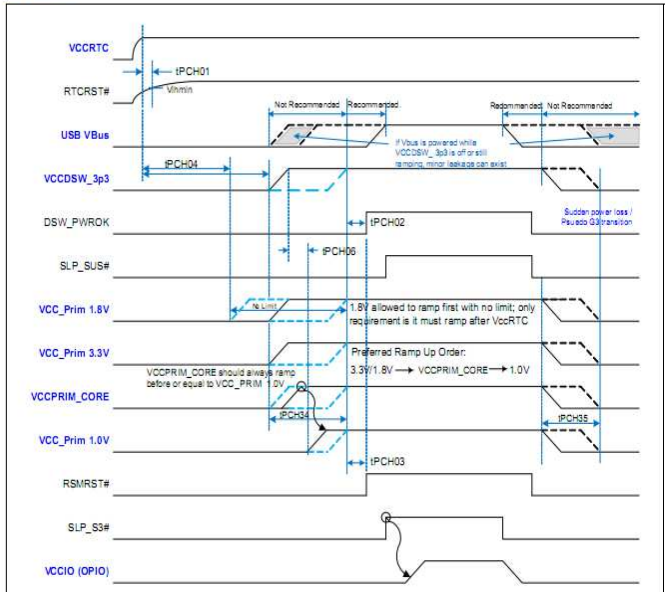


Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System

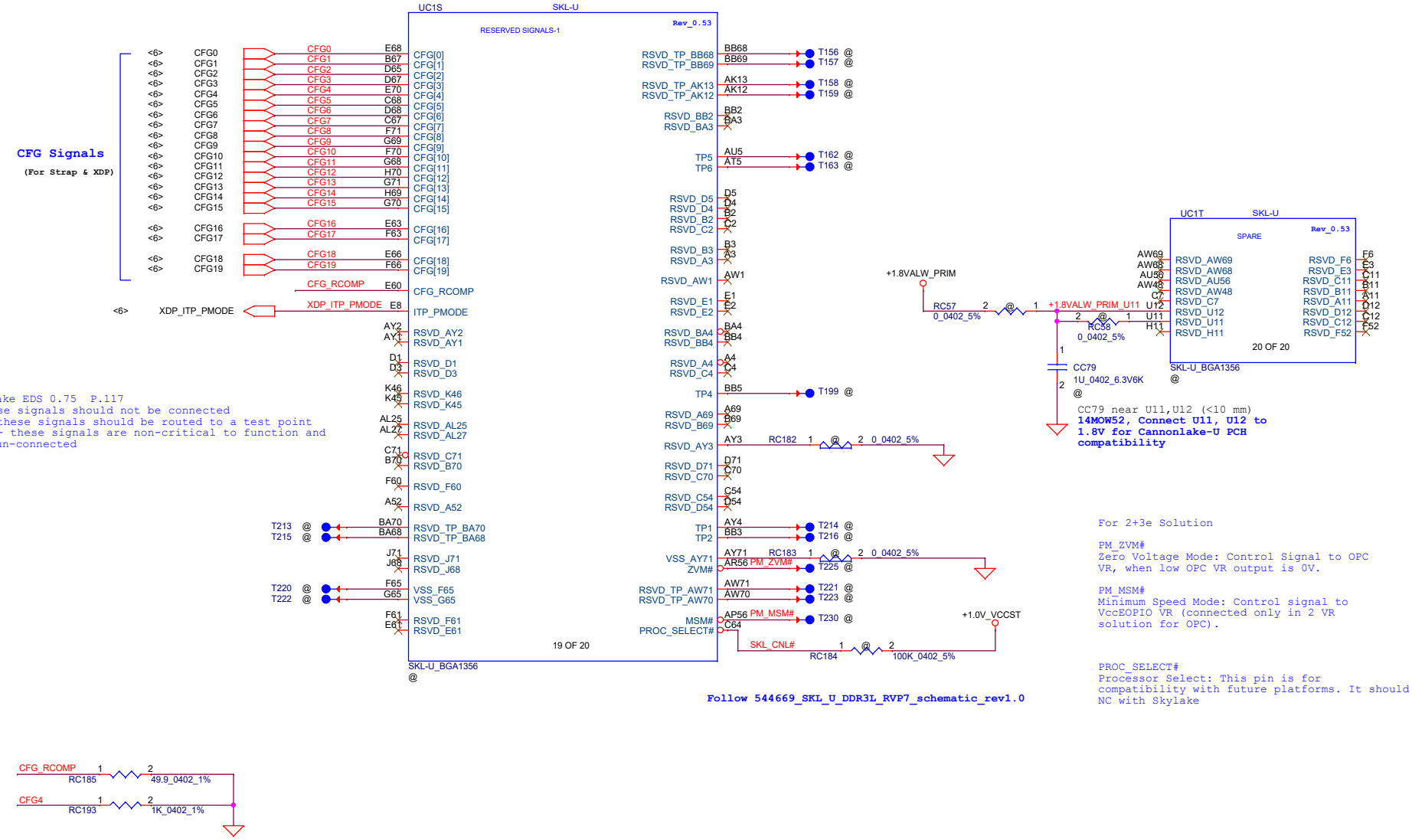


Notes:

1. VCC_PRIM 1.8 V includes VCCPGPPF, VCCATS and may include VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCC_PRIM 3.3 V includes VCCPRIM_3p3 and VCCRTCPRIM_3p3.
3. VCCPRIM_CORE is only applicable on SKL U/Y. For SKL H, the rail is merged with VCCPRIM_1p0.
4. VCC_PRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.		
Title: SKL-U(11/12)GND		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P	Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 16 of 64	



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.			
Title: SKL-U(12/12)RSVD			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 17 of 64		

Reverse Type

2-3A to 1 DIMMs/channel

DDR_B_DQS#[0..7]
DDR_B_D[0..63]
DDR_B_DQS[0..7]
DDR_B_MA[0..16]
DDR_B_BA0
DDR_B_BA1
DDR_B_BG0
DDR_B_BG1
DDR_B_CLK0
DDR_B_CLK#0
DDR_B_CLK1
DDR_B_CLK#1
DDR_B_CKE0
DDR_B_CKE1
DDR_B_CS#0
DDR_B_CS#1
SOC_SMBDATA
SOC_SMBCLK
DDR_B_ODT0
DDR_B_ODT1

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+1.2V_VDDQ

CD24 CD25 CD26 CD27 CD28 CD29 CD7 CD8
1U_0402_6.3V6K

4 as near side of the DIMM close to VDD pins

CD9 CD10 CD11 CD12 CD13 CD14 CD15 CD16 CD17
10U_0603_6.3V6M

Place these caps on the VTT plane close to DIMM

+0.6VS_VTT

CD30 CD31 CD32 CD33 CD22 CD23
1U_0402_6.3V6K
10U_0603_6.3V6M

+2.5V

C2140
10U_0603_6.3V6M
CD29
1U_0402_6.3V6K

+3VS

CD28
2.2U_0402_6.3V6M
.1U_0402_16V7K
+3VS_DIMM
close to DIMM

JDIMM1

DDR_B_D14	3	VSS	VSS	4	DDR_B_D11		
DDR_B_D15	5	VSS	DQ4	6	DDR_B_D10		
	7	VSS	DQ5	8			
	9	DQ1	VSS	10			
DDR_B_DQS#1	11	VSS	DQ0	12			
DDR_B_DQS1	13	DQS0_C	DM0*/DBI0*	14			
	15	DQS0_T	VSS	16	DDR_B_D8		
DDR_B_D13	17	VSS	DQ6	18			
	19	DQ7	VSS	20	DDR_B_D9		
DDR_B_D12	21	VSS	DQ2	22			
	23	DQ3	VSS	24	DDR_B_D4		
DDR_B_D1	25	VSS	DQ12	26			
	27	DQ13	VSS	28	DDR_B_D0		
DDR_B_D5	29	VSS	DQ8	30			
	31	DQ9	VSS	32	DDR_B_DQS#0		
	33	VSS	DQS1_C	34	DDR_B_DQS0		
	35	DM1*/DBI1*	DQS1_T	36			
DDR_B_D3	37	VSS	VSS	38	DDR_B_D6		
	39	DQ15	DQ14	40			
DDR_B_D2	41	VSS	VSS	42	DDR_B_D7		
	43	DQ10	DQ11	44			
DDR_B_D21	45	VSS	VSS	46	DDR_B_D20		
	47	DQ21	DQ20	48			
DDR_B_D17	49	VSS	VSS	50	DDR_B_D16		
	51	DQ17	DQ16	52			
DDR_B_DQS#2	53	VSS	VSS	54			
DDR_B_DQS2	55	DQS2_C	DM2*/DBI2*	56			
	57	DQS2_T	VSS	58	DDR_B_D19		
DDR_B_D23	59	VSS	DQ22	60			
	61	DQ23	VSS	62	DDR_B_D18		
DDR_B_D22	63	VSS	DQ18	64			
	65	DQ19	VSS	66	DDR_B_D28		
DDR_B_D29	67	VSS	DQ28	68			
	69	DQ29	VSS	70	DDR_B_D24		
DDR_B_D25	71	VSS	DQ24	72			
	73	DQ25	VSS	74	DDR_B_DQS#3		
	75	VSS	DQS3_C	76	DDR_B_DQS3		
	77	DM3*/DBI3*	DQS3_T	78			
DDR_B_D30	79	VSS	VSS	80	DDR_B_D31		
	81	DQ30	DQ31	82			
DDR_B_D26	83	VSS	VSS	84	DDR_B_D27		
	85	DQ26	DQ27	86			
	87	VSS	VSS	88			
	89	CB5_NC	CB4_NC	90			
	91	VSS	VSS	92			
	93	CB1_NC	CB0_NC	94			
	95	VSS	VSS	96			
	97	DQS8_C	DM8*/DBI8*	98			
	99	DQS8_T	VSS	100			
	101	VSS	CB6_NC	102			
	103	CB2_NC	VSS	104			
	105	VSS	CB7_NC	106			
	107	CB3_NC	VSS	108			
DDR_B_CKE0	109	VSS	RESET*	110	DDR_B_CKE1		
	111	CKE0	CKE1	112			
DDR_B_BG1	113	VDD1	VDD2	114			
DDR_B_BG0	115	BG1	ACT*	116			
	117	BG0	ALERT*	118			
DDR_B_MA12	119	VDD3	VDD4	120	DDR_B_MA11		
DDR_B_MA9	121	A12	A11	122	DDR_B_MA7		
	123	A9	A7	124			
DDR_B_MA8	125	VDD5	VDD6	126	DDR_B_MA5		
DDR_B_MA6	127	A8	A5	128	DDR_B_MA4		
	129	A6	A4	130			
DDR_B_MA3	131	VDD7	VDD8	132	DDR_B_MA2		
DDR_B_MA1	133	A3	A2	134			
	135	A1	EVENT*	136			
	137	VDD9	VDD10	138	DDR_B_CLK1		
DDR_B_CLK0	139	CK0_T	CK1_T	140	DDR_B_CLK#1		
DDR_B_CLK#0	141	CK0_C	CK1_C	142			
	143	VDD11	VDD12	144	DDR_B_MA0		
<7> DDR_B_PARITY		PARITY	A0				
DDR_B_BA1	145	BA1	A10_AP	146	DDR_B_MA10		
	147	VDD13	VDD14	148			
DDR_B_CS#0	149	S0*	BA0	150	DDR_B_BA0		
DDR_B_MA14	151	A14_WE*	A16_RAS*	152	DDR_B_MA16		
	153	VDD15	VDD16	154			
DDR_B_ODT0	155	ODT0	A15_CAS*	156	DDR_B_MA15		
DDR_B_CS#1	157	S1*	A13	158	DDR_B_MA13		
	159	VDD17	VDD18	160			
DDR_B_ODT1	161	ODT1	S2*/C0	162			
	163	VDD19	VREFCA	164			
	165	S3*/C1	SA2	166			
	167	VSS	VSS	168			
DDR_B_D37	169	DQ37	DQ36	170	DDR_B_D36		
DDR_B_D33	171	VSS	VSS	172	DDR_B_D32		
	173	DQ33	DQ32	174			
DDR_B_DQS#4	175	VSS	VSS	176			
DDR_B_DQS4	177	DQS4_C	DM4*/DBI4*	178			
	179	DQS4_T	VSS	180			
DDR_B_D38	181	VSS	DQ39	182	DDR_B_D39		
	183	DQ38	VSS	184			
DDR_B_D34	185	VSS	DQ35	186	DDR_B_D35		
	187	DQ34	VSS	188			
DDR_B_D44	189	VSS	DQ45	190	DDR_B_D45		
	191	DQ44	VSS	192			
DDR_B_D40	193	VSS	DQ41	194	DDR_B_D41		
	195	DQ40	VSS	196			
	197	VSS	DQS5_C	198	DDR_B_DQS#5		
	199	DM5*/DBI5*	DQS5_T	200	DDR_B_DQS5		
DDR_B_D43	201	VSS	VSS	202			
	203	DQ46	DQ47	204	DDR_B_D47		
DDR_B_D42	205	VSS	VSS	206			
	207	DQ42	DQ43	208	DDR_B_D46		
DDR_B_D52	209	VSS	VSS	210			
	211	DQ52	DQ53	212	DDR_B_D53		
DDR_B_D49	213	VSS	VSS	214			
	215	DQ49	DQ48	216	DDR_B_D48		
DDR_B_DQS#6	217	VSS	VSS	218			
DDR_B_DQS6	219	DQS6_C	DM6*/DBI6*	220			
	221	DQS6_T	VSS	222			
DDR_B_D55	223	VSS	DQ54	224	DDR_B_D54		
	225	DQ55	VSS	226			
DDR_B_D50	227	VSS	DQ51	228	DDR_B_D51		
	229	DQ51	VSS	230			
DDR_B_D61	231	VSS	DQ60	232	DDR_B_D60		
	233	DQ61	VSS	234			
DDR_B_D56	235	VSS	DQ57	236	DDR_B_D57		
	237	DQ56	VSS	238			
	239	VSS	DQS7_C	240	DDR_B_DQS#7		
	241	DM7*/DBI7*	DQS7_T	242	DDR_B_DQS7		
DDR_B_D59	243	VSS	VSS	244			
	245	DQ62	DQ63	246	DDR_B_D63		
DDR_B_D58	247	VSS	VSS	248			
	249	DQ58	DQ59	250	DDR_B_D62		
	251	VSS	VSS	252			
<8,18,33> SOC_SMBCLK	253	SCL	SDA	254	SOC_SMBDATA <8,18,33>		
+3VS_DIMM	255	VDDSPD	SA0	256			
	257	VPP1	VTT	258			
	259	VPP2	SA1	260			
			GND	261			
			GND	262			

CONN@ FOX_AS0A827-HZSB-7H

6/16 INTEL suggest
RD166 240_0402_1%
RD167 240_0402_1%

DDR_DRAMRST#_R
M_B_ACT#
DDR_B_ALERT#
<7> <7>
CD34 @ .1U_0402_16V7K

+DIMM_VREF_DQ

+2.5V
+0.6VS_VTT
+3VS
<8,18,33> SOC_SMBCLK
SOC_SMBDATA
RD108 @ 10K_0402_5%
<BOM Structure>
RD138 0_0402_5% @

+1.2V_VDDQ
+DIMM_VREF_DQ
20mil
<7> +0.6V_B_VREFDQ
RD10 2_0402_1%
CD21 0.022U_0402_16V7K
RD194 1K_0402_1%
RD12 24.9_0402_1%
RD199 1K_0402_1%

+1.2V_VDDQ
RD43 470_0402_1% <BOM Structure>
DDR_DRAMRST# R
RD45 @ 0_0402_5%
DDR_DRAMRST# <7,19>

Interleaved Memory

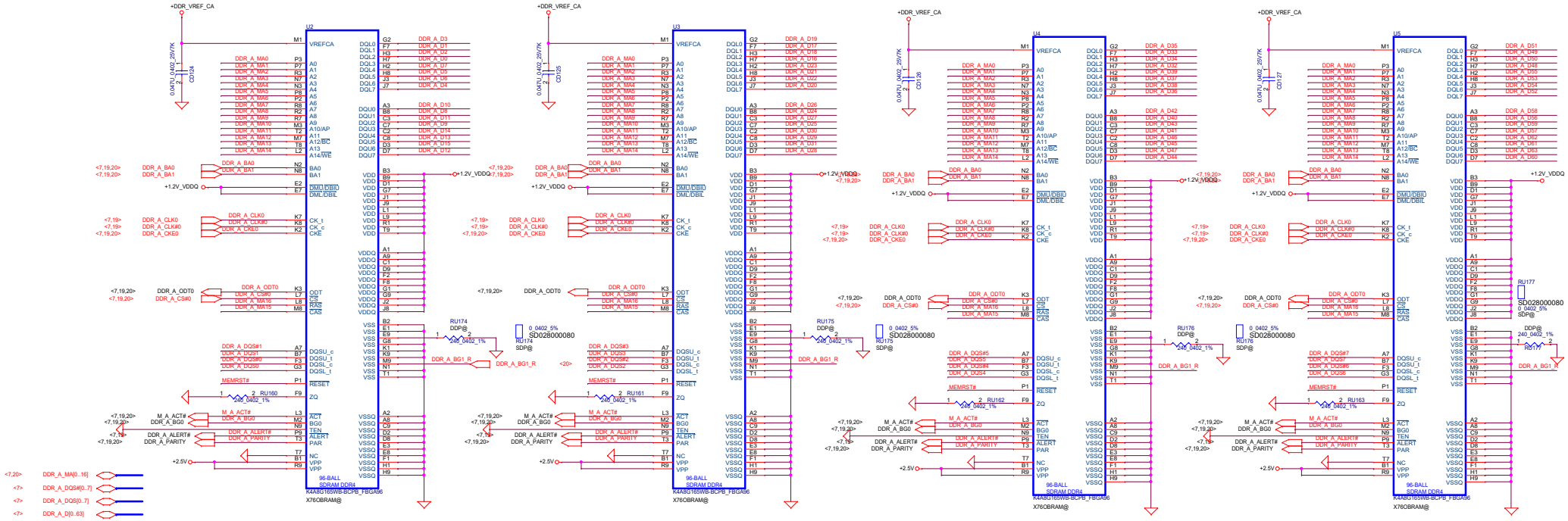
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

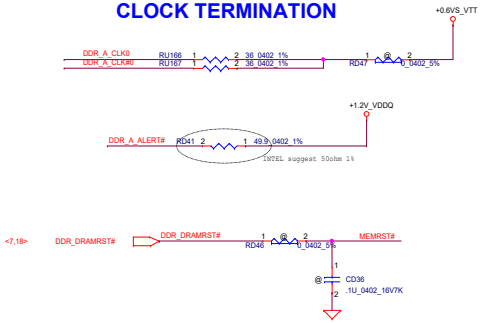
Title: DDR4_DIMM

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

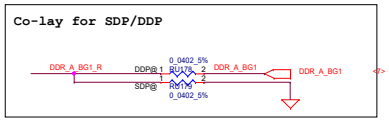
Date: Thursday, December 15, 2016 | Sheet 18 of 64



CLOCK TERMINATION



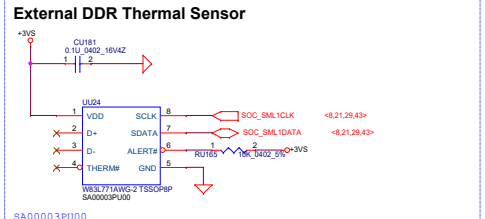
Co-lay for SDP/DDP

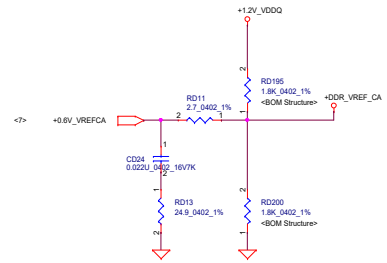


Data mapping

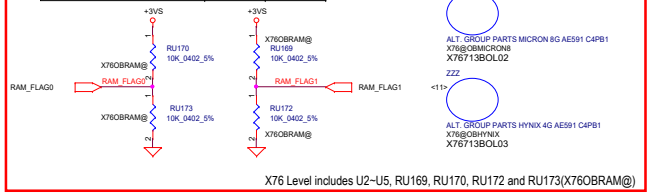
U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

External DDR Thermal Sensor





on board ram flag	FLAG1	FLAG0
	0	0
Micron 4G(SDP) SA00009V220	0	1
hynix 4G(SDP) SA0000A1H20	1	0
MICRON 8G (DDP)	1	1



X76 Level includes U2~U5, RU169, RU170, RU172 and RU173(X76OBRAM@)

Title: **DDR4 ON BOARD CHIPS**

Size: Custom | Document Number | Rev: 1.0

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<7,19> DDR_A_MA[0..16]

+1.2V_VDDQ

4 as near each on board RAM device as possible

Follow MA51

CU89
330U_D2_2V_Y
SGA00009S00
330U 2V H1.9
9mohm POLY

+2.5V

2 as near each on board RAM device as possible

CD41 CD42 CD43
<BOM Structure=BOM Structure>

+0.6VS_VTT

2 as near each on board RAM device as possible

+0.6VS_VTT

RP17
DDR_A_MA9
DDR_A_MA5
DDR_A_MA0
DDR_A_MA1
36_0804_8P4R_5%

RP18
DDR_A_MA6
DDR_A_MA11
DDR_A_MA7
DDR_A_MA4
36_0804_8P4R_5%

RP19
DDR_A_MA14
DDR_A_MA15
DDR_A_BA0
DDR_A_BA1
<7,19> DDR_A_BA0
<7,19> DDR_A_BA1
36_0804_8P4R_5%

RP20
DDR_A_ODT0
DDR_A_CS#0
DDR_A_MA16
DDR_A_MA10
<7,19> DDR_A_ODT0
<7,19> DDR_A_CS#0
36_0804_8P4R_5%

RP21
DDR_A_BG0
DDR_A_MA12
M_A_ACT#
DDR_A_CKE0
<7,19> DDR_A_BG0
<7,19> M_A_ACT#
<7,19> DDR_A_CKE0
36_0804_8P4R_5%

RP22
DDR_A_MA13
DDR_A_MA8
36_0804_8P4R_5%

RP24
DDR_A_MA3
DDR_A_MA2
DDR_A_PARITY
<7,19> DDR_A_PARITY
36_0804_8P4R_5%

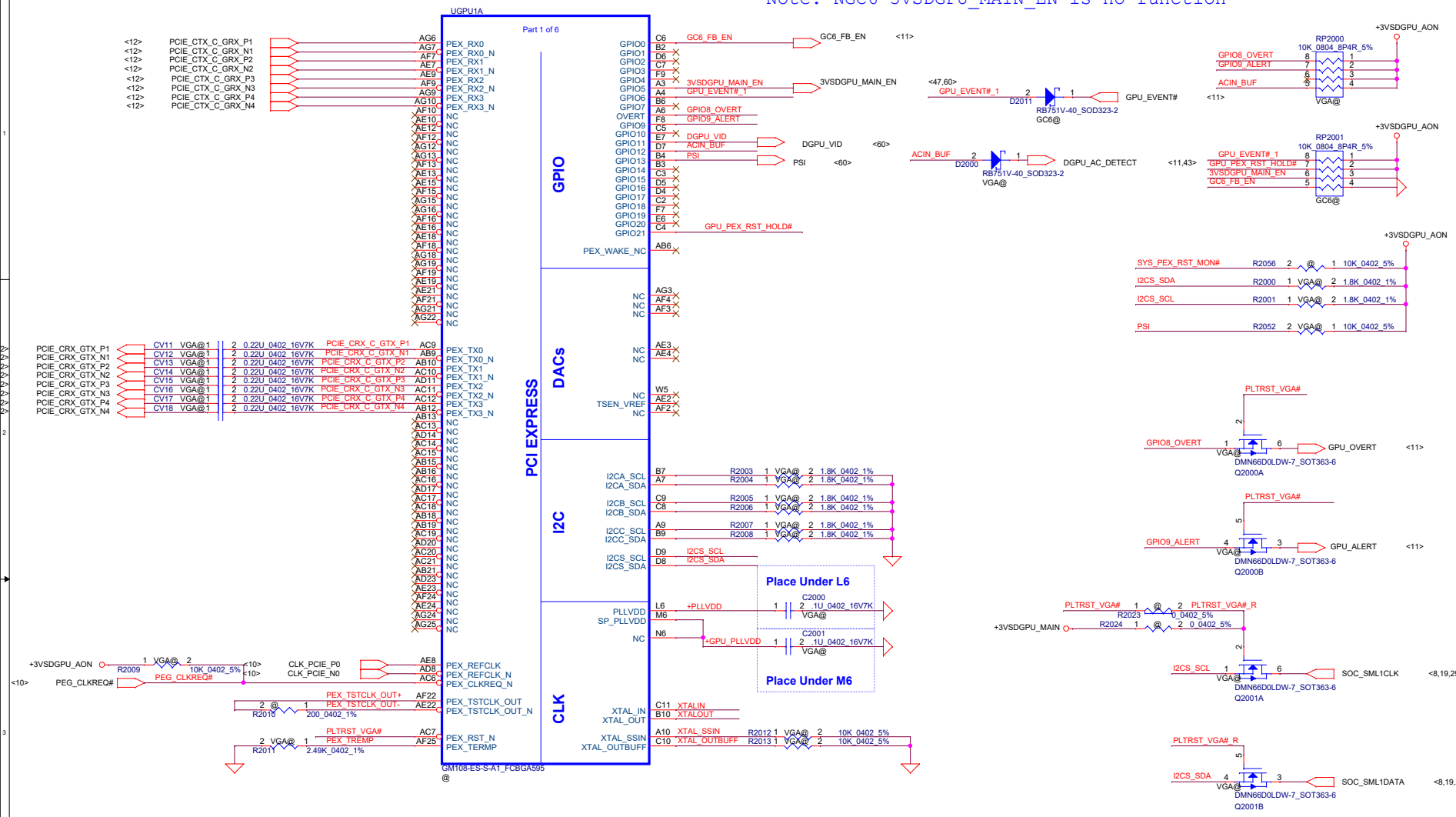
<19> DDR_A_BG1_R
DDR_A_BG1_R
RU180
DDP@
36_0402_1%

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Title: DDRIII ON BOARD CHIPS

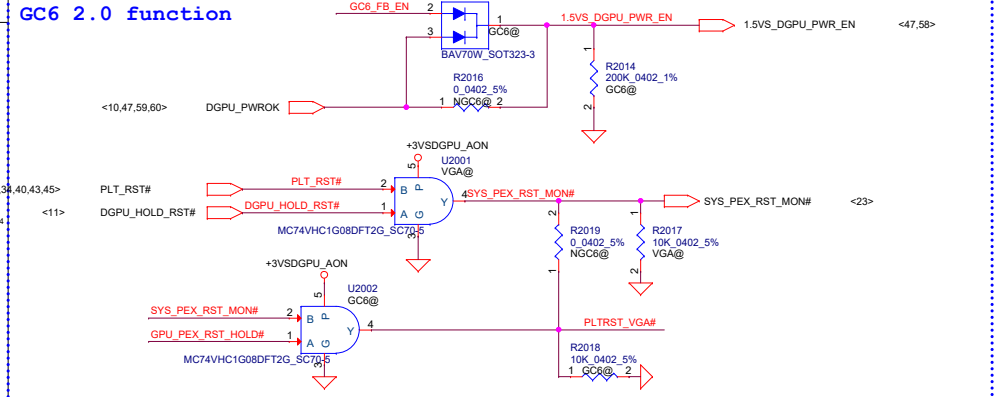
Size: Custom	Document Number	Rev 1.0
Date: Thursday, December 15, 2016	Sheet 20 of 64	

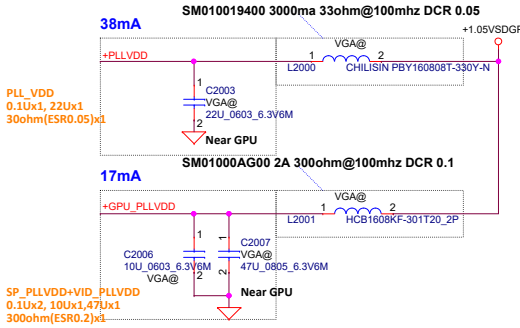
Note: NGC6 3VSDGPU_MAIN_EN is no function

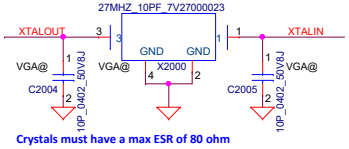


GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

GC6 2.0 function







Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title	N16X PEG 1/9		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 21 of 64		

VRAM Interface

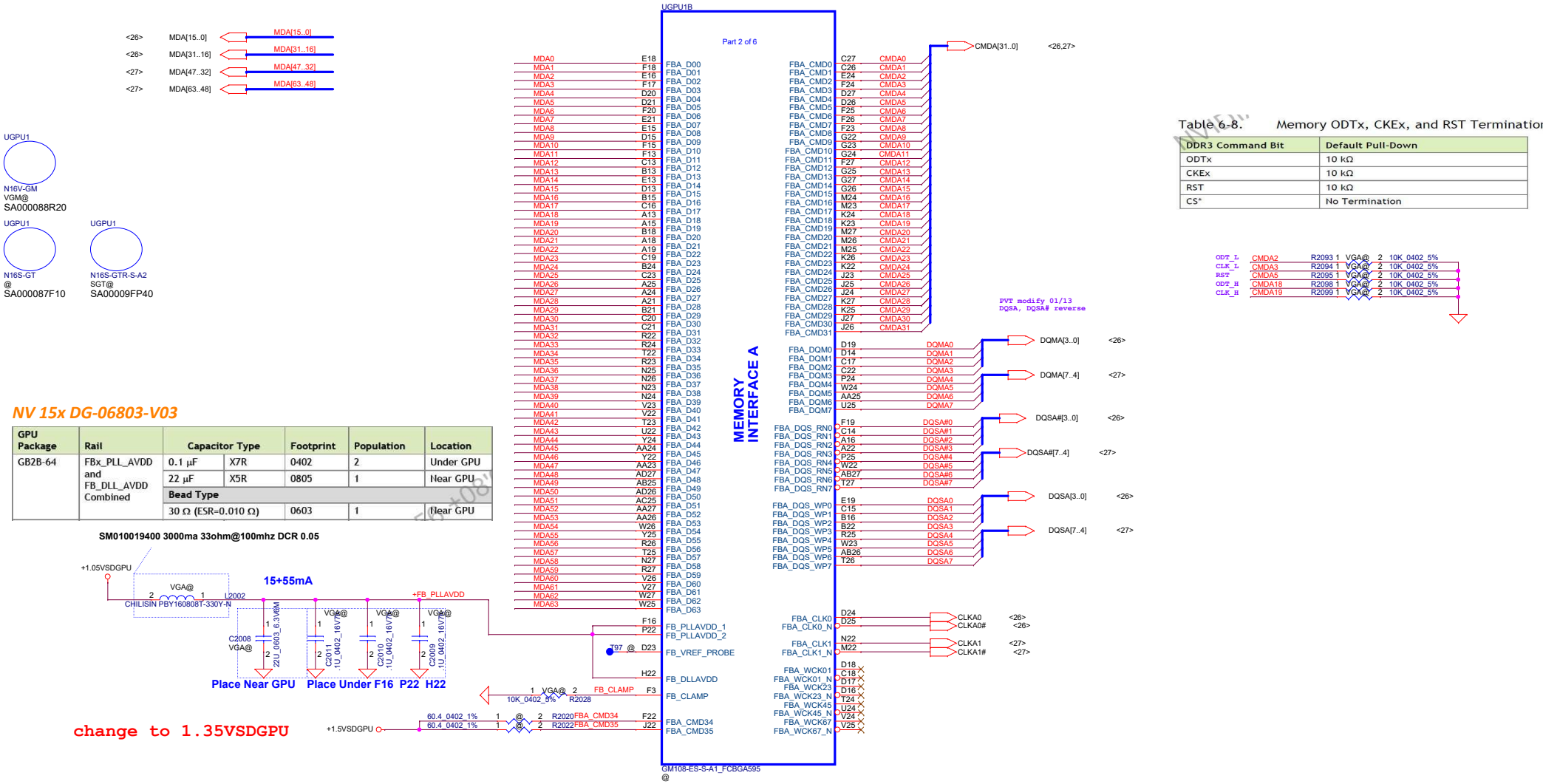


Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 kΩ
CKEx	10 kΩ
RST	10 kΩ
CS*	No Termination

NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

change to 1.35VSDGPU

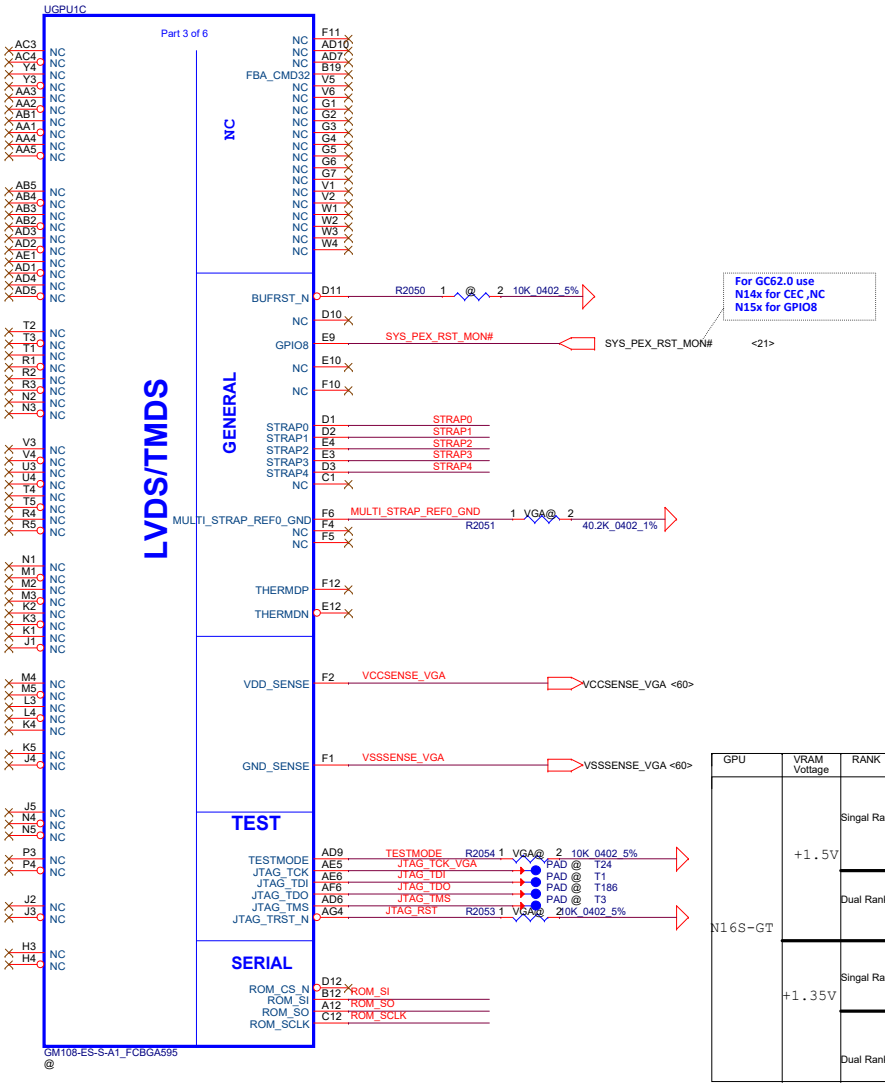
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

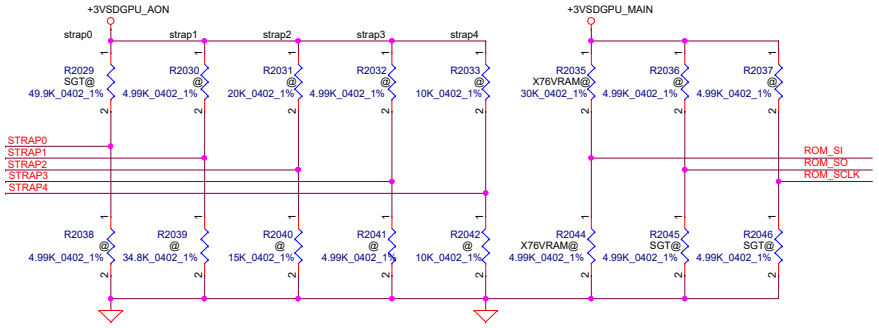
Title: N16X VRAM 2/9

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Thursday, December 15, 2016 | Sheet 22 of 64



MULTI LEVEL STRAPS



N16VGM Option Component

```
STRAP0  ---> R2029 2 VGM@1 45.3K_0402_1% SD034453280
STRAP1  ---> R2039 2 VGM@1 45.3K_0402_1% SD034453280
STRAP2  ---> R2031 2 VGM@1 10K_0402_1%   SD034100280
STRAP3  ---> R2041 2 VGM@1 4.99K_0402_1% SD034499180
STRAP4  ---> R2042 2 VGM@1 45.3K_0402_1% SD034453280
ROM_SO  ---> R2036 2 VGM@1 4.99K_0402_1% SD034499180
ROM_SCLK---> R2037 2 VGM@1 4.99K_0402_1% SD034499180

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x4
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0xE
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC
```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

For N16S-GT Multi strap table — **Decive ID : 0x1347**

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Singal Rank	X76713BOL04	1GHz	256Mx16x4 2GB	(SA00008DN80) Hynix H5TC4G63EFR-N0C	PU 50K	NC	NC	NC	NC	PU 10K	PD 4.99K	PD 4.99K
			X76614BOL54			0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 30K		
			X76629BOL08			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76614BOL58			0x2 (SA000076P20) Samsung K4W4G1646E-BC1A						PD 24.9K		
		Dual Rank	X76629BOL10	1GHz	256Mx16x8 4GB	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 24.9K		
			X76629BOL11			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629BOL12			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x2 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 15K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x8 4GB	0xE (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 35K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		

For N16V-GM Multi strap table — **Decive ID : 0x1299**

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.5V	Singal Rank	X76629BOL01	1GHz	256Mx16x4 2GB	0x9 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 45.3K	PD45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 10K	PU 4.99K	PU 4.99K
			X76629BOL02			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629BOL03			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x0 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 5K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank	X76629BOL04	900MHz	256Mx16x8 4GB	0xA (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 15K		
			X76629BOL05			0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
			X76629BOL06			0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: N16X STRAPS 3/9

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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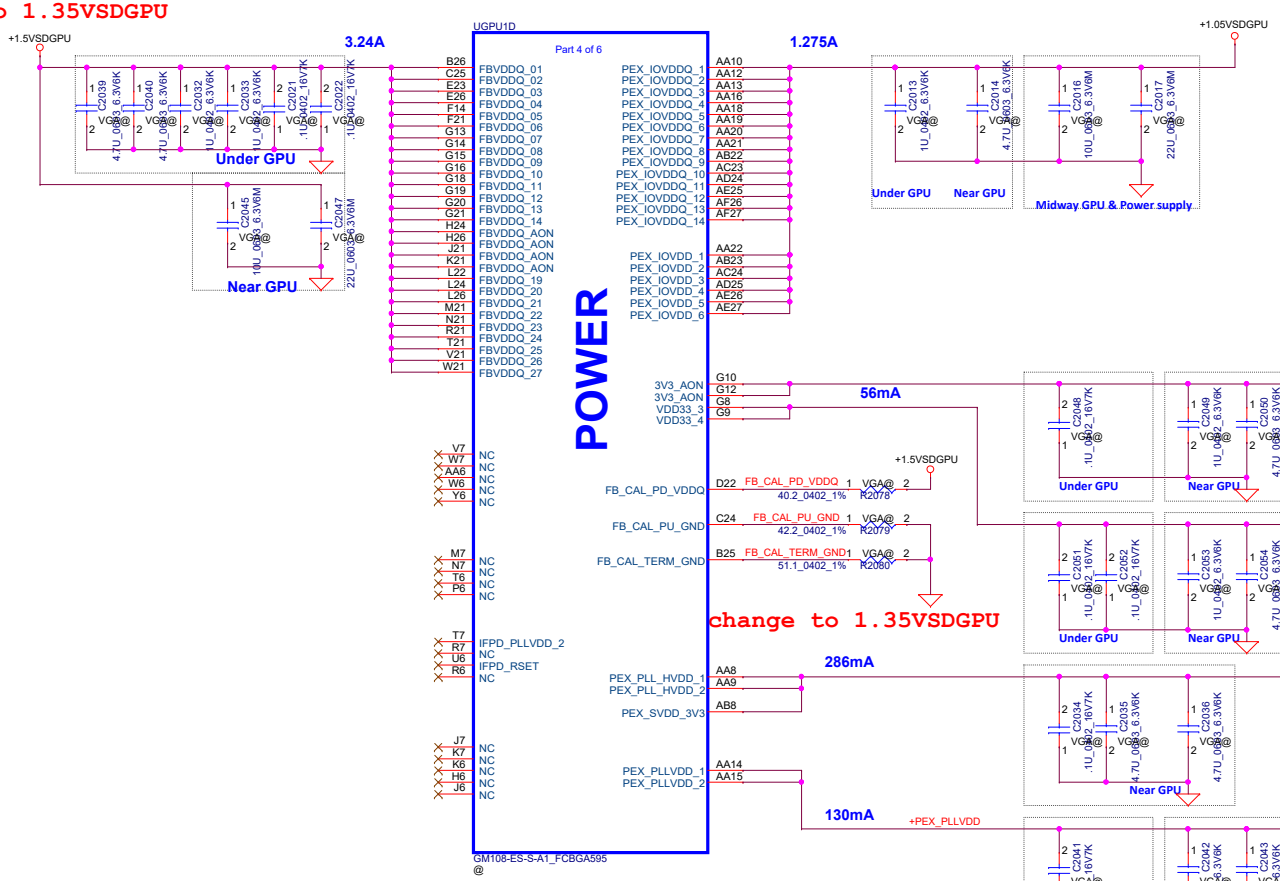
NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population		Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

change to 1.35VSDGPU



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: N16X POWER & GND 4/9

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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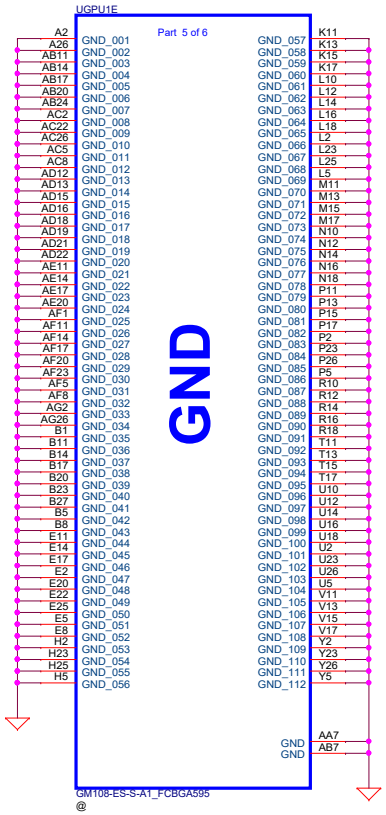

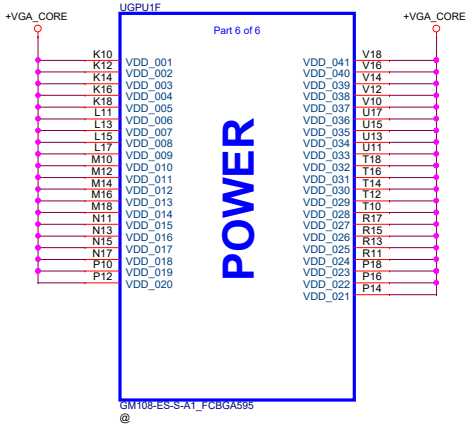

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GM-S DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GL DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

Compal Electronics, Inc.

Title: N16X POWER & GND 5/9

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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VRAM DDR3 chips

LOW BIT

ZZZ

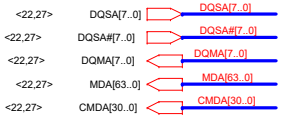
ALT. GROUP PARTS GT2G HYN 256M16 A4WAD
X76@VHY
X76614BOL54

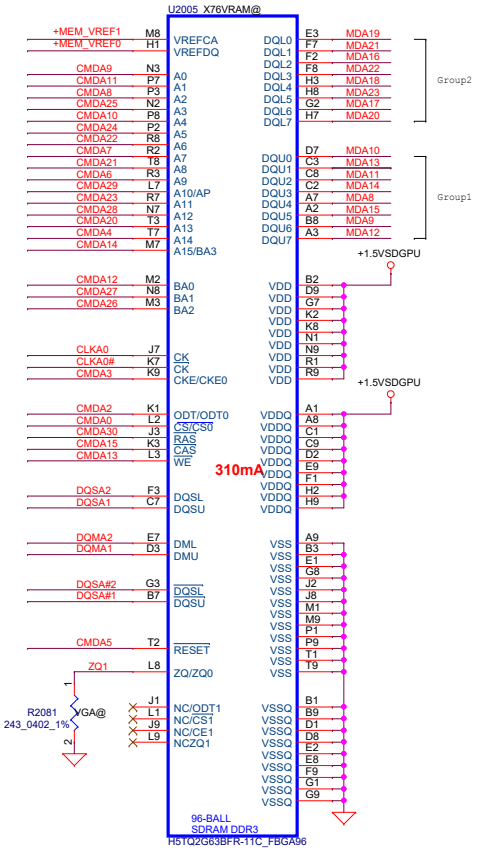
ZZZ

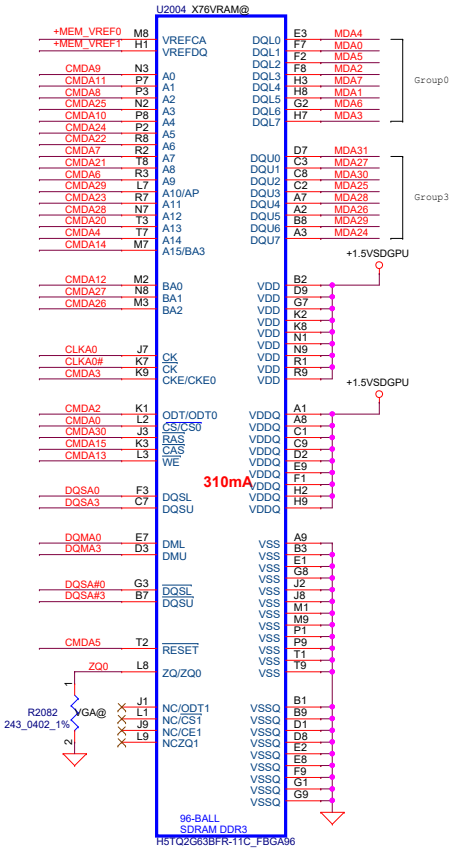
ALT. GROUP PARTS GT2G SAM-N 256M16 A4WAD
X76@VSAM
X76614BOL58

ZZZ

ALT. GROUP PARTS HYNIX 256M16 C4PB1
X76@VHY_E
X76713BOL04





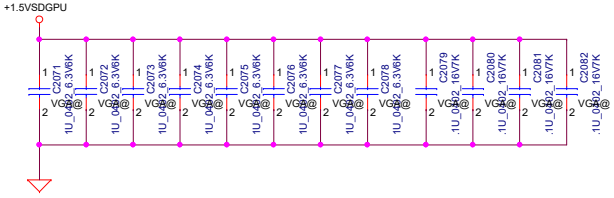


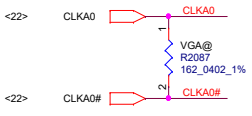
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

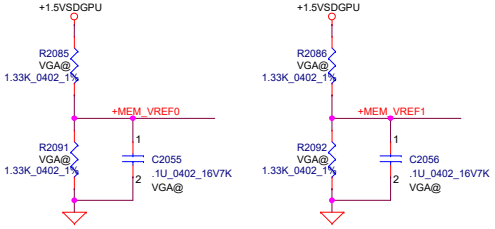
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM







Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

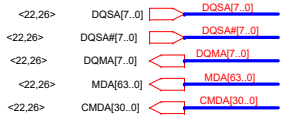
Title: N16X Upper Rank0 6/9

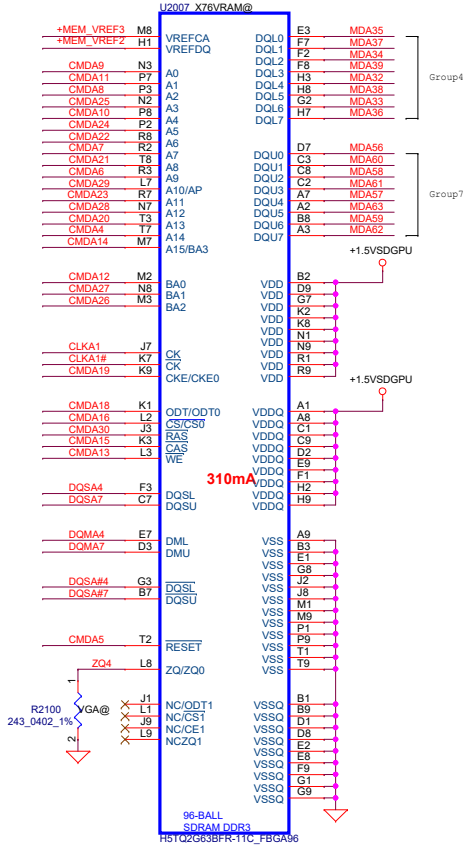
Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

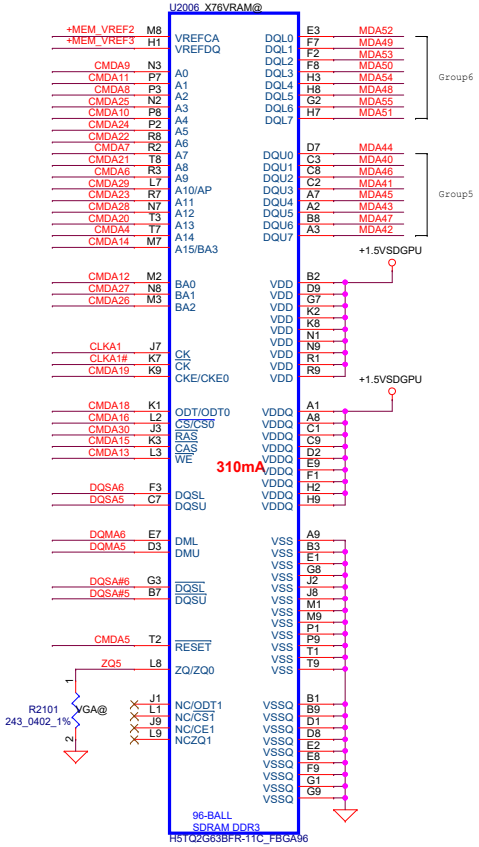
Date: Thursday, December 15, 2016 Sheet 26 of 64

VRAM DDR3 chips

HIGH BIT

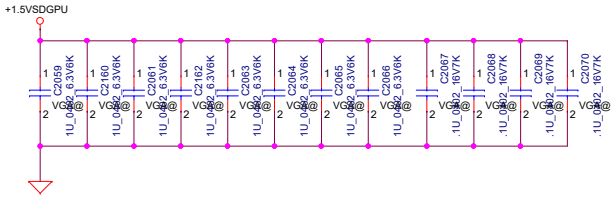


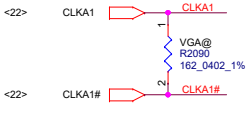


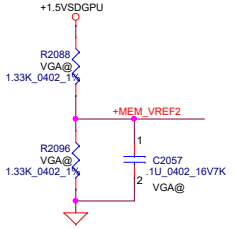


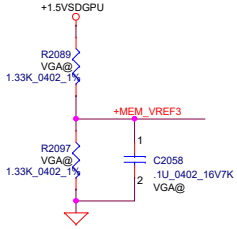
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

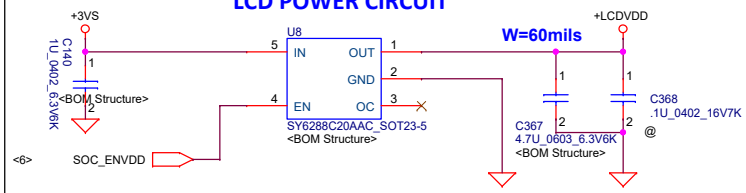
Compal Electronics, Inc.

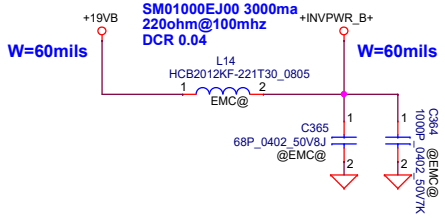
Title: N16X Lower Rank0 8/9

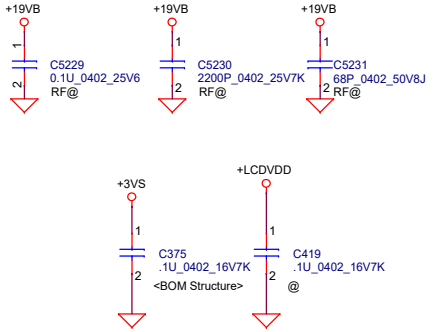
Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Thursday, December 15, 2016 | Sheet 27 of 64

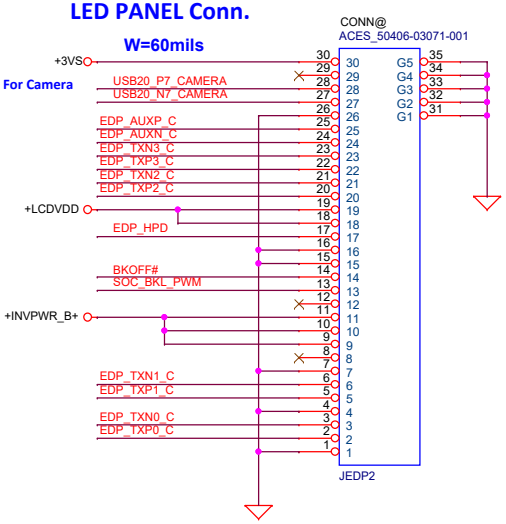
LCD POWER CIRCUIT

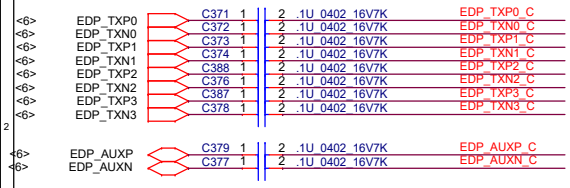


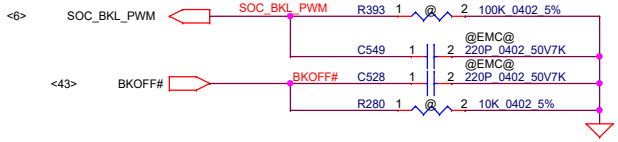


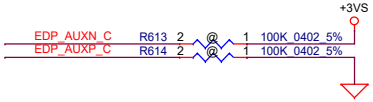


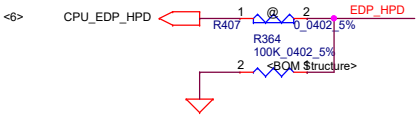
LED PANEL Conn.





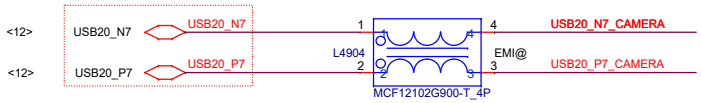






SP010011Z00

Camera



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: eDP Connector			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
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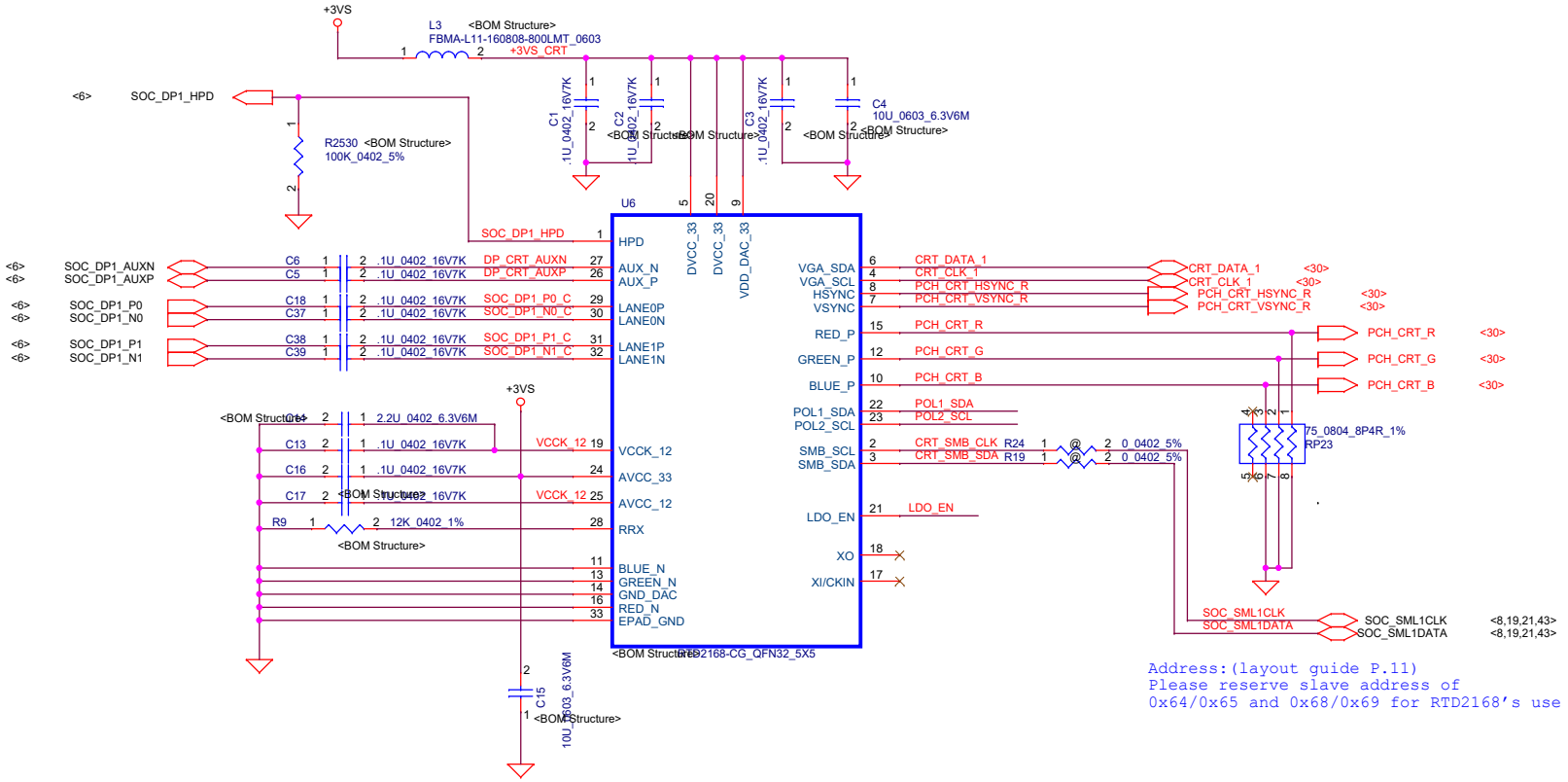
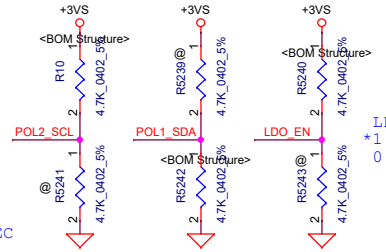


Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168's use

		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM



LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.		
Title: Realtek RTD2168		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P	Rev: 1.0
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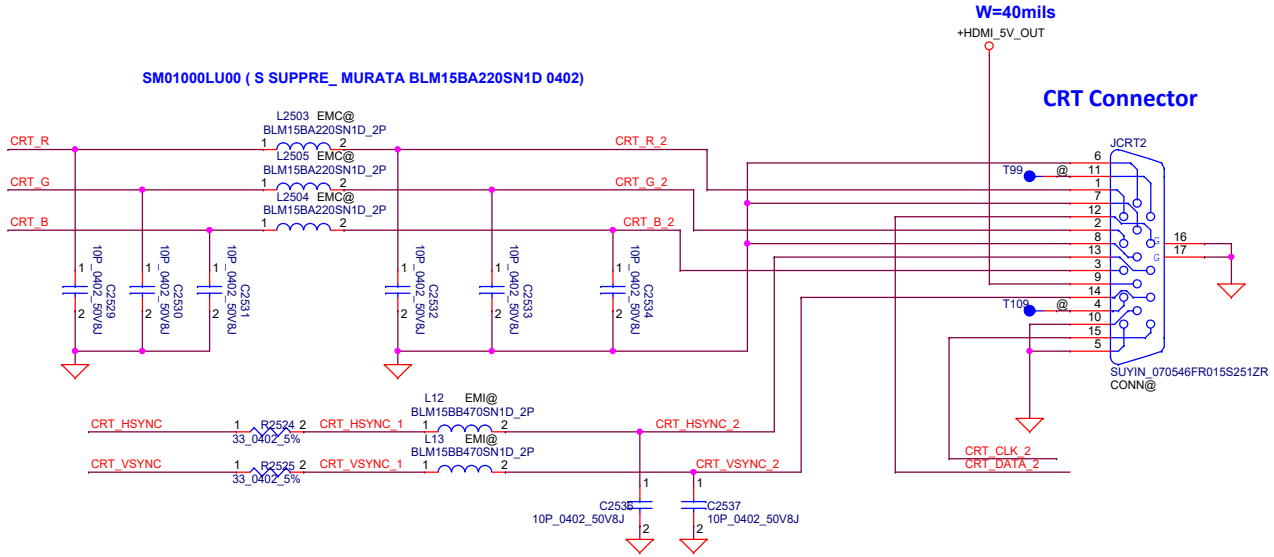
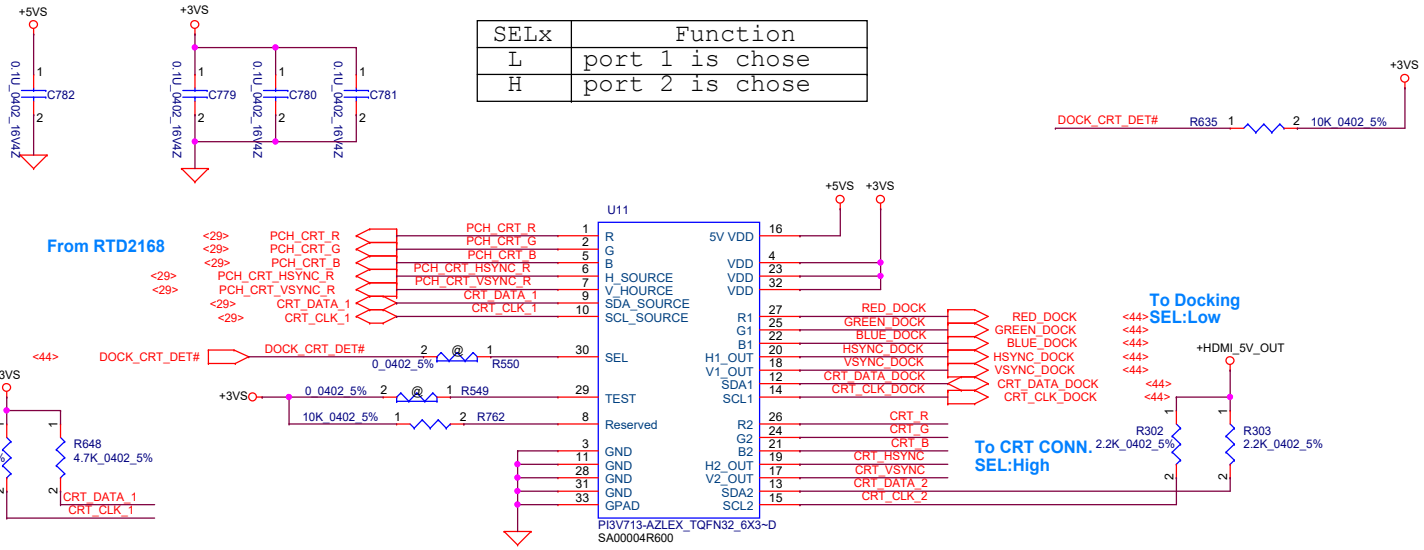
CRT conn.





SELx	Function
L	port 1 is chose
H	port 2 is chose

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: CRT CONN.			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
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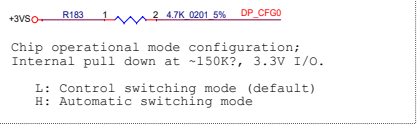
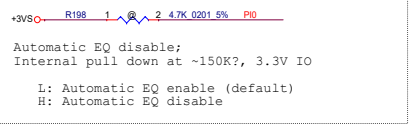


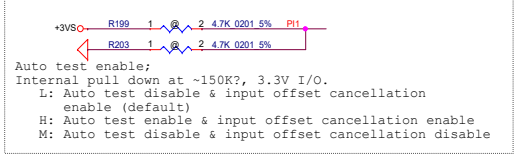
Chip operational mode configuration;
Internal pull down at ~150K?, 3.3V I/O.

L: Control switching mode (default)
H: Automatic switching mode

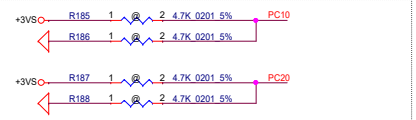


Automatic EQ disable;
Internal pull down at ~150K?, 3.3V IO

L: Automatic EQ enable (default)
H: Automatic EQ disable

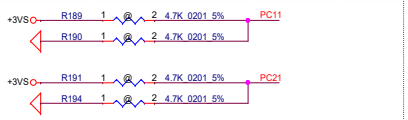


Auto test enable;
Internal pull down at ~150K?, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable



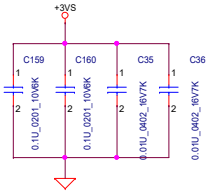
AUX interception disable for Port y (y=1,2)
Internal pull down at ~150K?, 3.3V I/O.

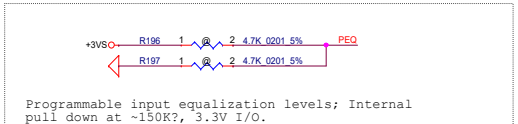
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mv and 0dB
M: AUX interception disable, driver output with fixed 400mv and 0dB



Output swing adjusment for Port y (y=1,2).
Internal pull down at ~150K?, 3.3V I/O.

L:default
H: +20%
M: -16.7%



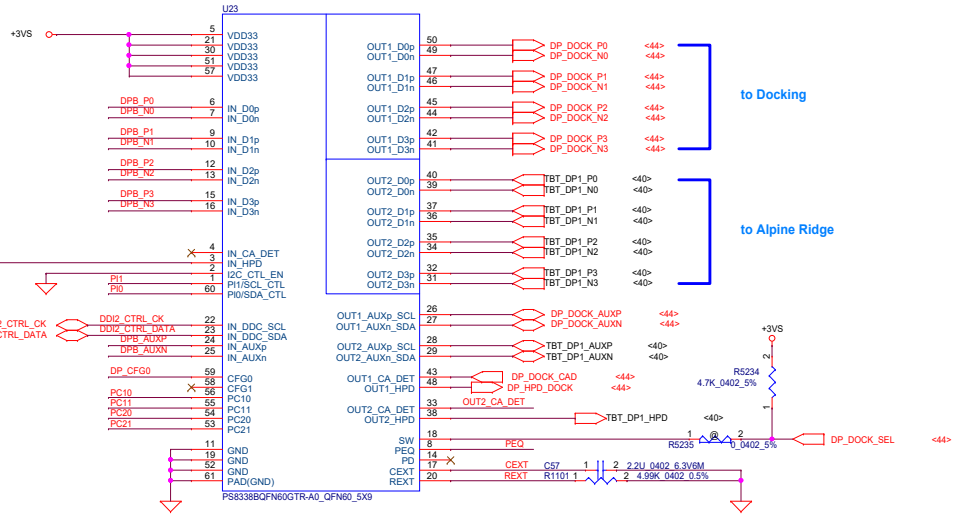


Programmable input equalization levels; Internal pull down at ~150K?, 3.3V I/O.

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

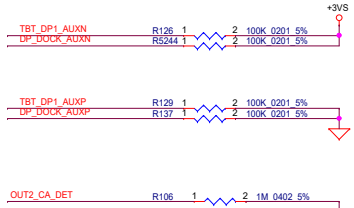
DP_MUX_SEL pin

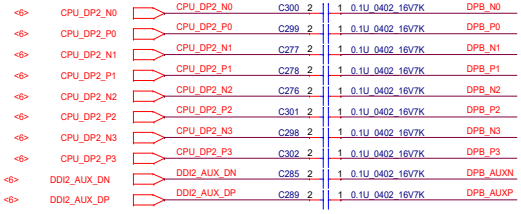
Port switching control or priority configuration;
Internal pull down at ~150K?, 3.3V I/O.
L: Port1 is selected or with higher priority (default)
H: Port2 is selected or with higher priority



to Docking

to Alpine Ridge





Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: P32-DP MUX

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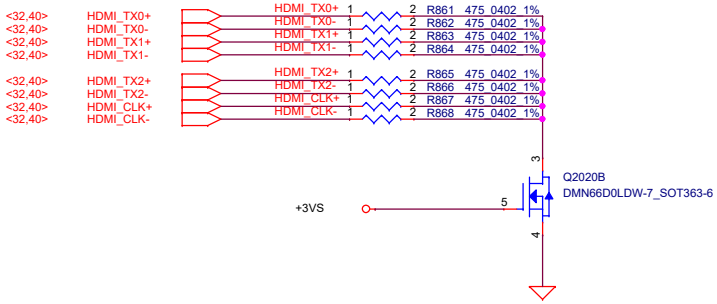
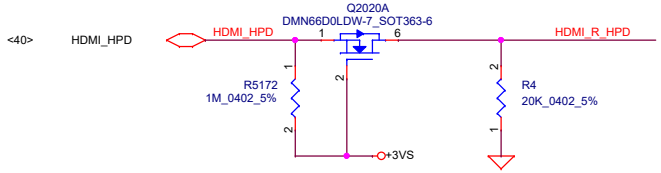
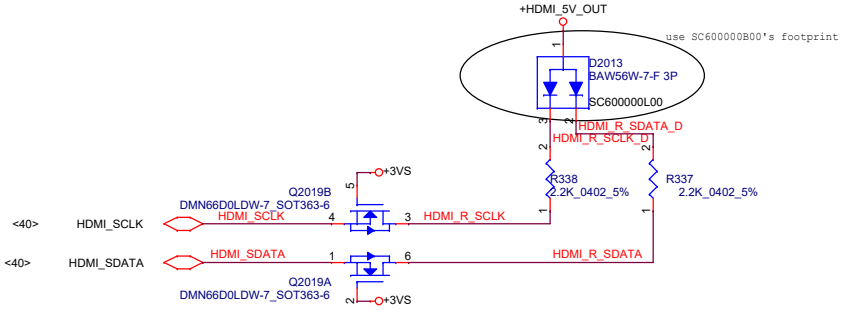
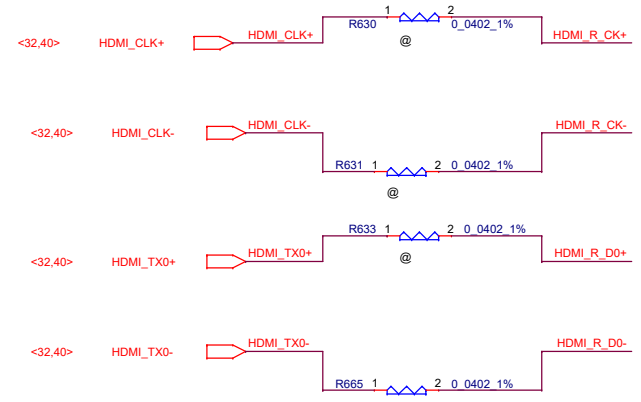
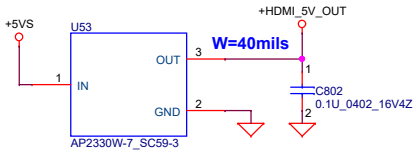
the onrigial BOM structure of R630, R631, R633, R665, R667, R668, R669, R671 is EMI@ , @ is for short pad only

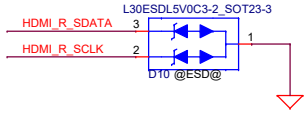


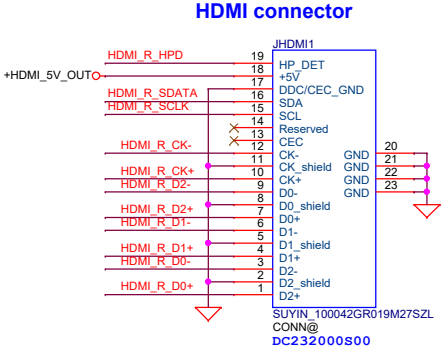












Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title	HDMI CONN.		
Size	Document Number		Rev
Custom	C4PB1/C5PB1 LA-E591P		1.0
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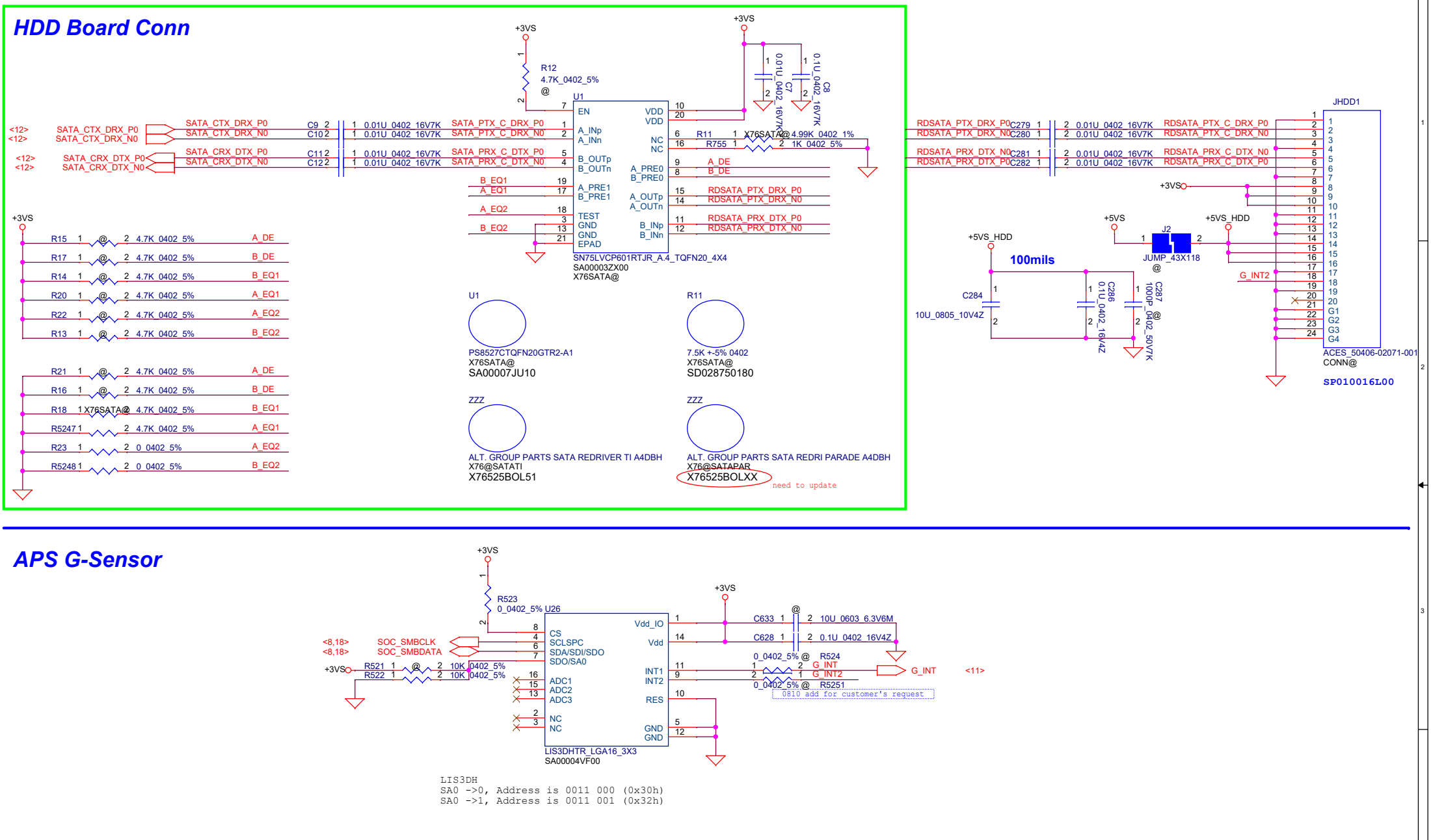
HDD Board Conn



APS G-Sensor


```
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)
```

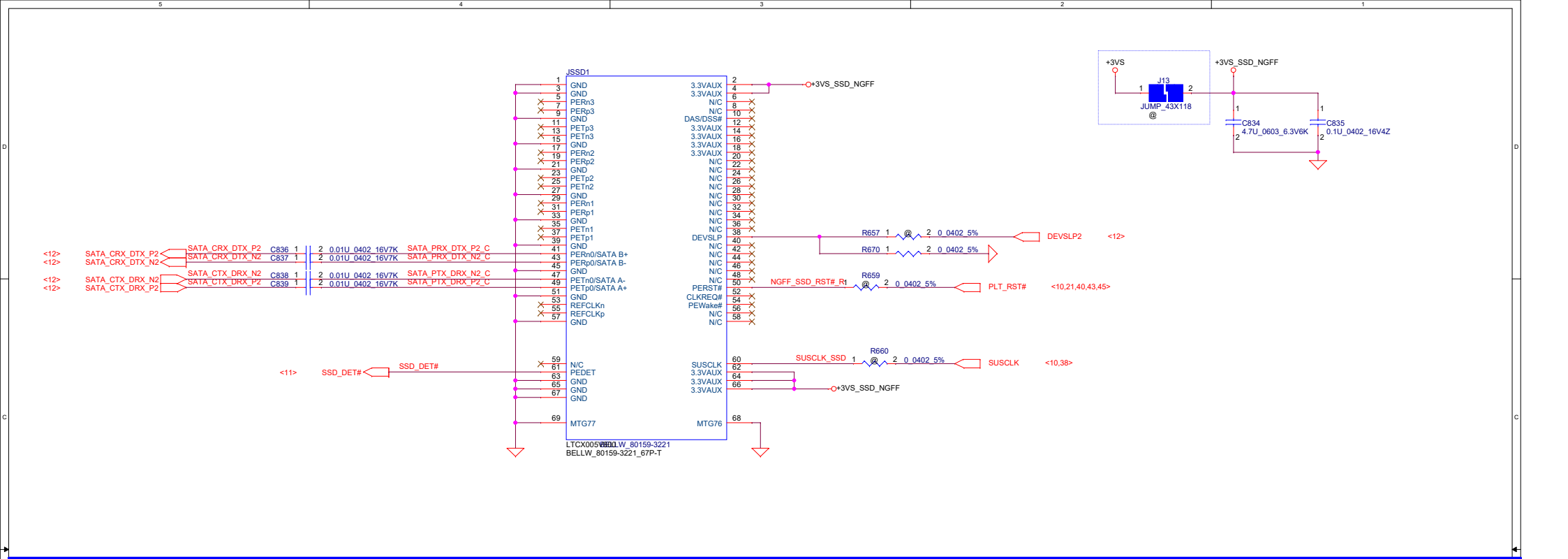
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

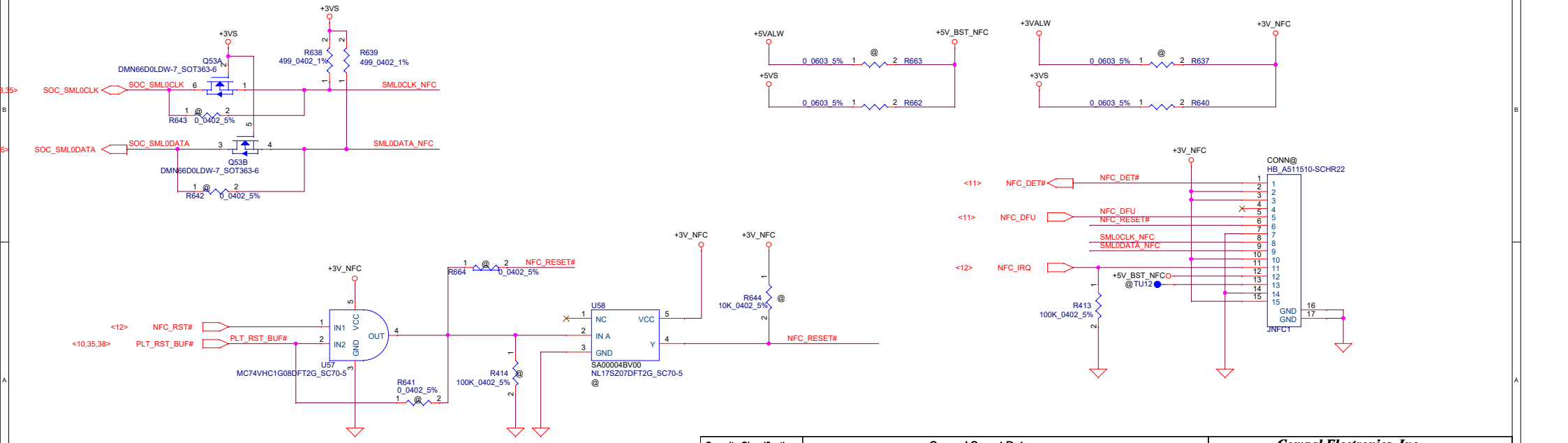
Compal Electronics, Inc.

Title: **HDD & G-Sensor**

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

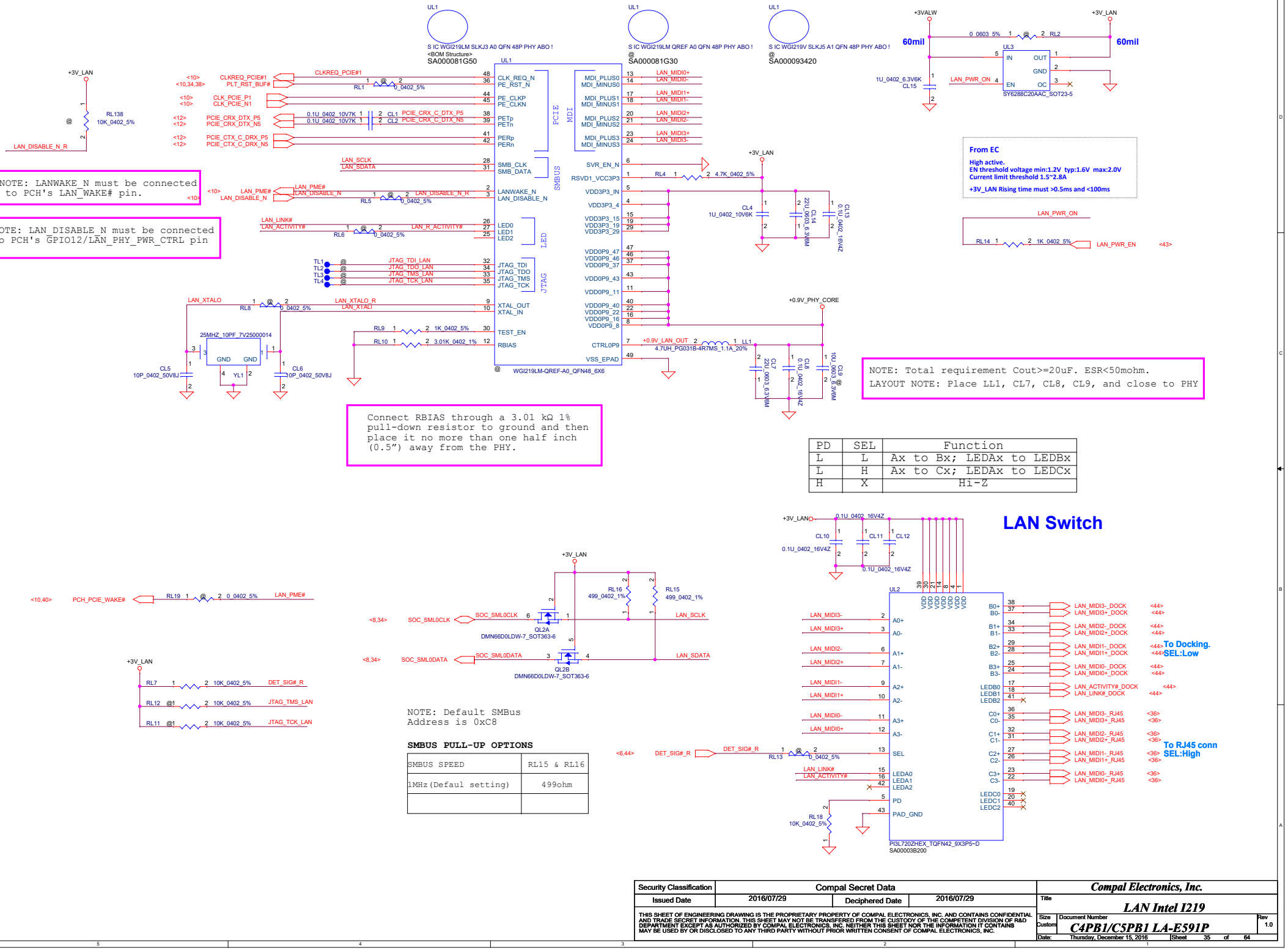
Date: Friday, December 16, 2016 | Sheet 33 of 64





Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title	mSATA & NFC		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 34 of 64		


UL1
S IC WGI219LM SLKJ3 A0 QFN 48P PHY ABO !
<BOM Structure>
SA000081G50
UL1
S IC WGI219LM QREF A0 QFN 48P PHY ABO !
@
SA000081G30
UL1
S IC WGI219V SLKJ5 A1 QFN 48P PHY ABO !
@
SA000093420
+3V_LAN
RL138
10K_0402_5%
LAN_DISABLE_N_R
CLKREQ_PCIE#1
PLT_RST_BUF#
RL1
0_0402_5%
CLK_PCIE_P1
CLK_PCIE_N1
PCIE_CRX_DTX_P5
PCIE_CRX_DTX_N5
0.1U_0402_10V7K
CL1
CL2
PCIE_CRX_C_DTX_P5
PCIE_CTX_C_DRX_P5
PCIE_CTX_C_DRX_N5
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
PCIE
MDI
MDI_PLUS0
MDI_MINUS0
MDI_PLUS1
MDI_MINUS1
MDI_PLUS2
MDI_MINUS2
MDI_PLUS3
MDI_MINUS3
LAN_MIDI0+
LAN_MIDI0-
LAN_MIDI1+
LAN_MIDI1-
LAN_MIDI2+
LAN_MIDI2-
LAN_MIDI3+
LAN_MIDI3-
LAN_SCLK
LAN_SDATA
SMB_CLK
SMB_DATA
SMBUS
SVR_EN_N
RSVD1_VCC3P3
RL4
4.7K_0402_5%
LAN_PME#
LAN_DISABLE_N
LAN_DISABLE_N_R
RL5
LANWAKE_N
LAN_LINK#
LAN_ACTIVITY#
LAN_R_ACTIVITY#
RL6
LED0
LED1
LED2
LED
VDD3P3_IN
VDD3P3_4
VDD3P3_15
VDD3P3_19
VDD3P3_29
CL4
1U_0402_10V6K
CL14
220U_0603_6.3V6M
CL13
0.1U_0402_16V4Z
VDD0P9_47
VDD0P9_46
VDD0P9_37
VDD0P9_43
VDD0P9_11
VDD0P9_40
VDD0P9_22
VDD0P9_16
VDD0P9_8
+0.9V_PHY_CORE
TL1
TL2
TL3
TL4
JTAG_TDI_LAN
JTAG_TDO_LAN
JTAG_TMS_LAN
JTAG_TCK_LAN
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
LAN_XTALO
LAN_XTALO_R
RL8
LAN_XTALI
XTAL_OUT
XTAL_IN
25MHZ_10PF_7V25000014
GND
YL1
CL5
10P_0402_50V8J
CL6
10P_0402_50V8J
RL9
1K_0402_5%
RL10
3.01K_0402_1%
TEST_EN
RBIAS
CTRL0P9
VSS_EPAD
+0.9V_LAN_OUT
4.7UH_PG031B-4R7MS_1.1A_20%
LL1
CL7
220U_0603_6.3V6M
CL8
0.1U_0402_16V4Z
CL9
10U_0603_6.3V6M
WGI219LM-QREF-A0_QFN48_6X6
+3VALW
60mil
+3V_LAN
60mil
0_0603_5%
RL2
UL3
IN
OUT
GND
EN
OC
LAN_PWR_ON
1U_0402_6.3V6K
CL15
SY6288C20AAC_SOT23-5
From EC
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms
LAN_PWR_ON
RL14
1K_0402_5%
LAN_PWR_EN
<43>
NOTE: LANWAKE_N must be connected to PCH's LAN_WAKE# pin.
NOTE: LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL pin
Connect RBIAS through a 3.01 kΩ 1% pull-down resistor to ground and then place it no more than one half inch (0.5") away from the PHY.
NOTE: Total requirement Cout>=20uF. ESR<50mohm.
LAYOUT NOTE: Place LL1, CL7, CL8, CL9, and close to PHY
PD
SEL
Function
L
L
Ax to Bx; LEDAx to LEDBx
L
H
Ax to Cx; LEDAx to LEDCx
H
X
Hi-Z
LAN Switch
+3V_LAN
0.1U_0402_16V4Z
CL10
CL11
CL12
UL2
VDD
A0+
A0-
A1+
A1-
A2+
A2-
A3+
A3-
SEL
LEDA0
LEDA1
LEDA2
PD
PAD_GND
B0+
B0-
B1+
B1-
B2+
B2-
B3+
B3-
LEDB0
LEDB1
LEDB2
C0+
C0-
C1+
C1-
C2+
C2-
C3+
C3-
LEDC0
LEDC1
LEDC2
LAN_MIDI3-
LAN_MIDI3+
LAN_MIDI2-
LAN_MIDI2+
LAN_MIDI1-
LAN_MIDI1+
LAN_MIDI0-
LAN_MIDI0+
LAN_ACTIVITY#_DOCK
LAN_LINK#_DOCK
LAN_MIDI3-_RJ45
LAN_MIDI3+_RJ45
LAN_MIDI2-_RJ45
LAN_MIDI2+_RJ45
LAN_MIDI1-_RJ45
LAN_MIDI1+_RJ45
LAN_MIDI0-_RJ45
LAN_MIDI0+_RJ45
To Docking.
SEL:Low
To RJ45 conn
SEL:High
DET_SIG#_R
RL13
RL18
10K_0402_5%
PI3L720ZHEX_TQFN42_9X3P5-D
SA00003B200
PCH_PCIE_WAKE#
RL19
0_0402_5%
LAN_PME#
SOC_SML0CLK
SOC_SML0DATA
QL2A
QL2B
DMN66D0LDW-7_SOT363-6
RL16
499_0402_1%
RL15
499_0402_1%
LAN_SCLK
LAN_SDATA
RL7
RL12
RL11
10K_0402_5%
DET_SIG#_R
JTAG_TMS_LAN
JTAG_TCK_LAN
NOTE: Default SMBus Address is 0xC8
SMBUS PULL-UP OPTIONS
SMBUS SPEED
RL15 & RL16
1MHz(Defaul setting)
499ohm
Security Classification
Compal Secret Data
Issued Date
2016/07/29
Deciphered Date
2016/07/29
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LAN Intel I219
Size
Custom
Document Number
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Rev
1.0
Date:
Thursday, December 15, 2016
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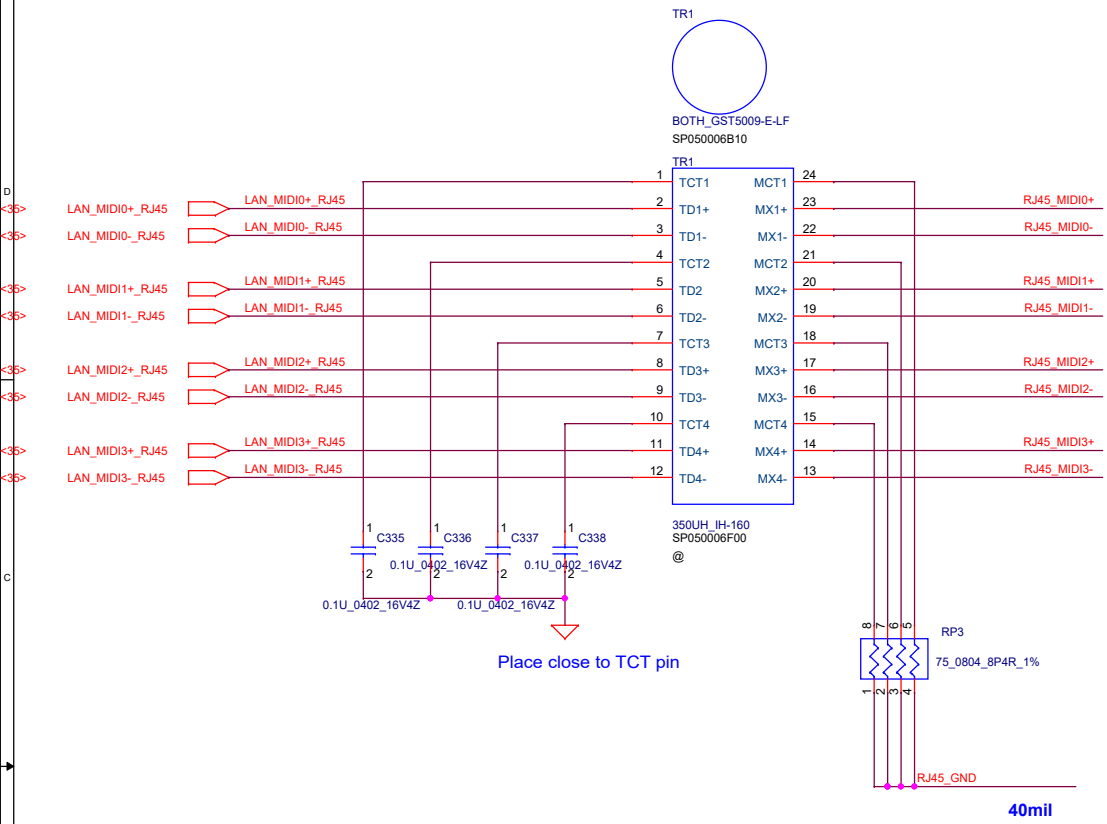
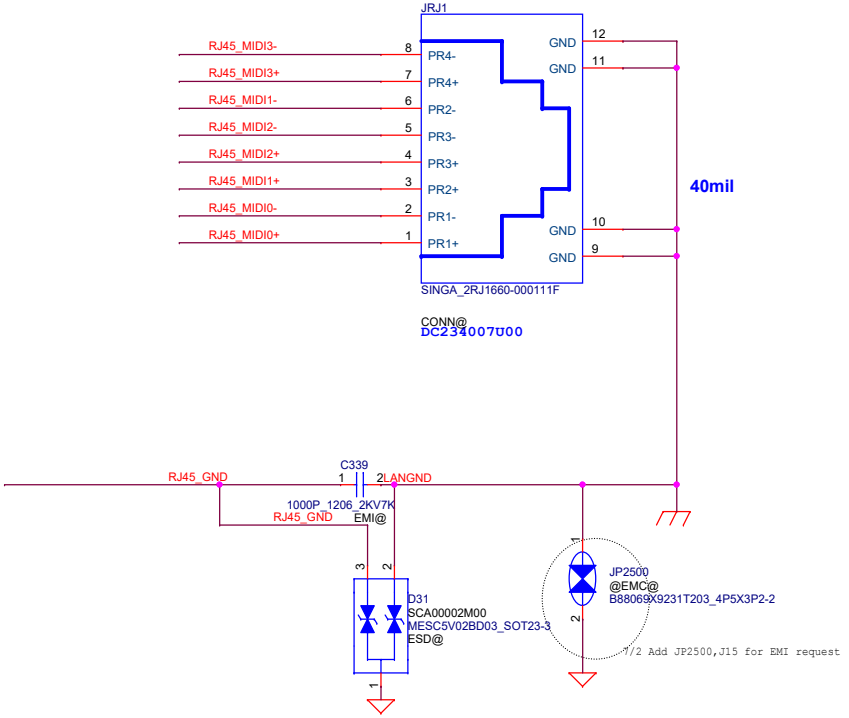
35
of
64

LAN Connector





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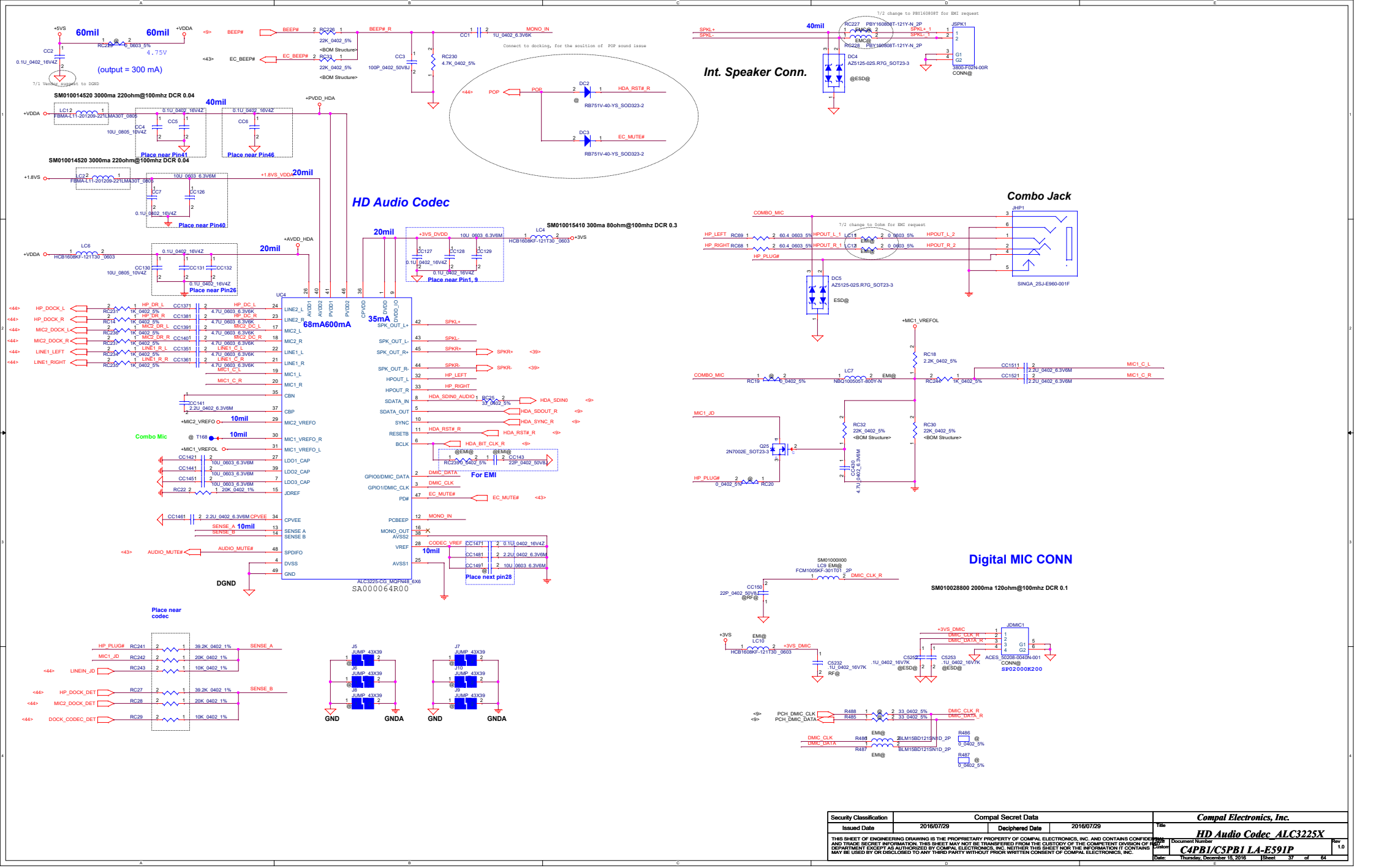
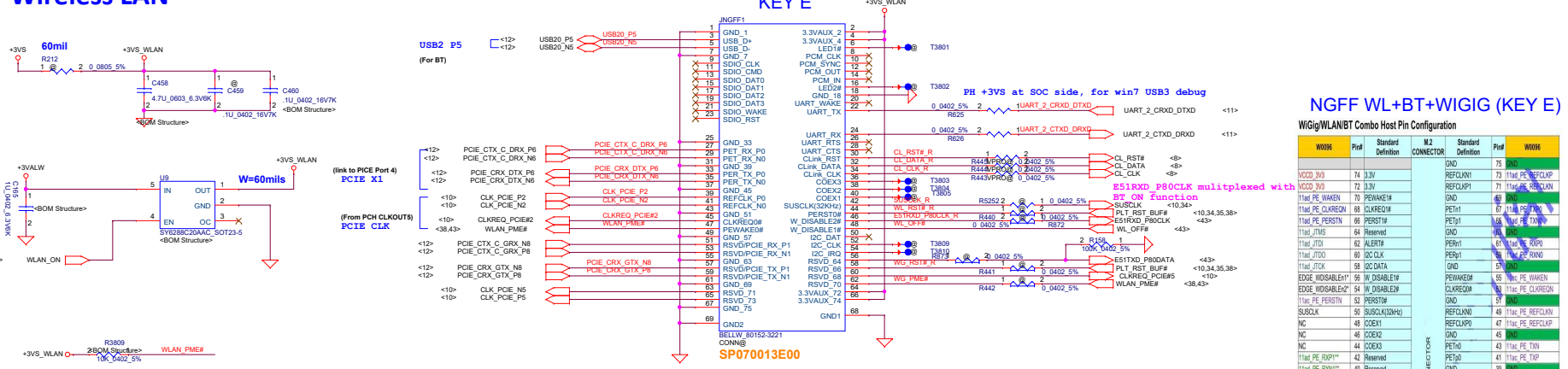
Title	LAN Magnetic & RJ45		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 36 of 64		


HD Audio Codec
Int. Speaker Conn.
Combo Jack
Digital MIC CONN
Int. Speaker Conn.
(output = 300 mA)
4.75V
SM010014520 3000ma 220ohm@100mhz DCR 0.04
SM010015410 300ma 80ohm@100mhz DCR 0.3
SM010028800 2000ma 120ohm@100mhz DCR 0.1
68mA600mA
35mA
For EMI
Combo Mic
DGND
GND
GNDA
SA000064R00
ALC3225-CG_MQFN48_6X6
Place near codec
Place next pin28
Place near Pin41
Place near Pin46
Place near Pin40
Place near Pin26
Place near Pin1, 9
SINGA_2SJ-E960-001F
SP02000K200
Security Classification
Compal Secret Data
Issued Date
2016/07/29
Deciphered Date
2016/07/29
Compal Electronics, Inc.
HD Audio Codec_ALC3225X
C4PBJ/C5PB1 LA-E591P
Rev 1.0
Thursday, December 15, 2016
Sheet 37 of 64

Wireless LAN



NGFF WL+BT+WIGIG (KEY E)

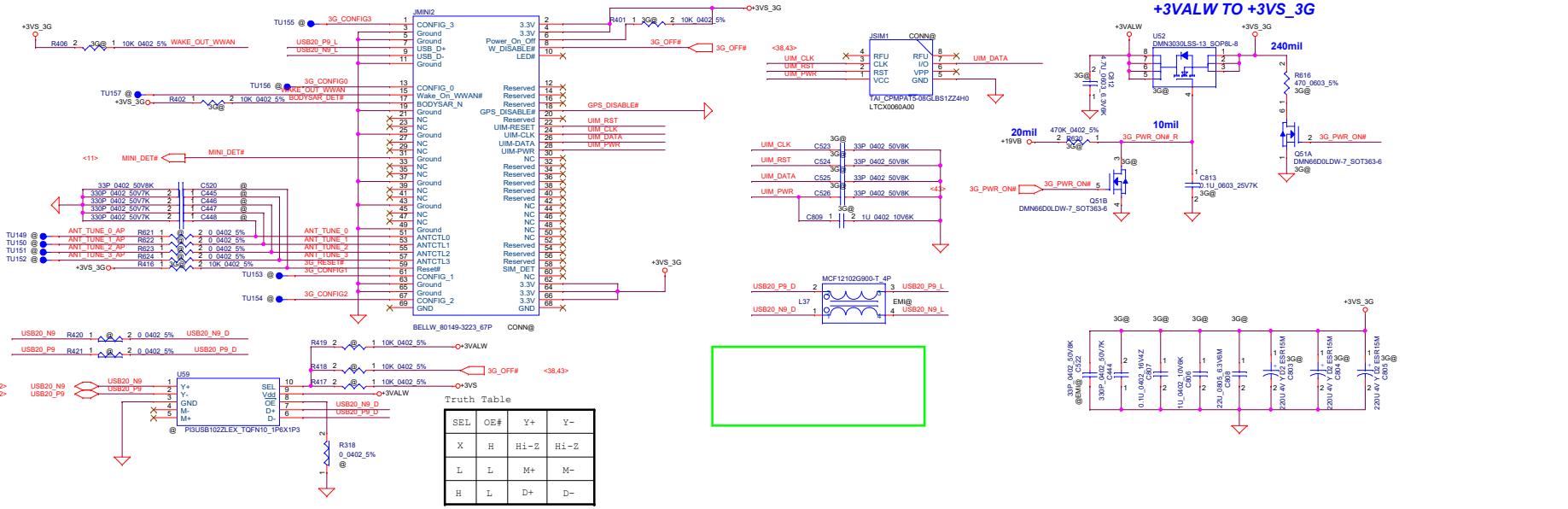
WiGig/WLAN/BT Combo Host Pin Configuration

W0J96	Pin#	Standard Definition	M.2 CONNECTOR	Standard Definition	Pin#	W0J96
				GND	75	GND
VCCD_3V3	74	3.3V		REFCLKN1	73	11ad_PE_REFCLKP
VCCD_3V3	72	3.3V		REFCLKP1	71	11ad_PE_REFCLKN
11ad_PE_WAKEN	70	PEWAKE1#		GND	69	GND
11ad_PE_CLKREQN	68	CLKREQ1#		PETn1	67	11ad_PE_TXN3
11ad_PE_PERSTN	66	PERST1#		PETp1	65	11ad_PE_TXP3
11ad_JTMS	64	Reserved		GND	63	GND
11ad_JTDI	62	ALERT#		PERn1	61	11ad_PE_RXP0
11ad_JTDO	60	I2C CLK		PERp1	59	11ad_PE_RXN0
11ad_JTCK	58	I2C DATA		GND	57	GND
EDGE_WDISABLE1**	56	W_DISABLE1#		PEWAKE0#	55	11ac_PE_WAKEN
EDGE_WDISABLE2*	54	W_DISABLE2#		CLKREQ0#	53	11ac_PE_CLKREQN
11ac_PE_PERSTN	52	PERST0#		GND	51	GND
SUSCLK	50	SUSCLK(32KHz)		REFCLKN0	49	11ac_PE_REFCLKN
NC	48	COEX1		REFCLKP0	47	11ac_PE_REFCLKP
NC	46	COEX2		GND	45	GND
NC	44	COEX3		PETn0	43	11ac_PE_TXN
11ad_PE_RXP1**	42	Reserved		PETp0	41	11ac_PE_TXP
11ad_PE_RXN1**	40	Reserved		GND	39	GND
GND	38	Reserved		PERn0	37	11ac_PE_RXN
11ad_PE_TXP1**	36	N/C		PERp0	35	11ac_PE_RXP
11ad_PE_TXN1**	34	N/C		GND	33	GND
GND	32	N/C		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		N/C	23	NC
11ad_JTRST	22	N/C		N/C	21	NC
NC	20	N/C		N/C	19	NC
GND	18	GND		N/C	17	NC
EDGE_LED2*	16	LED2#		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		GND	7	GND
EDGE_LED1*	6	LED1#		USB_D-	5	11ac_USB_DNEG
VCCD_3V3	4	3.3V		USB_D+	3	11ac_USB_DPOS
VCCD_3V3	2	3.3V		GND	1	GND

3.1.8.1.3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RTS~~ UART_RXD (Input): Receive Data
- ~~RTS~~ UART_TXD (Output): Transmit Data
- UART_RTS (Input): Request to Send (Host Flow Control)
- UART_CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake Up~~UART_Wake# (Output): Host wake-up line is optional in case the host support in band wake-up



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

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Compal Electronics, Inc.	
Title	mini Card & LTE CONN.
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P
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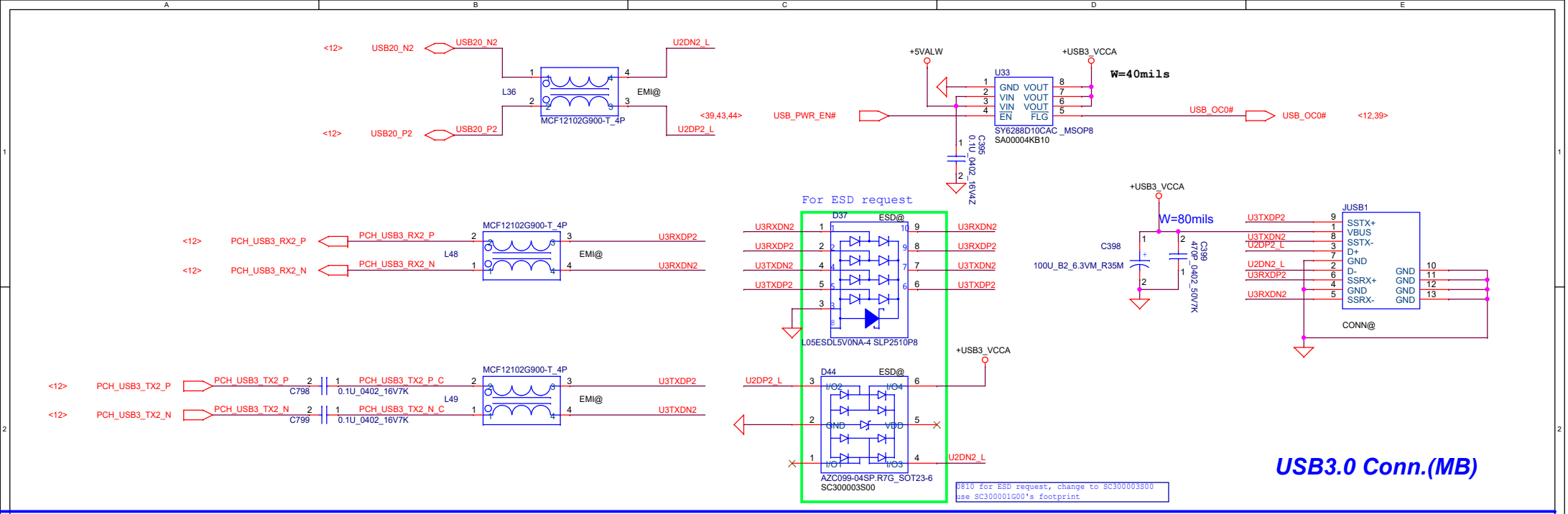
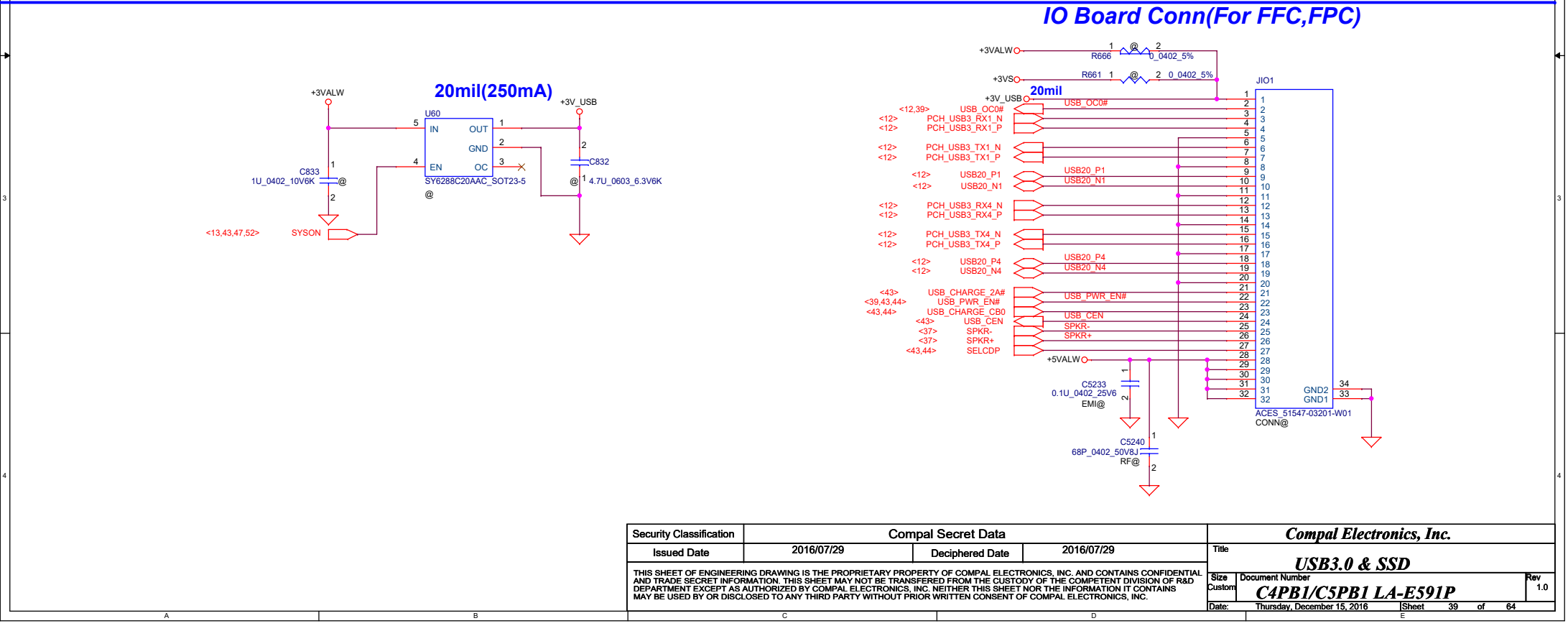
Date: Thursday, December 15, 2016	Sheet 38 of 84





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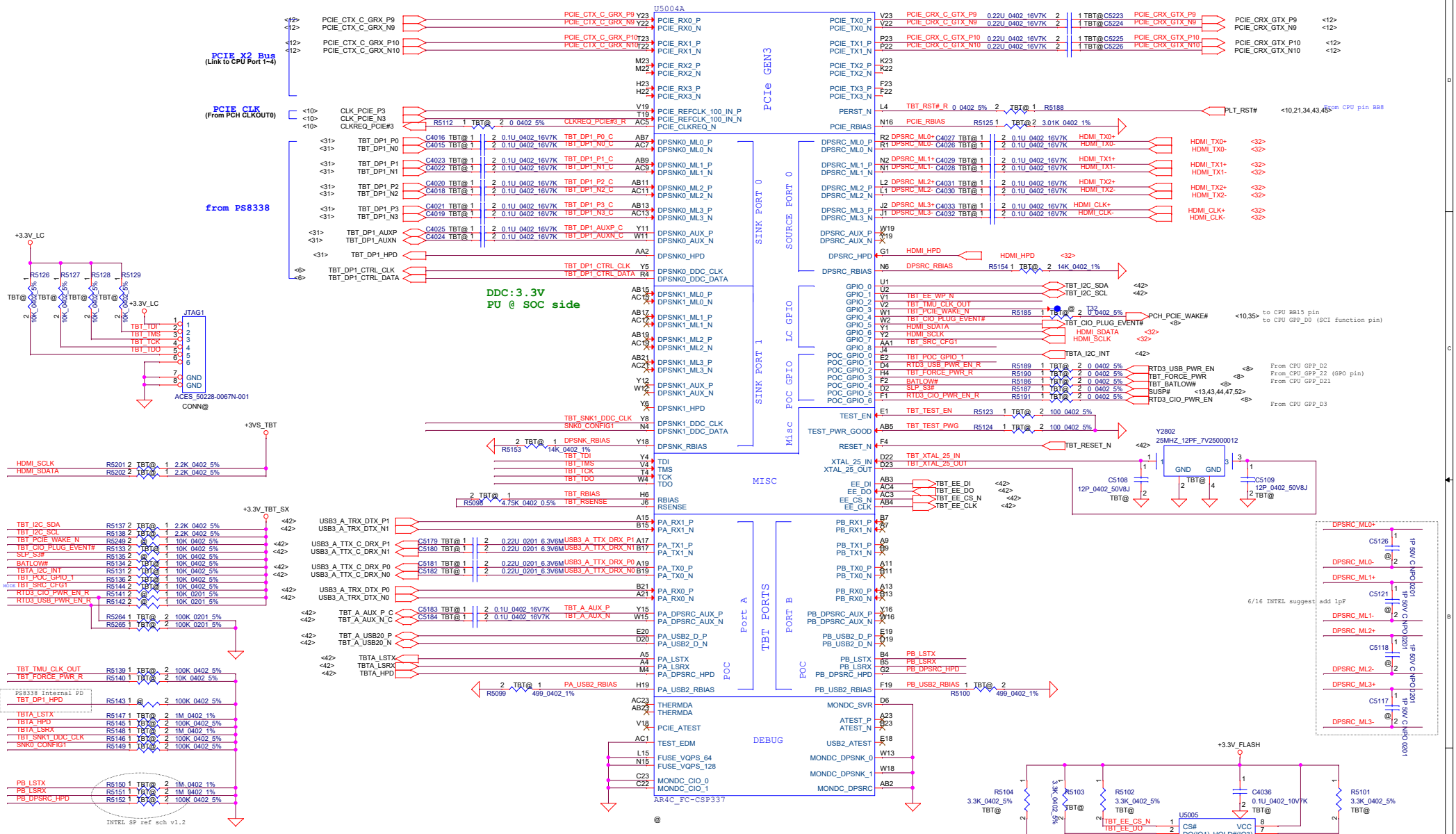
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: USB3.0 & SSD

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Thursday, December 15, 2016 | Sheet 39 of 64



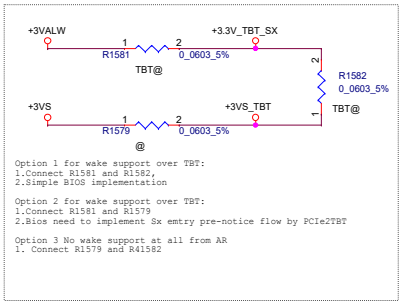
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: Alpine Ridge

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

Date: Thursday, December 15, 2016 | Sheet 40 of 64



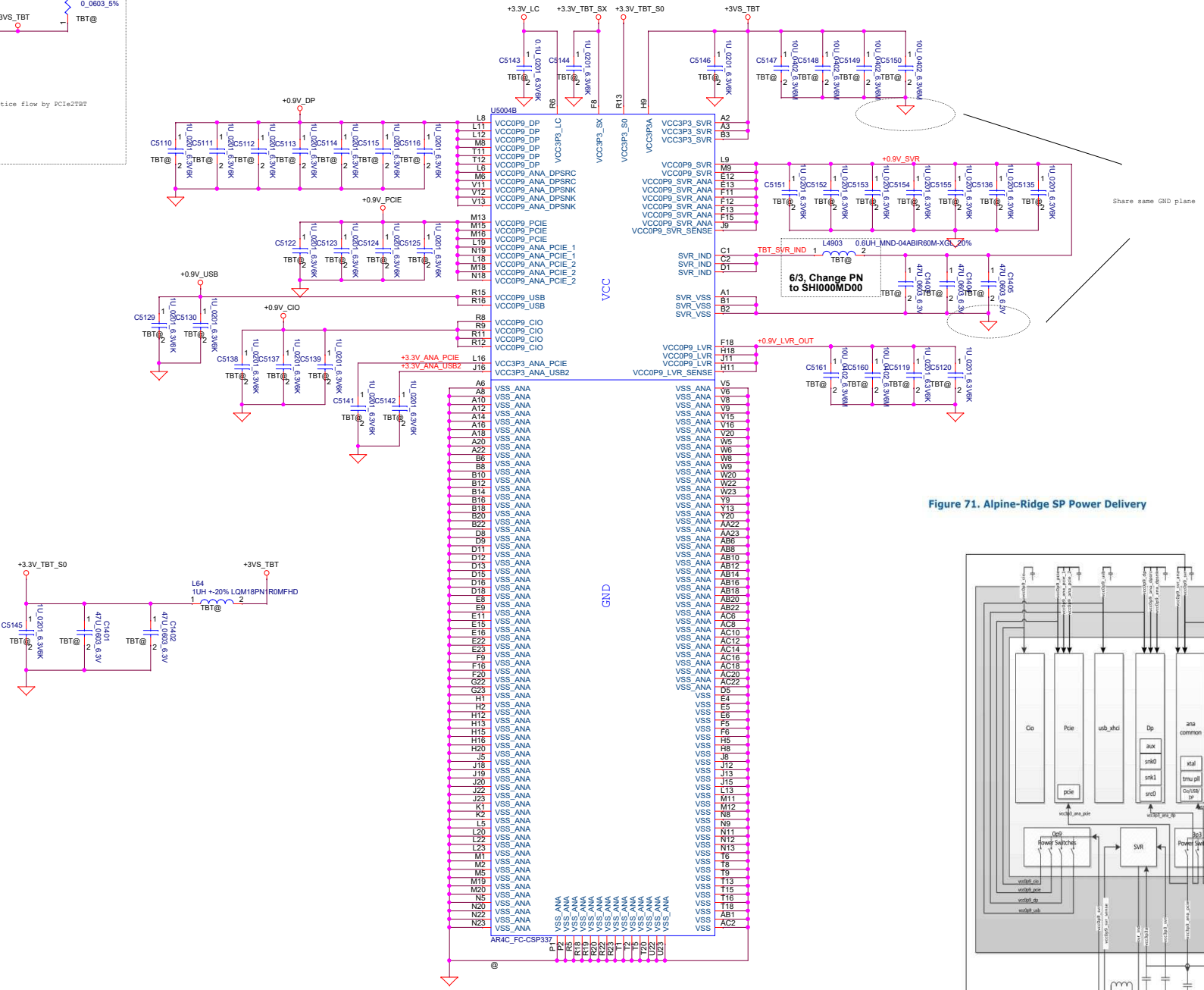


Figure 71. Alpine-Ridge SP Power Delivery

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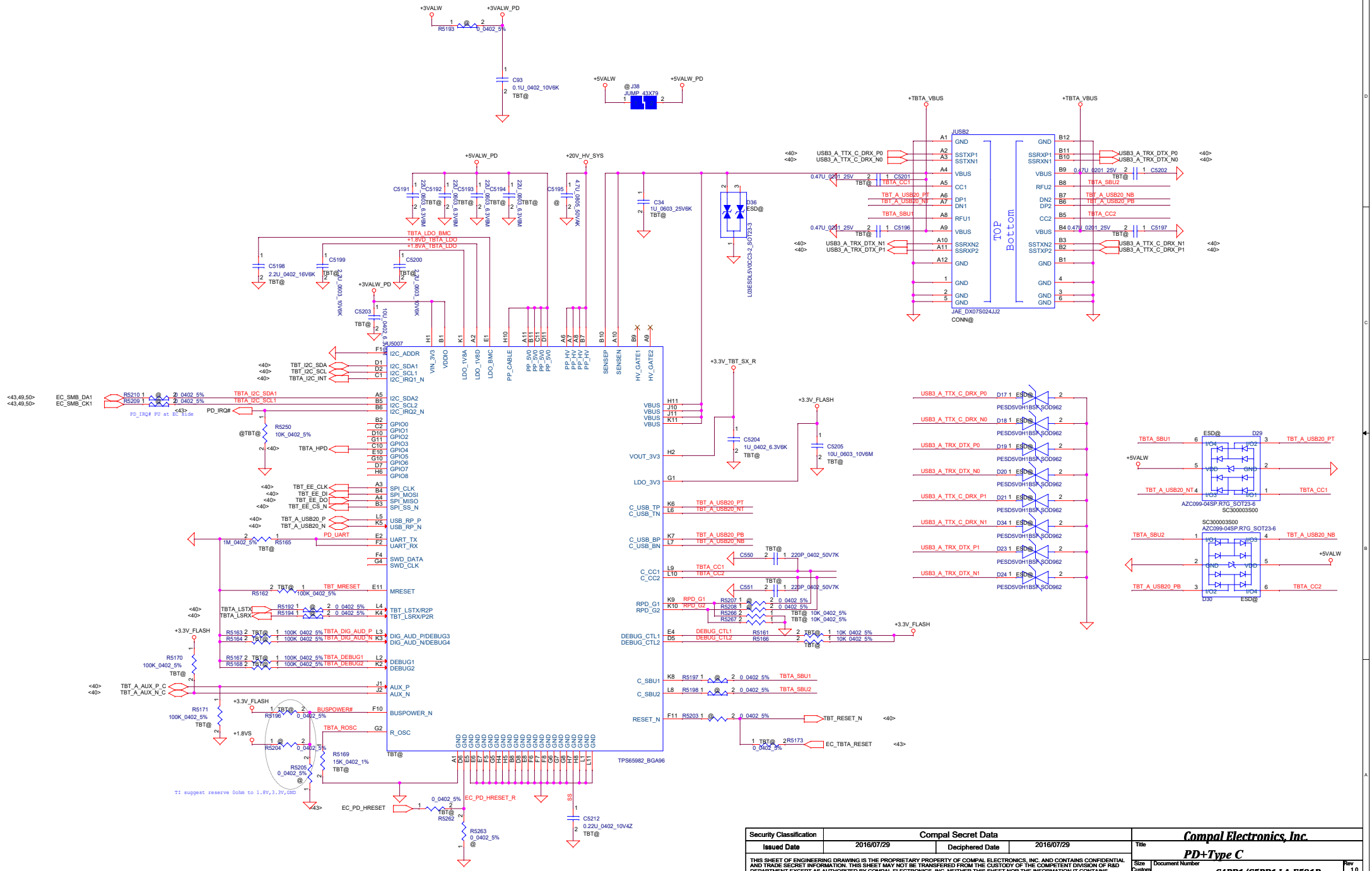
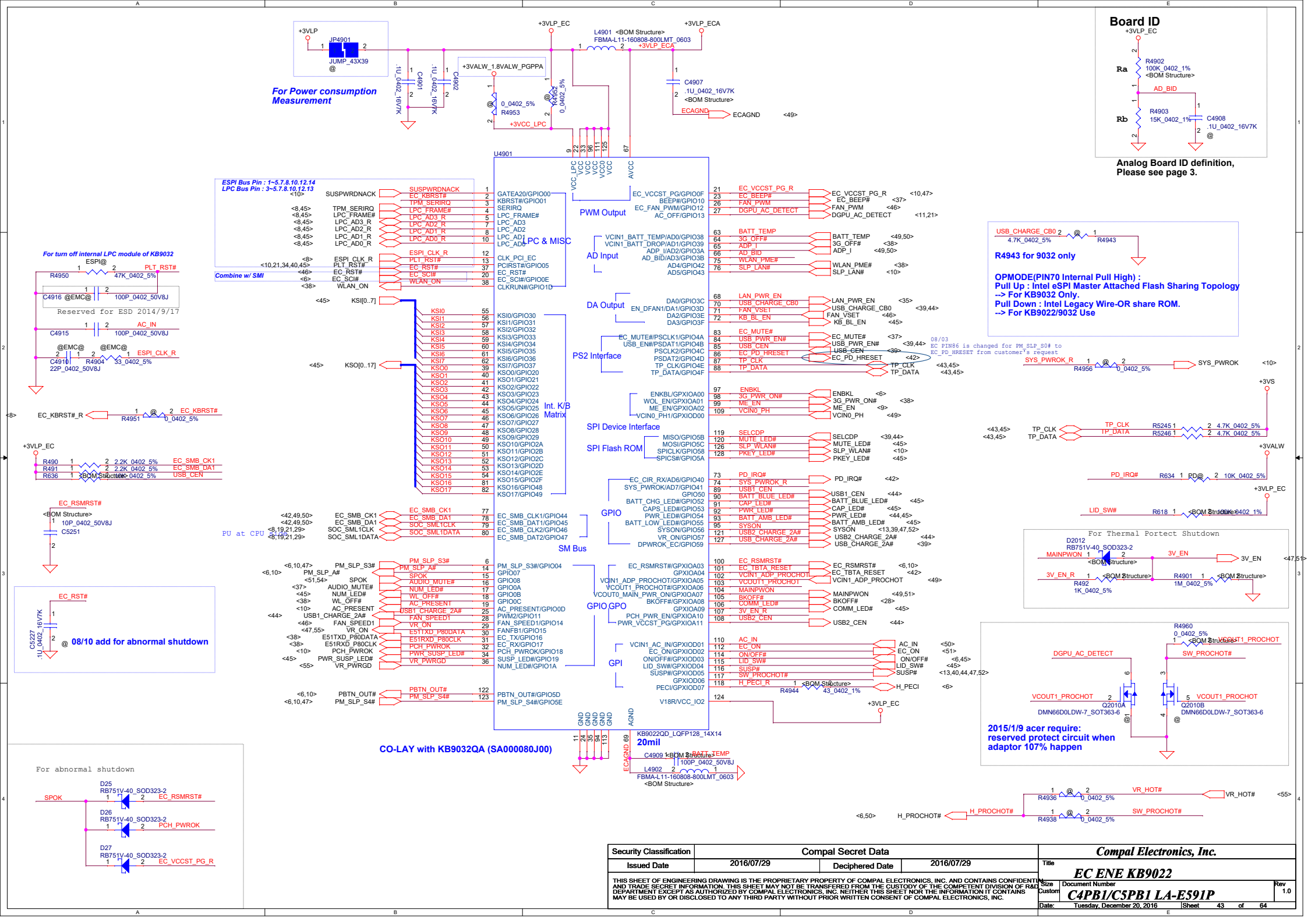
Compal Electronics, Inc.			
Title: Alpine Ridge-POWER			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet: 41	of: 64	



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: PD+Type C			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Monday, December 26, 2016	Sheet 42 of 64		



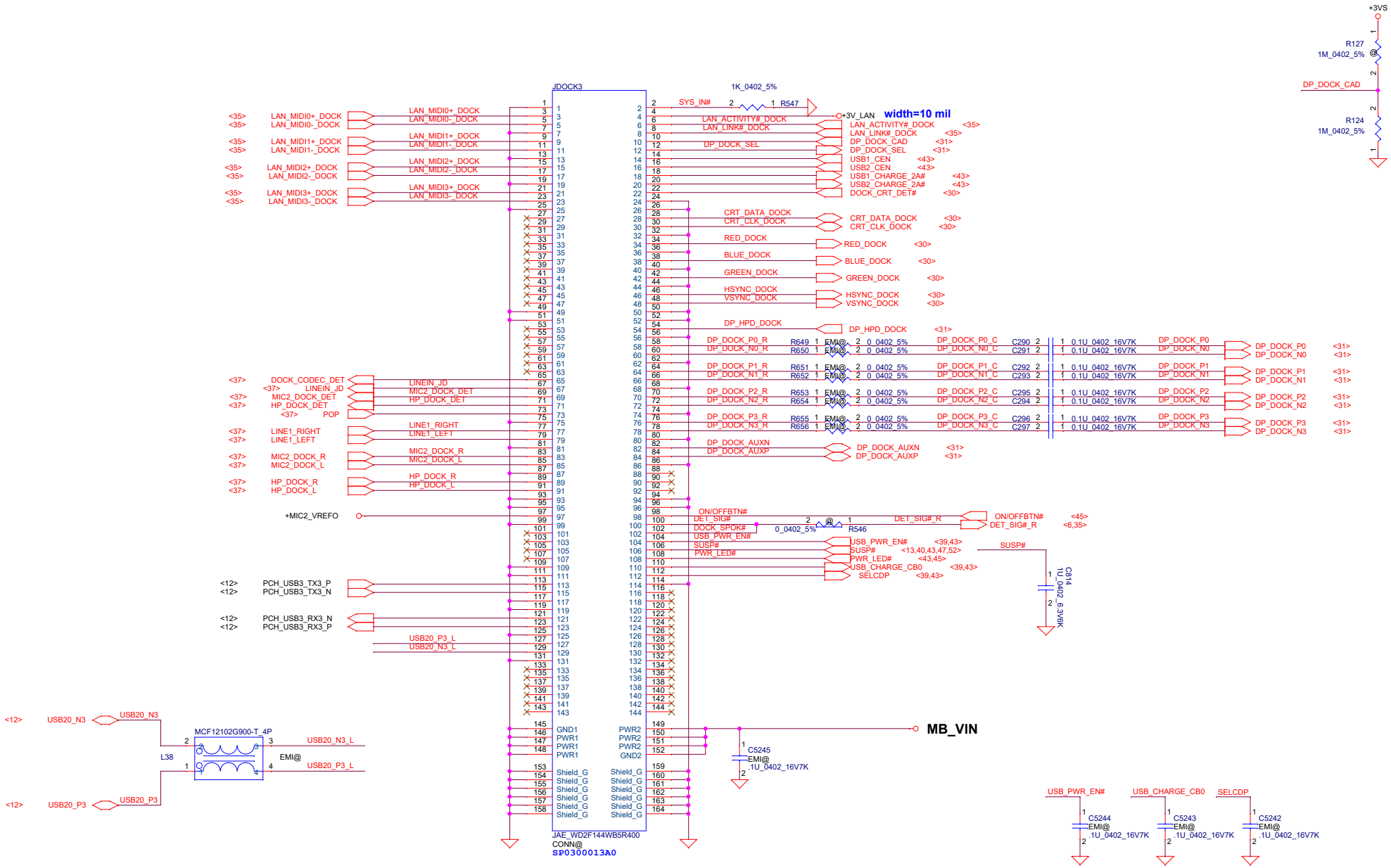
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: EC ENE KB9022

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Tuesday, December 20, 2016 | Sheet 43 of 64



Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.	
Title	E Series Dcok CONN.
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P
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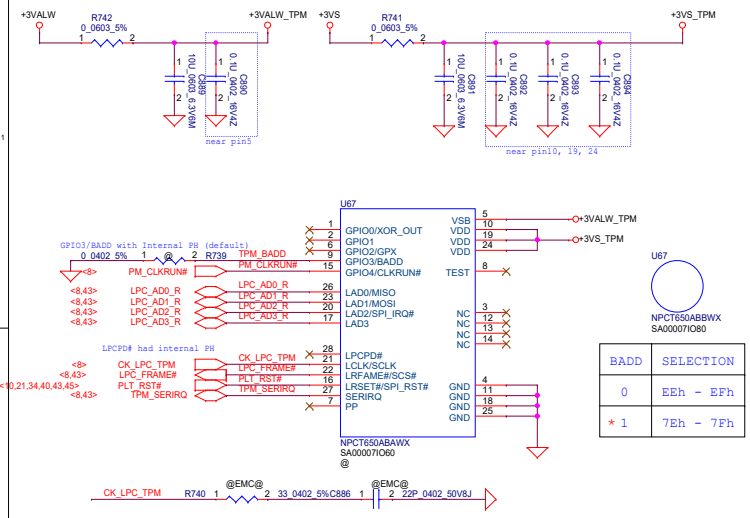
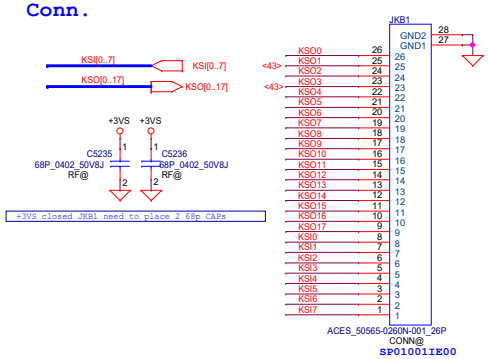
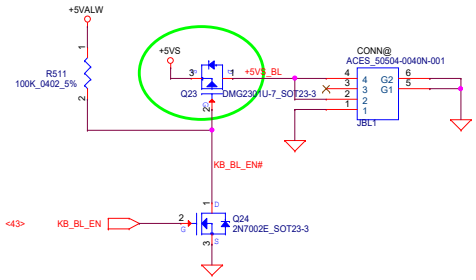
TPM



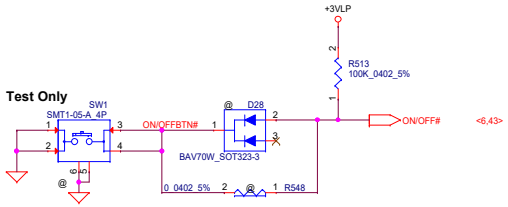
KB Conn.



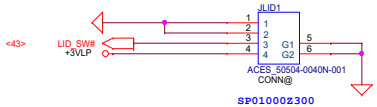
KB Backlight Conn



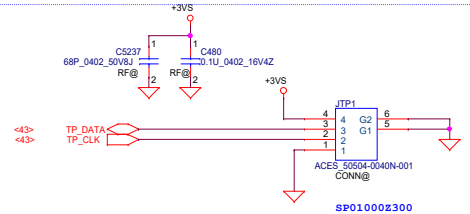
ON/OFF BTN



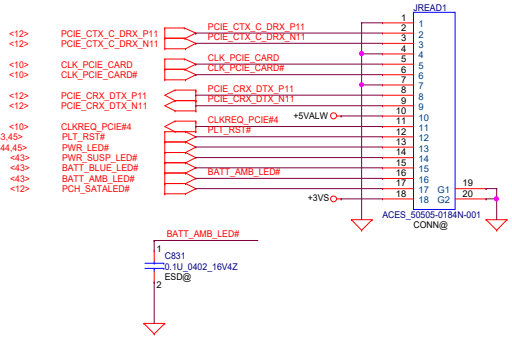
Lid Switch/B
(Hall Effect Switch)



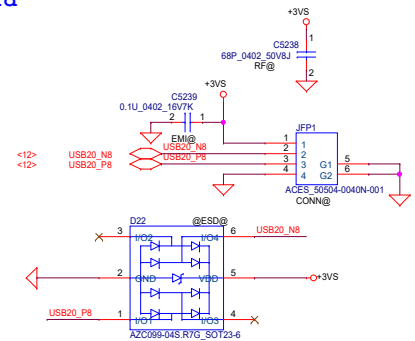
TP Conn.



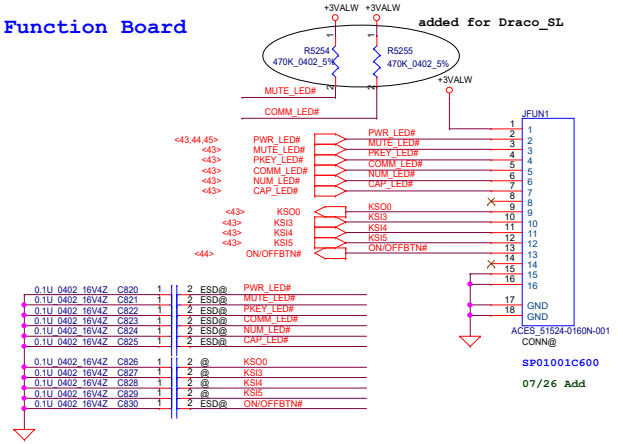
CardReader Board



FP Board



Function Board



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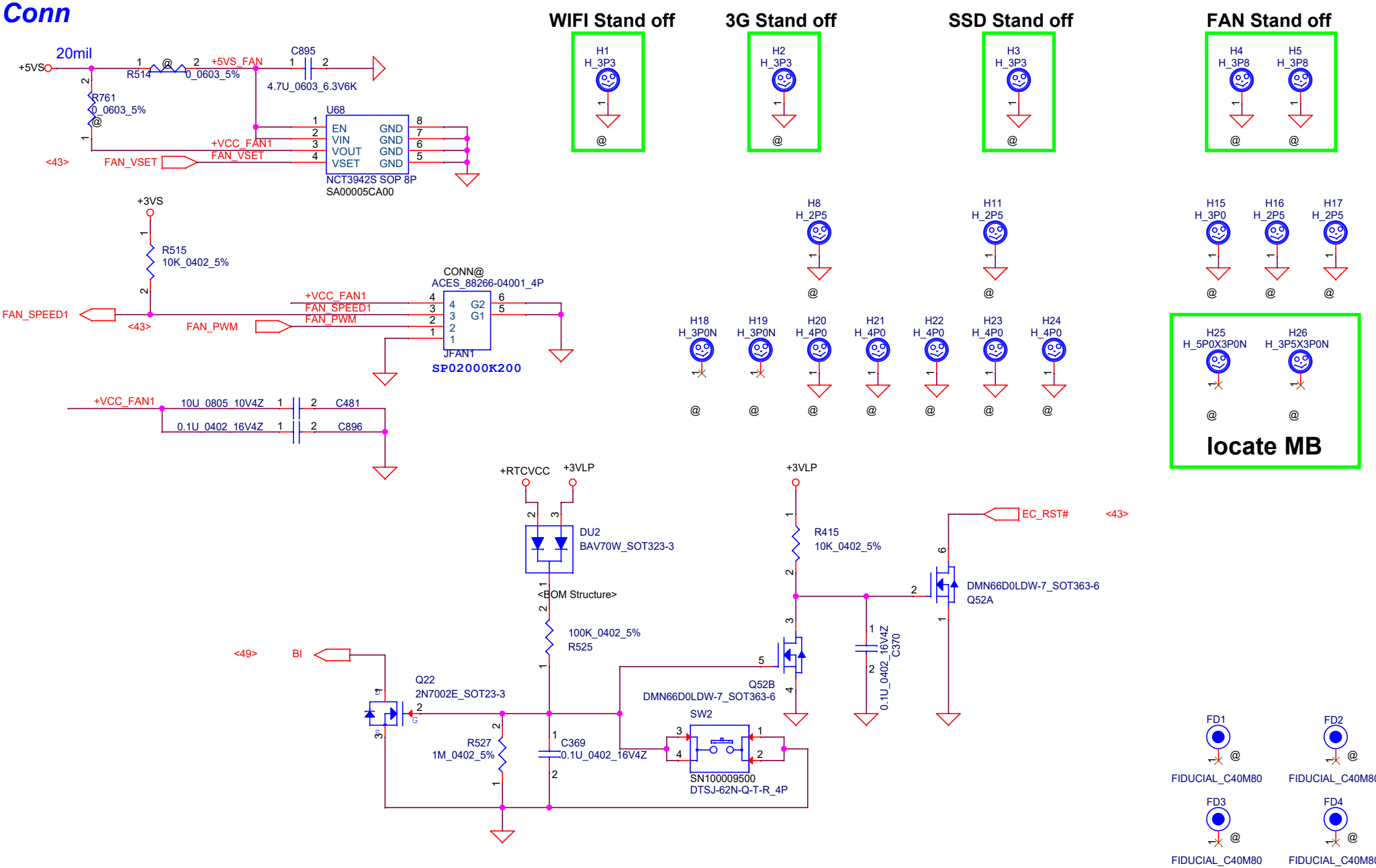
Compal Electronics, Inc.			
Title: KB/TP/LID/TPM/FUN/FP/CARD			
Size: C	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 45 of 64		

FAN Conn



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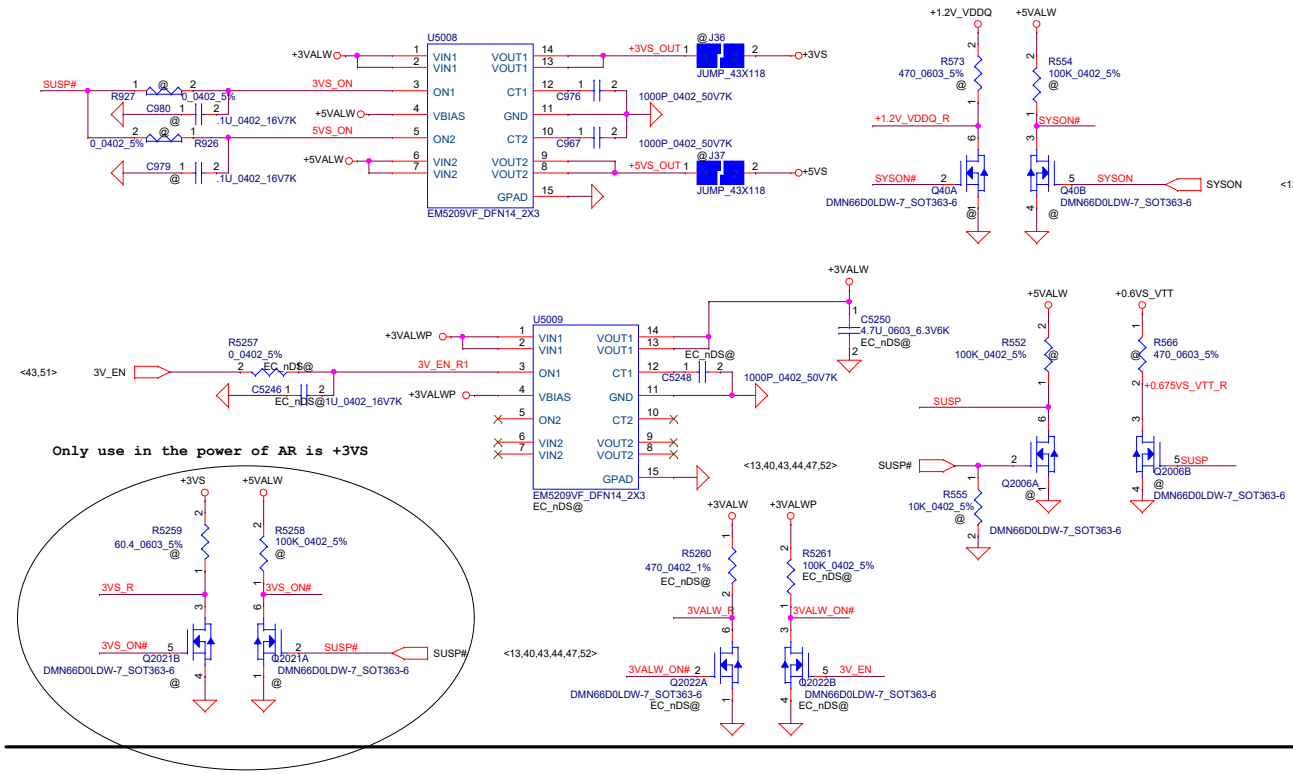
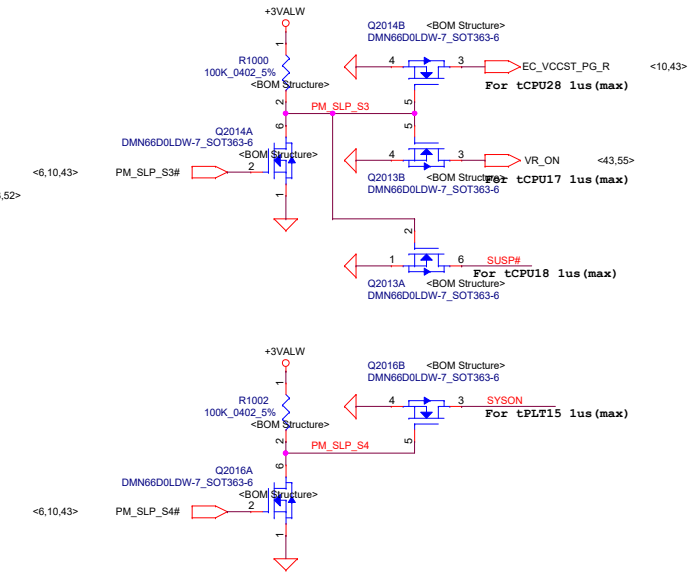
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.			
Title: FAN & Screw			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 46 of 64		

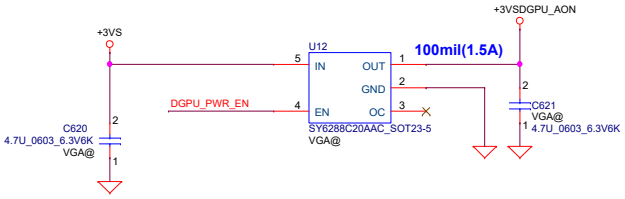
DC & VGA Interface



For Power Off Sequence

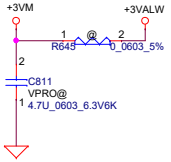


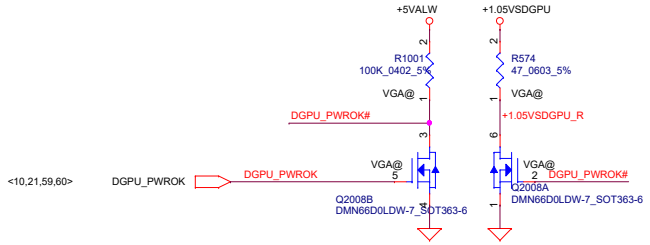
+3VS to +3VSDGPU_AON for GPU



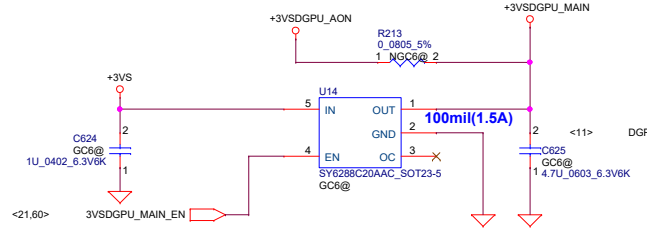
+3VALW to +3VM for Intel AMT

20mil(68mA)

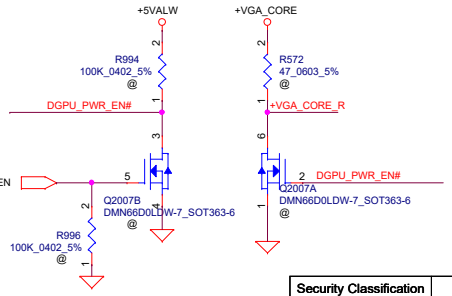


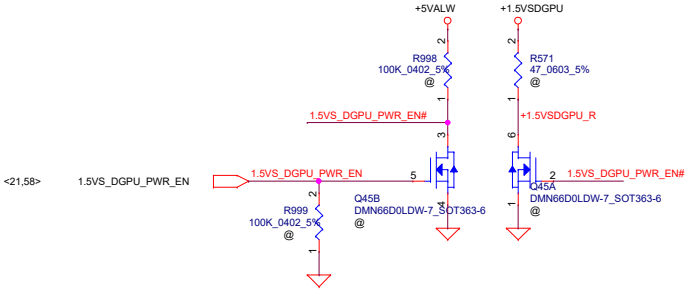


+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU





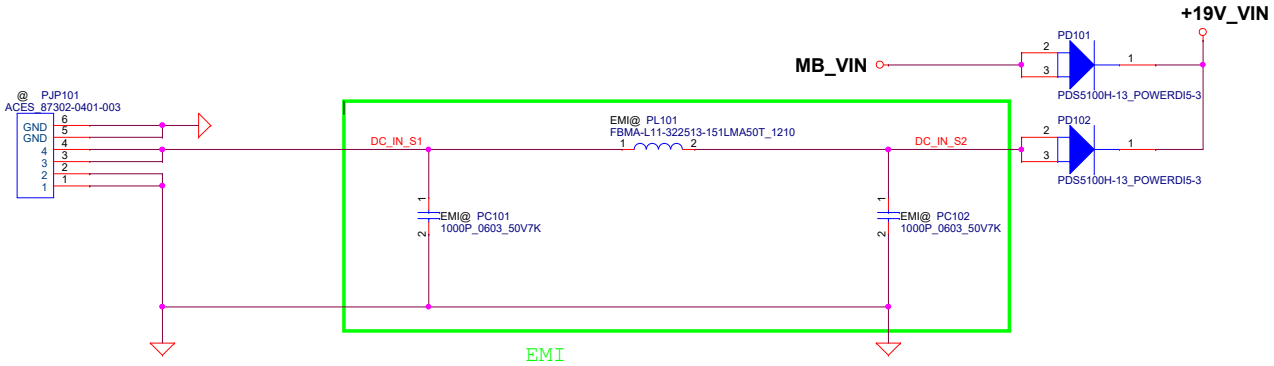
Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

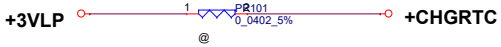
Compal Electronics, Inc.

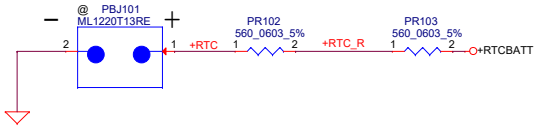
Title: DC Interface

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0
Date: Thursday, December 15, 2016	Sheet 47 of 64	

2015/7/8
PD101 and PD102 SCS00002F00 change to SCS00002M00







Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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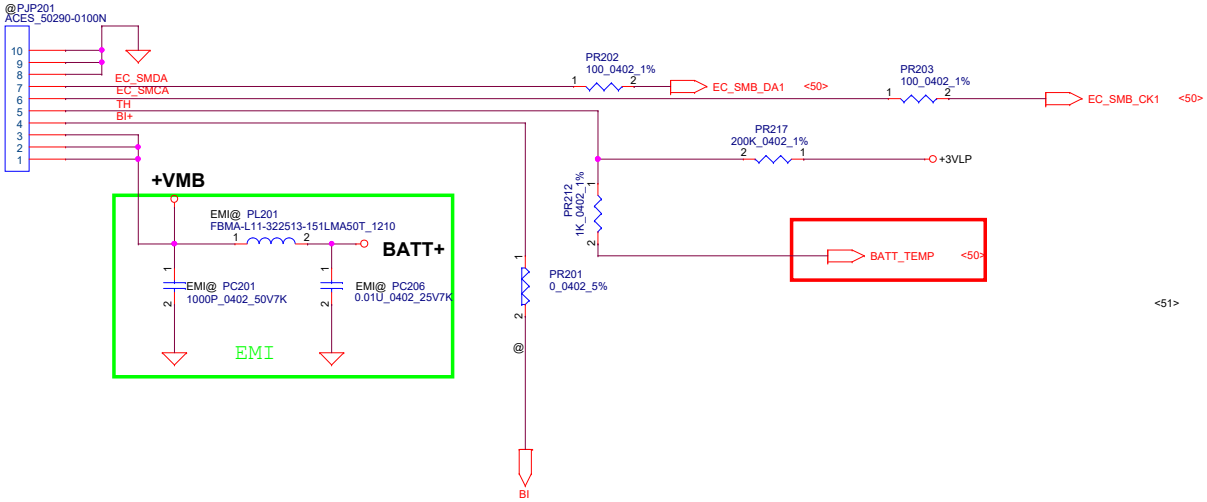
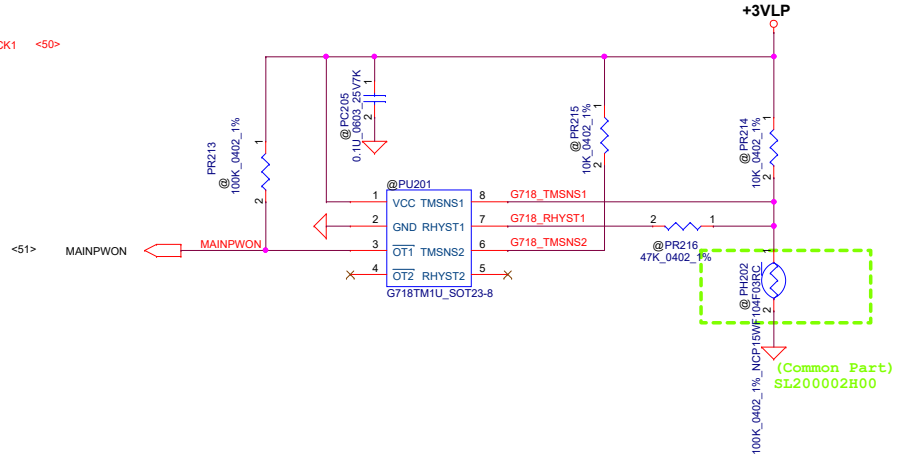
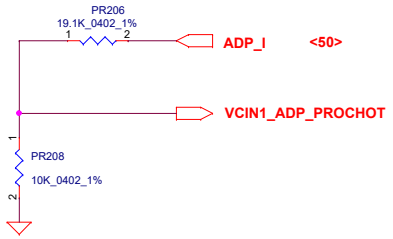




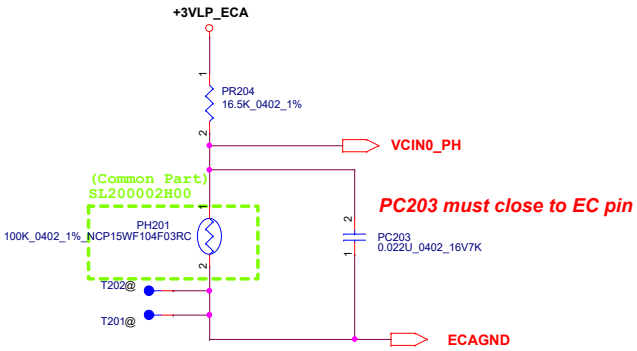
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

2015/07/09 update

For KB9022 sense 20mΩ	Active	Recovery
65W PR206 19.1K ohm SD034191280	84.5W,0.61V	65W,0.47V



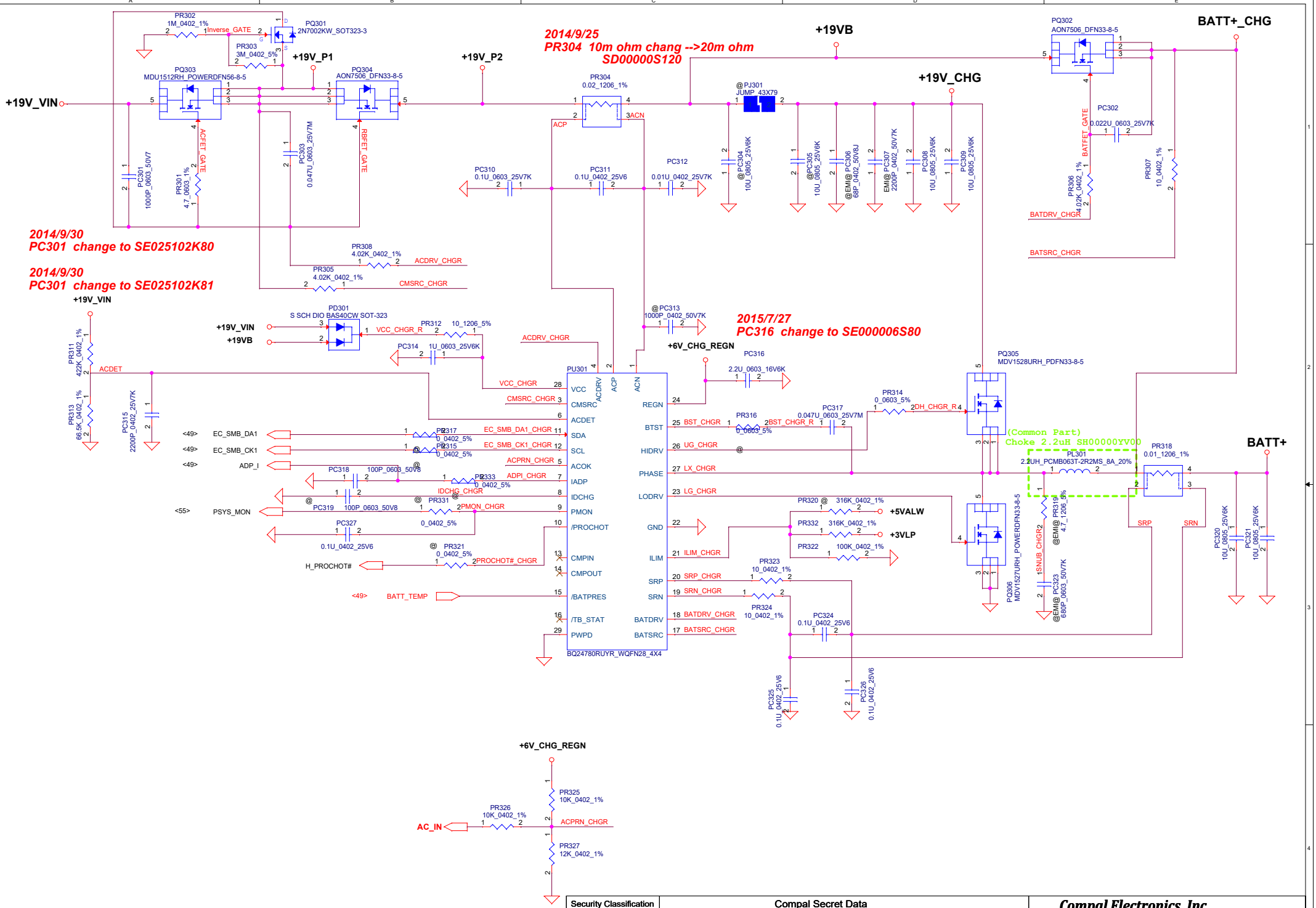
T202 T201 must close to PH201



PC203 must close to EC pin

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 49 of 64		



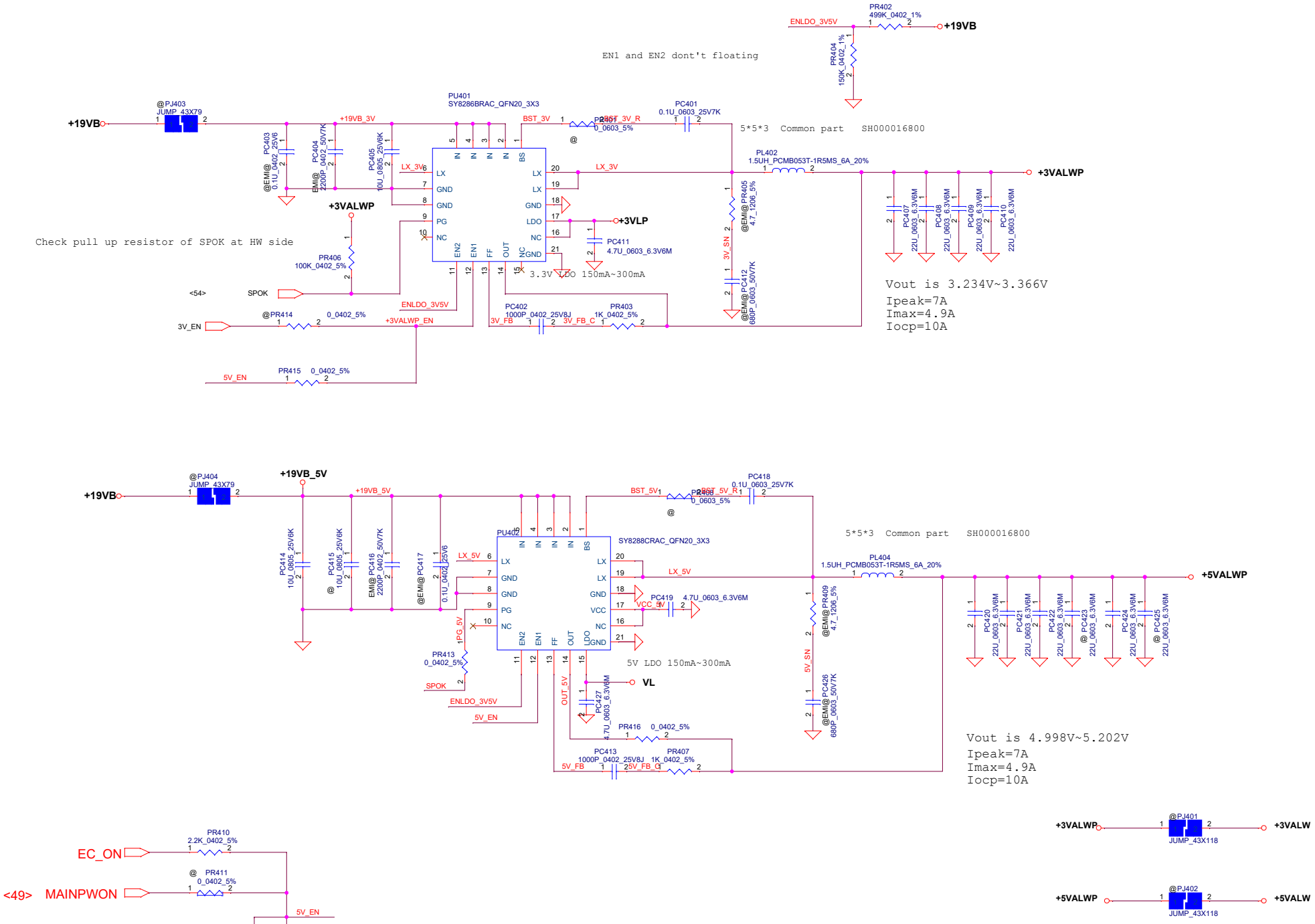
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: BQ24780

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

Date: Thursday, December 15, 2016 | Sheet 50 of 64



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: PWR-3.3VALWP/5VALWP			
Size: Custom	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 51 of 64		

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question, you can change from +1.2VP to +1.2VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Choke 1.5uH SH000016700
Common Part 7*7*3

Update Pc510 change to Common Part SF000006S00 20141227

change PQ502 form 7506 to 7716, 20150108

Change PR503 to 17.8K ohm
OCP setting 9.6A

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(6.19/10))
=1.2V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~9.6A
OVP: 110%~120%
VFB=0.75V, Vout=1.2V
MOSFET footprint: SIS412DN

3.8x3.8xH1.8
DCR: 20~25mohm
Idc / Isat: 3.8A

Iocp : 3.7A
FSW : 1MHz

Rdown

5/29 add PC526
In order to avoid capacitor decay

Vout=0.6V* (1+Rup/Rdown)
2.504V= 0.6V*(1+36.5K/11.5K)

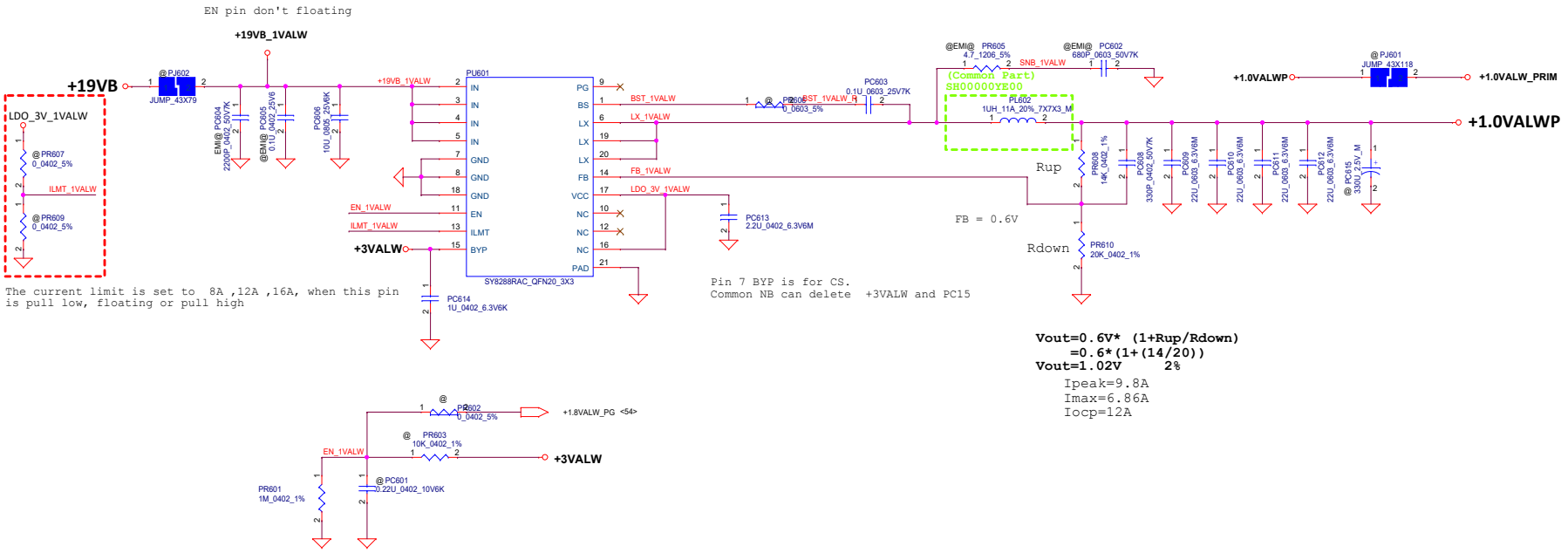
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Thursday, December 15, 2016 | Sheet 52 of 64



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

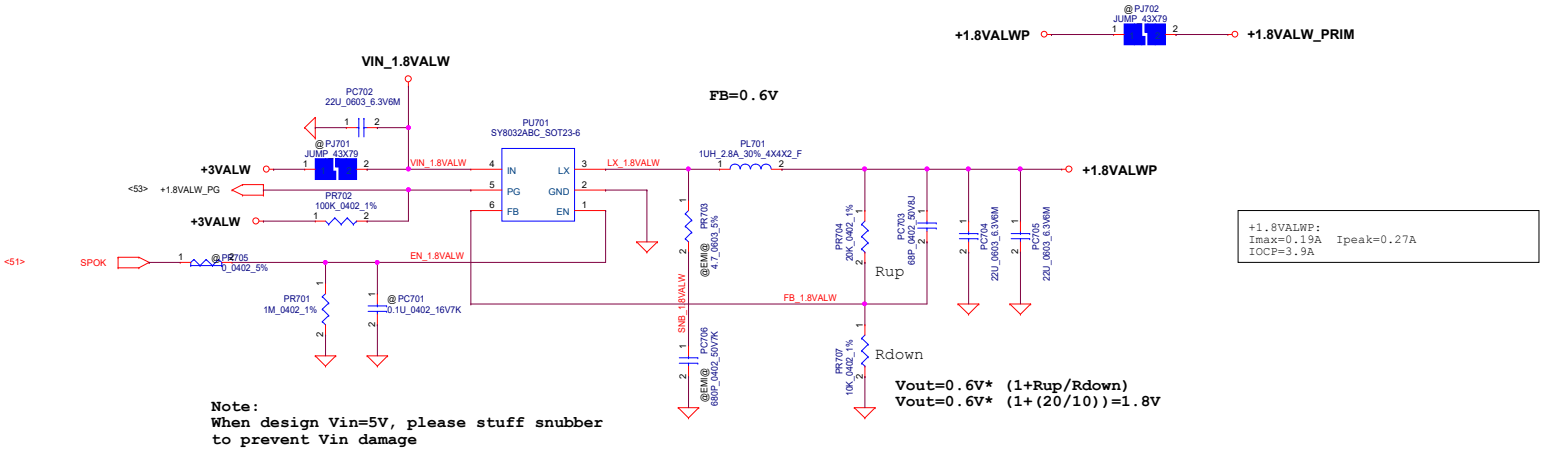
Title: +1.0VALWP

Size	Document Number	Rev
C	C4PB1/C5PB1 LA-E591P	1.0

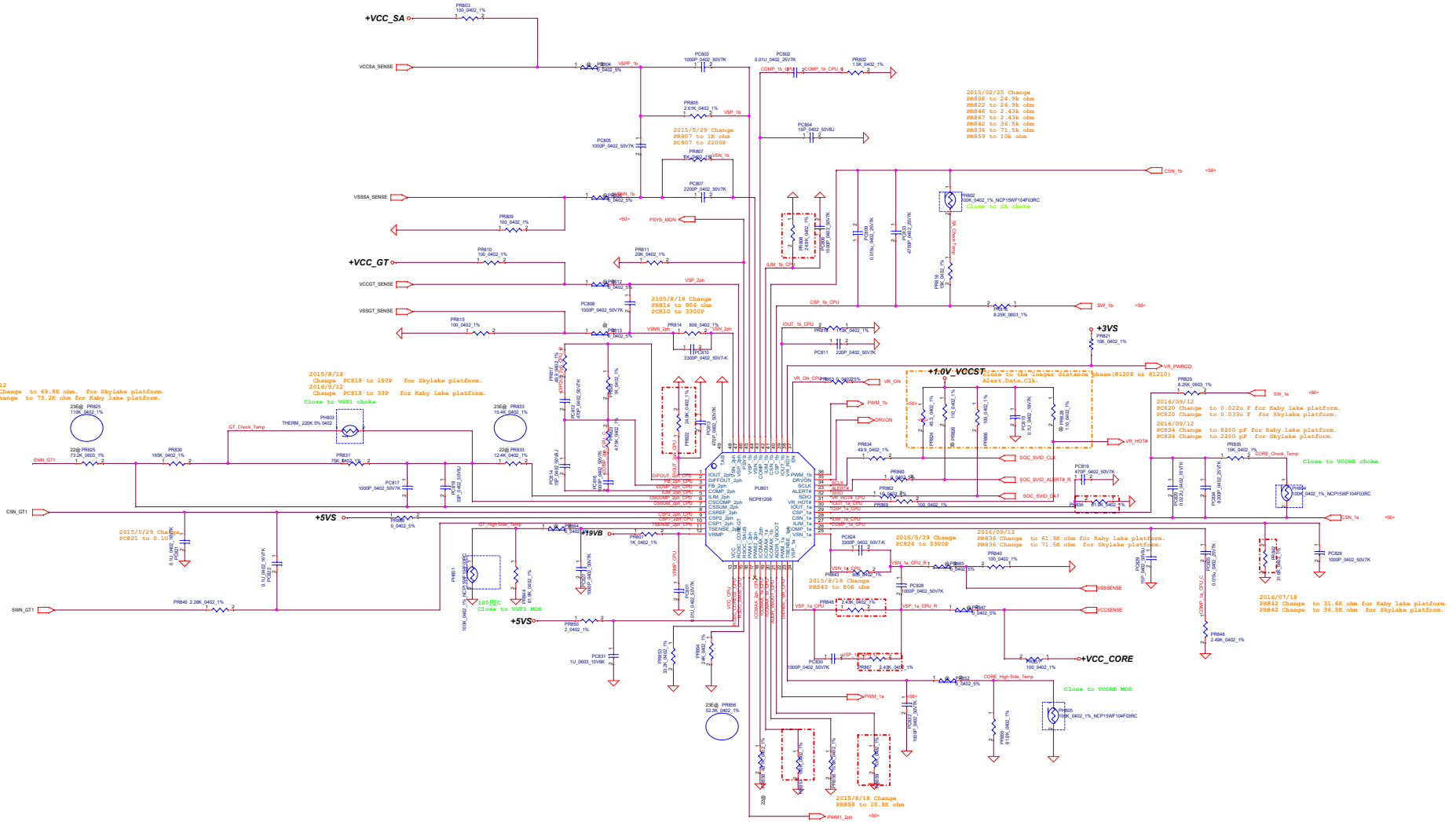
Date: Thursday, December 15, 2016 Sheet 53 of 64

Module model information

SY8032_V2.mdd



Compal Electronics, Inc.			
Title: SY8032			
Size: C	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet 54 of 64		



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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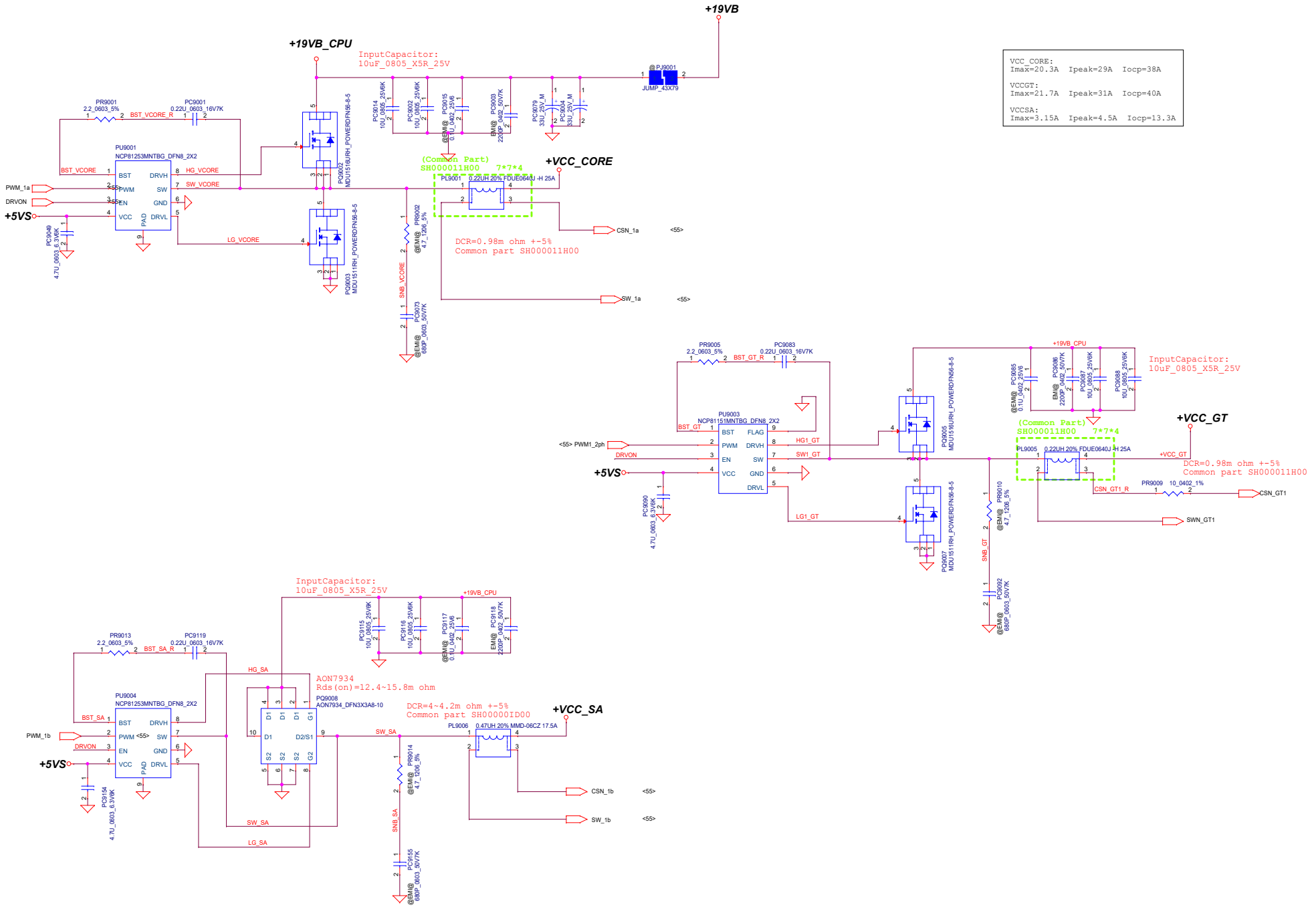
Compal Electronics, Inc.			
Title: IMVP8, NCP81208			
Size: D	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
Date: Thursday, December 15, 2016	Sheet: 55 of 64		



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: Power Train			
Size: C	Document Number: C4PB1/C5PB1 LA-E591P		Rev: 1.0
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Total VCORE Output Capacitor:
2015/07/09
22uF_0603_28PCS
1uF_0201_35PCS
UNPOP 0603_8PCS, 0201_3PCS, 330uF_R9_2PCS

+VCC_CORE

(Common Part)
SGA00009S00

+VCC_CORE

20150709
D2*1 22uF_0603*30 1uF_0201*9
unpop: 22uF_0603*8 1uF_0201*11

+VCC_GT

(Common Part)
SGA00009S00

1u_0201 SE00000U200比較貴,
故改1u_0201 SE00000UC00.

20140703
22uF_0603*6 1uF_0201*7
unpop: 22uF_0603*6

+VCC_SA

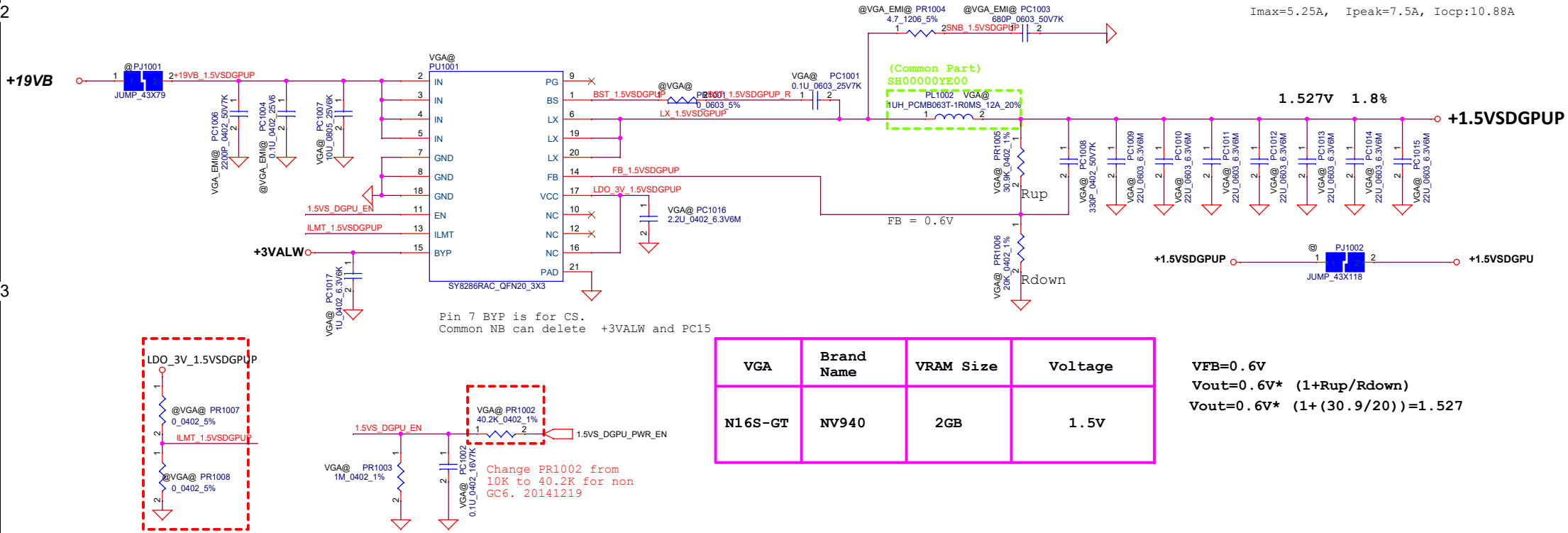
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	C4PB1/C5PB1 LA-E591P	1.0

Date: Thursday, December 15, 2016 Sheet 57 of 64



VGA	Brand Name	VRAM Size	Voltage
N16S-GT	NV940	2GB	1.5V

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.6V* (1+(30.9/20))=1.527

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

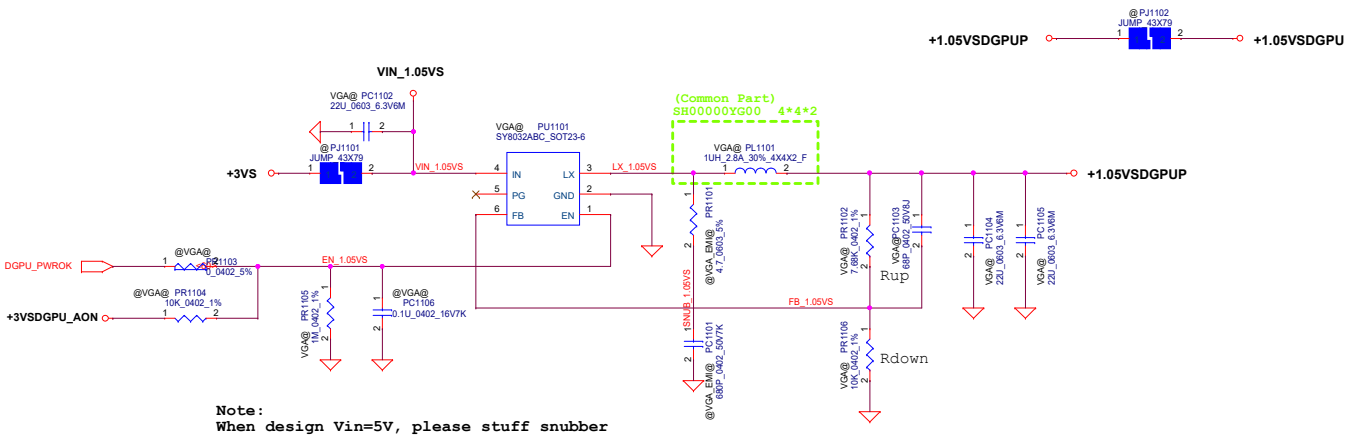
Title: 1.5VSDGPUP

Size: A3 | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

Date: Thursday, December 15, 2016 | Sheet 58 of 64

Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)

Imax= 0.77A, Ipeak= 1.1A , Iocp=3.5A

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	C4PB1/C5PB1 LA-E591P	1.0

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PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

unmount PRV5 for 2 phase select

2015/06/10 PR1215 change to 332K ohm
FSW= 450K Hz

N16S-GT EDP continuous:26A peak: 51A
L side Rds(on): 2.7mohm(Typ), 3.3mohm(Max)
Idsm: 70A@Ta=25C, 40A@Ta=70C

CHOKE:0.22uH, DCR 0.98m ohm, L/2 over 65A

FSW = 450Khz
(R=332K-->450Khz)
Imax=35A
Ipeak=51A
OCP = 63A
OVP=1.9(min), 2.1mohm(Max)

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR1209 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

N16S-GT
N16V-GM

Near GPU Core

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: NVIDIA VGA_CORE

Size	Document Number	Rev
C	C4PB1/C5PB1 LA-E591P	1.0

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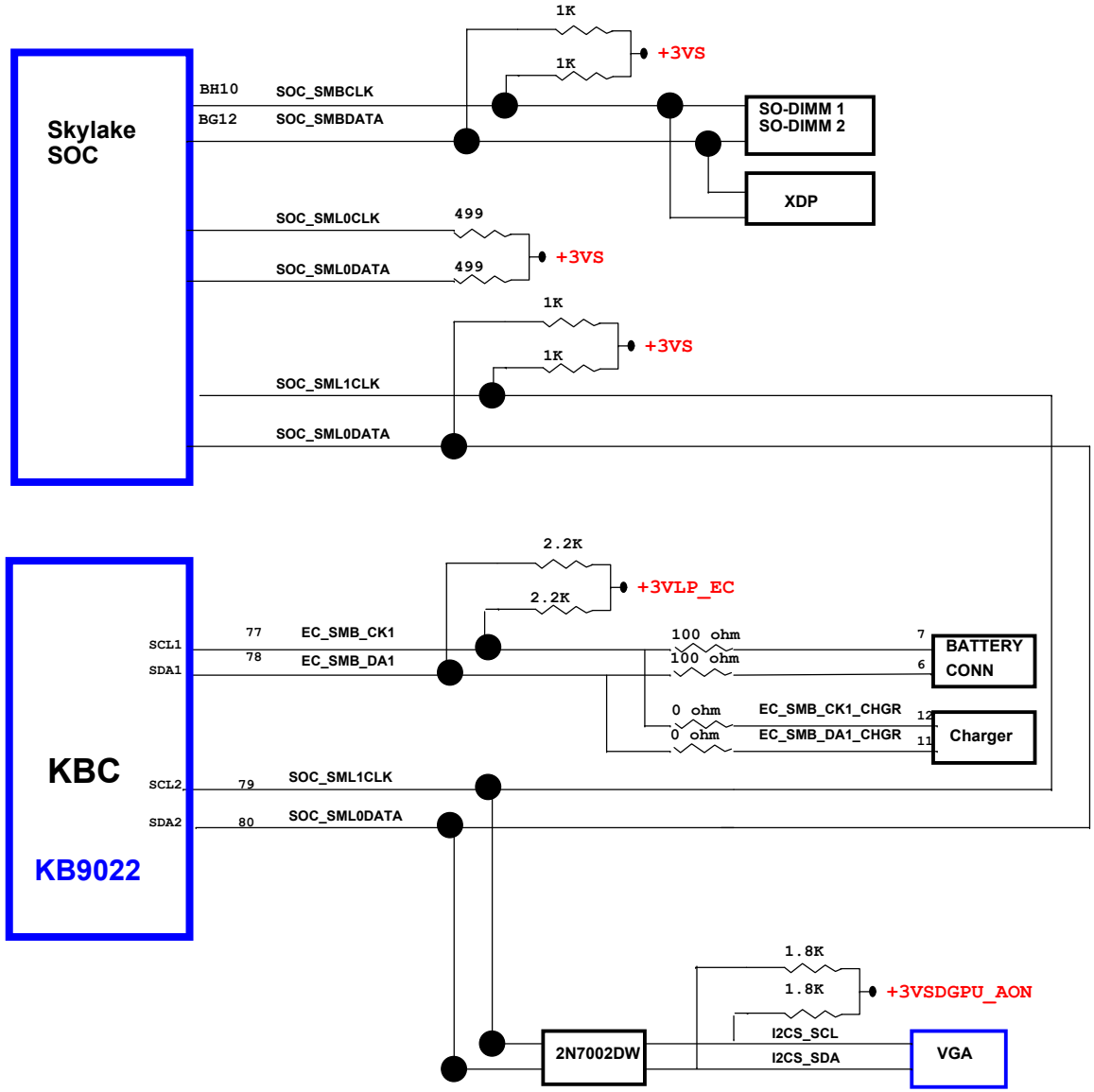

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SMBUS Routing Table

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01 02 03 04	Design Change.	ON FAE suggest to modify Parts for Kaby lake CPU setting	02	55	PC818 change to 33 pF. PC834 Change to 8200pF PC820 Change to 0.033 uF PR857 Change to 73.2K ohm PR836 Change to 61.9K ohm	9/21	PVT
05 06 07	Design Change.	For material issue, Changer main source part	02	56 48	PC9004,PC9079 change to SF000007700 (33 uF). PL9006 change to SH00000PK00 (0.47uH). PD101, PD102 change to SCS00005X00.	9/30	PVT
08							
09							
10							
11							
12							
13							
14							
14							

Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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BAD40 ->P6

0721
1. Modify RAM Flag for New on Onboard RAM, need to create new x76 level
2. Add NET DDR_A_BG1 for DDR4 DDP .
3. Add RU178, RU179 for NET DDR_A_BG1 to select SDP or DDP
4. DDR_A_BG1_R Connect to +0.6VS_VTT with PR24.2
5. RC38 adds new value 121_0402_1 for DDP.
6. ON Board RAM(U2~U5) PIN T7 Connect to GND for DDP.
7. Add RU174~RU177 to select SDP or DDP
8. Remove SAMSUNG 4G SA00008Z000 RAM
9. R625, R626 change to POP
10. USE JNGFF1.56 for Debug Signal "E51TXD_P80DATA"
11. IO Board power change to +3VALW
12. U5004's 3V power changes to +3VALW
13.Board ID changes to 0ohm for EVT
14.Add JUMP J38 for 3VALW output of U5009
15. add +3VALW discharge circuit, use Q2021
16. Change short pad to 0ohm
RL1,RL5,RL6,RL8,RL13,RC19,RC20,RD45,RD46,RD47,RC77,RC114,RC140,RC141,
RC143,RC154,RC156,RC161,RC162,RC163,RC167,RC168,RC169,RC171,RC172,
RC173,RC175,RC186,RC187,RC188,RC197,RC198,RC208,RC238,RC245,R407,R440,
R441,R442,R546,R550,R664,R666,R872,R873,R926,R927,R2023,R4936,R4938,
R4951,R4953,R4956,R5193,R5209,R5210,R5235,RC12,RC148,RC149,RC152,RC164,
RC176,RC190,RC192,RC209,RC229,R514,R645,R1580

0725
1. Use single RES RU180 to connect between DDR_A_BG1_R and +0.6VS_VTT instead of RP24
2. add new ciruit Q2022 for 3VALW's discharge, Q2021 is still keeps for 3VS

0725a
1. add new signal EC_PD_HRESET between EC and PD, and two RES R5262, R5263
2. Remove JP38

0729
1. Change R486, R487 to SM010009U00

0801
1. Delet net RP24.7

0802
1. Add C5252, C5253 for ESD

PVT
0919
1. Change below item to 0 ohm
R1580,R2023,R407,R440,R441,R442,R4936,R4938,R4951,R4953,R4956,R514,R5193,R5209,R5210,
R5235,R546,R550,R645,R664,R666,R872,R873,R926,R927,RC114,RC12,RC140,RC141,RC143,RC148,
RC149,RC152,RC154,RC156,RC161,RC162,RC163,RC164,RC167,RC168,RC169,RC171,RC172,RC173,
RC175,RC176,RC186,RC187,RC188,RC19,RC190,RC192,RC197,RC198,RC20,RC208,RC209,RC229,RC238,
RC245,RC77,RD45,RD46,RD47,RL1,RL13,RL5,RL6,RL8,

0921
1. RTD3_CIO_PWR_EN_R and RTD3_USB_PWR_EN_R Pull High from +3VS_TBT to +3.3V_TBT_SX
2. PD_IRQ#Pull High from 3VS to 3VALW
3. Add RC251 and RC252 for YC1 part
4. Chage RC148 RC198 to Bead
5. Change R5140 from 100K to 10K
6. Change R5150 and R5151 from 100K to 1M
7. Change Q2019 and Q2020 control single from 3VS to 3VS_TBT
8. Add D2013 for +HDMI_5V_OUT
9. Change C2536 and C2537 from @ to POP
10.add CC110 and CC118 for Intel's suggestion

0922
1. Change RTD3_CIO_PWR_EN_R and RTD3_USB_PWR_EN_R default setting from high to low
2. Change R5135 BOM Structure from TBT@ to @

0922a
1. Change R5170.1 power plan from +3.3V_TBT_SX to +3.3V_FLASH

0929
1. Change Board ID to 12K
2. Change C5108, C5109 from 20P to 12P

0929a
1. Update Power Schematic

1006
1. change YC2 to SJ10000PW00
2. add X76713BOL04 for NEW Hynix E-die VRAM
3. change U5004 part number to SA00009YL70

1007
1. Change R1580 to JUMP for 5V 3A for satisfaction
2. Import PWR 1007a Schematic

PreMP
1216
1.change R5196 to TBT@ and R5204 to @
2.change value of R5260 to 470ohm
3.change the Gate Input of Q2019 Q2020 from +3VS_TBT to +3VS
4.Board ID R4903 change to 15K

1226
1. add R5266, R5267 and pull down to GND

Security Classification	Compal Secret Data		
Issued Date	2016/07/29	Deciphered Date	2016/07/29

Compal Electronics, Inc.

Title: HW PIR

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DDR4 On Board RAM

X76713BOL03 Hynix

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U2
X76OBHY@

10K +-5% 0402
SD028100280
RU173
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U3
X76OBHY@

10K +-5% 0402
SD028100280
RU169
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U4
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U5
X76OBHY@

X76713BOL01 micron 4G

D4 512M16 MT40A512M16JY
SA00009V220
U2
X76OBMACRON4@

10K +-5% 0402
SD028100280
RU170
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U3
X76OBMACRON4@

10K +-5% 0402
SD028100280
RU172
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U4
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U5
X76OBMACRON4@

X76713BOL02 micron 8G

D4 16G MT40A1G16WBU
SA0000A3120
U2
X76OBMACRON8@

10K +-5% 0402
SD028100280
RU169
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U3
X76OBMACRON8@

10K +-5% 0402
SD028100280
RU170
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U4
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U5
X76OBMACRON8@

VRAM

X76614BOL54 Hynix

D3 256M16 H5TC4G63CFR
SA00008DN10
U2004
X76VHY@

30K +-1% 0402
SD034300280
R2044
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2005
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2006
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2007
X76VHY@

X76614BOL58 SANSUNG

D3 256M16 K4W4G1646E
SA000076PB0
U2004
X76VSAM@

24.9K +-1% 0402
SD034249280
R2044
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2005
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2006
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2007
X76VSAM@

X76713BOL04 Hynix E-die

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2004
X76VHY_E@

10K_0402_1%
SD034100280
R2035
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2005
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2006
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2007
X76VHY_E@

SATA Redriver

X76525BOL51 TI

SN75LVCP601RTJR
SA00003ZX00
U1
X76SATATI@

4.99K +-1% 0402
SD034499180
R11
X76SATATI@

need to update

X76525BOLXX Parade

PS8527CTQFN20GTR2-A2
SA00007JU10
U1
X76SATAPAR@

4.7K +-5% 0402
SD028470180
R18
X76SATAPAR@

7.5K +-5% 0402
SD028100280
R11
X76SATAPAR@

X76525BOL52 Parade

PS8527CTQFN20GTR2-A1
SA00007JU00
U1
X76SATAPARa@

4.7K +-5% 0402
SD028470180
R18
X76SATAPARa@

7.5K +-5% 0402
SD028100280
R11
X76SATAPARa@

X4EA5TBOL01 includes EMC@, EMI@ and ESD@

ZZZ

SMT EMC EE AE591 C4PB1
X4E@EMC
X4EA5TBOL01

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