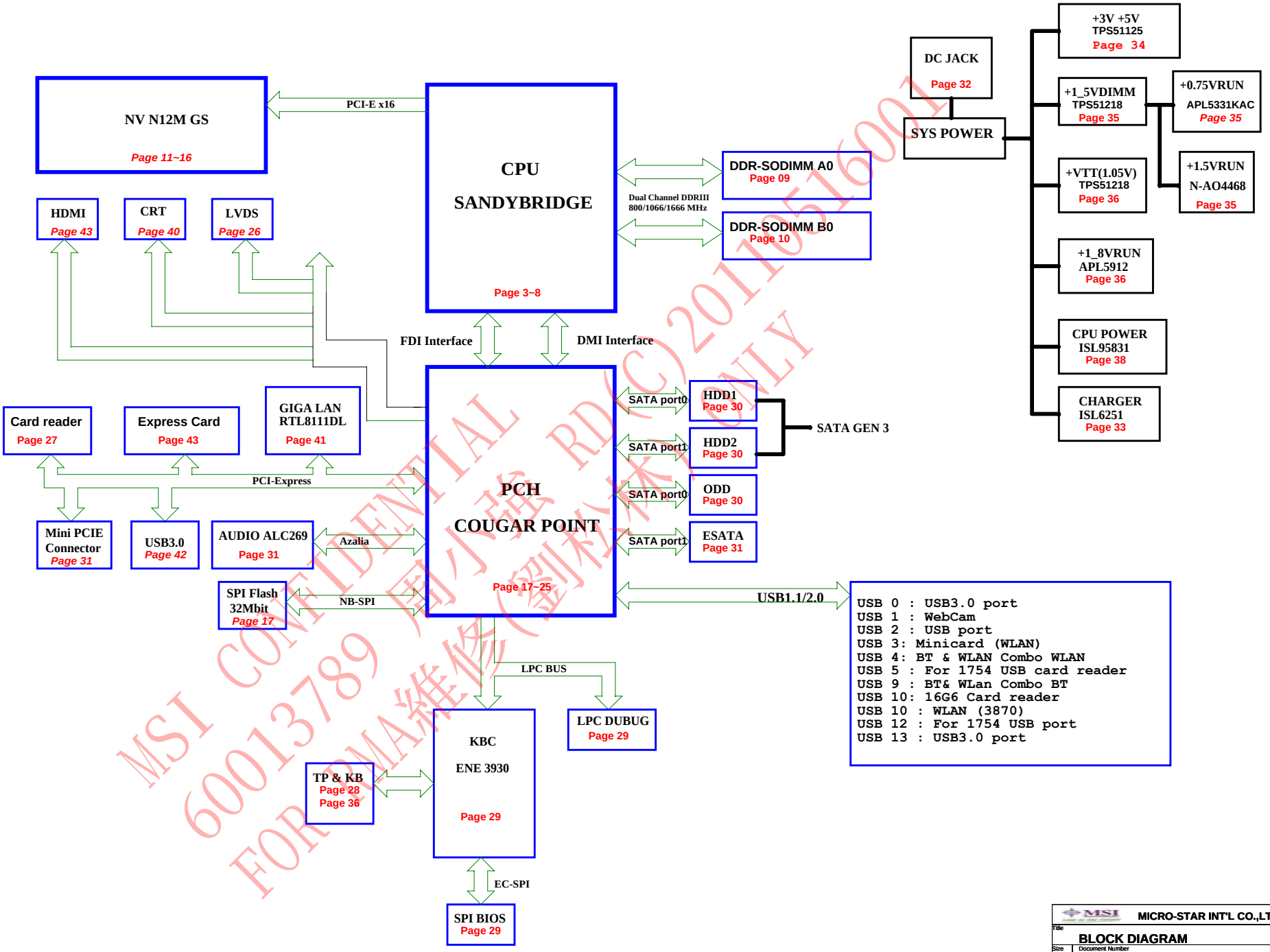
MS-1754 Ver : 10

Huron River Platform



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Title: BLOCK DIAGRAM

Size: Custom | Document Number: 16G9/1754 | Rev: 10

Date: Thursday, June 30, 2011 | Sheet 1 of 52

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

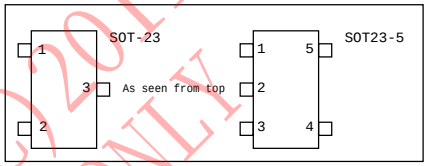
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



Power States

	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

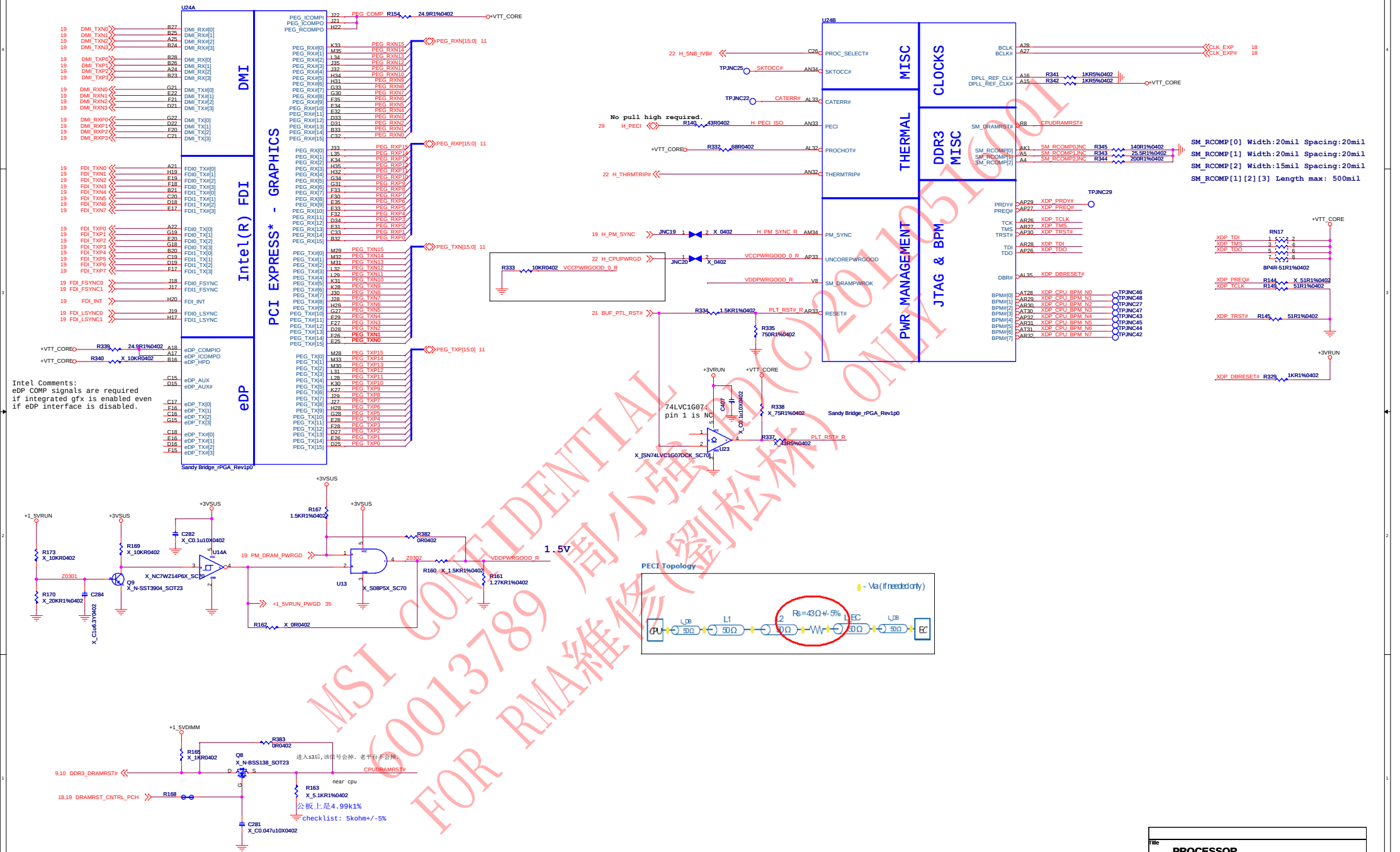
MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

Size: Custom | Document Number: MS-16G9/1754 | Rev: 10

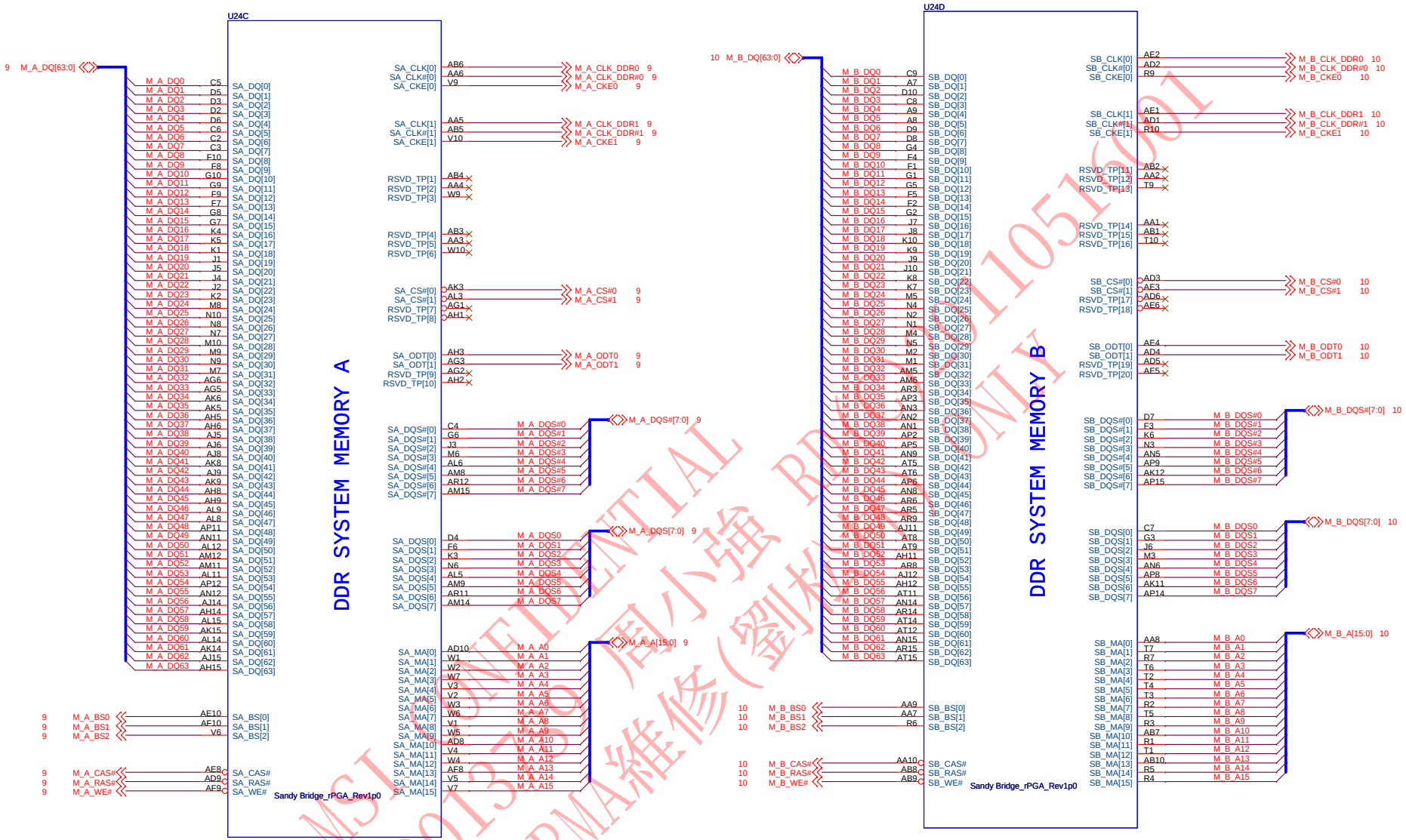
Date: Thursday, June 30, 2011 | Sheet 2 of 52

SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)



Title	PROCESSOR		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 3 of 52		

SANDYBRIDGE PROCESSOR (DDR3)



Title	DDR3		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 4 of 52		

SANDYBRIDGE PROCESSOR (POWER)

	148X schematic	CRB
+VCC_CORE	10UFx10 22UFx16 330UFx6	10UFx10 22UFx16 470UFx4
+VTT_CORE	10UFx7 22UFx5 330UFx2	22UFx29 330UFx2

Vcc for Processor core 0.3-1.1V

Iccmax: SV-QC 94A;
Iccmax: SV-DC 53A;

Icc_TDC: SV-DC 55A;
Icc_TDC: SV-DC 38A;

POWER

U24F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

Sandy Bridge_rPGA_Rev1p0

+VCC_CORE

+VTT_CORE

Spec is 8.5A

1.05V

JNC10

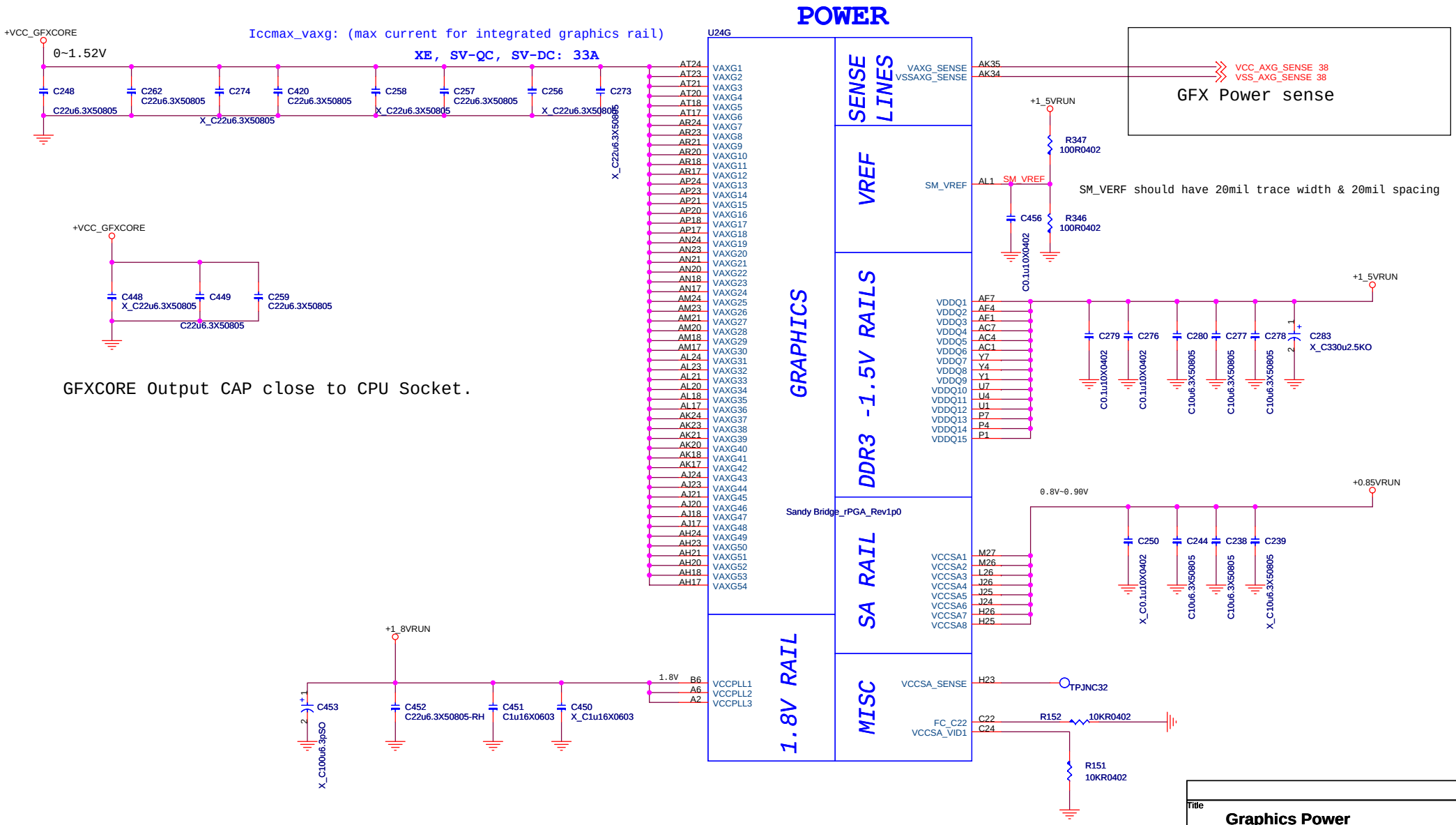
X_0402

Close to CPU

Close to IMVP7

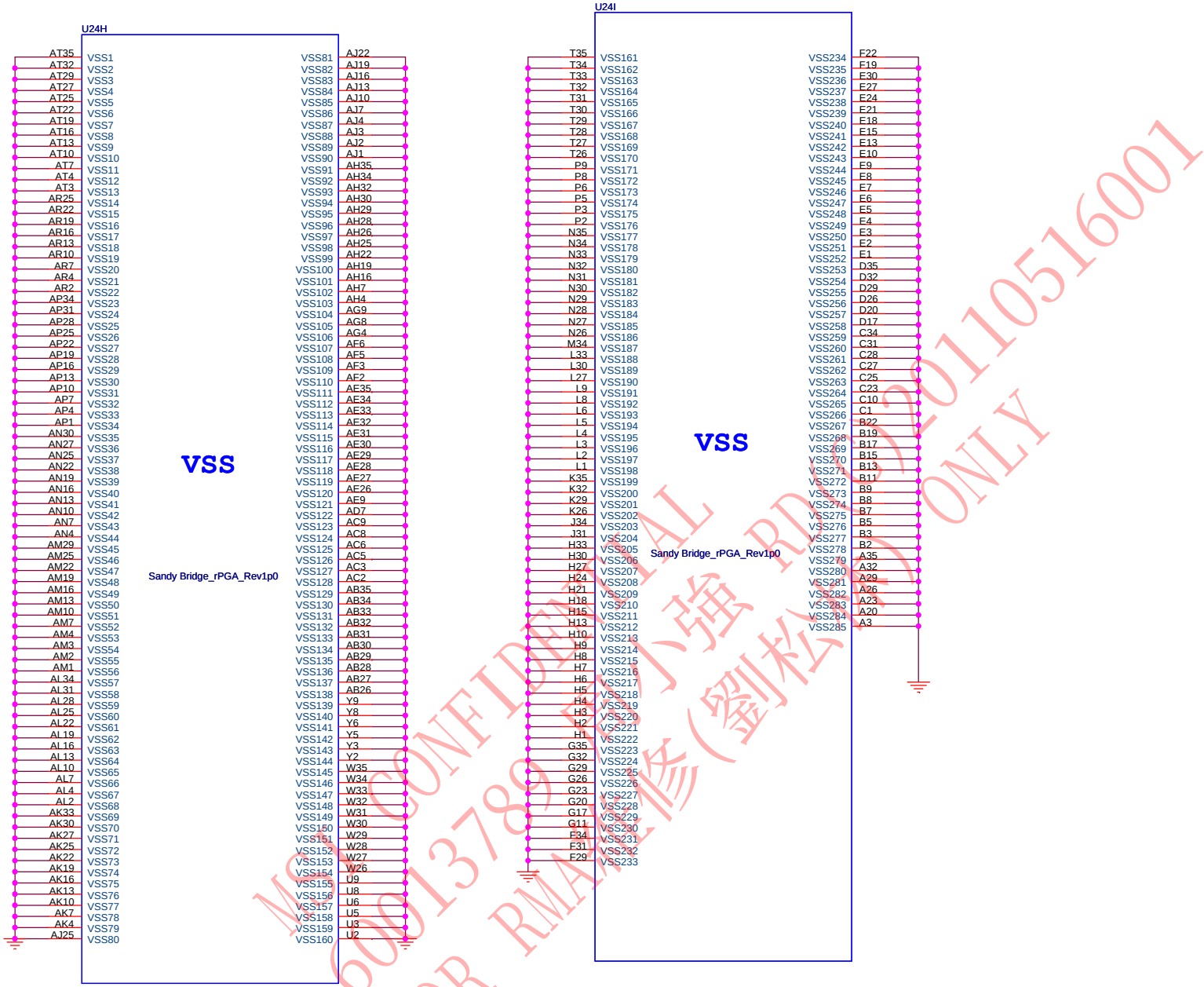
Title	PROCESSOR POWER
Size	Custom
Document Number	MS-16G9/1754
Rev	10
Date:	Thursday, June 30, 2011
Sheet	5 of 52

SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



Title	Graphics Power		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 6 of 52		

SANDYBRIDGE PROCESSOR (GND)



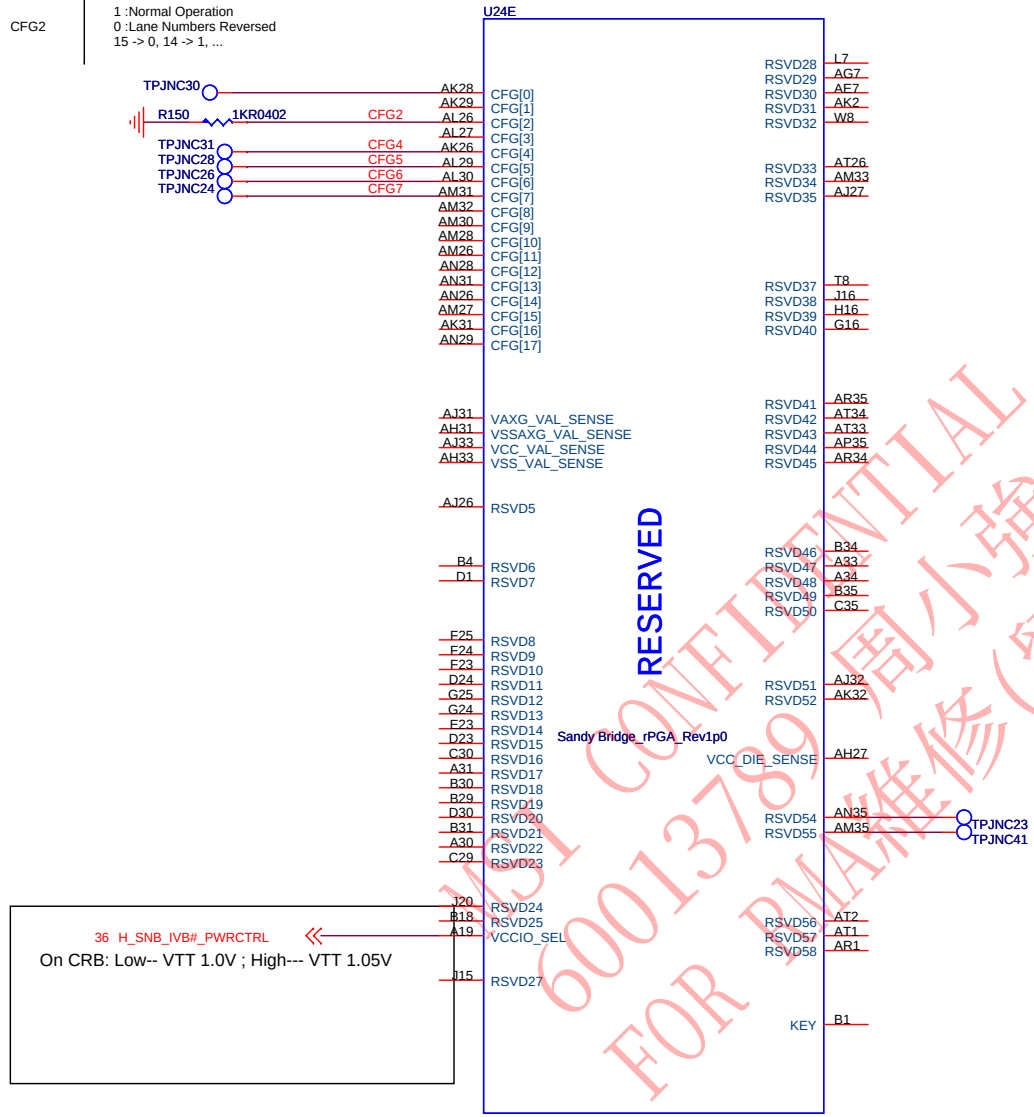
Title	PROCESSOR GND		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 7 of 52		

SANDYBRIDGE PROCESSOR (RESERVED)

The CFG signals have a default value of "1" if not terminated on the board.

CFG2- PCI-Express Static Lane Reversal

CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

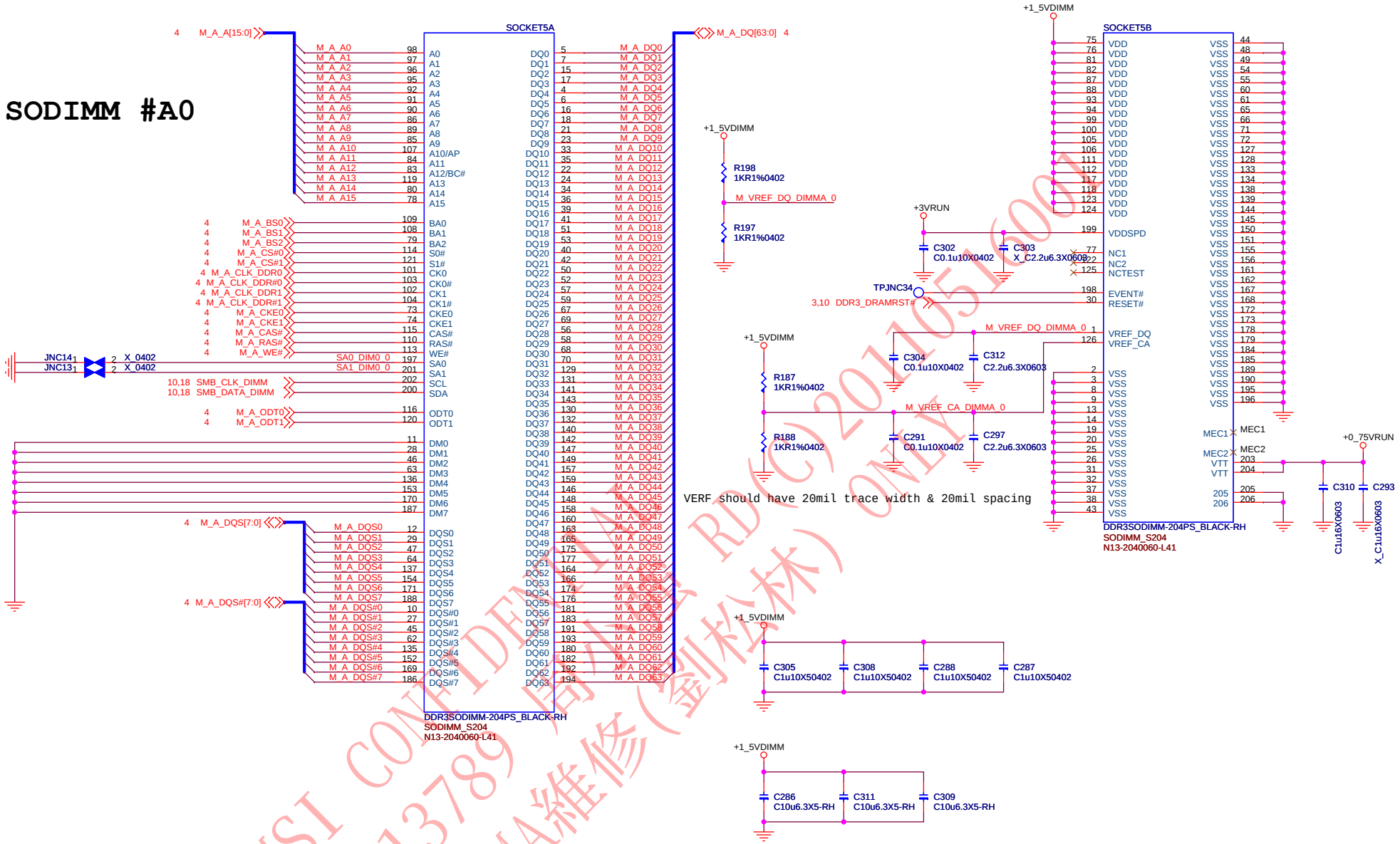
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

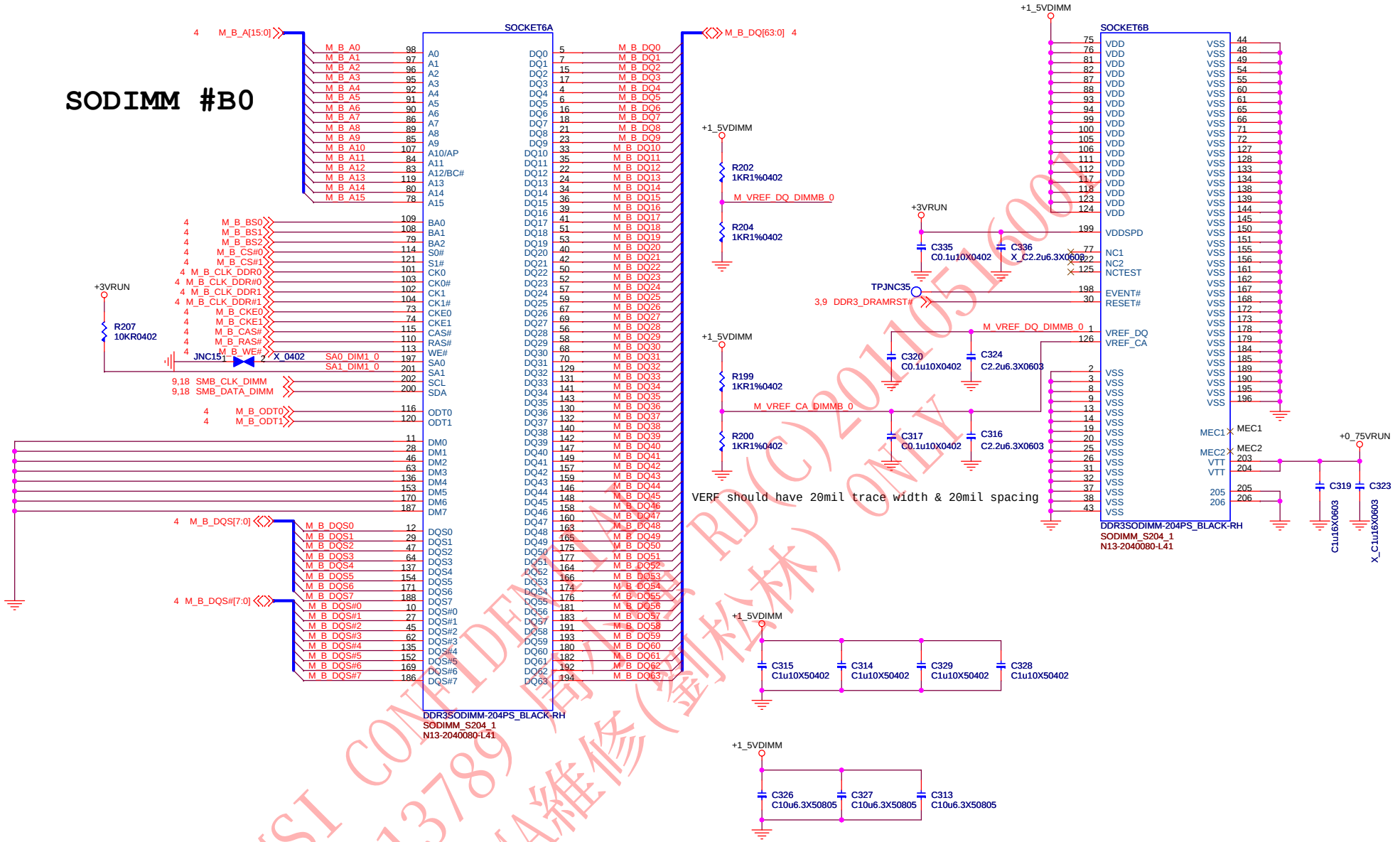
PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

DATASHEET记录	
CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

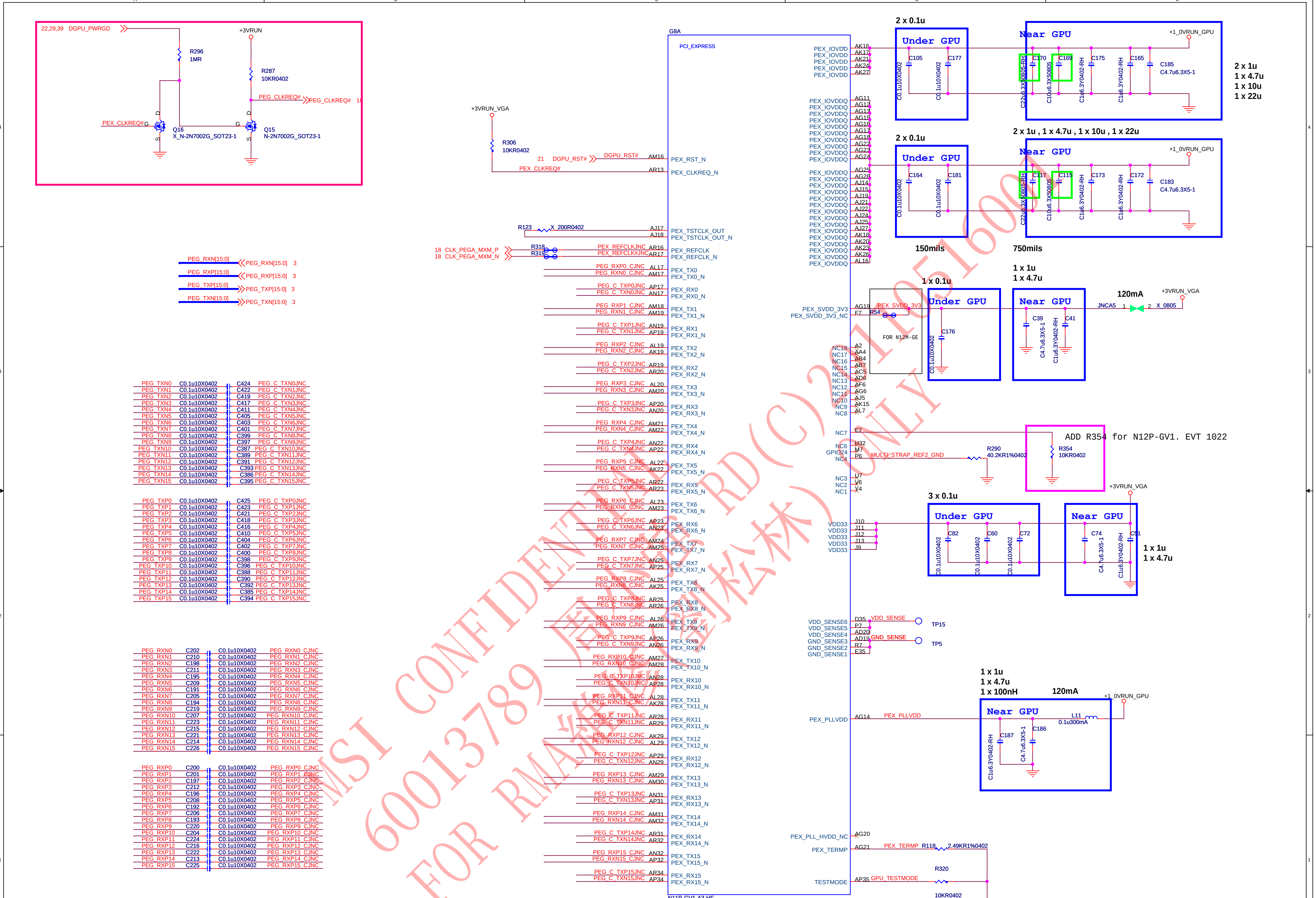
Title: PROCESSOR RESERVED			
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 8 of 52		



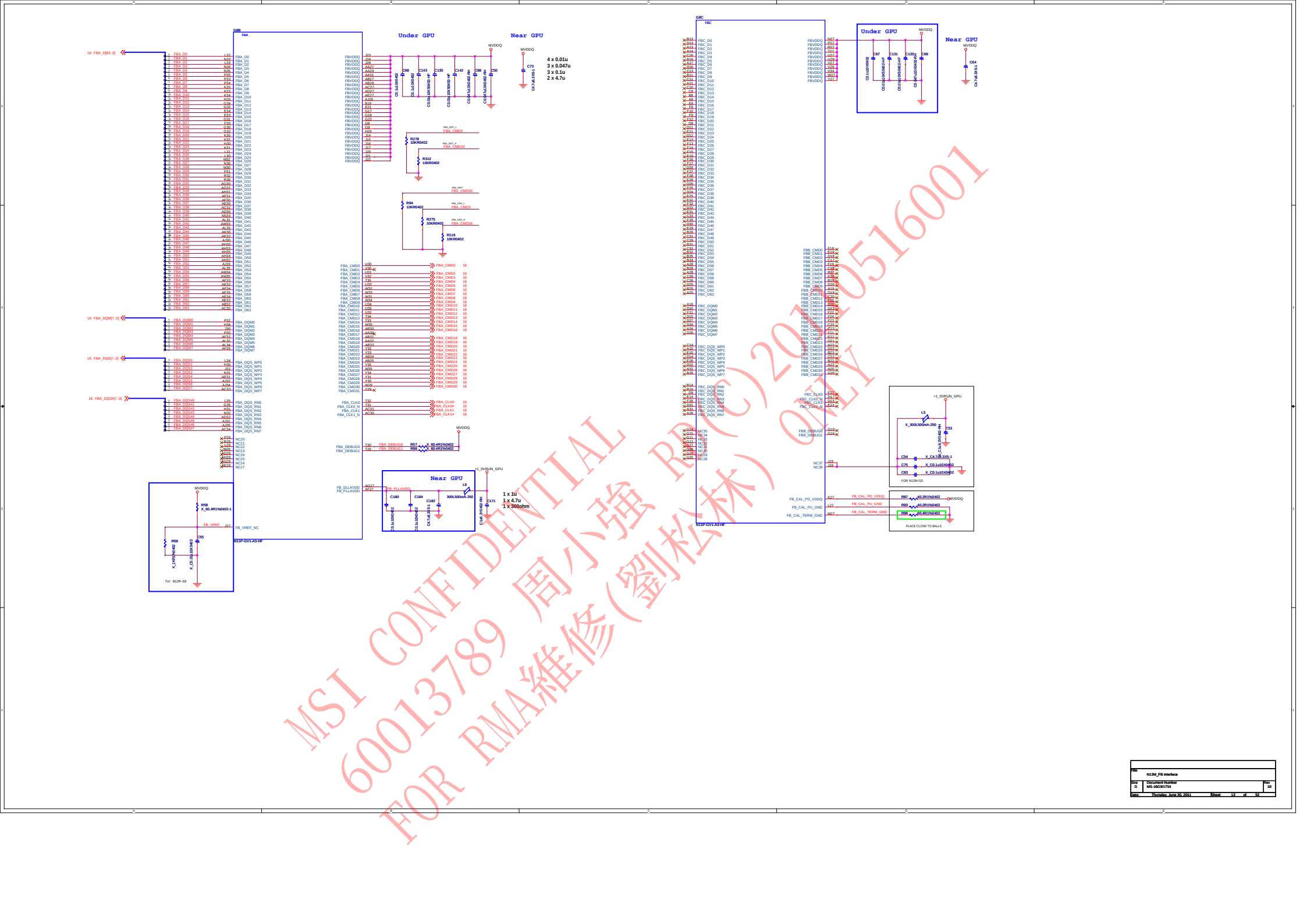
Title	DDR3 SODIMM A0	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 9 of 52	



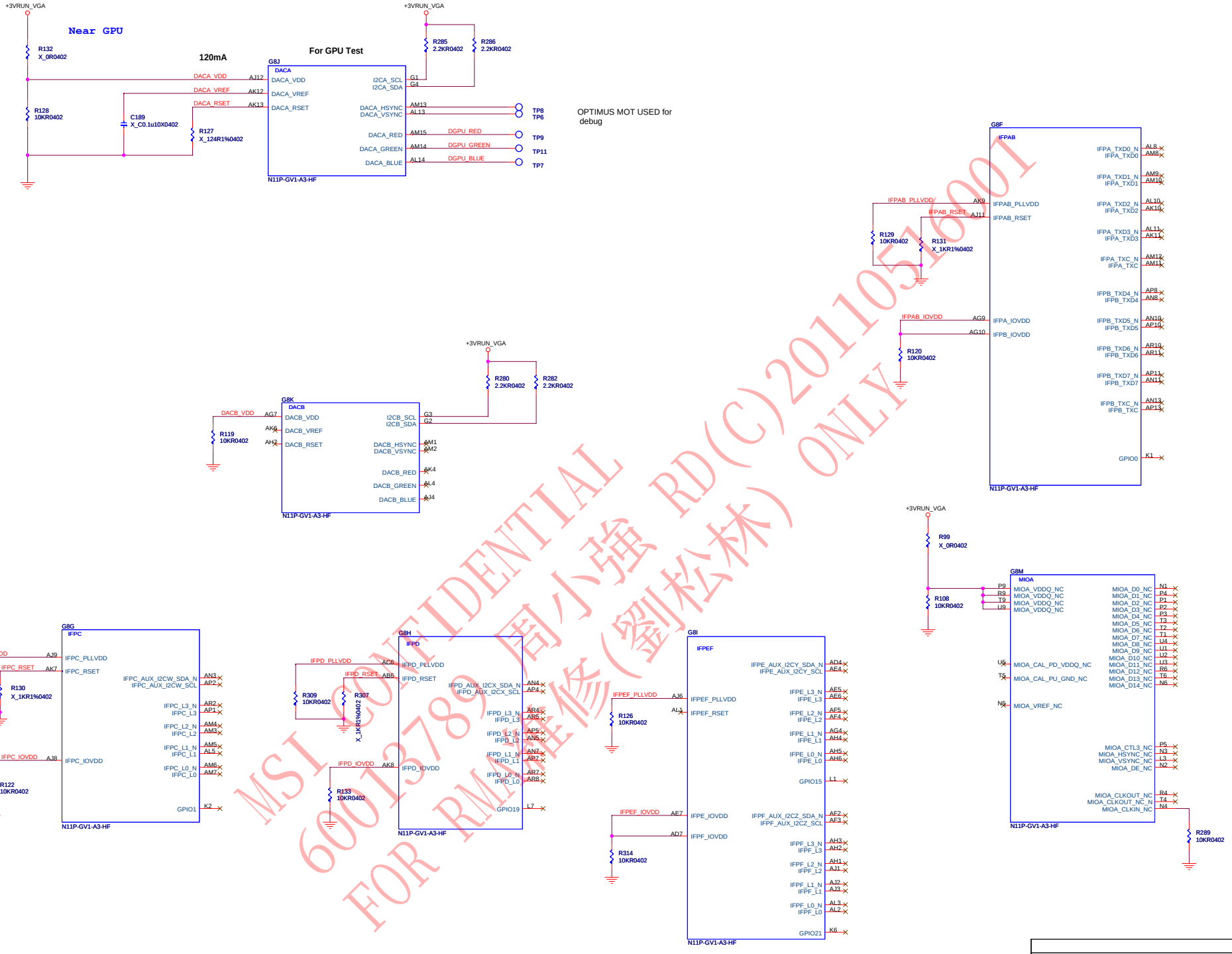
Title	DDR3 SODIMM B0	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 10 of 52	



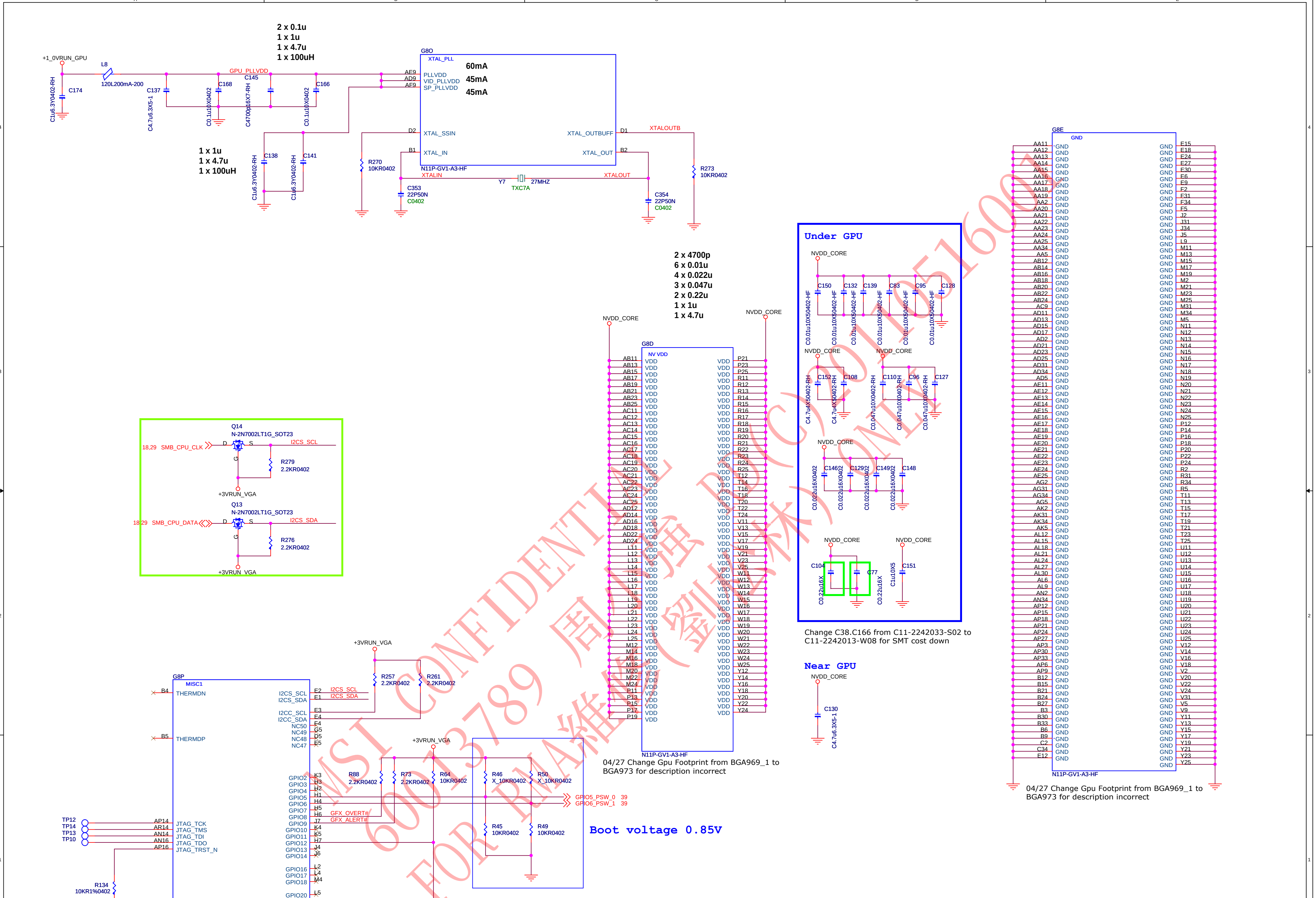
Title	N12M_PCIE		
Size C	Document Number MS-16G9/1754		Rev 10
Date: Thursday, June 30, 2011		Sheet 11 of 52	



Title	N12M_FB interface
Size	D
Document Number	MS-16G1G754
Rev	1B
Date	Thursday, June 30, 2011
Sheet	12 of 52



Title	N12M_CRT/LVDS?HDMI	
Size C	Document Number MS-16G9/1754	Rev 10
Date: Thursday, June 30, 2011	Sheet 13 of 52	



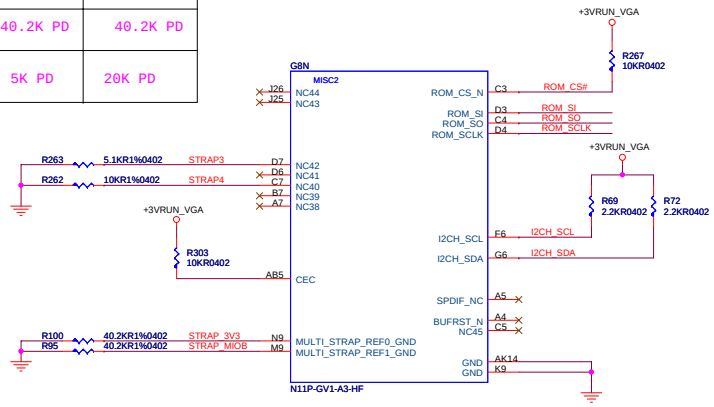
MICRO-STAR INT'L CO.,LTD.

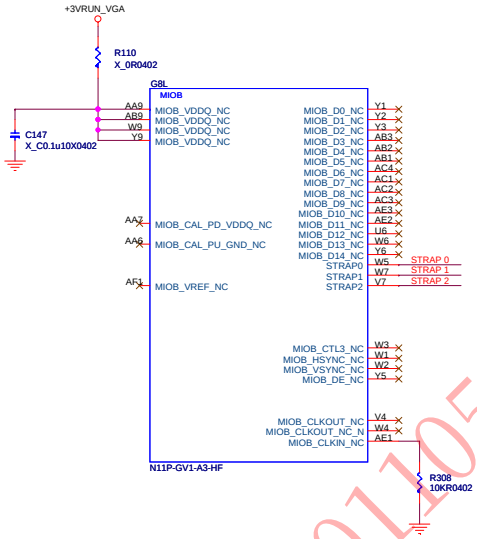
Title: N12M_GPIO/POWER

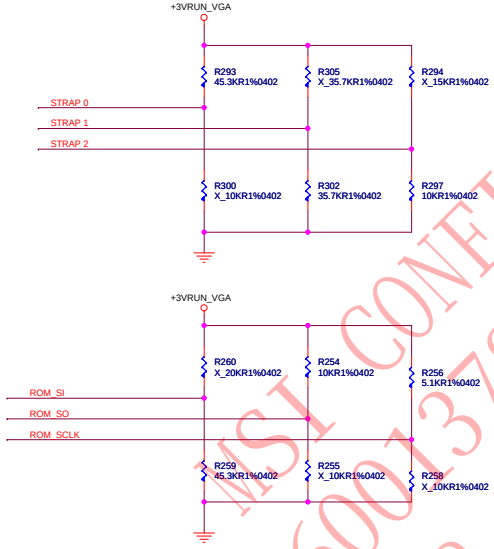
Size	Document Number	Rev
C	MS-16G9/1754	10

Date: Thursday, June 30, 2011 Sheet 14 of 52

	Strap3	Strap4
N12M-GS1	40.2K PD	40.2K PD
N12P-GV1/GVR	5K PD	20K PD







N12M

STRAP0 PU 45K	USER 3	1
	USER 2	1
	USER 1	1
	USER 0	1
STRAP1 PD 35K	3GIO_PADCFG 3	0
	3GIO_PADCFG 2	1
	3GIO_PADCFG 1	1
	3GIO_PADCFG 0	0
STRAP2	PCI_DEVID3	0
	PCI_DEVID2	1
	PCI_DEVID1	0
	PCI_DEVID0	0/1
ROM_SCLK PU 15K	PCI_DEVID 4	1
	SUBVENDOR	0
	SLOT_CLK	1
	PEX_PLL_EN	0
ROM_SI PD 35K	RAMCFG 3	0
	RAMCFG 2	1
	RAMCFG 1	1
	RAMCFG 0	1
ROM_SO PD 10K	XCLK_417	0
	FB_0_BAR_SIZE	0
	SMB_ALT_ADDR	0
	VGA_DEVICE	1

SM BUS define resolution 1111

N12M-GS:PD 35K,
N12M-GE:PU 35K
N12M-GS1:PD 35K
N12P-GV1: PD35K

N12M-GS:PD 25K,
N12M-GE:PU 15K
N12M-GS1: PU15K
N12P-GV1: PD45K
N12P-GVR: PD10K

N12M-GS:PU 15K,
N12M-GE:PU 15K,
N12M-GS1:PD 15K

Hynix 128Mx16---------- PD35K
Samsung 128Mx16------ PD45K

Have 27M hz CRYSTAL
FB Aperture size 256MB
0X9E(Default , not Multi-GPU usage)
VGA Device

Rvalue	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

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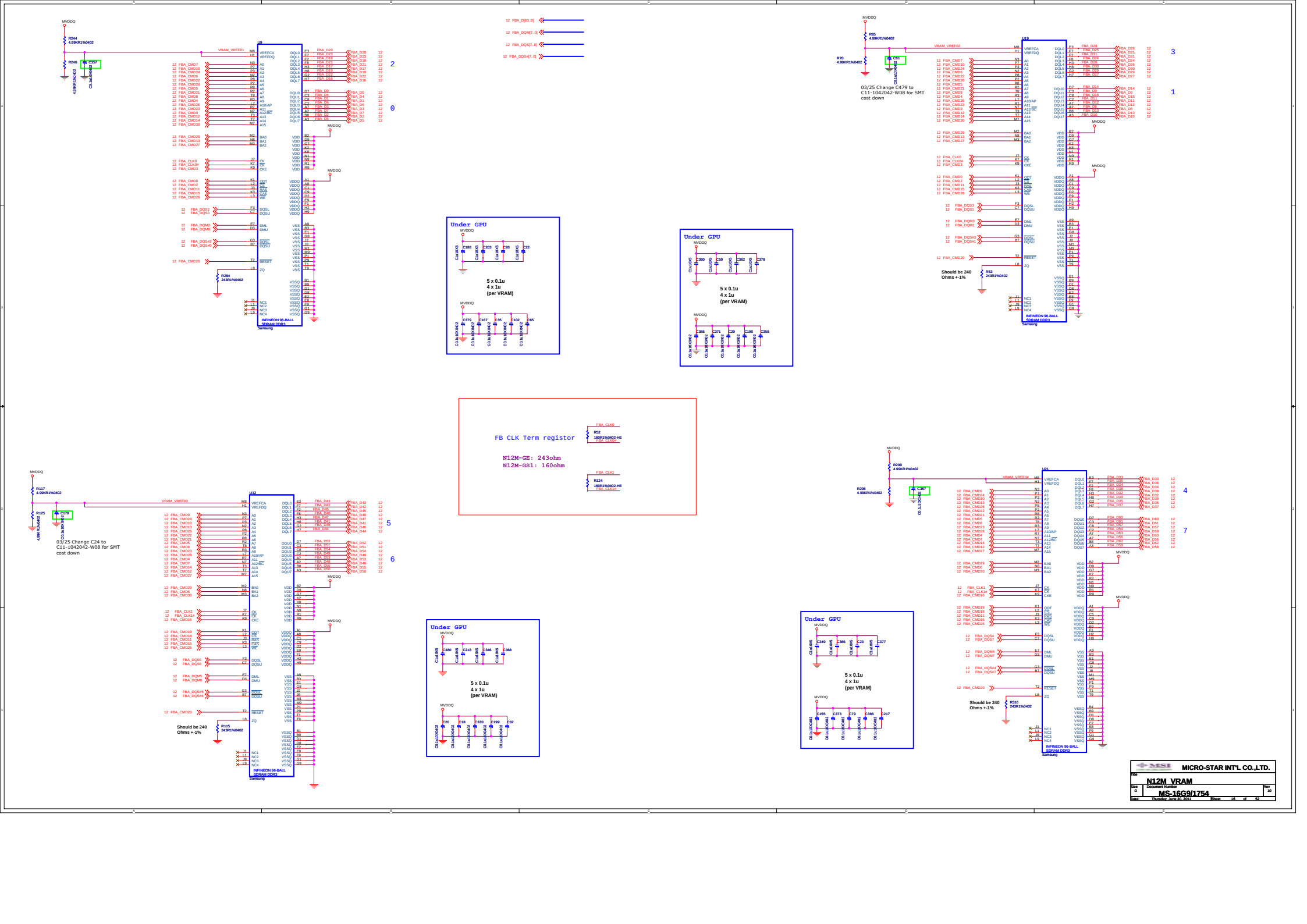
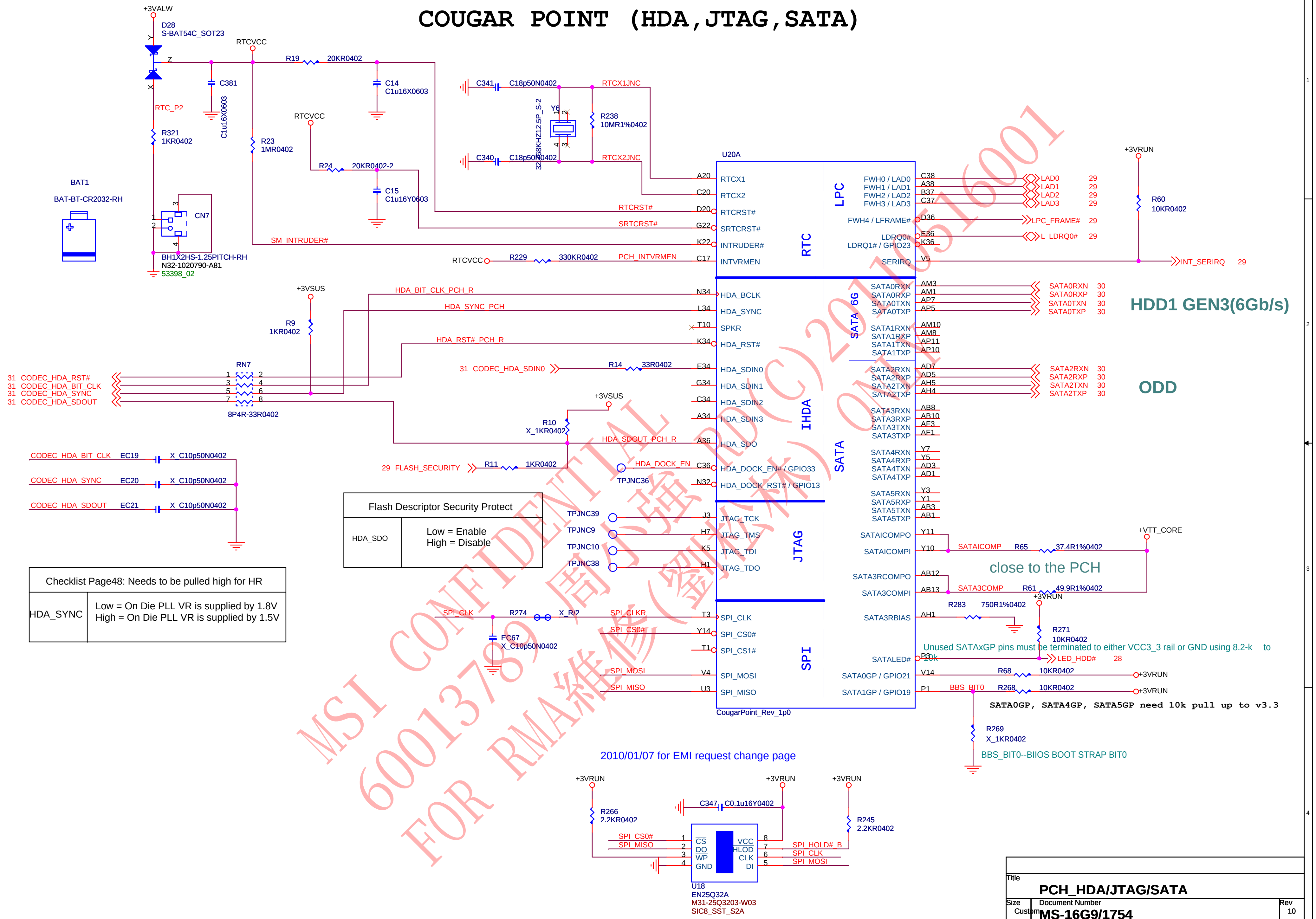
Title: N12M_STRAP

Size: C | Document Number: MS-16G9/1754 | Rev: 10

Date: Thursday, June 30, 2011 | Sheet 15 of 52

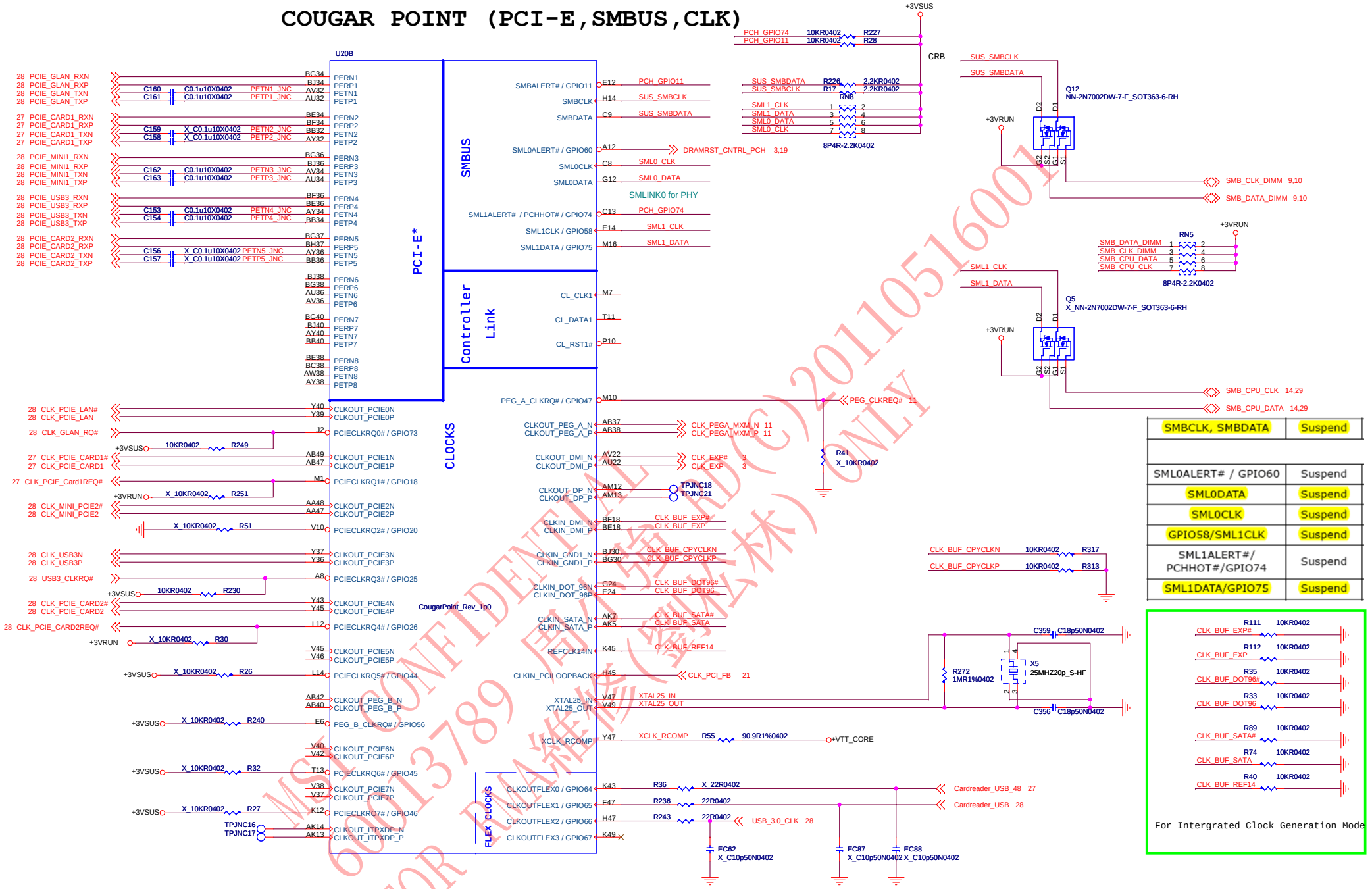

MVDDQ
R244 4.99KR1%0402
R246 4.99KR1%0402
R1 C357
CD.1U10V0402
VRAM_VREFD1
U9
VREFCA
VREFDQ
INFINEON 96-BALL SDRAM DDR3
Samsung
R284 243R1%0402
Under GPU
5 x 0.1u
4 x 1u
(per VRAM)
C188 C203 C93 C22
C360 C59 C362 C378
C379 C167 C35 C102 C85
C355 C371 C29 C190 C358
FB CLK Term registor
N12M-GE: 243ohm
N12M-GS1: 160ohm
FBA_CLK0
RS2 160R1%0402-HE
FBA_CLK0#
FBA_CLK1
R124 160R1%0402-HE
FBA_CLK1#
R117 4.99KR1%0402
R125 4.99KR1%0402
C179
VRAM_VREFD3
U12
03/25 Change C24 to C11-1042042-W08 for SMT cost down
R115 243R1%0402
Should be 240 Ohms +-1%
C380 C218 C346 C368
C20 C18 C370 C199 C32
R299 4.99KR1%0402
R298 4.99KR1%0402
C367
VRAM_VREFD4
U21
C349 C365 C23 C377
C155 C373 C79 C366 C217
R316 243R1%0402
R85 4.99KR1%0402
R70 4.99KR1%0402
C61
VRAM_VREFD2
U19
R53 243R1%0402
MICRO-STAR INT'L CO.,LTD.
N12M_VRAM
MS-16G9/1754
Size D
Rev 1.0
Date: Thursday, June 30, 2011
Sheet 16 of 52

COUGAR POINT (HDA,JTAG,SATA)



Title	PCH_HDA/JTAG/SATA	
Size Custom	Document Number MS-16G9/1754	Rev 10
Date: Thursday, June 30, 2011	Sheet 17 of 52	

COUGAR POINT (PCI-E,SMBUS,CLK)



SMBCLK, SMBDATA	Suspend
SML0ALERT# / GPIO60	Suspend
SML0DATA	Suspend
SML0CLK	Suspend
GPIO58/SML1CLK	Suspend
SML1ALERT#/ PCHHOT#/GPIO74	Suspend
SML1DATA/GPIO75	Suspend

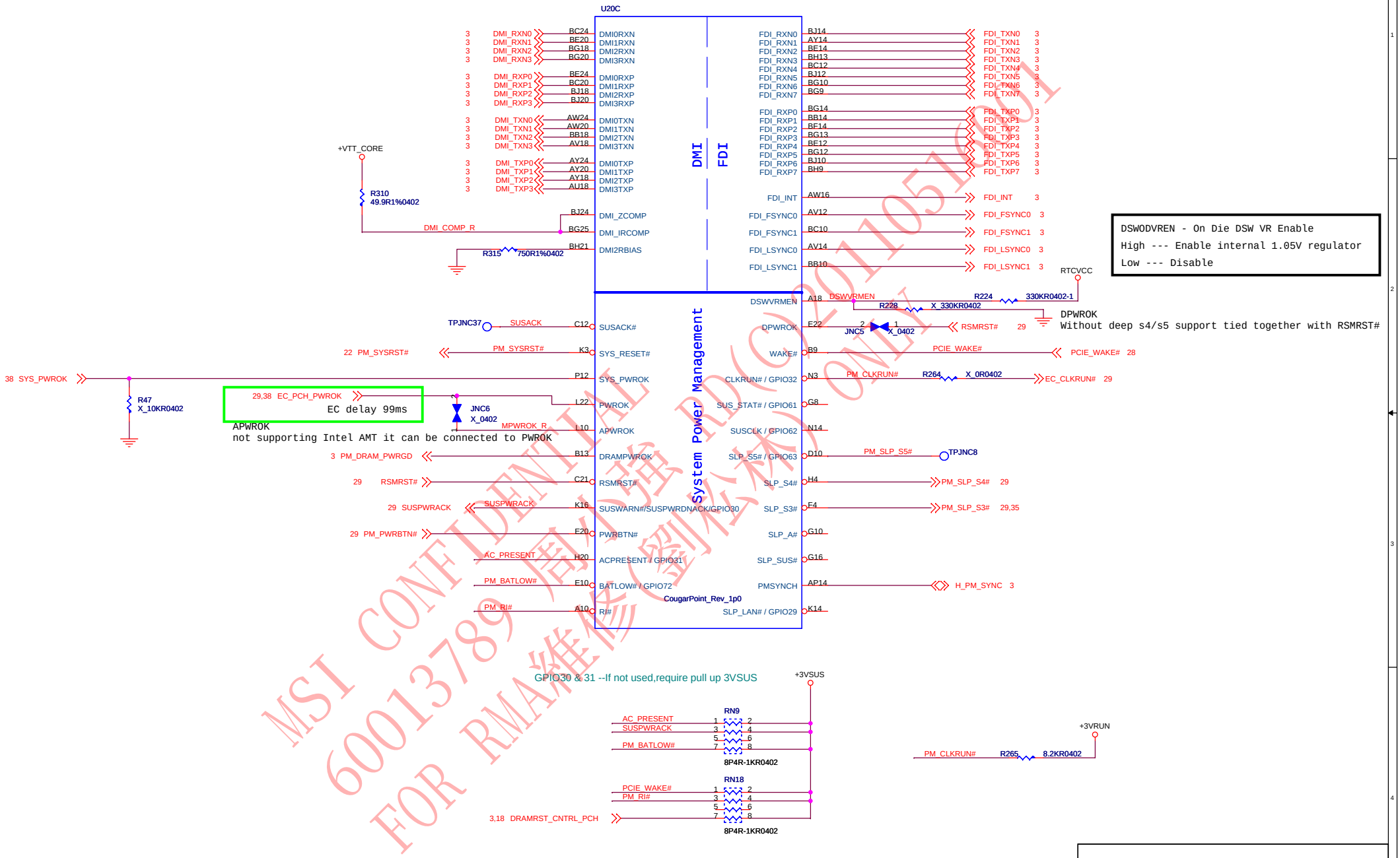
For Intergrated Clock Generation Mode

NOTE: If CLKREQ# control is not needed, say for a free running clock, do not pull-down signal to GND. This will increase leakage in Sx states. A 10 kOhms±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled via Intel? Management Engine (Intel? ME) FW. Please refer to Intel ME FW Bring Up Guide for configuring/disabling CLKREQ#.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

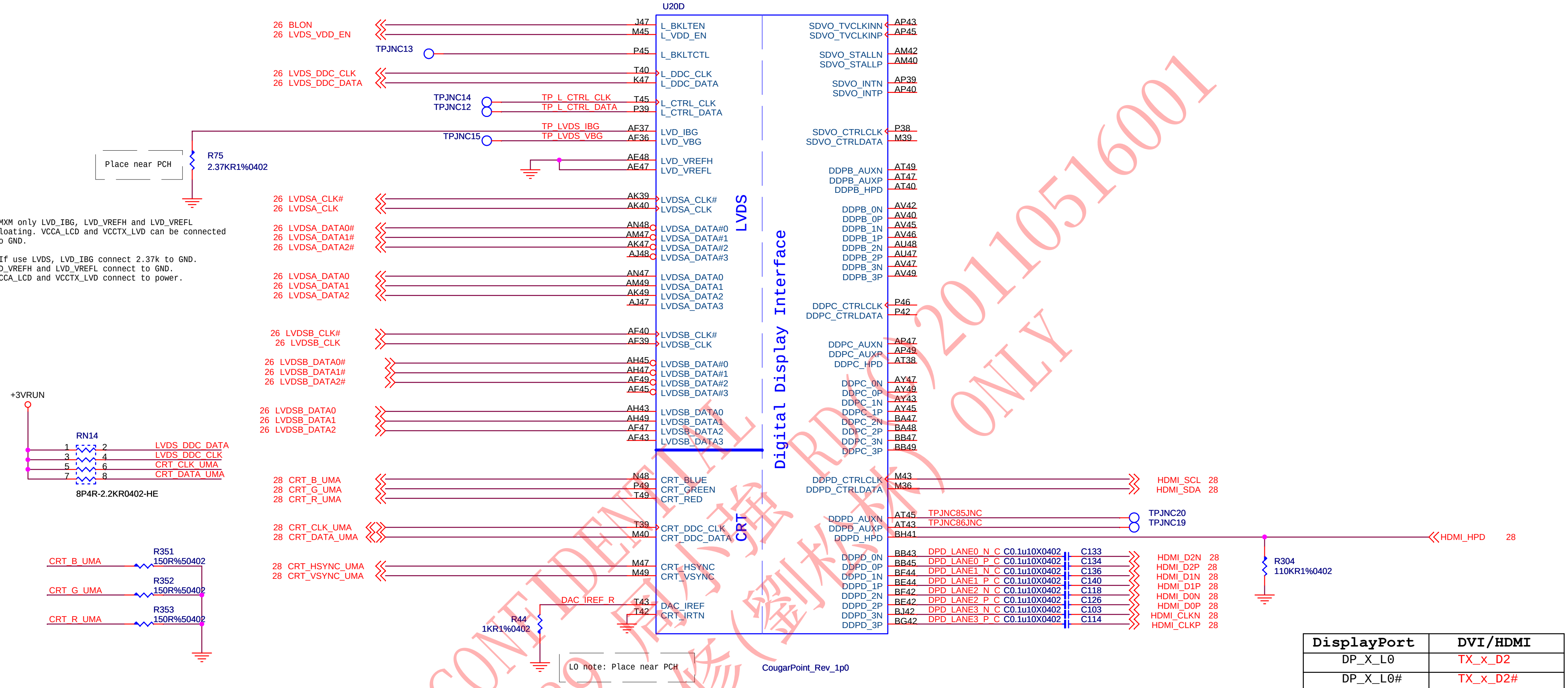
Title	PCH_PCIE/SMBUS/CLK		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 18 of 52		

COUGAR POINT (DMI,FDI,GPIO)



Title	PCH_DMI/FDI/GPIO		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 19 of 52		

COUGAR POINT (LVDS,DDI)

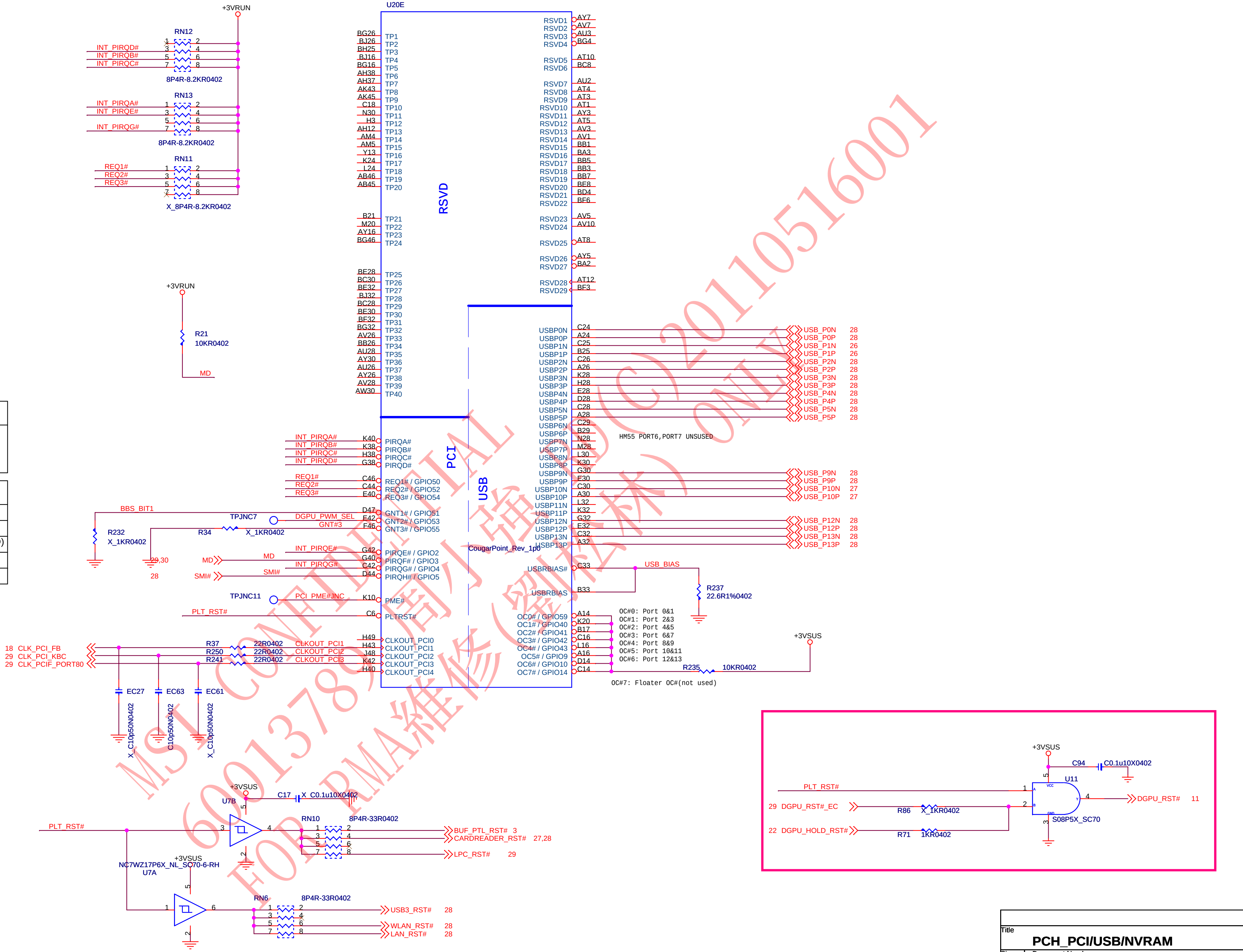


1.MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.

2.If use LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.

DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

COUGAR POINT (PCI,USB,NVRAM)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	_
1	1	SPI

Title: PCH_PCI/USB/NVRAM
Size: Custom | Document Number: MS-16G9/1754 | Rev: 10
Date: Thursday, June 30, 2011 | Sheet 21 of 52

COUGAR POINT (GPIO,VSS_NCTF,RSVD)

GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--High is support TLS,internal pull-down
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Un- Muxed. If not used Can be NC

GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled.

bios 设置gpio8 output high

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

GPIO36 --CRB connector to 3V

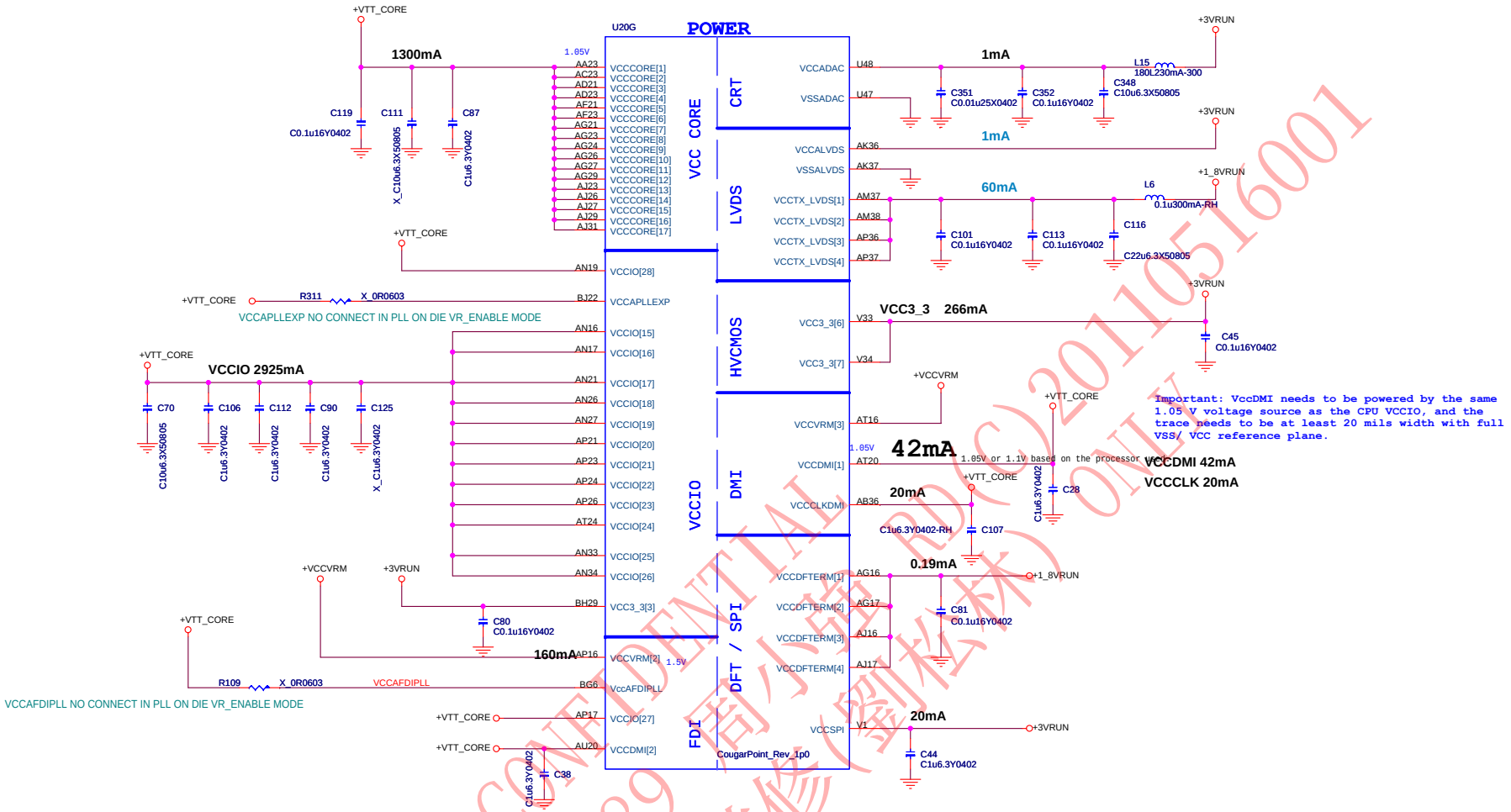
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX

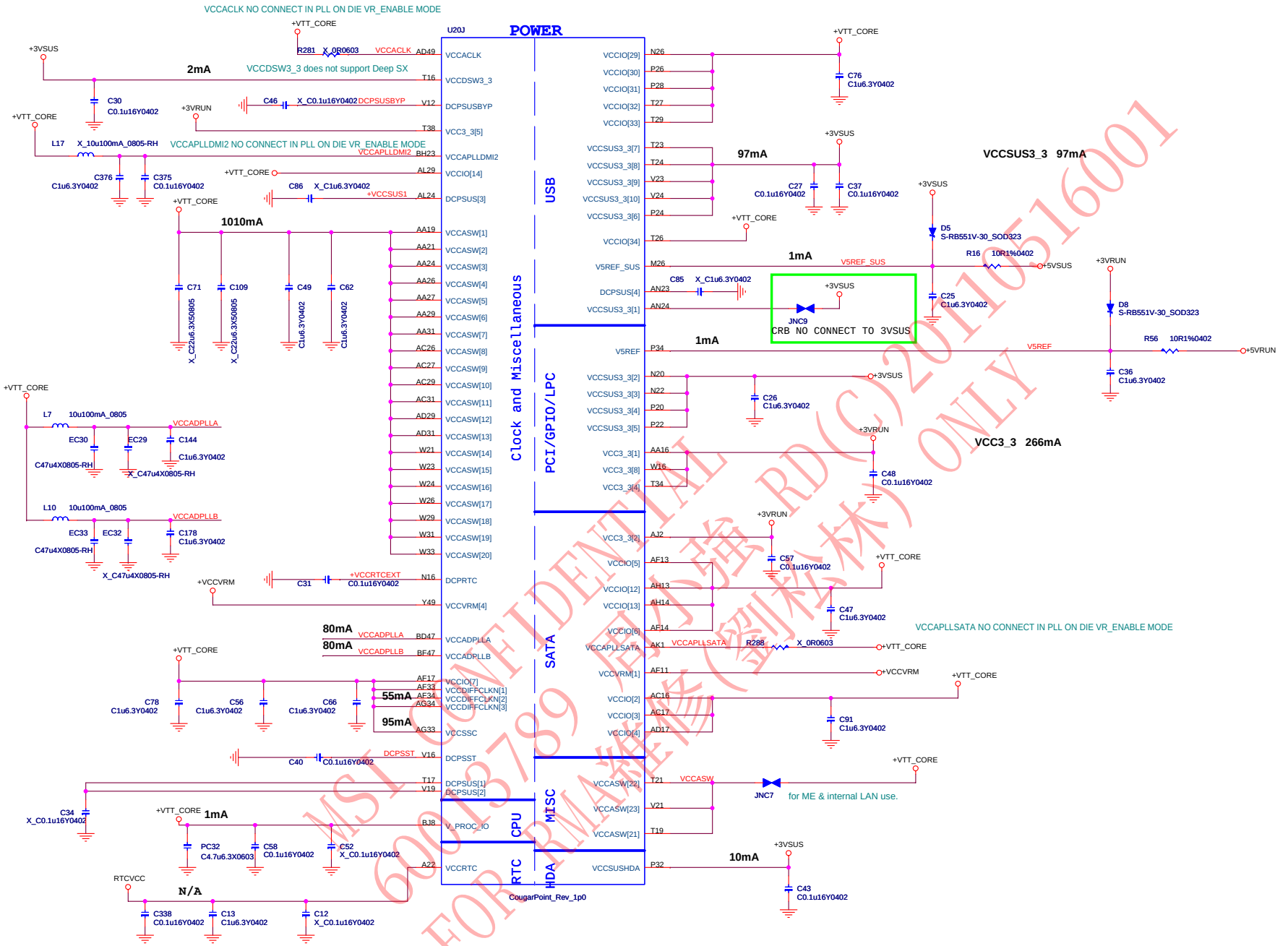
Title	PCH_GPIO/NCTF/RSVD	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 22 of 52	

COUGAR POINT (POWER)



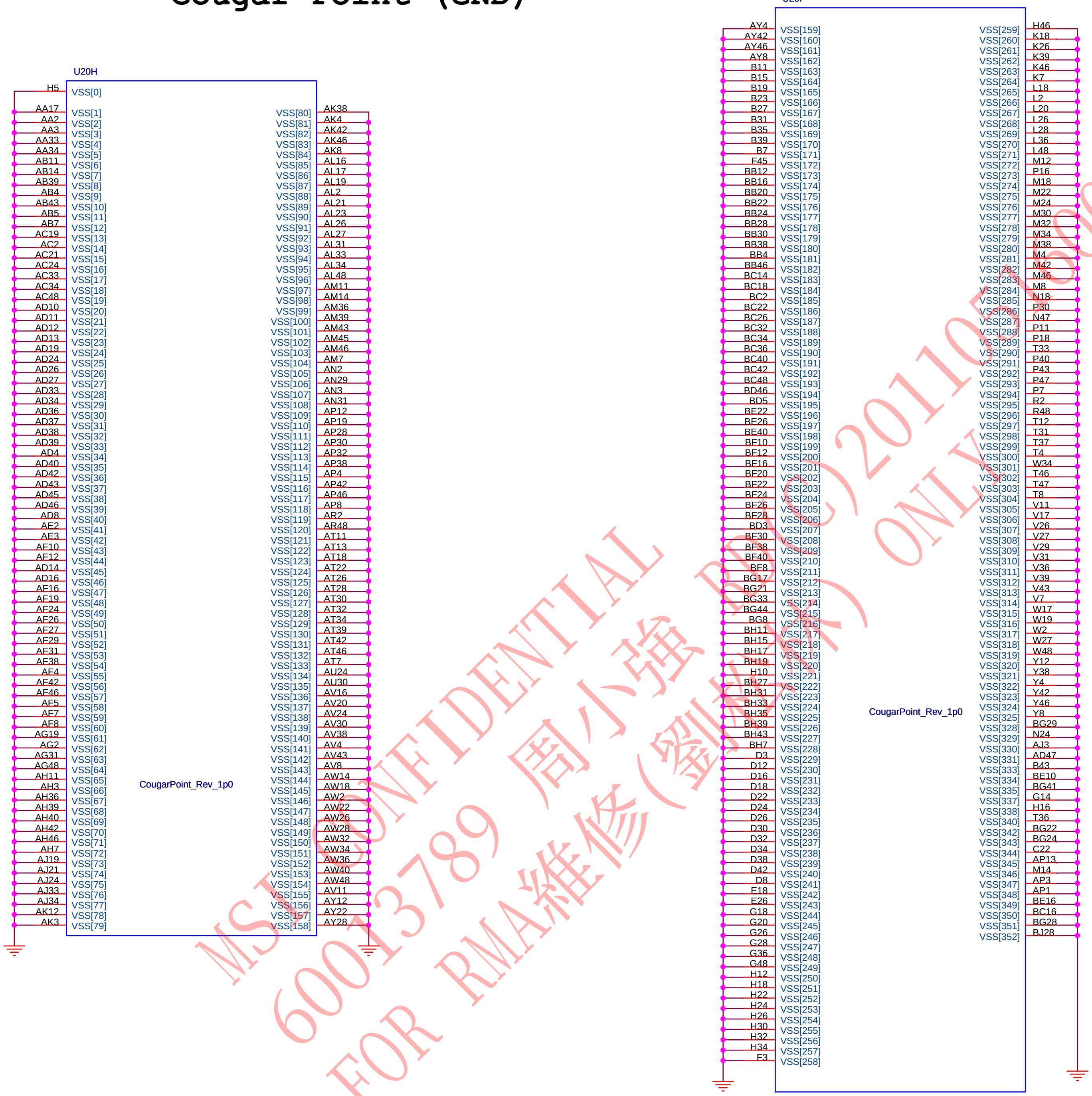
Title	PCH_POWER	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 23 of 52	

COUGAR POINT (POWER)

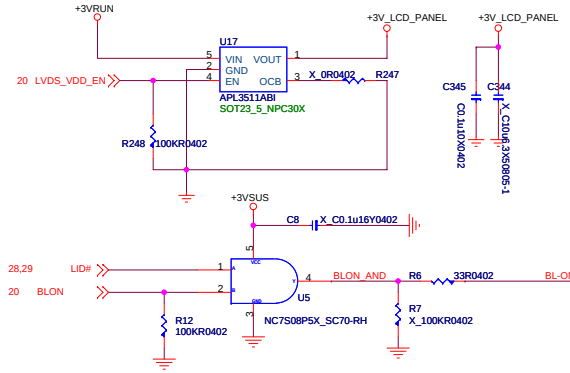


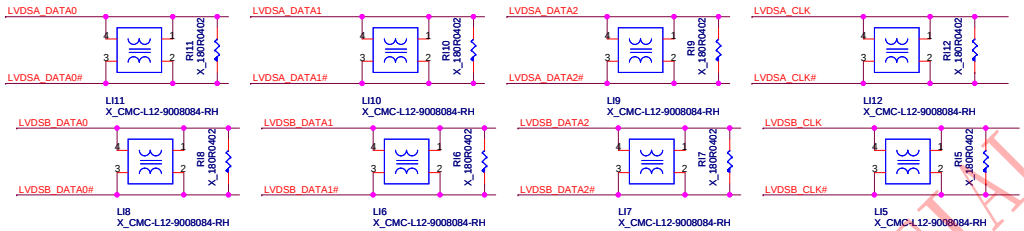
Title	PCH_POWER		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 24 of 52		

Cougar Point (GND)



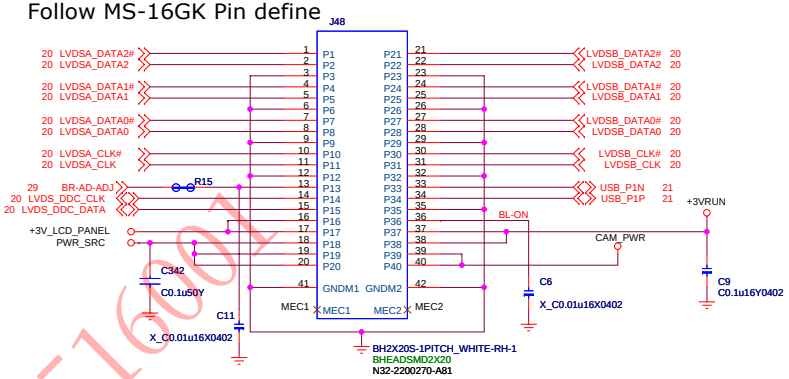
Title	PCH_GND	
Size Custom	Document Number MS-16G9/1754	Rev 10
Date: Thursday, June 30, 2011	Sheet 25 of 52	



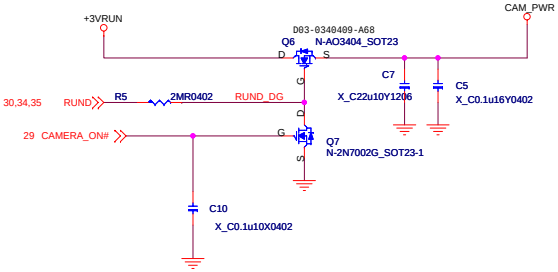


ChA.L ChB.H

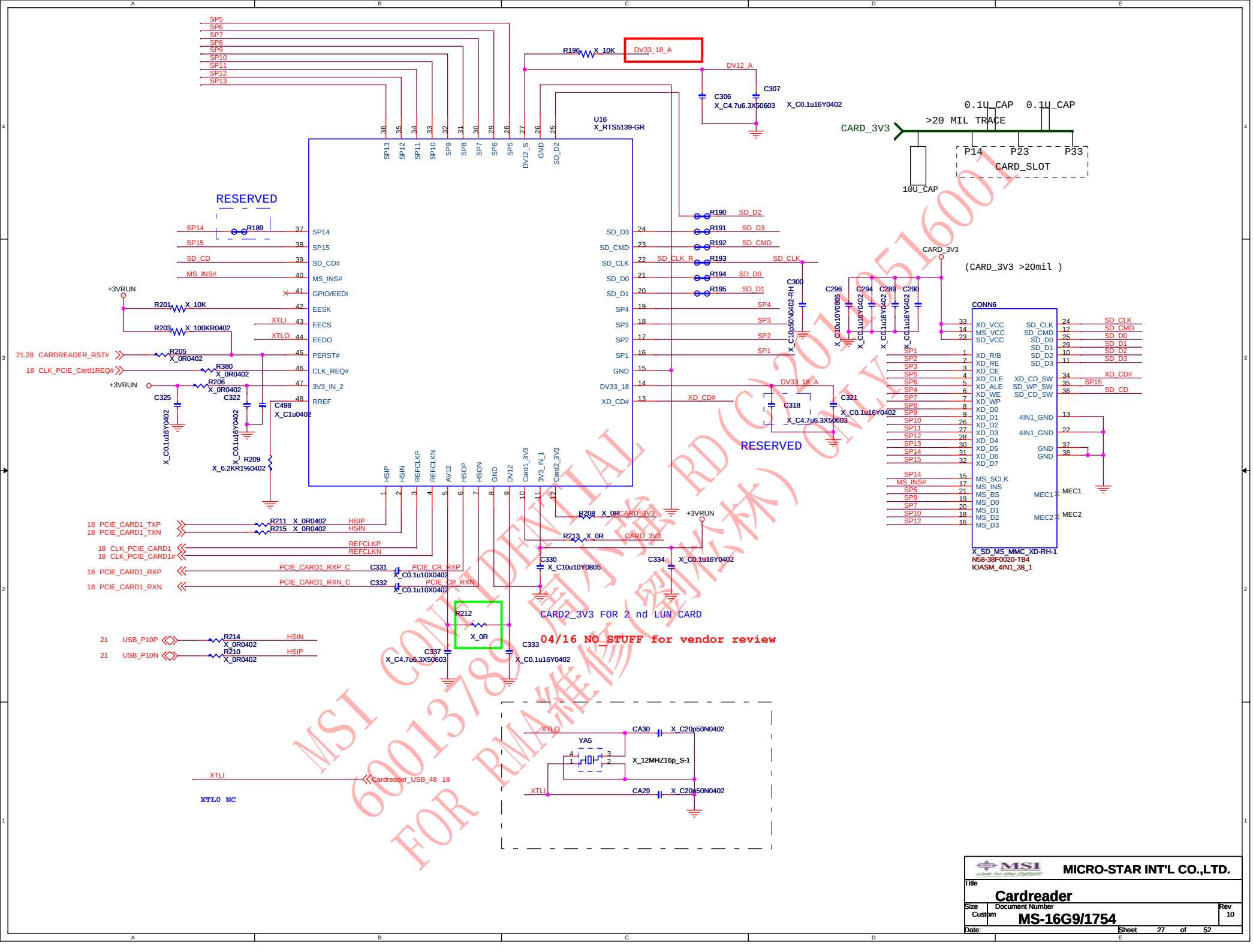
Follow MS-16GK Pin define



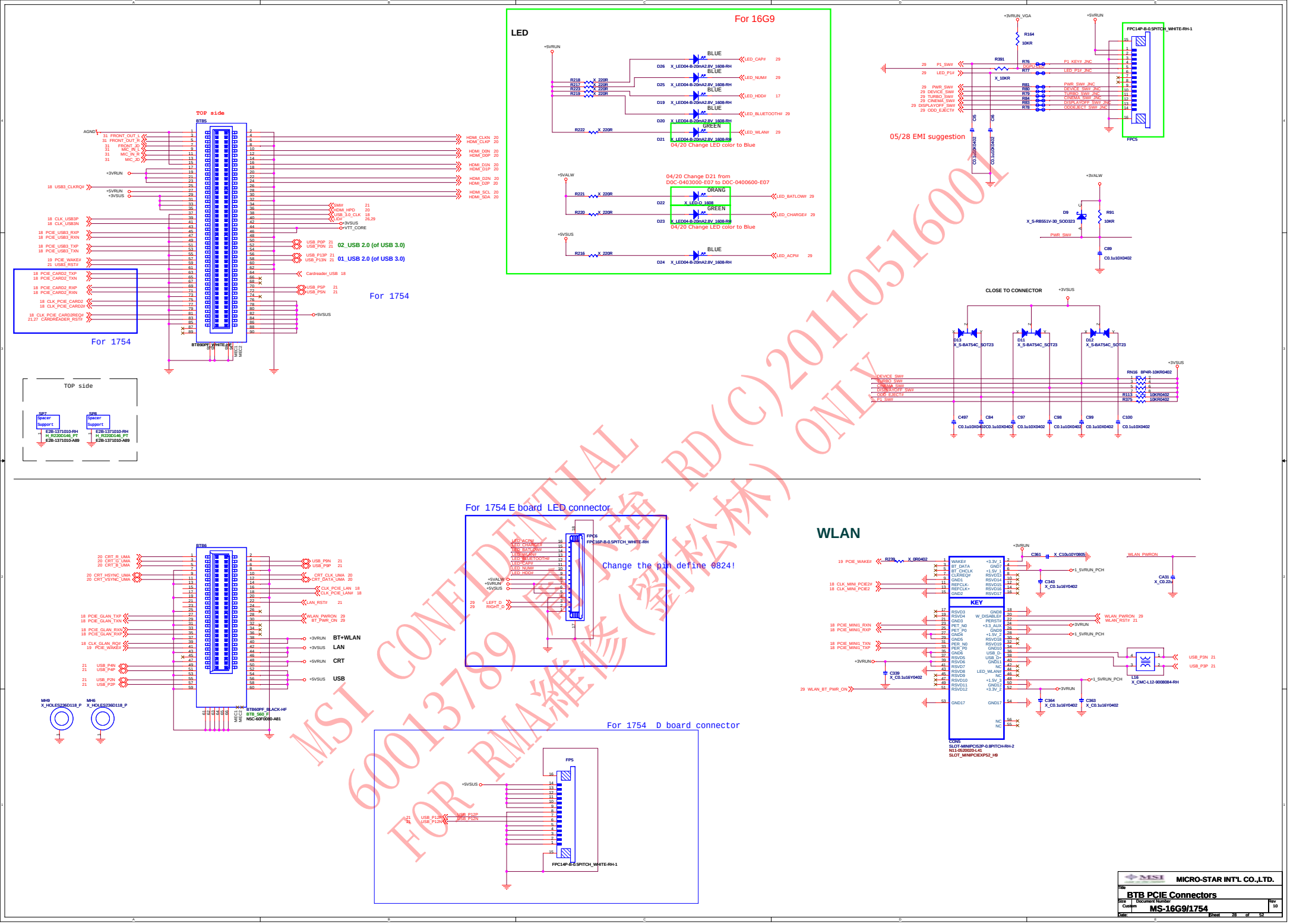
CAMERA LVDS ON

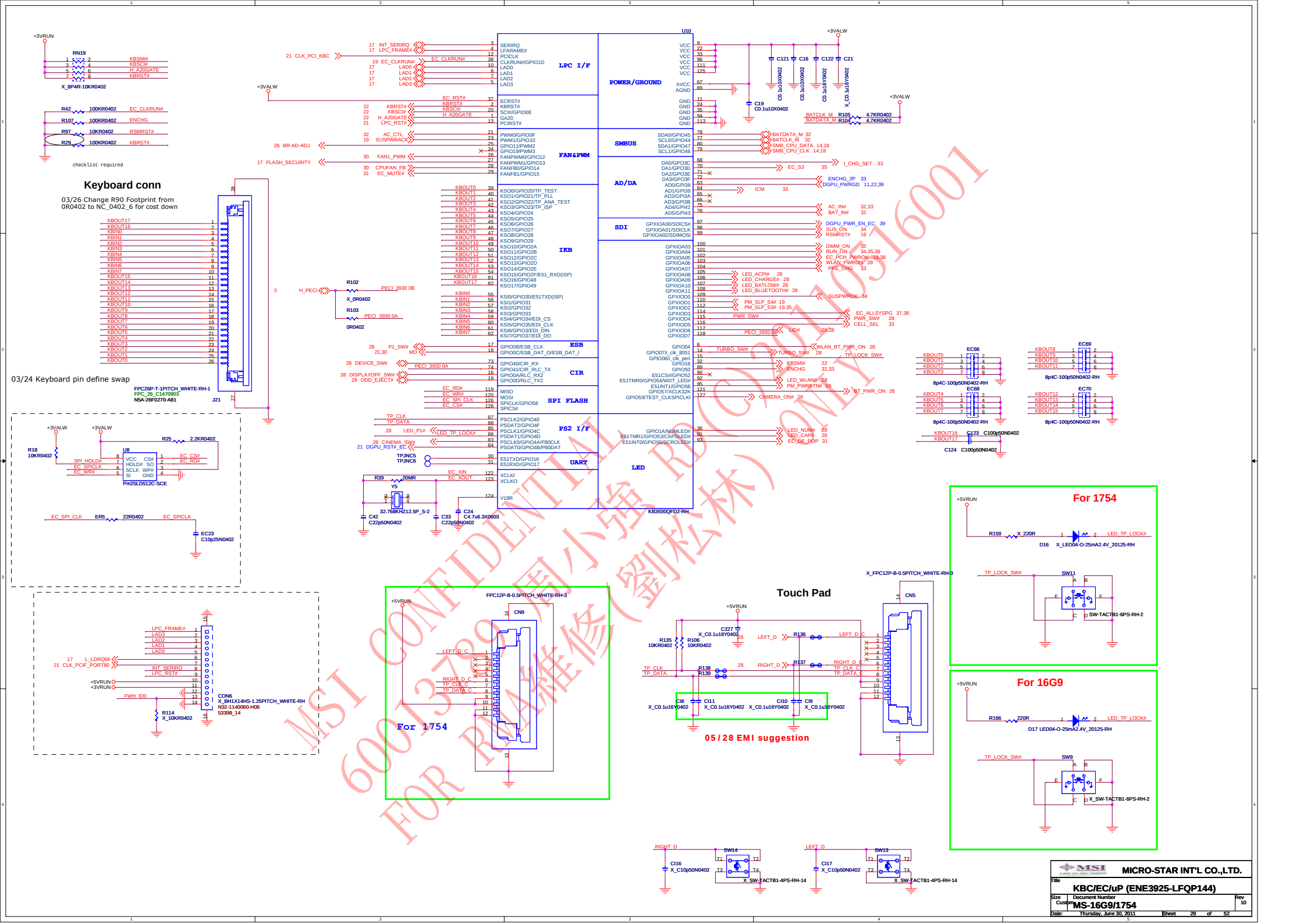


Title	CRT/LVDS/CCD		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 26 of 52		



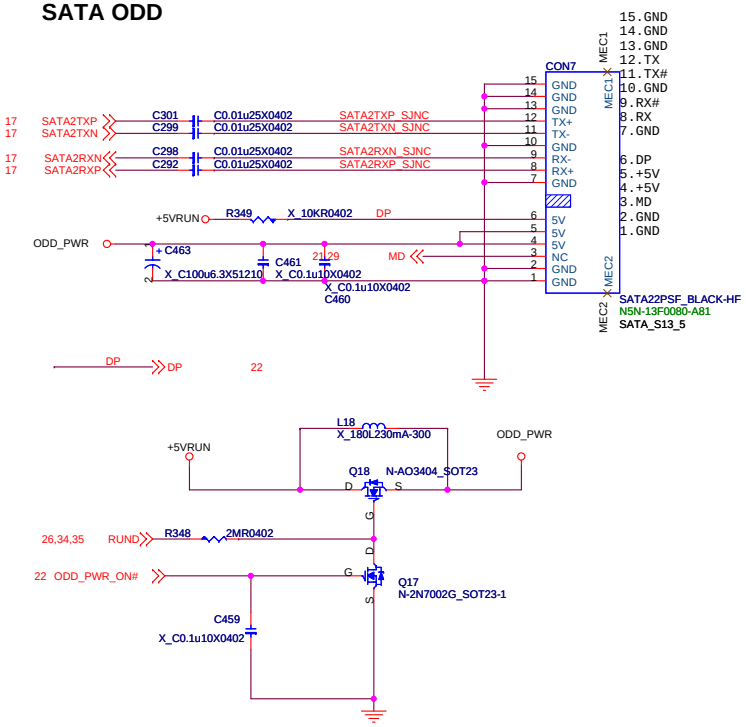
MSI	MICRO-STAR INT'L CO.,LTD.
Title	Cardreader
Size	Custom
Document Number	MS-16G9/1754
Rev	10
Date:	Sheet 27 of 52



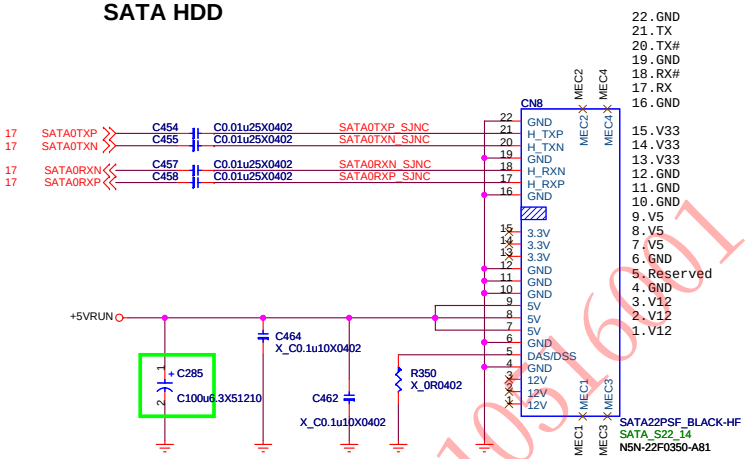


Title	MICRO-STAR INT'L CO.,LTD.
	KBC/EC/uP (ENE3925-LFQP144)
Size	Document Number: MS-16G9/1754
Rev	10
Date:	Thursday, June 30, 2011
Sheet	29 of 52

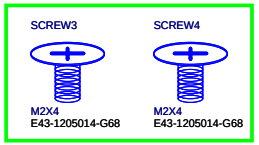
SATA ODD



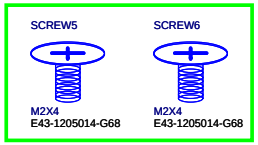
SATA HDD



2009/05/15 ə for Staggered Spin-up



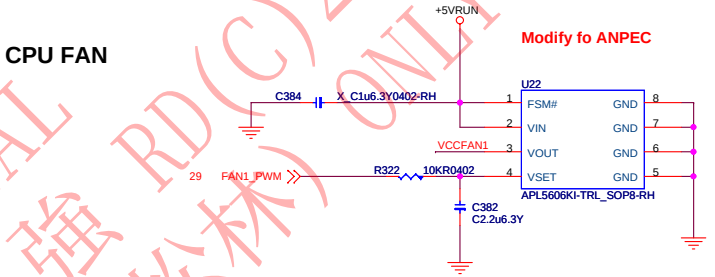
SCREW3,SCREW4 FOR HDD!

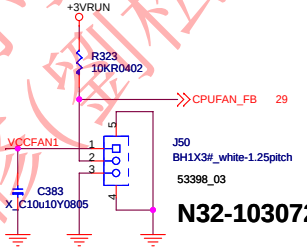


SCREW5,SCREW6 FOR 0DD!

CPU FAN

Modify fo ANPEC





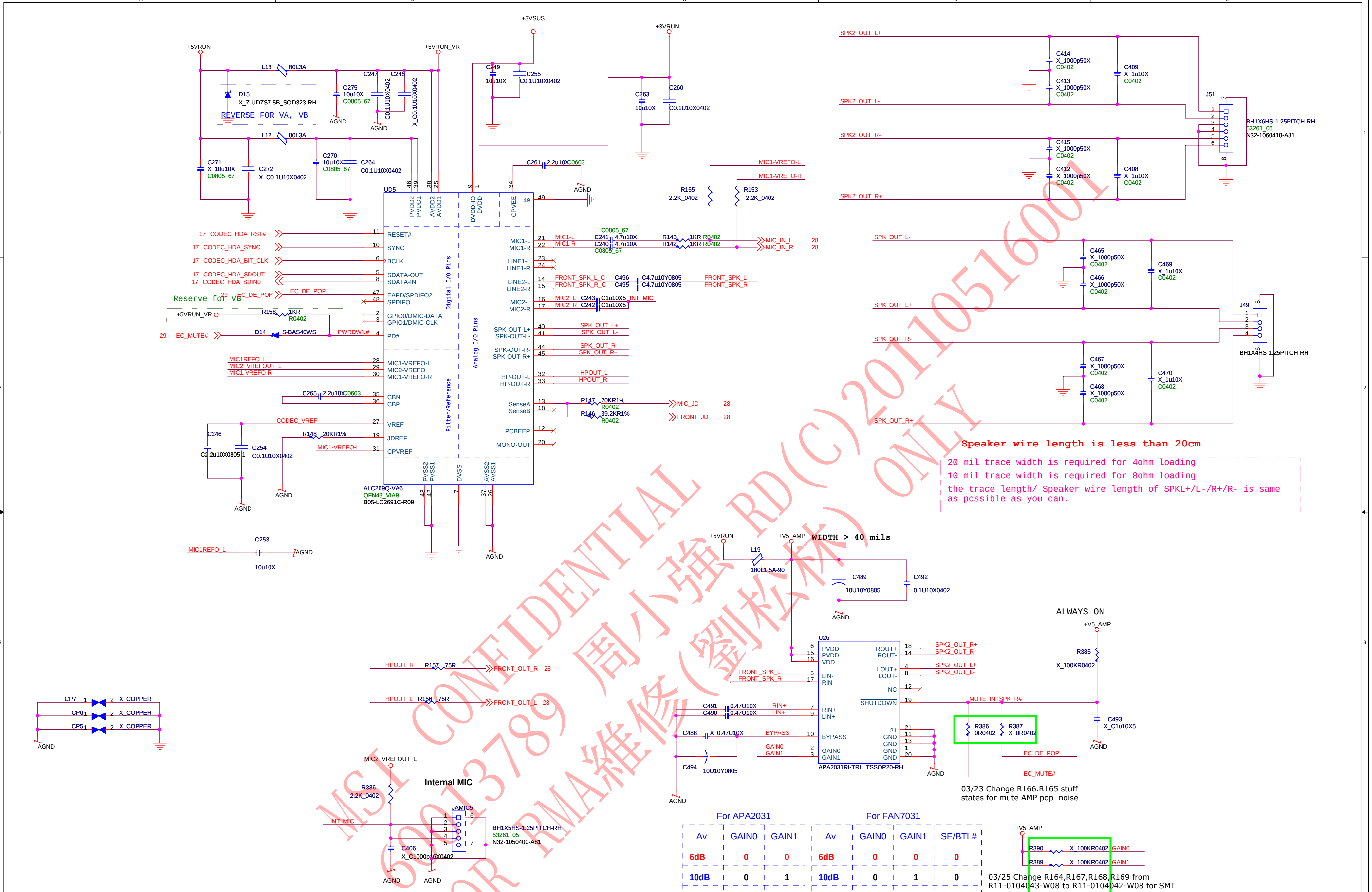
N32-1030720-A81

MICRO-STAR INT'L CO.,LTD.

Title: HDD2/ODD/ESATA Combo/FAN/BT

Size: Custom | Document Number: MS-16G9/1754 | Rev: 10

Date: Thursday, June 30, 2011 | Sheet 30 of 52



+5VRUN
+5VRUN_VR
+3VSUS
+3VRUN
L13 80L3A
L12 80L3A
D15 X_Z-UDZS7.5B_SOD323-RH
REVERSE FOR VA, VB
C275 10u10X C0805_67
C247 C0.1U10X0402
C245 X_C0.1U10X0402
C249 10u10X
C255 C0.1U10X0402
C263 10u10X
C260 C0.1U10X0402
C271 X_10u10X C0805_67
C272 X_C0.1U10X0402
C270 10u10X C0805_67
C264 C0.1U10X0402
C261 2.2u10X C0603
UD5
ALC269Q-VA6
QFN48_VIA9
B05-LC2691C-R09
Digital I/O Pins
Analog I/O Pins
Filter/Reference
17 CODEC_HDA_RST#
17 CODEC_HDA_SYNC
17 CODEC_HDA_BIT_CLK
17 CODEC_HDA_SDOUT
17 CODEC_HDA_SDIN0
Reserve for VB
29 EC_DE_POP
R158 1KR R0402
D14 S-BAS40WS
29 EC_MUTE#
PWRDWN#
MIC1REFO_L
MIC2_VREFOUT_L
MIC1-VREFO-R
C265 2.2u10X C0603
CODEC_VREF
C246 C2.2u10X0805-1
C254 C0.1U10X0402
R148 20KR1%
MIC1-VREFO-L
AGND
R155 2.2K_0402
R153 2.2K_0402
MIC1-VREFO-L
MIC1-VREFO-R
C241 4.7u10X
C240 4.7u10X
C0805_67
R143 1KR R0402
R142 1KR R0402
MIC_IN_L 28
MIC_IN_R 28
FRONT_SPK_L_C
FRONT_SPK_R_C
C496 C4.7u10Y0805
C495 C4.7u10Y0805
FRONT_SPK_L
FRONT_SPK_R
MIC2_L C243 C1u10X5
MIC2_R C242 C1u10X5
INT_MIC
SPK_OUT_L+
SPK_OUT_L-
SPK_OUT_R-
SPK_OUT_R+
HPOUT_L
HPOUT_R
R147 20KR1% R0402
R146 39.2KR1% R0402
MIC_JD 28
FRONT_JD 28
C253 10u10X
SPK2_OUT_L+
SPK2_OUT_L-
SPK2_OUT_R-
SPK2_OUT_R+
C414 X_1000p50X C0402
C413 X_1000p50X C0402
C409 X_1u10X C0402
C415 X_1000p50X C0402
C412 X_1000p50X C0402
C408 X_1u10X C0402
J51
BH1X6HS-1.25PITCH-RH
53261_06
N32-1060410-A81
C465 X_1000p50X C0402
C466 X_1000p50X C0402
C469 X_1u10X C0402
C467 X_1000p50X C0402
C468 X_1000p50X C0402
C470 X_1u10X C0402
J49
BH1X4HS-1.25PITCH-RH
Speaker wire length is less than 20cm
20 mil trace width is required for 4ohm loading
10 mil trace width is required for 8ohm loading
the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same as possible as you can.
+V5_AMP
WIDTH > 40 mils
L19 180L1.5A-90
C489 10U10Y0805
C492 0.1U10X0402
U26
APA2031RI-TRL_TSSOP20-RH
FRONT_SPK_L
FRONT_SPK_R
C491 0.47U10X RIN+
C490 0.47U10X LIN+
C488 X_0.47U10X BYPASS
C494 10U10Y0805
GAIN0
GAIN1
SPK2_OUT_R+
SPK2_OUT_R-
SPK2_OUT_L+
SPK2_OUT_L-
MUTE_INTSPK_R#
ALWAYS ON
R385 X_100KR0402
C493 X_C1u10X5
R386 0R0402
R387 X_0R0402
EC_DE_POP
EC_MUTE#
03/23 Change R166.R165 stuff states for mute AMP pop noise
HPOUT_R R157 75R FRONT_OUT_R 28
HPOUT_L R156 75R FRONT_OUT_L 28
CP7 X_COPPER
CP6 X_COPPER
CP5 X_COPPER
MIC2_VREFOUT_L
Internal MIC
R336 2.2K_0402
INT_MIC
JAMIC5
BH1X5HS-1.25PITCH-RH
53261_05
N32-1050400-A81
C406 X_C1000p16X0402
R390 X_100KR0402 GAIN0
R389 X_100KR0402 GAIN1
R384 100KR0402 GAIN0
R388 100KR0402 GAIN1
03/25 Change R164,R167,R168,R169 from R11-0104043-W08 to R11-0104042-W08 for SMT cost down

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

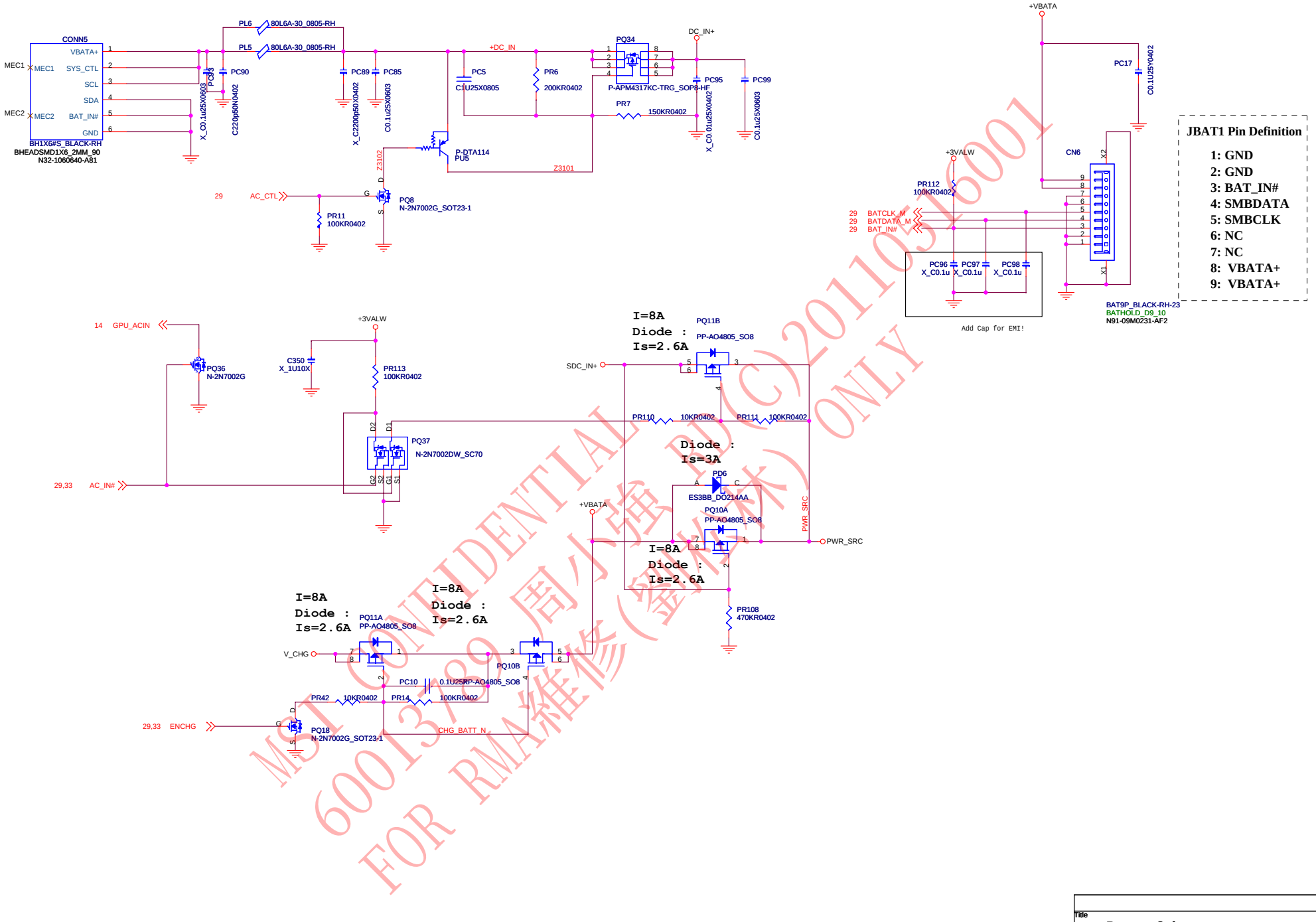
Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

MSI MICRO-STAR INT'L CO.,LTD.

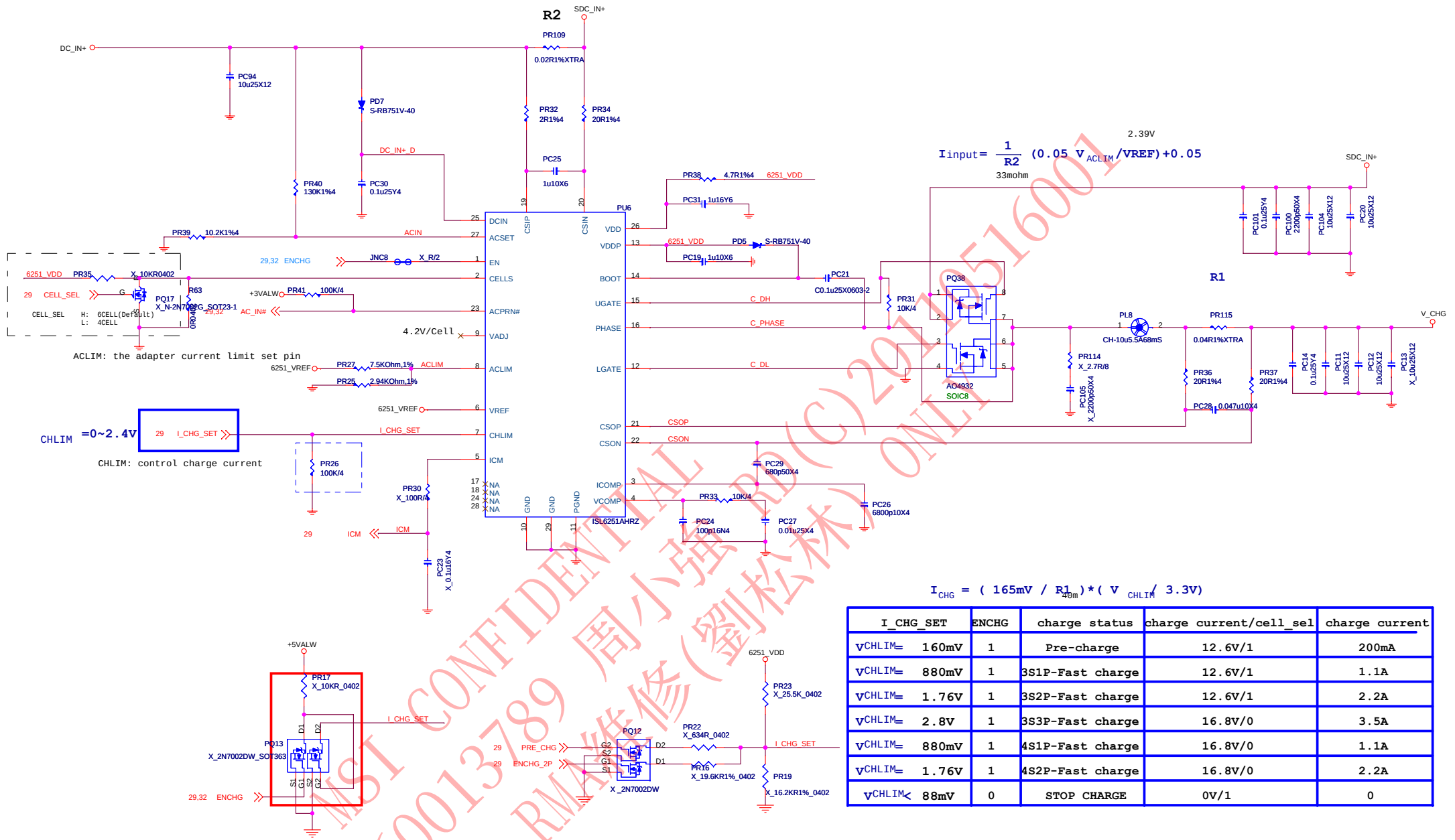
Title: AZALIA CODEC (ALC269Q_VA6)

Size: C Document Number: MS-16G9/1754 Rev: 10

Date: Thursday, June 30, 2011 Sheet 31 of 52



Title	Battery Select		
Size: Custom	Document Number: MS-16G9/1754		Rev: 10
Date: Thursday, June 30, 2011	Sheet 32 of 52		



$$I_{CHG} = (165mV / R1_{40m})*(V_{CHLIM} / 3.3V)$$

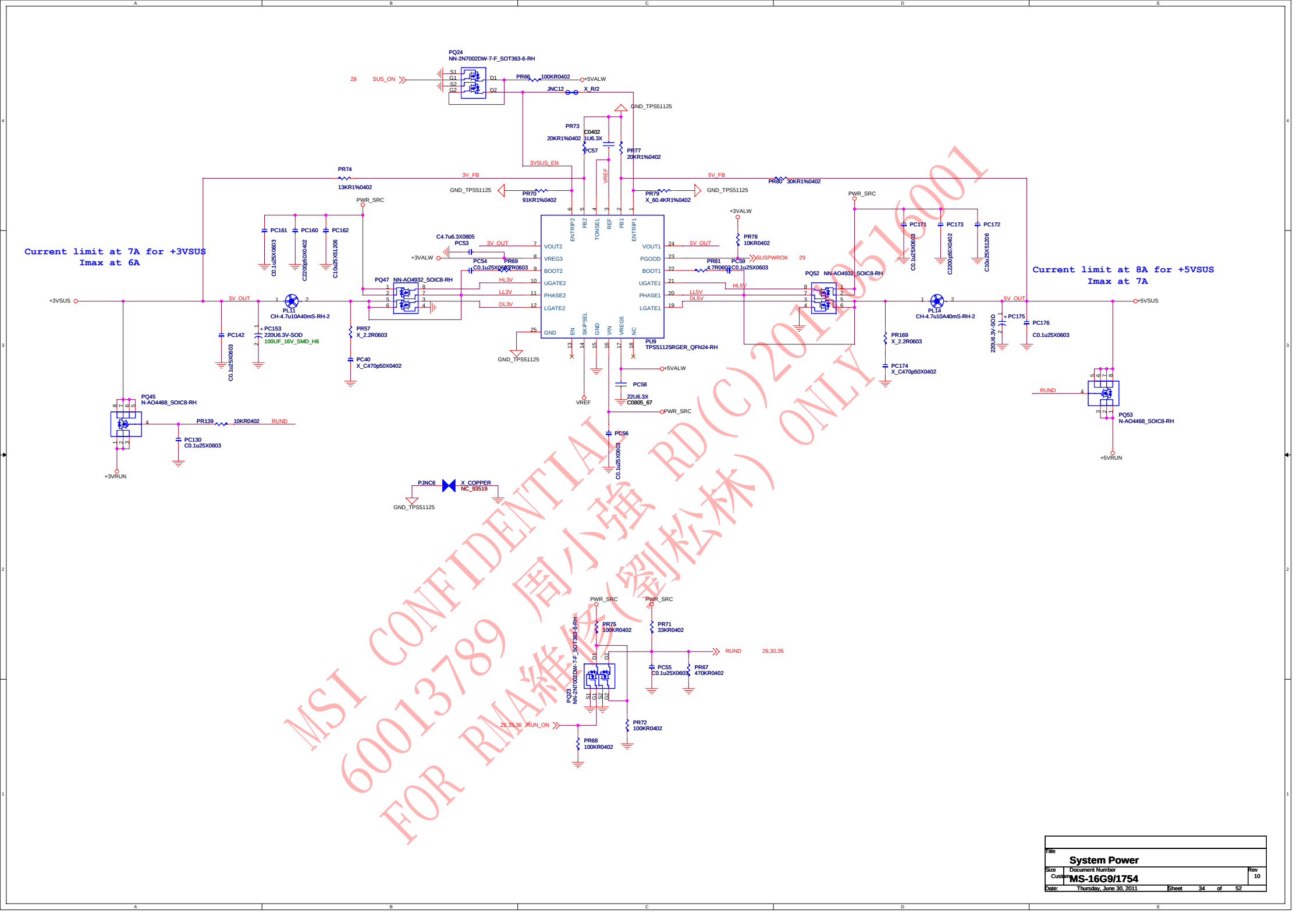
I_CHG_SET	ENCHG	charge status	charge current/cell_sel	charge current
VCHLIM= 160mV	1	Pre-charge	12.6V/1	200mA
VCHLIM= 880mV	1	3S1P-Fast charge	12.6V/1	1.1A
VCHLIM= 1.76V	1	3S2P-Fast charge	12.6V/1	2.2A
VCHLIM= 2.8V	1	3S3P-Fast charge	16.8V/0	3.5A
VCHLIM= 880mV	1	4S1P-Fast charge	16.8V/0	1.1A
VCHLIM= 1.76V	1	4S2P-Fast charge	16.8V/0	2.2A
VCHLIM< 88mV	0	STOP CHARGE	0V/1	0

MICRO-STAR INT'L CO.,LTD.

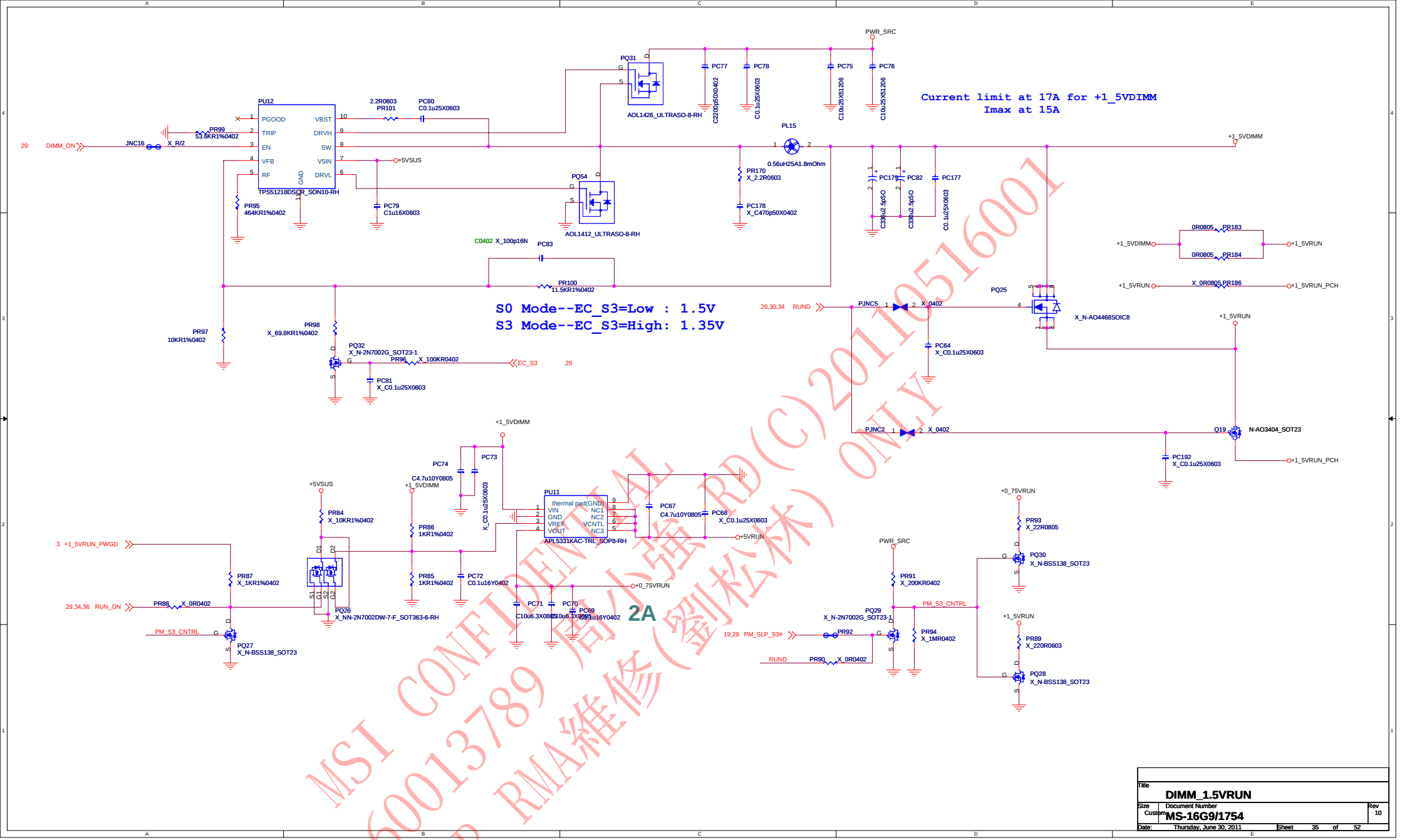
Title: Battery Charger

Size: Custom | Document Number: MS-16G9/1754 | Rev: 10

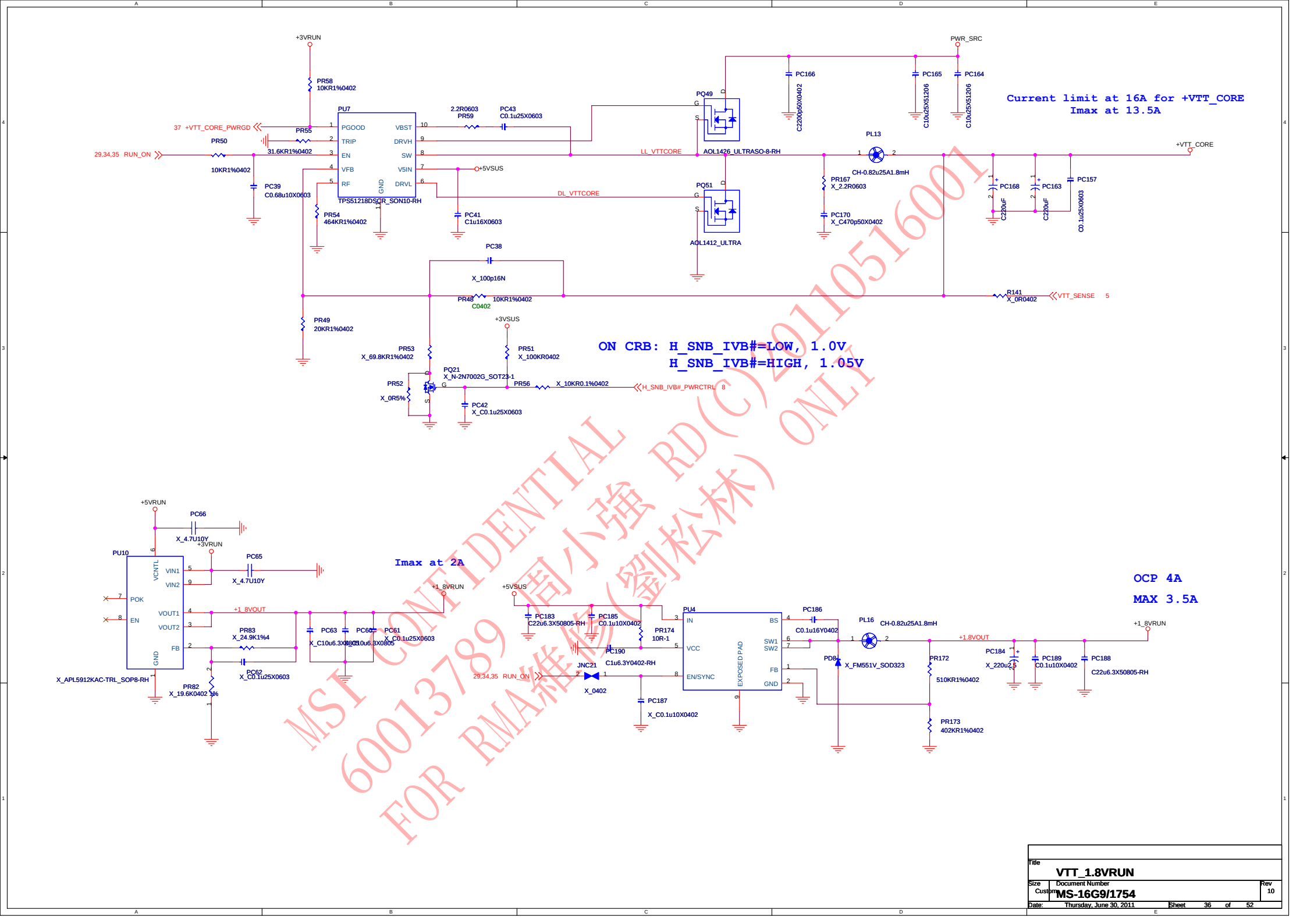
Date: Thursday, June 30, 2011 | Sheet 33 of 52



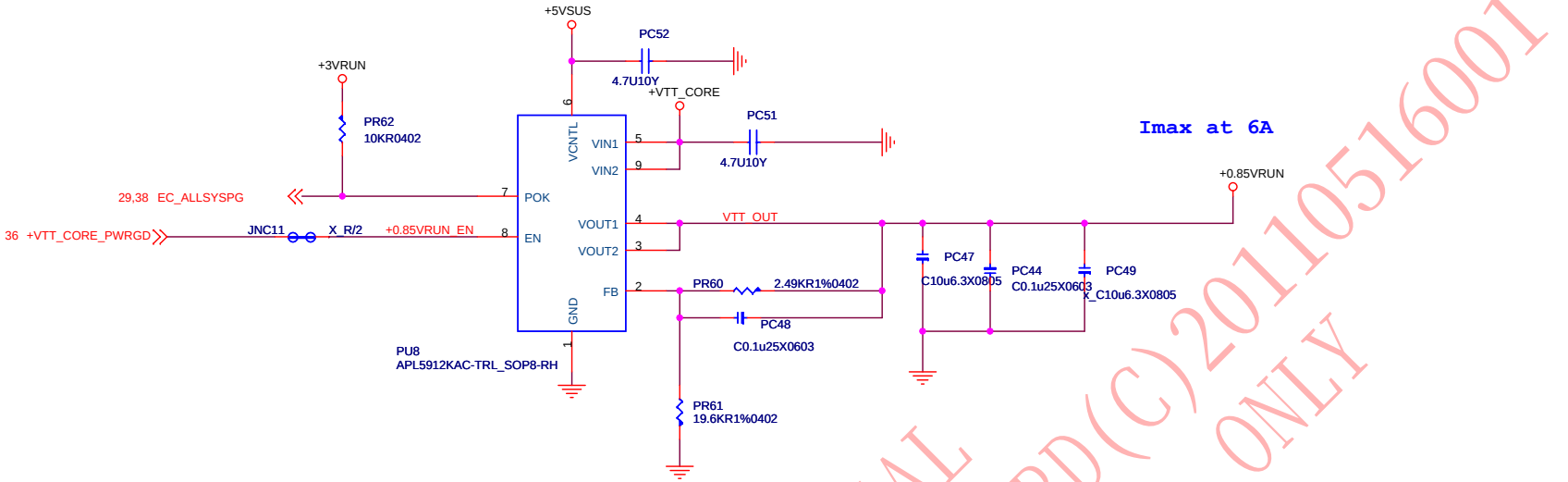
Title	System Power	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 34 of 52	

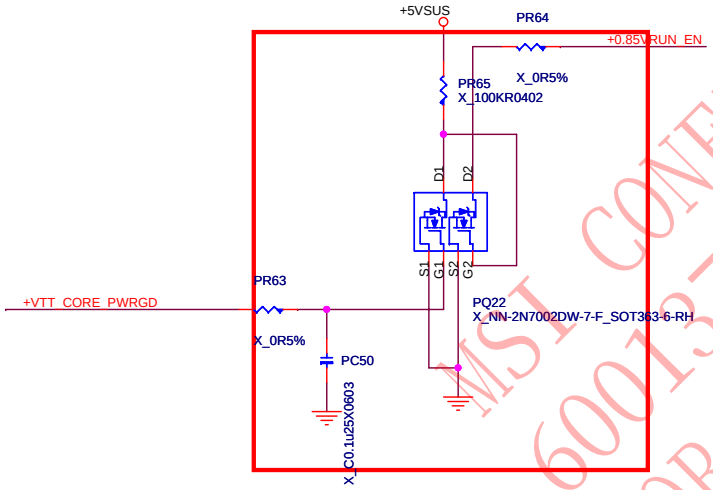


Title	DIMM_1.5VRUN	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 35 of 52	

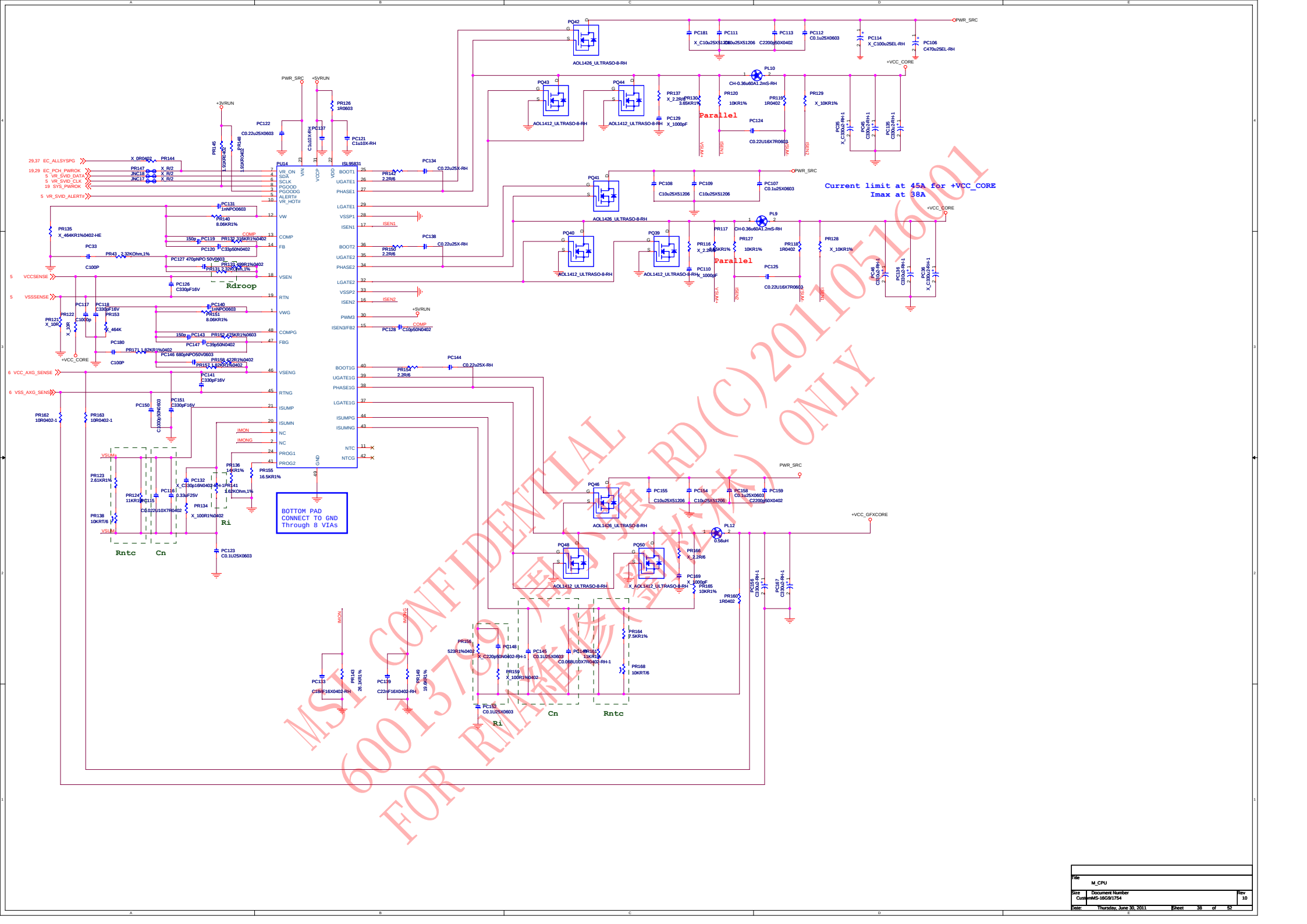


Title	VTT_1.8VRUN	
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 36 of 52	

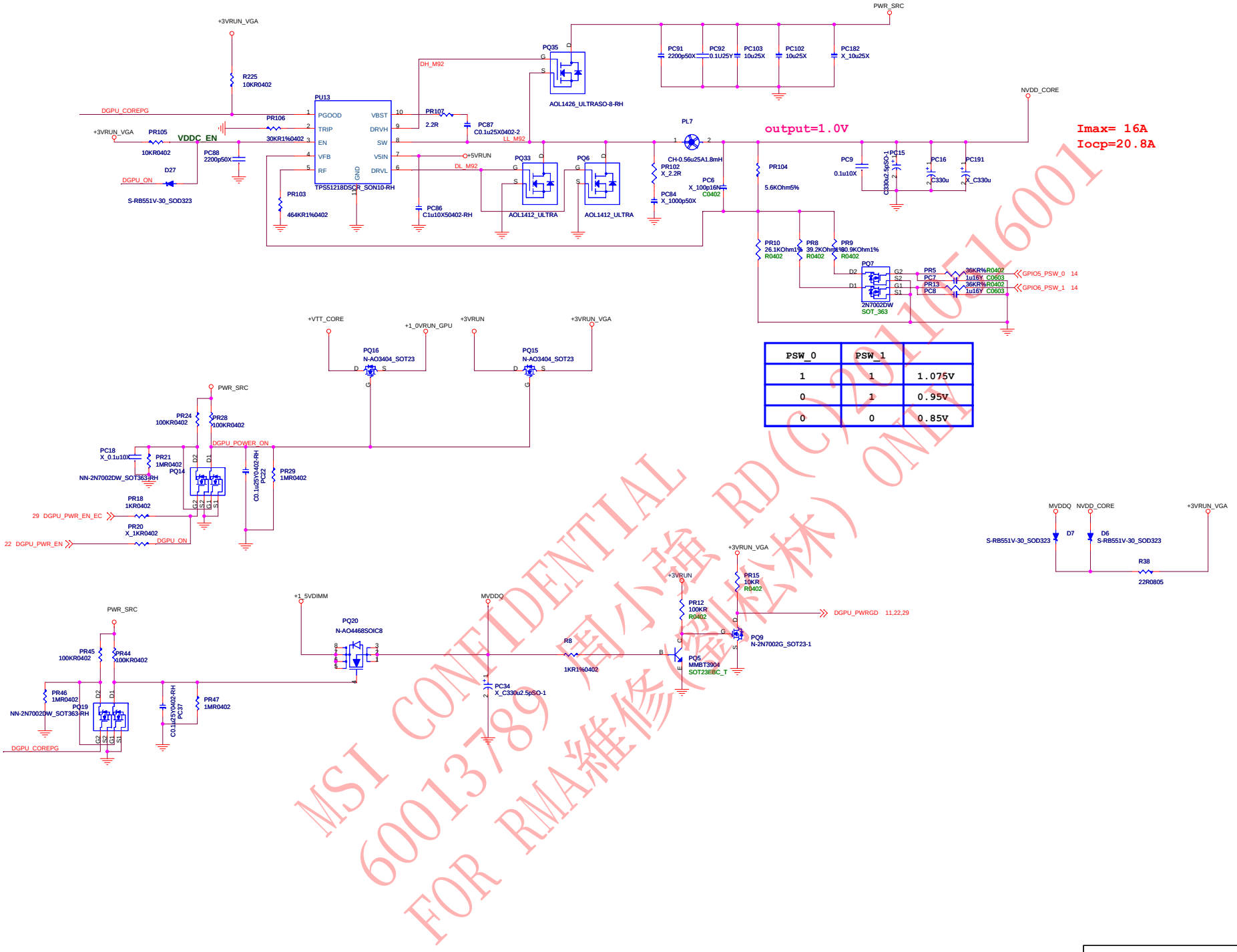




Title	0.85V	
Size B	Document Number MS-16G9/1754	Rev 10
Date: Thursday, June 30, 2011	Sheet 37 of 52	

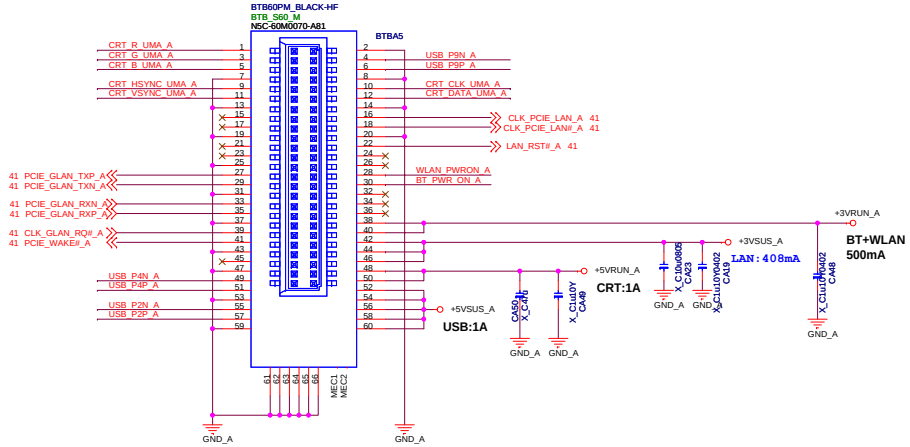


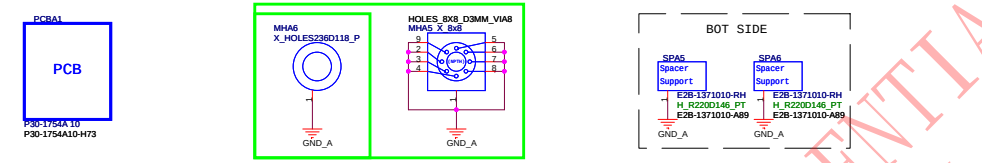
Title	M_CPU		
Size	Document Number		Rev
Custom	MS-16G9/1754		10
Date:	Thursday, June 30, 2011	Sheet 38 of 52	



Title	DGPU Power		
Size C	Document Number MS-16G9/1754		Rev 10
Date: Thursday, June 30, 2011	Sheet 39	of 52	

(ESATA,USB,LAN,CRT,BT+WLAN)

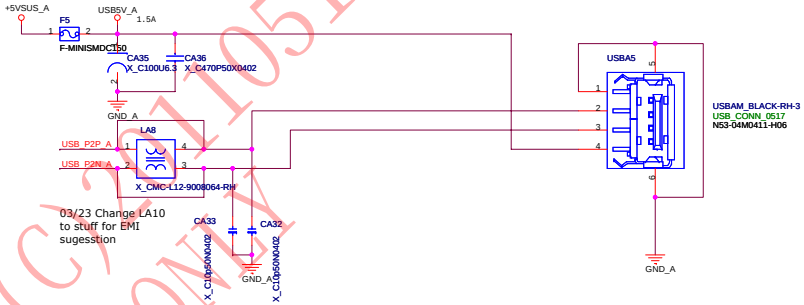




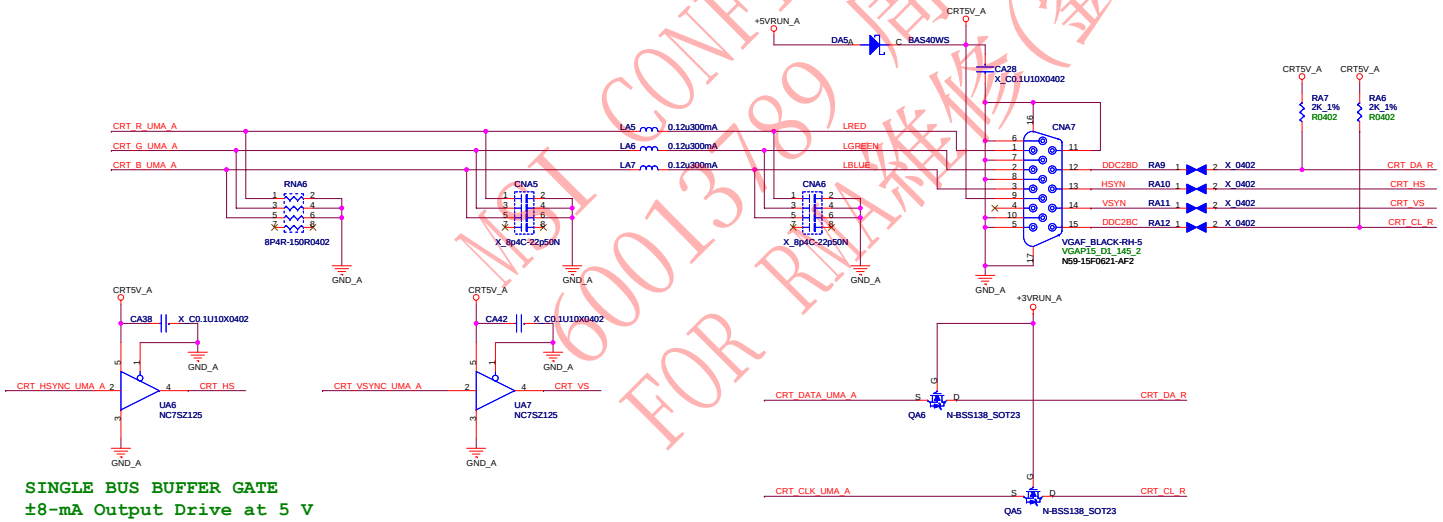
02/25 Change MHA8 to HOLES_R276D185P_PT

03/30 Change MHA8 to HOLES236D118_P

02/23 Change to 8 vias for EMI sugesstion

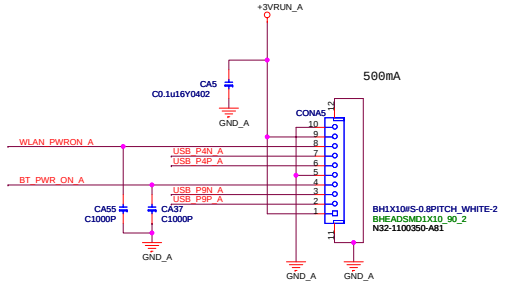


D-Sub Connecor

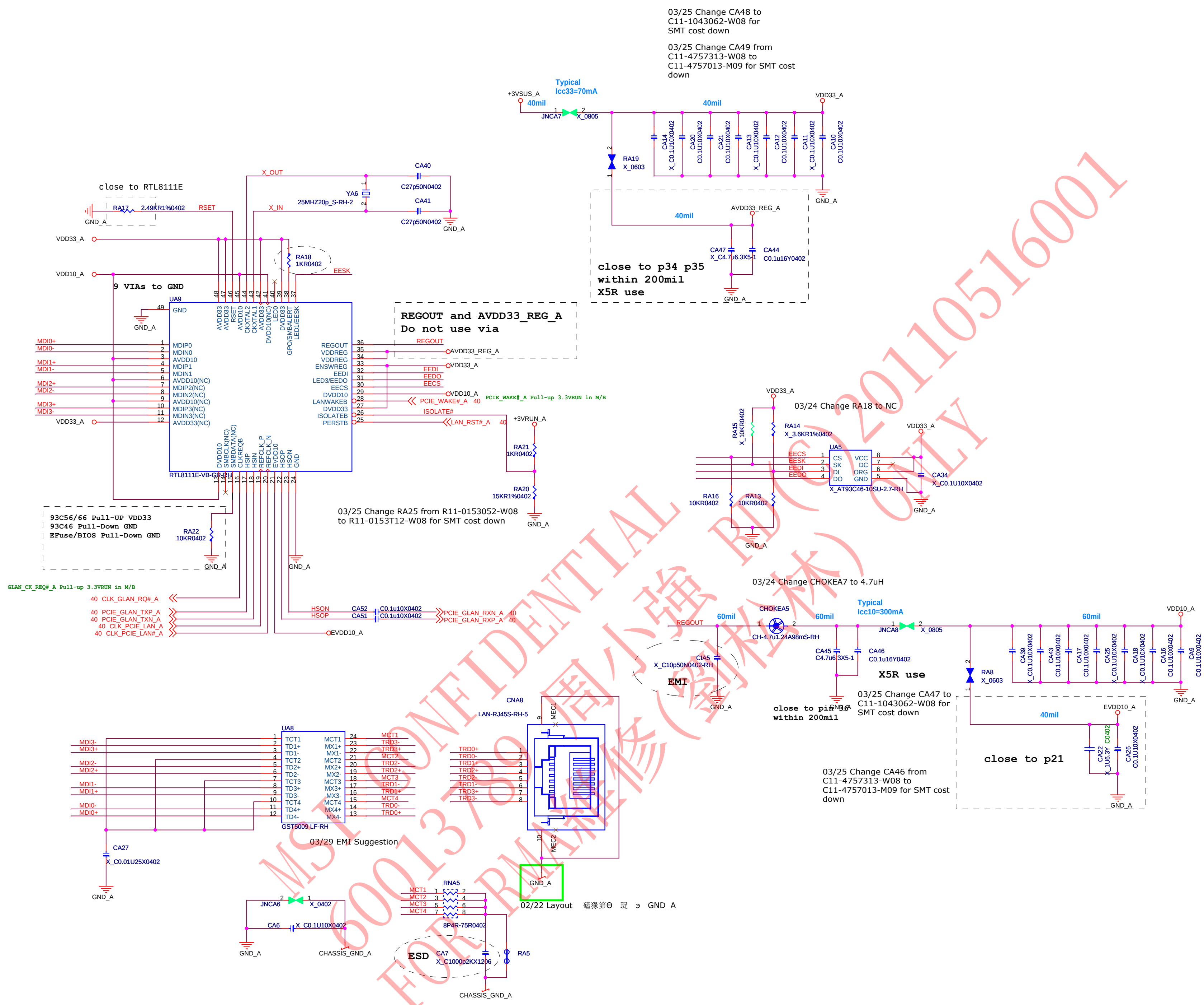


SINGLE BUS BUFFER GATE
±8-mA Output Drive at 5 V

BT and WLAN Combo Connector



MICRO-STAR INT'L CO.,LTD.	
Title	CRT/USB/LAN/BT/Conn
Size: Custom	Document Number: MS-16G9/1754 Rev: 10
Date: Thursday, June 30, 2011	Sheet 40 of 52

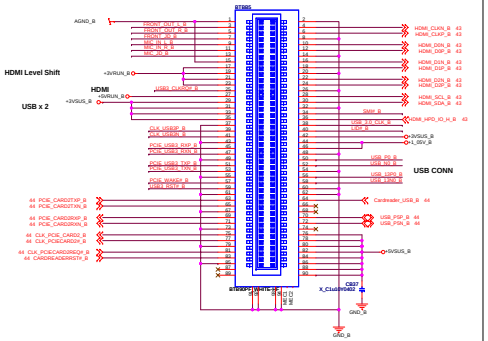


MICRO-STAR INT'L CO.,LTD.

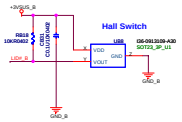
Title: PCIE GLAN(RTL8111E)

Size	Document Number	Rev
Custom	MS-16G9/1754	10

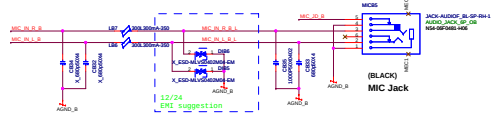
Date: Thursday, June 30, 2011 Sheet 41 of 52

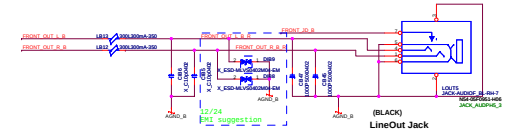


LID Switch



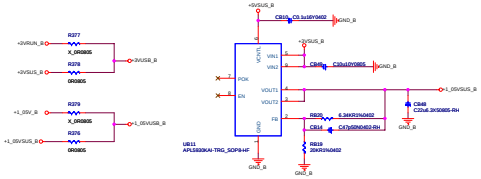
Audio Jack

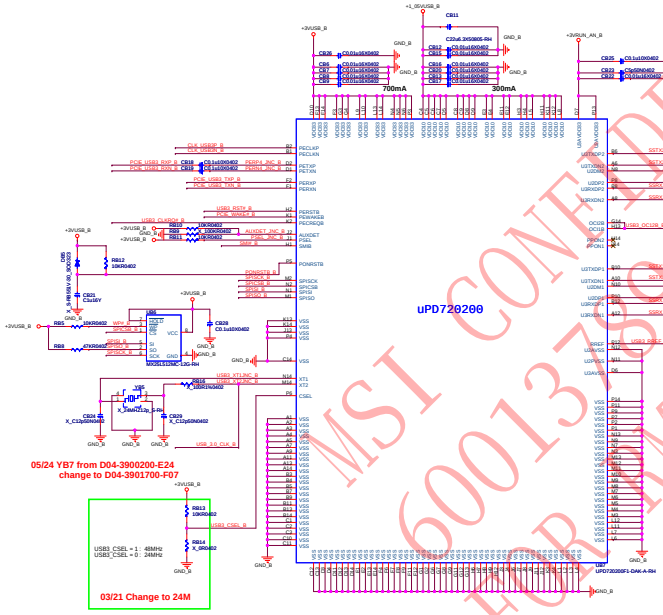


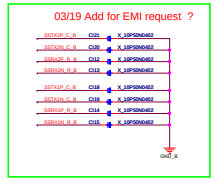


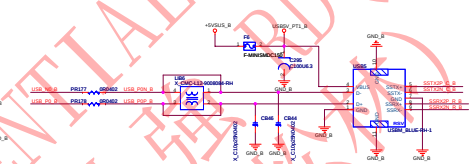
(才凹Card reader,USB 3.0 x 2)

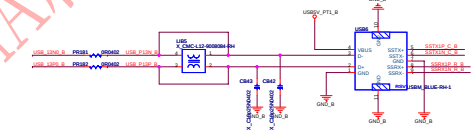
USB 3.0 Connector

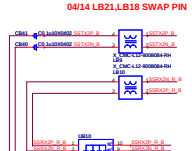


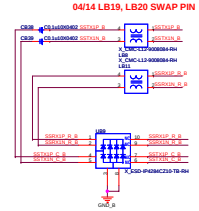












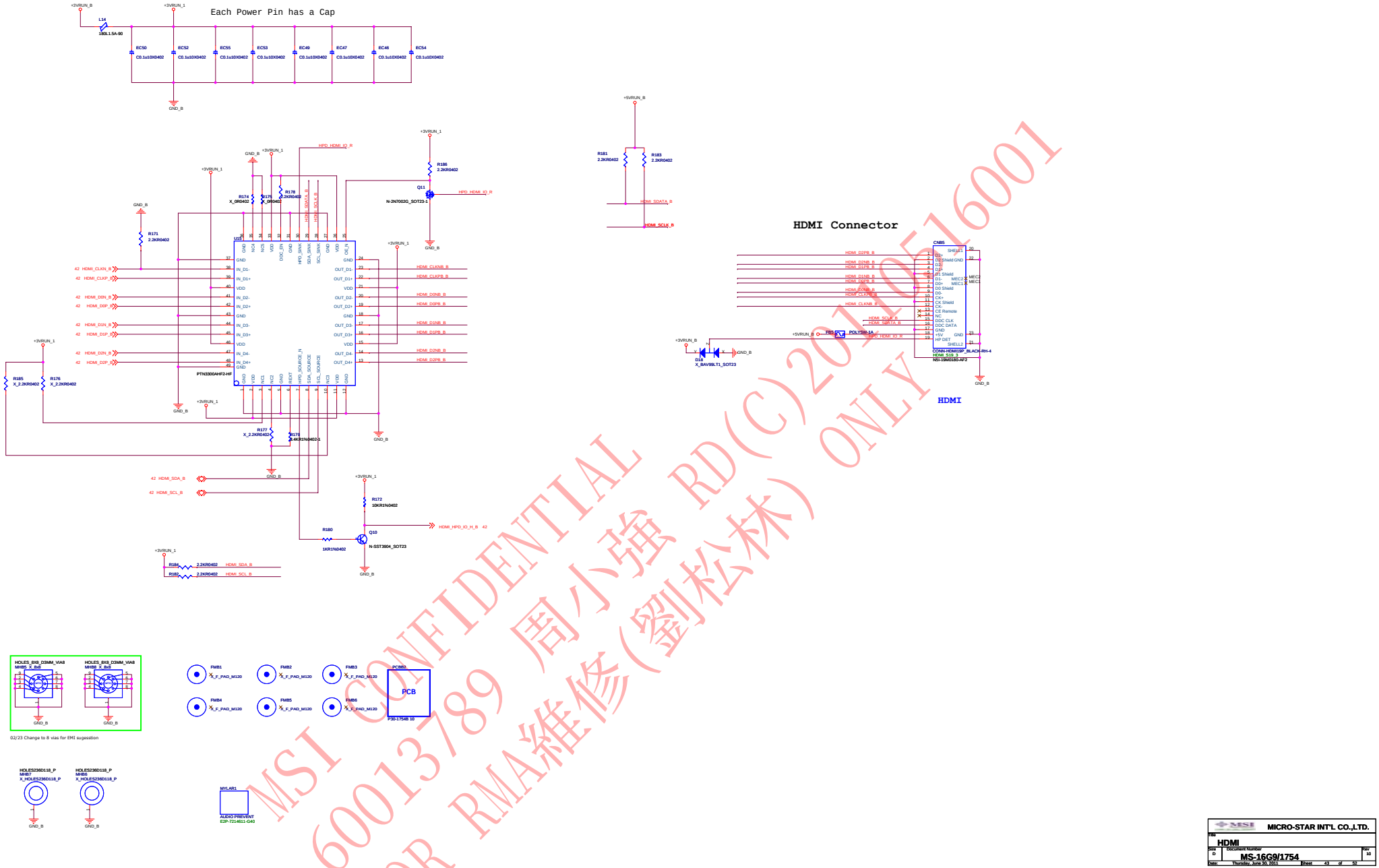
MICRO-STAR INT'L CO.,LTD.

Audio/USB*2/Conn

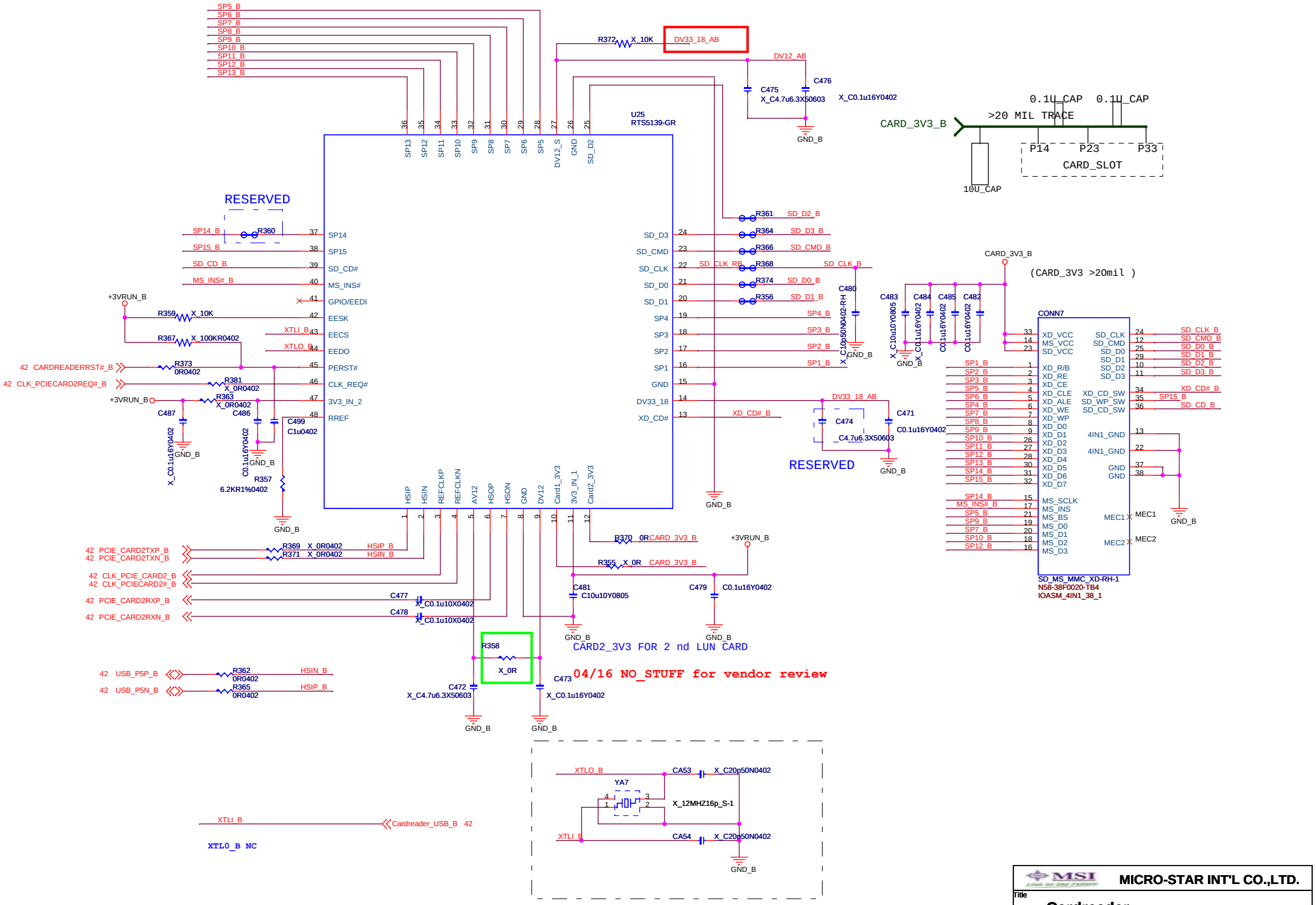
Code: MS-16G9/1754

Rev: 1.0

Date: Thursday, June 30, 2011 Sheet 43 of 53



MICRO-STAR INT'L CO.,LTD.			
Title: HDMI			
Size: D	Document Number: MS-16G9/1754		Rev: 3.0
Date: Thursday, June 30, 2022	Sheet: 43	of: 52	


U25
RTS5139-GR
RESERVED
R372 X_10K DV33_18_AB
DV12_AB
C475 X_C4.7u6.3X50603
C476 X_C0.1u16Y0402
GND_B
CARD_3V3_B
0.1U_CAP 0.1U_CAP
>20 MIL TRACE
P14 P23 P33
CARD_SLOT
10U_CAP
(CARD_3V3 >20mil)
CONN7
SD_MS_MMC_XD-RH-1
N58-38F0020-TB4
IOASM_4IN1_38_1
R359 X_10K
R367 X_100KR0402
R373 0R0402
R381 X_0R0402
R363 X_0R0402
R357 6.2KR1%0402
C487 C486 C499 C1u0402
C480 X_C10p50N0402-RH
C483 C484 C485 C482
R361 SD_D2_B
R364 SD_D3_B
R366 SD_CMD_B
R368 SD_CLK_B
R374 SD_D0_B
R356 SD_D1_B
SD_CLK_RD
XD_CD#_B
DV33_18_AB
C474 C4.7u6.3X50603
C471 C0.1u16Y0402
R369 X_0R0402 HSIP_B
R371 X_0R0402 HSIN_B
R370 0R CARD_3V3_B
R355 X_0R CARD_3V3_B
C481 C10u10Y0805
C479 C0.1u16Y0402
C477 X_C0.1u10X0402
C478 X_C0.1u10X0402
R358 X_0R
C472 X_C4.7u6.3X50603
C473 X_C0.1u16Y0402
CARD2_3V3 FOR 2 nd LUN CARD
04/16 NO_STUFF for vendor review
R362 0R0402 HSIN_B
R365 0R0402 HSIP_B
XTLI_B
Cardreader_USB_B 42
XTL0_B NC
YA7
X_12MHZ16p_S-1
CA53 X_C20p50N0402
CA54 X_C20p50N0402
MICRO-STAR INT'L CO.,LTD.
Title
Cardreader
Size Custom
Document Number
MS-16G9/1754
Rev 10
Date:
Sheet 44 of 52

03/30 Change LEDC7.LEDC8 from
D0C-04018F0-L05 to
D0C-0400600-E07

+5VRUN_C
RC6 100R
LEDC8 LED04-B-20mA2.8V_1608-RH (BLUE)
LEDC7 LED04-B-20mA2.8V_1608-RH (BLUE)
UMA_ON#

RC8 100R
LEDC4 LED-O_1608 Orange
DGPU_ON#

RC5 X_100R
LEDC6 X_LED-O_1608 (ORANGE)
LEDC5 X_LED-O_1608
LED_P1#_C

03/29 Remove ECO and Cinema LED for ID requestion

RC4 100KR0402
RC9 100KR0402
QC1 2N7002
RC7 X_0R0402
QC2 N-SST3904_SOT23
DGPU_LED_C
DGPU_ON#
UMA_ON#
GND_C

P.52
FPCC5
N5A-14F0090-A81
FPC_S14_3
FPC14P-T-0.5PITCH_WHITE-RH-2
P1_KEY#_C
DGPU_LED_C
LED_P1#_C
PWR_SW#_C
DEVICE_SW#_C
TURBO_SW#_C
CINEMA_SW#_C
DISPLAYOFF_SW#_C
ODDEJECT_SW#_C

PWR_SW#_C SW12
DEVICE_SW#_C SW8
TURBO_SW#_C SW7
P1_KEY#_C SW15
SW-TACTB1-6PS-RH-2

04/23 Change FPCC7 from N5A-14F0070-A81 to N5A-14F0090-A81(P/N only) for ME request

CNIC5
LED_P1#_C
DGPU_ON#
UMA_ON#
X_8p4C-0.1u25Y
03/30 SWAP

CINEMA_SW#_C SW10
DISPLAYOFF_SW#_C SW6
ODDEJECT_SW#_C SW5
04/28 Fix SWC8's HW mismatch

HOLES_NR91D91 HC2 X_ME_SCREW HOLE
HOLES_NR91D91 HC1 X_ME_SCREW HOLE

PWR_SW#_C DIC5
DEVICE_SW#_C DIC6
TURBO_SW#_C DIB7
CINEMA_SW#_C DIC7
DISPLAYOFF_SW#_C DIC8
ODDEJECT_SW#_C DIC9
P1_KEY#_C DIC10
UMA_ON#_C DIC11
DGPU_ON#_C DIC12
X_ESD-MLVS0402M04-EM

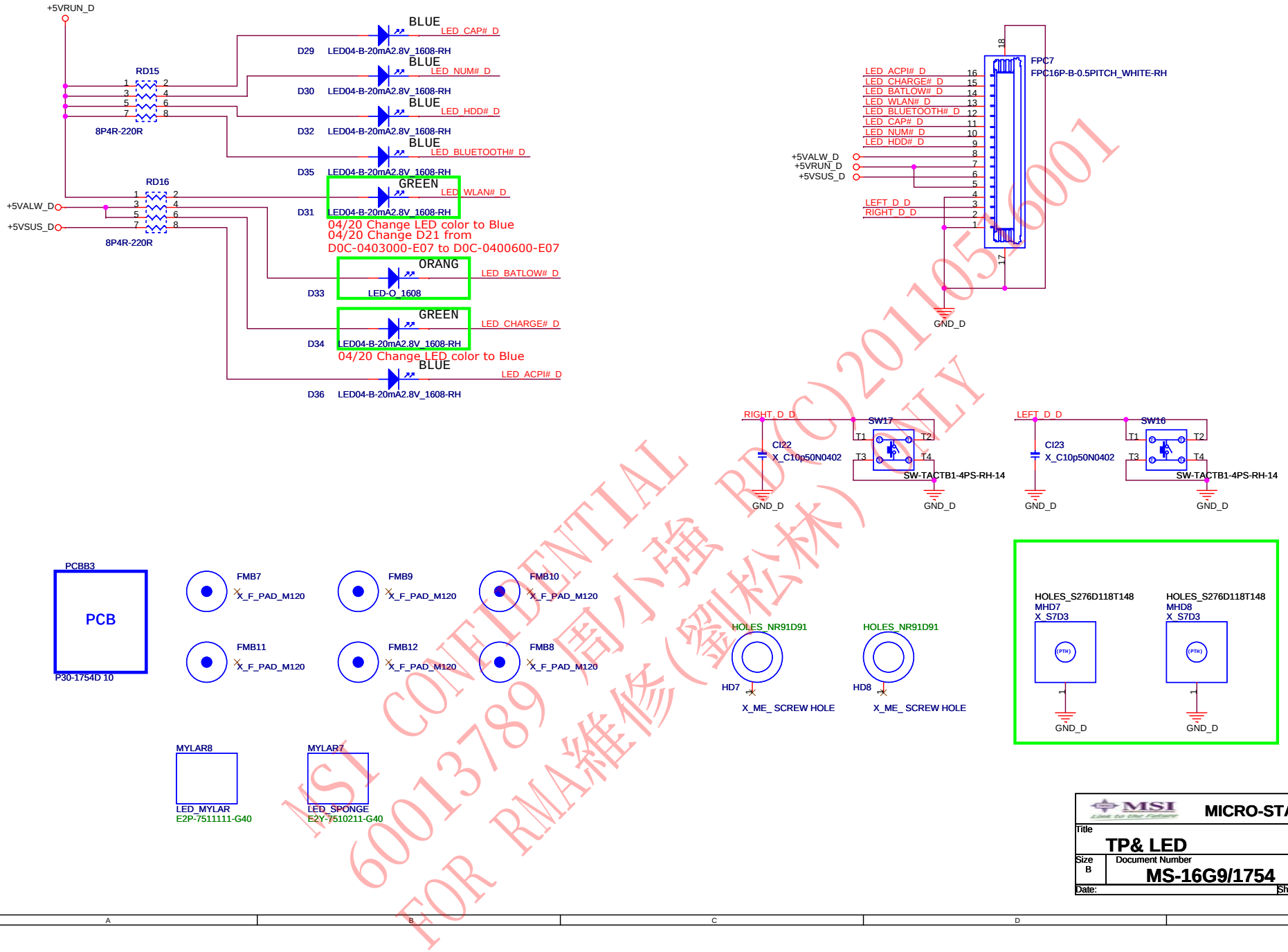
PCBC1
PCB
P30-1754C 10
P30-1754C10-H73

HOLES_8X8_D3MM_VIA8
MHC6_X_8x8
MHC5_X_8x8
02/10 Add 8 vias for EMI sugesstion

MYLAR18
FUNCTION_PCB_Mylar
E2M-7511611-G40
MYLAR17
FUNCTION_LED_Mylar
E2Y-7511911-G40

FMC14 X_F_PAD_M120
FMC12 X_F_PAD_M120
FMC13 X_F_PAD_M120
FMC10 X_F_PAD_M120
FMC5 X_F_PAD_M120

MICRO-STAR INT'L CO.,LTD.
Title: PWR_SW / LED
Size: B
Document Number: MS-16G9/1754
Rev: 10
Date:
Sheet 45 of 52

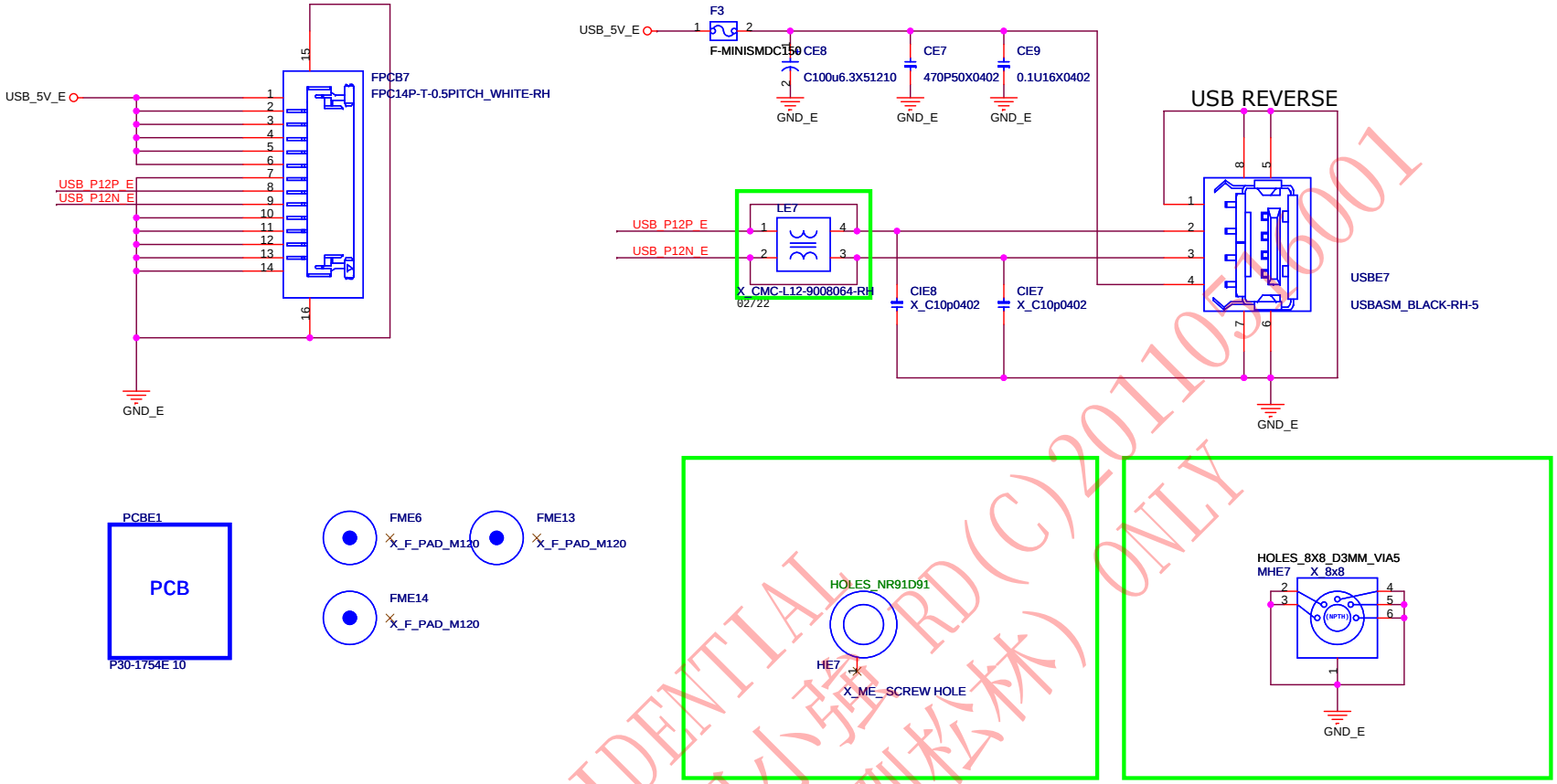


MSI MICRO-STAR INT'L CO.,LTD.

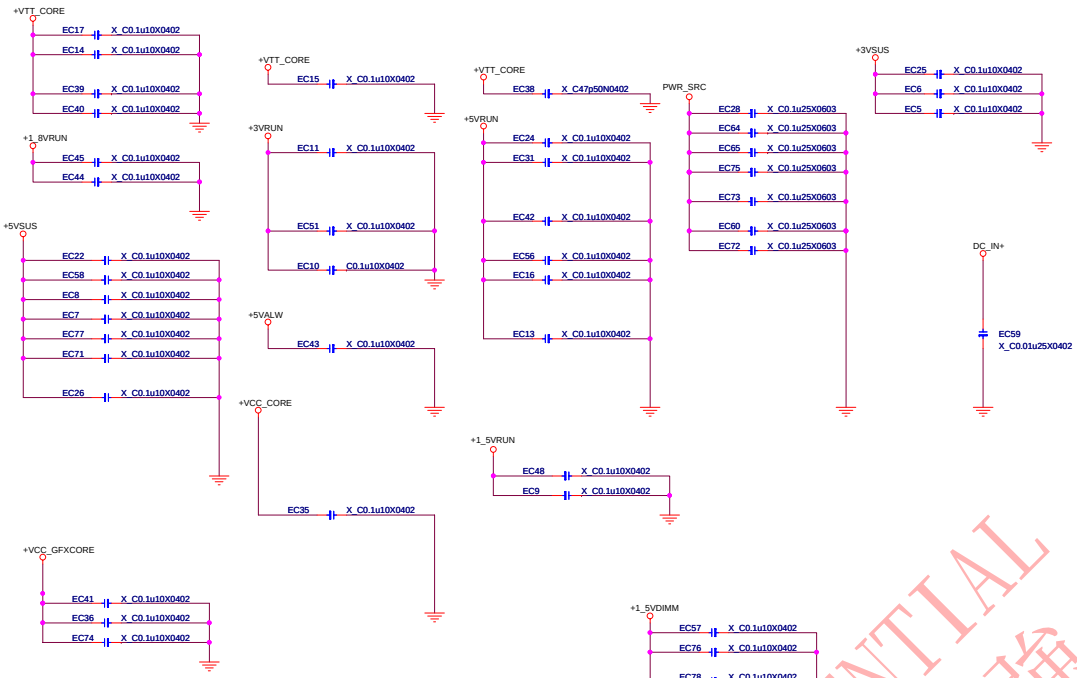
Title: TP& LED

Size: B | Document Number: MS-16G9/1754 | Rev: 10

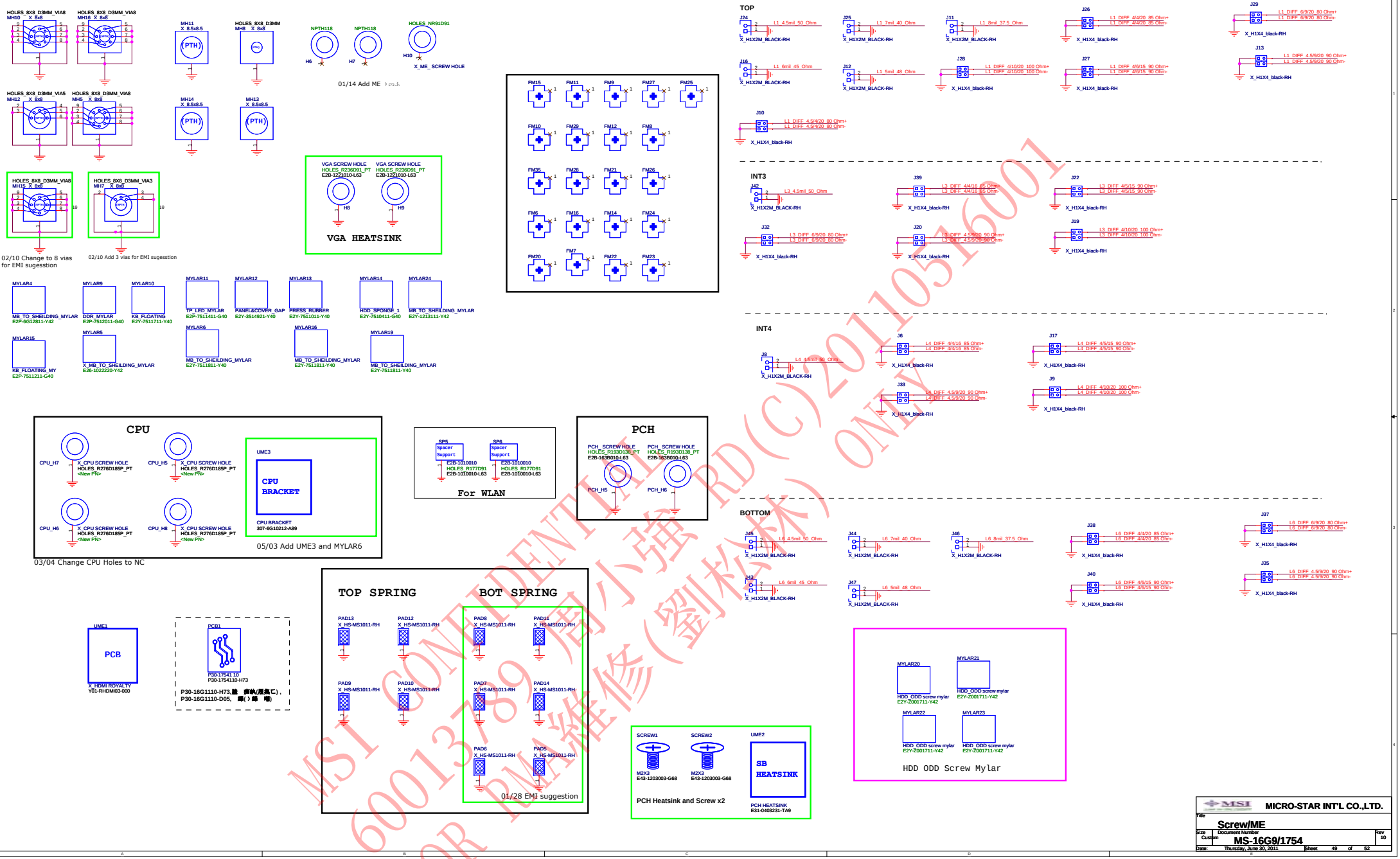
Date: | Sheet 46 of 52



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	[E] USB2.0 PORT	
Size B	Document Number MS-1754	Rev 10
Date: Thursday, June 30, 2011	Sheet 47 of 52	



MSI	MICRO-STAR INT'L CO.,LTD.	
Title: EMI		
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 48 of 52	

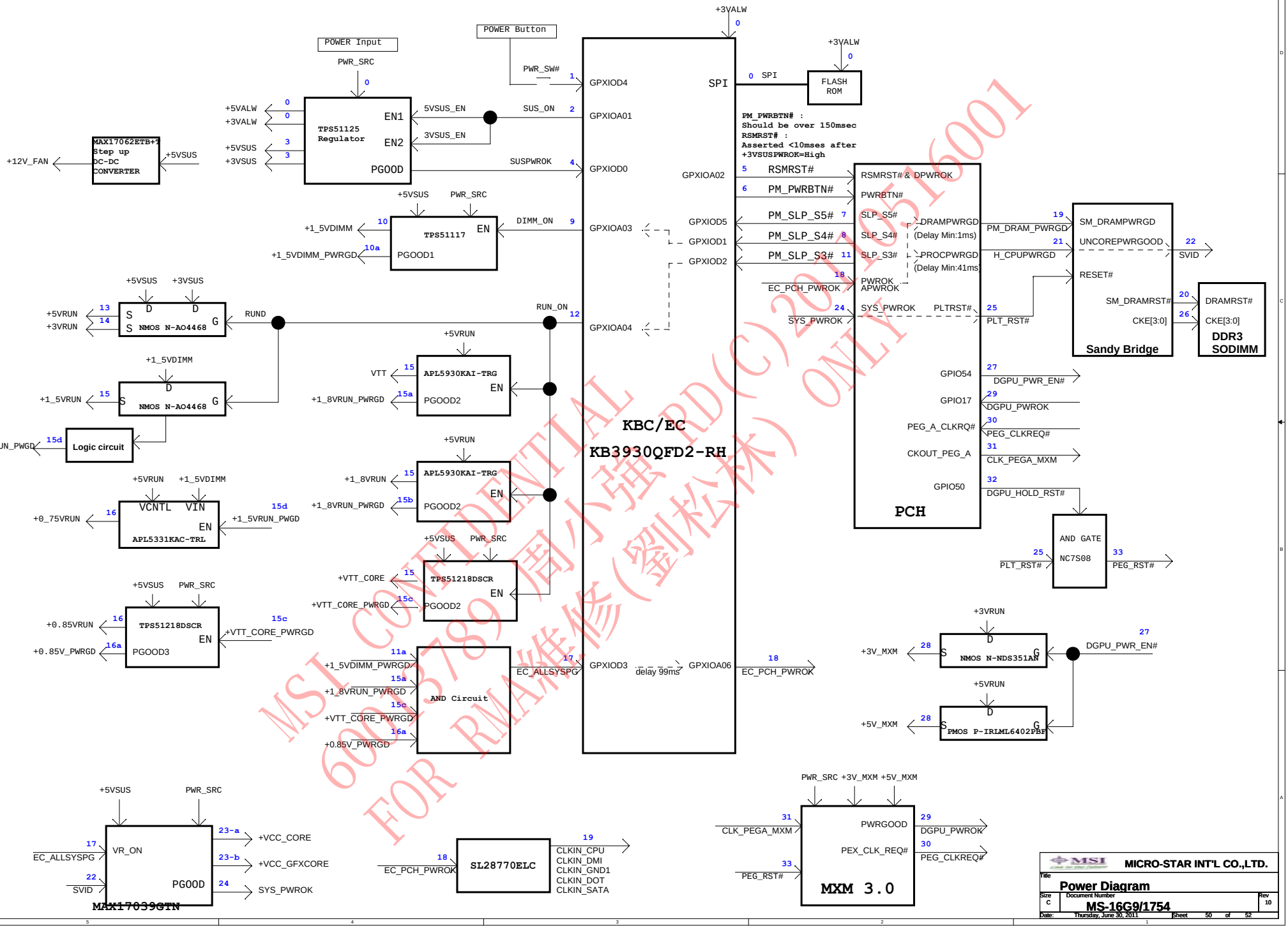


MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME

Size: Custom | Document Number: MS-16G9/1754 | Rev: 10

Date: Thursday, June 30, 2011 | Sheet 49 of 52



MICRO-STAR INT'L CO.,LTD.

Title: Power Diagram

Size: C | Document Number: MS-16G9/1754 | Rev: 10

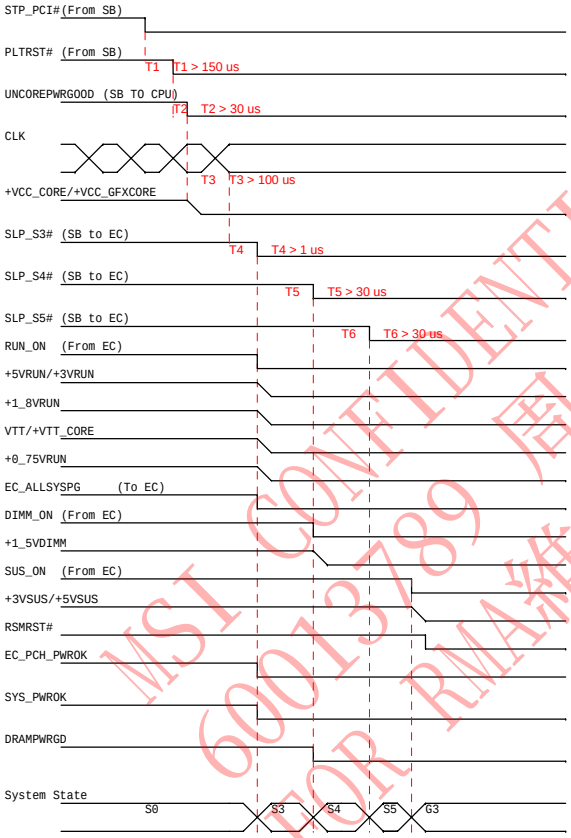
Date: Thursday, June 30, 2011 | Sheet 50 of 52

Power down Sequence DC mode S0 to G3

S0-S5

EC programming timing

Intel Huron River timing SPEC

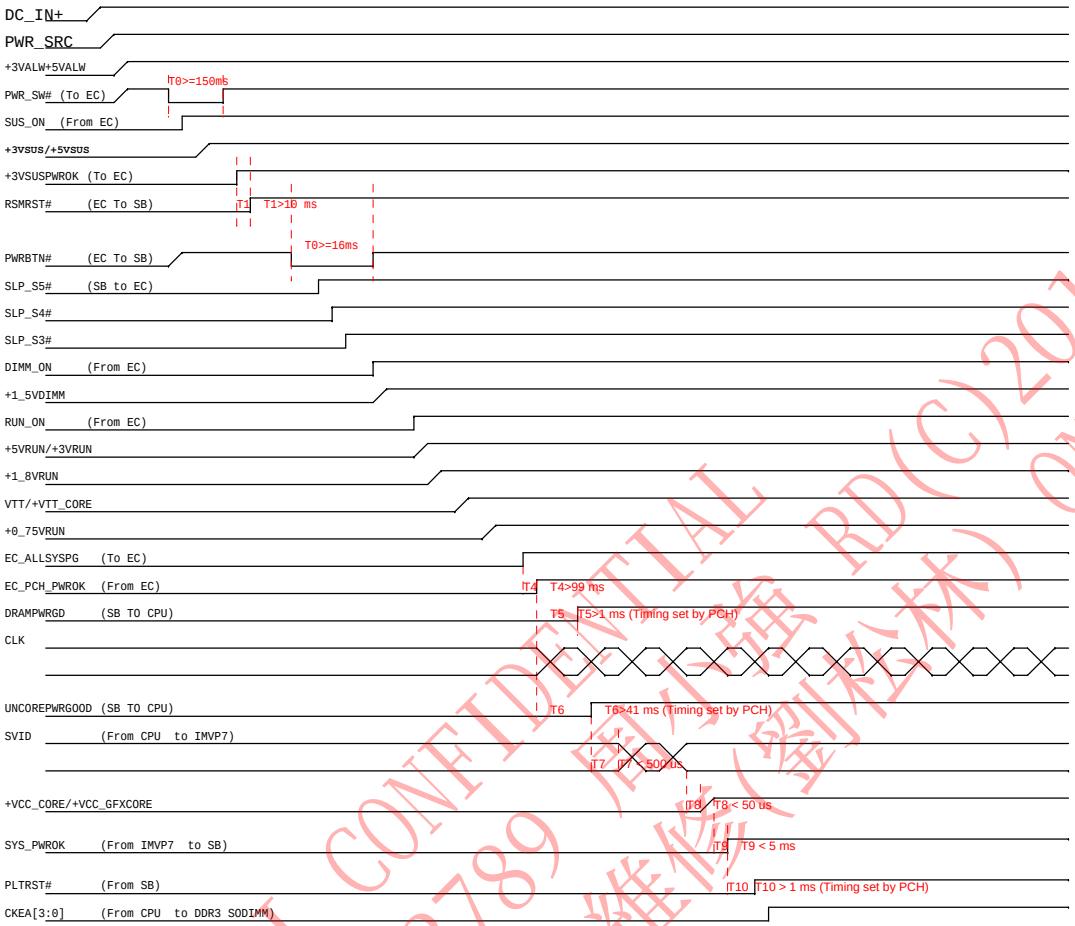


MSI	MICRO-STAR INT'L CO.,LTD.	
Title: Power Down Sequency		
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 51 of 52	

S5-S0

EC programming timing

Intel Huron River timing SPEC



MSI Link to the Future	MICRO-STAR INT'L CO.,LTD.	
Title: Power on Sequency		
Size: Custom	Document Number: MS-16G9/1754	Rev: 10
Date: Thursday, June 30, 2011	Sheet 52 of 52	