Table of Contents

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

<Core Design>

Title: Table of Contents

<OrgAddr1>

Engineer:

Size	Project Name	Rev
A3	CHARIOT	1.00

Date: Thursday, June 25, 2015 Sheet 1 of 76

Schematics Change History

Version	Date	Comments

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

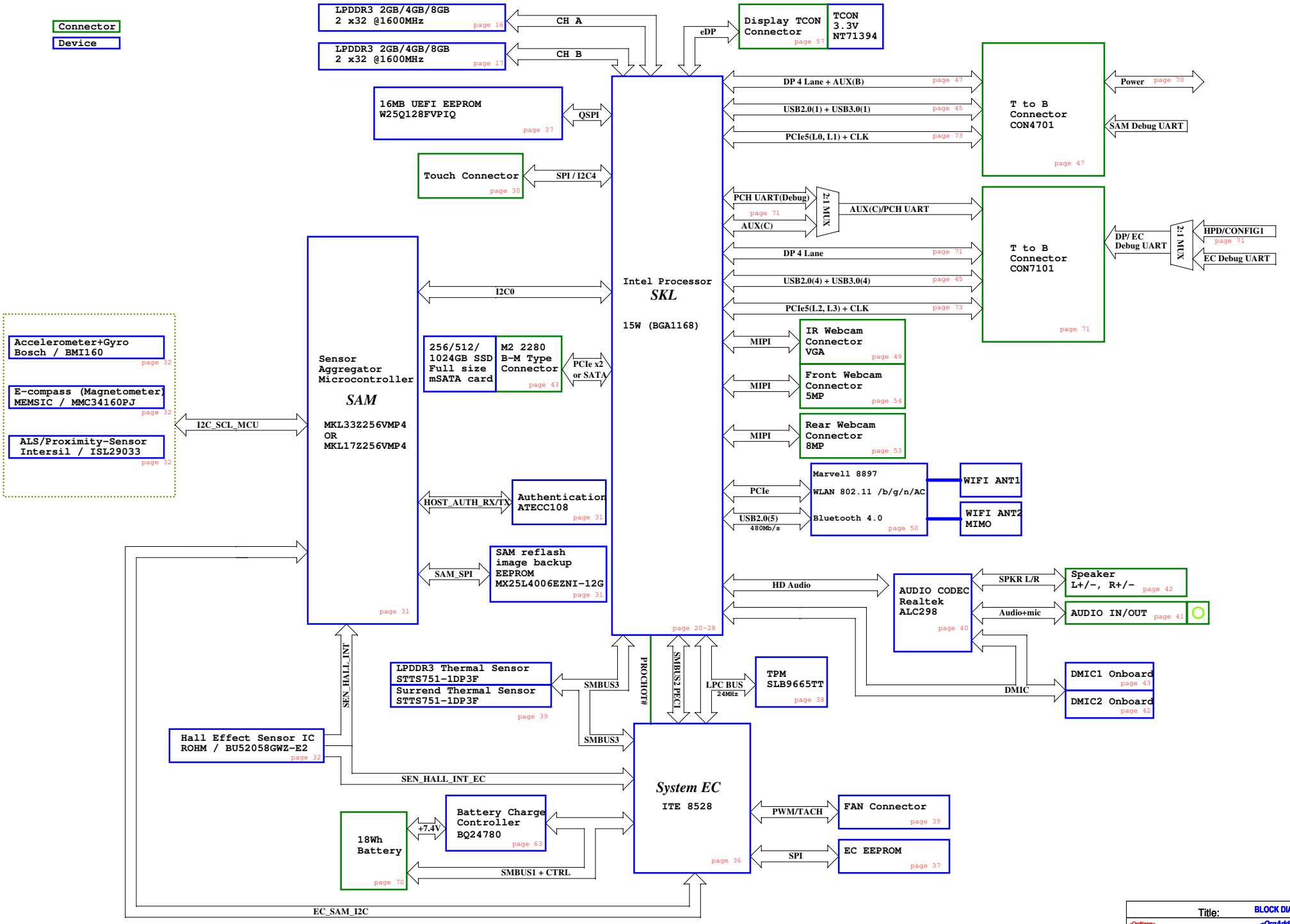
Property: BOM
I = Installed Part.
NI = Not Installed Part.

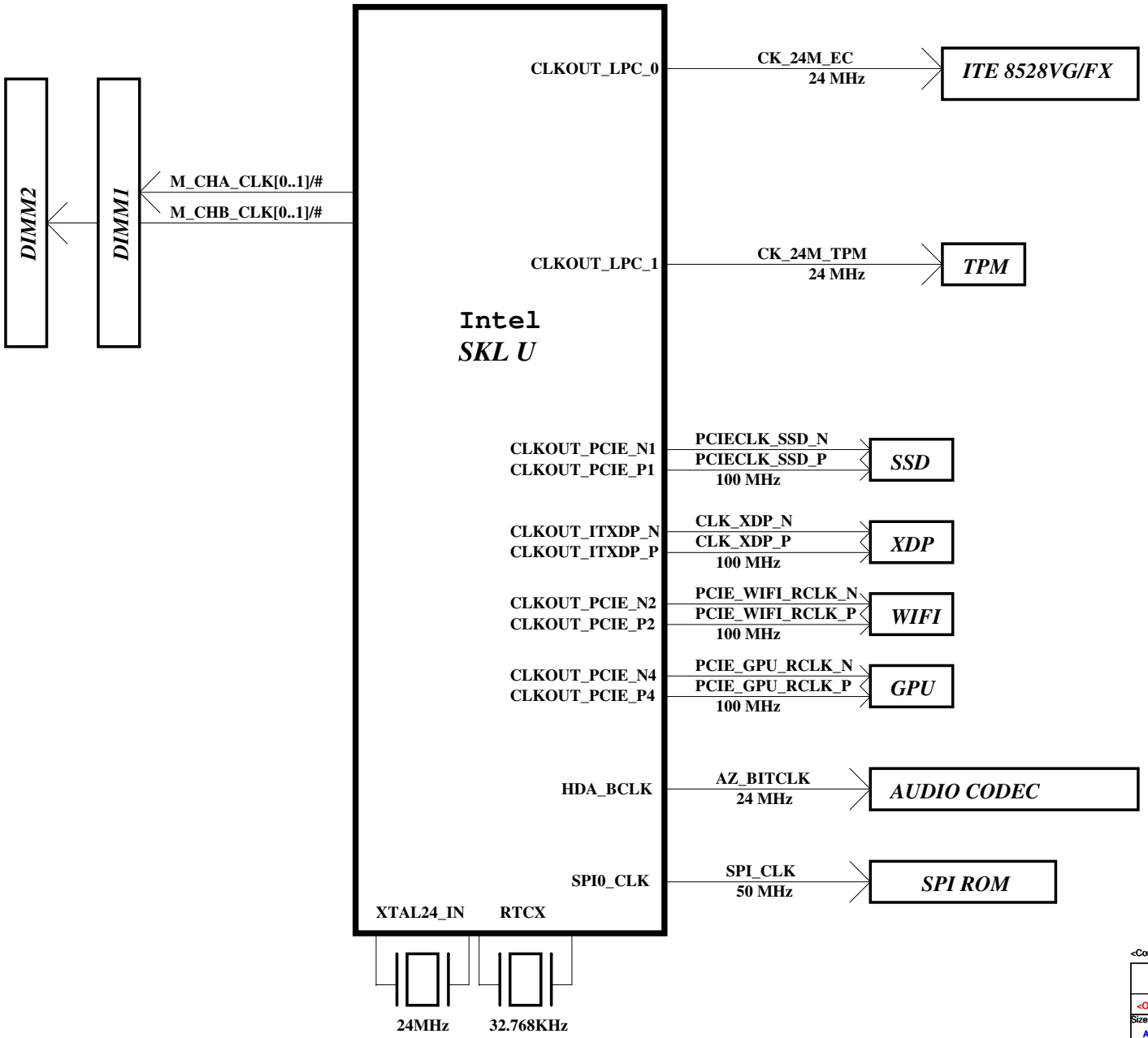
PROTO = PROTO Phase Only.
VP = Virtual Part.

MP = MPNI
S = Short after design fixed
XDP = Parts only for XDP

<Core Design>

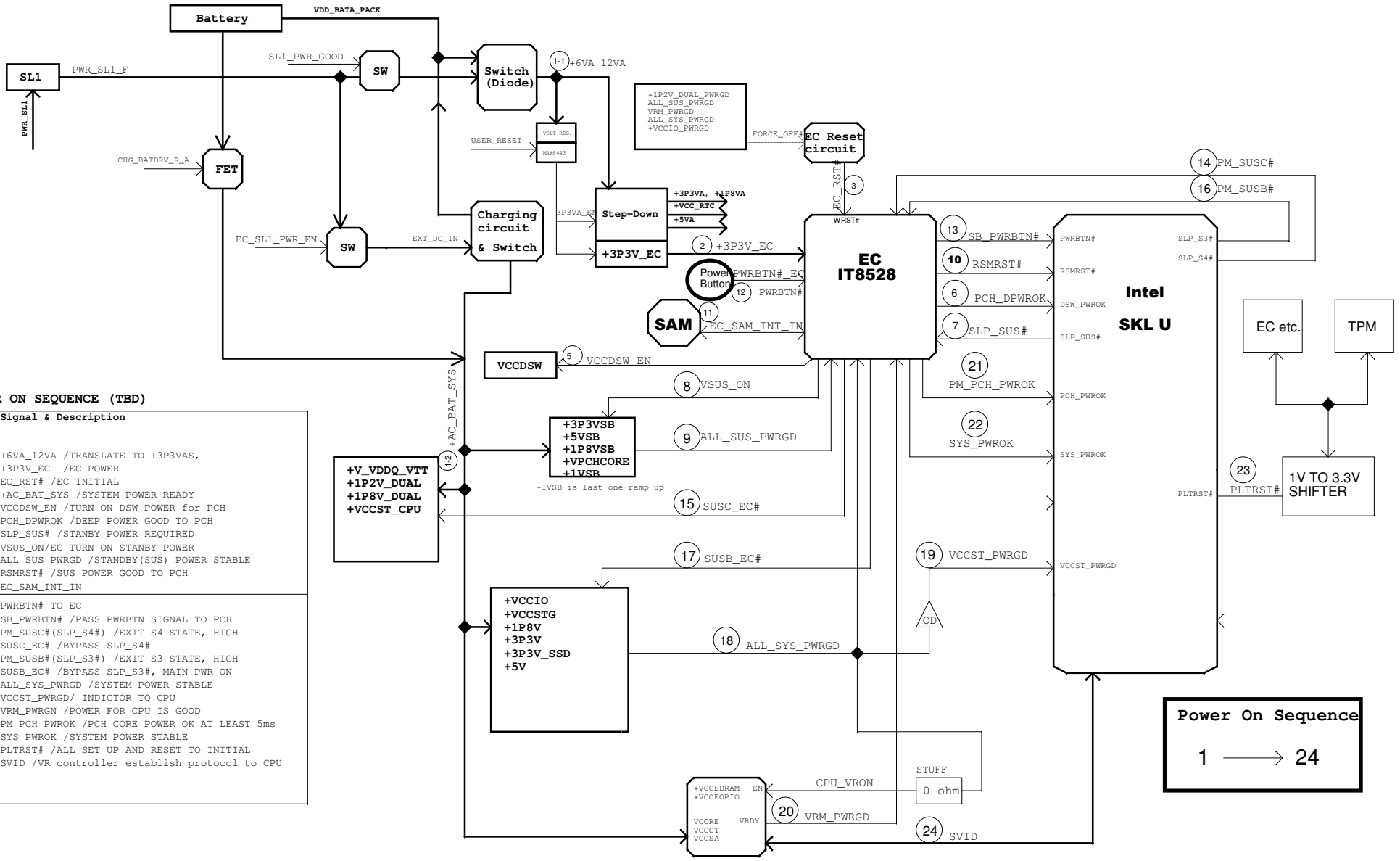
Title: CHANGE HISTORY-2
Engineer: <OrgAddr1>
Size: A3 | Project Name: CHARIOT | Rev: 1.00
Date: Thursday, June 25, 2015 | Sheet 2 of 76


Connector
Device
LPDDR3 2GB/4GB/8GB
2 x32 @1600MHz
page 16
CH A
LPDDR3 2GB/4GB/8GB
2 x32 @1600MHz
page 17
CH B
eDP
Display TCON
Connector
page 57
TCON
3.3V
NT71394
16MB UEFI EEPROM
W25Q128FVPIQ
page 37
QSPI
Touch Connector
page 30
SPI / I2C4
DP 4 Lane + AUX(B)
page 47
USB2.0(1) + USB3.0(1)
page 45
PCIe5(L0, L1) + CLK
page 73
T to B
Connector
CON4701
page 47
Power
page 70
SAM Debug UART
PCH UART(Debug)
page 71
AUX(C)
2:1 MUX
AUX(C)/PCH UART
DP 4 Lane
page 71
USB2.0(4) + USB3.0(4)
page 45
PCIe5(L2, L3) + CLK
page 73
T to B
Connector
CON7101
page 71
DP/ EC
Debug UART
2:1 MUX
HPD/CONFIG1
page 71
EC Debug UART
Intel Processor
SKL
15W (BGA1168)
page 20~28
I2C0
Sensor
Aggregator
Microcontroller
SAM
MKL33Z256VMP4
OR
MKL17Z256VMP4
page 31
Accelerometer+Gyro
Bosch / BMI160
page 32
E-compass (Magnetometer)
MEMSIC / MMC34160PJ
page 32
ALS/Proximity-Sensor
Intersil / ISL29033
page 32
I2C_SCL_MCU
256/512/
1024GB SSD
Full size
mSATA card
M2 2280
B-M Type
Connector
page 43
PCIe x2
or SATA
MIPI
IR Webcam
Connector
VGA
page 49
MIPI
Front Webcam
Connector
5MP
page 54
MIPI
Rear Webcam
Connector
8MP
page 53
HOST_AUTH_RX/TX
Authentication
ATECC108
page 31
PCIe
USB2.0(5)
480Mb/s
Marvell 8897
WLAN 802.11 /b/g/n/AC
Bluetooth 4.0
page 50
WIFI ANT1
WIFI ANT2
MIMO
SAM_SPI
SAM reflash
image backup
EEPROM
MX25L4006EZNI-12G
page 31
HD Audio
AUDIO CODEC
Realtek
ALC298
page 40
SPKR L/R
Speaker
L+/-, R+/-
page 42
Audio+mic
AUDIO IN/OUT
page 41
DMIC
DMIC1 Onboard
page 43
DMIC2 Onboard
page 42
SEN_HALL_INT
LPDDR3 Thermal Sensor
STTS751-1DP3F
Surrend Thermal Sensor
STTS751-1DP3F
page 39
SMBUS3
SMBUS3
#PROCHOT
SMBUS2 PECI
LPC BUS
24MHz
TPM
SLB9665TT
page 38
Hall Effect Sensor IC
ROHM / BU52058GWZ-E2
page 32
SEN_HALL_INT_EC
System EC
ITE 8528
page 36
PWM/TACH
FAN Connector
page 39
SPI
EC EEPROM
page 37
18Wh
Battery
page 70
+7.4V
Battery Charge
Controller
BQ24780
page 63
SMBUS1 + CTRL
EC_SAM_I2C
Title:
BLOCK DIAGRAM
<OrgName>
Engineer:
<OrgAddr1>
Size
Custom
Project Name
CHARIOT
Rev
1.00
Date:
Thursday, June 25, 2015
Sheet
3
of
76



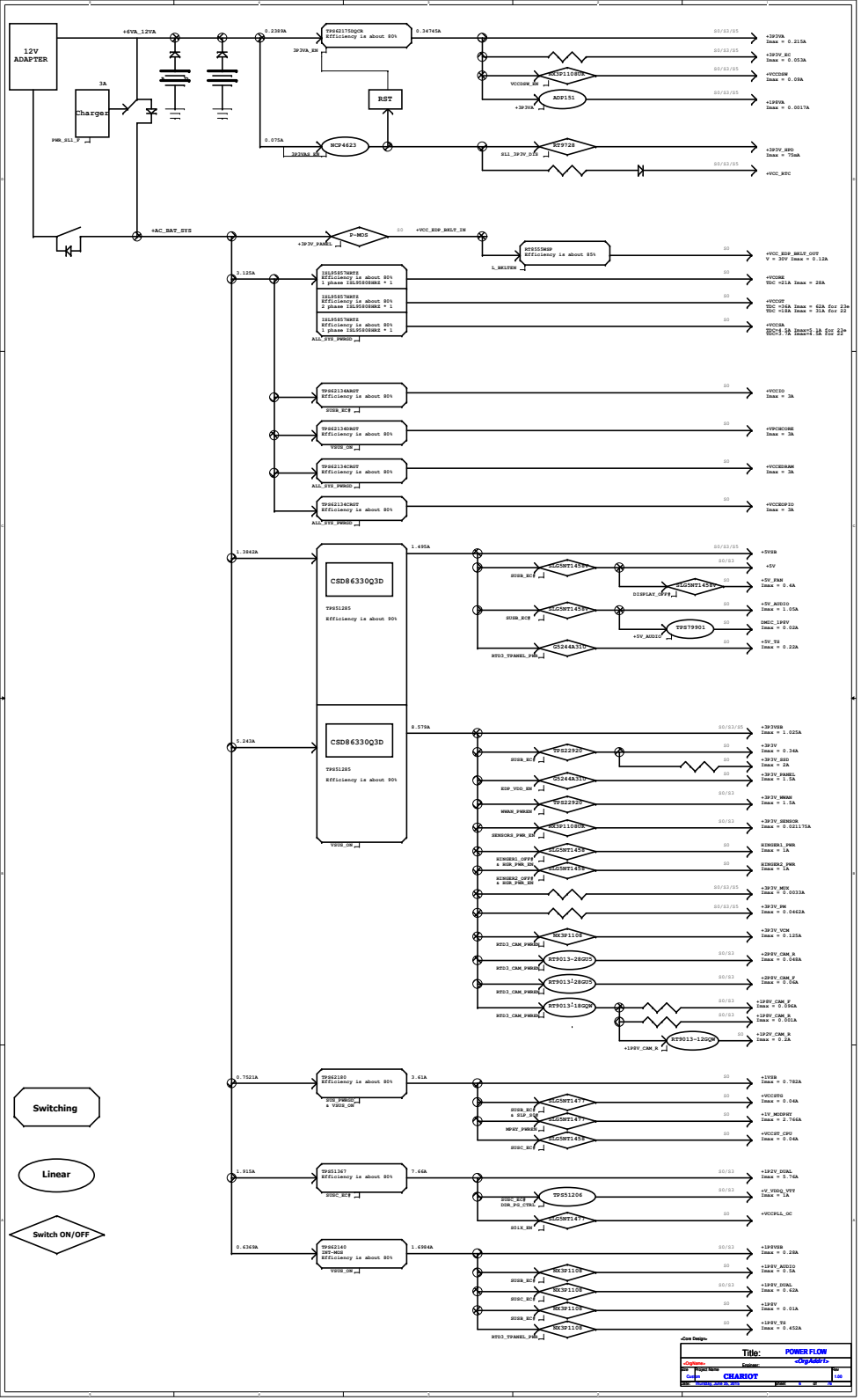
<Core Design>

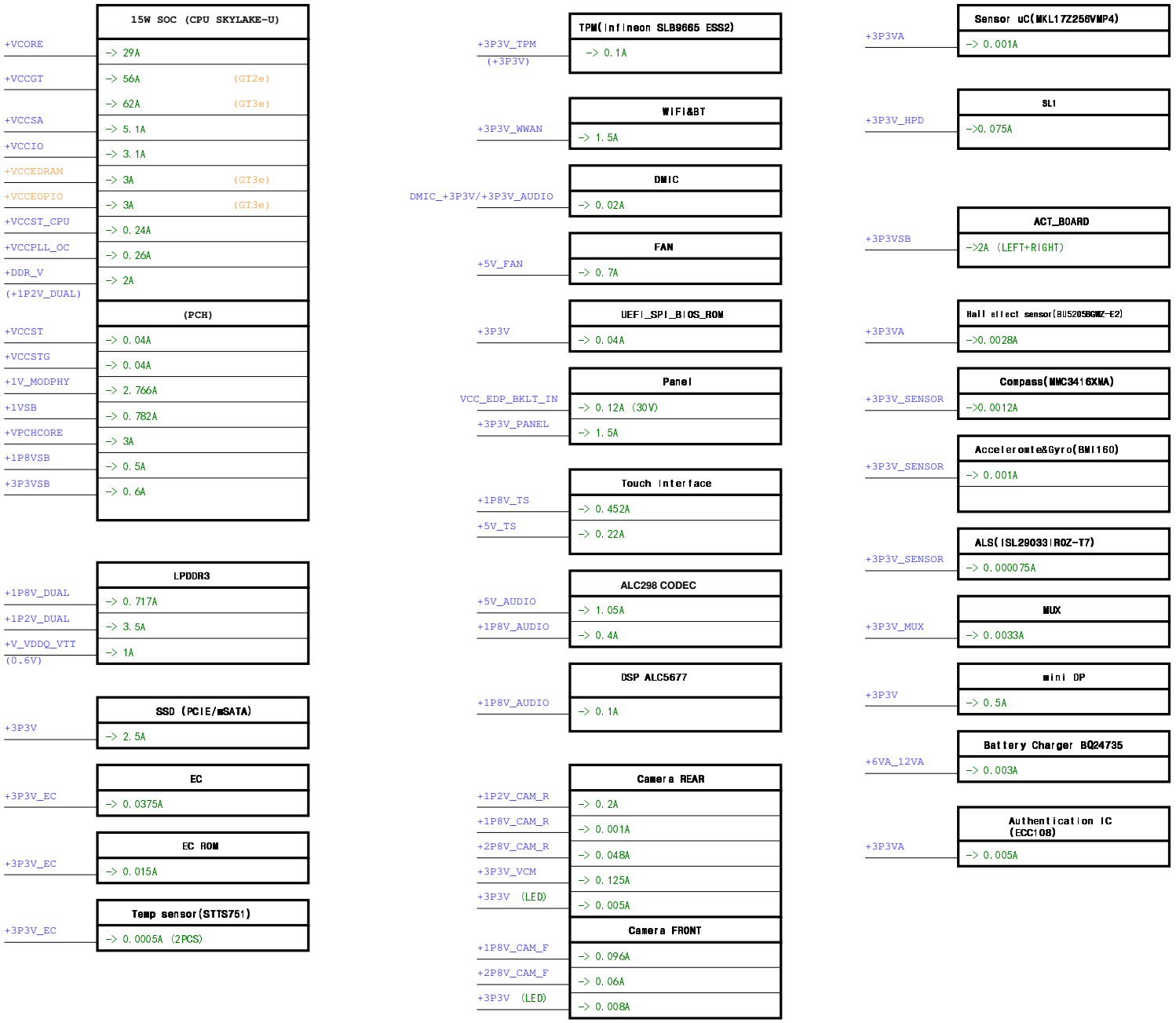
Title:	CLCOK DISTRIBUTION	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 4 of 76	



POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4.	+AC_BAT_SYS /SYSTEM POWER READY
5.	VCCDSW_EN /TURN ON DSW POWER for PCH
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	VSUS_ON/EC TURN ON STANBY POWER
9.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10.	RSMRST# /SUS POWER GOOD TO PCH
11.	EC_SAM_INT_IN
12	PWRBTN# TO EC
13.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14.	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15.	SUSC_EC# /BYPASS SLP_S4#
16.	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17.	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19.	VCCST_PWRGD/ INDICTOR TO CPU
20.	VRM_PWRGN /POWER FOR CPU IS GOOD
21.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22.	SYS_PWROK /SYSTEM POWER STABLE
23.	PLTRST# /ALL SET UP AND RESET TO INITIAL
24.	SVID /VR controller establish protocol to CPU


12V ADAPTER
+6VA_12VA
3A
Charger
PWR_SRC_P
0.2389A
TPS62175QDCR
Efficiency is about 90%
3P3VA_EN
0.3474A
RST
0.075A
RCP4623
3P3VAS_EN
+3P3VA
Imax = 0.215A
+3P3V_EC
Imax = 0.053A
+VCCDSW
Imax = 0.09A
+1P05A
Imax = 0.0017A
+3P3V_RTC
Imax = 75mA
+VCC_RTC
+AC_BAT_SYS
P-MOS
+3P3V_PMOS
+VCC_EDP_BKLT_IN
+VCC_EDP_BKLT_OUT
V = 30V Imax = 0.12A
3.125A
+VCORE
TDC =21A Imax = 28A
+VCCUT
TDC =34A Imax = 42A for 23w
TDC =18A Imax = 31A for 22
+VCCSA
TDC=4.5A Imax=5.1A for 23w
TDC=3.7A Imax=4.5A for 22
+VCCIO
Imax = 3A
+VPCHCORE
Imax = 3A
+VCCEDRAM
Imax = 3A
+VCCRCPIO
Imax = 3A
1.3842A
1.495A
CSD86330Q3D
TPS51285
Efficiency is about 90%
+5VSB
+5V
+5V_FAN
Imax = 0.4A
+5V_AUDIO
Imax = 1.05A
DMIC_1P85V
Imax = 0.02A
+5V_TS
Imax = 0.22A
0.243A
8.579A
+3P3VSB
Imax = 1.025A
+3P3V
Imax = 0.34A
+3P3V_SSD
Imax = 2A
+3P3V_PANEL
Imax = 1.5A
+3P3V_WWAN
Imax = 1.5A
+3P3V_SENSOR
Imax = 0.021175A
RINGER1_PWR
Imax = 1A
RINGER2_PWR
Imax = 1A
+3P3V_MIX
Imax = 0.0033A
+3P3V_PW
Imax = 0.0462A
+3P3V_VCM
Imax = 0.125A
+2P8V_CAM_R
Imax = 0.048A
+2P8V_CAM_F
Imax = 0.05A
+1P8V_CAM_F
Imax = 0.096A
+1P8V_CAM_R
Imax = 0.001A
+1P2V_CAM_R
Imax = 0.2A
0.7521A
3.41A
+1VSB
Imax = 0.782A
+VCCDTS
Imax = 0.04A
+1V_MODPHY
Imax = 2.744A
+VCCST_CPU
Imax = 0.04A
1.915A
7.66A
+1P2V_DDAL
Imax = 5.76A
+V_VDDQ_VTT
Imax = 1A
+VCCPLL_OC
0.6369A
1.6984A
+1P05VSB
Imax = 0.28A
+1P8V_AUDIO
Imax = 0.5A
+1P2V_DDAL
Imax = 0.42A
+1P8V
Imax = 0.01A
+1P8V_TS
Imax = 0.452A
Switching
Linear
Switch ON/OFF
Title: POWER FLOW
CHARIOT



<Core Design>

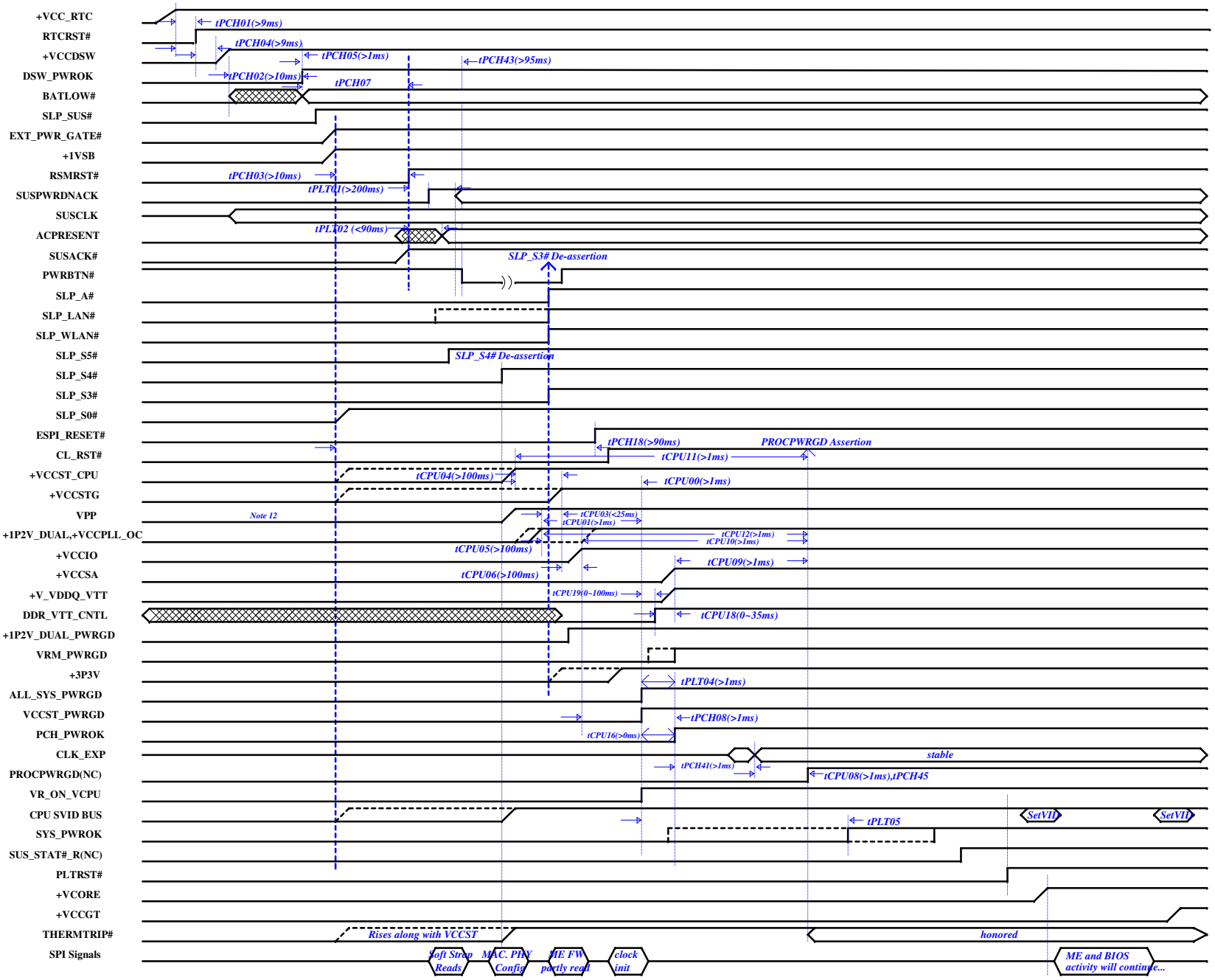
Title: POWER DISTRIBUTION

<OrgName> Engineer: <OrgAddr1>

Size: Custom | Project Name: CHARIOT | Rev: 1.00

Date: Thursday, June 25, 2015 | Sheet 7 of 76

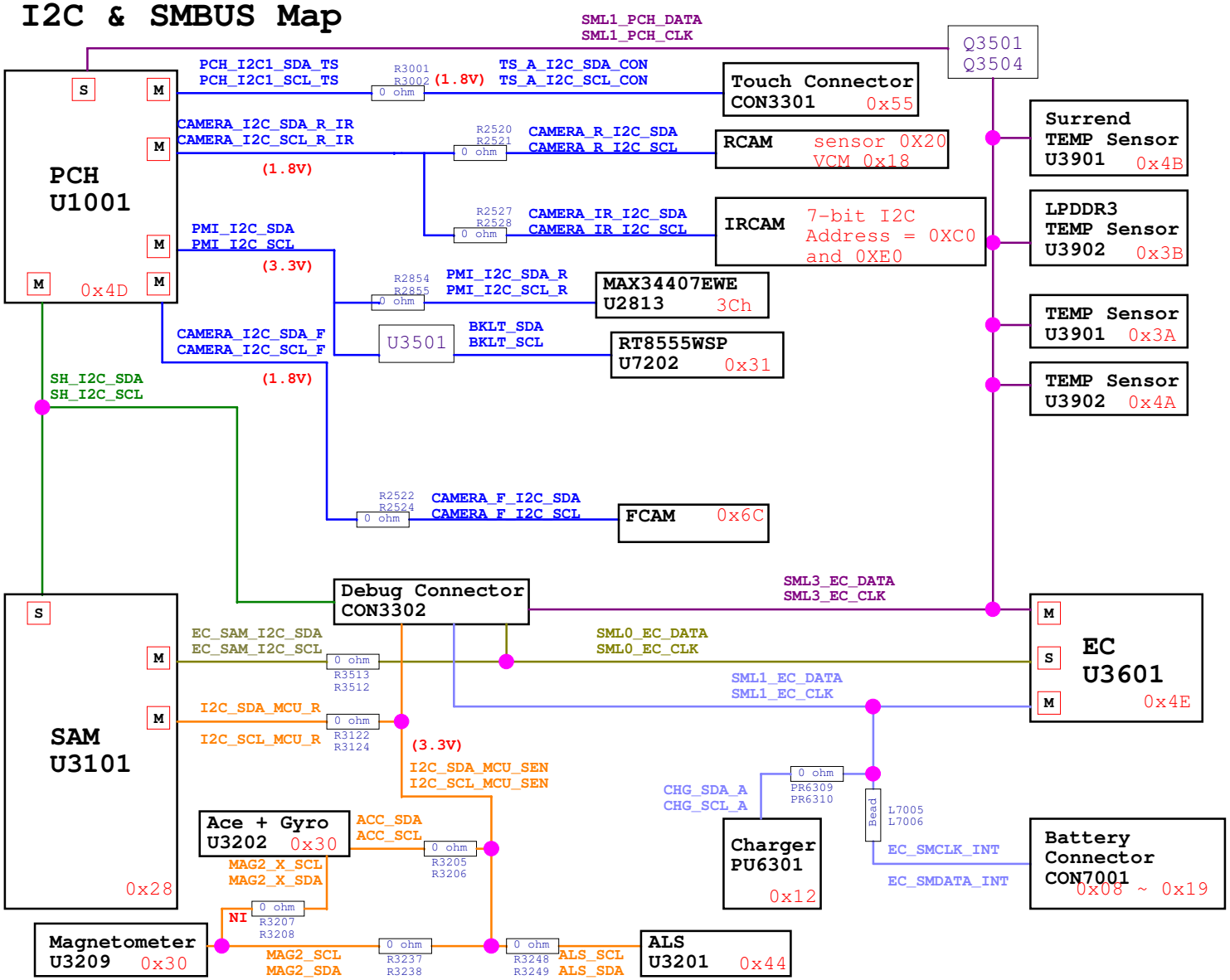
S5 to S0 Power Sequence



<Core Design>

Title:	POWER SEQUENCE	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 8 of 78	

I2C & SMBUS Map



Title:

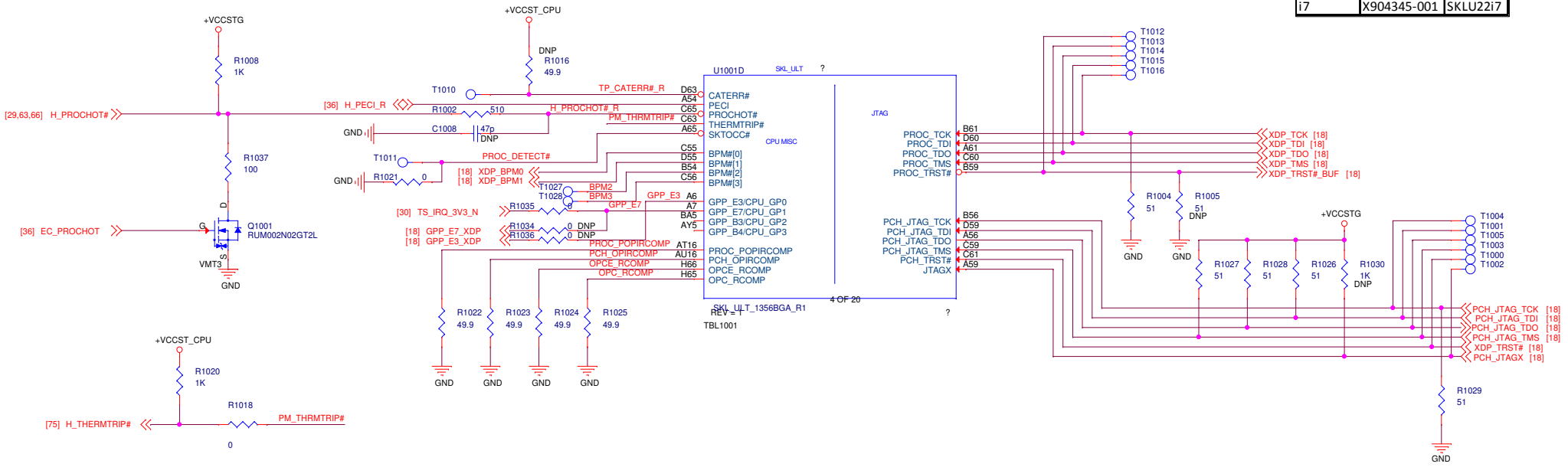
Engineer: <OrgAddr1>

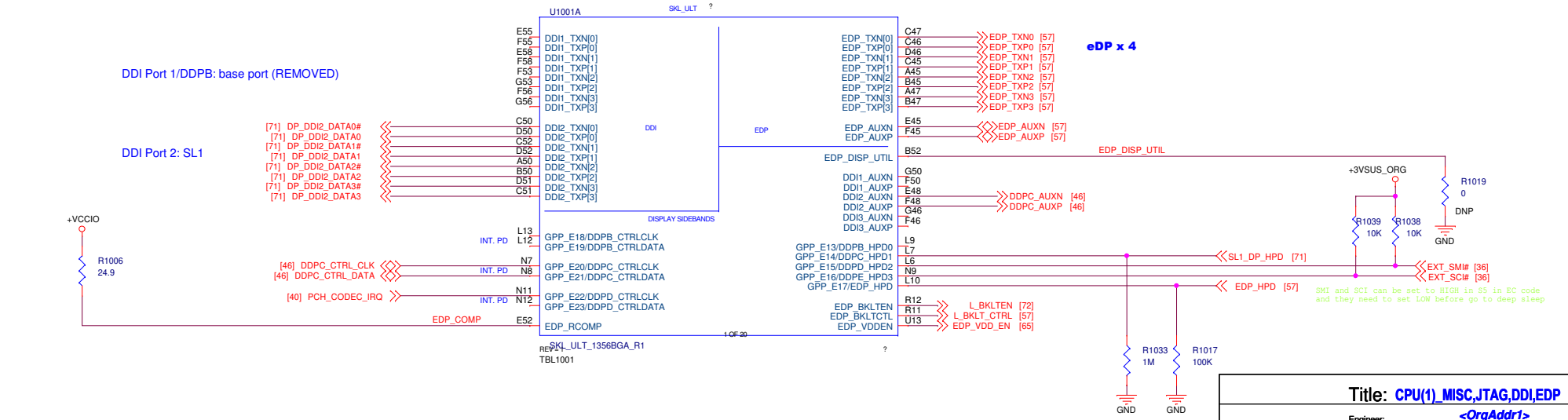
Size	Project Name	Rev
A2	CHARIOT	1.00

Date: Thursday, June 25, 2015 Sheet 9 of 76

TBL1001

CPU	MSPN	Intel PN
i3	X904344-001	SKLU22i3
i5	X904343-001	SKLU22i5
i7	X904345-001	SKLU22i7



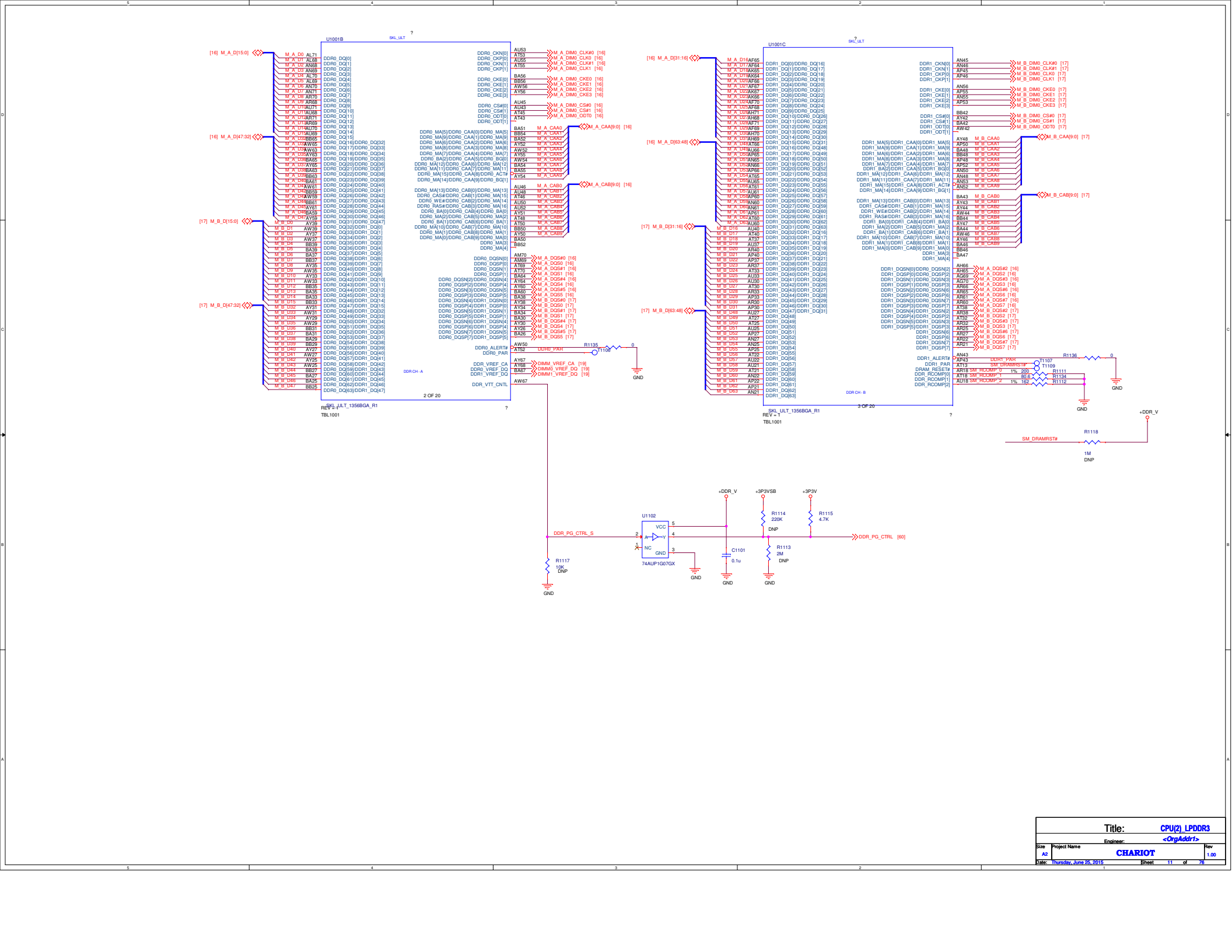


Title: CPU(1)_MISC,JTAG,DDI,EDP

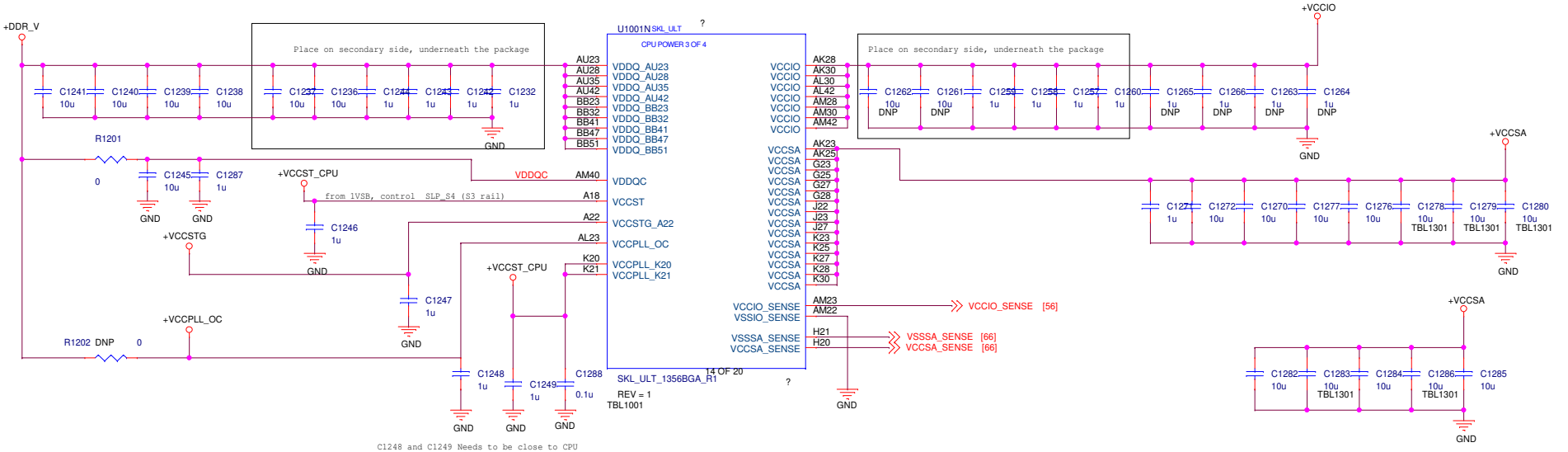
Engineer: <OrgAddr1>

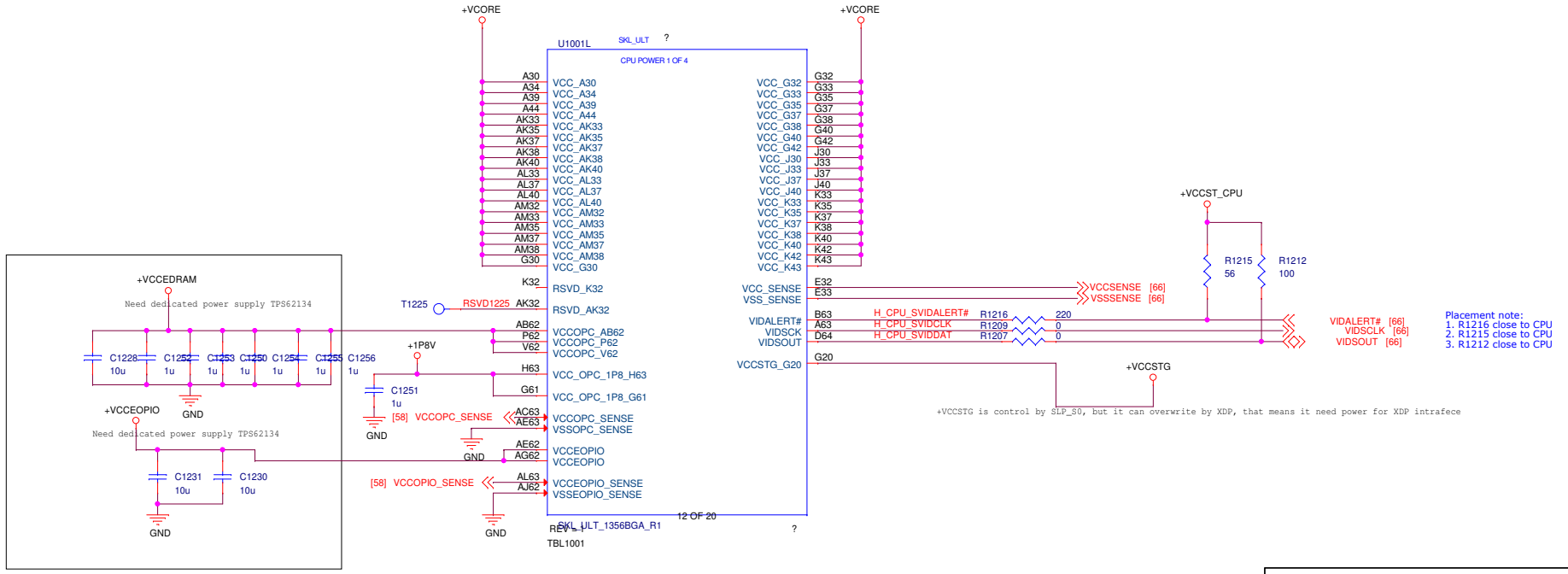
Size	Project Name	Rev
A3	CHARIOT	1.00

Date: Thursday, June 25, 2015 Sheet 10 of 76



Title:	CPU(2)_LPDDR3		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 11 of 76		



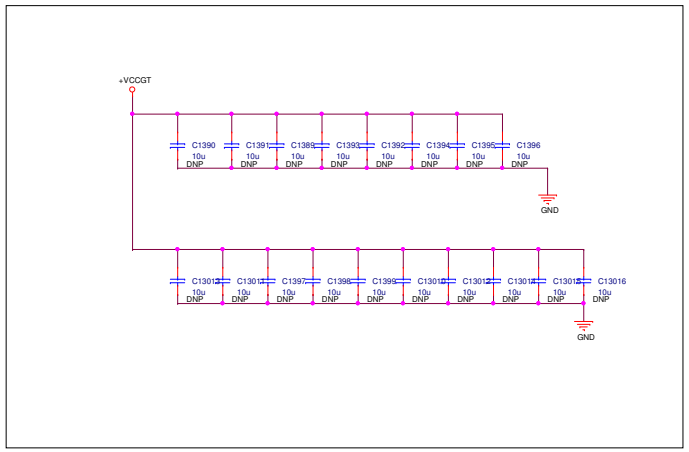


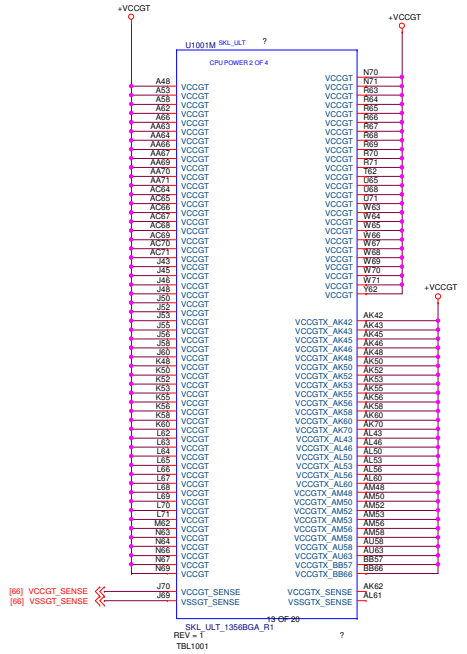
No Install all of parts in this block when use GT2

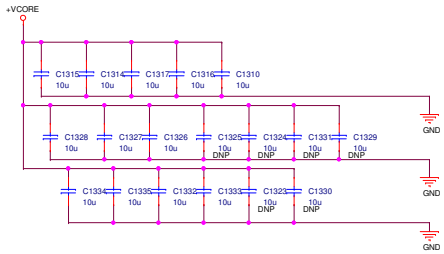
Title:	CPU(3)_SKL POWER1	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 12 of 76	

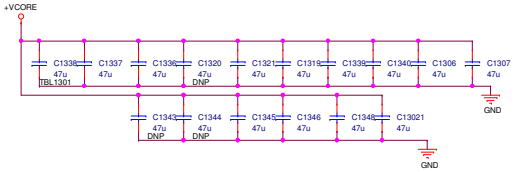
TBL1301

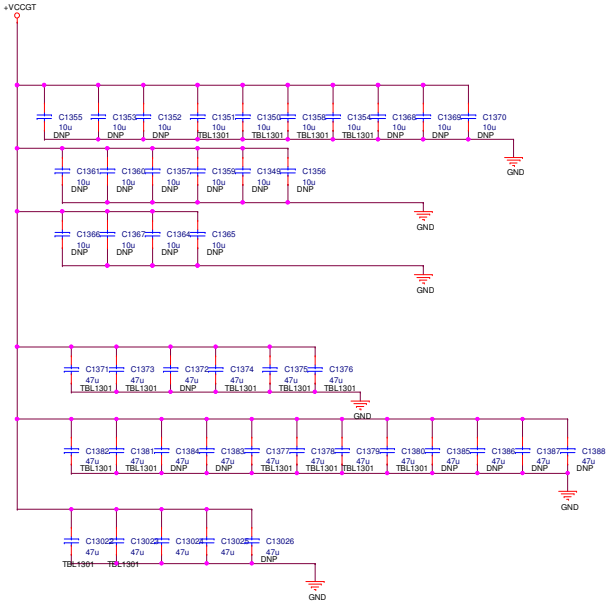
	GT2	GT3	Value	MSPN
C1338	No Stuff	Stuff	47uF	X904636-001
C1351	No Stuff	Stuff	10uF	X857759-001
C13023	No Stuff	Stuff	47uF	X904636-001
C1373	No Stuff	Stuff	47uF	X904636-001
C13022	No Stuff	Stuff	47uF	X904636-001
C1377	No Stuff	Stuff	47uF	X904636-001
C1378	No Stuff	Stuff	47uF	X904636-001
C1379	No Stuff	Stuff	47uF	X904636-001
C6869	No Stuff	Stuff	220uF	X907228-001
C1358	Stuff	No Stuff	10uF	X857759-001
C1354	Stuff	No Stuff	10uF	X857759-001
C1350	Stuff	No Stuff	10uF	X857759-001
C1371	No Stuff	Stuff	47uF	X904636-001
C1374	No Stuff	Stuff	47uF	X904636-002
C1375	No Stuff	Stuff	47uF	X904636-003
C1376	No Stuff	Stuff	47uF	X904636-004
C1380	No Stuff	Stuff	47uF	X904636-005
C1381	No Stuff	Stuff	47uF	X904636-006
C1382	No Stuff	Stuff	47uF	X904636-007
C1278	No Stuff	Stuff	10uF	X857759-001
C1279	No Stuff	Stuff	10uF	X857759-001
C1280	No Stuff	Stuff	10uF	X857759-001
C1283	No Stuff	Stuff	10uF	X857759-001
C1286	No Stuff	Stuff	10uF	X857759-001



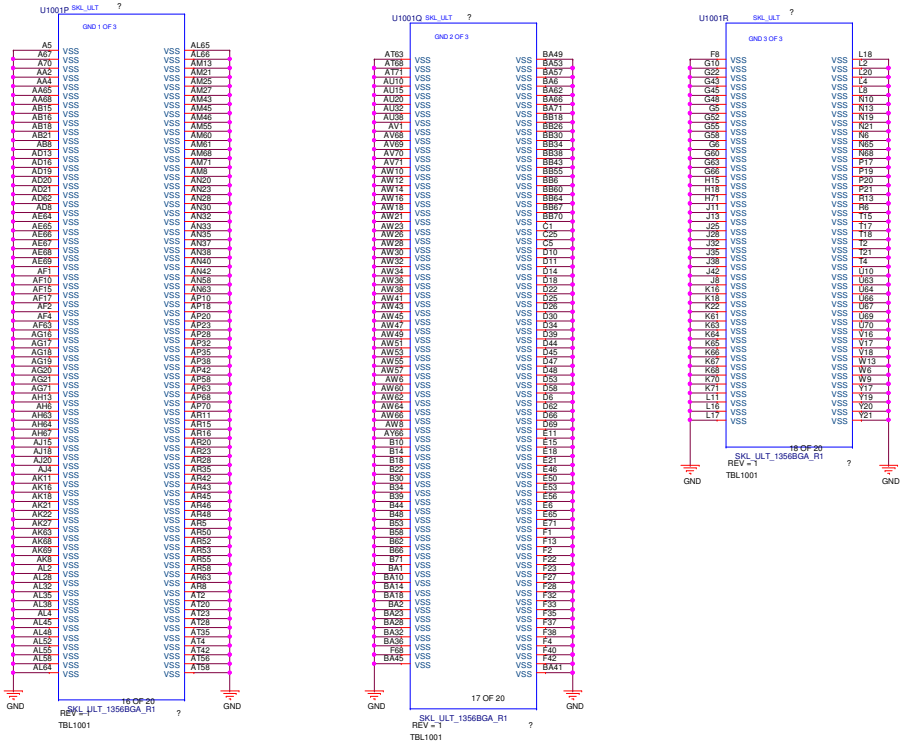




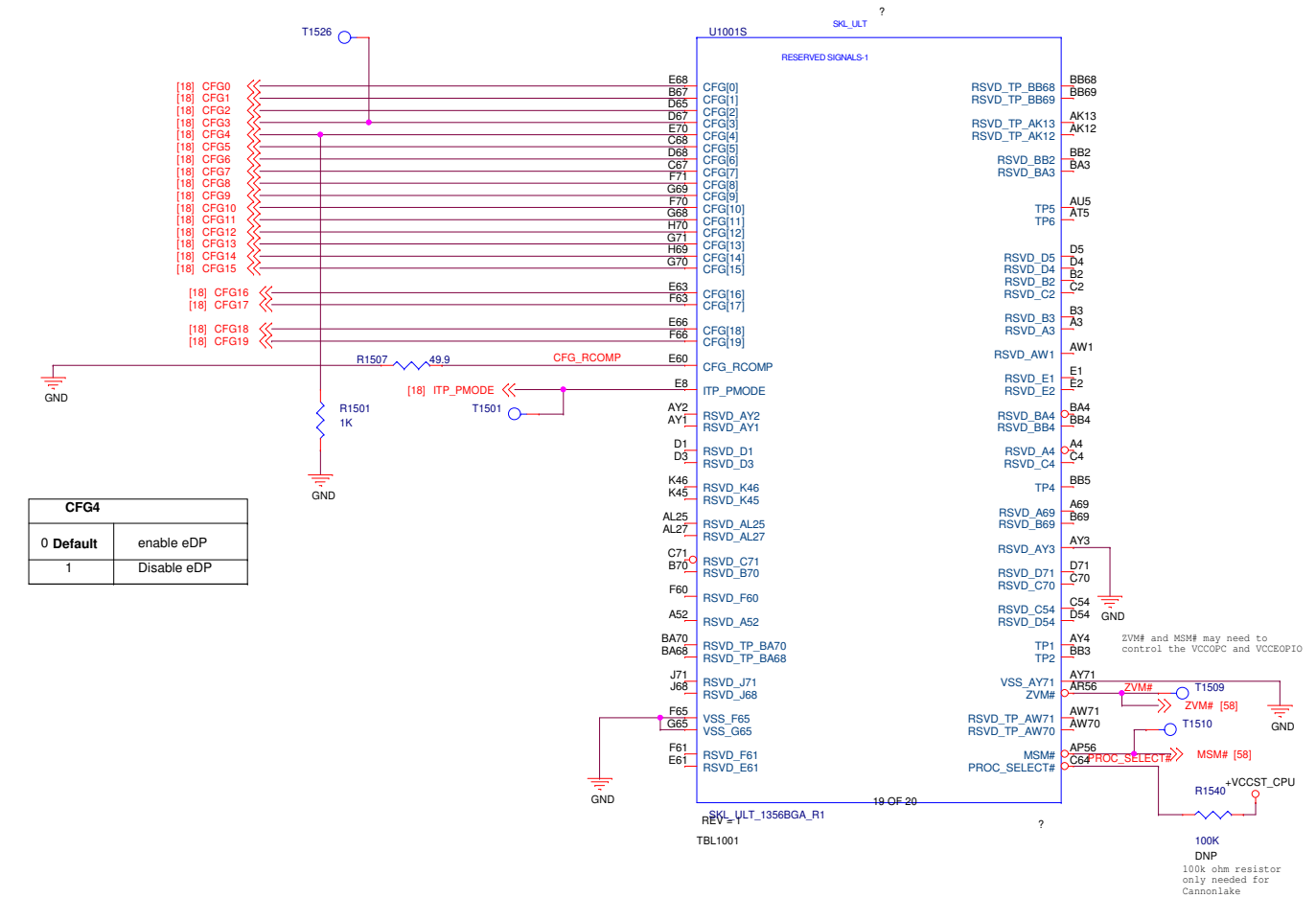




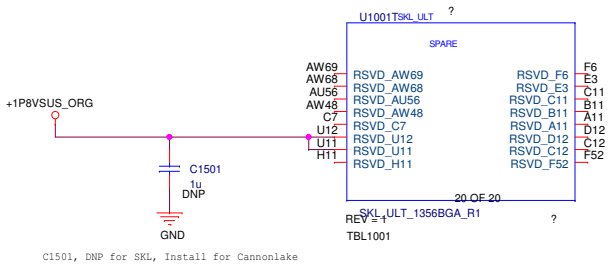
Title:	CPU(4)_SKL_POWER2	
Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 13 of 76	



Title:	CPU(5)_GND		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 14 of 76		

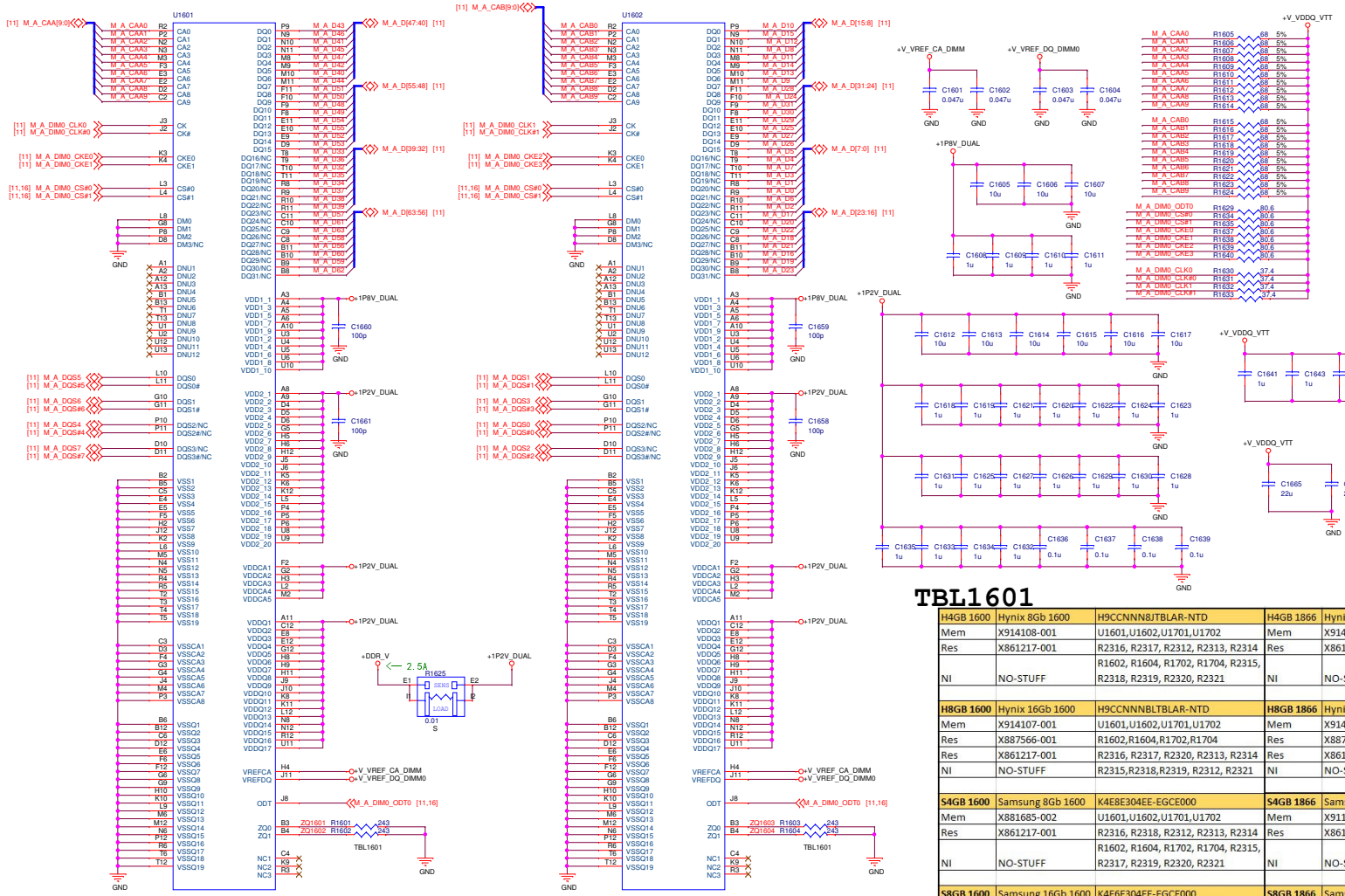


CFG4	
0 **Default**	enable eDP
1	Disable eDP



C1501, DNP for SKL, Install for Cannonlake

Title: CPU(6)_CFG_RESERVED			
Engineer: <OrgAddr1>			
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015		Sheet 15 of 76	



TBL1601

H4GB 1600	Hynix 8Gb 1600	H9CCNNN8JTBLAR-NTD	H4GB 1866	Hynix 8Gb 1866	H9CCNNN8JTBLAR-NUD
Mem	X914108-001	U1601,U1602,U1701,U1702	Mem	X914110-001	U1601,U1602,U1701,U1702
Res	X861217-001	R2316, R2317, R2312, R2313, R2314	Res	X861217-001	R2316, R2317, R2312, R2313, R2321
NI	NO-STUFF	R1602, R1604, R1702, R1704, R2315, R2318, R2319, R2320, R2321	NI	NO-STUFF	R1602, R1604, R1702, R1704, R2315, R2318, R2319, R2320, R2314
H8GB 1600	Hynix 16Gb 1600	H9CCNNNBLTBLAR-NTD	**H8GB 1866**	Hynix 16Gb 1866	H9CCNNNBLTBLAR-NUD
Mem	X914107-001	U1601,U1602,U1701,U1702	Mem	X914109-001	U1601,U1602,U1701,U1702
Res	X887566-001	R1602,R1604,R1702,R1704	Res	X887566-001	R1602,R1604,R1702,R1704
Res	X861217-001	R2316, R2317, R2320, R2313, R2314	Res	X861217-001	R2316, R2317, R2320, R2313, R2321
NI	NO-STUFF	R2315,R2318,R2319, R2312, R2321	NI	NO-STUFF	R2315,R2318,R2319, R2312, R2314
S4GB 1600	Samsung 8Gb 1600	K4E8E304EE-EGCE000	**S4GB 1866**	Samsung 8Gb 1866	K4E8E304EE-EGCF
Mem	X881685-002	U1601,U1602,U1701,U1702	Mem	X911501-001	U1601,U1602,U1701,U1702
Res	X861217-001	R2316, R2318, R2312, R2313, R2314	Res	X861217-001	R2316, R2318, R2312, R2313, R2321
NI	NO-STUFF	R1602, R1604, R1702, R1704, R2315, R2317, R2319, R2320, R2321	NI	NO-STUFF	R1602, R1604, R1702, R1704, R2315, R2317, R2319, R2320, R2314
S8GB 1600	Samsung 16Gb 1600	K4E6E304EE-EGCE000	**S8GB 1866**	Samsung 16Gb 1866	K4E6E304EE-EGCF
Mem	X889890-002	U1601,U1602,U1701,U1702	Mem	X911503-001	U1601,U1602,U1701,U1702
Res	X887566-001	R1602,R1604,R1702,R1704	Res	X887566-001	R1602,R1604,R1702,R1704
Res	X861217-001	R2316, R2318, R2320, R2313, R2314	Res	X861217-001	R2316, R2318, R2320, R2313, R2321
NI	NO-STUFF	R2315,R2317,R2319, R2312, R2321	NI	NO-STUFF	R2315,R2317,R2319, R2312, R2314
S16GB 1600	Samsung 32Gb 1600	K4EBE304EB-EGCE	**S16GB 1866**	Samsung 32Gb 1866	K4EBE304EB-EGCF
Mem		U1601,U1602,U1701,U1702	Mem	X930118-001	U1601,U1602,U1701,U1702
Res	X887566-001	R1602,R1604,R1702,R1704	Res	X887566-001	R1602,R1604,R1702,R1704
Res	X861217-001	R2316, R2318, R2312, R2319, R2314	Res	X861217-001	R2316, R2318, R2312, R2319, R2321
NI	NO-STUFF	R2315,R2317,R2320, R2313, R2321	NI	NO-STUFF	R2315,R2317,R2320, R2313, R2314
H16GB 1600	Hynix 32Gb 1600	H9CCNNNCLTMLAR-NTD	**H16GB 1866**	Hynix 32Gb 1866	H9CCNNNCLTMLAR-NUD
Mem		U1601,U1602,U1701,U1702	Mem	X934241-001	U1601,U1602,U1701,U1702
Res	X887566-001	R1602,R1604,R1702,R1704	Res	X887566-001	R1602,R1604,R1702,R1704
Res	X861217-001	R2316, R2317, R2312, R2319, R2314	Res	X861217-001	R2316, R2317, R2312, R2319, R2321
NI	NO-STUFF	R2315,R2318,R2320, R2313, R2321	NI	NO-STUFF	R2315,R2318,R2320, R2313, R2314

R1602 & R1604

8Gb/4GB	NC
16Gb/8GB	Install
32Gb/16GB	Install

(PCH side)

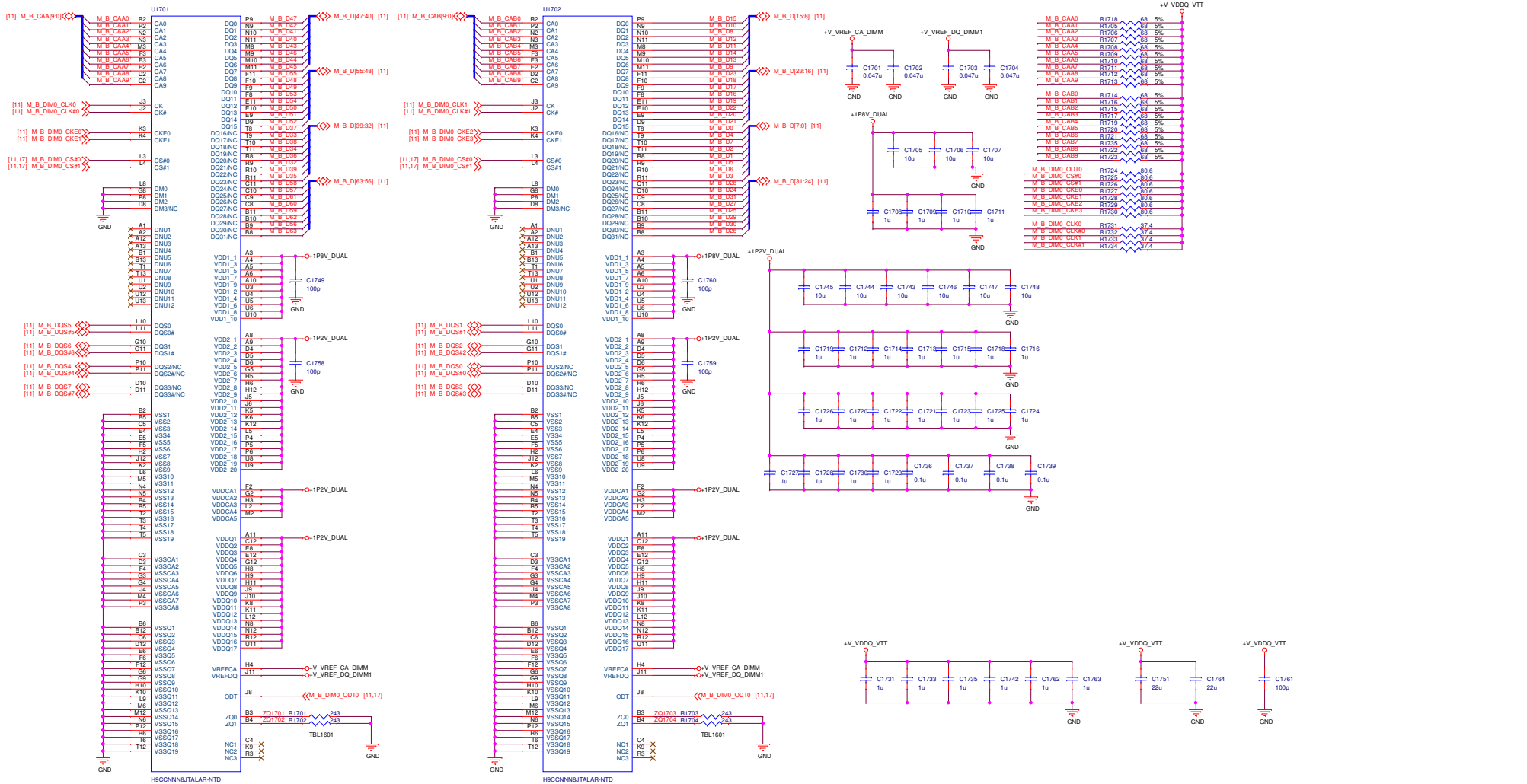
	MEM_ID2	MEM_ID3
8Gb/4GB	0	0
16Gb/8GB	1	0
32Gb/16GB	0	1

Title: LPDDR3(1)_MEMORY DOWN

<OrgName> Engineer: <OrgAddr1>

Size: A2 | Project Name: CHARIOT | Rev: 1.00

Date: Thursday, June 25, 2015 | Sheet 16 of 76



R1702 & R1704	
8Gb/4GB	NC
16Gb/8GB	Install

(PCH side)

	MEM_ID2	MEM_ID3
8Gb/4GB	0	0
16Gb/8GB	1	0
32Gb/16GB	0	1

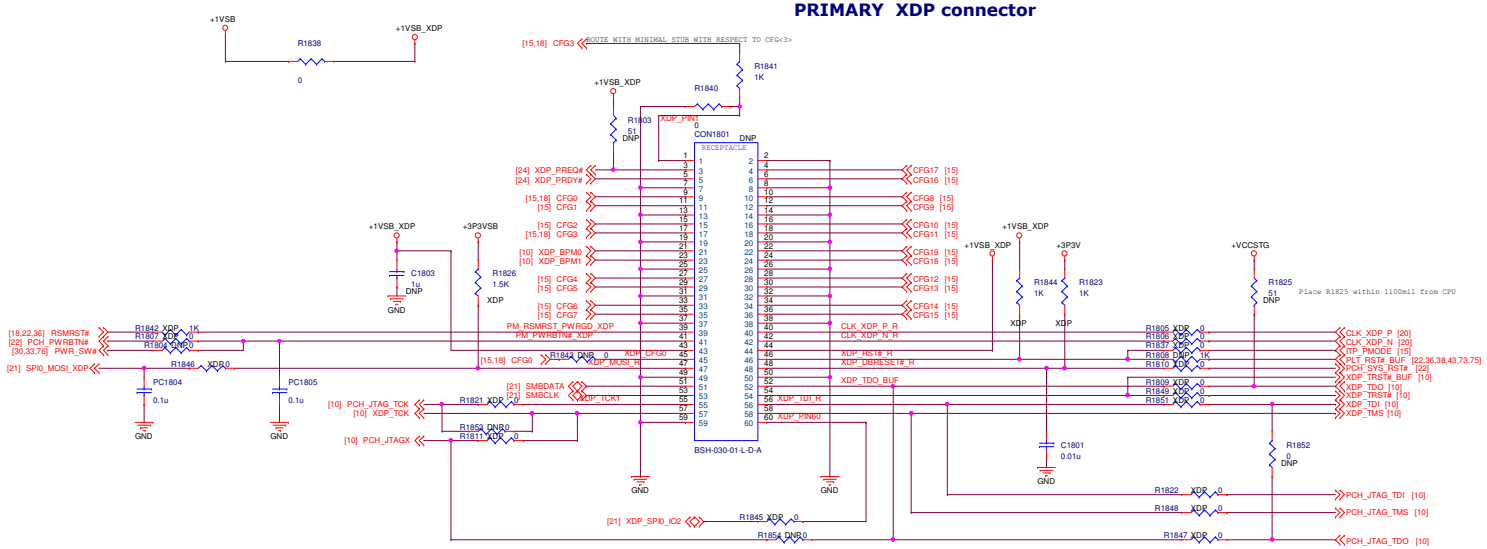
Title: LPDDR3(2)_MEMORY DOWN

Engineer: <OrgAddr1>

Size	Project Name	Rev
A2	CHARIOT	1.00

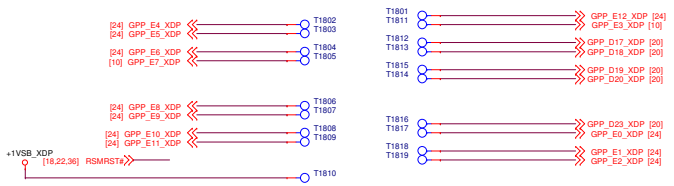
Date: Thursday, June 25, 2015 Sheet 17 of 76

PRIMARY XDP connector



put X854325-001 for MRB board and EV1, since it has been put onto bottom side, which in DNP by default.

SECOND XDP connector (TP only)

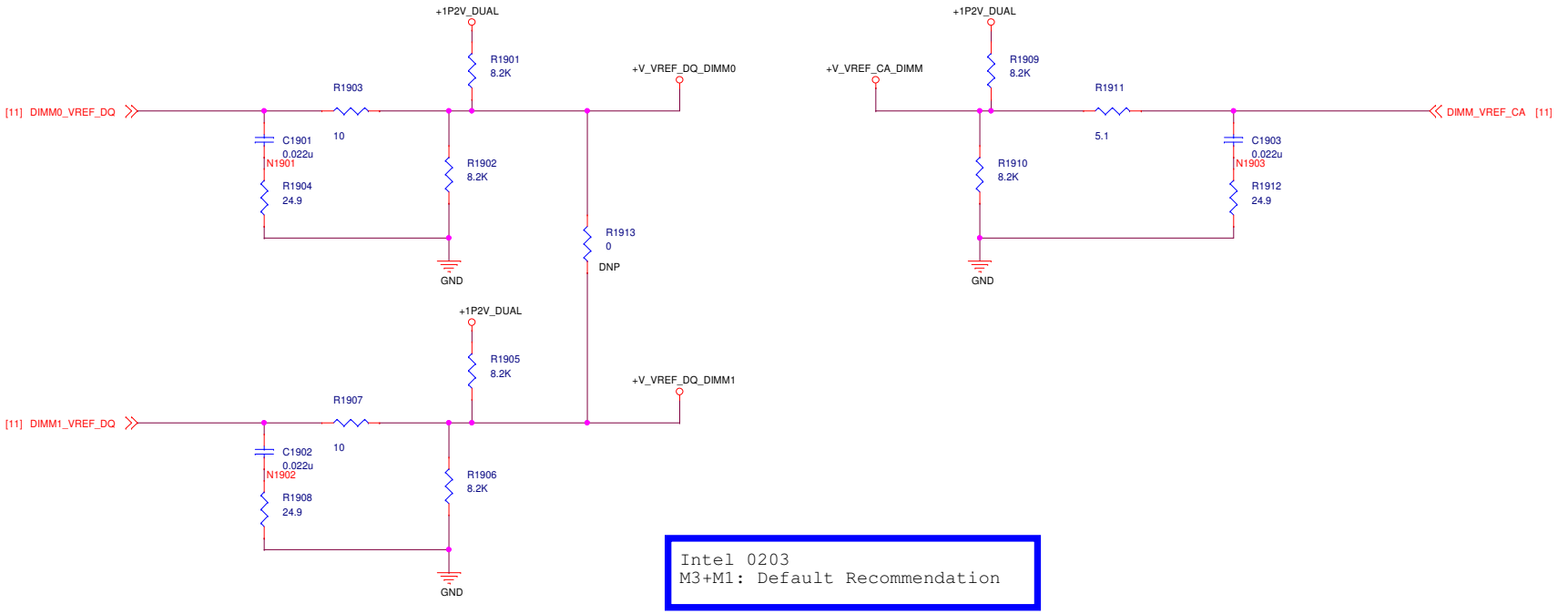


For the signals only go to XDP, the OR should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor location should follow the target signal routing.

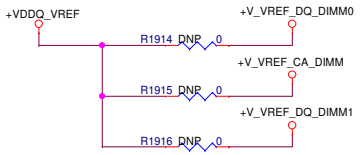
Title: XDP		
Engineer: <OrgAddr1>		
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 18 of 76	

LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

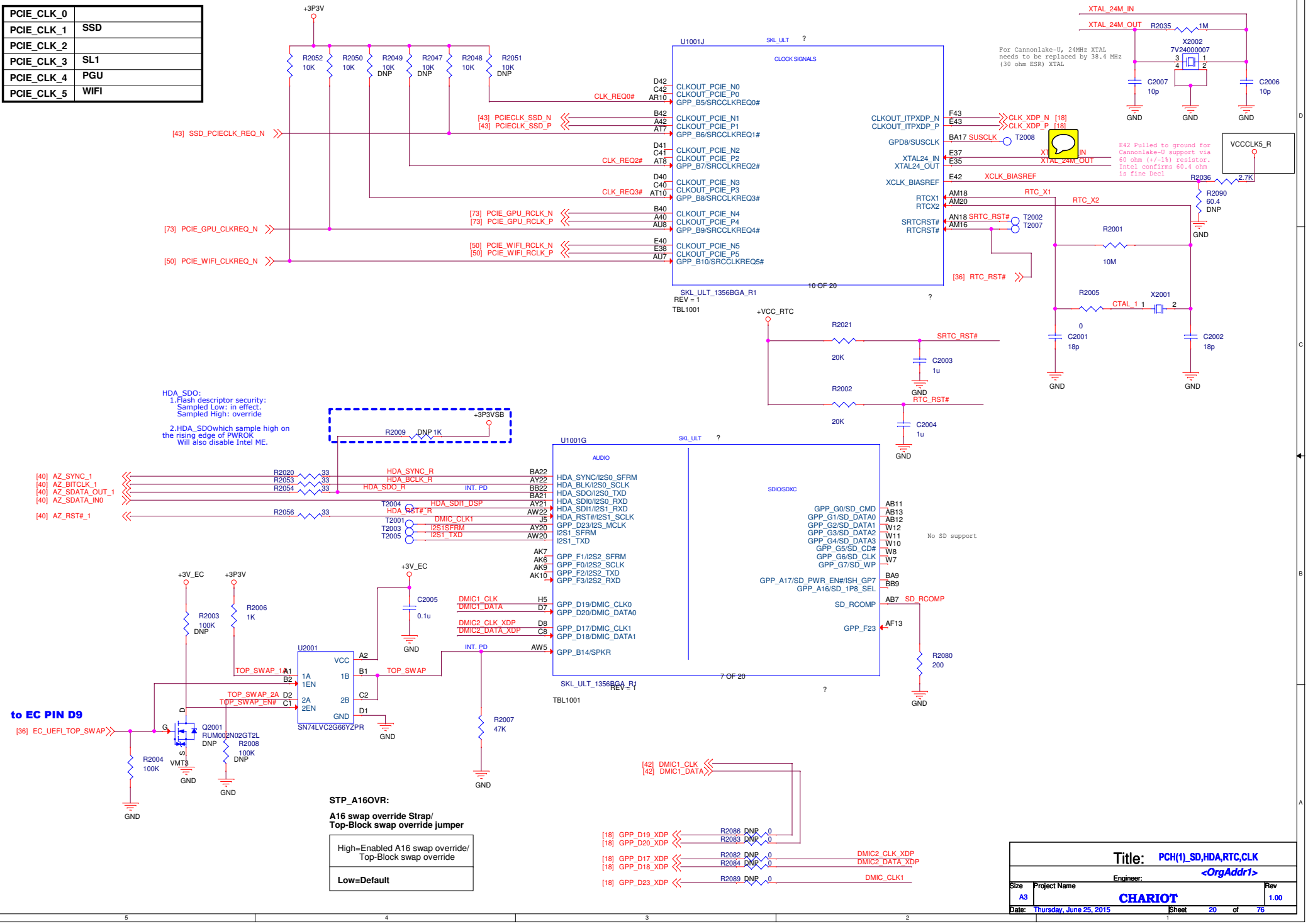


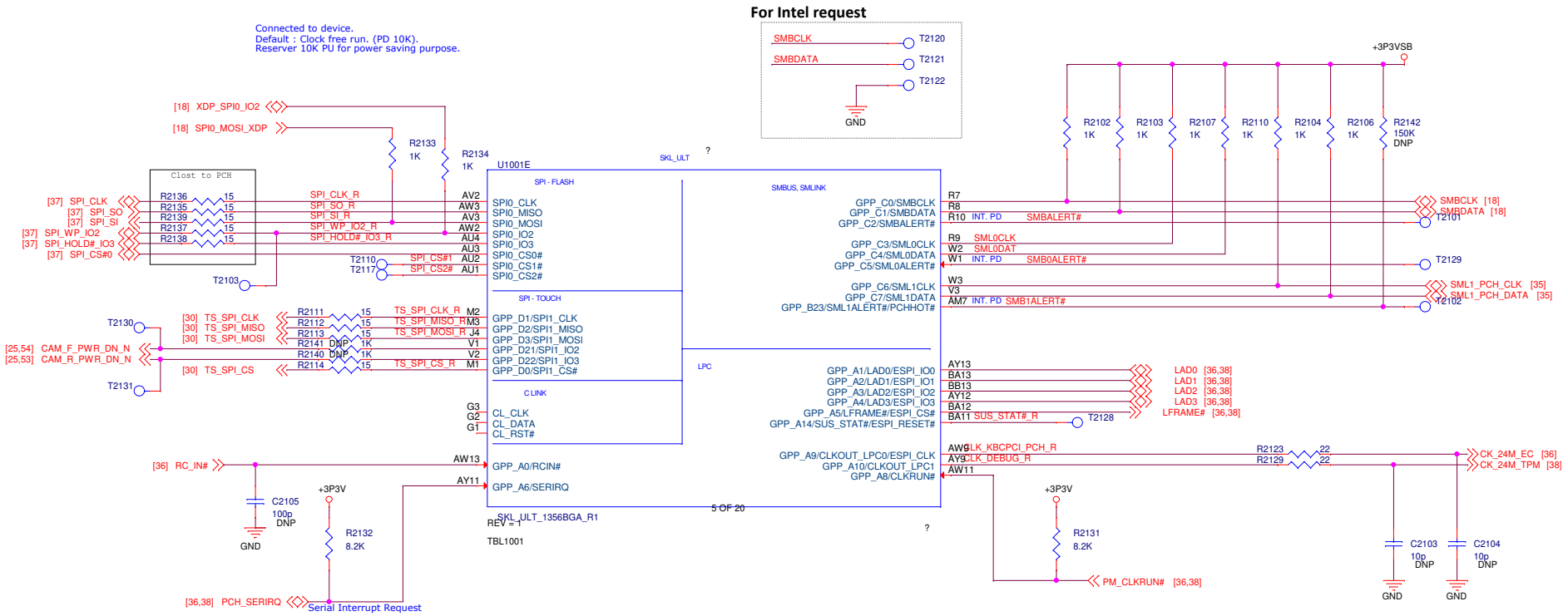
Intel 0203
M3+M1: Default Recommendation



Title:	LPDDR3(3)_CA/DQ Voltage	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 19 of 76	

PCIE_CLK_0	
PCIE_CLK_1	SSD
PCIE_CLK_2	
PCIE_CLK_3	SL1
PCIE_CLK_4	PGU
PCIE_CLK_5	WIFI

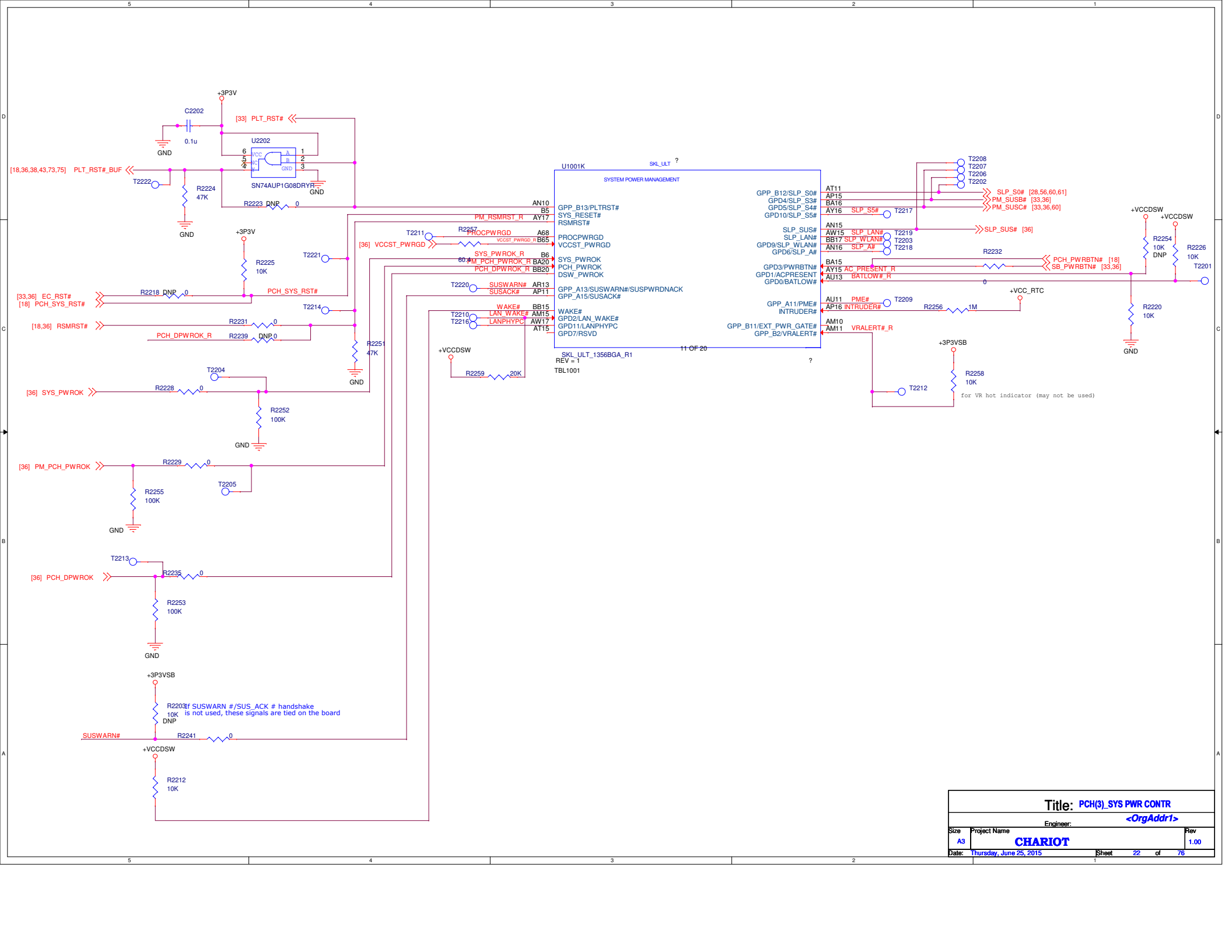




GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SML0ALERT#	
0 **Default**	LPC **(EC)**
1	eSPI **(EC)**

Title:	PCH(2)_CLK,SMB,LPC,SPI		
Engineer:	<OrgAddr1>		
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 21 of 76		

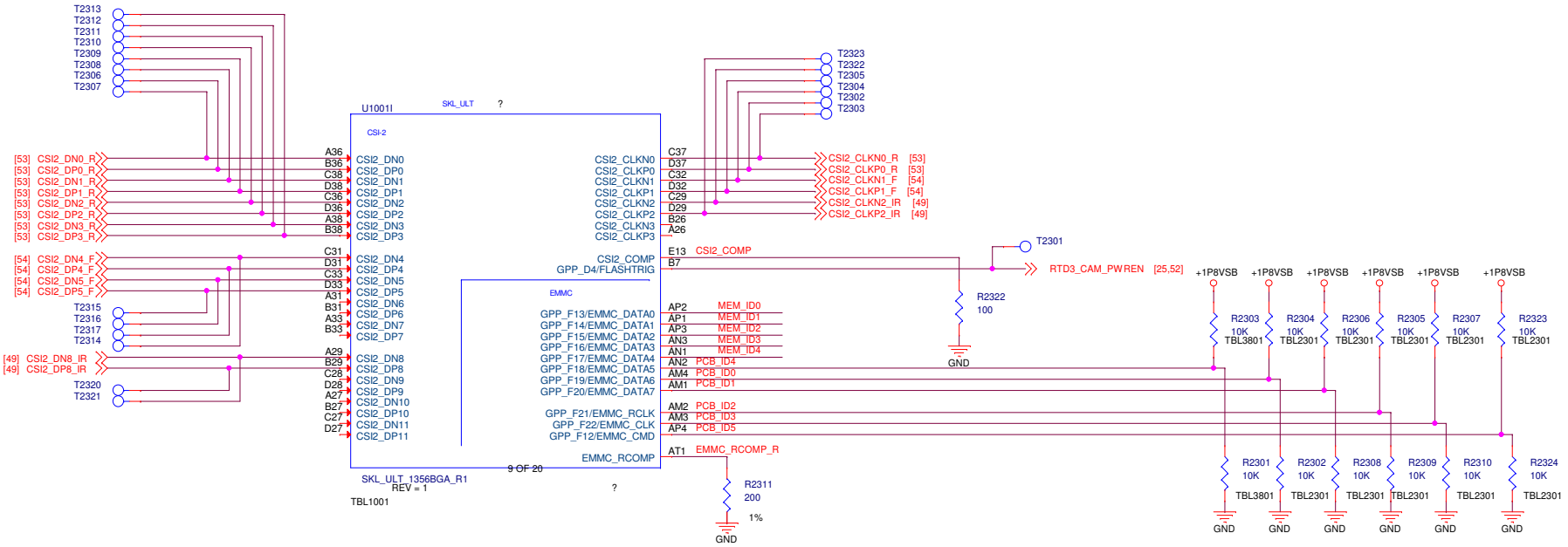


Title:	PCH(3)_SYS PWR CONTR	
	<OrgAddr1>	
Engineer:		
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 22 of 76	

TBL2301

Build	X861217-001 Qty (10K 0201)	PCH_Value	PCH_10K	PCH_NOSTUFF
i5 EV1.0	4	01111	R2304,R2305,R2306,R2307,R2324	R2302,R2308,R2309,R2310,R2323
i5 EV2A	4	00001	R2304,R2308,R2309,R2310,R2324	R2302,R2305,R2306,R2307,R2323
i5 EV2B	4	00010	R2302,R2306,R2309,R2310,R2324	R2304,R2305,R2307,R2308,R2323
i5 EV3A	4	00011	R2304,R2306,R2309,R2310,R2324	R2302,R2305,R2307,R2308,R2323
i5 EV3B	4	00100	R2302,R2305,R2308,R2310,R2324	R2304,R2306,R2307,R2309,R2323
i5DOE	4	00101	R2304,R2305,R2308,R2310,R2324	R2302,R2306,R2307,R2309,R2323
i5DV	4	00110	R2302,R2305,R2306,R2310,R2324	R2304,R2307,R2308,R2309,R2323

Those test point will be removed after check CSI



	MEM_ID4
1600 LPDDR3	0
1866 LPDDR3	1

	MEM_ID1	MEM_ID0
Hynix	0	0
Samsung	0	1

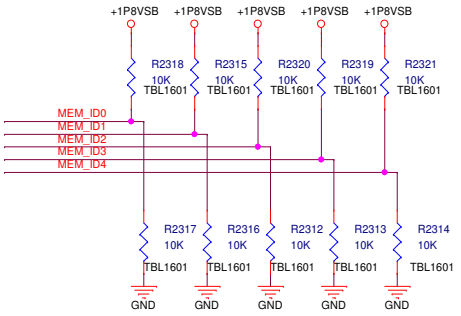
32Gb * 4(pcs) = 16GB
16Gb * 4(pcs) = 8GB
8Gb * 4(pcs) = 4GB

	MEM_ID2	MEM_ID3
4GB	0	0
8GB	1	0
16GB	0	1

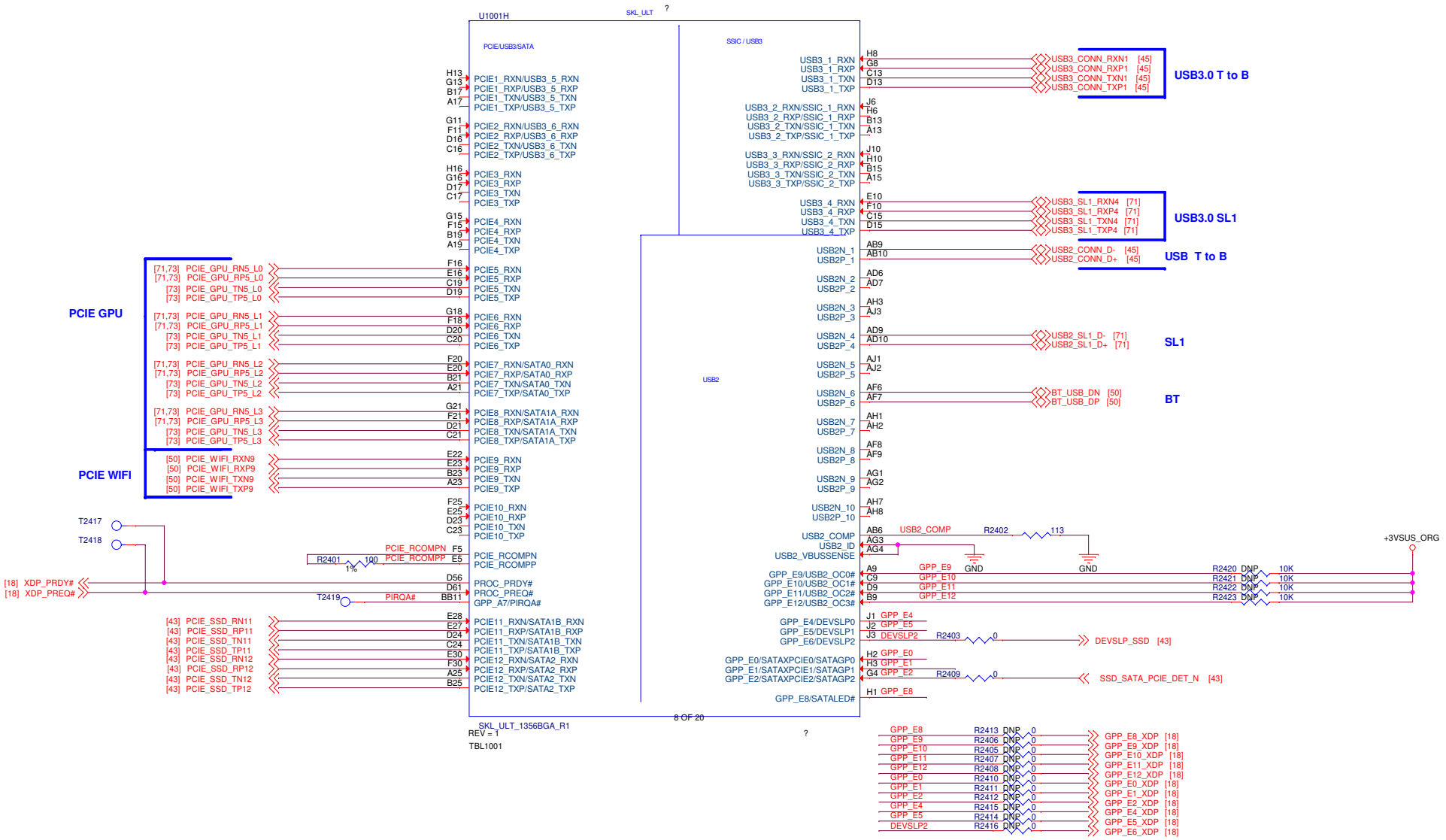
	R1602 & R1604	R1702 & R1704
4GB	NC	
8GB	Install	
16GB	Install	

		PCB_ID4
Infineon SLB9665		0
Nation Z		1

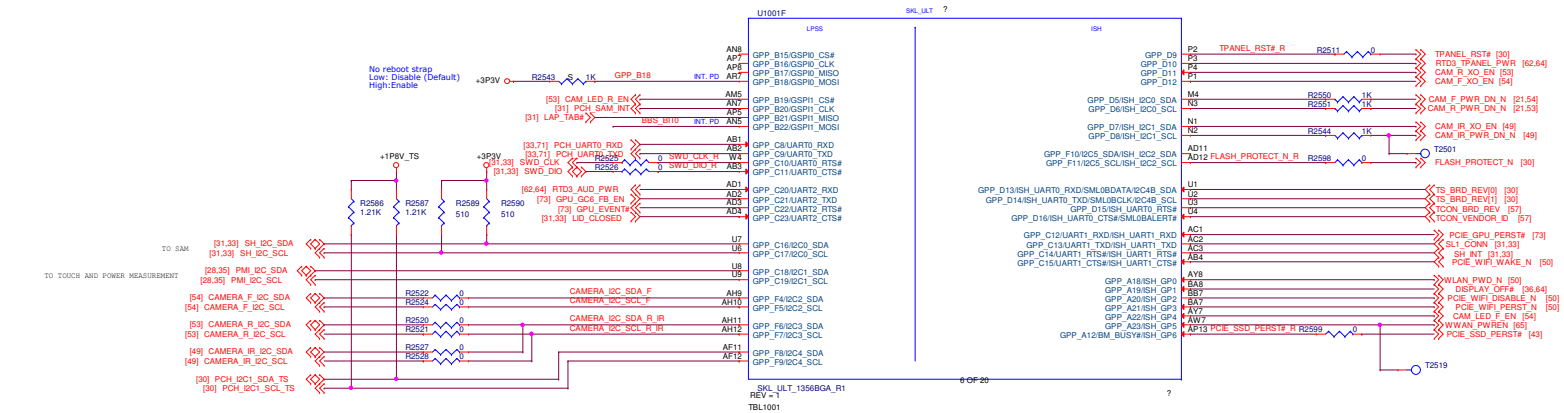
		PCBID5	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0
EV1.0	R1.00	0	1	1	1	1
EV2A	R1.01	0	0	0	0	1
EV2B	R1.02	0	0	0	1	0
EV3A	R1.03	0	0	0	1	1
EV3B	R1.04	0	0	1	0	0
DOE	R1.04	0	0	1	0	1
DV	R1.05	0	0	1	1	0

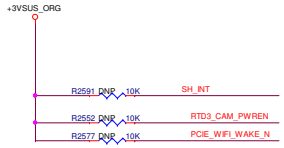


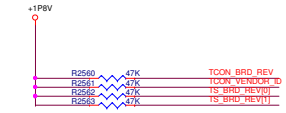
Title:	PCH(4)_CCI, HWID
	<OrgAddr1>
Engineer:	
Size: A3	Project Name: CHARIOT
Rev: 1.00	
Date: Thursday, June 25, 2015	Sheet 23 of 76

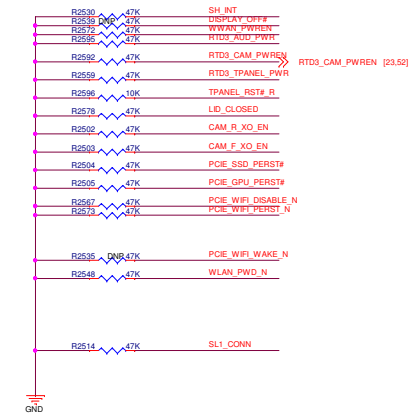


Title:	PCH(5)_PCIE,USB	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 24 of 76	





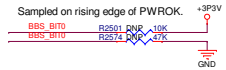




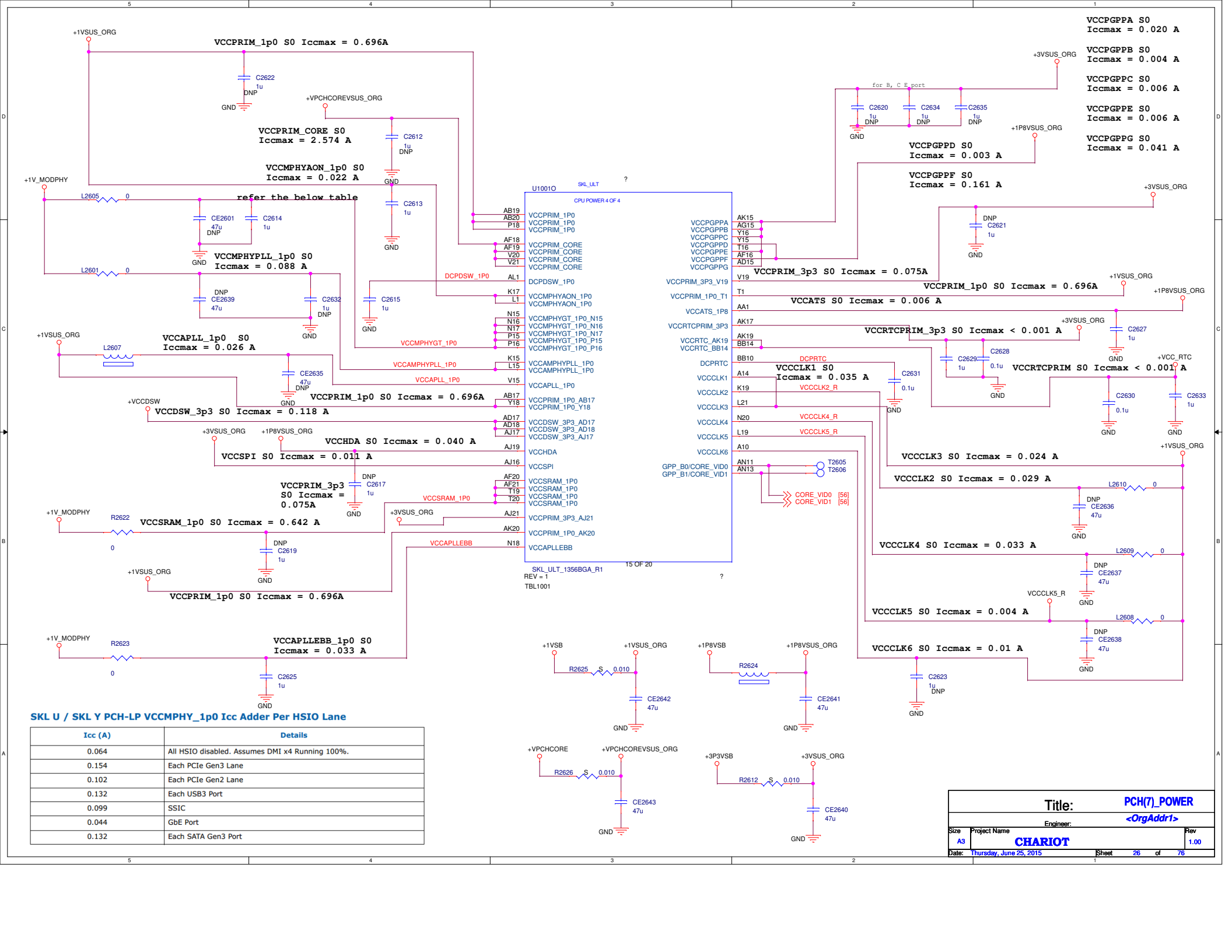
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC
0	SPI**(PCH)**

Sampled on rising edge of PWROK.

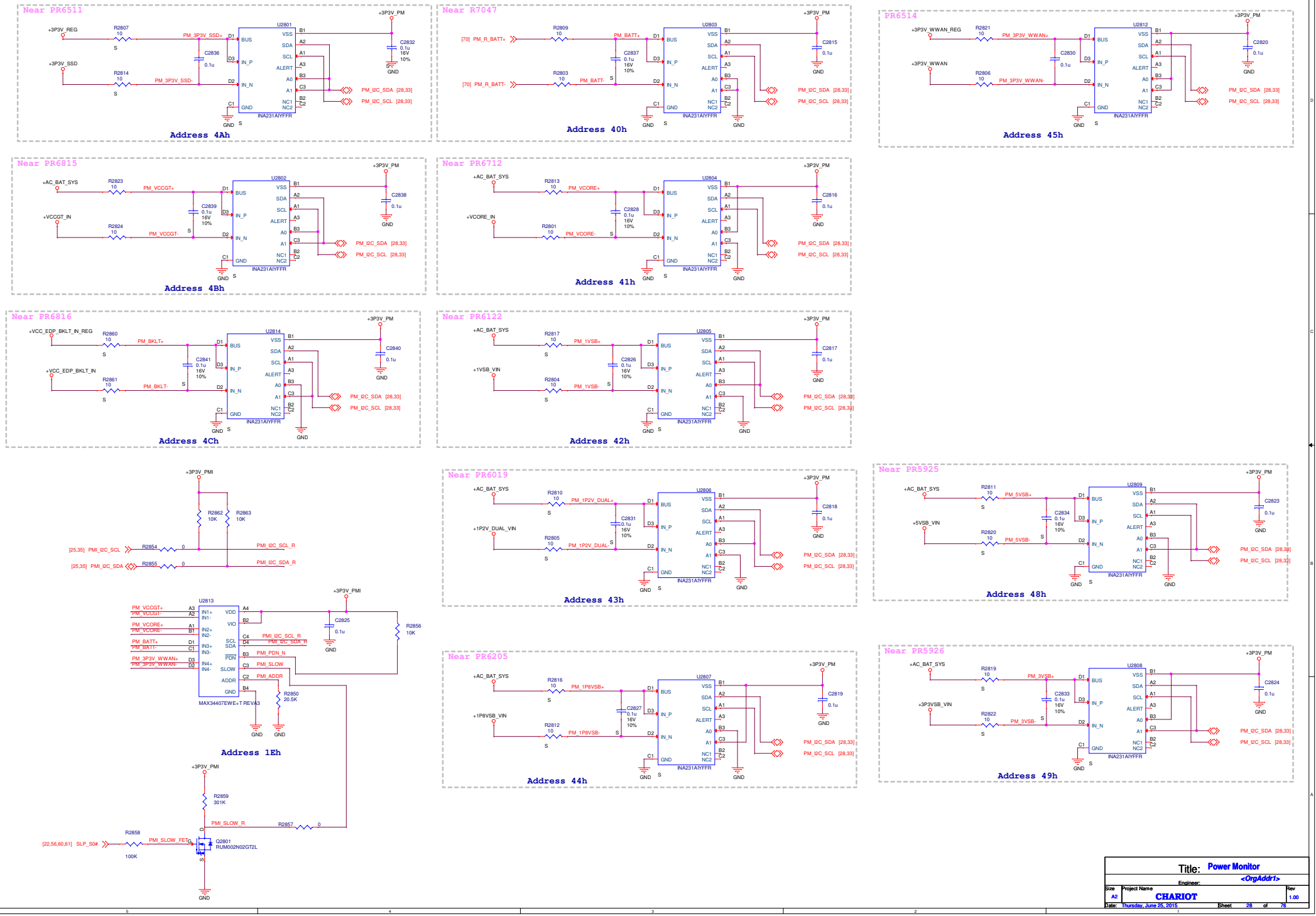


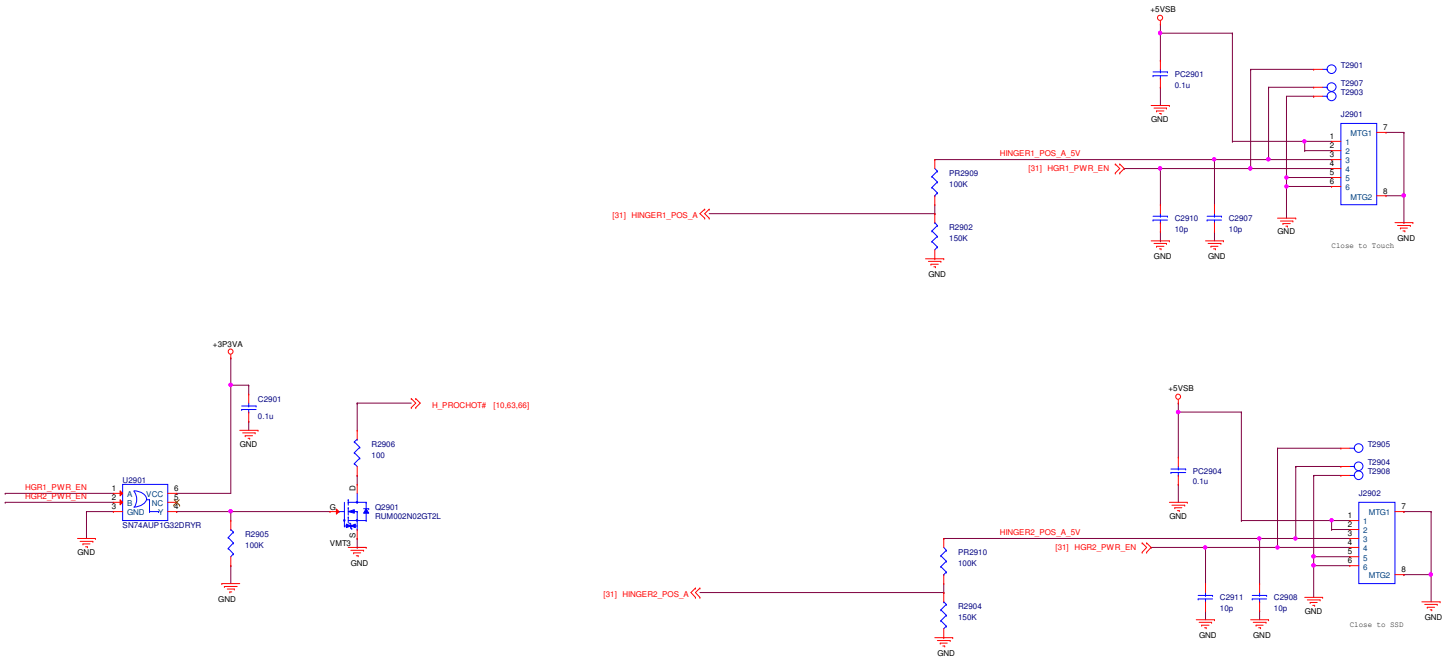
Title:	PCH(6)_CPU,GPIO,MISC	
Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 25 of 76	



Icc (A)	Details
0.064	All HSIO disabled. Assumes DMI x4 Running 100%.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

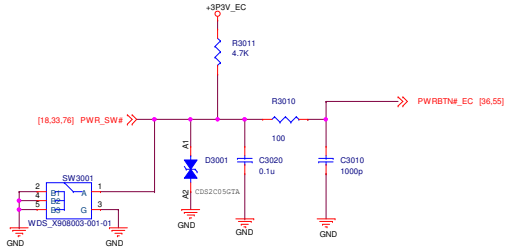
Title:	PCH(8)_empty			
Engineer:	<OrgAddr1>			
Size: A3	Project Name: CHARIOT			Rev: 1.00
Date: Thursday, June 25, 2015		Sheet 27 of 76		


Near PR6511
+3P3V_REG
R2807
10
S
PM_3P3V_SSD+
D1
BUS
+3P3V_SSD
R2814
10
S
PM_3P3V_SSD-
D2
IN_N
C2836
0.1u
D3
IN_P
C1
GND
U2801
VSS
SDA
SCL
ALERT
A0
A1
NC1
NC2
INA231AIYFFR
B1
A2
A1
A3
B3
C3
B2
C2
+3P3V_PM
C2832
0.1u
16V
10%
S
GND
PM_I2C_SDA [28,33]
PM_I2C_SCL [28,33]
Address 4Ah
Near R7047
[70] PM_R_BATT+
R2809
10
PM_BATT+
[70] PM_R_BATT-
R2803
10
PM_BATT-
C2837
0.1u
16V
10%
U2803
C2815
0.1u
Address 40h
PR6514
+3P3V_WWAN_REG
R2821
10
PM_3P3V_WWAN+
+3P3V_WWAN
R2806
10
PM_3P3V_WWAN-
C2830
0.1u
U2812
C2820
0.1u
Address 45h
Near PR6815
+AC_BAT_SYS
R2823
10
PM_VCCGT+
+VCCGT_IN
R2824
10
PM_VCCGT-
C2839
0.1u
16V
10%
U2802
C2838
0.1u
Address 4Bh
Near PR6712
+AC_BAT_SYS
R2813
10
PM_VCORE+
+VCORE_IN
R2801
10
PM_VCORE-
C2828
0.1u
16V
10%
U2804
C2816
0.1u
Address 41h
Near PR6816
+VCC_EDP_BKLT_IN_REG
R2860
10
PM_BKLT+
+VCC_EDP_BKLT_IN
R2861
10
PM_BKLT-
C2841
0.1u
16V
10%
U2814
C2840
0.1u
Address 4Ch
Near PR6122
+AC_BAT_SYS
R2817
10
PM_1VSB+
+1VSB_VIN
R2804
10
PM_1VSB-
C2826
0.1u
16V
10%
U2805
C2817
0.1u
Address 42h
+3P3V_PMI
R2862
10K
R2863
10K
[25,35] PMI_I2C_SCL
R2854
0
PMI_I2C_SCL_R
[25,35] PMI_I2C_SDA
R2855
0
PMI_I2C_SDA_R
U2813
PM_VCCGT+
PM_VCCGT-
PM_VCORE+
PM_VCORE-
PM_BATT+
PM_BATT-
PM_3P3V_WWAN+
PM_3P3V_WWAN-
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
IN4+
IN4-
VDD
VIO
SCL
SDA
PDN
SLOW
ADDR
GND
PMI_I2C_SCL_R
PMI_I2C_SDA_R
PMI_PDN_N
PMI_SLOW
PMI_ADDR
C2825
0.1u
R2856
10K
R2850
20.5K
MAX34407EWE+T REV A3
Address 1Eh
R2859
301K
PMI_SLOW_R
R2857
0
R2858
100K
[22,56,60,61] SLP_S0#
PMI_SLOW_FET
Q2801
RUM002N02GT2L
Near PR6019
+AC_BAT_SYS
R2810
10
PM_1P2V_DUAL+
+1P2V_DUAL_VIN
R2805
10
PM_1P2V_DUAL-
C2831
0.1u
16V
10%
U2806
C2818
0.1u
Address 43h
Near PR5925
+AC_BAT_SYS
R2811
10
PM_5VSB+
+5VSB_VIN
R2820
10
PM_5VSB-
C2834
0.1u
16V
10%
U2809
C2823
0.1u
Address 48h
Near PR6205
+AC_BAT_SYS
R2816
10
PM_1P8VSB+
+1P8VSB_VIN
R2812
10
PM_1P8VSB-
C2827
0.1u
16V
10%
U2807
C2819
0.1u
Address 44h
Near PR5926
+AC_BAT_SYS
R2819
10
PM_3VSB+
+3P3VSB_VIN
R2822
10
PM_3VSB-
C2833
0.1u
16V
10%
U2808
C2824
0.1u
Address 49h
Title: Power Monitor
Engineer: <OrgAddr1>
Size: A2
Project Name: CHARIOT
Rev: 1.00
Date: Thursday, June 25, 2015
Sheet 28 of 76

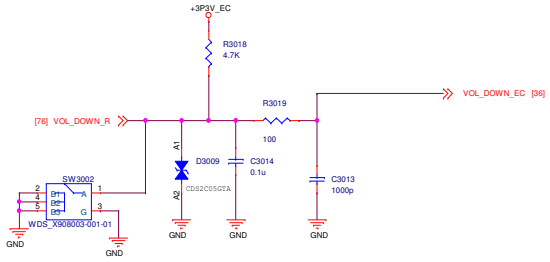


Title: Hinger connector		
Engineer: <OrgAddr1>		
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 29 of 76	

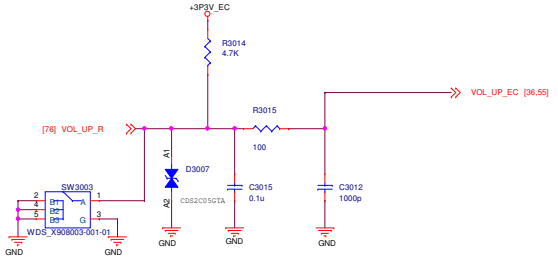
POWER BUTTON



VOL_DOWN BUTTON

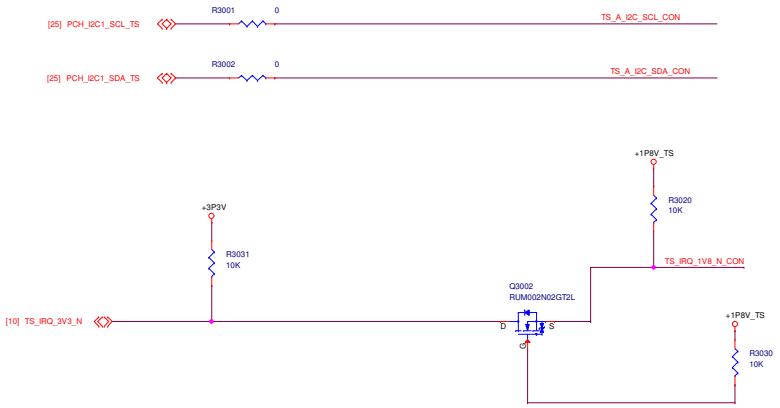


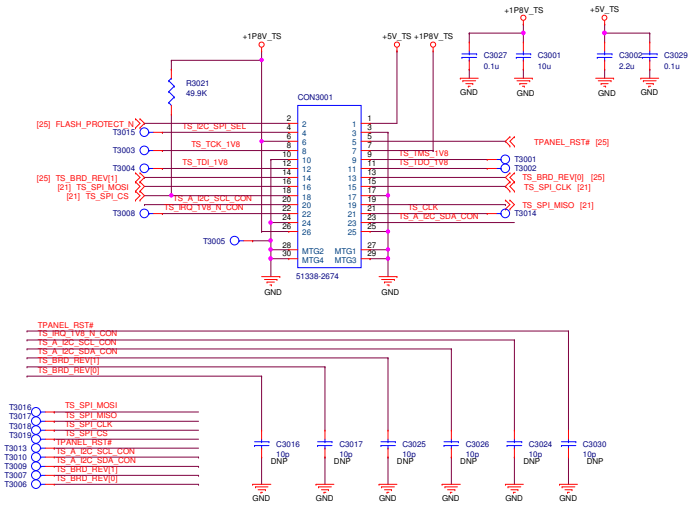
VOL_UP BUTTON



To PCH

To Touch

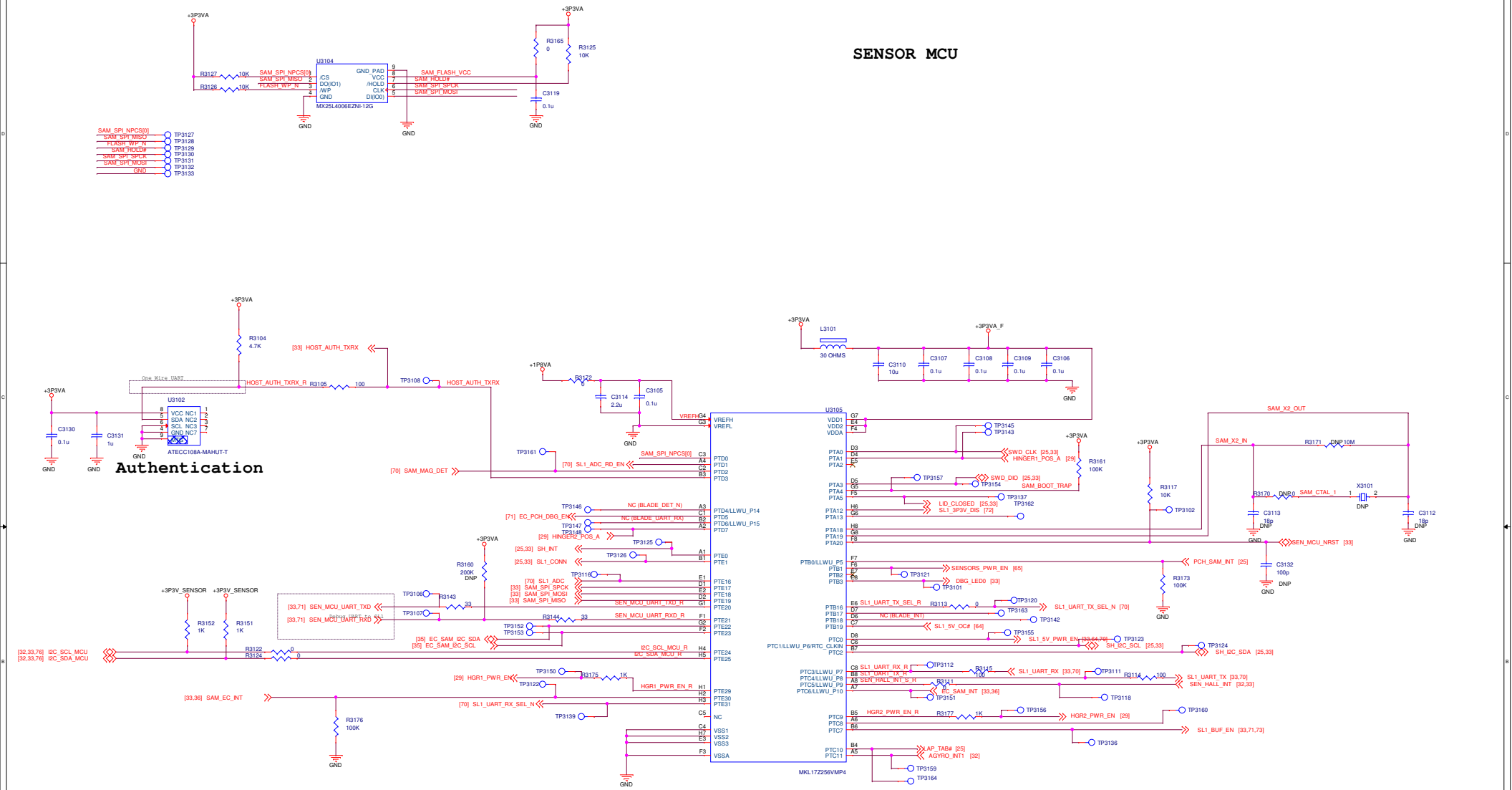




7-bit I2C Address = 0x55

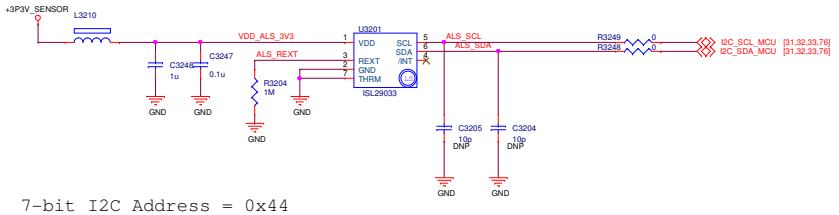
Title:	Touch Con & Key		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 30 of 76		

SENSOR MCU



	HINGER1_POS_A_R	HINGER1_POS_B_R
Closed	High	Low
Transition	High	High
Open	Low	High
fault	Low	Low

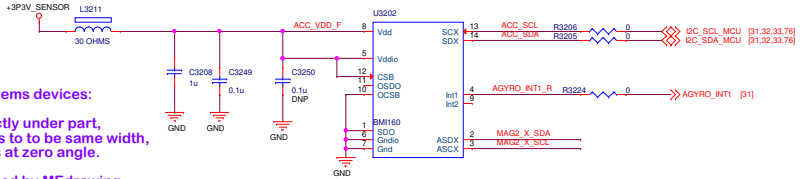
Title:	Sensor-uC
Engineer:	<OrgAddr1>
Size: A2	Project Name
Rev:	1.00
Date:	Thursday, June 25, 2015
Sheet	31 of 76



7-bit I2C Address = 0x44

Accelerometer & Gyro

max Idd = 900uA



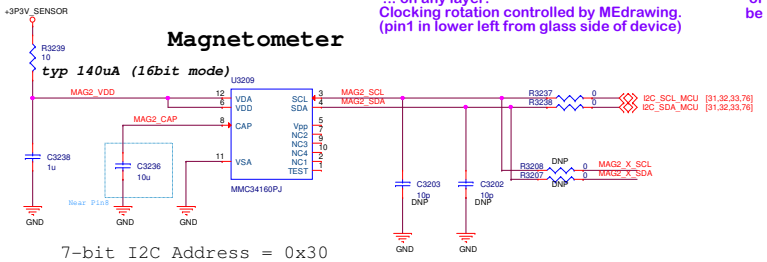
7-bit I2C Address = 0x68

Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to to be same width,
- All traces to enter pads at zero angle.

Clocking rotation controlled by MEdrawing.
(+X Device & +X Surface vectors must be parallel w/same direction
(i.e. if the part is located on the glass side of the PCB, the pin1 indicator dot should be in upper right corner)

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by MEdrawing.
(pin1 in lower left from glass side of device)

Magnetometer

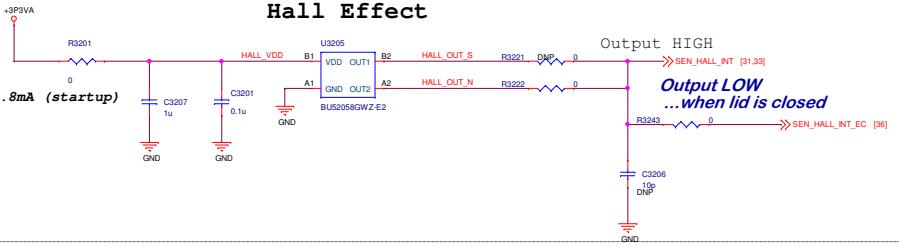


7-bit I2C Address = 0x30

Hall Effect

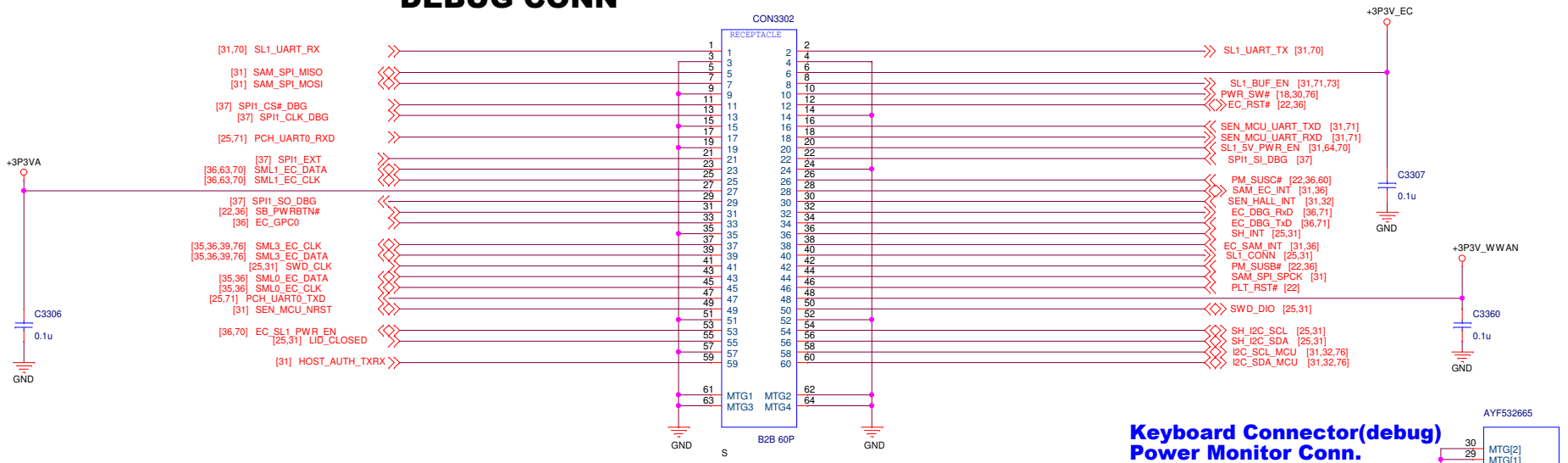
typ Idd = 5uA

typ Idd(en) = 2.8mA (startup)

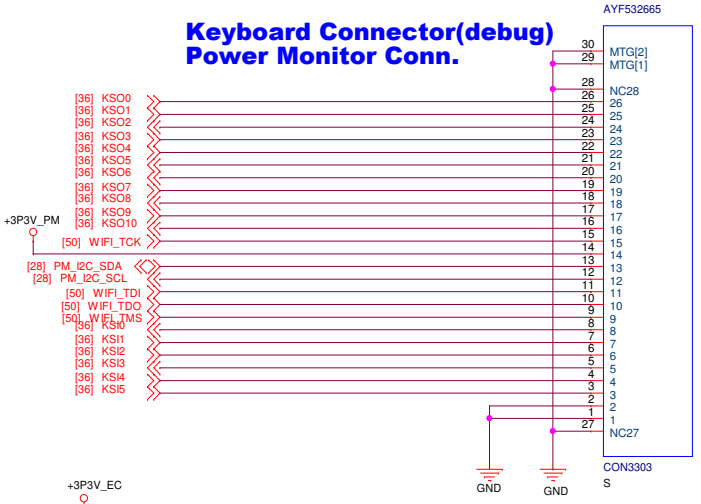


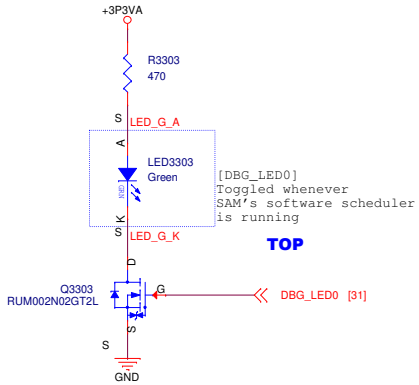
Title:	On Board-Sensors		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 32 of 76		

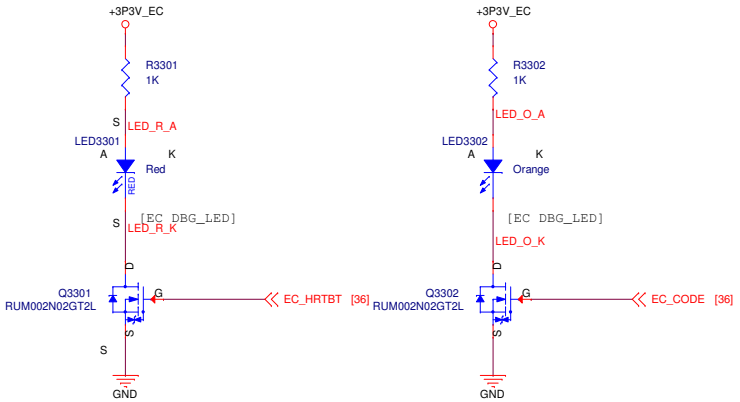
DEBUG CONN



Keyboard Connector(debug)
Power Monitor Conn.





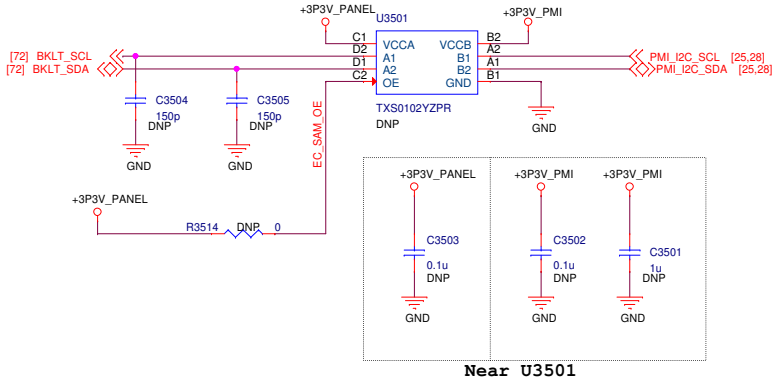


<Core Design>

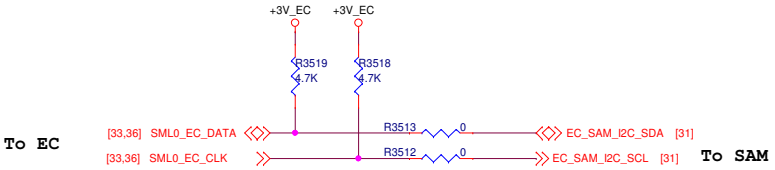
Title:	Debug Conn / LPC	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 33 of 76	

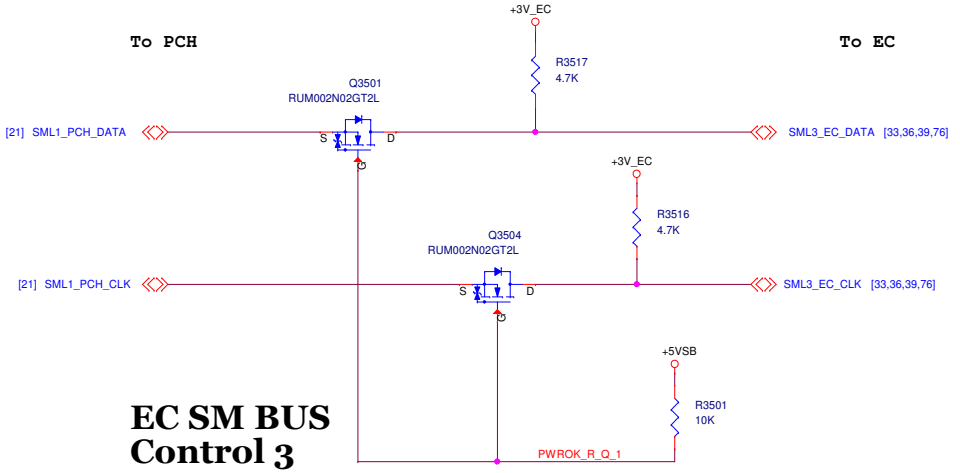
Title:	X
Engineer:	<OrgAddr1>
Size: A4	Project Name: CHARIOT
Rev: 1.00	
Date: Thursday, June 25, 2015	Sheet 34 of 76

EC SM BUS Control 3

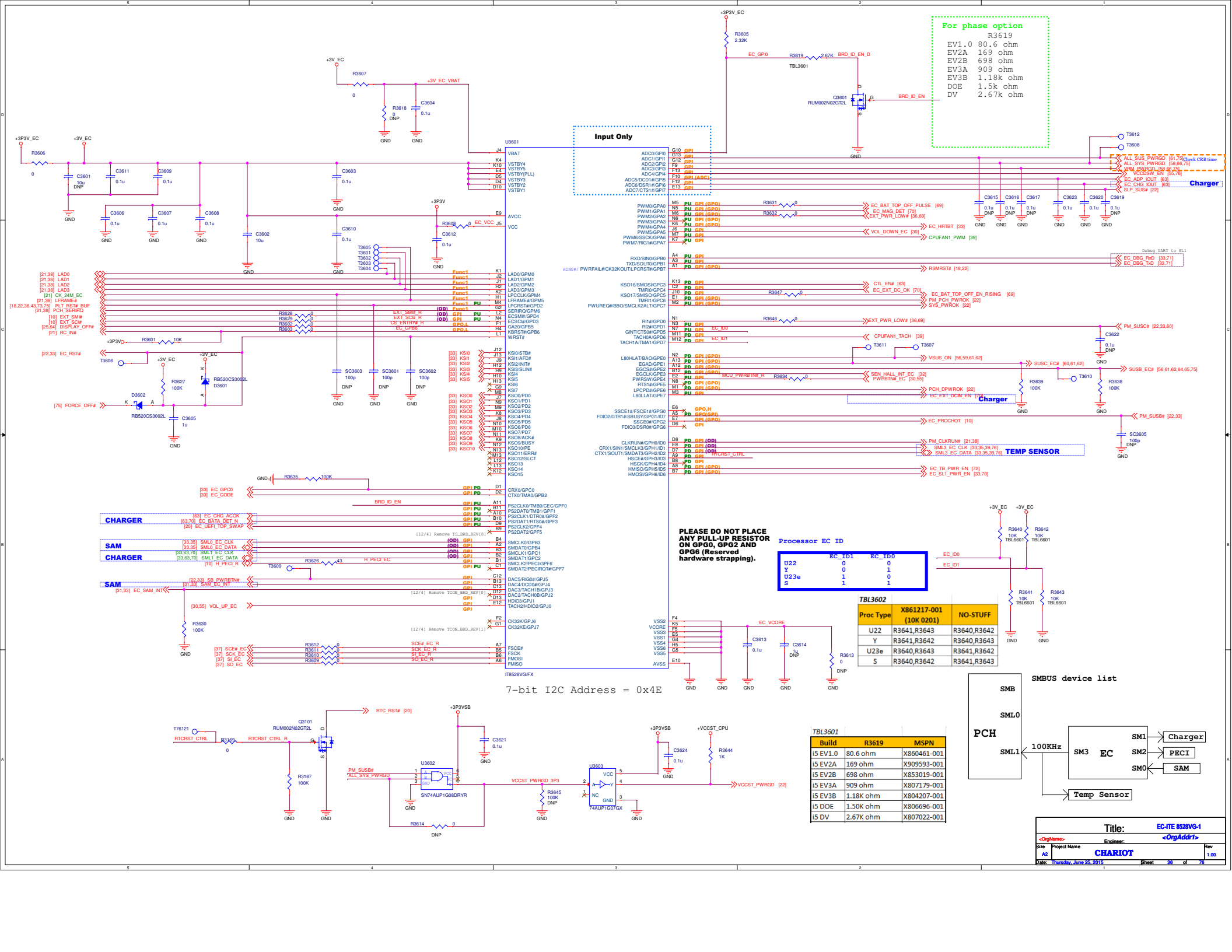


Near U3501



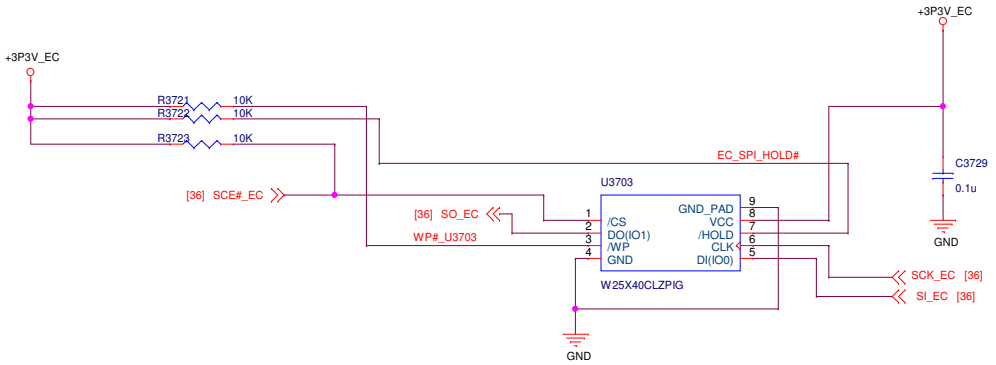


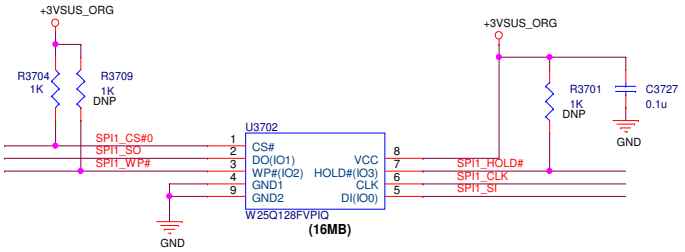
Title:	SM BUS	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 35 of 76	

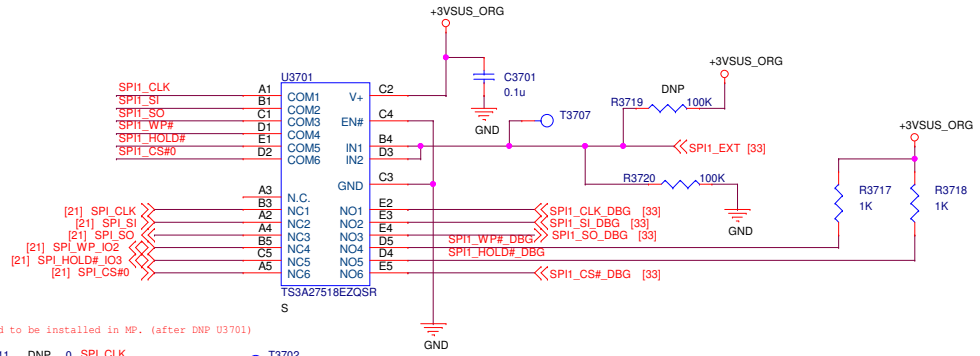

For phase option
R3619
EV1.0 80.6 ohm
EV2A 169 ohm
EV2B 698 ohm
EV3A 909 ohm
EV3B 1.18k ohm
DOE 1.5k ohm
DV 2.67k ohm
Input Only
U3601
ITB528VG/FX
7-bit I2C Address = 0x4E
PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG6 (Reserved hardware strapping).
Processor EC ID
EC_ID1 EC_ID0
U22 0 0
Y 0 1
U23e 1 0
S 1 1
TBL3602
Proc Type | X861217-001 (10K 0201) | NO-STUFF
U22 | R3641,R3643 | R3640,R3642
Y | R3641,R3642 | R3640,R3643
U23e | R3640,R3643 | R3641,R3642
S | R3640,R3642 | R3641,R3643
SMBUS device list
PCH
SMB
SML0
SML1
100KHz
EC
SM1
SM2
SM0
SM3
Charger
PECI
SAM
Temp Sensor
TBL3601
Build | R3619 | MSPN
i5 EV1.0 | 80.6 ohm | X860461-001
i5 EV2A | 169 ohm | X909593-001
i5 EV2B | 698 ohm | X853019-001
i5 EV3A | 909 ohm | X807179-001
i5 EV3B | 1.18K ohm | X804207-001
i5 DOE | 1.50K ohm | X806696-001
i5 DV | 2.67K ohm | X807022-001
Title: EC-ITE 8528VG-1
<OrgName>
Engineer: <OrgAddr1>
Size A2
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 36 of 76

EC SPI ROM

Need to change to X895988-001 4M bit



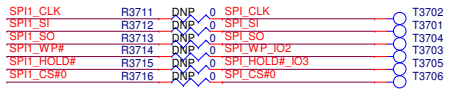




BW=200MHz

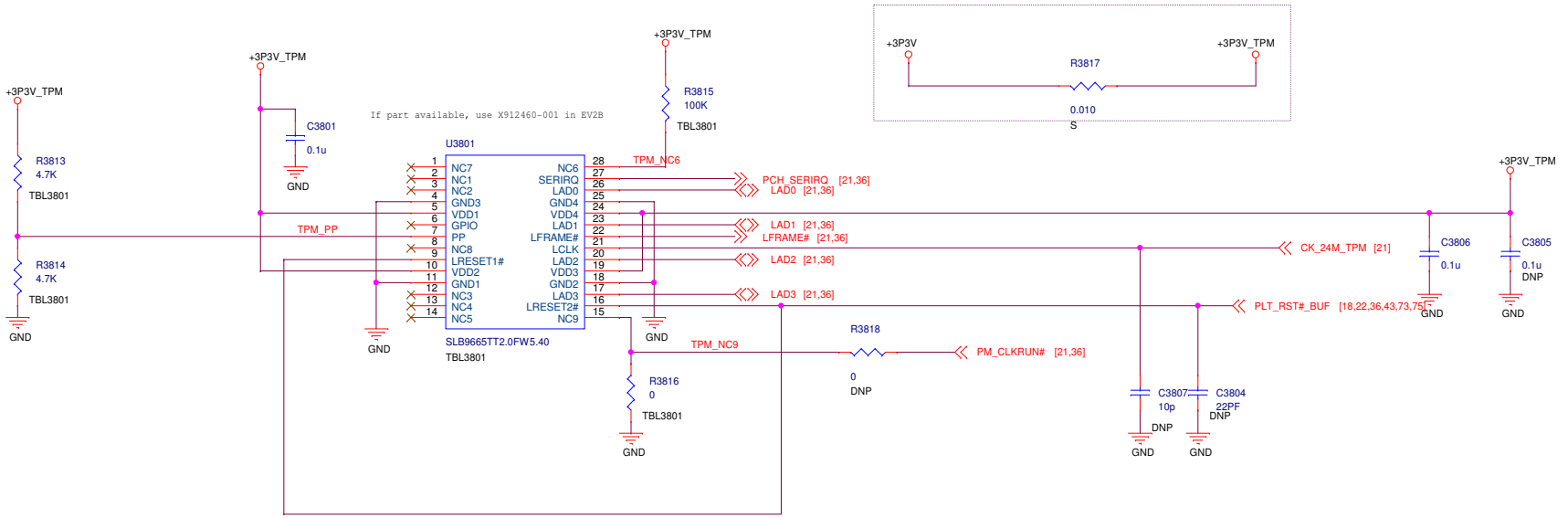
EN#	IN1/IN2	FUNCTION
L	L	COM to NC
L	H	COM to NO
H	X	Disconnect

R3711 to R3716 need to be installed in MP. (after DNP U3701)



Title:	EC-ITE 8528VG-2/SPI ROM	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 37 of 76	

Trusted Platform Module

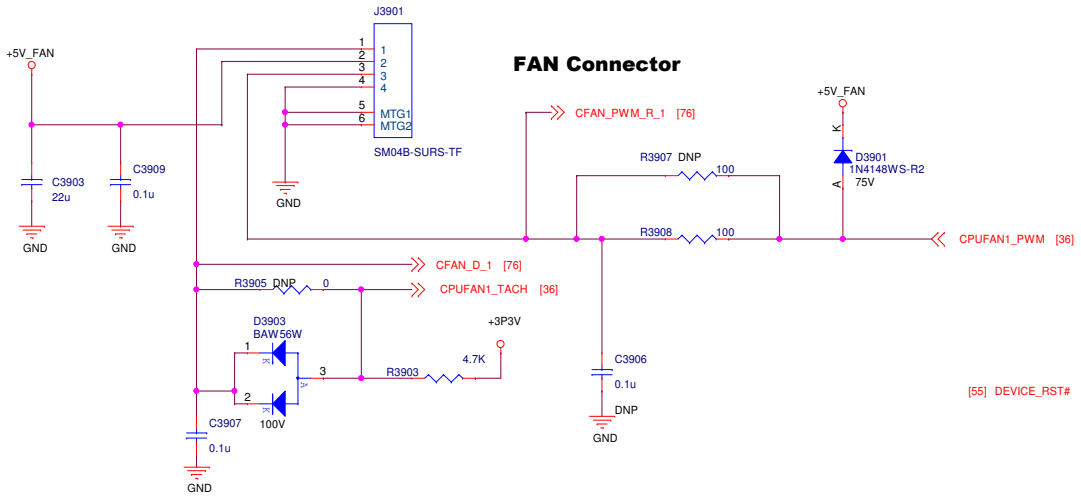


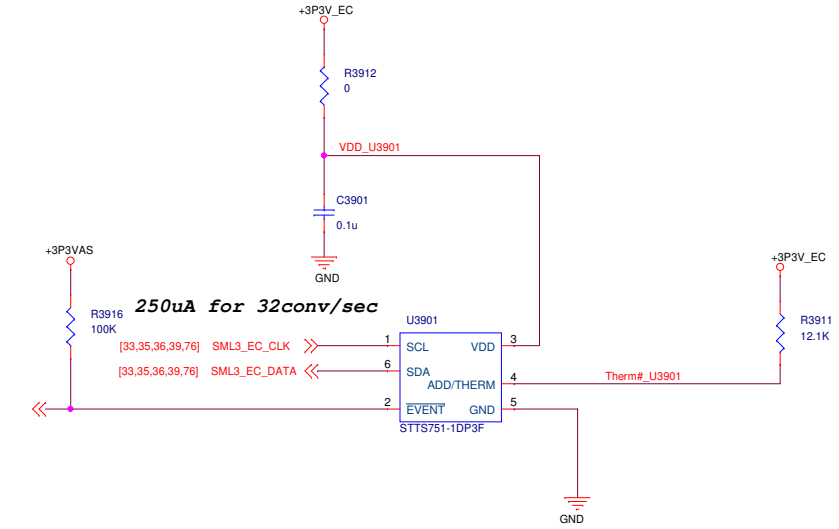
TBL3801

Ref	Infineon	NationZ
R2301	X861217-001	NO-STUFF
R2303	NO-STUFF	X861217-001
R3813	NO-STUFF	X800613-001
R3814	X800613-001	NO-STUFF
R3815	NO-STUFF	X813010-001
R3816	NO-STUFF	X811786-001
U3801	X912460-001	X930840-001

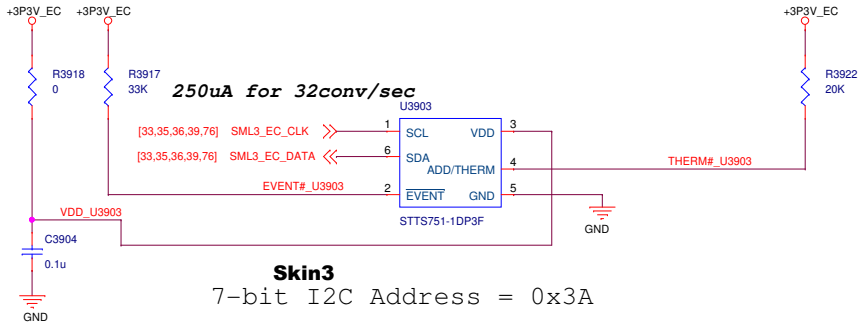
Title:	TPM	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 38 of 76	

+5V_FAN
Imax=0.7A
Trace Width>30mil

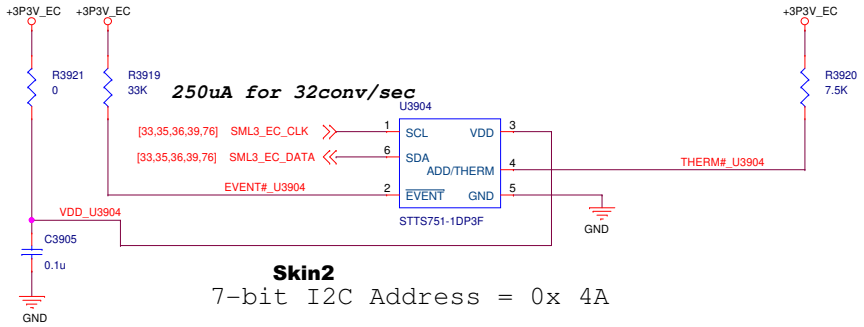




Skin0
7-bit I2C Address = 0x4B

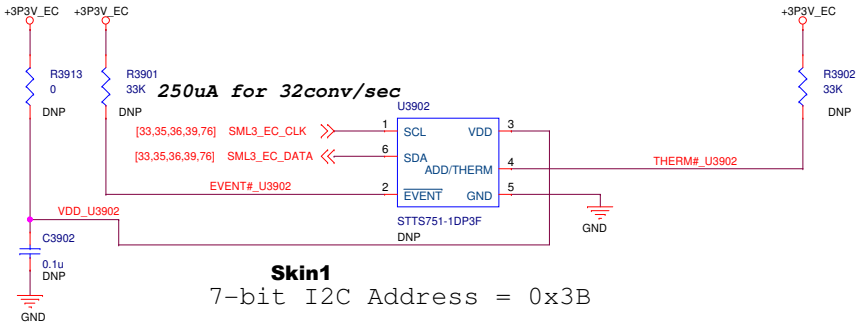


Skin3
7-bit I2C Address = 0x3A



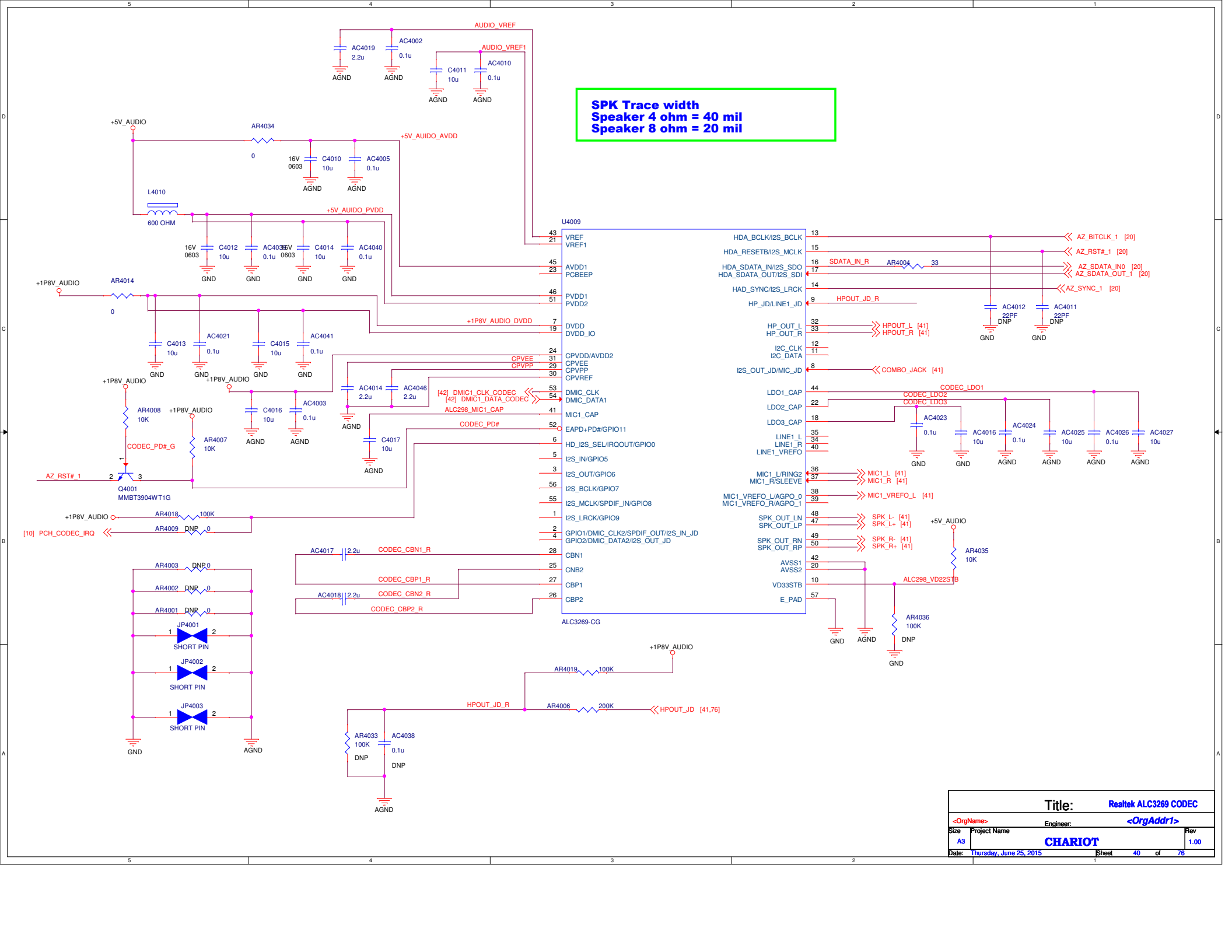
Skin2
7-bit I2C Address = 0x 4A

temp sensor for the right location testing

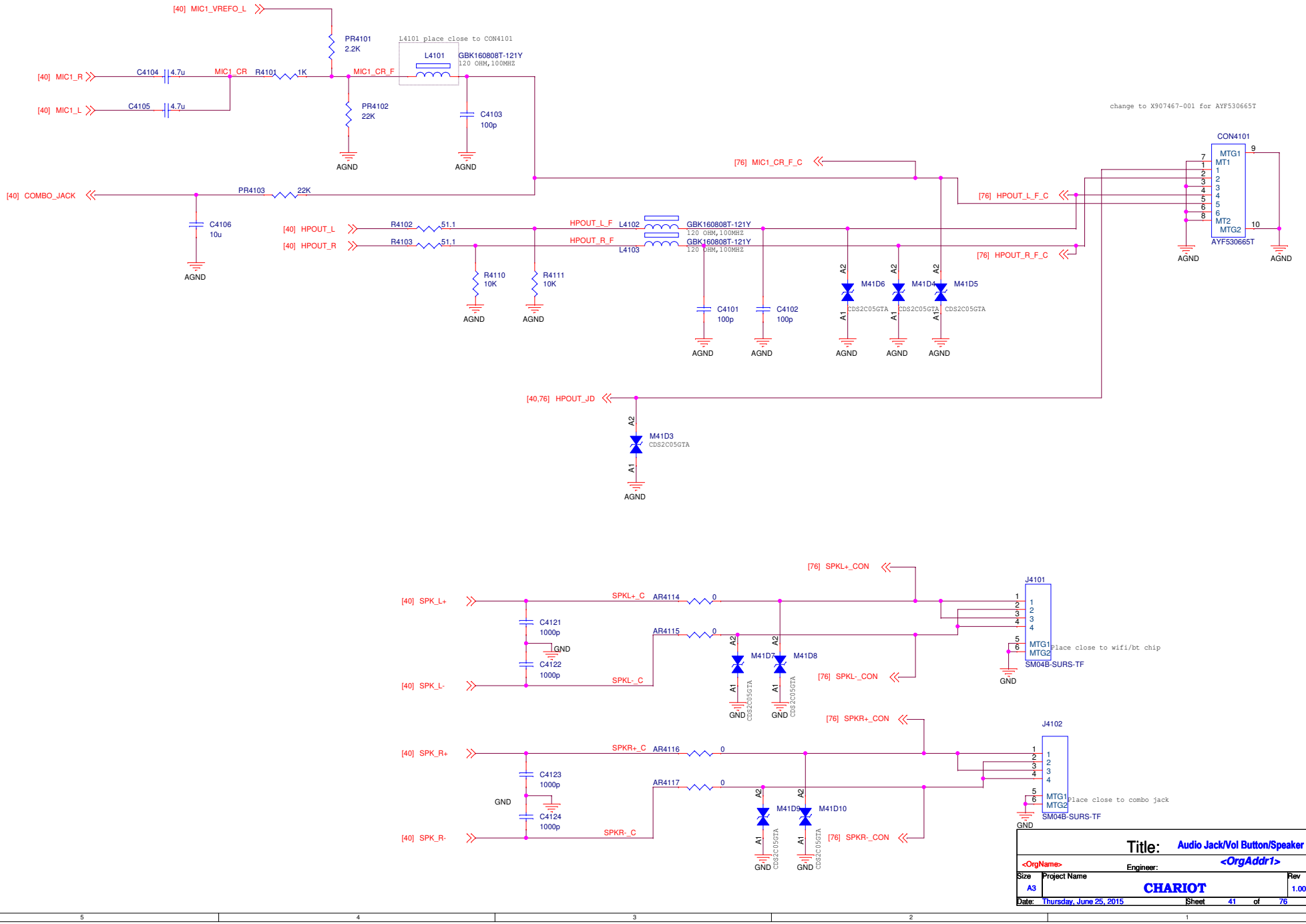


Skin1
7-bit I2C Address = 0x3B

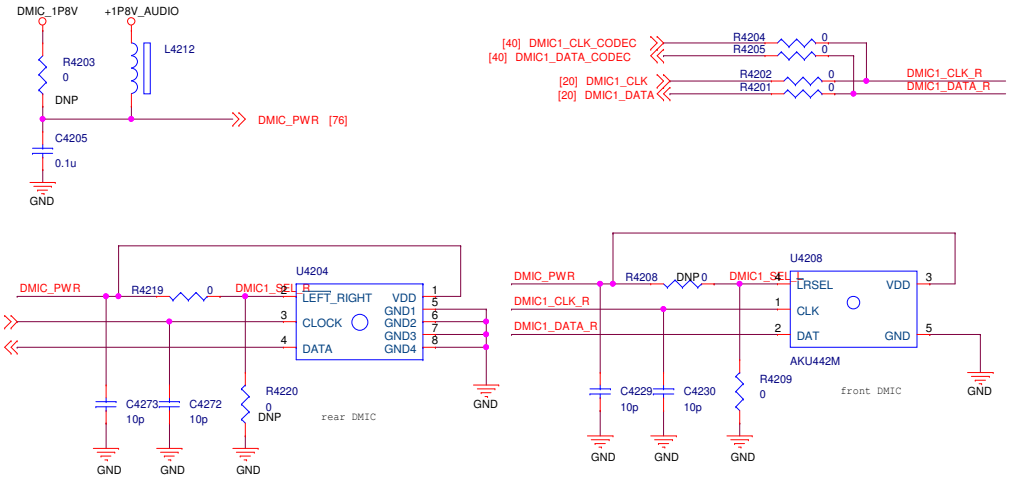
Title:	Temp Sensor/System Fan		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 39 of 76		


SPK Trace width
Speaker 4 ohm = 40 mil
Speaker 8 ohm = 20 mil
U4009
ALC3269-CG
AUDIO_VREF
AUDIO_VREF1
+5V_AUDIO
+5V_AUIDO_AVDD
+5V_AUIDO_PVDD
+1P8V_AUDIO
+1P8V_AUDIO_DVDD
AR4034
AR4014
L4010
600 OHM
AC4019
AC4002
C4011
AC4010
C4010
AC4005
C4012
AC4036
C4014
AC4040
C4013
AC4021
C4015
AC4041
AR4008
AR4007
CODEC_PD#_G
Q4001
MMBT3904WT1G
AZ_RST#_1
C4016
AC4003
AC4014
AC4046
C4017
CODEC_PD#
ALC298_MIC1_CAP
[42] DMIC1_CLK_CODEC
[42] DMIC1_DATA_CODEC
CPVEE
CPVPP
AR4018
AR4009
[10] PCH_CODEC_IRQ
AR4003
AR4002
AR4001
JP4001
JP4002
JP4003
SHORT PIN
AC4017
AC4018
CODEC_CBN1_R
CODEC_CBP1_R
CODEC_CBN2_R
CODEC_CBP2_R
AR4019
AR4006
AR4033
AC4038
HPOUT_JD_R
HPOUT_JD [41,76]
VREF
VREF1
AVDD1
PCBEEP
PVDD1
PVDD2
DVDD
DVDD_IO
CPVDD/AVDD2
CPVEE
CPVPP
CPVREF
DMIC_CLK
DMIC_DATA1
MIC1_CAP
EAPD+PD#/GPIO11
HD_I2S_SEL/IRQOUT/GPIO0
I2S_IN/GPIO5
I2S_OUT/GPIO6
I2S_BCLK/GPIO7
I2S_MCLK/SPDIF_IN/GPIO8
I2S_LRCK/GPIO9
GPIO1/DMIC_CLK2/SPDIF_OUT/I2S_IN_JD
GPIO2/DMIC_DATA2/I2S_OUT_JD
CBN1
CNB2
CBP1
CBP2
HDA_BCLK/I2S_BCLK
HDA_RESETB/I2S_MCLK
HDA_SDATA_IN/I2S_SDO
HDA_SDATA_OUT/I2S_SDI
HAD_SYNC/I2S_LRCK
HP_JD/LINE1_JD
HP_OUT_L
HP_OUT_R
I2C_CLK
I2C_DATA
I2S_OUT_JD/MIC_JD
LDO1_CAP
LDO2_CAP
LDO3_CAP
LINE1_L
LINE1_R
LINE1_VREFO
MIC1_L/RING2
MIC1_R/SLEEVE
MIC1_VREFO_L/AGPO_0
MIC1_VREFO_R/AGPO_1
SPK_OUT_LN
SPK_OUT_LP
SPK_OUT_RN
SPK_OUT_RP
AVSS1
AVSS2
VD33STB
E_PAD
SDATA_IN_R
AR4004
HPOUT_L [41]
HPOUT_R [41]
COMBO_JACK [41]
CODEC_LDO1
CODEC_LDO2
CODEC_LDO3
MIC1_L [41]
MIC1_R [41]
MIC1_VREFO_L [41]
SPK_L- [41]
SPK_L+ [41]
SPK_R- [41]
SPK_R+ [41]
AR4035
AR4036
ALC298_VD22STB
AZ_BITCLK_1 [20]
AZ_RST#_1 [20]
AZ_SDATA_IN0 [20]
AZ_SDATA_OUT_1 [20]
AZ_SYNC_1 [20]
Title: Realtek ALC3269 CODEC
<OrgName>
Engineer:
<OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 40 of 76

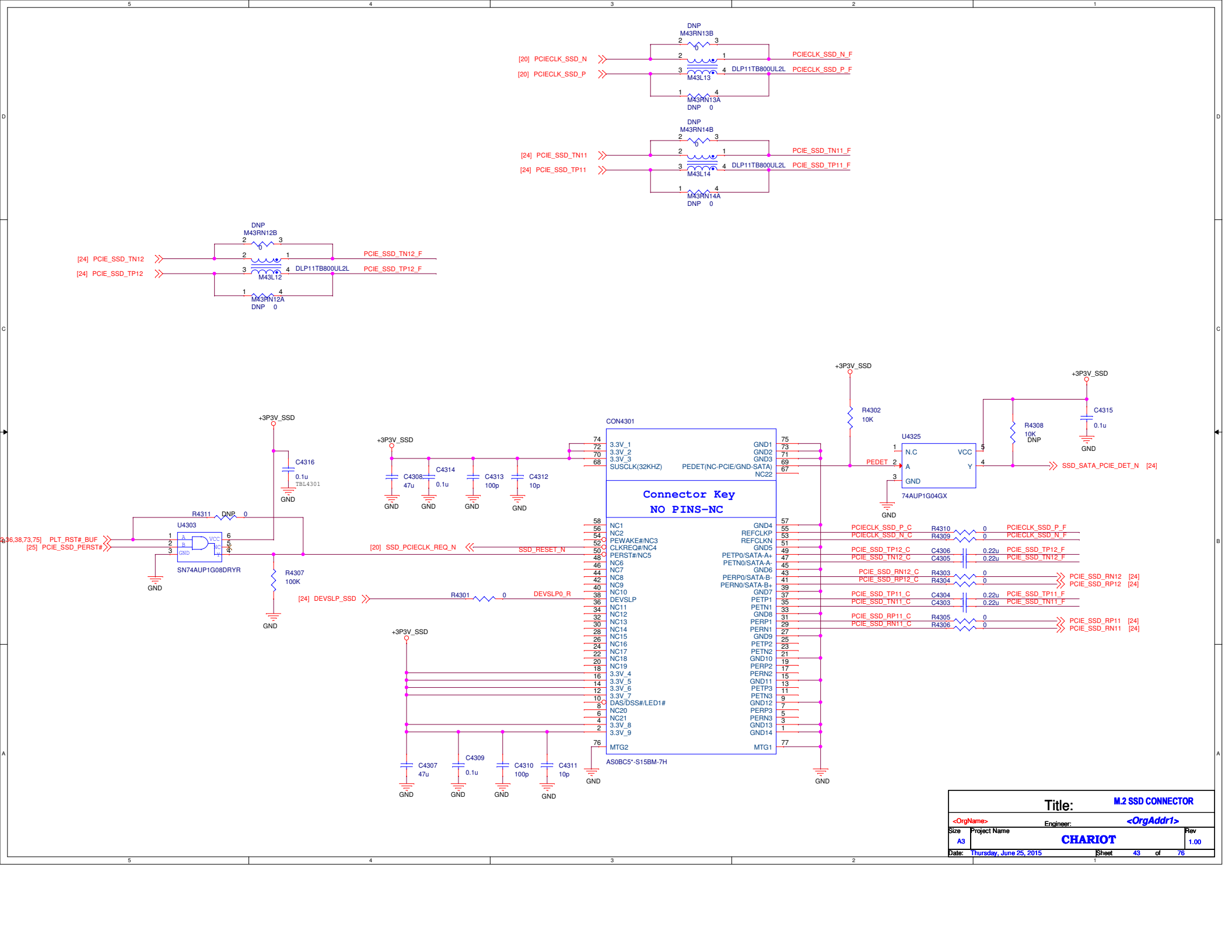
HP/MIC1 Combo Jack



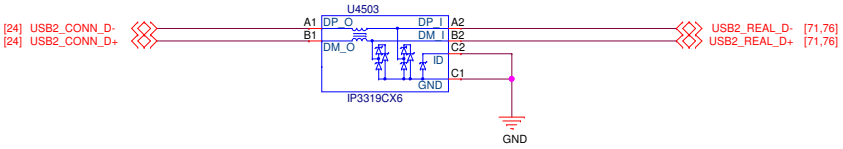
Title:	Audio Jack/Vol Button/Speaker		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 41 of 76		



Title:	DMIC CONN		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 42 of 76		


DNP
M43RN13B
[20] PCIECLK_SSD_N
[20] PCIECLK_SSD_P
PCIECLK_SSD_N_F
PCIECLK_SSD_P_F
M43L13
DLP11TB800UL2L
M43RN13A
DNP 0
DNP
M43RN14B
[24] PCIE_SSD_TN11
[24] PCIE_SSD_TP11
PCIE_SSD_TN11_F
PCIE_SSD_TP11_F
M43L14
M43RN14A
DNP 0
DNP
M43RN12B
[24] PCIE_SSD_TN12
[24] PCIE_SSD_TP12
PCIE_SSD_TN12_F
PCIE_SSD_TP12_F
M43L12
M43RN12A
DNP 0
+3P3V_SSD
R4302
10K
U4325
N.C
VCC
A
Y
GND
PEDET
74AUP1G04GX
R4308
10K
DNP
C4315
0.1u
SSD_SATA_PCIE_DET_N [24]
C4316
0.1u
TBL4301
R4311 DNP 0
U4303
[36,38,73,75] PLT_RST#_BUF
[25] PCIE_SSD_PERST#
SN74AUP1G08DRYR
R4307
100K
CON4301
C4308
47u
C4314
0.1u
C4313
100p
C4312
10p
Connector Key
NO PINS-NC
3.3V_1
3.3V_2
3.3V_3
SUSCLK(32KHZ)
PEDET(NC-PCIE/GND-SATA)
NC22
GND1
GND2
GND3
NC1
NC2
PEWAKE#/NC3
CLKREQ#/NC4
PERST#/NC5
NC6
NC7
NC8
NC9
NC10
DEVSLP
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
3.3V_4
3.3V_5
3.3V_6
3.3V_7
DAS/DSS#/LED1#
NC20
NC21
3.3V_8
3.3V_9
MTG2
MTG1
GND4
REFCLKP
REFCLKN
GND5
PETP0/SATA-A+
PETN0/SATA-A-
GND6
PERP0/SATA-B-
PERN0/SATA-B+
GND7
PETP1
PETN1
GND8
PERP1
PERN1
GND9
PETP2
PETN2
GND10
PERP2
PERN2
GND11
PETP3
PETN3
GND12
PERP3
PERN3
GND13
GND14
AS0BC5*-S15BM-7H
[20] SSD_PCIECLK_REQ_N
SSD_RESET_N
[24] DEVSLP_SSD
R4301 0 DEVSLP0_R
PCIECLK_SSD_P_C
PCIECLK_SSD_N_C
R4310 0 PCIECLK_SSD_P_F
R4309 0 PCIECLK_SSD_N_F
PCIE_SSD_TP12_C
PCIE_SSD_TN12_C
C4306 0.22u PCIE_SSD_TP12_F
C4305 0.22u PCIE_SSD_TN12_F
PCIE_SSD_RN12_C
PCIE_SSD_RP12_C
R4303 0 PCIE_SSD_RN12 [24]
R4304 0 PCIE_SSD_RP12 [24]
PCIE_SSD_TP11_C
PCIE_SSD_TN11_C
C4304 0.22u PCIE_SSD_TP11_F
C4303 0.22u PCIE_SSD_TN11_F
PCIE_SSD_RP11_C
PCIE_SSD_RN11_C
R4305 0 PCIE_SSD_RP11 [24]
R4306 0 PCIE_SSD_RN11 [24]
C4307
47u
C4309
0.1u
C4310
100p
C4311
10p
GND
Title: M.2 SSD CONNECTOR
<OrgName>
Engineer:
<OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 43 of 76

Title:			X
<OrgName>	Engineer:		<OrgAddr1>
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015		Sheet 44 of 76	

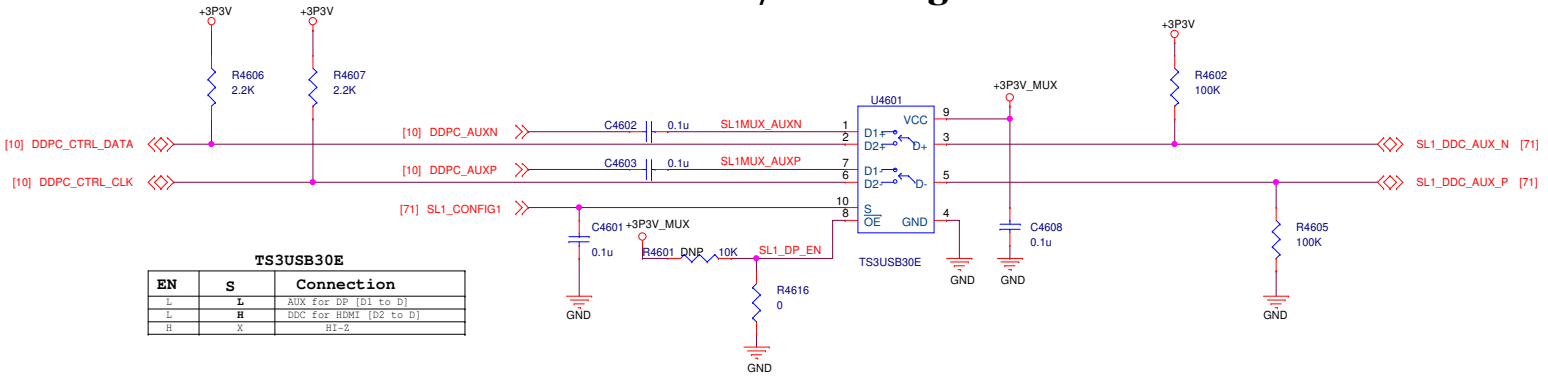


Note: IP3319CX6 D+ and D- is interchageable as seen in data sheet. Flipped for layout convenience.

Title:	USB3.0	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 45 of 76	

when you TI ts3usb30e (X870617-001), NIR4613 and R4601 and install R4615 and R4616

SL1 DP mux to HDMI/DVI Dongle control



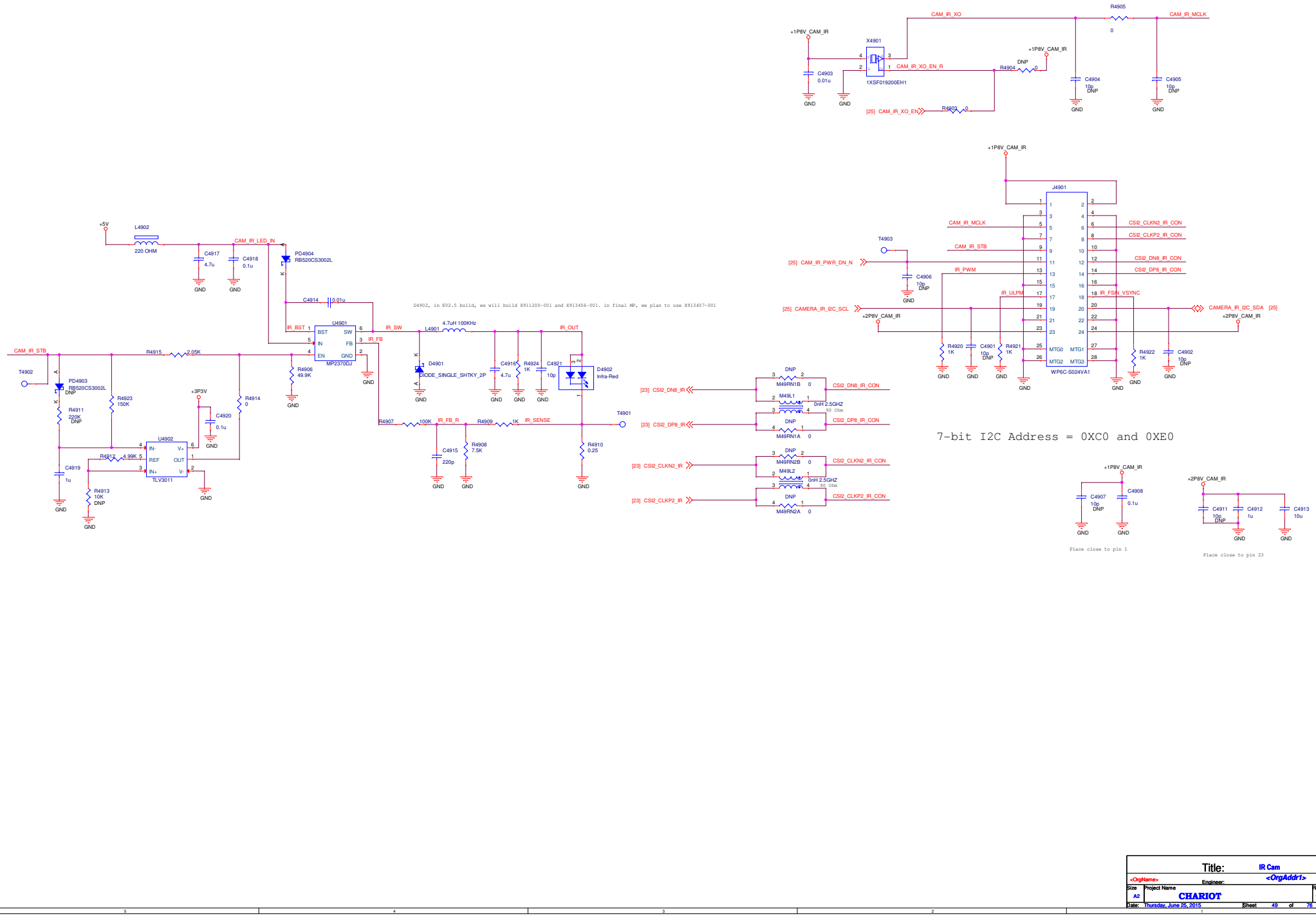
TS3USB30E

EN	S	Connection
L	L	AUX for DP [D1 to D]
L	H	DDC for HDMI [D2 to D]
H	X	HI-Z

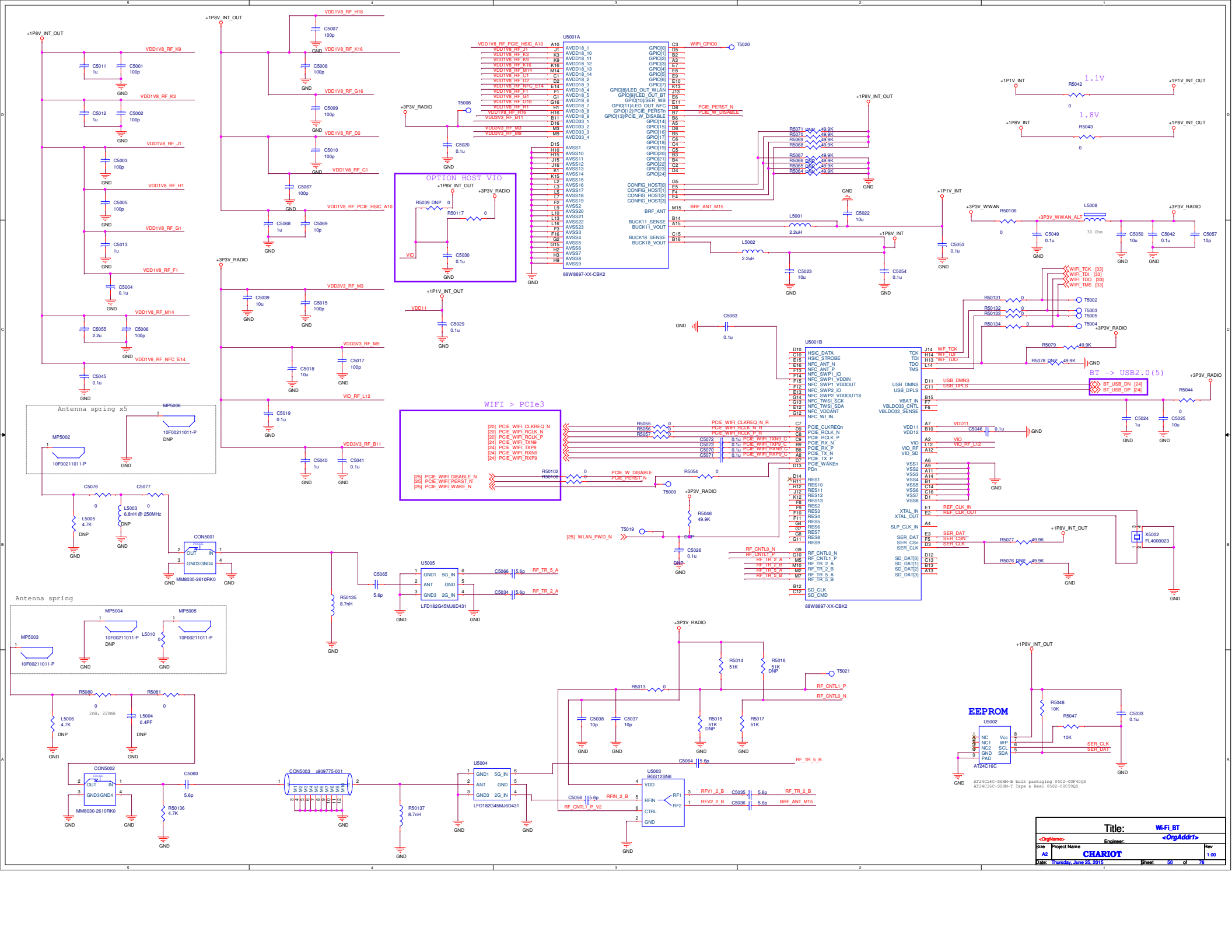
Title:	DP Dongle Control	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 46 of 76	

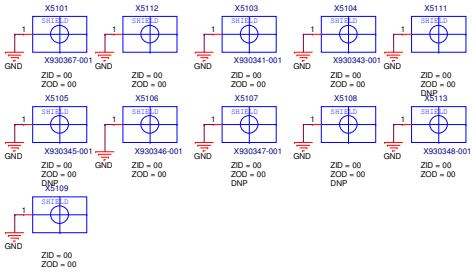
Title:	mDP		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 47 of 76		

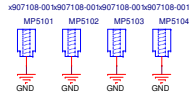
Title:	X		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 48 of 76		

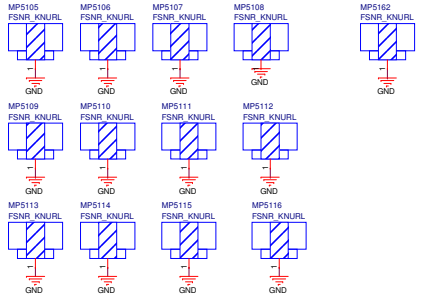


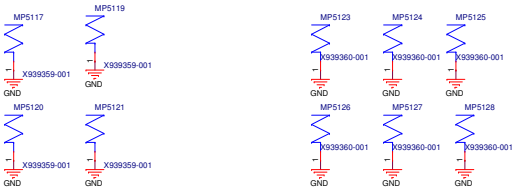
Title:	IR Cam	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 49 of 76	

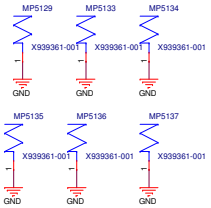

OPTION HOST VIO
WIFI > PCIe3
Antenna spring x5
Antenna spring
EEPROM
BT -> USB2.0(5)
U5001A
88W8897-XX-CBK2
U5001B
88W8897-XX-CBK2
U5005
LFD182G45MJ6D431
U5004
LFD182G45MJ6D431
U5003
BGS12SN6
U5002
AT24C16C
CON5001
MM8030-2610RK0
CON5002
MM8030-2610RK0
CON5003 x909775-001
X5002
FL4000023
Title: Wi-Fi_BT
<OrgName>
Engineer:
<OrgAddr1>
Size: A2
Project Name: CHARIOT
Rev: 1.00
Date: Thursday, June 25, 2015
Sheet 50 of 76



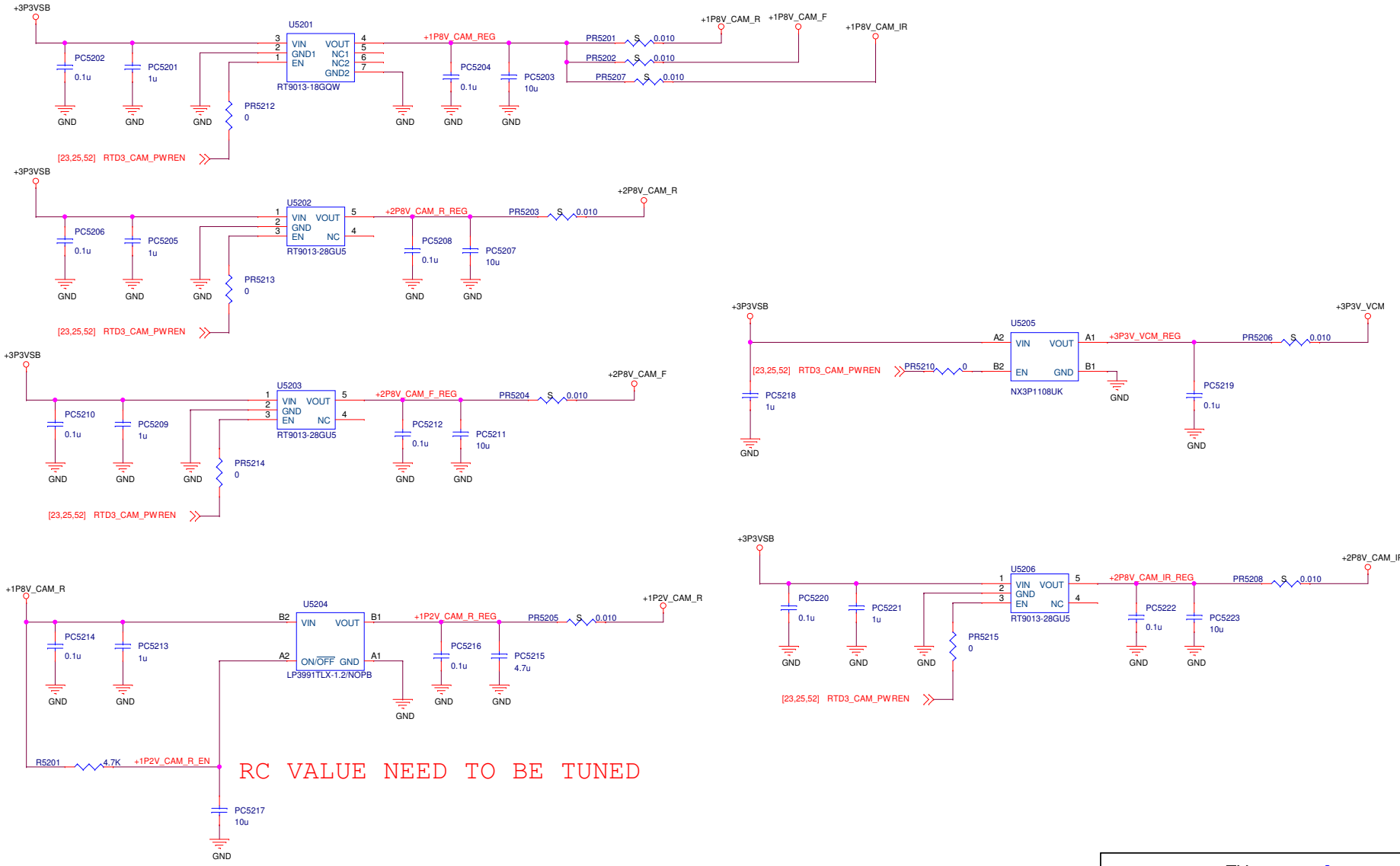




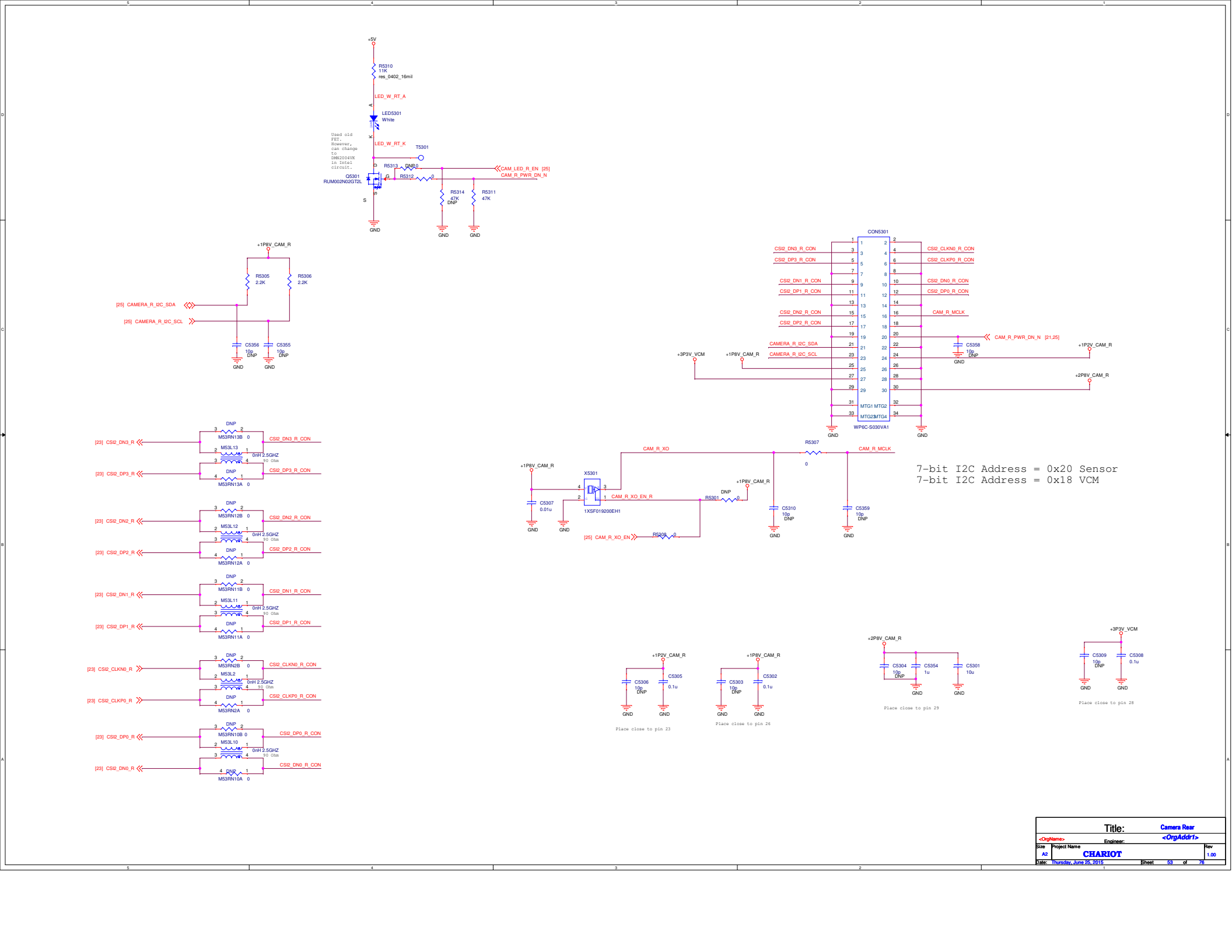




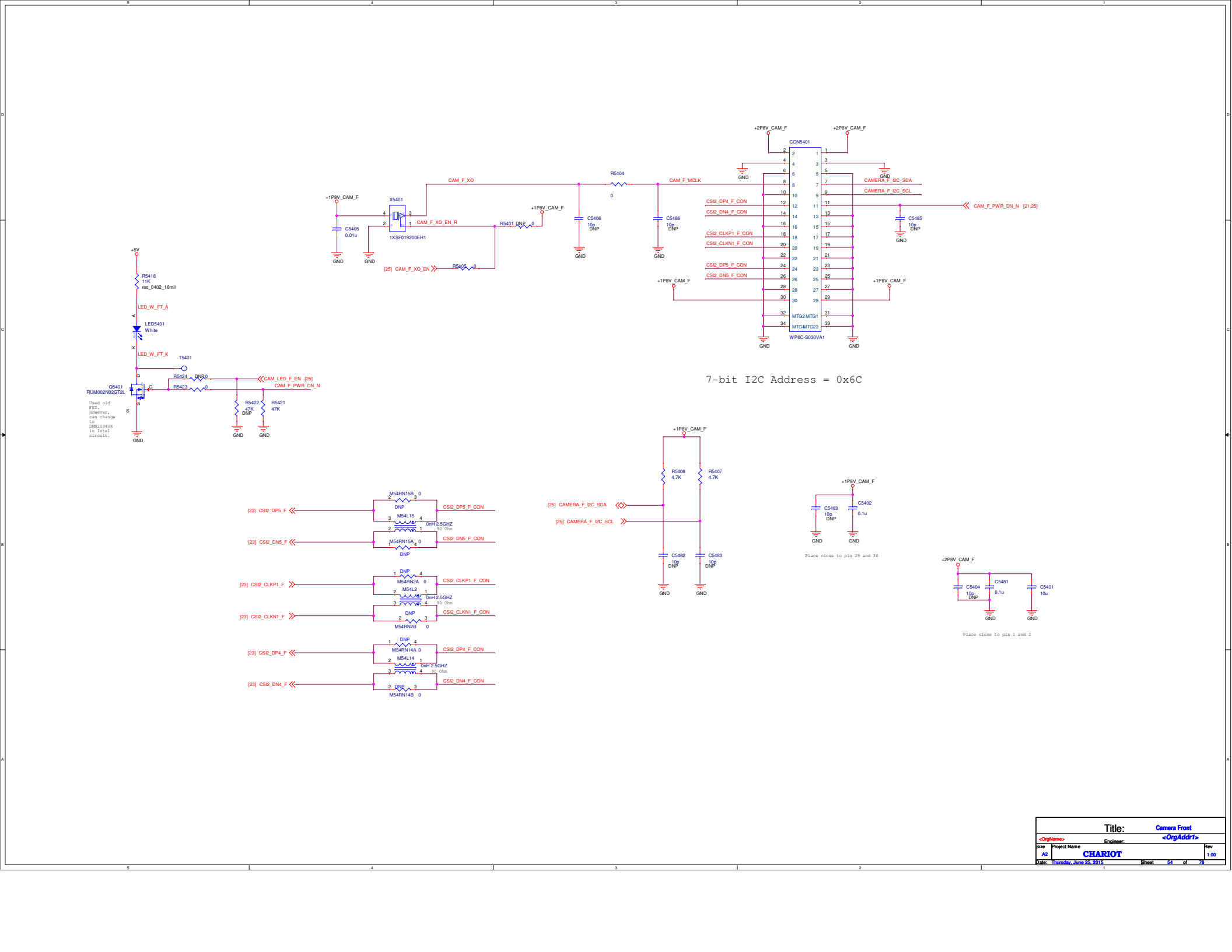
Title:	Components for ME/EMI		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 51 of 76		



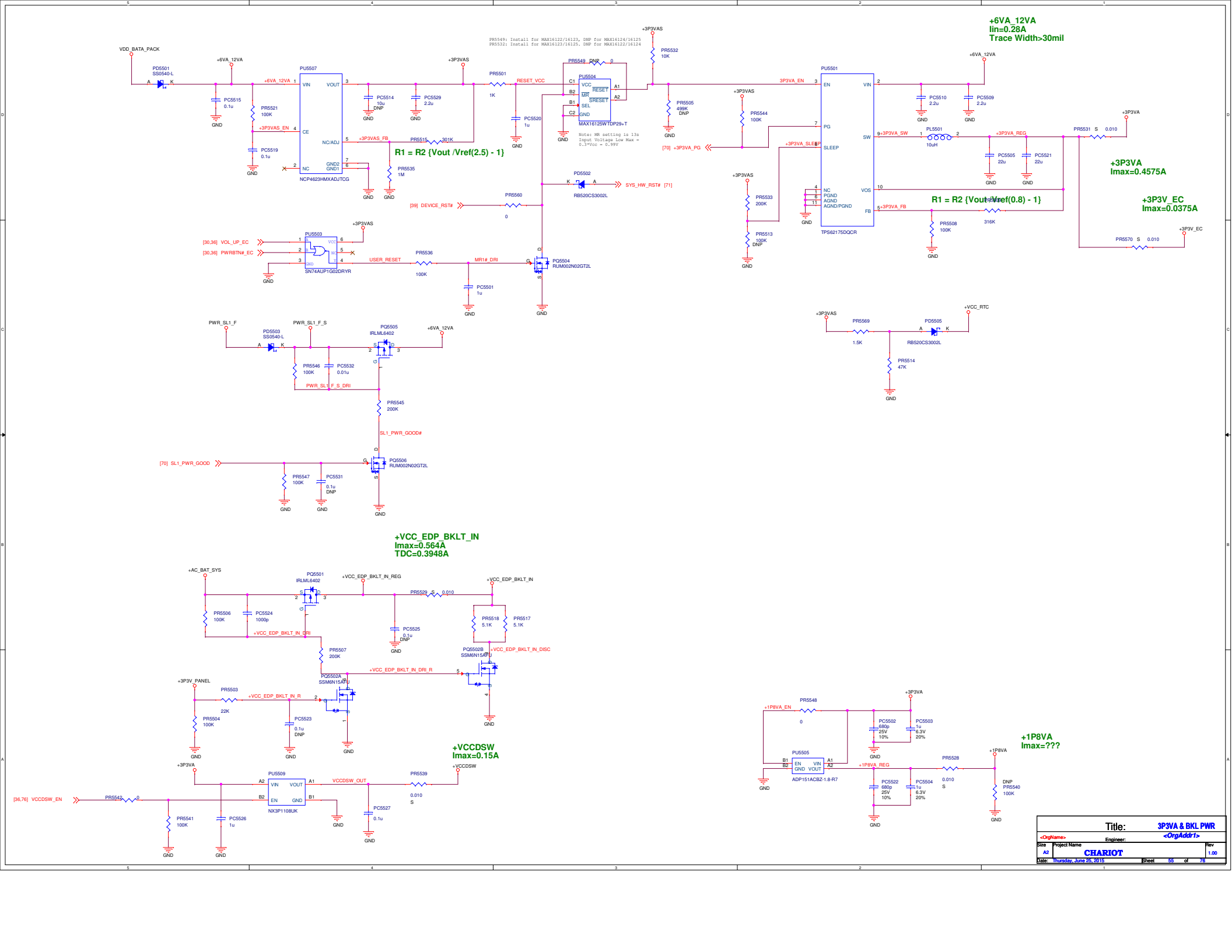
Title:	Camera power	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 52 of 76	

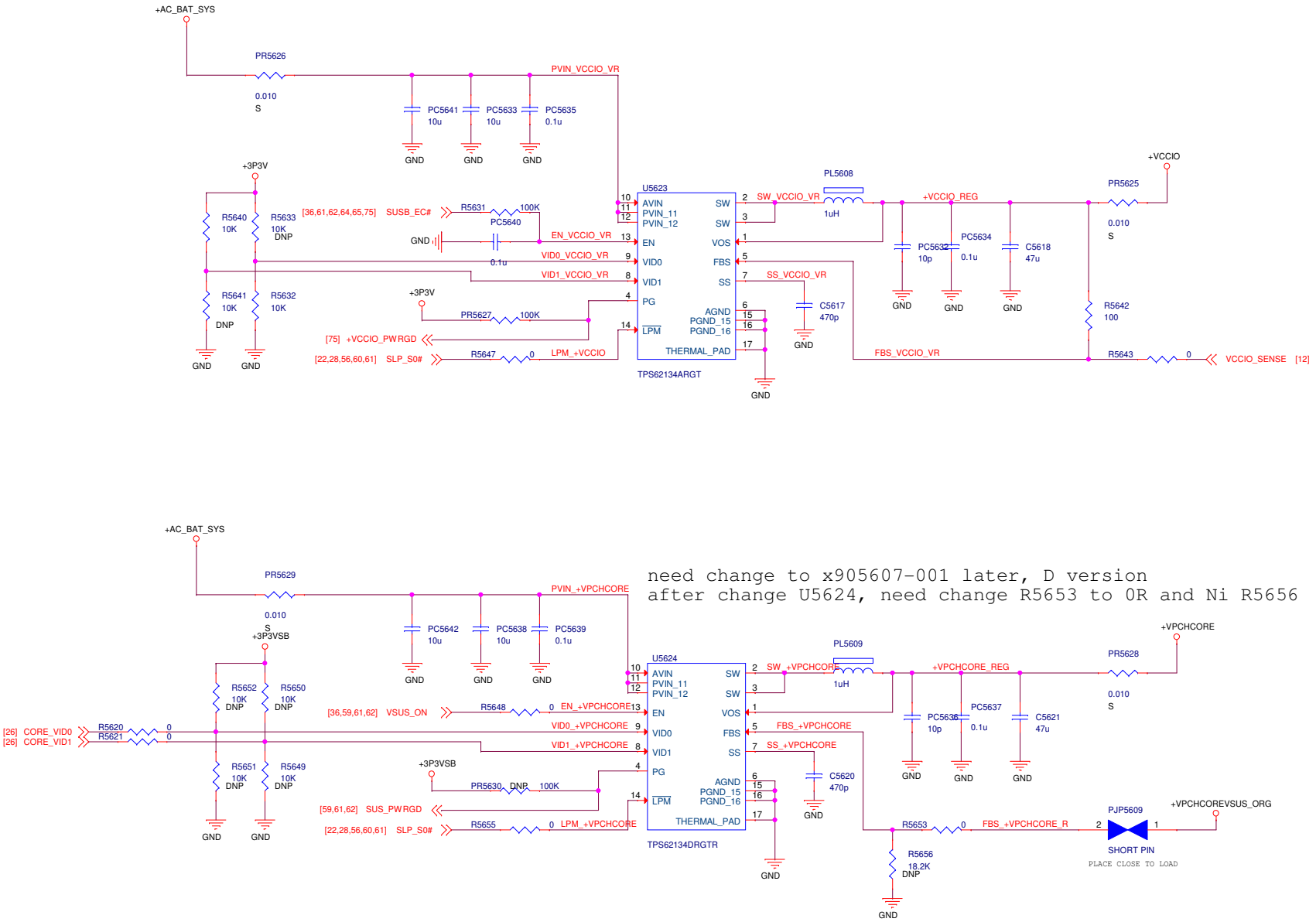


Title:	Camera Rear	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 53 of 76	



Title:	Camera Front	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 54 of 76	

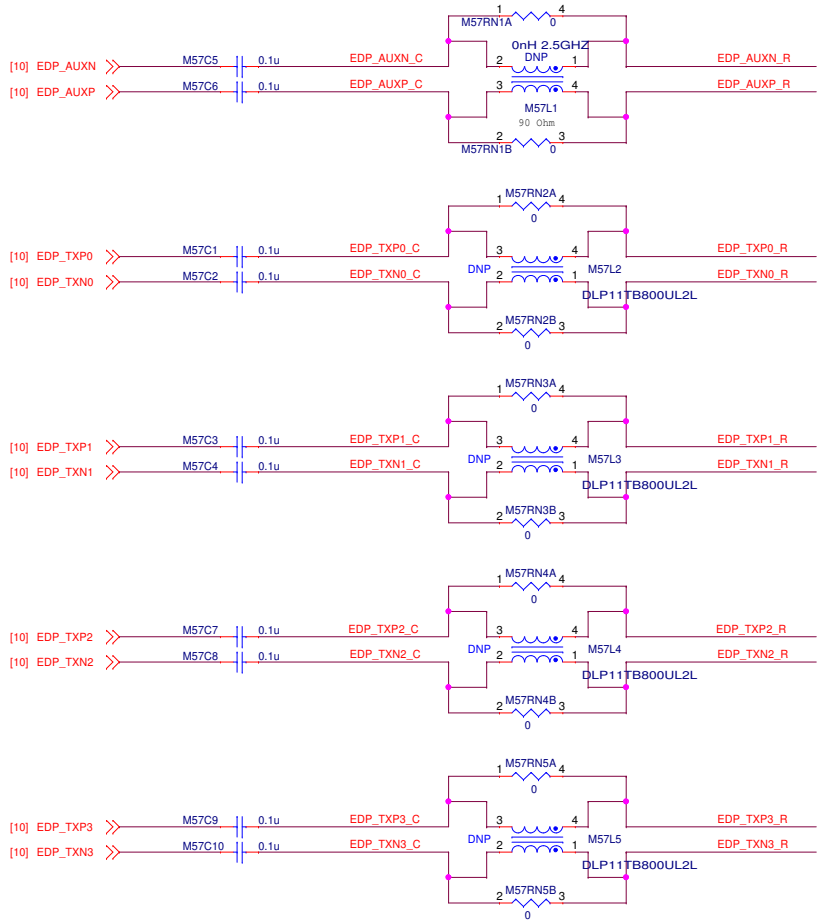

+6VA_12VA
Iin=0.28A
Trace Width>30mil
PR5549: Install for MAX16122/16123, DNP for MAX16124/16125
PR5532: Install for MAX16123/16125, DNP for MAX16122/16124
VDD_BATA_PACK
PD5501
SS0540-L
PC5515
0.1u
PR5521
100K
PU5507
NCP4623HMXADJTCG
PC5519
0.1u
PC5514
10u
DNP
PC5529
2.2u
PR5501
1K
PR5515
301K
PR5535
1M
R1 = R2 {Vout /Vref(2.5) - 1}
PC5520
1u
PR5549 DNP
PU5504
MAX16125WTDP29+T
Note: MR setting is 13s
Input Voltage Low Max =
0.3*Vcc = 0.99V
PR5532
10K
PR5505
499K
DNP
PD5502
RB520CS3002L
SYS_HW_RST# [71]
PR5560
0
[39] DEVICE_RST#
[70] +3P3VA_PG
PU5501
TPS62175DQCR
PR5544
100K
PR5533
200K
PR5513
100K
DNP
PC5510
2.2u
PC5509
2.2u
PL5501
10uH
PC5505
22u
PC5521
22u
PR5531
0.010
+3P3VA
Imax=0.4575A
+3P3V_EC
Imax=0.0375A
R1 = R2 {Vout /Vref(0.8) - 1}
PR5508
100K
316K
PR5570
0.010
[30,36] VOL_UP_EC
[30,36] PWRBTN#_EC
PU5503
SN74AUP1G02DRYR
USER_RESET
PR5536
100K
MR1#_DRI
PQ5504
RUM002N02GT2L
PC5501
1u
PWR_SL1_F
PWR_SL1_F_S
PD5503
SS0540-L
PQ5505
IRLML6402
PR5546
100K
PC5532
0.01u
PWR_SL1_F_S_DRI
PR5545
200K
SL1_PWR_GOOD#
[70] SL1_PWR_GOOD
PQ5506
RUM002N02GT2L
PR5547
100K
PC5531
0.1u
DNP
PR5569
1.5K
PD5505
RB520CS3002L
PR5514
47K
+VCC_EDP_BKLT_IN
Imax=0.564A
TDC=0.3948A
+AC_BAT_SYS
PQ5501
IRLML6402
+VCC_EDP_BKLT_IN_REG
PR5529
0.010
PR5506
100K
PC5524
1000p
+VCC_EDP_BKLT_IN_DRI
PR5507
200K
PC5525
0.1u
DNP
PR5518
5.1K
PR5517
5.1K
PQ5502B
SSM6N15AFU
+VCC_EDP_BKLT_IN_DISC
PQ5502A
SSM6N15AFU
+VCC_EDP_BKLT_IN_DRI_R
+3P3V_PANEL
PR5503
22K
+VCC_EDP_BKLT_IN_R
PR5504
100K
PC5523
0.1u
DNP
+VCCDSW
Imax=0.15A
PU5509
NX3P1108UK
VCCDSW_OUT
PR5539
0.010
[36,76] VCCDSW_EN
PR5542
0
PR5541
100K
PC5526
1u
PC5527
0.1u
PR5548
+1P8VA_EN
0
PC5502
680p
25V
10%
PC5503
1u
6.3V
20%
PU5505
ADP151ACBZ-1.8-R7
+1P8VA_REG
PR5528
0.010
PC5522
680p
25V
10%
PC5504
1u
6.3V
20%
PR5540
100K
DNP
+1P8VA
Imax=???
Title: 3P3VA & BKL PWR
<OrgName>
Engineer:
<OrgAddr1>
Size A2
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 55 of 78

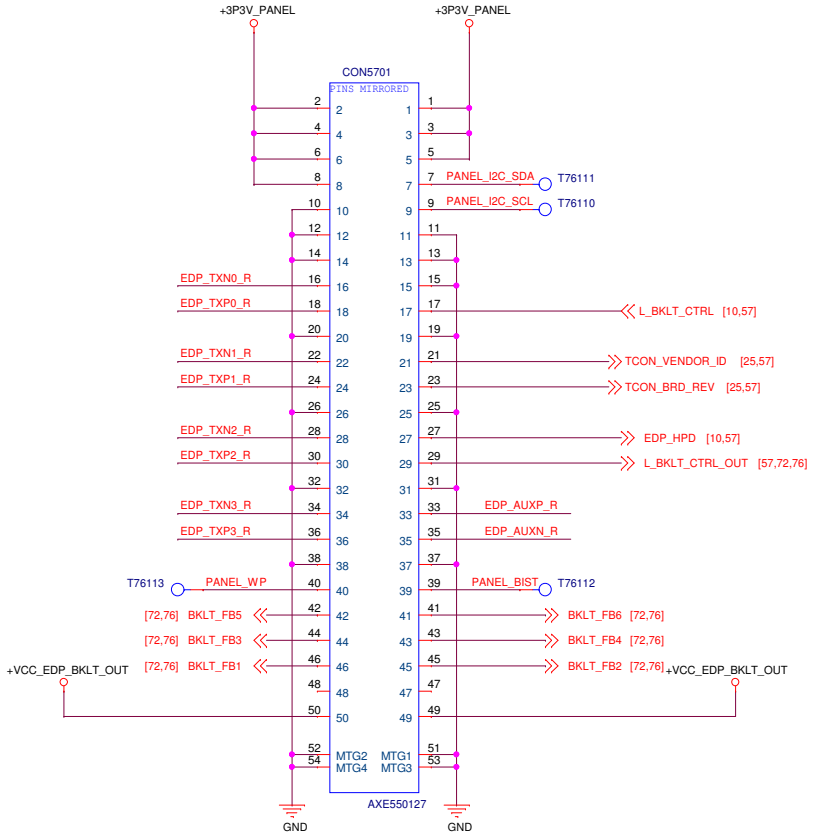


need change to x905607-001 later, D version
after change U5624, need change R5653 to 0R and Ni R5656

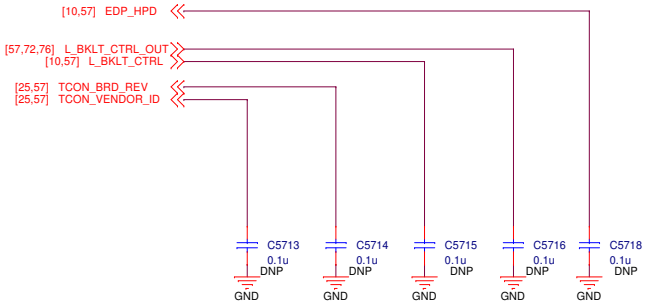
Title:	+VCCIO & 0P85VSB	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 56 of 76	

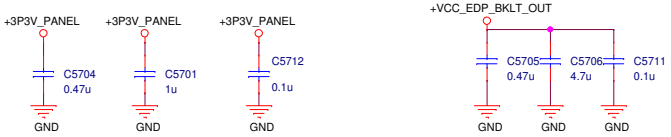
[1/7] Change M57L1, M57L2, M57L3, M57L4 and M57L5 to 0R



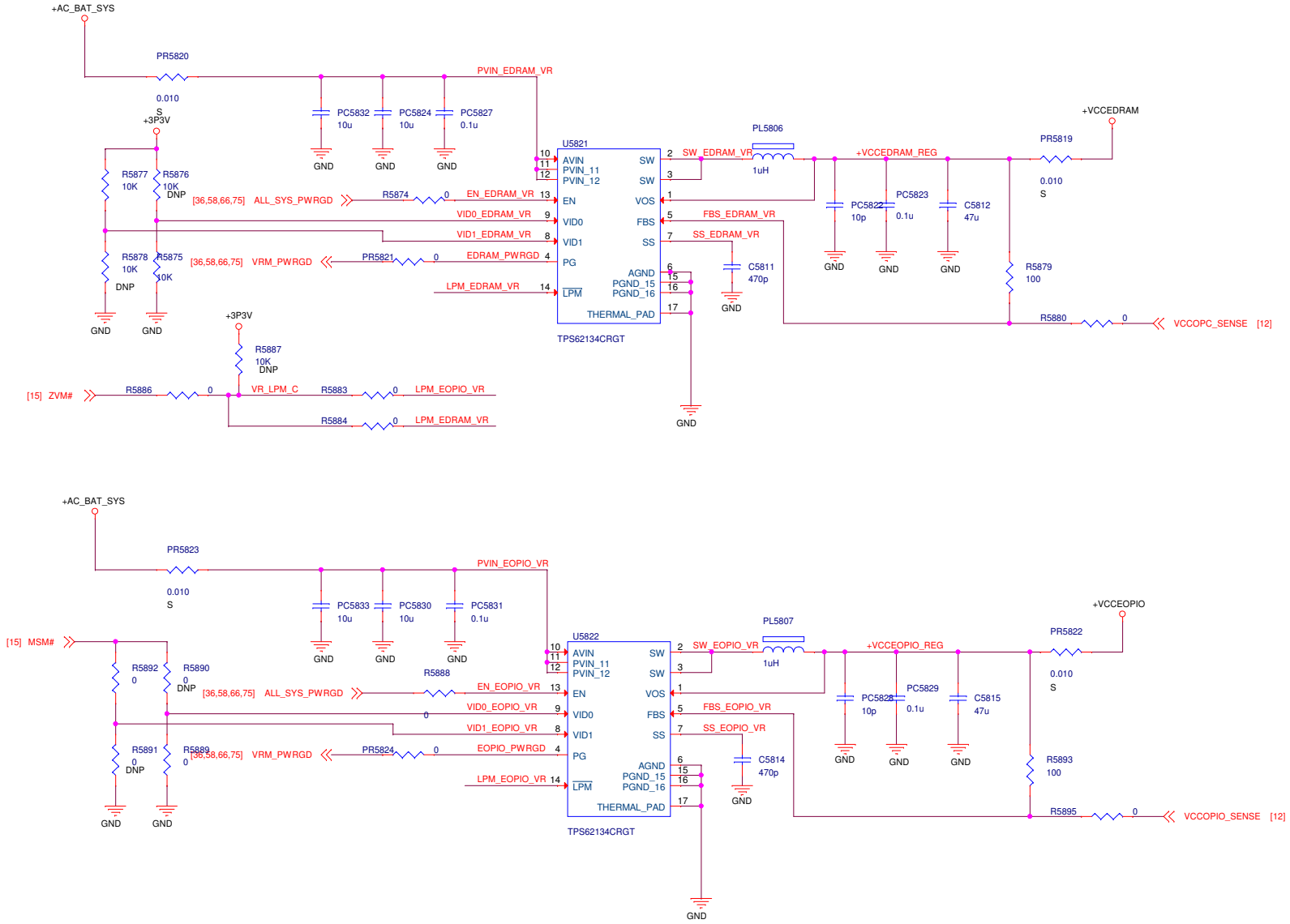


double check the connection to LCD



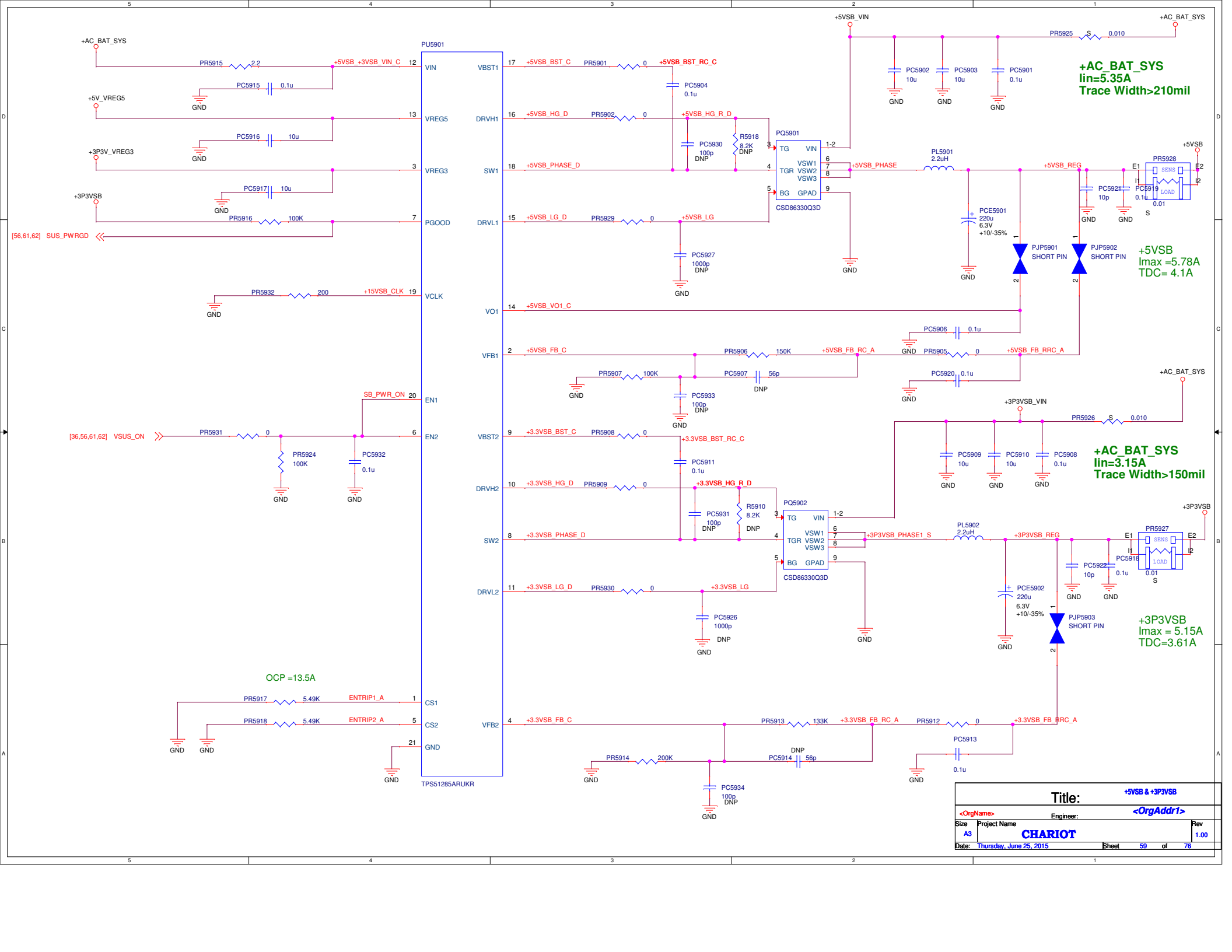


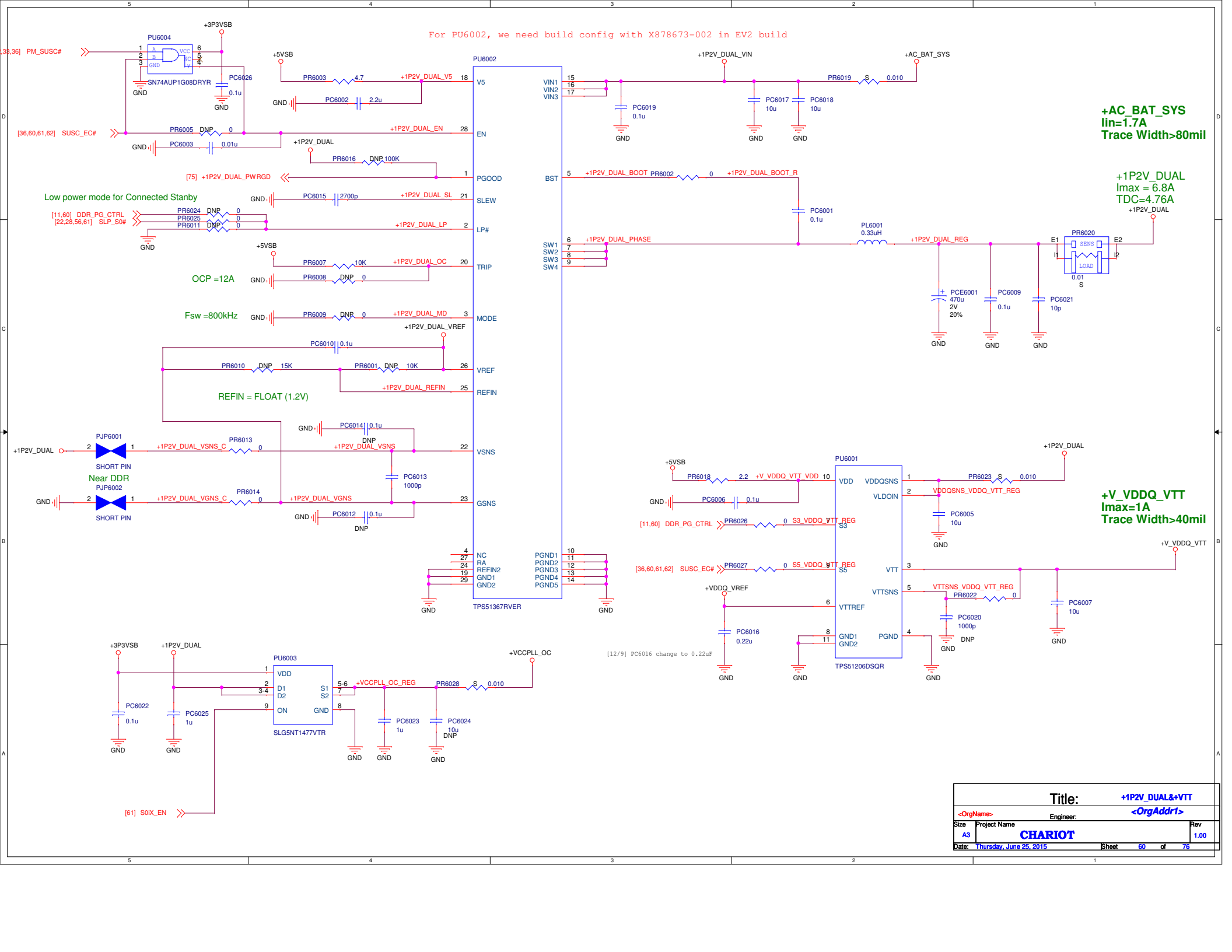
Title:	eDP connector	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 57 of 76	

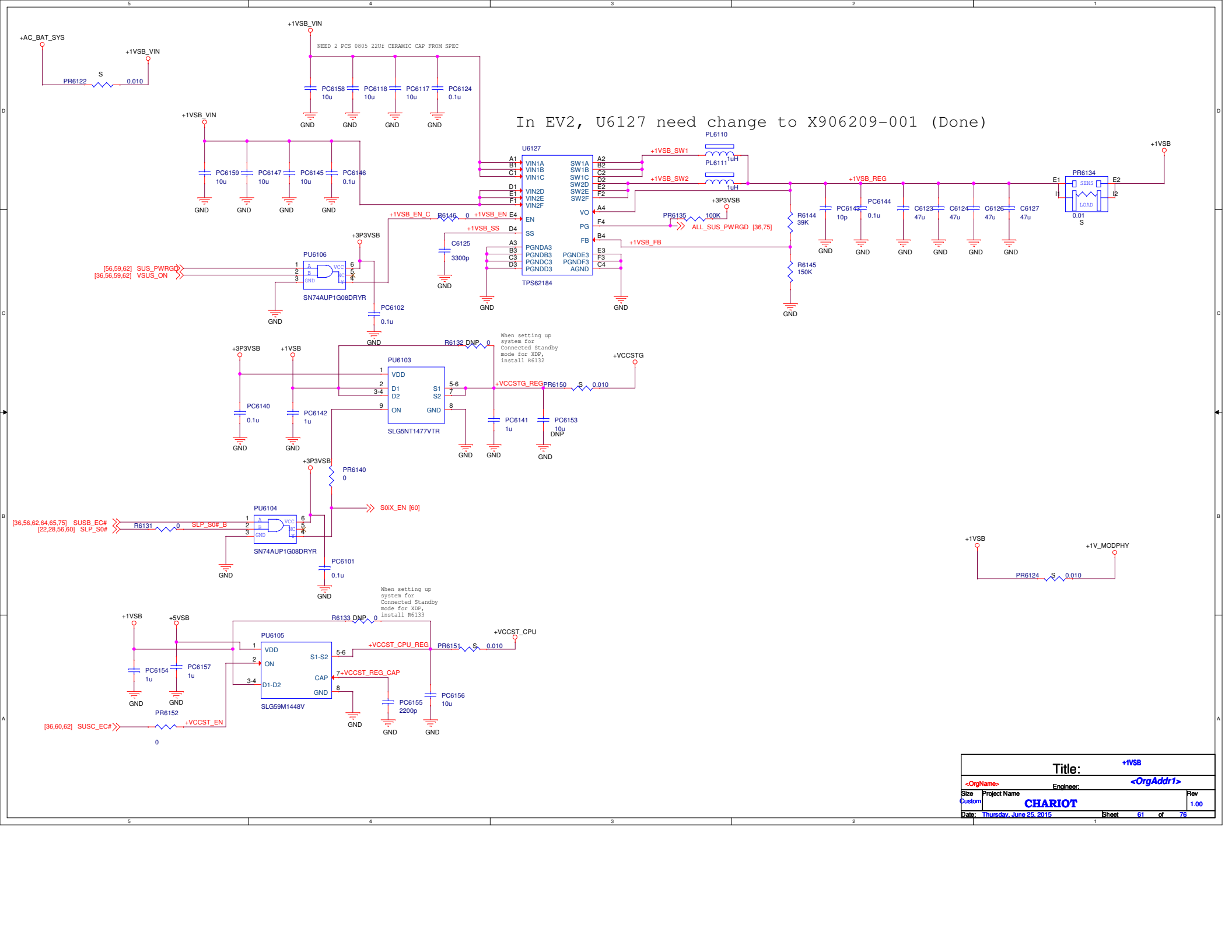


No Install all of part in this page when use GT2

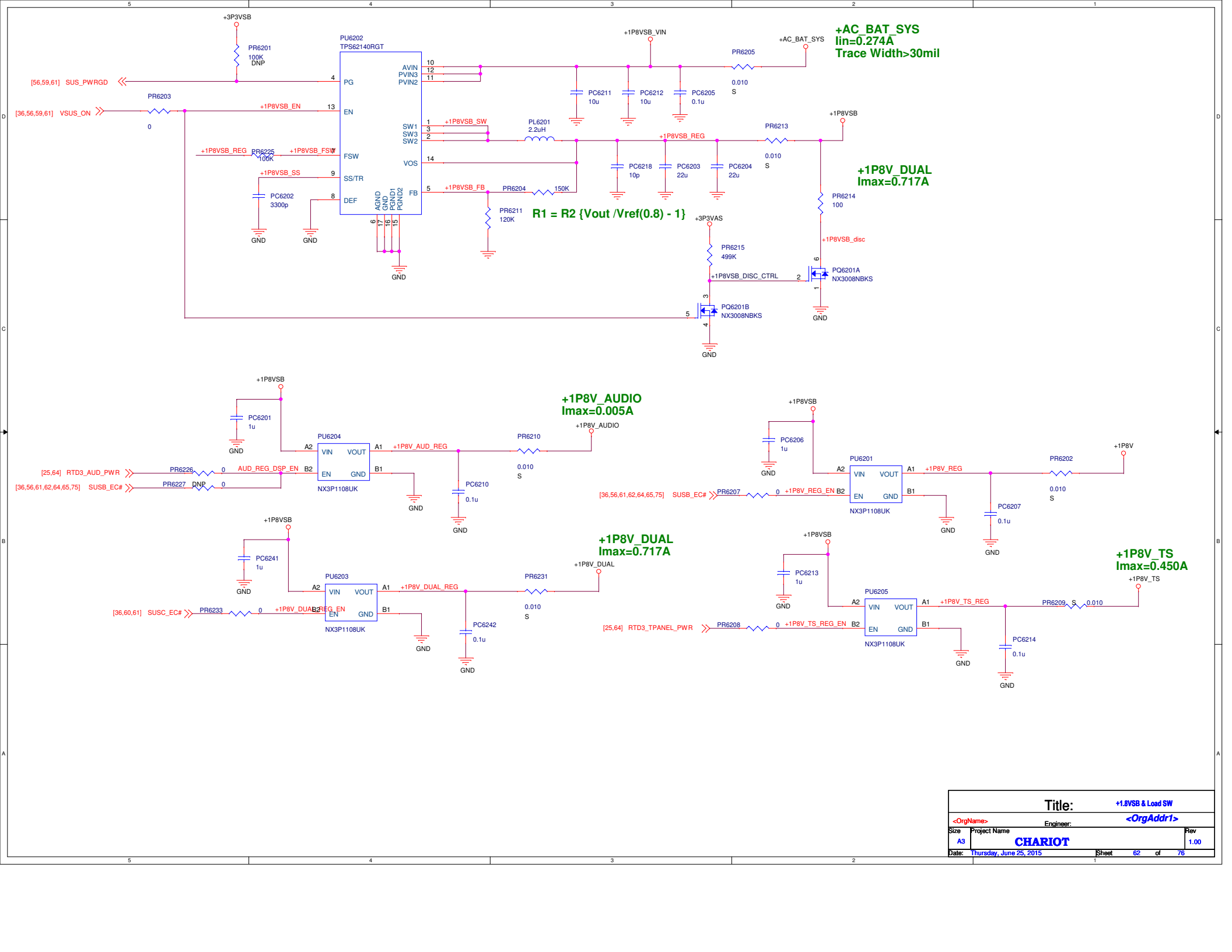
Title: +VCCEDRAM & +VCCEOPIO			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 58 of 76		

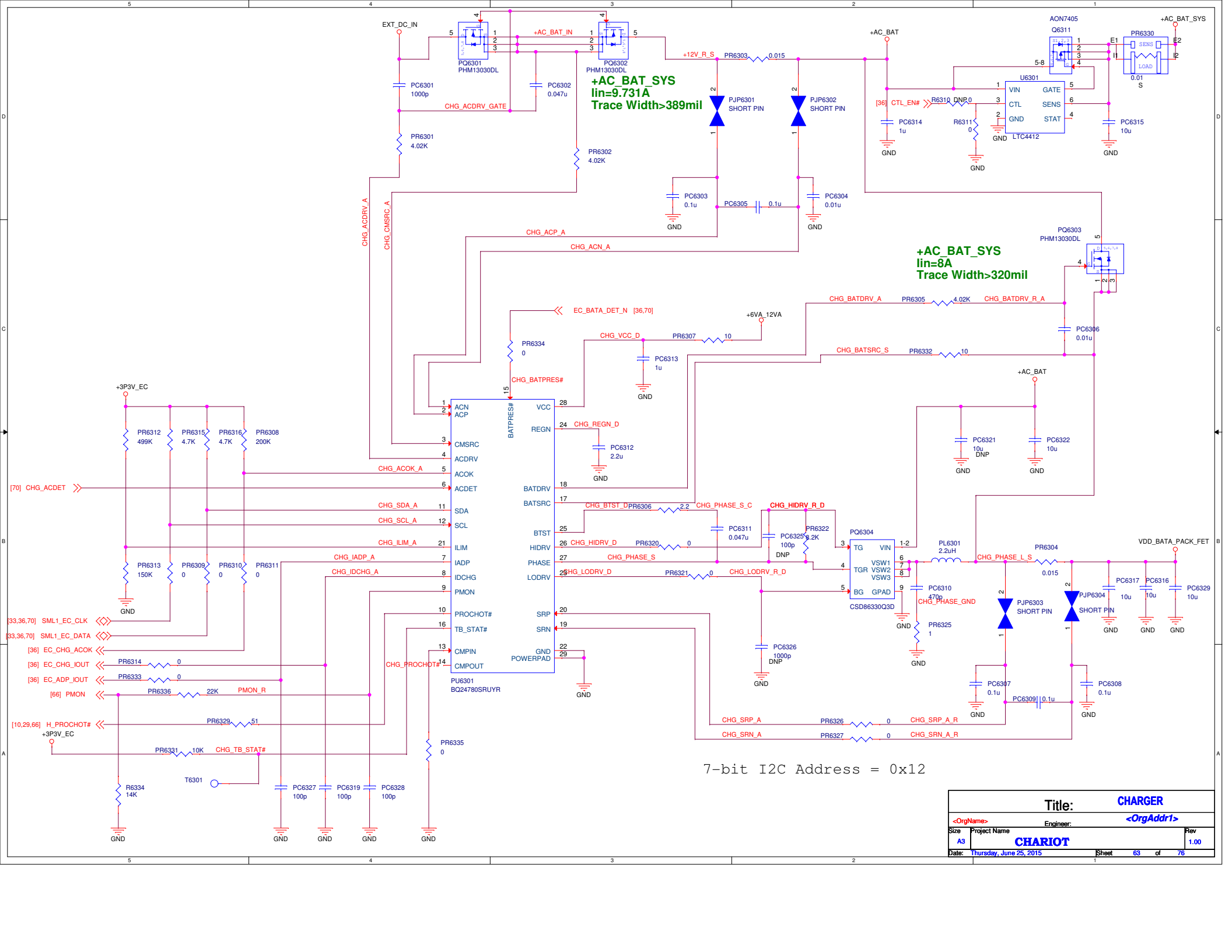

+AC_BAT_SYS
PR5915 2.2
+5VSB_+3VSB_VIN_C
PC5915 0.1u
GND
+5V_VREG5
PC5916 10u
+3P3V_VREG3
PC5917 10u
+3P3VSB
PR5916 100K
[56,61,62] SUS_PWRGD
PR5932 200
+15VSB_CLK
SB_PWR_ON
[36,56,61,62] VSUS_ON
PR5931 0
PR5924 100K
PC5932 0.1u
OCP =13.5A
PR5917 5.49K
ENTRIP1_A
PR5918 5.49K
ENTRIP2_A
PU5901
VIN
VREG5
VREG3
PGOOD
VCLK
EN1
EN2
CS1
CS2
GND
TPS51285ARUKR
VBST1
DRVH1
SW1
DRVL1
VO1
VFB1
VBST2
DRVH2
SW2
DRVL2
VFB2
+5VSB_BST_C
PR5901 0
+5VSB_BST_RC_C
PC5904 0.1u
+5VSB_HG_D
PR5902 0
+5VSB_HG_R_D
PC5930 100p DNP
R5918 8.2K DNP
+5VSB_PHASE_D
+5VSB_LG_D
PR5929 0
+5VSB_LG
PC5927 1000p DNP
+5VSB_VO1_C
+5VSB_FB_C
PR5906 150K
+5VSB_FB_RC_A
PR5907 100K
PC5907 56p DNP
PC5933 100p DNP
+3.3VSB_BST_C
PR5908 0
+3.3VSB_BST_RC_C
PC5911 0.1u
+3.3VSB_HG_D
PR5909 0
+3.3VSB_HG_R_D
PC5931 100p DNP
R5910 8.2K DNP
+3.3VSB_PHASE_D
+3.3VSB_LG_D
PR5930 0
+3.3VSB_LG
PC5926 1000p DNP
+3.3VSB_FB_C
PR5913 133K
+3.3VSB_FB_RC_A
PR5914 200K
PC5914 56p DNP
PC5934 100p DNP
PQ5901
PQ5902
TG
TGR
BG
VIN
VSW1
VSW2
VSW3
GPAD
CSD86330Q3D
PL5901 2.2uH
PL5902 2.2uH
+5VSB_PHASE
+3P3VSB_PHASE1_S
PCE5901 220u 6.3V +10/-35%
PCE5902 220u 6.3V +10/-35%
PJP5901 SHORT PIN
PJP5902 SHORT PIN
PJP5903 SHORT PIN
+5VSB_REG
+3P3VSB_REG
PR5928
PR5927
SENS
LOAD
0.01
PC5921 10p
PC5919 0.1u
PC5922 10p
PC5918 0.1u
+5VSB_VIN
PR5925 S 0.010
PC5902 10u
PC5903 10u
PC5901 0.1u
+AC_BAT_SYS
lin=5.35A
Trace Width>210mil
+5VSB
Imax =5.78A
TDC= 4.1A
PC5906 0.1u
PR5905 0
+5VSB_FB_RRC_A
PC5920 0.1u
+3P3VSB_VIN
PR5926 S 0.010
PC5909 10u
PC5910 10u
PC5908 0.1u
+AC_BAT_SYS
lin=3.15A
Trace Width>150mil
+3P3VSB
Imax = 5.15A
TDC=3.61A
PR5912 0
+3.3VSB_FB_RRC_A
PC5913 0.1u
Title: +5VSB & +3P3VSB
<OrgName>
Engineer:
<OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 59 of 76

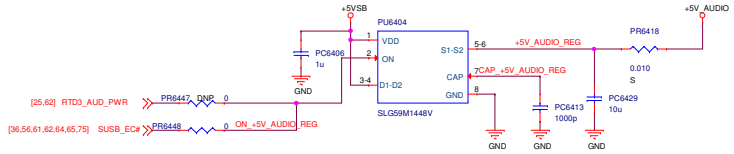

For PU6002, we need build config with X878673-002 in EV2 build
PU6004
SN74AUP1G08DRYR
PU6002
TPS51367RVER
+AC_BAT_SYS
Iin=1.7A
Trace Width>80mil
+1P2V_DUAL
Imax = 6.8A
TDC=4.76A
Low power mode for Connected Stanby
OCP =12A
Fsw =800kHz
REFIN = FLOAT (1.2V)
SHORT PIN
Near DDR
PU6001
TPS51206DSQR
+V_VDDQ_VTT
Imax=1A
Trace Width>40mil
[12/9] PC6016 change to 0.22uF
PU6003
SLG5NT1477VTR
Title: +1P2V_DUAL&+VTT
<OrgName>
Engineer:
<OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 60 of 76

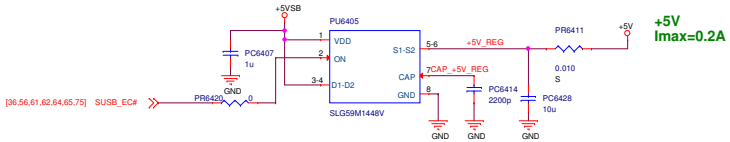


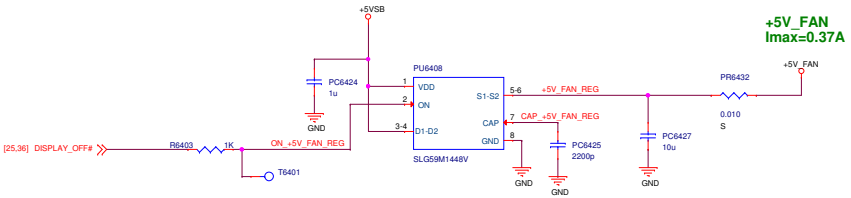
Title:	+1VSB		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 61 of 76		

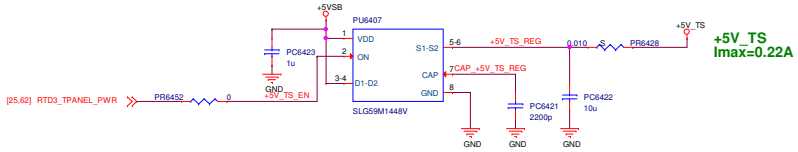

+AC_BAT_SYS
Iin=0.274A
Trace Width>30mil
+1P8V_DUAL
Imax=0.717A
R1 = R2 {Vout /Vref(0.8) - 1}
+1P8V_AUDIO
Imax=0.005A
+1P8V_DUAL
Imax=0.717A
+1P8V_TS
Imax=0.450A
PU6202
TPS62140RGT
PR6201
100K
DNP
PR6203
0
PR6205
0.010
S
PR6213
0.010
S
PR6214
100
PR6225
100K
PR6204
150K
PR6211
120K
PR6215
499K
PL6201
2.2uH
PC6202
3300p
PC6211
10u
PC6212
10u
PC6205
0.1u
PC6218
10p
PC6203
22u
PC6204
22u
PQ6201A
NX3008NBKS
PQ6201B
NX3008NBKS
+1P8VSB_VIN
+AC_BAT_SYS
+1P8VSB
+1P8VSB_REG
+1P8VSB_SW
+1P8VSB_FB
+1P8VSB_SS
+1P8VSB_FSW
+1P8VSB_EN
+1P8VSB_disc
+1P8VSB_DISC_CTRL
+3P3VSB
+3P3VAS
[56,59,61] SUS_PWRGD
[36,56,59,61] VSUS_ON
PG
EN
FSW
SS/TR
DEF
FB
VOS
SW1
SW3
SW2
AVIN
PVIN3
PVIN2
AGND
GND
PGND1
PGND2
PU6204
NX3P1108UK
PR6226
PR6227
PR6210
PC6201
1u
PC6210
0.1u
[25,64] RTD3_AUD_PWR
[36,56,61,62,64,65,75] SUSB_EC#
AUD_REG_DSP_EN
+1P8V_AUD_REG
+1P8V_AUDIO
PU6201
PR6207
PR6202
PC6206
1u
PC6207
0.1u
+1P8V_REG_EN
+1P8V_REG
+1P8V
PU6203
PR6233
PR6231
PC6241
1u
PC6242
0.1u
+1P8V_DUAL_REG_EN
+1P8V_DUAL_REG
PU6205
PR6208
PR6209
PC6213
1u
PC6214
0.1u
+1P8V_TS_REG_EN
+1P8V_TS_REG
+1P8V_TS
[36,60,61] SUSC_EC#
[25,64] RTD3_TPANEL_PWR
Title:
+1.8VSB & Load SW
<OrgName>
Engineer:
<OrgAddr1>
Size
A3
Project Name
CHARIOT
Rev
1.00
Date:
Thursday, June 25, 2015
Sheet
62
of
76

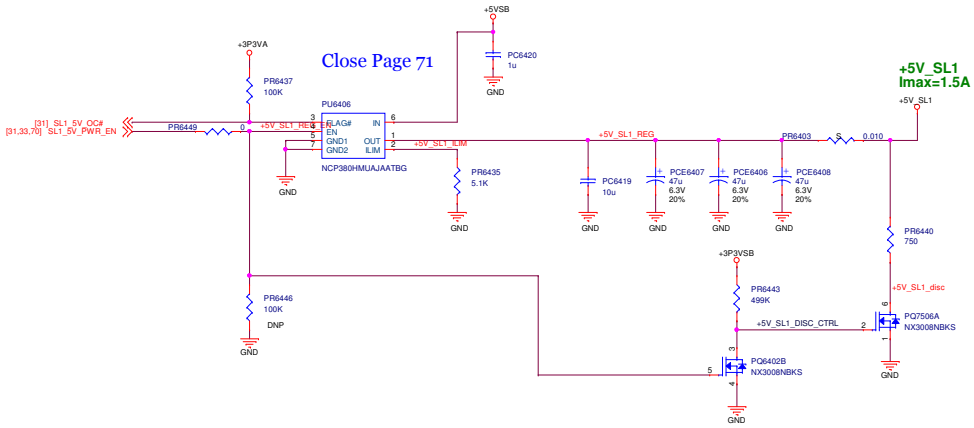

EXT_DC_IN
PQ6301 PHM13030DL
PQ6302 PHM13030DL
+AC_BAT_IN
+AC_BAT_SYS
Iin=9.731A
Trace Width>389mil
+12V_R_S
PR6303 0.015
PJP6301 SHORT PIN
PJP6302 SHORT PIN
+AC_BAT
AON7405
Q6311
PR6330 SENS LOAD 0.01 S
+AC_BAT_SYS
U6301 LTC4412
VIN GATE CTL SENS GND STAT
[36] CTL_EN#
R6310 DNP 0
R6311 0
PC6314 1u
PC6315 10u
PC6301 1000p
PC6302 0.047u
CHG_ACDRV_GATE
PR6301 4.02K
PR6302 4.02K
PC6303 0.1u
PC6305 0.1u
PC6304 0.01u
CHG_ACDRV_A
CHG_CMSRC_A
CHG_ACP_A
CHG_ACN_A
PQ6303 PHM13030DL
+AC_BAT_SYS
Iin=8A
Trace Width>320mil
EC_BATA_DET_N [36,70]
+6VA_12VA
CHG_BATDRV_A
PR6305 4.02K
CHG_BATDRV_R_A
PC6306 0.01u
PR6334 0
CHG_BATPRES#
CHG_VCC_D
PR6307 10
PC6313 1u
CHG_BATSRC_S
PR6332 10
+AC_BAT
PC6321 10u DNP
PC6322 10u
+3P3V_EC
PR6312 499K
PR6315 4.7K
PR6316 4.7K
PR6308 200K
PR6313 150K
PR6309 0
PR6310 0
PR6311 0
[70] CHG_ACDET
CHG_ACOK_A
CHG_SDA_A
CHG_SCL_A
CHG_ILIM_A
CHG_IADP_A
CHG_IDCHG_A
[33,36,70] SML1_EC_CLK
[33,36,70] SML1_EC_DATA
[36] EC_CHG_ACOK
[36] EC_CHG_IOUT
[36] EC_ADP_IOUT
[66] PMON
PR6314 0
PR6333 0
PR6336 22K
PMON_R
[10,29,66] H_PROCHOT#
PR6329 51
PR6331 10K
CHG_TB_STAT#
PR6335 0
T6301
R6334 14K
PC6327 100p
PC6319 100p
PC6328 100p
ACN ACP CMSRC ACDRV ACOK ACDET SDA SCL ILIM IADP IDCHG PMON PROCHOT# TB_STAT# CMPIN CMPOUT
BATPRES# VCC REGN BATDRV BATSRC BTST HIDRV PHASE LODRV SRP SRN GND POWERPAD
PU6301 BQ24780SRUYR
CHG_REGN_D
PC6312 2.2u
CHG_BTST_D
PR6306 2.2
CHG_PHASE_S_C
PC6311 0.047u
CHG_HIDRV_D
PR6320 0
CHG_HIDRV_R_D
PC6325 100p DNP
PR6322 5.2K
CHG_PHASE_S
CHG_LODRV_D
PR6321 0
CHG_LODRV_R_D
PC6326 1000p DNP
PQ6304
TG VIN TGR VSW1 VSW2 VSW3 BG GPAD
CSD86330Q3D
PL6301 2.2uH
CHG_PHASE_L_S
PR6304 0.015
VDD_BATA_PACK_FET
PC6310 470p
CHG_PHASE_GND
PR6325 1
PJP6303 SHORT PIN
PJP6304 SHORT PIN
PC6317 10u
PC6316 10u
PC6329 10u
PC6307 0.1u
PC6309 0.1u
PC6308 0.1u
CHG_SRP_A
PR6326 0
CHG_SRP_A_R
CHG_SRN_A
PR6327 0
CHG_SRN_A_R
7-bit I2C Address = 0x12
Title: CHARGER
<OrgName>
Engineer:
<OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
Date: Thursday, June 25, 2015
Sheet 63 of 76





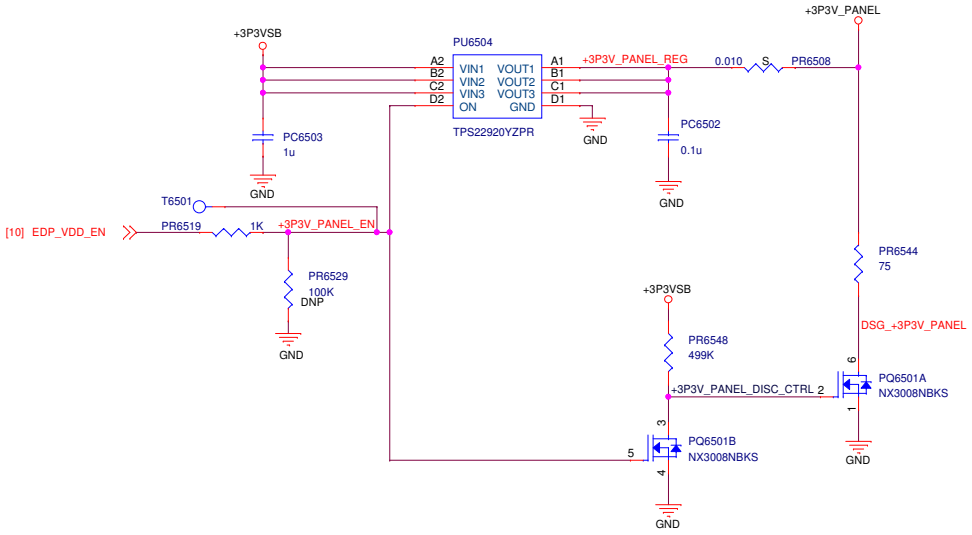




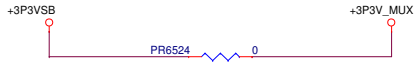


Title:	+5V Load SW		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 64 of 76		

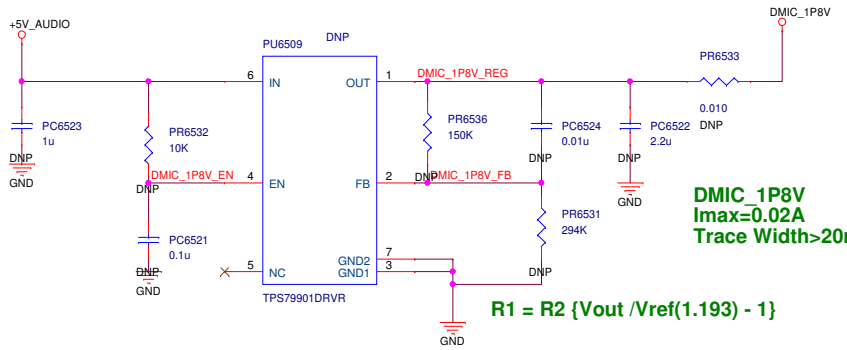
+3P3V_PANEL
Imax=0.273A
Trace Width>50mil



+3P3V_MUX
Imax=0.0033A



+3P3V_PM
Imax=???

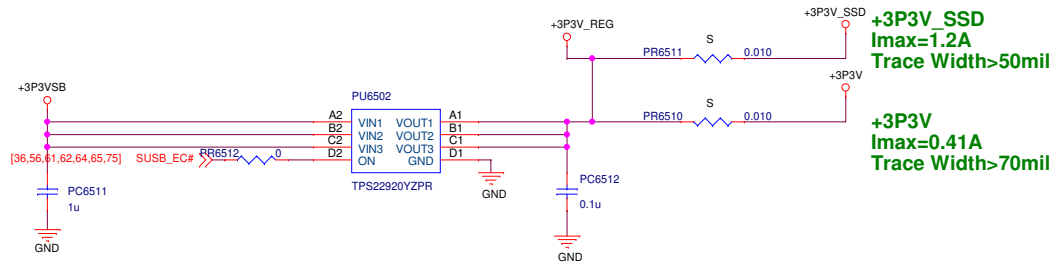


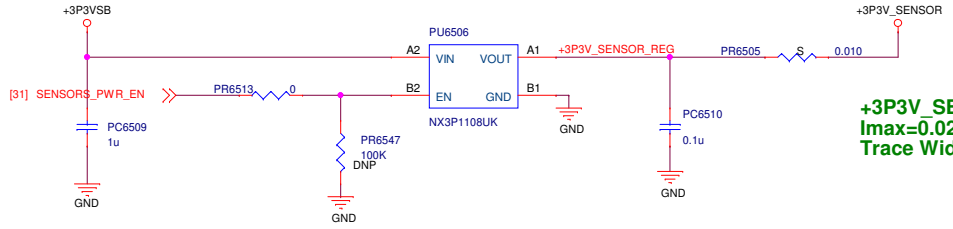
DMIC_1P8V
Imax=0.02A
Trace Width>20mil

R1 = R2 {Vout /Vref(1.193) - 1}

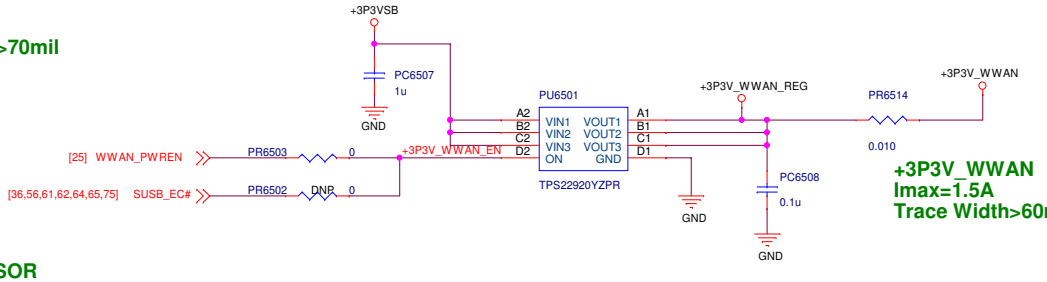
+3P3V_SSD
Imax=1.2A
Trace Width>50mil

+3P3V
Imax=0.41A
Trace Width>70mil



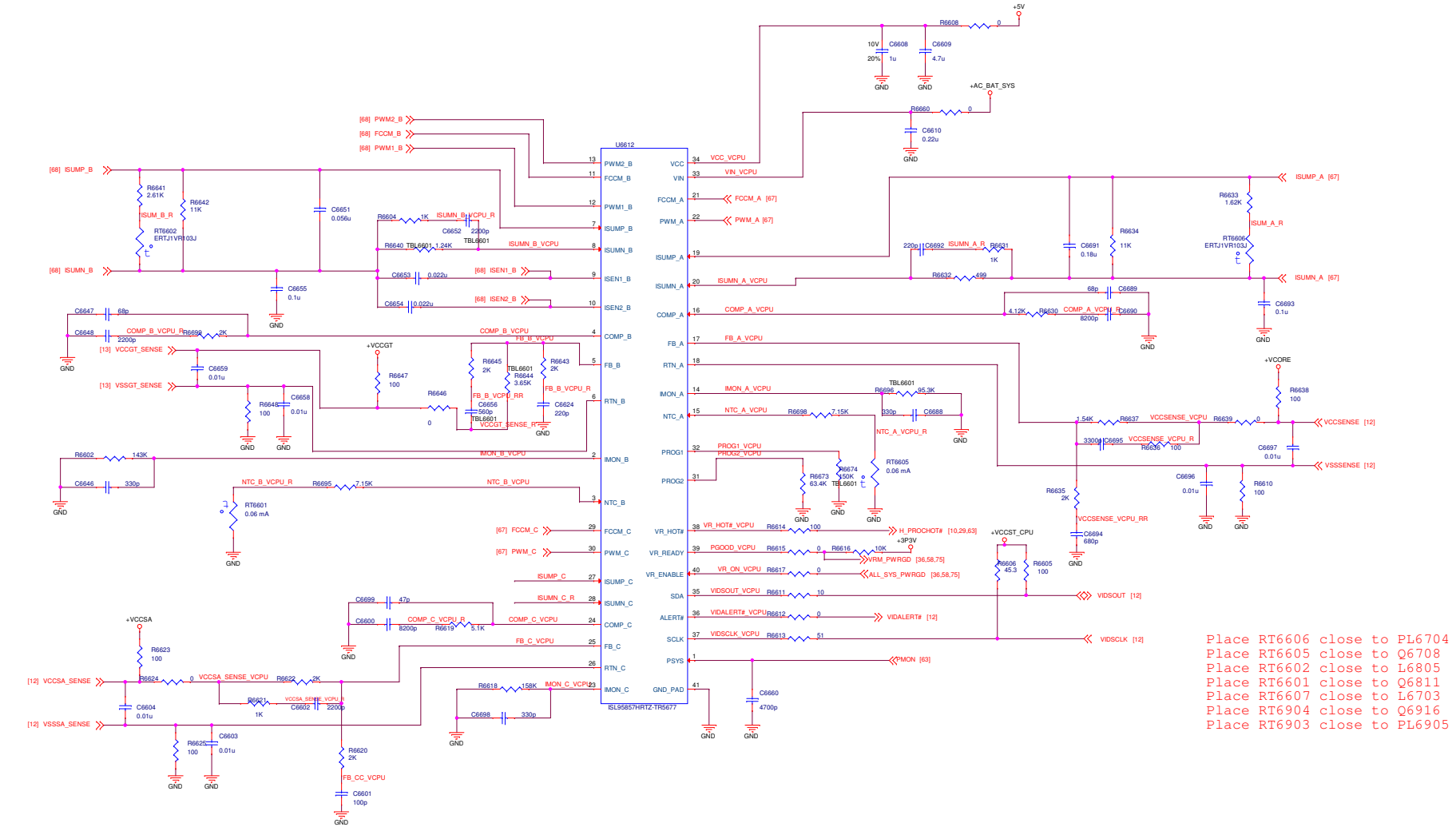


+3P3V_SENSOR
Imax=0.021175A
Trace Width>20mil



+3P3V_WWAN
Imax=1.5A
Trace Width>60mil

Title:	+3P3V Load SW	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 65 of 76	



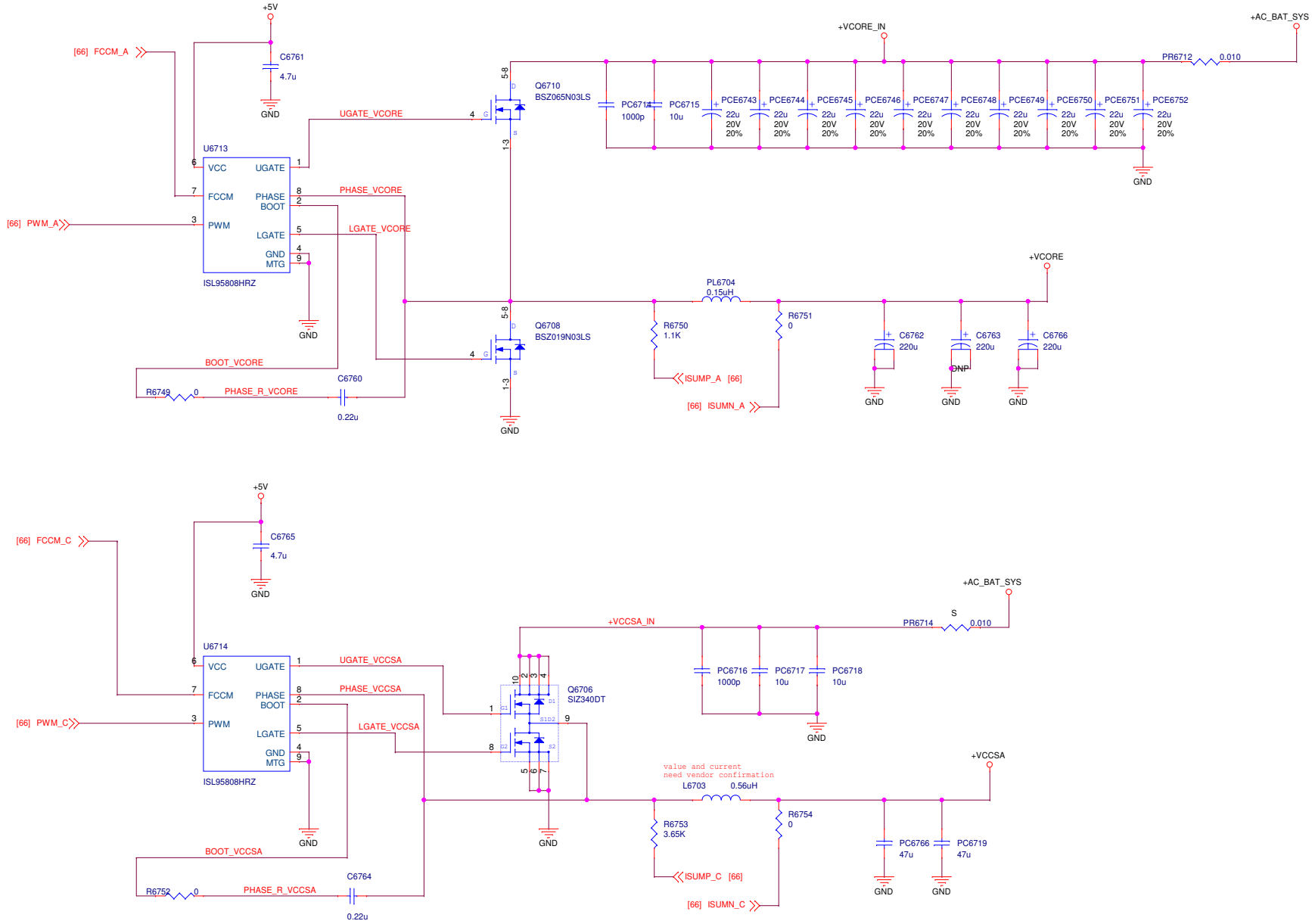
Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6601 close to Q6811
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

Intel spec	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	64A/36A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
DC_LL/AC_LL of Vcore	2.4/2.4	2.4/2.4
DC_LL/AC_LL of VCCGT	3.1/3.1	2.0/2.0
DC_LL/AC_LL of VCCSA	10.3/10.3	10.3/10.3
Change items		
Vcore	R6696 95.3K	R6696 93.1K
VCCGT	R6640 1.24K R6674 150K R6644 3.65K C6656 560P C6652 2200P	R6640 1.69K R6674 165K R6644 3.32K C6656 1200P C6652 3300P
VCCSA	R6618 158K	R6618 133K

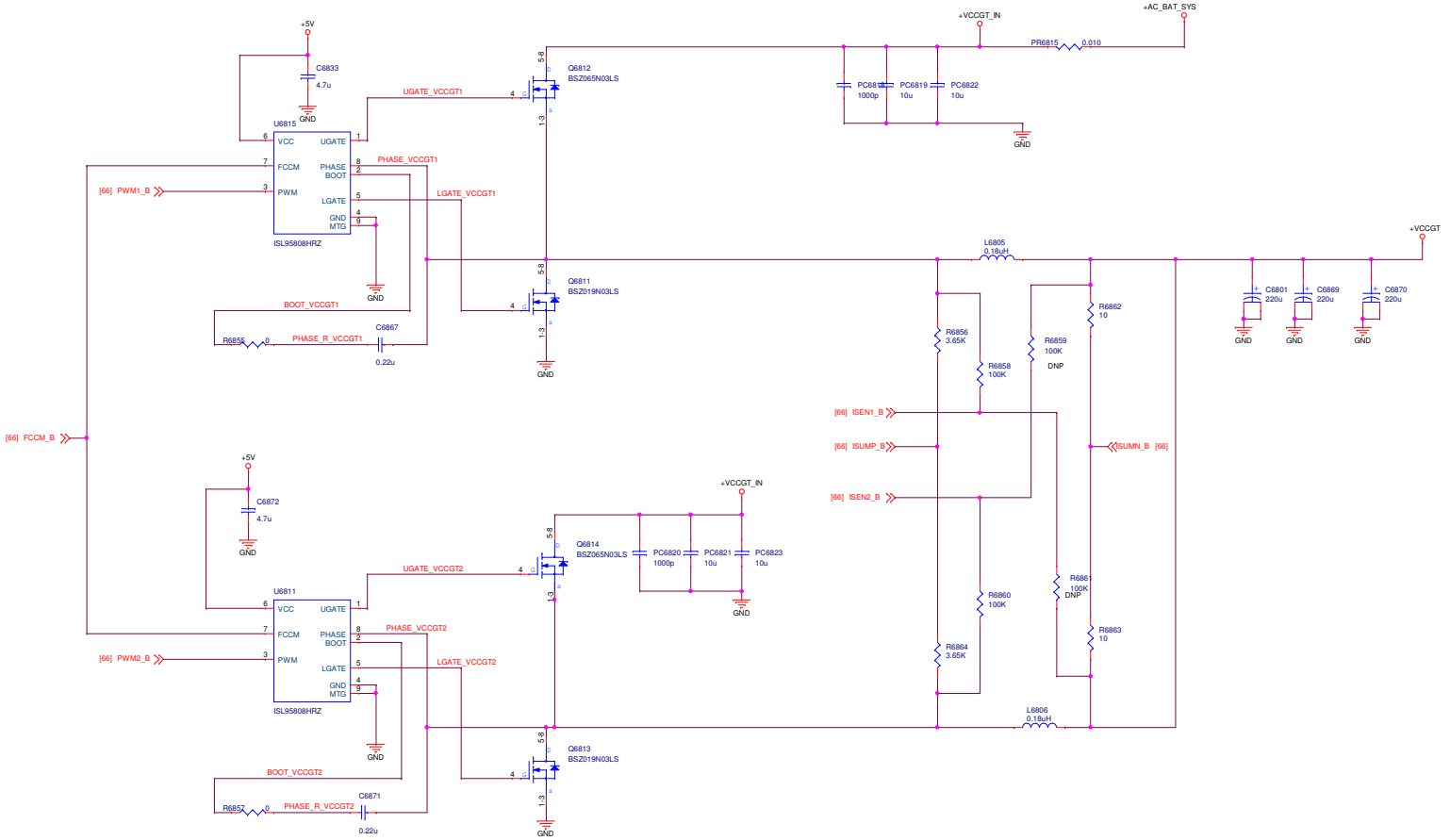
TBL6601

	GT2		GT3	
	Value	MSPN	Value	MSPN
R6640	1.24K	X895647-001	1.69K	X905787-001
R6674	150K	X857755-001	165K	X881346-001
R6644	3.65K	X909697-001	3.32K	X860524-001
C6656	560P	X930204-001	1200P	X930620-001
C6652	2200P	X885510-001	3300P	X892890-001
R6696	95.3K	X877081-001	93.1K	X930616-001
R6618	158K	X910075-001	133K	X881336-001

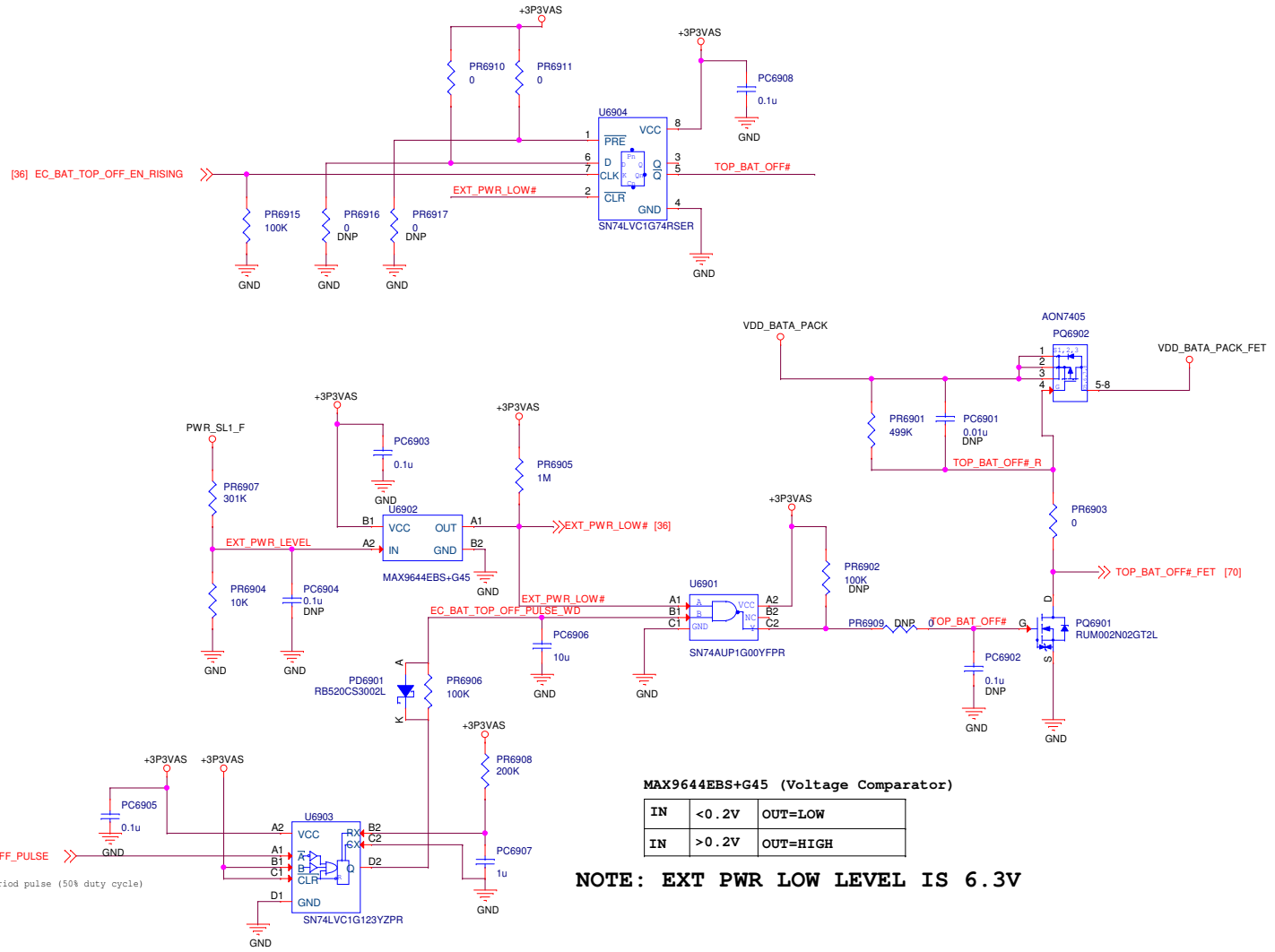
Title: VCPU contoller
<OrgName> Engineer: <OrgAddr1>
Size: A2 Project Name: CHARIOT Rev: 1.00
Date: Thursday, June 25, 2015 Sheet 68 of 76



Title: VCORE VCCSA		
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 67 of 76	



Title:	VCVGT	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 68 of 76	



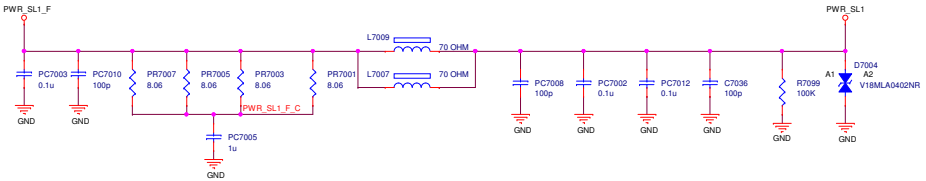
MAX9644EBS+G45 (Voltage Comparator)

IN	<0.2V	OUT=LOW
IN	>0.2V	OUT=HIGH

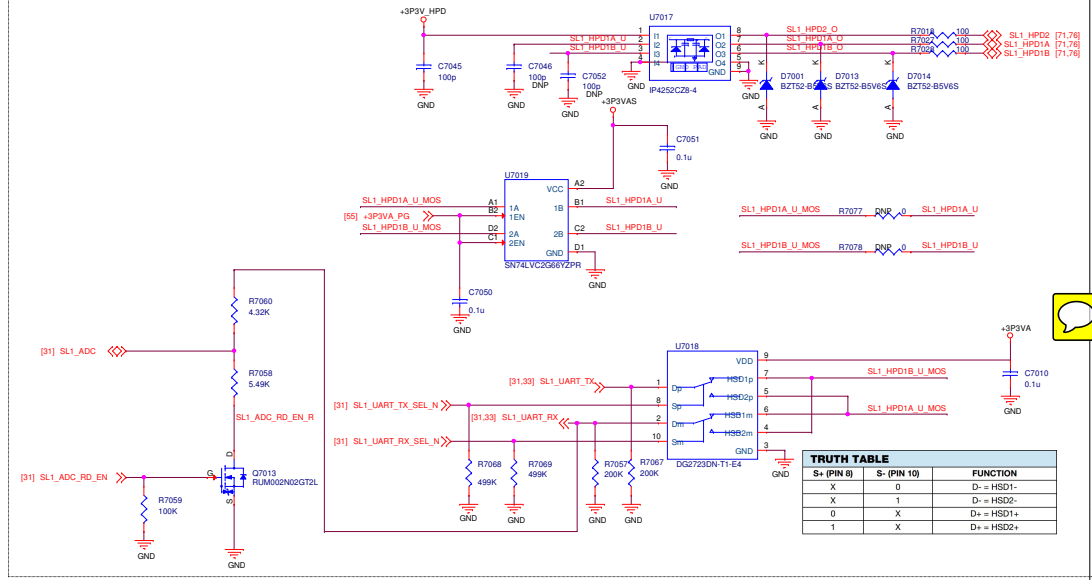
NOTE: EXT PWR LOW LEVEL IS 6.3V

>6.3V	Pulse	Out
1	1	0
1	0	1
0	1	1
0	0	1

Title:	TOP BAT SAVER	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 69 of 76	

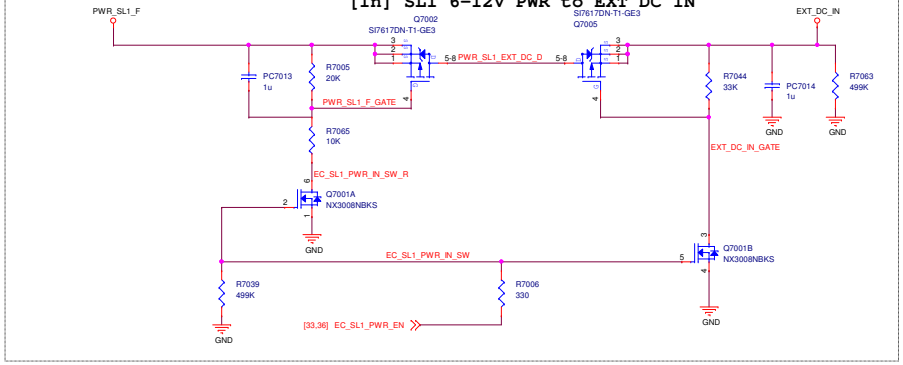


HPD FOR SL1 (ONE/TWO WIRE UART)

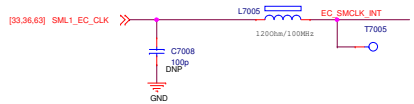


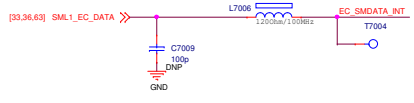
TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

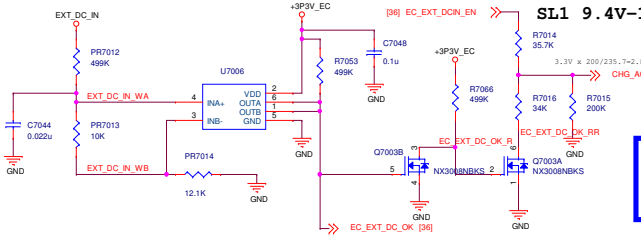
[In] SL1 6-12V PWR to EXT DC IN



Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed



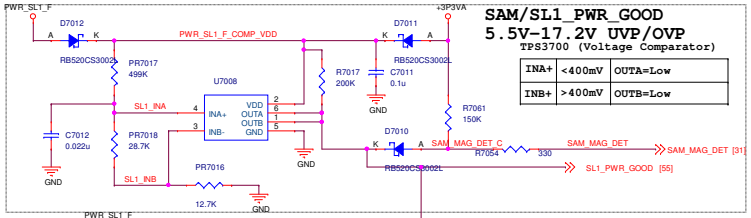




TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

CHG_ACDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES



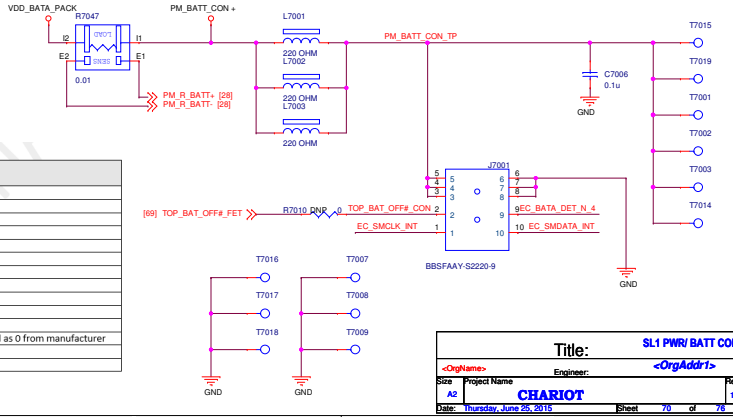
SAM/SL1_PWR_GOOD
5.5V-17.2V UVP/OVP

TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

[Out] SYS +5V PWR to SL1

18W Battery Connector



SL1 port discharger limit PSU anti-arc pulse voltage

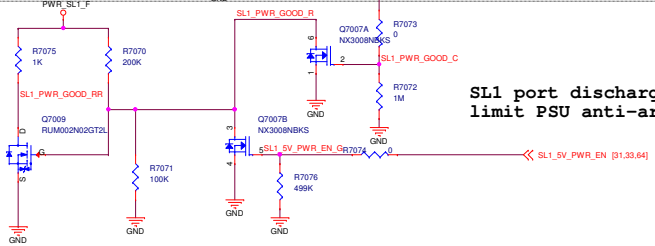


Table 13 – Standard SBS Commands

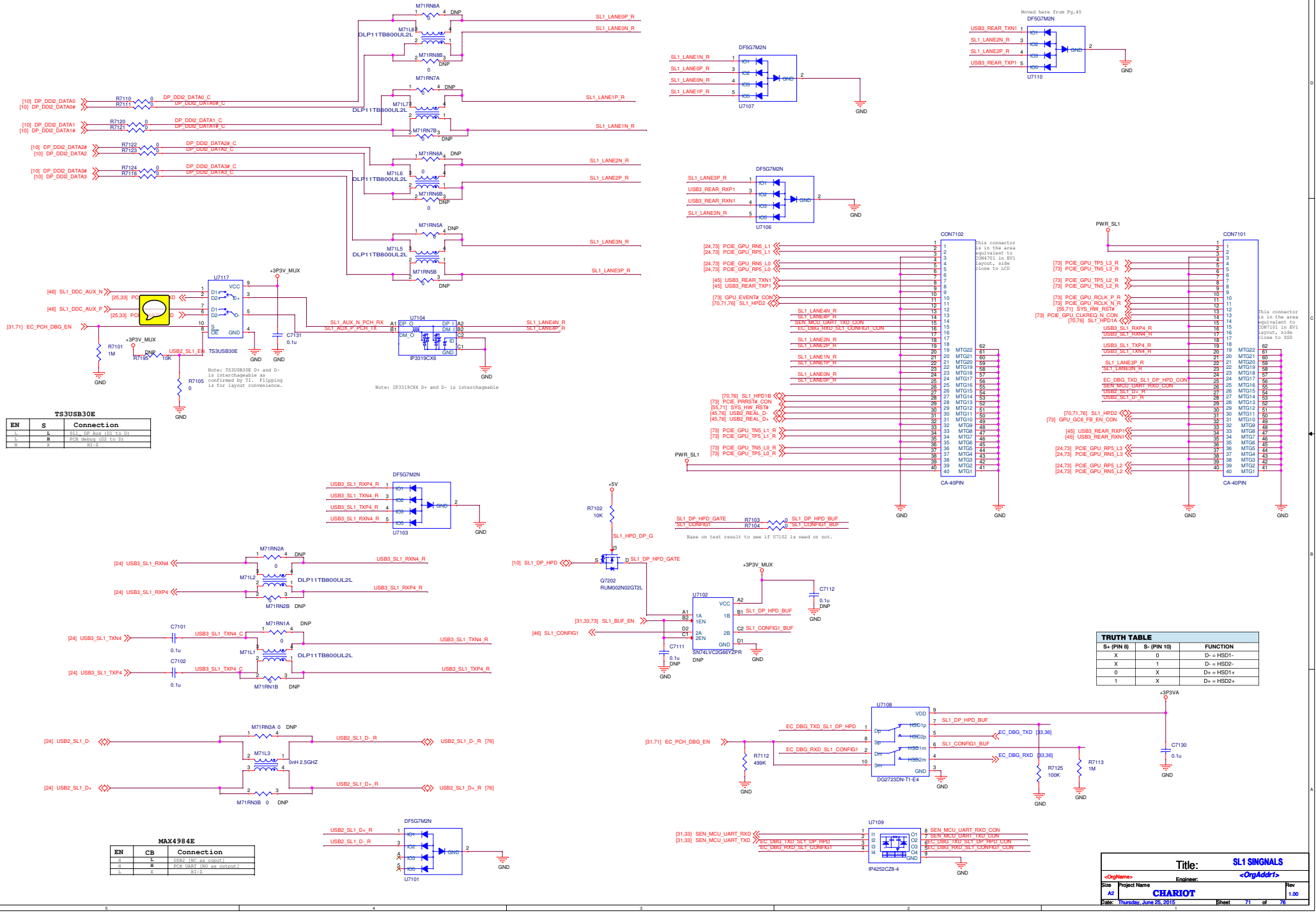
Name	SBS Command	Format	Value	Unit	Notes
Temperature	0x08	UINT16	variable	0.1K	---
Voltage	0x09	UINT16	variable	mV	---
Current	0x0a	INT16	variable	mA	---
Average Current	0x0b	INT16	variable	mA	---
Max Error	0x0c	UINT8	variable	%	---
Relative SOC	0x0d	UINT8	variable	%	---
Remaining Capacity	0x0f	UINT16	variable	mAh	---
Full Capacity	0x10	UINT16	fixed	mAh	---
Charging Current	0x14	UINT16	fixed	mA	---
Charging Voltage	0x15	UINT16	fixed	mV	---
Battery Status	0x16	UINT16	variable	--	---
Cycle Count	0x17	UINT16	variable	Count	Shipped as 0 from manufacturer
Design Capacity	0x18	UINT16	fixed	mAh	---
Design Voltage	0x19	UINT16	fixed	mV	---

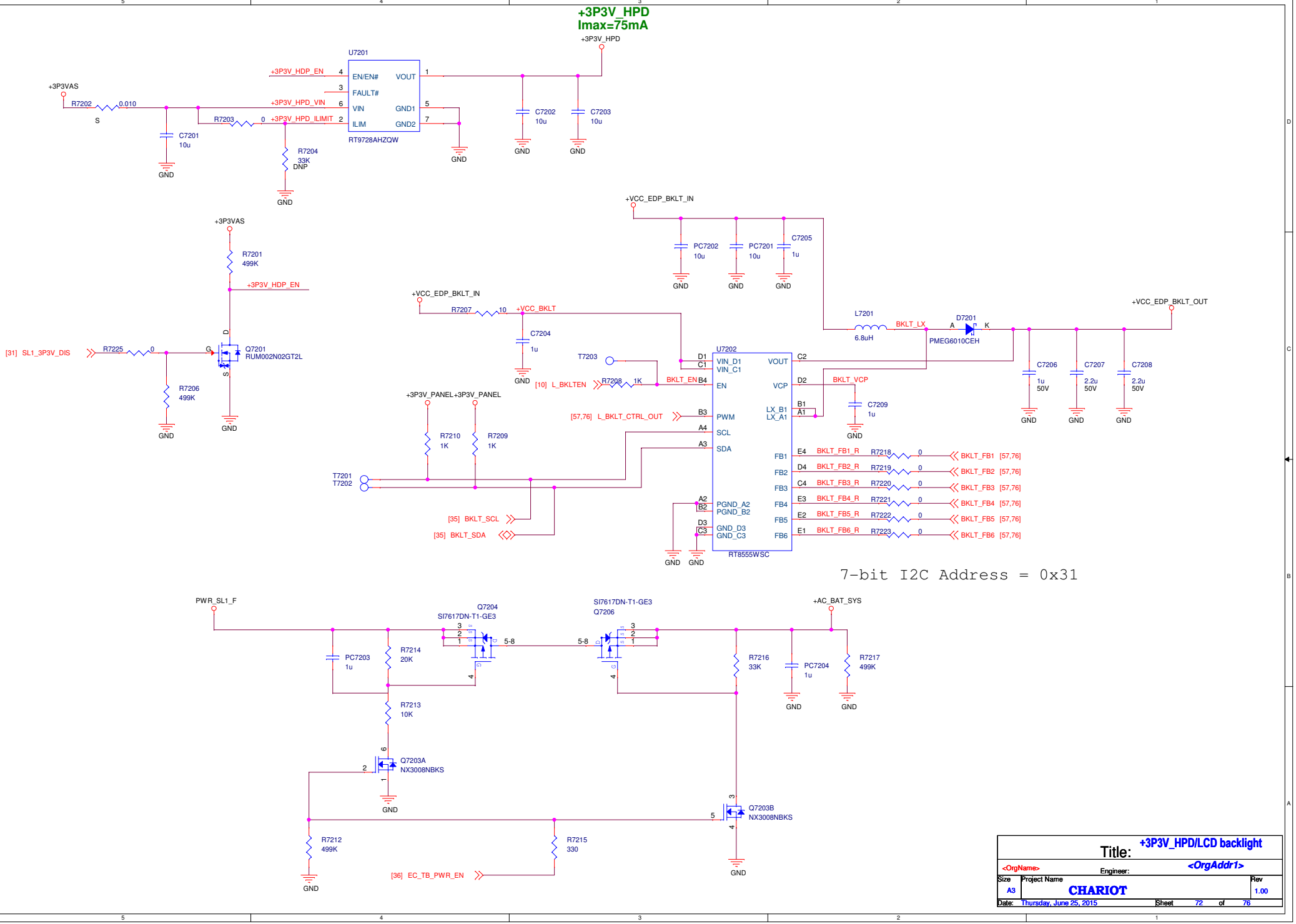
Title: SL1 PWR/ BATT CONN

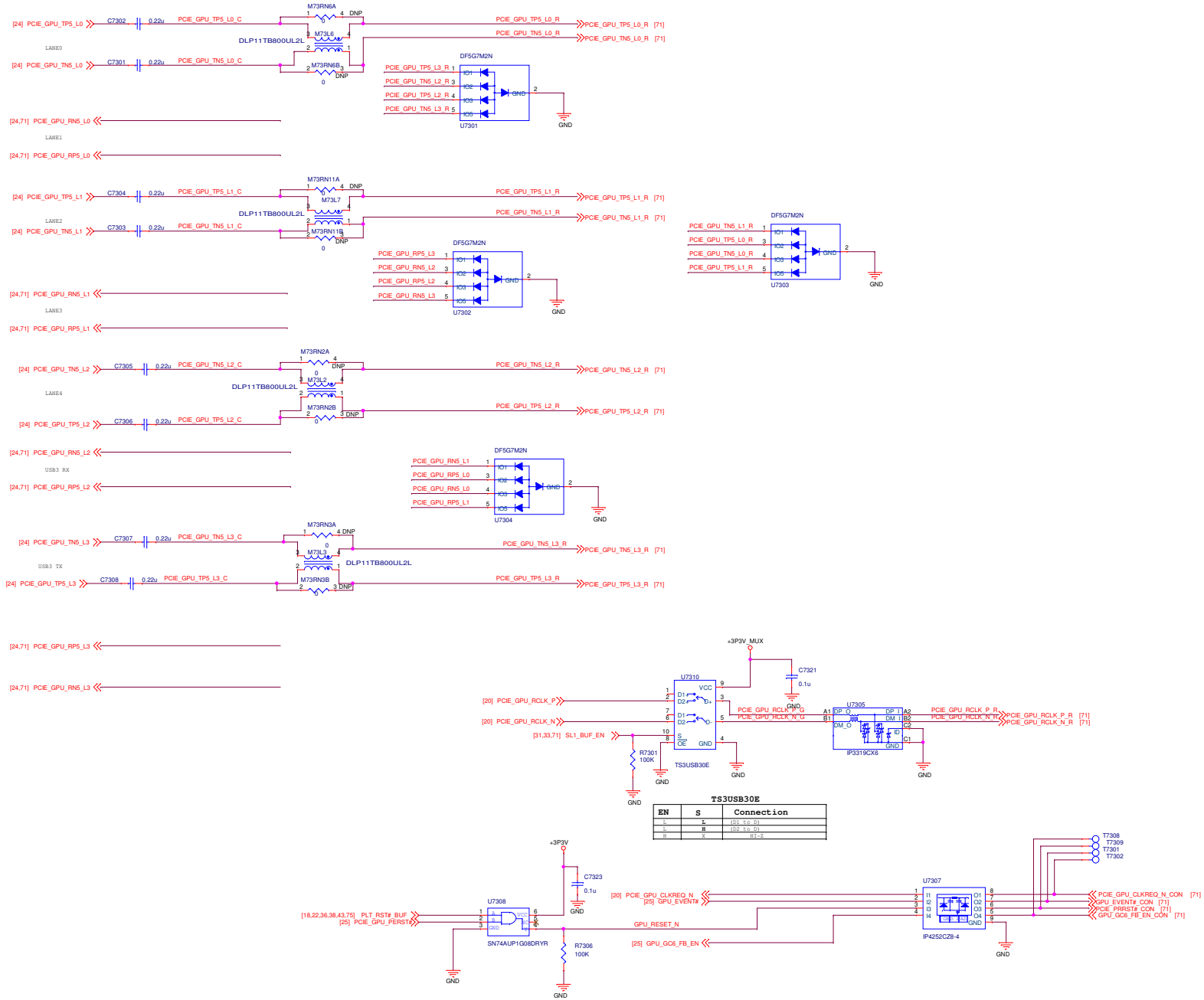
<OrgName> Engineer: <OrgAddr1>

Size: A2 | Project Name: CHARIOT | Rev: 1.00

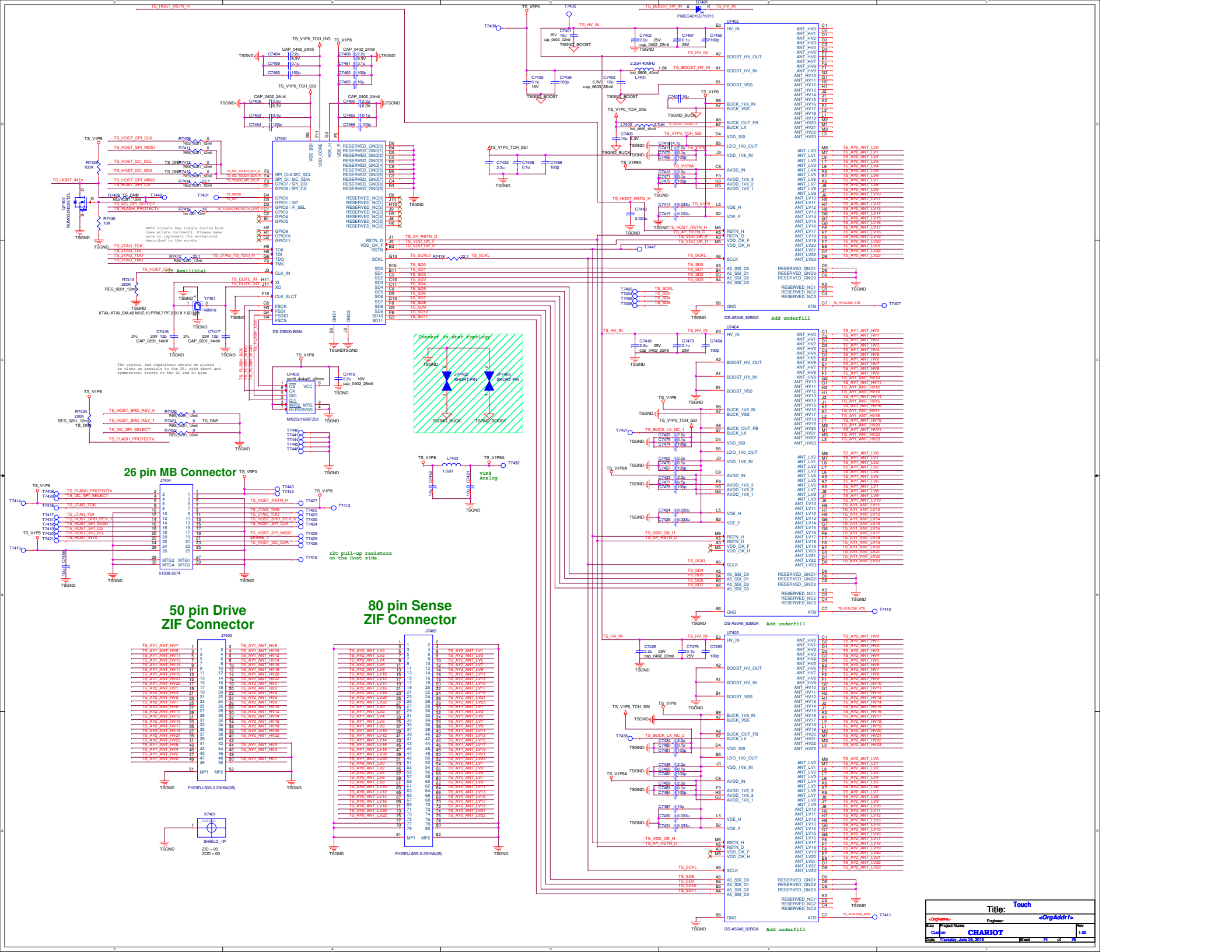
Date: Thursday, June 25, 2015 | Sheet 70 of 78

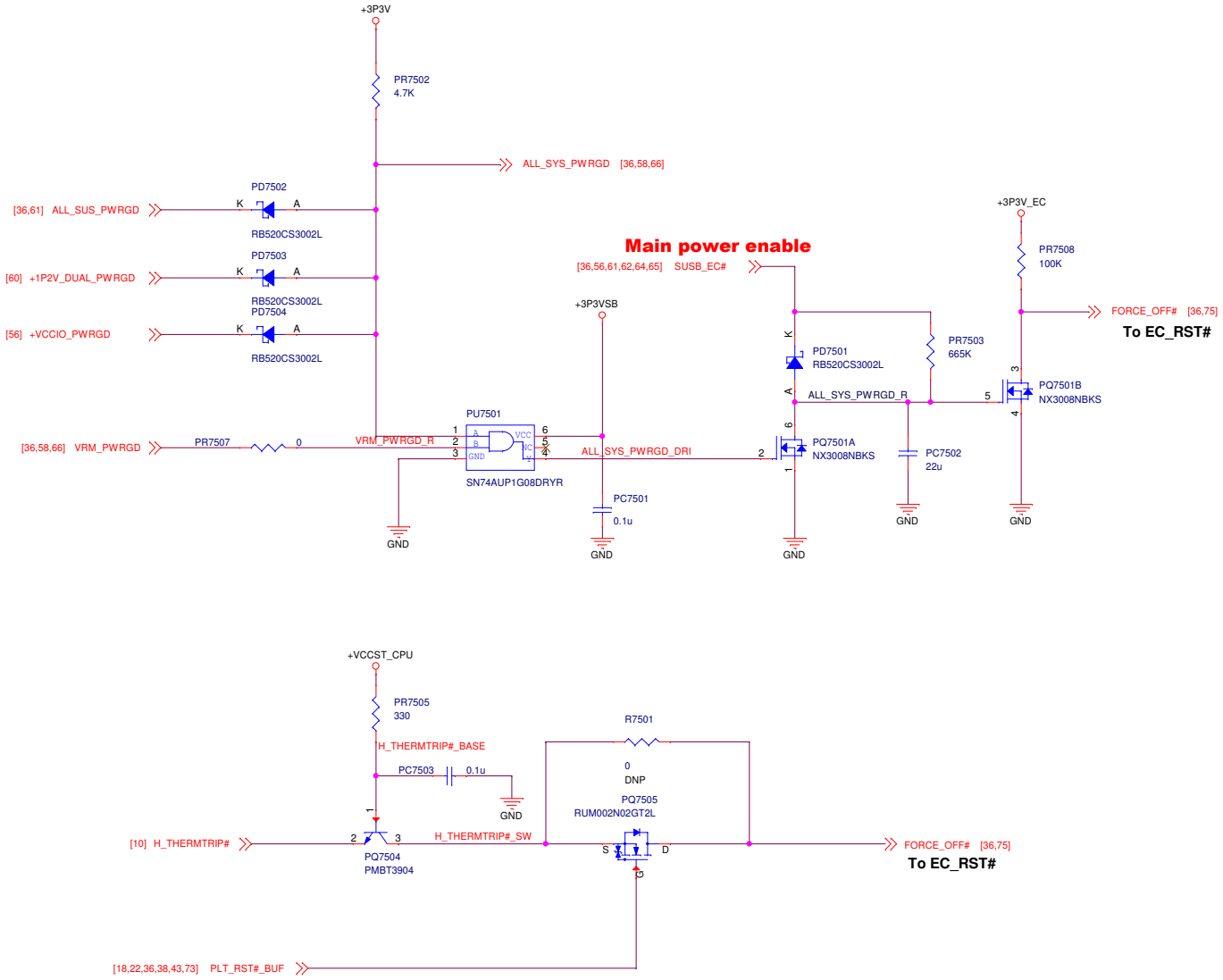

M71RN8A DNP
M71L8 DLP11TB800UL2L
M71RN8B DNP
SL1_LANE0P_R
SL1_LANE0N_R
M71RN7A DNP
M71L7 DLP11TB800UL2L
M71RN7B DNP
SL1_LANE1P_R
SL1_LANE1N_R
M71RN6A DNP
M71L6 DLP11TB800UL2L
M71RN6B DNP
SL1_LANE2N_R
SL1_LANE2P_R
M71RN5A DNP
M71L5 DLP11TB800UL2L
M71RN5B DNP
SL1_LANE3N_R
SL1_LANE3P_R
[10] DP_DDI2_DATA0
[10] DP_DDI2_DATA0#
R7110 0
R7111 0
DP_DDI2_DATA0_C
DP_DDI2_DATA0#_C
[10] DP_DDI2_DATA1
[10] DP_DDI2_DATA1#
R7120 0
R7121 0
DP_DDI2_DATA1_C
DP_DDI2_DATA1#_C
[10] DP_DDI2_DATA2
[10] DP_DDI2_DATA2#
R7122 0
R7123 0
DP_DDI2_DATA2_C
DP_DDI2_DATA2#_C
[10] DP_DDI2_DATA3
[10] DP_DDI2_DATA3#
R7124 0
R7116 0
DP_DDI2_DATA3_C
DP_DDI2_DATA3#_C
U7117
+3P3V_MUX
[46] SL1_DDC_AUX_N
[46] SL1_DDC_AUX_P
[25,33] PCH_DDI2_AUX_N
[25,33] PCH_DDI2_AUX_P
[31,71] EC_PCH_DBG_EN
R7101 1M
R7105 0
R7195 DNP
10K
USB2_SL1_EN
TS3USB30E
C7131 0.1u
SL1_AUX_N_PCH_RX
SL1_AUX_P_PCH_TX
U7104
IP3319CX6
SL1_LANE4N_R
SL1_LANE4P_R
Note: TS3USB30E D+ and D- is interchageable as confirmed by TI. Flipping is for layout convenience.
Note: IP3319CX6 D+ and D- is interchageable
TS3USB30E
EN | S | Connection
L | L | SL1_ DP Aux (D1 to D)
L | H | PCH debug (D2 to D)
H | X | Hi-Z
Moved here from Pg.45
DF5G7M2N
USB3_REAR_TXN1
SL1_LANE2N_R
SL1_LANE2P_R
USB3_REAR_TXP1
U7110
DF5G7M2N
SL1_LANE1N_R
SL1_LANE0P_R
SL1_LANE0N_R
SL1_LANE1P_R
U7107
DF5G7M2N
SL1_LANE3P_R
USB3_REAR_RXP1
USB3_REAR_RXN1
SL1_LANE3N_R
U7106
CON7102
This connector is in the area equivalent to CON4701 in EV1 layout, side close to LCD
[24,73] PCIE_GPU_RN5_L1
[24,73] PCIE_GPU_RP5_L1
[24,73] PCIE_GPU_RN5_L0
[24,73] PCIE_GPU_RP5_L0
[45] USB3_REAR_TXN1
[45] USB3_REAR_TXP1
[73] GPU_EVENT#_CON
[70,71,76] SL1_HPD2
SL1_LANE4N_R
SL1_LANE4P_R
SEN_MCU_UART1_TXD_CON
EC_DBG_RXD_SL1_CONFIG1_CON
SL1_LANE2N_R
SL1_LANE2P_R
SL1_LANE1N_R
SL1_LANE1P_R
SL1_LANE0N_R
SL1_LANE0P_R
[70,76] SL1_HPD1B
[73] PCIE_PRRST#_CON
[55,71] SYS_HW_RST#
[45,76] USB2_REAL_D-
[45,76] USB2_REAL_D+
[73] PCIE_GPU_TN5_L1_R
[73] PCIE_GPU_TP5_L1_R
[73] PCIE_GPU_TN5_L0_R
[73] PCIE_GPU_TP5_L0_R
PWR_SL1
CA-40PIN
PWR_SL1
CON7101
This connector is in the area equivalent to CON7101 in EV1 layout, side close to SSD
[73] PCIE_GPU_TP5_L3_R
[73] PCIE_GPU_TN5_L3_R
[73] PCIE_GPU_TP5_L2_R
[73] PCIE_GPU_TN5_L2_R
[73] PCIE_GPU_RCLK_P_R
[73] PCIE_GPU_RCLK_N_R
[55,71] SYS_HW_RST#
[73] PCIE_GPU_CLKREQ_N_CON
[70,76] SL1_HPD1A
USB3_SL1_RXP4_R
USB3_SL1_RXN4_R
USB3_SL1_TXP4_R
USB3_SL1_TXN4_R
SL1_LANE3P_R
SL1_LANE3N_R
EC_DBG_TXD_SL1_DP_HPD_CON
SEN_MCU_UART1_RXD_CON
USB2_SL1_D+_R
USB2_SL1_D-_R
[70,71,76] SL1_HPD2
[73] GPU_GC6_FB_EN_CON
[45] USB3_REAR_RXP1
[45] USB3_REAR_RXN1
[24,73] PCIE_GPU_RP5_L3
[24,73] PCIE_GPU_RN5_L3
[24,73] PCIE_GPU_RP5_L2
[24,73] PCIE_GPU_RN5_L2
DF5G7M2N
USB3_SL1_RXP4_R
USB3_SL1_TXN4_R
USB3_SL1_TXP4_R
USB3_SL1_RXN4_R
U7103
+5V
R7102 10K
SL1_HPD_DP_G
[10] SL1_DP_HPD
Q7202 RUM002N02GT2L
SL1_DP_HPD_GATE
SL1_DP_HPD_BUF
SL1_CONFIG1
R7103 0
R7104 0
SL1_CONFIG1_BUF
Base on test result to see if U7102 is need or not.
U7102
SN74LVC2G66YZPR
[31,33,73] SL1_BUF_EN
[46] SL1_CONFIG1
C7112 0.1u DNP
C7111 0.1u DNP
M71RN2A DNP
M71L2 DLP11TB800UL2L
M71RN2B DNP
[24] USB3_SL1_RXN4
[24] USB3_SL1_RXP4
USB3_SL1_RXN4_R
USB3_SL1_RXP4_R
C7101 0.1u
C7102 0.1u
M71RN1A DNP
M71L1 DLP11TB800UL2L
M71RN1B DNP
[24] USB3_SL1_TXN4
[24] USB3_SL1_TXP4
USB3_SL1_TXN4_C
USB3_SL1_TXP4_C
USB3_SL1_TXN4_R
USB3_SL1_TXP4_R
M71RN3A 0 DNP
M71L3 0nH 2.5GHZ
M71RN3B 0 DNP
[24] USB2_SL1_D-
[24] USB2_SL1_D+
USB2_SL1_D-_R
USB2_SL1_D+_R
[76]
MAX4984E
EN | CB | Connection
H | L | USB2 [NC as output]
H | H | PCH UART [NO as output]
L | X | Hi-Z
DF5G7M2N
USB2_SL1_D+_R
USB2_SL1_D-_R
U7101
U7108
DG2723DN-T1-E4
EC_DBG_TXD_SL1_DP_HPD
EC_DBG_RXD_SL1_CONFIG1
SL1_DP_HPD_BUF
SL1_CONFIG1_BUF
EC_DBG_TXD [33,36]
EC_DBG_RXD [33,36]
[31,71] EC_PCH_DBG_EN
R7112 499K
R7125 100K
R7113 1M
C7130 0.1u
+3P3VA
U7109
IP4252CZ8-4
[31,33] SEN_MCU_UART_RXD
[31,33] SEN_MCU_UART_TXD
EC_DBG_TXD_SL1_DP_HPD
EC_DBG_RXD_SL1_CONFIG1
SEN_MCU_UART_RXD_CON
SEN_MCU_UART_TXD_CON
EC_DBG_TXD_SL1_DP_HPD_CON
EC_DBG_RXD_SL1_CONFIG1_CON
TRUTH TABLE
S+ (PIN 8) | S- (PIN 10) | FUNCTION
X | 0 | D- = HSD1-
X | 1 | D- = HSD2-
0 | X | D+ = HSD1+
1 | X | D+ = HSD2+
Title: SL1 SINGNALS
<OrgName>
Engineer:
<OrgAddr1>
Size: A2
Project Name: CHARIOT
Rev: 1.00
Date: Thursday, June 25, 2015
Sheet 71 of 76


+3P3V_HPD
Imax=75mA
+3P3V_HPD
U7201
+3P3V_HDP_EN
EN/EN#
VOUT
FAULT#
+3P3V_HPD_VIN
VIN
GND1
+3P3V_HPD_ILIMIT
ILIM
GND2
RT9728AHZQW
+3P3VAS
R7202
0.010
S
R7203
0
C7201
10u
R7204
33K
DNP
C7202
10u
C7203
10u
GND
+VCC_EDP_BKLT_IN
PC7202
10u
PC7201
10u
C7205
1u
+3P3VAS
R7201
499K
+3P3V_HDP_EN
[31] SL1_3P3V_DIS
R7225
0
Q7201
RUM002N02GT2L
R7206
499K
+VCC_EDP_BKLT_IN
R7207
10
+VCC_BKLT
C7204
1u
T7203
[10] L_BKLTEN
R7208
1K
BKLT_EN
U7202
VIN_D1
VIN_C1
EN
PWM
SCL
SDA
PGND_A2
PGND_B2
GND_D3
GND_C3
VOUT
VCP
LX_B1
LX_A1
FB1
FB2
FB3
FB4
FB5
FB6
RT8555WSC
L7201
6.8uH
BKLT_LX
D7201
PMEG6010CEH
+VCC_EDP_BKLT_OUT
C7206
1u
50V
C7207
2.2u
50V
C7208
2.2u
50V
BKLT_VCP
C7209
1u
[57,76] L_BKLT_CTRL_OUT
+3P3V_PANEL
+3P3V_PANEL
R7210
1K
R7209
1K
T7201
T7202
[35] BKLT_SCL
[35] BKLT_SDA
BKLT_FB1_R
R7218
BKLT_FB1 [57,76]
BKLT_FB2_R
R7219
BKLT_FB2 [57,76]
BKLT_FB3_R
R7220
BKLT_FB3 [57,76]
BKLT_FB4_R
R7221
BKLT_FB4 [57,76]
BKLT_FB5_R
R7222
BKLT_FB5 [57,76]
BKLT_FB6_R
R7223
BKLT_FB6 [57,76]
7-bit I2C Address = 0x31
PWR_SL1_F
Q7204
SI7617DN-T1-GE3
5-8
SI7617DN-T1-GE3
Q7206
+AC_BAT_SYS
PC7203
1u
R7214
20K
R7213
10K
Q7203A
NX3008NBKS
R7216
33K
PC7204
1u
R7217
499K
Q7203B
NX3008NBKS
R7212
499K
R7215
330
[36] EC_TB_PWR_EN
Title: +3P3V_HPD/LCD backlight
<OrgName>
Engineer:
<OrgAddr1>
Size
A3
Project Name
CHARIOT
Rev
1.00
Date: Thursday, June 25, 2015
Sheet 72 of 76



Title:	PCIe GPU		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 73 of 76		


26 pin MB Connector
50 pin Drive ZIF Connector
80 pin Sense ZIF Connector
Connect in star topology
I2C pull-up resistors on the Host side.
Add underfill
Title: Touch
<OrgName>
<OrgAddr1>
Engineer:
Size: Custom
Project Name: CHARIOT
Rev: 1.00
Date: Thursday, June 25, 2015
Sheet 74 of 76



Title:	Power Protect	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 75 of 76	

+VCC_EDP_BKLT_OUT T7601
+3P3VA T7602
+3P3VSB T7603
+5VSB T7604
+5V T7605
+1VSB T7679
+1P8V_AUDIO T7665
+1P8V_TS T7666
+VCCEDRAM T7658
+VCCEOPIO T7660
+1P2V_DUAL T7611
+V_VDDQ_VTT T7612
+VCORE T7613
+VDDQ_VREF T7614
+1P8V T7615
+5V_AUDIO T7616
+1P8V_DUAL T7618
+1V_MODPHY T7619
+1P8VA T7620
+1P8VSB T7607
+VCCIO T7662
+VCCST_CPU T7661
+VCCSTG T7659
+VCC_RTC T7608
+3P3V T7609
+3P3V_SENSOR T7610
+3P3V_WWAN T7681
+3P3V_SSD T7687
+3P3V_PANEL T7685
+VPCHCORE T7686
+3P3V_EC T7629
+3P3VAS T76124
+VCCDSW T7630
+VCCGT T7652
+VCCSA T7657
[45,71] USB2_REAL_D- T7637
[45,71] USB2_REAL_D+ T7638
T7640
GND
[71] USB2_SL1_D+_R T7667
[71] USB2_SL1_D-_R T7668
[42] DMIC1_CLK_R T7641
[42] DMIC1_DATA_R T7699
[42] DMIC_PWR T7643
T7644
GND
[33,35,36,39] SML3_EC_DATA T7617 T7649
[33,35,36,39] SML3_EC_CLK T7669
[36,55] VCCDSW_EN
[31,32,33] I2C_SCL_MCU T7675 T7676
[31,32,33] I2C_SDA_MCU
+3P3V_HPD T7683
PWR_SL1 T7670 T7653 T7654 T7655 T76105 T76103
T7656 T7671 T7672 T7673 T76104 T76102
GND
DMIC_1P8V T7691
+5V_TS T7692
+2P8V_CAM_R T7694
+2P8V_CAM_F T7695
+1P8V_CAM_R T7696
+1P8V_CAM_F T7697
+1P2V_CAM_R T7698
+3P3V_VCM T76123
+2P8V_CAM_IR T7651
+1P8V_CAM_IR T7639
T76101
[70,71] SL1_HPD2
T7682
[70,71] SL1_HPD1B
T7684
[70,71] SL1_HPD1A
T7642 BKLT_FB1 [57,72]
T7650 BKLT_FB2 [57,72]
T7680 BKLT_FB3 [57,72]
T7606 BKLT_FB4 [57,72]
T7677 BKLT_FB5 [57,72]
T7678 BKLT_FB6 [57,72]
T7688 L_BKLT_CTRL_OUT [57,72]
[41] MIC1_CR_F_C T7625
T7626
GND
[41] HPOUT_L_F_C T7627
[41] HPOUT_R_F_C T7628
[40,41] HPOUT_JD T7674
close to CON4101
[39] CFAN_PWM_R_1 T7645
[39] CFAN_D_1 T7646
+5V_FAN T7648
T7647
GND
close to CON3901
[41] SPKR+_CON T7621
[41] SPKR-_CON T7622
[41] SPKL+_CON T7623
[41] SPKL-_CON T7624
close to speaker connector
T7631
AGND
close to audio
[30] VOL_UP_R T7632
[30] VOL_DOWN_R T7633
close to CON4101
T7634
GND
close to CON4901
[18,30,33] PWR_SW# T7635
T7636
GND
close to CON3003

Title:	Test Point		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, June 25, 2015	Sheet 76 of 76		