MS-7B23

ATX:243.8mm*243.8mm

Ver: 20

Intel -CoffeeLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *4Phase*

*GT POWER PAK *2 Phase*

Onboard Chip:

SIO: NCT5567D colay NCT5565D
HD Audio Codec: ALC887
LAN: RTL8111H
Flash ROM: SPI 64 MB

DP to VGA: RTD2167

CUT VBAT:SLG4B41231

Main Memory:

*DDR4 * 4 (Dual Channel)*

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8_VSB:GS7133

3VDSW:GS7116

VCCSTPLL:GS7133

System Chipset:

Cannon Lake B360

PWM:

VCORE - RT3606

DDR - RT8125E

DDR VPP25- MP2147

PCH(1.05V) - RT8125E

VCCSA - RT8125E

VCCIO - SY8288

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

*M.2 Slot * 2*

MSI

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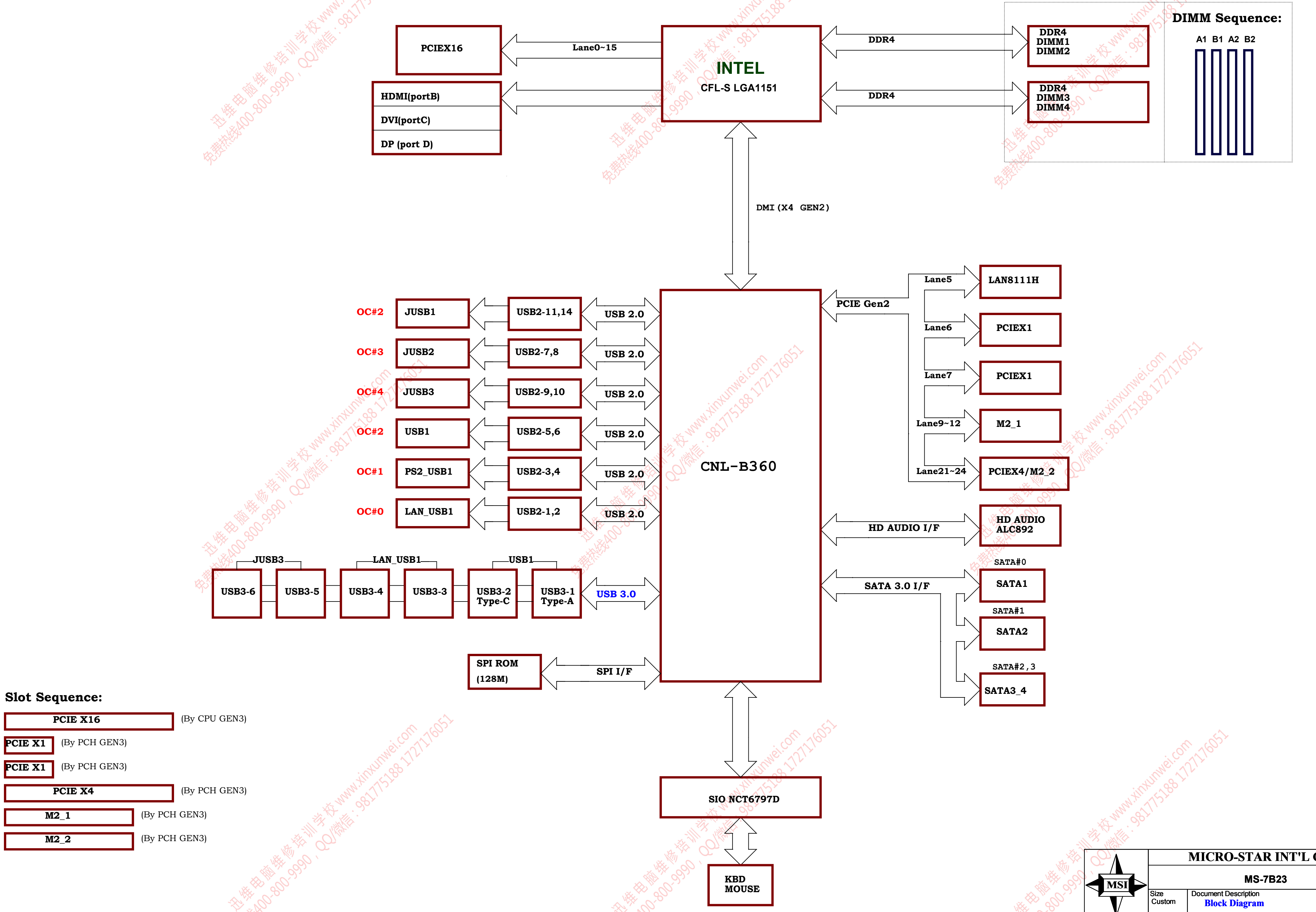
MS-7B23

Size	Document Description	Rev
Custom	Cover Sheet	20

Date: Friday, October 20, 2017 Sheet 1 of 63

MS-7B23 Block Diagram



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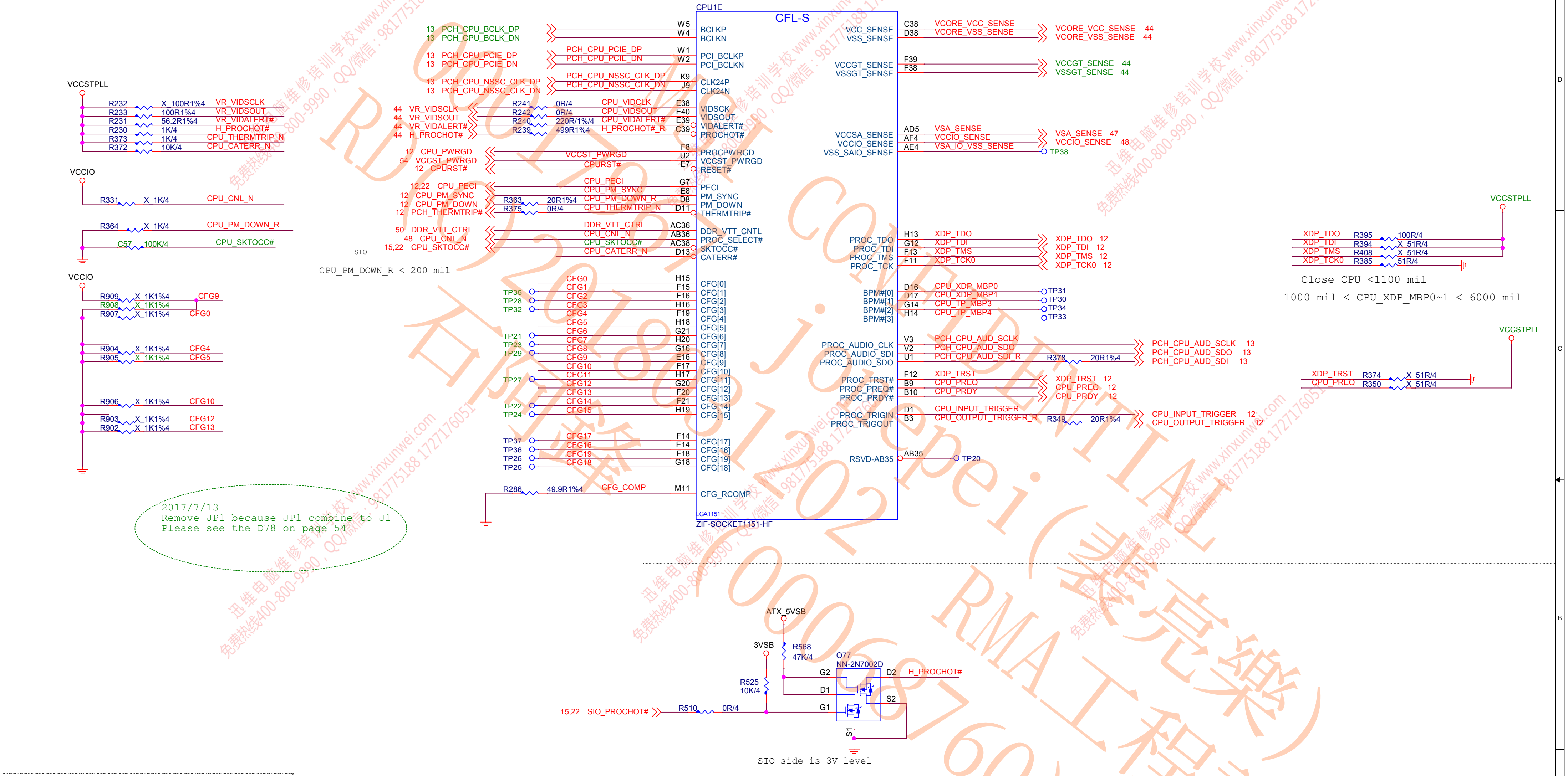
MS-7B23

Size	Document Description	Rev
Custom	Block Diagram	20

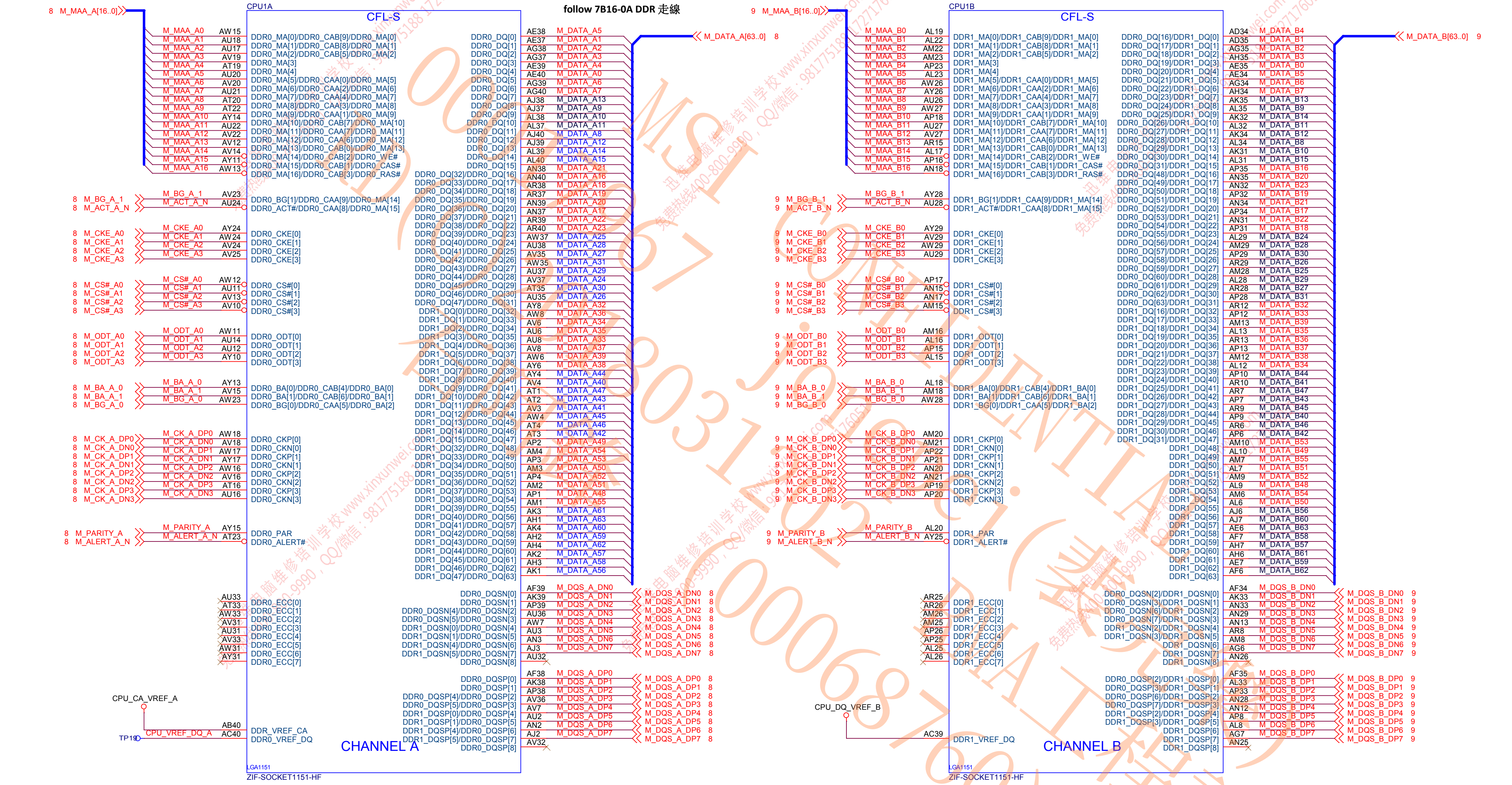
Date: Friday, October 20, 2017 | Sheet 2 of 63



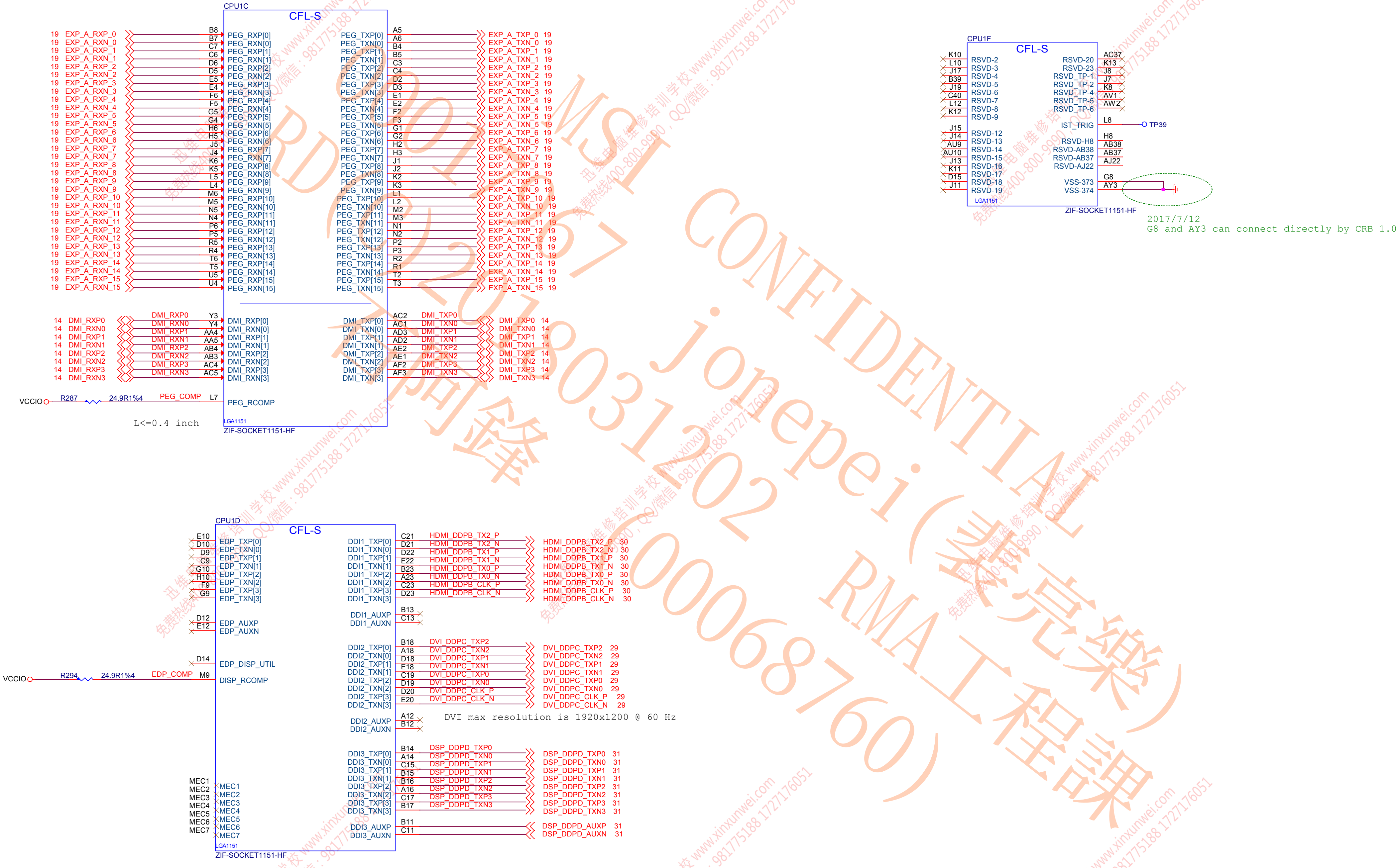
CFG Strap

CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

SOCKET PN N12-151A010-L06



MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size: Custom	Document Description: CPU-Memory	Rev: 20
Date: Friday, October 20, 2017	Sheet 4 of 63	



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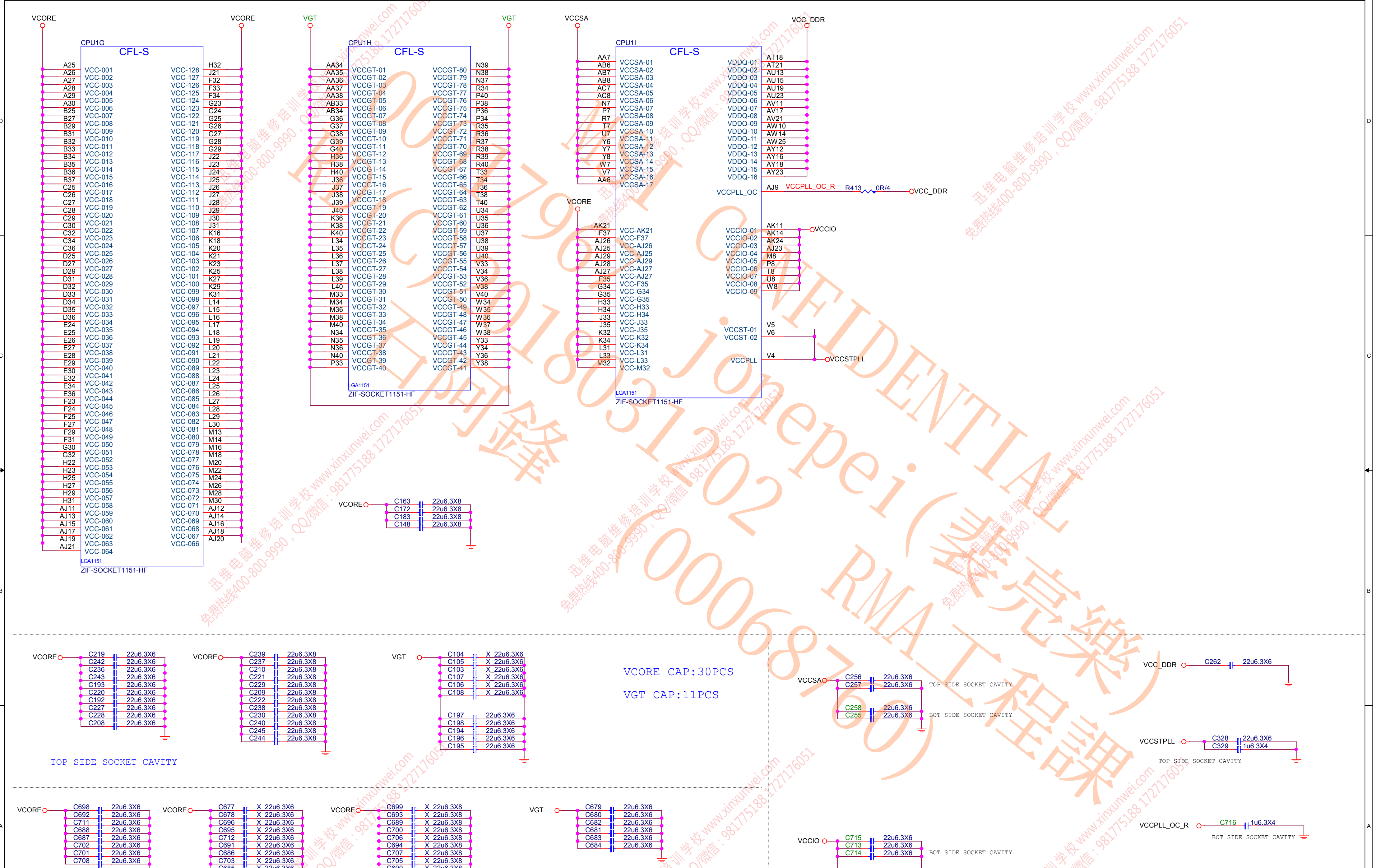
Size	Document Description	Rev
Custom	CPU-PEG/Display	20

Date: Friday, October 20, 2017 | Sheet 5 of 63

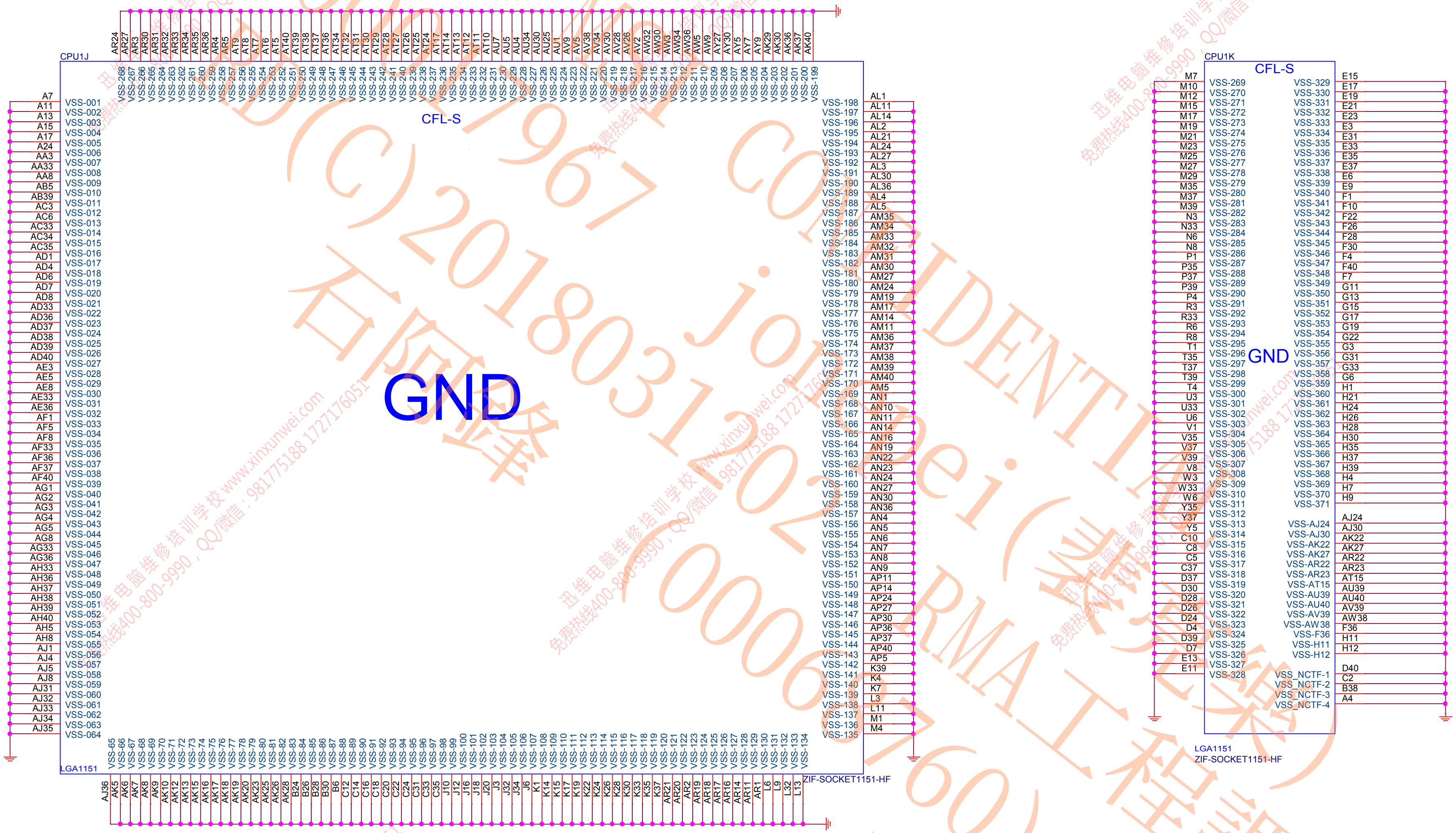


MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	CPU-Power	20

Date: Friday, October 20, 2017 Sheet 6 of 63



MICRO-STAR INT'L CO.,LTD

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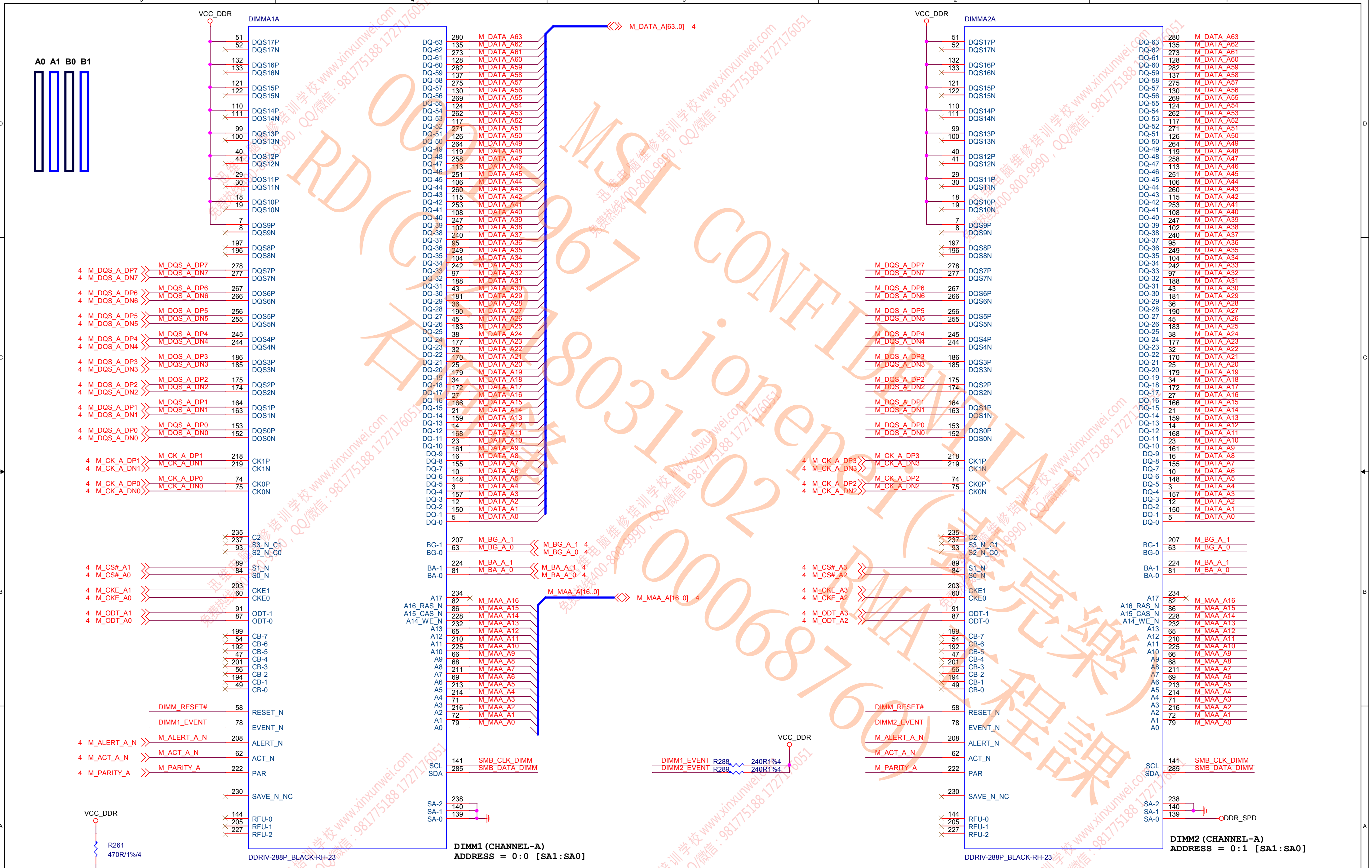
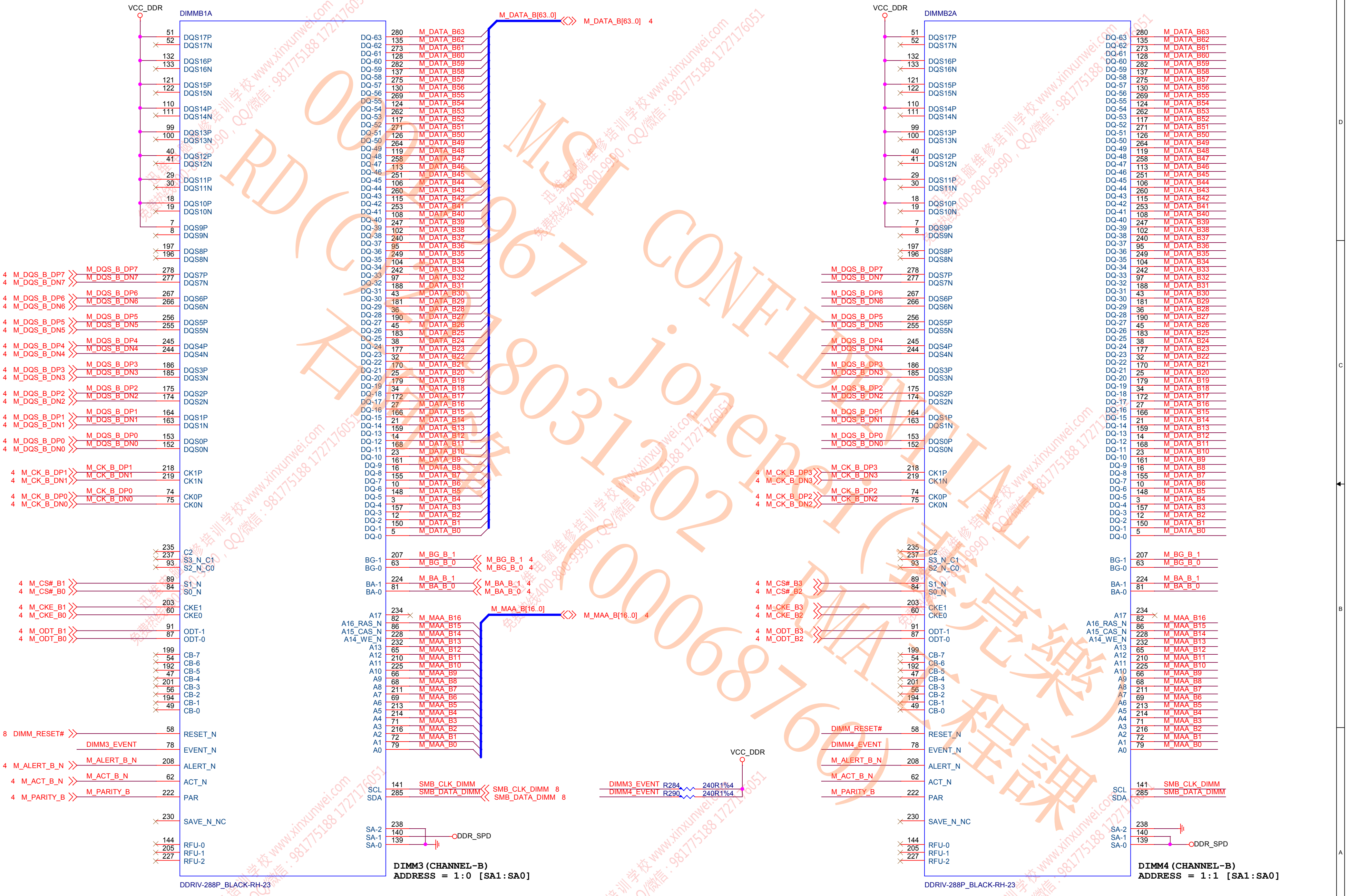
Size	Document Description	Rev
Custom	CPU-GND	20

Date: Friday, October 20, 2017 Sheet 7 of 63



MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size: Custom	Document Description: DDR4 SLOT-DIMM1/DIMM2	Rev: 20
Date: Friday, October 20, 2017	Sheet 8 of 63	



MICRO-STAR INT'L CO.,LTD

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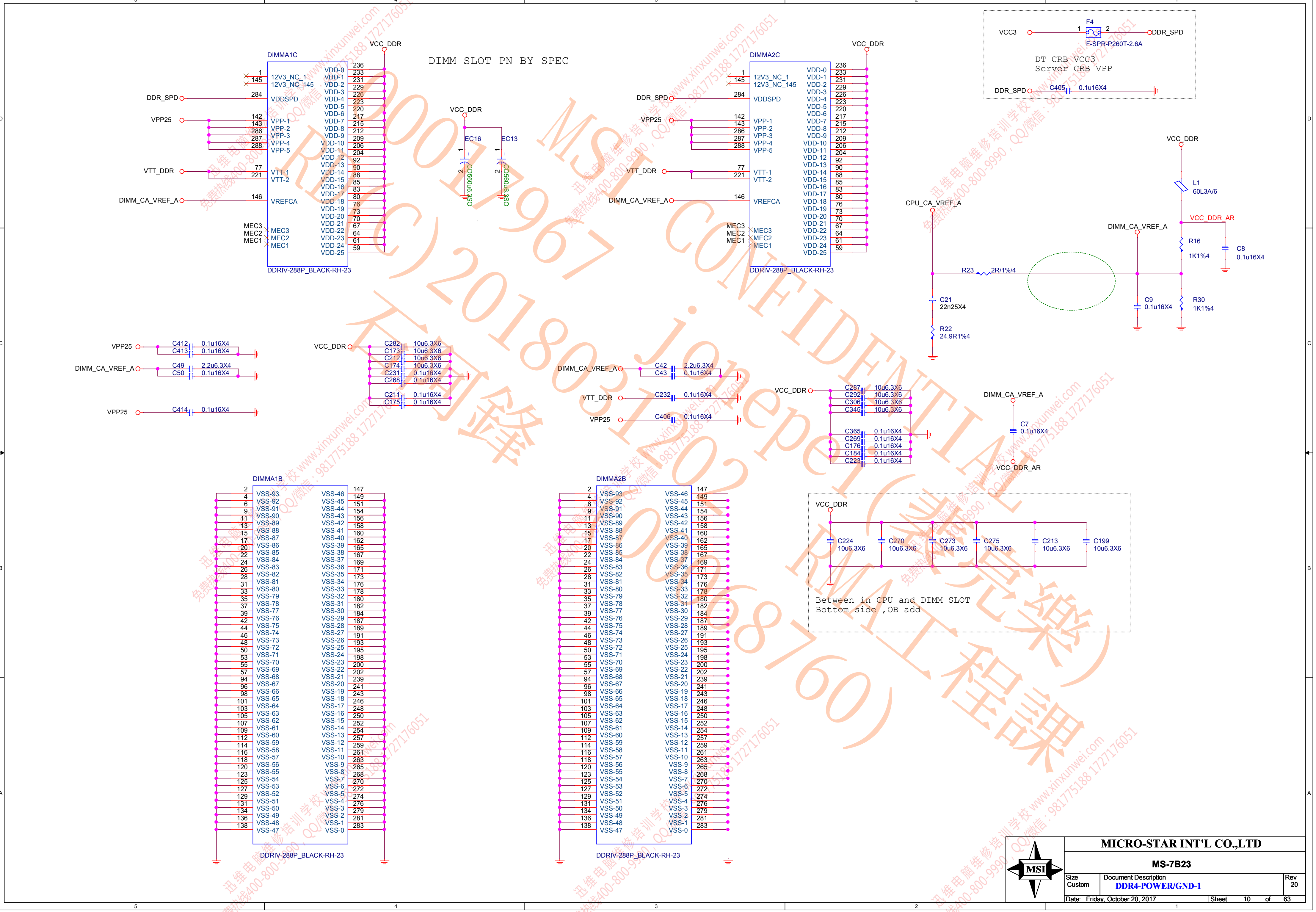
Size	Document Description	Rev
Custom	DDR4 DIMM 2	20

Date: Friday, October 20, 2017 | Sheet 9 of 63


DIMM SLOT PN BY SPEC
DIMMA1C
DDRIV-288P_BLACK-RH-23
DIMMA2C
DDRIV-288P_BLACK-RH-23
DIMMA1B
DDRIV-288P_BLACK-RH-23
DIMMA2B
DDRIV-288P_BLACK-RH-23
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
CPU_CA_VREF_A
VCC_DDR_AR
VCC3
F4
F-SPR-P260T-2.6A
DT CRB VCC3
Server CRB VPP
C405 0.1u16X4
EC16
EC13
CD560u6.3SO
L1 60L3A/6
R16 1K1%4
C8 0.1u16X4
R23 2R/1%/4
C21 22n25X4
R22 24.9R1%4
C9 0.1u16X4
R30 1K1%4
C7 0.1u16X4
C224 10u6.3X6
C270 10u6.3X6
C273 10u6.3X6
C275 10u6.3X6
C213 10u6.3X6
C199 10u6.3X6
Between in CPU and DIMM SLOT
Bottom side ,OB add
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size Custom
Document Description DDR4-POWER/GND-1
Rev 20
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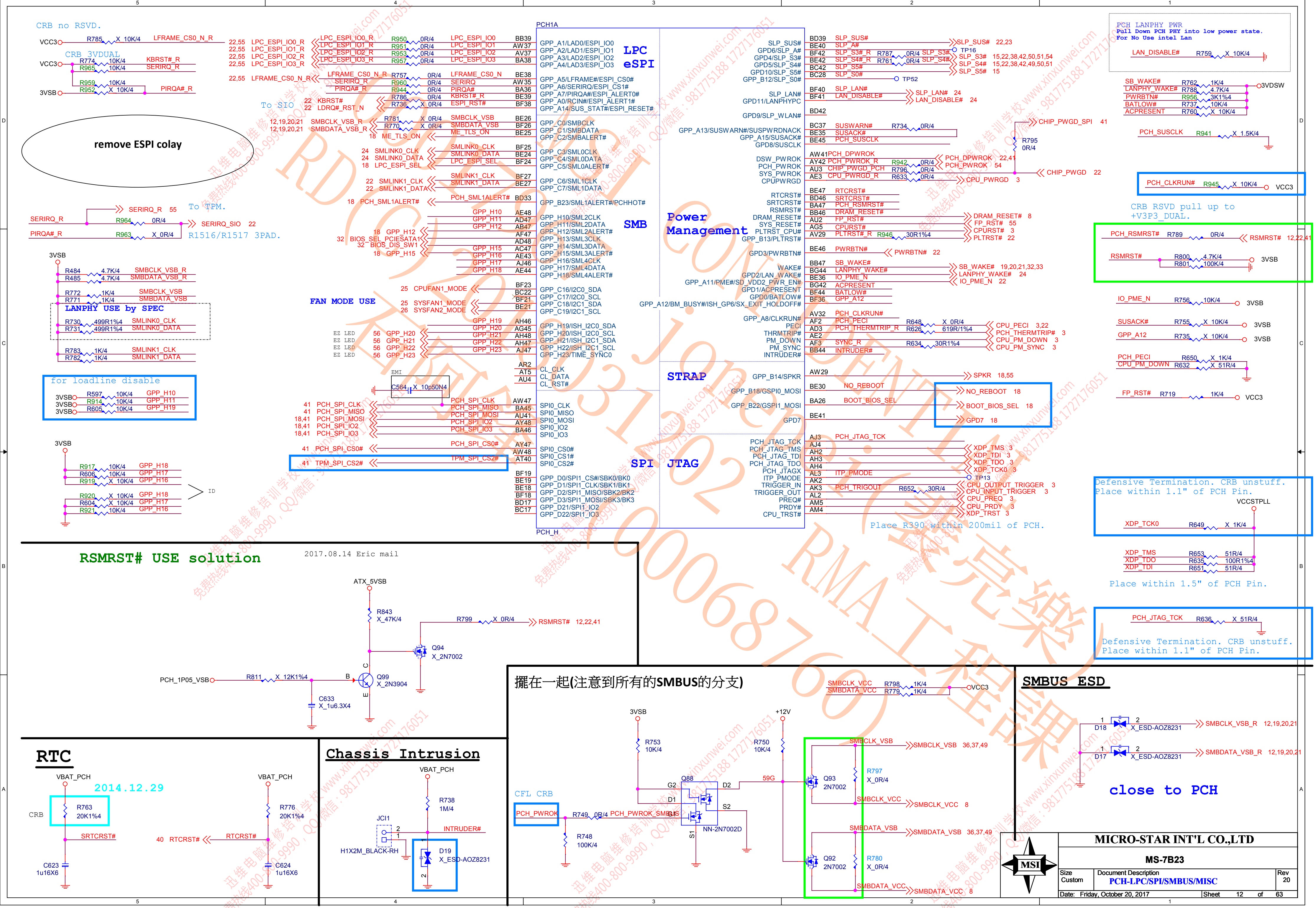
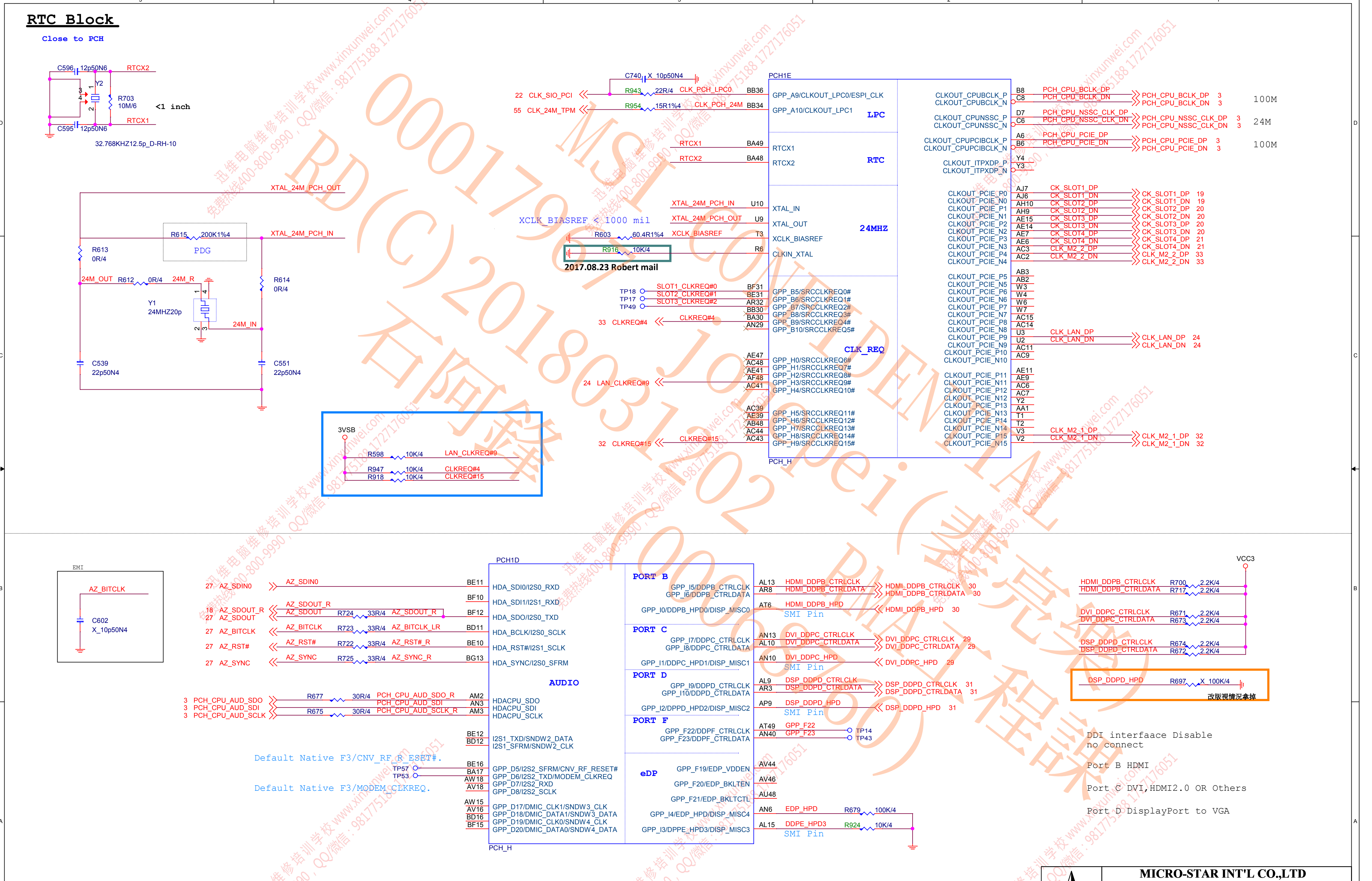
Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	20

Date: Friday, October 20, 2017 | Sheet 11 of 63



CRB no RSVD.
VCC3
R785 X_10K/4 LFRAME_CS0_N_R
CRB 3VDUAL
R774 10K/4 KBRST#_R
R965 10K/4 SERIRQ_R
3VSB
R959 10K/4
R952 X_10K/4 PIRQA#_R
remove ESPI colay
22,55 LPC_ESPI_IO0_R
22,55 LPC_ESPI_IO1_R
22,55 LPC_ESPI_IO2_R
22,55 LPC_ESPI_IO3_R
22,55 LFRAME_CS0_N_R
To SIO
22 KBRST#
22 LDRQ#_RST_N
12,19,20,21 SMBCLK_VSB_R
12,19,20,21 SMBDATA_VSB_R
18 ME_TLS_ON
24 SMLINK0_CLK
24 SMLINK0_DATA
18 LPC_ESPI_SEL
22 SMLINK1_CLK
22 SMLINK1_DATA
18 PCH_SML1ALERT#
SERIRQ_R 55
To TPM.
SERIRQ_R R964 0R/4 SERIRQ_SIO 22
PIRQA#_R R963 X_0R/4
R1516/R1517 3PAD.
R484 4.7K/4 SMBCLK_VSB_R
R485 4.7K/4 SMBDATA_VSB_R
R772 1K/4 SMBCLK_VSB
R771 1K/4 SMBDATA_VSB
LANPHY USE by SPEC
R730 499R1%4 SMLINK0_CLK
R731 499R1%4 SMLINK0_DATA
R783 1K/4 SMLINK1_CLK
R782 1K/4 SMLINK1_DATA
for loadline disable
R597 10K/4 GPP_H10
R914 10K/4 GPP_H11
R605 10K/4 GPP_H19
R917 10K/4 GPP_H18
R606 10K/4 GPP_H17
R919 X_10K/4 GPP_H16
R920 X_10K/4 GPP_H18
R604 X_10K/4 GPP_H17
R921 10K/4 GPP_H16
ID
FAN MODE USE
25 CPUFAN1_MODE
25 SYSFAN1_MODE
26 SYSFAN2_MODE
EZ LED 56 GPP_H20
EZ LED 56 GPP_H21
EZ LED 56 GPP_H22
EZ LED 56 GPP_H23
18 GPP_H12
32 BIOS_SEL_PCIESATA1
32 BIOS_SW1
18 GPP_H15
C564 X_10p50N4
41 PCH_SPI_CLK
41 PCH_SPI_MISO
18,41 PCH_SPI_MOSI
18,41 PCH_SPI_IO2
18,41 PCH_SPI_IO3
41 PCH_SPI_CS0#
41 TPM_SPI_CS2#
PCH1A
LPC eSPI
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
SMB
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_H10/SML2CLK
GPP_H11/SML2DATA
GPP_H12/SML2ALERT#
GPP_H13/SML3CLK
GPP_H14/SML3DATA
GPP_H15/SML3ALERT#
GPP_H16/SML4CLK
GPP_H17/SML4DATA
GPP_H18/SML4ALERT#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H21/ISH_I2C1_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H23/TIME_SYNC0
CL_CLK
CL_DATA
CL_RST#
SPI
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
GPP_D0/SPI1_CS#/SBK0/BK0
GPP_D1/SPI1_CLK/SBK1/BK1
GPP_D2/SPI1_MISO/SBK2/BK2
GPP_D3/SPI1_MOSI/SBK3/BK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
PCH_H
Power Management
SLP_SUS#
GPD6/SLP_A#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPP_B12/SLP_S0#
SLP_LAN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
GPD8/SUSCLK
DSW_PWROK
PCH_PWROK
SYS_PWROK
CPUPWRGD
RTCRST#
SRTCRST#
RSMRST#
DRAM_RESET#
SYS_RESET#
PLTRST_CPU#
GPP_B13/PLTRST#
GPD3/PWRBTN#
WAKE#
GPD2/LAN_WAKE#
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
PECI
THRMTRIP#
PM_DOWN
PM_SYNC
INTRUDER#
STRAP
GPP_B14/SPKR
GPP_B18/GSPI0_MOSI
GPP_B22/GSPI1_MOSI
GPD7
JTAG
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAGX
ITP_PMODE
TRIGGER_IN
TRIGGER_OUT
PREQ#
PRDY#
CPU_TRST#
SLP_SUS# 22,23
TP16
SLP_S3# 15,22,38,42,50,51,54
SLP_S4# 15,22,38,42,49,50,51,54
SLP_S5# 15
TP52
SLP_LAN# 24
LAN_DISABLE# 24
CHIP_PWGD_SPI 41
R795 0R/4
PCH_DPWROK 22,41
PCH_PWROK 54
CHIP_PWGD 22
CPU_PWRGD 3
DRAM_RESET# 8
FP_RST# 55
CPURST# 3
PLTRST# 22
PWRBTN# 22
SB_WAKE# 19,20,21,32,33
LANPHY_WAKE# 24
IO_PME_N 22
CPU_PECI 3,22
PCH_THERMTRIP# 3
CPU_PM_DOWN 3
CPU_PM_SYNC 3
SPKR 18,55
NO_REBOOT 18
BOOT_BIOS_SEL 18
GPD7 18
XDP_TMS 3
XDP_TDI 3
XDP_TDO 3
XDP_TCK0 3
TP13
CPU_OUTPUT_TRIGGER 3
CPU_INPUT_TRIGGER 3
CPU_PREQ 3
CPU_PRDY 3
XDP_TRST 3
Place R390 within 200mil of PCH.
PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
LAN_DISABLE# R759 X_10K/4
SB_WAKE# R762 1K/4 3VDSW
LANPHY_WAKE# R788 4.7K/4
PWRBTN# R956 3K1%4
BATLOW# R737 10K/4
ACPRESENT R760 X_10K/4
PCH_SUSCLK R941 X_1.5K/4
PCH_CLKRUN# R945 X_10K/4 VCC3
CRB RSVD pull up to +V3P3_DUAL.
PCH_RSMRST# R789 0R/4 RSMRST# 12,22,41
RSMRST# R800 4.7K/4 3VSB
R801 100K/4
IO_PME_N R756 10K/4 3VSB
SUSACK# R755 X_10K/4 3VSB
GPP_A12 R735 X_10K/4 3VSB
PCH_PECI R650 X_1K/4
CPU_PM_DOWN R632 X_51R/4
FP_RST# R719 1K/4 VCC3
Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.
VCCSTPLL
XDP_TCK0 R649 X_1K/4
XDP_TMS R653 51R/4
XDP_TDO R635 100R1%4
XDP_TDI R651 51R/4
Place within 1.5" of PCH Pin.
PCH_JTAG_TCK R636 X_51R/4
Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.
RSMRST# USE solution
2017.08.14 Eric mail
ATX_5VSB
R843 X_47K/4
R799 X_0R/4 RSMRST# 12,22,41
Q94 X_2N7002
PCH_1P05_VSB R811 X_12K1%4
Q99 X_2N3904
C633 X_1u6.3X4
RTC
VBAT_PCH
2014.12.29
CRB R763 20K1%4
SRTCRST#
C623 1u16X6
VBAT_PCH
R776 20K1%4
40 RTCRST# RTCRST#
C624 1u16X6
Chassis Intrusion
VBAT_PCH
R738 1M/4
JCI1
INTRUDER#
H1X2M_BLACK-RH
D19 X_ESD-AOZ8231
摆在一起(注意到所有的SMBUS的分支)
SMBCLK_VCC R798 1K/4 VCC3
SMBDATA_VCC R779 1K/4
3VSB
+12V
R753 10K/4
R750 10K/4
Q88
59G
NN-2N7002D
CFL CRB
PCH_PWROK R749 0R/4 PCH_PWROK_SMBUS
R748 100K/4
SMBCLK_VSB 36,37,49
Q93 2N7002
R797 X_0R/4
SMBCLK_VCC 8
SMBDATA_VSB 36,37,49
Q92 2N7002
R780 X_0R/4
SMBDATA_VCC 8
SMBUS ESD
D18 X_ESD-AOZ8231 SMBCLK_VSB_R 12,19,20,21
D17 X_ESD-AOZ8231 SMBDATA_VSB_R 12,19,20,21
close to PCH
MICRO-STAR INT'L CO.,LTD
MSI
MS-7B23
Size Custom
Document Description PCH-LPC/SPI/SMBUS/MISC
Rev 20
Date: Friday, October 20, 2017
Sheet 12 of 63



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-Audio/Display/Clock	20

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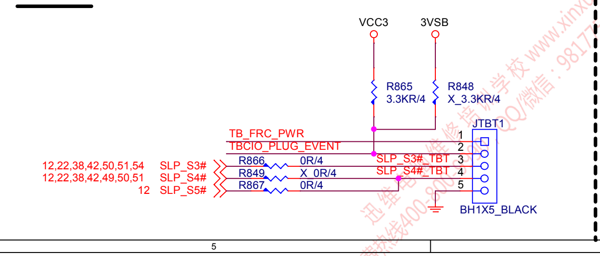
GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)

	GPP_I12	GPP_I13	GPP_I14
MORTAR	0	0	0
MORTAR ARCTIC	0	0	1
BAZOOKA PLUS	0	1	0

JTBT

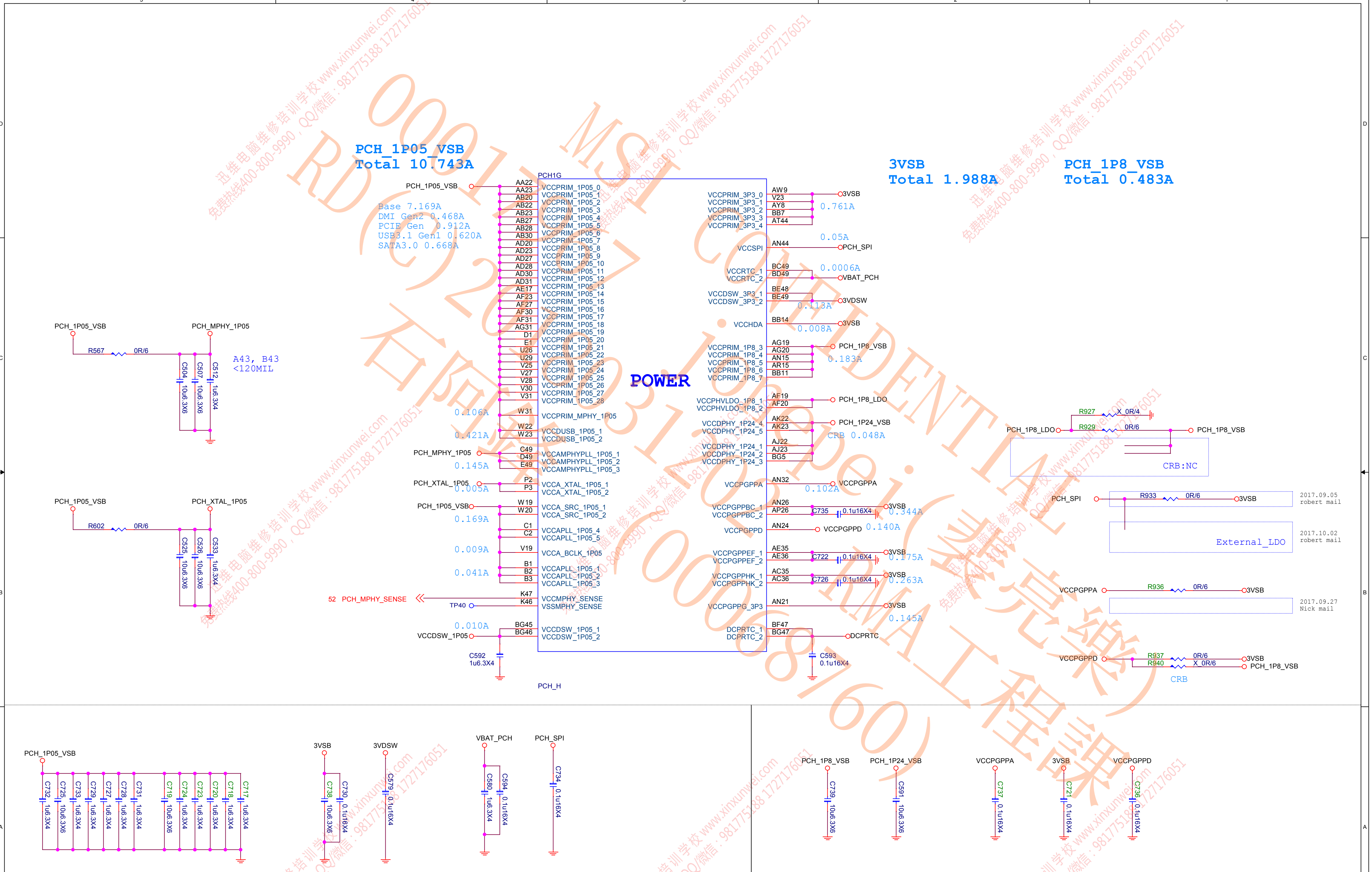


MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	PCH-GPIO/USBOC#/SATASTRAP	20

Date: Friday, October 20, 2017 Sheet 15 of 63

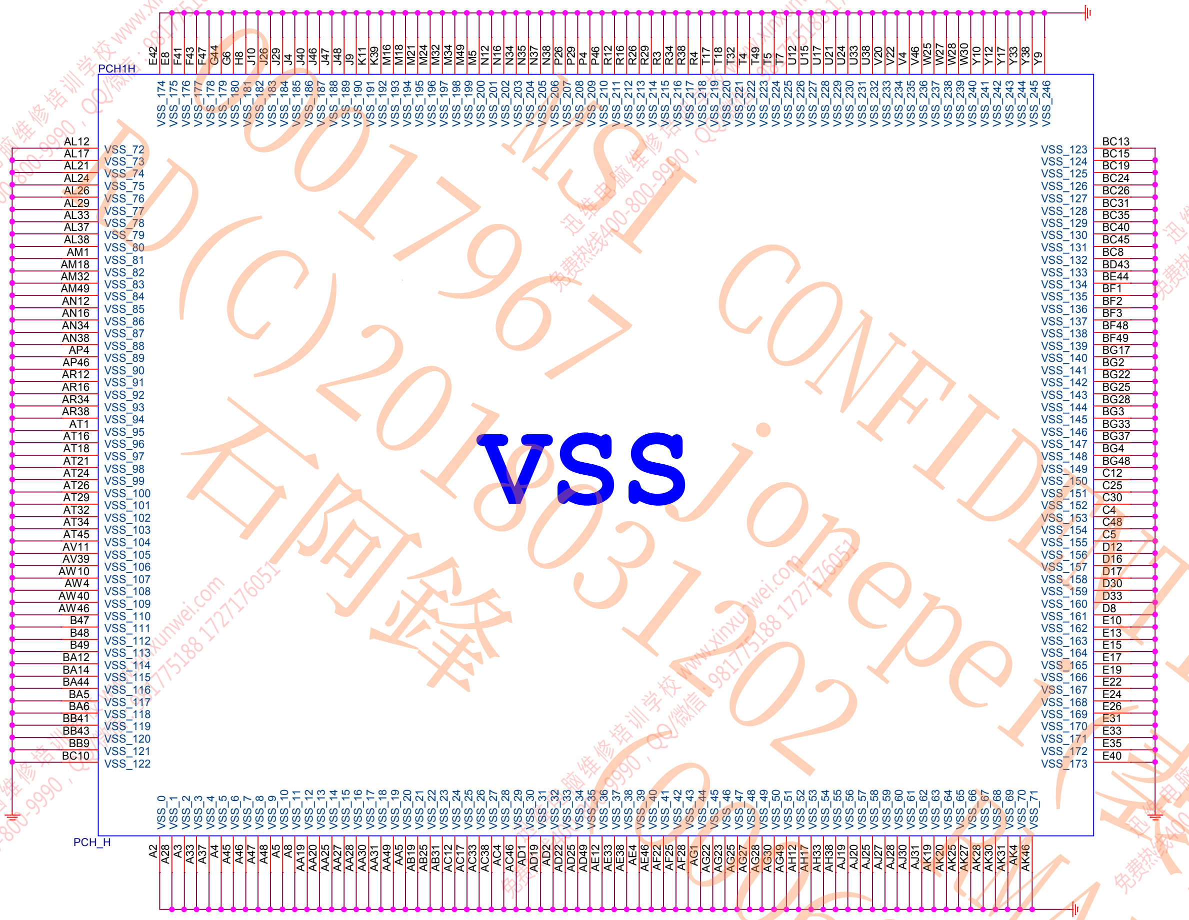


MICRO-STAR INT'L CO.,LTD

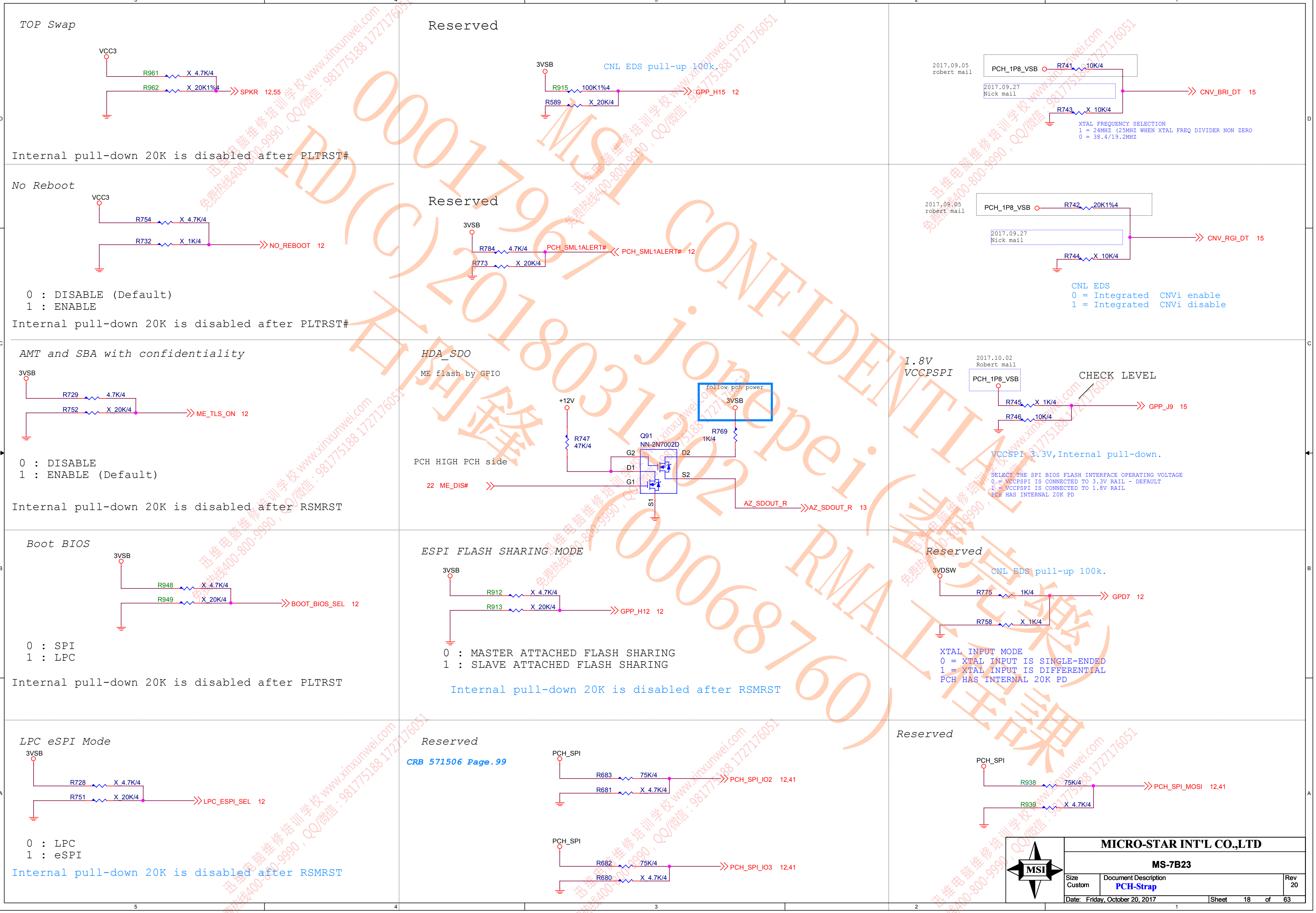
MS-7B23

Size	Document Description	Rev
Custom	PCH-Power	20

Date: Friday, October 20, 2017 Sheet 16 of 63



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B23	
Size: Custom	Document Description: PCH-GND	Rev: 20
Date: Friday, October 20, 2017	Sheet 17 of 63	


TOP Swap
VCC3
R961 X 4.7K/4
R962 X 20K1%4
SPKR 12,55
Internal pull-down 20K is disabled after PLTRST#
No Reboot
VCC3
R754 X 4.7K/4
R732 X 1K/4
NO_REBOOT 12
0 : DISABLE (Default)
1 : ENABLE
Internal pull-down 20K is disabled after PLTRST#
AMT and SBA with confidentiality
3VSB
R729 4.7K/4
R752 X 20K/4
ME_TLS_ON 12
0 : DISABLE
1 : ENABLE (Default)
Internal pull-down 20K is disabled after RSMRST
Boot BIOS
3VSB
R948 X 4.7K/4
R949 X 20K/4
BOOT_BIOS_SEL 12
0 : SPI
1 : LPC
Internal pull-down 20K is disabled after PLTRST
LPC eSPI Mode
3VSB
R728 X 4.7K/4
R751 X 20K/4
LPC_ESPI_SEL 12
0 : LPC
1 : eSPI
Internal pull-down 20K is disabled after RSMRST
Reserved
3VSB
CNL EDS pull-up 100k.
R915 100K1%4
R589 X 20K/4
GPP_H15 12
Reserved
3VSB
R784 4.7K/4
R773 X 20K/4
PCH_SML1ALERT#
PCH_SML1ALERT# 12
HDA_SDO
ME flash by GPIO
PCH HIGH PCH side
+12V
R747 47K/4
follow pch power
3VSB
R769 1K/4
Q91 NN-2N7002D
G2 D1 G1 D2 S2 S1
22 ME_DIS#
AZ_SDOUT_R
AZ_SDOUT_R 13
ESPI FLASH SHARING MODE
3VSB
R912 X 4.7K/4
R913 X 20K/4
GPP_H12 12
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING
Internal pull-down 20K is disabled after RSMRST
Reserved
CRB 571506 Page.99
PCH_SPI
R683 75K/4
R681 X 4.7K/4
PCH_SPI_IO2 12,41
PCH_SPI
R682 75K/4
R680 X 4.7K/4
PCH_SPI_IO3 12,41
2017.09.05 robert mail
PCH_1P8_VSB
R741 10K/4
2017.09.27 Nick mail
R743 X 10K/4
CNV_BRI_DT 15
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO
0 = 38.4/19.2MHZ
2017.09.05 robert mail
PCH_1P8_VSB
R742 20K1%4
2017.09.27 Nick mail
R744 X 10K/4
CNV_RGI_DT 15
CNL EDS
0 = Integrated CNVi enable
1 = Integrated CNVi disable
1.8V VCCPSPI
2017.10.02 Robert mail
PCH_1P8_VSB
CHECK LEVEL
R745 X 1K/4
R746 10K/4
GPP_J9 15
VCCSPI 3.3V,Internal pull-down.
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD
Reserved
3VDSW
CNL EDS pull-up 100k.
R775 1K/4
R758 X 1K/4
GPD7 12
XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD
Reserved
PCH_SPI
R938 75K/4
R939 X 4.7K/4
PCH_SPI_MOSI 12,41
MSI
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size Custom
Document Description PCH-Strap
Rev 20
Date: Friday, October 20, 2017
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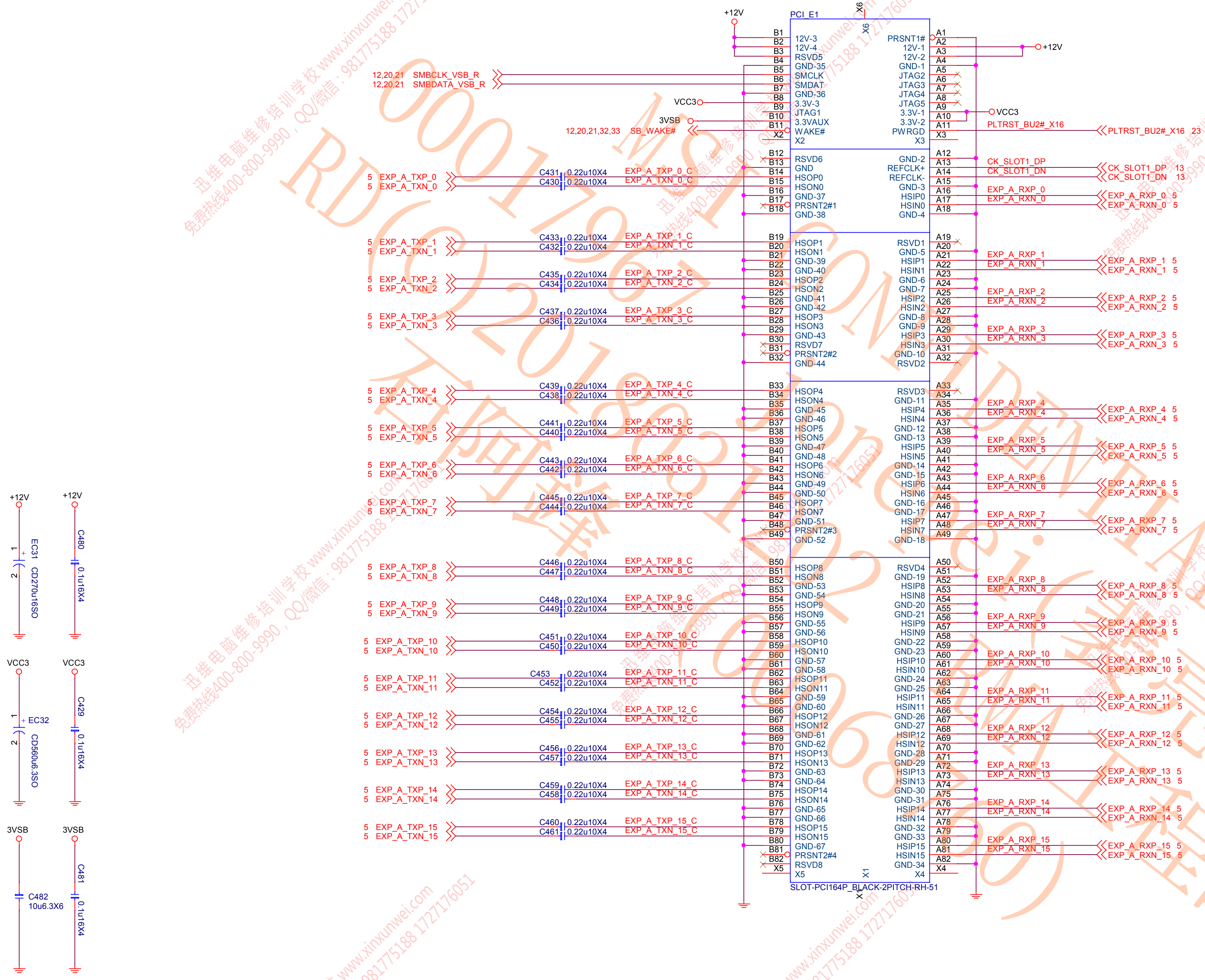

MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	PCIE SLOT-CPU(X16)	20

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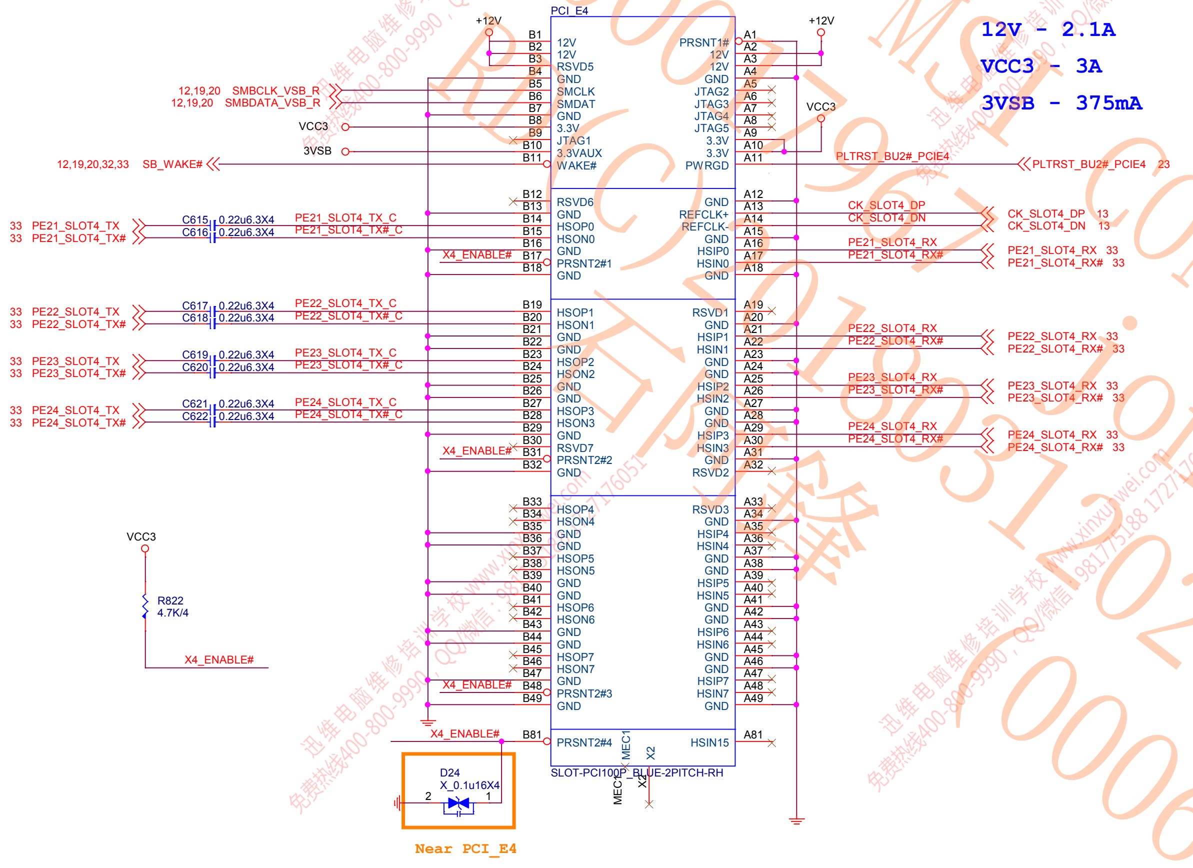
PCI Express X4 Slot

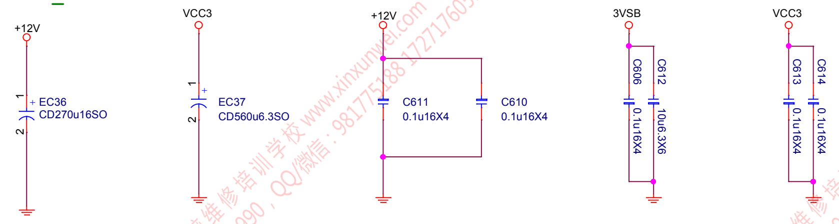


12V - 2.1A

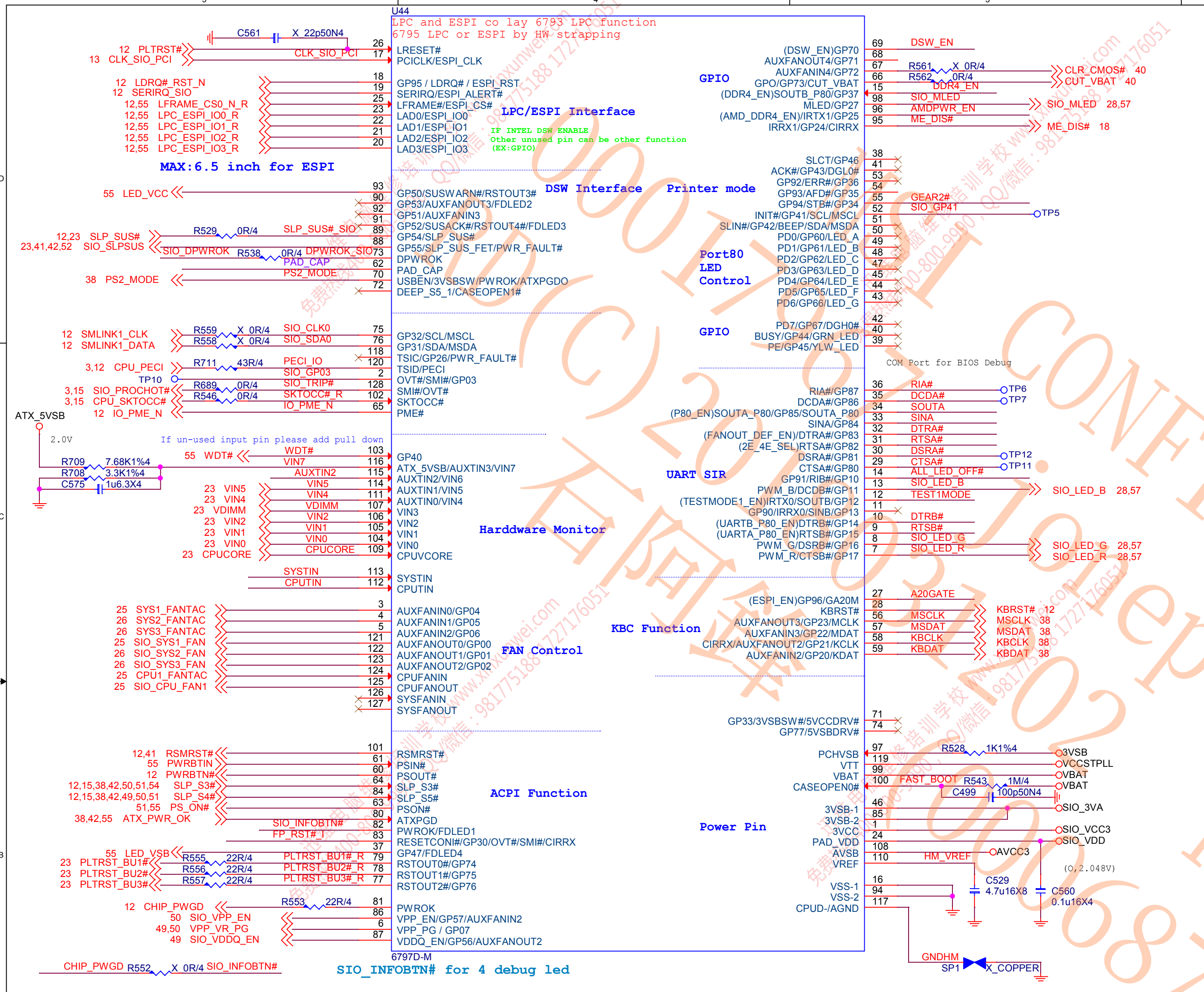
VCC3 - 3A

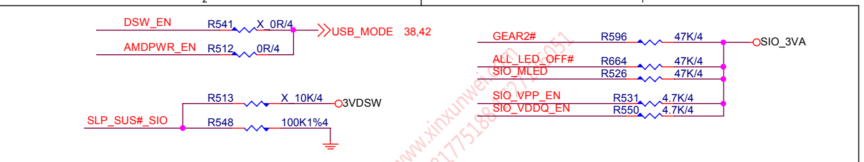
3VSB - 375mA

Near PCI_E4



MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size: Custom	Document Description: PCIE SLOT-PCH(X4)	Rev: 20
Date: Friday, October 20, 2017	Sheet 21 of 63	

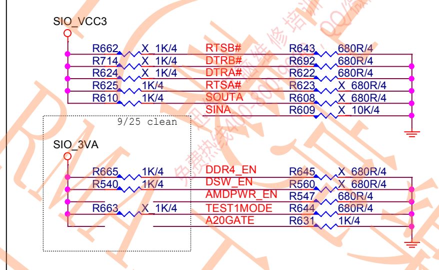




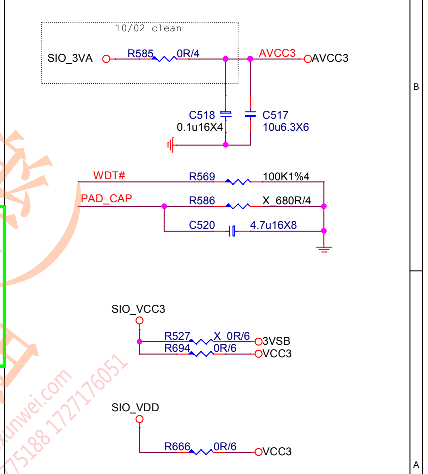
POWER ON STRAPPING PIN FOR NCT6797

PIN	NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	A20GATE	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

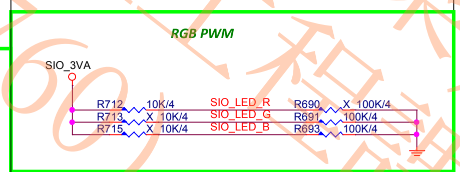
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

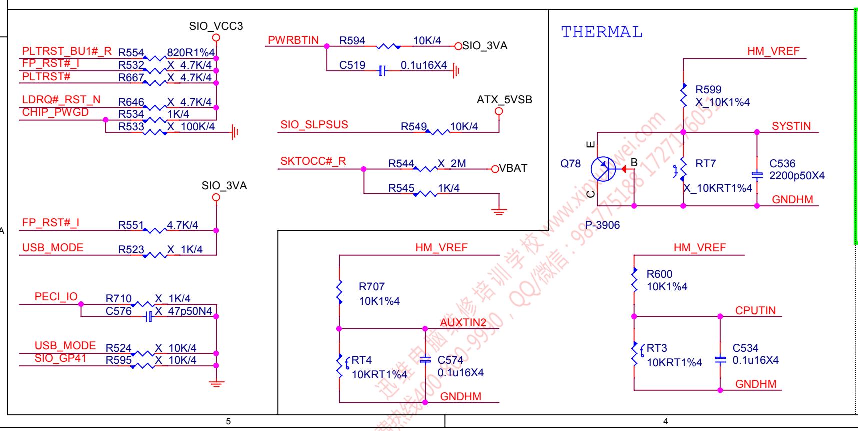


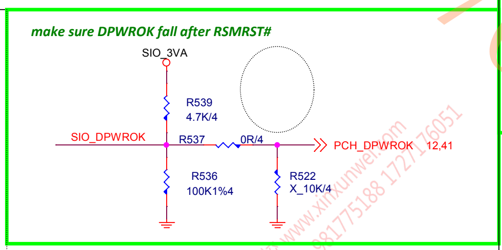
3V Analog Power



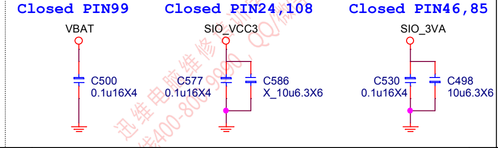
ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER







Closed PIN99 | Closed PIN24,108 | Closed PIN46,85



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Size: Custom	Document Description: SIO-NCT6793D-1		Rev: 20
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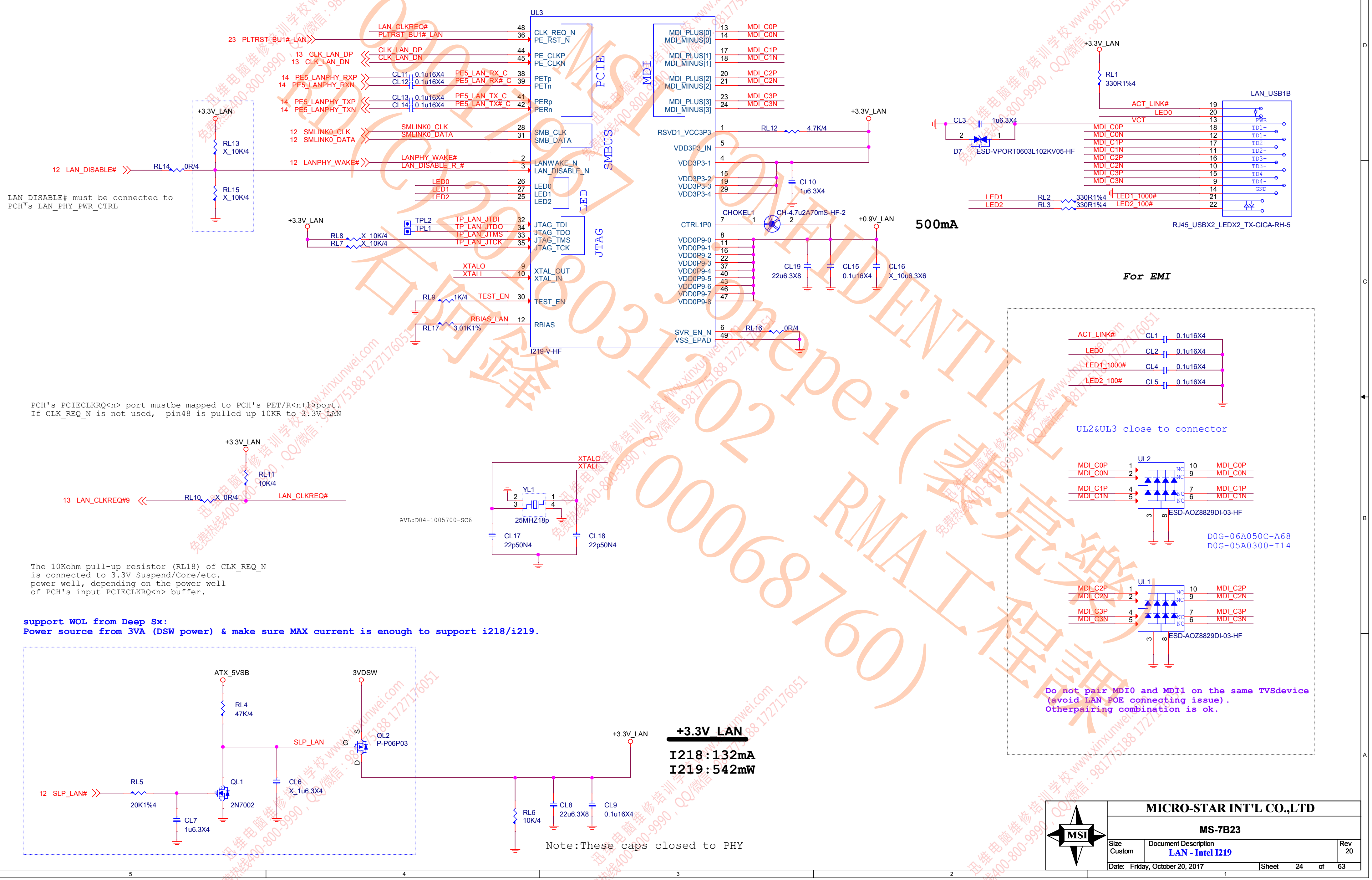
Intel Lan- i219

LAN Connector



LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue). Otherpairing combination is ok.

+3.3V_LAN

I218:132mA
I219:542mW

Note:These caps closed to PHY

MICRO-STAR INT'L CO.,LTD		
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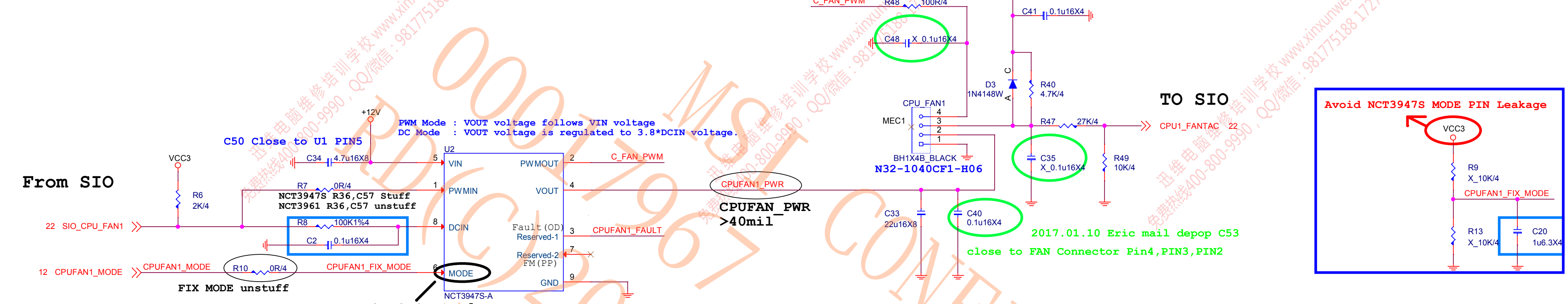
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

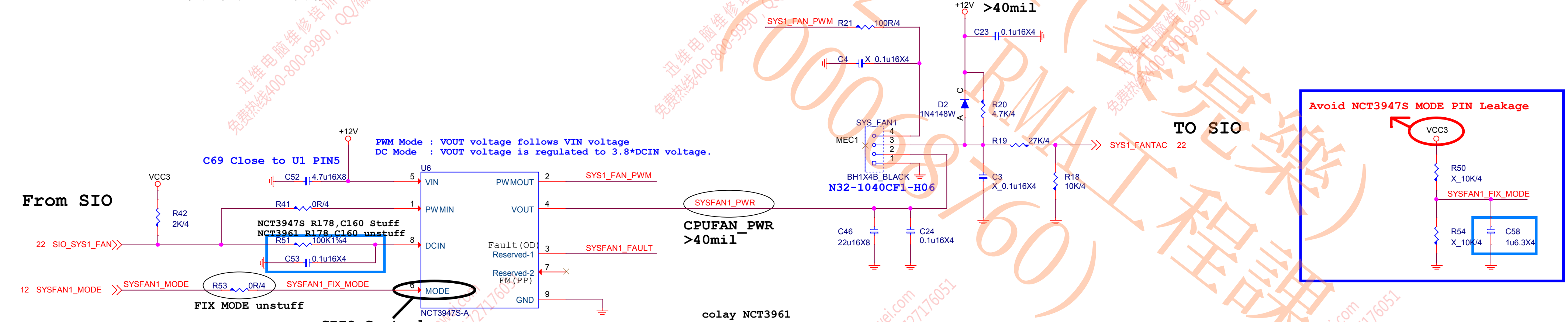
colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R5 100K/4 CPUFAN1_FAULT

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internal pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R25 100K/4 SYSFAN1_FAULT

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MS-7B23

Size: Custom | Document Description: FAN CONTROLLOR | Rev: 20

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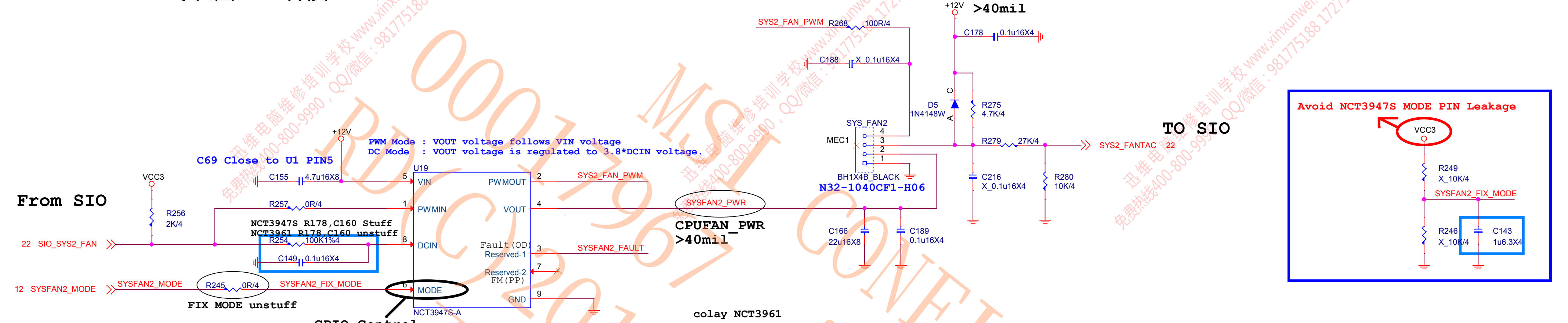
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internal pull up 1.65V

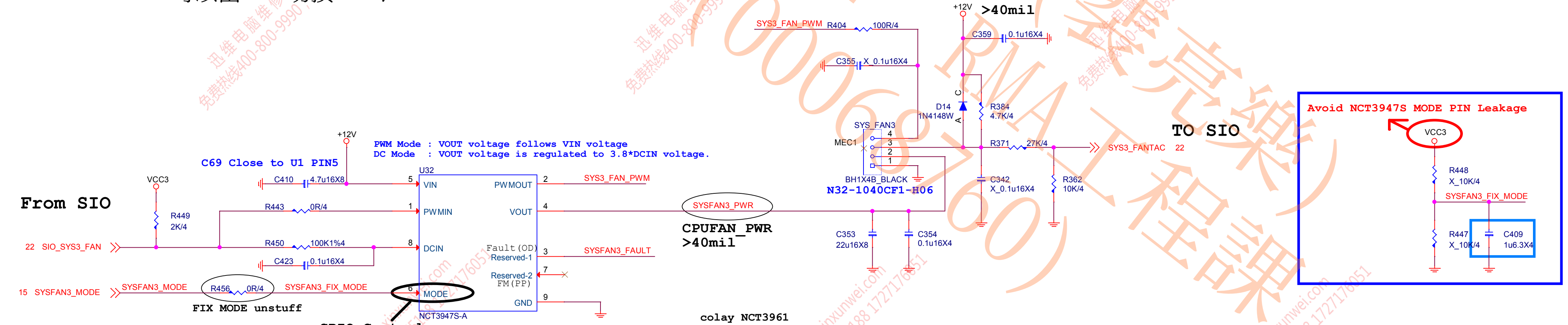
colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R269 100K/4 SYSFAN2_FAULT

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internal pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R393 100K/4 SYSFAN3_FAULT

MSI
MICRO-STAR INT'L CO.,LTD
MS-7B23

Size	Document Description	Rev
Custom	FAN CONTROLLOR	20

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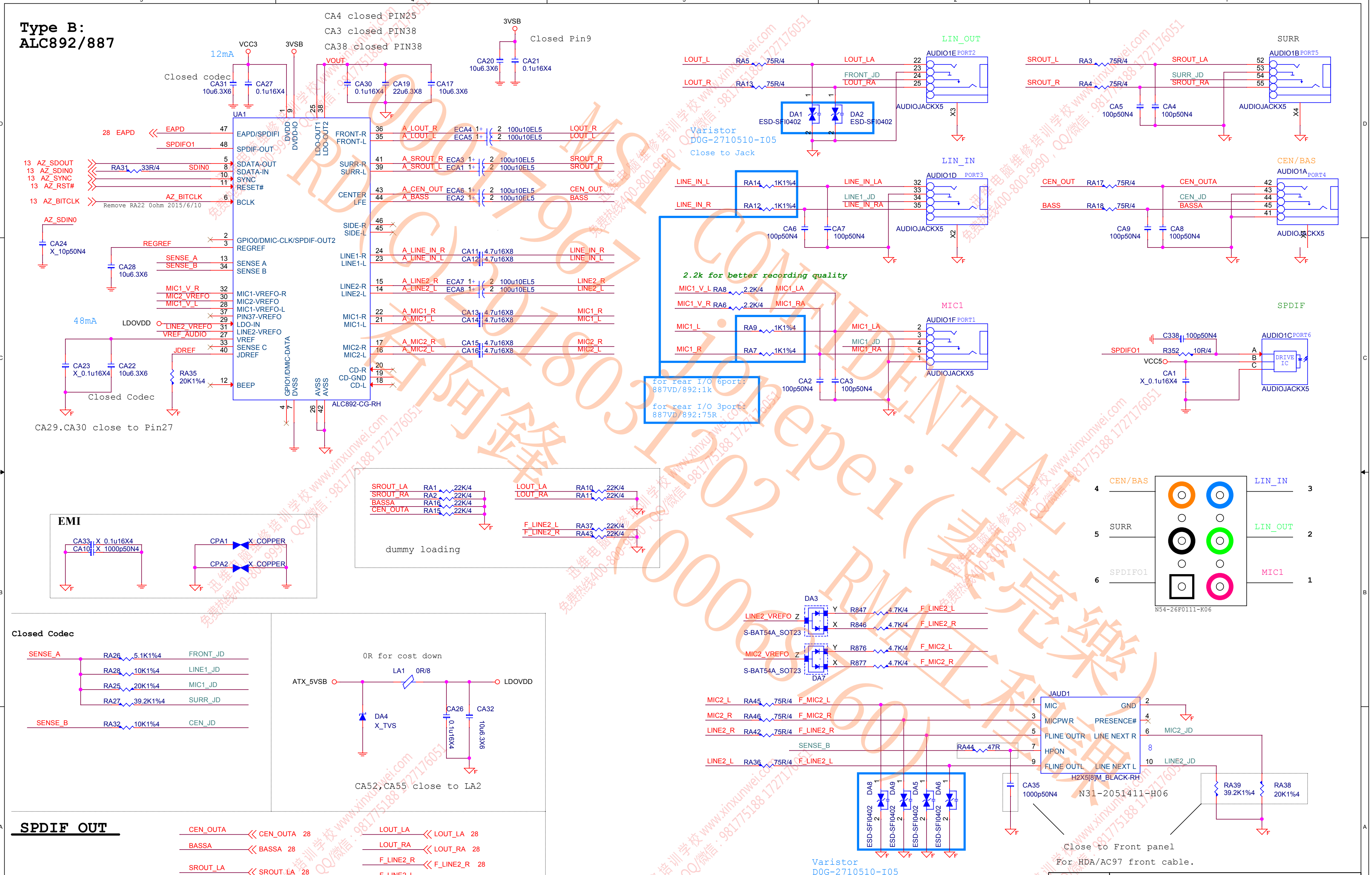

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MS-7B23

Size	Document Description	Rev
Custom	AUDIO - ALC892/887	20

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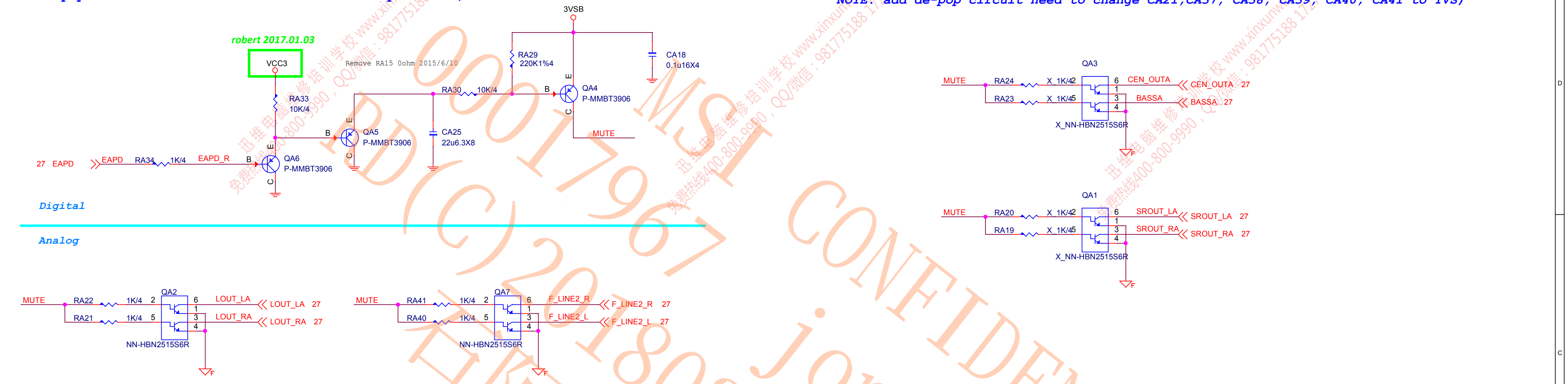
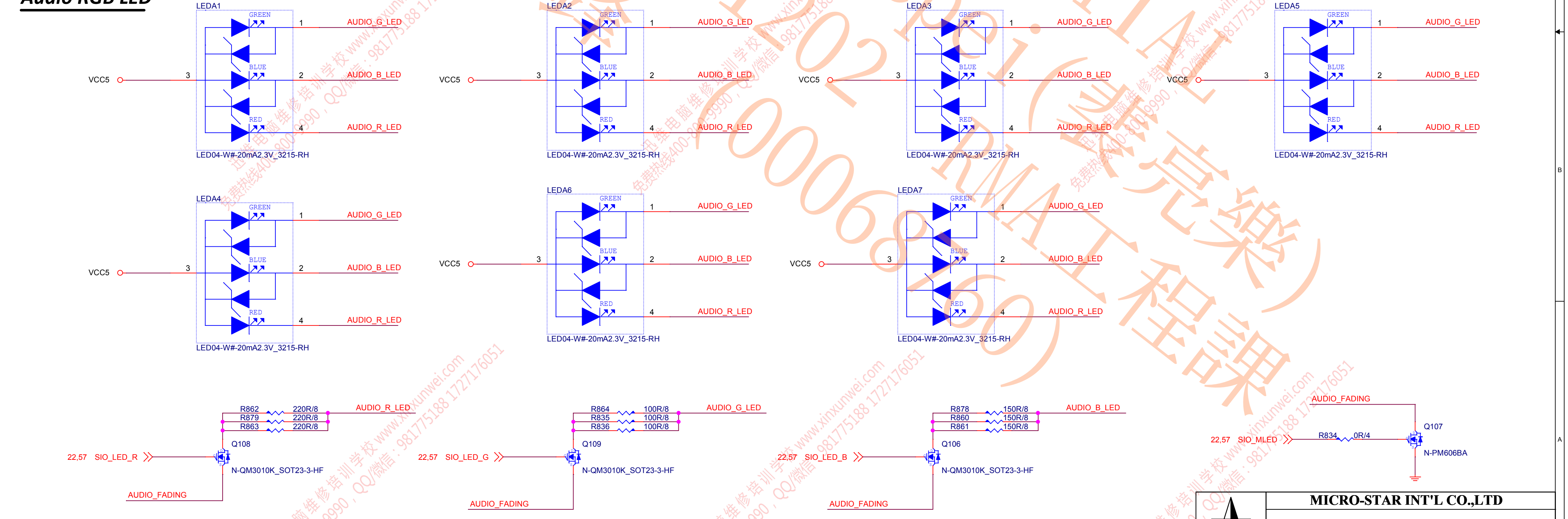
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA21,CA37, CA38, CA39, CA40, CA41 to TVS)



Audio RGB LED



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Size: Custom	Document Description: AUDIO - depop circuit — Rev 20
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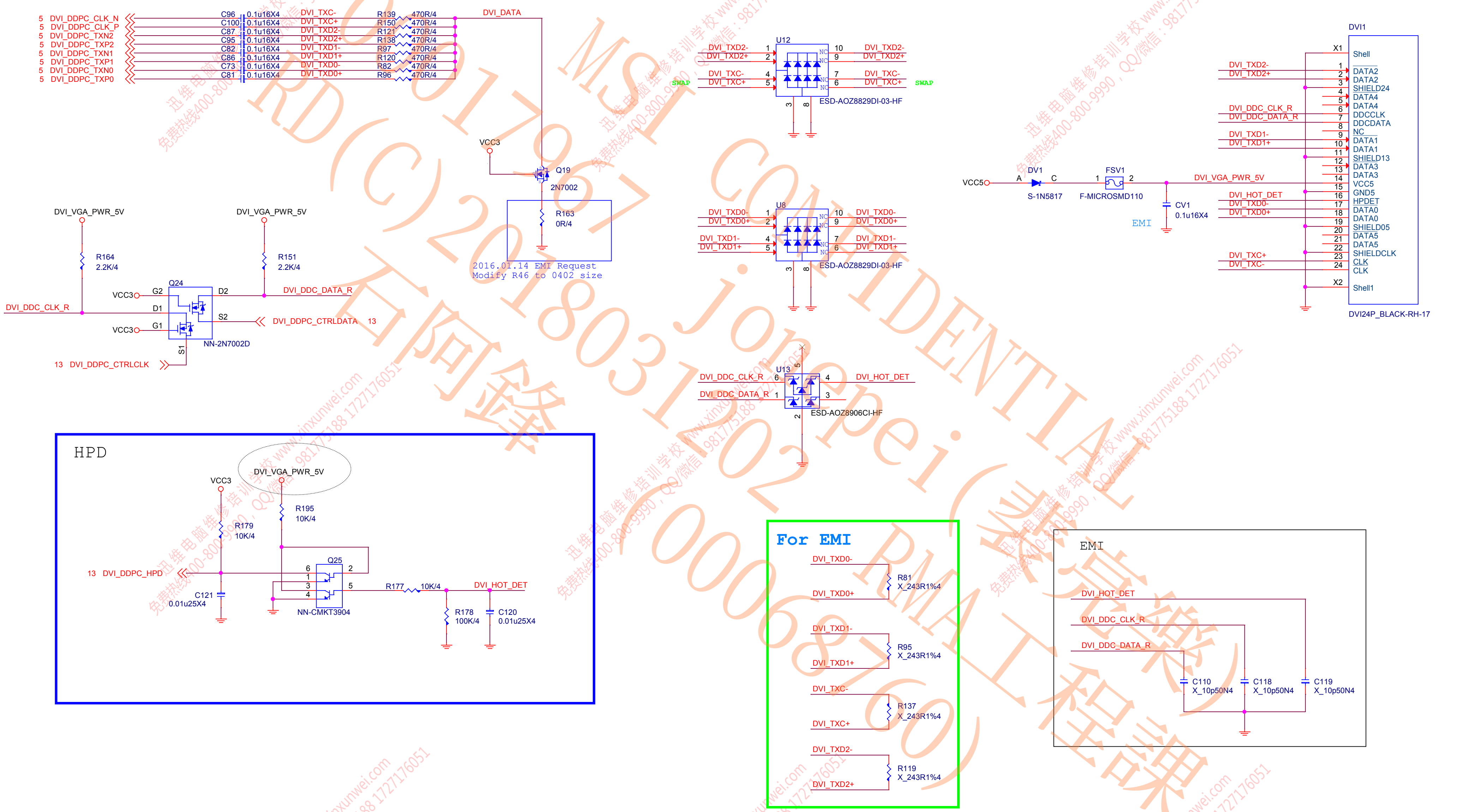
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



MSI	MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description DVI		Rev 20
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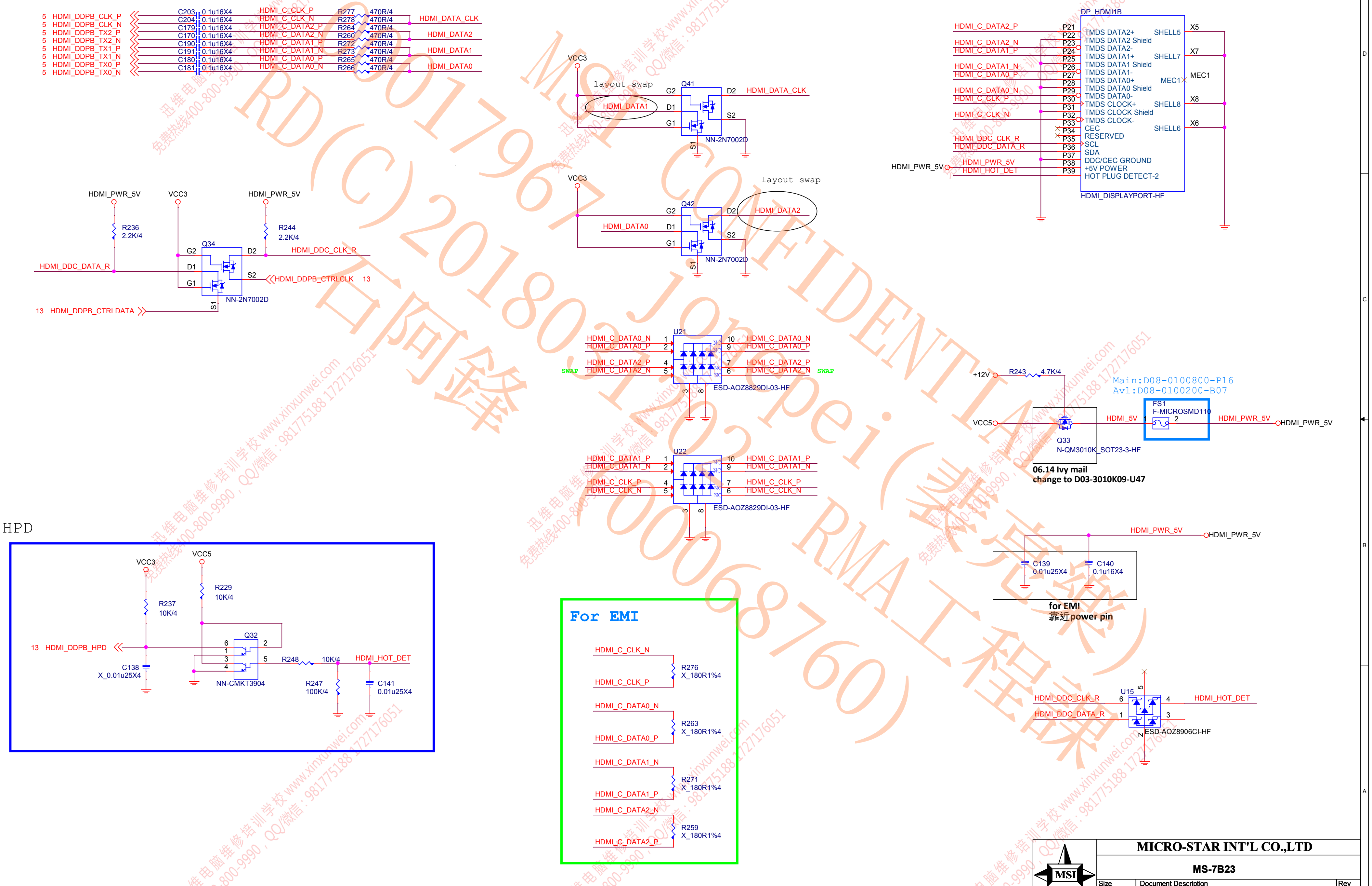
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	HDMI Connector	20

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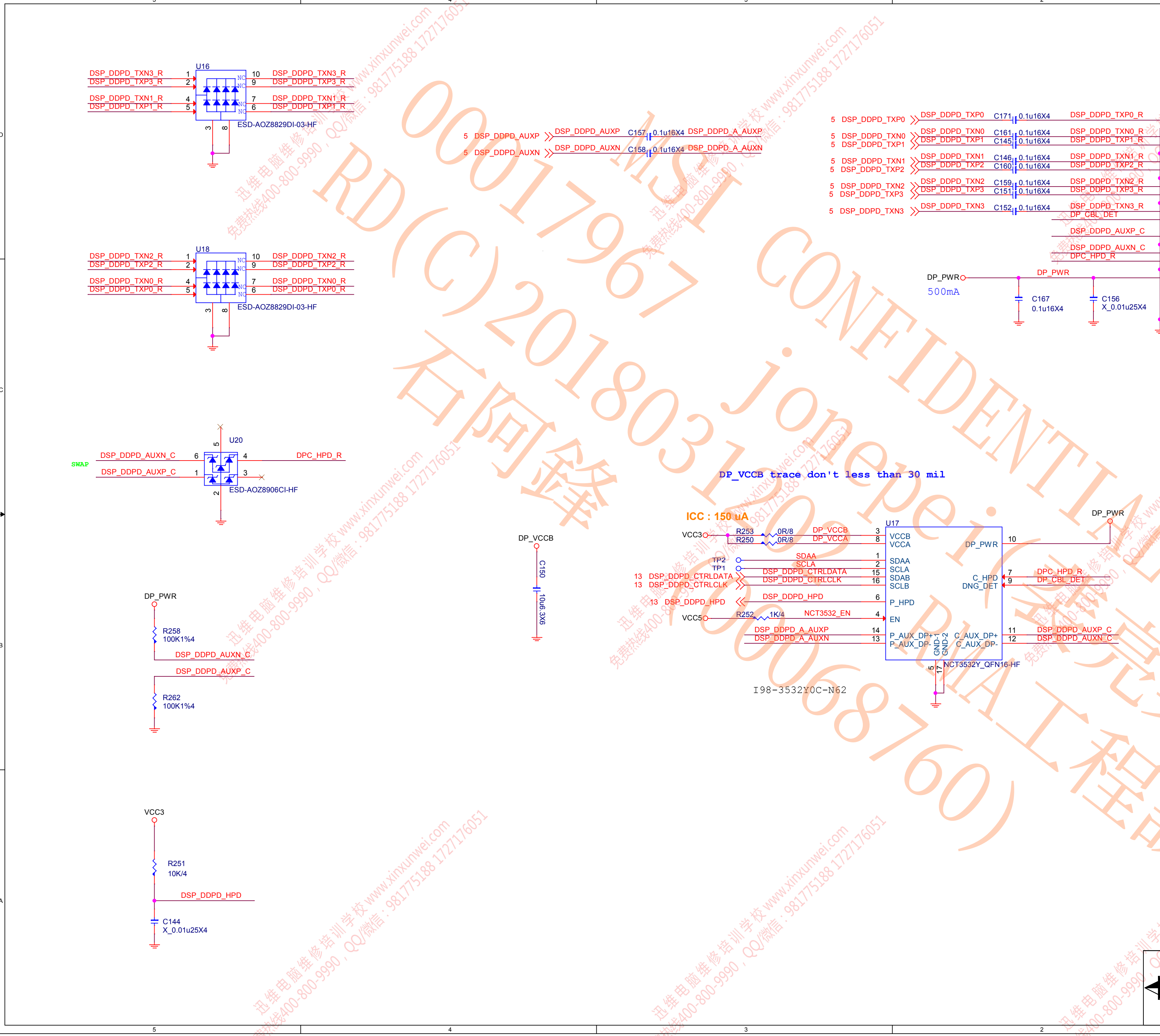

MICRO-STAR INT'L CO.,LTD	
MS-7B23	
Size: Custom	Document Description: VGA - ITE6516
Rev: 20	
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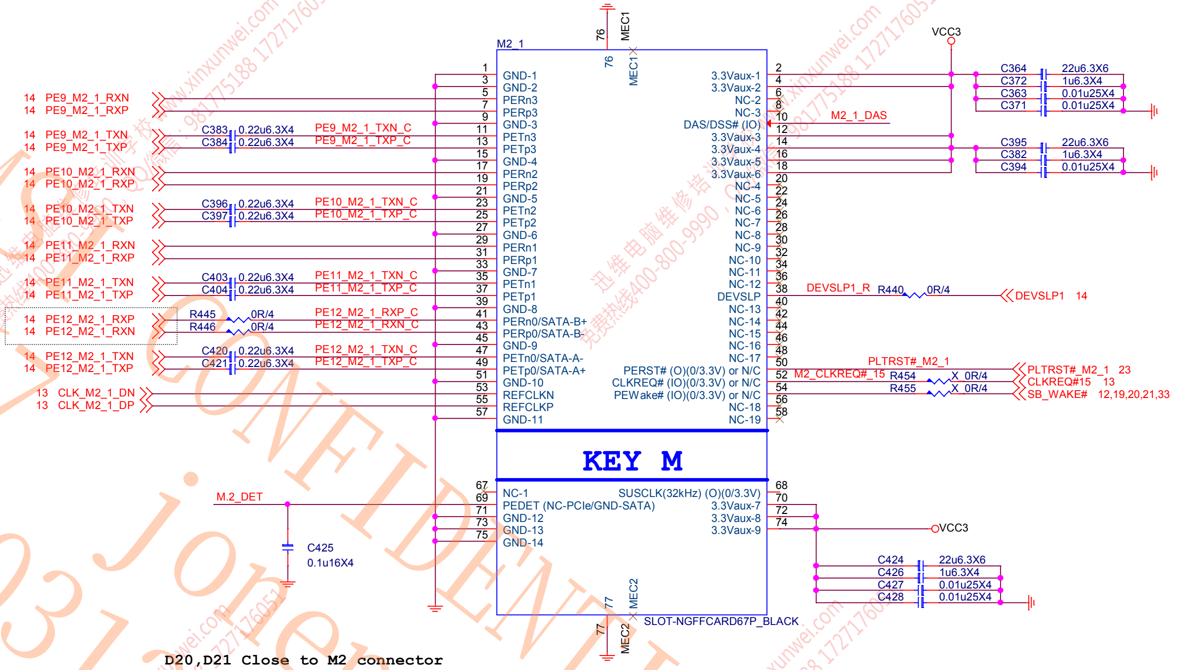
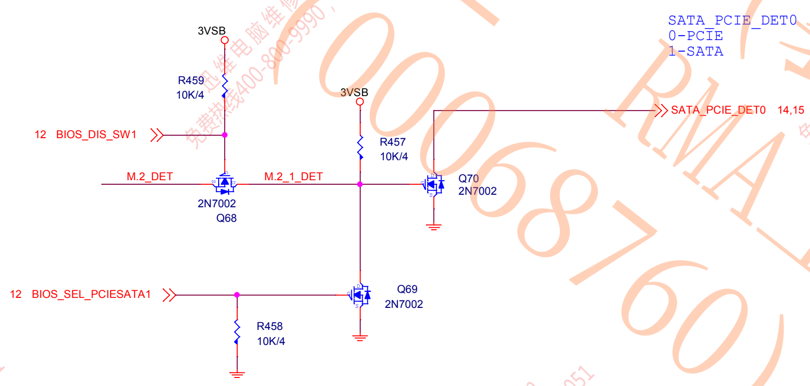
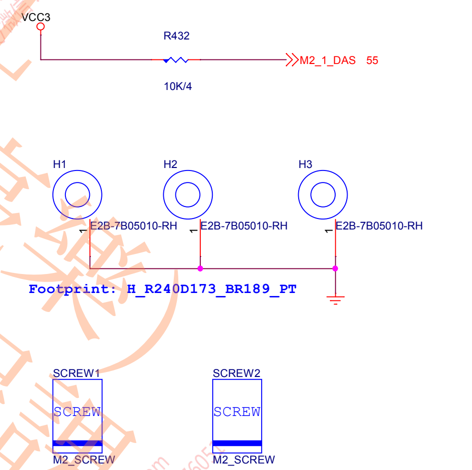


D20,D21 Close to M2 connector





BIOS_MODE

DIS_SW	*M1_SEL_PCIESATA*	***Mode***
0	*1*	***M2-SATA***
0	*0*	***M2-PCIE***
GPI	*GPI*	***AUTO***

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Size	Document Description	Rev
Custom	M.2-SLOT1	20

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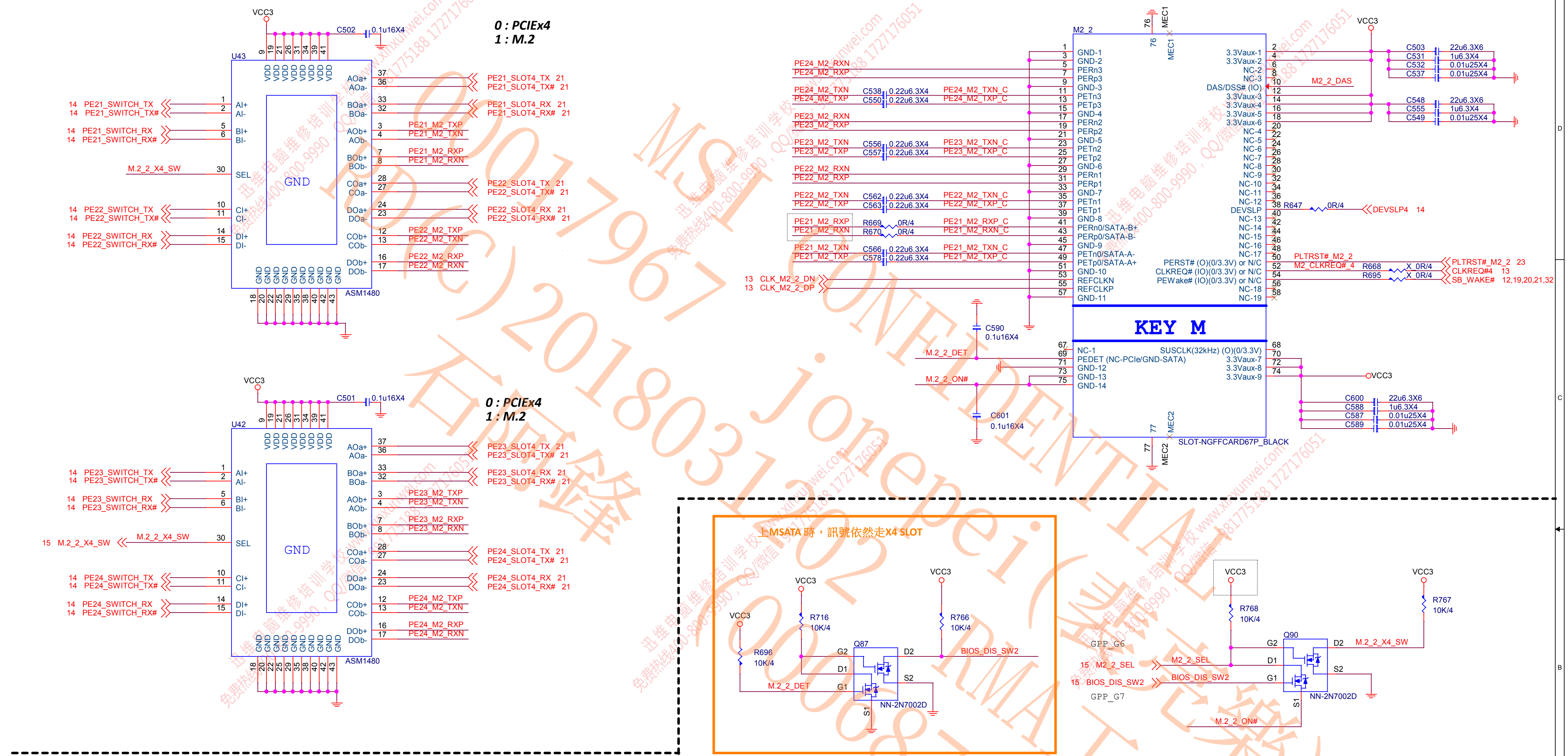

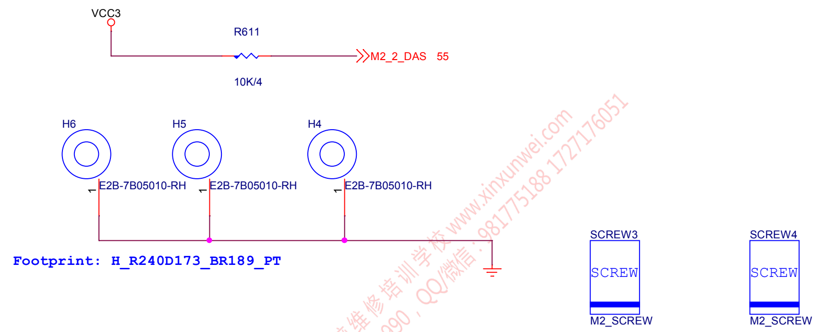

BIOS_MODE

GPP_G7 GPP_G6

BIOS_DIS_SW2	*M2_2_SEL*	*Mode*
0	0	*M2 SLOT-PCIE*
0	1	*X4 SLOT-PCIE*
GPI	*GPI*	*GPI*

MSI	MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description M.2-SLOT2		Rev 20
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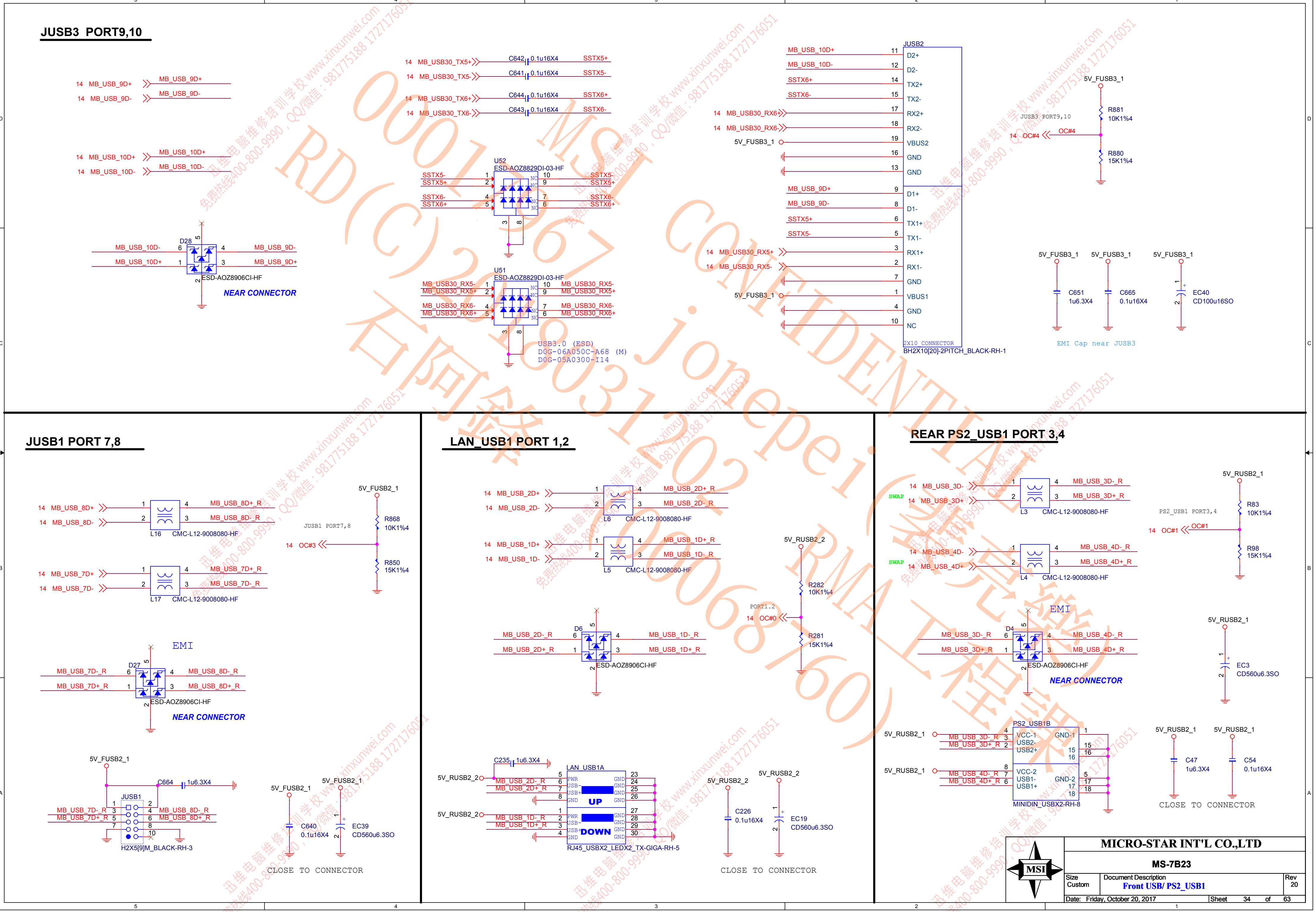

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MS-7B23		
Size: Custom	Document Description: Front USB/ PS2_USB1	Rev: 20
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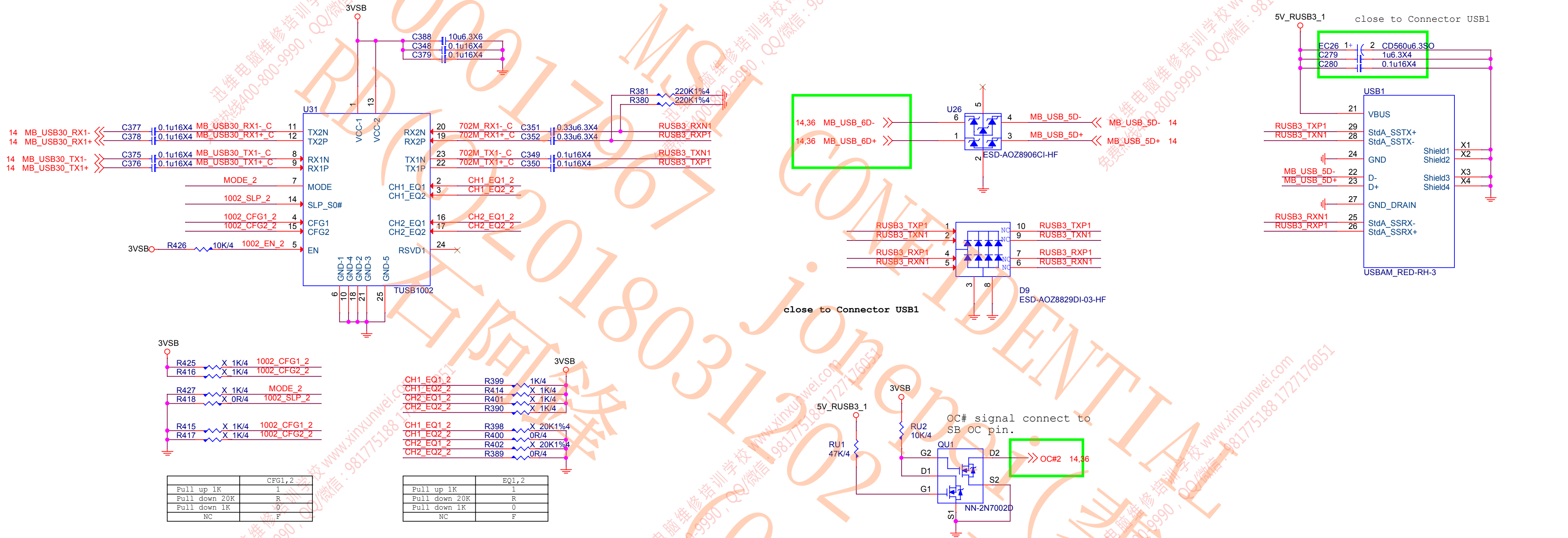
Rear TYPE A + Redriver



	CFG1,2
Pull up 1K	1
Pull down 20K	R
Pull down 1K	0
NC	F

	EQ1,2
Pull up 1K	1
Pull down 20K	R
Pull down 1K	0
NC	F

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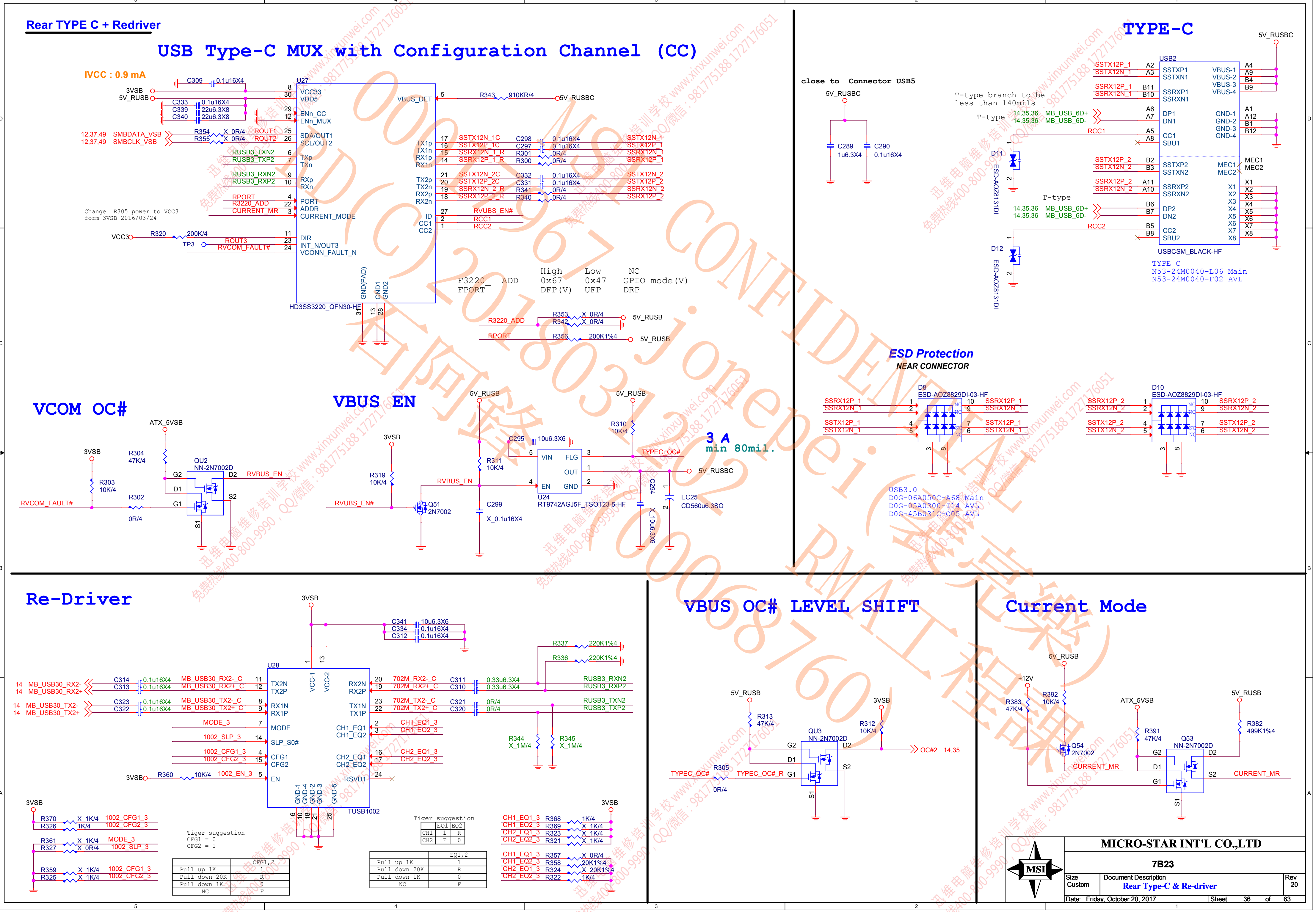
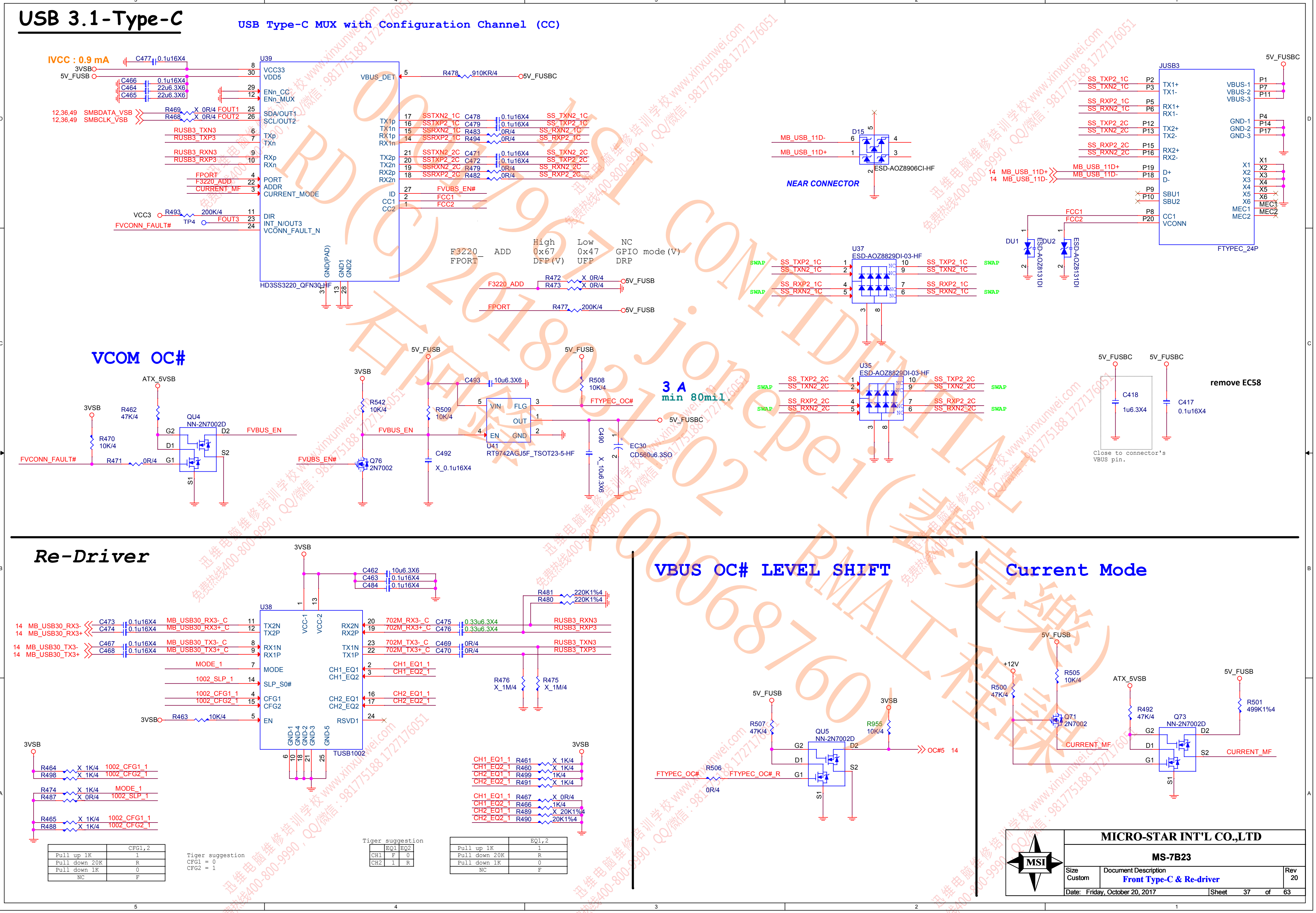


	CFG1,2
Pull up 1K	1
Pull down 20K	R
Pull down 1K	0
NC	F

	EQ1,2
Pull up 1K	1
Pull down 20K	R
Pull down 1K	0
NC	F

Tiger suggestion

	EQ1	EQ2
CH1	1	R
CH2	F	0



USB 3.1-Type-C
USB Type-C MUX with Configuration Channel (CC)
IVCC : 0.9 mA
NEAR CONNECTOR
VCOM OC#
3 A
min 80mil.
remove EC58
Close to connector's VBUS pin.
Re-Driver
VBUS OC# LEVEL SHIFT
Current Mode
Tiger suggestion
CFG1 = 0
CFG2 = 1
MICRO-STAR INT'L CO.,LTD
MS-7B23
Document Description
Front Type-C & Re-driver
Size Custom
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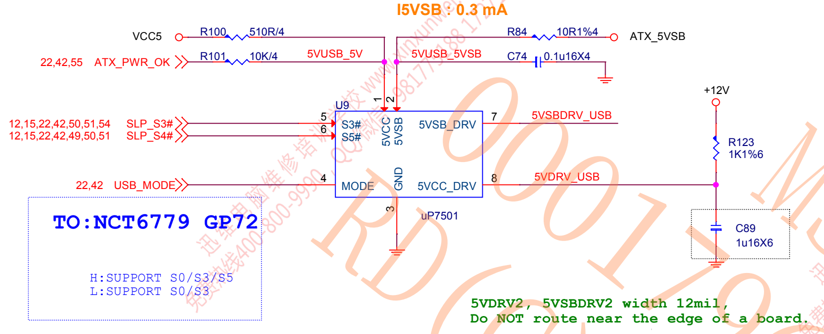
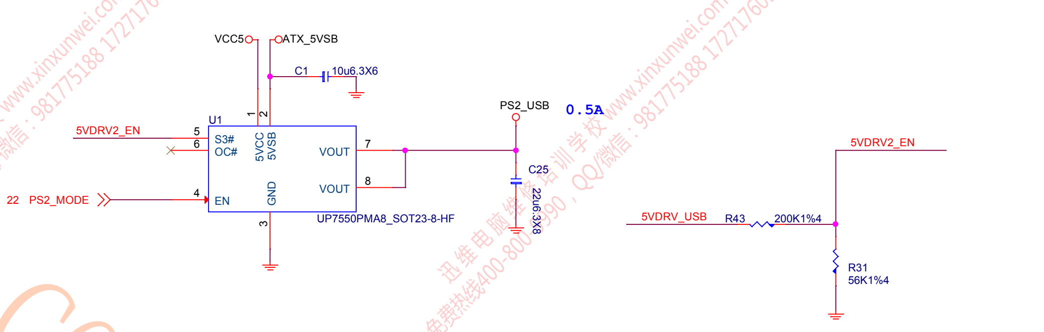
USB POWER

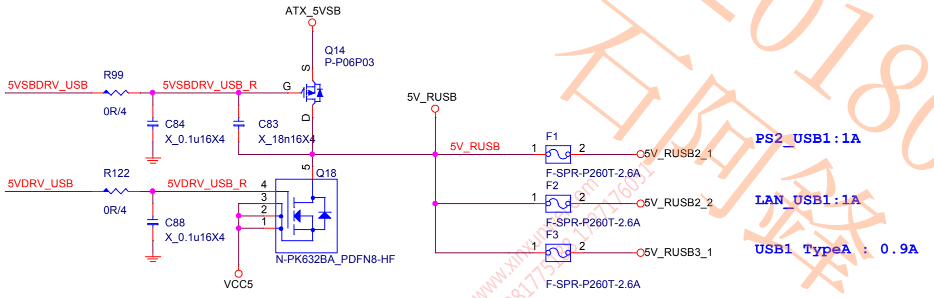


PS2 POWER

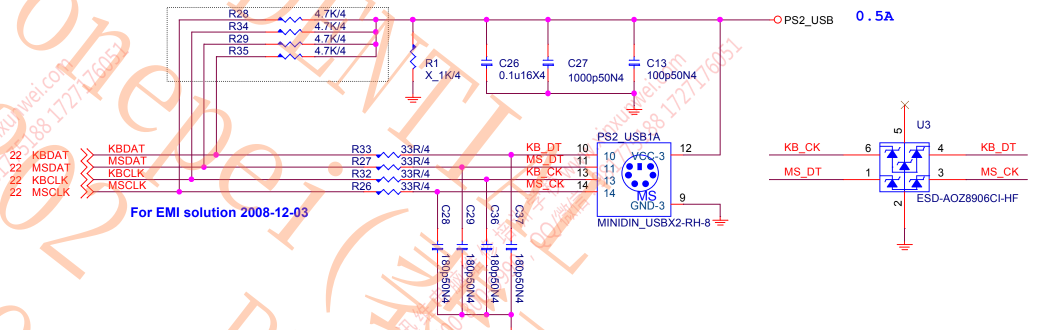
USB MODE



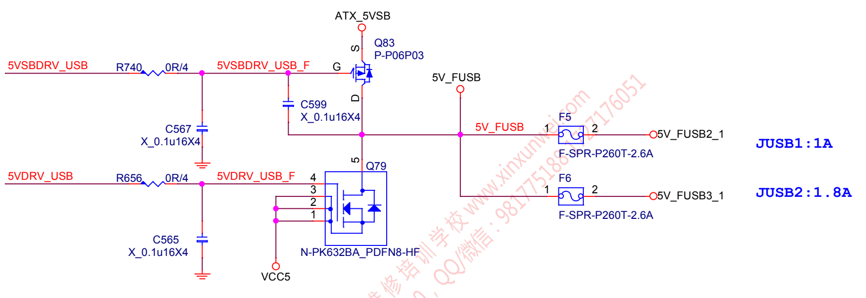
REAR USB PORT POWER



PS2 KEYBOARD & MOUSE CONNECTOR



FRONT USB PORT POWER



USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_FUSB2_1	Port5,6	OC#0
PS2_USB1	5V_RUSB2_2	Port9,10	OC#1
USB1	5V_FUSB3_1	Port1,2	OC#2
JUSB3	5V_RUSB3_1	Port3,4	OC#3
JUSB2	5V_RUSB2_1	Port7,8	OC#4

MICRO-STAR INT'L CO.,LTD

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Custom	USB Power	20

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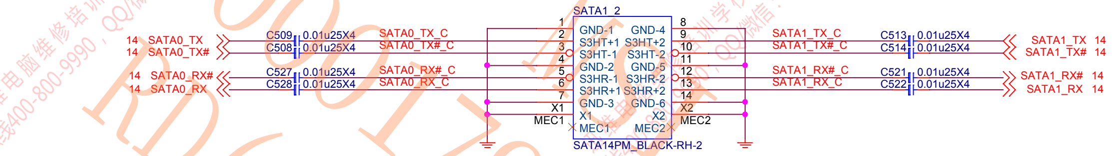
SATA PORT 0,1

Black 90 degree



SATA PORT 2,3

Black 180 degree

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: **SATA connector** — Rev 20
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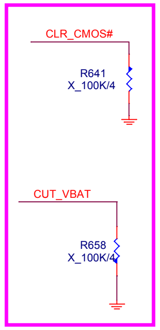
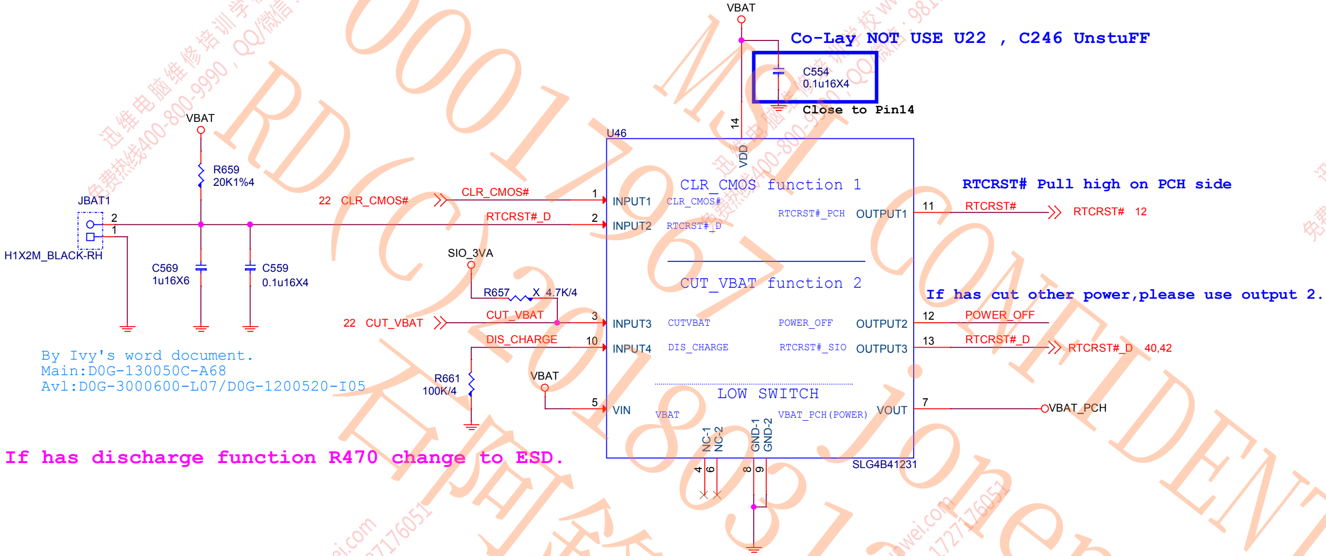
Cut VBAT

20160629





Co-Lay NOT USE U22 , C246 UnstuFF

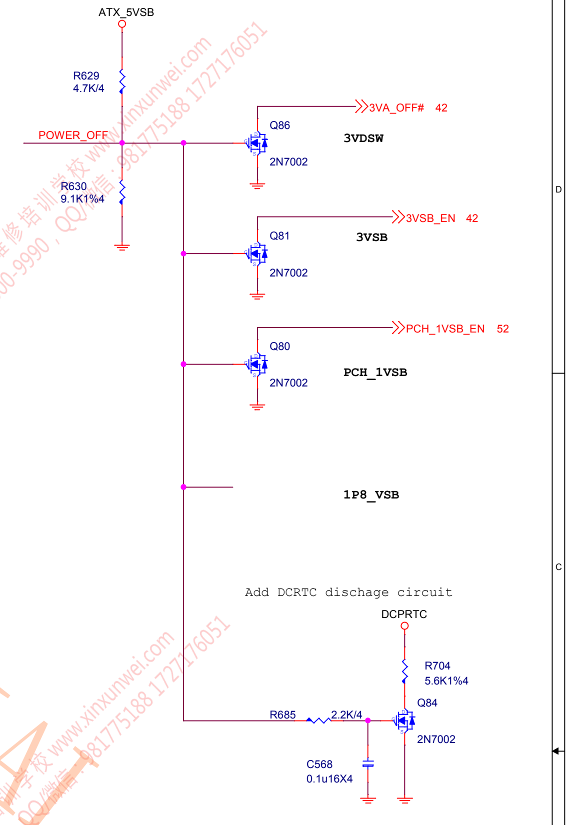
Close to Pin14

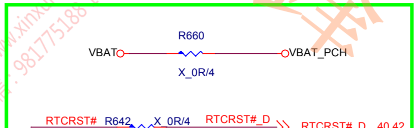
RTCRST# Pull high on PCH side

If has cut other power,please use output 2.

By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05

If has discharge function R470 change to ESD.

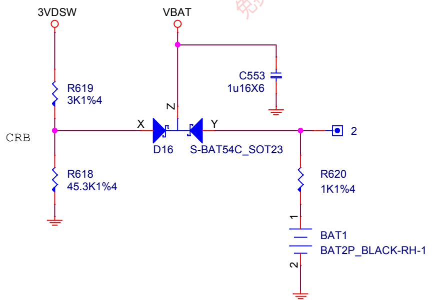




Co-Lay NOT USE U22 , STUFF R223 & R472

If STUFF R223 Please Check RTCRST# Double Pull High

VBAT



Function 1			
IN		OUT	
INPUT1	INPUT2	OUTPUT1	
0	1	1	Default
1	0	0	
1	1	0	
0	0	0	

Function 2					
IN		OUT			
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT	
0	0	0	1	1	Default
1	0	1	1	0 (discharge)	
0	1	1	0	0 (discharge)	
1	1	1	0	0 (discharge)	

MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	CUT VBAT circuit	20

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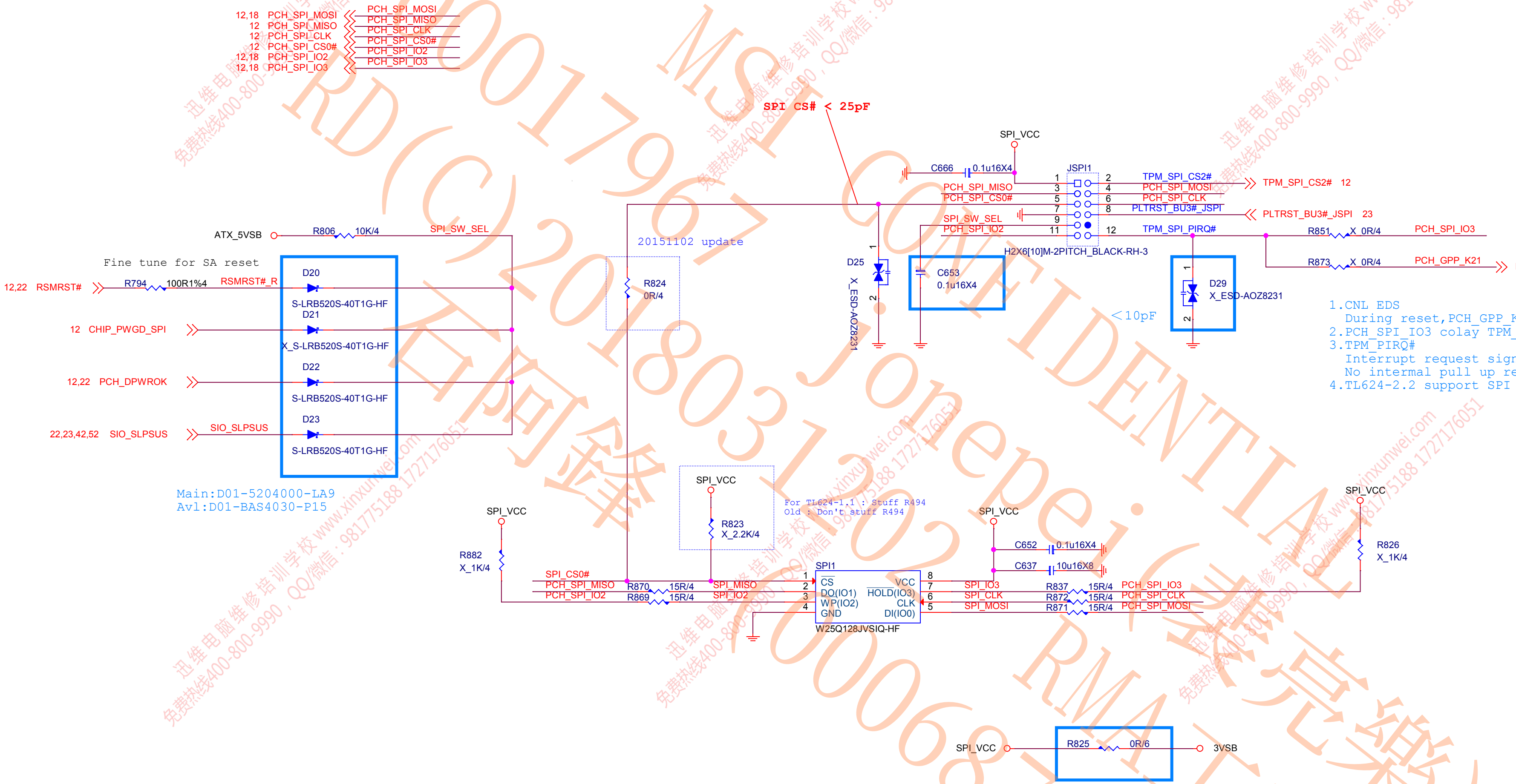

1.CNL EDS
During reset,PCH_GPP_K21 via 20k pull up to 3.3V.
2.PCH_SPI_IO3 colay TPM_PIRQ#(1.8V or 3.3V,OD)
3.TPM_PIRQ#
Interrupt request signal to the host.
No internal pull up resistor.Active low.
4.TL624-2.2 support SPI Standard Mode.

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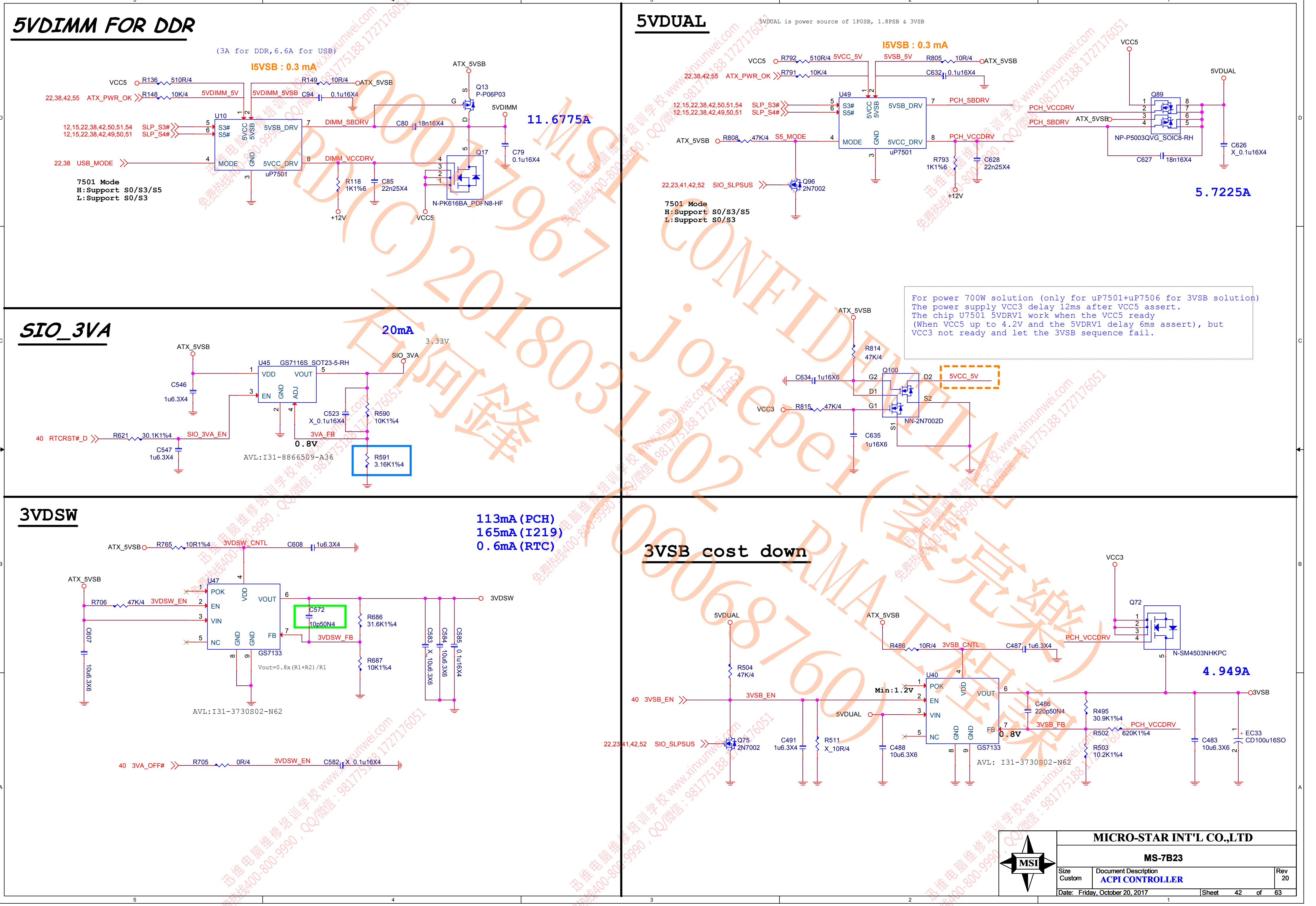
5VDIMM FOR DDR
(3A for DDR,6.6A for USB)
I5VSB : 0.3 mA
ATX_5VSB
VCC5
R136 510R/4
R149 10R/4
22,38,42,55 ATX_PWR_OK
R148 10K/4
5VDIMM_5V
5VDIMM_5VSB
C94 0.1u16X4
Q13 P-P06P03
5VDIMM
11.6775A
U10
12,15,22,38,42,50,51,54 SLP_S3#
12,15,22,38,42,49,50,51 SLP_S4#
S3# S5#
5VCC 5VSB
5VSB_DRV
DIMM_SBDRV
C80 18n16X4
22,38 USB_MODE
MODE
GND
5VCC_DRV
DIMM_VCCDRV
uP7501
Q17
C79 0.1u16X4
R118 1K1%6
C85 22n25X4
+12V
VCC5
N-PK616BA_PDFN8-HF
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
5VDUAL
5VDUAL is power source of 1P05B, 1.8PSB & 3VSB
I5VSB : 0.3 mA
R792 510R/4 5VCC_5V
5VSB_5V
R805 10R/4
R791 10K/4
C632 0.1u16X4
U49
PCH_SBDRV
PCH_VCCDRV
Q89
NP-P5003QVG_SOIC8-RH
C627 18n16X4
C626 X_0.1u16X4
ATX_5VSB
R808 47K/4 S5_MODE
5VCC_DRV
R793 1K1%6
C628 22n25X4
22,23,41,42,52 SIO_SLPSUS
Q96 2N7002
5.7225A
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
R814 47K/4
C634 1u16X6
Q100
5VCC_5V
R815 47K/4
NN-2N7002D
C635 1u16X6
SIO_3VA
20mA
3.33V
U45 GS7116S_SOT23-5-RH
VDD VOUT
EN GND ADJ
C546 1u6.3X4
C523 X_0.1u16X4
R590 10K1%4
3VA_FB
0.8V
40 RTCRST#_D
R621 30.1K1%4
SIO_3VA_EN
C547 1u6.3X4
AVL:I31-8866509-A36
R591 3.16K1%4
3VDSW
113mA(PCH)
165mA(I219)
0.6mA(RTC)
R765 10R1%4 3VDSW_CNTL
C608 1u6.3X4
U47
POK EN VIN NC
VOUT FB
R706 47K/4 3VDSW_EN
C572 10p50N4
R686 31.6K1%4
3VDSW_FB
R687 10K1%4
C583 X_10u6.3X6
C584 10u6.3X6
C585 0.1u16X4
C607 10u6.3X6
GS7133
Vout=0.8x(R1+R2)/R1
AVL:I31-3730S02-N62
40 3VA_OFF#
R705 0R/4
C582 X_0.1u16X4
3VSB cost down
VCC3
Q72
N-SM4503NHKPC
PCH_VCCDRV
R486 10R/4 3VSB_CNTL
C487 1u6.3X4
4.949A
R504 47K/4
40 3VSB_EN
Min:1.2V
U40
C486 220p50N4
R495 30.9K1%4
3VSB
3VSB_FB
R502 620K1%4
0.8V
Q75 2N7002
C491 1u6.3X4
R511 X_10R/4
C488 10u6.3X6
R503 10.2K1%4
C483 10u6.3X6
EC33 CD100u16SO
AVL: I31-3730S02-N62
MICRO-STAR INT'L CO.,LTD
MSI
MS-7B23
Size Custom
Document Description
ACPI CONTROLLER
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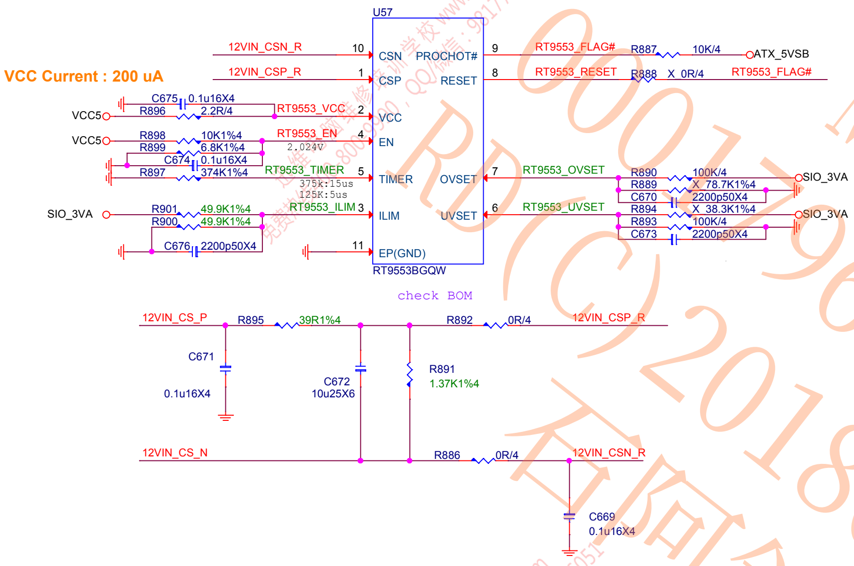
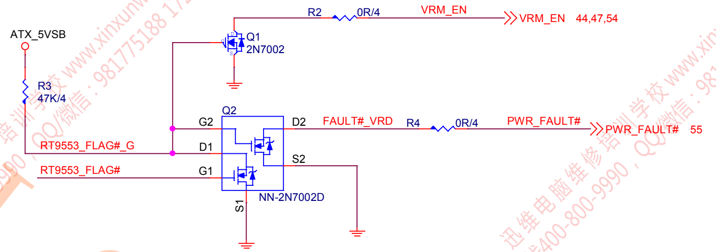
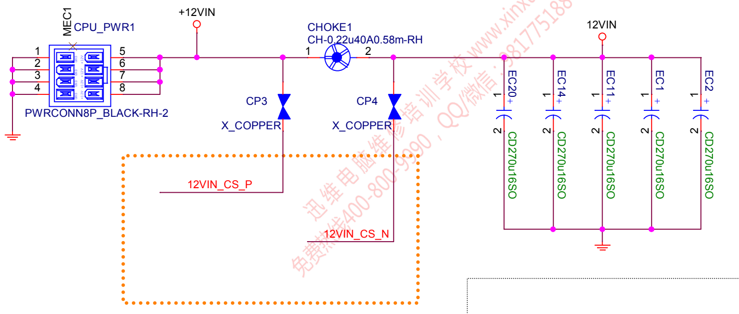
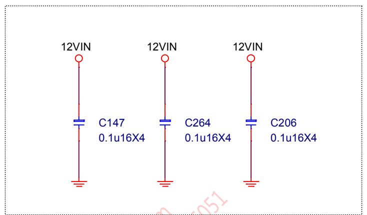




OCP:30A
Real OCP:30.05A
R17+R18>100k Vsio_3va= 3.38V Rdcr= 0.5 mohm

I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100
I3933_imon= 10uA/step
Istep=4.968A





D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	138	> Vcore current
I avg.	=	110.4	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	4	phase
I ripple	=	9.179738	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	45	> Vcore current
I avg.	=	36	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	5.986785	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	0.95	> output Vcore
D	=	0.079167	

I o = Icore(max)*0.8			
I core(max)	=	6.4	> Vcore current
I avg.	=	5.12	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	1.382393	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	1	pcs.

```
CORE:
D = Vout/Vin
  = 1.52/12
  = 0.126667
N = 4
Irms = Iout * [D/N - (D)^2]^(1/2)
     = 138* (0.031667 - 0.016044)^(1/2)
     = 17.2489A
```

```
GT:
D = Vout/Vin
  = 1.52/12
  = 0.126667
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
     = 45* (0.063333 - 0.016044)^(1/2)
     = 9.7857A
```

```
VCCIO:
D = Vout/Vin
  = 0.95/12
  = 0.079167
N = 1
Irms = Iout * [D/N - (D)^2]^(1/2)
     = 6.4* (0.079167 - 0.006267)^(1/2)
     = 1.728A
```

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Size: Custom	Document Description: 12VIN/CURRENT SENSE-RT9553	Rev: 20
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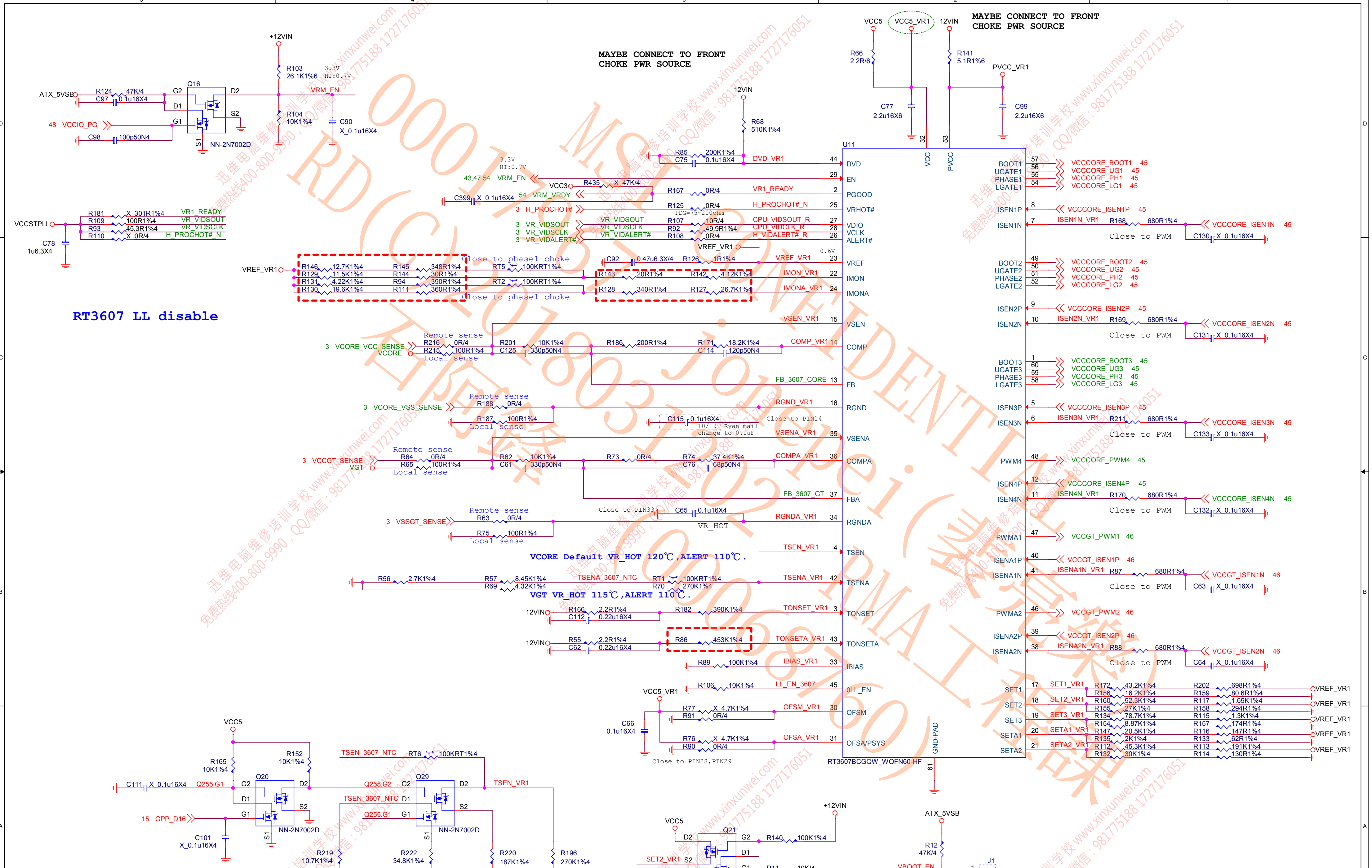

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MS-7B23

Size	Document Description	Rev
Custom	PWM-RT3607BC	20

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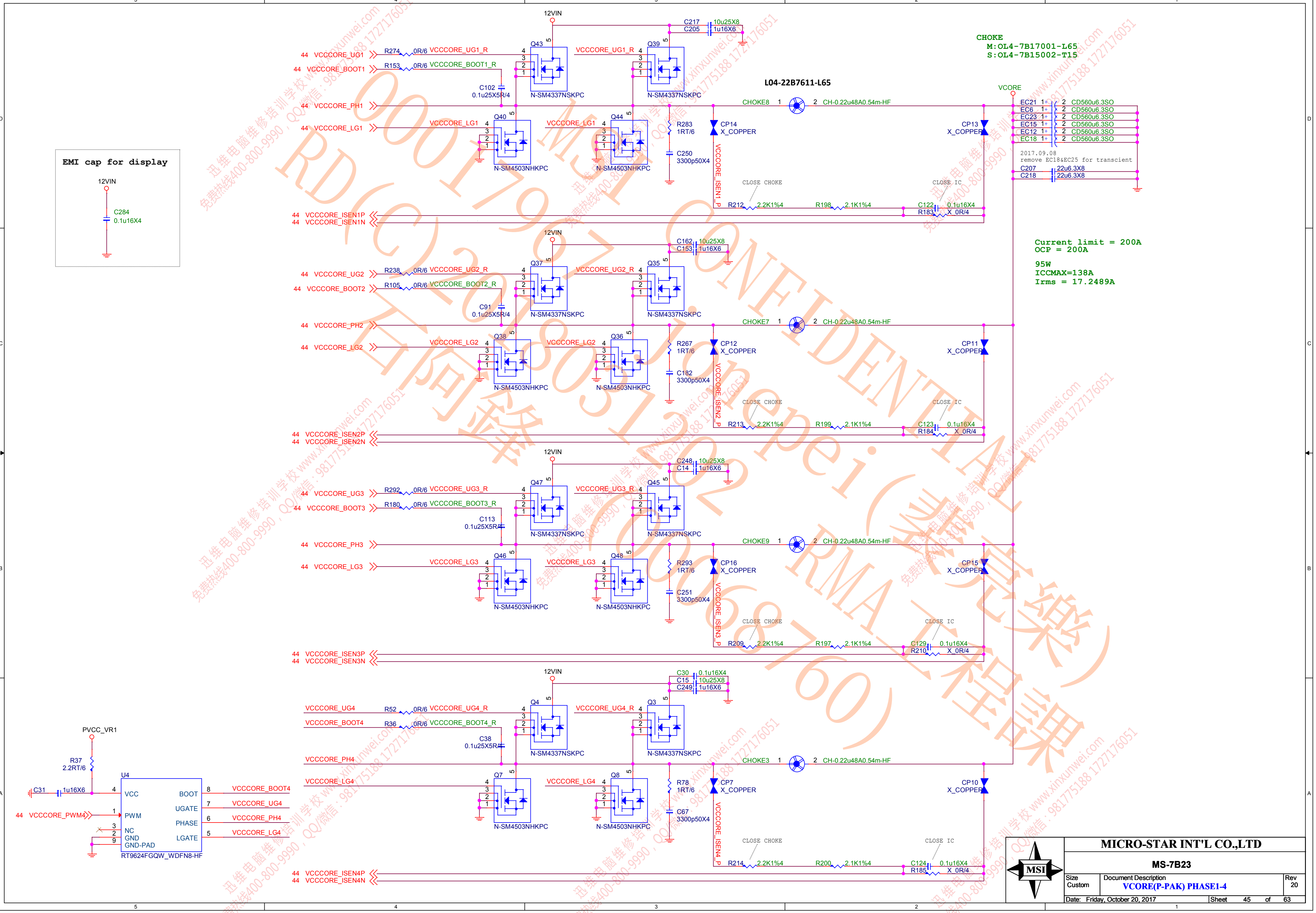

CHOKE
M:OL4-7B17001-L65
S:OL4-7B15002-T15
L04-22B7611-L65
VCORE
EMI cap for display
12VIN
C284
0.1u16X4
2017.09.08
remove EC18&EC25 for transcient
Current limit = 200A
OCP = 200A
95W
ICCMAX=138A
Irms = 17.2489A
CHOKE8
CHOKE7
CHOKE9
CHOKE3
CH-0.22u48A0.54m-HF
N-SM4337NSKPC
N-SM4503NHKPC
X_COPPER
CLOSE CHOKE
CLOSE IC
VCCCORE_UG1
VCCCORE_BOOT1
VCCCORE_PH1
VCCCORE_LG1
VCCCORE_ISEN1P
VCCCORE_ISEN1N
VCCCORE_UG2
VCCCORE_BOOT2
VCCCORE_PH2
VCCCORE_LG2
VCCCORE_ISEN2P
VCCCORE_ISEN2N
VCCCORE_UG3
VCCCORE_BOOT3
VCCCORE_PH3
VCCCORE_LG3
VCCCORE_ISEN3P
VCCCORE_ISEN3N
VCCCORE_UG4
VCCCORE_BOOT4
VCCCORE_PH4
VCCCORE_LG4
VCCCORE_ISEN4P
VCCCORE_ISEN4N
PVCC_VR1
R37
2.2RT/6
C31
1u16X6
U4
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624FGQW_WDFN8-HF
VCCCORE_PWM4
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size
Custom
Document Description
VCORE(P-PAK) PHASE1-4
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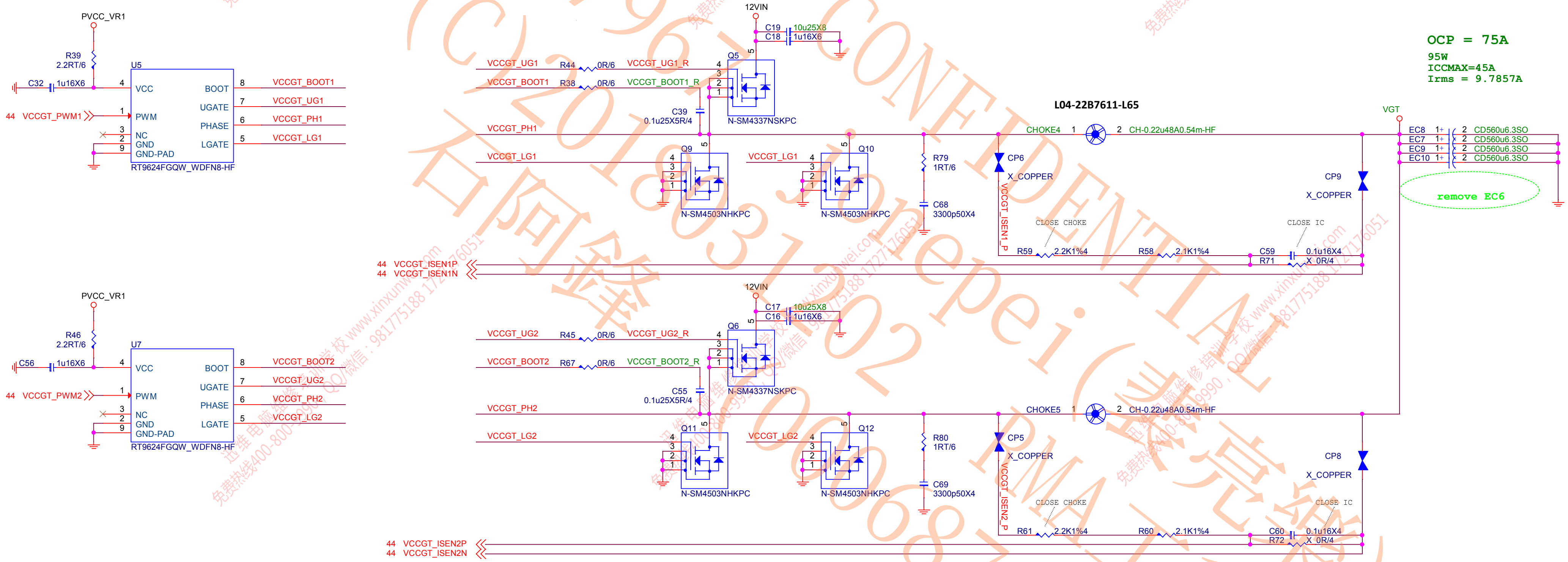

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Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 20
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SA Power:1.05V,11.1A

OCP:16.65A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 16.65* 3mohm / 10uA
= 14.28K

Rdson(low)10V

MOS : 5.1mohm

ICC : 1.25 mA

EN:VIH2.4V
EN pin Maximum:6.5V

FB:0.8V

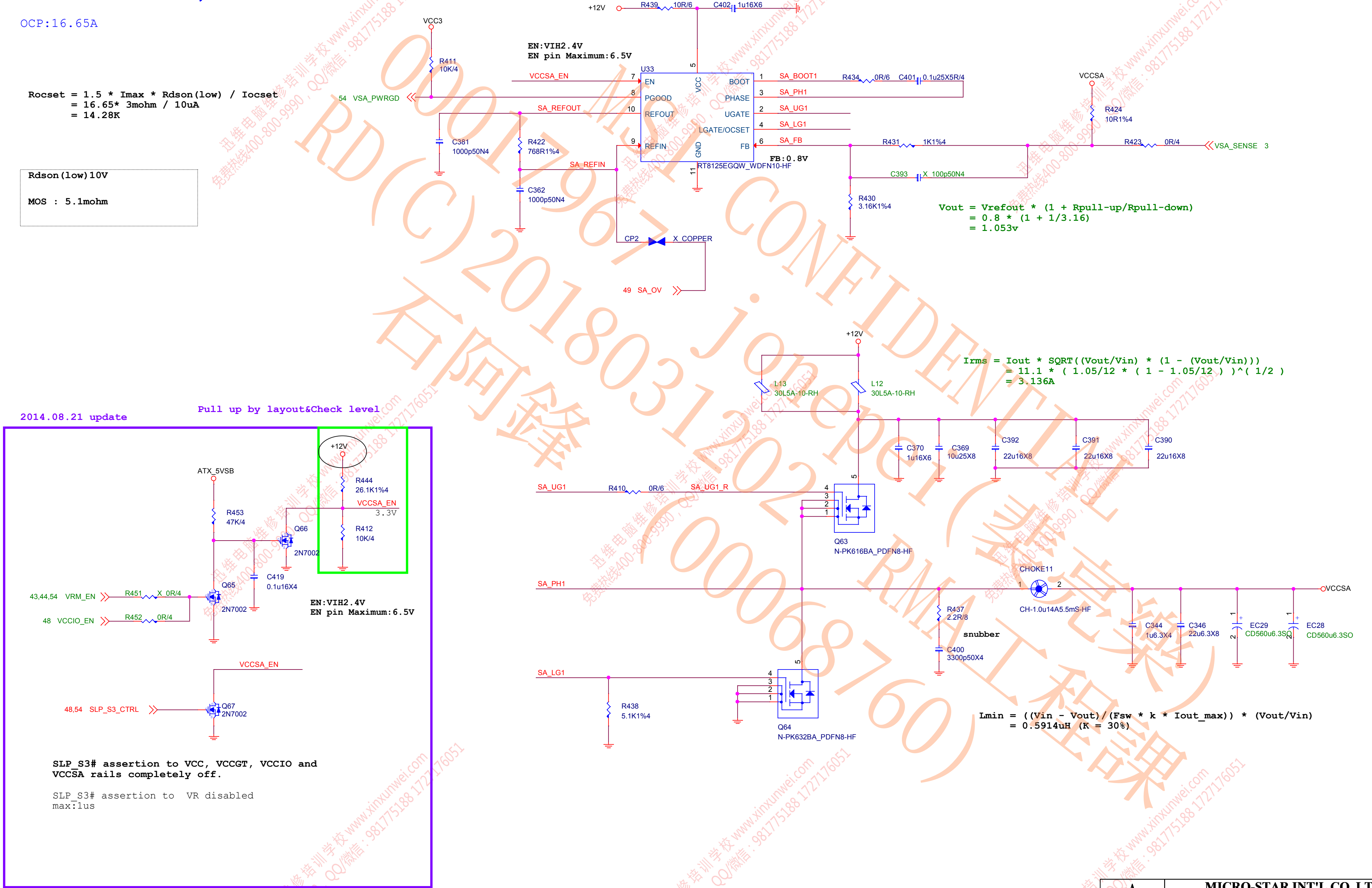
Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/3.16)
= 1.053v

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1 * (1.05/12 * (1 - 1.05/12))^(1/2)
= 3.136A

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

2014.08.21 update

Pull up by layout&Check level



EN:VIH2.4V
EN pin Maximum:6.5V

SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

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Size: Custom	Document Description: VCCSA - POWER RT8125E	Rev: 20
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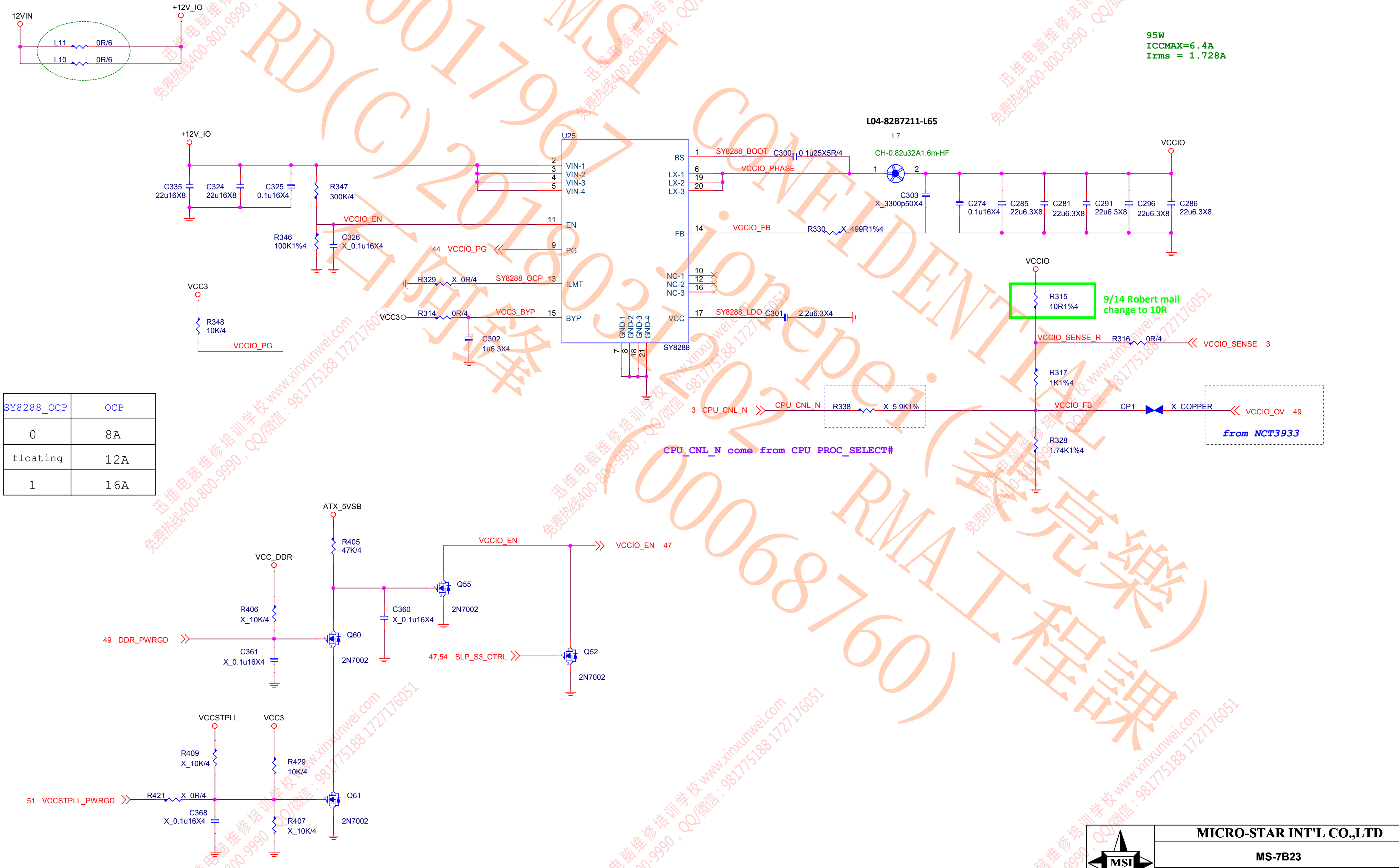
IO Power:0.95V,6.4A

IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

95W
ICCMAX=6.4A
Irms = 1.728A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

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Size: Custom	Document Description: VCCIO - SY8288	Rev: 20
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DDR4 Power:1.2V,19.8A *OCP:28A*

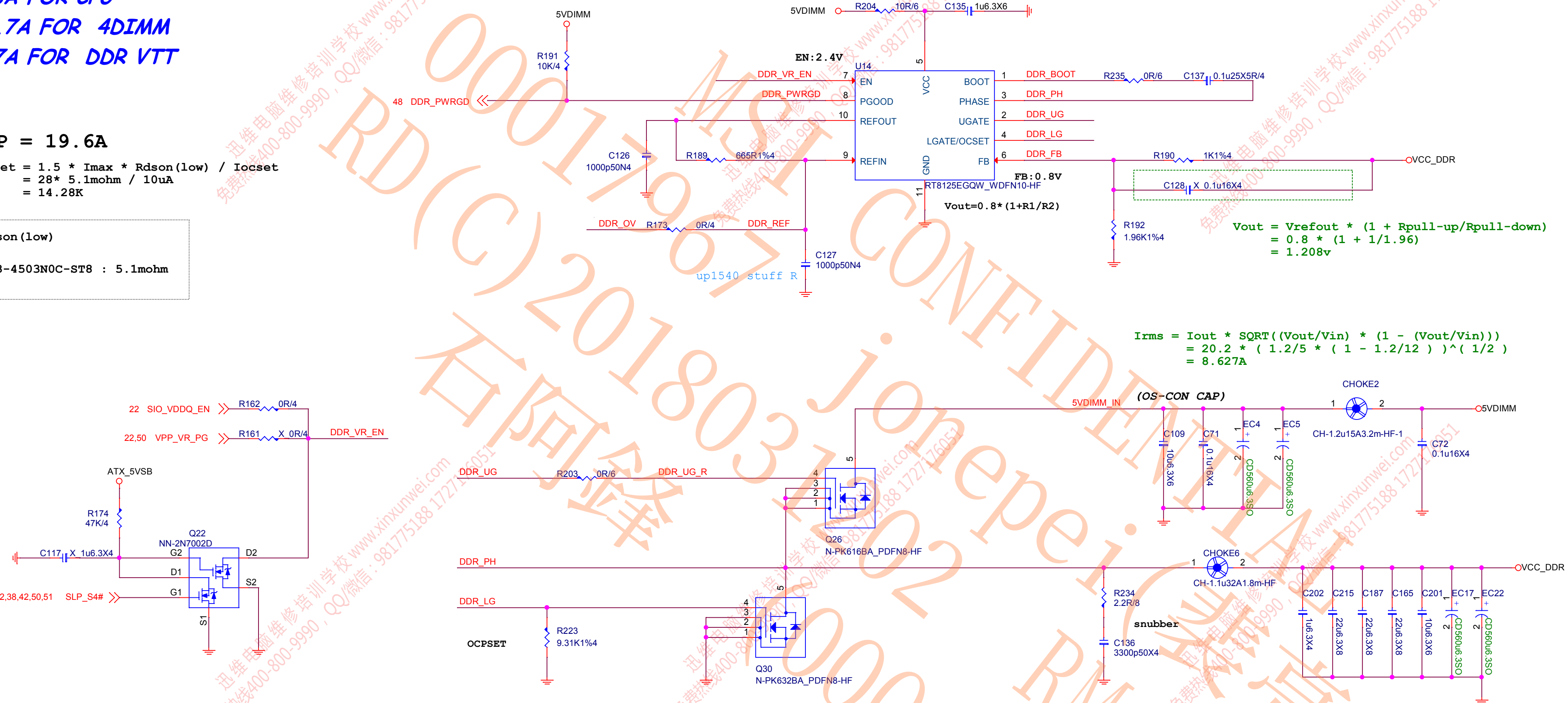
3.3A FOR CPU
15.7A FOR 4DIMM
0.7A FOR DDR VTT

OCP = 19.6A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 28* 5.1mohm / 10uA
= 14.28K

Rdson(low)

D03-4503N0C-ST8 : 5.1mohm



Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/1.96)
= 1.208v

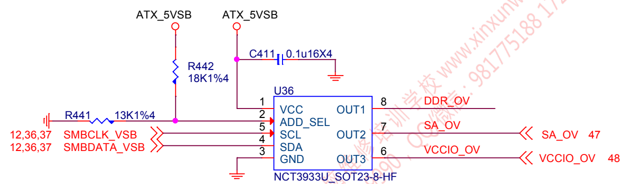
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 20.2 * (1.2/5 * (1 - 1.2/12))^(1/2)
= 8.627A

Datasheet公式計算
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH<L<1.2897uH

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



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Size: Custom	Document Description: DDR - RT8125E	Rev: 20
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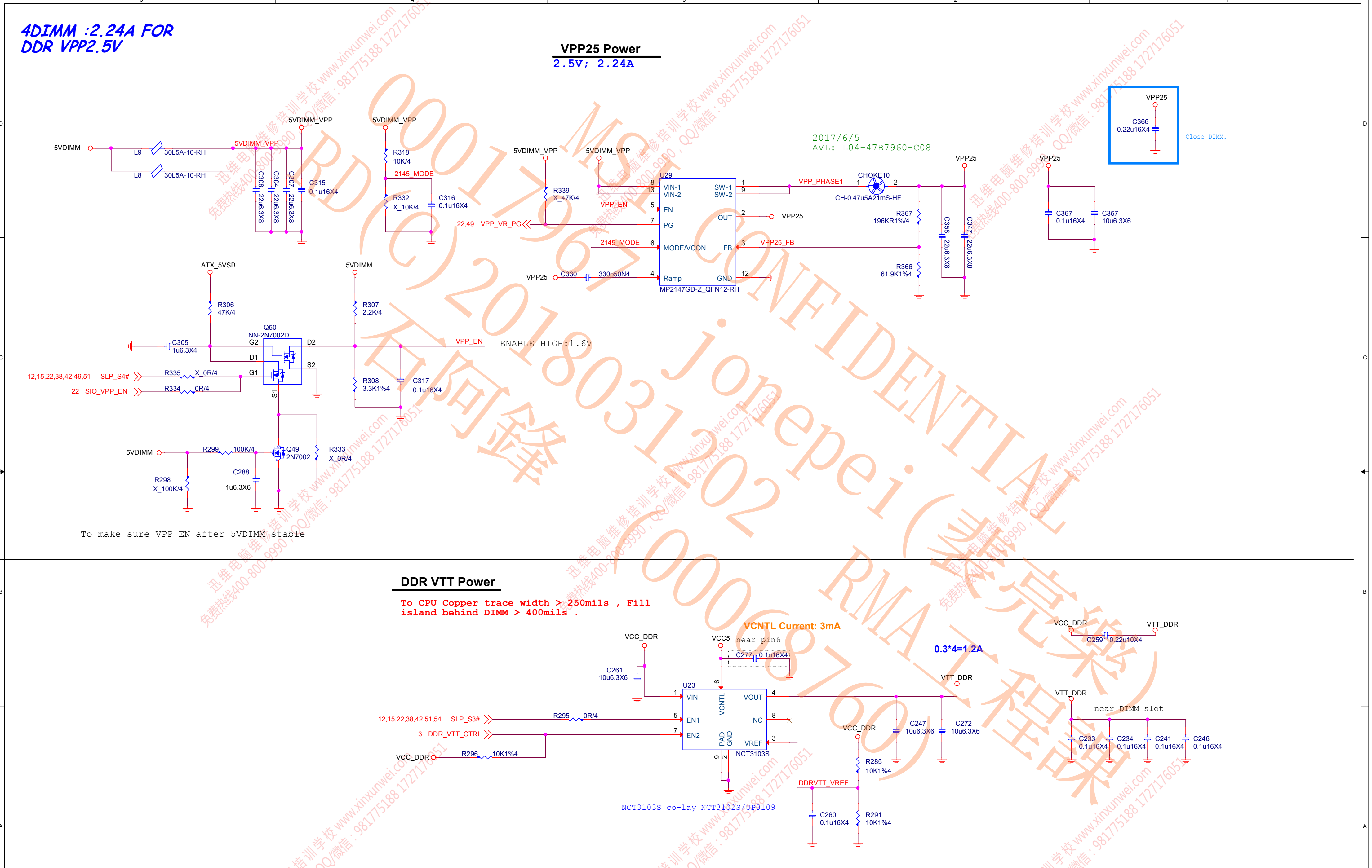

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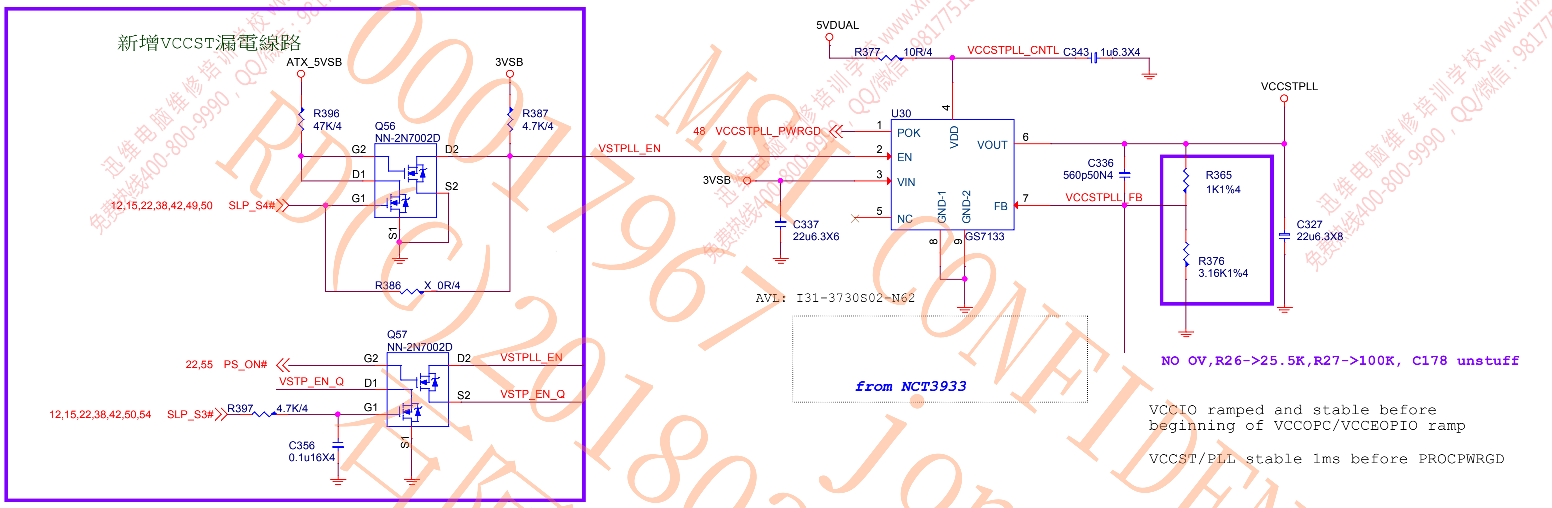
VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge



NO OV,R26->25.5K,R27->100K, C178 unstuff

VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

1.2V; 130mA

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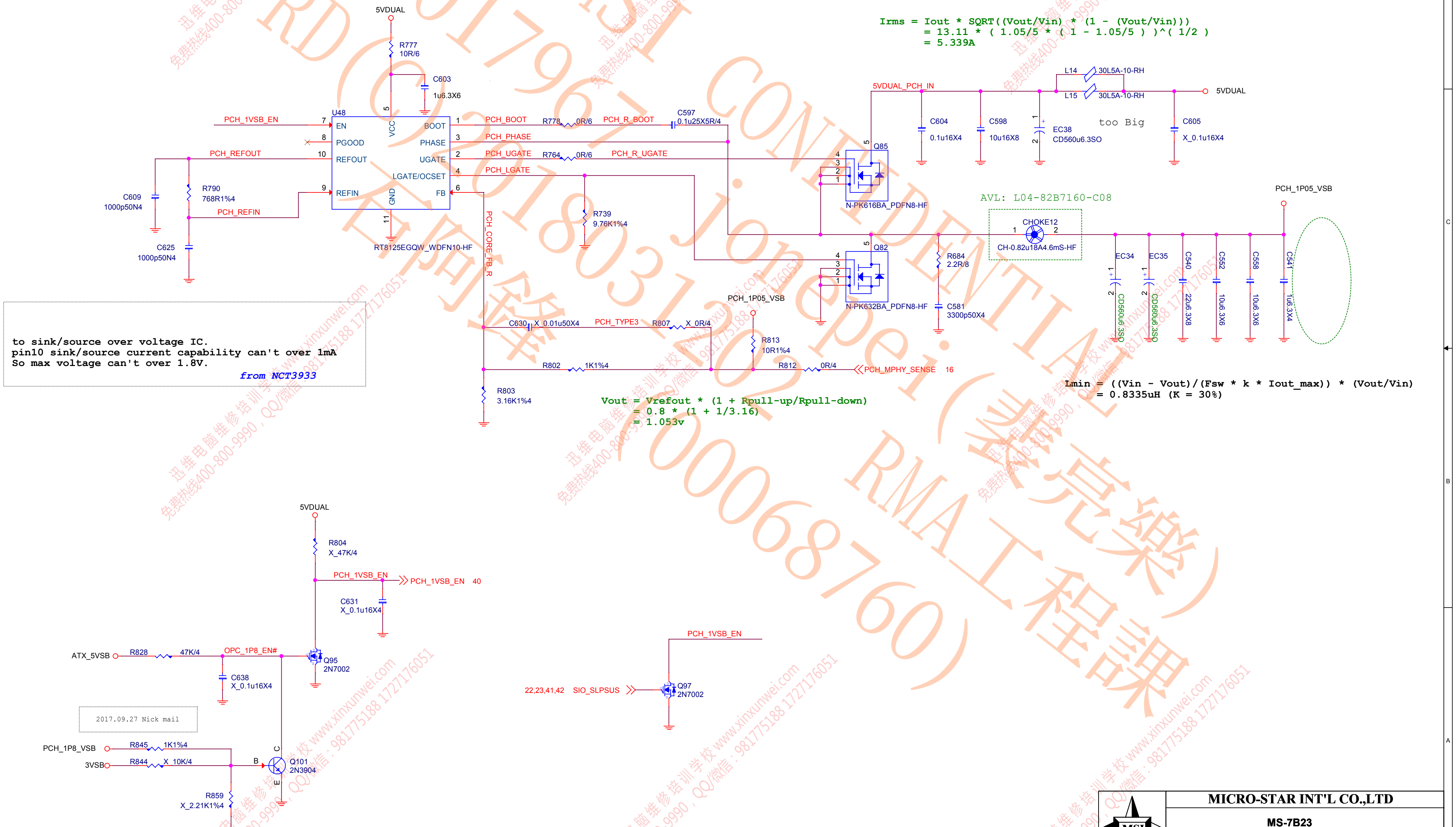
PCH_1VSB

1.05V; 13.11A

OCP=Rocset x Iocset / Rlgds(on)
=9.76K x 10u / 4.6m
= 21.21A

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.11 * (1.05/5 * (1 - 1.05/5))^(1/2)
= 5.339A



to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/3.16)
= 1.053v

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

2017.09.27 Nick mail

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1P8_VSB

1.8V; 589mA

MAX:589mA

Table 10-8. CNP-H VCCPRIM_1P8 Adder with and without CNVi

Details	Icc (DT) (mA)
Without CNVi	0
With CNVi	589

AVL:I31-8866509-A36

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Custom	PCH 1P8V	20

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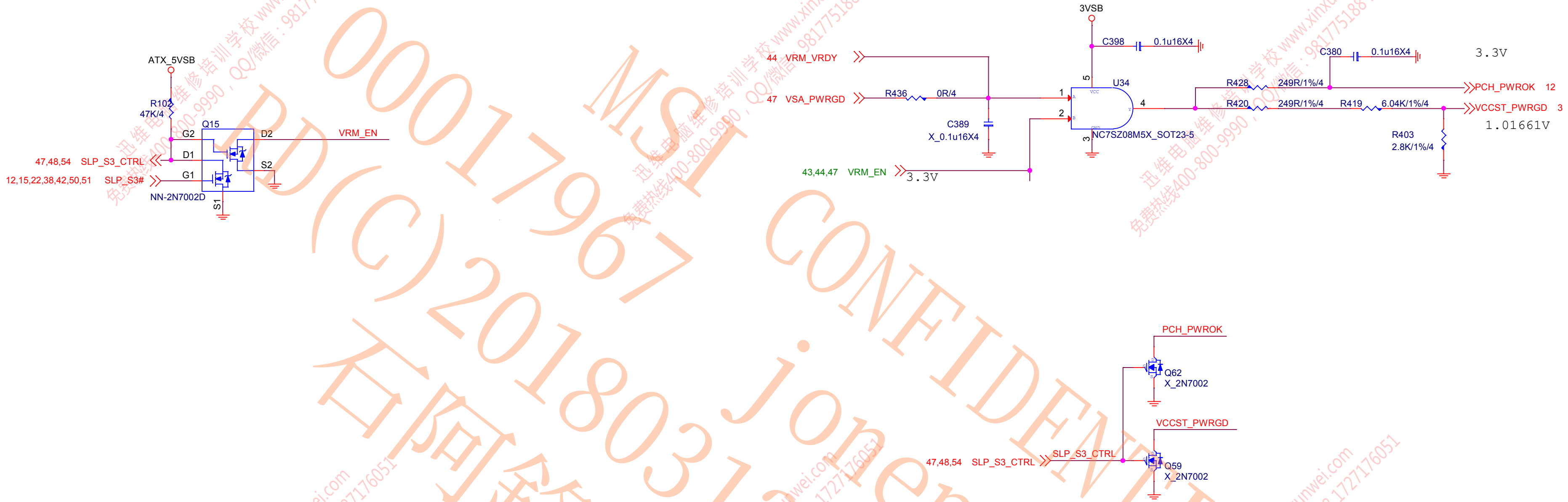
Sequence



MICRO-STAR INT'L CO.,LTD

MS-7B17

Size	Document Description	Rev
Custom	CPU PWR-VRM-Seqence	20

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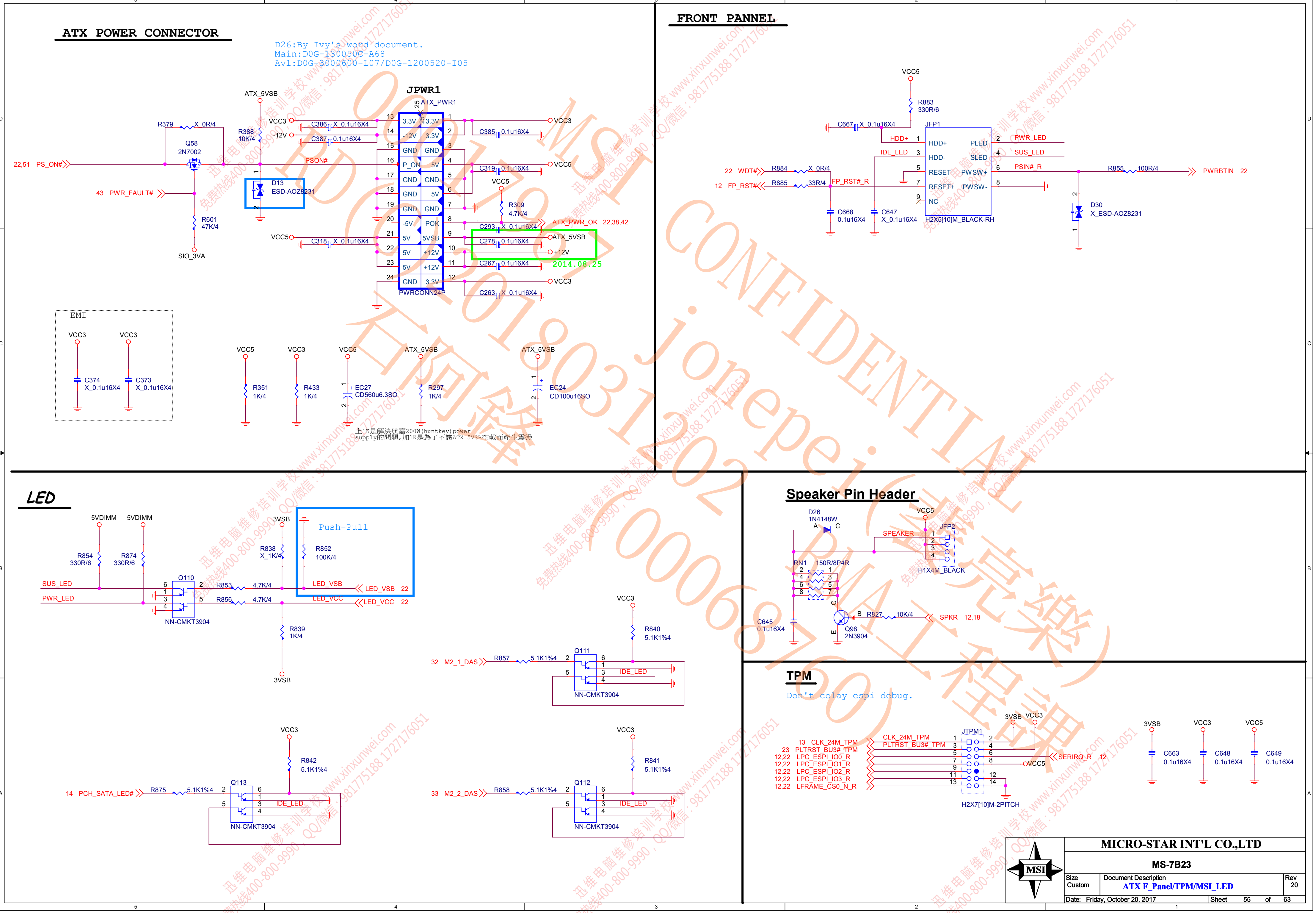

ATX POWER CONNECTOR
D26:By Ivy's word document.
Main:D0G-130050C-A68
Avl:D0G-3000600-L07/D0G-1200520-I05
JPWR1
ATX_PWR1
PWRCONN24P
EMI
上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪
FRONT PANNEL
JFP1
H2X5[10]M_BLACK-RH
LED
Push-Pull
Speaker Pin Header
JFP2
H1X4M_BLACK
TPM
Don't colay espi debug.
JTPM1
H2X7[10]M-2PITCH
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size Custom
Document Description
ATX F_Panel/TPM/MSI_LED
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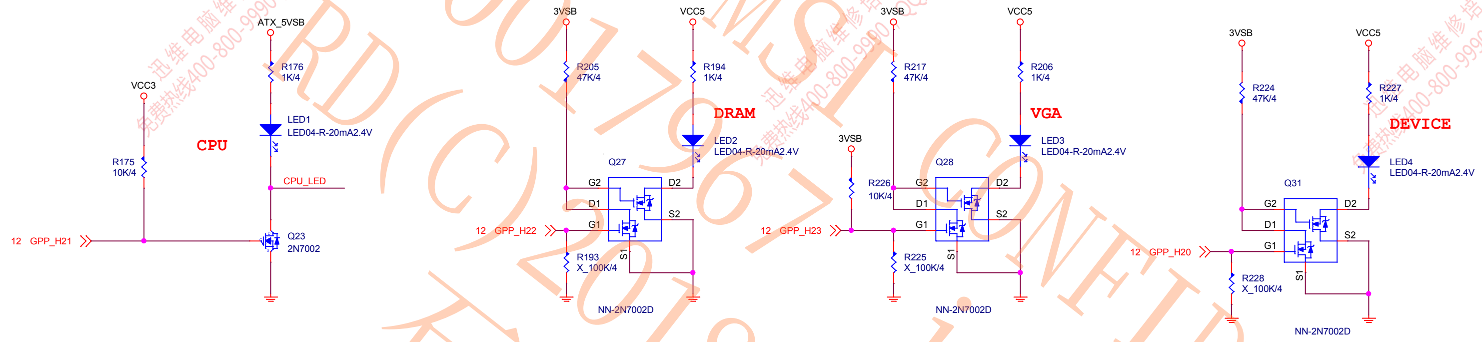
DEBUG LED



GPIO / LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

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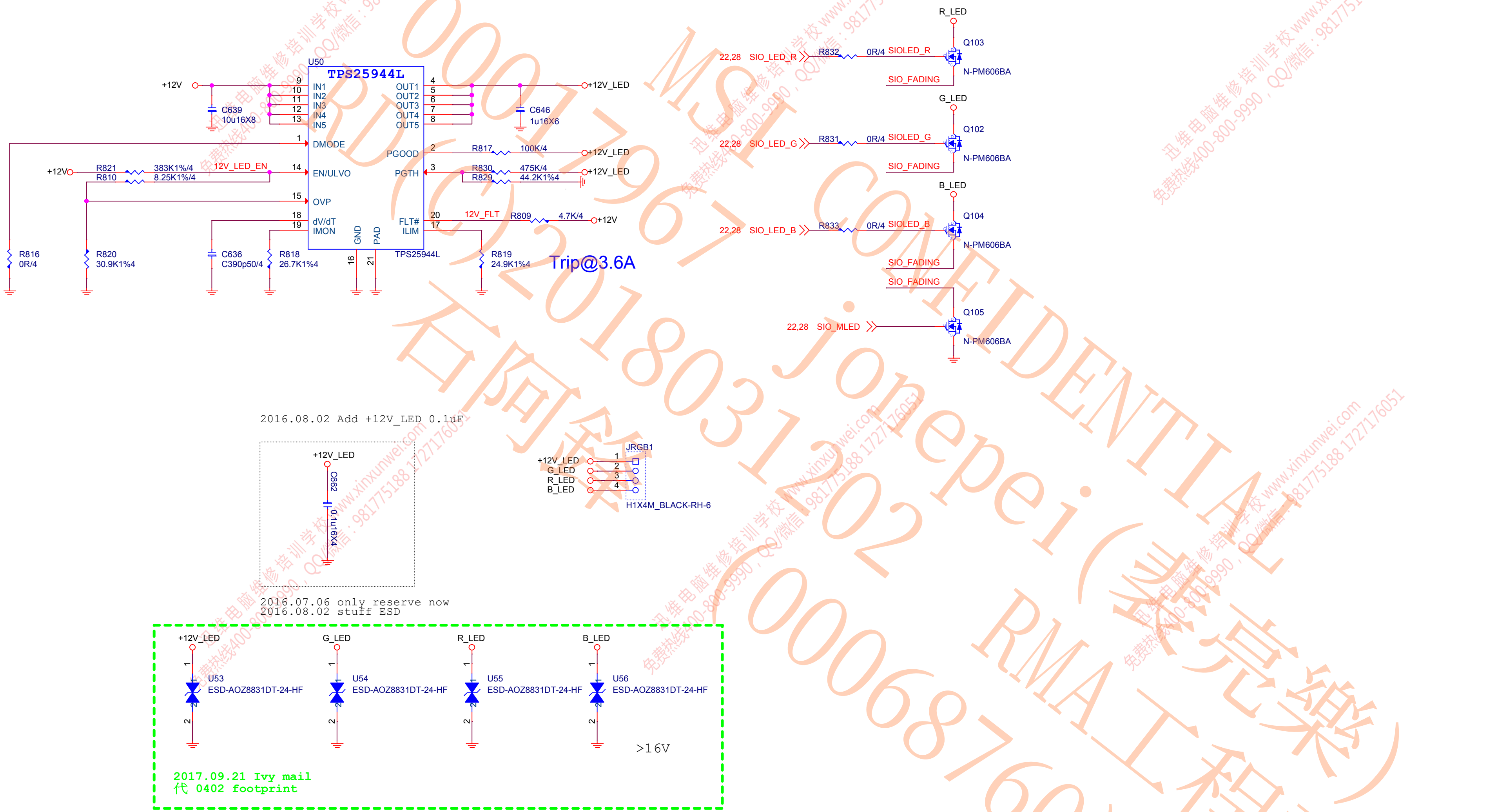
LED STRIPLINE



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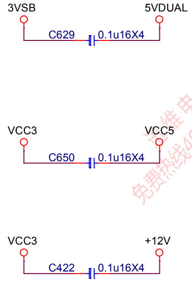
EMI CAP

2017.10.13 moat cap



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Size Custom	Document Description EMI	Rev 20
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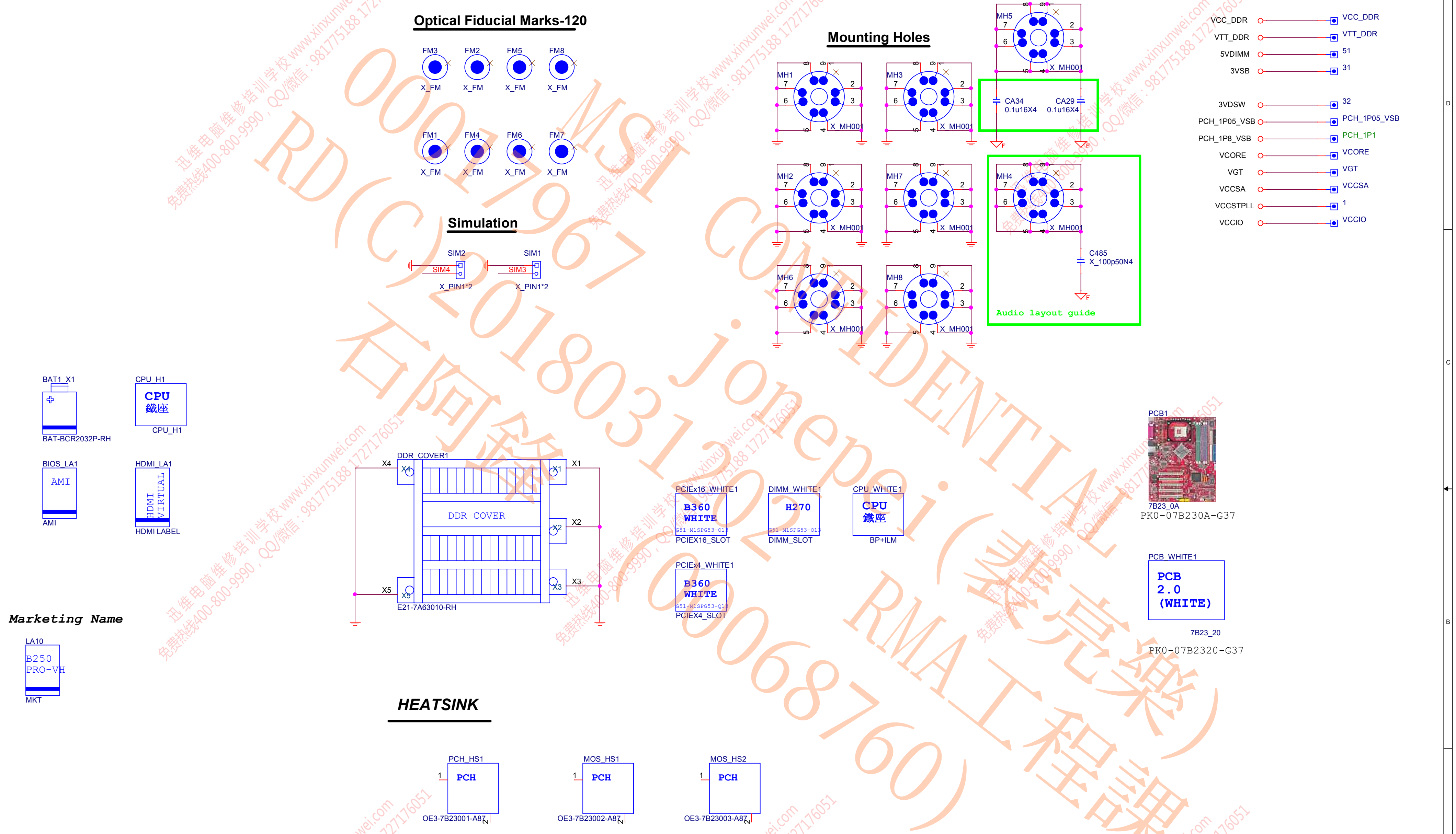

MICRO-STAR INT'L CO.,LTD		
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