MS-7D22

mATX
Ver: 10

RKL Platform

CPU:

Rocket lake S 65W

System Chipset:

H510 PCH_V

Onboard Chip:

HD Audio Codec : ALC897
LAN : INTEL I219
SIO : NTC6687
Flash ROM: SPI 256 MB X1

VGA Output:

HDMI Port
DVI Port
VGA Port

Main Memory:

*DDRIV (2666MHz) * 2*

PWM:

IMVP8 -RT3607

ACPI:

LDO

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 1*
*M.2 Slot * 1*
*Intel WIFI * 1*

Other:

*SATA3.0 *4*
*PS2 * 1*
*REAL USB3.1 *2*
REAL USB2.0 LAN_USB
*FRONT USB3.1 *2*
*FRONT USB2.0 *4*

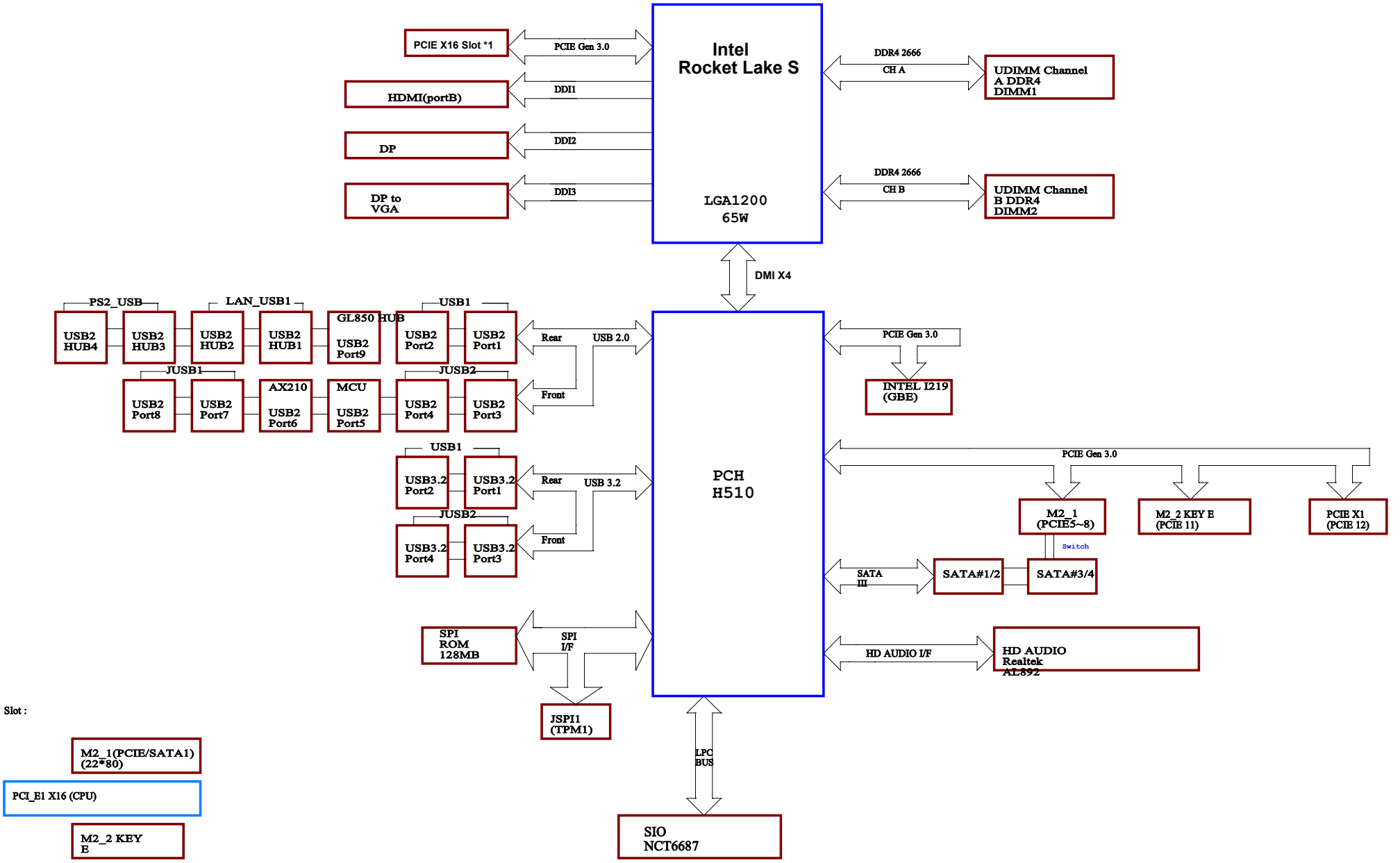
MICRO-STAR INT'L CO.,LTD

MS-7D22

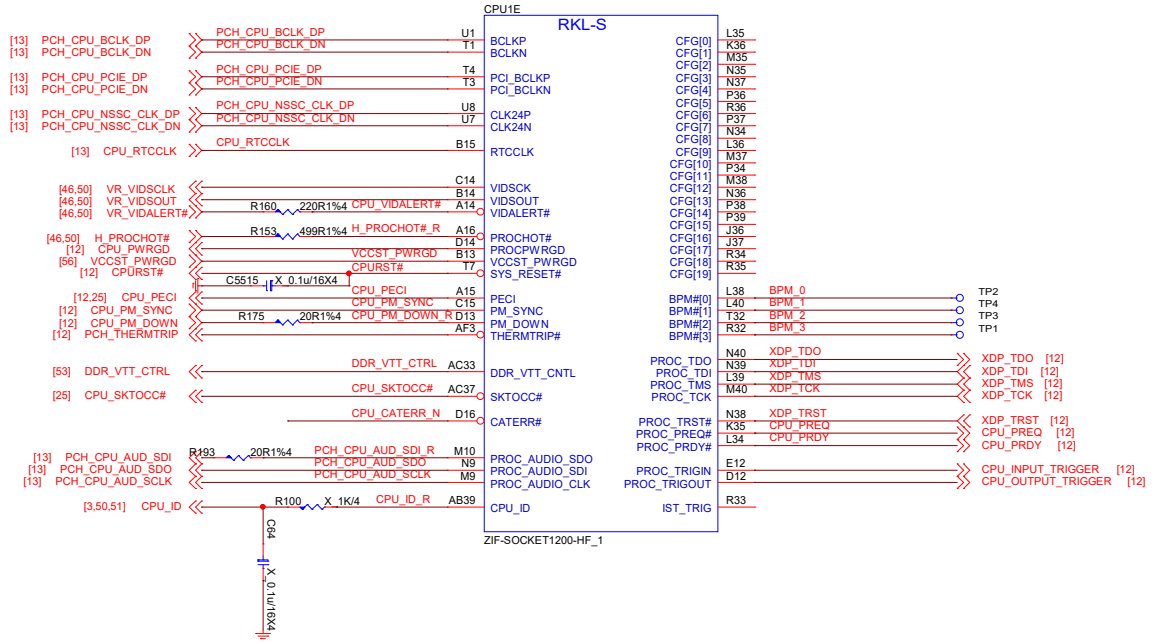
Size	Document Description	Rev
Custom	Cover Sheet	10

Date: Friday, December 18, 2020 Sheet 1 of 67

MS-7D22 Block Diagram



MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: Block Diagram
Rev: 10	
Date: Friday, December 18, 2020	Sheet 2 of 67



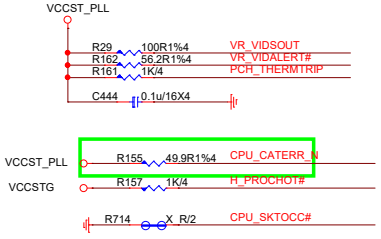
JTAG

PLACE R WITHIN 1.5" OF CPU

XDP_TCK R152 51R/4

PLACE R WITHIN 1.1" OF CPU PDG座

XDP_TRST R360 X_51R/4



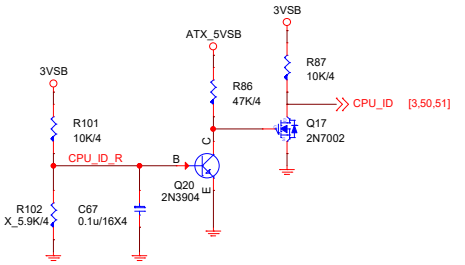
CFG Strap

CFG Table

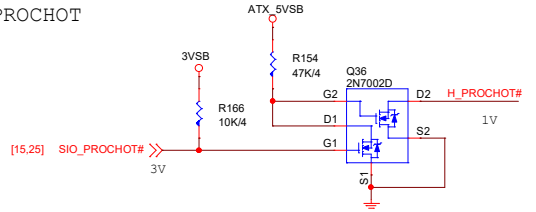
	HIGH	LOW	DESCRIPTION
0	No stall	Stall	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

CFG5 ENABLE#	CFG6	SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

CPU_ID



PROCHOT

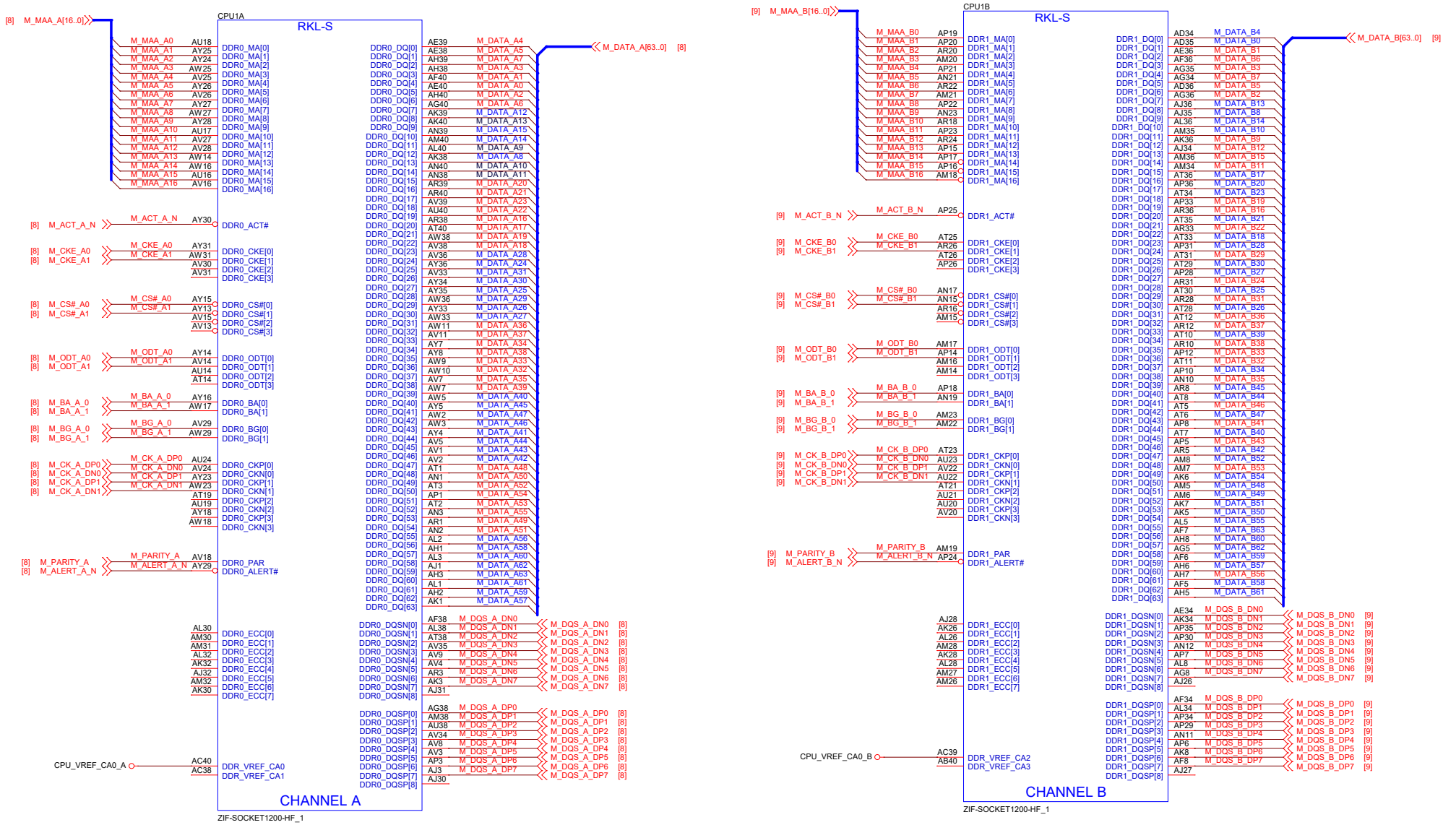


MICRO-STAR INT'L CO.,LTD

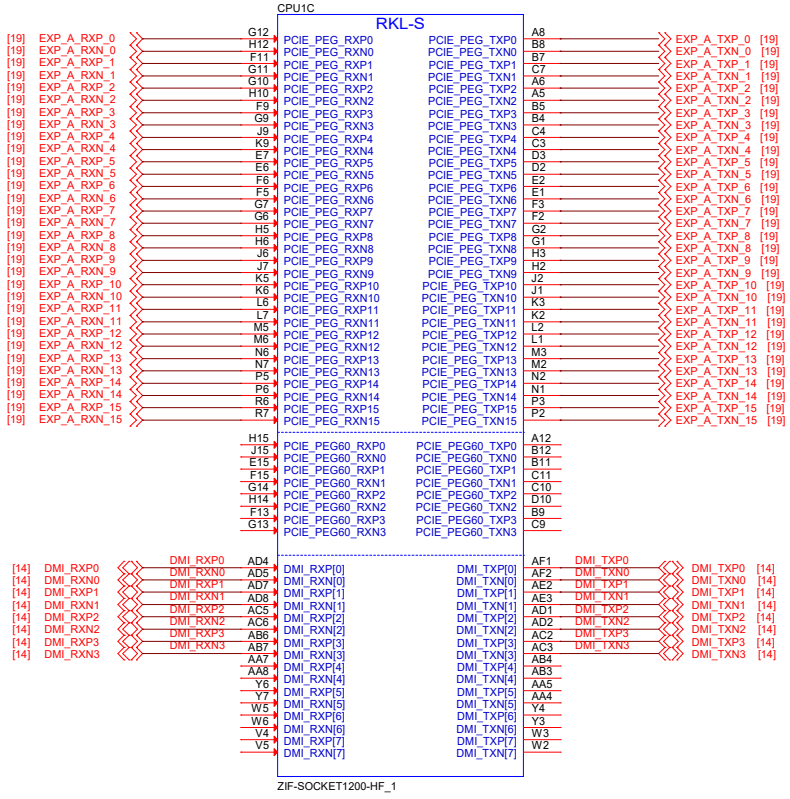
MS-7D22

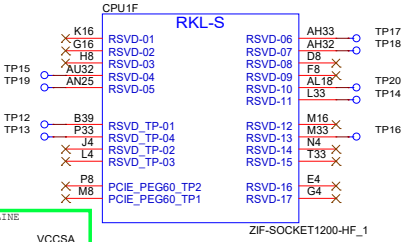
Size	Document Description	Rev
Custom	CPU-Control/MISC/CFG	10

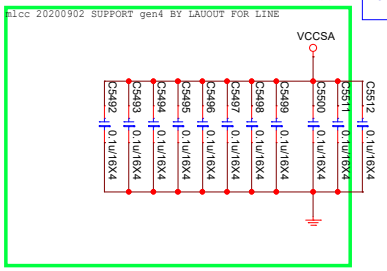
Date: Friday, December 18, 2020 Sheet 3 of 67



MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: CPU-Memory
Rev: 10	
Date: Friday, December 18, 2020	Sheet 4 of 67





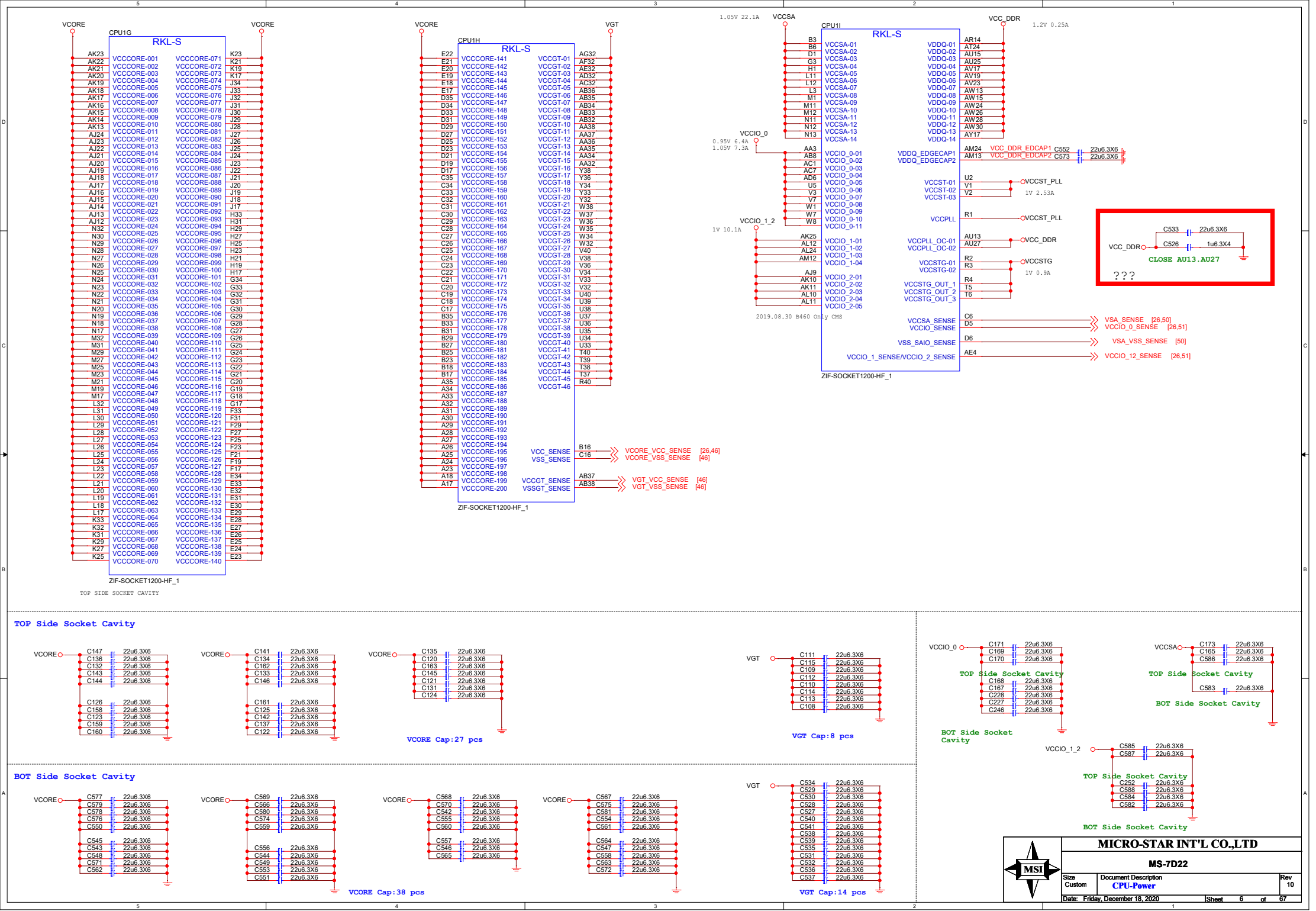


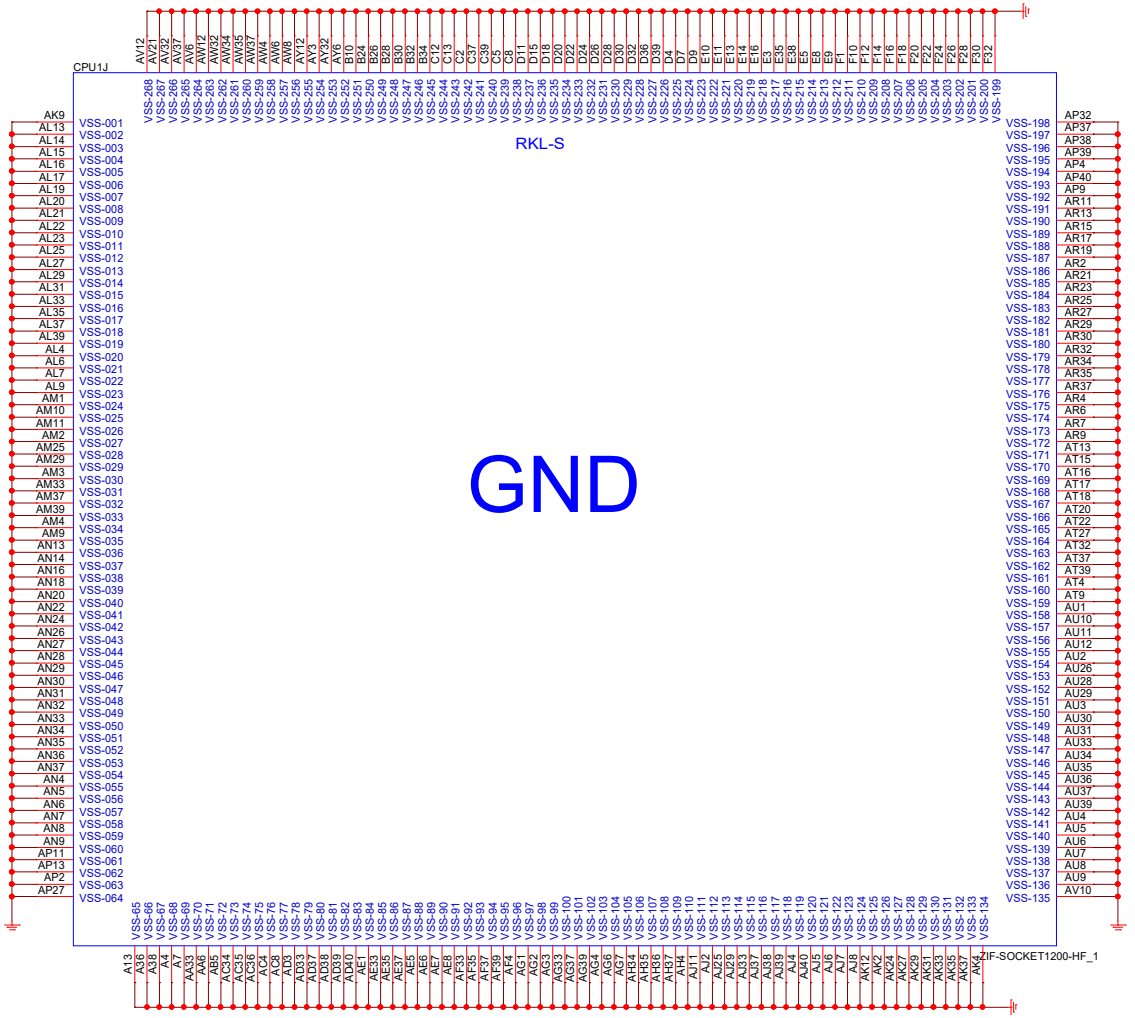
HDMI

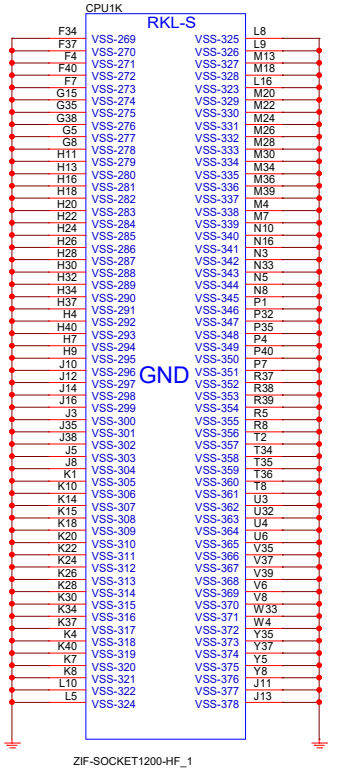
DP

DP to VGA

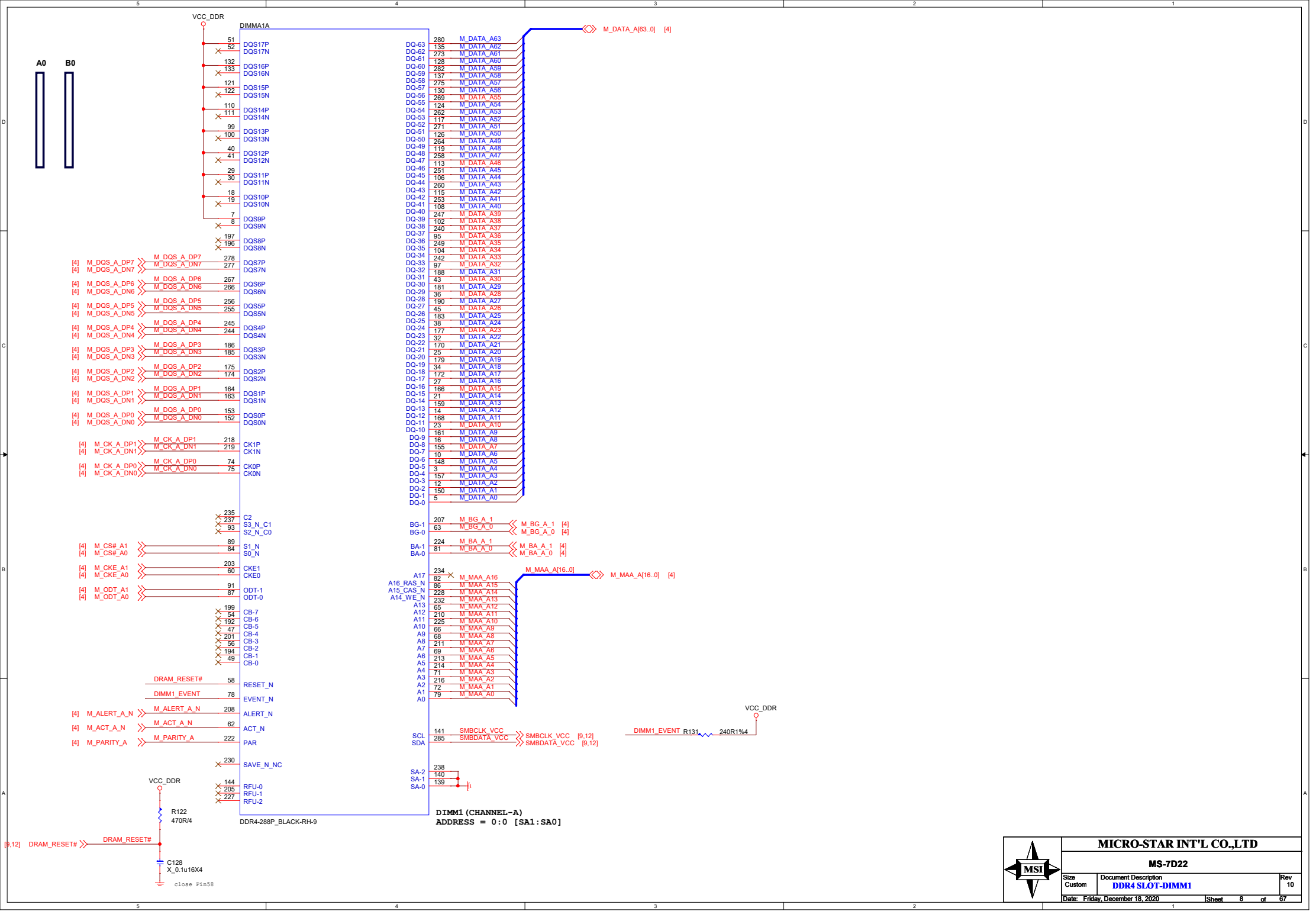
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: CPU-PEG/Display/RSD	Rev: 10
Date: Friday, December 18, 2020	Sheet 5 of 67	

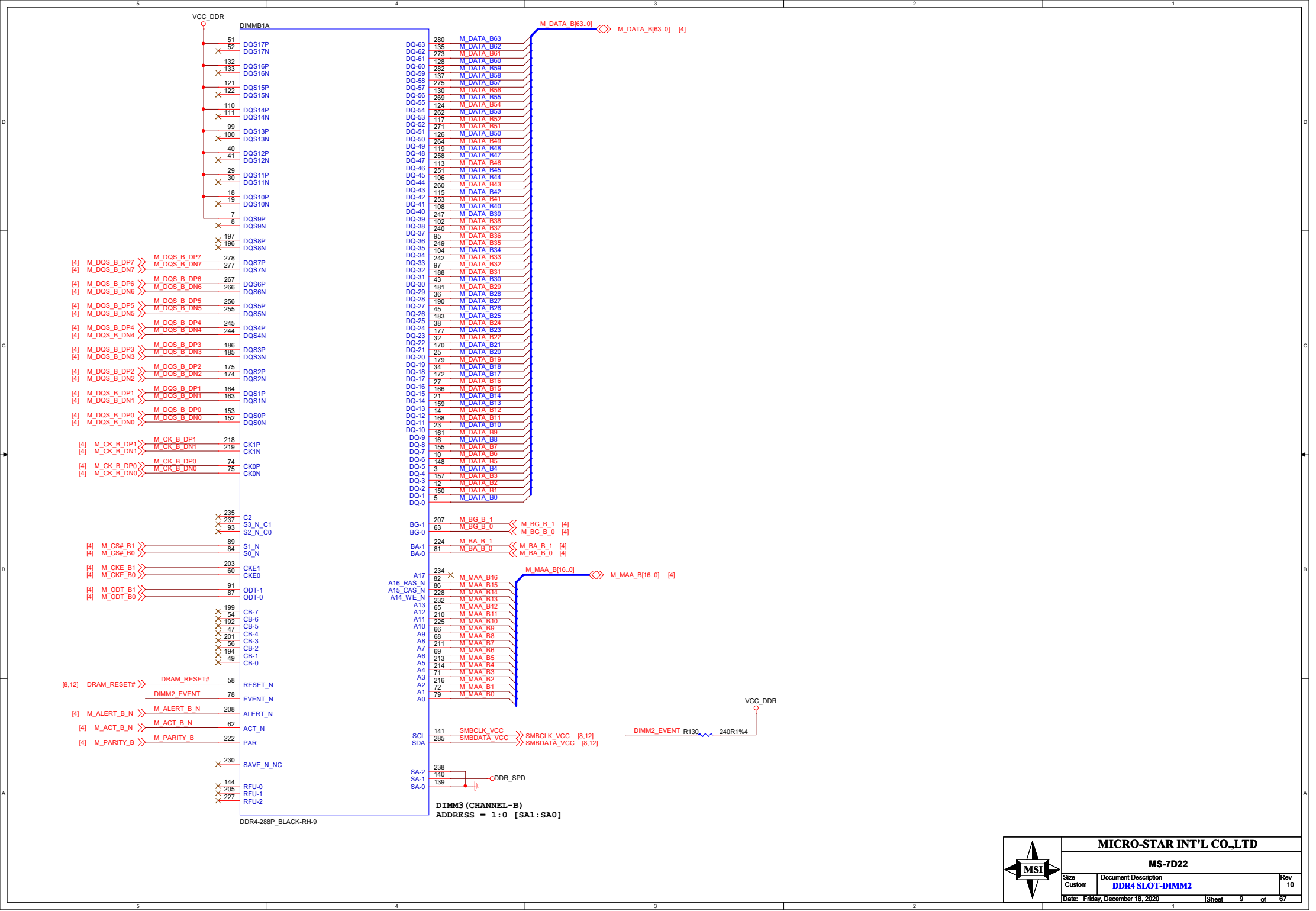

CPU1G
RKL-S
VCORE
ZIF-SOCKET1200-HF_1
TOP SIDE SOCKET CAVITY
CPU1H
VCC_SENSE
VSS_SENSE
VCCGT_SENSE
VSSGT_SENSE
VCORE_VCC_SENSE [26,46]
VCORE_VSS_SENSE [46]
VGT_VCC_SENSE [46]
VGT_VSS_SENSE [46]
CPU1I
VCCSA
VCC_DDR
1.05V 22.1A
1.2V 0.25A
VCCIO_0
VCCIO_1_2
VCCST_PLL
VCCPLL
VCC_DDR
VCCSTG
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VCCIO_1_SENSE/VCCIO_2_SENSE
VSA_SENSE [26,50]
VCCIO_0_SENSE [26,51]
VSA_VSS_SENSE [50]
VCCIO_12_SENSE [26,51]
2019.08.30 B460 Only CMS
CLOSE AU13.AU27
???
TOP Side Socket Cavity
VCORE Cap:27 pcs
VGT Cap:8 pcs
BOT Side Socket Cavity
VCORE Cap:38 pcs
VGT Cap:14 pcs
BOT Side Socket Cavity
MICRO-STAR INT'L CO.,LTD
MS-7D22
CPU-Power
Date: Friday, December 18, 2020
Sheet 6 of 67



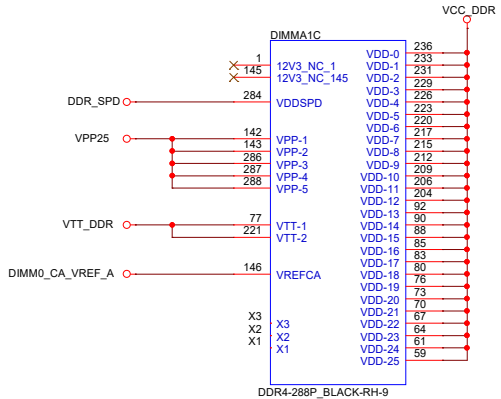


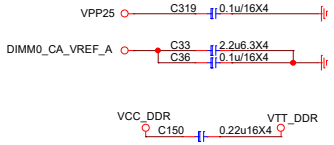
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: CPU-GND	Rev: 10
Date: Friday, December 18, 2020	Sheet 7 of 67	

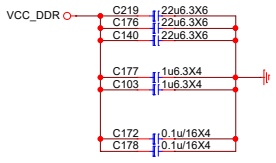

A0
B0
VCC_DDR
DIMMA1A
DDR4-288P_BLACK-RH-9
M_DATA_A[63..0] [4]
M_MAA_A[16..0]
M_MAA_A[16..0] [4]
M_BG_A_1 [4]
M_BG_A_0 [4]
M_BA_A_1 [4]
M_BA_A_0 [4]
SMBCLK_VCC [9,12]
SMBDATA_VCC [9,12]
DIMM1_EVENT
R131
240R1%4
R122
470R/4
[9,12] DRAM_RESET#
C128
X_0.1u16X4
close Pin58
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7D22
Size Custom
Document Description
DDR4 SLOT-DIMM1
Rev 10
Date: Friday, December 18, 2020
Sheet 8 of 67

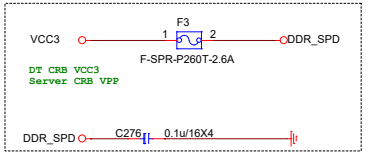


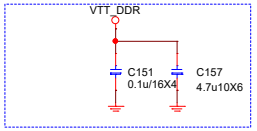
MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: DDR4 SLOT-DIMM2
Rev: 10	
Date: Friday, December 18, 2020	Sheet 9 of 67

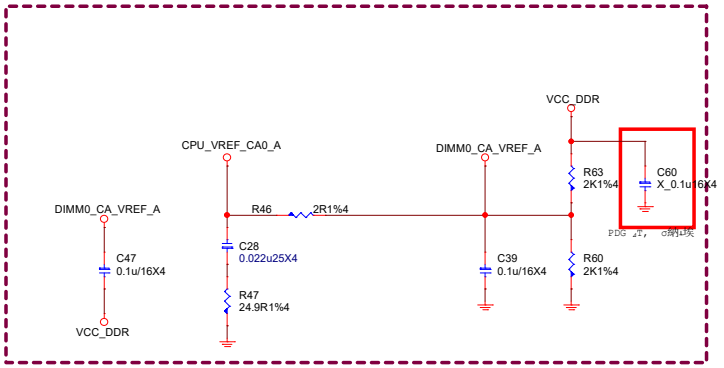


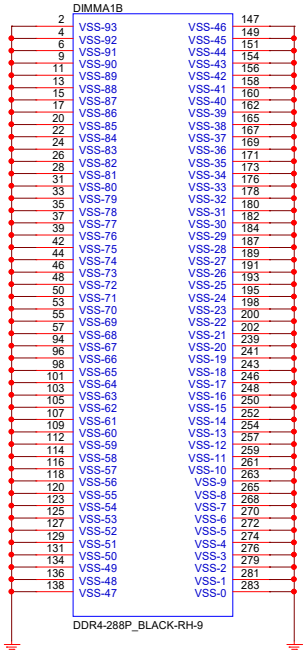


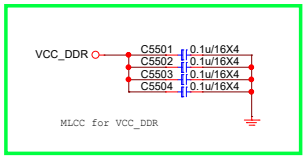




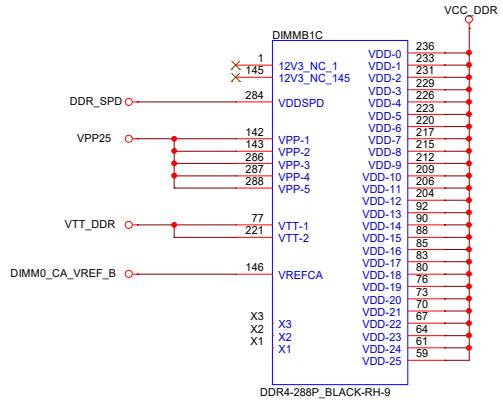


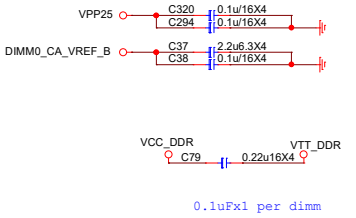




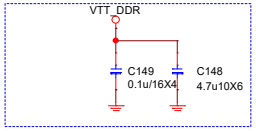


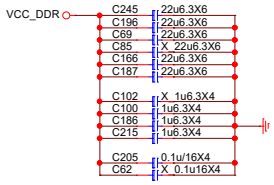
MICRO-STAR INT'L CO.,LTD			
MS-7D22			
Size: Custom	Document Description: DDR4-POWER/GND-1		Rev: 10
Date: Friday, December 18, 2020		Sheet 10 of 67	

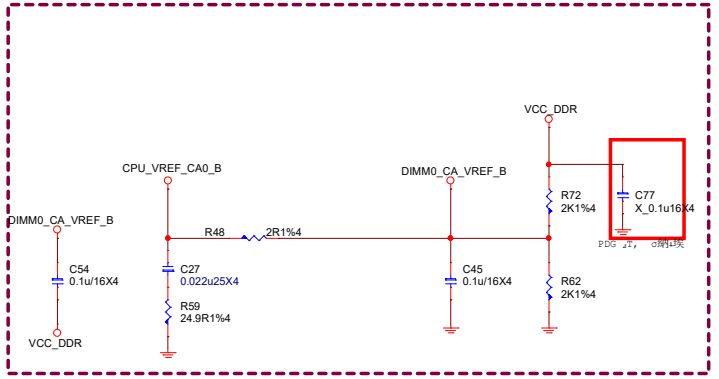


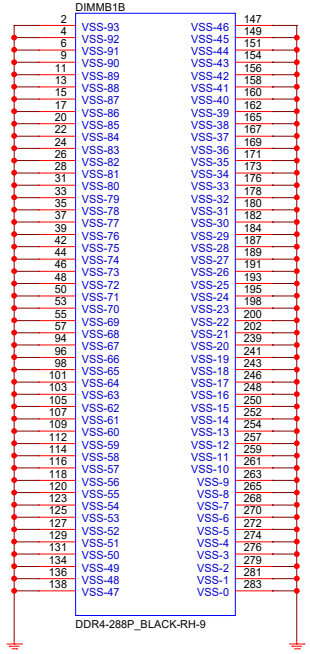


0.1uFx1 per dimm

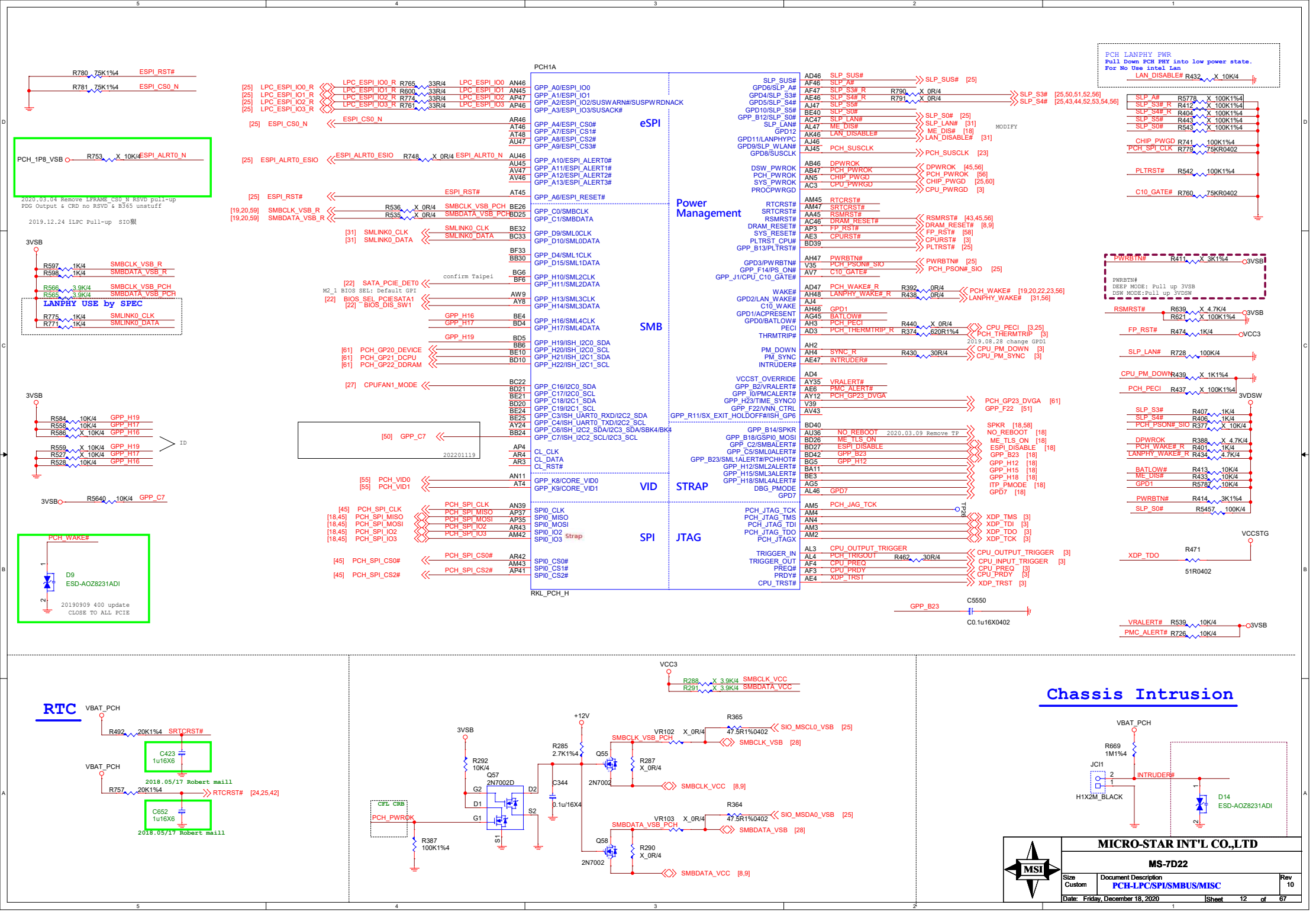




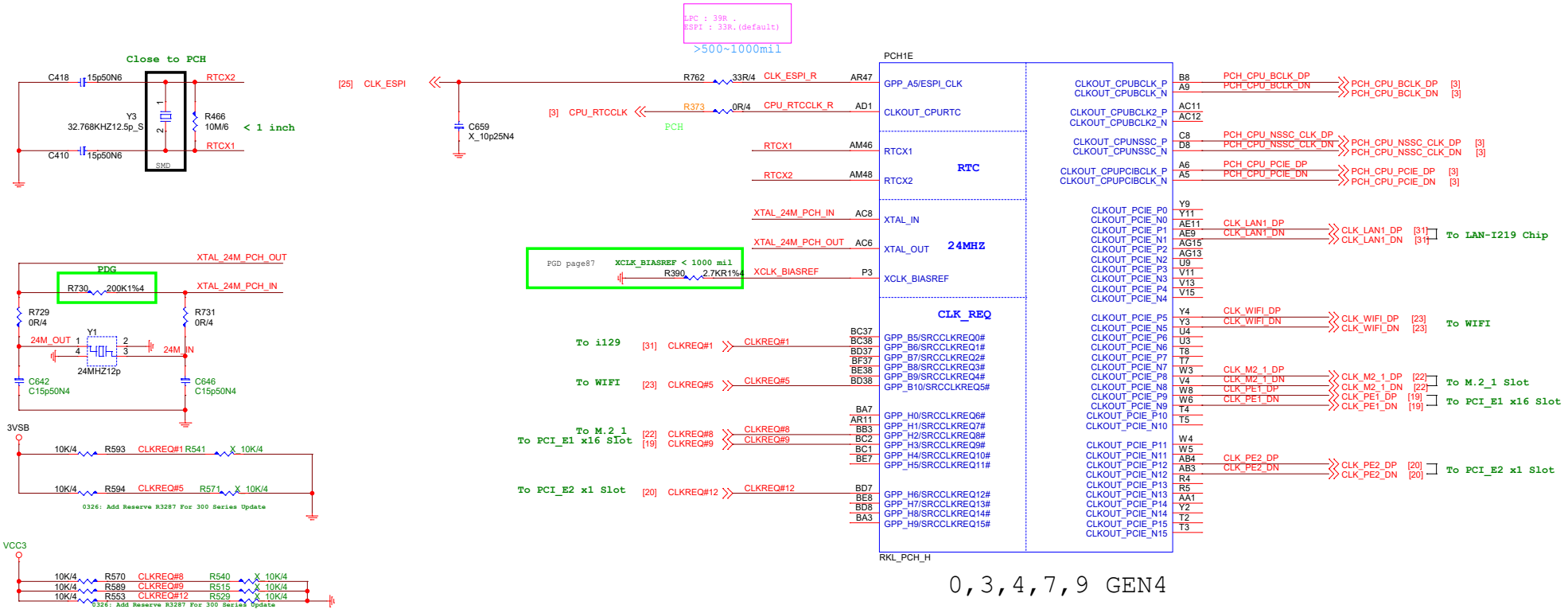




MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 10
Date: Friday, December 18, 2020	Sheet 11 of 67	

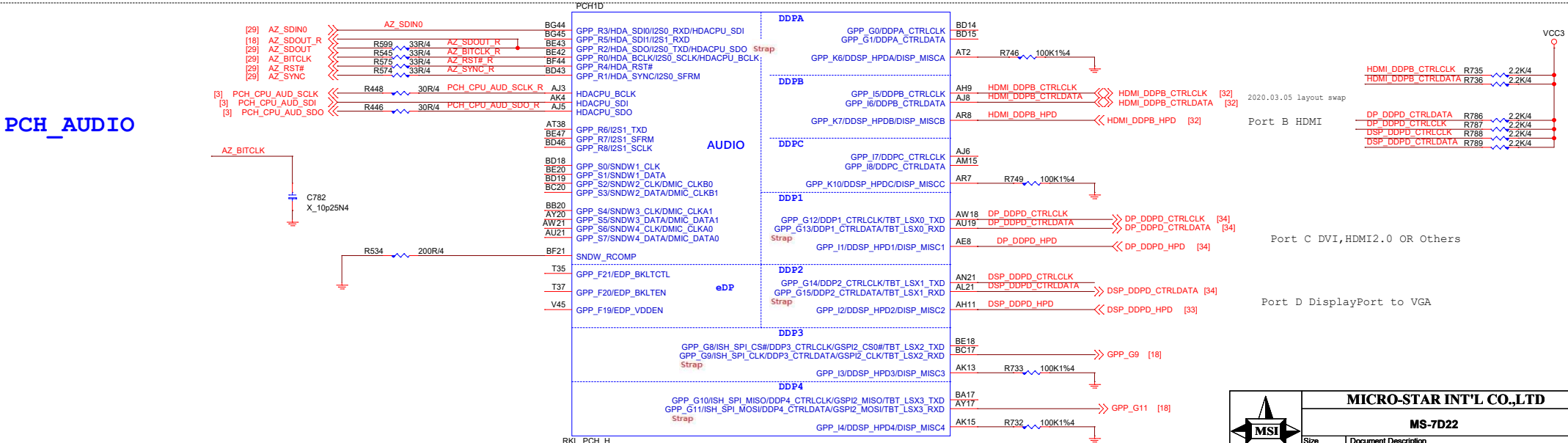

PCH1A
eSPI
Power Management
SMB
VID
SPI
STRAP
JTAG
RKL_PCH_H
PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
LANPHY USE by SPEC
RTC
Chassis Intrusion
MICRO-STAR INT'L CO.,LTD
MS-7D22
PCH-LPC/SPI/SMBUS/MISC

PCH_CLK



0,3,4,7,9 GEN4

PCH_AUDIO



MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: PCH-Clock/Audio
Rev: 10	
Date: Friday, December 18, 2020	Sheet 13 of 67

PCH1B

DMI

DMI0_RXP J32 ← DMI_TXP0 ← [5] DMI_TXP0
DMI0_RXN L31 ← DMI_TXN0 ← [5] DMI_TXN0
DMI1_RXP F30 ← DMI_TXP1 ← [5] DMI_TXP1
DMI1_RXN H30 ← DMI_TXN1 ← [5] DMI_TXN1
DMI2_RXP J29 ← DMI_TXP2 ← [5] DMI_TXP2
DMI2_RXN L29 ← DMI_TXN2 ← [5] DMI_TXN2
DMI3_RXP L26 ← DMI_TXP3 ← [5] DMI_TXP3
DMI3_RXN J26 ← DMI_TXN3 ← [5] DMI_TXN3
DMI4_RXP F26
DMI4_RXN H26
DMI5_RXP P26
DMI5_RXN R26
DMI6_RXP R22
DMI6_RXN P22
DMI7_RXP J24
DMI7_RXN L24

DMI0_TXP D32 → DMI_RXP0 → [5] DMI_RXP0
DMI0_TXN C32 → DMI_RXN0 → [5] DMI_RXN0
DMI1_TXP D31 → DMI_RXP1 → [5] DMI_RXP1
DMI1_TXN C30 → DMI_RXN1 → [5] DMI_RXN1
DMI2_TXP E30 → DMI_RXP2 → [5] DMI_RXP2
DMI2_TXN D30 → DMI_RXN2 → [5] DMI_RXN2
DMI3_TXP C29 → DMI_RXP3 → [5] DMI_RXP3
DMI3_TXN B29 → DMI_RXN3 → [5] DMI_RXN3
DMI4_TXP E28
DMI4_TXN D29
DMI5_TXP D27
DMI5_TXN C27
DMI6_TXP D26
DMI6_TXN C26
DMI7_TXP C25
DMI7_TXN A25

PCIE

PCIE1_RXP/USB31_7_RXP J15
PCIE1_RXN/USB31_7_RXN L16
PCIE2_RXP/USB31_8_RXP J18
PCIE2_RXN/USB31_8_RXN L19
PCIE3_RXP/USB31_9_RXP H17
PCIE3_RXN/USB31_9_RXN G17
PCIE4_RXP/USB31_10_RXP P17
PCIE4_RXN/USB31_10_RXN R17
GEN2X2

PCIE1_TXP/USB31_7_TXP C17
PCIE1_TXN/USB31_7_TXN B17
PCIE2_TXP/USB31_8_TXP C18
PCIE2_TXN/USB31_8_TXN D18
PCIE3_TXP/USB31_9_TXP E17
PCIE3_TXN/USB31_9_TXN D17
PCIE4_TXP/USB31_10_TXP D19
PCIE4_TXN/USB31_10_TXN C20

PCIE5_RXP (GBE) F20 ← PE5_M2_RXP_SW ← [22] PE5_M2_RXP_SW
PCIE5_RXN H20 ← PE5_M2_RXN_SW ← [22] PE5_M2_RXN_SW
PCIE6_RXP J21 ← PE6_M2_RXP ← [22] PE6_M2_RXP
PCIE6_RXN L21 ← PE6_M2_RXN ← [22] PE6_M2_RXN
PCIE7_RXP P19 ← PE7_M2_RXP ← [22] PE7_M2_RXP
PCIE7_RXN R19 ← PE7_M2_RXN ← [22] PE7_M2_RXN
PCIE8_RXP F24 ← PE8_M2_RXP ← [22] PE8_M2_RXP
PCIE8_RXN H24 ← PE8_M2_RXN ← [22] PE8_M2_RXN

PCIE5_TXP D21 → PE5_M2_TXP_SW → [22] PE5_M2_TXP_SW
PCIE5_TXN C21 → PE5_M2_TXN_SW → [22] PE5_M2_TXN_SW
PCIE6_TXP E20 → PE6_M2_TXP → [22] PE6_M2_TXP
PCIE6_TXN D20 → PE6_M2_TXN → [22] PE6_M2_TXN
PCIE7_TXP C23 → PE7_M2_TXP → [22] PE7_M2_TXP
PCIE7_TXN D23 → PE7_M2_TXN → [22] PE7_M2_TXN
PCIE8_TXP B21 → PE8_M2_TXP → [22] PE8_M2_TXP
PCIE8_TXN A22 → PE8_M2_TXN → [22] PE8_M2_TXN
To M.2_1

PCIE9_RXP (GBE) G33 ← PE9_LAN_RXP ← [31] PE9_LAN_RXP
PCIE9_RXN H33 ← PE9_LAN_RXN ← [31] PE9_LAN_RXN
PCIE10_RXP J35
PCIE10_RXN L34
PCIE9_TXP C33 → PE9_LAN_TXP → [31] PE9_LAN_TXP
PCIE9_TXN B33 → PE9_LAN_TXN → [31] PE9_LAN_TXN
PCIE10_TXP D34
PCIE10_TXN E34
To LAN-I219 Chip

PCIE11_RXP/SATA0A_RXP G36 ← PE11_WIFI_RXP ← [23] PE11_WIFI_RXP
PCIE11_RXN/SATA0A_RXN H35 ← PE11_WIFI_RXN ← [23] PE11_WIFI_RXN
PCIE12_RXP/SATA1A_RXP L36 ← PE12_X1_RX ← [20] PE12_X1_RX
PCIE12_RXN/SATA1A_RXN J37 ← PE12_X1_RX# ← [20] PE12_X1_RX#
(GBE)

PCIE11_TXP/SATA0A_TXP D35
PCIE11_TXN/SATA0A_TXN C35 → PE11_WIFI_TXP → [23] PE11_WIFI_TXP
PCIE12_TXP/SATA1A_TXP C36 → PE11_WIFI_TXN → [23] PE11_WIFI_TXN
PCIE12_TXN/SATA1A_TXN D36 → PE12_X1_TX → [20] PE12_X1_TX
To WIFI
To PCIE X1

PCIE13_RXP/SATA0B_RXP G39 ← SATA_RX0 ← [21] SATA_RX0
PCIE13_RXN/SATA0B_RXN H38 ← SATA_RX0# ← [21] SATA_RX0#
PCIE14_RXP/SATA1B_RXP H42 ← SATA_RX1 ← [21] SATA_RX1
PCIE14_RXN/SATA1B_RXN J41 ← SATA_RX1# ← [21] SATA_RX1#
PCIE15_RXP/SATA2_RXP C46 ← SATA_RX2 ← [21] SATA_RX2
PCIE15_RXN/SATA2_RXN D45 ← SATA_RX2# ← [21] SATA_RX2#
PCIE16_RXP/SATA3_RXP C47 ← SATA_RX3_SW ← [22] SATA_RX3_SW
PCIE16_RXN/SATA3_RXN D46 ← SATA_RX3#_SW ← [22] SATA_RX3#_SW
(GBE)

PCIE13_TXP/SATA0B_TXP B37
PCIE13_TXN/SATA0B_TXN C38 → SATA_TX0 → [21] SATA_TX0
PCIE14_TXP/SATA1B_TXP E38 → SATA_TX0# → [21] SATA_TX0#
PCIE14_TXN/SATA1B_TXN D38 → SATA_TX1 → [21] SATA_TX1
PCIE15_TXP/SATA2_TXP D39 → SATA_TX1# → [21] SATA_TX1#
PCIE15_TXN/SATA2_TXN C39 → SATA_TX2 → [21] SATA_TX2
PCIE16_TXP/SATA3_TXP C40 → SATA_TX2# → [21] SATA_TX2#
PCIE16_TXN/SATA3_TXN D40 → SATA_TX3_SW → [22] SATA_TX3_SW
SATA_TX3#_SW → [22] SATA_TX3#_SW
To SATA1
To SATA2
To SATA3
To SATA4

PCIE17_RXP/SATA4_RXP G43
PCIE17_RXN/SATA4_RXN F44
PCIE18_RXP/SATA5_RXP L42
PCIE18_RXN/SATA5_RXN K43
PCIE19_RXP/SATA6_RXP L41
PCIE19_RXN/SATA6_RXN N39
PCIE20_RXP/SATA7_RXP M37
PCIE20_RXN/SATA7_RXN M35

PCIE17_TXP/SATA4_TXP E41
PCIE17_TXN/SATA4_TXN D42
PCIE18_TXP/SATA5_TXP C42
PCIE18_TXN/SATA5_TXN B42
PCIE19_TXP/SATA6_TXP D43
PCIE19_TXN/SATA6_TXN C43
PCIE20_TXP/SATA7_TXP B44
PCIE20_TXN/SATA7_TXN A44

PCIE21_RXP N43
PCIE21_RXN N42
PCIE22_RXP R39
PCIE22_RXN P41
PCIE23_RXP P35
PCIE23_RXN P37
PCIE24_RXP T42
PCIE24_RXN T43

PCIE21_TXP E48
PCIE21_TXN E49
PCIE22_TXP G47
PCIE22_TXN F47
PCIE23_TXP J46
PCIE23_TXN J47
PCIE24_TXP H45
PCIE24_TXN G45

Max 16 pcie root ports(include GBE)

PCIE_RCOMPP B13
PCIE_RCOMPN A13
PCIECOMP_P
PCIECOMP_N
R328 100R1%4 PGD page87
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil

RKL_PCH_H

[19] PE1_WAKE# ← GPP_E4/SATA_DEVSLP0 N47
GPP_E5/SATA_DEVSLP1 M45
GPP_E6/SATA_DEVSLP2 M46
GPP_E0/SATAXPCIE0/SATAGP0 R45 → GPP_E0
GPP_E1/SATAXPCIE1/SATAGP1 P47 → GPP_E1
GPP_E2/SATAXPCIE2/SATAGP2 P46 → GPP_E2

[22] DEVSLP3 ← DEVSLP3 ← GPP_F5/SATA_DEVSLP3 W47
GPP_F6/SATA_DEVSLP4 V46
GPP_F7/SATA_DEVSLP5 U46
GPP_F8/SATA_DEVSLP6 U47
GPP_F9/SATA_DEVSLP7 T45
GPP_F0/SATAXPCIE3/SATAGP3 Y46 → GPP_F0
GPP_F1/SATAXPCIE4/SATAGP4 Y48 → GPP_F1
GPP_F2/SATAXPCIE5/SATAGP5 Y47 → GPP_F2
GPP_F3/SATAXPCIE6/SATAGP6 W46 → GPP_F3
GPP_F4/SATAXPCIE7/SATAGP7 W45 → GPP_F3 [58]

[27] SYSFAN1_MODE ← GPP_F10/SATA_SCLOCK T46
GPP_F11/SATA_SLOAD T48
GPP_F12/SATA_SDATAOUT1 T47
GPP_F13/SATA_SDATAOUT0 R46
GPP_E8/SATALED#/SPI1_CS1# L47 → PCH_SATA_LED# [58]

3VSB
PE1_WAKE# R602 10K/4 VCC3

PCH1C

USB32

MB_USB30_RX1+ [38] C10 USB31_1_RXP
MB_USB30_RX1- [38] D10 USB31_1_RXN
MB_USB30_RX2+ [38] E11 USB31_2_RXP
MB_USB30_RX2- [38] G11 USB31_2_RXN
GEN2X2
USB31_1_TXP C3 → MB_USB30_TX1+ [38]
USB31_1_TXN D4 → MB_USB30_TX1- [38]
USB31_2_TXP F6 → MB_USB30_TX2+ [38]
USB31_2_TXN D5 → MB_USB30_TX2- [38]
USB1

MB_USB30_RX3+ [37] D12 USB31_3_RXP
MB_USB30_RX3- [37] E12 USB31_3_RXN
MB_USB30_RX4+ [37] C11 USB31_4_RXP
MB_USB30_RX4- [37] D11 USB31_4_RXN
GEN2X2
USB31_3_TXP M13 → MB_USB30_TX3+ [37]
USB31_3_TXN M15 → MB_USB30_TX3- [37]
USB31_4_TXP D14 → MB_USB30_TX4+ [37]
USB31_4_TXN C14 → MB_USB30_TX4- [37]
JUSB2

USB31_5_RXP H15
USB31_5_RXN G14
USB31_6_RXP J13
USB31_6_RXN H12
GEN2X2
USB31_5_TXP D15
USB31_5_TXN C15
USB31_6_TXP E16
USB31_6_TXN D16

USB2

GPP_E9/USB_OC0# OC#0 [38] L46
GPP_E10/USB_OC1# OC#1 [37] L45
GPP_E11/USB_OC2# OC#2 K47
GPP_E12/USB_OC3# OC#3 [36] K46
GPP_I11/USB_OC4#/I2C4_SDA OC#4 [39] AM13
GPP_I12/USB_OC5#/I2C4_SCL OC#5 AK11
GPP_I13/USB_OC6#/I2C5_SDA OC#6 AP13
GPP_I14/USB_OC7#/I2C5_SCL OC#7 AM7

USB2P_1 K4 → MB_USB_1D+ [38]
USB2N_1 K3 → MB_USB_1D- [38]
USB2P_2 L8 → MB_USB_2D+ [38]
USB2N_2 K7 → MB_USB_2D- [38]
USB2P_3 L5 → MB_USB_3D+ [37]
USB2N_3 L4 → MB_USB_3D- [37]
USB2P_4 H7 → MB_USB_4D+ [59]
USB2N_4 G7 → MB_USB_4D- [59]
USB2P_5 M2 → MB_USB_5D+ [37]
USB2N_5 M1 → MB_USB_5D- [37]
USB1
JUSB2
MCU FOR LAYOUT

USB2P_6 L9 → MB_USB_6D+ [23]
USB2N_6 N11 → MB_USB_6D- [23]
USB2P_7 L3 → MB_USB_7D+ [36]
USB2N_7 M4 → MB_USB_7D- [36]
USB2P_8 G5 → MB_USB_8D+ [36]
USB2N_8 H5 → MB_USB_8D- [36]
USB2P_9 R11 → MB_USB_9D+ [41]
USB2N_9 P9 → MB_USB_9D- [41]
AX210
JUSB1
HUB GL850
LAN_USB1
BT2_USB1

USB2P_10 J3
USB2N_10 J4
USB2P_11 N8
USB2N_11 N7
USB2P_12 G3
USB2N_12 G2
USB2P_13 N3
USB2N_13 N4
USB2P_14 P13
USB2N_14 P15

USB_ID
USB_VBUSSENSE
USB2_COMP

R343 10K/4 USB2_ID F3
R333 10K/4 U2_VBUSE E1
R339 113R1%4 USB2_COMP E2
PGD page87
USB2_COMP < 1000 mil

H510 Not support

3VSB
R337 10K/4 OC#2
R738 10K/4 OC#5
R737 10K/4 OC#6
R739 10K/4 OC#7

OC [x]# pins require a pull-up to V3.3 A with 8.2

OC#0 C5551 C0.1u16X0402
OC#2 C5552 C0.1u16X0402
OC#3 C5553 C0.1u16X0402

3VSB
GPP_E0 R354 10K/4
GPP_E1 R5458 10K/4
GPP_E2 R352 10K/4
GPP_F0 R375 10K/4
GPP_F1 R383 X 10K/4
GPP_F2 R378 X 10K/4

确认接法，确认BIOS Porting 为GPO High, cost down

21ci203T

MICRO-STAR INT'L CO.,LTD
MS-7D22
Size: Custom
Document Description: PCH-DMI/PCIE/USB/SATA
Rev: 10
Date: Friday, December 18, 2020
Sheet 14 of 67

	GPP_G21	GPP_G22	GPP_G11
H410M PRO	0	0	0
H410M-A PRO	0	0	1
H410M GLOCK	0	1	1

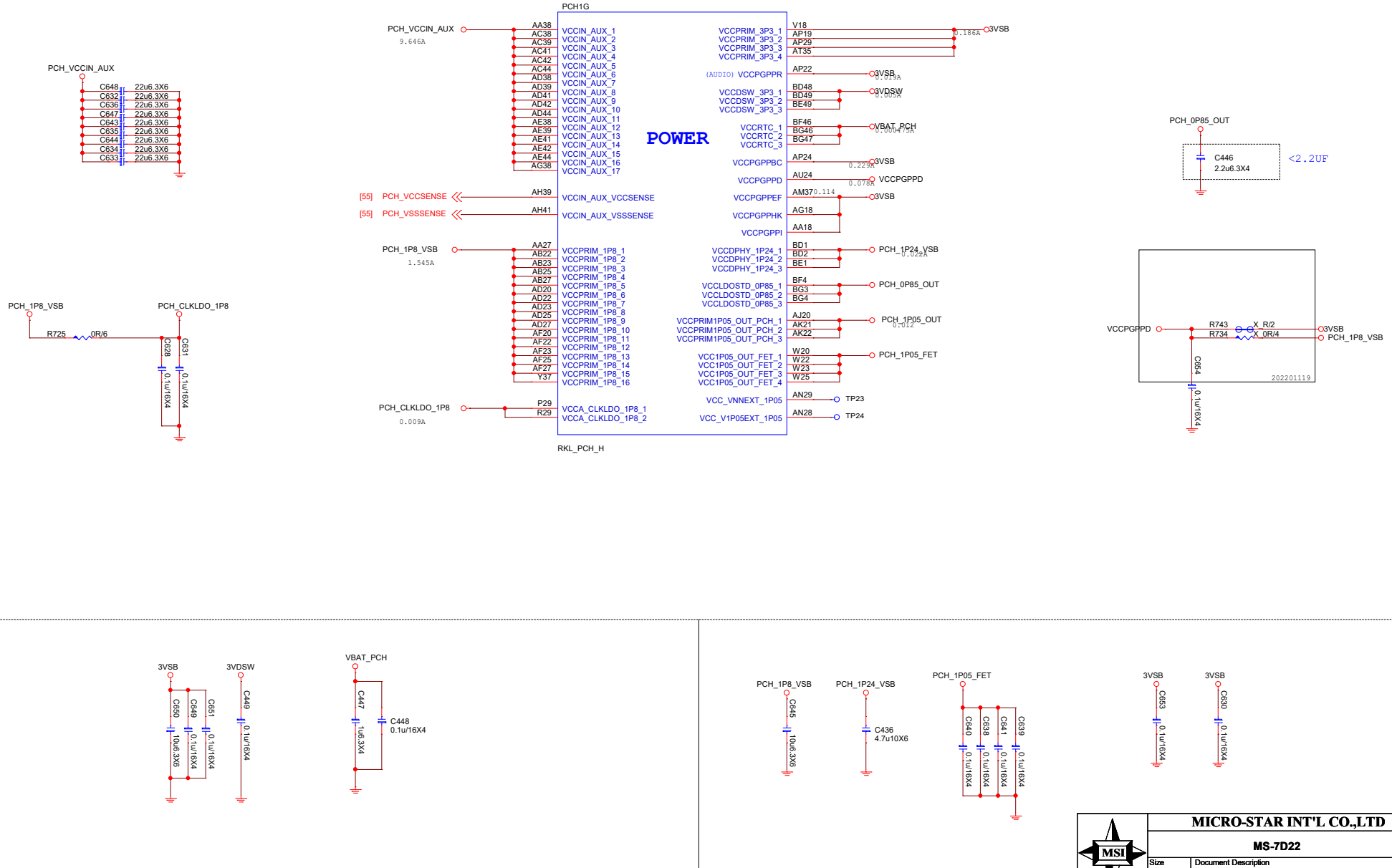
BIOS Select USE

MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	PCH-GPIO/RSVD	10

Date: Friday, December 18, 2020 Sheet 15 of 67

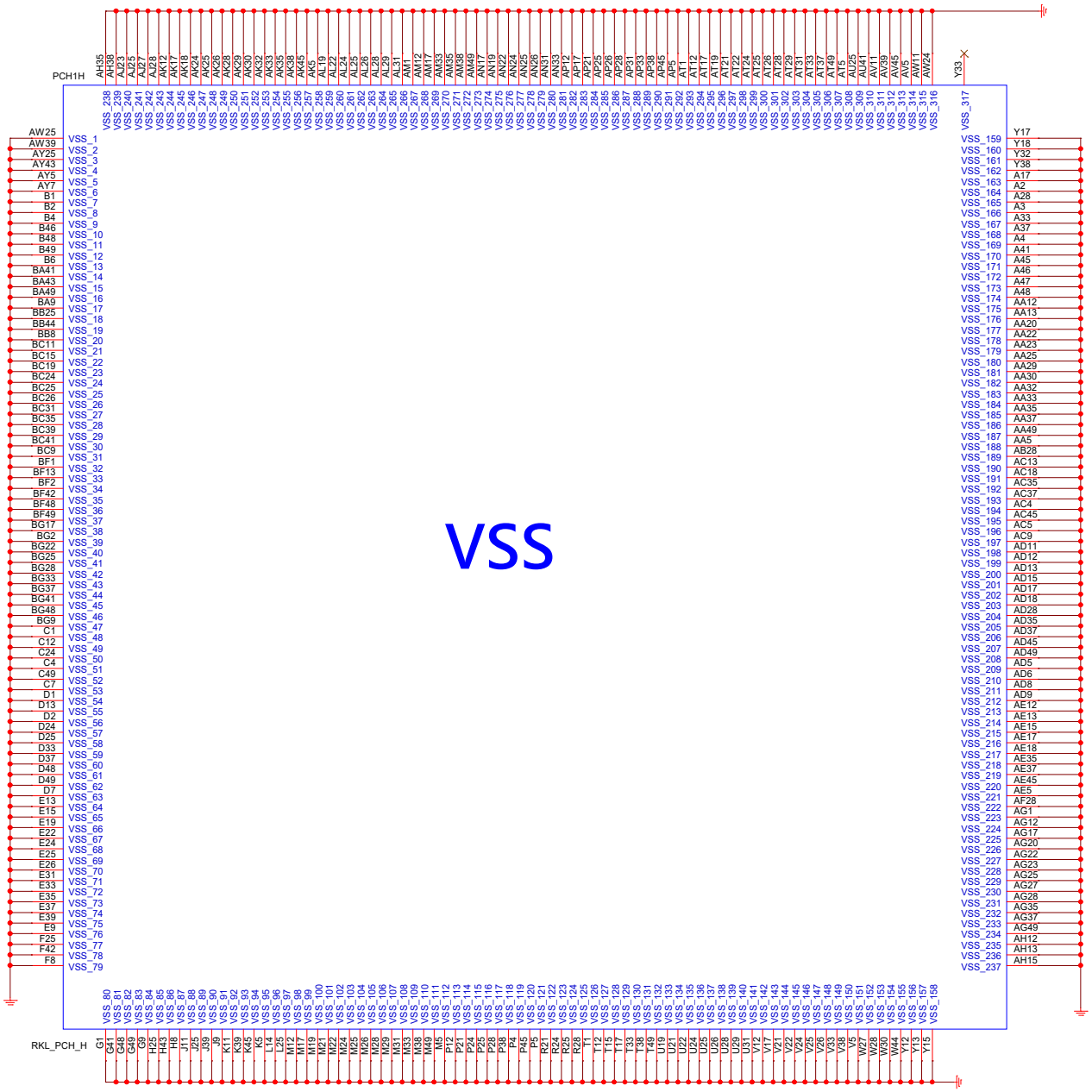


MICRO-STAR INT'L CO.,LTD

MS-7D22

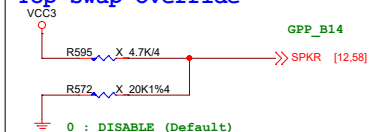
Size	Document Description	Rev
Custom	PCH-Power	10

Date: Friday, December 18, 2020 Sheet 16 of 67



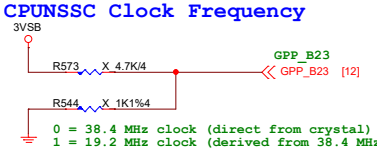
MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: PCH-GND
Rev: 10	
Date: Friday, December 18, 2020	Sheet 17 of 67

Top Swap Override



0 : DISABLE (Default)
1 : ENABLE
Internal Pull-down is disabled after PCH_PWROK is high.

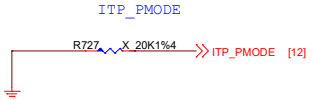
CPUNSSC Clock Frequency



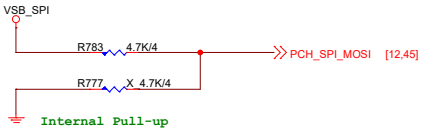
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)

Internal Pull-down is disabled after RSMRST# de-assert.

ITP_PMODE

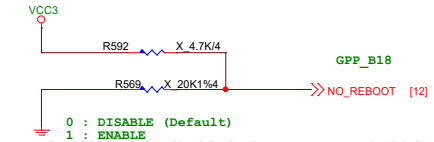


Reserved



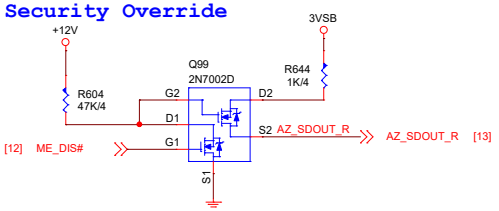
Internal Pull-up

No Reboot



0 : DISABLE (Default)
1 : ENABLE
Internal Pull-down is disabled after PCH_PWROK is high.

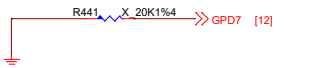
Flash Descriptor Security Override



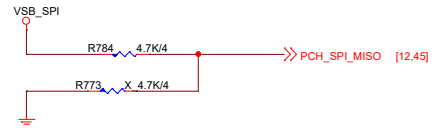
0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE:Flash Descritior Decurity(Override).

Internal Pull-down is disabled after PCH_PWROK is high.

R441

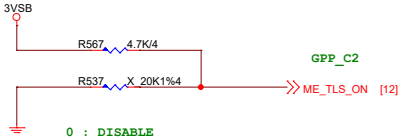


Reserved



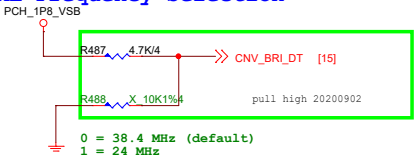
Internal Pull-up

TLS Confidentiality



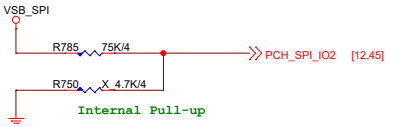
0 : DISABLE
1 : ENABLE (Default)
Internal Pull-down is disabled after RSMRST# de-assert.

XTAL Frequency Selection



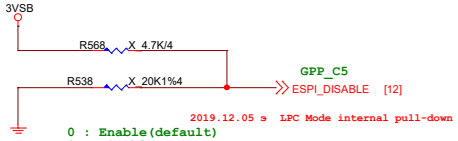
0 = 38.4 MHz (default)
1 = 24 MHz
INTERNAL 20K PD
The internal pull-down is disabled after RSMRST# de-asserts

Reserved



Internal Pull-up

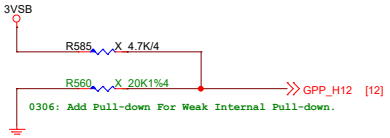
eSPI Disable



2019.12.05 s LPC Mode internal pull-down
0 : Enable(default)
1 : Disable

Internal Pull-down is disabled after RSMRST# de-assert.

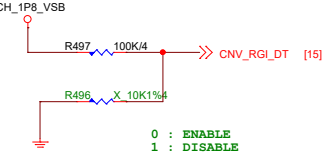
ESPI FLASH SHARING MODE



0306: Add Pull-down For Weak Internal Pull-down.

0=>Master Attached Flash Sharing (MAFS) enabled (Default)
1=>Slave Attached Flash Sharing (SAFS) enabled.
Internal Pull-down is disabled after RSMRST# de-assert.

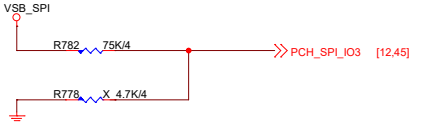
M.2 CNVi Mode Select



0 : ENABLE
1 : DISABLE

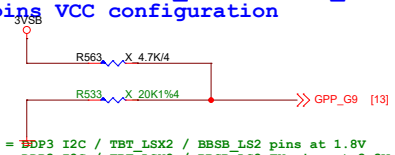
When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface

Reserved



Internal Pull-up

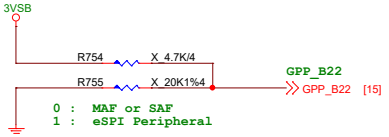
DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins VCC configuration



0 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1 = DDP3 I2C / TBT_LSX2 / BBSB_LS2_TX pins at 3.3V

Internal Pull-down is disabled after RSMRST# de-assert.

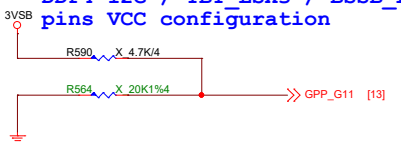
Boot BIOS Strap (BBS)



0 : MAF or SAF
1 : eSPI Peripheral

Internal Pull-down is disabled after PCH_PWROK is high.

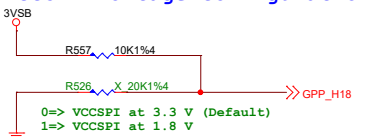
DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins VCC configuration



0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C /TBT_LSX3 / BBSB_LS3 pins at 3.3V

Internal Pull-down is disabled after RSMRST# de-assert.

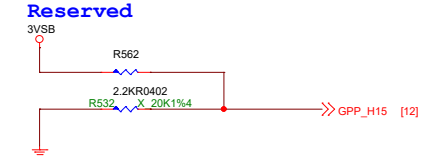
VCCSPI Voltage Configuration



0=> VCCSPI at 3.3 V (Default)
1=> VCCSPI at 1.8 V

The internal pull-down is disabled after RSMRST# de-asserts.

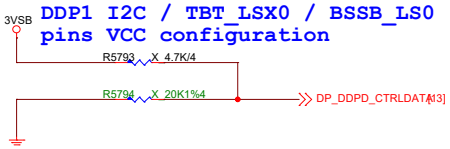
Reserved



0=> JTAG ODT is disabled
1=> JTAG ODT is enable

The internal pull-down is disabled after RSMRST# de-asserts

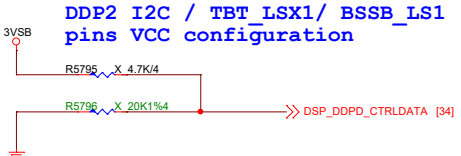
DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins VCC configuration



0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C /TBT_LSX3 / BBSB_LS3 pins at 3.3V

Internal Pull-down is disabled after RSMRST# de-assert.

DDP2 I2C / TBT_LSX1/ BSSB_LS1 pins VCC configuration



0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C /TBT_LSX3 / BBSB_LS3 pins at 3.3V

Internal Pull-down is disabled after RSMRST# de-assert.

MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: PCH-Strap
Rev: 10	
Date: Friday, December 18, 2020	Sheet 18 of 67

PCI Express X16 Slot

GEN3 OR GEN4?

12V - 5.5A

VCC3 - 3A

3VSB- 375mA

PE1_WAKE#_R

D11
ESD-AOZ8231ADI

20190909 400 update
CLOSE TO PCIE1

PCI_E1

SLOT-PCI164P_BLACK-2PITCH-RH-73

[19] GPP_F3

[19] PLTRST_BU1#

PLTRST_BU1#_PCIE1

VCC3 R5791 10K/4

C5554 0.1u/16X4

U71 74LVC1G08GV

R366 X_100R1%4

SMBus ESD

SMBCLK_VSB_R [12,19,20,59]

D6
X_ESD-AOZ8231ADI

SMBDATA_VSB_R [12,19,20,59]

D7
X_ESD-AOZ8231ADI

3VDSW

R5736 10K/4

D48 S-LRB520S-40T1G

R324 X_0R/4

[12,20,22,23,56] PCH_WAKE#

D49 S-LRB520S-40T1G

R323 X_0R/4

[14] PE1_WAKE#

PE1_WAKE#_R

202201119

3VSB C349 0.1u/16X4

C5558 C10u6.3X5-HF

VCC3 C342 0.1u/16X4

EC13 560u6.3V

+12V EC11 270u/16V

C339 0.1u/16X4

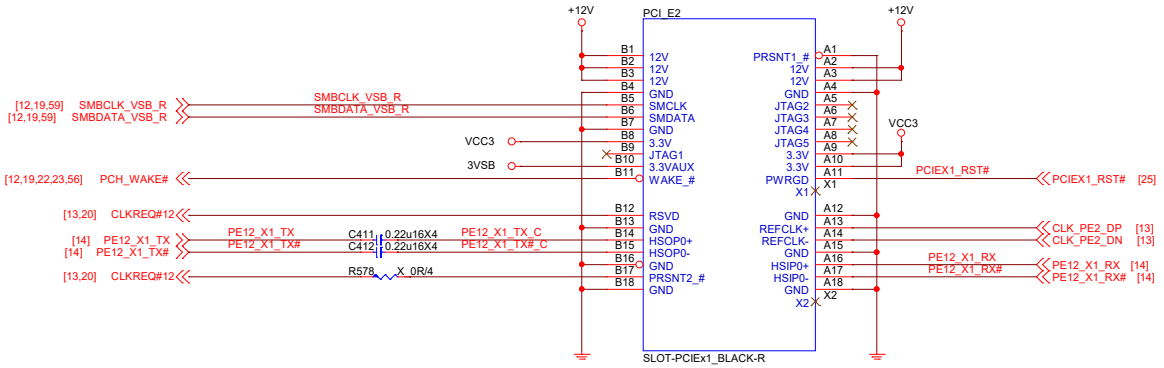
C340 X_22u16X8

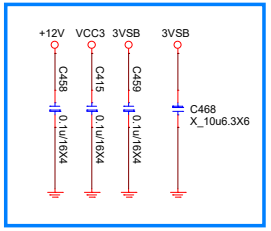
C341 X_22u16X8

add 20190814 for +12V noise

MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 10	
Date: Friday, December 18, 2020	Sheet 19 of 67

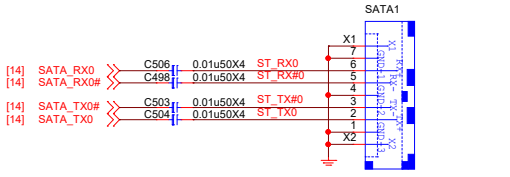
PCIE X1



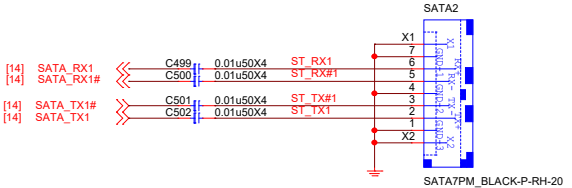


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: M.2-SLOT2	Rev: 10
Date: Friday, December 18, 2020	Sheet 20 of 67	

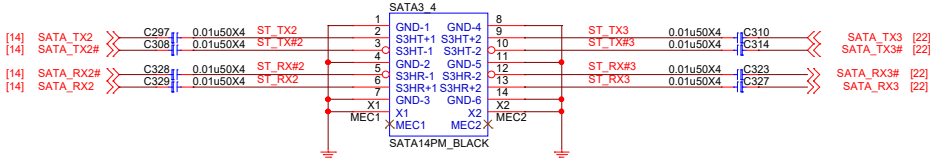
SATA Connector



N5N-07M2441-L06

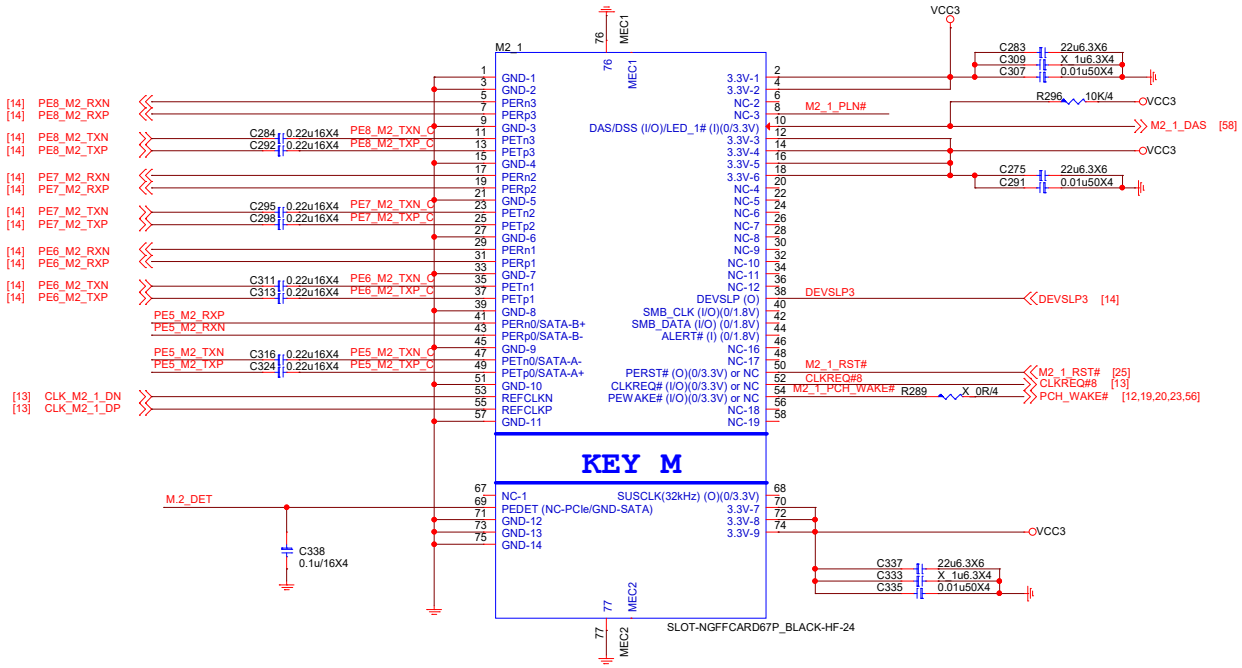


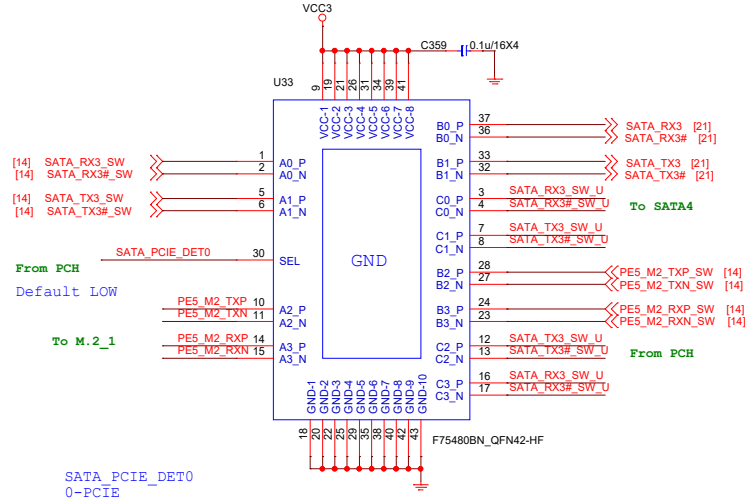
N5N-07M2441-L06

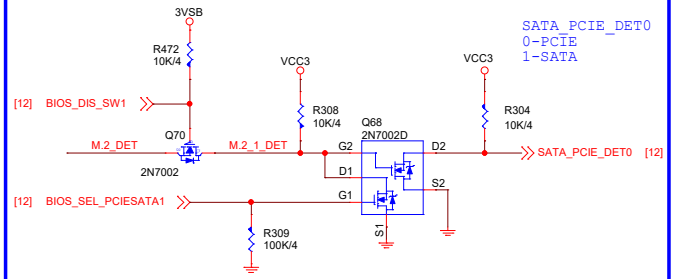


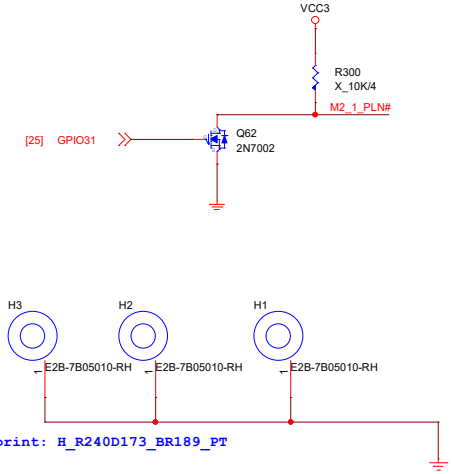
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: SATA Connector	Rev: 10
Date: Friday, December 18, 2020	Sheet 21 of 67	

M2_1









BIOS_MODE

GPP_H14 BIOS_DIS_SW1	GPP_H13 BIOS_SEL_PCIESATA1	Mode	GPP_H11 SATA_PCIE_DET0
0	1	M2-SATA	1
0	0	M2-PCIE	0
GPI(1)	GPI(0)	AUTO	

MICRO-STAR INT'L CO.,LTD

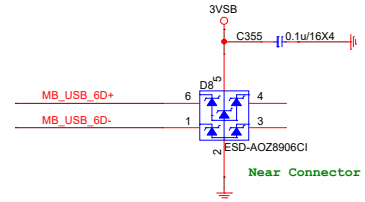
MS-7D22

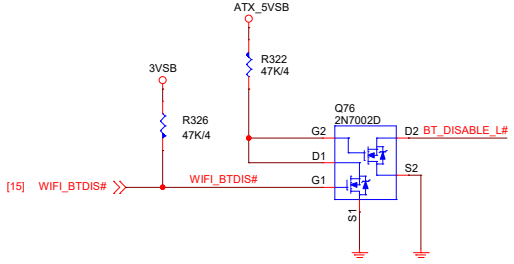
Size	Document Description	Rev
Custom	M.2-SLOT1	10

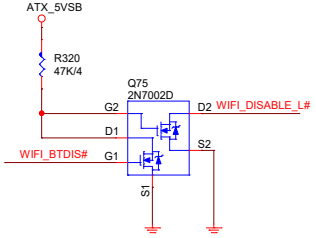
Date: Friday, December 18, 2020 Sheet 22 of 67

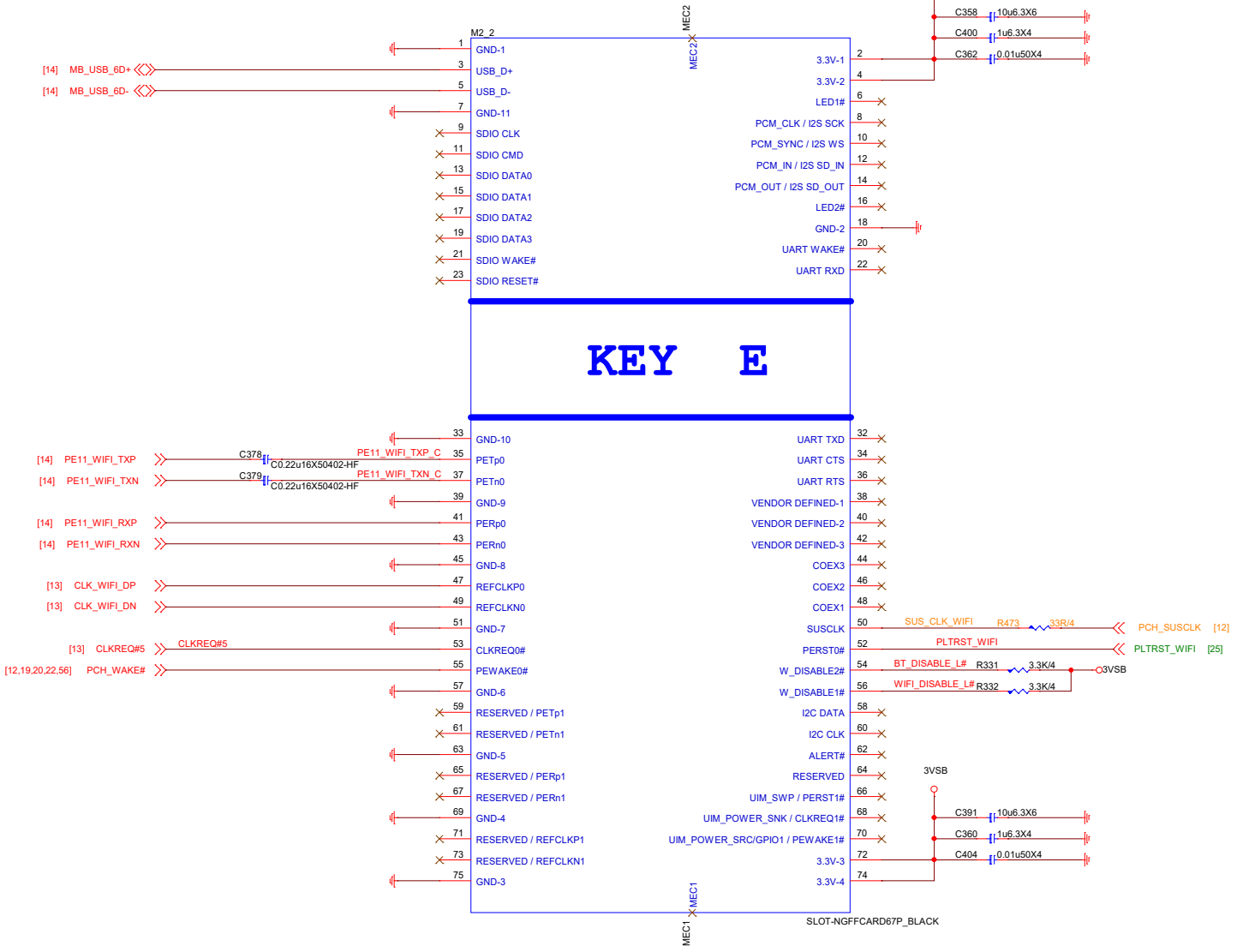
M2_2

950mA peak 2A



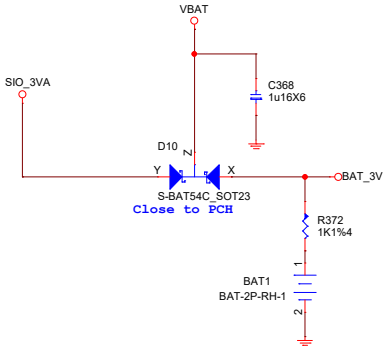


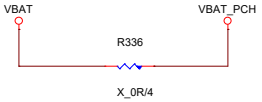


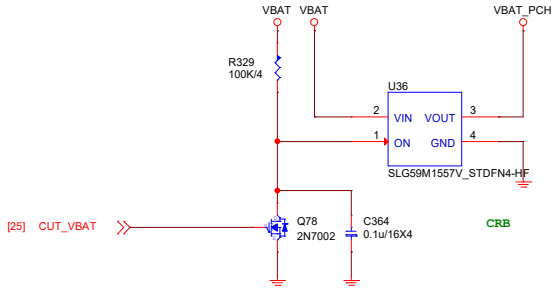


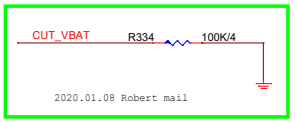
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: WIFI+BT	Rev: 10
Date: Friday, December 18, 2020	Sheet 23 of 67	

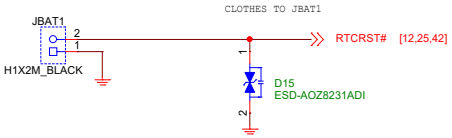
VBAT

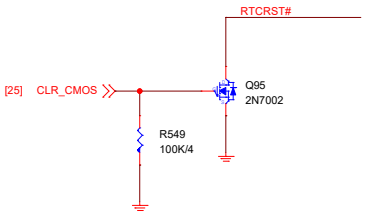












MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: VBAT Circurt	Rev: 10
Date: Friday, December 18, 2020	Sheet 24 of 67	

POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
27	ESPI_EN	KBRST#	LPC(VCC3)	ESPI(3VA)	VCC3 3VA
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789_EN disable	FAN789_EN enable	3VA

Strapping for LPC.

3V Analog Power

Closed PIN 54

Closed PIN1

Closed PIN99

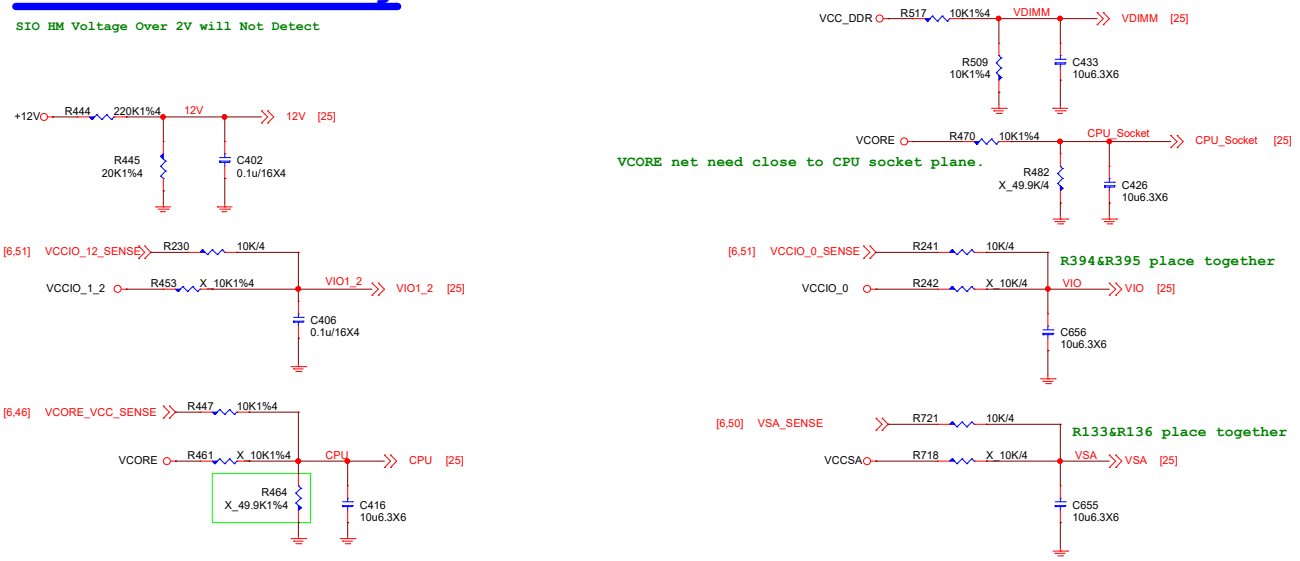
Closed PIN46,85

SPI ROM

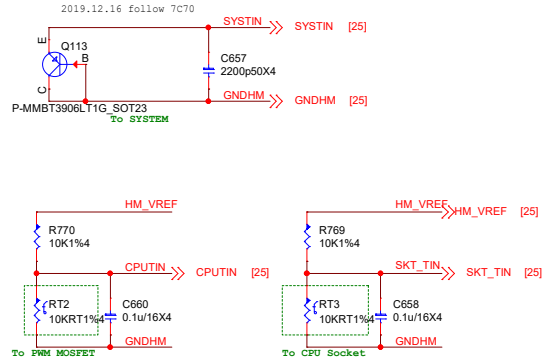
Manufacturer	MICRO-STAR INT'L CO.,LTD
Model	MS-7D22
Size	Custom
Document Description	SIO-NCT5687-1
Rev	10
Date	Friday, December 18, 2020
Sheet	25 of 67

HW Monitor - Voltage

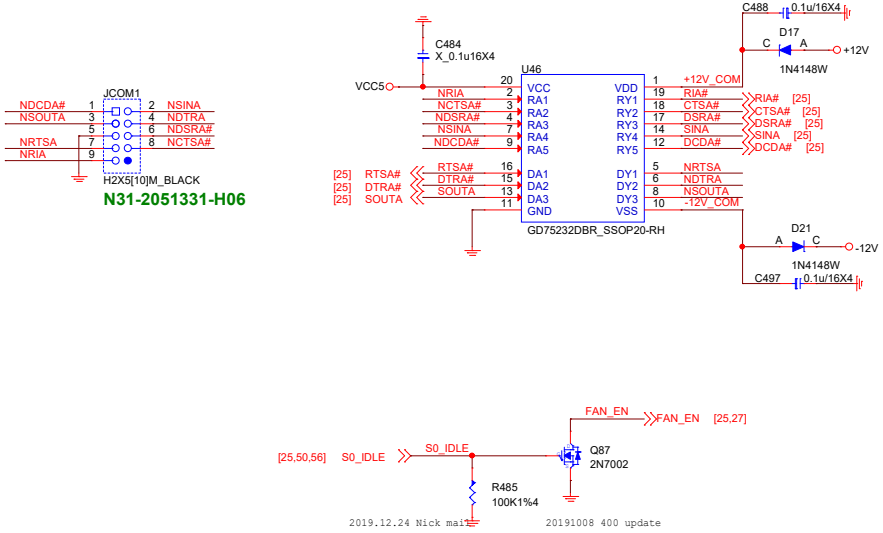
SIO HM Voltage Over 2V will Not Detect



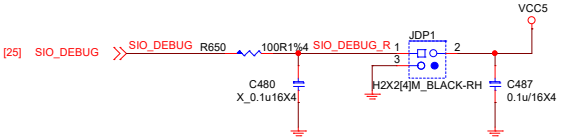
Thermal



COM Port



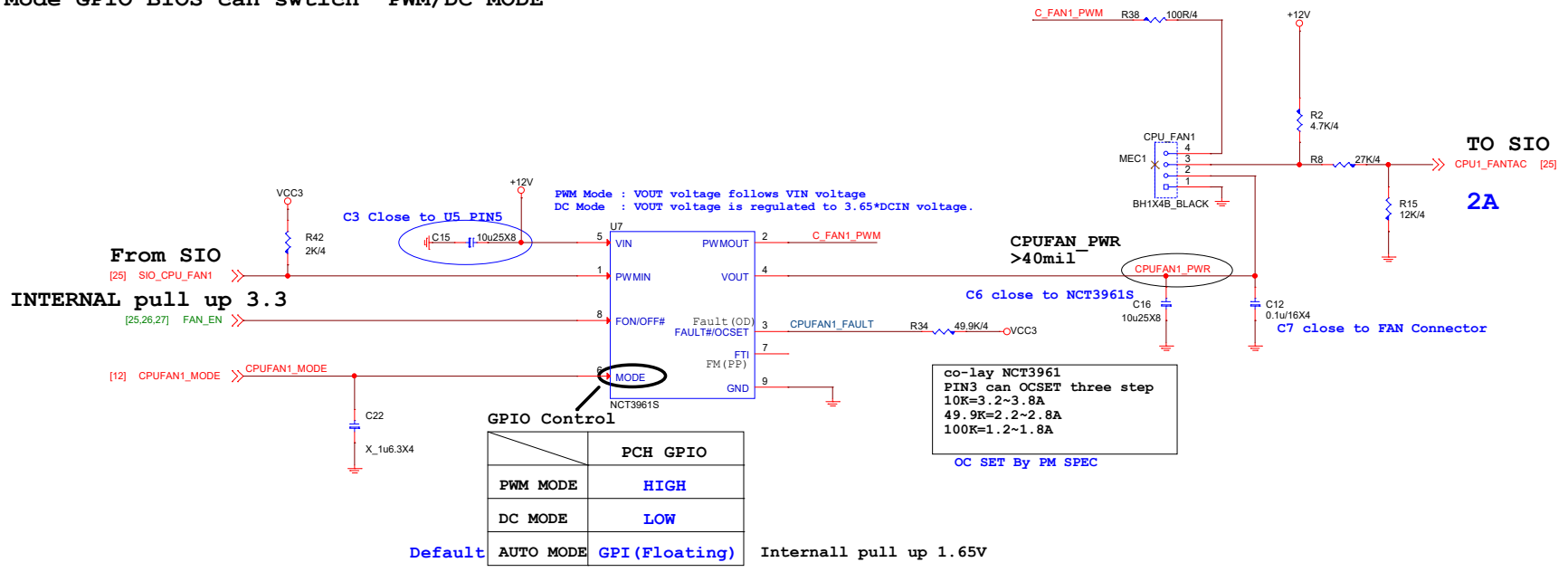
DEBUG PORT



MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: SIO-NCT5687-2	Rev: 10
Date: Friday, December 18, 2020	Sheet 26 of 67	

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



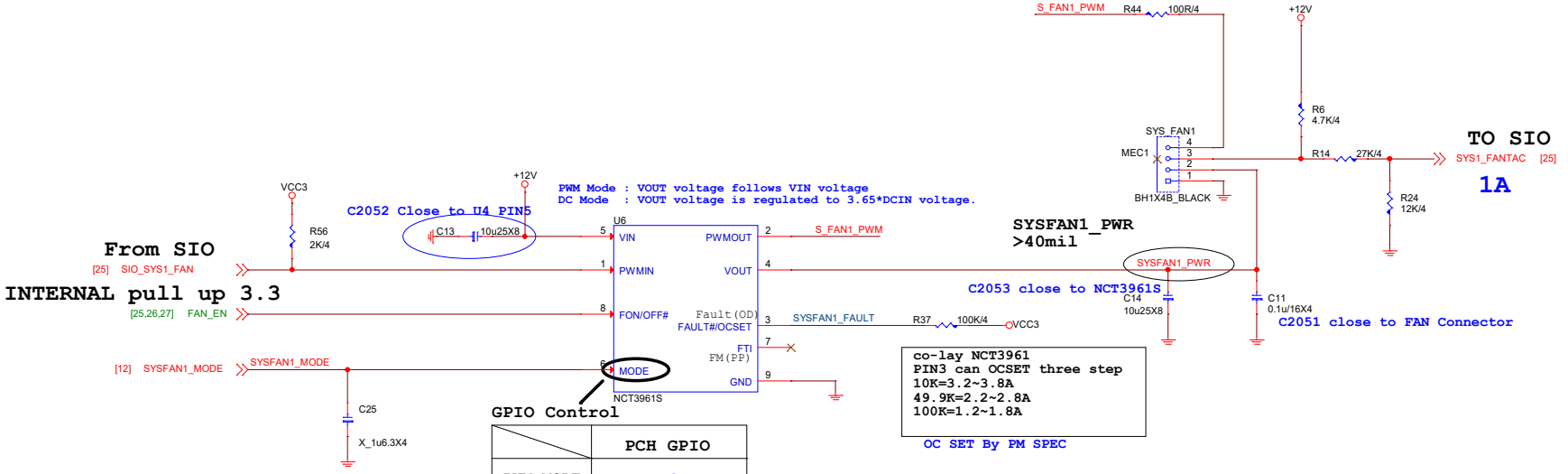
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD

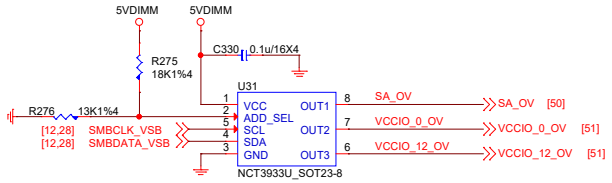
MS-7D22

Size	Document Description	Rev
Custom	CPU and PUMP FAN	10

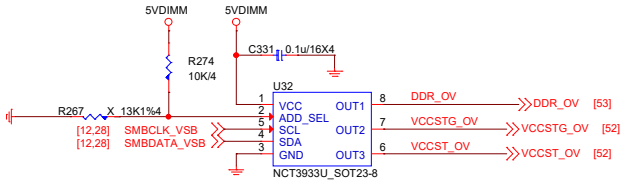
Date: Friday, December 18, 2020 Sheet 27 of 67

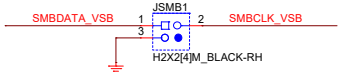
VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



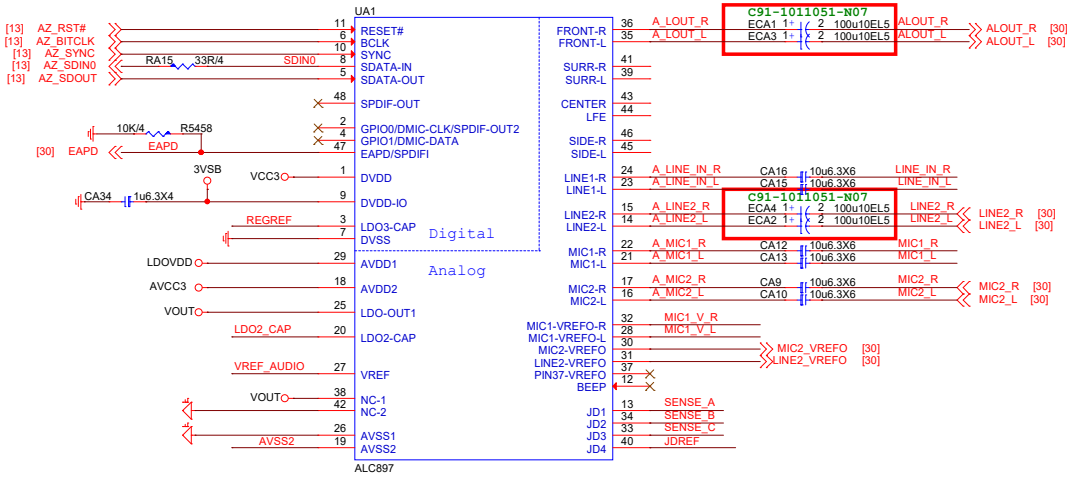
0x20:RH=10K,RL=OPEN

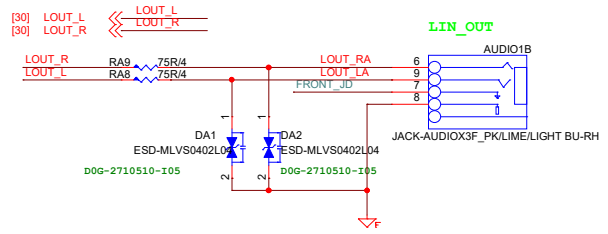


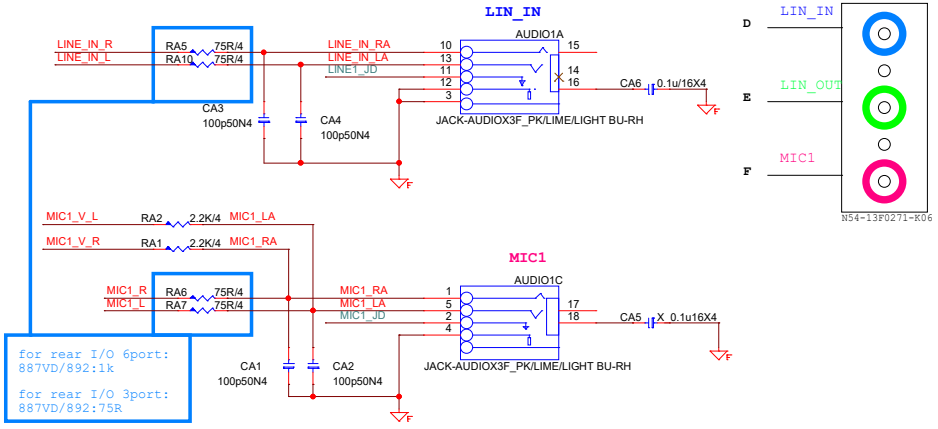


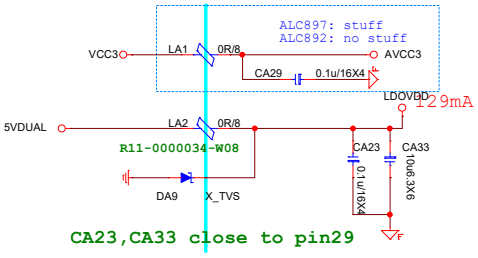
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: NCT3933	Rev: 10
Date: Friday, December 18, 2020	Sheet 28 of 67	

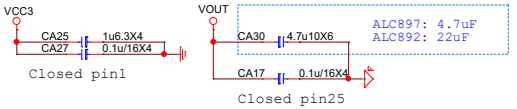
ALC897 COLAY 892

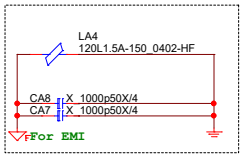


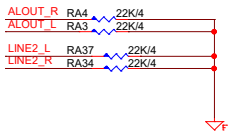




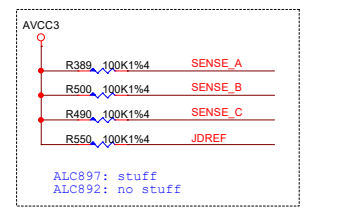


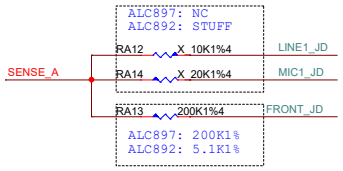


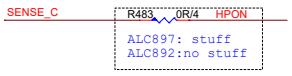


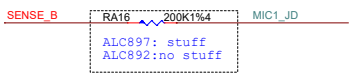


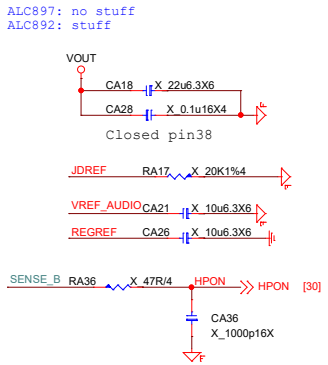
Closed Codec

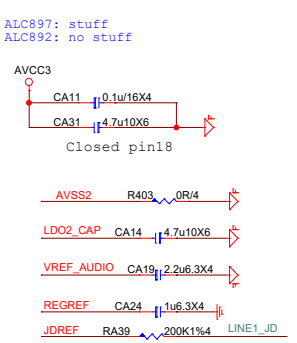












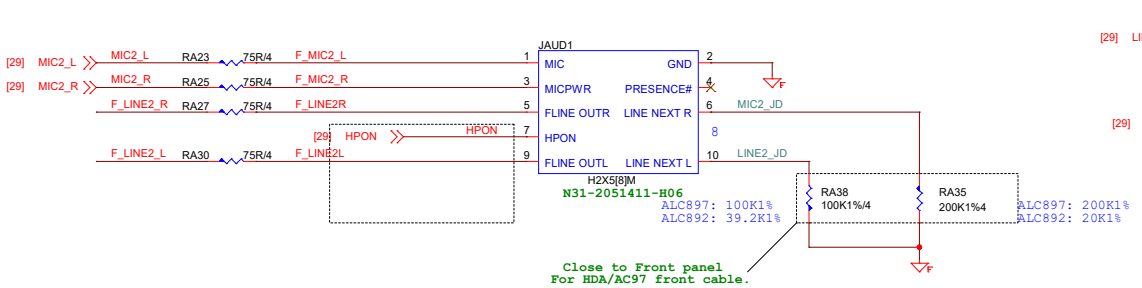
21ci203T

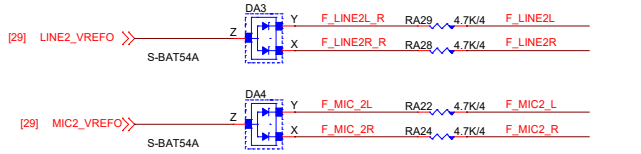
MICRO-STAR INT'L CO.,LTD

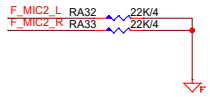
MS-7D22

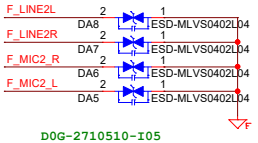
Size	Document Description	Rev
Custom	AUDIO-ALC897	10

Date: Friday, December 18, 2020 Sheet 29 of 67







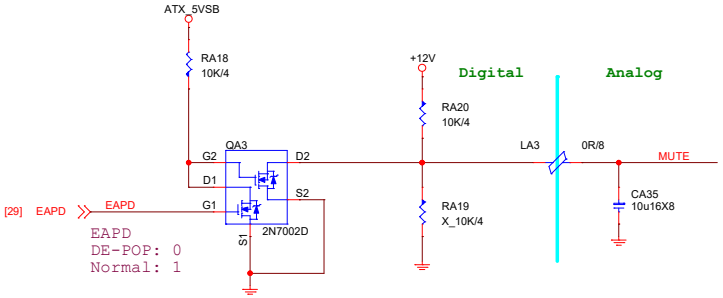


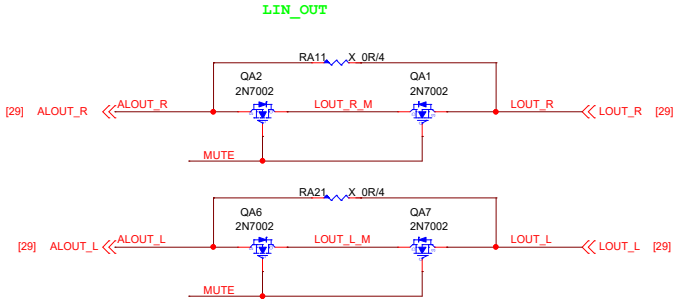
D0G-2710510-I05
Close to Front panel

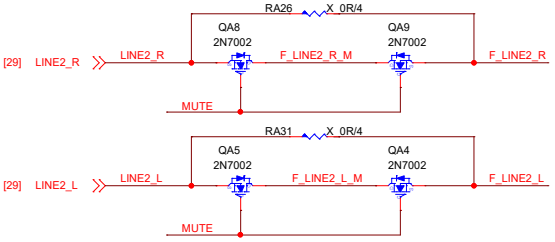
ESD protect

D0G-2710510-I05
AVL:D0G-2950500-SI0

De-POP circuit

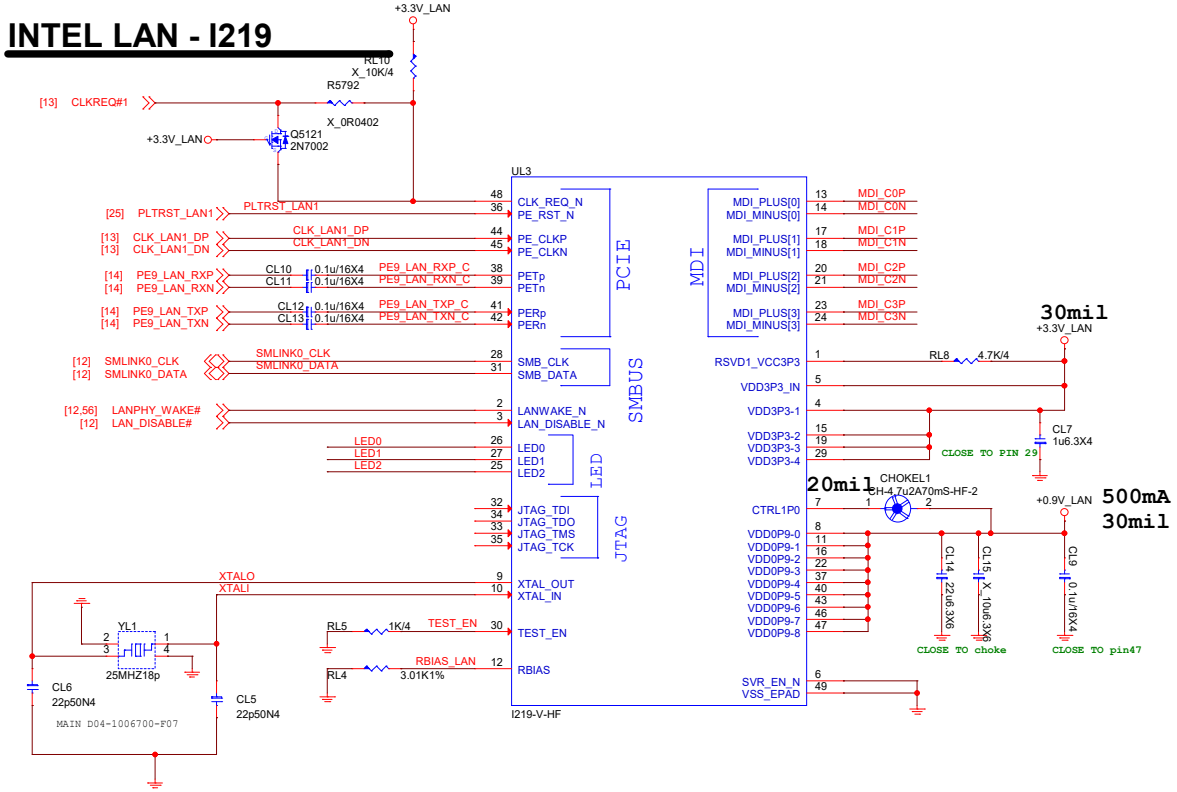




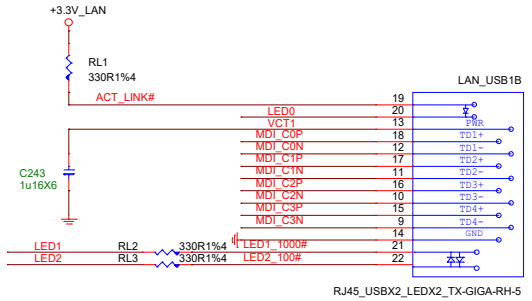


MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: AUDIO-ALC897
Rev: 10	
Date: Friday, December 18, 2020	Sheet 30 of 67

INTEL LAN - I219

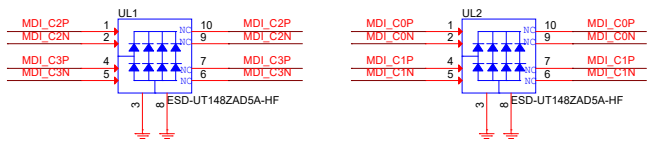


LAN Connector

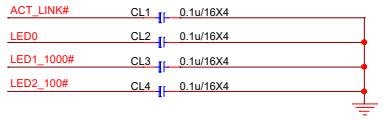


ESD Protect

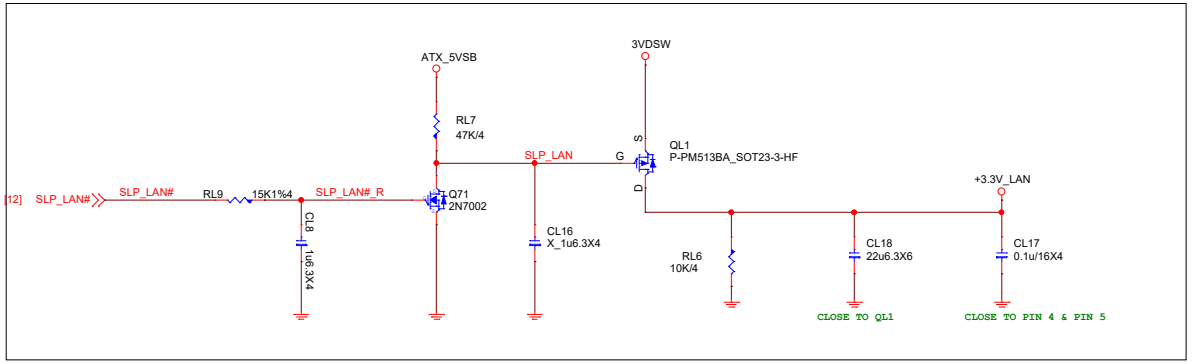
UL1 & UL2 close to connector



For EMI



support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



MICRO-STAR INT'L CO.,LTD

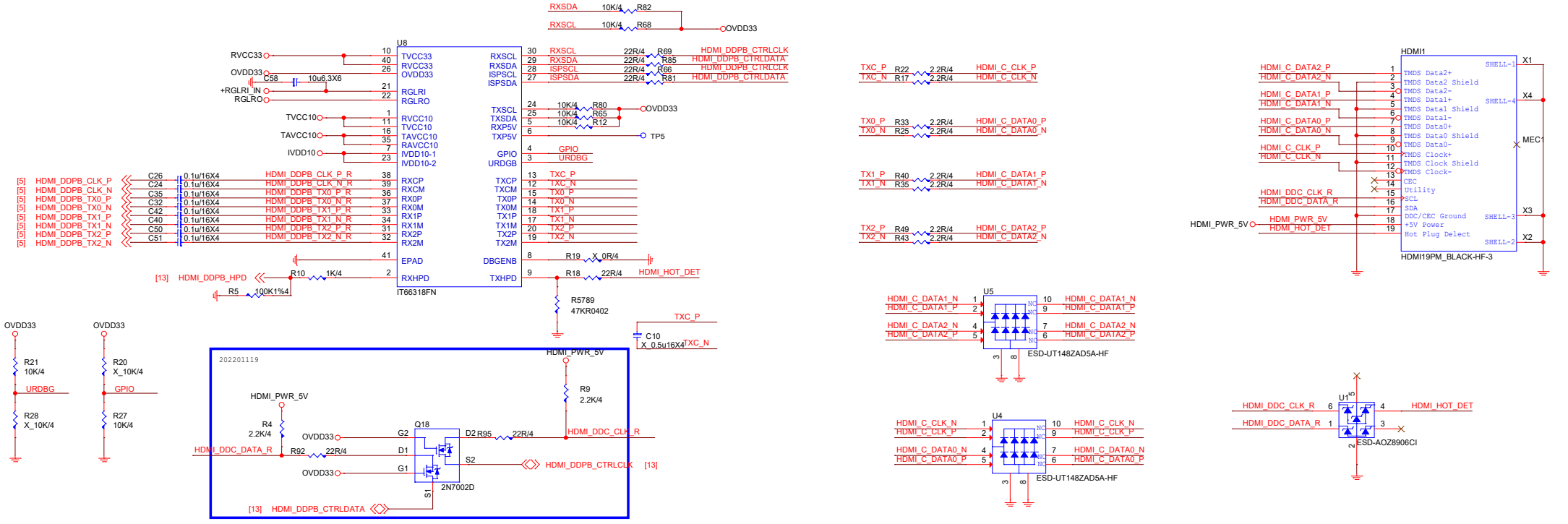
MS-7D22

Size	Document Description	Rev
Custom	RTL8125B	10

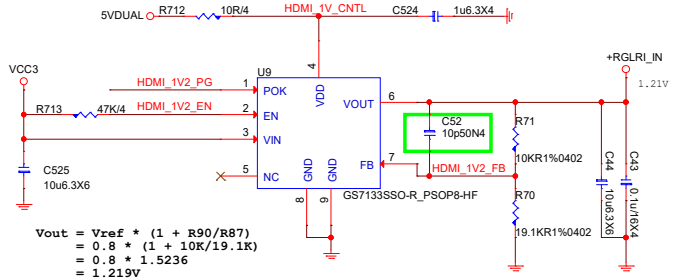
Date: Friday, December 18, 2020 Sheet 31 of 67

HDMI 2.0

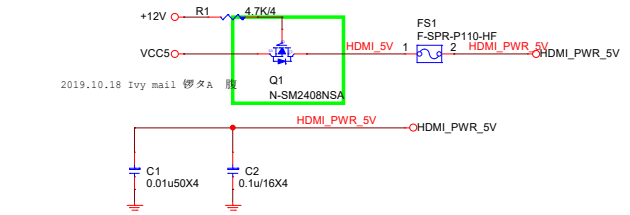
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



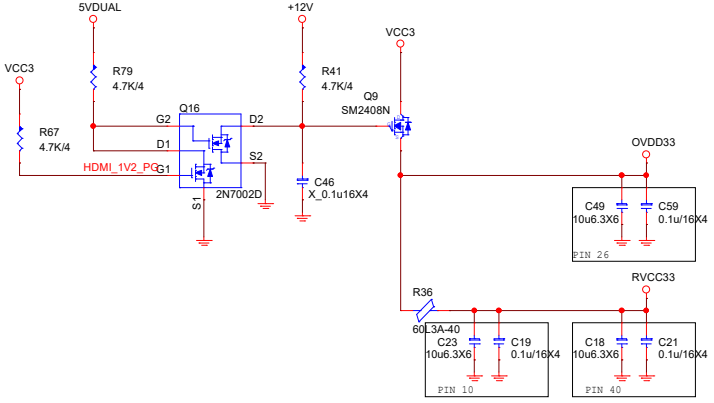
HDMI 1.2V



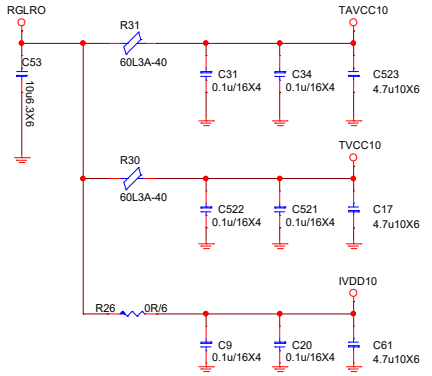
HDMI 5V



HDMI 3.3V



HDMI 1V



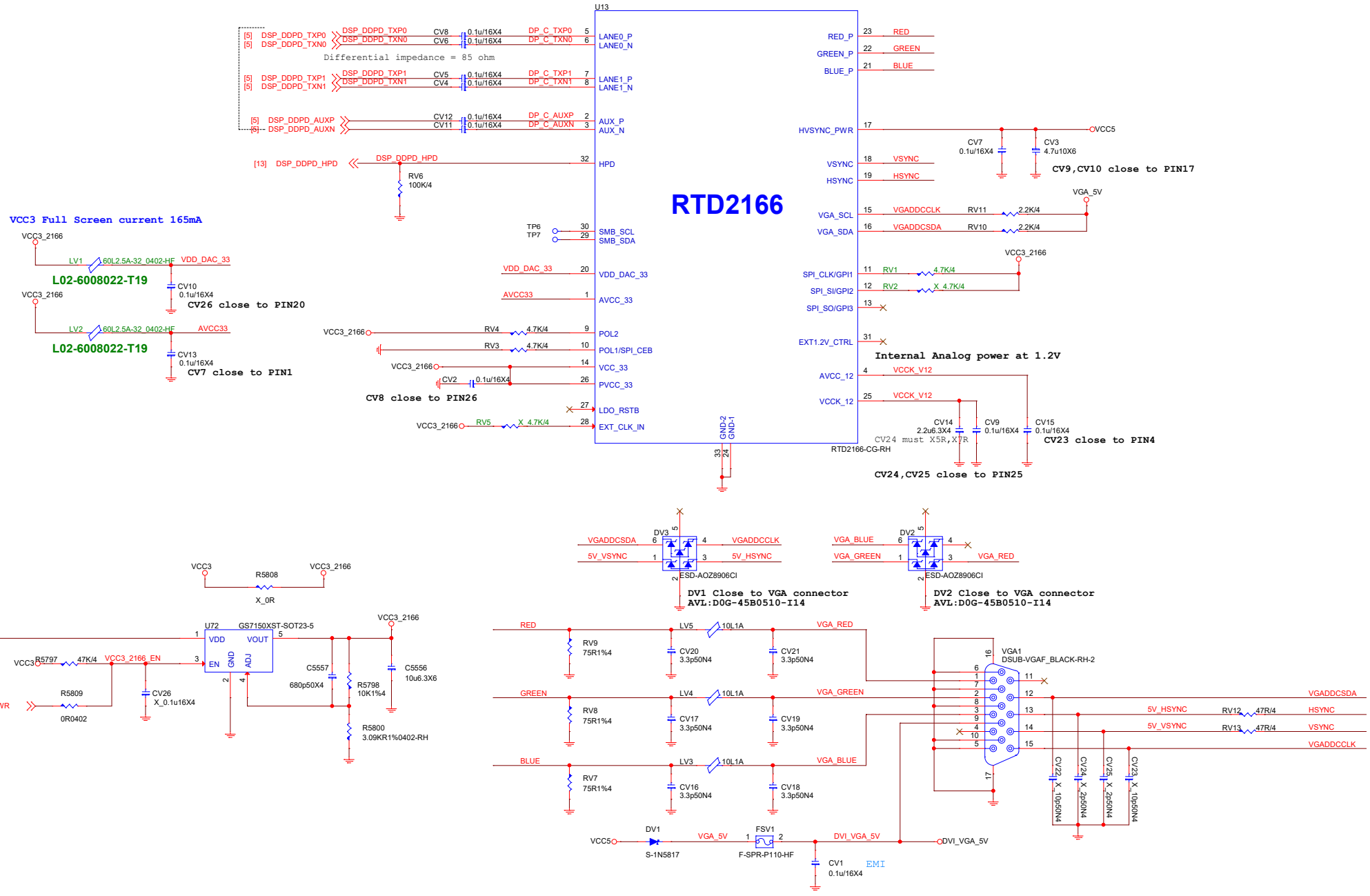
MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	HDMI Connector	10

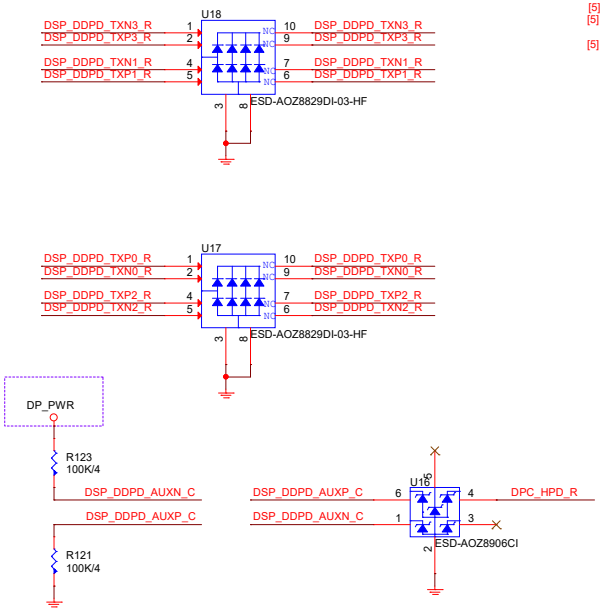
Date: Friday, December 18, 2020 Sheet 32 of 67

Note: If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

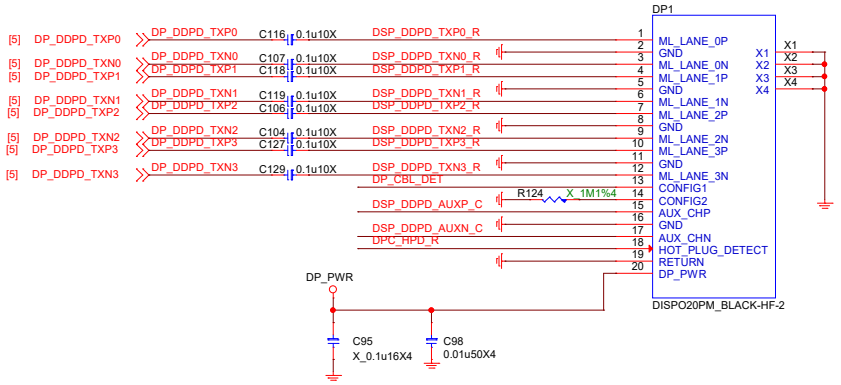


MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: DP Connector
Rev: 10	
Date: Friday, December 18, 2020	Sheet 33 of 67

ESD

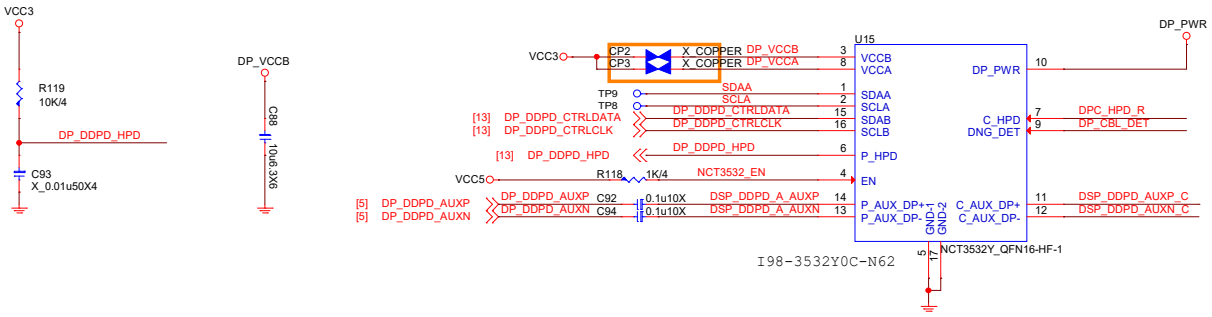


DP



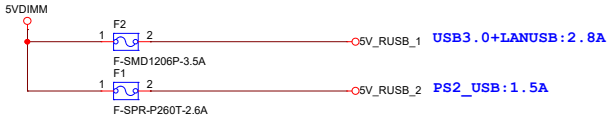
R82 (SharkBay CRB Rev0p70 have the resistor)

DP_VCCB trace don't less than 30 mil

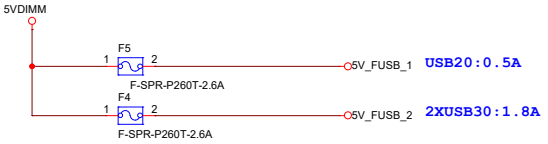


MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: DP Connector	Rev: 0A
Date: Friday, December 18, 2020	Sheet 34 of 67	

REAR USB PORT POWER



FRONT USB PORT POWER

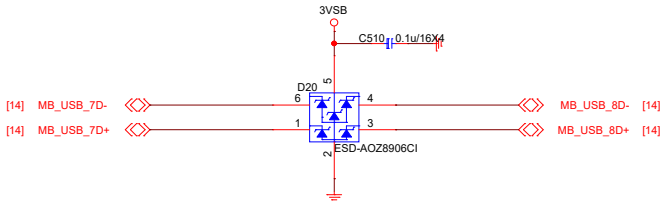


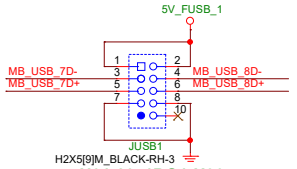
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: USB Power	Rev: 10
Date: Friday, December 18, 2020	Sheet 35 of 67	

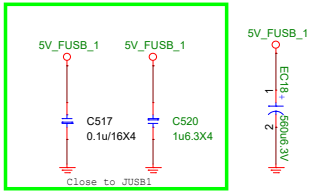
Front USB2.0

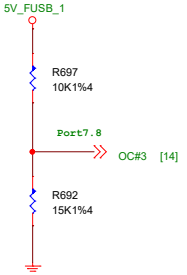
USB2.0 Port9.10

2A



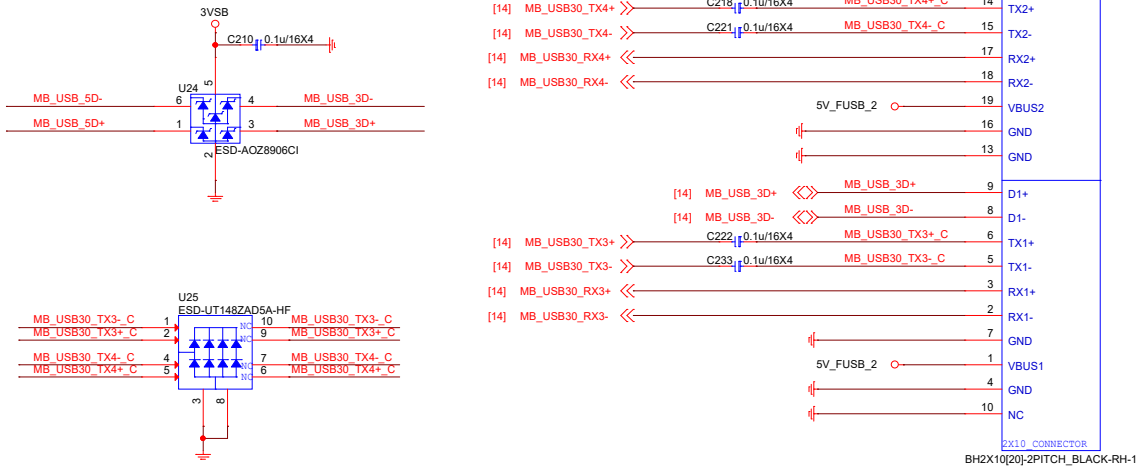






MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: XXX	Rev: 10
Date: Friday, December 18, 2020	Sheet 36 of 67	

Front USB3.1 Gen1

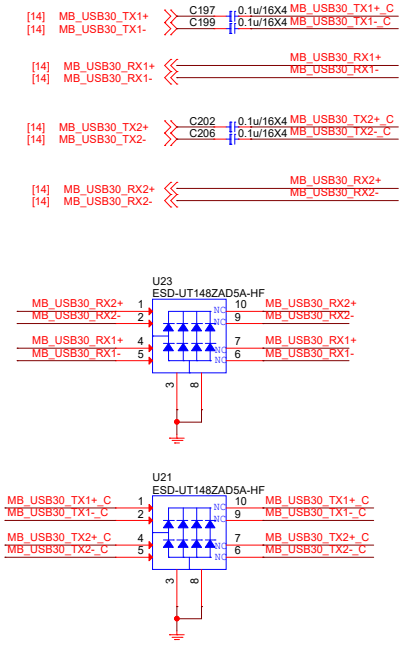


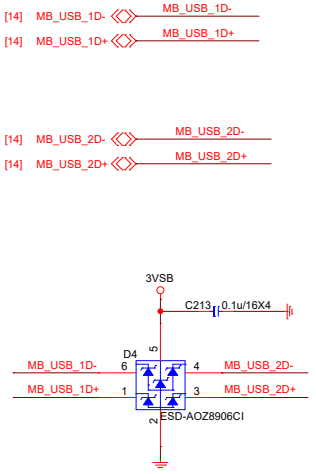
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: Front USB30	Rev: 10
Date: Friday, December 18, 2020	Sheet 37 of 67	

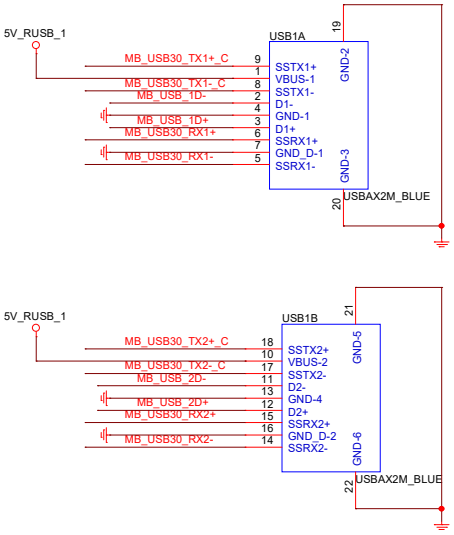
Rear USB3.0

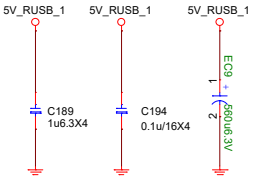
USB3.0 Port1.2
USB2.0 Port1.2

1.8A







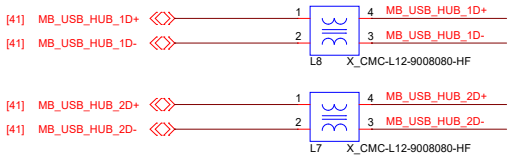


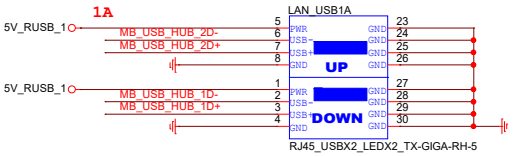
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: XXX	Rev: 10
Date: Friday, December 18, 2020	Sheet 38 of 67	

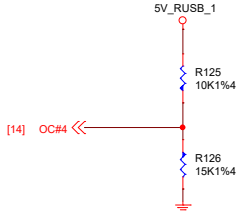
Rear lan USB2.0

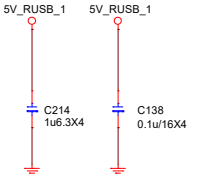
1A

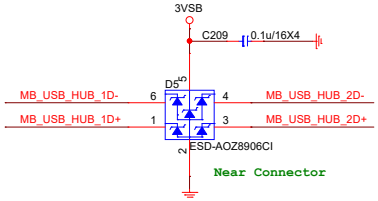
JUSB1 HUB 1 . 2











21ci203T

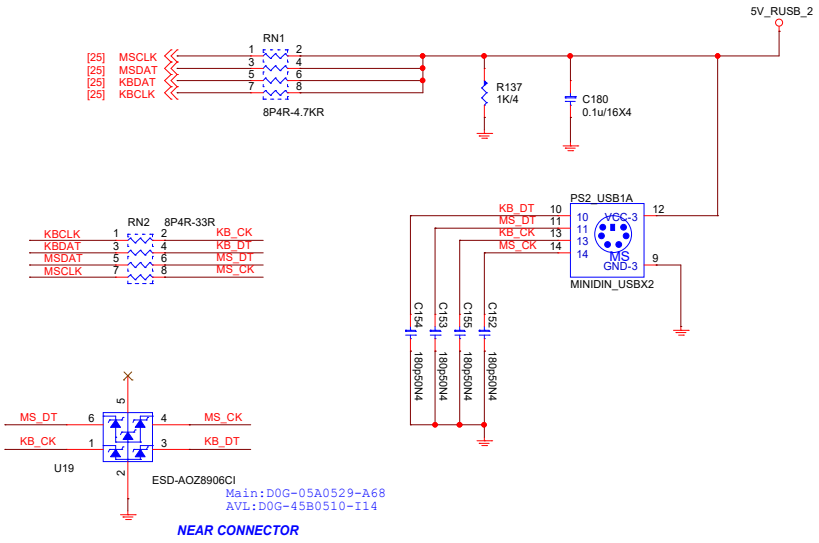
MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	Real LAN USB3.1/PS2	10

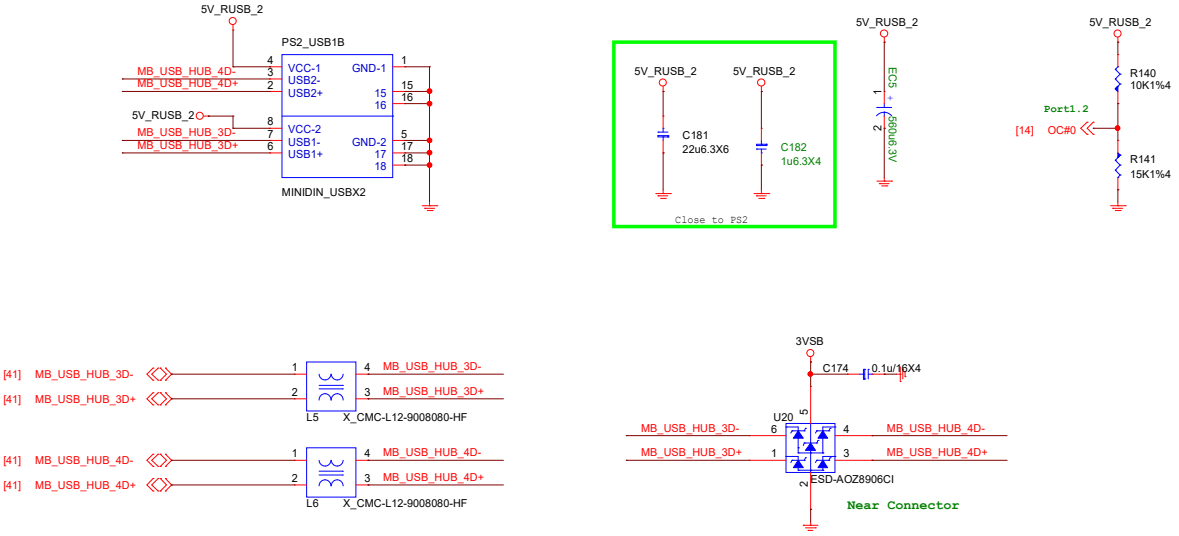
Date: Friday, December 18, 2020 Sheet 39 of 67

PS2 Connector



PS2 USB Connector

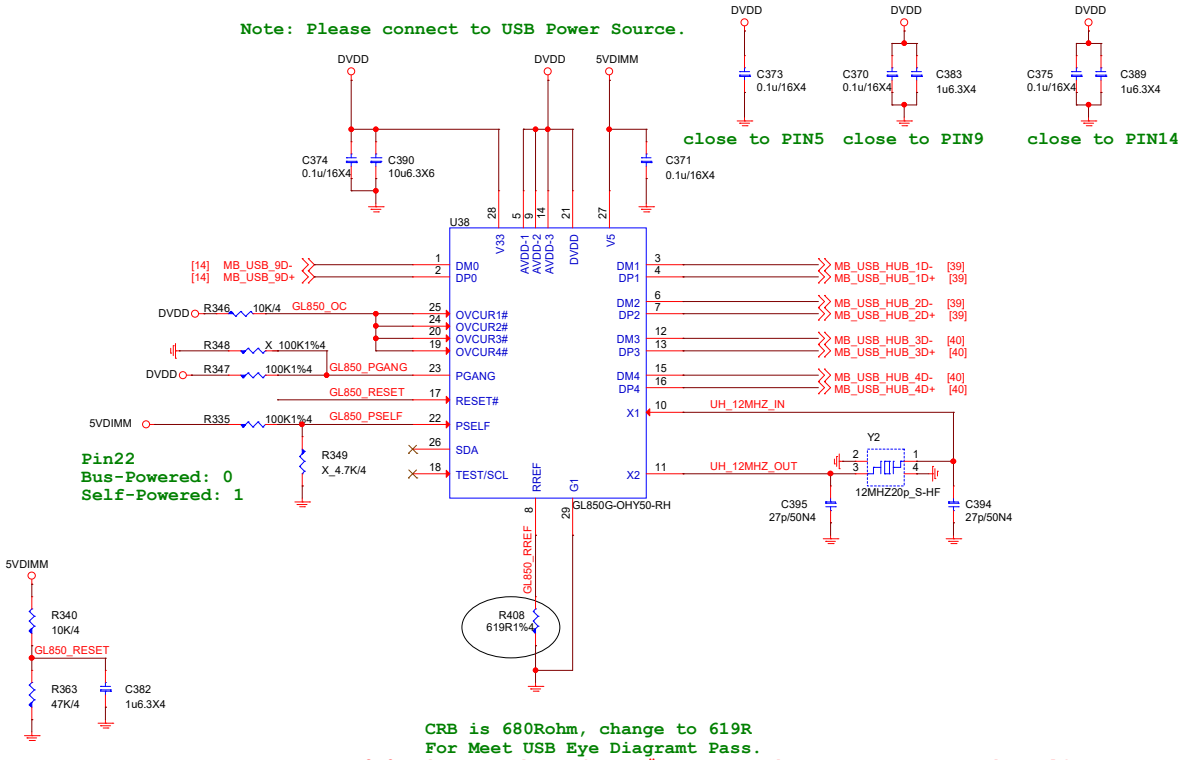
JUSB2 HUB 3.4



MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: Rear PS2+USB
Rev: 10	
Date: Friday, December 18, 2020	Sheet 40 of 67

Rear USB2.0 HUB

Note: Please connect to USB Power Source.



Pin23
Gang input:1
Individual input:0

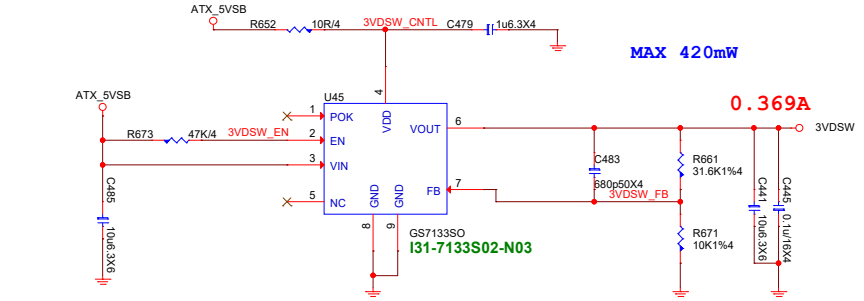
Pin22
Bus-Powered: 0
Self-Powered: 1

CRB is 680Rohm, change to 619R
For Meet USB Eye Diagramt Pass.

Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

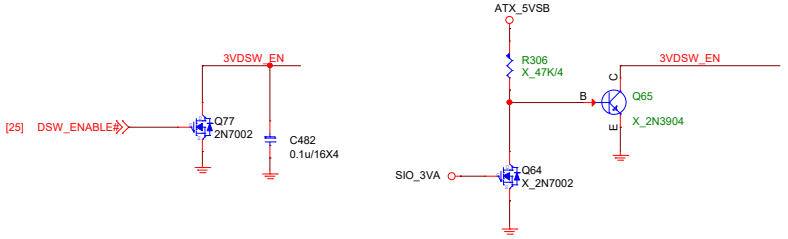
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: GL850	Rev: 10
Date: Friday, December 18, 2020	Sheet 41 of 67	

3VDSW



Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.369
=1.7*0.369
=0.6273W > 0.42W

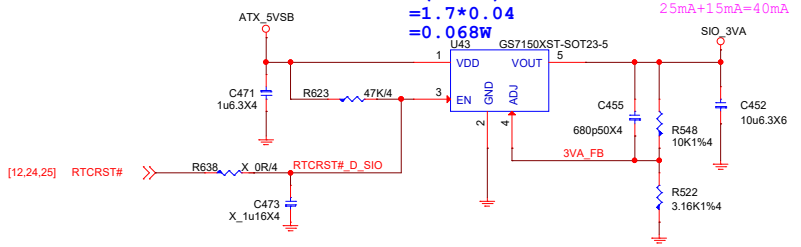
Change R661/R671 VALUE



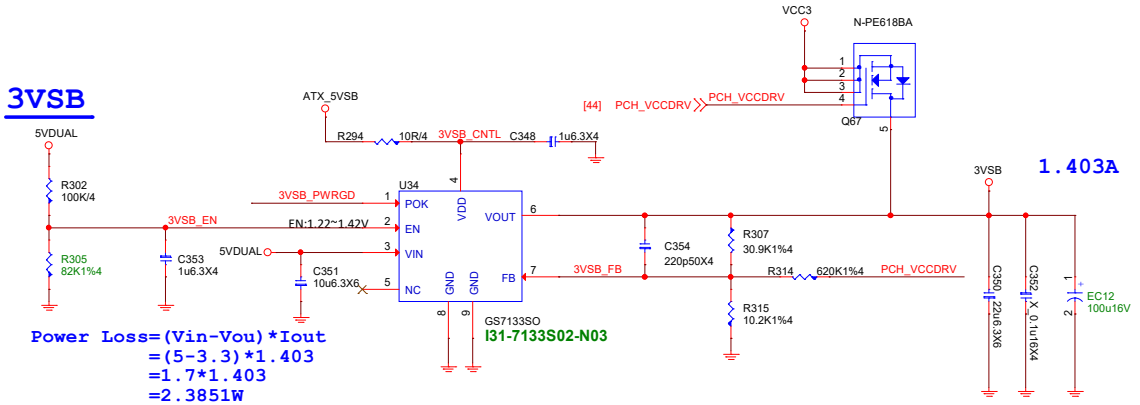
SIO_3VA

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.04
=1.7*0.04
=0.068W

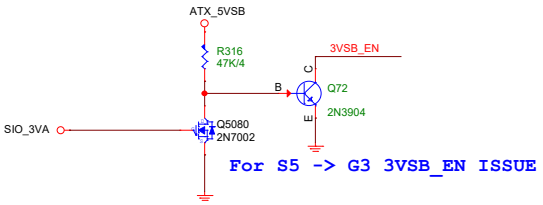
25mA+15mA=40mA



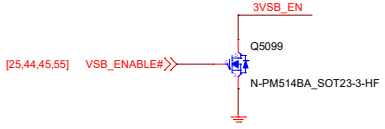
3VSB



Power Loss=(Vin-Vou)*Iout
=(5-3.3)*1.403
=1.7*1.403
=2.3851W



For S5 -> G3 3VSB_EN ISSUE



MICRO-STAR INT'L CO.,LTD

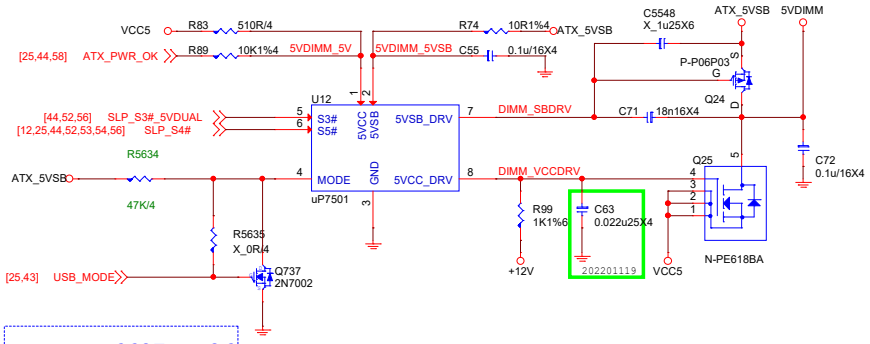
MS-7D22

Size	Document Description	Rev
Custom	ACPI	10

Date: Friday, December 18, 2020 Sheet 42 of 67

5VDIMM FOR DDR

10.98A



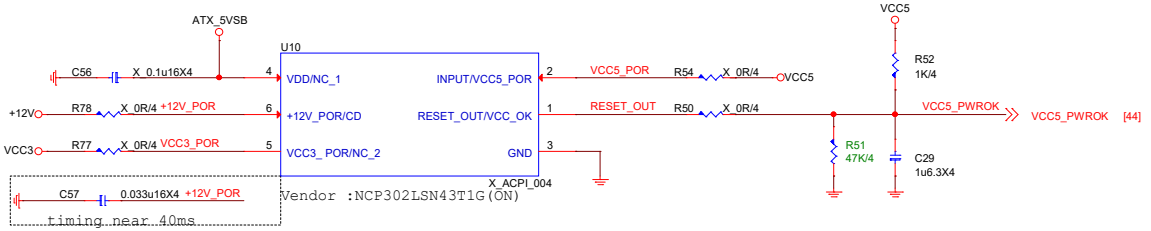
TO:NCT6687 GP86

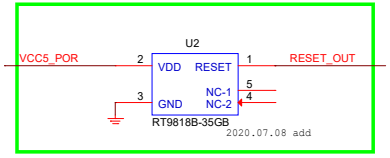
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

DIMM_SBDRV R109 X_0R/4 5VSBDRV2

DIMM_VCCDRV R94 X_0R/4 5VDRV2

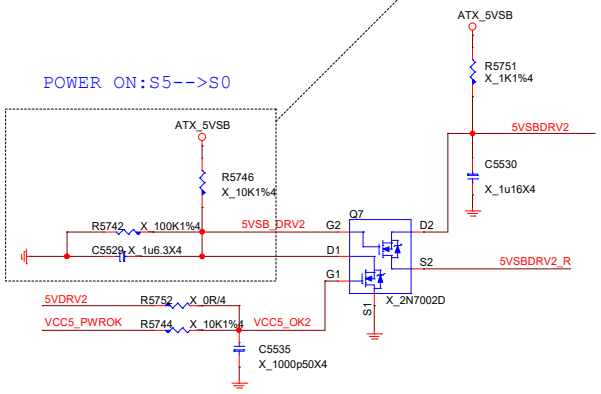
5VDIMM COLAY

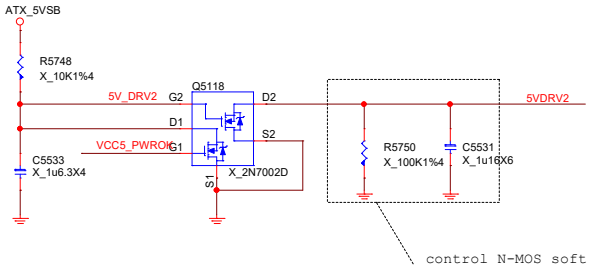


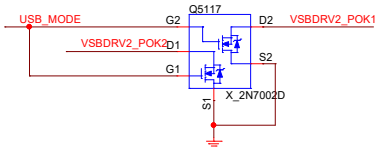


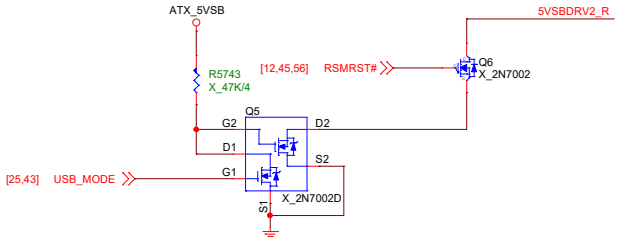
control P-MOS soft start and waiting ATX_5VSB ramp to 100%

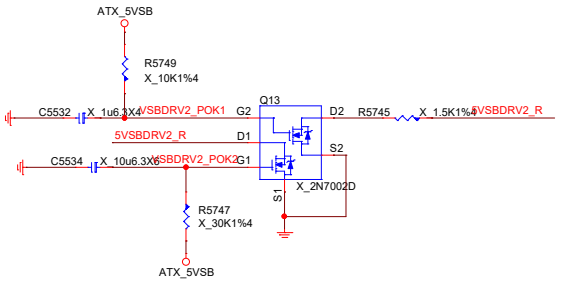
POWER ON:S5-->S0



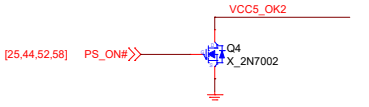








POWER OFF:S0-->S5



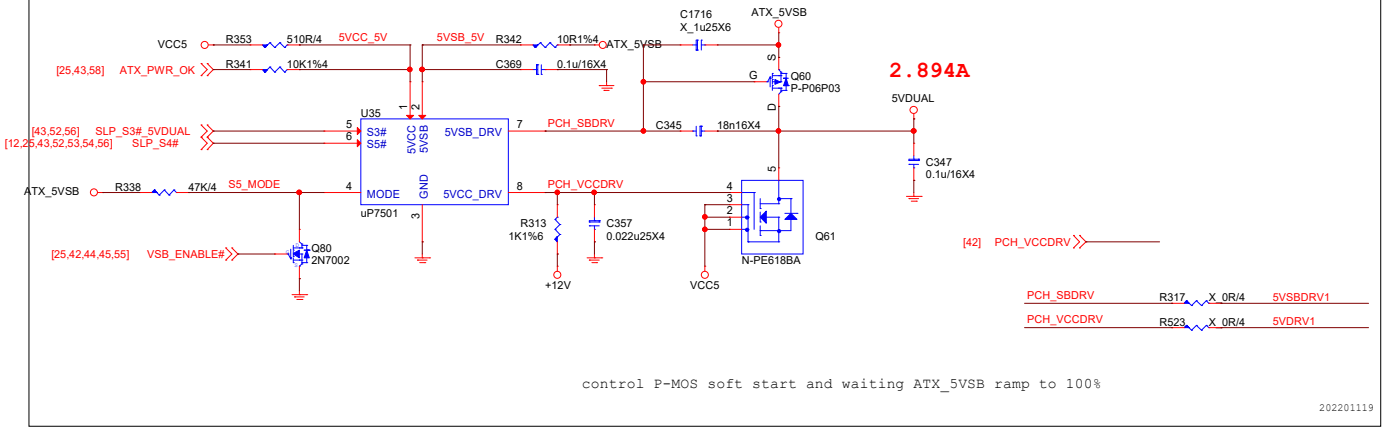
MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	ACPI	10

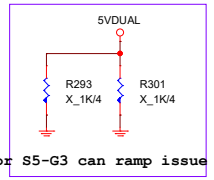
Date: Friday, December 18, 2020 Sheet 43 of 67

5VDUAL



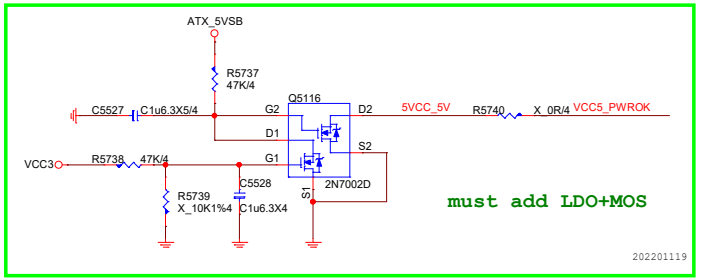
control P-MOS soft start and waiting ATX_5VSB ramp to 100%

202201119



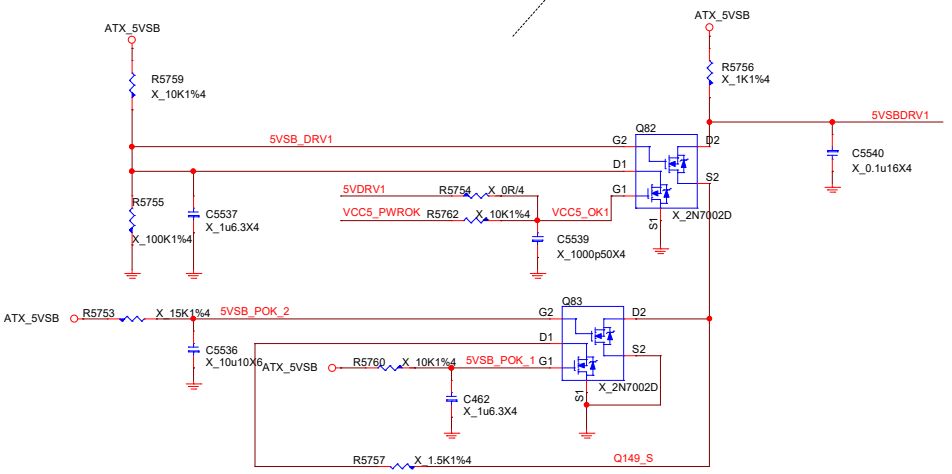
For S5-G3 can ramp issue

200302:un-stuff R419&R420

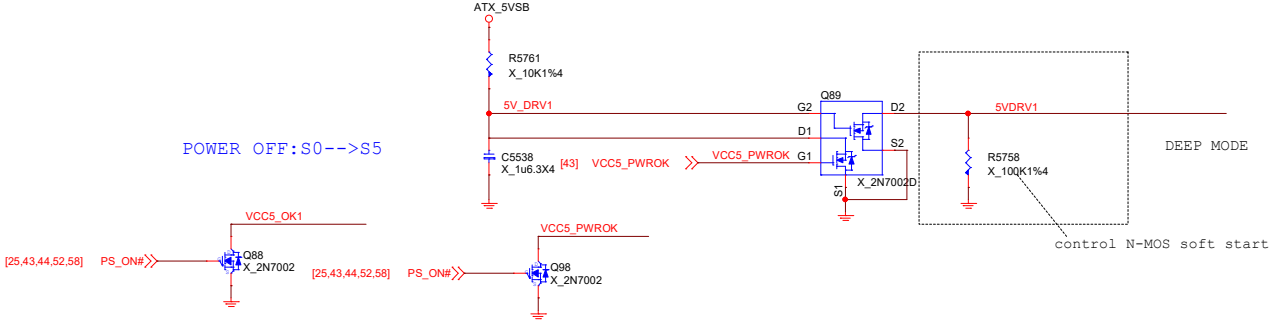


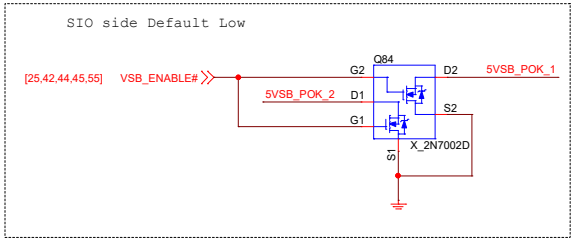
202201119

POWER ON:S5-->S0



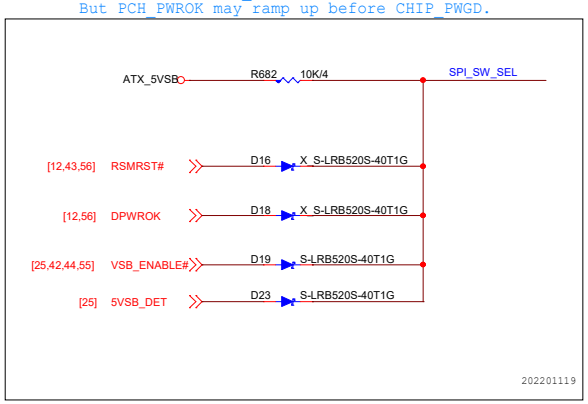
POWER OFF:S0-->S5





MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: ACPI	Rev: 10
Date: Friday, December 18, 2020	Sheet 44 of 67	

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



For TL624-1.
DEEP Mode : Stuff D48/R2517
DSW Mode : Stuff D48/D49/R2517

[12] PCH_SPI_CS0# → PCH_SPI_CS0#
[12] PCH_SPI_CLK → PCH_SPI_CLK
[12,18] PCH_SPI_MISO → PCH_SPI_MISO
[12,18] PCH_SPI_MOSI → PCH_SPI_MOSI
[12,18] PCH_SPI_IO2 → PCH_SPI_IO2
[12,18] PCH_SPI_IO3 → PCH_SPI_IO3

VSB_SPI
PCH_1P8_VSB — R683 0R/4
3VSB — R675 X_0R/4

VSB_SPI
0.1u/16X4 C486
For EMI

For SPI TPM USE

JTPM1 (H2X6[10]M-2PITCH_BLACK)
PCH_SPI_MISO R665 X_R/2 TPM_MISO
PCH_SPI_CS0#
SPI_SW_SEL
PCH_SPI_IO2 R660 X_R/2 TPM_IO2
TPM_SPI_CS2# R654 X_R/2 PCH_SPI_CS2# [12]
TPM_MOSI R655 X_R/2 PCH_SPI_MOSI
TPM_CLK R656 X_R/2 PCH_SPI_CLK
TPM_RST# TPM_RST# [25]
TPM_SPI_PIRQ# R672 X_R/2 GPP_E7 [15]

D13 ESD-AOZ8131DI — C493 0.1u/16X4
Close to JSPI1

D29 ESD-AOZ8131DI
Close to JSPI1

R662 X_R/2

VSB_SPI
R648 X_2.2K/4

PCH_SPI_CS#
PCH_SPI_MISO R651 33R/4 SPI1_MISO
PCH_SPI_IO2 R620 33R/4 SPI1_IO2

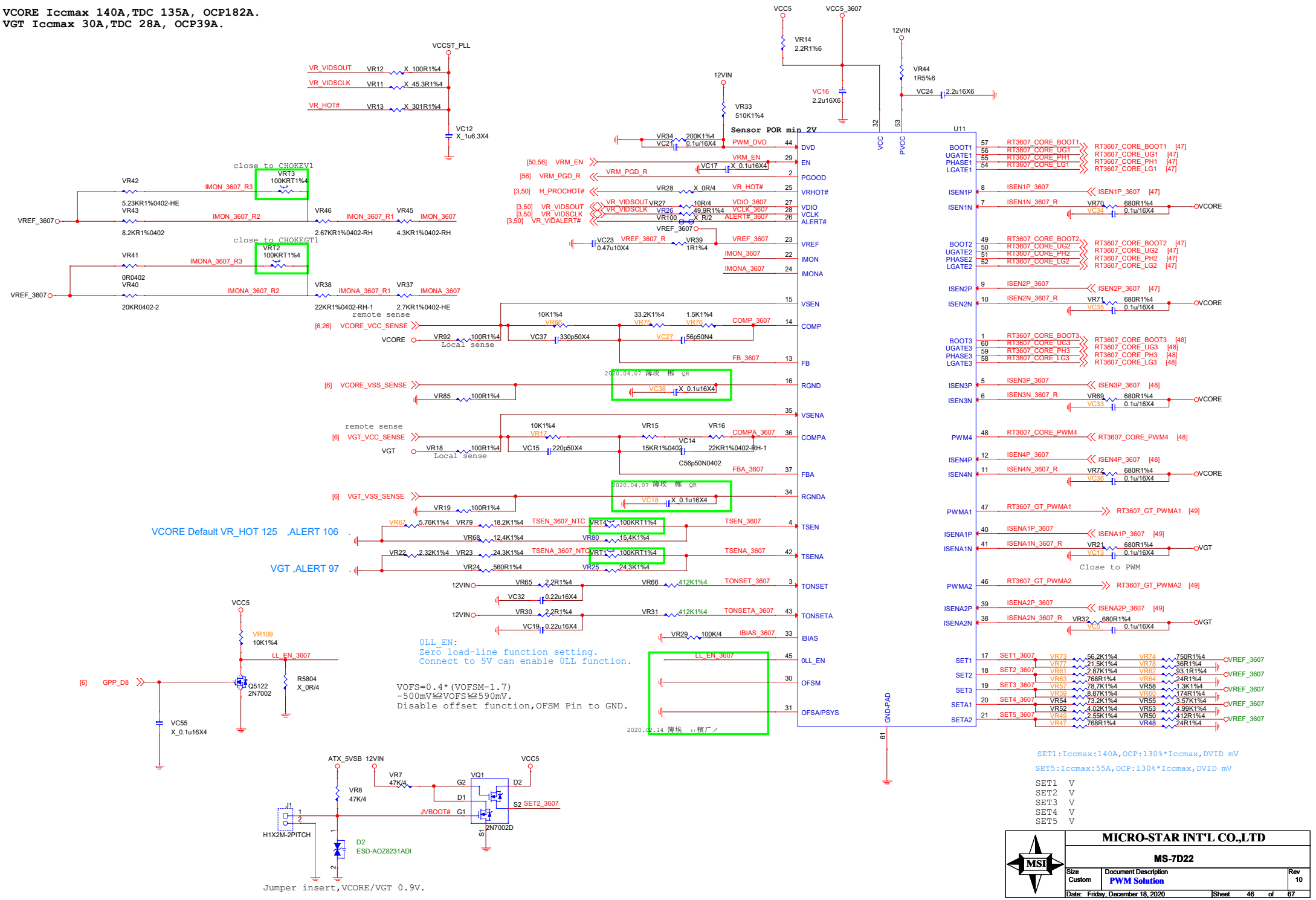
SPI1
CS
SO/SIO1
SIO2
GND
VCC
SIO3
SCLK
SI/SIO0
NC
N14_SPI_SP

VSB_SPI
C481 0.1u/16X4
C491 10u6.3X6
SPI1_IO3 R657 33R/4 PCH_SPI_IO3
SPI1_CLK R616 33R/4 PCH_SPI_CLK
SPI1_MOSI R596 33R/4 PCH_SPI_MOSI

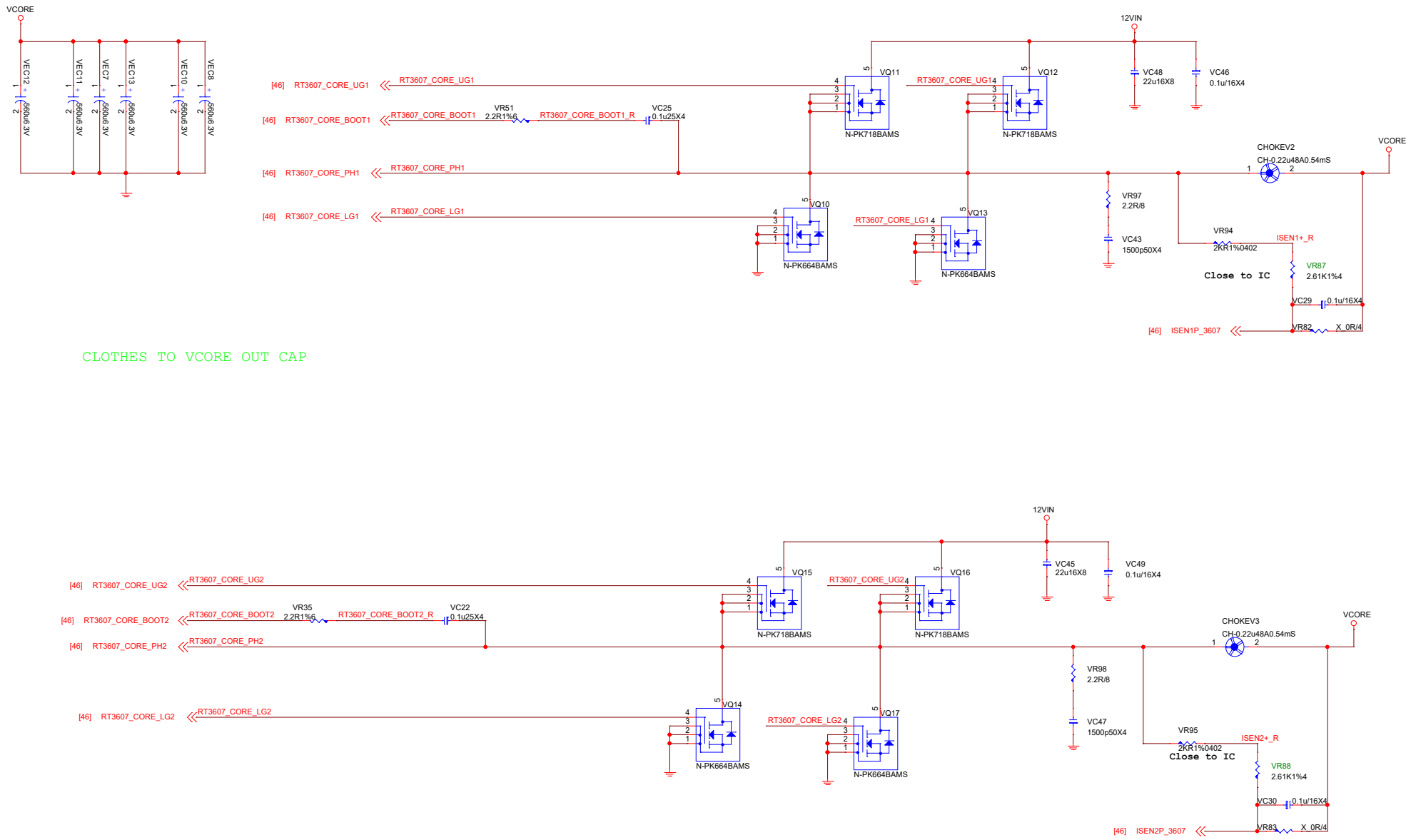
M31-2567300-M24
256MB SPI ROM

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: BIOS ROM	Rev: 10
Date: Friday, December 18, 2020	Sheet 45 of 67	

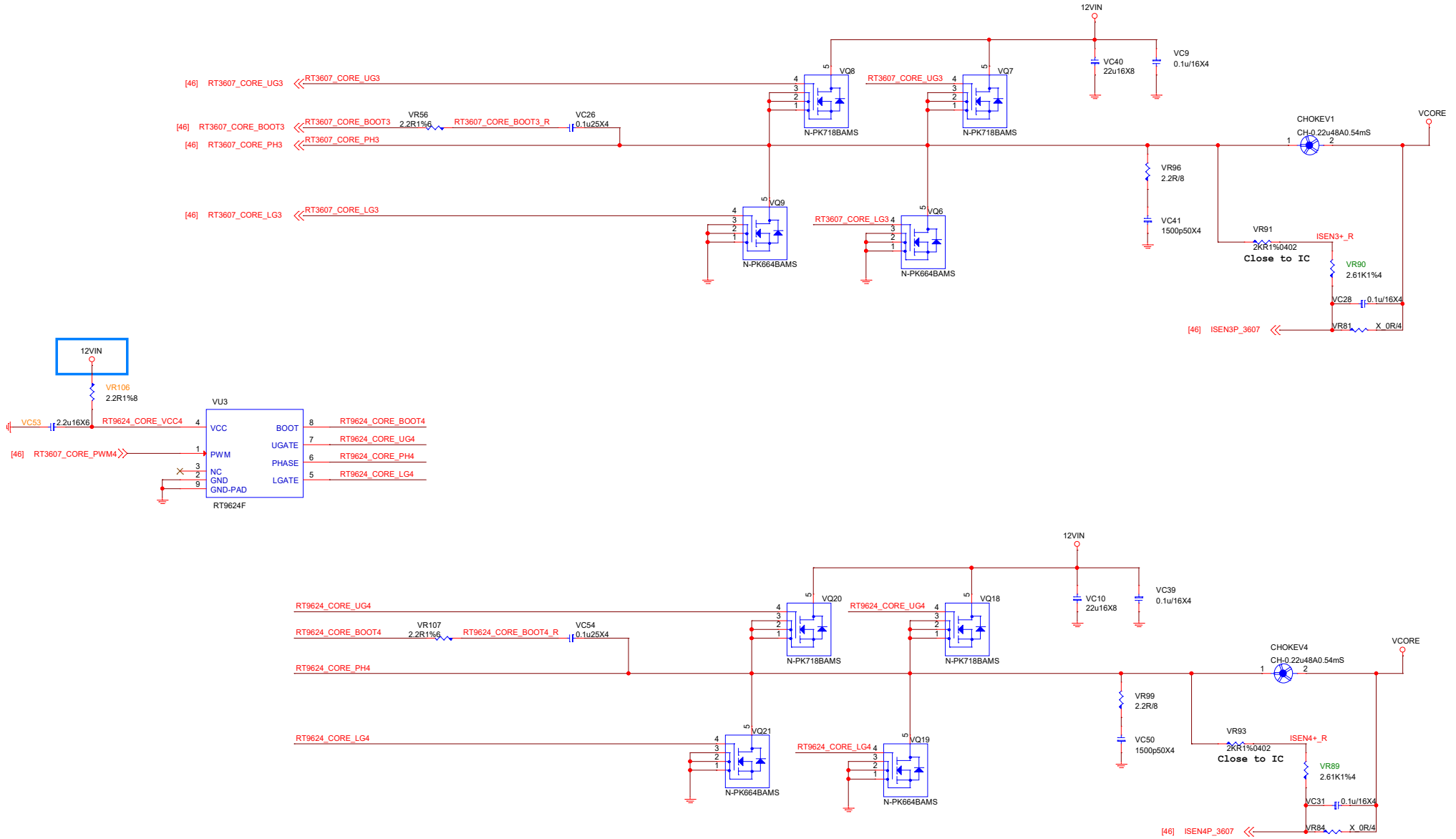
VCORE Iccmax 140A,TDC 135A, OCP182A.
VGT Iccmax 30A,TDC 28A, OCP39A.



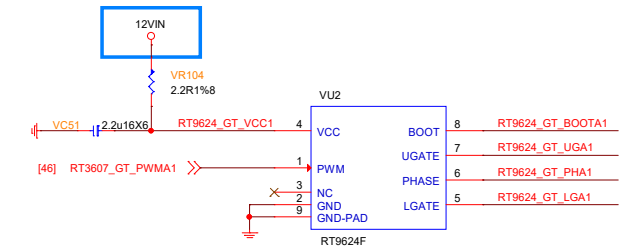
MICRO-STAR INT'L CO.,LTD	
MS-7D22	
Size: Custom	Document Description: PWM Solution
Rev: 10	
Date: Friday, December 18, 2020	Sheet 46 of 67

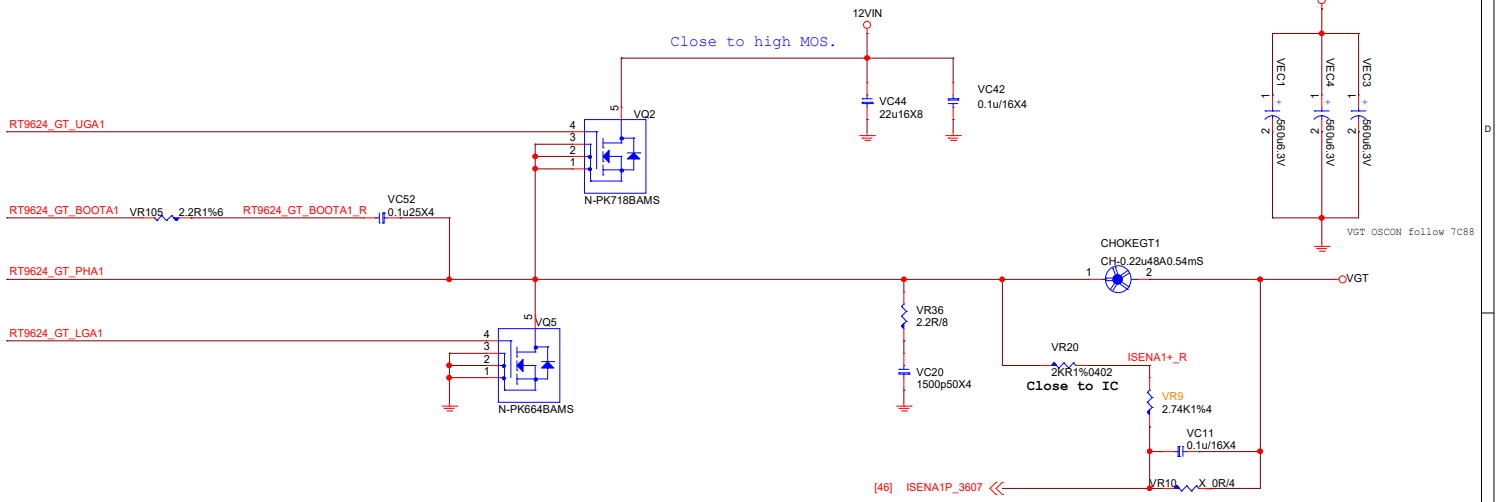


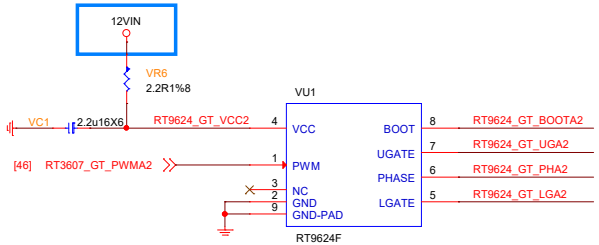
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: VCORE MOS-PHASE 1~2	Rev: 10
Date: Friday, December 18, 2020	Sheet 47 of 67	

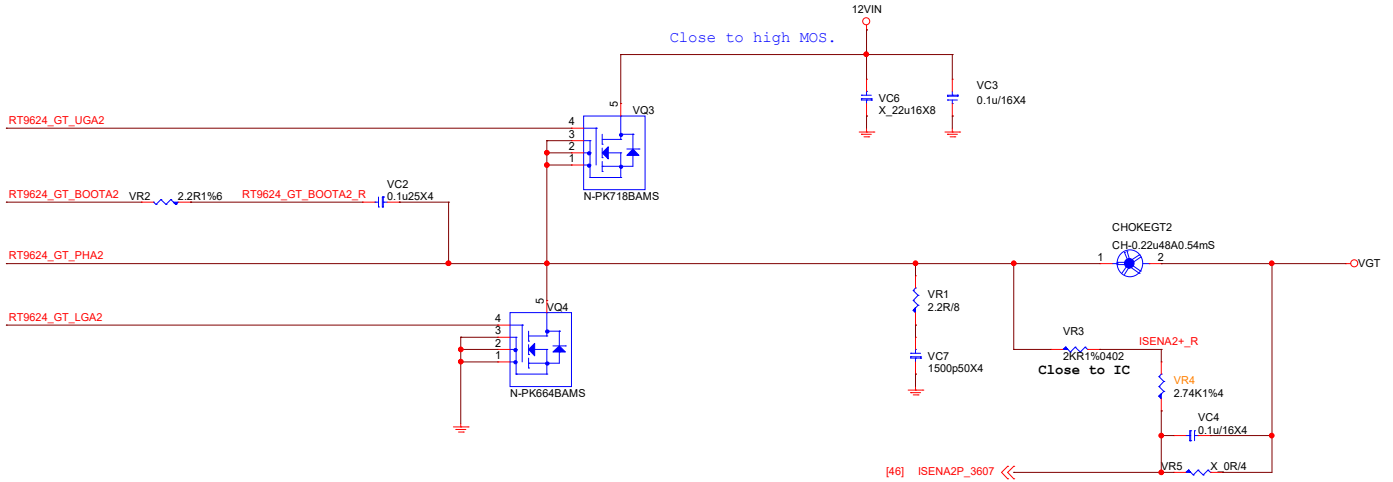


MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: VCORE MOS-PHASE 3~4	Rev: 10
Date: Friday, December 18, 2020	Sheet 48 of 67	

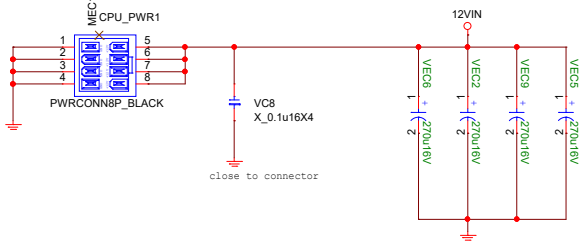








12VIN CONNECTOR



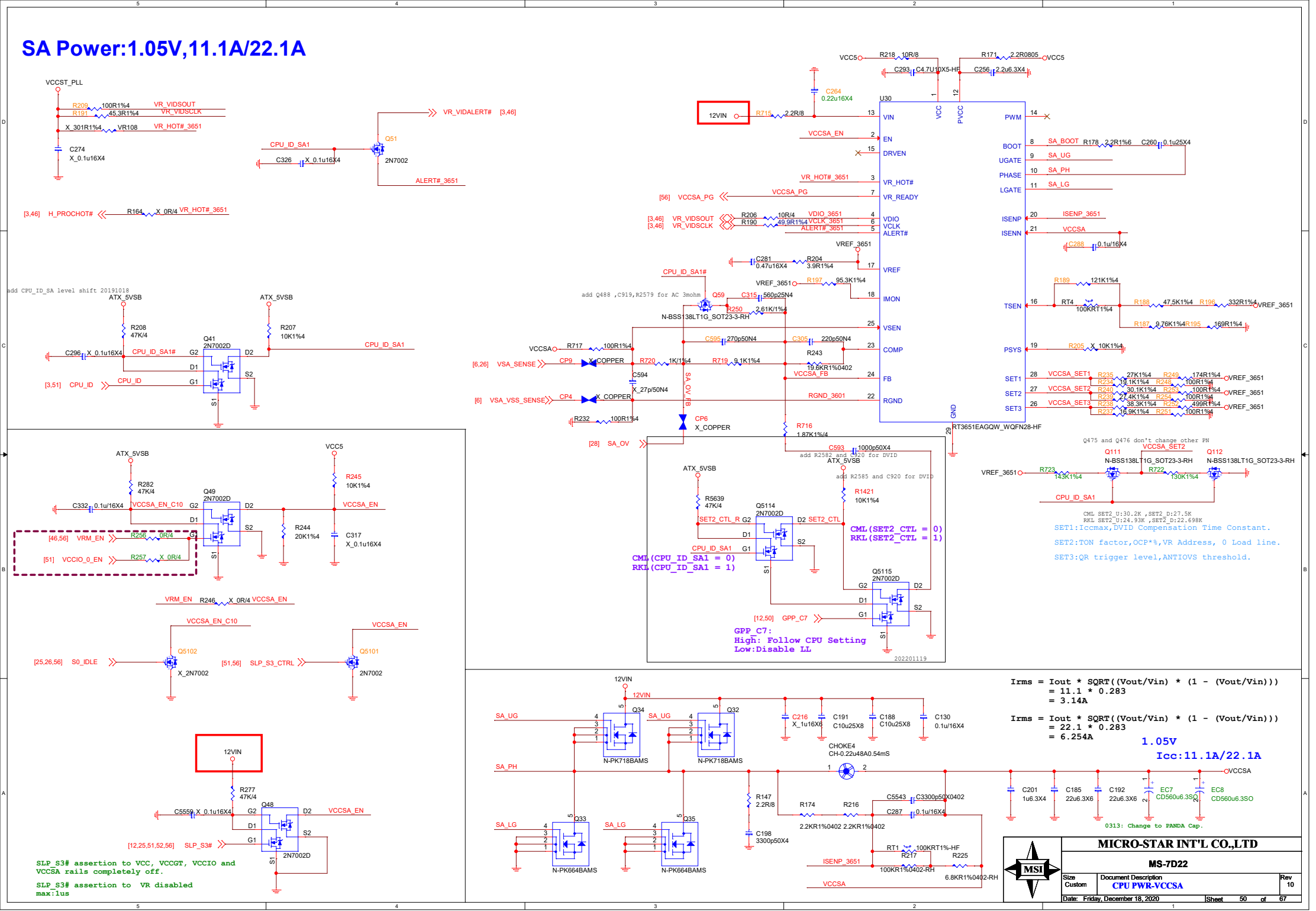
MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	VGT MOS-PHASE 1~2	10

Date: Friday, December 18, 2020 Sheet 49 of 67

SA Power:1.05V,11.1A/22.1A



MICRO-STAR INT'L CO.,LTD

MS-7D22

Size	Document Description	Rev
Custom	CPU PWR-VCCSA	10

Date: Friday, December 18, 2020 Sheet 50 of 67

VCCIO Power 0.95,6.4A

1.05,16.5A

CHOKE13 — +12V → +12V_VCCIO; C312 0.1u/16X4; CH-0.24u4.2A22mS-HF

Irms1 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6.4 * 0.27
= 1.728A

+12V_VCCIO: C300 C10u25X8, C299 C10u25X8, C279 0.1u/16X4

UIO2 AOZ2263AQI-10

R5766 75KR1%0402; R5767 1R1%; C5542 C4.7u16X5-HF; VCC5

TON, VCC, PGOOD, EN, PFM#, SS, BST, LX-1(10-11), LX-3, LX-4, LX-5, FB, AGND, PGND-1, PGND-2, PGND-3, PGND-4, PGND-5; IN(7-9)

VCCIO_0_PG, VCCIO_0_EN, VCCIO_0_PFM#, VCCIO_0_BOOT1, VCCIO_0_PH1, VCCIO_0_FB

C263 C0.01u50X0402-HF; C265 0.1u25X4

CHOKE7 — CH-0.68u15A5mS-HF-1

VCCIO_0; R227 10R1%4; VCCIO_0_SENSE [6,26]

FB:0.6V

C278 C1000p16X0402-RH; R202 1K1%4; R214 5.1KR1%0402; CP10 X_COPPER

Vout = Vref * (1 + R202/R214)
= 0.6 * (1 + 1K/1.74K)
= 0.6 * 1.5747
= 0.9448V

0.95V Icc:6.4A

from NCT3933 [28] VCCIO_0_OV

VCCIO_0_PH1 R168 X 2.2R/8 C255 X 3300p50X4 reserve snubber

C5514 0.1u/16X4; C5513 0.1u/16X4; C238 0.1u/16X4; C226 22u6.3X6; C237 22u6.3X6; C229 22u6.3X6; C244 22u6.3X6

ATX_5VSB; R265 47K/4; VCC5 ???? R271 100KR4

Q46 2N7002D: G2, D2, D1, G1, S2, S1; VCCIO_0_PG [56]; VCCIO_PG_R; CPU_ID

R273 100KR4; Q47 2N7002D: VCCIO_12_PG, [3,50,51] CPU_ID; R5779 X_10KR4; VCCIO_0_PFM#; R229 100KR1%0402

Irms2 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 16.5 * 0.283
= 4.67A

+12V_VCCIO: C302 C10u25X8, C303 C10u25X8, C277 0.1u/16X4

UIO1 AOZ2263AQI-10

R5764 75KR1%0402; R5765 1R1%; C5541 C4.7u16X5-HF; VCC5

TON, VCC, PGOOD, EN, PFM#, SS, BST, LX-1(10-11), LX-3, LX-4, LX-5, FB, AGND, PGND-1, PGND-2, PGND-3, PGND-4, PGND-5; IN(7-9)

VCCIO_12_PG, VCCIO_12_EN, VCCIO_12_PFM#, VCCIO_12_BOOT1, VCCIO_12_PH1

C269 C0.01u50X0402-HF; C258 0.1u25X4

CHOKE6 — 202201119 CH-0.68u15A5mS-HF-1

VCCIO_1_2; R212 10R1%4; VCCIO_12_SENSE [6,26]

Vout = Vref * (1 + R220/R224)
= 0.6 * (1 + 1K/1.5K)
= 0.6 * 1.6667
= 1V

0V (CPU_ID = 0)
1V (CPU_ID = 1)

FB:0.6V

C280 C1000p16X0402-RH; R220 1K1%4; R224 3.9KR1%0402

FOR LAYOUT SPACE DELAY CP5

from NCT3933 [28] VCCIO_12_OV

VCCIO_12_PH1 R172 X 2.2R/8 C253 X 3300p50X4 reserve snubber

1V Icc:9.6A

C247 22u6.3X6; C230 22u6.3X6; C241 22u6.3X6; C234 22u6.3X6; C231 22u6.3X6; C239 0.1u/16X4

ATX_5VSB; R259 47K/4; +12V; R266 30KR4

Q44 2N7002D: G2, D2, D1, G1, S2, S1; VCCIO_12_EN; VCCIO_0_EN; R262 10KR4; C321 X_0.1u16X4; C318 X_0.1u16X4

R5780 X_10KR4; VCCIO_12_PFM#; R233 100KR1%0402

VCC_DDR; R114 X_10K/4; [53] DDR_PWRGD; C82 0.22u10X4

Q26 2N7002D: G2, D2, D1, G1, S2, S1; Q26_D1; R115 47K/4; VCC3; C83 1u16X4; R116 X_10K/4

0330: Follow 300 Series Update

ATX_5VSB; R117 47K/4; [50,51,56] SLP_S3_CTRL; VCCIO_0_EN; VCCIO_0_EN_G; C86 X_0.1u16X4

Q43 2N7002D: G2, D2, D1, G1, S2, S1

+12V; R260 30KR4; VCCIO_0_EN; R258 10KR4; C322 X_0.1u16X4; VCCIO_0_EN [50]

ATX_5VSB; R263 47K/4; Q45 2N7002D: G2, D2 VCCIO_0_EN, D1, G1, S2, S1; R270 22K/4; VCC5; R264 100KR4; C325 1u16X4

+12V; R255 47K/4; Q42 2N7002D: G2, D2 VCCIO_0_EN, D1, G1, S2, S1; [12,25,50,52,56] SLP_S3#

R268 8.2KR1%0402; VCCIO_0_FB; Q50 2N7002; [3,50,51] CPU_ID

VCCIO_0

0.95V (CPU_ID = 0) Vout = 0.6 * (1 + 1K/1.344K)
1.05V (CPU_ID = 1) = 0.6 * 1.744
= 1.046V

3VSB; R350 X_10K/4; [12] GPP_F22; R351 100K/4; R362 X_10K/4; VCCIO_0_FB; R310 X_5.9K1%4; [15] GPP_F23; R361 100K/4

Q74 2N7002D: G2, D2, D1, G1, S2, S1; R311 X_5.9K1%4 VCCIO_0_FB

information from PDG page686

GPP_F22	GPP_F23	CPU_ID	VCCIO_0
Low	Low	Low	0.95V
Low	Low	High	1.05V
High	Low	High	1.075V
Low	High	High	1.100V
High	High	High	1.125V

MICRO-STAR INT'L CO.,LTD

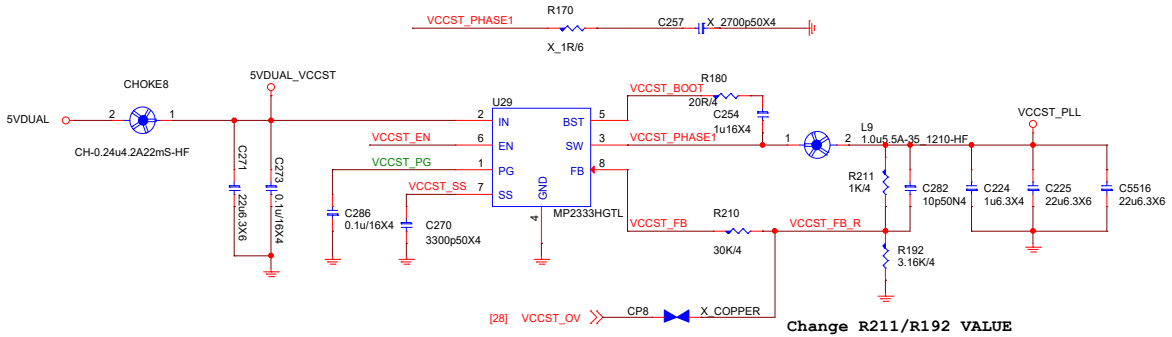
MS-7D22

Size: Custom | Document Description: CPU PWR-VCCIO | Rev: 10

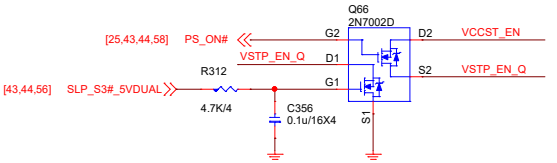
Date: Friday, December 18, 2020 | Sheet 51 of 67

VCCST

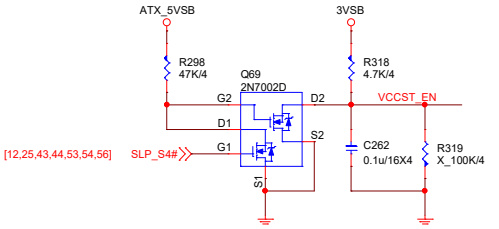
1.05V; 0.92A/2.3A



Change R211/R192 VALUE

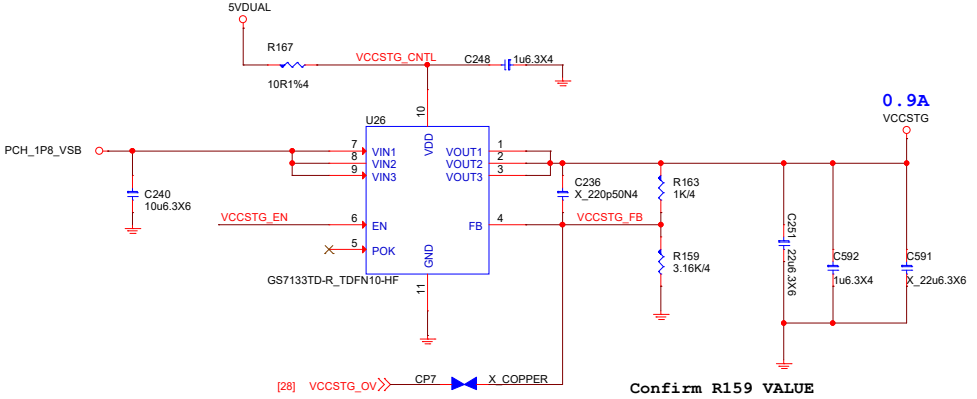


for S0ix

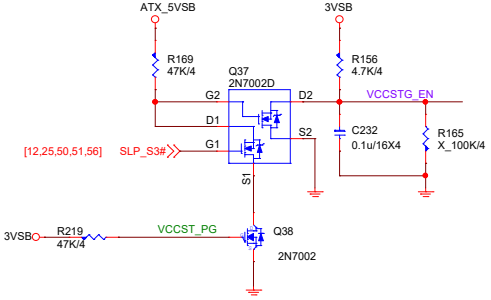


VCCSTG

1.05V; 0.2A/0.9A



Confirm R159 VALUE



Power Loss=(Vin-Vou)*Iout
=(1.8-1.05)*0.9
=0.75*0.9
=0.675W < 1.33W

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: CPU PWR-VCCST/PLL	Rev: 10
Date: Friday, December 18, 2020	Sheet 52 of 67	

DDR4 Power:1.2V,8.77A

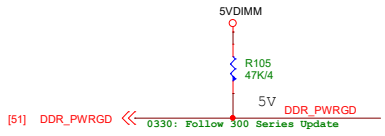
3.7A For CPU
0.225A For CPU(VCCSTPLL)
4.6A For 2DIMM
0.375A For DDR VTT

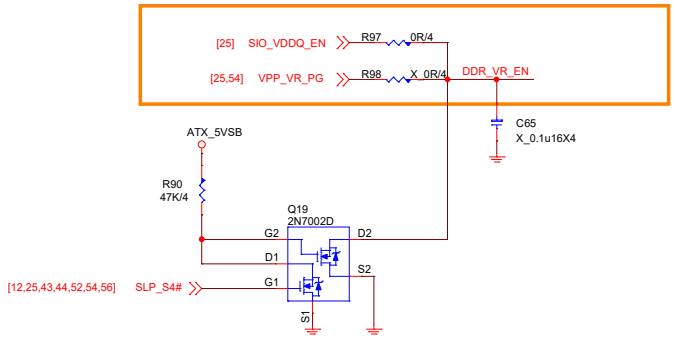
OCP = 12.5~16.6A; Choke Isat=32A

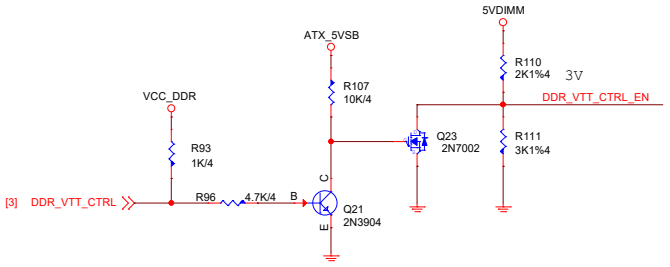
*Rlimit = Llimit * Rds * 10 /5uA*
*= 15.8*3.9*10/5 = 123.24K*

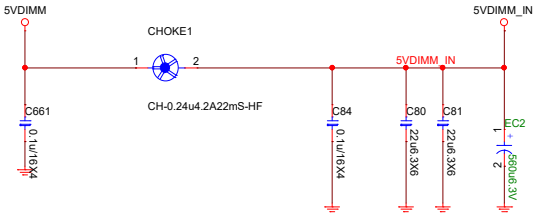
*0.4V<=Rlimit *5uA<=3V*
*123.24*0.005=0.6162*

D03-4503N0C-ST8
*Current limit= 124K*5uA/10/5.1mohm)=12.16A*
*Current limit= 124K*5uA/10/3.9mohm)=15.9A*

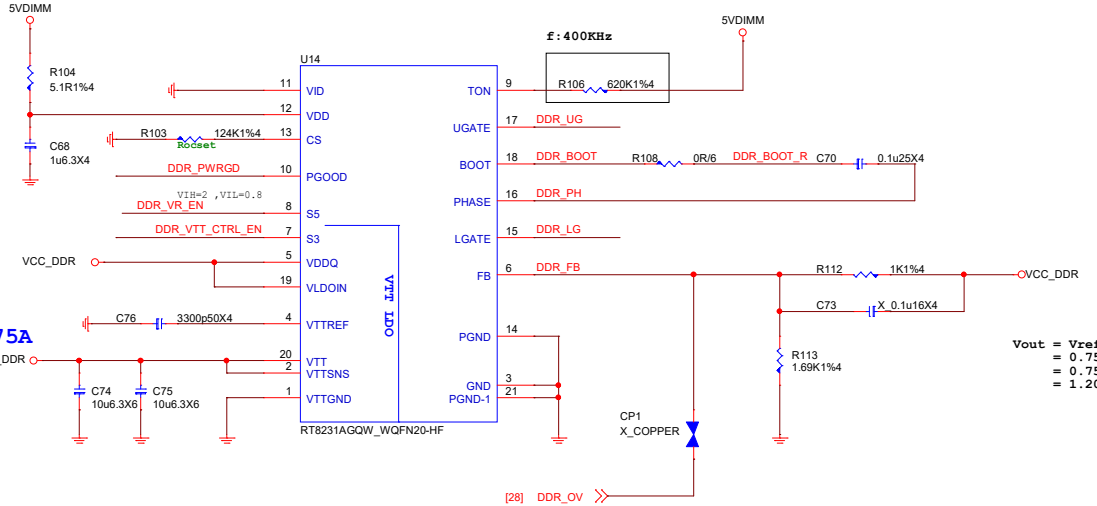






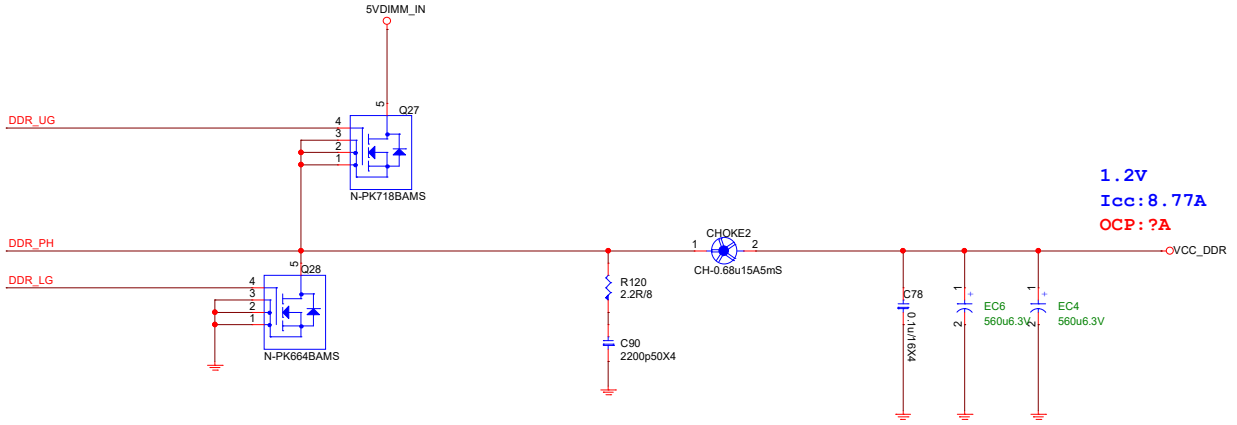


Irms = Iout * SQRT((Vout/Vin) * (1-(Vout/Vin)))
=12.15* 0.427
= 5.2A



FB:0.75V
Vout = Vref * (1 + R215/R222)
= 0.75 * (1 + 1K/1.69K)
= 0.75 * 1.591
= 1.208V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.5* 0.427
= 5.765A



1.2V
Icc:8.77A
OCP:?A

MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: DDR4 Power	Rev: 10
Date: Friday, December 18, 2020	Sheet 53 of 67	

VPP2.5V Power:2.5V,3A

IC OCP:4.6

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 3 * 0.5
     = 1.5A
```

OCP real 3.8A

L=(Vout-(1-Vout/Vin))/(Fsw*Iout*0.4)
=1.66uH

f:1MHz

5VDIMM
CHOKE3
CH-0.24u4.2A22mS-HF
5VDIMM_VPP
C203 X_22u6.3X6
C204 22u6.3X6
C207 0.1u/16X4

U22
SY8113KAIC_TSOT23-8-HF
VIN=4.5~18V
VIH>1.5V
open drain
VPP_EN
VPP_PG
IN
EN
PG
SS
BS
LX
FB
GND
VPP_BOOT
R151 0R/6
VPP_BOOT_R
C217 0.1u/16X4
VPP_PHASE
VPP25_FB
C208 0.01u50X4

CHOKE5
1.0u5.5A-35_1210-HF
VPP25
R150 52.3K1%4
C211 22p50N4
R148 16.5K1%4
C235 22u6.3X6
C223 22u6.3X6
C220 X_22u6.3X6
C242 0.22u16X4

Tss=Css*Vref/Iss
10nF*0.6/4u=1.499ms

Vout=0.6*((R1/R2)+1))
0.6*((52.3/16.5)+1)=2.501

VPP_PHASE R149 X_1R1%6 C212 X_2700p50N4
reserve snubber

ATX_5VSB
R138 47K/4
Q30 2N7002D
1u6.3X4 C183
G2
D1
G1
D2
S2
S1
[12,25,43,44,52,53,56] SLP_S4#
R135 X_0R/4
[25] SIO_VPP_EN
R136 0R/4
5VDIMM
R142 2.2K/4
3V
VPP_EN
R144 3.3K1%4
C190 0.1u/16X4
5V
R134 100K1%4
Q29
R133 X_100K/4
C175 1u6.3X4
2N7002

VPP25
R146 10K/4
2.5V
VPP_PG
C195 0.1u/16X4
ATX_5VSB
R139 47K/4
Q31 2N7002D
5VDIMM
R145 2K1%4
3V
VPP_VR_PG
VPP_VR_PG [25,53]
R143 3K1%4

MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: DDR PWR VPP25/VTT	Rev: 10
Date: Friday, December 18, 2020	Sheet 54 of 67	

PCH_Power:VCCIN_AUX

1.8V 9.646A

VID[1]	VID[1]	PCH_VCCIN_AUX_VOLTAGE
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Tss~600uS

VID Tup and down~135uS

NCP81269MNTXG

PCH_1P8_VSB

1.8V; 1.545A

MP2333HGTL

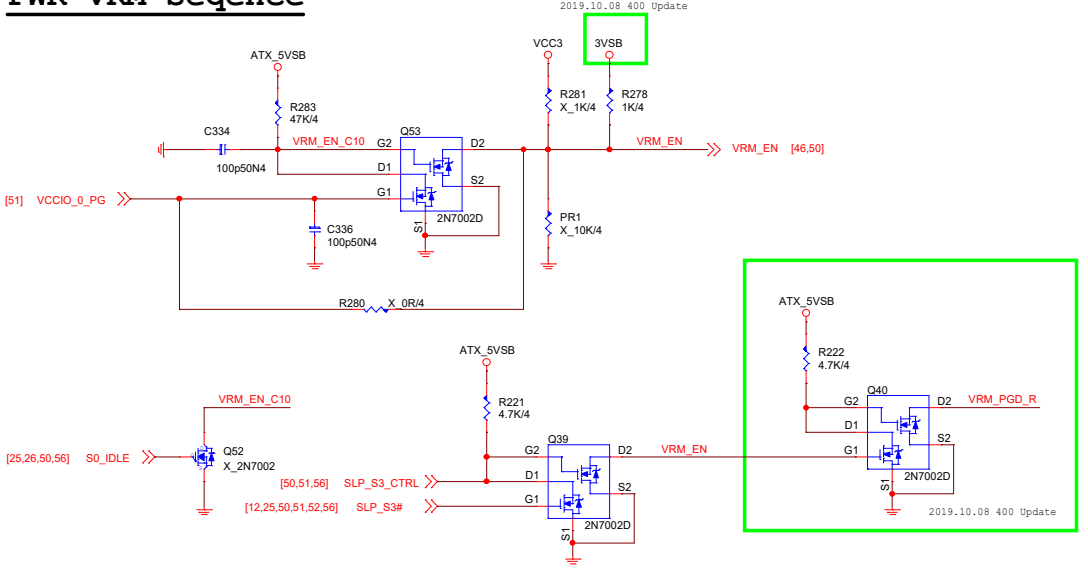
MS-7D22

Size: Custom | Document Description: PCH POWER | Rev: 10

Date: Friday, December 18, 2020 | Sheet 55 of 67

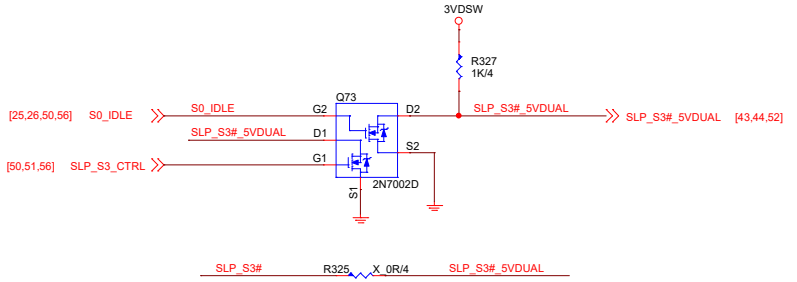
PWR-VRM-Seqence

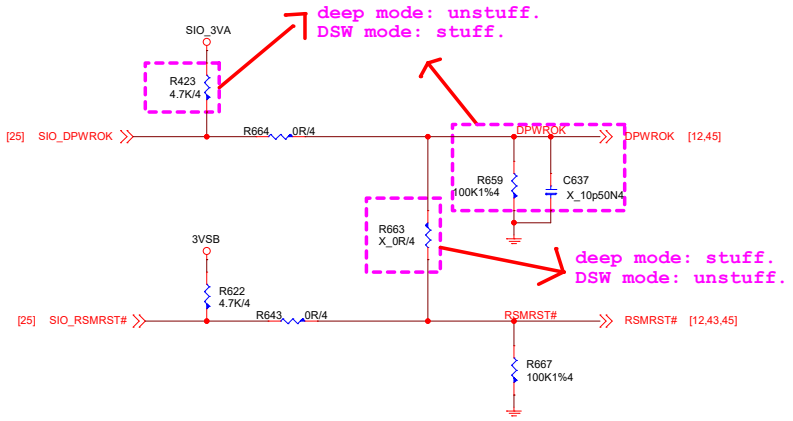
2019.10.08 400 Update



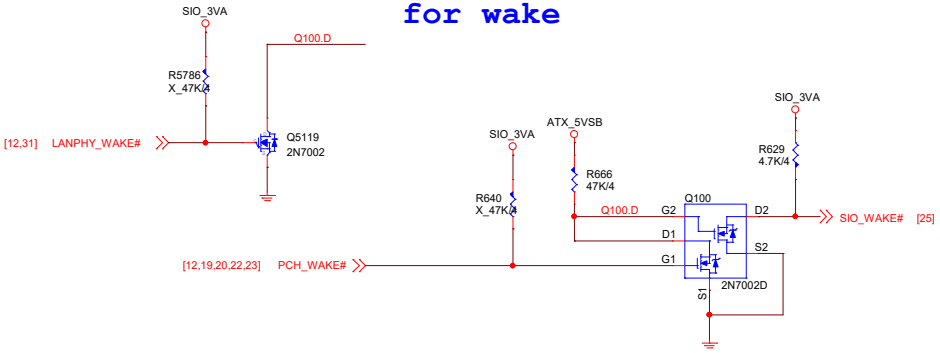
for 5VDIMM and 5VDUAL

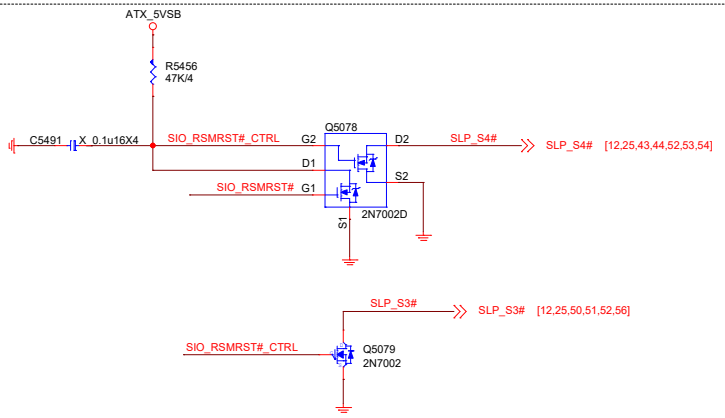
for S0ix

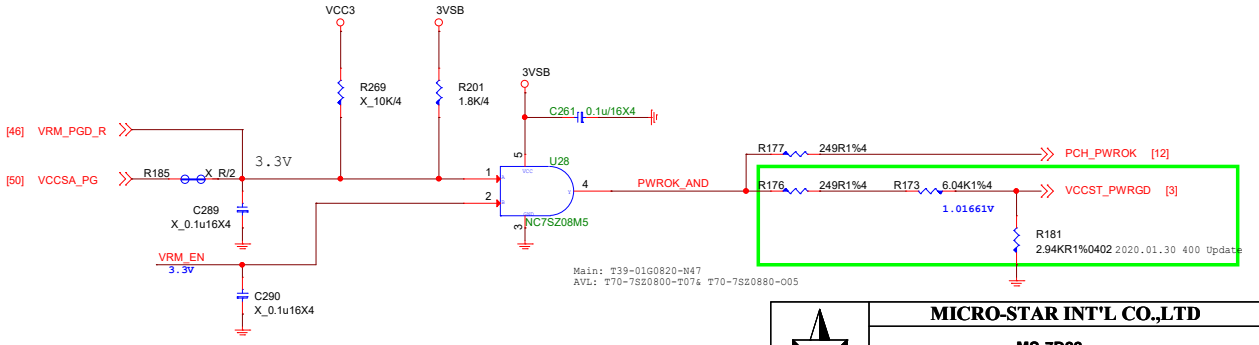




for wake

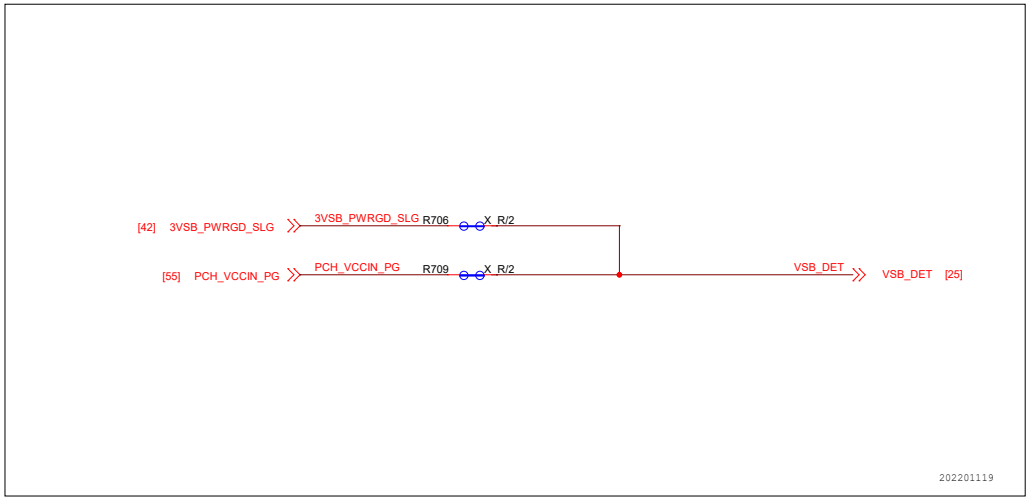






MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: POWER SEQUENCE	Rev: 10
Date: Friday, December 18, 2020	Sheet 56 of 67	

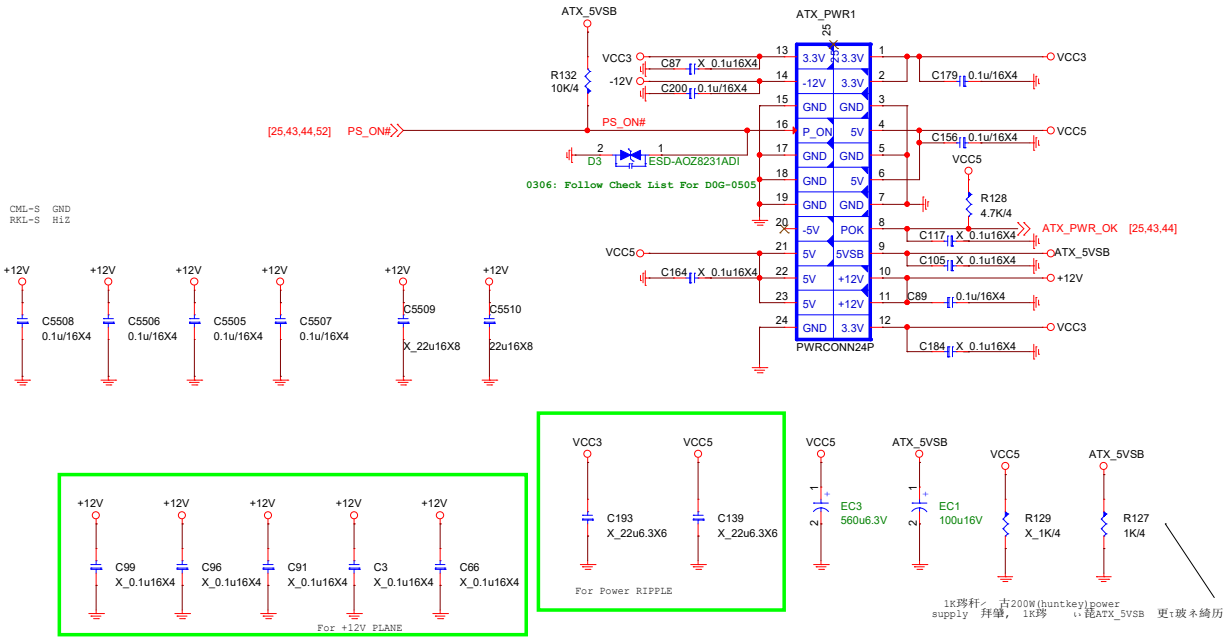
FOR RSMRST#/DPWROK/SLP_SUS# INTEL seqence request



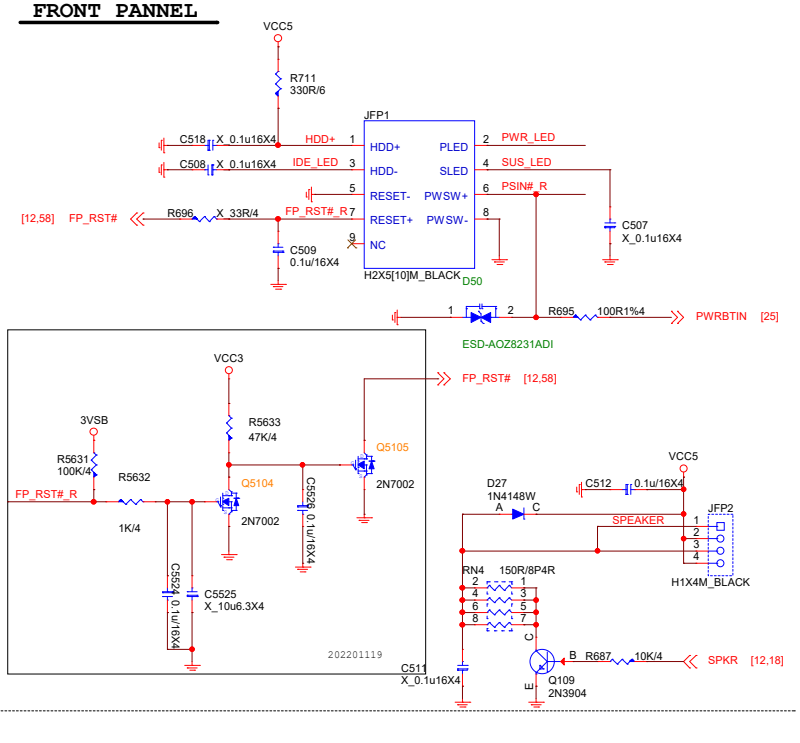
MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: POWER SEQUENCE	Rev: 10
Date: Friday, December 18, 2020	Sheet 57 of 67	

ATX POWER CONNECTOR

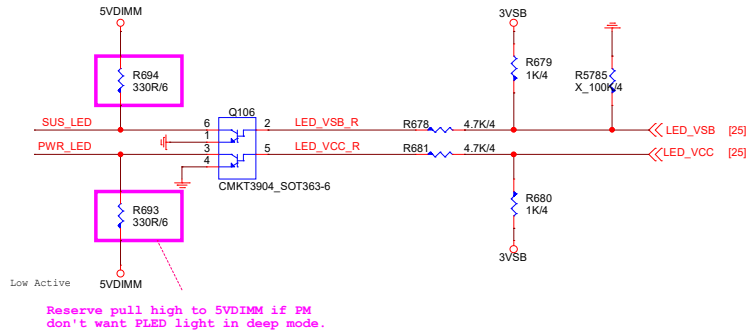
JPWR1

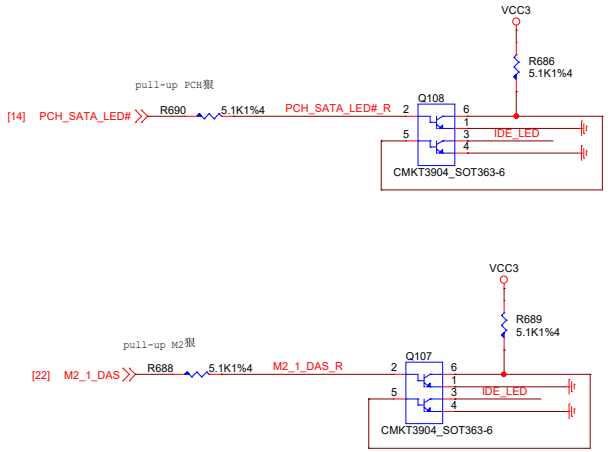


FRONT PANNEL



Front Panel LED

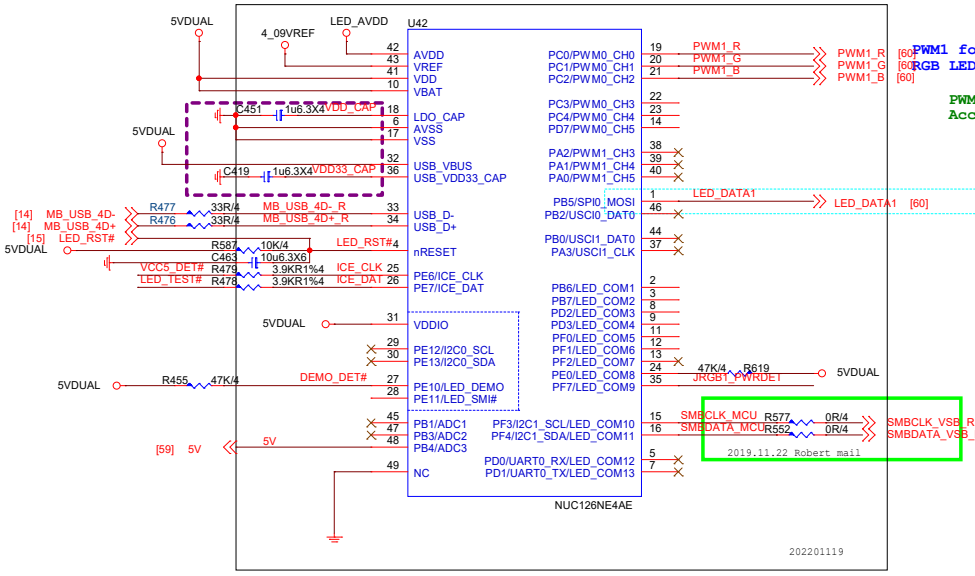




MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: ATX Connector/F_Panel	Rev: 10
Date: Friday, December 18, 2020	Sheet 58 of 67	

LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.



PWM1 for JRGB1
RGB LED STRIPLINE USED

PWM3 for Others
According to demand configuration

PIN1 for JPIPE_LED1~3 and JRAINBOW1
PIN46 for JCORSAIR1
PIN44 for JRAINBOW2

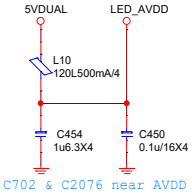
COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.

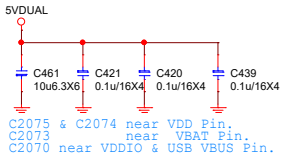
COM9~12 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~12,
To achieve 4 group Non-synchronized
onboard LED control.

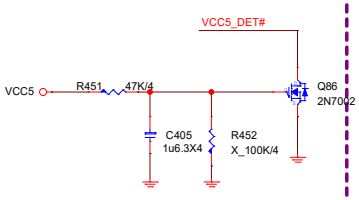
PS. COM1 is the first action block,
next is COM2, and so on.

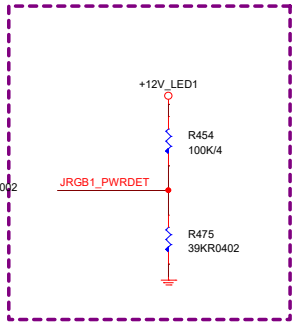
Pin15,16 can configure to master
smbus if spec requirement.

Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1
Board Side LED	COM 1~8	No Use
Board Side LED	COM 9~16	No Use

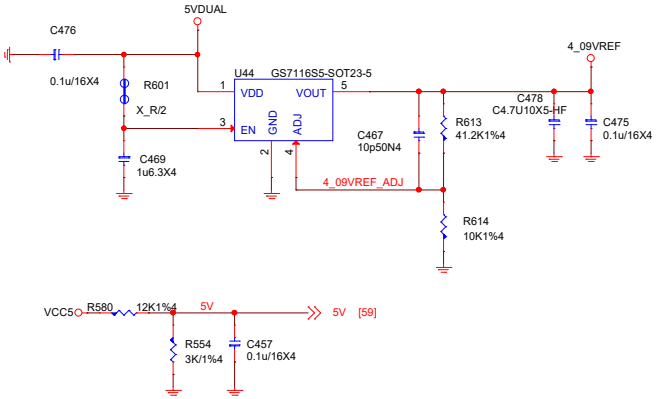








Voltage HW monitor

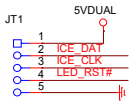


Option spec for voltage monitor require.
VDD1,2,3 is example.

IF no JPWRLED1 & JPIPE_LED spec

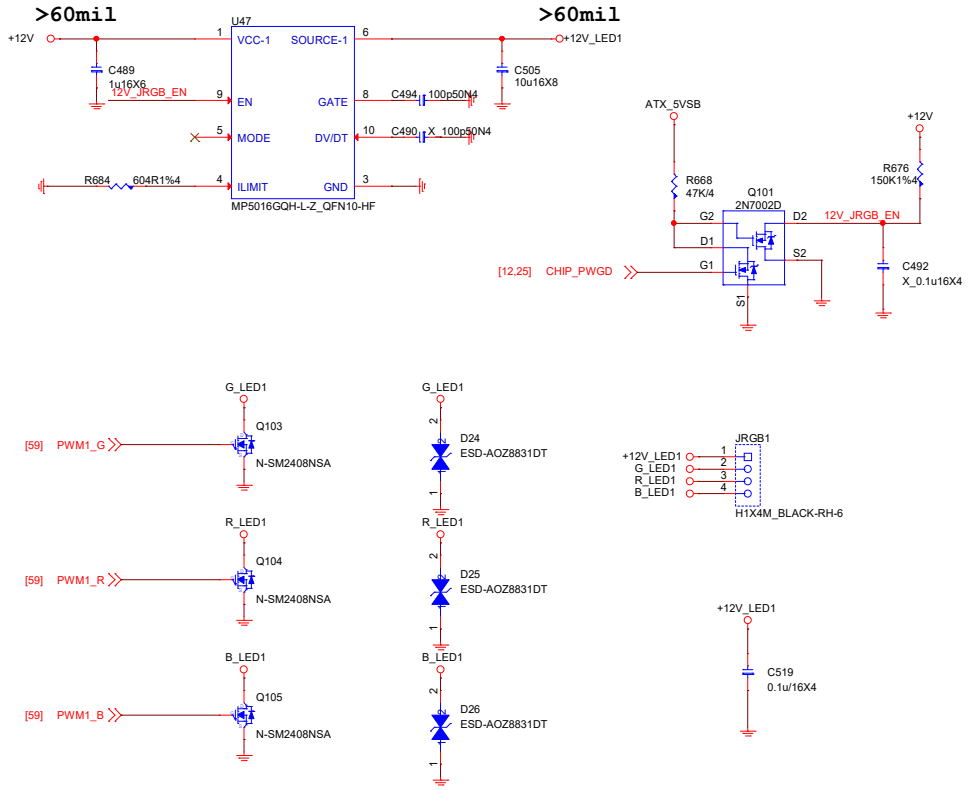
MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JT1 for FW update

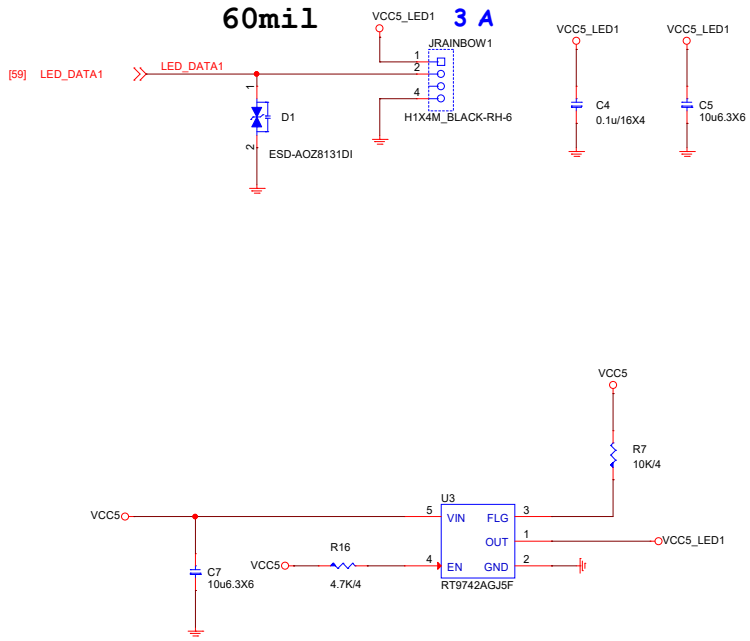


MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: MCU Control	Rev: 0A
Date: Friday, December 18, 2020	Sheet 59 of 67	

JRGB1

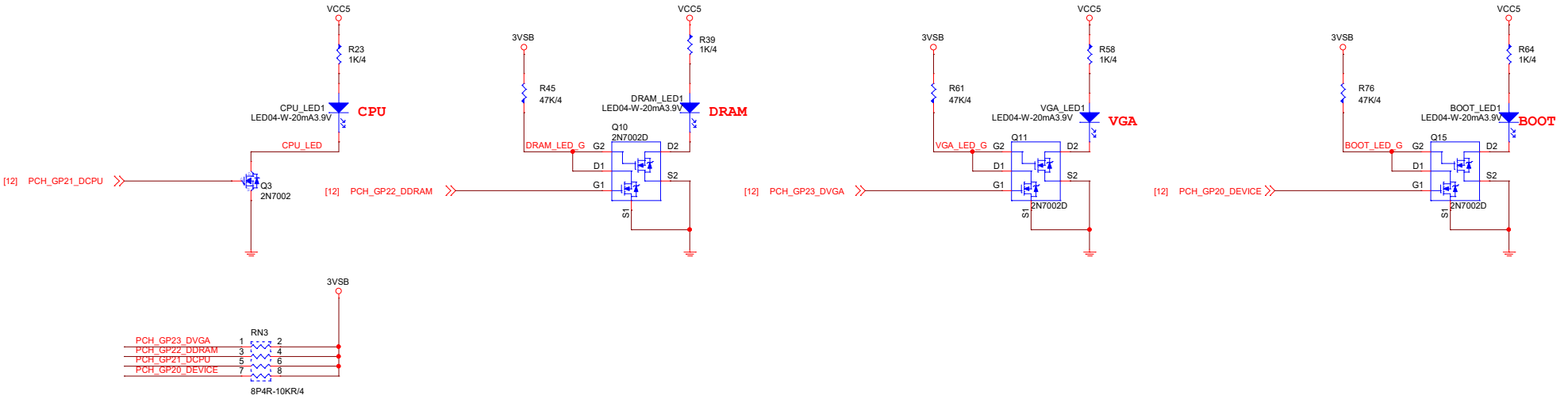


JRAINBOW1 LED



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: JRGB and JRAINBOW1 LED	Rev: 0A
Date: Friday, December 18, 2020	Sheet 60 of 67	

EZ Debug LED



MICRO-STAR INT'L CO.,LTD		
MS-7D22		
Size: Custom	Document Description: EZ Debug LED	Rev: 10
Date: Friday, December 18, 2020	Sheet 61 of 67	

PCB1

7D22-0A

PD0-07D220A-G37
PD0-07D220A-E48

CPU_H1

CPU
腦就

CPU_H1

BAT1_X1
BAT-CR2032-RH
D06-0100101-D73

Heat Sink

HS_PCH1

PCH
Shink

MCE1
MCE2

E31-0409430-K08

BIOS_LA1

AMI

AMI

HDMI_LA1

HDMI VIRTUAL

HDMI LABEL

CFOS_LA1

CFOS VIRTUAL

CFOS LABEL

MKT_LA1

H510-PRO

MKT

Simulation

SIM1

SIM1

X_PIN1*2

SIM2

SIM2

X_PIN1*2

Optical Fiducial Marks-120

FM2 FM1 FM4 FM3

X_FM X_FM X_FM X_FM

FM5 FM6 FM8 FM7

X_FM X_FM X_FM X_FM

Mounting Holes

MH1 MH2 MH3

X_MH001 X_MH001 X_MH001

MH5 MH4 MH6

X_MH001 X_MH001 X_MH001

C435
0.1u/16X4

C477
0.1u/16X4

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D22	
Size: Custom	Document Description: Manual Parts	Rev: 10
Date: Friday, December 18, 2020	Sheet 62 of 67	