Project Name : GM5TGFX

Platform : TGL-H+GN20-P

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

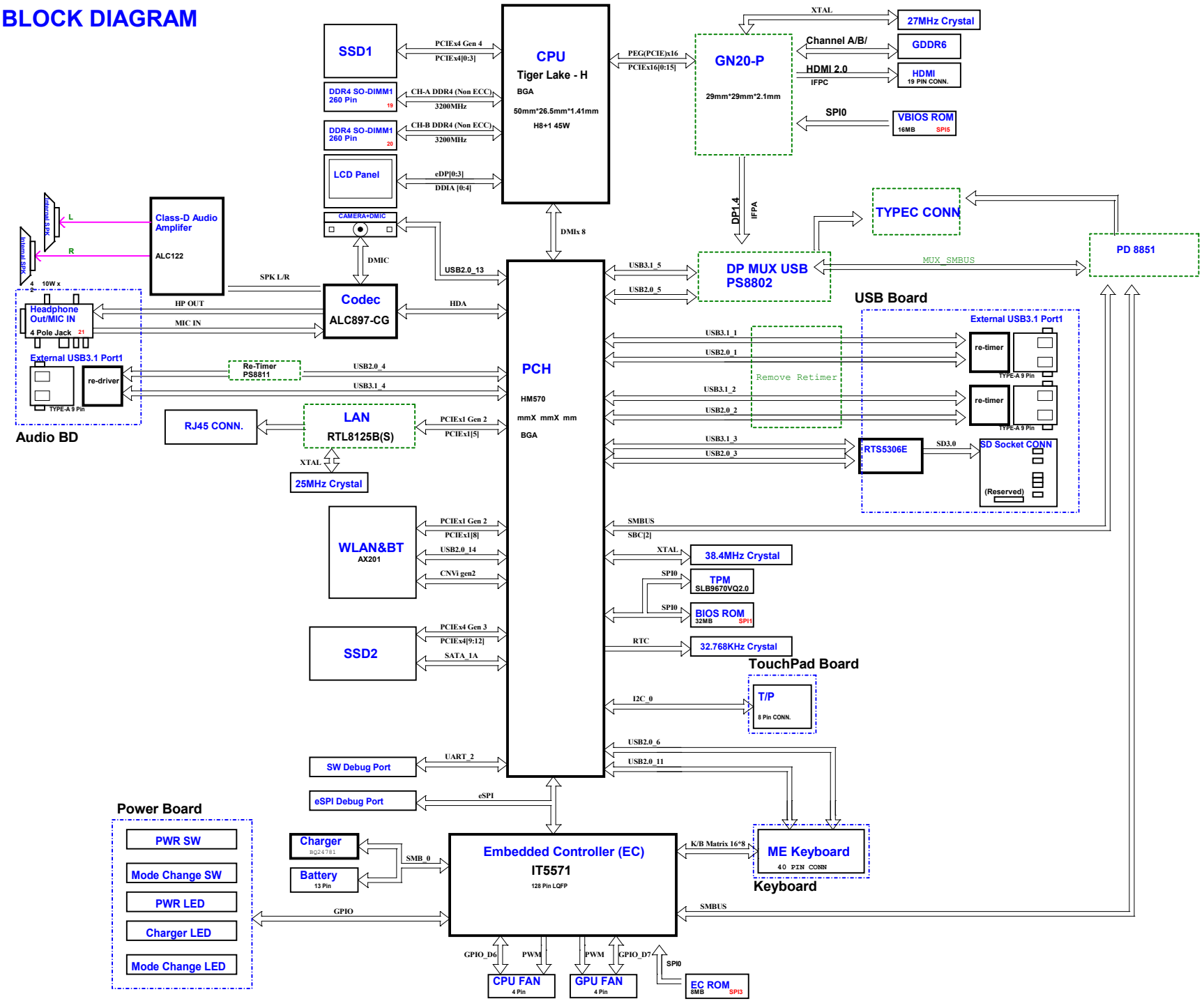
同方国际信息技术有限公司

Title: INDEX

Size: Custom | Document Number: GM5TGFX | Rev: 1.2

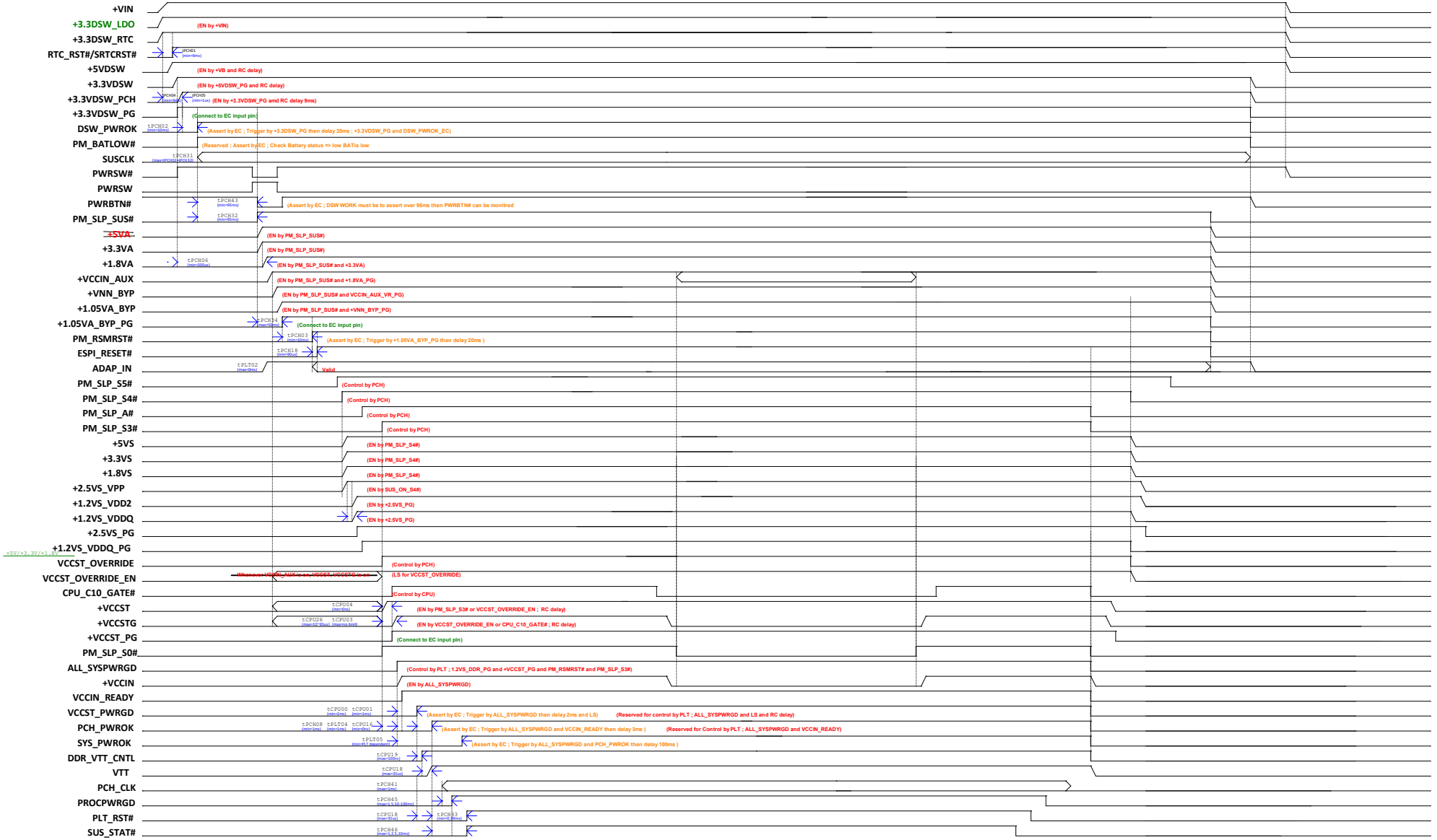
Date: Tuesday, May 18, 2021 | Sheet 1 of 78

SYSTEM BLOCK DIAGRAM



同方国际信息技术有限公司			
Title	SYSTEM BLOCK		
Size	Document Number	GM5TGFX	Rev 1.2
Custom			
Date: Tuesday, May 18, 2021	Sheet 2 of 78		

POWER ON SEQUENCE



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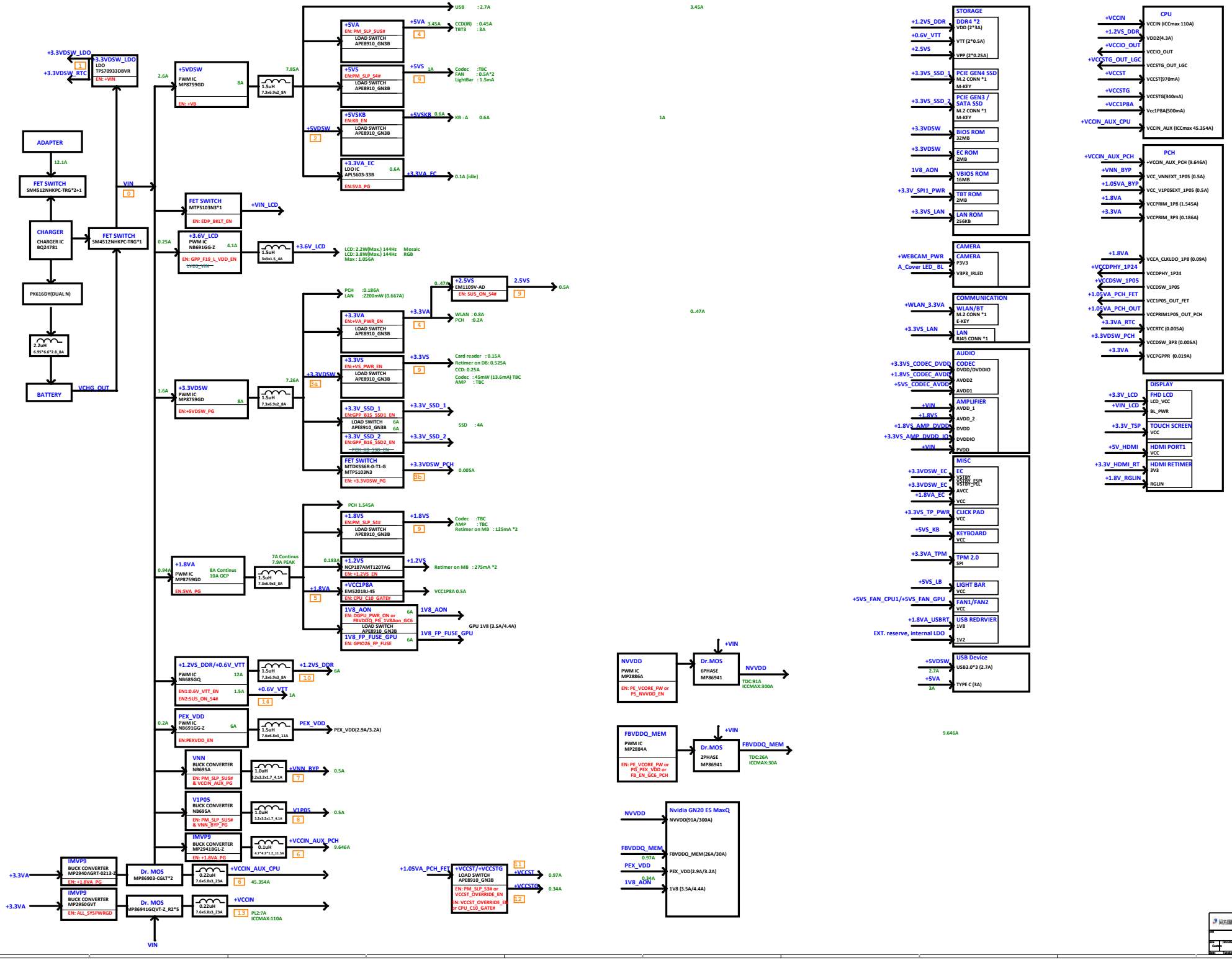
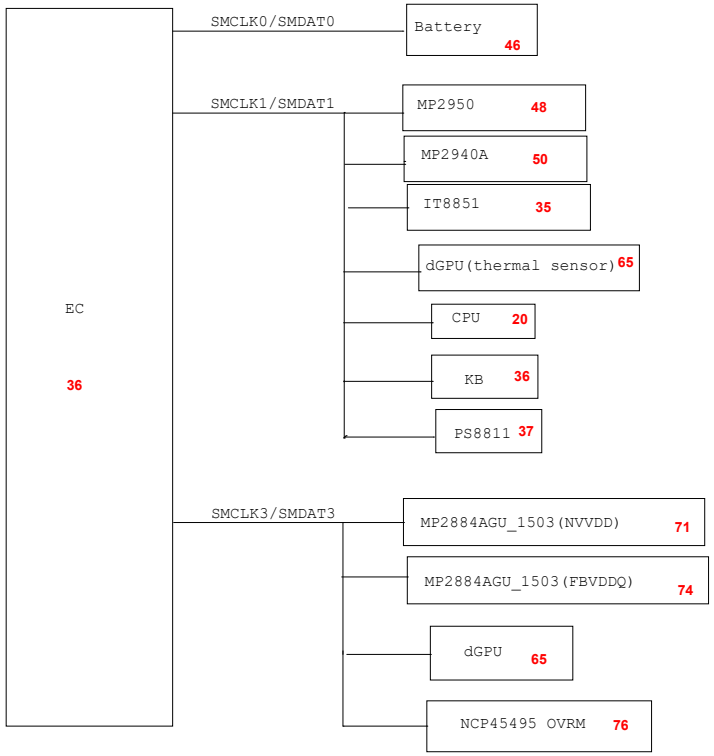
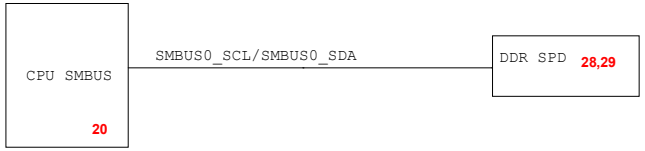
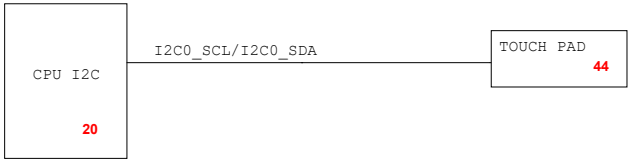
Title	POWER SEQUENCE		
Size: D	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 3 of 78		


ADAPTER
12.1A
FET SWITCH
SM4512NHKPC-TRG*2+1
CHARGER
CHARGER IC
BQ24781
PK616DY(DUAL N)
2.2uH
6.95*6.6*2.8_8A
BATTERY
VCHG_OUT
VIN
+3.3VDSW_LDO
+3.3VDSW_RTC
3.3VDSW_LDO
LDO
TPS70933DBVR
EN: +VIN
+5VDSW
PWM IC
MP8759GD
8A
EN: +VB
1.5uH
7.3x6.9x2_8A
+3.3VDSW
PWM IC
MP8759GD
8A
EN:+5VDSW_PG
+3.6V_LCD
PWM IC
NB691GG-Z
4.1A
EN: GPP_F19_L_VDD_EN
+VIN_LCD
FET SWITCH
MTP5103N3*1
EN: EDP_BKLT_EN
+1.8VA
PWM IC
MP8759GD
8A Continus
10A OCP
EN:5VA_PG
7A Continus
7.9A PEAK
+1.2VS_DDR/+0.6V_VTT
PWM IC
NB685GQ
12A
EN1:0.6V_VTT_EN
EN2:SUS_ON_S4#
1.5A
PEX_VDD
PWM IC
NB691GG-Z
6A
EN:PEXVDD_EN
VNN
BUCK CONVERTER
NB695A
EN: PM_SLP_SUS#
& VCCIN_AUX_PG
V1P05
BUCK CONVERTER
NB695A
EN: PM_SLP_SUS#
& VNN_BYP_PG
IMVP9
BUCK CONVERTER
MP2941BGL-Z
EN: +1.8VA_PG
IMVP9
BUCK CONVERTER
MP2940AGRT-0213-Z
EN: +1.8VA_PG
IMVP9
BUCK CONVERTER
MP2950GVT
EN: ALL_SYSPWRGD
Dr. MOS
MP86903-CGLT*2
Dr. MOS
MP86941GQVT-Z_R2*5
+3.3VA
+3.3VA
VIN
+5VA
EN: PM_SLP_SUS#
LOAD SWITCH
APE8910_GN3B
+5VS
EN:PM_SLP_S4#
LOAD SWITCH
APE8910_GN3B
+5VSKB
EN:KB_EN
LOAD SWITCH
APE8910_GN3B
+3.3VA_EC
LDO IC
APL5603-33B
EN:5VA_PG
+3.3VA
EN:+VA_PWR_EN
LOAD SWITCH
APE8910_GN3B
+3.3VS
EN:+VS_PWR_EN
LOAD SWITCH
APE8910_GN3B
+3.3V_SSD_1
EN:GPP_B15_SSD1_EN
LOAD SWITCH
APE8910_GN3B
+3.3V_SSD_2
EN:GPP_B16_SSD2_EN
FET SWITCH
MTDK5S6R-0-T1-G
MTP5103N3
EN: +3.3VDSW_PG
+1.8VS
EN:PM_SLP_S4#
LOAD SWITCH
APE8910_GN3B
+1.2VS
NCP187AMT120TAG
EN: +1.2VS_EN
+VCC1P8A
EM5201BJ-45
EN: CPU_C10_GATE#
1V8_AON
EN: DGPU_PWR_ON or
FBVDDQ_PG_1V8Aon_GC6
LOAD SWITCH
APE8910_GN3B
1V8_FP_FUSE_GPU
EN: GPIO26_FP_FUSE
+2.5VS
EM1109V-AD
EN: SUS_ON_S4#
+1.05VA_PCH_FET
+VCCST/+VCCSTG
LOAD SWITCH
APE8910_GN3B
EN: PM_SLP_S3# or
VCCST_OVERRIDE_EN
EN: VCCST_OVERRIDE_EN
or CPU_C10_GATE#
USB : 2.7A
CCD(IR) : 0.45A
TBT3 : 3A
Codec :TBC
FAN : 0.5A*2
LightBar : 1.5mA
KB : A 0.6A
0.1A (idle)
LCD: 2.2W(Max.) 144Hz
LCD: 3.8W(Max.) 144Hz
Max : 1.056A
Mosaic
RGB
PCH :0.186A
LAN :2200mW (0.667A)
WLAN : 0.8A
PCH :0.2A
Card reader : 0.15A
Retimer on DB: 0.525A
CCD: 0.25A
Codec : 45mW (13.6mA) TBC
AMP : TBC
SSD : 4A
0.005A
PCH 1.545A
Codec :TBC
AMP :TBC
Retimer on MB :125mA *2
Retimer on MB : 275mA *2
VCC1P8A 0.5A
GPU 1V8 (3.5A/4.4A)
PEX_VDD(2.9A/3.2A)
+VCCIN_AUX_CPU
45.354A
+VCCIN
PL2:2A
ICCMAX:110A
0.5A
0.97A
0.34A
NVVDD
PWM IC
MP2886A
EN: PE_VCORE_FW or
PS_NVVDD_EN
Dr.MOS
6PHASE
MP86941
NVVDD
TDC:91A
ICCMAX:300A
FBVDDQ_MEM
PWM IC
MP2884A
EN: PE_VCORE_FW or
PG_PEX_VDD or
FB_EN_GC6_PCH
Dr.MOS
2PHASE
MP86941
FBVDDQ_MEM
TDC:26A
ICCMAX:30A
Nvidia GN20 E5 MaxQ
NVVDD(91A/300A)
FBVDDQ_MEM(26A/30A)
PEX_VDD(2.9A/3.2A)
1V8 (3.5A/4.4A)
3.45A
1A
0..47A
9.646A
STORAGE
DDR4 *2
VDD (2*3A)
VTT (2*0.5A)
VPP (2*0.25A)
PCIE GEN4 SSD
M.2 CONN *1
M-KEY
PCIE GEN3 /
SATA SSD
M.2 CONN *1
M-KEY
BIOS ROM
32MB
EC ROM
2MB
VBIOS ROM
16MB
TBT ROM
2MB
LAN ROM
256KB
CAMERA
CAMERA
P3V3
V3P3_IRLED
COMMUNICATION
WLAN/BT
M.2 CONN *1
E-KEY
LAN
RJ45 CONN *1
AUDIO
CODEC
DVDD/DVDDIO
AVDD2
AVDD1
AMPLIFIER
AVDD_1
AVDD_2
DVDD
DVDDIO
PVDD
MISC
EC
VSTBY
VSTBY_EDPI
VSTBY_PYE
AVCC
VCC
CLICK PAD
VCC
KEYBOARD
VCC
TPM 2.0
SPI
LIGHT BAR
VCC
FAN1/FAN2
VCC
USB REDRVIER
1V8
1V2
USB Device
USB3.0*3 (2.7A)
TYPE C (3A)
CPU
VCCIN (ICCmax 110A)
VDD2(4.3A)
VCCIO_OUT
VCCSTG_OUT_LGC
VCCST(970mA)
VCCSTG(340mA)
Vcc1P8A(500mA)
VCCIN_AUX (ICCmax 45.354A)
PCH
+VCCIN_AUX_PCH (9.646A)
VCC_VNNEXT_1P05 (0.5A)
VCC_V1P05EXT_1P05 (0.5A)
VCCPRIM_1P8 (1.545A)
VCCPRIM_3P3 (0.186A)
VCCA_CLKLDO_1P8 (0.09A)
VCCDPHY_1P24
VCCDSW_1P05
VCC1P05_OUT_FET
VCCPRIM1P05_OUT_PCH
VCCRTC (0.005A)
VCCDSW_3P3 (0.005A)
VCCPGPPR (0.019A)
DISPLAY
FHD LCD
LCD_VCC
BL_PWR
TOUCH SCREEN
VCC
HDMI PORT1
VCC
HDMI RETIMER
3V3
RGLIN
POWER MAP
GM5TGFX
1.2

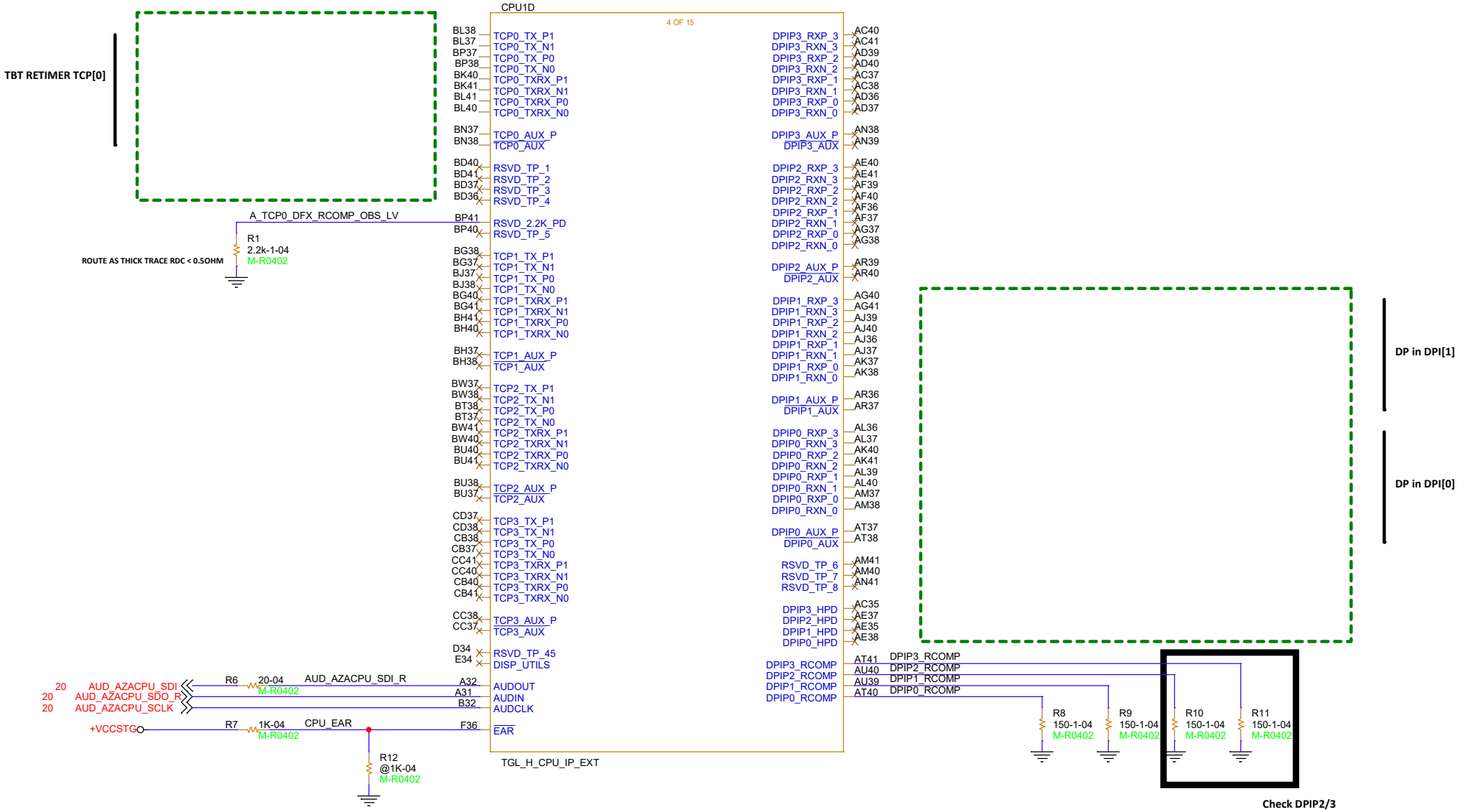
Type	Location	Firmware
MP2950	U23	??
MP2940	U29	??
MP2884 (NVVDD)	U25	??
MP2884 (FB_MEM)	U84	??
IT8851	PU3	??





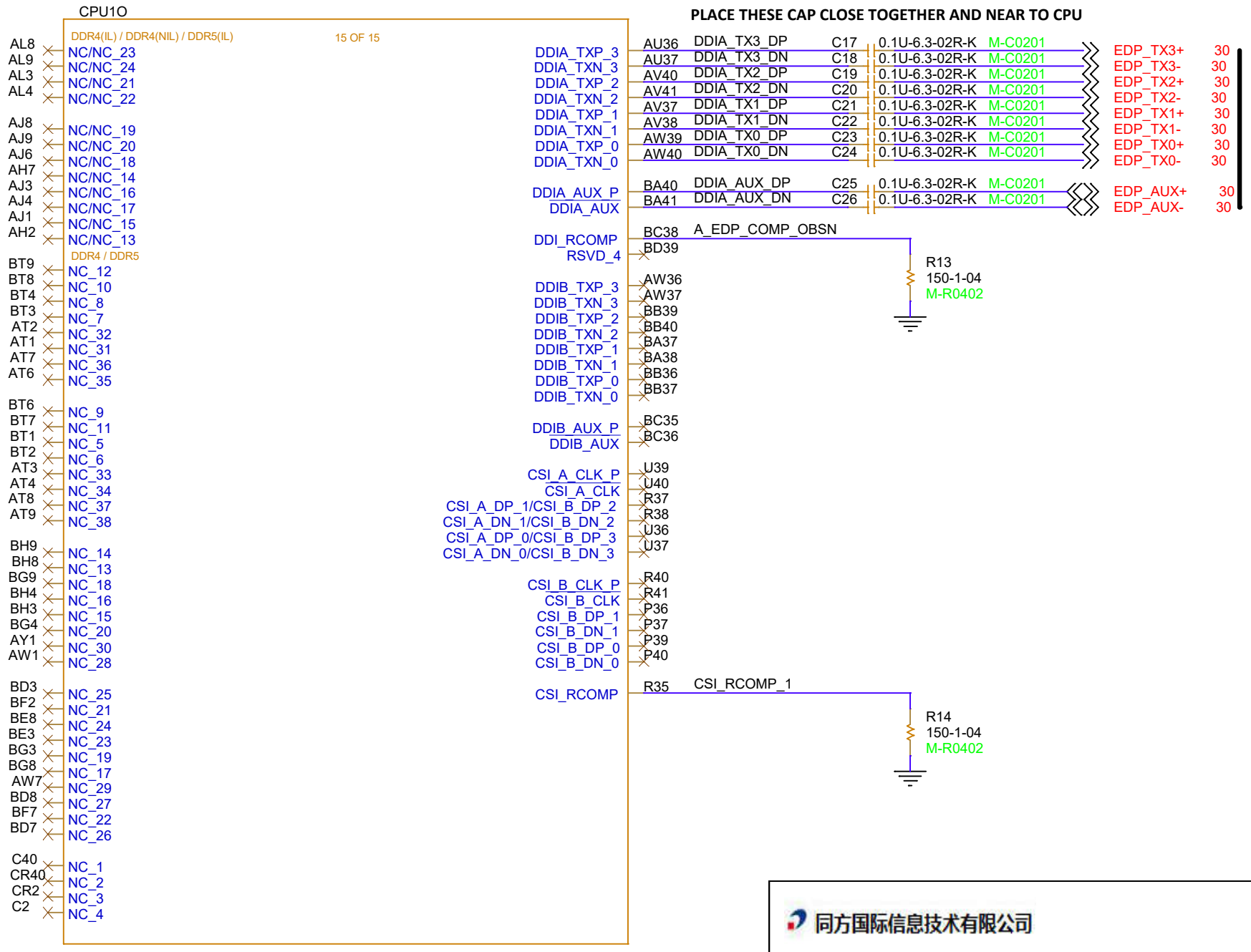


同方国际信息技术有限公司		
Title	SMBUS Block&FW Ver	
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 5 of 78	



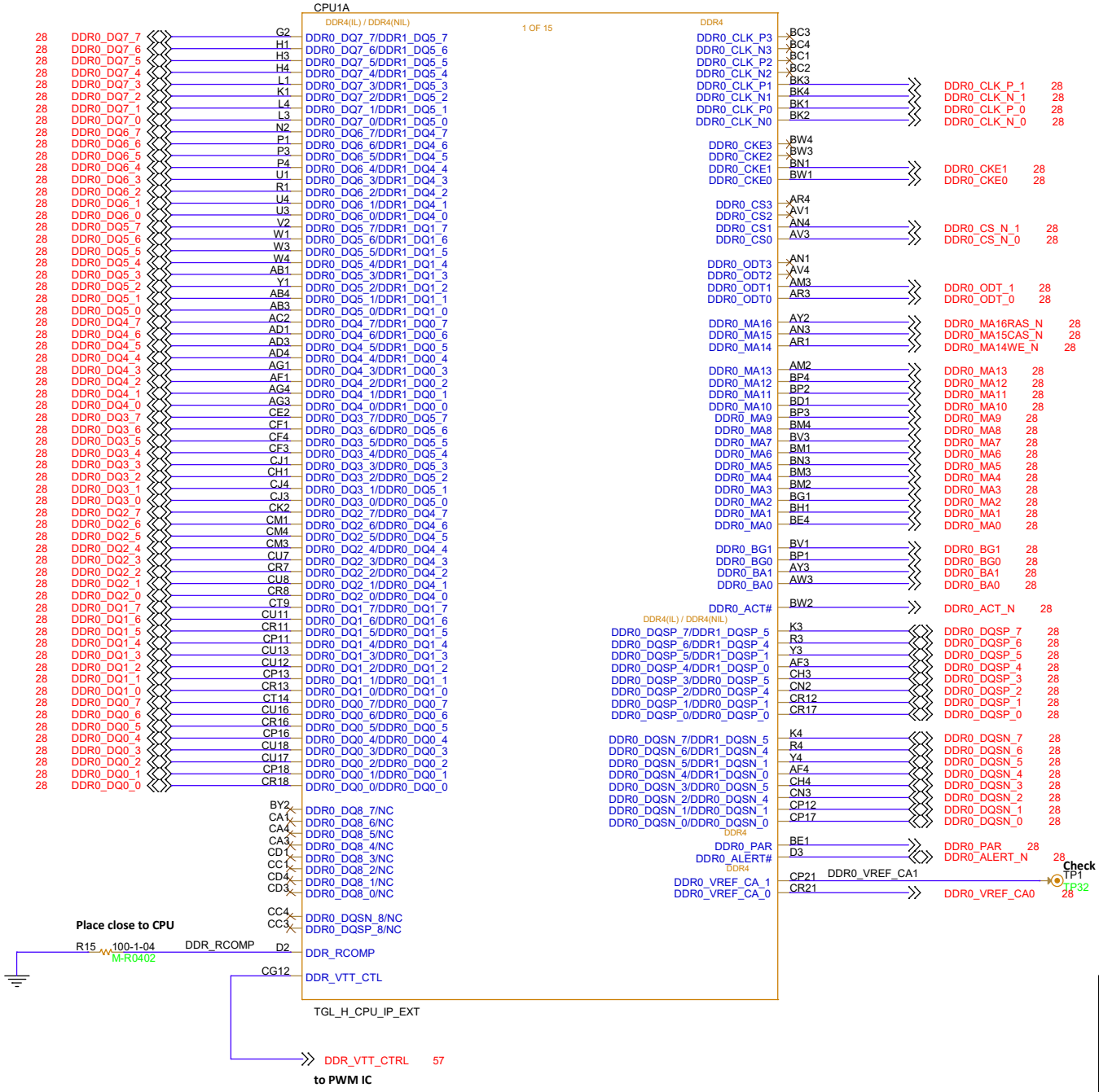
同方国际信息技术有限公司

Title	TGL_H TBT/DDI	
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 6 of 78	



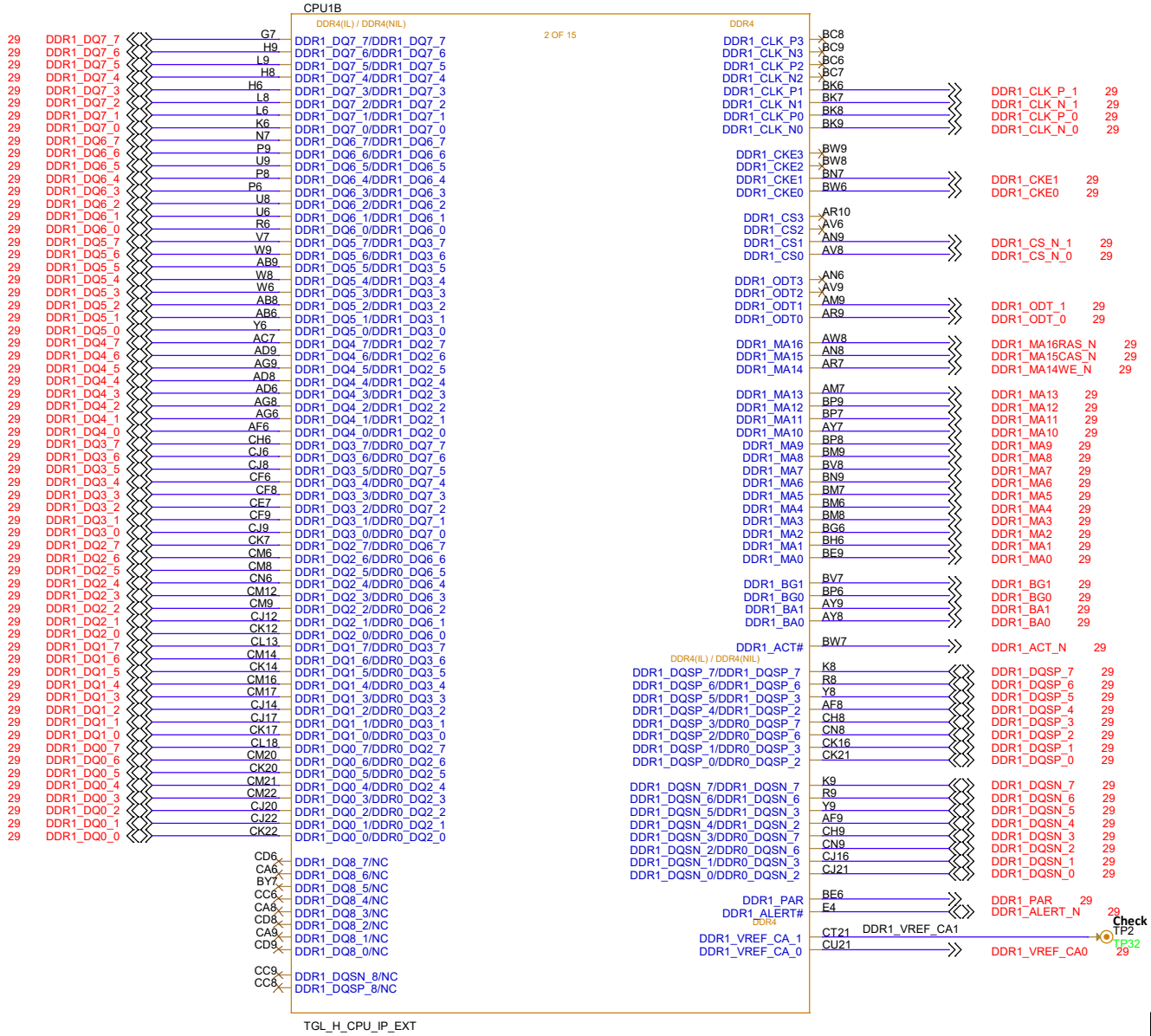
同方国际信息技术有限公司

Title	TGL_H eDP	
Size A	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 7 of 78	



同方国际信息技术有限公司

Title	TGL_H MEMORY CHA	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 8 of 78	



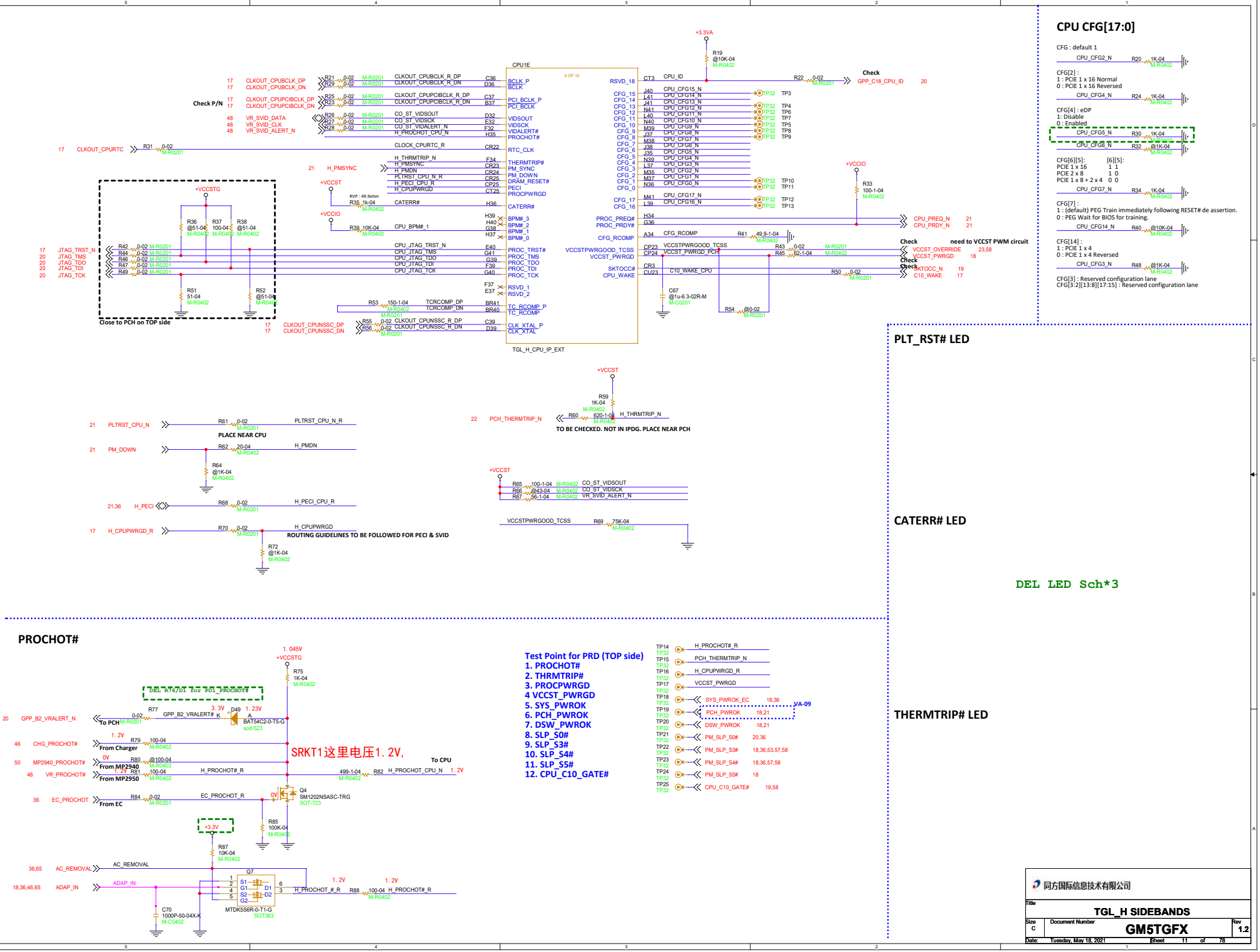
同方国际信息技术有限公司

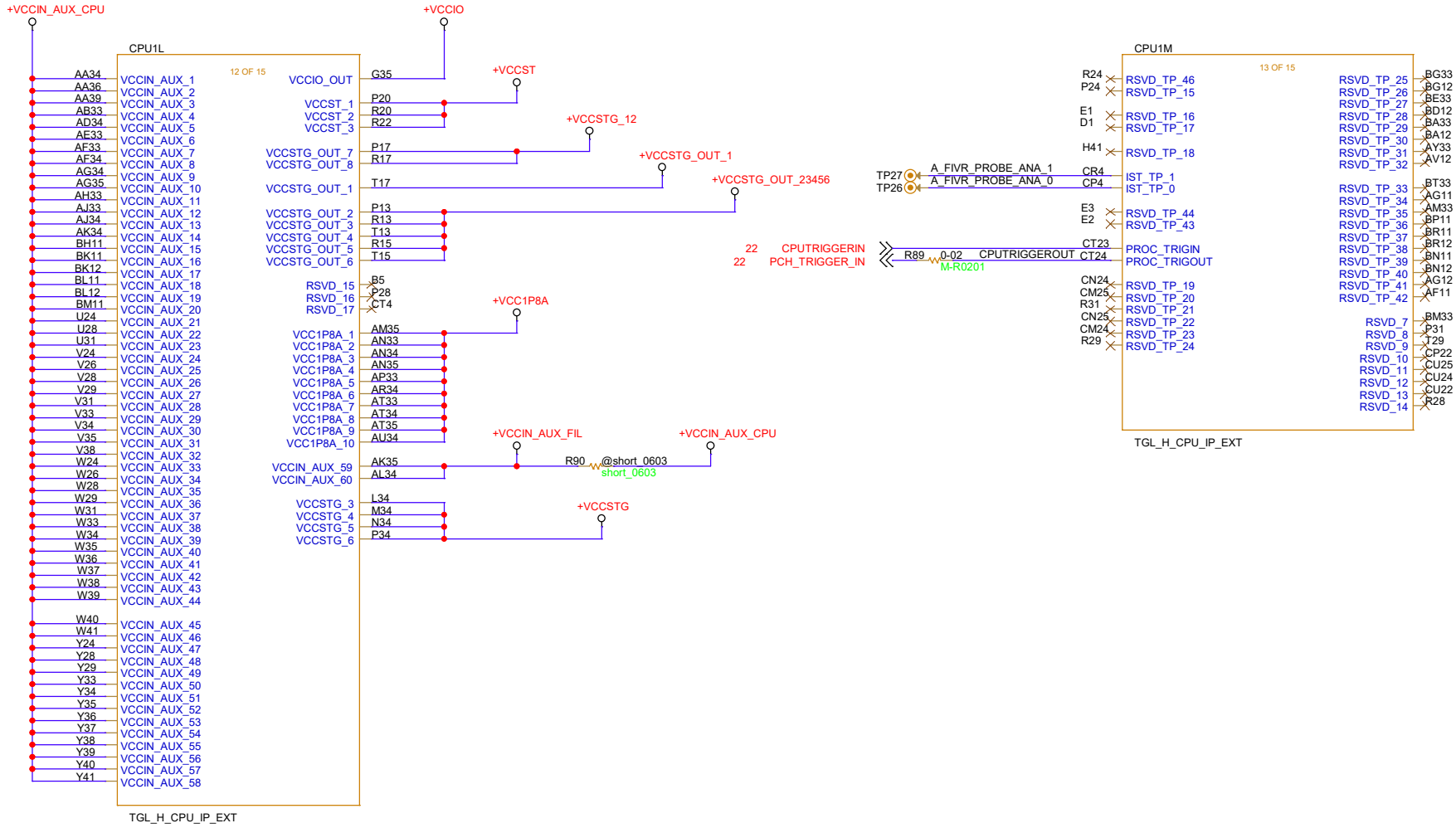
Title	TGL_H MEMORY CHB		
Size B	Document Number GM5TGFX		Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 9 of 78		

CPU PCIE Configuration Table		
PCIE4	SSD1	Gen 4 by 4
PCIE16	NV GN20	Gen 4 by 16

同方国际信息技术有限公司

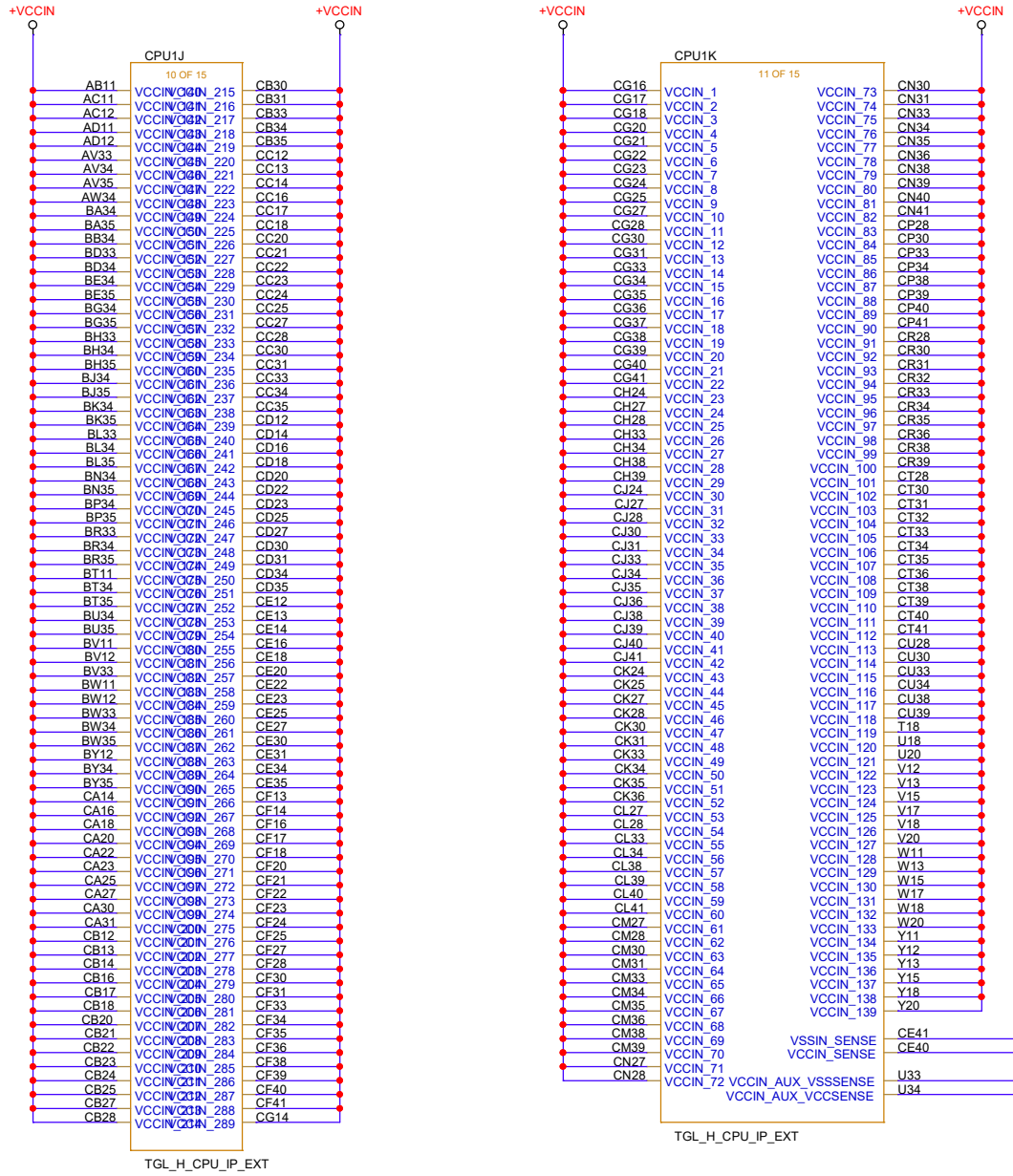
Title	TGL_H PEG/DMI	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 10 of 78	


CPU CFG[17:0]
CFG : default 1
CFG[2] :
1 : PCIE 1 x 16 Normal
0 : PCIE 1 x 16 Reversed
CFG[4] : eDP
1: Disable
0 : Enabled
CFG[6][5]: [6][5]:
PCIE 1 x 16 1 1
PCIE 2 x 8 1 0
PCIE 1 x 8 + 2 x 4 0 0
CFG[7] :
1 : (default) PEG Train immediately following RESET# de assertion.
0 : PEG Wait for BIOS for training.
CFG[14] :
1 : PCIE 1 x 4
0 : PCIE 1 x 4 Reversed
CFG[3] : Reserved configuration lane
CFG[3:2][13:8][17:15] : Reserved configuration lane
CPU1E
TGL_H_CPU_IP_EXT
Check P/N
Close to PCH on TOP side
PLT_RST# LED
CATERR# LED
THERMTRIP# LED
DEL LED Sch*3
PLACE NEAR CPU
TO BE CHECKED. NOT IN IPDG. PLACE NEAR PCH
ROUTING GUIDELINES TO BE FOLLOWED FOR PECI & SVID
PROCHOT#
SRKT1这里电压1. 2V,
Test Point for PRD (TOP side)
1. PROCHOT#
2. THRMTRIP#
3. PROCPWRGD
4 VCCST_PWRGD
5. SYS_PWROK
6. PCH_PWROK
7. DSW_PWROK
8. SLP_S0#
9. SLP_S3#
10. SLP_S4#
11. SLP_S5#
12. CPU_C10_GATE#
同方国际信息技术有限公司
TGL_H SIDEBANDS
GM5TGFX
1.2
Tuesday, May 18, 2021
11 of 78



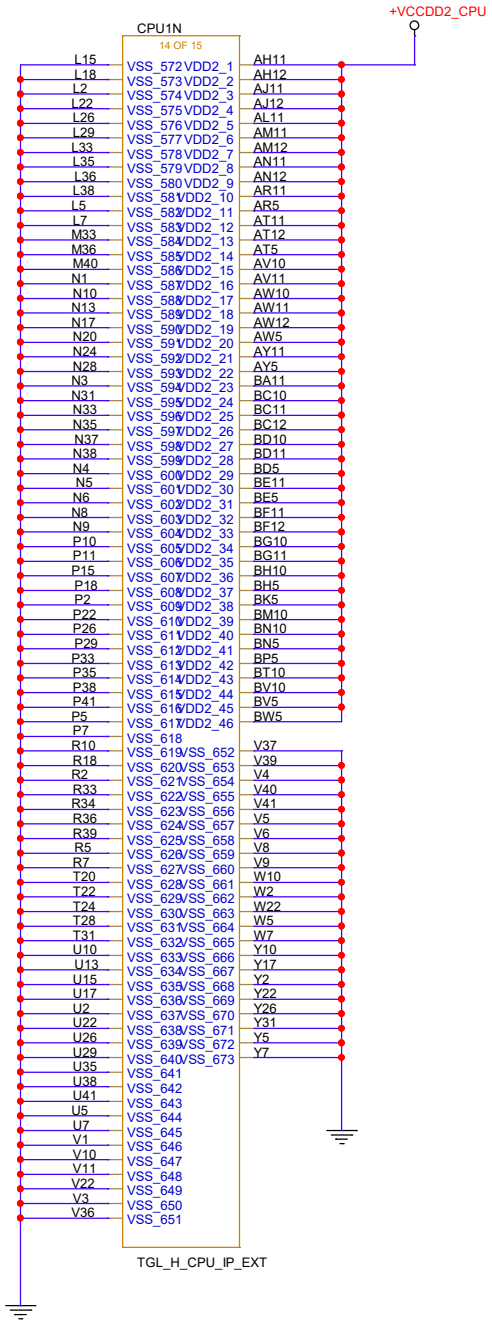
同方国际信息技术有限公司

Title	TGL_H PWR 1,FIVR	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 12 of 78	



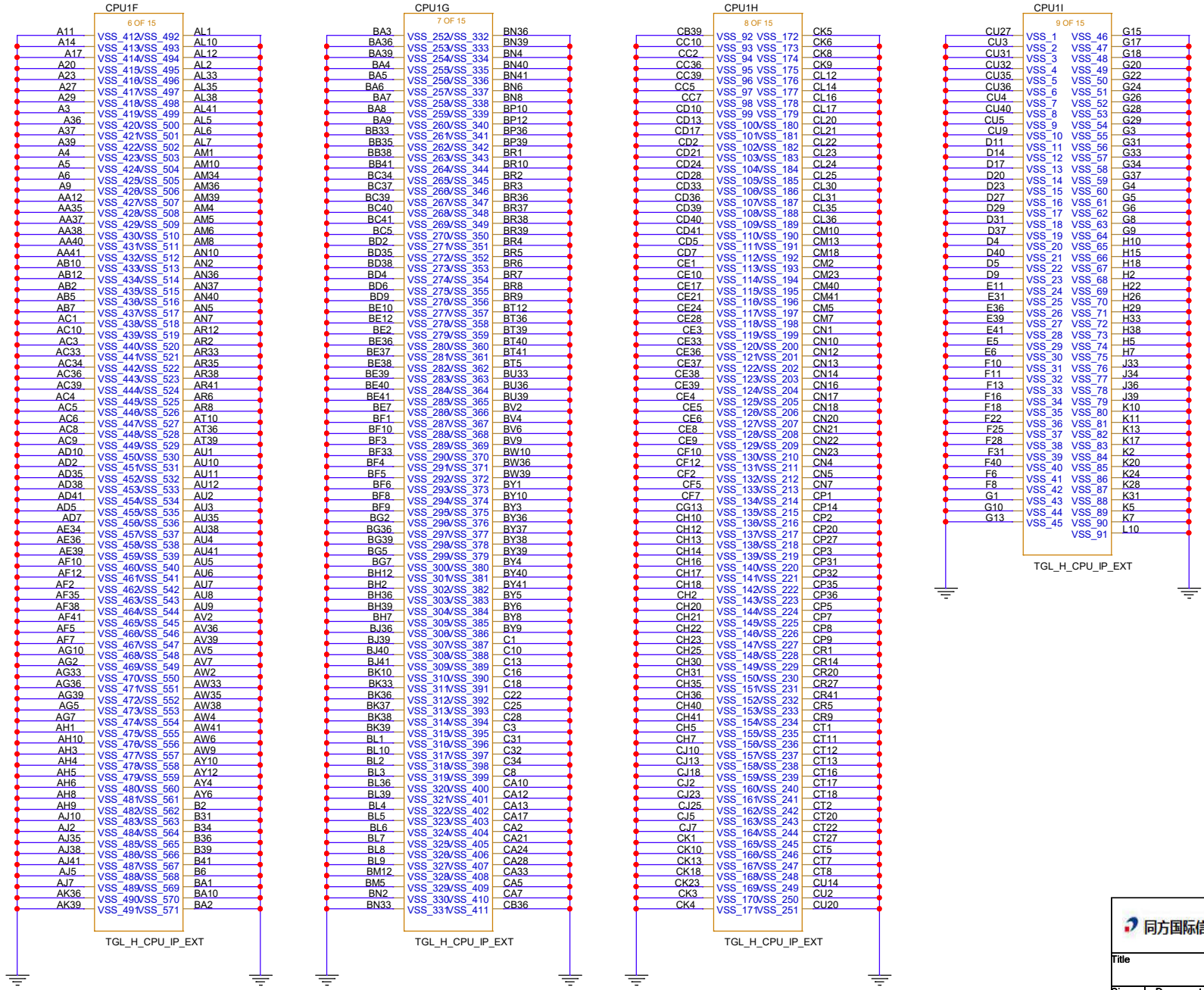
同方国际信息技术有限公司

Title	TGL_H PWR 2	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 13 of 78	



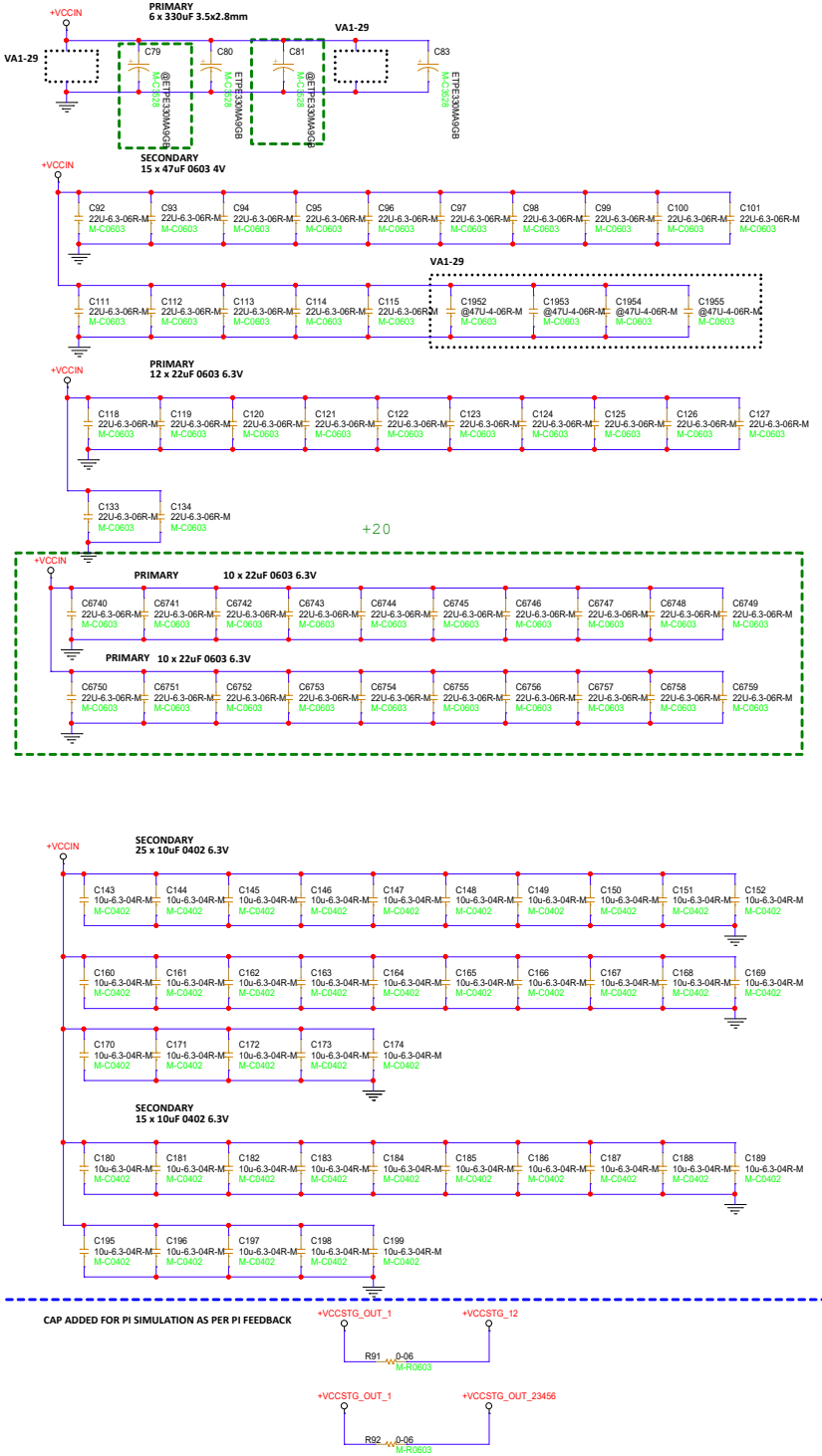
同方国际信息技术有限公司

Title	TGL_H PWR 3/GND	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 14 of 78	


CPU1F
6 OF 15
A11 A14 A17 A20 A23 A27 A29 A3 A36 A37 A39 A4 A5 A6 A9 AA12 AA35 AA37 AA38 AA40 AA41 AB10 AB12 AB2 AB5 AB7 AC1 AC10 AC3 AC33 AC34 AC36 AC39 AC4 AC5 AC6 AC8 AC9 AD10 AD2 AD35 AD38 AD41 AD5 AD7 AE34 AE36 AE39 AF10 AF12 AF2 AF35 AF38 AF41 AF5 AF7 AG10 AG2 AG33 AG36 AG39 AG5 AG7 AH1 AH10 AH3 AH4 AH5 AH6 AH8 AH9 AJ10 AJ2 AJ35 AJ38 AJ41 AJ5 AJ7 AK36 AK39
VSS_412/VSS_492 VSS_413/VSS_493 VSS_414/VSS_494 VSS_415/VSS_495 VSS_416/VSS_496 VSS_417/VSS_497 VSS_418/VSS_498 VSS_419/VSS_499 VSS_420/VSS_500 VSS_421/VSS_501 VSS_422/VSS_502 VSS_423/VSS_503 VSS_424/VSS_504 VSS_425/VSS_505 VSS_426/VSS_506 VSS_427/VSS_507 VSS_428/VSS_508 VSS_429/VSS_509 VSS_430/VSS_510 VSS_431/VSS_511 VSS_432/VSS_512 VSS_433/VSS_513 VSS_434/VSS_514 VSS_435/VSS_515 VSS_436/VSS_516 VSS_437/VSS_517 VSS_438/VSS_518 VSS_439/VSS_519 VSS_440/VSS_520 VSS_441/VSS_521 VSS_442/VSS_522 VSS_443/VSS_523 VSS_444/VSS_524 VSS_445/VSS_525 VSS_446/VSS_526 VSS_447/VSS_527 VSS_448/VSS_528 VSS_449/VSS_529 VSS_450/VSS_530 VSS_451/VSS_531 VSS_452/VSS_532 VSS_453/VSS_533 VSS_454/VSS_534 VSS_455/VSS_535 VSS_456/VSS_536 VSS_457/VSS_537 VSS_458/VSS_538 VSS_459/VSS_539 VSS_460/VSS_540 VSS_461/VSS_541 VSS_462/VSS_542 VSS_463/VSS_543 VSS_464/VSS_544 VSS_465/VSS_545 VSS_466/VSS_546 VSS_467/VSS_547 VSS_468/VSS_548 VSS_469/VSS_549 VSS_470/VSS_550 VSS_471/VSS_551 VSS_472/VSS_552 VSS_473/VSS_553 VSS_474/VSS_554 VSS_475/VSS_555 VSS_476/VSS_556 VSS_477/VSS_557 VSS_478/VSS_558 VSS_479/VSS_559 VSS_480/VSS_560 VSS_481/VSS_561 VSS_482/VSS_562 VSS_483/VSS_563 VSS_484/VSS_564 VSS_485/VSS_565 VSS_486/VSS_566 VSS_487/VSS_567 VSS_488/VSS_568 VSS_489/VSS_569 VSS_490/VSS_570 VSS_491/VSS_571
AL1 AL10 AL12 AL2 AL33 AL35 AL38 AL41 AL5 AL6 AL7 AM1 AM10 AM34 AM36 AM39 AM4 AM5 AM6 AM8 AN10 AN2 AN36 AN37 AN40 AN5 AN7 AR12 AR2 AR33 AR35 AR38 AR41 AR6 AR8 AT10 AT36 AT39 AU1 AU10 AU11 AU12 AU2 AU3 AU35 AU38 AU4 AU41 AU5 AU6 AU7 AU8 AU9 AV2 AV36 AV39 AV5 AV7 AW2 AW33 AW35 AW38 AW4 AW41 AW6 AW9 AY10 AY12 AY4 AY6 B2 B31 B34 B36 B39 B41 B6 BA1 BA10 BA2
TGL_H_CPU_IP_EXT
CPU1G
7 OF 15
BA3 BA36 BA39 BA4 BA5 BA6 BA7 BA8 BA9 BB33 BB35 BB38 BB41 BC34 BC37 BC39 BC40 BC41 BC5 BD2 BD35 BD38 BD4 BD6 BD9 BE10 BE12 BE2 BE36 BE37 BE38 BE39 BE40 BE41 BE7 BF1 BF10 BF3 BF33 BF4 BF5 BF6 BF8 BF9 BG2 BG36 BG39 BG5 BG7 BH12 BH2 BH36 BH39 BH7 BJ36 BJ39 BJ40 BJ41 BK10 BK33 BK36 BK37 BK38 BK39 BL1 BL10 BL2 BL3 BL36 BL39 BL4 BL5 BL6 BL7 BL8 BL9 BM12 BM5 BN2 BN33
VSS_252/VSS_332 VSS_253/VSS_333 VSS_254/VSS_334 VSS_255/VSS_335 VSS_256/VSS_336 VSS_257/VSS_337 VSS_258/VSS_338 VSS_259/VSS_339 VSS_260/VSS_340 VSS_261/VSS_341 VSS_262/VSS_342 VSS_263/VSS_343 VSS_264/VSS_344 VSS_265/VSS_345 VSS_266/VSS_346 VSS_267/VSS_347 VSS_268/VSS_348 VSS_269/VSS_349 VSS_270/VSS_350 VSS_271/VSS_351 VSS_272/VSS_352 VSS_273/VSS_353 VSS_274/VSS_354 VSS_275/VSS_355 VSS_276/VSS_356 VSS_277/VSS_357 VSS_278/VSS_358 VSS_279/VSS_359 VSS_280/VSS_360 VSS_281/VSS_361 VSS_282/VSS_362 VSS_283/VSS_363 VSS_284/VSS_364 VSS_285/VSS_365 VSS_286/VSS_366 VSS_287/VSS_367 VSS_288/VSS_368 VSS_289/VSS_369 VSS_290/VSS_370 VSS_291/VSS_371 VSS_292/VSS_372 VSS_293/VSS_373 VSS_294/VSS_374 VSS_295/VSS_375 VSS_296/VSS_376 VSS_297/VSS_377 VSS_298/VSS_378 VSS_299/VSS_379 VSS_300/VSS_380 VSS_301/VSS_381 VSS_302/VSS_382 VSS_303/VSS_383 VSS_304/VSS_384 VSS_305/VSS_385 VSS_306/VSS_386 VSS_307/VSS_387 VSS_308/VSS_388 VSS_309/VSS_389 VSS_310/VSS_390 VSS_311/VSS_391 VSS_312/VSS_392 VSS_313/VSS_393 VSS_314/VSS_394 VSS_315/VSS_395 VSS_316/VSS_396 VSS_317/VSS_397 VSS_318/VSS_398 VSS_319/VSS_399 VSS_320/VSS_400 VSS_321/VSS_401 VSS_322/VSS_402 VSS_323/VSS_403 VSS_324/VSS_404 VSS_325/VSS_405 VSS_326/VSS_406 VSS_327/VSS_407 VSS_328/VSS_408 VSS_329/VSS_409 VSS_330/VSS_410 VSS_331/VSS_411
BN36 BN39 BN4 BN40 BN41 BN6 BN8 BP10 BP12 BP36 BP39 BR1 BR10 BR2 BR3 BR36 BR37 BR38 BR39 BR4 BR5 BR6 BR7 BR8 BR9 BT12 BT36 BT39 BT40 BT41 BT5 BU33 BU36 BU39 BV2 BV4 BV6 BV9 BW10 BW36 BW39 BY1 BY10 BY3 BY36 BY37 BY38 BY39 BY4 BY40 BY41 BY5 BY6 BY8 BY9 C1 C10 C13 C16 C18 C22 C25 C28 C3 C31 C32 C34 C8 CA10 CA12 CA13 CA17 CA2 CA21 CA24 CA28 CA33 CA5 CA7 CB36
TGL_H_CPU_IP_EXT
CPU1H
8 OF 15
CB39 CC10 CC2 CC36 CC39 CC5 CC7 CD10 CD13 CD17 CD2 CD21 CD24 CD28 CD33 CD36 CD39 CD40 CD41 CD5 CD7 CE1 CE10 CE17 CE21 CE24 CE28 CE3 CE33 CE36 CE37 CE38 CE39 CE4 CE5 CE6 CE8 CE9 CF10 CF12 CF2 CF5 CF7 CG13 CH10 CH12 CH13 CH14 CH16 CH17 CH18 CH2 CH20 CH21 CH22 CH23 CH25 CH30 CH31 CH35 CH36 CH40 CH41 CH5 CH7 CJ10 CJ13 CJ18 CJ2 CJ23 CJ25 CJ5 CJ7 CK1 CK10 CK13 CK18 CK23 CK3 CK4
VSS_92 VSS_172 VSS_93 VSS_173 VSS_94 VSS_174 VSS_95 VSS_175 VSS_96 VSS_176 VSS_97 VSS_177 VSS_98 VSS_178 VSS_99 VSS_179 VSS_100/VSS_180 VSS_101/VSS_181 VSS_102/VSS_182 VSS_103/VSS_183 VSS_104/VSS_184 VSS_105/VSS_185 VSS_106/VSS_186 VSS_107/VSS_187 VSS_108/VSS_188 VSS_109/VSS_189 VSS_110/VSS_190 VSS_111/VSS_191 VSS_112/VSS_192 VSS_113/VSS_193 VSS_114/VSS_194 VSS_115/VSS_195 VSS_116/VSS_196 VSS_117/VSS_197 VSS_118/VSS_198 VSS_119/VSS_199 VSS_120/VSS_200 VSS_121/VSS_201 VSS_122/VSS_202 VSS_123/VSS_203 VSS_124/VSS_204 VSS_125/VSS_205 VSS_126/VSS_206 VSS_127/VSS_207 VSS_128/VSS_208 VSS_129/VSS_209 VSS_130/VSS_210 VSS_131/VSS_211 VSS_132/VSS_212 VSS_133/VSS_213 VSS_134/VSS_214 VSS_135/VSS_215 VSS_136/VSS_216 VSS_137/VSS_217 VSS_138/VSS_218 VSS_139/VSS_219 VSS_140/VSS_220 VSS_141/VSS_221 VSS_142/VSS_222 VSS_143/VSS_223 VSS_144/VSS_224 VSS_145/VSS_225 VSS_146/VSS_226 VSS_147/VSS_227 VSS_148/VSS_228 VSS_149/VSS_229 VSS_150/VSS_230 VSS_151/VSS_231 VSS_152/VSS_232 VSS_153/VSS_233 VSS_154/VSS_234 VSS_155/VSS_235 VSS_156/VSS_236 VSS_157/VSS_237 VSS_158/VSS_238 VSS_159/VSS_239 VSS_160/VSS_240 VSS_161/VSS_241 VSS_162/VSS_242 VSS_163/VSS_243 VSS_164/VSS_244 VSS_165/VSS_245 VSS_166/VSS_246 VSS_167/VSS_247 VSS_168/VSS_248 VSS_169/VSS_249 VSS_170/VSS_250 VSS_171/VSS_251
CK5 CK6 CK8 CK9 CL12 CL14 CL16 CL17 CL20 CL21 CL22 CL23 CL24 CL25 CL30 CL31 CL35 CL36 CM10 CM13 CM18 CM2 CM23 CM40 CM41 CM5 CM7 CN1 CN10 CN12 CN13 CN14 CN16 CN17 CN18 CN20 CN21 CN22 CN23 CN4 CN5 CN7 CP1 CP14 CP2 CP20 CP27 CP3 CP31 CP32 CP35 CP36 CP5 CP7 CP8 CP9 CR1 CR14 CR20 CR27 CR41 CR5 CR9 CT1 CT11 CT12 CT13 CT16 CT17 CT18 CT2 CT20 CT22 CT27 CT5 CT7 CT8 CU14 CU2 CU20
TGL_H_CPU_IP_EXT
CPU1I
9 OF 15
CU27 CU3 CU31 CU32 CU35 CU36 CU4 CU40 CU5 CU9 D11 D14 D17 D20 D23 D27 D29 D31 D37 D4 D40 D5 D9 E11 E31 E36 E39 E41 E5 E6 F10 F11 F13 F16 F18 F22 F25 F28 F31 F40 F6 F8 G1 G10 G13
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45
VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91
G15 G17 G18 G20 G22 G24 G26 G28 G29 G3 G31 G33 G34 G37 G4 G5 G6 G8 G9 H10 H15 H18 H2 H22 H26 H29 H33 H38 H5 H7 J33 J34 J36 J39 K10 K11 K13 K17 K2 K20 K24 K28 K31 K5 K7 L10
TGL_H_CPU_IP_EXT
同方国际信息技术有限公司
Title
TGL_H GND
Size B
Document Number
GM5TGFX
Rev 1.2
Date: Tuesday, May 18, 2021
Sheet 15 of 78

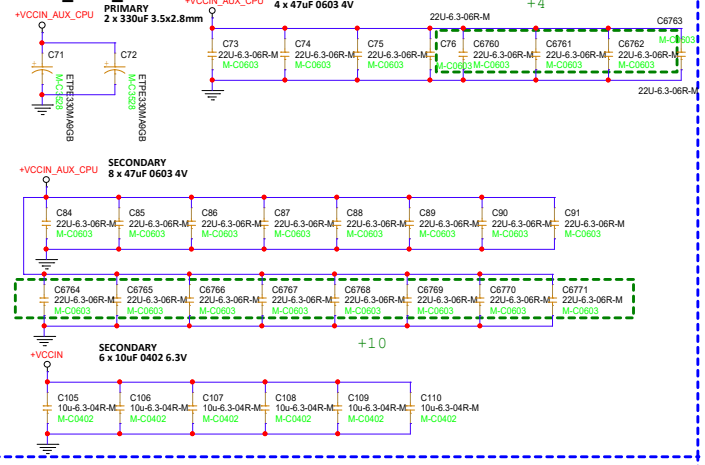
CPU CAPS

+VCCIN

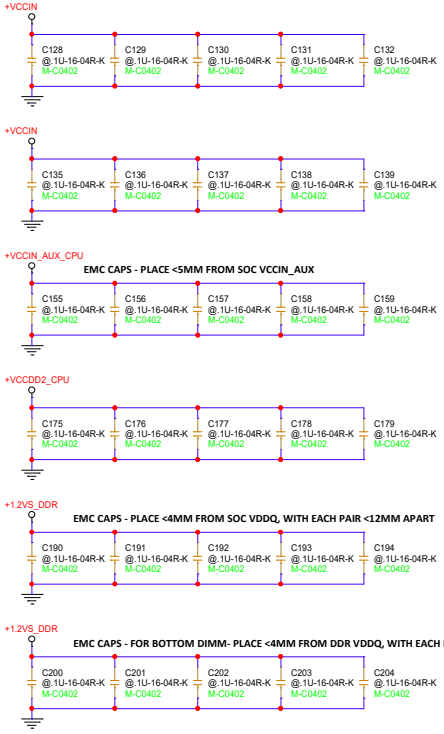


CAP ADDED FOR PI SIMULATION AS PER PI FEEDBACK

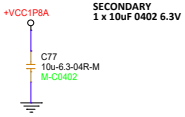
+VCCIN_AUX_CPU



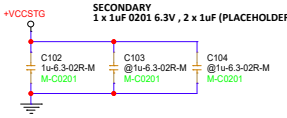
EMC CAPS



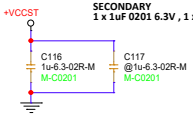
+VCC1P8A



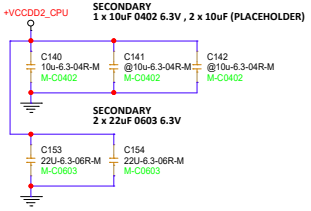
+VCCSTG



+VCCST



+VCCDD2_CPU



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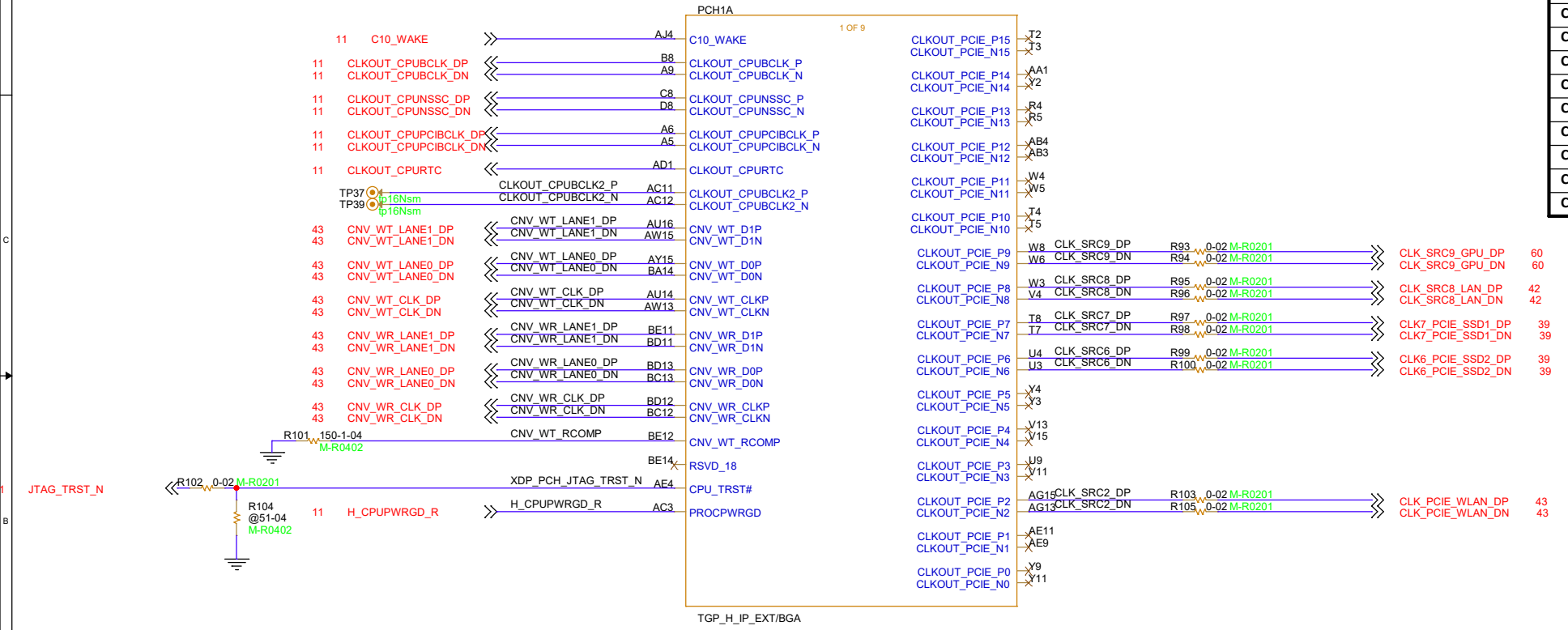
Title	TGL_H CAP	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 16 of 78	

PCIE CLKOUT Configuration Table	
CLKOUT_PCIE0	N/A
CLKOUT_PCIE1	N/A
CLKOUT_PCIE2	WLAN
CLKOUT_PCIE3	N/A
CLKOUT_PCIE4	N/A
CLKOUT_PCIE5	N/A
CLKOUT_PCIE6	SSD2
CLKOUT_PCIE7	SSD1
CLKOUT_PCIE8	LAN
CLKOUT_PCIE9	GPU
CLKOUT_PCIE10	N/A
CLKOUT_PCIE11	N/A
CLKOUT_PCIE12	N/A
CLKOUT_PCIE13	N/A
CLKOUT_PCIE14	N/A
CLKOUT_PCIE15	N/A



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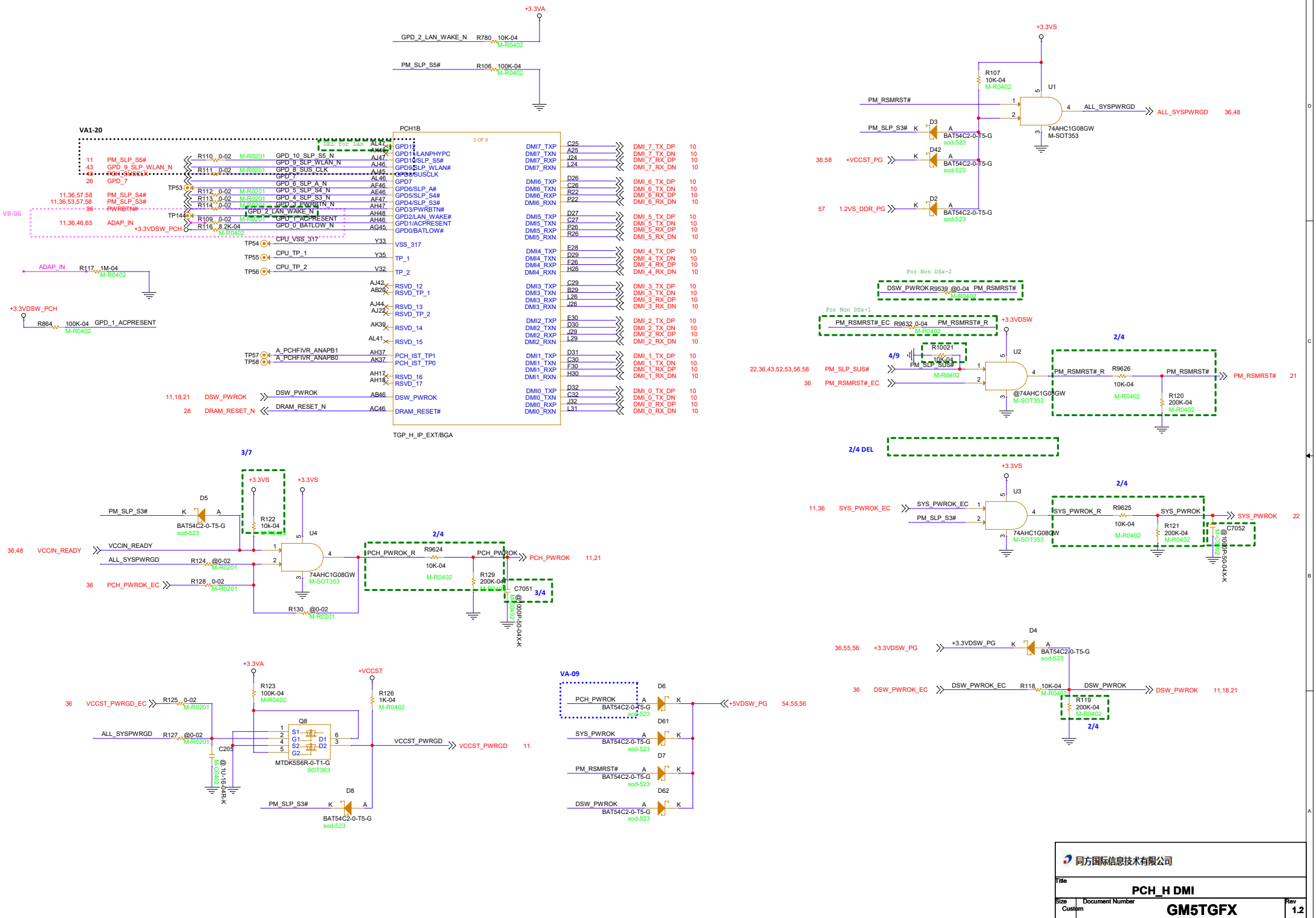
Title	PCH_H CLOCK/CNVI	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 17 of 78	


+3.3VA
GPD_2_LAN_WAKE_N
R780 10K-04 M-R0402
PM_SLP_S5#
R106 100K-04 M-R0402
VA1-20
PCH1B
2 OF 9
DEL for Lan
PM_SLP_S5#
GPD_9_SLP_WLAN_N
GPD_8_SUS_CLK
GPD_7
GPD_6_SLP_A_N
GPD_5_SLP_S4_N
GPD_4_SLP_S3_N
GPD_3_PWRBTN_N
GPD_2_LAN_WAKE_N
GPD_1_ACPRESENT
GPD_0_BATLOW_N
R110 0-02 M-R0201
R111 0-02 M-R0201
R112 0-02 M-R0201
R113 0-02 M-R0201
R114 0-02 M-R0201
R109 0-02 M-R0201
R116 8.2K-04 M-R0402
+3.3VDSW_PCH
GPD12
GPD11/LANPHYPC
GPD10/SLP_S5#
GPD9/SLP_WLAN#
GPD8/SUSCLK
GPD7
GPD6/SLP_A#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD3/PWRBTN#
GPD2/LAN_WAKE#
GPD1/ACPRESENT
GPD0/BATLOW#
CPU_VSS_317
CPU_TP_1
CPU_TP_2
VSS_317
TP_1
TP_2
RSVD_12
RSVD_TP_1
RSVD_13
RSVD_TP_2
RSVD_14
RSVD_15
PCH_IST_TP1
PCH_IST_TP0
RSVD_16
RSVD_17
DSW_PWROK
DRAM_RESET#
TGP_H_IP_EXT/BGA
DMI7_TXP
DMI7_TXN
DMI7_RXP
DMI7_RXN
DMI6_TXP
DMI6_TXN
DMI6_RXP
DMI6_RXN
DMI5_TXP
DMI5_TXN
DMI5_RXP
DMI5_RXN
DMI4_TXP
DMI4_TXN
DMI4_RXP
DMI4_RXN
DMI3_TXP
DMI3_TXN
DMI3_RXP
DMI3_RXN
DMI2_TXP
DMI2_TXN
DMI2_RXP
DMI2_RXN
DMI1_TXP
DMI1_TXN
DMI1_RXP
DMI1_RXN
DMI0_TXP
DMI0_TXN
DMI0_RXP
DMI0_RXN
ADAP_IN
R117 1M-04 M-R0402
R864 100K-04 GPD_1_ACPRESENT M-R0402
+3.3VS
R107 10K-04 M-R0402
U1
PM_RSMRST#
PM_SLP_S3#
D3
D42
D2
BAT54C2-0-T5-G sod-523
+VCCST_PG
1.2VS_DDR_PG
74AHC1G08GW M-SOT353
ALL_SYSPWRGD
For Non DSx-2
DSW_PWROK R9539 @0-04 PM_RSMRST# M-R0402
For Non DSx-1
PM_RSMRST#_EC R9632 0-04 PM_RSMRST#_R M-R0402
+3.3VDSW
2/4
4/9
R10021 10K-04
PM_SLP_SUS#
U2
@74AHC1G08GW M-SOT353
R9626 10K-04 M-R0402
R120 200K-04 M-R0402
3/7
D5
U4
R122 10k-04 M-R0402
VCCIN_READY
ALL_SYSPWRGD
PCH_PWROK_EC
R124 @0-02 M-R0201
R128 0-02 M-R0201
R130 @0-02 M-R0201
R9624 10K-04 M-R0402
R129 200K-04 M-R0402
C7051 @ 1000P-50-04X-K M-C0402
3/4
2/4 DEL
U3
SYS_PWROK_EC
SYS_PWROK_R
R9625 10K-04 M-R0402
R121 200K-04 M-R0402
C7052 @ 1000P-50-04X-K M-C0402
+3.3VA
+VCCST
R123 100K-04 M-R0402
R126 1K-04 M-R0402
Q8
MTDK5S6R-0-T1-G SOT363
R125 0-02 M-R0201
R127 @0-02 M-R0201
C205 @ 1U-16-04R-K M-C0402
VCCST_PWRGD
D8
VA-09
D6
D61
D7
D62
+5VDSW_PG
D4
+3.3VDSW_PG
R118 10K-04 M-R0402
R119 200K-04 M-R0402
同方国际信息技术有限公司
PCH_H DMI
GM5TGFX
1.2
Tuesday, May 18, 2021
18 of 78

SRCCLKREQ Configuration Table	
SRCCLKREQ6#	SSD2
SRCCLKREQ7#	SSD1
SRCCLKREQ8#	LAN
SRCCLKREQ9#	GPU
SRCCLKREQ10#	N/A
SRCCLKREQ11#	N/A
SRCCLKREQ12#	N/A
SRCCLKREQ13#	N/A
SRCCLKREQ14#	N/A
SRCCLKREQ15#	N/A

GPP_R2/HDA_SDO	Flash Descriptor Security Override
0	ME Enable security (Default)
1	ME Disabled security

GPP_R2_HDA_SDO_0

36 MELOCK# — R131 1K-1-04 M-R0402

PCH1C

3 OF 9

GPP_S7/SNDW4_DATA/DMIC_DATA0
GPP_S6/SNDW4_CLK/DMIC_CLKA0
GPP_S5/SNDW3_DATA/DMIC_DATA1
GPP_S4/SNDW3_CLK/DMIC_CLKA1
GPP_S3/SNDW2_DATA/DMIC_CLKB1
GPP_S2/SNDW2_CLK/DMIC_CLKB0
GPP_S1/SNDW1_DATA
GPP_S0/SNDW1_CLK

GPP_R19/ISH_GP5
GPP_R18/ISH_GP4
GPP_R17/ISH_GP3
GPP_R16/ISH_GP2
GPP_R15/ISH_GP1
GPP_R14/ISH_GP0
GPP_R13/ISH_GP7
GPP_R12/CLKOUT_48
GPP_R11/SX_EXIT_HOLDOFF#/ISH_GP6
GPP_R10/ISH_UART0_RTS#/GSPI2_CS1#
GPP_R9/PCIE_LNK_DOWN
GPP_R8/I2S1_SCLK
GPP_R7/I2S1_SFRM
GPP_R6/I2S1_TXD
GPP_R5/HDA_SDI/I2S1_RXD
GPP_R4/HDA_RST#
GPP_R3/HDA_SDI/I2S0_RXD/HDACPU_SDI
GPP_R2/HDA_SDO/I2S0_TXD/HDACPU_SDO
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R0/HDA_BCLK/I2S0_SCLK/HDACPU_BCLK

44 TP_INT#

TP59 TP22

GPP_R_5_HDA_SDI_1 — R9606 33-1-04 M-R0402 — GPP_R4_HDA_RST#
GPP_R3_HDA_SDI_0 — R135 33-1-04 M-R0402 — GPP_R2_HDA_SDO_0
R136 33-1-04 M-R0402 — GPP_R1_HDA_SYNC
R137 33-1-04 M-R0402 — GPP_R0_HDA_BCLK

40 HDA_RST
40 HDA_SDI_0
26,40 HDA_SDO_I2S0_TXD
40 HDA_SYNC
40 HDA_BCLK

GPP_R0_HDA_BCLK — C206 @22P-25V-C0402-CNV

43 GPP_K11_M2_CNVI_EN_N

50,52,58 GPP_K9_CORE_VID_1
50,52,58 GPP_K8_CORE_VID_0

30 GPP_K6_eDP_HPD

GPP_K11
GPP_K10/DDSP_HPDC/DISP_MISCC
GPP_K9/CORE_VID1
GPP_K8/CORE_VID0
GPP_K7/DDSP_HPDB/DISP_MISCB
GPP_K6/DDSP_HPDA/DISP_MISCA
GPP_K5/ADR_COMPLETE
GPP_K4/GSXCLK
GPP_K3/GSXSRESET#
GPP_K2/GSXDIN
GPP_K1/GSXSLOAD
GPP_K0/GSXDOUT

26 GPP_J7_CNV_MFUART2_TXD

43 GPP_J5_CNV_RGI_RSP
26,43 GPP_J4_CNV_RGI_DT
43 GPP_J3_CNV_BRI_RSP
26,43 GPP_J2_CNV_BRI_DT

GPP_J1_CPU_C10_GATEB

GPP_J9
GPP_J8
GPP_J7/CNV_MFUART2_TXD
GPP_J6/CNV_MFUART2_RXD
GPP_J5/CNV_RGI_RSP/UART0_CTS#
GPP_J4/CNV_RGI_DT/UART0_TXD
GPP_J3/CNV_BRI_RSP/UART0_RXD
GPP_J2/CNV_BRI_DT/UART0_RTS#
GPP_J1/CPU_C10_GATE#
GPP_J0/CNV_PA_BLANKING

USB_OC#_7
USB_OC#_6
USB_OC#_5
USB_OC#_4

35 USB_OC#_6
45 USB_OC#_5
45 USB_OC#_4

GPP_I14/USB_OC7#/I2C5_SCL
GPP_I13/USB_OC6#/I2C5_SDA
GPP_I12/USB_OC5#/I2C4_SCL
GPP_I11/USB_OC4#/I2C4_SDA
GPP_I10
GPP_I9
GPP_I8/DDPC_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I4/DDSP_HPD4/DISP_MISC4
GPP_I3/DDSP_HPD3/DISP_MISC3
GPP_I2/DDSP_HPD2/DISP_MISC2
GPP_I1/DDSP_HPD1/DISP_MISC1
GPP_I0/PMCALERT#

39 GPP_I9_SSD1_RST_N — +3.3VA — R9870 10K-04 M-R0402 — PMCALERT#

DEL R141/R142 for GPP_I0 I2C_PS_INT_N

TGH_H_IP_EXT/BGA

GPP_H23/TIME_SYNC0
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
GPP_H9/SRCCLKREQ15#
GPP_H8/SRCCLKREQ14#
GPP_H7/SRCCLKREQ13#
GPP_H6/SRCCLKREQ12#
GPP_H5/SRCCLKREQ11#
GPP_H4/SRCCLKREQ10#
GPP_H3/SRCCLKREQ9#
GPP_H2/SRCCLKREQ8#
GPP_H1/SRCCLKREQ7#
GPP_H0/SRCCLKREQ6#

GPP_H18_SML4ALERT_N 26
GPP_H17_SSD1_EN 39
GPP_H15_PEG_WAKE_N 26
GPP_H13_PEG_RESET# 60
GPP_H12_SMLALERT_N 26

DEL PD INT

GPP_H3_CLKREQ9_GPU_N 60
GPP_H2_CLKREQ8_LAN_N 42
GPP_H1_CLKREQ7_SSD1_N 39
GPP_H0_CLKREQ6_SSD2_N 39

GPP_F23 — Remove GPP_F23_PCH_LAN_RST#

GPP_F22/vNN_CTRL
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN
GPP_F18/M2_SKT2_CFG3
GPP_F17/M2_SKT2_CFG2
GPP_F16/M2_SKT2_CFG1
GPP_F15/M2_SKT2_CFG0
GPP_F14/PS_ON#
GPP_F13/SATA_SDATAOUT0
GPP_F12/SATA_SDATAOUT1
GPP_F11/SATA_SLOAD
GPP_F10/SATA_SCLOCK
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
GPP_F4/SATAXPCIE7/SATAGP7
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F0/SATAXPCIE3/SATAGP3

GPP_F18_LCDVDD_RST#

Remove GPP_F17_LANDISABLE#

GPP_F15_SKTOCC_N — R140 0-02 M-R0201 — SKTOCC_N 11

GPP_F12_Wlan_ON 43
GPP_F10_BIOS_REC 26
GPP_F9_WIFI_WAKE# 43

wlan_wake up

GPIO_SD 45

USB_OC#_3

GPP_E12/USB_OC3#
GPP_E11/USB_OC2#
GPP_E10/USB_OC1#
GPP_E9/USB_OC0#
GPP_E8/SATALED#/SPI1_CS1#
GPP_E7/CPU_GP1
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_E3/CPU_GP0
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E0/SATAXPCIE0/SATAGP0

GPP_E11_U2_OC#_AUDIO 26
GPP_E10_U2_OC#_USB 26
GPP_E9_U2_OC#_TYPE_C 26

GPP_E5_SATA_DEVSLP_1 39

GPP_E2_SATAHDD_GP2 — VB-06

GPP_E3_EC_SMI# 36

GPP_E1_M.2_SSD2_PEDET 39
GPP_E0_SATAXPCIE_0_SATAGP_0 26

DEL PD INT

For MS — +3.3VA — R9570 @100K-04 M-R0402 — +3.3V — R132 @100K-04 M-R0402 — GPP_H13_PEG_RESET#

+3.3V — R133 100K-04 M-R0402 — GPP_F18_LCDVDD_RST#

GPP_F20_L_BKLT_EN
GPP_F19_L_VDD_EN

R138 100K-04 M-R0402
R139 100K-04 M-R0402

+3.3VA

USB_OC#_7 — R143 10K-04 M-R0402
USB_OC#_6 — R144 10K-04 M-R0402
USB_OC#_5 — R145 10K-04 M-R0402
USB_OC#_4 — R146 10K-04 M-R0402
USB_OC#_3 — R147 10K-04 M-R0402
GPP_H2_CLKREQ8_LAN_N — R148 @10K-04 M-R0402

+3.3V — R9536 @10K-04 M-R0402 — GPP_E2_SATAHDD_GP2

GPP_E3_EC_SMI#

+3.3VS — R1583 @10K-04 M-R0402

3/7

+3.3V — R149 10K-04 M-R0402 — +1.8V

C207 1U-16-04R-K M-C0402

U5

11,58 CPU_C10_GATE# — CPU_C10_GATE# — 74AUP1G07GW M-SOT353 — GPP_J1_CPU_C10_GATEB

5/15

+3.3V — R10028 @100K-04 — GPP_J1_CPU_C10_GATEB

Q280 @MTDK5S6R-0-T1-G
MTDK5S6R
VGS(th) max=+1.5V

R10029 @10K-04 — +3.3V — CPU_C10_GATE#

Title	PCH_H GPIO	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 19 of 78	

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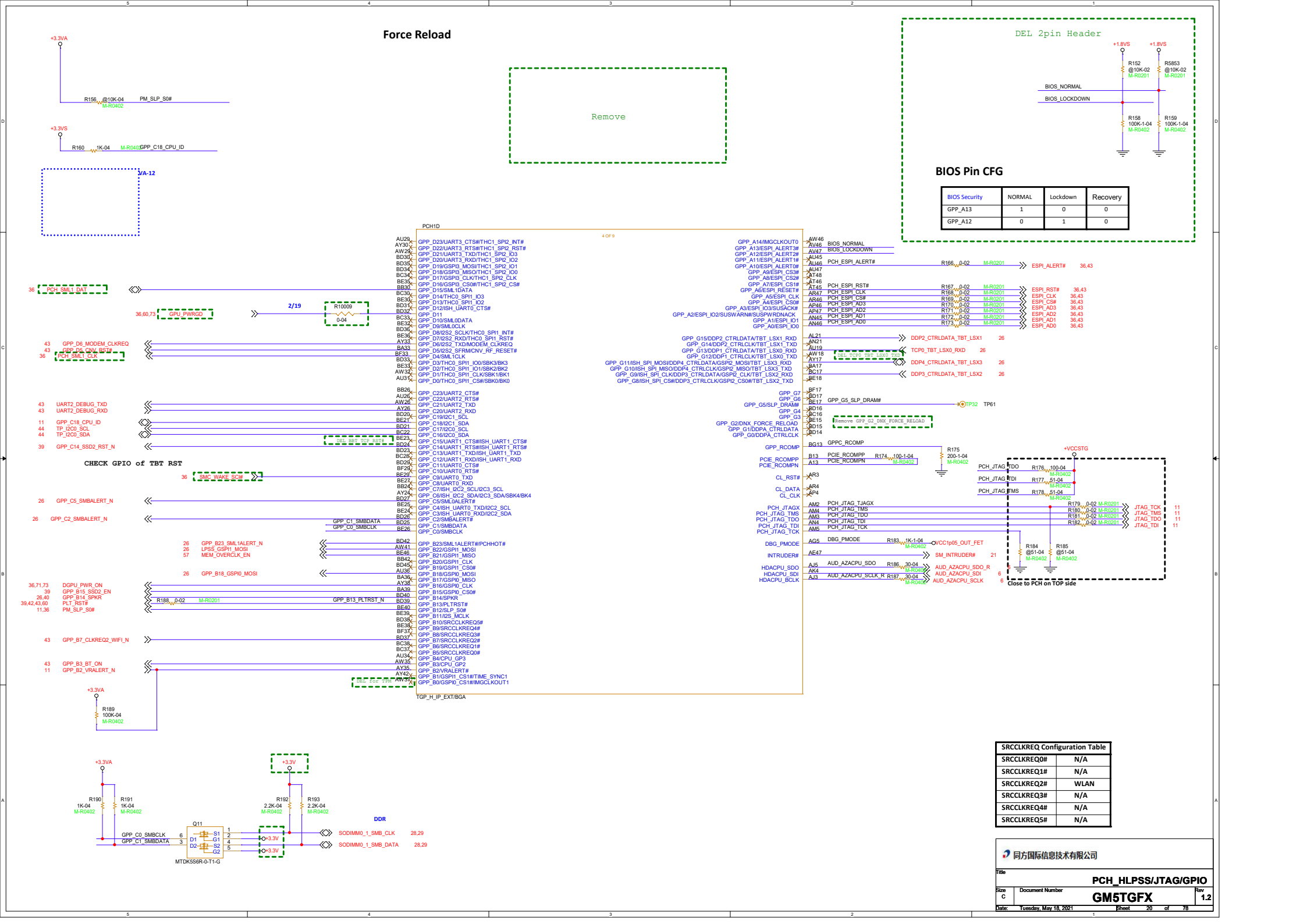
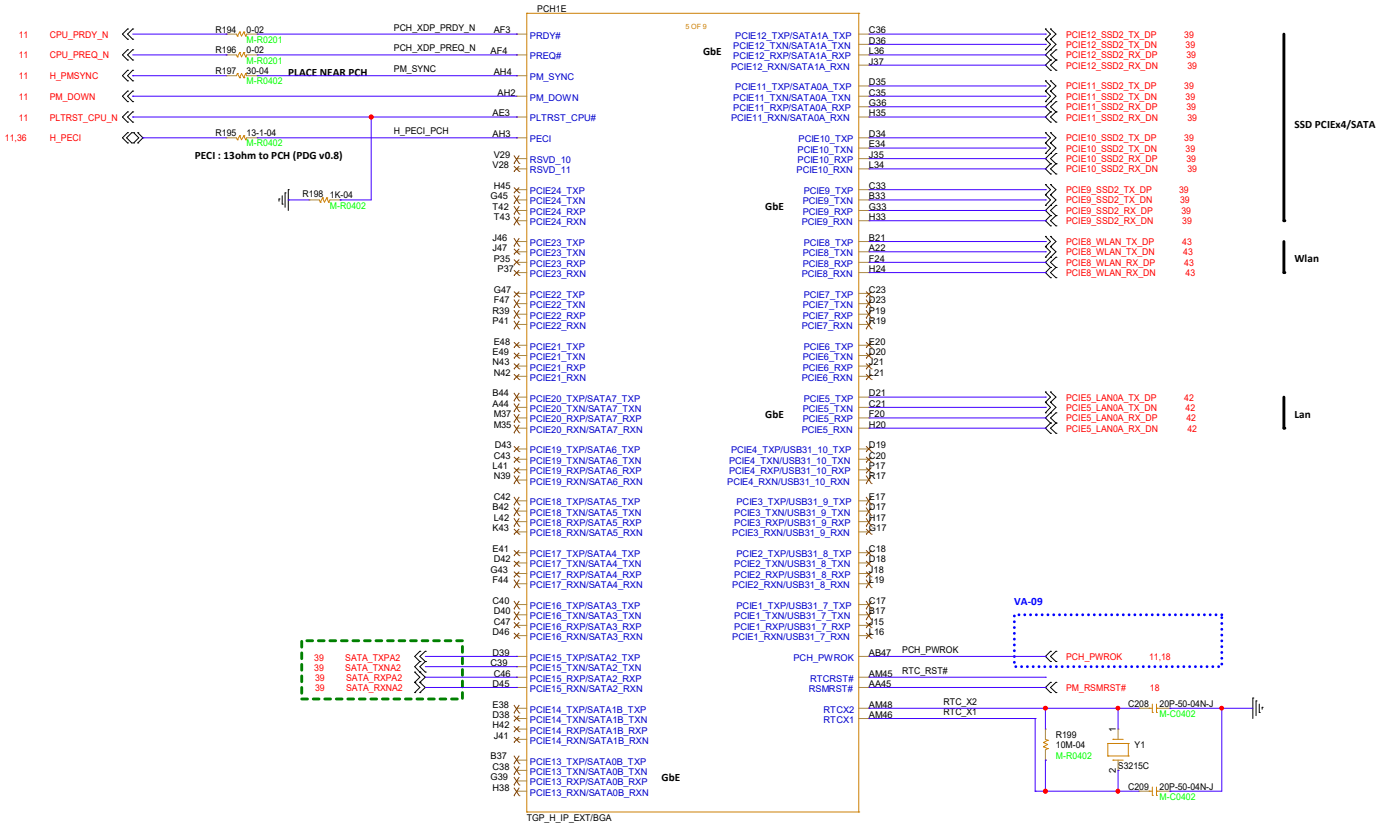
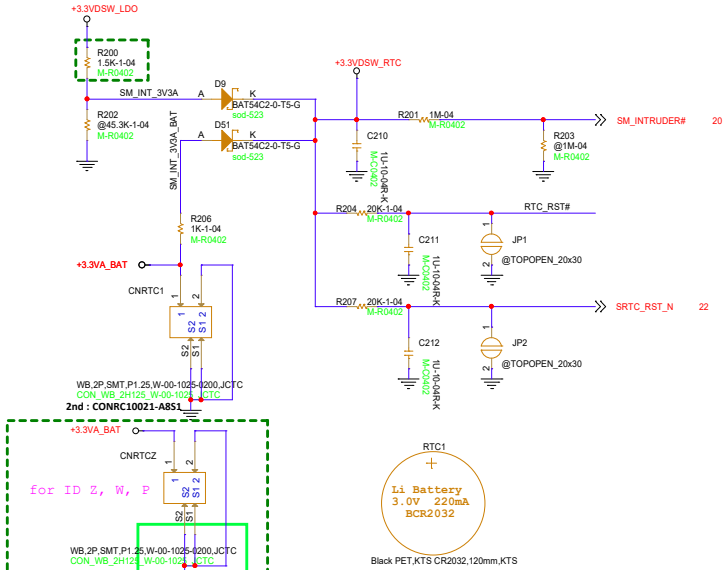

Force Reload
Remove
DEL 2pin Header
BIOS Pin CFG
BIOS Security | NORMAL | Lockdown | Recovery
GPP_A13 | 1 | 0 | 0
GPP_A12 | 0 | 1 | 0
CHECK GPIO of TBT RST
SRCCLKREQ Configuration Table
SRCCLKREQ0# N/A
SRCCLKREQ1# N/A
SRCCLKREQ2# WLAN
SRCCLKREQ3# N/A
SRCCLKREQ4# N/A
SRCCLKREQ5# N/A
同方国际信息技术有限公司
PCH_HLPSS/JTAG/GPIO
GM5TGFX
Size C
Rev 1.2
Tuesday, May 18, 2021
Sheet 20 of 78

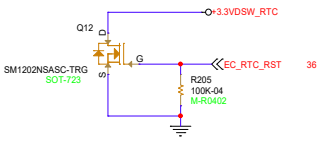


PCH PCIE Configuration Table		
PCIE1	N/A	
PCIE2	N/A	
PCIE3	N/A	
PCIE4	N/A	
PCIE5	LAN	Gen 2 by 1
PCIE6	N/A	
PCIE7	N/A	
PCIE8	WLAN	Gen 2 by 1
PCIE9 PCIE10 PCIE11 PCIE12	SSD2	Gen 3 by 4 or SATA
PCIE13	N/A	
PCIE14	N/A	
PCIE15	SATA HDD	
PCIE16	N/A	
PCIE17	N/A	
PCIE18	N/A	
PCIE19	N/A	
PCIE20	N/A	
PCIE21	N/A	
PCIE22	N/A	
PCIE23	N/A	
PCIE24	N/A	

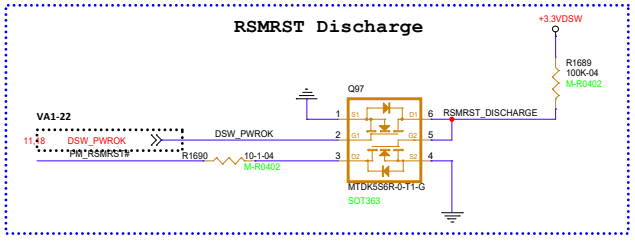
SUS Battery



CLEAR CMOS



VA-21



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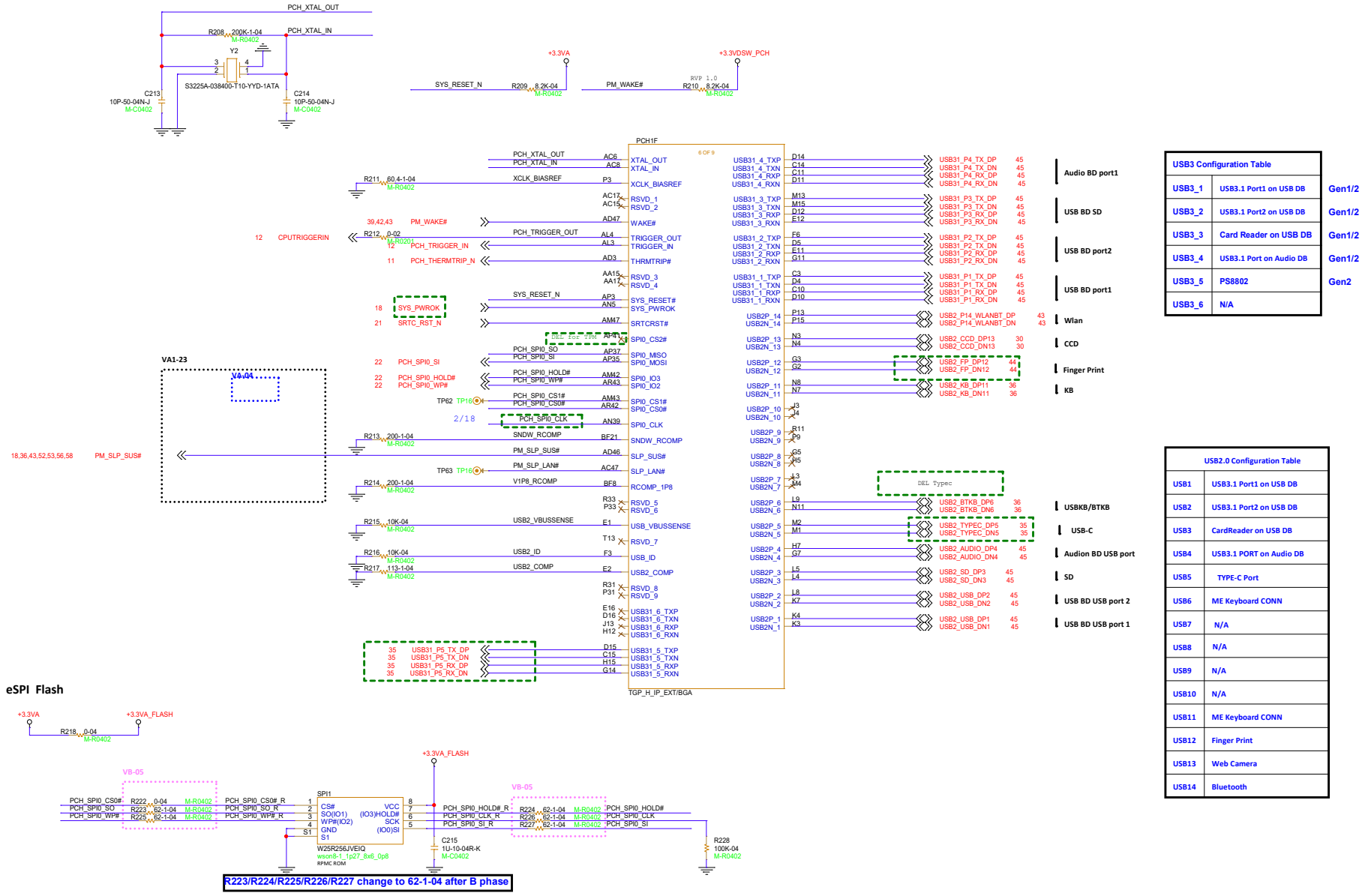
Title	PCH_H HSIO PCIE/RTC		
Size C	Document Number GM5TGFX		Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 21 of 78		



USB3 Configuration Table		
USB3_1	USB3.1 Port1 on USB DB	Gen1/2
USB3_2	USB3.1 Port2 on USB DB	Gen1/2
USB3_3	Card Reader on USB DB	Gen1/2
USB3_4	USB3.1 Port on Audio DB	Gen1/2
USB3_5	PS8802	Gen2
USB3_6	N/A	

USB2.0 Configuration Table	
USB1	USB3.1 Port1 on USB DB
USB2	USB3.1 Port2 on USB DB
USB3	CardReader on USB DB
USB4	USB3.1 PORT on Audio DB
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	N/A
USB10	N/A
USB11	ME Keyboard CONN
USB12	Finger Print
USB13	Web Camera
USB14	Bluetooth

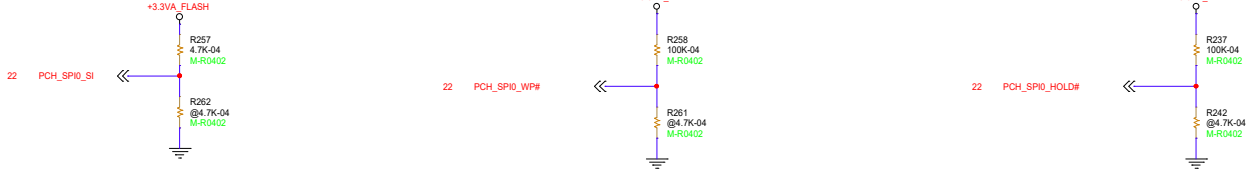
eSPI Flash

R223/R224/R225/R226/R227 change to 62-1-04 after B phase

SPI0_MOSI	Reserved
External pull-up is required. Recommend 4.7 kOhm pull up. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling	

SPI0_IO2	Reserved
External pull-up is required. Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.	

SPI0_IO3	Reserved
External pull-up is required. Recommend 100 K if pulled up to 3.3 V or 75 K if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.	



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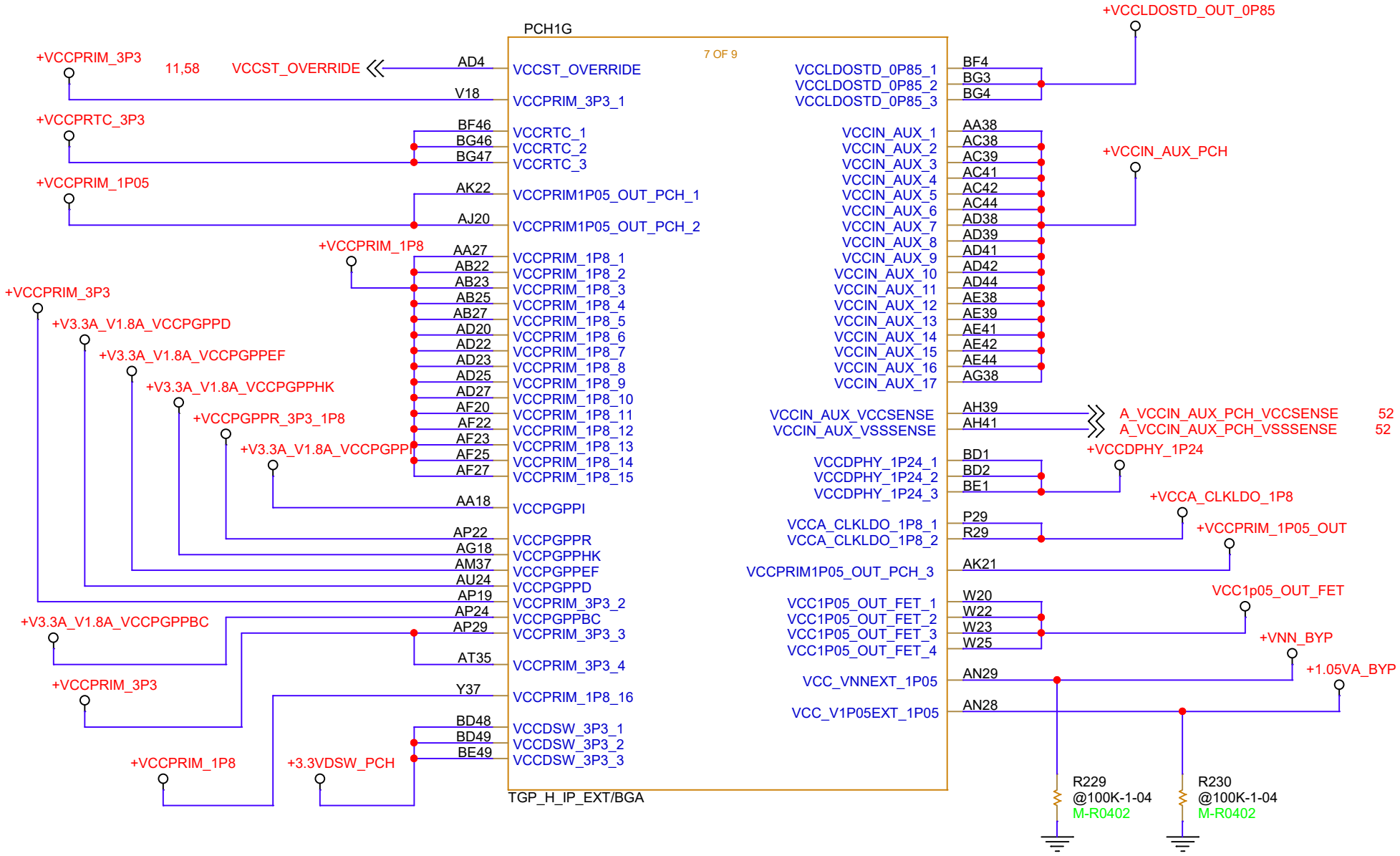
Title: PCH_H HSIO USB/BIOS

Size: C | Document Number: GM5TGFX | Rev: 1.2

Date: Tuesday, May 18, 2021 | Sheet 22 of 78



GPIO Group	PCH_GPIO_rail	Power_rail	Voltage
Primary Well Group A	N/A	BIOS SETTING	BIOS SETTING
Primary Well Group B/C	VCCPGPPBC	+V3.3A_V1.8A_VCCPGPPBC	+3.3VA
Primary Well Group D	VCCPGPPD	+V3.3A_V1.8A_VCCPGPPD	+1.8VA
Primary Well Group E/F	VCCPGPPEF	+V3.3A_V1.8A_VCCPGPPEF	+3.3VA
Primary Well Group G	N/A	BIOS SETTING	BIOS SETTING
Primary Well Group H/K	VCCPGPPHK	+V3.3A_V1.8A_VCCPGPPHK	+3.3VA
Primary Well Group I	VCCPGPPI	+V3.3A_V1.8A_VCCPGPPI	+3.3VA
Primary Well Group J	VCCPRIM_1P8	VCCPRIM_1P8	+1.8VA Only
Primary Well Group R	VCCPGPPR	VCCPGPPR	+3.3VA
Primary Well Group S	VCCPRIM_1P8	VCCPRIM_1P8	+1.8VA Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	VCCDSW_3P3	+3.3VA Only

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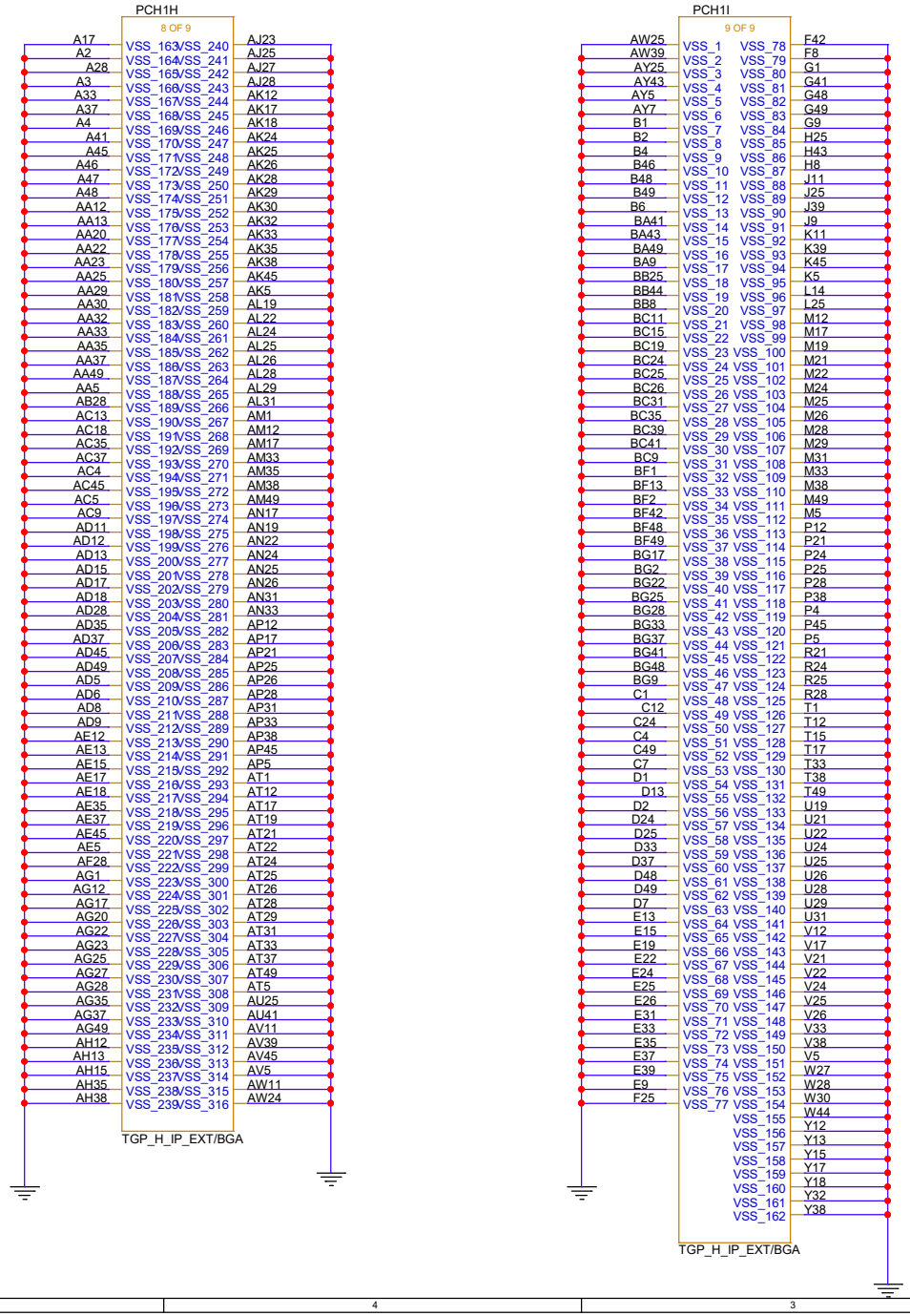
Title: PCH_H POWER

Size: A | Document Number: GM5TGFX | Rev: 1.2

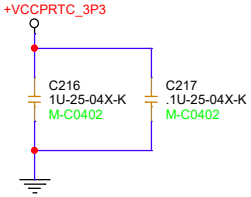
Date: Tuesday, May 18, 2021 | Sheet 23 of 78



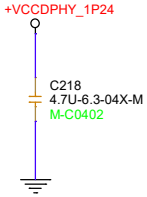
同方国际信息技术有限公司

Title	PCH_H GND	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 24 of 78	

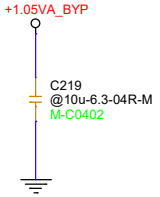
+VCCPRTC_3P3



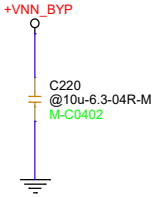
+VCCDPHY_1P24



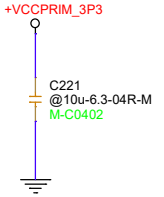
+VCC_V1P05EXT_1P05



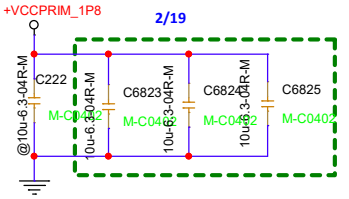
+VCC_VNNEXT_1P05



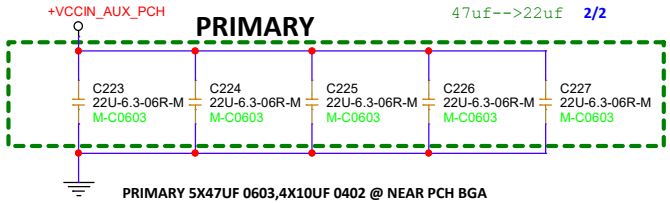
+VCCPRIM_3P3

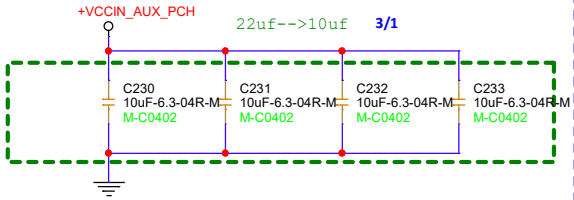


+VCCPRIM_1P8

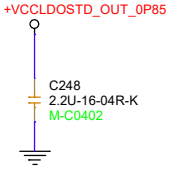


TGL-H RVP MPI SOCKET STUFFING

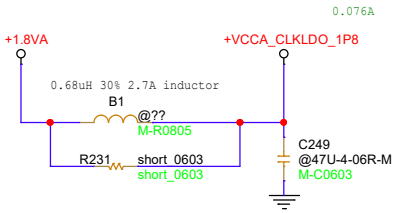




+VCCLDOSTD_OUT_0P85



+VCCA_CLKLDO_1P8



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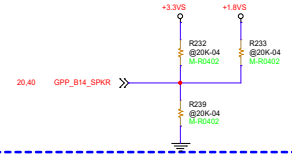
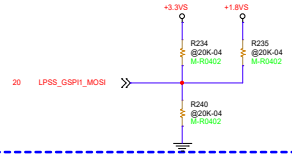
Title	PCH_H CAP		
Size B	Document Number GM5TGFX		Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 25 of 78		

PCH STRAPS

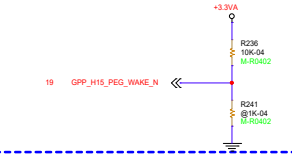
GPP_B14/SPKR	Top Swap Override This strap has a 20 kohm ∓ 30% internal pull-down.
0	Disable Top Swap mode(Default)
1	Enable Top Swap mode.



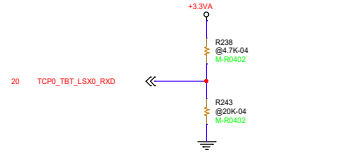
GPP_B22/GSPI1_MOSI	Boot BIOS Strap (BBS) This strap has a 20 kohm ∓ 30% internal pull-down.
0	BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF)
1	BIOS fetches are routed to the eSPI Peripheral Channe



GPP_H15/SML3ALERT#	Reserved This strap has a 20 kohm ∓ 30% internal pull-down.
0	JTAG ODT is disabled
1	JTAG ODT is enabled

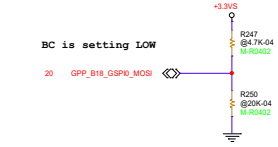


GPP_G13/DDP1_CTRLDATA /TBT_LSX0_RXD	DDP1 I2C /TBT_LSX0 /BSSB_LS0 pins VCC configuration This strap has a 20 kohm ∓ 30% internal pull-down.
0	DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V
1	DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V



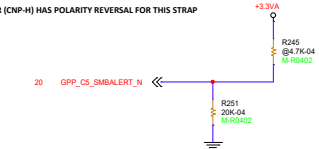
GPP_B18/GSPI0_MOSI	No Reboot This strap has a 20 kohm ∓ 30% internal pull-down.
0	No Reboot mode. (Default)
1	Enable No Reboot mode.

BC is setting LOW



GPP_C5/SML0ALERT#	eSPI Disable This strap has a 20 kohm ∓ 30% internal pull-down.
0	eSPI. (Default)
1	Disable eSPI

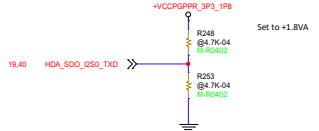
INTERPOSER (CNP-H) HAS POLARITY REVERSAL FOR THIS STRAP



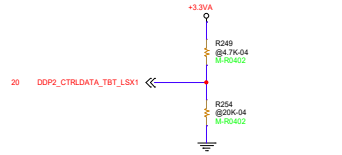
GPP_B23/SML1ALERT#/ PCHHOT#	CPUNSSC Clock Frequency This strap has a 20 kohm ∓ 30% internal pull-down.
0	38.4 MHz clock (direct from crystal) (default)
1	19.2 MHz clock (derived from 38.4 MHz crystal)

GPP_R2/HDA_SDO/I2S0_TXD/ HDACPU_SDO	Flash Descriptor Security Override This strap has a 20 kohm ∓ 30% internal pull-down.
0	Enable security measures defined in the Flash Descriptor. (Default)
1	Disable Flash Descriptor Security (override)

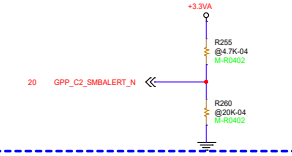
This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.



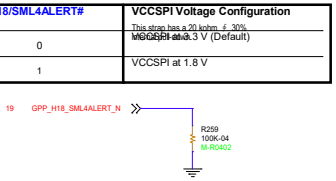
GPP_G15/DDP2_CTRLDATA/ TBT_LSX1_RXD	DDP2 I2C /TBT_LSX1 /BSSB_LS01 pins VCC configuration This strap has a 20 kohm ∓ 30% internal pull-down.
0	DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V
1	DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V



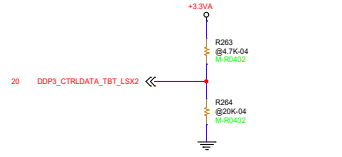
GPP_C2/SMBALERT#	TLS Confidentiality This strap has a 20 kohm ∓ 30% internal pull-down.
0	TLS cipher suite (no confidentiality). (Default)
1	Enable TLS cipher suite (no confidentiality).



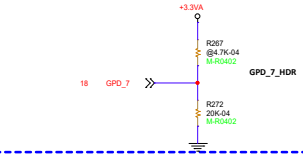
GPP_H18/SML4ALERT#	VCCSPI Voltage Configuration This strap has a 20 kohm ∓ 30% internal pull-down.
0	VCCSPI at 3.3 V (Default)
1	VCCSPI at 1.8 V



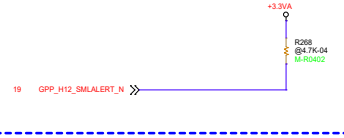
GPP_G9/ISH_SPI_CLK/DDP3_ CTRLDATA/GSPI2_CLK/TBT_ LSX2_RXD	DDP3 I2C /TBT_LSX2 /BBSB_LS2 pins VCC configuration This strap has a 20 kohm ∓ 30% internal pull-down.
0	DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1	DDP3 I2C / TBT_LSX2 / BBSB_LS2_TX pins at 3.3V



GPD7	Reserved
This strap has a 20 kOhm ∓ 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.	

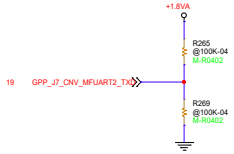


GPP_H12/SML2ALERT#	eSPI Flash Sharing Mode This strap has a 20 kohm ∓ 30% internal pull-down.
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled



GPP_J7_CNV_MFUART2_TXD

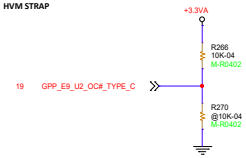
FOR CNL-H INTERPOSER ONLY



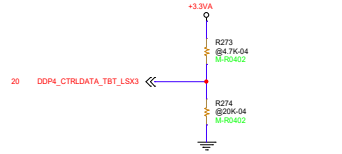
GPP_E9_USB2_OCB_0

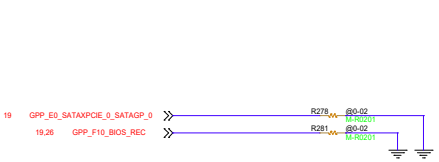
RING OSCILLATOR BYPASS

HVM STRAP

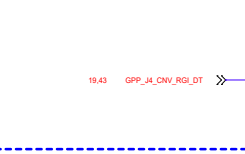


GPP_G11/ISH_SPI_MOSI/DDP4 _CTRLDATA/GSPI2_MOSI/TBT _LSX3_RXD	DDP4 I2C /TBT_LSX3 /BSSB_LS3 pins VCC configuration This strap has a 20 kohm ∓ 30% internal pull-down.
0	DDP4 I2C / TBT_LSX3 / BSSB_LS3 pins at 1.8V
1	DDP4 I2C /TBT_LSX3 / BSSB_LS3 pins at 3.3V





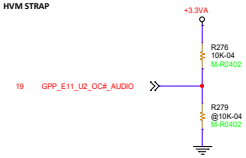
GPP_J4/CNV_RGI_DT /UART0_TXD	M.2 CNVi Mode Select This strap has a 20 kohm ∓ 30% internal pull-down.
0	Integrated CNVi enabled
1	Integrated CNVi disabled.



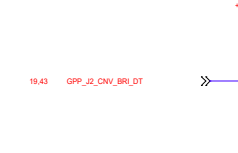
GPP_E11_USB2_OCB_2

XTAL INPUT FREQUENCY[1]

HVM STRAP



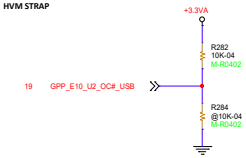
GPP_J2/CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Selection This strap has a 20 kohm ∓ 30% internal pull-down.
0	38.4 MHz (default)
1	24 MHz



GPP_E10_USB2_OCB_1

XTAL INPUT FREQUENCY[0]

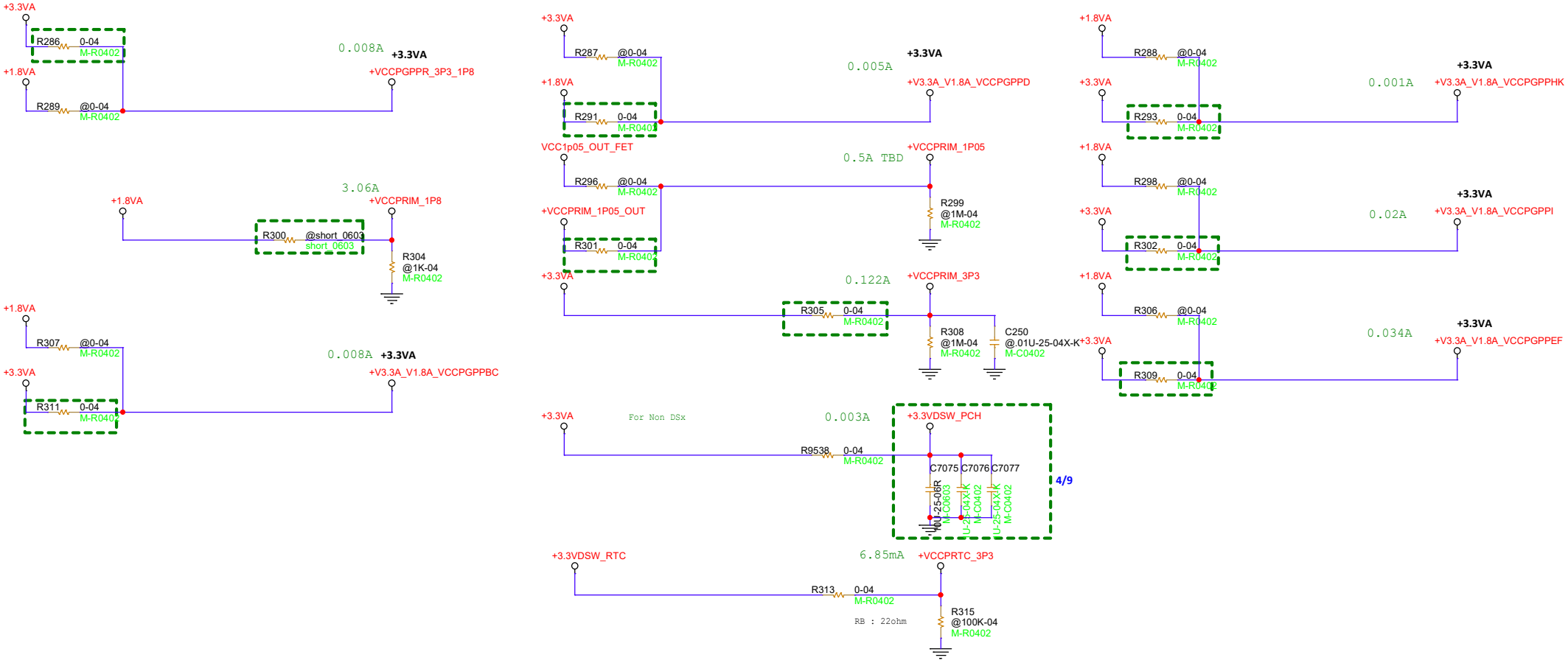
HVM STRAP



同方国际信息技术有限公司

Title	PCH_H STARPS	
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 26 of 78	

PCH DERIVED RAILS



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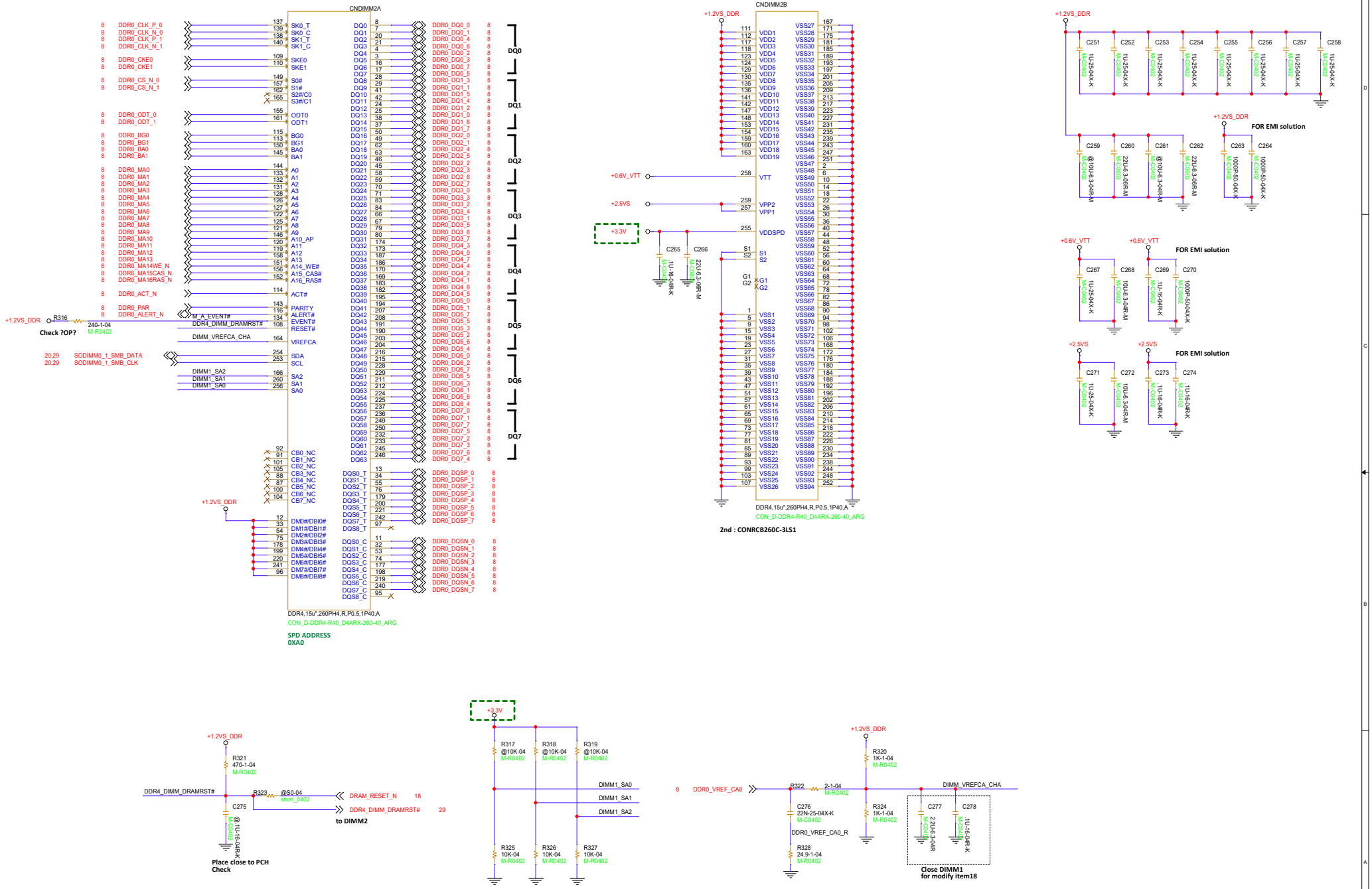
Title	PCH_H DERIVED RAILS	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 27 of 78	



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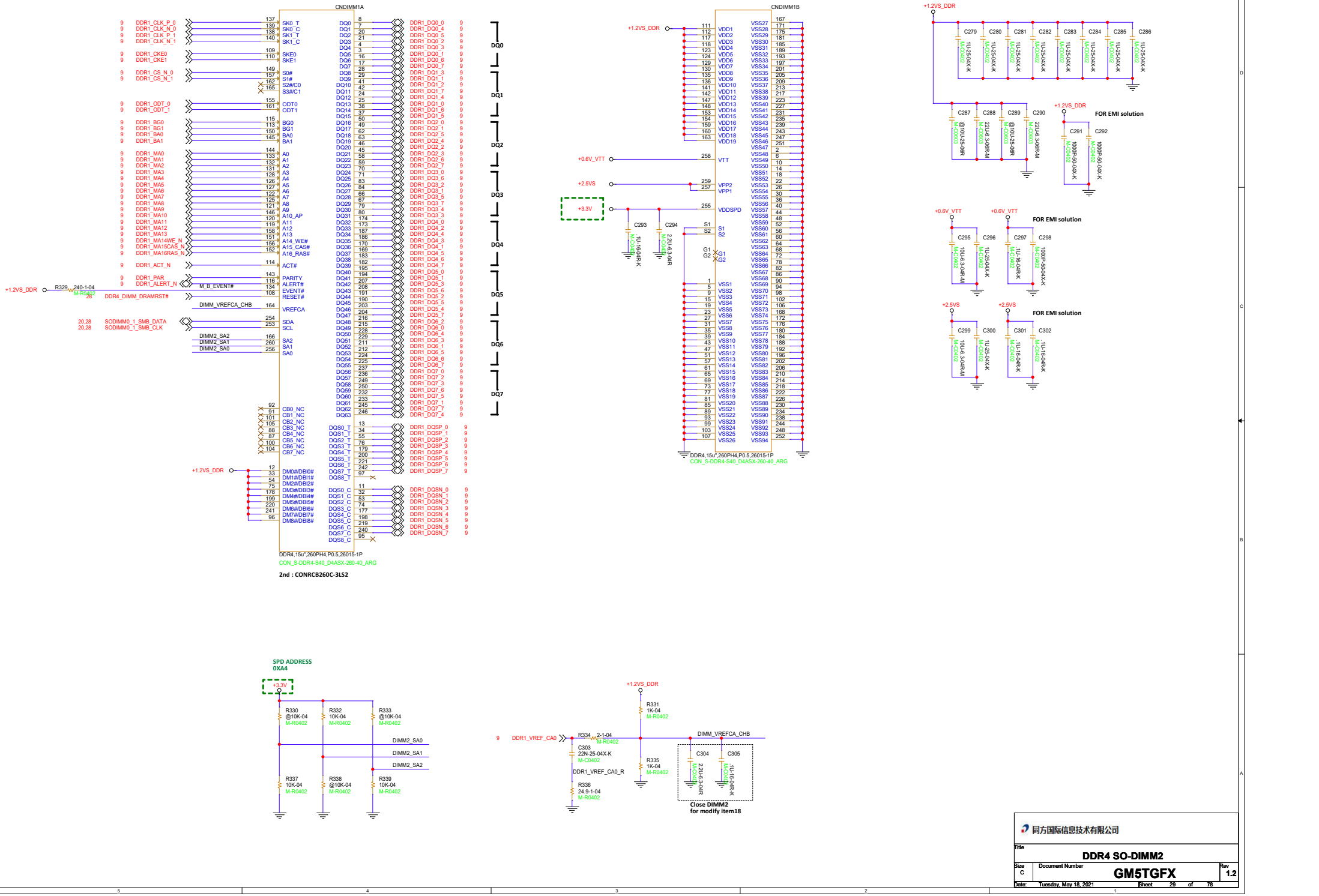
Title	DDR4 SO-DIMM1	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 28 of 78	

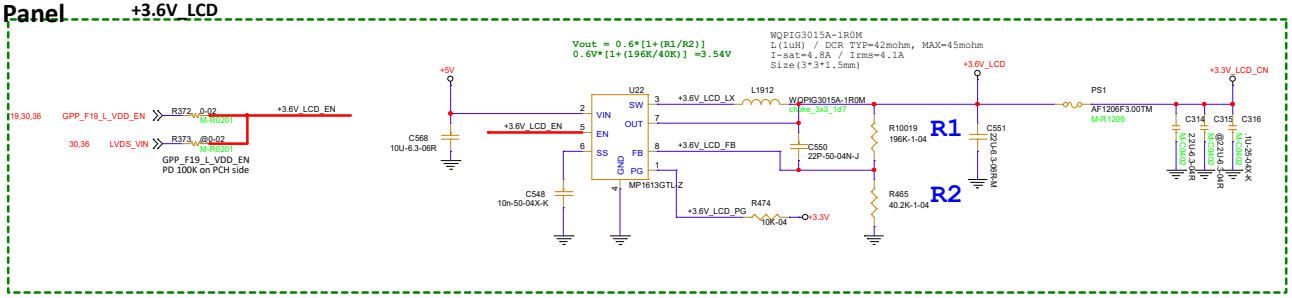


同方国际信息技术有限公司

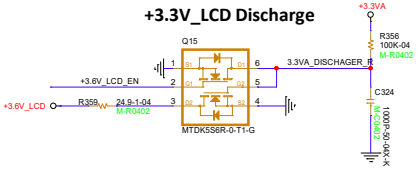
Title	DDR4 SO-DIMM2	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 29 of 78	

Panel

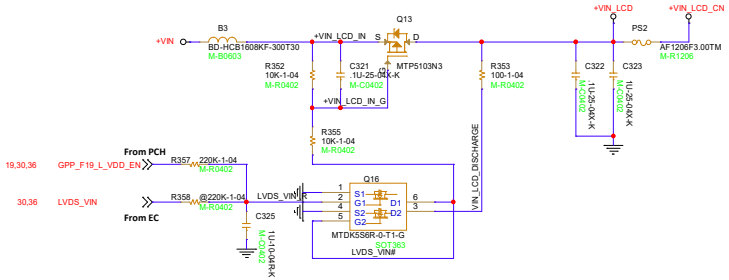
+3.6V_LCD



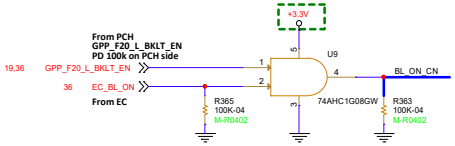
+3.3V_LCD Discharge



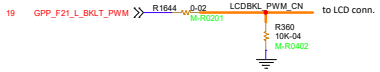
LCD VIN

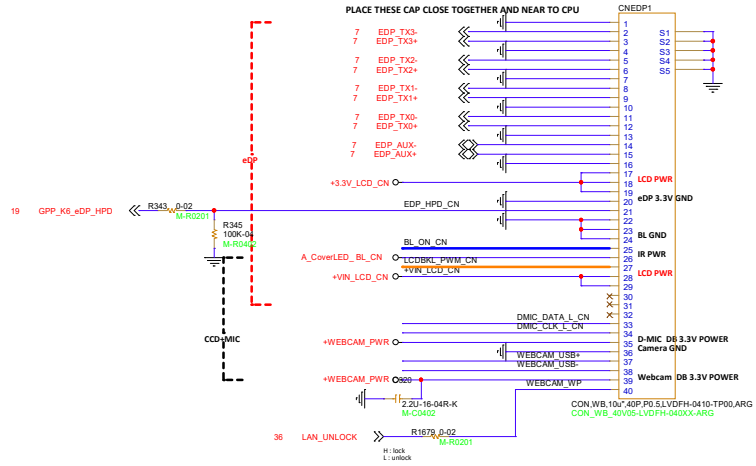


BL_EN



LCD PWM

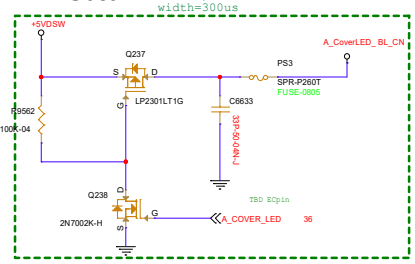


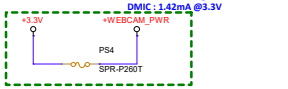


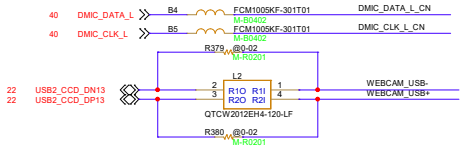
IR + Webcam

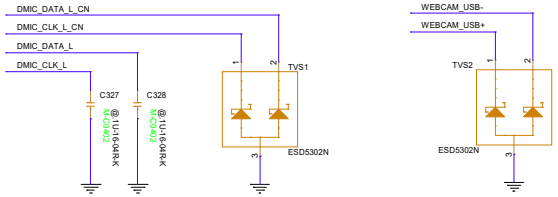
EMFA0P02J MOS SPEC
ID=-3A, 100 miniOHM@Pulse
width=300us

IR : 450mA @ 5V (max : 650mA@5V)
Camera : 250mA @3.3V
DMIC : 1.42mA @3.3V









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Title	eDP Panel/CAMERA	
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 30 of 78	

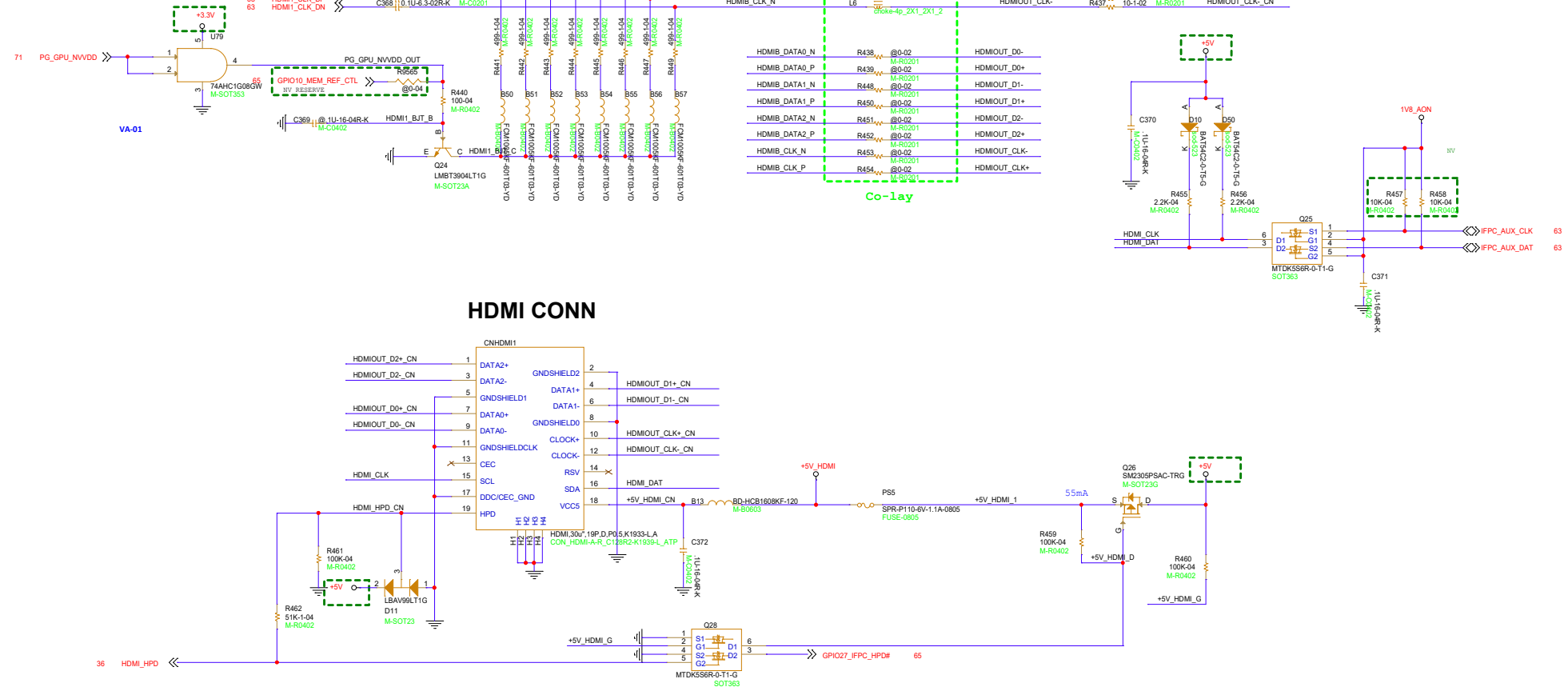
同方国际信息技术有限公司

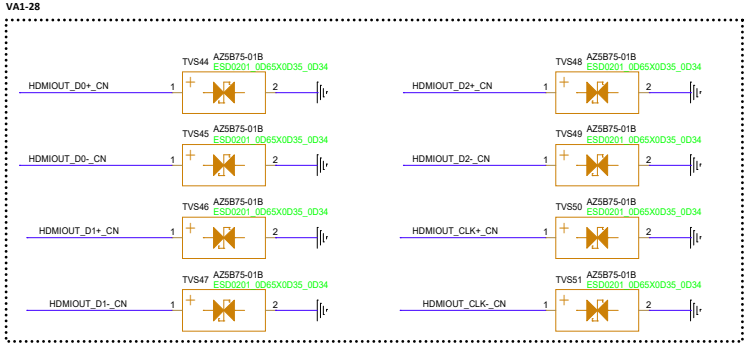
Title	TBD	
Size: C	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 31 of 78	

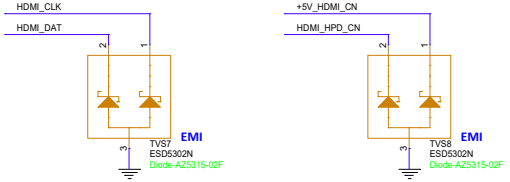
HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported

HDMI CONN







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Title	HDMI	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 32 of 78	

同方国际信息技术有限公司

Title

TBT4 RETIMER 1/3

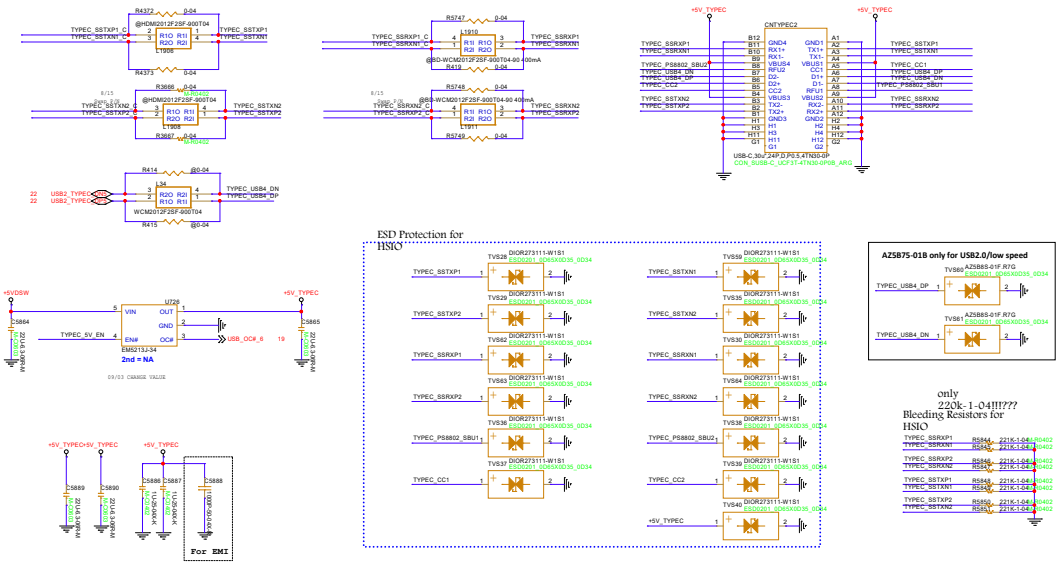
Size	Document Number	Rev
Custom	GM5TGFX	1.2

Date: Tuesday, May 18, 2021 Sheet 33 of 78

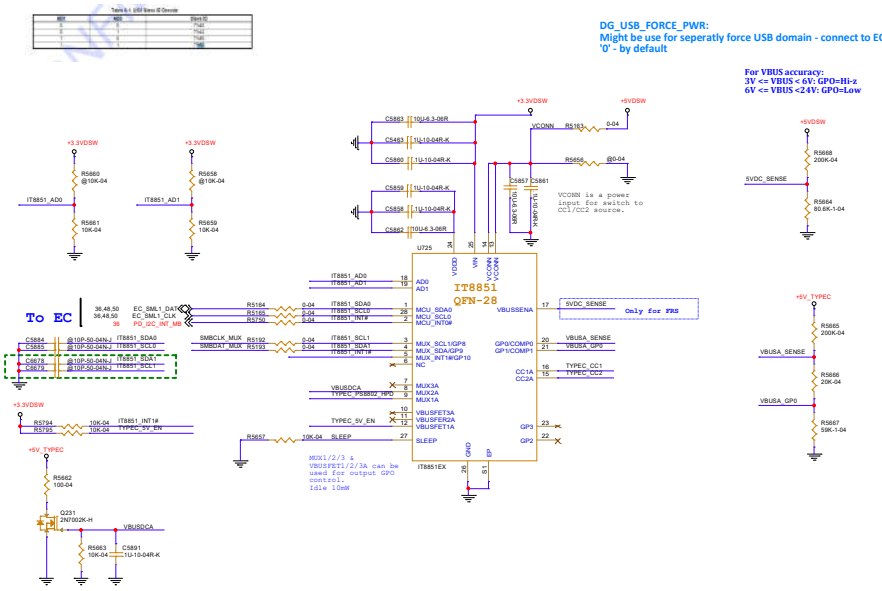
同方国际信息技术有限公司

Title	TBT4 PD 2/3	
Size: C	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 34 of 78	

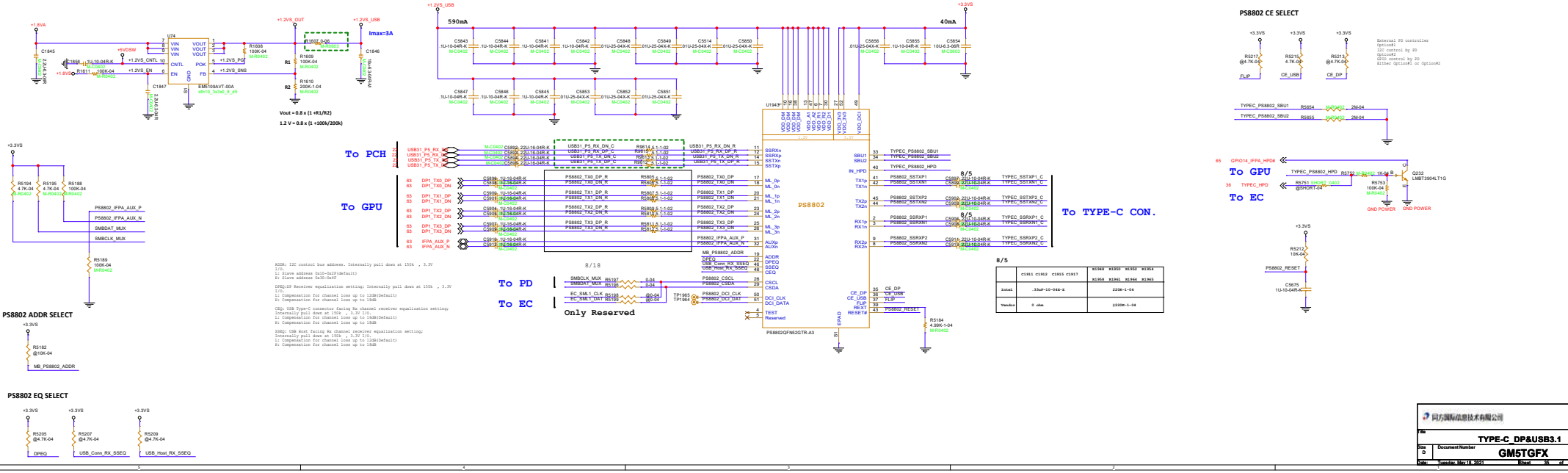
TYPE-C CON.



PD

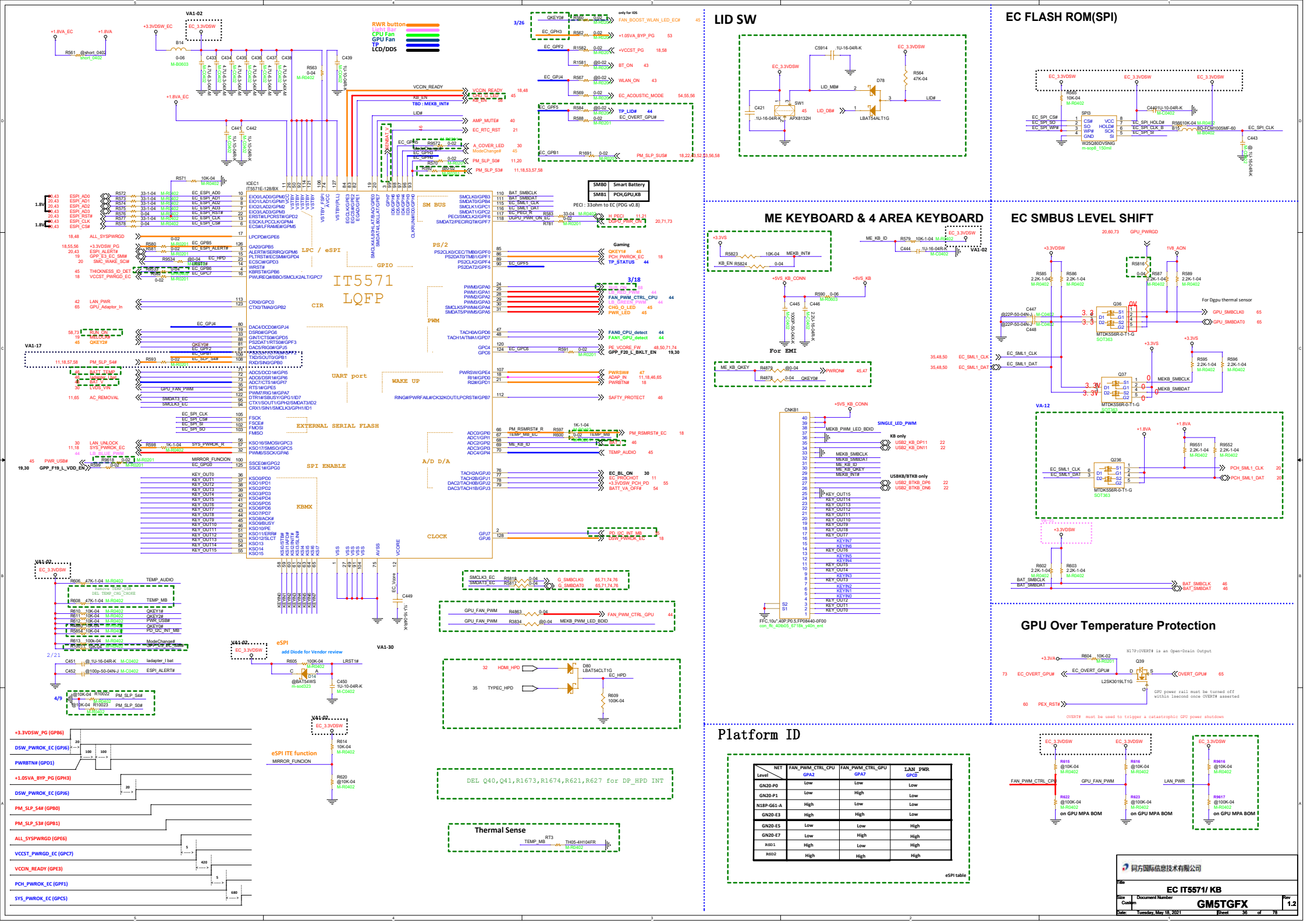


+1.2VS



	C1911 C1912 C1915 C1917	R1908 R1930 R1932 R1934 R1958 R1961 R1964 R1965
Intel	.33uF-10-04X-E	220R-1-04
Vendor	0 ohm	(220R-1-04

同方国际信息技术有限公司			
File	TYPE-C_DP&USB3.1		
Size D	Document Number GM5TGFX		Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 35 of 78		


LID SW
EC FLASH ROM(SPI)
ME KEYBOARD & 4 AREA KEYBOARD
EC SMBUS LEVEL SHIFT
GPU Over Temperature Protection
Platform ID
IT5571
LQFP
LPC / eSPI
GPIO
SM BUS
PS/2
PWM
CIR
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
CLOCK
KBMX
eSPI
eSPI ITE function
Thermal Sense
DEL Q40,Q41,R1673,R1674,R621,R627 for DP_HPD INT
eSPI table
EC IT5571/ KB
GM5TGFX

Remove

TPM2.0

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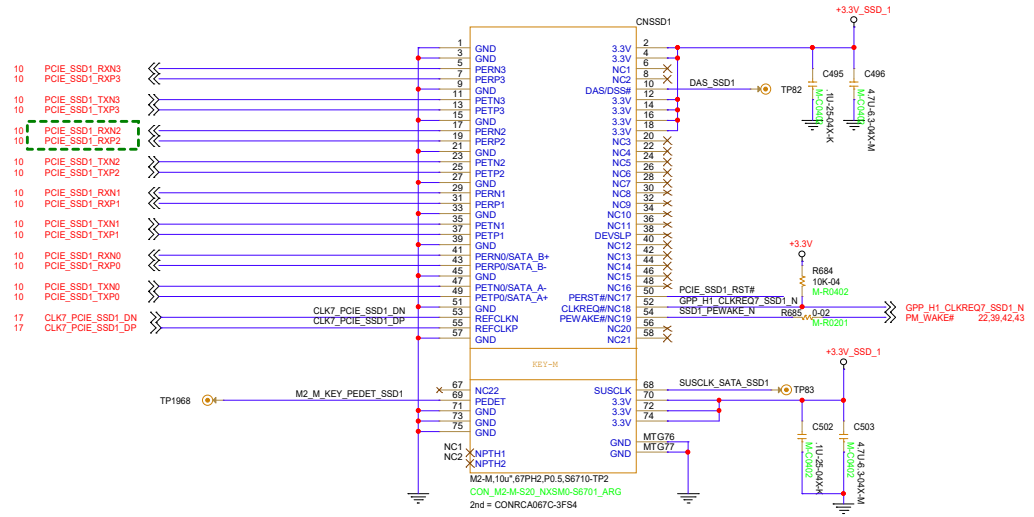
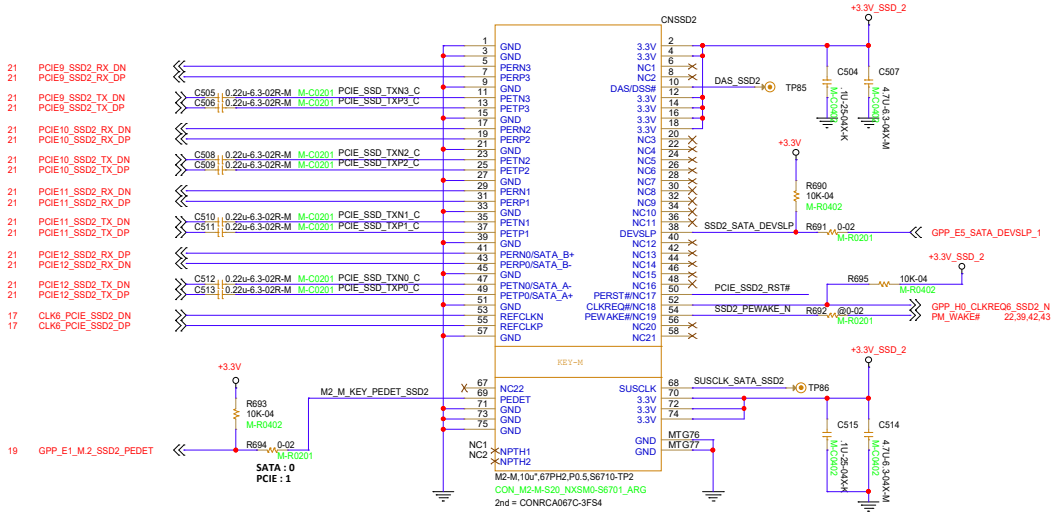
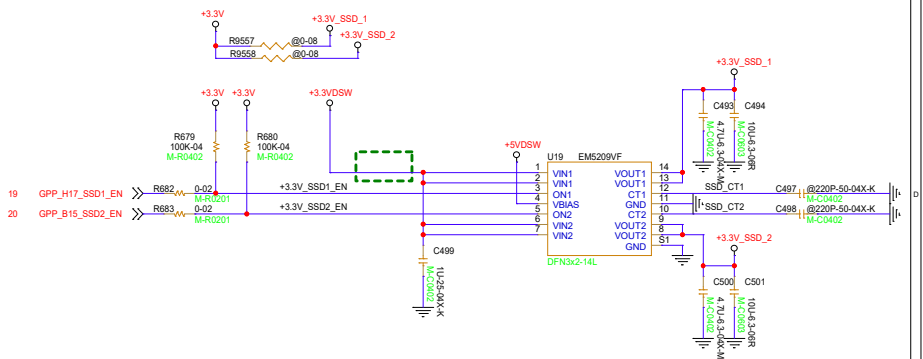
Title: TPM 2.0		
Size: A	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 38 of 78	

PCIEx4 Gen4 SSD

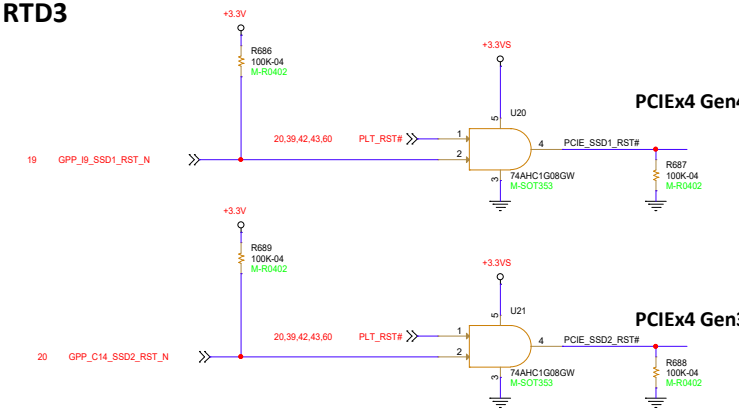


PCIEx4 Gen3/SATA SSD

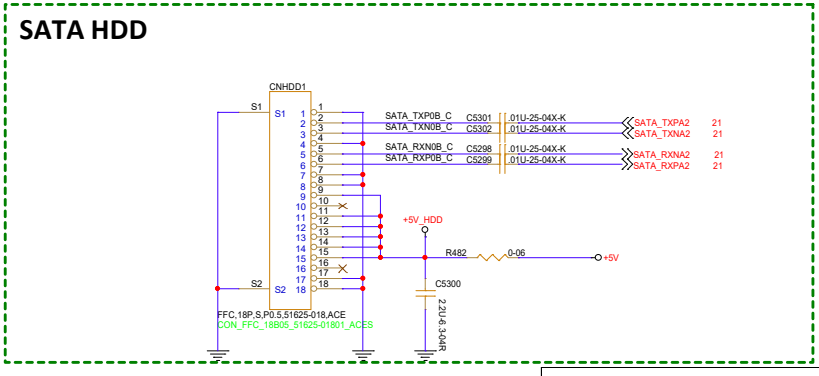




RTD3



SATA HDD



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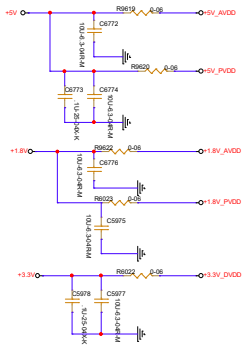
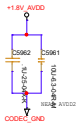
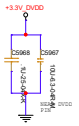
Title	M.2 PCIEx4 Gen4/Gen3+SATA	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 39 of 78	

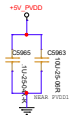
CODEC ALC256

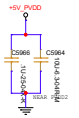
2/2

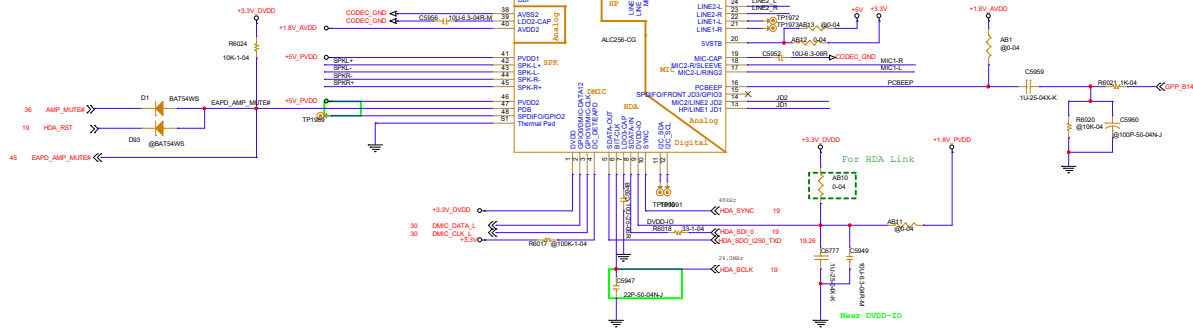




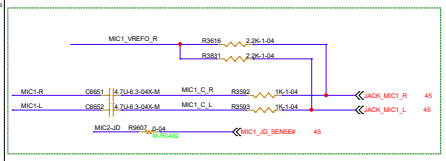




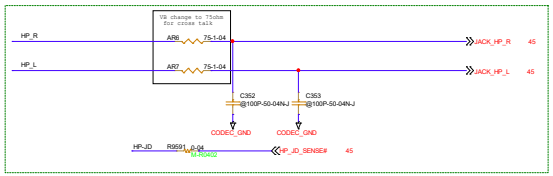




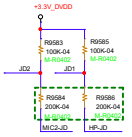
For 3 Stage MIC Jack

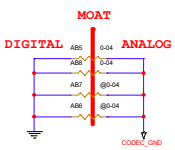


For 3 Stage HP Jack

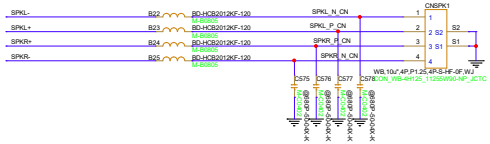


Reserved for Line in1





INT_SPEAKER



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Title: AUDIO ALC256

Size: Custom | Document Number: GM5TGFX | Rev: 1.2

Date: Tuesday, May 18, 2021 | Sheet 40 of 78

AMP-ALC122

DEL ALC122

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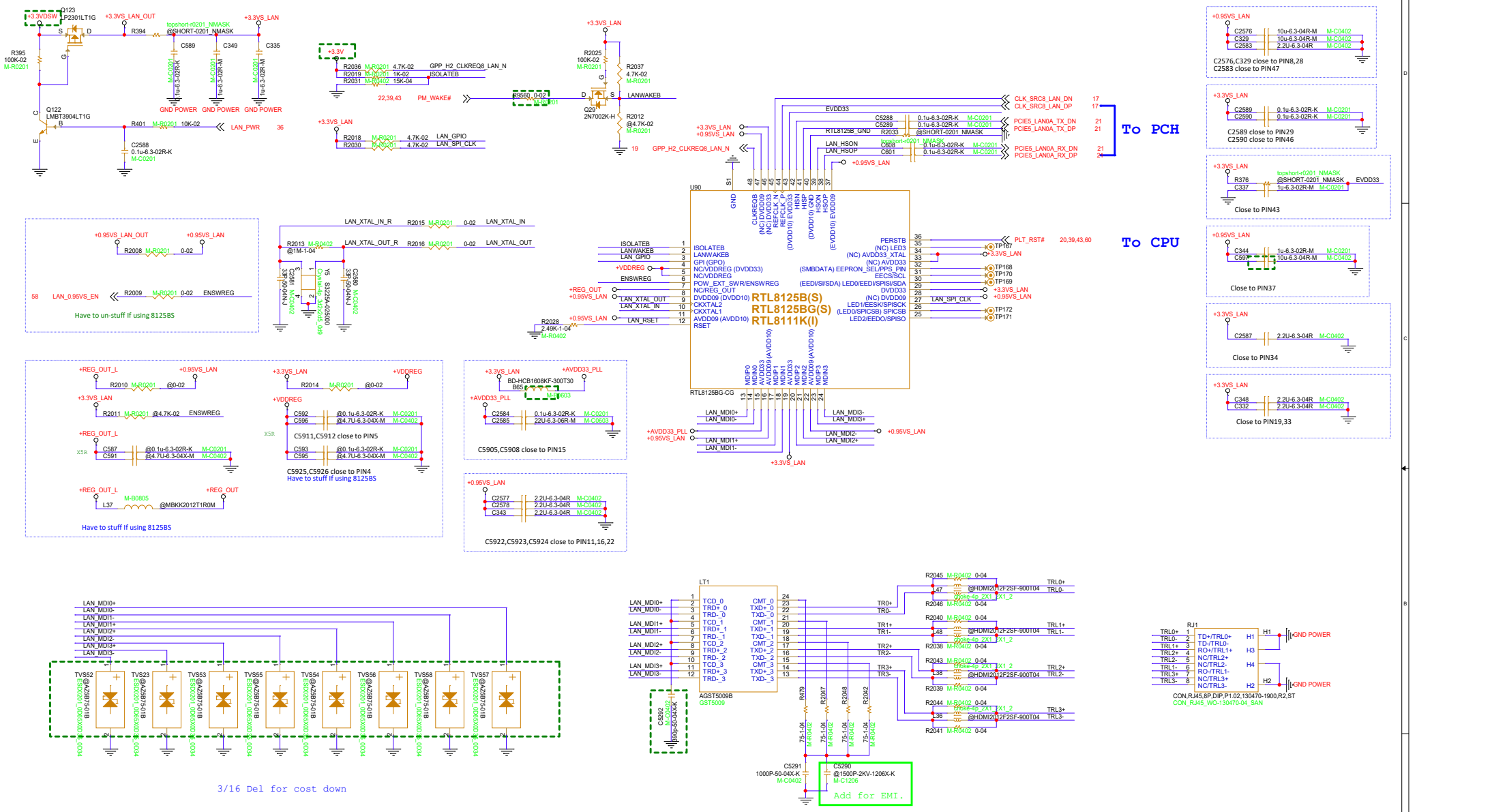
Title	AMPLIFIER ALC122	
Size: C	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 41 of 78	



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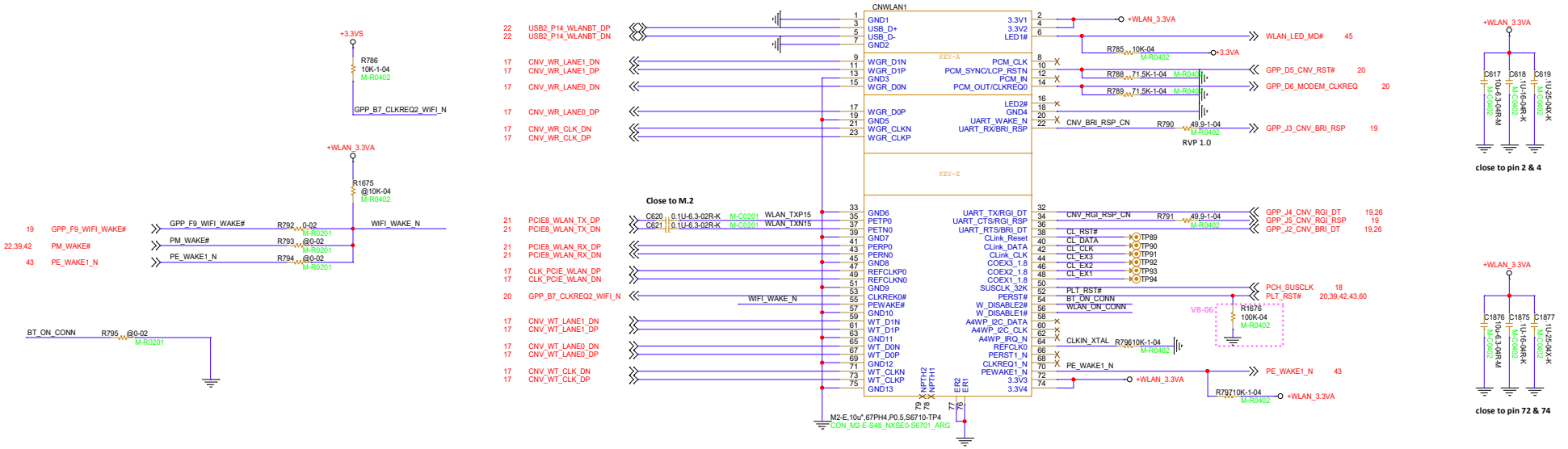
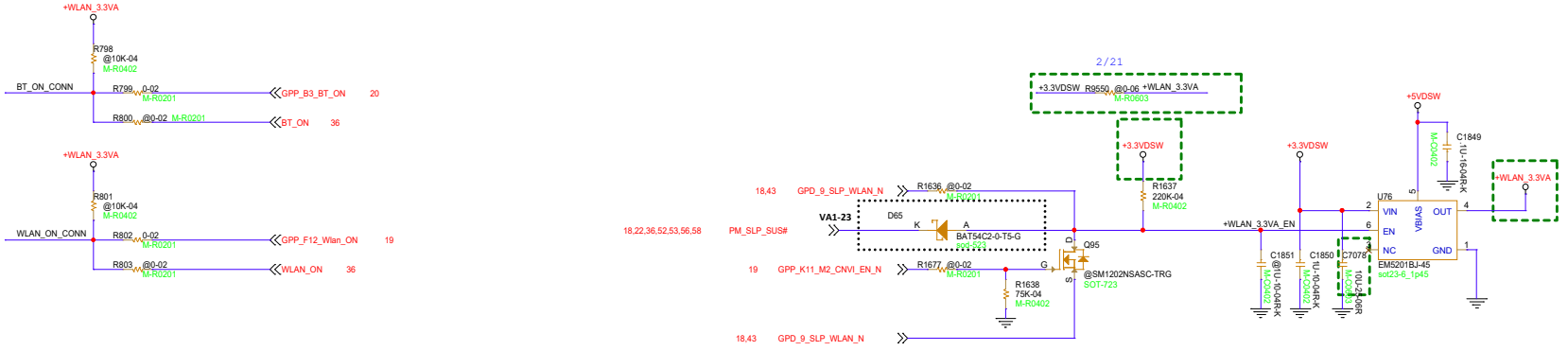
Title	LAN RTL8125B(S)	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 42 of 78	

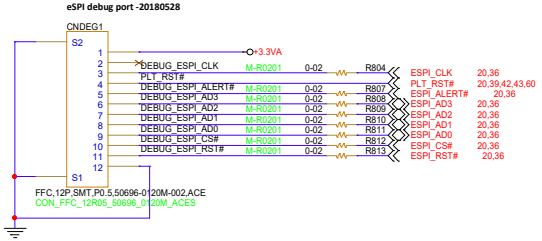
WLAN/BT CONN



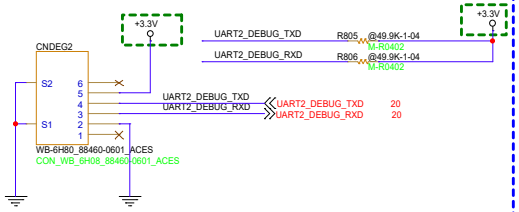
RTD3



eSPI debug port



UART debug port



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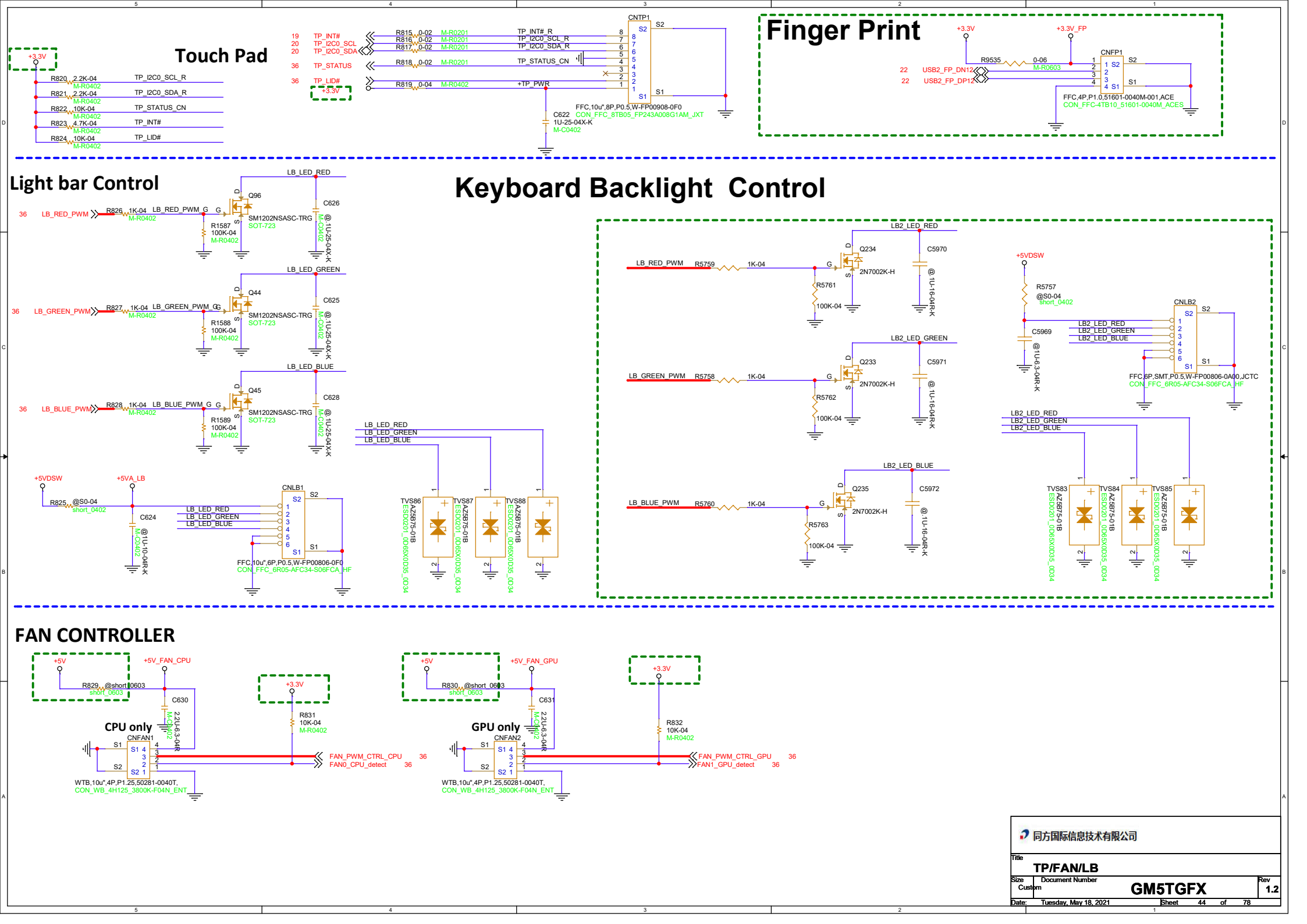
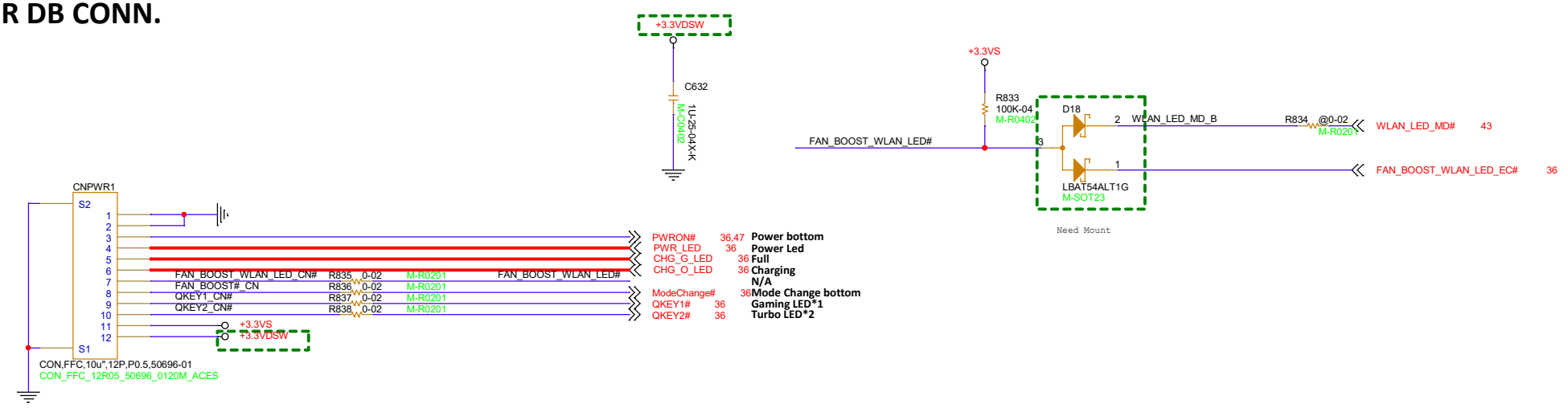
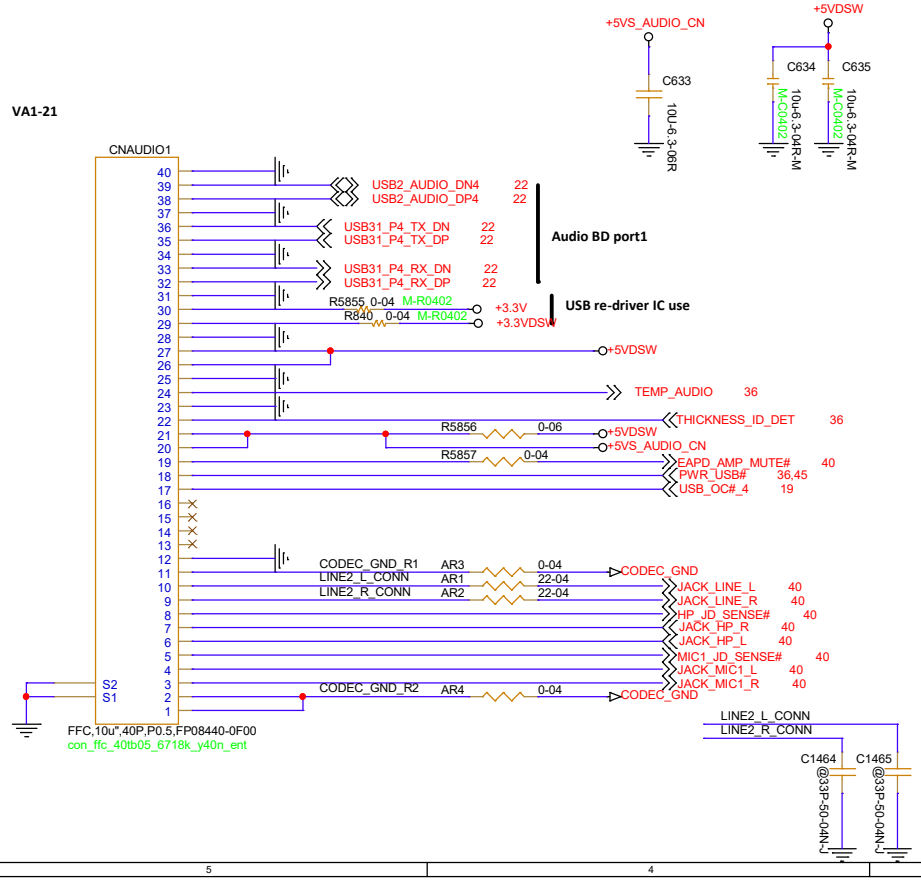
Title	WIFI/BT/DEBUG/DCI	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 43 of 78	


Touch Pad
Finger Print
Light bar Control
Keyboard Backlight Control
FAN CONTROLLER
CPU only
GPU only
同方国际信息技术有限公司
TP/FAN/LB
GM5TGFX
Rev 1.2
Tuesday, May 18, 2021
Sheet 44 of 78

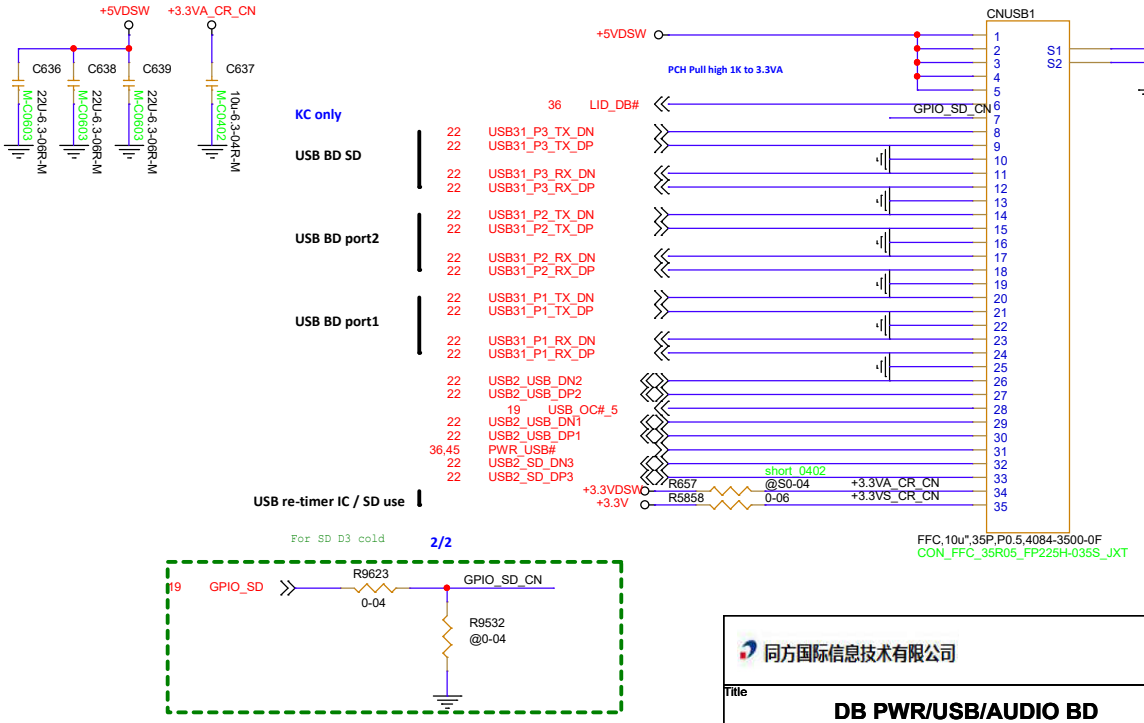
POWER DB CONN.



Audio DB CONN.

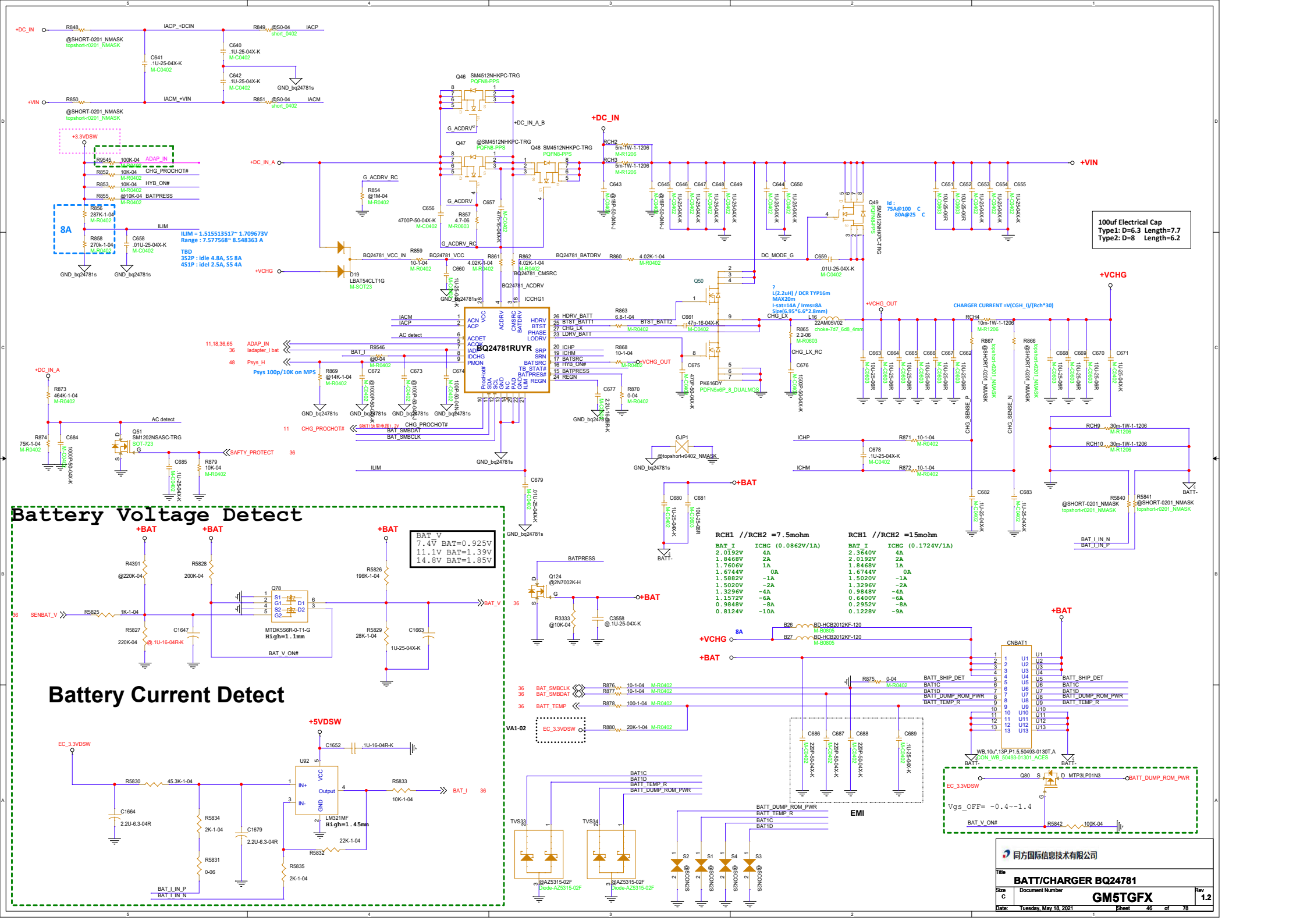


USB DB CONN.



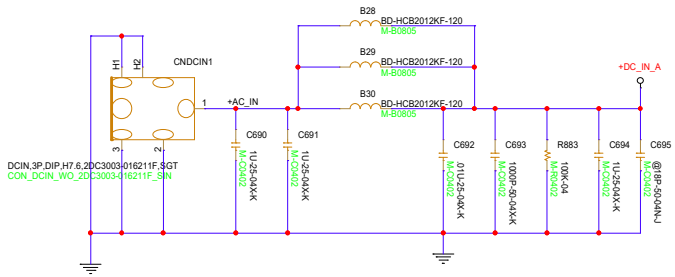
同方国际信息技术有限公司

Title	DB PWR/USB/AUDIO BD	
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 45 of 78	

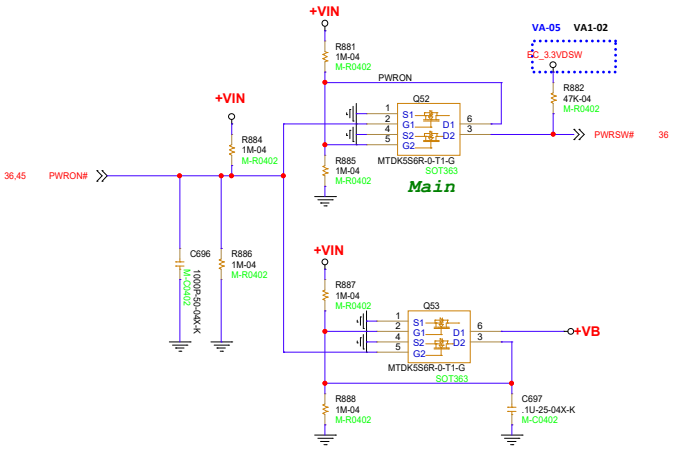

Battery Voltage Detect
Battery Current Detect
BQ24781RUYR
+DC_IN
+VIN
+VCHG
+BAT
+5VDSW
+3.3VDSW
8A
ILIM = 1.515513517~ 1.709673V
Range : 7.577568~ 8.548363 A
TBD
3S2P : idle 4.8A, S5 8A
4S1P : idel 2.5A, S5 4A
100uf Electrical Cap
Type1: D=6.3 Length=7.7
Type2: D=8 Length=6.2
CHARGER CURRENT =V(CGH_I)/(Rch*30)
RCH1 //RCH2 =7.5mohm
BAT_I ICHG (0.0862V/1A)
2.0192V 4A
1.8468V 2A
1.7606V 1A
1.6744V 0A
1.5882V -1A
1.5020V -2A
1.3296V -4A
1.1572V -6A
0.9848V -8A
0.8124V -10A
RCH1 //RCH2 =15mohm
BAT_I ICHG (0.1724V/1A)
2.3640V 4A
2.0192V 2A
1.8468V 1A
1.6744V 0A
1.5020V -1A
1.3296V -2A
0.9848V -4A
0.6400V -6A
0.2952V -8A
0.1228V -9A
BAT_V
7.4V BAT=0.925V
11.1V BAT=1.39V
14.8V BAT=1.85V
Psys 100p/10K on MPS
EMI
同方国际信息技术有限公司
BATT/CHARGER BQ24781
GM5TGFX
1.2
Tuesday, May 18, 2021
Sheet 46 of 78

+DC_IN

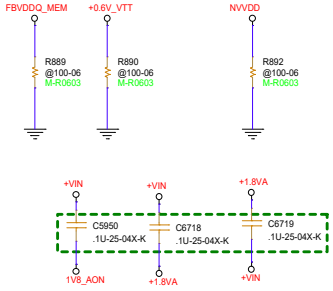
EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms



Power Bottom



Discharge Resistor

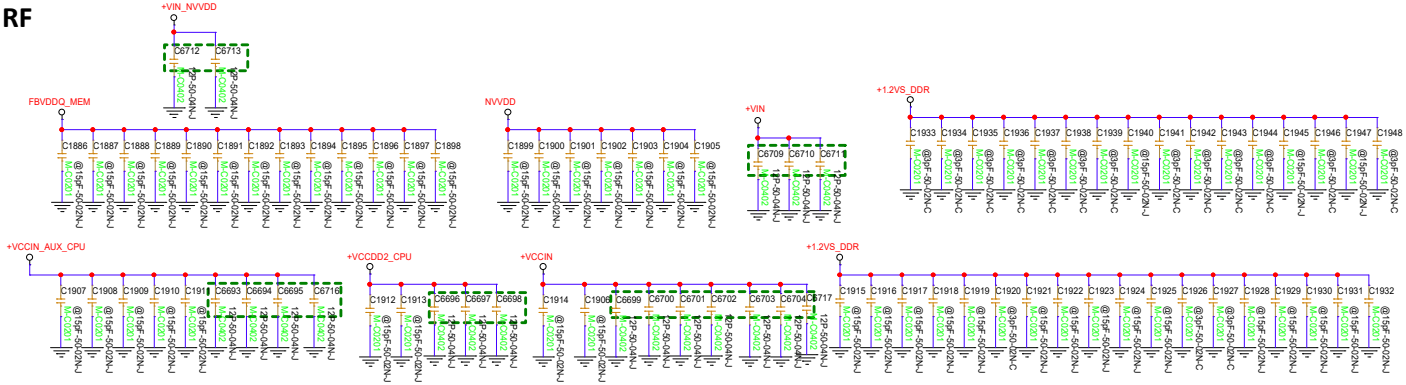


For SMT

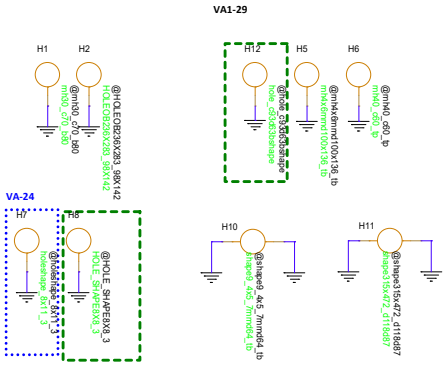
Place to TOP Side

TP98	TP32	+5VDSW
TP99	TP32	+3.3VDSW
TP100	TP32	+1.8VA
TP101	TP32	+VNN_BYP
TP102	TP32	+0.6V_VTT
TP103	TP32	+1.2VS_DDR
TP104	TP32	+2.5VS
TP134	TP32	+1.05VA_BYP

For RF



PCB HOLE



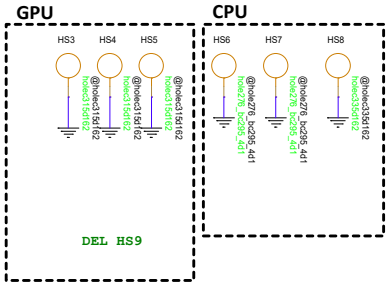
WLAN HOLE

DEL

THERMAL HOLE

GPU

CPU

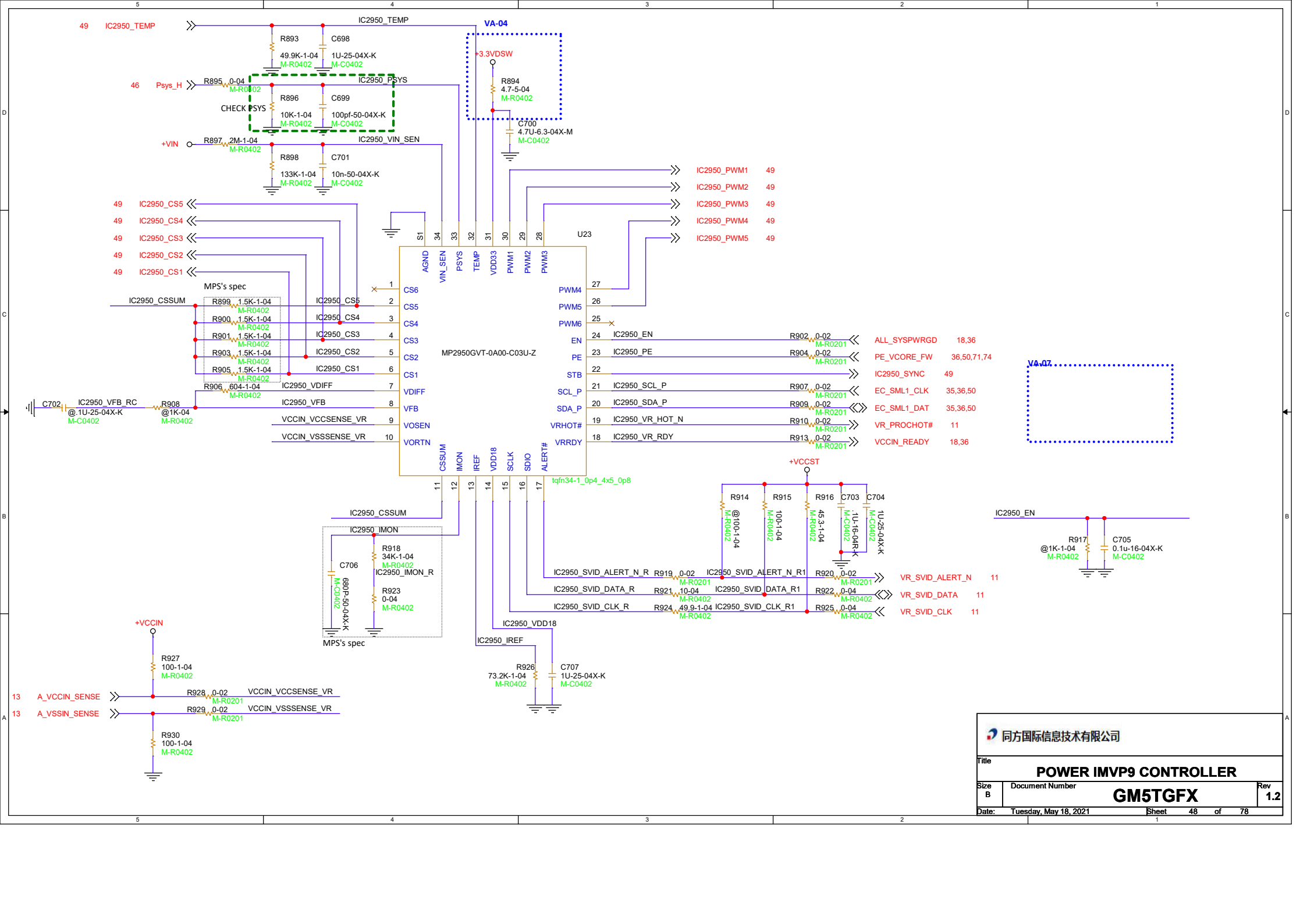


DEL PCH Bracket

Mark point

同方国际信息技术有限公司

Title	DC IN/PWR_SW/H-S CAP/SCREW	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 47 of 78	


49 IC2950_TEMP
IC2950_TEMP
R893 49.9K-1-04 M-R0402
C698 1U-25-04X-K M-C0402
VA-04
+3.3VDSW
R894 4.7-5-04 M-R0402
C700 4.7U-6.3-04X-M M-C0402
46 Psys_H
R895 0-04 M-R0402
IC2950_PSYS
CHECK PSYS
R896 10K-1-04 M-R0402
C699 100pf-50-04X-K M-C0402
+VIN
R897 2M-1-04 M-R0402
IC2950_VIN_SEN
R898 133K-1-04 M-R0402
C701 10n-50-04X-K M-C0402
IC2950_PWM1 49
IC2950_PWM2 49
IC2950_PWM3 49
IC2950_PWM4 49
IC2950_PWM5 49
49 IC2950_CS5
49 IC2950_CS4
49 IC2950_CS3
49 IC2950_CS2
49 IC2950_CS1
MPS's spec
IC2950_CSSUM
R899 1.5K-1-04 M-R0402
R900 1.5K-1-04 M-R0402
R901 1.5K-1-04 M-R0402
R903 1.5K-1-04 M-R0402
R905 1.5K-1-04 M-R0402
IC2950_CS5
IC2950_CS4
IC2950_CS3
IC2950_CS2
IC2950_CS1
R906 604-1-04 M-R0402
IC2950_VDIFF
C702 IC2950_VFB_RC @.1U-25-04X-K M-C0402
R908 @1K-04 M-R0402
IC2950_VFB
VCCIN_VCCSENSE_VR
VCCIN_VSSSENSE_VR
S1
AGND
VIN_SEN
PSYS
TEMP
VDD33
PWM1
PWM2
PWM3
U23
CS6
CS5
CS4
CS3
CS2
CS1
VDIFF
VFB
VOSEN
VORTN
MP2950GVT-0A00-C03U-Z
PWM4
PWM5
PWM6
EN
PE
STB
SCL_P
SDA_P
VRHOT#
VRRDY
tqfn34-1_0p4_4x5_0p8
IC2950_EN
IC2950_PE
IC2950_SCL_P
IC2950_SDA_P
IC2950_VR_HOT_N
IC2950_VR_RDY
R902 0-02 M-R0201
R904 0-02 M-R0201
R907 0-02 M-R0201
R909 0-02 M-R0201
R910 0-02 M-R0201
R913 0-02 M-R0201
ALL_SYSPWRGD 18,36
PE_VCORE_FW 36,50,71,74
IC2950_SYNC 49
EC_SML1_CLK 35,36,50
EC_SML1_DAT 35,36,50
VR_PROCHOT# 11
VCCIN_READY 18,36
VA-07
CSSUM
IMON
IREF
VDD18
SCLK
SDIO
ALERT#
+VCCST
R914 @100-1-04 M-R0402
R915 100-1-04 M-R0402
R916 45.3-1-04 M-R0402
C703 1U-16-04R-K M-C0402
C704 1U-25-04X-K M-C0402
IC2950_CSSUM
IC2950_IMON
R918 34K-1-04 M-R0402
IC2950_IMON_R
C706 680P-50-04X-K M-C0402
R923 0-04 M-R0402
MPS's spec
IC2950_SVID_ALERT_N_R
IC2950_SVID_DATA_R
IC2950_SVID_CLK_R
R919 0-02 M-R0201
R921 10-04 M-R0402
R924 49.9-1-04 M-R0402
IC2950_SVID_ALERT_N_R1
IC2950_SVID_DATA_R1
IC2950_SVID_CLK_R1
R920 0-02 M-R0201
R922 0-04 M-R0402
R925 0-04 M-R0402
VR_SVID_ALERT_N 11
VR_SVID_DATA 11
VR_SVID_CLK 11
IC2950_EN
R917 @1K-1-04 M-R0402
C705 0.1u-16-04X-K M-C0402
IC2950_VDD18
IC2950_IREF
R926 73.2K-1-04 M-R0402
C707 1U-25-04X-K M-C0402
+VCCIN
R927 100-1-04 M-R0402
13 A_VCCIN_SENSE
13 A_VSSIN_SENSE
R928 0-02 M-R0201
R929 0-02 M-R0201
VCCIN_VCCSENSE_VR
VCCIN_VSSSENSE_VR
R930 100-1-04 M-R0402
同方国际信息技术有限公司
Title
POWER IMVP9 CONTROLLER
Size B
Document Number
GM5TGFX
Rev 1.2
Date: Tuesday, May 18, 2021
Sheet 48 of 78

VCCIN

TGL-H
TDC= A max;
ICC max= A

VCCIN : 0~2.05V(Max)
IccMax : 105A
DC_LL : 1.7m ohm

VCCIN_AUX_CPU : 1.8V(Typ)
IccMax : 26.5A
DC_LL : 1.5m ohm

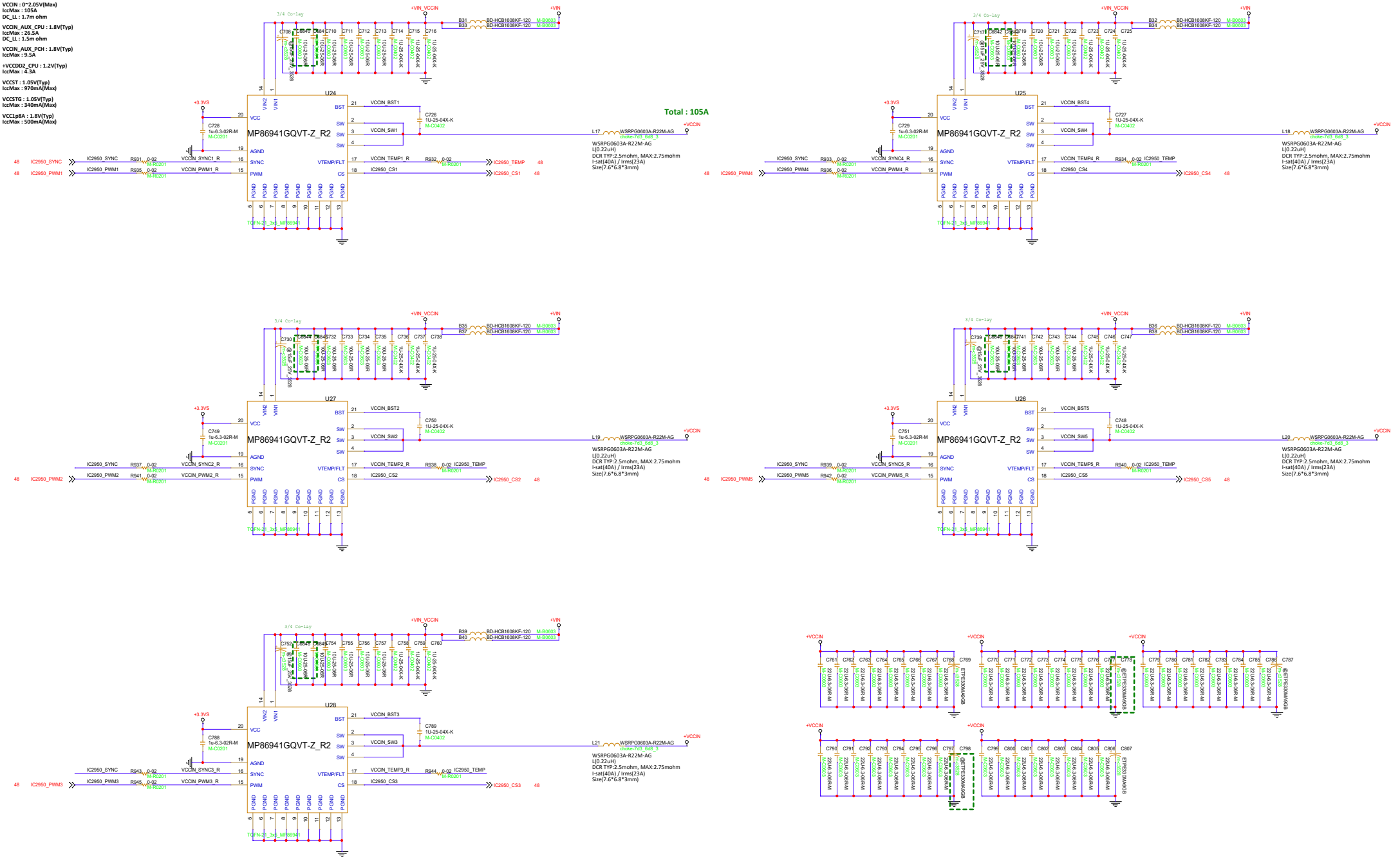
VCCIN_AUX_PCH : 1.8V(Typ)
IccMax : 9.5A

+VCCD02_CPU : 1.2V(Typ)
IccMax : 4.3A

VCCST : 1.05V(Typ)
IccMax : 970mA(Max)

VCCSTG : 1.05V(Typ)
IccMax : 340mA(Max)

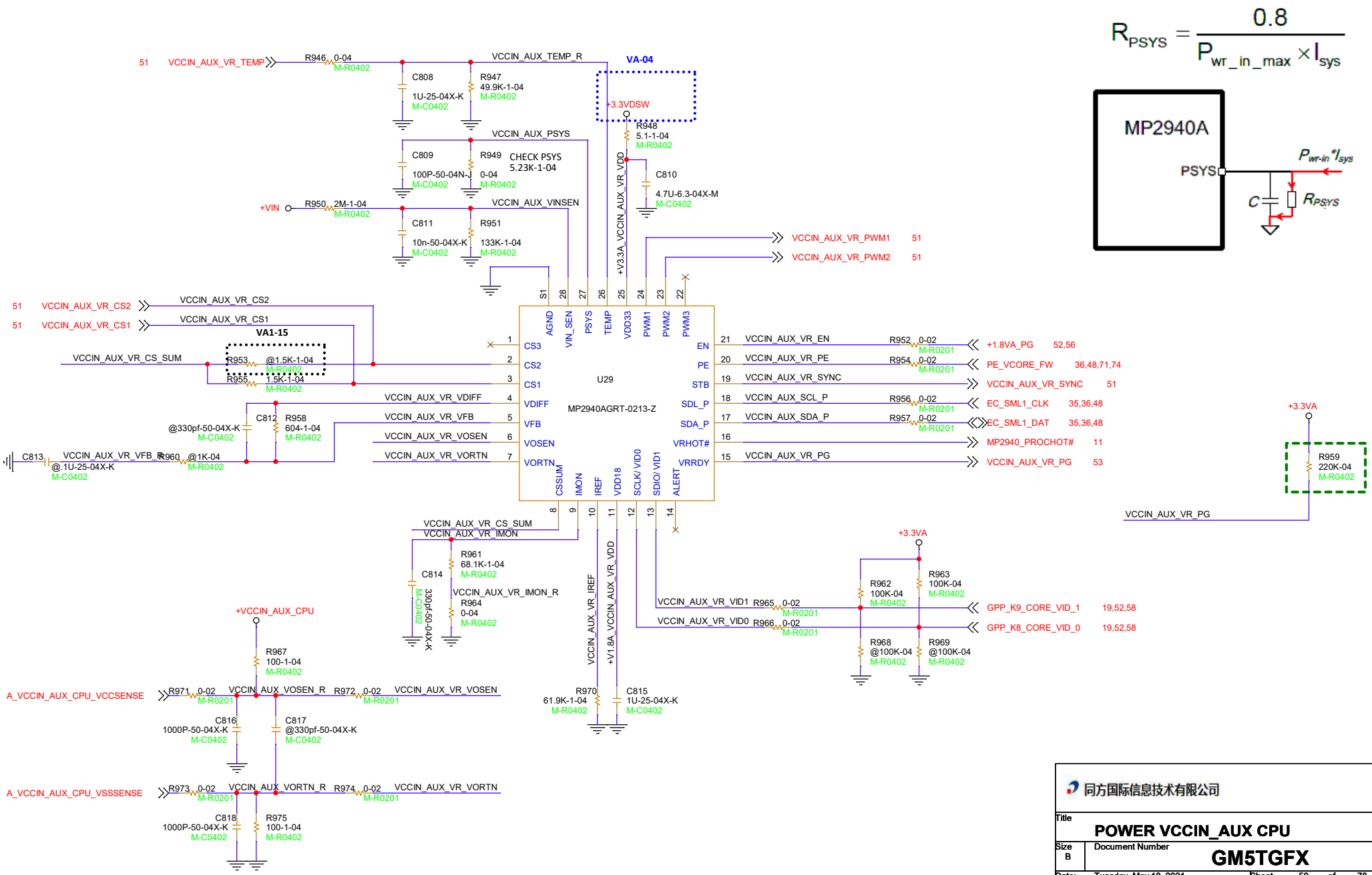
VCC1p8A : 1.8V(Typ)
IccMax : 500mA(Max)



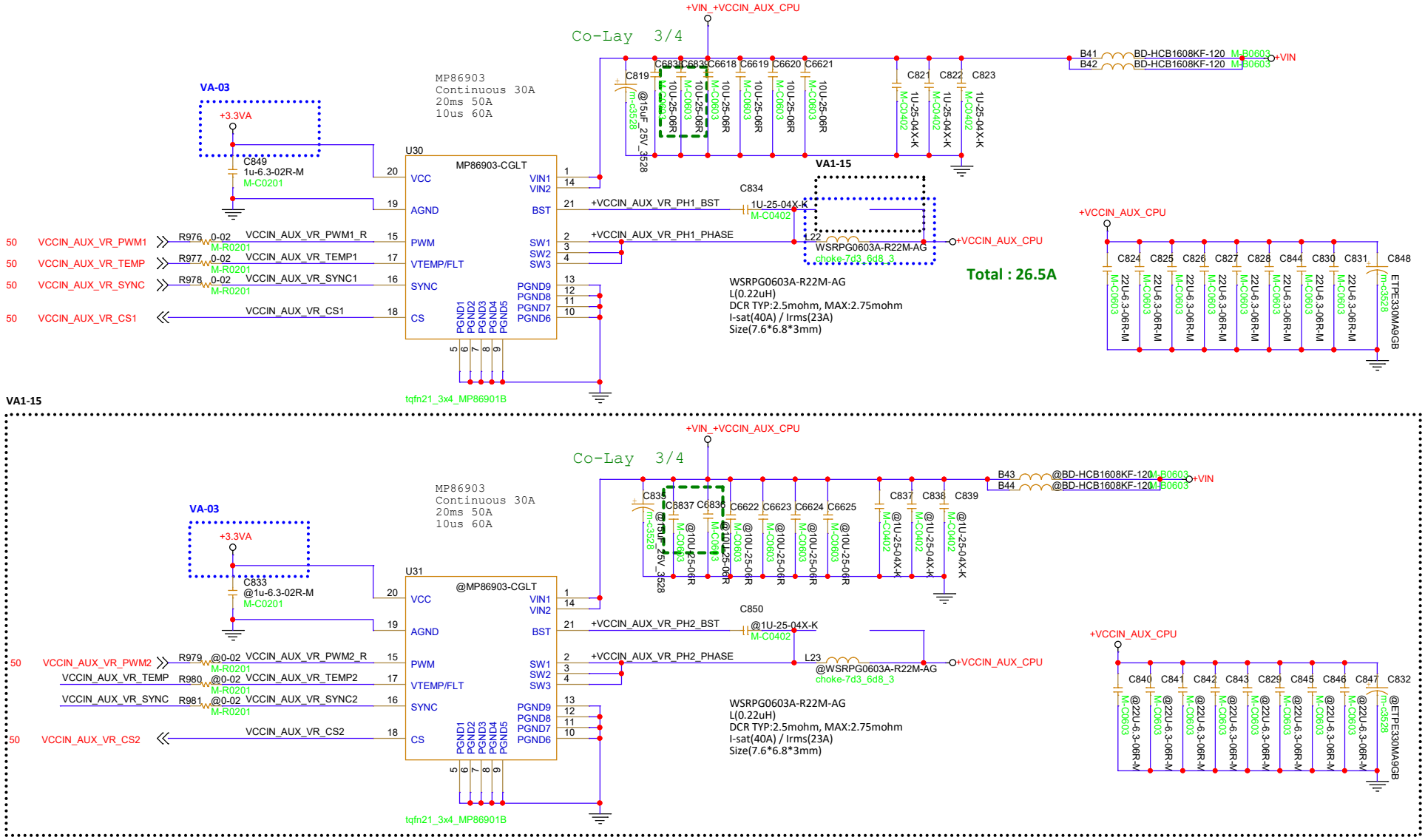
同方国际信息技术有限公司

Title: POWER IMVP9 DR_MOS
Size: Custom | Document Number: GM5TGFX | Rev: 1.2
Date: Tuesday, May 18, 2021 | Sheet 49 of 78

VCCIN_AUX CPU



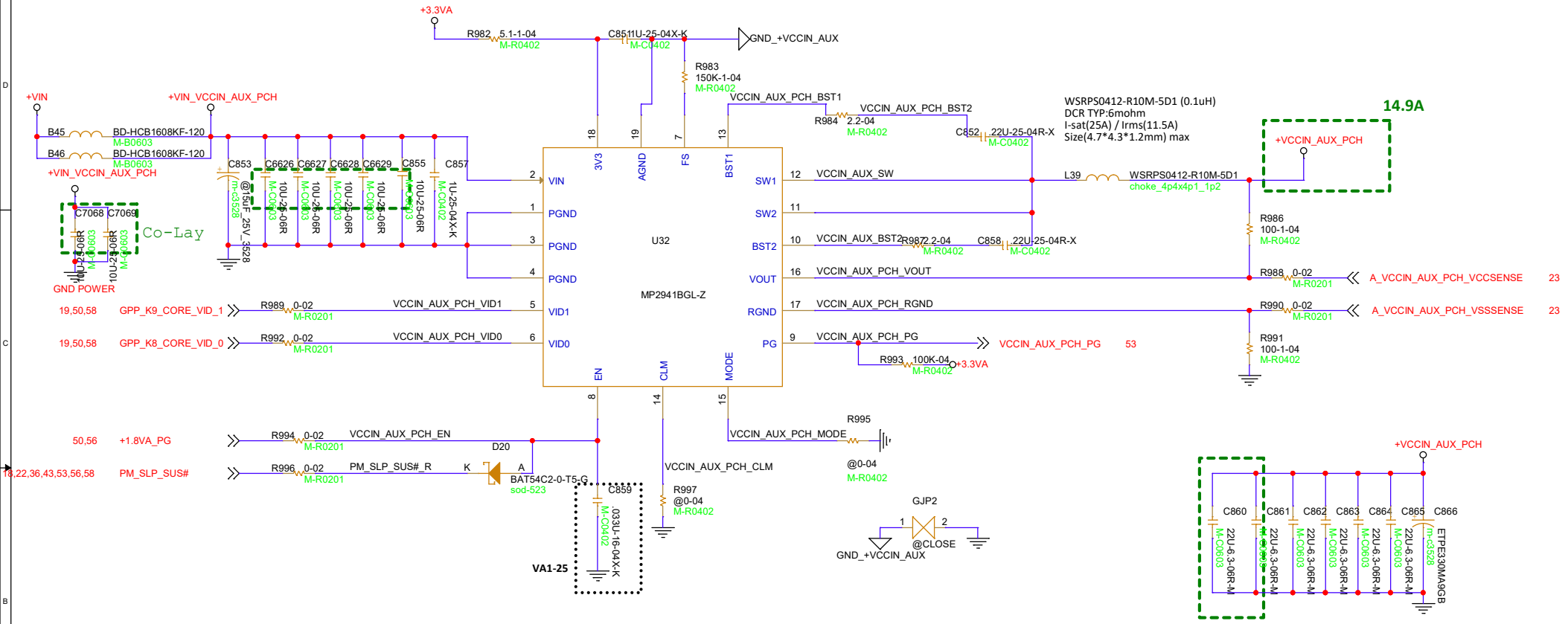
同方国际信息技术有限公司	
Title	POWER VCCIN_AUX CPU
Size B	Document Number GM5TGFX Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 50 of 78



同方国际信息技术有限公司

Title	POWER VCCIN_AUX DR_MOS	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 51 of 78	

VCCIN_AUX_PCH

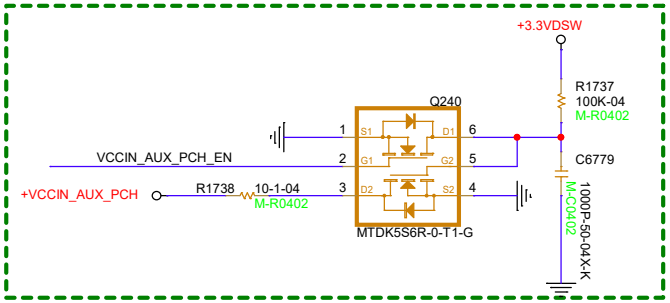


VCCIN_AUX VID

VID[1] Pin State	VID[0] Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.65	Full Current, TGL-UP4
1	1	1.8	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

+VCCIN_AUX_PCH discharge

2/4



同方国际信息技术有限公司

Title	POWER VCCIN_AUX PCH	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 52 of 78	

VNN_BYP/+1.05_BYP

Table 3: Control Bit Logic

	LP #	C1	C0	VOUT (V)
V1P05_BYP	0	X	X	0
	1	0	0	1.05
	1	0	1	1.05
	1	1	0	0.96
	1	1	1	0.96
VNN_BYP	0	X	X	0.7
	1	0	0	1.05
	1	0	1	1.05
	1	1	0	0.78
	1	1	1	0.7

Table 180. VCC_VNNEXT_1P05 VR Voltage Configurations

SLP_S3# State	VNN_CTRL State (Optional)	Output Voltage (V)
0	N/A	1.05
1	0	0.78
1	1	0.70

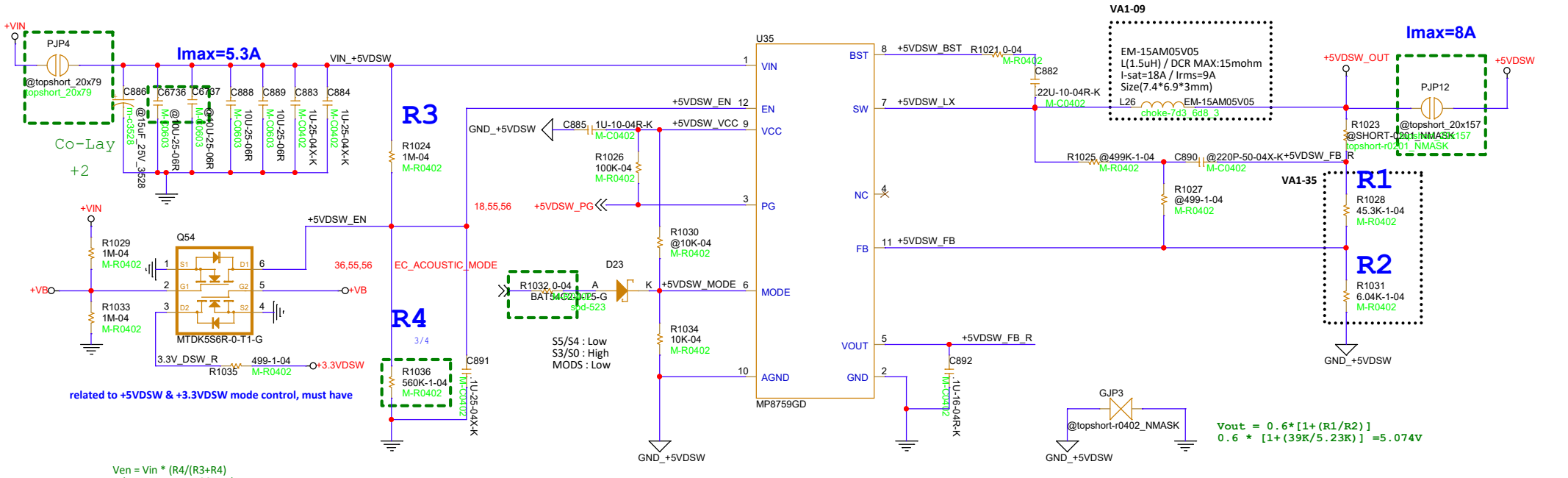
Table 181. VCC_V1P056EXT_1P05 VR Voltage Configurations

V1P05_CTRL State	Output Voltage (V)
0	1.05
1	0.96

同方国际信息技术有限公司

Title	POWER VNN_BYP/+1.05_BYP	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 53 of 78	

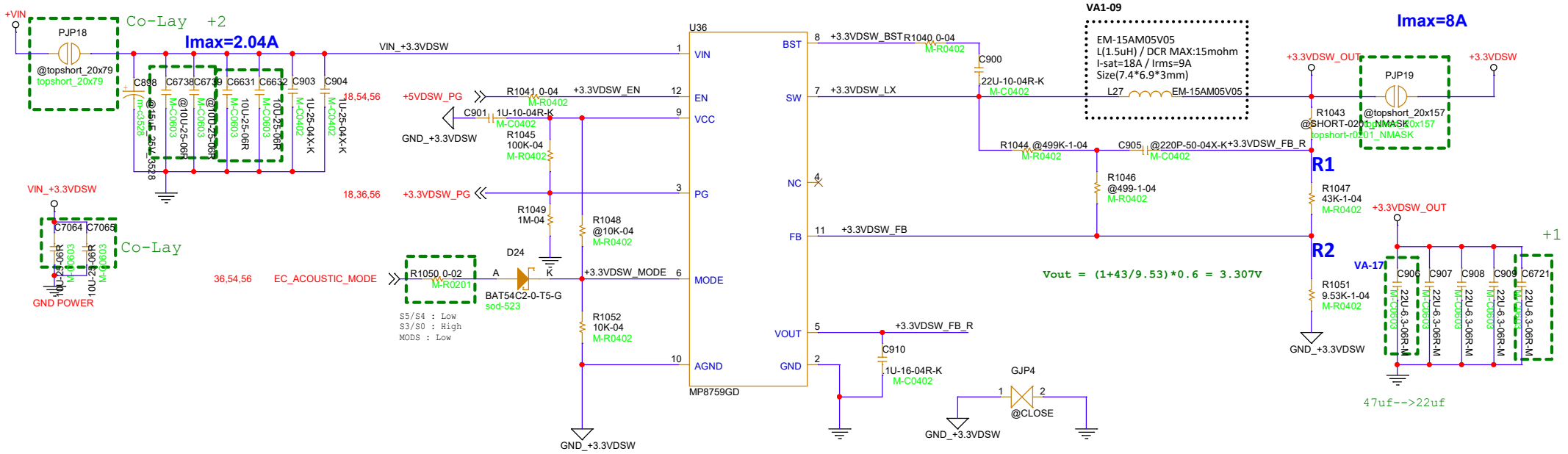
5VDSW Converter



同方国际信息技术有限公司

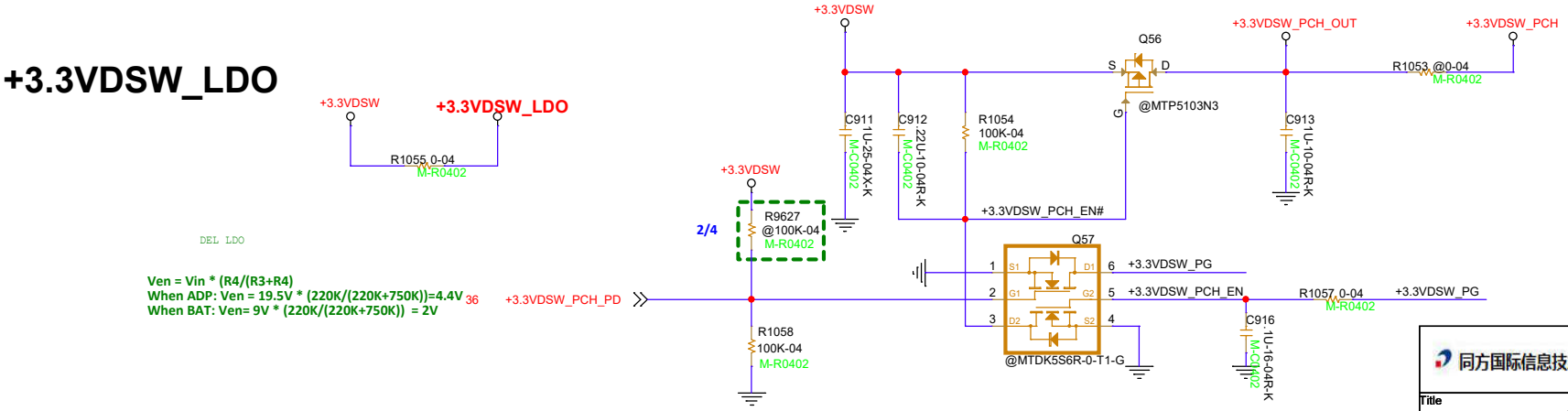
Title	POWER +5VDSW	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 54 of 78	

3.3VDSW Converter



3.3VA_DSW Discharge

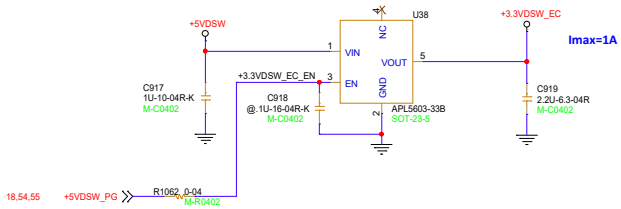
+3.3VDSW_LDO



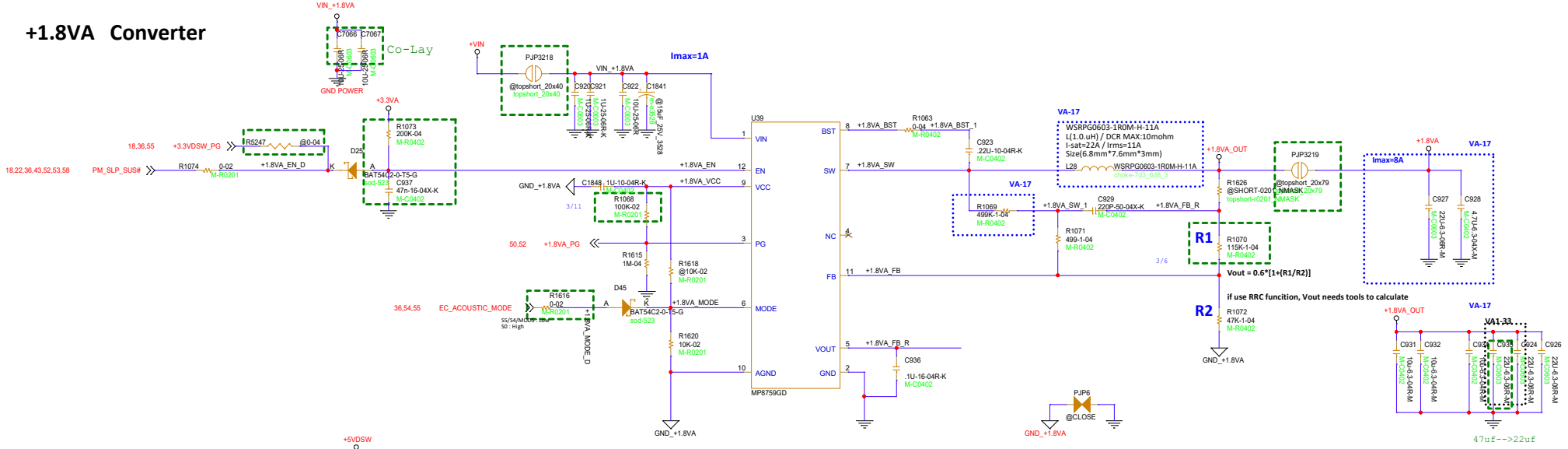
同方国际信息技术有限公司

Title	POWER +3.3VDSW	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 55 of 78	

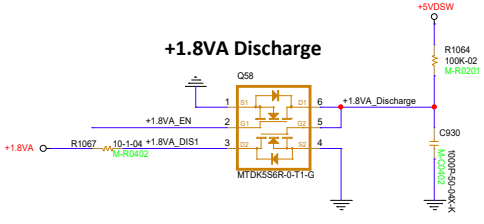
+3.3VA_EC



+1.8VA Converter



+1.8VA Discharge

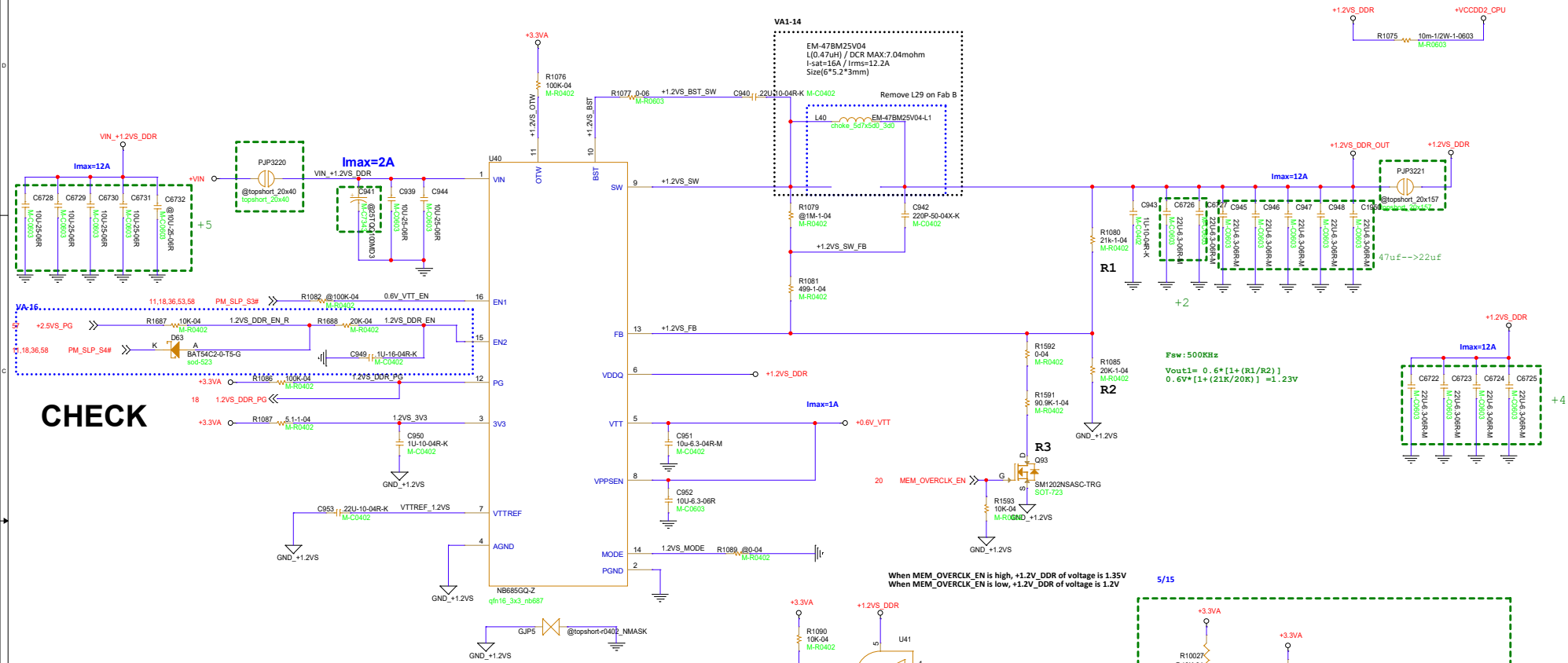


同方国际信息技术有限公司

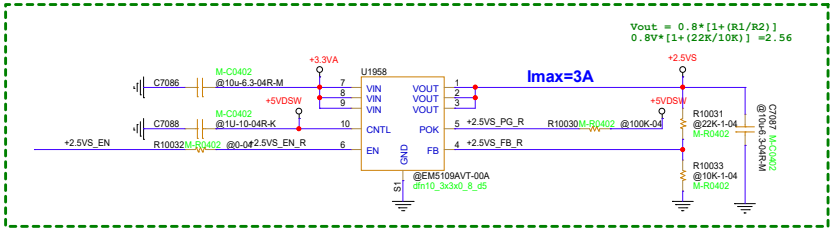
Title	POWER +1.8VA/+3.3VA_EC	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 56 of 78	

+1.2VS_DDR/+0.6V_VTT

+VCCDD2_CPU

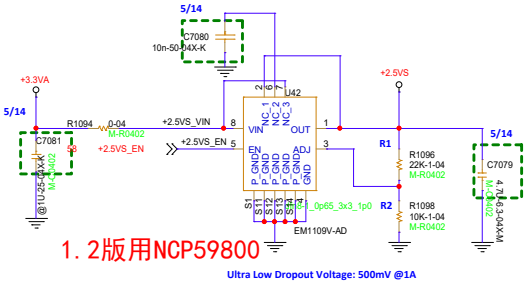


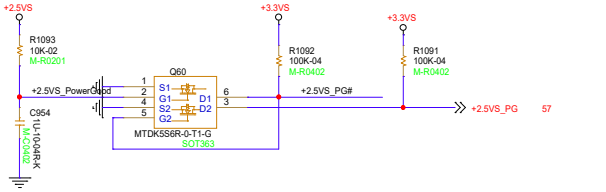
10PIN IC CO-LAY SCH 5/18



+2.5VS

Vout=0.8*(1+R1/R2)





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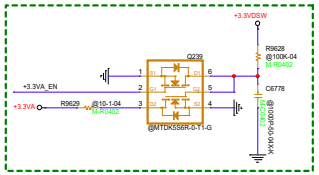
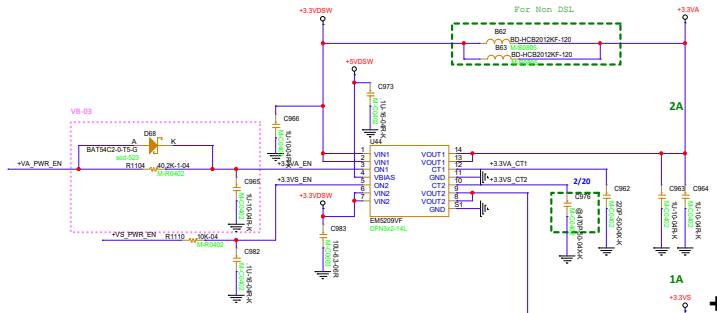
Title	POWER +1.2VS/2.5VS/VTT	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 57 of 78	

Remove +5VA

2/4 +3.3VA discharge



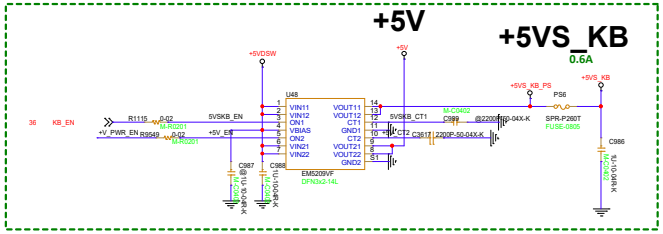
+3.3VA



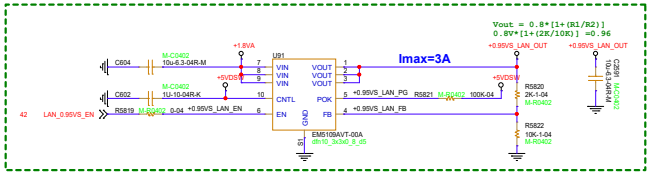
+3.3VS

+5V

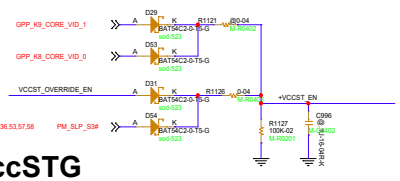
+5VS_KB



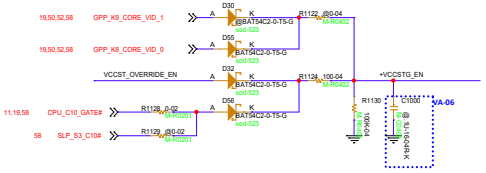
+0.95VS_LAN

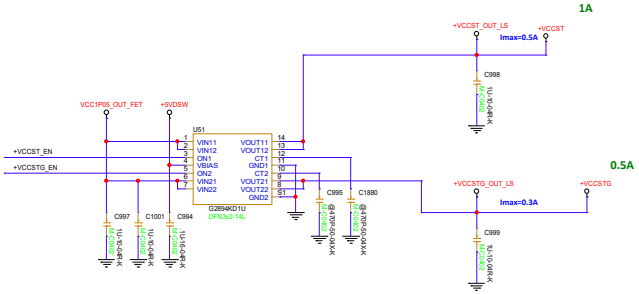


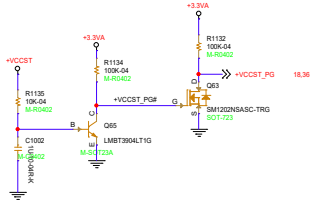
VccST

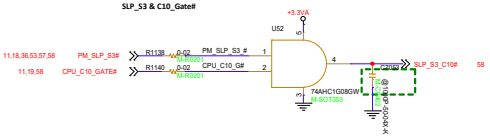


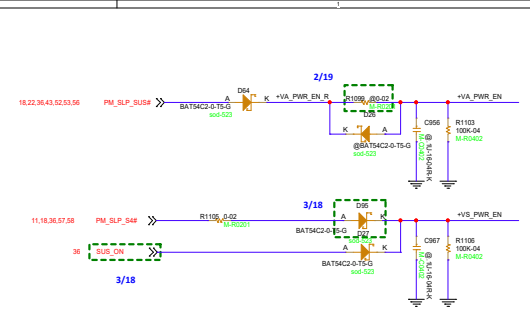
VccSTG

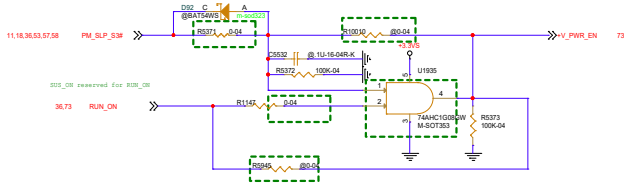


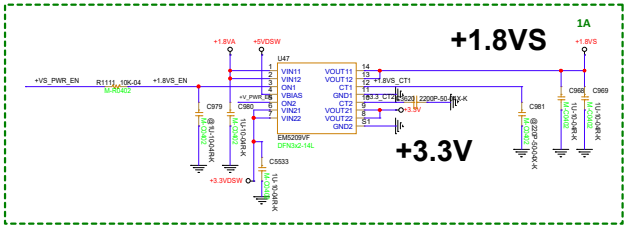




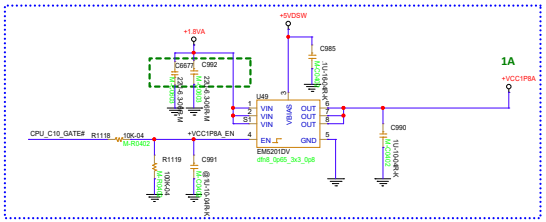


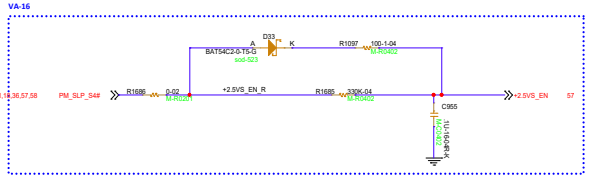






+VCC1P8A





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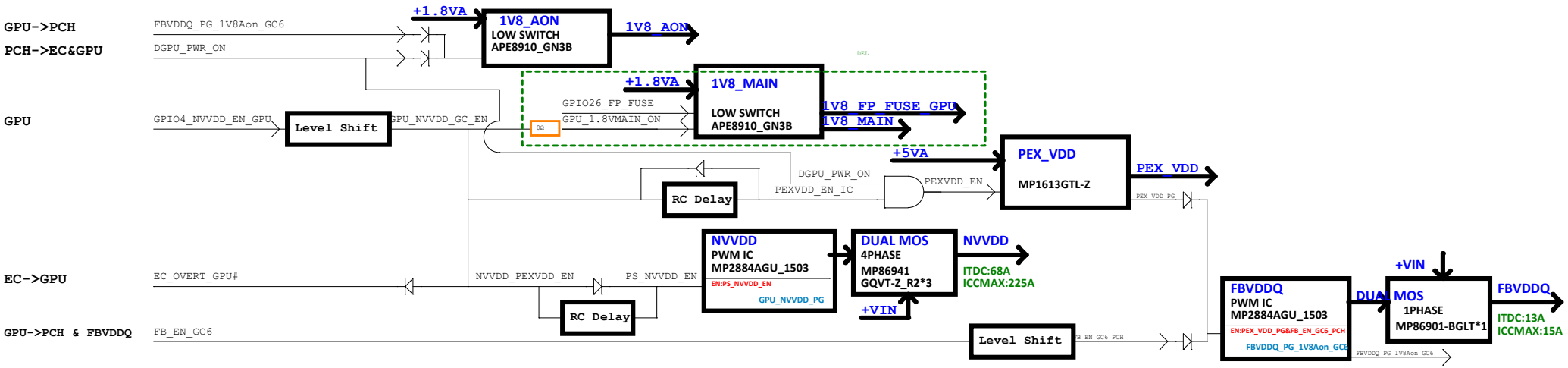
Title	POWER +VA / +VS / +V
Size: Custom	Document Number: GM5TGFX
Rev	1.2
Date: Tuesday, May 18, 2021	Sheet 58 of 78

DPU Sequence Control



NWDD/MSVDD merged: 1V8&VPP >NV_3V3>(NWDD+MSVDD)> PEXVDD> FBVDD(Q)
1, All GPU power rails must ramp up after 1V8
2, FBVDD(Q) should ramp up after VPP and PEXVDD for cold boot.

POWER ON	**+1.8V&VPP**	**NV_3V3**	**NVVDD+MSVDD**	**PEX_VDD**	**FBVDDQ**
POWER OFF	**NV_3V3**	**PEX_VDD**	**NVVDD+MSVDD**	**FBVDDQ**	**+1.8V&VPP**

POWER UP sequence is required:
1,The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2,It is recommended that the delay from 1V8 on to PEXVDD/GPU_PGOOD assertion not exceed 20ms.
3,The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4,Power up NWDD must be 90% before PEXVDD can start ramp-up .
5,Power up 1V8 must be 90% before NV_3V3 ramp up.
6,All.3V devices that connect to the GPU must be powered after 1V8: GPU cannot have any 3.3V leakage paths before GPU 1V8 power rail is present.
7,Refer to the JEDEC Memory Specification for memory-related power sequencing.

The following power-down sequence is required:
1,For GDDR6. VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
2,All 3.3V devices that connect to the GPU must be ramped down before 1V8: GPU cannot have any 3.3V leakage paths after 1.8V power-down.
3,Power down of PEXVDD must be less than 10% before NWVDD can start ramp-down.
4,Power down of NV_3V3 must be less than 10% before 1V8 can start ramp-down.

Figure 3.4 GPU Power Up Sequencing for NVVDD/MSVDD merged rail

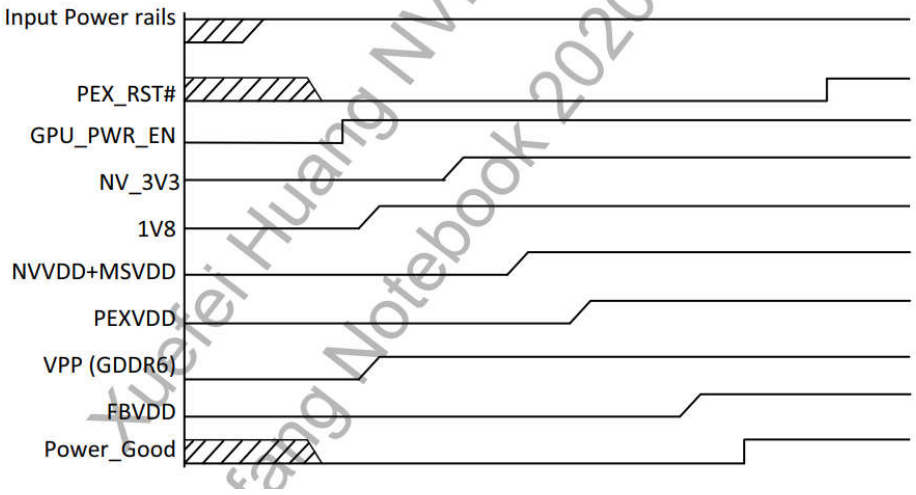
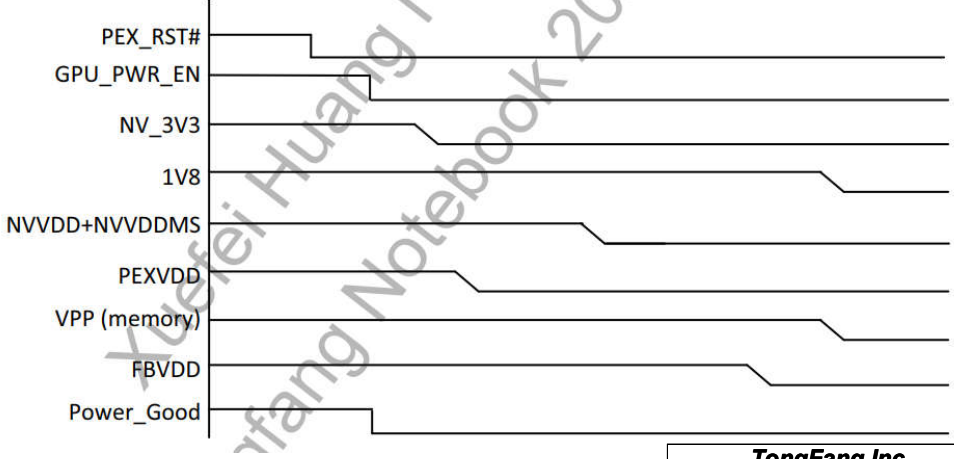
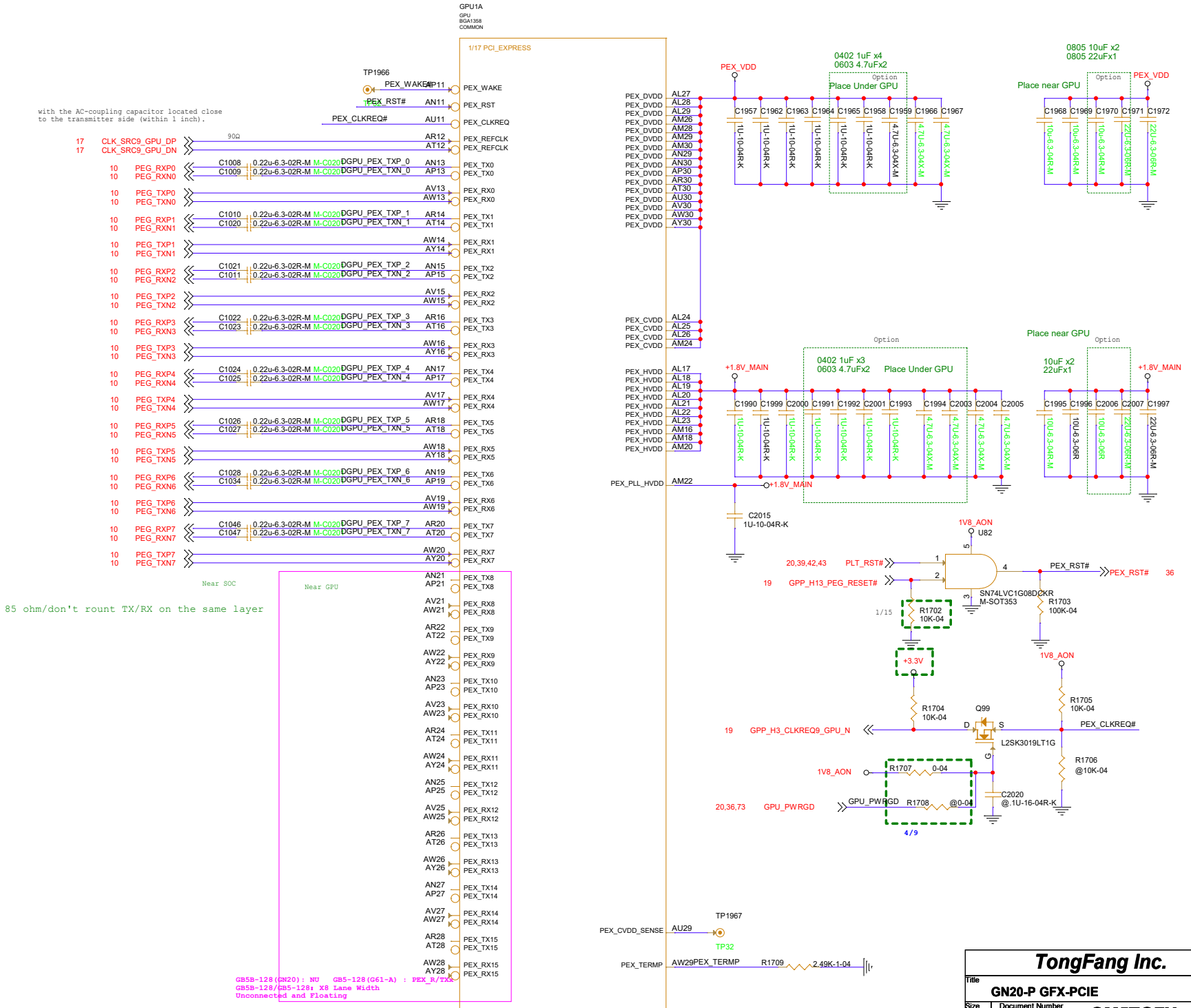


Figure 3.6 GPU Power down Sequencing for NVVDD/MSVDD merged rail



TongFang Inc.			
Title: GN20-P POWER SEQUENCE			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 59 of 78		



Company	TongFang Inc.
Title	GN20-P GFX-PCIE
Size	Custom
Document Number	GM5TGFX
Rev	1.2
Date	Tuesday, May 18, 2021
Sheet	60 of 78

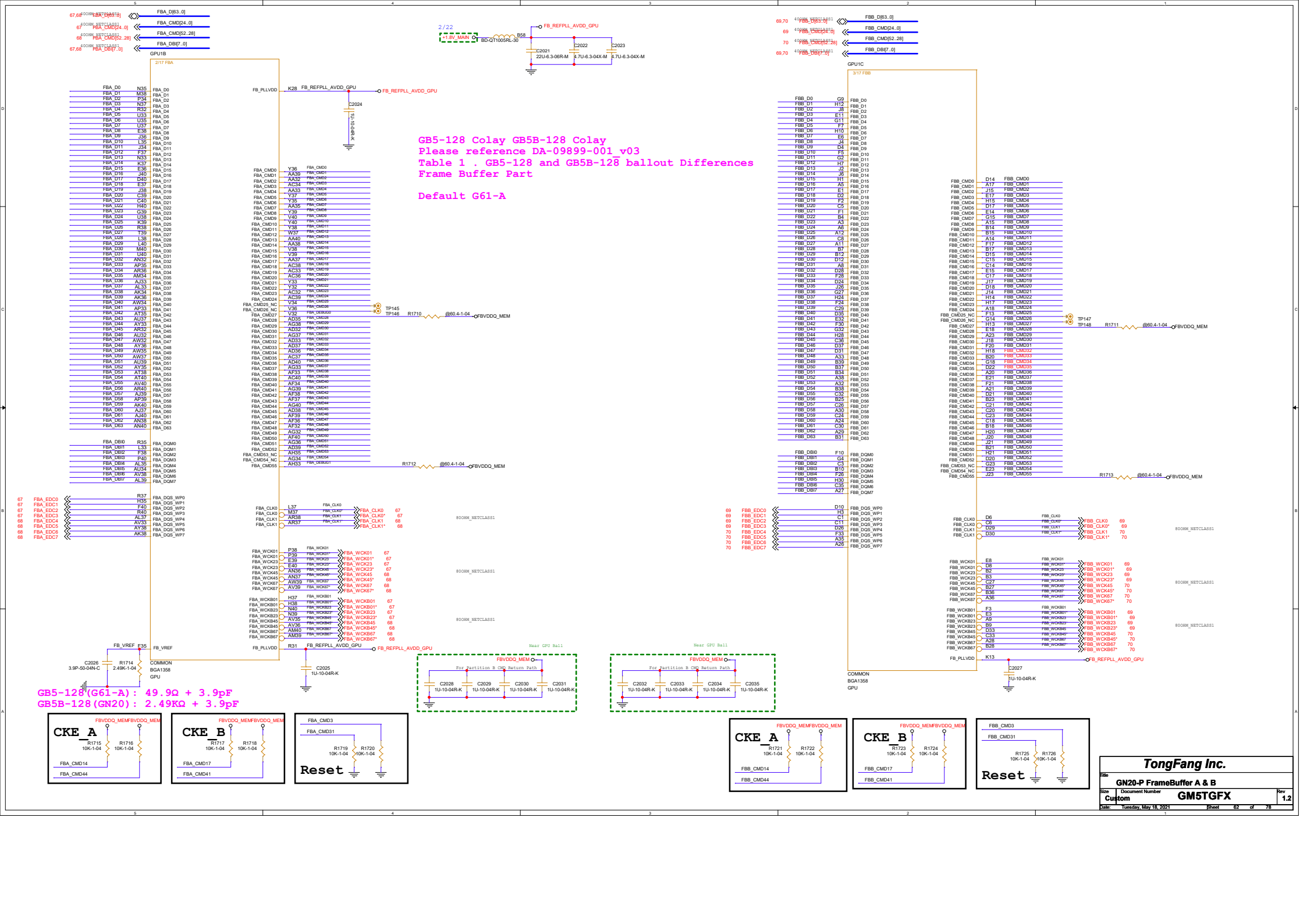
Table 6.4 GDDR6 Mode 3 Mapping, GB5-GB5-256 and GB5B-128

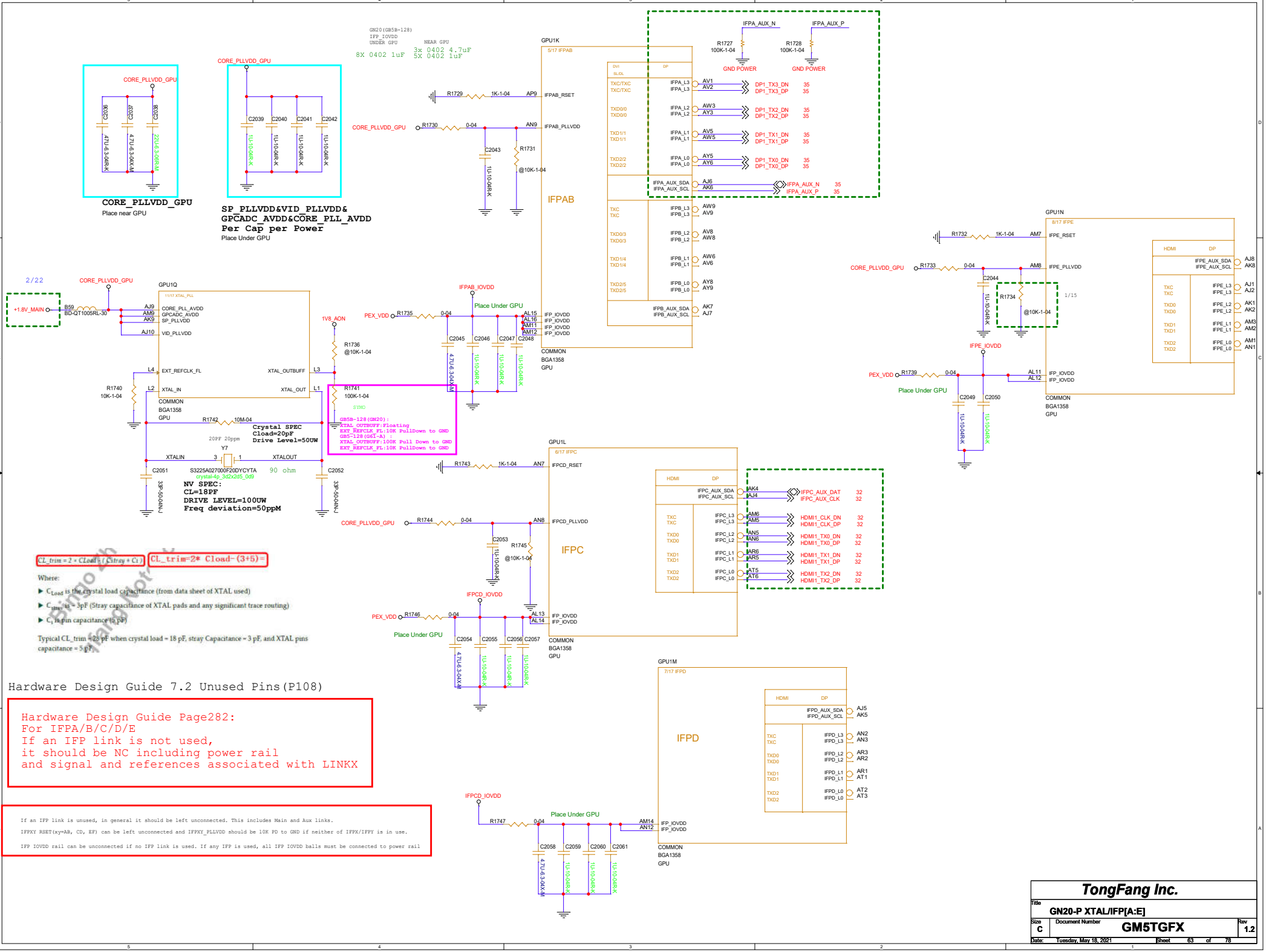
GB5-256 and GB5B-128	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB5-256 and GB5B-128	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0,1: CA8_A Bytes 2,3: -------	FBx_CMD28	Bytes 4,5: ------- Bytes 6,7: CA8_B
FBx_CMD1	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD29	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD2	Bytes 0-1: CA9_A Bytes 2,3: -------	FBx_CMD30	Bytes 4,5: ------- Bytes 6,7: CA9_B
FBx_CMD3	Bytes 0-3: RST*	FBx_CMD31	Bytes 4-7: RST*
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA9_B	FBx_CMD32	Bytes 4,5: CA9_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD33	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: ------- Bytes 2,3: CA8_B	FBx_CMD34	Bytes 4,5: CA8_A Bytes 6,7: -------
FBx_CMD7	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD35	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD8	Bytes 0,1: ------- Bytes 2,3: CA4_B	FBx_CMD36	Bytes 4,5: CA4_A Bytes 6,7: -------
FBx_CMD9	Bytes 0,1: ------- Bytes 2,3: CABI_B	FBx_CMD37	Bytes 4,5: CABI_A Bytes 6,7: -------
FBx_CMD10	Bytes 0,1: CABI_A Bytes 2,3: -------	FBx_CMD38	Bytes 4,5: ------- Bytes 6,7: CABI_B
FBx_CMD11	Bytes 0,1: CA4_A Bytes 2,3: -------	FBx_CMD39	Bytes 4,5: ------- Bytes 6,7: CA4_B
FBx_CMD12	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD40	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD13	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD41	Bytes 4,5: ------- Bytes 6,7: CKE_B
FBx_CMD14	Bytes 0,1: CKE_A Bytes 2,3: -------	FBx_CMD42	Bytes 4,5: ------- Bytes 6,7: CA5_B
FBx_CMD15	Bytes 0,1: CA5_A Bytes 2,3: -------	FBx_CMD43	Bytes 4,5: CA5_A Bytes 6,7: -------
FBx_CMD16	Bytes 0,1: ------- Bytes 2,3: CA5_B	FBx_CMD44	Bytes 4,5: CKE_A Bytes 6,7: -------
FBx_CMD17	Bytes 0,1: ------- Bytes 2,3: CKE_B	FBx_CMD45	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD18	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD46	Bytes 4,5: CA3_A Bytes 6,7: -------
FBx_CMD19	Bytes 0,1: ------- Bytes 2,3: CA7_B	FBx_CMD47	Bytes 4,5: CA7_A Bytes 6,7: -------
FBx_CMD20	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD48	Bytes 4,5: CA6_A Bytes 6,7: -------
FBx_CMD21	Bytes 0,1: ------- Bytes 2,3: CA6_B	FBx_CMD49	Bytes 4,5: ------- Bytes 6,7: CA6_B
FBx_CMD22	Bytes 0,1: CA6_A Bytes 2,3: -------	FBx_CMD50	Bytes 4,5: ------- Bytes 6,7: CA3_B
FBx_CMD23	Bytes 0,1: CA7_A Bytes 2,3: -------	FBx_CMD51	Bytes 4,5: ------- Bytes 6,7: CA7_B
FBx_CMD24	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD52	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD25	Bytes 0,1: ------- Bytes 2,3: -------	FBx_CMD53	Bytes 4,5: ------- Bytes 6,7: -------
FBx_CMD26	Bytes 0,1: ------- Bytes 2,3: -------	FBx_CMD54	Bytes 4,5: ------- Bytes 6,7: -------
GB5-256	GPU FB Channel 0 & 1		
FBx_CMD27	DEBUG0[1]		
FBx_CMD55	DEBUG1[1]		

Note:

1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

TongFang Inc.			
Title: GN20-P Frame Buffer Mapping			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 61 of 78		


GB5-128 Colay GB5B-128 Colay
Please reference DA-09899-001_v03
Table 1 . GB5-128 and GB5B-128 ballout Differences
Frame Buffer Part
Default G61-A
GB5-128(G61-A): 49.9Ω + 3.9pF
GB5B-128(GN20): 2.49KΩ + 3.9pF
GPU1B
GPU1C
COMMON
BGA1358
GPU
CKE_A
CKE_B
Reset
TongFang Inc.
GN20-P FrameBuffer A & B
GM5TGFX
Custom
Tuesday, May 18, 2021
62 of 78
1.2



$CL\_trim = 2 \times CLoad \pm (Cstray + Ci)$ $CL\_trim=2*\ Cload-(3+5)=$

Where:

- C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} is ~ 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 25 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF)

Hardware Design Guide 7.2 Unused Pins(P108)

Hardware Design Guide Page282:
For IFPA/B/C/D/E
If an IFP link is not used,
it should be NC including power rail
and signal and references associated with LINKX

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links.

IFPXY_RSET(xy=AB, CD, EF) can be left unconnected and IFPXY_PLLVDD should be 10K PD to GND if neither of IFPXY/IFPYY is in use.

IFP_IOVDD rail can be unconnected if no IFP link is used. If any IFP is used, all IFP IOVDD balls must be connected to power rail

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Title: GN20-P XTAL/IFP[A:E]			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021		Sheet 63 of 78	

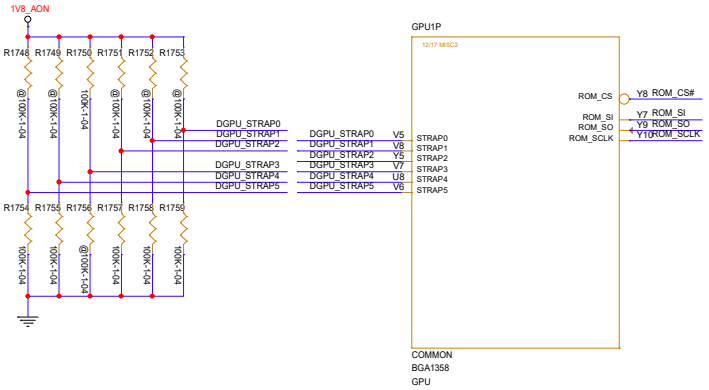


Table 4. GN20-P1/P0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

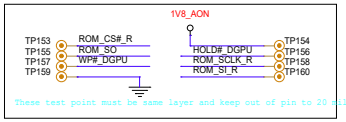
Table 9.3 RAMCFG

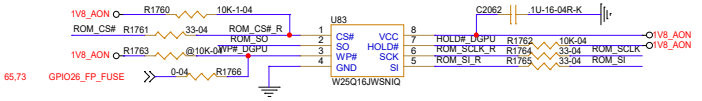
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

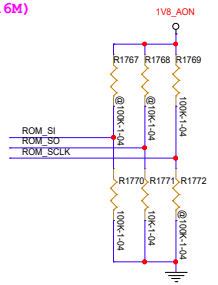




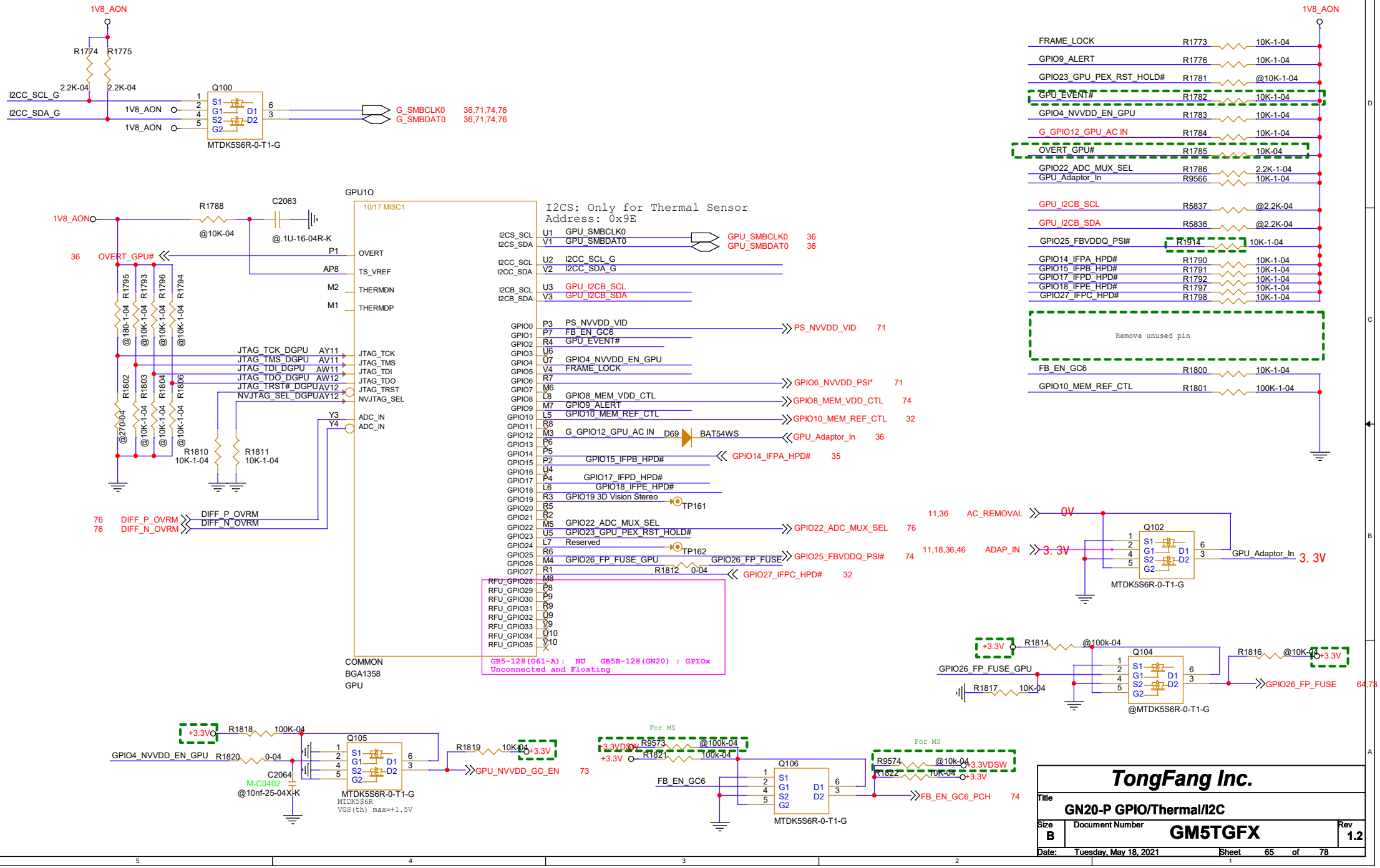
GB5-128(G61-A): OVR-M GEN1 GD25LQ80CTIGR(8M)
No need GPIO26(R1763 Stuff R1766 NU)
GB5B-128(GN20): OVR-M GEN2 W25Q16JWSNIQ(16M)
Need GPIO26(R1763 NU R1766 Stuff)

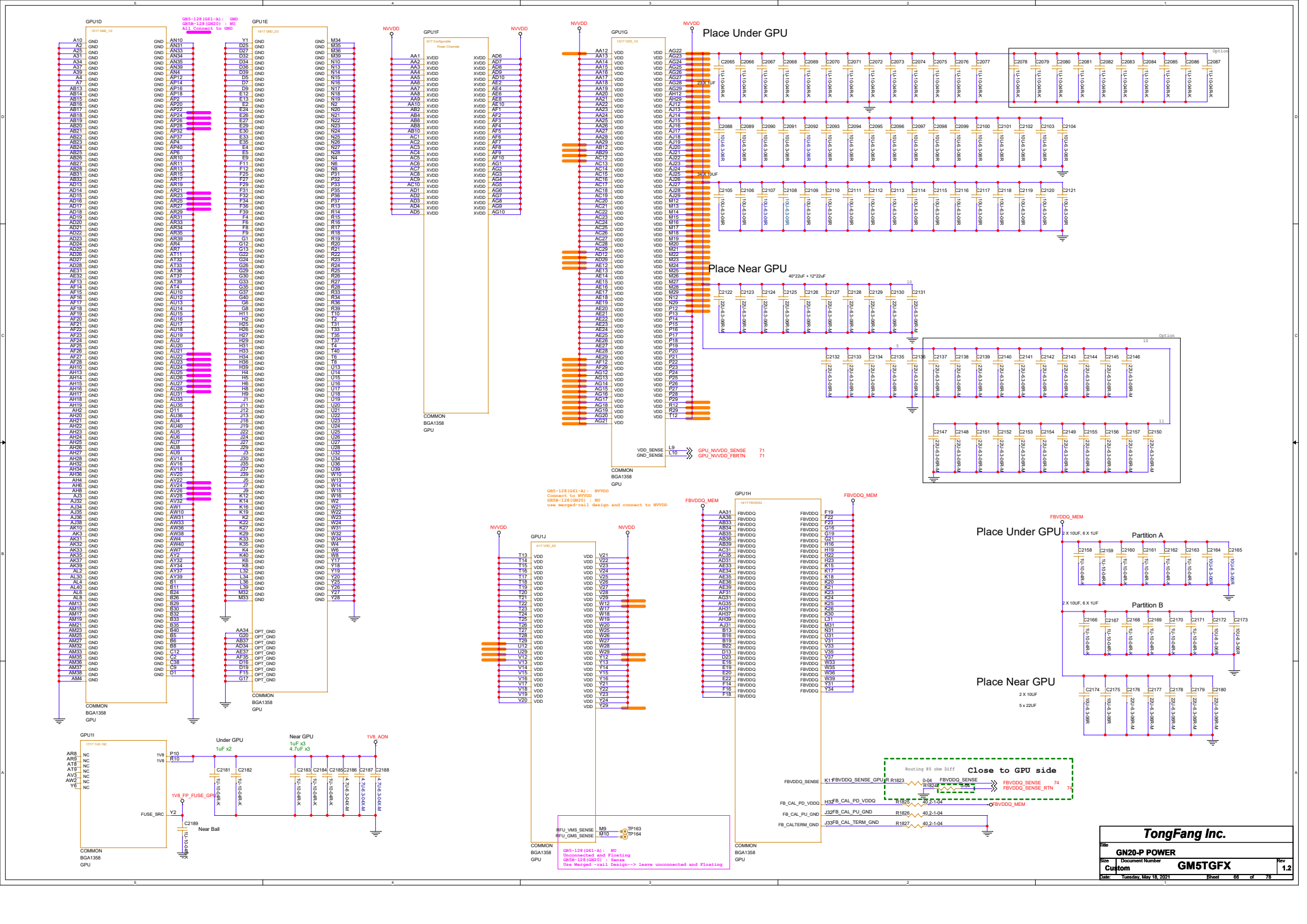
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS OVERT* Function Disabled
L	L	H	FS OVERT* Function Enabled(Default)

GB5-128	L L L to Enable FS OVERT*
GB5B-128	L L H to Enable FS OVERT*



TongFang Inc.			
Title: GN20-P STRAP/Serial ROM			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021		Sheet 64 of 78	


1V8_AON
R1774 2.2K-04
R1775 2.2K-04
I2CC_SCL_G
I2CC_SDA_G
Q100
MTDK5S6R-0-T1-G
G_SMBCLK0 36,71,74,76
G_SMBDAT0 36,71,74,76
GPU1O
10/17 MISC1
I2CS: Only for Thermal Sensor
Address: 0x9E
R1788 @10K-04
C2063 @.1U-16-04R-K
OVERT_GPU#
TS_VREF
THERMDN
THERMDP
JTAG_TCK_DGPU
JTAG_TMS_DGPU
JTAG_TDI_DGPU
JTAG_TDO_DGPU
JTAG_TRST#_DGPU
NVJTAG_SEL_DGPU
ADC_IN
R1810 10K-1-04
R1811 10K-1-04
DIFF_P_OVRM
DIFF_N_OVRM
GPU_SMBCLK0
GPU_SMBDAT0
I2CC_SCL_G
I2CC_SDA_G
GPU_I2CB_SCL
GPU_I2CB_SDA
PS_NVVDD_VID
FB_EN_GC6
GPU_EVENT#
GPIO4_NVVDD_EN_GPU
FRAME_LOCK
GPIO6_NVVDD_PSI*
GPIO8_MEM_VDD_CTL
GPIO9_ALERT
GPIO10_MEM_REF_CTL
G_GPIO12_GPU_AC IN
D69 BAT54WS
GPU_Adaptor_In
GPIO14_IFPA_HPD#
GPIO15_IFPB_HPD#
GPIO17_IFPD_HPD#
GPIO18_IFPE_HPD#
GPIO19 3D Vision Stereo
TP161
GPIO22_ADC_MUX_SEL
GPIO23_GPU_PEX_RST_HOLD#
Reserved
TP162
GPIO26_FP_FUSE_GPU
GPIO25_FBVDDQ_PSI#
R1812 0-04
GPIO27_IFPC_HPD#
RFU_GPIO28
RFU_GPIO29
RFU_GPIO30
RFU_GPIO31
RFU_GPIO32
RFU_GPIO33
RFU_GPIO34
RFU_GPIO35
GB5-128(G61-A): NU GB5B-128(GN20) : GPIOx
Unconnected and Floating
COMMON
BGA1358
GPU
1V8_AON
FRAME_LOCK R1773 10K-1-04
GPIO9_ALERT R1776 10K-1-04
GPIO23_GPU_PEX_RST_HOLD# R1781 @10K-1-04
GPU_EVENT# R1782 10K-1-04
GPIO4_NVVDD_EN_GPU R1783 10K-1-04
G_GPIO12_GPU_AC IN R1784 10K-1-04
OVERT_GPU# R1785 10K-04
GPIO22_ADC_MUX_SEL R1786 2.2K-1-04
GPU_Adaptor_In R9566 10K-1-04
GPU_I2CB_SCL R5837 @2.2K-04
GPU_I2CB_SDA R5836 @2.2K-04
GPIO25_FBVDDQ_PSI# R1914 10K-1-04
GPIO14_IFPA_HPD# R1790 10K-1-04
GPIO15_IFPB_HPD# R1791 10K-1-04
GPIO17_IFPD_HPD# R1792 10K-1-04
GPIO18_IFPE_HPD# R1797 10K-1-04
GPIO27_IFPC_HPD# R1798 10K-1-04
Remove unused pin
FB_EN_GC6 R1800 10K-1-04
GPIO10_MEM_REF_CTL R1801 100K-1-04
AC_REMOVAL 0V
ADAP_IN 3. 3V
Q102
MTDK5S6R-0-T1-G
GPU_Adaptor_In 3. 3V
+3.3V R1814 @100k-04
GPIO26_FP_FUSE_GPU
R1817 10K-04
Q104
@MTDK5S6R-0-T1-G
R1816 @10K-04 +3.3V
GPIO26_FP_FUSE
+3.3V R1818 100K-04
GPIO4_NVVDD_EN_GPU R1820 0-04
C2064 M-C0402 @10nf-25-04X-K
Q105
MTDK5S6R-0-T1-G
MTDK5S6R
VGS(th) max=+1.5V
R1819 10K-04 +3.3V
GPU_NVVDD_GC_EN
For MS
+3.3VDSW R9573 @100k-04
+3.3V R1821 100k-04
FB_EN_GC6
Q106
MTDK5S6R-0-T1-G
R9574 @10k-04 +3.3VDSW
R1822 10K-04 +3.3V
FB_EN_GC6_PCH
TongFang Inc.
Title
GN20-P GPIO/Thermal/I2C
Size B
Document Number GM5TGFX
Rev 1.2
Date: Tuesday, May 18, 2021
Sheet 65 of 78


GPU1D
GPU1E
GPU1F
GPU1G
GPU1H
GPU1J
GPU1I
COMMON
BGA1358
GPU
Place Under GPU
Place Near GPU
Under GPU
Near GPU
Near Ball
NVVDD
FBVDDQ_MEM
1V8_AON
Partition A
Partition B
2 X 10UF, 6 X 1UF
2 X 10UF
5 x 22UF
40*22uF + 12*22uF
220X 1UF
34X 10UF
Close to GPU side
Routing 85 ohm Diff
FBVDDQ_SENSE
FBVDDQ_SENSE_RTN
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
VDD_SENSE
GND_SENSE
GPU_NVVDD_SENSE
GPU_NVVDD_FBRTN
RFU_VMS_SENSE
RFU_GMS_SENSE
GB5-128(G61-A) : GND
GB5B-128(GN20) : NO
All Connect to GND
GB5-128(G61-A) : NVVDD
Connect to NVVDD
GB5B-128(GN20) : NO
use merged-rail design and connect to NVVDD
GB5-128(G61-A) : NO
Unconnected and Floating
GB5B-128(GN20) : Sense
Use Merged -rail Design--> leave unconnected and Floating
TongFang Inc.
GN20-P POWER
GM5TGFX
Custom
1.2
Tuesday, May 18, 2021
Sheet 68 of 78

62 FBA_D[31..0] — FBA_D[31..0]

62 FBA_DBI[3..0] — FBA_DBI[3..0]

62 FBA_CMD[24..0] — FBA_CMD[24..0]

62 FBA_EDC[3..0] — FBA_EDC[3..0]

Maximum VRAM case Temp is 85 celsius degree

VRAM1A

?

FBGA180

COMMON

NORMAL

FBA_D9	B4	DQ0_A
FBA_D13	A3	DQ1_A
FBA_D10	B3	DQ2_A
FBA_D14	B2	DQ3_A
FBA_D12	E3	DQ4_A
FBA_D15	E2	DQ5_A
FBA_D8	F2	DQ6_A
FBA_D11	G2	DQ7_A
FBA_EDC1	C2	EDC0_A
FBA_DBI1	D2	DBI0_A
62 FBA_WCKB01	D4	WCK0_t_A
62 FBA_WCKB01*	D5	WCK0_c_A
FBA_D6	B11	DQ8_A
FBA_D4	A12	DQ9_A
FBA_D5	B12	DQ10_A
FBA_D7	B13	DQ11_A
FBA_D1	E12	DQ12_A
FBA_D2	E13	DQ13_A
FBA_D0	F13	DQ14_A
FBA_D3	G13	DQ15_A
FBA_EDC0	C13	EDC1_A
FBA_DBI0	D13	DBI1_A
62 FBA_WCK01	D11	WCK1_t_A
62 FBA_WCK01*	D10	WCK1_c_A

x16 | x8

VRAM1B

?

FBGA180

COMMON

NORMAL

FBA_D16	U4	DQ0_B
FBA_D22	V3	DQ1_B
FBA_D23	U3	DQ2_B
FBA_D17	U2	DQ3_B
FBA_D19	P3	DQ4_B
FBA_D21	P2	DQ5_B
FBA_D20	N2	DQ6_B
FBA_D18	M2	DQ7_B
FBA_EDC2	T2	EDC0_B
FBA_DBI2	R2	DBI0_B
62 FBA_WCK23	R4	WCK0_t_B
62 FBA_WCK23*	R5	WCK0_c_B
FBA_D25	U11	DQ8_B
FBA_D29	V12	DQ9_B
FBA_D28	U12	DQ10_B
FBA_D30	U13	DQ11_B
FBA_D27	P12	DQ12_B
FBA_D26	P13	DQ13_B
FBA_D31	N13	DQ14_B
FBA_D24	M13	DQ15_B
FBA_EDC3	T13	EDC1_B
FBA_DBI3	R13	DBI1_B
62 FBA_WCKB23	R11	WCK1_t_B
62 FBA_WCKB23*	R10	WCK1_c_B

x16 | x8

DECOUPLING FOR ONE DRAM

CLOSE or UNDER DRAM

0402 1uF x18

0603 10uF x 4

FBVDDQ_MEM

C2190 C2191 C2192 C2193 C2194 C2195 C2196 C2197 C2198 C2199 C2200 C2201 C2202 C2203 C2204 C2205 C2206 C2207 — 1U-1004R-K

C2208 C2209 C2210 C2211 — 10U-6.3-06R

AROUND DRAM

0603 10uF x2

0603 22uF x 6

330uF POSCAP x1

C2212 C2213 C2214 C2215 C2216 C2217 C2218 C2219 — 10U-6.3-06R / 22U-6.3-06R-M

C2220 C2221 C2222 C2223 C2224 C2225 C2226 C2227 C2228 C2229 C2230 C2231 C2232 C2233 — 22U-6.3-06R-M

C6680 — EEFSTD0J33R

Replace Poscap

VRAM1C

?

FBGA180

COMMON

FBA_CMD1	H3	CA0_A
FBA_CMD13	G11	CA1_A
FBA_CMD12	G4	CA2_A
FBA_CMD24	H12	CA3_A
FBA_CMD11	H5	CA4_A
FBA_CMD15	H10	CA5_A
FBA_CMD22	J12	CA6_A
FBA_CMD23	J11	CA7_A
FBA_CMD0	J4	CA8_A
FBA_CMD2	J3	CA9_A
FBA_CMD10	J5	CABI_A
FBA_CMD14	G10	CKE_A
VREFC	K1	
C2234 R1829	@820P-50-04X-K / 1K-1-04	
TCK	N5	
TDI	F10	
TDO	N10	
TMS	C5	
FBA_CMD5	L3	CA0_B
FBA_CMD18	M11	CA1_B
FBA_CMD7	M4	CA2_B
FBA_CMD20	L12	CA3_B
FBA_CMD8	L5	CA4_B
FBA_CMD16	L10	CA5_B
FBA_CMD21	K12	CA6_B
FBA_CMD19	K11	CA7_B
FBA_CMD6	K4	CA8_B
FBA_CMD4	K3	CA9_B
FBA_CMD9	K5	CABI_B
FBA_CMD17	M10	CKE_B
ZQ_A	J14	FBA_ZQ1_A
ZQ_B	K14	FBA_ZQ1_B
R1831 121-1-04 / R1832 121-1-04		
FBA_CMD3	J1	RESET
62 FBA_CLK0*	K10	CLK_c
62 FBA_CLK0	J10	CLK_t
RFU_A	G5	
RFU_B	G6	

DEL 4/10

VRAM1D

?

FBGA180

COMMON

VSS: A11 A13 A2 A4 B1 B14 C10 C12 C3 C5 D1 D12 D14 D3 E11 E4 F1 F12 F14 F3 G1 G12 G14 G3 H11 H4 L11 L4 M1 M12 M14 M3 N1 N12 N14 N3 P11 P4 R1 R12 R14 R3 T10 T12 T3 T5 U1 U14 V11 V13 V2 V4

FBVDDQ_MEM

VDD: A1 A14 E10 E5 H13 H2 L13 L2 P10 P5 V1 V14

FBVDDQ_MEM

VDDQ: B10 B5 C1 C11 C14 C4 E1 E14 F11 F4 H1 H14 J13 J2 K13 K2 L1 L14 N11 N4 P1 P14 T1 T11 T14 T4 U10 U5

1V8_AON

VPP: A10 A5 V10 V5

Close to DRAM 0402 1uF x4

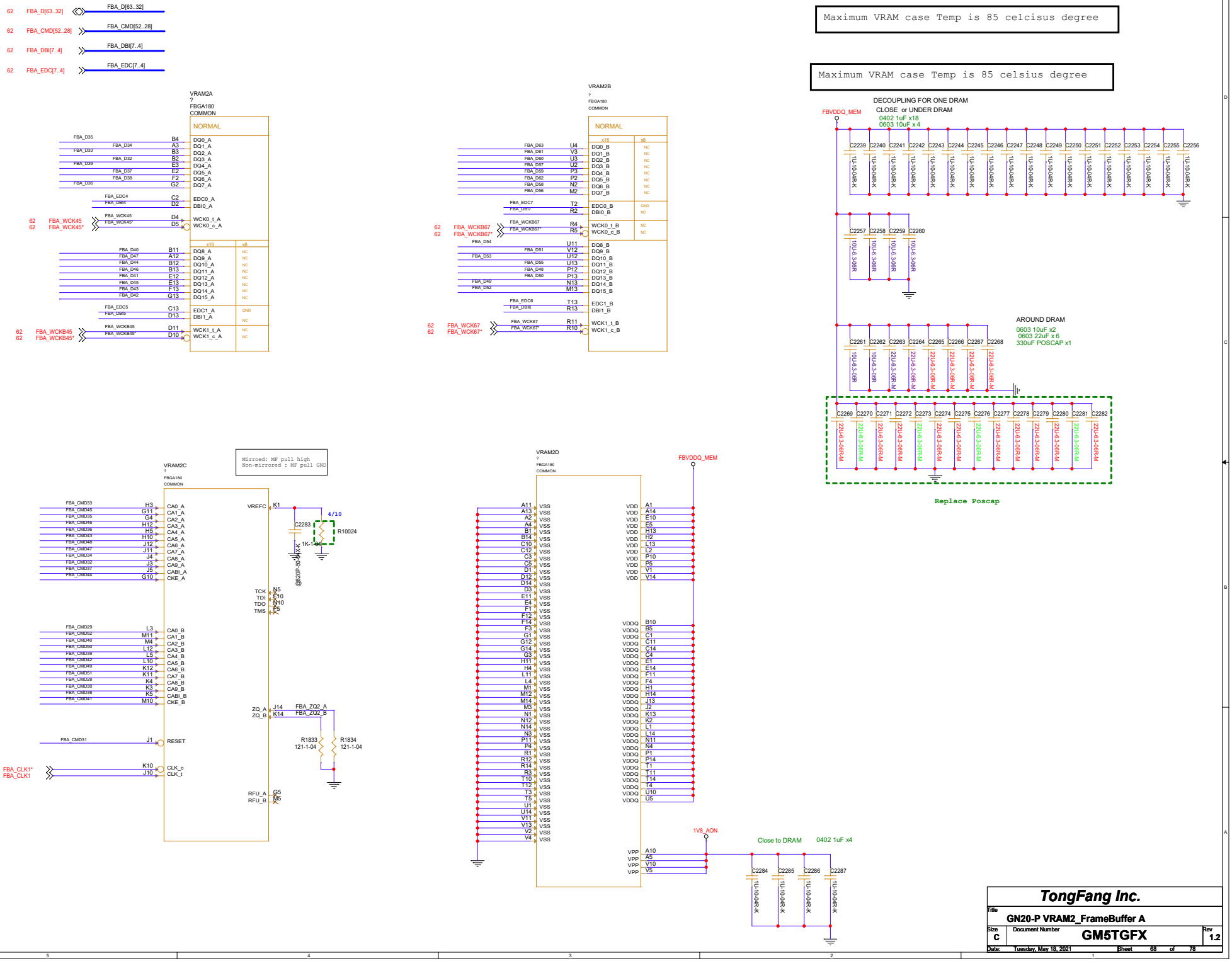
C2235 C2236 C2237 C2238 — 1U-10-04R-K

Title	GN20-P VRAM1_FrameBuffer A	
Size C	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 67 of 78	

TongFang Inc.

Maximum VRAM case Temp is 85 celcisus degree

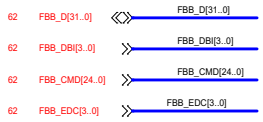
Maximum VRAM case Temp is 85 celsius degree

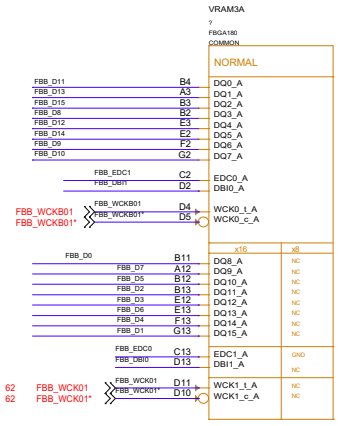


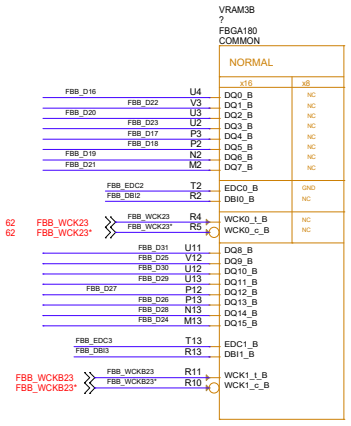
TongFang Inc.			
Title	GN20-P VRAM2_FrameBuffer A		
Size C	Document Number GM5TGFX		Rev 1.2
Date: Tuesday, May 18, 2021		Sheet 68 of 78	

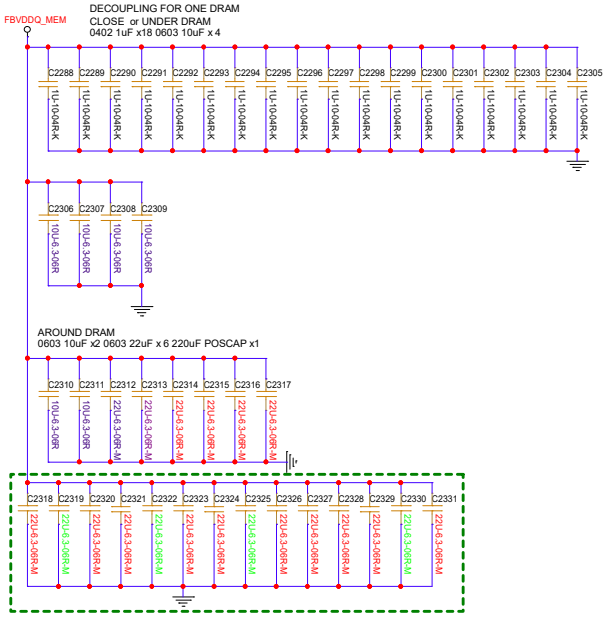
Maximum VRAM case Temp is 85 celcisus degree

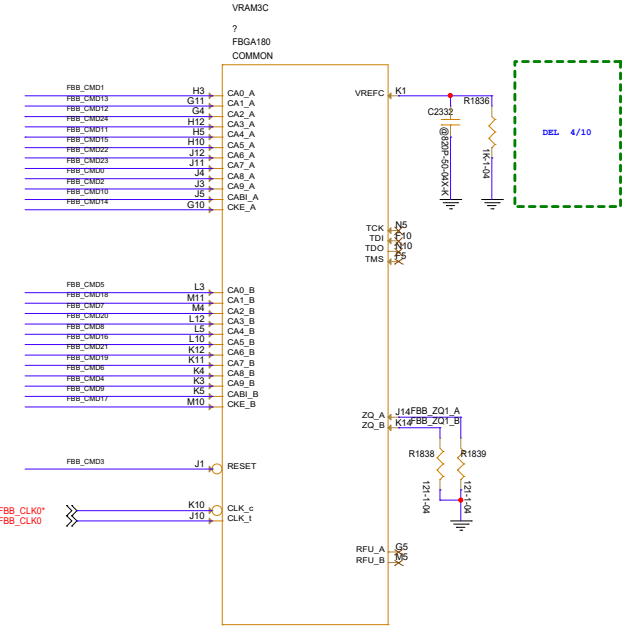
Maximum VRAM case Temp is 85 celsius degree

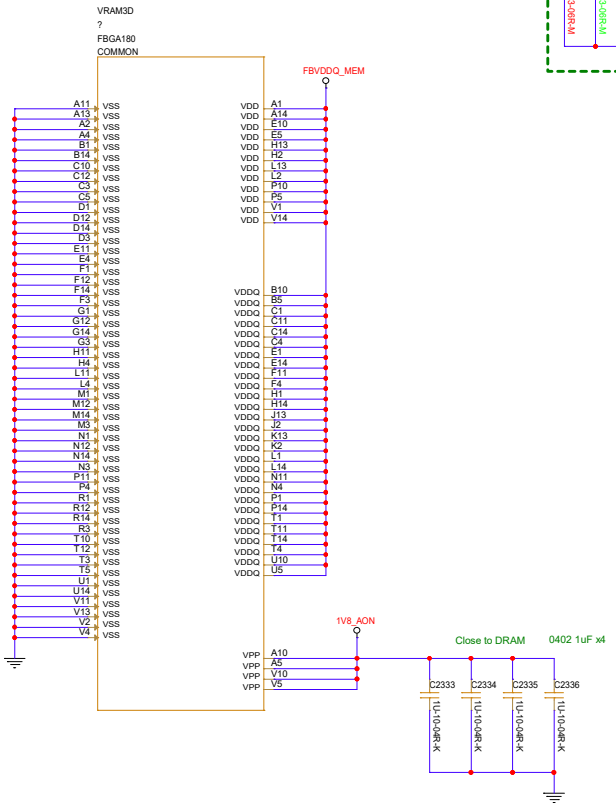












TongFang Inc.			
Title: GN20-P VRAM3_FrameBuffer B			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 69 of 78		

Maximum VRAM case Temp is 85 celcisus degree

Maximum VRAM case Temp is 85 celsius degree

62 FBB_DBI[7..4] — FBB_DBI[7..4]

62 FBB_D[63..32] — FBB_D[63..32]

62 FBB_CMD[52..28] — FBB_CMD[52..28]

62 FBB_EDC[7..4] — FBB_EDC[7..4]

VRAM4A
?
FBGA180
COMMON
NORMAL

FBB_D38 B4 DQ0_A
FBB_D35 A3 DQ1_A
FBB_D37 B3 DQ2_A
FBB_D34 B2 DQ3_A
FBB_D39 E3 DQ4_A
FBB_D36 E2 DQ5_A
FBB_D33 F2 DQ6_A
FBB_D32 G2 DQ7_A
FBB_EDC4 C2 EDC0_A
FBB_DBI4 D2 DBI0_A
62 FBB_WCK45 FBB_WCK45* D4 D5 WCK0_t_A WCK0_c_A
FBB_D41 B11 DQ8_A
FBB_D44 A12 DQ9_A
FBB_D42 B12 DQ10_A
FBB_D47 B13 DQ11_A
FBB_D40 E12 DQ12_A
FBB_D46 E13 DQ13_A
FBB_D45 F13 DQ14_A
FBB_D43 G13 DQ15_A
FBB_EDC5 C13 EDC1_A
FBB_DBI5 D13 DBI1_A
62 FBB_WCKB45 FBB_WCKB45* D11 D10 WCK1_t_A WCK1_c_A

VRAM4B
?
FBGA180
COMMON
NORMAL

FBB_D63 U4 DQ0_B
FBB_D58 V3 DQ1_B
FBB_D61 U3 DQ2_B
FBB_D62 U2 DQ3_B
FBB_D56 P3 DQ4_B
FBB_D57 P2 DQ5_B
FBB_D60 N2 DQ6_B
FBB_D59 M2 DQ7_B
FBB_EDC7 T2 EDC0_B
FBB_DBI7 R2 DBI0_B
62 FBB_WCKB67 FBB_WCKB67* R4 R5 WCK0_t_B WCK0_c_B
FBB_D53 U11 DQ8_B
FBB_D48 V12 DQ9_B
FBB_D51 U12 DQ10_B
FBB_D50 U13 DQ11_B
FBB_D55 P12 DQ12_B
FBB_D52 P13 DQ13_B
FBB_D54 N13 DQ14_B
FBB_D49 M13 DQ15_B
FBB_EDC6 T13 EDC1_B
FBB_DBI6 R13 DBI1_B
62 FBB_WCK67 FBB_WCK67* R11 R10 WCK1_t_B WCK1_c_B

DECOUPLING FOR ONE DRAM
CLOSE or UNDER DRAM
0402 1uF x18 0603 10uF x 4

FBVDDQ_MEM

C2337 C2338 C2339 C2340 C2341 C2342 C2343 C2344 C2345 C2346 C2347 C2348 C2349 C2350 C2351 C2352 C2353 C2354 — 1U-1004R-K
C2355 C2356 C2357 C2358 — 10U-6.3-06R

AROUND DRAM
0603 10uF x2 0603 22uF x 6 220uF POSCAP x1

C2359 C2360 — 10U-6.3-06R
C2361 C2362 C2363 C2364 C2365 C2366 — 22U-6.3-06R-M
C2367 C2368 C2369 C2370 C2371 C2372 C2373 C2374 C2375 C2376 C2377 C2378 C2379 C2380 — 22U-6.3-06R-M
C6681 — EEFSTD0J331R

Replace Poscap

VRAM4C
?
FBGA180
COMMON

FBB_CMD33 H3 CA0_A
FBB_CMD45 G11 CA1_A
FBB_CMD35 G4 CA2_A
FBB_CMD46 H12 CA3_A
FBB_CMD36 H5 CA4_A
FBB_CMD43 H10 CA5_A
FBB_CMD48 J12 CA6_A
FBB_CMD47 J11 CA7_A
FBB_CMD34 J4 CA8_A
FBB_CMD32 J3 CA9_A
FBB_CMD37 J5 CABI_A
FBB_CMD44 G10 CKE_A
VREFC K1 — C2381 1K-1-04 4/10 R10025 @820P-50-04X-K
TCK N5
TDI P10
TDO N10
TMS P5
FBB_CMD29 L3 CA0_B
FBB_CMD52 M11 CA1_B
FBB_CMD40 M4 CA2_B
FBB_CMD50 L12 CA3_B
FBB_CMD39 L5 CA4_B
FBB_CMD42 L10 CA5_B
FBB_CMD49 K12 CA6_B
FBB_CMD51 K11 CA7_B
FBB_CMD28 K4 CA8_B
FBB_CMD30 K3 CA9_B
FBB_CMD38 K5 CABI_B
FBB_CMD41 M10 CKE_B
FBB_CMD31 J1 RESET
62 FBB_CLK1* FBB_CLK1 K10 J10 CLK_c CLK_t
ZQ_A J14 FBB_ZQ2_A
ZQ_B K14 FBB_ZQ2_B
R1840 121-1-04 R1841 121-1-04
RFU_A G5
RFU_B M5

VRAM4D
?
FBGA180
COMMON

FBVDDQ_MEM

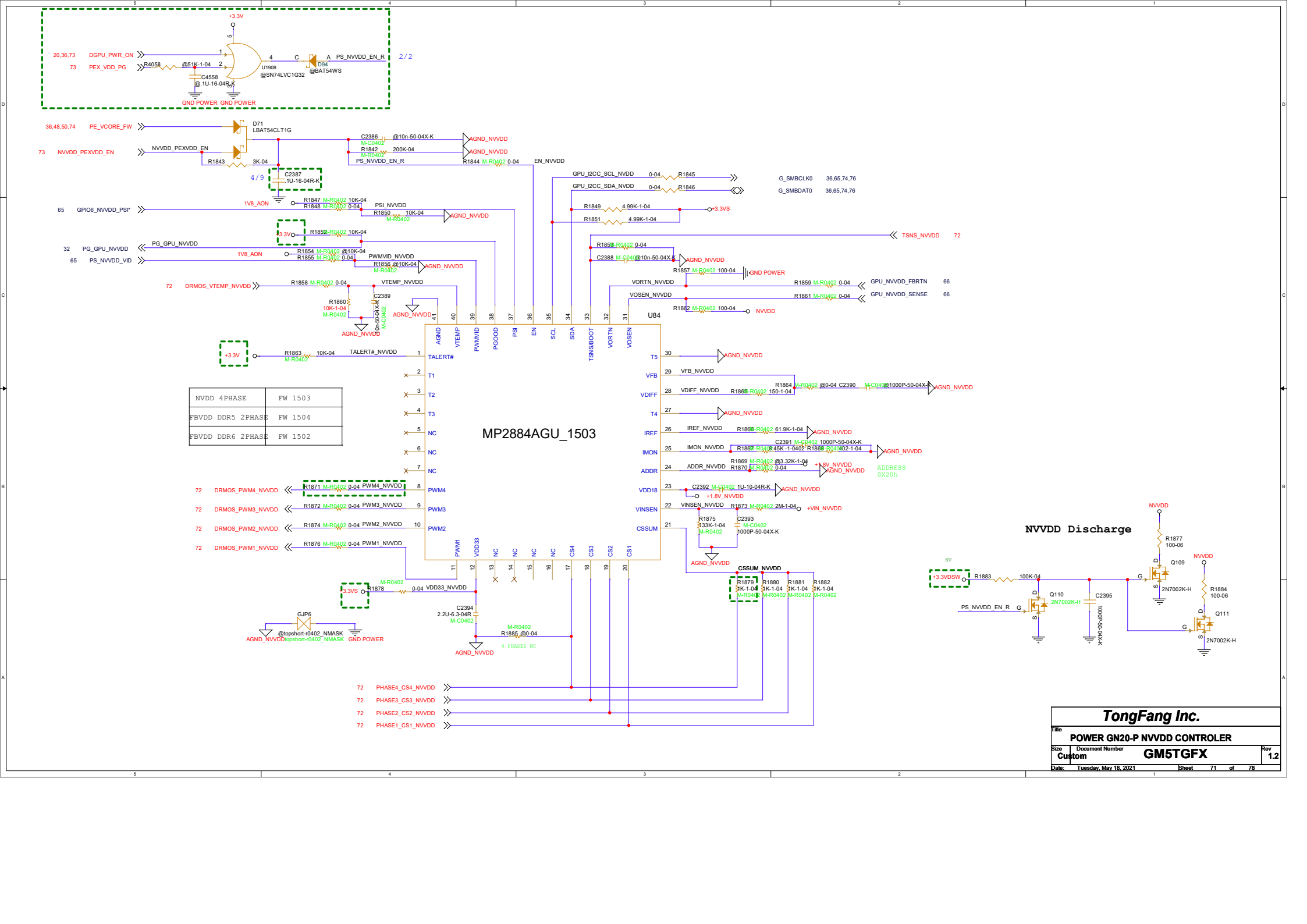
VSS: A11 A13 A2 A4 B1 B14 C10 C12 C3 C5 D1 D12 D14 D3 E11 E4 F1 F12 F14 F3 G1 G12 G14 G3 H11 H4 L11 L4 M1 M12 M14 M3 N1 N12 N14 N3 P11 P4 R1 R12 R14 R3 T10 T12 T3 T5 U1 U14 V11 V13 V2 V4
VDD: A1 A14 E10 E5 H13 H2 L13 L2 P10 P5 V1 V14
VDDQ: B10 B5 C1 C11 C14 C4 E1 E14 F11 F4 H1 H14 J13 J2 K13 K2 L1 L14 N11 N4 P1 P14 T1 T11 T14 T4 U10 U5
VPP: A10 A5 V10 V5

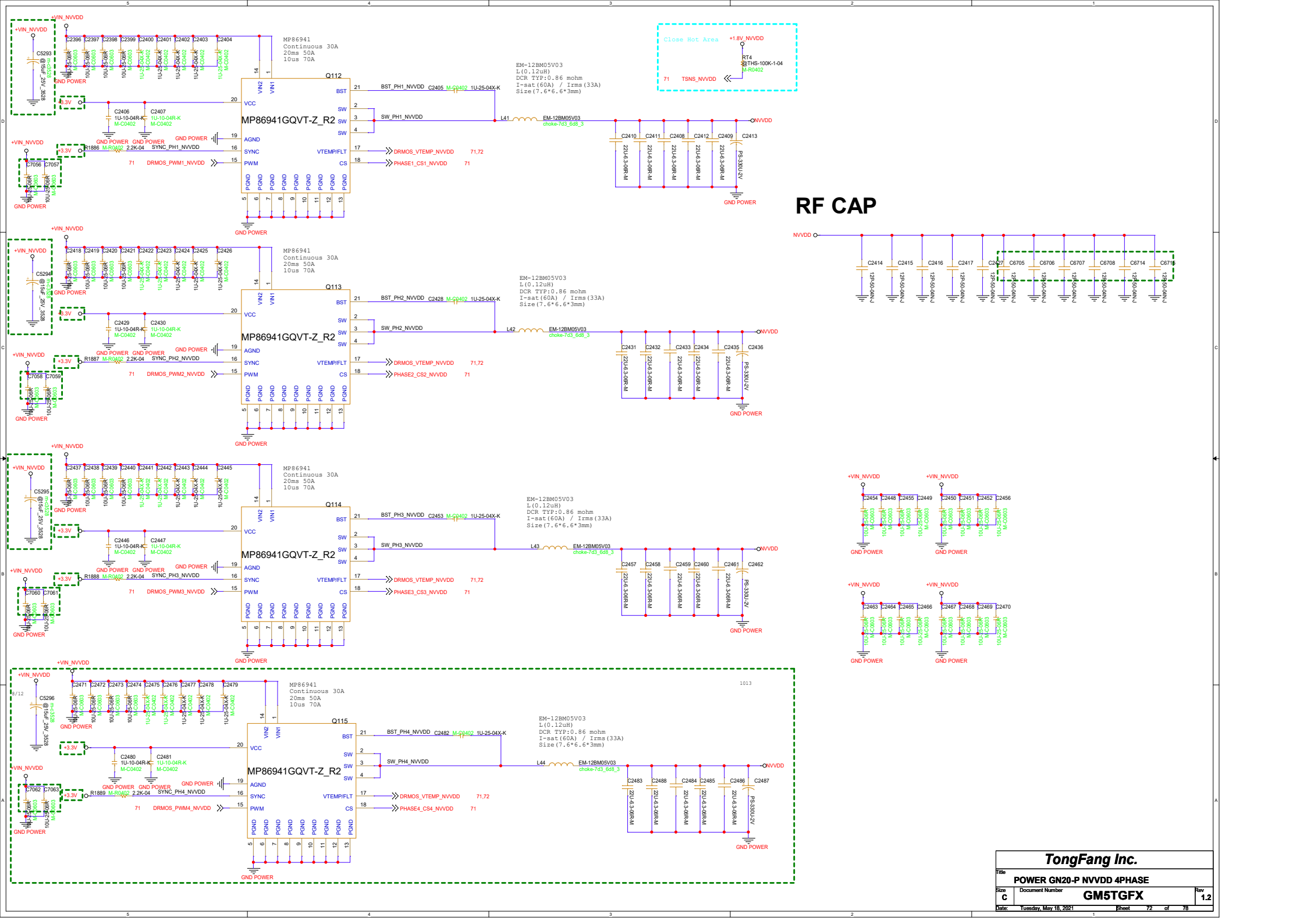
1V8_AON

Close to DRAM 0402 1uF x4

C2382 C2383 C2384 C2385 — 1U-10-04R-K

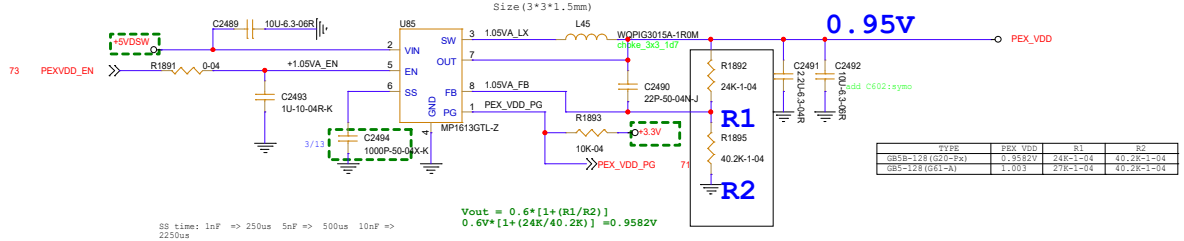
TongFang Inc.			
Title: GN20-P VRAM4_FrameBuffer B			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 70 of 78		


MP2884AGU_1503
U84
NVDD Discharge
NVDD 4PHASE FW 1503
FBVDD DDR5 2PHASE FW 1504
FBVDD DDR6 2PHASE FW 1502
TongFang Inc.
POWER GN20-P NVDD CONTROLER
GM5TGFX
Custom
Tuesday, May 18, 2021
Sheet 71 of 78


MP86941
Continuous 30A
20ms 50A
10us 70A
MP86941GQVT-Z_R2
Q112
Q113
Q114
Q115
EM-12BM05V03
L(0.12uH)
DCR TYP:0.86 mohm
I-sat(60A) / Irms(33A)
Size(7.6*6.6*3mm)
Close Hot Area
+1.8V_NVDDD
RT4
THS-100K-1-04
TSNS_NVDDD
RF CAP
NVDDD
TongFang Inc.
POWER GN20-P NVDDD 4PHASE
GM5TGFX
Rev 1.2
Tuesday, May 18, 2021
Sheet 72 of 78

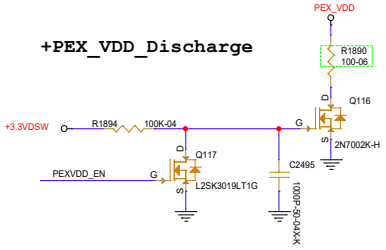
+1.8V/PEX_VDD

PEX_VDD

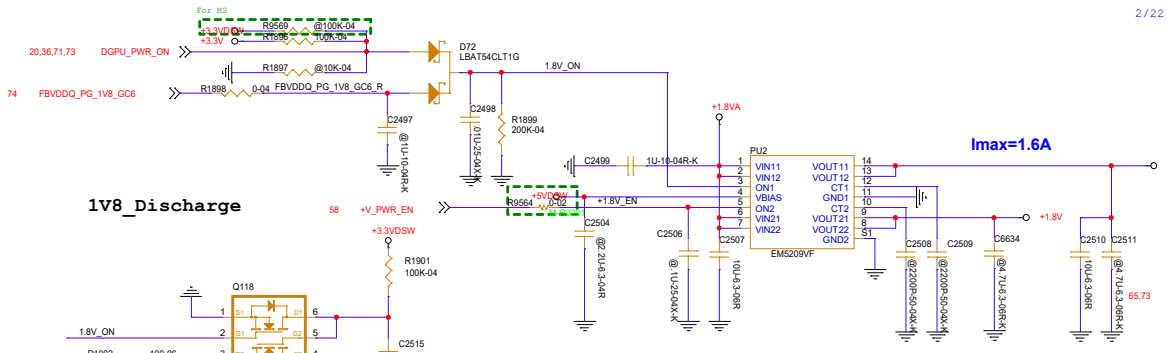


TYPE	PEX_VDD	R1	R2
GB5B-128(G20-Px)	0.9582V	24K-1-04	40.2K-1-04
GB5-128(G61-A)	1.003	27K-1-04	40.2K-1-04

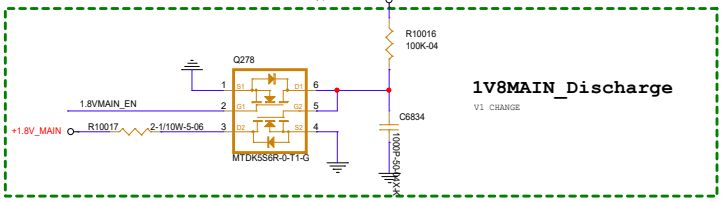
+PEX_VDD_Discharge

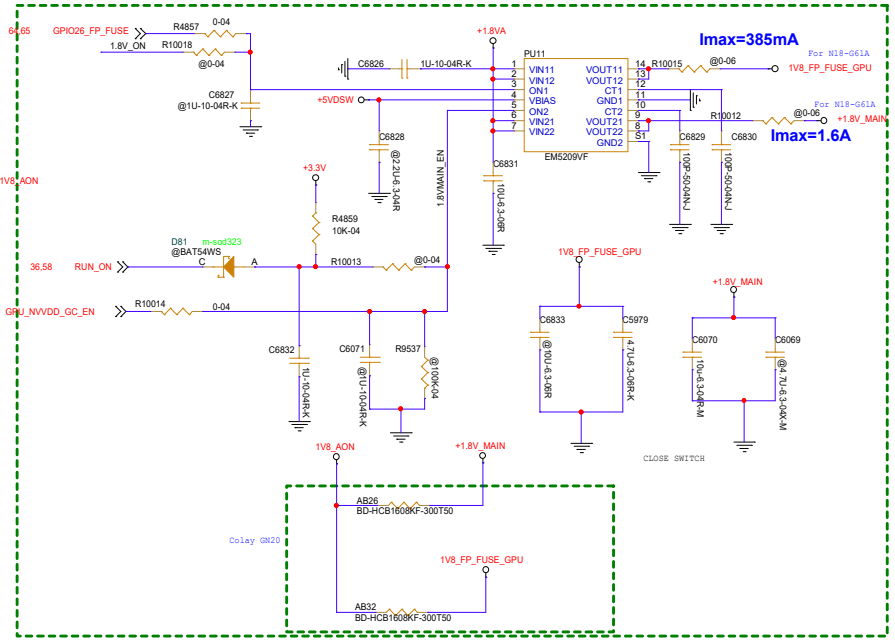


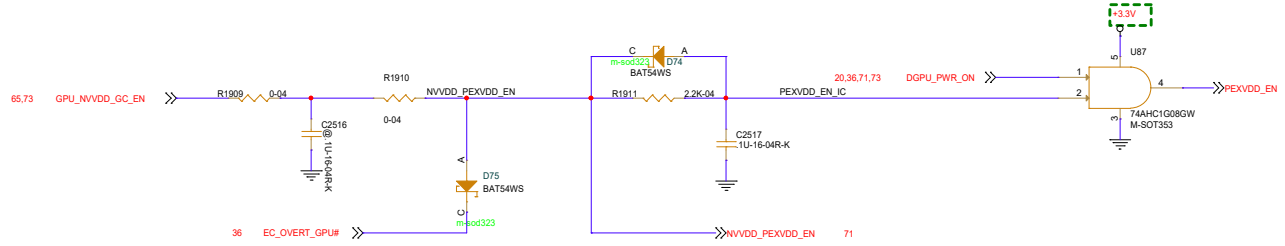
1V8_Discharge

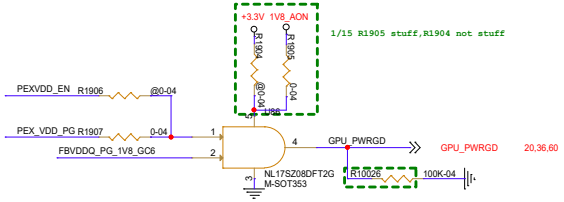


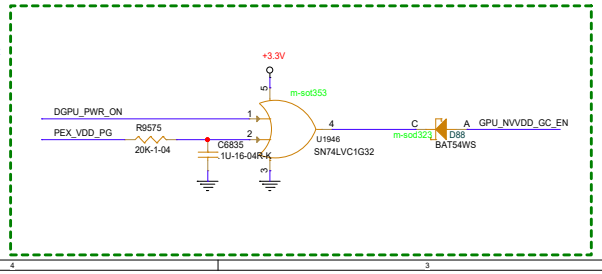
1V8MAIN_Discharge

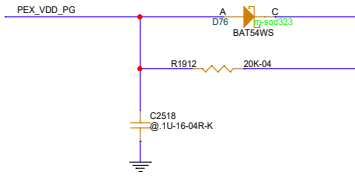






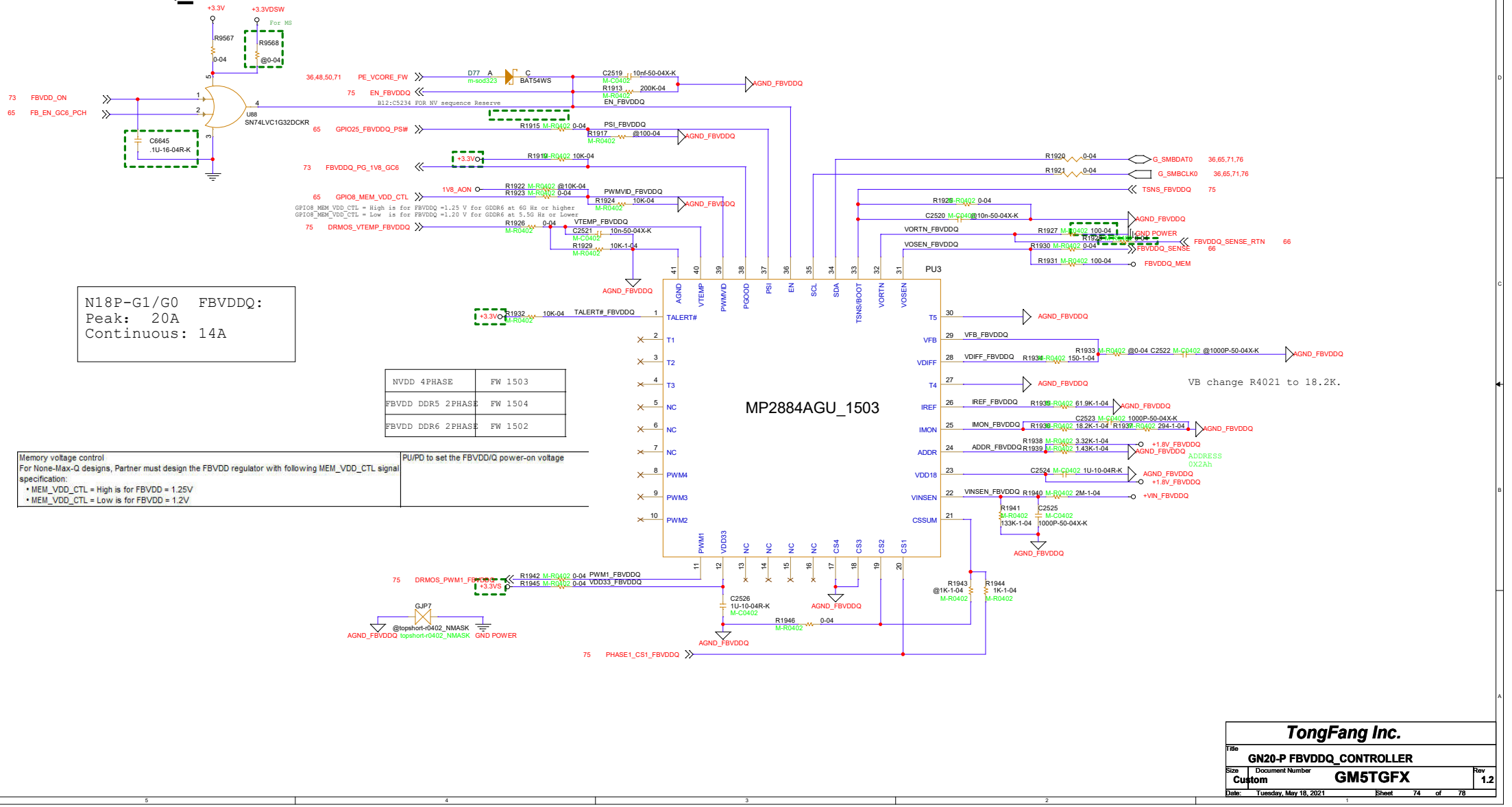






TongFang Inc.			
Title: GN20-P +1.8V_AON/PEX_VDD			
Size: C	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 73 of 78		

FBVDDQ_MEM



N18P-G1/G0 FBVDDQ:
Peak: 20A
Continuous: 14A

NVDD 4PHASE	FW 1503
FBVDD DDR5 2PHASE	FW 1504
FBVDD DDR6 2PHASE	FW 1502

Memory voltage control For None-Max-Q designs, Partner must design the FBVDD regulator with following MEM_VDD_CTL signal specification: • MEM_VDD_CTL = High is for FBVDD = 1.25V • MEM_VDD_CTL = Low is for FBVDD = 1.2V	PU/PD to set the FBVDD/Q power-on voltage

VB change R4021 to 18.2K.

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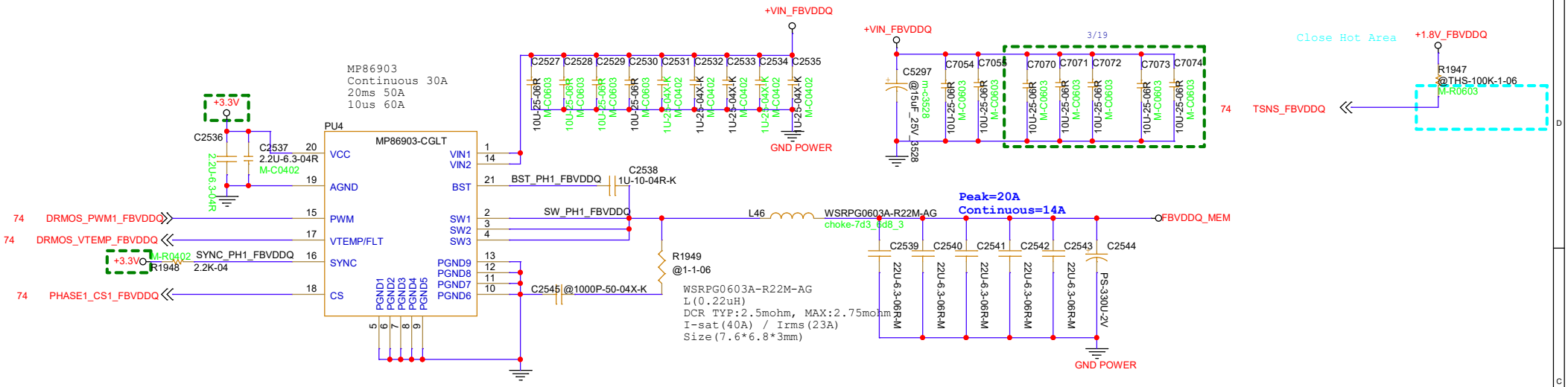
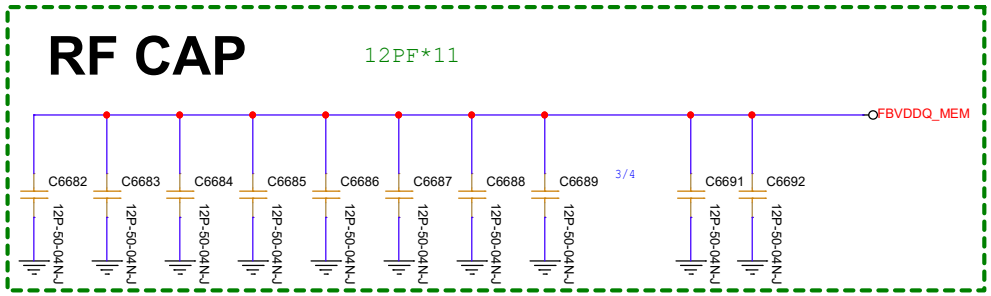
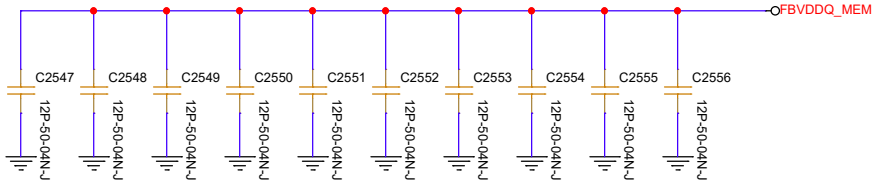
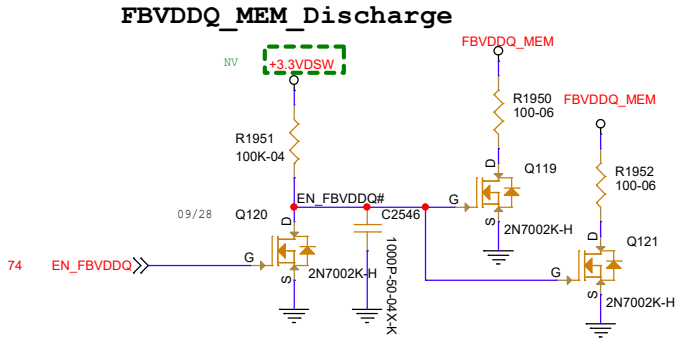
Title: GN20-P FBVDDQ_CONTROLLER		
Size: Custom	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 74 of 78	

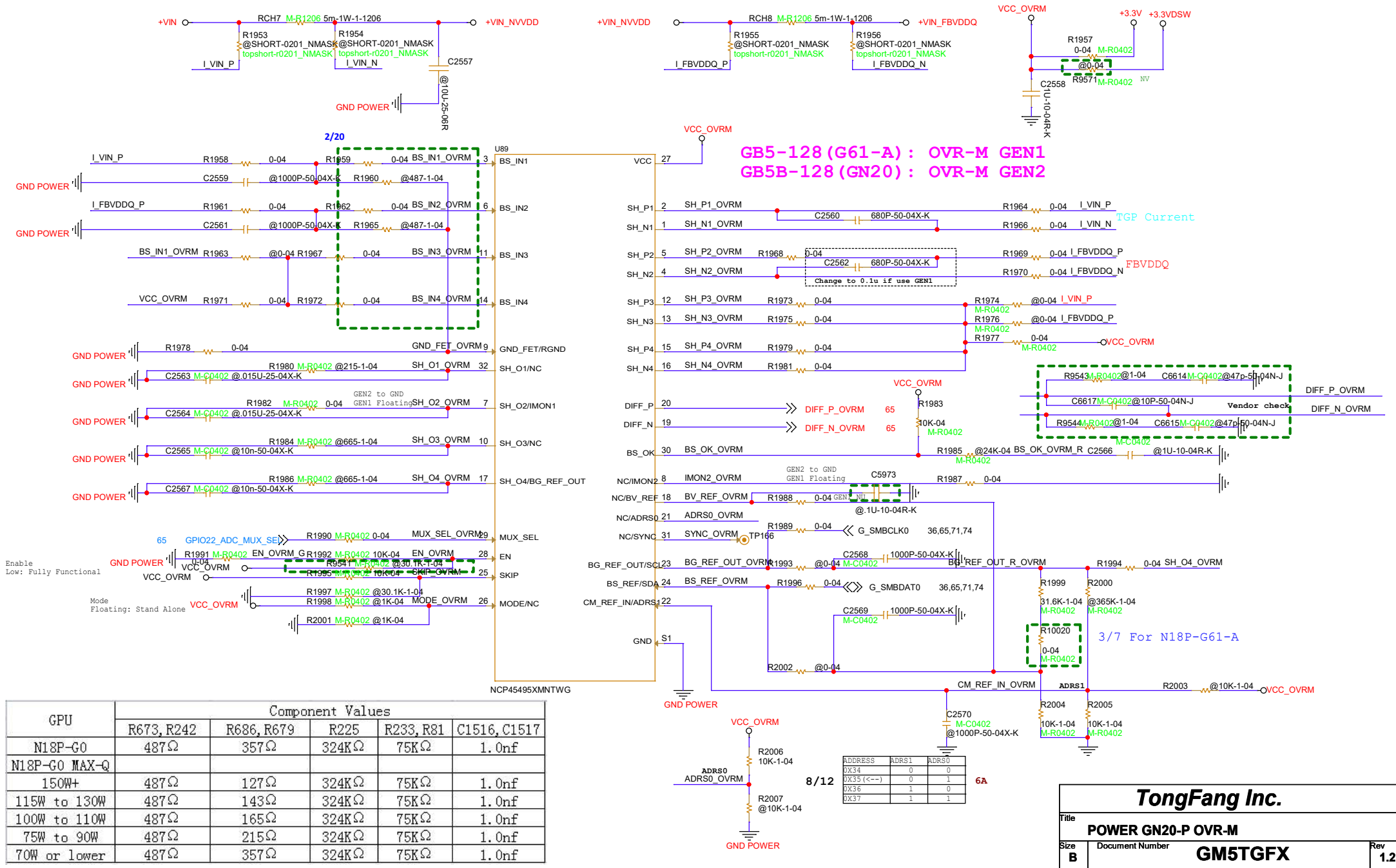








TongFang Inc.			
Title: GN20-P _FBVDDQ_1PHASE			
Size: B	Document Number: GM5TGFX		Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 75 of 78		



GPU	Component Values				
	R673, R242	R686, R679	R225	R233, R81	C1516, C1517
N18P-G0	487Ω	357Ω	324KΩ	75KΩ	1.0nf
N18P-G0 MAX-Q					
150W+	487Ω	127Ω	324KΩ	75KΩ	1.0nf
115W to 130W	487Ω	143Ω	324KΩ	75KΩ	1.0nf
100W to 110W	487Ω	165Ω	324KΩ	75KΩ	1.0nf
75W to 90W	487Ω	215Ω	324KΩ	75KΩ	1.0nf
70W or lower	487Ω	357Ω	324KΩ	75KΩ	1.0nf

ADDRESS	ADRS1	ADRS0
0X34	0	0
0X35 (<--)	0	1
0X36	1	0
0X37	1	1

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Title	POWER GN20-P OVR-M	
Size B	Document Number GM5TGFX	Rev 1.2
Date: Tuesday, May 18, 2021	Sheet 76 of 78	

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TongFang Inc.		
Title: Reserved		
Size: C	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 77 of 78	

A to A1 change list(2/2)

1. P40 Change Audio Codec from ALC897 to ALC256
2. P45 Add R9623 For SD D3 Cold
3. P71 Add U1908,R4058,C4558,D94 For NVVDD Sequence
4. P18 Add R9624,R9625,R9626 and Modify R119,R120,R121,R129 to Improve Power loss sequence
5. P18 Del R9563 for SYS_PWROK sequence
6. P55 Add R9627 for +3.3VDSW_PCH_PD reference voltage
7. P58 Add Q239,R9628,R9629,C6778 For +3.3VA discharge
8. P52 Add Q240,R1737,R1738,C6779 for +VCCIN_AUX_PCH discharge
9. P53 Add Q241,R9630,R9631,C6780 for +VNN_BYP discharge
10. P22 Change PCH AN39 pin net name to PCH_SPI0_CLK
11. P76 DEL R1960,R1965 GND and connect to U89pin9
12. P18 Add R9632 for PM_RSMRST#_R co-lay
13. P20 Add R10009 for GPU_PWRGD
14. P25 Add C6823,C6824,C6825 for +VCCPRIM_1P8
15. P58 R1099 not mount
16. P46 R9545 mount for ADAP_IN
17. P58 C976 mount for +3.3VS_SS
18. P58 Add R10010 for +V_PWR_EN
19. P19 R132 not mount for GPP_H13_PEG_RESET#
20. P43 R9550 not mount for +WLAN_3.3VA
21. P19 R148 not mount for GPP_H2_CLKREQ8_LAN_N
22. P19 R1583 not mount and P36 add R10011 for GPP_E3_EC_SMI#
23. P73. Add PU11and Q278 sch for N18P-G61A
24. P73 Reserve U1946 for NV Sequence
25. P30 Change NB691GG-Z to MP1613GTL-Z for +3.6V_LCD
26. P54 Change R1036 from 220K to 560K for 5VDSW not output on Bat mode(9V)
27. P25 Change C230,C231,C232,C233 from 22uf to 10uf
28. P66,70 Change C6680,C6681 from EEFSX0D331EY to EEFST0D331R
29. P73 Change EM5209 from XP5209 to EM5209VF

A1 to A2 change list(3/4)

1. P58 +3.3VA discharge sch not mount
2. P75 Del C6690 for thermal bracket short issue
3. P51 Co-lay C6836,C6837,C6838,C6839 for +VIN_+VCCIN_AUX_CPU
4. P49 Co-lay C6840~C6849 for +VIN_VCCIN
5. P18,P58 Reserve C7051,C7052,C7053 for sequence
6. P56 R1069,R1071,C929 not mount,change R1070 to 90.9K for +1.8VA
7. P73 Change C2494 from 10nf to 1nf for GC6 issue

A2 to B change list(3/7)

1. P19 Change R149 pull high from +3.3VA to +3.3V, U5 pull high from +1.8VA to +1.8V for leakage issue
2. P18 Change R122 pull high from +3.3VA to +3.3VS
3. P76 Add R10020 for N18P_G61-A
4. P53~P57 change open to short for 12 Jumpers
5. P75 Add C7054,C7055 for +VIN_FBVDDQ co-lay
6. P72 Add C7056~C7063 for +VIN_NVVDD
7. P56 Change R1068 from 200K to 100K for +1.8VA
8. P55 Add C7064,C7065 for VIN_+3.3VDSW co-lay
9. P56 Add C7066,C7067 for VIN_+1.8VA co-lay
10. P52 Add C7068,C7069 for +VIN_VCCIN_AUX_PCH
11. P73 Change C2494 from 10nf to 1nf for GC6 issue
12. P42 Del TVS23,TVS52~TVS58 for cost down
13. P32 Del TVS44~TVS51 for costdown
14. P58 Add D95 for +VS_PWR_EN (FBMEM FW can't read issue)
15. P75 Add C7070~C7074 for +VIN_FBVDDQ
16. P71 R1869 not mount, Change R1870 from 2K to 0 ohm for NVVDD FW issue

B to NPI change list(3/29)

1. P30 Change PS1 from Poly-switch to fuse for LCD flicker issue
2. P36 FAN_BOOST_WLAN_LED_EC# short to QKEY0# for CapsLock LED issue
3. P18 Add R10021 for PM_SLP_SUS# pull down
4. P36 Add R10022,R10023 for PM_SLP_S4#/S0# pull down
5. P27 Add C7075,C7076,C7077 for +3.3VDSW_PCH Power rail
6. P60 R1707 mount, R1708 not mount for GC6 issue
7. P71 Change C2387 to R1843 end point for NV sequence
8. P67 DEL R1828,R1830,Q107 for VRAM1
9. P68 Add R10024 for VRAM2
10 P69 DEL R1835,R1837,Q108 for VRAM3
11. P70 Add R10025 for VRAM4
12. P65 Change R1914 from FBMEM VR side to GPU side
13. P73 Add R10026 for GPU_PWRGD step issue
14. P43 Add C7078 for WLAN Power improve
15. P30 Change R359 from 10 ohm to 24.9 ohm for LCD sequence
16. P43 Q95 not mount for cost down
17. P55 Q56,Q57 not mount for cost down
18. P32 Change R430~R437 from 0 ohm to 10 ohm for HDMI Signal issue
19. P73 U1946,D88,C6835 mount, R9575,R1912 mount 20K,C2518 not mount for GPU sequence
20. P71 Change R1843 from 10K to 3K for GPU sequence
21. P74 C6645 mount 0.1uf for GPU sequence

V1.0 to V1.1 change list(4/28)

1. P19 Add R9870 for PMCALERT(PMC initial issue)
2. P57,P58 DEL R1088,R1095,R1112 for cost down
3. R560 need mount for Capslock LED issue

V1.1 to V1.2 change list(5/15)

1. P19 Add Q280,R10028,R10029 for C10_GATEB co-lay
2. P57 Add R674,C7085,Q279,R271,Q17,R10027 for DDR_VTT_CNTL co-lay
3. P57 Add C7081,C7080,C7079 &change U42 foot print to dfn8-1_0p65_3x3_1p0 for NCP59800-D co-lay
4. P57 Add U1958,C7086,C7088,R10032,R10030,R10031,R10033,C7087 for EM5109AVT-00A co-lay

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Title: History		
Size: B	Document Number: GM5TGFX	Rev: 1.2
Date: Tuesday, May 18, 2021	Sheet 78 of 78	