Compal Confidential

Model Name : Dopey_KL/Sleepy_KL/Taurus_KL

Compal Project Name : EH7L1/EH5L1/FH5T1

File Name : LA-H781P

Compal Confidential

EH7L1/EH5L1 MB Schematic Document

LA-H781P

Rev: 1.B

2019.05.13

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2019/12/11

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: EH7L1 LA-H781P	Rev: 1B
Date: Tuesday, May 14, 2019	Sheet 1 of 58	

HDMI Conn.

page 29

DDI1
HDMI x 4 lanes

eDP

page 28

eDP

DDI

Intel Kabylake U

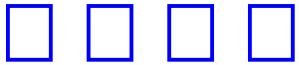
Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)
(KBL-U_23E Fuse Down)
Processor

Dual Core + GT2
Quad Core + GT2

Memory BUS
Dual Channel
1.2V DDR4 2133/2400

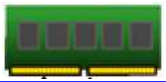
Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16



page 19

260pin DDR4-SO-DIMM X1



page 20

Nvidia N16S-GTR /
N17S-G0/G2
with GDDR5 x2
page 21~27

page 31

(Reserved PCIE 3.0 x4)
(Port 9-12, 8GT/s)

PCIe 3.0 x 4
8GT/s
port 1-4

SATA3.0
6.0 Gb/s
port 12
(SATA2)

Flexible IO
Base-U PCIE2.0
Premium-U PCIE3.0

USB 3.0
conn x1
USB3 port 1
USB2 port 1

page 36

USB 2.0
conn x2
USB2 port2
USB2 Port3 on SUB/B

page 36

CMOS
Camera
USB2 port 7

page 28

USBx8 48MHz

HD Audio 3.3V 24MHz

NGFF
WLAN
USB2 port 5

PCIe 1.0
2.5GT/s
port 6
page 31

PCIe 1.0
2.5GT/s
port 5

LAN(GbE)
Realtek 8111H
page 30

RJ45 conn.

SATA3.0
6.0 Gb/s
port 7
(SATA0)

SATA HDD
Conn.

page 33

SATA3.0
6.0 Gb/s
port 8
(SATA1)

SATA CDROM
Conn.

page 33

15W
1356pin BGA
page 07~18

SPI

SPI ROM
64Mb page 9

HDA Codec
ALC255 page 32

Touch
Screen

USB2 port 6
page 28

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022
page 37

Int. Speaker
page 32

Int. DMIC
on Camera
page 28

UAJ
page 36

Fan Control
page 39

Sub Board

LS-H781P IO/B
page 35

LS-H782P HDD/B
page 33

LSH783P HS/B
page 38

LSH784P ODD/B
page 33

RTC CKT.
page 15

Power On/Off CKT.
page 38

DC/DC Interface CKT.
page 40

Power Circuit DC/DC
page 41~54

Int.KBD

page 38

Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

page 38

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
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Date: Monday, May 13, 2019 Sheet 2 of 58

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1(EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	0.2(EVT2)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	1.0(DVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.A(PVT)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	1.B(MP)
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
Acer BYOC	BYOC@ / NBYOC@
CODEC(ALC255/256)	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
CPU Selection	U42@/U22@
ODD Support	ODD@
G Sensor	BA@
TPM	TPM@ / NTPM@
Finger Print	FP@/FPEMC@
UMA or DGPU	UMA@/VGA@
DGPU Serial Select	N17S@
Intel Modern Standby	MSB@/NMSB@
N17SG1	N16SGTR@ / N17SG1@
MB Stage	EVT@/DVT@/PVT@/MP@
Memory Select	X76H4G@/X76M4G@/ X76S4G@
Memory Mode	SDP@ / DDP@
VRAM BOM Select	X76N17H2G@ X76N17M2G@ X76N17S2G@
BOM Select	X76@
15" 17" LID	15@/15DIS@

43 level BOM table

43 Level	Description	BOM Structure
431AHUBOL55	SMT MB AH781 EH5L1 I370U23E 130 HDMI	U22@/CMC@/LPC@/RD@/NBYOC@/255@/MP@/MEM@/NMSB@/NTPM@/DAZ1B@/X76M@/N16X4E@/DIS@/VGA@/N16X@/MX130@/N16X76VRAMMP@/SR3N6@/15DIS@/15@/EH5L1@
431AHUBOL57	SMT MB AH781 EH5L1 I370U22 130 HDMI	U22@/CMC@/LPC@/RD@/NBYOC@/255@/MP@/MEM@/NMSB@/NTPM@/DAZ1B@/X76M@/N16X4E@/DIS@/VGA@/N16X@/MX130@/N16X76VRAMMP@/SR3TK@/15DIS@/15@/EH5L1@
431AHUBOL07	SMT MB AH781 EH7L1 I37020U22 130 HDMI	U22@/CMC@/LPC@/RD@/NBYOC@/255@/MP@/MEM@/NMSB@/ODD@/NTPM@/DAZ1B@/X76M@/N16X4E@/DIS@/VGA@/N16X@/MX130@/N16X76VRAMMP@/SR3TK@/EH7L1@
431AHUBOL13	SMT MB AH781 EH7L1 I370U23E 130 HDMI	U22@/CMC@/LPC@/RD@/NBYOC@/255@/MP@/MEM@/NMSB@/ODD@/NTPM@/DAZ1B@/X76M@/N16X4E@/DIS@/VGA@/N16X@/MX130@/N16X76VRAMMP@/SR3N6@/EH7L1@

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VSDGPU	+1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON*2	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

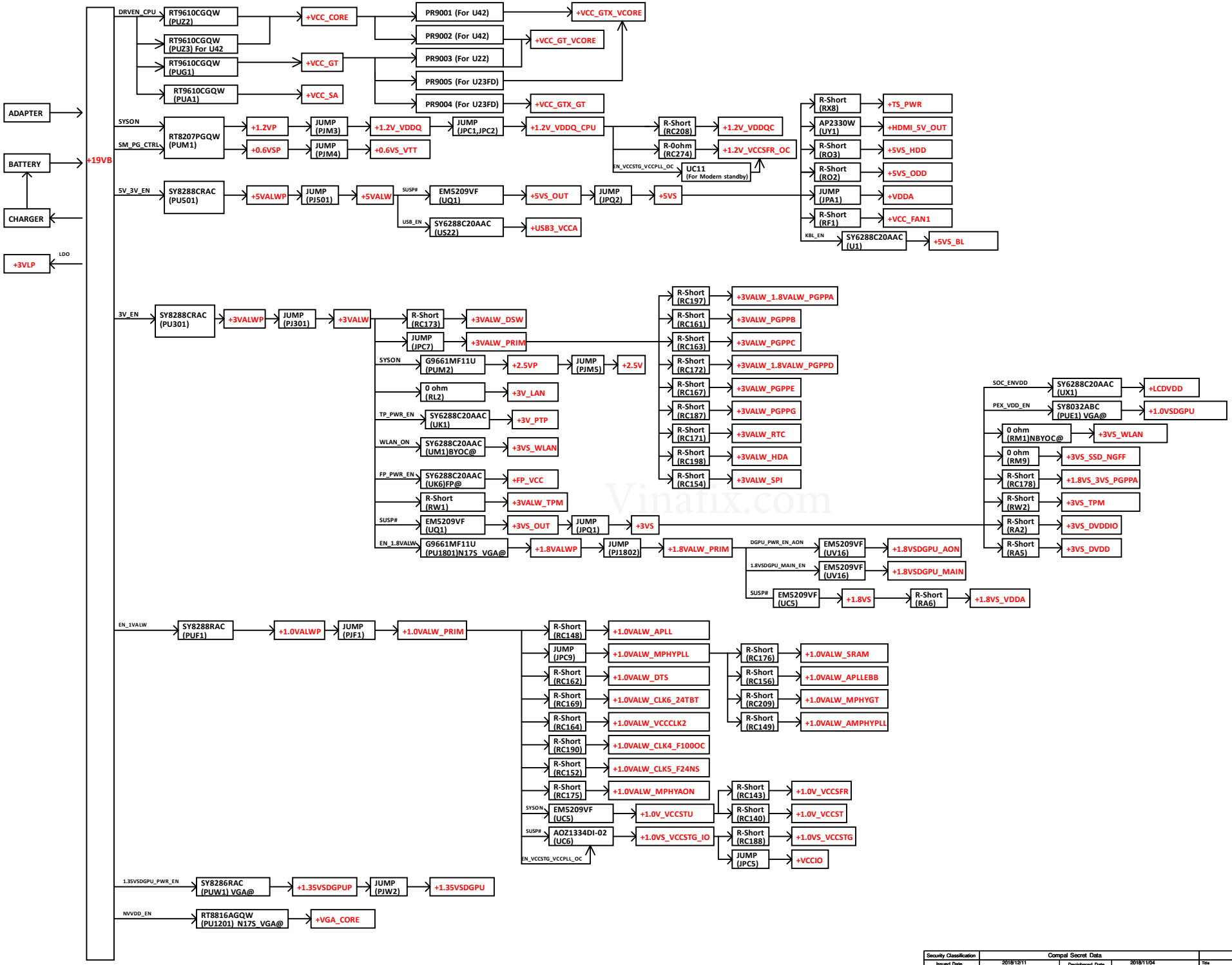
Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

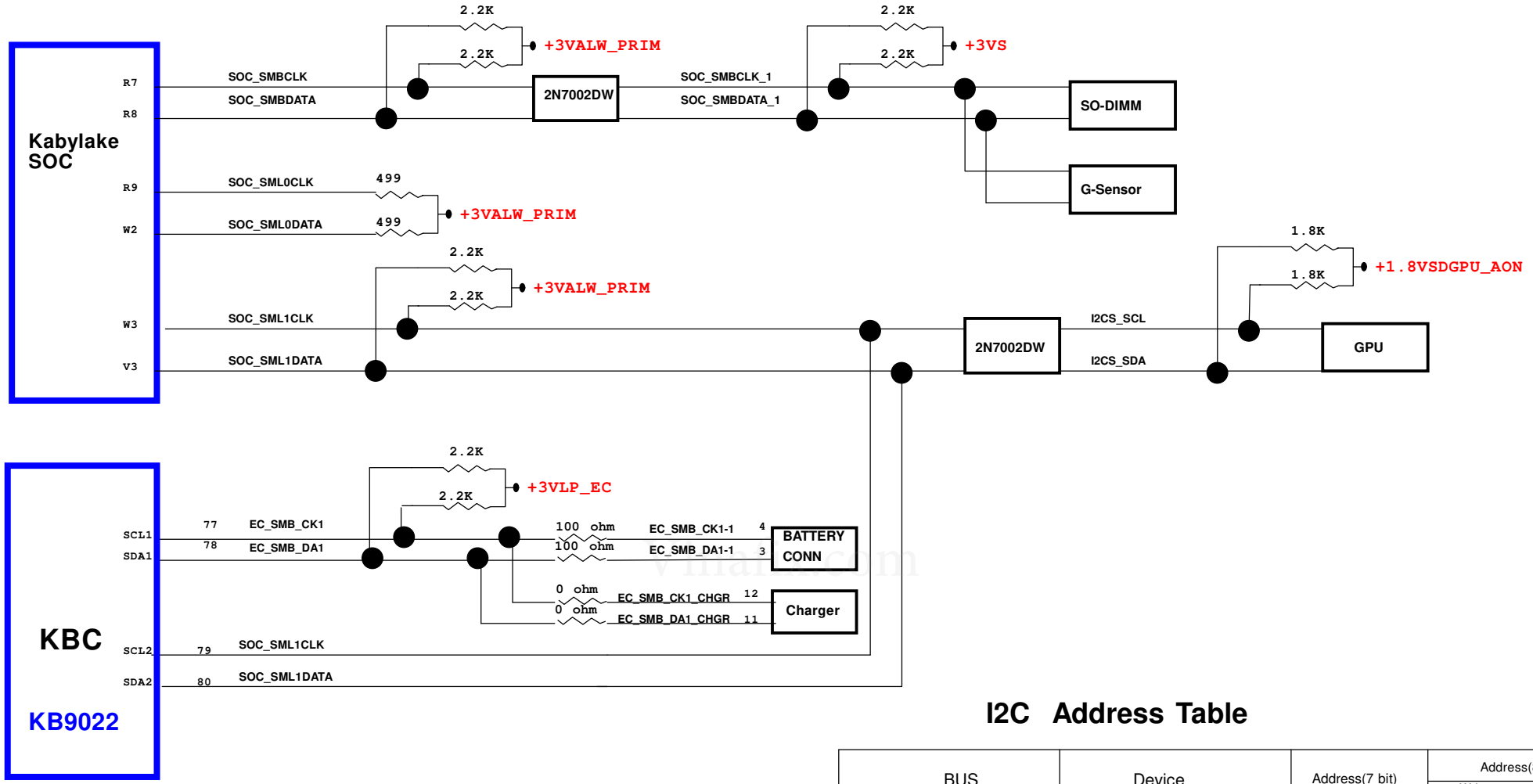
Title: Notes List

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

Date: Monday, May 13, 2019 | Sheet 3 of 58



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/11	Deciphered Date	2018/11/04
Title	Power Rail		
Size	Document Number		Rev
Custom	EH7LI LA-H781P		1S
Date: Monday, May 13, 2019	Sheet 4 of 58		



I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved			
I2C_1 (+3VALW_PGPPC_E)	TM-P3393-003 (TP)	0x2C		
	FA577E-1206 (TP-ELAN)	0x15		
	SA577C-12A0 (TP-ELAN)	0x15		
SOC_SMBCLK (+3VS)	SO-DIMM	0xA4		
	G-Sensor	0x30		
SOC_SML1CLK (+3VALW_PRIM)	VGA	0x9E		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24781RUYR (Charger IC)	0x12		
	BATTERY PACK	0x16		

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SMBUS Routing Table

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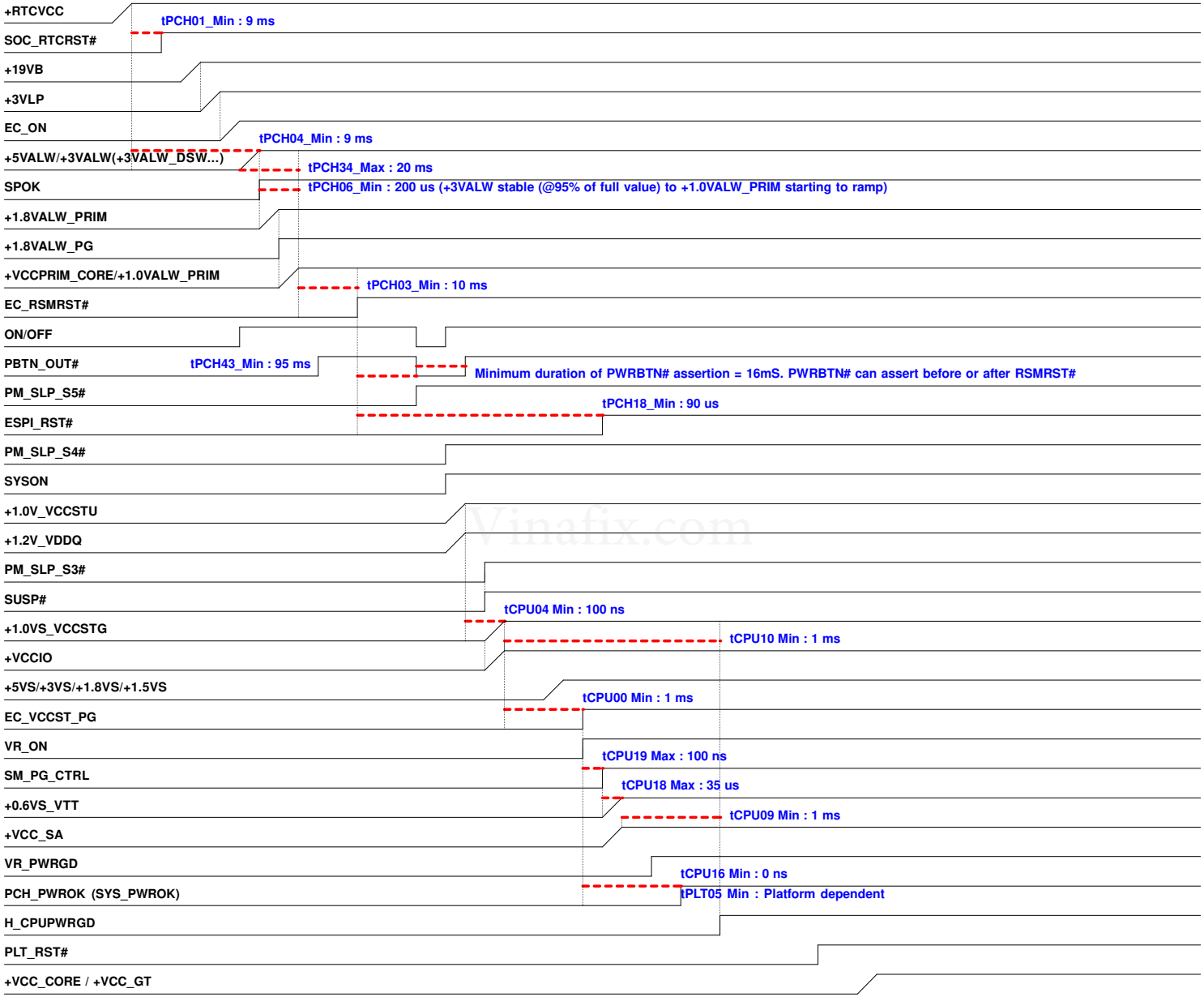
PWR Sequence_KBL-U22/U42



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.		
Title: Power Sequence		
Size: Custom	Document Number: EH7L1 LA-H781P	Rev: 1B
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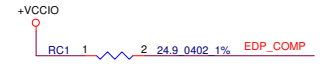
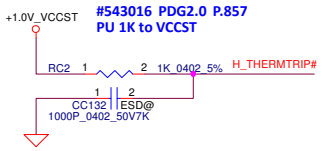
Functional Strap Definitions

#543016 PDG2.0 P.844

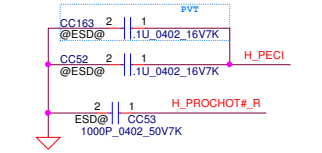
DDPB_CTRLDATA
DDPC_CTRLDATA
Display Port B/C Detected
NC =Port is not detected.
PU =Port is detected.

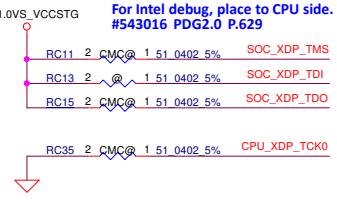


#543016 PDG2.0 P.225
COMPENSATION PU for eDP
Trace width=5 mils,Spacing=25mil,Max length=600mils

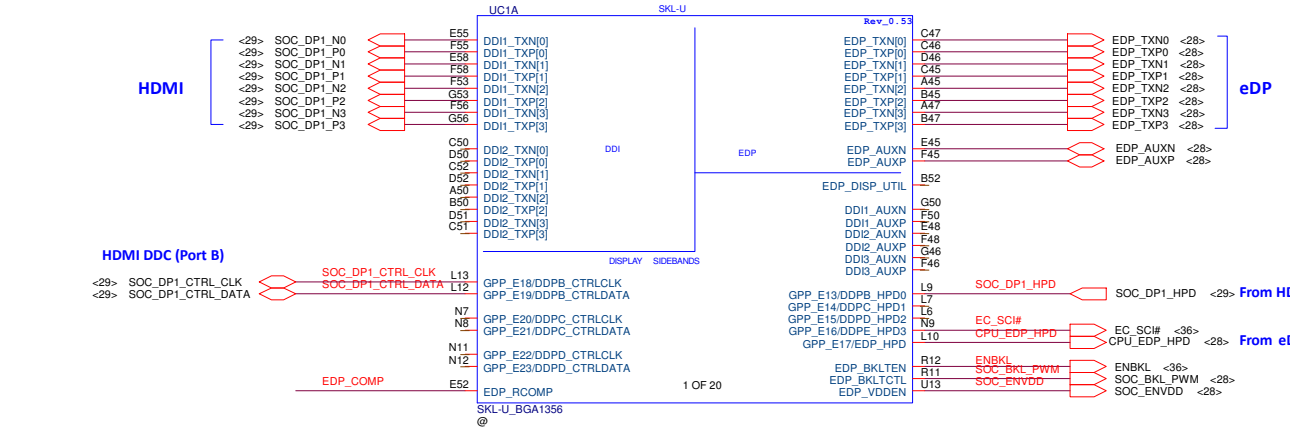


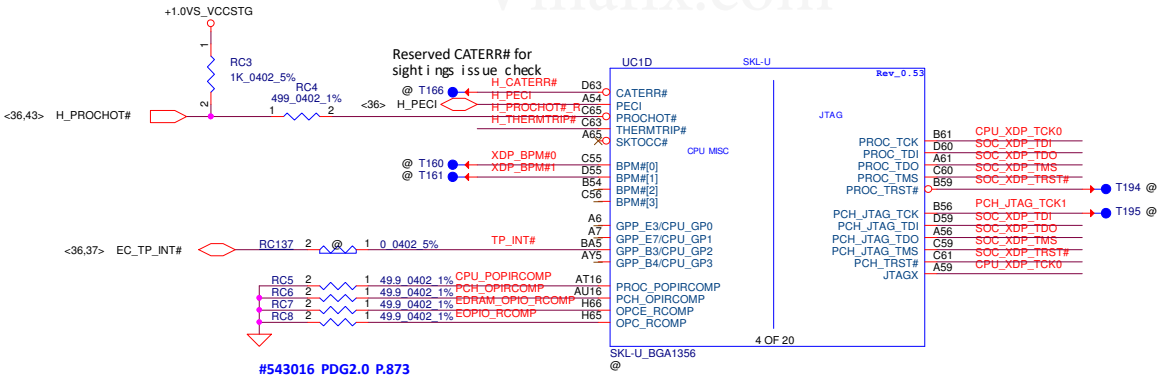
#543016 PDG2.0 P.857
PU 1K to VCCST





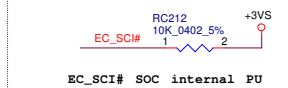
For Intel debug, place to CPU side.
#543016 PDG2.0 P.629



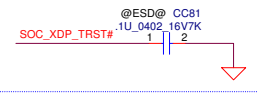


#543016 PDG2.0 P.873
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB1.1 P.52
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD 50ohm



#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- **GPP_B14 GPP_B20 GPP_B23**
- **GPP_C[23: 22**
- **GPP_D[4: 0**
- **GPP_E[8: 0], GPP_E[16: 13**



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **KBL-U(1/12)DDI,MSIC,XDP,EDP**

Size: Custom | Document Number: **EH7L1 LA-H781P** | Rev: 1B

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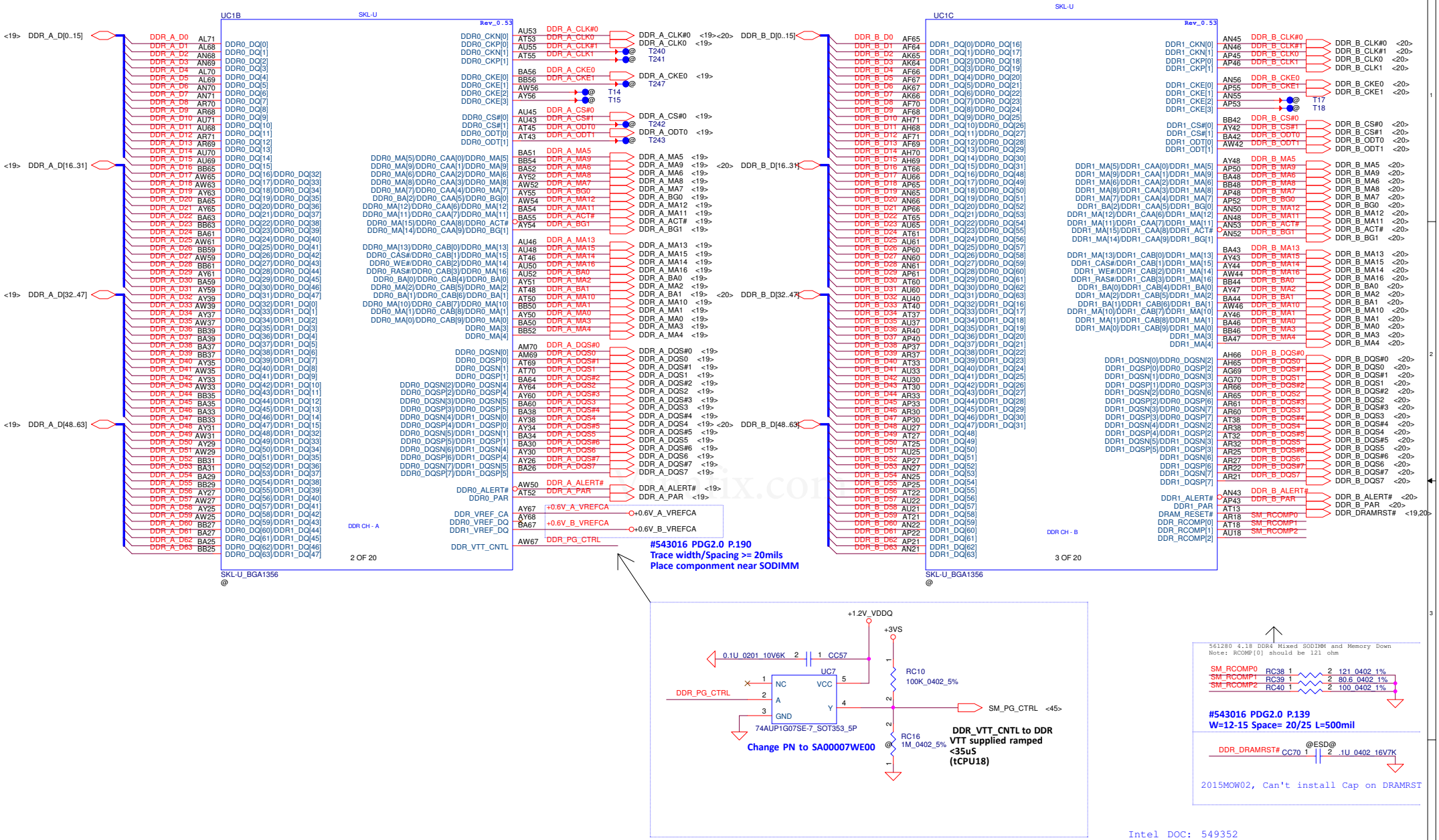
Interleaved Memory



#543016 PDG2.0 P.190
Trace width/Spacing >= 20mils
Place component near SODIMM

Intel DOC: 549352

3. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: KBL-U(2/12)DDR4

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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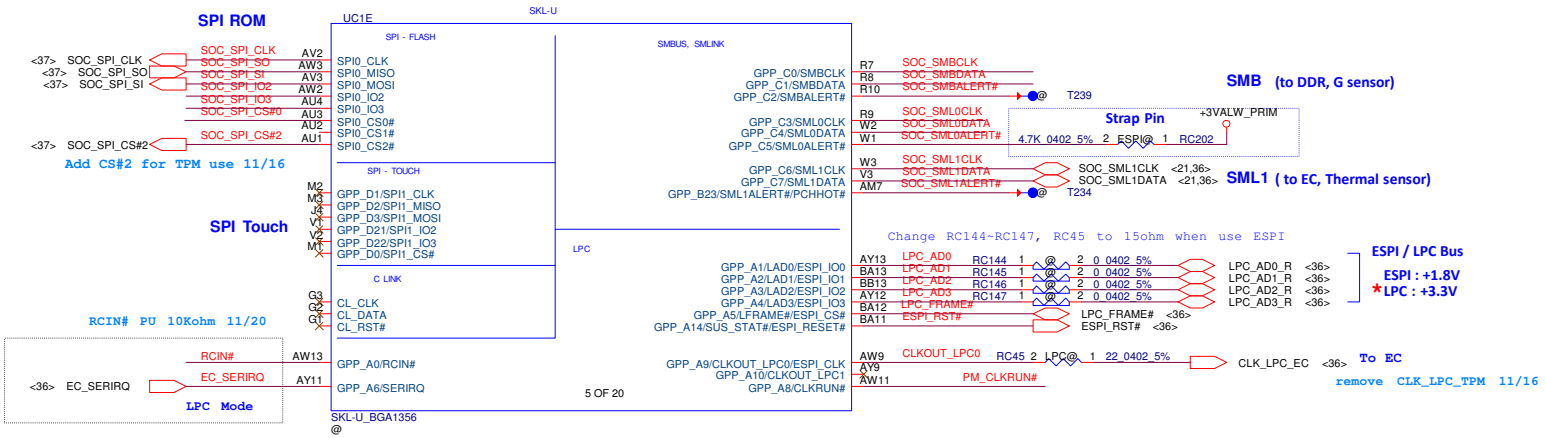

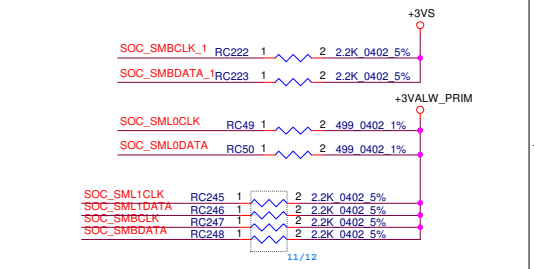

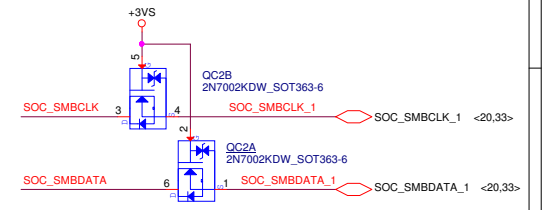

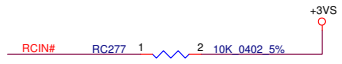

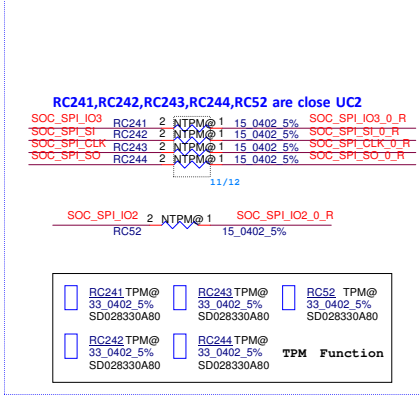

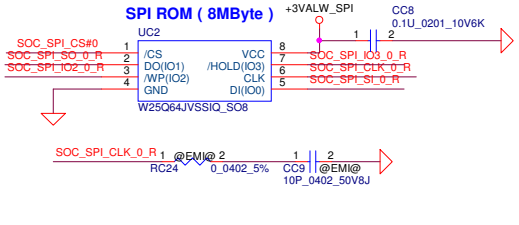

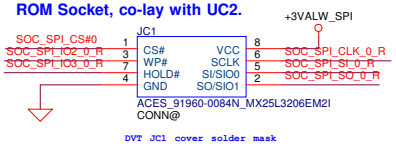

* SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

* SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto (TLS) (with confidentiality).
Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: KBL-U(3/12)SPI,ESPI,SMB,LPC

Size	Document Number	Rev
Custom	EH7L1 LA-H781P	1B

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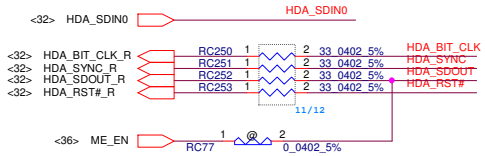
HDA for AUDIO



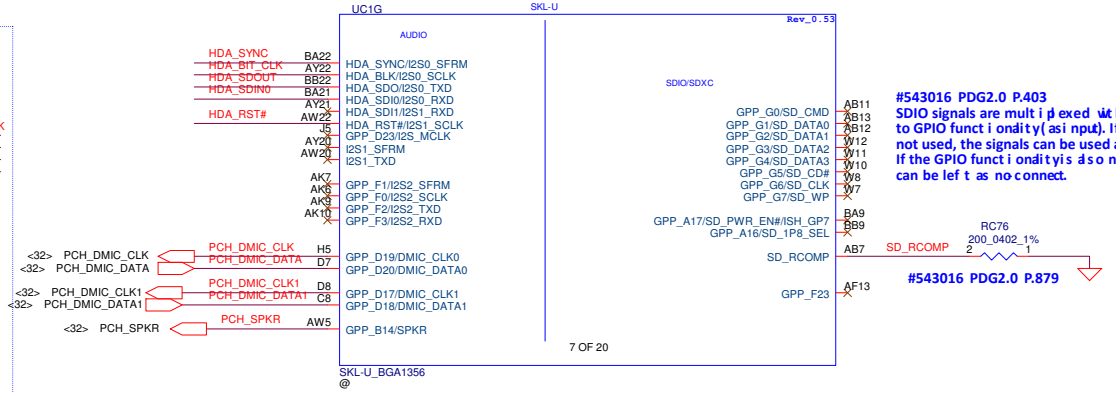
HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override For 4Mic 11/29
0 = Enable security measures defi nedi nt he fl ash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

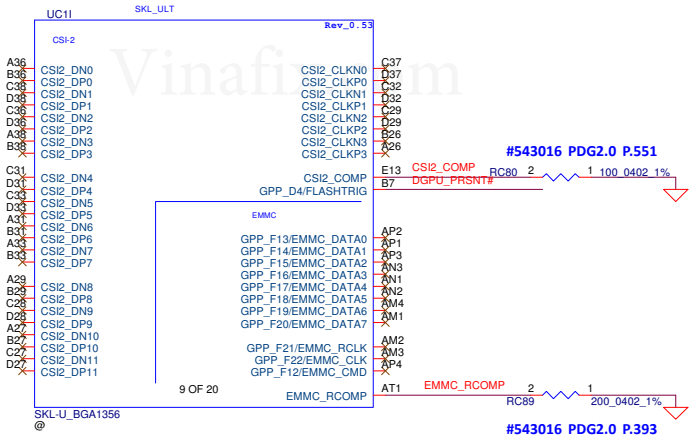
TOP Swap Override
*** 0 = Disable TOP Swap mode.**
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilit i es
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



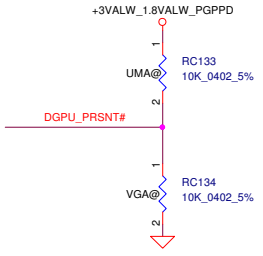
#543016 PDG2.0 P.403
SDIO signals are multi pl exed wi th GPIOs and default to GPIO functi onality(asi nput). If SDI Cl nterfaceis not used, the signals can be used as GPIOs instead. If the GPIO functi onality is also not used, these signals can be left as no connect.

#543016 PDG2.0 P.879



#543016 PDG2.0 P.551

#543016 PDG2.0 P.393



	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	KBL-U(4/12)HDA,EMMC,SDIO,CSI2
Size: Custom	Document Number: EH7L1 LA-H781P
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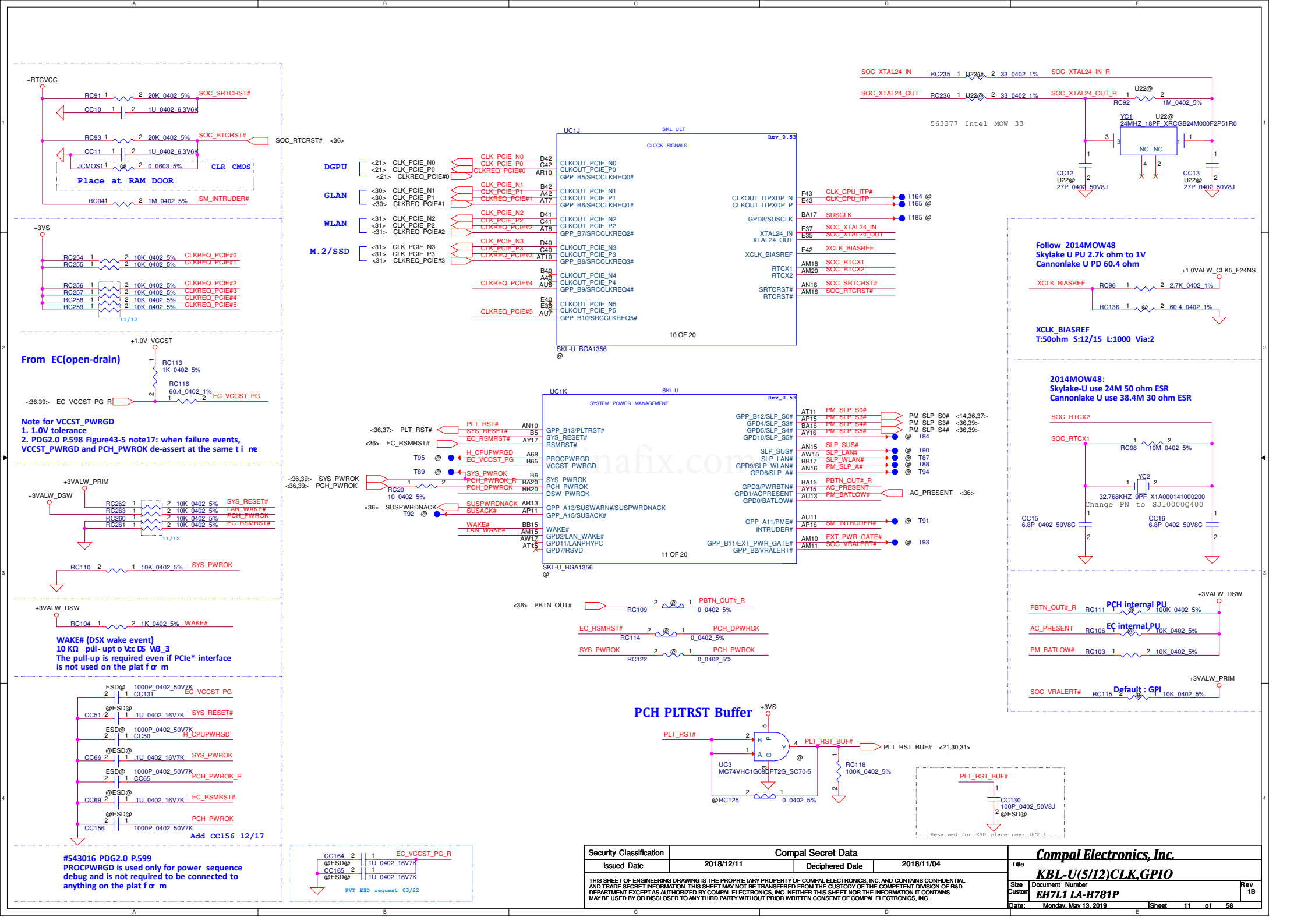
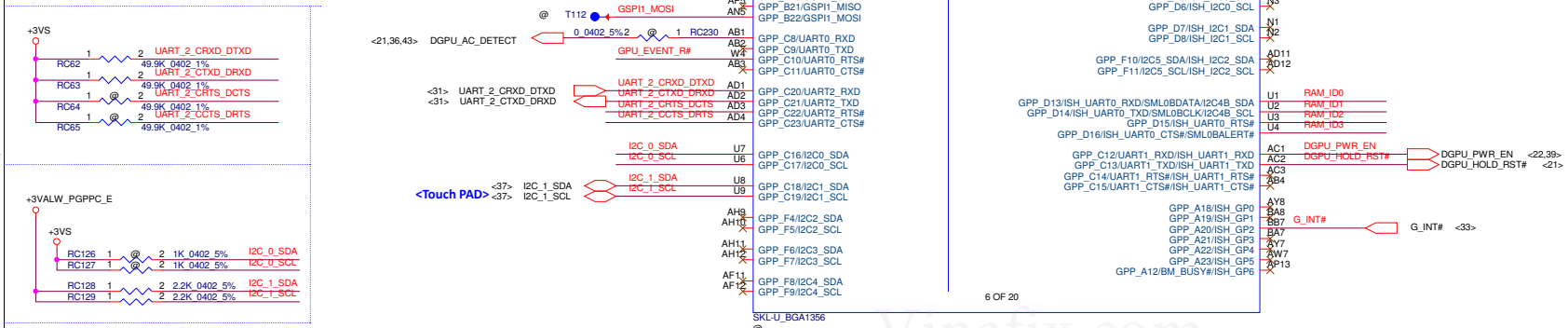
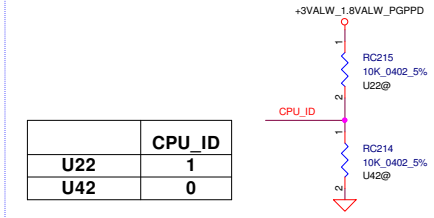
Date: Monday, May 13, 2019	Sheet 10 of 58



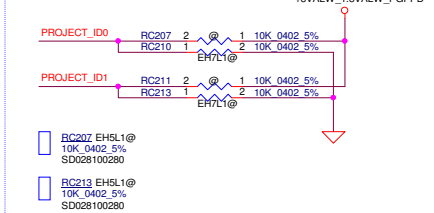
Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	KBL-U(5/12)CLK,GPIO
Size: Custom	Document Number: EH7L1 LA-H781P
Rev	1B
Date: Monday, May 13, 2019	Sheet 11 of 58

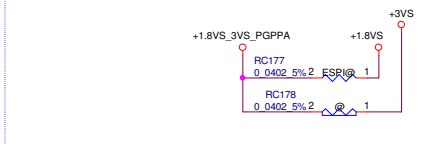




	CPU_ID
U22	1
U42	0



Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
EH7L1	0	0
EH5L1 (FH5T1)	0	1
	1	0
	1	1



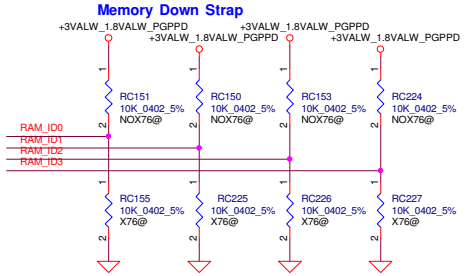
Functional Strap Definitions

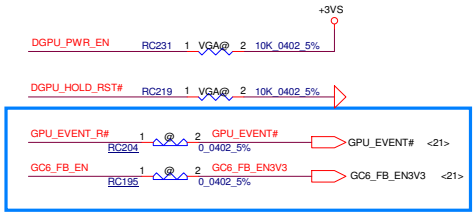
GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

***0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
***0 = SPI Mode --> AAX05 Use**
1 = LPC Mode





	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABO!)
Micron 4GB	0	0	0	1	SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABO!)
Samsung 4GB	0	0	1	0	SA0000B6F30 (S IC D4 512M16 K4A8G165WC-BCTD FBGA ABO!)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: KBL-U(6/12)GPIO

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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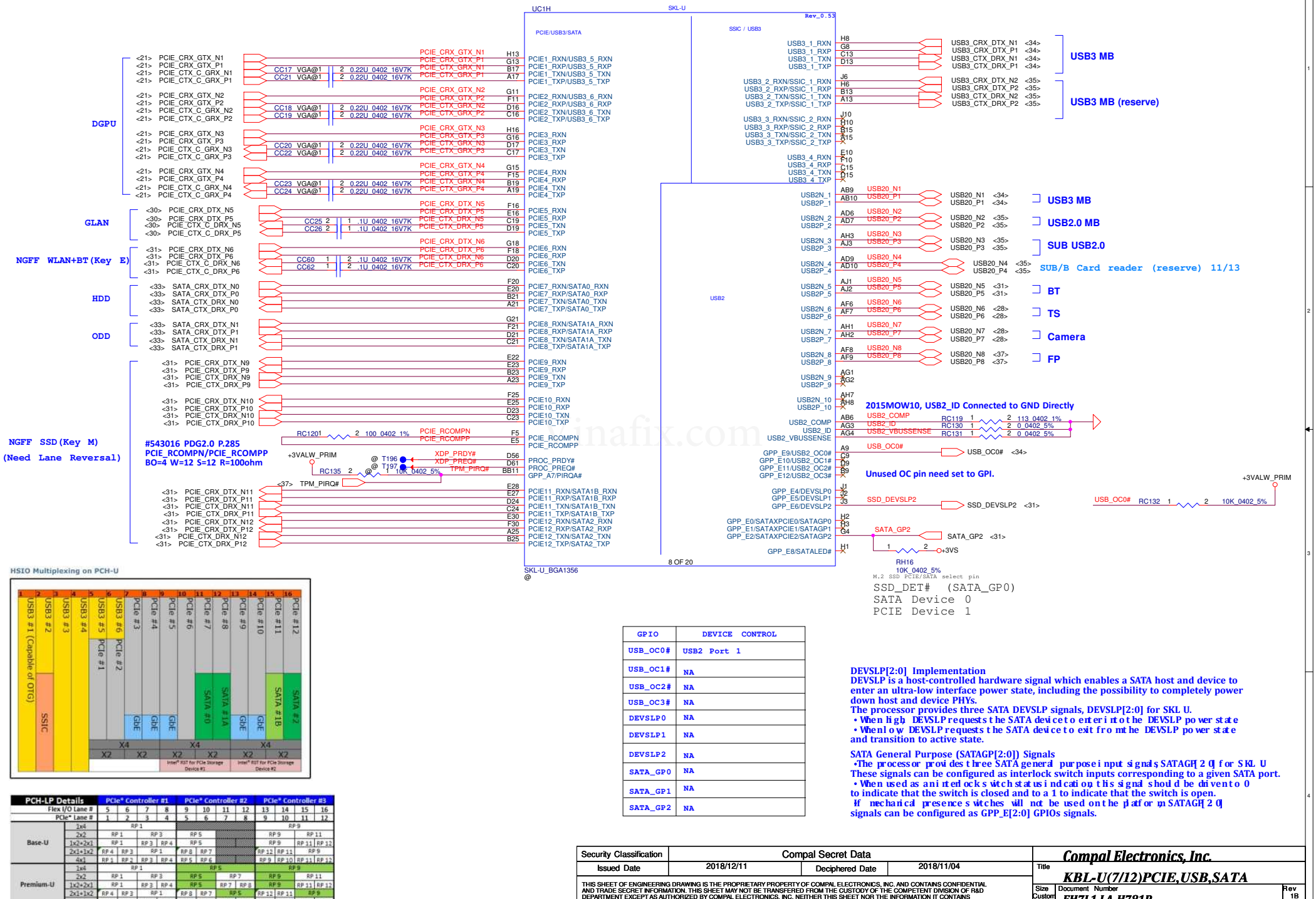

HSIO Multiplexing on PCH-U

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7			RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

- When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL U

These signals can be configured as interlock switch inputs corresponding to a given SATA port.

- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.

If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: KBL-U(7/12)PCIE,USB,SATA

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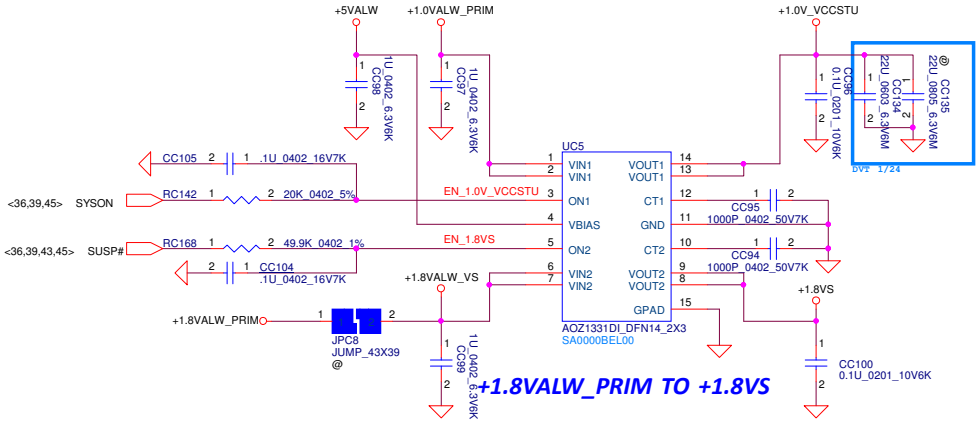
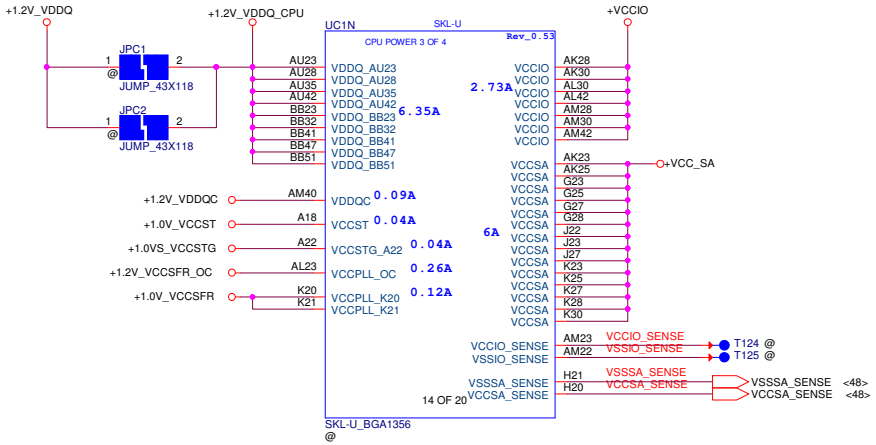
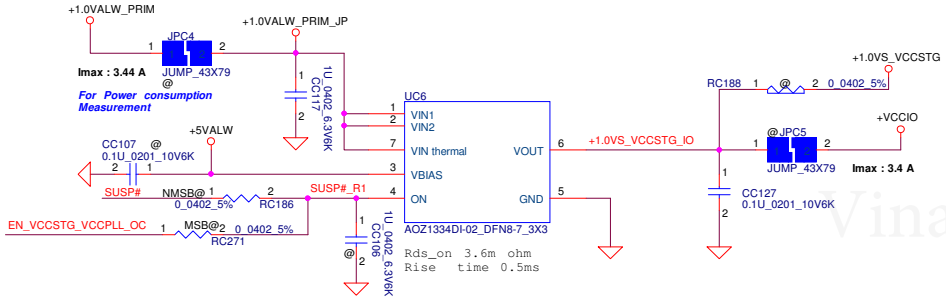
Date: Monday, May 13, 2019 | Sheet 13 of 58

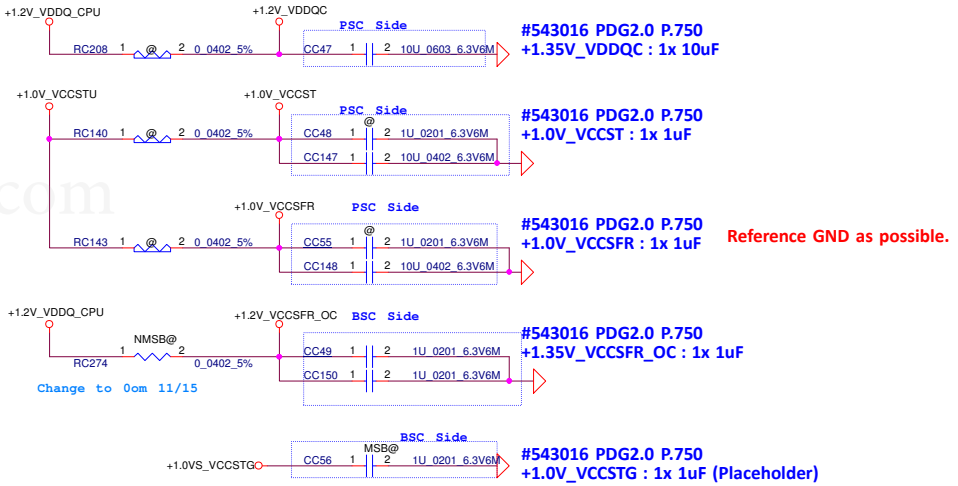
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

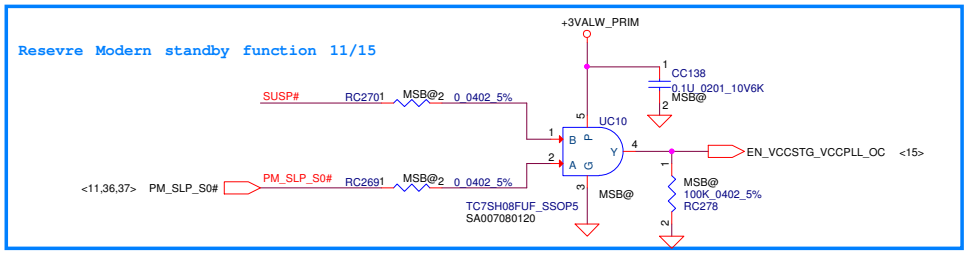


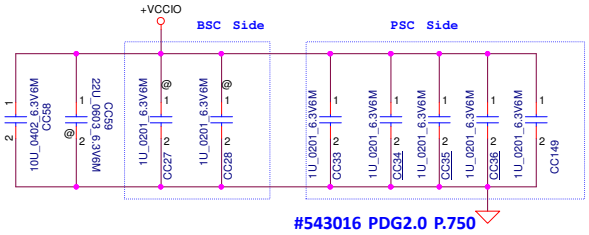


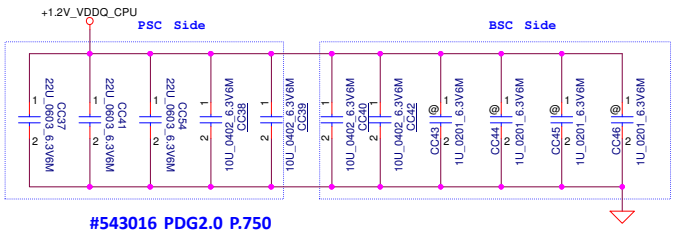
+1.0VALW_PRIM TO +1.0VS_VCCSTG





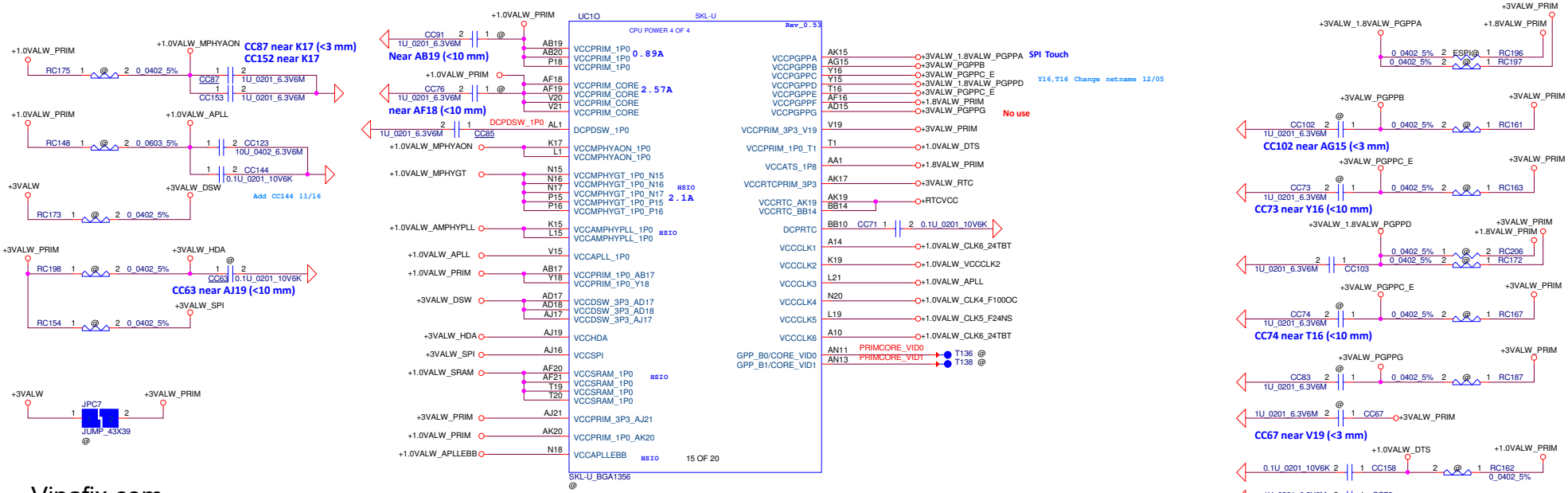




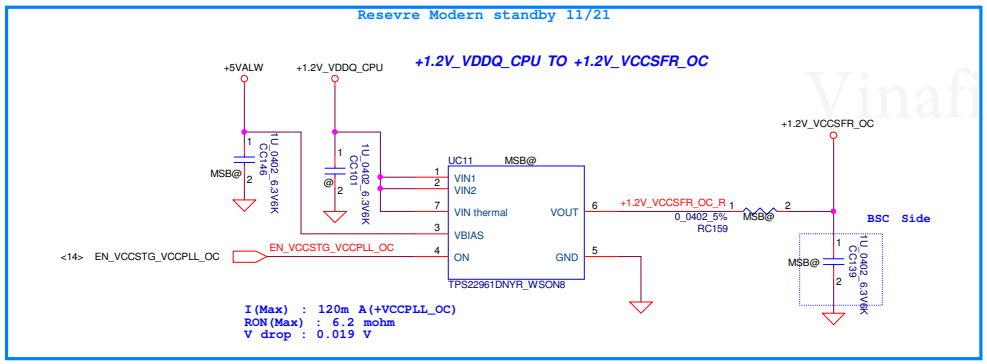


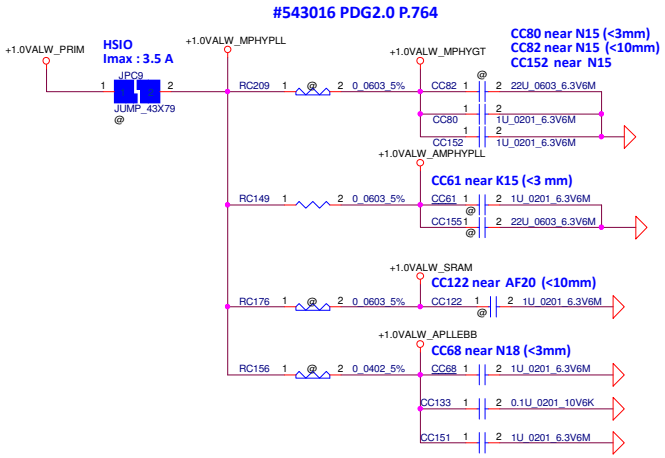
Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

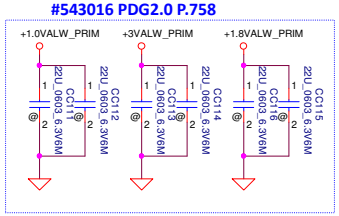
Compal Electronics, Inc.			
Title: KBL-U(8/12)Power			
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
Date: Monday, May 13, 2019	Sheet 14 of 58		



Vinafix.com

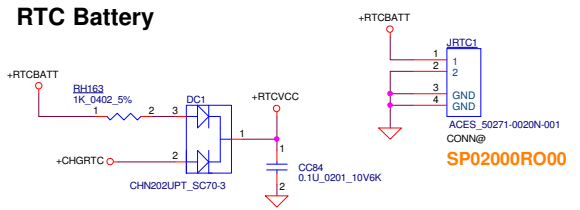






#543016 PDG2.0 P.470
VCCRTC does not exceed 3.2 V.

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+RTCVCC	3.143V
Result : Pass	



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.

Title: KBL-U(9/12)Power

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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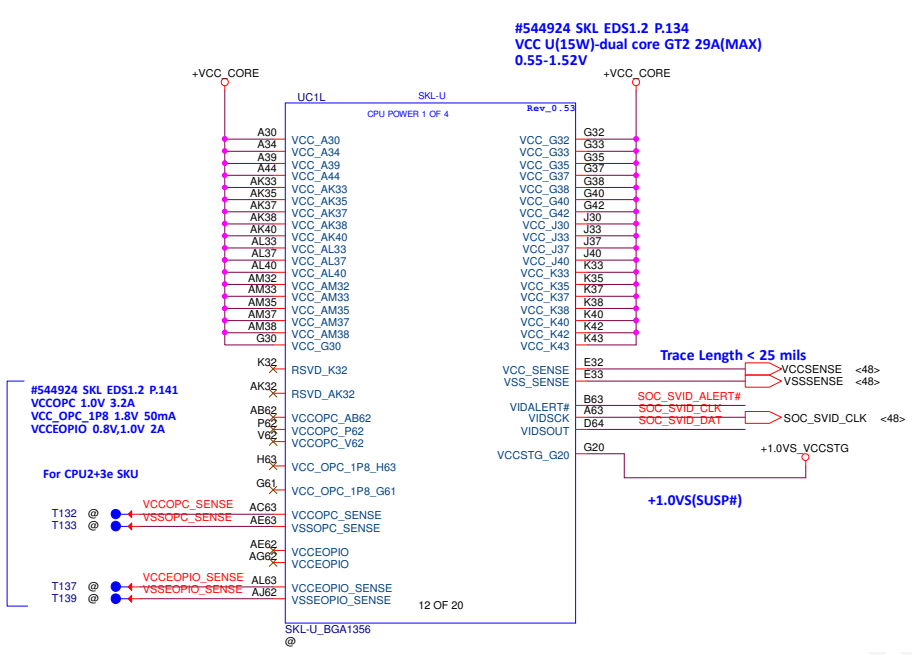
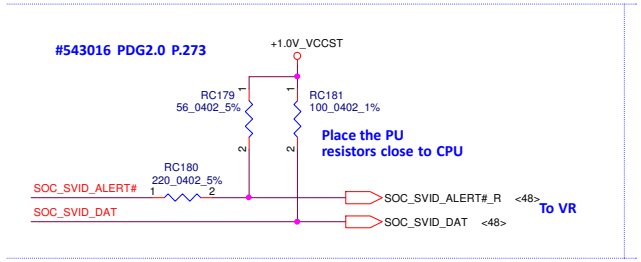
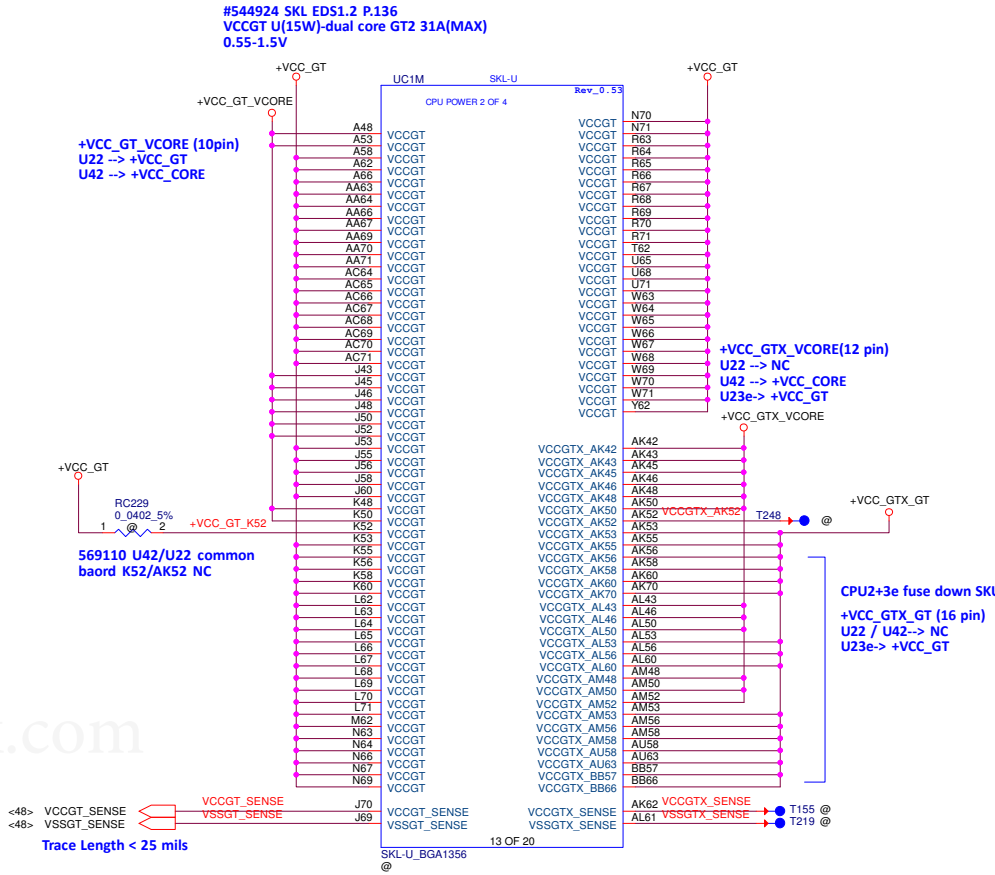




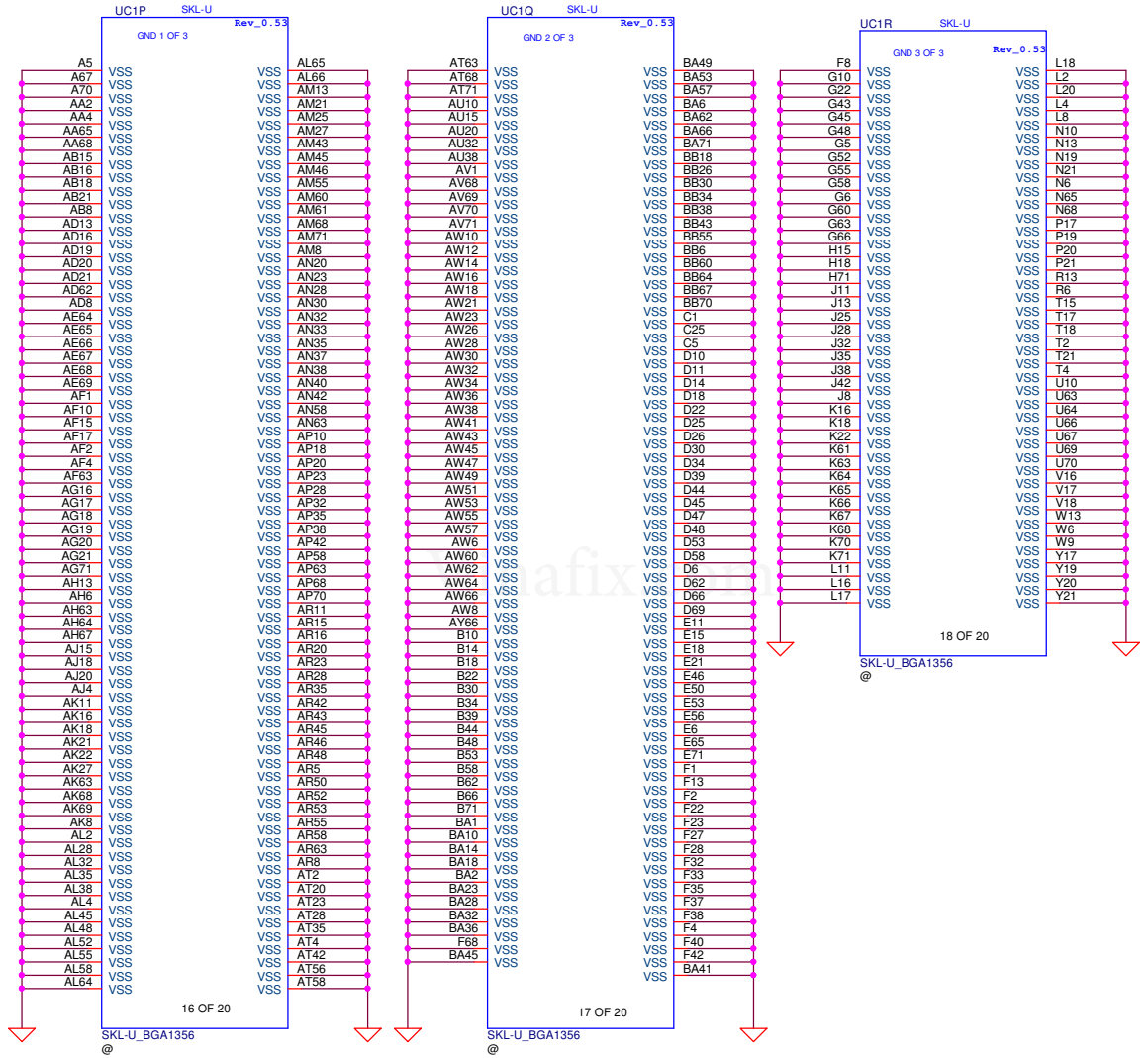


Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.			
Title	KBL-U(10/12)Power,SVID		
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
Date: Monday, May 13, 2019	Sheet 16 of 58		



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.

Title: **KBL-U(11/12)GND**

Size	Document Number	Rev
Custom	EH7L1 LA-H781P	1B

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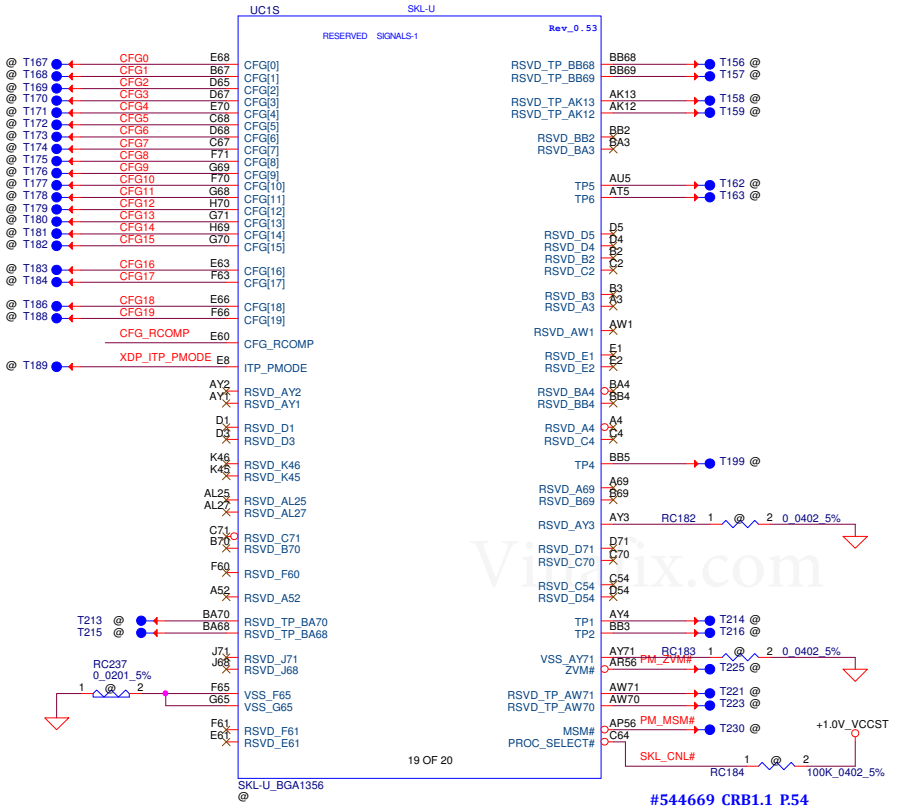
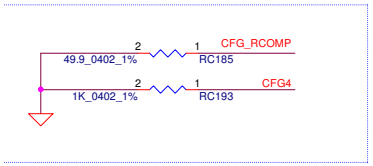
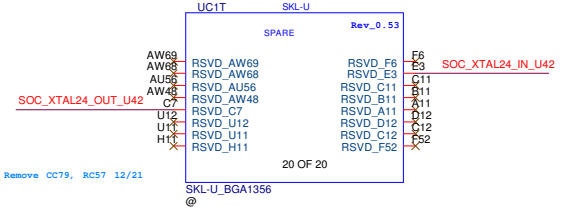






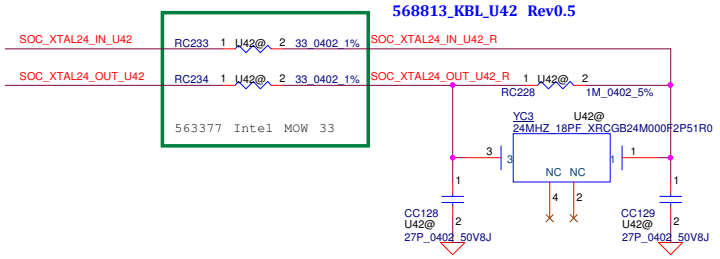
For 2+3e Solut i on

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solut i on f or OPQ.

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.

Title: KBL-U(12/12)RSVD

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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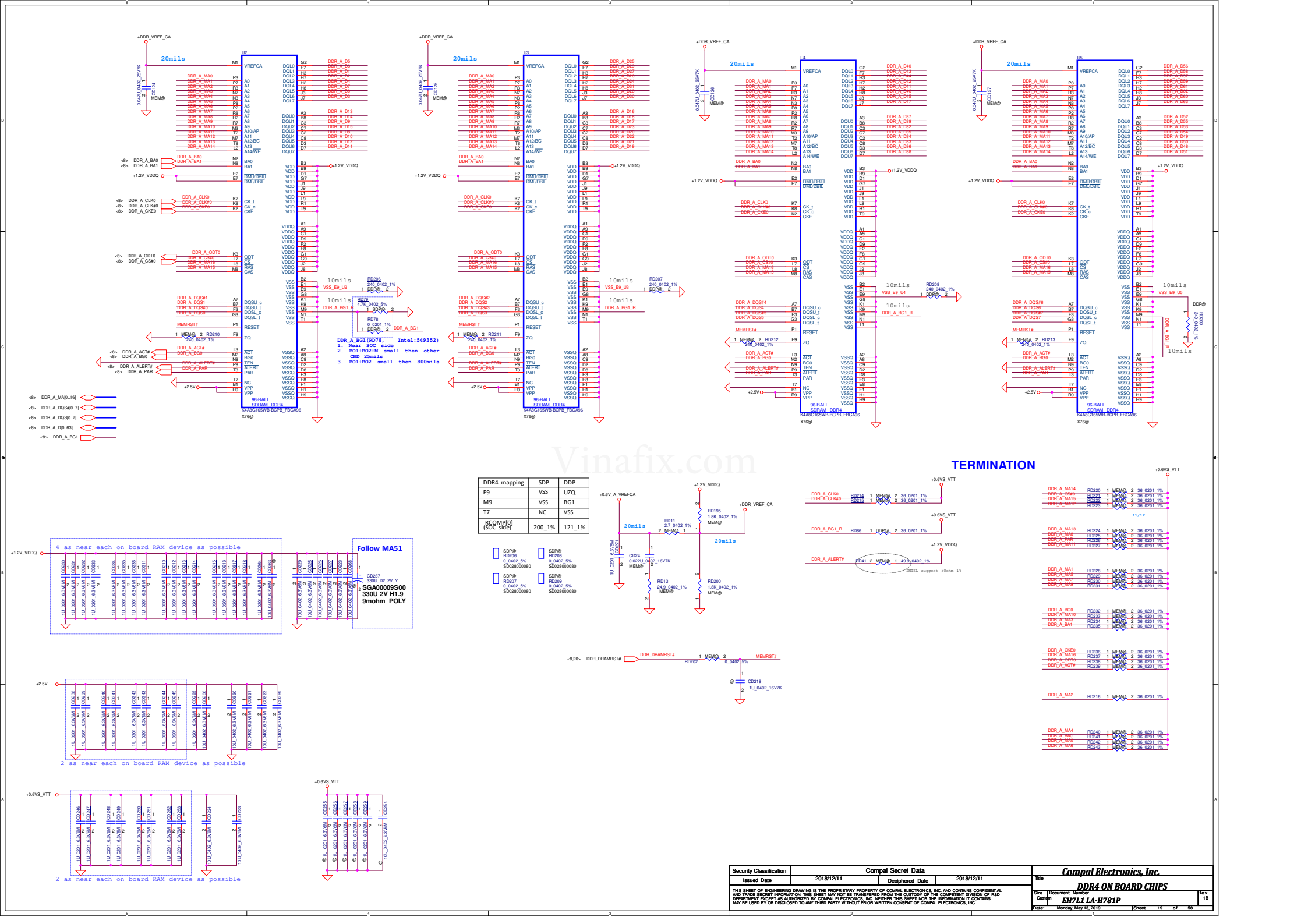

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.	
Title	DDR4 ON BOARD CHIPS
Size: Custom	Document Number: EH7L1 LA-H781P
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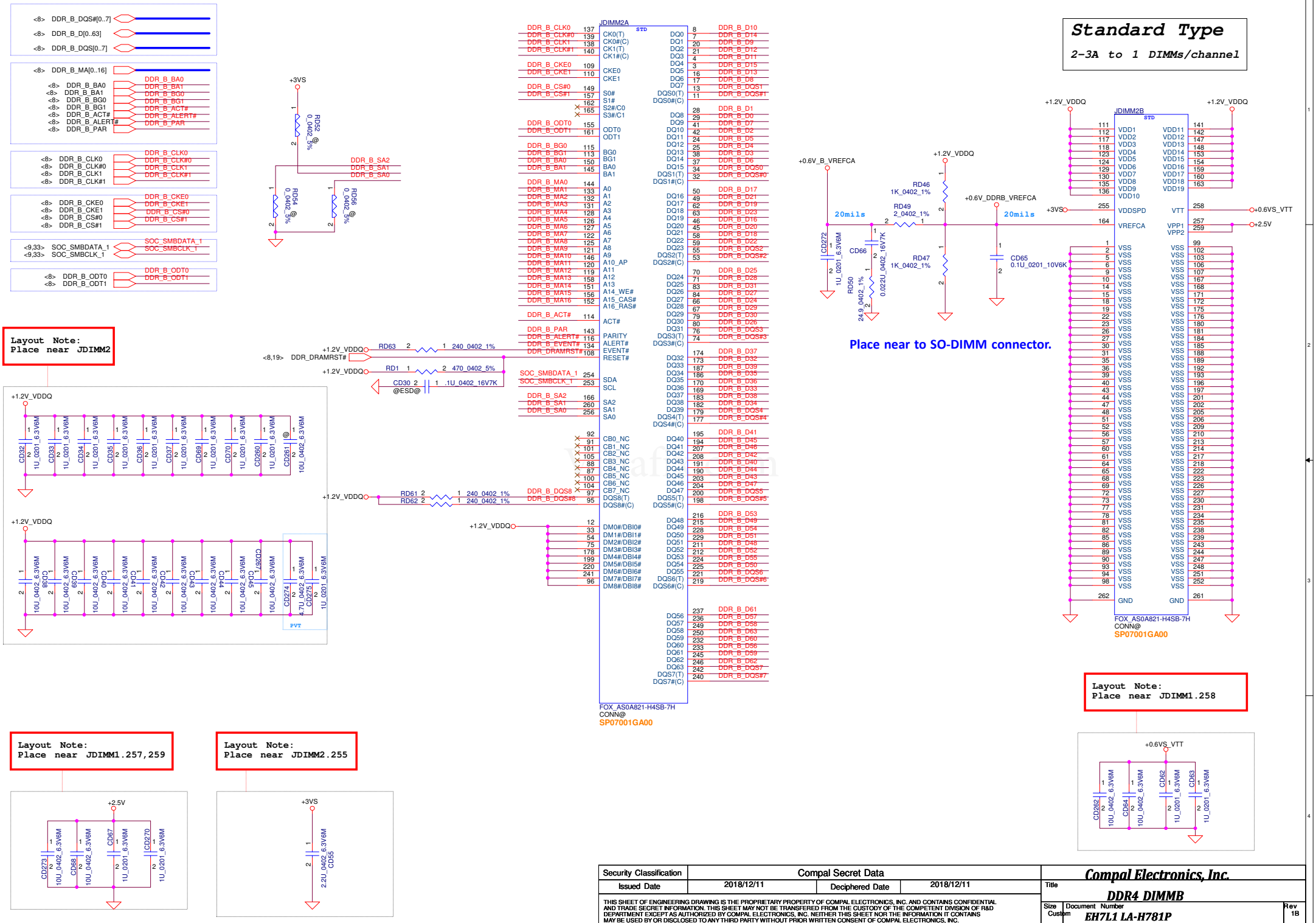
Standard Type

2-3A to 1 DIMMs/channel



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.			
Title	DDR4 DIMMB		
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
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N16 GPU

GPIO	I/O	USAGE
GPIO0	O	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	I	FRAME_LOCK#
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		

N17 GPU

GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	I/O	NVVDDS_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16		Reserved
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D_VISION
GPIO20		Reserved
GPIO21		Reserved (OC_WARN)
GPIO22		Reserved
GPIO23		Reserved

DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU

GC6 2.0 function

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

Security Classification	Compal Secret Data		
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Title: N16X/N17S PEG 1/9

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VRAM Interface

<26> MDA[15..0]
<26> MDA[31..16]
<27> MDA[47..32]
<27> MDA[63..48]

UGPU1
S IC N16S-GTR-S-A2 BGA 595P GPU ABO !
MX130@
SA00009FP40

UGPU1
S IC N16S-GTR-S-A2 BGA 595P GPU ABO !
MX130BR@
SA00009FP70

UGPU1
S IC N17S-G1-A1 BGA 595P GPU ABO !
N17SG1@
SA0000ANV10

UGPU1 N17SG0R1@
S IC N17S-G0-A1 BGA 595P GPU
SA0000CC900

UGPU1 N17SG0R3@
S IC N17S-G0-A1 BGA 595P GPU ABO !
SA0000CC920

UGPU1 N17SG2R1@
S IC N17S-G2-A1 BGA 595P GPU
SA0000CCB00

UGPU1 N17SG2R3@
S IC N17S-G2-A1 BGA 595P GPU ABO !
SA0000CCB20

UGPU1B
Part 2 of 6
MEMORY INTERFACE A
GM108-ES-S-A1_FCBGA595
@

CMDA[31..0] <26,27>

+1.35VSDGPU

CMDA14 2 VGA@ 1 RV87 10K_0402_5%
CMDA30 2 VGA@ 1 RV88 10K_0402_5%
CMDA13 2 VGA@ 1 RV89 10K_0402_5%
CMDA29 2 VGA@ 1 RV90 10K_0402_5%

+3VS

RV106 10K_0402_5% @
RV108 10K_0402_5% @
QV7A @
QV7B PJT138KA 2N SOT363-6 @
PJT138KA 2N SOT363-6

Power Side PU to +3VS_1.8VSDGPU_AON

RV188 0_0402_5% 1 VGA@ 2 VGA_CORE_PG

DV10 N17S@ RB751S40T1G_SOD523-2

RV103 10K_0402_1%
DGPU_MAIN_EN
CV231 @ .1U_0402_16V7K
<21,39> 3_1.8VSDGPU_MAIN_EN

UV10 N16X@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
VCC: 2.0 ~ 5.5V
Push Pull Output

+3VS_1.8VSDGPU_AON
VCC: 1.65 ~ 5.5V
Push Pull Output
UV10 N17S@ NL17SZ08DFT2G_SC70-5
PEX_VDD_EN
PEX_VDD_EN <39,52>
DGPU_PWR_EN <12,39>

DV7 N17S@ RB751S40T1G_SOD523-2
<21,36> GPU_OVERT#
RV189 N17S@ 2.2K_0402_5% SD028220180
RV189 1 N16X@ 2 1K_0402_1%
NVVDD_EN <53>
DV11 @ RB751S40T1G_SOD523-2
CV263 .1U_0402_16V7K VGA@

+3VS_1.8VSDGPU_AON
CV230 0.1U_0201_10V6K @
<21> PLTRST_VGA#
+3VS_1.8VSDGPU_AON
RV105 10K_0402_5%
<21> GC6_FB_EN1V8
QV6A PJT138KA 2N SOT363-6 @
QV6B PJT138KA 2N SOT363-6 @
UV9
RV281 100K_0402_5%
NL17SZ08DFT2G_SC70-5
VGA_CORE_PG
VGA_CORE_PG <53>
Reserve RV281 11/28

Near Power PWM IC

VCC: 1.65 ~ 5.5V
Push Pull Output

Thermal shutdown protection

UV9 N16SGTR@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
UV9 N16SGTRBR@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
UV9 N17SG1@ NL17SZ08DFT2G_SC70-5 SA00003R000

-> UV9:
CQ/BR 940MX V
CQ/BR MX130 X
CQ MX150 V
CQ MX230/MX250 X

-> QV6:
940MX/MX130/MX150/MX230/MX250 X

-> DV7:
CQ 940MX V
BR 940MX X
CQ/BR MX130 X
MX150/MX230/MX250 V

DV7 MX130@ RB751S40T1G_SOD523-2 SCS00006300

-> DV11: MX150/MX230/MX250 remove

-> RV102 and CV230:
CQ/BR 940MX V
CQ/BR MX130 X
CQ MX150 V
CQ MX230/MX250 X

RV102 N16SGTR@ 10K_0402_5% SD028100280
RV102 N16SGTRBR@ 10K_0402_5% SD028100280
RV102 N17SG1@ 10K_0402_5% SD028100280
CV230 N16SGTR@ 0.1U_0201_10V6K SE00000SV00
CV230 N16SGTRBR@ 0.1U_0201_10V6K SE00000SV00
CV230 N17SG1@ 0.1U_0201_10V6K SE00000SV00

For N16X (not used)
UV9 MC74VHC1G08DFT2G_SC70-5 SA00000OH00
QV6 2N7002KDW_SOT363-6 SB00000EO00

+PEX_IOVDDQ
15+55mA
Place Under F16 P22
+FB_PLLAVDD
L2002 PBY160808T-300Y-N_2P
C2008 22U_0603_6.3V6M
C2011 .1U_0402_16V7K
C2010 .1U_0402_16V7K
C2009 0.1U_0201_10V6K
C2736 0.1U_0201_10V6K
Place Near GPU
Place Under H22
SM010008A00 3000ma 30ohm@100mhz DCR 0.03

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Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

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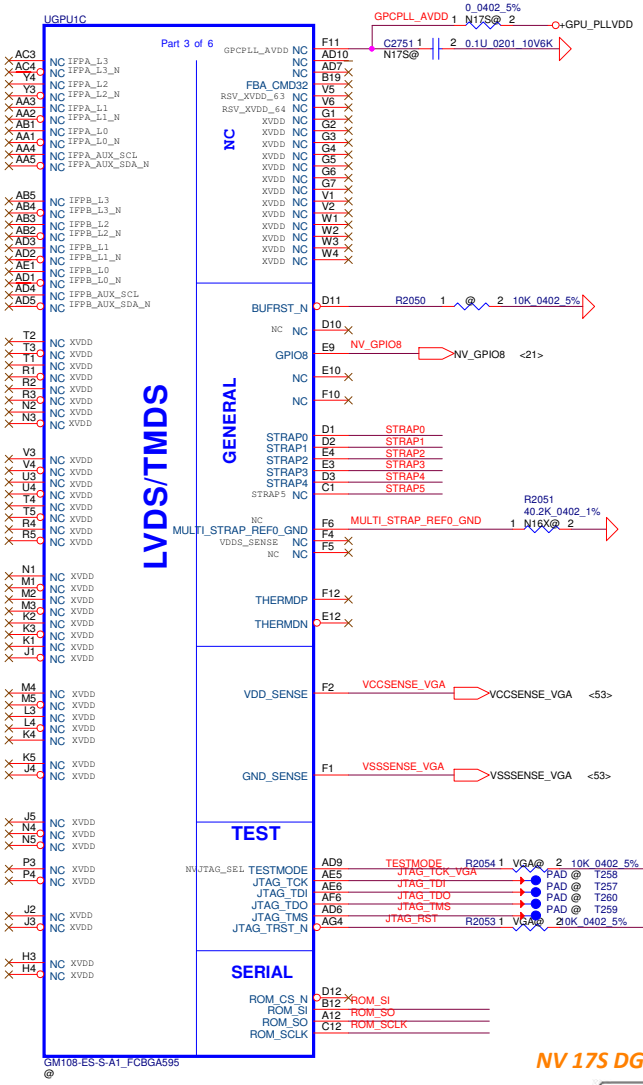
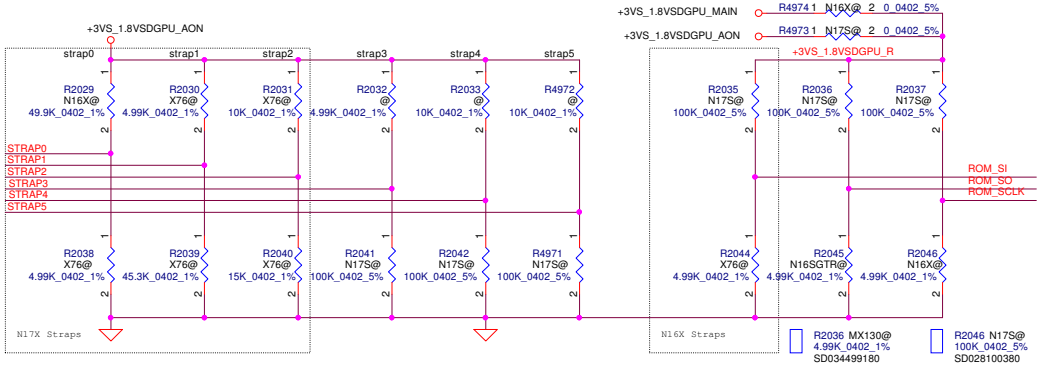




Multi strap table

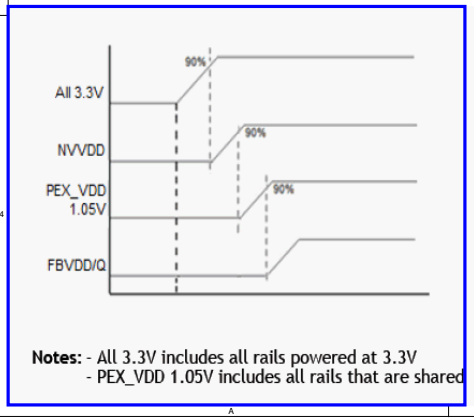
Decive ID : N16S-GTR 0x134D
MX130 0x174D

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N16S-GTR	+1.35V		X76828BOL09	2.5GHz	256Mx32x2 2G	0x0 (SA00009TA10) Samsung K4G80325FB-HC25	PU 49.9K	NC	NC	NC	NC	NC	PD 4.99K (R2044)	PD 4.99K	PD 4.99K
			X76828BOL08			0x8 (SA00009TV50) Micron MT51J256M32HF-70:B							PU 4.99K (R2035)		
			X76828BOL07			0x9 (SA00009U160) Hynix H5GC8H24AJR-R0C							PU 10K (R2035)		

Decive ID :N17S-G0-A1 0x1D11 / N17S-G2-A1 0x1D13

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G0 / N17S-G2	+1.35V		X76828BOL03	3.0GHz	256Mx32x2 2G	0x0 (SA00009TA10) Samsung K4G80325FB-HC25	PD 100K	PD 100K	PD 100K	PD 100K	PD 100K	PD 100K	PU 100K	PU 100K	PU 100K
			X76828BOL02			0x4 (SA00009TV50) Micron MT51J256M32HF-70:B	PD 100K	PD 100K	PU 100K						PD 100K
			X76828BOL01			0x5 (SA00009U160) Hynix H5GC8H24AJR-R0C	PU 100K	PD 100K	PU 100K						

VGA Power Sequence (N16X)



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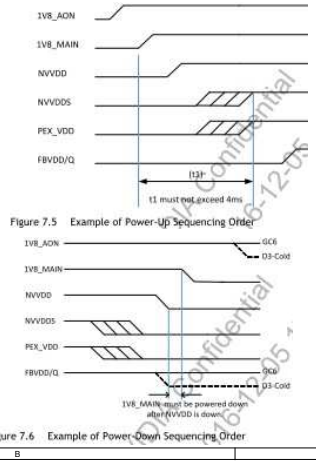

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Table 3-4. GPU Core Sensing Line Routing Constrains

Constraint Parameter	Requirement
Single-ended impedance	25 Ω ± 10%
Differential Trace Impedance	50 Ω ± 15%
Reference Plane	GND Reference
Routing Type	Stripline[1] or Microstrip
Dielectric spacing	Stripline: ≥ 3.0x dielectric Microstrip: ≥ 4.0x dielectric
Intrapair skew	≤ 5 ps
Via stub	
Trace length	GPU to R_S/R_G ≤ 250 mm (9842.5 mil) R_S/R_G to VR ≤ 50 mm (1968.5 mil)

Note:
1. Stripline is recommended to minimize EMI. Do not route over any voids.

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

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Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 µF X7R	0402	N/A	1	Under GPU
	4.7 µF X6S	0603	N/A	1	Near GPU
	22 µF X6S	0805	N/A	1	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU

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Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

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Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

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Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

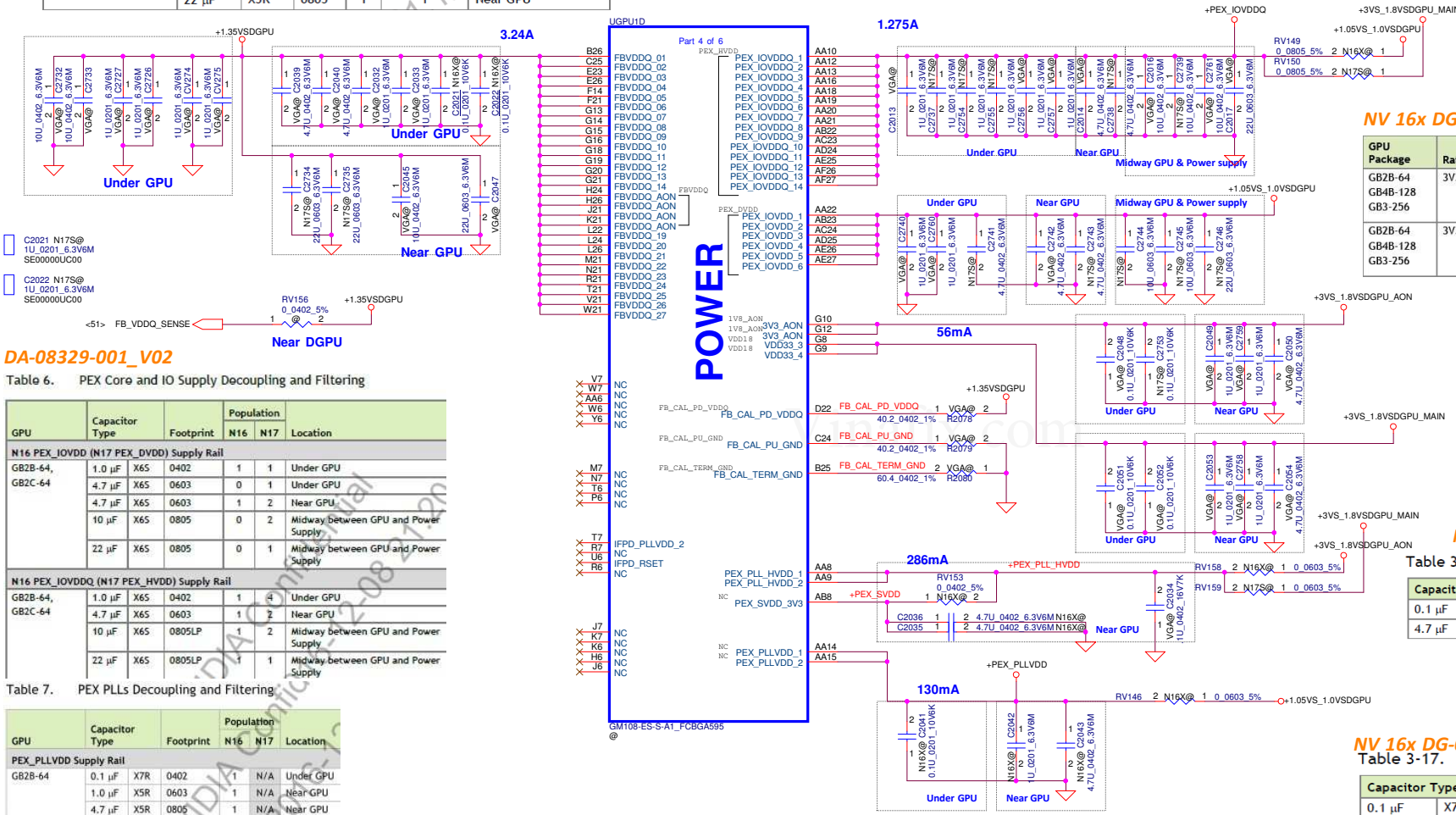

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Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5/ BGA-170	1.35 V or 1.50 V	40.2 Ω	40.2 Ω	60.4 Ω

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GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

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Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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Table 9. VDD AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU
N16 3V3_AON (N17 1V8_AON) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU

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Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

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Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU

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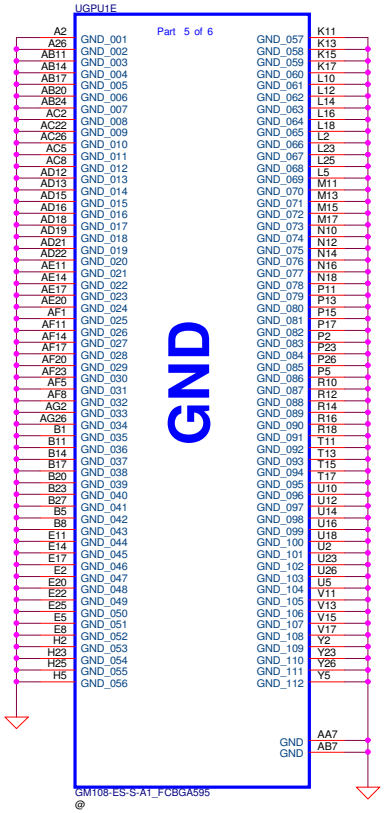

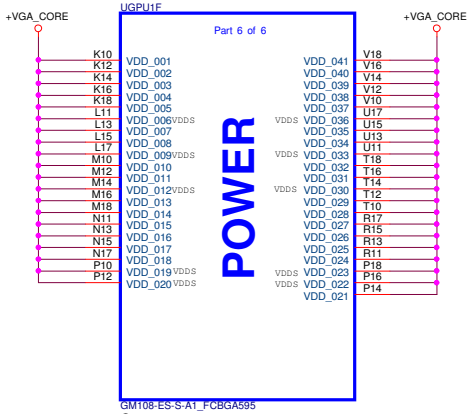

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Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

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Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	330 µF	POS	7343	N/A	1	Near GPU

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Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	–	2.0	–	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	–	2.0	–	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16S-GMR	GDDR5	34.0	–	2.9	–	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	–	3.1	–	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

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Table 5. EDP-Continuous [3]

Product	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	18.5	–	2.0	–	4.2	0.8	0.06
	GDDR5 @ 2.5 GHz	18.5	–	2.0	–	4.7	0.8	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06

Table 6. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	30.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	–	3.1	–	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

SP-08318-001_V03

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	60.1	3.2	6.6	0.2

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: N16X/N17S POWER & GND 5/9

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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VRAM GDDR5 chips

Channel 0 BOT SIDE

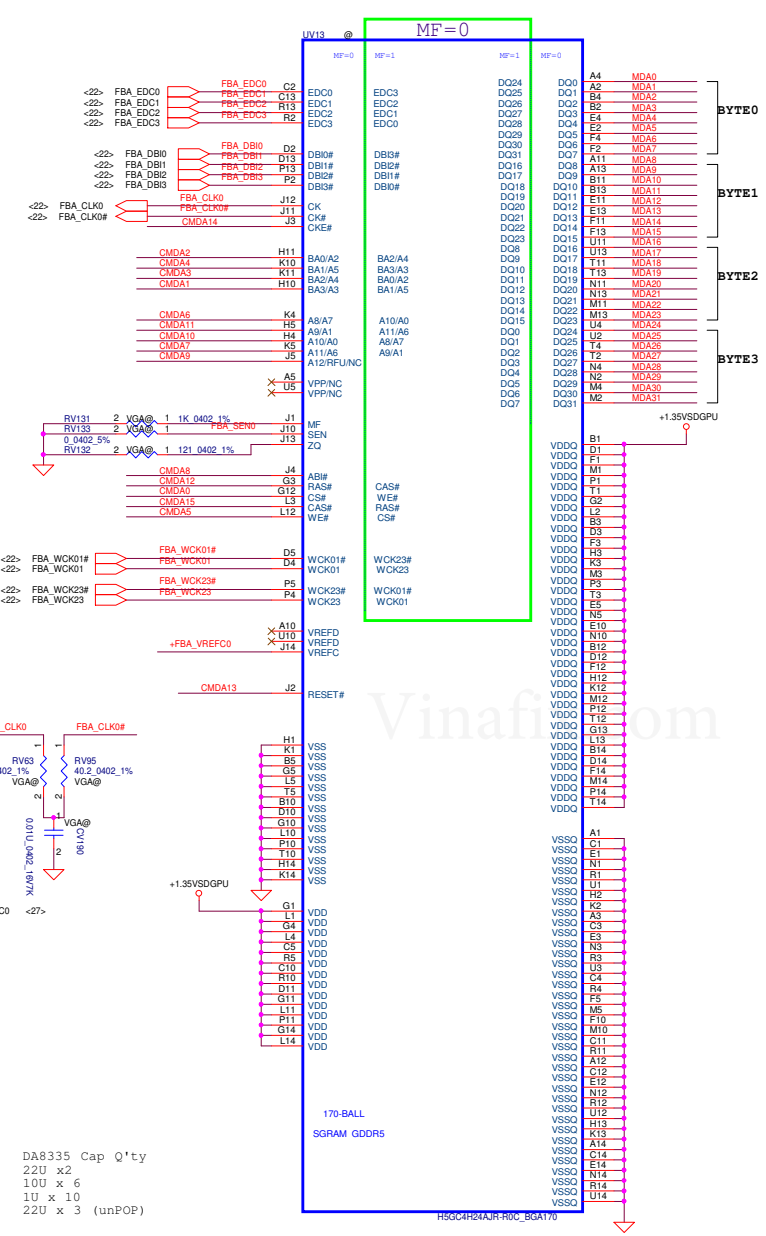
<22,27> MDA[63..0] MDA[63..0]
<22,27> CMDA[31..0] CMDA[31..0]

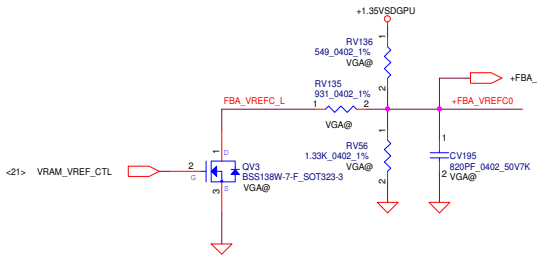
X76 for N16X 2G VRAM

X76 for N17S 2G VRAM

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#





DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: N16X/N17S Lower Rank0 6/9

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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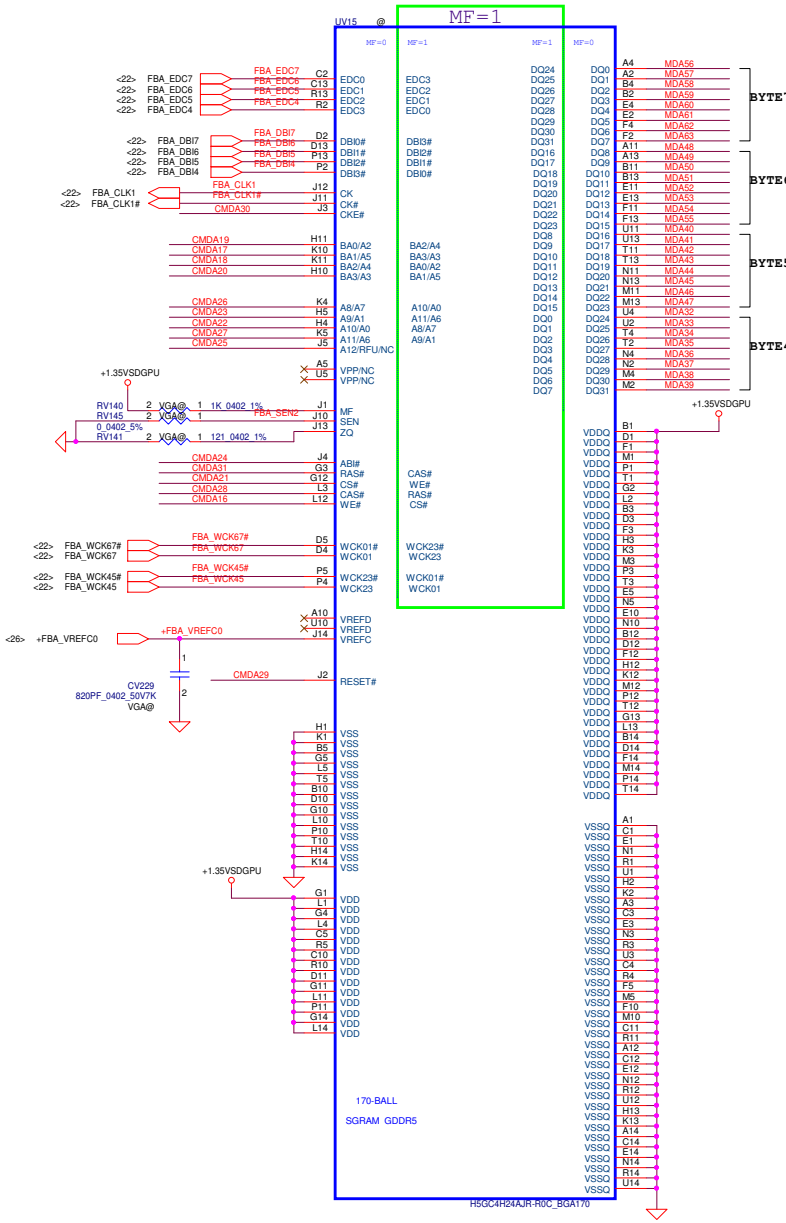
VRAM GDDR5 chips

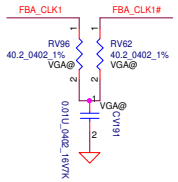
<22,26> MDA[63..0] → MDA[63..0]
<22,26> CMDA[31..0] → CMDA[31..0]

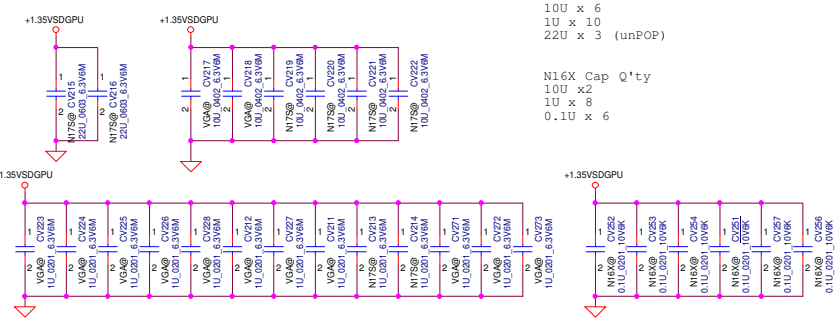
GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 1 BOT SIDE







DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: *N16X/N17S Lower Rank1 7/9*

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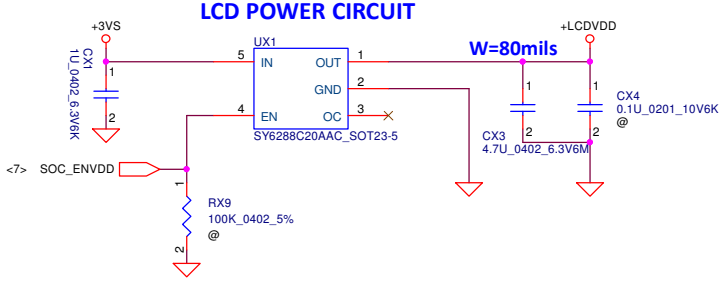
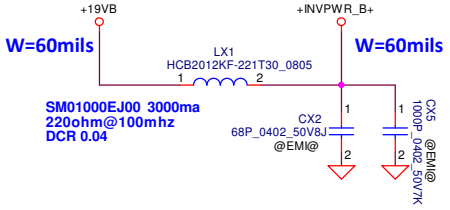
LCD POWER CIRCUIT

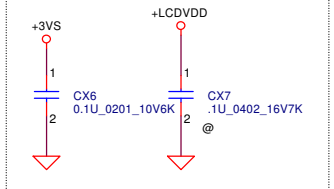


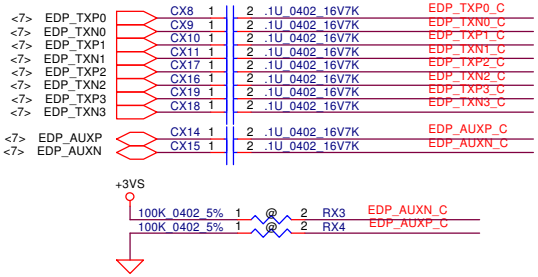
Change to +19VB 11/16

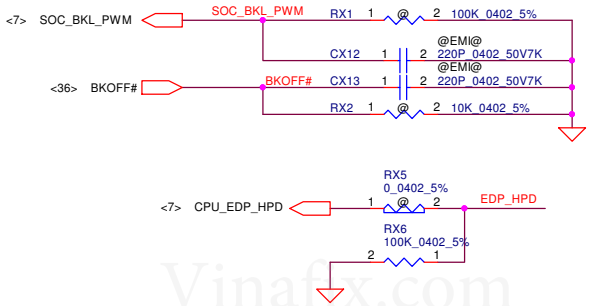


Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

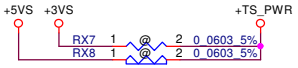
Place closed to JEDP1



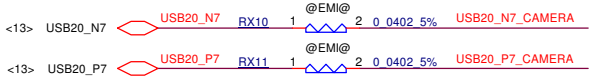




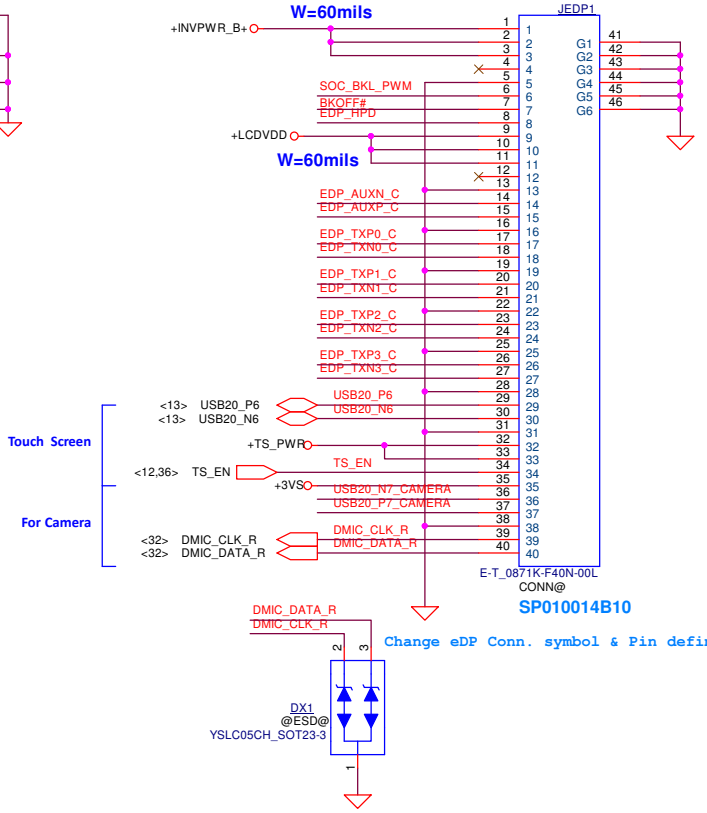
Touch Screen



Camera



LED PANEL Conn.



Change eDP Conn. symbol & Pin define 11/20

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title: eDP Connector			
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
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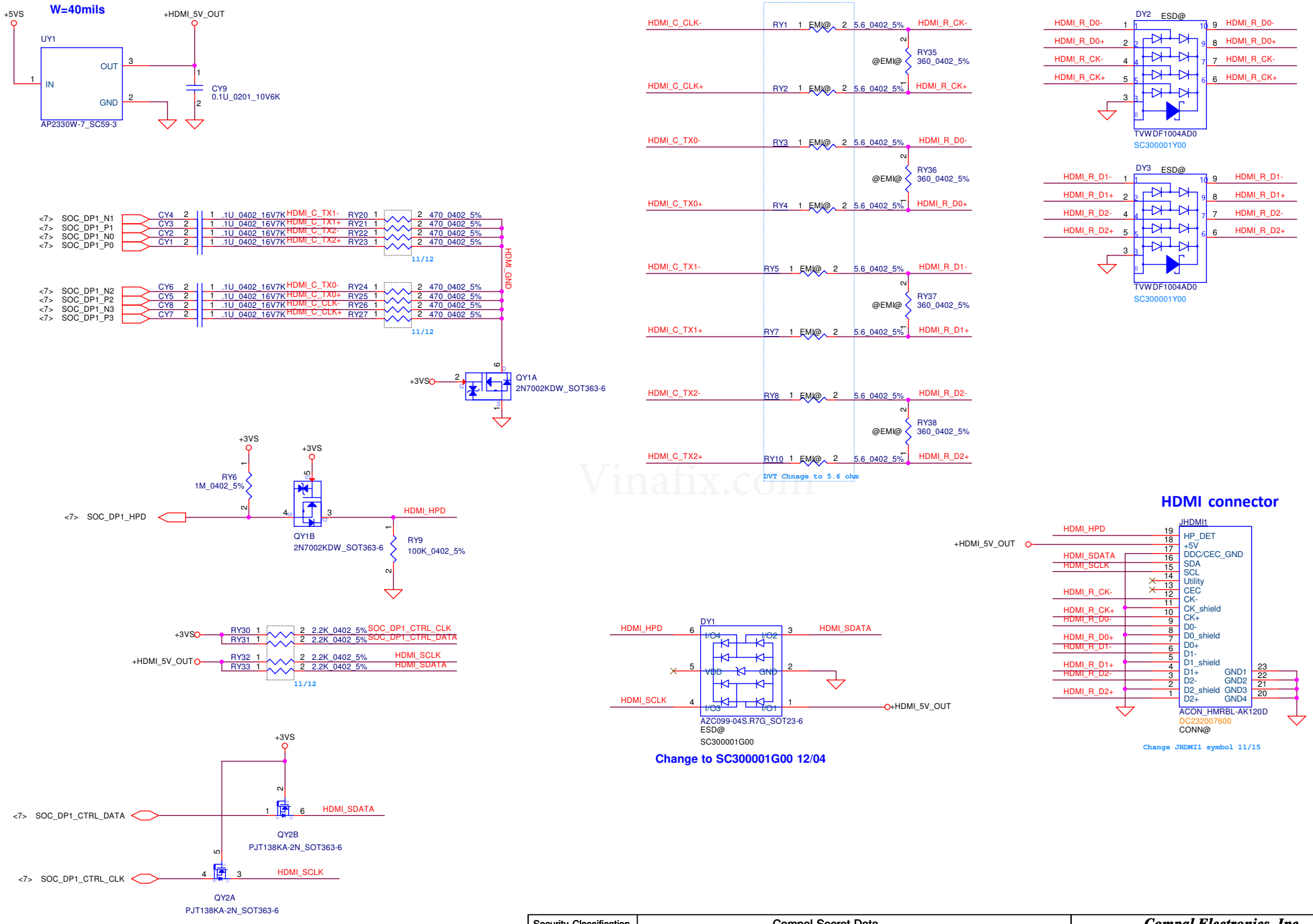

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title: HDMI CONN.			
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
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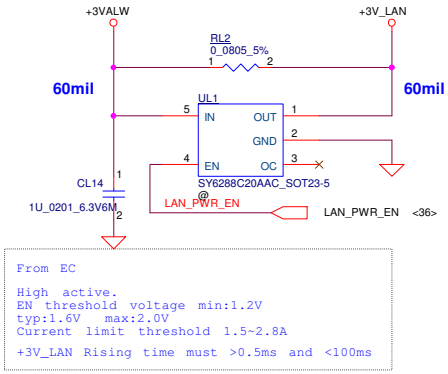
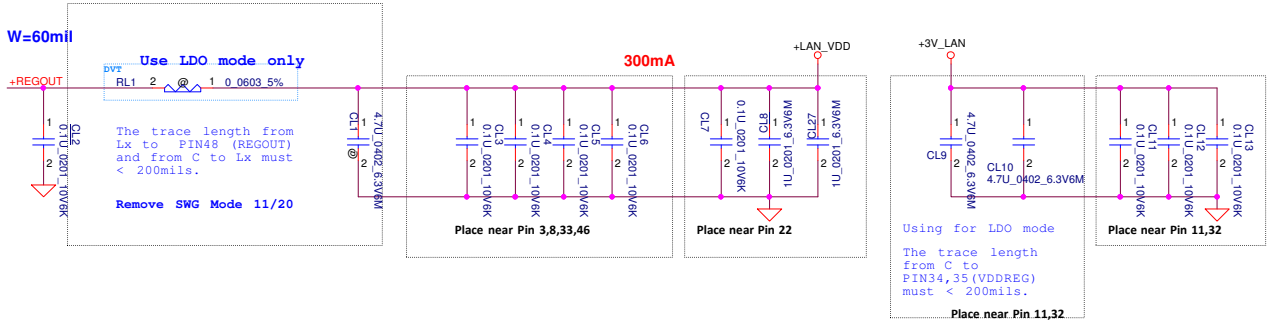
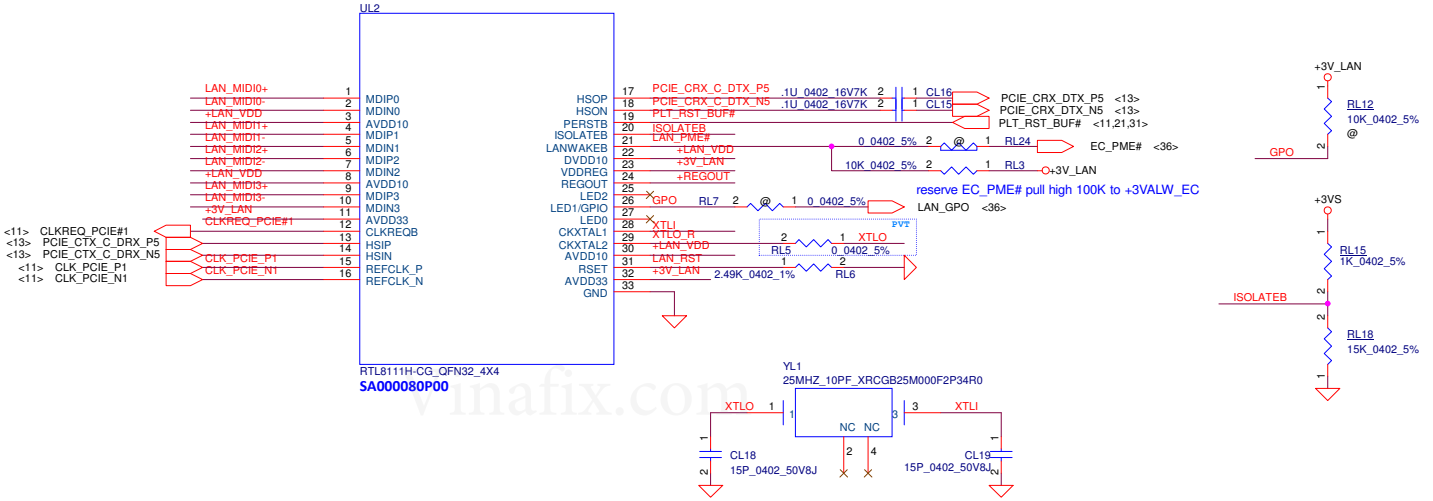
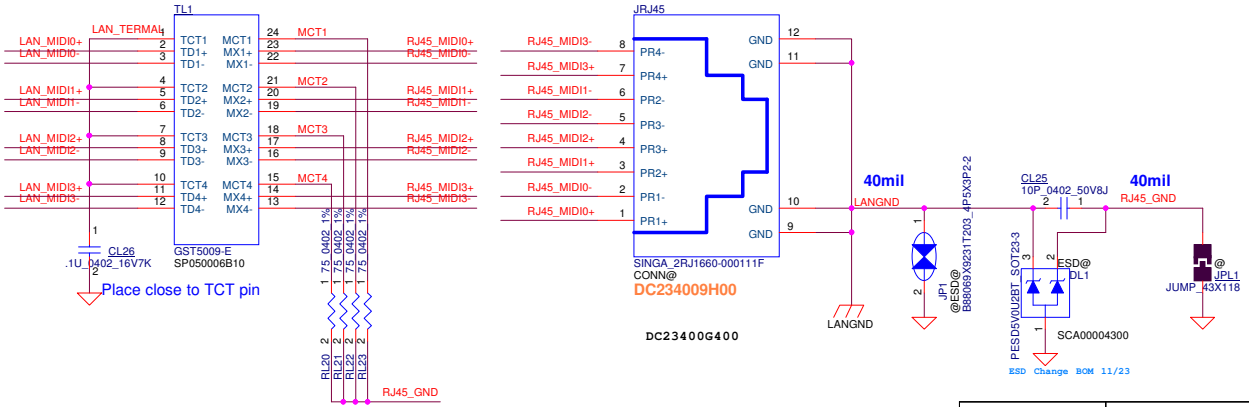
LAN-RTL8111H









Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	LAN RTL8111H		
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
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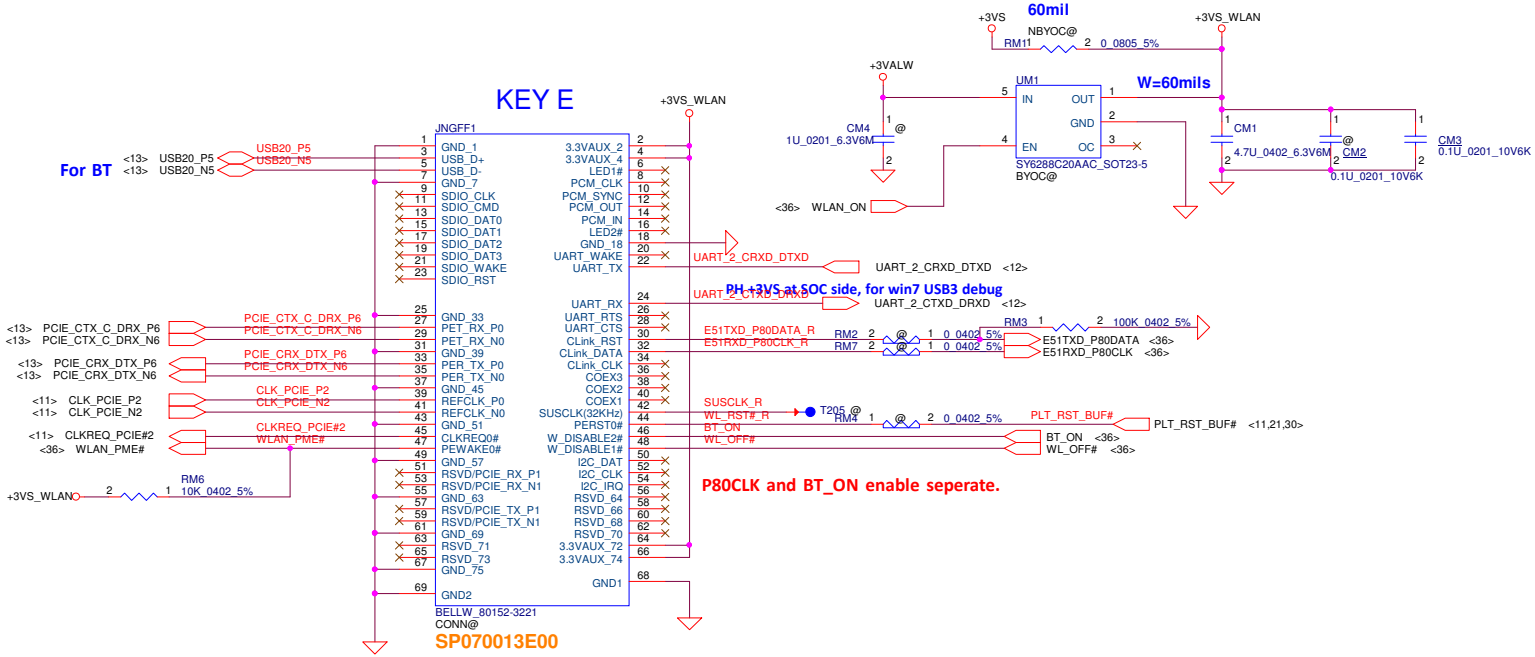
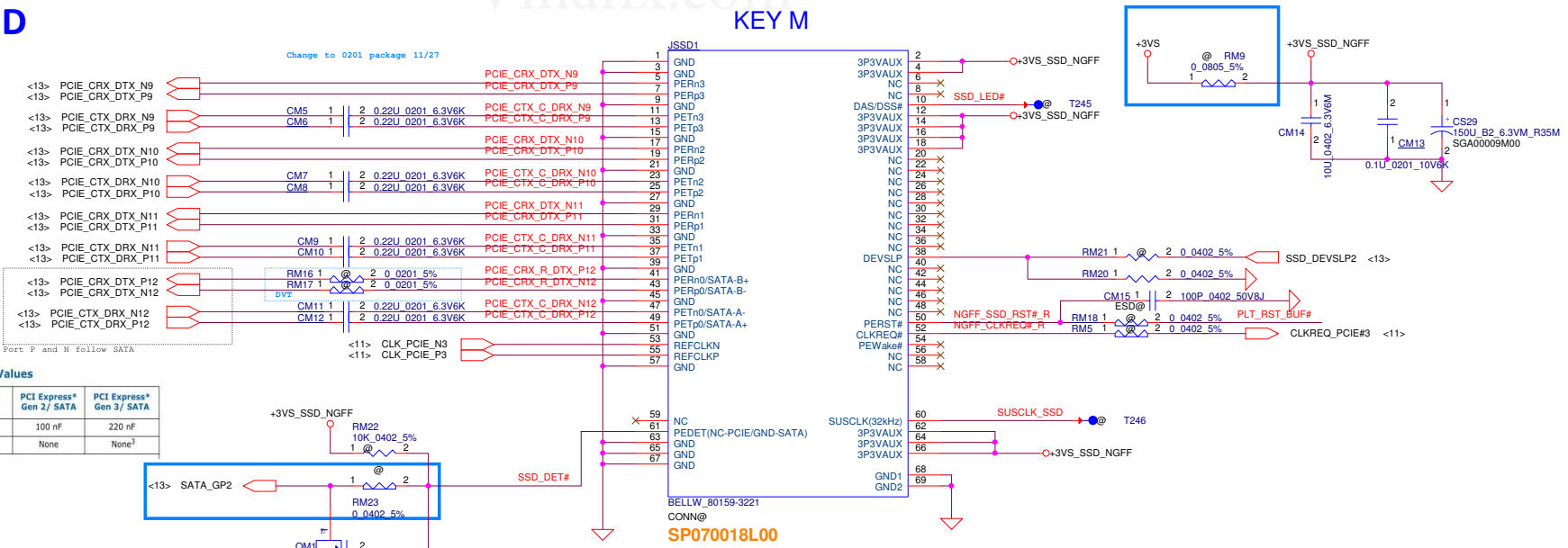
Wireless LAN

NGFF WL+BT (KEY E)



mSATA/SSD



PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	M.2 Key E (WLAN)/Key M(SSD)
Size / Custom	Document Number: EH7L1 LA-H781P
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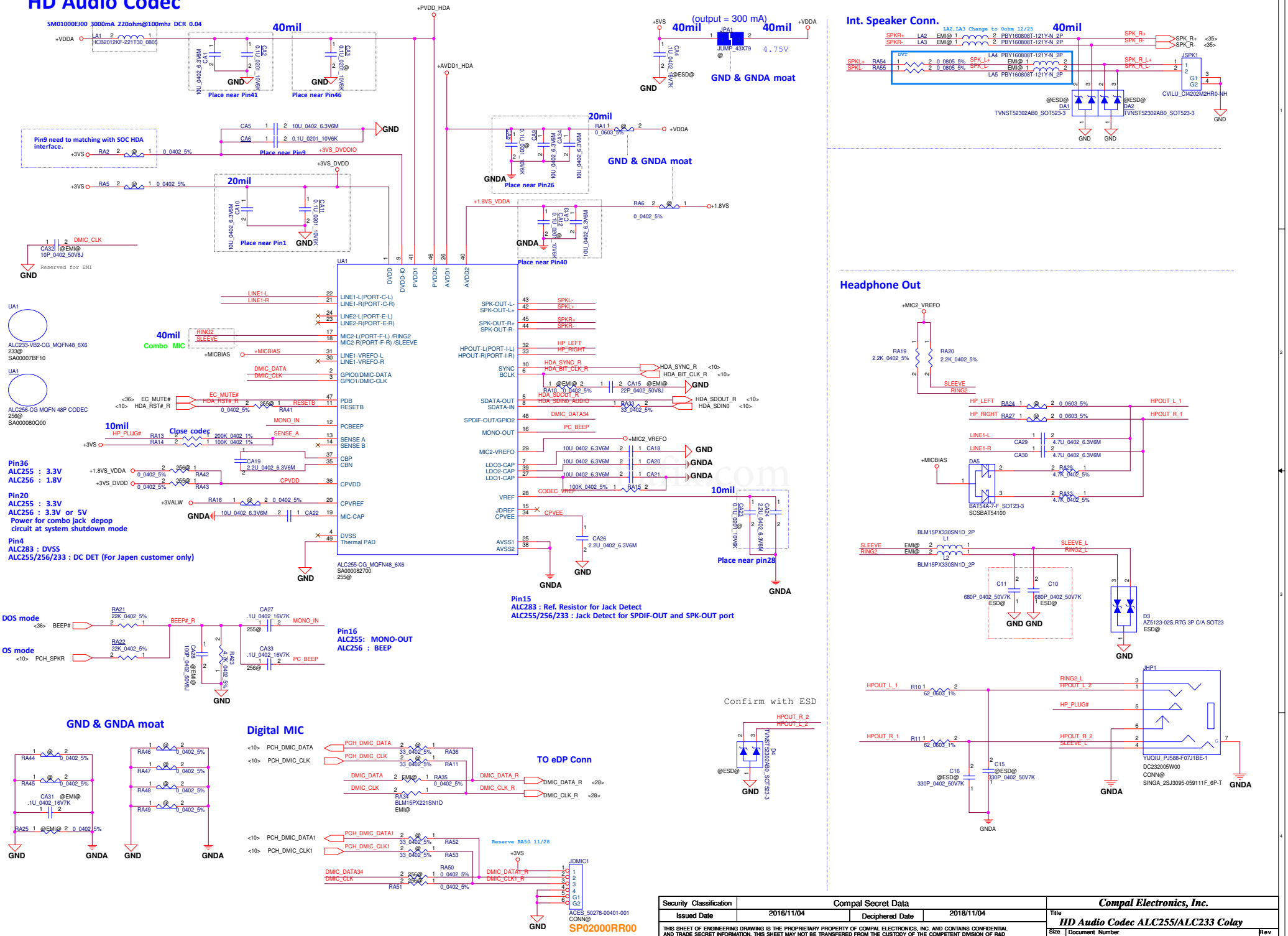
HD Audio Codec



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Compal Electronics, Inc.

Title: *HD Audio Codec ALC255/ALC233 Colay*

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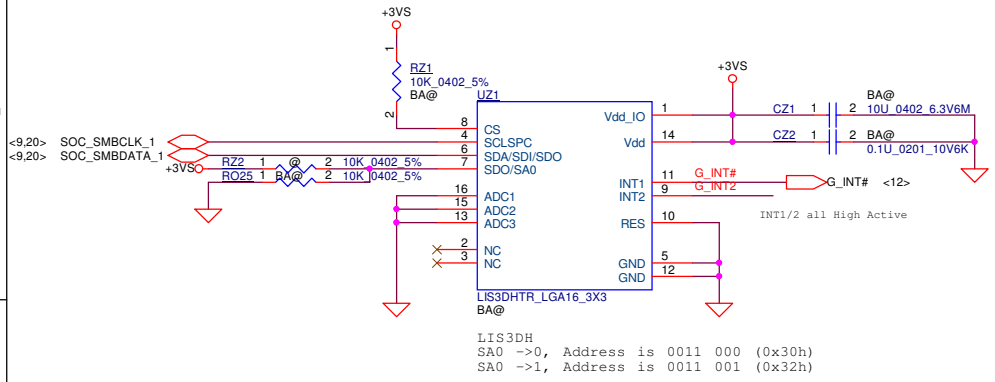
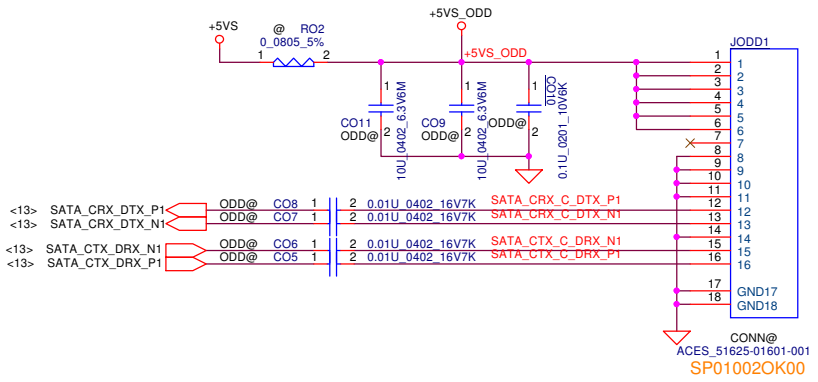
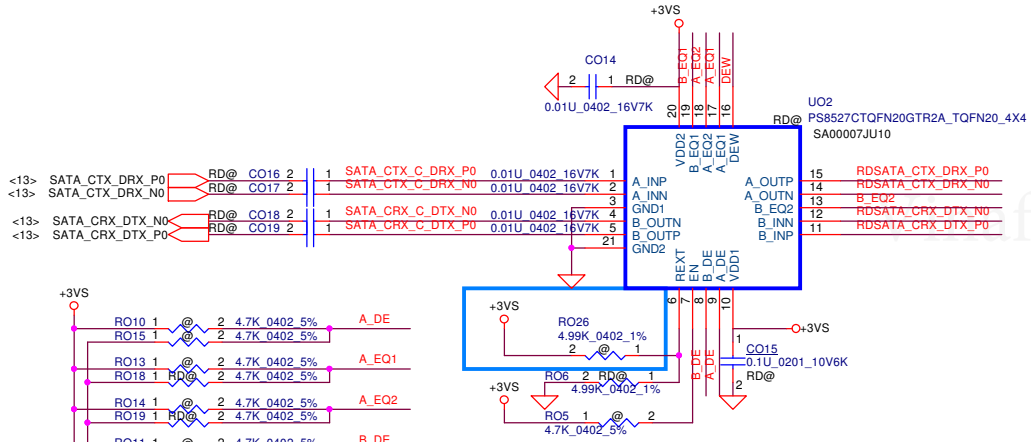
G-Sensor reserved for BA serial

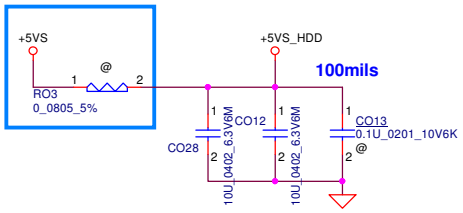


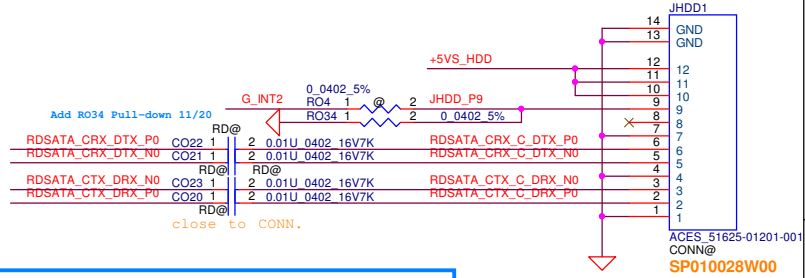
SATA ODD Conn.



SATA Re-Driver and cable HDD Conn.



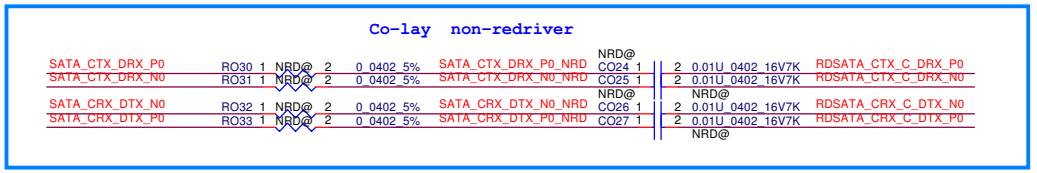




PS8527C EQ and DE

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
* L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

A_DE	De_Emphasis
* M	-3.5dB(Default)
L	0dB
H	-6dB



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Compal Electronics, Inc.

Title: HDD/ODD/ HDD Re-Driver

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

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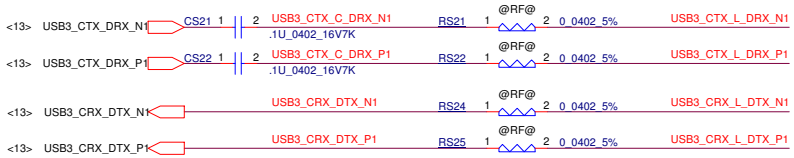
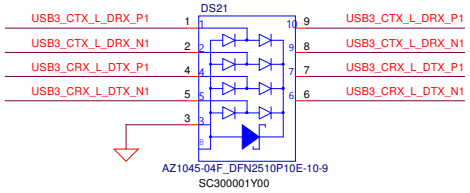
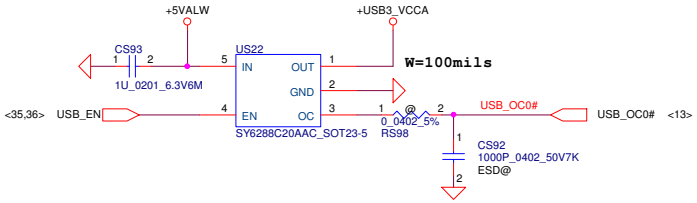
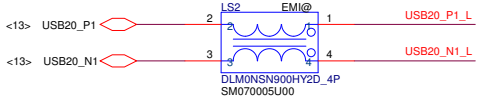
USB3.0 (Port 1)

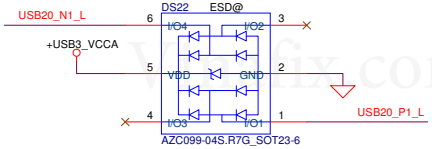


For ESD request

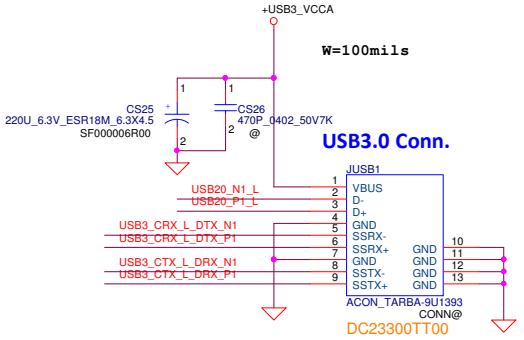








SWAP pin 12/13



Change USB3.0 Conn. symbol 11/16

remove USB Charger IC 12/12

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	USB Conn/USB_B		
Size: Custom	Document Number: EH7L1 LA-H781P		Rev: 1B
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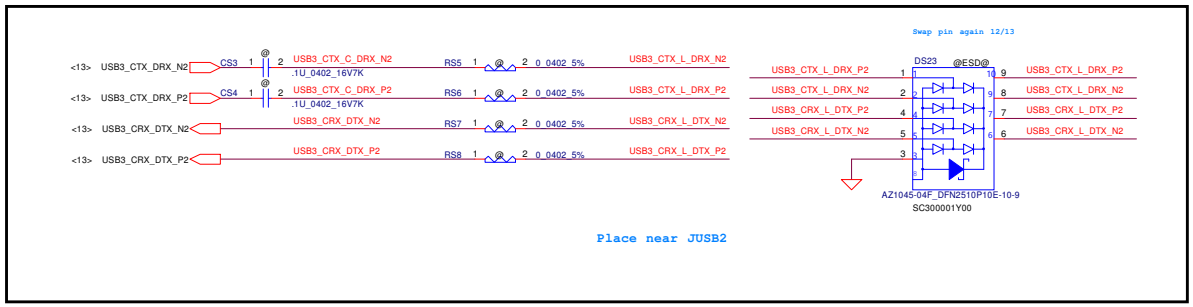
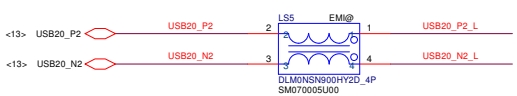
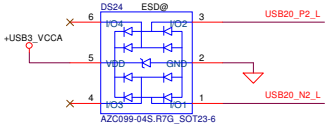
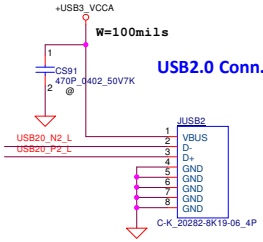
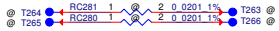
USB2.0 (Port 2)





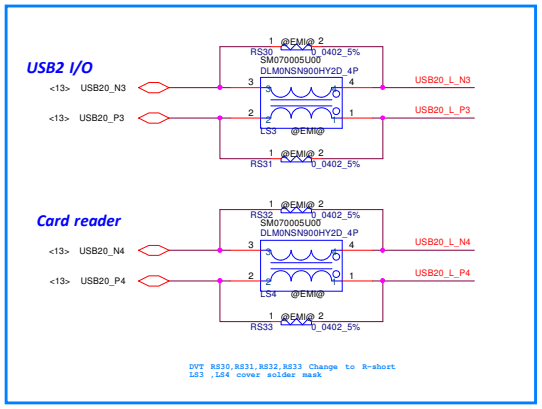


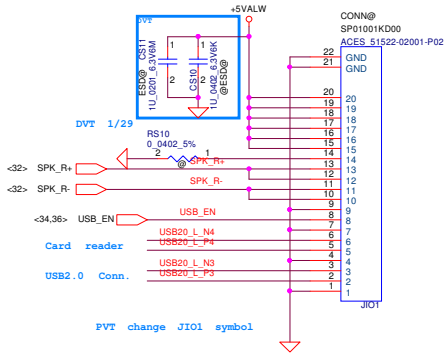




Change USB3.0 Conn. symbol
Reserve U3 first 11/16

USB/B (USBx1,Card Reader,SPK)





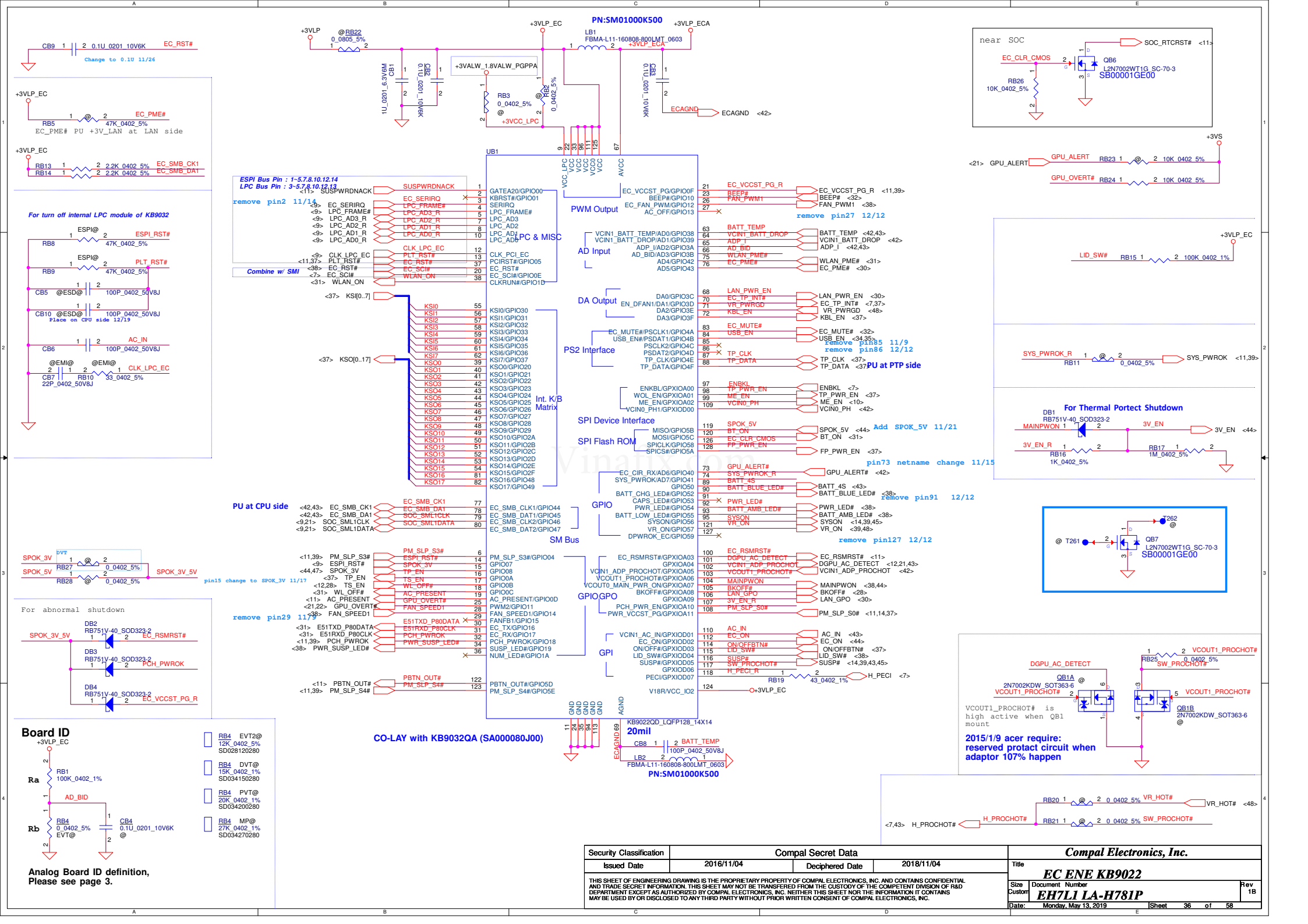
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: USB2.0 / IO_B

Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

Date: Monday, May 13, 2019 | Sheet 35 of 58



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

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Compal Electronics, Inc.

Title: **EC ENE KB9022**

Size: Custom | Document Number: **EH7L1 LA-H781P** | Rev: 1B

Date: Monday, May 13, 2019 | Sheet 36 of 58

change Pin define same as EH5AW 11/16

ON/OFF BTN

RK1 100K_0402_5%
+3VLP
<36> ON/OFFBTN#
ON/OFFBTN#

PVT Remove SWK1 3/27

KSI[0..7]
KSO[0..17]
KSI[0..7] <36>
KSO[0..17] <36>

KB Conn.

JKB1
GND2, GND1
KSO16, KSO17, KSO0, KSO1, KSO2, KSO3, KSO4, KSO5, KSO6, KSO7, KSO8, KSO9, KSO10, KSO11, KSO12, KSO13, KSO14, KSO15
KSI0, KSI1, KSI2, KSI3, KSI4, KSI5, KSI6, KSI7
ON/OFFBTN#
ACES_85201-2805
CONN@
SP01000GO00

KB BackLight

+5VS
U1 IN OUT GND EN OC
SY6288C20AAC_SOT23-5
<36> KBL_EN
+5VS_BL
JBL1
GND GND
ACES_51524-0040N-001
CONN@
SP010022M00
C3 0.1U_0201_10V6K

TP/B Conn.

+3VALW
+3VS
RK3 0_0402_5%
+3V_PTP
UK1 IN OUT GND EN OC
SY6288C20AAC_SOT23-5
CK13 1U_0201_6.3V6M
CK3 1U_0201_6.3V6M
CK1 4.7U_0402_6.3V6M
RK4 10K_0402_5%
EC_TP_INT#
TP_PWR_EN <36>

TP_PWR_EN follow SYSON behavior

EC PS2
PCH I2C
<7,36> EC_TP_INT#
<36> TP_EN
CK2 0.1U_0201_10V6K
JTP1
TP_CLK, TP_DATA, I2C_1_SDA_R, I2C_1_SCL_R, EC_TP_INT#, TP_EN, GND, GND
ACES_51524-00801-001
CONN@
SP01001A910

QK1B 2N7002KDW_SOT363-6
RK7 2.2K_0402_5%
RK10 2.2K_0402_5%
<12> I2C_1_SCL
I2C_1_SCL_R
RK8 0_0402_5%
QK1A 2N7002KDW_SOT363-6
<12> I2C_1_SDA
I2C_1_SDA_R
RK9 0_0402_5%

RK5 4.7K_0402_5%
RK6 4.7K_0402_5%
<36> TP_CLK
<36> TP_DATA
TP_CLK
TP_DATA

Vinafix.com

TPM

change TPM to NPCT750 11/16

+3VALW
RW1 0_0603_5%
+3VALW_TPM
CW1, CW2, CW7 TPM@
near pin1

+3VS
RW2 0_0603_5%
+3VS_TPM
CW3, CW4, CW5, CW6, CW8 TPM@
near pin8,22

RW10 TPM@ 10K_0402_5% TPM_PIRQ#

<9> SOC_SPI_SO — SOC_SPI_SO — RW5 TPM@ 33_0402_5% — SOC_SPI_SO_TPM_R
<9> SOC_SPI_SI — SOC_SPI_SI — RW6 TPM@ 33_0402_5% — SOC_SPI_SI_TPM_R
<9> SOC_SPI_CLK — SOC_SPI_CLK — RW7 TPM@ 33_0402_5% — SOC_SPI_CLK_TPM_R

UW1 place close and before UC7

UW1 TPM@
<11,14,36> PM_SLP_S0# — RW11 TPM@ 0_0402_5%
SDA/GPIO0, SCL/GPIO1, GPIO3, MISO, MOSI/GPIO7, PIRQ/GPIO2, SCLK, SCS/GPIO5, PLTRST, NC, GPIO4, PP/GPIO6
SOC_SPI_SO_TPM_R, SOC_SPI_SI_TPM_R, TPM_PIRQ#, SOC_SPI_CLK_TPM_R, SOC_SPI_CS#2, PLT_RST#
<13> TPM_PIRQ#
<9> SOC_SPI_CS#2
<11,36> PLT_RST#
+3VALW_TPM
+3VS_TPM
VSB, VHIO, VHIO, NC..., GND, GND, PGND
NPCT750AAAYX_QFN32_5X5

SA0000AQ230 S IC NPCT750AAAYX QFN 32P TPM
SA0000AQ250 S IC NPCT750AABYX QFN 32P TPM

Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

+3VALW
+5VALW
RK16 FP@ 0_0603_5%
RK17 FP@ 0_0603_5%
UK6 IN OUT GND EN OC
SY6288C20AAC_SOT23-5 FP@
+FP_VCC
FP@ CK12 4.7U_0402_6.3V6M
FP@ CK11 1U_0201_6.3V6M
FP_PWR_EN <36>

<13> USB20_N8 — USB20_N8 — LK2 FPEMC@ — USB20_N8_L
<13> USB20_P8 — USB20_P8 — USB20_P8_L
DLM0NSN900HY2D_4P
SM070005U00
DVT 1/24

DK2 FPEMC@
+FP_VCC
USB20_P8_L
USB20_N8_L
I/O4, I/O2, VDD, GND, I/O3, I/O1
AZC099-04S.R7G_SOT23-6

SP010020S00
CONN@
JXT_FP201H-008G10M
USB20_P8_L
USB20_N8_L
GND GND
JFP1

Update pin define 01/19

PIN	ETU801	SA464K-2200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

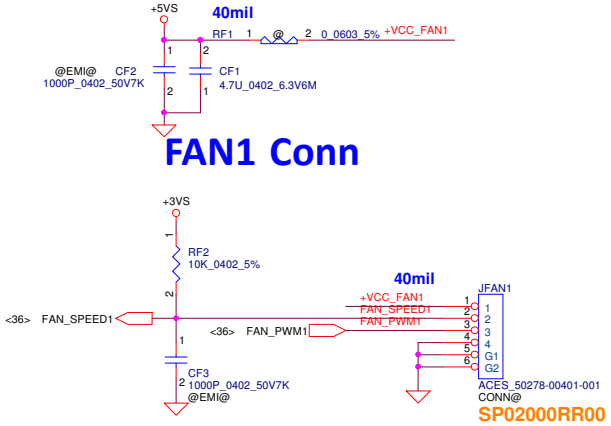
Compal Electronics, Inc.

Title: KB & TP & TPM & LID & FP

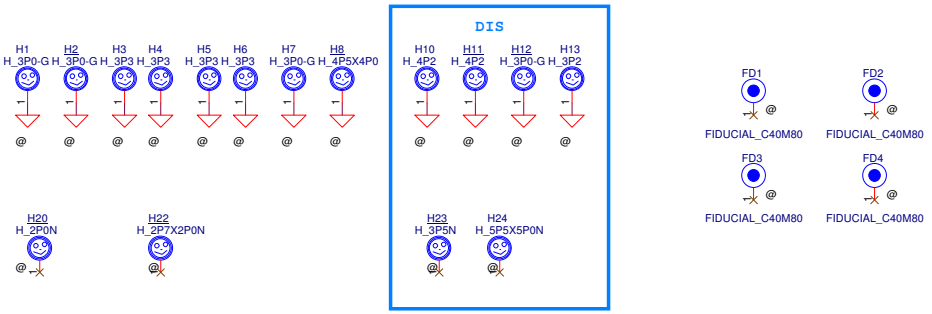
Size: Custom | Document Number: EH7L1 LA-H781P | Rev: 1B

Date: Monday, May 13, 2019 | Sheet 37 of 58

FAN1 Conn

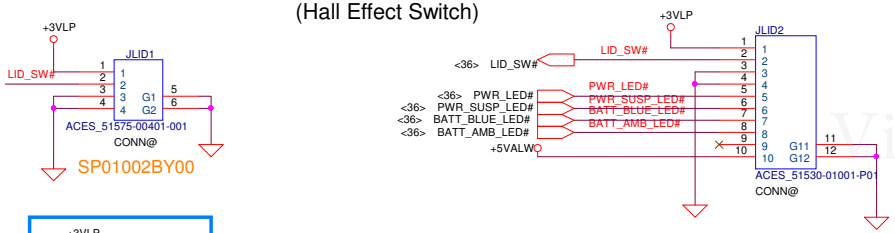


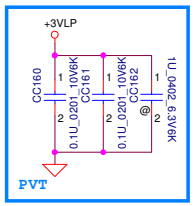
Screw Hole

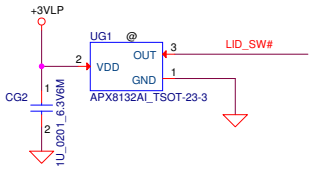


Lid Switch

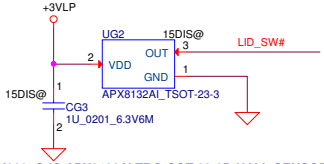
(Hall Effect Switch)



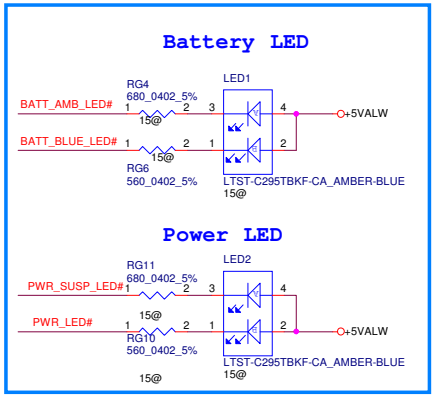




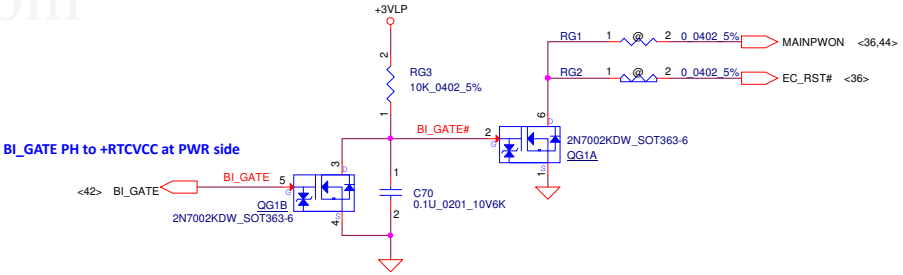
SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR



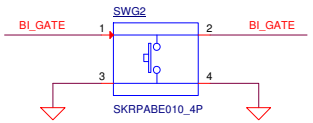
SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR



Reset Circuit



Reset Button



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **FAN &LID& Screw Hole & Reset**

Size	Document Number	Rev
Custom	EH7L1 LA-H781P	1B

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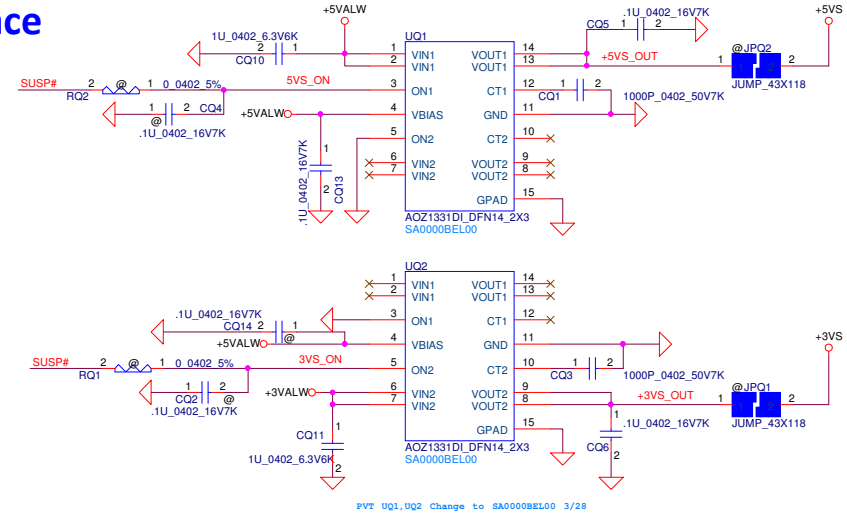
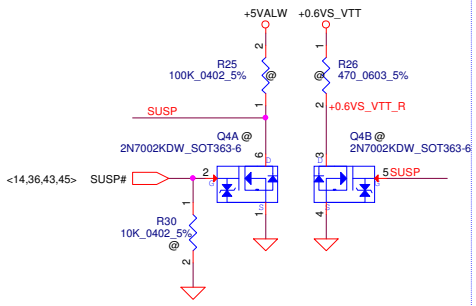
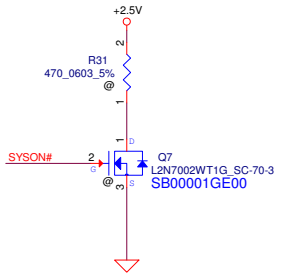
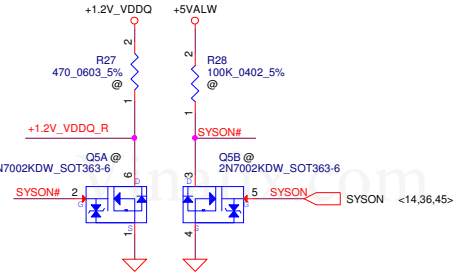
DC Interface

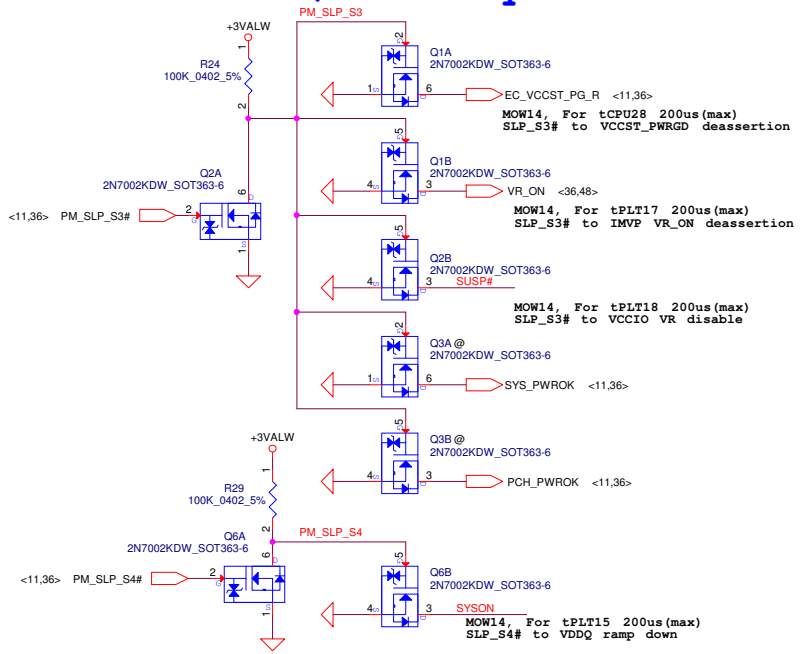


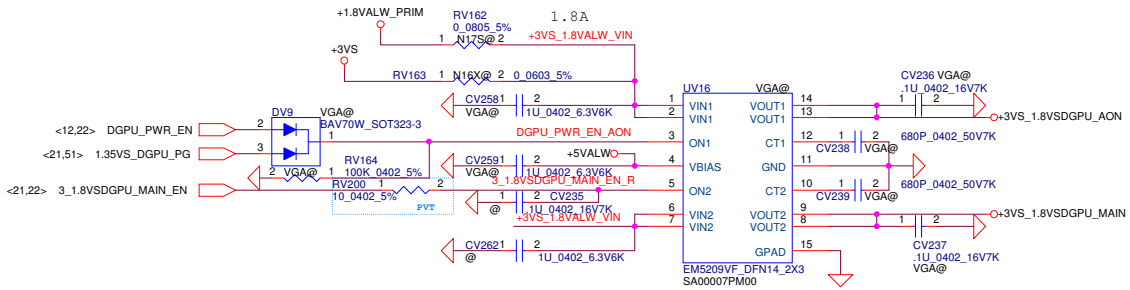


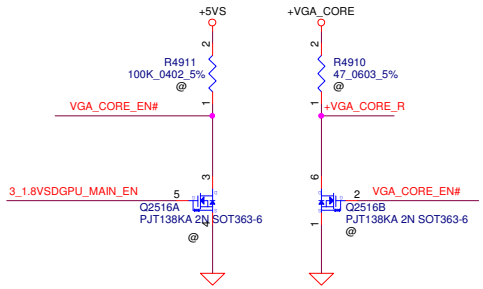




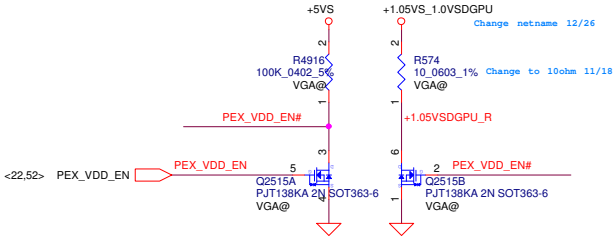
For Power ON/Off Sequence

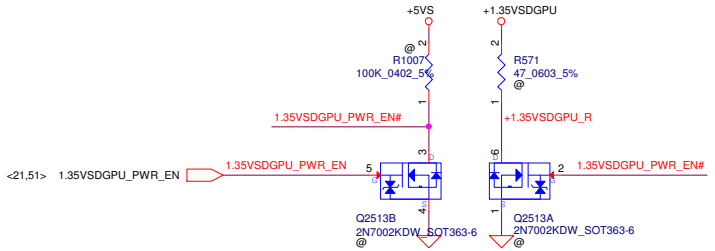






+3VS to +3VSDGPU_AON for GPU





Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **DC Interface**

Size	Document Number	Rev
Custom	EH7L1 LA-H781P	1B

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Kabylake_U22 CPU Part Number

HDCP2.2

UC1 SR343@
CPU_KBL_H0_i3-7100U_2.4G
SA0000A38M0

UC1 SR343BR@
CPU_KBL_H0_i3-7100U_2.4G
SA0000A38O0

UC1 SR342@
CPU_KBL_H0_i5-7200U_2.5G
SA0000A37N0

UC1 SR342BR@
CPU_KBL_H0_i5-7200U_2.5G
SA0000A37O0

UC1 SR341@
CPU_KBL_H0_i7-7500U_2.7G
SA0000A34L0

UC1 SR341BR@
CPU_KBL_H0_i7-7500U_2.7G
SA0000A34M0

UC1 SR3JY@
CPU_KBL_H0_i3-7130U_2.7G
SA0000B2Y70

UC1 QNZU@
CPU_KBL_H0_i3-7020U_2.3G QS
SA0000BLH20

UC1 SR3TK@
CPU_KBL_H0_i3-7020U_2.3G
SA0000BLH60

Kabylake_R U42 CPU Part Number

UC1 SR3LA@
CPU_KBL_Y0_U42_I5-8250U_1.6G
SA0000AWB40

UC1 SR3LABR@
CPU_KBL_Y0_U42_I5-8250U_1.6G
SA0000AWB90

UC1 SR3LC@
CPU_KBL_Y0_U42_I7-8550U_1.8G
SA0000AWC40

UC1 SR3LCBR@
CPU_KBL_Y0_U42_I7-8550U_1.8G
SA0000AWC70

Kabylake_RU22 CPU Part Number

UC1 SR3W0@
CPU_KBL_Y0_RU22_I3-8130U_2.2G
SA0000BKN60

UC1 SR3W0BR@
CPU_KBL_Y0_RU22_I3-8130U_2.2G
SA0000BKN70

UC1 SR3LD@
CPU_KBL_Y0_RU22_I3-7020U_2.3G
SA0000BLD70

Kabylake_U23E Fuse Down CPU

UC1 SR3N6@
CPU_KBL_J1_i3-7020U_2.3G
SA0000BVB10

UC1 QNMU@
CPU_KBL_J1_i3-7020U_2.3G QS
SA0000BVB00

PCB Number

ZZZ PCB@
PCB 2MD LA-H781P REV0 MB 4
DA600260010

ZZZ DAZ10@
PCB EH7L1 LA-H781P LS-H781P/H782P/H783P/H784P
DAZ2MD00100

ZZZ DAZ1A@
PCB EH7L1 LA-H781P LS-H781P/H782P/H783P
DAZ2MD00101

ZZZ1 DAZ1B@
PCB EH7L1 LA-H781P LS-H781P/H802P/H783P
DAZ2MD00301

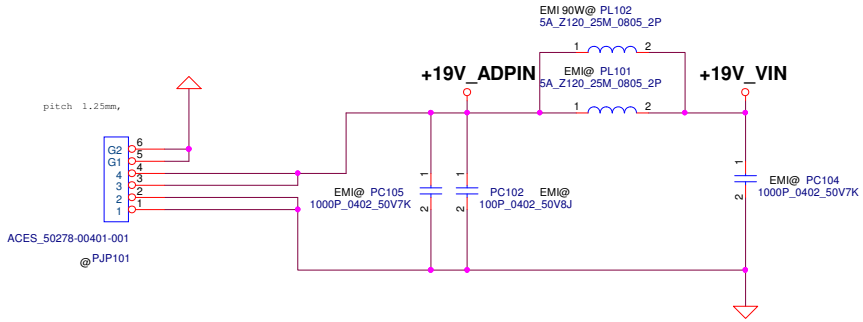
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

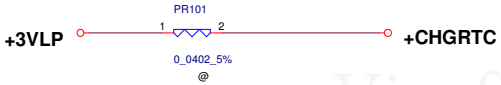
Compal Electronics, Inc.

Title: CPU/X76 BOM

Size: Custom | Document Number: CPU/X76 BOM | Rev: 1B

Date: Monday, May 13, 2019 | Sheet 40 of 58





Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

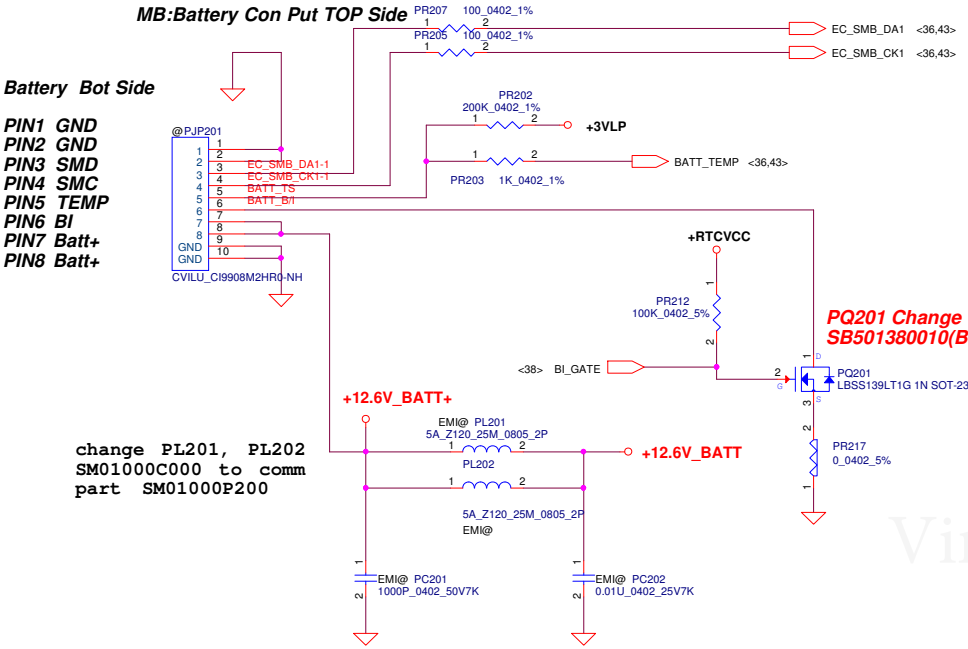
Compal Electronics, Inc.

Title: **PWR DCIN / Pre-charge**

Size: Custom | Document Number: **EH5AW M/B LA-G521P** | Rev: 1B

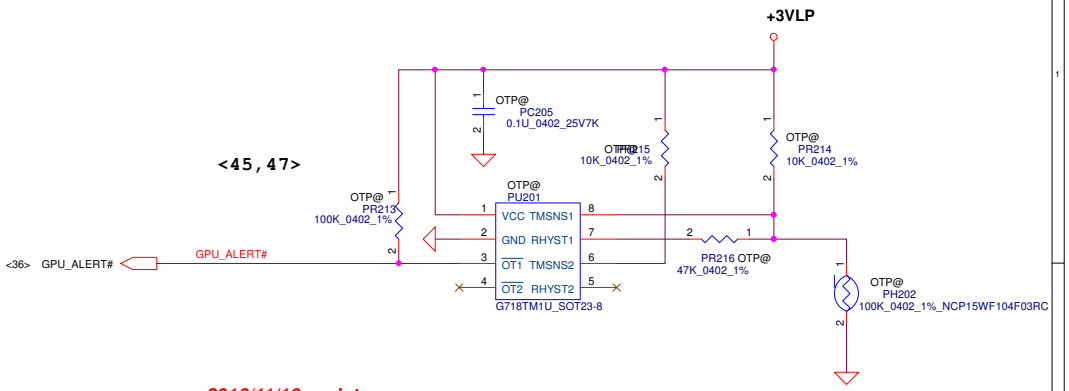
Date: Monday, May 13, 2019 | Sheet 41 of 58

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200



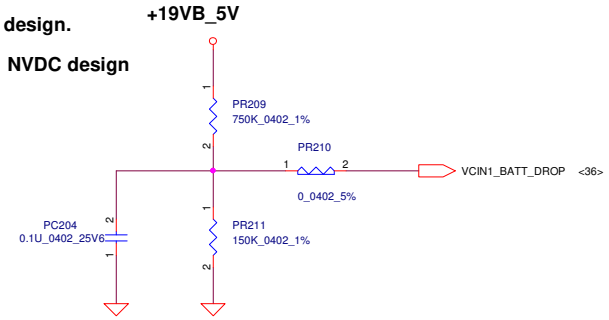
2016/11/16 update

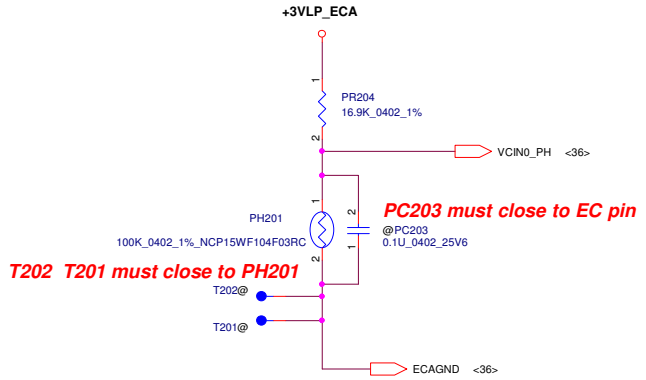
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm	58.5W,0.61V	Active=recovery
65W PR206 19.1K ohm	84.5W,0.61V	Active=recovery
90W PR206 30.1K ohm	117W,0.61V	Active=recovery
PH1	2V	1V

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

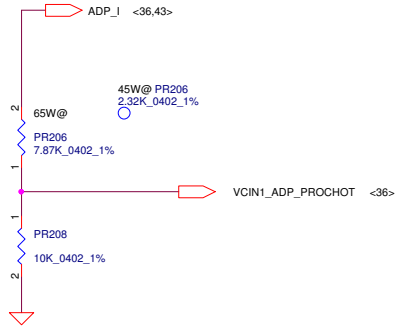
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





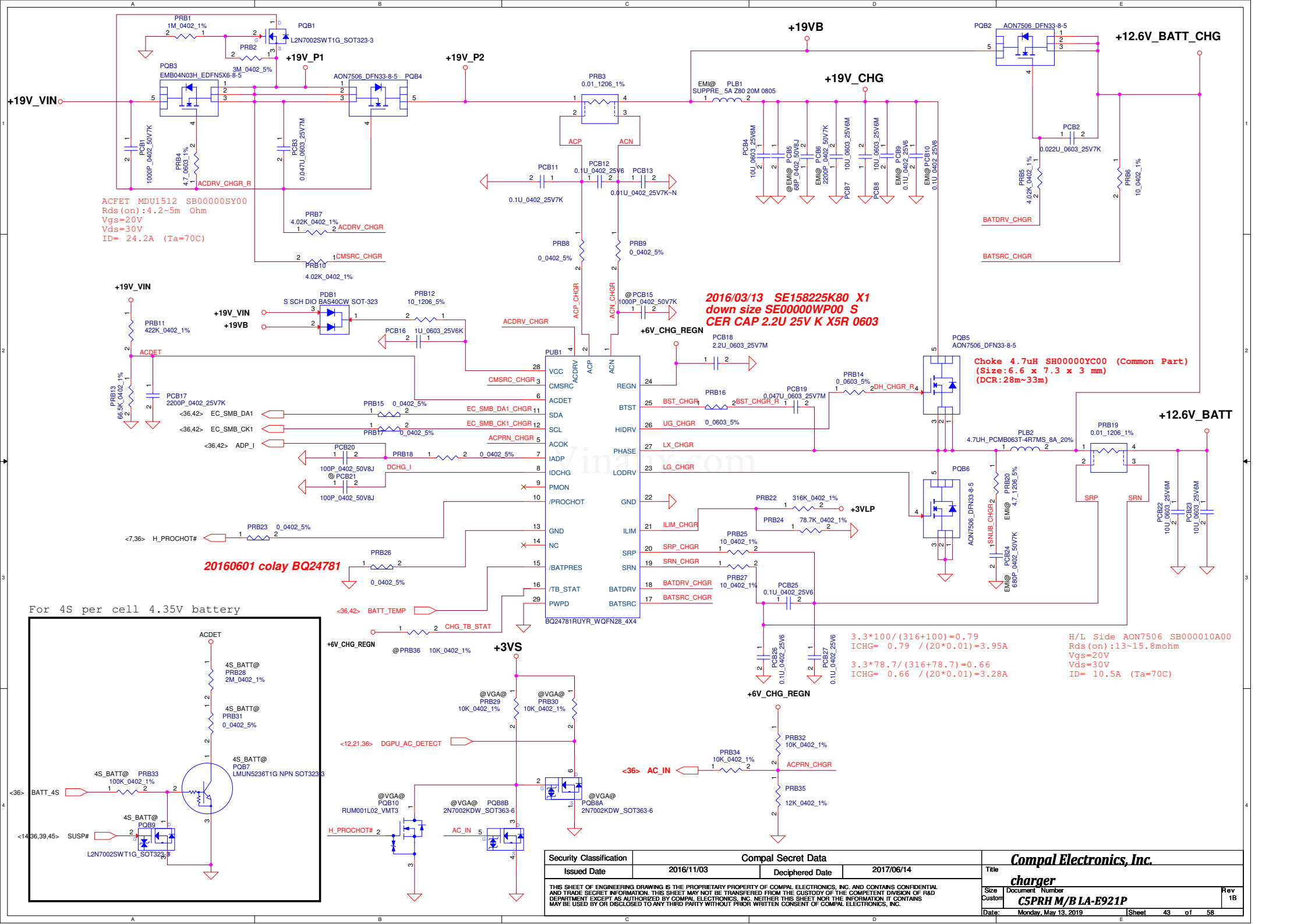
PC203 must close to EC pin

T202 T201 must close to PH201



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size Custom	Document Number EH5AW M/B LA-G521P		Rev 1B
Date: Monday, May 13, 2019	Sheet 42 of 58		


+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+12.6V_BATT_CHG
+12.6V_BATT
ACFET MDU1512 SB00000SY00
Rds(on):4.2~5m Ohm
Vgs=20V
Vds=30V
ID= 24.2A (Ta=70C)
2016/03/13 SE158225K80 X1
down size SE00000WP00 S
CER CAP 2.2U 25V K X5R 0603
Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)
20160601 colay BQ24781
For 4S per cell 4.35V battery
+6V_CHG_REGN
+3VS
+3VLP
BQ24781RUYR_WQFN28_4X4
3.3*100/(316+100)=0.79
ICHG= 0.79 /(20*0.01)=3.95A
3.3*78.7/(316+78.7)=0.66
ICHG= 0.66 /(20*0.01)=3.28A
H/L Side AON7506 SB000010A00
Rds(on):13~15.8mohm
Vgs=20V
Vds=30V
ID= 10.5A (Ta=70C)
Compal Electronics, Inc.
charger
C5PRH M/B LA-E921P
Compal Secret Data
2016/11/03
2017/06/14
Monday, May 13, 2019
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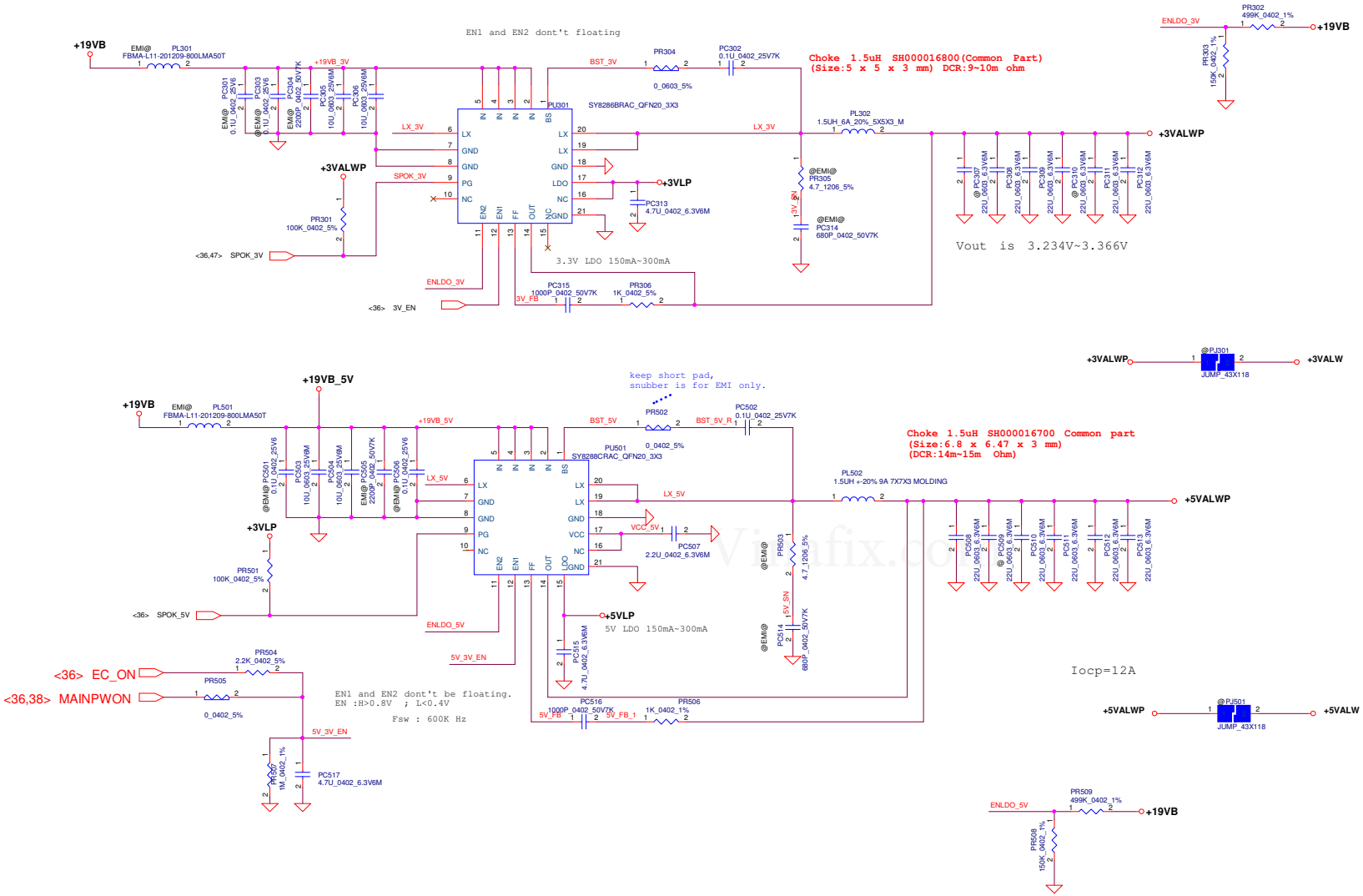

Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2019/11/15

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1B

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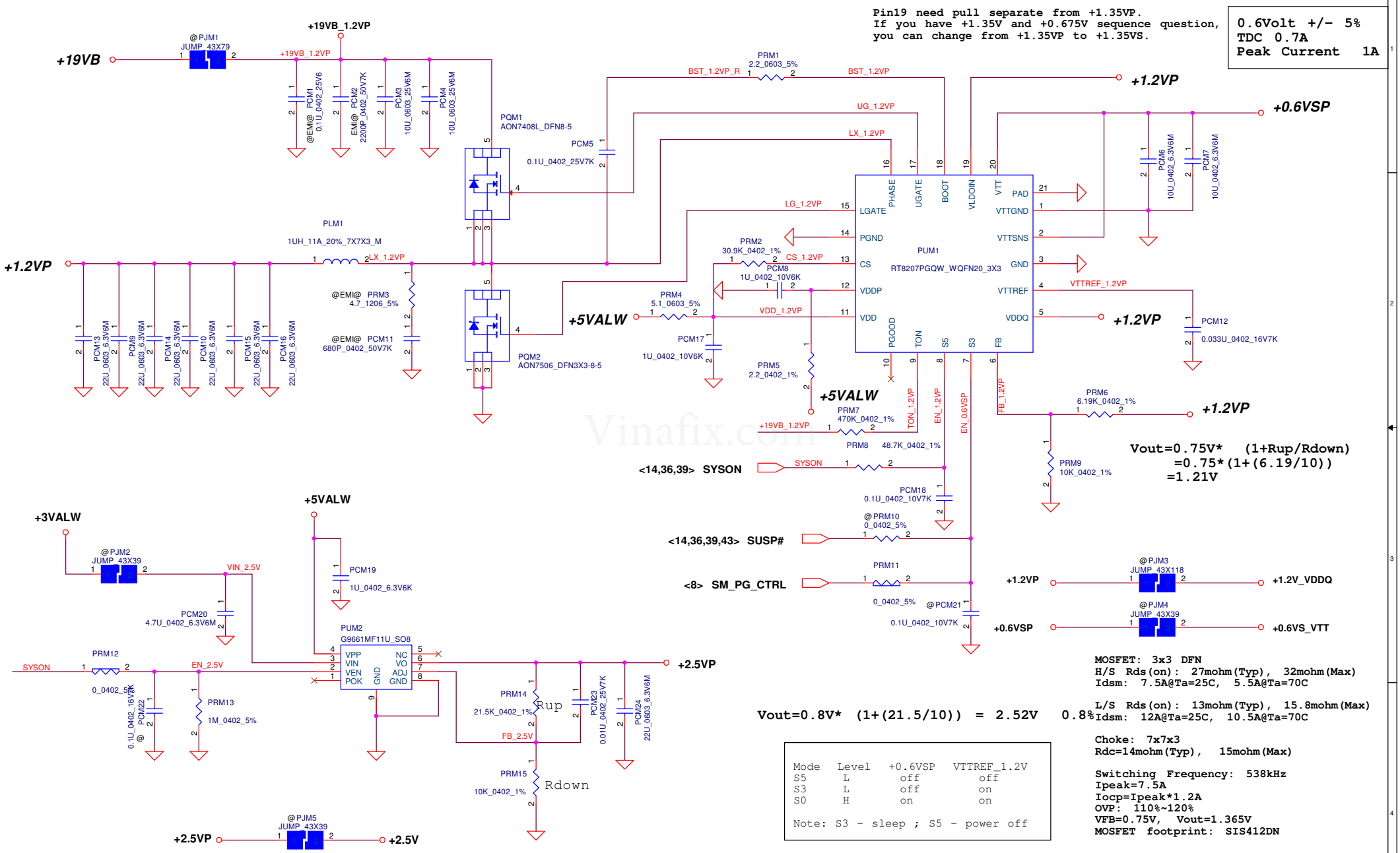

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1B

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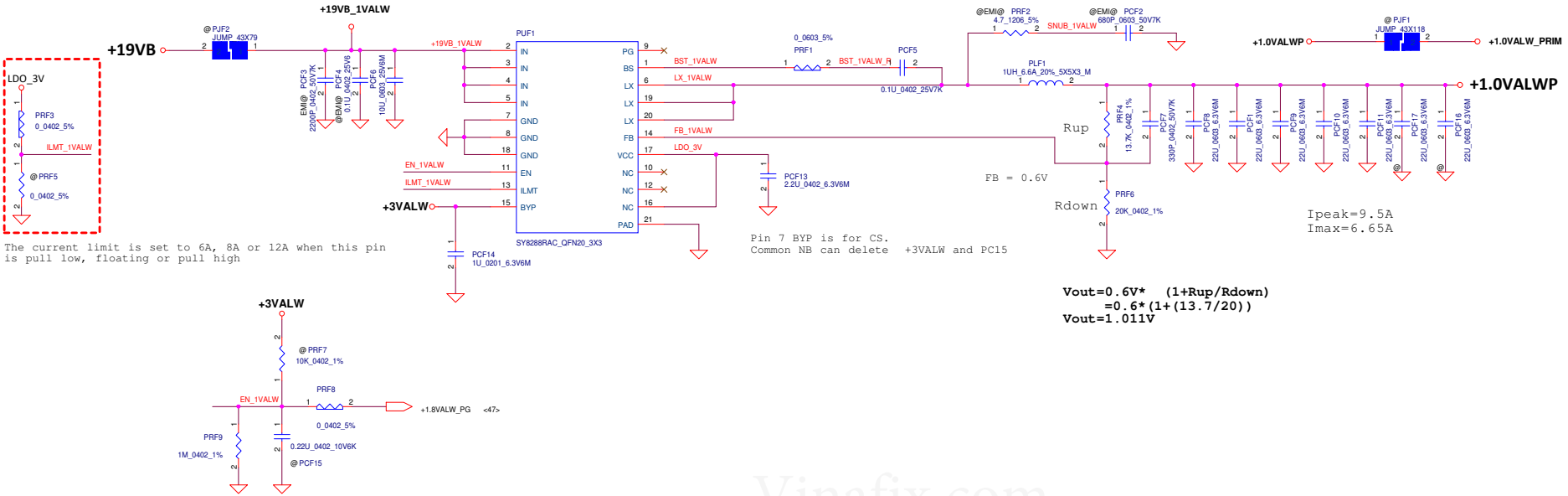
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	1B

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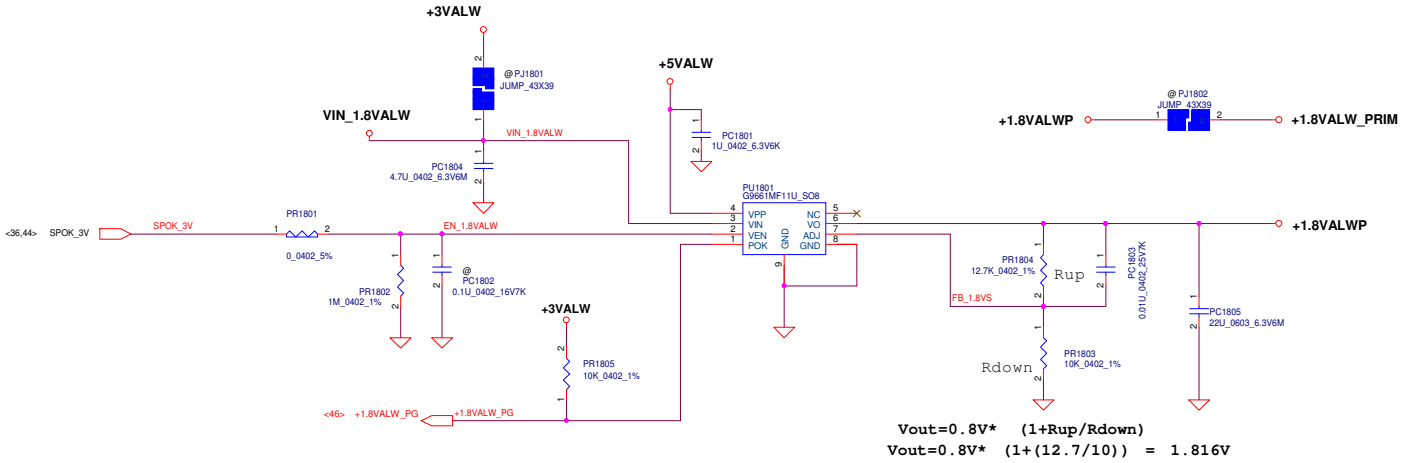

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	1B

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Module model information

RT3602AE_U22_RU42_colay_V1A.mdd for IC portion

RT3602AE_U22_RU42_colay_V1B.mdd for SW portion

PRZ1 and PRZ22 are for debug only.
VCCSSA_SENSE and VSSSA_SENSE need other resistor at HW side.

PRZ41 and PRZ21 are for debug only.
VCCCORE_SENSE and VSSCORE_SENSE need other resistor at HW side.

	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

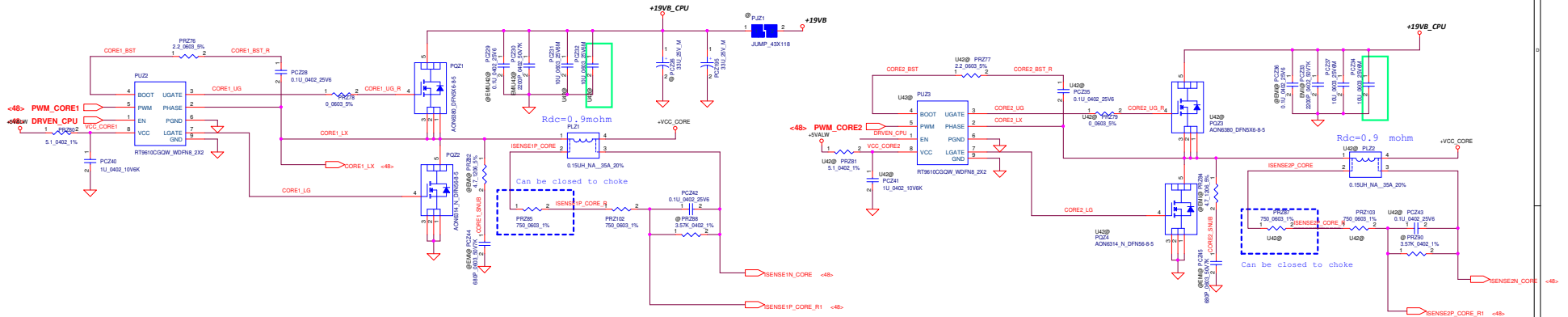
Set DRVEN output function at PS4. Set to 5V DRVEN is floating, and set to GND DRVEN is low at PS4.

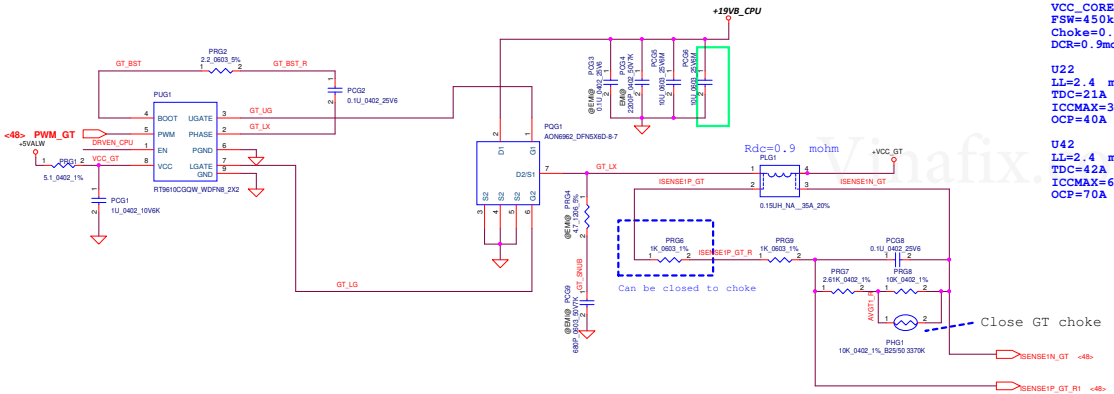
PRZ59 and PRZ60 are for debug only.
VCCGT_SENSE and VSSGT_SENSE need other resistor at HW side.

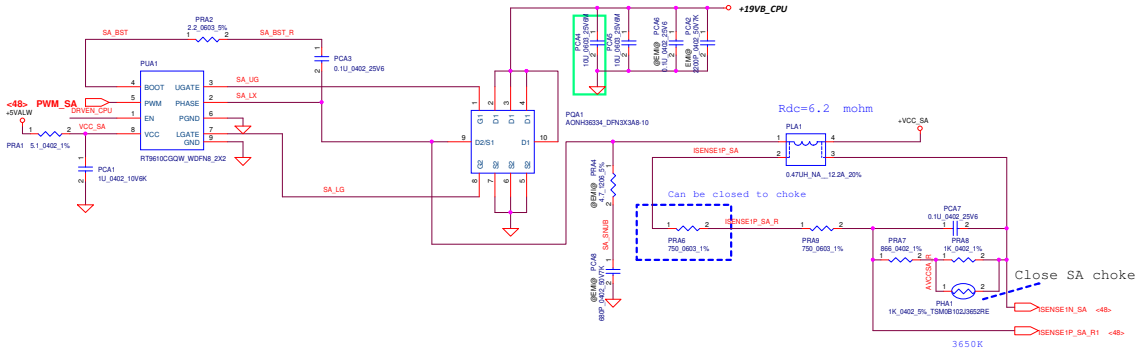
EN
High: > 0.7V
Low: < 0.3V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date	2019/09/01

Title	CPU_CORE		
Size	Document Number		Rev
	EH5AW M/B LA-G521P		1B
Date:	Monday, May 13, 2019	Sheet 48 of 58	







VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

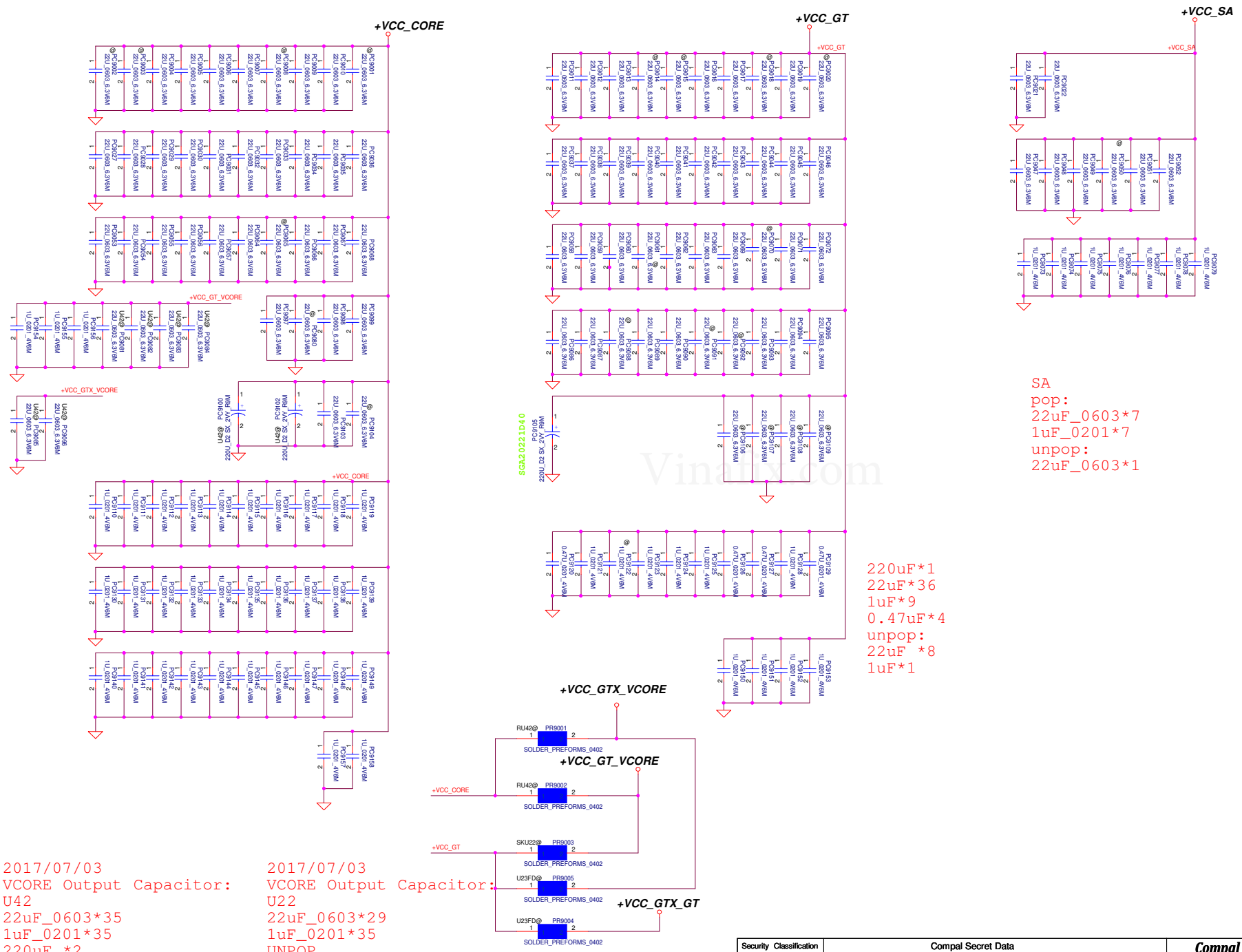
U42
LL=3.1 mohm
TDC=12A
ICCMAX=31A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=6A
OCP=9.5A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date 2019/09/01	Title: CPU Power stage
			Size: Document Number: EH5AW M/B LA-G521P Rev: 1B
			Date: Monday, May 13, 2019 Sheet 49 of 58



Security Classification	Compal Secret Data		
Issued Date	2018/10/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title: Power Train			
Size: C	Document Number: EH5AW M/B LA-G521P		Rev: 1B
Date: Monday, May 13, 2019	Sheet 50 of 58		

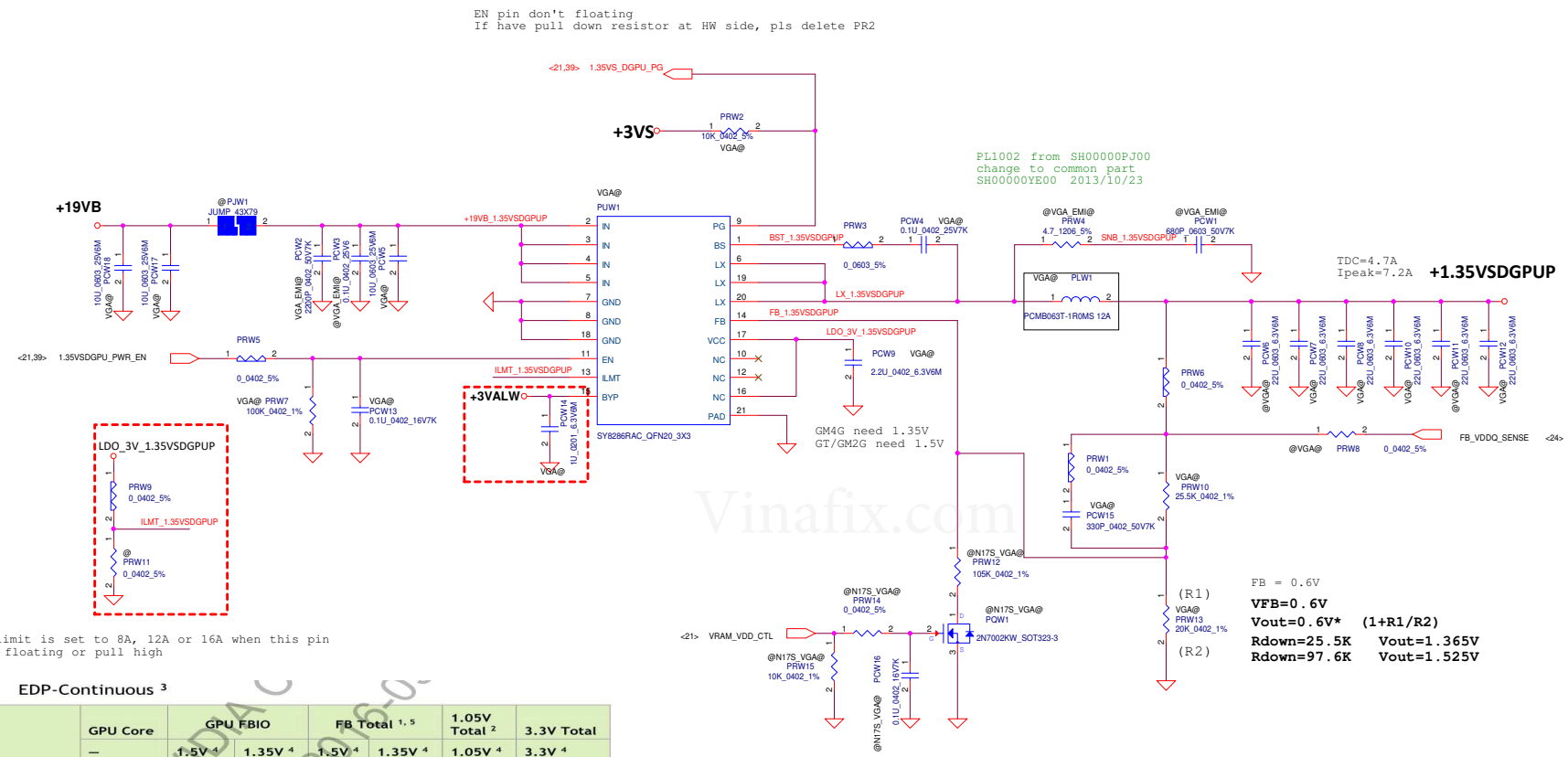


Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9		6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6		9.5	2.9

Table 7. Output EDP-Continuous

Product	NVVDD	GPU FBIO	FB Total[5]	1.0V Total[1]	1.8V Total[2]
	—	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	—	1.35V[3]	1.35V[3]	1.0V[3]
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	Power Train
Size C	Document Number EH5AW M/B LA-G521P
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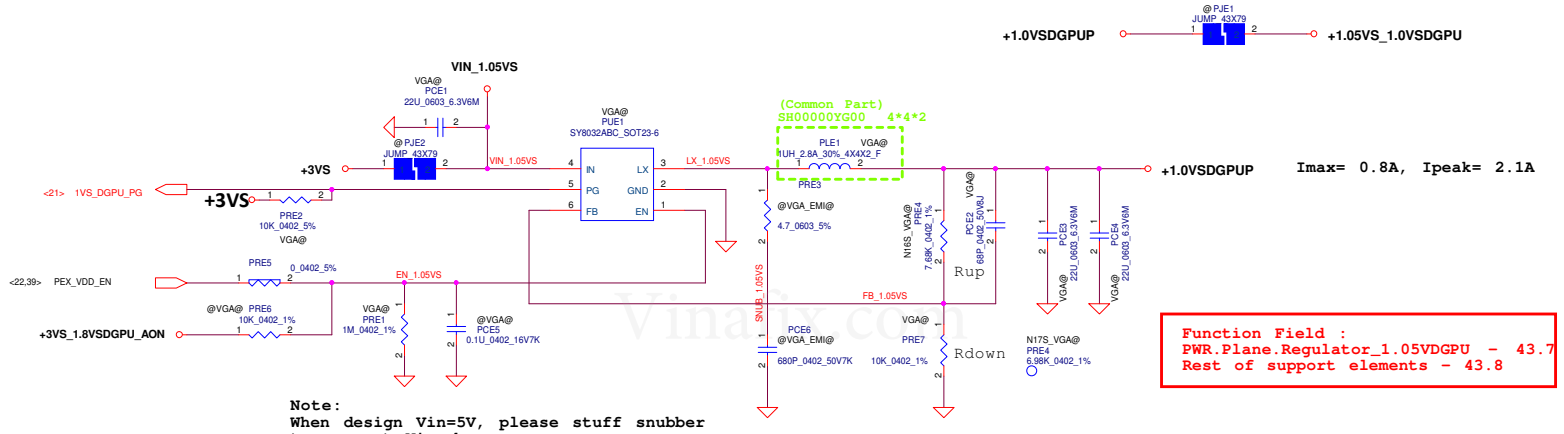
Module model information

SY8032_V2.mdd



Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
N16=>1.05V
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.32/10)=1.039 (-1%)

N17=>1.0V
Vout=0.6V*(1+(6.98/10)=1.019V (1.02%)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Power Train

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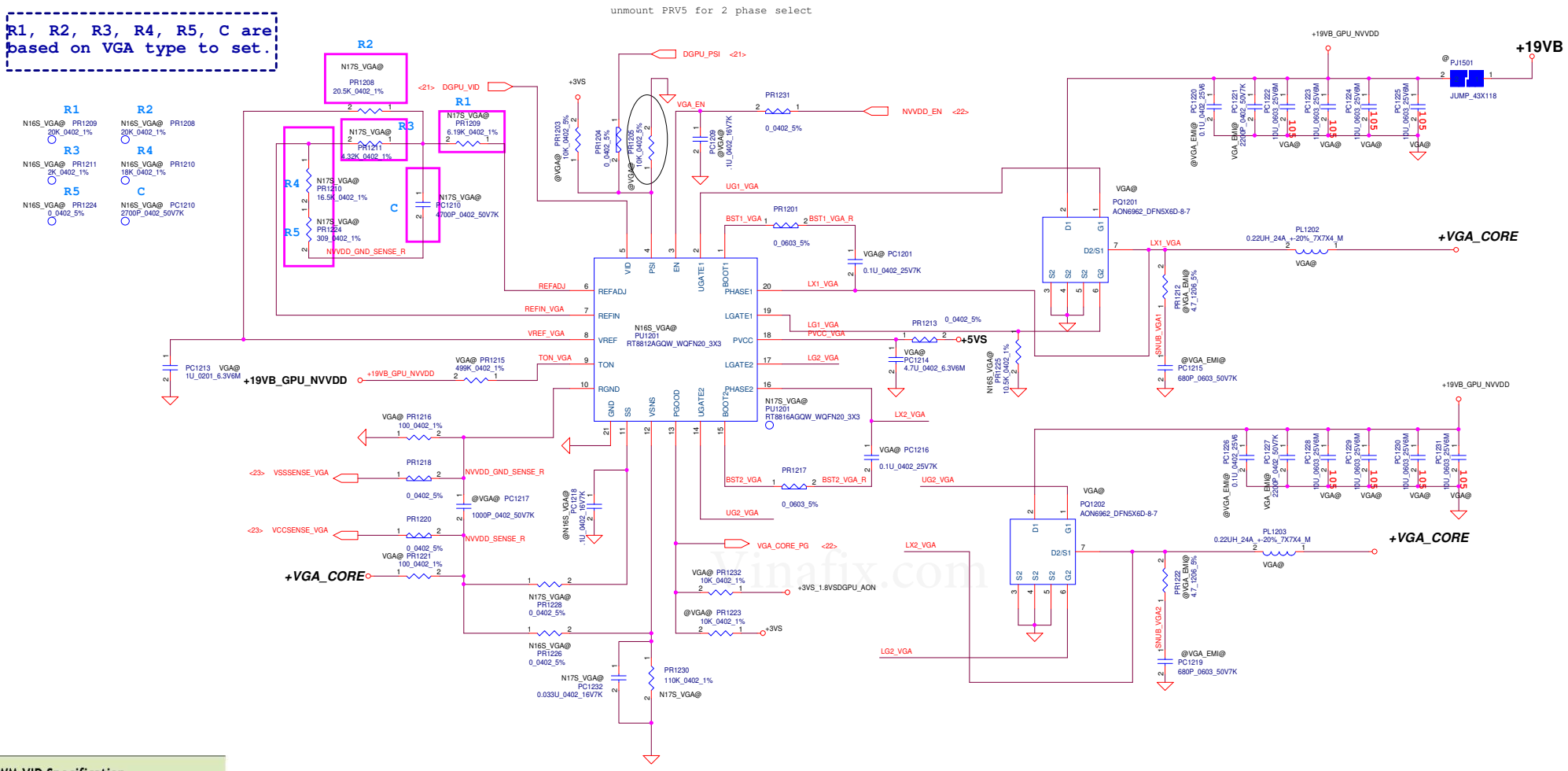
R1, R2, R3, R4, R5, C are based on VGA type to set.



PWM-VID Specification		
		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F_{PWM}	MHz	1.125
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core – (A)
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification	Compal Secret Data		
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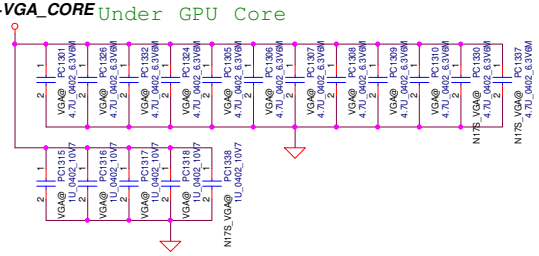
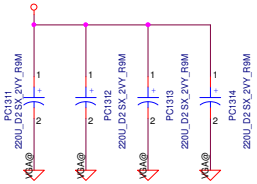
GB4-128 package

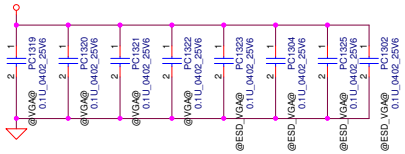
+VGA_CORE Under GPU Core



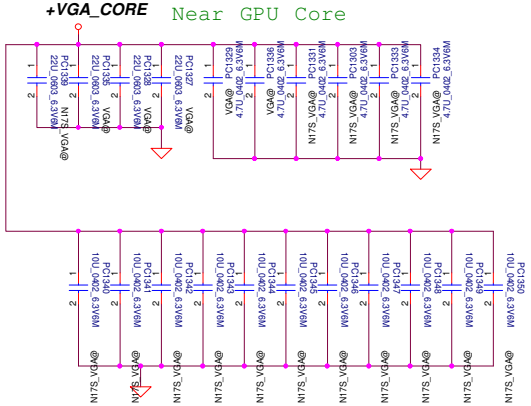
+VGA_CORE



+VGA_CORE



+VGA_CORE Near GPU Core



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	1B

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