MS-7D17

uATX

Ver: 12

Intel -RKL-S plamform

CPU:

Comet lake S 65W

PWM:

IMVP8 -RAA229001

Onboard Chip:

HD Audio Codec:ALC897
LAN- RTL8125B
SIO:NTC6687
Flash ROM: SPI 128 MB X1

System Chipset:

B560

Display Output:

HDMI Port

DP Port

Main Memory:

DDRIV (2933MHz) * 4 (Dual Channel)

ACPI:

LDO

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 1
M.2 Slot * 2

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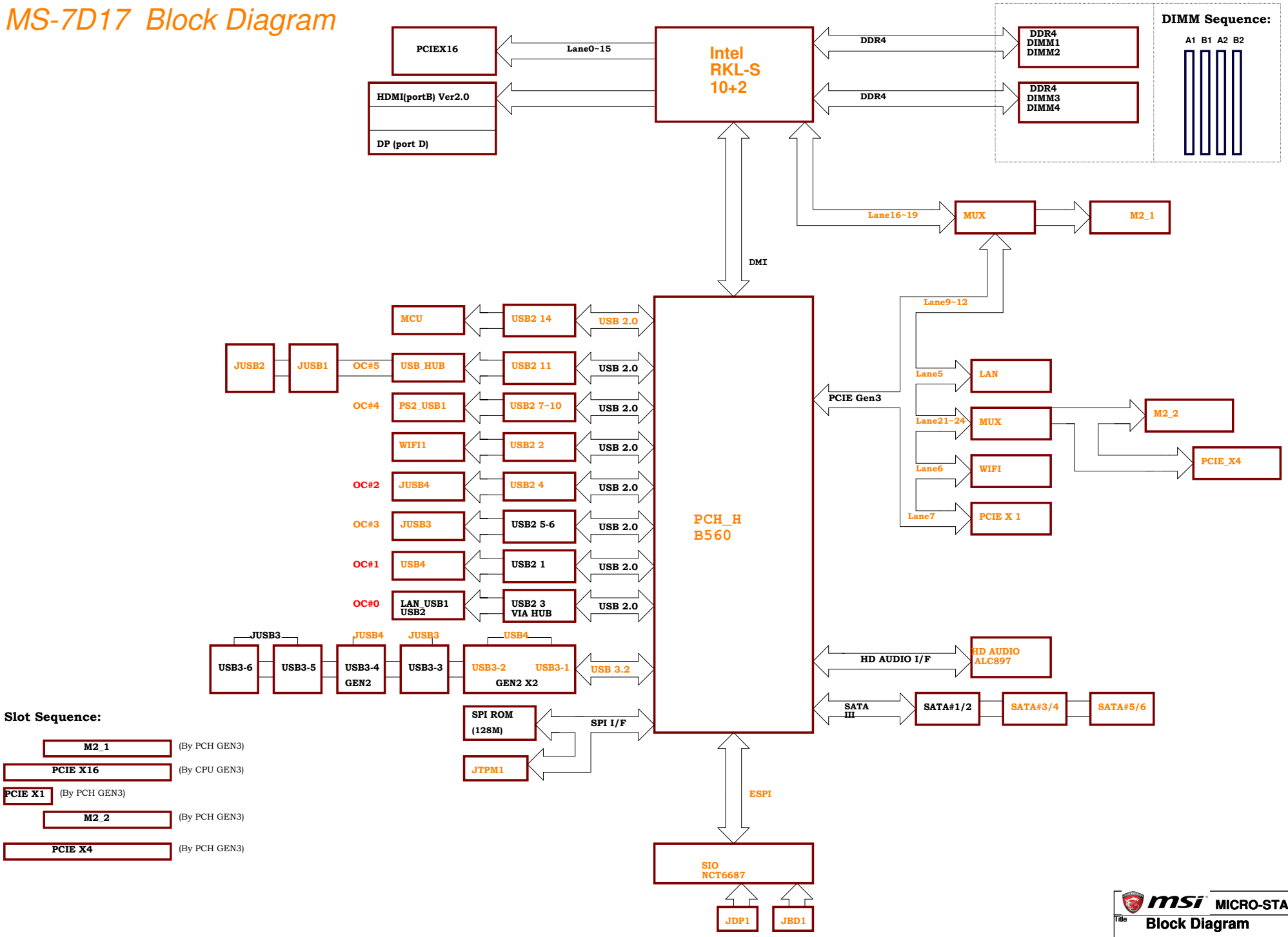
Title: Cover Sheet

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 1 of 73

MS-7D17 Block Diagram



Slot Sequence:

M2_1	(By PCH GEN3)
PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN3)
M2_2	(By PCH GEN3)
PCIE X4	(By PCH GEN3)

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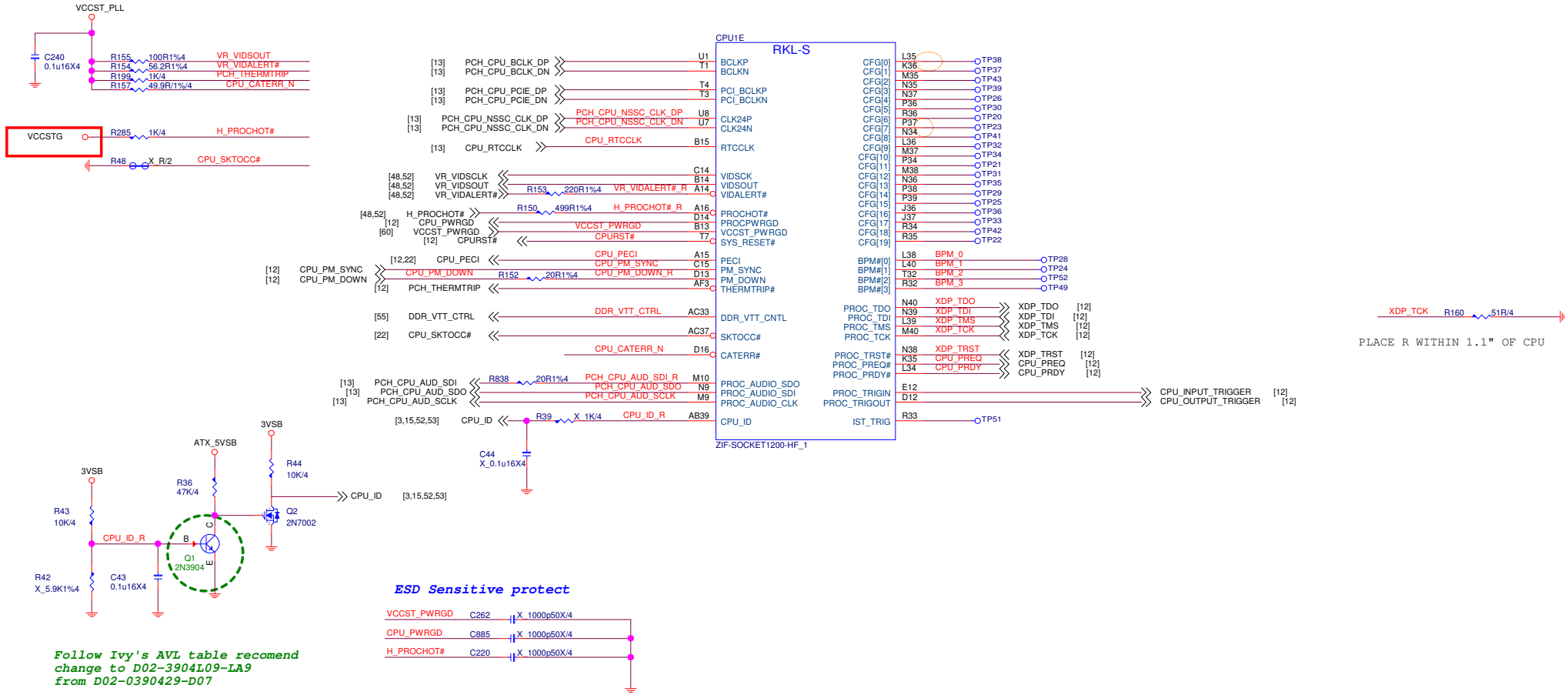
Title: Block Diagram

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 2 of 73



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No stall	Stall	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

CFG5 CFG6

ENABLE#		SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

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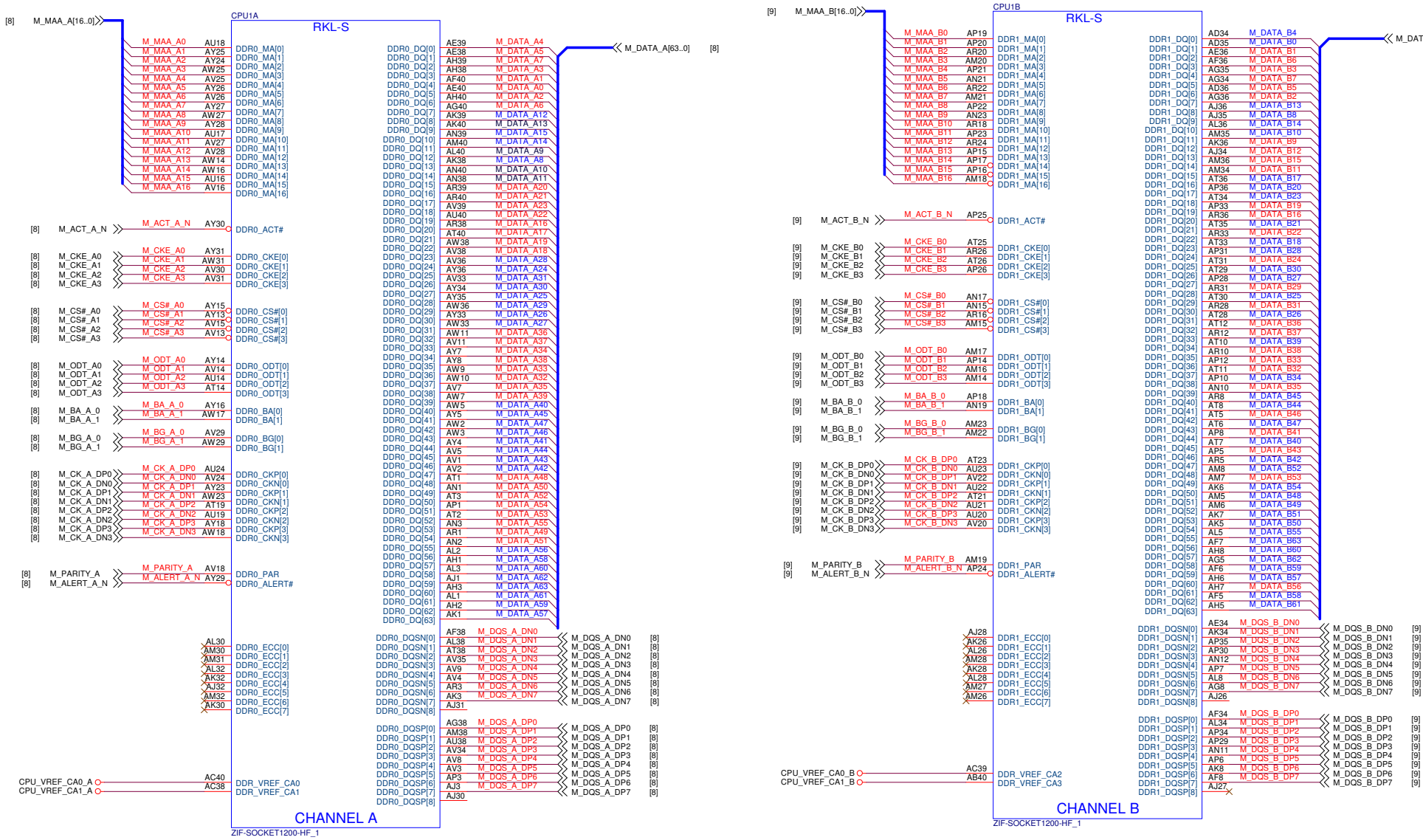
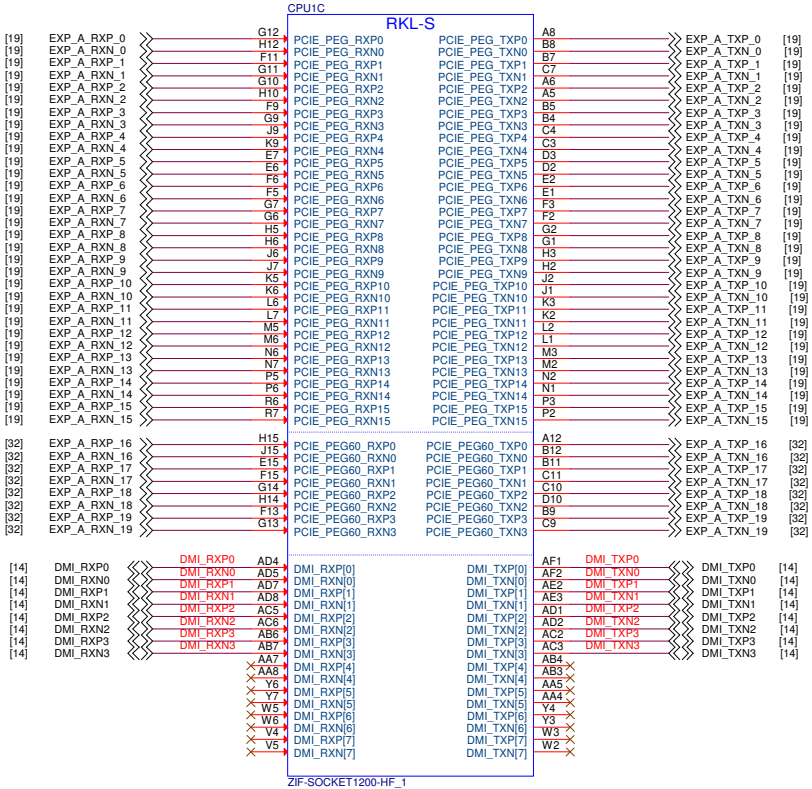
Title: CPU-Control/MISC/CFG

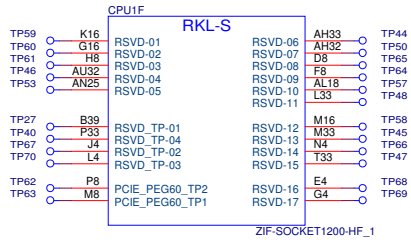
Size | Document Number: MS-7D17 | Rev: 12

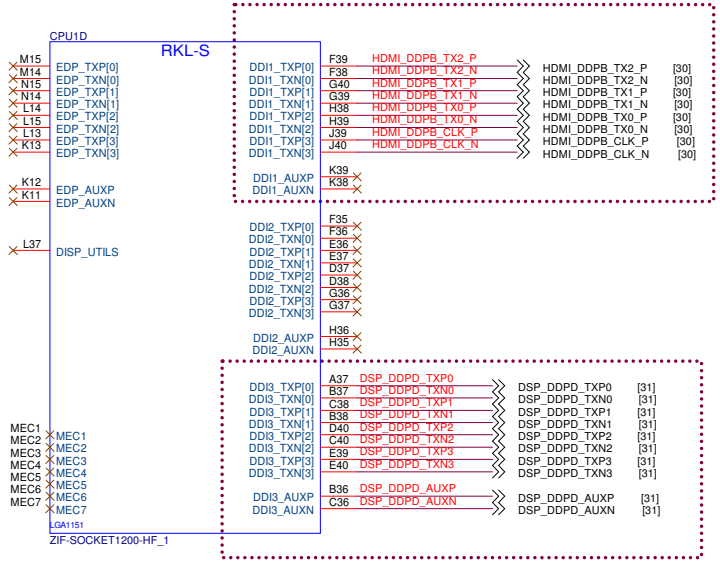
Date: Monday, March 15, 2021 | Sheet 3 of 73



MICRO-STAR INT'L CO.,LTD.		
Title	CPU-Memory	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 4 of 73	





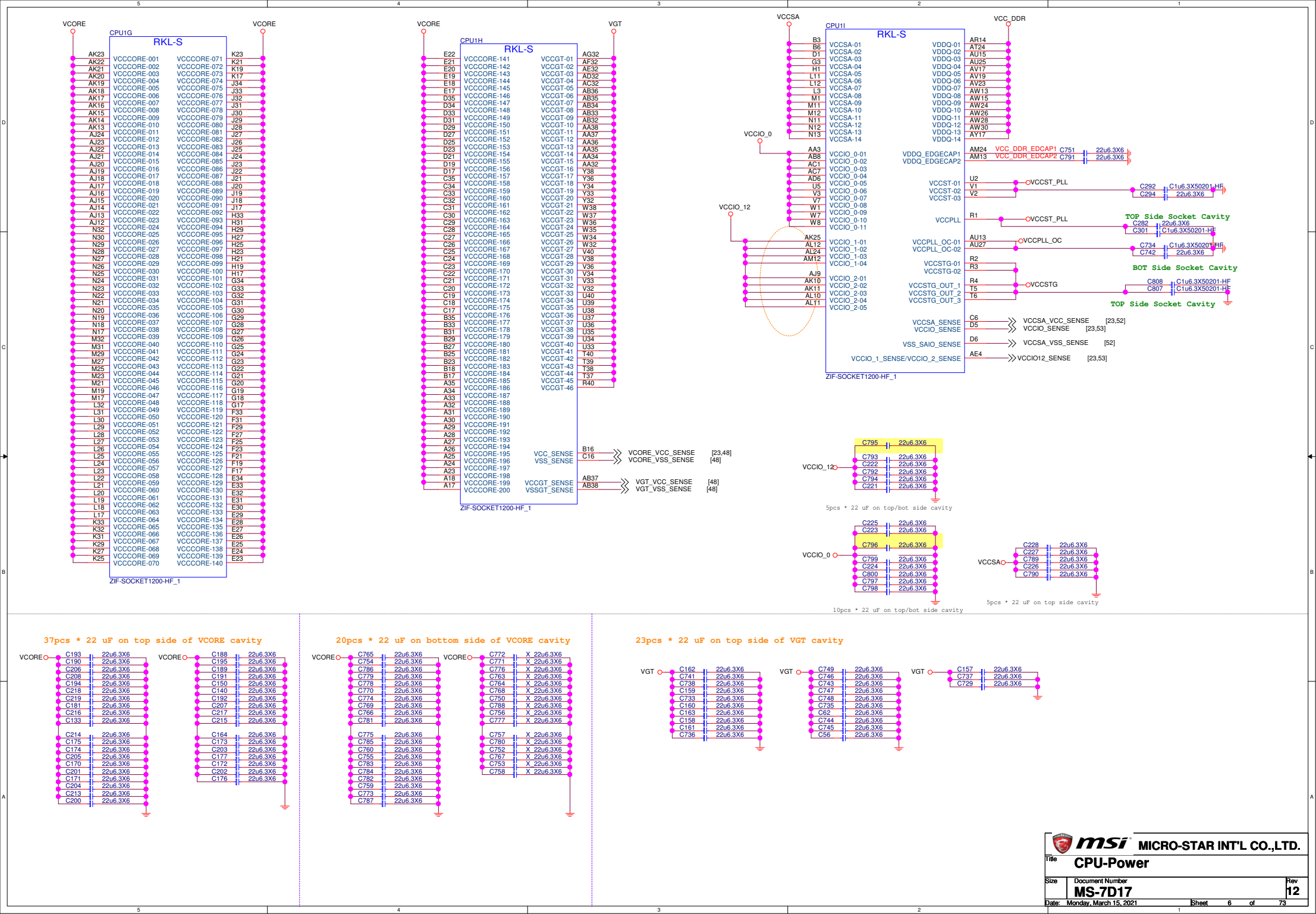


MICRO-STAR INT'L CO.,LTD.

Title: CPU-PEG/Display/RSD

Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 5 of 73

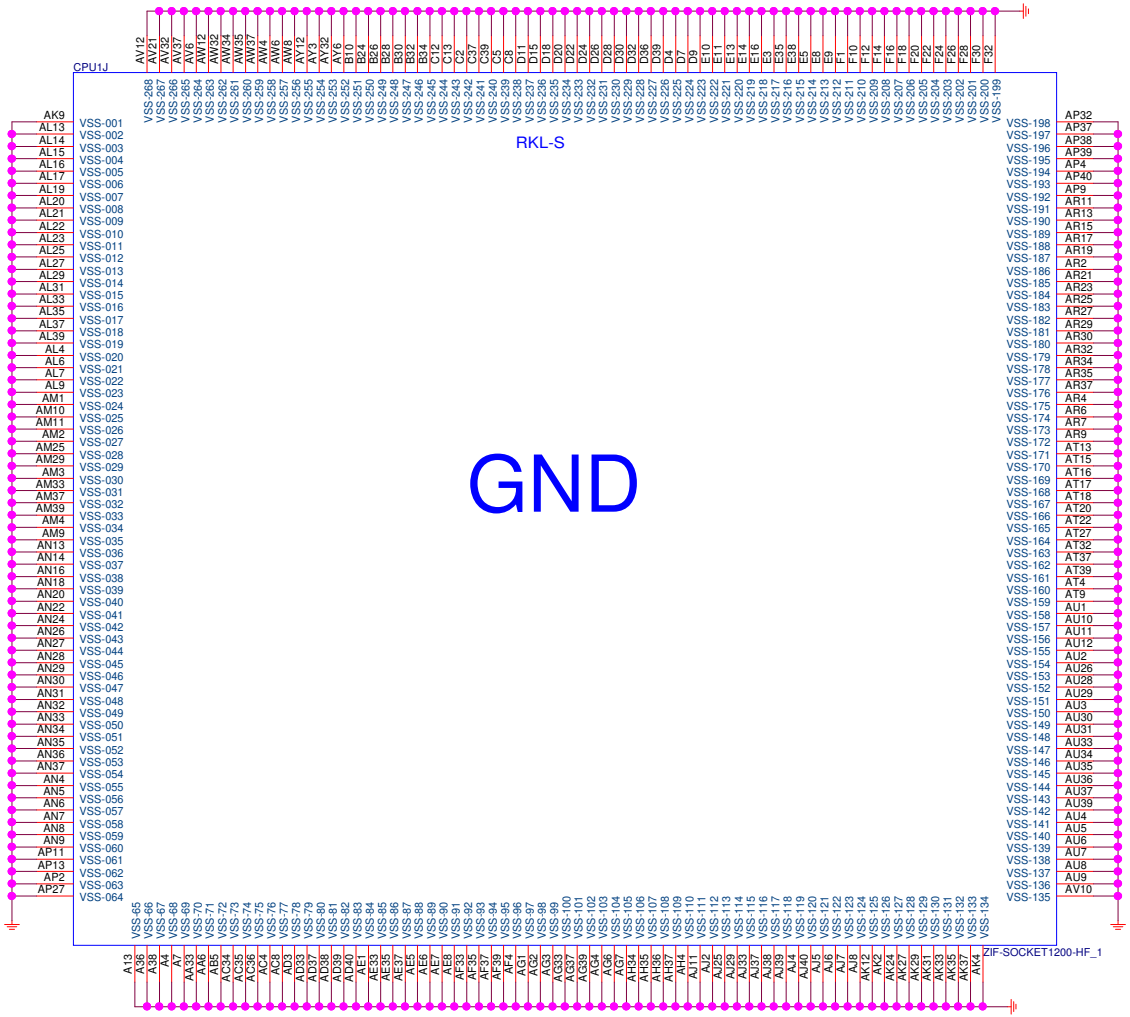


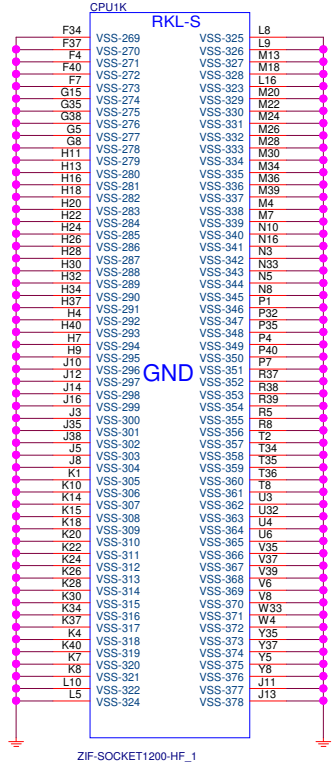
MICRO-STAR INT'L CO.,LTD.

Title: CPU-Power

Size: Document Number: MS-7D17 Rev: 12

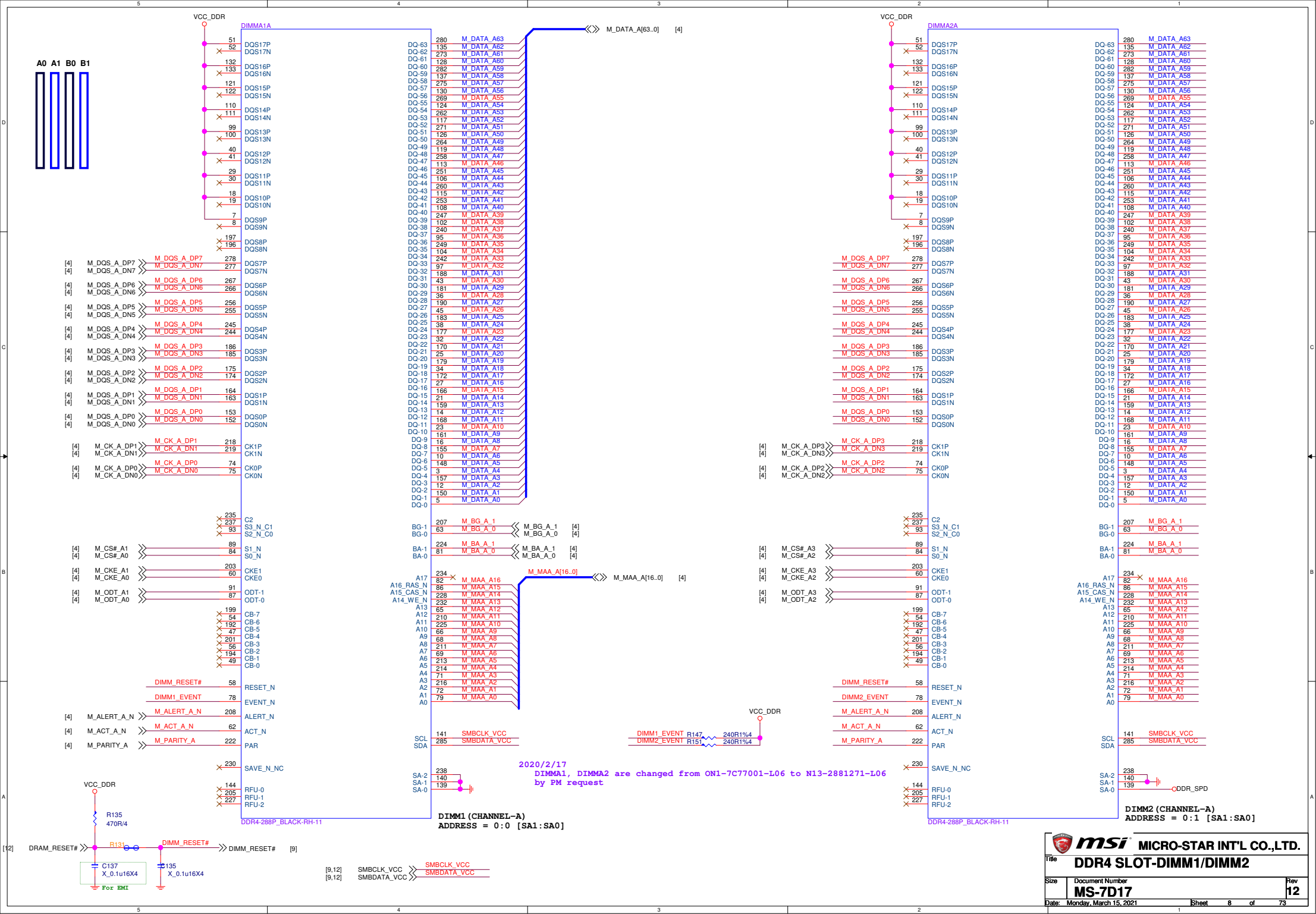
Date: Monday, March 15, 2021 Sheet 6 of 73





MICRO-STAR INT'L CO.,LTD.

Title	CPU-GND	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 7 of 73	

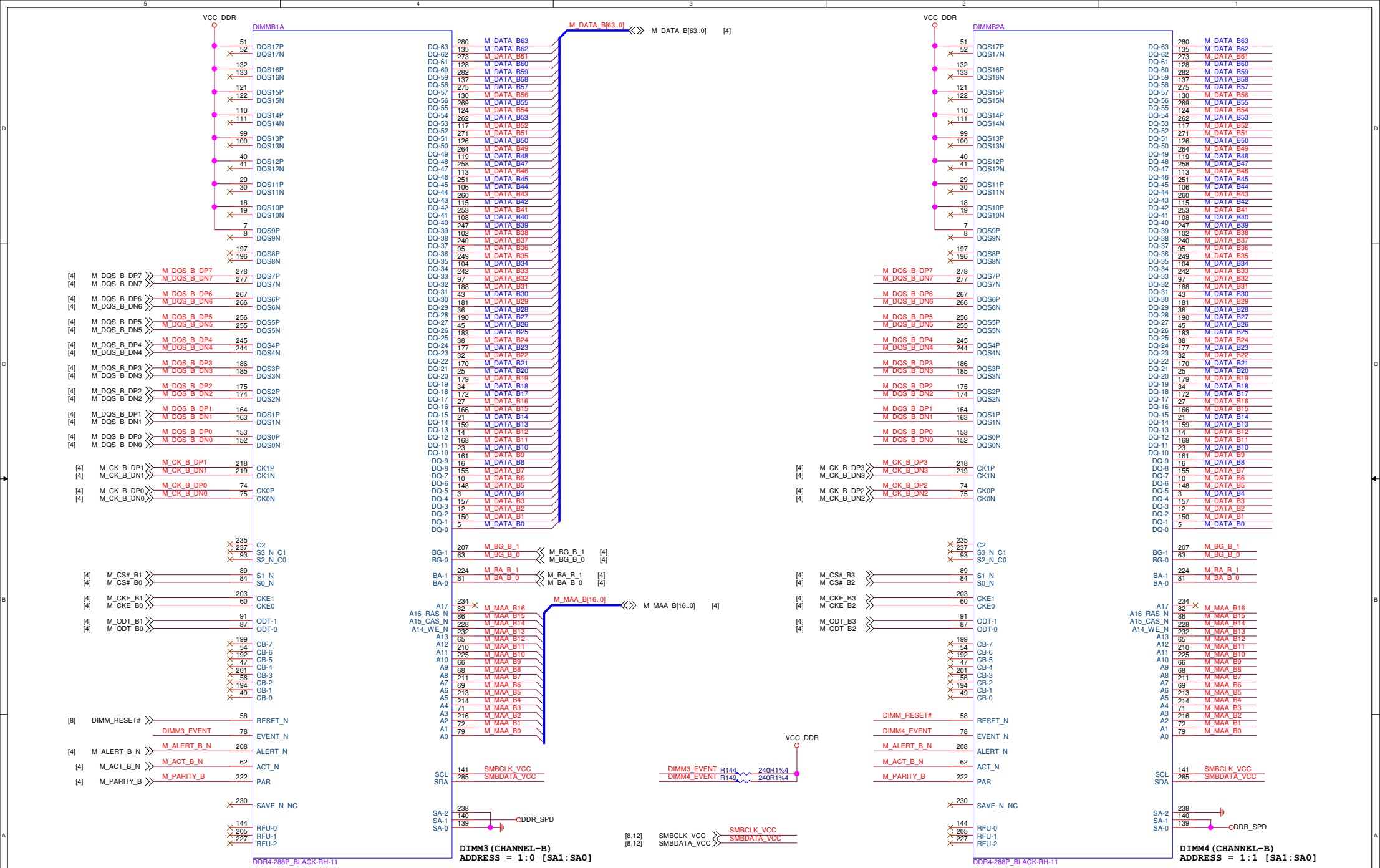


MICRO-STAR INT'L CO.,LTD.

Title: DDR4 SLOT-DIMM1/DIMM2

Size: | Document Number: MS-7D17 | Rev: 12

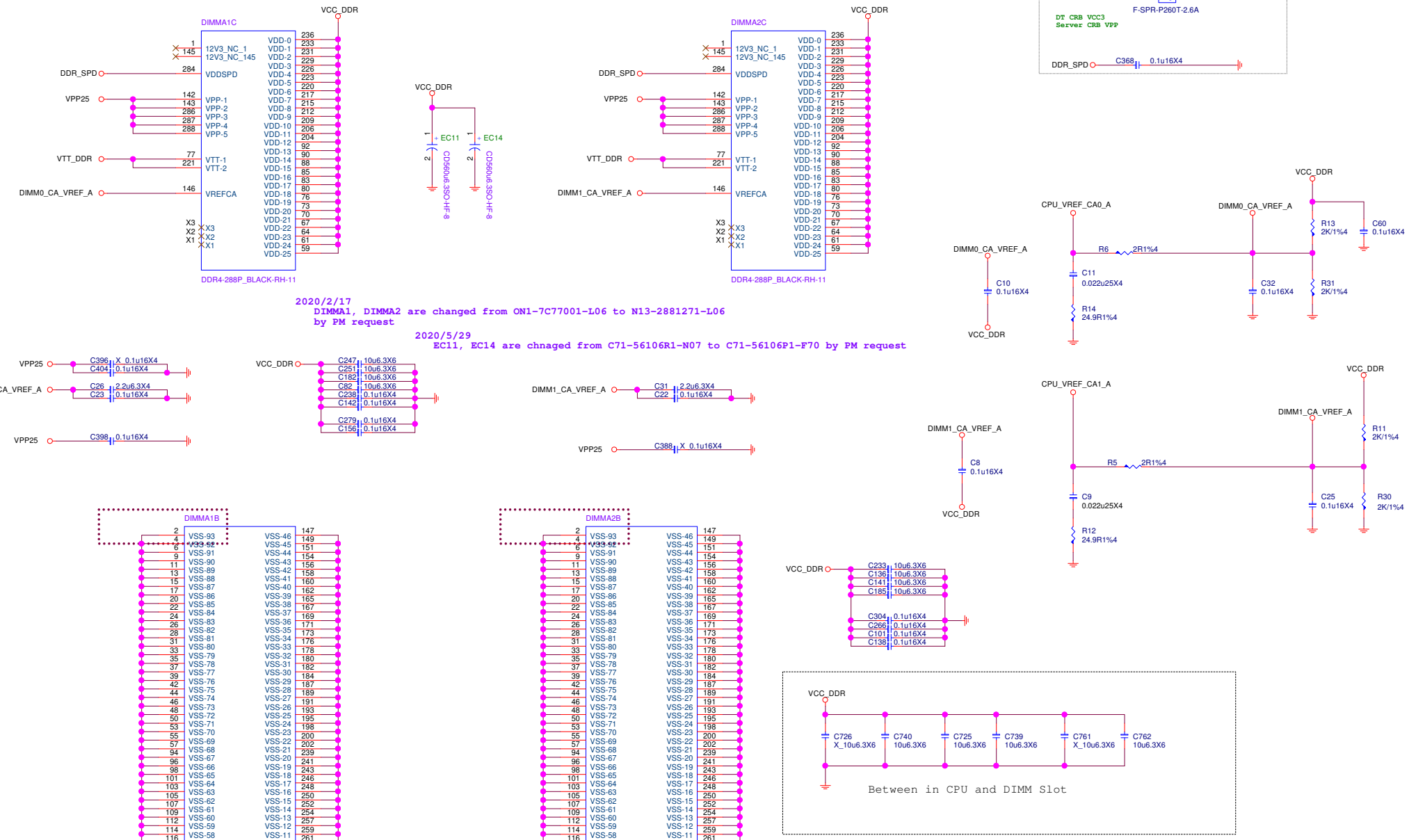
Date: Monday, March 15, 2021 | Sheet 8 of 73



2020/2/17
DIMMB1, DIMMB2 are changed from ON1-7C77001-L06 to N13-2881271-L06
by PM request

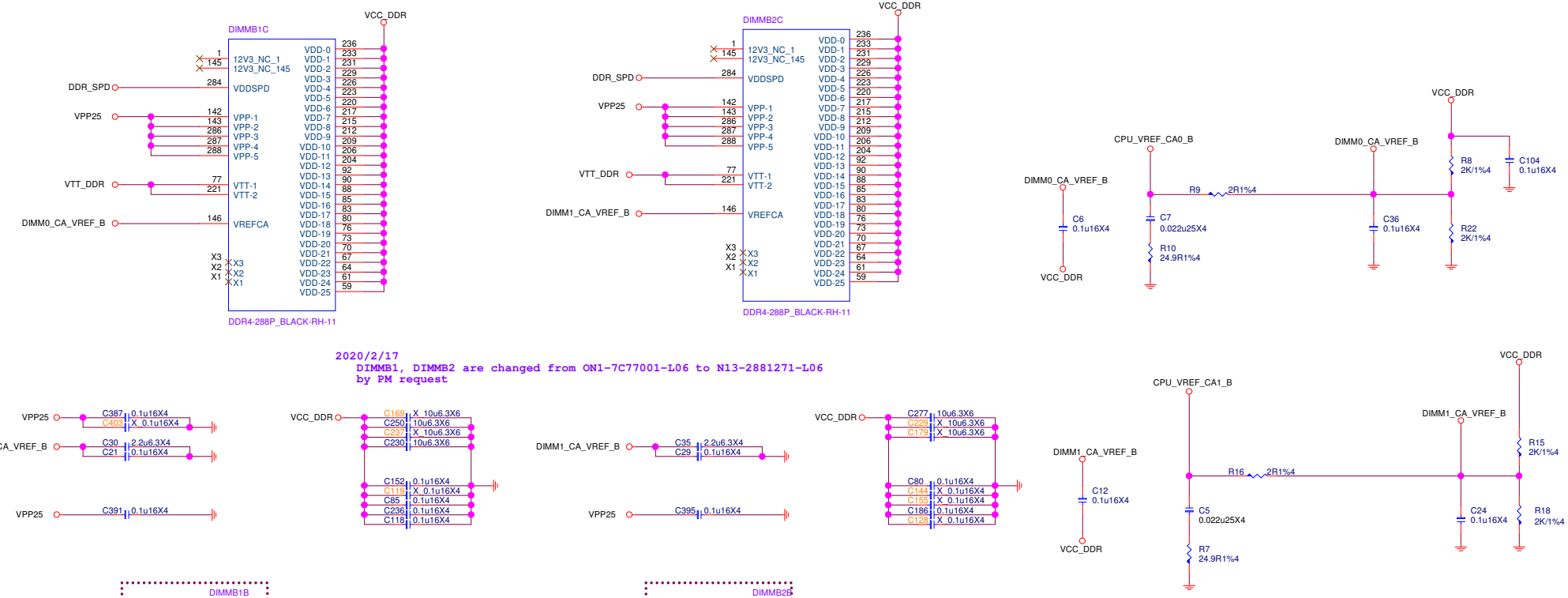
MICRO-STAR INT'L CO.,LTD.

Title	DDR4 SLOT-DIMM3/DIMM4	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 9 of 73	



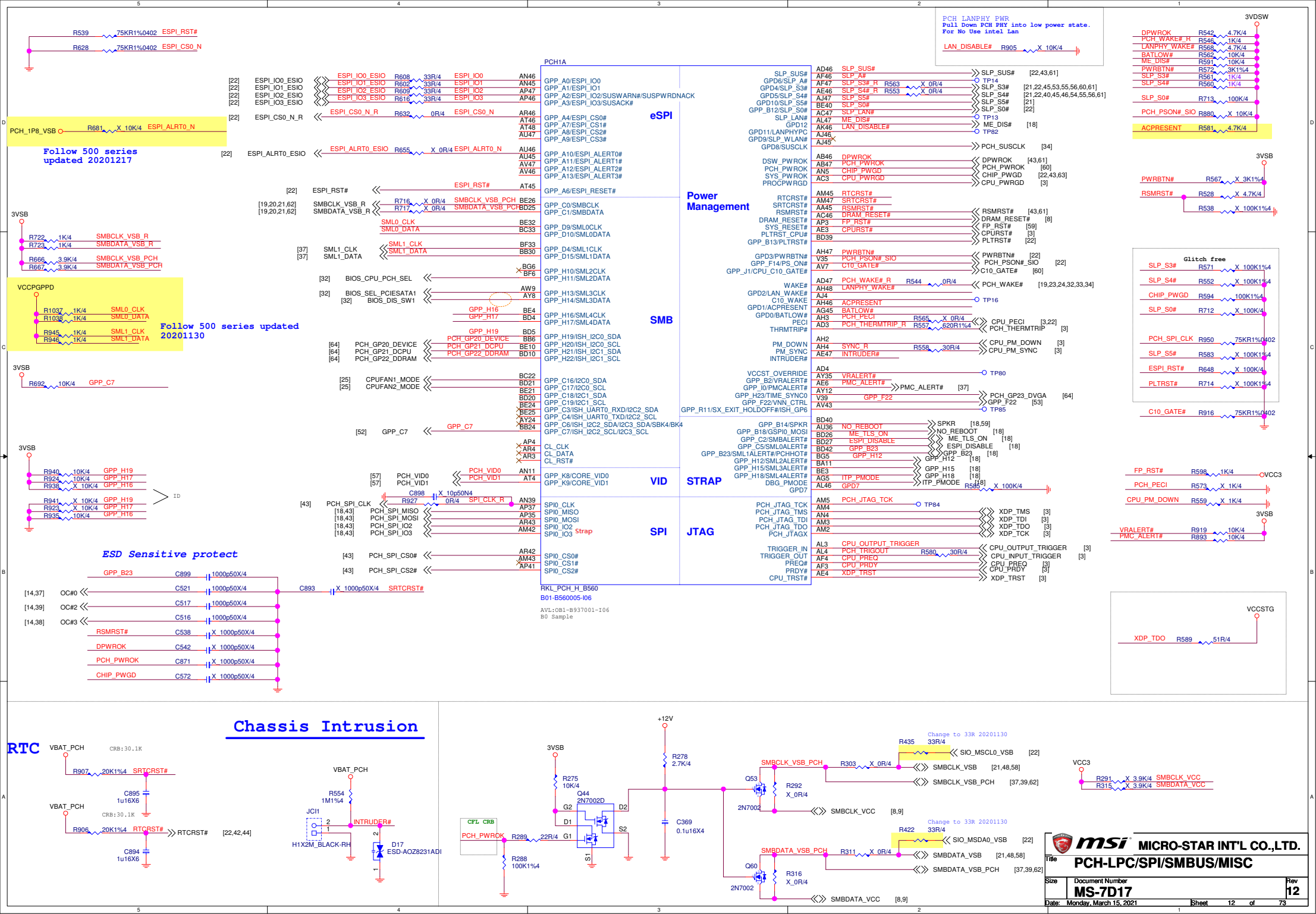
MICRO-STAR INT'L CO.,LTD.

Title	DDR4-POWER/GND-1	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 10 of 73	

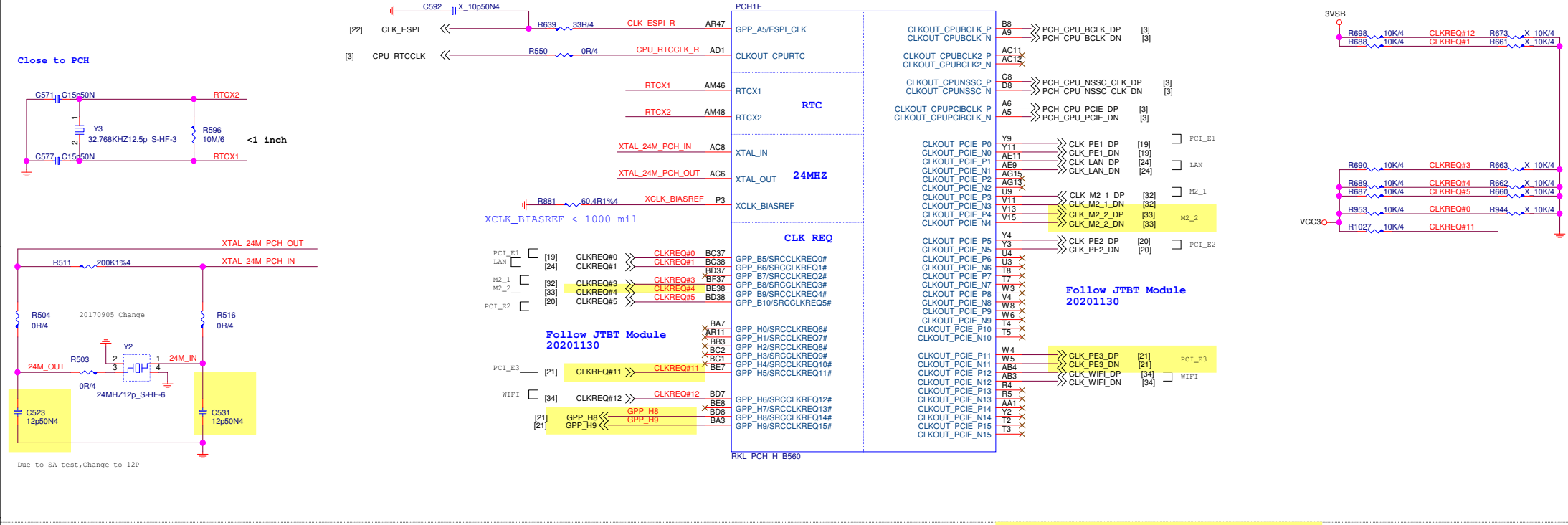


Title	DDR4-POWER/GND-2
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	11 of 73

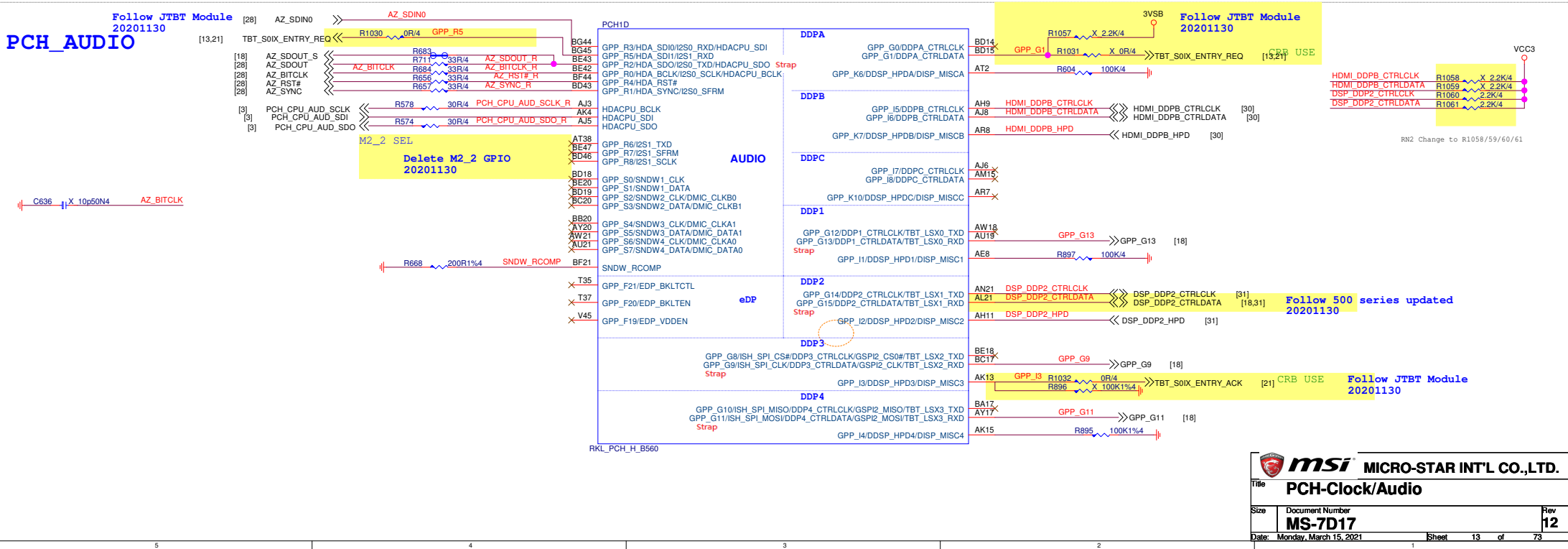
MICRO-STAR INT'L CO.,LTD.


PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
LAN_DISABLE# R905 X_10K/4
PCH1A
eSPI
Power Management
SMB
VID
STRAP
SPI
JTAG
RKL_PCH_H_B560
B01-B560005-I06
AVL:0B1~B937001-I06
B0 Sample
Follow 500 series updated 20201217
Follow 500 series updated 20201130
ESD Sensitive protect
Chassis Intrusion
RTC
Glitch free
Change to 33R 20201130
Change to 33R 20201130
MICRO-STAR INT'L CO.,LTD.
PCH-LPC/SPI/SMBUS/MISC
MS-7D17
Rev 12
Monday, March 15, 2021
Sheet 12 of 73

PCH_CLK

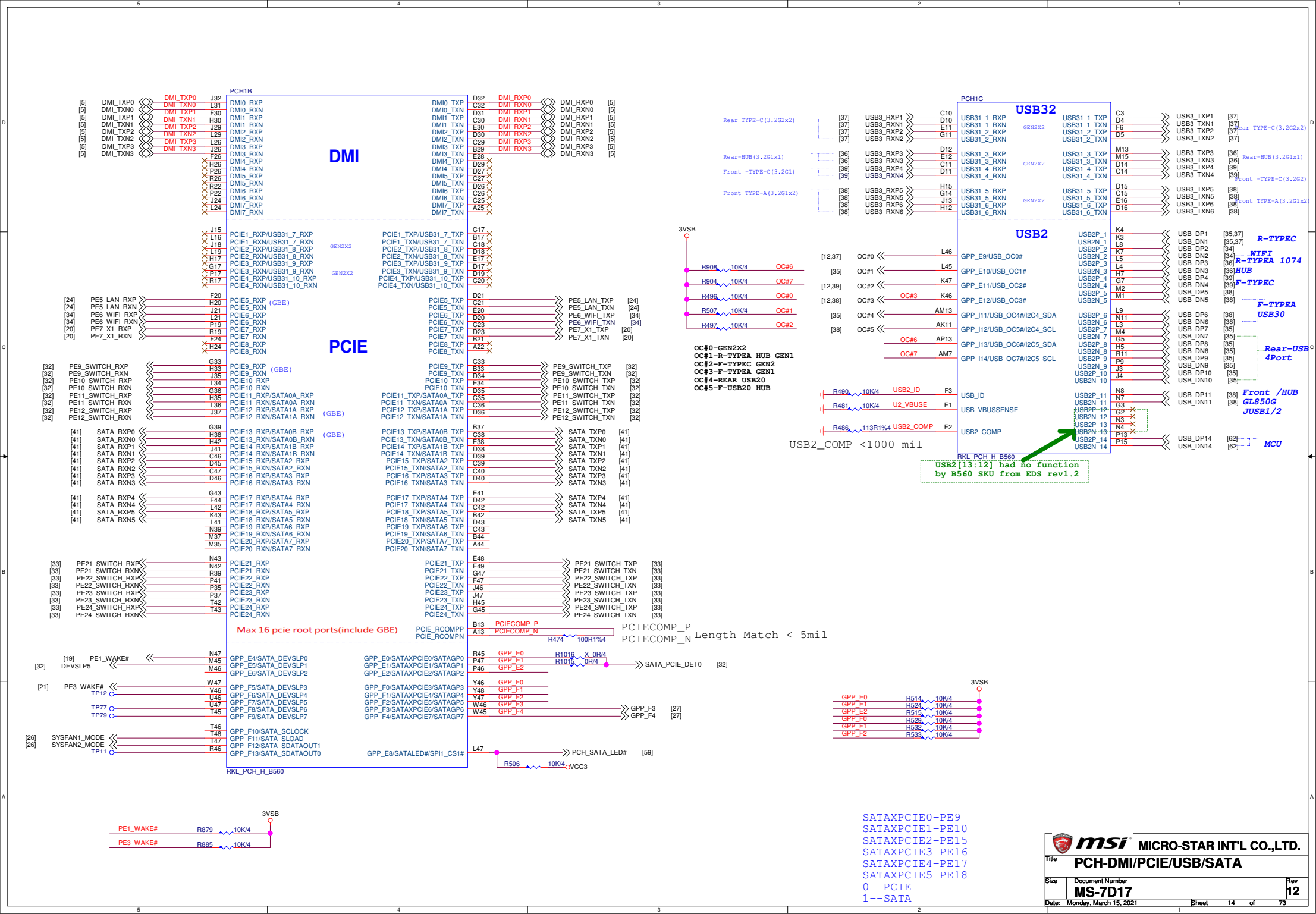


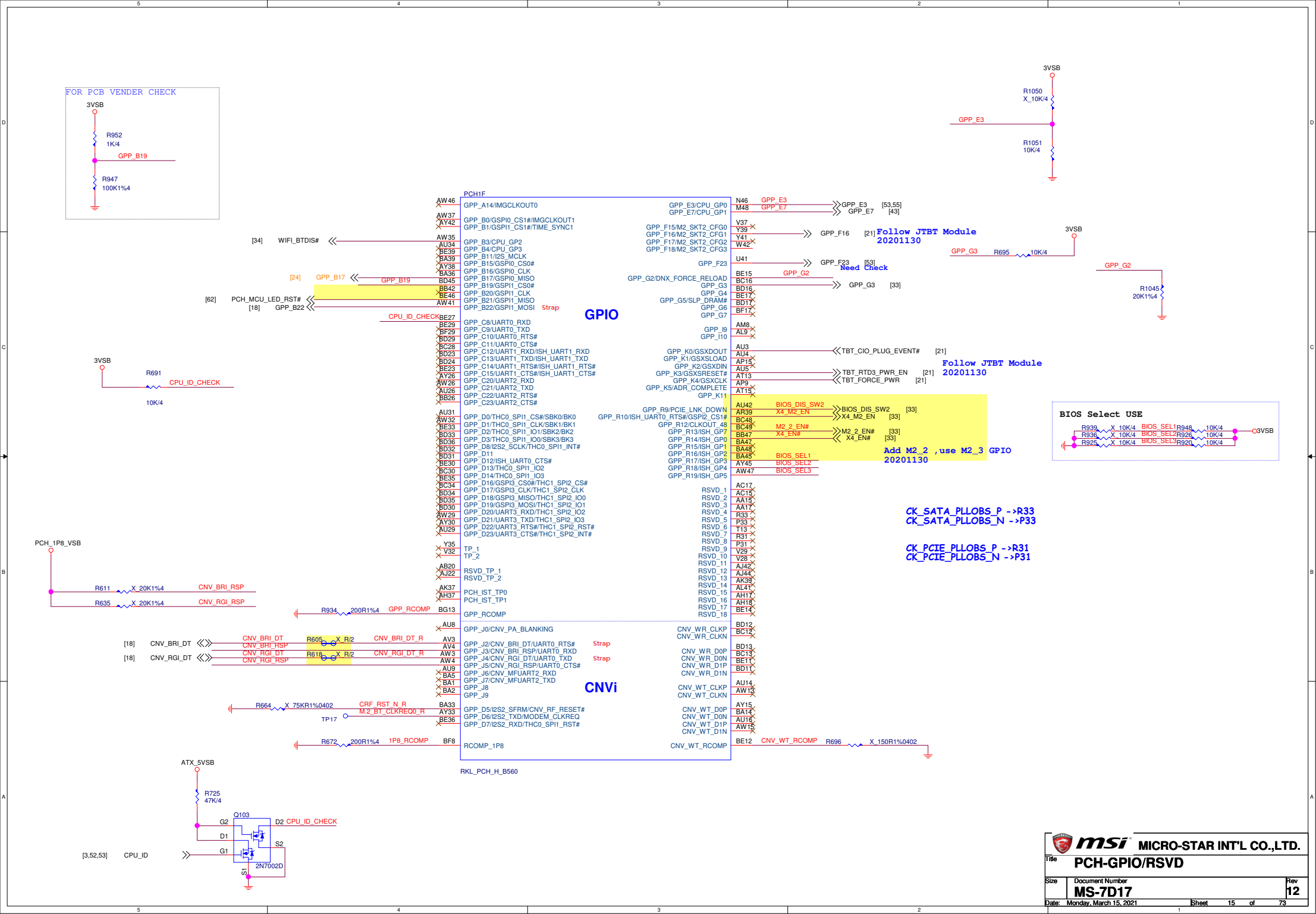
PCH_AUDIO

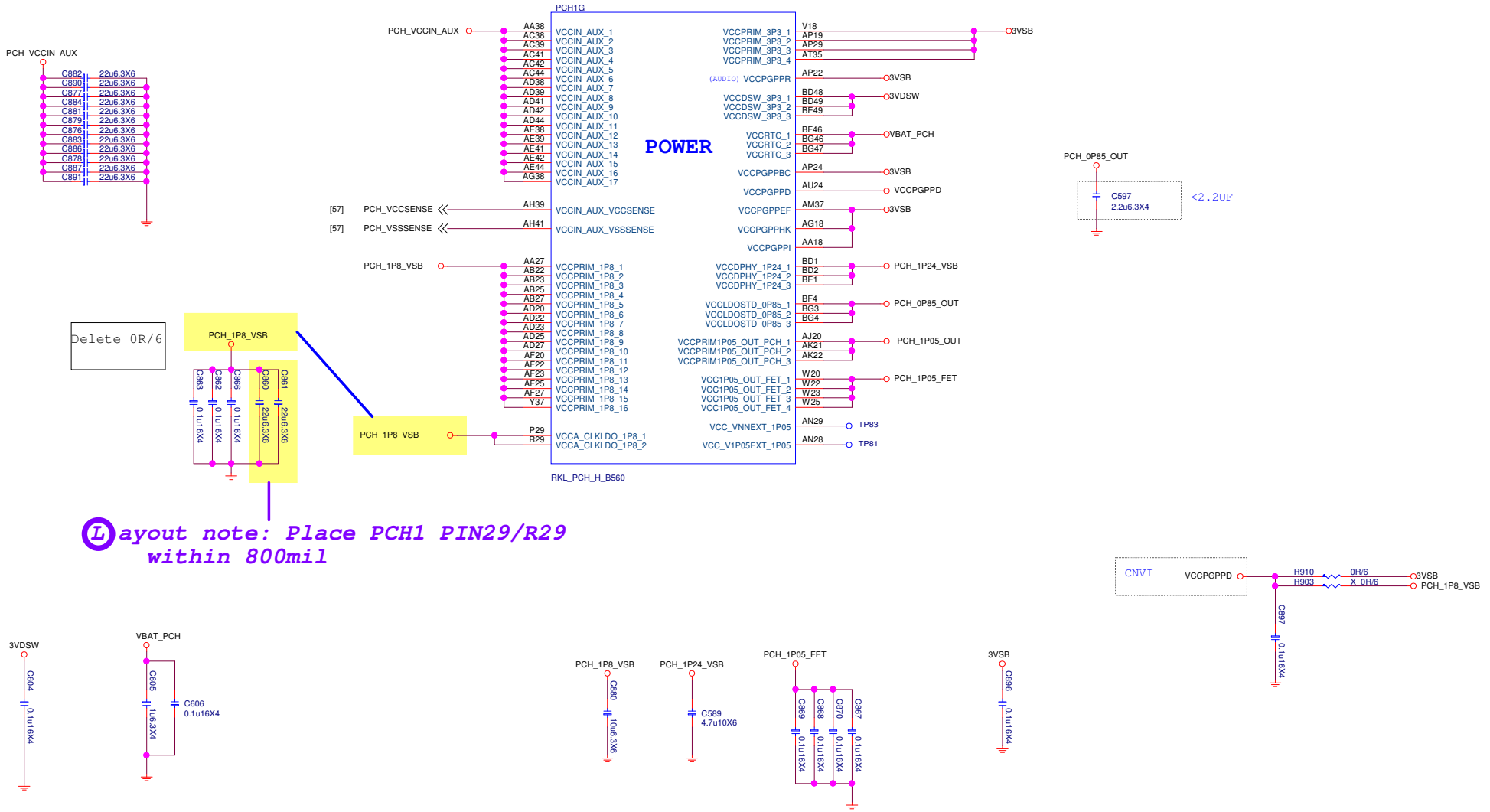


MICRO-STAR INT'L CO.,LTD.

Title	PCH-Clock/Audio	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 13 of 73	


PCH1B
DMI
PCIE
Max 16 pcie root ports(include GBE)
RKL_PCH_H_B560
PCH1C
USB32
USB2
RKL_PCH_H_B560
USB2_COMP <1000 mil
USB2[13:12] had no function by B560 SKU from EDS rev1.2
OC#0-GEN2X2
OC#1-R-TYPEA HUB GEN1
OC#2-F-TYPEC GEN2
OC#3-F-TYPEA GEN1
OC#4-REAR USB20
OC#5-F-USB20 HUB
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
R-TYPEC
WIFI
R-TYPEA 1074
HUB
F-TYPEC
F-TYPEA
USB30
Rear-USB 4Port
Front /HUB
GL850G
JUSB1/2
MCU
MICRO-STAR INT'L CO.,LTD.
PCH-DMI/PCIE/USB/SATA
MS-7D17
12
Monday, March 15, 2021
14
73


FOR PCB VENDER CHECK
3VSB
R952
1K/4
GPP_B19
R947
100K1%4
PCH1F
GPIO
CNVi
RKL_PCH_H_B560
GPP_A14/IMGCLKOUT0
GPP_B0/GSPI0_CS1#/IMGCLKOUT1
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_B11/I2S_MCLK
GPP_B15/GSPI0_CS0#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B19/GSPI1_CS0#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
Strap
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_D0/THC0_SPI1_CS#/SBK0/BK0
GPP_D1/THC0_SPI1_CLK/SBK1/BK1
GPP_D2/THC0_SPI1_IO1/SBK2/BK2
GPP_D3/THC0_SPI1_IO0/SBK3/BK3
GPP_D8/I2S2_SCLK/THC0_SPI1_INT#
GPP_D11
GPP_D12/ISH_UART0_CTS#
GPP_D13/THC0_SPI1_IO2
GPP_D14/THC0_SPI1_IO3
GPP_D16/GSPI3_CS0#/THC1_SPI2_CS#
GPP_D17/GSPI3_CLK/THC1_SPI2_CLK
GPP_D18/GSPI3_MISO/THC1_SPI2_IO0
GPP_D19/GSPI3_MOSI/THC1_SPI2_IO1
GPP_D20/UART3_RXD/THC1_SPI2_IO2
GPP_D21/UART3_TXD/THC1_SPI2_IO3
GPP_D22/UART3_RTS#/THC1_SPI2_RST#
GPP_D23/UART3_CTS#/THC1_SPI2_INT#
TP_1
TP_2
RSVD_TP_1
RSVD_TP_2
PCH_IST_TP0
PCH_IST_TP1
GPP_RCOMP
GPP_J0/CNV_PA_BLANKING
GPP_J2/CNV_BRI_DT/UART0_RTS#
GPP_J3/CNV_BRI_RSP/UART0_RXD
GPP_J4/CNV_RGI_DT/UART0_TXD
GPP_J5/CNV_RGI_RSP/UART0_CTS#
GPP_J6/CNV_MFUART2_RXD
GPP_J7/CNV_MFUART2_TXD
GPP_J8
GPP_J9
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD/THC0_SPI1_RST#
RCOMP_1P8
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_F15/M2_SKT2_CFG0
GPP_F16/M2_SKT2_CFG1
GPP_F17/M2_SKT2_CFG2
GPP_F18/M2_SKT2_CFG3
GPP_F23
GPP_G2/DNX_FORCE_RELOAD
GPP_G3
GPP_G4
GPP_G5/SLP_DRAM#
GPP_G6
GPP_G7
GPP_I9
GPP_I10
GPP_K0/GSXDOUT
GPP_K1/GSXSLOAD
GPP_K2/GSXDIN
GPP_K3/GSXSRESET#
GPP_K4/GSXCLK
GPP_K5/ADR_COMPLETE
GPP_K11
GPP_R9/PCIE_LNK_DOWN
GPP_R10/ISH_UART0_RTS#/GSPI2_CS1#
GPP_R12/CLKOUT_48
GPP_R13/ISH_GP7
GPP_R14/ISH_GP0
GPP_R15/ISH_GP1
GPP_R16/ISH_GP2
GPP_R17/ISH_GP3
GPP_R18/ISH_GP4
GPP_R19/ISH_GP5
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
RSVD_18
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WR_D0P
CNV_WR_D0N
CNV_WR_D1P
CNV_WR_D1N
CNV_WT_CLKP
CNV_WT_CLKN
CNV_WT_D0P
CNV_WT_D0N
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_RCOMP
[34] WIFI_BTDIS#
[24] GPP_B17
GPP_B19
[62] PCH_MCU_LED_RST#
[18] GPP_B22
CPU_ID_CHECK
3VSB
R691
CPU_ID_CHECK
10K/4
PCH_1P8_VSB
R611 X_20K1%4 CNV_BRI_RSP
R635 X_20K1%4 CNV_RGI_RSP
R934 200R1%4 GPP_RCOMP
[18] CNV_BRI_DT
[18] CNV_RGI_DT
CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
R605 X_R/2 CNV_BRI_DT_R
R618 X_R/2 CNV_RGI_DT_R
R664 X_75KR1%0402 CRF_RST_N_R
M.2_BT_CLKREQ0_R
TP17
R672 200R1%4 1P8_RCOMP
ATX_5VSB
R725
47K/4
Q103
2N7002D
G2
D1
G1
S2
S1
D2 CPU_ID_CHECK
[3,52,53] CPU_ID
GPP_E3
GPP_E7
GPP_E3 [53,55]
GPP_E7 [43]
GPP_F16 [21]
Follow JTBT Module
20201130
GPP_F23 [53]
Need Check
GPP_G2
GPP_G3 [33]
TBT_CIO_PLUG_EVENT# [21]
TBT_RTD3_PWR_EN [21]
TBT_FORCE_PWR [21]
Follow JTBT Module
20201130
BIOS_DIS_SW2
X4_M2_EN
M2_2_EN#
X4_EN#
BIOS_SEL1
BIOS_SEL2
BIOS_SEL3
Add M2_2 ,use M2_3 GPIO
20201130
CK_SATA_PLLOBS_P ->R33
CK_SATA_PLLOBS_N ->P33
CK_PCIE_PLLOBS_P ->R31
CK_PCIE_PLLOBS_N ->P31
3VSB
R1050
X_10K/4
GPP_E3
R1051
10K/4
GPP_G3
R695 10K/4
GPP_G2
R1045
20K1%4
BIOS Select USE
R939 X_10K/4 BIOS_SEL1
R936 X_10K/4 BIOS_SEL2
R925 X_10K/4 BIOS_SEL3
R948 10K/4
R926 10K/4
R920 10K/4
3VSB
R696 X_150R1%0402 CNV_WT_RCOMP
MICRO-STAR INT'L CO.,LTD.
Title
PCH-GPIO/RSVD
Size
Document Number
MS-7D17
Rev
12
Date: Monday, March 15, 2021
Sheet 15 of 73

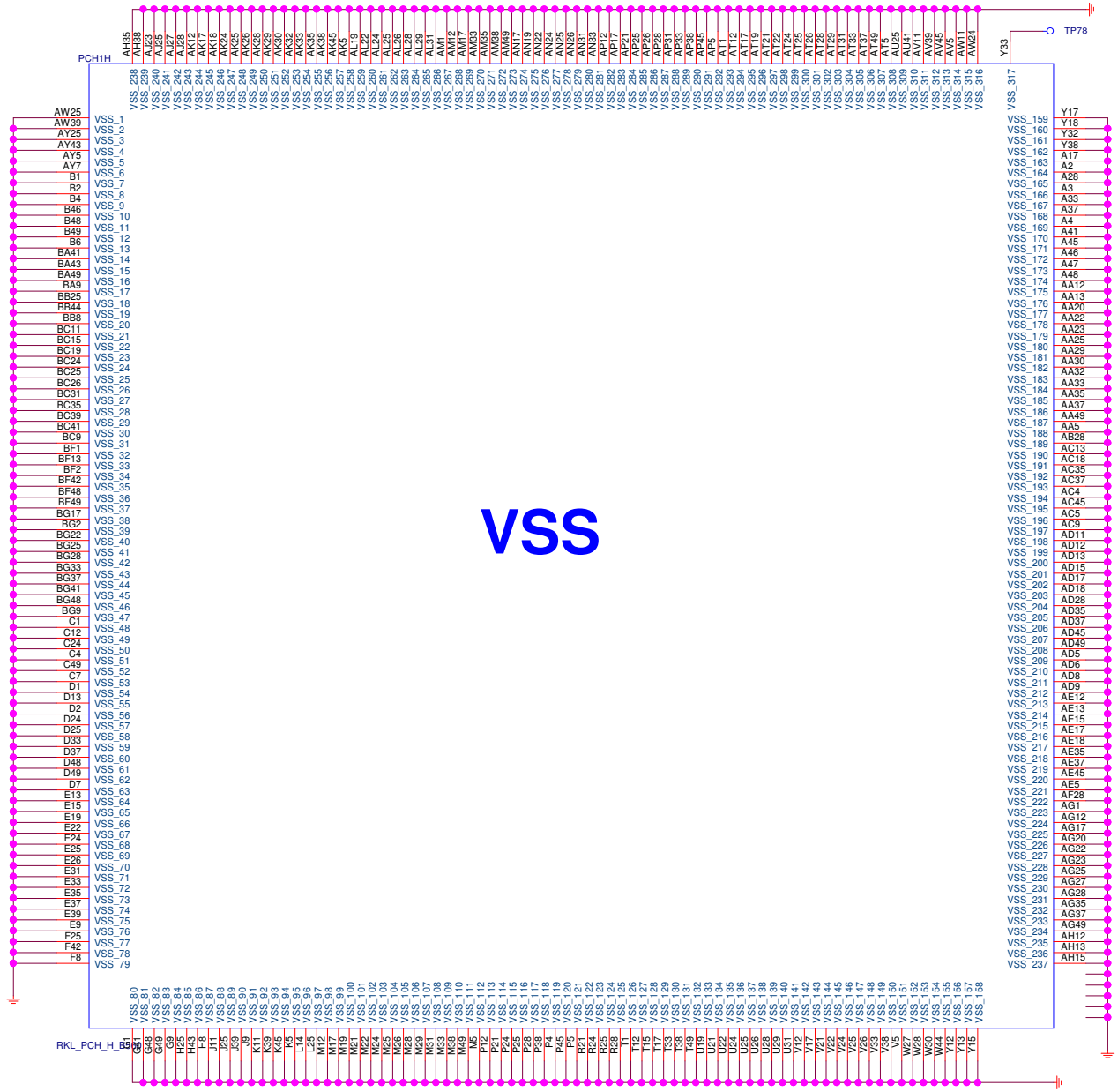


MICRO-STAR INT'L CO.,LTD.

Title: PCH-Power

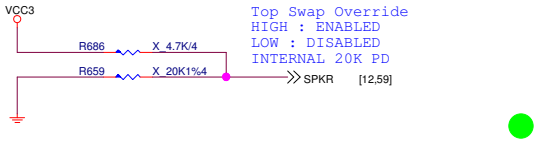
Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 16 of 73

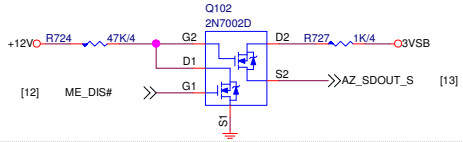


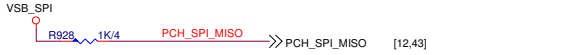
MSI	MICRO-STAR INT'L CO.,LTD.
Title	PCH-GND
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	17 of 73

Top Swap Override
HIGH : ENABLED
LOW : DISABLED
INTERNAL 20K PD

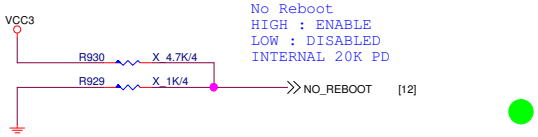


FLASH DESCRIPTOR SECURITY OVERRIDE
HIGH : ENABLE
LOW : DISABLE
INTERNAL 20K PD

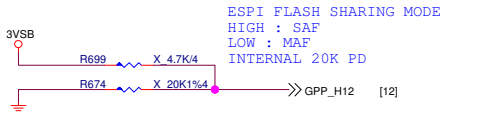




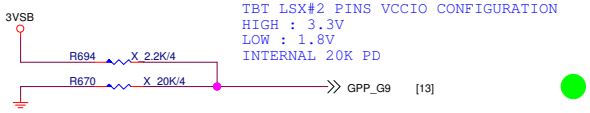
No Reboot
HIGH : ENABLE
LOW : DISABLED
INTERNAL 20K PD



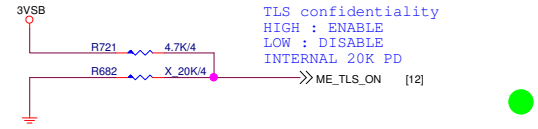
ESPI FLASH SHARING MODE
HIGH : SAF
LOW : MAF
INTERNAL 20K PD



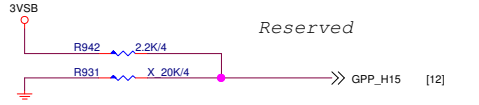
TBT LSX#2 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD



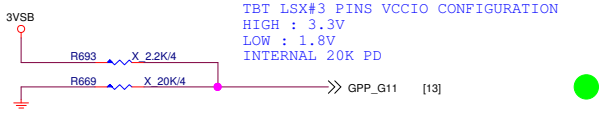
TLS confidentiality
HIGH : ENABLE
LOW : DISABLE
INTERNAL 20K PD



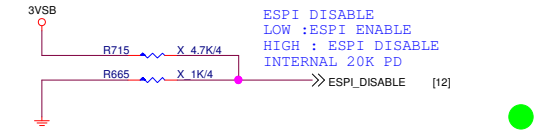
Reserved



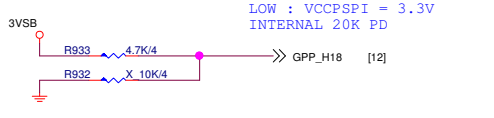
TBT LSX#3 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD



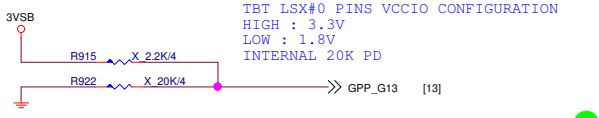
ESPI DISABLE
LOW :ESPI ENABLE
HIGH : ESPI DISABLE
INTERNAL 20K PD



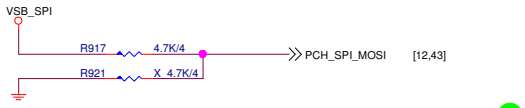
SPI VCCIO CONFIGURATION
HIGH : VCCPSPI = 1.8V
LOW : VCCPSPI = 3.3V
INTERNAL 20K PD



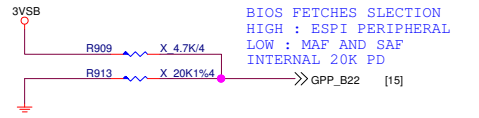
TBT LSX#0 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD



Reserved

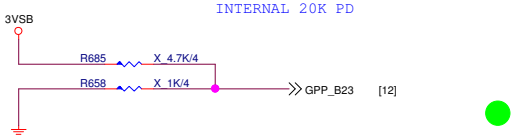


BIOS FETCHES SLECTION
HIGH : ESPI PERIPHERAL
LOW : MAF AND SAF
INTERNAL 20K PD

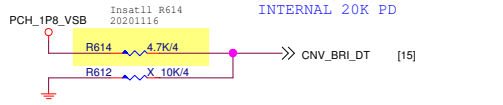


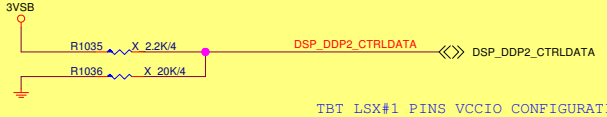
Delete

CPUNSSC CLOCK FREQ
HIGH : 19.2MHZ
LOW : 38.4MHZ
INTERNAL 20K PD



XTAL SEL1
1 = 24MHZ
0 = 38.4/19.2MHZ
INTERNAL 20K PD

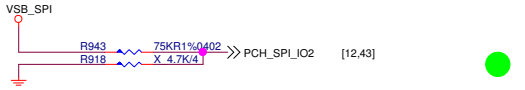




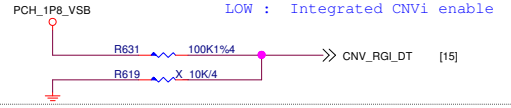
TBT LSX#1 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD

Follow 500 series updated 20201130

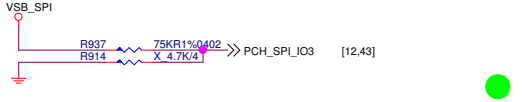
Reserved



M.2 CNVi Mode Select
HIGH : Integrated CNVi disable
LOW : Integrated CNVi enable



Reserved



ITP_PMODE

MICRO-STAR INT'L CO.,LTD.

Title	PCH-Strap	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 18 of 73	

PCI_Express X16 Slot

12V - 5.5A

VCC3 - 3A

3VSB- 375mA

Layout note:+12V TRACE WIDTH >=220MIL
VCC3 WIDTH>=80mil
3VSB WIDTH>=20mil

2020/1/31
R2748 is unstuffed by module circuit updated

20190910
R4594, D102 are added by module updated

Follow 500 series updated
20201130

2020/5/29
EC22 is chnaged from C71-56106R1-N07 to C71-56106P1-F70 by PM request

2020/5/29
EC23 is changed from C71-27118C1-N07 to C71-27118A1-F70 by PM request

PCI_E1
SLOT-PCI164P_BLACK-2PITCH-RH-73
N11-1642081-L06
SLOT_PCIEXP164_23P

SMBus ESD

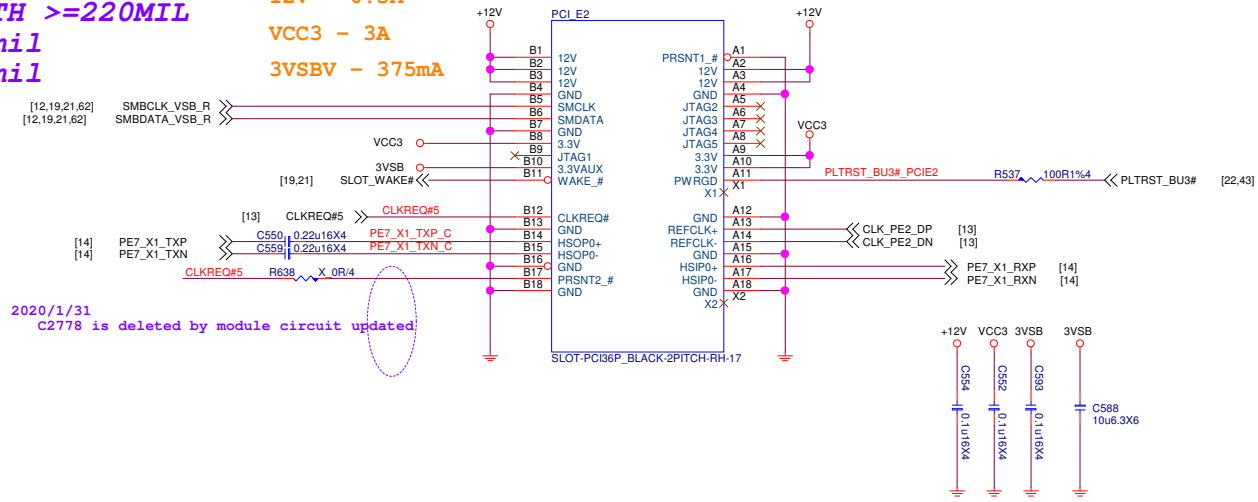
D15 X_ESD-AOZ8231ADI
D14 X_ESD-AOZ8231ADI
D13 ESD-AOZ8231ADI
D36 S-LRB520S-40T1G
D37 S-LRB520S-40T1G
EC21 CD560u6.3SO-HF-8
EC20 CD270u16SO-HF-24
C429 C22u16X50805-HF

Title	PCIE SLOT X16
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	19 of 73

MICRO-STAR INT'L CO.,LTD.

Layout note:+12V TRACE WIDTH >=220MIL
VCC3 WIDTH>=80mil
3VSB WIDTH>=20mil

12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



2020/1/31
C2778 is deleted by module circuit updated

MICRO-STAR INT'L CO.,LTD.

Title	PCIE SLOT-PCH(X1)	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 20 of 73	

PCI_Express X4 Slot

Layout note:+12V TRACE WIDTH >=220MIL
VCC3 WIDTH>=80mil
3VSB WIDTH>=20mil

2.1A at +12V
3A at VCC3
375mA at 3VSB

2020/2/17
PCI_E3 is changed from N11-1000321-L06 to N11-1000151-L06 by PM request

2020/1/31
R597 is unstuffed and C2777 is deleted by same as module circuit

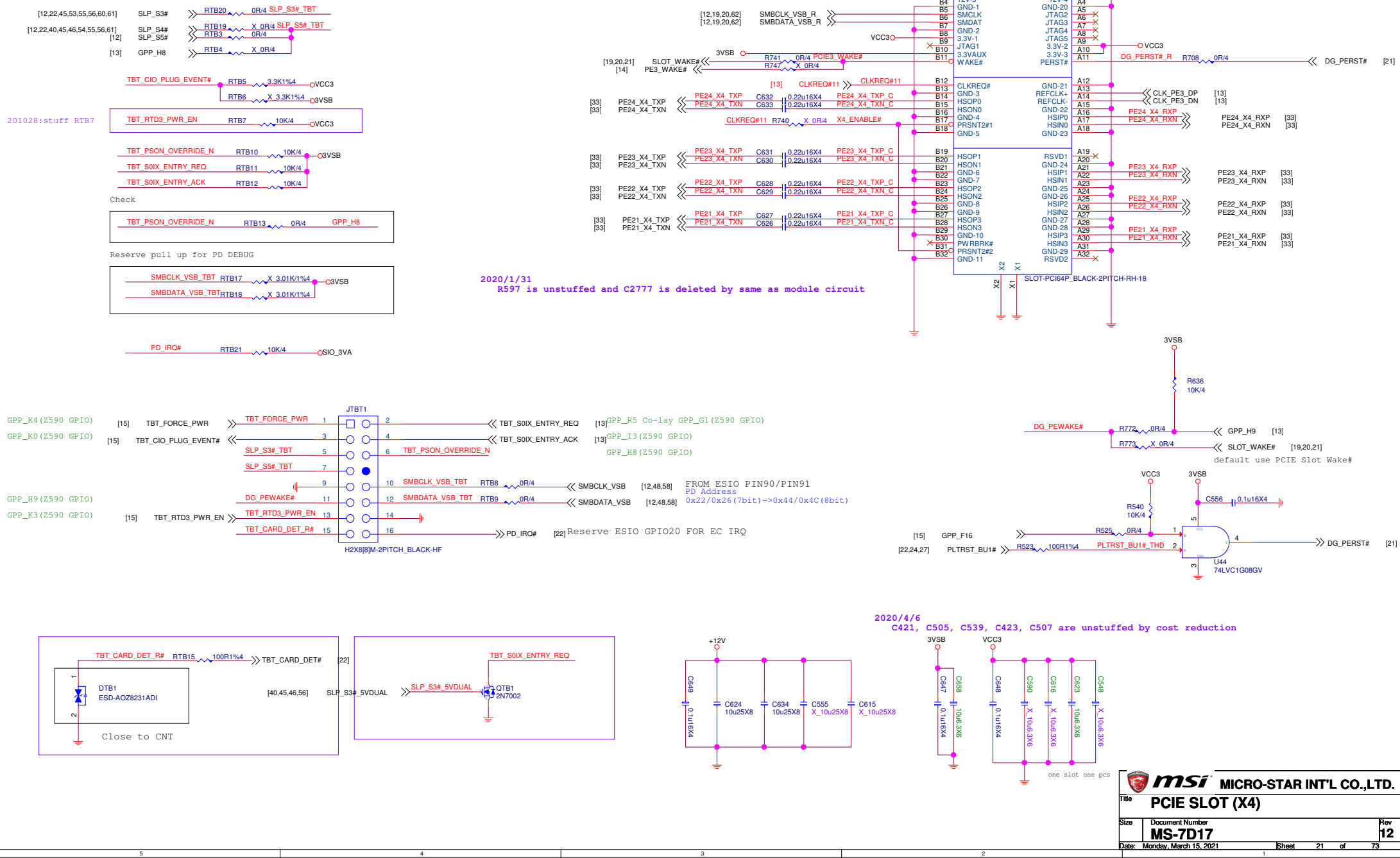
2020/4/6
C421, C505, C539, C423, C507 are unstuffed by cost reduction

201028:stuff RTB7

Check

Reserve pull up for PD DEBUG

Close to CNT



Title	PCIE SLOT (X4)
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	21 of 73

MICRO-STAR INT'L CO.,LTD.

POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA

Follow JTBT Module 20201130

190909:Add GPIO53 for PORT80 Strap change SPEC H disable L enable.

Follow JTBT Module 20201130

190902:Add Q129

Add Q128 20201116

RTCRST DET

3V Analog Power

Closed PIN108

SPI ROM

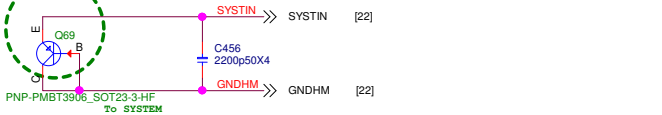
DEBUG PORT

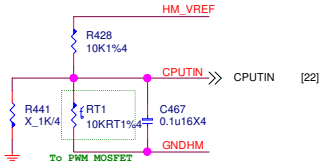
Title	SIO-NCT6687-1
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	22 of 73

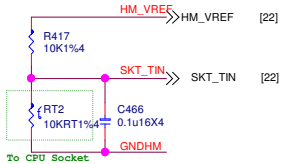
MICRO-STAR INT'L CO.,LTD.

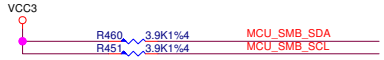
Thermal

Follow Ivy's AVL table recomend change to D02-03906D9-N47 from D02-0390629-O05

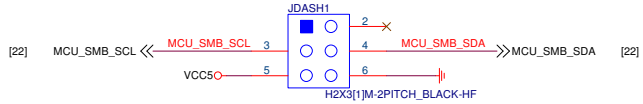






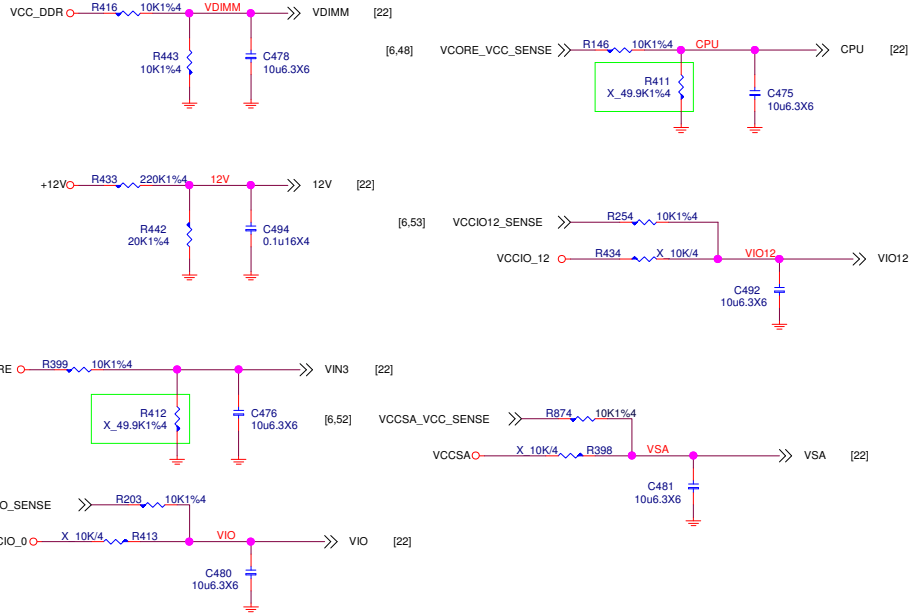


For 4472 Card

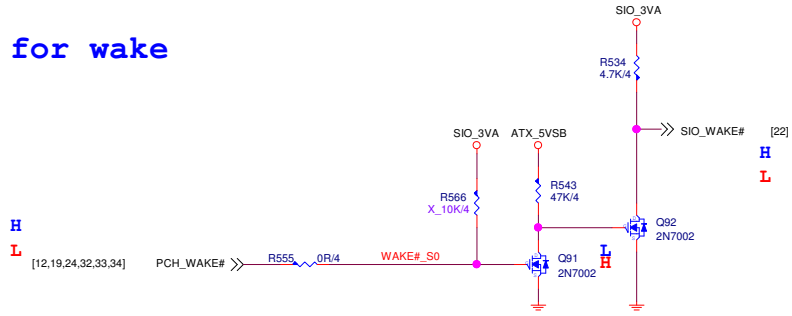


HW Monitor - Voltage

SIO HM Voltage Over 2V will Not Detect



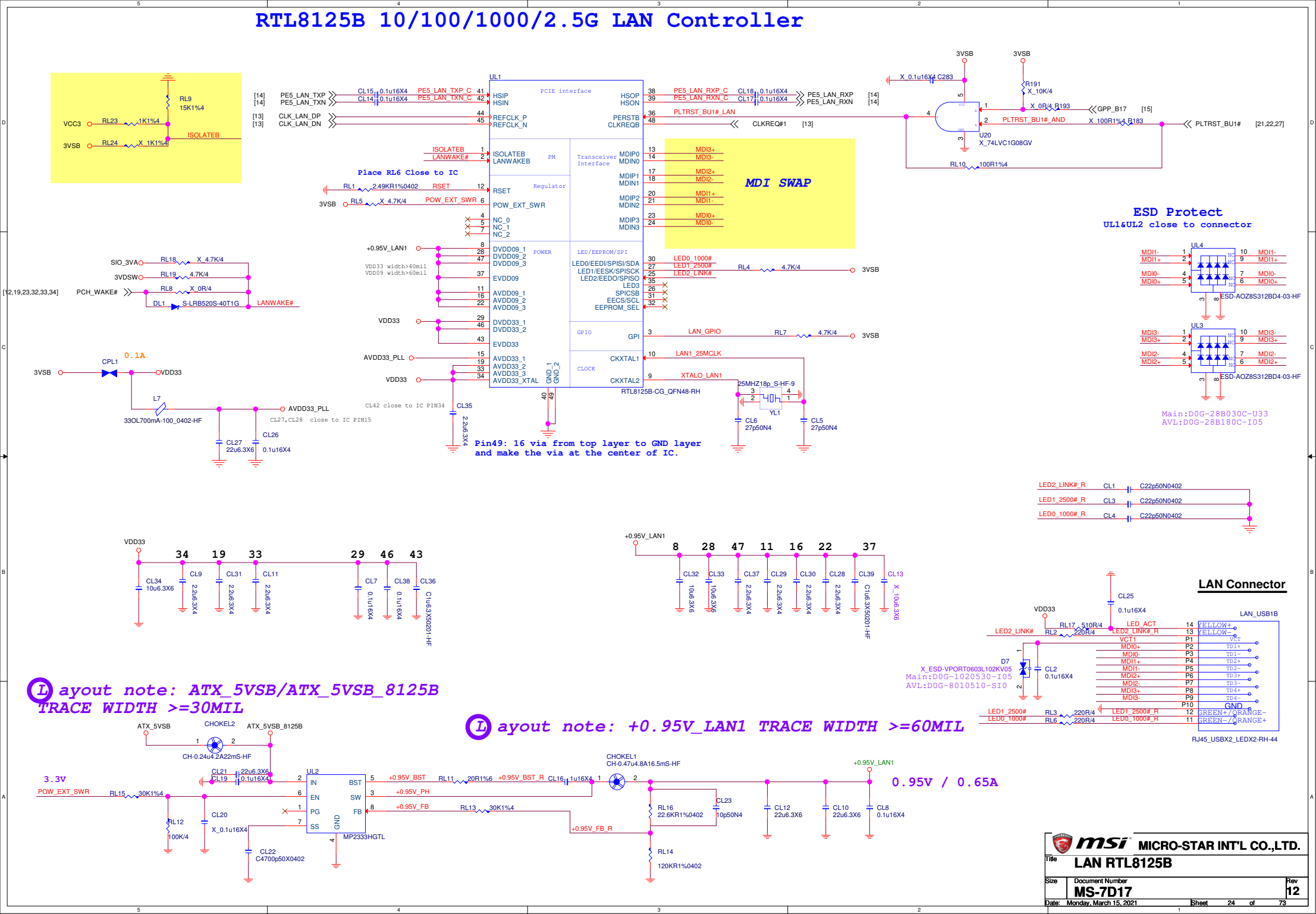
for wake



MICRO-STAR INT'L CO.,LTD.

Title	SIO-NCT6687-2	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 23 of 73	

RTL8125B 10/100/1000/2.5G LAN Controller

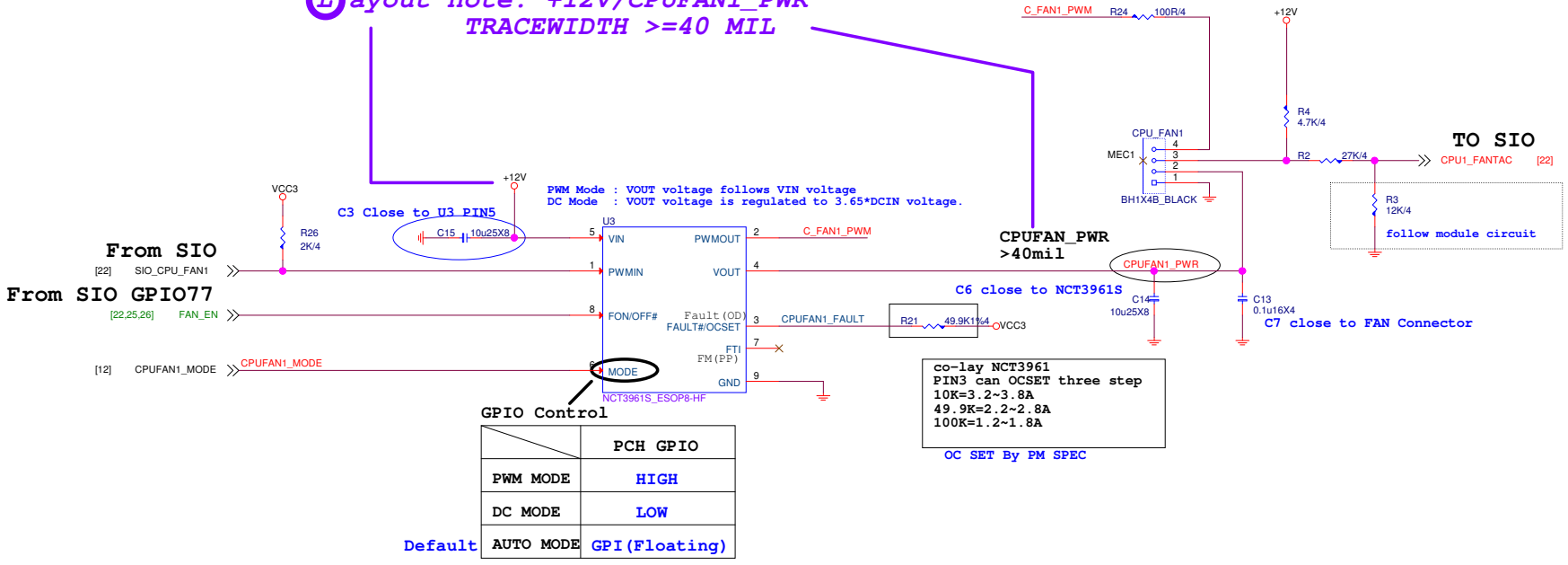


Title	MICRO-STAR INT'L CO.,LTD.		
	LAN RTL8125B		
Size	Document Number	Rev	
	MS-7D17	12	
Date:	Monday, March 15, 2021	Sheet	24 of 73

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

Layout note: +12V/CPUFAN1_PWR
TRACEWIDTH >=40 MIL



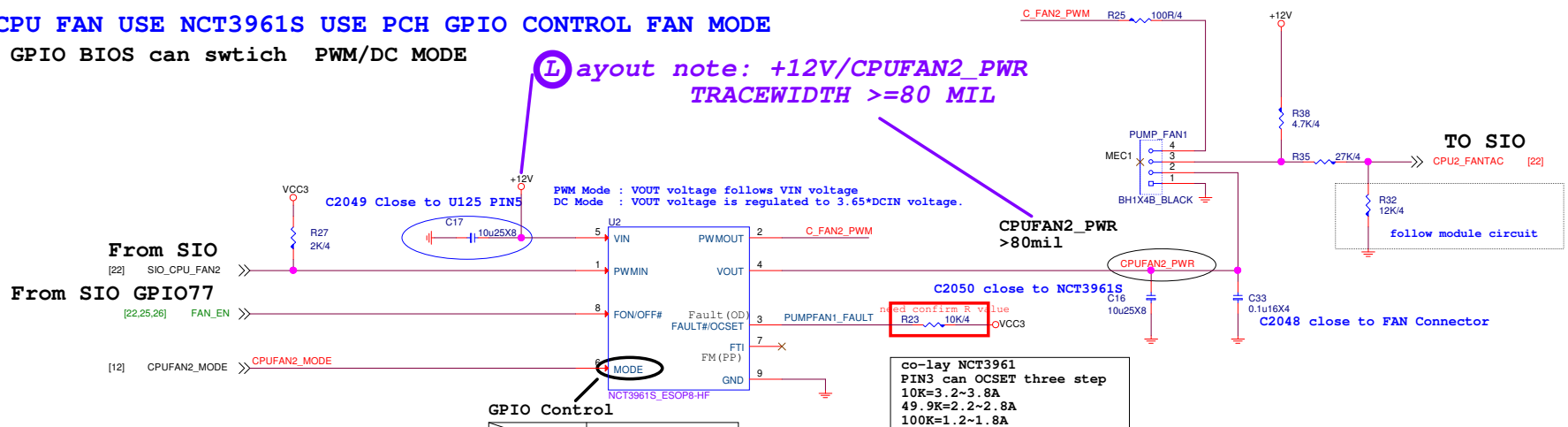
GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

Layout note: +12V/CPUFAN2_PWR
TRACEWIDTH >=80 MIL



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD.

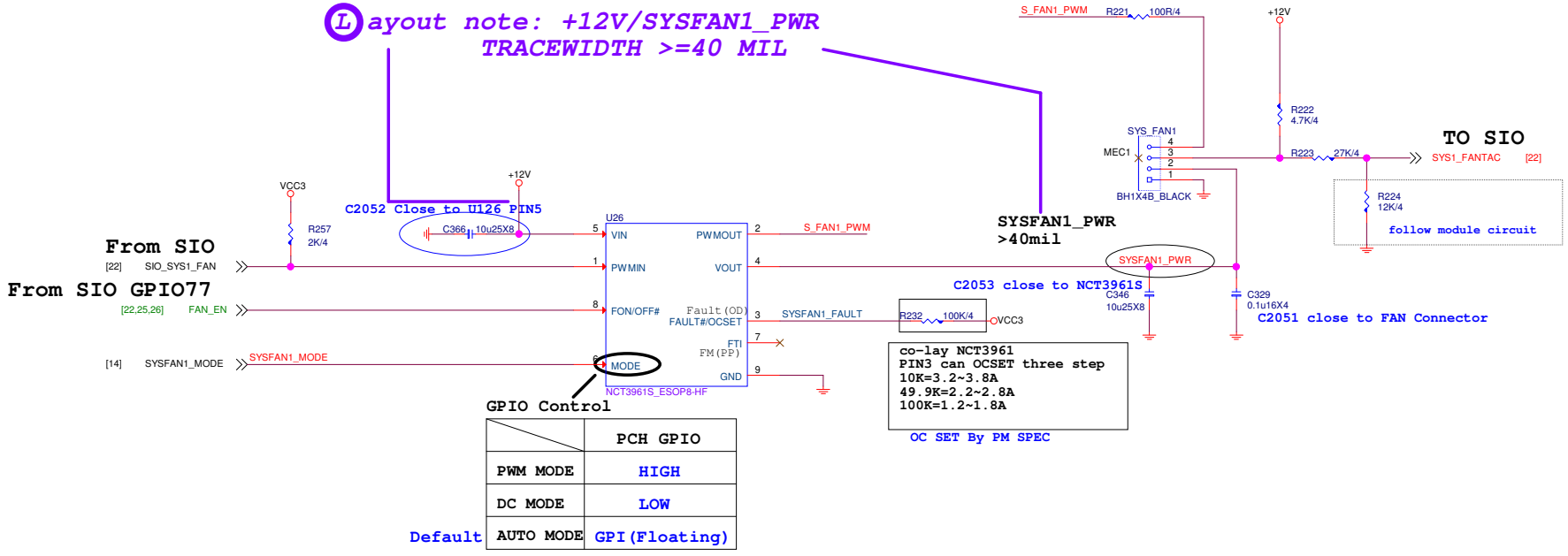
Title: CPU and PUMP FAN

Size | Document Number: MS-7D17 | Rev: 12

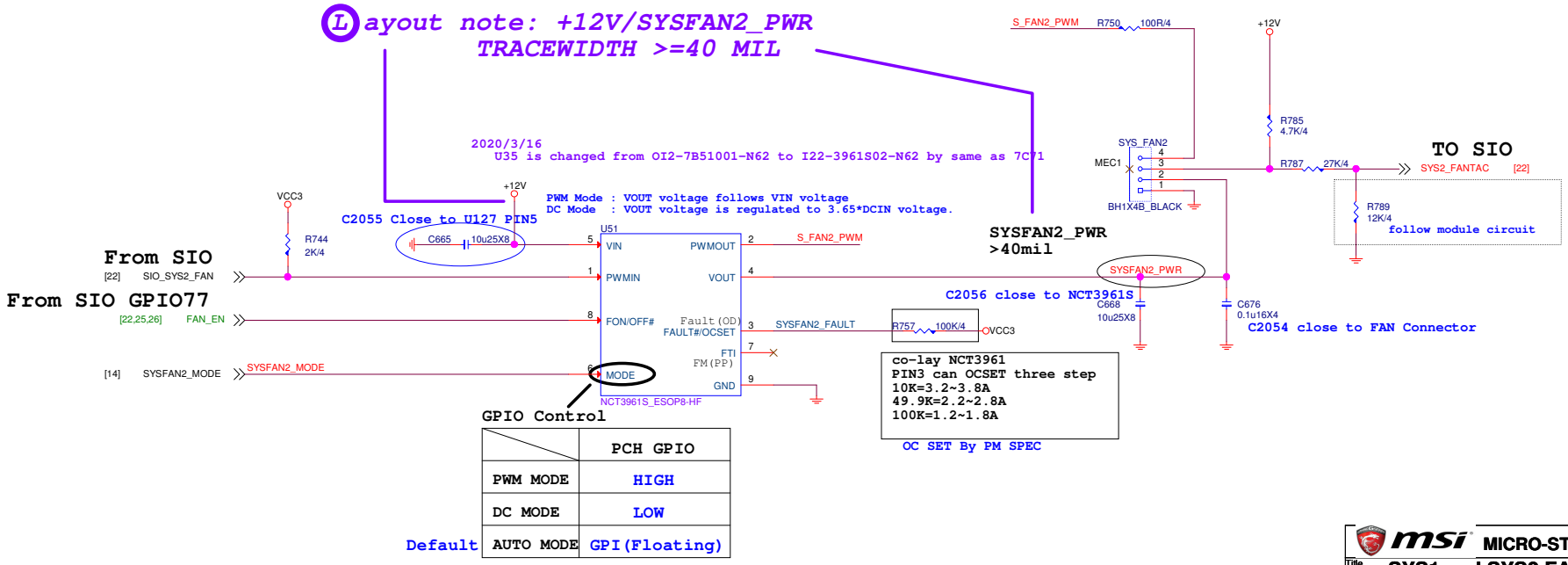
Date: Monday, March 15, 2021 | Sheet 25 of 73

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



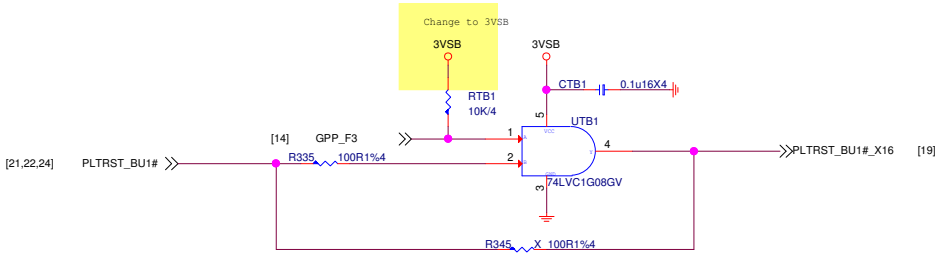
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

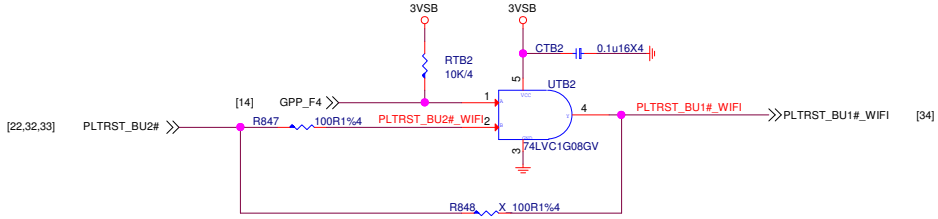
MICRO-STAR INT'L CO.,LTD.

Title: SYS1 and SYS2 FAN

Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 26 of 73





MICRO-STAR INT'L CO.,LTD.

Title

Size	Document Number	Rev
	MS-7D17	12

Date: Monday, March 15, 2021 Sheet 27 of 73

ALC897

UA1
ALC897
B05-LC89704-R09
AVL:0B5-7D1002-R09

follow PCH power well

Digital
Analog

Closed pin1
Closed pin25
Closed pin18
Closed pin38
Close to JAUD1
Closed Codec

LIN_OUT
SURR
LIN_IN
MIC1
CEN/BAS

For EMI
For EMI

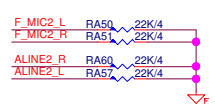
4	CEN/BAS	LIN_IN	3
5	SURR	LIN_OUT	2
6	SPDIFO1	MIC1	1

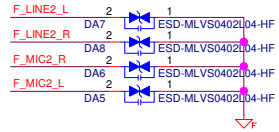
MICRO-STAR INT'L CO.,LTD.

Title: AUDIO-ALC897-1

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 28 of 73

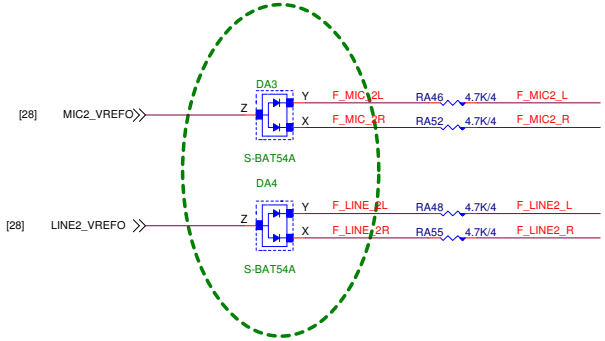




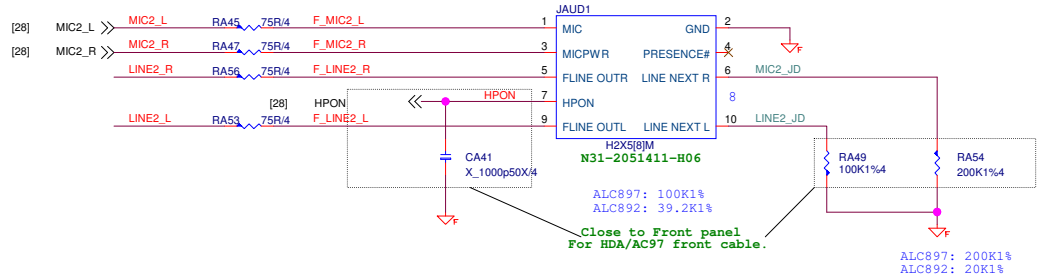
Close to Front panel

ESD protect

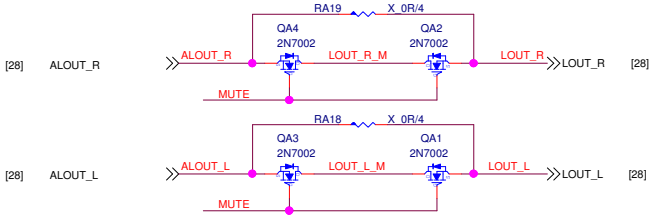
D0G-2710510-I05
AVL:ODG-7C71001-T43

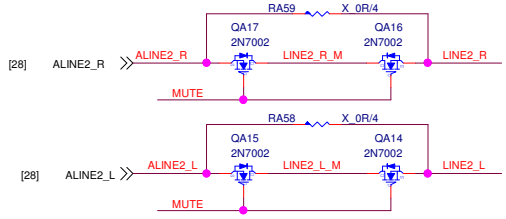


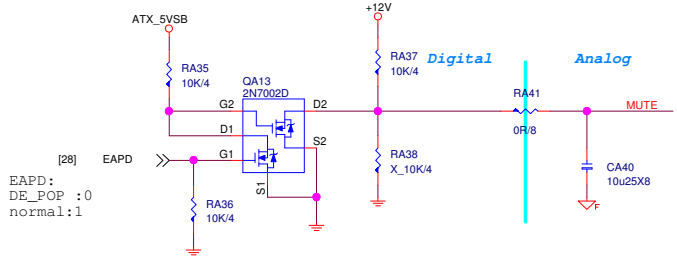
Follow Ivy's AVL table recomend change to D01-AT54A09-P15

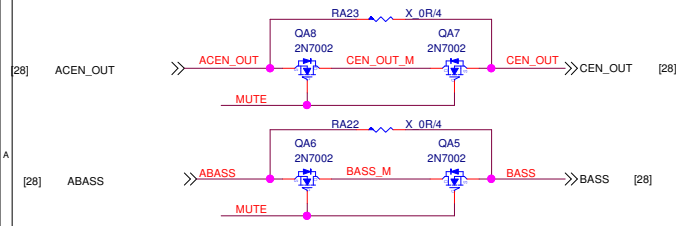


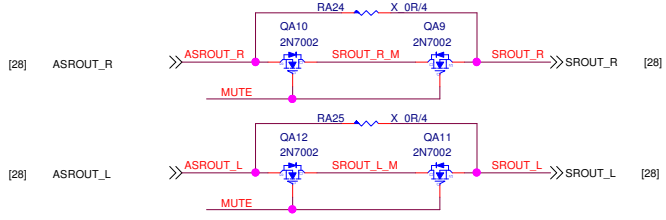
De-POP circuit









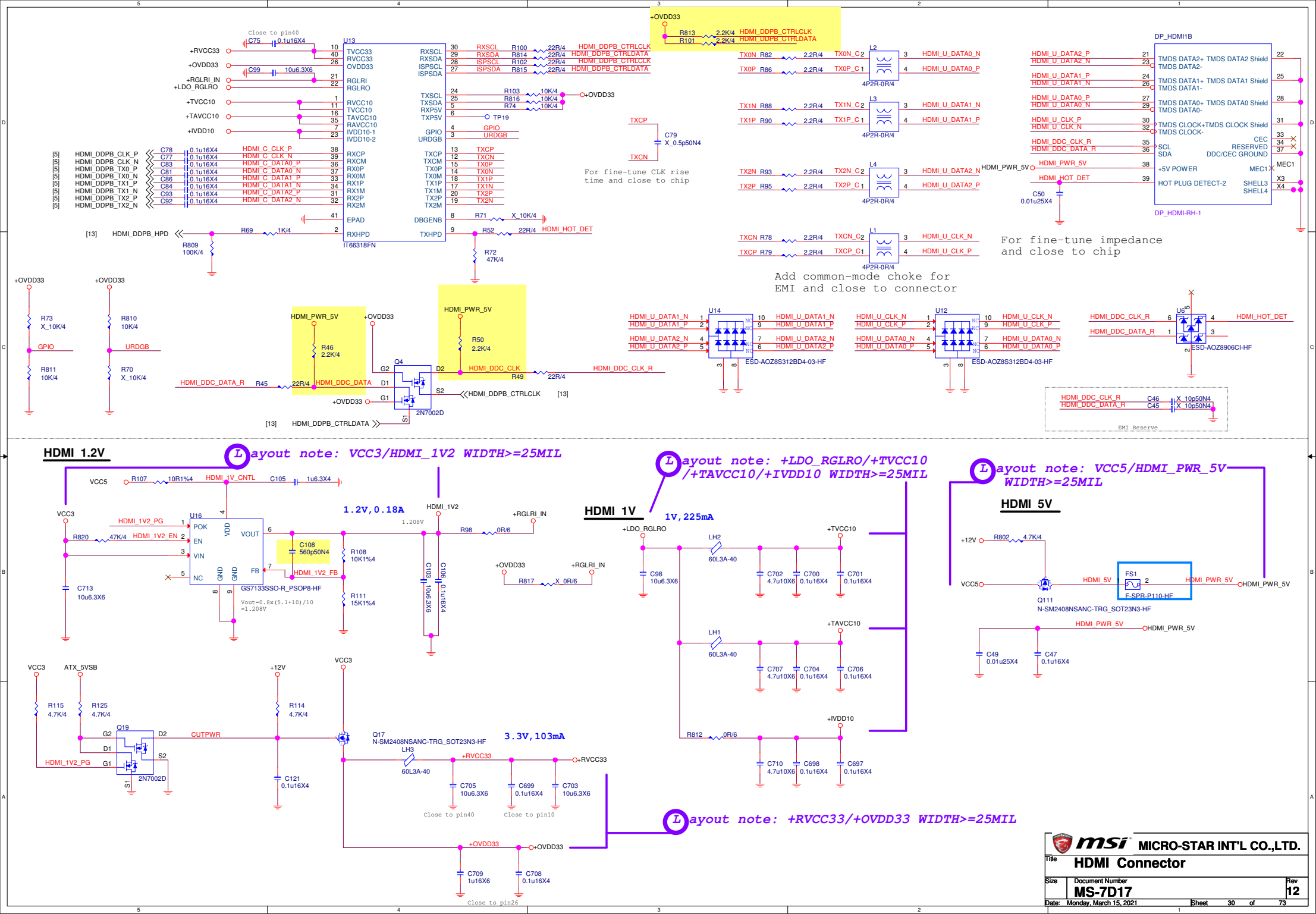


MICRO-STAR INT'L CO.,LTD.

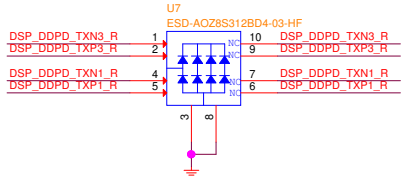
Title: AUDIO-ALC897-2

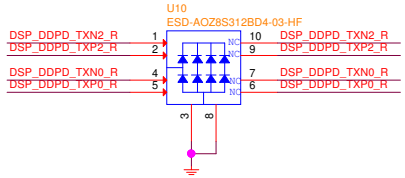
Size: Document Number: MS-7D17 Rev: 12

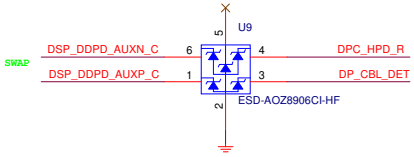
Date: Monday, March 15, 2021 Sheet 29 of 73

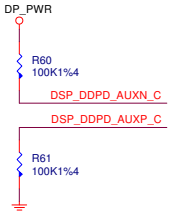

HDMI 1.2V
Layout note: VCC3/HDMI_1V2 WIDTH>=25MIL
1.2V,0.18A
HDMI 1V
Layout note: +LDO_RGLRO/+TVCC10 /+TAVCC10/+IVDD10 WIDTH>=25MIL
1V,225mA
HDMI 5V
Layout note: VCC5/HDMI_PWR_5V WIDTH>=25MIL
3.3V,103mA
Layout note: +RVCC33/+OVDD33 WIDTH>=25MIL
Add common-mode choke for EMI and close to connector
For fine-tune CLK rise time and close to chip
For fine-tune impedance and close to chip
IT66318FN
GS7133SSO-R_PSOP8-HF
2N7002D
N-SM2408NSANC-TRG_SOT23N3-HF
F-SPR-P110-HF
ESD-AOZ8S312BD4-03-HF
ESD-AOZ8906CI-HF
DP_HDMI-RH-1
EMI Reserve
MSI MICRO-STAR INT'L CO.,LTD.
Title HDMI Connector
Size Document Number MS-7D17 Rev 12
Date: Monday, March 15, 2021 Sheet 30 of 73

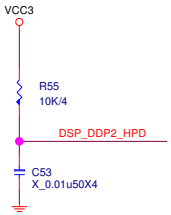
DP

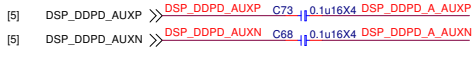




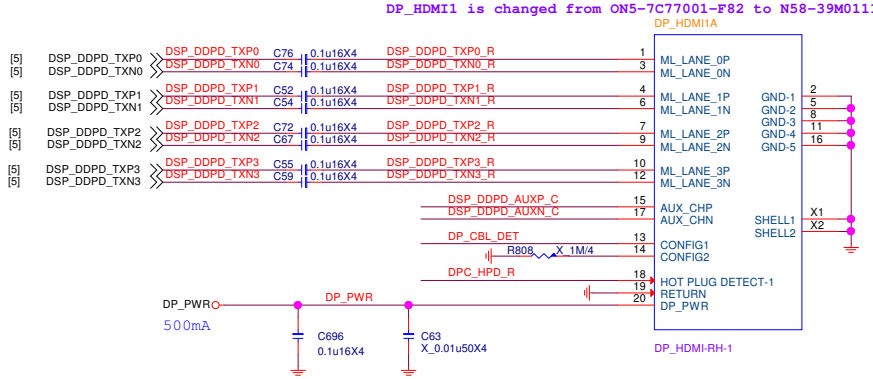




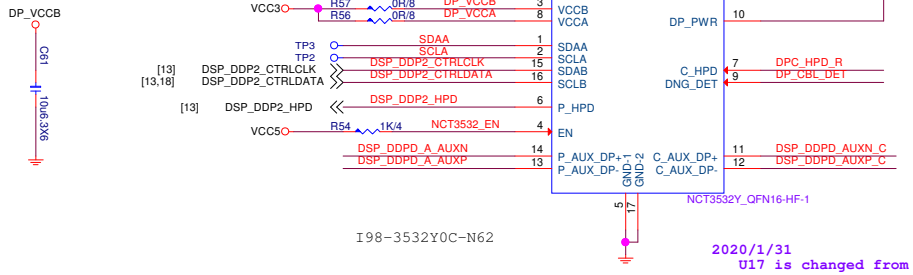




2020/3/16
DP_HDMI1 is changed from ON5-7C77001-F82 to N58-39M0111-F82 by PM request



Layout note:DP_VCCA/DP_VCCB/DP_PWR WIDTH>=30MIL



I98-3532Y0C-N62

2020/1/31
U17 is changed from I98-3532Y0C-N62 to I98-3532Y1C-N62 by Ivy's comment

MICRO-STAR INT'L CO.,LTD.

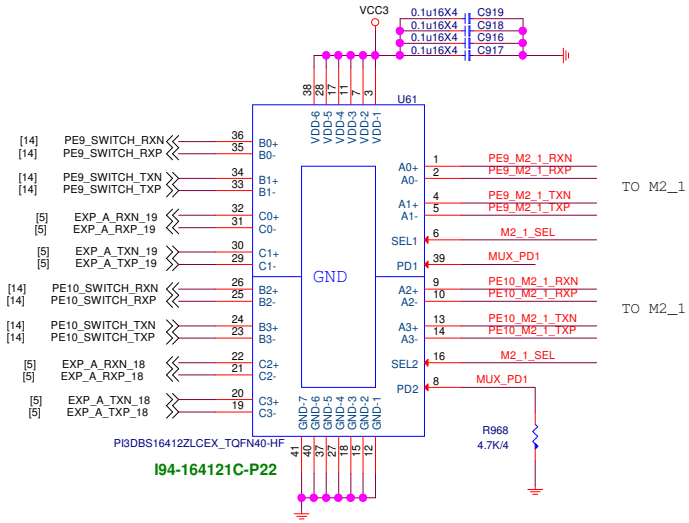
Title: DisplayPort Connector

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 31 of 73

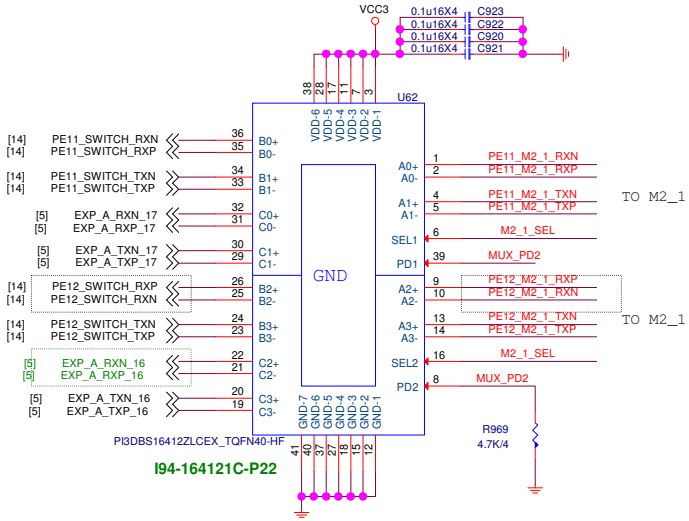
M.2 Connector

M.2 Connector



TO M2_1

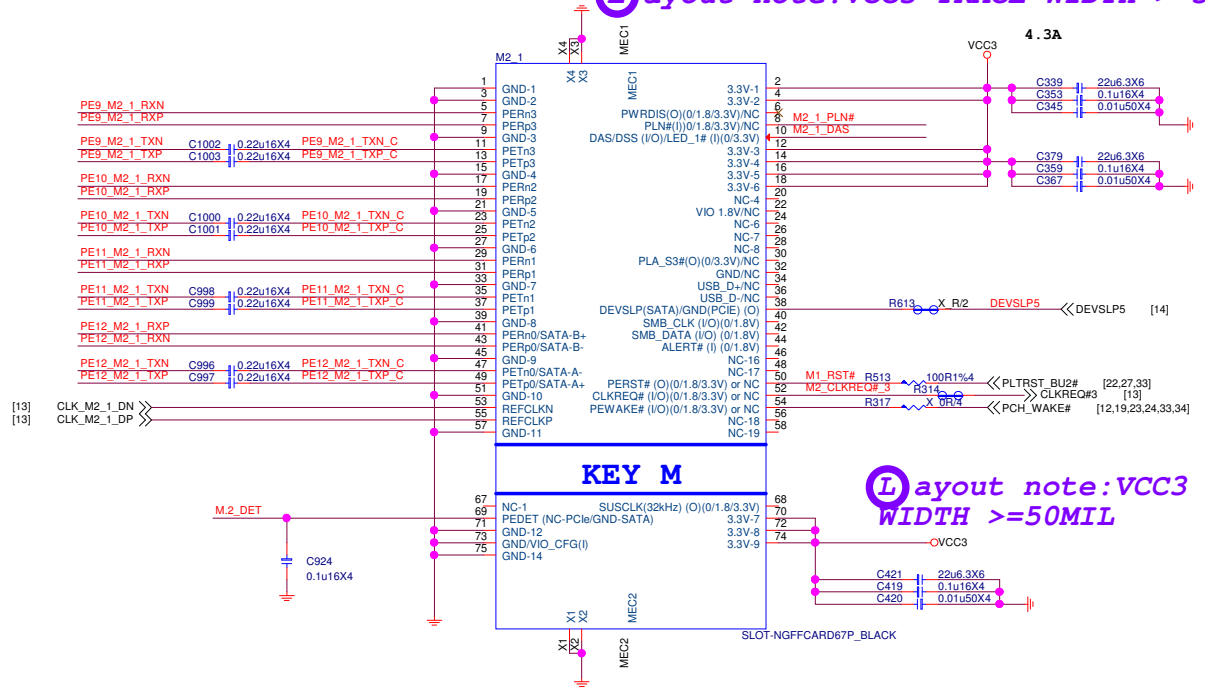
TO M2_1



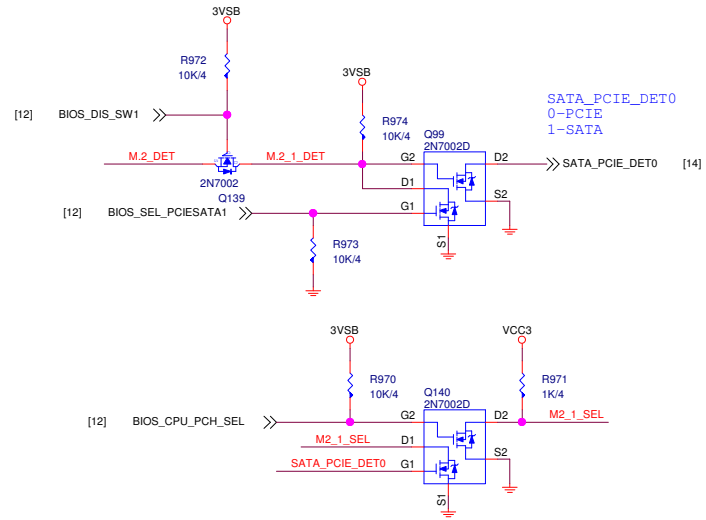
TO M2_1

TO M2_1

Layout note:VCC3 TRACE WIDTH >=50MIL



Layout note:VCC3 WIDTH >=50MIL



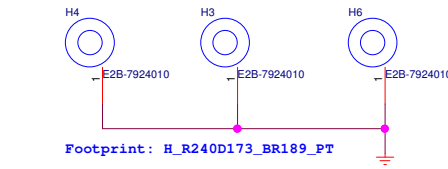
BIOS_MODE

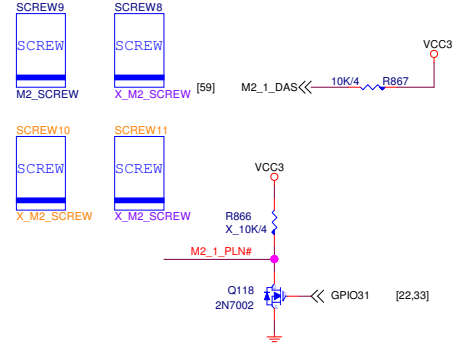
DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

BIOS_SEL

BIOS_CPU_PCH_SEL GPP_K7	
GPI (1)	CML(PCH)
GPO (0)	RKL(CPU)

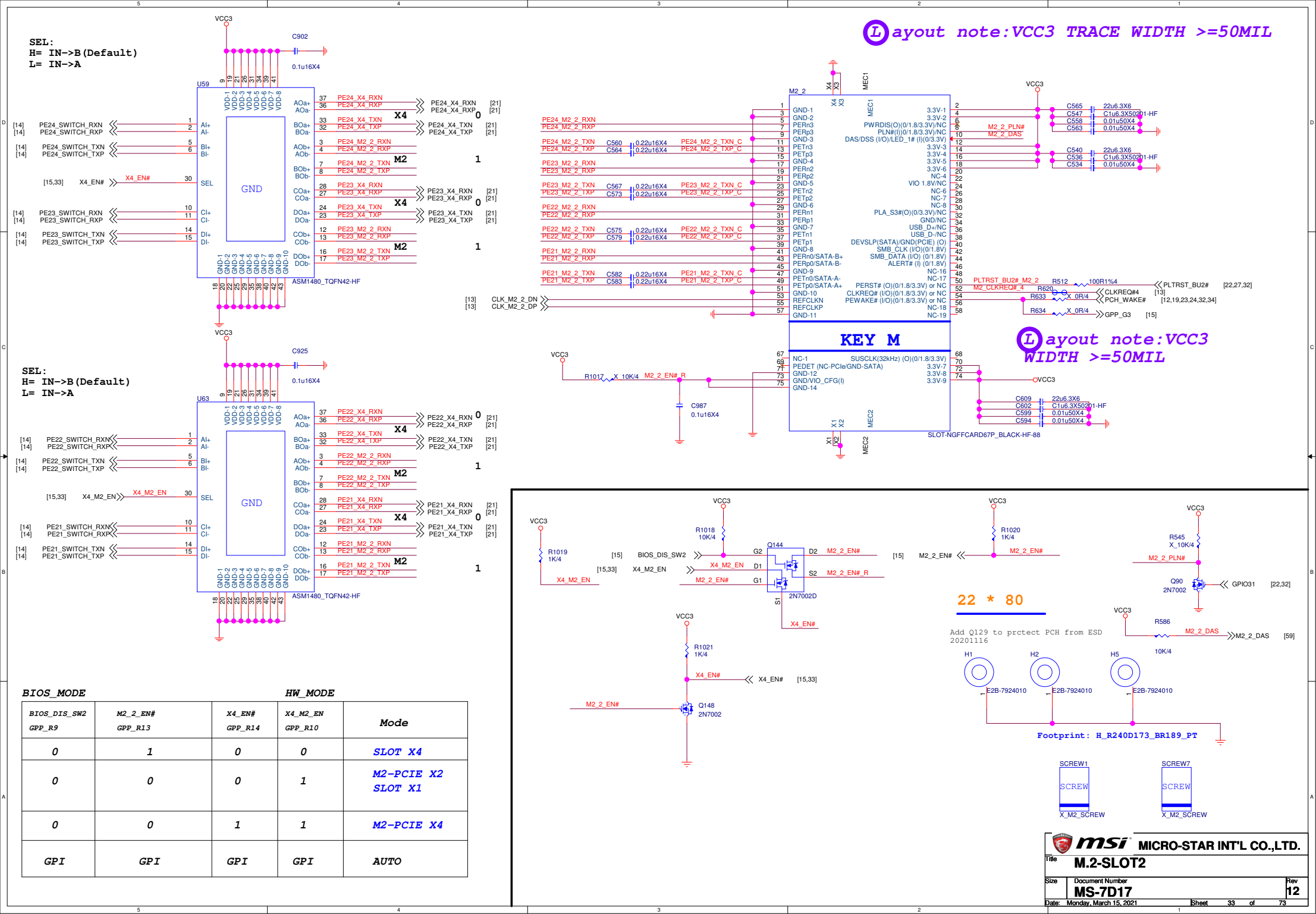
22 * 80





MICRO-STAR INT'L CO.,LTD.

Title	M.2-SLOT1	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 32 of 73	



BIOS_MODE / HW_MODE

BIOS_DIS_SW2 GPP_R9	M2_2_EN# GPP_R13	X4_EN# GPP_R14	X4_M2_EN GPP_R10	Mode
0	1	0	0	SLOT X4
0	0	0	1	M2-PCIE X2 SLOT X1
0	0	1	1	M2-PCIE X4
GPI	GPI	GPI	GPI	AUTO

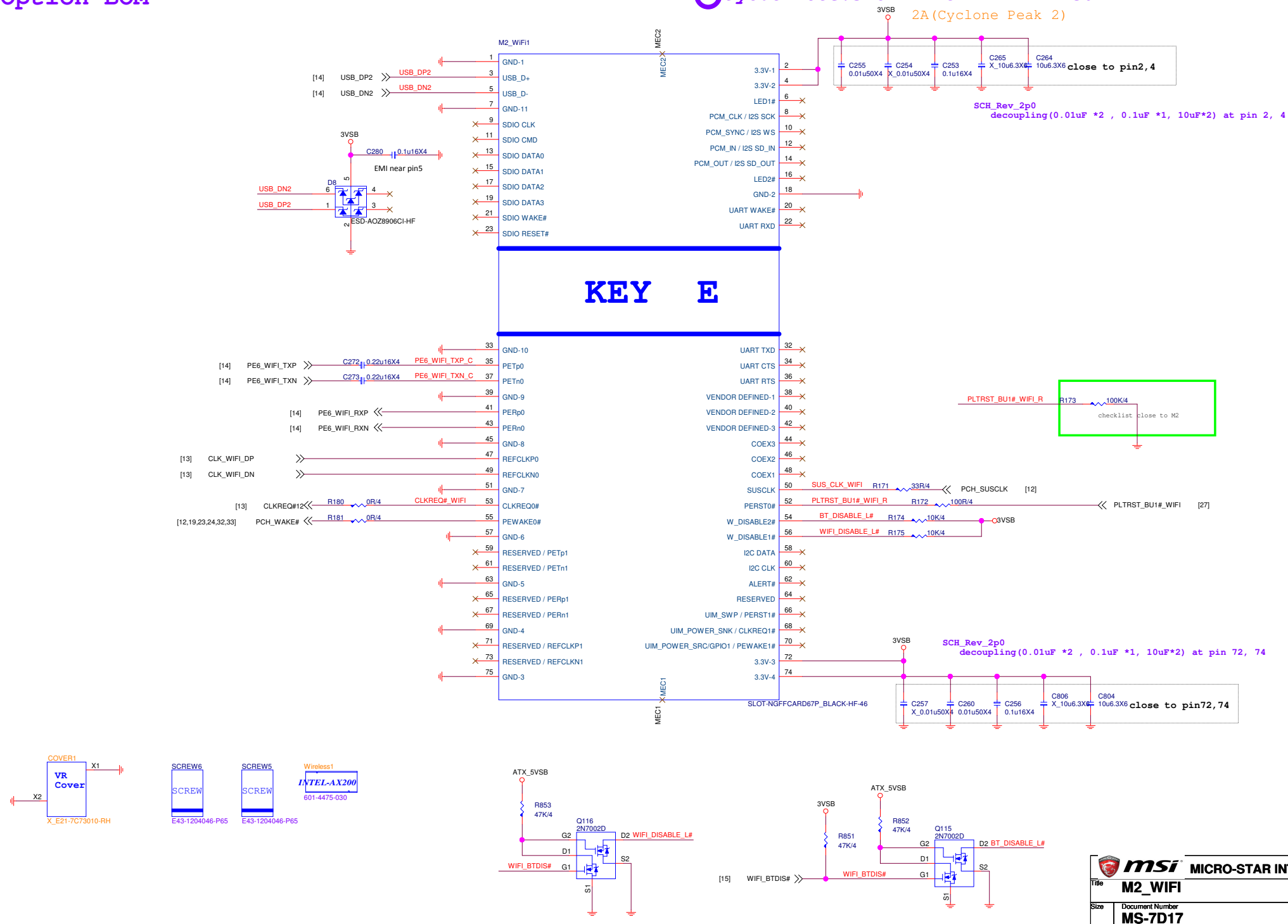
Title	M.2-SLOT2
Size	Document Number: MS-7D17
Rev	12
Date:	Monday, March 15, 2021
Sheet	33 of 73

MICRO-STAR INT'L CO.,LTD.

Option BOM

Layout note:3VSB TRACE WIDTH >=50MIL

2A(Cyclone Peak 2)

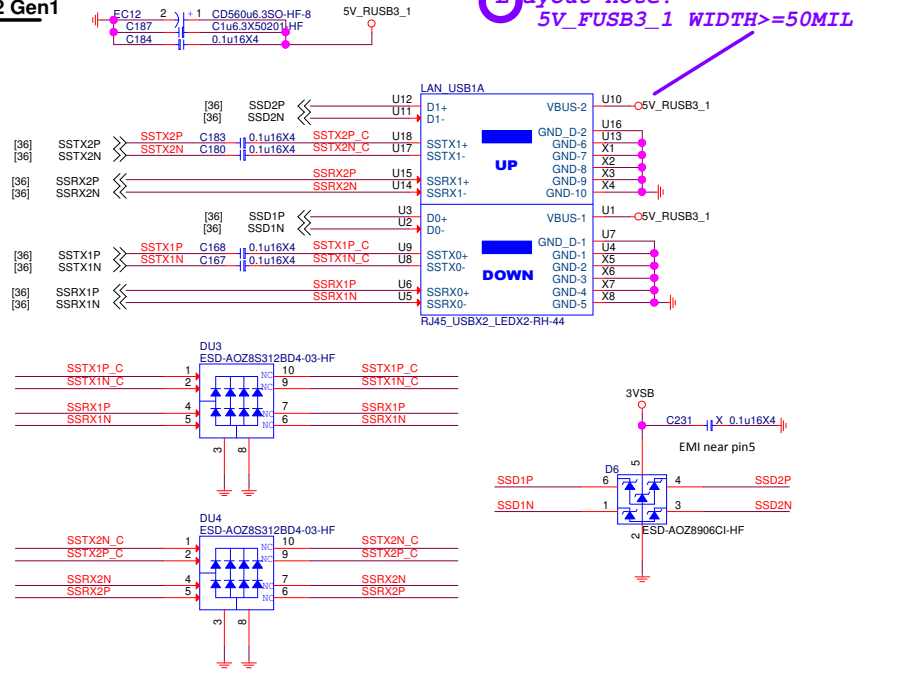


MICRO-STAR INT'L CO.,LTD.

Title	M2_WIFI	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 34 of 73	

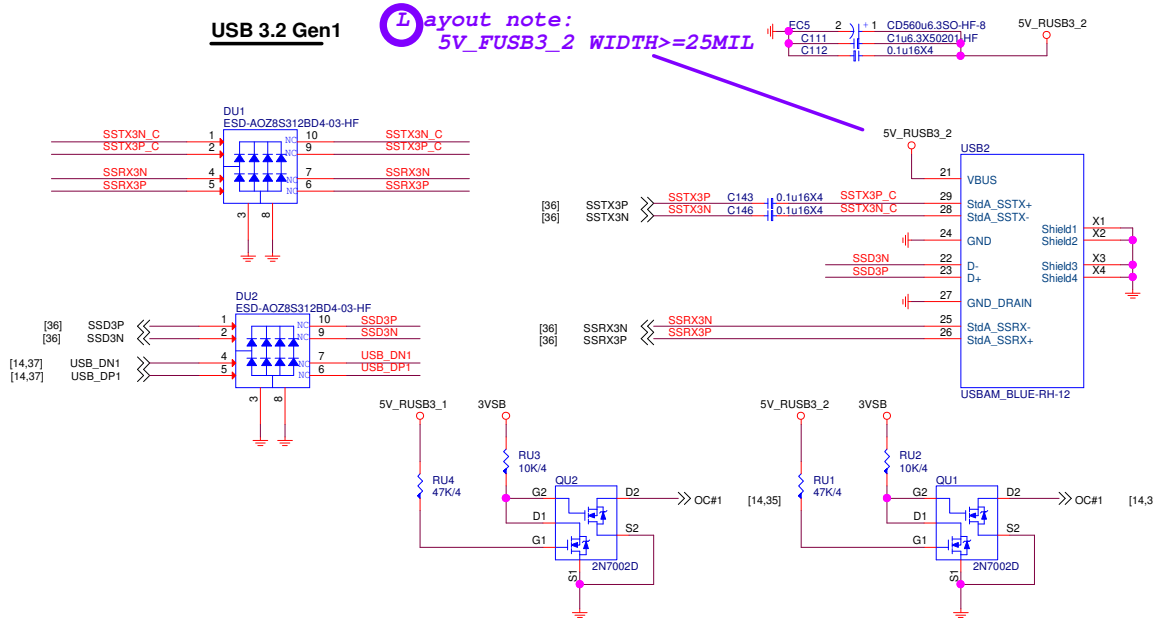
USB 3.2 Gen1

Layout note:
5V_FUSB3_1 WIDTH>=50MIL



USB 3.2 Gen1

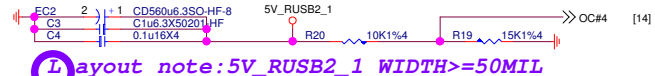
Layout note:
5V_FUSB3_2 WIDTH>=25MIL



GL850G USB2.0 HUB

USB 2.0

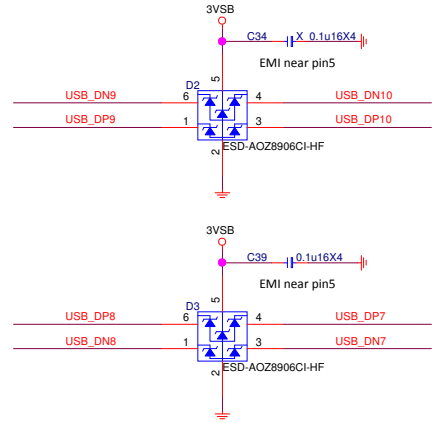
2020/5/29
EC3 is chnaged from C71-56106R1-N07 to C71-56106P1-F70 by PM request

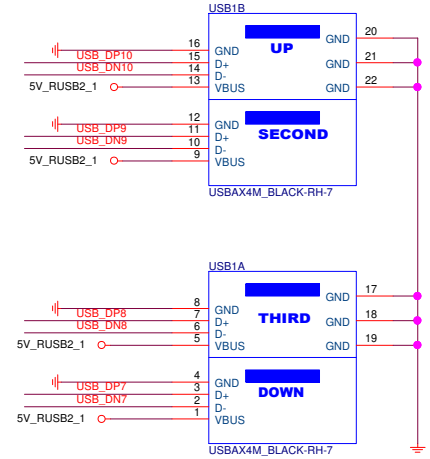


Layout note:5V_RUSB2_1 WIDTH>=50MIL

[14] USB_DP7 — USB_DP7
[14] USB_DN7 — USB_DN7
[14] USB_DP8 — USB_DP8
[14] USB_DN8 — USB_DN8
[14] USB_DP9 — USB_DP9
[14] USB_DN9 — USB_DN9
[14] USB_DP10 — USB_DP10
[14] USB_DN10 — USB_DN10

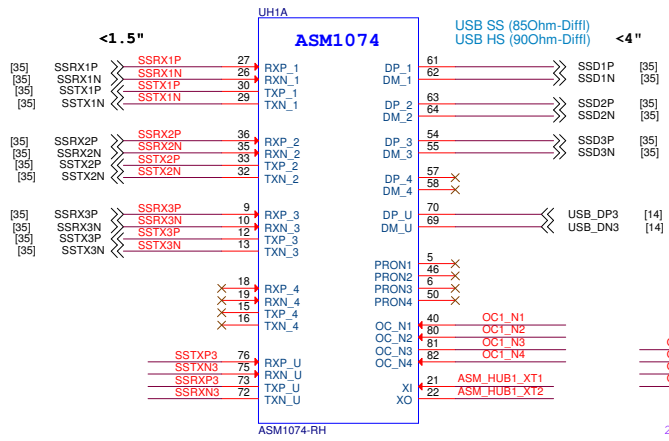
For Cost Down,USB1 direct connect to PCH
Reserve Part Placement space

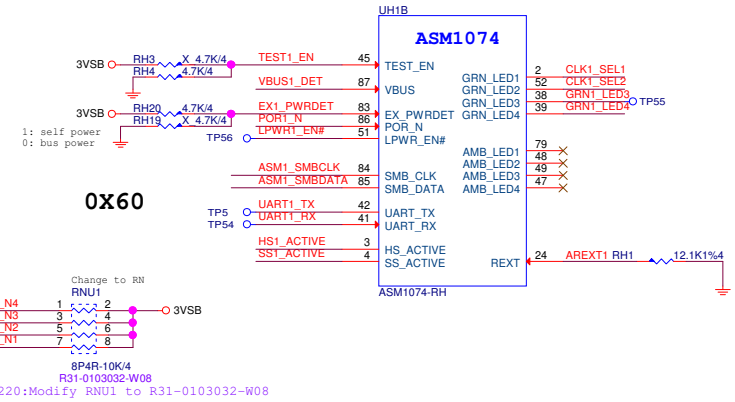


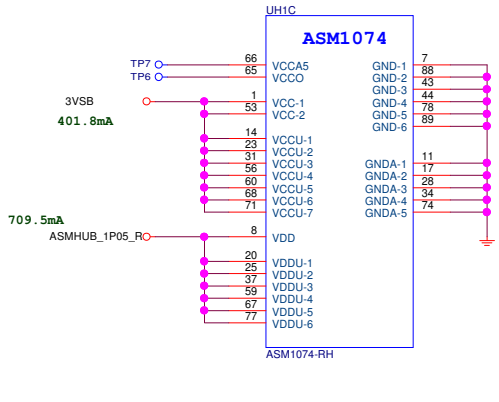


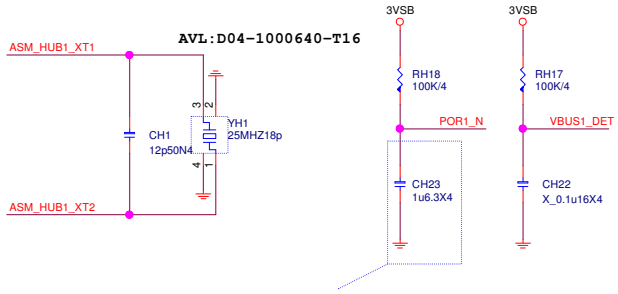
MSI MICRO-STAR INT'L CO.,LTD.

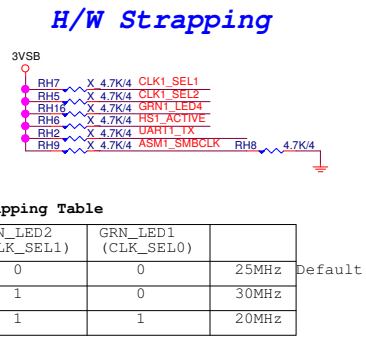
Title	Rear USB	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 35 of 73	

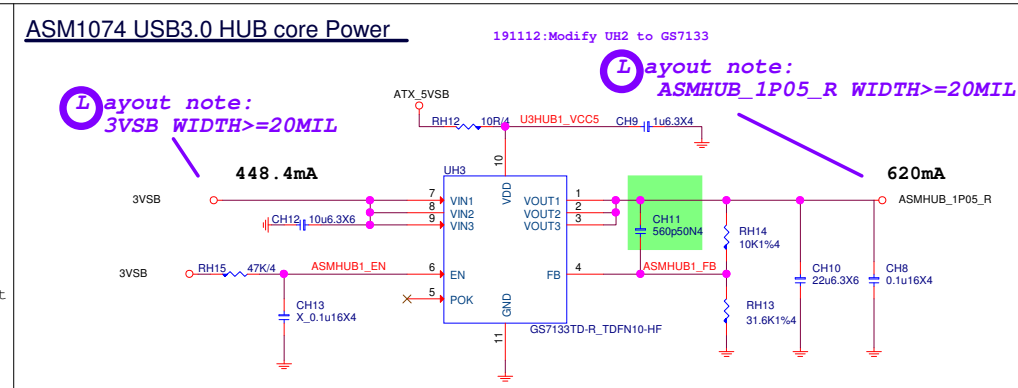


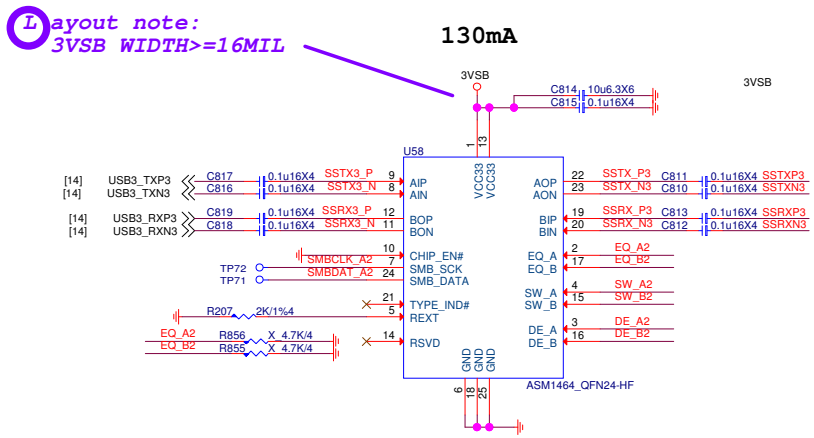


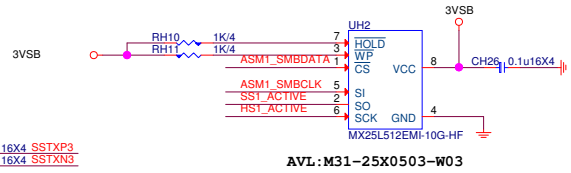


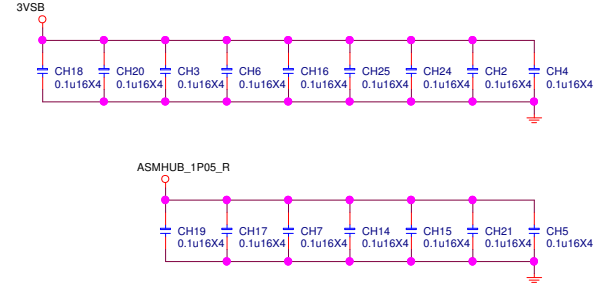












MICRO-STAR INT'L CO.,LTD.

Title: Rear USB 3.1Gen1-HUB

Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 36 of 73

Layout note:
3VSB WIDTH>=30MIL

In diodes,
C723,C727,C728,C731
C715,C717,C719,C721,
C722,C724,C714,C716
change to 0.1uF

Pin9/30 in diodes is power VDD33

Pin20/21 in diodes must connect to IT8851

In diodes,
R832,R826 4.7k
R825,R823 NC

Level Settings

Pin39/40 in diodes is NC

	4-leve Settings	SW	DG
L	0 to GND	900mVppd	1.0dB
R	68K to GND	1100mVppd	-1.5dB
F	NC	1200mVppd	0.0dB
H	0 to VDD	1000mVppd	2.5dB

U56 GL9905
I98-099050C-G08
AVL:OI9-7D06001-G08

R832/R826 Change to 68k to GND
By vendor recommend

Mode SEL

In diodes,
R130,R132,R836,R2833 must pop
R134 must depop

	H	L	F
RXDET_EN	RX enable(default)	RX disable	
I2C_EN	I2C mode	Pin mode(default)	
CTL1/SCL			Pin mode
CTL2/SDA	Pin mode(default)		

OPT_0.1UF_1 X_0.1u16X4
OPT_4.7k_1 X_4.7K/4
C11-1042012-M09
R11-0472012-W08
OPT_200_1 X_PI3EQX2004ZHEX
I98-020040C-D07

Layout note:
5V_RUSBC WIDTH>=80MIL

USB4 USBCSM_BLACK-HF
ESD-AOZ8131DI
T-type

close to USB3 Connector

U57 U55 ESD-AOZ8S312BD4-03-HF

U17 IT8851FN
B07-088510C-I15
AVL:OB7-7D08001-I15

H:3A under S0 mode
L:1.5A under S3, S5 mode

VCONN request 500mA

Layout note:
5V_RUSB WIDTH>=80MIL

U15 RT9742AGJ5F

> 80mil.
3A

Only for FRS

if length too much , can use 0.1u solution.
test pass can remove.

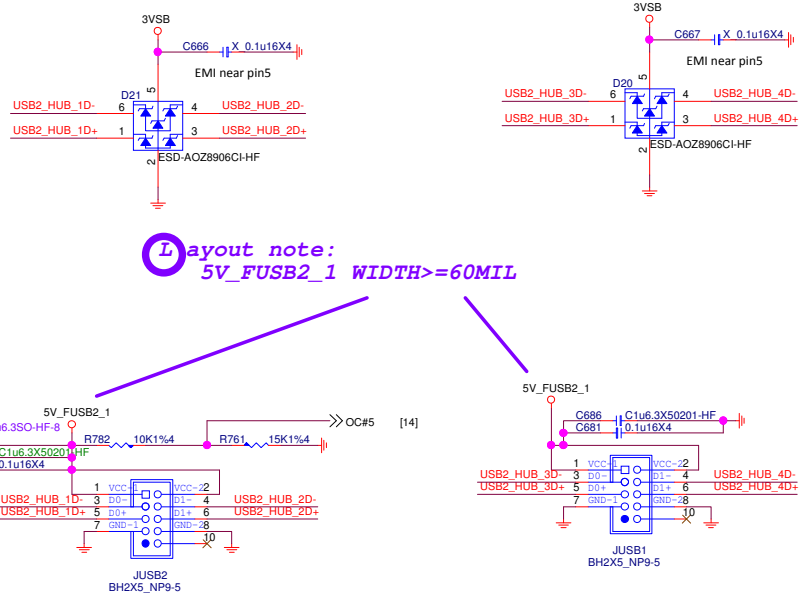
MICRO-STAR INT'L CO.,LTD.

Title: Rear USB 3.2 Gen1 Type C

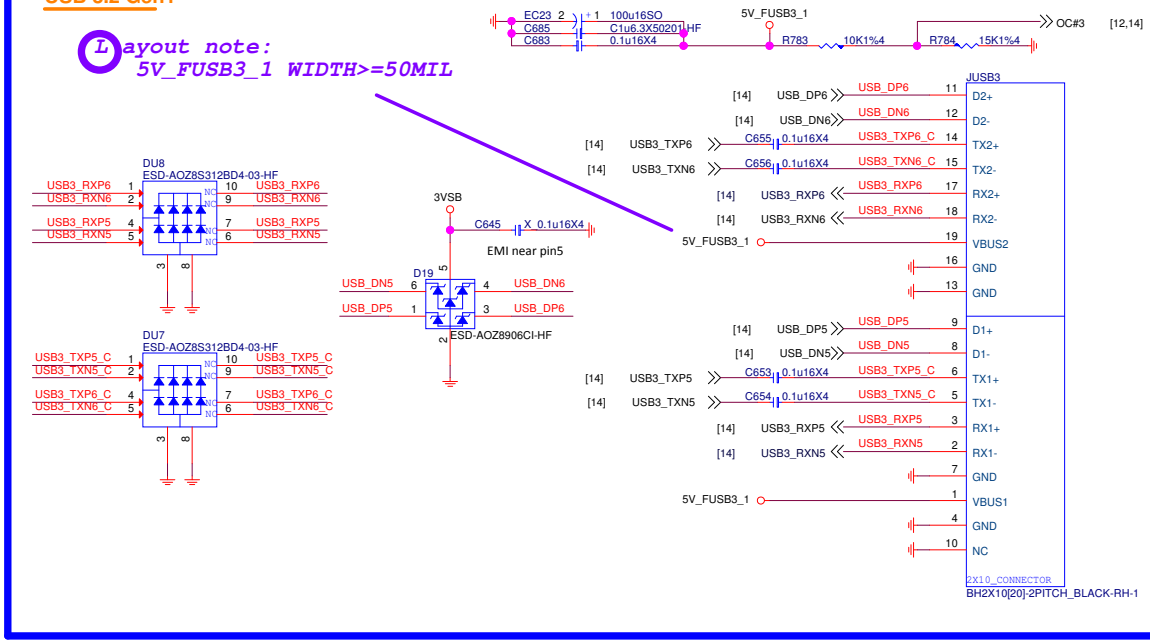
Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 37 of 73

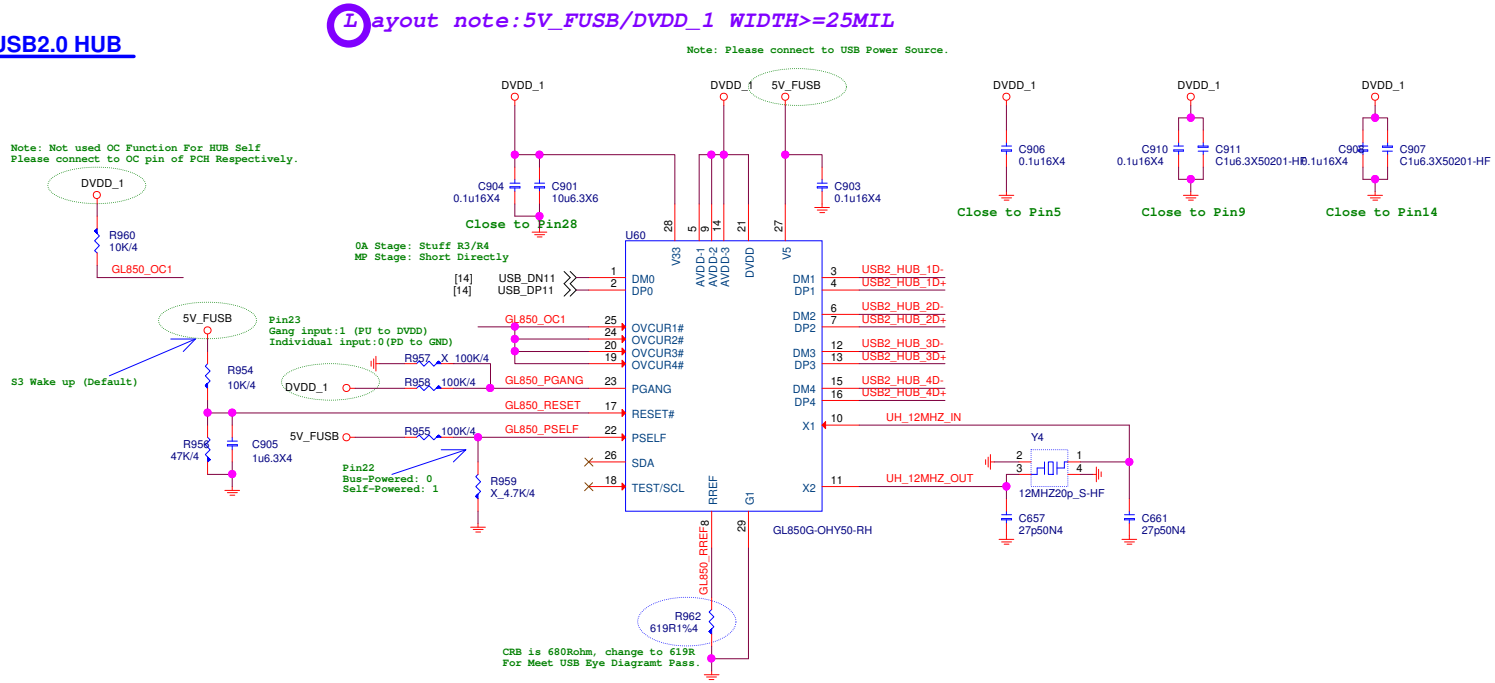
USB 2.0



USB 3.2 Gen1



GL850G USB2.0 HUB

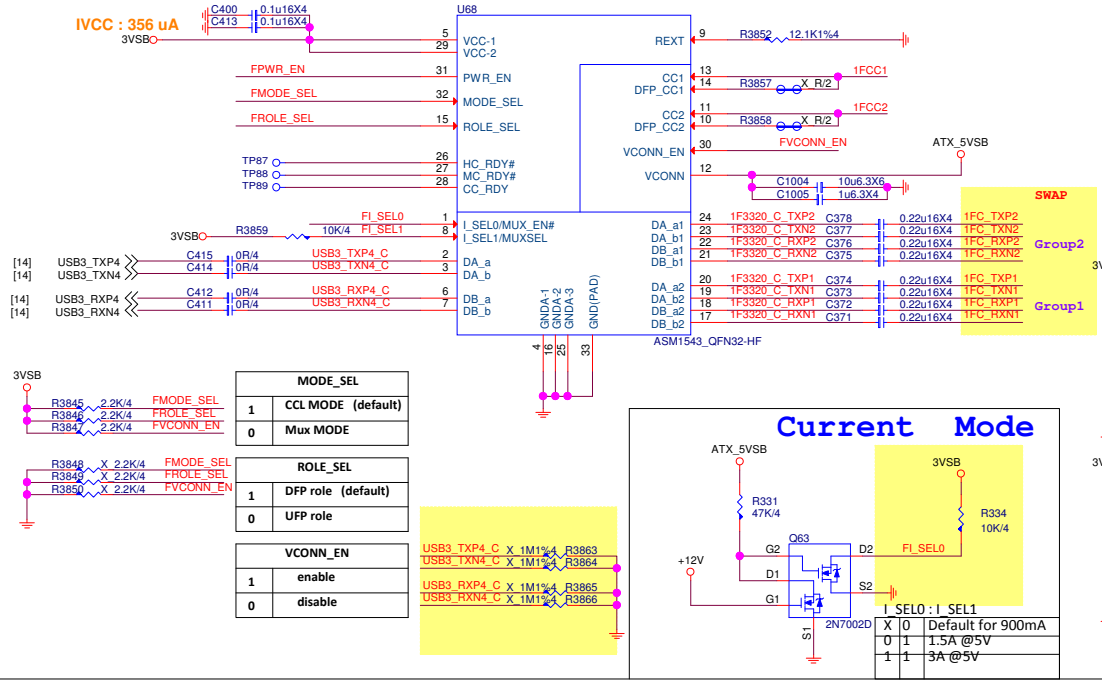


MICRO-STAR INT'L CO.,LTD.

Title	FUSB 3.2 G1/GL850 USB2.0 Hub	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 38 of 73	

USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

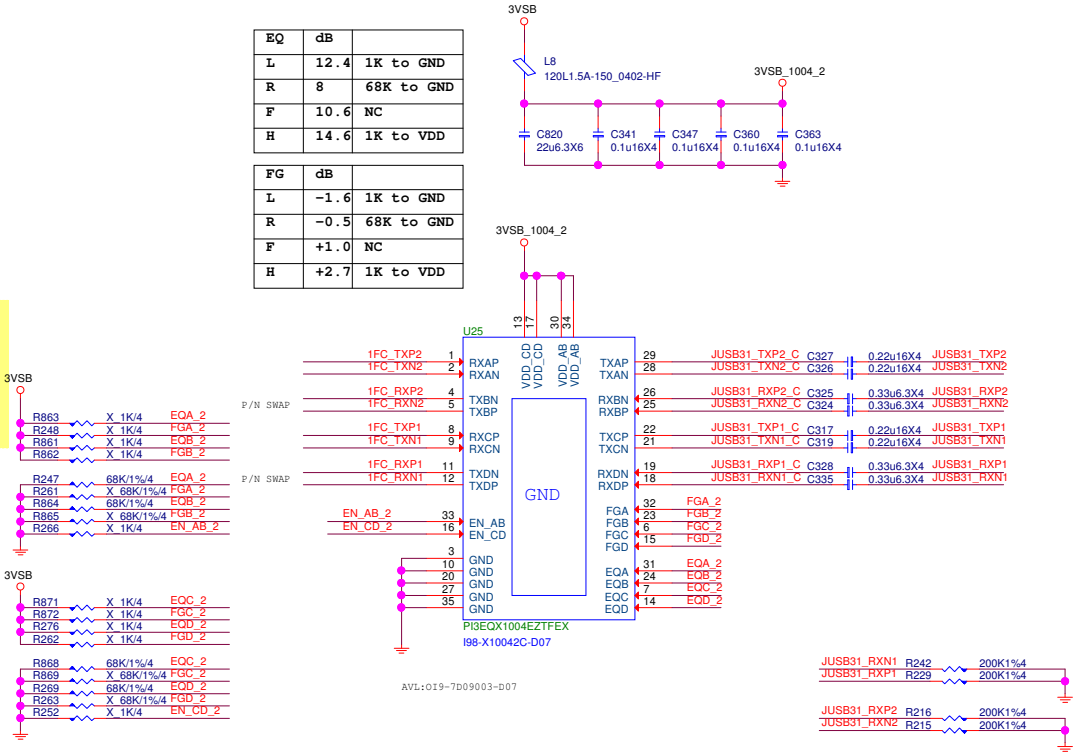
VCONN_EN	
1	enable
0	disable

Current Mode

I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

EQ	dB	
L	12.4	1K to GND
R	8	68K to GND
F	10.6	NC
H	14.6	1K to VDD

FG	dB	
L	-1.6	1K to GND
R	-0.5	68K to GND
F	+1.0	NC
H	+2.7	1K to VDD



VBUS EN

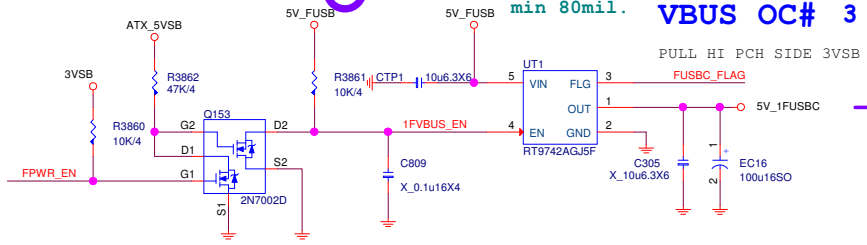
Layout note: 5V_1FUSBC WIDTH>=80MIL

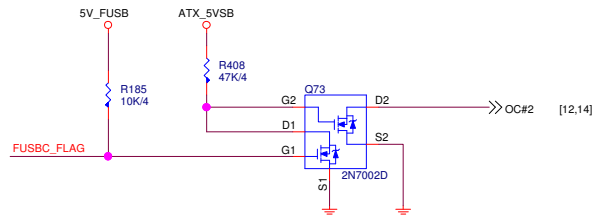
Layout note: 5V_FUSB WIDTH>=80MIL

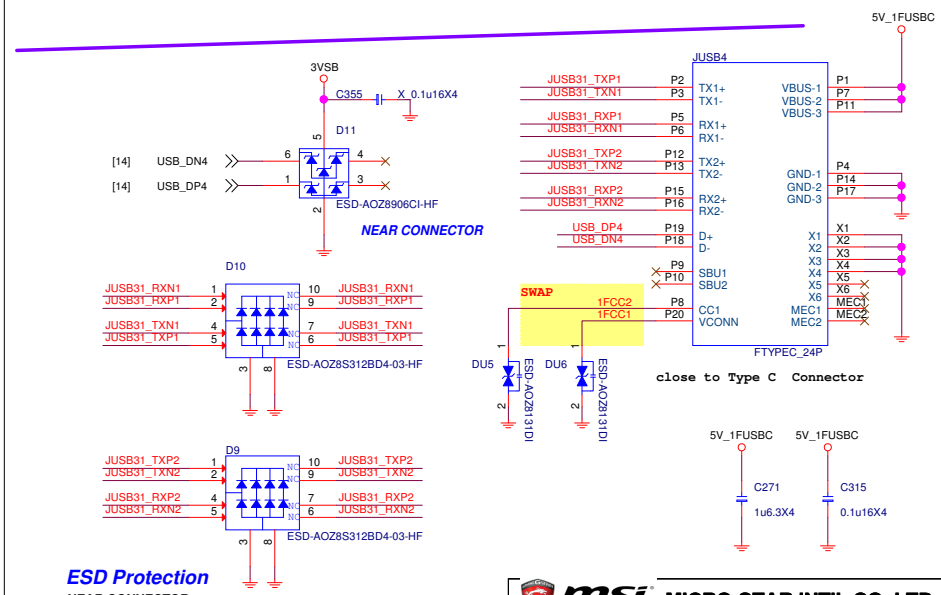
min 80mil.

VBUS OC# 3 A

PULL HI PCH SIDE 3VSB

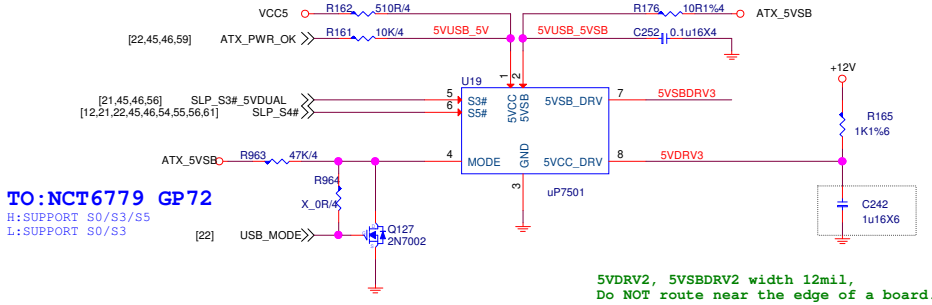






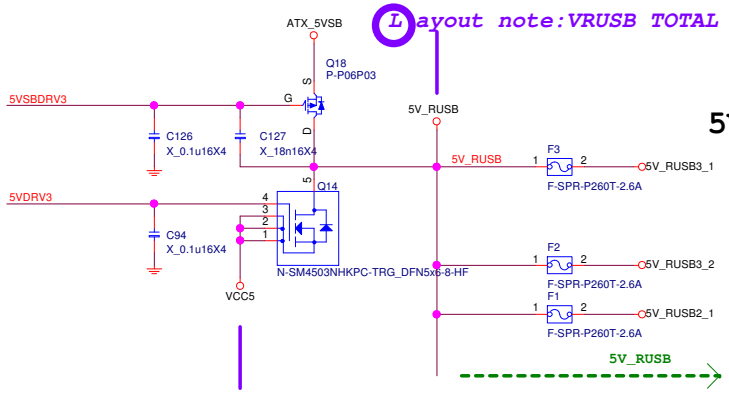
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Front USB 3.2 Gen 1 Type C	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 39 of 73	

USB POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

REAR USB PORT POWER



Layout note:VRUSB TOTAL WIDTH>=200mil

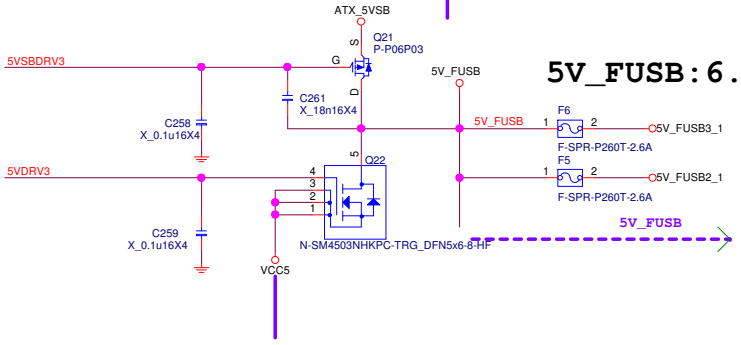
5V_RUSB:7.7A

LAN_USB1A - 1.8A	Layout note:5V_RUSB to 5V_RUSB3_1 WIDTH>=50MIL
USB1 - 0.9A	Layout note:5V_RUSB to 5V_RUSB3_2 WIDTH>=25MIL
PS2_USB1 - 2A	Layout note:5V_RUSB to 5V_RUSB2_1 WIDTH>=50MIL
USB2 - 3A	Layout note:5V_RUSB to U11 WIDTH>=80mil

Layout note:VCC5 to 5V_RUSB WIDTH>=200mil

FRONT USB PORT POWER

Layout note:VRUSB TOTAL WIDTH>=170mil



5V_FUSB:6.8A

JUSB3 - 1.8A	Layout note:5V_FUSB to 5V_FUSB3_1 WIDTH>=50MIL
JUSB1+JUSB2 - 2A	Layout note:5V_FUSB to 5V_FUSB2_1 WIDTH>=60MIL
JUSB4 - 3A	Layout note:5V_FUSB to UT1 WIDTH>=80MIL

Layout note:VCC5 to 5V_FUSB WIDTH>=170mil

MICRO-STAR INT'L CO.,LTD.

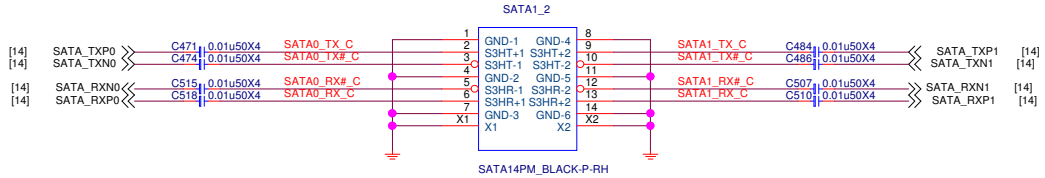
Title: USB /PS2 Power

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 40 of 73

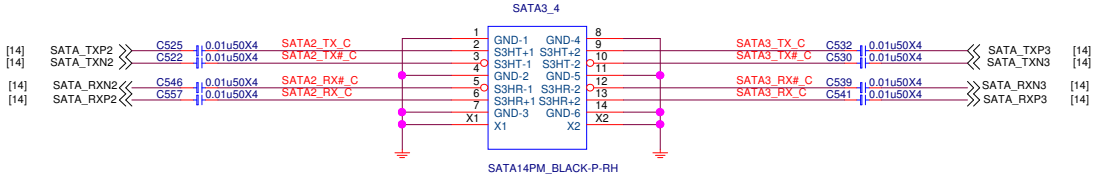
SATA PORT 0,1

Black 90 degree



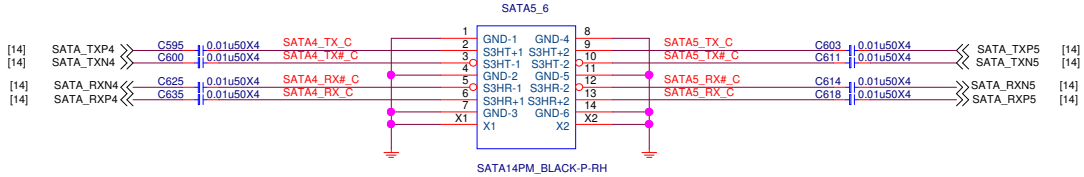
SATA PORT 2,3

Black 90 degree



SATA PORT 4,5

Black 90 degree



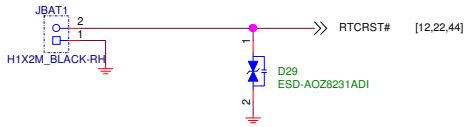
MICRO-STAR INT'L CO.,LTD.

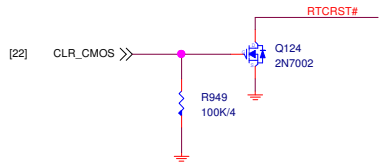
Title: SATA connector

Size: | Document Number: MS-7D17 | Rev: 12

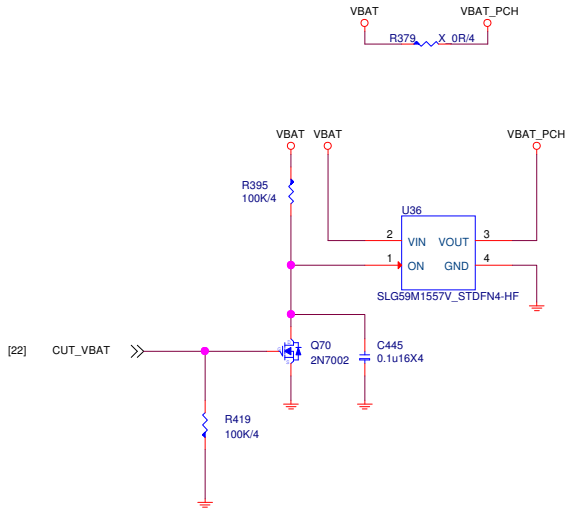
Date: Monday, March 15, 2021 | Sheet 41 of 73

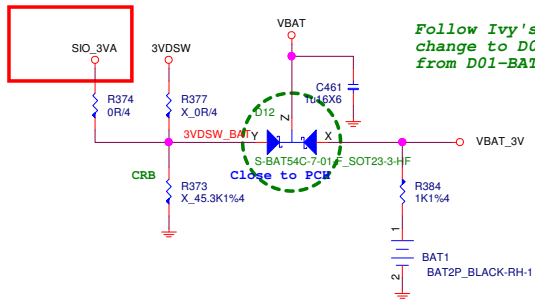
CUT_VBAT/CLR_CMOS





VBAT



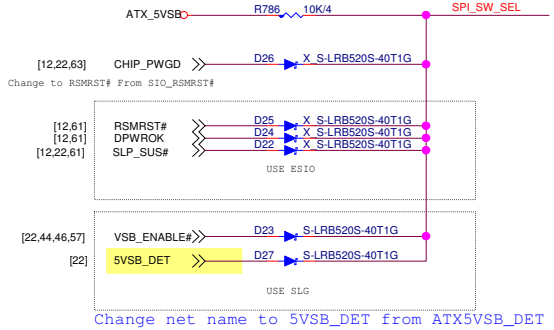


Follow Ivy's AVL table recomend
change to D01-BAT54H9-N47
from D01-BAT54H9-D07

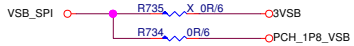
MICRO-STAR INT'L CO.,LTD.

Title	VBAT Circuit	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 42 of 73	

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

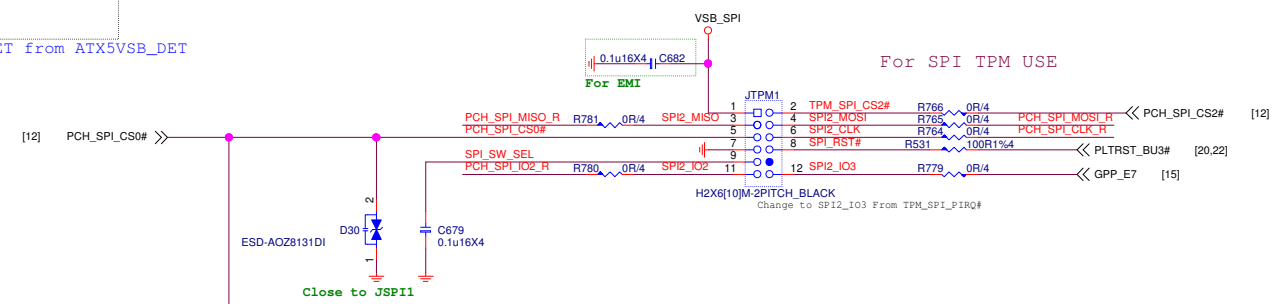


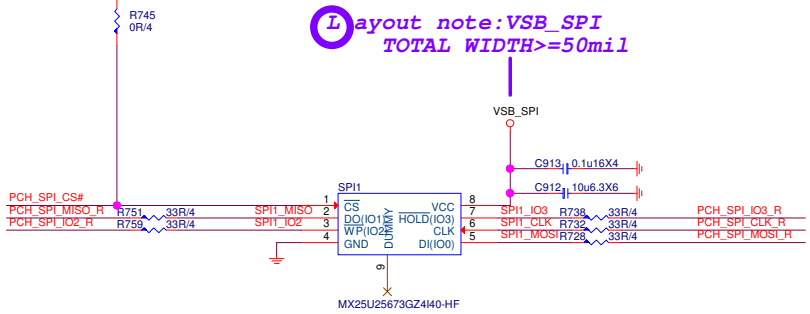
Change net name to 5VSB_DET from ATX5VSB_DET
20111116



Layout note:VSB_SPI
TOTAL WIDTH>=50mil

For SPI TPM USE





AVL:M31-2525620-W03

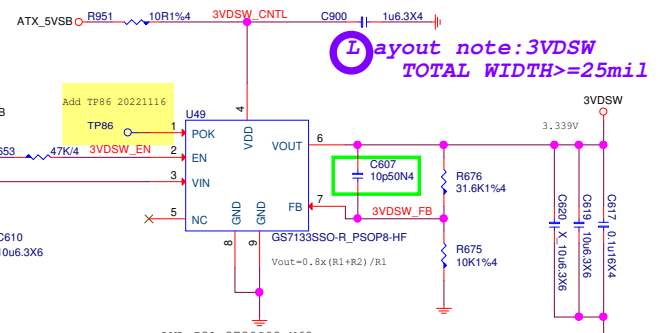
MICRO-STAR INT'L CO.,LTD.

Title: BIOS ROM

Size | Document Number: MS-7D17 | Rev: 12

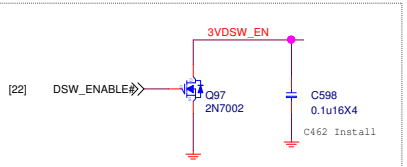
Date: Monday, March 15, 2021 | Sheet 43 of 73

3VDSW



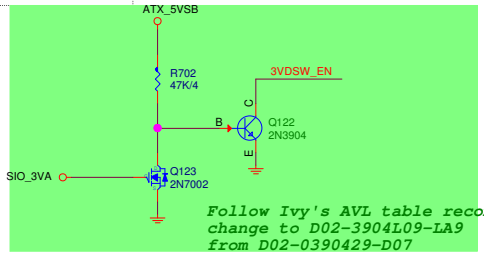
Layout note:3VDSW
TOTAL WIDTH>=25mil

Layout note:ATX_5VSB
TOTAL WIDTH>=25mil



Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.113
=1.7*0.113
=0.1921W < 1.33W

OUT 3.3V/0.113A
IN 5V/0.113A



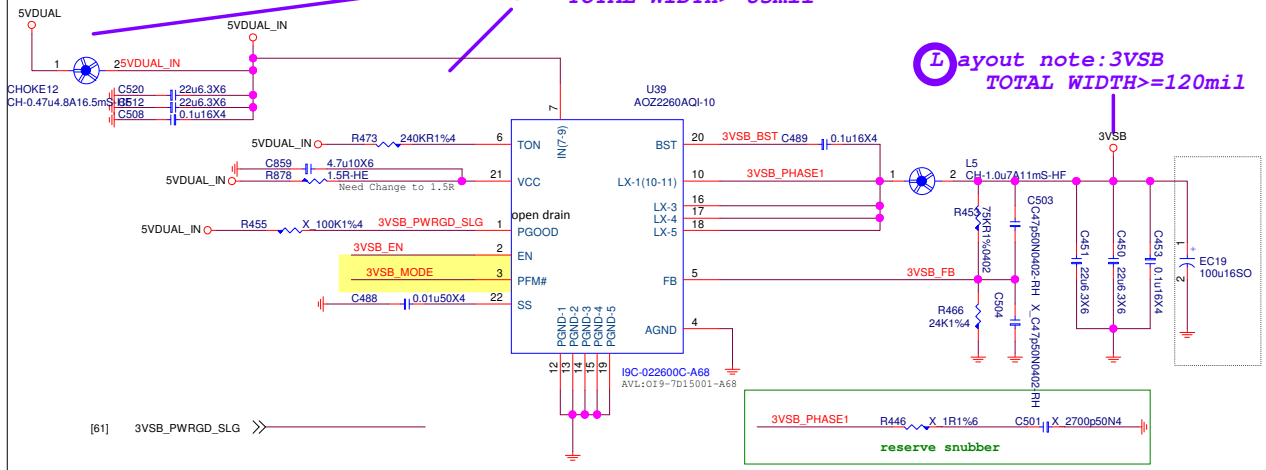
Follow Ivy's AVL table recomend
change to D02-3904L09-LA9
from D02-0390429-D07

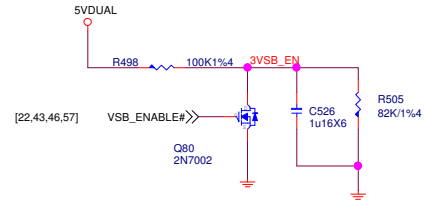
SYS_3VSB

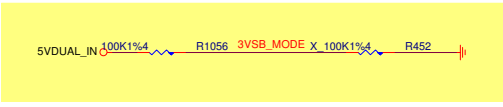
OUT 3.3V/5.05A
IN 5V/3.4A

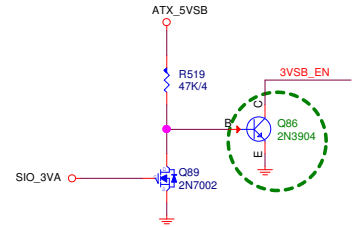
Layout note:5VDUAL_IN/5VDUAL
TOTAL WIDTH>=85mil

Layout note:3VSB
TOTAL WIDTH>=120mil







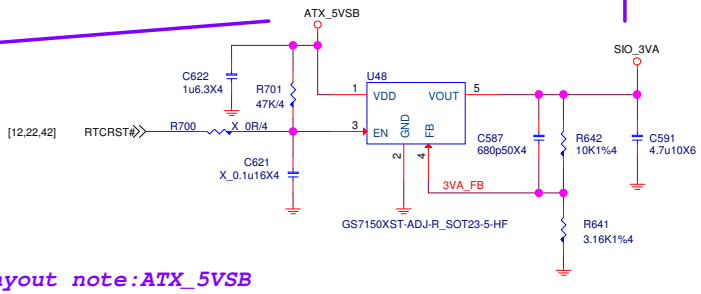


For S5-G3 3VSB EN issue

Follow Ivy's AVL table recomend
change to D02-3904L09-LA9
from D02-0390429-D07

SIO_3VA

Layout note:SIO_3VA
TOTAL WIDTH>=25mil



Layout note:ATX_5VSB
TOTAL WIDTH>=25mil

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.113
=1.7*0.113
=0.1921W < 1.33W

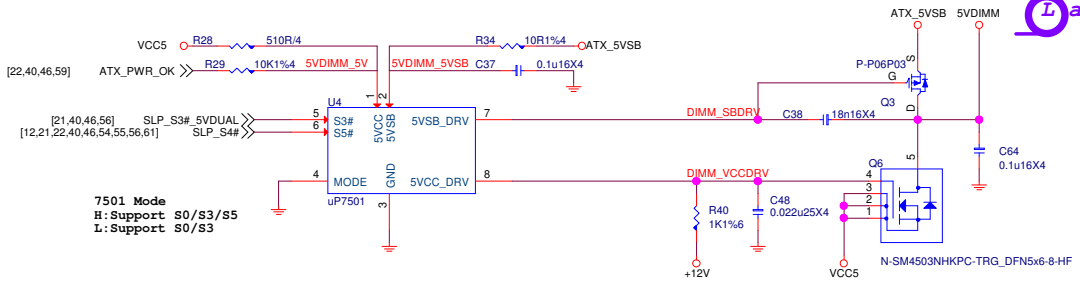
MICRO-STAR INT'L CO.,LTD		
MS-7D17		
Size: Custom	Document Description: SYSTEM POWER	Rev: 12
Date: Monday, March 15, 2021	Sheet 44 of 73	

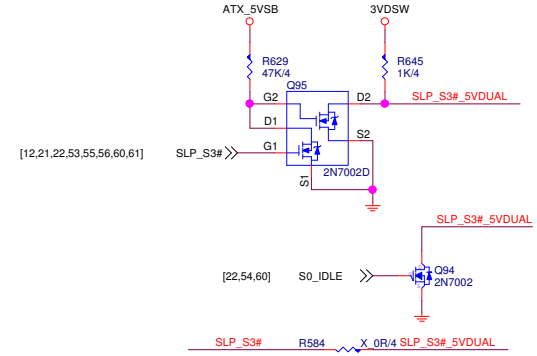
5VDIMM FOR DDR 5V/7.6A

Layout note:ATX_5VSB WIDTH>=50mil

S0IX

Layout note:+5VDIMM/VCC5 WIDTH>=200mil





5VDIMM COLAY

MICRO-STAR INT'L CO.,LTD

MS-7D17

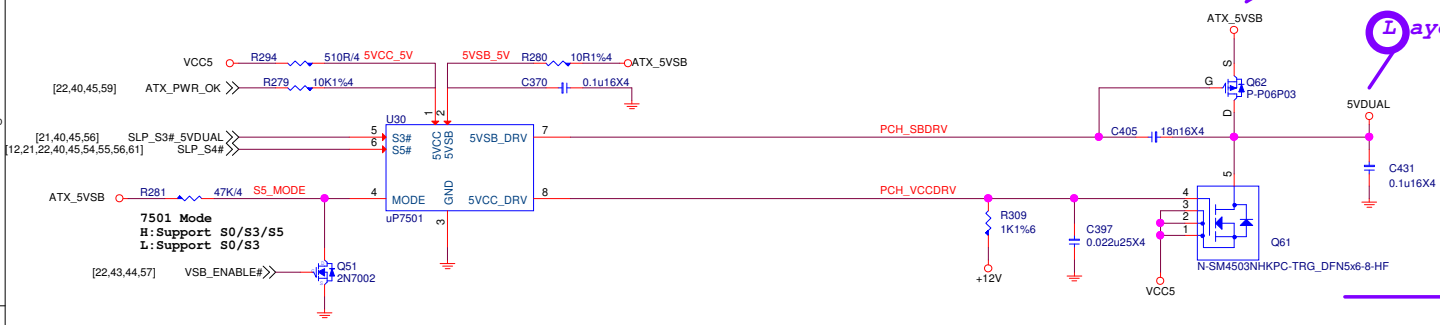
Size	Document Description	Rev
Custom	M.2_2-SLOT2	12

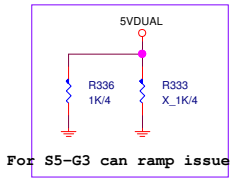
Date: Monday, March 15, 2021 Sheet 45 of 73

5VDUAL 5V/10.44A

L ayout note:5VSB TOTAL WIDTH>=50mil

L ayout note:5VDUAL/VCC5 TOTAL WIDTH>=270mil



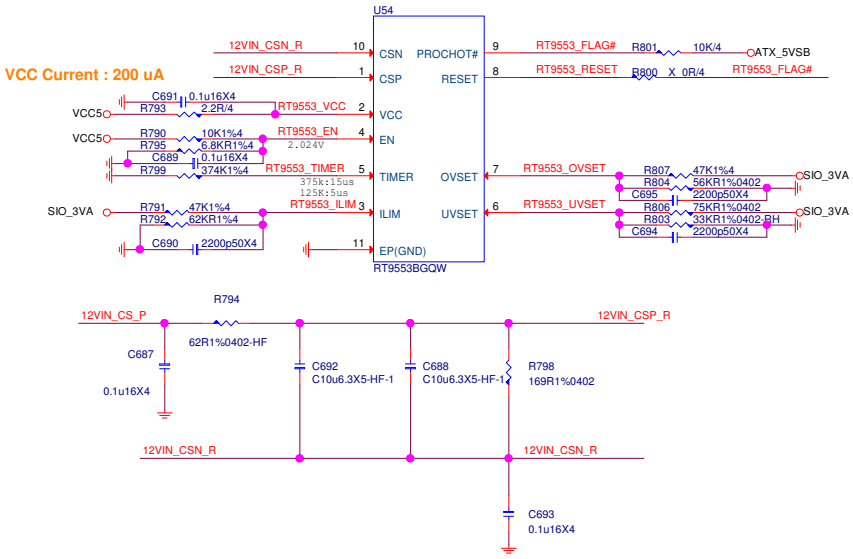


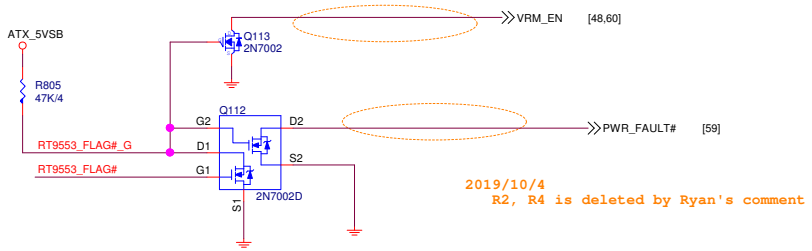
For S5-G3 can ramp issue

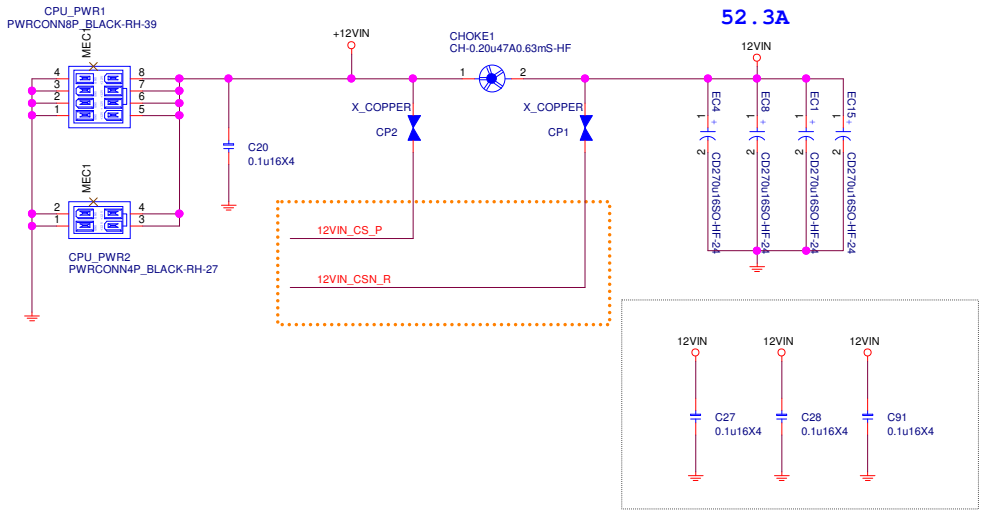
200302:un-stuff R419&R420

MICRO-STAR INT'L CO.,LTD		
MS-7D17		
Size: Custom	Document Description: PCIE SWITCH	Rev: 12
Date: Monday, March 15, 2021	Sheet 46 of 73	

OCP: 45A For 8 core 245A Support







D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.72	> output Vcore
D	=	0.143333	

I o = Icore(max)*0.8			
I core(max)	=	245	> Vcore current
I avg.	=	196	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	12	phase
I ripple	=	5.723403	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE$_{TEMP}$	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	55	> Vcore current
I avg.	=	44	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	7.317182	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE$_{TEMP}$	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.05	> output Vcore
D	=	0.0875	

I o = Icore(max)*0.8			
I core(max)	=	22.1	> Vcore current
I avg.	=	17.68	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	4.995773	A

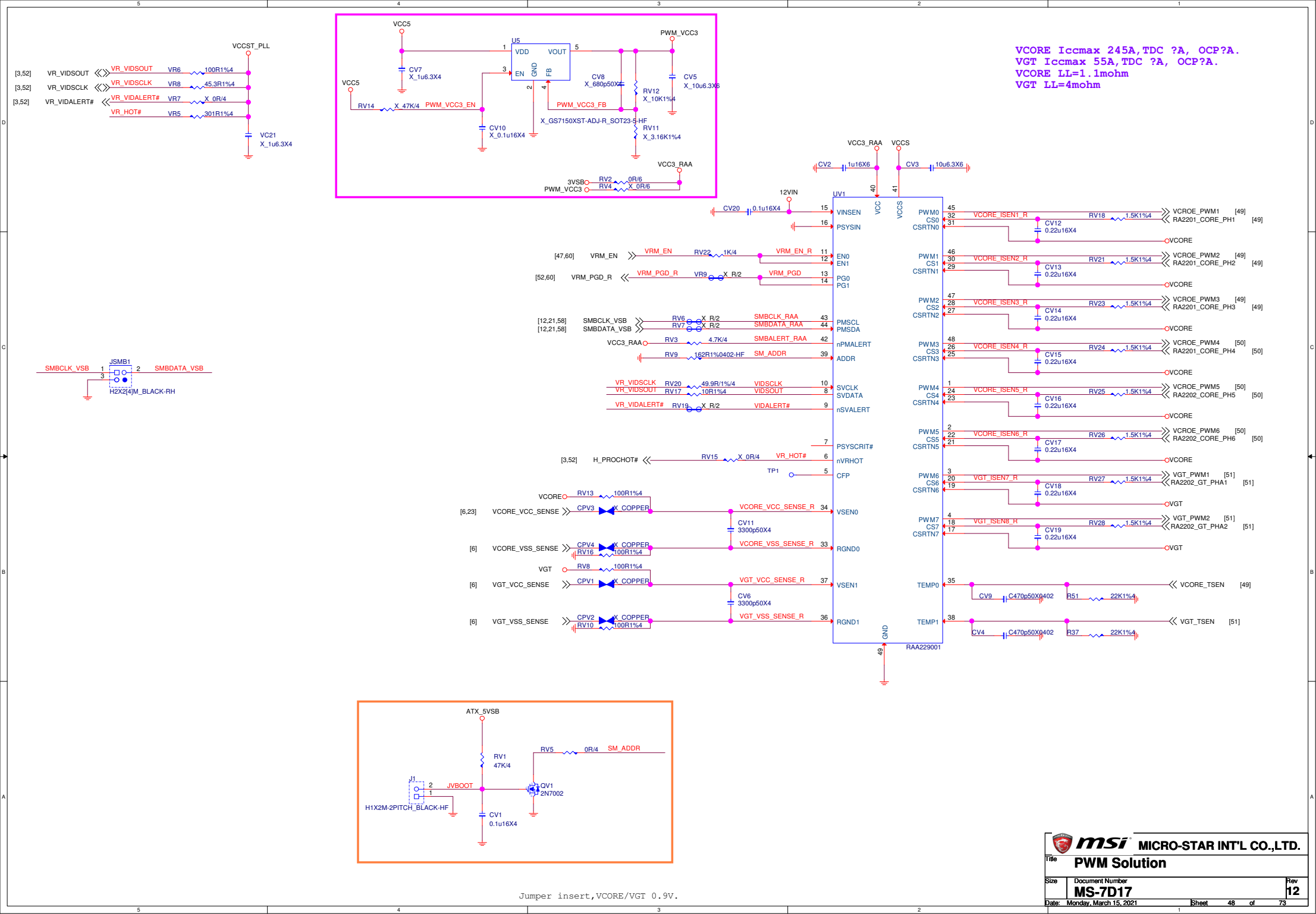
How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE$_{TEMP}$	=	1	
Input Cap.	=	1	pcs.

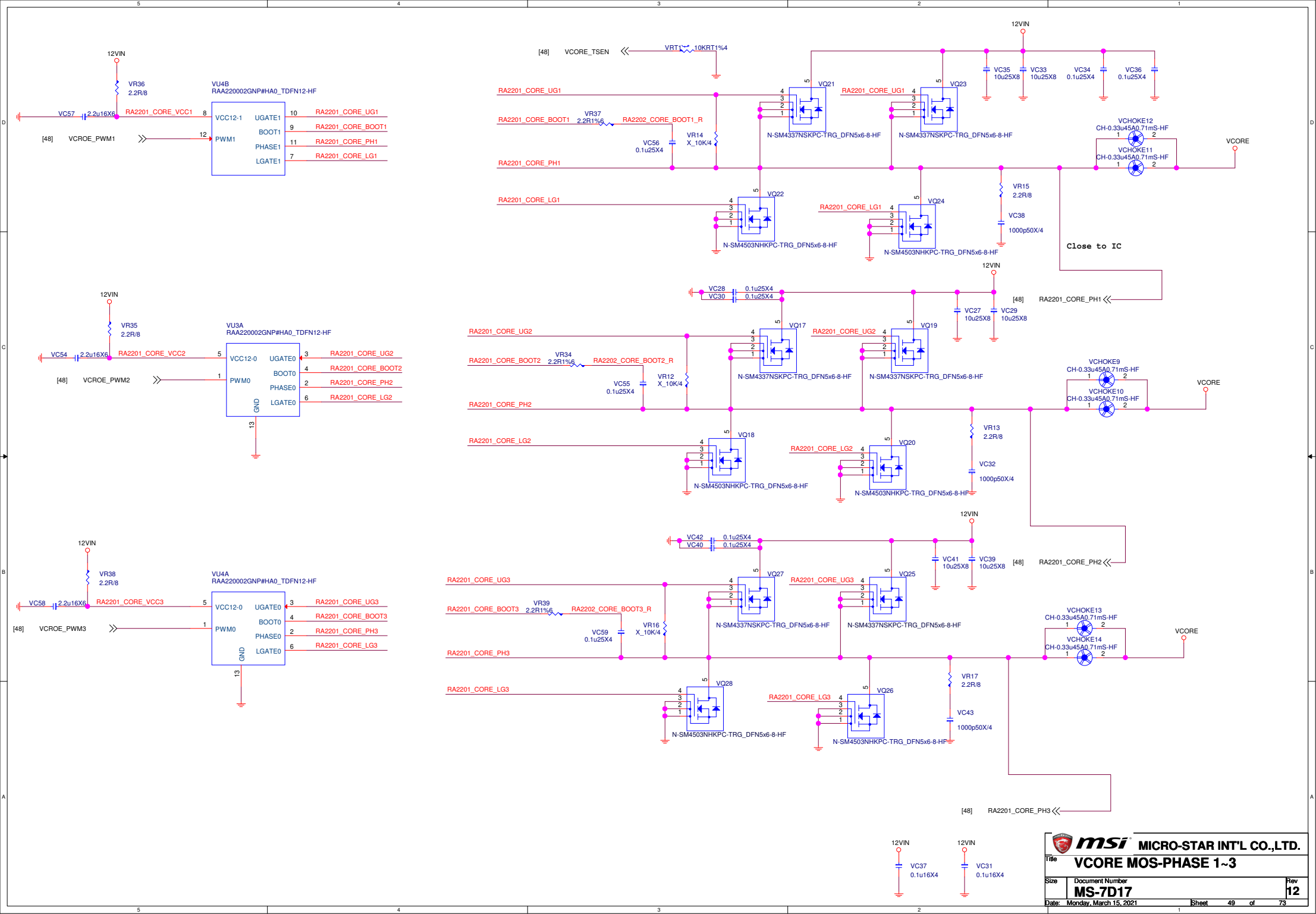
MICRO-STAR INT'L CO.,LTD.

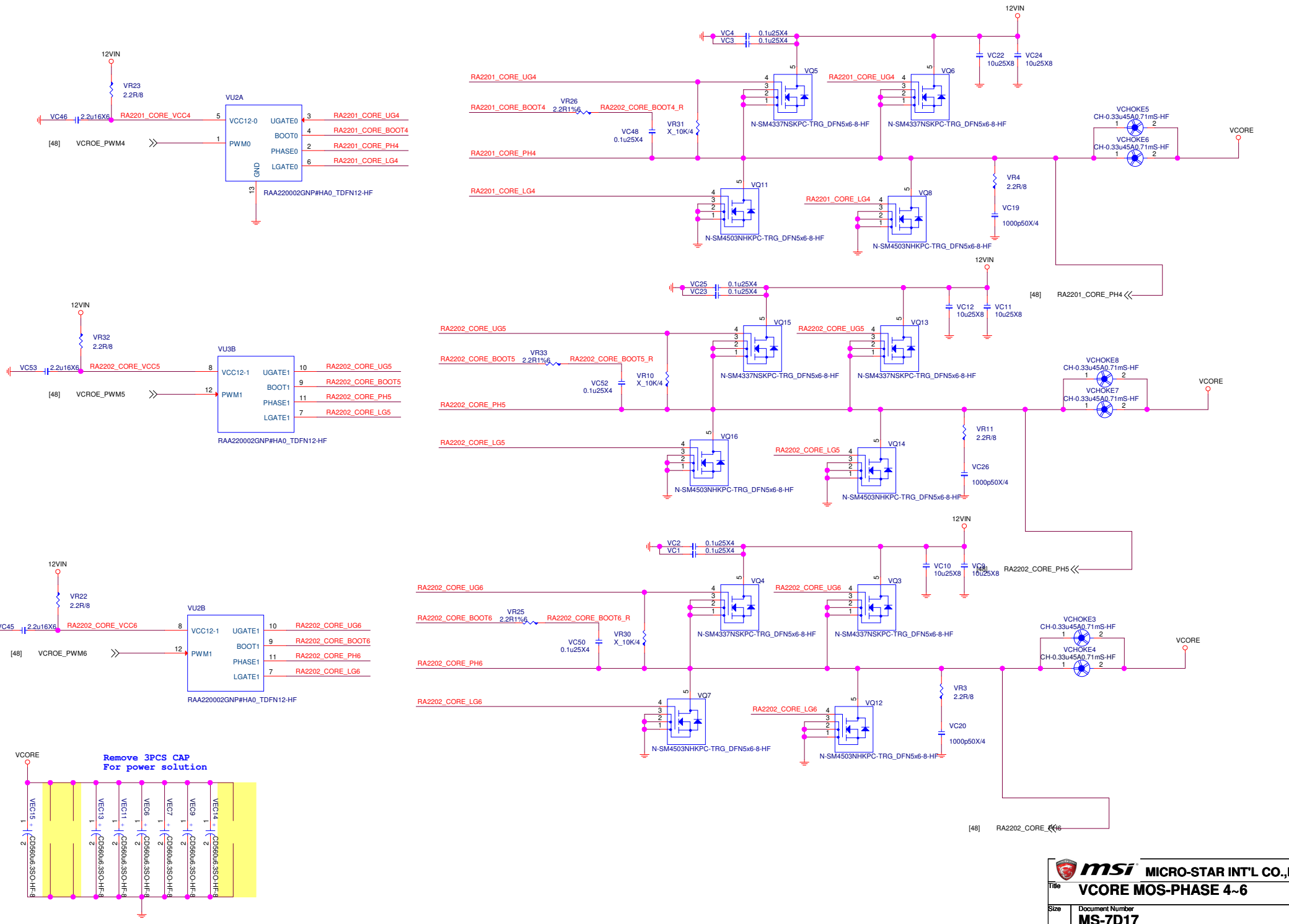
Title: 12VIN/CURRENT SENSE-RT9553

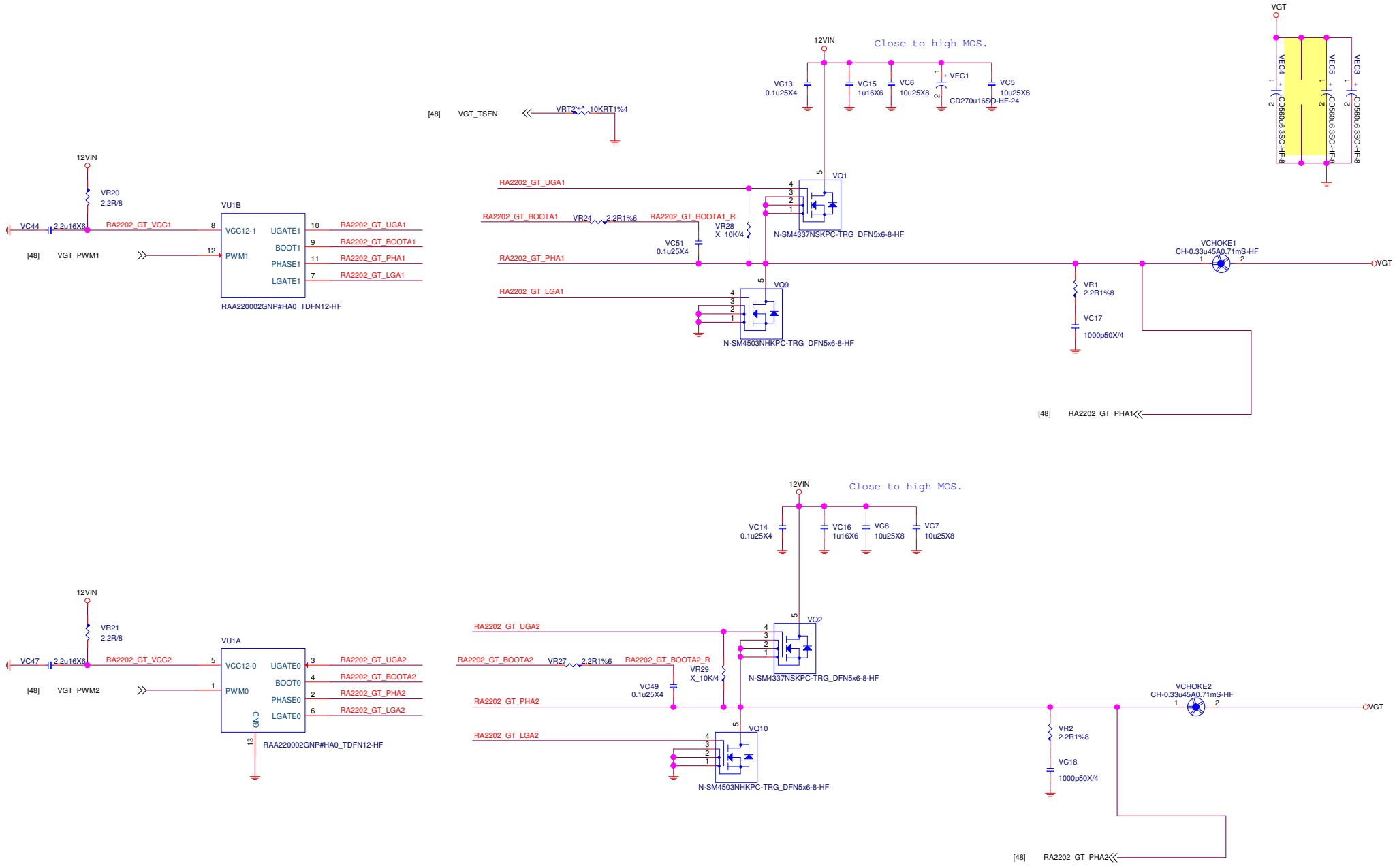
Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 47 of 73


VCORE Iccmax 245A,TDC ?A, OCP?A.
VGT Iccmax 55A,TDC ?A, OCP?A.
VCORE LL=1.1mohm
VGT LL=4mohm
VCCST_PLL
VR_VIDSOUT
VR_VIDSCLK
VR_VIDALERT#
VR_HOT#
VC21 X_1u6.3X4
VCC5
PWM_VCC3
U5 VDD VOUT EN GND FB
CV7 X_1u6.3X4
CV8 X_680p50X
CV5 X_10u6.3X6
RV12 X_10K1%4
RV14 X_47K/4
PWM_VCC3_EN
PWM_VCC3_FB
CV10 X_0.1u16X4
X_GS7150XST-ADJ-R_SOT23-5-HF
RV11 X_3.16K1%4
VCC3_RAA
3VSB
RV2 0R/6
RV4 X_0R/6
VCC3_RAA
VCCS
CV2 1u16X6
CV3 10u6.3X6
12VIN
UV1
CV20 0.1u16X4
VINSEN
PSYSIN
VRM_EN
VRM_EN_R
RV22 1K/4
EN0
EN1
VRM_PGD_R
RV9 X_R/2
PG0
PG1
SMBCLK_VSB
SMBDATA_VSB
SMBCLK_RAA
SMBDATA_RAA
PMSCL
PMSDA
SMBALERT_RAA
nPMALERT
RV3 4.7K/4
RV9 162R1%0402-HF
SM_ADDR
ADDR
VR_VIDSCLK
VR_VIDSOUT
RV20 49.9R/1%/4
RV17 10R1%4
VIDSCLK
VIDSOUT
SVCLK
SVDATA
VR_VIDALERT#
RV19 X_R/2
VIDALERT#
nSVALERT
PSYSCRIT#
H_PROCHOT#
RV15 X_0R/4
VR_HOT#
nVRHOT
TP1
CFP
VCORE
RV13 100R1%4
VCORE_VCC_SENSE
CPV3 X_COPPER
VCORE_VCC_SENSE_R
VSEN0
CV11 3300p50X4
VCORE_VSS_SENSE
CPV4 X_COPPER
RV16 100R1%4
VCORE_VSS_SENSE_R
RGND0
VGT
RV8 100R1%4
VGT_VCC_SENSE
CPV1 X_COPPER
VGT_VCC_SENSE_R
VSEN1
CV6 3300p50X4
VGT_VSS_SENSE
CPV2 X_COPPER
RV10 100R1%4
VGT_VSS_SENSE_R
RGND1
GND
RAA229001
PWM0 CS0 CSRTN0
PWM1 CS1 CSRTN1
PWM2 CS2 CSRTN2
PWM3 CS3 CSRTN3
PWM4 CS4 CSRTN4
PWM5 CS5 CSRTN5
PWM6 CS6 CSRTN6
PWM7 CS7 CSRTN7
VCORE_ISEN1_R
VCORE_ISEN2_R
VCORE_ISEN3_R
VCORE_ISEN4_R
VCORE_ISEN5_R
VCORE_ISEN6_R
VGT_ISEN7_R
VGT_ISEN8_R
RV18 1.5K1%4
RV21 1.5K1%4
RV23 1.5K1%4
RV24 1.5K1%4
RV25 1.5K1%4
RV26 1.5K1%4
RV27 1.5K1%4
RV28 1.5K1%4
CV12 0.22u16X4
CV13 0.22u16X4
CV14 0.22u16X4
CV15 0.22u16X4
CV16 0.22u16X4
CV17 0.22u16X4
CV18 0.22u16X4
CV19 0.22u16X4
VCROE_PWM1 RA2201_CORE_PH1
VCROE_PWM2 RA2201_CORE_PH2
VCROE_PWM3 RA2201_CORE_PH3
VCROE_PWM4 RA2201_CORE_PH4
VCROE_PWM5 RA2202_CORE_PH5
VCROE_PWM6 RA2202_CORE_PH6
VGT_PWM1 RA2202_GT_PHA1
VGT_PWM2 RA2202_GT_PHA2
VCORE
VGT
TEMP0
TEMP1
VCORE_TSEN
VGT_TSEN
CV9 C470p50X0402
R51 22K1%4
CV4 C470p50X0402
R37 22K1%4
JSMB1
SMBCLK_VSB
SMBDATA_VSB
H2X2[4]M_BLACK-RH
ATX_5VSB
RV1 47K/4
RV5 0R/4 SM_ADDR
J1
JVBOOT
QV1 2N7002
H1X2M-2PITCH_BLACK-HF
CV1 0.1u16X4
Jumper insert,VCORE/VGT 0.9V.
MICRO-STAR INT'L CO.,LTD.
PWM Solution
MS-7D17
12
Monday, March 15, 2021
48 of 73


12VIN
VR36
2.2R/8
VC57
2.2u16X6
RA2201_CORE_VCC1
VU4B
RAA220002GNP#HA0_TDFN12-HF
VCC12-1
PWM1
UGATE1
BOOT1
PHASE1
LGATE1
[48] VCROE_PWM1
RA2201_CORE_UG1
RA2201_CORE_BOOT1
RA2201_CORE_PH1
RA2201_CORE_LG1
12VIN
VR35
2.2R/8
VC54
2.2u16X6
RA2201_CORE_VCC2
VU3A
RAA220002GNP#HA0_TDFN12-HF
VCC12-0
PWM0
GND
UGATE0
BOOT0
PHASE0
LGATE0
[48] VCROE_PWM2
RA2201_CORE_UG2
RA2201_CORE_BOOT2
RA2201_CORE_PH2
RA2201_CORE_LG2
12VIN
VR38
2.2R/8
VC58
2.2u16X6
RA2201_CORE_VCC3
VU4A
RAA220002GNP#HA0_TDFN12-HF
VCC12-0
PWM0
GND
UGATE0
BOOT0
PHASE0
LGATE0
[48] VCROE_PWM3
RA2201_CORE_UG3
RA2201_CORE_BOOT3
RA2201_CORE_PH3
RA2201_CORE_LG3
[48] VCORE_TSEN
VRT1 10KRT1%4
12VIN
VC35 10u25X8
VC33 10u25X8
VC34 0.1u25X4
VC36 0.1u25X4
RA2201_CORE_UG1
RA2201_CORE_BOOT1
VR37 2.2R1%6
RA2202_CORE_BOOT1_R
VR14 X_10K/4
VC56 0.1u25X4
RA2201_CORE_PH1
RA2201_CORE_LG1
VQ21
VQ23
VQ22
VQ24
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE12
CH-0.33u45A0.71mS-HF
VCHOKE11
CH-0.33u45A0.71mS-HF
VCORE
VR15 2.2R/8
VC38 1000p50X/4
Close to IC
12VIN
VC28 0.1u25X4
VC30 0.1u25X4
VC27 10u25X8
VC29 10u25X8
[48] RA2201_CORE_PH1
RA2201_CORE_UG2
RA2201_CORE_BOOT2
VR34 2.2R1%6
RA2202_CORE_BOOT2_R
VC55 0.1u25X4
VR12 X_10K/4
RA2201_CORE_PH2
RA2201_CORE_LG2
VQ17
VQ19
VQ18
VQ20
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE9
CH-0.33u45A0.71mS-HF
VCHOKE10
CH-0.33u45A0.71mS-HF
VCORE
VR13 2.2R/8
VC32 1000p50X/4
12VIN
VC42 0.1u25X4
VC40 0.1u25X4
VC41 10u25X8
VC39 10u25X8
[48] RA2201_CORE_PH2
RA2201_CORE_UG3
RA2201_CORE_BOOT3
VR39 2.2R1%6
RA2202_CORE_BOOT3_R
VC59 0.1u25X4
VR16 X_10K/4
RA2201_CORE_PH3
RA2201_CORE_LG3
VQ27
VQ25
VQ28
VQ26
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE13
CH-0.33u45A0.71mS-HF
VCHOKE14
CH-0.33u45A0.71mS-HF
VCORE
VR17 2.2R/8
VC43 1000p50X/4
[48] RA2201_CORE_PH3
12VIN
VC37 0.1u16X4
12VIN
VC31 0.1u16X4
MICRO-STAR INT'L CO.,LTD.
Title
VCORE MOS-PHASE 1~3
Size
Document Number
MS-7D17
Rev
12
Date: Monday, March 15, 2021
Sheet 49 of 73


12VIN
VR23
2.2R/8
VC46
2.2u16X6
RA2201_CORE_VCC4
[48]
VCROE_PWM4
VU2A
VCC12-0
PWM0
GND
UGATE0
BOOT0
PHASE0
LGATE0
RA2201_CORE_UG4
RA2201_CORE_BOOT4
RA2201_CORE_PH4
RA2201_CORE_LG4
RAA220002GNP#HA0_TDFN12-HF
12VIN
VR32
2.2R/8
VC53
2.2u16X6
RA2202_CORE_VCC5
[48]
VCROE_PWM5
VU3B
VCC12-1
PWM1
UGATE1
BOOT1
PHASE1
LGATE1
RA2202_CORE_UG5
RA2202_CORE_BOOT5
RA2202_CORE_PH5
RA2202_CORE_LG5
RAA220002GNP#HA0_TDFN12-HF
12VIN
VR22
2.2R/8
VC45
2.2u16X6
RA2202_CORE_VCC6
[48]
VCROE_PWM6
VU2B
VCC12-1
PWM1
UGATE1
BOOT1
PHASE1
LGATE1
RA2202_CORE_UG6
RA2202_CORE_BOOT6
RA2202_CORE_PH6
RA2202_CORE_LG6
RAA220002GNP#HA0_TDFN12-HF
VCORE
Remove 3PCS CAP
For power solution
VEC15
VEC13
VEC11
VEC6
VEC7
VEC9
VEC14
CD560u6.3SO-HF
12VIN
VC4
VC3
0.1u25X4
0.1u25X4
VC22
10u25X8
VC24
10u25X8
RA2201_CORE_UG4
RA2201_CORE_BOOT4
VR26
2.2R1%6
RA2202_CORE_BOOT4_R
VC48
0.1u25X4
VR31
X_10K/4
RA2201_CORE_PH4
RA2201_CORE_LG4
VQ5
VQ6
VQ11
VQ8
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE5
CH-0.33u45A0.71mS-HF
VCHOKE6
CH-0.33u45A0.71mS-HF
VCORE
VR4
2.2R/8
VC19
1000p50X/4
12VIN
VC25
VC23
0.1u25X4
0.1u25X4
VC12
10u25X8
VC11
10u25X8
[48]
RA2201_CORE_PH4
RA2202_CORE_UG5
RA2202_CORE_BOOT5
VR33
2.2R1%6
RA2202_CORE_BOOT5_R
VC52
0.1u25X4
VR10
X_10K/4
RA2202_CORE_PH5
RA2202_CORE_LG5
VQ15
VQ13
VQ16
VQ14
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE8
CH-0.33u45A0.71mS-HF
VCHOKE7
CH-0.33u45A0.71mS-HF
VCORE
VR11
2.2R/8
VC26
1000p50X/4
12VIN
VC2
VC1
0.1u25X4
0.1u25X4
VC10
10u25X8
VC9
10u25X8
[48]
RA2202_CORE_PH5
RA2202_CORE_UG6
RA2202_CORE_BOOT6
VR25
2.2R1%6
RA2202_CORE_BOOT6_R
VC50
0.1u25X4
VR30
X_10K/4
RA2202_CORE_PH6
RA2202_CORE_LG6
VQ4
VQ3
VQ7
VQ12
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
VCHOKE3
CH-0.33u45A0.71mS-HF
VCHOKE4
CH-0.33u45A0.71mS-HF
VCORE
VR3
2.2R/8
VC20
1000p50X/4
[48]
RA2202_CORE_PH6
MICRO-STAR INT'L CO.,LTD.
Title
VCORE MOS-PHASE 4~6
Size
Document Number
MS-7D17
Rev
12
Date: Monday, March 15, 2021
Sheet 50 of 73



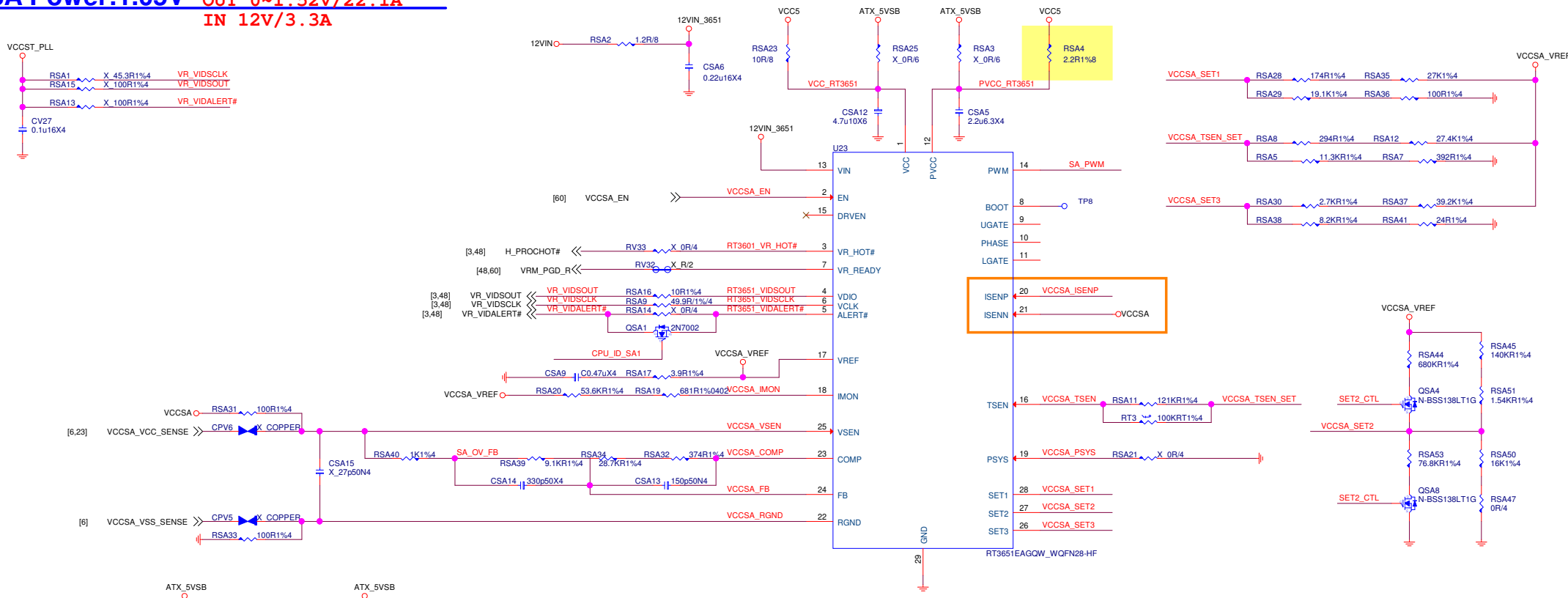
MICRO-STAR INT'L CO.,LTD.

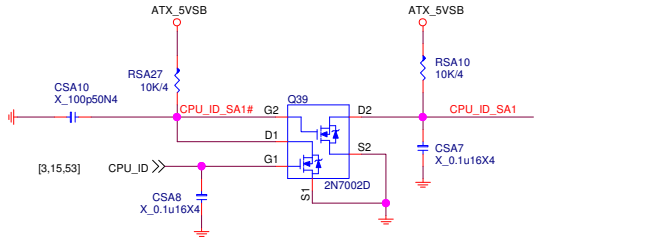
Title: VGT MOS-PHASE 1~2

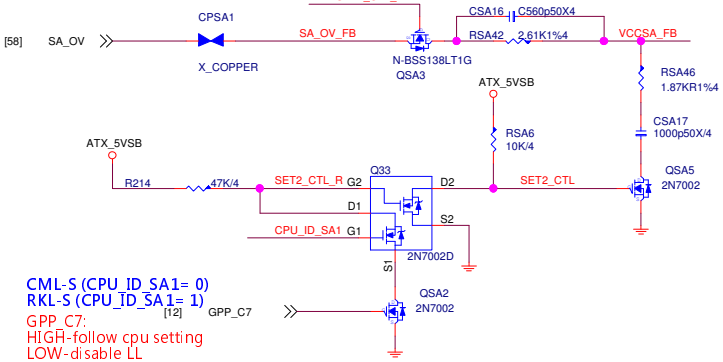
Size | Document Number: MS-7D17 | Rev: 12

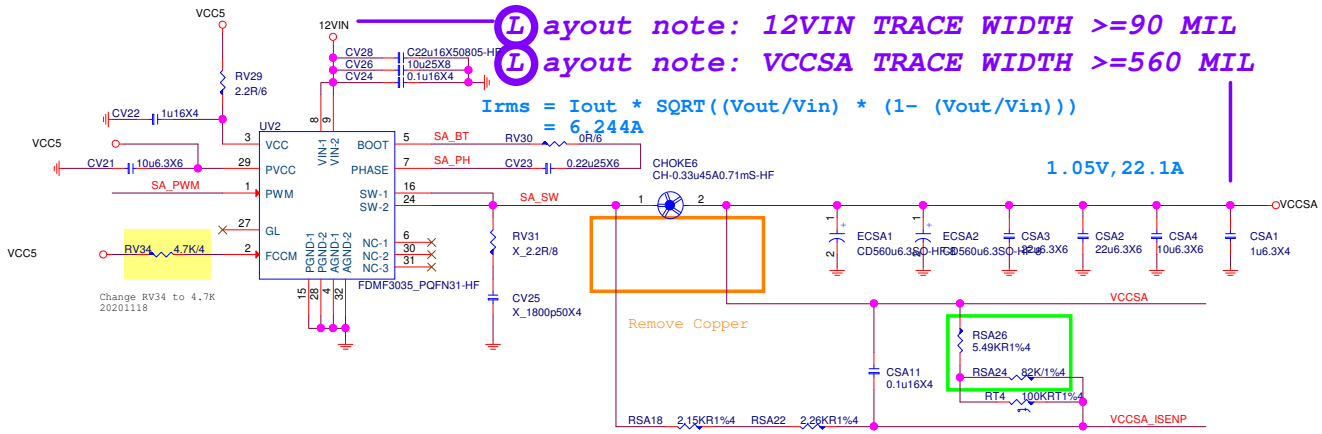
Date: Monday, March 15, 2021 | Sheet 51 of 73

SA Power:1.05V OUT 0~1.52V/22.1A
IN 12V/3.3A









MICRO-STAR INT'L CO.,LTD.

Title	CPU VCCSA	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 52 of 73	

IO Power:VCCIO_0 OUT 0.95~1.1V/7.5A IN 12V/1A

Layout note: +12V WIDTH >=50 MIL

Layout note: +12_VCCIO WIDTH >=40 MIL

Layout note:VCCIO_0 WIDTH >=190 MIL

CHOKE9 CH-0.47u4.8A16.5mS-HF

+12V → C418 0.1u16X4 → +12V_VCCIO

+12V_VCCIO: C390, C399, C386, C380 (C22u16X50805-HF, 10u25X8, 10u25X8, 0.1u16X4)

Tss=Css*Vref/Iss
18n*0.6/5uA=2.16ms

ATX_5VSB: R321 47K/4, C410 X_0.1u16X4

[60] SLP_S3_CTRL → VCCIO_EN, VCCIO_EN_G

Q54 2N7002D: G2, D1, G1, D2, S2, S1

+12V: R298 30K1%4, R270 10K/4

VCCIO_EN → [60]

[54,56] DDR_PWRGD

VCC3: R330 47K/4, C408 1u6.3X4, R329 X_10K/4

C409 0.22u16X4

Q55 2N7002D: G2, D1, G1, D2, S2, S1

VCCIO_EN_Q → [15,53,55]

+12V: R290 47K/4

Q43 2N7002D: G2, D1, G1, D2, S2, S1

VCCIO_EN

[12,21,22,45,55,56,60,61] SLP_S3#

VCC5

R1041 75KR1%0402

U66 AOZ2263AQI-10

TON, VCC, PGOOD, EN, PFM#, SS, IN(7-9), BST, LX-1(10-11), LX-3, LX-4, LX-5, FB, AGND, PGND-1, PGND-2, PGND-3, PGND-4, PGND-5

R1040 1.5R-HE

C992 4.7u10X6

R327 100K1%4

VCCIO_PG

VCCIO_EN

R1054 100K1%4 VCCIO_0_MODE

C991 0.01u50X4

I9C-022630C-A68

AVL:OI9-7D15002-A68

VCCIO_BOOT1 R255 0R/6 C337 0.1u25X4

VCCIO_PH1 R234 X_2.2R/8 C342 X_3300p50X4

reserve snubber

CHOKE15 CH-0.68u15.5A4.85mS-HF

FB:0.8V

VCCIO_FB

C993 1000p50X/4

R205 10R1%4

R206 0R/4 → VCCIO_SENSE [6,23]

R226 1K1%4

R227 5.1K1%4

VCCIO_0: C307 22u6.3X6, C298 22u6.3X6, C295 22u6.3X6, C296 22u6.3X6, C300 22u6.3X6, C289 0.1u16X4

CP6 X_COPPER

from NCT3933

[58] VCCIO_OV

Q151 2N7002D: GPP_E3, VCCIO_12_MODE, GPP_E3, G2, D1, G1, D2, S2, S1

VCCIO_0_MODE

3VSB

R200 X_10K/4

[15] GPP_F23

R219 100K1%4

R201 X_10K/4

[12] GPP_F22

R202 100K1%4

VCCIO_FB

R212 8.2KR1%4

[3,15,52,53] CPU_ID → Q32 2N7002

0.95V (CPU_ID = 0)
1.05V (CPU_ID = 1)

Q150 2N7002D: GPP_F22, G2, D2, R1053 X_5.9K1%4, VCCIO_FB, VCCIO_FB, R1052 X_5.9K1%4, D1, GPP_F23, G1, S2, S1

Layout note: +12_VCCIO WIDTH >=40 MIL

IO Power:VCCIO_12 OUT 1V/9.6A IN 12V/1A

Layout note:VCCIO_12 WIDTH >=250 MIL

+12V_VCCIO: C392, C402, C389, C382 (C22u16X50805-HF, 10u25X8, 10u25X8, 0.1u16X4)

VCC5

R1042 75KR1%0402

U67 AOZ2263AQI-10

TON, VCC, PGOOD, EN, PFM#, SS, IN(7-9), BST, LX-1(10-11), LX-3, LX-4, LX-5, FB, AGND, PGND-1, PGND-2, PGND-3, PGND-4, PGND-5

R1043 1.5R-HE

C994 4.7u10X6

R300 100K1%4

VCCIO_12_PG

VCCIO_12_EN

R1055 100K1%4 VCCIO_12_MODE

C995 0.01u50X4

I9C-022630C-A68

AVL:OI9-7D15002-A68

USM;1~1.6V
PFM;2.2~VIN

VCCIO_BOOT12 R251 0R/6 C338 0.1u25X4

VCCIO_12_PH

VCCIO_12_PH R235 X_2.2R/8 C343 X_3300p50X4

CHOKE16 CH-0.68u15.5A4.85mS-HF

VCCIO_12_FB

C340 1000p50X/4

R240 10R1%4

R244 0R/4 → VCCIO12_SENSE [6,23]

R253 1K1%4

R231 3.9K1%4

VCCIO_12: C288 0.1u16X4, C303 22u6.3X6, C312 22u6.3X6, C309 22u6.3X6

VCCIO_12: C311 22u6.3X6, C308 22u6.3X6, C310 22u6.3X6

CP7 X_COPPER

from NCT3933

[58] VCCIO_12_OV

ATX_5VSB: R295 22K1%4, R304 47K/4

Q47 2N7002D: G2, D1, G1, D2, S2, S1

VCCIO_EN

R282 100K1%4, C381 1u6.3X4

ATX_5VSB: R305 47K/4

Q48 2N7002D: G2, D1, G1, D2, S2, S1

VCCIO_EN

+12V: R277 30K1%4, R271 10K/4, C356 X_0.1u16X4

VCCIO_12_EN

[3,15,52,53] CPU_ID → Q41 2N7002

VCCIO_12_PG → Q49 2N7002

ATX_5VSB: R310 47K/4

Q59 2N7002D: G2, D1, G1, D2, S2, S1

VCCIO_PG_R

CPU_ID

VCCIO_PG → [60]

MICRO-STAR INT'L CO.,LTD		
MS-7D17		
Size: Custom	Document Description: CPU PWR-VCCIO-RT8125E	Rev: 12
Date: Monday, March 15, 2021	Sheet 53 of 73	

DDR4 Power:1.2V, 14.4A

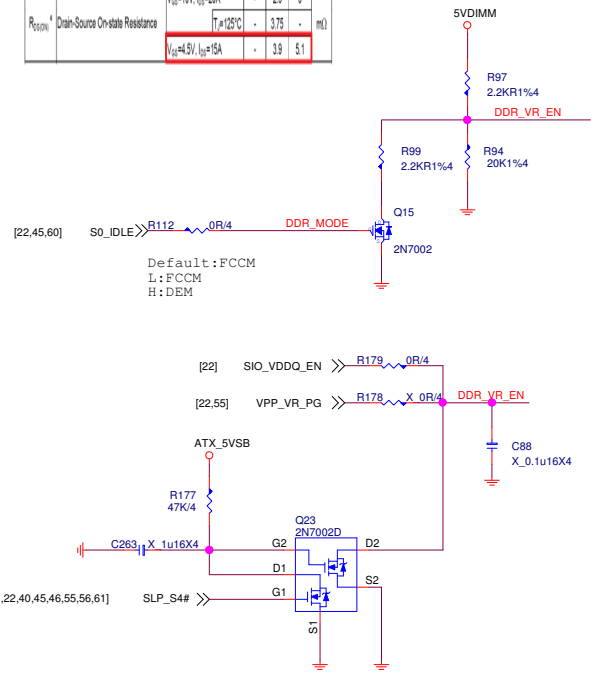
OUT 1.2V/14.4A
IN 5V/4.1A

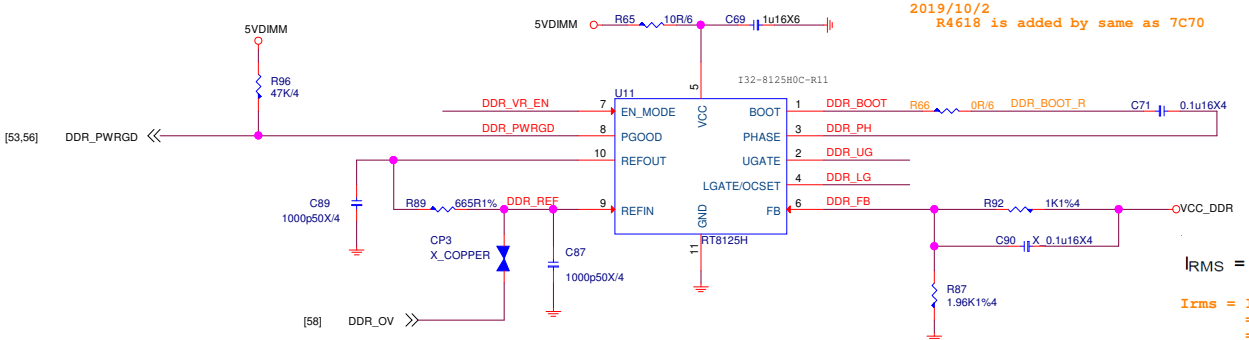
4.3A For CPU
9.1A For 4DIMM
0.7A For DDR VTT
0.251A For VCCPLL_OC

Iout = 4.3+9.1+0.7+0.215=14.351A

Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/5.1m
=14.3529A
Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/3.9m
=18.769A

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Static Characteristics							
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=20A		-	2.5	3	mΩ
			T_J=125°C	-	3.75	-	
		V_{GS}=4.5V, I_{DS}=15A		-	3.9	5.1	





2019/10/2
R4618 is added by same as 7C70

$$V_{OUT} = \left[V_{REFOUT} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)\right] + \frac{\Delta V_{OUT}}{2}$$

Vout=Vrefout*(1+R1/R2)
=0.794x(1+1/1.96)
=1.1991v

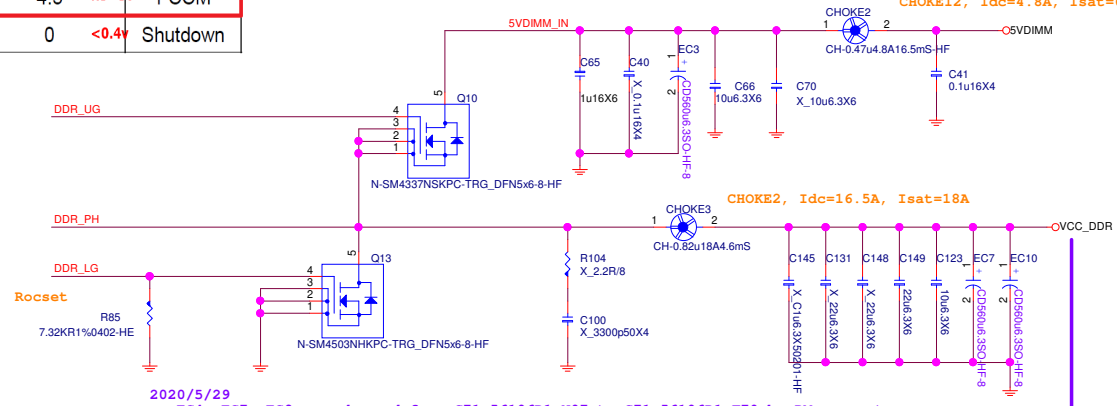
$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.67 * SQRT(0.1824)
= 5.882A

Table 1. States of EN_MODE Control Circuit

Q1	Q2	V_{EN_MODE} (V)	Mode
ON	OFF	2.37 2.1~2.7v	DEM
OFF	OFF	4.5 4.3~5v	FCCM
OFF	ON	0 <0.4v	Shutdown

Layout note: 5VDIMM/5VDIMM_IN WIDTH >=110 MIL



2020/5/29
EC4, EC7, EC9 are chnaged from C71-56106R1-N07 to C71-56106P1-F70 by PM request

Layout note: VCC_DDR WIDTH >=360 MIL

ΔIL=(Vin-Vout)/(L*Fsw) * Vout/Vin
=(5-1.2)/(0.82u*300K)*(1.2/5)
=3.7073A

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Rocset = [(1.3* Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= [(1.3*13.67) -(0.5*3.7073)]* 3.9m / 10u
= 6.2077Kohm

Rocset = [(1.3*Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= ((1.3*13.67) - (0.5*3.7073)]* 5.1m / 10u
= 8.1178Kohm

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.2*13.67) * (1.2/5)
= 1.1119uH

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.4*13.67) * (1.2/5)
= 0.55596uH

So L range = 0.55596uH ~ 1.1119uH

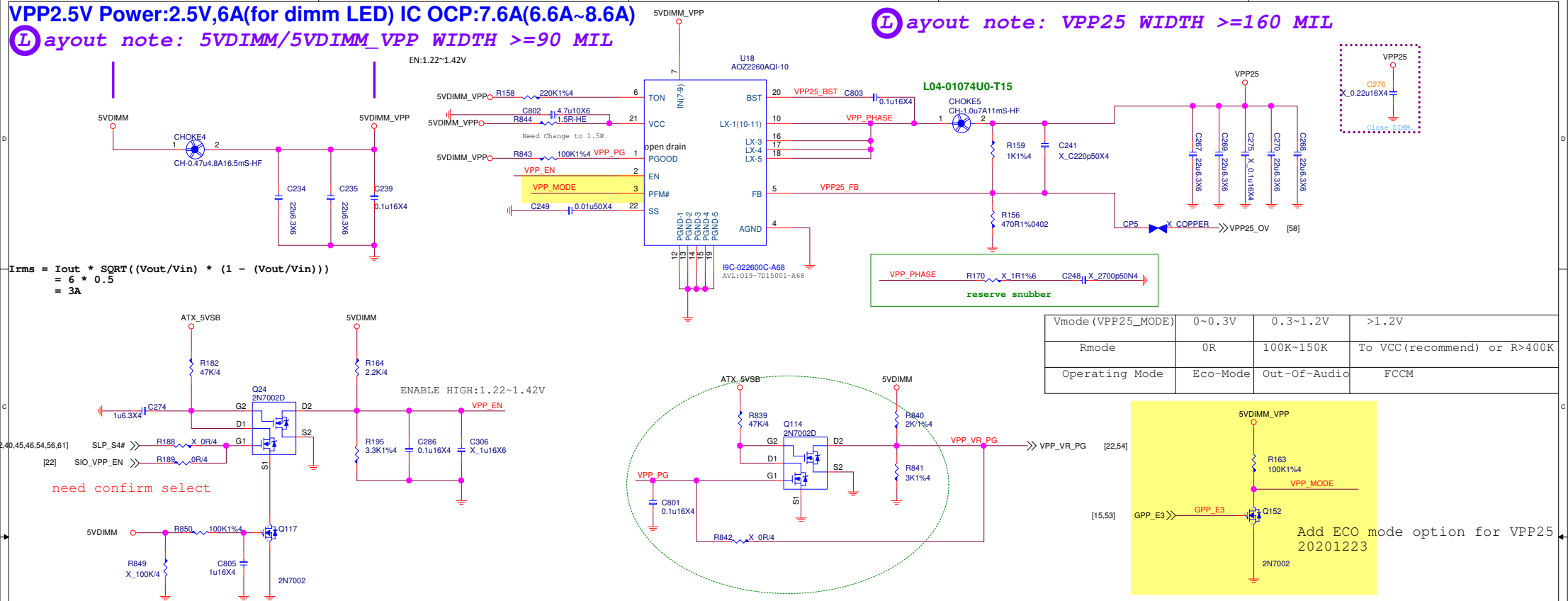
MICRO-STAR INT'L CO.,LTD.

Title	DDR4 Power	
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 54 of 73	

VPP2.5V Power:2.5V,6A(for dimm LED) IC OCP:7.6A(6.6A~8.6A)

Layout note: 5VDIMM/5VDIMM_VPP WIDTH >=90 MIL

Layout note: VPP25 WIDTH >=160 MIL



Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6 * 0.5
= 3A

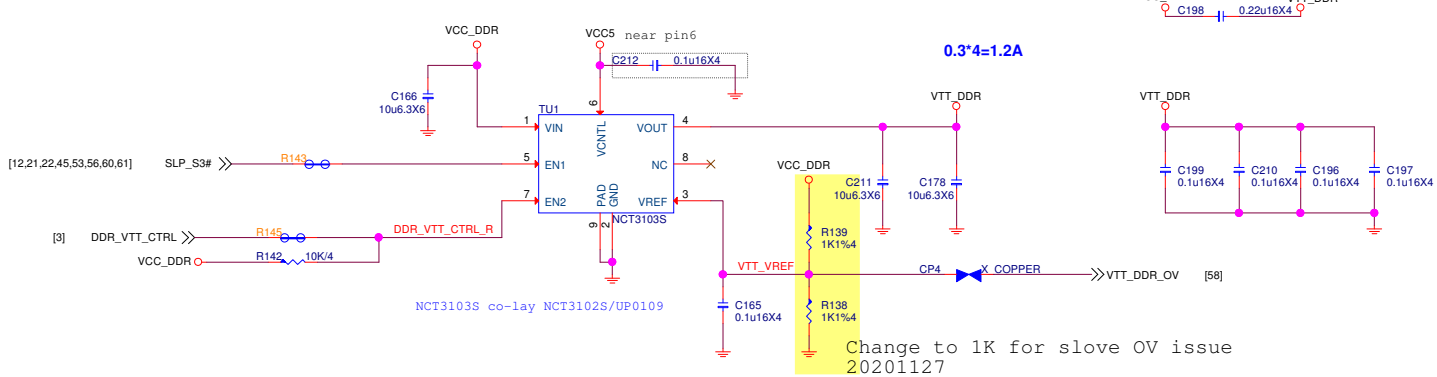
Vmode(VPP25_MODE)	0~0.3V	0.3~1.2V	>1.2V
Rmode	0R	100K~150K	To VCC(recommend) or R>400K
Operating Mode	Eco-Mode	Out-Of-Audio	FCCM

Layout note: VCC_DDR WIDTH >=40 MIL

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

Layout note: VTT_DDR WIDTH >=40 MIL



MICRO-STAR INT'L CO.,LTD.

Title: DDR PWR VPP25/VTT

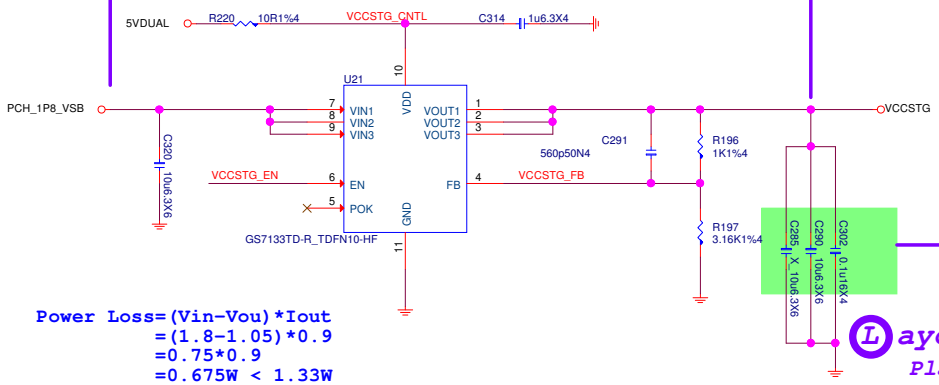
Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 55 of 73

VCCSTG

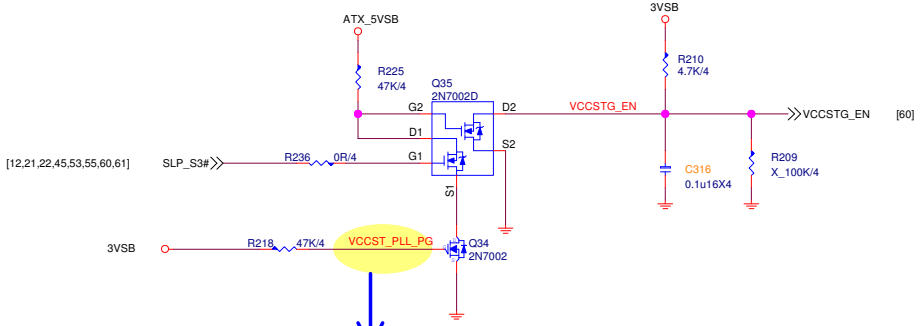
OUT 1.05V/0.9A
IN 1.8V/0.62A

Layout note: 1P8_VSB TRACE WIDTH >=20 MIL
Layout note: VCCSTG TRACE WIDTH >=35 MIL



Layout note: Place near CPU

Power Loss=(Vin-Vou)*Iout
=(1.8-1.05)*0.9
=0.75*0.9
=0.675W < 1.33W

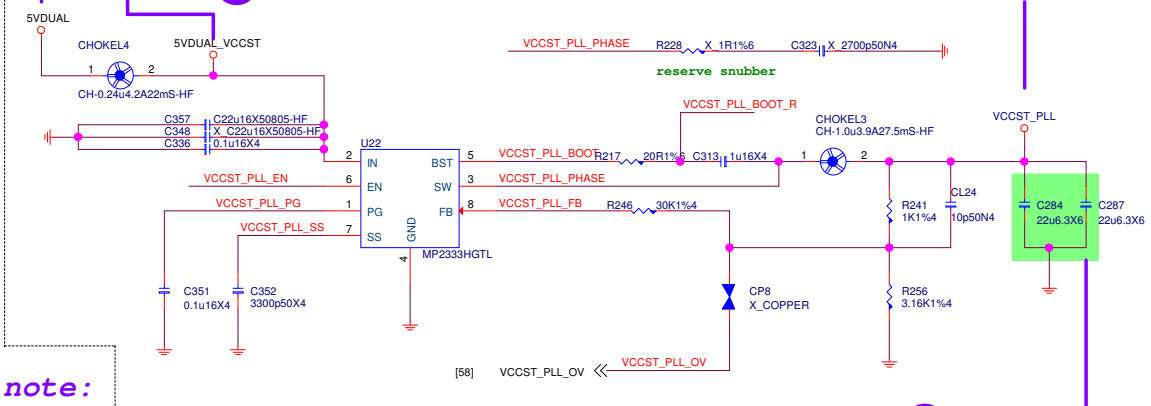


VCCST must always ramp with or earlier then VCCSTG. VCCST >= VCCSTG at all times during ramp.

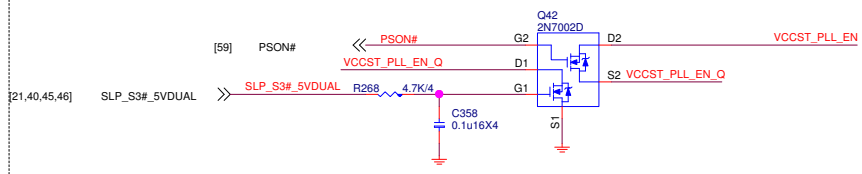
VCCST_PLL

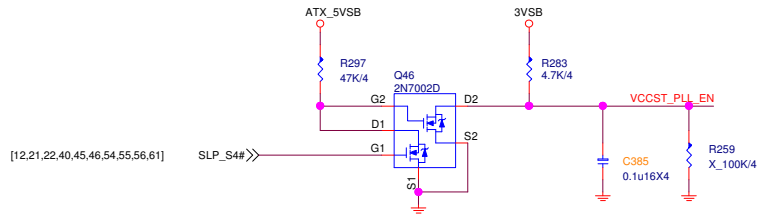
OUT 1.05V/2.3A
IN 5V/0.6A

Layout note: 5VDUAL/5VDUAL_VCCST TRACE WIDTH >=25 MIL
Layout note: VCCST_PLL TRACE WIDTH >=60 MIL



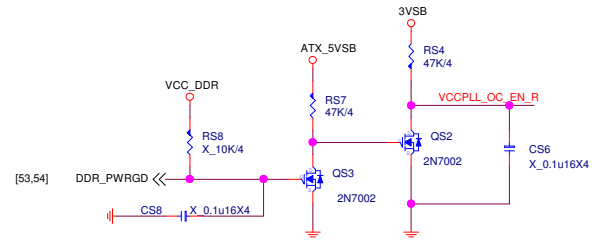
Layout note: Place near CPU



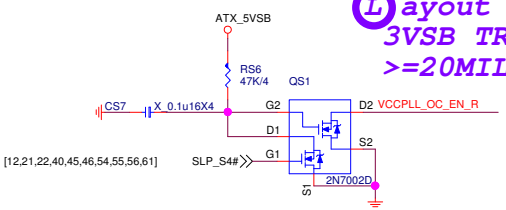


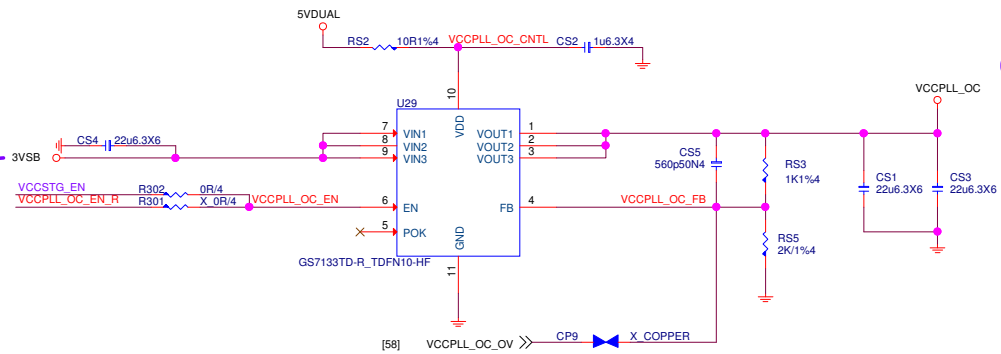
VCCPLL_OC

OUT 1.2V/0.25A
IN 3.3V/0.2A



Layout note: 3VSB TRACE WIDTH >=20MIL





Layout note: VCCPLL_OC TRACE WIDTH >=20MIL

MICRO-STAR INT'L CO.,LTD.

Title: CPU PWR-VCCST/PLL

Size: | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 56 of 73

PCH_VCCIN_AUX Power

OUT 1.8V/9.646A
IN 5V/4.1A

Layout note: 5VDUAL/5VDUAL_PCH_IN TRACE WIDTH >=110 MIL

5VDUAL_PCH_IN
RT_VCC
RT_PVCC
VR18 2.2R1%6
VR19 2.2R1%6

3VSB
R368 100K/4 PCH_VID0
R367 100K/4 PCH_VID1
VID[1:0]=11 --> 1.8V
VID[1:0]=10 --> 1.65V
VID[1:0]=01 --> 1.1V
VID[1:0]=00 --> 0V

C441 1u16X6
C440 1u16X6

5VDUAL R378 2.2R/6 VSYS
C444 0.1u16X4
PCH_VCCIN_EN
[61] PCH_VCCIN_PG
[12] PCH_VID0
[12] PCH_VID1
FSWSEL
R396 97.6KR1%4
OCP=18.6A

U37 RT6543AGQW_WQFN20-HF
VSYS VCC PVCC
EN PGOOD AUX_VID0 AUX_VID1 FSWSEL CS_DIS ISENSEP ISENSEN GND PGND
UGATE BOOT PH LGATE VOUT FB COMP RGND
PCH_VCCIN_UG
PCH_VCCIN_BST
PCH_VCCIN_PH
PCH_VCCIN_LG
RT6543_FB
RT6543_COMP

R397 0R/6 PCH_VCCIN_UG_R
R409 2.2R1%6 PCH_VCCIN_BST_R
C458 0.1u16X4
C463 2200p50X4
R423 10K1%4
C472 X_470p50V4
R429 X_3.4KR1%4
C462 27p50N4
R410 6.2KR1%4

5VDUAL_PCH_IN
R421 X_47K/4 FSWSEL R414 X_47K/4
FSWSEL
5V :800kHz
0V :400kHz
NC:600kHz

Remove 1PCS CAP
For power solution

5VDUAL_PCH_IN
C433 0.1u16X4
C435 10u6.3X6
C434 10u6.3X6
EC18 CD560u6.3SO-HF-8
CHOKE10 CH-0.47u4.8A16.5mS-HF
CHOKE11, Idc=4.8A, Isat=6.7A
5VDUAL
C406 X_0.1u16X4

Q68 N-SM4337NSKPC-TRG_DFN5x6-8-HF
Q67 N-SM4503NHKPC-TRG_DFN5x6-8-HF

Layout note: PCH_VCCIN_AUX TRACE WIDTH >=250 MIL
PCH_VCCIN_AUX
CHOKE11 CH-0.15u21A2.4mS-HF
R364 2.2R/8
C432 1000p50X/4
C388 C490 C498 C485 C489 C495 C873 C875 22u6.3X6

PCH_VCCIN_AUX
VR40 100R1%4
VR41 100R1%4
C470 0.1u16X4
PCH_VCCSENSE_R
PCH_VSSSENSE_R
R877 X_R/2 PCH_VCCSENSE [16]
R876 X_R/2 PCH_VSSSENSE [16]

PCH_VCCIN_EN
Q121 2N7002
[43,44,46,57] VSB_ENABLE#
ATX_5VSB
R875 47K/4
PCH_1P8_PG#
Q120 2N7002
3VSB
R365 47K/4
PCH_VCCIN_EN
R370 X_20K1%4
C439 0.1u16X4
C853 X_0.1u16X4

PCH_1P8_VSB R730 1K1%4 PCH_1P8_PG
Q125 2N3904
C644 3300p50X4

Follow Ivy's AVL table recomend
change to D02-3904L09-LA9
from D02-0390429-D07

PCH_1P8_VSB Power

OUT 1.8V/2.2A
IN 5V/1A

Layout note:5VDUAL/5VDUAL_1P8_VSB TRACE WIDTH >=25MIL
Layout note:PCH_1P8_VSB TRACE WIDTH >=60 MIL

5VDUAL
CHOKE13 CH-0.47u4.8A16.5mS-HF
5VDUAL_1P8_VSB

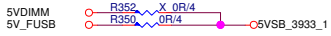
3VSB
R961 47K/4
PCH_1P8_EN
[22,43,44,46,57] VSB_ENABLE#
Q126 2N7002
C909 0.1u16X4

C637 C22u16X50805-HF
C638 X_C22u16X50805-HF
C640 0.1u16X4

U50 MP2333HGTL
IN BST SW FB EN PG SS GND
PCH_1P8_EN
PCH_1P8_PG
PCH_1P8_SS
C643 X_0.1u16X4
C652 3300p50X4

PCH_1P8_PHASE
R726 X_1R1%6
C639 X_2700p50N4
reserve snubber
PCH_1P8_R
PCH_1P8_BOOT
R746 20R1%6
C646 1u16X4
PCH_1P8_PHASE
PCH_1P8_FB
R742 20K1%4
PCH_1P8_FB_R
R748 40.2K1%4
R749 32.4K1%4
CHOKE14 1.0u5.5A-35_1210-HF
C650 10p50N4
PCH_1P8_VSB
C641 22u6.3X6
C642 22u6.3X6

MSI MICRO-STAR INT'L CO.,LTD.
Title: PCH POWER
Size: Document Number: MS-7D17 Rev: 12
Date: Monday, March 15, 2021 Sheet 57 of 73

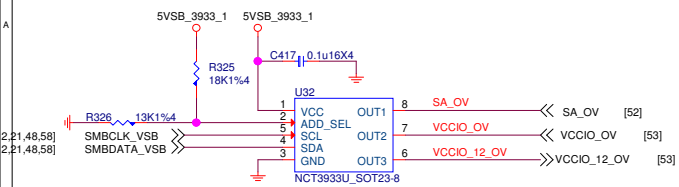


UPI VOLTAGE CONSOLE

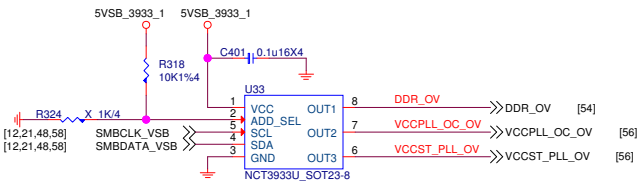
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

UPI VOLTAGE CONSOLE

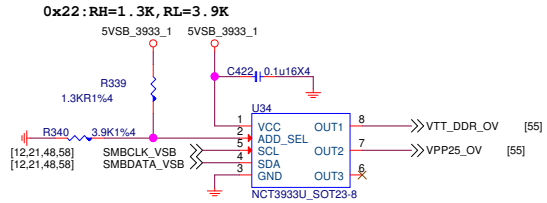
0x26:RH=18K,RL=13K



0x20:RH=18K,RL=OPEN



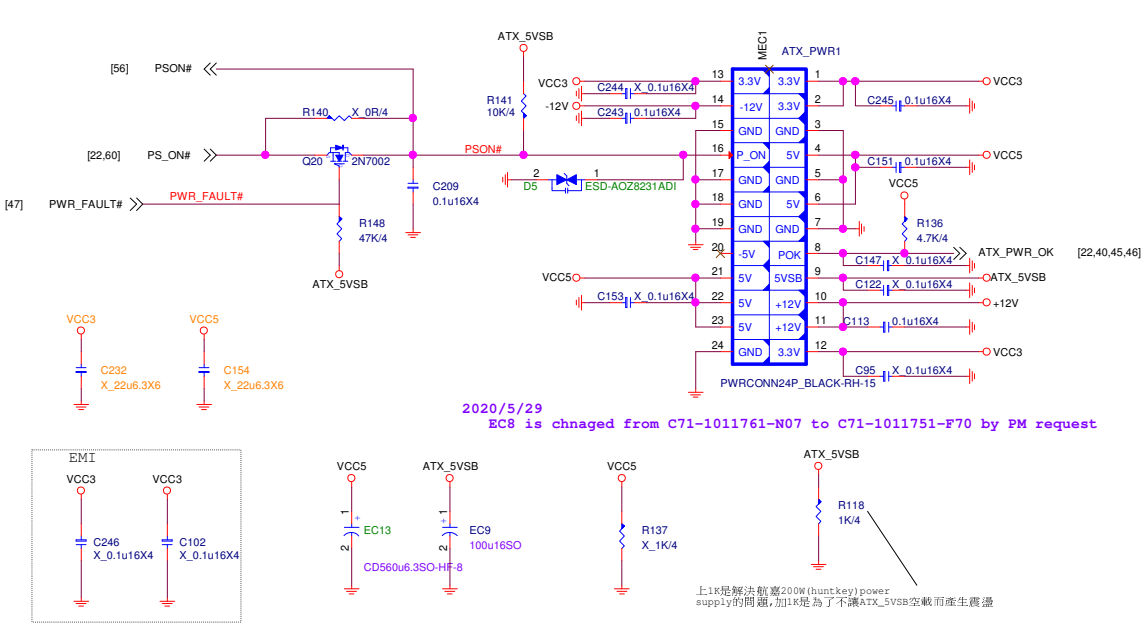
0x22:RH=1.3K,RL=3.9K



MICRO-STAR INT'L CO.,LTD.

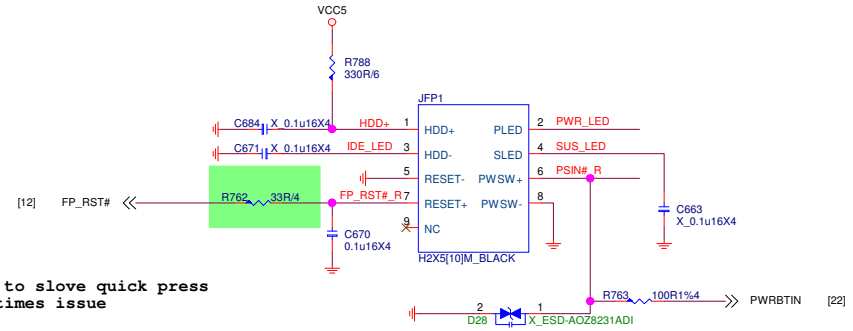
Title	PCH 1P8V -GS7133/OV	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 58 of 73	

ATX POWER CONNECTOR

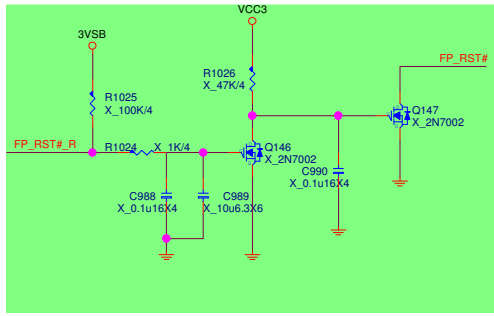


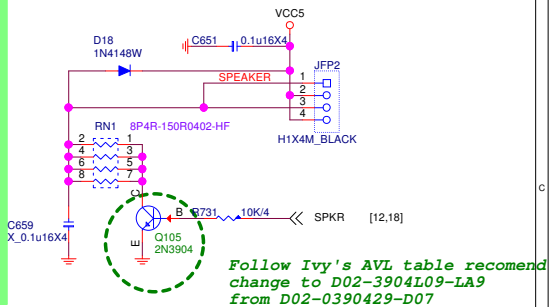
2020/5/29
EC8 is chnaged from C71-1011761-N07 to C71-1011751-F70 by PM request

FRONT PANNEL



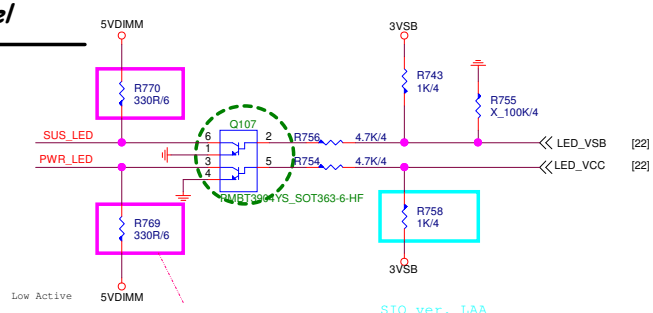
Add the circuit to slove quick press Reset button 2 times issue





Follow Ivy's AVL table recomend change to D02-3904L09-LA9 from D02-0390429-D07

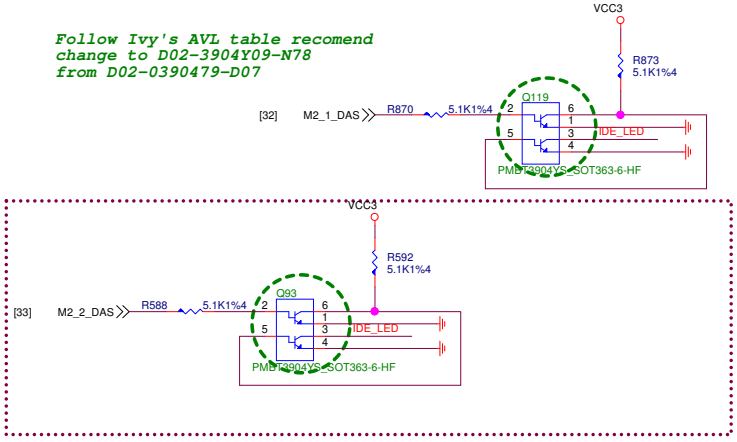
Front Panel LED

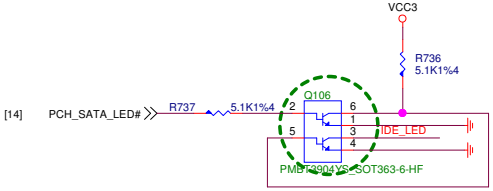


Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

SIO ver. LAA
Push pull pin, no need to stuff resisters.

Follow Ivy's AVL table recomend change to D02-3904Y09-N78 from D02-0390479-D07

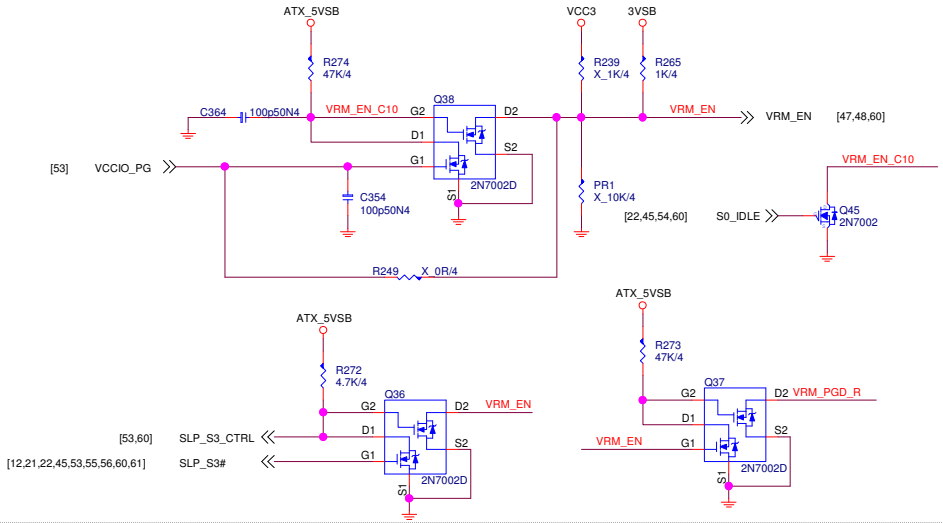




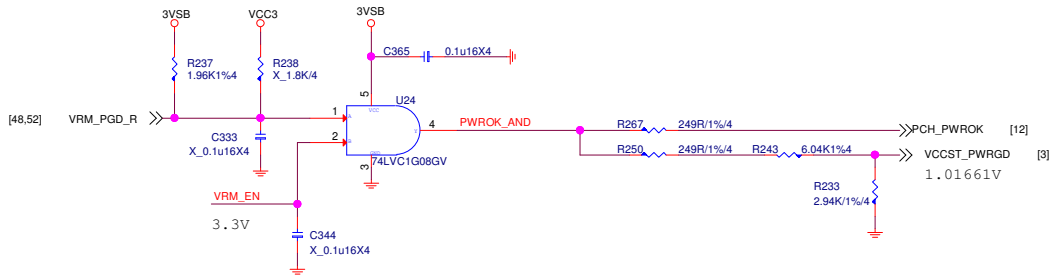
MICRO-STAR INT'L CO.,LTD.

Title	ATX Connector/F_Panel	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 59 of 73	

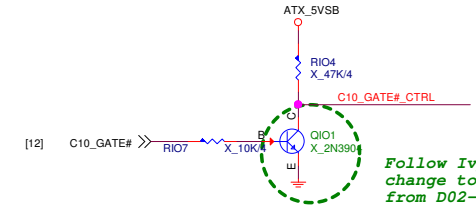
PWR-VRM-Seqence



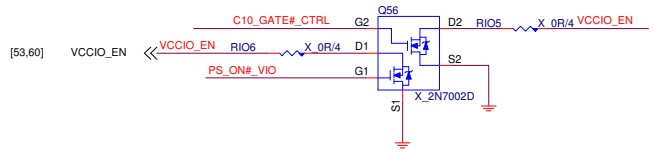
PCH_PWROK/VCCST_PWRGD

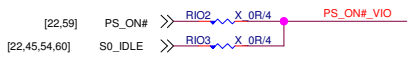


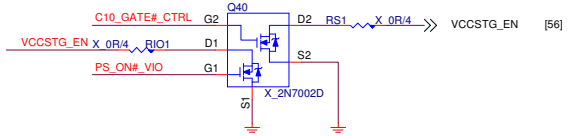
S0IX: VCCIO/VCCSTG/VCCSA OFF

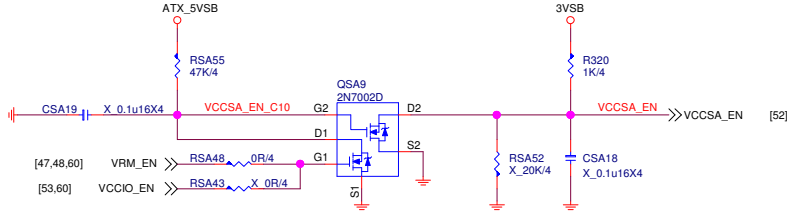


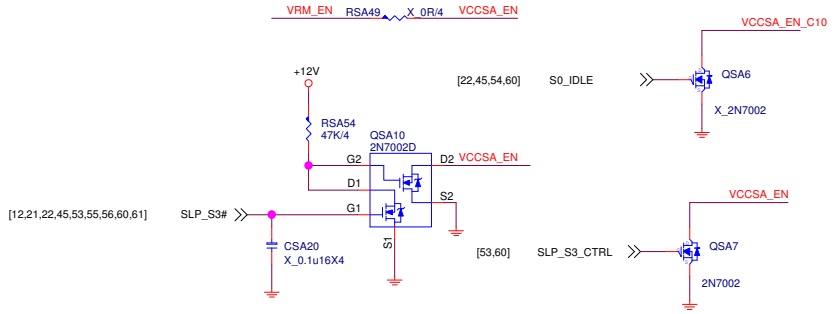
Follow Ivy's AVL table recomend change to D02-3904L09-LA9 from D02-0390429-D07



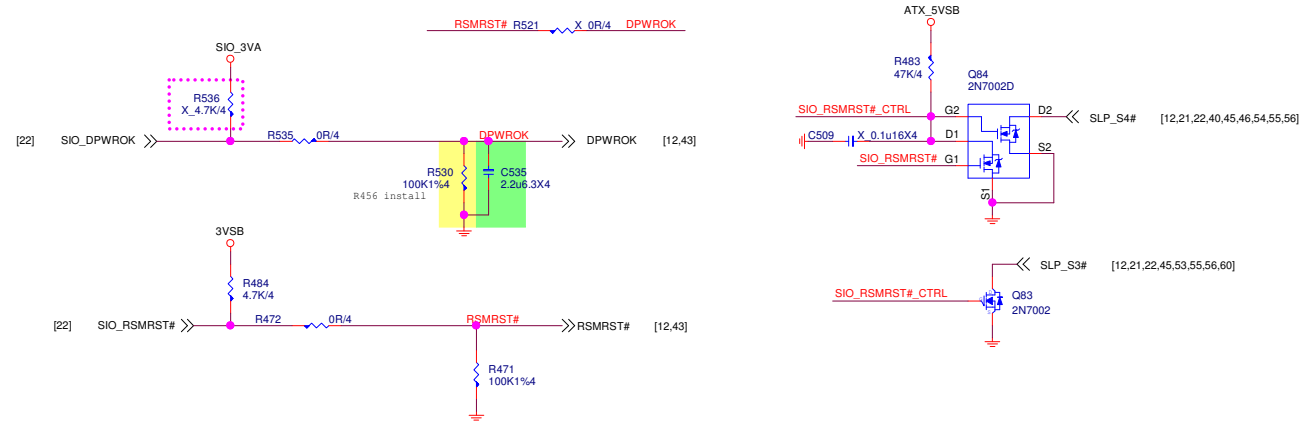








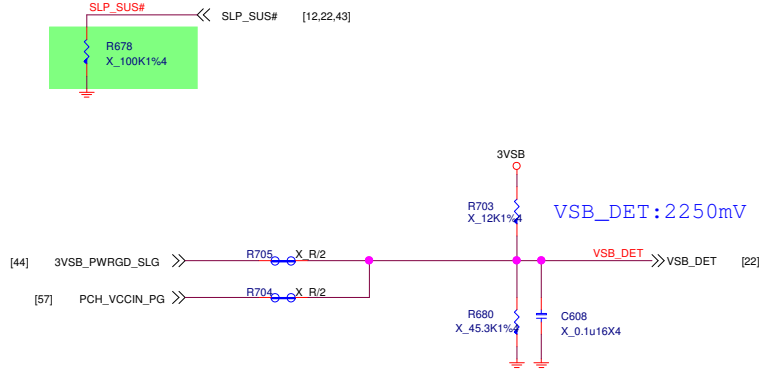
MSI MICRO-STAR INT'L CO.,LTD.		
Title: POWER SEQUENCE		
Size	Document Number: MS-7D17	Rev: 12
Date: Monday, March 15, 2021	Sheet 60 of 73	



FOR RSMRST#/DPWROK/SLP_SUS# INTEL seqence request

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

Delete SLG4F42051
20201116



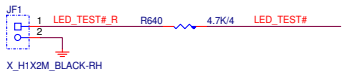
MICRO-STAR INT'L CO.,LTD.

Title	X	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 61 of 73	

IF no JPWRLED1 & JPIPE_LED spec

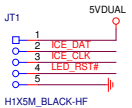
MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test

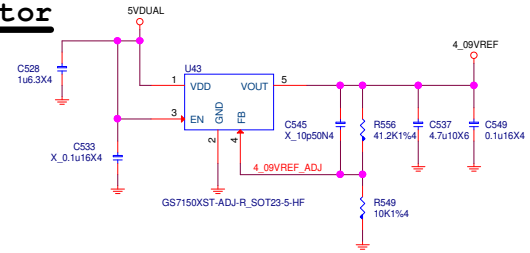


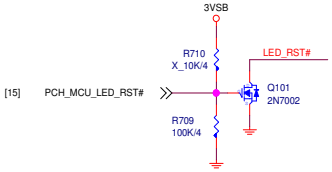
Check with LED model spec

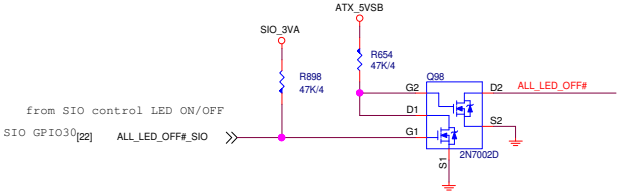
JT1 for FW update



Voltage Monitor

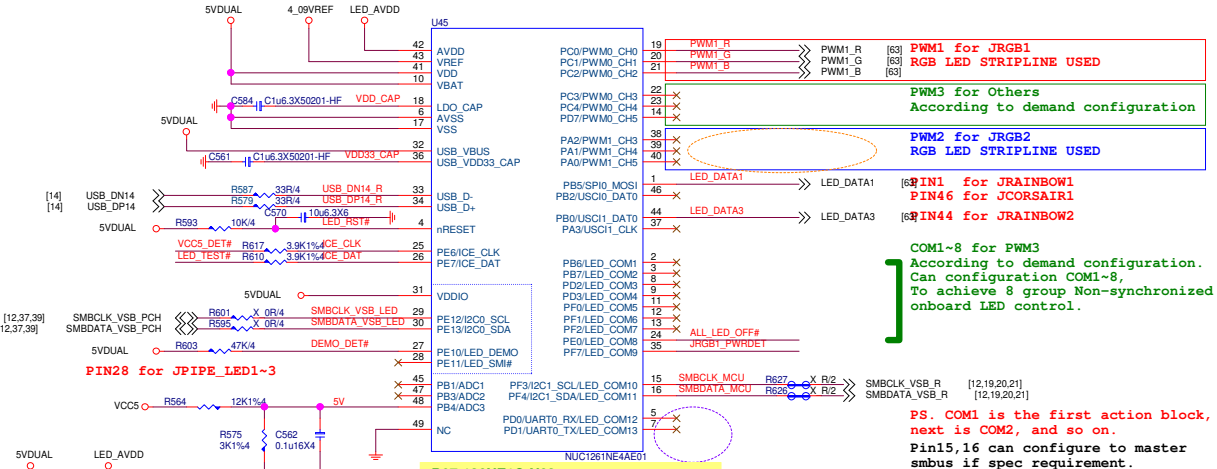


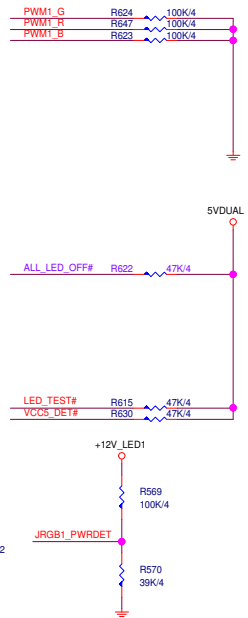




48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.





Control	Net Name	PWM USE
PCH	LED_DATA4	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_DATA1	No Use
JRAINBOW2	LED_DATA3	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~12	PWM2

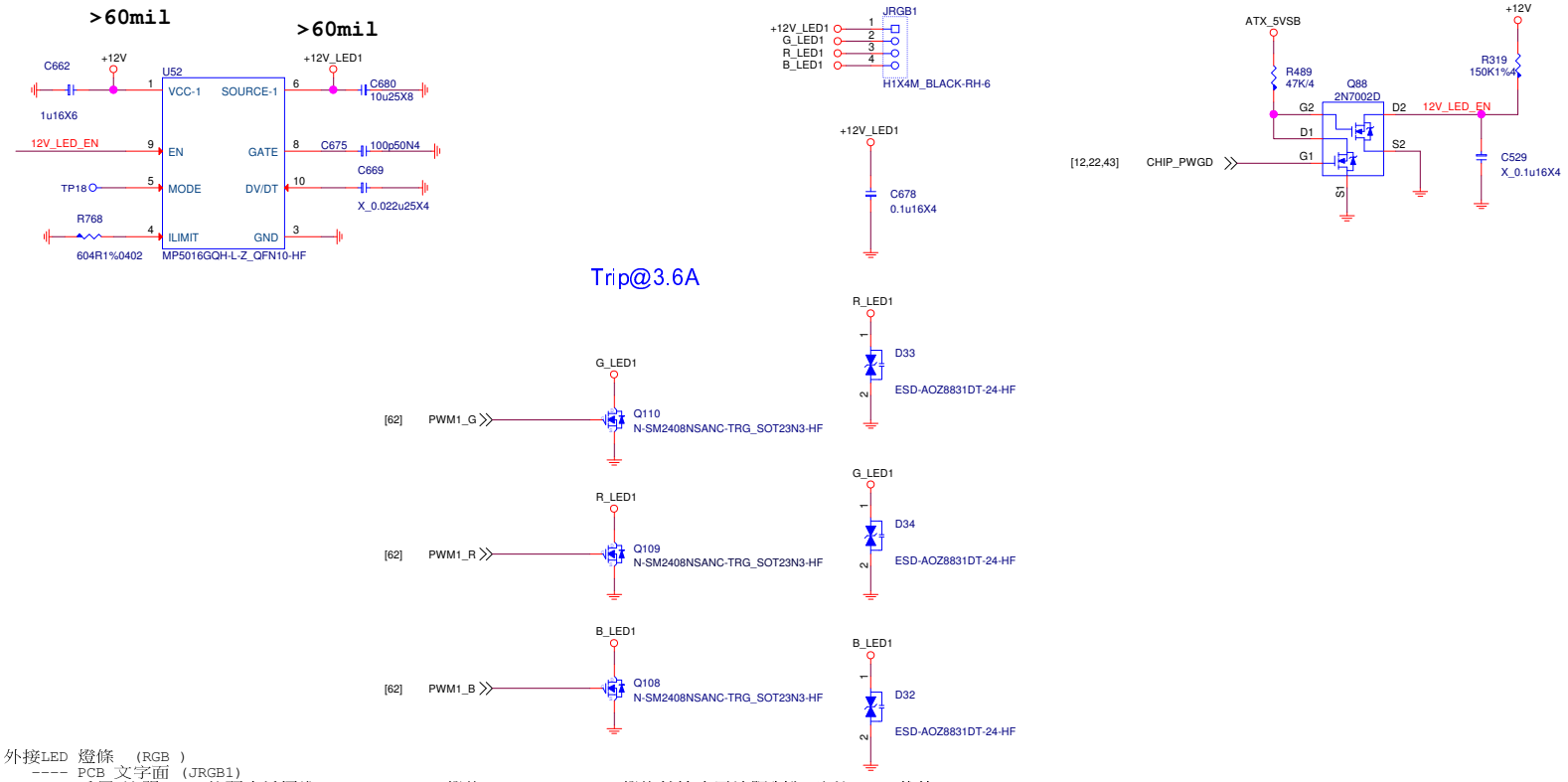
MICRO-STAR INT'L CO.,LTD.

Title: LED MCU Control

Size | Document Number: MS-7D17 | Rev: 12

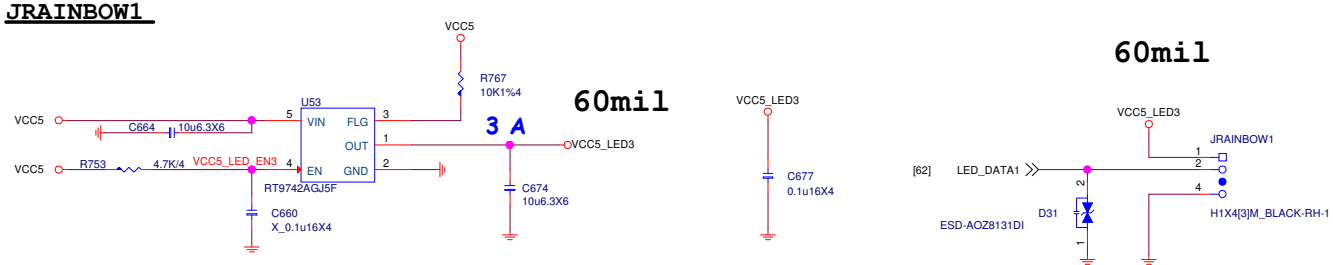
Date: Monday, March 15, 2021 | Sheet 62 of 73

JRGB1

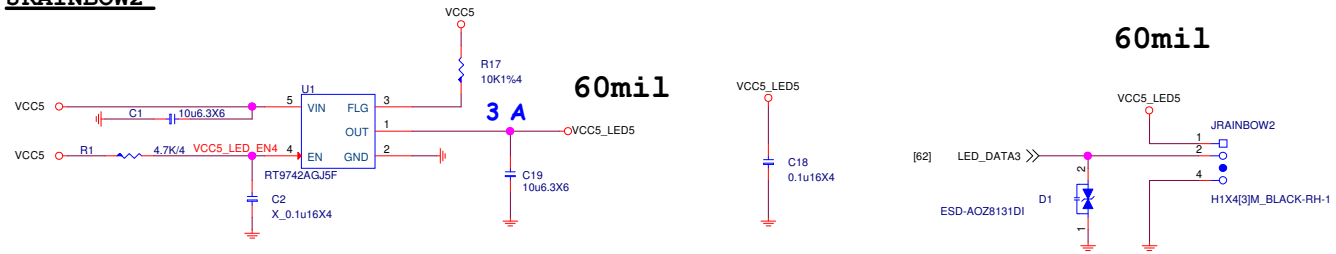


外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRAINBOW1



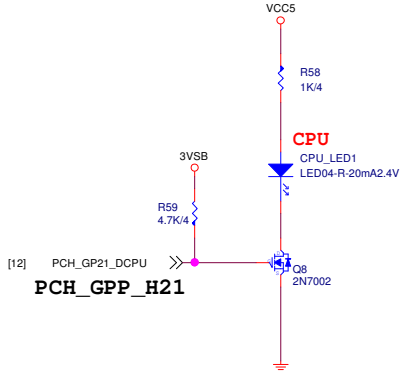
JRAINBOW2

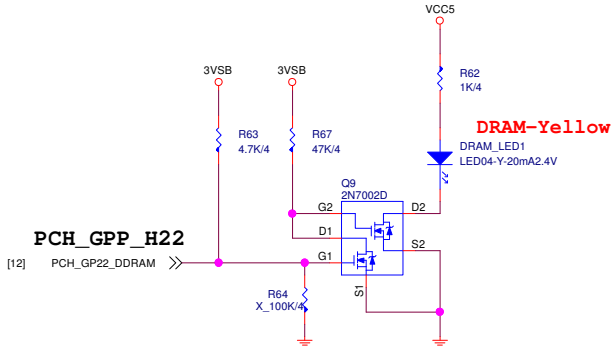


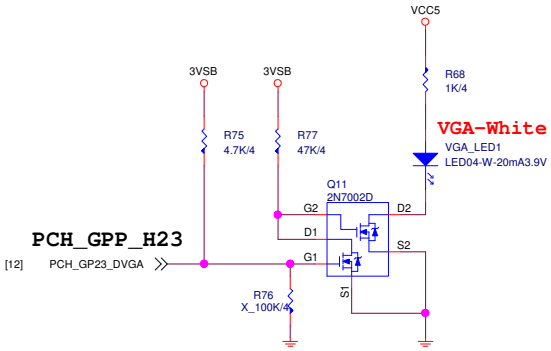
MICRO-STAR INT'L CO.,LTD.

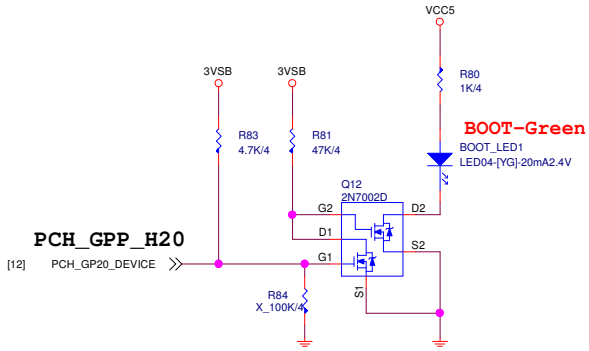
Title	LED PIN HEADER	
Size	Document Number MS-7D17	Rev 12
Date: Monday, March 15, 2021	Sheet 63 of 73	

EZ DEBUG LED









GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED滅掉。
5. 因此最後正常順利開機後，四個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

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Title: EZ DEBUG LED

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 64 of 73

BAT1_X1

BAT-BCR2032P-RH

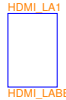
CPU_H1

AZIF0020-P001CC

BIOS_LA1

AMI

HDMI_LA1



HDMI_LABEL

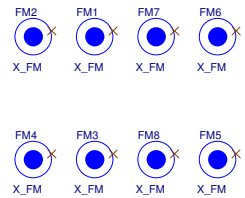
CFOS_LA1

Y02-MU00170-CFO

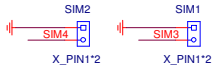
PCB1

7D17_12

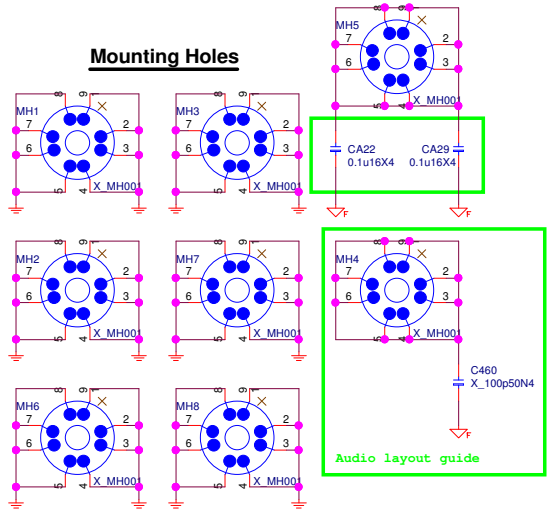
Optical Fiducial Marks-120



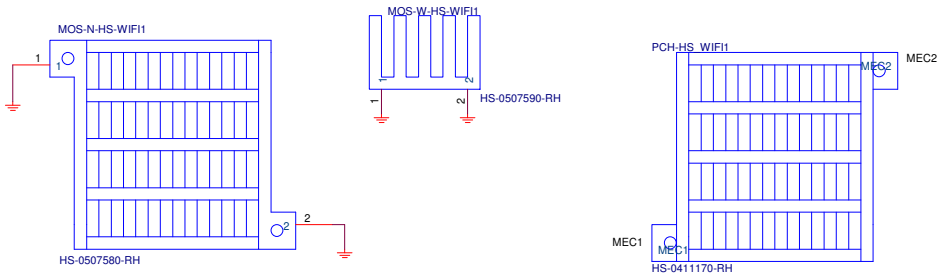
Simulation



Mounting Holes



1.0 option - WiFi



M2-COVER-W1

0P10B08433

IO-WIFI1

CSCZ-SHIELD328

MK_LA_WIFI1

G51-M1SPR46-Q13

1.0 option - None WiFi

MOS-N-HS1

X_HS-0507560-RH

MOS-W-HS1

X_HS-0507570-RH

PCH-HS1

X_HS-0411140-RH

M2_1-COVER1

X_0P10B08429

IO-1

X_CSCZ-SHIELD329

MK_LA1

X_G51-M1SPR48-Q13

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Title: Manual Parts

Size | Document Number: MS-7D17 | Rev: 12

Date: Monday, March 15, 2021 | Sheet 65 of 73

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MS-7D17

Size	Document Description	Rev
Custom	Clock Gen-6V41821	12

Date: Monday, March 15, 2021 Sheet 66 of 73