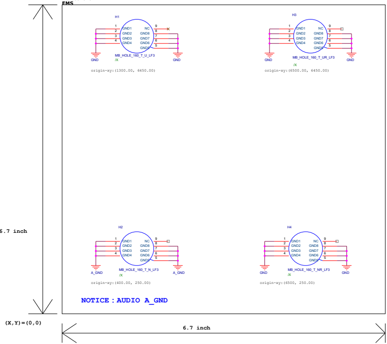
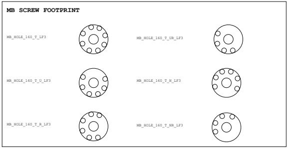
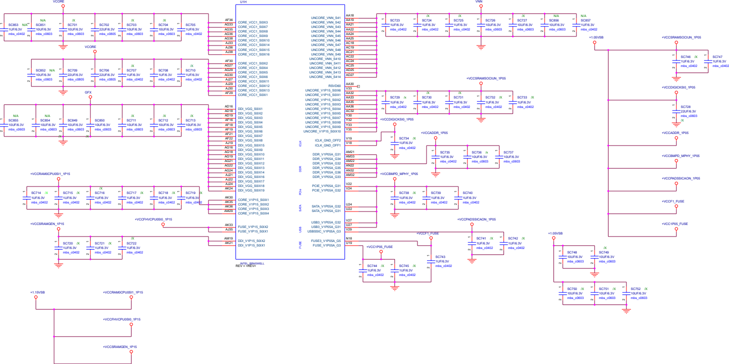
Mini-ITX Screw Hole



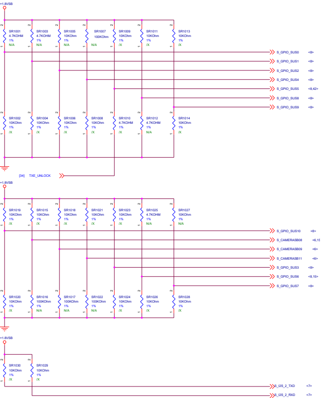


<Variant Name>

ASUSTEK COMPUTER INC	Title : Mini-ITX Screw Hole	
	Engineer: Frank_Guo	
Size: A3	Project Name: Mini-ITX Screw Hole&FIDUCIAL MASK Demo	Rev: 0.02B
Date: Friday, March 27, 2015	Sheet 1 of 75	



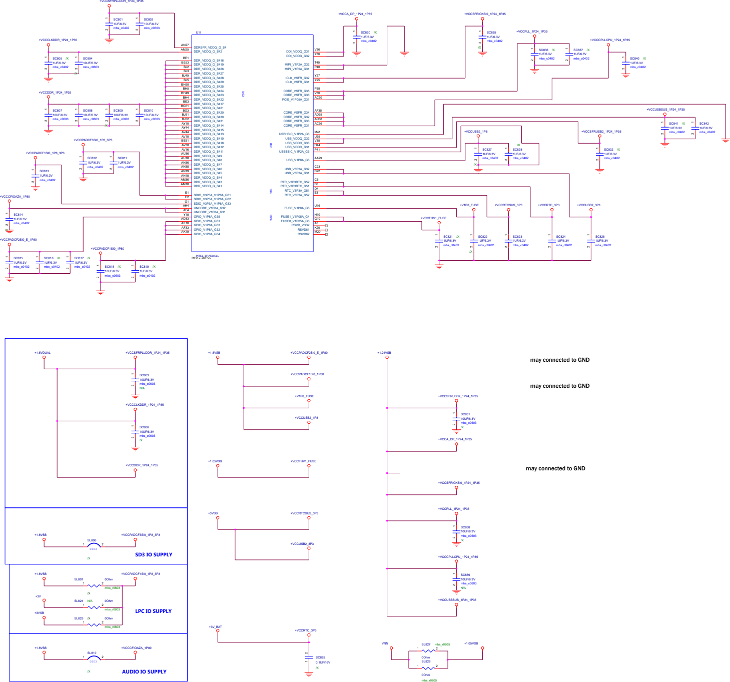
U1H
VCORE
SC853 N/A 1UF/6.3V mbs_c0402
SC851 N/A 10UF/6.3V mbs_c0603
SC701 /X 10UF/6.3V mbs_c0603
SC702 22UF/6.3V mbs_c0805
SC703 /X 10UF/6.3V mbs_c0603
SC704 /X 10UF/6.3V mbs_c0603
SC705 1UF/6.3V mbs_c0402
SC852 N/A 10UF/6.3V mbs_c0603
SC709 22UF/6.3V mbs_c0805
SC706 22UF/6.3V mbs_c0805
SC707 /X 1UF/6.3V mbs_c0402
SC708 1UF/6.3V mbs_c0402
SC710 /X 1UF/6.3V mbs_c0402
GFX
SC855 N/A 10UF/6.3V mbs_c0603
SC854 N/A 10UF/6.3V mbs_c0603
SC849 10UF/6.3V mbs_c0603
SC850 10UF/6.3V mbs_c0603
SC711 10UF/6.3V mbs_c0603
SC712 10UF/6.3V mbs_c0603
SC713 10UF/6.3V mbs_c0603
+VCCRAM0CPU0SI1_1P15
SC714 /X 1UF/6.3V mbs_c0402
SC715 /X 1UF/6.3V mbs_c0402
SC716 /X 1UF/6.3V mbs_c0402
SC717 /X 1UF/6.3V mbs_c0402
SC718 /X 1UF/6.3V mbs_c0402
SC719 /X 1UF/6.3V mbs_c0402
+VCCSRAMGEN_1P15
SC720 /X 1UF/6.3V mbs_c0402
SC721 /X 1UF/6.3V mbs_c0402
SC722 1UF/6.3V mbs_c0402
+VCCFHVCPU0SI0_1P15
AF36 AG33 AG35 AG36 AG38 AJ33 AJ36 AJ35 AJ38
CORE_VCC1_S0IX3 CORE_VCC1_S0IX7 CORE_VCC1_S0IX8 CORE_VCC1_S0IX9 CORE_VCC1_S0IX10 CORE_VCC1_S0IX14 CORE_VCC1_S0IX15 CORE_VCC1_S0IX16
AF30 AG27 AG29 AG30 AJ27 AJ29 AJ30 AF29
CORE_VCC1_S0IX2 CORE_VCC1_S0IX4 CORE_VCC1_S0IX5 CORE_VCC1_S0IX6 CORE_VCC1_S0IX11 CORE_VCC1_S0IX12 CORE_VCC1_S0IX13 CORE_VCC1_S0IX1
AD16 AD18 AD19 AF16 AF18 AF19 AF21 AF22 AJ19 AG16 AG18 AG19 AG21 AG22 AG24 AJ21 AJ22 AJ24 AK24
DDI_VGG_S0IX1 DDI_VGG_S0IX2 DDI_VGG_S0IX3 DDI_VGG_S0IX4 DDI_VGG_S0IX6 DDI_VGG_S0IX7 DDI_VGG_S0IX8 DDI_VGG_S0IX15 DDI_VGG_S0IX9 DDI_VGG_S0IX10 DDI_VGG_S0IX11 DDI_VGG_S0IX12 DDI_VGG_S0IX13 DDI_VGG_S0IX14 DDI_VGG_S0IX16 DDI_VGG_S0IX17 DDI_VGG_S0IX18 DDI_VGG_S0IX19
AK30 AK35 AK38 AM29
CORE_V1P15_S0IX1 CORE_V1P15_S0IX2 CORE_V1P15_S0IX3 CORE_V1P15_S0IX4
AA33 AJ35
FUSE_V1P15_S0IX2 FUSE_V1P15_S0IX1
AM19 AK21
DDI_V1P15_S0IX2 DDI_V1P15_S0IX1
INTEL_BRASWELL
REV = <REV>
UNCORE_VNN_S41 UNCORE_VNN_S42 UNCORE_VNN_S43 UNCORE_VNN_S44 UNCORE_VNN_S45 UNCORE_VNN_S46 UNCORE_VNN_S47 UNCORE_VNN_S48 UNCORE_VNN_S49 UNCORE_VNN_S410 UNCORE_VNN_S411 UNCORE_VNN_S412 UNCORE_VNN_S413 UNCORE_VNN_S414
AA18 AA19 AA21 AA22 AA24 AA25 AC18 AC19 AC21 AC22 AC24 AC25 AD25 AD27
RSVD60 AA30
UNCORE_V1P15_S0IX6 UNCORE_V1P15_S0IX1 UNCORE_V1P15_S0IX2 UNCORE_V1P15_S0IX3 UNCORE_V1P15_S0IX4 UNCORE_V1P15_S0IX5 UNCORE_V1P15_S0IX7 UNCORE_V1P15_S0IX8 UNCORE_V1P15_S0IX9 UNCORE_V1P15_S0IX10
V33 AA32 AA33 AA35 AA36 AC32 Y30 Y32 Y33 Y35
ICLK ICLK_GND_OFF2 ICLK_GND_OFF1 V19 V18
DDR DDR_V1P05A_G31 DDR_V1P05A_G34 DDR_V1P05A_G32 DDR_V1P05A_G35 DDR_V1P05A_G36 DDR_V1P05A_G33
AM21 AM33 AM22 AN22 AN32 AM32
PCIe PCIE_V1P05A_G31 PCIE_V1P05A_G32 V22 V24
SATA SATA_V1P05A_G32 SATA_V1P05A_G31 U24 U22
USB USB3_V1P05A_G32 USB3_V1P05A_G31 USBSSIC_V1P05A_G3 V27 U27 V29
FUSE FUSE3_V1P05A_G5 FUSE_V1P05A_G3 N18 U19
VNN
SC723 1UF/6.3V mbs_c0402
SC724 /X 1UF/6.3V mbs_c0402
SC725 /X 1UF/6.3V mbs_c0402
SC726 /X 10UF/6.3V mbs_c0603
SC727 /X 10UF/6.3V mbs_c0603
SC856 N/A 10UF/6.3V mbs_c0603
SC857 N/A 1UF/6.3V mbs_c0402
+VCCSRAMSOCIUN_1P05
SC729 /X 1UF/6.3V mbs_c0402
SC730 /X 1UF/6.3V mbs_c0402
SC731 /X 1UF/6.3V mbs_c0402
SC732 /X 1UF/6.3V mbs_c0402
SC733 /X 1UF/6.3V mbs_c0402
+VCCDIGICKSI0_1P05
SC734 /X 1UF/6.3V mbs_c0402
+VCCADDR_1P05
SC735 /X 1UF/6.3V mbs_c0402
SC736 /X 10UF/6.3V mbs_c0603
SC737 10UF/6.3V mbs_c0603
+VCCBMPD_MPHY_1P05
SC738 /X 1UF/6.3V mbs_c0402
SC739 1UF/6.3V mbs_c0402
SC740 1UF/6.3V mbs_c0402
+VCCPADSSICAON_1P05
SC741 /X 1UF/6.3V mbs_c0402
SC742 /X 1UF/6.3V mbs_c0402
+VCCF1_FUSE
SC743 1UF/6.3V mbs_c0402
+VCC1P05_FUSE
SC744 /X 1UF/6.3V mbs_c0402
SC745 /X 1UF/6.3V mbs_c0402
+1.05VSB
+VCCSRAMSOCIUN_1P05
SC746 /X 1UF/6.3V mbs_c0402
SC747 1UF/6.3V mbs_c0402
+VCCDIGICKSI0_1P05
SC728 22UF/6.3V mbs_c0603 /X
+VCCADDR_1P05
+VCCBMPD_MPHY_1P05
+VCCPADSSICAON_1P05
+VCCF1_FUSE
+VCC1P05_FUSE
+1.05VSB
SC748 10UF/6.3V mbs_c0603
SC749 /X 10UF/6.3V mbs_c0603
SC750 /X 10UF/6.3V mbs_c0603
SC751 /X 10UF/6.3V mbs_c0603
SC752 /X 10UF/6.3V mbs_c0603
+1.15VSB
+VCCRAM0CPU0SI1_1P15
+VCCFHVCPU0SI0_1P15
+VCCSRAMGEN_1P15

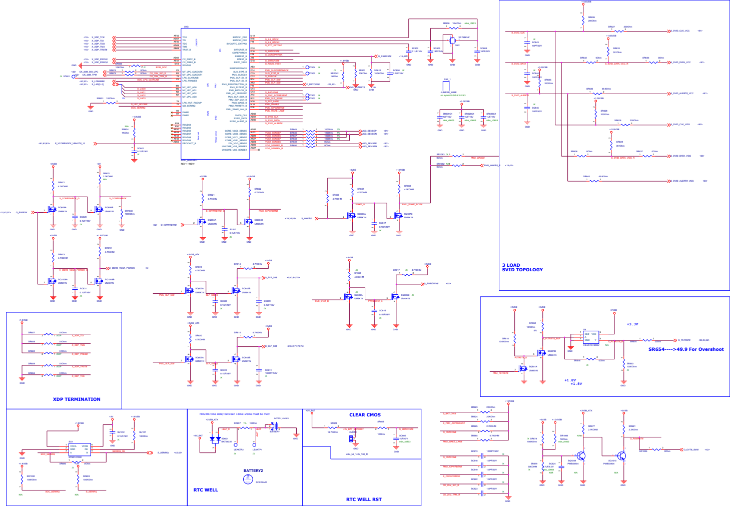


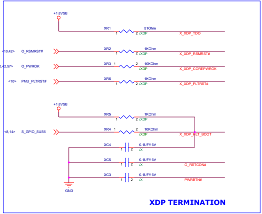
All straps are sampled on the rising edge of **PMU_RSMRST_N**.

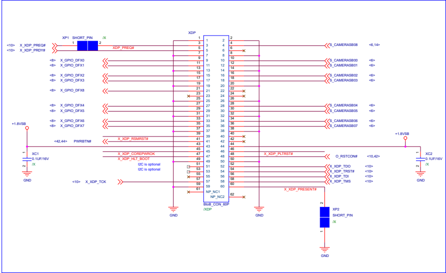
Table 2-27. Straps

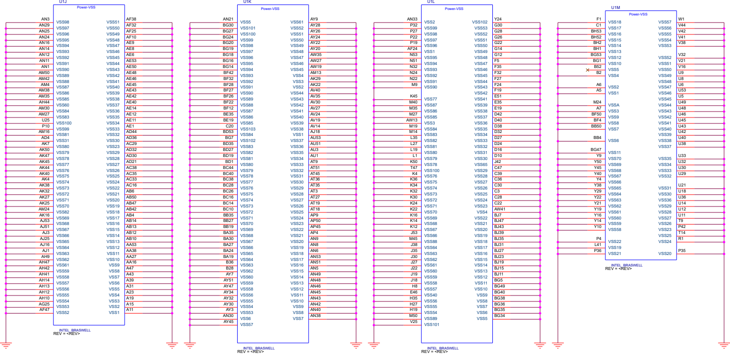
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass

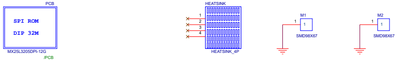

U1I
INTEL_BRASWELL
REV = <REV>
DDR
USB
RTC
FUSE
may connected to GND
may connected to GND
may connected to GND
SD3 IO SUPPLY
LPC IO SUPPLY
AUDIO IO SUPPLY
+1.5VDUAL
+1.8VSB
+1.24VSB
+1.05VSB
+3VSB
+3V_BAT
+3V
VNN


3 LOAD
SVID TOPOLOGY
SR654---->49.9 For Overshoot
+3.3V
+1.8V
XDP TERMINATION
PDG:RC time delay between 18ms~25ms must be met!
CLEAR CMOS
BATTERY2
RTC WELL
RTC WELL RST

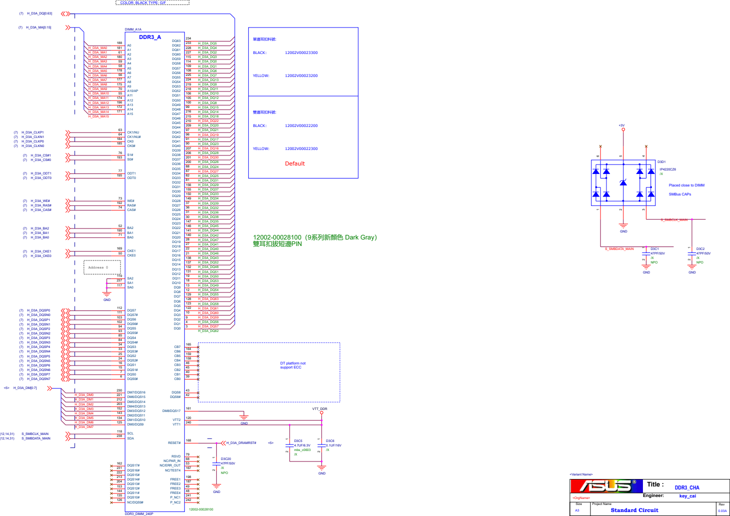

+1.8VSB
XR1 51Ohm /XDP X_XDP_TDO
<10,42> O_RSMRST# XR2 1KOhm /XDP X_XDP_RSMRST#
<10,42,57> O_PWROK XR3 10KOhm /XDP X_XDP_COREPWROK
<10> PMU_PLTRST# XR6 1KOhm /XDP X_XDP_PLTRST#
+1.8VSB
XR5 1KOhm /XDP
<8,14> S_GPIO_SUS6 XR4 10KOhm /XDP X_XDP_HLT_BOOT
XC4 0.1UF/16V /X
XC5 0.1UF/16V /X O_RSTCON#
XC3 0.1UF/16V /X PWRBTN#
GND
XDP TERMINATION


XDP
<10> X_XDP_PREQ#
<10> X_XDP_PRDY#
XP1 SHORT_PIN /X
XDP_PREQ#
S_CAMERASB08 <6,14>
<8> X_GPIO_DFX0
<8> X_GPIO_DFX1
<8> X_GPIO_DFX2
<8> X_GPIO_DFX3
<8> X_GPIO_DFX8
<8> X_GPIO_DFX4
<8> X_GPIO_DFX5
<8> X_GPIO_DFX6
<8> X_GPIO_DFX7
S_CAMERASB00 <6>
S_CAMERASB01 <6>
S_CAMERASB02 <6>
S_CAMERASB03 <6>
S_CAMERASB04 <6>
S_CAMERASB05 <6>
S_CAMERASB06 <6>
S_CAMERASB07 <6>
+1.8VSB
<42,44> PWRBTN#
X_XDP_RSMRST#
XC1 0.1UF/16V /X
X_XDP_COREPWROK
X_XDP_HLT_BOOT
I2C is optional
I2C is optional
X_XDP_PLTRST#
O_RSTCON# <10,42>
+1.8VSB
XC2 0.1UF/16V /X
X_XDP_TDO <10>
X_XDP_TRST# <10>
X_XDP_TDI <10>
X_XDP_TMS <10>
<10> X_XDP_TCK
NP_NC1
NP_NC2
BtoB_CON_60P
/XDP
X_XDP_PRESENT#
XP2 SHORT_PIN /X
GND



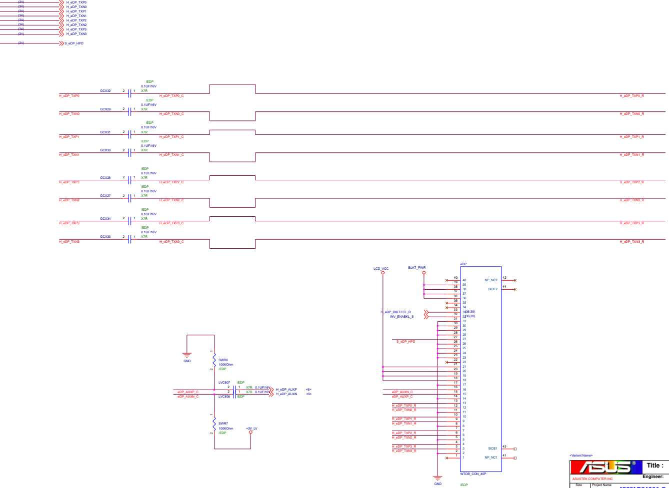


08001-04280000



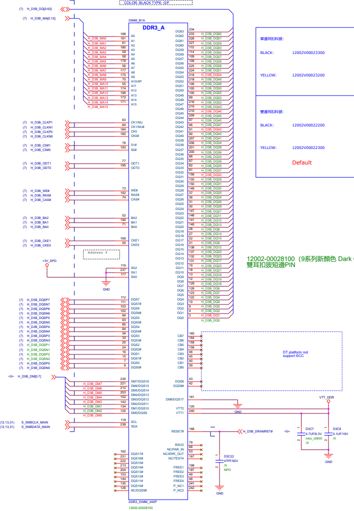
<Variant Name>

ASUS	Title : DDR3_CHA	
<OrgName>	Engineer: key_cai	
Size A3	Project Name Standard Circuit	Rev 0.03A
Date: Friday, March 27, 2015	Sheet 16 of 75	



<Variant Name>

ASUSTEK COMPUTER INC.	Title :	Clock GEN
	Engineer:	Alex_Jia
Size: A3	Project Name: ICS9LRS4206_Demo	Rev: 0.01C
Date: Friday, March 27, 2015	Sheet 20	of 75



單邊耳扣料號:

BLACK: 12002V00023300

YELLOW: 12002V00023200

雙邊耳扣料號:

BLACK: 12002V00022200

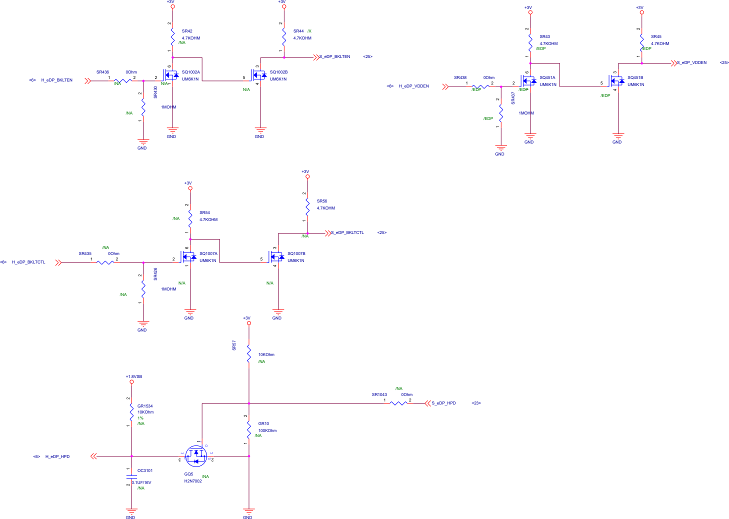
YELLOW: 12002V00022300

Default

12002-00028100（9系列新顏色 Dark Gray）
雙耳扣拔短邊PIN

<Variant Name>

<OrgName>	Title : DDR3_CHB	Engineer: key_cai
Size A3	Project Name **Standard Circuit**	Rev 0.03A
Date: Friday, March 27, 2015	Sheet 17	of 75


+3V
SR42
4.7KOHM
/NA
+3V
SR44 /X
4.7KOHM
S_eDP_BKLTEN
<25>
SR436
0Ohm
<6> H_eDP_BKLTEN
/NA
N/A
SQ1002A
UM6K1N
SR430
1MOHM
SQ1002B
UM6K1N
N/A
GND
GND
GND
+3V
SR43
4.7KOHM
/EDP
+3V
SR45
4.7KOHM
/EDP
S_eDP_VDDEN
<25>
SR438
0Ohm
<6> H_eDP_VDDEN
/EDP
/EDP
SQ451A
UM6K1N
SQ451B
UM6K1N
/EDP
SR437
/EDP
1MOHM
GND
GND
GND
+3V
SR56
4.7KOHM
+3V
SR54
4.7KOHM
/NA
/NA
S_eDP_BKLTCTL
<25>
/NA
SR435
0Ohm
<6> H_eDP_BKLTCTL
SQ1007A
UM6K1N
SQ1007B
UM6K1N
SR426
N/A
N/A
1MOHM
/NA
GND
GND
GND
+3V
SR57
10KOhm
/NA
+1.8VSB
/NA
SR1043
0Ohm
S_eDP_HPD
<23>
GR1534
10KOhm
1%
/NA
GR10
100KOhm
/NA
<6> H_eDP_HPD
OC3101
0.1UF/16V
/NA
GQ5
H2N7002
/NA
GND
GND

ASUS PCB Logo

PCB MADE IN CHINA

LOGO7 1 PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

LOGO5 1 WEEE_LOGO
WEEE_LOGO
/X

If don't need Component Silk,
delete this block

NEED_COMP_SILK

STANDARD CIRCUIT	
XUMR	OTHER

LOGO_HD_DEMO_OTHER
/X

New Project Logo

LOGO8 1 VCCI
VCCI
/X

LOGO4 1 MARK_L
MARK_L
/X

LOGO6 1 CE
CE
/X

LOGO2 1 FCC
FCC
/X

LOGO3 1 RCM
RCM
/X

LOGO1 1 EMI_D33005_H
EMI_D33005_H
/X

D33005

LOGO9 1 CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

CAN ICES-3 (B)/NMB-3(B)

Old Project Logo

<Variant Name>

ASUSTEK COMPUTER INC	Title : PCB Logo
	Engineer: Kell_Huang
Size A3	Project Name Silkscreen Demo Circuit	Rev 0.2A
Date: Friday, March 27, 2015	Sheet 2 of 75


<23> LVDS_TX_TA1N
LVDS_TX_TA1N_R <23>
<23> LVDS_TX_TA1P
LVDS_TX_TA1P_R <23>
<23> LVDS_TX_TB1N
LVDS_TX_TB1N_R <23>
<23> LVDS_TX_TB1P
LVDS_TX_TB1P_R <23>
<23> LVDS_TX_TC1N
LVDS_TX_TC1N_R <23>
<23> LVDS_TX_TC1P
LVDS_TX_TC1P_R <23>
<23> LVDS_TX_TD1N
LVDS_TX_TD1N_R <23>
<23> LVDS_TX_TD1P
LVDS_TX_TD1P_R <23>
<23> LVDS_TX_TCLK1N
<23> LVDS_TX_TCLK1P
<23> LVDS_TX_TCLK0N
<23> LVDS_TX_TCLK0P
GR267 1 2 0Ohm /LVDS_40
GR268 1 2 0Ohm /LVDS_40
GR269 1 2 0Ohm /LVDS_40
GR270 1 2 0Ohm /LVDS_40
LVDS_TX_TCLK1N_R <23>
LVDS_TX_TCLK1P_R <23>
LVDS_TX_TCLK0N_R <23>
LVDS_TX_TCLK0P_R <23>
<23> LVDS_TX_TA0N
LVDS_TX_TA0N_R <23>
<23> LVDS_TX_TA0P
LVDS_TX_TA0P_R <23>
<23> LVDS_TX_TB0N
LVDS_TX_TB0N_R <23>
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LVDS_TX_TC0N_R <23>
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LVDS_TX_TC0P_R <23>
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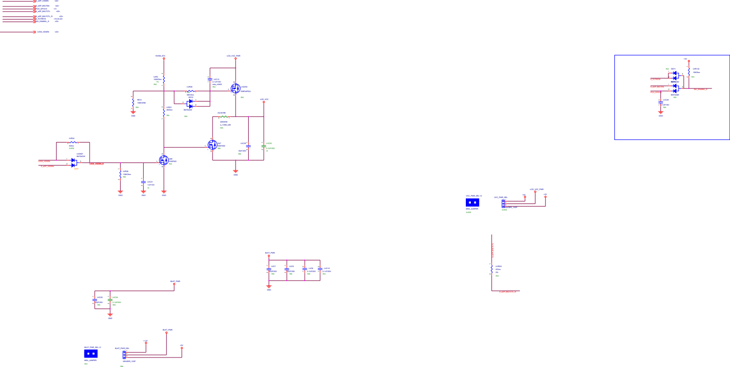
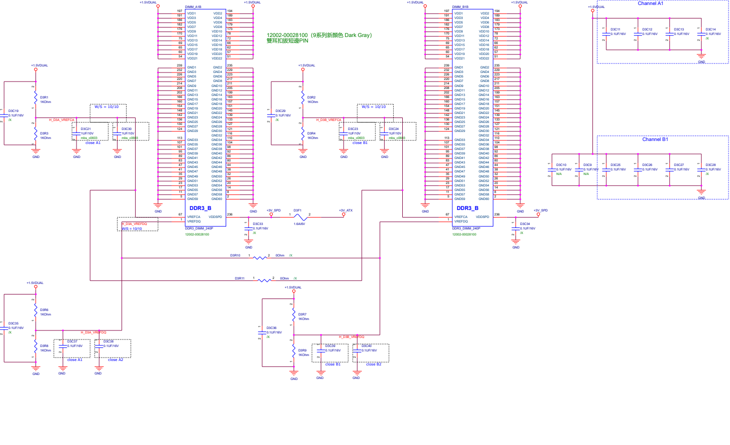
LVDS_TX_TD0P_R <23>

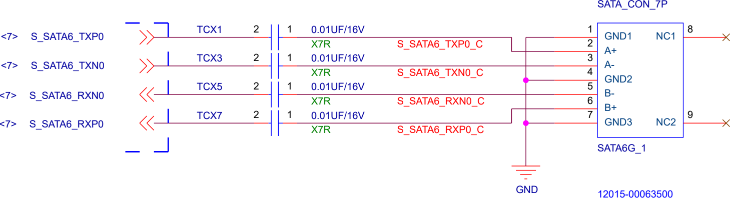


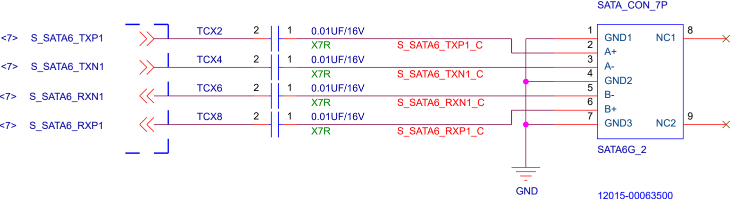
LVDS_VDDEN
LCD_VCC_PWR
LCD_VCC
GND
MINI_JUMPER
HEADER_1X3P
VCC_PWR_SEL
BLKT_PWR
BLKT_PWR_SEL
+12V
+5V
+3V

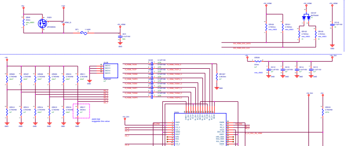


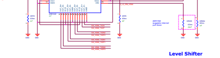
<Variant Name>

Title :	DDR3_POWER	
<OrgName>	Engineer:	key_cai
Size: A3	Project Name: Standard Circuit	Rev: 0.03A
Date: Friday, March 27, 2015	Sheet 18 of 75	


SATA_CON_7P
<7> S_SATA6_TXP0
<7> S_SATA6_TXN0
<7> S_SATA6_RXN0
<7> S_SATA6_RXP0
TCX1
TCX3
TCX5
TCX7
0.01UF/16V
X7R
S_SATA6_TXP0_C
S_SATA6_TXN0_C
S_SATA6_RXN0_C
S_SATA6_RXP0_C
GND1
A+
A-
GND2
B-
B+
GND3
NC1
NC2
SATA6G_1
GND
12015-00063500


SATA_CON_7P
<7> S_SATA6_TXP1
<7> S_SATA6_TXN1
<7> S_SATA6_RXN1
<7> S_SATA6_RXP1
TCX2
TCX4
TCX6
TCX8
0.01UF/16V
X7R
S_SATA6_TXP1_C
S_SATA6_TXN1_C
S_SATA6_RXN1_C
S_SATA6_RXP1_C
GND1
A+
A-
GND2
B-
B+
GND3
NC1
NC2
SATA6G_2
GND
12015-00063500

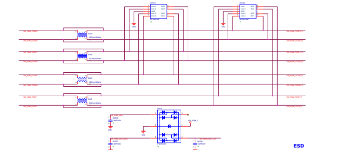




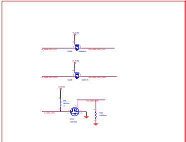
EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	1	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		

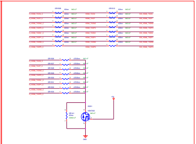
Level Shifter



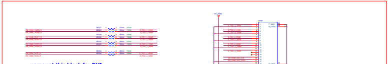
ESD



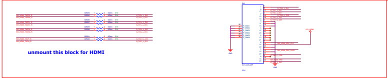
Level Shifter



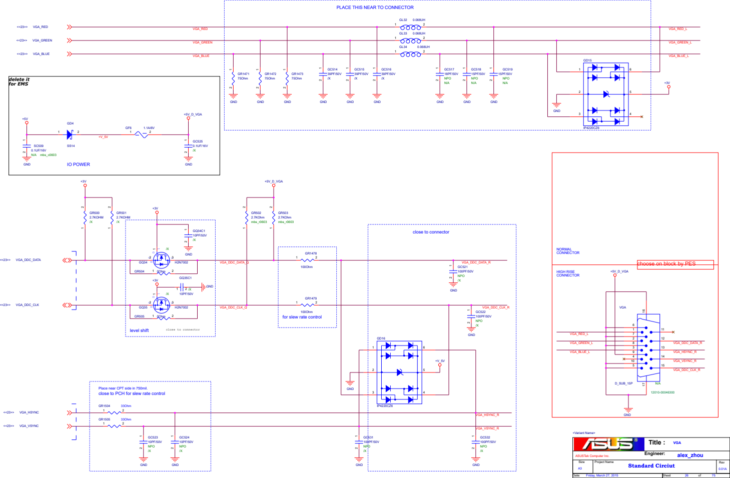
unmount this block for Level Shifter



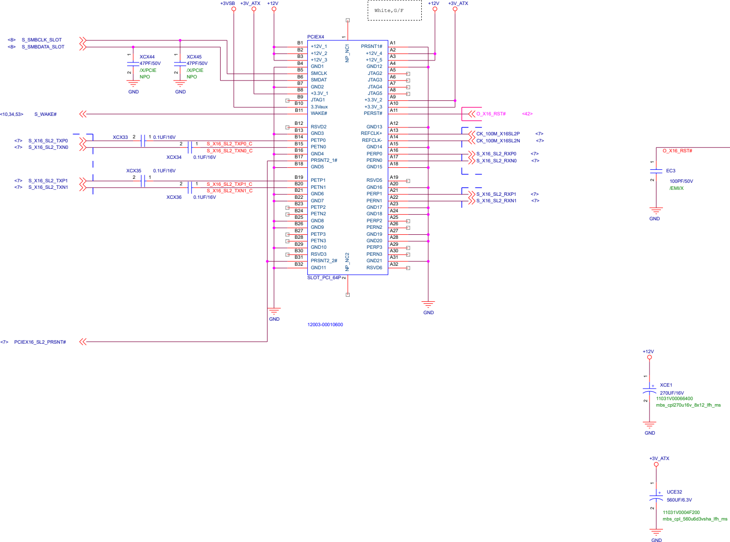
unmount this block for DVI

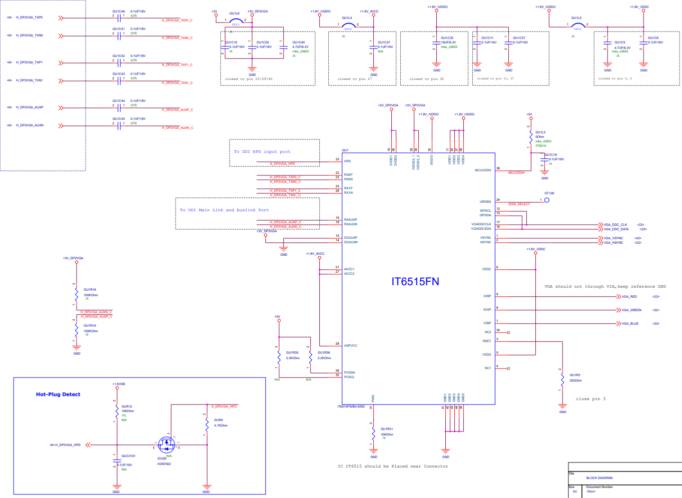


unmount this block for HDMI



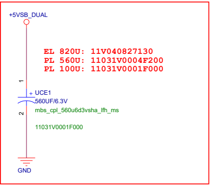
PLACE THIS NEAR TO CONNECTOR
<<23>> VGA_RED
<<23>> VGA_GREEN
<<23>> VGA_BLUE
GL32 0.068UH
GL33 0.068UH
GL34 0.068UH
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
GR1471 75Ohm
GR1472 75Ohm
GR1473 75Ohm
GC514 39PF/50V /X
GC515 39PF/50V /X
GC516 39PF/50V /X
GC517 18PF/50V NPO N/A
GC518 15PF/50V NPO N/A
GC519 15PF/50V NPO N/A
GD15
IP4220CZ6
+3V
GND
delete it for EMS
+5V
GD4
SS14
+V_5V
GF6 1.1A/6V
+5V_D_VGA
SC509 0.1UF/16V N/A mbs_c0603
GC525 0.1UF/16V /X
IO POWER
GR500 2.7KOHM /X
GR501 2.7KOHM /X
GQ34C1 10PF/50V /X
GQ34 H2N7002
GR504 0Ohm
GQ35C1 10PF/50V /X
GQ35 H2N7002
GR505 0Ohm
level shift
close to connector
<<23>> VGA_DDC_DATA
<<23>> VGA_DDC_CLK
GR502 2.7KOhm mbs_r0603
GR503 2.7KOhm mbs_r0603
VGA_DDC_DATA_Q
VGA_DDC_CLK_Q
GR1478 100Ohm
GR1479 100Ohm
for slew rate control
close to connector
VGA_DDC_DATA_R
VGA_DDC_CLK_R
GC521 100PF/50V NPO /X
GC522 100PF/50V NPO /X
GD16
IP4220CZ6
Place near CPT side in 750mil.
close to PCH for slew rate control
<<23>> VGA_HSYNC
<<23>> VGA_VSYNC
GR1504 33Ohm
GR1505 33Ohm
GC523 10PF/50V NPO /X
GC524 10PF/50V NPO /X
GC531 100PF/50V NPO /X
GC532 100PF/50V NPO /X
VGA_HSYNC_R
VGA_VSYNC_R
NORMAL CONNECTOR
HIGH RISE CONNECTOR
choose on block by PES
VGA
D_SUB_15P
N/A
12010-00046300
<Variant Name>
ASUS
Title : VGA
Engineer: alex_zhou
ASUSTek Computer Inc.
Size A3
Project Name
Standard Circiut
Rev 0.01A
Date: Friday, March 27, 2015
Sheet 26 of 75


+3VSB
+3V_ATX
+12V
White,G/F
PCIEX4
SLOT_PCI_64P
NP_NC1
NP_NC2
B1 +12V_1
B2 +12V_2
B3 +12V_3
B4 GND1
B5 SMCLK
B6 SMDAT
B7 GND2
B8 +3.3V_1
B9 JTAG1
B10 3.3Vaux
B11 WAKE#
B12 RSVD2
B13 GND3
B14 PETP0
B15 PETN0
B16 GND4
B17 PRSNT2_1#
B18 GND5
B19 PETP1
B20 PETN1
B21 GND6
B22 GND7
B23 PETP2
B24 PETN2
B25 GND8
B26 GND9
B27 PETP3
B28 PETN3
B29 GND10
B30 RSVD3
B31 PRSNT2_2#
B32 GND11
A1 PRSNT1#
A2 +12V_4
A3 +12V_5
A4 GND12
A5 JTAG2
A6 JTAG3
A7 JTAG4
A8 JTAG5
A9 +3.3V_2
A10 +3.3V_3
A11 PERST#
A12 GND13
A13 REFCLK+
A14 REFCLK-
A15 GND14
A16 PERP0
A17 PERN0
A18 GND15
A19 RSVD5
A20 GND16
A21 PERP1
A22 PERN1
A23 GND17
A24 GND18
A25 PERP2
A26 PERN2
A27 GND19
A28 GND20
A29 PERP3
A30 PERN3
A31 GND21
A32 RSVD6
12003-00010600
<8> S_SMBCLK_SLOT
<8> S_SMBDATA_SLOT
XCX44 47PF/50V /X/PCIE NPO
XCX45 47PF/50V /X/PCIE NPO
GND
<10,34,53> S_WAKE#
<7> S_X16_SL2_TXP0
<7> S_X16_SL2_TXN0
XCX33 0.1UF/16V
XCX34 0.1UF/16V
S_X16_SL2_TXP0_C
S_X16_SL2_TXN0_C
XCX35 0.1UF/16V
XCX36 0.1UF/16V
<7> S_X16_SL2_TXP1
<7> S_X16_SL2_TXN1
S_X16_SL2_TXP1_C
S_X16_SL2_TXN1_C
<7> PCIEX16_SL2_PRSNT#
O_X16_RST# <42>
CK_100M_X16SL2P <7>
CK_100M_X16SL2N <7>
S_X16_SL2_RXP0 <7>
S_X16_SL2_RXN0 <7>
S_X16_SL2_RXP1 <7>
S_X16_SL2_RXN1 <7>
O_X16_RST#
EC3 100PF/50V /EMI/X
XCE1 270UF/16V 11031V00066400 mbs_cpl270u16v_8x12_lfh_ms
UCE32 560UF/6.3V 11031V0004F200 mbs_cpl_560u6d3vsha_lfh_ms

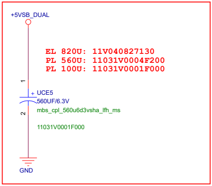


Title	BLOCK DIAGRAM		
Size A3	Document Number <Doc>		Rev V1.0
Date: Friday, March 27, 2015	Sheet 25 of 75		

PL CAP & EL CAP co-lay



PL CAP & EL CAP co-lay



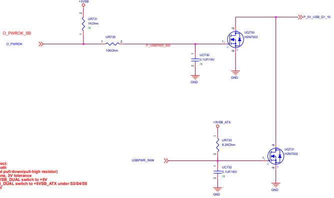
BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	USB
CS_USB_0.2B	

HD_DEMO_USB
/X

<Variant Name>

ASUSTEK COMPUTER INC	Title : USB CAP Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Friday, March 27, 2015	Sheet 22 of 100	



USBPWR_SW# GPIO select:
1. could be GPI & GPO both
2. default GPI (no internal pull-down/pull-high resistor)
3. +3VSB_ATX power plane, 3V tolerance
4. High level to force +5VSB_DUAL switch to +5V
5. Low level to let +5VSB_DUAL switch to +5VSB_ATX under S3/S4/S5
6. default need High level

<Variant Name>

ASUSTEK COMPUTER INC	Title : USB Power		
	Engineer: Kell_Huang		
Size A3	Project Name	Chipset USB Demo Circuit	Rev 0.0
Date: Friday, March 27, 2015	Sheet: 23	of 100	

Fiducial Mask
(光學點)

Delete it for EMS

圓形光學點

LayoutRD會依空間大小,
擺放大顆或小顆光學點;
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆光學點

小顆光學點

Delete it for EMS

十字光學點

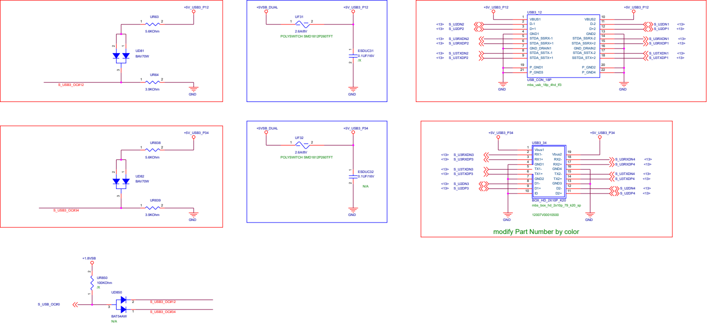
LayoutRD會依空間大小,
擺放大顆或小顆光學點;
所以兩種光學點都需畫入線路中,
最後再做刪除.

大顆光學點

小顆光學點

<Variant Name>

ASUSTEK COMPUTER INC	Title :	Fiducial Mask	
	Engineer:	Kell_Huang	
Size: A3	Project Name: Silkscreen Demo Circuit		Rev: 0.1B
Date: Friday, March 27, 2015		Sheet 3 of 75	



<Variant Name>

ASUS	Title : USB3 Port		
ASUSTEK COMPUTER INC	Engineer: Kell_Huang		
Size: A3	Project Name: Chipset USB Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015	Sheet 12	of 100	

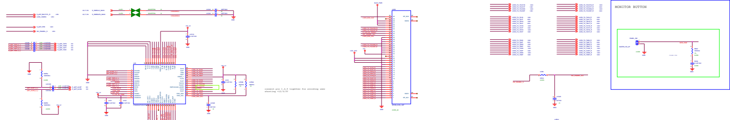
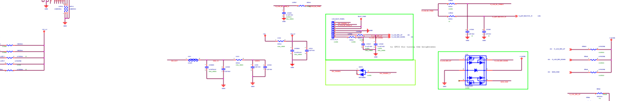
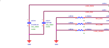
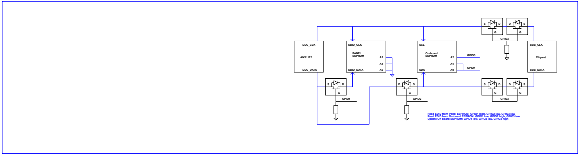


Table11. Power on Pins Configuration

Configuration Signal	Purpose	Definition
I2C_ADDR	I2C Slave address selection	L: 0x10h~0x1Fh H: 0x90h~0x9Fh
RLV_CFG	LVDS color depth and data mapping selection	L: 8-bit LVDS, VESA mapping M: 8-bit LVDS, JEIDA mapping H: 6-bit LVDS, both VESA and JEIDA mapping
RLV_LNK	LVDS single link or dual link selection	L: Single link LVDS H: Dual link LVDS







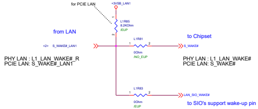
Note:

1. LAN IC power change to +3VSB_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)
2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN IC Page, and change BOM to use +3VSB_ATX power plane GPIO
3. for Intel PHY LAN, L1_LAN_DISABLE# pull high resistor L1R7 Optional change to /EUP
4. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN IC Page
5. for Intel PCIE LAN, L1_DEV_OFF# choose +3VSB_ATX power plane GPIO
6. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN IC Page

Hardware Solution

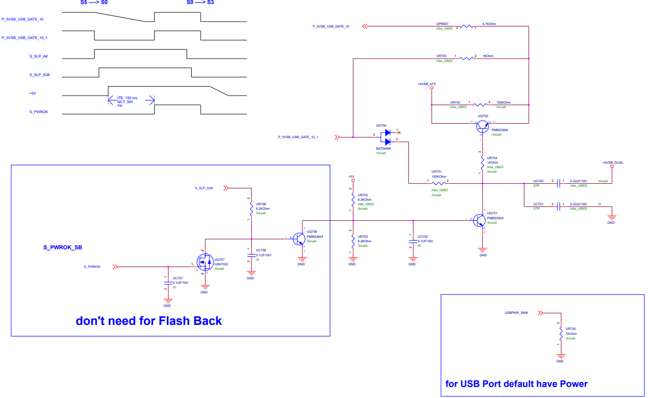
POWER

SIO Solution



<Variant Name>

ASUSTEK COMPUTER INC	Title :	Deep S4/S5 Wake
	Engineer:	Kell_Huang
Size: A3	Project Name: LAN Demo Circuit	Rev: 0.0
Date: Friday, March 27, 2015	Sheet 23 of 100	



Inrush Circuit for USB Port default have Power or Flash Back Function

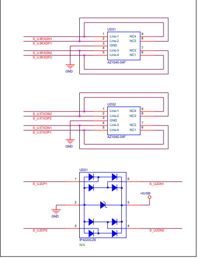
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB Inrush	
	Engineer: Kell_Huang	
Size A3	Project Name Chipset USB Demo Circuit	Rev 0.0
Date: Friday, March 27, 2015	Sheet 24 of 100	

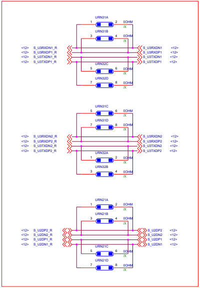
Port 12

Delete it for EMS

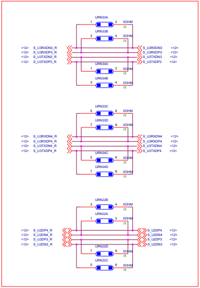
ESD Diode



Reserve Location (RES A)

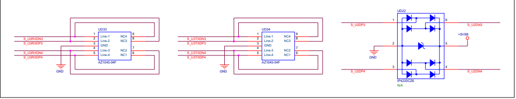


Reserve Location (RES A)



Delete it for EMS

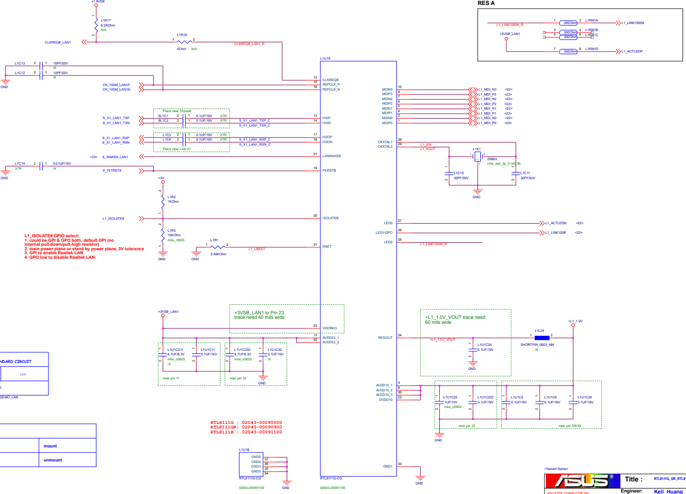
ESD Diode



Port 34

<Variant Name>

ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Friday, March 27, 2015	Sheet 13 of 100	



L1_ISOLATE# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI to enable Realtek LAN
4. GPO low to disable Realtek LAN

RTL8111G : 02043-00090500
RTL8111GR: 02043-00090900
RTL8111H : 02043-00091100

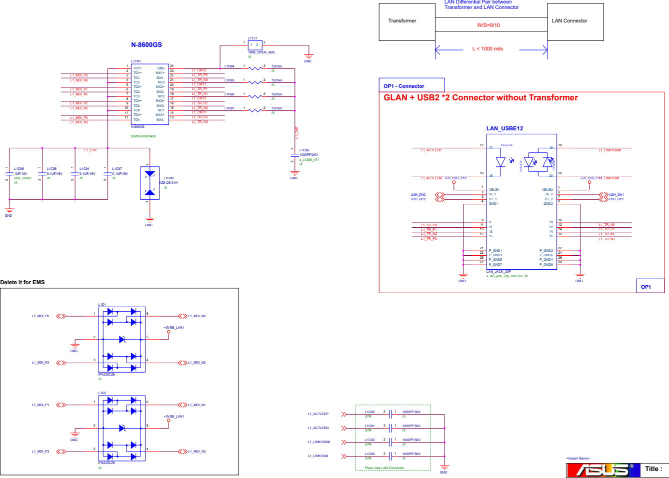
STANDARD CIRCUIT	
XOMB	LAN
LAN_0.4E	

LOGO_HD_DEMO_LAN
/X

BOM	
N/A	mount
/X	unmount

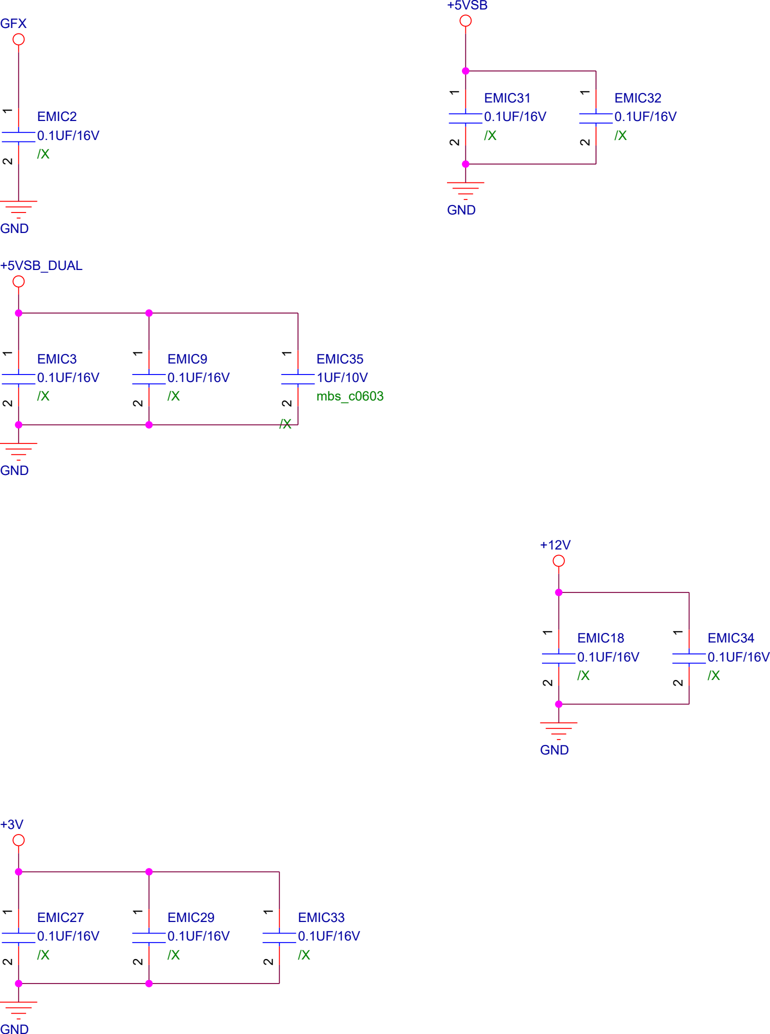
<Variant Name>

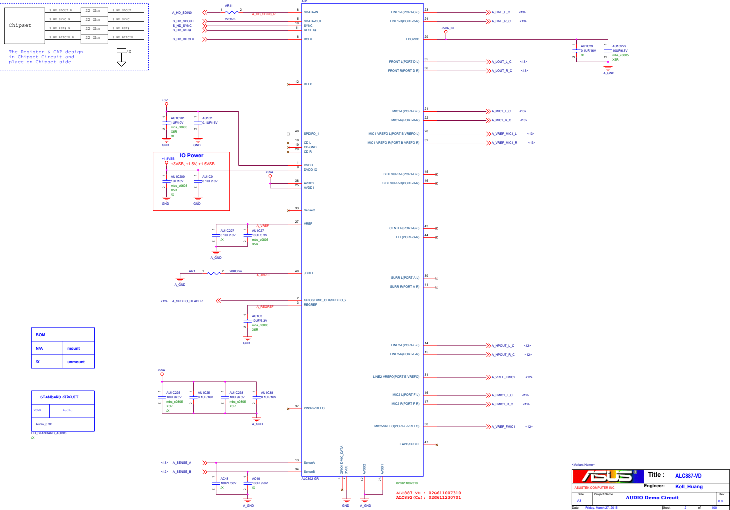
ASUSTEK COMPUTER INC	Title : RTL8111G_GR_RTL8111H
	Engineer: Kell_Huang
Size: A3	Project Name: LAN Demo Circuit
Rev: 0.0	
Date: Friday, March 27, 2015	Sheet 2 of 100



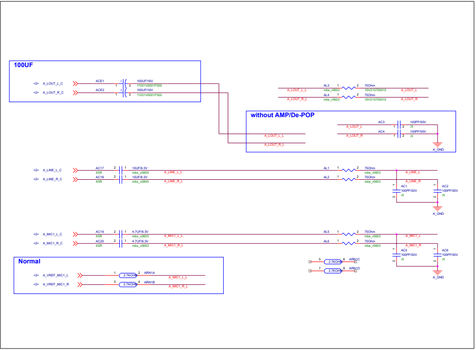
<Variant Name>

ASUSTEK COMPUTER INC	Title : LAN Connector	
	Engineer: Kell_Huang	
Size A3	Project Name LAN Demo Circuit	Rev 0.0
Date: Friday, March 27, 2015	Sheet 22 of 100	

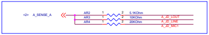

GFX
EMIC2
0.1UF/16V
/X
GND
+5VSB
EMIC31
0.1UF/16V
/X
EMIC32
0.1UF/16V
/X
GND
+5VSB_DUAL
EMIC3
0.1UF/16V
/X
EMIC9
0.1UF/16V
/X
EMIC35
1UF/10V
mbs_c0603
/X
GND
+12V
EMIC18
0.1UF/16V
/X
EMIC34
0.1UF/16V
/X
GND
+3V
EMIC27
0.1UF/16V
/X
EMIC29
0.1UF/16V
/X
EMIC33
0.1UF/16V
/X
GND

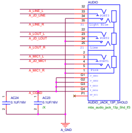

Chipset
S_HD_SDOUT_R 22 Ohm S_HD_SDOUT
S_HD_SYNC_R 22 Ohm S_HD_SYNC
S_HD_RST#_R 22 Ohm S_HD_RST#
S_HD_BITCLK_R 22 Ohm S_HD_BITCLK
The Resistor & CAP design
in Chipset Circuit and
place on Chipset side
/X
AU1
A_HD_SDIN0
AR11
A_HD_SDIN0_R
S_HD_SDOUT
S_HD_SYNC
S_HD_RST#
S_HD_BITCLK
22Ohm
SDATA-IN
SDATA-OUT
SYNC
RESET#
BCLK
BEEP
SPDIFO_1
CD-L
CD-GND
CD-R
DVDD
DVDD-IO
AVDD2
AVDD1
SenseC
VREF
JDREF
GPIO0/DMIC_CLK/SPDIFO_2
REGREF
PIN37-VREFO
SenseA
SenseB
ALC892-GR
GPIO1/DMIC_DATA
DVSS
AVSS2
AVSS1
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
LDOVDD
FRONT-L(PORT-D-L)
FRONT-R(PORT-D-R)
MIC1-L(PORT-B-L)
MIC1-R(PORT-B-R)
MIC1-VREFO-L(PORT-B-VREFO-L)
MIC1-VREFO-R(PORT-B-VREFO-R)
SIDESURR-L(PORT-H-L)
SIDESURR-R(PORT-H-R)
CENTER(PORT-G-L)
LFE(PORT-G-R)
SURR-L(PORT-A-L)
SURR-R(PORT-A-R)
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
LINE2-VREFO(PORT-E-VREFO)
MIC2-L(PORT-F-L)
MIC2-R(PORT-F-R)
MIC2-VREFO(PORT-F-VREFO)
EAPD/SPDIFI
A_LINE_L_C <13>
A_LINE_R_C <13>
+5VA_IN
AU1C29 0.1UF/16V /X
AU1C229 10UF/6.3V mba_c0805 X5R
A_GND
A_LOUT_L_C <13>
A_LOUT_R_C <13>
A_MIC1_L_C <13>
A_MIC1_R_C <13>
A_VREF_MIC1_L <13>
A_VREF_MIC1_R <13>
A_HPOUT_L_C <12>
A_HPOUT_R_C <12>
A_VREF_FMIC2 <12>
A_FMIC1_L_C <12>
A_FMIC1_R_C <12>
A_VREF_FMIC1 <12>
+3V
AU1C201 1UF/10V mba_c0603 X5R /X
AU1C1 0.1UF/16V
GND
IO Power
+1.8VSB
+3VSB, +1.5V, +1.5VSB
AU1C209 1UF/10V mba_c0603 X5R /X
AU1C9 0.1UF/16V
+5VA
A_VREF
AU1C227 0.1UF/16V /X
AU1C27 10UF/6.3V mba_c0805 X5R
AR1 20KOhm
A_JDREF
<12> A_SPDIFO_HEADER
A_REGREF
AU1C3 10UF/6.3V mba_c0805 X5R
BOM
N/A mount
/X unmount
STANDARD CIRCUIT
Audio_0.3D
HD_STANDARD_AUDIO
/X
AU1C225 10UF/6.3V mba_c0805 X5R /X
AU1C25 0.1UF/16V
AU1C238 10UF/6.3V mba_c0805 X5R
AU1C38 0.1UF/16V
<13> A_SENSE_A
<12> A_SENSE_B
AC48 100PF/50V /X
AC49 100PF/50V /X
02G611007310
ALC887-VD : 02G611007310
ALC892 (Cu) : 02G611230701
<Variant Name>
ASUS
ASUSTEK COMPUTER INC
Title : ALC887-VD
Engineer: Kell_Huang
Size A3
Project Name
AUDIO Demo Circuit
Rev 0.0
Date: Friday, March 27, 2015
Sheet 2 of 100

Delete it for EMS



for ALC887-VD2/ALC892





DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207
Audio 10U: 11011-00066000
Gamer 10U: 11011-0006Z000
EL 100U : 11G040810743
PL 100U : 11031V0001F000
Audio 100U: 11011-00026000
Gamer 100U: 11011-0002Z000

<Variant Name>

ASUSTEK COMPUTER INC	Title : 3 Jacks		
	Engineer: Kell_Huang		
Size: A3	Project Name: AUDIO Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015		Sheet 13 of 100	

You can only choose 6 pcs point for your project! Please choose them by your need!

Intel Platform

Priority1, must choose if MB have these functions

1 LAN

IP1 IMPEDANCE_CONTROL /X

IP2 IMPEDANCE_CONTROL /X

2 PCIE GEN2/3

IP3 IMPEDANCE_CONTROL /X

IP4 IMPEDANCE_CONTROL /X

3 DDR3 DATA&CTRL

IP5 IMPEDANCE_CONTROL /X

4 USB2.0

IP7 IMPEDANCE_CONTROL /X

IP8 IMPEDANCE_CONTROL /X

Priority2, can choose if MB have these functions (by project)

1 DP/DVI/HDMI

IP9 IMPEDANCE_CONTROL /X

IP10 IMPEDANCE_CONTROL /X

2 USB3.0

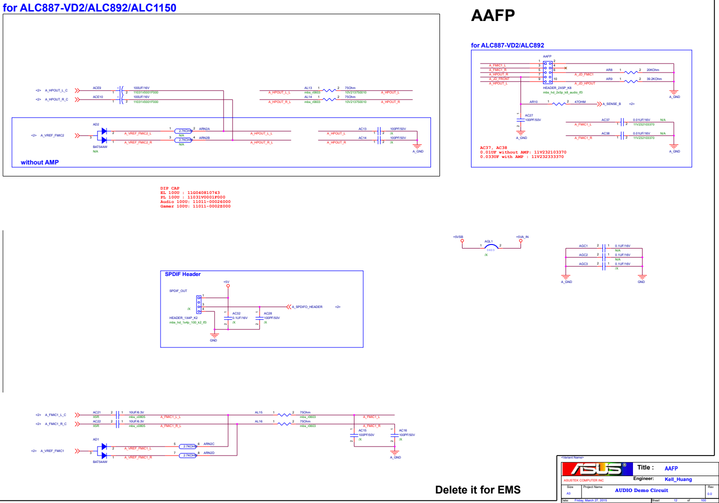
IP11 IMPEDANCE_CONTROL /X

IP12 IMPEDANCE_CONTROL /X

Delete it for EMS

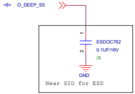
<Variant Name>

ASUSTEK COMPUTER INC	Title :	PCB Impedance Point	
	Engineer:	Kell_Huang	
Size: A3	Project Name	Silkscreen Demo Circuit	Rev: 0.1B
Date: Friday, March 27, 2015		Sheet 4 of 75	



for ALC887-VD2/ALC892/ALC1150
AAFP
for ALC887-VD2/ALC892
A_HPOUT_L_C
A_HPOUT_R_C
ACE9
ACE10
100UF/16V
11031V0001F000
AL13
AL14
75Ohm
mbs_r0603
10V213750010
A_HPOUT_L
A_HPOUT_R
A_VREF_FMIC2
AD2
BAT54AW
N/A
2.7KOHM
ARN2A
ARN2B
A_VREF_FMIC2_L
A_VREF_FMIC2_R
A_HPOUT_L_L
A_HPOUT_R_L
AC13
AC14
100PF/50V
/X
A_GND
without AMP
AAFP
A_FMIC1_L
A_FMIC1_R
A_HPOUT_R
A_JD_FRONT
A_HPOUT_L
HEADER_2X5P_K8
mbs_hd_2x5p_k8_audio_lf3
AR8
AR9
20KOhm
39.2KOhm
A_JD_FMIC1
A_JD_HPOUT
AR10
470HM
A_SENSE_B
AC27
100PF/50V
AC37
AC38
0.01UF/16V
11V232103370
AC37, AC38
0.01UF without AMP: 11V232103370
0.033UF with AMP : 11V232333370
DIP CAP
EL 100U : 11G040810743
PL 100U : 11031V0001F000
Audio 100U: 11011-00026000
Gamer 100U: 11011-0002Z000
+5VSB
AGL1
+5VA_IN
/X
AGC1
AGC2
AGC3
0.1UF/16V
GND
SPDIF Header
+5V
SPDIF_OUT
HEADER_1X4P_K2
mbs_hd_1x4p_100_k2_lf3
AC32
0.1UF/16V
AC28
100PF/50V
A_SPDIFO_HEADER
A_FMIC1_L_C
A_FMIC1_R_C
AC21
AC22
10UF/6.3V
XSR
mbs_c0805
A_FMIC1_L_L
A_FMIC1_R_L
AL15
AL16
75Ohm
mbs_r0603
A_FMIC1_L
A_FMIC1_R
AC15
AC16
100PF/50V
A_VREF_FMIC1
AD1
BAT54AW
A_VREF_FMIC1_L
A_VREF_FMIC1_R
2.7KOHM
ARN2C
ARN2D
Delete it for EMS
Title :
AAFP
ASUSTEK COMPUTER INC
Engineer:
Kell_Huang
Size
A3
Project Name
AUDIO Demo Circuit
Rev
0.0
Date:
Friday, March 27, 2015
Sheet
12
of
100

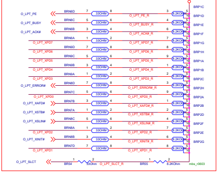
ERP Circuit



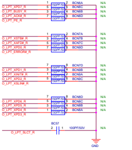
<Variant Name>

ASUSTEK COMPUTER INC	Title : ERP		
	Engineer: Kell_Huang		
Size: A4	Project Name: Super I/O Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015	Sheet 26 of 100		

RES A

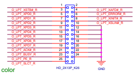


LPT PORT



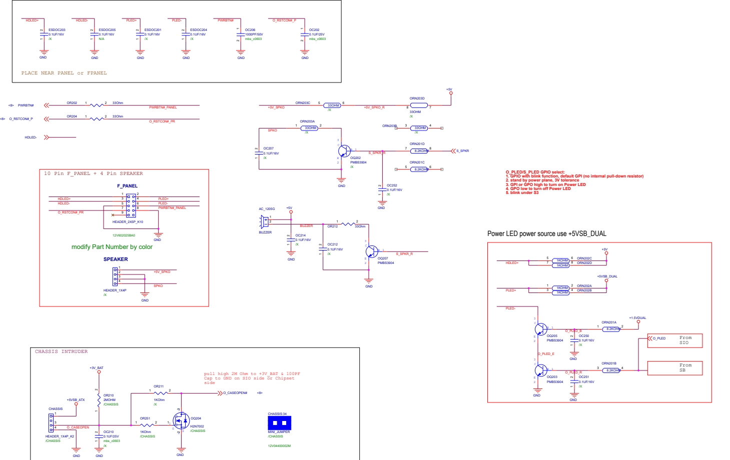
Power from VGA Port

LPT Header



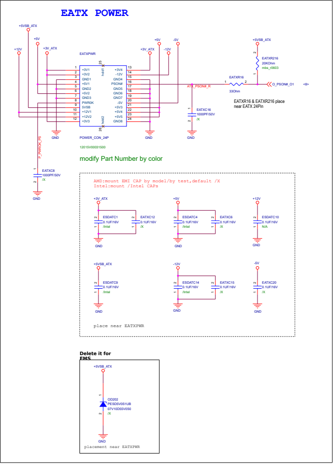
<Variant Name>

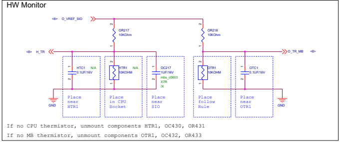
ASUSTEK COMPUTER INC	Title : COM_LPT	Engineer: Kell_Huang	
Size A3	Project Name	Super I/O Demo Circuit	Rev 0.0
Date: Friday, March 27, 2015	Sheet 43	of 75	

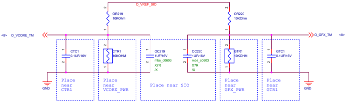


<Variant Name>

ASUS	Title :	PANEL	
ASUSTEK COMPUTER INC	Engineer:	Kell_Huang	
Size: A3	Project Name: Super I/O Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015	Sheet 23 of 100		



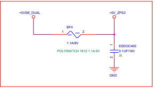




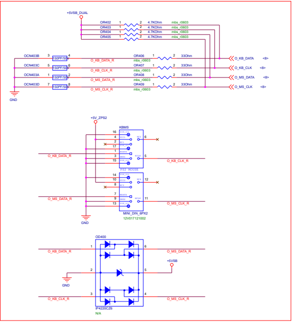
<Variant Name>

ASUSTEK COMPUTER INC	Title : EATX		
	Engineer: Kell_Huang		
Size: A3	Project Name: Super I/O Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015	Sheet 24	of 100	

Dedicated Power

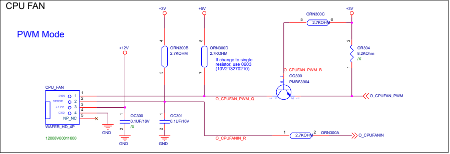


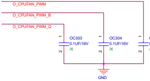
KBMS

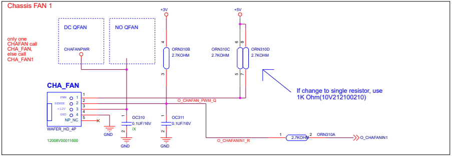


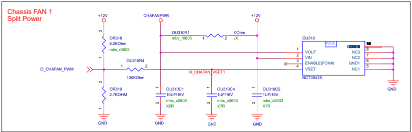
<Variant Name>

ASUSTEK COMPUTER INC	Title : KBMS		
	Engineer: Kell_Huang		
Size A3	Project Name Super I/O Demo Circuit		Rev 0.0
Date: Friday, March 27, 2015	Sheet 25	of 100	



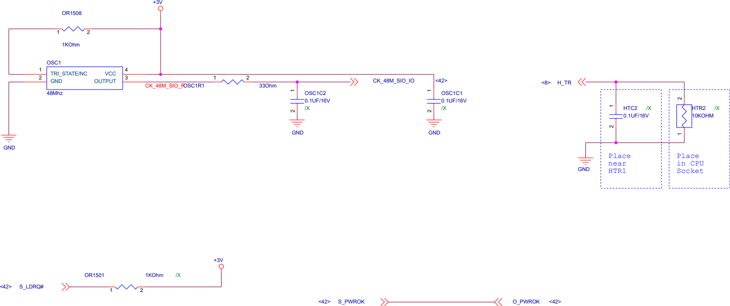






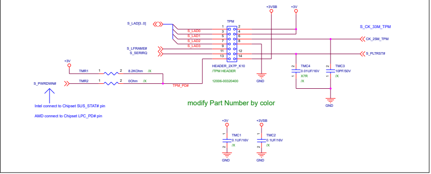
<Variant Name>

ASUSTEK COMPUTER INC	Title :	CPU_FAN		
	Engineer:	Kell_Huang		
Size: A3	Project Name	Super I/O Demo Circuit		Rev: 0.0
Date: Friday, March 27, 2015		Sheet 27	of 100	


+3V
OR1508
1
2
1KOhm
OSC1
1
TRI_STATE/NC
VCC
4
2
GND
OUTPUT
3
48Mhz
GND
CK_48M_SIO_R
OSC1R1
1
2
33Ohm
CK_48M_SIO_IO
<42>
OSC1C2
0.1UF/16V
/X
GND
OSC1C1
0.1UF/16V
/X
GND
<8>
H_TR
HTC2
/X
0.1UF/16V
HTR2
/X
10KOHM
GND
Place
near
HTR1
Place
in CPU
Socket
+3V
OR1501
1KOhm
/X
<42>
S_LDRQ#
1
2
<42>
S_PWROK
O_PWROK
<42>

Delete it for EMS

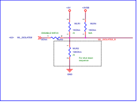
2x7 Pin TPM Header

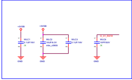


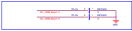
BOM	mount TPM	unmount TPM
/TPM	mount	unmount
/X	unmount	unmount

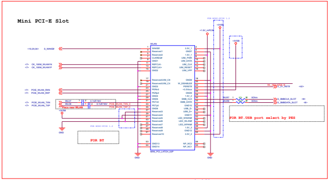
<Variant Name>

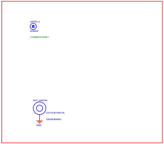
ASUSTEK COMPUTER INC	Title : TPM Header		
	Engineer: Kell_Huang		
Size A3	Project Name Other Demo Circuit		Rev 0.1C
Date: Friday, March 27, 2015	Sheet 12	of 100	


+3V
+3VSB
WLR1
WLR4
DISABLE WIFI/X
WL_ISOLATE#
WL_ISOLATE#_R
WLR2
For shut down sequence
GND

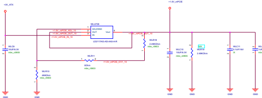

+3VSB
WLC1
WLC2
WLC3
WLC4
O_XT_RST#
GND

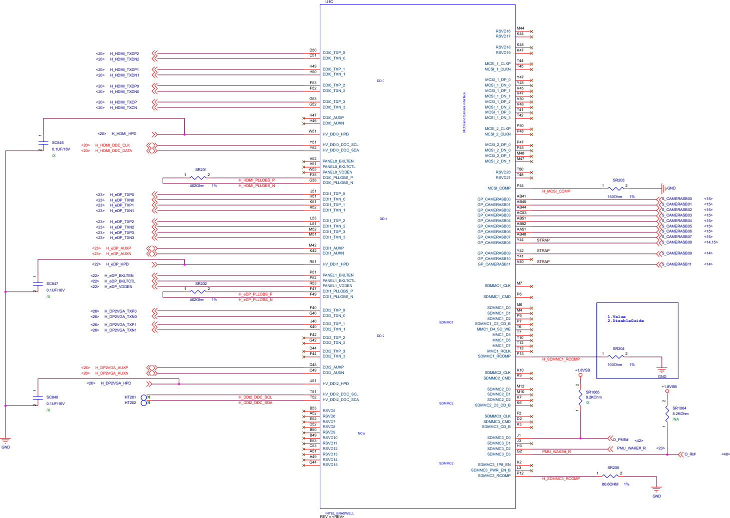

WLC5
WLC6
CK_100M_WLAN1P
CK_100M_WLAN1N
10PF/50V
GND


Mini PCI-E Slot
FOR MINI-PCIE 1.2
+1.5V_mPCIE
+3VSB
WLAN
S_WAKE#
CK_100M_WLAN1N
CK_100M_WLAN1P
PCIE_WLAN_RXN
PCIE_WLAN_RXP
PCIE_WLAN_TXN
PCIE_WLAN_TXP
WLC7
WLC8
0.1UF/16V
PCIE_WLAN_TXN_C
PCIE_WLAN_TXP_C
Place near WLAN
WAKE#
Reserved1
Reserved2
CLKREQ#
REFCLK-
REFCLK+
PERn0
PERp0
PETn0
PETp0
3.3V_1
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
W_DISABLE#
PERST#
+3.3Vaux
SMB_CLK
SMB_DATA
USB_D-
USB_D+
LED_WWAN#
LED_WLAN#
LED_WPAN#
MINI_PCI_LATCH_52P
WL_ISOLATE#_R
O_XT_RST#
WLR7
WLR8
0Ohm
S_SMBCLK_SLOT
S_SMBDATA_SLOT
FOR BT.USB port select by PES
FOR BT
GND

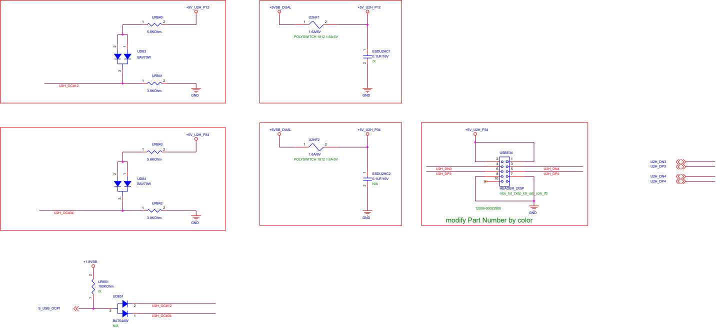

mSATA_2
SCREW
NUT_mSATA2
GND

Io=0.5A


+3V_ATX
+1.5V_mPCIE
WLU709
ADJ/GND
OUT
IN
Vout
LD2117AG-AD-AA3-A-R
+1.5V_mPCIE_ADJ_10
+1.5V_mPCIE_OUT_10
+1.5V_mPCIE_IN_10
+1.5V_mPCIE_OV1_10
WLC9
10UF/6.3V
WLR10
WLR11
0Ohm
WLR18
2.49KOhm
WLC10
10UF/6.3V
N/A
WLR19
2.49KOhm
WLC11
0.1UF/16V
WLC12
1UF/16V
GND



U1C
DDI0_TXP_0
DDI0_TXN_0
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_3
DDI0_TXN_3
DDI0_AUXP
DDI0_AUXN
HV_DDI0_HPD
HV_DDI0_DDC_SCL
HV_DDI0_DDC_SDA
PANEL0_BKLTEN
PANEL0_BKLTCTL
PANEL0_VDDEN
DDI0_PLLOBS_P
DDI0_PLLOBS_N
DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
HV_DDI1_HPD
PANEL1_BKLTEN
PANEL1_BKLTCTL
PANEL1_VDDEN
DDI1_PLLOBS_P
DDI1_PLLOBS_N
DDI2_TXP_0
DDI2_TXN_0
DDI2_TXP_1
DDI2_TXN_1
DDI2_TXP_2
DDI2_TXN_2
DDI2_TXP_3
DDI2_TXN_3
DDI2_AUXP
DDI2_AUXN
HV_DDI2_HPD
HV_DDI2_DDC_SCL
HV_DDI2_DDC_SDA
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
DDI0
DDI1
DDI2
NC's
SDMMC1
SDMMC2
SDMMC3
MCSI and Camera interface
RSVD16
RSVD17
RSVD18
RSVD19
MCSI_1_CLKP
MCSI_1_CLKN
MCSI_1_DP_0
MCSI_1_DN_0
MCSI_1_DP_1
MCSI_1_DN_1
MCSI_1_DP_2
MCSI_1_DN_2
MCSI_1_DP_3
MCSI_1_DN_3
MCSI_2_CLKP
MCSI_2_CLKN
MCSI_2_DP_0
MCSI_2_DN_0
MCSI_2_DP_1
MCSI_2_DN_1
RSVD20
RSVD21
MCSI_COMP
GP_CAMERASB00
GP_CAMERASB01
GP_CAMERASB02
GP_CAMERASB03
GP_CAMERASB04
GP_CAMERASB05
GP_CAMERASB06
GP_CAMERASB07
GP_CAMERASB08
GP_CAMERASB09
GP_CAMERASB10
GP_CAMERASB11
SDMMC1_CLK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3_CD_B
MMC1_D4_SD_WE
MMC1_D5
MMC1_D6
MMC1_D7
MMC1_RCLK
SDMMC1_RCOMP
SDMMC2_CLK
SDMMC2_CMD
SDMMC2_D0
SDMMC2_D1
SDMMC2_D2
SDMMC2_D3_CD_B
SDMMC3_CLK
SDMMC3_CMD
SDMMC3_CD_B
SDMMC3_D0
SDMMC3_D1
SDMMC3_D2
SDMMC3_D3
SDMMC3_1P8_EN
SDMMC3_PWR_EN_B
SDMMC3_RCOMP
<20> H_HDMI_TXDP2
<20> H_HDMI_TXDN2
<20> H_HDMI_TXDP1
<20> H_HDMI_TXDN1
<20> H_HDMI_TXDP0
<20> H_HDMI_TXDN0
<20> H_HDMI_TXCP
<20> H_HDMI_TXCN
<20> H_HDMI_HPD
<20> H_HDMI_DDC_CLK
<20> H_HDMI_DDC_DATA
SC846
0.1UF/16V
/X
SR201
402Ohm 1%
H_HDMI_PLLOBS_P
H_HDMI_PLLOBS_N
<23> H_eDP_TXP0
<23> H_eDP_TXN0
<23> H_eDP_TXP1
<23> H_eDP_TXN1
<23> H_eDP_TXP2
<23> H_eDP_TXN2
<23> H_eDP_TXP3
<23> H_eDP_TXN3
<23> H_eDP_AUXP
<23> H_eDP_AUXN
<22> H_eDP_HPD
<22> H_eDP_BKLTEN
<22> H_eDP_BKLTCTL
<22> H_eDP_VDDEN
SC847
0.1UF/16V
/X
SR202
402Ohm 1%
H_eDP_PLLOBS_P
H_eDP_PLLOBS_N
<26> H_DP2VGA_TXP0
<26> H_DP2VGA_TXN0
<26> H_DP2VGA_TXP1
<26> H_DP2VGA_TXN1
<26> H_DP2VGA_AUXP
<26> H_DP2VGA_AUXN
<26> H_DP2VGA_HPD
SC848
0.1UF/16V
/X
HT201
HT202
H_DDI2_DDC_SCL
H_DDI2_DDC_SDA
GND
SR203
150Ohm 1%
H_MCSI_COMP
GND
STRAP
STRAP
STRAP
S_CAMERASB00 <15>
S_CAMERASB01 <15>
S_CAMERASB02 <15>
S_CAMERASB03 <15>
S_CAMERASB04 <15>
S_CAMERASB05 <15>
S_CAMERASB06 <15>
S_CAMERASB07 <15>
S_CAMERASB08 <14,15>
S_CAMERASB09 <14>
S_CAMERASB11 <14>
1.Value
2.DisableGuide
SR204
100Ohm 1%
H_SDMMC1_RCOMP
GND
+1.8VSB
SR1065
8.2KOhm
/X
+1.8VSB
SR1064
8.2KOhm
/NA
O_PME# <42>
PMU_WAKE#_R <23>
PMU_WAKE#_R
O_RI# <48>
SR205
80.6OHM 1%
H_SDMMC3_RCOMP
GND
INTEL_BRASWELL
REV = <REV>

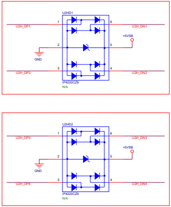


<Variant Name>

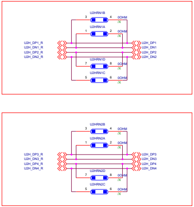
ASUSTEK COMPUTER INC	Title : USB2 HUB Port		
	Engineer: Kell_Huang		
Size: A3	Project Name: USB2 HUB Demo Circuit		Rev: 0.1C
Date: Friday, March 27, 2015	Sheet 43	of 100	

Delete it for EMS

ESD Diode

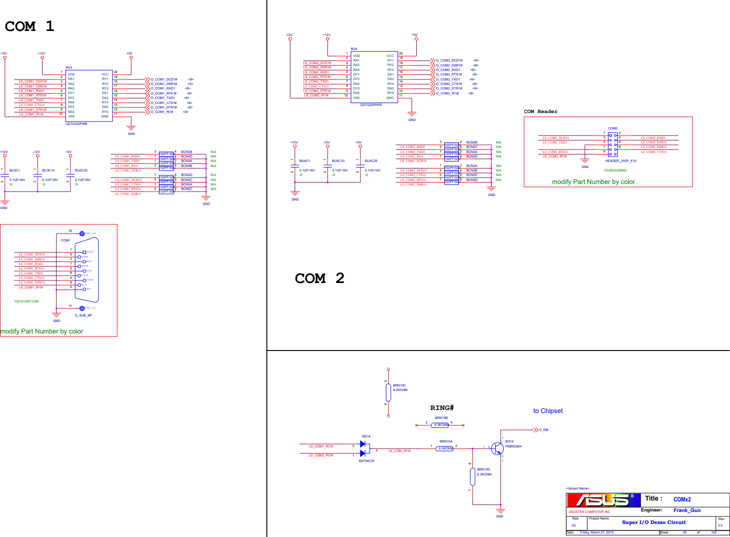


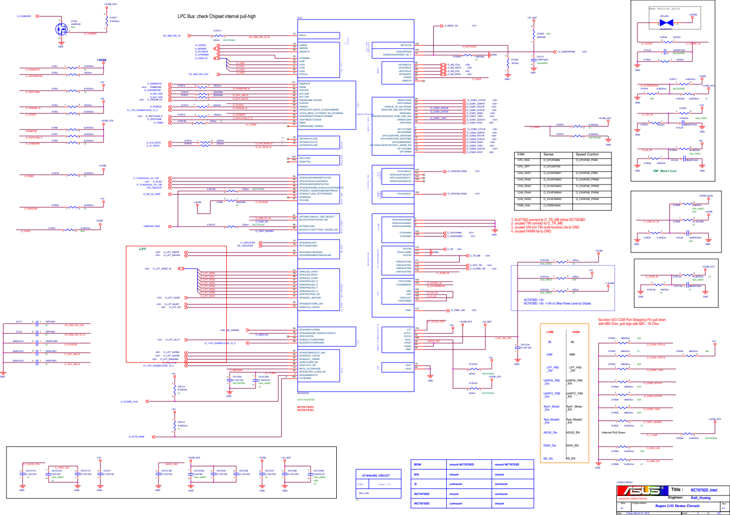
Reserve Location (RES A)



<Variant Name>

ASUSTEK COMPUTER INC	Title : USB2 HUB Port		
	Engineer: Kell_Huang		
Size: A3	Project Name: USB2 HUB Demo Circuit		Rev: 0.1C
Date: Friday, March 27, 2015	Sheet 44 of 100		


COM 1
BU3
GD75232PWR
LS_COM1_DCD1#
LS_COM1_DSR1#
LS_COM1_RXD1
LS_COM1_RTS1#
LS_COM1_TXD1
LS_COM1_CTS1#
LS_COM1_DTR1#
LS_COM1_RI1#
O_COM1_DCD1#
O_COM1_DSR1#
O_COM1_RXD1
O_COM1_RTS1#
O_COM1_TXD1
O_COM1_CTS1#
O_COM1_DTR1#
O_COM1_RI1#
GND
BU3C1
BU3C10
BU3C20
0.1UF/16V
BCN5B
BCN4D
BCN4A
BCN4B
BCN5D
BCN4C
BCN5A
BCN5C
N/A
COM1
12010-00011300
D_SUB_9P
modify Part Number by color
COM 2
BU4
GD75232PWR
LS_COM2_DCD1#
LS_COM2_DSR1#
LS_COM2_RXD1
LS_COM2_RTS1#
LS_COM2_TXD1
LS_COM2_CTS1#
LS_COM2_DTR1#
LS_COM2_RI1#
O_COM2_DCD1#
O_COM2_DSR1#
O_COM2_RXD1
O_COM2_RTS1#
O_COM2_TXD1
O_COM2_CTS1#
O_COM2_DTR1#
O_COM2_RI1#
BU4C1
BU4C10
BU4C20
BCN2B
BCN2C
BCN3A
BCN2D
BCN2A
BCN3B
BCN3C
BCN3D
COM Header
COM2
HEADER_2X5P_K10
12V602025BA0
modify Part Number by color
BRN10C
8.2KOHM
RING#
BRN10B
to Chipset
O_RI#
BD14
BAT54CW
LS_COM1_RI1#
LS_COM2_RI1#
LS_COM_RI1#
BRN10A
BQ14
PMBS3904
BRN10D
<Variant Name>
Title : COMx2
ASUSTEK COMPUTER INC
Engineer: Frank_Guo
Project Name
Super I/O Demo Circuit
Size A3
Rev 0.0
Date: Friday, March 27, 2015
Sheet 42 of 100



FAN	Sense	Speed Control
CPU_FAN	O_CPUFANIN	O_CPUFAN_PWM
CPU_OPT	O_CPUOPTIN	
CHA_FAN1	O_CHAFANIN1	O_CHAFAN_PWM
CHA_FAN2	O_CHAFANIN2	O_CHAFAN_PWM2
CHA_FAN3	O_CHAFANIN3	O_CHAFAN_PWM3
CHA_FAN4	O_CHAFANIN4	O_CHAFAN_PWM4
CHA_FAN5	O_CHAFANIN5	O_CHAFAN_PWM5
PWR_FAN	O_PWRFANIN	

LOW	HIGH
2E	4E
24M	48M
LPT_P80_Dis	LPT_P80_EN
UARTA_P80_Dis	UARTA_P80_EN
UARTC_P80_Dis	UARTC_P80_EN
Test1_Mode_Dis	Test1_Mode_EN
Test_Mode0_Dis	Test_Mode0_EN
ASUS_Dis	ASUS_EN
DSW_Dis	DSW_EN
K8_Dis	K8_EN

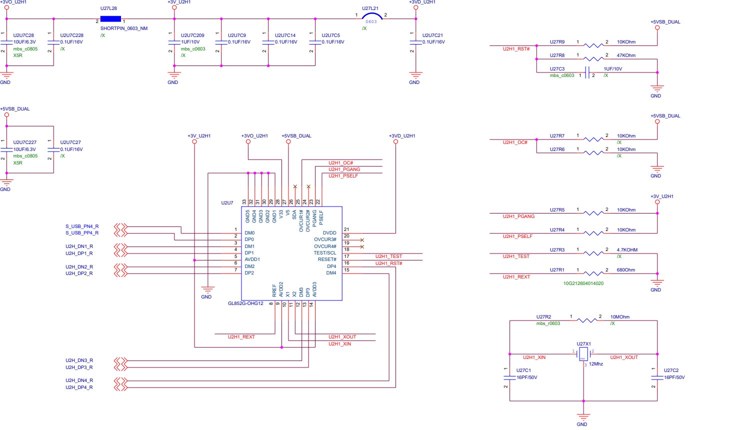
BOM	mount NCT6792D	mount NCT6793D
N/A	mount	mount
/X	unmount	unmount
/NCT6792D	mount	unmount
/NCT6793D	unmount	mount

Delete it for EMS

COM Debug Header

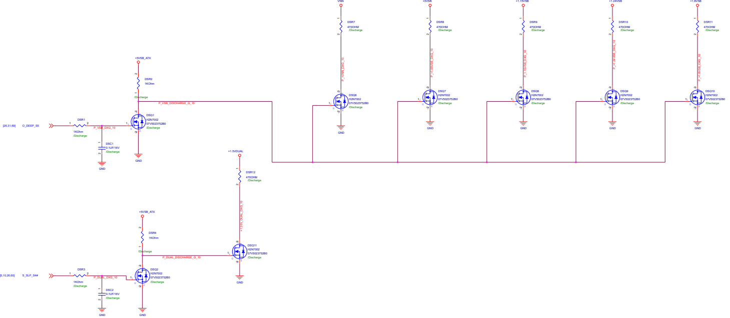
<Variant Name>

ASUSTEK COMPUTER INC	Title :	Debug Header	
	Engineer:	Kell_Huang	
Size: A	Project Name: Other Demo Circuit		Rev: 0.1C
Date: Friday, March 27, 2015	Sheet 22 of 100		



<Variant Name>

ASUSTEK COMPUTER INC	Title : GL852		
	Engineer: Kell_Huang		
Size: A4	Project Name: USB2 HUB Demo Circuit		Rev: 0.1C
Date: Friday, March 27, 2015	Sheet 42	of 100	



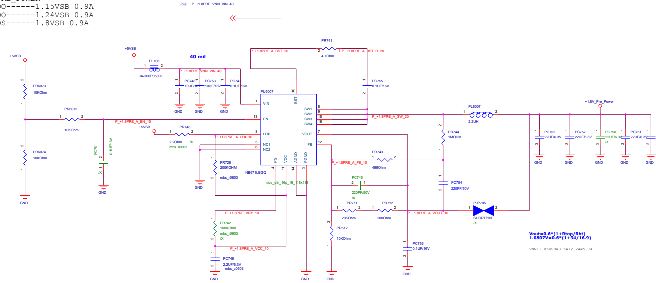
<Variant Name>

ASUSTEK COMPUTER INC	Title :	
	Engineer:	
Size: Custom	Project Name	Rev: 0.1C
Date: Friday, March 27, 2015	Sheet 56 of 75	

+5VSB===>+1.8V_Pre_Power

(1.804V)

```
1.8_PRE_POWER
---LDO------1.15VSB 0.9A
---LDO------1.24VSB 0.9A
---MOS------1.8VSB 0.9A
```

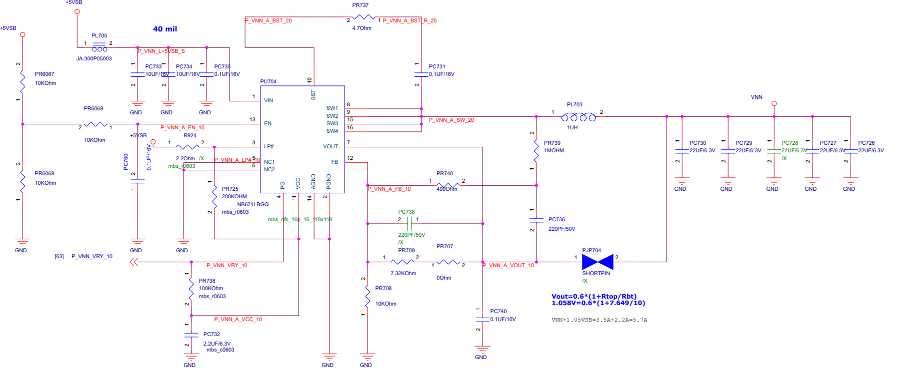


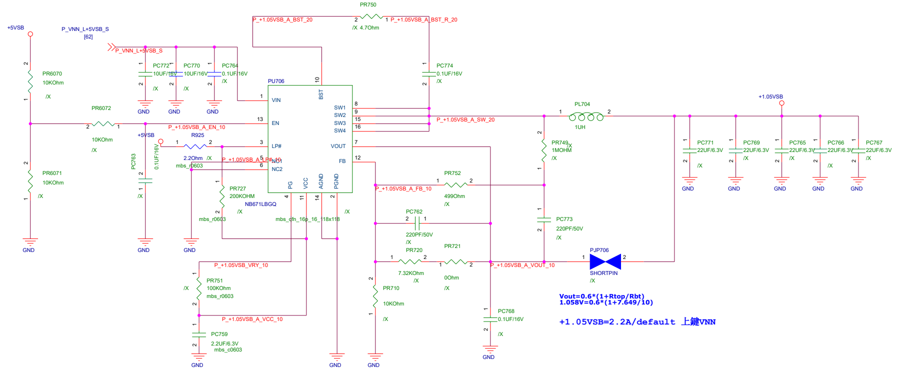
Vout=0.6*(1+Rtop/Rbt)
1.0807V=0.6*(1+34/16.9)

VNN=1.05VSB=3.5A+2.2A=5.7A

<Variant Name>

ASUS	**Title :**	1.8		
ASUSTek Computer Inc.	**Engineer:**	**ABEL_YANG**		
Size: Custom	Project Name: **BWIC**			Rev: 1.00
Date: Friday, March 27, 2015		Sheet 62	of 74	



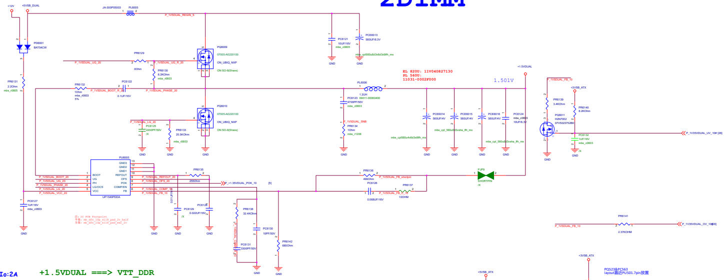


<Variant Name>

ASUSTek Computer Inc.	Title : VNN		
	Engineer: ABEL_YANG		
Size: Custom	Project Name: BWIC		Rev: 1.00
Date: Friday, March 27, 2015		Sheet 59 of 74	

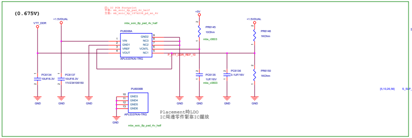
+5VSB_DUAL ===> +1.5VDUAL Io:12A

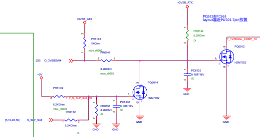
2DIMM



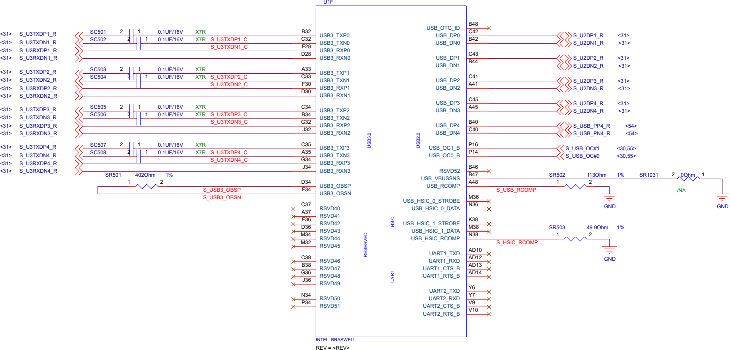
Io:2A

+1.5VDUAL ===> VTT_DDR

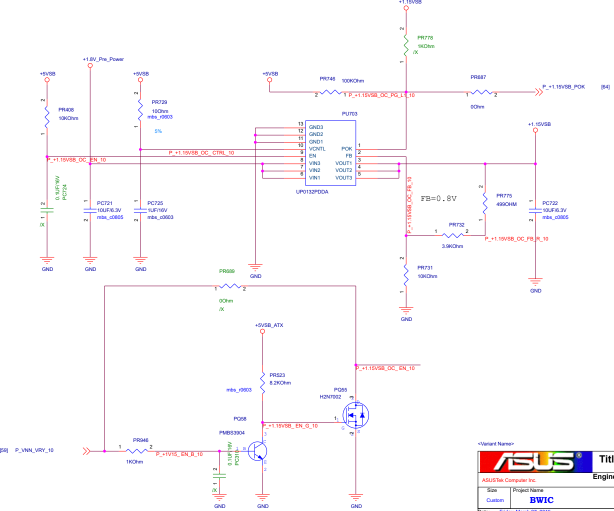




P_O_+1.35V_SET	P_O_+1.2V_SET		+1.5VDUAL
0	0		1.2V(1.209V)
X	0		1.35V(1.362V)
0	X		1.5V(1.515V)
X	X		1.65V(1.669V)



U1F
<31> S_U3TXDP1_R
<31> S_U3TXDN1_R
<31> S_U3RXDP1_R
<31> S_U3RXDN1_R
SC501 2 1 0.1UF/16V X7R
SC502 2 1 0.1UF/16V X7R S_U3TXDP1_C
S_U3TXDN1_C
B32 USB3_TXP0
C32 USB3_TXN0
F28 USB3_RXP0
D28 USB3_RXN0
<31> S_U3TXDP2_R
<31> S_U3TXDN2_R
<31> S_U3RXDP2_R
<31> S_U3RXDN2_R
SC503 2 1 0.1UF/16V X7R
SC504 2 1 0.1UF/16V X7R S_U3TXDP2_C
S_U3TXDN2_C
A33 USB3_TXP1
C33 USB3_TXN1
F30 USB3_RXP1
D30 USB3_RXN1
<31> S_U3TXDP3_R
<31> S_U3TXDN3_R
<31> S_U3RXDP3_R
<31> S_U3RXDN3_R
SC505 2 1 0.1UF/16V X7R
SC506 2 1 0.1UF/16V X7R S_U3TXDP3_C
S_U3TXDN3_C
C34 USB3_TXP2
B34 USB3_TXN2
G32 USB3_RXP2
J32 USB3_RXN2
<31> S_U3TXDP4_R
<31> S_U3TXDN4_R
<31> S_U3RXDP4_R
<31> S_U3RXDN4_R
SC507 2 1 0.1UF/16V X7R
SC508 2 1 0.1UF/16V X7R S_U3TXDP4_C
S_U3TXDN4_C
C35 USB3_TXP3
A35 USB3_TXN3
G34 USB3_RXP3
J34 USB3_RXN3
SR501 402Ohm 1%
1 2
D34 USB3_OBSP
F34 USB3_OBSN
S_USB3_OBSP
S_USB3_OBSN
USB3.0
C37 RSVD40
A37 RSVD41
F36 RSVD42
D36 RSVD43
M34 RSVD44
M32 RSVD45
C38 RSVD46
B38 RSVD47
G36 RSVD48
J36 RSVD49
N34 RSVD50
P34 RSVD51
RESERVED
INTEL_BRASWELL
REV = <REV>
USB2.0
B48 USB_OTG_ID
C42 USB_DP0
B42 USB_DN0
S_U2DP1_R <31>
S_U2DN1_R <31>
C43 USB_DP1
B44 USB_DN1
S_U2DP2_R <31>
S_U2DN2_R <31>
C41 USB_DP2
A41 USB_DN2
S_U2DP3_R <31>
S_U2DN3_R <31>
C45 USB_DP3
A45 USB_DN3
S_U2DP4_R <31>
S_U2DN4_R <31>
B40 USB_DP4
C40 USB_DN4
S_USB_PP4_R <54>
S_USB_PN4_R <54>
P16 USB_OC1_B
P14 USB_OC0_B
S_USB_OC#1 <30,55>
S_USB_OC#0 <30,55>
B46 RSVD52
B47 USB_VBUSSNS
A48 USB_RCOMP
SR502 113Ohm 1%
1 2
S_USB_RCOMP
GND
SR1031 2 0Ohm 1
/NA
GND
HSIC
M36 USB_HSIC_0_STROBE
N36 USB_HSIC_0_DATA
K38 USB_HSIC_1_STROBE
M38 USB_HSIC_1_DATA
N38 USB_HSIC_RCOMP
SR503 49.9Ohm 1%
1 2
S_HSIC_RCOMP
GND
UART
AD10 UART1_TXD
AD12 UART1_RXD
AD13 UART1_CTS_B
AD14 UART1_RTS_B
Y6 UART2_TXD
Y7 UART2_RXD
V9 UART2_CTS_B
V10 UART2_RTS_B



<Variant Name>

ASUS

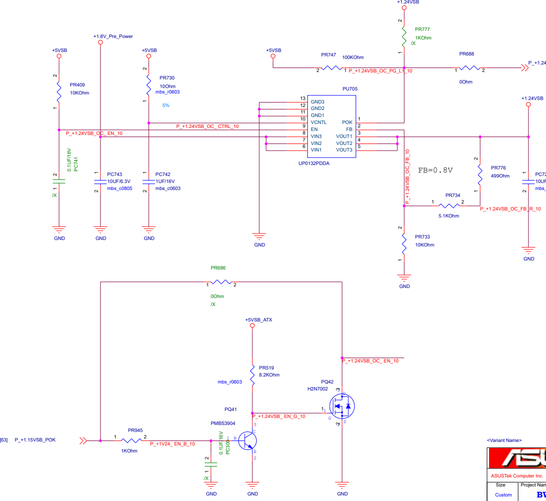
Title : 1.15

ASUSTek Computer Inc.

Engineer: ABEL_YANG

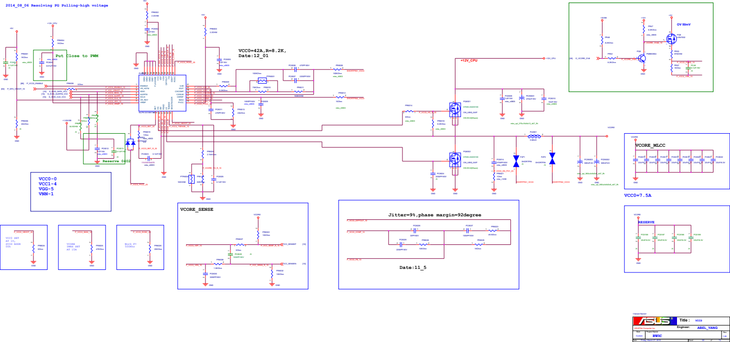
Size	Project Name	Rev
Custom	BWIC	1.00

Date: Friday, March 27, 2015 Sheet 63 of 74

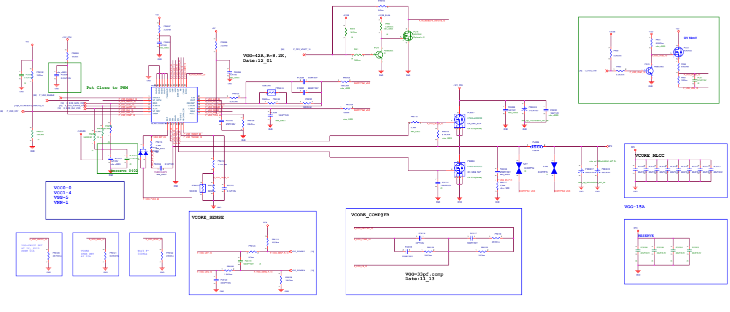


<Variant Name>

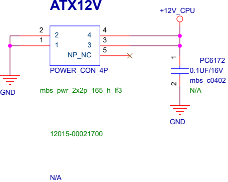
ASUSTek Computer Inc.	Title : 1.24		
	Engineer: ABEL_YANG		
Size: Custom	Project Name: BWIC		Rev: 1.00
Date: Friday, March 27, 2015	Sheet 64	of 74	



2014_08_06 Resolving PG Pulling-high voltage
Put Close to PWM
VCC0=42A,R=8.2K,
Date:12_01
+12V_CPU
OV 50mV
VCORE_MLCC
VCC0=7.5A
RESERVE
Reserve 0402
VCC0-0
VCC1-4
VGG-5
VNN-1
VCORE_SENSE
Jitter=9%,phase margin=92degree
Date:11_5
Title : VCC0
Engineer: ABEL_YANG
BWIC

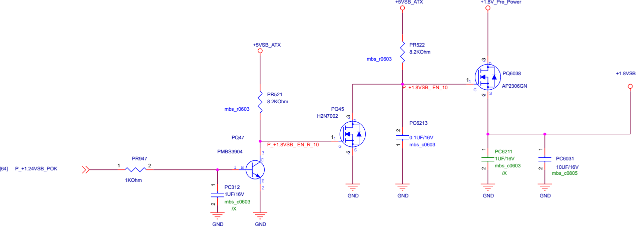


ASUSTek Computer Inc.	Title : VGG		
	Engineer: ABEL_YANG		
Size: Custom	Project Name: BWIC		Rev: 1.00
Date: Friday, March 27, 2015	Sheet: 60	of: 74	



<Variant Name>

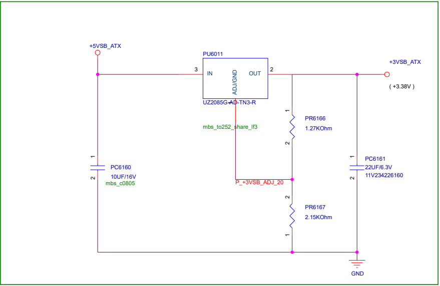
ASUSTek Computer Inc.	Title : CONNECTOR		
	Engineer: JASON		
Size: Custom	Project Name: BAYTRAIL		Rev: 1.00
Date: Friday, March 27, 2015	Sheet 66 of 74		



<Variant Name>

ASUS	**Title :** 1.8	
ASUSTek Computer Inc.	**Engineer:** ABEL_YANG	
Size: Custom	Project Name: **BWIC**	Rev: 1.00
Date: Friday, March 27, 2015	Sheet 65 of 74	

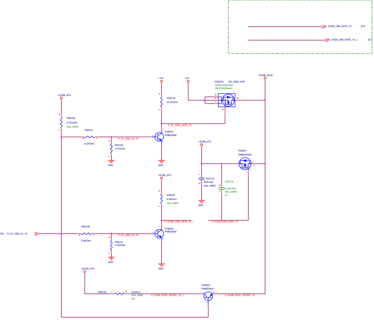
+5VSB_ATX ====>+3VSB_ATX



0.33A

<Variant Name>

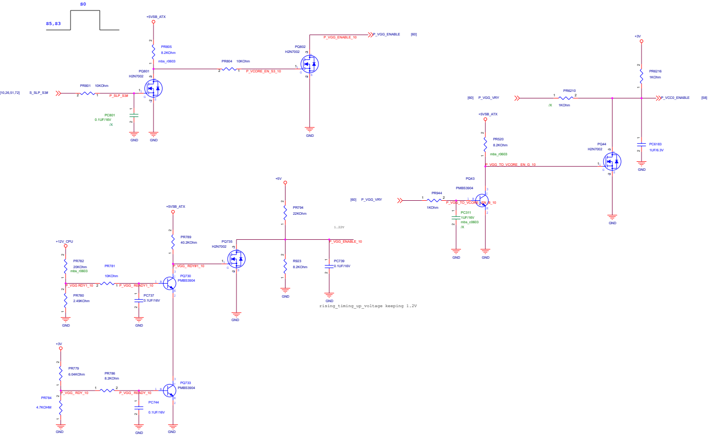
ASUSTek Computer Inc.	Title : +3VSB	
	Engineer: JASON	
Size: Custom	Project Name: BAYTRAIL	Rev: 1.00
Date: Friday, March 27, 2015	Sheet 67 of 74	



<Variant Name>

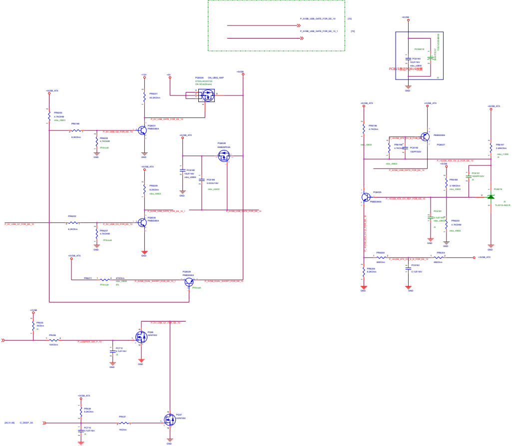
ASUSTEK COMPUTER INC	Title :	+5VSB_DUAL
	Engineer:	Herry Fan
Size: A2	Project Name	Rev: 0.08C
Date: Friday, March 27, 2015	Sheet 69 of 74	

POWER SEQUENCE



<Variant Name>

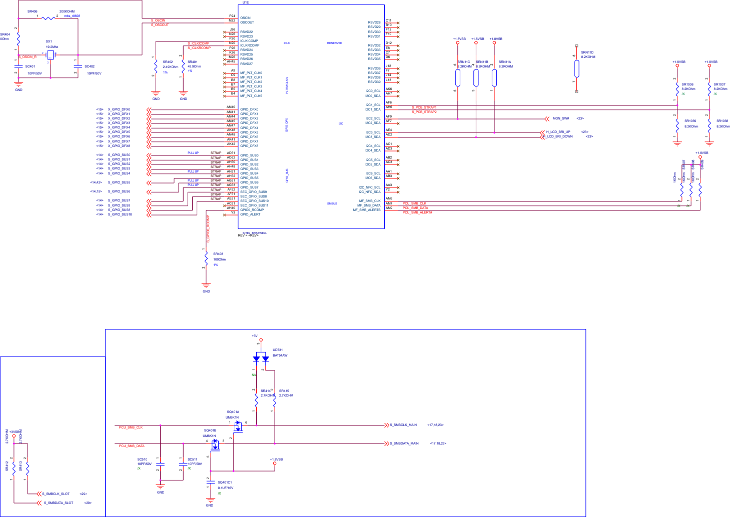
ASUSTek Computer Inc.	Title : sequence	
	Engineer: ABEL_YANG	
Size: Custom	Project Name: BWIC	Rev: 1.00
Date: Friday, March 27, 2015	Sheet 68 of 74	



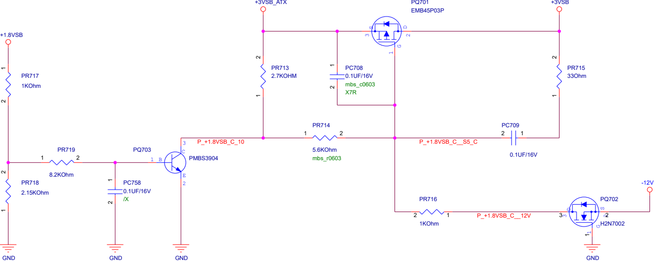
USBPWR_SW# GPIO select:
1. could be GPI & GPO both
2. default GPI (no internal pull-down/pull-high resistor)
3. +3VSB_ATX power plane, 3V tolerance
4. High level to force +5VSB_DUAL switch to +5V
5. Low level to let +5VSB_DUAL switch to +5VSB_ATX under S3/S4/S5
6. default need High level

<Variant Name>

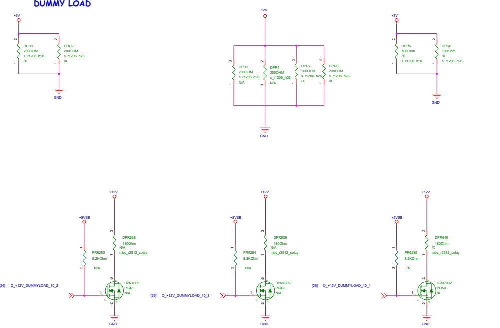
ASUSTEK COMPUTER INC	Title :	+5VSB_DUAL
	Engineer:	Herry Fan
Size: A2	Project Name	Rev: 0.08C
Date: Friday, March 27, 2019	Sheet 70	of 76



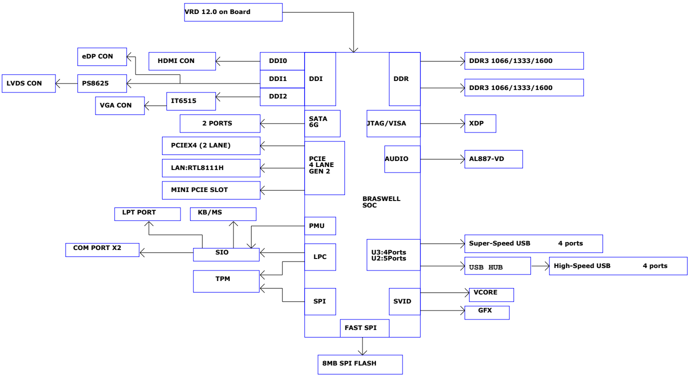
U1E
SR406
200KOHM
mbs_r0603
SR404
0Ohm
SX1
19.2MHz
S_OSCIN_R
SC401
10PF/50V
SC402
10PF/50V
GND
S_OSCIN
S_OSCOUT
OSCIN
OSCOUT
S_ICLKICOMP
S_ICLKRCOMP
SR402
2.49KOhm
1%
SR401
49.9Ohm
1%
ICLKICOMP
ICLKRCOMP
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
MF_PLT_CLK0
MF_PLT_CLK1
MF_PLT_CLK2
MF_PLT_CLK3
MF_PLT_CLK4
MF_PLT_CLK5
ICLK
RESERVED
PLTFM CLK's
X_GPIO_DFX0
X_GPIO_DFX1
X_GPIO_DFX2
X_GPIO_DFX3
X_GPIO_DFX4
X_GPIO_DFX5
X_GPIO_DFX6
X_GPIO_DFX7
X_GPIO_DFX8
GPIO_DFX
S_GPIO_SUS0
S_GPIO_SUS1
S_GPIO_SUS2
S_GPIO_SUS3
S_GPIO_SUS4
S_GPIO_SUS5
S_GPIO_SUS6
S_GPIO_SUS7
S_GPIO_SUS8
S_GPIO_SUS9
S_GPIO_SUS10
PULL UP
STRAP
SEC_GPIO_SUS8
SEC_GPIO_SUS9
SEC_GPIO_SUS10
SEC_GPIO_SUS11
GPIO_RCOMP
GPIO_ALERT
GPIO_SUS
S_GPIO_RCOMP
SR403
100Ohm
1%
INTEL_BRASWELL
REV = <REV>
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
RSVD39
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C4_SCL
I2C4_SDA
I2C5_SCL
I2C5_SDA
I2C6_SCL
I2C6_SDA
I2C_NFC_SCL
I2C_NFC_SDA
I2C
SMBUS
MF_SMB_CLK
MF_SMB_DATA
MF_SMB_ALERTB
S_PCB_STRAP1
S_PCB_STRAP2
MON_SW#
H_LCD_BRI_UP
H_LCD_BRI_DOWN
PCU_SMB_CLK
PCU_SMB_DATA
PCU_SMB_ALERT#
+1.8VSB
SRN11C
SRN11B
SRN11A
SRN11D
8.2KOHM
SR1036
SR1037
SR1038
SR1039
8.2KOhm
SR1107
SR1108
SR1109
1KOhm
+3V
UD731
BAT54AW
SR414
SR415
2.7KOHM
SQ401A
SQ401B
UM6K1N
S_SMBCLK_MAIN
S_SMBDATA_MAIN
<17,18,23>
SC510
SC511
10PF/50V
SQ401C1
0.1UF/16V
+3VSB
SR412
SR413
2.7KOHM
S_SMBCLK_SLOT
S_SMBDATA_SLOT
<29>



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, March 27, 2015	Sheet 74	of 74

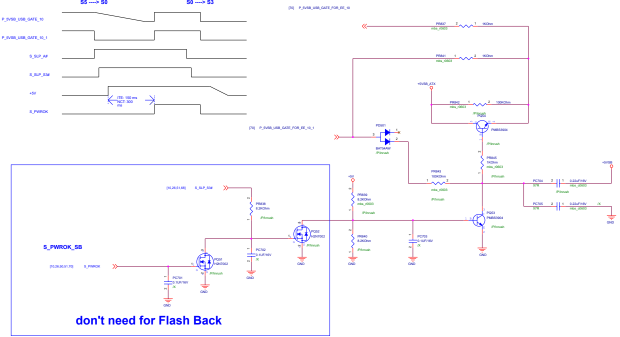


ASUSTek Computer Inc.	Title :	+5VSB_DUAL/+1.1VSB	
	Engineer:		
Size: B	Project Name: FM2 PLUS		Rev: 1.00
Date: Friday, March 27, 2015	Sheet 71 of 74		



<Variant Name>

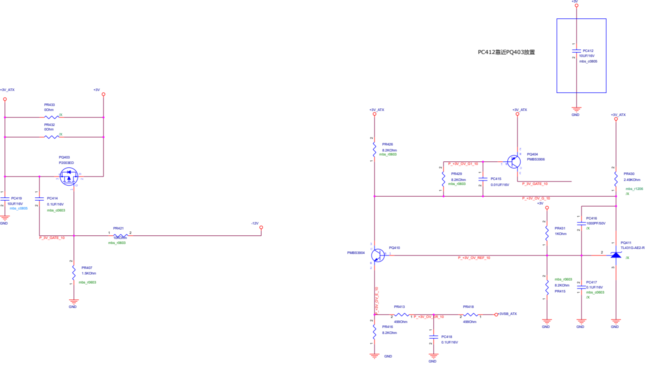
	Title :	BLOCK DIAGRAM
<OrgName>	Engineer:	key_cai
Size: A3	Project Name: Standard Circuit	Rev: 0.01A
Date: Friday, March 27, 2015	Sheet 75	of 75



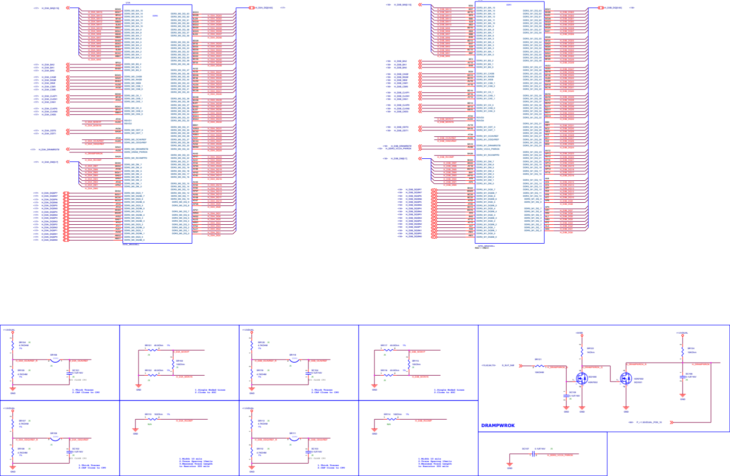
Inrush Circuit for USB Port default have Power or Flash Back Function

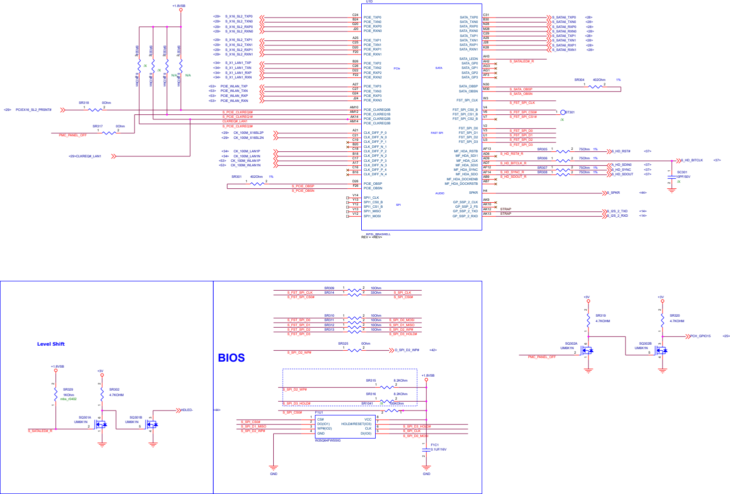
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB Inrush	
	Engineer: Kell_Huang	
Size A3	Project Name Chipset USB Demo Circuit	Rev 0.0
Date: Friday, March 27, 2015	Sheet 72 of 74	



ASUSTek Computer Inc.	**Title :** +5VSB_DUAL/+1.1VSB	
	Engineer:	
Size A2	Project Name **FM2 PLUS**	Rev 1.00
Date: Friday, March 27, 2015	Sheet 73 of 74	


DRAMPWROK
INTEL_BRASWELL
1.Thick Traces
2.CAP Close to CPU
1.Single Ended Lines
2.Close to SOC



U1D
+1.8VSB
SR318 0Ohm
PCIEX16_SL2_PRSNT#
SR317 0Ohm
PMC_PANEL_OFF
<29>CLKREQ#_LAN1
S_X16_SL2_TXP0
S_X16_SL2_TXN0
S_X16_SL2_RXP0
S_X16_SL2_RXN0
S_X16_SL2_TXP1
S_X16_SL2_TXN1
S_X16_SL2_RXP1
S_X16_SL2_RXN1
S_X1_LAN1_TXP
S_X1_LAN1_TXN
S_X1_LAN1_RXP
S_X1_LAN1_RXN
PCIE_WLAN_TXP
PCIE_WLAN_TXN
PCIE_WLAN_RXP
PCIE_WLAN_RXN
S_PCIE_CLKREQ0#
S_PCIE_CLKREQ1#
CLKREQ#_LAN1
S_PCIE_CLKREQ3#
CK_100M_X16SL2P
CK_100M_X16SL2N
CK_100M_LAN1P
CK_100M_LAN1N
CK_100M_WLAN1P
CK_100M_WLAN1N
SR301 402Ohm 1%
S_PCIE_OBSP
S_PCIE_OBSN
PCIe
SATA
FAST SPI
SPI
AUDIO
SATA_TXP0
SATA_TXN0
SATA_RXP0
SATA_RXN0
SATA_TXP1
SATA_TXN1
SATA_RXP1
SATA_RXN1
SATA_LEDN
SATA_GP0
SATA_GP1
SATA_GP2
SATA_GP3
SATA_OBSP
SATA_OBSN
FST_SPI_CLK
FST_SPI_CS0_B
FST_SPI_CS1_B
FST_SPI_CS2_B
FST_SPI_D0
FST_SPI_D1
FST_SPI_D2
FST_SPI_D3
MF_HDA_RSTB
MF_HDA_SDI1
MF_HDA_CLK
MF_HDA_SDI0
MF_HDA_SYNC
MF_HDA_SDO
MF_HDA_DOCKENB
MF_HDA_DOCKRSTB
SPKR
GP_SSP_2_CLK
GP_SSP_2_FS
GP_SSP_2_TXD
GP_SSP_2_RXD
S_SATA6_TXP0
S_SATA6_TXN0
S_SATA6_RXP0
S_SATA6_RXN0
S_SATA6_TXP1
S_SATA6_TXN1
S_SATA6_RXP1
S_SATA6_RXN1
S_SATALED#_R
SR304 402Ohm 1%
S_SATA_OBSP
S_SATA_OBSN
S_FST_SPI_CLK
S_FST_SPI_CS0#
S_FST_SPI_CS1#
ST301
S_FST_SPI_D0
S_FST_SPI_D1
S_FST_SPI_D2
S_FST_SPI_D3
SR305 75Ohm 1%
S_HD_RST#
S_HD_RST#_R
SR306 75Ohm 1%
S_HD_BITCLK
S_HD_BITCLK_R
S_HD_SDIN0
SR307 75Ohm 1%
S_HD_SYNC
SR308 75Ohm 1%
S_HD_SDOUT
S_HD_SYNC_R
S_HD_SDOUT_R
SC301 10PF/50V
S_SPKR
STRAP
S_I2S_2_TXD
S_I2S_2_RXD
INTEL_BRASWELL
REV = <REV>
Level Shift
+1.8VSB
SR329 1KOhm
mbs_r0402
+3V
SR302 4.7KOHM
SQ301A UM6K1N
SQ301B UM6K1N
HDLED-
S_SATALED#_R
BIOS
SR309 10Ohm
SR314 33Ohm
S_FST_SPI_CLK
S_FST_SPI_CS0#
S_SPI_CLK
S_SPI_CS0#
SR310 10Ohm
SR311 10Ohm
SR312 10Ohm
SR313 10Ohm
S_SPI_D0_MOSI
S_SPI_D1_MISO
S_SPI_D2_WP#
S_SPI_D3_HOLD#
SR325 0Ohm
O_SPI_D2_WP#
SR315 8.2KOhm
SR316 8.2KOhm
SR1041 100KOhm
+1.8VSB
F1U1
CS#
DO(IO1)
WP#(IO2)
GND
VCC
HOLD#/RESET(IO3)
CLK
DI(IO0)
W25Q64FWSSIG
F1C1 0.1UF/16V
GND
+3V
SR319 4.7KOHM
SQ302A UM6K1N
PMC_PANEL_OFF
+3V
SR320 4.7KOHM
SQ302B UM6K1N
PCH_GPIO15