MS-7B58

ATX

Ver: 10

Intel -Kabylake-R plamform Z370

CPU:

CFL-S

System Chipset:

Z370

Onboard Chip:

HD Audio Codec:ALC1220
LAN:Killer E2400 colay E2500
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 2*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *2*
*REAR USB2.0 *3*
REAR USB TYPE A+C

MICRO-STAR INT'L CO.,LTD

MS-7B58

Size: Custom | Document Description: Cover Sheet | Rev: 10

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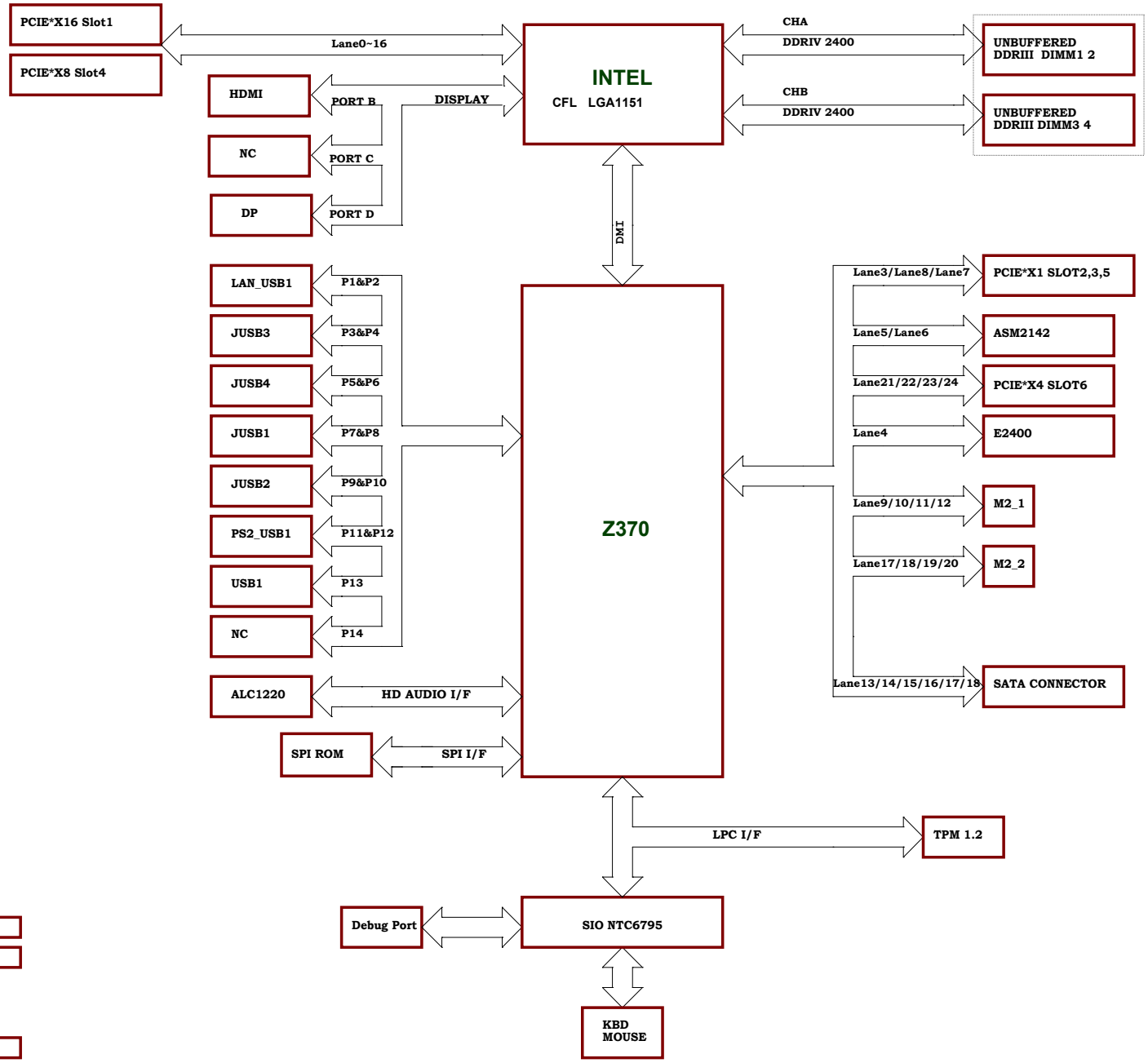
MS-7A78 Block Diagram



Slot Sequence:

- M.2
- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X8
- PCIE X1 / M.2
- PCIE X4

MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: Block Diagram
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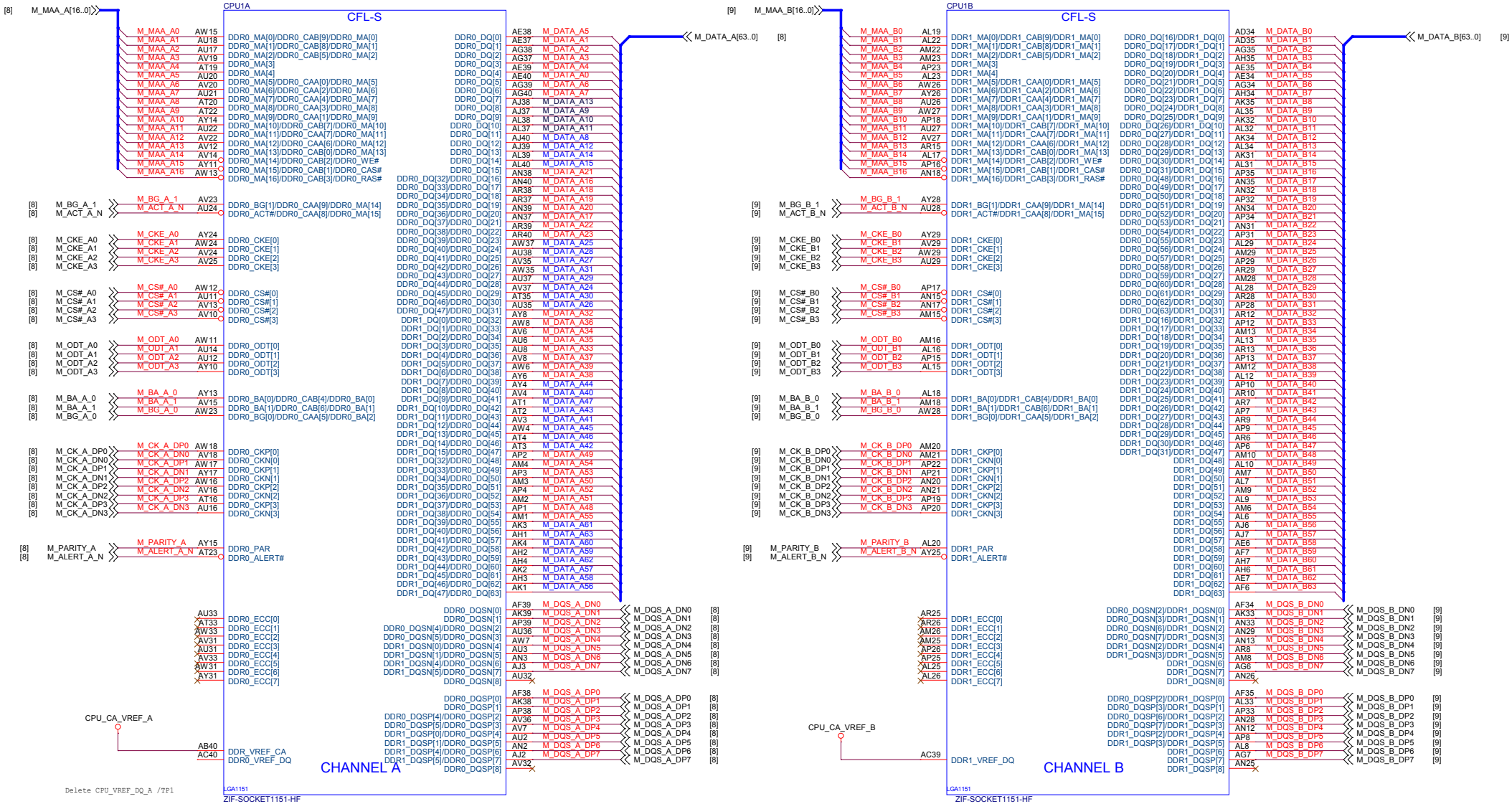
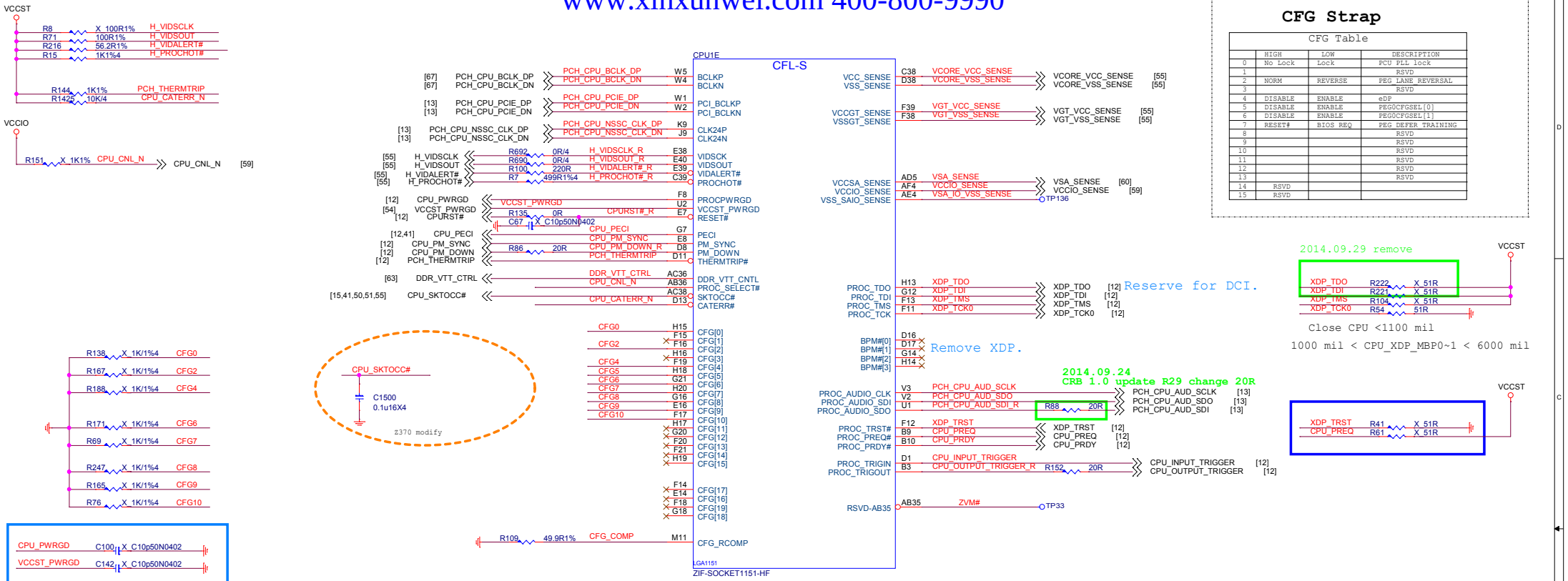


MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: CPU-Memory
Rev: 10	
Date: Monday, July 24, 2017	Sheet 3 of 72



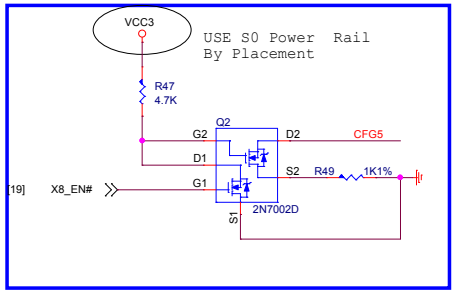
CFG Strap

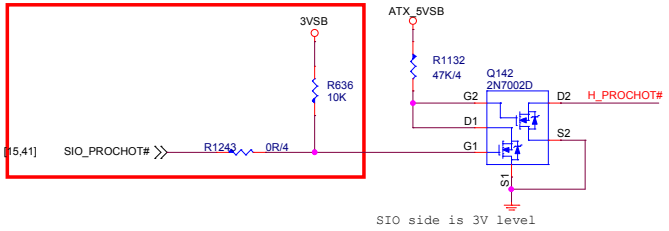
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

X8 Ctrl

ENABLE# X8	SLOT1	SLOT4
0	X8	X8
1	X16	X0





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1			RSVD
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3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU-Control/MISC/CFG/Audio	10

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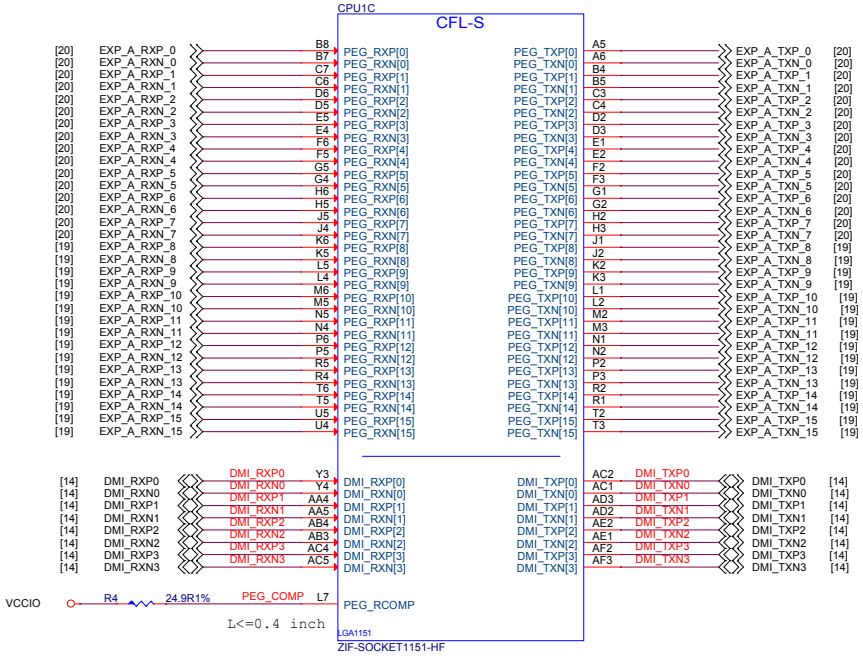
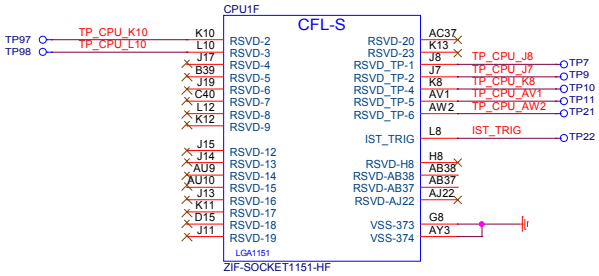
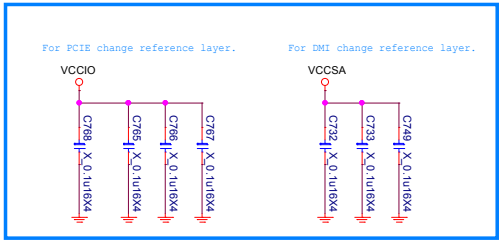
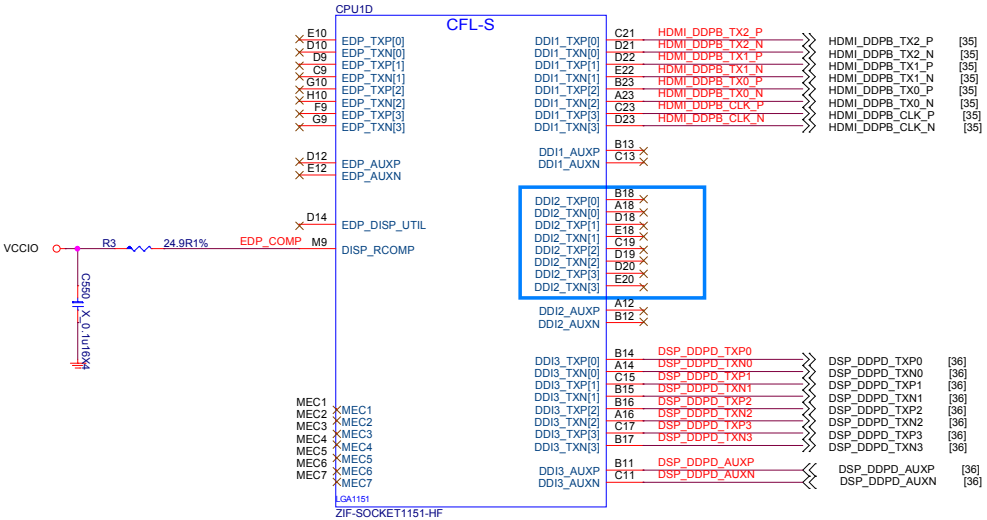




TP7, TP9, TP10, TP11, TP21, TP22, TP97, TP98
Reservd for CPU XDP debug pin

Z370 Modify;





MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: CPU-PEG/Display
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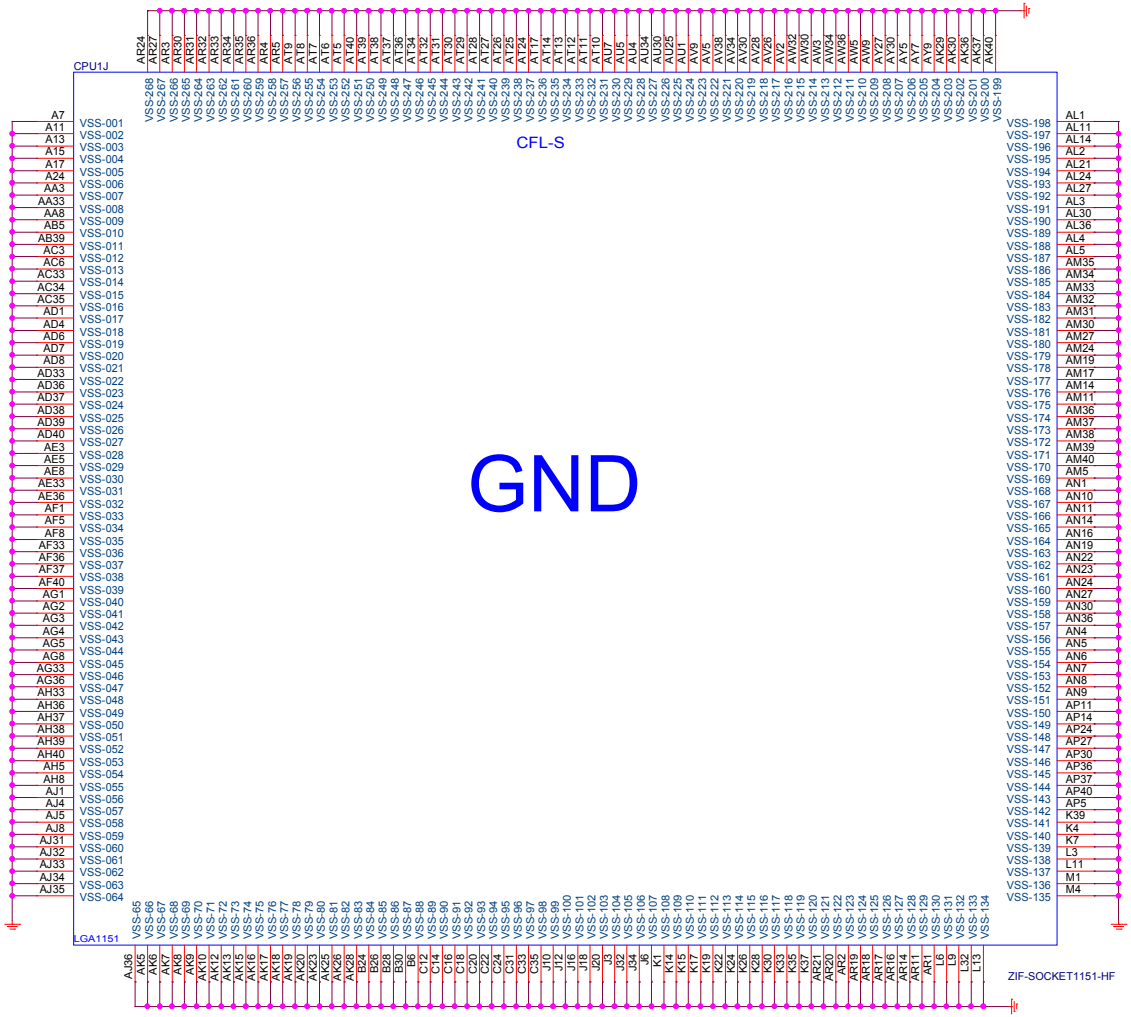
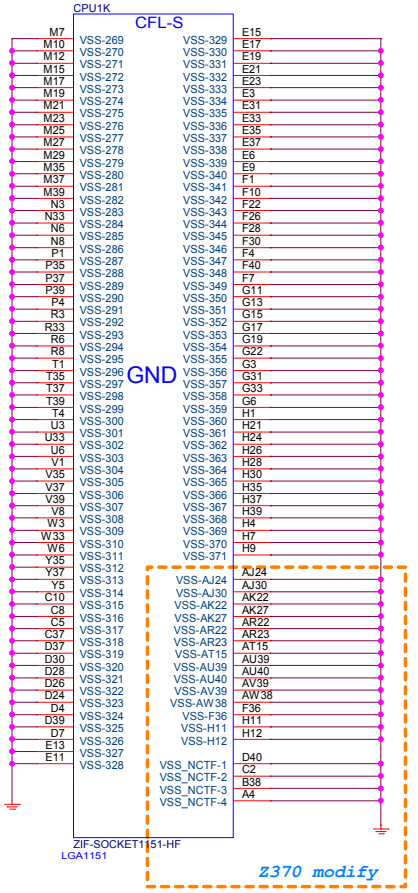
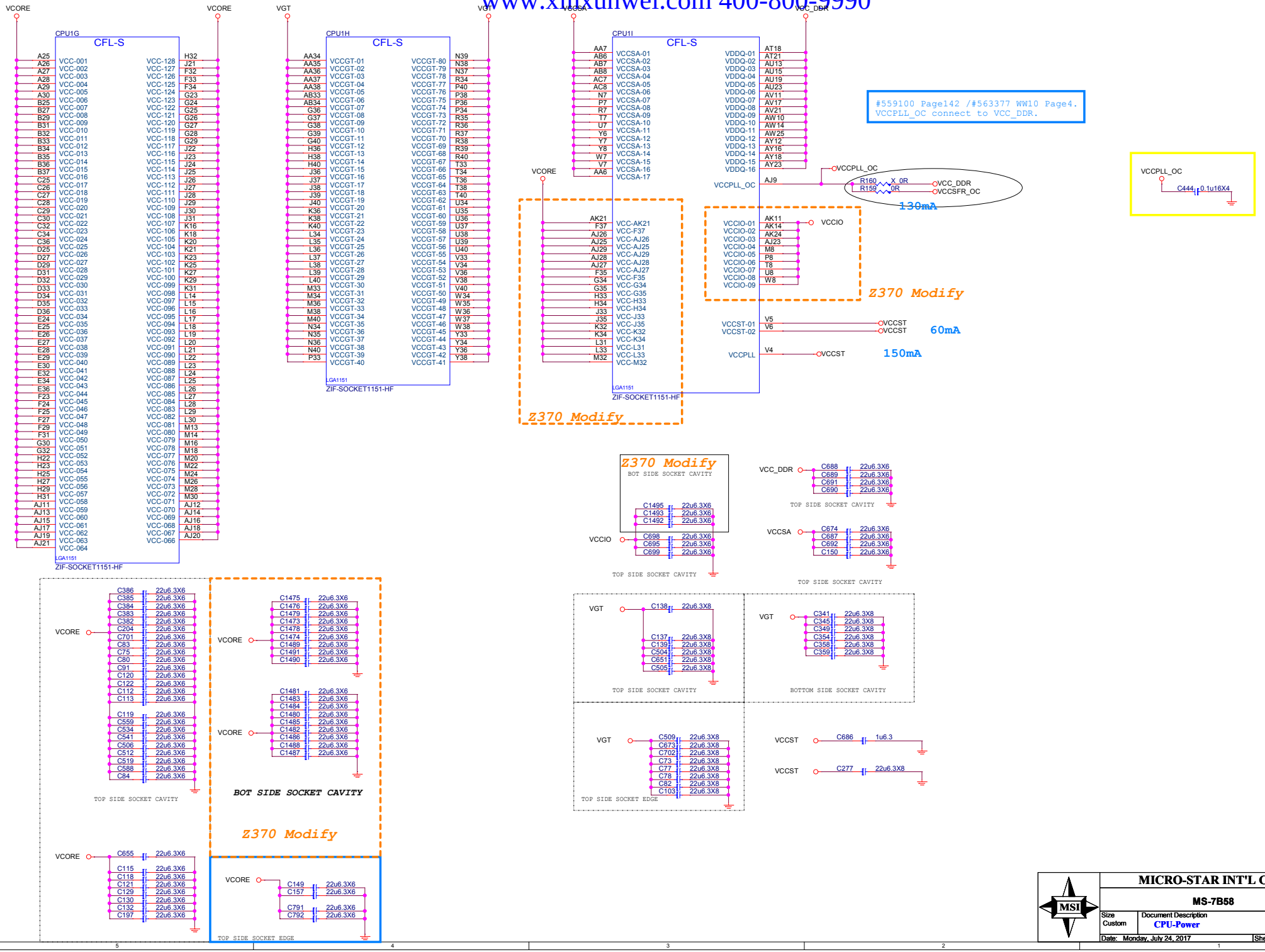
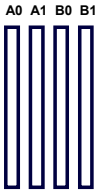




MICRO-STAR INT'L CO.,LTD		
MS-7B58		
Size: Custom	Document Description: CPU-GND	Rev: 10
Date: Monday, July 24, 2017	Sheet 6 of 72	



MICRO-STAR INT'L CO.,LTD			
MS-7B58			
Size: Custom	Document Description: CPU-Power		Rev: 10
Date: Monday, July 24, 2017		Sheet 7 of 72	



DIMMA1A

DDRIV-288P_BLACK-RH-21

DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DIMMA2A

DDRIV-288P_BLACK-RH-21

DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7B58
Size	Custom
Document Description	DDR4 SLOT-DIMM1/DIMM2
Rev	10
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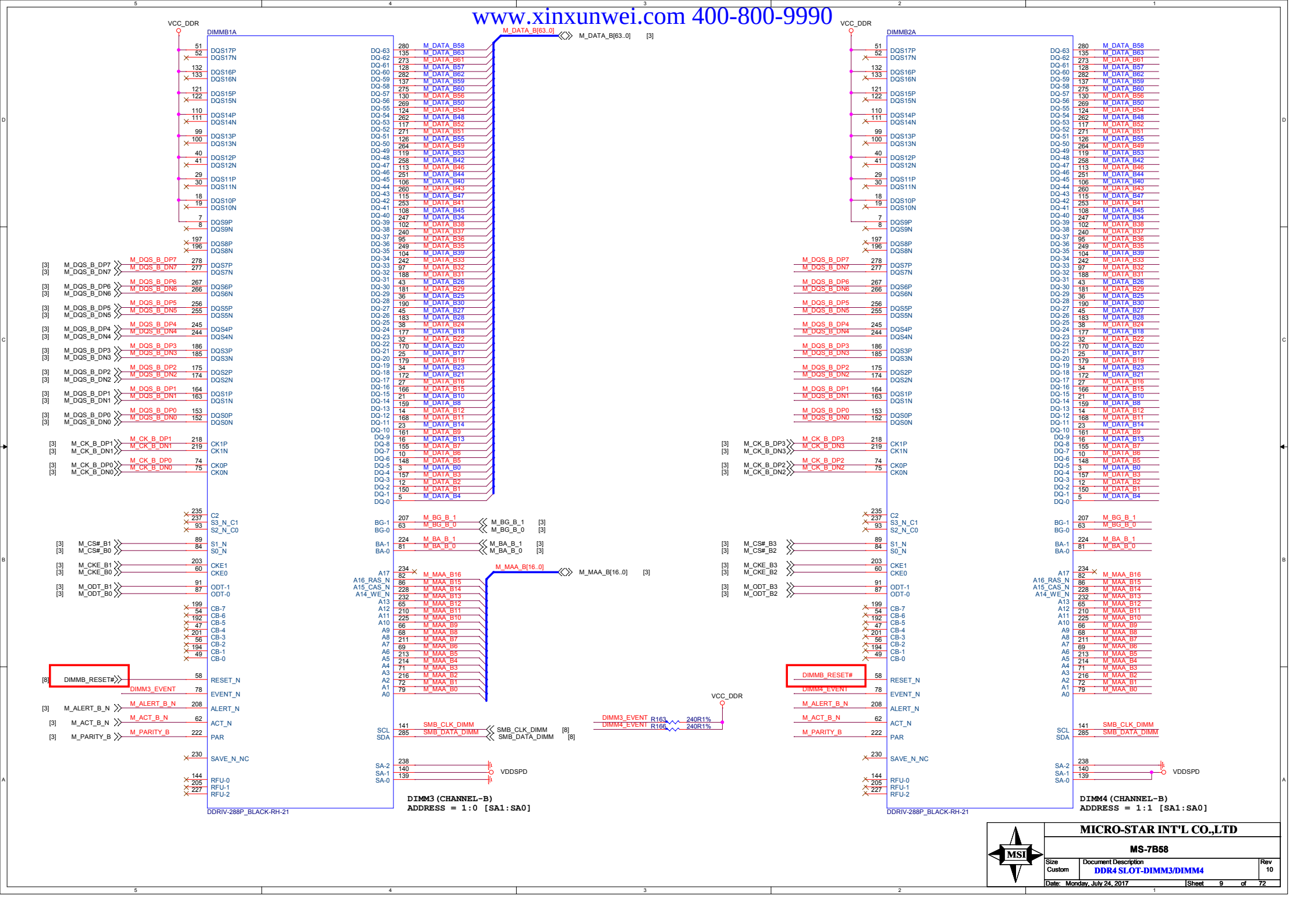
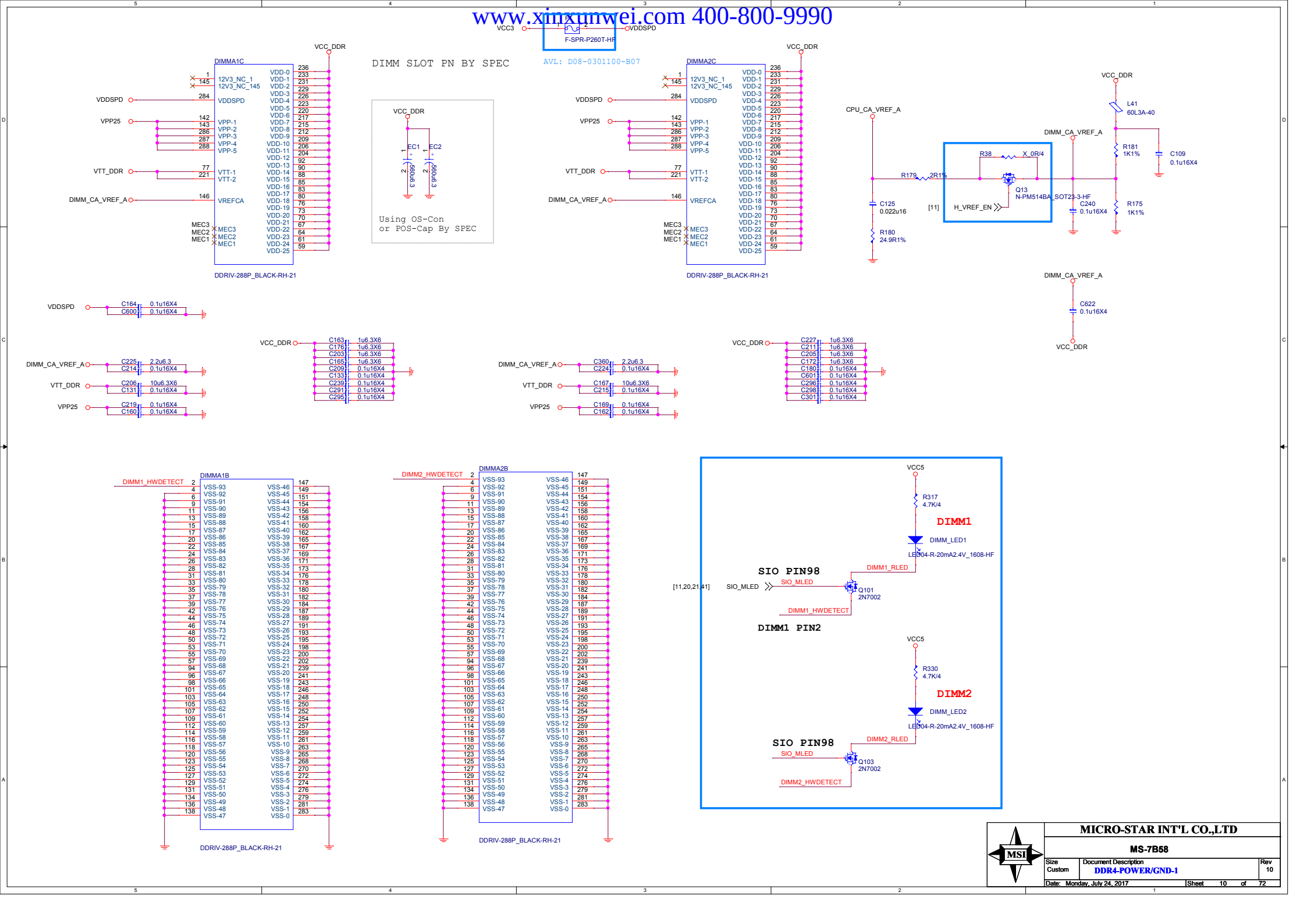
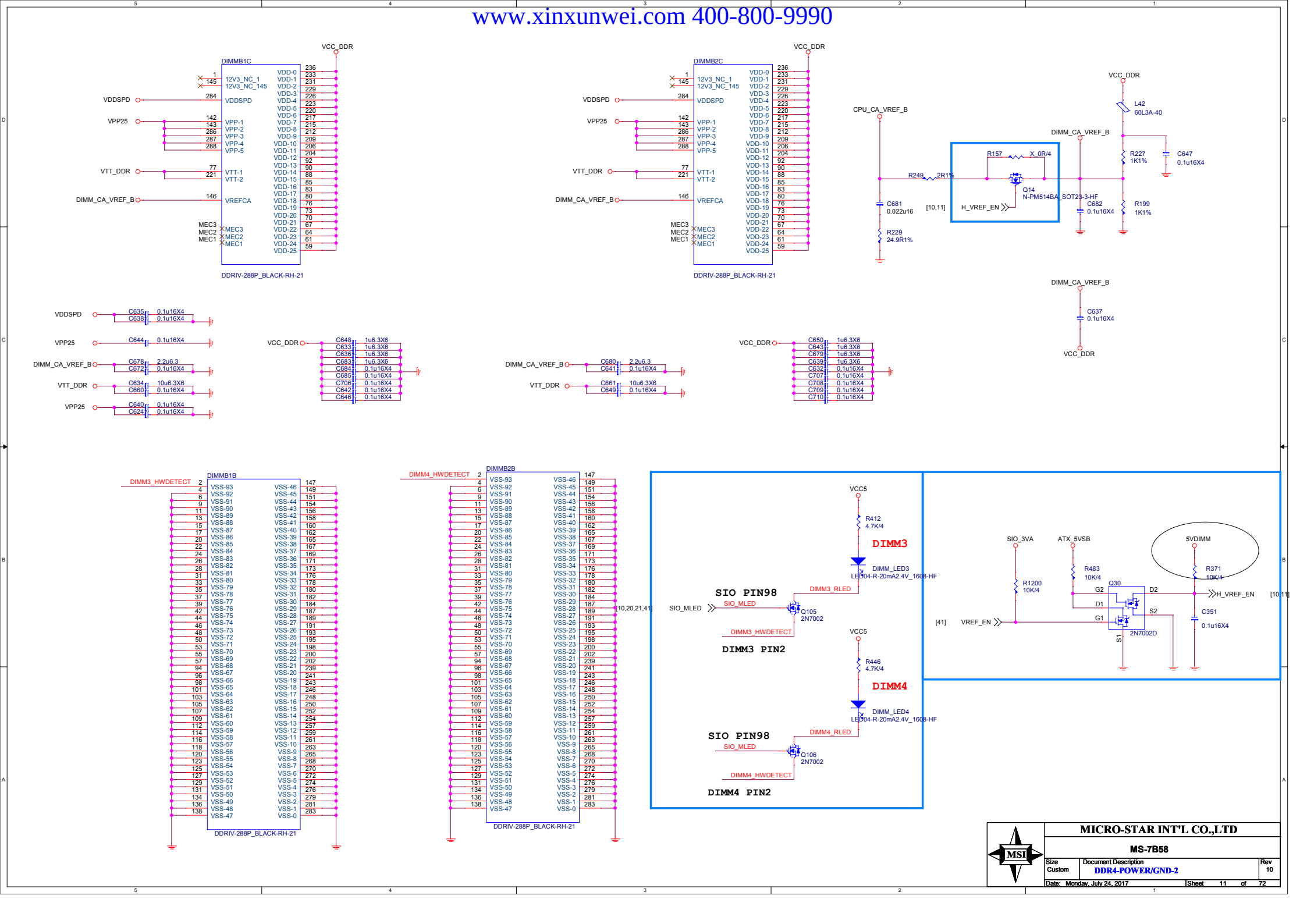


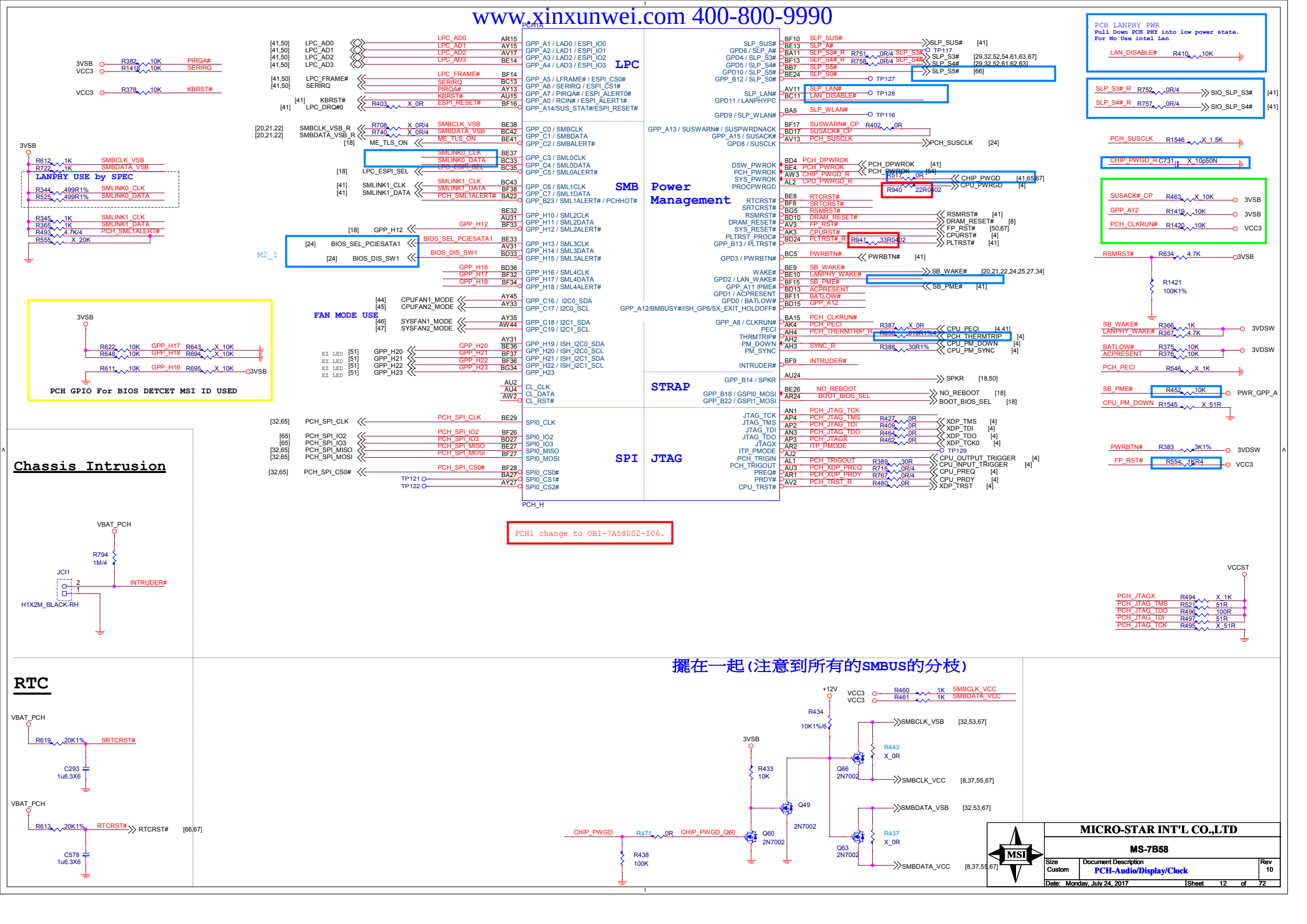
MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4
Rev: 10	
Date: Monday, July 24, 2017	Sheet 9 of 72



MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: DDR4-POWER/GND-1
Rev: 10	
Date: Monday, July 24, 2017	Sheet 10 of 72



MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: DDR4-POWER/GND-2
Rev: 10	
Date: Monday, July 24, 2017	Sheet 11 of 72



RTC Block

Close to PCH

C289 12p50N6 RTCX2
Y2
R481 10M/6 <1 inch
C292 12p50N6 RTCX1
32.768KHZ12.5p_D-RH-10

AVL: D04-0306001-C11/D04-0306101-T02

CRB
SRCCLKREQ pull up power change to VCC3.

VCC3
R290 10K LAN_CLKREQ#4
R304 10K M2_CLKREQ#9
R420 10K M2_CLKREQ#10
R311 10K ASM1142_CLKREQ#5

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
R445 1MR1%4
R212 0R
R218 0R
24M_OUT
24M_IN
Y1
24MHZ20p_S-HF
C285 C22p50N/4
C284 C22p50N/4

PCH1E

[41] CLK_SIO_PCI R559 22R CLK_PCH_LPC0 BE15
[50] TPM_CLK R468 22R CLK_PCH_LPC1 AY17
BC17
GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
GPP_A10 / CLKOUT_LPC1
GPP_A16 / CLKOUT_48
LPC

RTCX1 BF7
RTCX2 BG7
RTC

XTAL_24M_PCH_IN E1
XTAL_24M_PCH_OUT A5
C551 0.1u16X4
PCH_CLK5_1P0 R346 2.7K1% XCLK_BIASREF F1
XCLK_BIASREF < 500 mil
24MHZ

TP123 CLKREQ#0 BE22
TP124 CLKREQ#1 BA24
TP125 CLKREQ#2 BA19
TP126 CLKREQ#3 BE23
LAN_CLKREQ#4 BD22
ASM1142_CLKREQ#5 BF23
Z370 modify
LAN_CLKREQ#4 [34]
TP132 CLKREQ#6 AR29
TP133 CLKREQ#7 AU27
TP134 CLKREQ#8 BG30
M2_CLKREQ#9 BF30
M2_CLKREQ#10 BD29
M2_CLKREQ#9 [24]
M2_CLKREQ#10 [25]
GPP_B5 / SRCCLKREQ0#
GPP_B6 / SRCCLKREQ1#
GPP_B7 / SRCCLKREQ2#
GPP_B8 / SRCCLKREQ3#
GPP_B9 / SRCCLKREQ4#
GPP_B10 / SRCCLKREQ5#
GPP_H0 / SRCCLKREQ6#
GPP_H1 / SRCCLKREQ7#
GPP_H2 / SRCCLKREQ8#
GPP_H3 / SRCCLKREQ9#
GPP_H4 / SRCCLKREQ10#
CLK_REQ
BE31 GPP_H5 / SRCCLKREQ11#
AY29 GPP_H6 / SRCCLKREQ12#
AV29 GPP_H7 / SRCCLKREQ13#
BD31 GPP_H8 / SRCCLKREQ14#
BF31 GPP_H9 / SRCCLKREQ15#
PCH_H

CLKOUT_CPUBCLK_P H1 PCH_IDT_BCLK_DP PCH_IDT_BCLK_DP [67]
CLKOUT_CPUBCLK_N H2 PCH_IDT_BCLK_DN PCH_IDT_BCLK_DN [67]
CLKOUT_CPUNSSC_P G2 PCH_CPU_NSSC_CLK_DP PCH_CPU_NSSC_CLK_DP [4]
CLKOUT_CPUNSSC_N G1 PCH_CPU_NSSC_CLK_DN PCH_CPU_NSSC_CLK_DN [4]
CLKOUT_CPUPCIBCLK_P J2 PCH_CPU_PCIE_DP PCH_CPU_PCIE_DP [4]
CLKOUT_CPUPCIBCLK_N J3 PCH_CPU_PCIE_DN PCH_CPU_PCIE_DN [4]
CLKOUT_ITPXDP_P L3
CLKOUT_ITPXDP_N L2

CLKOUT_PCIE_P0 P7 CLK_PE2_DP CLK_PE2_DP [22] PCI_E2
CLKOUT_PCIE_N0 P5 CLK_PE2_DN CLK_PE2_DN [22]
CLKOUT_PCIE_P1 M5 CLK_PE6_DP CLK_PE6_DP [21] PCI_E6
CLKOUT_PCIE_N1 M7 CLK_PE6_DN CLK_PE6_DN [21]
CLKOUT_PCIE_P2 G7 CLK_PE4_DP CLK_PE4_DP [21] PCI_E4
CLKOUT_PCIE_N2 H7 CLK_PE4_DN CLK_PE4_DN [21]
CLKOUT_PCIE_P3 K5 CLK_PE1_DP CLK_PE1_DP [20] PCI_E1
CLKOUT_PCIE_N3 K7 CLK_PE1_DN CLK_PE1_DN [20]
CLKOUT_PCIE_P4 E4 CLK_LAN_DP CLK_LAN_DP [34] LAN
CLKOUT_PCIE_N4 E3 CLK_LAN_DN CLK_LAN_DN [34]
CLKOUT_PCIE_P5 C6 CLK_ASM1142_DP CLK_ASM1142_DP [27] ASMEDIA
CLKOUT_PCIE_N5 C5 CLK_ASM1142_DN CLK_ASM1142_DN [27]
CLKOUT_PCIE_P6 T7 CLK_PE3_DP CLK_PE3_DP [22] PCI_E3
CLKOUT_PCIE_N6 T8 CLK_PE3_DN CLK_PE3_DN [22]
CLKOUT_PCIE_P7 V7 CLK_PE5_DP CLK_PE5_DP [22] PCI_E5
CLKOUT_PCIE_N7 V5 CLK_PE5_DN CLK_PE5_DN [22]
CLKOUT_PCIE_P8 Y11
CLKOUT_PCIE_N8 Y10
Delete U2
CLKOUT_PCIE_P9 M1 CLK_M2_1_DP CLK_M2_1_DP [24] M.2
CLKOUT_PCIE_N9 M2 CLK_M2_1_DN CLK_M2_1_DN [24]
CLKOUT_PCIE_P10 P2 CLK_M2_2_DP CLK_M2_2_DP [25]
CLKOUT_PCIE_N10 P3 CLK_M2_2_DN CLK_M2_2_DN [25]
CLKOUT_PCIE_P11 T3
CLKOUT_PCIE_N11 T2
CLKOUT_PCIE_P12 U2
CLKOUT_PCIE_N12 U1
CLKOUT_PCIE_P13 AA5
CLKOUT_PCIE_N13 Y7
CLKOUT_PCIE_P14 R2
CLKOUT_PCIE_N14 R3
CLKOUT_PCIE_P15 T11
CLKOUT_PCIE_N15 T13

AZ_BITCLK
C774 X_12p50N6

PCH1D

[38] AZ_SDIN0 AZ_SDIN0 BA2 HDA_SDI0
[18] AZ_SDOUT_R AZ_SDOUT_R BB1 HDA_SDI1
[38] AZ_SDOUT AZ_SDOUT R352 33R AZ_SDOUT_R BC3 HDA_SDO
[38] AZ_BITCLK AZ_BITCLK R349 33R AZ_BITCLK_LR BB3 HDA_BCLK
[38] AZ_RST# AZ_RST# R350 33R AZ_RST#_R BC1 HDA_RST#
[38] AZ_SYNC AZ_SYNC R351 33R AZ_SYNC_R BG6 HDA_SYNC

AUDIO

[4] PCH_CPU_AUD_SCLK R335 30R PCH_CPU_AUD_SCLK_R AM2 DISPA_BCLK
[4] PCH_CPU_AUD_SDO R325 30R PCH_CPU_AUD_SDO_R AM3 DISPA_SDO
[4] PCH_CPU_AUD_SDI PCH_CPU_AUD_SDI AN2 DISPA_SDI

AP36 GPP_D5 / I2S0_SFRM
AU43 GPP_D6 / I2S0_TXD
AV44 GPP_D7 / I2S0_RXD
AU42 GPP_D8 / I2S0_SCLK
AP42 GPP_D17 / DMIC_CLK1
AN43 GPP_D18 / DMIC_DATA1
AP38 GPP_D19 / DMIC_CLK0
AM43 GPP_D20 / DMIC_DATA0

PORT B
GPP_I5 / DDPB_CTRLCLK AW5 HDMI_DDPB_CTRLCLK HDMI_DDPB_CTRLCLK [35]
GPP_I6 / DDPB_CTRLDATA AV7 HDMI_DDPB_CTRLDATA HDMI_DDPB_CTRLDATA [35]
GPP_I0 / DDPB_HPD0 AP7 HDMI_DDPB_HPD HDMI_DDPB_HPD [35]

PORT C
GPP_I7 / DDPC_CTRLCLK AT5 HDMI_DDPC_CTRLCLK
GPP_I8 / DDPC_CTRLDATA BA6 HDMI_DDPC_CTRLDATA
GPP_I1 / DDPC_HPD1 AT8 HDMI_DDPC_HPD R732 10K

PORT D
GPP_I9 / DDPD_CTRLCLK AY1 DSP_DDPD_CTRLCLK DSP_DDPD_CTRLCLK [36]
GPP_I10 / DDPD_CTRLDATA AY2 DSP_DDPD_CTRLDATA DSP_DDPD_CTRLDATA [36]
GPP_I2 / DDPD_HPD2 AP8 DSP_DDPD_HPD DSP_DDPD_HPD [36]

eDP
GPP_F19 / eDP_VDDEN AC42
GPP_F20 / eDP_BKLTEN AE35
GPP_F21 / eDP_BKLTCTL AE36
GPP_I4 / EDP_HPD BA1 EDP_HPD R176 100K
GPP_I3 / DDPE_HPD3 AT7 DDPE_HPD3 R153 10K
PCH_H

VCC3
HDMI_DDPB_CTRLCLK R347 2.2K
HDMI_DDPB_CTRLDATA R348 2.2K
HDMI_DDPC_CTRLCLK R453 X_2.2K
HDMI_DDPC_CTRLDATA R454 X_2.2K
DSP_DDPD_CTRLCLK R741 2.2K/4
DSP_DDPD_CTRLDATA R759 2.2K/4

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Size: Custom
Document Description: PCH-USB/PCIE/DMI/SATA
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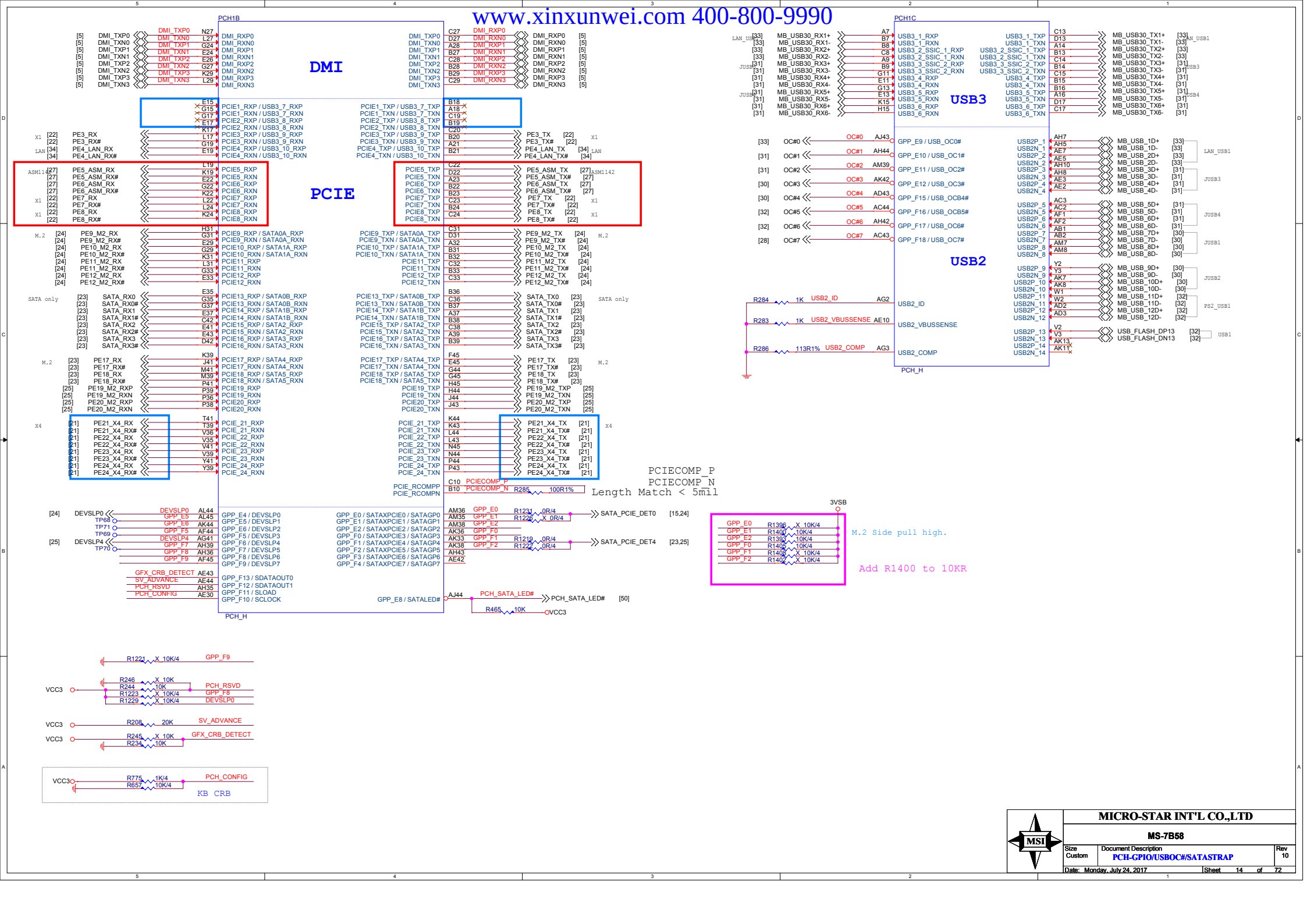
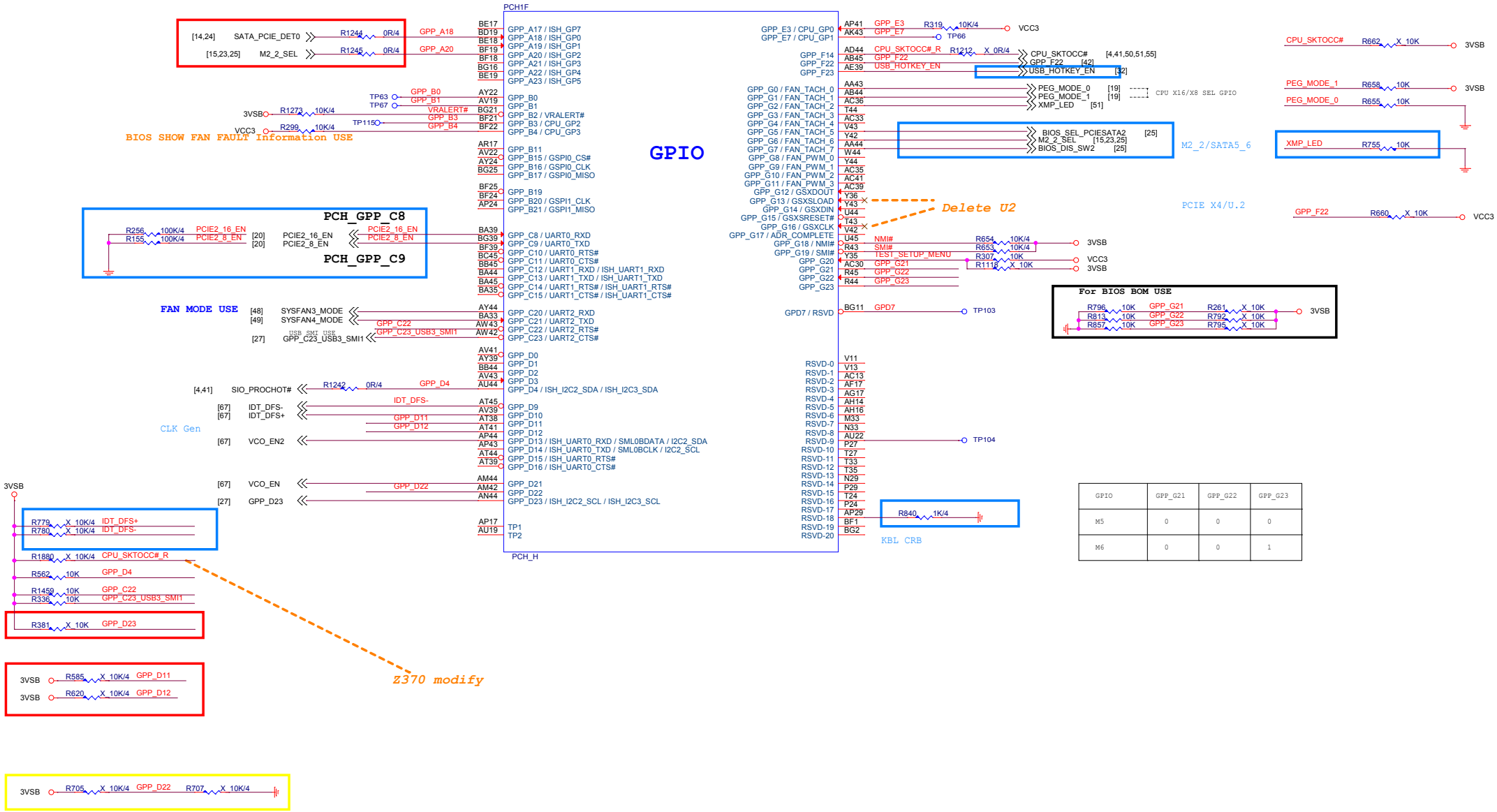


MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: PCH-GPIO/USBOC#/SATASTRAP
Rev: 10	
Date: Monday, July 24, 2017	Sheet 14 of 72



GPIO	GPP_G21	GPP_G22	GPP_G23
M5	0	0	0
M6	0	0	1

MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	PCH-LPC/SPI/SMBUS/MISC	10

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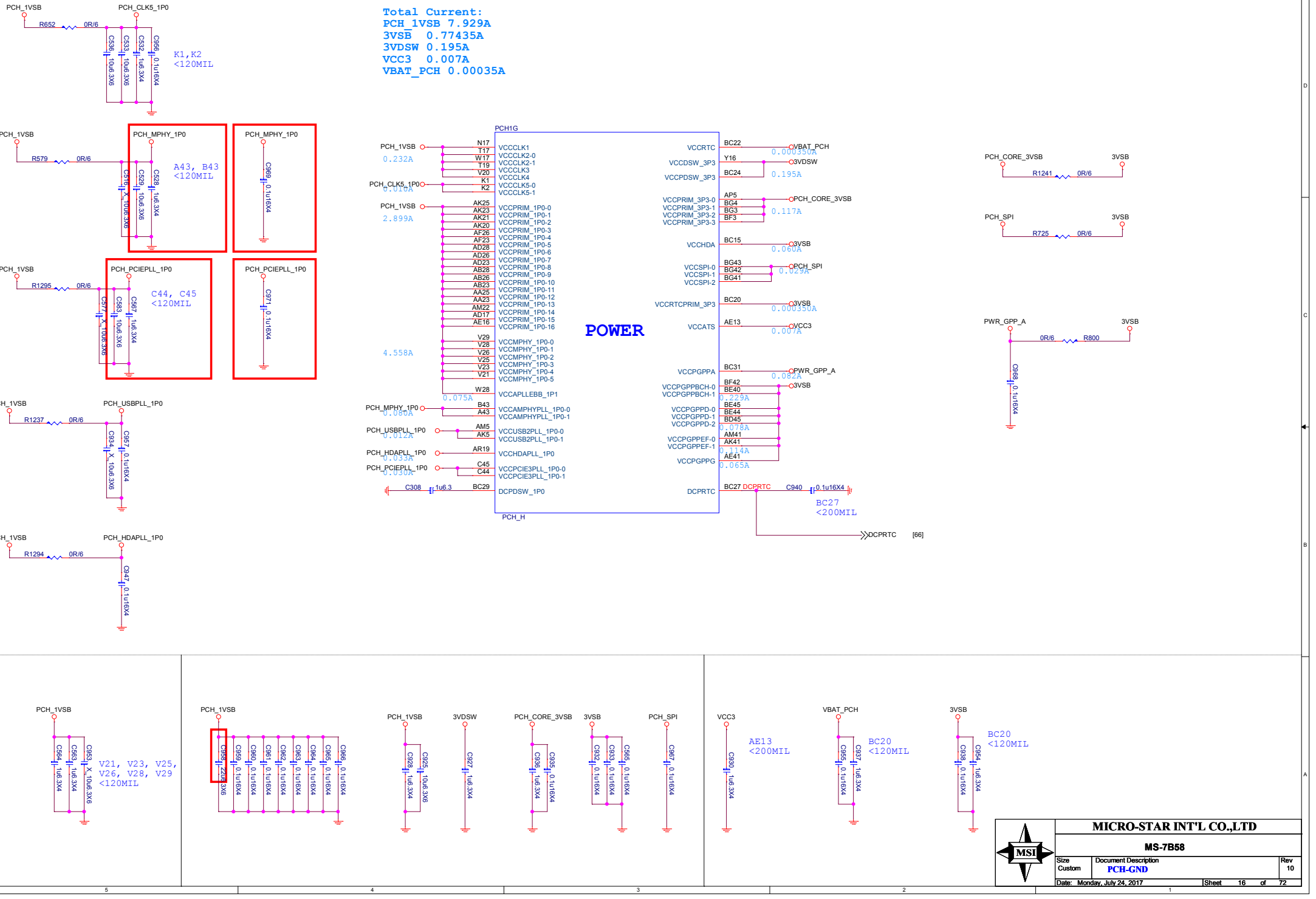
Total Current:
PCH_1VSB 7.929A
3VSB 0.77435A
3VDSW 0.195A
VCC3 0.007A
VBAT_PCH 0.00035A



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-GND	10

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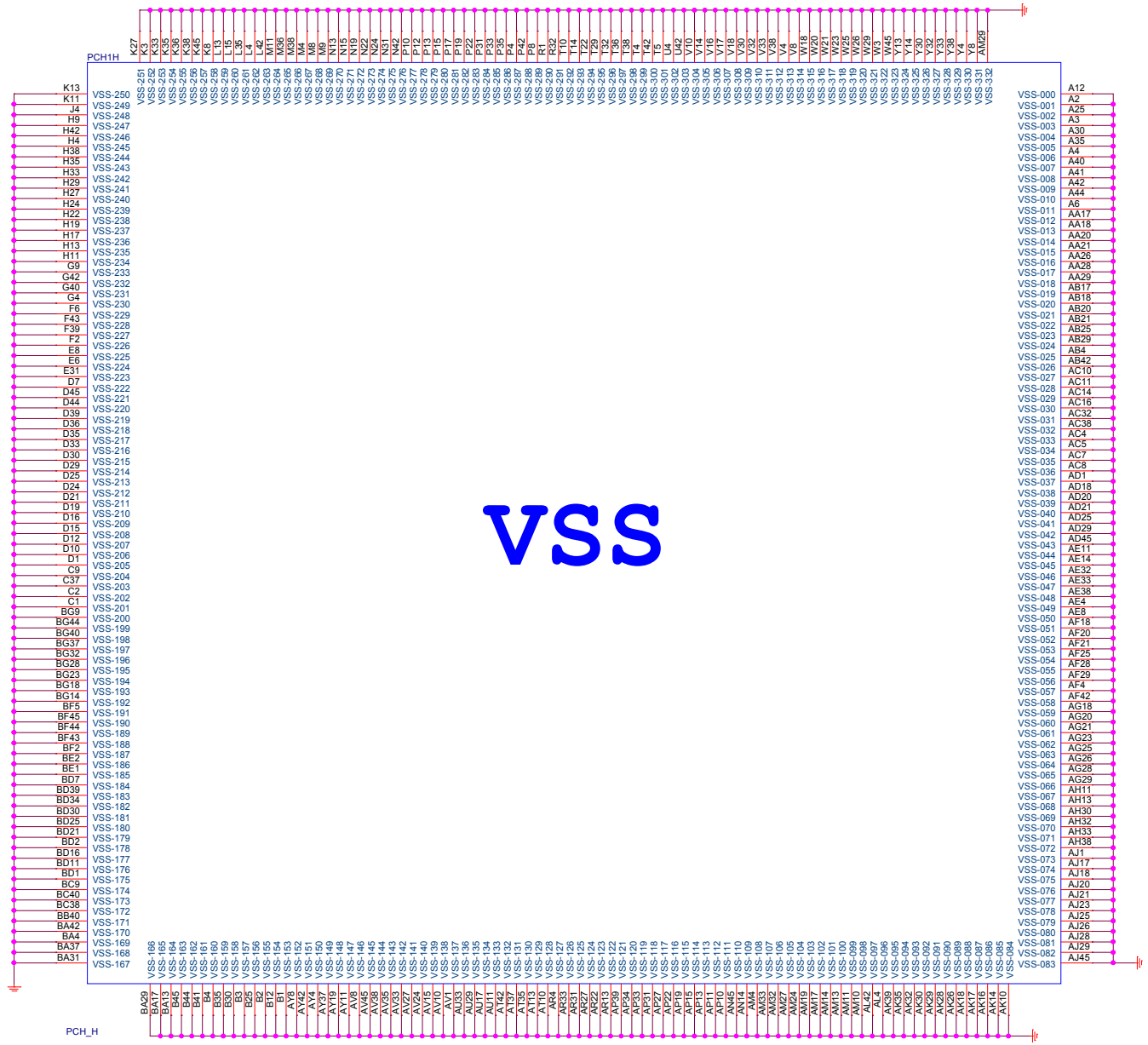

MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: PCH-Power
Rev: 10	
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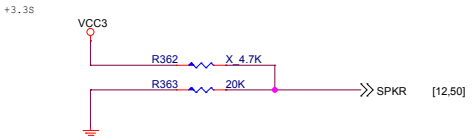
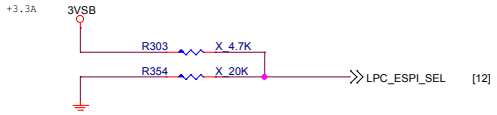
TOP Swap



Internal pull-down is disabled after PLTRST#

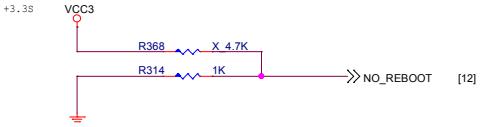
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

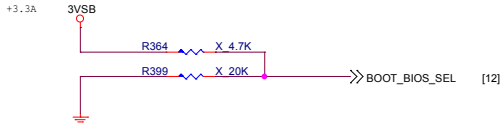
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

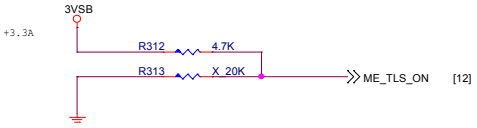
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

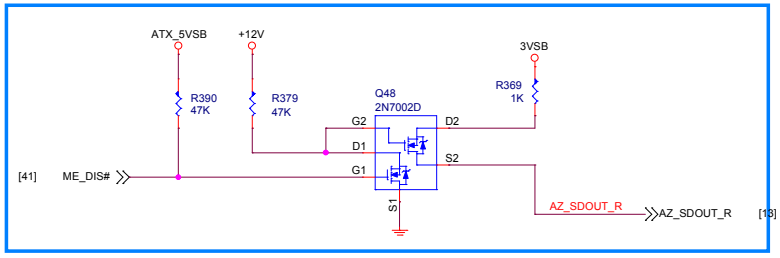
AMT and SBA with confidentiality



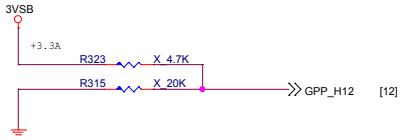
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

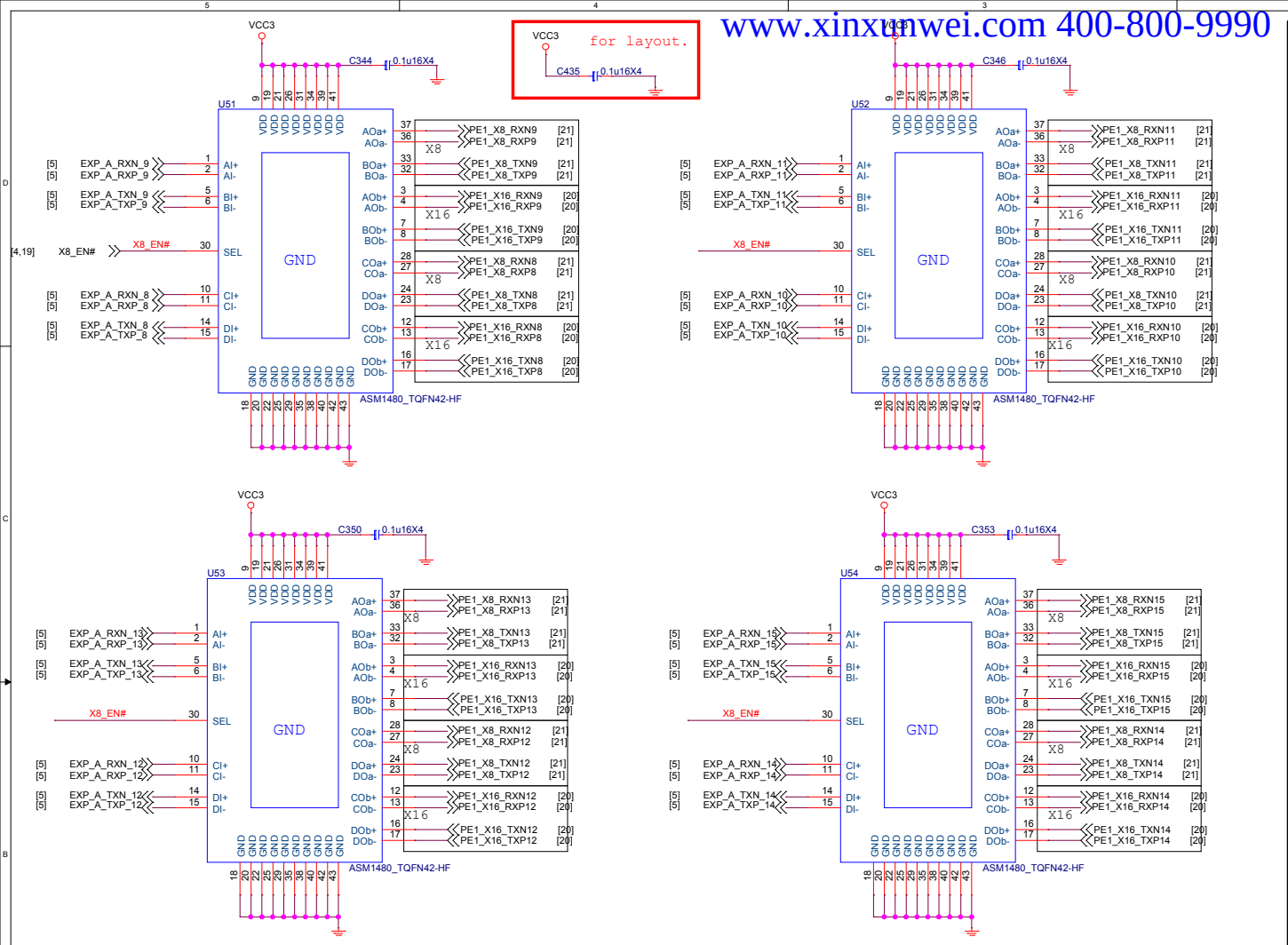
Internal pull-down is disabled after RSMRST

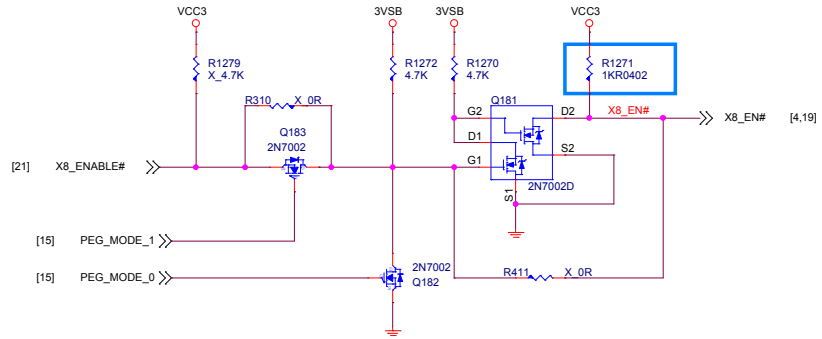
MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	PCH-Strap	10

Date: Monday, July 24, 2017 Sheet 18 of 72





MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0/2	MODE_1
AUTO	0	1

MICRO-STAR INT'L CO.,LTD

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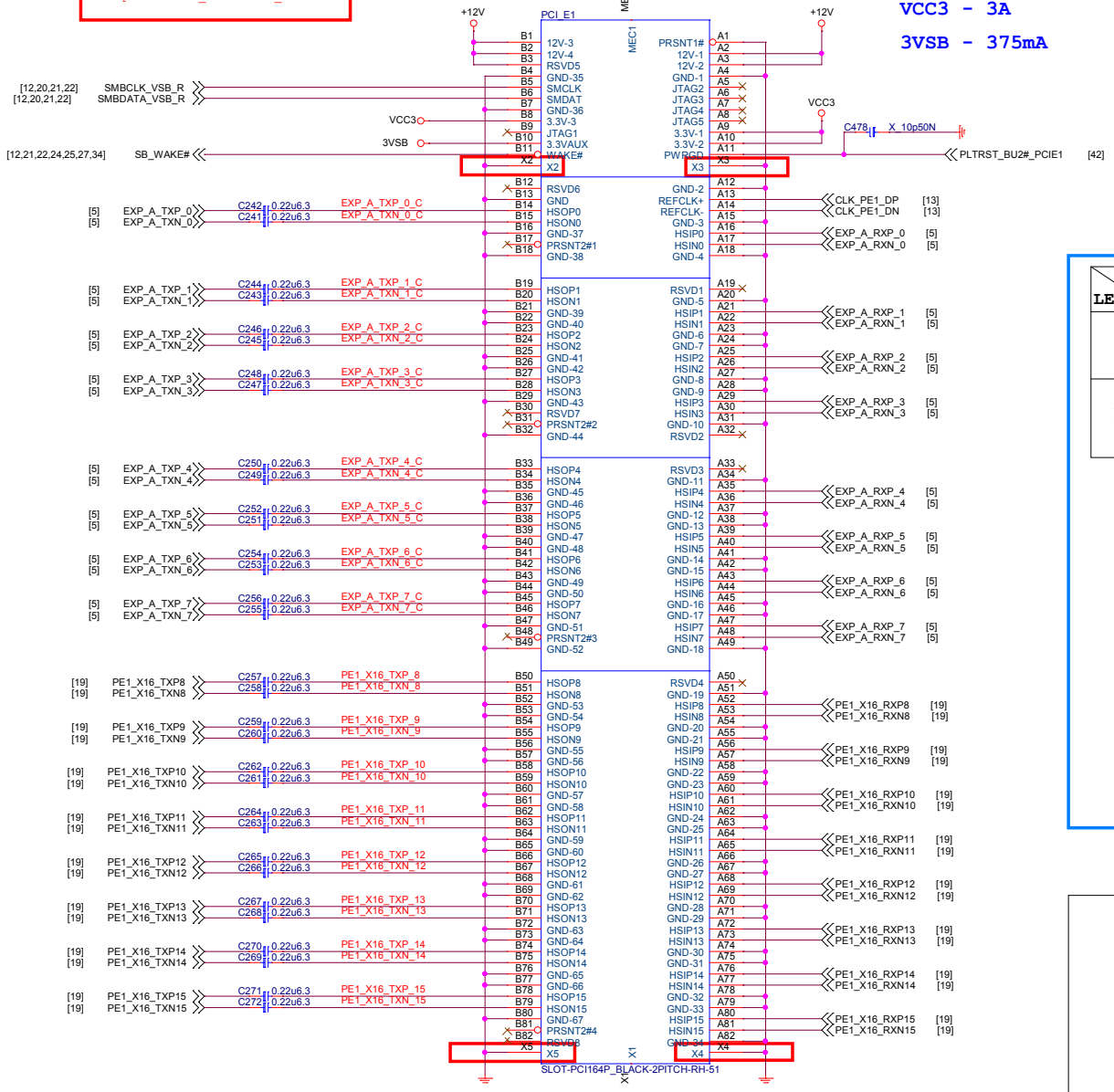
Size	Document Description	Rev
Custom	PCIE SWITCH	10

Date: Monday, July 24, 2017 Sheet 19 of 72

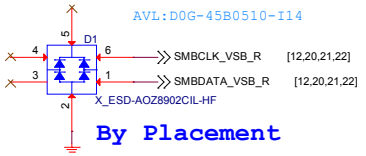
P/N:N11-1641491-L06
Footprint:SLOT_PCIEXP164_13

12V - 5.5A
VCC3 - 3A
3VSB - 375mA



SMBCLK_VSB_R R676 4.7KR/4 3VSB
SMBDATA_VSB_R R681 4.7KR/4 3VSB

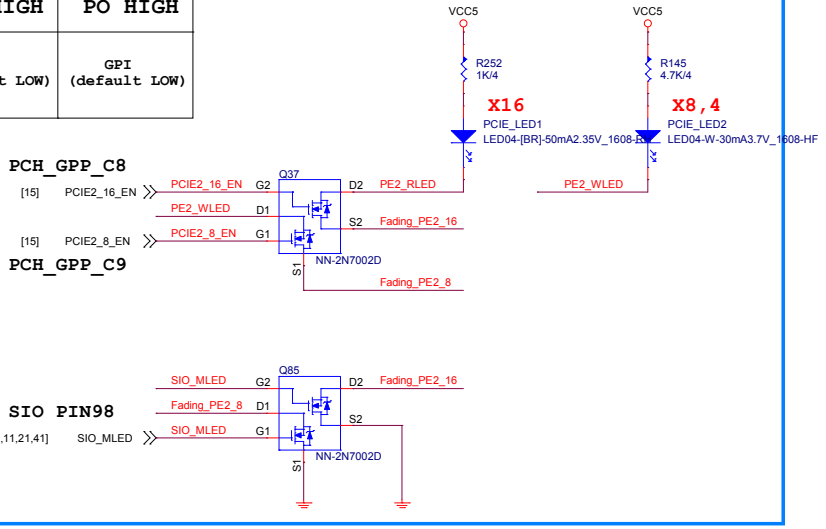
SMBUS_ESD

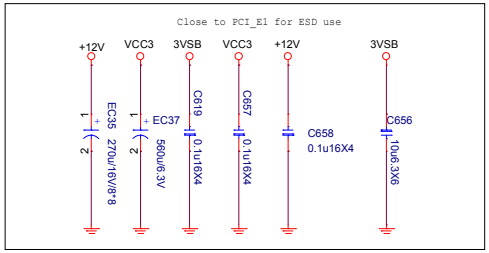


By Placement

GPIO / LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

PCIE SLOT LED





MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	PCIE SLOT (X16)	10

Date: Monday, July 24, 2017 Sheet 20 of 72

PCI Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSB- 375mA

P/N:N11-1000221-L06
Footprint:SLOT_PCIEXP100_5

P/N:N11-1000151-L06
Footprint:SLOT_PCIEXP100_3

PCI_E4 — SLOT-PCI100P_BLACK-2PITCH-RH-5

PCI_E6 — SLOT-PCI100P_BLUE-2PITCH-RH

20170216

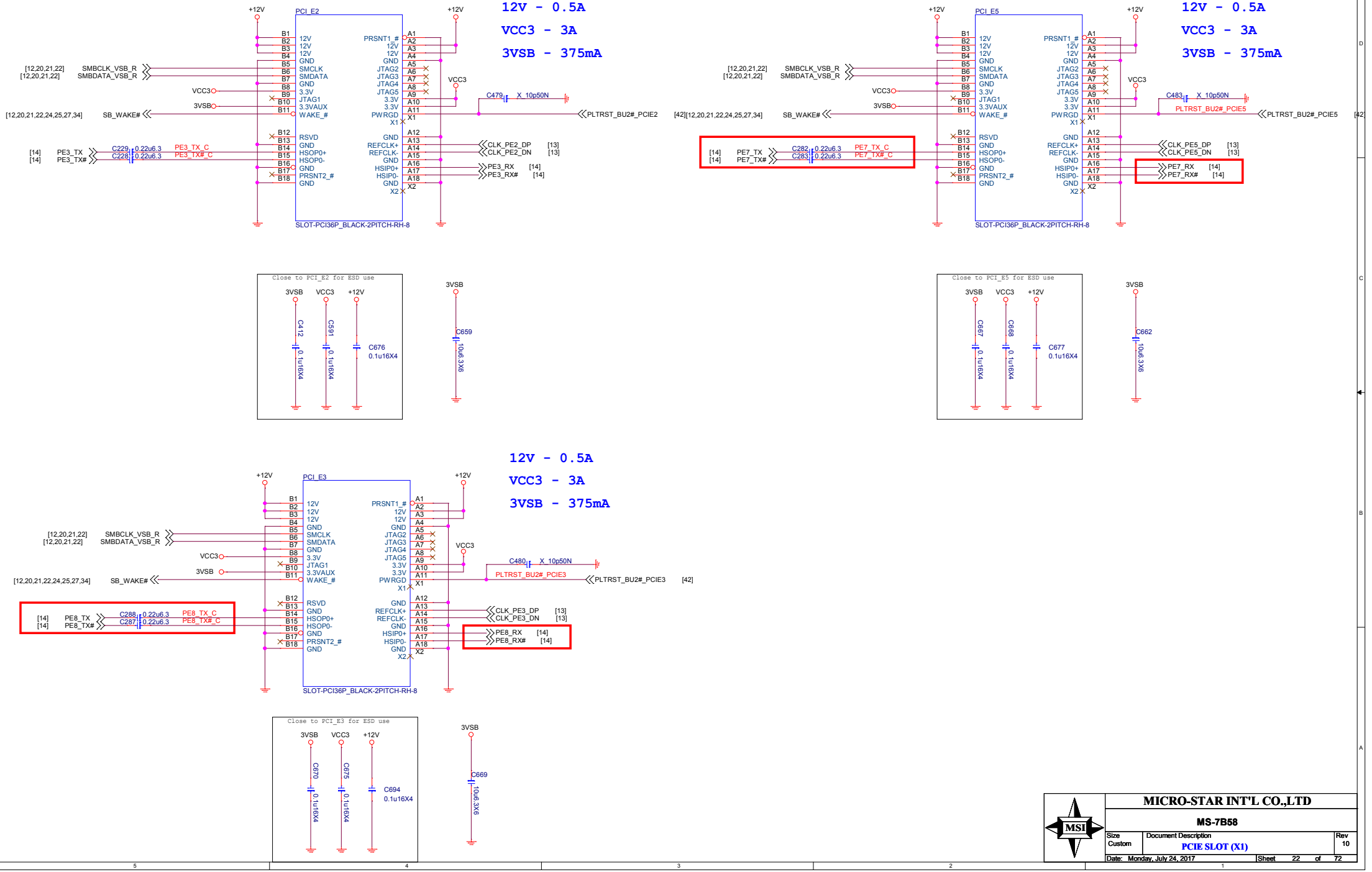
Close to PCI_E4 for ESD use

Close to PCI_E6 for ESD use

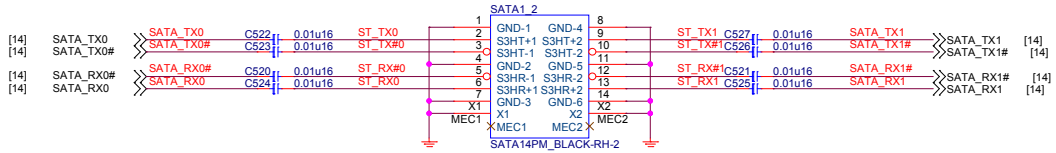
X8,4 — PCIE_LED3 LED04-W-30mA3.7V_1608-HF

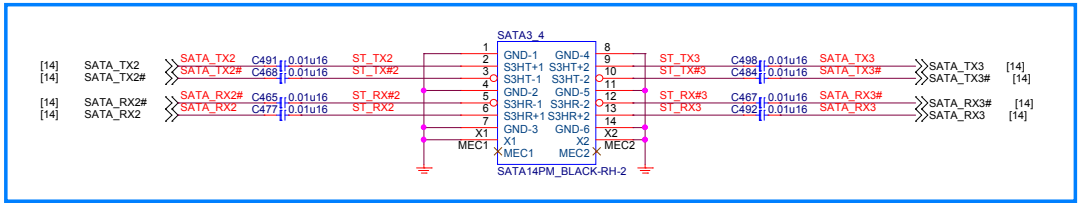
X4 — PCIE_LED4 LED04-W-30mA3.7V_1608-HF VF:2.7~3.7V

MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: PCIE SLOT (X4) — Rev: 10
Date: Monday, July 24, 2017	Sheet 21 of 72

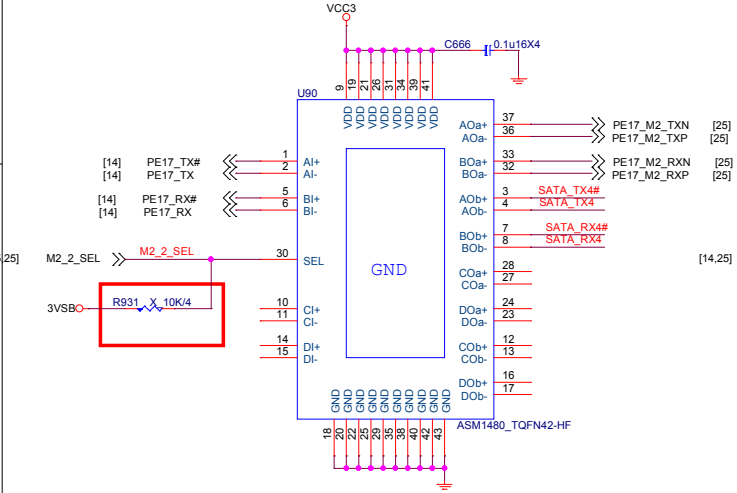


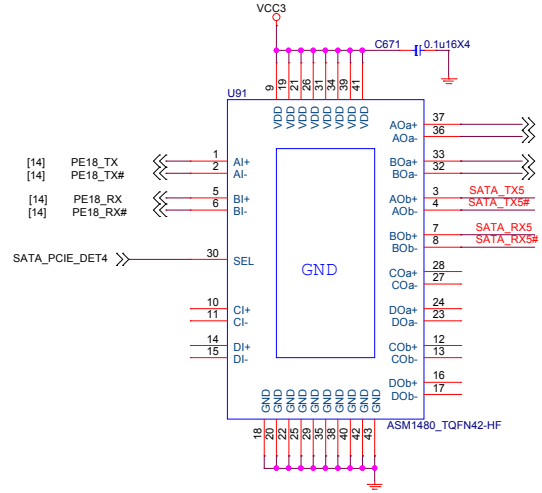
MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: PCIE SLOT (X1)
Rev: 10	
Date: Monday, July 24, 2017	Sheet 22 of 72

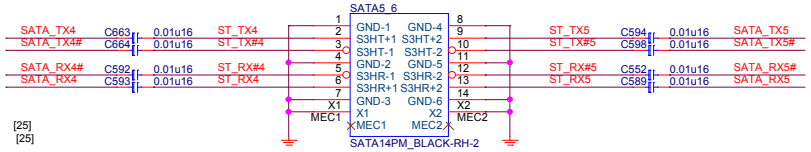




M2_2_SEL
0:to m2_2
1:to SATA

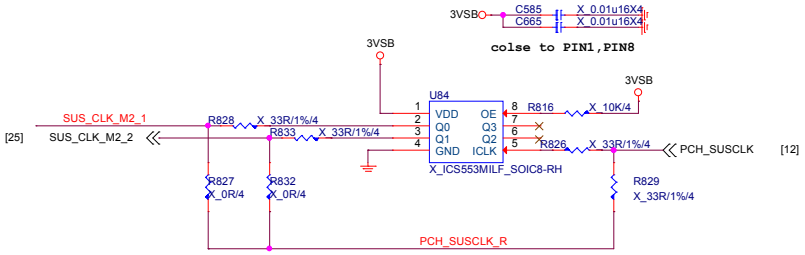


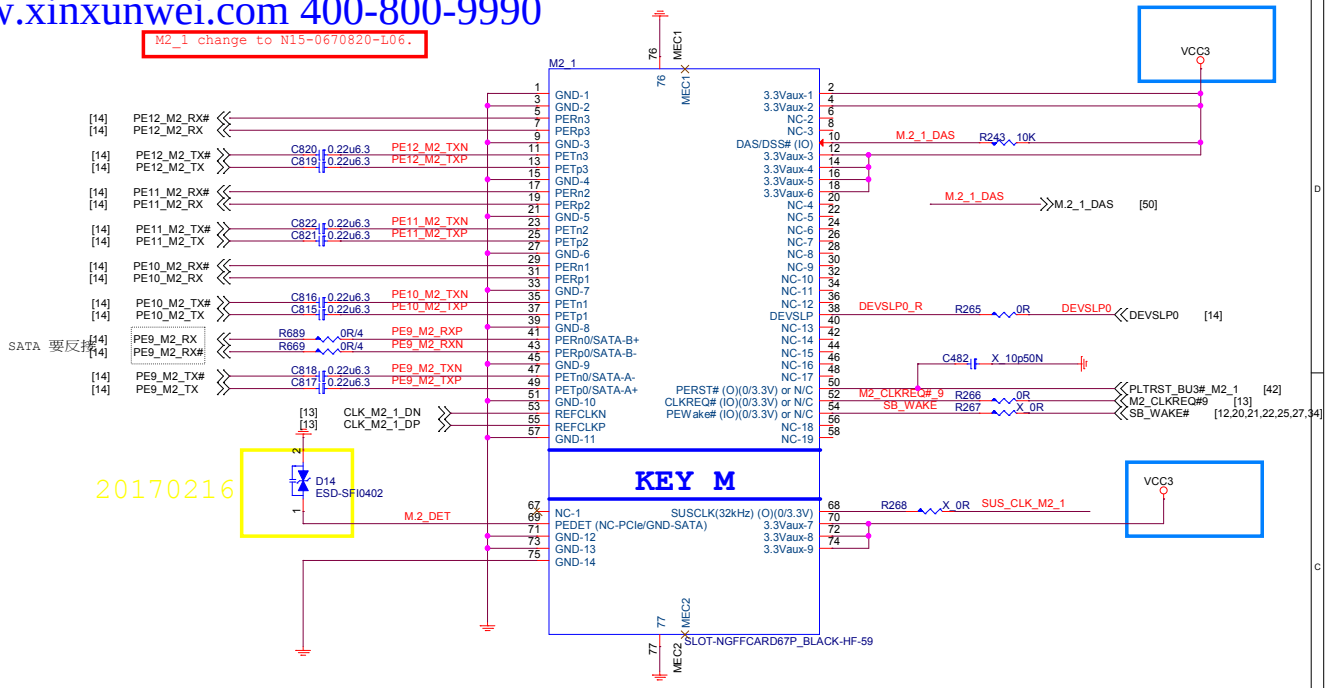




MICRO-STAR INT'L CO.,LTD		
MS-7B58		
Size: Custom	Document Description: SATA Connector	Rev: 10
Date: Monday, July 24, 2017	Sheet 23 of 72	

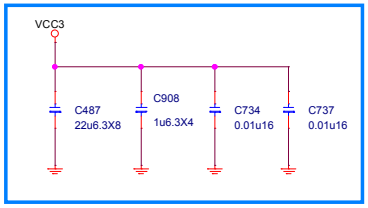
M2_1 change to N15-0670820-L06.



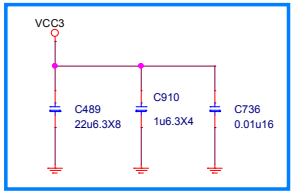


M.2 VCC3>=2.5A

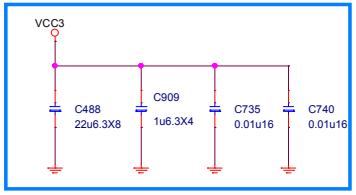
Near Pin2,Pin4

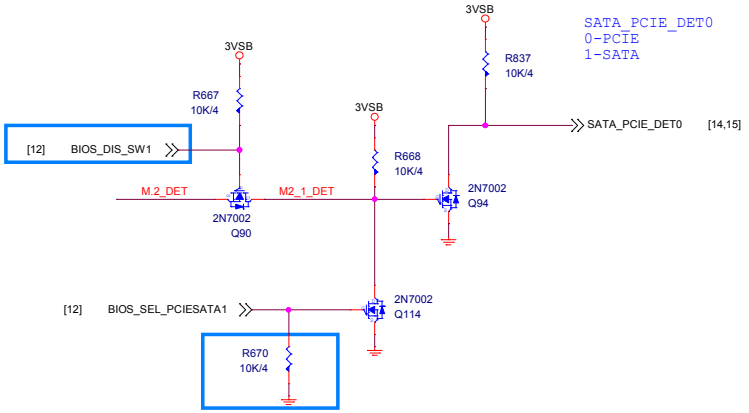


Near Pin12,Pin14,Pin16,Pin18



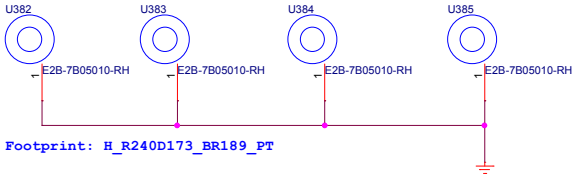
Near Pin70,Pin72,Pin74

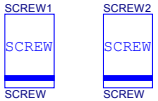


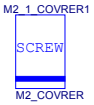


BIOS_MODE

BIOS_DIS_SW	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

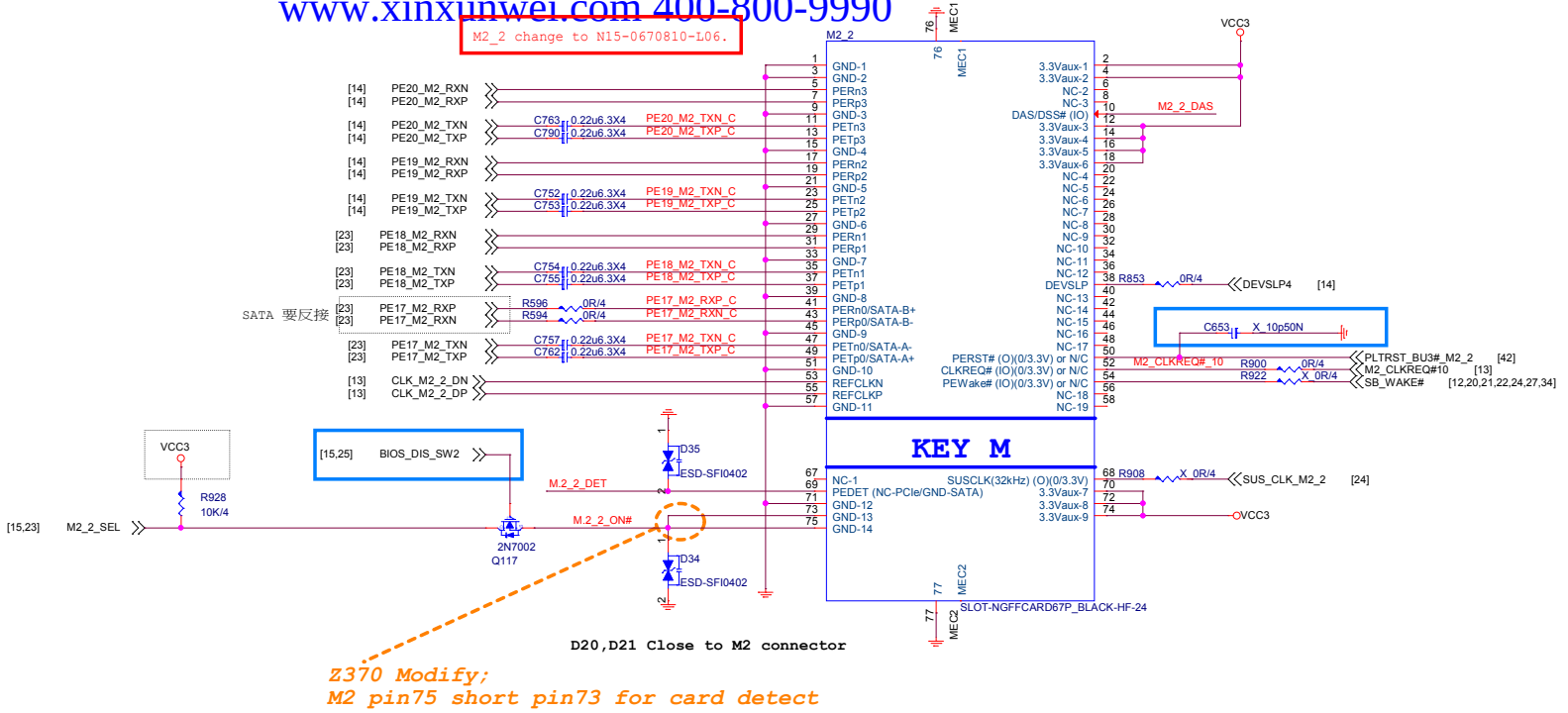






MICRO-STAR INT'L CO.,LTD	
MS-7B58	
Size: Custom	Document Description: M.2-SLOT1
Rev: 10	
Date: Monday, July 24, 2017	Sheet 24 of 72

M2_2 change to N15-0670810-L06.

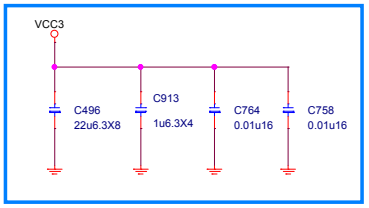


D20,D21 Close to M2 connector

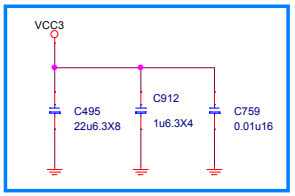
Z370 Modify;
M2 pin75 short pin73 for card detect

M.2 VCC3>=2.5A

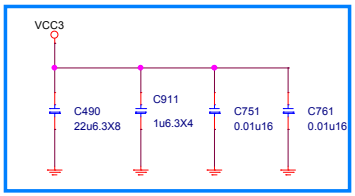
Near Pin2,Pin4

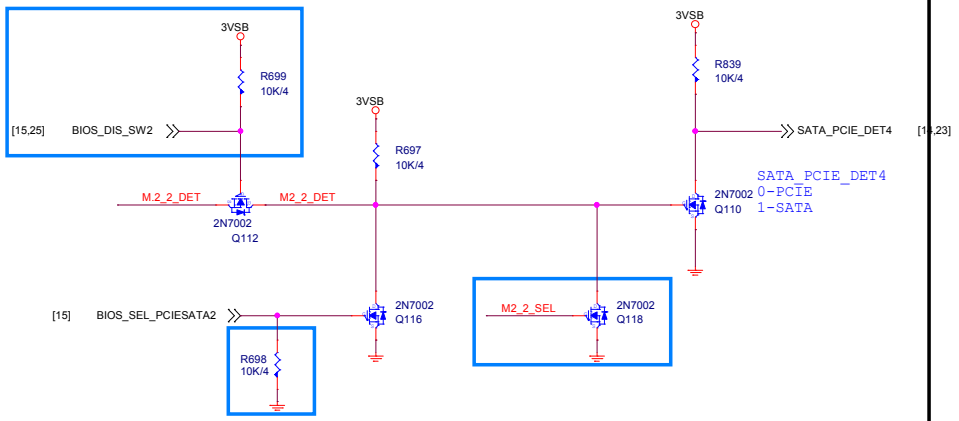


Near Pin12,Pin14,Pin16,Pin18



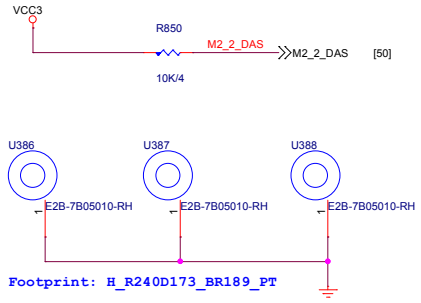
Near Pin70,Pin72,Pin74



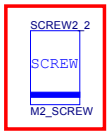


BIOS_MODE

BIOS_DIS_SW	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
0	*0*	*1*	*M2-SATA*
0	*0*	*0*	*M2-PCIE*
GPI	*GPI*	*GPI*	*AUTO*



Footprint: H_R240D173_BR189_PT



MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	M.2-SLOT2	10

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MICRO-STAR INT'L CO.,LTD

MS-7B58

Size	Document Description	Rev
Custom	U.2 Connector	10

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Z370 modify ASM2142-->ASM3142

Common trace should be greater than >15mil with other signal.

CLK Rule (Follow SB PDG)

[13] CLK_ASM1142_DP
[13] CLK_ASM1142_DN

PCIE Rule (Follow SB PDG)

[14] PE5_ASM_RX
[14] PE5_ASM_RX#
[14] PE5_ASM_TX
[14] PE5_ASM_TX#
[14] PE6_ASM_RX
[14] PE6_ASM_RX#
[14] PE6_ASM_TX
[14] PE6_ASM_TX#

C797 X_10p50N PLTRST_BU1#_ASM1142
ASM1142_WAKE#
TPU1

UU1A 1042

PE_CLKP
PE_CLKN
PTX0P
PTX0N
PRX0P
PRX0N
PTX1P
PTX1N
PRX1P
PRX1N
PE_RST#
PE_WAKE#
RSV
SMI#
PORST#
SPI_CLK
SPI_CS#
SPI_DI
SPI_DO
XI
XO
UART_RX
UART_TX
TEST_EN
REXT

ASM3142

ASM3142-RH

USB HS (90Ohm-Diff)

U2DP_A / U2DM_A
SSD12+ / SSD12-
U3TXP_A / U3TXN_A / U3RXP_A / U3RXN_A
SSTX12P / SSTX12N / SSRX12P / SSRX12N
USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)
U2DP_B / U2DM_B
SSD13+ / SSD13-
U3TXP_B / U3TXN_B / U3RXP_B / U3RXN_B
SSTX13P / SSTX13N / SSRX13P / SSRX13N
USB SS (80Ohm-Diff)
PRON_A / PRON_B
PPONA / PPONB
PPON_X Internal Pull-up to VCC3
OCI_A# / OCI_B#
OCIA / OCIB
OCI_X Internal Pull-up to SUS
UART_RX / UART_TX
RX/TX Internal Pull-up

Chip to Connector ~1.5 inch.

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

UART_RX RU22 X_4.7K
UART_TX RU23 X_4.7K
For sata express mode use only.

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

XO CU25 12p50N XI
YU1
D04-0901200-F07
D04-0901100-T16
YU1 20MHZ18p_S

UU1B 1042 ASM3142

NC-1 NC-2 NC-3 NC-4
VCCHSUS
VDDSUS-1 VDDSUS-2
GND PGND
VCCH-1 VCCH-2
VCCLP-1 VCCLP-2
VCCLU-1 VCCLU-2 VCCLU-3
VDD-1 VDD-2 VDD-3
VDDP-1 VDDP-2
VDDU-1 VDDU-2 VDDU-3

3VSB USB3_1P1_VSB
VCC3 USB3_2P5 USB3_1P1
TPU9

ASM3142-RH

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

ASM_SMI1 RU17 80.6K1% VCC3 PONRST# CU9 1u16X6
USB_SPISCK USB_SPICSB USB_SPISI USB_SPISO

[12,20,21,22,24,25,34] SB_WAKE#
SB_WAKE# CU51 0.1u16X4 ASM1142_WAKE#
Q64 NN-2N7002D
S1 ASM_SMI1
3VSB RU46 4.7K
[15] GPP_C23_USB3_SMI
VCC3 RU51 4.7K

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

P/N:B02-031420C-AD0

VCC3 RU47 4.7K USB_SPISCK RU48 X_4.7K

[42]
[15] GPP_D23
PLTRST_BU1#
3VSB CU45 X_0.1u16X4
UU8 X_NC7SZ08M5X_SOT23-5
ASM2142_RST# RU7 23R0402 PLTRST_BU1#_ASM1142
RU6 0R

	UU8	RU6	CU39
ASM2142	O	X	O
ASM3142	X	O	X

O: Stuff
X: Unstuff

USB3_1P1 Close to UU1.58 CU50 10u6.3X6
USB3_1P1 Close to UU1.41 CU48 10u6.3X6
USB3_1P1 Close to UU1.35/47/52 CU16 CU19 CU26 2.2u6.3
USB3_1P1_VSB Close to UU1.21/34 CU21 CU23 0.1u16X4
VCC3 Close to UU1.4/32 CU10 CU13 0.1u16X4
USB3_2P5 Close to UU1.38/44/55/62 CU11 CU12 CU14 CU15 2.2u6.3
USB3_1P1 Close to UU1.1/12/33 CU17 CU18 CU20 0.1u16X4
3VSB Close to UU1.24 CU22 0.1u16X4
CU52 0.1u16X4
Close to UU1.20

ASM3142 1.1v Core Power

SN:L01-0107118-M26

VCC5 CU31 22u6.3X8 RU2 47K VCC3
UU6 MP2143DJ_TSOT23-8-RH
VIN EN PG SW OUT FB PGND AGND
USB3_1P2_PH LU3 1.0u5.5A-35_1210-HF USB3_1P1
USB3_1P2_FB RU3 200K1%04 CU28 X_0.1u16X4 RU4 240K1%04
CU32 22u6.3X8 CU33 22u6.3X8 CU29 0.1u16X4

ASM3142 2.5v Analog Power

VCC3 CU37 1u6.3X4
UU7 GS7116S_SOT23-5-RH
VDD VOUT EN GND ADJ
USB3_2P5
CU34 47p50N04 RU39 430K1%04 CU38 1u6.3X4
RU35 200K1%04

ASM3142 1.1v Suspend Power

3VSB CU2 1u6.3
UU2 GS7116S5-ADJ-R
VDD VOUT EN GND ADJ
USB3_1P1_VSB
CU4 47p50N04 RU34 75K1%04 CU3 1u6.3
RU33 200K1%04

EEPROM

VCC3 RU27 10K RU30 10K USB_SPICSB
UU3 MX25L512EMI-10G
HOLD WP CS VCC SI SO SCK GND
CU49 0.1u16X4
USB_SPISO RU24 X_4.7K USB_SPISI USB_SPISCK
RU38 X_4.7K USB_SPISO

M:M31-25L1022-M24 (1M)
S:M31-25X2023-W03 (2M)

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ASM 1142	10

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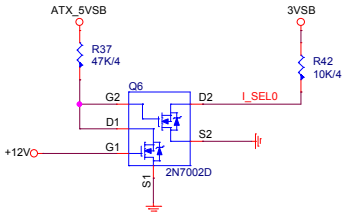
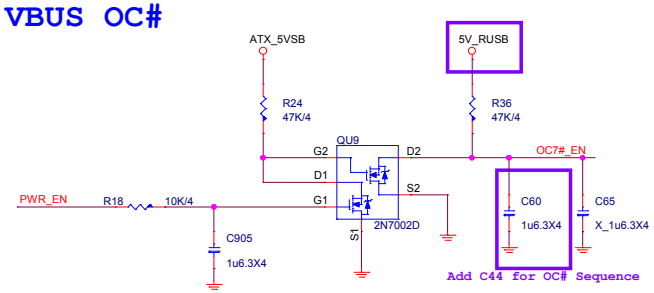
Current Mode

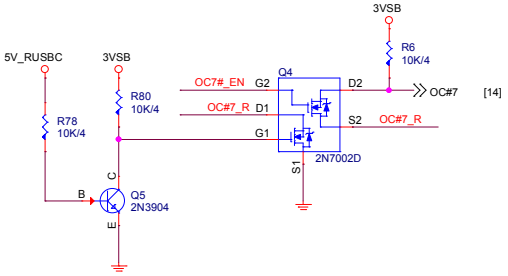


I_SEL0 : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

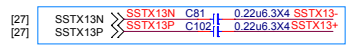
1.5A under S3 mode
3A under S0 mode

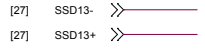
VBUS OC#

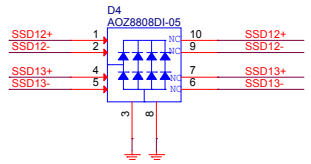


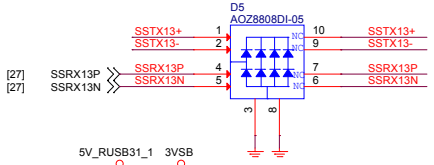


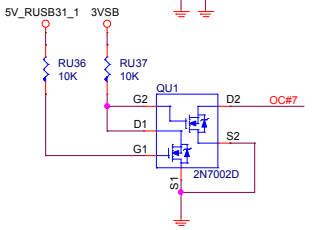
TYPE-A



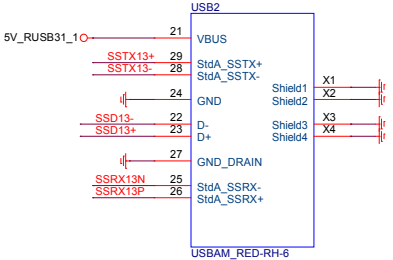


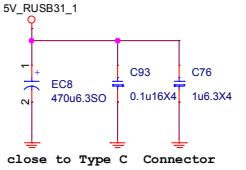




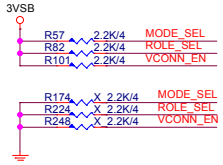


Red gold plating





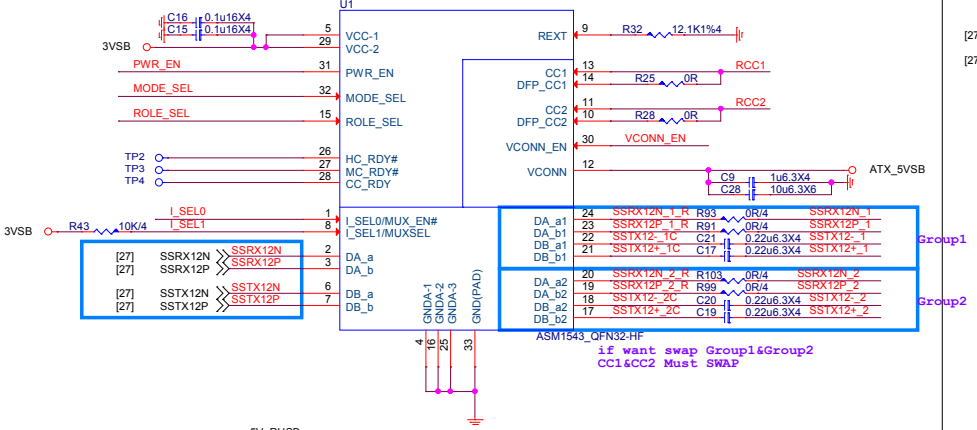
USB Type-C MUX with Configuration Channel (CC)



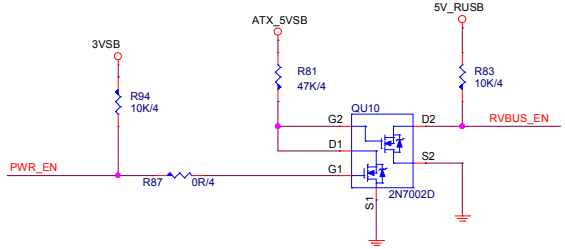
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

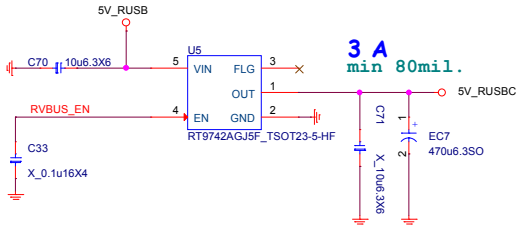
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

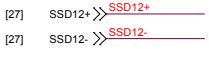


if want swap Group1&Group2
CC1&CC2 Must SWAP





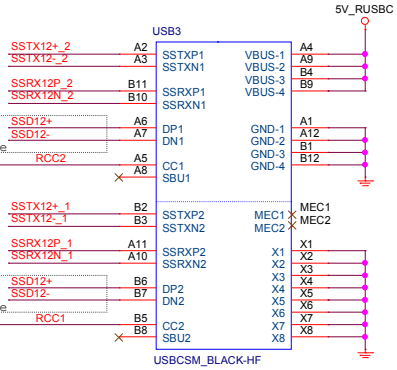
TYPE-C

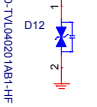


Port反結時CC也反接
T-type 分支需小於140mils

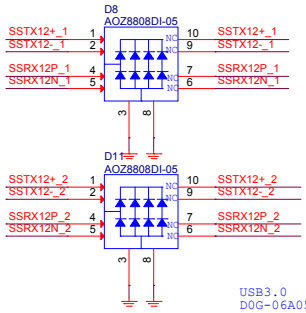
OC#7

Black gold plating

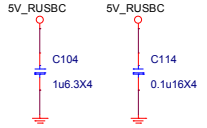




ESD Protection
NEAR CONNECTOR



close to Type C Connector



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

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Size	Document Description	Rev
Custom	USB TYPE C	10

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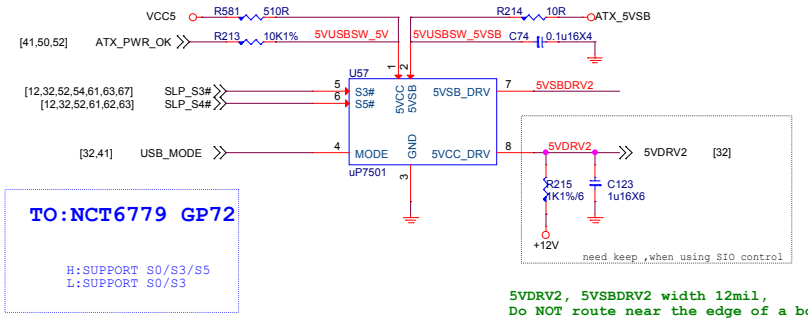
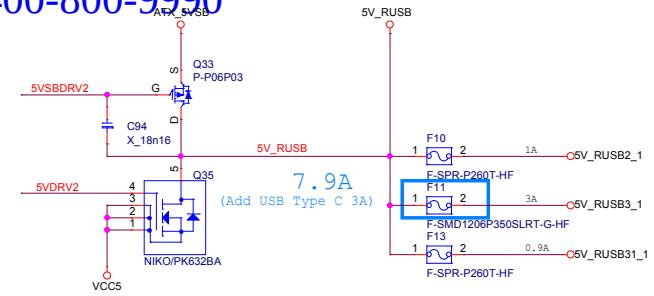
USB PORT POWER



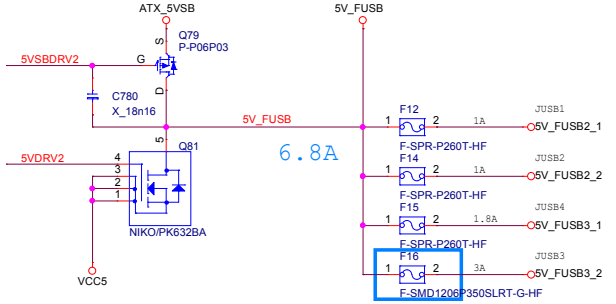
TO:NCT6779 GP72

H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



need confirm C780 value



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-005
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

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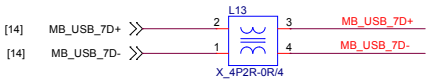
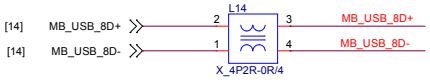
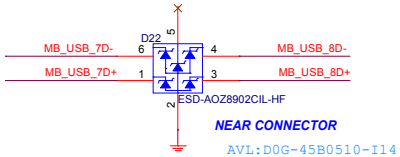
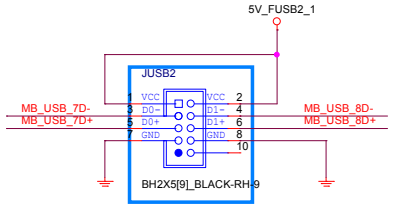




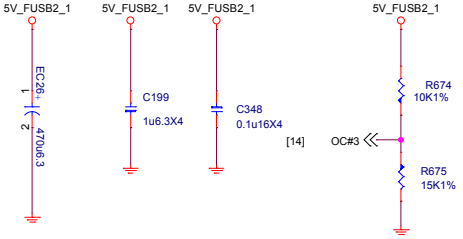


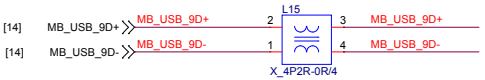
AVL:D0G-45B0510-I14

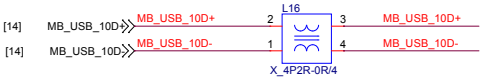
1.0A

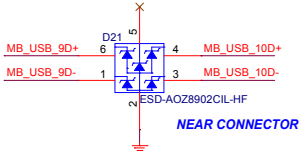


EMI Cap near Connector.



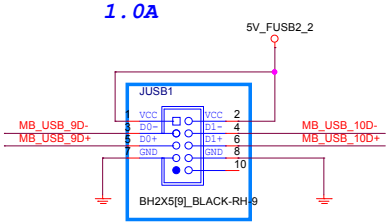




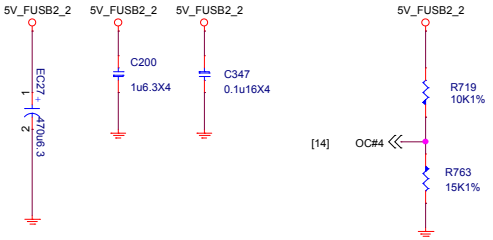


AVL:D0G-45B0510-I14

1.0A



EMI Cap near Connector.



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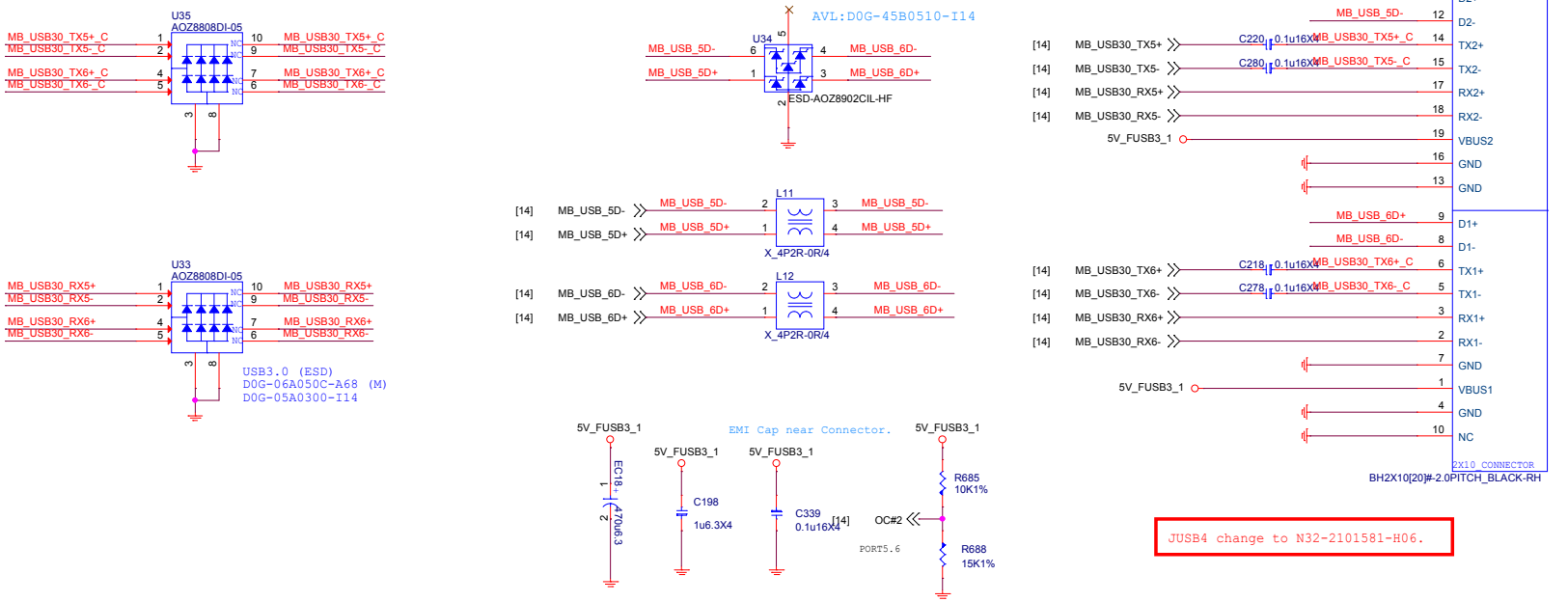

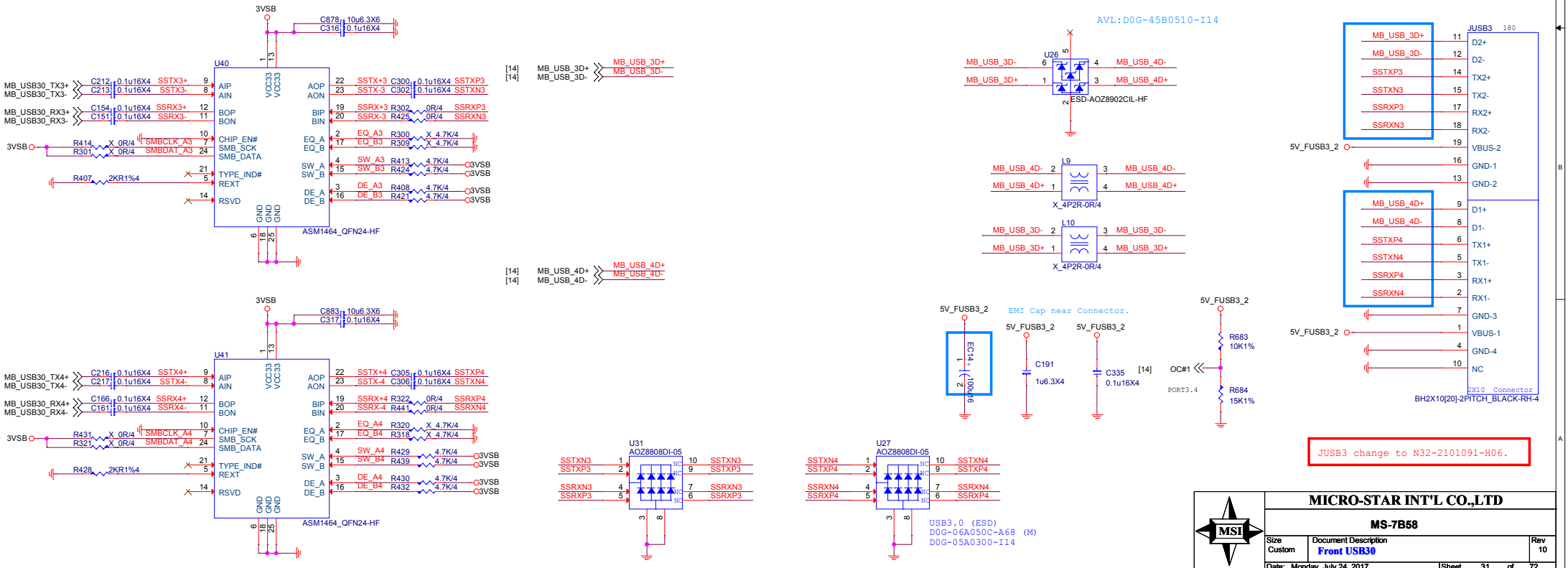

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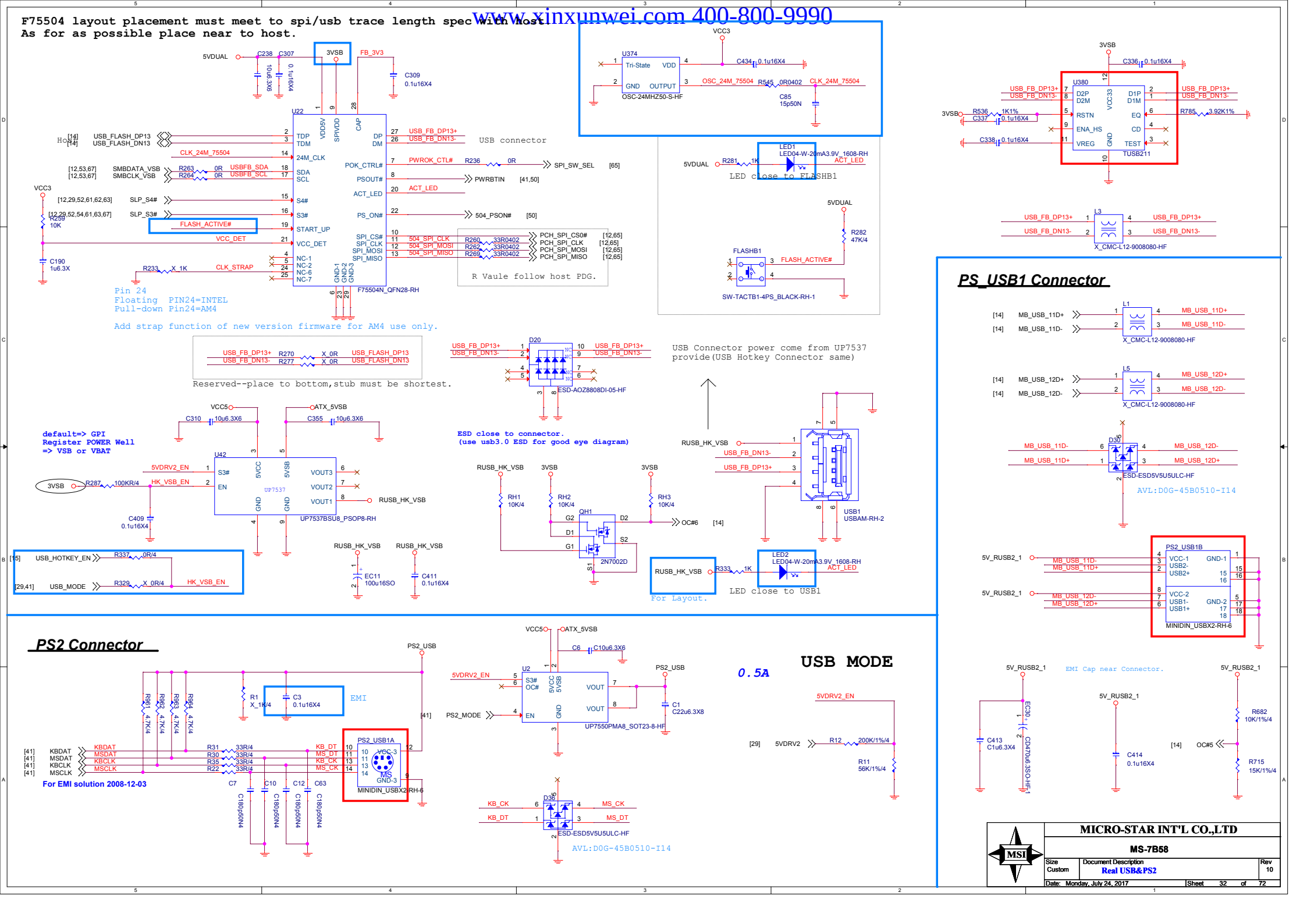
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



PS_USB1 Connector

PS2 Connector

USB MODE

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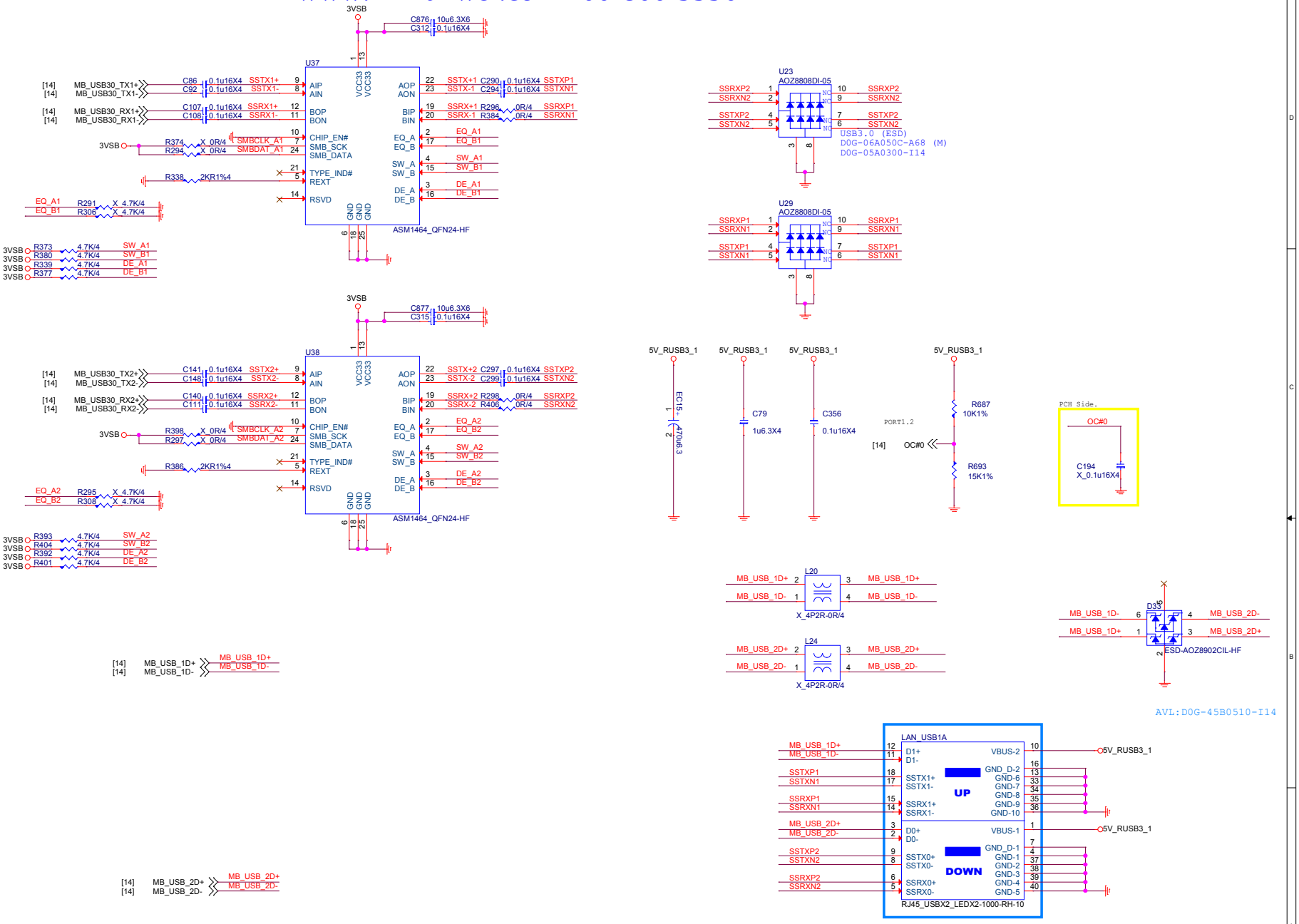
LAN USB3.0



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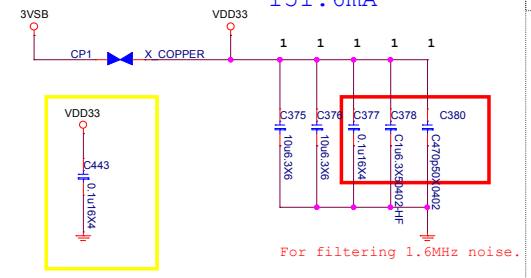
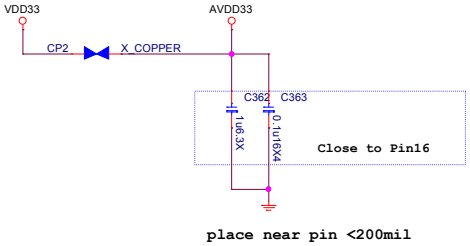
E2400 GIGA LAN

PIN2:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

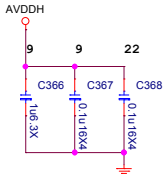
E2500:B06-E25000C-R54
E2400:B06-E24000C-R54

151.6mA

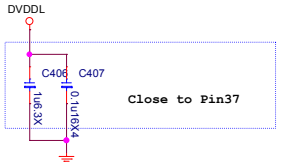




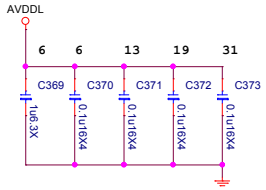
place near pin <200mil



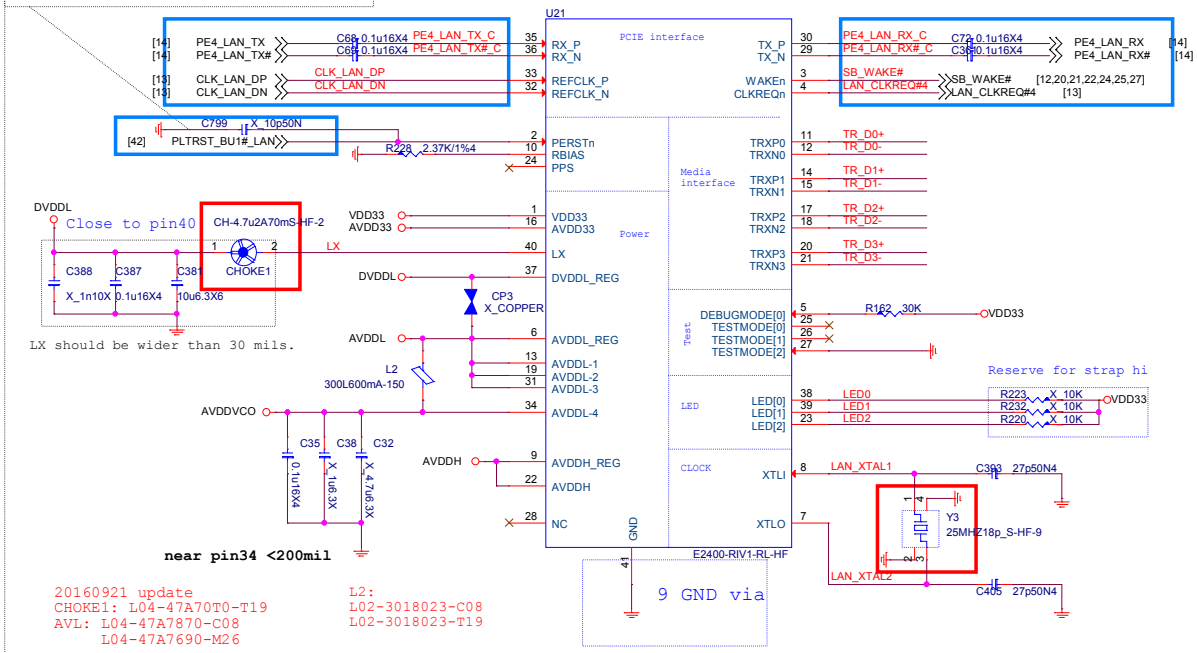
place near pin <200mil



place near pin <200mil



place near pin <200mil



20160921 update
CHOKE1: L04-47A70T0-T19
AVL: L04-47A7870-C08
L04-47A7690-M26

L2:
L02-3018023-C08
L02-3018023-T19

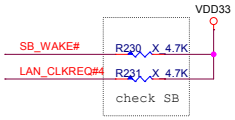
note:

LED0:
1=High core voltage
0=Low core voltage

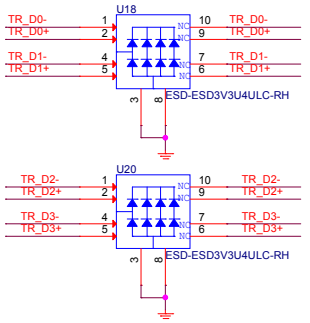
LED1:
1=SWR mode
0=LDO mode

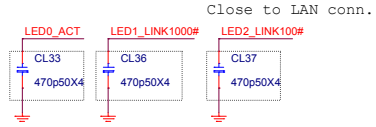
LED2:
1=25MHz clock
0=48MHz clock

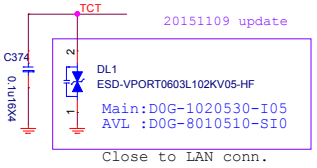
VDD33 >= 30mils;
AVDD33 >= 30mils;
AVDDH >= 20mils;
AVDDL >= 20mils.
DVDDL >= 20mils.
Pin LX to L1 >= 30mils.

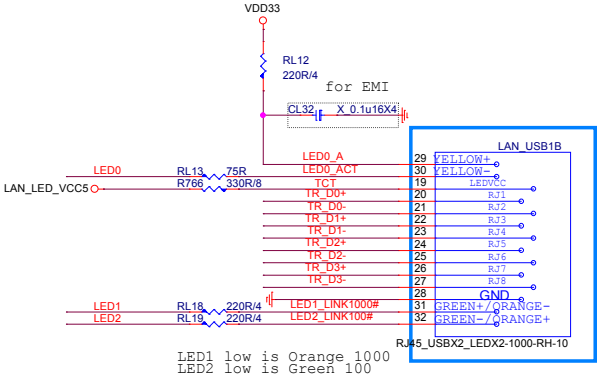


EMC

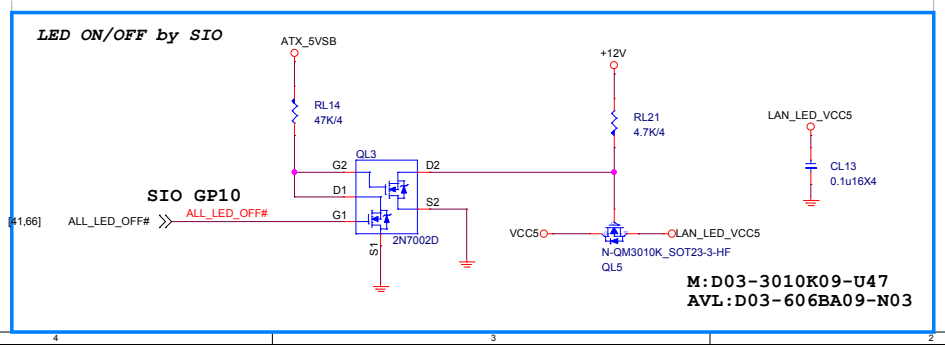








LED1 low is Orange 1000
LED2 low is Green 100



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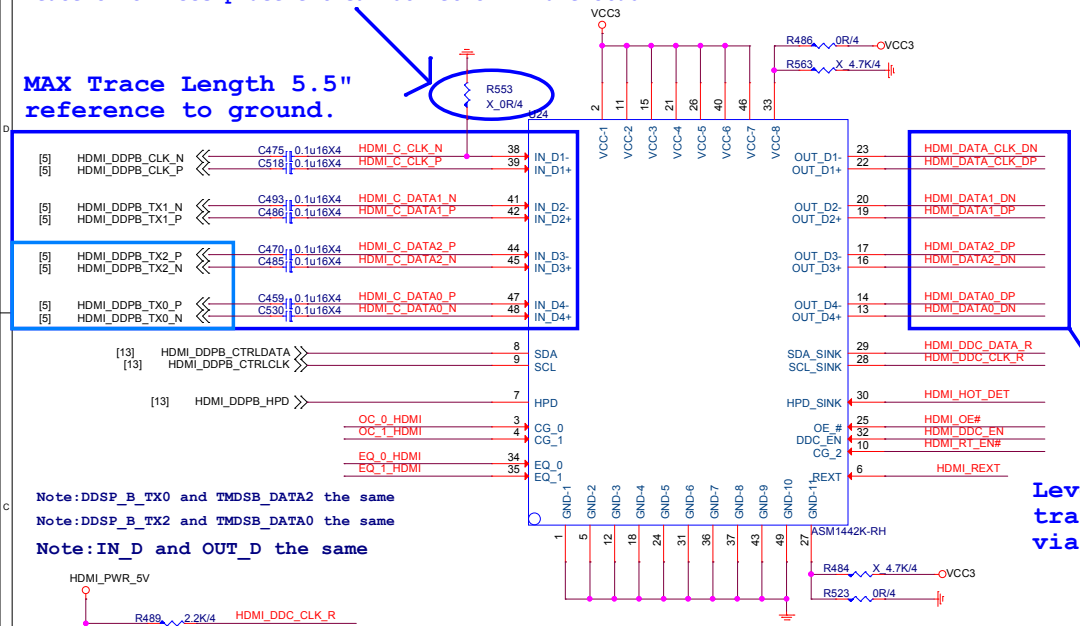
HDMI level shifter

Please CHECK R553 placement cannot let CLK- have stub

MAX Trace Length 5.5" reference to ground.



Note:DDSP_B_TX0 and TMDSB_DATA2 the same

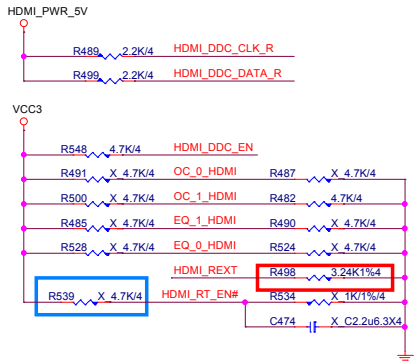
Note:DDSP_B_TX2 and TMDSB_DATA0 the same

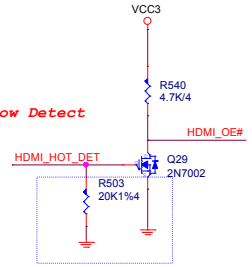
Note:IN_D and OUT_D the same

Level Shift to HDMI connector total trace length > 0.9" ; < 1"
via count ≦ 2 ,reference to ground.

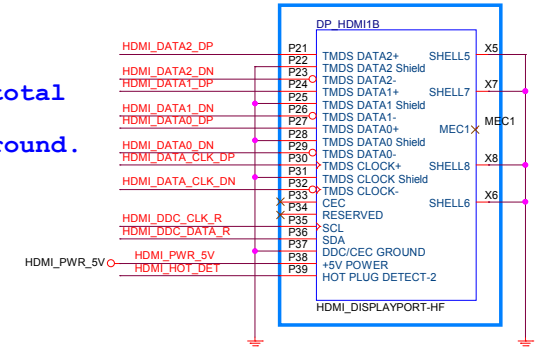
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

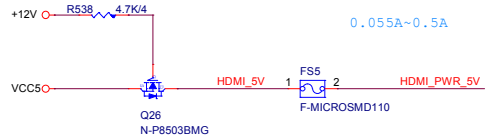
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	





注意High/Low Detect



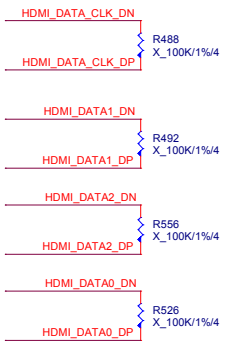


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

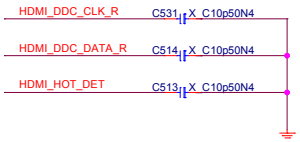
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

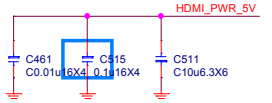
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

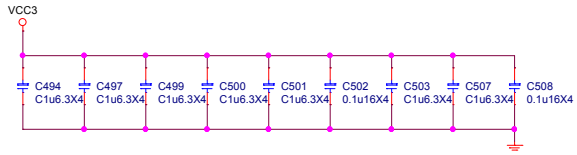
EMI



EMI cap.







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Custom	DP_HDMI1 Connector	10

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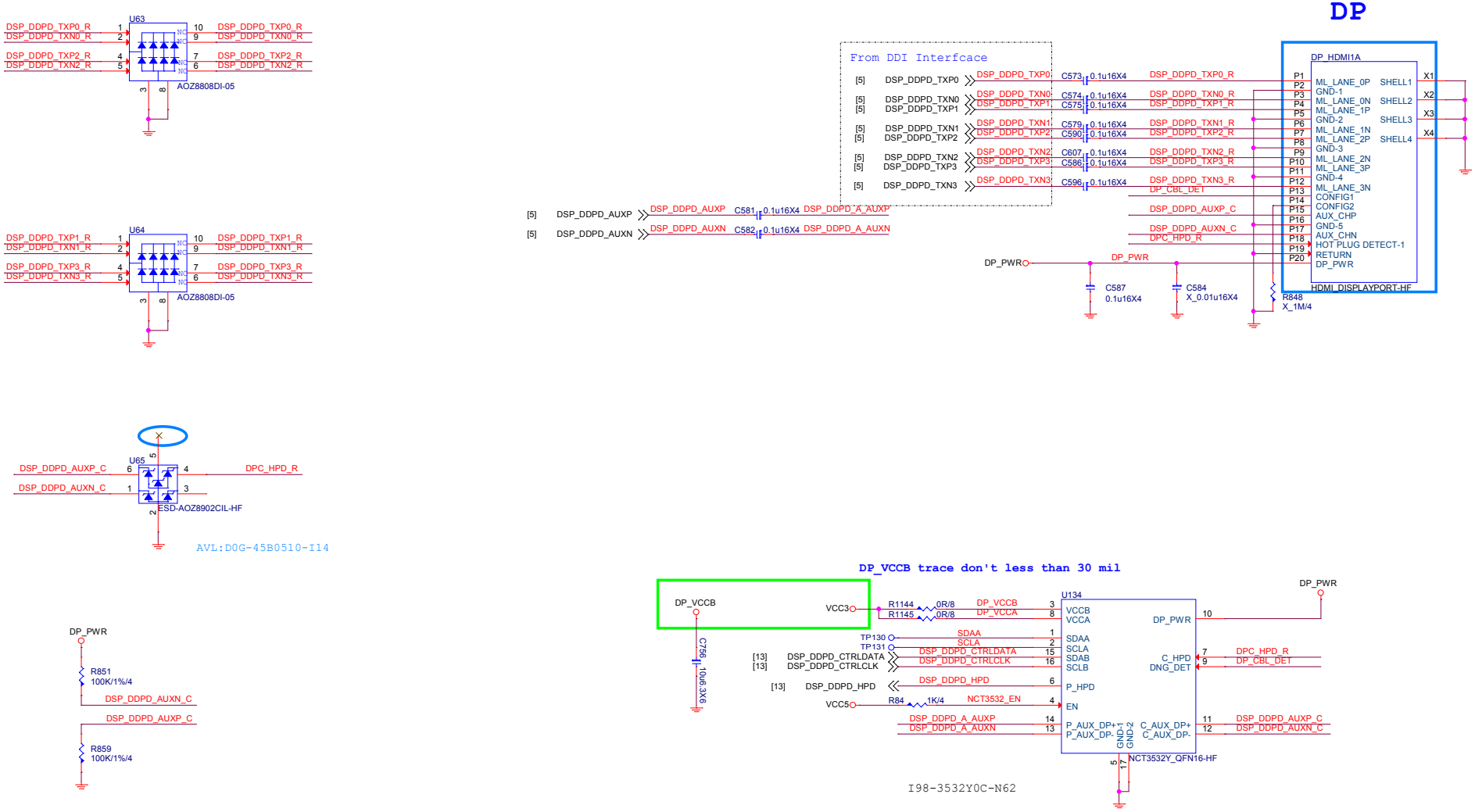
DP



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MS-7B58	
Size: Custom	Document Description: DP Connector
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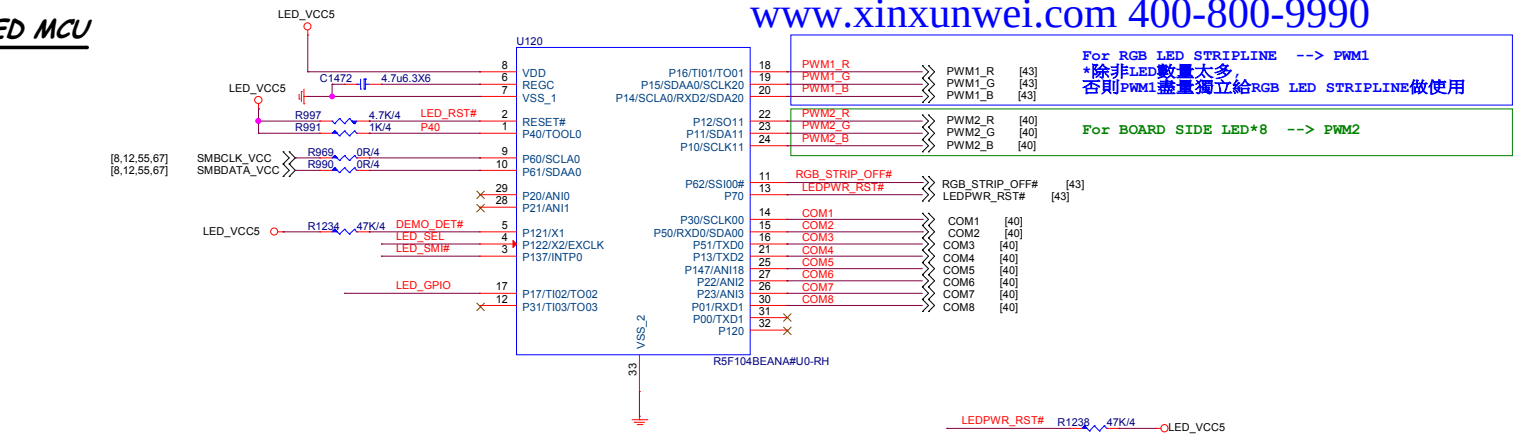
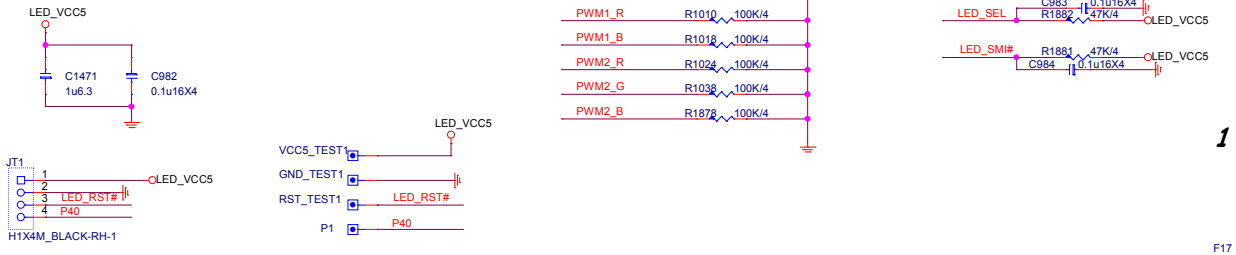
LED MCU



For RGB LED STRIPLINE --> PWM1
*除非LED數量太多，
否則PWM1盡量獨立給RGB LED STRIPLINE做使用

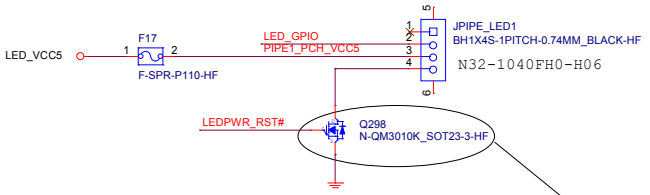
For BOARD SIDE LED*8 --> PWM2

Control	Net Name	PWM USE
PCH	LED_GPIO	PWM3
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
LED STRIPLINE	RGB_STRIP_OFF#	PWM1
Board Side LED	COM X~8	PWM2
PCIE Side LED	COM 1~X	PWM1



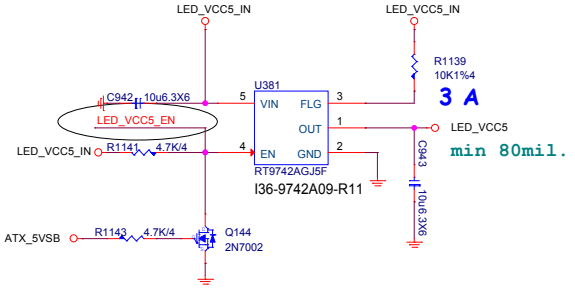
1 PCH HEATSINK LED

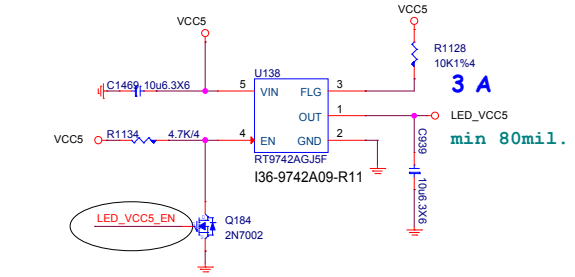
8PCS LED*0.16W=1.28W PIPE1_PCH_VCCS need 20mil



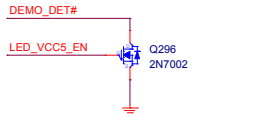
If JPIPE module doesn't has LED driver IC then can remove these MOS.

EXTERNAL POWER INPUT

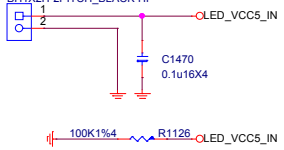




LED Demo Button



External Power



Delete JPIPE2/3
(Aduio/IO cover LED CONN.)
BY PM spec

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ALC1220

P/N:B05-012201C-R09

UA1

ALC1220-CG-RH

follow PCH power well

all of JD resistors should be placed as close as possible to the sense pin of codec.

Remove RA29,RA30

near JACK

CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

CPVDD:150mA

Closed Codec

EMI

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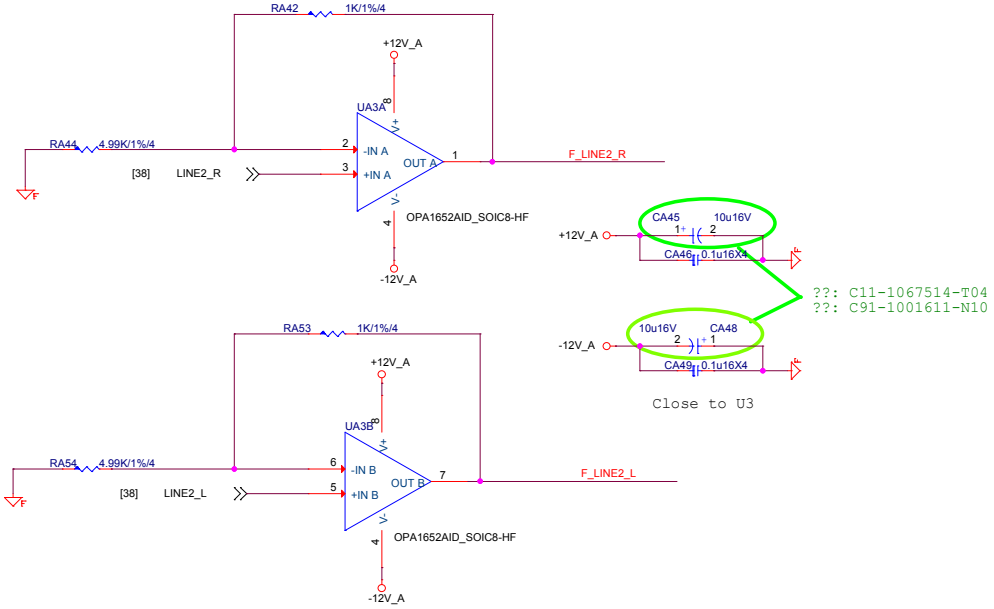
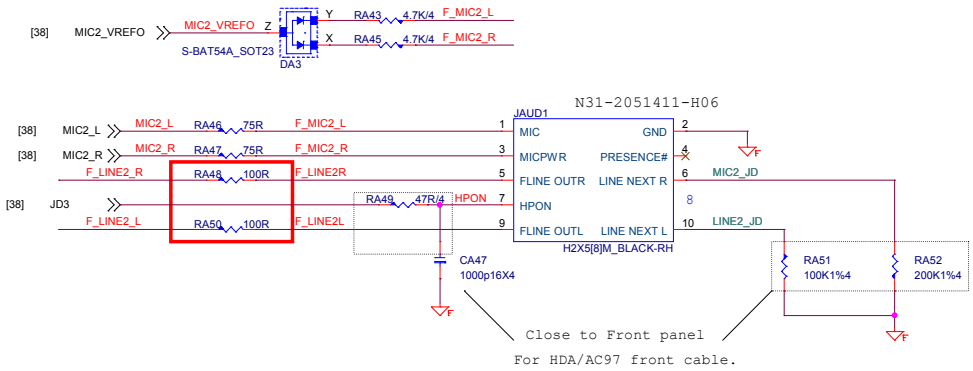
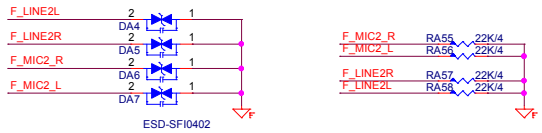




Close to Jack

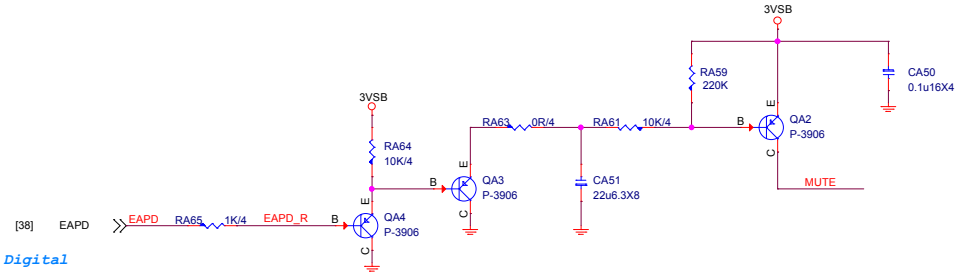
ESD protect

D0G-2950500-SI0
D0G-3010510-I05

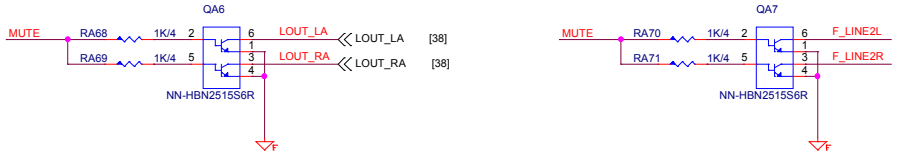


Rear Line OUT De-POP circuit

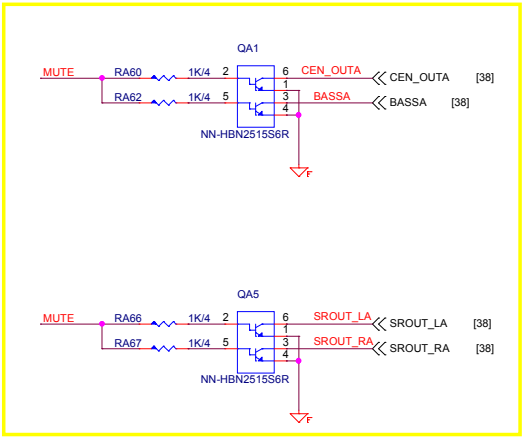
(De-pop circuit for Rear Line out & Front Headphone out)



Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



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	MS-7B58..	
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Audio moat is transparent and width 40mil

[37] COM1
[37] COM2
[37] COM3
[37] COM4
[37] COM5
[37] COM6
[37] COM7
[37] COM8

[37,40] PWM2_R
[37,40] PWM2_G
[37,40] PWM2_B

R1213 220R/8
R1883 220R/8
R1884 220R/8
AUD_R_LED
[37,40] PWM2_R
Q310
N-QM3010K_SOT23-3-HF

R1151 100R/8
R1154 100R/8
R1153 100R/8
AUD_G_LED
[37,40] PWM2_G
Q311
N-QM3010K_SOT23-3-HF

R1147 150R/8
R1150 150R/8
R1149 150R/8
AUD_B_LED
[37,40] PWM2_B
Q312
N-QM3010K_SOT23-3-HF

AUDLED1
Q206 PA002FMG
LED_VCC5
LED_VCC5_A1
COM1
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED2
Q299 PA002FMG
LED_VCC5
LED_VCC5_A2
COM2
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED3
Q300 PA002FMG
LED_VCC5
LED_VCC5_A3
COM3
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED4
Q301 PA002FMG
LED_VCC5
LED_VCC5_A4
COM4
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED5
Q302 PA002FMG
LED_VCC5
LED_VCC5_A5
COM5
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED6
Q303 PA002FMG
LED_VCC5
LED_VCC5_A6
COM6
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED7
Q304 PA002FMG
LED_VCC5
LED_VCC5_A7
COM7
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

AUDLED8
Q305 PA002FMG
LED_VCC5
LED_VCC5_A8
COM8
AUD_G_LED
AUD_B_LED
AUD_R_LED
LED04-W#-20mA2.3V_3215-RH

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Z370 Modify;Add 0ohm R1887

U3

LPC Interface

DSW Interface

Printer mode

Port80 LED Control

GPIO

UART SIR

Harddware Monitor

KBC Function

FAN Control

ACPI Function

Power Pin

6793D-M/colay 6795

IF INTEL DSW ENABLE
Other unused pin can be other function
(EX:GPIO)

Closed PIN99 Closed PIN24,108 Closed PIN46,85

Z370 modify

SLP_SUS Co-lay circuit

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

3V Analog Power

Intel
6793 pull down
6795 pull down

6793 DDR4_EN strapping
6795 ESPI_EN strapping

Intel
6793 pull high
6795 LPC pull down/ESPI pull high

ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER

6793 Test point
6795 DDR4_EN strapping

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HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

VCC_DDR R592 10K1% VDIMM → VDIMM [41]
R580 10K1%
C438 10u6.3X6

VCORE R574 10K1% CPUVCORE → CPUVCORE
R573 X_10K1%
C431 10u6.3X6

+12V R591 220K1% VIN0 → VIN0 [41]
R589 20K1%
C446 0.1u16X4

VCC5 R590 12K1% VIN1 → VIN1 [41]
R588 3K1%
C445 0.1u16X4

PCH_1VSB R595 10K1% VIN2 → VIN2 [41]
C476 10u6.3X6

BIOS REQUEST FROM VIN2 POWER FAULT DISABLE.

VCCIO R564 10K1% VIN4 → VIN4 [41]
C408 10u6.3X6

VGT R551 10K1% VIN6 → VIN6 [41]
C400 10u6.3X6

VCCSA R552 10K1% VIN5 → VIN5 [41]
C401 10u6.3X6

VCC_DDR → VCC_DDR_TP
VCORE [41] → VCORE_TP
PCH_1VSB → PCH_1VSB_TP
VCCIO → VCCIO_TP
VGT → VGT_TP
VCCSA → VCCSA_TP

SERIAL PORT 1

Z370 Modify;PM Spec change

Thermal Monitor

HM_VREF → HM_VREF [41]
R587 X_10K/1%/4
SYSTIN → SYSTIN [41]
Q67 P-3906 (E, B, C)
RT2 X_10KRT1%4
C416 2.2n50X
GNDHM → GNDHM [41]

HM_VREF
R750 10K1%4
CPUTIN → CPUTIN [41]
RT3 10KRT1%4
C861 0.1u16X4
GNDHM

Debug LED

Placement
POST2 POST1

Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

Debug LED OFF BIOS control

[41,42] LED_A R449 220R/4 H0_LED_A
LED_B R470 220R/4 H0_LED_B
LED_C R451 220R/4 H0_LED_C
LED_D R455 220R/4 H0_LED_D
LED_E R456 220R/4 H0_LED_E
LED_F R457 220R/4 H0_LED_F
LED_G R450 220R/4 H0_LED_G

[41,42] LED_A R504 220R/4 L0_LED_A
LED_B R604 220R/4 L0_LED_B
LED_C R560 220R/4 L0_LED_C
LED_D R561 220R/4 L0_LED_D
LED_E R602 220R/4 L0_LED_E
LED_F R601 220R/4 L0_LED_F
LED_G R516 220R/4 L0_LED_G

H0_LED_A..G → POST2 (a b c d e f g DP) LED06-R-7SEG-RH-1
L_DGH_0# → C1# C2#

L0_LED_A..G → POST1 (a b c d e f g DP) LED06-R-7SEG-RH-1
L_DGL_0# → C1# C2#

SIO_3VA R458 X_10K DGH_0# R459 0R L_DGH_0#
[41] DGH_0#

SIO_3VA R466 X_10K DGL_0# R467 0R L_DGL_0#
[41] DGL_0#

PLTRST

[41] PLTRST_BU1#_R R1504 22R1% PLTRST_BU1# R1109 100R1% PLTRST_BU1#_LAN → PLTRST_BU1# [27], PLTRST_BU1#_LAN [34]

[41] PLTRST_BU3#_R R1501 22R1% PLTRST_BU3# R1110 100R1% PLTRST_BU3#_M2_1 → PLTRST_BU3#_M2_1 [24]
PLTRST_BU3# R1112 100R1% PLTRST_BU3#_M2_2 → PLTRST_BU3#_M2_2 [25]
Delete U2
PLTRST_BU3# R1108 100R1% PLTRST_BU3#_TPM → PLTRST_BU3#_TPM [50]

VCC3
PCH Side RSVD Pull high to 3VSB.
[15] GPP_F22 → U139 (X_NC7SZ08M5X) C1130 X_0.1u16X4
PE_RESET_N R635 100R1% PLTRST_BU2#_PCIE1 → PLTRST_BU2#_PCIE1 [20]

[41] PLTRST_BU2#_R R1503 22R1% PLTRST_BU2#
R701 0R
R700 100R1% PLTRST_BU2#_PCIE2 → PLTRST_BU2#_PCIE2 [22]
R703 100R1% PLTRST_BU2#_PCIE4 → PLTRST_BU2#_PCIE4 [21]
R1105 100R1% PLTRST_BU2#_PCIE3 → PLTRST_BU2#_PCIE3 [22]
R1113 100R1% PLTRST_BU2#_PCIE5 → PLTRST_BU2#_PCIE5 [22]
R1114 100R1% PLTRST_BU2#_PCIE6 → PLTRST_BU2#_PCIE6 [21]

SIO / PCH / JSPI / CLK GEN

SIO SIO_RSMRST# R782 RSMRST# → PCH
R783 SIO_RSMRST#_SPI → JSPI

SIO DPWROK_SIO R566 SIO_DPWROK R776 PCH_DPWROK → PCH
R781 SIO_DPWROK → JSPI

SIO SIO_INFOBTN# R626 CHIP_PWGD R517 CHIP_PWGD_R → PCH
SIO_PWROK R663 R471 CHIP_PWGD_Q60 → Q60
R784 CHIP_PWGD_SPI → JSPI
R665 CHIP_PWGD_IDT → CLK GEN

PCH SLP_S3#_R R751 SLP_S3# → To Other
R752 SIO_SLP_S3# → SIO

PCH SLP_S4#_R R758 SLP_S4# → To Other
R757 SIO_SLP_S4# → SIO

For Signals Monotonic

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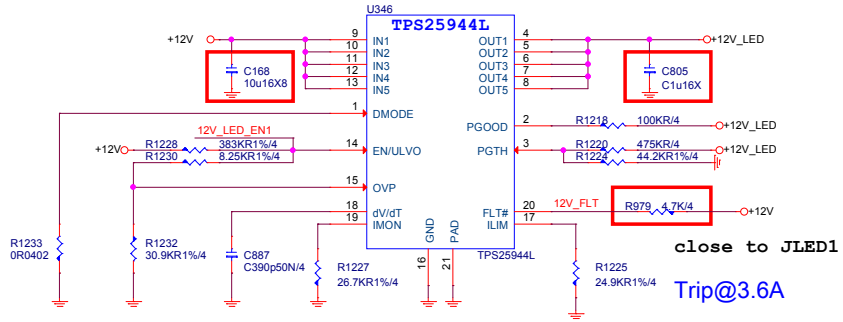
LED Control by SIO

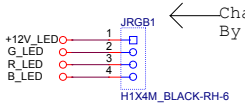
2016.07.06 Use TPS25944L

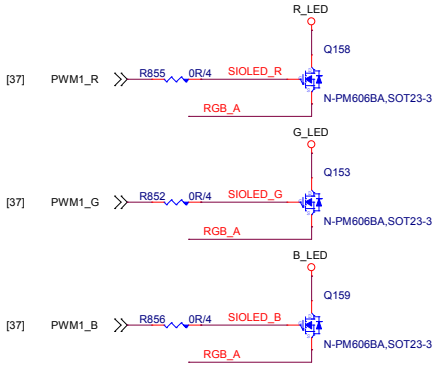


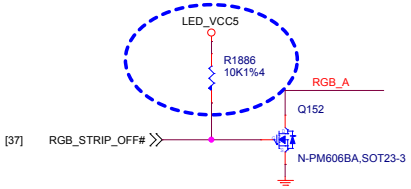
close to JLED1

Trip@3.6A

Change location to JRGB1 form JLED1
By PM request

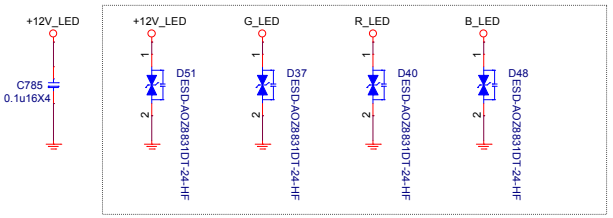


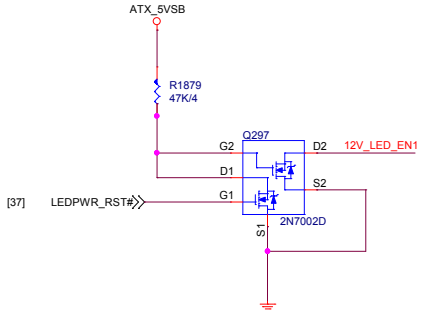




2016.07.06 only reserve now

close to JLED1





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Size: Custom	Document Description: SIO-NTC6792D-2	Rev: 10
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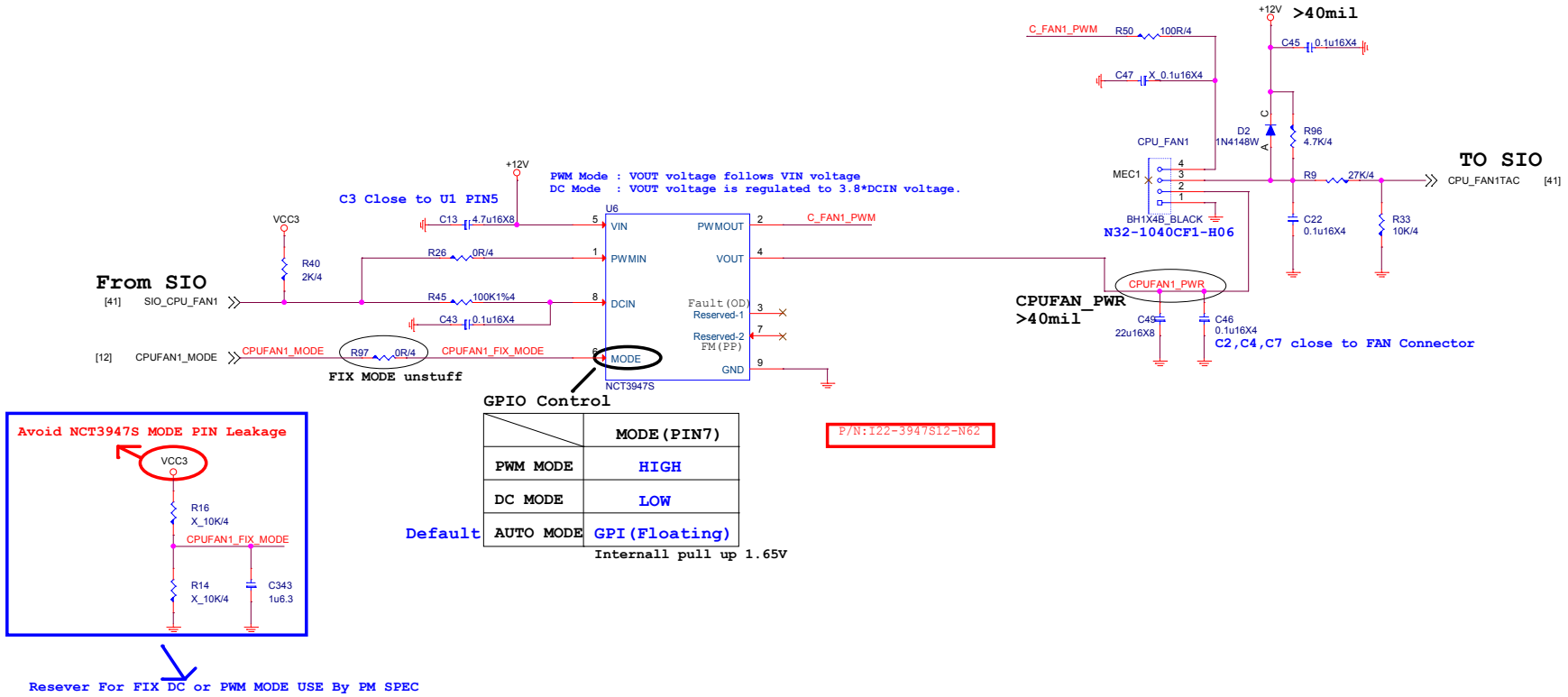
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU FAN1	Rev: 10
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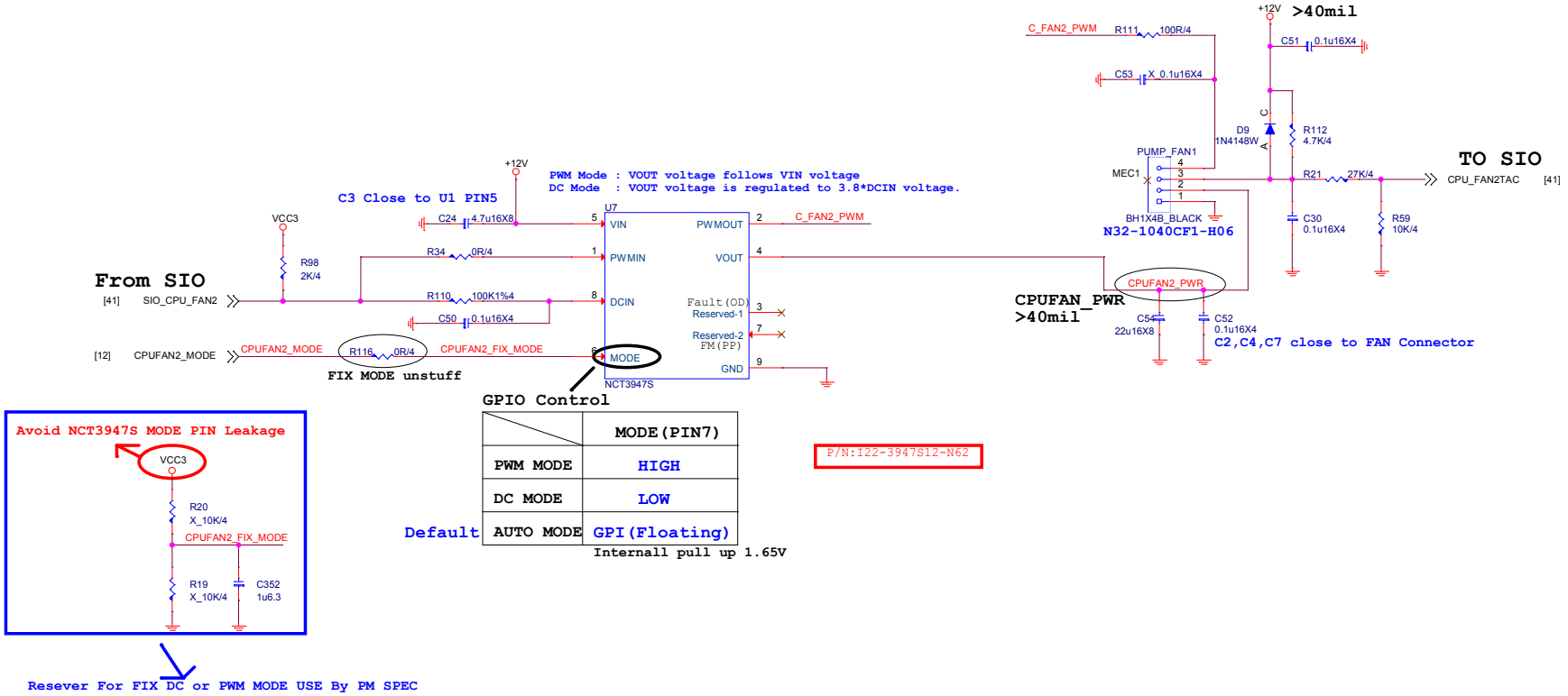
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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Size: Custom	Document Description: CPU FAN2	Rev: 10
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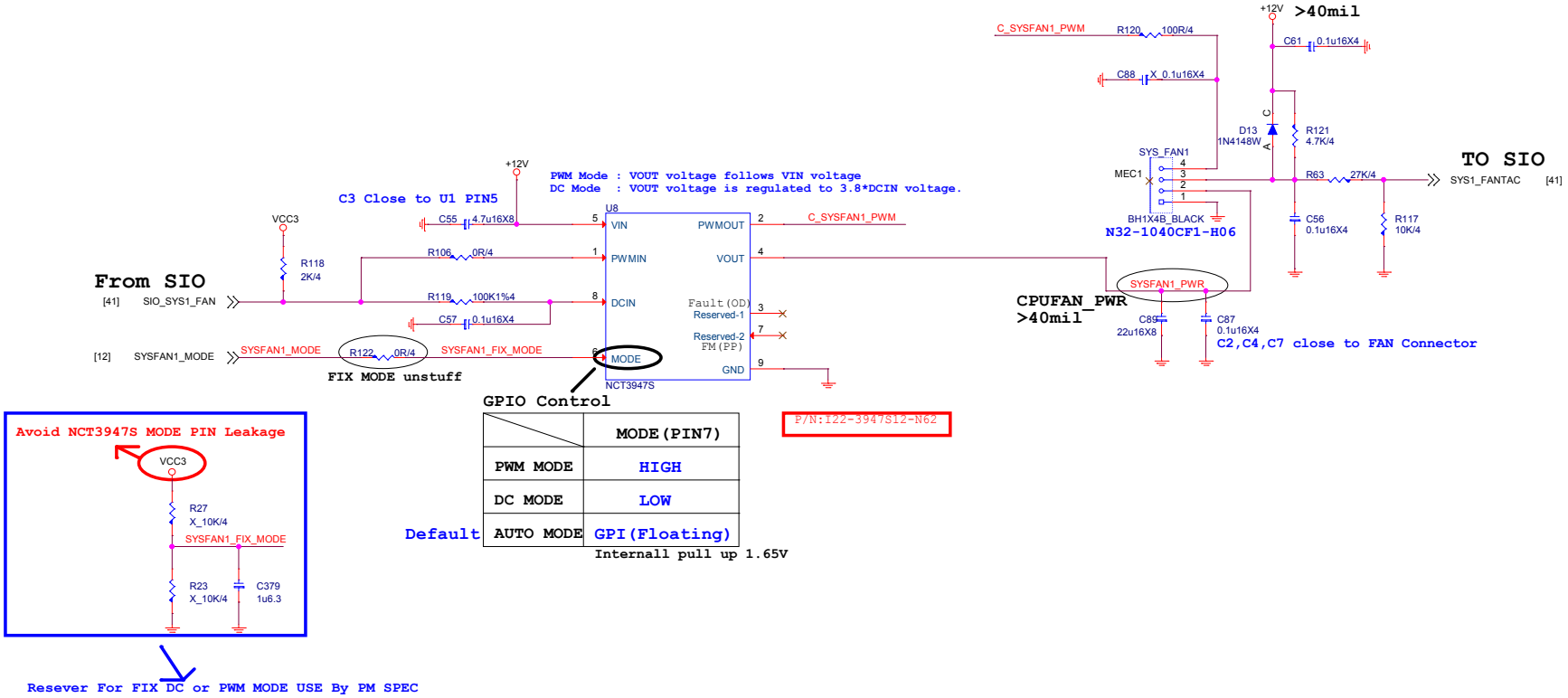
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切換 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Size: Custom | Document Description: SYSTEM FAN1 | Rev: 10

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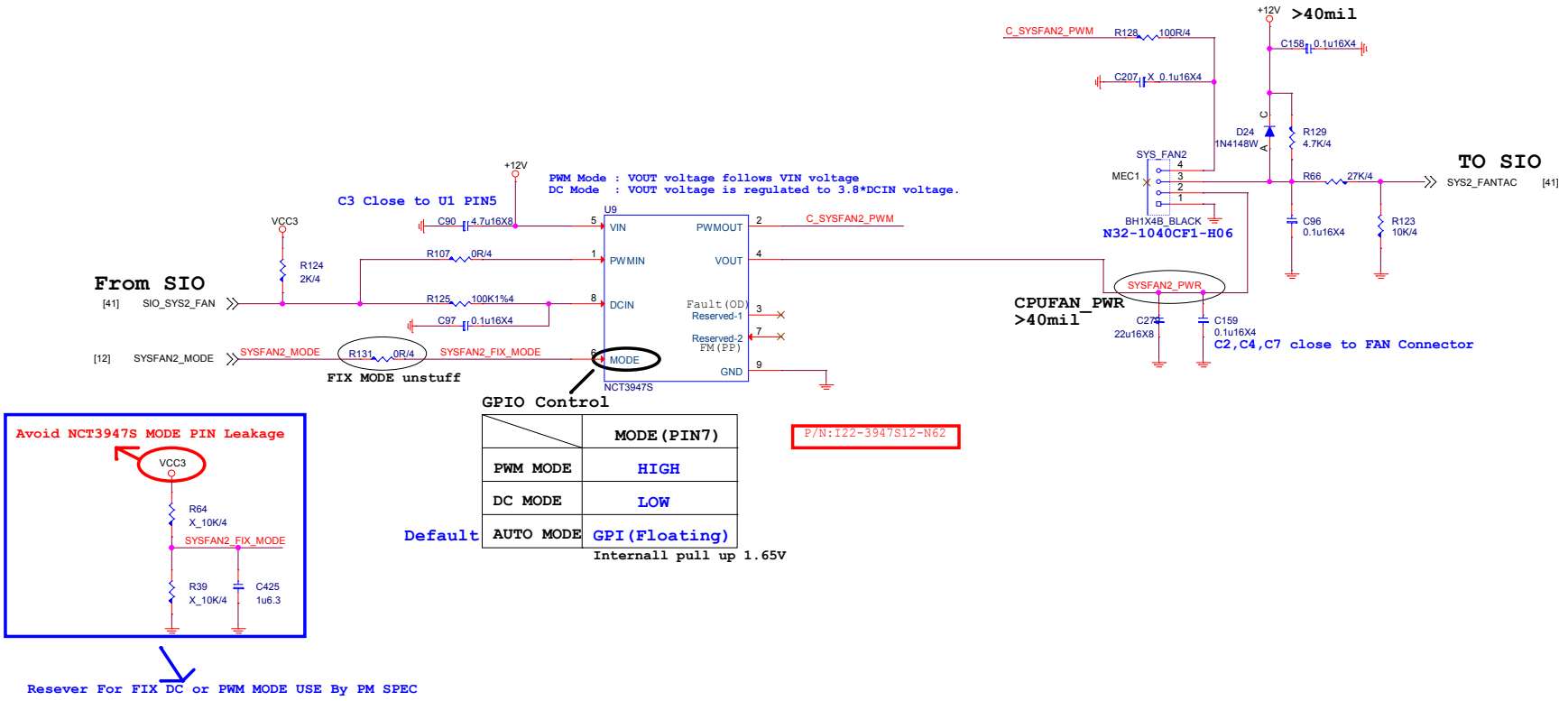
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



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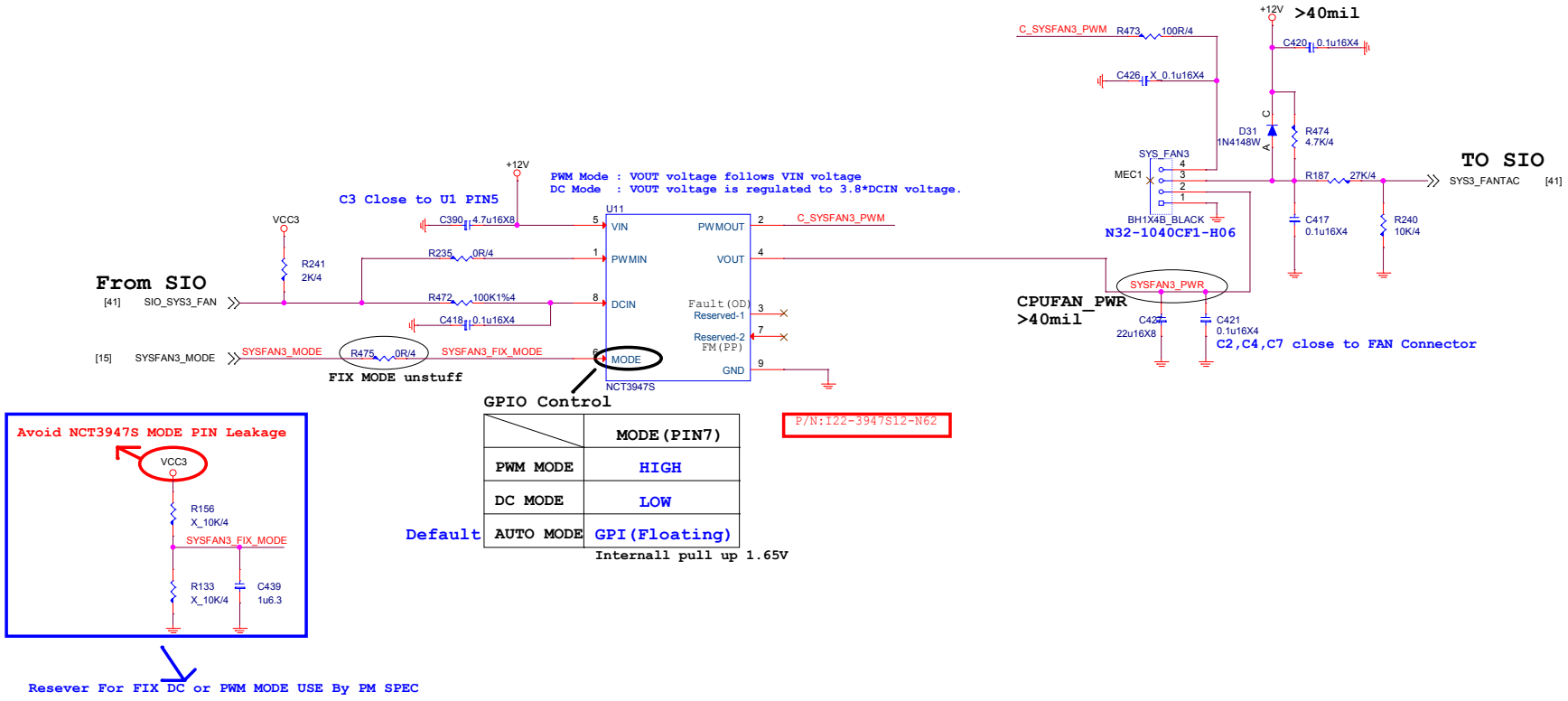
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Size: Custom | Document Description: SYSTEM FAN3 | Rev: 10

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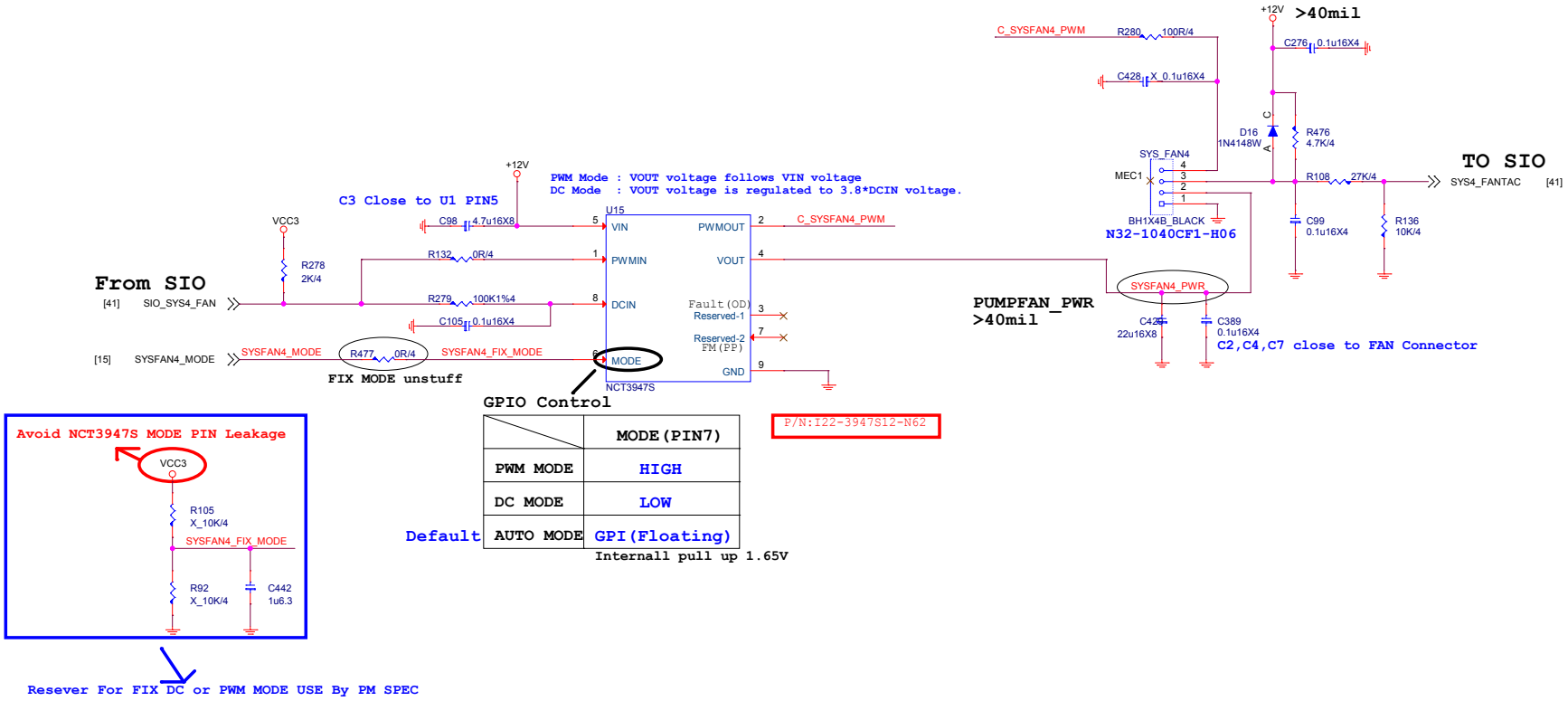
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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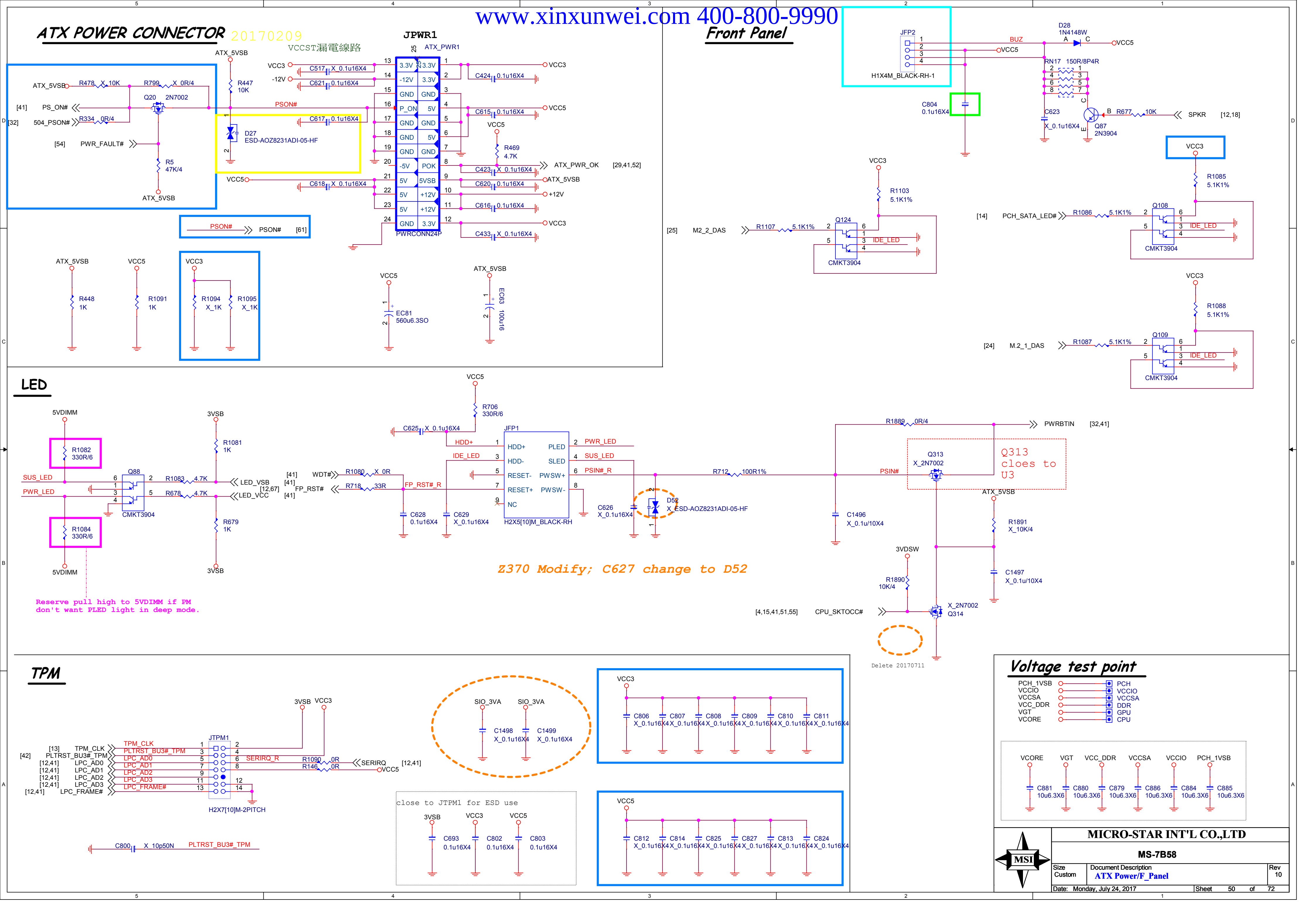

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ATX POWER CONNECTOR
20170209
VCCST漏電線路
JPWR1
ATX_PWR1
PWRCONN24P
Front Panel
JFP2
H1X4M_BLACK-RH-1
D28 1N4148W
RN17 150R/8P4R
Q87 2N3904
SPKR
PCH_SATA_LED#
M2_2_DAS
M.2_1_DAS
CMKT3904
IDE_LED
ATX_PWR_OK
PSON#
D27 ESD-AOZ8231ADI-05-HF
Q20 2N7002
LED
Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.
JFP1
H2X5[10]M_BLACK-RH
Z370 Modify; C627 change to D52
Q313 cloes to U3
PWRBTIN
CPU_SKTOCC#
Delete 20170711
TPM
JTPM1
H2X7[10]M-2PITCH
close to JTPM1 for ESD use
Voltage test point
PCH_1VSB
VCCIO
VCCSA
VCC_DDR
VGT
VCORE
MICRO-STAR INT'L CO.,LTD
MS-7B58
Document Description
ATX Power/F_Panel
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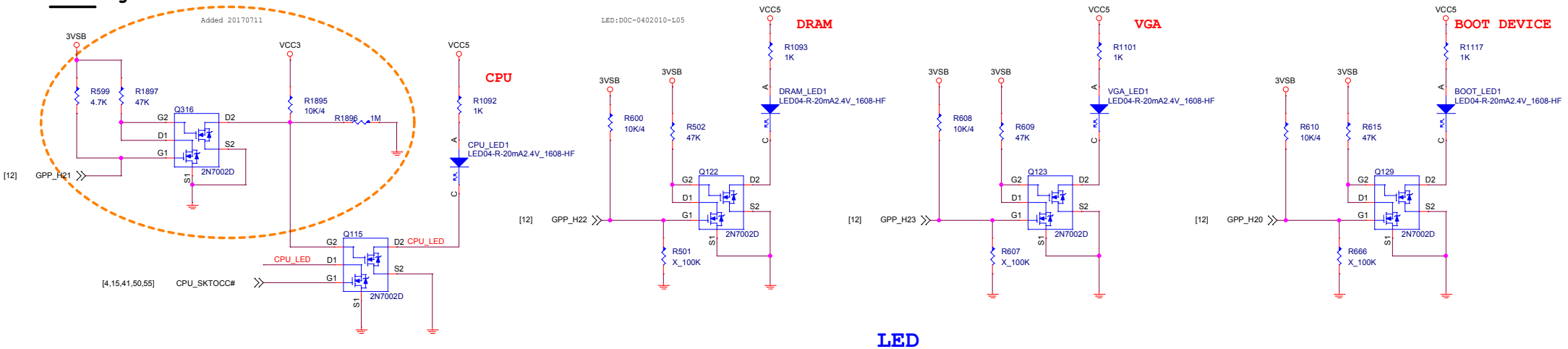
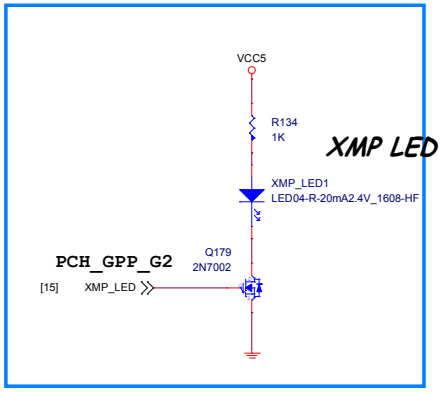
EZ Debug LED



LED
紅 : D0C-040P100-H91

GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



LED
紅 : D0C-040P100-H91

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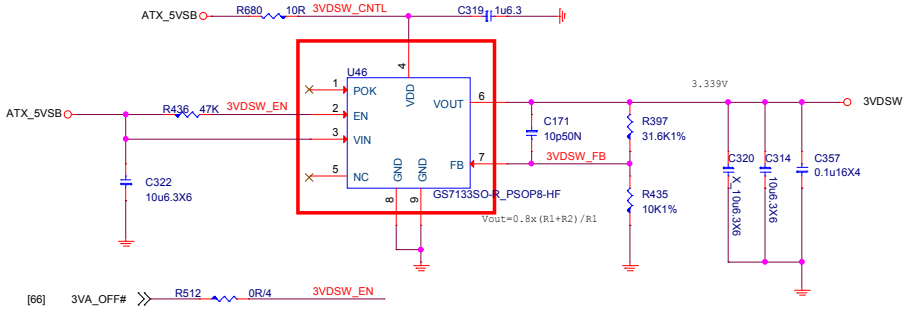
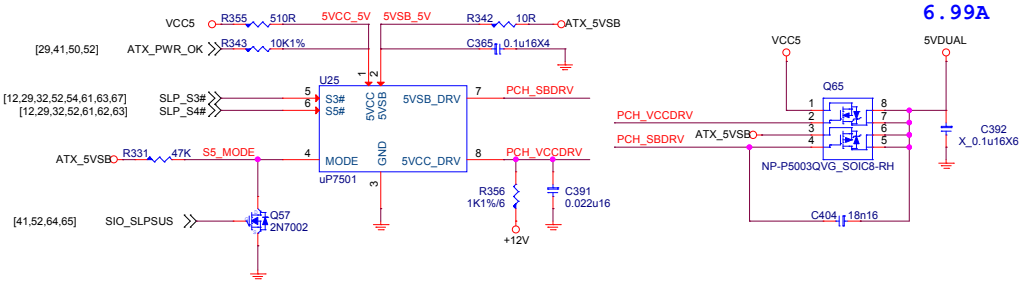
3VDSW



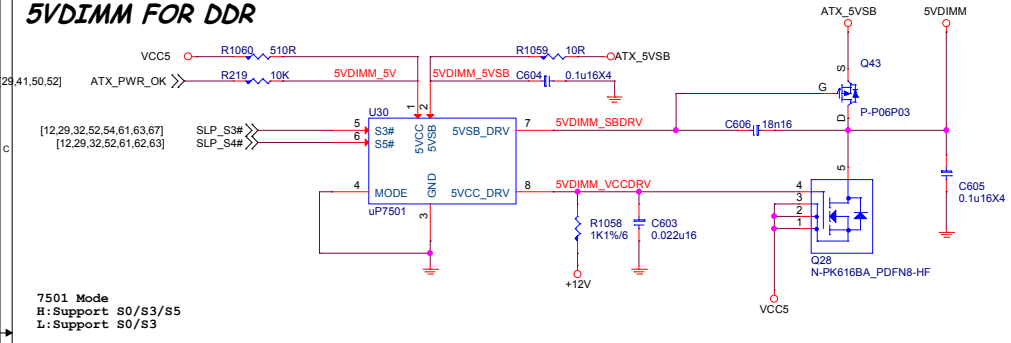
5VDUAL

5VDUAL is power source of 1P0SB

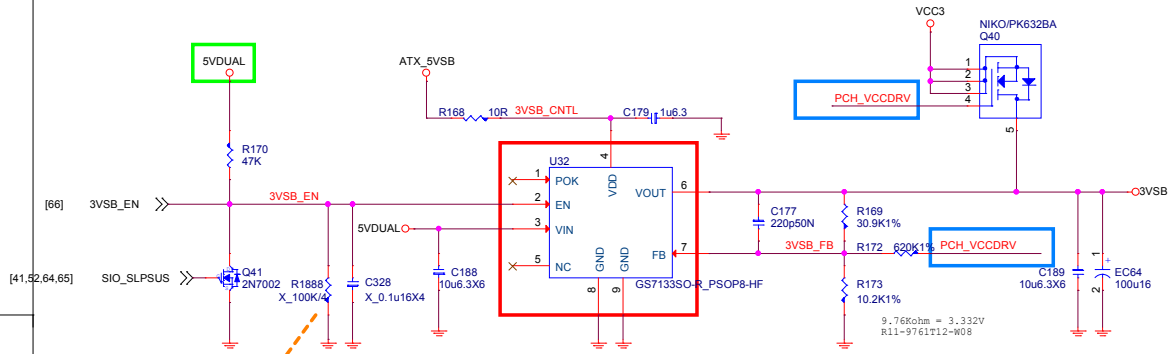
6.99A



5VDIMM FOR DDR

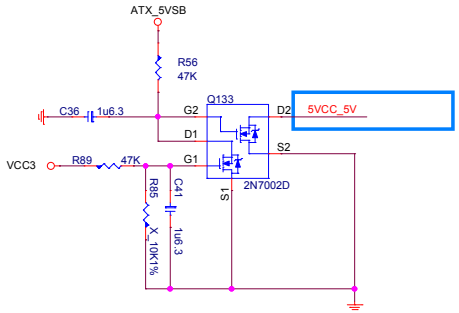


3VSB cost down



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

Z370 Modify; Add Delay



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Size: Custom	Document Description: ACPI UPI	Rev: 10
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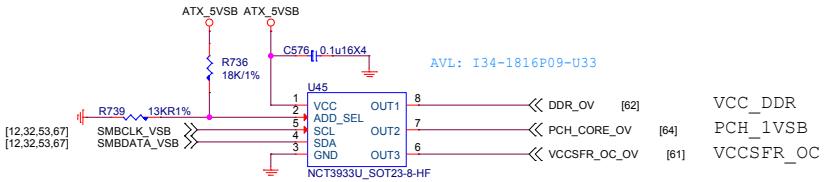
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

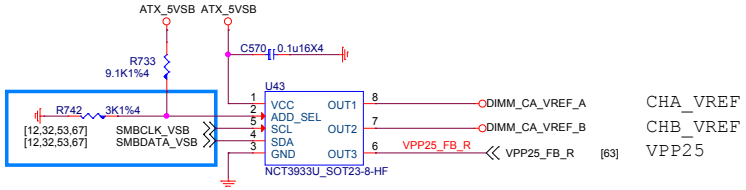
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



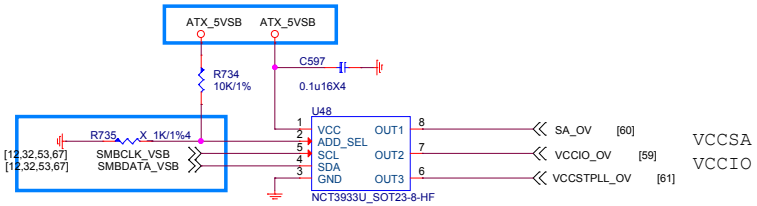
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



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Custom	OV-NCT3933/GPIO-NCT5605	10

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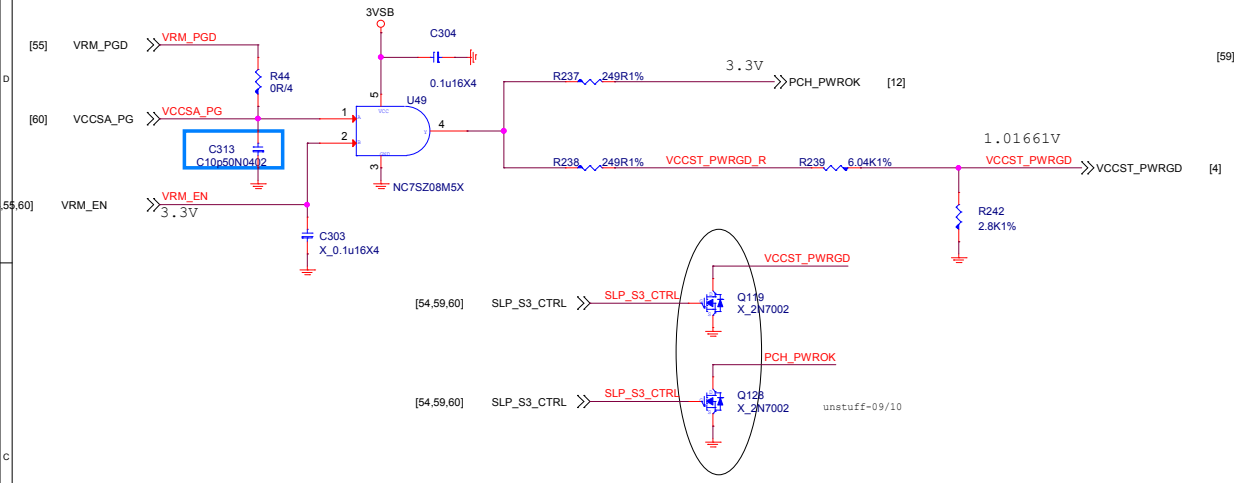
PCH_PWROK Control from VCCIO_PG&VCCSA

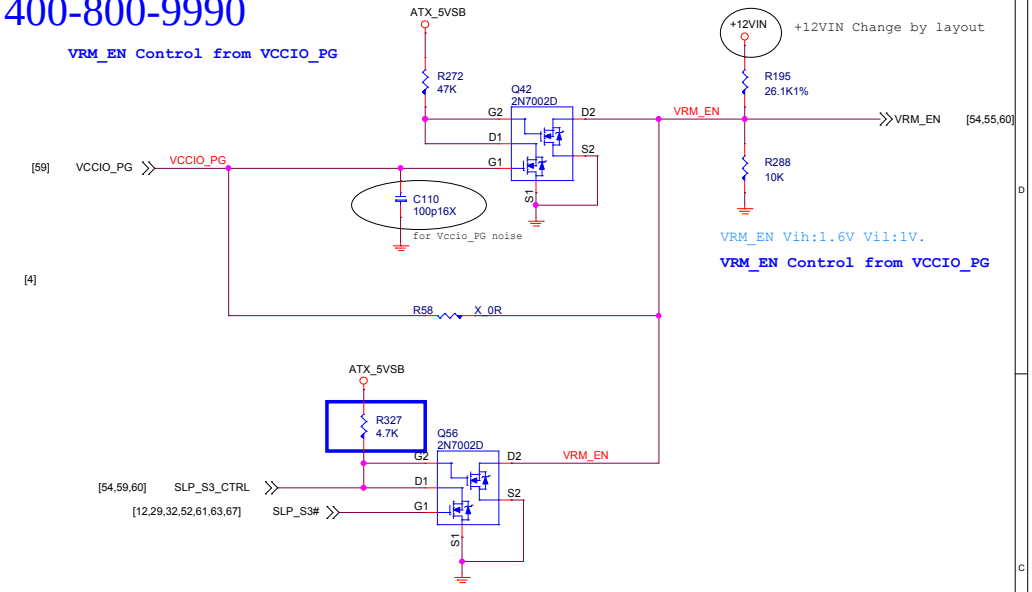
VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA

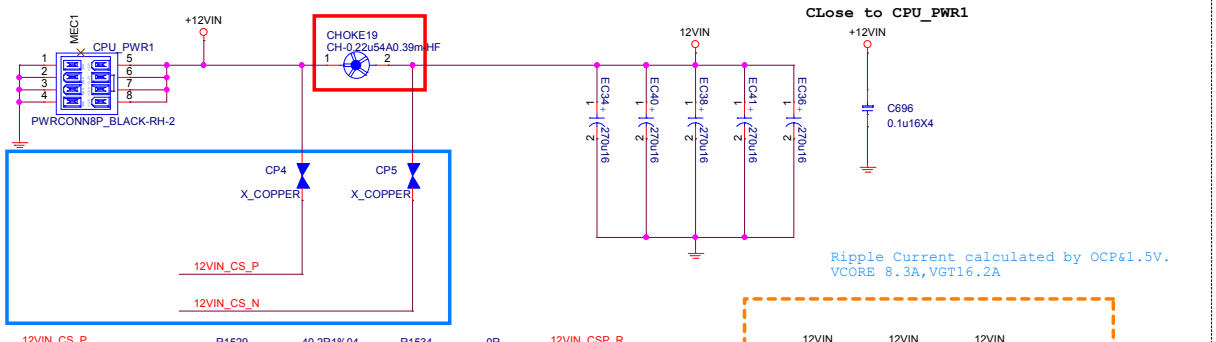
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



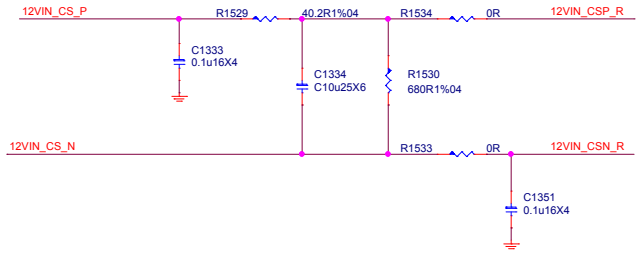
VRM_EN Control from VCCIO_PG

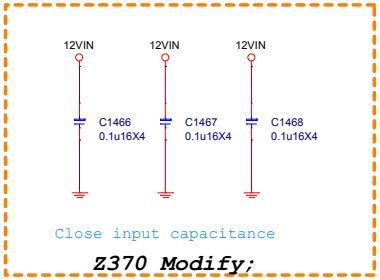


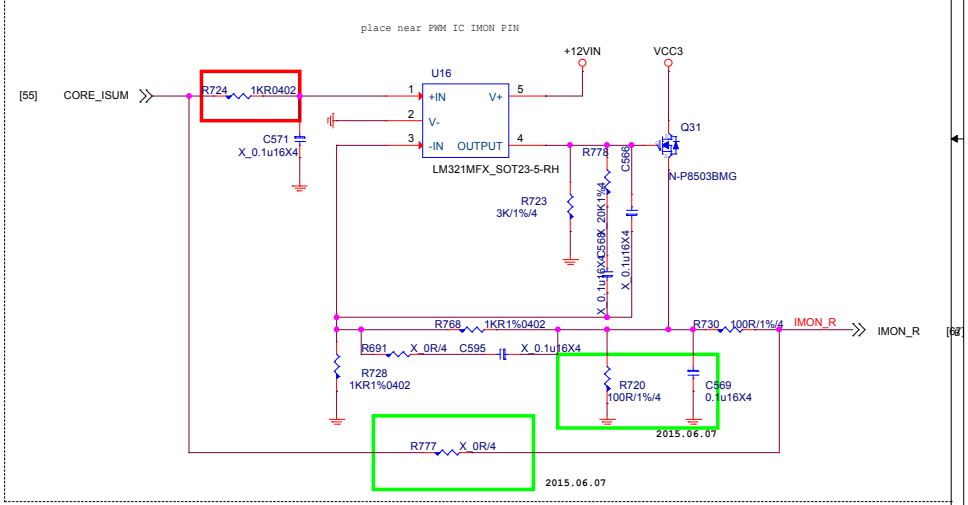
CLose to CPU_PWR1

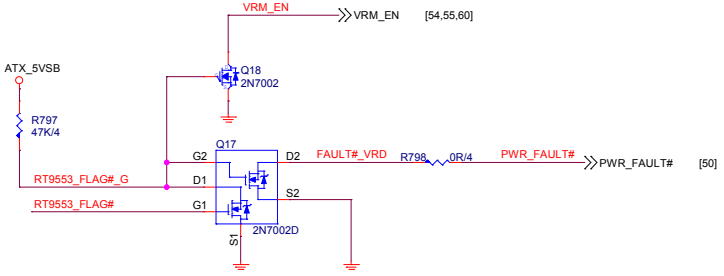


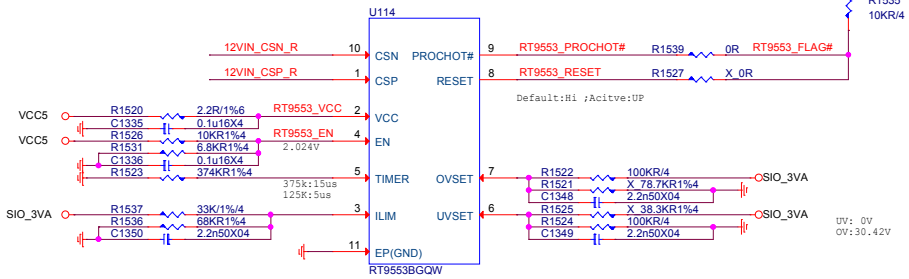
Ripple Current calculated by OCP&1.5V.
VCORE 8.3A,VGT16.2A











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Custom	Rear I/O PS2	10

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Vcore: ICC Max 138A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A

VU1 change to I32-9508Q0C-U33.

Close IC

VR13=45.3K,for VGT ICCMAX=45.3A.
VR17=140K,for VCORE ICCMAX=140A.

PROG1: For 4+1 Setting
PROG2: Vboot 0V~SMBUS Adress 8Ah.
PROG3: For Phase Extension Enable.

SMBus address=8Ah
VR32=16.5K,R225=38.3K,Vboot:1.05V.
VR32=16.5K,R225 unstuff,Vboot 0V.

Diff pair

Diff pair

Close Phase1 CHOKE

Close Phase1 MOS

[(39.2+2)/154]*100=26.75Kohm

Close Phase2 CHOKE

Close Phase2 MOS

[(30+0.68)/58]*48=25.39Kohm

20170216

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Size: Custom	Document Description: PWM-UP9508 VCORE+VGT
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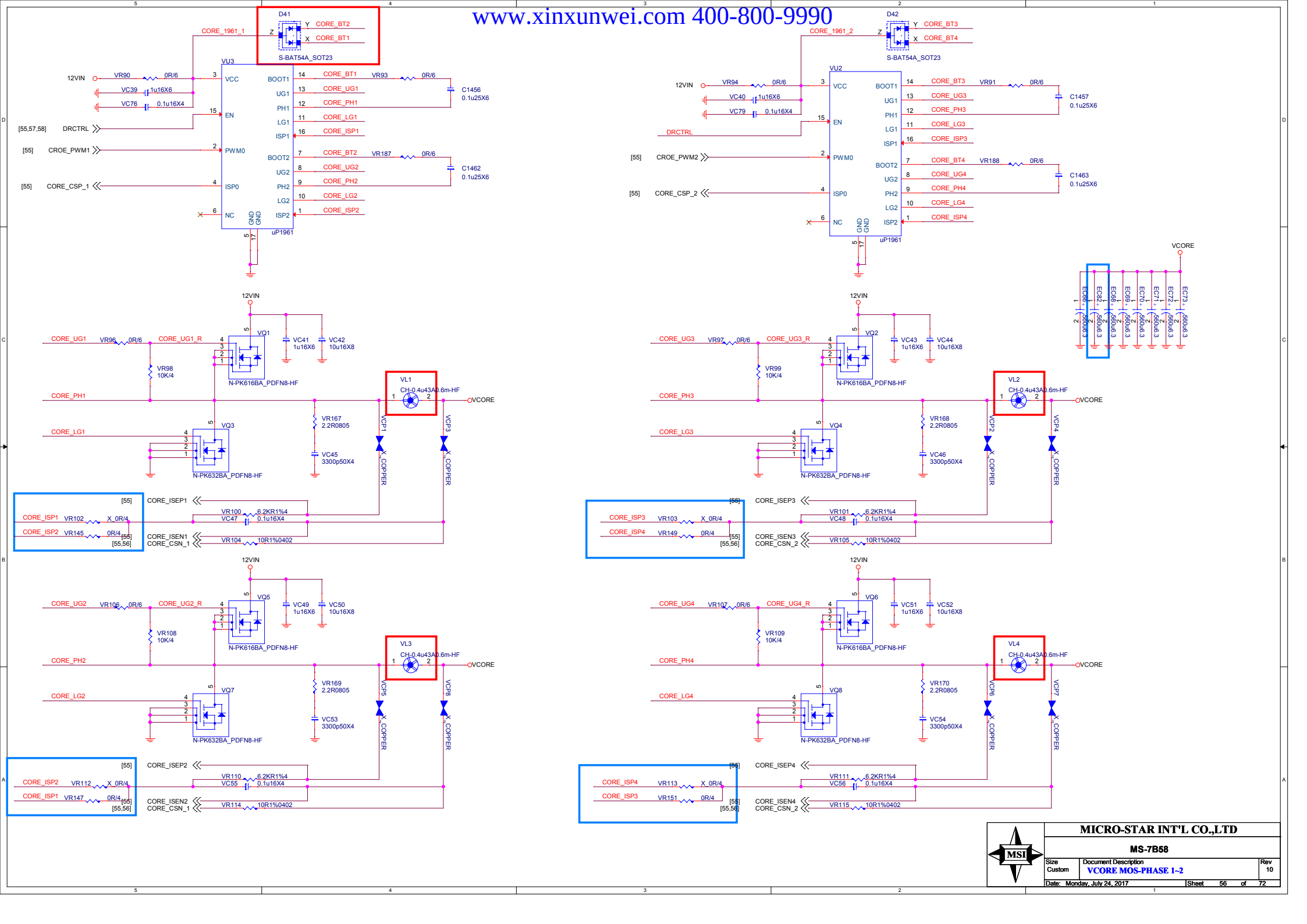

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Size	Document Description	Rev
Custom	VCORE MOS-PHASE 1~2	10

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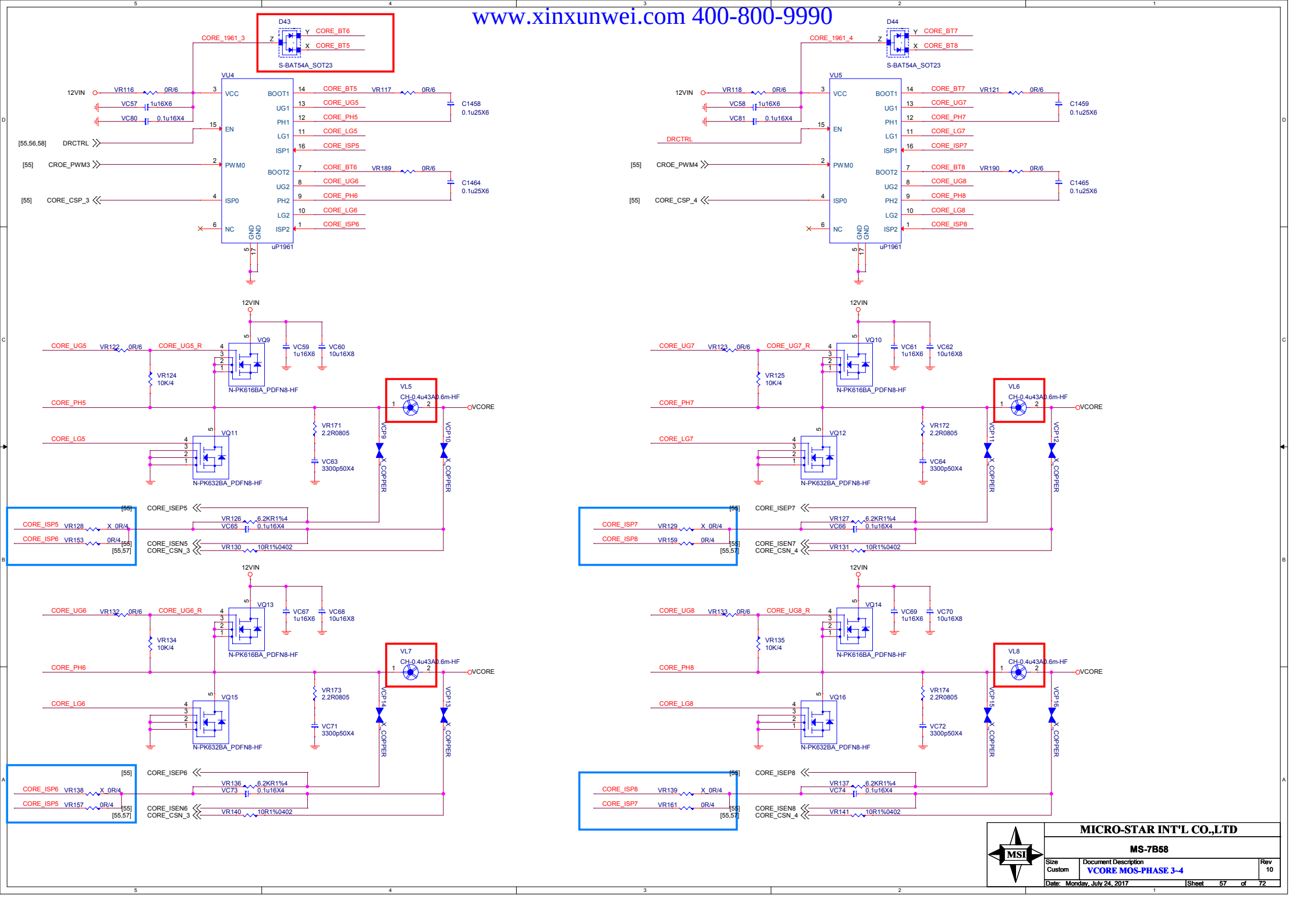

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Size	Document Description	Rev
Custom	VCORE MOS-PHASE 3-4	10

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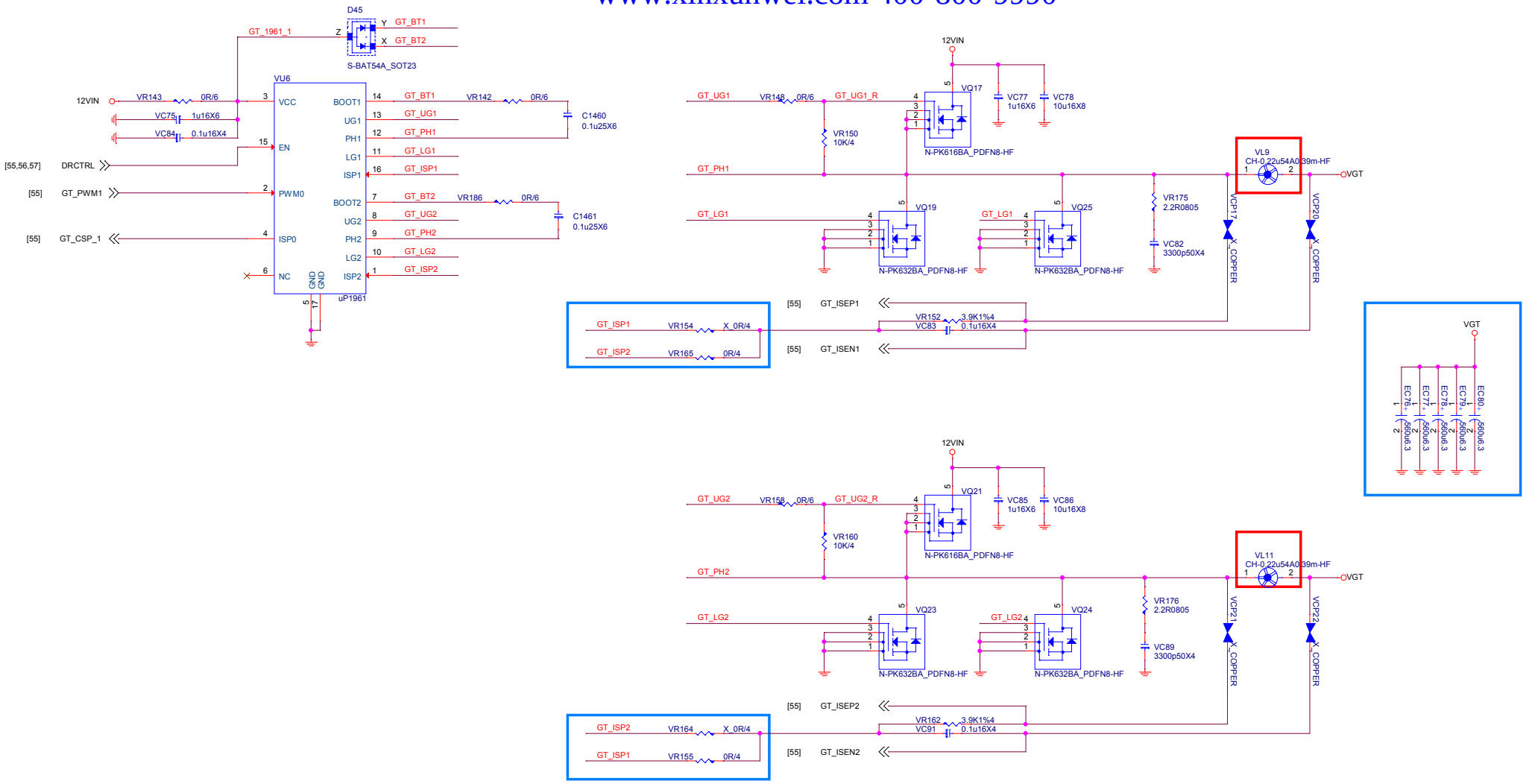

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Size: Custom	Document Description: VGT MOS-PHASE 1~2	Rev: 10
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VCCIO

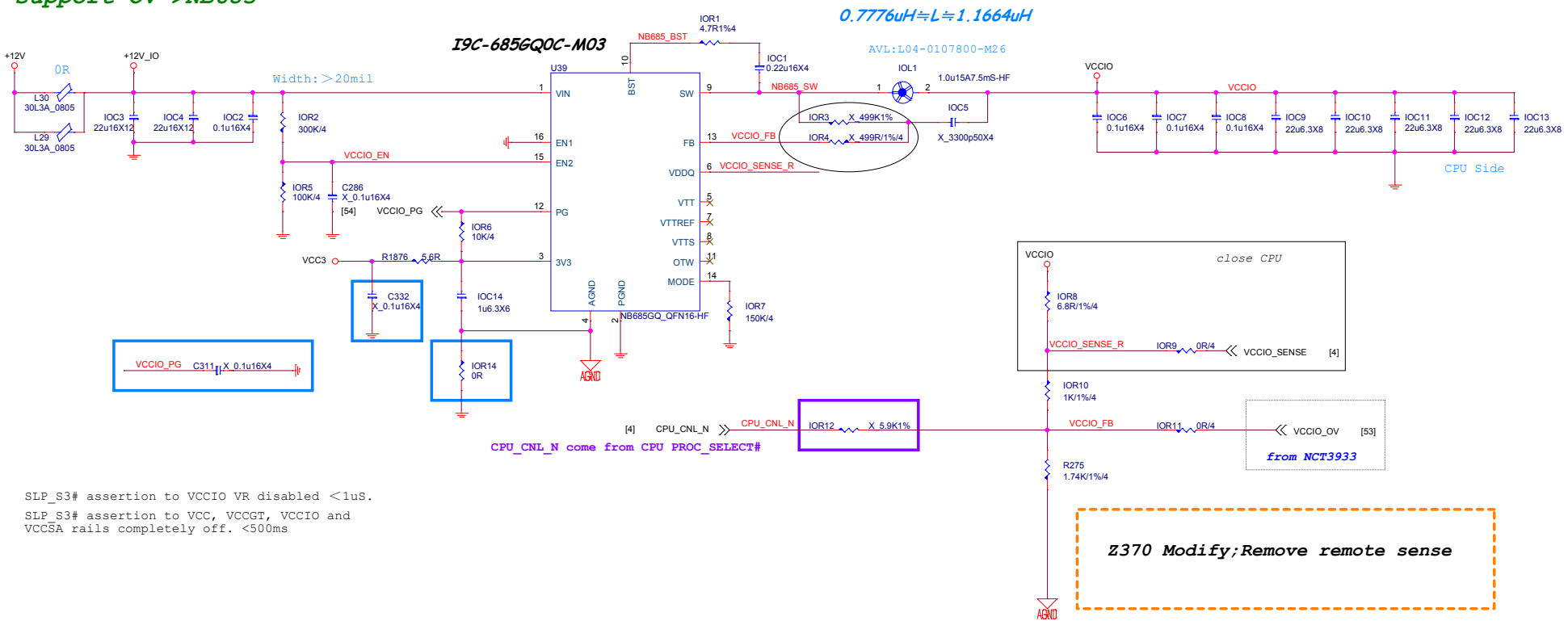
0.95V; 5.5A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685

I9C-685GQ0C-M03

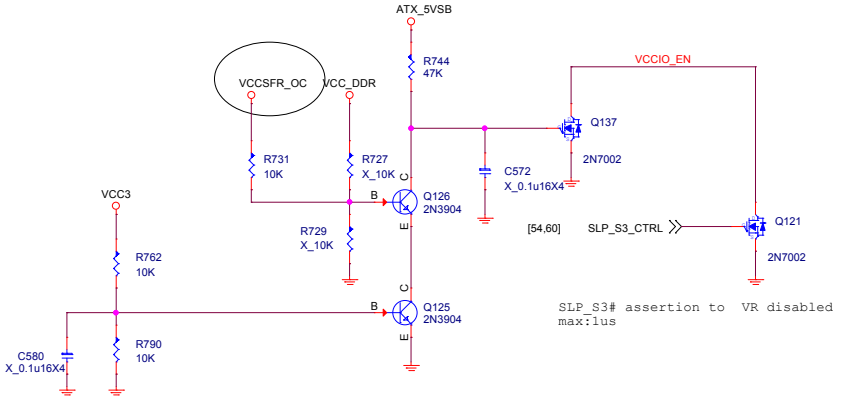
0.7776uH≒L≒1.1664uH



SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms

Z370 Modify;Remove remote sense



SLP_S3# assertion to VR disabled max:1us

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SA Power:1.05V,11.1A

*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.3mohm]/10uA*
=15.54(3.3)mohm/10uA*
=5.1282Kohm

Rocs:5.23K,OCP:
D03-632BA0C-N03 : 15.848A

Rdson(low)10V

D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

2014.08.25 update

EN:VIH2.4V
EN pin Maximum:6.5V

U4 RT8125EGQW_WDFN10-HF

FB:0.8V

Add R1885

Z370 Modify;Remove remote sense
delete VSA_IO_VSS_SENSE

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 18* 0.2825
= 5.086A

Pull up by layout&Check level

VRM_EN線路update

EN:VIH2.4V
EN pin Maximum:6.5V

EN:VIH2.4V
EN pin Maximum:6.5V

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

Change to 1206 package

1.05V,11.1A

P/N:L04-01073F0-M26

snubber

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

2014.12.25
for up1540:R417 no stuff

Signals reference +12V.

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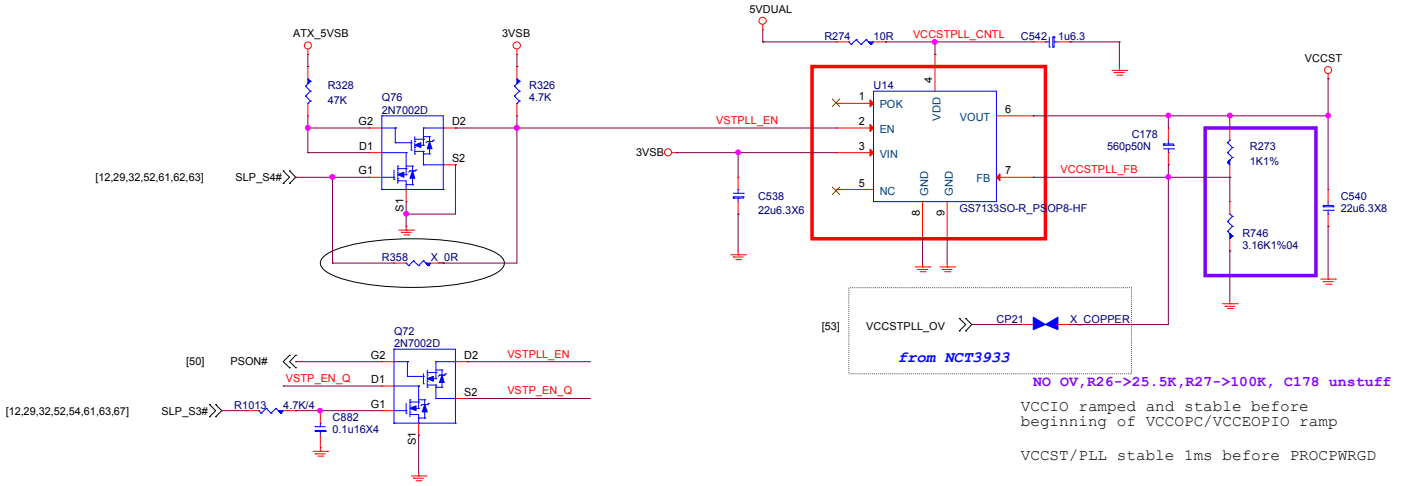
VCCST

for Gaming3/5, Classic, ECO and H110

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



NO OV,R26->25.5K,R27->100K, C178 unstuff

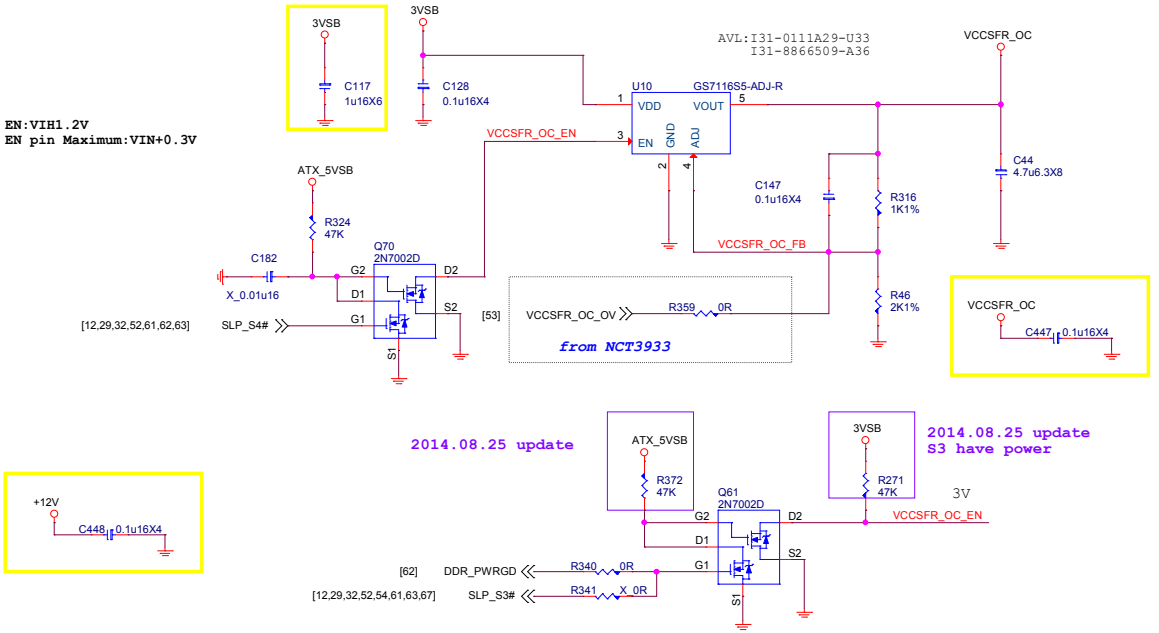
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update

2014.08.25 update
S3 have power

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Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 10
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DDR4_1.2V 2.8A+9.2A+1.2A=13.2A

3.3A FOR CPU

9.2A FOR 4DIMM

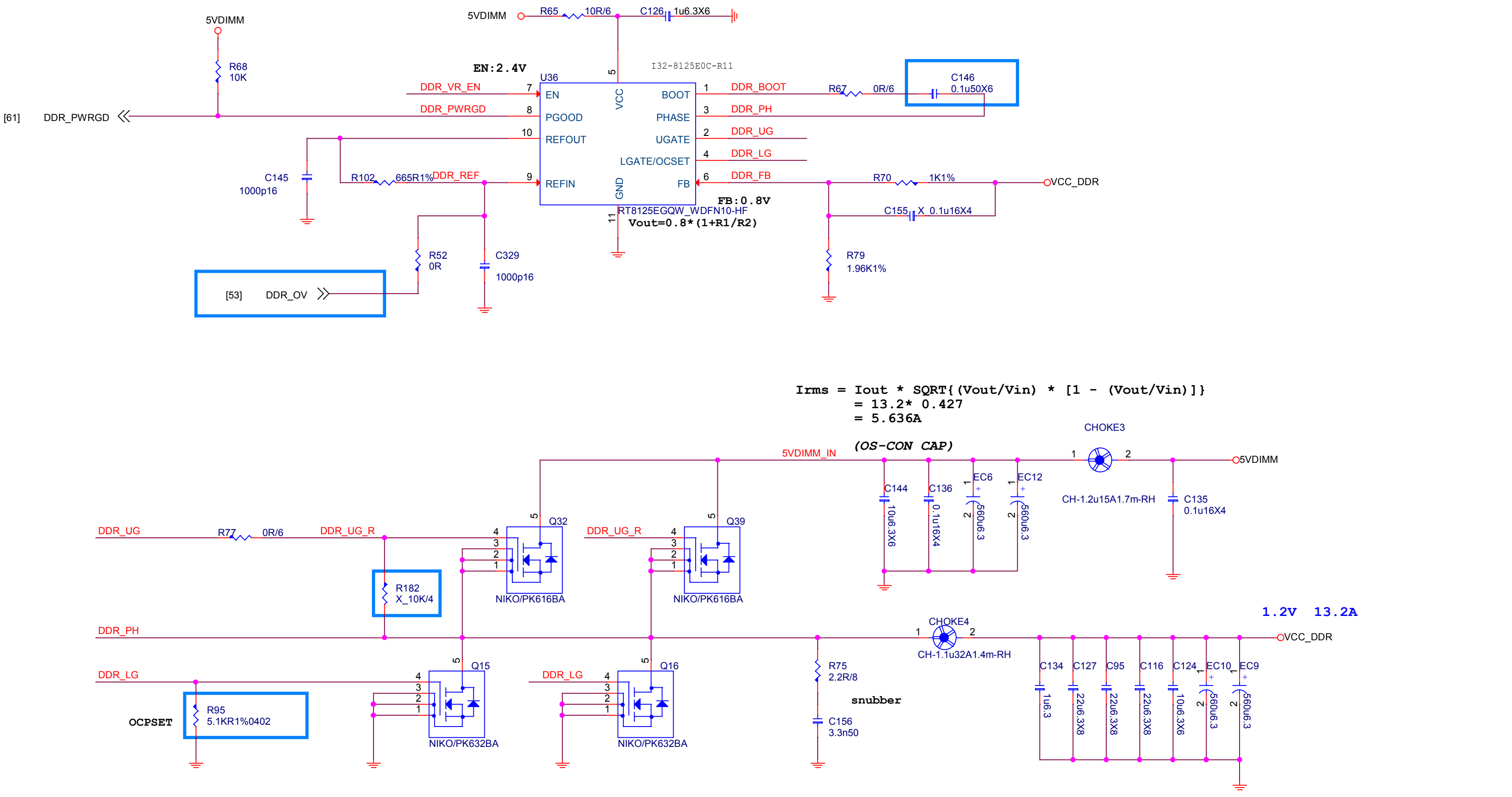
1.2A FOR DDR VTT

*OCP =13.2A*1.5=19.8A*
Rocs(R3)=OCP[Rdson(Low side)/2]/10uA*
=19.8A(4.6/2)mohm/10uA*
=4.554Kohm < 5K ohm

Rocpset:5.1K
OCP=Rocset/[Rdson(Low side)/2]*10uA
=5.1K/2.3mohm*10uA
=22.1A

Rdson(low)4.5V

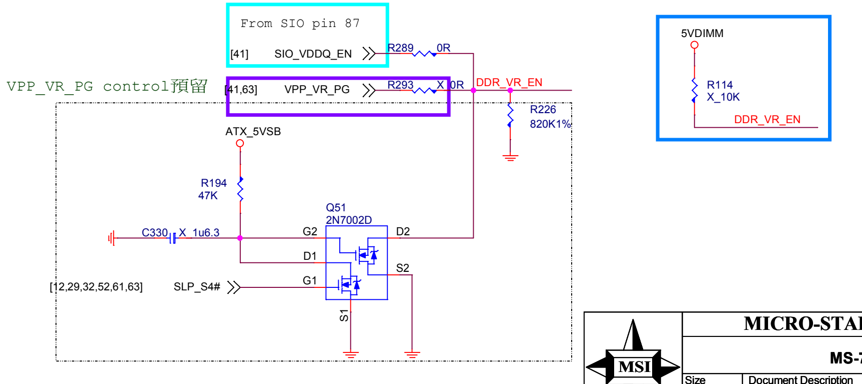
D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



Datasheet?:Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

CAP ESR?:0.2432uH≒ L ≒1.2897uH

2014.12.17 update



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MS-7B58			
Size: Custom	Document Description: DDR4 Power-RT8125C		Rev: 10
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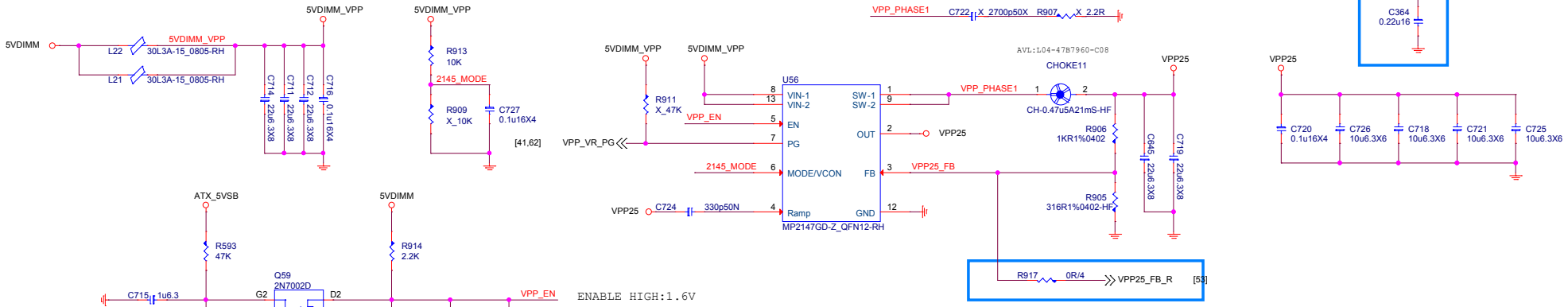
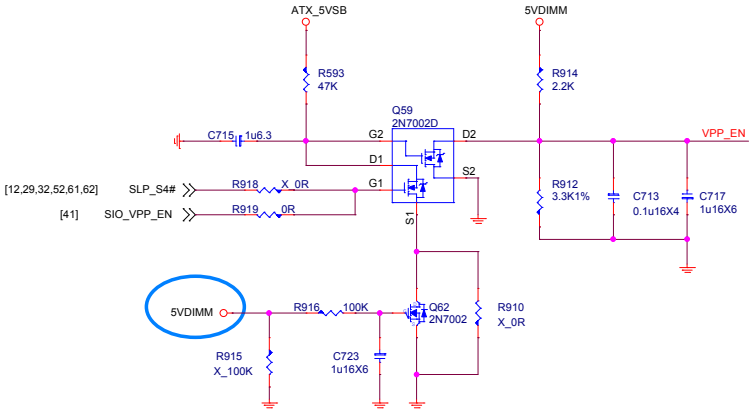
4DIMM :2.84A FOR DDR VPP2.5V

www.xinxunwei.com 400-800-9990

VPP25 Power

2.5V; 2.24A

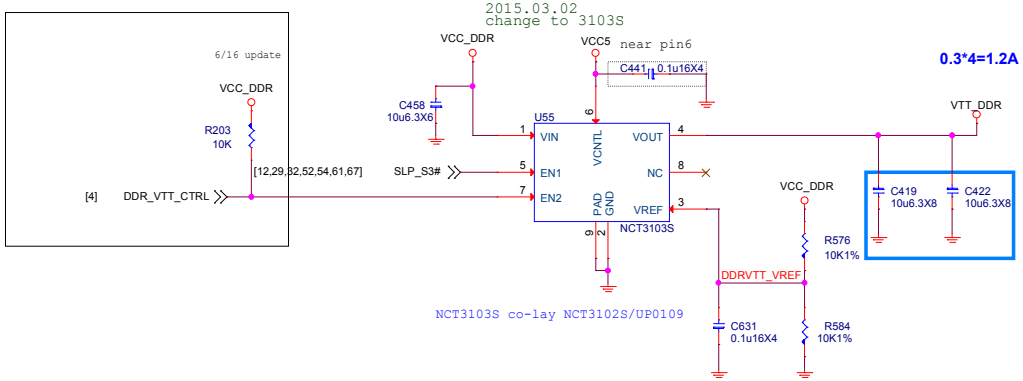


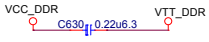


ENABLE HIGH:1.6V

To make sure VPP EN after 5VDIMM stable

DDR VTT Power





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PCH 1VSB

1.0V; 10A(7.929A)

OCP = 15A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 15A * 4.6mohm / 10uA
= 6.9K

Rocs:6.81K,OCP:
D03-632BA0C-N03 : 14.8A

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

1504 change to 8125 I32-8125E0C-R11

2014.08.25:Change 1u/0603

MAX:7.929A

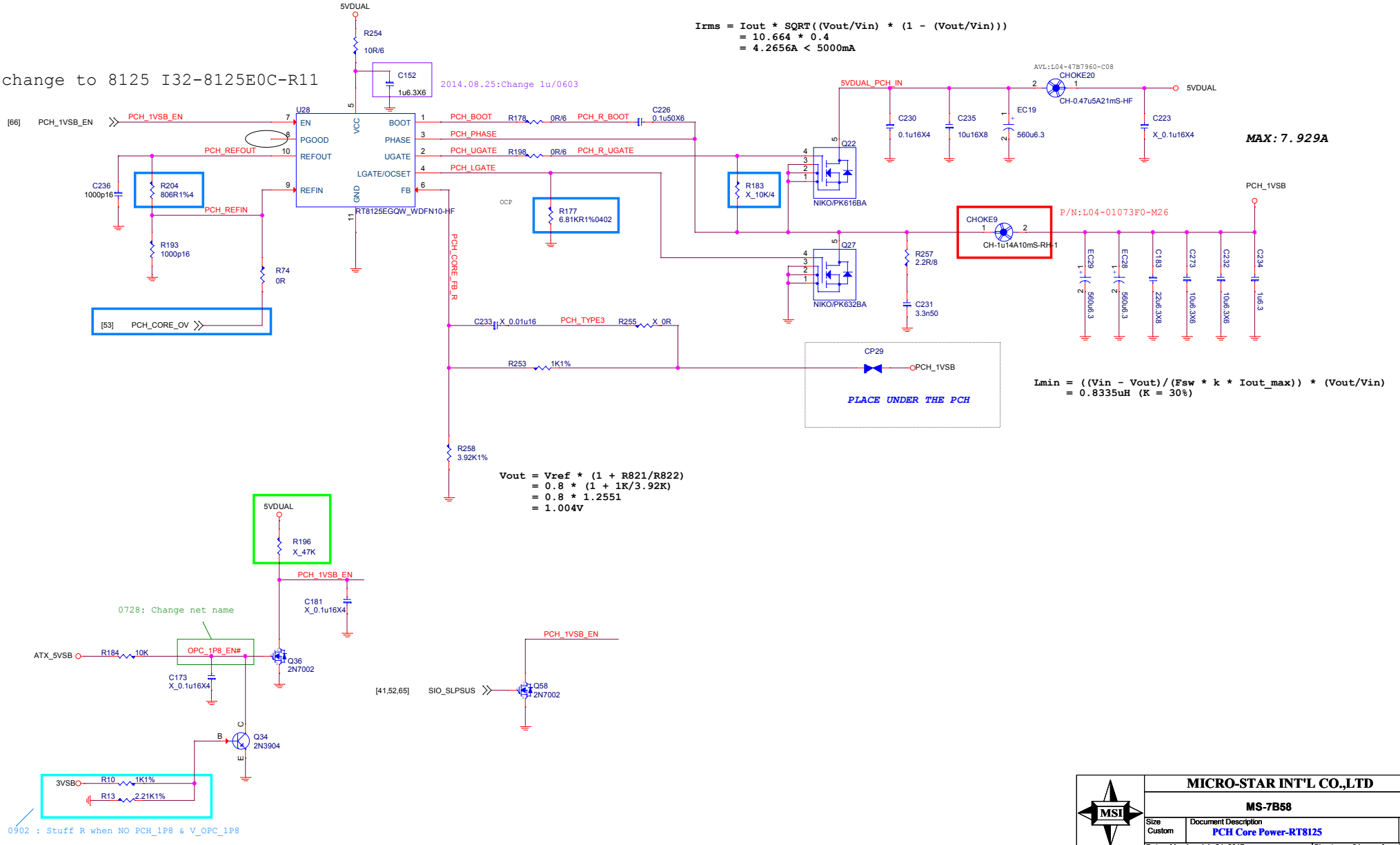
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

PLACE UNDER THE PCH

0728: Change net name

0902 : Stuff R when NO PCH_1P8 & V_OPC_1P8



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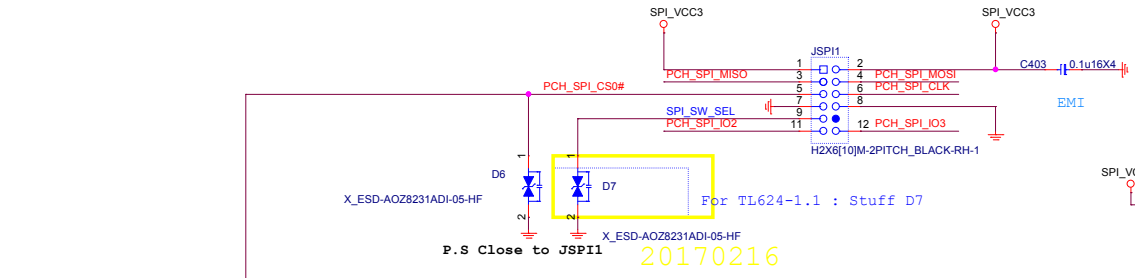
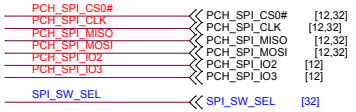
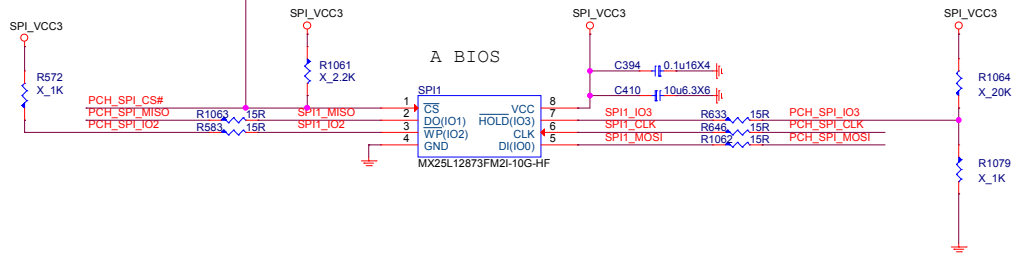
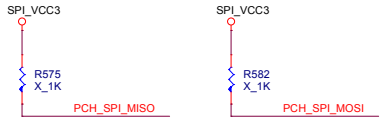
JSPI1 change to N31-2061451-H06.

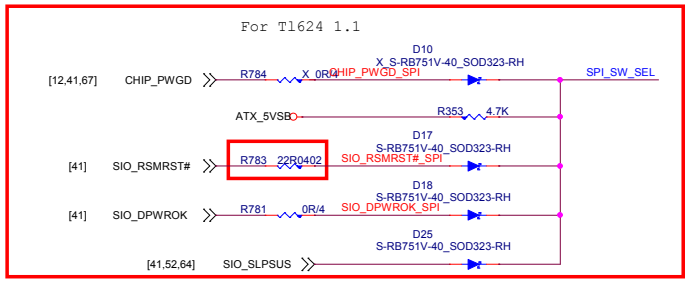








2014.09.29



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272

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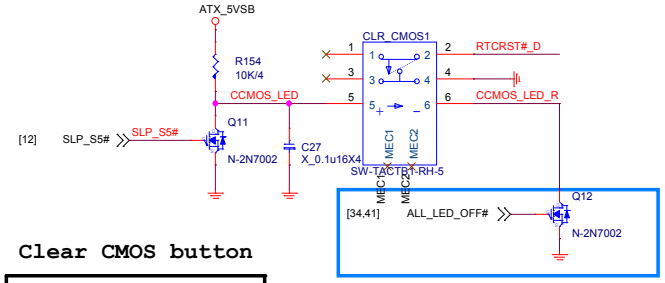
Clear CMOS HW MODE



Clear CMOS button

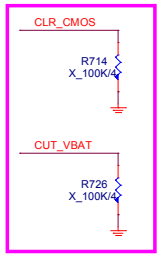
LED LIGHTING RULE
S0/S3/S4 : LED OFF
S5 : LED ON

By PM SPEC

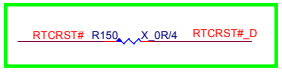
Function 1			
IN		OUT	
INPUT1	INPUT2	OUTPUT1	
0	1	1	Default
1	0	0	
1	1	0	
0	0	0	

Function 2					
IN		OUT			
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT	
0	0	0	1	1	Default
1	0	1	1	0 (discharge)	
0	1	1	0	0 (discharge)	
1	1	1	0	0 (discharge)	

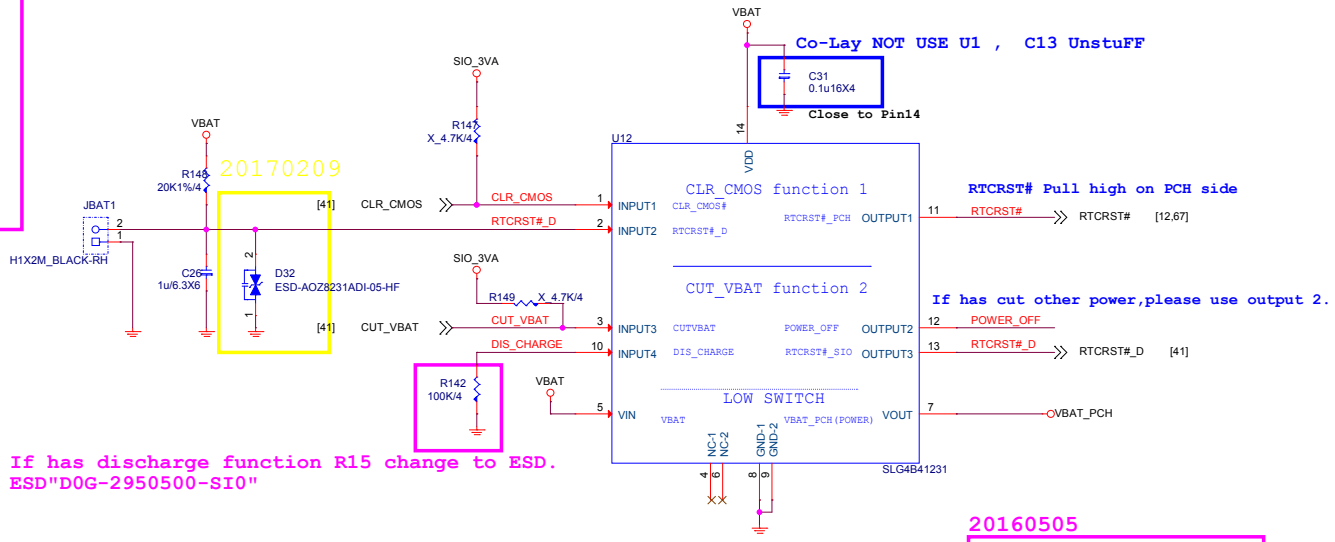
20160629



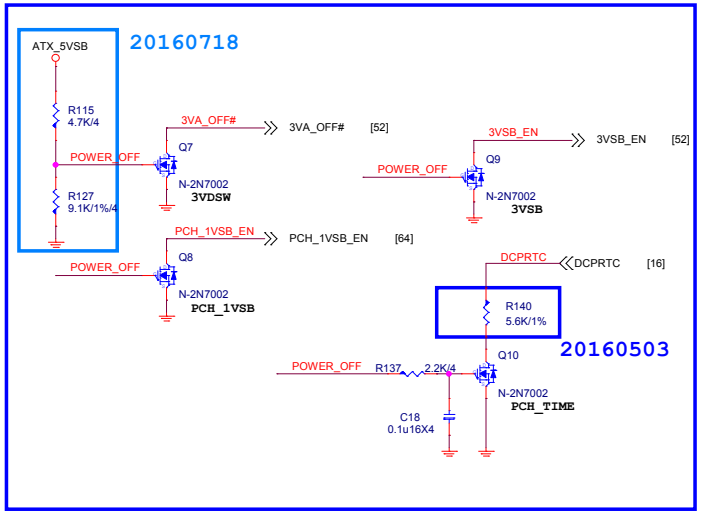
Co-Lay NOT USE U1 , R20 STUFF



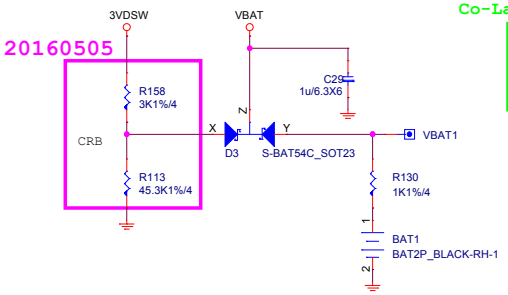
If STUFF R20 Please Check RTCRST# Double Pull High



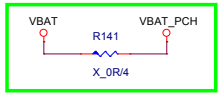
Co-Lay NOT USE U1 , ALL UNSTUFF



20160505



Co-Lay NOT U1 , Stuff R18



20160505

Remove

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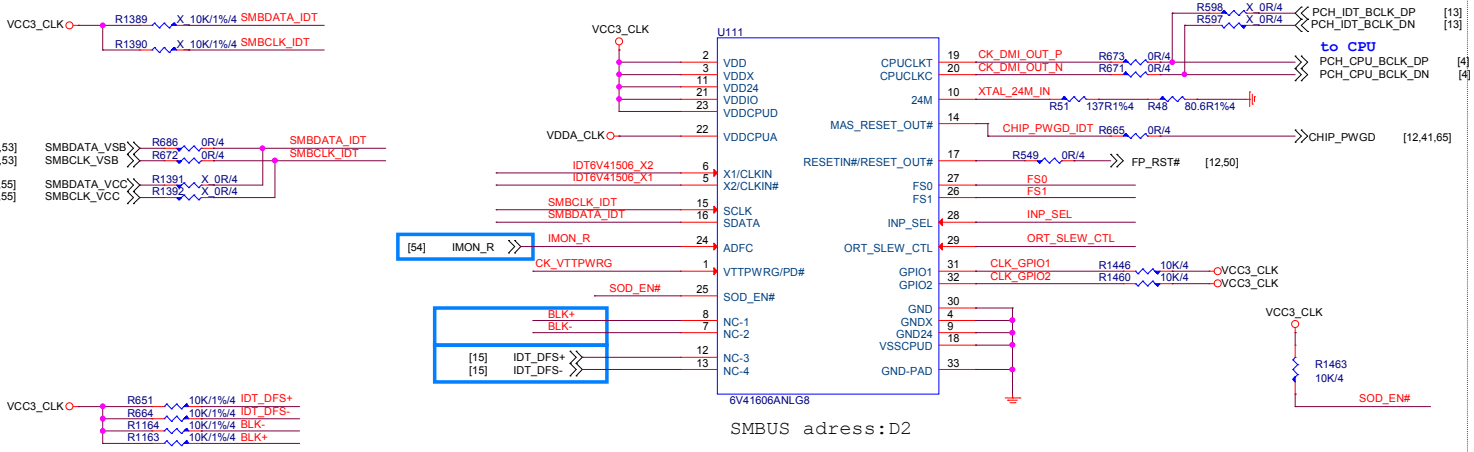
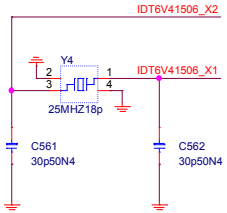
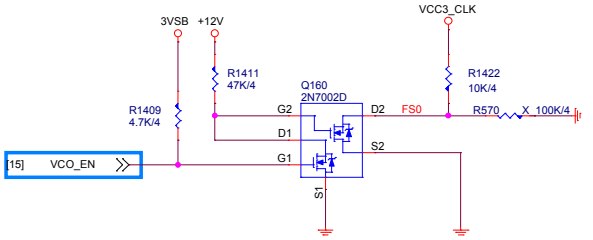
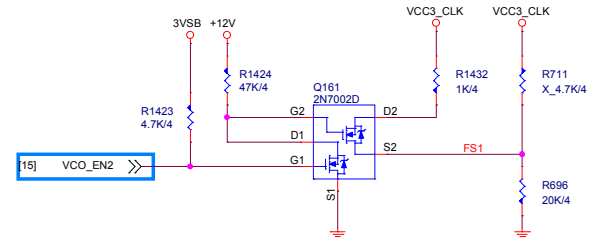


SMBUS adress:D2

Remove VDDA_CLK 0V.

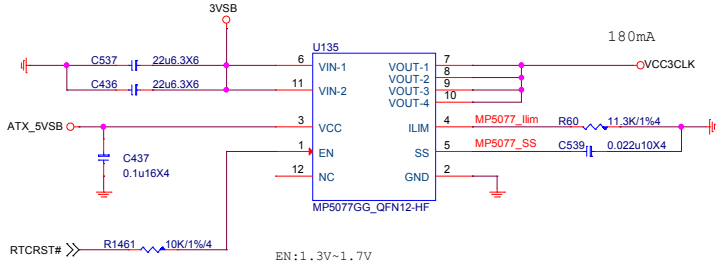


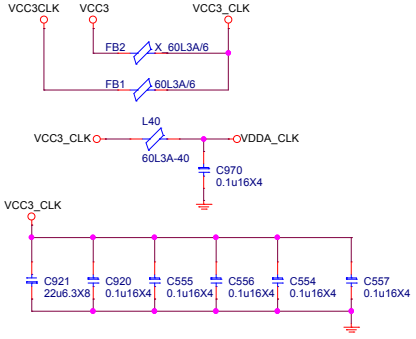


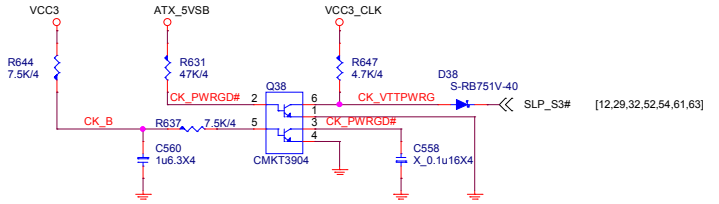


FS1	FS0	VCO Frequency
0	0	VCO 200MHz
0	1	VCO 400MHz (default)
1	0	VCO 1000MHz
1	1	VCO 100MHz

INP_SEL	
0	25MHz crystal input
1	100MHz differential input







To POWER 2015/02/03

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PCB

PCB1

7a78_11

PD0-07A7811-G37
PD0-07A7811-E48

CPU_H1

CPU
鎖座

CPU_H1

BAT1_X1

BAT-BCR2032P-RH

PCH Heatsink

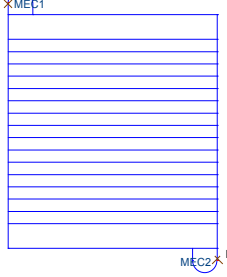
HS_PCH1_M6

LABEL

X_HS-0408660-HF

HS_PCH1

MEC1



MEC2

HS-0408660-HF

Mounting Holes

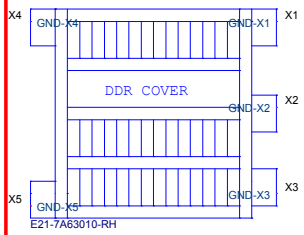
MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9

X_MH001

C466
0.1u16X4

C510
0.1u16X4

CV_DDR1



E21-7A63010-RH

VR Cover

CFOS_LA1

LABEL

CFOS_LABEL

U31_LA1

LABEL

U31_LABEL

NAH_LA1

LABEL

NAH_LABEL

BIOS_LA1

LABEL

BIOS_LABEL

SLI_LA1

LABEL

SLI_LABEL

HDMI_LA1

LABEL

HDMI_LABEL

XSPLIT_LA1

LABEL

SPLIT_LABEL

SSE_LA1

LABEL

SSE_LABEL

MKT_LA1

LABEL

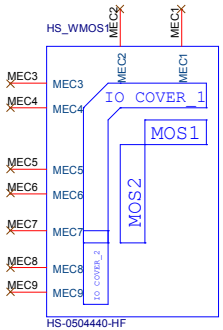
MKT_LABEL

MKT_M6

LABEL

X_MKT_LABEL

HS_WMOS



HS-0504440-HF

HS_IO_NMOS_M6

LABEL

HS-0504430-HF

Simulation

SIM1

SIM1

X_PIN1*2

SIM2

SIM2

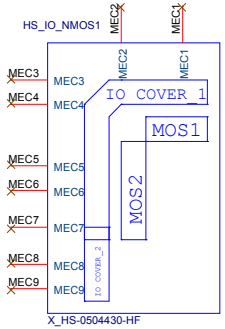
X_PIN1*2

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8

X_FM

HS_IO_NMOS1



X_HS-0504430-HF

MOS Heatsink

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