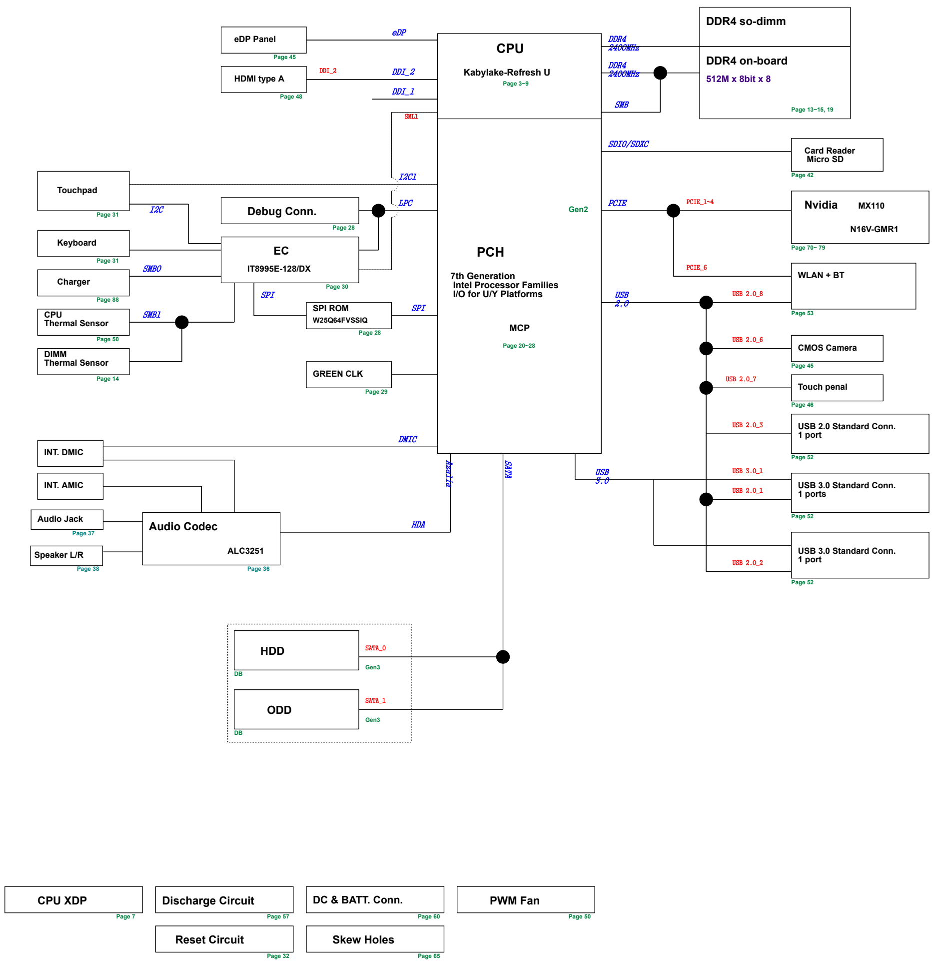
SYSTEM PAGE REF.

BLOCK DIAGRAM

X545FB SCHEMATIC Revision 1.0

Non Connected Standby



Power

- +VCCGT +VCCCORE +VCCST +VCCSA — Page 80 & 81
- +1.0VSUS / +1.8VSUS — Page 83
- +0.95VSG +VCCPRIM_CORE — Page 84
- +1.2V / +VTT / +2.5V — Page 86
- +3VADSW/+5VSUS — Page 87
- Load Switch — Page 88
- Charger — Page 89
- +VDDC — Page 91

Project Name: X445FB Rev: R1.0
Title : Block Diagram
Size: Custom Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE
Date: Wednesday, July 17, 2019 Sheet 1 of 102

PCH_CPT GPIO

	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_A0	Nativel	RC_IN#		EXT PU 10K	+3VS	PU at EC
	GPP_A1	Nativel	LPC_AD0				
	GPP_A2	Nativel	LPC_AD1				
	GPP_A3	Nativel	LPC_AD2				
	GPP_A4	Nativel	LPC_AD3				
	GPP_A5	Nativel	LPC_FRAME#				
	GPP_A6	Nativel	INT_SERIRQ		EXT PU 10K	+3VS	
	GPP_A7	GPO	N/A				
	GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS	
	GPP_A9	Nativel	CLK_KBCPCI_PCH				
	GPP_A10	Native	CLK_DEBUG				
For 555 N/A	GPP_A11	GPI	N/A	需確認是否具wake 功能			
	GPP_A12	GPO	N/A				
	GPP_A13	Nativel	SUSWARN#		EXT PU 10K	+3VSUS	
	GPP_A14	Nativel	PCH_SUS_STAT#				
Need Add EC	GPP_A15	Nativel	PCH_SUSACK#				
For 555 N/A	GPP_A16	GPO	N/A (SD_1P8_SEL)				
For 555 N/A	GPP_A17	GPO	N/A (SD_PWR_EN#)				
	GPP_A18	GPO	N/A				
	GPP_A19	GPO	N/A				
	GPP_A20	GPO	N/A				
	GPP_A21	GPO	N/A				
	GPP_A22	GPO	N/A				
	GPP_A23	GPO	N/A				
For 555 N/A	GPP_B0	Native	N/A (VCCPRIM_VID0)		EXT PU 10K	+3VS	
For 555 N/A	GPP_B1	Native	N/A (VCCPRIM_VID1)		EXT PU 10K	+3VS	
	GPP_B2	GPO	N/A				
	GPP_B3	GPO	N/A				
	GPP_B4	GPO	N/A				
	GPP_B5	Native	CK_REQ_P0# DGPU		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B6	Native	CK_REQ_P1#		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B7	Native	CK_REQ_P2#		EXT PU 10K	+3VS	
	GPP_B8	Native	CK_REQ_P3#		EXT PU 10K	+3VS	
	GPP_B9	Native	CK_REQ_P4# GLAN		EXT PU 10K	+3VS	
	GPP_B10	Native	CK_REQ_P5# WLAN		EXT PU 10K	+3VS	
	GPP_B11	Native	MPHY_PWREN (N/A)		EXT PU 20K	+3VSUS	
	GPP_B12	Native	PCH_SLP_S0#				
	GPP_B13	Native	PLT_RST#				
	GPP_B14	GPO	PCH_GPPB14				
For 555 N/A	GPP_B15	GPO	N/A (GSPI0_CS_R#)				
For 555 N/A	GPP_B16	GPO	N/A (GSPI0_CLK_R)				
For 555 N/A	GPP_B17	GPO	N/A (GSPI0_MISO_R)				
	GPP_B18	GPO	N/A (PCH_GPPB18)				
	GPP_B19	GPO	BT_ON/OFF#				
	GPP_B20	GPO	GPU_EVENT#		EXT PU 10K	+3VSG	
	GPP_B21	GPI	DGPU_FB_CLAMP_GPIO		EXT PU 10K	PU at DGPU	
	GPP_B22	GPO	PCH_GPPB22				
	GPP_B23	Native	SML1ALERT#		EXT PU 10K	+3VSUS	
	GPP_C0	Native	SMB_CK		EXT PU 2.2K	+3VSUS	
	GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C2	GPO	GPP_C2				
For 555 N/A	GPP_C3	Native	SML0_CK		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C4	Native	SML0_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C5	GPO	GPP_C5				
	GPP_C6	Native	SML1_CK		EXT PU 2.2K	+3VSUS	
	GPP_C7	Native	SML1_DATA		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C8	GPO	N/A (PCH_GPPC8)				
For 555 N/A	GPP_C9	GPO	N/A (PCH_GPPC9)				
For 555 N/A	GPP_C10	GPO	N/A (PCH_GPPC10)				
For 555 N/A	GPP_C11	GPO	N/A (PCH_GPPC11)				
	GPP_C12	GPI	DIMM_SEL0		EXT PU 10K	+3VSUS	
	GPP_C13	GPI	DIMM_SEL1		EXT PU 10K	+3VSUS	
	GPP_C14	GPI	DIMM_SEL2	UART1_RTS#	EXT PU 10K	+3VSUS	
	GPP_C15	GPI	N/A	UART1_CTS#			
	GPP_C16	GPO	AOAC_WLANLED(N/A)				
For 555 N/A	GPP_C17	GPO	N/A (ALS_INT#)				
For X541UV N/A	GPP_C18	Native	I2C1_SDA_TCH_PAD		PU 4.7K	+3VSUS	
For X541UV N/A	GPP_C19	Native	I2C1_SCL_TCH_PAD		PU 4.7K	+3VSUS	
	GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VSG	PU at DGPU
	GPP_C21	GPO	GPU_RST#		EXT PU 10K	+3VS	
	GPP_C22	GPO	DGPU_PWR_EN#		EXT PU 10K	+3VSUS	
	GPP_C23	GPI	TPanel_INT#		EXT PU 10K	+3VS	
	GPP_D0	GPO	N/A				
	GPP_D1	GPO	N/A				
	GPP_D2	GPO	N/A				
	GPP_D3	GPO	N/A				
For 555 N/A	GPP_D4	GPI	GPIO_SMI_ASM1142(N/A)				
	GPP_D5	GPO	SATA_ODD_PWRGT		EXT PU 10K	+3VS	
	GPP_D6	GPI	SATA_ODD_DA#		EXT PU 10K	+3VS	
	GPP_D7	GPO	N/A				
	GPP_D8	GPO	N/A				
	GPP_D9	GPI	PCB_ID0		EXT PU 10K		
For X541UV N/A	GPP_D10	GPI	DMIC_ID		EXT PU 10K		
	GPP_D11	GPI	TOUCHPAD_ID		EXT PU 10K		
	GPP_D12	GPI	TOUCH_PANEL_ID		EXT PU 10K		
	GPP_D13	GPI	TOUCHPAD_INTR#		EXT PU 10K	+3VS	
	GPP_D14	GPO	WLAN_LED_R				
X541UV Change	GPP_D15	GPO	SNSR_HUB_PWREN				
	GPP_D16	GPO	N/A	UART0_CTS#			
	GPP_D17	GPO	N/A				
	GPP_D18	GPO	N/A				
For 555 N/A	GPP_D19	GPO	(N/A) DMIC_CLK_PCH				
For 555 N/A	GPP_D20	GPO	(N/A) DMIC_DATA_PCH				
	GPP_D21	GPO	N/A				
	GPP_D22	GPO	N/A				

	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	
	GPP_D23	GPO	N/A				
	GPP_E0	GPI	DIRECT_ESATA_DETECT_R#		EXT PU 10K	+3VS	
	GPP_E1	GPI	SATA_ODD_FRONT_R#		EXT PU 10K	+3VS	
	GPP_E2	GPI	MSATA_MPCIE_DET#		EXT PU 10K	+3VS	
	GPP_E3	GPO	N/A				
	GPP_E4	GPO	SATA0_DEVSLP				
	GPP_E5	GPO	SATA1_PHYSLP_DIRECT				
	GPP_E6	GPO	SATA2_DEVSLP				
	GPP_E7	GPO	N/A				
	GPP_E8	NATIVE	PCH_SATA_LED#		EXT PU 10K	+3VS	
	GPP_E9	NATIVE	USB_OC_1_2#_R		EXT PU 10K	+3VSUS	
	GPP_E10	GPI	USB_OC_3_4#		EXT PU 10K	+3VSUS	
	GPP_E11	GPI	USB_OC_5_6#		EXT PU 10K	+3VSUS	
	GPP_E12	GPI	USB_OC_7_8#		EXT PU 10K	+3VSUS	
	GPP_E13	NATIVE	DDPB_HPD_PCH		EXT PD 100K	PD at IC of eDP to VGA	
	GPP_E14	NATIVE	HDMI_HP		EXT PD 1M	+3VS	PD at HDMI conn
	GPP_E15	GPO	EXT_SMI#		EXT PU 10K	+3VS	
	GPP_E16	GPI	EXT_SCI#		EXT PU 10K	+3VS	
	GPP_E17	NATIVE	EDP_HPD_CON			PD at LVDS conn	
	GPP_E18	NATIVE	DDPB_SCL_PCH				
	GPP_E19	NATIVE	DDPB_SDA_PCH		EXT PU 10K	+3VS	
	GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS	PU at HDMI conn
	GPP_E22	GPO	N/A				
	GPP_E23	GPO	N/A				
	GPP_F0	GPO	N/A				
	GPP_F1	GPO	N/A				
	GPP_F2	GPO	N/A				
	GPP_F3	GPO	N/A				
	GPP_F4	GPO	N/A				
	GPP_F5	GPO	N/A				
	GPP_F6	GPO	N/A				
	GPP_F7	GPO	N/A				
	GPP_F8	GPO	N/A				
	GPP_F9	GPO	N/A				
	GPP_F10	GPO	N/A				
	GPP_F11	GPO	N/A				
	GPP_F12	GPO	N/A				
	GPP_F13	GPO	N/A				
	GPP_F14	GPO	N/A				
	GPP_F15	GPO	N/A				
	GPP_F16	GPO	N/A				
	GPP_F17	GPO	N/A				
	GPP_F18	GPO	N/A				
	GPP_F19	GPO	N/A				
	GPP_F20	GPO	N/A				
	GPP_F21	GPO	N/A				
	GPP_F22	GPO	N/A				
	GPP_F23	GPO	N/A				
For 555 N/A	GPP_G0	GPO	N/A (SDIO_CMD)				
For 555 N/A	GPP_G1	GPO	N/A (SDIO_D0)				
For 555 N/A	GPP_G2	GPO	N/A (SDIO_D1)				
For 555 N/A	GPP_G3	GPO	N/A (SDIO_D2)				
For 555 N/A	GPP_G4	GPO	N/A (SDIO_D3)				
For 555 N/A	GPP_G5	GPO	N/A (SDIO_CD#)				
For 555 N/A	GPP_G6	GPO	N/A (SDIO_CLK)				
For 555 N/A	GPP_G7	GPO	N/A (SDIO_WP)				
For 555 ADD	GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW	
	GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW	
	GPD2	GPI	PCH_GPD2#		EXT PU 10K	+3VA_DSW	
	GPD3	Native	PM_PWRBTN#				
	GPD4	Native	PM_SUSB#		EXT PD 100K	PD at EC	
	GPD5	Native	PM_SUSC#		EXT PD 100K	PD at EC	
For 555 ADD	GPD6	Native	PM_SLP_A_R#				
	GPD7	GPO	WLAN_ON#				
For 555 N/A	GPD8	Native	NA (SUS_CK)		EXT PD 1K		
	GPD9	Native	PCH_SLP_WLAN# (N/A)				
	GPD10	Native	SLP_S5# (N/A)				
	GPD11	Native	LAN_PWREN (N/A)				VC lose

EC IT8995 GPIO

	Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
	GPA0	O	PWR_LED	LOW		
	GPA1	OD	CHG_LED#	HIGH	EXT 10K PU	+3VA_EC
	GPA2	OD	CHG_FULL_LED#	HIGH	EXT 10K PU	+3VA_EC
For 555 N/A	GPA3	Alt	EC_GPA3	LOW		
For 555 N/A	GPA4	O	EC_GPA4	LOW	EXT 10K PU	+3VA_EC
	GPA5	Alt	FAN0_PWM	LOW		
	GPA6	Alt	KB_LED_PWM	LOW		
For 555 N/A	GPA7	O	EC_GPA7 (N/A)	HIGH		
	GPB0	Alt	AC_IN_OC#	HIGH	EXT 10K PU	+3VA
	GPB1	I	LID_SW#	HIGH	EXT 10K PU	+3VA
For 555 N/A	GPB2	OD	(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPB3	I	PWR_SW#	HIGH	EXT 10K PU	+3VA
	GPB4	O	PS_ON	HIGH		
For 555 N/A	GPB5	O	A20GATE (N/A)	LOW	EXT 10K PU	+3VS
	GPB6	OD	RC_IN#	HIGH	EXT 10K PU	+3VS
For 555 N/A	GPC0	O	(N/A)	LOW		
	GPC1	Alt	SMB1_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPC2	Alt	SMB1_DAT	LOW	EXT 4.7K PU	+3VA_EC
	GPC3	O	PM_PWRBTN#	HIGH		
For 555 N/A	GPC4	I	EC_GPC4 (N/A)	LOW	EXT 10K PU	+3VS
	GPC5	I	PM_SUSC#	HIGH	EXT 100K PD	
	GPC6	Alt	BAT1_IN_OC#	HIGH	EXT 10K PD	
For 555 N/A	GPC7	I	(N/A)	LOW		
	GPD0	I	PCH_SLP_S0#	HIGH		
	GPD1	O	ME_AC_PRESENT	LOW	EXT 100K PU	+3VA_DSW
	GPD2	Alt	BUF_PLT_RST#	HIGH	EXT 100K PD	
	GPD3	OD	EXT_SCI#	HIGH	EXT 10K PU	+3VS
	GPD4	OD	EXT_SMI#	HIGH	EXT 10K PU	+3VS
	GPD5	O	OP_SD#	HIGH		
	GPD6	Alt	FAN0_TACH	LOW	EXT 10K PU	+3VS
For 555 N/A	GPD7	Alt	(N/A)	LOW	EXT 10K PU	+3VS
	GPE0	O	SUSB_EC#	HIGH	EXT 10K PD	
	GPE1	O	SUSC_EC#	HIGH	EXT 10K PD	
	GPE2	O	1.2V_ON	LOW		
	GPE3	O	N/A	HIGH		
For 555 N/A	GPE4	O	(N/A)	HIGH		
	GPE5	I	PM_SUSB#	LOW	EXT 100K PD	
For 555 N/A	GPE6	OD	CAP_LED#	HIGH		
	GPE7	OD	THRO_CPU#	HIGH	EXT 1K PU	+VCCSTG
	GPF0	O	5VSUS_ON	LOW	EXT 10K PU/ 1M PD	+3VA_EC
	GPF1	O	VSUS_ON	LOW	EXT 100K PU	+3VA_EC
	GPF2	Alt	SMB0_CLK	HIGH	EXT 4.7K PU	+3VA_EC
	GPF3	Alt	SMB0_DATA	HIGH	EXT 4.7K PU	+3VA_EC
	GPF4	Alt	TP_CLK	HIGH	EXT 4.7K PU	+3VS
	GPF5	Alt	TP_DAT	HIGH	EXT 4.7K PU	+3VS
	GPF6	Alt	PECI_EC	LOW		
	GPF7	O	PCH_SPI_OV	LOW		
	GPG0	O	DGPU_LIMIT	LOW		
	GPG1	O	PCH_SUSACK#	HIGH		
	GPG2	I	PWRLIMIT_EC#	HIGH	EXT 100K PU	+3VA_EC
For 555 N/A	GPG6	O	(N/A)	LOW		
	GPH0	Alt	PM_CLKRUN#	HIGH	EXT 8.2K PU	+3VS
For 555 N/A	GPH1	Alt	SMB3_CLK N/A	HIGH		
For 555 N/A	GPH2	Alt	SMB3_DAT N/A	HIGH		
	GPH3	O	PM_RSMRST#	HIGH	EXT 10K PD	
	GPH4	O	DPWROK_EC	LOW	EXT 10K PD	
	GPH5	O	PM_PWROK	LOW	EXT 100K PD	
	GPH6	O	PM_SYSPWROK	LOW	EXT 10K PD	
	GPH7	O	LCD_BACKOFF#	HIGH		
	GPI0	I	PM_SLP_SUS#	HIGH	EXT 10K PU/ 100K PD	+3VA_EC
	GPI1	I	3VSUS_PWRGD	LOW		
	GPI2	I	ALL_SYSTEM_PWRGD	LOW	EXT 10K PU	+3VS
	GPI3	I	IMVP8_PWRGD	LOW	EXT 10K PU	+3VS
	GPI4	I	3VA_DSW_PWRGD	LOW	EXT 100K PU	+3VA_DSW
	GPI5	I	ME_SusPwrDnAck_EC	LOW		
	GPI6	Alt	A/D_MAX_POWER	LOW	EXT 0 PD	
	GPI7	Alt	MB_MAX_POWER	LOW	EXT 100K PU/93.1K PD	+3VACC
	GPJ0	I	EC_WAKE_SCI	LOW		
	GPJ1	O	3VADSW_ON	LOW	EXT 100K PU	+3VA_EC
For 555 N/A	GPJ2	Alt	PL_REF_EC N/A	LOW		
	GPJ3	O	WLAN_PWR_EN	LOW		
For 555 N/A	GPJ4	Alt	IBAT_REF_EC N/A	LOW		
For 555 N/A	GPJ5	I	EC_GPJ5	LOW		
For 555 N/A	GPJ6	I	N/A	LOW		+3VS
For 555 N/A	GPJ7	O	N/A	HIGH		

*1: EC config GPI; Function output

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

USB3 Port

USB3_1	USB 3.0 Port 0
USB3_2	USB 3.0 Port 1
USB3_3	USB 3.0 Port 2
USB3_4	

PCI Express

PCIE 1	DGPU
PCIE 2	
PCIE 3	
PCIE 4	
PCIE 5	GLAN
PCIE 6	WLAN
PCIE 9	
PCIE 10	
PCIE 11	
PCIE 12	

SATA Port

SATA 0	HDD
SATA 1	ODD / 2nd HDD

PCI CLK

CLK0	DGPUx4
CLK1	
CLK2	
CLK3	
CLK4	LAN
CLK5	WLAN

USB Port

USB 1	USB 2.0 Port
USB 2	USB 2.0 Port
USB 3	USB 2.0 Port
USB 4	
USB 5	
USB 6	CAMERA
USB 7	TOUCH_PANEL
USB 8	WLAN/BT
USB 9	
USB 10	

USB 3.0 Port 0
USB 3.0 Port 1
USB 3.0 Port 2

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

For X540UPR ADD

BOM

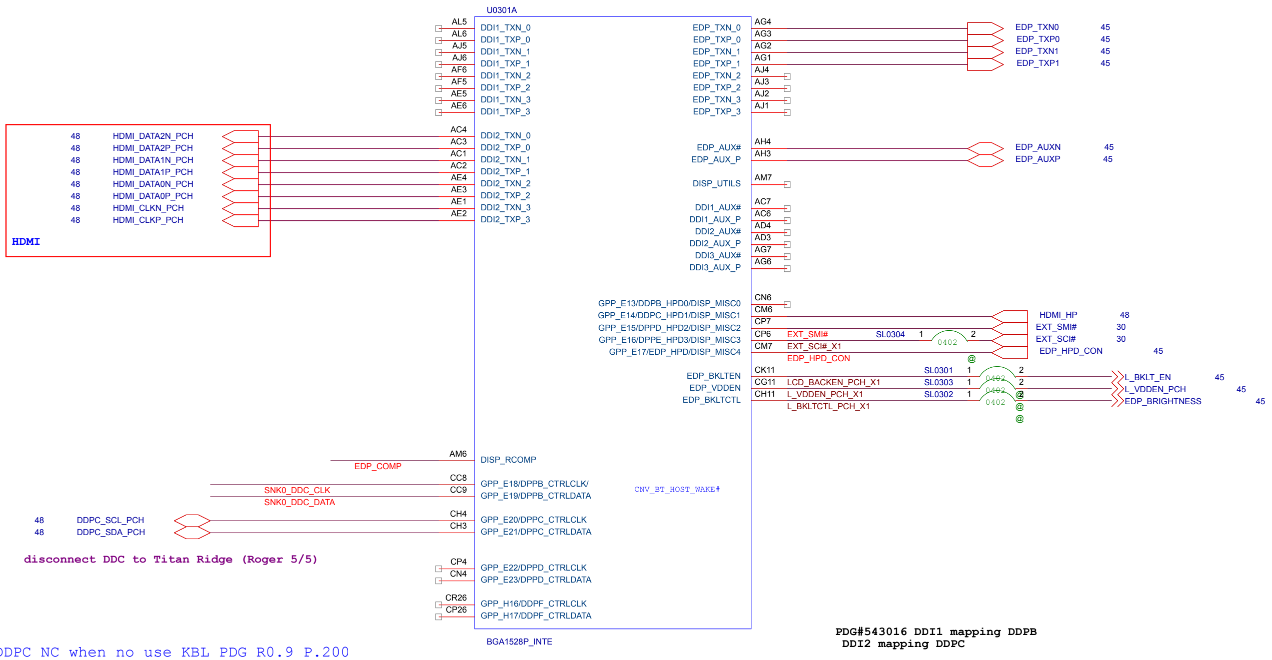
Project Name: X445FB		Rev R1.0
Title : System Setting		
Size D	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 2 of 102	

Main Board

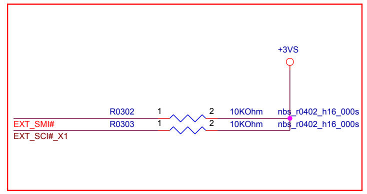
Display Port

A	EDP
B	Type C(DP)
C	HDMI

Intel Version	ASUS P/N
ES-0	01001-01540000

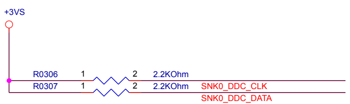


disconnect DDC to Titan Ridge (Roger 5/5)



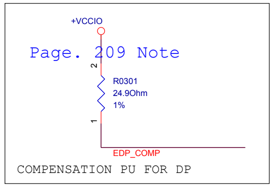
DDPC NC when no use KBL PDG R0.9 P.200

DDI Enable pull up. Disable NC.



	HDMI
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK

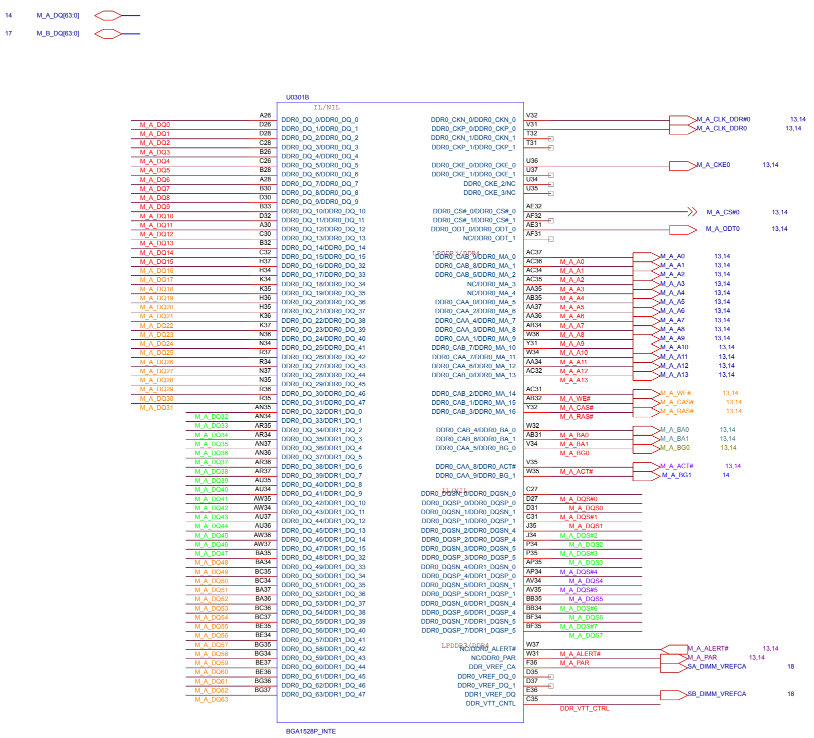
PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC

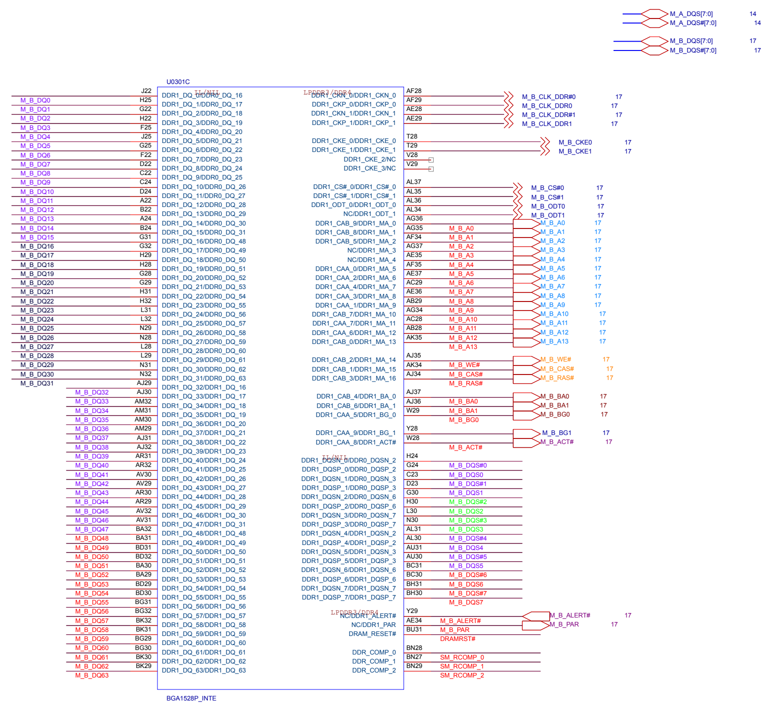


<Variant Name>

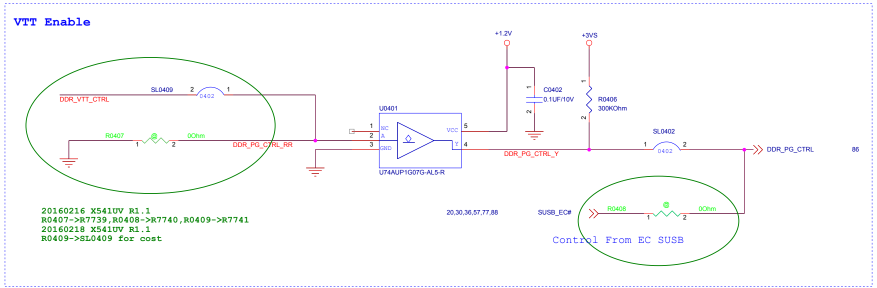
ASUS	Project Name: X445FB	Rev: R1.0
Title : CPU_DISPLAY		
Size: Custom	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 3 of 102	

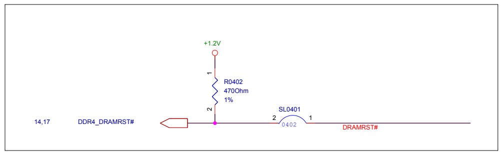
Interleaved

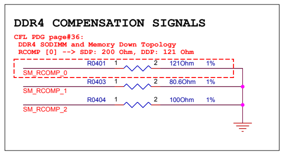




DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120



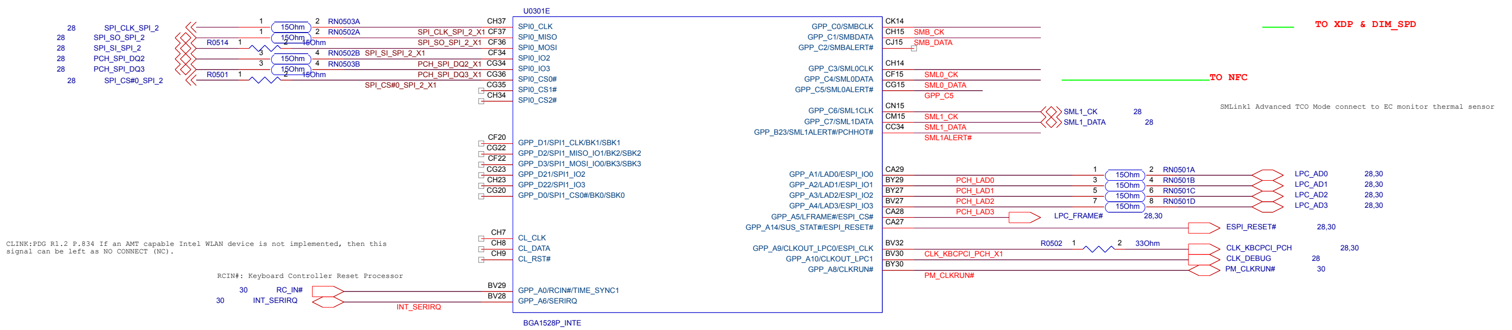


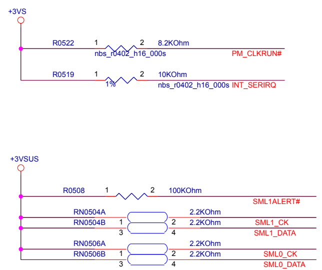


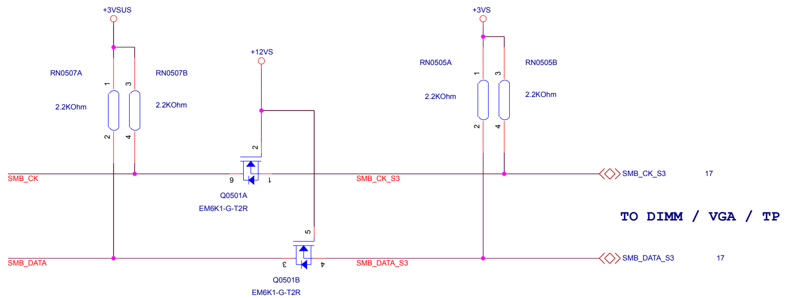
<Variant Name>

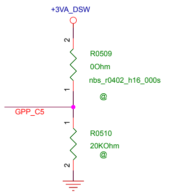
ASUS	Title : CPU_DDR4	
NB1-RD3EE1	Engineer: NB_EE	
Size: C	Project Name: X445FB	Rev: R1.0
Date: Wednesday, July 17, 2019	Sheet 4 of 102	

Main Board









GPP_C5: weak internal pull down	
PU	SPI BUS
PD	LPC is selected for EC (Default)

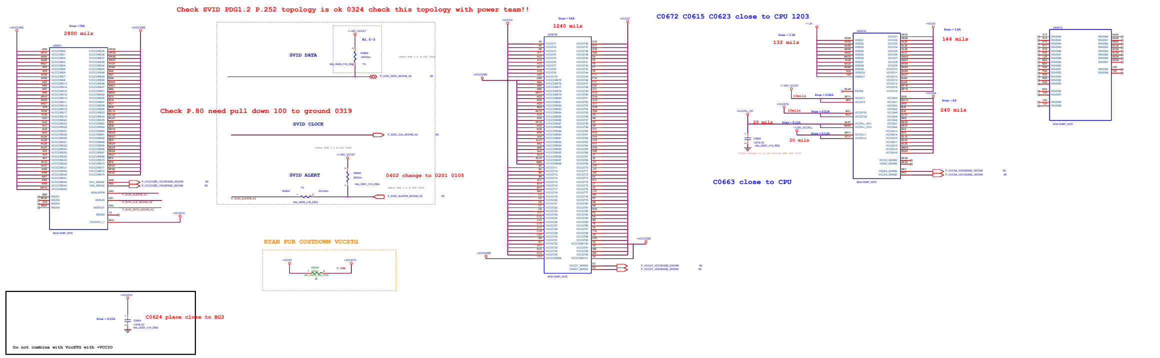
Transport Layer Security (TLS) Confidentiality

GPP_C2: weak internal pull down	
PU	Enable
PD	Disable Intel ME TLS ipher suite (no confodentiality) (Default)

TP for Boundary Scan Test

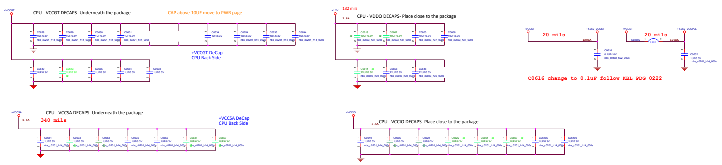
<Variant Name>

Project Name: X445FB		Rev: R1.0
Title : CPU_LPC,SPI,SMB,CLINK		
Size: Custom	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 5 of 102	



Power Plane:

+VCCCORE		
+VCCSA	System Agent power rail	
+VCCGT	Sliced graphics power rail	
+1.0V_VCCPLL=+VCCST	CPU PLL power rails	
+VCCIO_CPU=+VCCIO=+VCCSTG	IO power rail	Gated version of VCCST
+VCCPLL_OC=+1.2V	CPU digital PLL power rails	
+VDDQ_CPU=+1.2V	CPU Memory power rail, voltage dependent on memory technology	
+VCCST	Sustain voltage for processor in Standby modes	
+VCC_EDRAM_EOPIO		
+VCC_EDRAM_1P8		



WHL Ballmap Changes

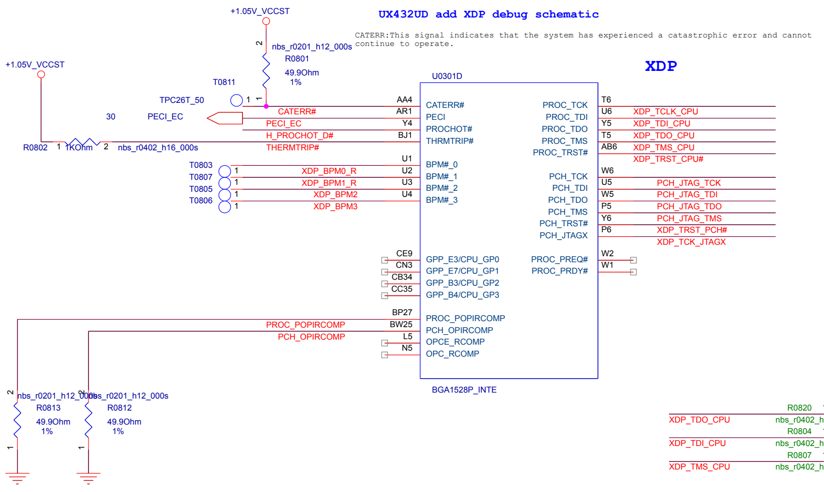
WHL ES1 will be a CFL-U43e fused down to CFL-U42

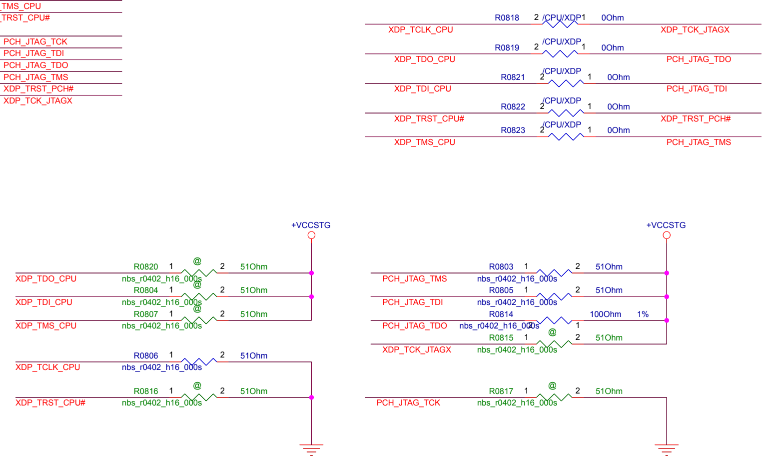
Pin Number	CFL U43E Netname	WHL ES1 Netname	WHL ES2 Netname
AH26	ZVM_N	RSVD	RSVD
T25	VSSEOPIO_SENSE	RSVD	RSVD
V25	VCCEOPIO_SENSE	RSVD	RSVD
AA24	VCCEOPIO	RSVD	RSVD
AA26	VCCEOPIO	RSVD	RSVD
AB25	VCCEOPIO	RSVD	RSVD
AC24	VCCEOPIO	RSVD	RSVD
AC25	VCCEOPIO	RSVD	RSVD
AC26	VCCEOPIO	RSVD	RSVD
AD24	VCCEOPIO	RSVD	RSVD
AD26	VCCEOPIO	RSVD	RSVD
K12	VCCEDRAM	RSVD	RSVD
K14	VCCEDRAM	RSVD	RSVD
K15	VCCEDRAM	RSVD	RSVD
K17	VCCEDRAM	RSVD	RSVD
K18	VCCEDRAM	RSVD	RSVD
K20	VCCEDRAM	RSVD	RSVD
L25	VCCEDRAM	RSVD	RSVD
M24	VCCEDRAM	RSVD	RSVD
M26	VCCEDRAM	RSVD	RSVD
P24	VCCEDRAM	RSVD	RSVD
P26	VCCEDRAM	RSVD	RSVD
R24	VCCEDRAM	RSVD	RSVD
R25	VCCEDRAM	RSVD	RSVD
R26	VCCEDRAM	RSVD	RSVD
Y24	VCC_EDRAM_FUSEPRG	RSVD	RSVD
Y25	VCC_EDRAM_FUSEPRG	RSVD	RSVD
V24	VCC_EDRAM_1P8	RSVD	RSVD
W25	VCC_EDRAM_1P8	RSVD	RSVD
AJ27	MSM_N	RSVD	RSVD
B35	EDRAM_VIEW[1]	RSVD	RSVD
A34	EDRAM_VIEW[0]	RSVD	RSVD
G4	EDRAM_THERMDC	RSVD	RSVD
G3	EDRAM_THERMDA	RSVD	RSVD
L5	EDRAM_OPIO_RCOMP	RSVD	RSVD
C34	EDRAM_EDM	RSVD	RSVD
G1	EANALOGVP[1]	RSVD	RSVD
G2	EANALOGVP[0]	RSVD	RSVD
D34	CPU_EOPIO_VIEW[1]	RSVD	RSVD
A35	CPU_EOPIO_VIEW[0]	RSVD	RSVD
N5	CPU_EOPIO_RCOMP	RSVD	RSVD

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

* Pins marked RSVD must be left as NC

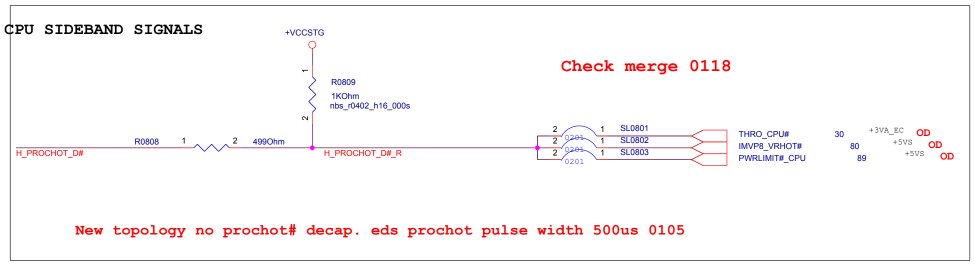
Main Board





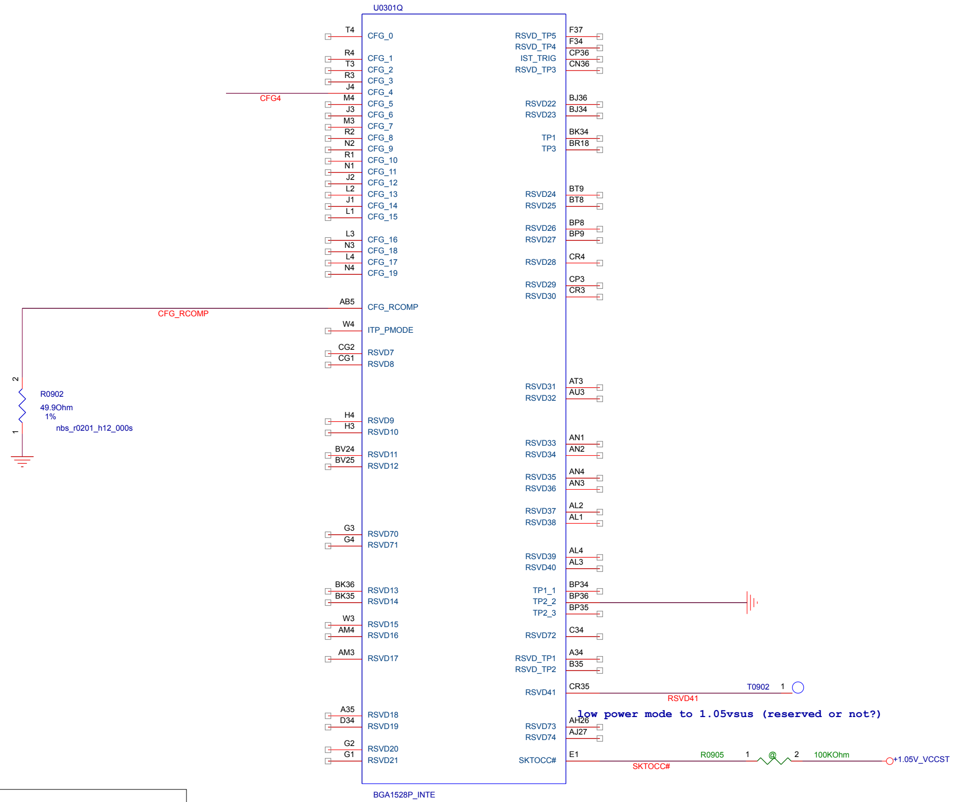
On Package Cache resistance Compensation
from processor: Refer to the appropriate platform
design guide for implementation details and values.
Unconnected for Processors without OPC.

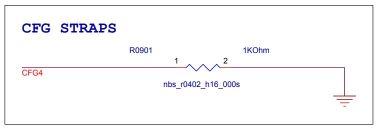
No OPC Check remove 且R0811 R0810量測兩端為0V 0126



<Variant Name>

ASUS	Project Name: X445FB	Rev: R1.0
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 8 of 102	

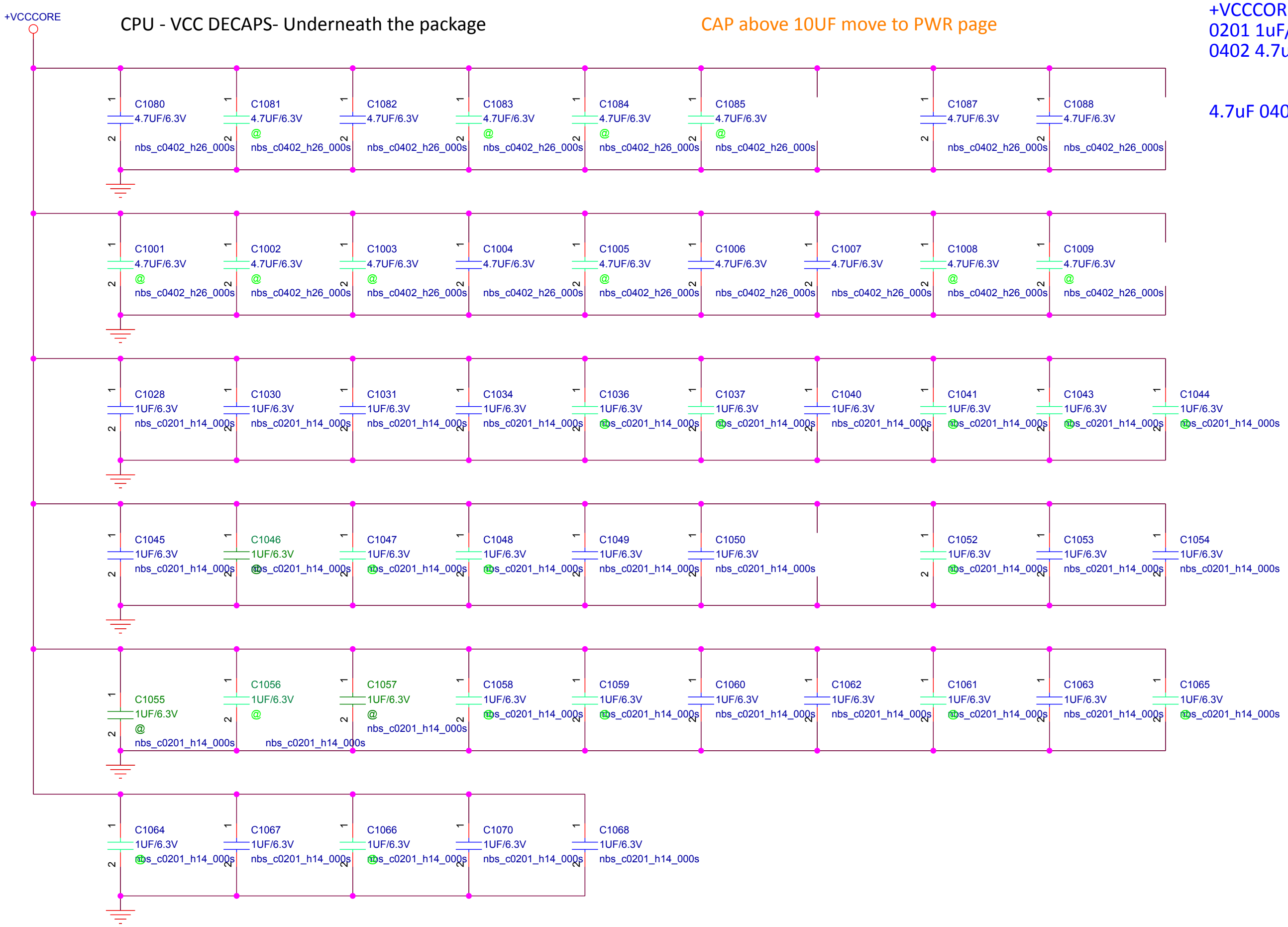




	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

<Variant Name>

Project Name: X445FB
Rev: R1.0
Title : CPU_CFG,RSVD
Size: Custom
Dept.: NB1-RD3EE1
Engineer: NB_EE
Date: Wednesday, July 17, 2019
Sheet 9 of 102

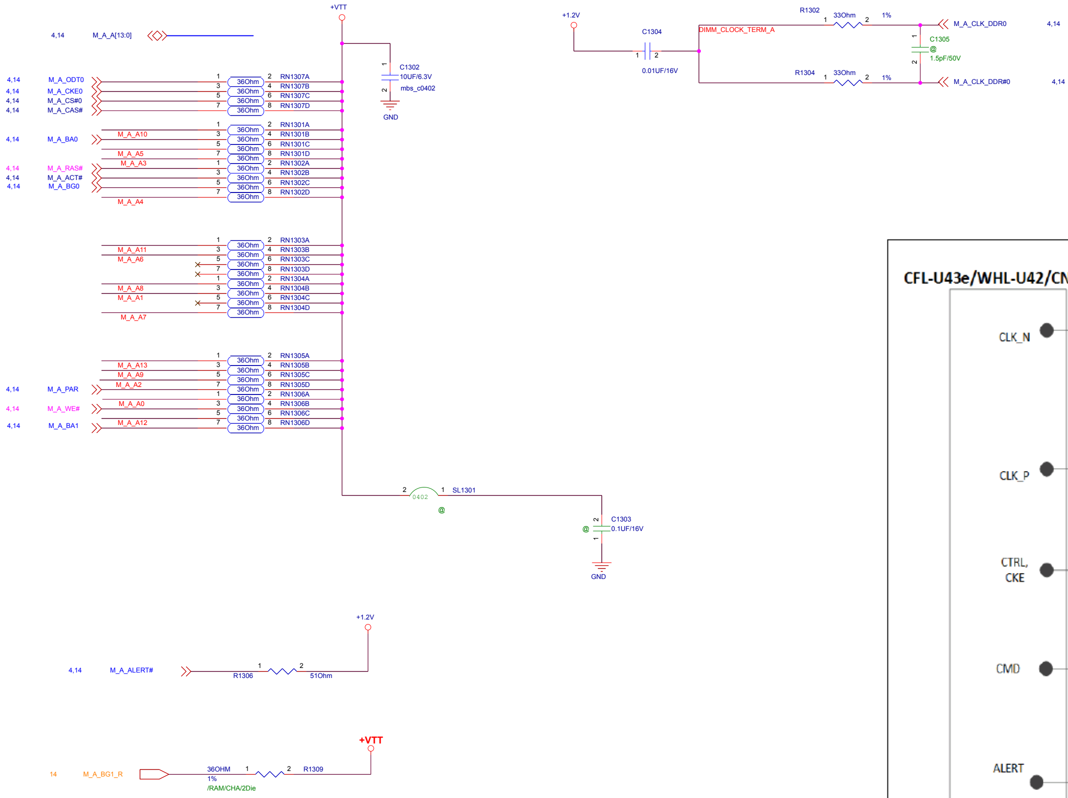


CAP above 10UF move to PWR page

+VCCCORE DeCap
0201 1uF/6.3V X5R h14 *35
0402 4.7uF/6.3V X5R h13 * 18

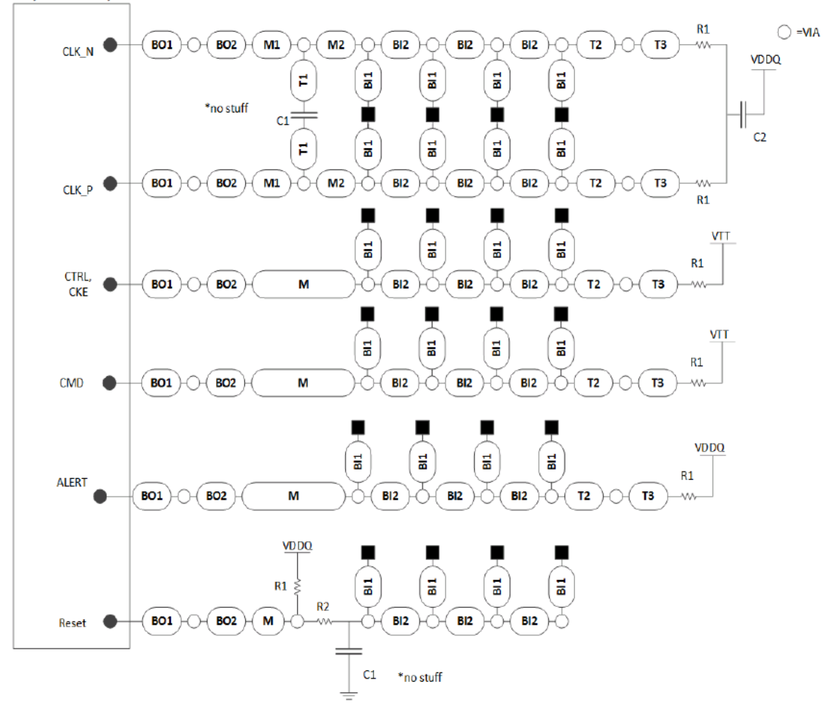
4.7uF 0402 H=0.33

Project Name
X445FB



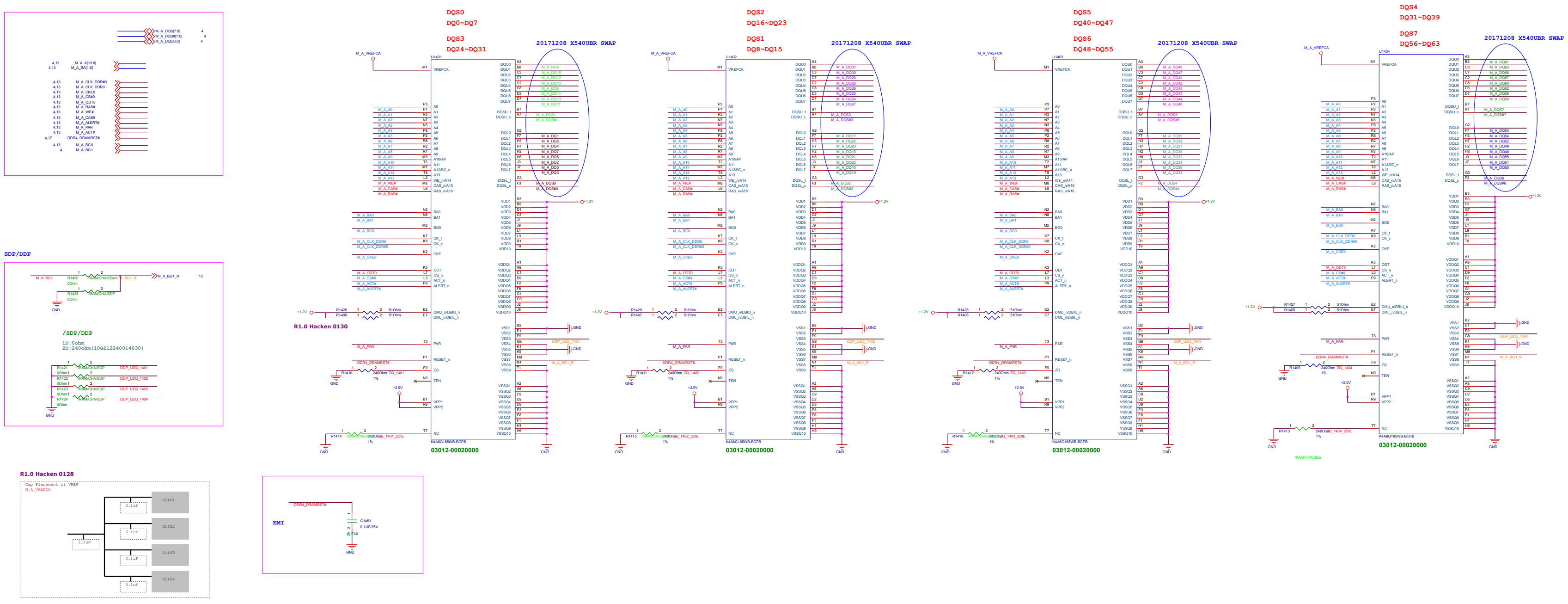
BG1 Rtt for DDP.

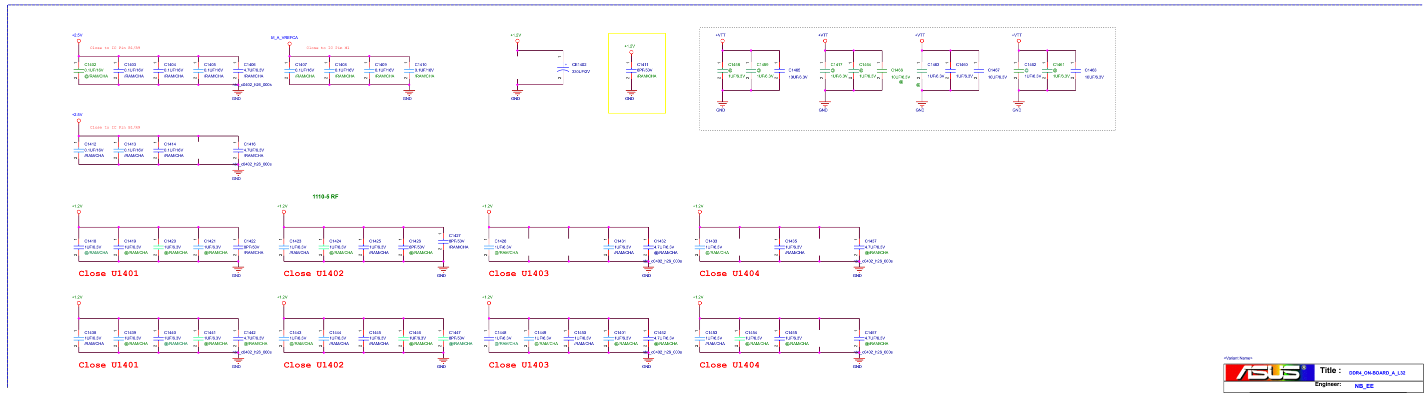
CFL-U43e/WHL-U42/CNL-U22



Note: The ALERT signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.

<Variant Name>



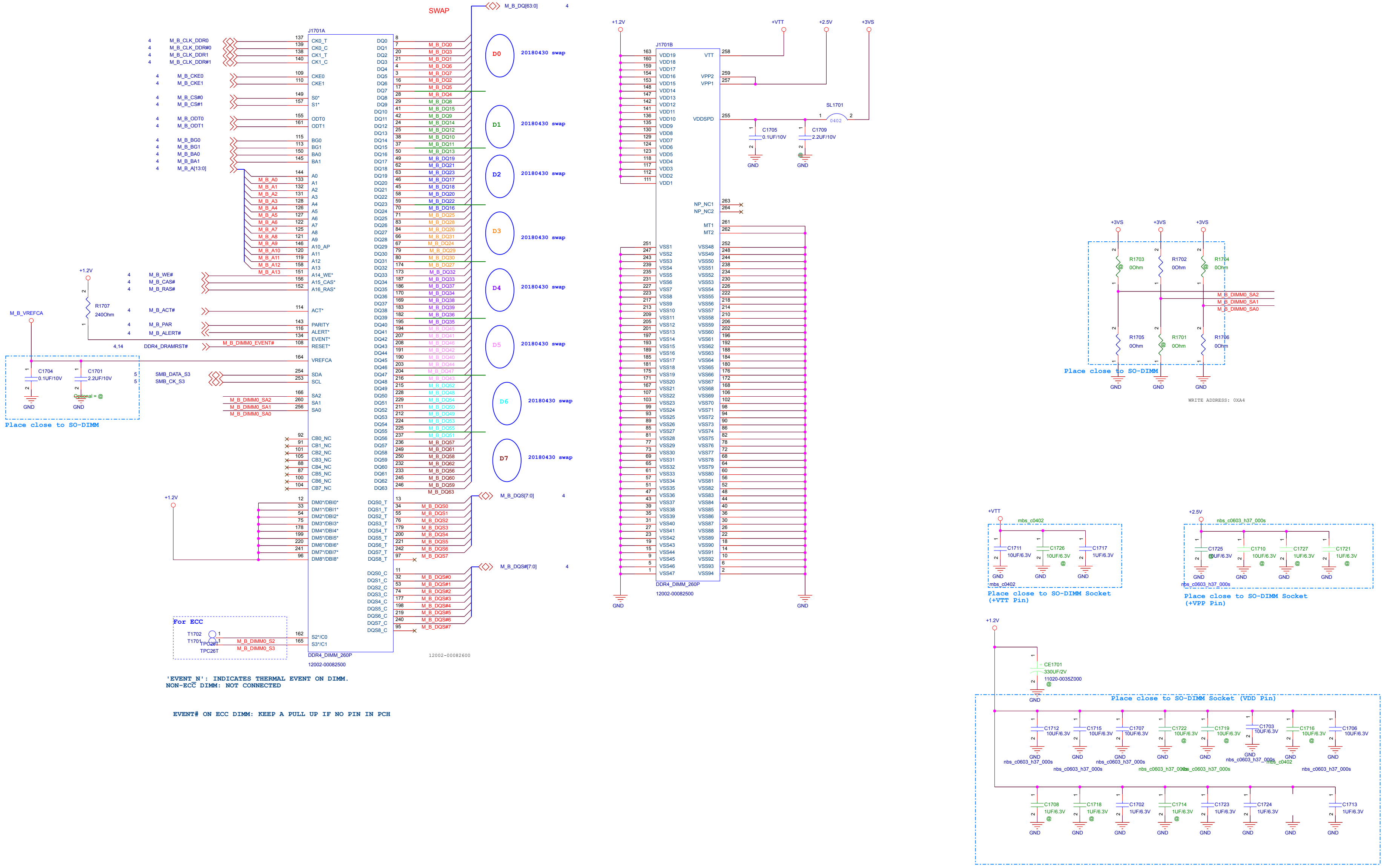


Onboard Memory Source

ASUS P/N	Capacity	Vendor
03012-00020500	4Gb 512X16	MICRON/MT40A512M16LY-075:E
03012-00020300	4Gb 512X16	HYNIX/H5AN8G6NAFR-UHC

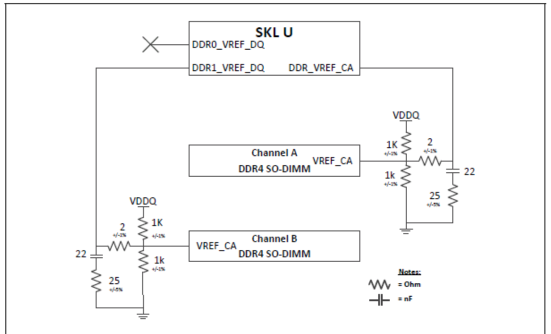
<Variant Name>

Title :	DDR4_ON-BOARD_A_L32
Engineer:	NB_EE
Size	D
Project Name	X445FB
Rev	R1.0
Date:	Wednesday, July 17, 2019
Sheet	14 of 102



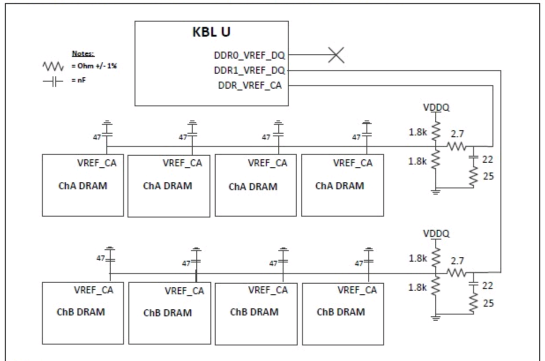
SWAP
M_B_DQ[63:0]
J1701A
DDR4_DIMM_260P
12002-00082500
D0 20180430 swap
D1 20180430 swap
D2 20180430 swap
D3 20180430 swap
D4 20180430 swap
D5 20180430 swap
D6 20180430 swap
D7 20180430 swap
M_B_DQS[7:0]
M_B_DQS#[7:0]
M_B_VREFCA
Place close to SO-DIMM
For ECC
J1701B
DDR4_DIMM_260P
12002-00082500
Place close to SO-DIMM
WRITE ADDRESS: 0XA4
Place close to SO-DIMM Socket (+VTT Pin)
Place close to SO-DIMM Socket (+VPP Pin)
Place close to SO-DIMM Socket (VDD Pin)
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



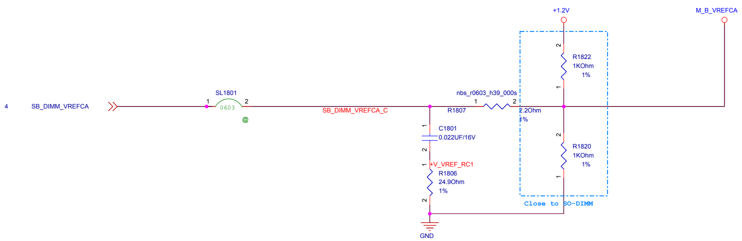
Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

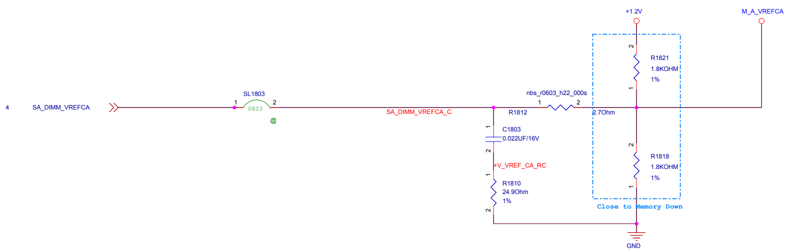
Figure 4-50. KBL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

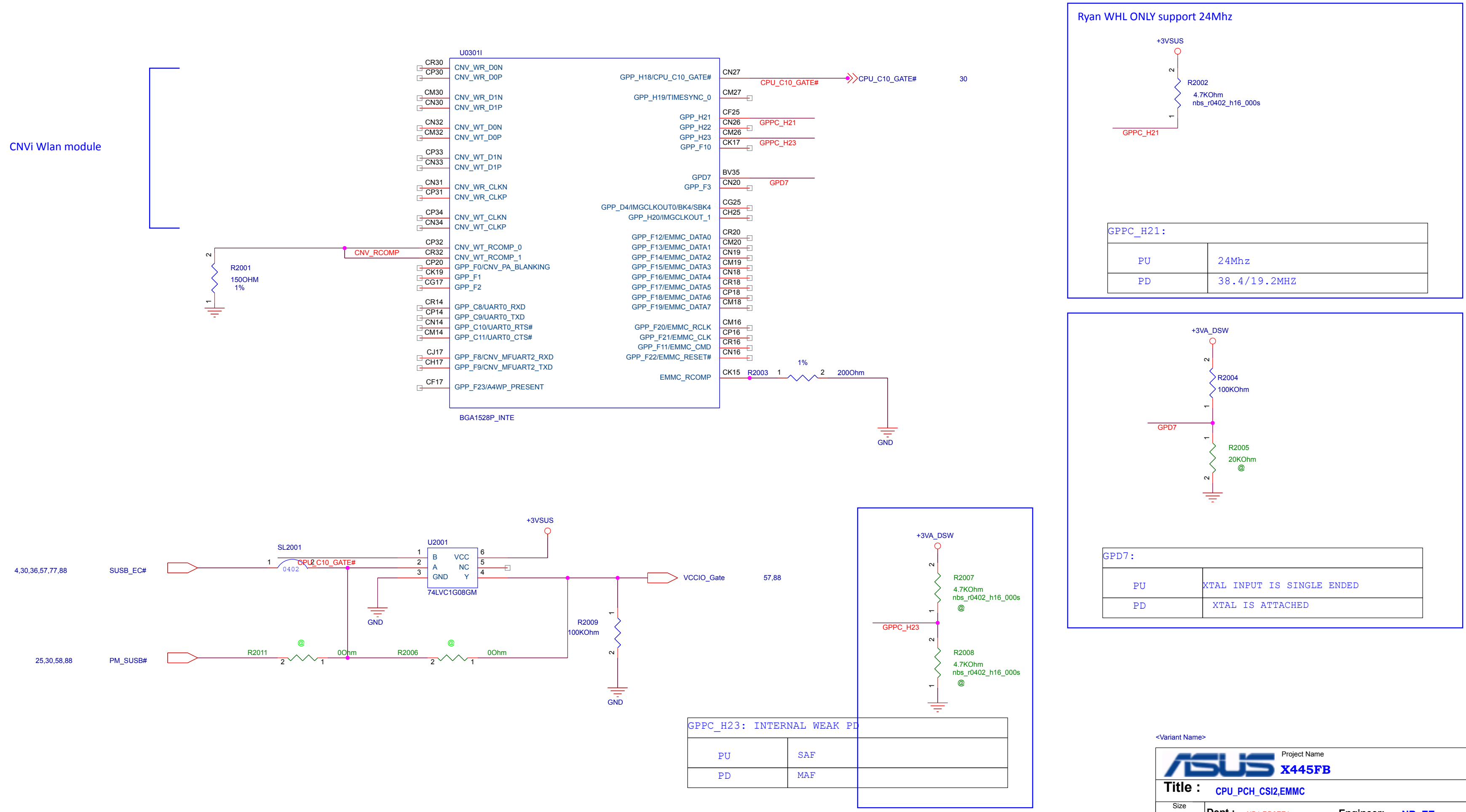


Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

All Vref trace must be 20 mils width







GPPC_H21:	
PU	24Mhz
PD	38.4/19.2MHZ

GPD7:	
PU	XTAL INPUT IS SINGLE ENDED
PD	XTAL IS ATTACHED

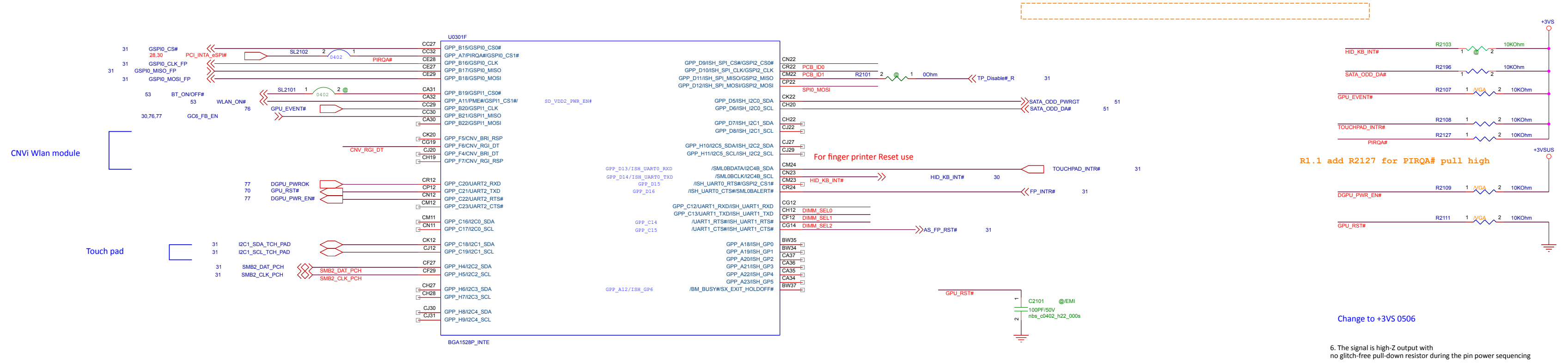
GPPC_H23: INTERNAL WEAK PD	
PU	SAF
PD	MAF

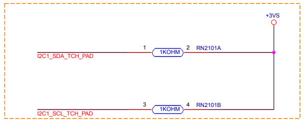
<Variant Name>

ASUS	Project Name X445FB	Rev R1.0
Title : CPU_PCH_CSI2,EMMC		
Size B	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 20 of 102	

2016/10/21 X542UA_#52, Add GSPI0 for FingerPrint & PU to +3VS

R1.1 add R2127 for PIRQA# pull high





0131 Ryan change to 1K
for ScreenPad rising time fail

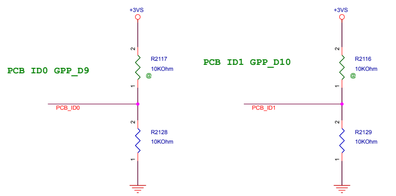
No Reboot

NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable

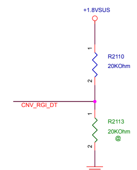
Boot BIOS Strap Bit BBS

PCH_GPPB22: weak internal pull down	
PU	LPC
PD	SPI (Default)

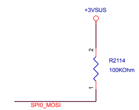


PCB ID

PCB_ID1(GPP_D10)	PCB_ID0(GPP_D09)	NOTE
0	0	
0	1	
1	0	
1	1	



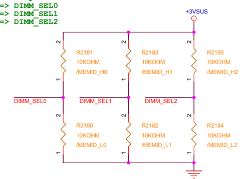
PCH_GPPF6: weak internal pull HIGH	
PU	INTEGRATED CNVI DISABLE
PD	INTEGRATED CNVI ENABLE



PCH_GPPD12:
External pull-up is required
(CNL_PCH EDS 0.7 #56)

DDR4 Table			DIMM_SEL# 0	1	2	Key Part List
03012-00020600 SAMSUNG/K4A8G165WB-BCRC	CHA	Samsung 4GB	0	0	0	
03012-00020500 MICRON/MT40A512M16LY-075:E	CHA	MICRON 4GB	0	0	1	
03012-00040500 HYNIX/H5ANAG6NCMR-VKC	CHA	HYNIX 8GB	0	1	0	
03012-00020601 MICRON/MT40A1G16KNR-075:E	CHA	MICRON 8GB	0	1	1	
	CHA		1	0	0	
	CHA		1	0	1	

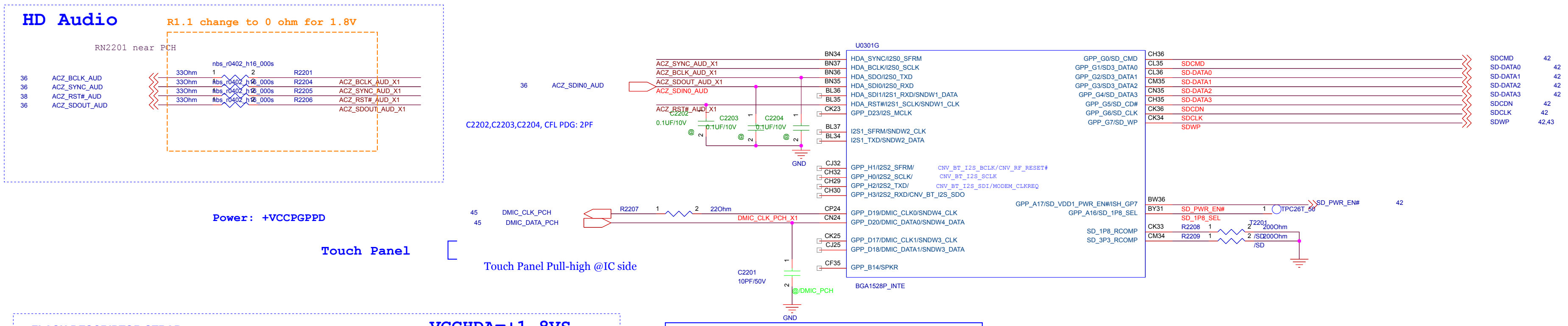
Onboard Memory PCB-ID:
GPP_I2 => DIMM_SEL0
GPP_I3 => DIMM_SEL1
GPP_I4 => DIMM_SEL2



<Variant Name>

Project Name: X445FB	Rev: R1.0
Title : CPU_CFG,RSVD,GND	
Size: Custom; Dept.: NB1-RD3EE1; Engineer: NB_EE	
Date: Wednesday, July 17, 2019	Sheet 21 of 102

HD Audio



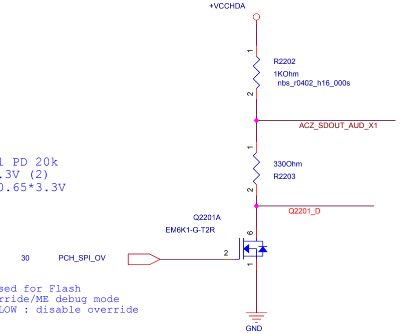
Power: +VCCPGPPD

Touch Panel

Touch Panel Pull-high @IC side

FLASH DESCRIPTOR STRAP

VCCHDA=+1.8VS



HDA_SDO
0=Enable
1=Disable Override

ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2) ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V

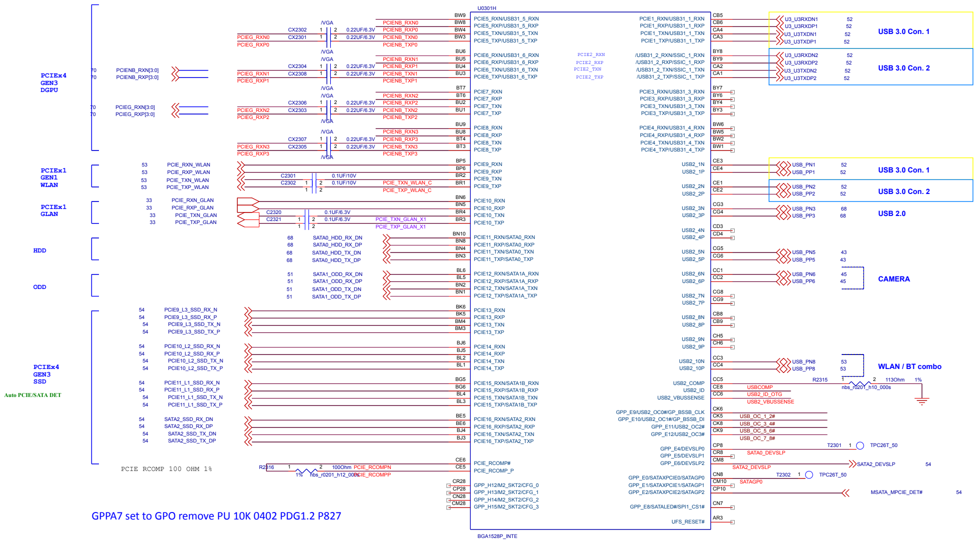
ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

Intel: To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 KΩ to 2.2 KΩ ±5% resistor.

Top-Block Swap Override

EDS 4.3.1

PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)



GPPA7 set to GPO remove PU 10K 0402 PDG1.2 P827

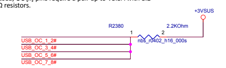
PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	N/A		
PCIE 2	N/A		
PCIE 3	N/A		
PCIE 4	N/A		
PCIE 5	N/A		
PCIE 6	WLAN		Port5
PCIE 7/SATA 0	SSD	SATA SSD	Port4
PCIE 8/SATA 1A	SSD		
PCIE 9	SSD		
PCIE 10	SSD		
PCIE 11/SATA 1B	N/A		

	USB 2.0
1	USB 3.0 Con. 1
2	USB 3.0 Con. 2
3	USB 2.0 Con. 3
4	
5	CARD READER
6	Camera
7	
8	BT
9	
10	BT

	USB 3.0
USB3_1	USB 3.0 Con. 1
USB3_2	USB 3.0 Con. 2
USB3_3	
USB3_4	

Merge 0119

If unused, OC [x] pins require a pull-up to V3.3A with 8.2~10 KΩ resistors.

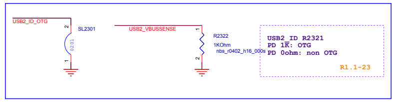


When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

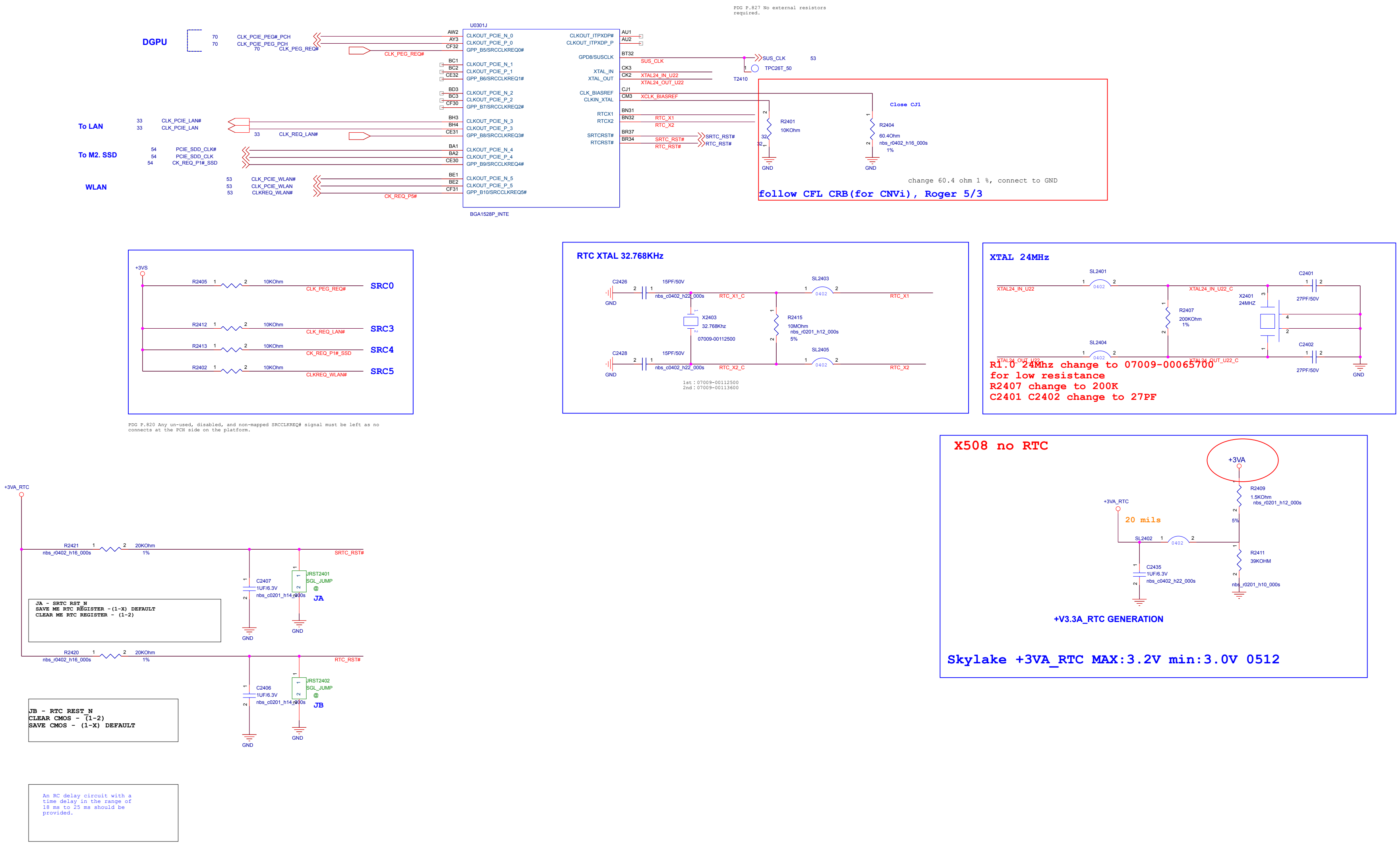
R1.2 SATA_DEVSLP change to DEVSLP2

SATA PORT2 0323

PDG1.2 P.848 Unused SATAGP[2:0] pins can be left as no connect and need to be default to GPIO functionality, refer to an unused GPIO for termination guidance.

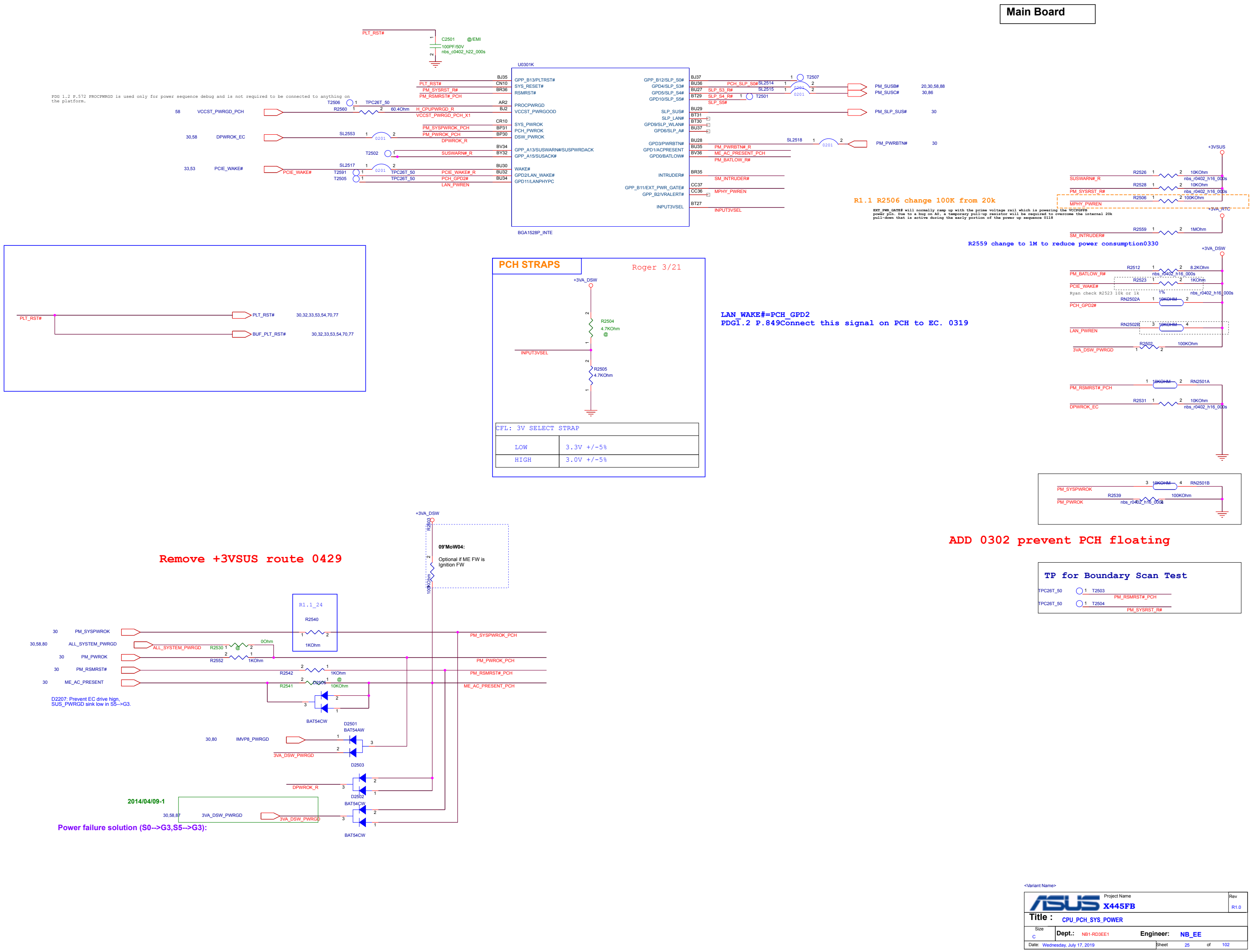


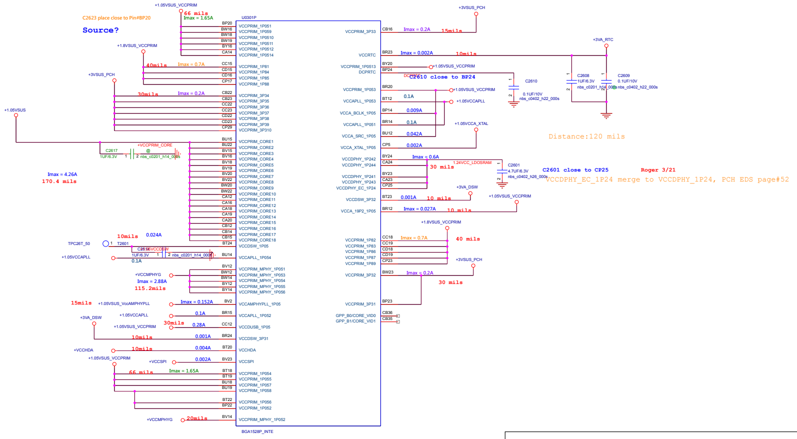
<Variant Name>



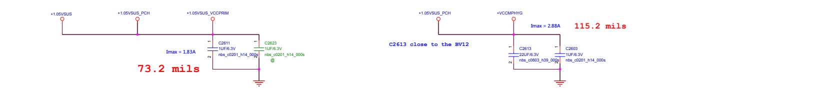
<Variant Name>

ASUS	Project Name: X445FB	Rev: R1.0
Title : CPU_PCH_CLOCK SIGNALS,RTC		
Size: C	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 24 of 102	


Main Board
PCH STRAPS
Roger 3/21
CFL: 3V SELECT STRAP
LOW 3.3V +/-5%
HIGH 3.0V +/-5%
LAN_WAKE#=PCH_GPD2
PDG1.2 P.849Connect this signal on PCH to EC. 0319
R1.1 R2506 change 100K from 20k
R2559 change to 1M to reduce power consumption0330
ADD 0302 prevent PCH floating
TP for Boundary Scan Test
Remove +3VSUS route 0429
D2207: Prevent EC drive high, SUS_PWRGD sink low in S5-->G3.
2014/04/09-1
Power failure solution (S0-->G3,S5-->G3):
X445FB
Title : CPU_PCH_SYS_POWER
Dept.: NB1-RD3EE1
Engineer: NB_EE
Date: Wednesday, July 17, 2019
Sheet 25 of 102

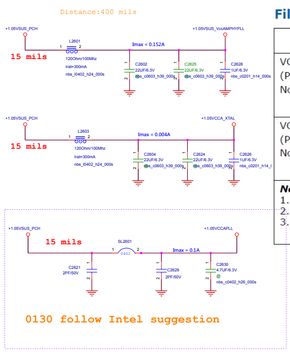


+1.05VSUS



Filter requirement for +1.05VSUS

LC size 0603->0402 DCR MAX 0.3 ohm 0126

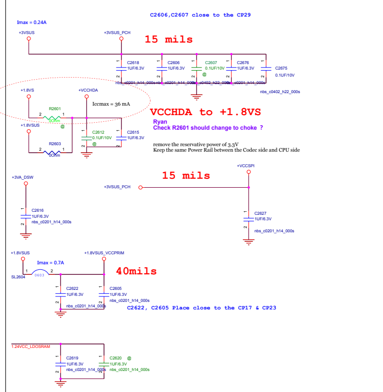


Filter Requirements for CFL U PCH

Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin F1) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin B22) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

Notes:
1. Placeholder is only. Does not need to be stuffed.
2. All capacitors are edge capacitors unless labeled otherwise.
3. 2x 22uF 0603 caps can optionally be used instead of 1x 47 uF 0603 caps. Caps should be with X5R temperature characteristics.

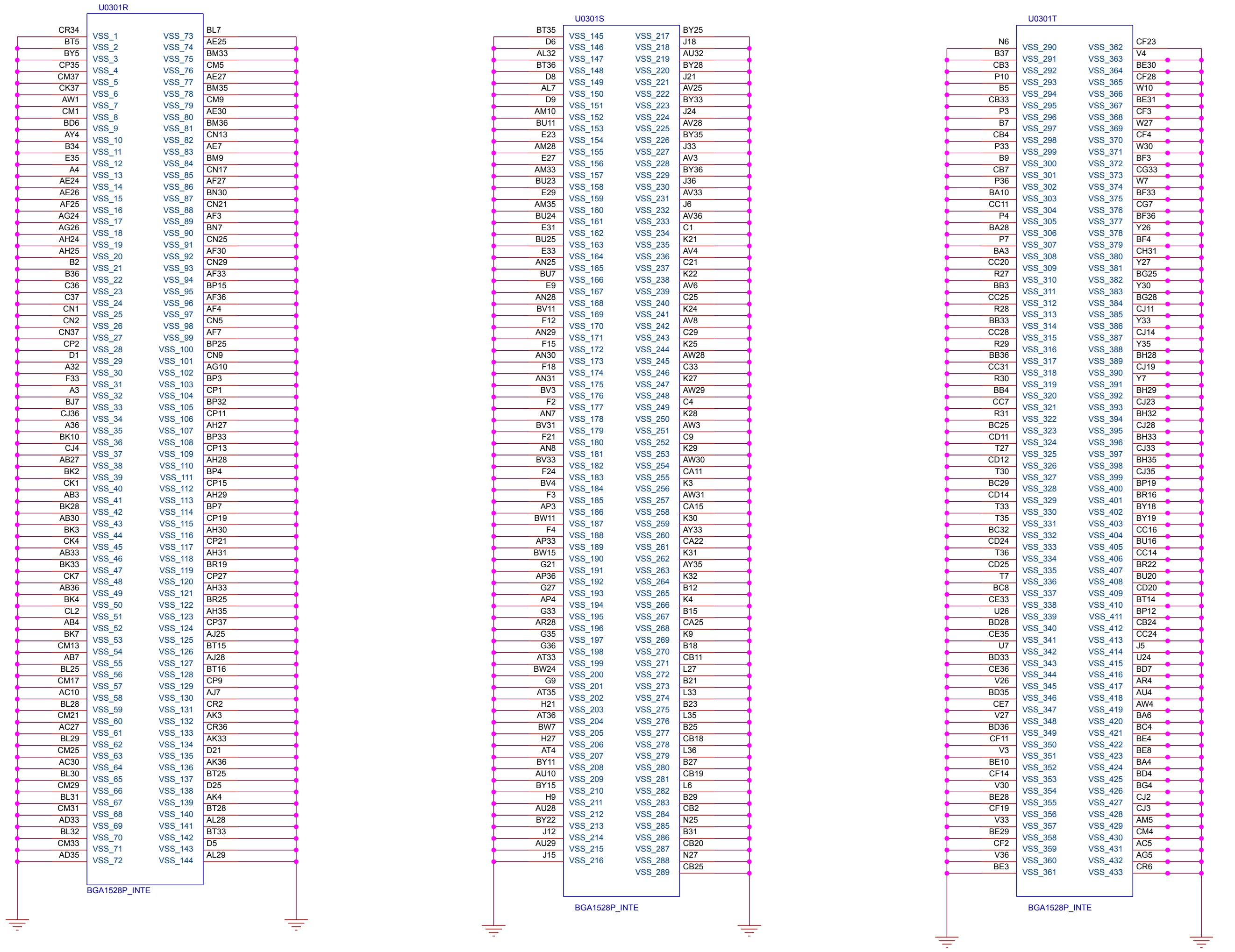
+3VSUS / +1.8VSUS



X445FB

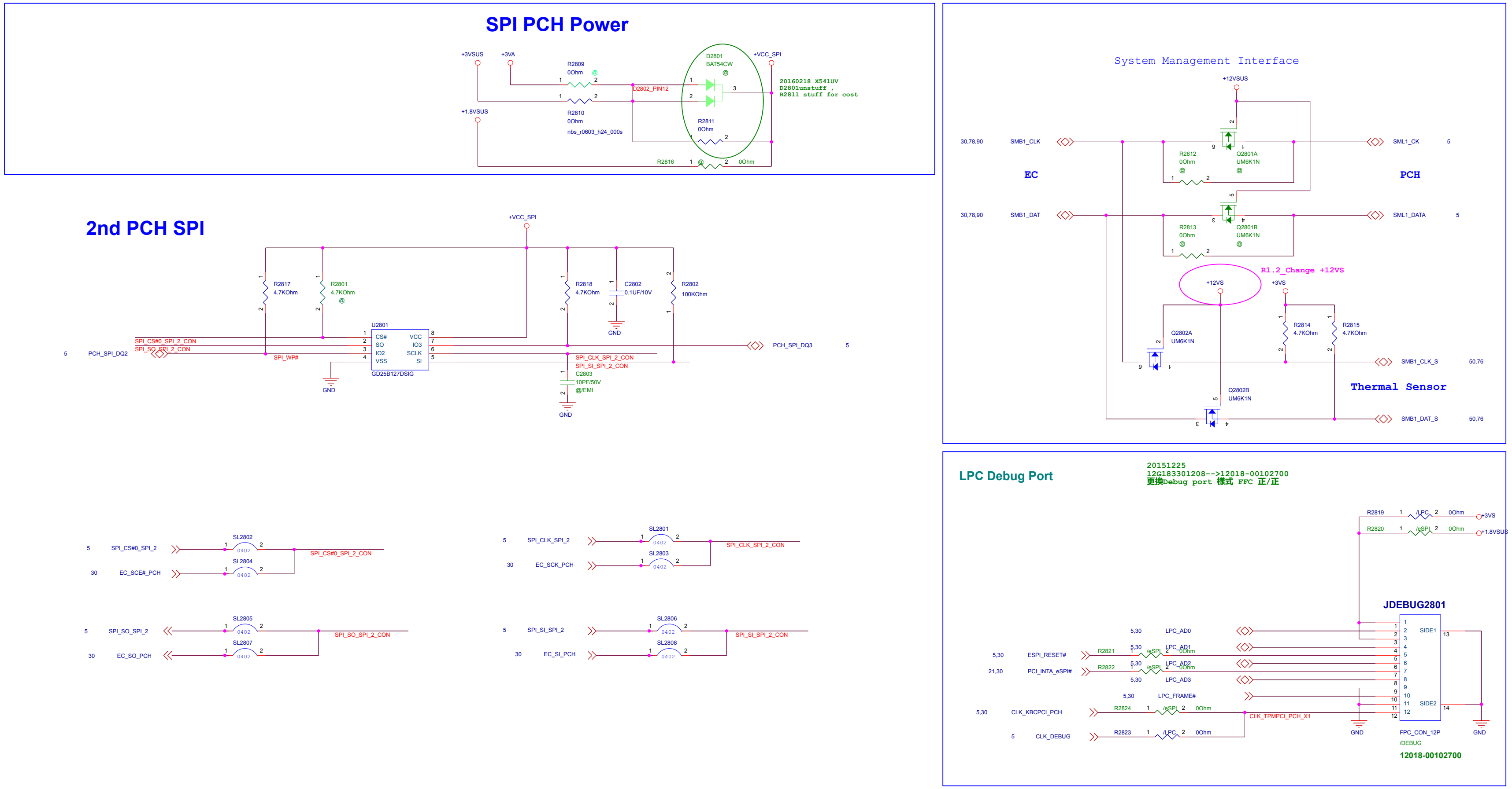
Title : CPU_PCH_POEWR,GND

Engineer: NB_EE

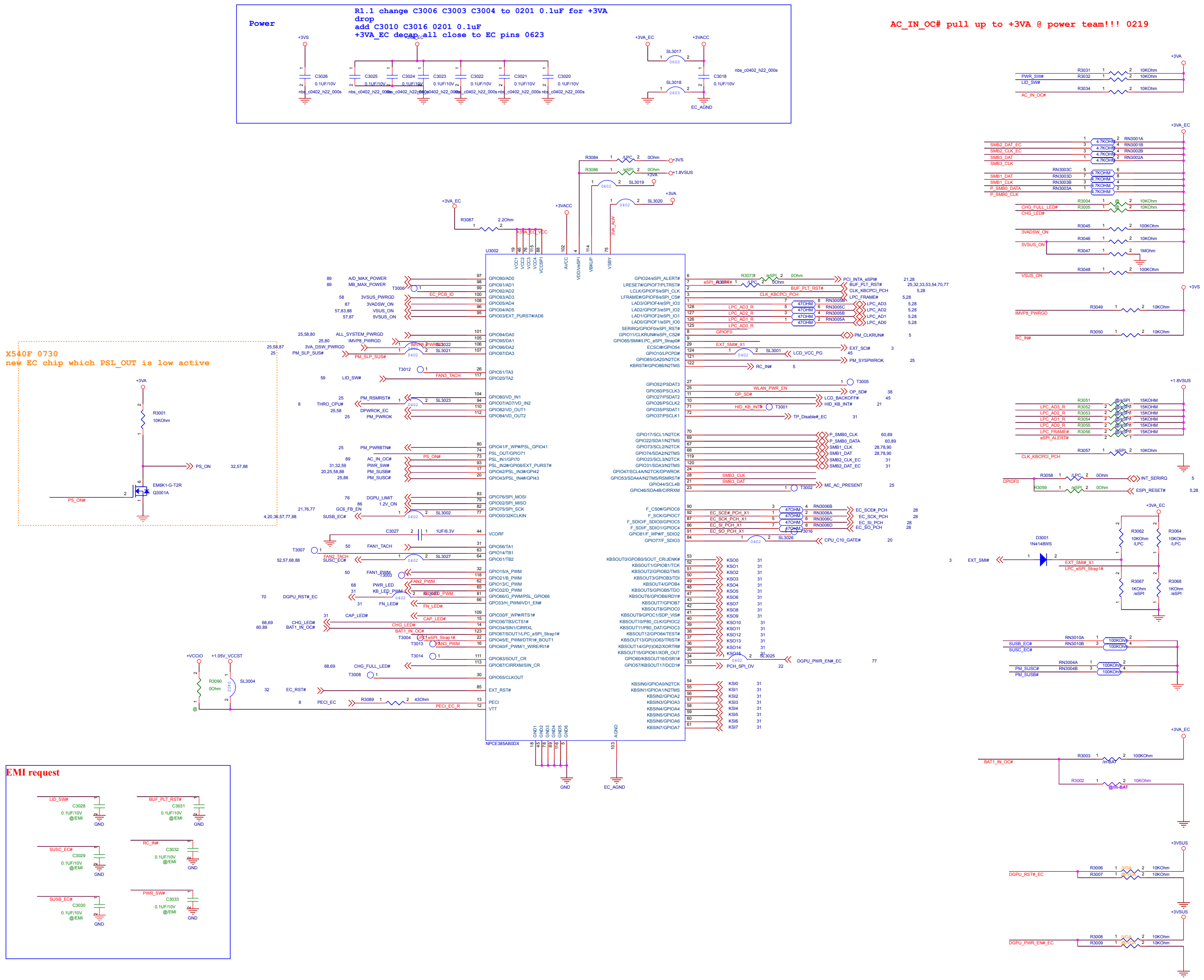


<Variant Name>

Project Name: X445FB		Rev: R1.0
Title : CPU_PCH_POEWR,GND		
Size: B	Dept.: NB1-RD3EE1	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 27 of 102	



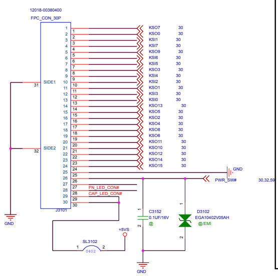
SPI PCH Power
2nd PCH SPI
System Management Interface
EC
PCH
Thermal Sensor
LPC Debug Port
20151225
12G183301208-->12018-00102700
更換Debug port 樣式 FFC 正/正
JDEBUG2801
12018-00102700
20160218 X541UV
D2801unstuff ,
R2811 stuff for cost
R1.2_Change +12VS

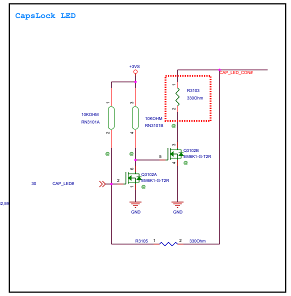


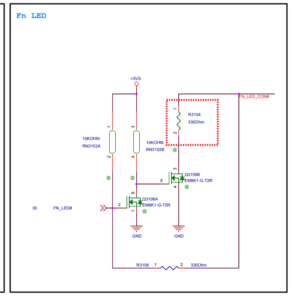
Power
R1.1 change C3006 C3003 C3004 to 0201 0.1uF for +3VA drop
add C3010 C3016 0201 0.1uF
+3VA_EC decap all close to EC pins 0623
AC_IN_OC# pull up to +3VA @ power team!!! 0219
X540F 0730
new EC chip which PSL_OUT is low active
EMI request
NPCE385A8DX

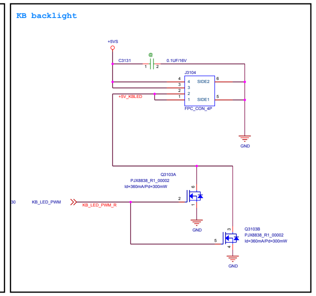
Main Board

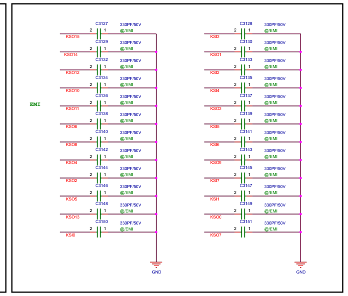
Internal Keyboard

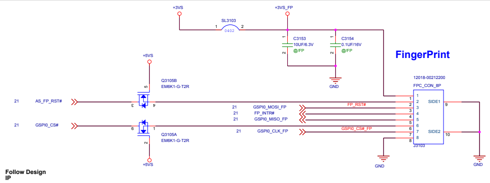


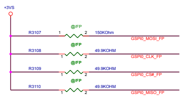


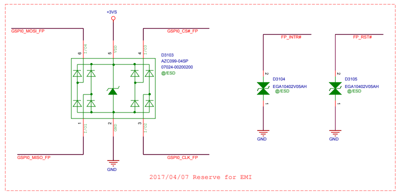






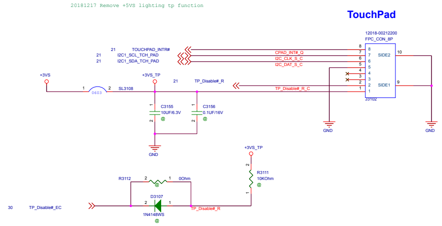






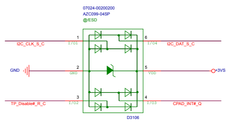
CN1	
PIN NO.	PIN DEFINE*
1	VDD_3.3V_TP
2	GND
3	PS2_CLK
4	PS2_DATA
5	GND
6	SDA
7	SCL
8	INT

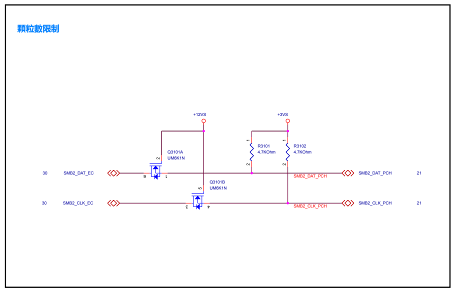
CN2	
PIN NO.	PIN DEFINE*
1	VDD_3.3V_FP
2	FP_RSTN
3	FP_MOSI
4	FP_INTN
5	FP_MISO
6	FP_CSN
7	FP_SCK
8	GND

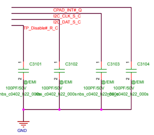


USB Finger printer (Reserved)

PIN NO.	PIN DEFINE*
1	VDD_3.3V
2	NC
3	D-
4	D+
5	GND
6	I2C_DATA
7	I2C_CLK
8	TOUCH -INT*



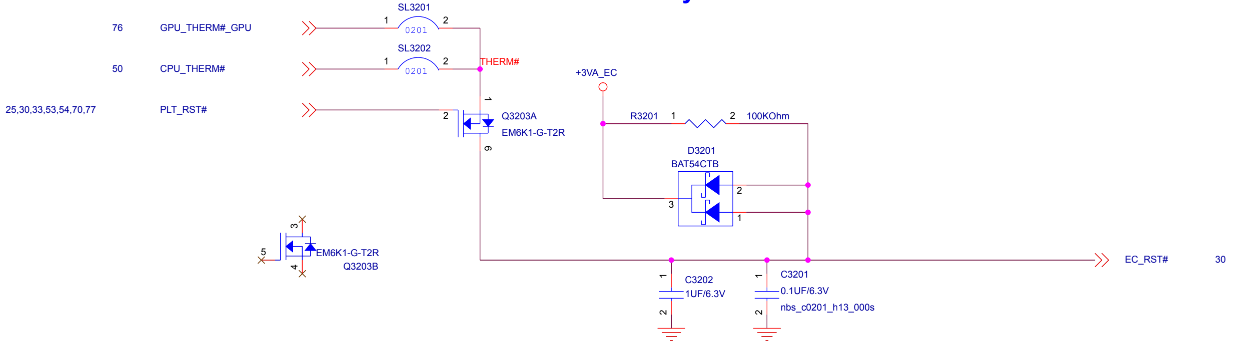




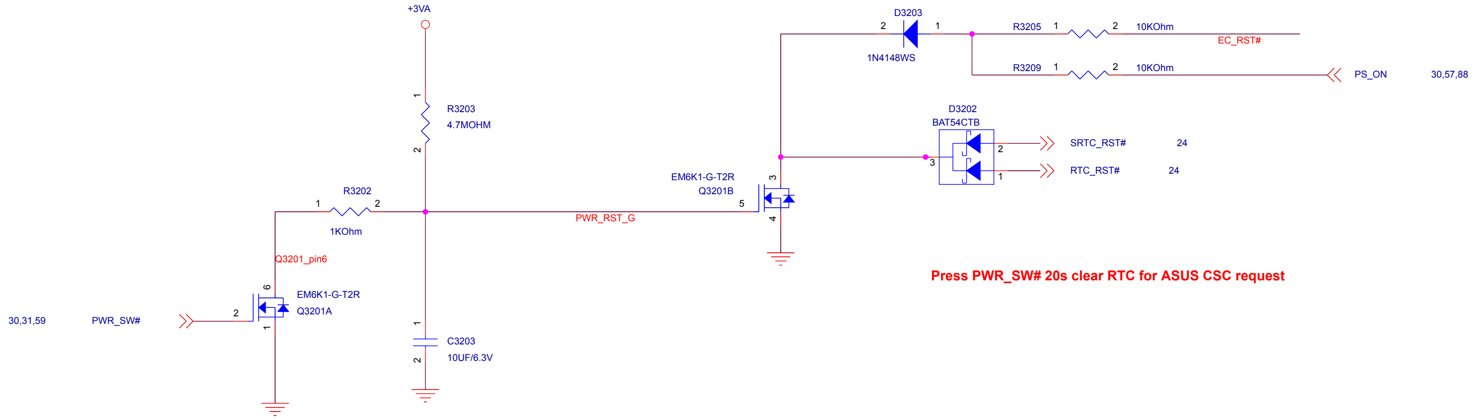
BOM

Project Name: X445FB		Rev: R1.0
Title : EC-IT8995_KB,TP		
Size: E	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 31 of 102	

Thermal Policy



battery embedded (press pwr_sw 40sec, then reset ec & RTC)



<Variant Name>

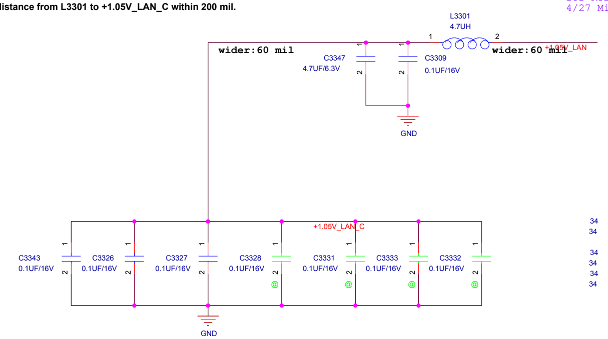
Title

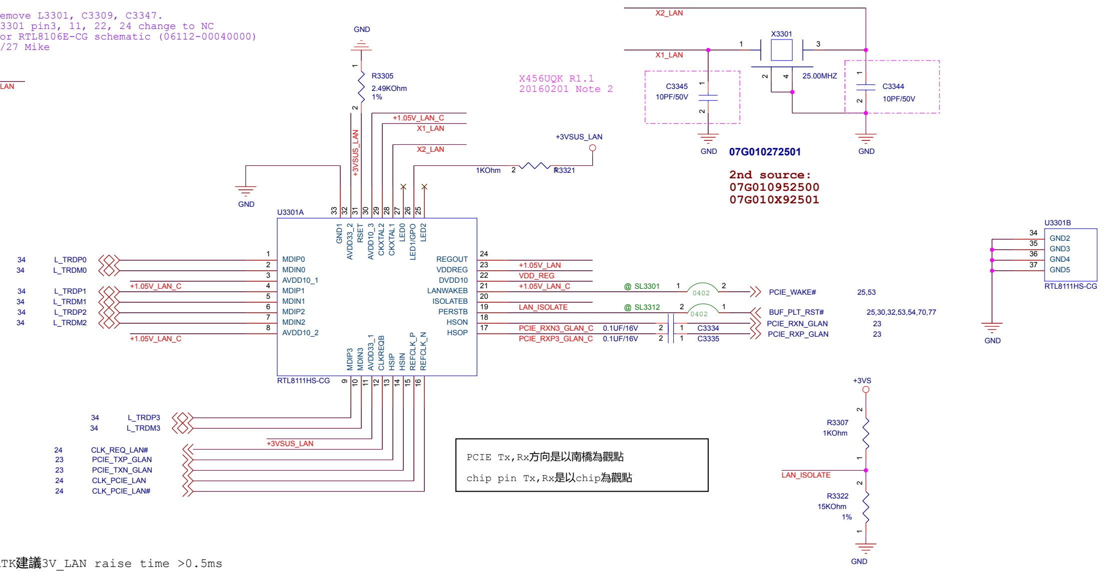
Engineer

ASUSTeK COMPUTER INC. NB4

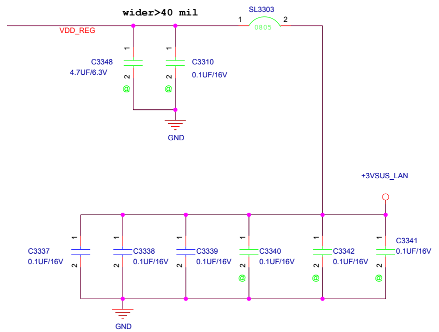
The distance from u3301.36 to L3301 within 200 mil.

The distance from L3301 to +1.05V_LAN_C within 200 mil.

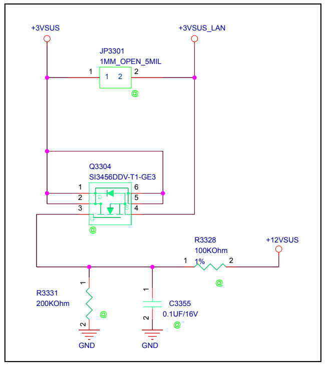




The distance from U3301.34, U3301.35 , VDD_REG net to SL3303 within 200 mil.



RTK建議3V_LAN raise time >0.5ms



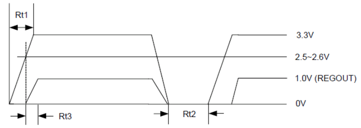


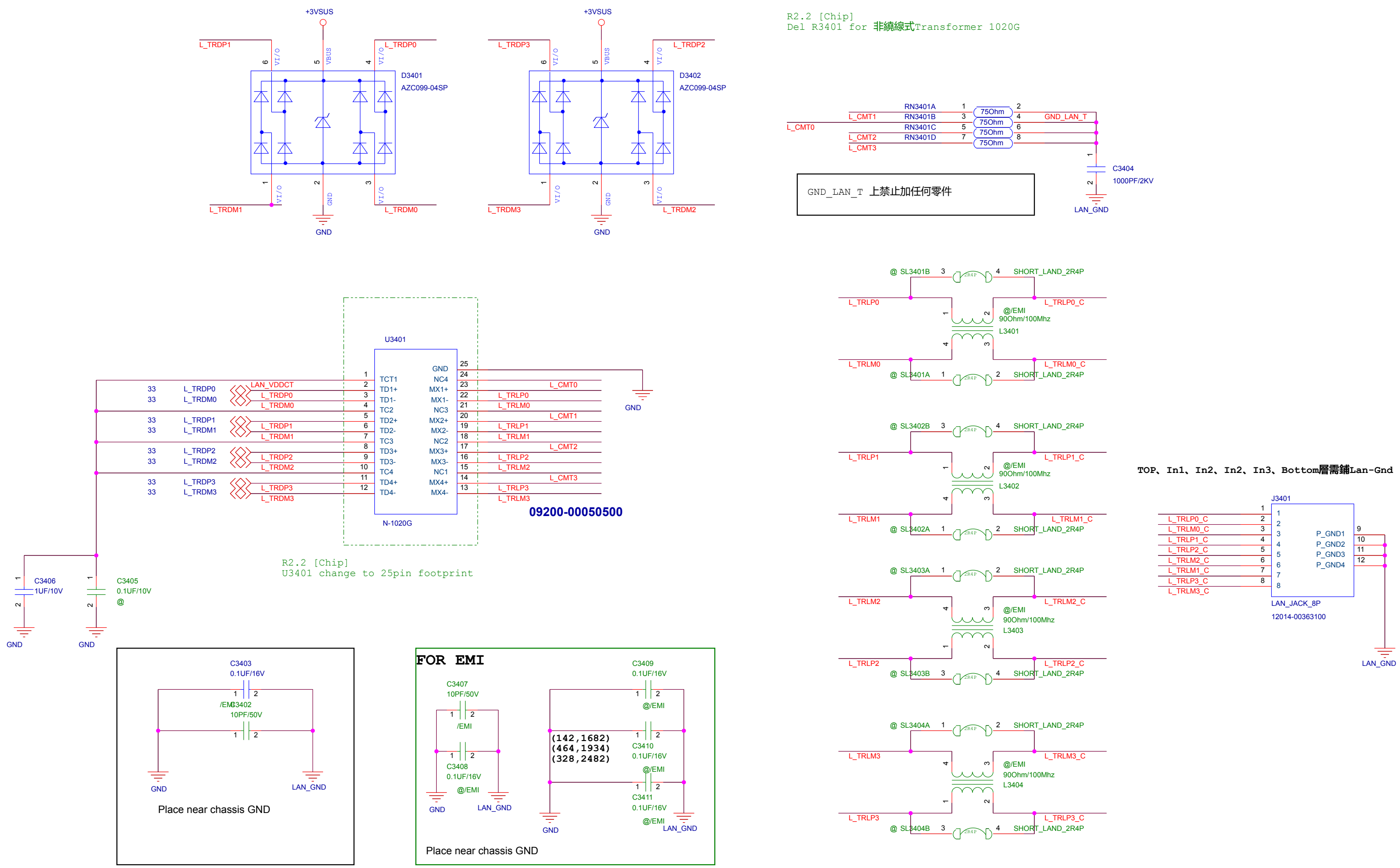
Figure 3. Power Sequence

Table 17. Power Sequence Parameter

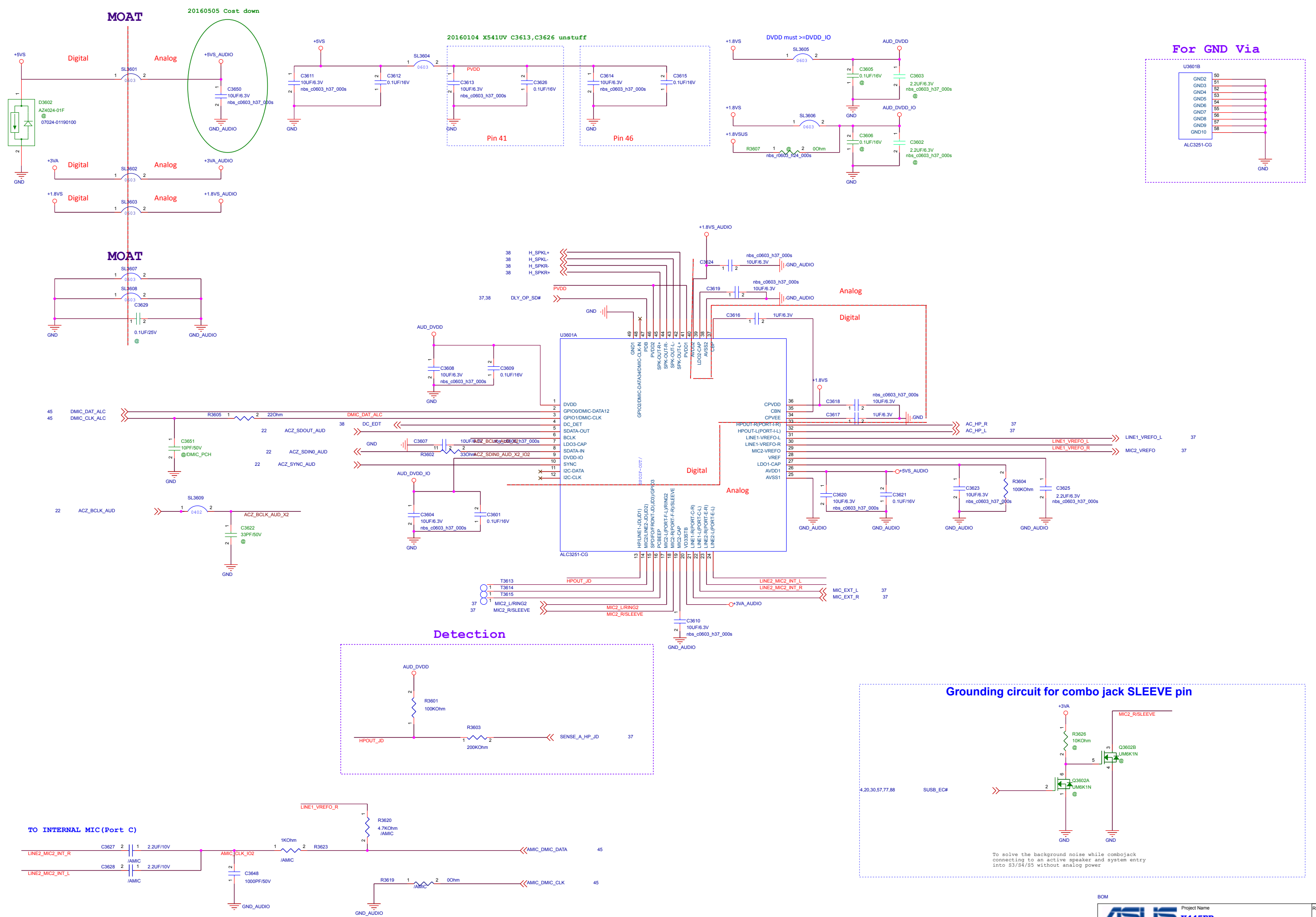
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

RJ45 con.



+3VSUS
D3401
AZC099-04SP
D3402
AZC099-04SP
R2.2 [Chip]
Del R3401 for 非繞線式Transformer 1020G
RN3401A
RN3401B
RN3401C
RN3401D
75Ohm
L_CMT0
L_CMT1
L_CMT2
L_CMT3
GND_LAN_T
C3404
1000PF/2KV
LAN_GND
GND_LAN_T 上禁止加任何零件
U3401
N-1020G
09200-00050500
R2.2 [Chip]
U3401 change to 25pin footprint
C3406
1UF/10V
C3405
0.1UF/10V
GND
C3403
0.1UF/16V
C3402
10PF/50V
Place near chassis GND
FOR EMI
C3407
10PF/50V
C3408
0.1UF/16V
C3409
0.1UF/16V
C3410
0.1UF/16V
C3411
0.1UF/16V
@/EMI
(142,1682)
(464,1934)
(328,2482)
Place near chassis GND
SHORT_LAND_2R4P
90Ohm/100Mhz
L3401
L3402
L3403
L3404
TOP、In1、In2、In2、In3、Bottom層需鋪Lan-Gnd
J3401
LAN_JACK_8P
12014-00363100



BOM

Project Name: X445FB		Rev R1.0
Title : HDD Board-AUD-ALC3236		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 36 of 102	

Universal Jack (Normal open type)

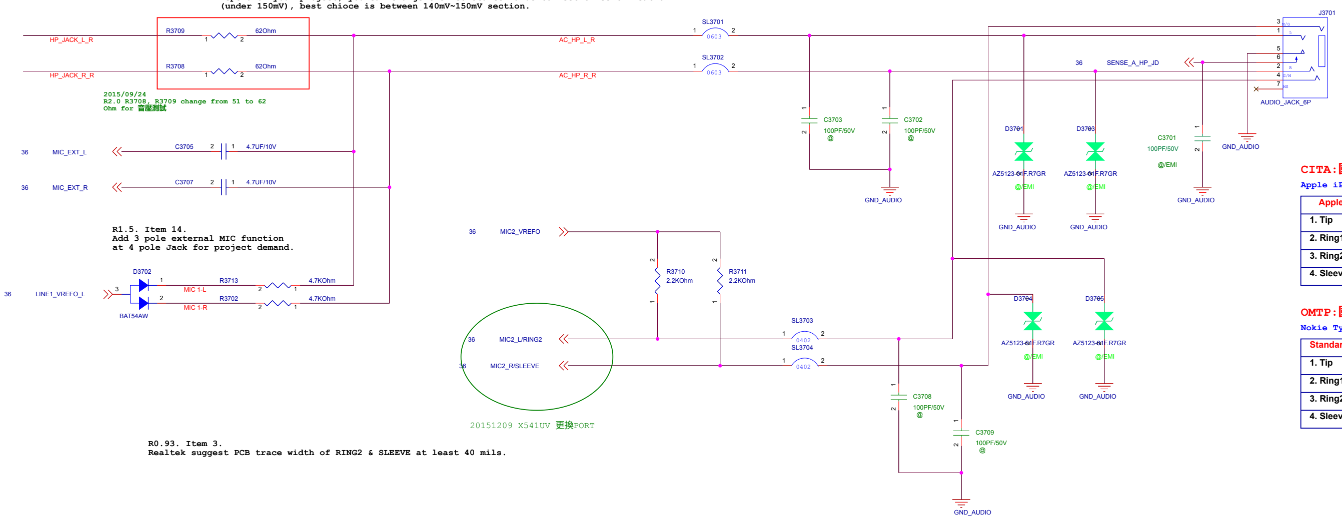
R1.3. Item 12.
Add 4 pole headset jack normal
open type for project demand.

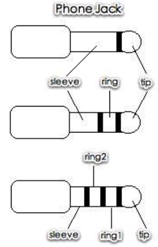
• 尺寸：一般分三種規格，2.5mm、3.5mm、6.35mm。
• 種類：一般分也三種規格，TS 端子 (Mono)、TRS 端子 (Stereo)、TRRS 端子 (Stereo + Mic/Video)。

R1.4. Item 13.
Recommand the HP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification
(under 150mV), best chioce is between 140mV~150mV section.

2015/09/24
R2.0 R3708, R3709 change from 51 to 62
Ohm for 音壓測試

R1.5. Item 14.
Add 3 pole external MIC function
at 4 pole Jack for project demand.





CITA：國際標準

Apple iPhone/HTC/小米 的 Phone Jack 定義：

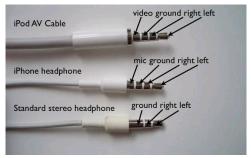
Apple	iPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mic	Video

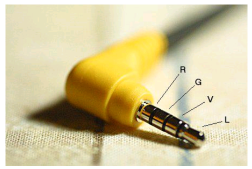
OMTP：國家標準

Nokie Type 的 Phone Jack 定義：

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel

R0.93. Item 3.
Realtek suggest PCB trace width of RING2 & SLEEVE at least 40 mils.



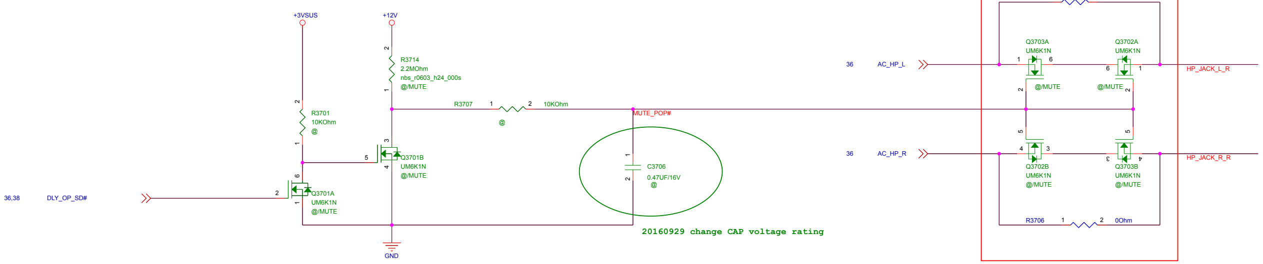


耳機pop noise mute線路

MUTE CONTROL

20151215 +3VS Change to +1.8VS

MUTE CONTROL



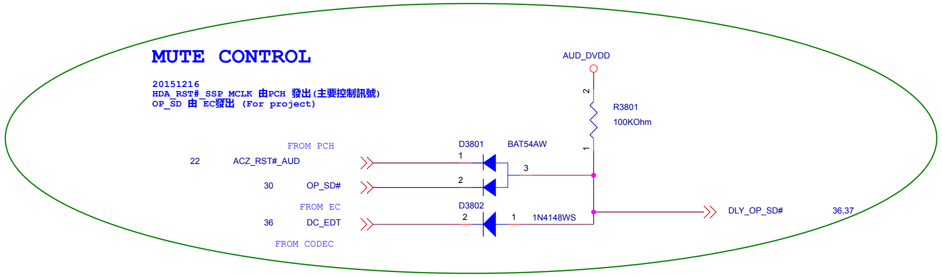
20160929 change CAP voltage rating

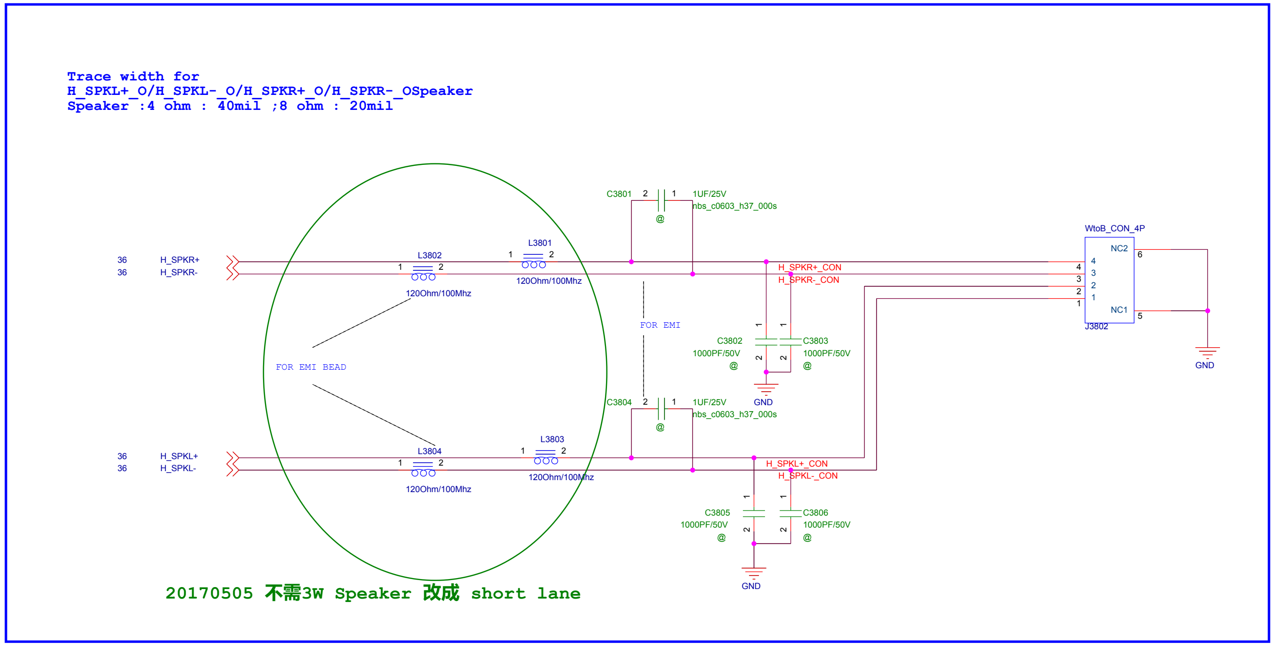
BOM

Project Name

Rev

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD





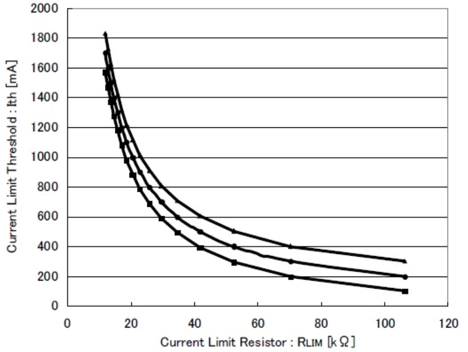
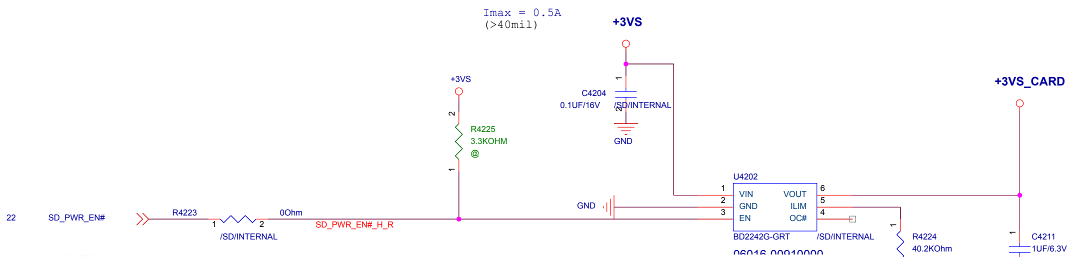


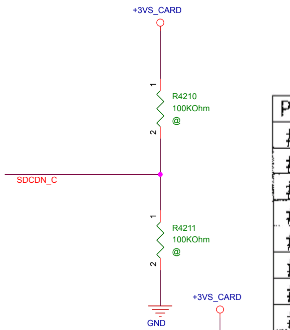
Figure 45. Ith vs. RLIM graph

3.3V POWER SD CARD POWER

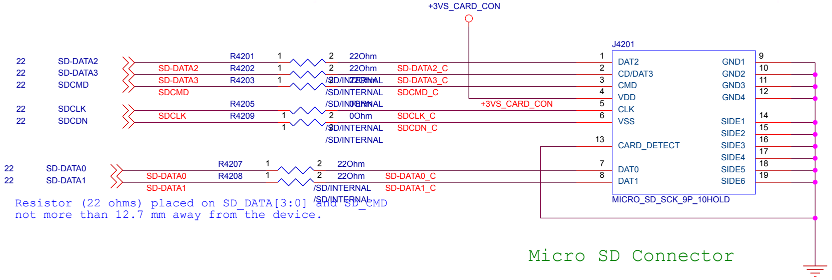


7.14.2.2 SD_VDD1_PWR_EN Polarity

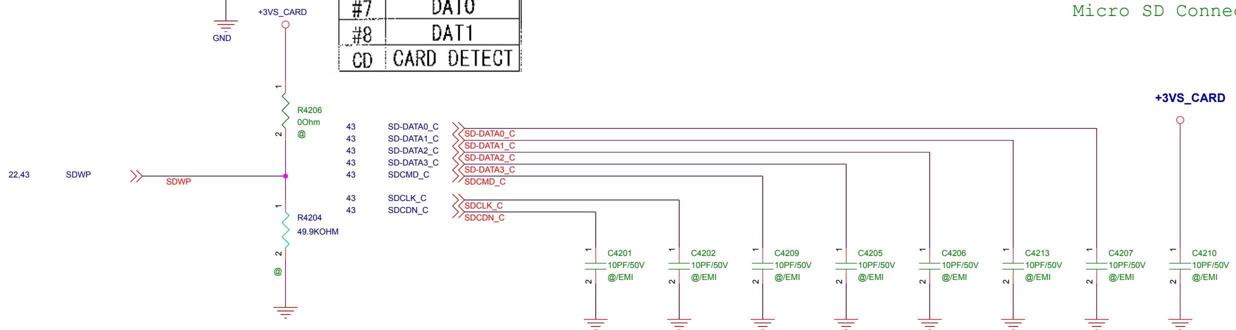
Signal SD card power enable (SD_VDD1_PWR_EN#) assertion logic can be changed by BIOS. In default BIOS implementation this signal has an Active High assertion logic.



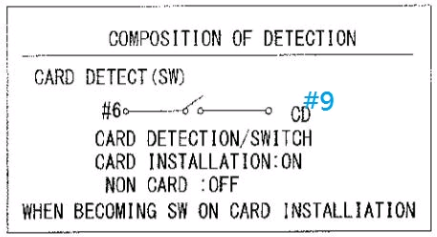
PIN	SD mode
#1	DAT2
#2	DAT3/CD
#3	CMD
#4	V_{DD}
#5	CLK
#6	Vss
#7	DAT0
#8	DAT1
CD	CARD DETECT



Micro SD Connector



EMI



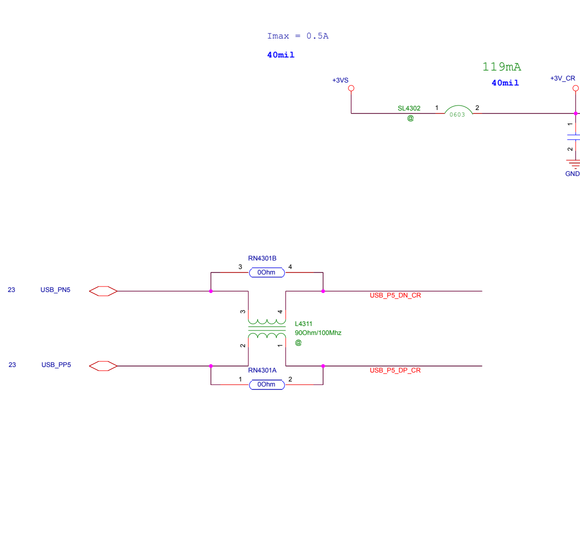
BOM

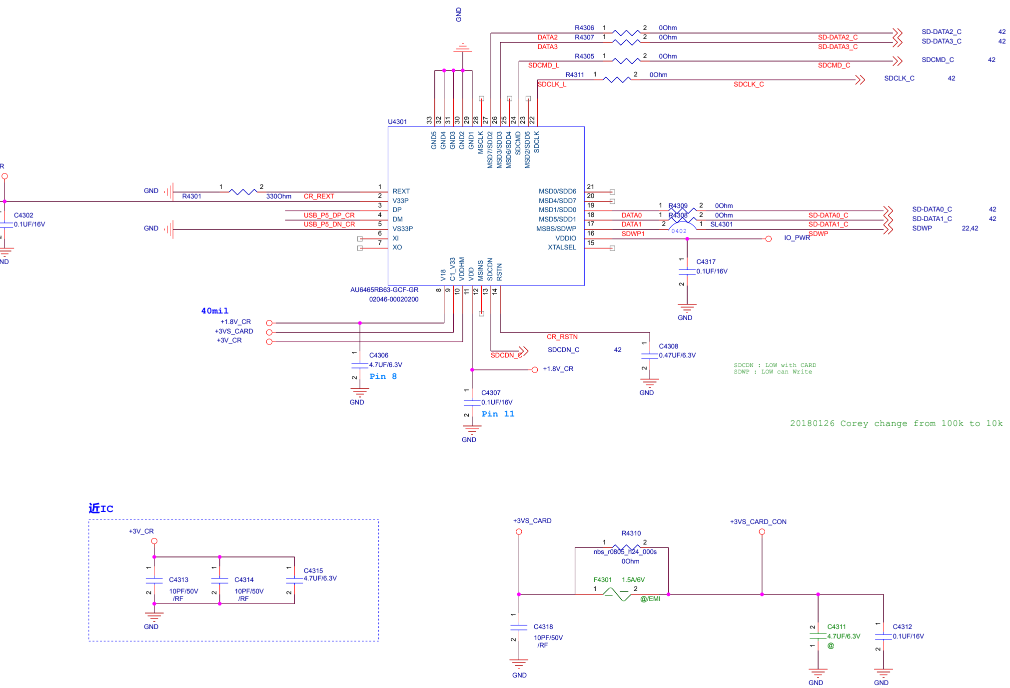
ASUS	Project Name: X508F	Rev: R1.0
Title :	CARD READER CONNECTOR	
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 42	of 102

USB Card Reader

AU6465

	mode	Vin (V)	Lin (mA)	mW
AU6465 (Enable Power saving mode)	Suspend with card	3.3V	0.33	1.1
	Suspend without card	3.3V	0.14	0.46
	Idle with card	3.3V	32.8	108.24
	Idle without card	3.3V	0.14	0.46
	operating	3.3V	119	392.7
Use SanDisk SDHC 8G card (Extreme Pro)				

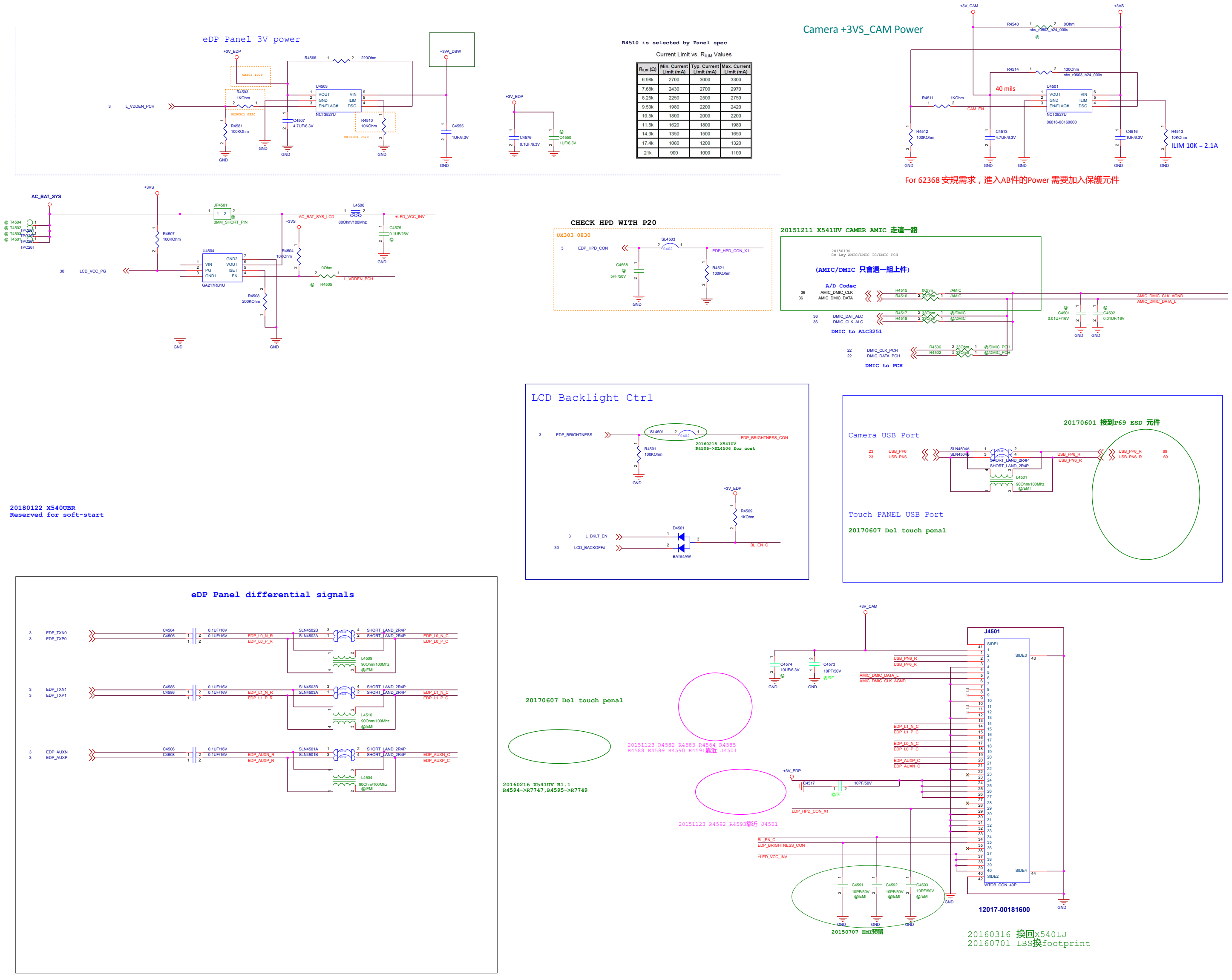




<Variant Name>

ASUSTeK COMPUTER INC.	Title : IO_BD-2(AU6465RB63)	
	Engineer: EE	
Size: Custom	Project Name: UX310UV	Rev: 1.0
Date: Wednesday, July 17, 2019	Sheet 43 of 102	

eDP (LVDS) Panel

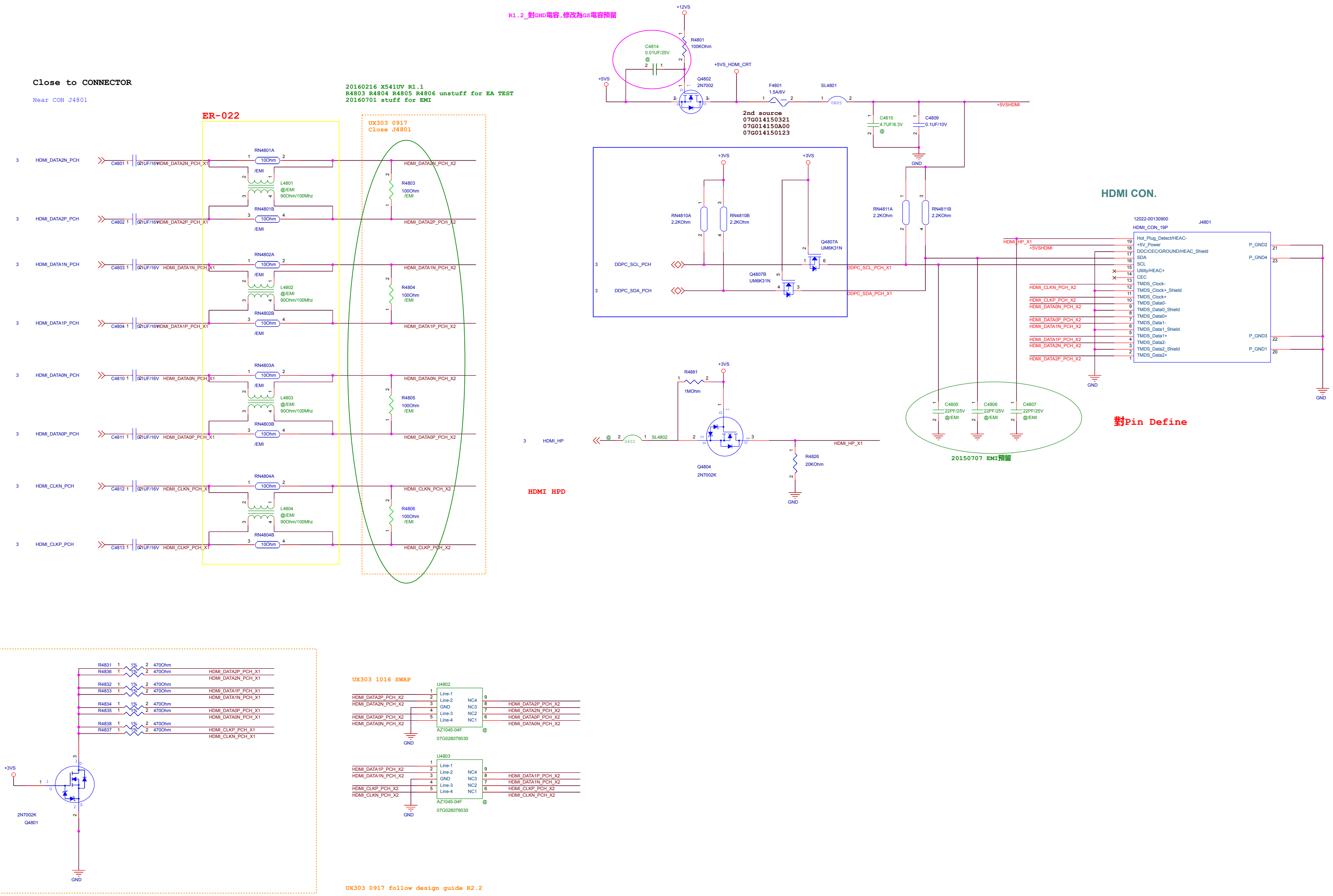


R4510 is selected by Panel spec

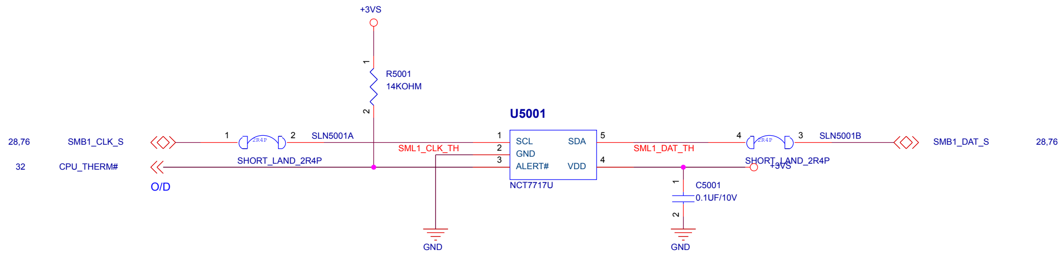
Current Limit vs. R_{ILIM} Values

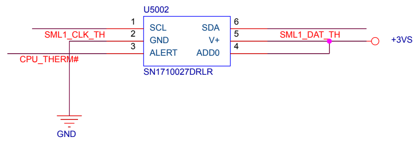
R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.98k	2700	3000	3300
7.68k	2430	2700	2970
8.25k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1200	1320
21k	900	1000	1100

HDMI type-A


R1.2_對GND電容,修改為GS電容預留
Close to CONNECTOR
Near CON J4801
ER-022
20160216 X541UV R1.1
R4803 R4804 R4805 R4806 unstuff for EA TEST
20160701 stuff for EMI
UX303 0917
Close J4801
2nd source
07G014150321
07G014150A00
07G014150123
HDMI CON.
HDMI_CON_19P
J4801
HDMI HPD
20150707 EMI預留
對Pin Define
UX303 1016 SWAP
U4802
U4803
AZ1045-04F
UX303 0917 follow design guide R2.2
HDMI_DATA2N_PCH
HDMI_DATA2P_PCH
HDMI_DATA1N_PCH
HDMI_DATA1P_PCH
HDMI_DATA0N_PCH
HDMI_DATA0P_PCH
HDMI_CLKN_PCH
HDMI_CLKP_PCH
DDPC_SCL_PCH
DDPC_SDA_PCH
HDMI_HP
+5VSHDMI
GND

CPU Thermal Sensor





5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

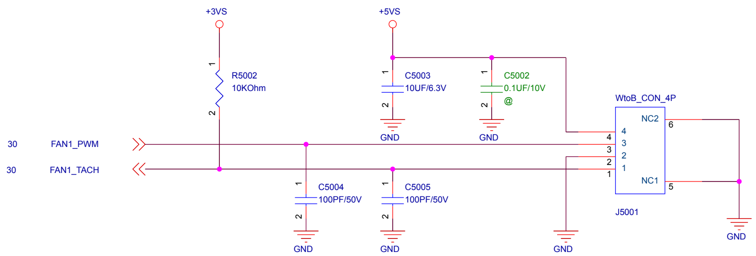
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

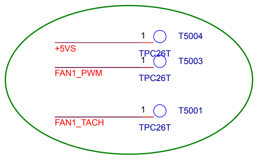
PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

-----------------OTHER SIGNALS
10 mils
===============GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
--------------------OTHER SIGNALS
Avoid FSB,Power

DC FAN Control





請將測點至於TOP面
R2.0 新增_Tim_20150820

<Variant Name>

ASUSTeK COMPUTER INC. NB3

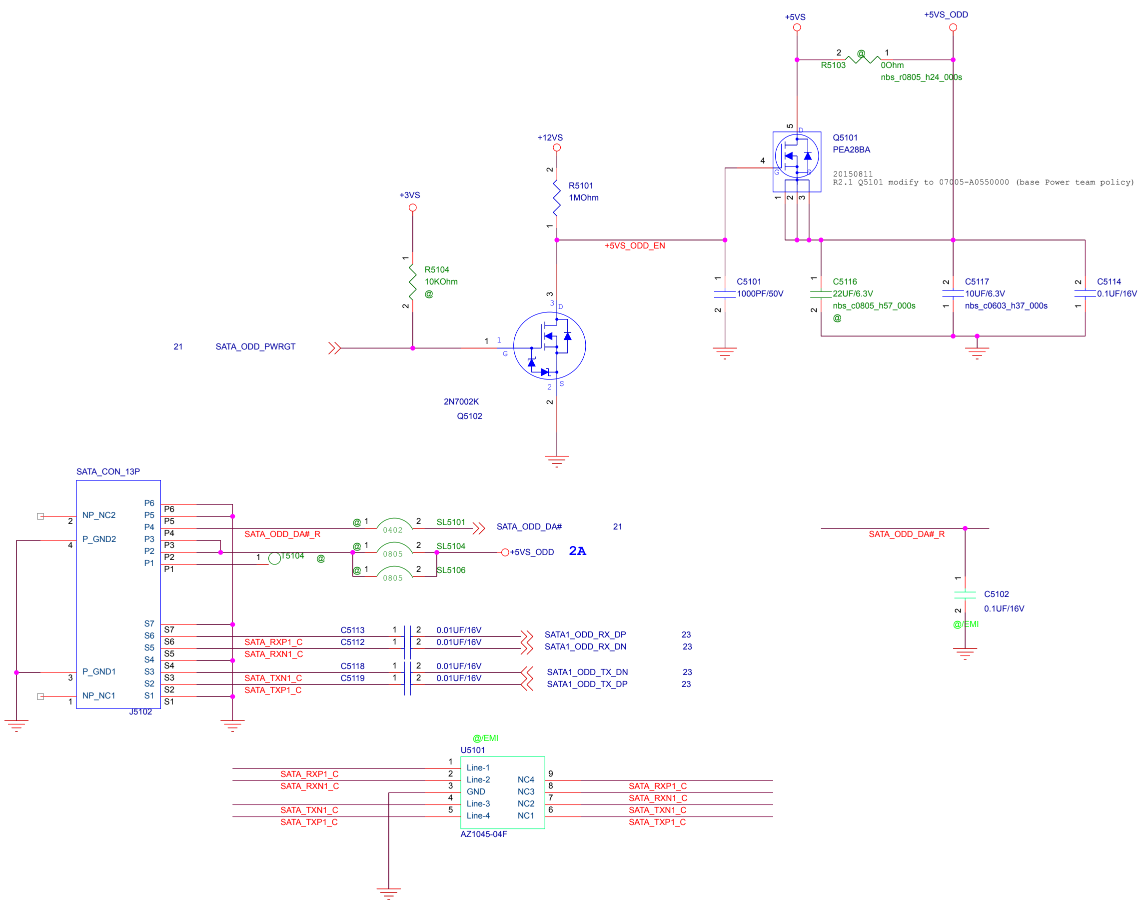
Title : 50_FAN_Thermal Sensor

Engineer: NB_EE

Size	Project Name	Rev
B	X445FB	R1.0

Date: Wednesday, July 17, 2019 Sheet 50 of 102

SATA ODD CONN.



BOM

Project Name **X445FB**

Title : SATA HDD & ODD

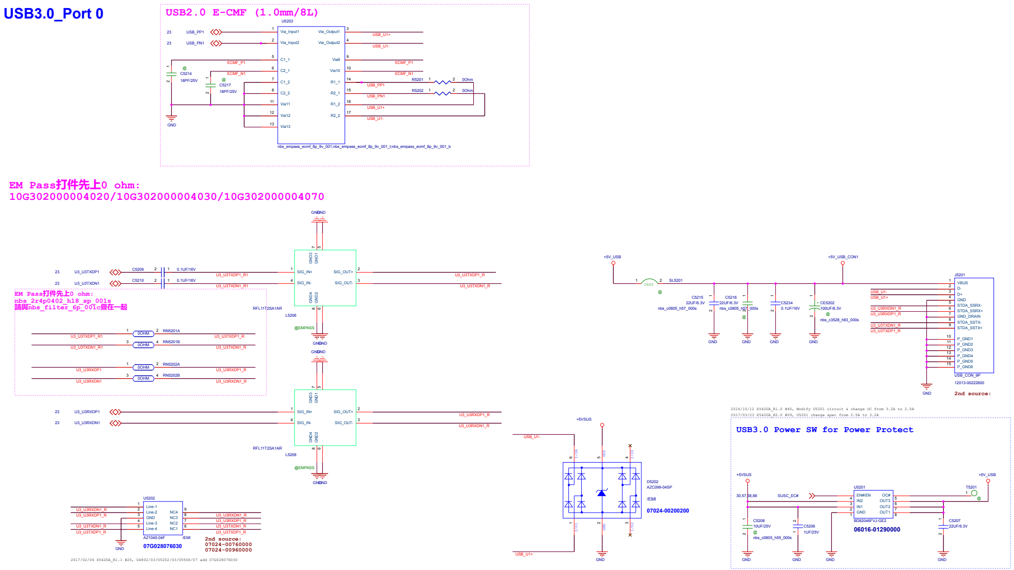
Size B

Dept.: ASUSTeK COMPUTER INC. **Engineer:** NB_

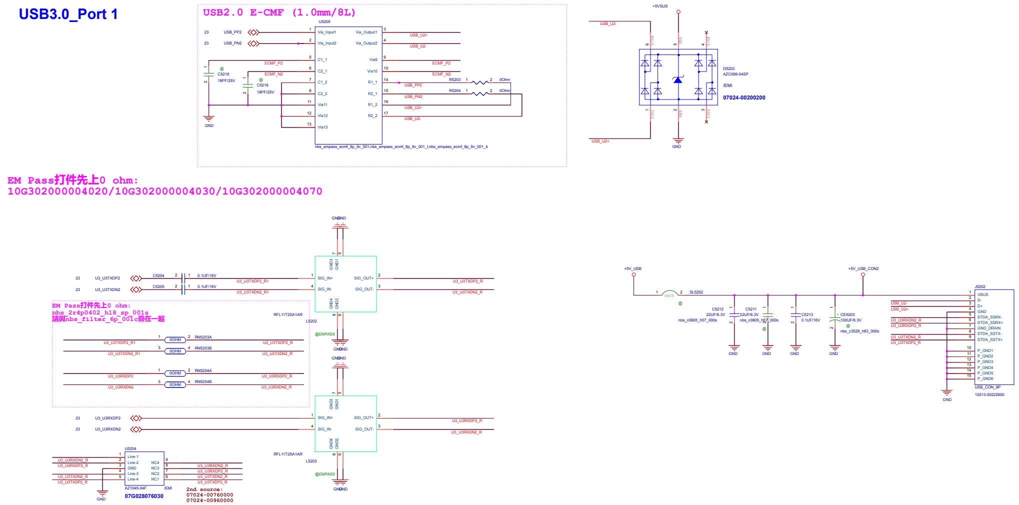
Date: Wednesday, July 17, 2019

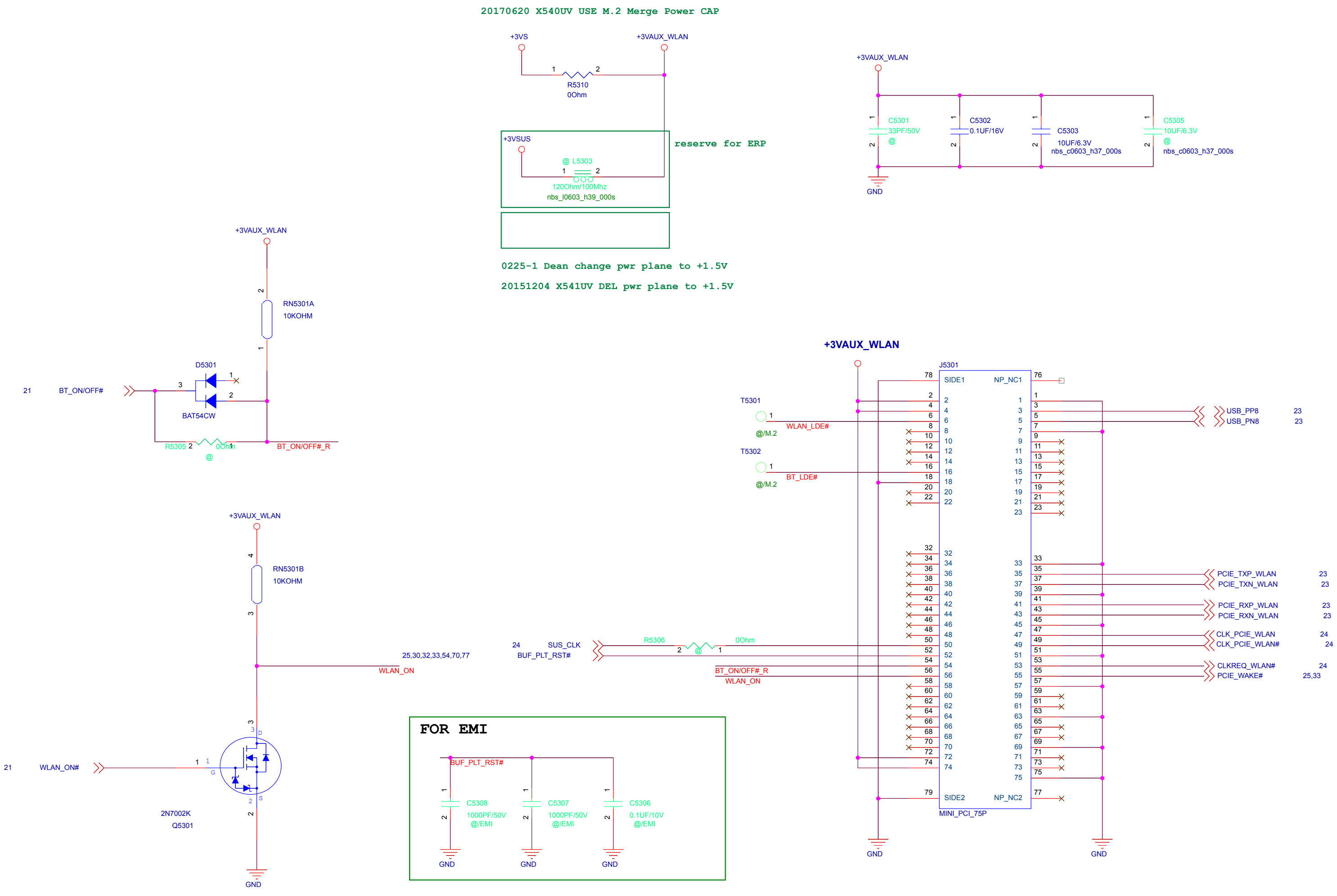
Sheet 51

USB3.0_Port 0



USB3.0_Port 1



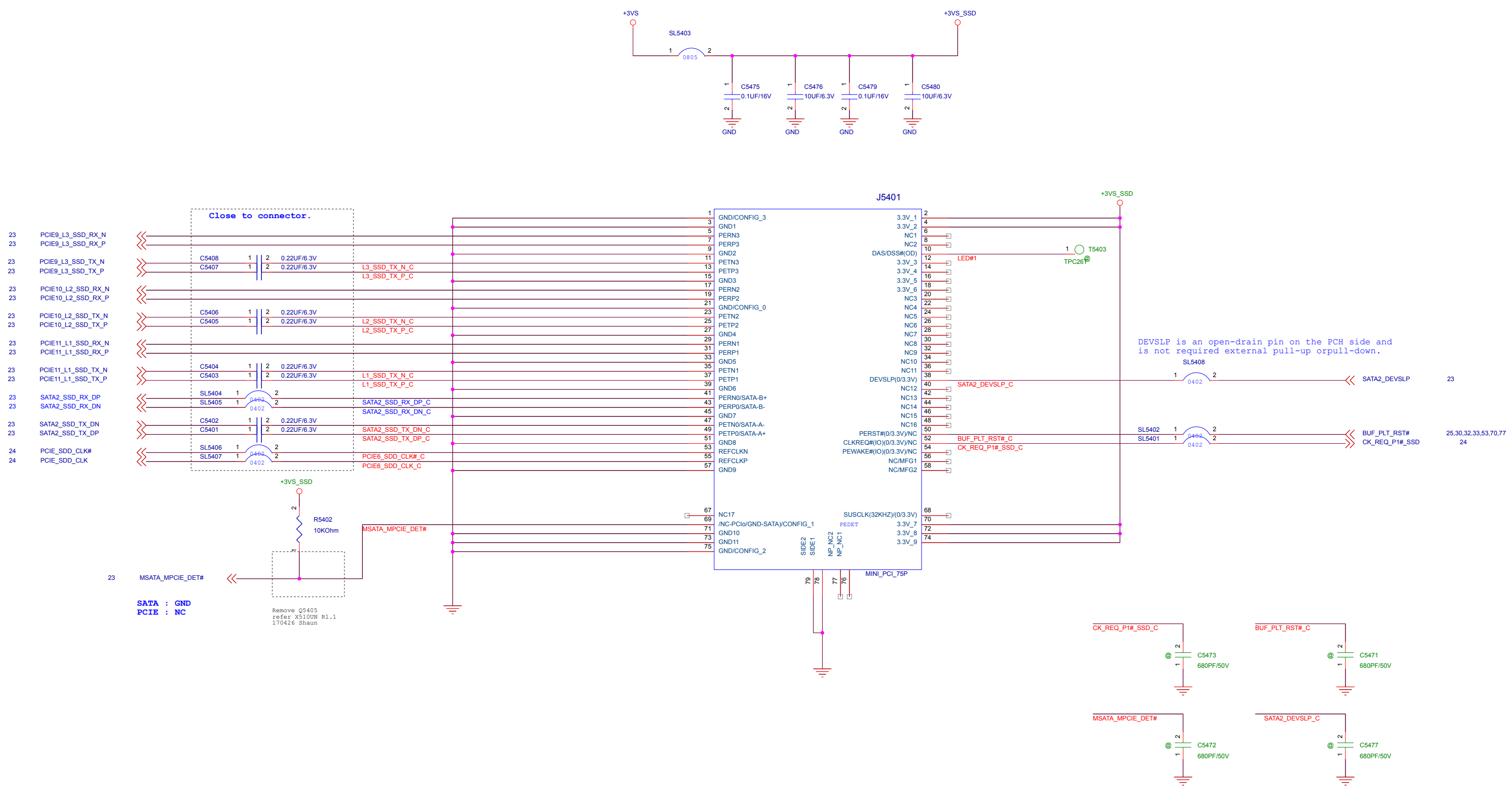


20170620 X540UV USE M.2 Merge Power CAP
+3VS
+3VAUX_WLAN
R5310
0Ohm
+3VSUS
@ L5303
120Ohm/100Mhz
nbs_l0603_h39_000s
reserve for ERP
0225-1 Dean change pwr plane to +1.5V
20151204 X541UV DEL pwr plane to +1.5V
C5301
33PF/50V
C5302
0.1UF/16V
C5303
10UF/6.3V
nbs_c0603_h37_000s
C5305
10UF/6.3V
GND
RN5301A
10KOHM
D5301
BAT54CW
BT_ON/OFF#
R5305
0Ohm
BT_ON/OFF#_R
RN5301B
10KOHM
25,30,32,33,54,70,77
WLAN_ON
WLAN_ON#
2N7002K
Q5301
FOR EMI
BUF_PLT_RST#
C5308
1000PF/50V
@/EMI
C5307
1000PF/50V
@/EMI
C5306
0.1UF/10V
@/EMI
J5301
SIDE1
NP_NC1
SIDE2
NP_NC2
MINI_PCI_75P
T5301
@/M.2
WLAN_LDE#
T5302
BT_LDE#
SUS_CLK
R5306
USB_PP8
USB_PN8
PCIE_TXP_WLAN
PCIE_TXN_WLAN
PCIE_RXP_WLAN
PCIE_RXN_WLAN
CLK_PCIE_WLAN
CLK_PCIE_WLAN#
CLKREQ_WLAN#
PCIE_WAKE#
25,33

0915-1 Dean
0915-2 Dean
0922-6 Dean
1003-4 rick

Main Board

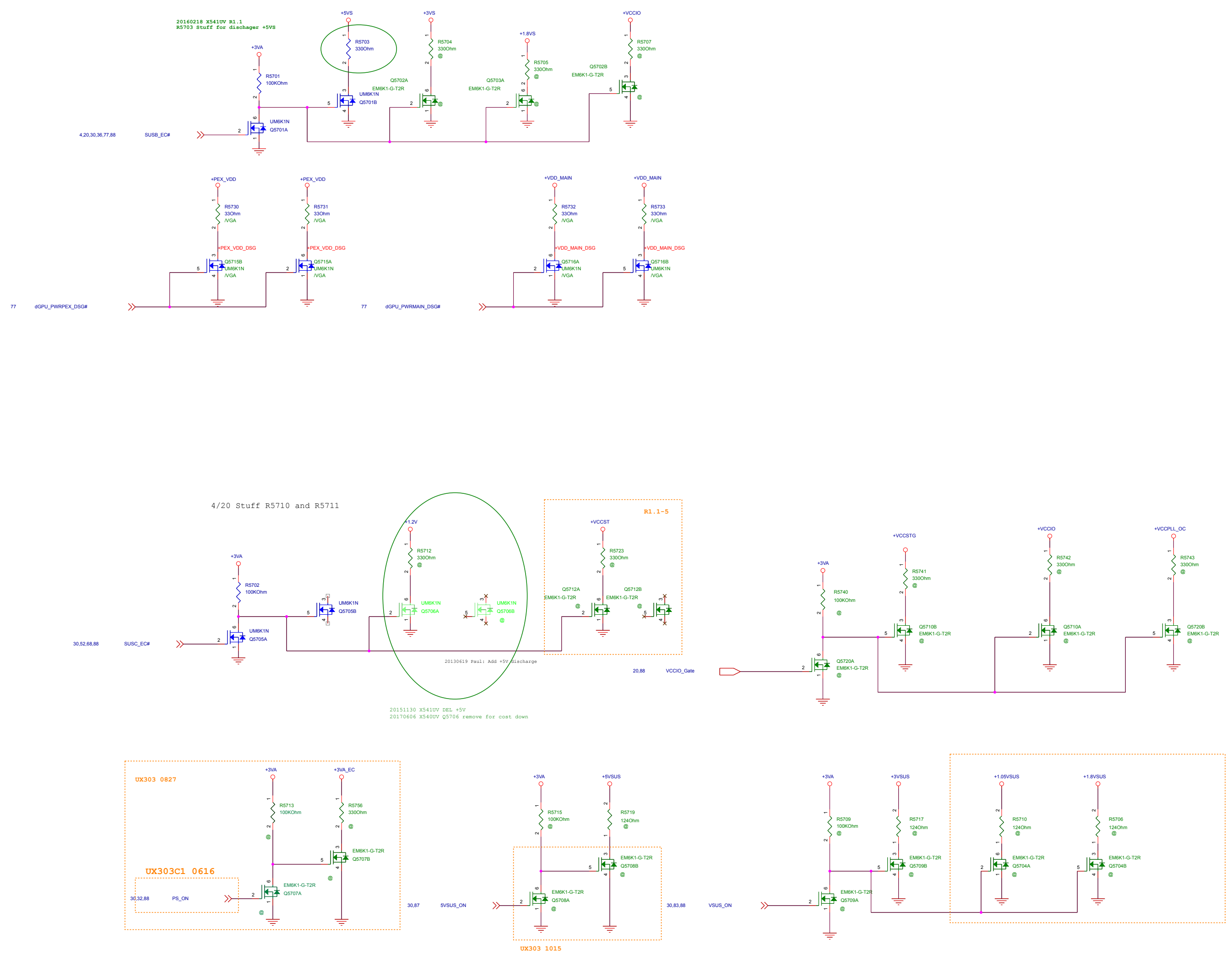
1109-4 rick



<Variant Name>

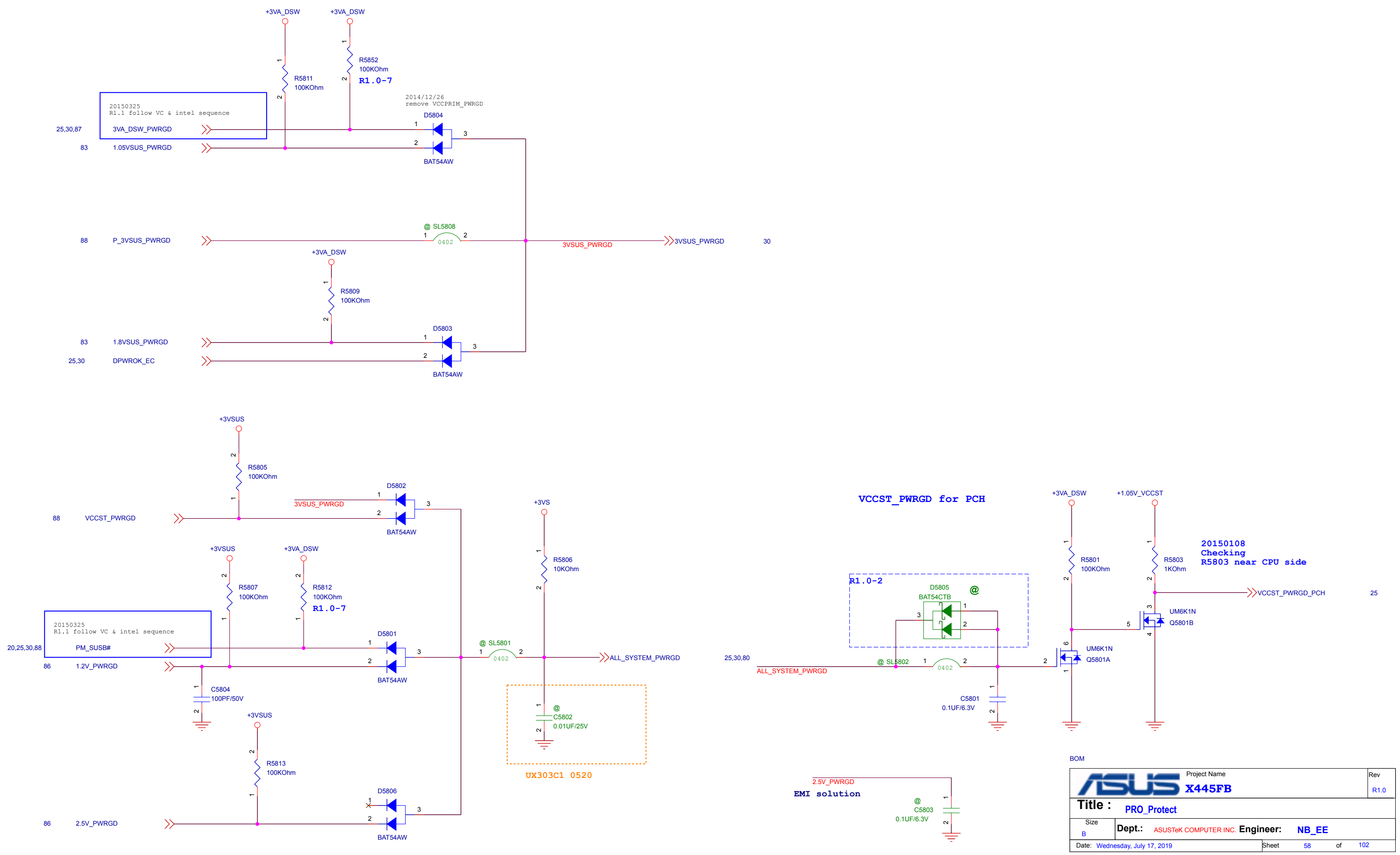
ASUSTeK COMPUTER INC.	Title : NGFF(KEY-M)_SSD		
	Engineer: NB_EE		
Size: Custom	Project Name: X445FB		Rev: R1.0
Date: Wednesday, July 17, 2019	Sheet 54 of 102		

Main Board



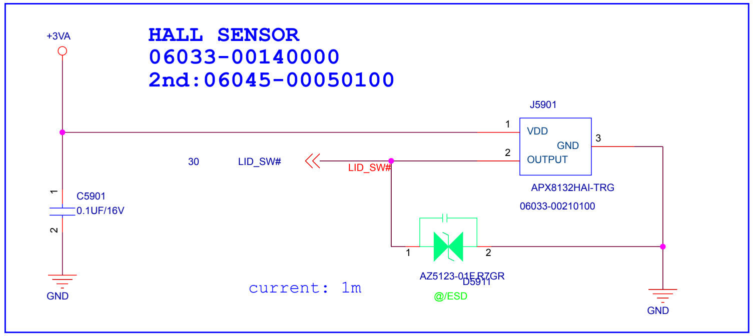
BOM

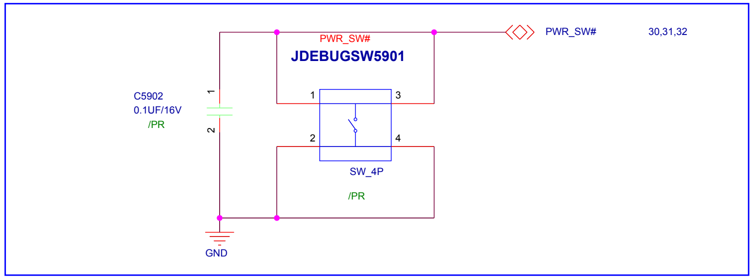
Project Name X445FB		Rev. R1.0
Title : DSG_Discharge		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 57	of 102



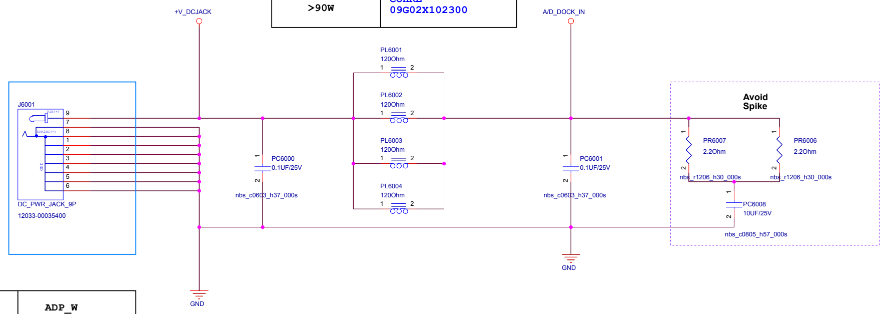
+3VA_DSW
R5811
100KOhm
R5852
100KOhm
R1.0-7
20150325
R1.1 follow VC & intel sequence
2014/12/26
remove VCCPRIM_PWRGD
25,30,87
3VA_DSW_PWRGD
83
1.05VSUS_PWRGD
D5804
BAT54AW
88
P_3VSUS_PWRGD
@ SL5808
0402
3VSUS_PWRGD
30
R5809
100KOhm
83
1.8VSUS_PWRGD
25,30
DPWROK_EC
D5803
BAT54AW
+3VSUS
R5805
100KOhm
D5802
3VSUS_PWRGD
88
VCCST_PWRGD
BAT54AW
+3VS
R5806
10KOhm
R5807
100KOhm
R5812
100KOhm
R1.0-7
20,25,30,88
PM_SUSB#
86
1.2V_PWRGD
D5801
BAT54AW
@ SL5801
0402
ALL_SYSTEM_PWRGD
C5804
100PF/50V
@
C5802
0.01UF/25V
UX303C1 0520
R5813
100KOhm
D5806
86
2.5V_PWRGD
BAT54AW
VCCST_PWRGD for PCH
+1.05V_VCCST
R5801
100KOhm
R5803
1KOhm
20150108
Checking
R5803 near CPU side
R1.0-2
D5805
BAT54CTB
@
VCCST_PWRGD_PCH
25
UM6K1N
Q5801B
UM6K1N
Q5801A
25,30,80
ALL_SYSTEM_PWRGD
@ SL5802
0402
C5801
0.1UF/6.3V
2.5V_PWRGD
EMI solution
@
C5803
0.1UF/6.3V
BOM
Project Name
X445FB
Rev
R1.0
Title : PRO_Protect
Size
B
Dept.: ASUSTeK COMPUTER INC.
Engineer: NB_EE
Date: Wednesday, July 17, 2019
Sheet 58 of 102

LED indicato
Charger LED



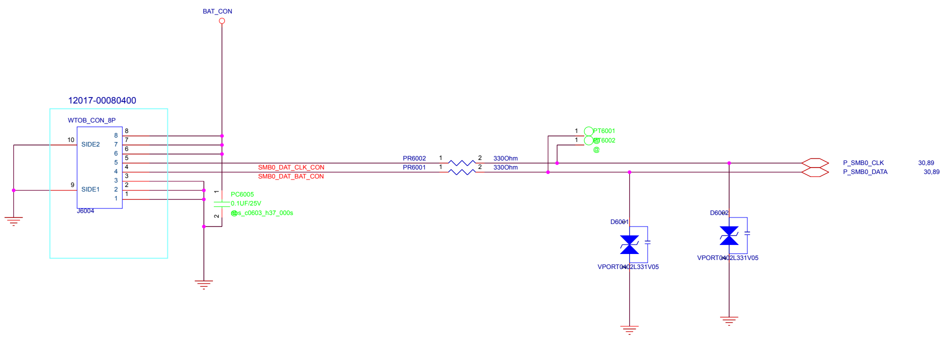


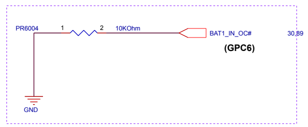
瓦數	Bead 數量
45W & 65W	BEAD * 3 09002-00130300
90W	BEAD * 4 09002-00130300
>90W	COHKE 09G02X102300



PLUG (mm)	ADP_W
4 Phi	33W ~ 65W
4.5 Phi	65W ~ 150W
6 Phi	90W ~ 280W

Battery Connector

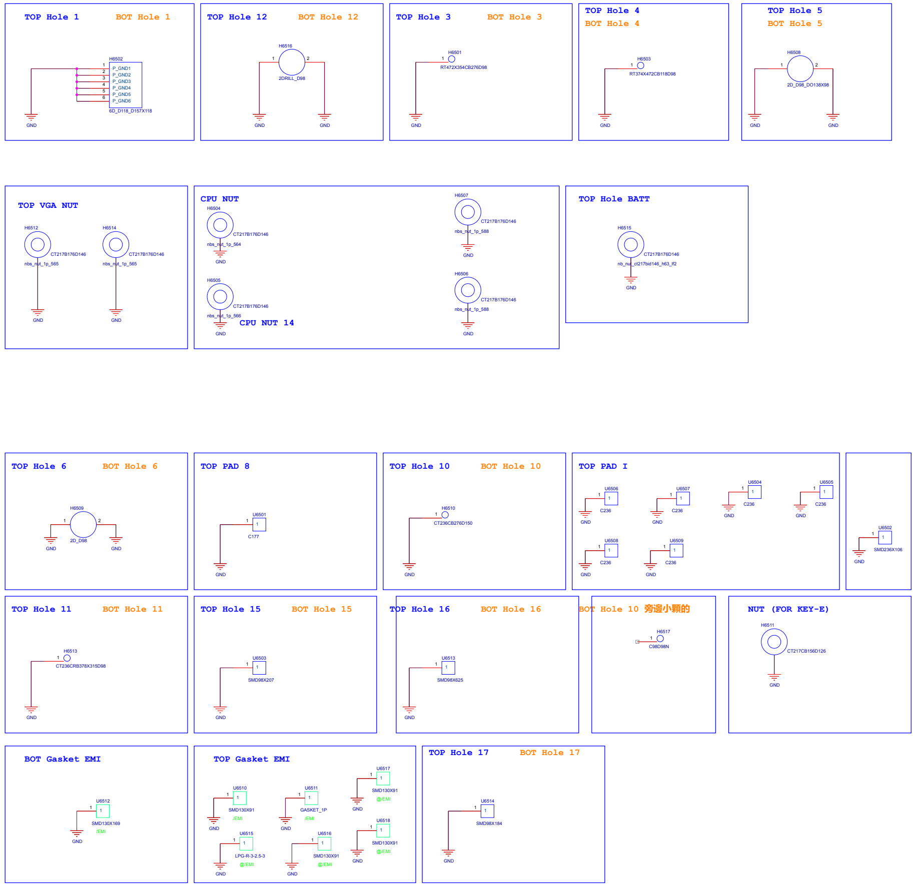


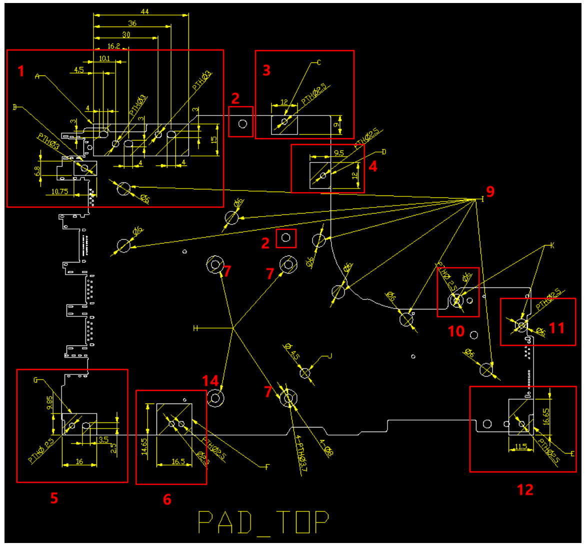


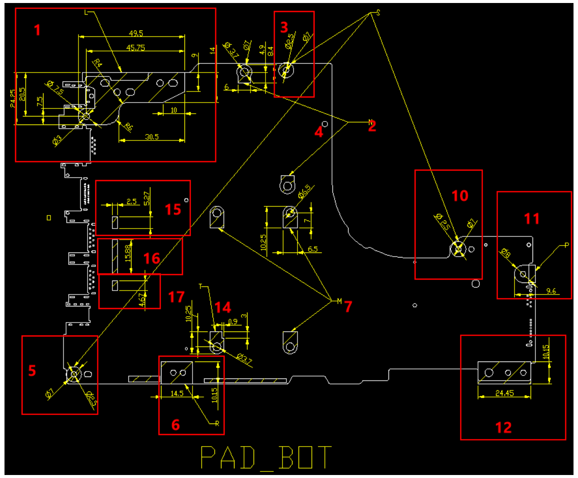
Close to EC & CHECK EC Page Yes or No Pu Down

<Variant Name>

Project Name: DESIGN_IP		Rev: R1.0
Title : DC & BAT Connector		
Size: Custom	Dept.: ASUS	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 60	of 102





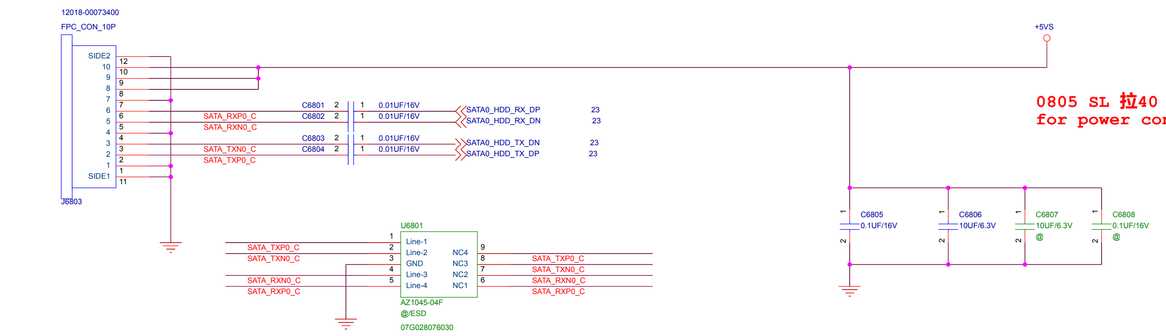


BOM

Project Name: X445FB		Rev: R1.0
Title : IO_SATA HDD & SPEAKER		
Size: E	Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE	
Date: Wednesday, July 17, 2019	Sheet 65 of 102	

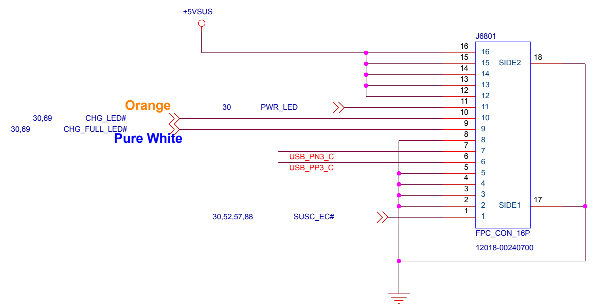
2018/07/03 modify connector same as X507UF (FFC Type)

2018/07/10 SL5101/SL5102



0805 SL 拉40 mil trace = 1A
for power consumption

Reserve for EMI
170426 Shaun
Change to 07G028076030 ESD
170427 Shaun
4-5 6-7 swape
170428 Shaun

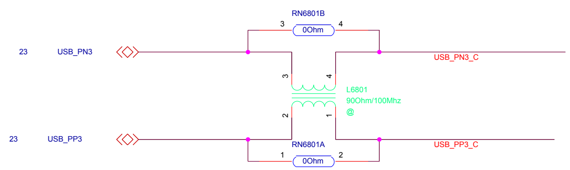


Orange

Pure White

s530 HDD FFC PIN DEFINE

FFC	PIN DEFINE	SATA CONN
	GND	P11
	GND	P10
1	5V	P9
2	5V	P8
3	5V	P7
	GND	P6
	GND	P5
	GND	P4
4	GND	S7
5	RXP(B+)	S6
6	RXN(B-)	S5
7	GND	S4
8	TXN(A-)	S3
9	TXP(A+)	S2
10	GND	S1



Gasket

20160713 EMI change U6901 U6902

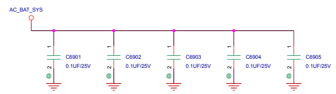
20170607 X540UV EMI GASKET

EMI CAP

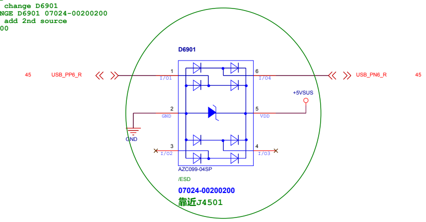
DDR4 CAPs

POWER CAPs

EMI AC_BAT_SYS CAP

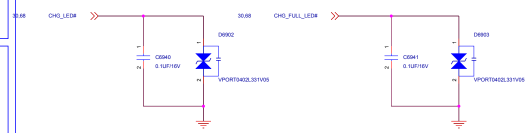


20160223 X541UV
CAMER for ESD
TOUCH for ESD
20160713 EMI change D6901
20170712 CHANGE D6901 07024-00200200
20170728 EDS add 2nd source
07024-00710000



LED CAPs

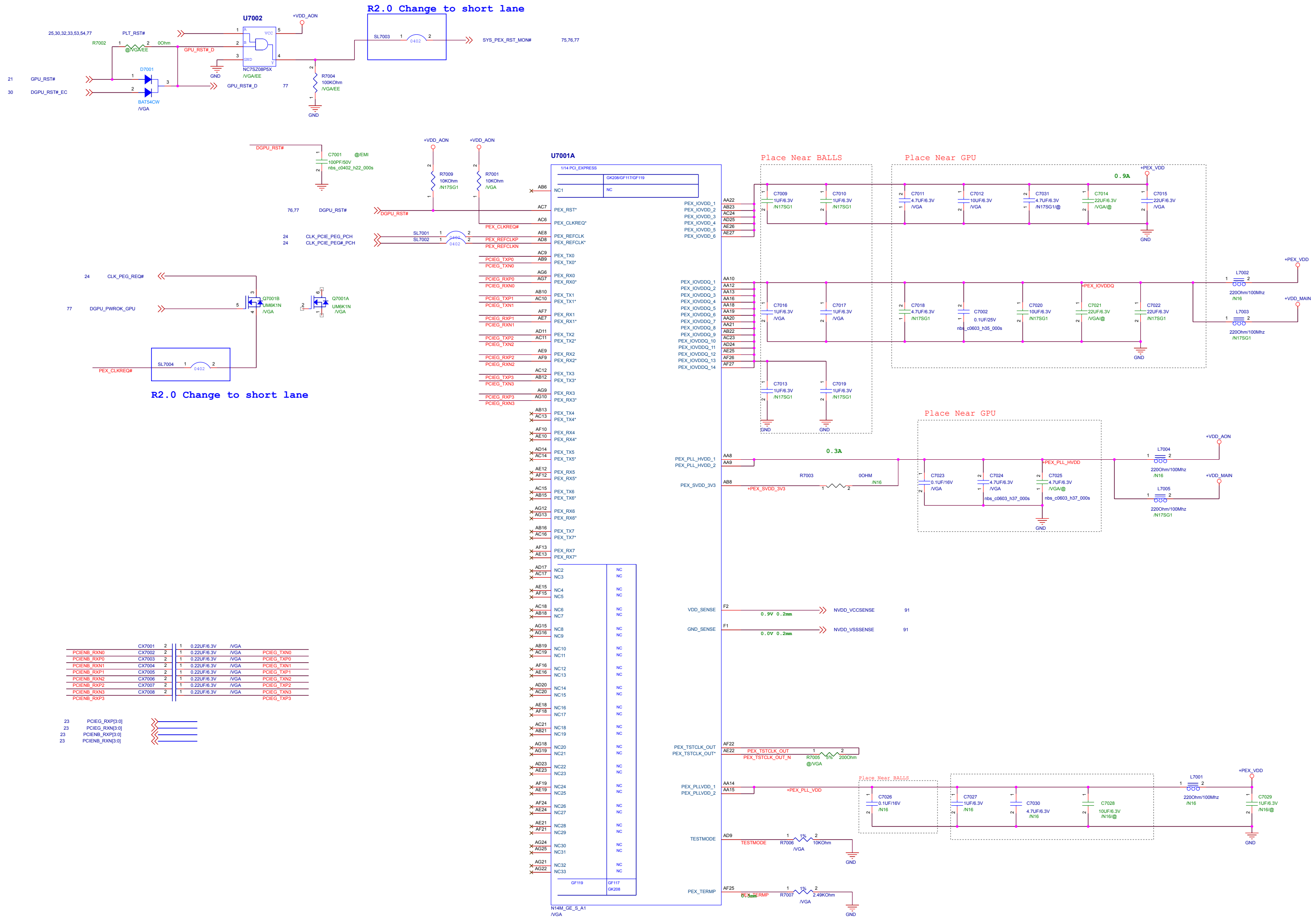
20170818 X540UV ESD 靠近LED5904



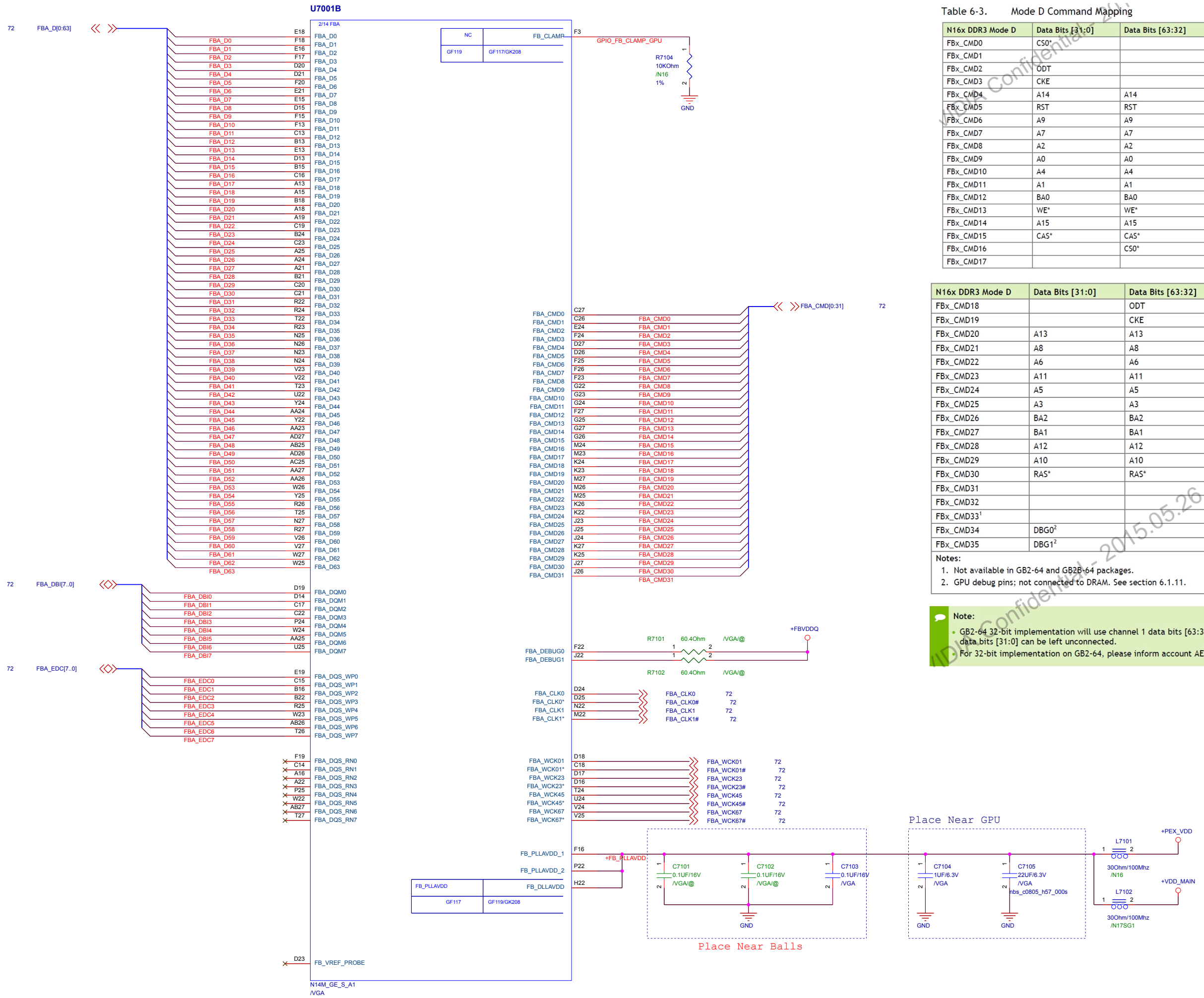
GUP CAPs

BOM

ASUS	Project Name X445FB	Rev R1.0
Title : EMI		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB_EE
Date: Wednesday, July 17, 2019	Sheet 69	of 102



R2.0 Change to short lane
U7002
NC7SZ08P5X
+VDD_AON
PLT_RST#
GPU_RST#
DGPU_RST#_EC
GPU_RST#_D
SYS_PEX_RST_MON#
R7004
100KOhm
D7001
BAT54CW
GND
U7001A
1/14 PCI_EXPRESS
DGPU_RST#
CLK_PCIE_PEG_PCH
CLK_PCIE_PEG#_PCH
CLK_PEG_REQ#
DGPU_PWROK_GPU
PEX_CLKREQ#
R2.0 Change to short lane
PEX_RST*
PEX_CLKREQ*
PEX_REFCLK
PEX_REFCLK*
Place Near BALLS
Place Near GPU
0.9A
+PEX_VDD
+VDD_MAIN
PEX_IOVDD_1
PEX_IOVDDQ_1
Place Near GPU
0.3A
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NVDD_VCCSENSE
NVDD_VSSSENSE
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*
PEX_PLLVDD_1
PEX_PLLVDD_2
TESTMODE
PEX_TERMP
N14M_GE_S_A1
/VGA
PCIEG_RXP[3:0]
PCIEG_RXN[3:0]
PCIENB_RXP[3:0]
PCIENB_RXN[3:0]



BOM Mount: 02004-00300400

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

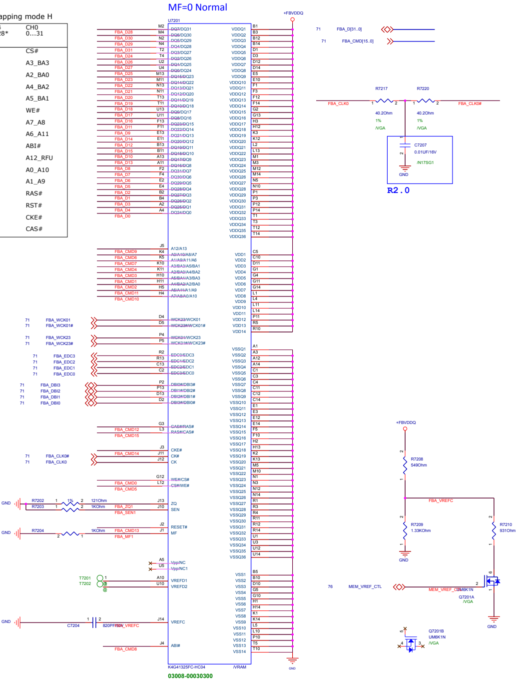
Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.

FBA Partition Memory (1 of 2)

CMD mapping mode H

GB2-64 GB4-128*	CH0 0...31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	ABI#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#

MF=0 Normal

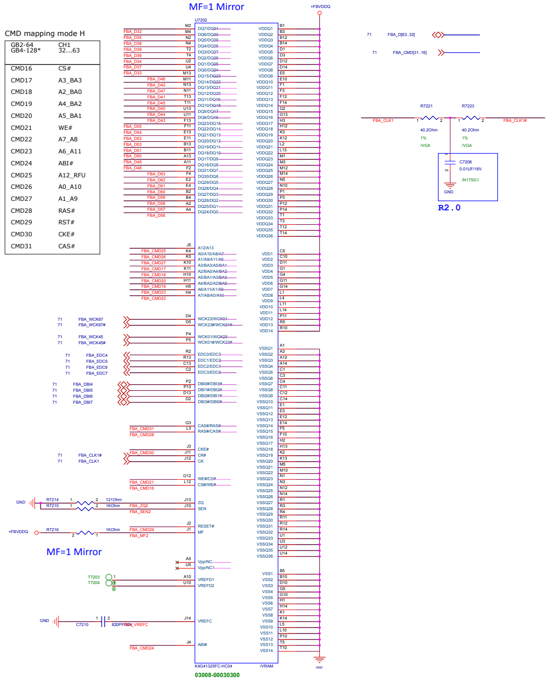


FBA Partition Memory (2 of 2)

CMD mapping mode H

GB2-64 GB4-128*	CH1 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	ABI#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

MF=1 Mirror



	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

USE GDDR5 VRAM 128Mb x 32 (512MB)

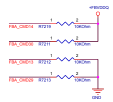
1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)

2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

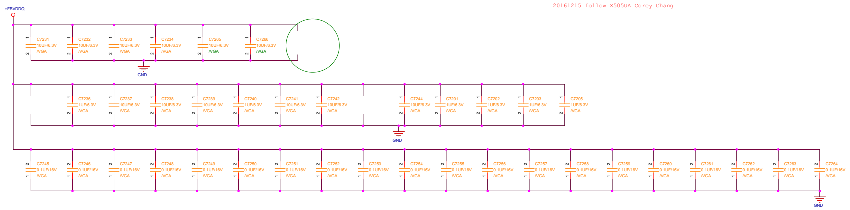
3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

GDD5 MODE SELECTION

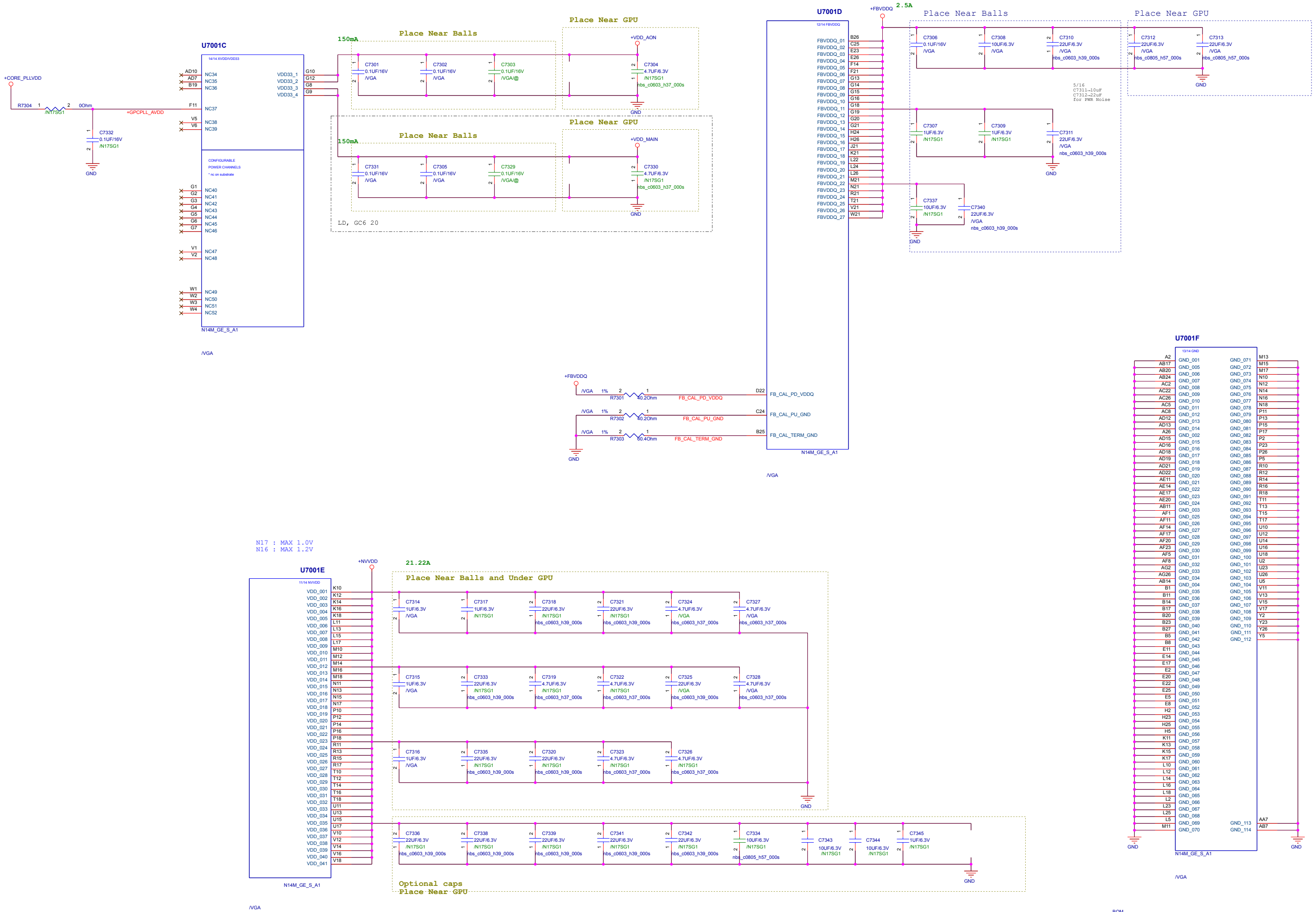
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ



20161215 follow X505UA Corey Chang



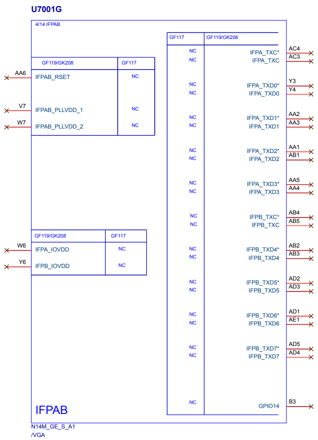
Project Name	X530FN	Rev R2.0
Title :	GPU_GDDR5A	
Size Custom	Dept.: ASUSTeK	Engineer: NB2_EE2
Date: Wednesday, July 17, 2019	Sheet 72 of 102	

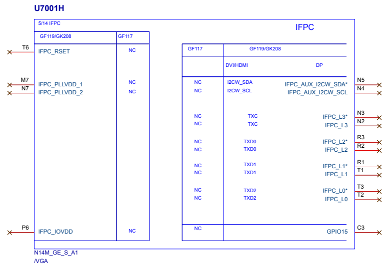


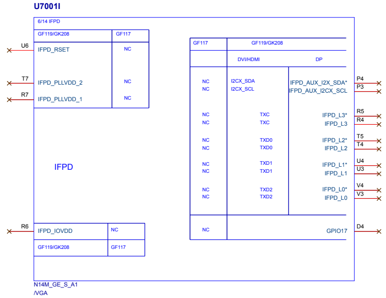
BOM

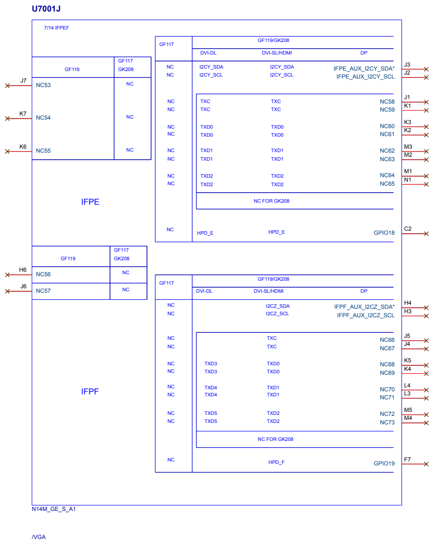
Project Name	X530FN	Rev R2.0
Title :	GPU_GDDR5B	
Size C	Dept.: ASUSTeK	Engineer: NB2_EE2
Date: Wednesday, July 17, 2019	Sheet 73	of 102

LVDS

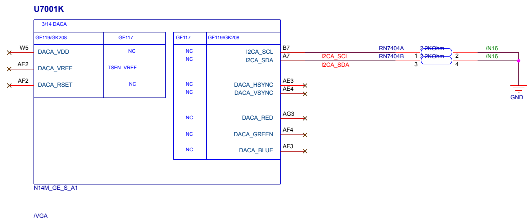

U7001G
4/14 IFPAB
IFPAB
N14M_GE_S_A1
/VGA


U7001H
5/14 IFPC
IFPC
N14M_GE_S_A1
/VGA


U7001I
6/14 IFPD
IFPD
N14M_GE_S_A1
/VGA


U7001J
7/14 IFPEF
IFPE
IFPF
N14M_GE_S_A1
/VGA

CRT


U7001K
3/14 DACA
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
GND
N14M_GE_S_A1
/VGA

VGA DEVICE = 0
PCIE CFG = 0
DEVID CFG = 0
SMB_ALT_ADDR = 0

DA-08329-001_v03_secured p.44
Table 11. N17/GB2C-64 Ternary Strapping

Strap Pin	N17S-G0,G2 GDDR5 MICRON(256*32) MT51J256M32HF-80:B 03008-00051600 (0x9)	N17S-G0,G2 GDDR5 HYNIX(256*32) H5GC8H24AJR-R2C 03008-00052000 (0xA)	N16V-GMR1, GDDR5 MICRON(256*32) MT51J256M32HF-70:B 03008-00051700 (0x8)	N16V-GMR1, GDDR5 HYNIX(256*32) H5GC8H24MJR-R0C 03008-00051100 (0x5)
STRAP0	L: R7504 = 100Kohm	H: R7530 = 100Kohm	R7501 = 49.9Kohm, R7504=>@	
STRAP1	L: R7505&R7502 = 100Kohm	L: R7505&R7502 = 100Kohm	Do not stuff	
STRAP2	H: R7506 = 100Kohm	H: R7506 = 100Kohm	Do not stuff	
STRAP3	L: R7510 = 100Kohm		Do not stuff	
STRAP4	L: R7511 = 100Kohm		Do not stuff	
STRAP5	L: R7512 = 100Kohm		Do not stuff	
ROM_SO	H: R7517 = 100Kohm		R7526 => 4.99K ohm, R7520=>@	R7526 => 4.99K ohm, R7520=>@
ROM_SI	H: R7516 = 100Kohm		R7516 = 4.99Kohm, R7519=>@	R7516 = @, R7519= 30.1K ohm
ROM_SCLK	M: R7513,R7518 = 100Kohm		R7521 =>4.99Kohm, R7518=>@	R7521 =>4.99Kohm, R7518=>@

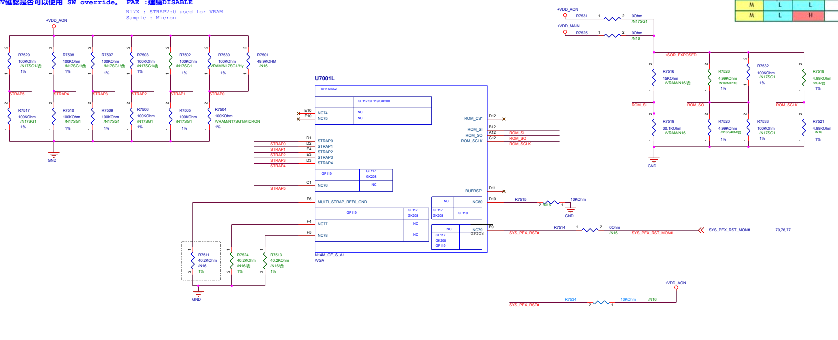
設定 ROM_SCLK,ROM_SI,ROM_SO PULL DOWN， 與NV確認是否可以使用 SW override。 FAE :建議DISABLE

N17X : STRAP2:0 used for VRAM
Sample : Micron

VG BOM 帶入主料時記得要加2nd Source

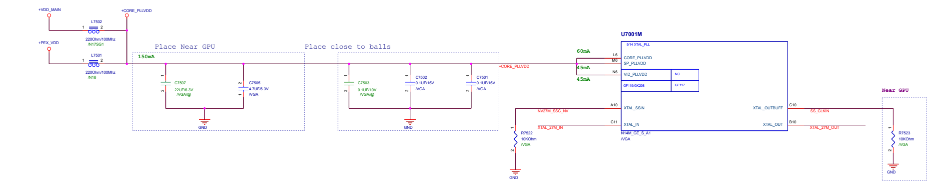
4.99K = 10G212499114010
10K = 10G212100214010
15K = 10G212150214030
20K = 10G212200214030
24.9K = 10G212249214010
30.1K = 10G212301214010
34.8K = 10G212348214010
45.3K = 10G212453214010
49.9K = 10G212499214010

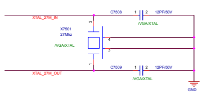
Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	N17/SAMSUNG
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	N17/HYNIX
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	



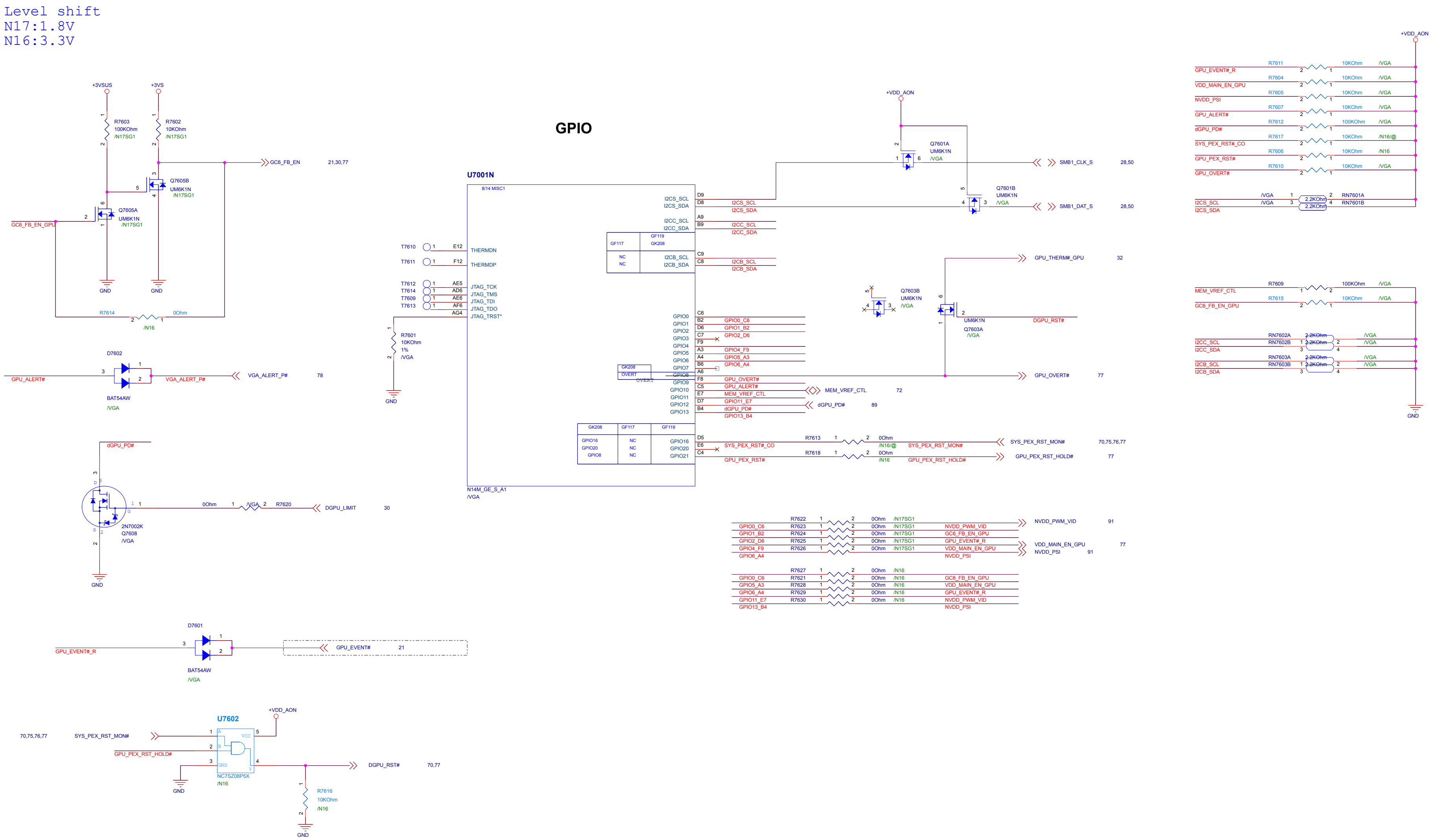
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND	
4.99 kΩ	1000	0000	N16/SAMSUNG
10.0 kΩ	1001	0001	N16/HYNIX
15.0 kΩ	1010	0010	
20.0 kΩ	1011	0011	
24.9 kΩ	1100	0100	
30.1 kΩ	1101	0101	
34.8 kΩ	1110	0110	
45.3 kΩ	1111	0111	

Xtal

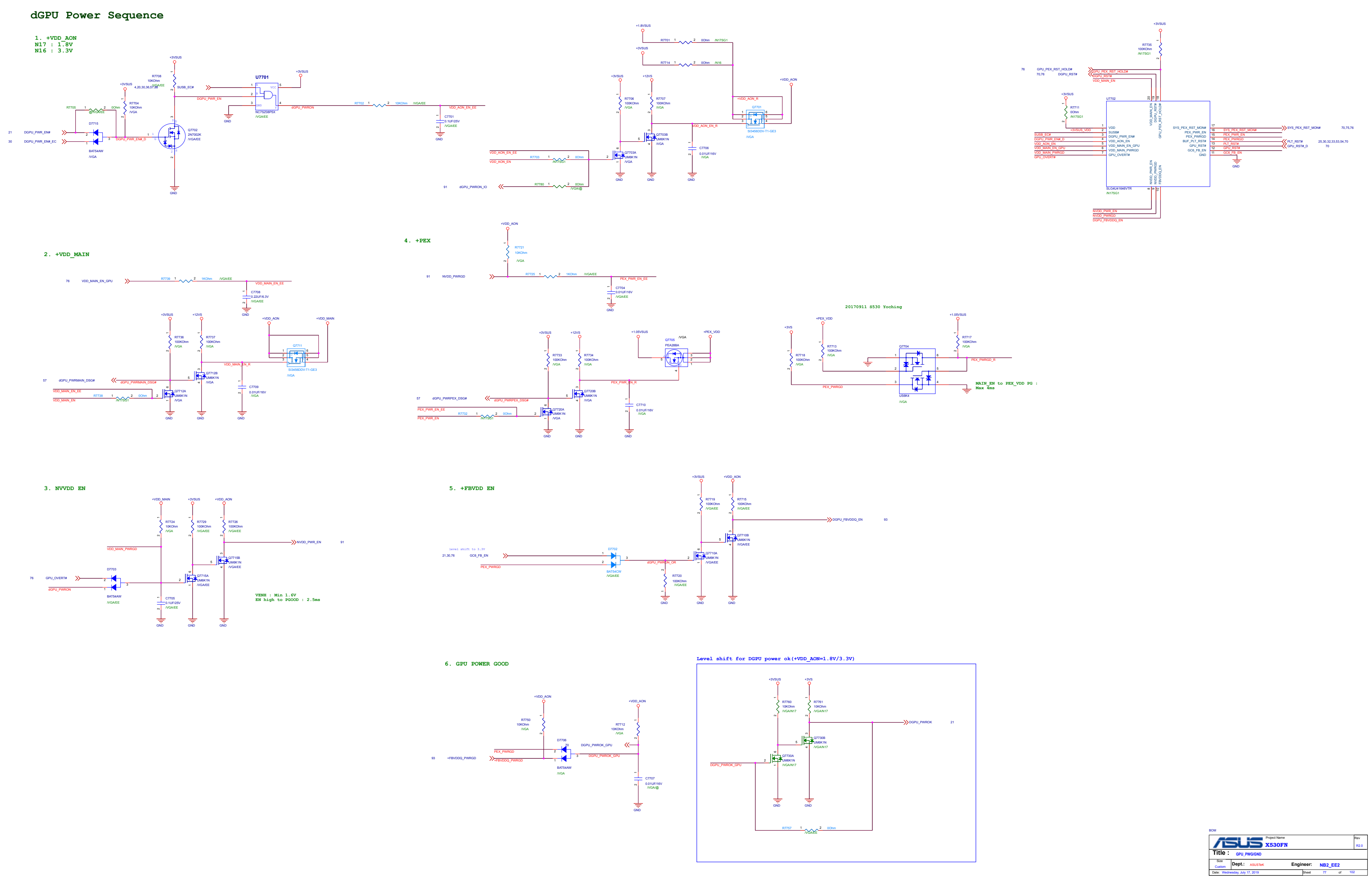




ASUS X530FN
Title : GPU_GPIO_THERMAL
Engineer: NB2_EE2



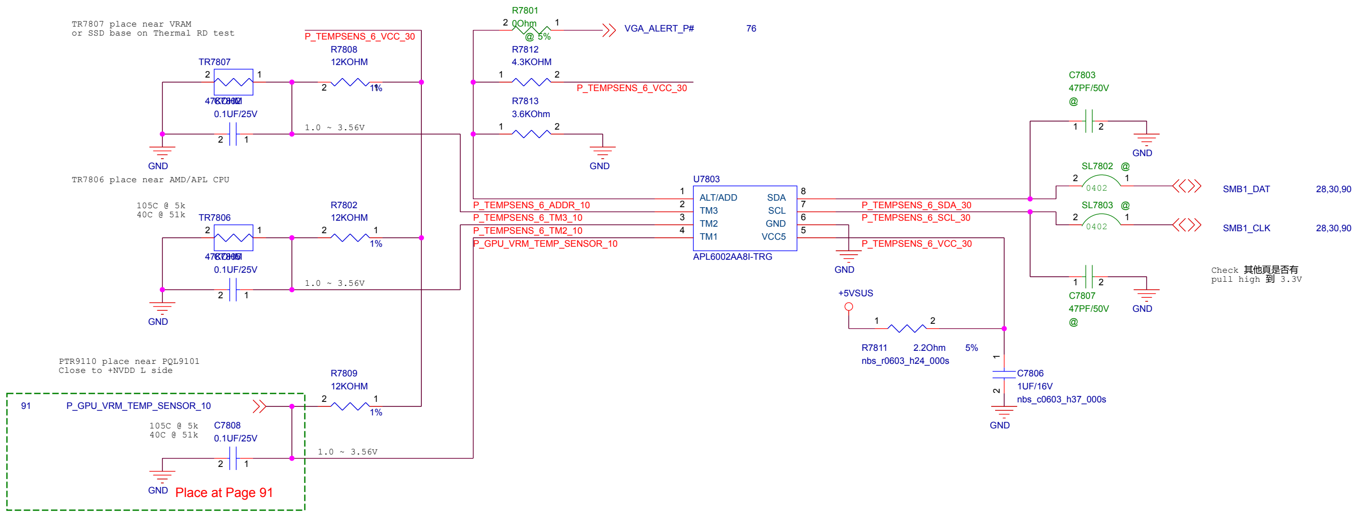
Level shift
N17:1.8V
N16:3.3V
GPIO
U7001N
8/14 MISC1
N14M_GE_S_A1
/VGA
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO16
GPIO20
GPIO21
+3VSUS
+3VS
+VDD_AON
R7603
100KOhm
/N17SG1
R7602
10KOhm
/N17SG1
Q7605B
UM6K1N
Q7605A
GC6_FB_EN
21,30,77
GC6_FB_EN_GPU
R7614
0Ohm
/N16
GND
D7602
BAT54AW
/VGA
GPU_ALERT#
VGA_ALERT_P#
VGA_ALERT_P#
78
dGPU_PD#
2N7002K
Q7608
R7620
0Ohm
DGPU_LIMIT
30
D7601
GPU_EVENT#_R
GPU_EVENT#
21
U7602
NC7SZ08P5X
/N16
SYS_PEX_RST_MON#
70,75,76,77
GPU_PEX_RST_HOLD#
DGPU_RST#
70,77
R7616
10KOhm
R7601
10KOhm
1%
Q7601A
UM6K1N
Q7601B
SMB1_CLK_S
28,50
SMB1_DAT_S
28,50
GPU_THERM#_GPU
32
Q7603B
Q7603A
DGPU_RST#
GPU_OVERT#
77
MEM_VREF_CTL
72
dGPU_PD#
89
R7613
R7618
SYS_PEX_RST#_CO
GPU_PEX_RST#
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
77
NVDD_PWM_VID
91
VDD_MAIN_EN_GPU
77
NVDD_PSI
91
R7622
R7623
R7624
R7625
R7626
R7627
R7621
R7628
R7629
R7630
GPIO0_C6
GPIO1_B2
GPIO2_D6
GPIO4_F9
GPIO5_A3
GPIO6_A4
GPIO11_E7
GPIO13_B4
GC6_FB_EN_GPU
GPU_EVENT#_R
R7611
R7604
R7605
R7607
R7612
R7617
R7606
R7610
VDD_MAIN_EN_GPU
NVDD_PSI
GPU_ALERT#
SYS_PEX_RST#_CO
GPU_PEX_RST#
GPU_OVERT#
RN7601A
RN7601B
2.2KOhm
R7609
R7615
MEM_VREF_CTL
RN7602A
RN7602B
RN7603A
RN7603B



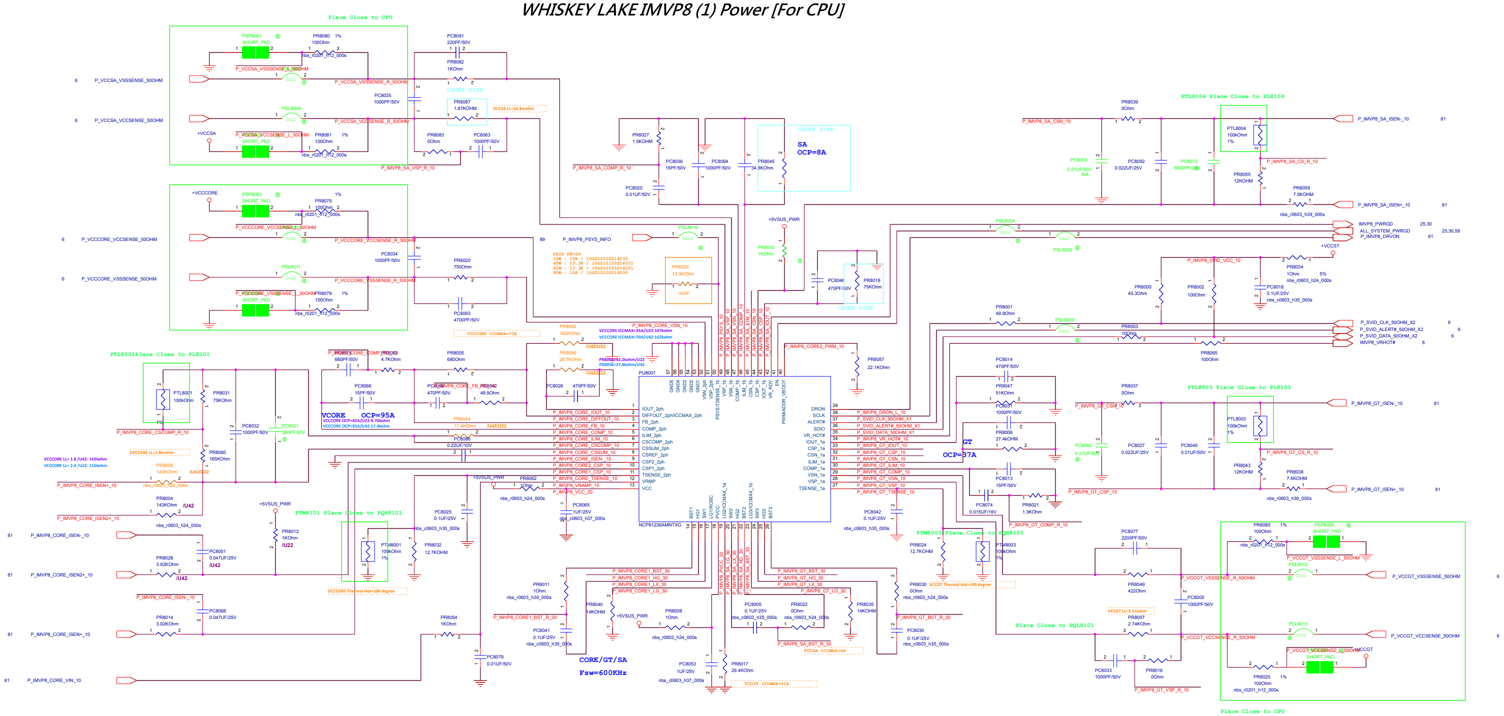
dGPU Power Sequence
1. +VDD_AON
N17 : 1.8V
N16 : 3.3V
2. +VDD_MAIN
3. NVVDD EN
4. +PEX
5. +FBVDD EN
6. GPU POWER GOOD
20170911 8530 Yoching
MAIN_EN to PEX_VDD PG : Max 4ms
VENB : Min 1.6V
EN high to PGOOD : 2.5ms
Level shift for DGPU power ok(+VDD_AON=1.8V/3.3V)
ASUS
X530FN
Title :
GPU_PWRGD

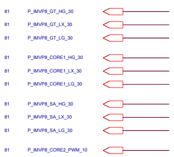
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7812	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7813	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



WHISKEY LAKE IMVP8 (1) Power [For CPU]





	PR8052	PR8056	PR8044	PR8009
/U42	162kohm	27.4kohm	17.4Kohm	143kohm
/U22	107kohm	42.2Kohm	9.76kohm	115kohm

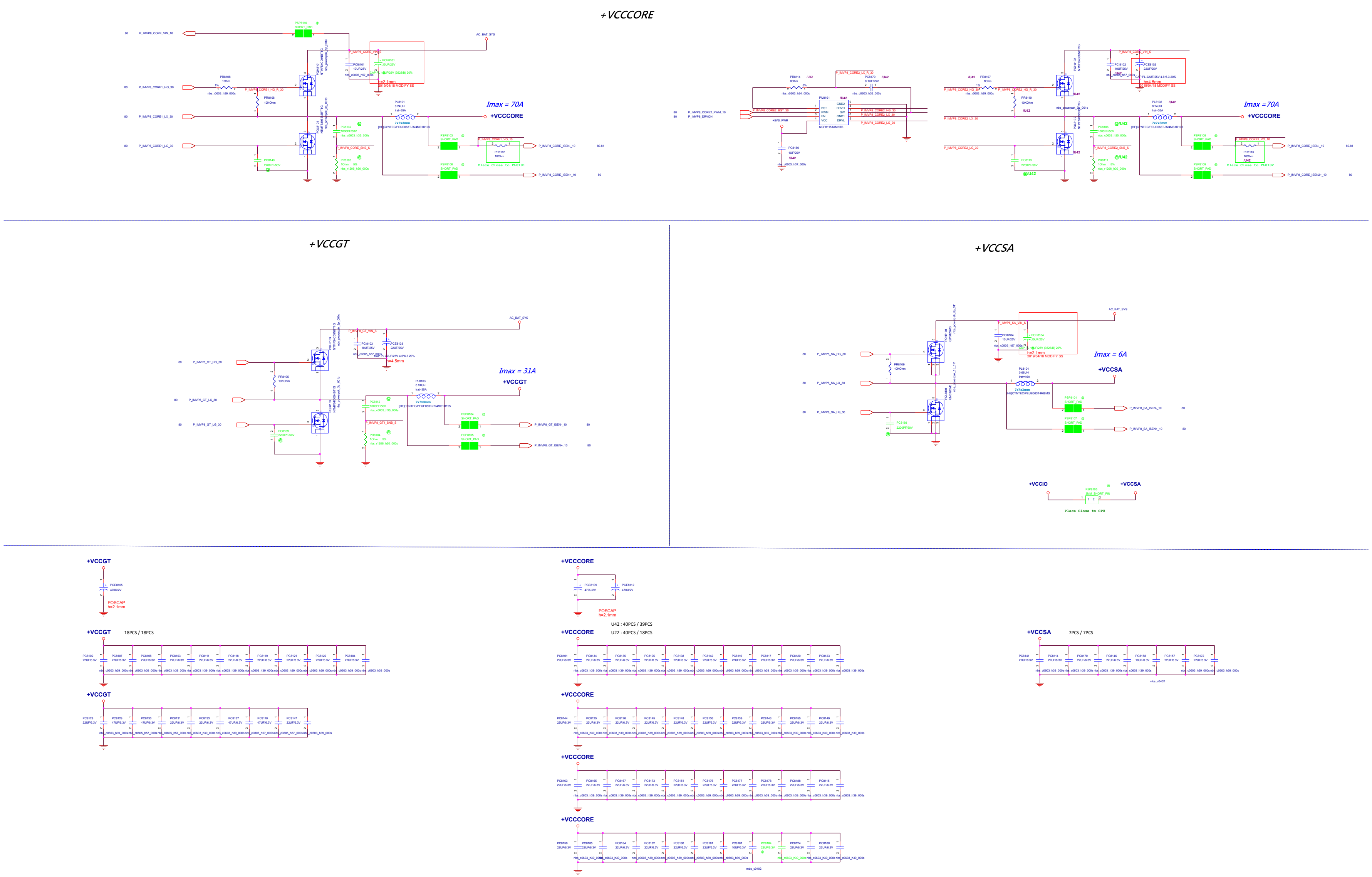
NCP81236A Rpsys Setting

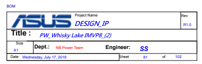
Adaptor	33W	45W	65W	90W
Psys_Pmax	100W	150W	150W	200W
CHG PMON Gain	2uA/W	1uA/W	1uA/W	1uA/W
Rpsys	10kohm	13.3kohm	13.3kohm	10kohm

BOM

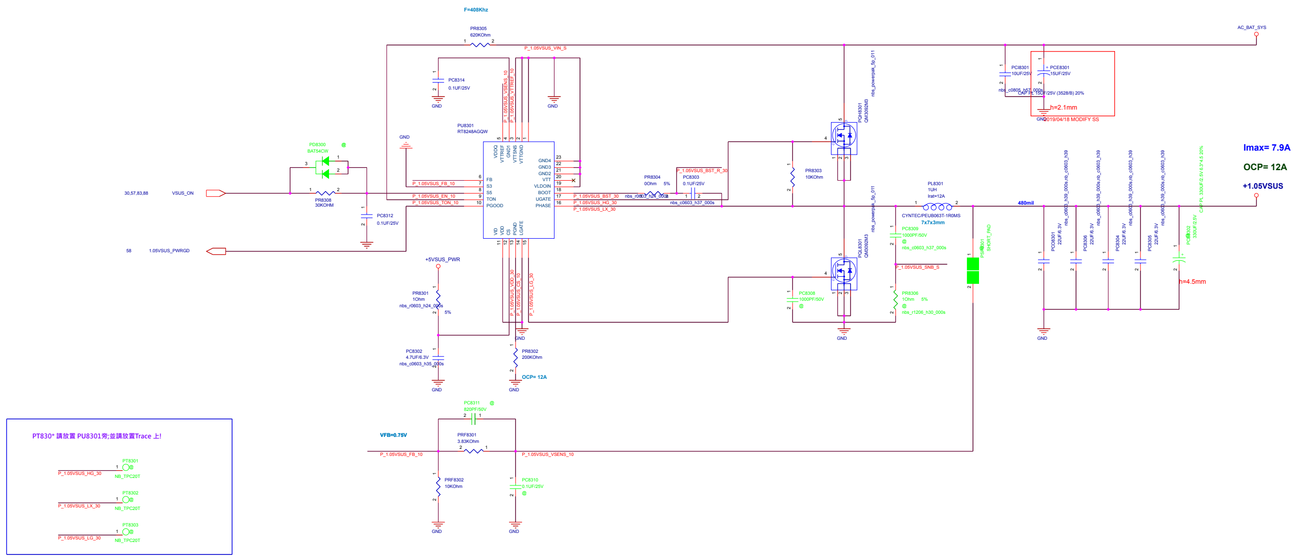
Project Name: DESIGN_IP		Rev: R1.0
Title : PW_Whisky Lake IMVP8_(1)		
Size: A2	Dept.: NB Power Team	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 80 of 102	

Wishky LAKE IMVP8 Power (2)[For CPU]

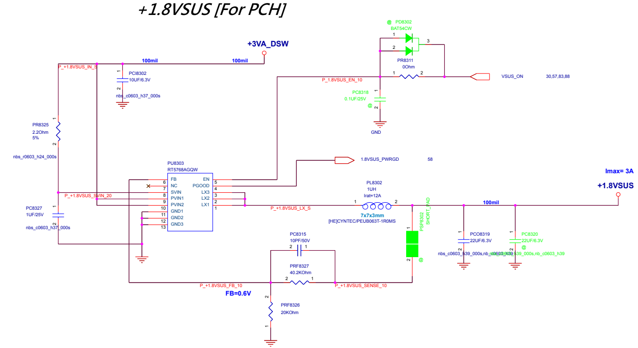




+1.05VSUS [For PCH]



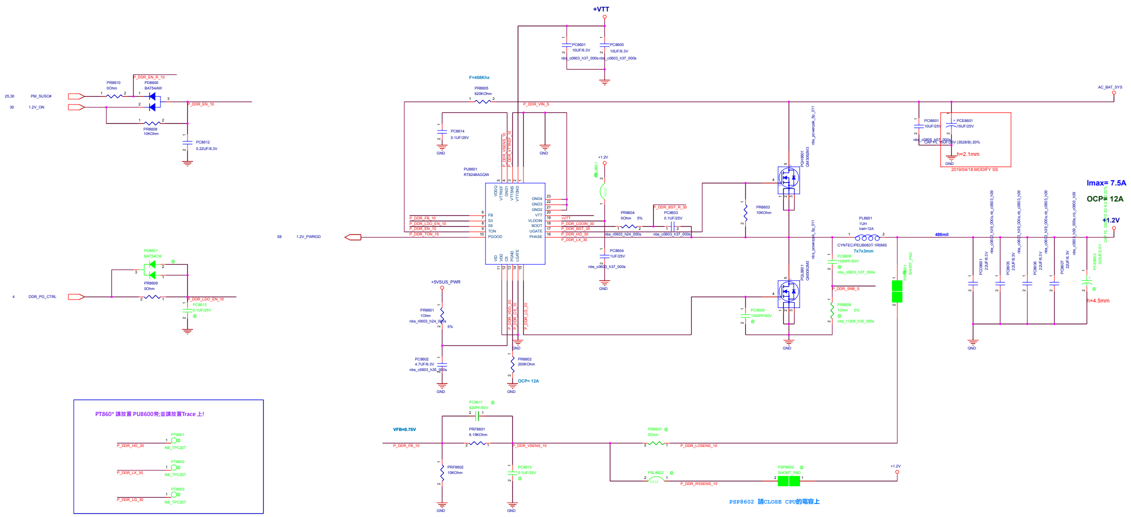
+1.8VSUS [For PCH]



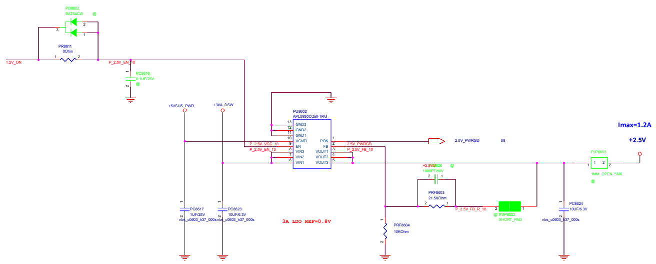
<Core Design>

Project Name: DESIGN_IP		Rev: R1.0
Title : PW_+1.05VSUS/+1.8VSUS		
Size: A2	Dept.: NB Power team	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 83	of 102

+1.2V / +VTT [For Memory]



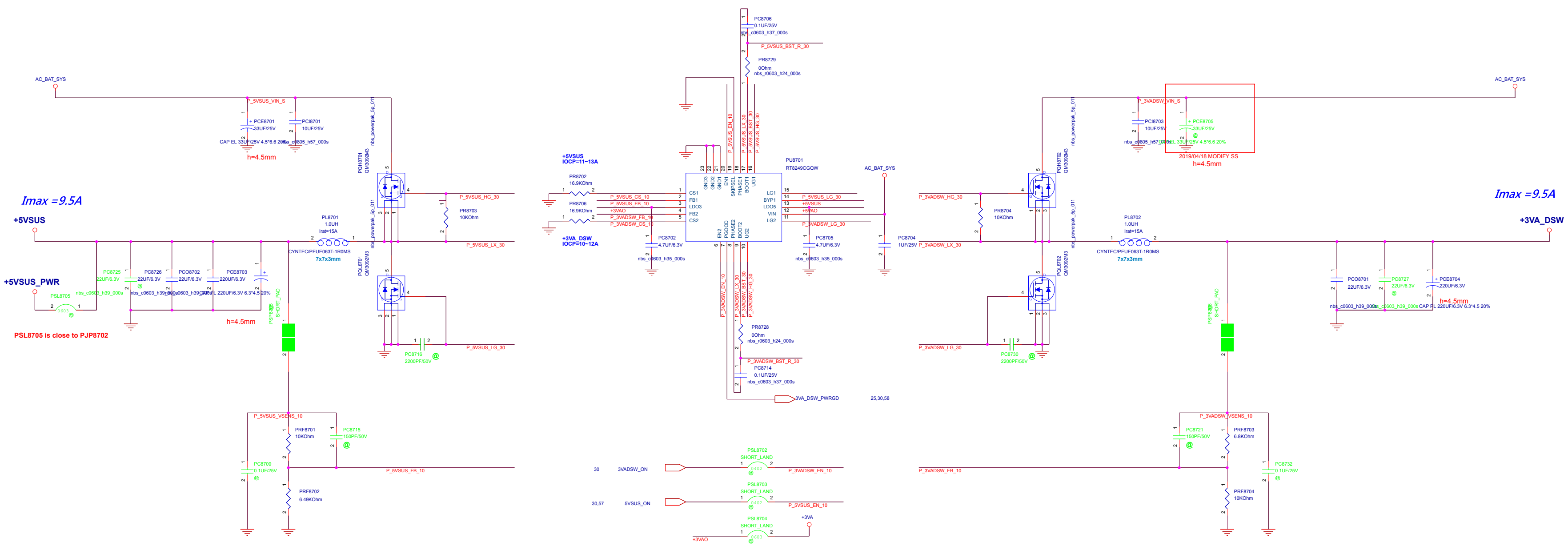
+2.5V



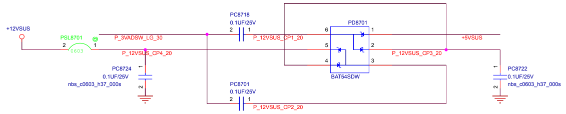
<Core Design>

ASUS Project Name DESIGN_IP		Rev R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size A1	Dept.: NB Power team	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 86 of 103	

+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



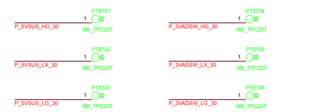
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8701旁;並請放置Trace 上!

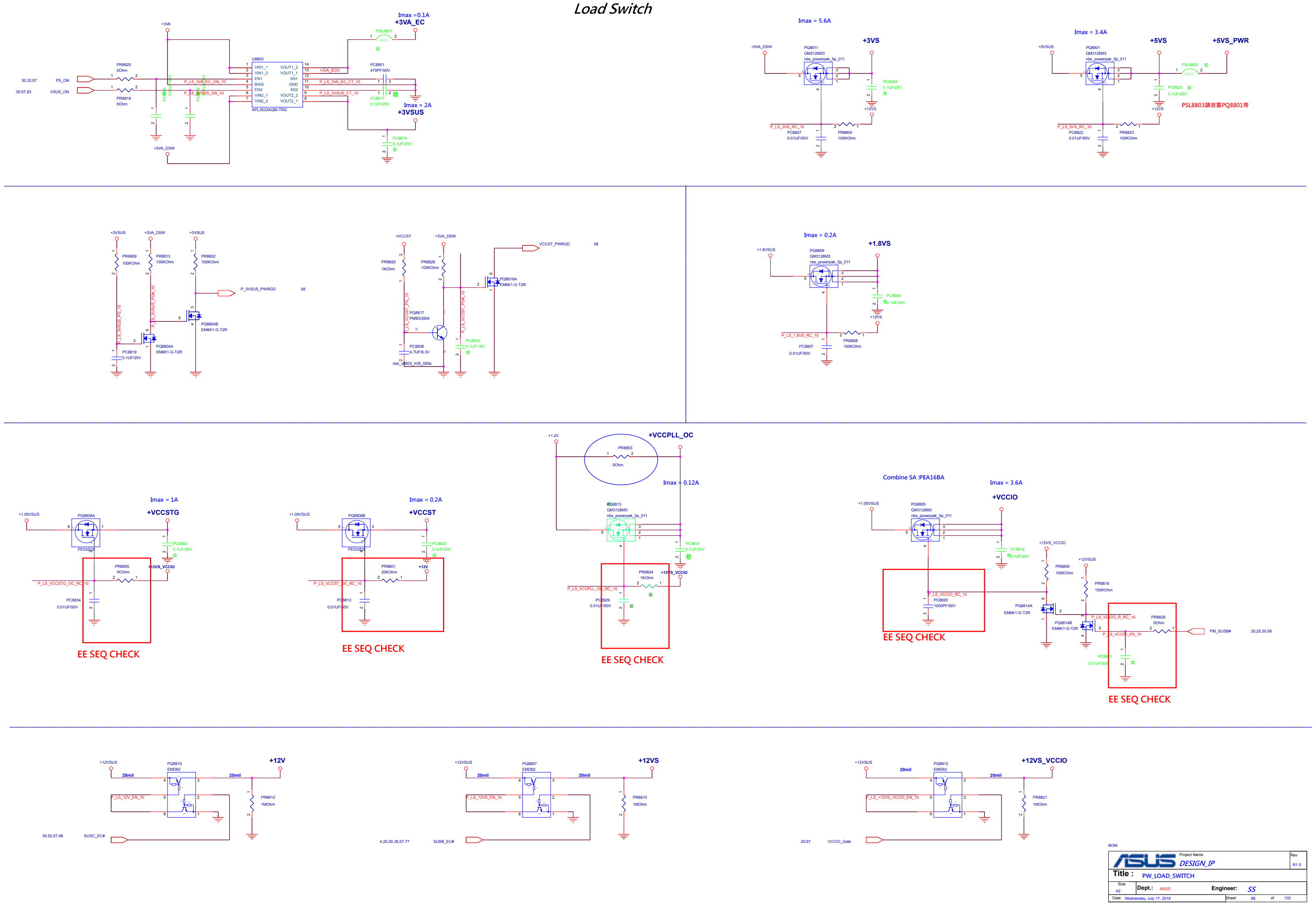


MOSFET	Power SPEC(peak)	OCP	R(PR8302)
QM3126M3	<6A	7.5A~10A	22K (10G212220214030)
PEA28BA	<6A	7.5A~10A	27K (10G212270214030)
PEA16BA	6~10A	12A~15A	15K (10G212150214030)
5 * 6 (1+1)	>10A	17A~20A	自行調整

BOM

ASUS	Project Name DESIGN_IP	Rev R1.0
Title : PW_+3VA_DSW/+5VSUS		
Size A2	Dept.: ASUS	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 87 of 102	

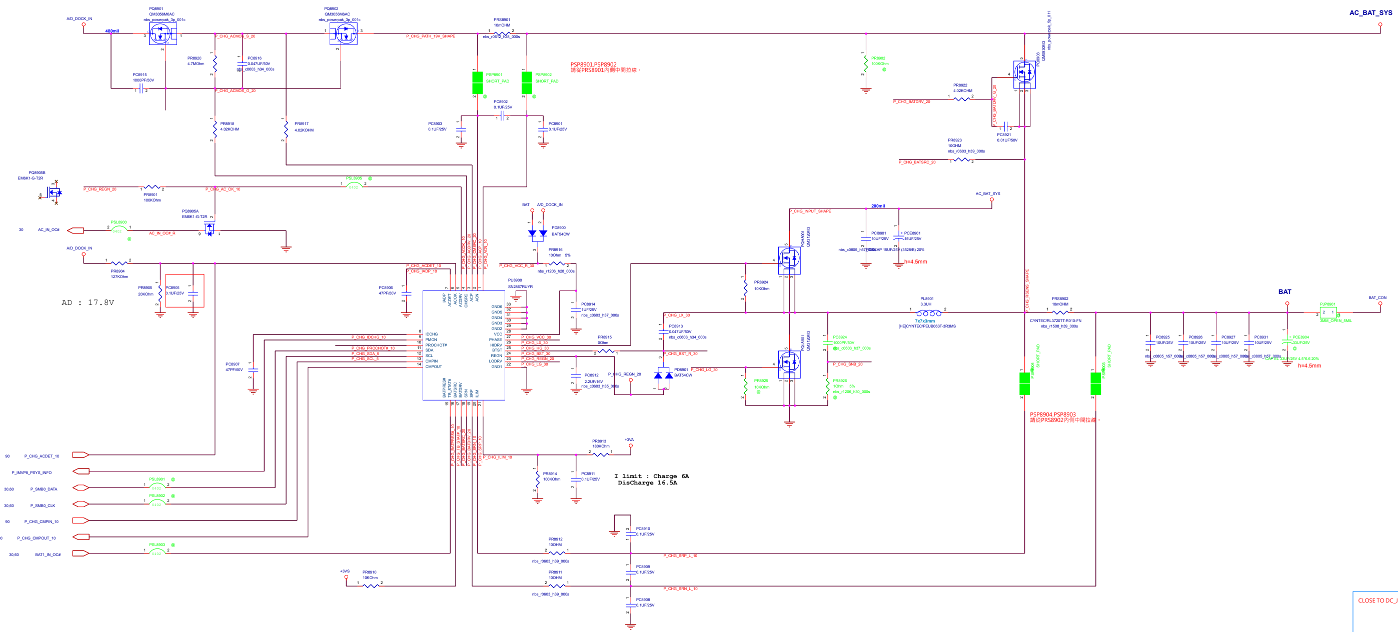
Load Switch

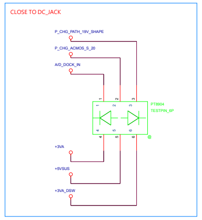


Imax =0.1A
+3VA_EC
Imax = 2A
+3VSUS
Imax = 5.6A
+3VS
Imax = 3.4A
+5VS
+5VS_PWR
Imax = 0.2A
+1.8VS
+VCCPLL_OC
Imax = 0.12A
Imax = 1A
+VCCSTG
Imax = 0.2A
+VCCST
Combine SA :PEA16BA
Imax = 3.6A
+VCCIO
EE SEQ CHECK
EE SEQ CHECK
EE SEQ CHECK
EE SEQ CHECK
EE SEQ CHECK
+12V
+12VS
+12VS_VCCIO
Title :
PW_LOAD_SWITCH
Dept.:
Engineer:

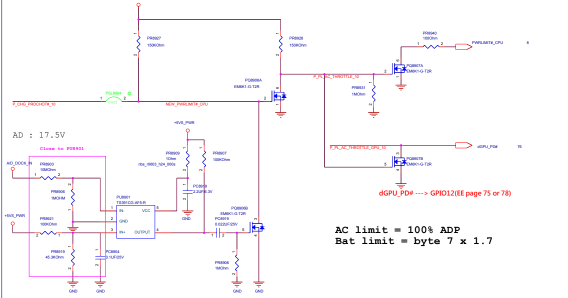
	PQ8901 & PQ8902
<65W ACFET	QM3056M6AC 07005-A0480100
>90W ACFET	QM3058M6AC 07005-A0790000

PRS8901	<=40W	<=120W	>=120W
	20m	10m	5m
	10125-0004B000	10125-0001B100	10G21DR00515111

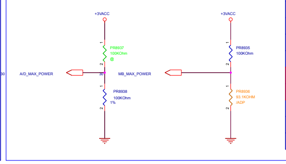




HW_Throttle

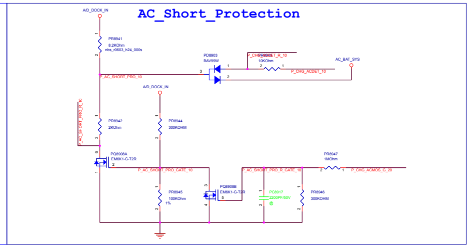


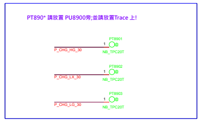
Adaptor select
total power = 90% ADP



Adaptor select			
		X/UX Series	G Series
PRS8901		10m	5m
PR8936			
14K 10G212140214030	0.4V	30W	120W
31.6K 10G212316214030	0.8V	40W	150W
56K 10G212560214030	1.2V	45W	180W
93.1K 10G212931214031	1.6V	65W	230W
150K 10G212150314031	2.0V	75W	300W
270K 10G212270314030	2.4V	90W	330W
560K 10G212560314030	2.8V	120W	400W

AC_Short_Protection





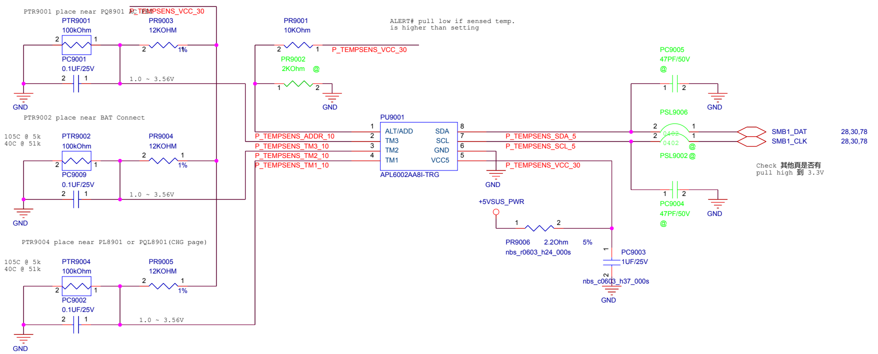
Title : PW_CHARGER
DESIGN_IP
Engineer: SS

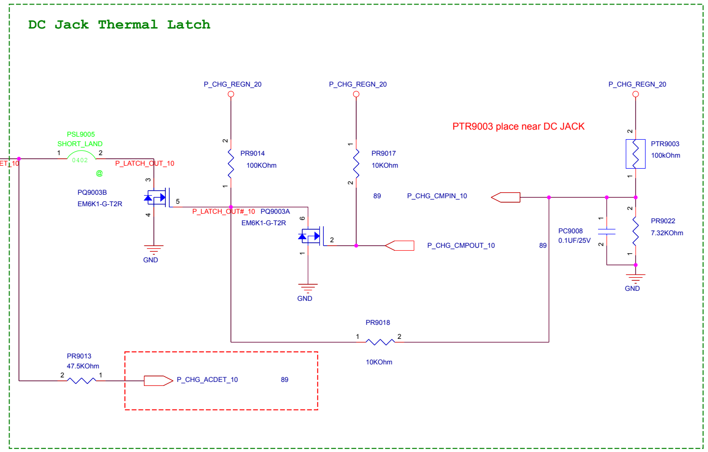
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert





<Variant Name>

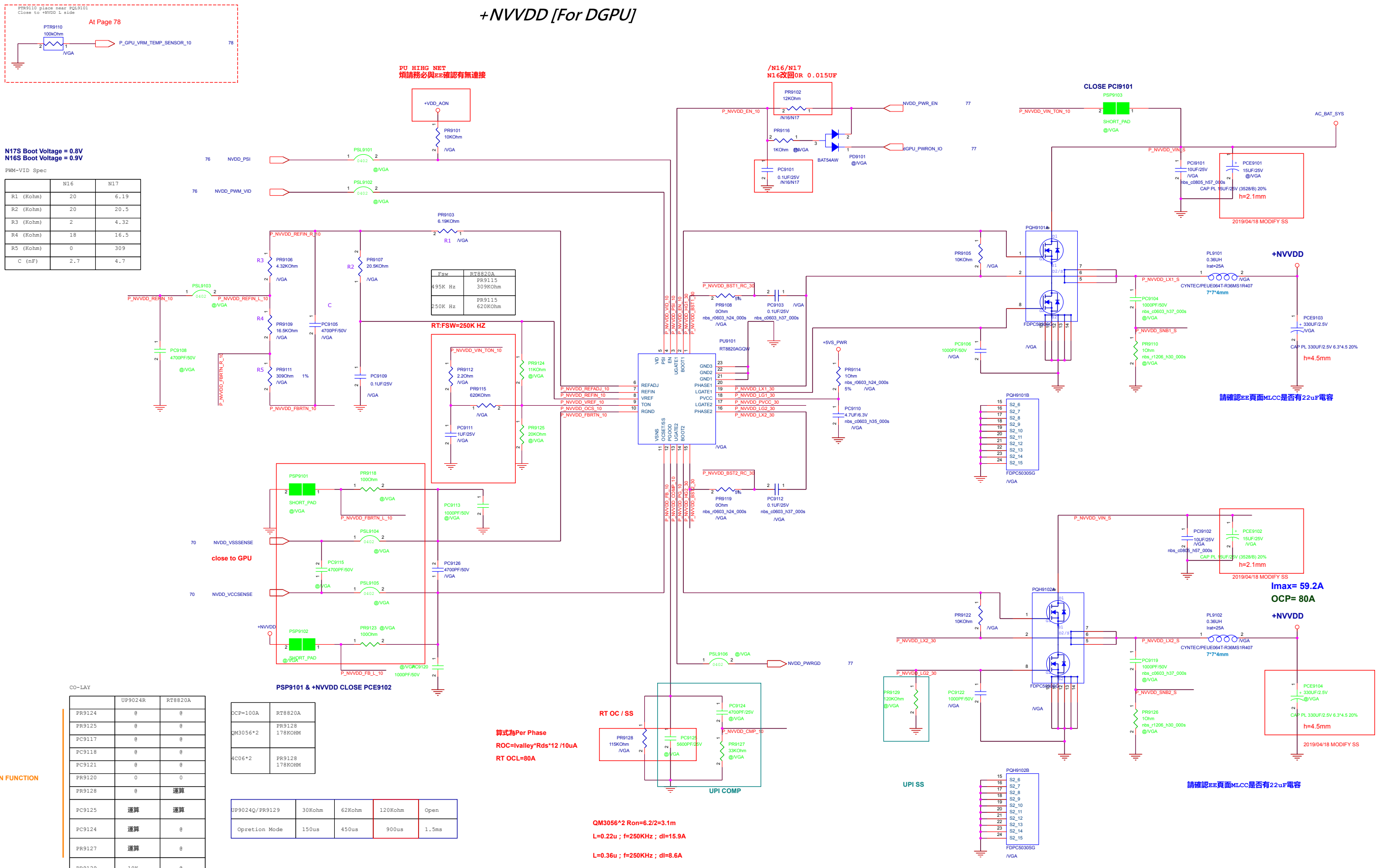
ASUS	Project Name: DESIGN_IP	Rev: R1.0
Title : PW_PROTECTION		
Size: A3	Dept.: ASUS	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 90	of 102

+NVVDD [For DGPU]

N17S Boot Voltage = 0.8V
N16S Boot Voltage = 0.9V

PWM-VID Spec

	N16	N17
R1 (Kohm)	20	6.19
R2 (Kohm)	20	20.5
R3 (Kohm)	2	4.32
R4 (Kohm)	18	16.5
R5 (Kohm)	0	309
C (nF)	2.7	4.7



Fsw	RT8820A
495K Hz	PR9115 309KOhm
250K Hz	PR9115 620KOhm

RT:FSW=250K HZ

算式為Per Phase
ROC=Ivalley*Rds*12 /10uA
RT OCL=80A

QM3056^2 Ron=6.2/2=3.1m
L=0.22u ; f=250KHz ; dI=15.9A

L=0.36u ; f=250KHz ; dI=8.6A

CO-LAY

12PIN FUNCTION

9PIN FUNCTION

	UP9024R	RT8820A
PR9124	@	@
PR9125	@	@
PC9117	@	@
PC9118	@	@
PC9121	@	@
PR9120	0	0
PR9128	@	運算
PC9125	運算	運算
PC9124	運算	@
PR9127	運算	@
PR9129	10K	@
PR9115	@	620K
PR9130	10K	@
PR9113	620KOhm	@
PC9116	改電阻對地	@
PC9111	@	1UF
PR9112	@	2.2Ohm

OCP=100A	RT8820A
QM3056*2	PR9128 178KOHM
4C06*2	PR9128 178KOHM

UP9024Q/PR9129	30Kohm	62Kohm	120Kohm	Open
Opretion Mode	150us	450us	900us	1.5ms

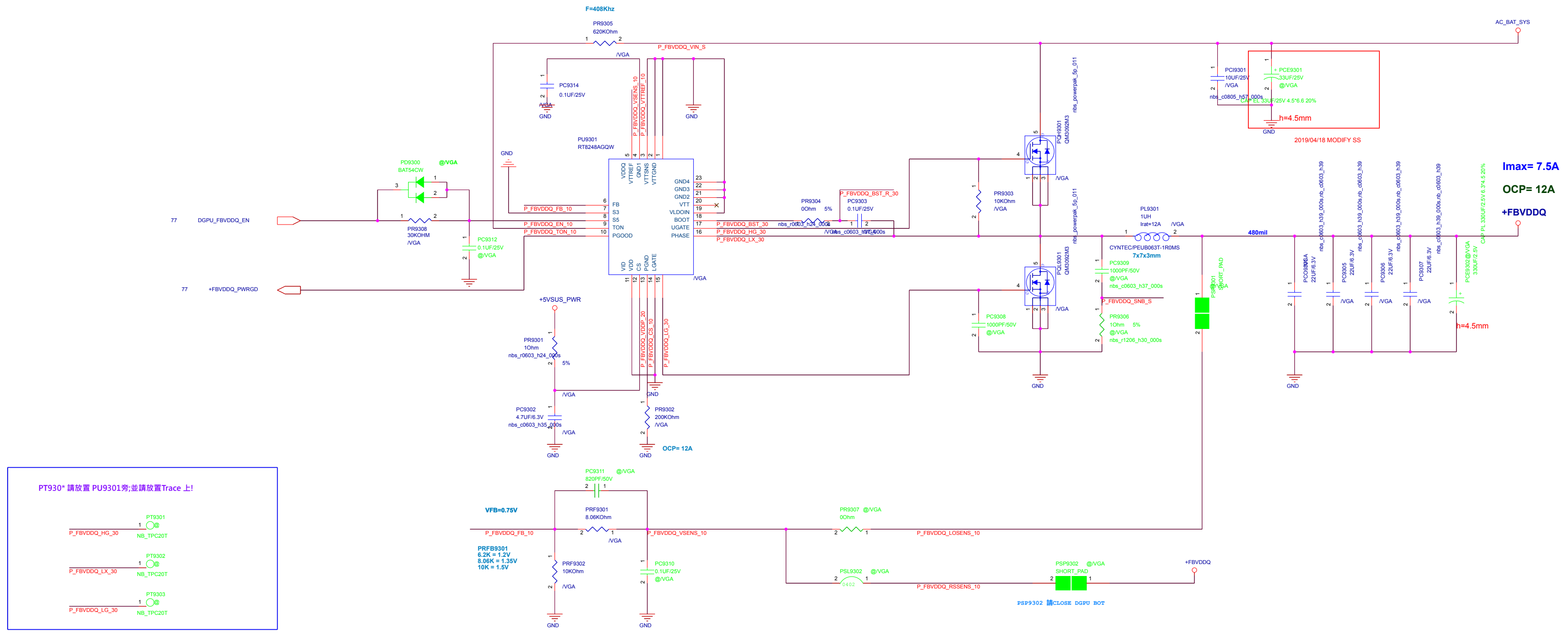
PT910* 請放置 PU9101旁;並請放置Trace 上!

P_NVVDD_HG1_30 PT9101 @/VGA NB_TPC20T
P_NVVDD_HG2_30 PT9102 @/VGA NB_TPC20T
P_NVVDD_LX1_30 PT9103 @/VGA NB_TPC20T
P_NVVDD_LX2_30 PT9104 @/VGA NB_TPC20T
P_NVVDD_LG1_30 PT9105 @/VGA NB_TPC20T
P_NVVDD_LG2_30 PT9106 @/VGA NB_TPC20T

<Variant Name>

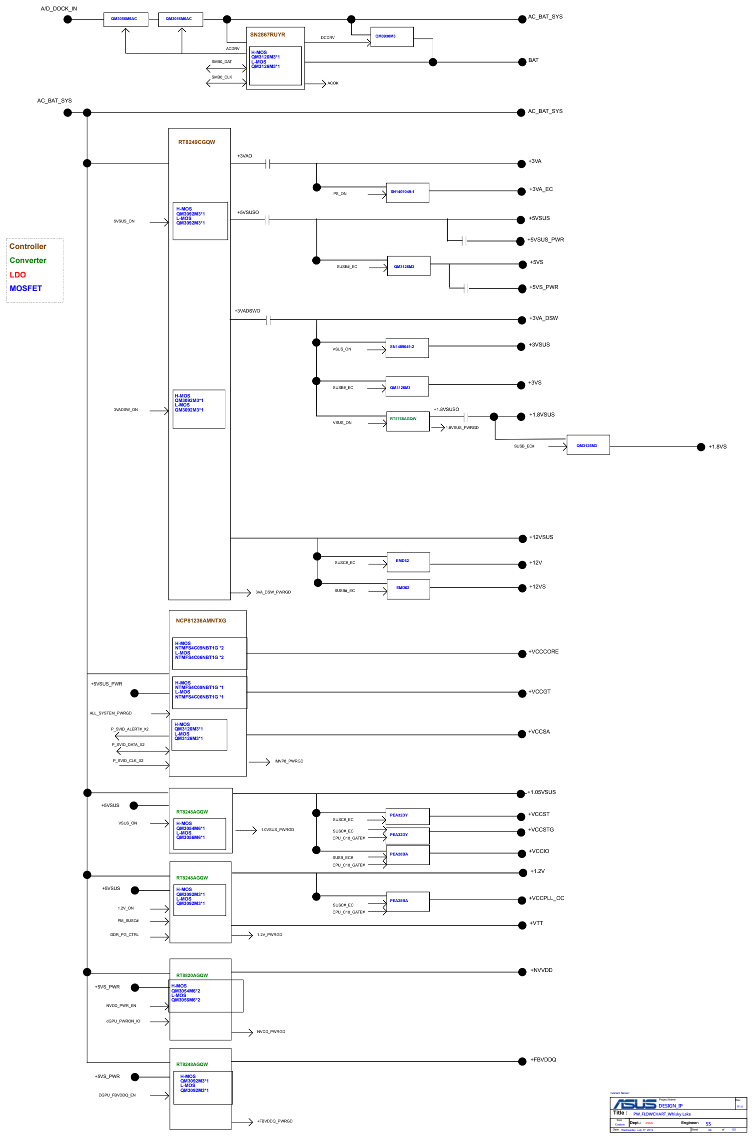
Project Name: DESIGN_IP		Rev: R1.0
Title : PW_+NVVDD		
Size: A2	Dept.: NB Power Team	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 91 of 102	

+FBVDDQ [For VRAM]



<Core Design>

ASUS	Project Name: DESIGN_IP	Rev: R1.0
Title : PW_+FBVDDQ		
Size: A2	Dept.: NB Power team	Engineer: SS

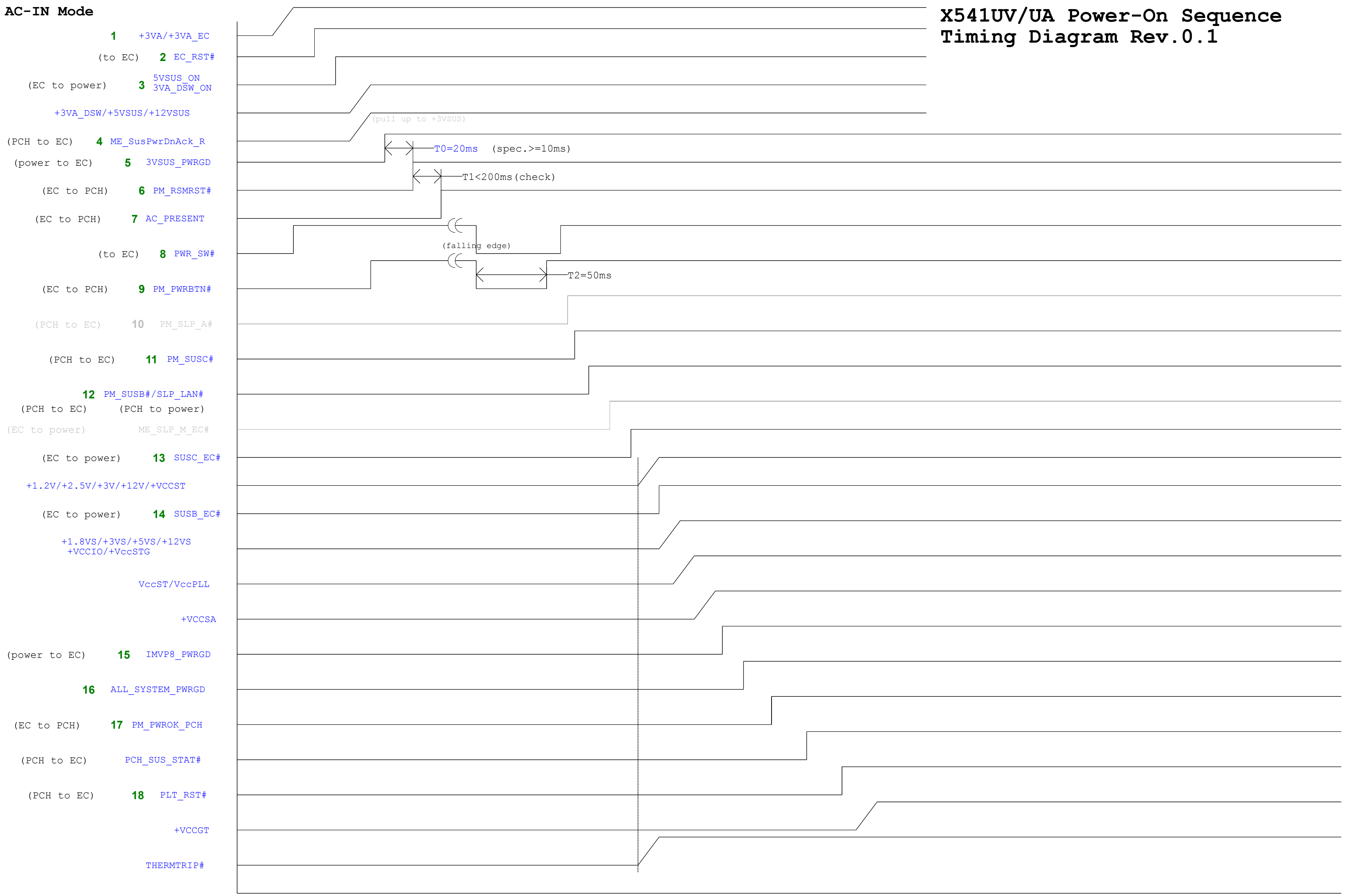


<Variant Name>

ASUS	Project Name DESIGN_IP	Rev R1.0
Title :	PW_FLOWCHART_Whisky Lake	
Size Custom	Dept.: ASUS	Engineer: SS
Date: Wednesday, July 17, 2019	Sheet 99 of 102	

X541UV/UA Power-On Sequence Timing Diagram Rev.0.1

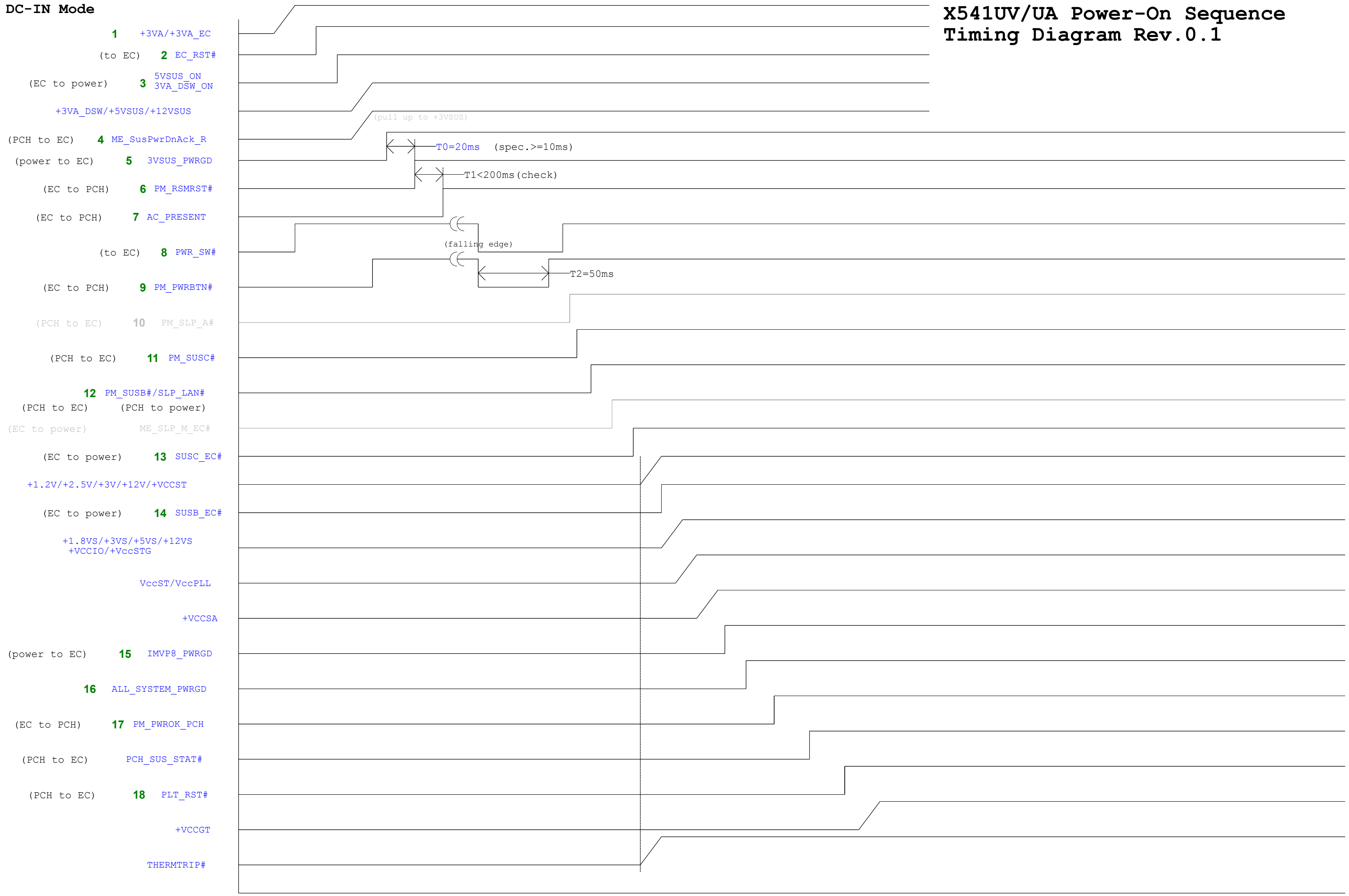
AC-IN Mode



BOM

Project Name X445FB		Rev R1.0
Title : Power On Timing		
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE	

X541UV/UA Power-On Sequence Timing Diagram Rev.0.1



BOM
Project Name: X445FB
Rev: R1.0
Title : Power On Timing
Size: C
Dept.: ASUSTeK COMPUTER INC. Engineer: NB_EE
Date: Wednesday, July 17, 2019 Sheet 101 of 102