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03	Change List	1A	
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05	HSW MCP(MEMORY/GND)	1A	
06	HSW MCP(CFG/PwrMGT)	1A	
07	HSW MCP(POWER)	1A	
08	HSW PCH(RTC/HDA/SATA)	1A	
09	HSW PCH(PCIE/USB)	1A	
10	HSW PCH(CLK/LPC/SPI/SMB)	1A	
11	HSW PCH(GPIO/LPIO/MISC)	1A	
12	HSW PCH(POWER)	1A	
13	DDR3L DIMM0-STD 4H(CH-A)	1A	
14	DDR3L DIMM1-RVS 4H(CH-B)	1A	
15	HOLE/EMI/KB	1A	
16	WPCE985L & FLASH	1A	
17	EDP/TS/CAMERA/NFC	1A	
18	HDD/Gsensor/TP/FAN	1A	
19	HDMI/THERMAL	1A	
20	USB3.0	1A	
21	WLAN/KB-BL	1A	
22	LED BD CON/USB BD CON	1A	
23	Sensors Hub & Sensors	1A	
24	POWER +VCC_CORE (NCP81101)	1A	
25	POWER 3VPCU&RVCC5(TPS51427)	1A	
26	POWER 1.35VSUS/VTT_MEM	1A	
27	POWER +1.05V(G5602R41U)	1A	
28	POWER VCC1.5/Thermal	1A	
29	POWER(BAT IN / ADA IN/ UL)	1A	
30	POWER CHARGER (ISL88732)	1A	
31	POWER VGA_CORE/1.0(RT8812A)	1A	
32	POWER VCC1.5_VRAM/1.05V	1A	
33	NVIDIA N14 GB2-64 PCIE 1/4	1A	
34	NVIDIA N14 GB2-64 TMDS 2/4	1A	
35	NVIDIA N14 GB2-64 VRAM 3/4	1A	
36	NVIDIA N14 GB2-64 VRAM 4/4	1A	
37	IO PORT LIST	1A	
38	SMBUS	1A	
39	Power Table	1A	

Page	Title of schematic page	Rev.	Date
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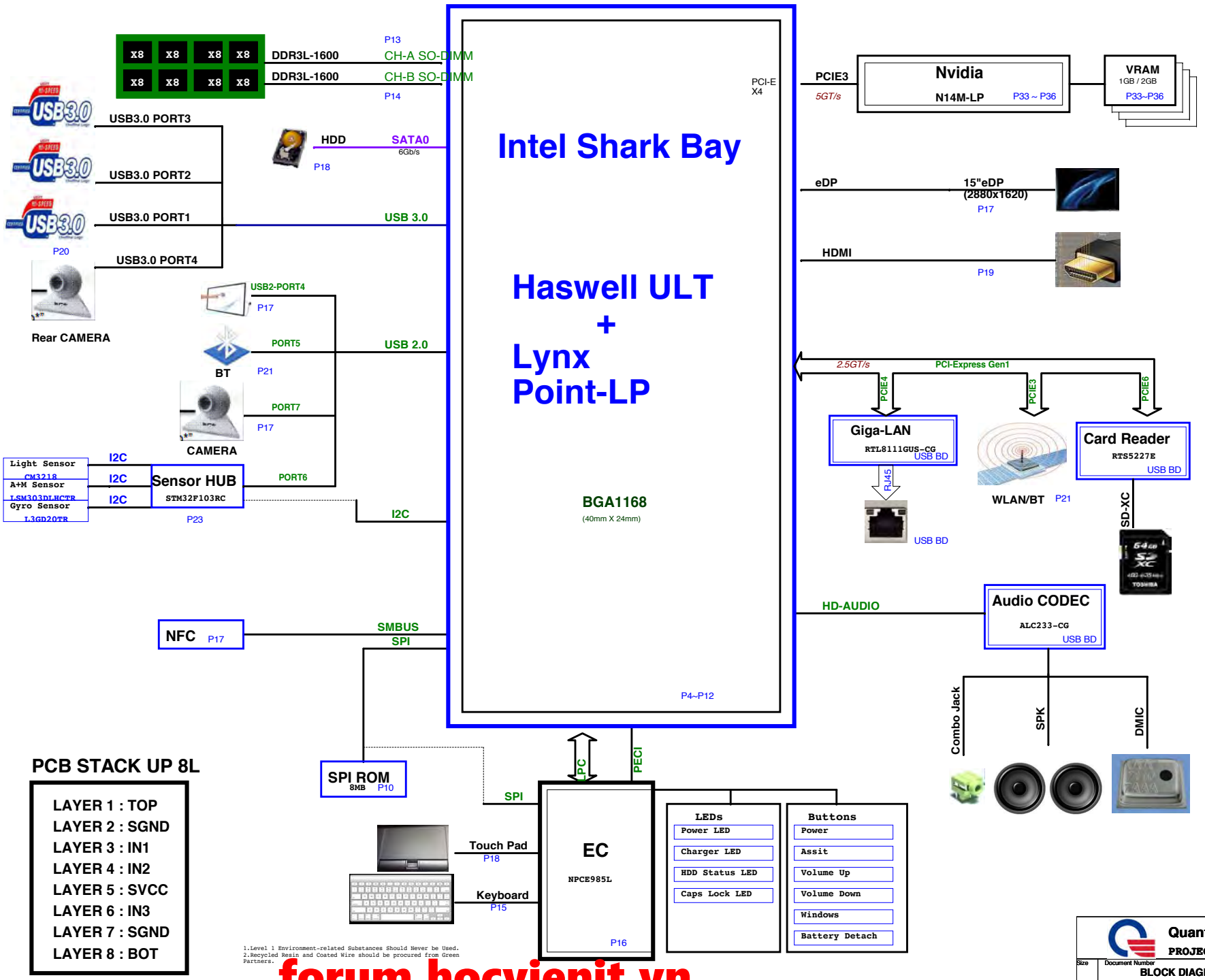
		1A	
		1A	
		1A	

1

* : No mount
E@ : For DIS GFX
I@ : For UMA

FI3 BLOCK DIAGRAM

02



PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

1.Level 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT : FI3

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Change List

MB_SCH_DVT_001

P14 Change footprint from 0603 to 0402

Reason : Corresponsive material with R149
Possible Risk: No.

MB_SCH_DVT_002

P9 Change USB port assignment

Reason : Design spec. change
Possible Risk: No.

MB_SCH_DVT_003

P18 Add USB 3.0 and control signal to CON16 .

Reason : Implement Rear camera
Possible Risk: Yes

MB_SCH_DVT_004

P4 Change netname of GPIO 78 from EC_A20GATE to GPIO78

P16 Remove EC_A20GATE

Reason : EC_A20GATE is not necessary and the GPIO for Rear CAM power enable .
Possible Risk: no

MB_SCH_DVT_005

P22 CON9/CON22 change pin assignment

Reason :Change USB2.0 to USB3.0 and implement RTD3 control signal for LAN .
Possible Risk: no

MB_SCH_DVT_006

P9 PCH GPIO29 use for WLAN_PW_EN

Reason :Change the power well of WLAN_PW_EN from sus to DSW. .
Possible Risk: no

MB_SCH_DVT_007

P11 Change GPIO08 for LAN_RST#
P11 PCH GPIO24 use for PCH_LAN_WAKE#

Reason :Implement RTD3 in LAN. .
Possible Risk: no

MB_SCH_DVT_008

P17 Change CON6 USB port assignment and add MODE_LID-2# to pin 12 of CON 6

Reason :USB port assignment change and add mode detection for stand mode .
Possible Risk: no

MB_SCH_DVT_009

P20 Add R24452 without mount for TPS2543 .

Reason :Reserve for TPS2543 .
Possible Risk: no

MB_SCH_DVT_010

P21 Remove D5 .

Reason :for cost down
Possible Risk: no

MB_SCH_DVT_011

P21 change R2442 from unmout to mount
P21 change R2444 from mout to unmount

Reason :Change PLTRST#_WLAN instead of PLTRST for RTD3
Possible Risk: no

MB_SCH_DVT_012

P15 Add serial resistor RP11~RP16 on K/B matrix

Reason :For ESD protection
Possible Risk: no

MB_SCH_DVT_013

P21 Add a AND gate for WLAN power enable

Reason :The power enable of WLAN can be controlled by application .
Possible Risk: no

MB_SCH_DVT_014

P21 Change WLAN_WAKE# PU power well from +3V_S5 to +3V_S5_DSW .

Reason :The signal is belong to" DSW " power well
Possible Risk: no

MB_SCH_DVT_015

P16 Change EC GPIO55 from DRAM_VOLTAGE_SET to SIO_WAKE_GPIO27#
P16 Change EC GPIO84 from NV_ALERT_EC# to EC_WLAN_PWR_EN

Reason :For WLAN iSCT control
Possible Risk: no

MB_SCH_DVT_016

P16 Change EC GPIO32 from IMVP_PWRGD to MODE_LID-2#
P16 add KR28 PU for MODE_LID-2#
Reason :Mode detction for stand mode
Possible Risk: no

MB_SCH_DVT_017

P34 Remove NV_ALERT_EC#

Reason :This signal didn't implement .
Possible Risk: no

MB_SCH_DVT_018

P11 Change PCH GPIO12 as LAN_ISOLATE#

P22 Add LAN_ISOLATE# on pin28 of CON9

Reason :For LAN RTD3.
Possible Risk: no

MB_SCH_DVT_019

P18 Change CON16 from 20 pin to 30 pin connector

MB_SCH_DVT_020

P8 Change Y1 package for Broadwell requirement

MB_SCH_DVT_021

P21 Change CON13 to DFH52M059

MB_SCH_DVT_022

P11 GPIO59 use for R_CAM_ON

MB_SCH_DVT_023

P18 Add Q41
P18 Add Q37,Q38, Q40,R24453,R24454,C2340
P18 add R24456 100K ohm pull down on R_CAM_ON
P18 Change Q24 from DDTC144EUA to 2N7002W
P18 Change Q23 from 2N7002W to 2N7002DW
P18 Remove R2437 0 ohm and R2436 (0 ohm NC)
P18 Add R219,R24455,C2415,C2416,U53
P18 Add F24

MB_SCH_DVT_024

P11 Change HDD_PW_EN from GPIO90 to GPIO13
P11 Change R302 from 10k ohm pull high to 100k ohm pull down
P11 Add R24463 ,R24462 100K pull down for CR_PW_EN and GPU_PW_EN

MB_SCH_DVT_025

P23 add R24457 ,R24458 100K ohm pull down
P23 Remove reserve resistor , R2450 ,R2384

MB_SCH_DVT_026

P17 add R24459 ,R24460,R24461 100K ohm pull down
P17 Remove reserve resistor , R180,R258,R259,R2435,R2434,R2450

MB_SCH_DVT_027

P11 Change R293,R304,R310,R308,R289,R297,R306 from mount to un-mount .
P10 Remove RP4 , Add R24464 10 K ohm for CCD_PWR_EN without mount , add R24465 10K ohm for GPIO11 with mount .
P11 Change R118 from NC to mount

MB_SCH_DVT_028

P4 Change the netname of GPIO77 from EC_EXT_SMI# to GPIO77
P11 Change the netname of GPIO35 from GPIO35 to EC_EXT_SMI#

MB_SCH_DVT_029(2013-05-08)

P16 Add KC16 150 pF without mount
P16 Add KD5
P18 Add C2359 220pF
P18 Change Q21,Q37,Q38 from TPCC8067-H to NTTFS4C10N
P17 Change U5,U18,U26 from G5254T11U to G527ATP11U
P17 Remove R24448 ,R24447,R382 1.9Kohm
P17 Add R24466 ,R24467,R24468 40.2Kohm
P23 Change U29 from G5254T11U to G527ATP11U
P23 Remove R2449 1.9Kohm
P23 Add R24469 40.2Kohm

MB_SCH_DVT_029(2013-05-08)

P18 Add R24470 40.2Kohm
P18 Change U29 from G5254HT11U to G527ATP11U
P18 Remove R24455 1Kohm

MB_SCH_DVT_030(2013-05-09)

P11 Change netname of GPIO47 from GPIO47 to DB_DET
P18 Add Q42 2N7002W
P18 Add Q42 2N7002W
P12 Add C475 0.47uF
P21 Change U27 from TPS2557DRBR to G547E1P81U
P21 Remove R2454 100K ohm

MB_SCH_DVT_031(2013-05-10)

P11 Change netname of GPIO16 from GPIO16 to DB_DET
P12 Change Q8 from 2N7002W to NTTFS4C10N
P14 Change R271, R272, R273, R274, R275, R276, R277 from 10k ohm to 100k ohm
P7 Change R42 from 10k ohm to 100k ohm
P8 Change R278, R279, R280, R280, R281 from 10k ohm to 100k ohm
P9 Change R73, R282 from 10k ohm to 100k ohm
P10 Change R24464(no mount), R24465, R86 from 10k ohm to 100k ohm
P10 Change R283, R285, R300, R315, R313, R317,
R115, R296, R298, R299, R301, R303, R305, R307, R309, R312,
R314, R316(no mount), R318, R319, R320, R293(no mount), R290,
R291, R304(no mount), R294, R310(no mount), R308(no mount),
R284, R112, R288, R311, R292, R287, R295, R116, R117, R118, R119,
R286, R289(no mount), R297(no mount), R114, R122, R306(no mount),
R125(no mount), R126, R127(no mount), R128, R129(no mount), R130,
R131(no mount), R132, R133(no mount), R134, R135(GPU SKU only)
from 10k ohm to 100k ohm

P15 Change KR2, KR4, KR19, KR26, KR27, KR28 from 10k ohm to 100k ohm
P21 Change R24445,R2446 from 10k ohm to 100k ohm
P4 Change R14,R15 from 10k ohm to 100k ohm

MB_SCH_DVT_032(2013-05-14)

P23 Add R24471 100K ohm for SH_ALS_INT#

MB_SCH_DVT_033(2013-05-16)

P15 Change H1,H3,H4 footprint

MB_SCH_DVT_034(2013-05-17)

P23 U29 PIN1 change +3V_SENSORHUB for optional non CS design
P23 R2451 PIN2 change +3V_S5 for optional non CS design

MB_SCH_DVT_035(2013-05-18)

P23 R2451 mount
P23 change U29 ,C2337,R24469,R2449,R24457 to un-mout
P21 Add R24472 0 ohm
P21 Mount R2444
P21 Un-mount R2446,R24442,Q34,Q35,R2447,U28,R2442,R2443,U30

MB_SCH_DVT_036(2013-05-21)

P11 Mount R310
P18 Mount R2440
P17 CON6 change FP and P/N .
P15 CON4 change FP and P/N .
P21 CON14 change FP and P/N .
P22 CON9 and CON22 change FP and P/N .

MB_SCH_DVT_037(2013-05-28)

P17 Change CON6 Footprint

MB_SCH_DVT_038(2013-05-29)

P22 Change LAN_RST# ,LAN_ISOLATE# , PCH_LAN_WAKE# to CON22

P22 Change CON9 pin define

MB_SCH_DVT_039(2013-05-30)

P7 Add R24475 ,R24476,R24479,R24480 0 ohm
P7 Add C2417,C2418,C2419,C2420 0.1 uF
P7 Add U54,U55 74LVC1G07GW
P7 R24474 ,R24473,R24478,R24477 without mount 0 ohm
P7 Change C49 to mount 680pF from un-mount
P7 Change R41,R44 pull up t0 +3V_S5 from +3V
P22 Change PCH_LAN_WAKE# to pin29 on CON22
P22 Change ACZ_SDOUT to pin28 on CON22
P23 Mount R2359,R2361,R2363,R2365,R2367,R2369 10k ohm

MB_SCH_DVT_040(2013-05-31)

P11 Change R288 to un-mount
P17 Add U56 TC7SH08FU
P17 Add R24481 100K ohm
P9 Add R24482 100K ohm
P9 Add U57 TC7SH08FU
P9 Add C2421 0.1uF
P9 R24483 without mount
P19 Change HR22,HR25 from 2.2Kohm to 4.7k ohm
P19 Change HR20,HR33 from un-mount to mount 4.7k ohm
P34 Change VC78,VC79 from 12pF to 10pF
P23 Change C2300,C2301 from 22pF to 18pF

MB_SCH_DVT_041(2013-06-02)

P18 Change pin 5 and pin 6 of +5V_HDD_+3V_SSD_F to GND on CON16
P18 Change pin 7 of +3V_CCD to GND on CON16

MB_SCH_DVT_042(2013-06-03)

P22 Change F10,F11,F12 Footprint

MB_SCH_DVT_043(2013-06-04)

P20 Add C2432 ,C2433,C2434 0.22uF without mount
P16 Add KR29 100k ohm
P7 Add C2435 3.3pF
P13 Add C2437,C2436 ,C2441 3.3pF
P13 Change C2112 ,C2114 from NC to mount 3.3pF
P14 Change C160,C162 from NC to mount 3.3pF
P14 Add C2438,C2439,C2440 3.3pF
P17 Add C2442,C2443 3.3pF
P18 Add R24484,R24485,R24486,R24487

MB_SCH_DVT_044(2013-06-05)

P21 Change R24441 from mount to un-mount .
P22 Change CON22 from 40 pin to 44pin
P15 Change H7 NUT P/N

MB_SCH_DVT_045(2013-06-07)

P8 Change R59,R60,R61 ,R64,R65,R66 from mount to un-mout .

MB_SCH_DVT_046(2013-06-10)

P18 Change C276 from 220p to 1000p

MB_SCH_DVT_047(2013-06-11)

P11 Change R126 value from 100k_4 to E@100K_4
P11 Change R125 value from *100K_4 to I@100K_4
P29 Change PR167 from 470K/NTC to 680K/NTC for ajusting thermal trigger point
P29 Change PR171 from 6.98K to 0 for ajusting thermal trigger point

MB_SCH_PVT_001(2013-07-07)

P22 Change CON9 From 50281-00301-001 to 50501-03001-001

MB_SCH_PVT_002(2013-07-013)

P08 Add Q46 , R24484 for no power issue(un-mount)
P16 EC GPIO85 add EC_RTC_RST for workaround solution
P17 Change F2 from fast fuse to poly switch fuse .
P07 BOM remove C2417,C2418,C2419,C2420,U54,U55
P07 R40,R24475,R24476,R24479,R24480 change to short pad.
P12 R138,R139 change to short pad.
P13 R161,r163 change to short pad.
P14 R2145 change to short pad.
P16 KL1,KR25,KR18 change to short pad.
P17 Remove F6,C297 ,Add U58,C2444,R24485,R24487,R24486,C2445
P21 R2445 change to short pad.

MB_SCH_PVT_003(2013-07-016)

P24 Change PR24, PR26, PR11, PR7 to short pad.
P25 Change PR43, PR230, PR53, PR45, PR52, PR54, PR36, PR48, PR85 to short pad.
P26 Change PC61 from 0.01uF to NC for E/E request on power sequence.
P26 Del PR100 for layout space saving
P27 Change PR114 to short pad.
P28 Change PR117 to short pad.
P28 Change PR148 from 374K to 330K to fine-tune UVP trigger point.
P30 Add PC134 1000PF
P31 Change VPR11, VPR23, VPR25 to short pad.
P32 Change VPR41 to short pad.

MB_SCH_PVT_004(2013-07-017)

P18 CON18 change FP .

MB_SCH_PVT_005(2013-07-018)

P18 Add R24488 100K ohm

MB_SCH_PVT_006(2013-07-020)

P12 Add C2446,C2447,C2448,C2449,C2450,C2451,C2452,C2453 220 pF for EMI requirement
P04 R2412 change to short pad
P10 R95,r96,R97,R98 change to short pad
P17 R2448 change to short pad
P18 R219 change to short pad

MB_SCH_PVT_007(2013-07-022)

P11 Change R308,R306 from NC to mount .
P17 Change R24459,r24461,C294,C295 from mount to unmount .
P22 Change R262,R264 from 75ohm to 220 ohm
P22 Change R264 from 75ohm to 100 ohm

MB_SCH_PVT_008(2013-07-023)

P17 Add Resever pad D24
P18 Change C276 from 1000pF to 4700pF

MB_SCH_PVT_009(2013-07-024)

P9 Change VC157,VC158,VC159,VC160,VC161,VC162,VC163,VC164 from 0.1u to 0.22u

MB_SCH_PVT_009(2013-07-024)

P25 Change PR38 from 255K to 196K for fine-tuning OCP.

MB_SCH_PVT_010(2013-07-026)

P22 Change R261 from 470ohm to 120 ohm
P22 Change R263 from 75ohm to 220 ohm

MB_SCH_PVT_011(2013-07-30)

P17 Change C2331 and C2333 from 1uF to 2.2uF
P17 Change C2332 from 0.1uF to 2.2uF

MB_SCH_PVT_012(2013-08-04)

P19 Change HR33 ,R228,R229,R24450,R24451 to NC .
P19 Change R28 to 42.2K ,change R212 to 17.8K ,change R204 to 60.4k , change R210
to 24.9K , change R216 to 76.8K , change R218 to 32.4k

P17 Change C2442,C220,C2443 to 10u and change C228 to mount 22uF from NC .

MB_SCH_PVT-1_001(2013-08-06)

P17 Change F2 fuse type from poly switch to fast fuse --considering cable burn out issue .
P10 Add damping resistor R24489,R24490,R24491,R24492,R24493 on LPC bus : solve siganl overshoot and undershoot issue

MB_SCH_PVT-1_002(2013-08-09)

P15 Remove D21 and D23 , H3 and H6 connect to GND for EMI request .

MB_SCH_PVT-1_003(2013-08-15)

P8 Correct Q46 connection.
P23 Remove C2308,C2309,C2310,C2312,R2390,R2392,C2315,U23 --E-compass move to LED BD
P23 Add CON27

MB_SCH_PVT-1_004(2013-08-18)

P17 Change CON6 pin 11 from MODE_LID# to +LCDVCC for Backup solution of OFHD panel
P17 Add R24494
P17 Remove MOD_LID# and reserve it in EC

MB_SCH_PVT-1_005(2013-08-21)

P8 Change Q46/R24484 from um-mount to mount

MB REV. E

MB_SCH_PVT-2_001(2013-08-23)

P17 reserve R24495,R24496,R24497 to co-lay LVDS power switch between GMT and UPI

MB_SCH_PVT-2_002(2013-08-30)

P17 Change VIN source of U6 from +3V to +3V_WAKE

P17 R24497/R24495 : NC , R24496 mount

MB_SCH_PVT-3_002(2013-09-16)

P11 Change R315 from mount to un-mount

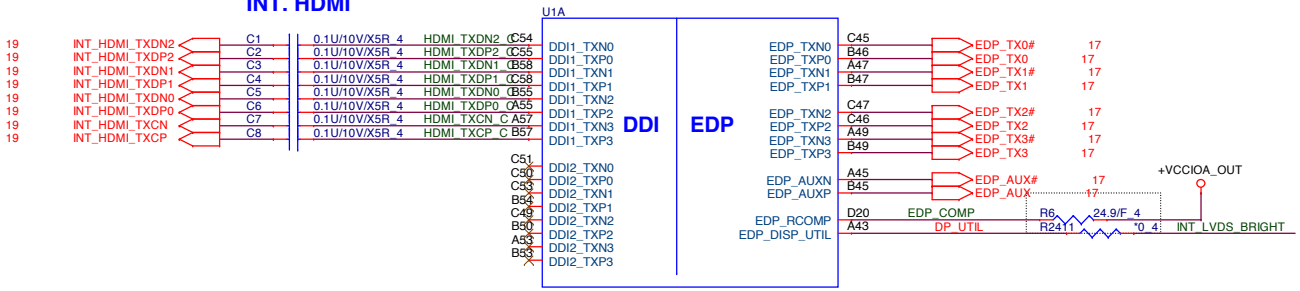
MB_SCH_PVT-3_004(2013-09-22)

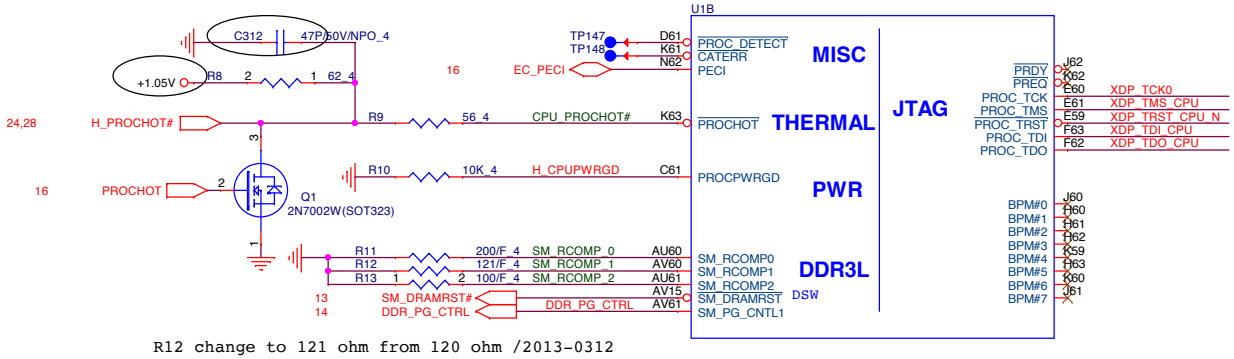
P17 Change U6 from G5243 to BCD AP22802

MB_SCH_PVT-3_005(2013-10-08)

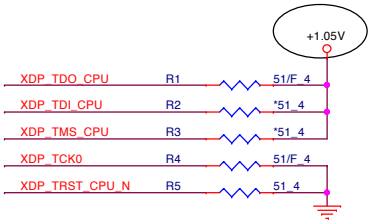
P34 Add VRAM ID for Micron VRAM

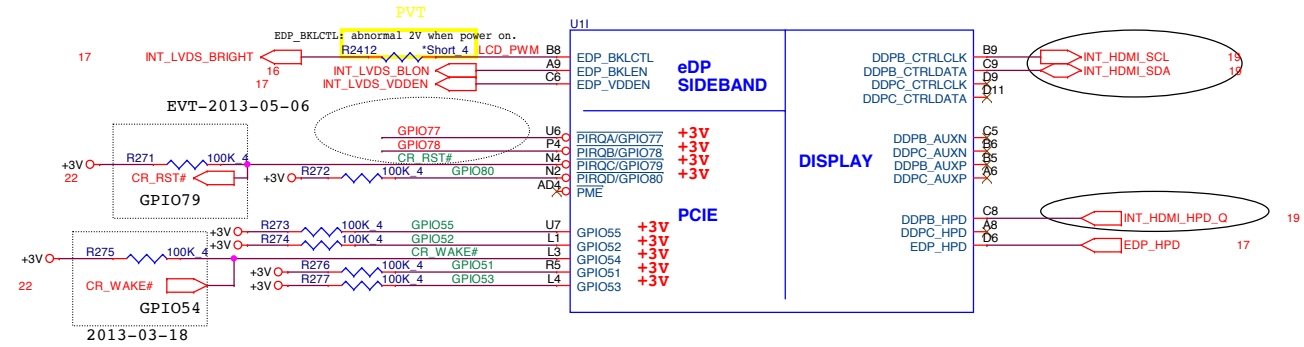
Haswell ULT (DISPLAY)

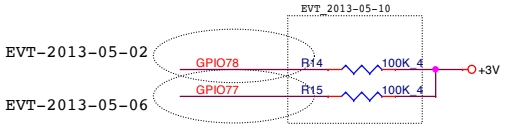




R12 change to 121 ohm from 120 ohm /2013-0312







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Quanta Computer Inc.
PROJECT : FI3

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	HSW MCP(Display/eDP)	1C
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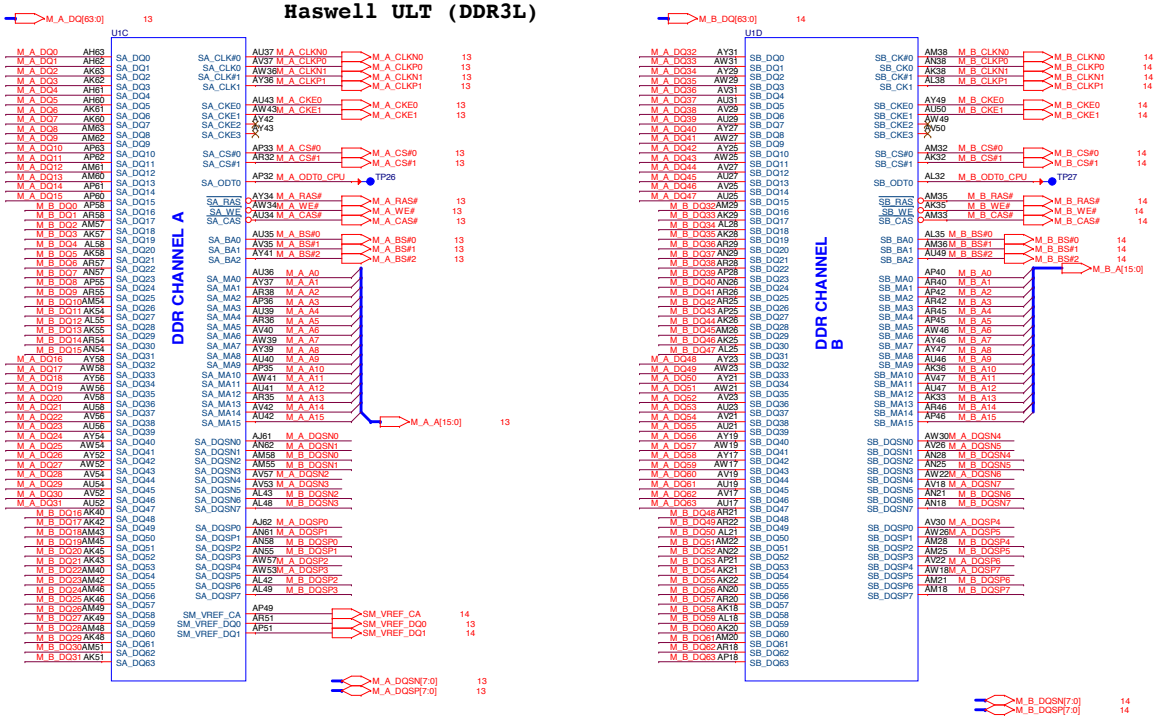
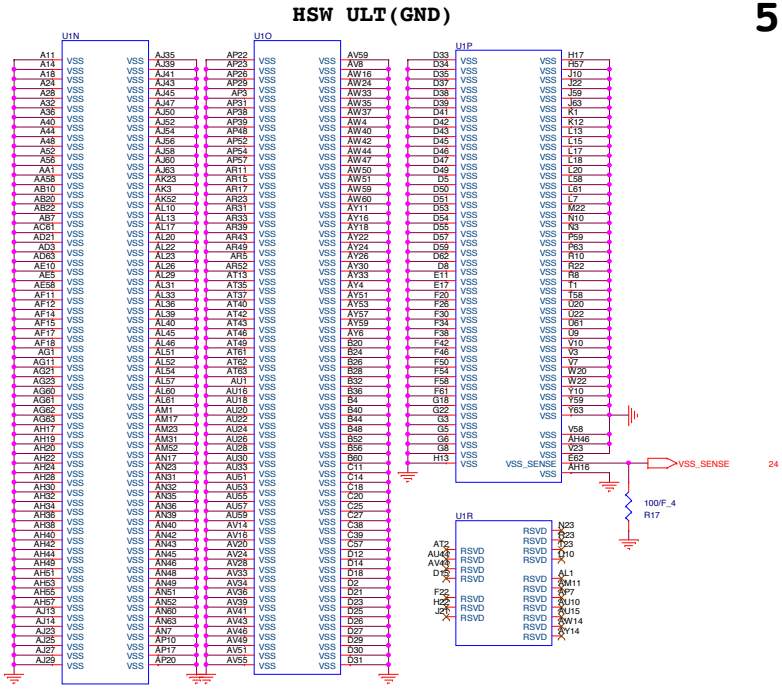
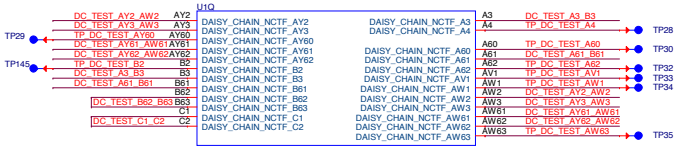
Haswell ULT (DDR3L)



HSW ULT(GND)





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Quanta Computer Inc.
PROJECT :FI3

Size	Document Number	Rev
	HSW MCP(Memory)	1C
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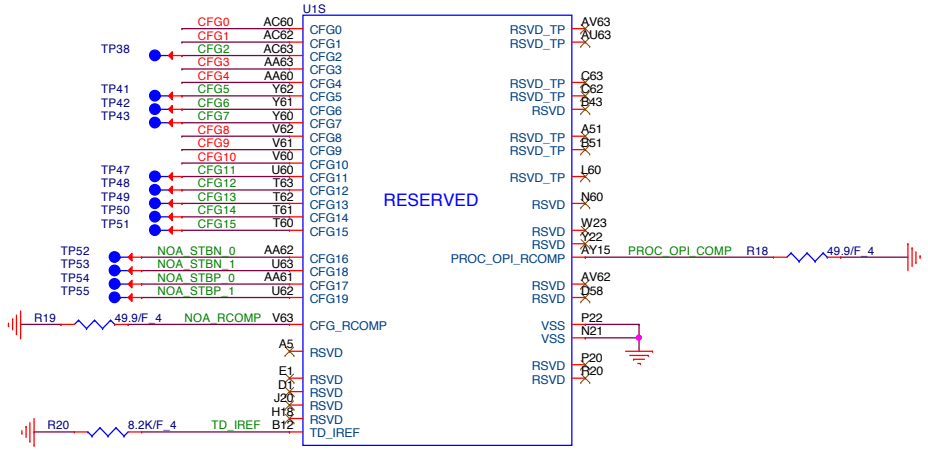
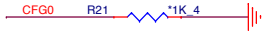
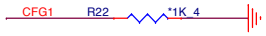
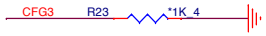
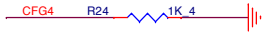
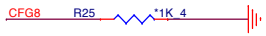
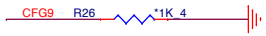
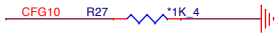


Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	

1.Level 1 Environment-related Substances Should Never be Used.
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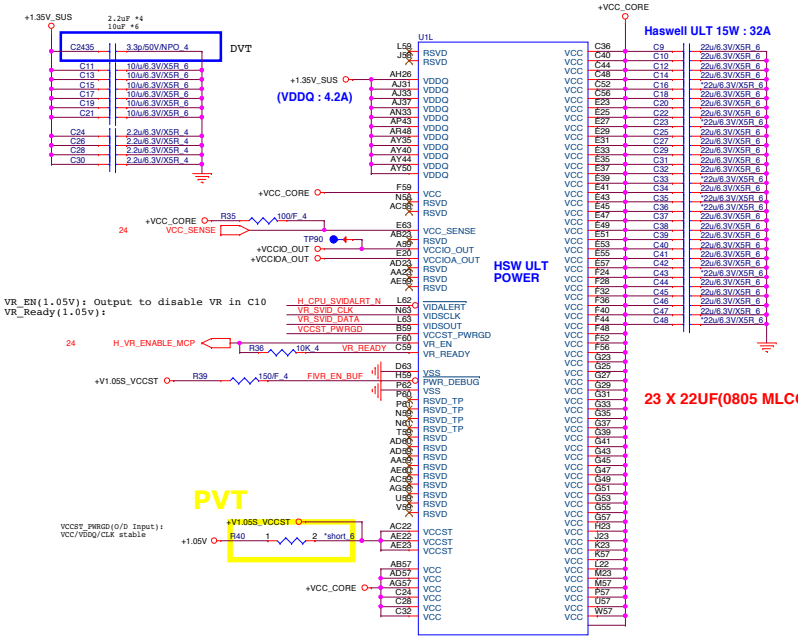
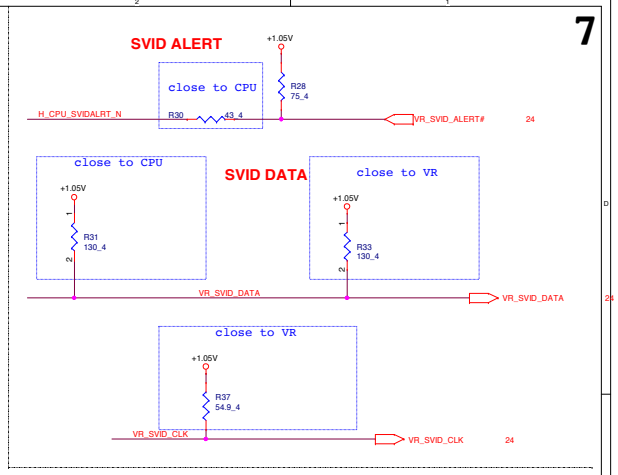
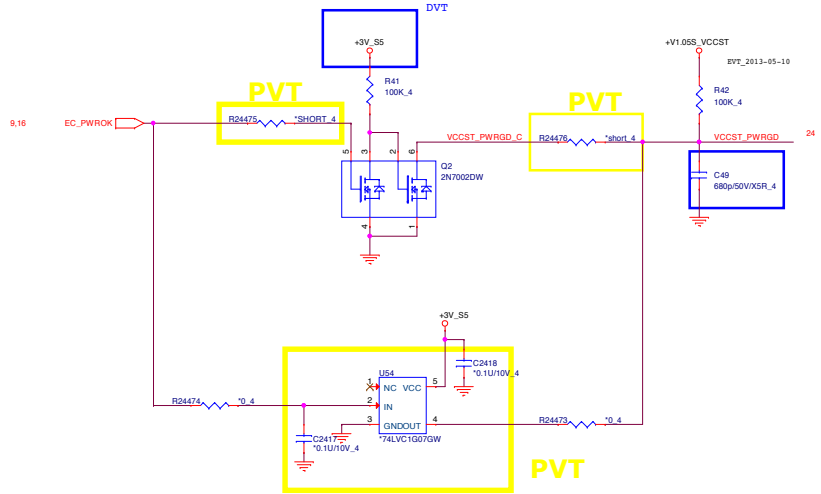
Quanta Computer Inc.
PROJECT : FI3

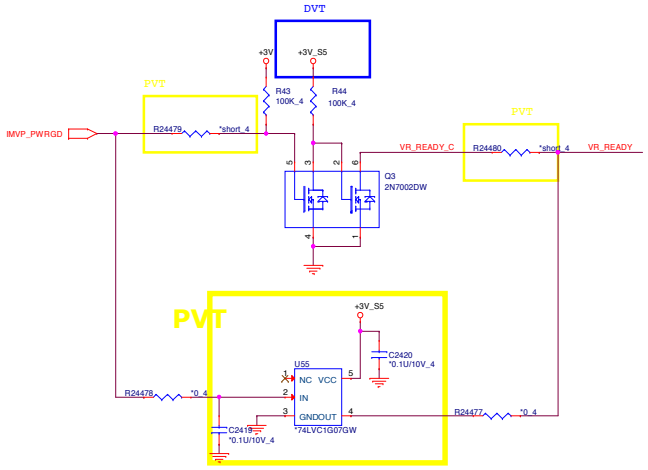
Size	Document Number	Rev
	HSW MCP(CFG)	1C
Date: Tuesday, October 08, 2013	Sheet 6 of 40	

Haswell ULT MCP(POWER)





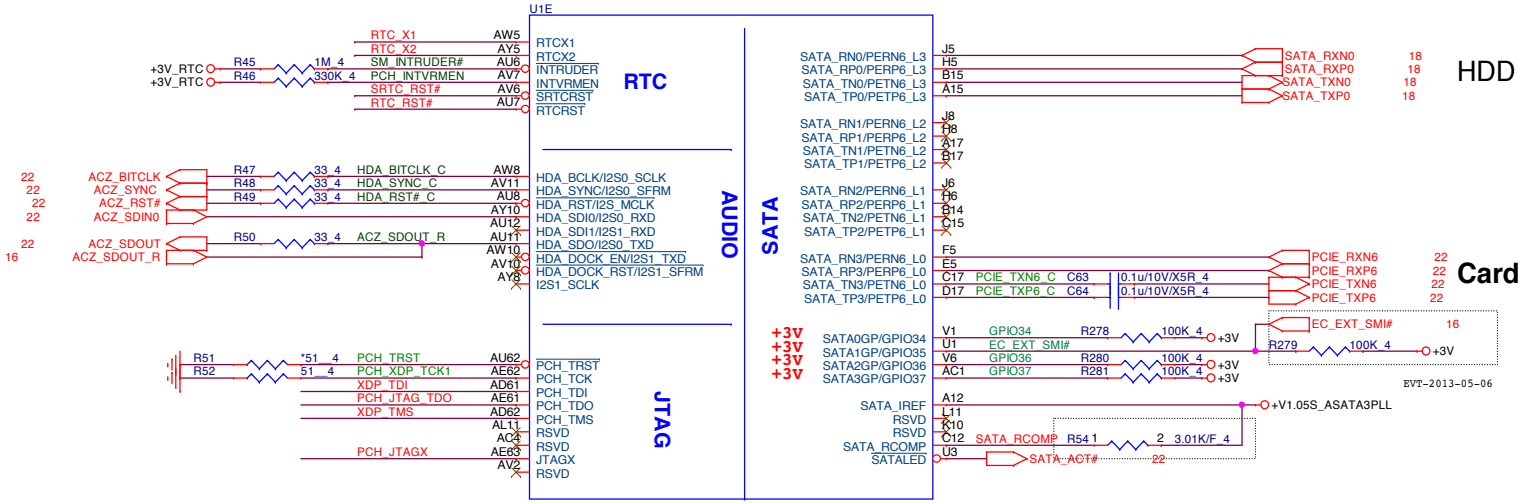


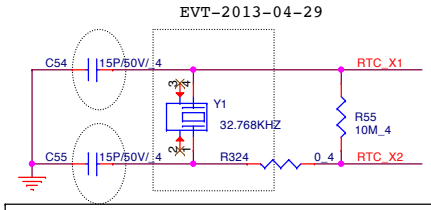


Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HSW MCP(Power)	1C
Date: Tuesday, October 08, 2013	Sheet 7 of 40	

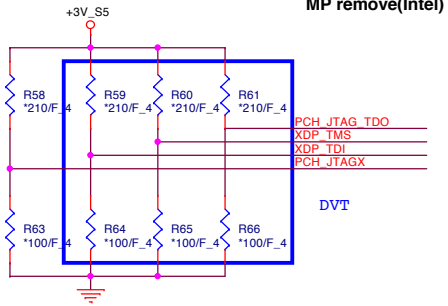
Haswell ULT (RTC, HDA, JTAG, SATA)

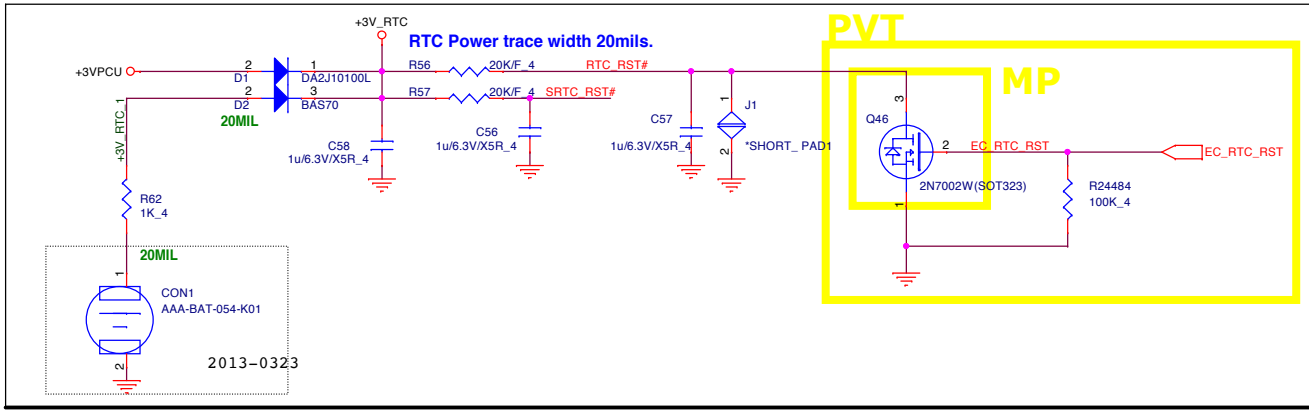




PCH JTAG Debug (CLG)

MP remove(Intel)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R67 *1K_4 SPKR 11,22
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

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2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HSW PCH(RTC/HDA/SATA)	1C
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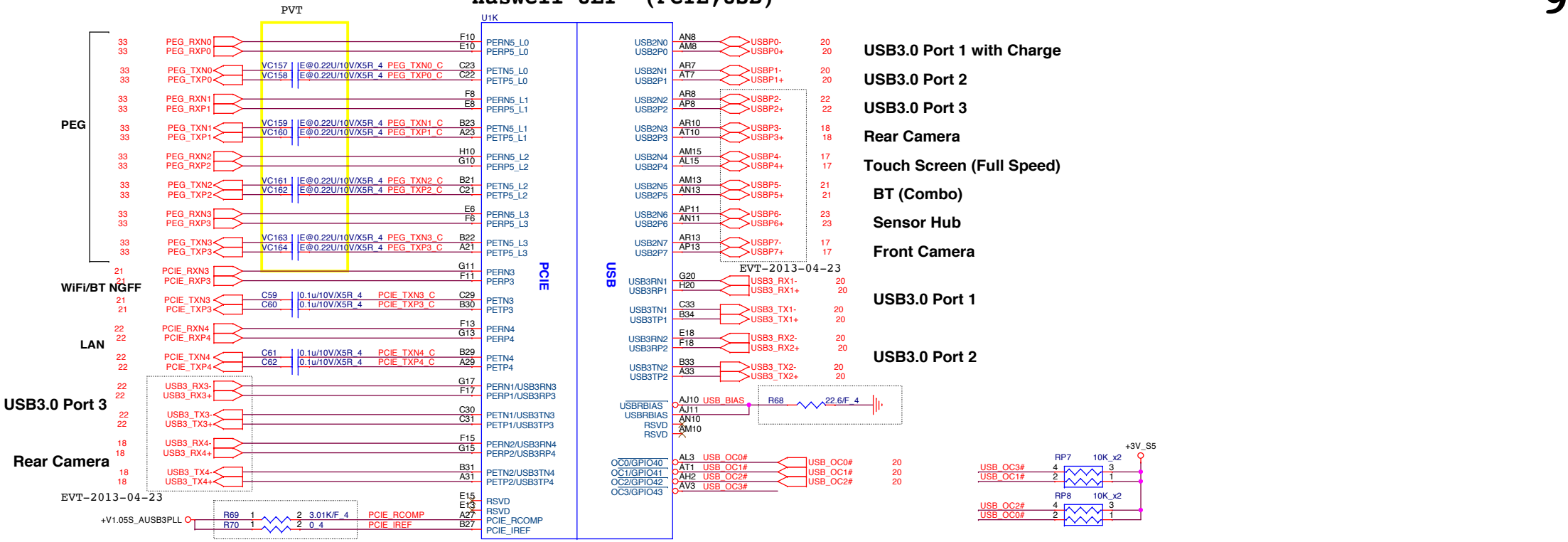
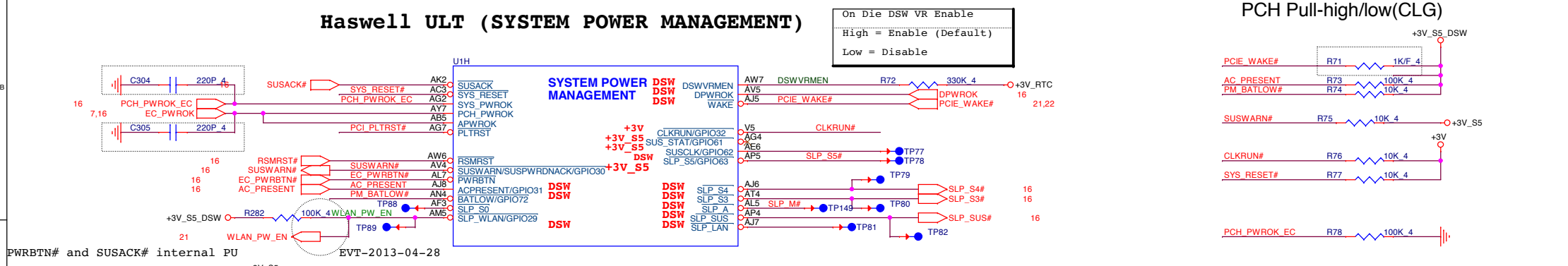
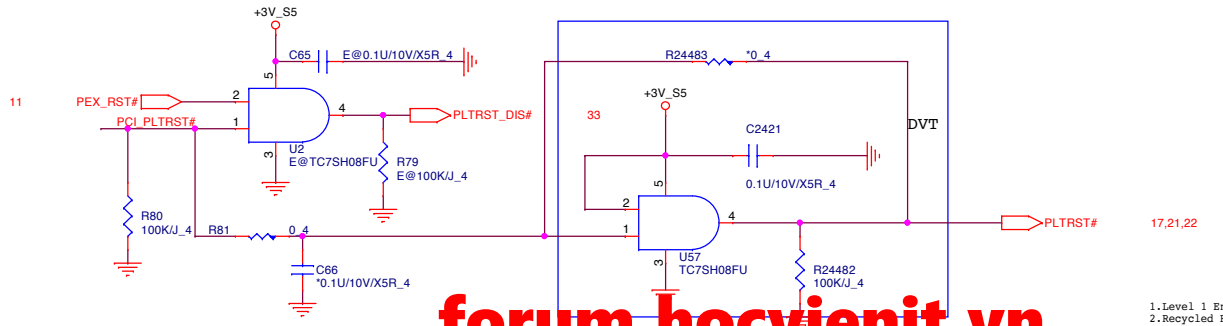
Haswell ULT (PCIE,USB)



Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



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PROJECT : FI3

Size	Document Number	Rev
	HSW PCH(PCIE/USB)	1C
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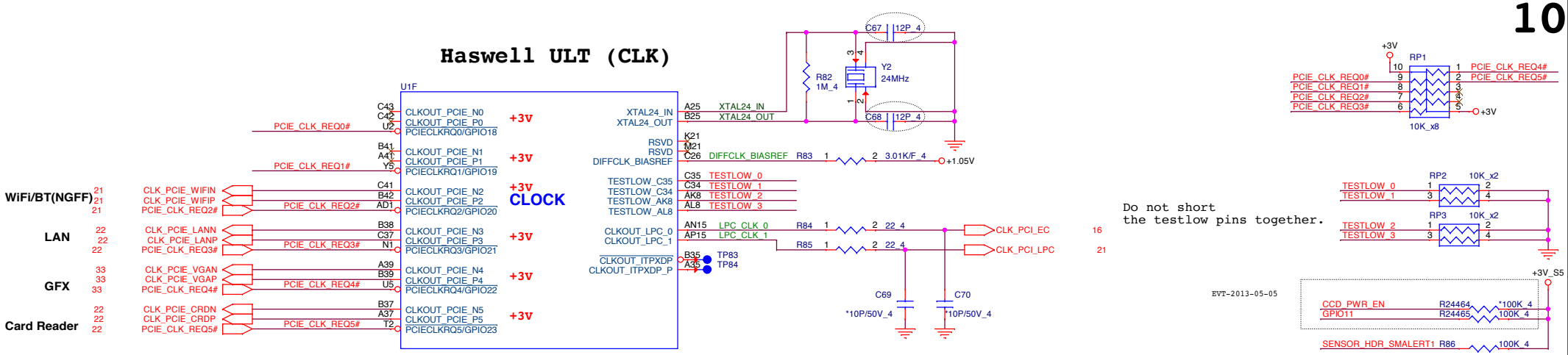
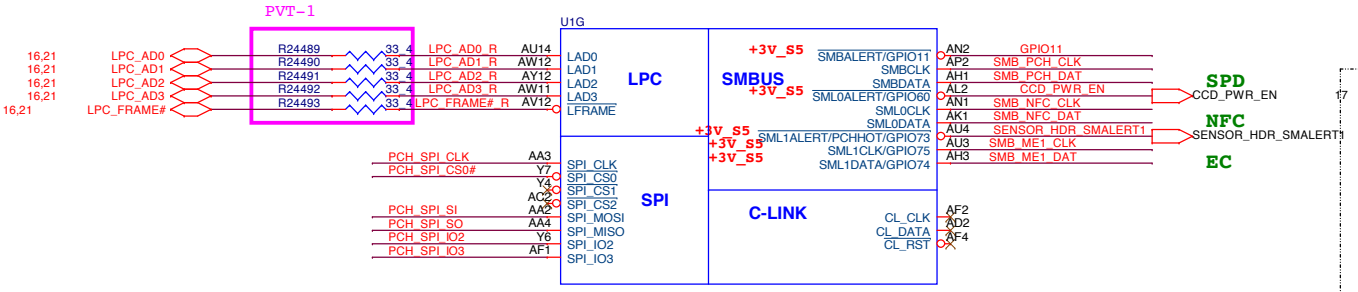
Haswell ULT (CLK)

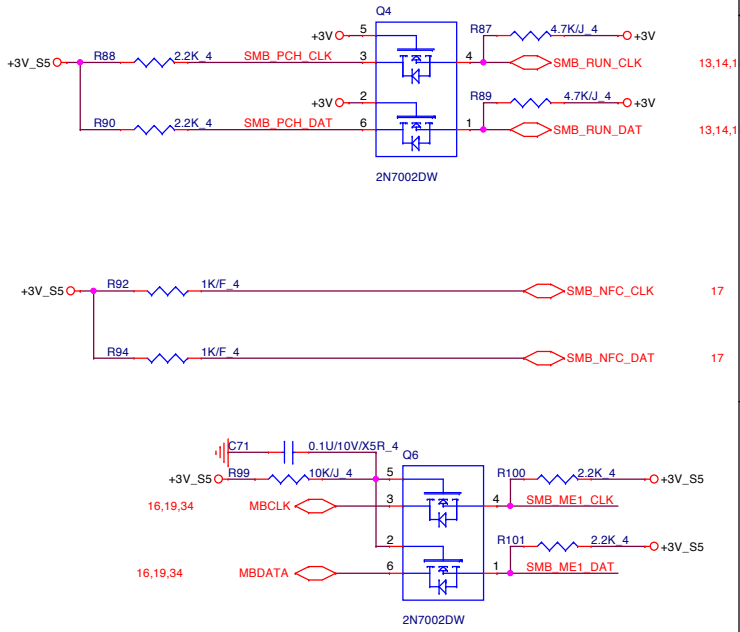


Do not short
the testlow pins together.

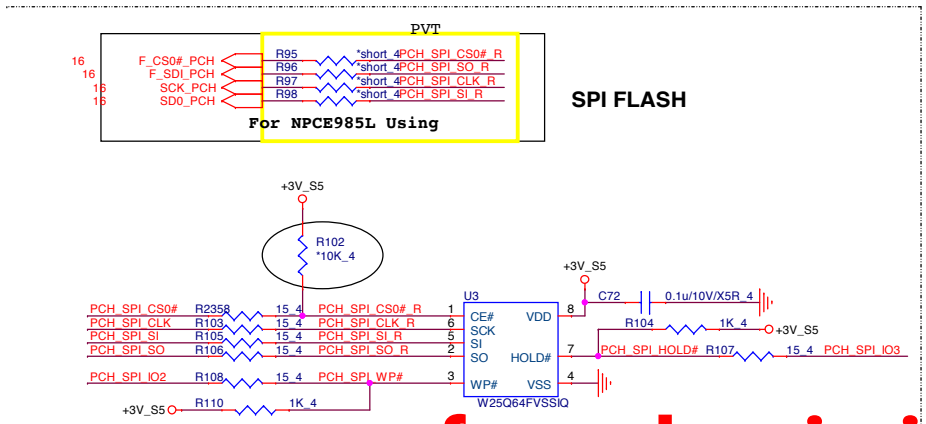
Haswell ULT (LPC/SPI/SMB/CLINK)



SMBus/Pull-up(CLG)



SPI FLASH



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	1C
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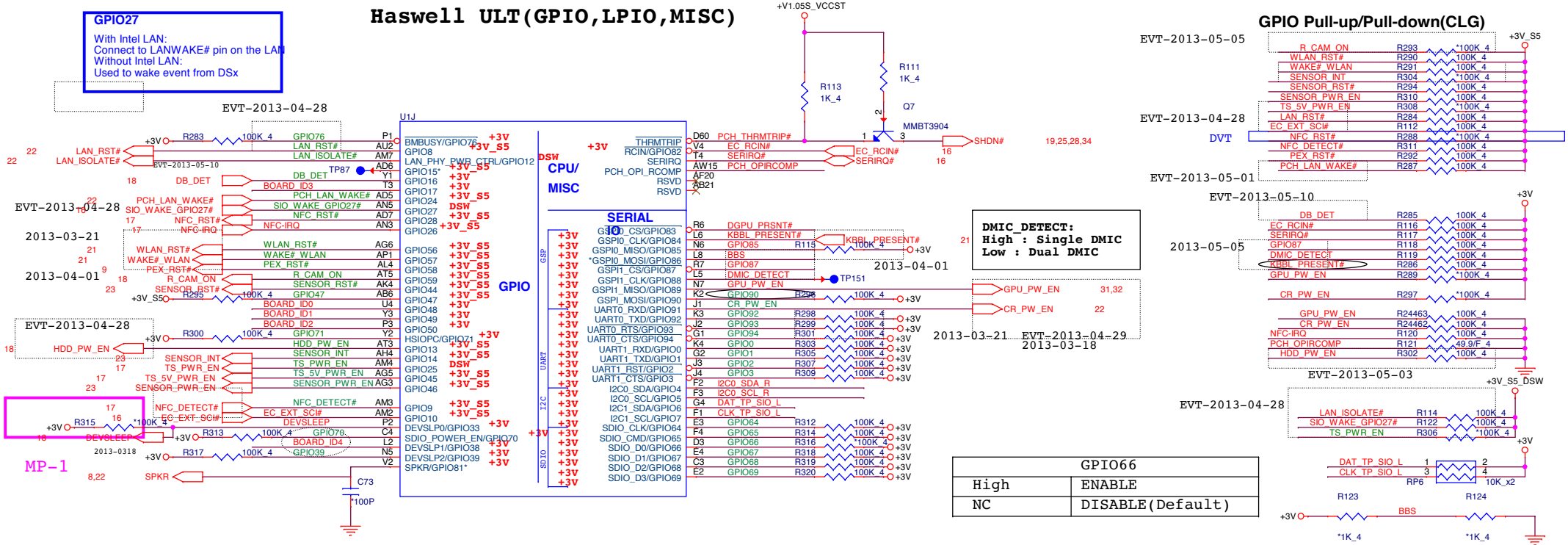
Haswell ULT(GPIO,LPIO,MISC)

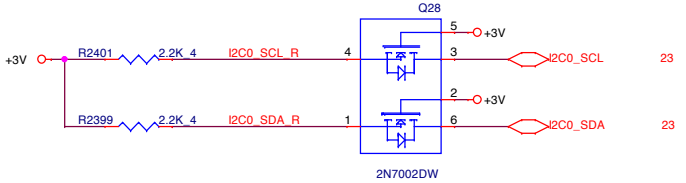
GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

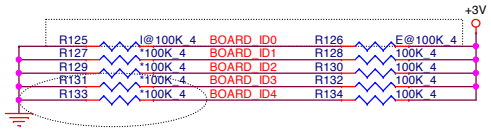


DMIC_DETECT:
High : Single DMIC
Low : Dual DMIC

GPIO66	
High	ENABLE
NC	DISABLE(Default)

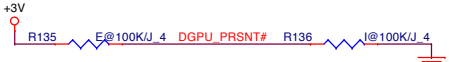
GPIO Pull-up/Pull-down(CLG)





R127(Low) R128(High)
R125(Low) R126(High)

	Board ID1	Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1



PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HSW PCH(GPIO/MISC)	1C
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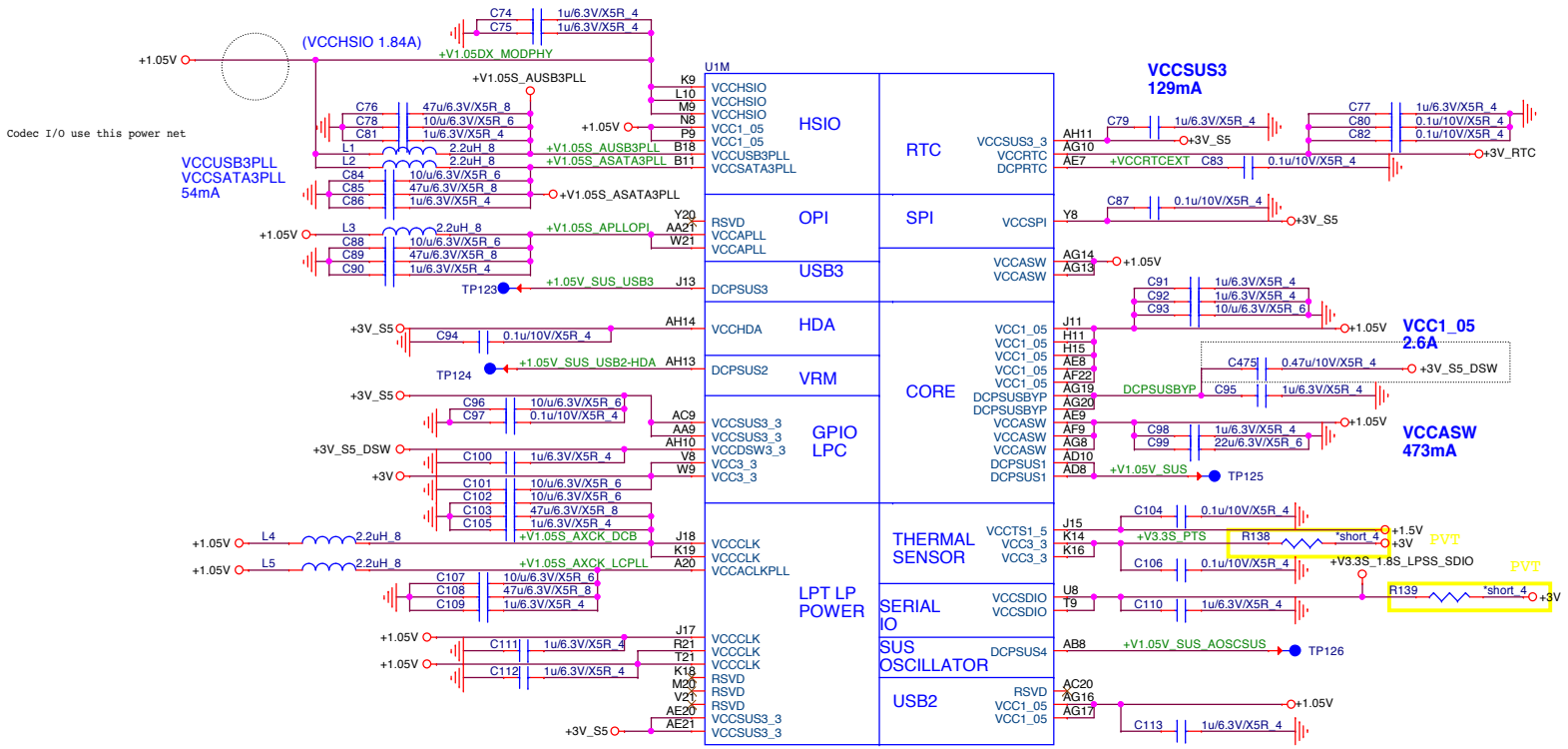
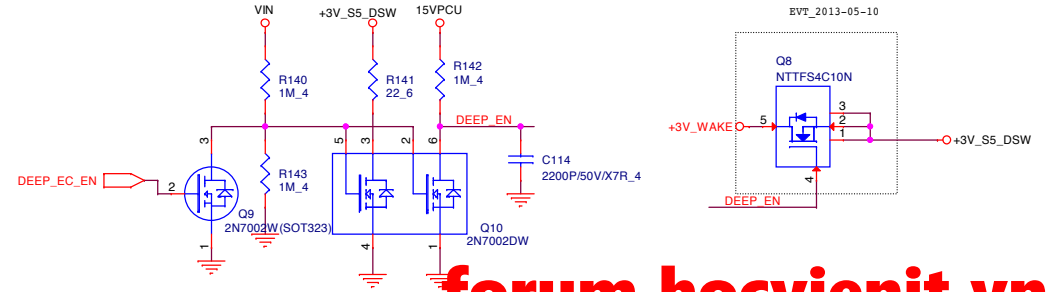


DEEP STANDBY



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HSW PCH(Power)	1C
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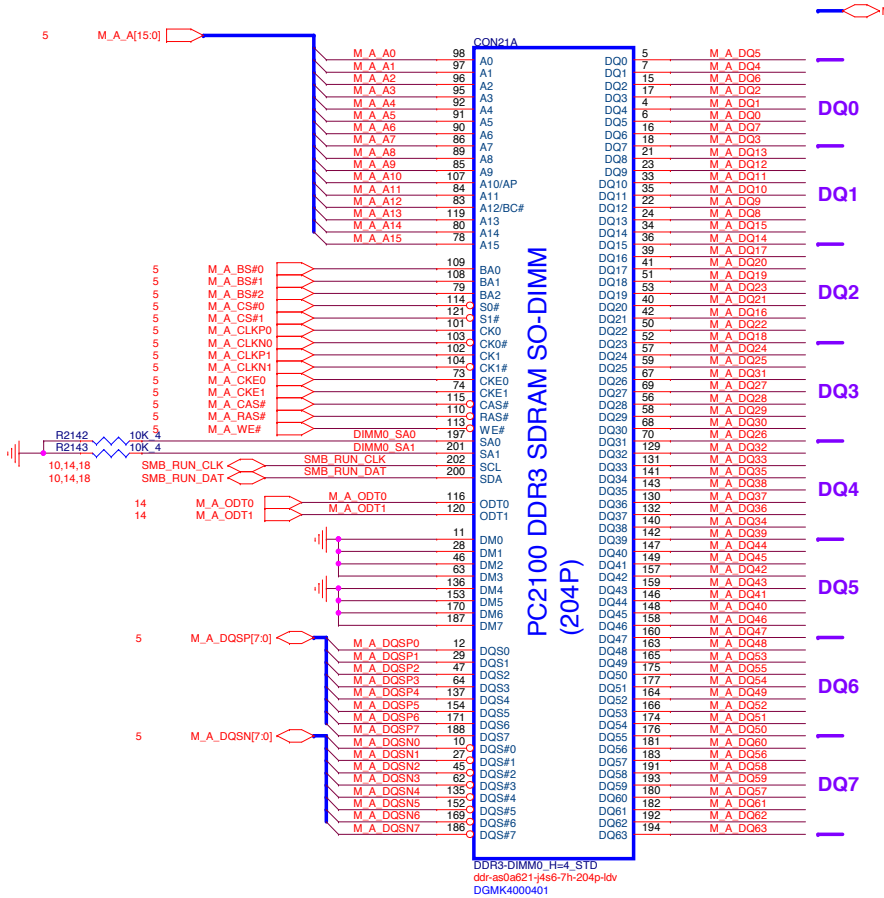

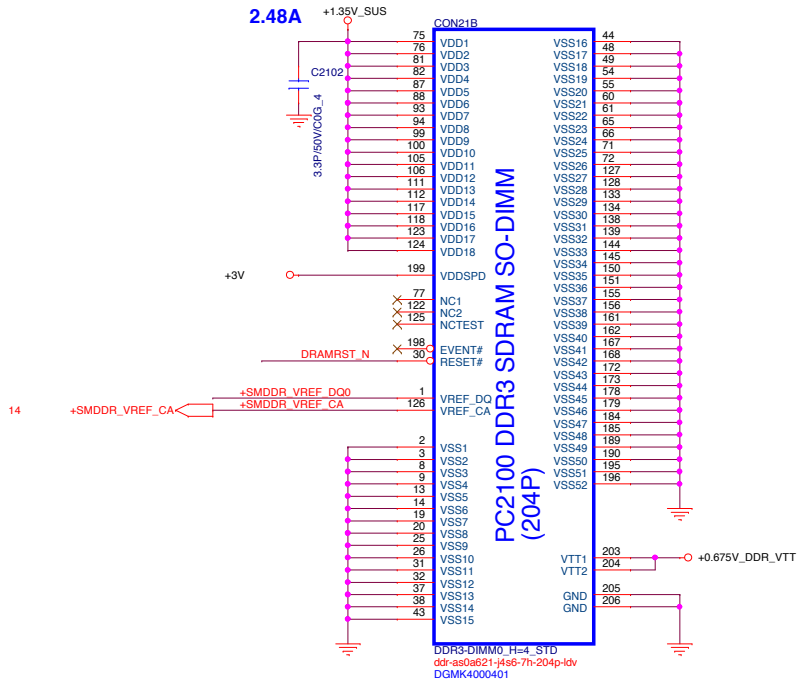

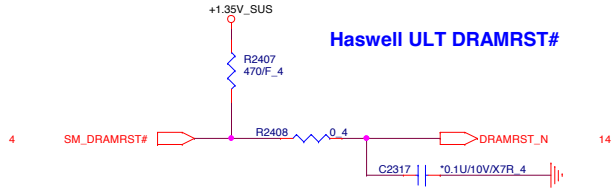

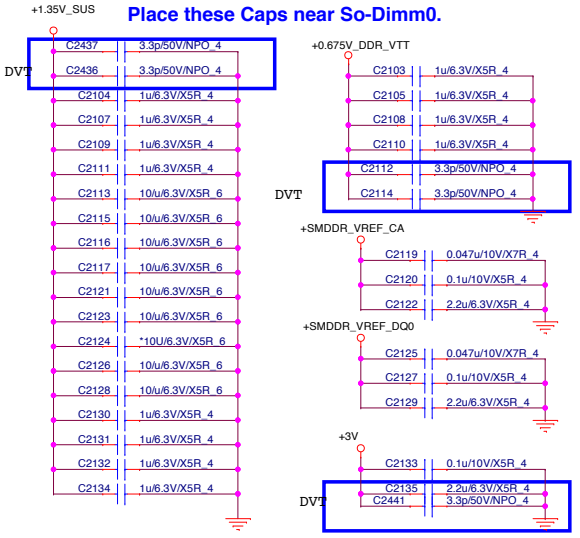

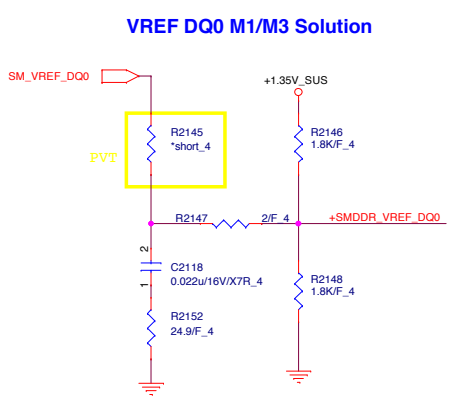

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	DDR3L DIMM0-STD 4H (CH-A)	1C
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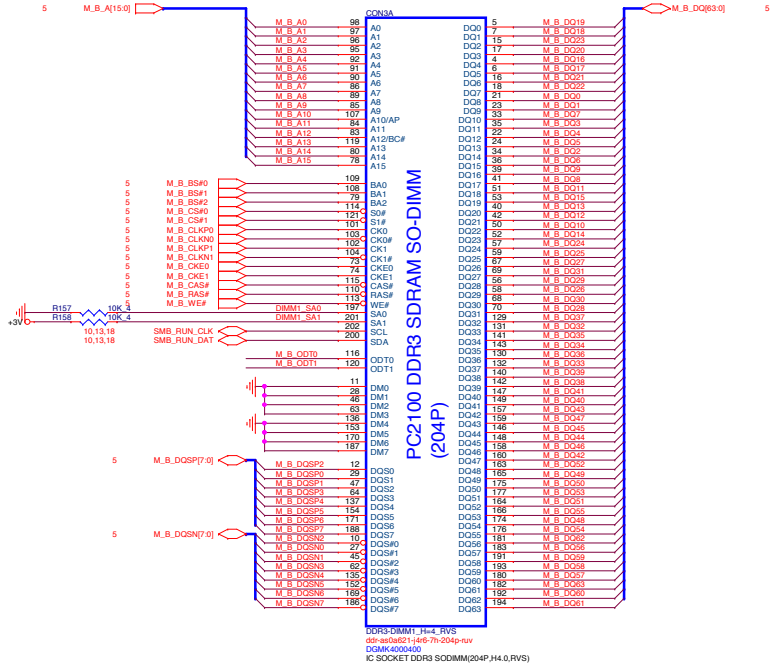

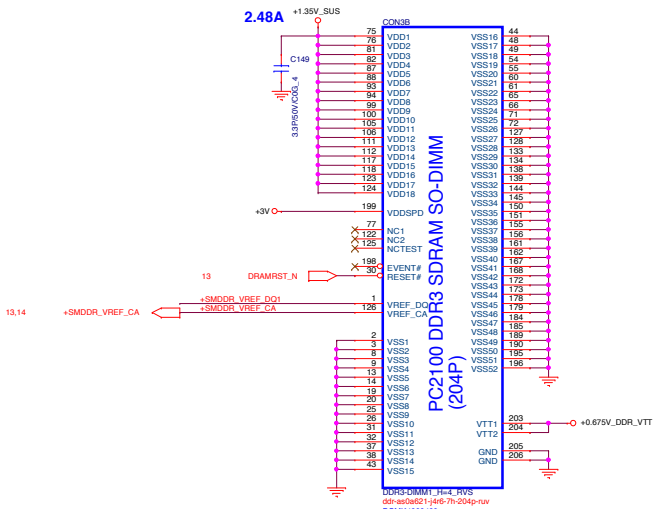

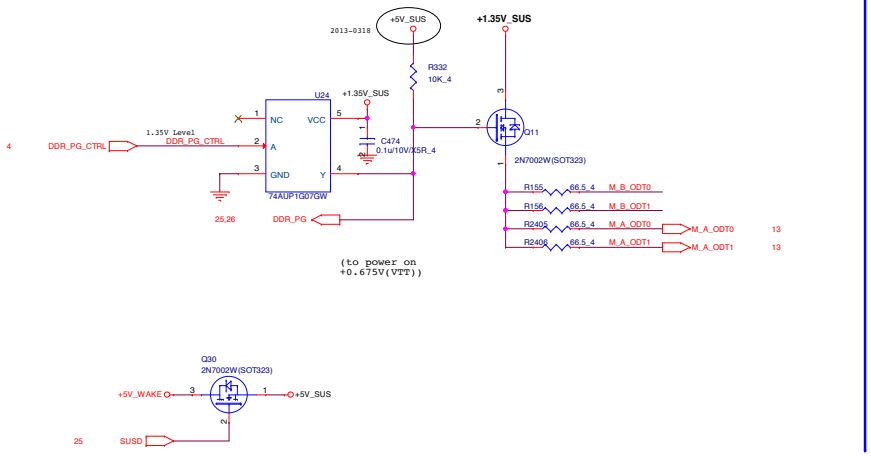

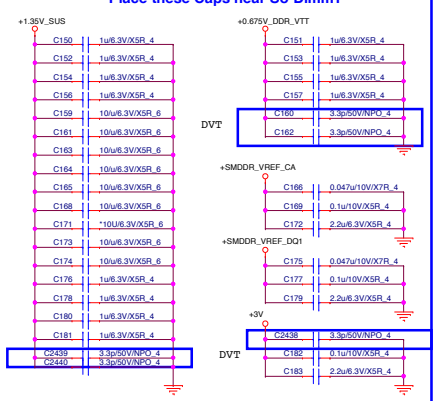

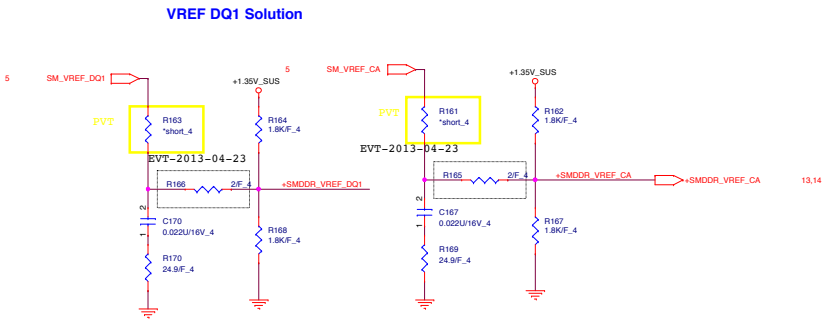

1.Level 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	DDR3L DIMM1-RVS 4H (CH-B)	1C

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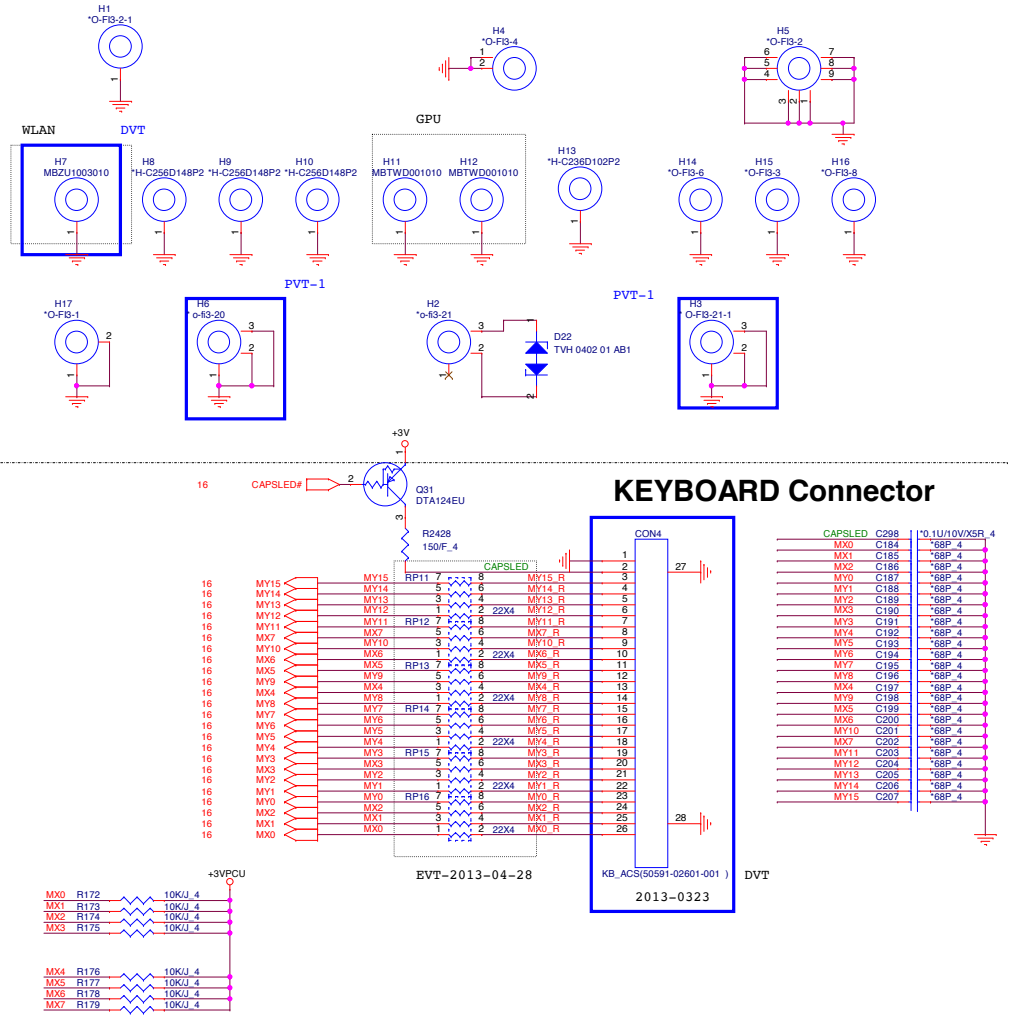

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Quanta Computer Inc.
PROJECT :FI3

Size	Document Number	Rev
	HOLE/EMI/KB	1C
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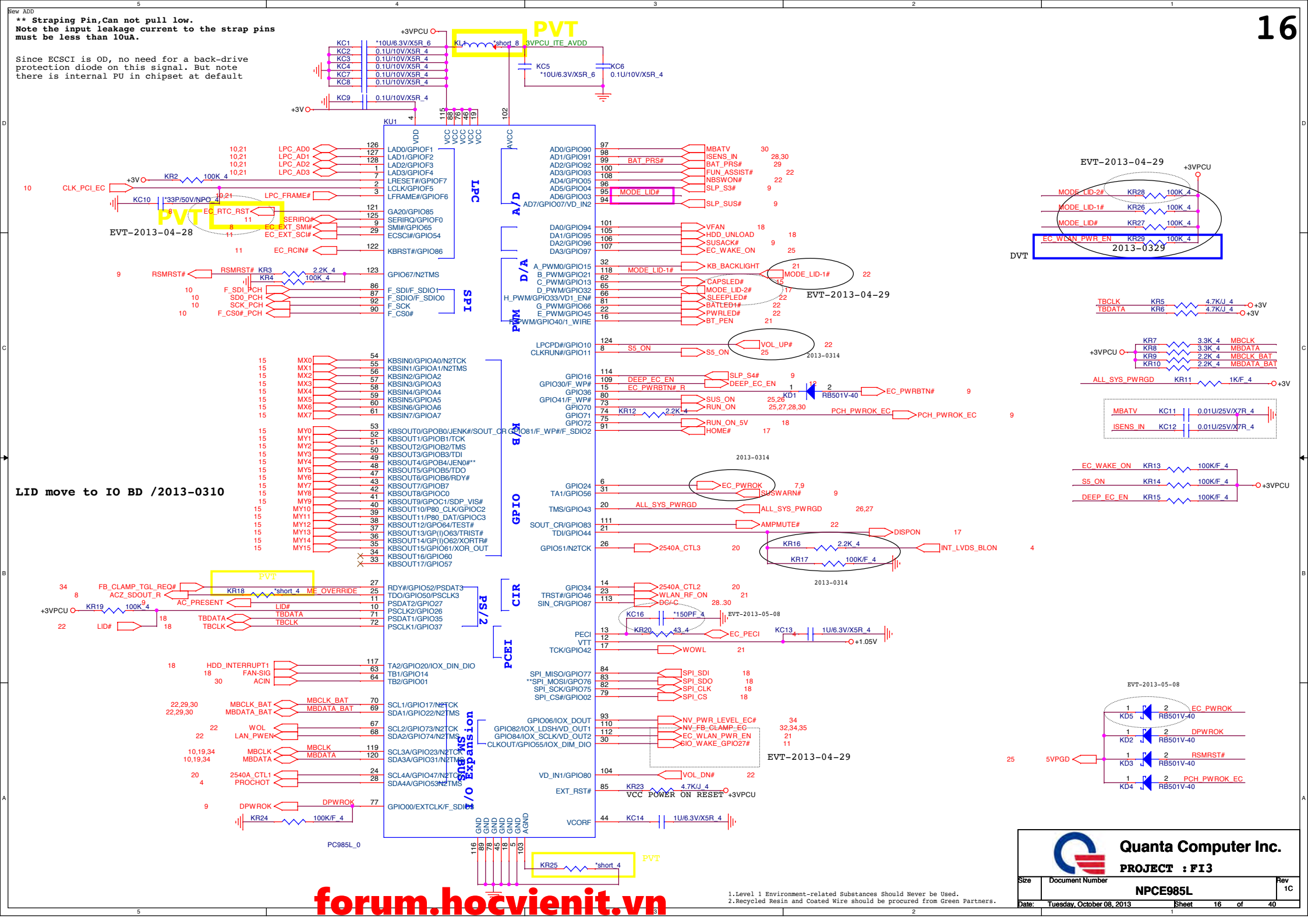
New ADD

** Straping Pin,Can not pull low.
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

LID move to IO BD /2013-0310



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	NPCE985L	1C
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Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

Current limit
Typ:1A(880mA~1120mA)

USB Camera Power

Current limit
Typ:1A(880mA~1120mA)

DMIC

Current limit
Typ:1A(880mA~1120mA)

Current limit
Typ:1A(880mA~1120mA)

eDP

FAST,UL/CSA

Camera

Touch Screen

EVT-2013-04-28

EVT-2013-04-23

NB LVDS enable

AU LCDVCC:
I rush = 2A/0.5ms
IDD = 0.3A

Pin Configuration

G5243A

SOT-23-5

Pin Configuration

NFC

NFC module :
Vender : Samsung SNC-i20
Power consumption : Max. 160mW/48mA
Power Ripple +/- 50mV

Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	eDP/TS/Camera/NFC	1C

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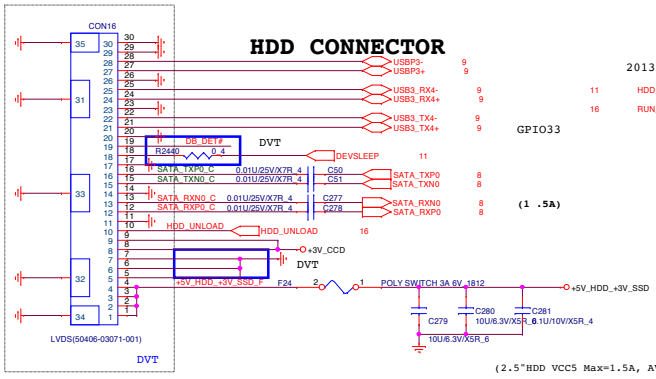
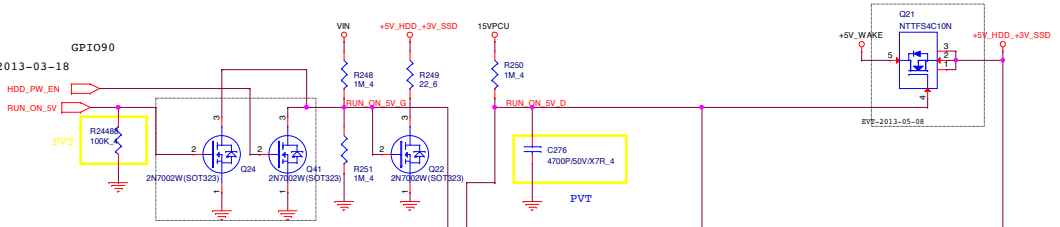
HDD CONNECTOR



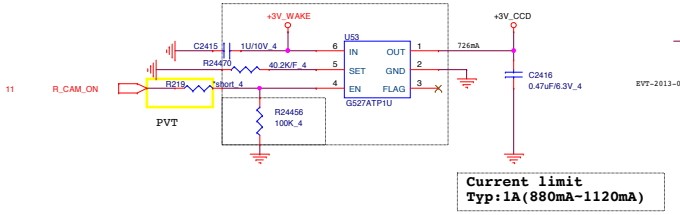
2013-03-18

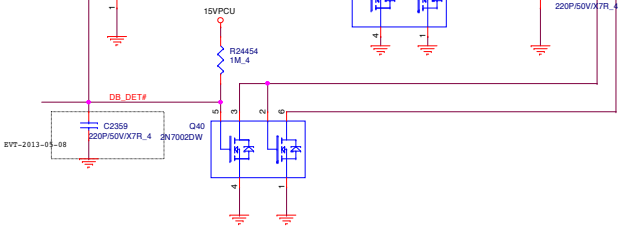
GPIO90

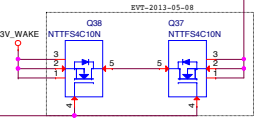


(2.5"HDD VCC5 Max=1.5A, AVG=0.6A)

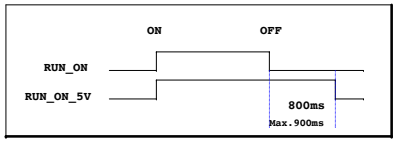
(2.5"SSD VCC5 typ=0.8A,Max=1.54A)



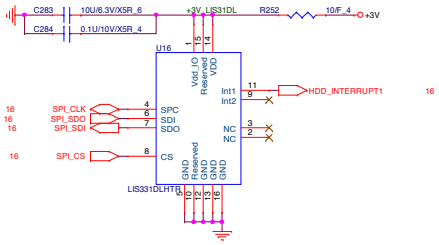




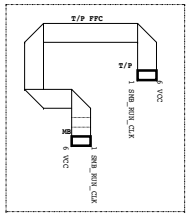
Current limit
Typ:1A(880mA~1120mA)

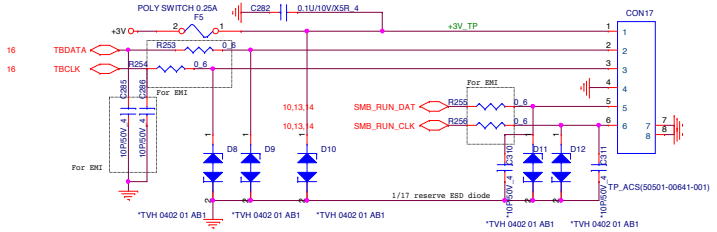


HDD PROTECT SPI INTERFACE

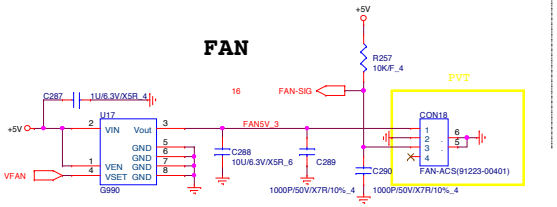


T/P Board to T/P





FAN



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :FI3

Size	Document Number	Rev
	HDD/ODD/TP/FAN	1C

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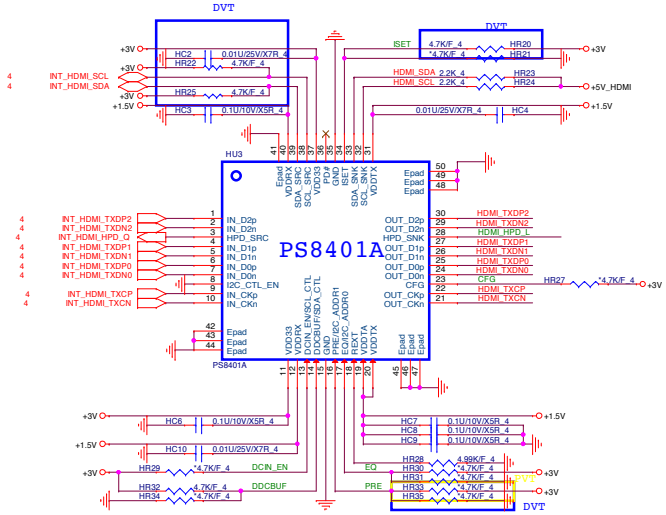
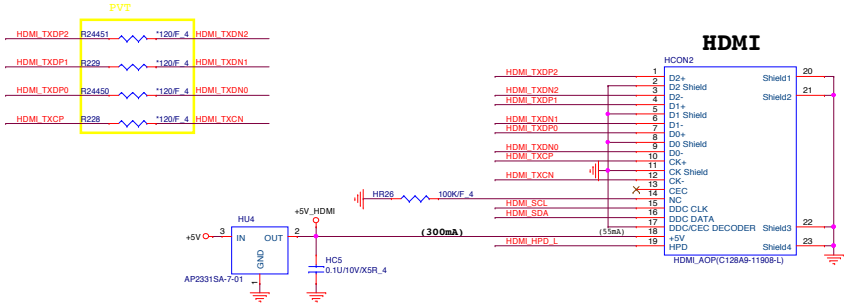
3 Level Input:
L: LOW, internal pull down.
H: High, external pull up.
M: VDD33/2, both external pull-up and pull-down.





DCIN_EN: DC cou;ing enable; Internal pull down at ~150k, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

EQ: Receiver equalization setting; Internal pull down at ~150k, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

ISET: TMDS output swing adjustment; Internal pull down at ~150k, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

DDCBUF: Enable active DDC buffer; Internal pull up at ~150K, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: passive DDC pass-through with internal ~10K pull up resistor

PRE: Output pre-emphasis setting; Internal pull down at ~150k, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

CFG: Configuration pin, 3.3V IO, internal pull down at ~150k. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable

Move to sub Board

RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

95	18.5K
100	15K
107	10.3K
110	8.2K

T.B.D

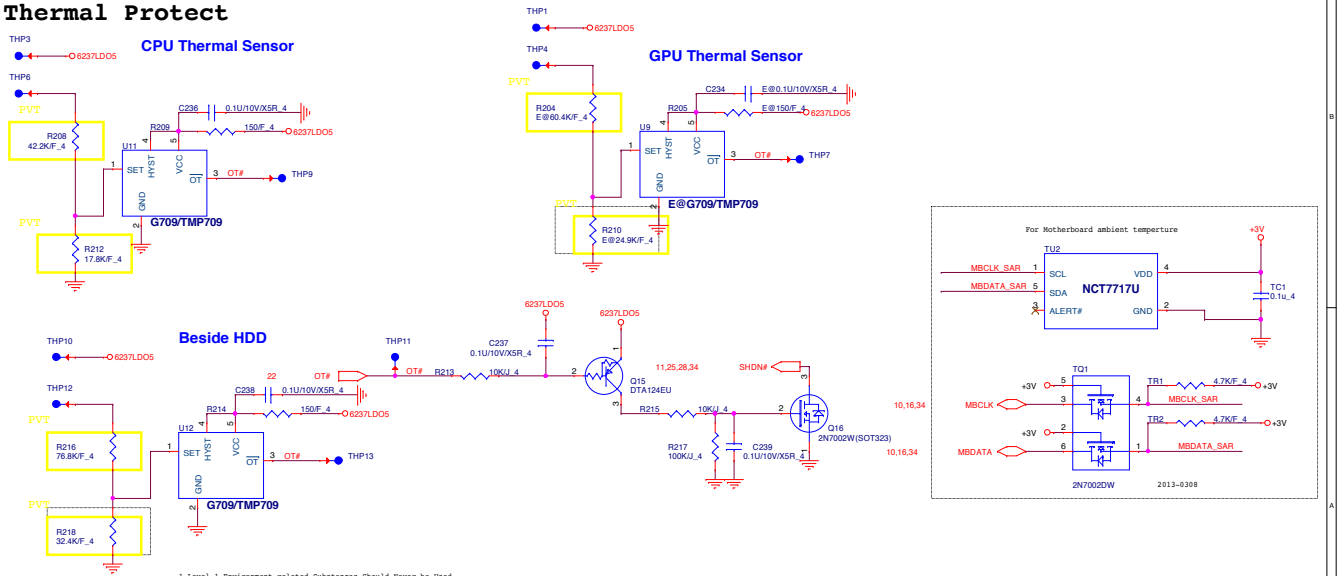
DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	96	R212=17.85K	17.8K		
Near GFX sensor temp	86	R210=24.97K	24.9K		
Near HDD sensor temp	76	R218=32.34K	32.4K		

UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	96	R212=17.85K	17.8K		
Near HDD sensor temp	76	R218=32.34K	32.4K		

H/W Thermal Protect



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	HDMI/Thermal IC	1C

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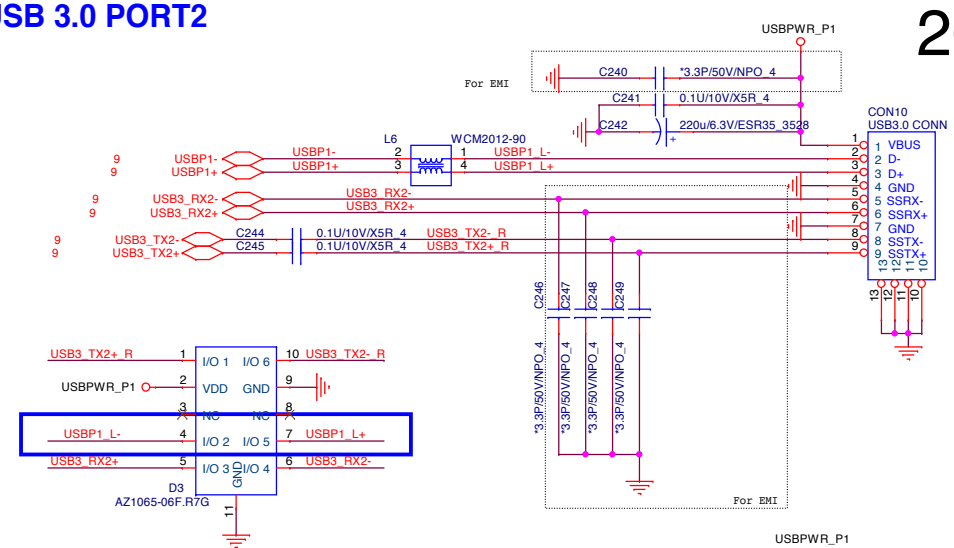
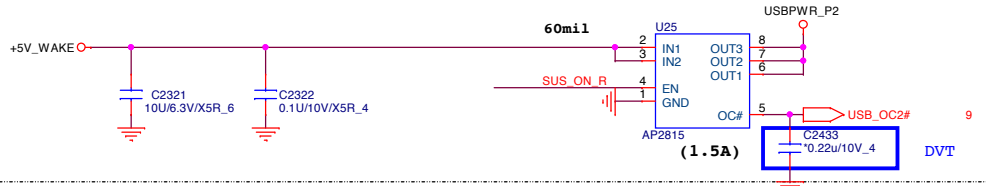
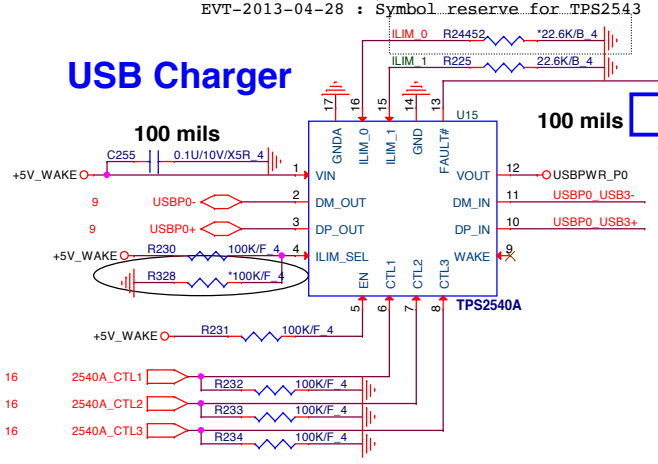
USB 3.0 PORT2



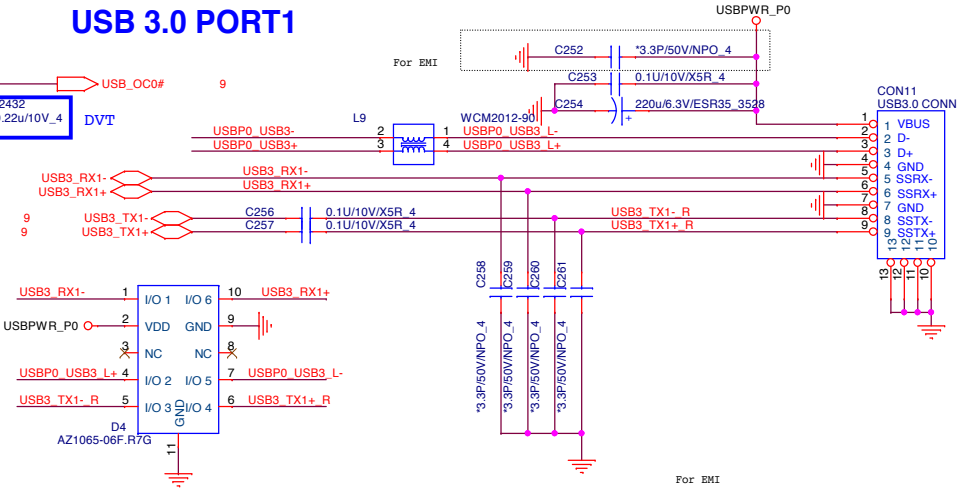


EVT-2013-04-28 : Symbol reserve for TPS2543

USB Charger

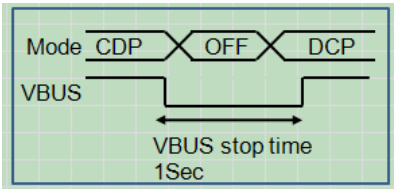


USB 3.0 PORT1



	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL	(I LIMIT(A)= 48000/R)	
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	USB/USB Charger	1C
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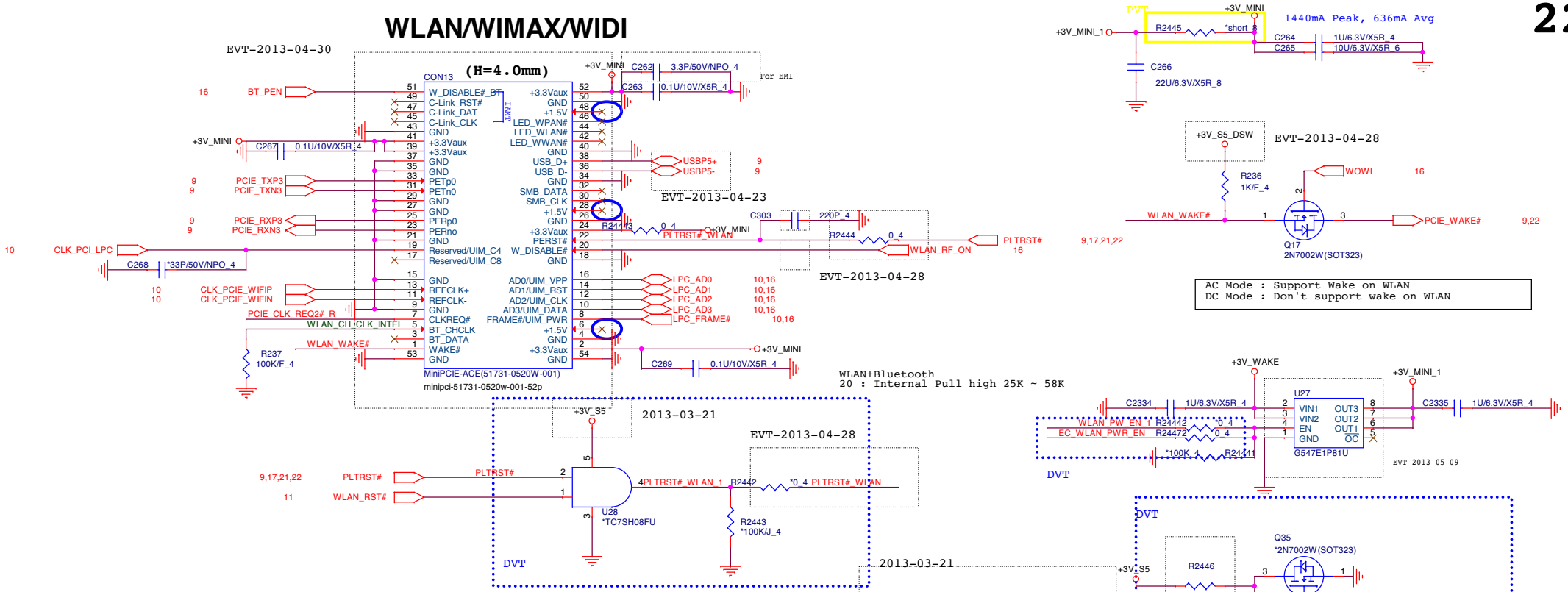
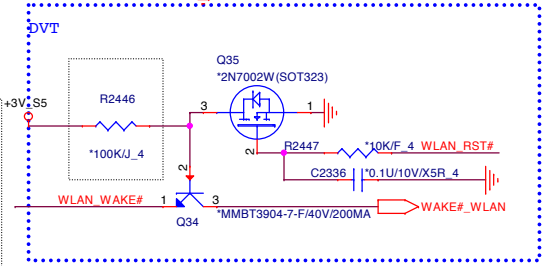
WLAN/WIMAX/WIDI

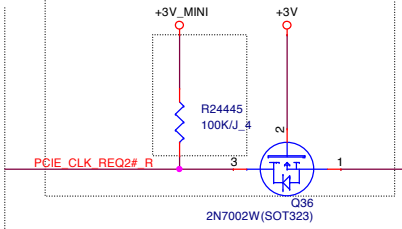


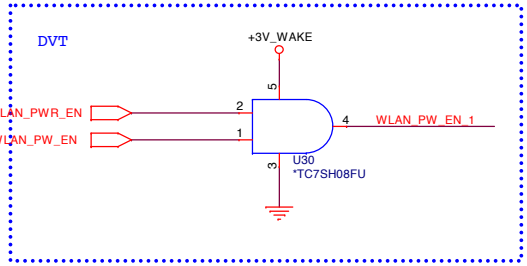
AC Mode : Support Wake on WLAN
DC Mode : Don't support wake on WLAN

WLAN+Bluetooth
20 : Internal Pull high 25K ~ 58K

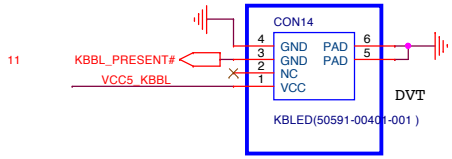


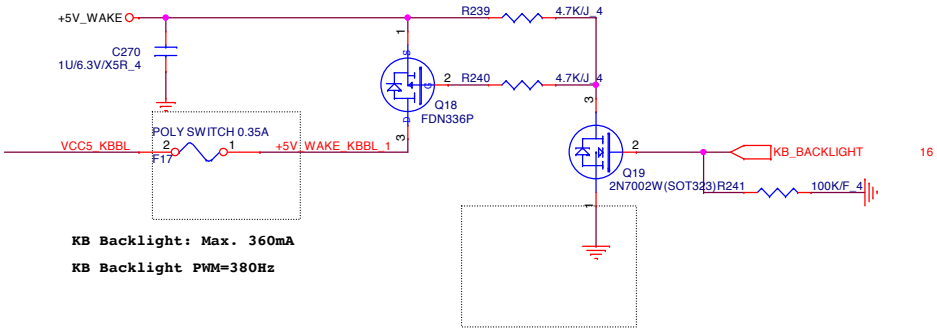
2013-03-21





KB BACKLIGHT





KB Backlight: Max. 360mA

KB Backlight PWM=380Hz

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	WLAN/KB BL	1C
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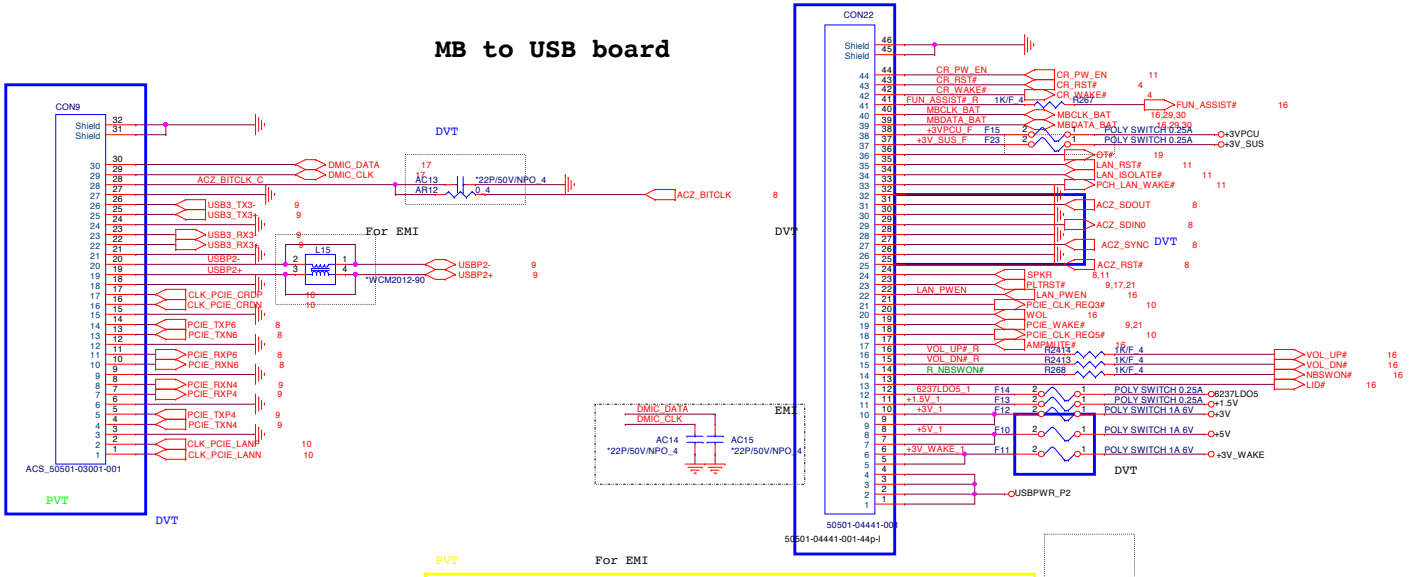
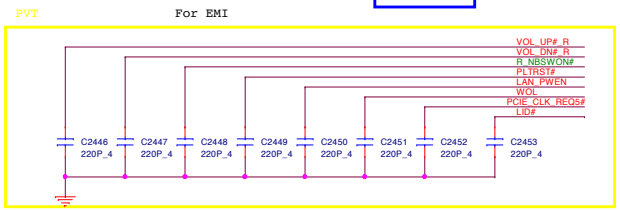
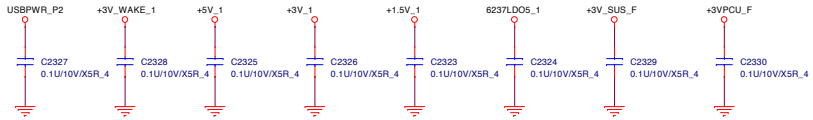
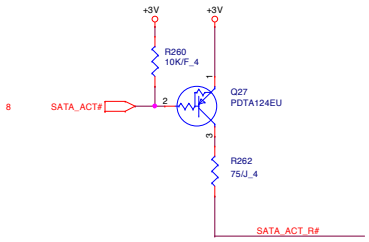
MB to USB board







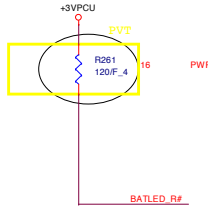
SATA LED



	VF MIN	VF MAX	A
Orange LED	1.7V	2.4V	7.27mA / 4.09 mA

(3.3 - 1.7)V / 220 Ω = 7.27 mA
(3.3 - 2.4)V / 220Ω =4.09 mA

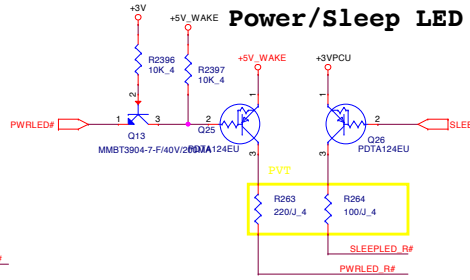
BATTERY LED



	VF MIN	VF MAX	A
Umber LED	1.7V	2.4V	7.27mA / 4.09 mA

(3.3 - 1.7)V / 220 Ω = 7.27 mA
(3.3 - 2.4)V / 220Ω =4.09 mA

Power/Sleep LED

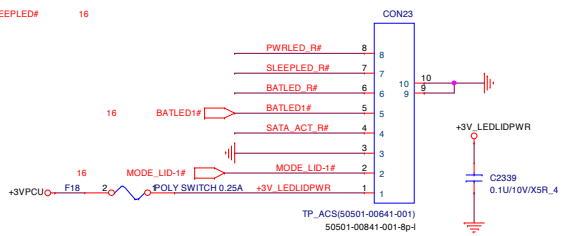


	VF MIN	VF MAX	A
Pure green LED	2.7V	3.7V	4.89mA / 2.76 mA

(5- 2.7)V / 470 Ω = 4.89 mA
(5 - 3.7)V / 470Ω = 2.76 mA

	VF MIN	VF MAX	A
Umber LED	1.7V	2.4V	7.27mA / 4.09mA

(3.3 - 1.7)V / 220 Ω = 7.27 mA
(3.3 - 2.4)V / 220Ω =4.09 mA



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	LED/RF/KB/PS	1C
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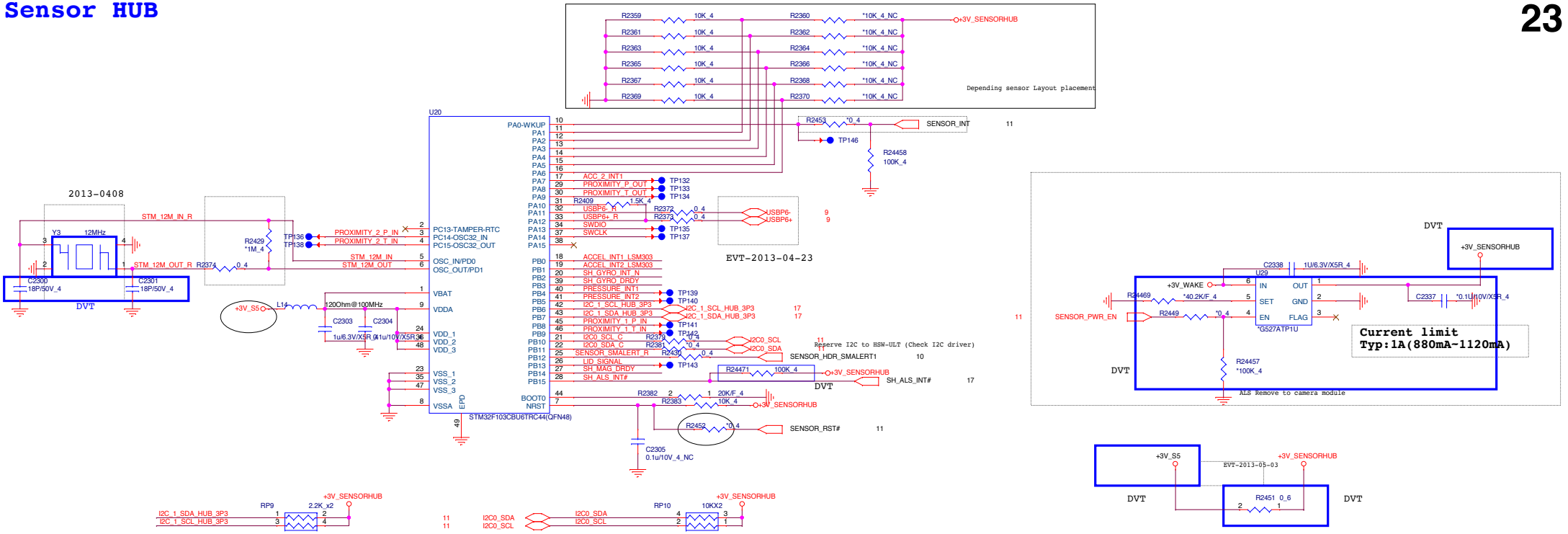
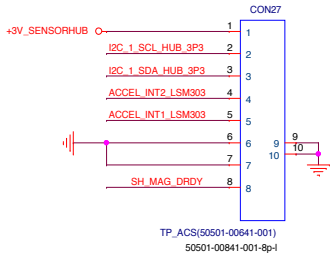
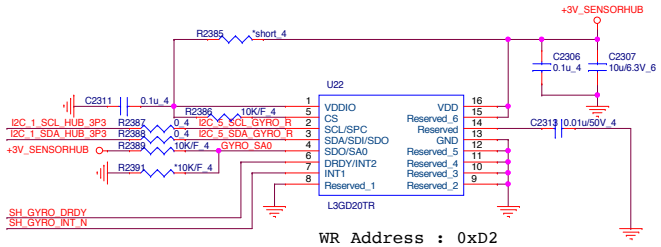
Sensor HUB

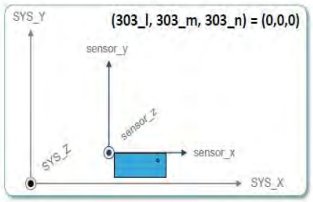


G-sensor/E-compass/Magnetometer

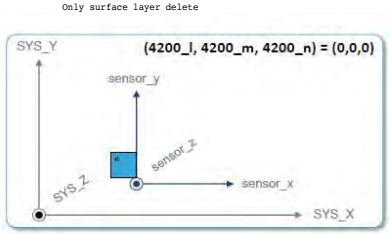


Gyroscope





Only surface layer delete



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Quanta Computer Inc.
PROJECT : FI3
Size | Document Number: Sensors Hub & Sensors | Rev: 1C
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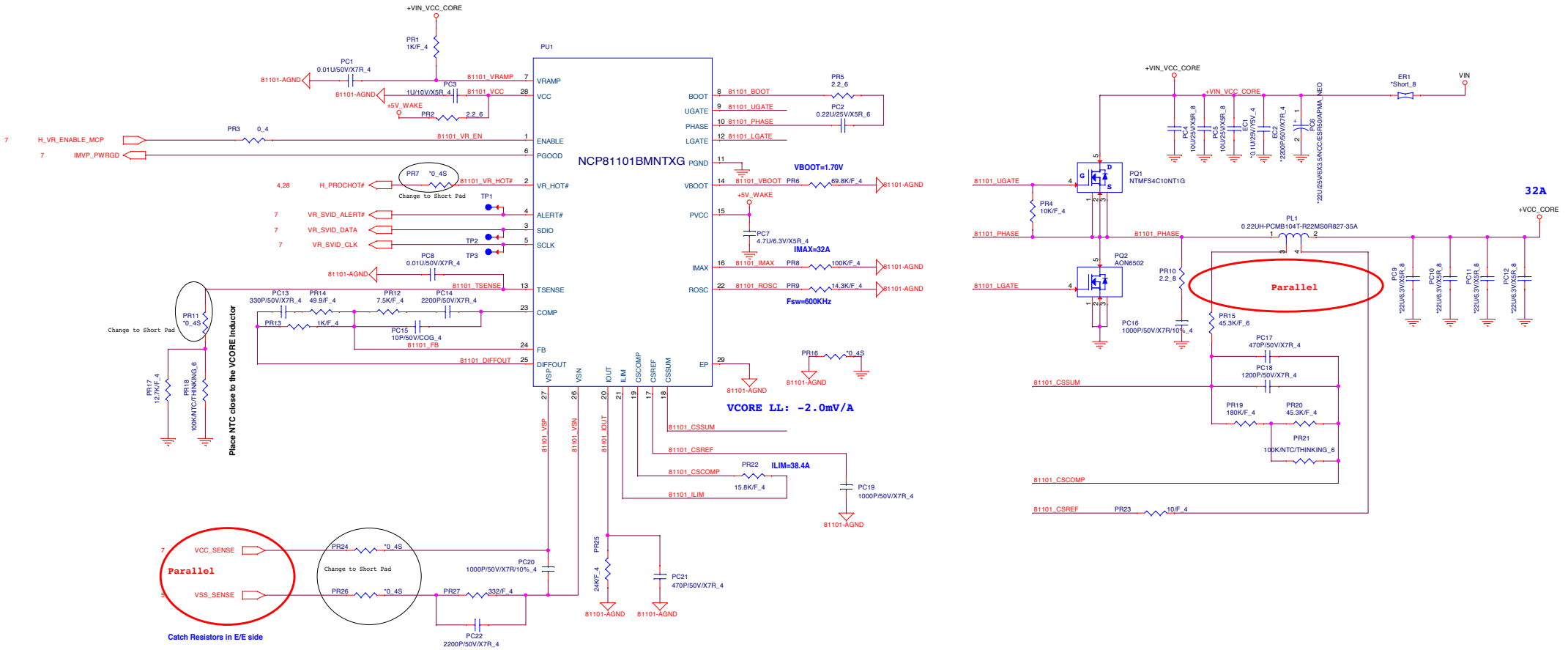

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	+VCC_CORE (NCP81101)	1C

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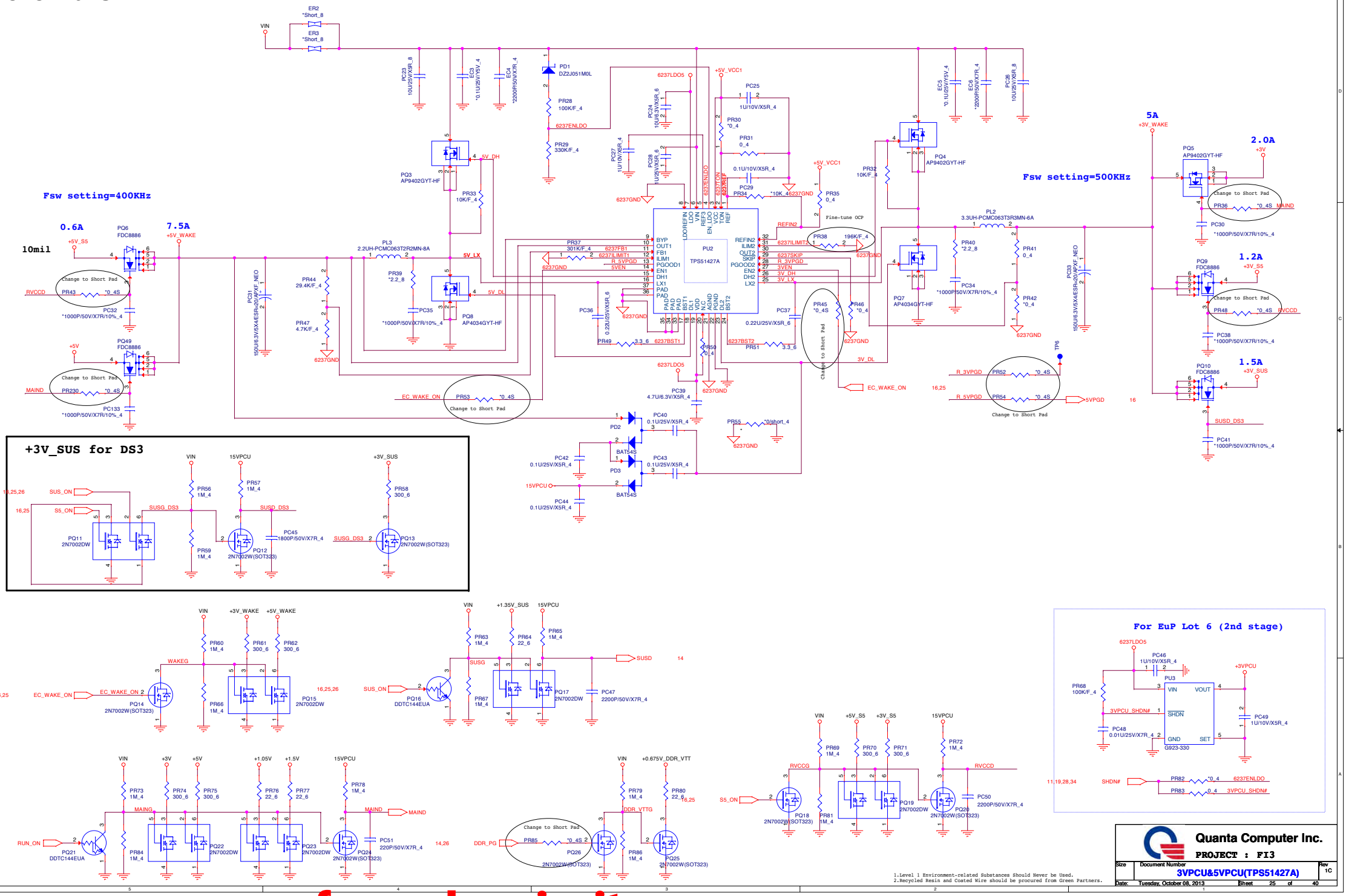
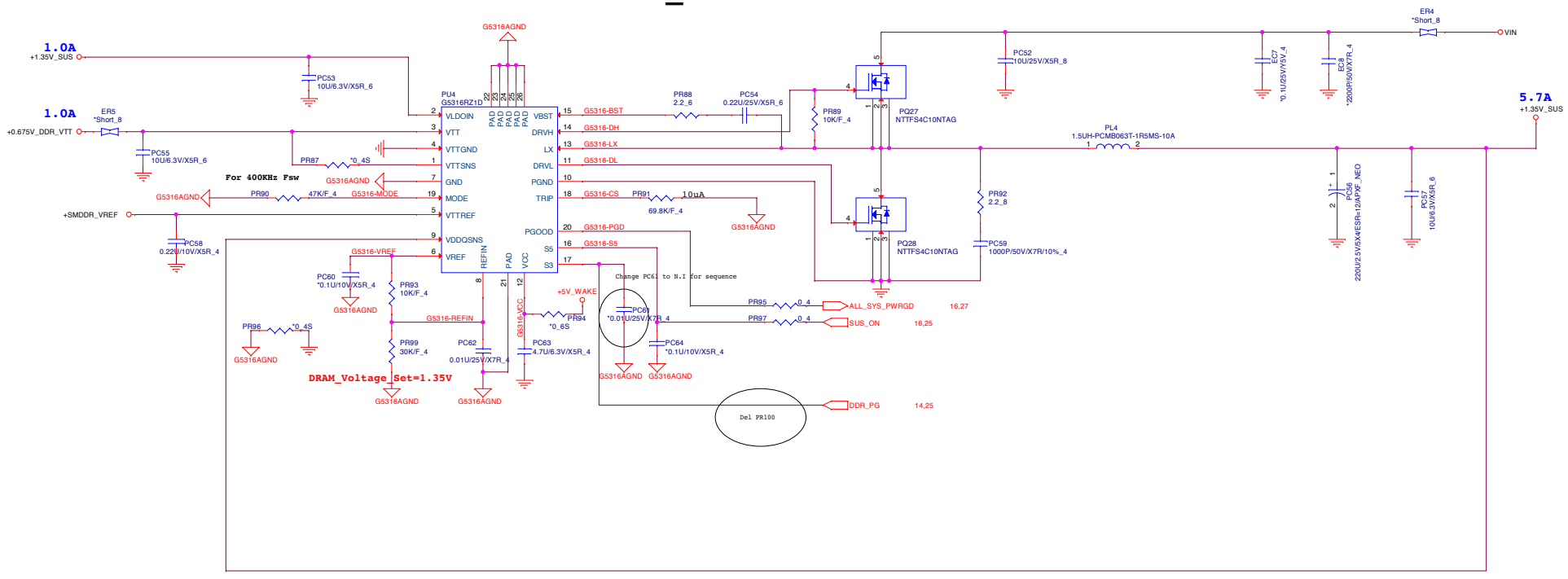


1.35VSUS & VTT_MEM



MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	**Non-tracking discharge**
0	**47Kohm**	**400KHz**	

STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	1.5VSUS/VTT_MEM	1C

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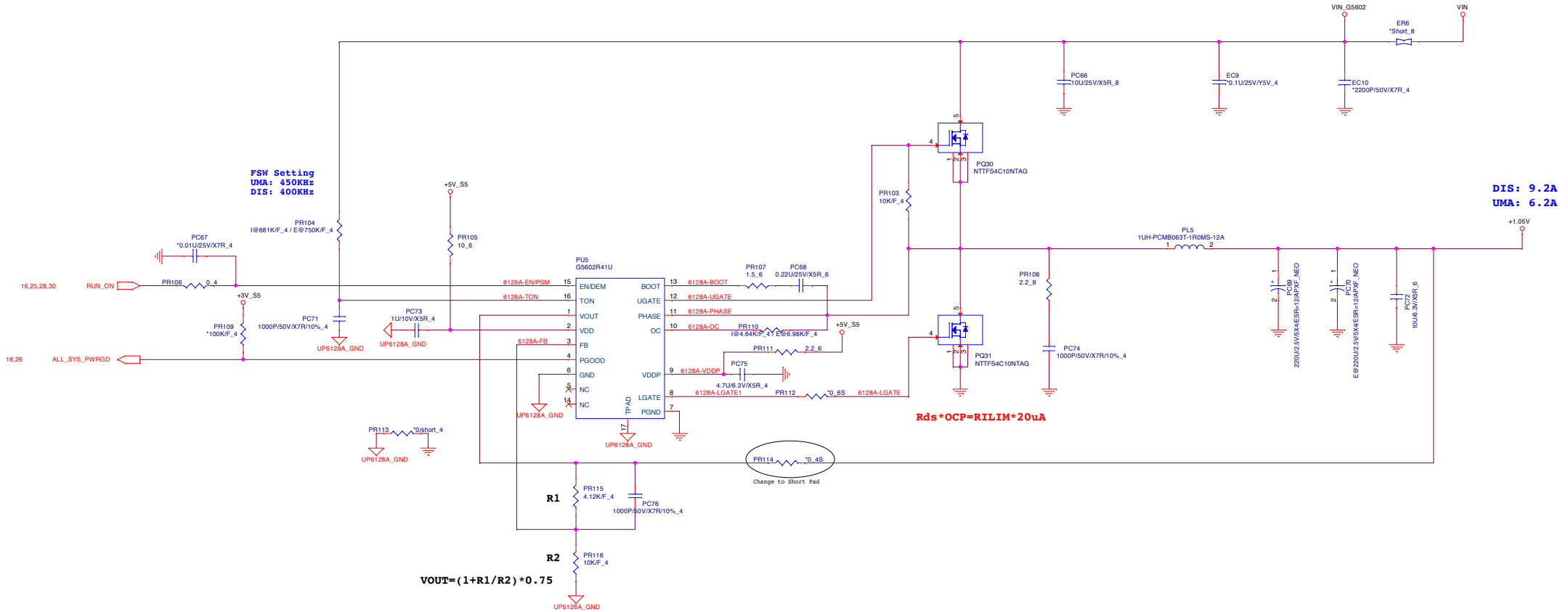

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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	+1.05V	1C
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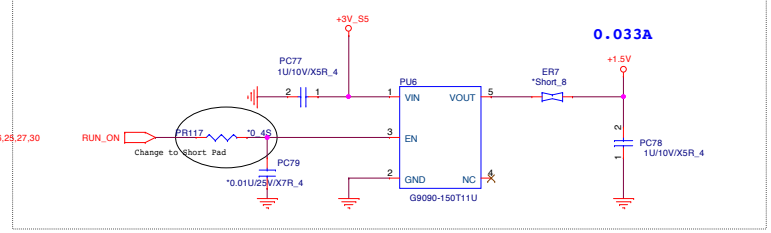
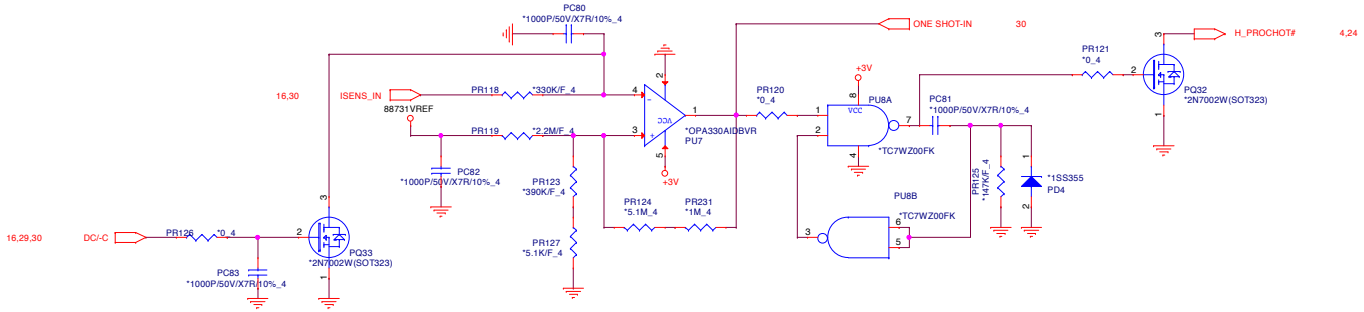
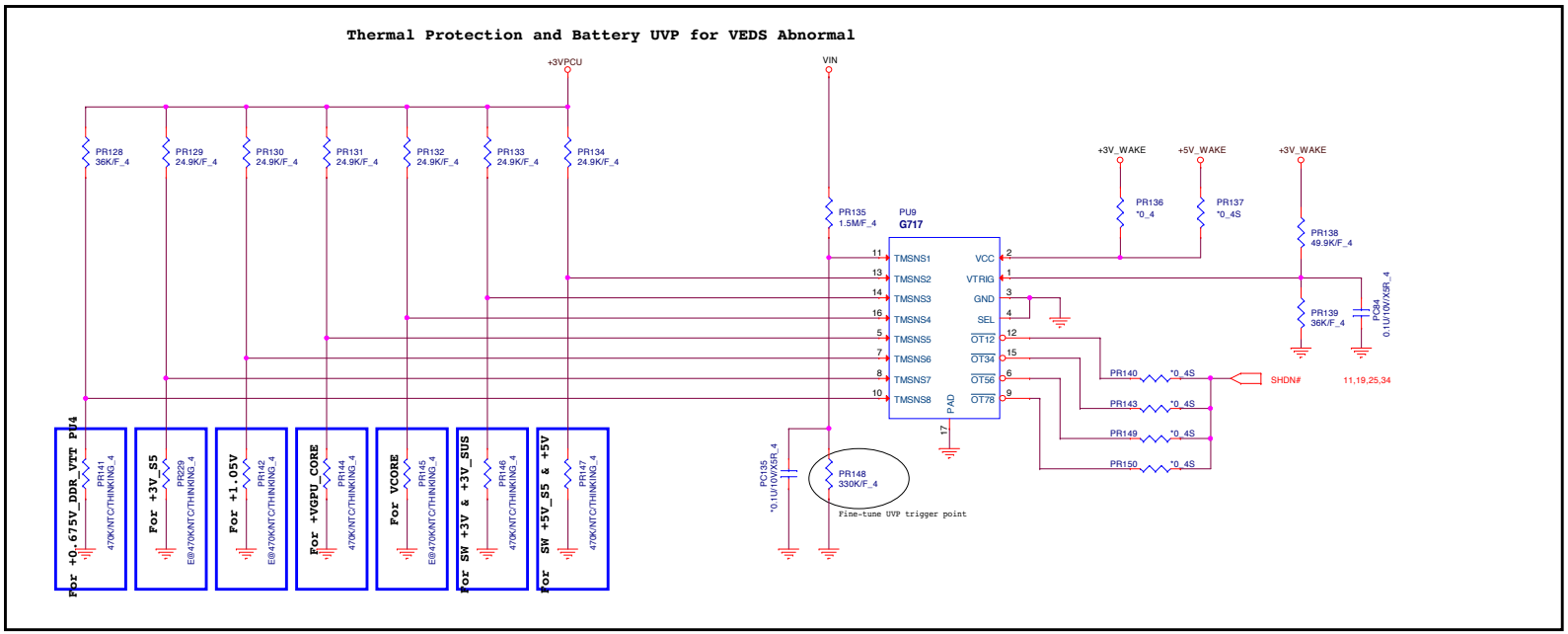
VCC1.5



One-Shot 10ms PROCHOT# For ADP



Thermal Protection and Battery UVP for VEDS Abnormal



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Quanta Computer Inc.
PROJECT : FI3

Size	Document Number	Rev
	VCC1.5/Thermal Protection	1C

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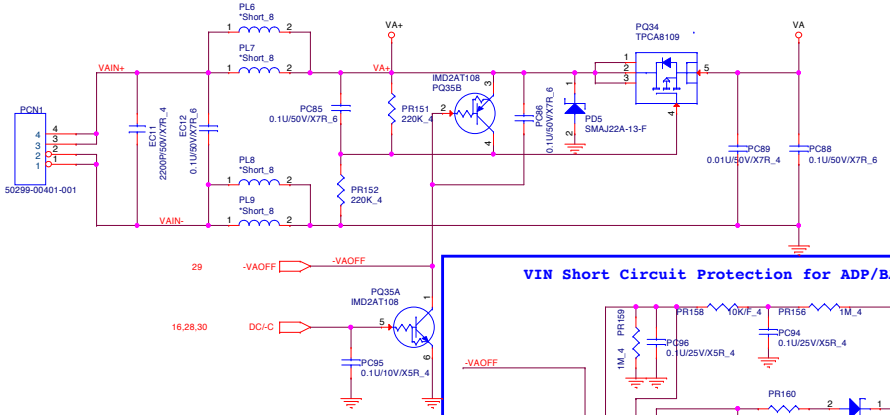
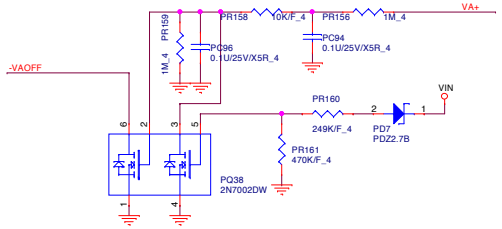
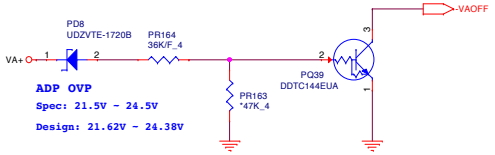


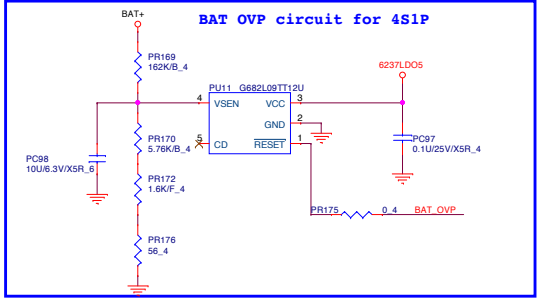
VIN Short Circuit Protection for ADP/BAT



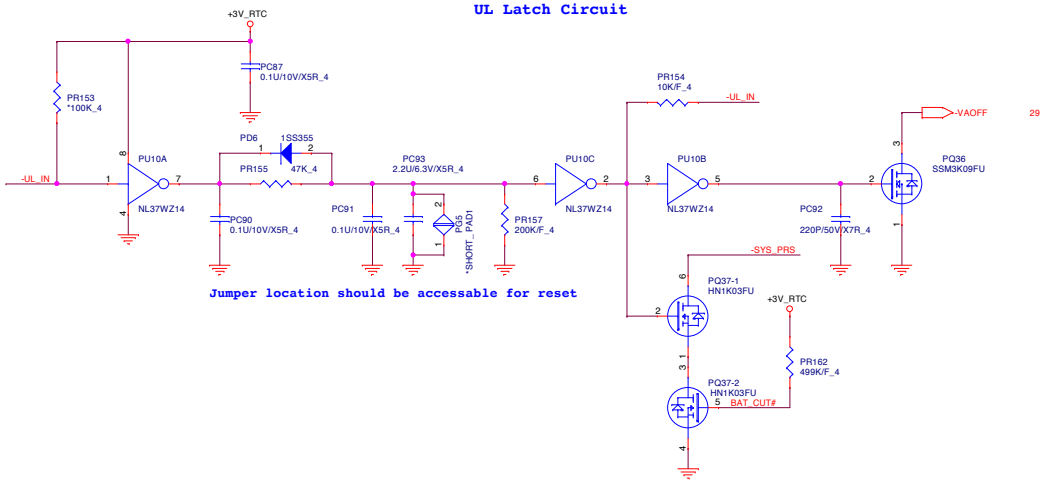
Separate adapter OVP from UL circuit



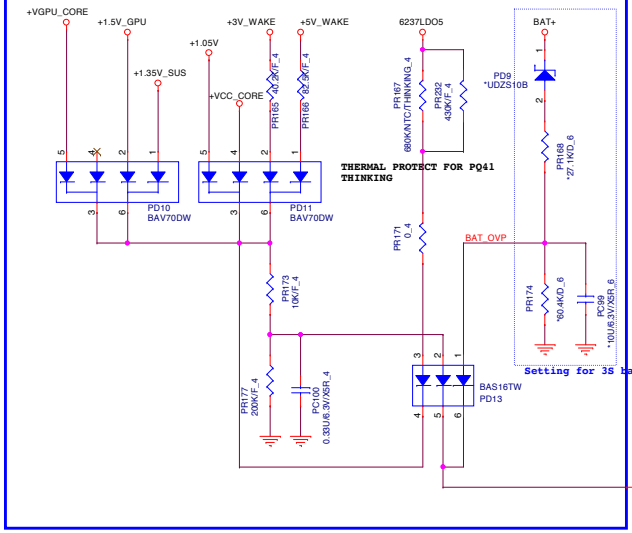
BAT OVP circuit for 4S1P

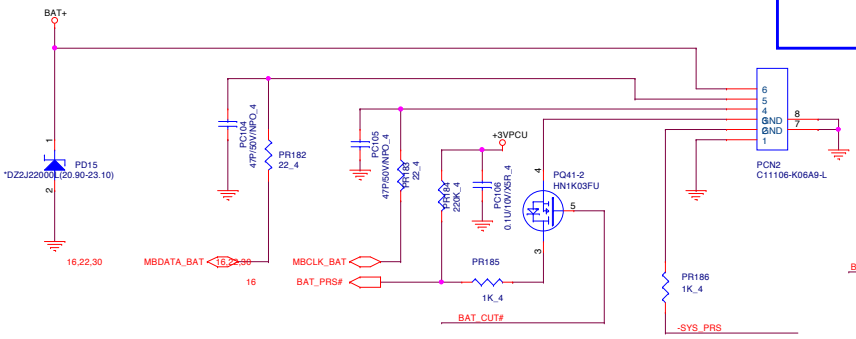


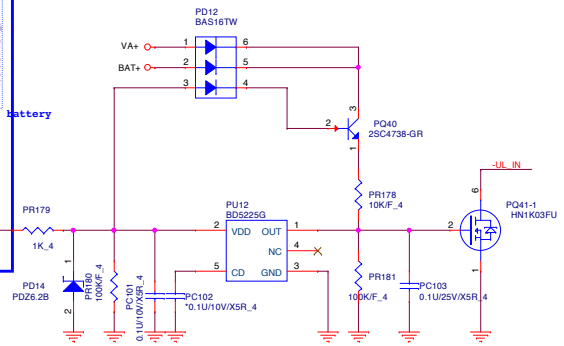
UL Latch Circuit



System OVP for VEDS







1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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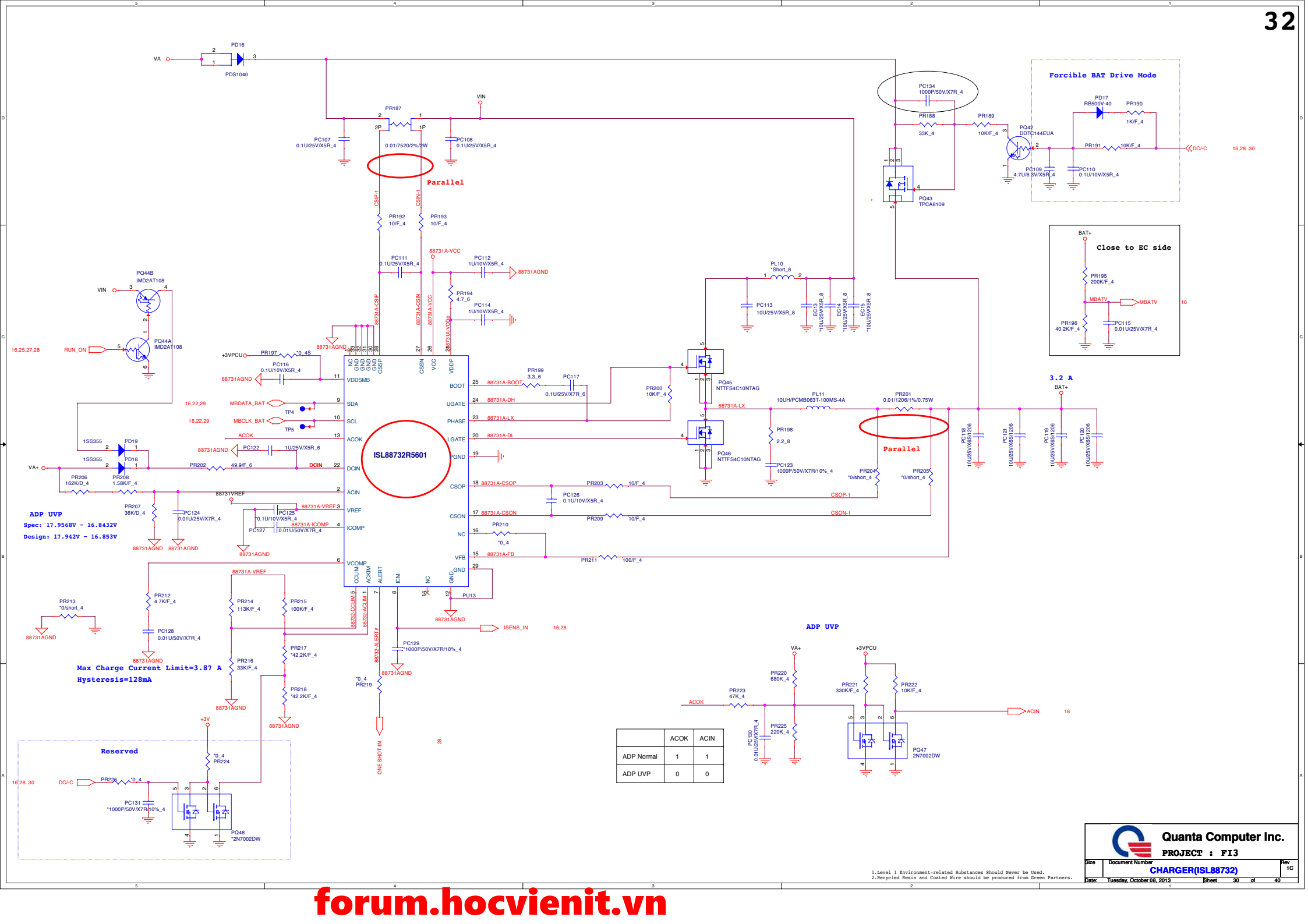

	ACOK	ACIN
ADP Normal	1	1
ADP UVP	0	0

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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	CHARGER(ISL88732)	1C

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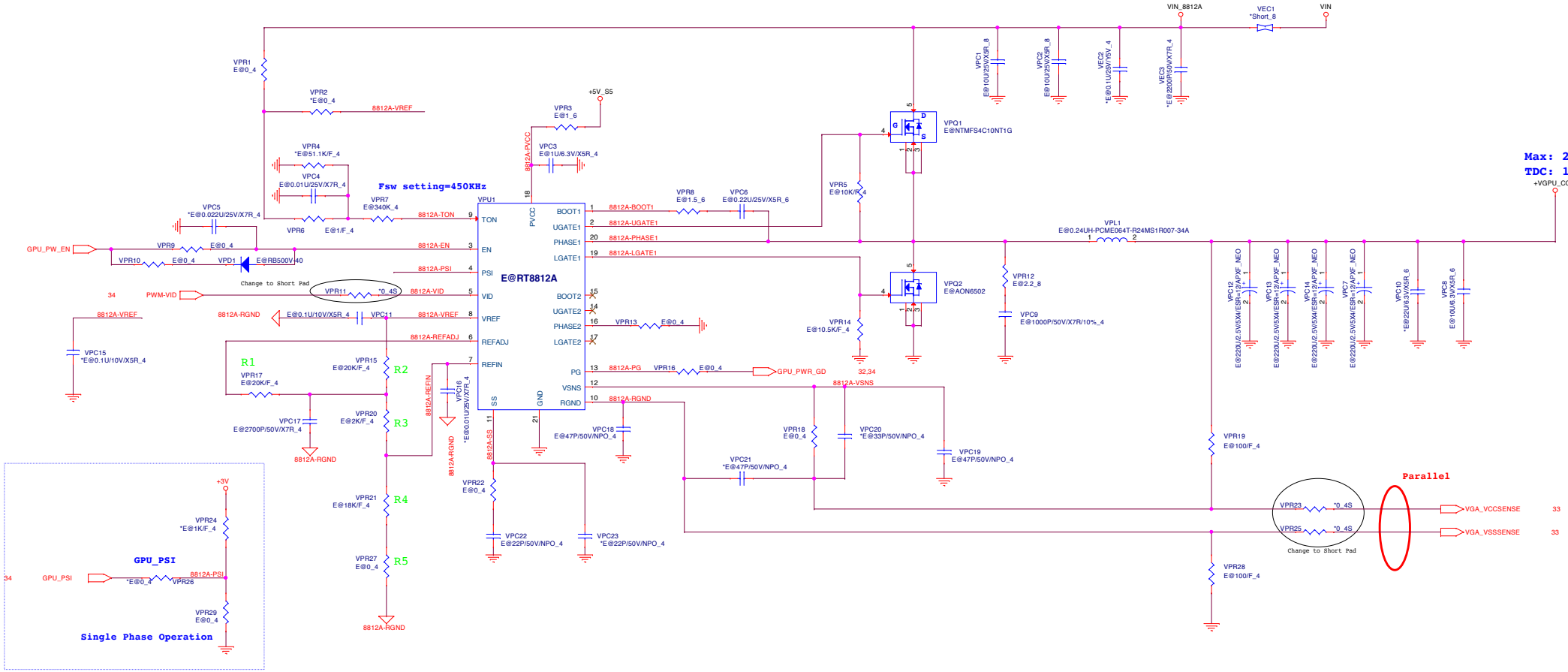
VGA-CORE



1.Level 1 Environment-related Substances Should Never be Used.
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	VGA_CORE (RT8812A)	1C
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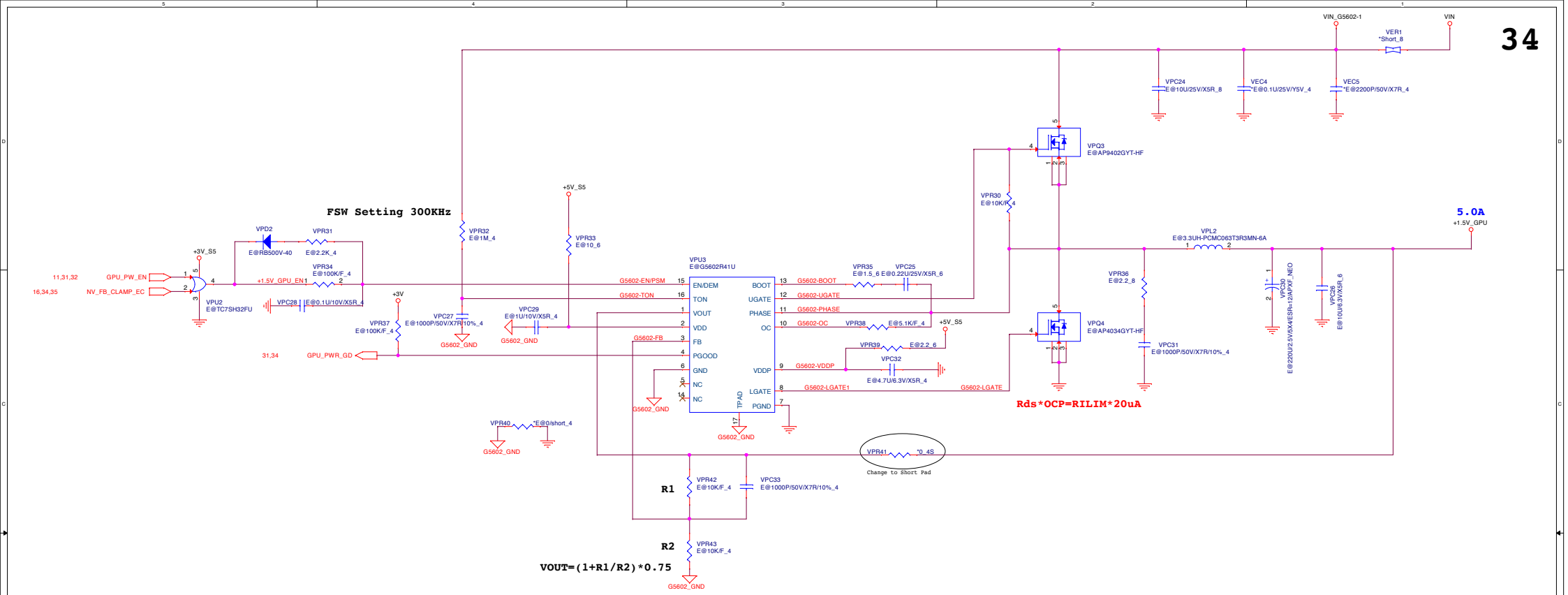

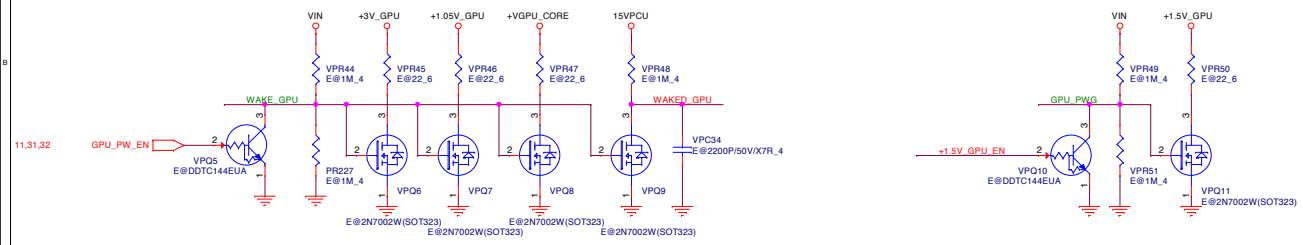

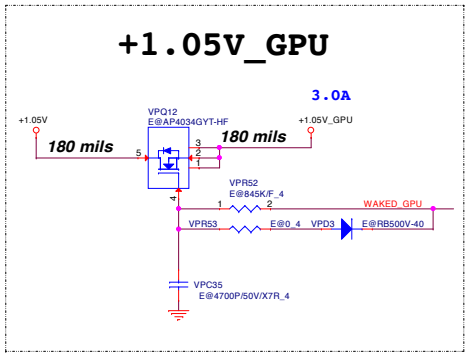

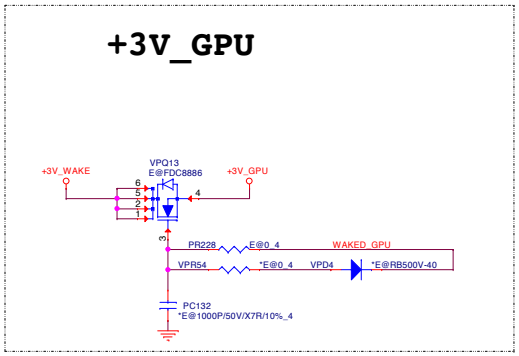

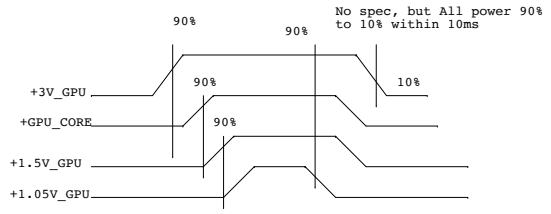

1.Level 1 Environment-related Substances Should Never be Used.
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	1.8_GPU / 1.0_GPU	1C
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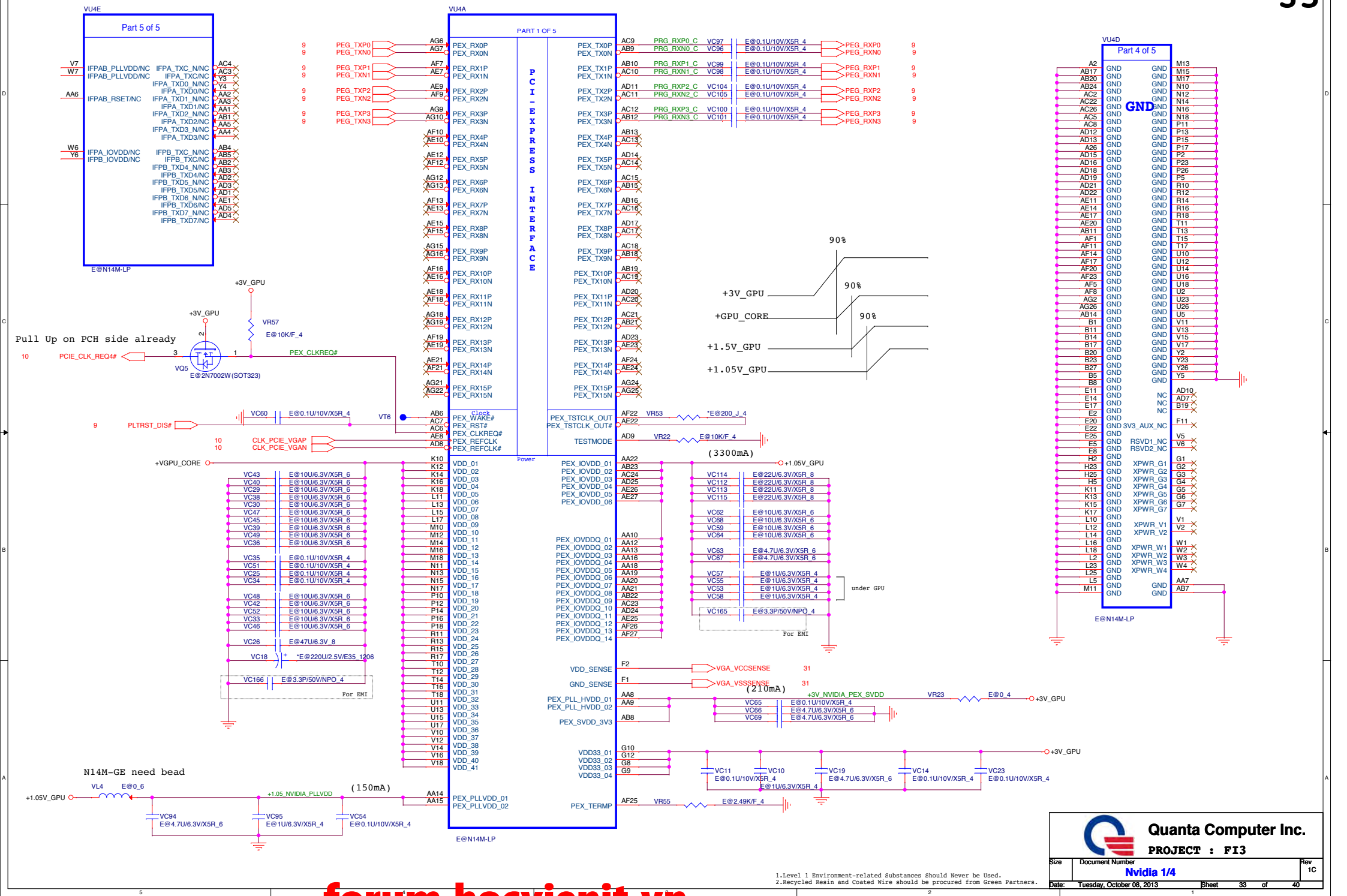

1.Level 1 Environment-related Substances Should Never be Used.
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PROJECT : FI3		
Size	Document Number	Rev
	Nvidia 1/4	1C
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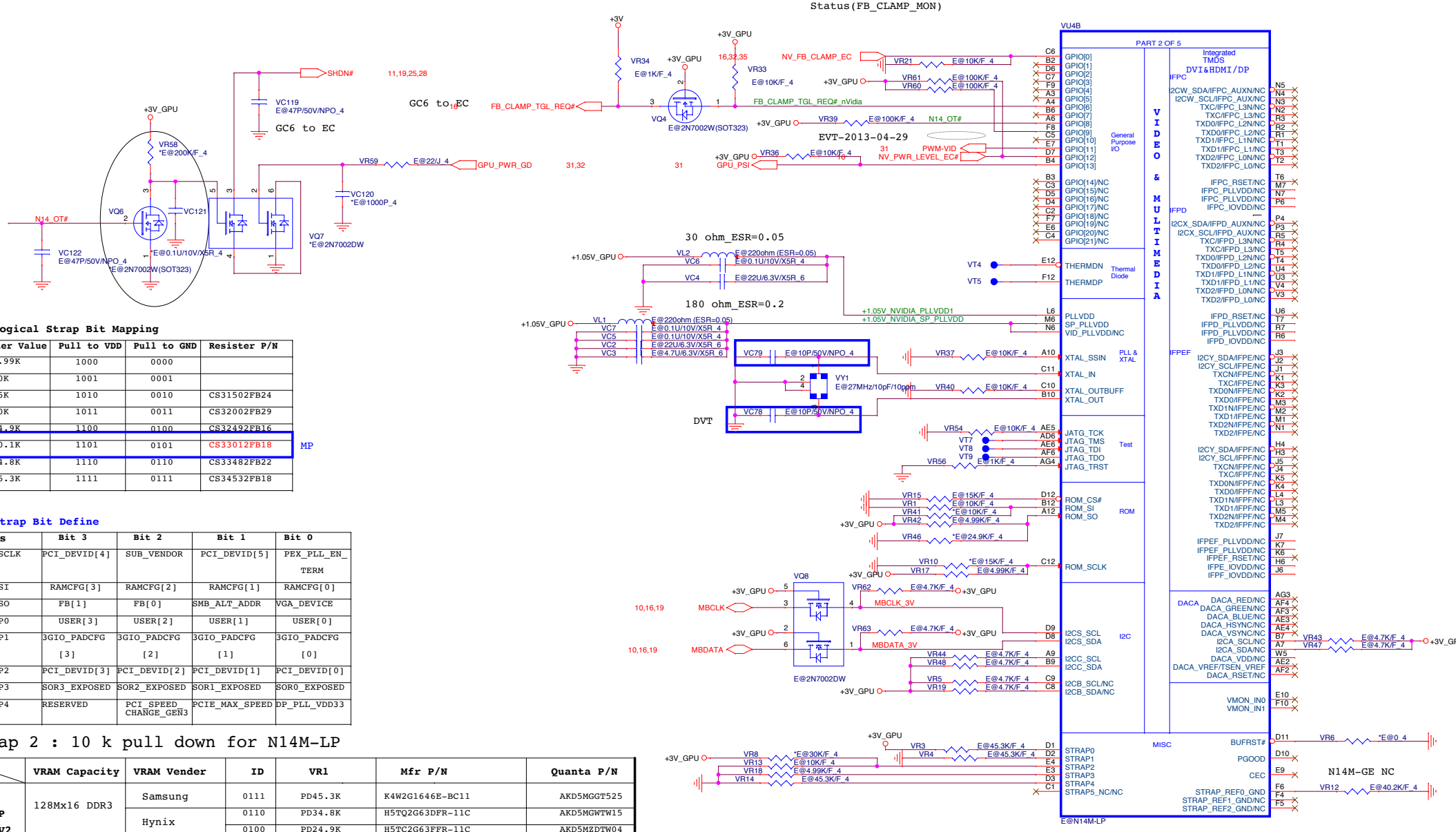

N14 Logical Strap Bit Mapping

Resister Value	Pull to VDD	Pull to GND	Resister P/N	
4.99K	1000	0000		
10K	1001	0001		
15K	1010	0010	CS31502FB24	
20K	1011	0011	CS32002FB29	
24.9K	1100	0100	CS32492FB16	
30.1K	1101	0101	CS33012FB18	MP
34.8K	1110	0110	CS33482FB22	
45.3K	1111	0111	CS34532FB18	

N14 Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33

Strap 2 : 10 k pull down for N14M-LP

	VRAM Capacity	VRAM Vender	ID	VR1	Mfr P/N	Quanta P/N	
N14M-LP N14P-GV2	128Mx16 DDR3	Samsung	0111	PD45.3K	K4W2G1646E-BC11	AKD5MGGT525	
		Hynix	0110	PD34.8K	H5TQ2G63DFR-11C	AKD5MGWTW15	
			0100	PD24.9K	H5TC2G63FFR-11C	AKD5MZDTW04	
		Mircon	0101	PD30.1K	MT41K128M16JT-107G:K	AKD5DGSTL06	MP
	256Mx16 DDR3	Samsung	0011	PD20K	K4W4G1646B-HC11	AKD5MGWT525	
		Hynix	0010	PD15K	H5TC4G63AFR-11C	AKD5PGWTW10	
		Mircon	1101	VR41 Mount VR1 NC PU30.1K	MT41K256M16HA-107G:E	AKD5PGSTL07	MP

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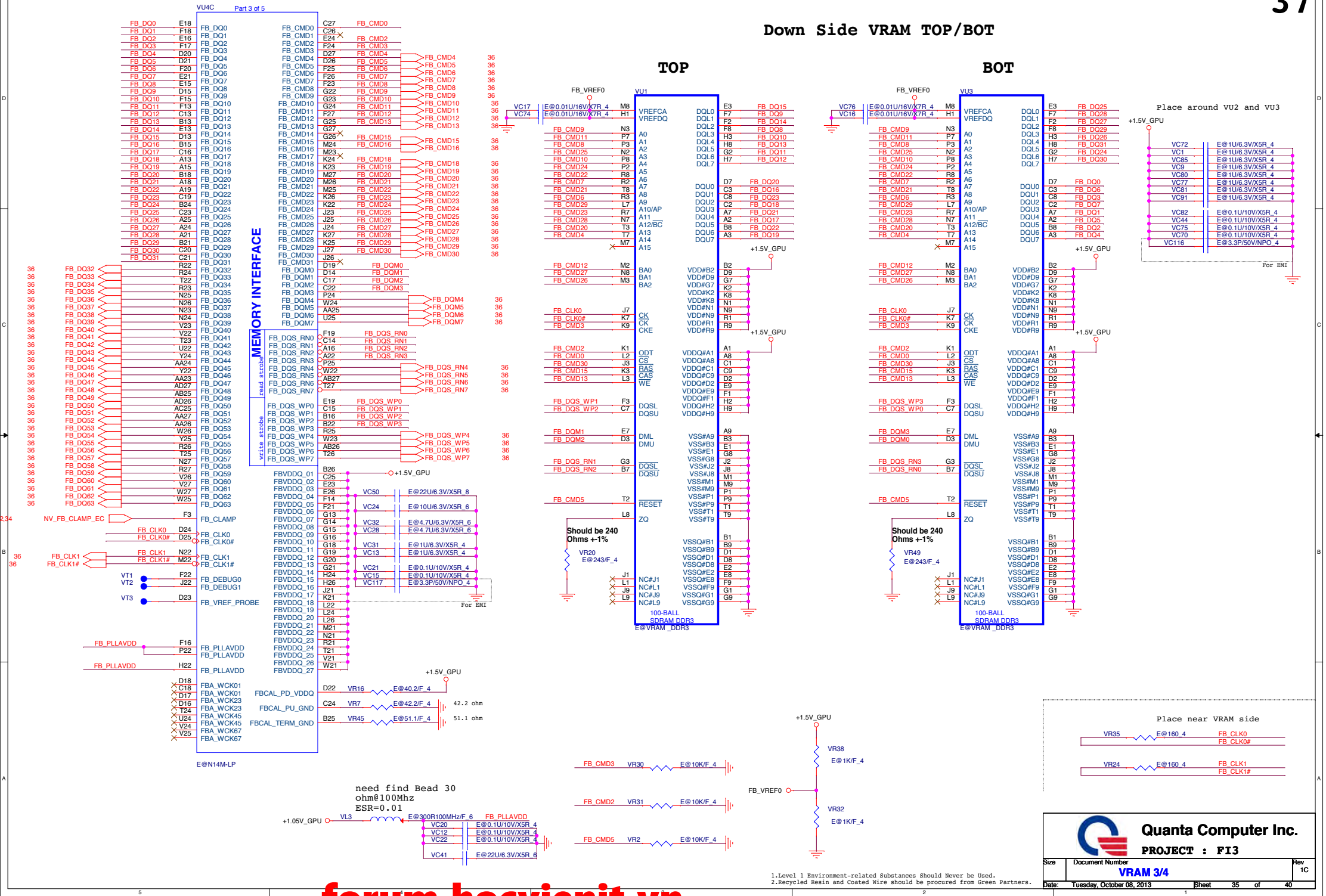
Down Side VRAM TOP/BOT



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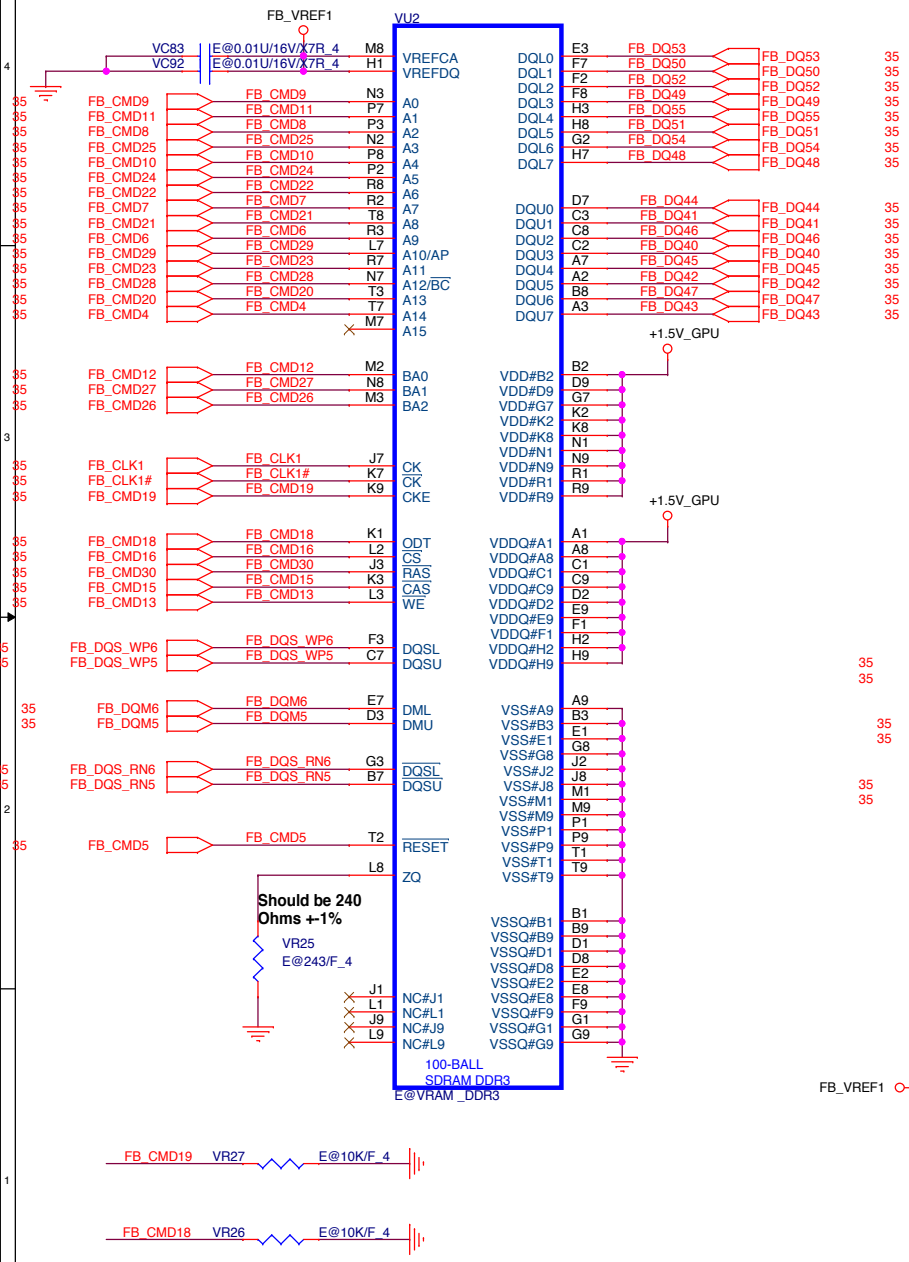
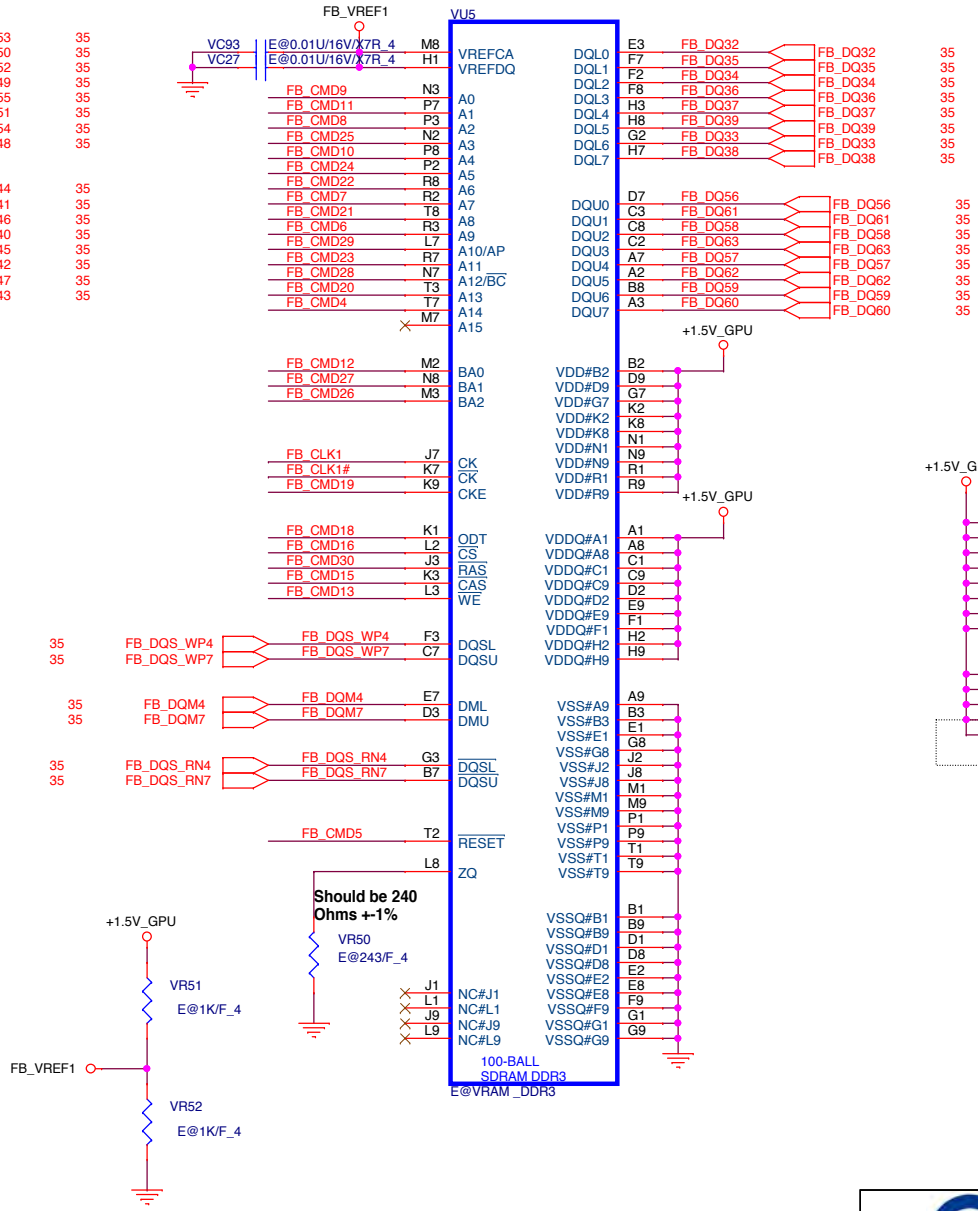
Up Side VRAM TOP/BOT

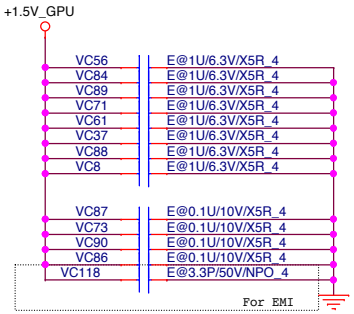
TOP



BOT



Place around VU4 and VU5



1.Level 1 Environment-related Substances Should Never be Used.
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USB PORT Architecture	
PORT 0	EXT. USB3.0
PORT 1	EXT. USB3.0
PORT 2	EXT. USB3.0
PORT 3	Rear Camera
PORT 4	Touch Screen
PORT 5	WiMax/BT
PORT 6	Sensor Hub
PORT 7	Camera

PCIE BUS	
PORT 1	N/A
PORT 2	N/A
PORT 3	WLAN Port
PORT 4	GLAN(RTL8111G)
PORT 5	dGPU
PORT 6	CARD READER

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A

USB3.0 PORT Architecture	
PORT 1	EXT. USB3.0
PORT 2	EXT. USN3.0
PORT 3	EXT. USN3.0
PORT 4	Rear Camera

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88732	0001 001X	0001 0010	0001 0011	Charger
N14M-LP	1001 1110	-	1001 1110	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
T.B.D	0011 0010			Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

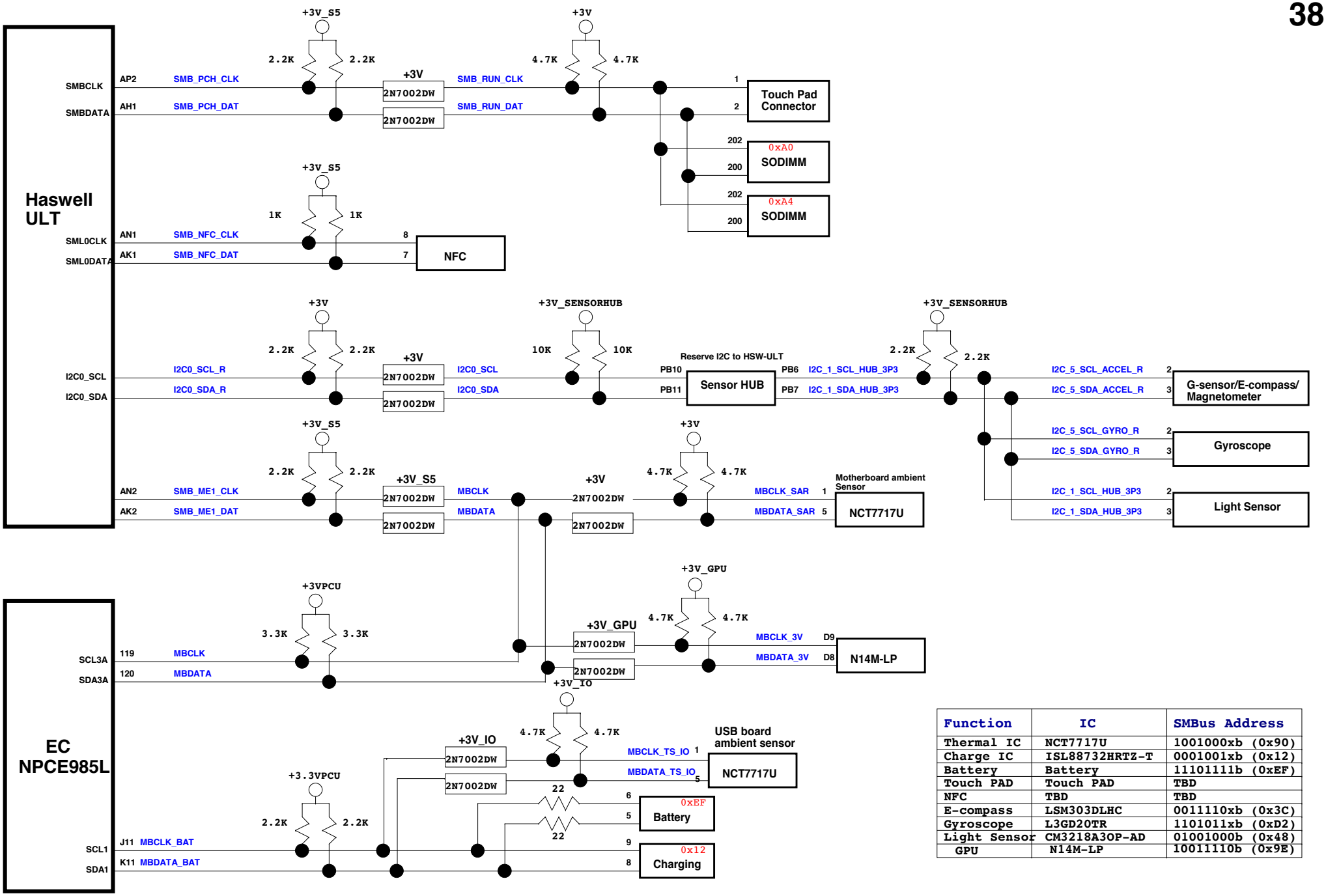
R127(Low) R128(High) — R125(Low) R126(High)

	Board ID1	Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.5V_GPU	H	L	L	L	L	L	L	L
+3V_GPU	H	L	L	L	L	L	L	L
+1.05V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L

	VRAM Capacity	VRAM Vender	ID	VR1	Mfr P/N	Quanta P/N
N14M-LP N14P-GV2	128Mx16 DDR3	Samsung	0111	PD45.3K	K4W2G1646E-BC11	AKD5MGGT525
		Hynix	0110	PD34.8K	H5TQ2G63DFR-11C	AKD5MGWTW15
			0100	PD24.9K	H5TC2G63FFR-11C	AKD5MZDTW04
	256Mx16 DDR3	Samsung	0011	PD20K	K4W4G1646B-HC11	AKD5MGWT525
		Hynix	0010(TBD)	PD15K	H5TC4G63AFR-11C	AKD5PGWTW10



Function	IC	SMBus Address
Thermal IC	NCT7717U	1001000xb (0x90)
Charge IC	ISL88732HRTZ-T	0001001xb (0x12)
Battery	Battery	11101111b (0xEF)
Touch PAD	Touch PAD	TBD
NFC	TBD	TBD
E-compass	LSM303DLHC	0011110xb (0x3C)
Gyroscope	L3GD20TR	1101011xb (0xD2)
Light Sensor	CM3218A3OP-AD	01001000b (0x48)
GPU	N14M-LP	10011110b (0x9E)

1.Level 1 Environment-related Substances Should Never be Used.
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OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.5V_GPU	H	L	L	L	L	L	L	L
+3V_GPU	H	L	L	L	L	L	L	L
+1.05V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L

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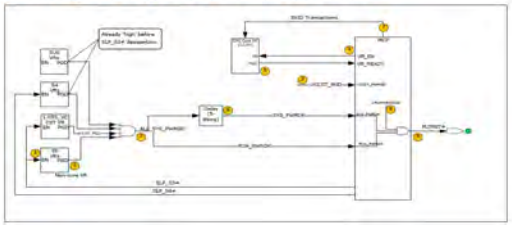
Figure 2-4. Flow Diagram for SYS_PWROK Generation – ULT Platform



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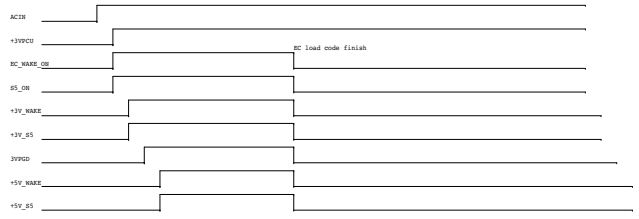

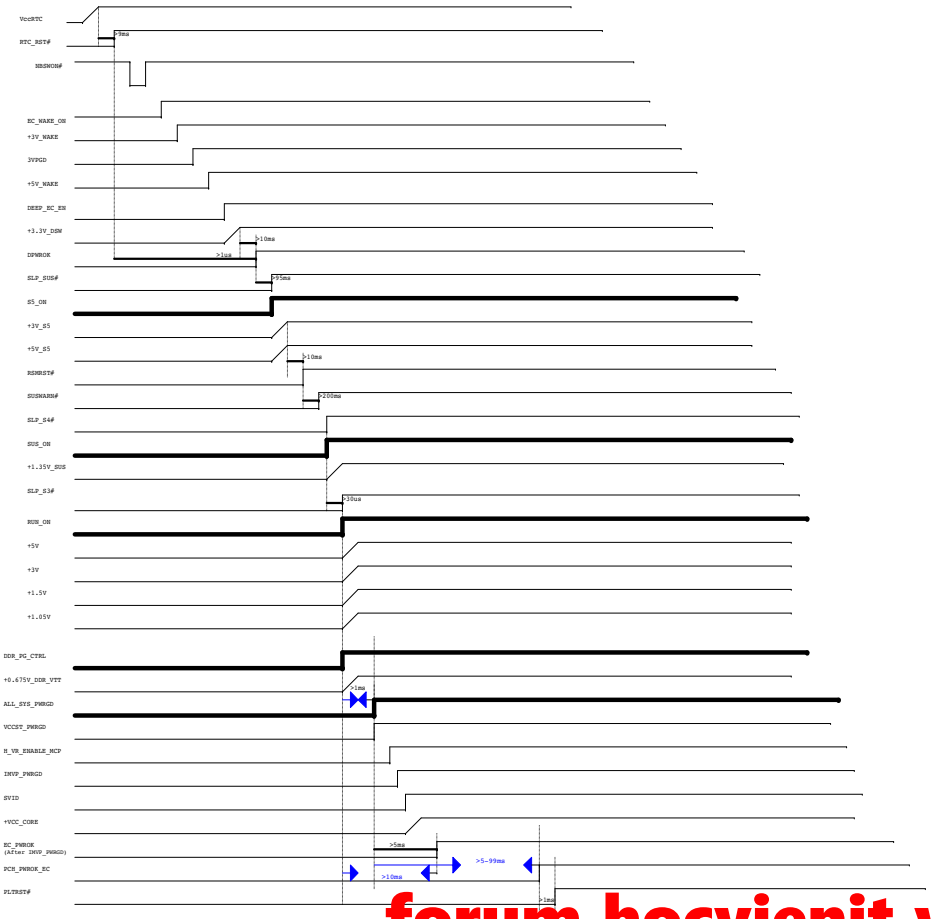

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