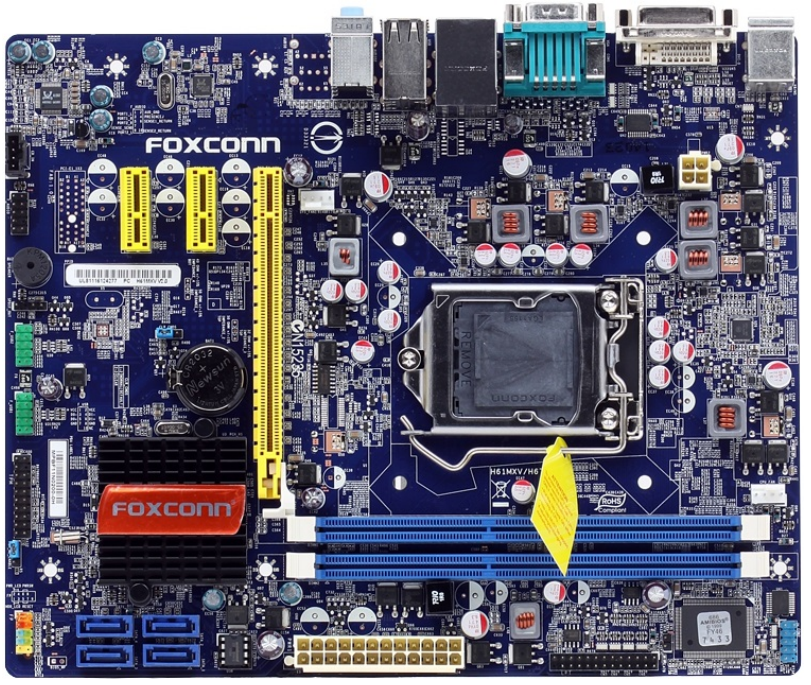

FOXCONN
FOXCONN
REMOVE


FOXCONN

H61MX

Fab A

Micro ATX 9.6X8.0

CPU:

Intel Sandy Bridge processors in LGA1155 Package

System Chipset:

PCH

Main Memory:

Dual Channel / DDR-III * 2 (Max 8GB)

On Board Device:

PCI Bridge :IT8893E/BX

SIO:IT8728F/CX

LAN:RealTek RTL8111E-VB-GR

HDA Codec:ALC888/ALC662

BIOS:SPI Flash ROM 4M

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1
PCI SLOT * 2

Version	Function	SKU	BOM
Fab.A			

FOXCONN

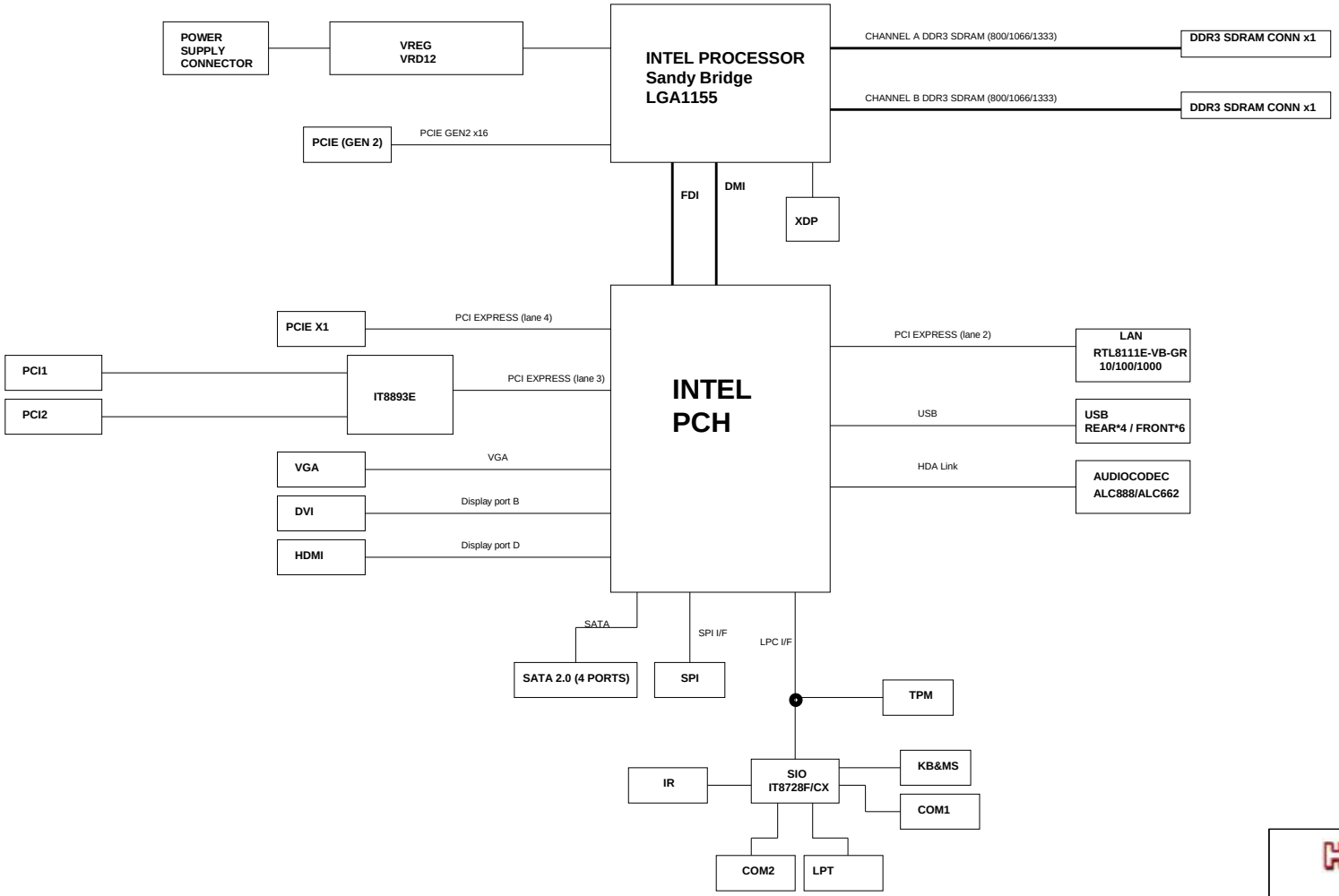
FOXCONN PCEG

Title: Cover Sheet

Size: C | Document Number: H61MX | Rev: A

Date: Tuesday, May 03, 2011 | Sheet 1 of 46

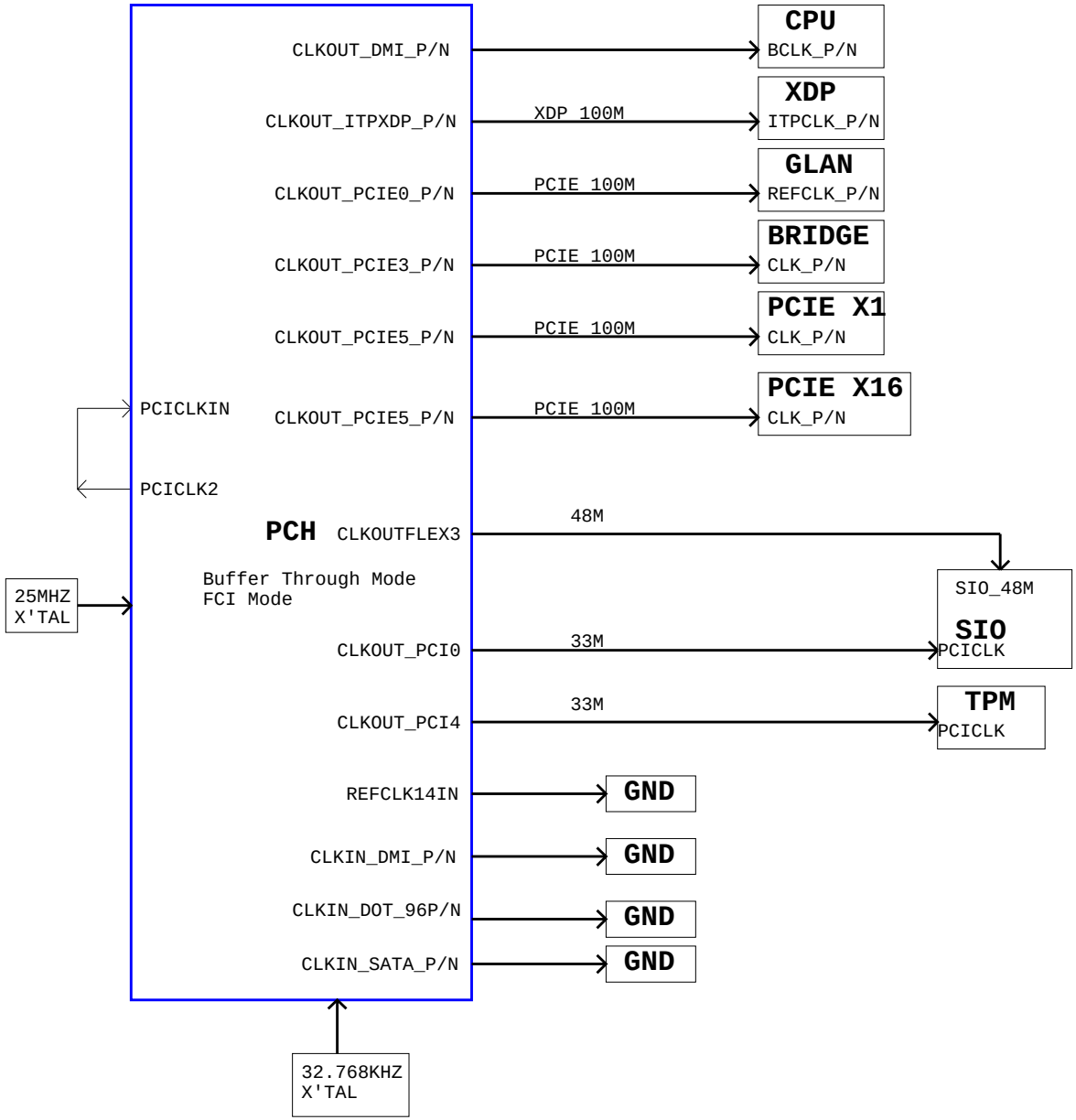
BLOCK DIAGRAM



FOXCONN PCEG

Title: Block Diagram		
Size: C	Document Number: H61MX	Rev: A
Date: Tuesday, May 03, 2011	Sheet 2 of 46	

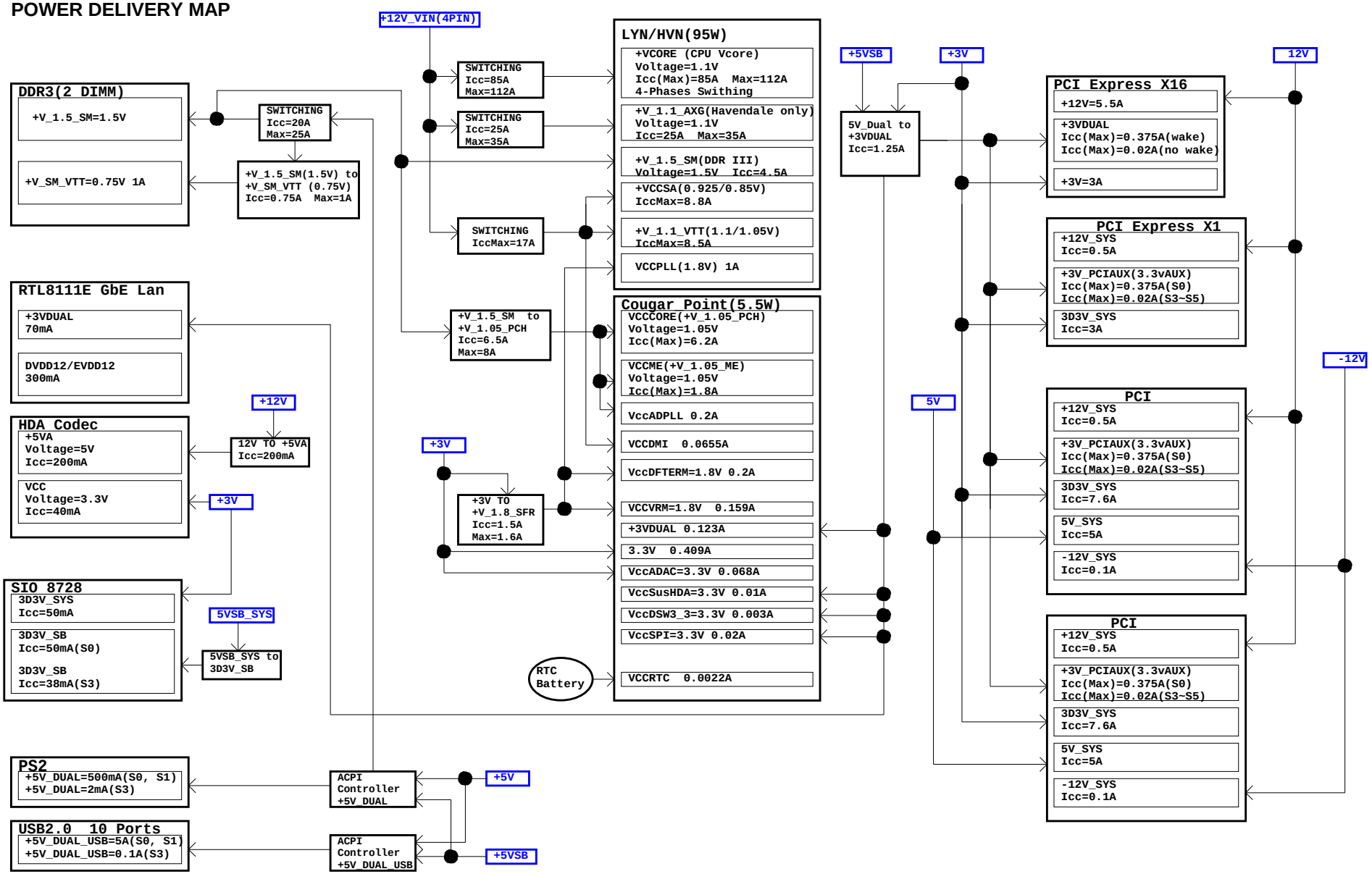
CLOCK DISTRIBUTION



FOXCONN PCEG

Title: Clock Distribution		
Size: C	Document Number: H61MX	Rev: A
Date: Tuesday, May 03, 2011	Sheet 3 of 46	

POWER DELIVERY MAP



FOXCONN PCEG

Title: Power Delivery Map

Size: C | Document Number: H61MX | Rev: A

Date: Tuesday, May 03, 2011 | Sheet 4 of 46

POWER ON SEQUENCE

G3 w/RTC Loss to S4/S5 (Without Deep S4/S5 Support) Timing Diagram

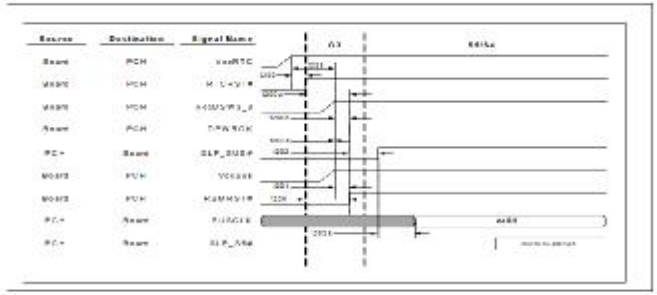


Figure 8-4. S3/M3 to S0 Timing Diagram

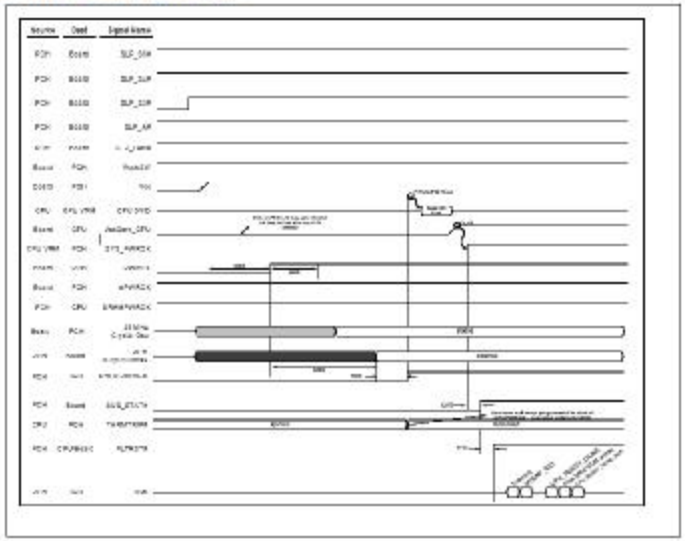


Figure 8-8. DRAMPWROK Timing Diagram

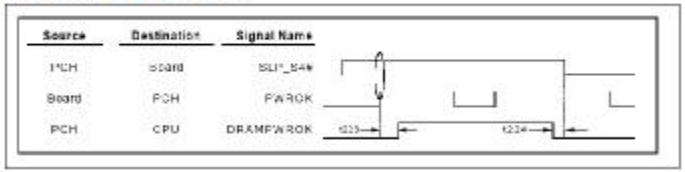


Figure 8-3. S5 to S0 Timing Diagram

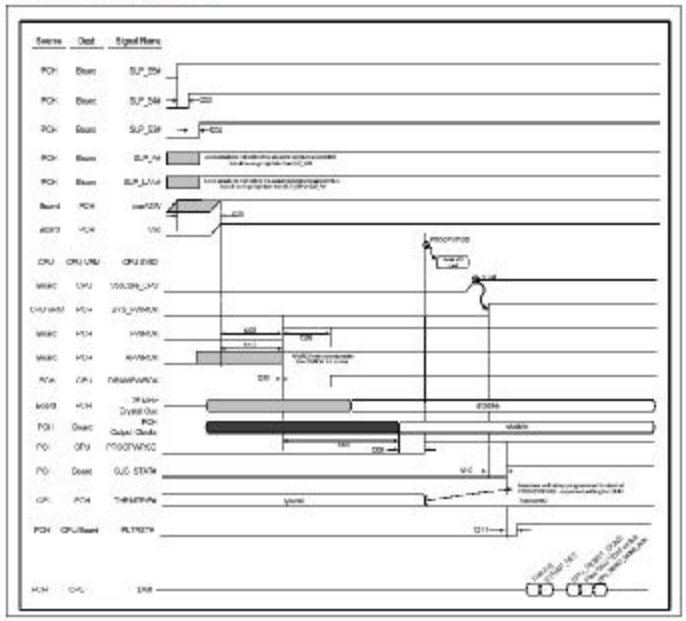
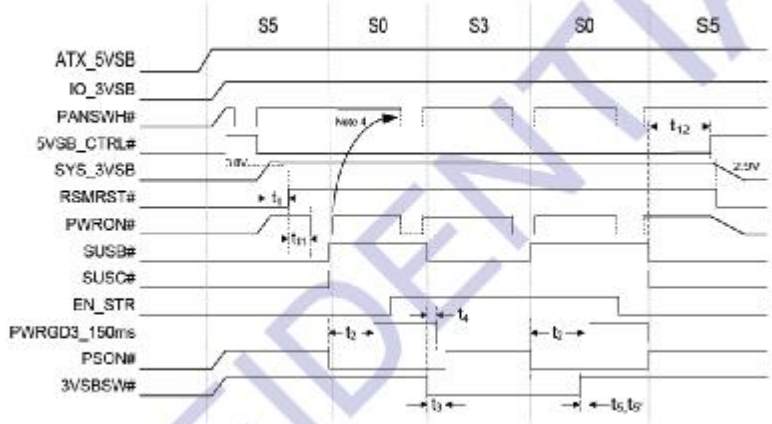


Figure 11-16. EuP Function Signal Timings



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FOXCONN PCEG

Title: Power On Sequence

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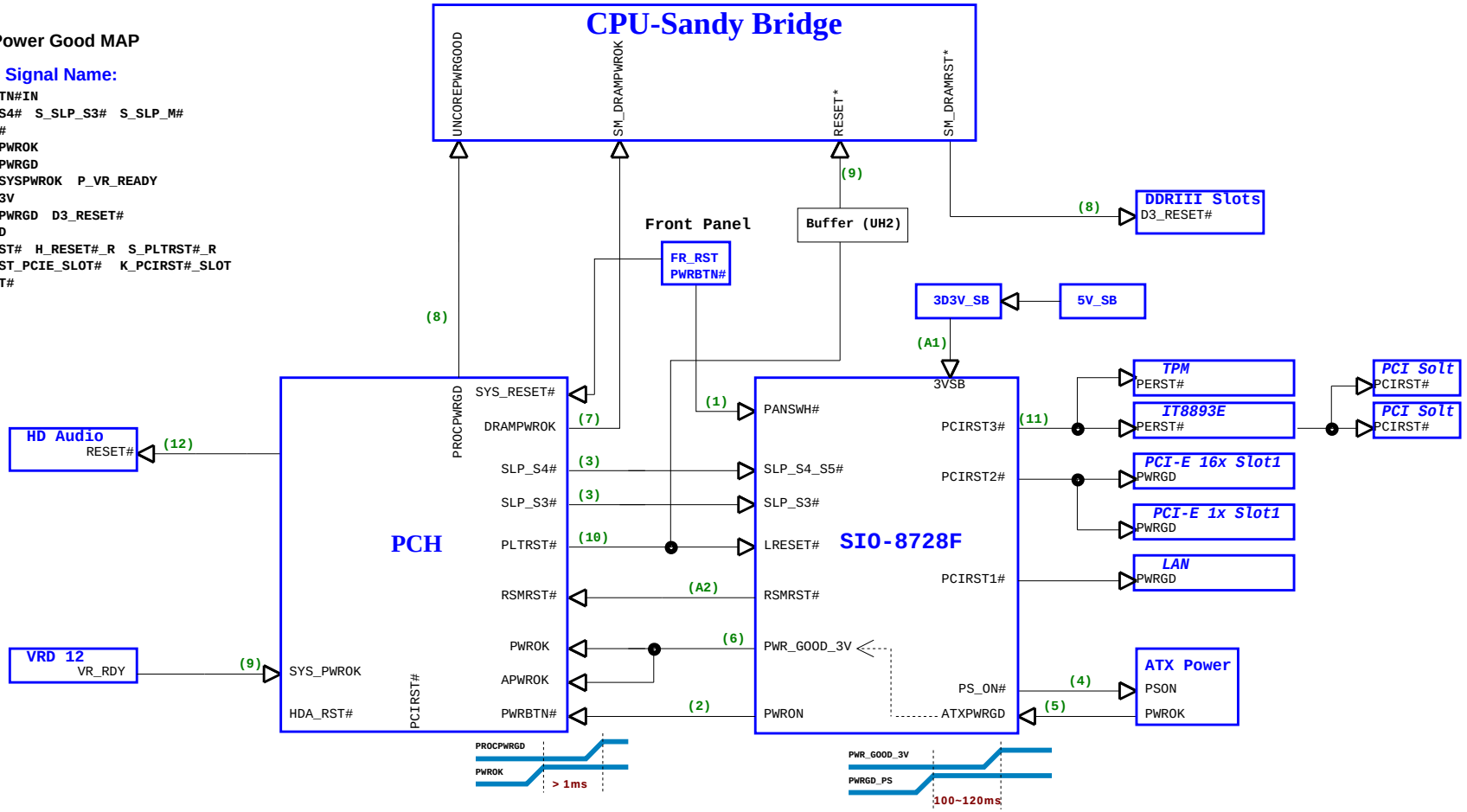
RESET / Power Good MAP

Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#



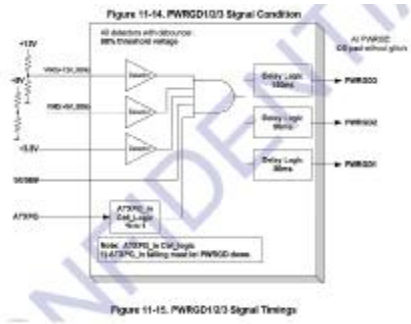


Figure 11-15. PWRGD1/2/3 Signal Timings

FOXCONN PCEG

Title: Reset/power good		
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IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	16	0	0

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	17	2	2

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

FOXCONN PCEG

Title: STRAP

Size: C | Document Number: H61MX | Rev: A

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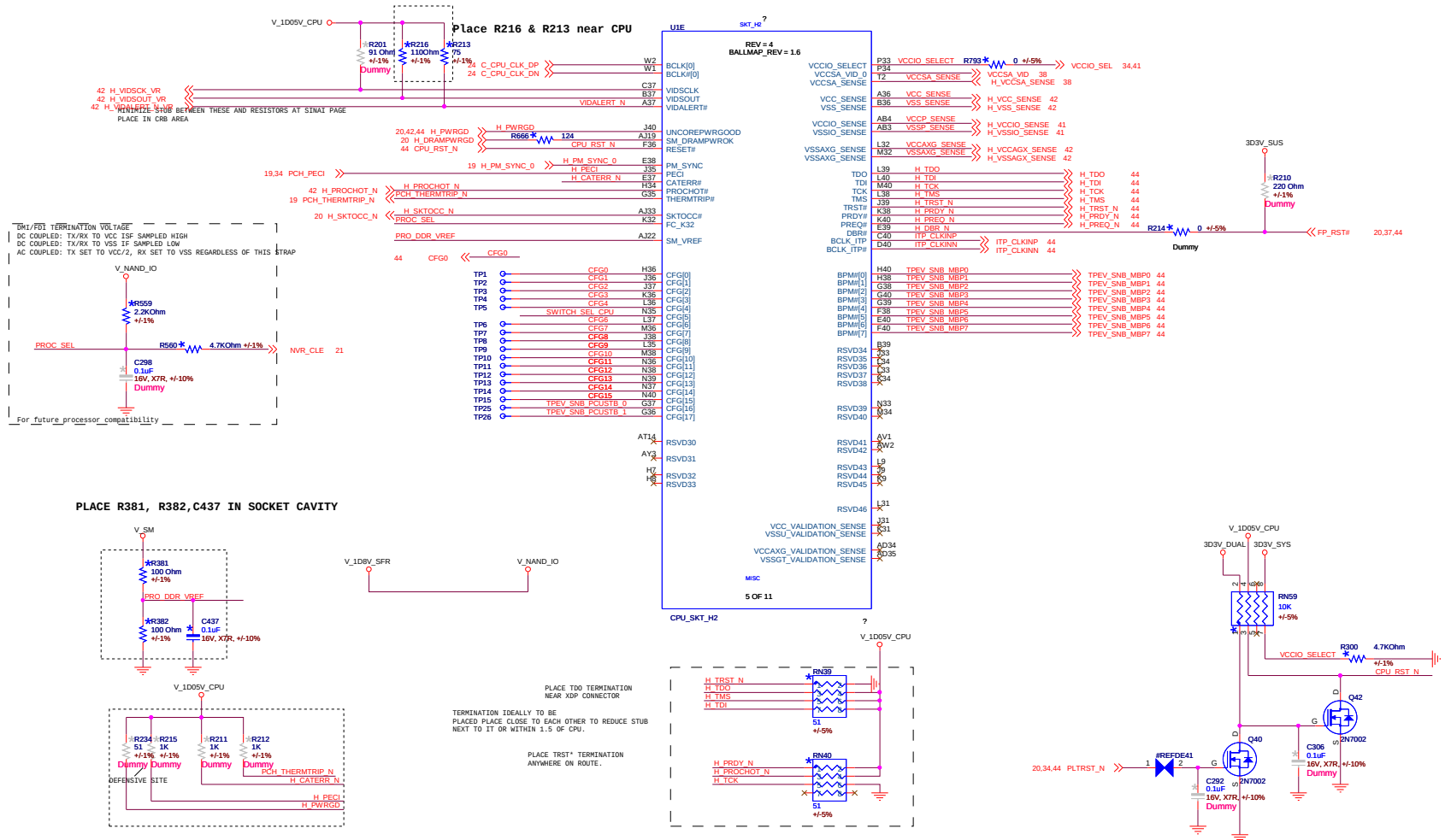
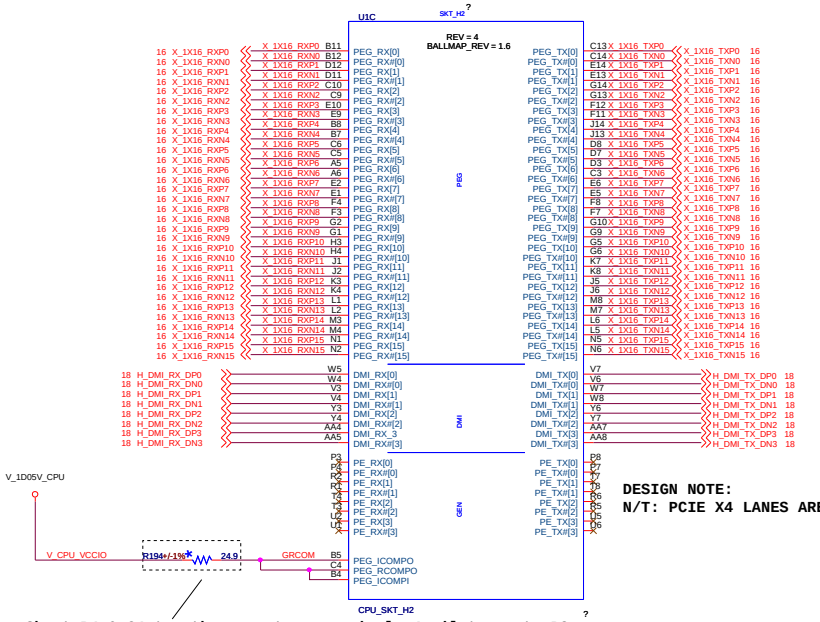
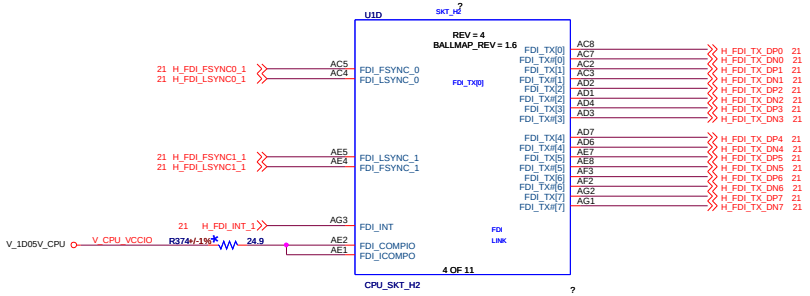


FOXCONN PCEG

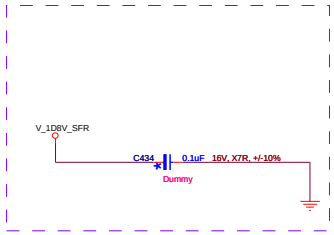
Title	CPU1-MSIC	
Size C	Document Number H61MX	Rev A
Date: Tuesday, May 03, 2011	Sheet 8 of 46	



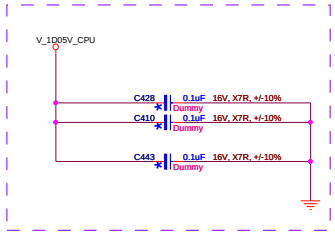


DESIGN NOTE:
N/T: PCIE X4 LANES ARE NOT SUPPORTED ON DESKTOP CPU SKUS

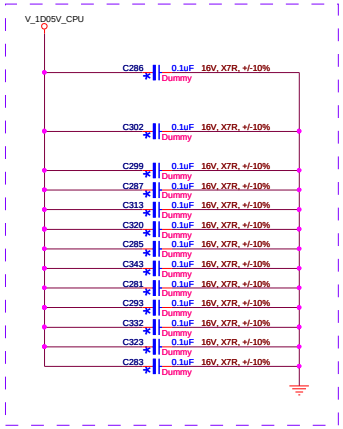
Short B4 & C4 together, route as a single 4 mil trace to R2
Route B5 to R2 as a aeperate 10 mil trace



Stiching CAP for FDI



Stiching CAP for DMI



Stiching CAP for PEG

FOXCONN PCEG

Title	CPU2-PEG/DMI/FDI	
Size C	Document Number H61MX	Rev A
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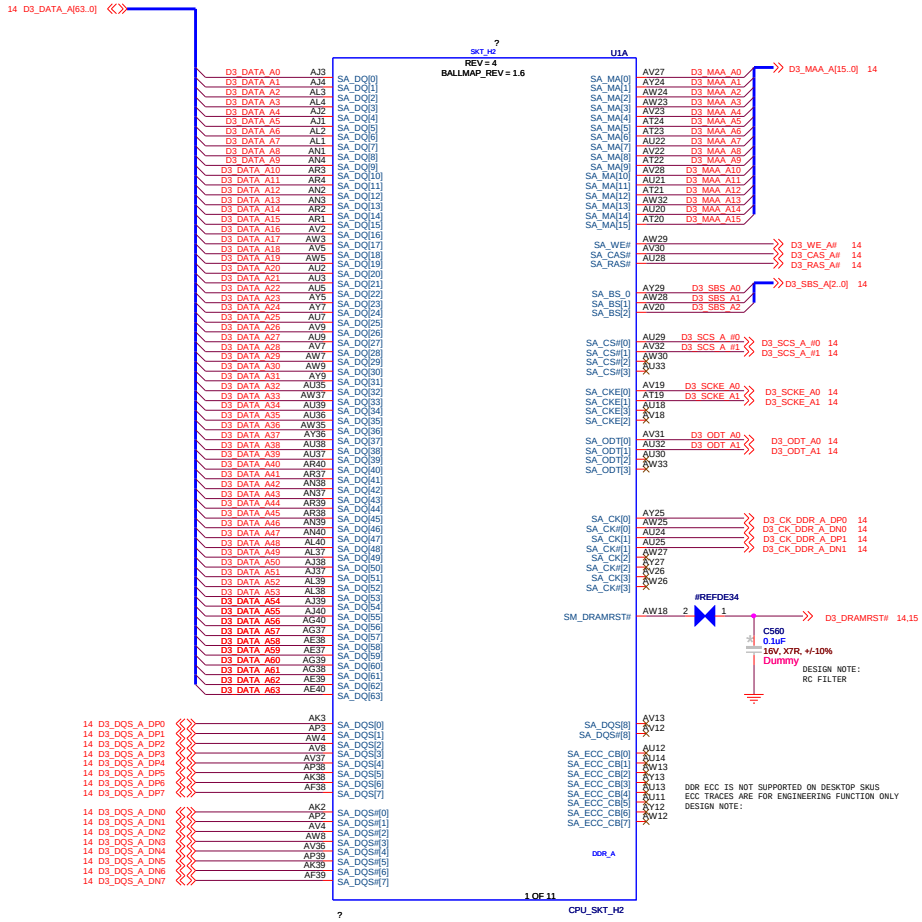
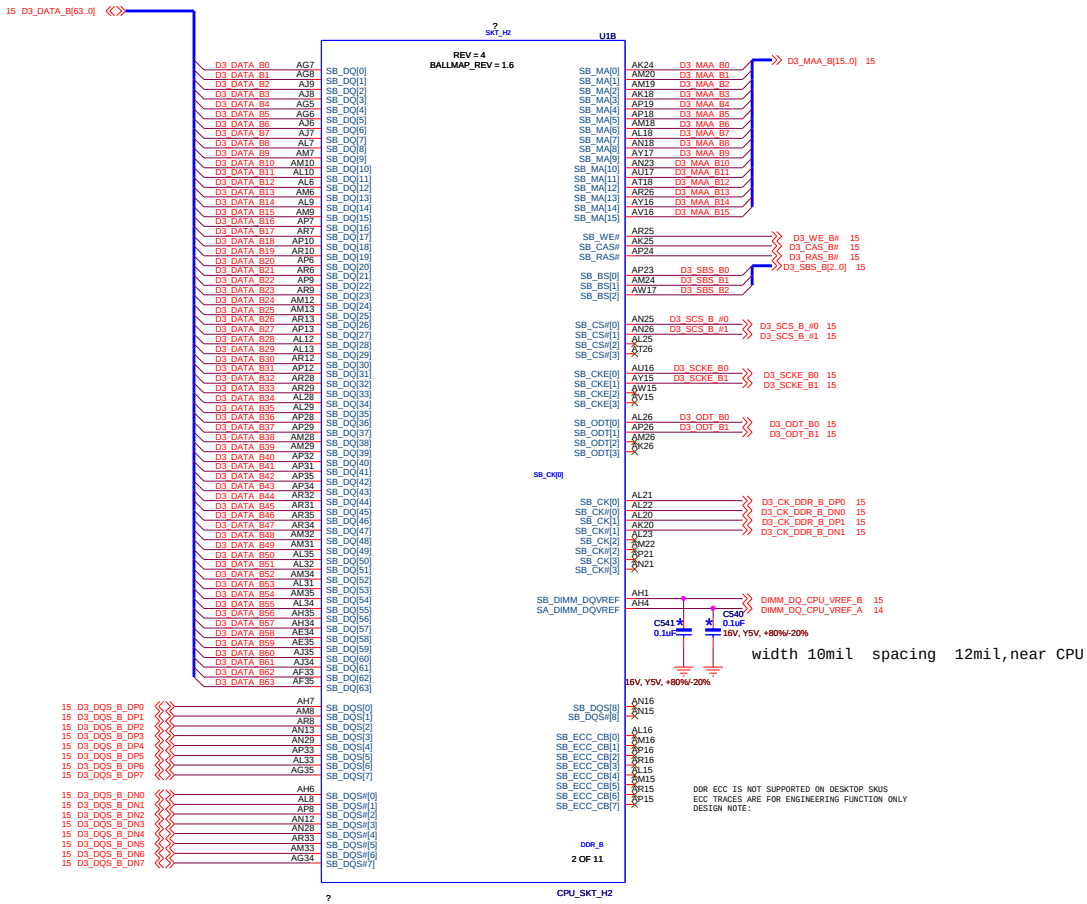


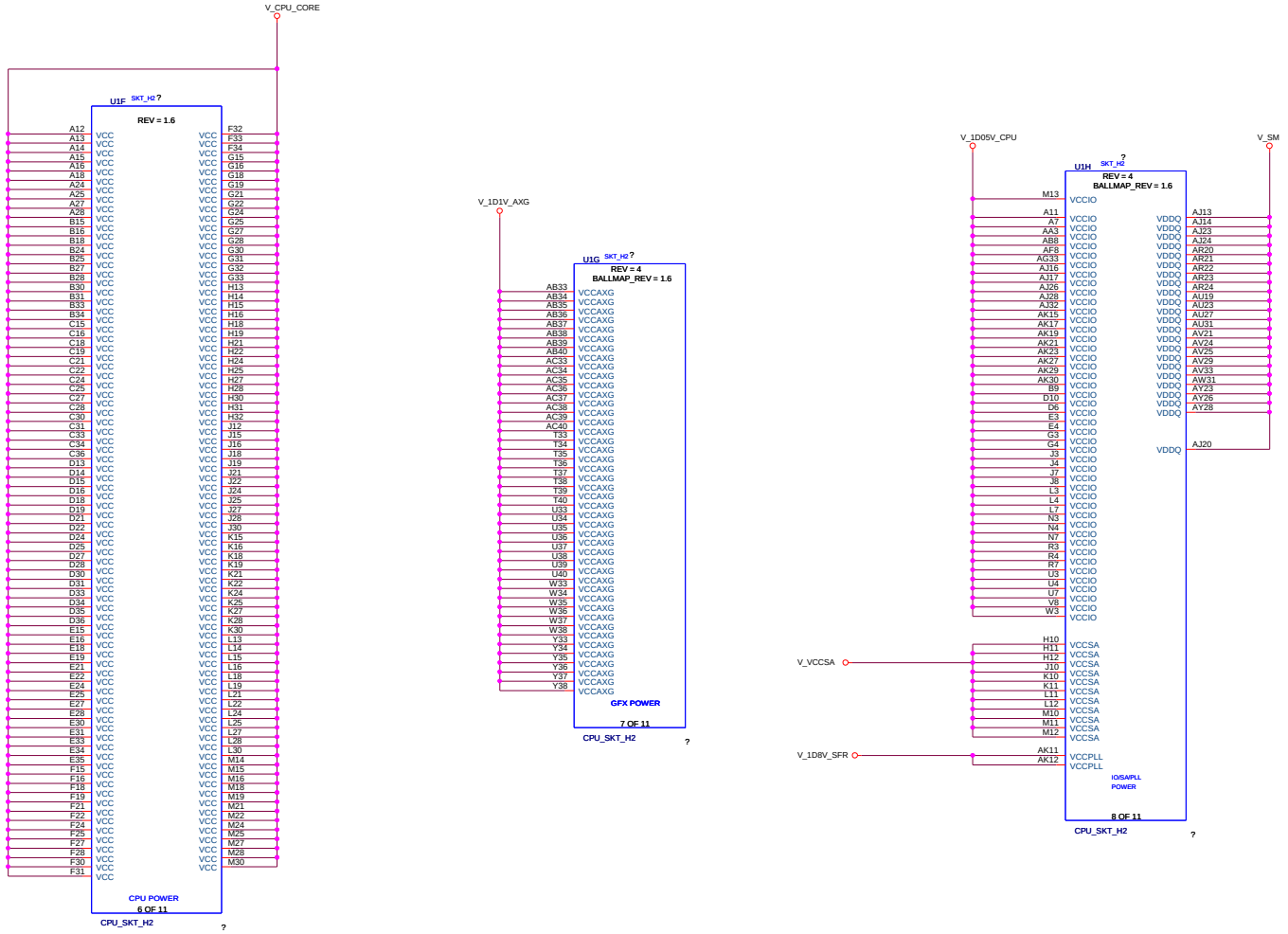
FOXCONN PCEG

Title	CPU3-DDR3_CHA		
Size C	Document Number H61MX		Rev A
Date: Tuesday, May 03, 2011		Sheet 10 of 46	



FOXCONN PCEG

Title	CPU4-DDR3_CHB	
Size C	Document Number H61MX	Rev A
Date: Tuesday, May 03, 2011	Sheet 11 of 46	



FOXCONN PCEG

Title	CPU5-POWER	
Size C	Document Number H61MX	Rev A
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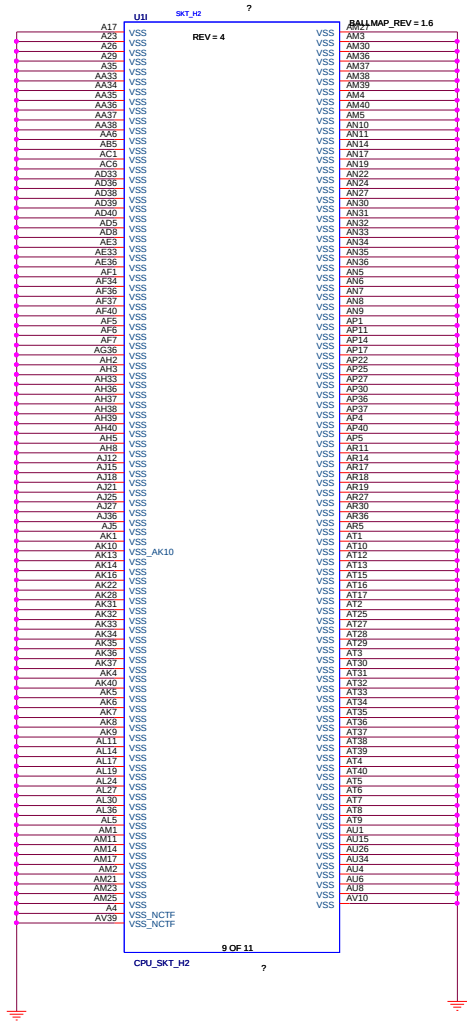

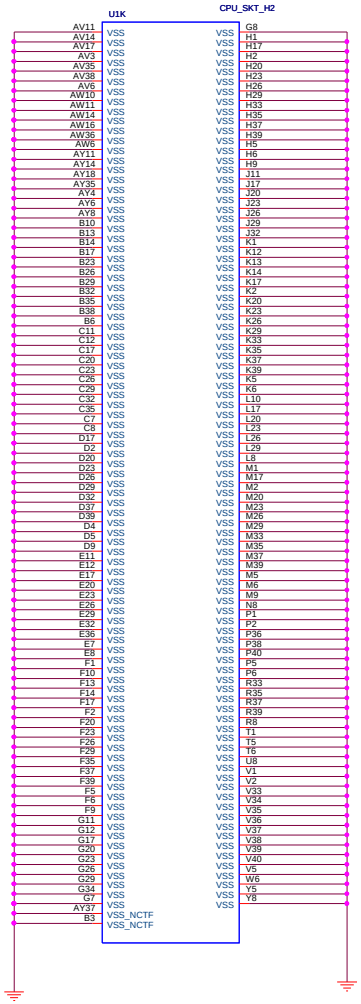

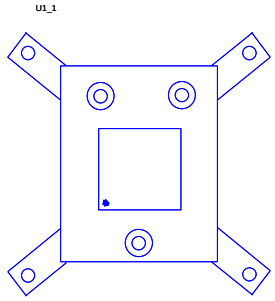

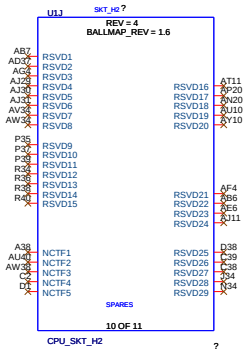

FOXCONN PCEG

Title: CPU6-GND		
Size: C	Document Number: H61MX	Rev: A
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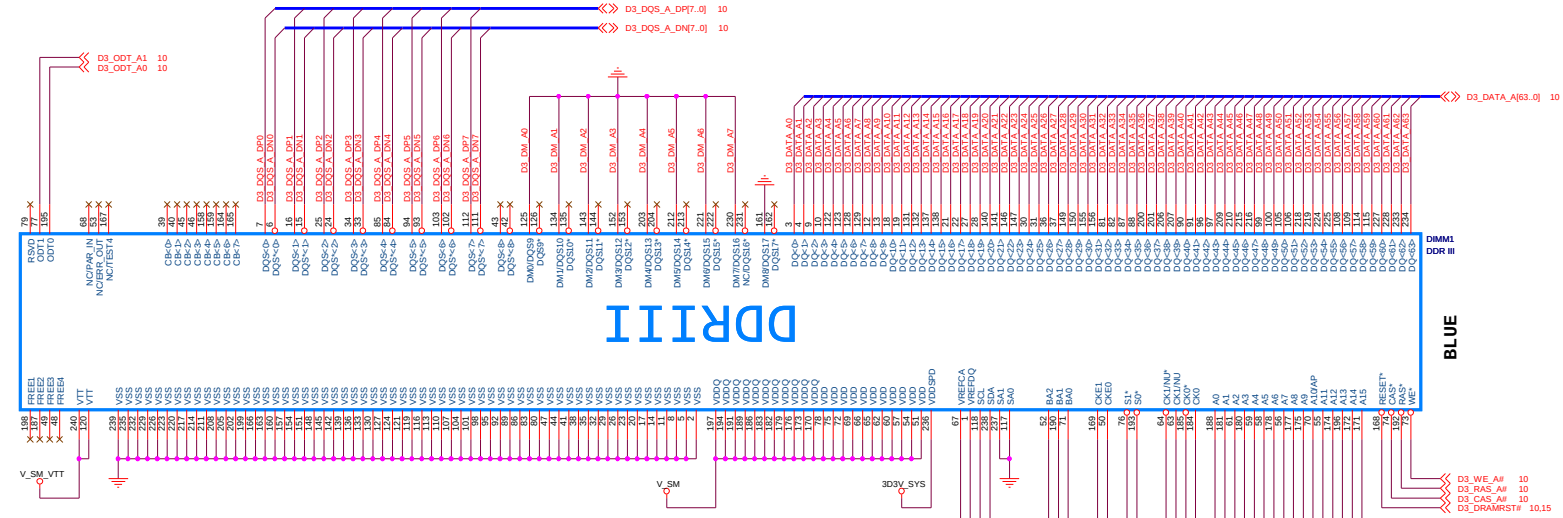
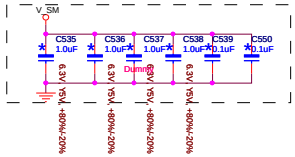
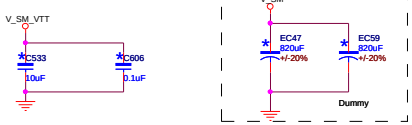
CHANNEL A DIMM 1
SMB ADDRESS:000

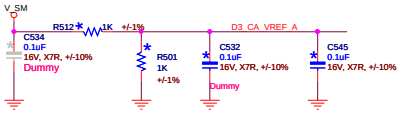


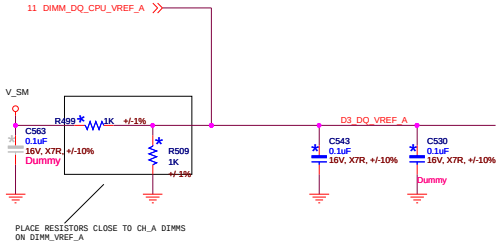
CLOSE TO DIMM POWER PIN



PLACE BETWEEN DIMM1 AND CPU







FOXCONN PCEG

Title: DDR3-1:CHA			
Size: C	Document Number: H61MX		Rev: A
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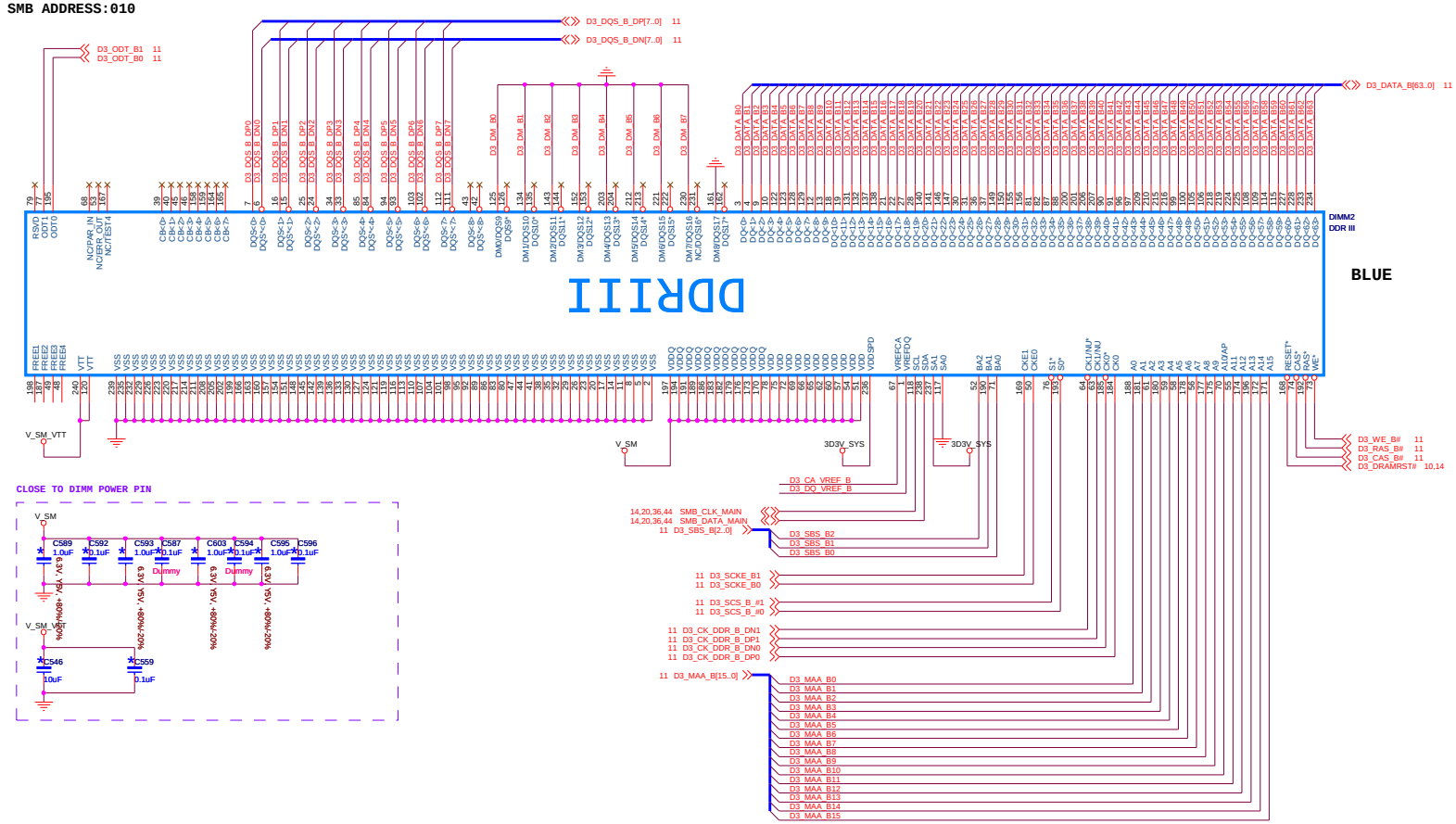
CHANNEL B DIMM 3
SMB ADDRESS:010



FOXCONN PCEG

Title	DDR3-2:CHB	
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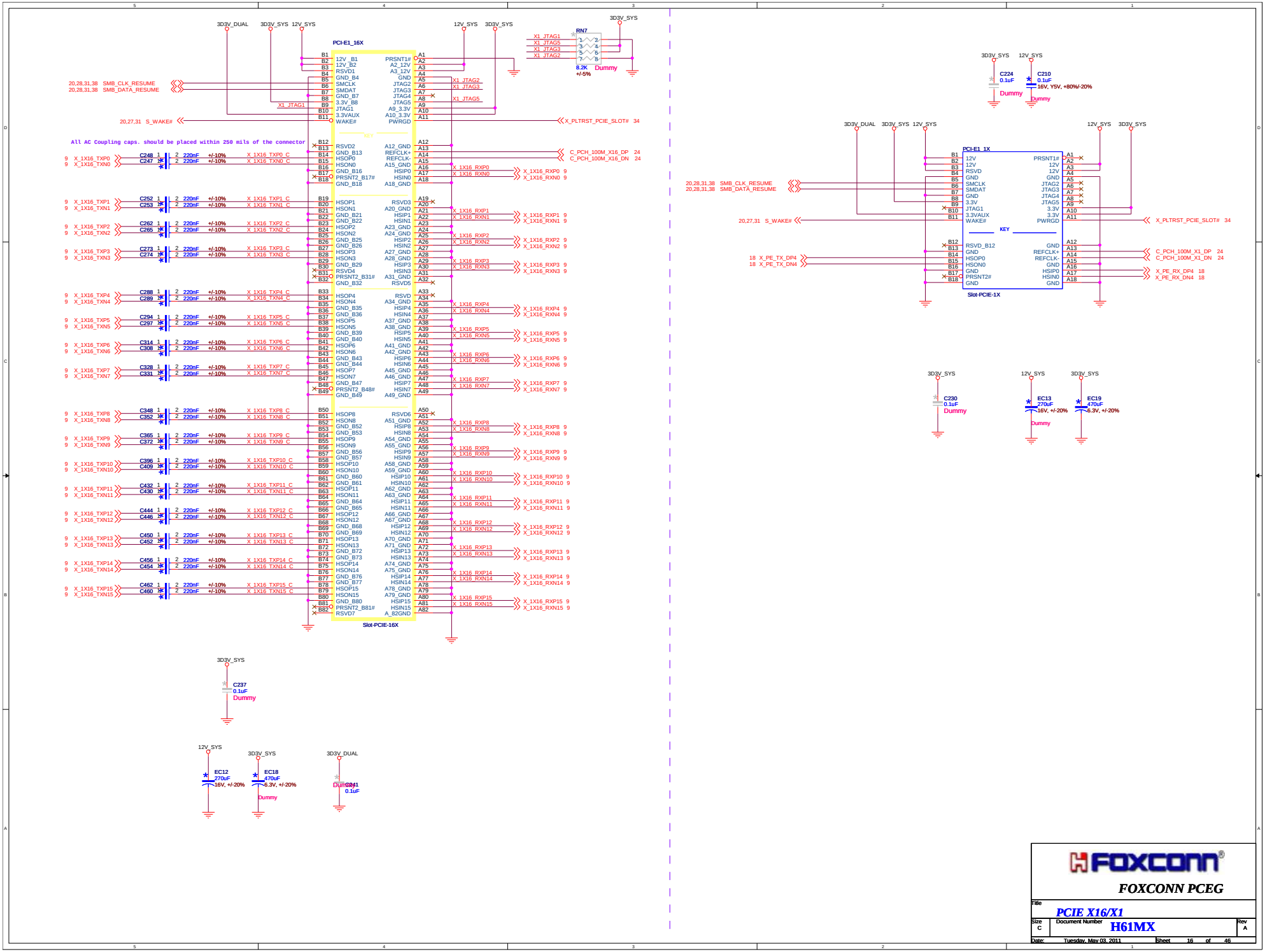

FOXCONN PCEG

Title: PCIE X16/X1

Size: C | Document Number: H61MX | Rev: A

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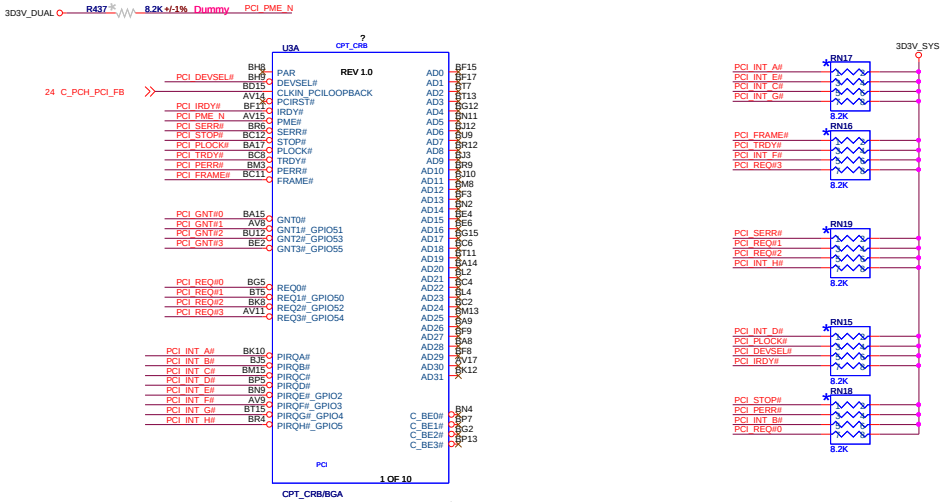

STRAP: Boot BIOSselect

check whether GNT1 or SATA1GP(GPIO19)

BOOT DEVICE	GNT1	SATA1GP
LPC	0	0
NAND	0	1
PCI	1	0
SPI	1	1

PCI_GNT#0 R445 * 1K Dummy

PCI_GNT#1 R438 * 1K Dummy

Internal pull-up

PCI_GNT#3 R446 * 1K Dummy

PCI_GNT#2 R454 * 1K Dummy

DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode

GNT2#/GPIO53:ESI strap for server platform
ONLY,Do not pull low.

FOXCONN PCEG

Title: PCH1-PCI

Size: C | Document Number: H61MX | Rev: A

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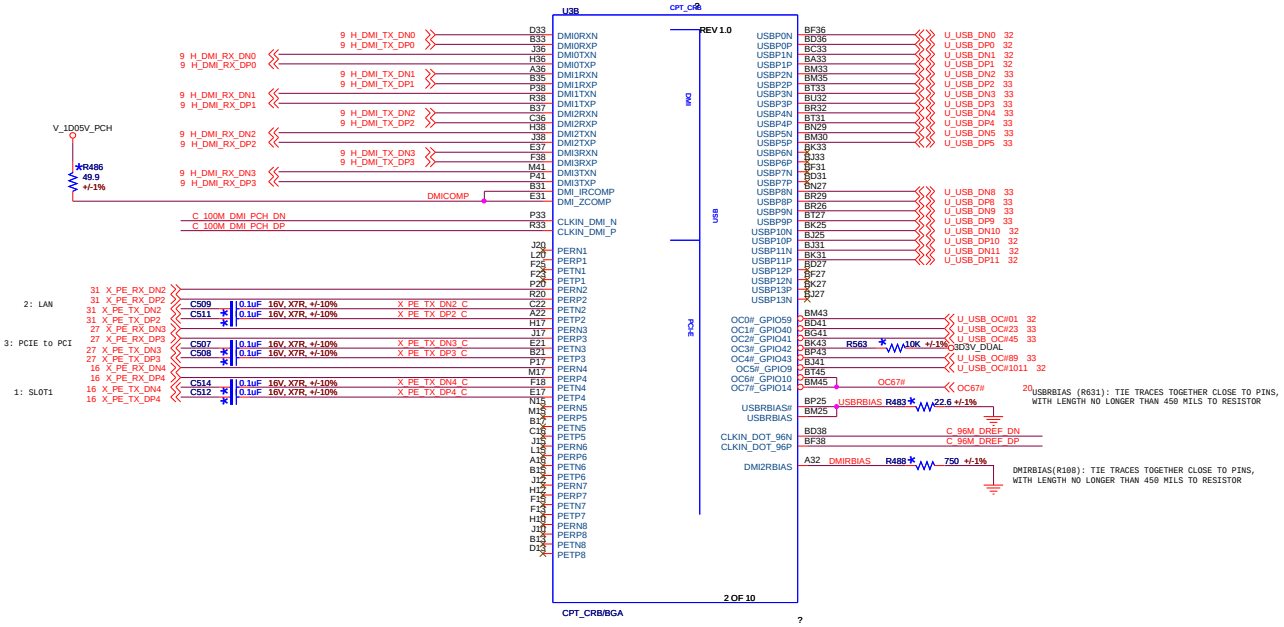

FOXCONN PCEG

Title	PCH2-DMI/PCIE/USB	
Size C	Document Number H61MX	Rev A
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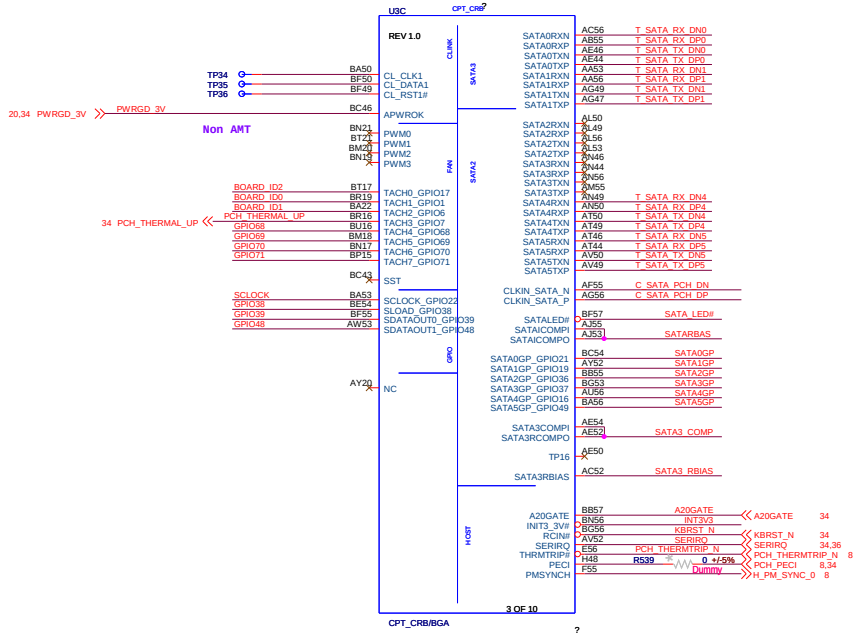
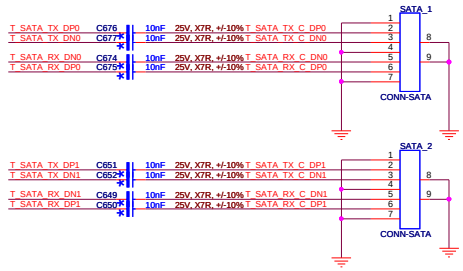
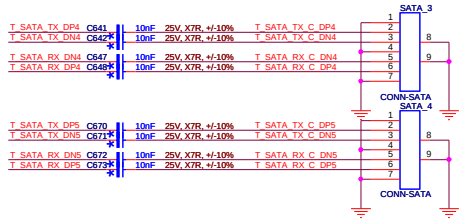
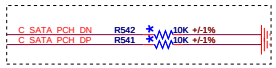


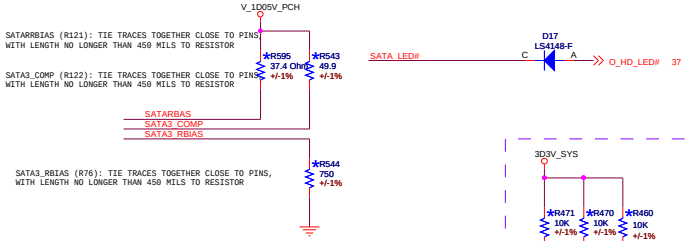


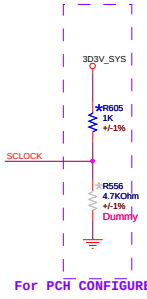




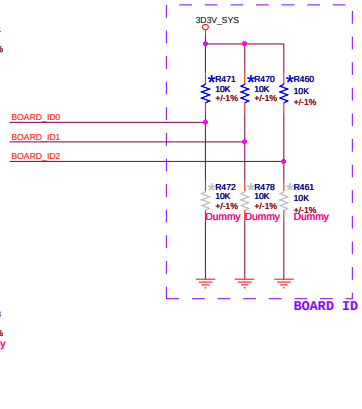
Stub is as short as possible

Resistor can change RN



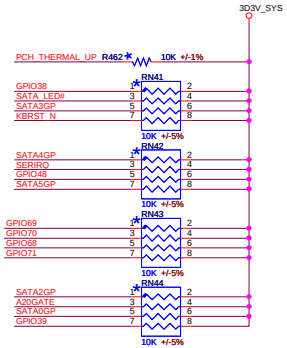


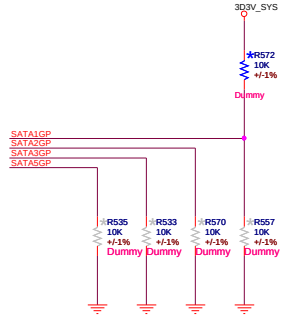
For PCH CONFIGURE



BOARD ID

Need double check





FOXCONN PCEG

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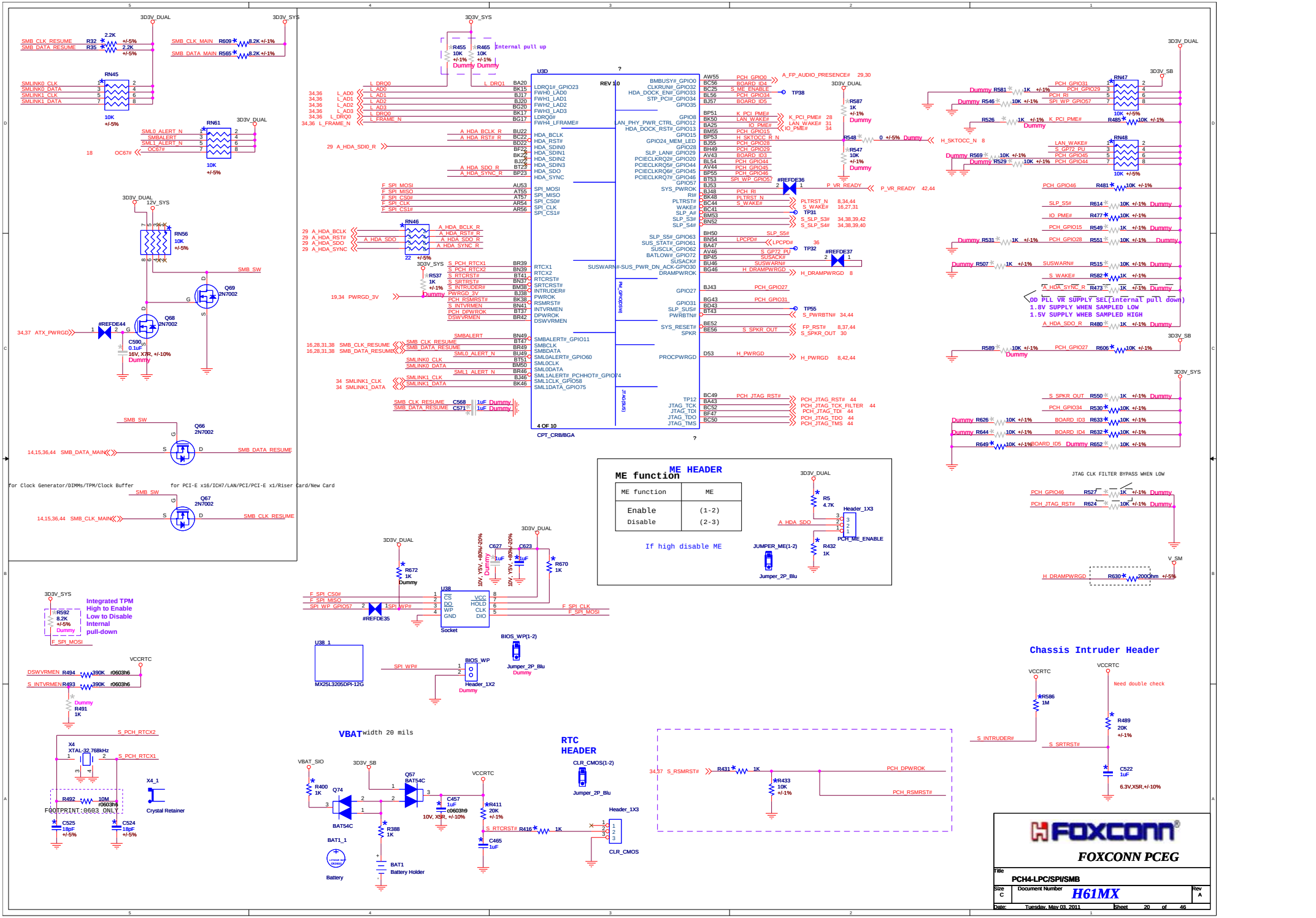
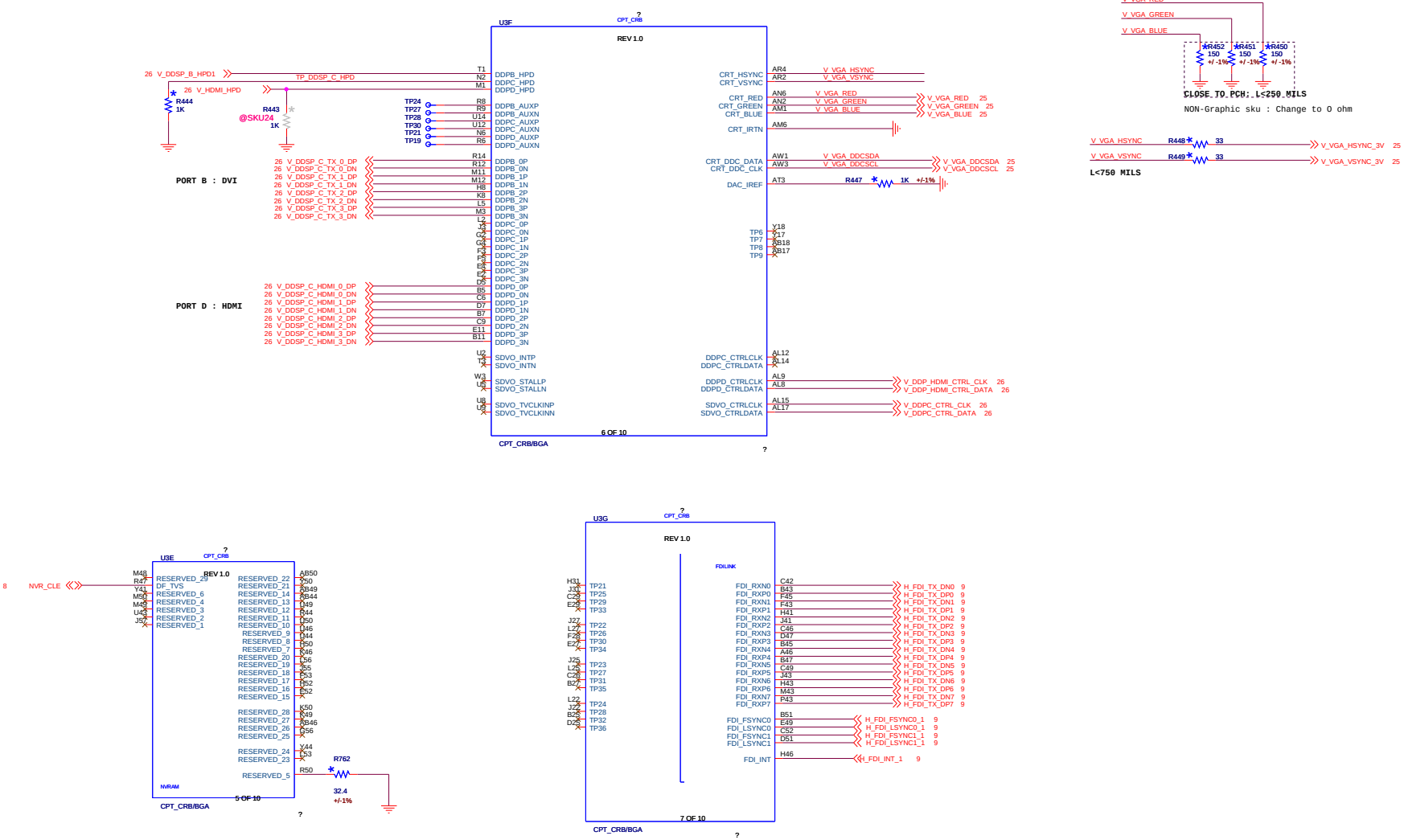
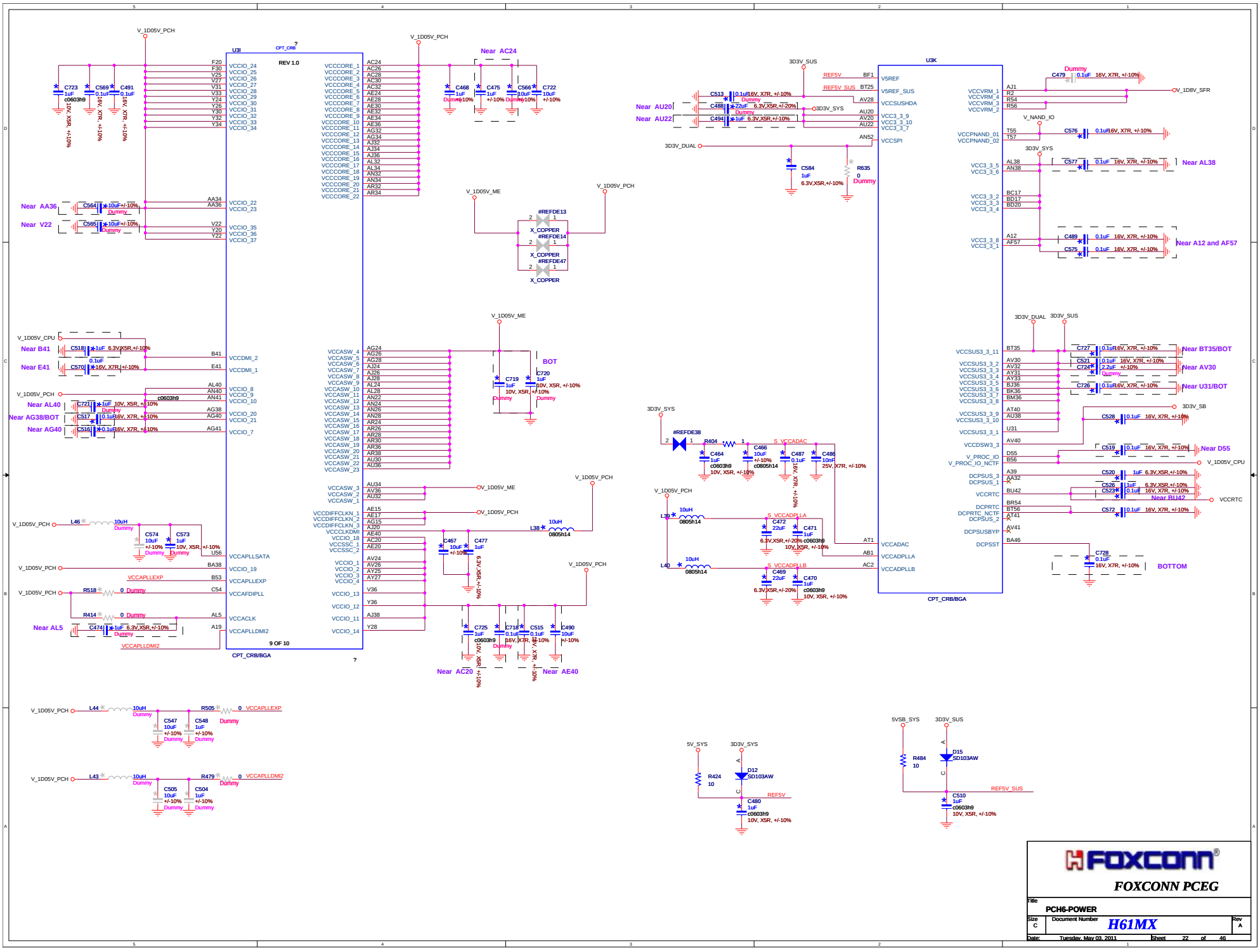

3D3V_DUAL
3D3V_SYS
SMB_CLK_RESUME R32 2.2K +/-5%
SMB_DATA_RESUME R35 2.2K +/-5%
SMB_CLK_MAIN R609 8.2K +/-1%
SMB_DATA_MAIN R565 8.2K +/-1%
RN45
SMLINK0_CLK
SMLINK0_DATA
SMLINK1_CLK
SMLINK1_DATA
10K +/-5%
RN61
SML0_ALERT_N
SMBALERT
SML1_ALERT_N
OC67#
18
10K +/-5%
12V_SYS
RN56 10K +/-5%
SMB_SW
Q69 2N7002
Q68 2N7002
#REFDE44
34,37 ATX_PWRGD
C590 0.1uF 16V, X7R, +/-10% Dummy
for Clock Generator/DIMMs/TPM/Clock Buffer
for PCI-E x16/ICH7/LAN/PCI/PCI-E x1/Riser Card/New Card
Q66 2N7002
14,15,36,44 SMB_DATA_MAIN
SMB_DATA_RESUME
Q67 2N7002
14,15,36,44 SMB_CLK_MAIN
SMB_CLK_RESUME
R455 10K +/-1% Dummy
R465 10K +/-1% Internal pull up
U3D
REV 1.0
LDRQ1#_GPIO23
FWH0_LAD0
FWH1_LAD1
FWH2_LAD2
FWH3_LAD3
LDRQ0#
FWH4_LFRAME#
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1#
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
DPWROK
DSWVRMEN
SMBALERT#_GPIO11
SMBCLK
SMBDATA
SML0ALERT#_GPIO60
SML0CLK
SML0DATA
SML1ALERT# PCHHOT#_GPIO74
SML1CLK_GPIO58
SML1DATA_GPIO75
TP12
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
4 OF 10
CPT_CRB/BGA
BMBUSY#_GPIO0
CLKRUN#_GPIO32
HDA_DOCK_EN#_GPIO33
STP_PCI#_GPIO34
GPIO35
GPIO8
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO24_MEM_LED
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK
RI#
PLTRST#
WAKE#
SLP_A#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SUS_STAT#_GPIO61
SUSCLK_GPIO62
BATLOW#_GPIO72
SUSACK#
SUSWARN#-SUS_PWR_DN_ACK-GPIO30
DRAMPWROK
GPIO27
GPIO31
SLP_SUS#
PWRBTN#
SYS_RESET#
SPKR
PROCPWRGD
PM_GPIO(30)
JTAG(5)
AW55 PCH_GPIO0 A_FP_AUDIO_PRESENCE# 29,30
BC56 BOARD_ID4
BC25 S_ME_ENABLE TP38
BL56 PCH_GPIO34
BJ57 BOARD_ID5
BP51 K_PCI_PME#
BK50 LAN_WAKE#
BA25 IO_PME#
BM55 PCH_GPIO15
BP53 H_SKTOCC_R_N
BJ55 PCH_GPIO28
BH49 PCH_GPIO29
AV43 BOARD_ID3
BL54 PCH_GPIO44
AV44 PCH_GPIO45
BP55 PCH_GPIO46
BT53 SPI_WP_GPIO57
BJ53
BJ48 PCH_RI
BK48 PLTRST_N
BC44 S_WAKE#
BC41
BM53
BN52
BH50 SLP_S5#
BN54 LPCPD#
BA47
AV46 S_GP72_PU
BP45 SUSACK#
BU46 SUSWARN#
BG46 H_DRAMPWRGD
BJ43 PCH_GPIO27
BG43 PCH_GPIO31
BD43
BT43
BE52
BE56 S_SPKR_OUT
D53 H_PWRGD
BC49 PCH_JTAG_RST#
BA43
BC52
BF47
BC50
R587 1K +/-1% Dummy
R548 0 +/-5% Dummy H_SKTOCC_N 8
R547 10K +/-1% Dummy
#REFDE36
P_VR_READY 42,44
#REFDE37
TP32
TP31
TP55
S_PWRBTN# 34,44
FP_RST# 8,37,44
S_SPKR_OUT 30
H_PWRGD 8,42,44
PCH_JTAG_RST# 44
PCH_JTAG_TCK_FILTER 44
PCH_JTAG_TDI 44
PCH_JTAG_TDO 44
PCH_JTAG_TMS 44
RN46
A_HDA_SDO
A_HDA_BCLK_R
A_HDA_RST#_R
A_HDA_SDO_R
A_HDA_SYNC_R
22 +/-5%
R537 1K +/-1% Dummy
19,34 PWRGD_3V
S_PCH_RTCX1
S_PCH_RTCX2
S_RTCRST#
S_SRTRST#
S_INTRUDER#
PWRGD_3V
PCH_RSMRST#
S_INTVRMEN
PCH_DPWROK
DSWVRMEN
SMBALERT
SML0_ALERT_N
SML1_ALERT_N
SMLINK0_CLK
SMLINK0_DATA
SMLINK1_CLK
SMLINK1_DATA
16,28,31,38 SMB_CLK_RESUME
16,28,31,38 SMB_DATA_RESUME
SMB_CLK_RESUME C568 1uF Dummy
SMB_DATA_RESUME C571 1uF Dummy
ME HEADER
ME function
ME function | ME
Enable | (1-2)
Disable | (2-3)
If high disable ME
R5 4.7K
Header_1X3
PCH_ME_ENABLE
R432 1K
JUMPER_ME(1-2)
Jumper_2P_Blu
R672 1K Dummy
C627 1uF
C623 1uF
10V, Y5V, +80%/-20%
R670 1K
U38
Socket
#REFDE35
F_SPI_CS0#
F_SPI_MISO
SPI_WP_GPIO57
F_SPI_CLK
F_SPI_MOSI
U38_1
MX25L3205DPI-12G
BIOS_WP(1-2)
Jumper_2P_Blu Dummy
BIOS_WP
Header_1X2 Dummy
SPI_WP#
Integrated TPM
High to Enable
Low to Disable
Internal
pull-down
R592 8.2K +/-5% Dummy
VCCRTC
DSWVRMEN R494 390K r0603h6
S_INTVRMEN R493 390K r0603h6
R491 1K Dummy
S_PCH_RTCX2
S_PCH_RTCX1
X4 XTAL-32.768kHz
X4_1
Crystal Retainer
R492 10M r0603h6
FOOTPRINT:0603 ONLY
C525 18pF +/-5%
C524 18pF +/-5%
VBAT width 20 mils
VBAT_SIO
R400 1K
Q74
BAT54C
Q57 BAT54C
C457 1uF c0603h9 10V, X5R, +/-10%
R411 20K +/-1%
R388 1K
BAT1_1
Battery
BAT1 Battery Holder
C465 1uF
RTC HEADER
CLR_CMOS(1-2)
Jumper_2P_Blu
Header_1X3
CLR_CMOS
34,37 S_RSMRST#
R431 1K
R433 10K +/-1%
PCH_DPWROK
PCH_RSMRST#
Chassis Intruder Header
R586 1M
Need double check
R489 20K +/-1%
C522 1uF 6.3V,X5R,+/-10%
S_INTRUDER#
S_SRTRST#
RN47
RN48
PCH_GPIO31
PCH_RI
SPI_WP_GPIO57
K_PCI_PME#
LAN_WAKE#
S_GP72_PU
PCH_GPIO45
PCH_GPIO44
R481 10K +/-1%
R614 10K +/-1% Dummy
R477 10K +/-1%
R549 1K +/-1% Dummy
R551 10K +/-1% Dummy
R515 10K +/-1% Dummy
R582 1K +/-1%
R473 1K +/-1% Dummy
R480 1K +/-1% Dummy
R606 10K +/-1%
R550 1K +/-1% Dummy
R530 10K +/-1%
R633 10K +/-1%
R632 10K +/-1%
R652 10K +/-1%
OD PLL VR SUPPLY SEL(internal pull down)
1.8V SUPPLY WHEN SAMPLED LOW
1.5V SUPPLY WHEB SAMPLED HIGH
JTAG CLK FILTER BYPASS WHEN LOW
R527 1K +/-1% Dummy
R624 10K +/-1% Dummy
R630 200Ohm +/-5%
V_SM
FOXCONN
FOXCONN PCEG
Title
PCH4-LPC/SPI/SMB
Size C
Document Number H61MX
Rev A
Date: Tuesday, May 03, 2011
Sheet 20 of 46



FOXCONN PCEG

Title	PCH5-NVAND/FDI/DISPLAY	
Size C	Document Number H61MX	Rev A
Date: Tuesday, May 03, 2011	Sheet 21 of 46	


U3I
CPT_CRB
REV 1.0
9 OF 10
CPT_CRB/BGA
U3K
CPT_CRB/BGA
V_1D05V_PCH
V_1D05V_ME
V_1D05V_CPU
3D3V_SUS
3D3V_SYS
3D3V_DUAL
5V_SYS
5VSB_SYS
Near AC24
Near AA36
Near V22
Near B41
Near E41
Near AL40
Near AG38/BOT
Near AG40
Near AL5
Near AC20
Near AE40
Near AU20
Near AU22
Near AL38
Near A12 and AF57
Near BT35/BOT
Near AV30
Near U31/BOT
Near D55
Near BU42
BOT
BOTTOM
VCCAPLLSATA
VCCAPLLEXP
VCCAPLLDMI2
VCCAFDIPLL
VCCACLK
VCCADAC
VCCADPLLA
VCCADPLLB
VCCRTC
V_NAND_IO
V_1D8V_SFR
V_PROC_IO
V_PROC_IO_NCTF
FOXCONN PCEG
PCH6-POWER
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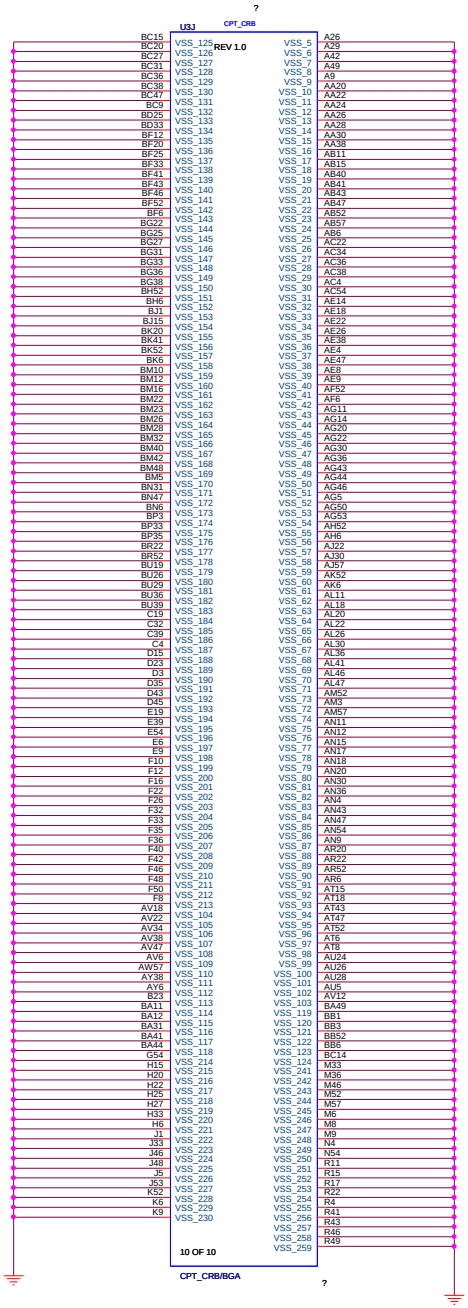
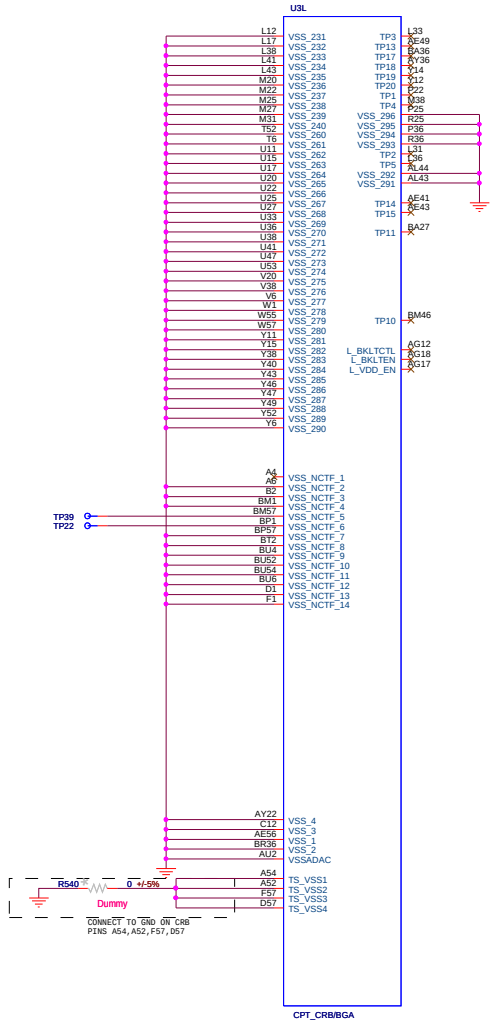
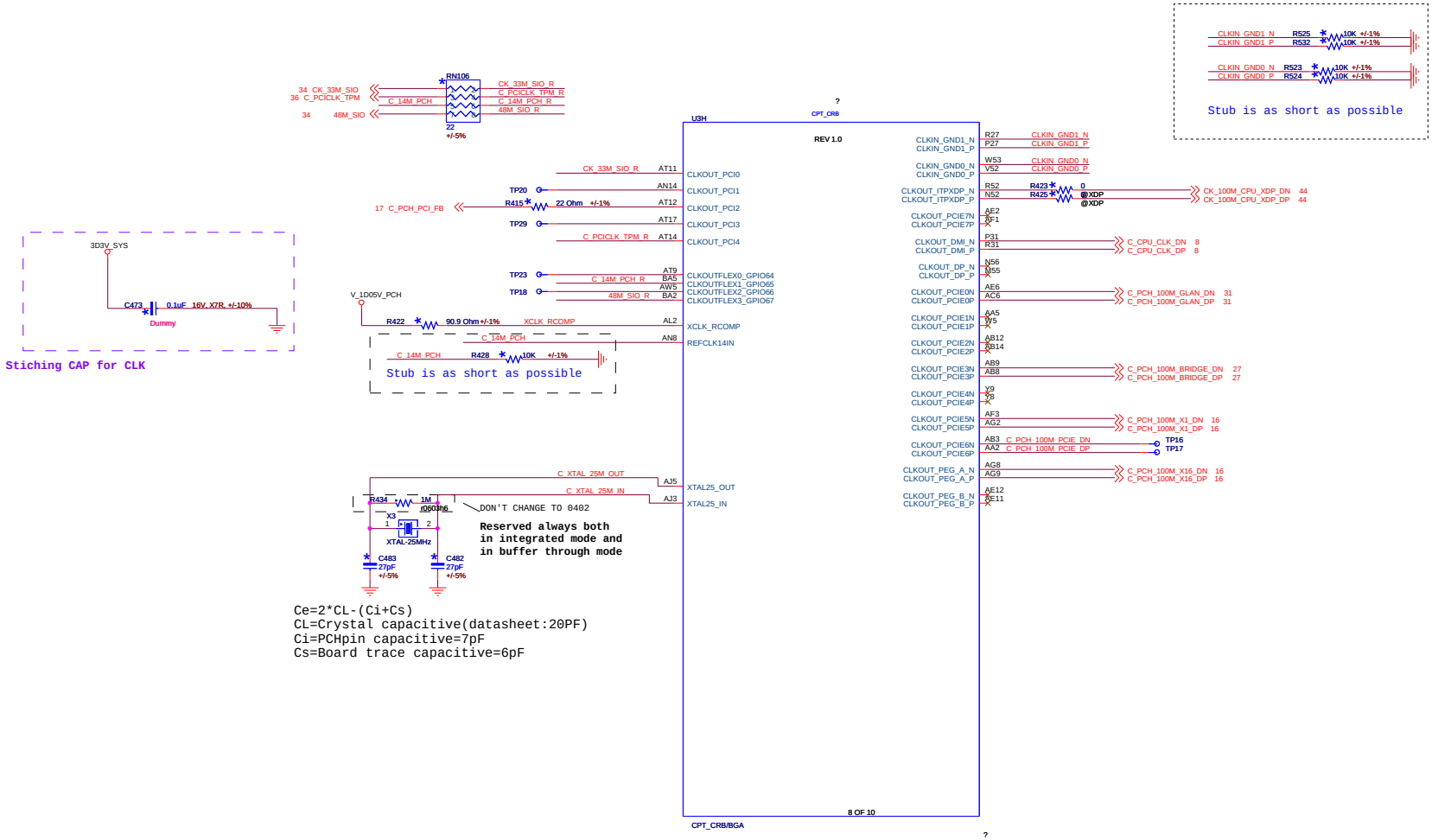




FOXCONN PCEG

Title: PCH7-GND			
Size: C	Document Number: H61MX		Rev: A
Date: Tuesday, May 03, 2011	Sheet 23 of 46		



Ce=2*CL-(Ci+Cs)
CL=Crystal capacitive(datasheet:20PF)
Ci=PCHpin capacitive=7pF
Cs=Board trace capacitive=6pF

FOXCONN PCEG

Title: PCH8-CLOCK		
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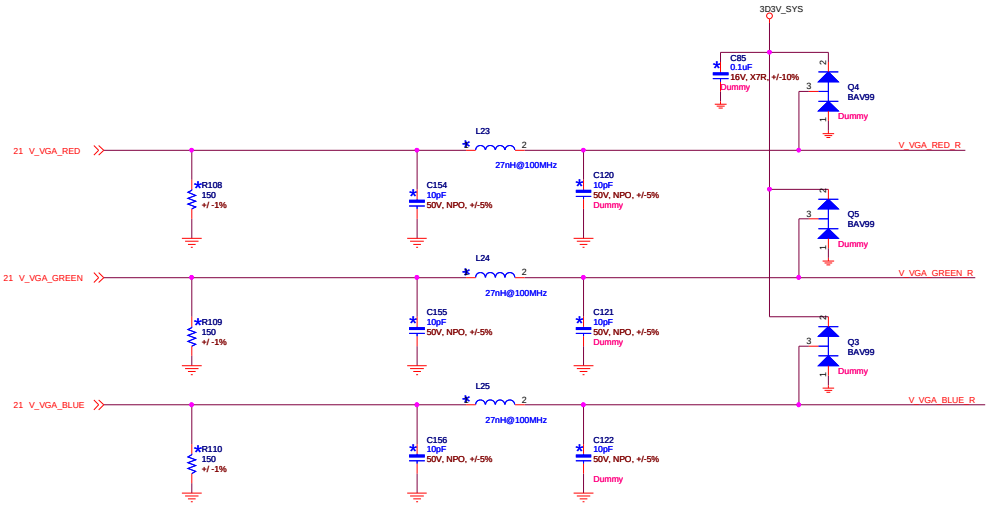

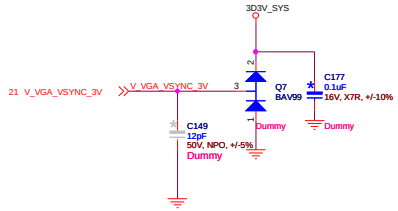

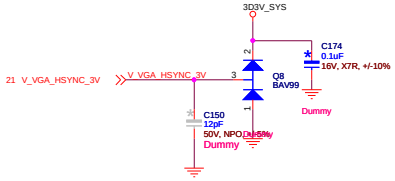

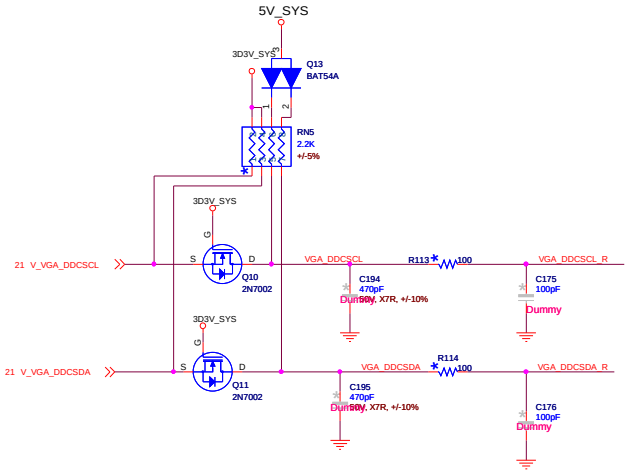

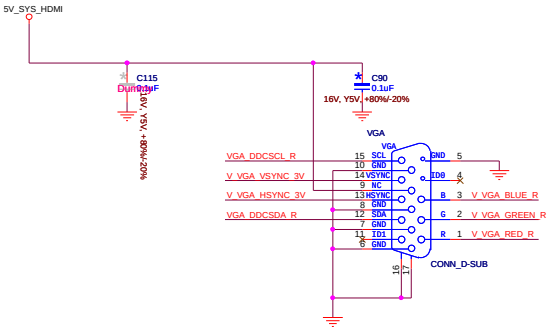

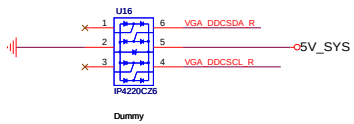

FOXCONN PCEG

Title: VGA

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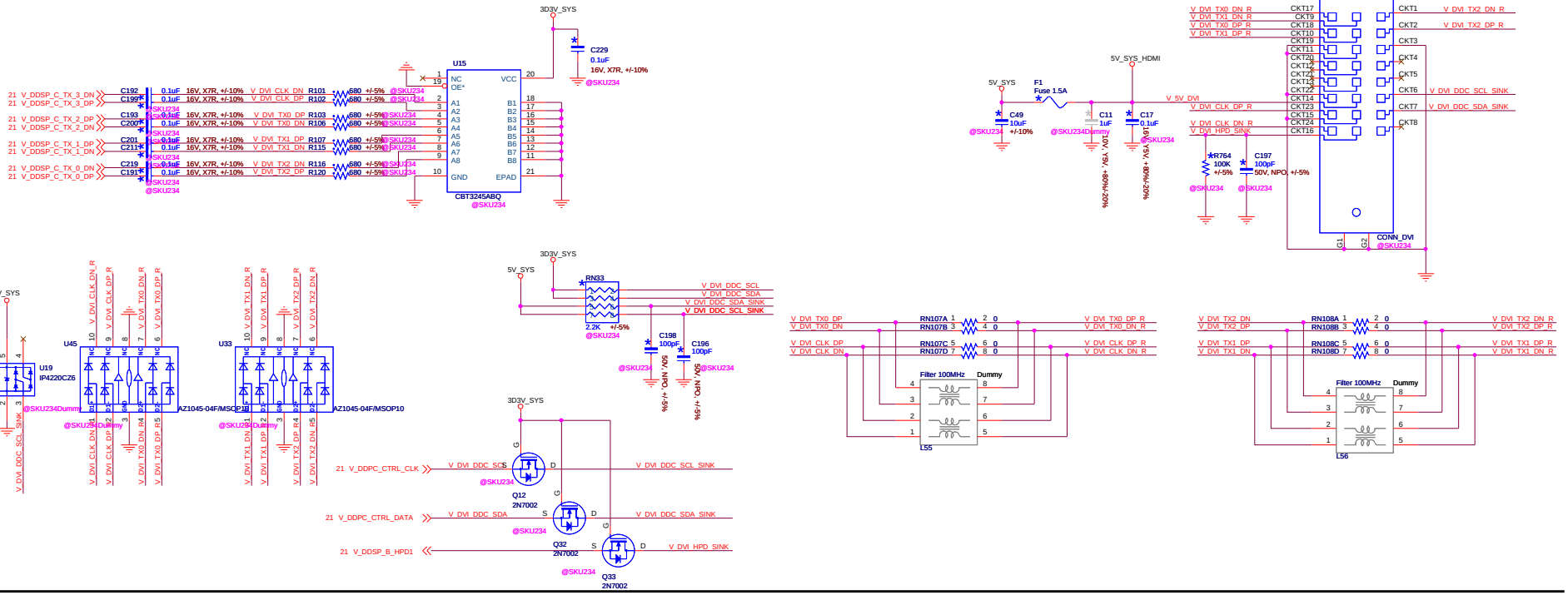
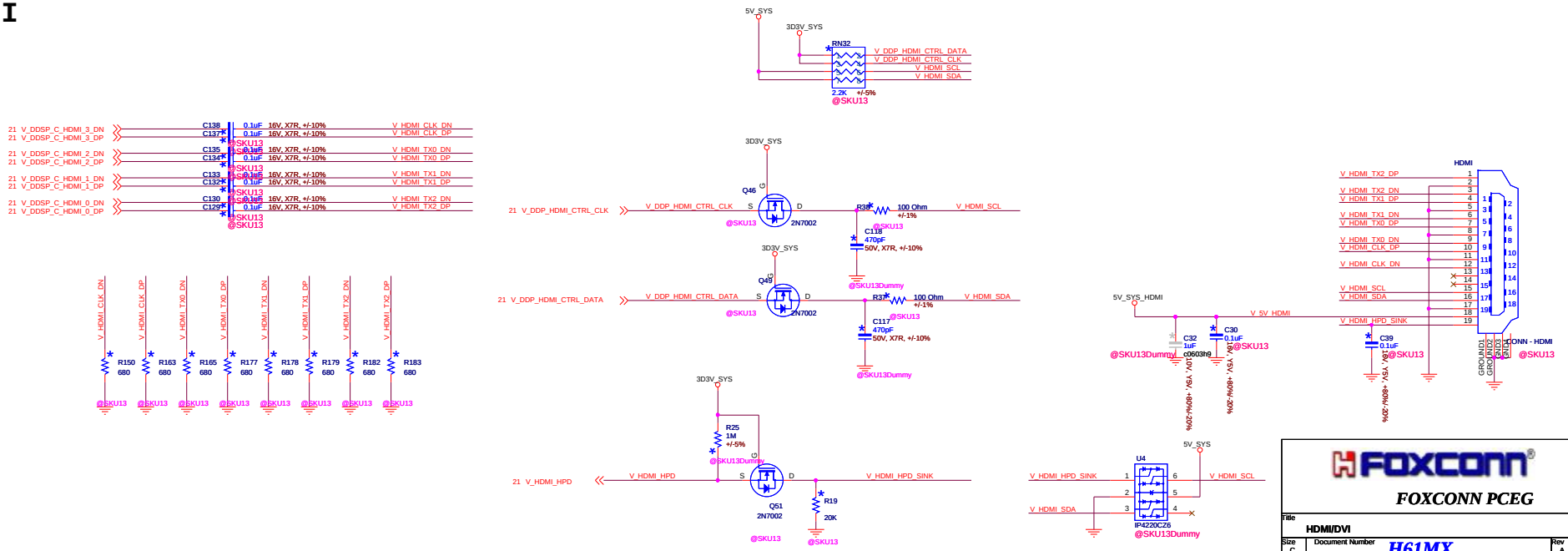
DVI-D



HDMI



FOXCONN PCEG

Title	HDMI/DVI	
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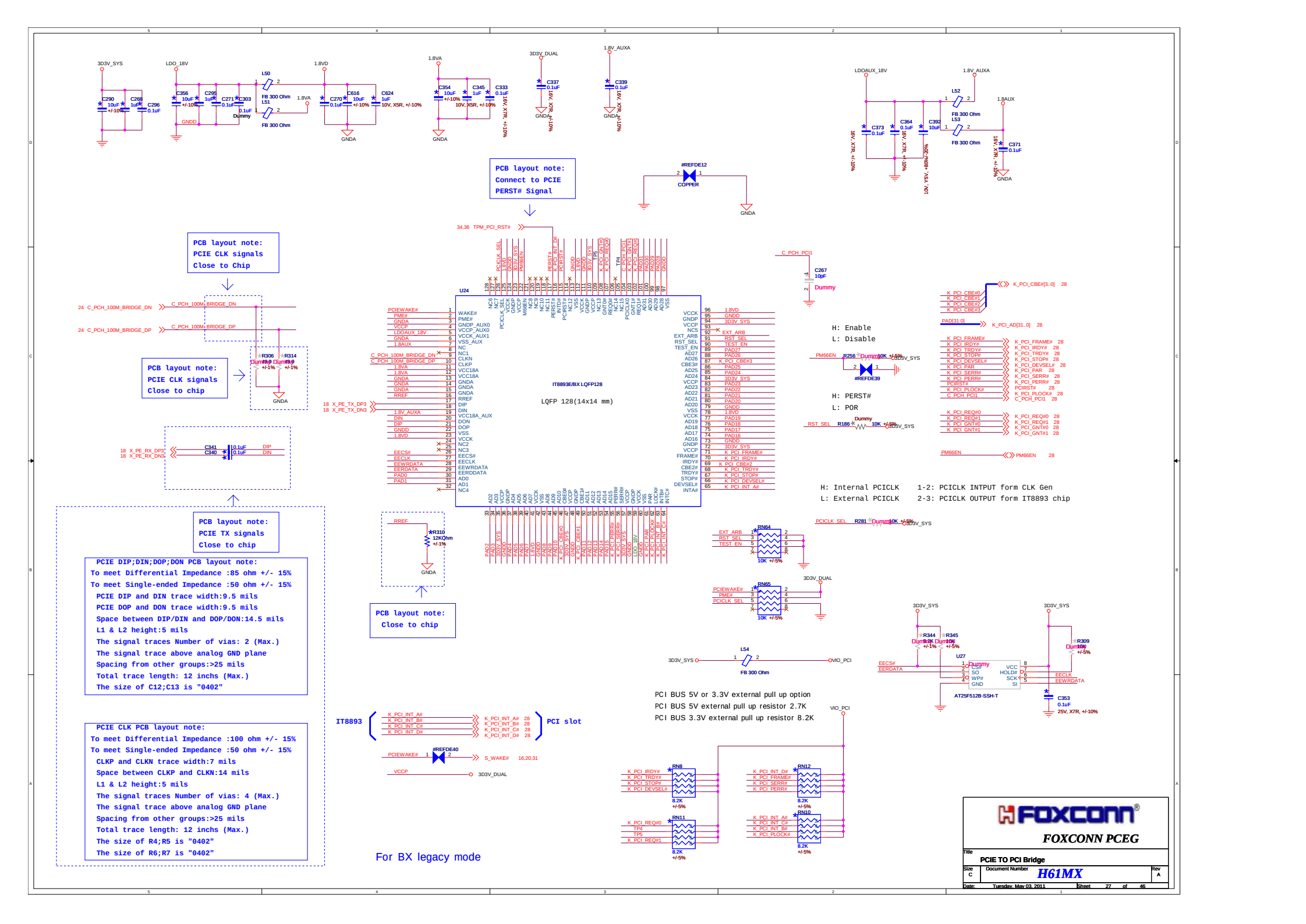
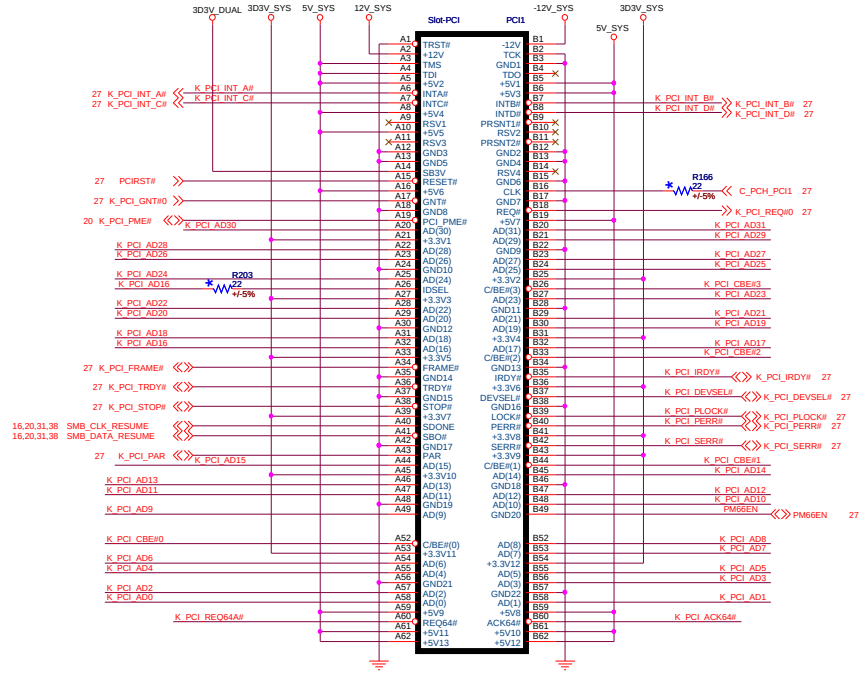
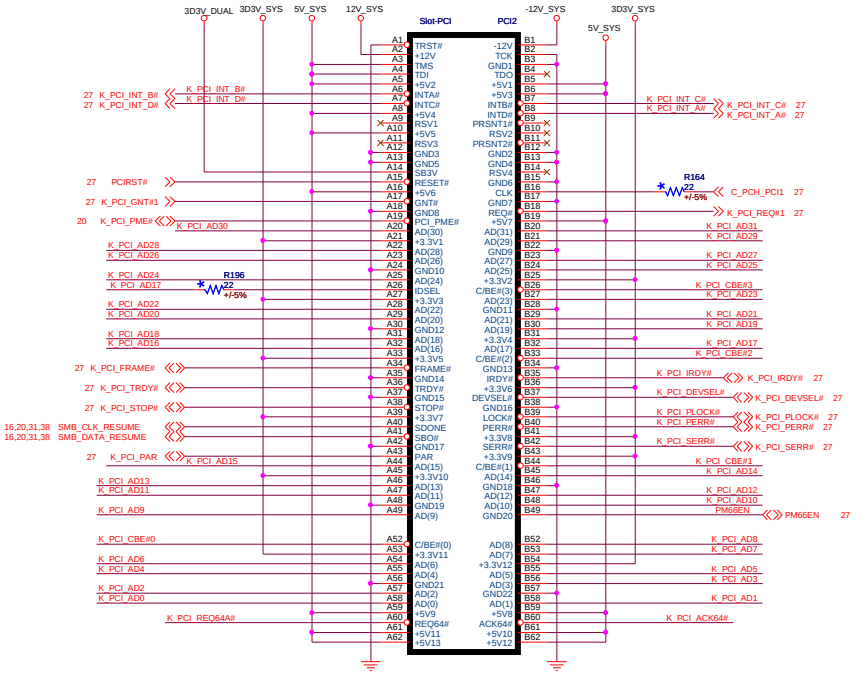

PCB layout note:
Connect to PCIE
PERST# Signal
PCB layout note:
PCIE CLK signals
Close to Chip
PCB layout note:
PCIE CLK signals
Close to chip
PCB layout note:
PCIE TX signals
Close to chip
PCB layout note:
Close to chip
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C12;C13 is "0402"
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
IT8893E/BX LQFP128
LQFP 128(14x14 mm)
H: Enable
L: Disable
H: PERST#
L: POR
H: Internal PCICLK
L: External PCICLK
1-2: PCICLK INTPUT form CLK Gen
2-3: PCICLK OUTPUT form IT8893 chip
PCI BUS 5V or 3.3V external pull up option
PCI BUS 5V external pull up resistor 2.7K
PCI BUS 3.3V external pull up resistor 8.2K
IT8893
PCI slot
For BX legacy mode
FOXCONN PCEG
PCIE TO PCI Bridge
H61MX

PCI 1



IRQ: A B C D
IDSEL: AD16
REQ/GNT: 0

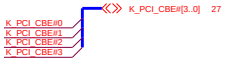
PCI 2

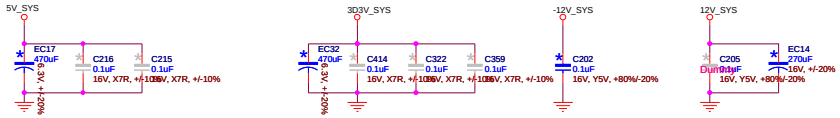


IRQ: B C D A
IDSEL: AD17
REQ/GNT: 1

PCI BUS if use 5V external pull up resistor is 2.7K

2010.6.22 update





FOXCONN PCEG		
Title: PCI SLOT1/2		
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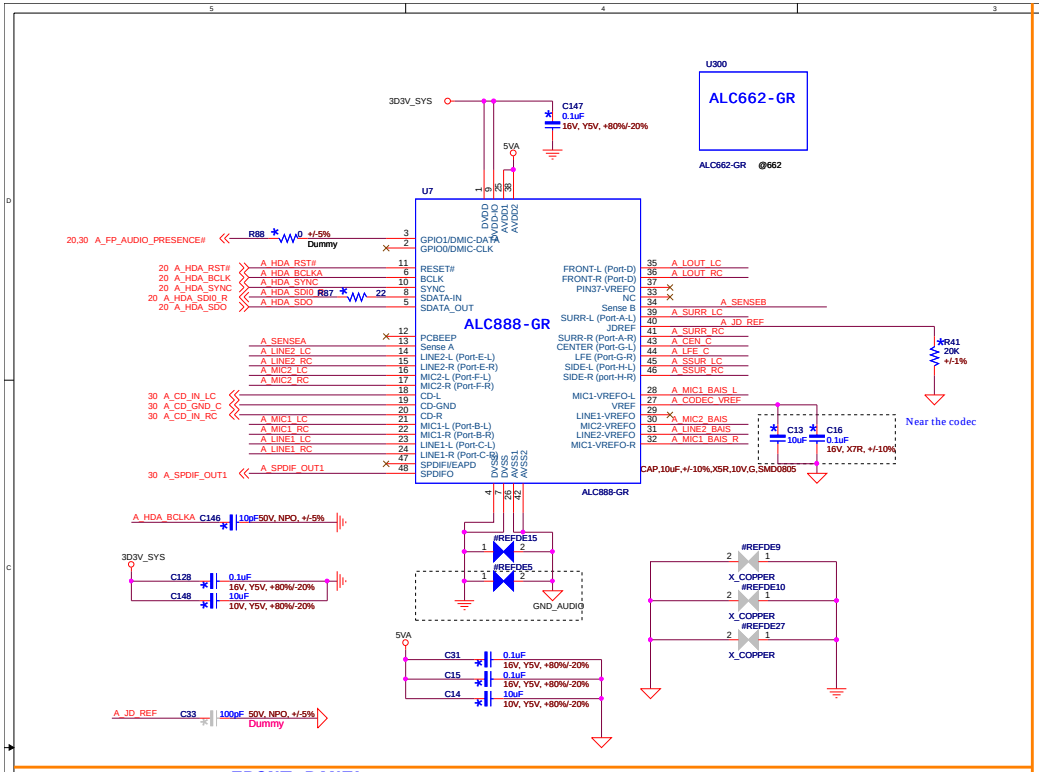

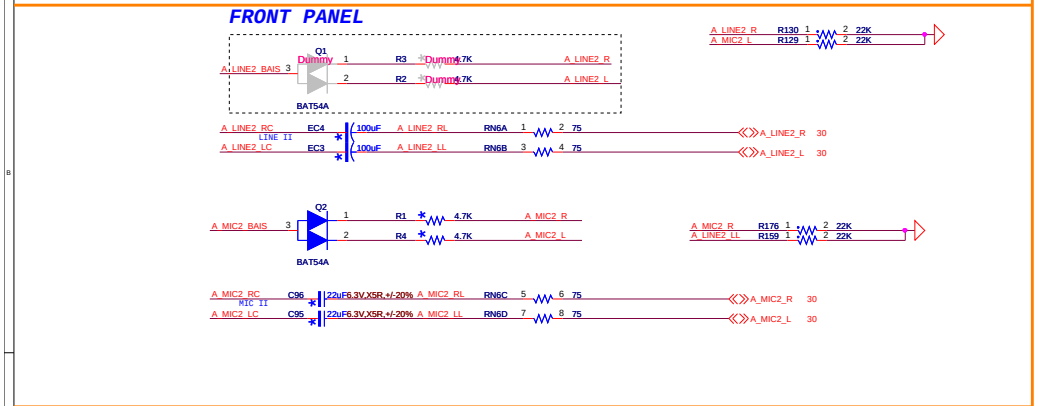

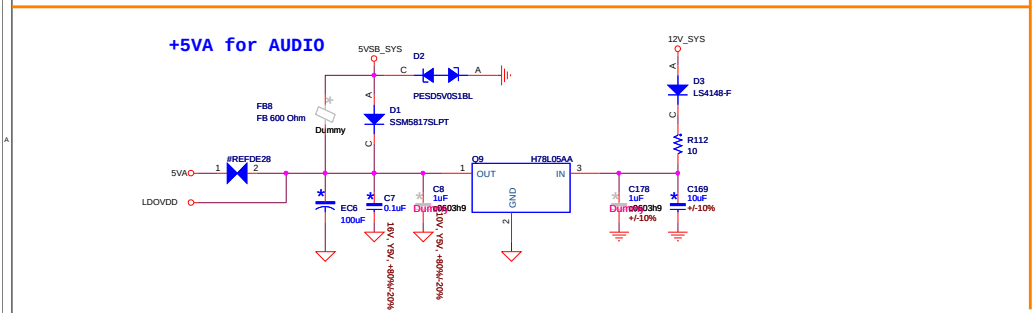

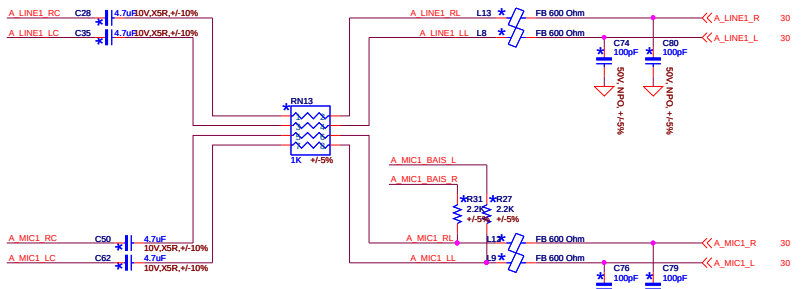

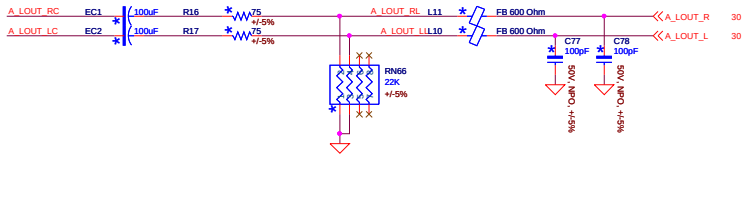

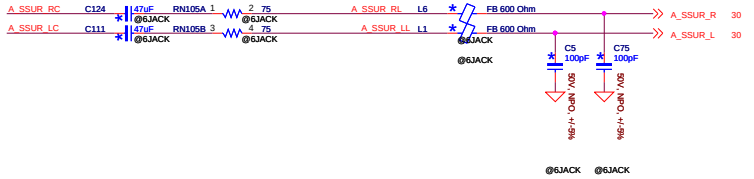

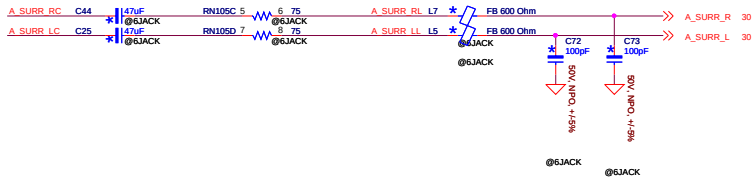

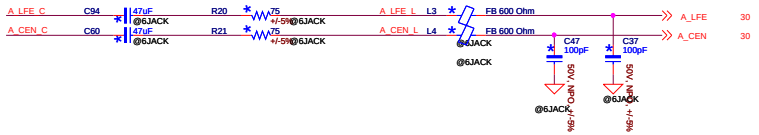

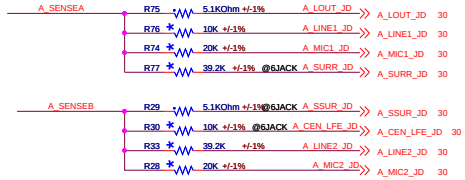

FOXCONN PCEG

Title: AUDIO_ALC888/ALC662

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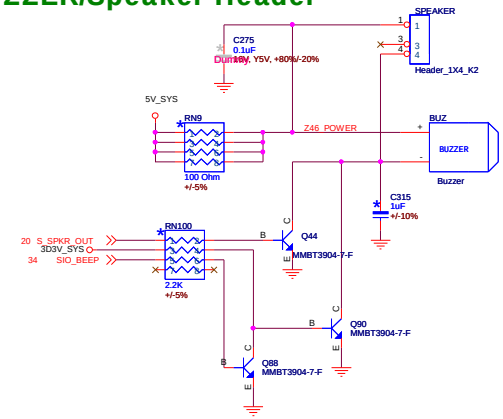
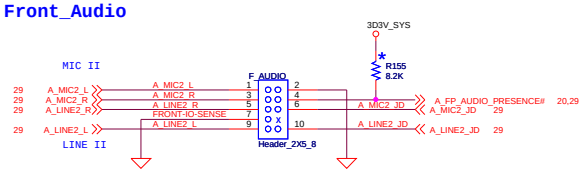
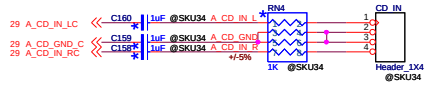
BUZZER/Speaker Header

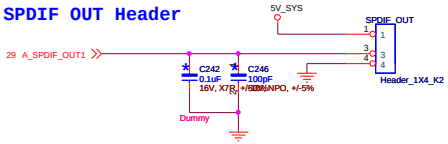


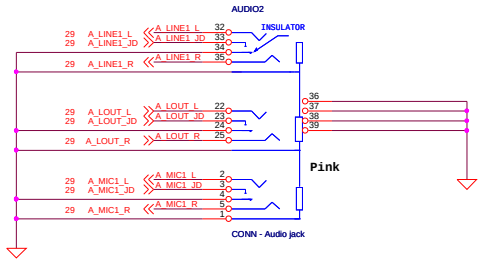
Front_Audio



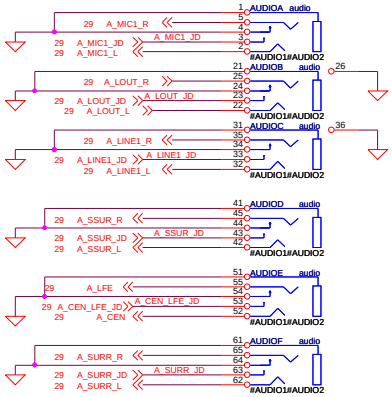


SPDIF OUT Header





Colay



AUDIO1

CONN-6 Ports Audio
@6JACK

Audio Jack

C	LINE IN (UAJ)	F	SURR OUT (UAJ)
B	LINE OUT (UAJ)	E	CEN/LFE (UAJ)
A	MIC IN (UAJ)	D	SIDE SURR OUT (UAJ)

FOXCONN

FOXCONN PCEG

Title: AUDIO CONN/SPDIF/CD-IN

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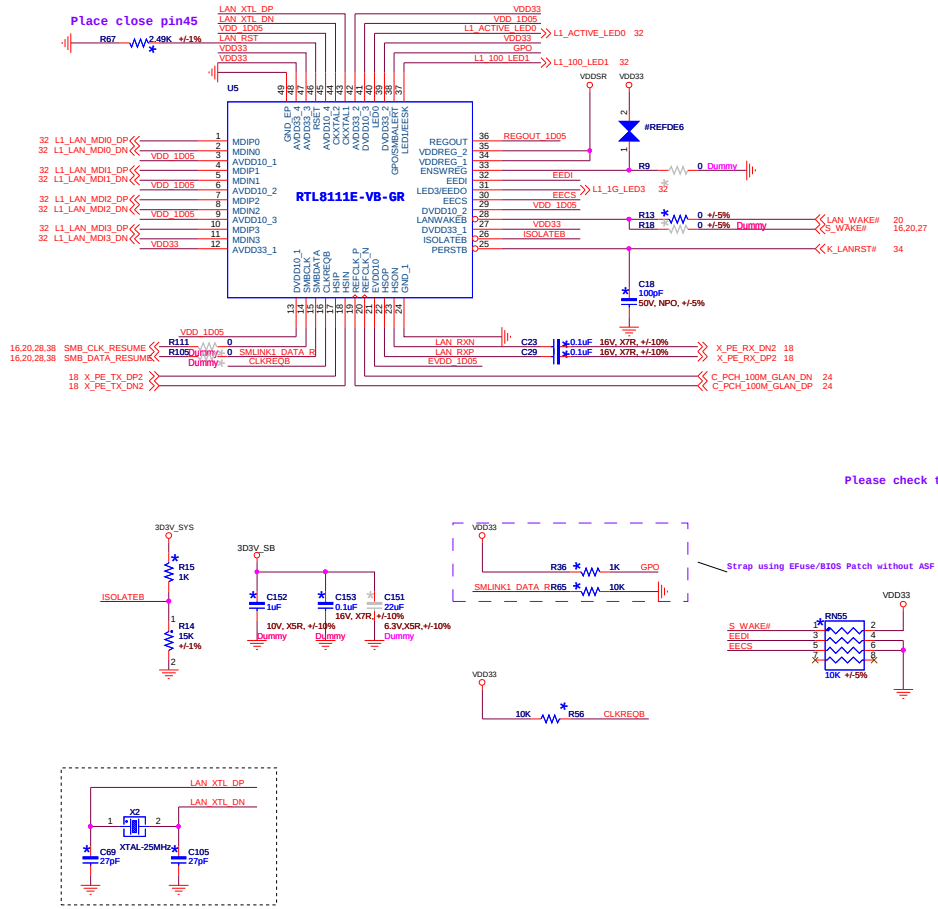

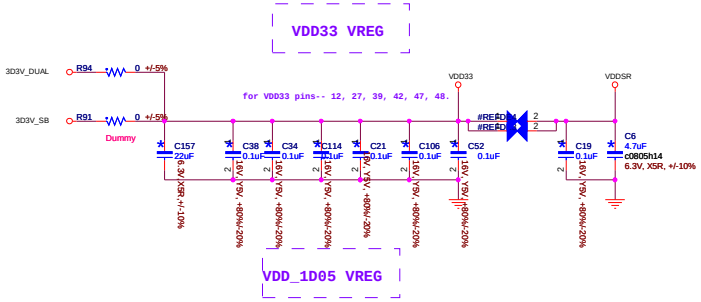

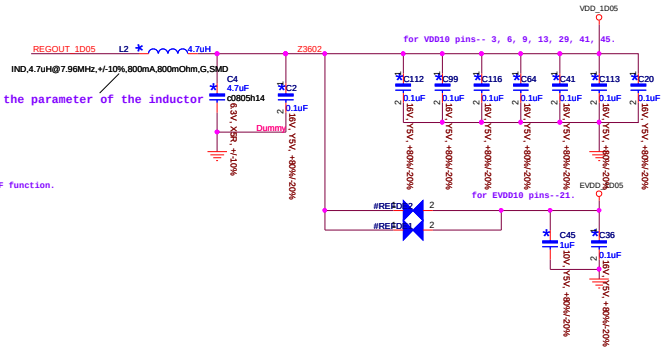

FOXCONN PCEG

Title	LAN_RTL8111E	
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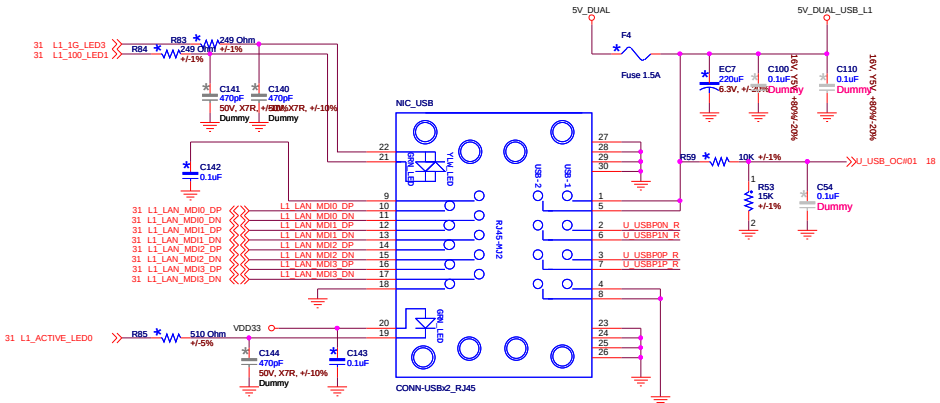

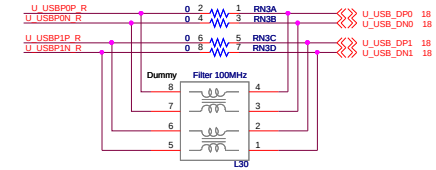

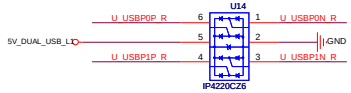

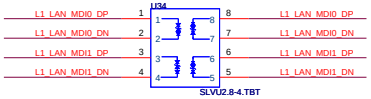

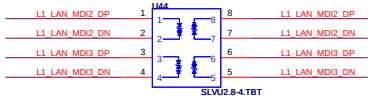

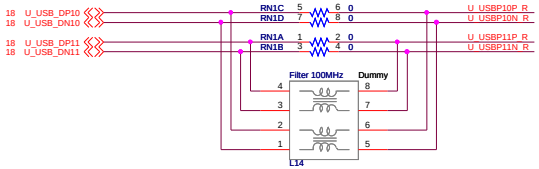

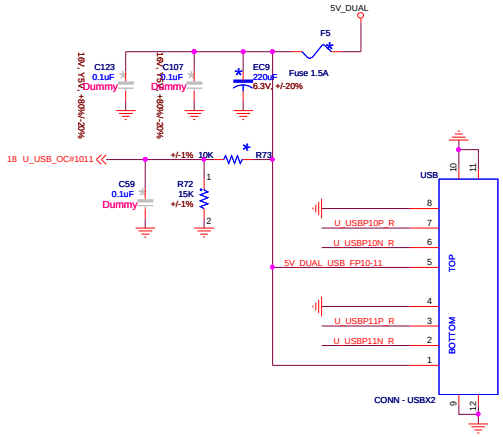

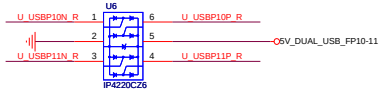

FOXCONN PCEG

Title	LAN/USB2.0 CONN	
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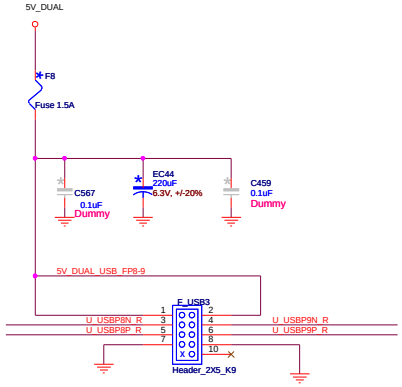
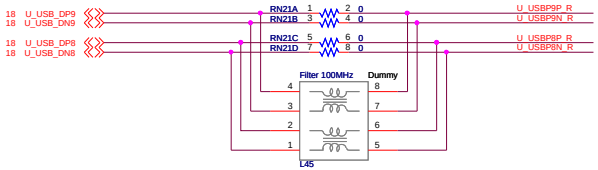
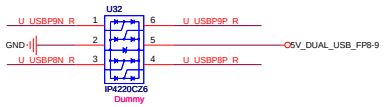
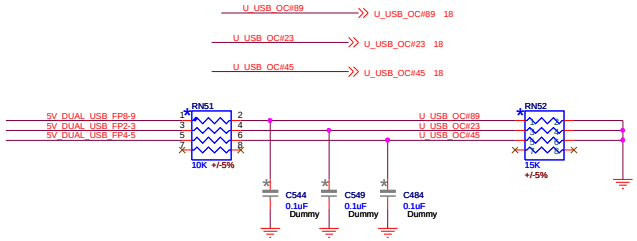
Front_USB1

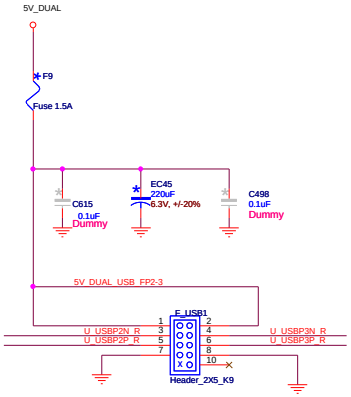


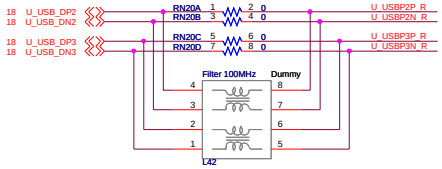


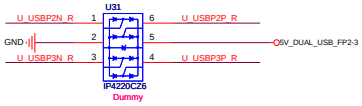


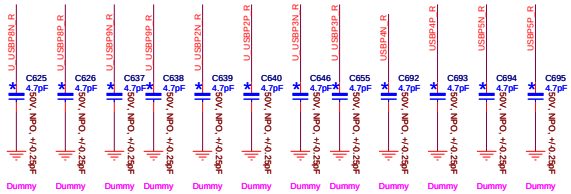


Front_USB2

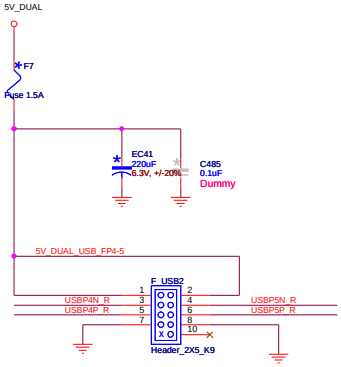


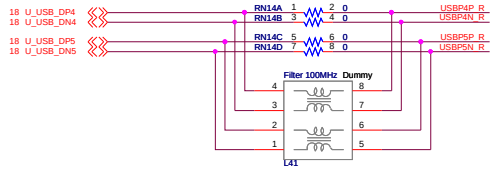


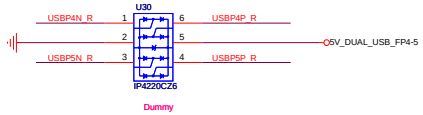




Front_USB3







FOXCONN PCEG

Title	Front USB2.0 Header	
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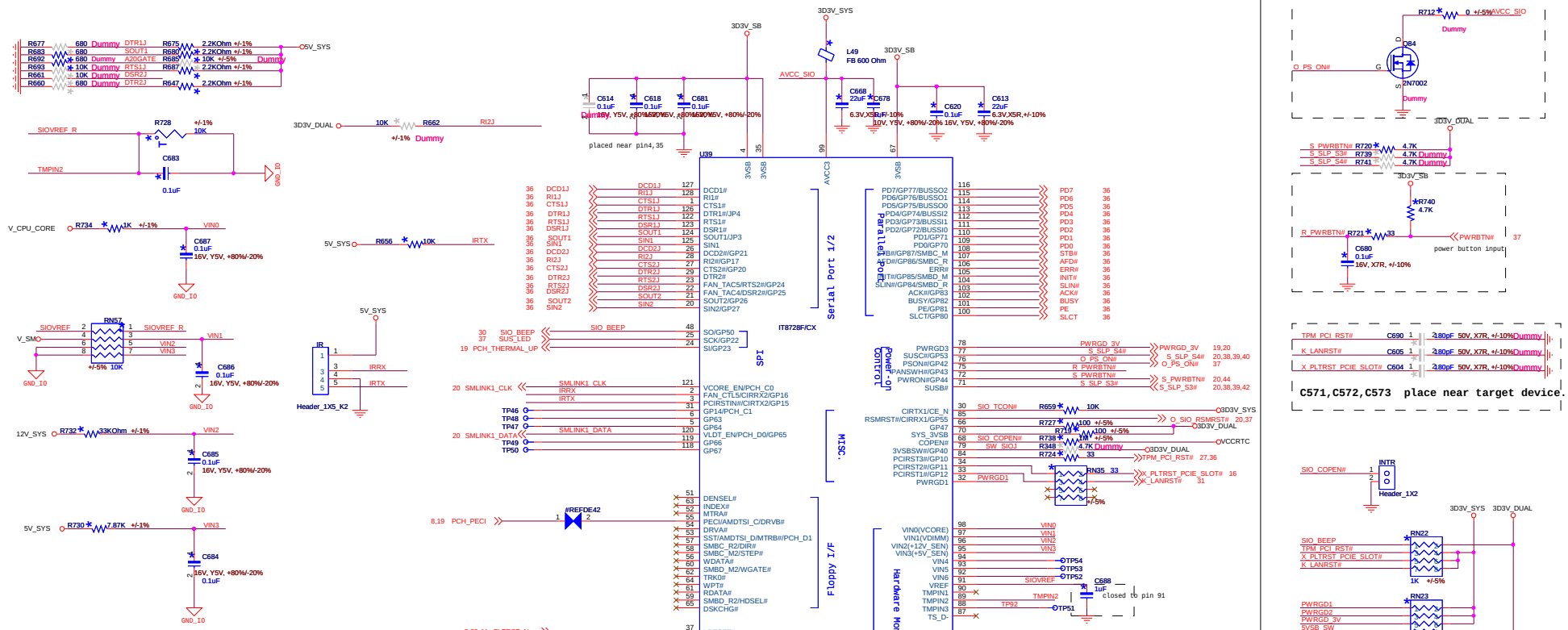
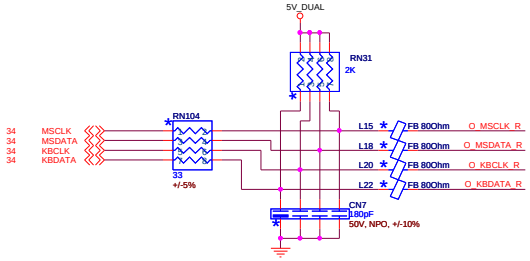


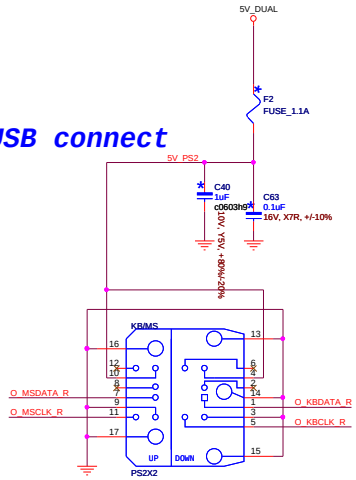
IT8728 Power On Strapping Options

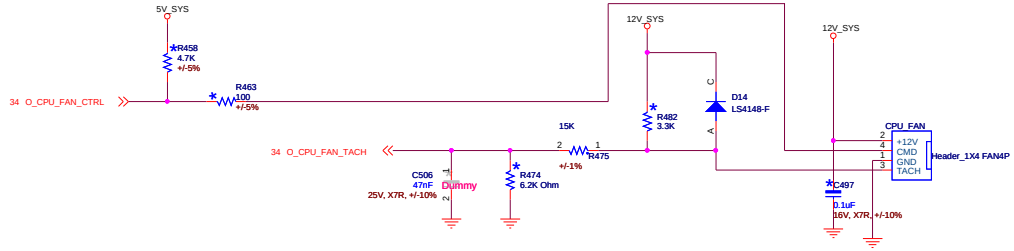
	Symbol	value	Description
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h

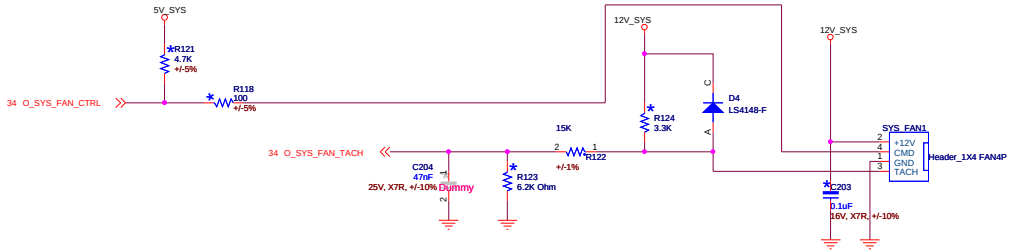
Add for EMI on 0929

KB /USB connect









FOXCONN PCEG

Title: PS2/FAN

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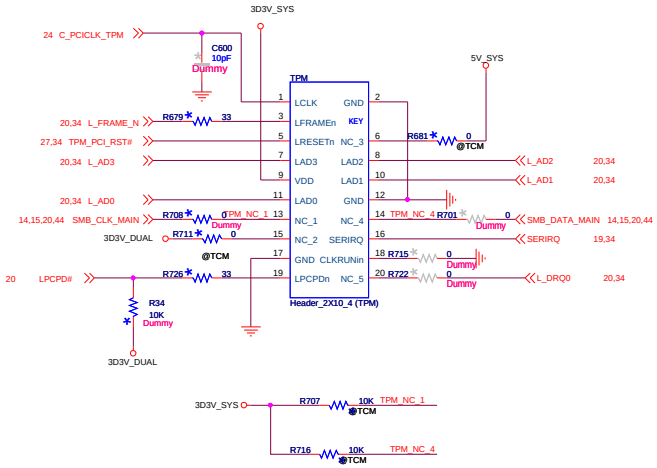
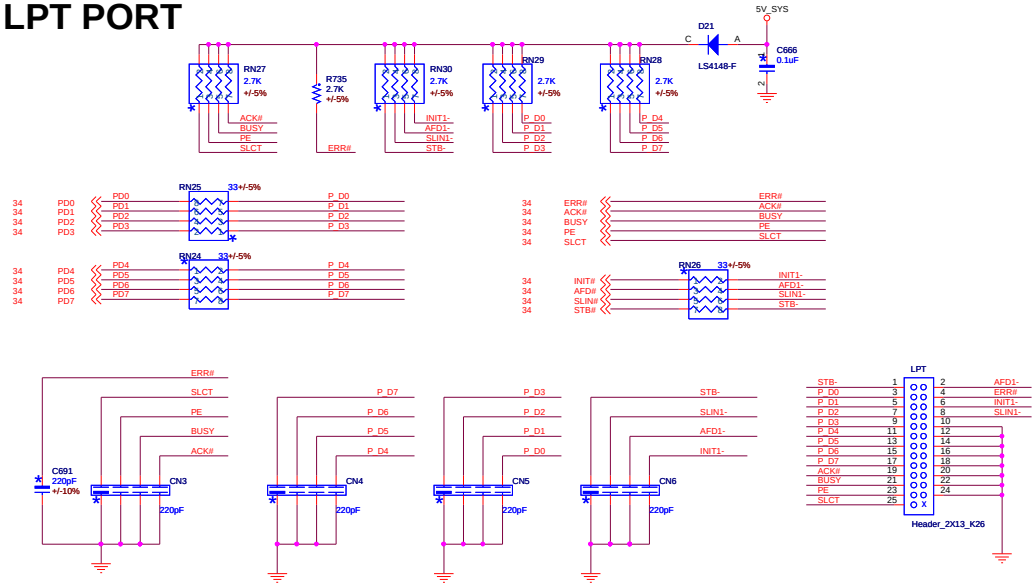
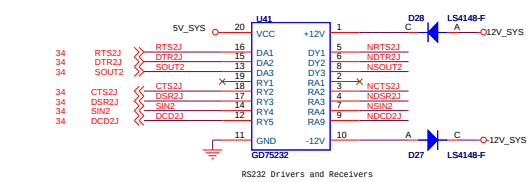
TPM

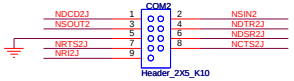


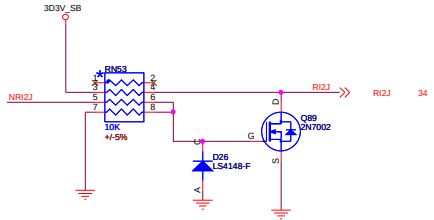
LPT PORT

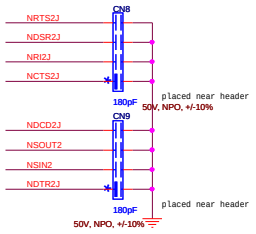


COM HEADER

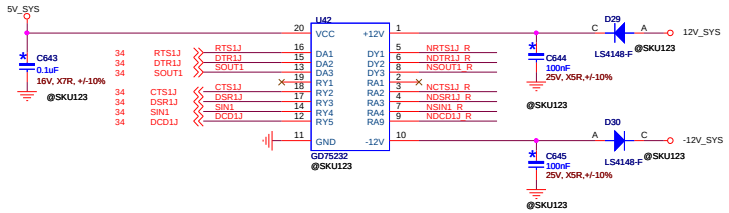


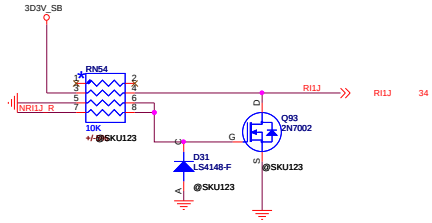


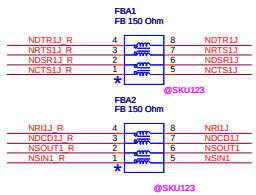


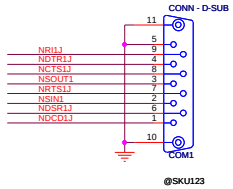


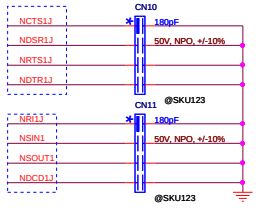
COM PORT











FOXCONN PCEG

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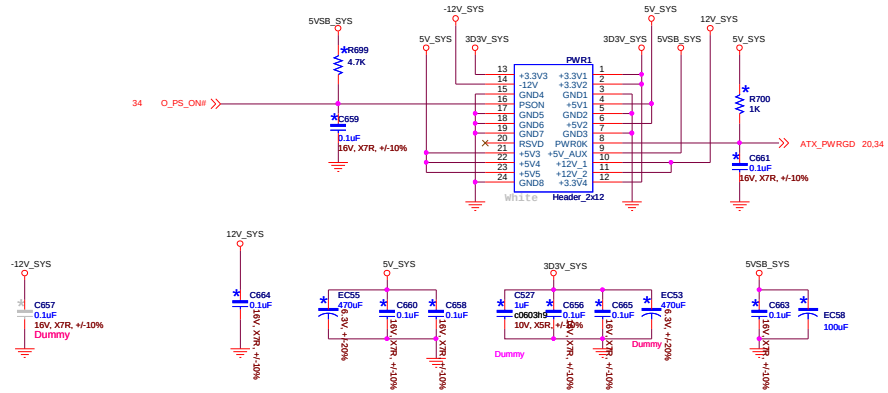
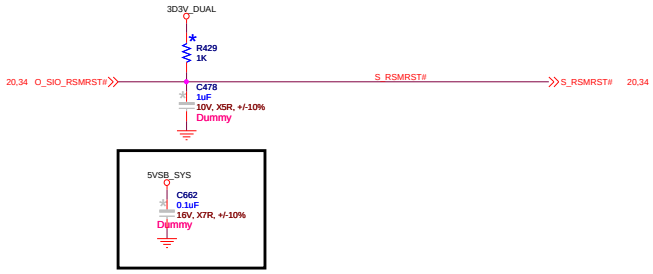
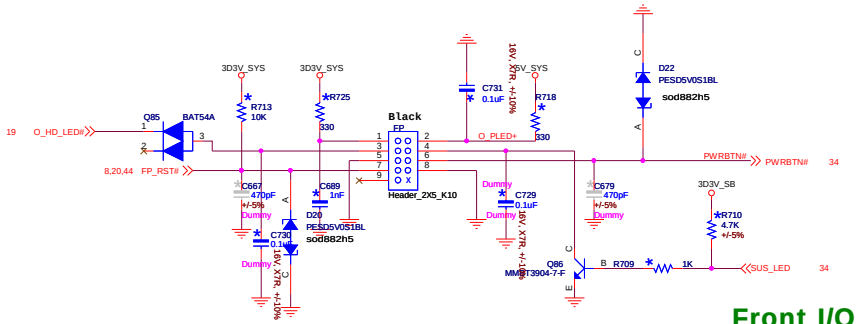
ATX POWER CONNECTOR



RESUME RESET LOGIC





S0 : Power LED is on;
S1 : Power LED is blinking;
S3~S5: Power LED is off.

Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Detect pin
Detect pin	9	10	Key

Front I/O Header

FOXCONN

FOXCONN PCEG

Title: ATX CONN/FP PANEL/RSMRST

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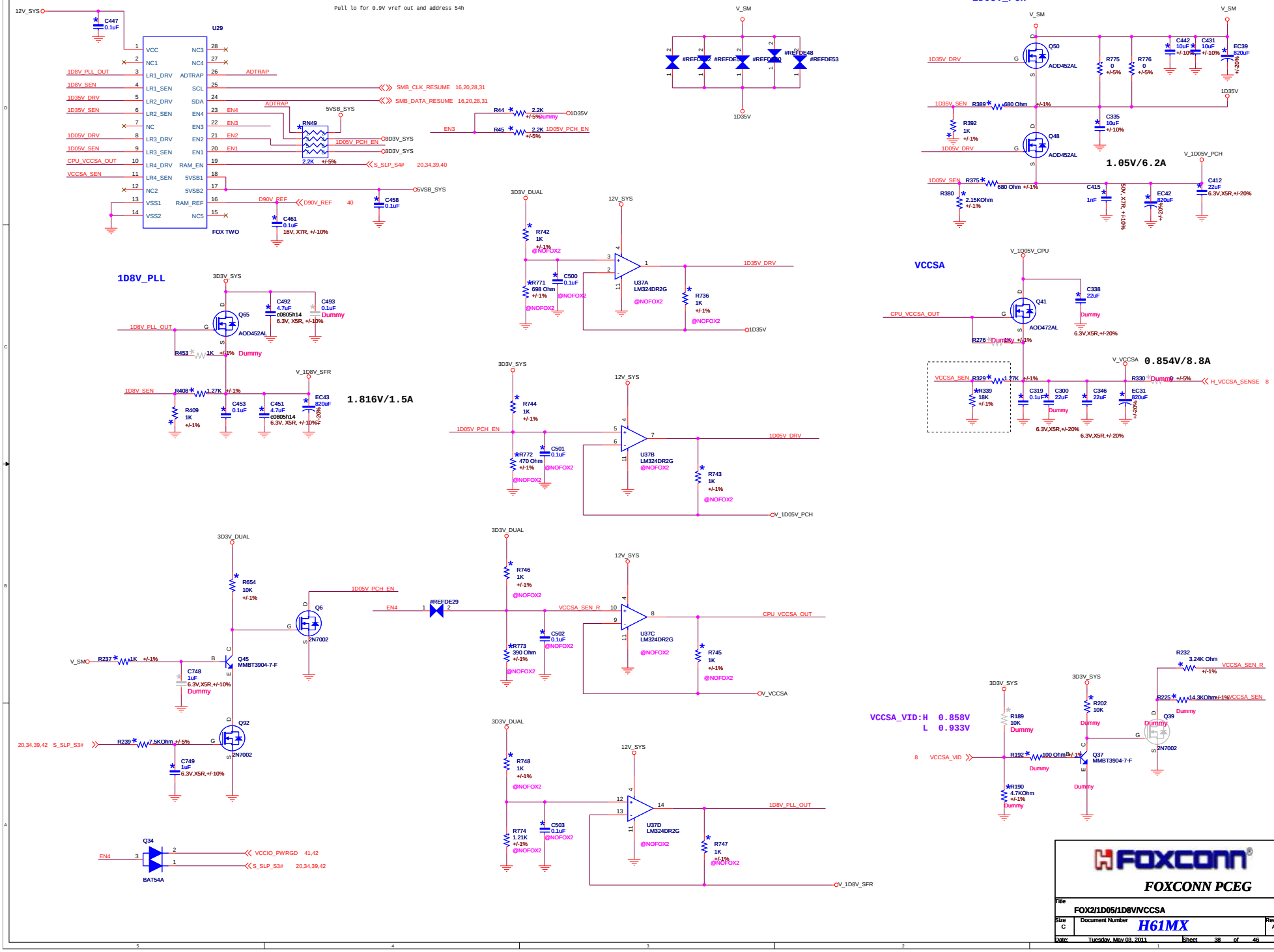
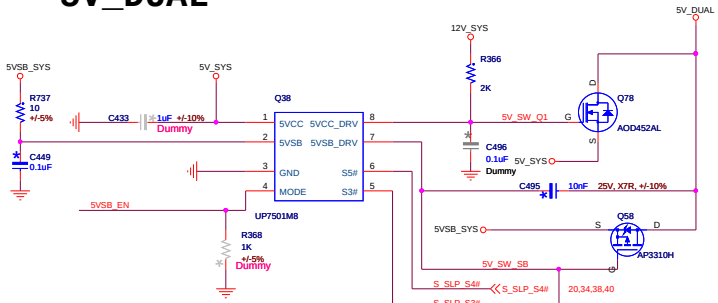
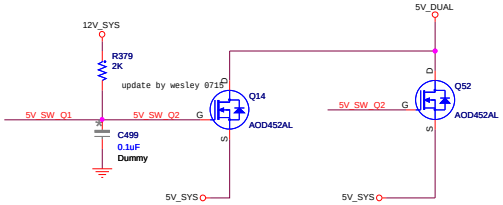

Pull lo for 0.9V vref out and address 54h
U29
FOX TWO
1D05V_PCH
1D8V_PLL
1.816V/1.5A
VCCSA
1.05V/6.2A
0.854V/8.8A
VCCSA_VID:H 0.858V
L 0.933V
FOXCONN PCEG
FOX2/1D05/1D8V/VCCSA
H61MX
Tuesday, May 03, 2011

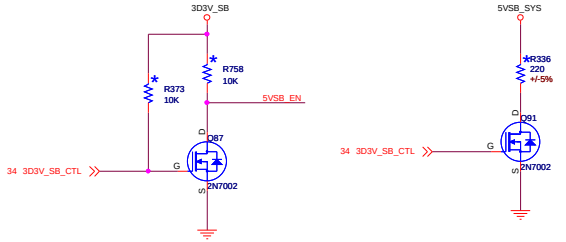
5V_DUAL





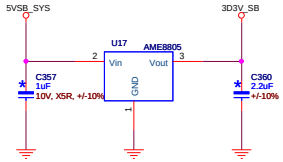
HI= S4/S5 5VDUAL FORM 5VSB
Low= S4/S5 5VDUAL TURN OFF

S5	S3	MODE	5VDUAL/5V_DUAL_USB
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

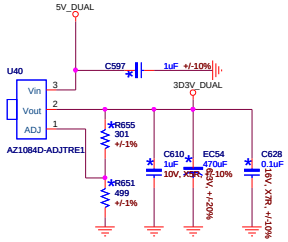


3D3V_SB

Max. output current = 3A



3D3V_DUAL



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

FOXCONN PCEG

Title	5V_DUAL/3.3V_SB/3.3V_DUAL	
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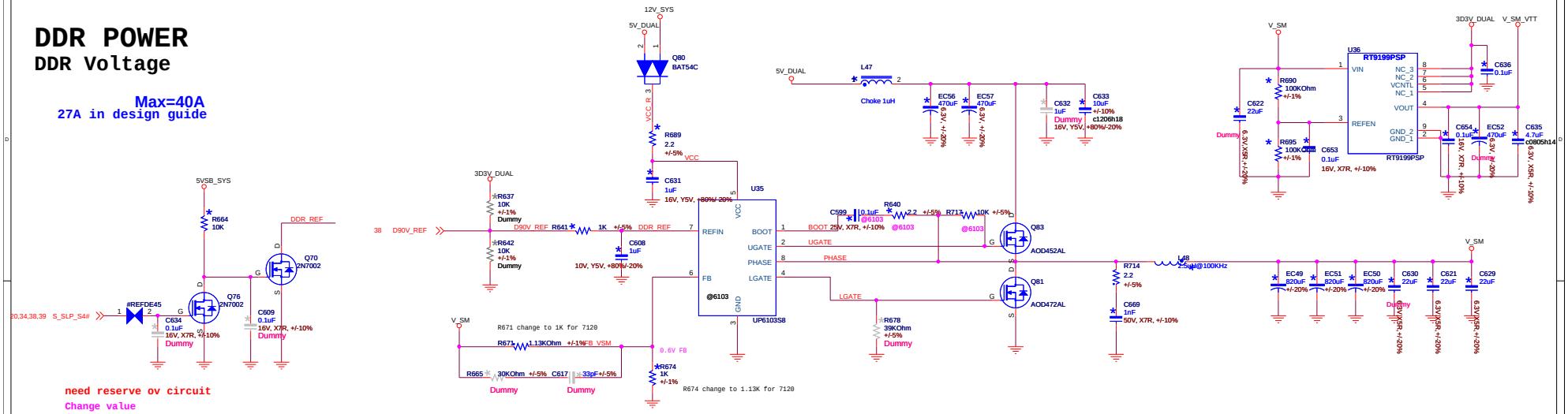
DDR POWER

DDR Voltage

Max=40A

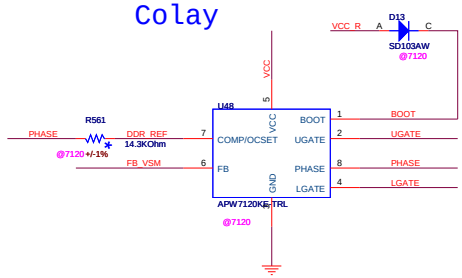
27A in design guide



need reserve ov circuit

Change value for 60A OCP

Colay



FOXCONN PCEG

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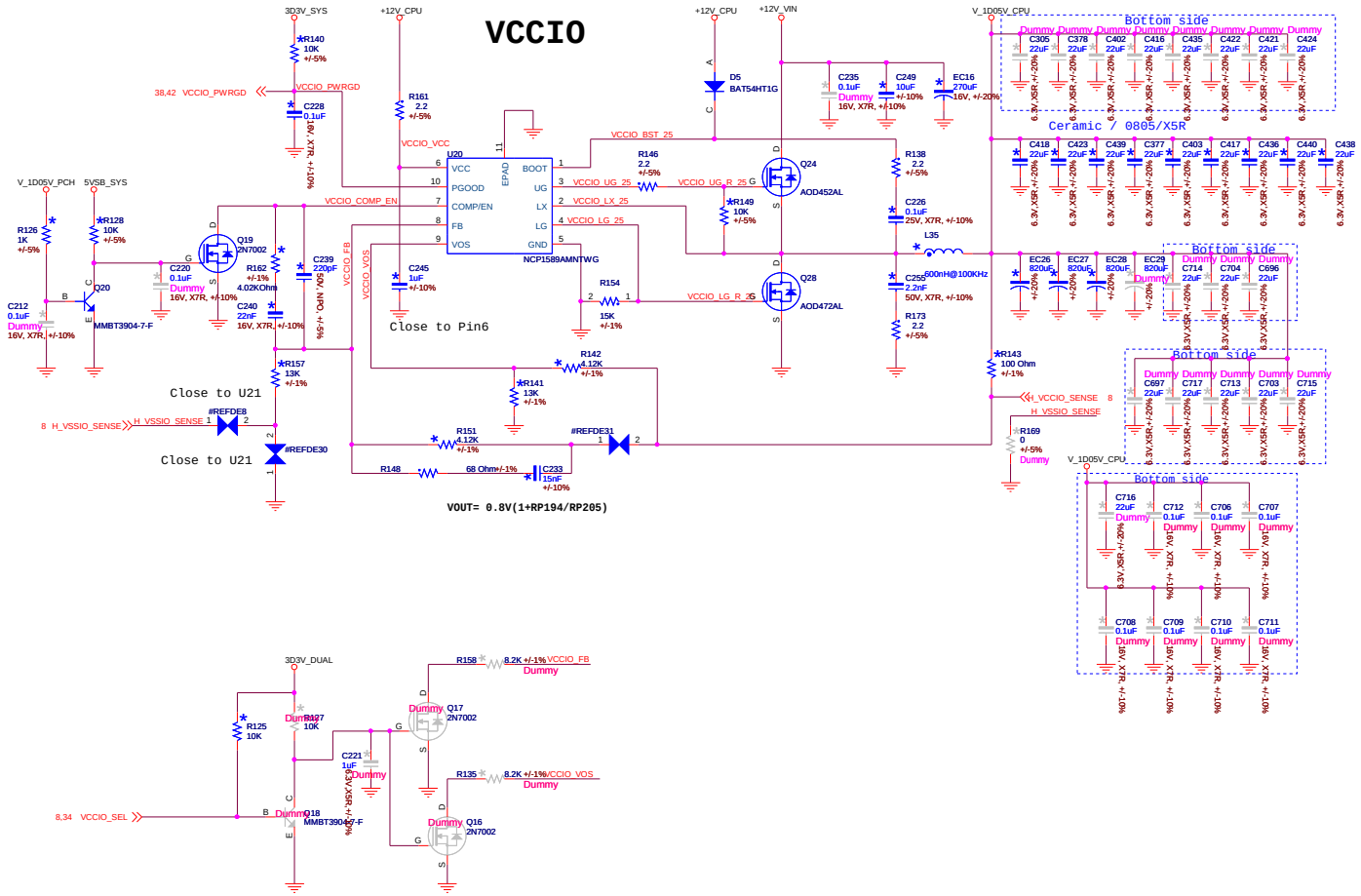
VCCIO

1.05V or 1.0V/17A MAX



FOXCONN PCEG

Title: CPU_VCCIO		
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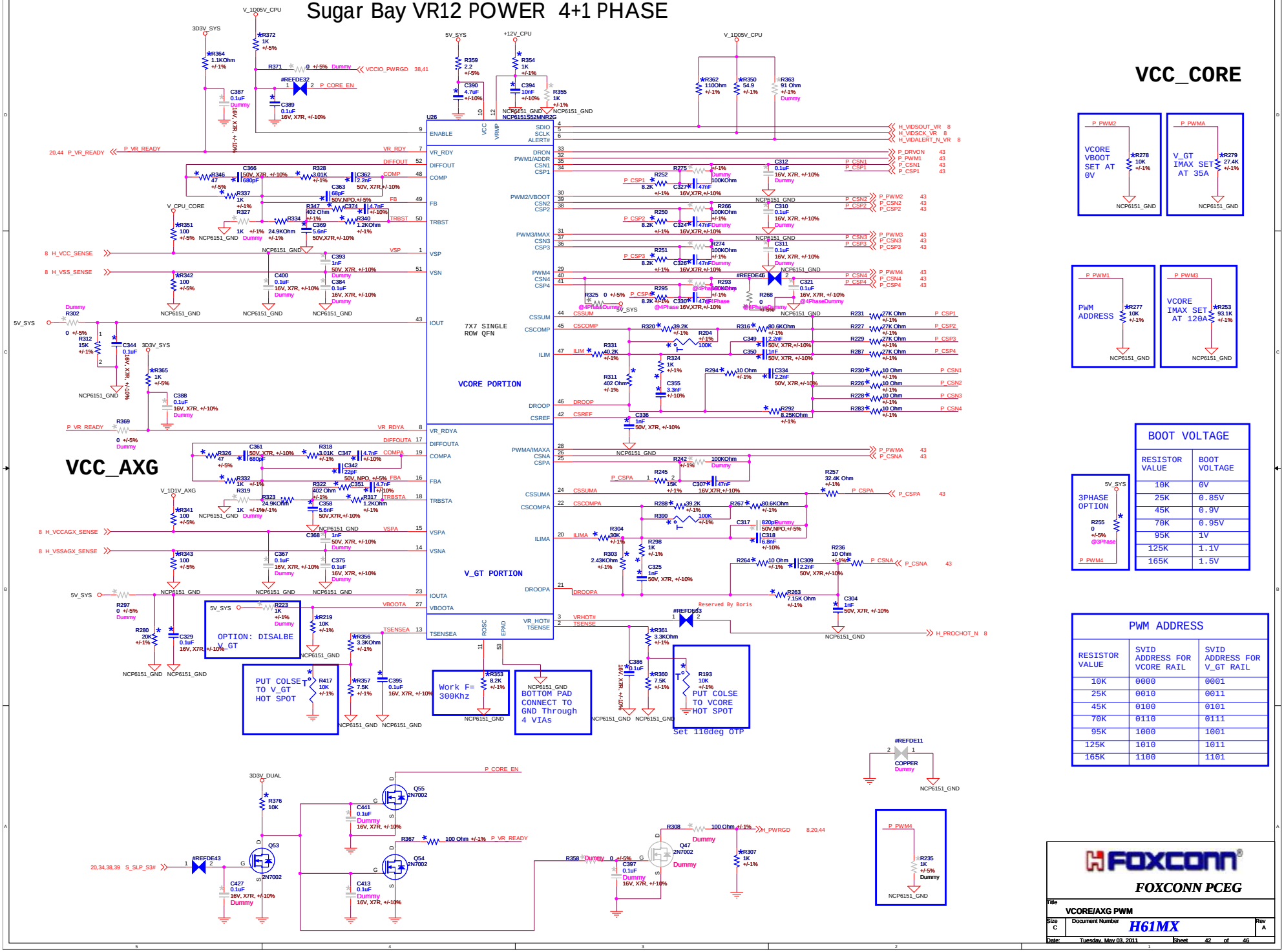
Sugar Bay VR12 POWER 4+1 PHASE



BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

FOXCONN PCEG

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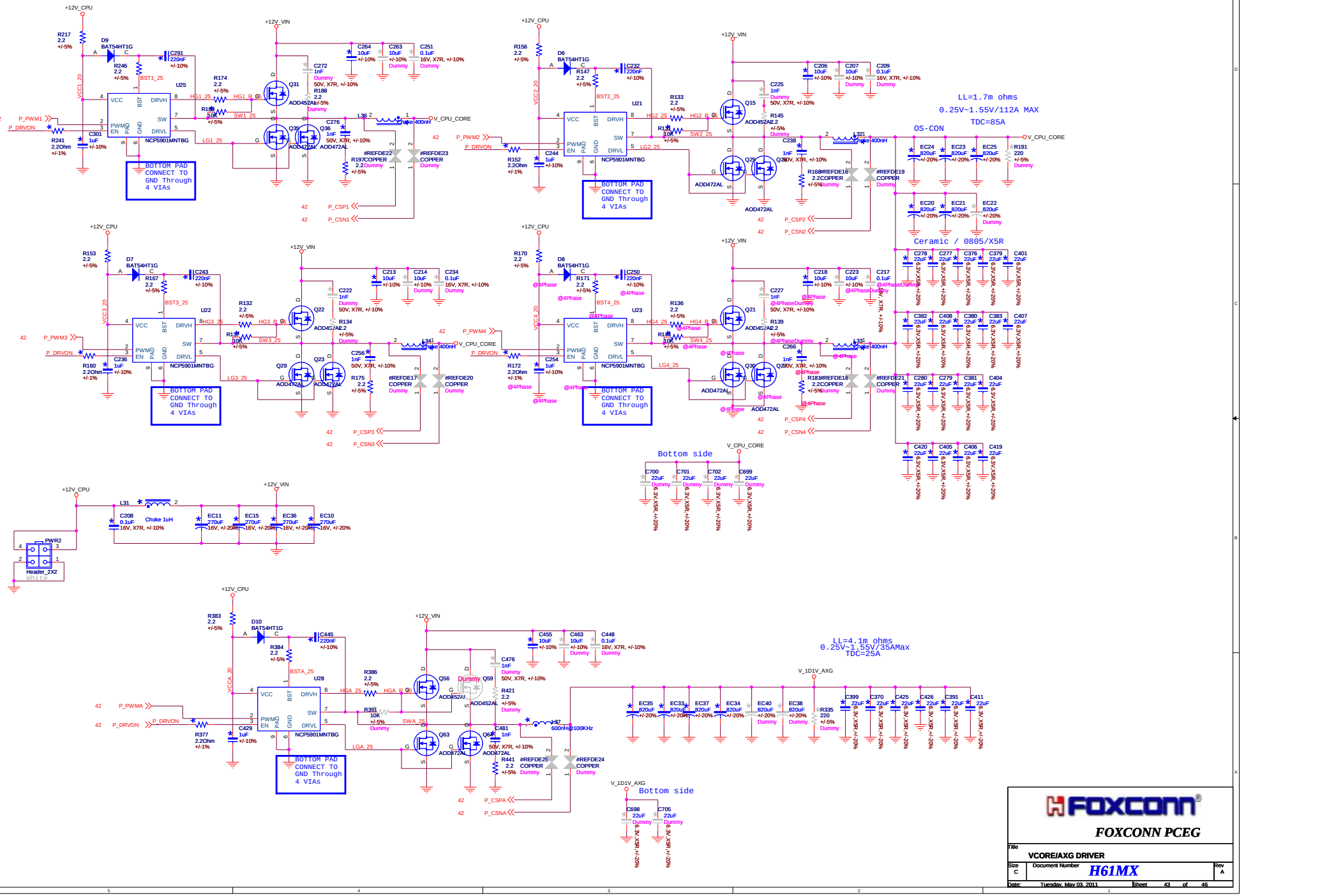

FOXCONN PCEG

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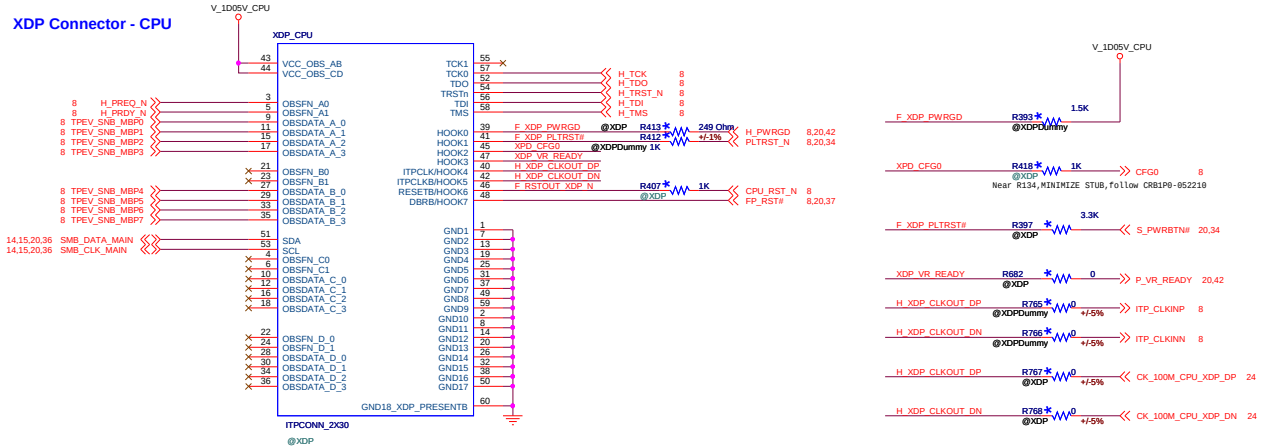
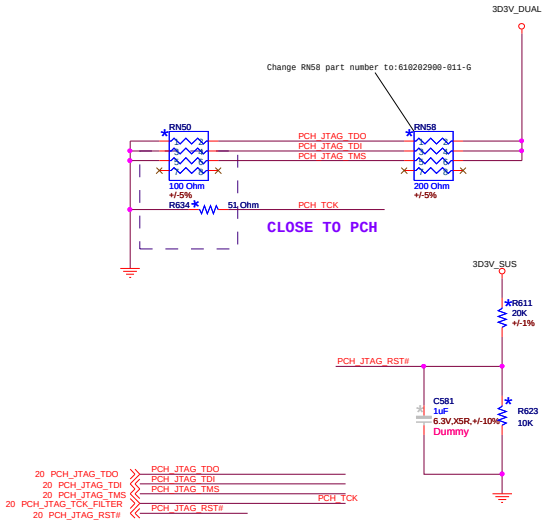
XDP Connector - CPU



XDP Connector - PCH



FOXCONN PCEG

Title: XDP		
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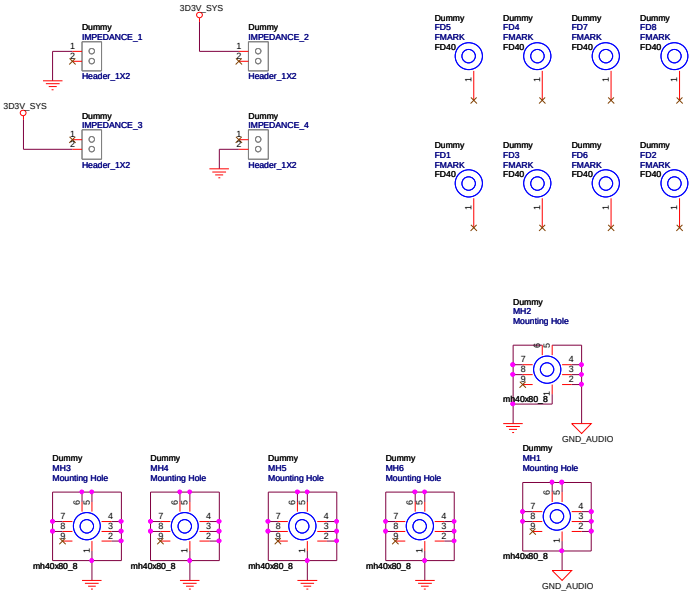

FOXCONN PCEG

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FOXCONN PCEG

Title: Changelist

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