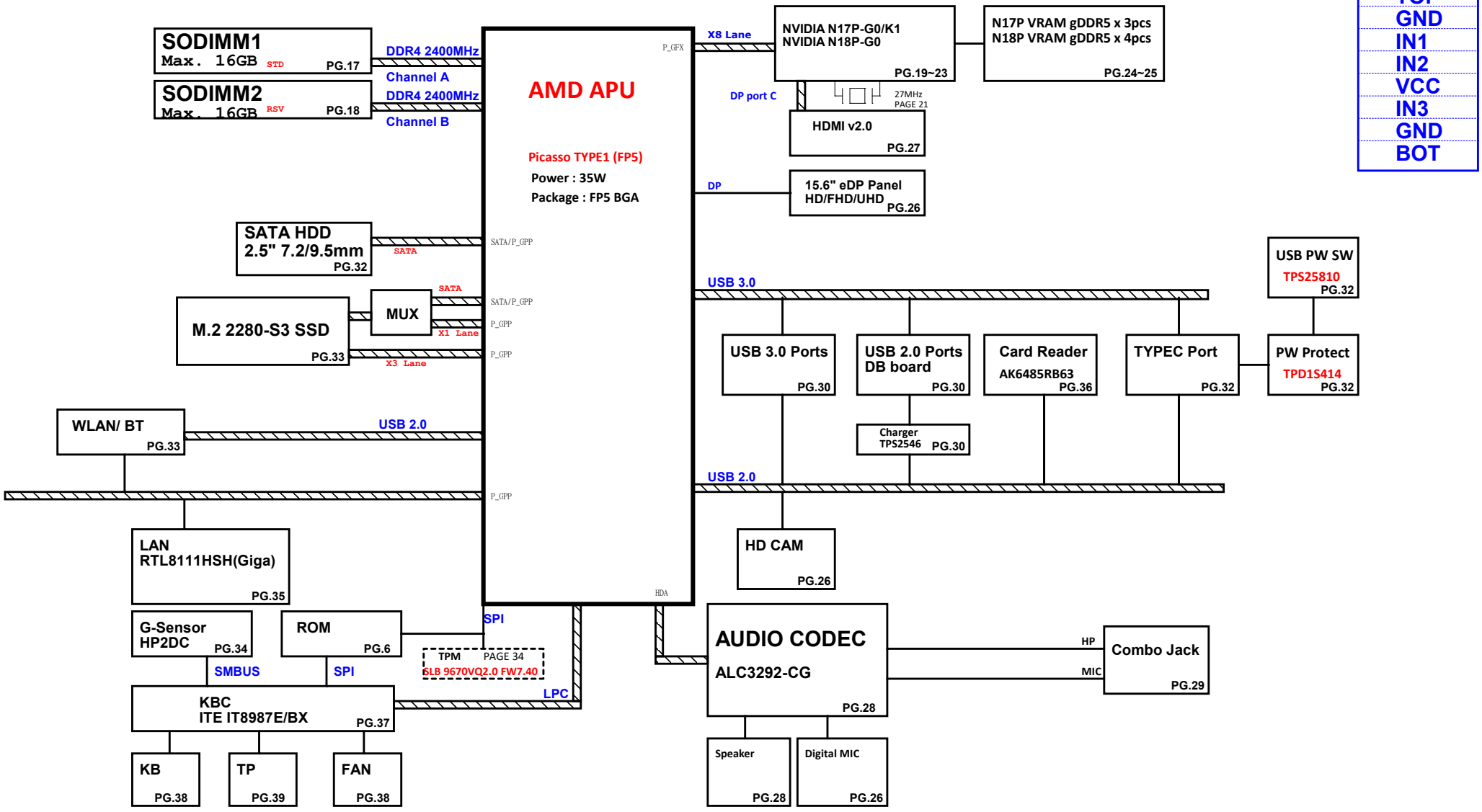
G3HA Picasso System Block Diagram

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



PROJECT : G3HA
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	Block Diagram	1A

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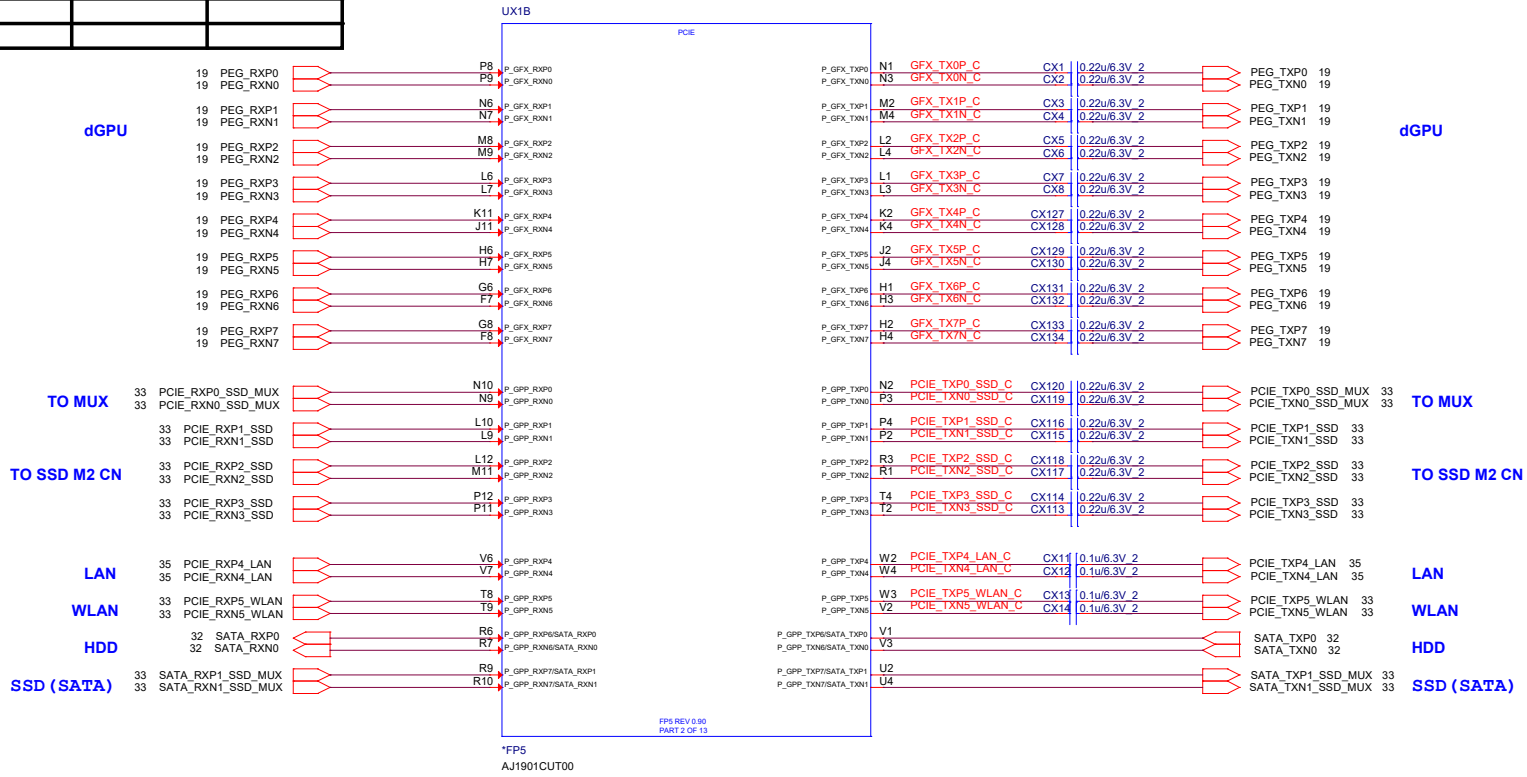
APU PCIE

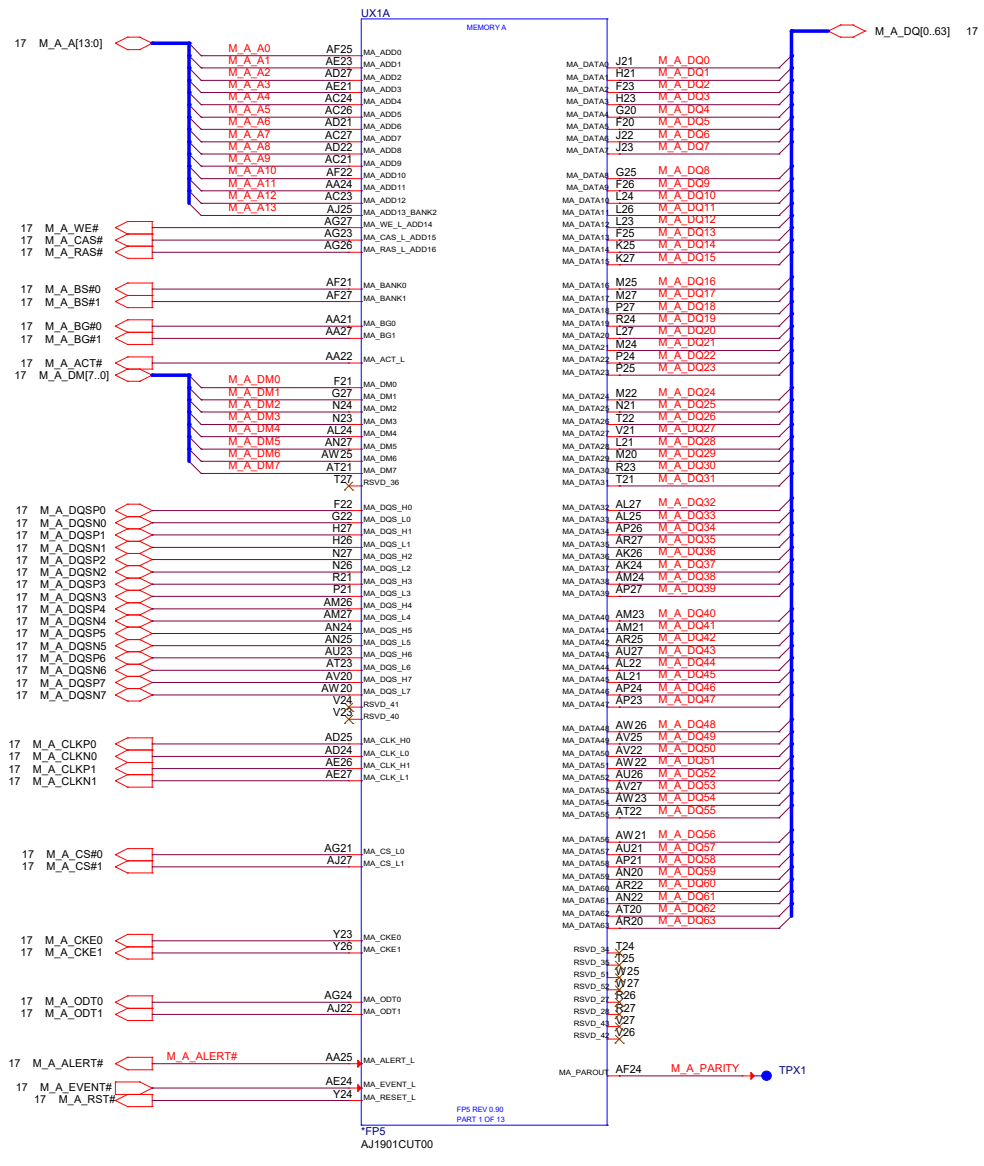
02

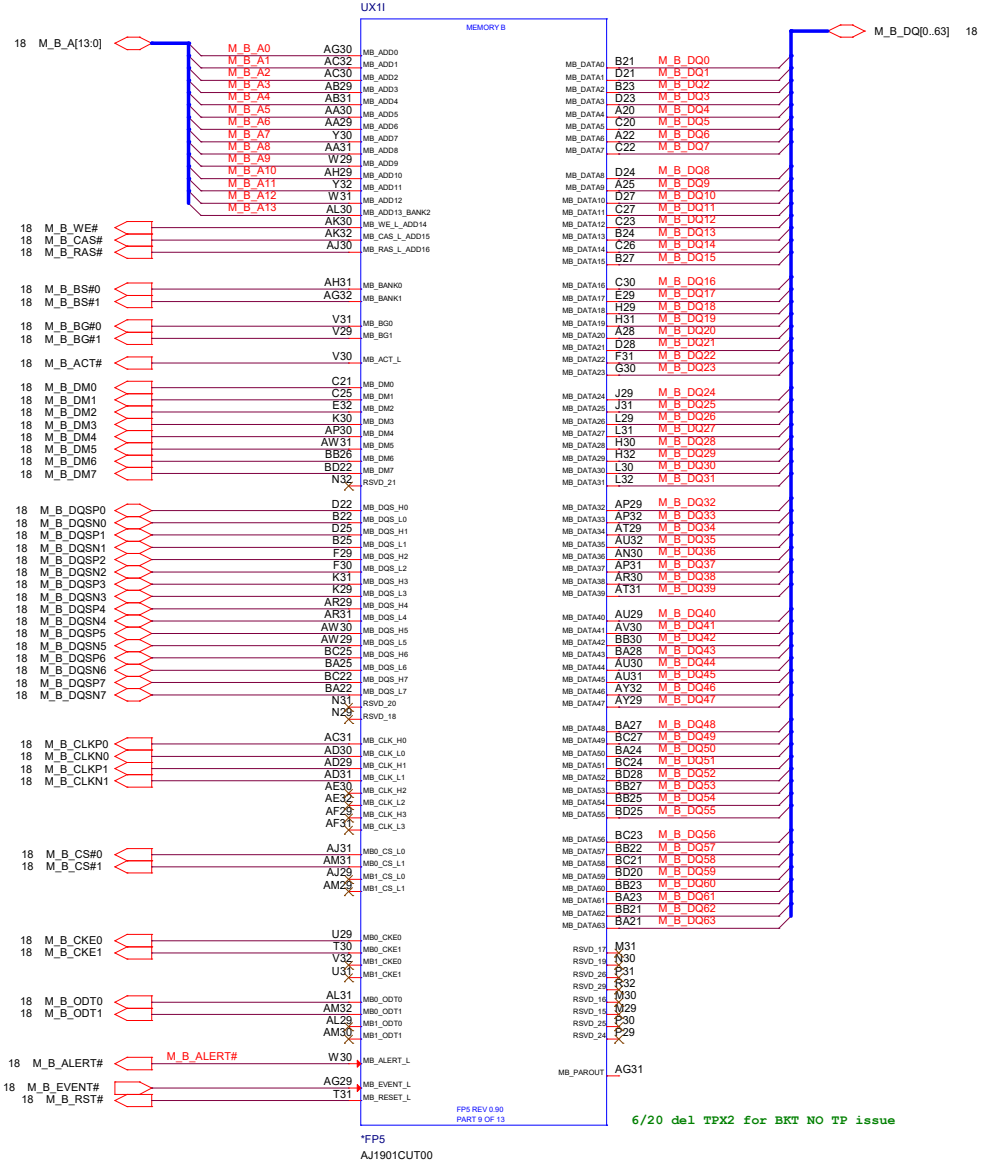
AMD APU	TOP BSQ	QBCON
Picasso R7-3700U	AJ03700UT01	
Picasso R5-3500U	AJ03500UT01	



APU MEMORY

03





6/20 del TPX2 for BKT NO TP issue

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APU DISPLAY and MISC

04

eDP Panel

26 INT_eDP_TXP0 / 26 INT_eDP_TXN0 → C8 DP0_TXP0 / A8 DP0_TXN0
26 INT_eDP_TXP1 / 26 INT_eDP_TXN1 → D8 DP0_TXP1 / B8 DP0_TXN1
26 INT_eDP_TXP2 / 26 INT_eDP_TXN2 → B6 DP0_TXP2 / C7 DP0_TXN2
26 INT_eDP_TXP3 / 26 INT_eDP_TXN3 → C6 DP0_TXP3 / D6 DP0_TXN3
E6 DP1_TXP0 / D5 DP1_TXN0
E1 DP1_TXP1 / C1 DP1_TXN1
F3 DP1_TXP2 / E4 DP1_TXN2
F4 DP1_TXP3 / F2 DP1_TXN3

UX1C
DISPLAY/SVI2/JTAG/TEST

G15 DP_BLON → APU_LVDS_BLON_R
F15 DP_DIGON → APU_DISP_ON_R
L14 DP_VARY_BL → APU_DPST_PWM_R

eDP

D9 DP0_AUXP → INT_eDP_AUXP 26
B9 DP0_AUXN → INT_eDP_AUXN 26
C10 DP0_HPD → CPU_EDP_HPD 26

G11 DP1_AUXP
F11 DP1_AUXN
G13 DP1_HPD → CPU_HDMI_HPD 27

2/21 : Del HDMI Signal , add HDMI / DP HPD

J12 DP2_AUXP
H12 DP2_AUXN
K13 DP2_HPD
CPU_HDMI_HPD RX3 100K_1%_2
CPU_EDP_HPD RX173 100K_1%_2
CPU_DP_HPD RX175 100K_1%_2

J10 DP3_AUXP
H10 DP3_AUXN
K8 DP3_HPD → CPU_DP_HPD → TPX33

3/18 : need check DP_HPD

K15 DP_STEREOSYNC → DP_STEREOSYNC RX5 1K_1%_2 / RX6 *1K_1%_2 → +1.8V

F14 RSVD_4
F12 RSVD_3
F10 RSVD_2

APU_TEST14 RX16 *10K_5%_2
APU_TEST15 RX17 *10K_5%_2
APU_TEST16 RX18 *10K_5%_2
APU_TEST17 RX19 *10K_5%_2
→ +1.8V

AP14 TEST4 APU_TEST4 → TPX3
AN14 TEST5 APU_TEST5 → TPX4
F13 TEST6
G18 TEST14 APU_TEST14
H19 TEST15 APU_TEST15
F18 TEST16 APU_TEST16
F19 TEST17 APU_TEST17
W24 TEST31 APU_TEST31 RX14 *1K_1%_2 / RX15 *0_5%_2 → +1.8V
AR11 TEST41 APU_TEST41 → TPX5
AJ21 TEST470 APU_TEST470 → TPX6
AK21 TEST471 APU_TEST471 → TPX7

V4 SMU_ZVDDP RX20 196_1%_4 → +0.95V
AW11 CORETYPE APU_CORETYPE RX21 *1K_5%_2 → +3VS5

AN11 VDDP_SENSE → VDDP_SENSE 44
J19 VDDCR_SOC_SENSE CPU_VDDNB_RUN_FB_H → CPU_VDDNB_RUN_FB_H 46
K18 VDDCR_SENSE CPU_VDD_RUN_FB_H → CPU_VDD0_RUN_FB_H 46

J18 VSS_SENSE_A
AM11 VSS_SENSE_B VSS_SENSEB → TPX9 → CPU_VDD0_RUN_FB_L 46

CPU_VDDNB_RUN_FB_H → TPX10
CPU_VDD_RUN_FB_H → TPX11

*FP5
AJ1901CUT00
FP5 REV 0.90
PART 3 OF 13

ESD mount

+1.8V
RX2 300_5%_2 APU_RST#
RX1 300_5%_2 APU_PWRGD
APU_RST#
APU_PWRGD
CX18 150p/50V_4
CX17 150p/50V_4

+3V
RX4 1K_5%_2 APU_ALERT#
RX7 1K_5%_2 APU_THERMTRIP#
RX8 1K_5%_2 APU_SIC
RX11 1K_5%_2 APU_SID

APU_TDI AU2 TDI
APU_TDO AU4 TDO
APU_TCK AU1 TCK
APU_TMS AU3 TMS
APU_TRST# AV3 TRST_L
APU_DBREQ# AW3 DBREQ_L

APU_RST# AW4 RESET_L
APU_PWRGD AW2 PWROK

APU_SIC H14 SIC DUAL
APU_SID J14 SID DUAL
APU_ALERT# J15 ALERT_L 3V
APU_THERMTRIP# AP16 THERMTRIP_L 3V
APU_PROCHOT#_R L19 PROCHOT_L 3V
37 APU_THERMTRIP#

SVC_APU F16 SVC0
SVD_APU H16 SVD0
SVT_APU J16 SVT0

6/11 modify follow CRB

+3V
R9660 4.7K_4
R9663 100K/F_4
PCH_DISP_ON → PCH_DISP_ON 26
DX2 RB500V-40 → PCIE_RST#
Q3001 2N7002K
APU_DISP_ON_R R3025 CZ@2.2K_4
Q3004 METR3904-G
R3028 100K/F_4

6,7,21,22,28,37,46,48 +1.8V
5,6,7,17,18,21,26,27,28,32,33,35,36,37,38,39,46,48,49,50,51,52,53 +3V
7,37,44 +0.95V
5,6,7,34,44,45,48,53 +1.8VS5
5,6,7,23,32,33,37,39,42,43,44,48,53,54 +3VS5

6/11 modify follow CRB

+3V
R9661 100K/F_4
R9662 2.2K_4
PCH_LVDS_BLON → PCH_LVDS_BLON 26
DX1 RB500V-40 → PCIE_RST# 5,19,33,35
Q3000 2N7002K
APU_LVDS_BLON_R R3023 2.2K_4
Q3002 METR3904-G
R3026 100K/F_4

6/11 modify follow CRB

+3V
R9664 1K_4
R9665 100K/F_4
10/08: SI , change to 1K for LG Panel PWM
PCH_DPST_PWM → PCH_DPST_PWM 26
Q9046 2N7002K
APU_DPST_PWM_R R9666 CZ@2.2K_4
Q9047 METR3904-G
R9667 100K/F_4

5/7 remove R22/R23 for +3V leakage

+3V
RX22 *2.2K_5%
RX23 *2.2K_5%_2
6,37 MBCLK1
6,37 MBDATA1
+1.8V
QX2B DMN5L06DWK-7
QX2A DMN5L06DWK-7
APU_SIC
APU_SID

+3V
RX13 1K_1%_2
APU_PROCHOT#_R

APU Serial VID

+1.8V
RX24 1K_1%_2
RX25 1K_1%_2
RX26 1K_1%_2
SVT_APU RX29 *Short_0201 → CPU_SVT 46
SVC_APU RX30 *Short_0201 → CPU_SVC 46
SVD_APU RX31 *Short_0201 → CPU_SVD 46
APU_PWRGD RX32 *Short_0201 → CPU_PWRGD_SVID_REG 46
RX33 *220_5%_2
RX34 *220_5%_2
RX35 *220_5%_2

HDT+ Connector for Debug only

Can remove on MP

+3V
CX125 *0.1u/6.3V_2
CPU_LDT_RST_HTPA# 4
APU_RST# 1
UX4 TC7SH08FU(F)

Close to HDT & No remove.
+1.8VS5
APU_TDI 1K_1%_2 RX154
APU_TCK 1K_1%_2 RX155
APU_TMS 1K_1%_2 RX156
APU_TRST# 1K_1%_2 RX157
APU_DBREQ# 1K_1%_2 RX158

1214:modify to +1.8VS5 for FP5 SCL

5/9 stuff HDT for AMD debug

+1.8VS5
TPX20 APU_TEST18_TP
TPX21 APU_TEST19_TP
APU_RST_L_BUF
TPX22 CPU_LDT_RST_HTPA#
TPX23 APU_DBREQ#
APU_DBRDY
APU_TCK
APU_TMS
APU_TDI
APU_TRST#
APU_TDO
APU_PWROK_BUF

HDT None-CIS
20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 21 1 22
HDT CONN 88511-2001-20p-l

UX5 74LVC2G07GW
APU_RST# 1 A1
APU_PWRGD 3 A2
GND 2
VCC 5
Y1 6
Y2 4
CX126 *0.1u/6.3V_2
+3V
APU_RST_L_BUF
APU_PWROK_BUF
1K_1%_2 RX152
1K_1%_2 RX153
+1.8V

	PN
EU (V1)	DFFC20FR255
EP (V1)	DFFC20FR031

Boot-VID code

SVC	SVD	VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

EC H_PROCHOT#

46 VRHOT → RX119 *Short_0201
37,53,55 H_PROCHOT# → RX120 *Short_0201 → APU_PROCHOT#_R
CX123 220p/25V_2

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APU GPIO/AZ/UART

05

HDA INTERFACE

RSMRST_GATE# from EC

PWRGD CIRCUIT

SPI TPM Need install RX149/RX168

Note: If TPM in on a S0 rail, disable the integrated pull-up and populate an external pull-up resistor to VDD_18_S0 rail.

1213:change VGA_RSTB for VGA sequence

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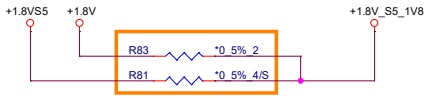
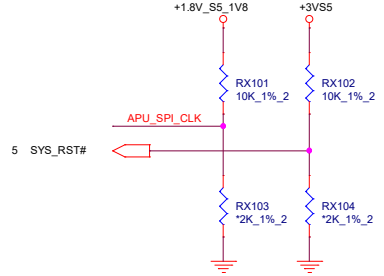
USB2 Port	Function
USB0/0	TYPE-C
USB0/1	TYPE-A
USB0/2	TYPE-A
USB0/3	BT
USB1/0	Camera
USB1/1	CARD READER

STRAPS PINS



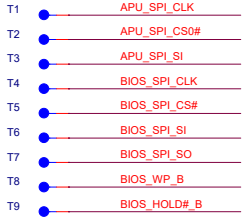
0130:correct power rail to S5

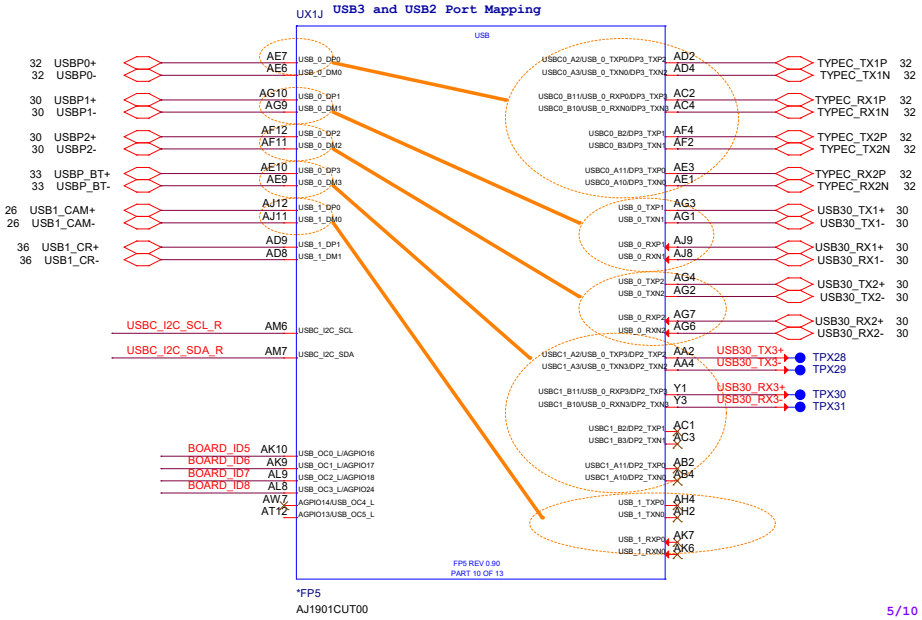


REQUIRED STRAPS

	APU_SPI_CLK	SYS_RST# (Int Pull-Up)
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	normal reset mode DEFAULT
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

SMT require put on TOP side





*FP5
AJ1901CUT00

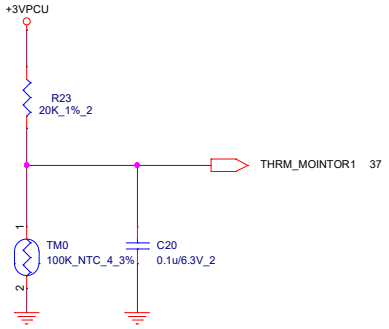
USB TYPE C

U3B NORMAL

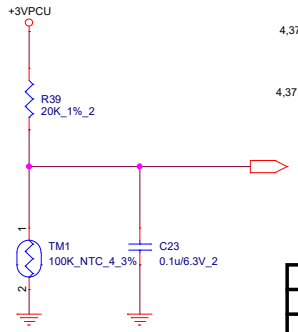
U3B NORMAL

USB3 Port	Function
USB0/0	TYPE-C
USB0/1	TYPE-A
USB0/2	TYPE-A
USB0/3	NC
USB1/0	NC

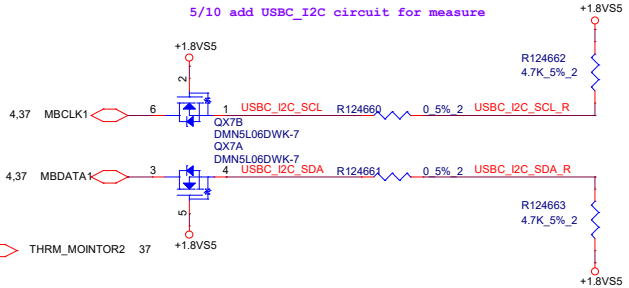
CPU Thermal Protect



Pipe Thermal Protect



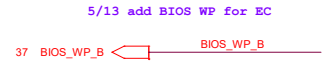
5/10 add USBC_I2C circuit for measure

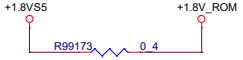


Vender	Size	P/N (1.8V)
WND	16M	AKE5DZN0N01
GGD	16M	AKE5DZN0Q02
Socket	DG008000011	

SPI ROM Sharing (8M Byte)

5/13 add BIOS WP for EC

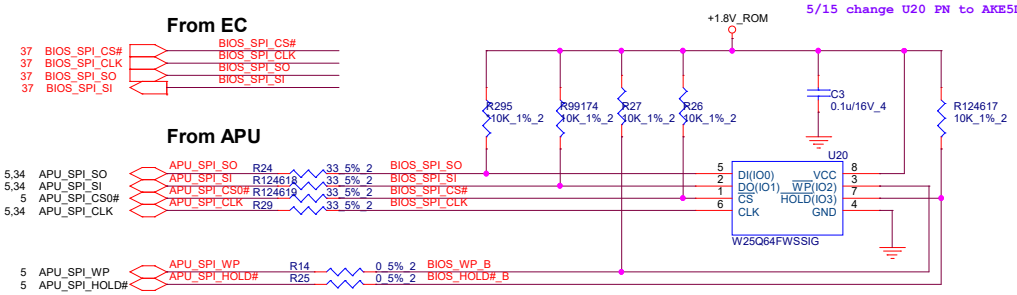




From EC

From APU

5/15 change U20 PN to AKE5DZN0N01



BOARD ID SETTING

Board ID 0	Definition
0	NA(Default)
1	

Board ID [2:1]	Definition
00	N17P
01	N18P
10	N18E
11	NA

Board ID [5:4:3]	Definition (SATA port option)
000	NA(Default)
001	NA
010	NA
011	NA
100	NA
101	NA
110	NA
111	NA

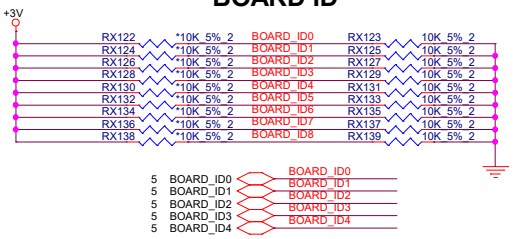
Board ID [6]	Definition
0	G-Sensor(Default)
1	Non G-Sensor

Board ID [7]	Definition
0	NA(Default)
1	NA

Board ID [8]	Definition
0	None TPM
1	TPM

2/21 : Board ID need chack with BIOS

BOARD ID



4,5,7,23,32,33,37,39,42,43,44,48,53,54 +3VS5
4,5,7,34,44,45,48,53 +1.8VS5
4,7,21,22,28,37,46,48 +1.8V

06

NB5

PROJECT : G3HA
Quanta Computer Inc.

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APU POWER

07

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 7*22UF+1*1UF+1*180PF

+VDDCR_SOC

CX35 180p/25V_2 | CX36 1u/10V_2 | CX37 22U/6.3V_6 | CX38 22U/6.3V_6 | CX39 22U/6.3V_6 | CX40 22U/6.3V_6 | CX41 22U/6.3V_6 | CX42 22U/6.3V_6 | CX43 22U/6.3V_6

RR DG: 9*22UF+2*1UF+4*0.22uf+3*180PF

BOTTOM SIDE DECOUPLING UNDER APU

VDDIO_MEM-DDR4:6A

+1.2VSUS

CX46 22u/6.3V_6 | CX65 22u/6.3V_6 | CX66 22u/6.3V_6 | CX47 22u/6.3V_6 | CX48 22u/6.3V_6 | CX67 22u/6.3V_6 | CX68 22u/6.3V_6 | CX69 22u/6.3V_6 | CX70 22u/6.3V_6 | CX49 1u/10V_2 | CX71 1u/10V_2 | CX72 180p/25V_2

CX73 0.22u/6.3V_2 | CX74 0.22u/6.3V_2 | CX75 0.22u/6.3V_2 | CX76 0.22u/6.3V_2 | CX77 180p/25V_2 | CX78 180p/25V_2

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

RR DG: 1*22UF+3*1UF

BOTTOM SIDE DECOUPLING UNDER APU

+0.95VS5 | +VDDP_S5 | RX106 *0_5% 4/S | CX90 22u/6.3V_6 | CX91 1u/6.3V_4 | CX92 1u/6.3V_4 | CX93 1u/6.3V_4

RR DG: 1*22UF+1*1UF

+1.8V | +APU_VDDIO_AZ | RX108 *0_5% 4/S | CX97 1u/6.3V_4 | CX98 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+2*1UF

+3V | +APU_VDD_33 | RX110 *0_5% 4/S | CX102 1u/6.3V_4 | CX103 1u/6.3V_4 | CX104 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+2*1UF

+3VS5 | +APU_VDD_33_S5 | RX115 *0_5% 4/S | CX110 1u/6.3V_4 | CX111 1u/6.3V_4 | CX112 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+1.8V | +VDD_18 | RX107 *0_5% 4/S | RX169 *0_5% 4/S | CX94 1u/6.3V_4 | CX95 1u/6.3V_4 | CX96 22u/6.3V_6

RR DG: 1*22UF+2*1UF

BOTTOM SIDE DECOUPLING UNDER APU

VDDBT_RTC | 4.5uA | RX111 1K_1%_2 | +1.5V_RTC | RX113 *0_5%_2 | CX105 0.22u/6.3V_2 | CX106 1u/10V_2

+1.8VS5 | +VDD_18_S5 | RX109 *0_5% 4/S | CX99 1u/6.3V_4 | CX100 1u/6.3V_4 | CX101 22u/6.3V_6

RR DG: 1*22UF+2*1UF

BOTTOM SIDE DECOUPLING UNDER APU

+VDDCR_SOC | UX1F | POWER | 13A | 70A

M15 VDDCR_SOC_1, M18 VDDCR_SOC_2, M19 VDDCR_SOC_3, N16 VDDCR_SOC_4, N18 VDDCR_SOC_5, N20 VDDCR_SOC_6, P17 VDDCR_SOC_7, P19 VDDCR_SOC_8, R18 VDDCR_SOC_9, R20 VDDCR_SOC_10, T19 VDDCR_SOC_11, U18 VDDCR_SOC_12, U20 VDDCR_SOC_13, V19 VDDCR_SOC_14, W18 VDDCR_SOC_15, W20 VDDCR_SOC_16, Y19 VDDCR_SOC_17

T32 VDDIO_MEM_S3_1, V28 VDDIO_MEM_S3_2, W28 VDDIO_MEM_S3_3, W32 VDDIO_MEM_S3_4, Y22 VDDIO_MEM_S3_5, Y25 VDDIO_MEM_S3_6, Y28 VDDIO_MEM_S3_7, AA20 VDDIO_MEM_S3_8, AA23 VDDIO_MEM_S3_9, AA26 VDDIO_MEM_S3_10, AA28 VDDIO_MEM_S3_11, AA32 VDDIO_MEM_S3_12, AC20 VDDIO_MEM_S3_13, AC22 VDDIO_MEM_S3_14, AC25 VDDIO_MEM_S3_15, AC28 VDDIO_MEM_S3_16, AD23 VDDIO_MEM_S3_17, AD26 VDDIO_MEM_S3_18, AD28 VDDIO_MEM_S3_19, AD32 VDDIO_MEM_S3_20, AE20 VDDIO_MEM_S3_21, AE22 VDDIO_MEM_S3_22, AE25 VDDIO_MEM_S3_23, AE28 VDDIO_MEM_S3_24, AF23 VDDIO_MEM_S3_25, AF26 VDDIO_MEM_S3_26, AF28 VDDIO_MEM_S3_27, AF32 VDDIO_MEM_S3_28, AG20 VDDIO_MEM_S3_29, AG22 VDDIO_MEM_S3_30, AG25 VDDIO_MEM_S3_31, AG28 VDDIO_MEM_S3_32, AJ20 VDDIO_MEM_S3_33, AJ23 VDDIO_MEM_S3_34, AJ26 VDDIO_MEM_S3_35, AJ28 VDDIO_MEM_S3_36, AJ32 VDDIO_MEM_S3_37, AK28 VDDIO_MEM_S3_38, AL28 VDDIO_MEM_S3_39, AL32 VDDIO_MEM_S3_40

+APU_VDDIO_AZ — AP12 VDDIO_AUDIO — 0.2A

+APU_VDD_33 — AL18 VDD_33_1, AM17 VDD_33_2 — 0.25A

+VDD_18 — AL20 VDD_18_1, AM19 VDD_18_2 — 2A

+VDD_18_S5 — AL19 VDD_18_S5_1, AM18 VDD_18_S5_2 — 0.5A

+APU_VDD_33_S5 — AL17 VDD_33_S5_1, AM16 VDD_33_S5_2 — 0.25A

+VDDP_S5 — AL14 VDDP_S5_1, AL15 VDDP_S5_2, AM14 VDDP_S5_3 — 1A

+VDDP_S0 — AL13 VDDP_1, AM12 VDDP_2, AM13 VDDP_3, AN12 VDDP_4, AN13 VDDP_5 — 4A

VDDBT_RTC — AT11 VDDBT_RTC_G

G7 VDDCR_1, G10 VDDCR_2, G12 VDDCR_3, G14 VDDCR_4, H8 VDDCR_5, H11 VDDCR_6, H15 VDDCR_7, K7 VDDCR_8, K12 VDDCR_9, K14 VDDCR_10, L8 VDDCR_11, M7 VDDCR_12, M10 VDDCR_13, N14 VDDCR_14, P7 VDDCR_15, P10 VDDCR_16, P13 VDDCR_17, P15 VDDCR_18, R8 VDDCR_19, R14 VDDCR_20, R16 VDDCR_21, T7 VDDCR_22, T10 VDDCR_23, T13 VDDCR_24, T15 VDDCR_25, T17 VDDCR_26, U14 VDDCR_27, U16 VDDCR_28, V13 VDDCR_29, V15 VDDCR_30, V17 VDDCR_31, W7 VDDCR_32, W10 VDDCR_33, W14 VDDCR_34, W16 VDDCR_35, Y8 VDDCR_36, Y13 VDDCR_37, Y15 VDDCR_38, Y17 VDDCR_39, AA7 VDDCR_40, AA10 VDDCR_41, AA14 VDDCR_42, AA16 VDDCR_43, AA18 VDDCR_44, AB13 VDDCR_45, AB15 VDDCR_46, AB17 VDDCR_47, AB19 VDDCR_48, AC14 VDDCR_49, AC16 VDDCR_50, AC18 VDDCR_51, AD7 VDDCR_52, AD10 VDDCR_53, AD13 VDDCR_54, AD15 VDDCR_55, AD17 VDDCR_56, AD19 VDDCR_57, AE8 VDDCR_58, AE14 VDDCR_59, AE16 VDDCR_60, AE18 VDDCR_61, AF7 VDDCR_62, AF10 VDDCR_63, AF13 VDDCR_64, AF15 VDDCR_65, AF17 VDDCR_66, AF19 VDDCR_67, AG14 VDDCR_68, AG16 VDDCR_69, AG18 VDDCR_70, AH13 VDDCR_71, AH15 VDDCR_72, AH17 VDDCR_73, AH19 VDDCR_74, AJ7 VDDCR_75, AJ10 VDDCR_76, AJ14 VDDCR_77, AJ16 VDDCR_78, AJ18 VDDCR_79, AK13 VDDCR_80, AK15 VDDCR_81, AK17 VDDCR_82, AK19 VDDCR_83

FP5 REV 0.90
PART 6 OF 13

*FP5
AJ1901CUT00

+VDDNB_CORE 17,18,43 | +1.2VSUS | +0.9VS5 4,6,21,22,28,37,46,48 | +1.8V | +3V 4,5,6,17,18,21,26,27,28,32,33,35,36,37,38,39,46,48,49,50,51,52,53 | +3VS5 4,5,6,23,32,33,37,39,42,43,44,48,53,54 | +VCC_CORE 46,47 | +1.8VS5 4,5,6,34,44,45,48,53 | +0.95V 4,37,44 | +3VPCU 6,30,32,33,37,38,41,42,54,55

+VCC_CORE

CX50 22U/6.3V_6 | CX51 22U/6.3V_6 | CX52 22U/6.3V_6 | CX53 22U/6.3V_6 | CX54 22U/6.3V_6

RR DG: 16*22UF+1*180PF

CX55 22U/6.3V_6 | CX56 22U/6.3V_6 | CX57 22U/6.3V_6 | CX44 22U/6.3V_6

CX58 22U/6.3V_6 | CX59 22U/6.3V_6 | CX60 22U/6.3V_6 | CX61 22U/6.3V_6 | CX62 22U/6.3V_6 | CX63 22U/6.3V_6 | CX45 22U/6.3V_6 | CX64 180p/25V_2

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 2*22UF+8*1UF+1*180PF

+0.95V | +VDDP_S0

RX105 *0_5% 6/S | RX170 *0_5% 6/S

BOTTOM SIDE DECOUPLING UNDER APU

CX79 1u/10V_2 | CX80 180p/25V_2 | CX81 1u/10V_2 | CX82 1u/10V_2 | CX83 1u/10V_2

CX84 22u/6.3V_6 | CX85 22u/6.3V_6 | CX86 1u/10V_2

CX87 1u/10V_2 | CX88 1u/10V_2 | CX89 1u/10V_2

VDDBT_RTC

QX5 2N7002K

EC_RTC_RST 37

RX116 10K_5%_2

+BAT_RTC | RX112 470_1%_4 | +VCCRTC_2 | +3VPCU | DX6 BAT54CW | 20MIL | +3VRTC

UX3 AP2138N-1.5TRG1 (GND, VIN, VOUT)

CX108 0.1u/6.3V_2 | CX109 1u/6.3V_4 | CX107 10u/6.3V_4 | +1.5V_RTC

NB5

PROJECT : G3HA
Quanta Computer Inc.

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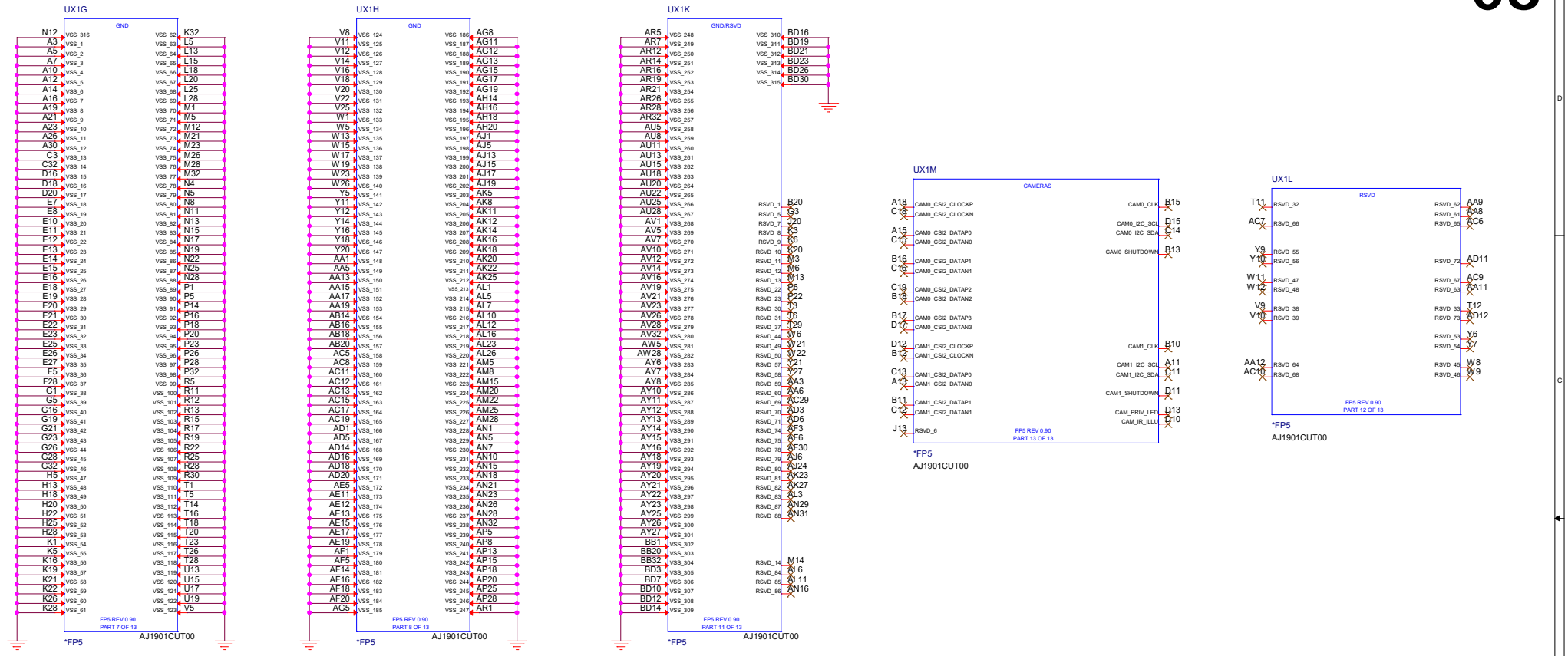
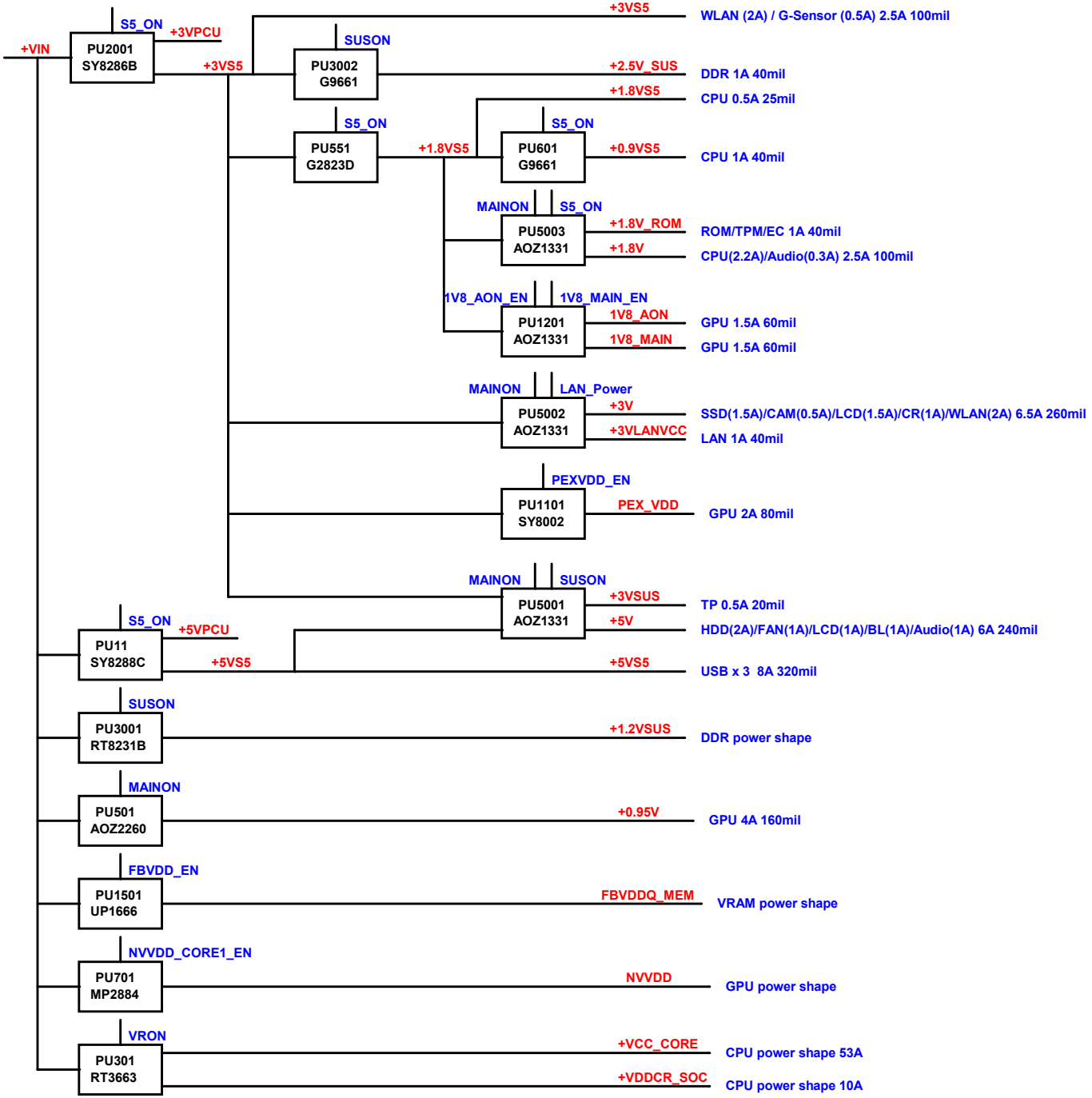
APU GND



NB5	**PROJECT : G3HA** Quanta Computer Inc.	
Size: Custom	Document Number: RR 7/7(GND/RSVD)	Rev: 1A
Date: Friday, June 21, 2019	Sheet 8 of 54	



NB5

PROJECT : G3HA
Quanta Computer Inc.

Size	Document Number	Rev
C	PCH 3/7 (SATA/LPC/CLK)	1A

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A	PCH 3/7 (SATA/LPC/CLK)	1A

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Size	Document Number	Rev
Custom	PCH 3/7 (SATA/LPC/CLK)	1A

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Size	Document Number	Rev
Custom	PCH 4/7 (GPIO/MISC)	1A

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Size	Document Number	Rev
C	PCH 6/7 (POWER)	1A

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PROJECT : G3HA
Quanta Computer Inc.

Size	Document Number	Rev
B	PCH 7/7 (GND)	1A

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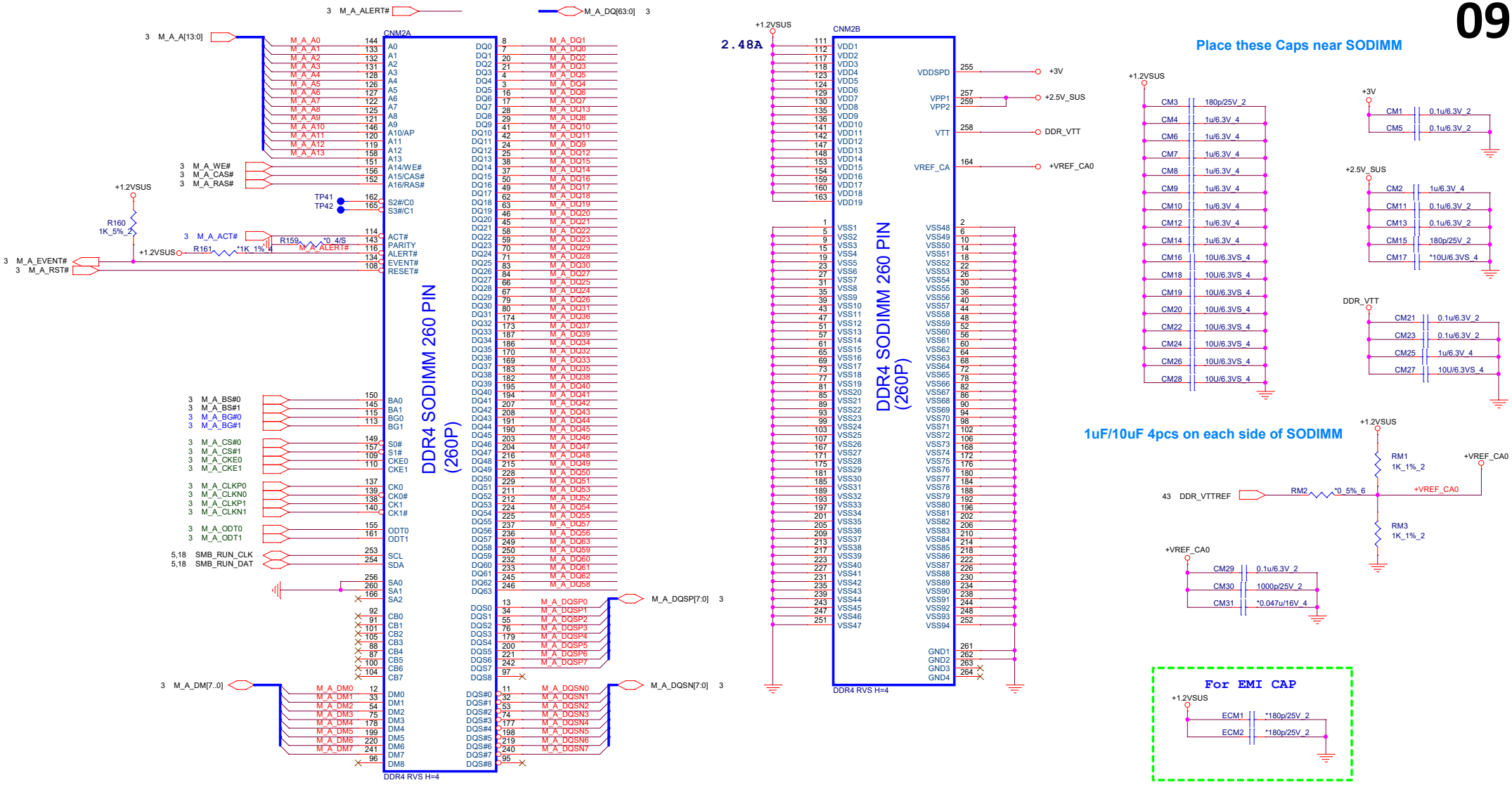
NB5

PROJECT : G3HA
Quanta Computer Inc.

Size	Document Number	Rev
	Strap Pins	1A
Date: Friday, June 21, 2019	Sheet 16of 54	

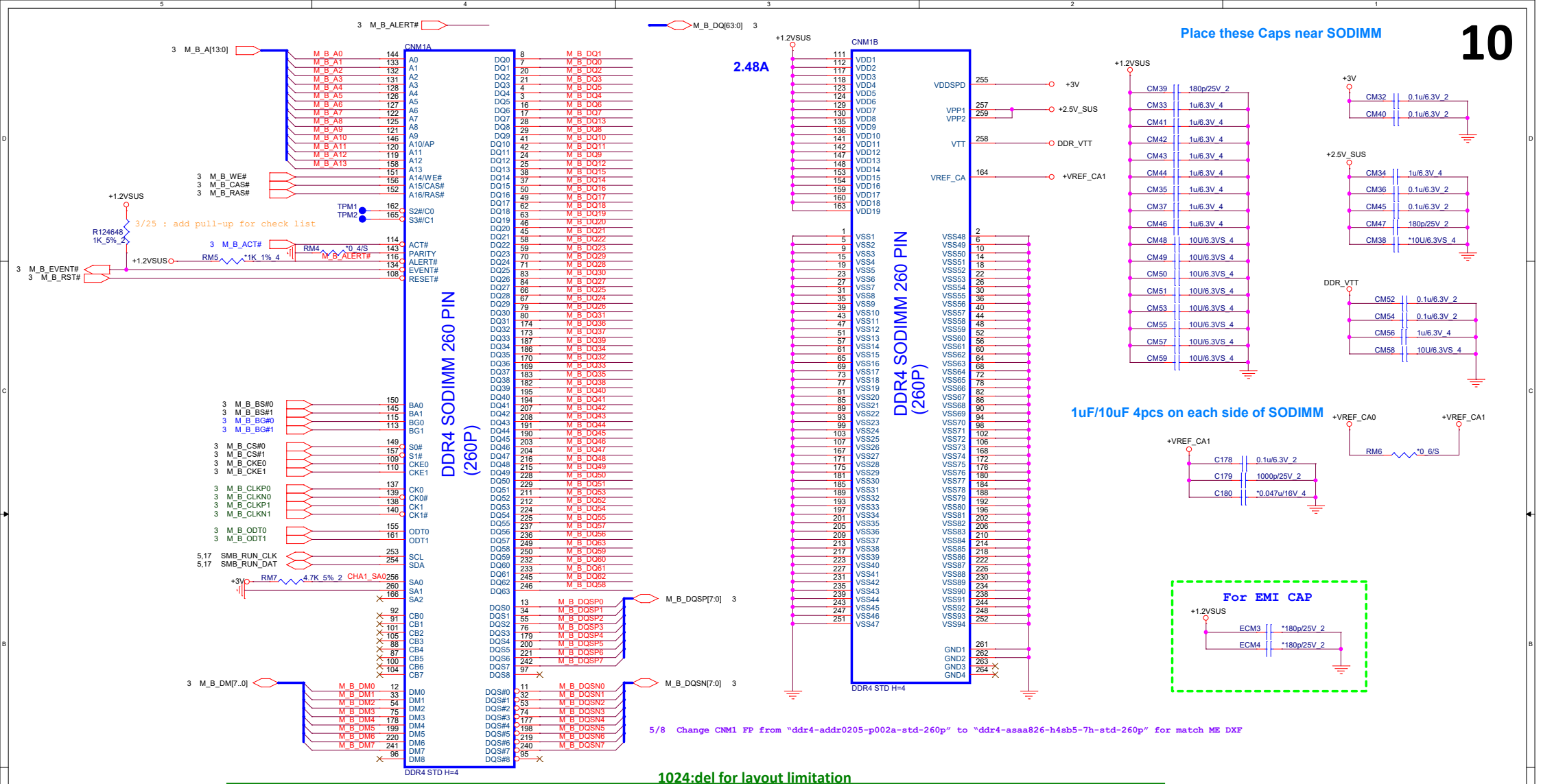


Place these Caps near SODIMM

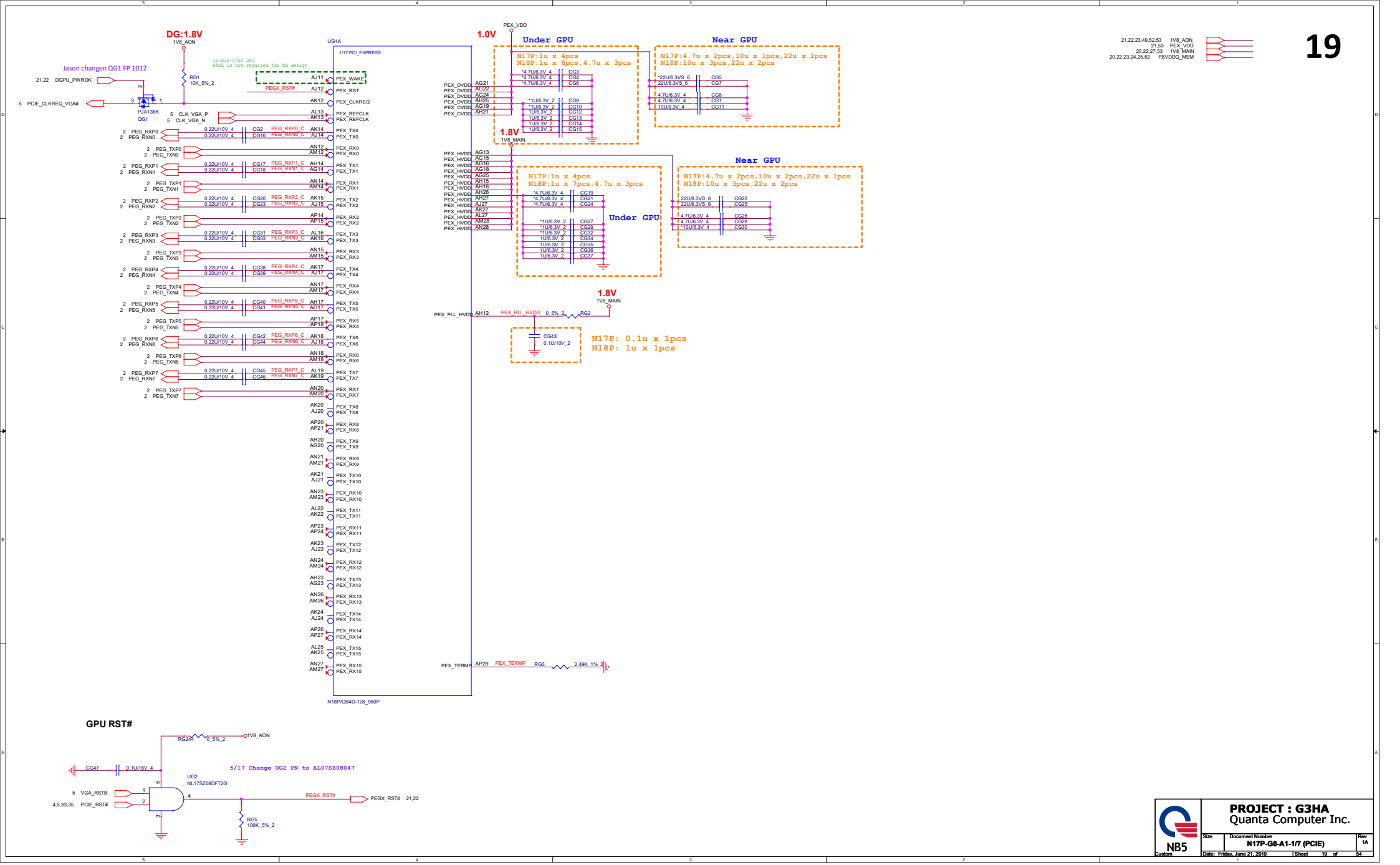
1uF/10uF 4pcs on each side of SODIMM

5/8 Change CNM2 FP from "ddr4-as0a826-h4rb-7h-rvs-smt" to "ddr4-asaa826-h4rb5-7h-rvs-260p" for match ME DXF

NB5	PROJECT : G3HA Quanta Computer Inc.	
Size: Custom	Document Number: CHA0 DDR4 DIMM0-RVS(4.0H)	Rev: 1A
Date: Friday, June 21, 2019	Sheet 17 of 54	



PROJECT : G3HA Quanta Computer Inc.			
NB5	Size: Custom	Document Number: CHA1 DDR4 DIMM1-STD(4.0H)	Rev: 1A
	Date: Friday, June 21, 2019	Sheet 18 of 54	


DG:1.8V
1V8_AON
Jason changen QG1 FP 1012
JS-N18-0705 Del
WAKE is not required for NB design
21,22 DGPU_PWROK
RG1 10K_5%_2
5 PCIE_CLKREQ_VGA#
QG1 PJA138K
PEGX_RST#
5 CLK_VGA_P
5 CLK_VGA_N
UG1A
1/17 PCI_EXPRESS
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEX_TX0
PEX_RX0
PEX_TX1
PEX_RX1
PEX_TX2
PEX_RX2
PEX_TX3
PEX_RX3
PEX_TX4
PEX_RX4
PEX_TX5
PEX_RX5
PEX_TX6
PEX_RX6
PEX_TX7
PEX_RX7
PEX_TX8
PEX_RX8
PEX_TX9
PEX_RX9
PEX_TX10
PEX_RX10
PEX_TX11
PEX_RX11
PEX_TX12
PEX_RX12
PEX_TX13
PEX_RX13
PEX_TX14
PEX_RX14
PEX_TX15
PEX_RX15
N18P/GB4D-128_960P
1.0V
PEX_VDD
Under GPU
N17P:1u x 4pcs
N18P:1u x 6pcs,4.7u x 3pcs
Near GPU
N17P:4.7u x 2pcs,10u x 1pcs,22u x 1pcs
N18P:10u x 3pcs,22u x 2pcs
1.8V
1V8_MAIN
N17P:1u x 4pcs
N18P:1u x 7pcs,4.7u x 3pcs
Under GPU
Near GPU
N17P:4.7u x 2pcs,10u x 2pcs,22u x 1pcs
N18P:10u x 3pcs,22u x 2pcs
PEX_PLL_HVDD
PEX_PLL_HVDD 0_5% 2
RG2
CG43 0.1U/10V_2
N17P: 0.1u x 1pcs
N18P: 1u x 1pcs
PEX_TERMP
PEX_TERMP RG3 2.49K_1% 2
GPU RST#
RG244 0_5%_2
CG47 0.1U/16V_4
5/17 Change UG2 PN to AL07SZ08047
UG2
NL17SZ08DFT2G
5 VGA_RSTB
4,5,33,35 PCIE_RST#
RG5 100K_5%_2
PEGX_RST# 21,22
21,22,23,49,52,53 1V8_AON
21,53 PEX_VDD
20,22,27,53 1V8_MAIN
20,22,23,24,25,52 FBVDDQ_MEM
19
PROJECT : G3HA
Quanta Computer Inc.
NB5
Custom
Size
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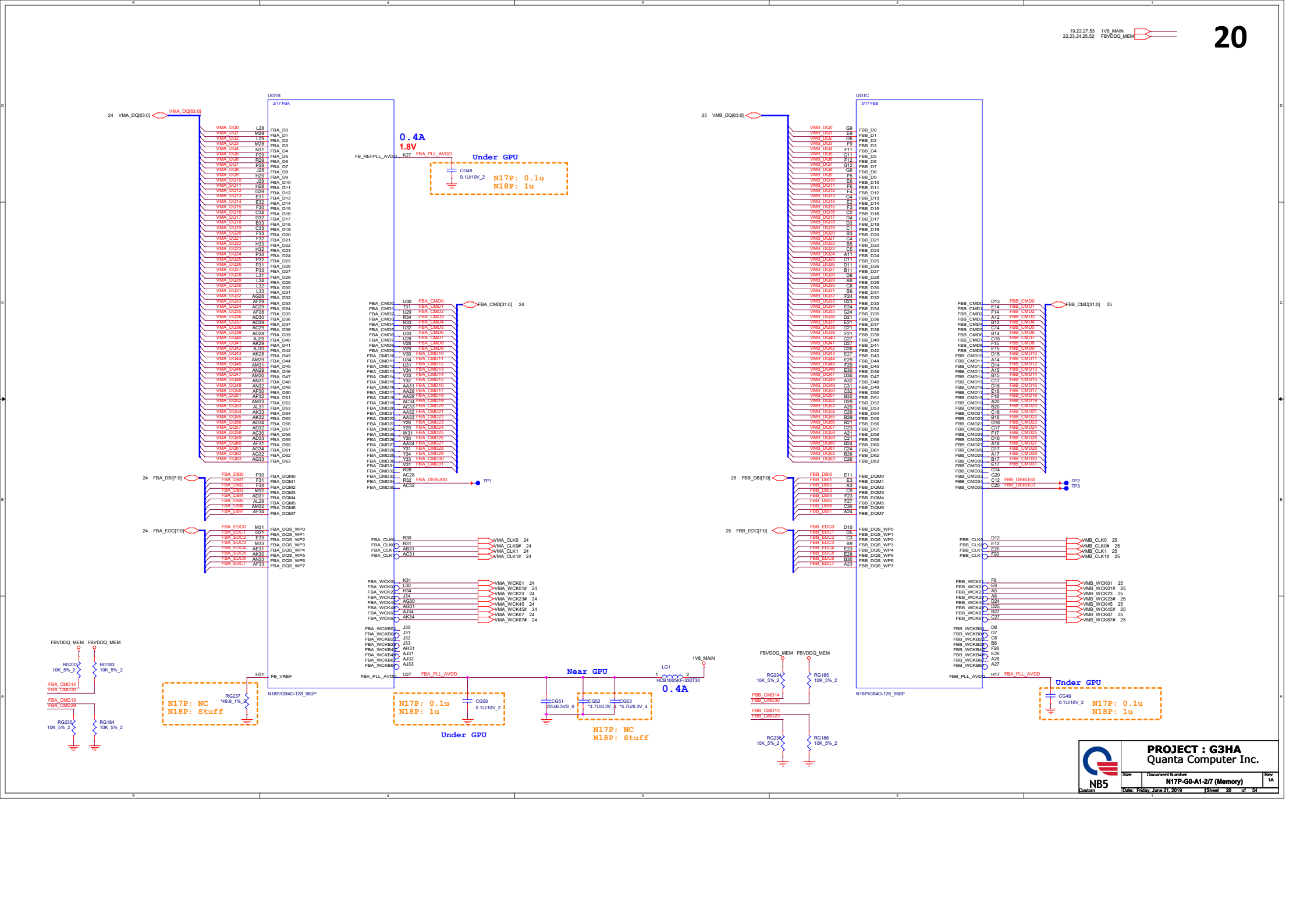
19,22,27,53 1V8_MAIN
22,23,24,25,52 FBVDDQ_MEM
UG1B
2/17 FBA
UG1C
3/17 FBB
24 VMA_DQ[63:0]
25 VMB_DQ[63:0]
0.4A
1.8V
FB_REFPLL_AVDD
K27 FBA_PLL_AVDD
Under GPU
CG48
0.1U/10V_2
N17P: 0.1u
N18P: 1u
FBA_CMD[31:0] 24
FBB_CMD[31:0] 25
24 FBA_DBI[7:0]
25 FBB_DBI[7:0]
FBA_DEBUG0
FBB_DEBUG0
TP1
TP2
TP3
24 FBA_EDC[7:0]
25 FBB_EDC[7:0]
FBVDDQ_MEM
RG233
10K_5%_2
RG183
10K_5%_2
FBA_CMD14
FBA_CMD30
FBA_CMD13
FBA_CMD29
RG235
10K_5%_2
RG184
10K_5%_2
H31 FB_VREF
RG237
*49.9_1%
N17P: NC
N18P: Stuff
N18P/GB4D-128_960P
FBA_PLL_AVDD
Near GPU
1V8_MAIN
LG1
HCB1005KF-330T30
0.4A
CG50
0.1U/10V_2
N17P: 0.1u
N18P: 1u
Under GPU
CG51
2.2U/6.3VS_6
CG52
*4.7U/6.3V_4
CG53
*4.7U/6.3V_4
N17P: NC
N18P: Stuff
RG234
10K_5%_2
RG185
10K_5%_2
RG236
10K_5%_2
RG186
10K_5%_2
H17 FBB_PLL_AVDD
CG49
0.1U/10V_2
N17P: 0.1u
N18P: 1u
PROJECT : G3HA
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NB5
Custom
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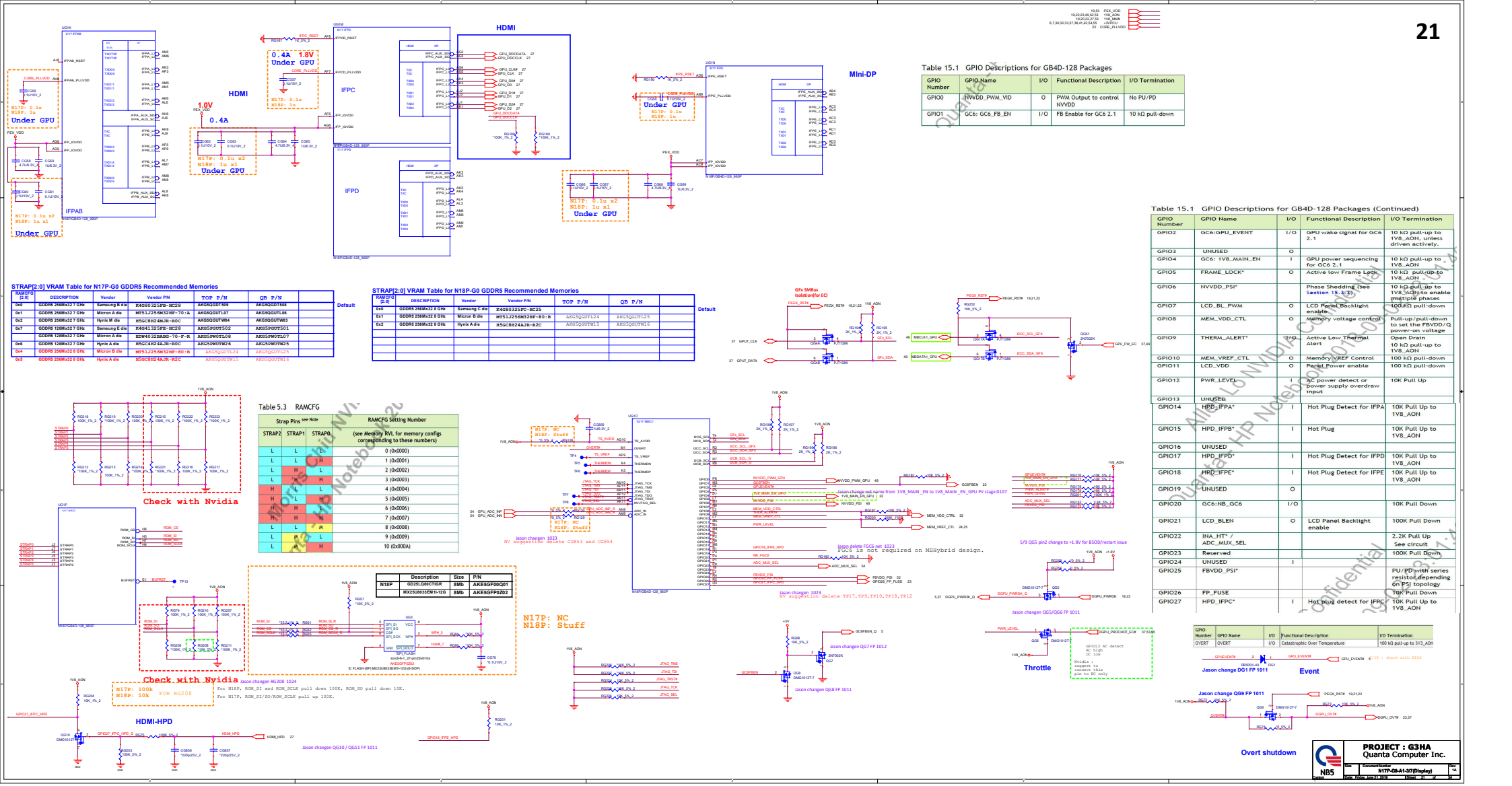


Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No PU/PD
GPIO1	GC6: GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down

Table 15.1 GPIO Descriptions for GB4D-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	GC6:GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6: 1V8_MAIN_EN	I	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AON
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*		Phase Shedding (see Section 15.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug	10K Pull Up to 1V8_AON
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	UNUSED	O		
GPIO20	GC6:NB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HT* / ADC_MUX_SEL			2.2K Pull Up See circuit
GPIO23	Reserved			100K Pull Down
GPIO24	UNUSED	I		
GPIO25	FBVDD_PSI*			PU/PD with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot Plug detect for IFPC	10K Pull Up to 1V8_AON

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508	
0x1	GDDR5 256Mx32 7 GHz	Micron A die	MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06	
0x2	GDDR5 256Mx32 7 GHz	Hynix M die	H5GC8H24MJR-R0C	AKG5QGUTW03	AKG5QGUTW04	
0x7	GDDR5 128Mx32 7 GHz	Samsung E die	K4G41325FE-HC28	AKG5SQDTS01	AKG5SQDTS02	
	GDDR5 128Mx32 7 GHz	Micron A die	EDW4032BABG-70-F-R	AKG5PW0TL08	AKG5PW0TL07	
0x6	GDDR5 128Mx32 7 GHz	Hynix A die	H5GC4H24AJR-R0C	AKG5PWUTW26	AKG5PWUTW25	
0x4	GDDR5 256Mx32 6 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25	
0x5	GDDR5 256Mx32 6 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16	

Default

STRAP[2:0] VRAM Table for N18P-G0 GDDR5 Recommended Memories

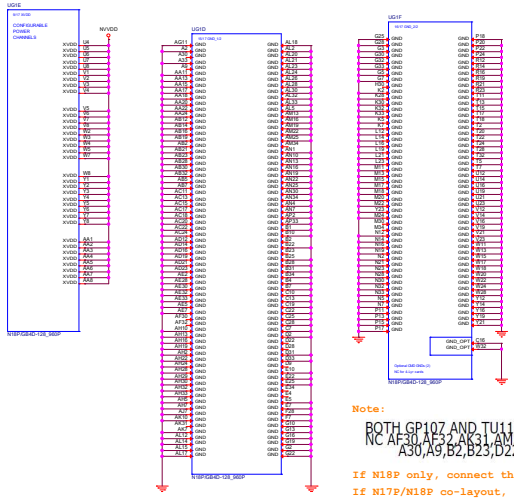
RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 8 GHz	Samsung C die	K4G80325FC-HC25			
0x1	GDDR5 256Mx32 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25	
0x2	GDDR5 256Mx32 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16	

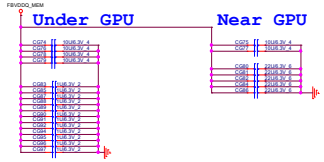
Default

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

	Description	Size	P/N
N18P	GD25LQ80CTIGR	8Mb	AKESGF00Q81
	MX25U8033EM1I-12G	8Mb	AKESGFP0Q02



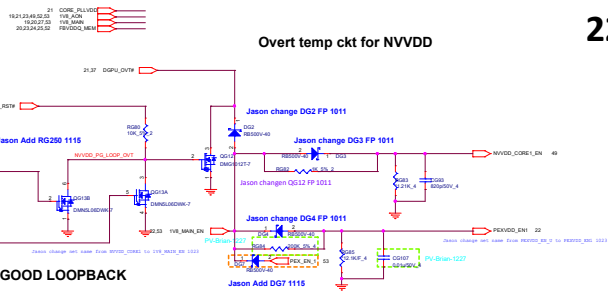


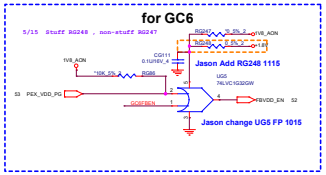
Note:

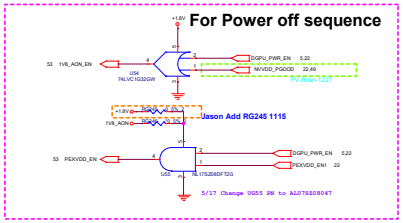
BOTH GP107 AND TU117-G5 NEED
NC AF30,AF32,AK31,AM34,F34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

If N18P only, connect these pin to GND
If N17P/N18P co-layout, leave these pin NC
If N17P only, leave these pin NC

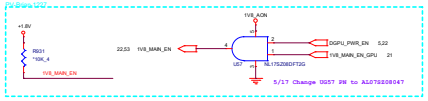
Jason remove those FGC6 1023

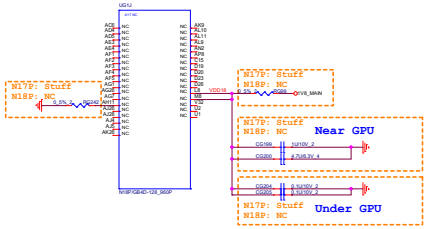


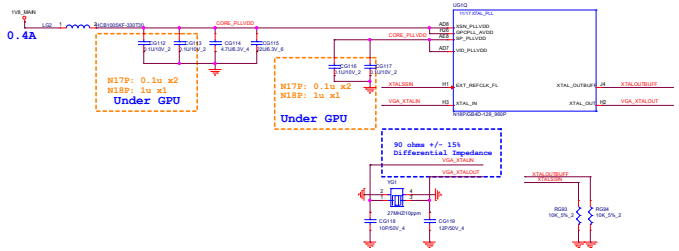




Jason add For Power off sequence 1023

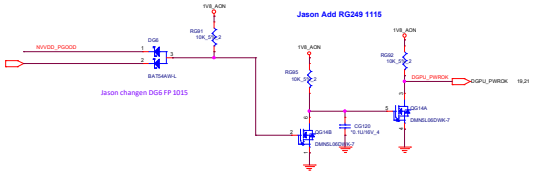


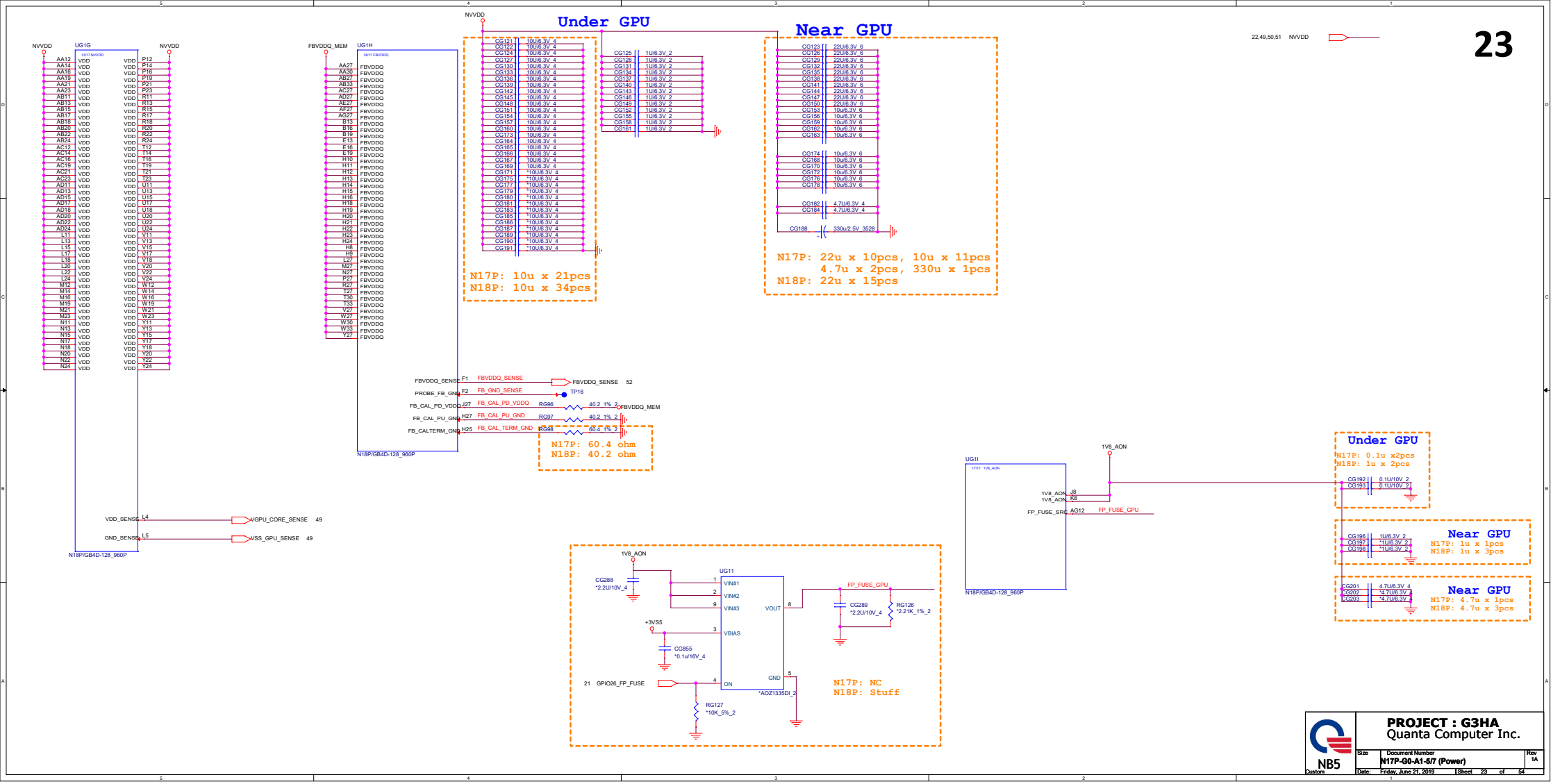




	GC6_1V8_MAIN_EN	GC6FBEN	NB_FGC6	1V8_AON	1V8_MAIN	NVVDD	PEX_VDD	FBVDDQ
POWER ON	1	0	0	ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FGC6	0	1	1	ON	ON	OFF	ON	ON

GPU All power good





Project	G3HA
Company	Quanta Computer Inc.
Size	NB5
Document Number	N17P-G0-A1-5/7 (Power)
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CHANNEL A: 2G/4G GDDR5

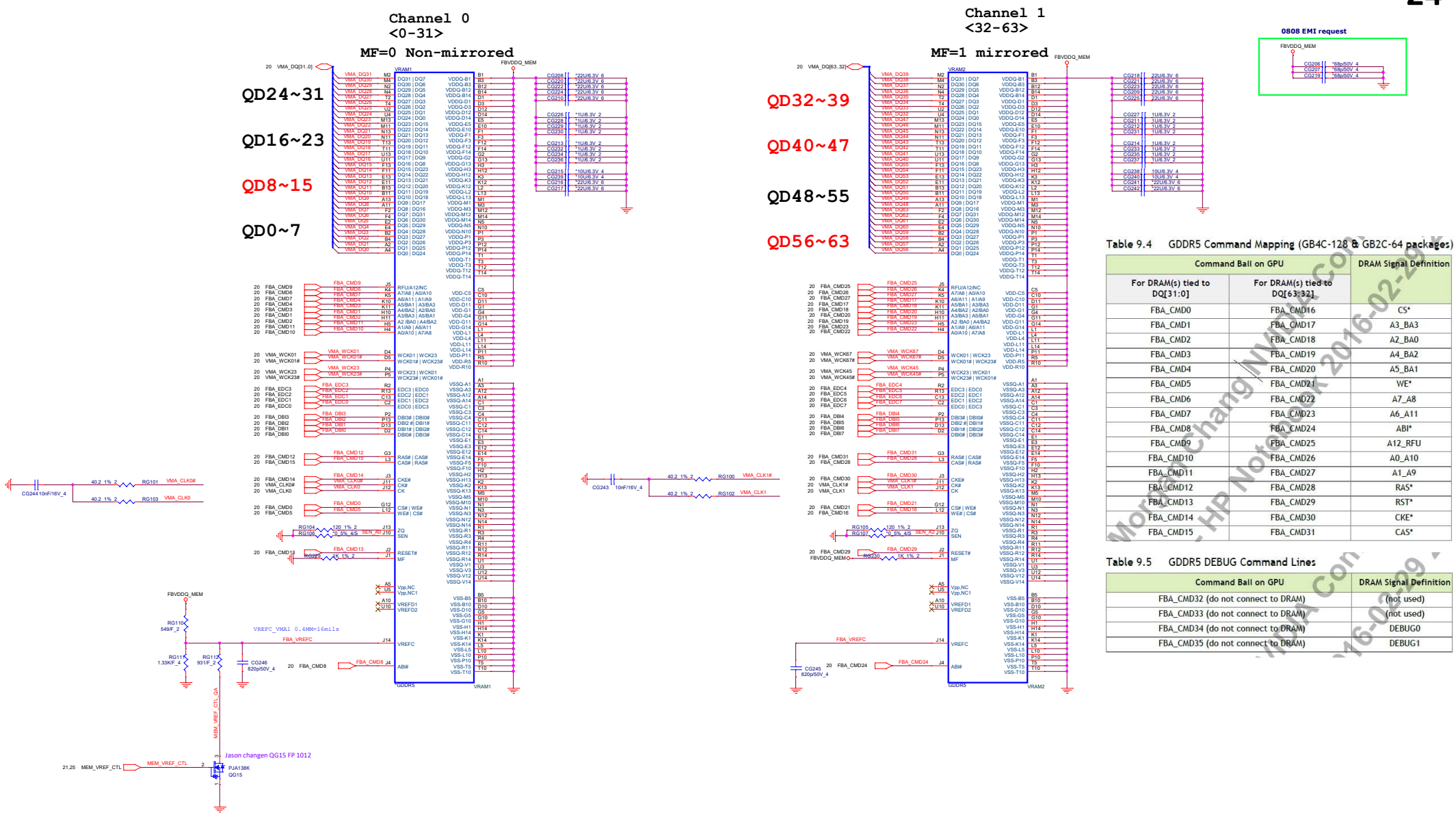


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

Jason change 1023
Follow N18P EBoard bit swap connection

swap DQ30 ,DQ31
swap DQ20 ,DQ22,DQ23
swap DQ12 ,DQ15

Channel 0
<0-31>
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

Channel 1
<32-63>
MF=1 mirrored

QD32~39
QD40~47
QD48~55
QD56~63

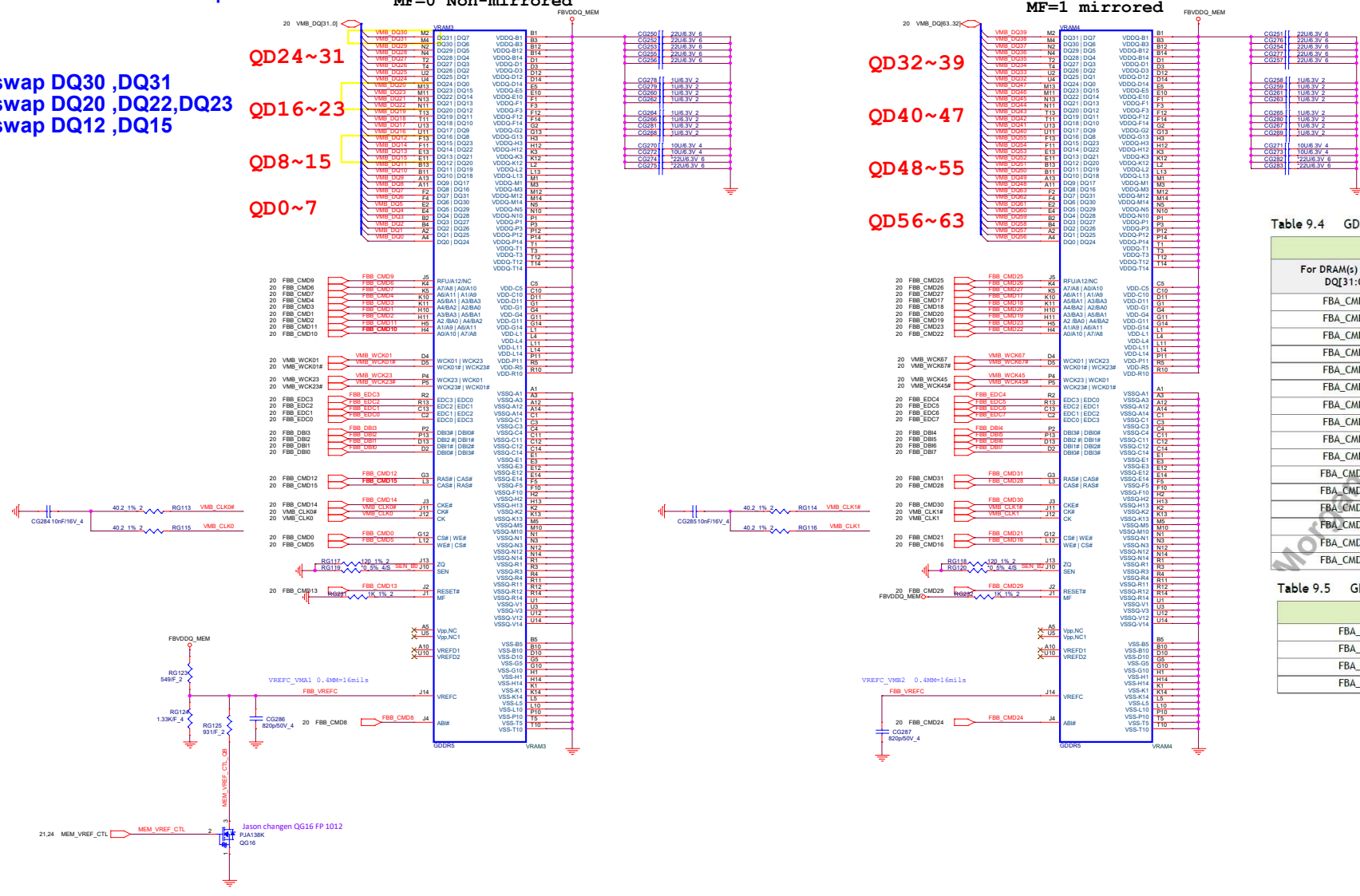


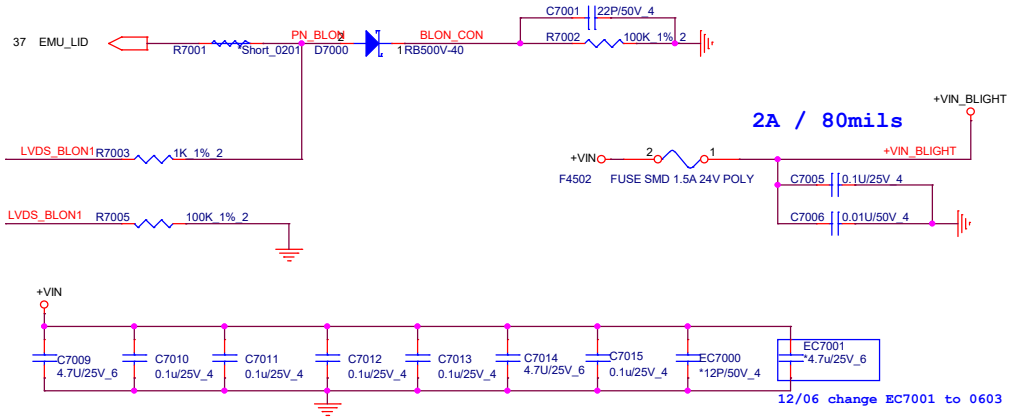
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

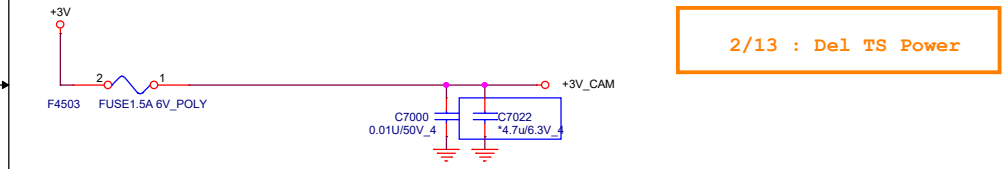
Table 9.5 GDDR5 DEBUG Command Lines

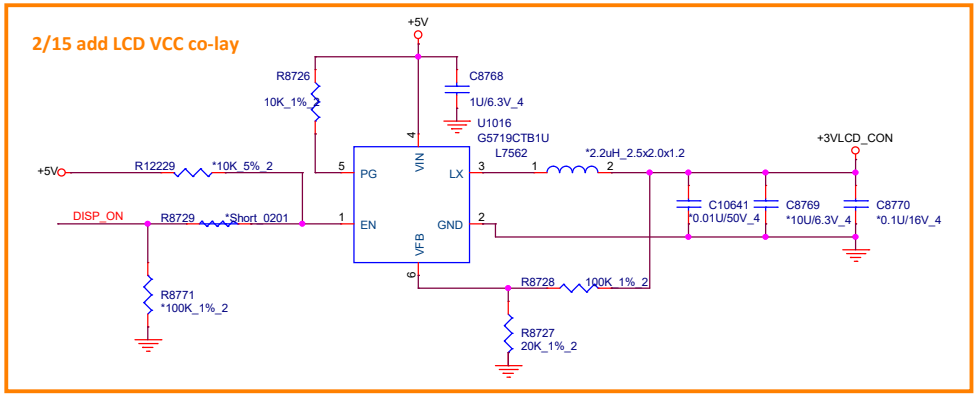
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

LID Switch



Touch screen

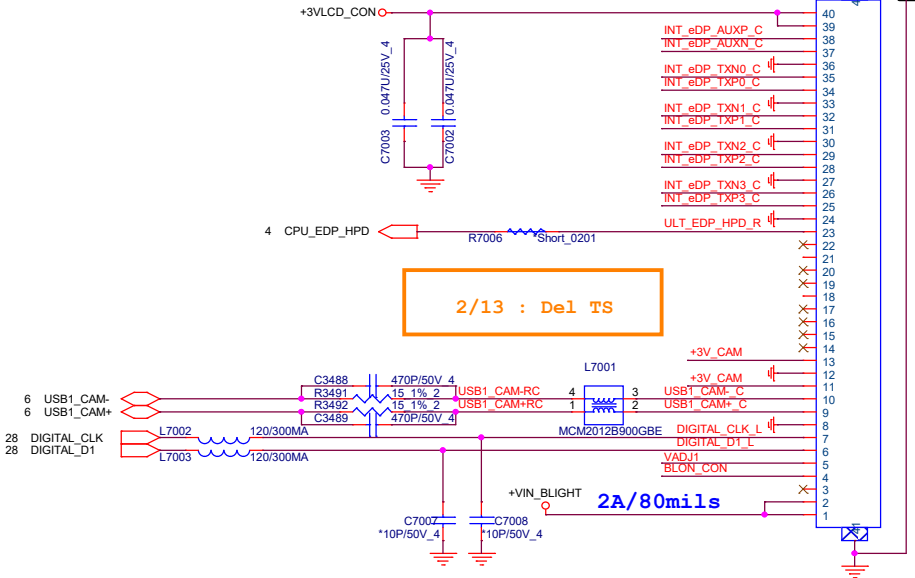


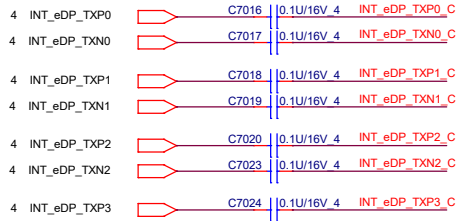


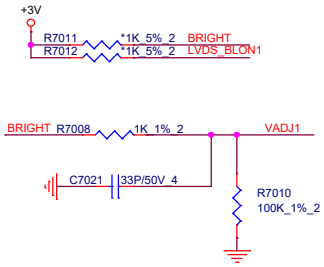
eDP Conn.

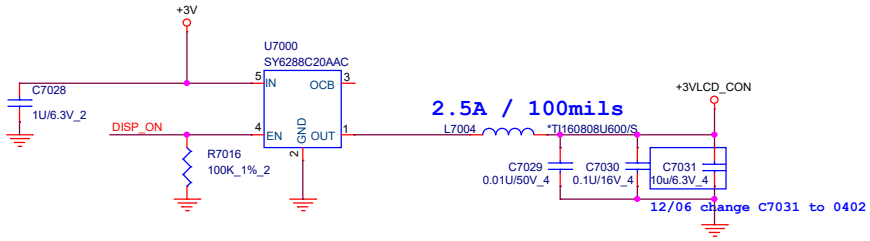
3/17 : Change CN7000 FP

FFC 40P 1R FR
51693-0400t-v01-40p-l
DFFC40FR103
CN7000









4,5,6,7,17,18,21,27,28,32,33,35,36,37,38,39,46,48,49,50,51,52,53 +3V
6,7,30,32,33,37,38,41,42,54,55 +3VPCU
27,28,32,38,48,54 +5V
38,40,41,42,43,44,46,47,48,52 +VIN

NB5

PROJECT : G3HA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
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4,5,6,7,17,18,21,26,28,32,33,35,36,37,38,39,46,48,49,50,51,52,53 +3V

26,28,32,38,48,54 +5V

01/11 change to 0 ohm for NV suggest

TX2_HDMI+	R20426	6.8/F_4	TX2_HDMI+CN
TX2_HDMI-	R20429	6.8/F_4	TX2_HDMI-CN
TX1_HDMI+	R20431	6.8/F_4	TX1_HDMI+CN
TX1_HDMI-	R20433	6.8/F_4	TX1_HDMI-CN
TX0_HDMI+	R20443	6.8/F_4	TX0_HDMI+CN
TX0_HDMI-	R20445	6.8/F_4	TX0_HDMI-CN
TXC_HDMI+	R20436	6.8/F_4	TXC_HDMI+CN
TXC_HDMI-	R20438	6.8/F_4	TXC_HDMI-CN

1/11 modify for HDMI2.0

01/11 unstuff for HDMI output from GPU

EMI Solution

TX2_HDMI+	R20427	*120_1%_2	TX2_HDMI-
TX1_HDMI+	R20432	*120_1%_2	TX1_HDMI-
TX0_HDMI+	R20444	*120_1%_2	TX0_HDMI-
TXC_HDMI+	R20437	*120_1%_2	TXC_HDMI-

11/04 modify for HDMI2.0

11/03 modify for HDMI2.0

21 GPU_D0	C20637	0.1U/16V_4	TX0_HDMI+
21 GPU_D0#	C20638	0.1U/16V_4	TX0_HDMI-
21 GPU_D1	C20629	0.1U/16V_4	TX1_HDMI+
21 GPU_D1#	C20632	0.1U/16V_4	TX1_HDMI-
21 GPU_D2	C20626	0.1U/16V_4	TX2_HDMI+
21 GPU_D2#	C20628	0.1U/16V_4	TX2_HDMI-
21 GPU_CLK	C20633	0.1U/16V_4	TXC_HDMI+
21 GPU_CLK#	C20634	0.1U/16V_4	TXC_HDMI-

21 GPU_DDCCLK

21 GPU_DDCDATA

03/23/16 Modify for N17P.

1V8_MAIN — Q20001 DMG1012T-7 — DGPU_CL_HDMIP

R20425	499_1%_2	TX2_HDMI+
R20428	499_1%_2	TX2_HDMI-
R20430	499_1%_2	TX1_HDMI+
R20434	499_1%_2	TX1_HDMI-
R20440	499_1%_2	TX0_HDMI+
R20446	499_1%_2	TX0_HDMI-
R20435	499_1%_2	TXC_HDMI+
R20439	499_1%_2	TXC_HDMI-

R20038 1M_5%_2 — C20133 0.1U/16V_4

05/20/16 Modify

ESD

U20018 *AZ1043-04F.R7G

TX0_HDMI-CN	1	10	TX0_HDMI-CN
TX0_HDMI+CN	2	9	TX0_HDMI+CN
	3	8	
TXC_HDMI-CN	4	7	TXC_HDMI-CN
TXC_HDMI+CN	5	6	TXC_HDMI+CN

U20017 *AZ1043-04F.R7G

TX1_HDMI-CN	1	10	TX1_HDMI-CN
TX1_HDMI+CN	2	9	TX1_HDMI+CN
	3	8	
TX2_HDMI-CN	4	7	TX2_HDMI-CN
TX2_HDMI+CN	5	6	TX2_HDMI+CN

1125 Reserve ESD protection component

1125 SWAP

02/08 U20018、U20017 change to BC001043Z00 by sourcer suggest

HDMI SMBus Isolation

Close to HDMI connector

R20450 *0_5%_2 — 1V8_MAIN — Q20028 PJT138K

1V8_MAIN R20449 10K_5%_2 — GPU_DDCCLK — HDMI_SCLK

GPU_DDCDATA — HDMI_SDATA — 1V8_MAIN R20453 10K_5%_2

R20454 *0_5%_2

01/15 update to DFHD19MR440

CN20006 HDMI CONN

TX2_HDMI+CN	1	SHELL1	20
	2	D2+	
TX2_HDMI-CN	3	D2 Shield	
TX1_HDMI+CN	4	D2-	
	5	D1+	
TX1_HDMI-CN	6	D1 Shield	
TX0_HDMI+CN	7	D1-	
	8	D0+SHELL2	23
TX0_HDMI-CN	9	D0 Shield	
TXC_HDMI+CN	10	D0-	
	11	CK+	
TXC_HDMI-CN	12	CK Shield	22
	13	CK- SHELL3	
	14	CE Remote	
HDMI_SCLK	15	NC	
HDMI_SDATA	16	DDC CLK	
	17	DDC DATA	
	18	GND	
	19	+5V	
		HP DET	21
		SHELL4	

D20000 BAT54AW-L — +5V_HDMIC — 5V_HSMBCK R20451 2.2K_5%_2 — 5V_HSMBDT R20448 2.2K_5%_2

C20641 *10P/50V_4 — C20642 *10P/50V_4

40 mils

+5V — F20000 SMD1206P150TFT/1.5A/6V_1206 — +5V_HDMIC

05/27/16 Modify

VC20001 *TVM0G5R5M220R — C20137 0.1U/16V_4

HDMI_HPD — VC20002 *TVM0G5R5M220R — C20181 220P/50V_4

2/21 : add HDMI HPD circuit to CPU

HDMI HPD Circuit

+3V — R7701 1K_5%_2 — +5V — R5099 100K_5%_2

4 CPU_HDMI_HPD — R5034 *Short_0201 — HDMI_HPD_Q_R

Q7701B 2N7002KDW

Q7701A 2N7002KDW — HDMI_DET_R — R7702 200K_1%_2 — HDMI_HPD

R5096 100K_5%_2

HDMI_HPD — HDMI_HPD 21 — R20042 *20K_1%_2

2KV ESD protection

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Quanta Computer Inc.

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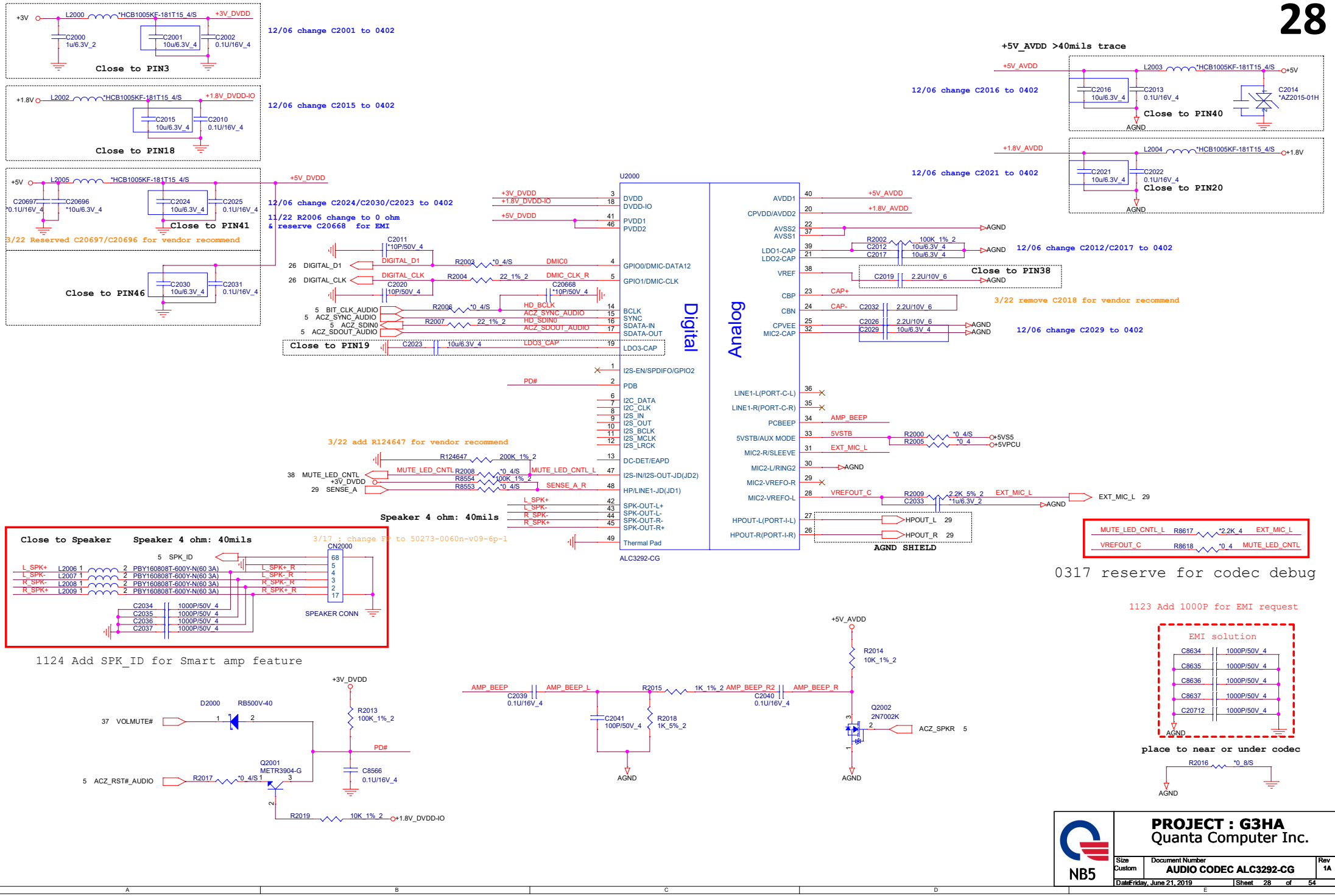

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Quanta Computer Inc.			
NB5	Size: Custom	Document Number: AUDIO CODEC ALC3292-CG	Rev: 1A
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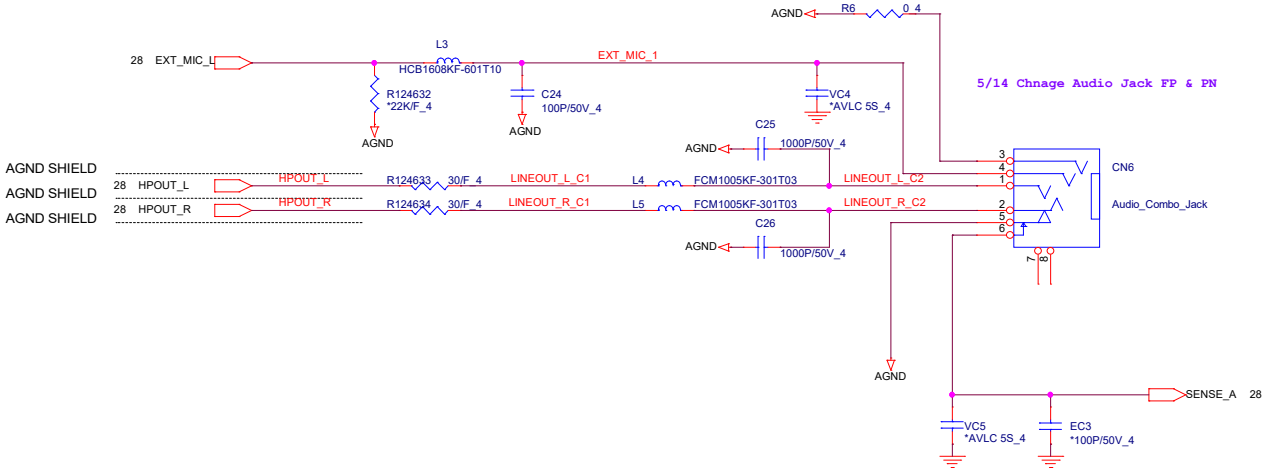
Head Phone out



HOLE

NB5	**PROJECT : G3HA** Quanta Computer Inc.	
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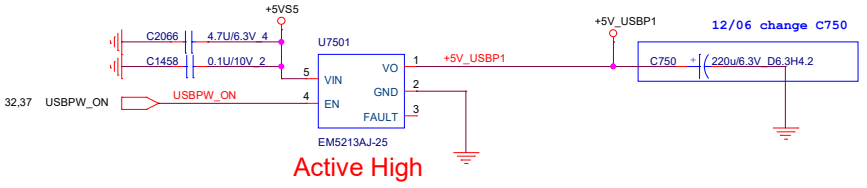
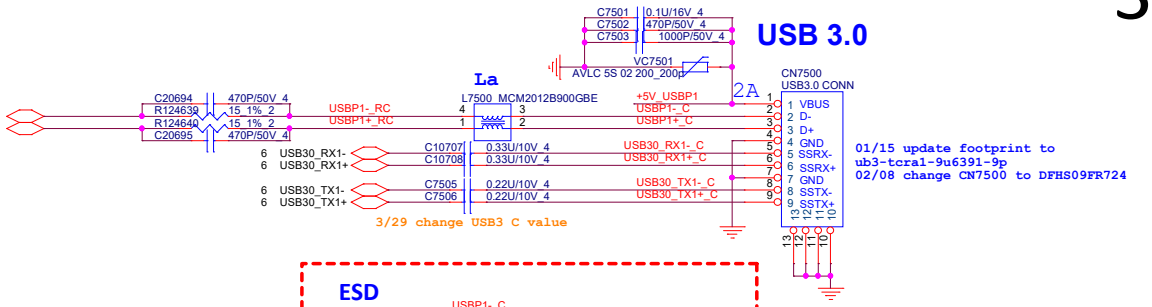
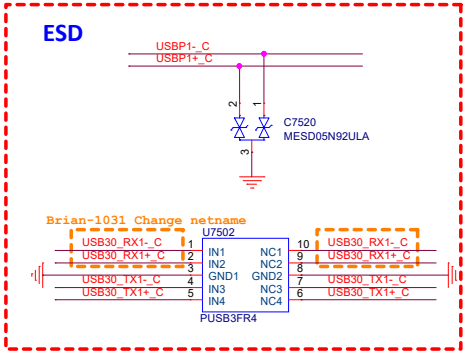
USB BC1.2



USB 3.0

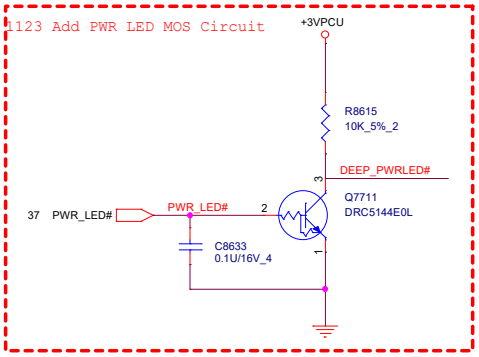


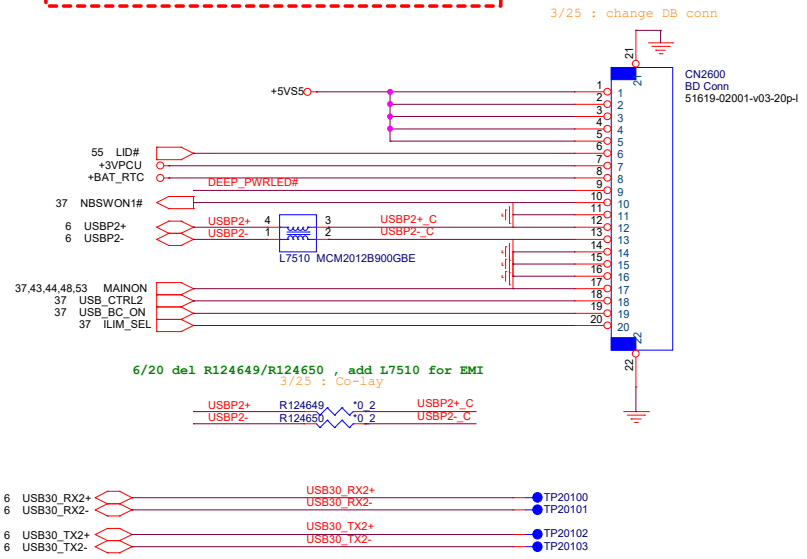
ESD



Daughter Board

Power LED





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Size: Custom	Document Number: USB3.0/DB	Rev: 1A
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Quanta Computer Inc.

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HDD

SATA HDD

SATA_TXP0_C — C4600 0.01U/50V_4 — SATA_TXP0 2
SATA_TXN0_C — C4601 0.01U/50V_4 — SATA_TXN0 2
SATA_RXN0_C — C4602 0.01U/50V_4 — SATA_RXN0 2
SATA_RXP0_C — C4603 0.01U/50V_4 — SATA_RXP0 2

12/06 change C4605/C4604 to 0402

+5V — C4604 *10u/6.3V_4 — C4605 10u/6.3V_4 — C4606 0.1U/16V_4

HD4600

SATA LED

5,33 SATA_LED#
5 ACC_LED#
SATA_LED# — ACC_LED# — R4807 200/F_6
VC4800 *AVLC5S_4 — SATA_R_LED1 — LED4801 LED 3P WHITE/AMBER (Amber) — VC4801 *AVLC5S_4
R4805 39_6 — +3V

TYPE-C

5/17 Change U6350 PN to AL180600001

U6350 TPS25810RVCR(QFN)

+5VS5 — C6358 22U/6.3V_6 — C6352 *47u/6.3V_8 — C6353 47u/6.3V_8 — C6355 22U/6.3V_6 — C6354 22U/6.3V_6 — C6357 0.1u/16V_4

IN01 IN02 IN03 VAUX — TI TPS25810RVC — EN CHG CHG_HI REF REF_RTN GND01 PwPd

OUT01 OUT02 — +TYPEC_VBUS_C
CC1 — 5447_CC1
CC2 — 5447_CC2
FAULT# — 25810_FAULT#
LD_DET# — 25810_LD_DET#
UFP# — 25810_UFP#
POL# — 25810_POL#
AUDIO# — 25810_AUO#
DEBUG# — 25810_DBG#

30,37 USBPW_ON
37 EC_TYPEC_CHG — EC_TYPEC_CHG
37 EC_TYPEC_CHG_HI — EC_TYPEC_CHG_HI
25810_REF — R6360 100K_1%_2 — 25810_REF_RTN

25810_POL# — R6350 100K_1%_2 — +3V
25810_FAULT# — R6353 100K_1%_2 — +5VS5
25810_LD_DET# — R6354 100K_1%_2
25810_UFP# — R6355 100K_1%_2
25810_AUO# — R6356 100K_1%_2
25810_DBG# — R6357 100K_1%_2
EC_TYPEC_CHG — R6358 *100K_1%_2 — +5VS5
EC_TYPEC_CHG_HI — R6359 *100K_1%_2

Add Type-C A/B side recognization

+3VPCU — R6361 10K_5%_2 — +3V
37 EXT_SEL — 2N7002KDW Q6301A — 25810_POL# — +5VS5
37 ID2 — Q6301B 2N7002KDW — 25810_UFP#
R6362 10K_5%_2 — +3VPCU

5/7 Q20029B change to Q6301B

CC/SBU Overvoltage protection

U6300

5447_CC1 — CC1 — C_CC1 — CC1_CON
5447_CC2 — CC2 — C_CC2 — CC2_CON
SBU1 — C_SBU1 — TYPEC_SBU1
SBU2 — C_SBU2 — TYPEC_SBU2
RpD_G1 RpD_G2

*TPD6S300
D1 — USBP_TYPC+_C1 — R6300 *0_2 — USBP0+_C
D2 — USBP_TYPC-_C1 — R6301 *0_2 — USBP0-_C
NC1 NC2 GND1 GND2 GND3 PAD

C6305 *0.1U/10V_2 — VBIAS
+3VS5 — VPWR — C6308 1u/6.3V_4
R6302 *100K_1%_2
FLT

5447_CC1 — R6303 0_2 — CC1_CON
5447_CC2 — R6304 0_2 — CC2_CON

TYPE C USB ESD

U6302 AZ1045-04F.R7G
TYPEC_TX1P_C — Line-1 — NC#4 — TYPEC_TX1P_C
TYPEC_TX1N_C — Line-2 — NC#3 — TYPEC_TX1N_C
GND#1 GND2
TYPEC_RX1P_C — Line-3 — NC#2 — TYPEC_RX1P_C
TYPEC_RX1N_C — Line-4 — NC#1 — TYPEC_RX1N_C

U6303 AZ1045-04F.R7G
TYPEC_TX2P_C — Line-1 — NC#4 — TYPEC_TX2P_C
TYPEC_TX2N_C — Line-2 — NC#3 — TYPEC_TX2N_C
GND#1 GND2
TYPEC_RX2P_C — Line-3 — NC#2 — TYPEC_RX2P_C
TYPEC_RX2N_C — Line-4 — NC#1 — TYPEC_RX2N_C

USBP0+_C
USBP0-_C
C10405 MESD05N92ULA

5/7 co-layout R124658/R124659 BOTTOM SIDE UNDER U6400

+TYPEC_VBUS_C — C6400 2.2u/25V_4 — C6402 10u/25V_6 — R124657 249_1%_4
25810_UFP# — R6450 100K_1%_2 — R6432 0_2
R124658 *0_5%_6 — R124659 *0_5%_6
3/17 : change U6400 to TPD1S414
U6400 TPD1S414
VBUS_SYS1 VBUS_SYS2 VBUS_SYS3 — VBUS_CON1 VBUS_CON2 VBUS_CON3
ACK EN GND1 GND2 GND3 GND4
+TYPEC_VBUS — C6403 2.2u/25V_4 — C6404 4.7u/25V_8

5/7 add R124657 for vendor recommend
5/7 change C6400 / C6402 value for vendor recommend

6/14 ub31-020090hb024m51nzl-24p Footprint
使用生產線有修改過後的
ub31-020090hb024m51nzl-24p-smt

TYPE-C CONN

3/17 : change conn FP

CN7724

6 TYPEC_TX1P — C206 0.1U/10V_2 — TYPEC_TX1P_C — A2 SSTXp1
6 TYPEC_TX1N — C202 0.1U/10V_2 — TYPEC_TX1N_C — A3 SSTXn1
6 TYPEC_RX1P — C20698 0.1U/10V_2 — TYPEC_RX1P_C — B11 SSRXp1
6 TYPEC_RX1N — C20699 0.1U/10V_2 — TYPEC_RX1N_C — B10 SSRXn1
VBUS#1 VBUS#2 VBUS#3 VBUS#4 — A4 B4 A9 B9 — +TYPEC_VBUS — 3A

6 TYPEC_TX2P — C243 0.1U/10V_2 — TYPEC_TX2P_C — B2 SSTXp2
6 TYPEC_TX2N — C246 0.1U/10V_2 — TYPEC_TX2N_C — B3 SSTXn2
6 TYPEC_RX2P — C20700 0.1U/10V_2 — TYPEC_RX2P_C — A11 SSRXp2
6 TYPEC_RX2N — C20701 0.1U/10V_2 — TYPEC_RX2N_C — A10 SSRXn2
GND#1 GND#2 GND#3 GND#4 GND#6 NC#1 NC#2 GND#5 GND#8 GND#7 — A1 A12 B1 B12 2 5 6 1 4 3

6 USBP0+ — C20692 470P/50V_4 — R124630 15_1%_2 — USBP0+_RC — L7567 MCM2012B900GBE — USBP0+_C — A6 Dp1 — B6 Dp2
6 USBP0- — R124631 15_1%_2 — C20693 470P/50V_4 — USBP0-_RC — USBP0-_C — A7 Dn1 — B7 Dn2

CC1_CON — A5 CC1
CC2_CON — B5 CC2
TYPEC_SBU1 — A8 SBU1
TYPEC_SBU2 — B8 SBU2

TP6300 — TP20098 — D6300 EGA10402V05AH_0.2p — D6301 EGA10402V05AH_0.2p
020090HB024M51NZL

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SSD

2/26 : Change SSD conn for ME

5/8 Change CN1012 FP from "ngff-apci0107-p001a-75p-km" to "ngff-nfsm0-s6710-tp40-75p-km" for match ME DXF

2/21 : add MUX circuit

From CPU's SATA to MUX

From CPU's PCIe to MUX

U4300 CBTL02043ABQ

Sel = L --> CPU's SATA
Sel = H --> CPU's PCIe

2/21 : add SSD RST circuit

U9013 *TC7SH08FU(F)

D6542 BAT54AW-L

Q12510 2N7002K

CN4900
NASM0-S6701-TS40
DFHS75FR586
ngff-nfsm0-s6710-tp40-75p-km

NGFF MKEY

100 mils

Q4900 2N7002K

5/8 Change CN1012 FP from "ngff-as0bc26-s30be-7h-ke" to "ngff-nfse0-s6710-tph4-ke-smt" for match ME DXF

2/21 : Change WLAN power

Width: 100 mils

3/17 : Change WLAN conn for ME

Remove Net RF_LINK# and need check if Ra and Rb can be NI

CN1012
NFSE0-S6710-TP48

NGFF EKEY

2/21 : Del CNVi / add BT/RF OFF

Q5003 2N7002KDW

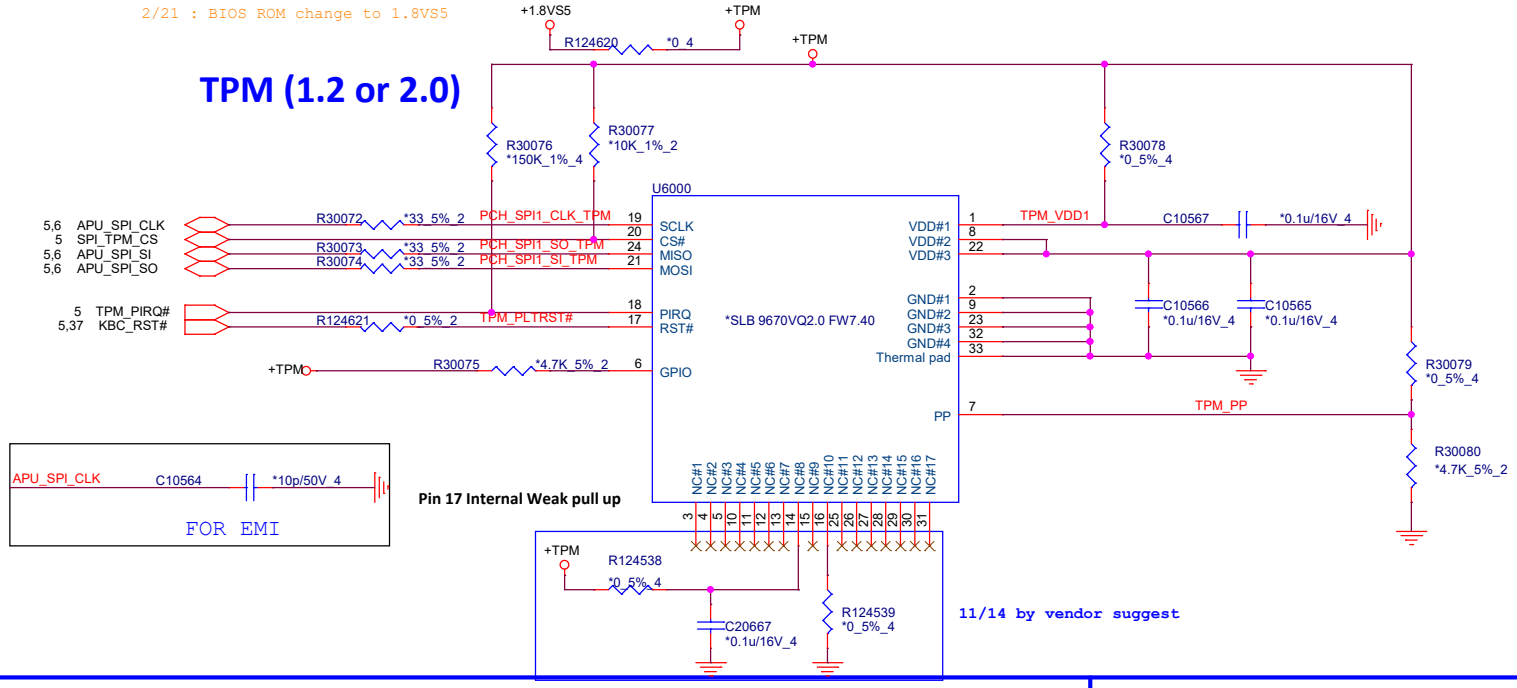
Support Wake Function(Reserve)

Q6005 *DRC5144E0L

Q6006 *2N7002K

2/21 : BIOS ROM change to 1.8VS5

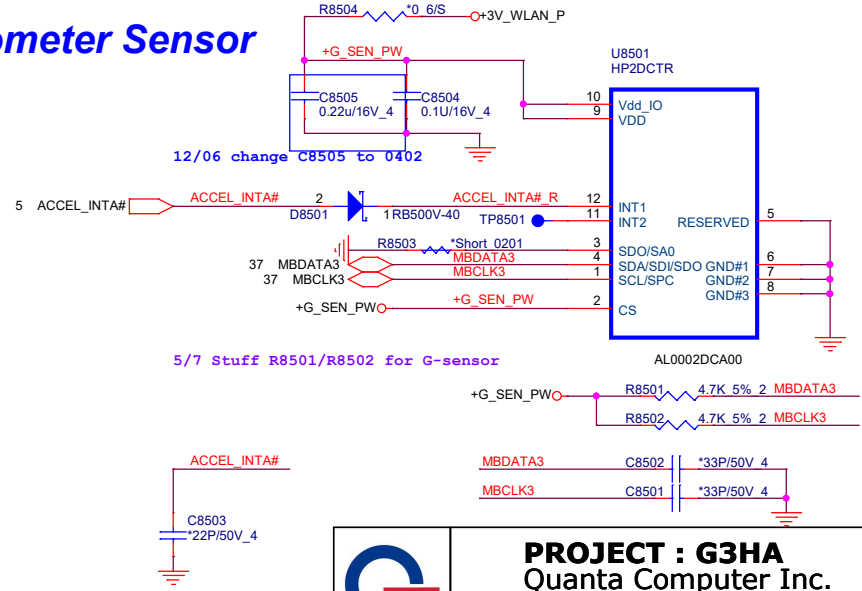
TPM (1.2 or 2.0)



IR CAM

2/13 : Del IR CAM

Accelerometer Sensor



NB5

PROJECT : G3HA
Quanta Computer Inc.

Size	Document Number	Rev
B	TPM/IR CAM/Sensor	1A
Date: Friday, June 21, 2019	Sheet 34 of 54	

LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff La, Ca ,Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

6/12 change L3000 FP to choke-lqh32pn4r7nn01

6/14 choke-lqh32pn4r7nn01已經取消換l3_2x2_5-2h

Power trace Layout 寬度> 60mil

>60mil >60mil

+1.05V_LAN_REGOUT L3000 4.7UH+-20%650MA_1210 +1.05V_LAN

La

Ca C3004 0.1U/16V_4

Cb C3005 4.7u/6.3VS_2

PIN3 Cc C3006 0.1U/16V_4

PIN8 Cd C3007 0.1U/16V_4

PIN30 Ce C3008 0.1U/16V_4

PIN22 Cf C3009 0.1U/16V_4

PIN22 Cg C3010 1u/6.3V_2

PIN22 Ch C3011 0.1U/16V_4

XTAL1 XTAL2 Y3000 25MHZ +-10PPM

C3000 12P/50V_4 C3001 12P/50V_4

5/13 C3000/C3001 chnage to 12P for vendor recommend

LAN_AMBLED# TP3000

LAN_LED1 TP3001

LED2 TP3002

+1.05V_LAN R3001 2.49K_1%_2

+3V_LAN

LAN_AMBLED# Ra R3003 *Short_0201 LAN_WLED#

R3004 *0_4 LAN_WLED# Rb

+3V R3002 1K_5%_2 ISOLATEB R3005 15K_1%_2

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

For GbE

* Place Ra

For 10/100

* Place Rb

5/15 U3000 change PN to AL008118002 network booster

U3000

Please add 9 GND VIAs connection with thermal PAD

GND 33

RSET 31 XTAL2 30 XTAL1 29 LAN_LED1 28 LED0 27 LED1/GPO 26 LED2(LED1) 25

AVDD33 32 RSET AVDD10#2 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2(LED1)

MDI0+ 1 MDI0- 2 MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10#1 3 4 5 6 7 8

+1.05V_LAN +1.05V_LAN

RTL8107ESH-CG

REGOUT(NC) 24 +1.05V_LAN_REGOUT

VDDREG(VDD33) 23 +3V_LAN

DVDD10(NC) 22 +1.05V_LAN

LANWAKEB 21 PCIE_WAKE# R R3006 *Short_0201 PCIE_WAKE# 5,33

ISOLATEB 20 ISOLATEB

PERSTB 19

HSON 18 PCIE_RXN4_LAN_C C3002 0.1U/16V_4 PCIE_RXN4_LAN 2

HSOP 17 PCIE_RXP4_LAN_C C3003 0.1U/16V_4 PCIE_RXP4_LAN 2

PCIE_RST# 4,5,19,33

MDIP3(NC) 9 MDIN3(NC) 10 AVDD33(NC) 11 CLKREQB 12 HSIP 13 HSIN 14 REFCLK_P 15 REFCLK_N 16

RTL8111HSH-CG

For GbE

* Place RTL8111HSH-CG

For 10/100

* Place RTL8107ESH-CG

6/19 change LED3000 PN to BE0R0105Z00

+3VLANVCC R3017 360_4 LED3000 3P AMBER LED LAN_AMBLED#

VC3000 *AVLC5S_4

+3VLANVCC R3018 360_4 LED3001 3P WHITE LED LAN_WLED#

VC3001 *AVLC5S_4

MDI3+ MDI3-

+3V_LAN

5 PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN#

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN4_LAN PCIE_TXP4_LAN

CLK_PCIE_LANN 5 CLK_PCIE_LANP 5 PCIE_TXN4_LAN 2 PCIE_TXP4_LAN 2

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3VLANVCC +3V_LAN

PIN11 C3013 0.1U/16V_4 Cj

PIN32 C3014 0.1U/16V_4 Ck

PIN11 C3015 *4.7U/6.3VS_2 Cm

PIN32 C3016 *4.7U/6.3VS_2 Cn

PIN23 C3017 4.7U/6.3VS_2 Co

PIN23 C3018 0.1U/16V_4 Cp

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp

For 10/100：Ua

For Giga：Ub

TRA_V_DAC C3022 0.01U/50V_4

1st source：NS681684 DB0LE6LAN20

2nd source：N-3110M DB0Y11LAN00

Ub

U3002

MDI2+ 2 MDI2- 3 MDI3- 5 MDI3+ 6 MDI0- 8 MDI0+ 9 MDI1- 11 MDI1+ 12

TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-

MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-

23 22 20 19 17 16 14 13

MDI2+_1 MDI2-_1 MDI3-_1 MDI3+_1 MDI0-_1 MDI0+_1 MDI1-_1 MDI1+_1

TRA_V_DAC 1 TRA_V_DAC 4 TRA_V_DAC 7 TRA_V_DAC 10 TRA_V_DAC 25

TCT1 TCT2 TCT3 TCT4 GND

MCT1 MCT2 MCT3 MCT4

24 21 18 15

LAN_MCTG0 Ra R3011 75/F_4

LAN_MCTG1 Rb R3012 75/F_4

LAN_MCTG2 Rc R3014 75/F_4

LAN_MCTG3 Rd R3016 75/F_4

NS892407

For GiGA

BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb

For Giga：Ra,Rb,Rc,Rd

C3020 10P/3KV_1808

3/25 : Change LAN conn

RJ45

5/14 change RJ45 PN to DFTJ08FR625

R3013 *0_6/S

MDI3-_1 8 MDI3+_1 7 MDI1-_1 6 MDI2-_1 5 MDI2+_1 4 MDI1+_1 3 MDI0-_1 2 MDI0+_1 1

11 12 9 10

2RJ3010-108211F CN3000

R3015 *0_6/S

4,5,6,7,17,18,21,26,27,28,32,33,36,37,38,39,46,48,49,50,51,52,53 48 +3V +3VLANVCC

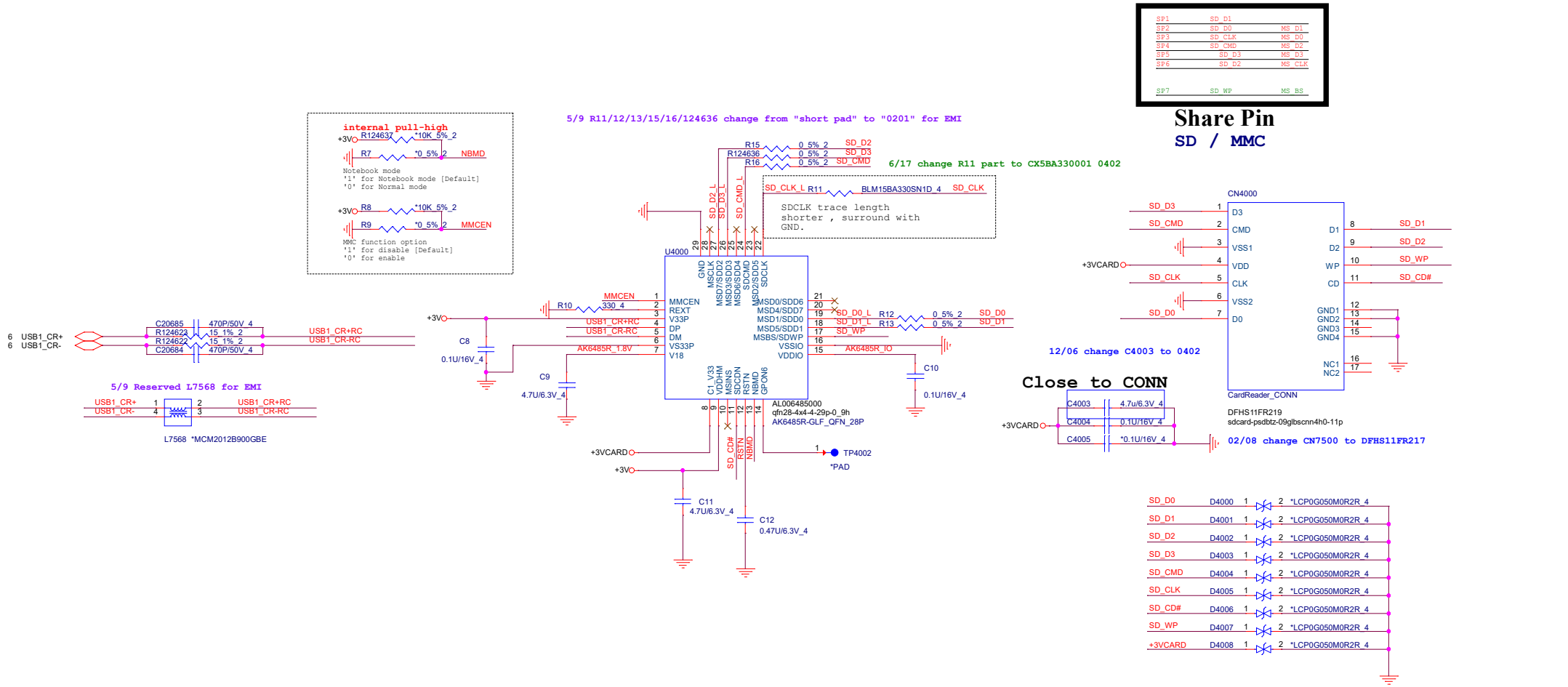
NB5

PROJECT : G3HA

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8107ESH-CG/RJ45	1A
Date: Friday, June 21, 2019	Sheet 35 of 54	

CardReader - AK6485



PROJECT : G3HA Quanta Computer Inc.			
NB5	Size: Custom	Document Number: CR AK6485RB63 / CR SOCKET	Rev: 1A
	Date: Friday, June 21, 2019	Sheet: 36 of 54	

Close to Pin 106

2/21 : Pin106 change to 1.8V

IT8987

LPC / GPIO / PS/2 / SM_BUS / UART / FLASH / PWM / KBMX / WAKE UP / A/D D/A / CLOCK

3/15 : change to BC1.2

3/5 : change to TP

3/17 : change to Type-C function

For Gsensor

For GPU thermal

for Battery charge/charge

for APU / DDR Thermmal IC

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

11/15 delete SUSWARN#_EC change to TPS

2/21 : change to TP

For Touch-Pad

5/14 add TP_INTH#_EC for EC requirement

2/26 : TS ON change to TP EN

Close to BIOS

5/13 add BIOS WP for EC (Pin17)

Open Drain need pu high

Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	N18E
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	N18P
135W	10K(CS31002FB26)	17.8K(CS31782FB10)	2.11V	N17P
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check

Change to 1SS355 as Current loss

3/17 : change to Type-C

5/13 remove R5133 double pull-up

CLOSE to EC Pin

For HW Throttling

3/6 : move to power page

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

4,5,6,7,17,18,21,26,27,28,32,33,35,36,38,39,46,48,49,50,51,52,53 +3V
4,5,6,7,23,32,33,39,42,43,44,48,53,54 +3VS5
6,7,30,32,33,38,41,42,54,55 +3VPCU

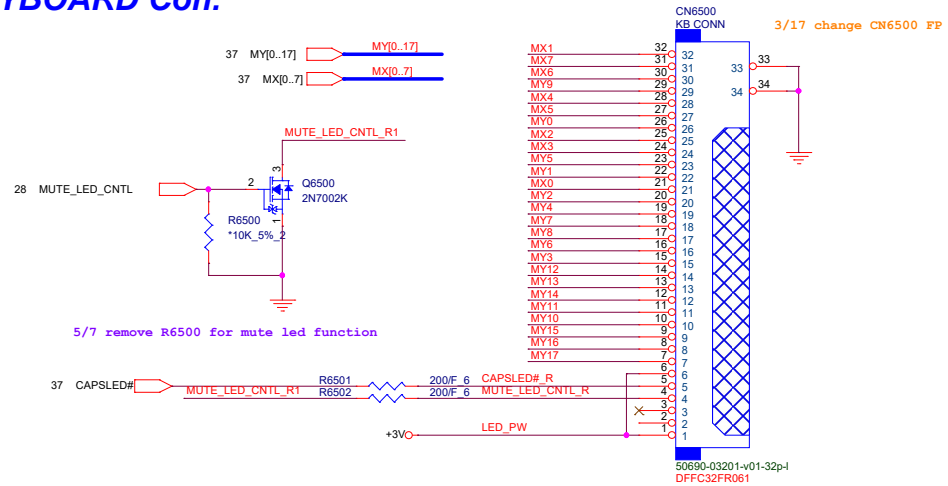
PROJECT : G3HA
Quanta Computer Inc.

NB5

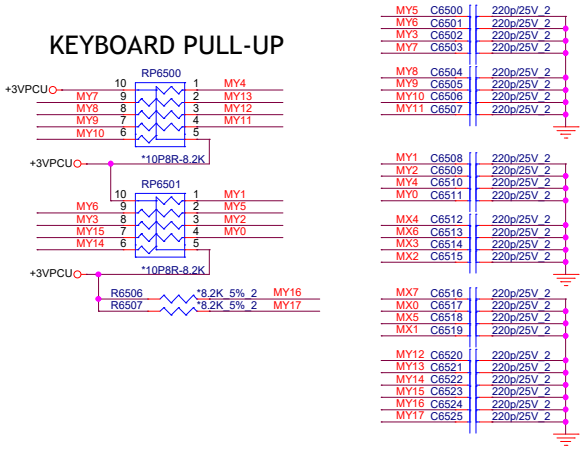
Size	Document Number	Rev
Custom	EC (IT8987)	1A

Date: Tuesday, June 25, 2019 Sheet 37 of 54

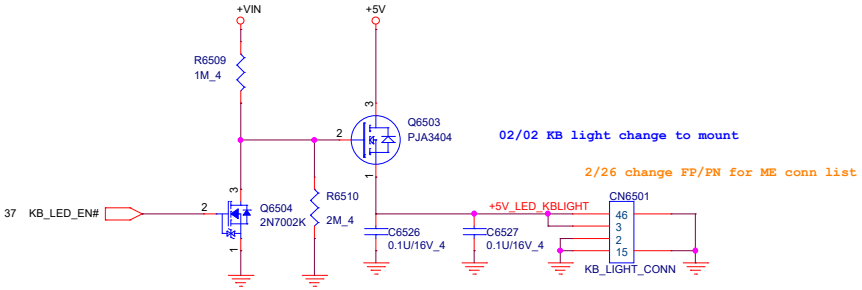
KEYBOARD Con.



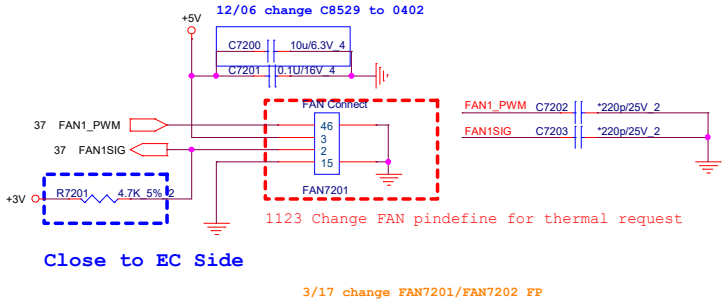
KEYBOARD PULL-UP

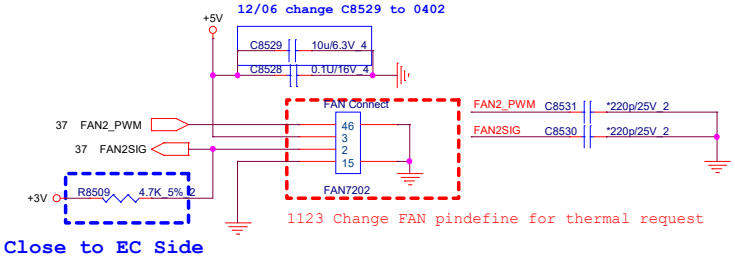


KB LIGHT CONN



FAN

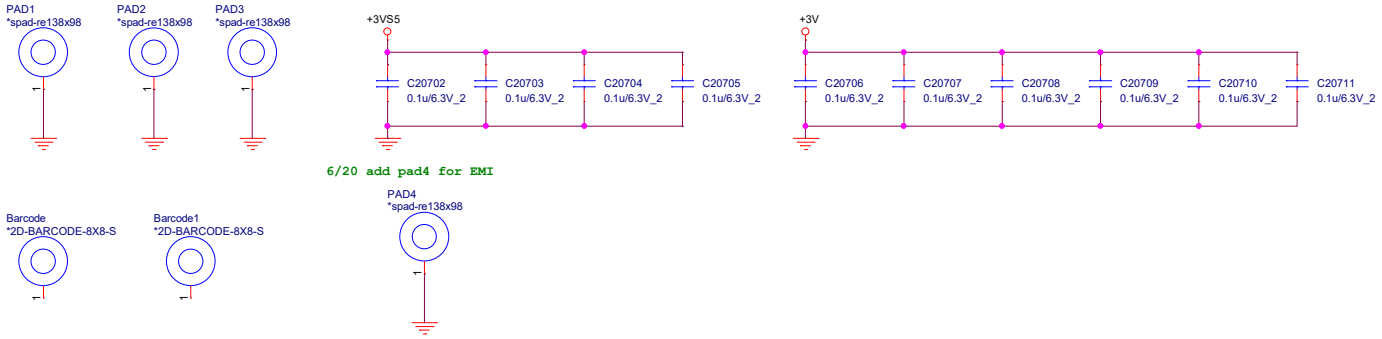




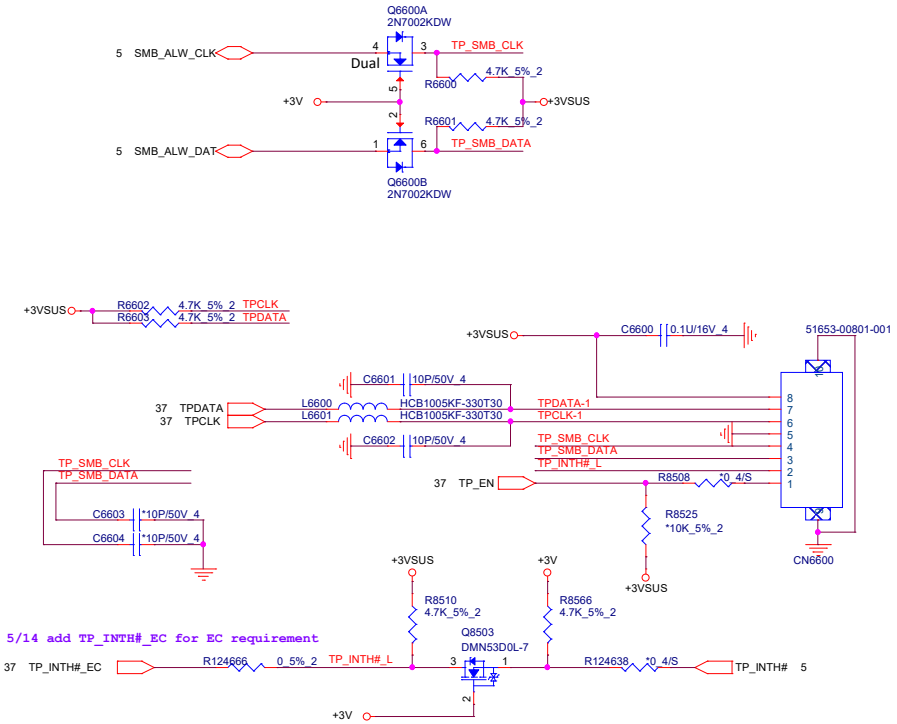
NB5	PROJECT : G3HA Quanta Computer Inc.	
Size: Custom	Document Number: KB/TP/FAN/HOLE	Rev: 1A
Date: Friday, June 21, 2019	Sheet 38 of 54	

RF Solution

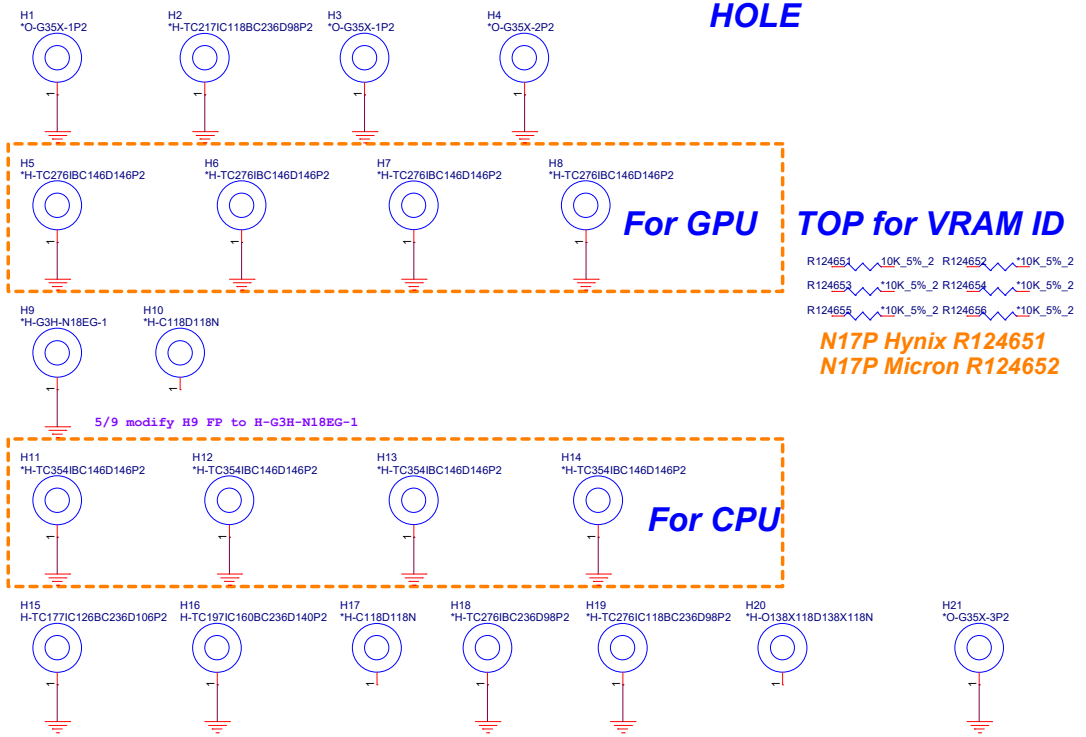
For EMI



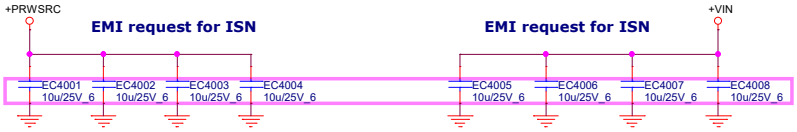
Touch Pad Connector



HOLE



NB5	PROJECT : G3HA Quanta Computer Inc.	
Size: Custom	Document Number: RF Solution	Rev: 1A
Date: Friday, June 21, 2019	Sheet 39 of 54	



PROJECT : G35P Quanta Computer Inc.		
Size: Custom	Document Number: RF Solution	Rev: 1A
Date: Friday, June 21, 2019	Sheet 40 of 55	

+3VPCU 6,7,30,32,33,37,38,42,54,55
+5VPCU 28,42,48,53
+PRWSRC 40
+BAT_RTC 7,30,55

Picaso 35W_N17P 40W N18P 50W 0403

150W/19.5V/7.6A

15.6"

CN1001
51280-01201-V01

PQ1004 AP0203GMT-HF
PQ1003 AP0203GMT-HF
PQ1002 AONS32314
PQ1001 AONS32314

PU1001 BQ24738HRGRR

PD1000 RB500V-40
PD1001 *PDZ5.6B
PD1002 P4SMAJ20A
PD1003 *P4SMAJ20A
PD1004 *PDZ5.6B
PD1005 RB500V-40
PD1006 *RB500V-40
PD1008 *PDZ5.6B
PD1009 BAS316
PD1010 BAS316

PQ1005 METR3904-G
PQ1007 AON7408
PQ1008 METR3904-G
PQ1009 2N7002K
PQ1000 2N7002K
PQ3 *2N7002K
PQ72 *METR3904-G

BAT1001
51437-0120T-V01

Place this cap close to EC

Place this ZVS close to Diode away +VIN

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

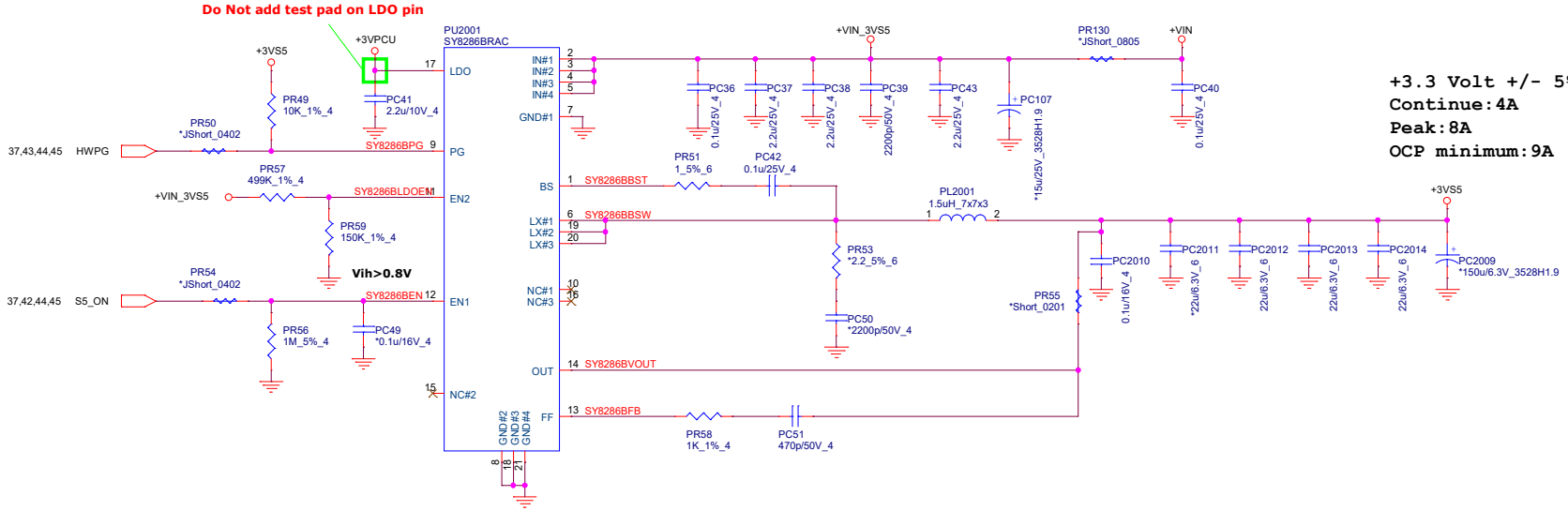
Place this R&C close to EC

MIN. BATV=7.2V

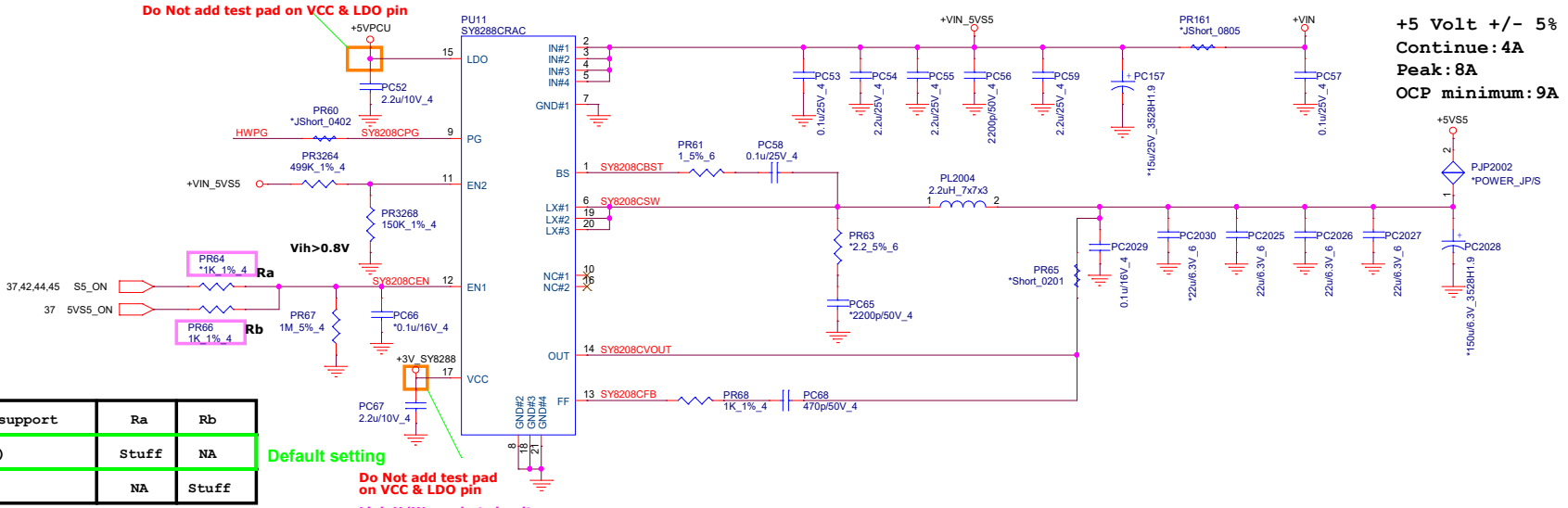
Setting MAX Icharge to 5A

PROJECT : G35P	
Quanta Computer Inc.	
Size: Custom	Document Number: Charger (BQ24738H)
Rev: 1A	
Date: Friday, June 21, 2019	Sheet: 41of 55

+VIN 26,38,40,41,43,44,46,47,48,52
+3VS5 4,5,6,7,23,32,33,37,39,43,44,48,53,54
+5VS5 28,30,32,43,44,45,46,47,48,49,52,53
+3VPCU 6,7,30,32,33,37,38,41,54,55
+5VPCU 28,41,48,53



+3.3 Volt +/- 5%
Continue:4A
Peak:8A
OCP minimum:9A



+5 Volt +/- 5%
Continue:4A
Peak:8A
OCP minimum:9A

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Default setting

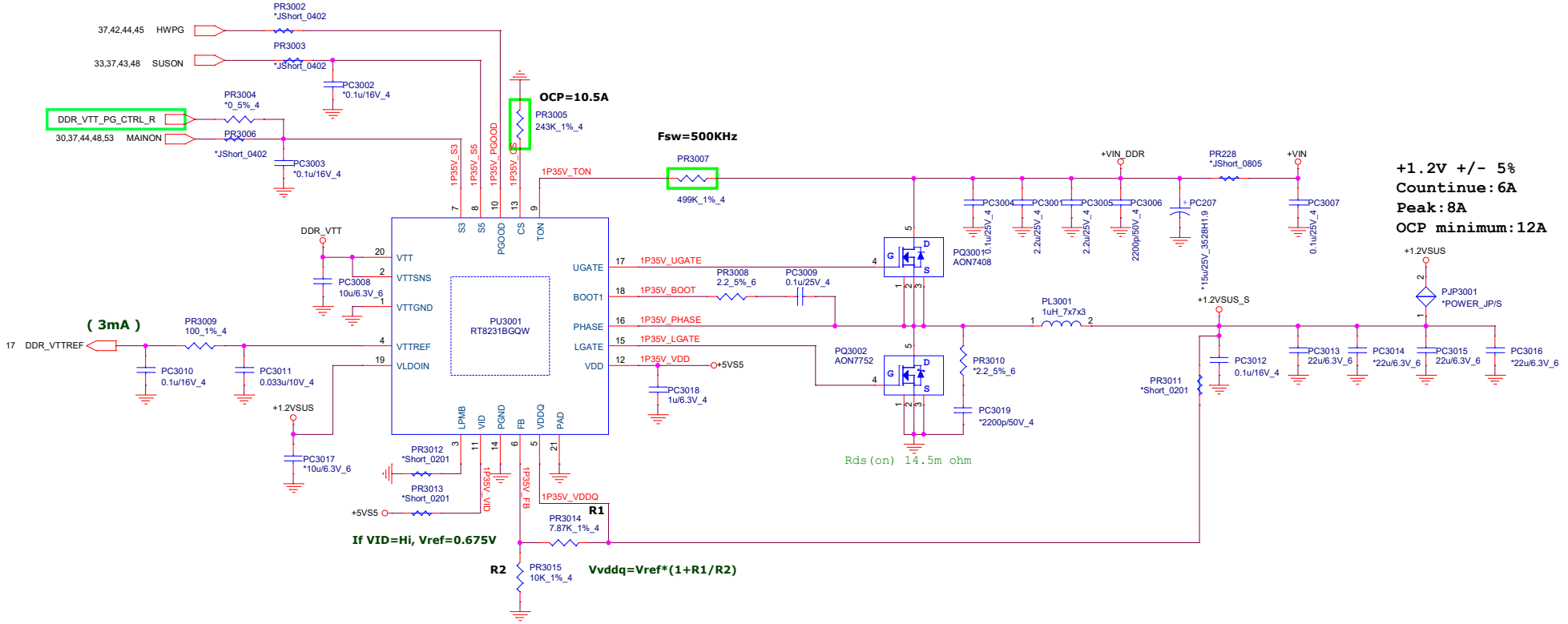
Do Not add test pad on VCC & LDO pin

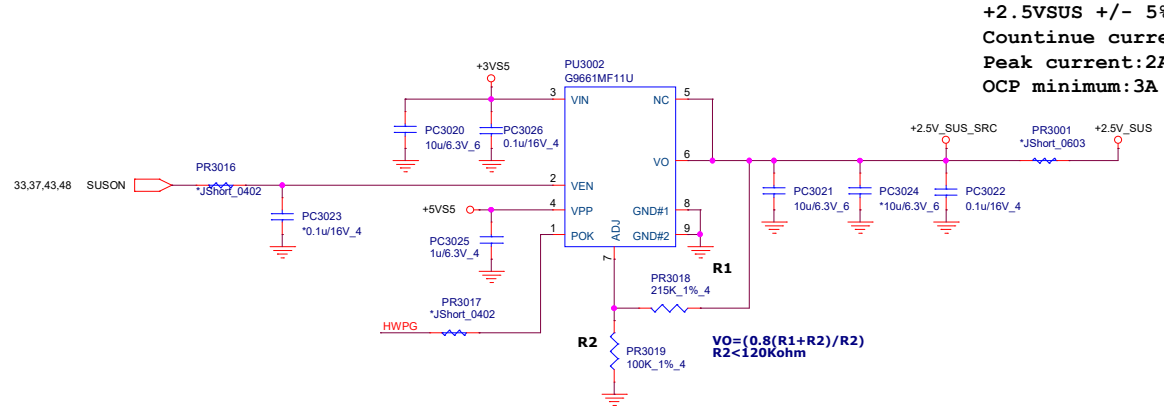
Link H/W prochot circuit

3VCC is to make use of internal driver 10mA maximum when heavy loading (internal current limit is 15mA typ.)

PROJECT : G35P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Friday, June 21, 2019	Sheet 42 of 55	





+VIN 26,38,40,41,42,44,46,47,48,52
+5VS5 28,30,32,42,44,45,46,47,48,49,52,53
+1.2VSUS 7,17,18
DDR_VTT 17,18
+2.5V_SUS 17,18

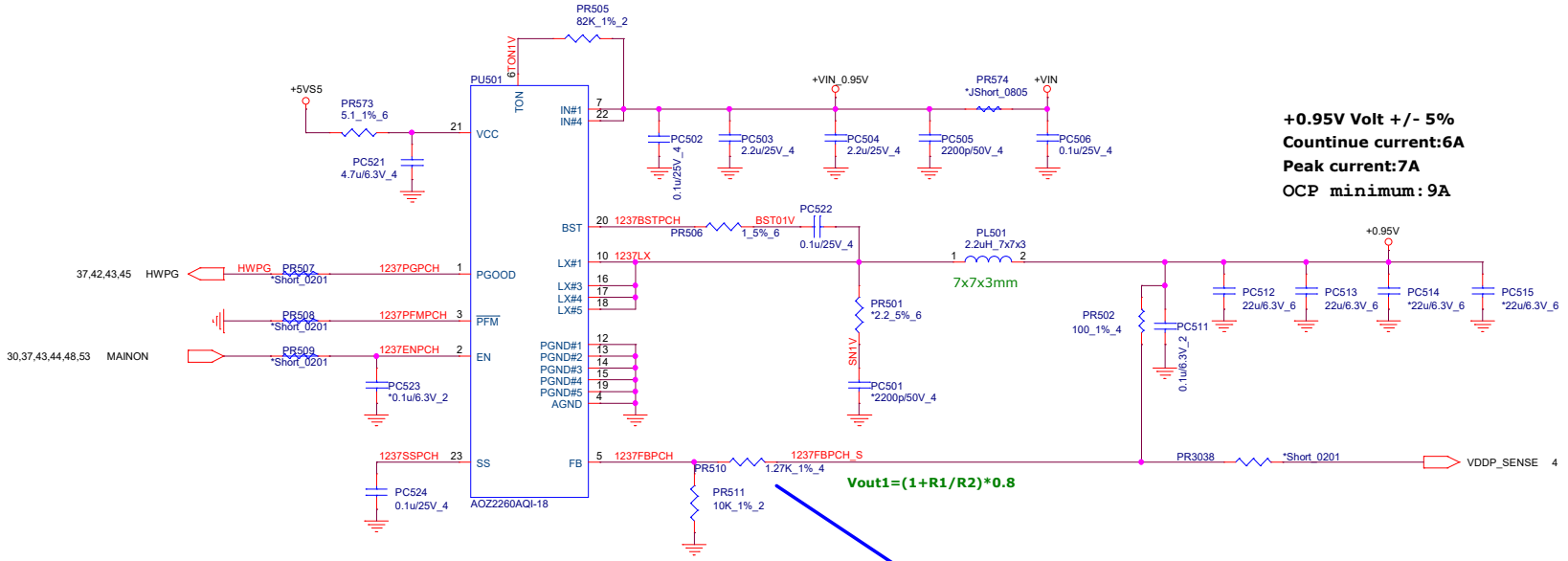
PROJECT : G35P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR4 (RT8231B)	1A
Date: Friday, June 21, 2019	Sheet 43 of 55	

+VIN 26,38,40,41,42,43,46,47,48,52
+3VS5 4,5,6,7,23,32,33,37,39,42,43,48,53,54
+5VS5 28,30,32,42,43,45,46,47,48,49,52,53
+0.95V 4,7,37
+1.8VS5 4,5,6,7,34,45,48,53
MAINON 30,37,43,44,48,53

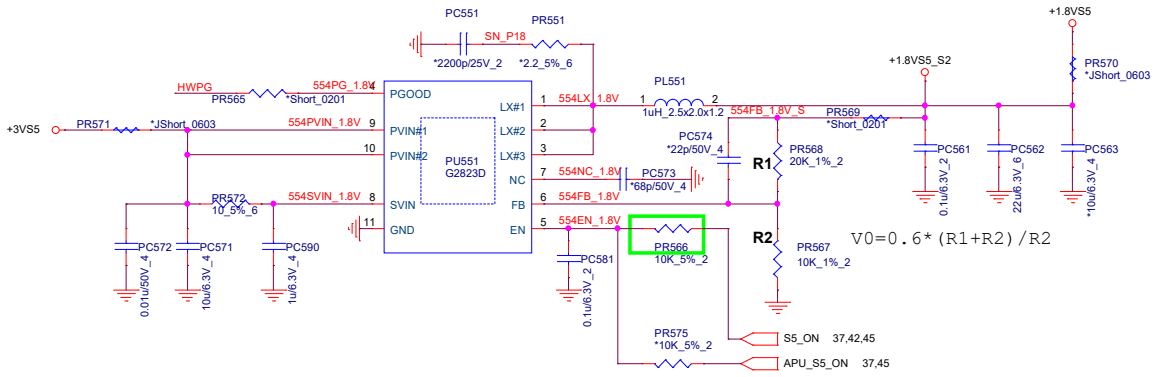
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

+0.95V Volt +/- 5%
Countinue current:6A
Peak current:7A
OCP minimum: 9A



	R1		
Raven	1.27K	CS21272FB15	0.9V
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V

1.8VS5 +/- 3%
TDC: 3A
EDP: 4A



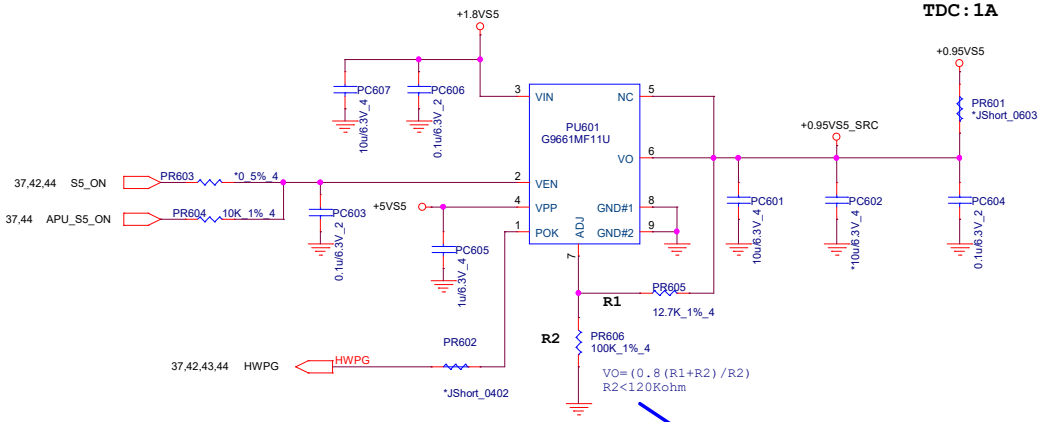
PROJECT : G7C
Quanta Computer Inc.

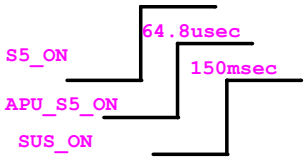
BU5

Size	Document Number	Rev
Custom	+0.95V/+1.8VS5	1A

Date: Friday, June 21, 2019 Sheet 44 of 55

+0.95V +/- 5%
TDC:1A





	R1		
Raven	12.7K	CS31272FB17	0.9V
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V
Stoney VDDP=0.95V

NB5

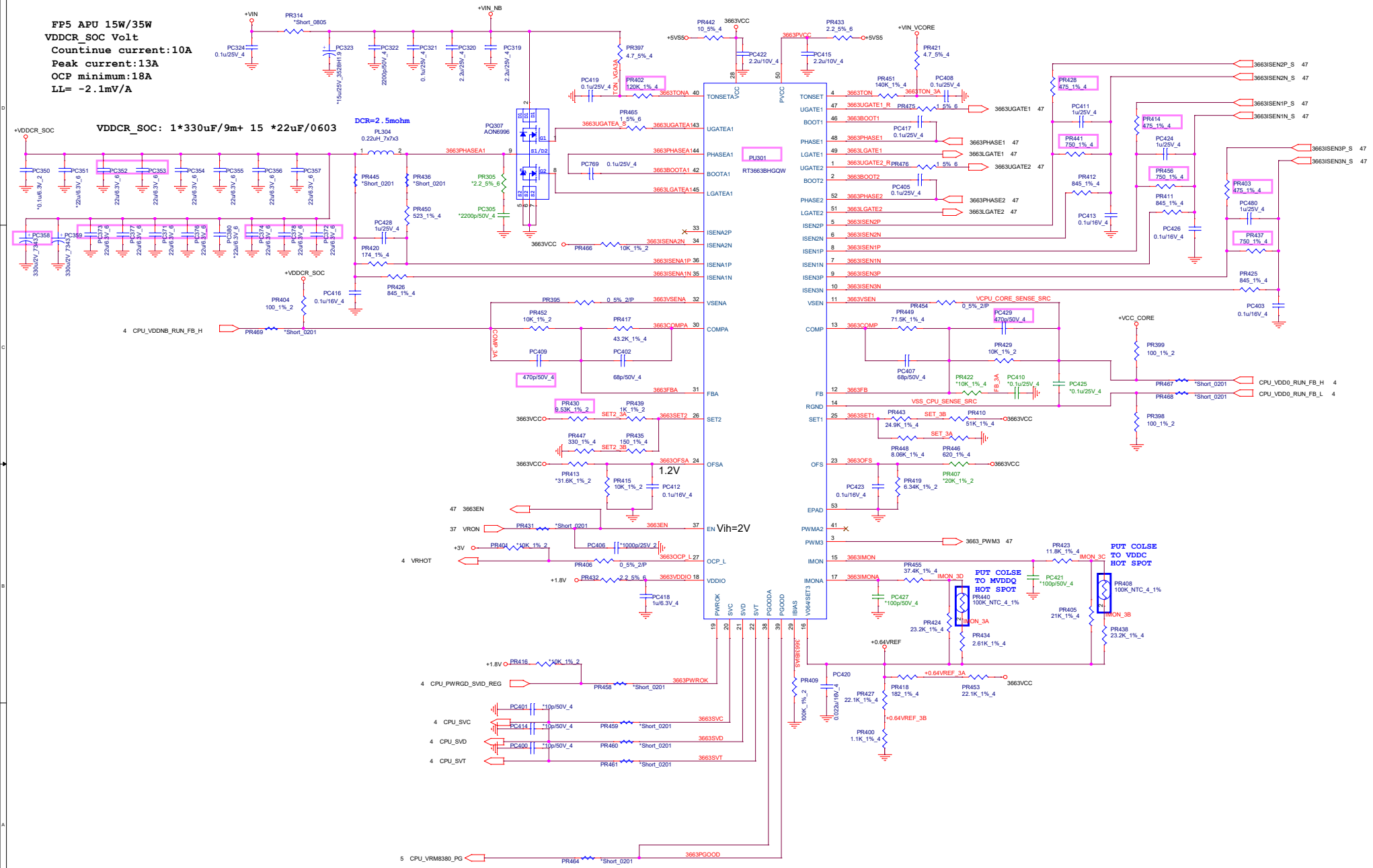
PROJECT : G7CE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+0.95VS5	1A

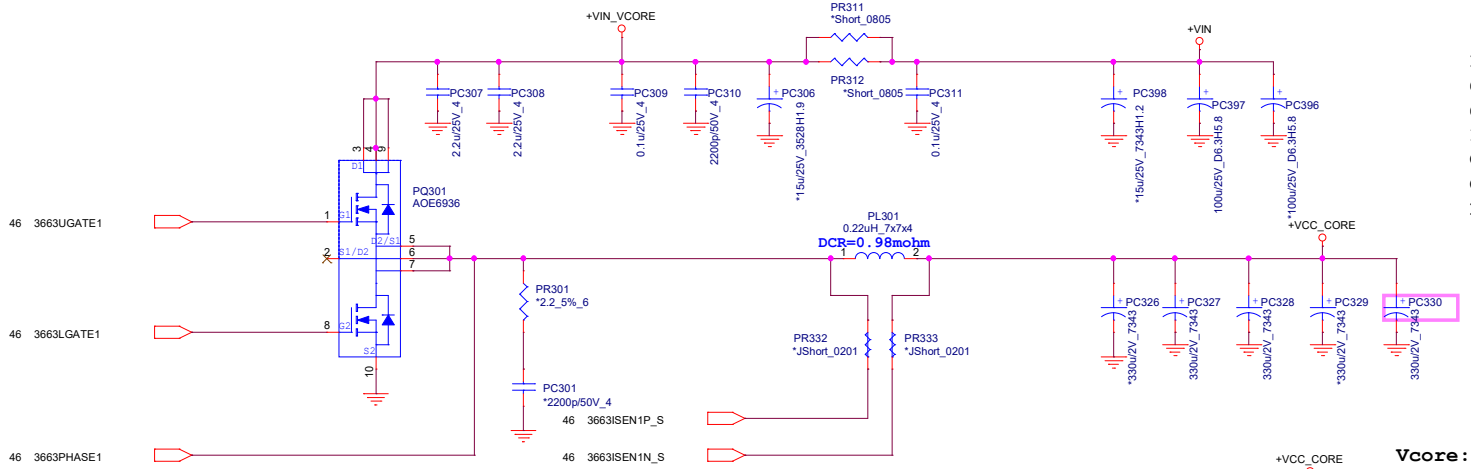
Date: Friday, June 21, 2019 Sheet 45 of 55

FP5 APU 15W/35W
VDDCR_SOC Volt
Countinue current:10A
Peak current:13A
OCP minimum:18A
LL= -2.1mV/A

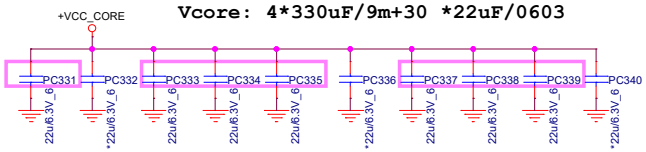
VDDCR_SOC: 1*330uF/9m+ 15 *22uF/0603

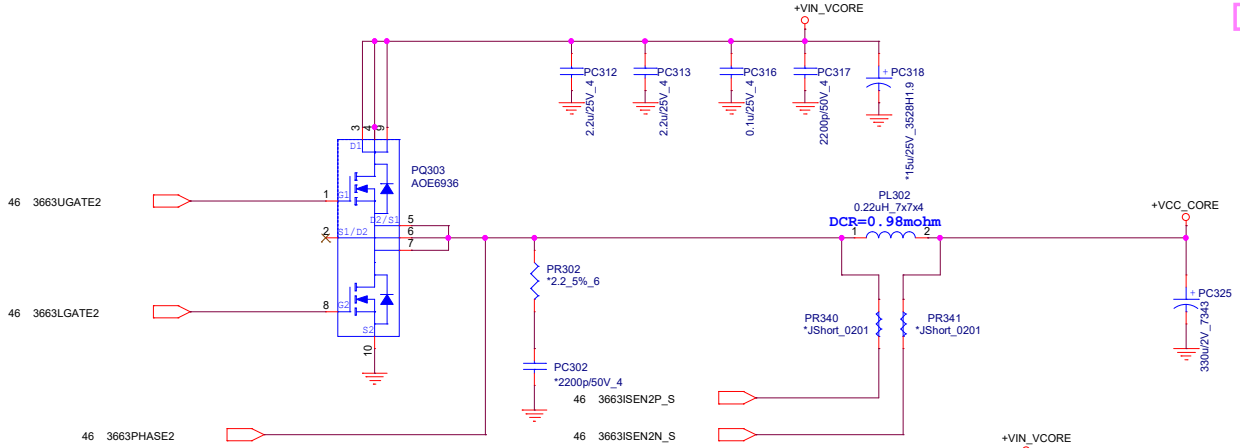


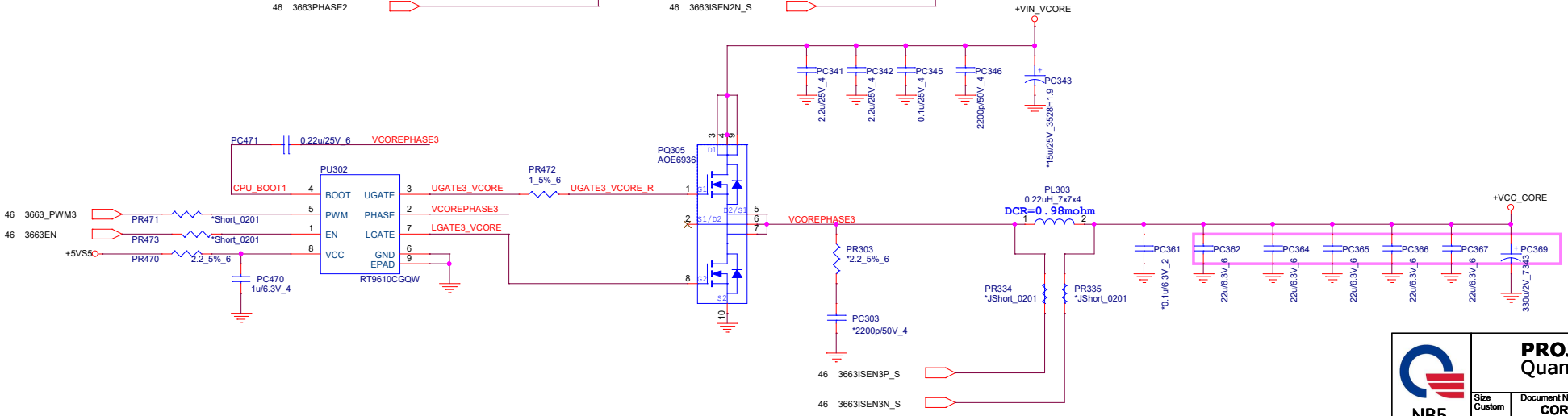
FP5 APU 35W
CPU CORE Volt
Countinue current:53A
Peak current:70A
OCP_TDC:90A
OCP_SPIKE:120A
LL= -0.7mV/A



Vcore: 4*330uF/9m+30 *22uF/0603





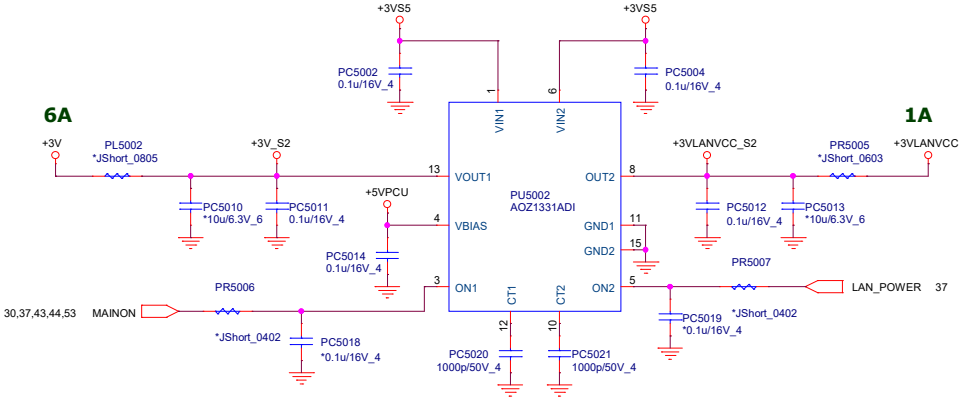


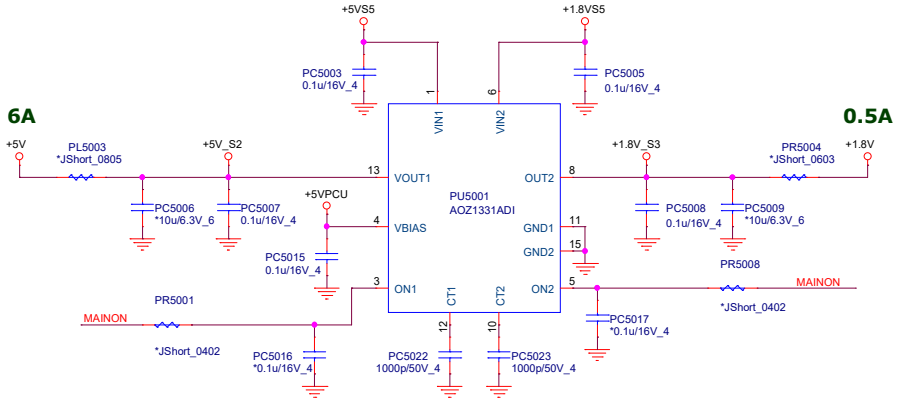
PROJECT : G7BF
Quanta Computer Inc.

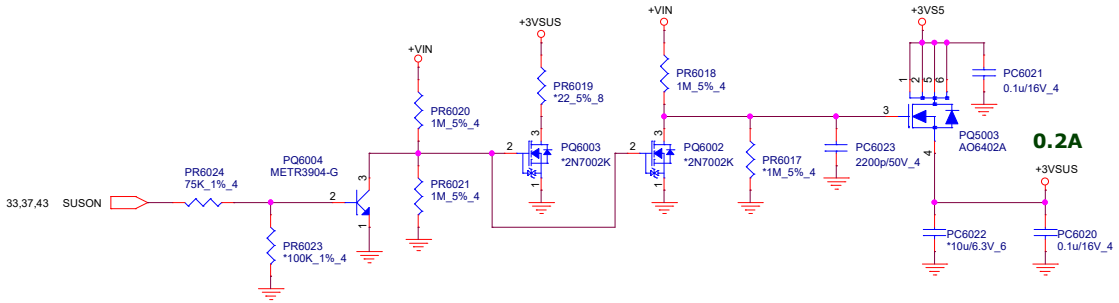
NB5

Size	Document Number	Rev
Custom	CORE_NB2	1A
Date: Friday, June 21, 2019	Sheet 47 of 55	

+3V 4,5,6,7,17,18,21,26,27,28,32,33,35,36,37,38,39,46,49,50,51,52,53
+5V 26,27,28,32,38,54
+3VS5 4,5,6,7,23,32,33,37,39,42,43,44,53,54
+5VS5 28,30,32,42,43,44,45,46,47,49,52,53
+3VSUS 39
+3VLANVCC 35

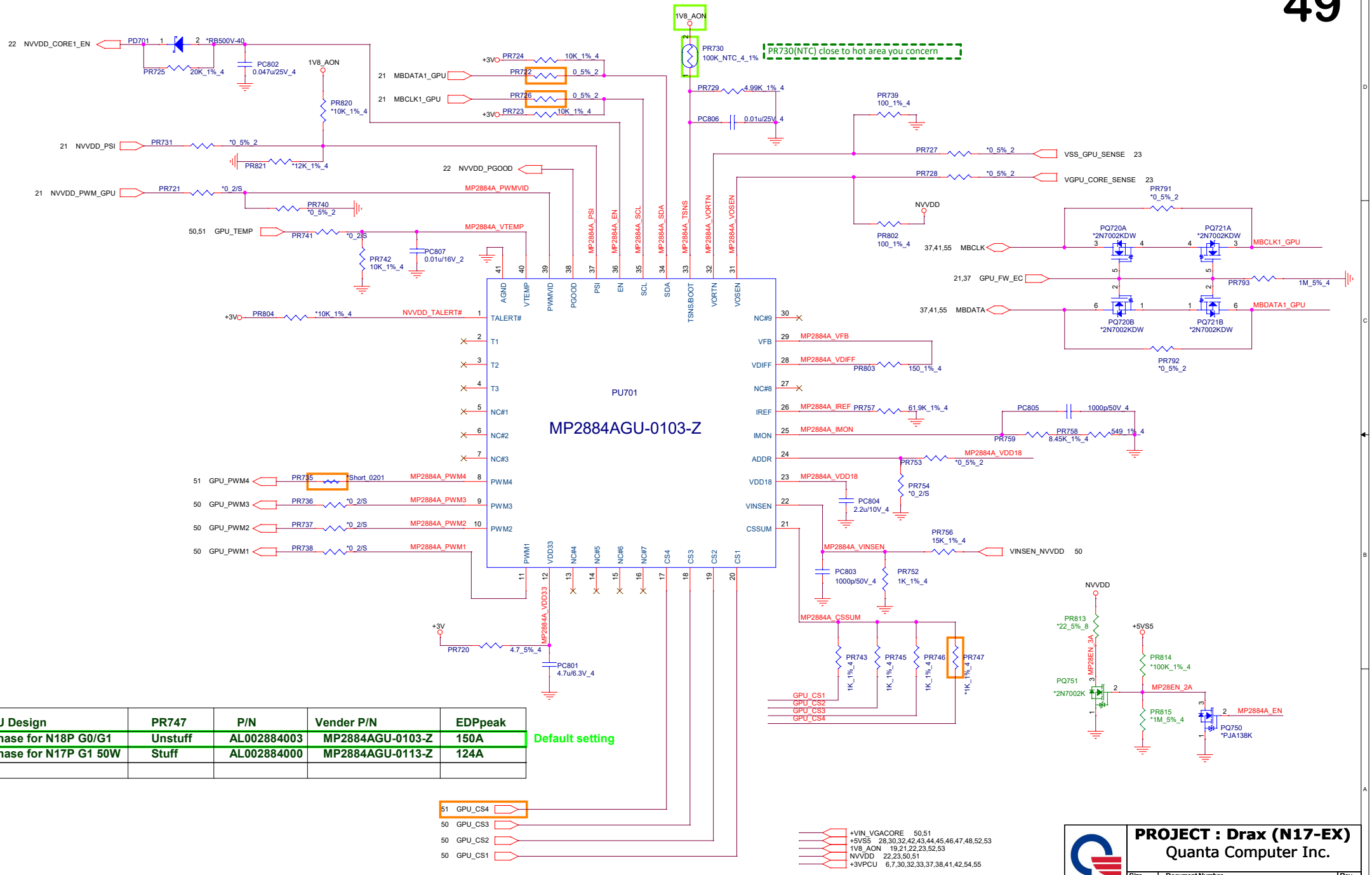






PROJECT : G35P
Quanta Computer Inc.

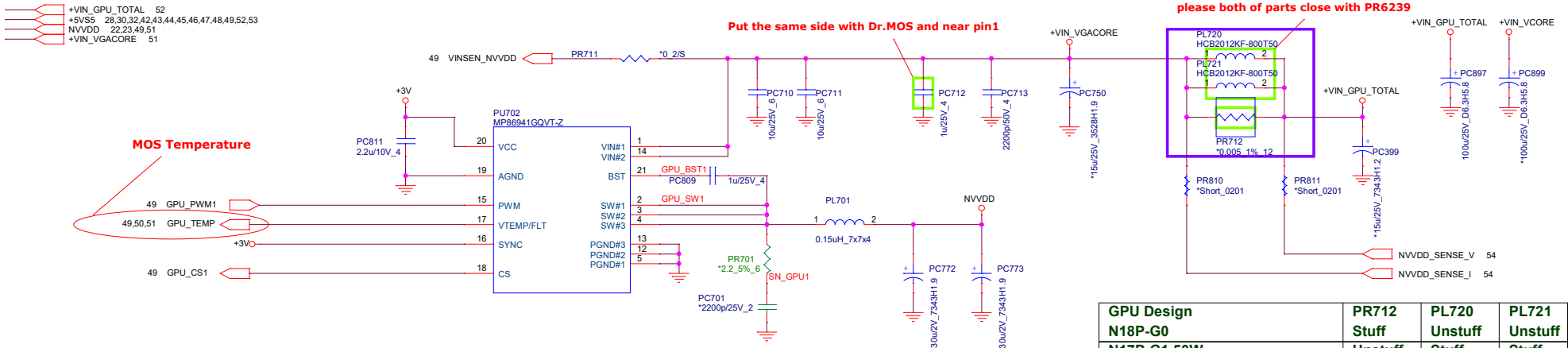
Size	Document Number	Rev
Custom	Load switch IC (AOZ1331D)	1A
Date: Friday, June 21, 2019	Sheet 48 of 55	



GPU Design	PR747	P/N	Vender P/N	EDPpeak
3 Phase for N18P G0/G1	Unstuff	AL002884003	MP2884AGU-0103-Z	150A
4 Phase for N17P G1 50W	Stuff	AL002884000	MP2884AGU-0113-Z	124A

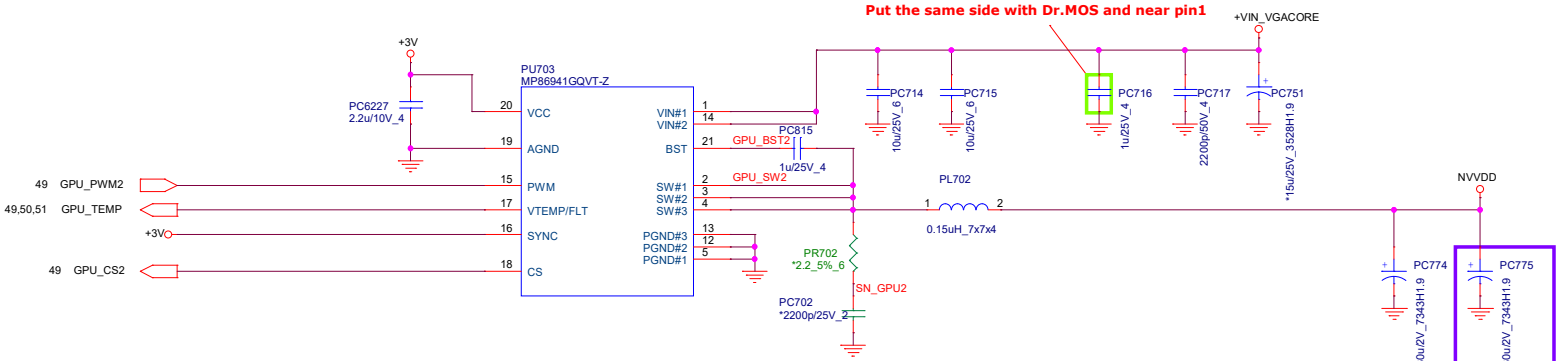
Default setting

NB5	**PROJECT : Drax (N17-EX)** Quanta Computer Inc.	
	Size: Custom — Document Number: +VGACORE (MP2884AGU)	Rev: 1A
	Date: Friday, June 21, 2019	Sheet 49 of 55



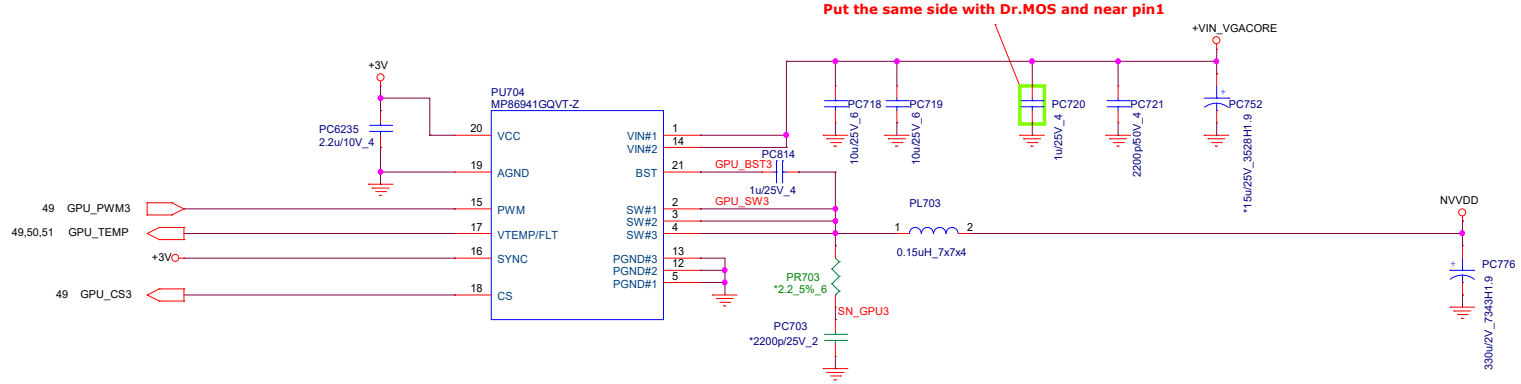
GPU Design	PR712	PL720	PL721	SPCAP
N18P-G0	Stuff	Unstuff	Unstuff	3pcs
N17P-G1 50W	Unstuff	Stuff	Stuff	3pcs
N17P-G0 K1 / N17P-G0 40W	Unstuff	Stuff	Stuff	2pcs

Default setting



Default setting

```
N18P G0/G0 MaxQ/40W/29W
GPU CORE Volt
Cuntinue current:45A/35A
Peak current: 150A/6uSec.
OCP Minimum: 195A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS
```



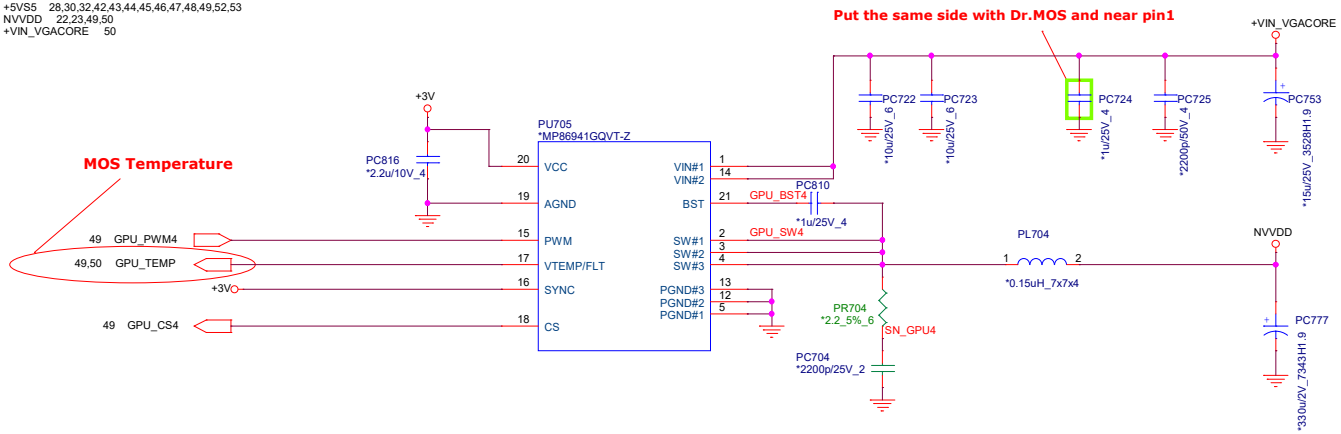

```
N17P-G1 (50W)-- support 4phase
N17P-G0 (40W) --support 3 phase
N17P-G0 K1(40W)--support 3phase
Cuntinue current:59A/50A/39A
Peak current: 124A/100A/111A
OCP Minimum: 160A/130A/140A
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS
```

NB5

PROJECT : Drax (N17-EX)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE (NCP81151)	1A
Date: Friday, June 21, 2019	Sheet 50 of 55	

+5VS5 28,30,32,42,43,44,45,46,47,48,49,52,53
NVVDD 22,23,49,50
+VIN_VGACORE 50

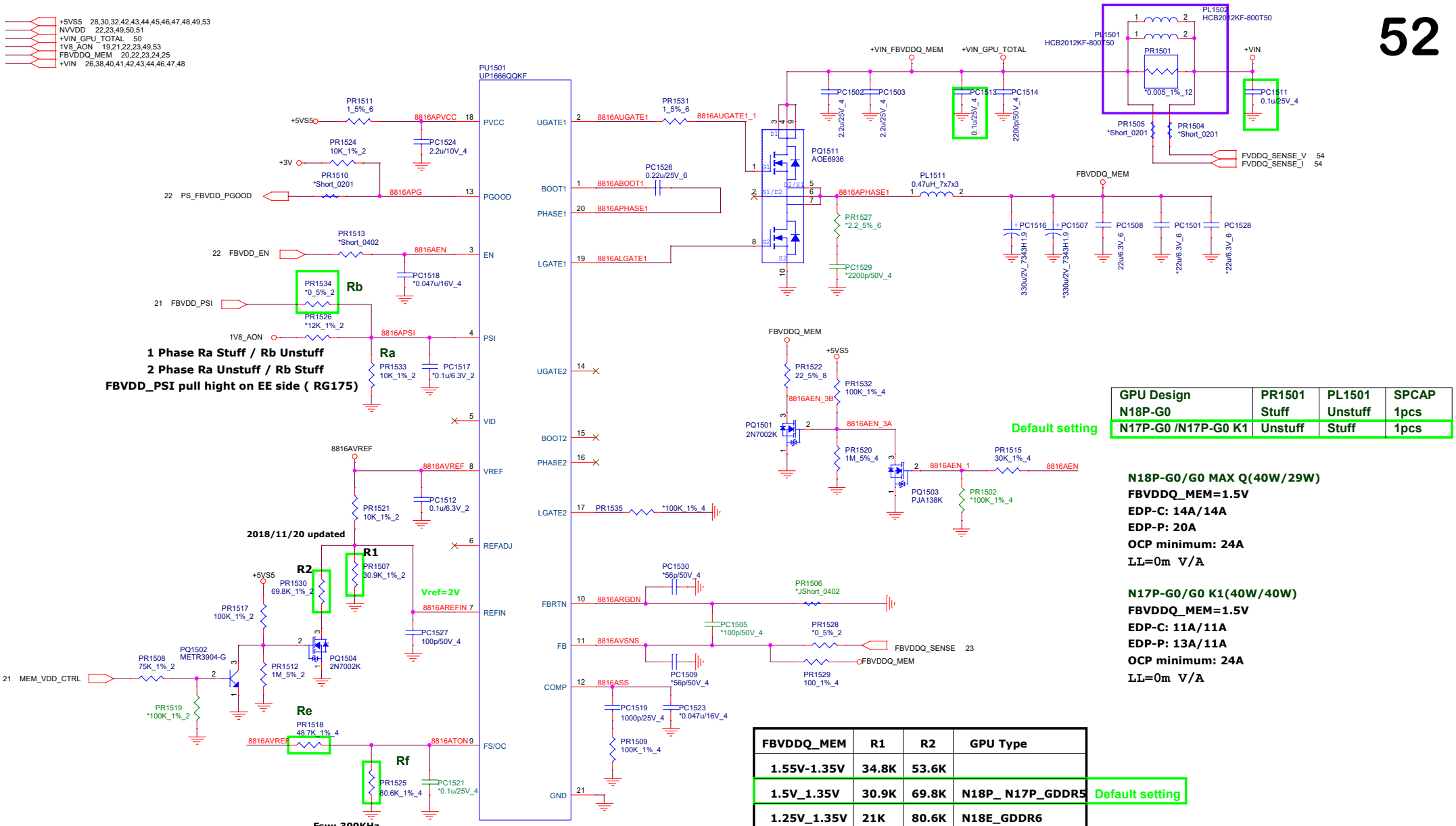


PROJECT : Drax (N17-EX)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCORE (NCP81151)	1A
Date: Friday, June 21, 2019	Sheet 51 of 55	

NB5

+5VS5 28,30,32,42,43,44,45,46,47,48,49,53
NVVDD 22,23,49,50,51
+VIN_GPU_TOTAL 50
1V8_AON 19,21,22,23,49,53
FBVDDQ_MEM 20,22,23,24,25
+VIN 26,38,40,41,42,43,44,46,47,48



1 Phase Ra Stuff / Rb Unstuff
2 Phase Ra Unstuff / Rb Stuff
FBVDD_PSI pull hight on EE side (RG175)

2018/11/20 updated

Vref=2V

Fsw: 300KHz

	Ra	Re	Rf	OCP
N18P G0 1-Phase	Stuff	48.7K	80.6K	25A
N18E G0 2-Phase	Unstuff	47.5K	78.7K	48A

Default setting

GPU Design	PR1501	PL1501	SPCAP
N18P-G0	Stuff	Unstuff	1pcs
N17P-G0 /N17P-G0 K1	Unstuff	Stuff	1pcs

Default setting

N18P-G0/G0 MAX Q(40W/29W)
FBVDDQ_MEM=1.5V
EDP-C: 14A/14A
EDP-P: 20A
OCP minimum: 24A
LL=0m V/A

N17P-G0/G0 K1(40W/40W)
FBVDDQ_MEM=1.5V
EDP-C: 11A/11A
EDP-P: 13A/11A
OCP minimum: 24A
LL=0m V/A

FBVDDQ_MEM	R1	R2	GPU Type
1.55V-1.35V	34.8K	53.6K	
1.5V_1.35V	30.9K	69.8K	N18P_ N17P_GDDR5
1.25V_1.35V	21K	80.6K	N18E_GDDR6
Fix 1.35V	21K	Open	
Fix 1.5V	30.1K	Open	

Default setting

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V_1.55V
0	1.35V

PROJECT : WBC
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	FBVDDQ_MEM(UP1666)	1A

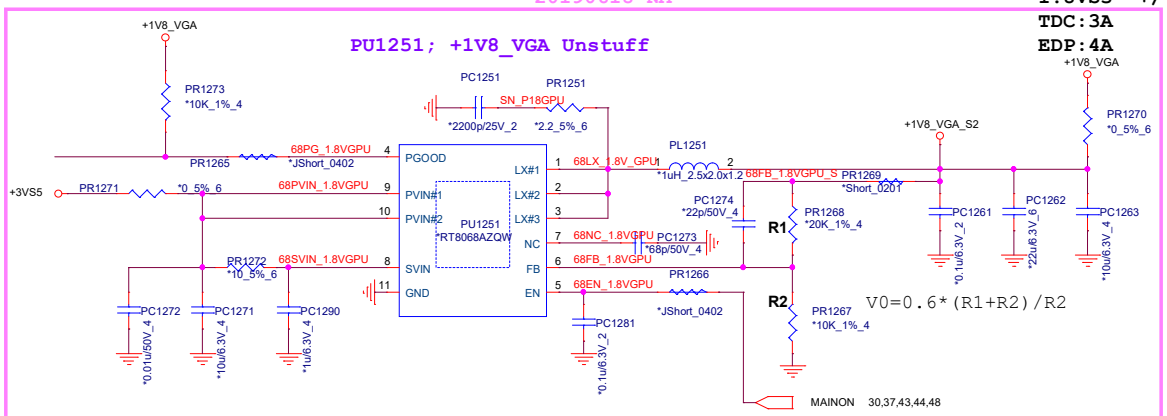
Date: Friday, June 21, 2019 Sheet 52 of 55

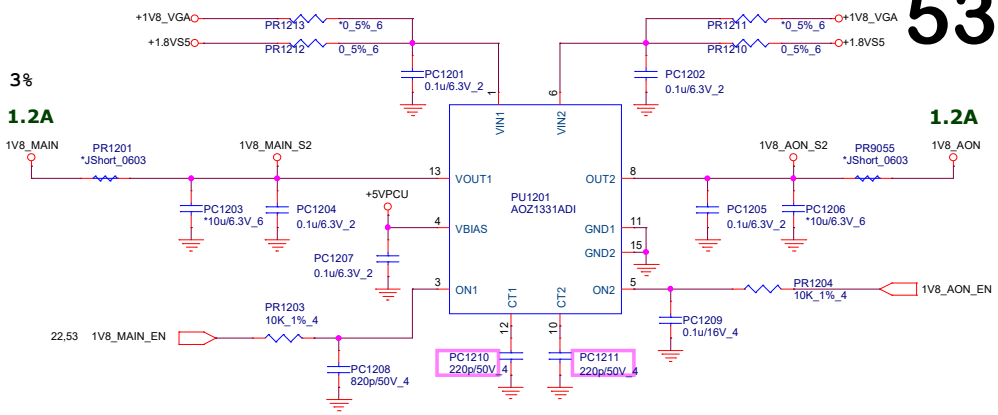
+VIN 26,38,40,41,42,43,44,46,47,48,52
+3VS5 4,5,6,7,23,32,33,37,39,42,43,44,48,54
+5VS5 28,30,32,42,43,44,45,46,47,48,49,52
1V8_MAIN 19,20,22,27
1V8_AON 19,21,22,23,49,52
+1.2VSUS 7,17,18,43
PEX_VDD 19,21

20190618-NA

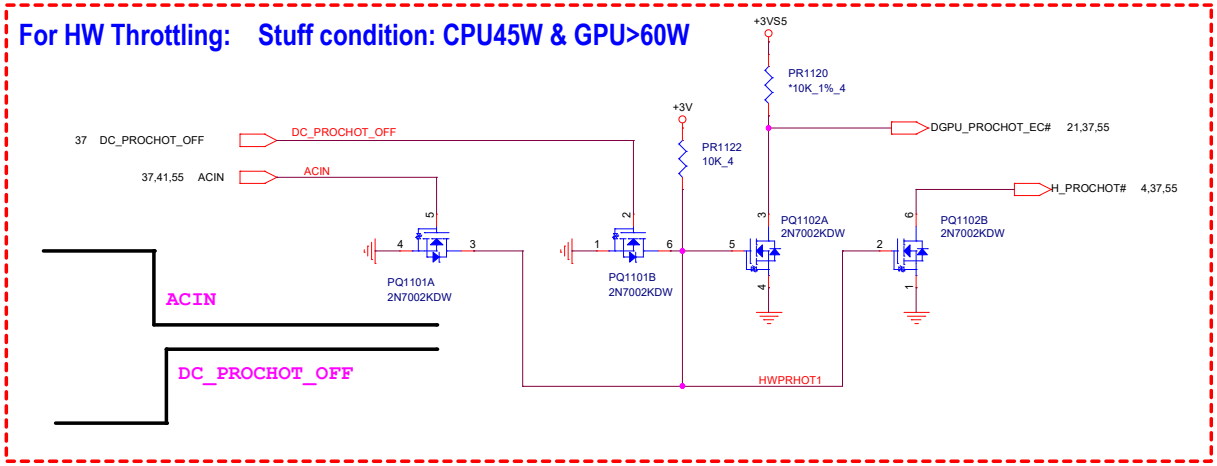
1.8VS5 +/- 3%
TDC:3A
EDP:4A
1.2A

PU1251; +1V8_VGA Unstuff



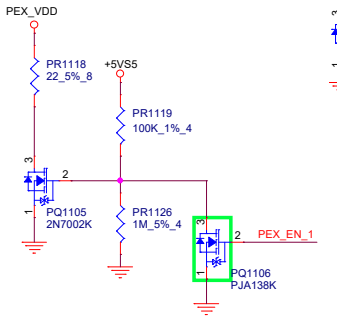


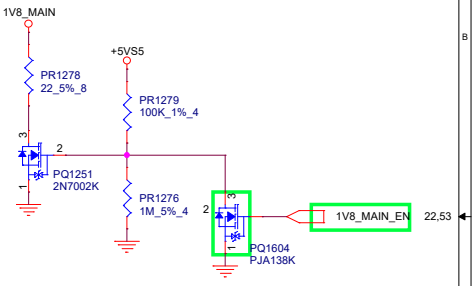
For HW Throttling: Stuff condition: CPU45W & GPU>60W



N18E-G0 MAX Q

+1.0V_GFX Volt +/- 5%
EDP=2.2A
EDP_peak = 2.6A





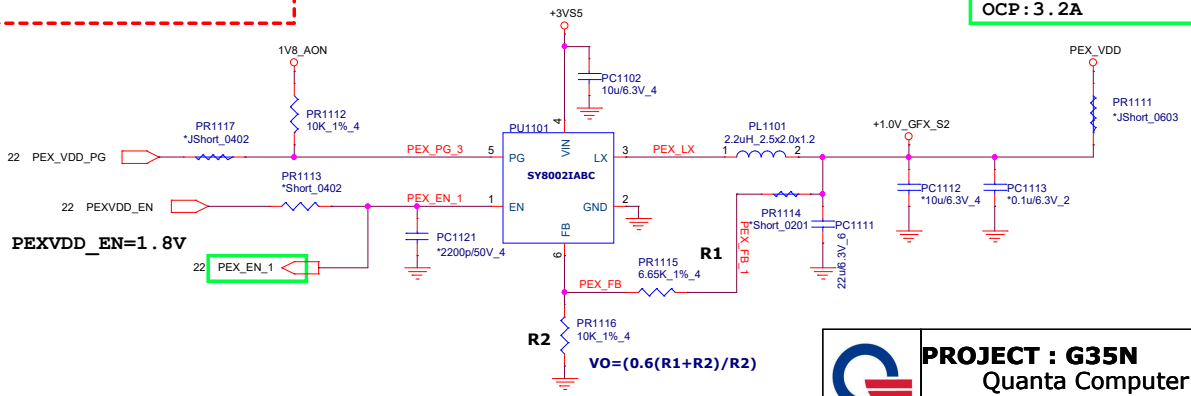
N18P-G0

+1.0V_GFX Volt +/- 5%
EDP=3.31A
EDP_peak = TBD

+1.0V_GFX +/- 5%
TDC:0.4A
EDP:1A
OCP:3.2A

N17P G0/G1

1V8_AON
1V8_MAIN
NVVDD
NVVDDS
PEX_VDD
FBVDDQ



NB5

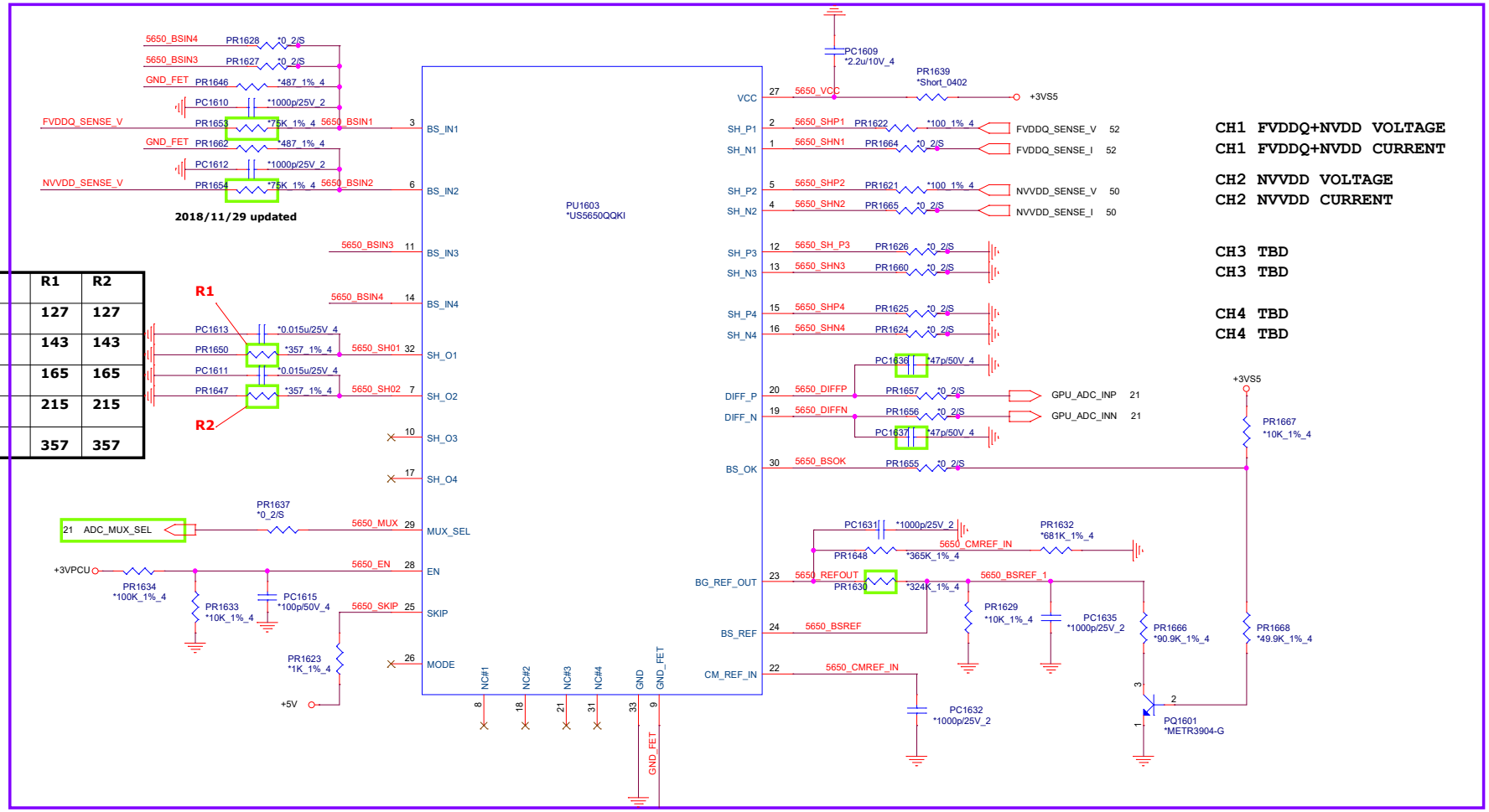
PROJECT : G35N
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(AOZ1331DI)	1A
Date: Friday, June 21, 2019	Sheet 53 of 55	

+3V 4,5,6,7,17,18,21,26,27,28,32,33,35,36,37,38,39,46,48,49,50,51,52,53

For N18P, N17P unstuff

UPI OVR Setting	R1	R2
N18E G3 (150W+)	127	127
N18E G2 (115W to 130W)	143	143
100W to 110W	165	165
N18E-G0,N18E-G1 (75W to 90W) N18E-G2 MaxQ,N18E-G3 MaXQ	215	215
N18P G0 N18P G0 MaxQ N18E G0 MaxQ (70W or Lower)	357	357



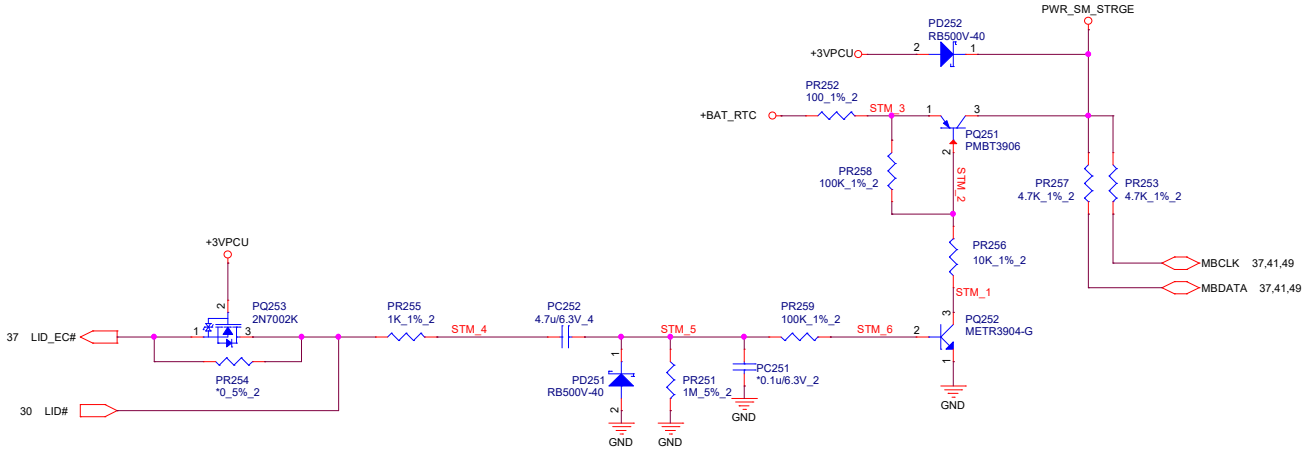
PROJECT : NLC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGAMON	1A

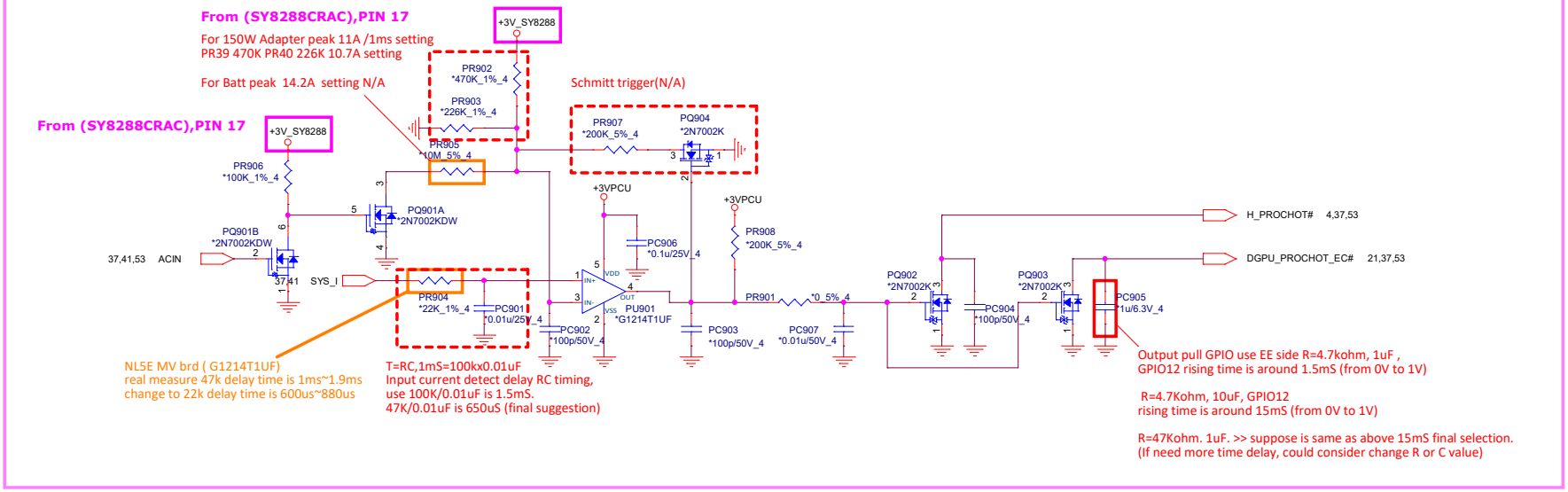
NB5

Date: Friday, June 21, 2019 Sheet 54 of 55

7,30,41 +BAT_RTC
6,7,30,32,33,37,38,41,42,54 +3VPCU



20190618-NA



PROJECT : G35P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	STORAGE MODE	1A
Date: Friday, June 21, 2019	Sheet 55 of 55	