PCB Number: 15133

PAGE	TITLE	
01	COVER PAGE_NTC	
02	BLOCK DIAGRAM	
03	CPU (PCIE/DMI)	
04	CPU (CFG/CLOCK/PM)	
05	CPU (DDR4 CHANNEL A)	
06	CPU (DDR4 CHANNEL B)	
07	CPU (DDI/EDP)	
08	CPU (CPU Power)	
09	CPU (VSS)	
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11	DDR DIMM_1	
12	DDR DIMM_2(R)	
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15	PCH (SPI/UART/I2C)	
16	PCH (DMI/PCI-E/USB)	
17	PCH (PCI-E/SATA)	
18	PCH (CLOCK/CL)	
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21	PCH (POWER)	
22	PCH Strap	
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24	SIO 6685D	
25	SPI&RTC	
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27	Audio Codec (ALC233/VB2)	
28	Audio DSP&AMP(R)	
29	Audio Jack (MIC/SPEA)(1/2)	
30	Audio Jack (function) (R)	
31	LAN 8111GN/F	
32	RJ45	
33	Card Reader_RTS5229	
34	USB Charger#	
35	USB redrive#(R)	
36	USB30 rear	
37	USB20 (BIOS RECOVERY)#(R)	
38	USB30 side	
39	USB20_REAR	
40	Power Plane EN Sequence	
41	Switch power-(R)	
42	Switch power-3V_S0/5V_S0	
43	ATX(BATT Conn)	
44	Power meter#	
45	DCDC-3D3V&5V(TPS51275)	
46	VCORE(NCP81102)	
47	VCORE OUTPUT(NCP81102)	
48	CPU Core_#(R)	
49	V_GT OUTPUT(NCP81151)	
50	VCCSA/VCCIO(NCP5230/TPS533)	
51	MEM/MEMVTT (NCP1589D)	
52	DCDC-1D05V(NCP1589D)	
53	PWR_12V(NCP1589A)	
54	LDO-& 1.5V & 1.2V	
55	LCD/Converter Connector	
56	HDMI	
57	DP_out#(R)	
58	DVI_#(R)	
59	Display switch_#(R)	
60	HDD&ODD	
61	Mini card-WLAN	
62	Mini card-SSD(R)	
63	Mini card-NGFF#(R)	
64	Converter board	
65	COM/CAM/TP/powerbutton/INT)	
66	DP IN/OUT (Repeater/SW)#(R)	
67	THERMAL SENSOR HEAD#(R)	
68	Debug_LPC	
69	4K Panel#(R)	
70	G Sensor#(R)	
71	Thunderbolt_(1/5)#(R)	
72	Thunderbolt_(2/5)#(R)	
73	Thunderbolt_(3/5)#(R)	
74	Thunderbolt_(4/5)#(R)	
75	Thunderbolt_(5/5)#(R)	

PAGE	TITLE	
76	GPU_function (1/5)#(R)	
77	GPU_function (2/5)#(R)	
78	GPU_function (3/5)#(R)	
79	GPU_function (4/5)#(R)	
80	GPU_function (5/5)#(R)	
81	GPU VRAM_1,2 (1/4)#(R)	
82	GPU VRAM_3,4 (2/4)#(R)	
83	GPU VRAM_5,6 (3/4)#(R)	
84	GPU VRAM_7,8 (4/4)#(R)	
85	GPU CORE_(solution)#(R)	
86	GPU discrete power#(R)	
87	GPU Switch_(1/2)#(R)	
88	GPU Switch_(2/2)#(R)	
89	GPU_others#(R)	
90	NFC#(R)	
91	TPM	
92	PS2/Parallel	
93	Express Card#(R)	
94	Smart Card#(R)	
95	SCALR DP703/PS8625	
96	MCU#(R)	
97	Intel LAN_#(R)	
98	LAN Switch_conn#(R)	
99	XDP&ITP(R)	
100	Label_RTC BATT	
101	GPIO table	
102	Power sequence	
103	Power delivery chart	
104	SMBUS table	
105	Clock MAP	
106	RESET Flow Chart	
107	Change History	

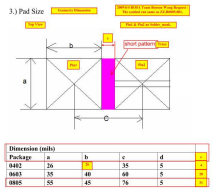
Design note:

10KR3	10K	R	3		
	value=10K	resistor	Size=0603		
SCD1U10V2	S	C	D1U	10V	2
	type=SMD	capacitor	value=0.1U	Withstang voltage=10V	Size=0402

Short-PAD:
0402=ZZ.00PAD.M11=0.65A
0603=ZZ.00PAD.M21=0.875A
0805=ZZ.00PAD.M31=1.375A

Size Current

BOM Configuration	BOM Configuration
(R_):Unmount	(LPT_):For parallel port
(X_):For debug	(TPM_):TPM function
(D_):Scalar DP703	(NTPM_):NO TPM function
(T_):Translater PS8625	(TCM_):TPM function
(UD_):USB debug	(NTCM_):NO TCM function
(C_):Changer function	
(NC_):No Changer function	
(SPI_):SPI BUS TPM	
(LPC_):LPC BUS TPM	
(COM_):For external COM PORT	



Dimension (mils)				
Package	a	b	c	d
0402	26	26	35	5
0603	35	40	60	5
0805	55	45	76	5

0805封裝尺寸/0402封裝尺寸/0603封裝尺寸/1206封裝尺寸
封裝尺寸與功率關係：封裝尺寸與封裝的對應關係

0201 1/20W	0402=1.0mmx0.5mm
0402 1/16W	0603=1.6mmx0.8mm
0603 1/10W	0805=2.0mmx1.2mm
0805 1/8W	1206=3.2mmx1.6mm
1206 1/4W	1210=3.2mmx2.5mm
	1812=4.5mmx3.2mm
	2225=5.6mmx6.5mm

TEST CONDITION FOR JUMPER (0W)

Item	WR12	WR08	WR06	WR04
Power Rating At 70° C	1/4W	1/8W	1/10W	1/16W
Resistance	MAX.50mW			
Rated Current	2A	1.5A	1A	1A
Peak Current	5A	3.5A	3A	1.5A
Operating Temperature	-55~155° C			

BD Information:
T=1.6 +/-0.1MM 8layers
L*W=240mmX 190mm

How to option FUSE
FUSE calculate Current:AI(A)
FUSE actual Current:A(A)
EXP calculate:
AI=X+0.8
1) A=AI+(+/-0.1)
2) AI+0.1<=A<=AI+0.4

Find==>Part Reference=(C|R)[2-9]

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PCB BOARD SIZE
240mmX 190mm
6 Layer

Internal Slot/Header
Front/rear/side IO
Chipset/IC

NC81203
(3 Phase 65W+2Phase)
P:46~48

DDR4 SO-DIMM
2133 MHz
P:12
DIMM1

DDR4 SO-DIMM
2133 MHz
P:13
DIMM2

Channel A
64 bit

Channel B
64 bit

HDMI CONN
P:56

DDI (HDMI OUT)

Intel
Skylake LGA1151
S-LINE 4+2 65W
Quad code
P:3~11

Adapter 20V
P:45

PCB MOUNTING HOLES-PTH

20" Panel
P:55
LVDS

Parade DP703
Parade PS8625
(Colay Scalar)
P:95

EDP

100MHz

DMI

PECI

2D WEBCAM P:65

USB 2.0 *3
P:16
480Mb/S

USB2.0 x2 rear
P:39

Card reader
P:33
PCIE Gen1 Interface

USB3.0 x2 side
USB3.0 x2 rear

USB3.0 x4
P:38
P:36
P:16
4.8Gb/S

SATA *1
Slim ODD
P:60
P:19
SATA3.0 BUS

SATA *1
3.5" HDD
P:60
P:19
SATA3.0 BUS

P:29
Combo Jack

Realtek
ALC233VB
P:27
High Definition Audio

P:29
Speaker
2WX2

P:15~23
Intel PCH H110

P:17
SPI BUS
SPI Flash ROM
8MB
P:25

PCIE Gen1 Interface
NGFF Card
P:61

WLAN1
PCIE Gen1 Interface
RTL8111G
P:31
RJ45
6KV
P:32

25M

PCIE Gen1 Interface
Colay
SATA Interface
M.2 SSD
P:62

100MHz
14MHz / 25MHz / 48MHz
48MHz
33MHz
14.318MHz
32.768KHz
32.7K

TPM/TCM
P:91
SPI Interface

PS2
P:92

LPC BUS

PECI

Com port1
P:65

Com port2
P:65

P:24
ECIO
NCT 6685D

SYS 1X4 FAN
P:26

Parallel port
P:92

PCB STACKUP 6Layer
190*240 mm
1.6mm

TOP
GND/PWR
L3-signal
L4-signal
GND
BOTTOM

PCB Color:==>
ET phase:Red
SDV phase:Blue
SIT/SVT phase:Green

<Variant Name>

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Title: BLOCK DIAGRAM
Size: C
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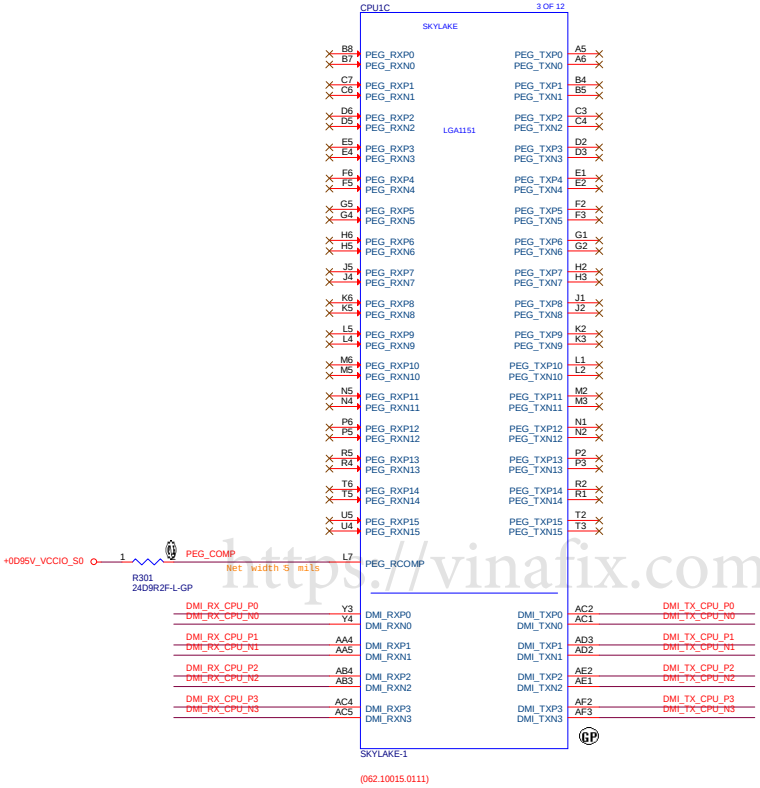
DMI

16 DMI_RX_CPU_P[0..3]
16 DMI_RX_CPU_N[0..3]

16 DMI_TX_CPU_P[0..3]
16 DMI_TX_CPU_N[0..3]



Signal	Trace Width (mils)	Isolation Spacing (mils)	Resistor Value	Max Length (mils)
CPU Signals				
PEG_RCOMP	5	15 mils	24.9ohm +/- 1% Pull Up to VCCIO	600

<Variant Name>

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Title: CPU_(PCIE/DMI)

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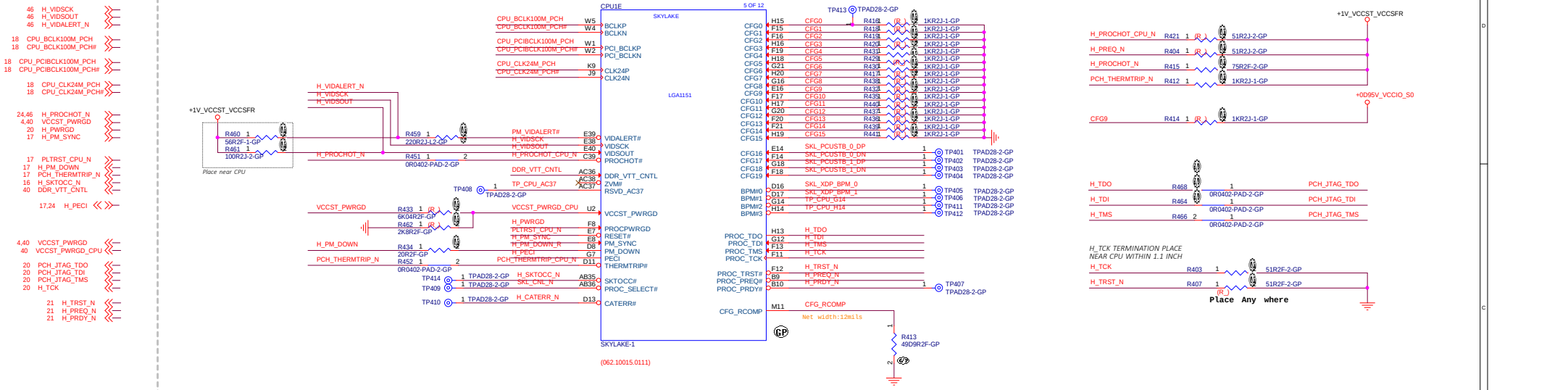
Date: Saturday, June 18, 2016 | Sheet 3 of 106



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Component	Value	✔
CFG_RCOMP	49.9 ohm +/- 1% pull down termination to GND	

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[0]		Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		
CFG[2]	Reserved. No connect			
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - An external Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1	
CFG[19:5]	Reserved configuration lands. A test point may be placed on the board for these lands.			

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Title: CPU (CFG/CLOCK/PM)

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CHANNEL A

<Variant Name>

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Title: CPU_(DDR4 CHANNEL A)

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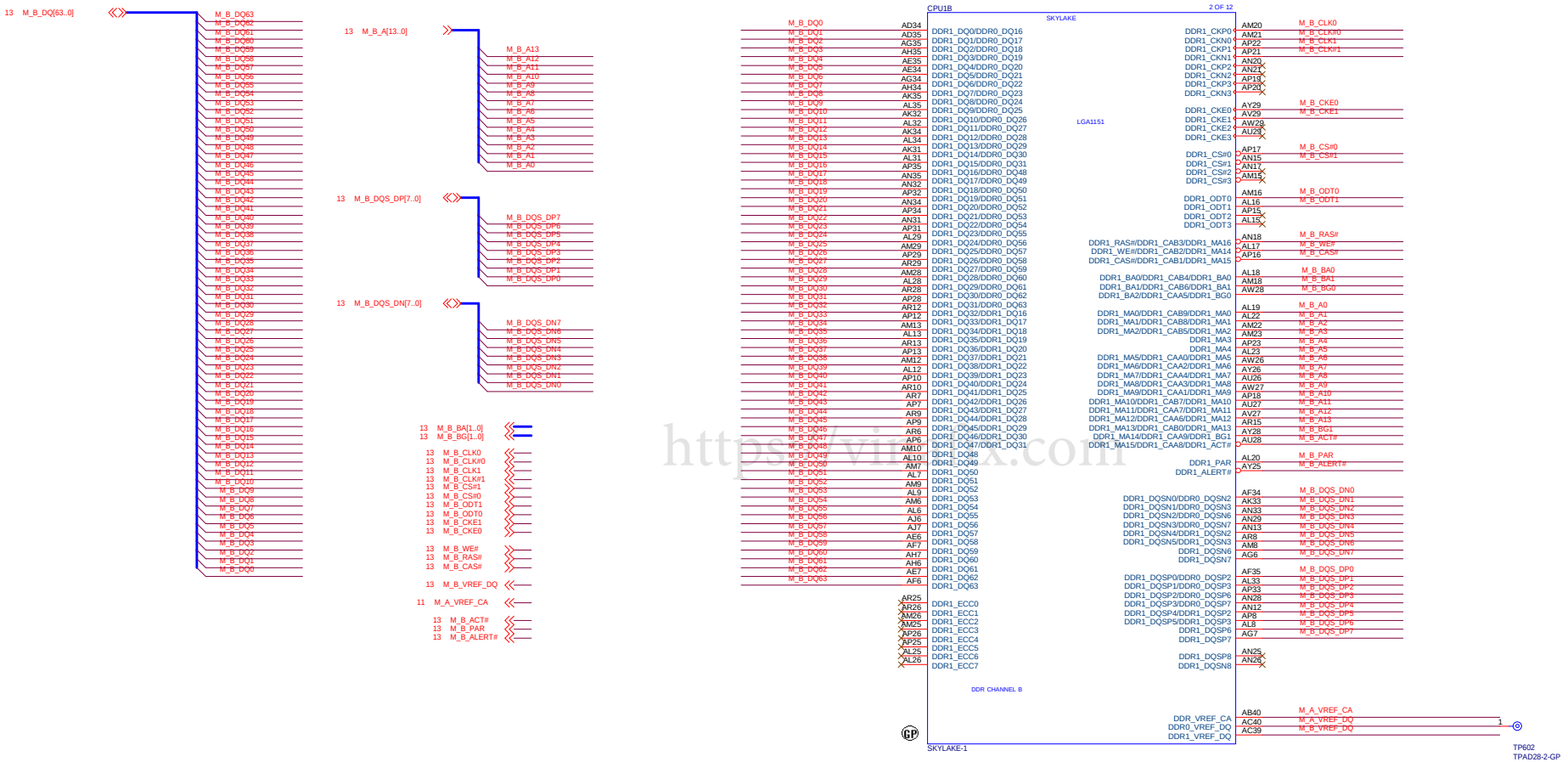
CHANNEL B DIMM0



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<Variant Name>

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Title: CPU_(DDR4 CHANNEL B)		
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HDMI OUT

56 HDMI_DATA_CPU_P0
56 HDMI_DATA_CPU_N0
56 HDMI_DATA_CPU_P1
56 HDMI_DATA_CPU_N1
56 HDMI_DATA_CPU_P2
56 HDMI_DATA_CPU_N2
56 HDMI_CLK_CPU_P3
56 HDMI_CLK_CPU_N3

EDP

95 eDP_TX_CPU_P0
95 eDP_TX_CPU_N0
95 eDP_TX_CPU_P1
95 eDP_TX_CPU_N1
95 eDP_TX_CPU_P2
95 eDP_TX_CPU_N2
95 eDP_TX_CPU_P3
95 eDP_TX_CPU_N3

95 eDP_AUX_CPU_P
95 eDP_AUX_CPU_N

20 AUD_AZACPU_SDO
20 AUD_AZACPU_SDI_R
20 AUD_AZACPU_SCLK

HDMI Connector <= HDMI(Port 1)

CPU1D — SKYLAKE — 4 OF 12

HDMI_DATA_CPU_P2 C21 — DDI1_TXP0
HDMI_DATA_CPU_N2 D21 — DDI1_TXN0
HDMI_DATA_CPU_P1 D22 — DDI1_TXP1
HDMI_DATA_CPU_N1 E22 — DDI1_TXN1
HDMI_DATA_CPU_P0 B23 — DDI1_TXP2
HDMI_DATA_CPU_N0 A23 — DDI1_TXN2
HDMI_CLK_CPU_P3 C23 — DDI1_TXP3
HDMI_CLK_CPU_N3 D23 — DDI1_TXN3

LGA1151

B13 — DDI1_AUXP
C13 — DDI1_AUXN

B18 — DDI2_TXP0
A18 — DDI2_TXN0
D18 — DDI2_TXP1
E18 — DDI2_TXN1
C19 — DDI2_TXP2
D19 — DDI2_TXN2
D20 — DDI2_TXP3
E20 — DDI2_TXN3

A12 — DDI2_AUXP
B12 — DDI2_AUXN

B14 — DDI3_TXP0
A14 — DDI3_TXN0
C15 — DDI3_TXP1
B15 — DDI3_TXN1
B16 — DDI3_TXP2
A16 — DDI3_TXN2
C17 — DDI3_TXP3
B17 — DDI3_TXN3

B11 — DDI3_AUXP
C11 — DDI3_AUXN

SKYLAKE-1

(062.10015.0111)

eDP (Port D) => Scalar

EDP_TXP0 — E10 — eDP_TX_CPU_P0
EDP_TXN0 — D10 — eDP_TX_CPU_N0
EDP_TXP1 — D9 — eDP_TX_CPU_P1
EDP_TXN1 — C9 — eDP_TX_CPU_N1
EDP_TXP2 — H10 — eDP_TX_CPU_N2
EDP_TXN2 — G10 — eDP_TX_CPU_P2
EDP_TXP3 — G9 — eDP_TX_CPU_N3
EDP_TXN3 — F9 — eDP_TX_CPU_P3

EDP_AUXP — D12 — eDP_AUX_CPU_P
EDP_AUXN — E12 — eDP_AUX_CPU_N

EDP_DISP_UTIL — D14 — EDP_DISP_UTIL — 1 — TP701 TPAD28-2-GP

EDP_RCOMP — M9 — DP_RCOMP — R703 1 2 24D9R2F-L-GP — +0D95V_VCCIO_S0
Net width 5 mils

PROC_AUDIO_CLK — V3 — AUD_AZACPU_SCLK
PROC_AUDIO_SDI — V2 — AUD_AZACPU_SDO
PROC_AUDIO_SDO — U1 — AUD_AZACPU_SDI — R704 1 2 20R2F-GP — AUD_AZACPU_SDI_R

GP

Signal	Trace Width (mils)	Isolation Spacing (mils)	Resistor Value	Max Length (mils)
CPU Signals				
PEG_RCOMP	5	15 mils	24.9ohm +/- 1% Pull Up to VCCIO	600
eDP_RCOMP	5	20 mils to other RCOMP signals; 25 mils to other signals	24.9ohm +/- 1% Pull Up to VCCIO	600

<Variant Name>

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Title: CPU_(DDI/EDP)

Size: B | Document Number: A7400 | Rev: -1B

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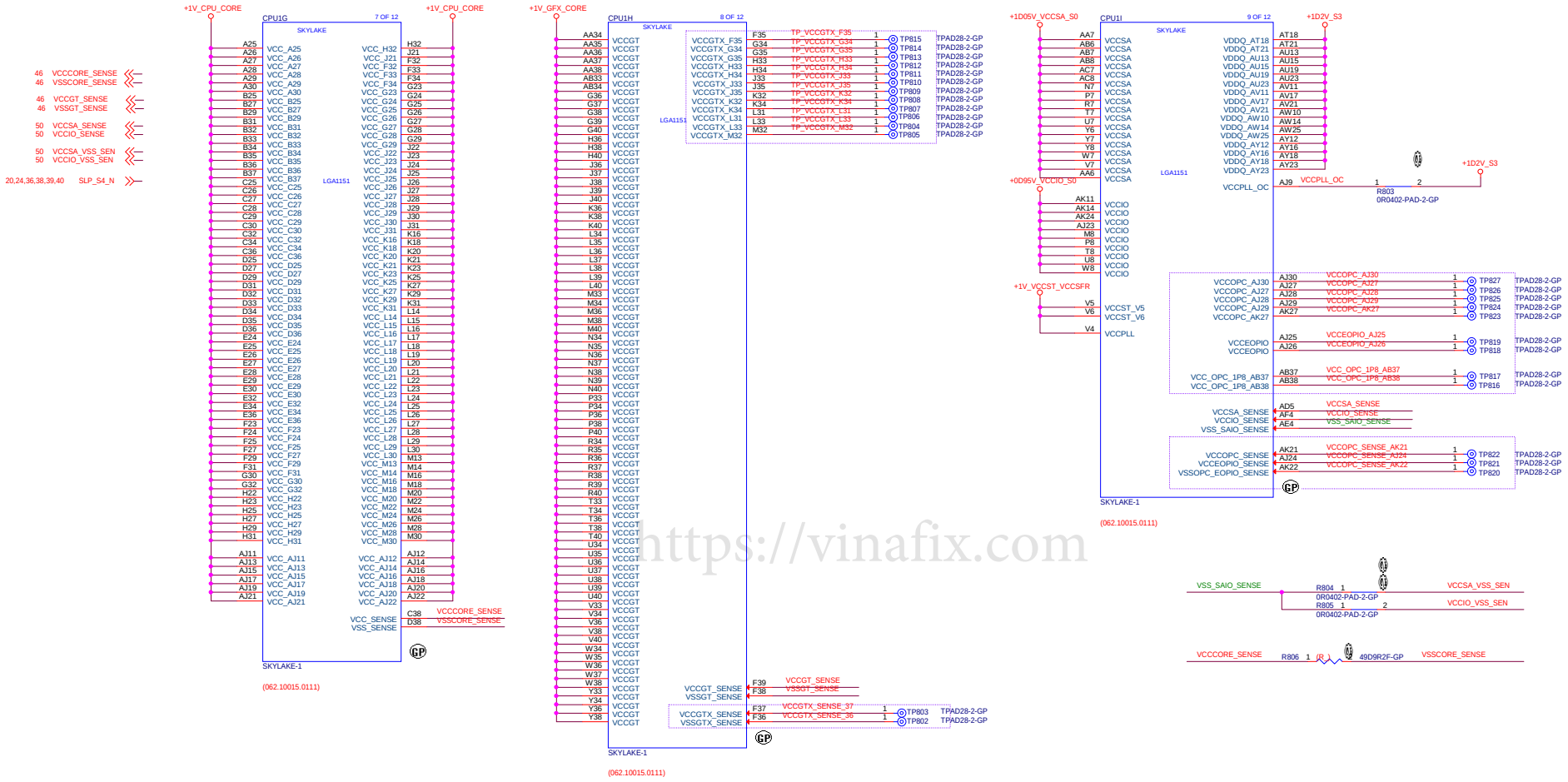

<Variant Name>

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Title: CPU_(CPU Power)

Size	Document Number	Rev
C	A7400	-1B

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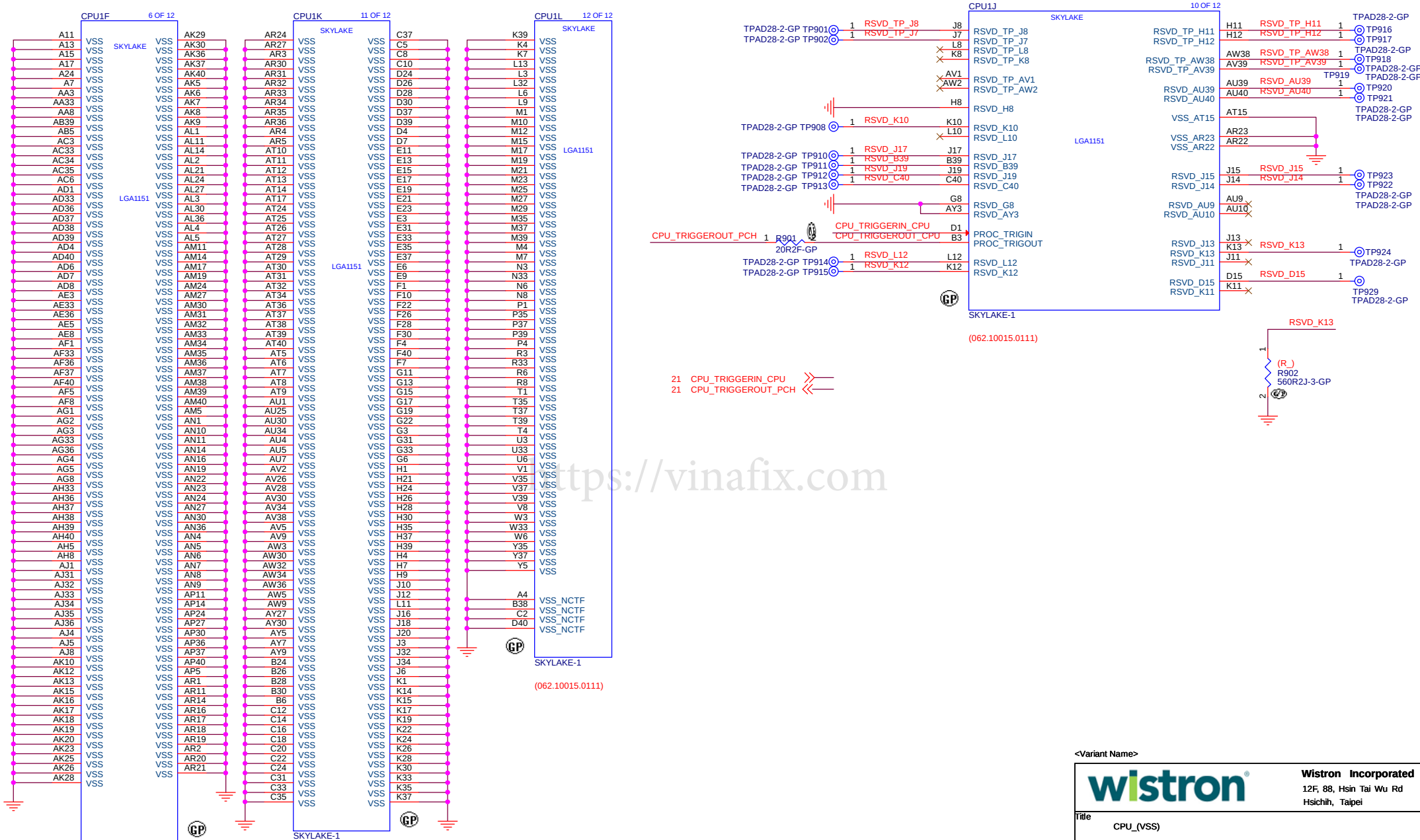

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Title	CPU_(VSS)	
Size B	Document Number A7400	Rev -1B
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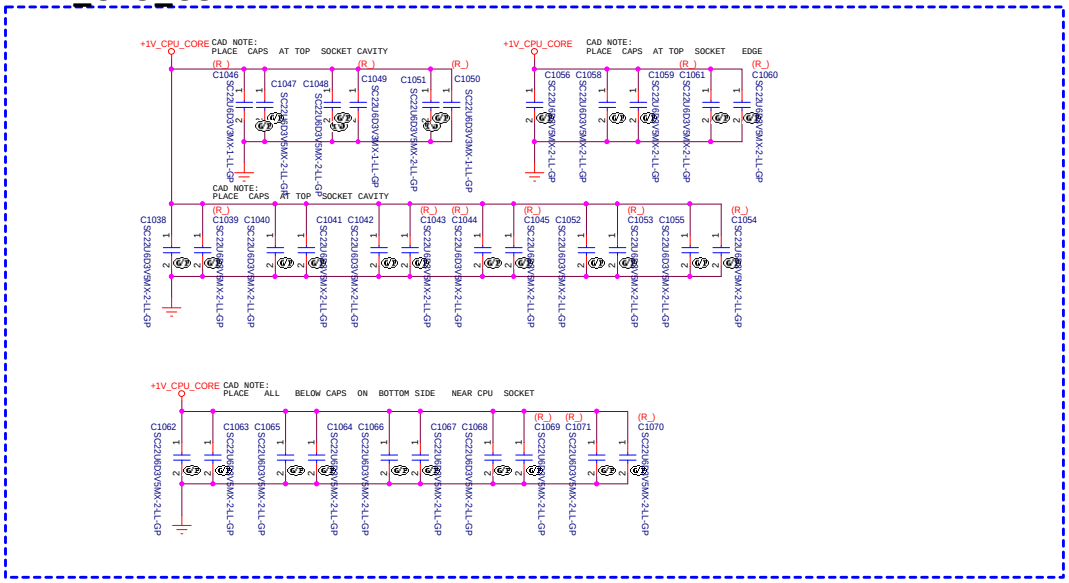
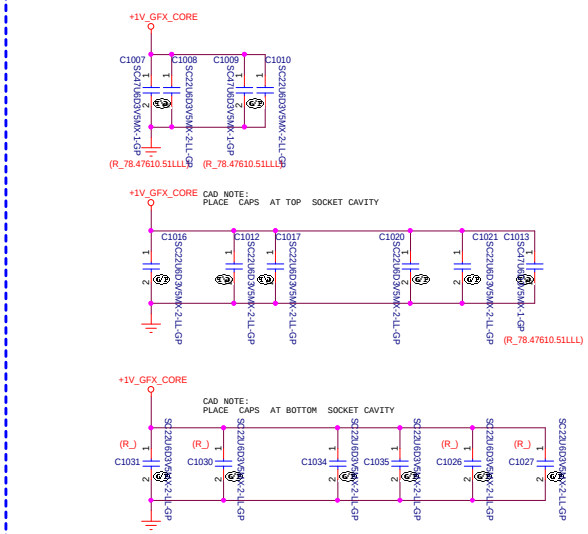
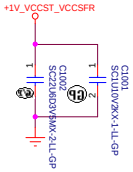
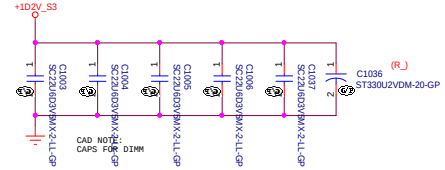
+1V_CPU_CORE

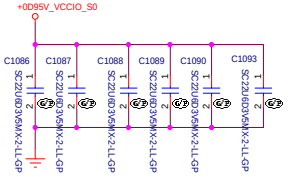


+1V_GFX_CORE









<Variant Name>

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Hsichih, Taipei

Title: CPU Power CAP

Size: C | Document Number: A7400 | Rev: 1B

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CHANNEL-A XMM1, A0, H=9.2mm

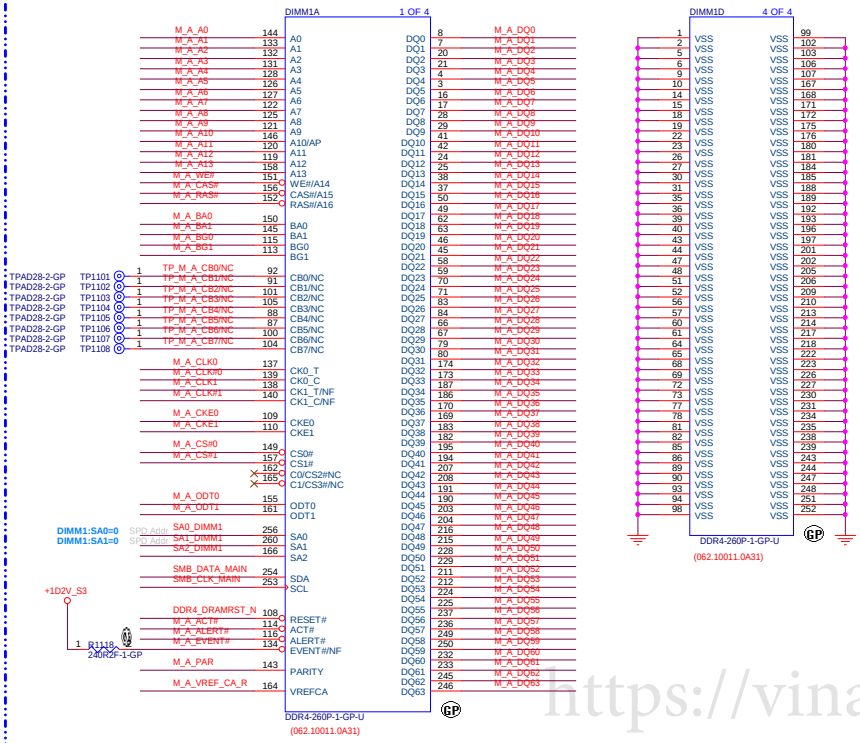
DDR DATA
5 M_A_DQ[63..0]
5 M_A_DQS_DN[7..0]
5 M_A_DQS_DP[7..0]

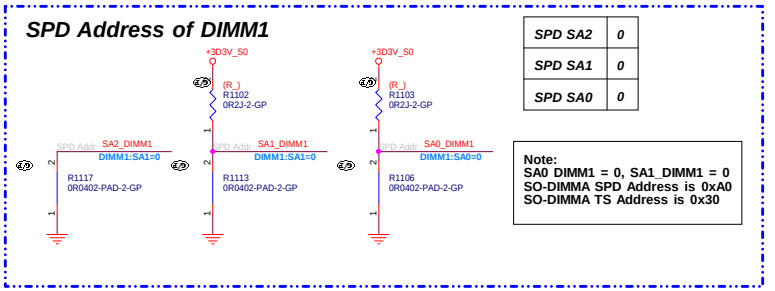
DDR CMD/ADD
5 M_A_A[13..0]
5 M_A_CAS#
5 M_A_WE#
5 M_A_RAS#

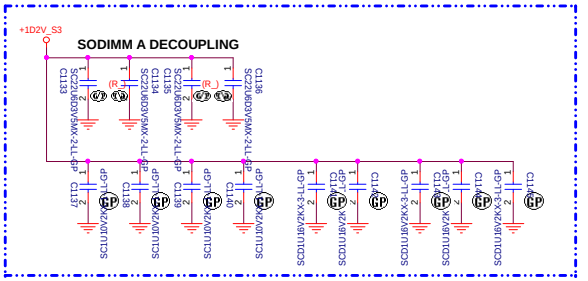
DDR CTRL
5 M_A_ODT0
5 M_A_ODT1
5 M_A_CKE0
5 M_A_CKE1
5 M_A_CS#0
5 M_A_CS#1

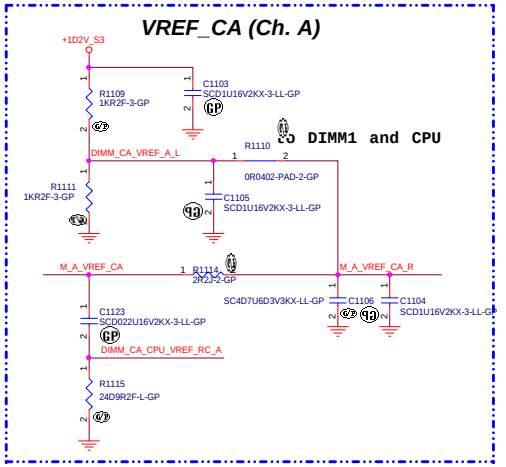
DDR CLOCK
5 M_A_CLK0
5 M_A_CLK#0
5 M_A_CLK1
5 M_A_CLK#1

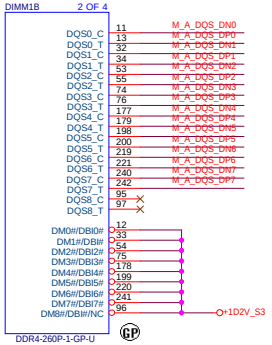
DDR OTHERS
13,20,95 SMB_DATA_MAIN
13,20,95 SMB_CLK_MAIN
13,20 DDR4_DRAMRST_N
6 M_A_VREF_CA
5 M_A_BA[1..0]
5 M_A_BG[1..0]
5 M_A_ACT#
5 M_A_ALERT#
5 M_A_PAR

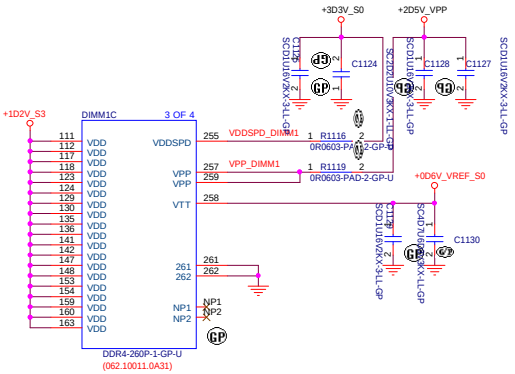












SPD Address Table

SMBus_0	
Device	8-bit Address(hex)
DIMM_A0	Write Addr:0xA0 / Read Addr:0xA1 — SA1=0;SA0=0
DIMM_A1	Write Addr:0xA2 / Read Addr:0xA3 — SA1=0;SA0=1
DIMM_B0	Write Addr:0xA4 / Read Addr:0xA5 — SA1=1;SA0=0
DIMM_B1	Write Addr:0xA6 / Read Addr:0xA7 — SA1=1;SA0=1

1	0	1	0	0	SA1	SA0	0

Note:0' 3~7 bit as default

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR DIMM_1
Size: C
Document Number: A7400
Rev: -1B
Date: Saturday, June 18, 2016
Sheet 11 of 106

<Variant Name>

wistron®	**Wistron Incorporated** 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: DDR DIMM_2(R)		
Size: A	Document Number: A7400	Rev: -1B
Date: Saturday, June 18, 2016	Sheet 12 of 106	

CHANNEL-B DIMM2, A4, H=5.2mm

DDR DATA
6 M_B_DQ[63..0]
6 M_B_DQS_DN[7..0]
6 M_B_DQS_DP[7..0]

DDR CMD/ADD
6 M_B_A[13..0]
6 M_B_WE#
6 M_B_RAS#
6 M_B_CAS#
6 M_B_BA[1..0]
6 M_B_BG[1..0]

DDR CTRL
6 M_B_CS#1
6 M_B_CS#0
6 M_B_CKE1
6 M_B_CKE0
6 M_B_ODT0
6 M_B_ODT1

DDR CLOCK
6 M_B_CLK0
6 M_B_CLK#0
6 M_B_CLK1
6 M_B_CLK#1

DDR OTHERS
11,20 DDR4_DRAMRST_N
11,20,95 SMB_DATA_MAIN
11,20,95 SMB_CLK_MAIN
6 M_B_ACT#
6 M_B_PAR
6 M_B_ALERT#
6 M_B_VREF_DQ

DIMM2A 1 OF 4 — DDR4-260P-GP-U1 (062.10011.0A41)

DIMM2D 4 OF 4 — DDR4-260P-GP-U1 (062.10011.0A41)

DIMM2B 2 OF 4 — DDR4-260P-GP-U1 (062.10011.0A41)

DIMM2C 3 OF 4 — DDR4-260P-GP-U1 (062.10011.0A41)

SPD Address of DIMM2

SPD SA2	0
SPD SA1	1
SPD SA0	0

R1301 0R0402-PAD-2-GP (SA2_DIMM2, DIMM1:SA1=0)
R1324 0R0402-PAD-2-GP
R1305 0R2J-2-GP (SA1_DIMM2, DIMM2:SA1=1)
R1302 0R2J-2-GP (SA0_DIMM2, DIMM2:SA0=0)
R1306 0R0402-PAD-2-GP

Note:
SA0 DIMM2 = 0, SA1_DIMM2 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

VREF_DQ (Ch. B)

To DIMM1 and CPU

SPD Address Table

SMBus 0		
Device	8-bit Address(hex)	
DIMM A0	Write Addr:0xA0 Read Addr:0xA1	SA1=0;SA0=0
DIMM A1	Write Addr:0xA2 Read Addr:0xA3	SA1=0;SA0=1
DIMM B0	Write Addr:0xA4 Read Addr:0xA5	SA1=1;SA0=0
DIMM B1	Write Addr:0xA6 Read Addr:0xA7	SA1=1;SA0=1

1	0	1	0	0	SA1	SA0	0

Note:0' 3~7 bit as default

PWR_SEQ = 19 or 29

Place these caps close to VTT1 and VTT2.

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR DIMM_3
Size: C | Document Number: A7400 | Rev: -1B
Date: Saturday, June 18, 2016 | Sheet 13 of 106

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
DDR DIMM_4(R)

Size	Document Number	Rev
A	A7400	-1B

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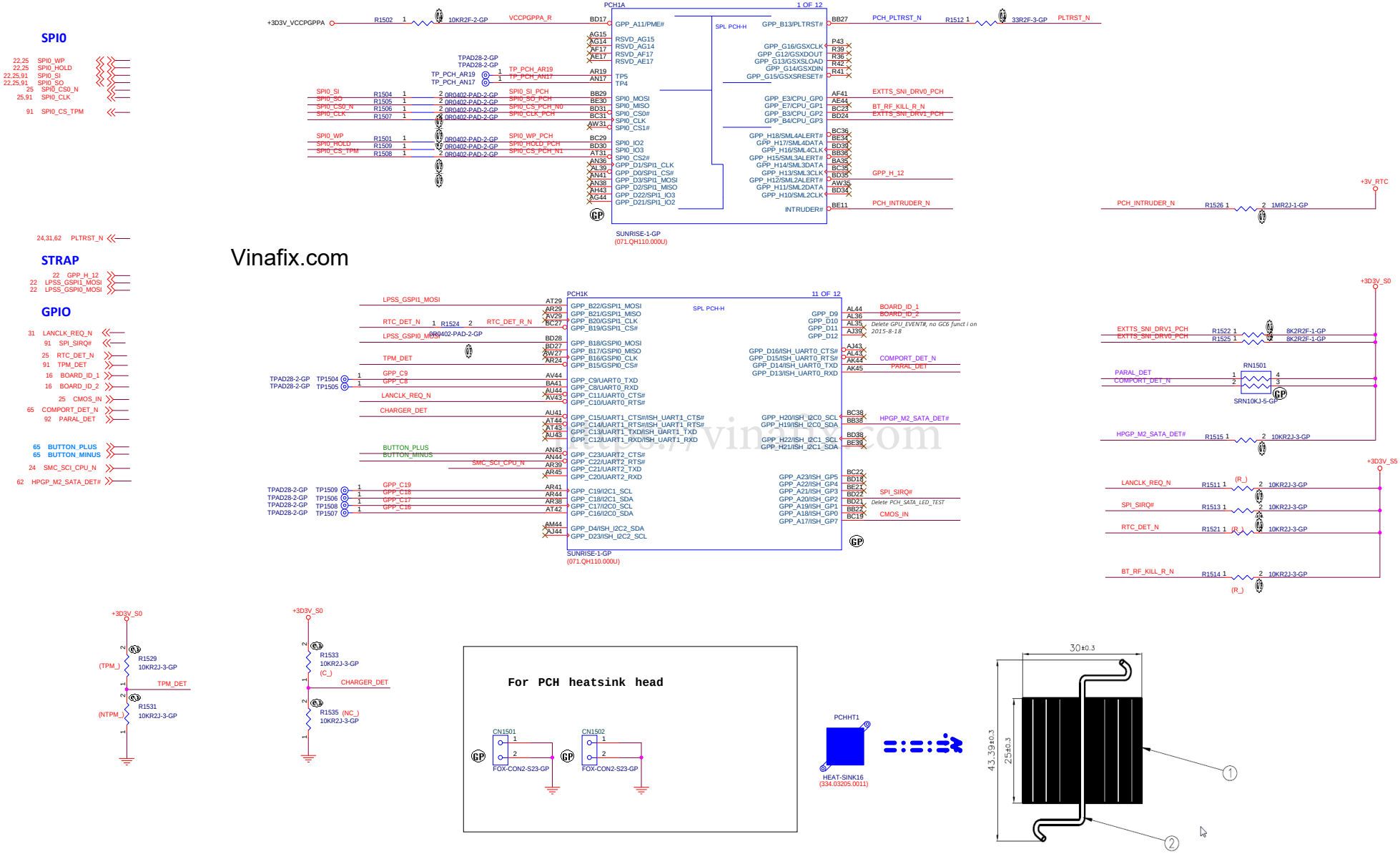
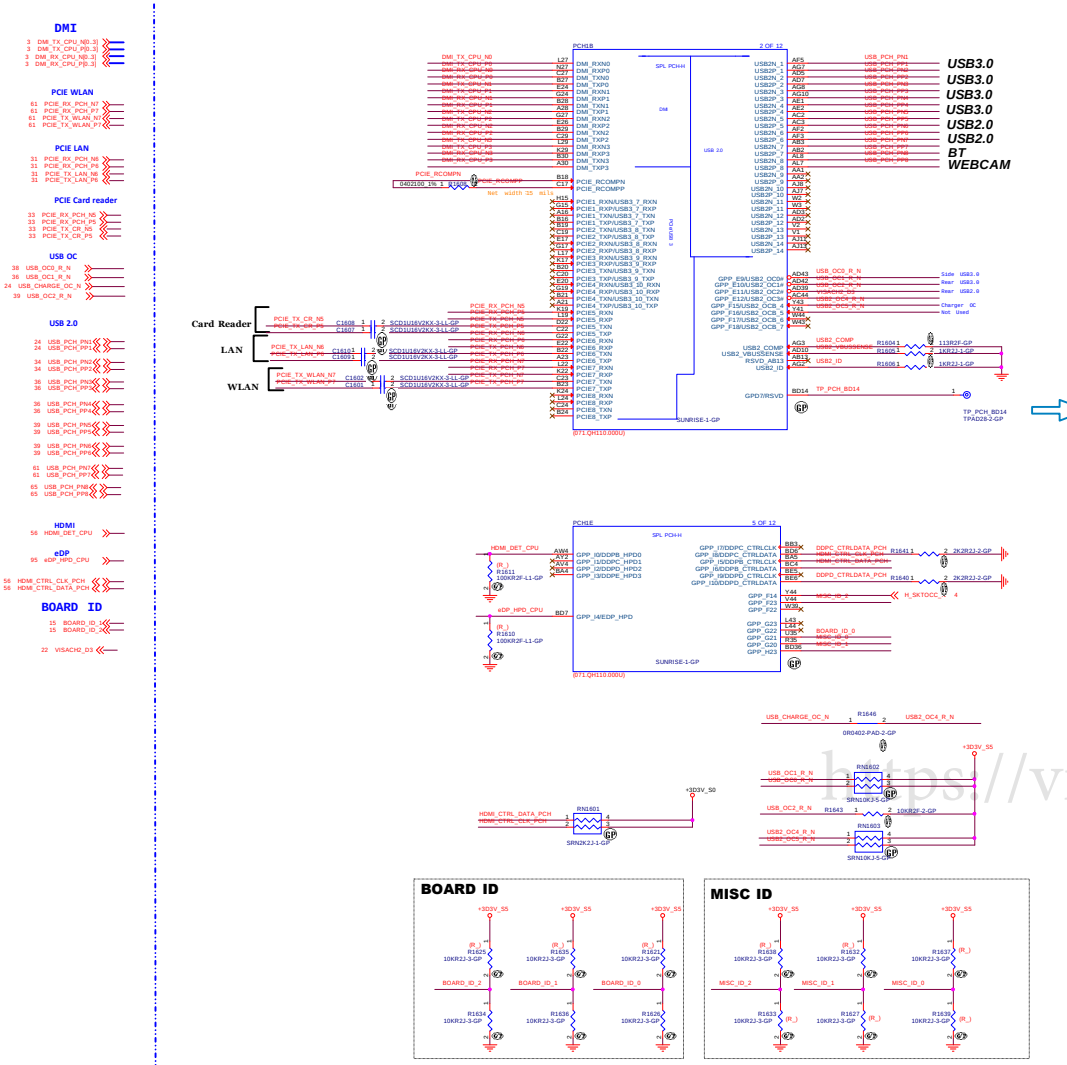


<Variant Name>

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: PCH_(SPI/UART/I2C)		
Size: C	Document Number: A7400	Rev: -1B
Date: Saturday, June 18, 2016	Sheet 15 of 106	



USB 2.0 Table,H110表 用10,Port 1-port8

Pair	Device	
1	USB2.0 signal for side USB31	Debug Card Port
2	USB2.0 signal for side USB32	Charger Port
3	USB2.0 signal for rear USB33	Double USB3.0
4	USB2.0 signal for rear USB33	
5	USB2.0 signal for rear USB21	Double USB2.0
6	USB2.0 signal for rear USB21	
7	USB2.0 signal for BT to WLAN1	wireless card
8	USB2.0 signal for WEBCAM	2D webcam
9	X	Not used
10	X	Not used

PCIE Table 共 20 PCI E port. H1

Port	Device	Share BUS
1~4	X	
5	CARD READER	PCIE
6	LAN	PCIE
7	WLAN	PCIE
8	X	
9~10	SSD	PCIE
11~12	X	
13	HDD	SATA
14	ODD	SATA
15	SSD	SATA
16~20	X	

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length	Length Matching
PCIE_RCOMPN	M1: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.1 ohm).	At least 12 mils to any adjacent high speed I/O.	100 ohm +/-1% external resistor. Differential between RCOMPP/ RCOMPN	NA	Both RCOMPP & RCOMPN need to matched to less than 1% trace and board
PCIE_RCOMPP	M2: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.1 ohm).			NA	

Table 1-2. PCH-H SKUs

Features	H110	H170	HM170	QM170	Z170	B150	Q150	Q170
Intel® Rapid Storage Technology	AHCI Mode	Full Features[8]	Full Features[8]	Full Features[8]	Full Features[8]	AHCI Mode	AHCI Mode	Full Features[8]
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10[1]	14[3]	12[2]	12[2]	14[3]	12[2]	14[3]	14[3]
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express* Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2[6]	2[6]	2[6]	3[7]	0	0	3[7]
Processor dgfx bifurcation support	No	No	Yes[5]	Yes[5]	Yes[5]	No	No	Yes[5]

Notes:
1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. SATA Express Capable Ports (x2)
5. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported
6. Intel® RST PCIe supports RAID configuration 0/1.
7. Intel® RST PCIe supports RAID configuration 0/1/5
8. Full featured includes SATA RAID 0/1/5/10 support

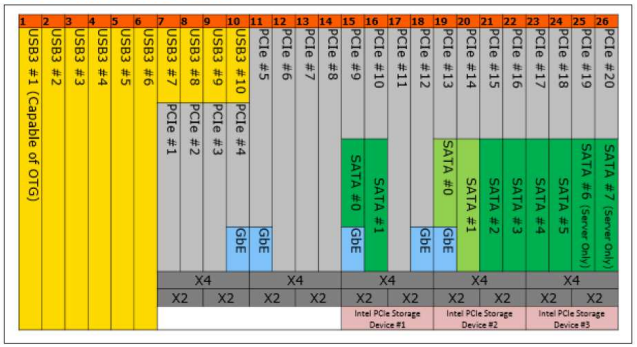
Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15[1]	16[1]	17	18	19[1]	20[1]	21	22	23	24	25	26
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA0/ LAN	SATA1	SATA	SATA	N/A	N/A	N/A	N/A

HSIO Multiplexing on PCH-H



<Variant Name>
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: PCH_(DMI/PCI-E/USB)
Size: D
Document Number: A7400
Rev: -1B
Date: Saturday, June 18, 2016
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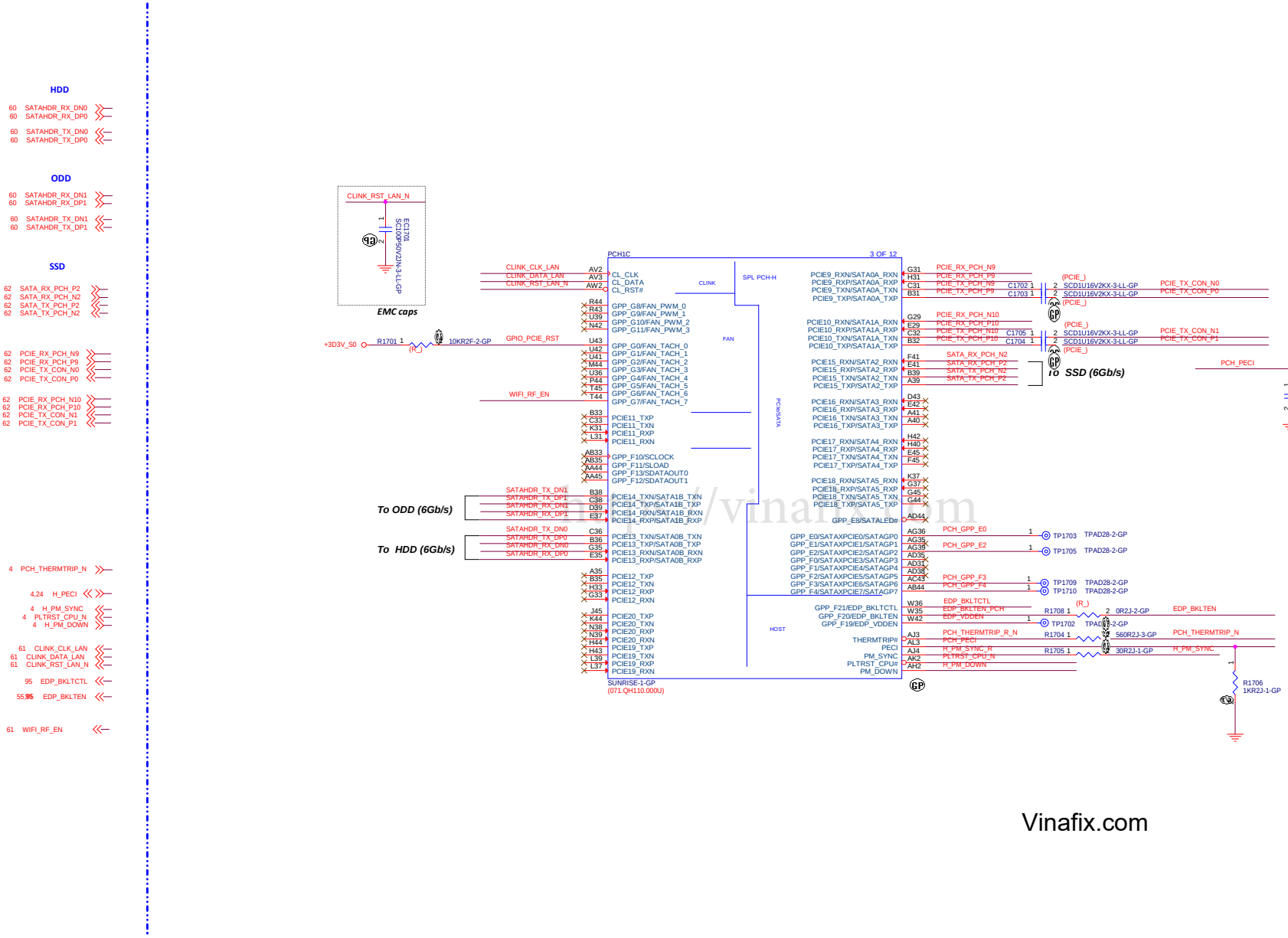

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_(PCI-E/SATA)

Size	Document Number	Rev
C	A7400	-1B

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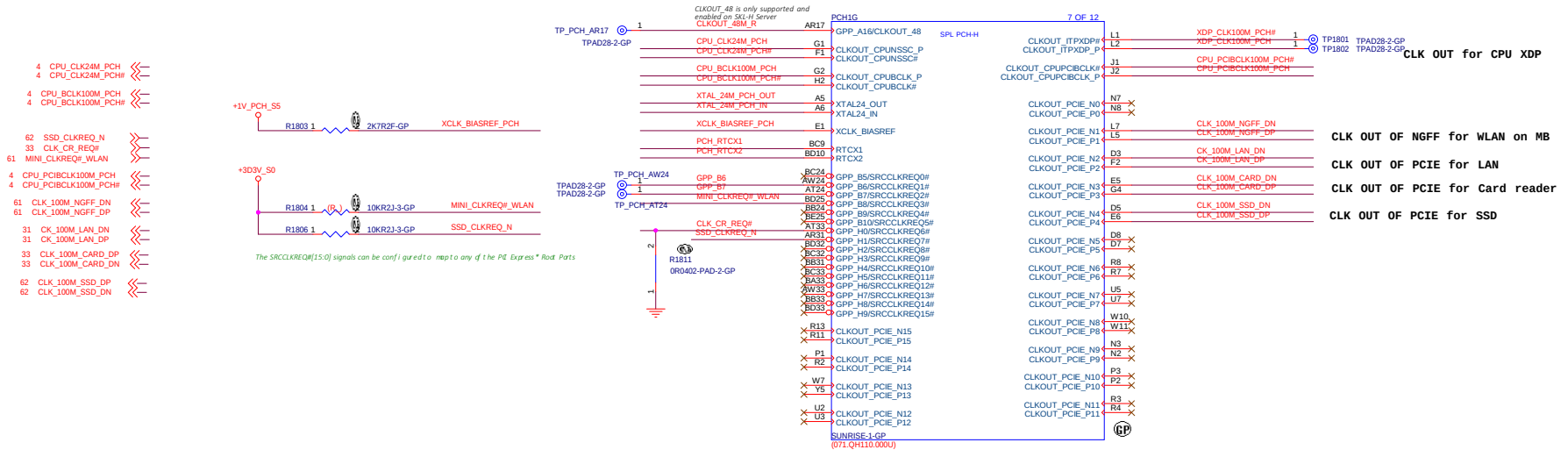
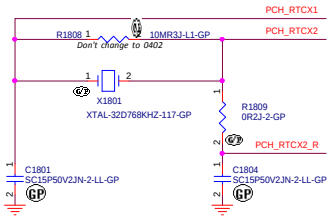
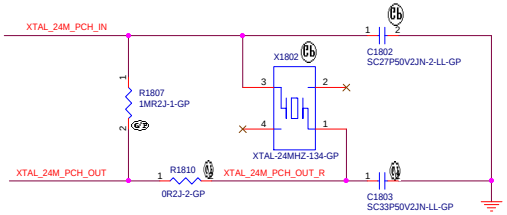


Crystal 32.768KHz



Crystal 24MHz



<Variant Name>

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Wistron Incorporated
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Hsichih, Taipei

Title: PCH_(CLOCK/CL)

Size	Document Number	Rev
C	A7400	-1B

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USB3.0

38 USB3_TX1_DN
38 USB3_TX1_DP
38 USB3_RX1_DN
38 USB3_RX1_DP

34 USB3_TX2_DN
34 USB3_TX2_DP
34 USB3_RX2_DN
34 USB3_RX2_DP

36 USB3_TX3_DN
36 USB3_TX3_DP
36 USB3_RX3_DN
36 USB3_RX3_DP

36 USB3_TX4_DN
36 USB3_TX4_DP
36 USB3_RX4_DN
36 USB3_RX4_DP

LPC interface

19,24,68 L_AD0
19,24,68 L_AD1
19,24,68 L_AD2
19,24,68 L_AD3

19,24,68 L_FRAME_N
24 SER_IRQ

24 KBRST_N
24 L_DRQ_N
24 CK_PCH_33M_SIO

DEBUG Card

19,24,68 L_FRAME_N
19,24,68 L_AD0
19,24,68 L_AD1
19,24,68 L_AD2
19,24,68 L_AD3

68 LPC_CLK_PCH24M_P0

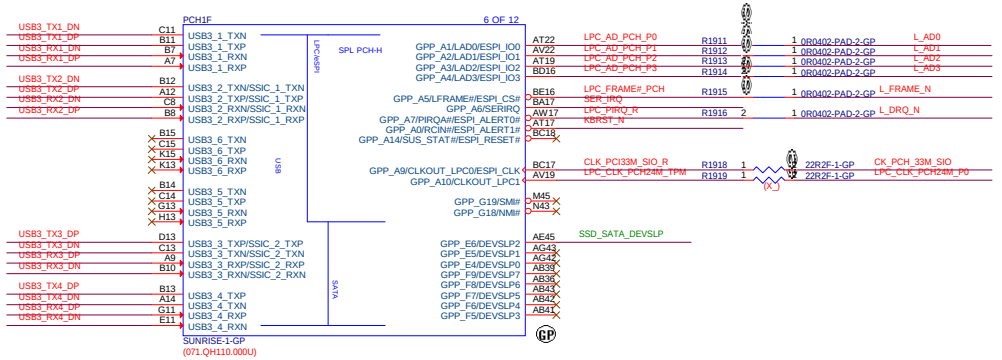
62 SSD_SATA_DEVSLP

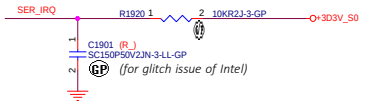
FOR Side USB3.0

FOR Side USB3.0

FOR Rear USB3.0

FOR Rear USB3.0





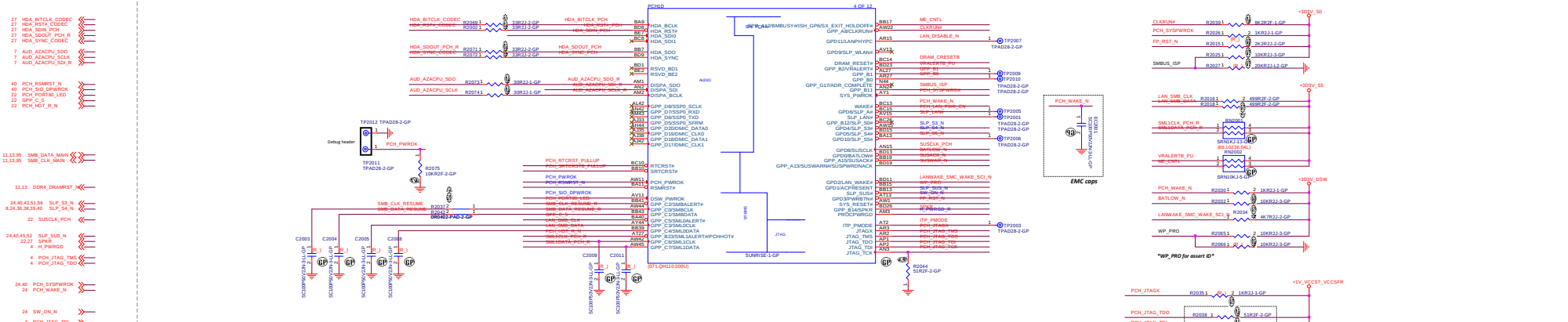
<Variant Name>

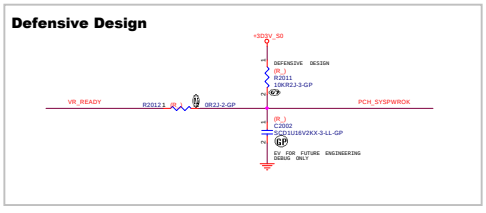
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

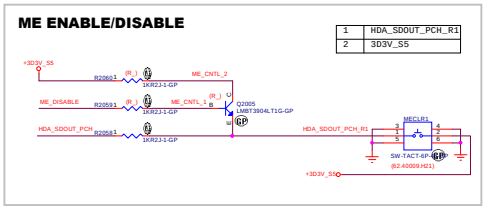
Title: PCH_(USB/ESPI)

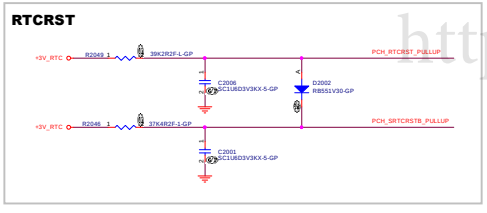
Size: C | Document Number: A7400 | Rev: -1B

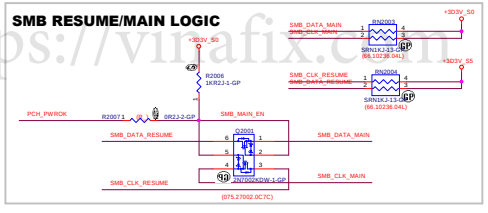
Date: Saturday, June 18, 2016 | Sheet 19 of 106

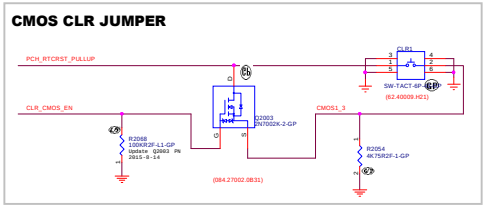


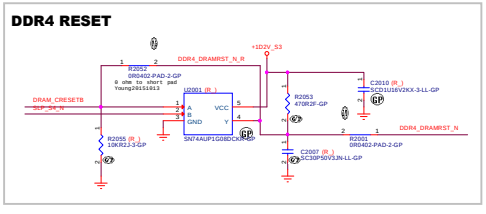












<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_(GPIO/SMBUS/HDA/JTAG)

Size: D | Document Number: A7409 | Rev: -18

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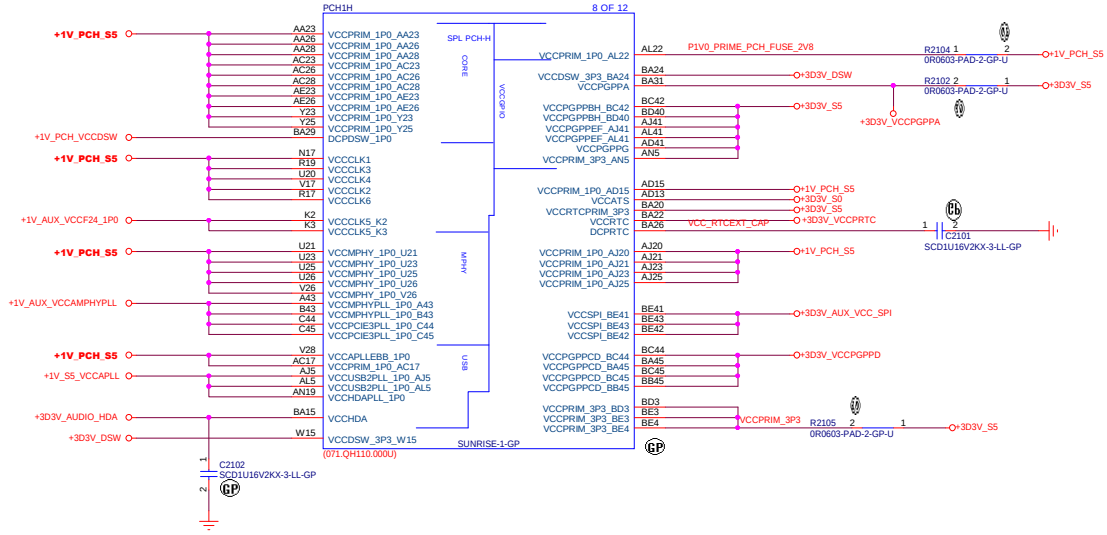

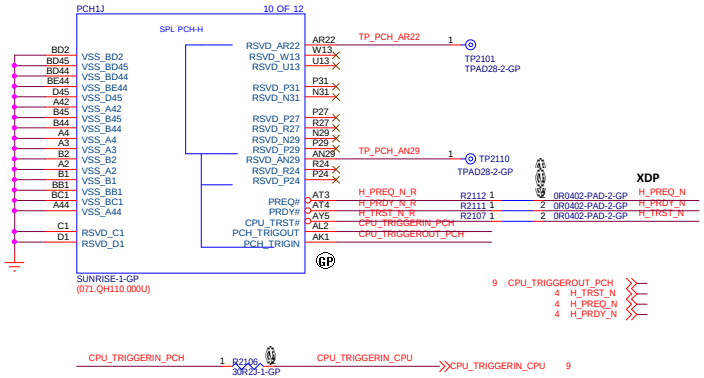

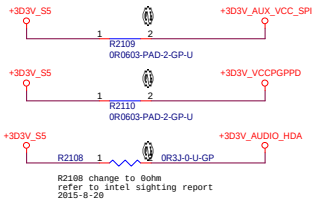

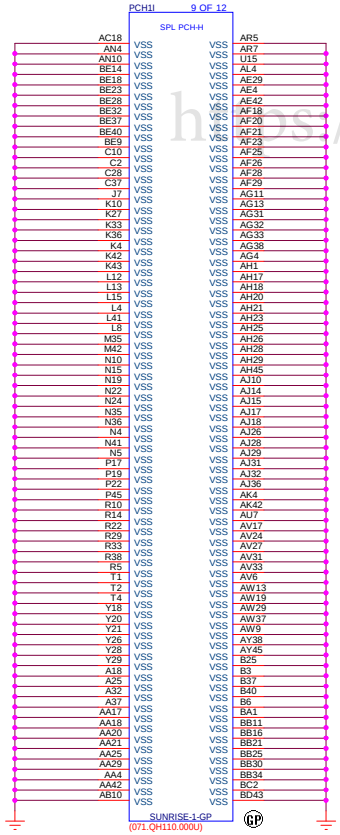

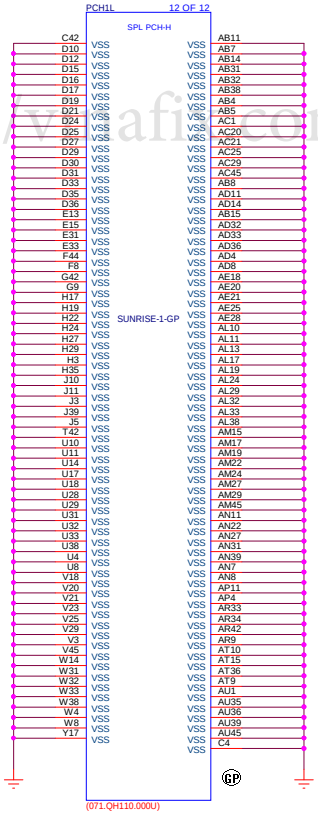

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_(POWER)

Size	Document Number	Rev
C	A7400	-1B

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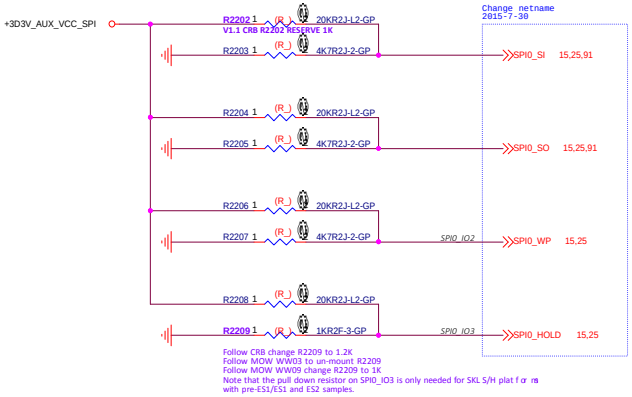
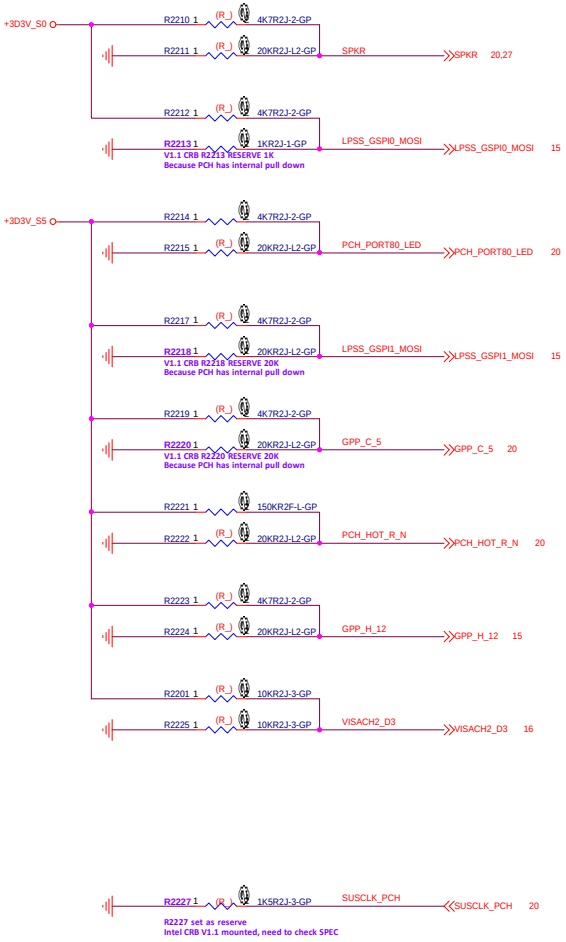
PCH STRAP FUNCTIONS





SPI_MOSI (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_MISO (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_IO2 (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_IO3 (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU

SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

<Variant Name>

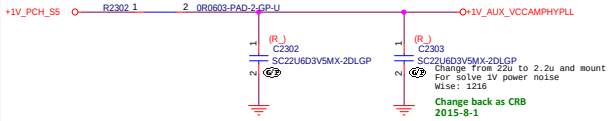
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

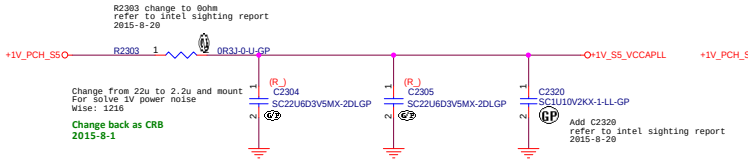
Title: PCH_Strap

Size: C | Document Number: A7400 | Rev: -1B

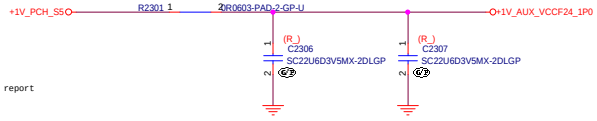
Date: Saturday, June 18, 2016 | Sheet 22 of 106



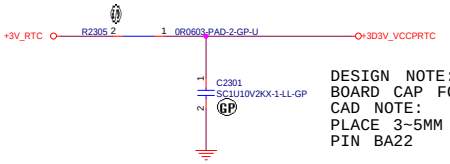
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A43, B43, C44, C45



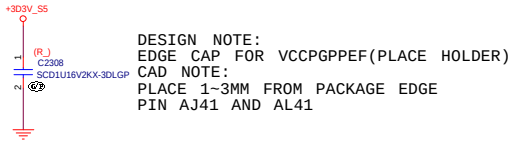
DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



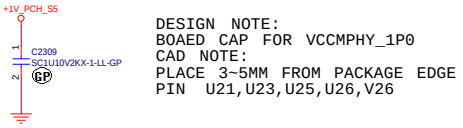
DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3



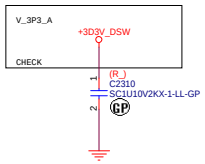
DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22



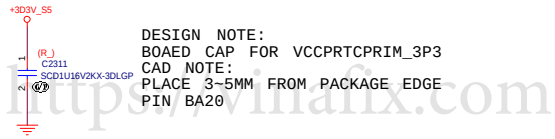
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41



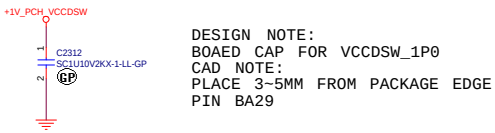
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



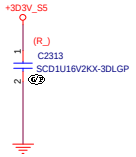
DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN W15



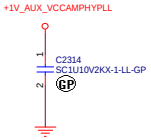
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



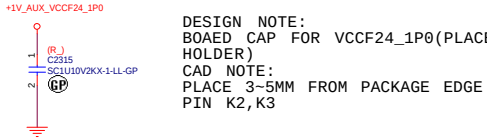
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



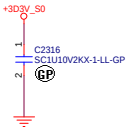
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



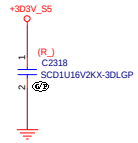
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42, A43, B43



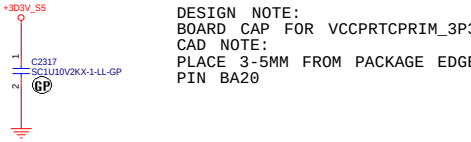
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



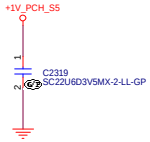
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



DESIGN NOTE:
BOARD CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3-5MM FROM PACKAGE EDGE
PIN BA20



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH Power CAP

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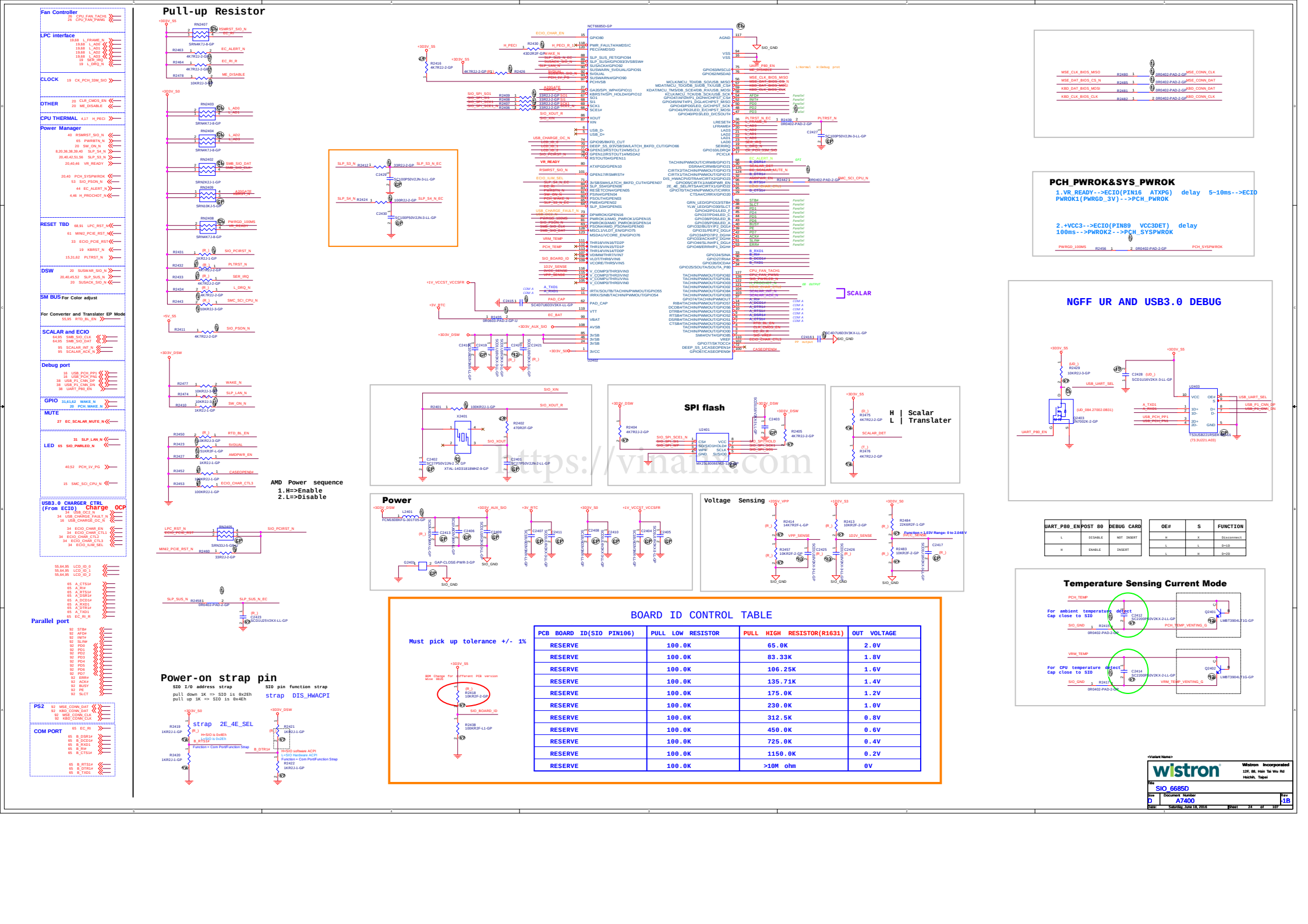
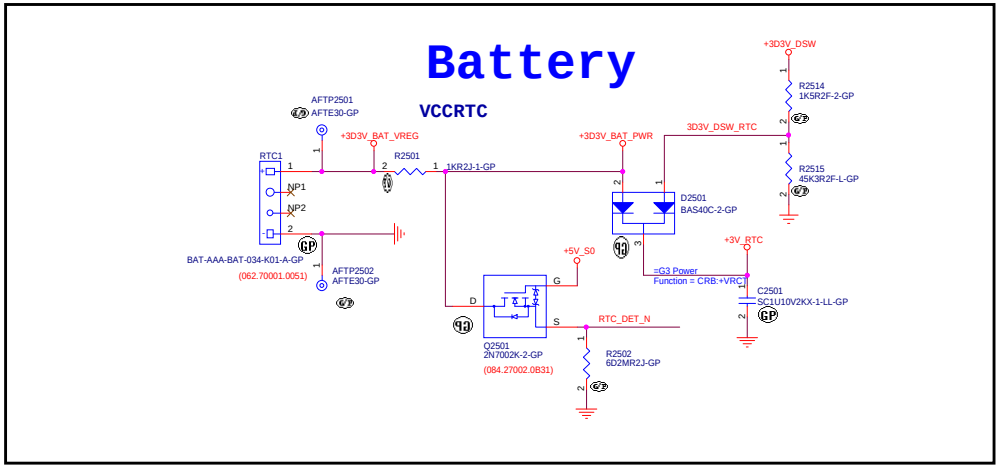
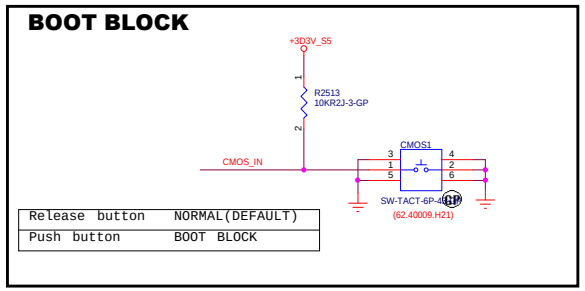


UART_P80_EN	POST 80	DEBUG CARD
L	DISABLE	NOT INSERT
H	ENABLE	INSERT

OE#	S	FUNCTION
H	X	Disconnect
L	L	D+1D
L	H	D+2D

PCB BOARD ID(SIO PIN106)	PULL LOW RESISTOR	PULL HIGH RESISTOR(R1631)	OUT VOLTAGE
RESERVE	100.0K	65.0K	2.0V
RESERVE	100.0K	83.33K	1.8V
RESERVE	100.0K	106.25K	1.6V
RESERVE	100.0K	135.71K	1.4V
RESERVE	100.0K	175.0K	1.2V
RESERVE	100.0K	230.0K	1.0V
RESERVE	100.0K	312.5K	0.8V
RESERVE	100.0K	450.0K	0.6V
RESERVE	100.0K	725.0K	0.4V
RESERVE	100.0K	1150.0K	0.2V
RESERVE	100.0K	>10M ohm	0V

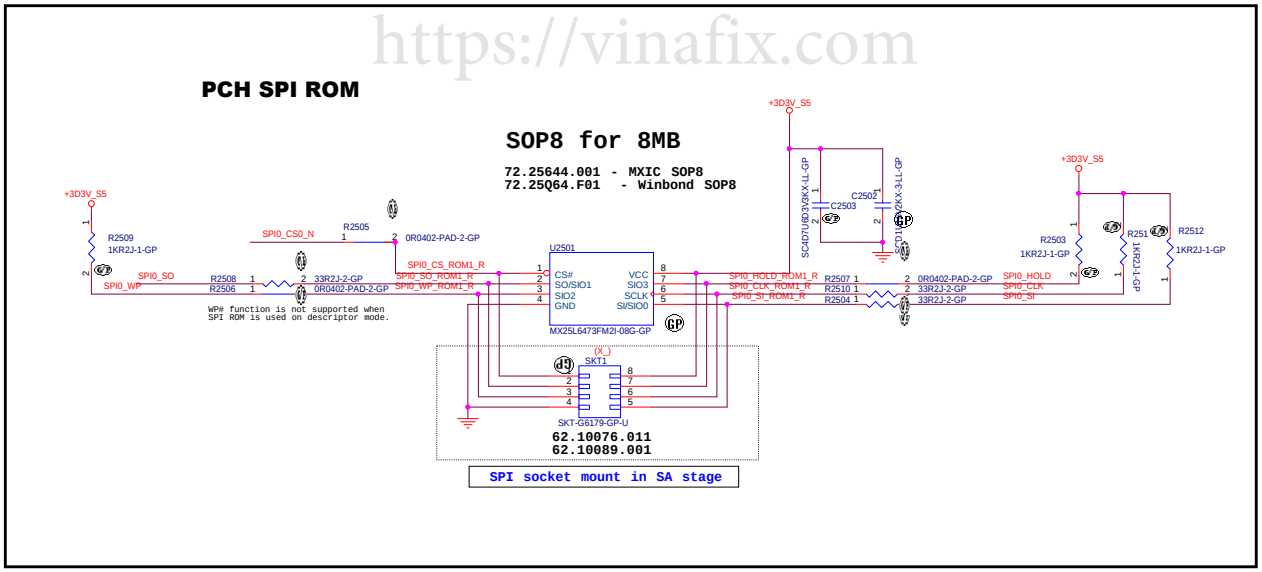




SPI ROM

15,22,91 SPI0_SI
15,22,91 SPI0_SO
15 SPI0_CS0_N
15,91 SPI0_CLK
15,22 SPI0_WP
15,22 SPI0_HOLD

15 RTC_DET_N
15 CMOS_IN



<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SPI&RTC

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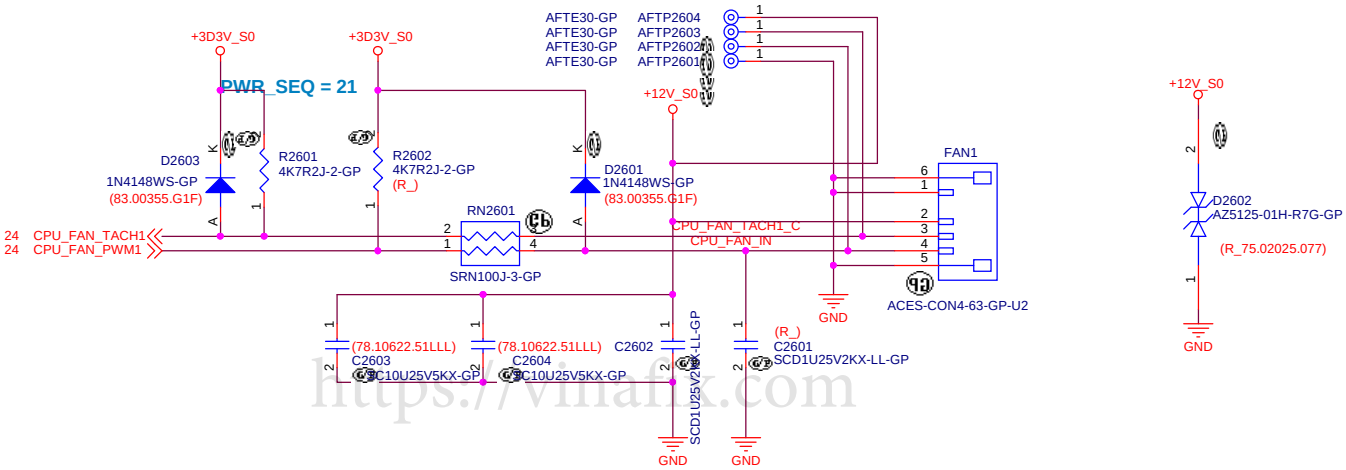
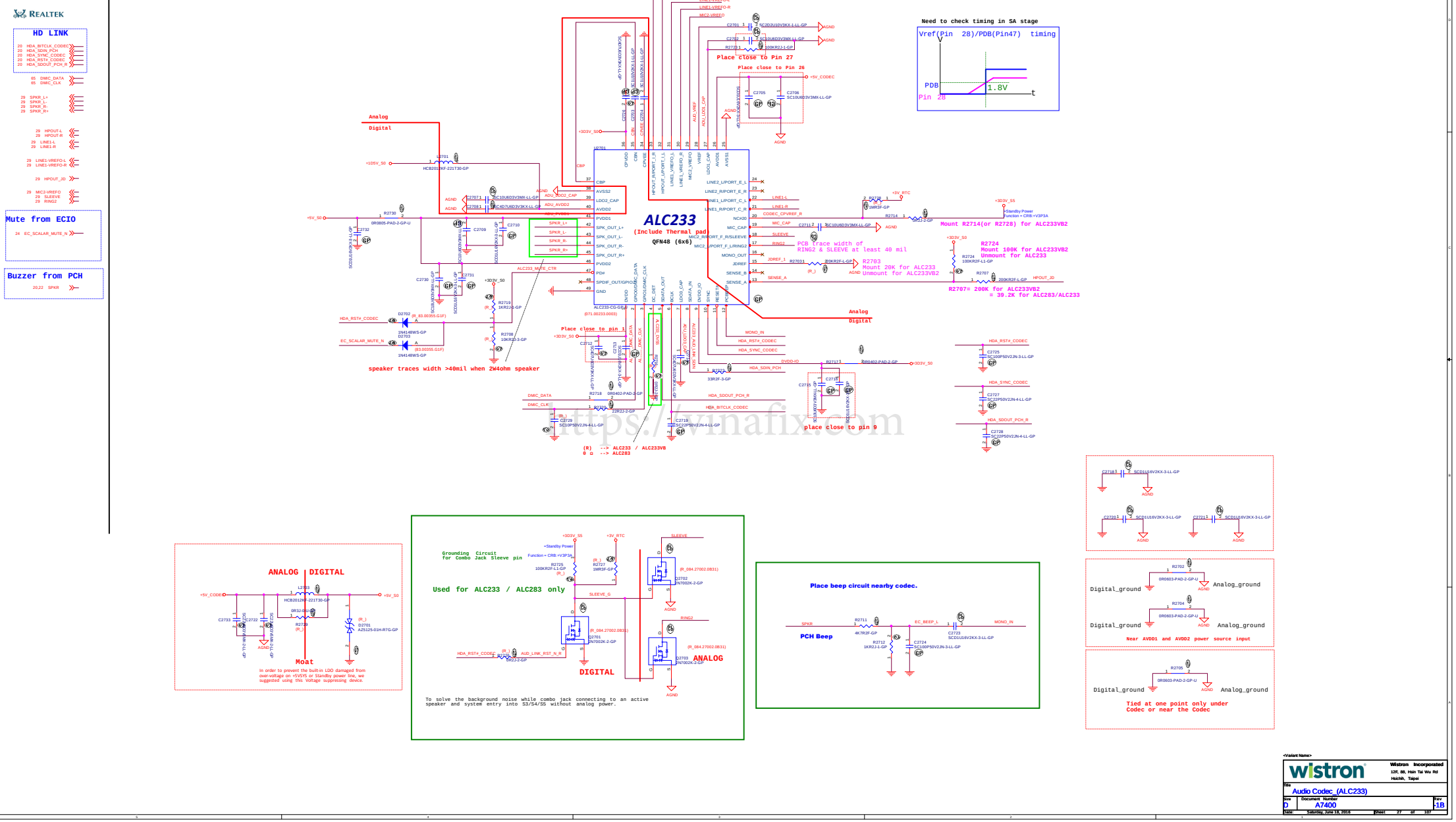
CPU FAN



<Variant Name>

wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: Fan_		
Size: B	Document Number: A7400	Rev: -1B
Date: Saturday, June 18, 2016	Sheet 26 of 107	


REALTEK
HD LINK
20 HDA_BITCLK_CODEC
20 HDA_SDIN_PCH
20 HDA_SYNC_CODEC
20 HDA_RST#_CODEC
20 HDA_SDOUT_PCH_R
65 DMIC_DATA
65 DMIC_CLK
29 SPKR_L+
29 SPKR_L-
29 SPKR_R-
29 SPKR_R+
29 HPOUT-L
29 HPOUT-R
29 LINE1-L
29 LINE1-R
29 LINE1-VREFO-L
29 LINE1-VREFO-R
29 HPOUT_JD
29 MIC2-VREFO
29 SLEEVE
29 RING2
Mute from ECIO
24 EC_SCALAR_MUTE_N
Buzzer from PCH
20,22 SPKR
ALC233
(Include Thermal pad)
QFN48 (6x6)
Analog
Digital
Need to check timing in SA stage
Vref(Pin 28)/PDB(Pin47) timing
PDB
1.8V
Pin 28
Place close to Pin 27
Place close to Pin 26
Place close to pin 1
Place close to pin 9
PCB Trace width of
RING2 & SLEEVE at least 40 mil
R2703
Mount 20K for ALC233
Unmount for ALC233VB2
Mount R2714(or R2728) for ALC233VB2
R2724
Mount 100K for ALC233VB2
Unmount for ALC233
R2707= 200K for ALC233VB2
= 39.2K for ALC283/ALC233
speaker traces width >40mil when 2W4ohm speaker
(R) --> ALC233 / ALC233VB
0 Ω --> ALC283
ANALOG DIGITAL
Moat
In order to prevent the built-in LDO damaged from over-voltage on +5VS/S or Standby power line, we suggested using this Voltage suppressing device.
Grounding Circuit
for Combo Jack Sleeve pin
Used for ALC233 / ALC283 only
DIGITAL
ANALOG
To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power.
Place beep circuit nearby codec.
PCH Beep
Digital_ground
Analog_ground
Near AVDD1 and AVDD2 power source input
Tied at one point only under
Codec or near the Codec
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Audio Codec (ALC233)
A7400
Saturday, June 16, 2018

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Audio DSP&AMP_(3W)

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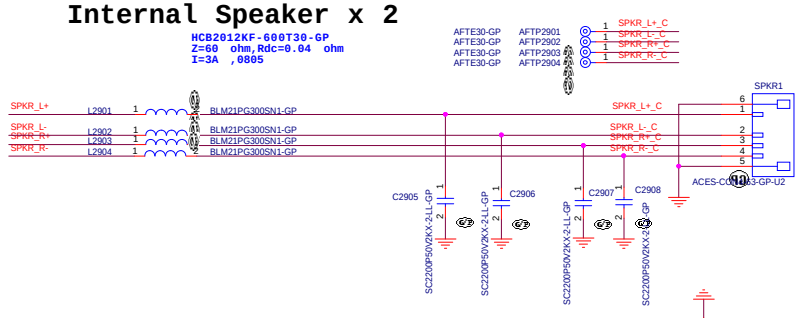
Date: Saturday, June 18, 2016 Sheet 28 of 107

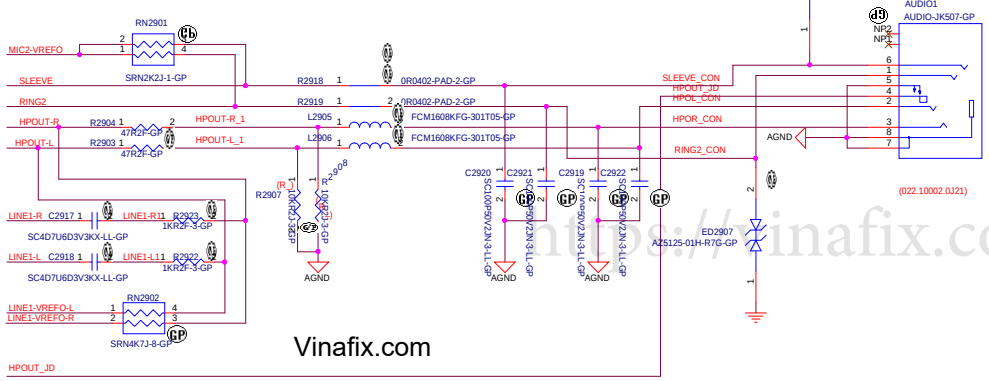
Internal Speaker x 2

HCB2012KF-600T30-GP
Z=60 ohm,Rdc=0.04 ohm
I=3A ,0805



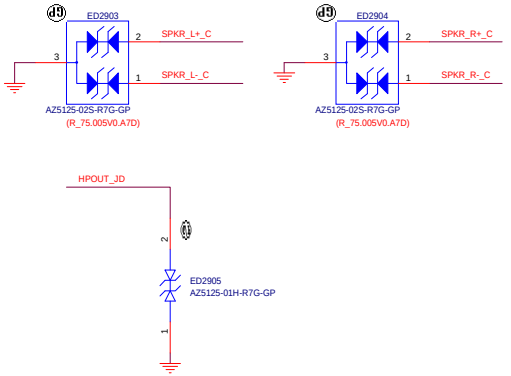
UAJ Headset

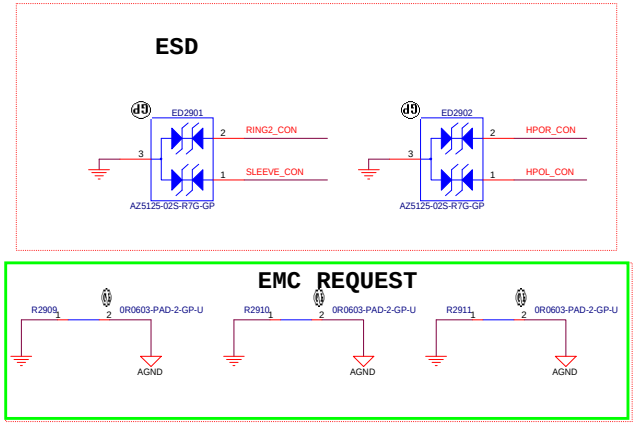
(ALC233 supported iPhone/Nokia headset, Headphone)

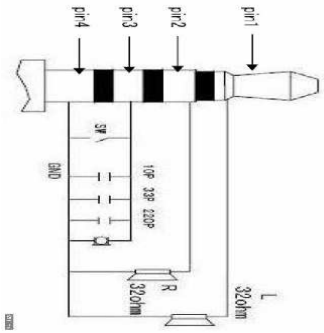


Vinafix.com

ESD

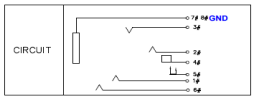


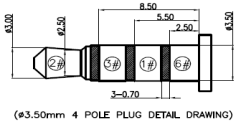




Pin Define:
Pin1: Ring2
Pin2: HP_L
Pin3: HP_R
Pin4: JD
Pin5: AGND
Pin6: Sleeve
Pin7: GND
Pin8: GND

B.COLOR
1.BLACK





4-pin 3.5mm Headset Connector Pinout

Nokia, Lenovo mobile		
Pin Number	**Pin Name**	**Description**
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Microphone**
4	Sleeve	**Ground / Common**

iPhone, Samsung, Blackberry, HTC		
Pin Number	**Pin Name**	**Description**
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Ground / Common**
4	Sleeve	**Microphone**

27 SPKR_L+
27 SPKR_L-
27 SPKR_R-
27 SPKR_R+

27 HPOUT_JD

27 LINE1-VREFO-L
27 LINE1-VREFO-R

27 HPOUT-L
27 HPOUT-R

27 LINE1-L
27 LINE1-R

27 MIC2-VREFO

27 SLEEVE
27 RING2

<variant_name>

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Audio Jack_(MIC/SPEA)(1/2)

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Date: Saturday, June 18, 2016 | Sheet 29 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Audio Jack_(function) (2/2)

Size	Document Number	Rev
A	A7400	-1B

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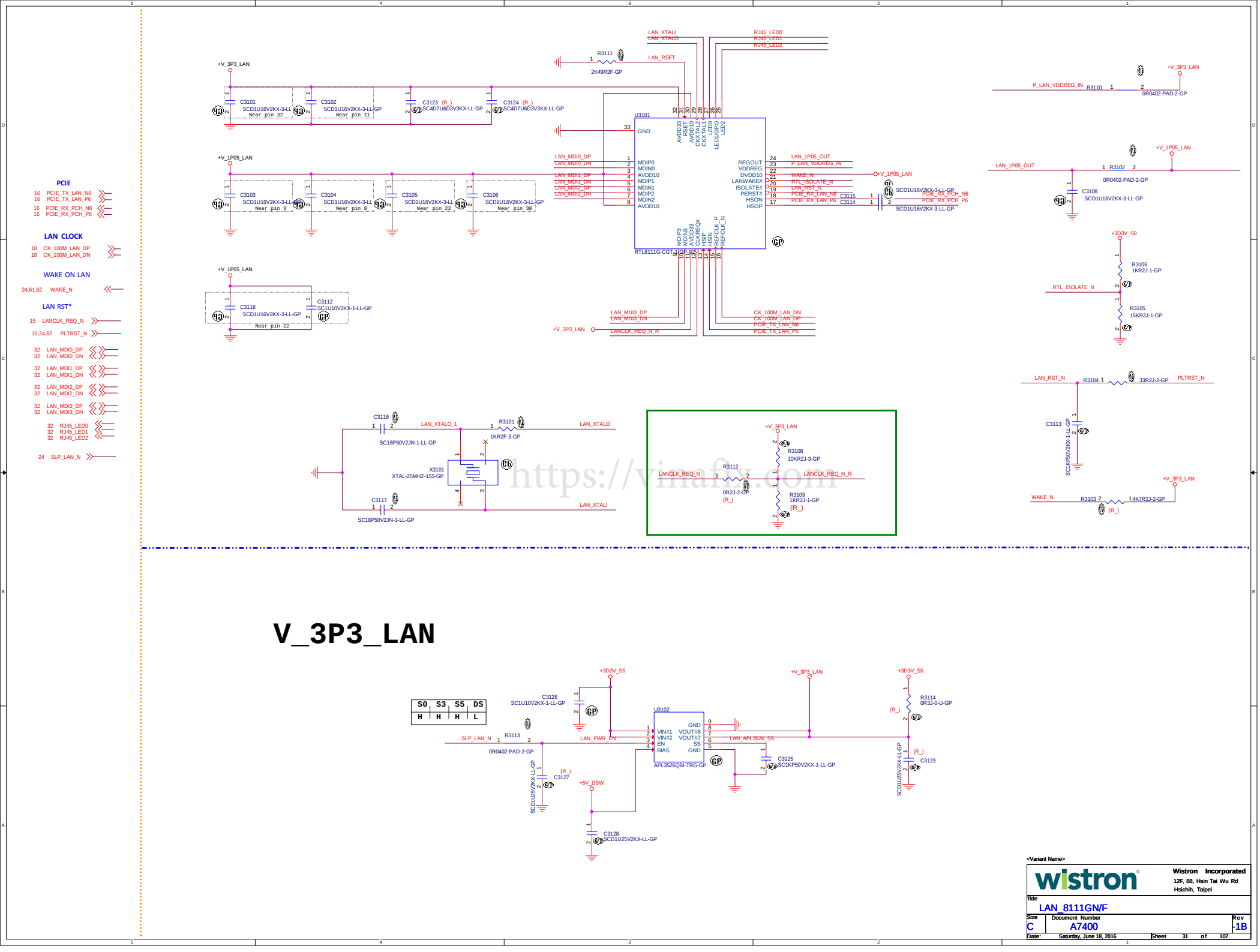
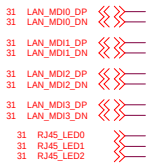
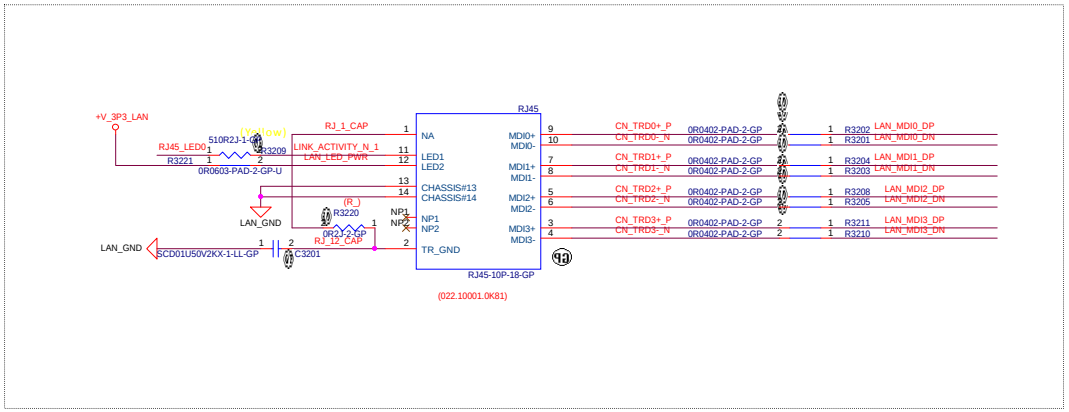


V_3P3_LAN

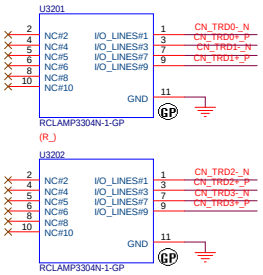


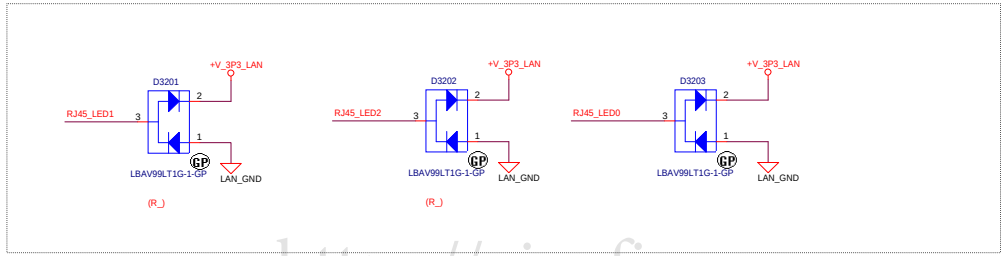


Blink

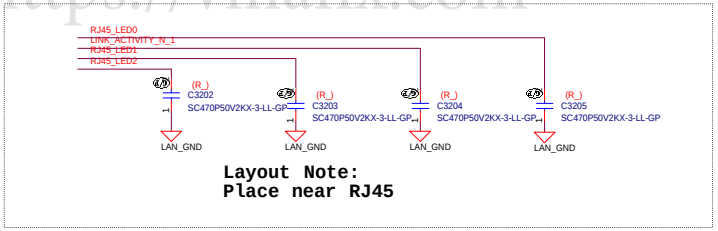
		Giga	100	10
Lef t LED	Link	Blink	Blink	Yellow
Right LED	Act	Orange	Green	X

Reserve RClamp





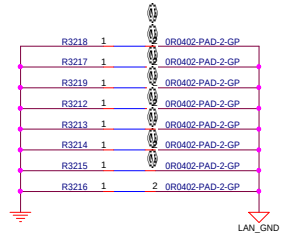
LINK_ACTIVITY_N==>RJ_LED0
SPEED_100_N ==>RJ_LED1
SPEED_1000_N ==>RJ_LED2



Layout Note:
Place near RJ45

L2 Previous component
68.00128.041: CHIP BEAD BK1005LL220-T TAIYO

C10 Previous component
78.10324.2FLLL: CHIP CAP C 0.01U 50V K0402 X7R
it is not Lily's component.

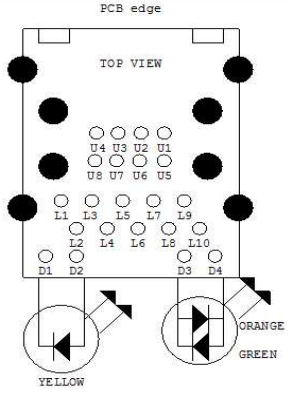


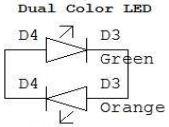
Layout Note:
Place around RJ45

RJ45 definition for LI

(1) LAN LED Status

WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		





Yellow: Domin Wavelength (λp) 582-593nm,Luminous Intensity (Iv) 12-50mcd.
Green: Domin Wavelength (λp) 567-578nm, Luminous Intensity (Iv) 10-50mcd.
Orange: Domin Wavelength (λp) 600-613nm, Luminous Intensity (Iv) 9-60mcd.
(2)need to follow "RJ45 common spec"

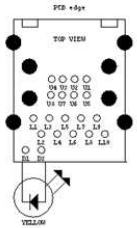
RJ45 common spec

1.2 definition for LC

(1) LAN LED Status

(2) Yellow: Domin Wavelength (λp) 582-593nm,Luminous Intensity (Iv) 12-50mcd.

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	



always on
blinking

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RJ45

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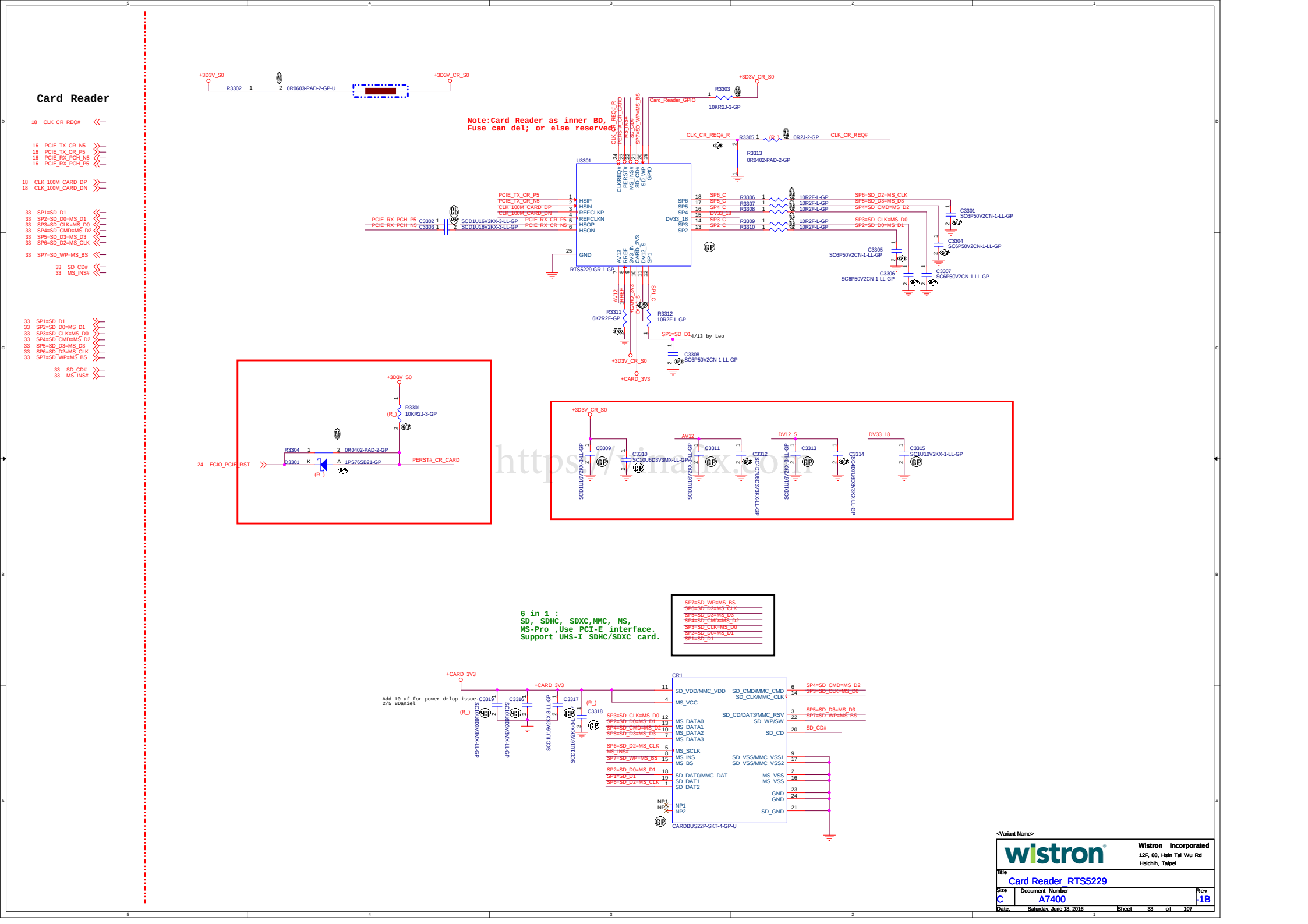
Card Reader



<variant_name>

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd, Hsichih, Taipei
Title	Card Reader_RTS5229
Size	C
Document Number	A7400
Rev	-1B
Date:	Saturday, June 18, 2016
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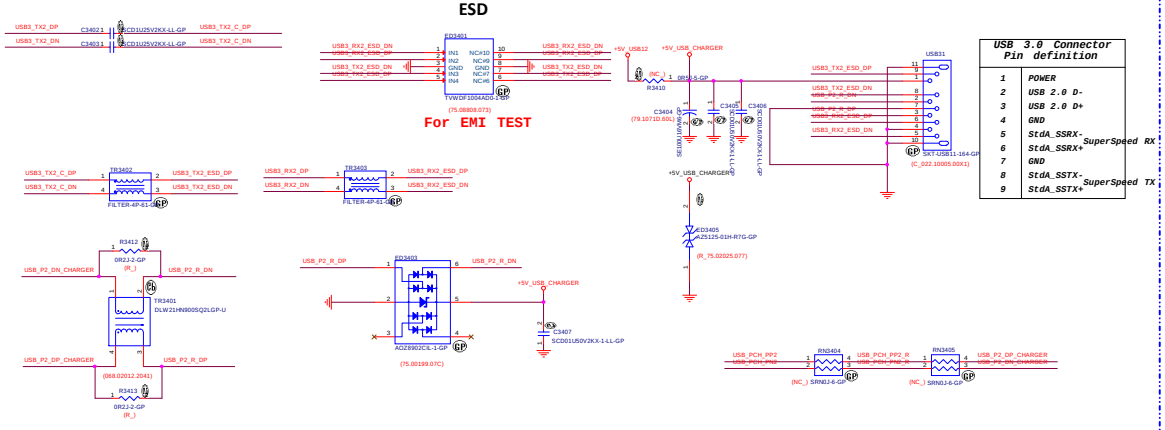
SIDE USB3.0 CONNECTOR

ESD



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

OTHERS (From ECIO)

24 USB_OC2_N
24 USB_CHARGE_FAULT_N
24 ECIO_CHAR_EN

CHARGER CTRL (From ECIO)

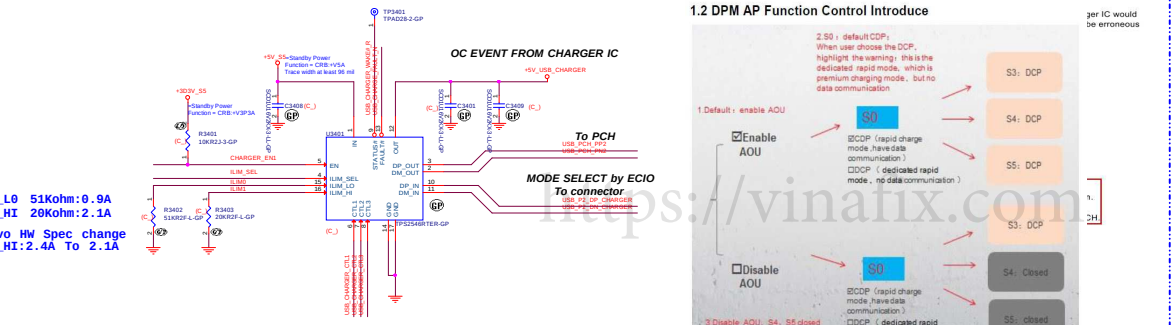
24 ECIO_ILIM_SEL
24 ECIO_CHAR_CTL1
24 ECIO_CHAR_CTL3
24 ECIO_CHAR_CTL2

USB 2.0

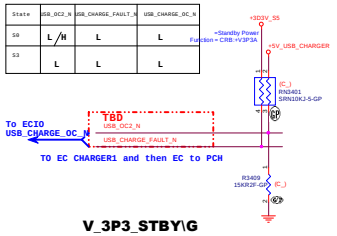
16 USB_PCH_PP2
16 USB_PCH_PN2

USB 3.0

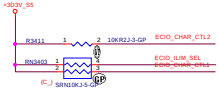
19 USB3_TX2_DP
19 USB3_TX2_DN
19 USB3_RX2_DP
19 USB3_RX2_DN

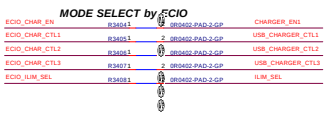


1.2 DPM AP Function Control Introduce



V_3P3_STBY\G





Control pin Truth Table Setting				
Mode	CTL1	CTL2	CTL3	ILIM_SEL
SDP(S3)	1	1	1	0
CDP(S0)	1	1	1	1
DCP(S4/S5)	0	1	1	1

Control Pin Settings Matched to System Power States

System Power State	Battery Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Max Battery Charging Current
S0	SDP	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI

S0:CDP 1.5A ==>1 1 1 1

S4/S5:DCP 1.5A ==>0 0 1 1

System Power State	Battery Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Max Battery Charging Current
S3/S4/S5	Auto mode, no load detection, no mouse wake	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

S3:SDP_HI 0.5A ==>0 1 1 1

Note:
1)All shaded boxes are device charging modes
2) See below table for CTL settings corresponding to flow line conditions

	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Default status:

ECIO_CHAR_CTL1	ECIO_CHAR_CTL2	ECIO_CHAR_EN	Mode	State
1	1	1	CDP	S0
0	1	1	DCP with HID auto detect USB data pass through	S3
0	0	1	DCP	S4/S5
0	0	0	Shut down	EN DSW and DIS CHAR on S4/S5

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB redrive#

Size: D | Document Number: A7400 | Rev: 1B

Date: Saturday, June 18, 2016 | Sheet 35 of 107

USB 3.0 X2

19 USB3_TX3_DN
19 USB3_TX3_DP
19 USB3_RX3_DN
19 USB3_RX3_DP

19 USB3_TX4_DN
19 USB3_TX4_DP
19 USB3_RX4_DN
19 USB3_RX4_DP

USB2.0X2==>

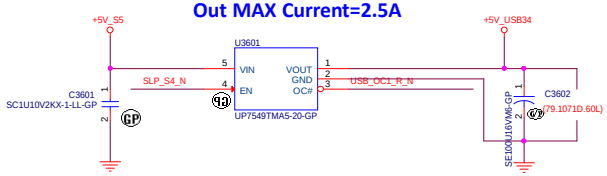
16 USB_PCH_PN3
16 USB_PCH_PP3

16 USB_PCH_PN4
16 USB_PCH_PP4

16 USB_OC1_R_N

8,20,24,38,39,40 SLP_S4_N

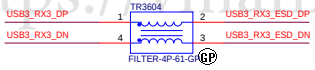
Out MAX Current=2.5A

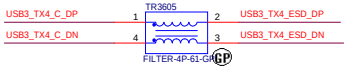


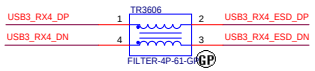
Coupling caps

From PCH USB3.0 port TX

USB 3.0







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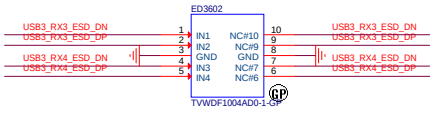

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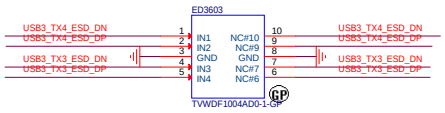
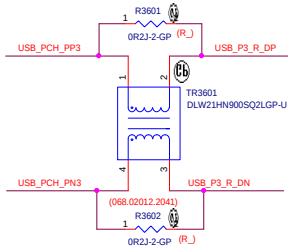
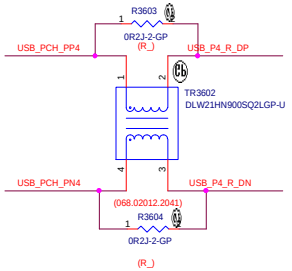


USB 2.0





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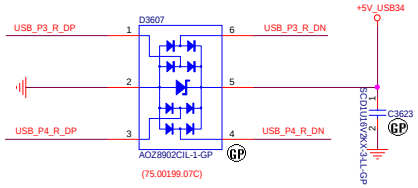

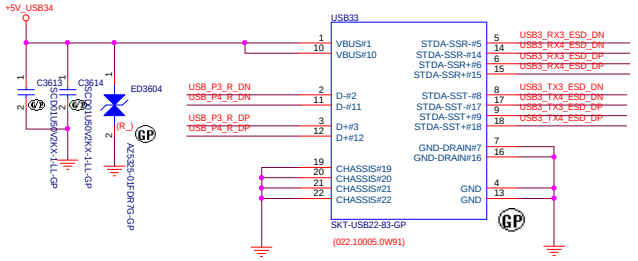

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
USB20_(BIOS RECOVERY)#

Size	Document Number	Rev
C	A7400	-1B

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24 USB_P1_CNN_DP
24 USB_P1_CNN_DN

8,20,24,36,39,40 SLP_S4_N

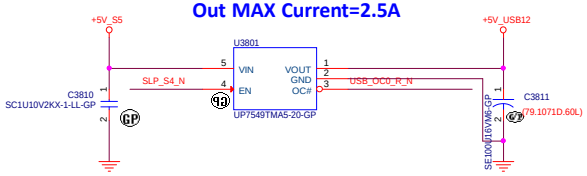
19 USB3_TX1_DP
19 USB3_TX1_DN
19 USB3_RX1_DP
19 USB3_RX1_DN

To PCH USB OC pin

16 USB_OC0_R_N

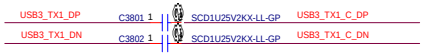
24 UART_P80_EN

Out MAX Current=2.5A

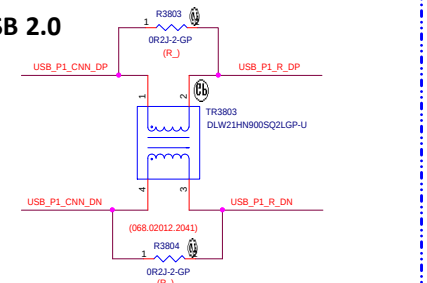


Coupling caps

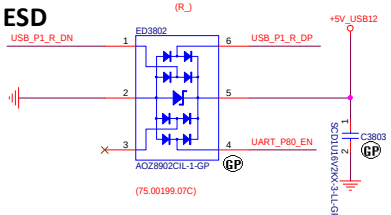
From PCH USB3.0 port TX



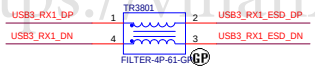
USB 2.0



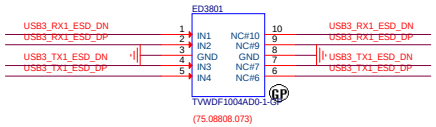
ESD



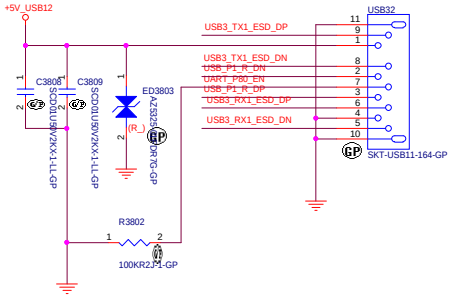
USB 3.0



ESD



USB Debug port



<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB30

Size	Document Number	Rev
C	A7400	-1B

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16 USB_PCH_PN5
16 USB_PCH_PP5
16 USB_PCH_PN6
16 USB_PCH_PP6
8,20,24,36,38,40 SLP_S4_N

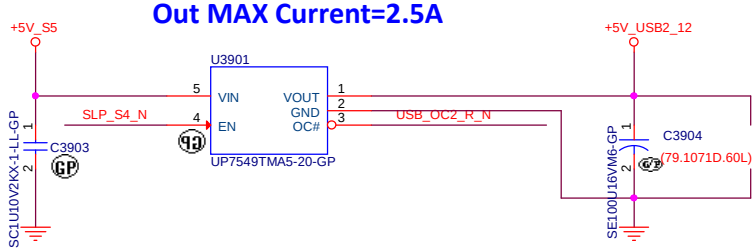
To FCH USB OC pin

16 USB_OC2_R_N

USB2.0 PORT4

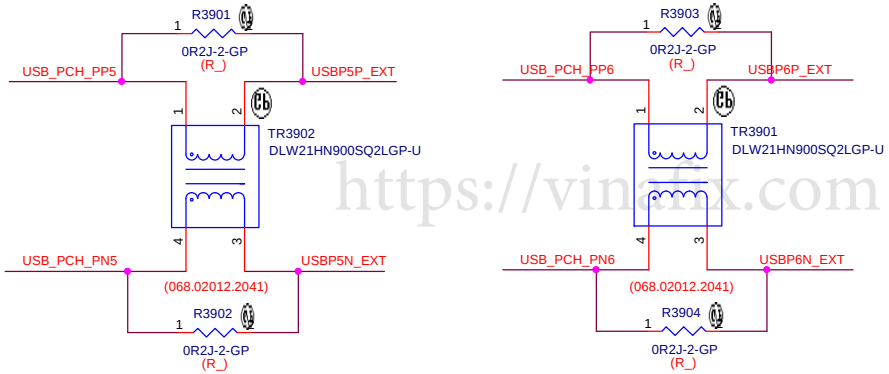
16,36 USB_PCH_PN4
16,36 USB_PCH_PP4

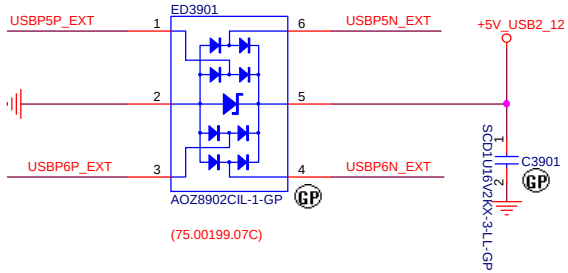
Out MAX Current=2.5A

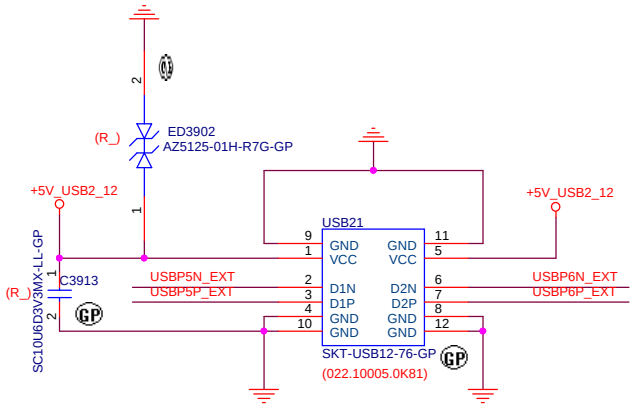


Vinafix.com

USB 2.0







<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB30_PORT1234 USB SW

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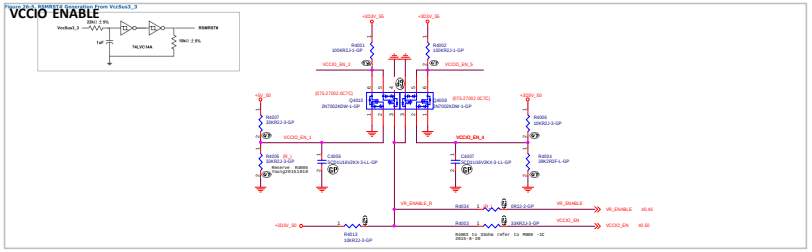
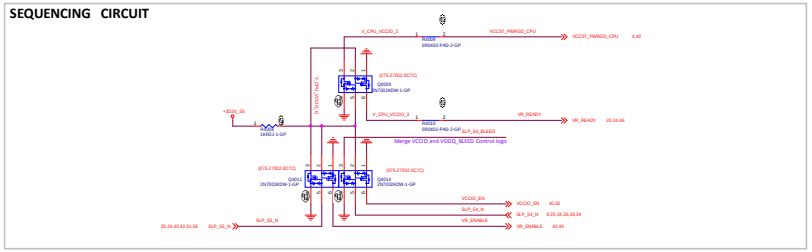
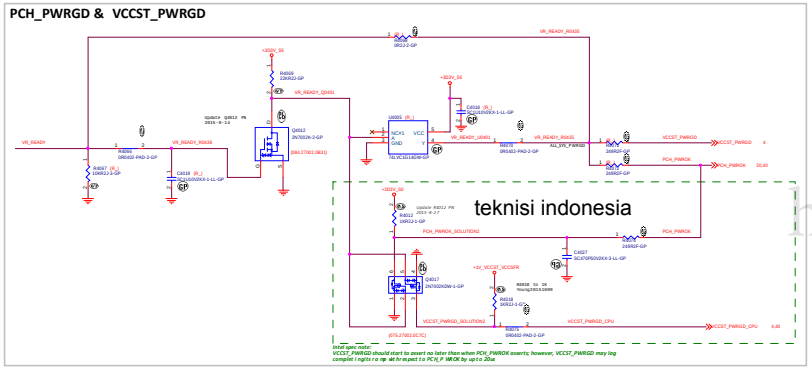
VCCIO ENABLE



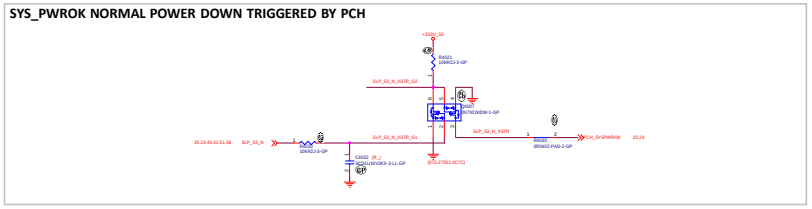
SEQUENCING CIRCUIT



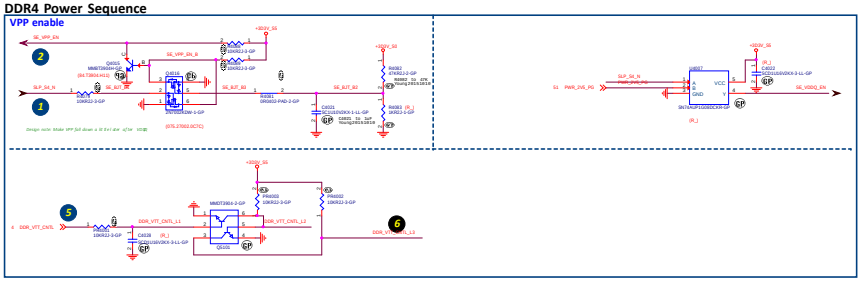
PCH_PWRGD & VCCST_PWRGD



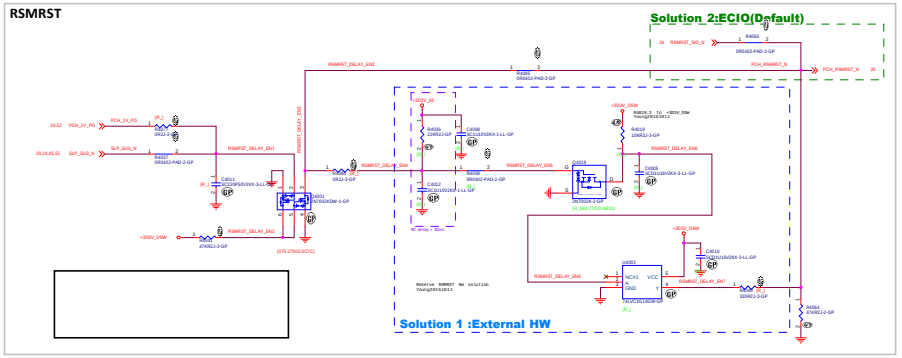
SYS_PWROK NORMAL POWER DOWN TRIGGERED BY PCH



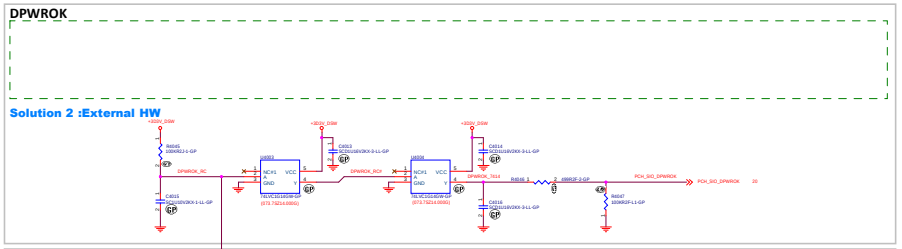
DDR4 Power Sequence



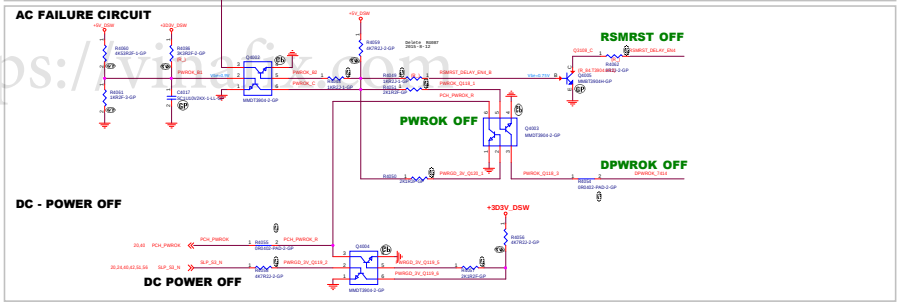
RSMRST



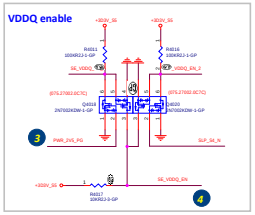
DPWROK

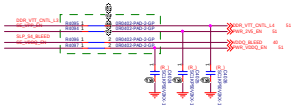


AC FAILURE CIRCUIT

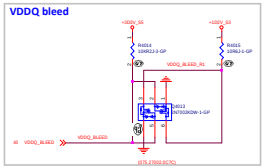


VDDQ enable

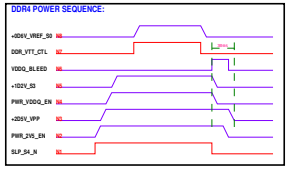




VDDQ bleed



DDR4 POWER SEQUENCE:



Wistron Incorporated			
Power Plane EN Sequence			
Size	Document Number		Rev
Custom	A7400		1S
Date: Monday, June 29, 2015		Sheet 48 of 87	

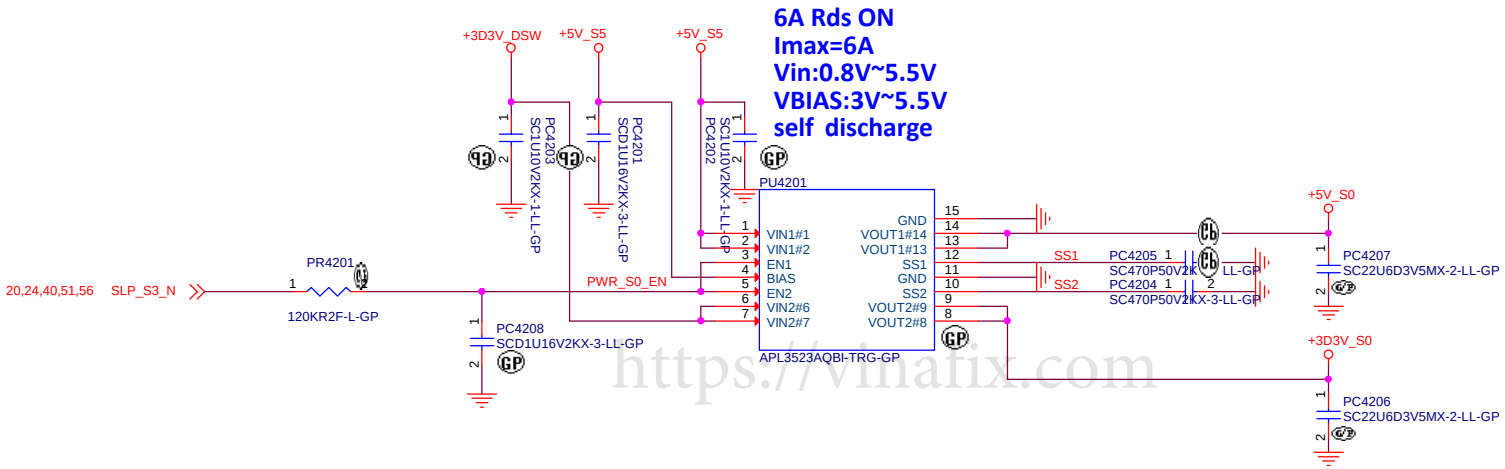
Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Switch power-(R) +DS3		
Size: A	Document Number: A7400	Rev: -1B
Date: Saturday, June 18, 2016	Sheet 41 of 107	

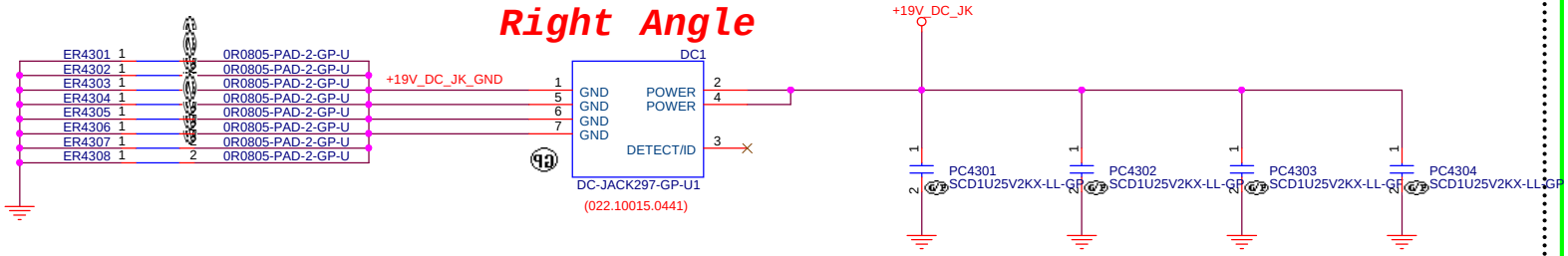


<Variant Name>

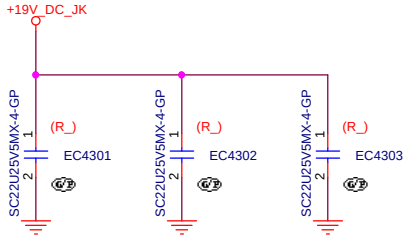
Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	PWR_+5V_S0/ +5V_S3/+3.3V_S0
Size: B	Document Number: A7400 — Rev: -1B
Date: Saturday, June 18, 2016	Sheet 42 of 107

Adapter path==>

Right Angle



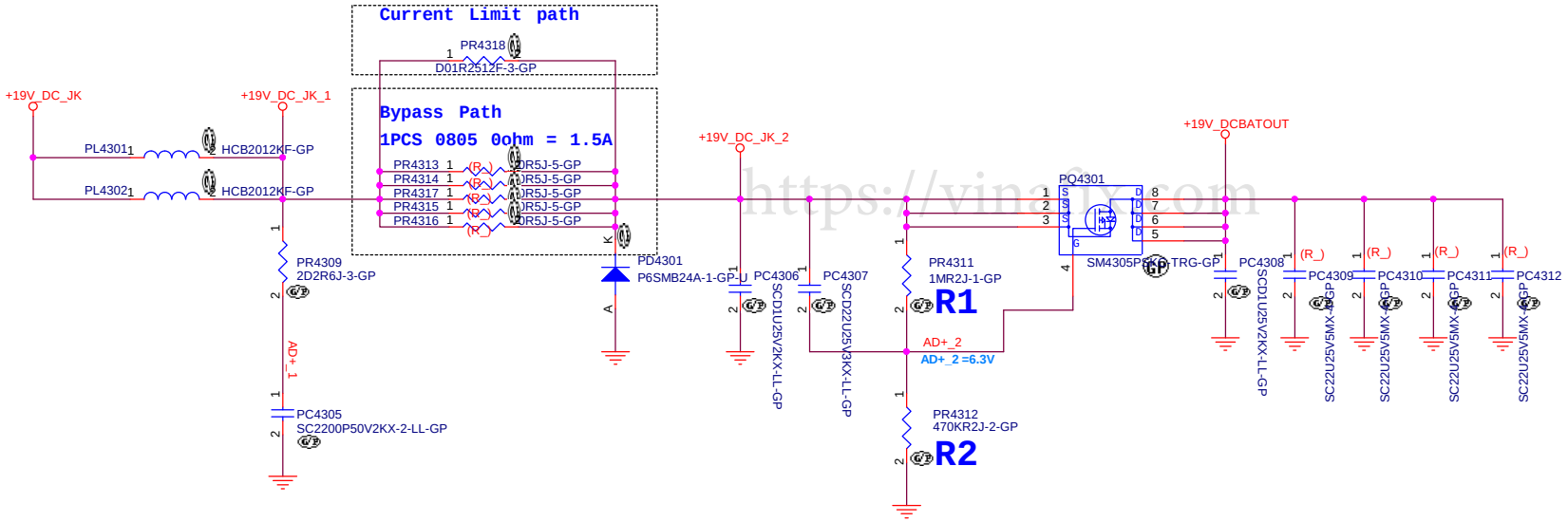
Add for EMI/EMC

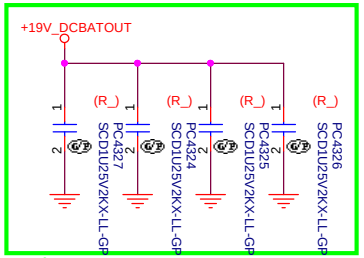


Current Limit path

Bypass Path

1PCS 0805 0ohm = 1.5A



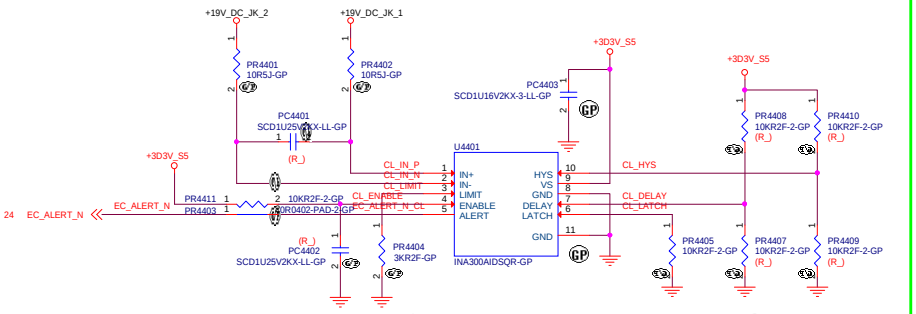


EMI/EMC

<Variant Name>

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	ATX(BATT Conn)
Size: B	Document Number: A7400 Rev: -1B
Date: Saturday, June 18, 2016	Sheet 43 of 107

Current meter



HYSTERESIS	HYSTERESIS SETTING
Floating	2mV
GND	4mV
VSS	8mV

DELAY	ALERT DELAY (µ s)
Floating	10uS
GND	50uS
VSS	100uS

OUTPUT MODE	LATCH SETTING
Transparent mode	LATCH = low
Latch mode	LATCH = high

	PARAMETER	EQUATION
VTRIP	Desired current trip value	ILOAD × RSENSE
VLIMIT	Programmed threshold limit voltage	VLIMIT = VTRIP
VLIMIT(1)	Threshold voltage	(ILIMIT × RLIMIT) – NAF
RLIMIT(1)	Threshold limit setting resistor	(VLIMIT + NAF) / ILIMIT
RLIMIT(1)	Limit setting resistor	(VLIMIT + 500 µ V) / 20 µA

(1) NAF is used with the 10-µ s delay setting. NAF can be omitted in the RLIMIT calculation for the 50-µ s and 100-µ s delay setting

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

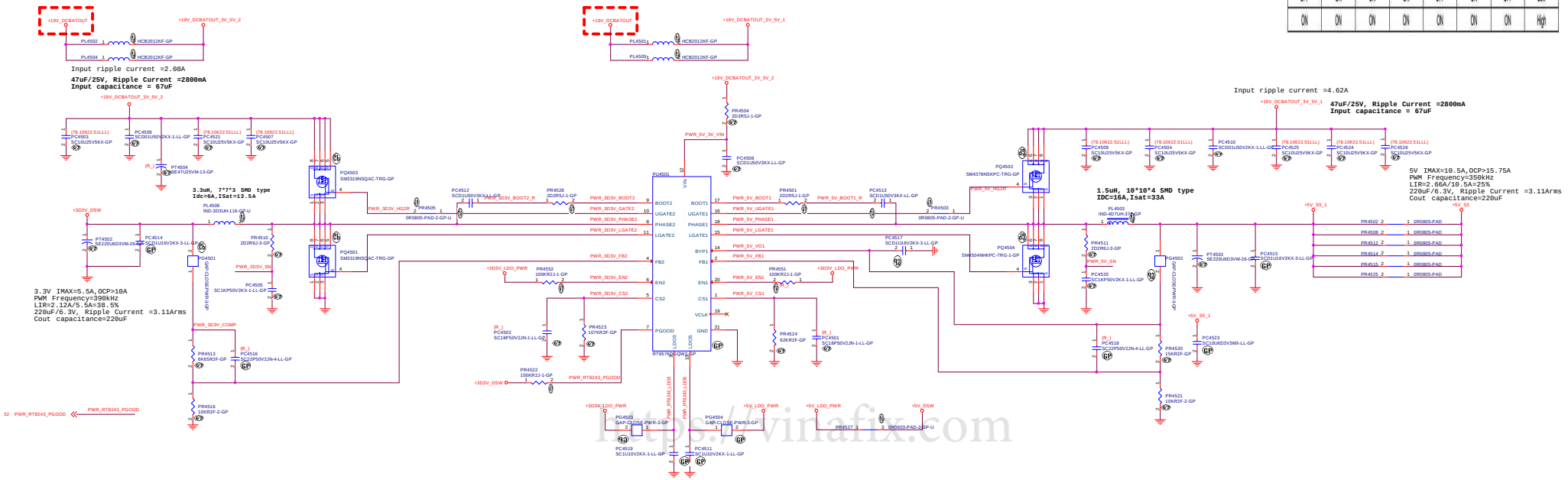
Title: Power meter

Size: C | Document Number: A7400 | Rev: -1B

Date: Saturday, June 18, 2016 | Sheet 44 of 107

Table 1. Enabling/PGOOD State (TPS51275B/C)

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High



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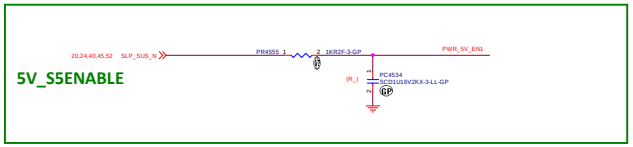
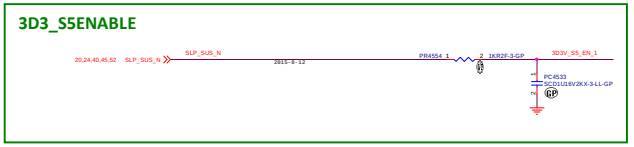
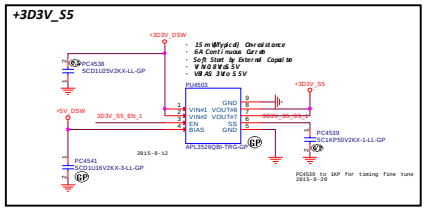
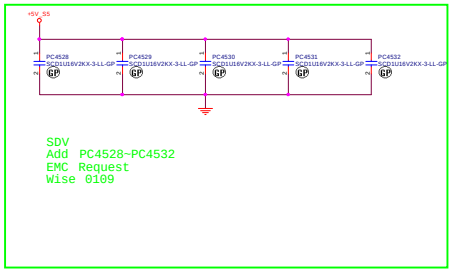
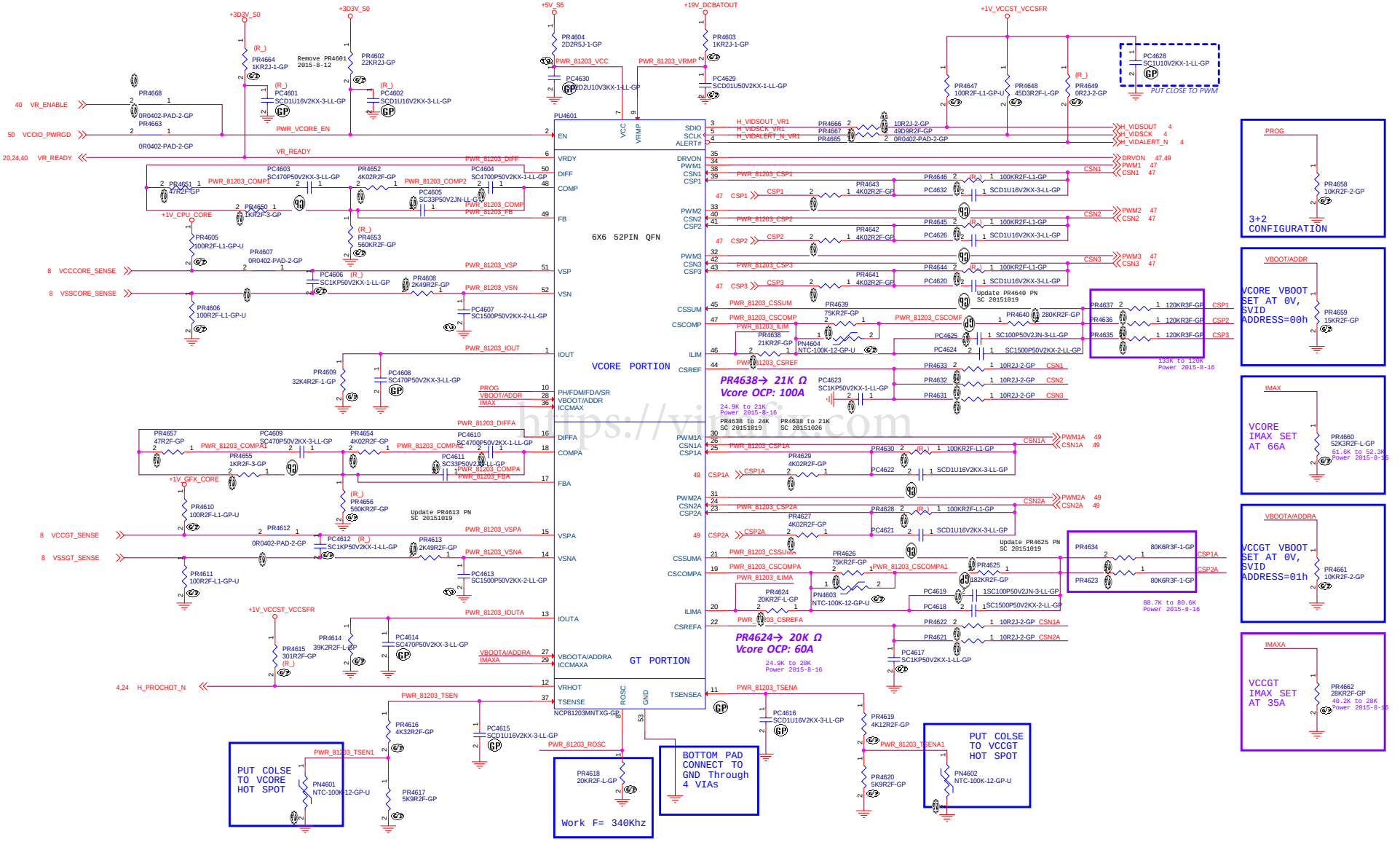








Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VCORE(NCP81102)

Size	Document Number	Rev
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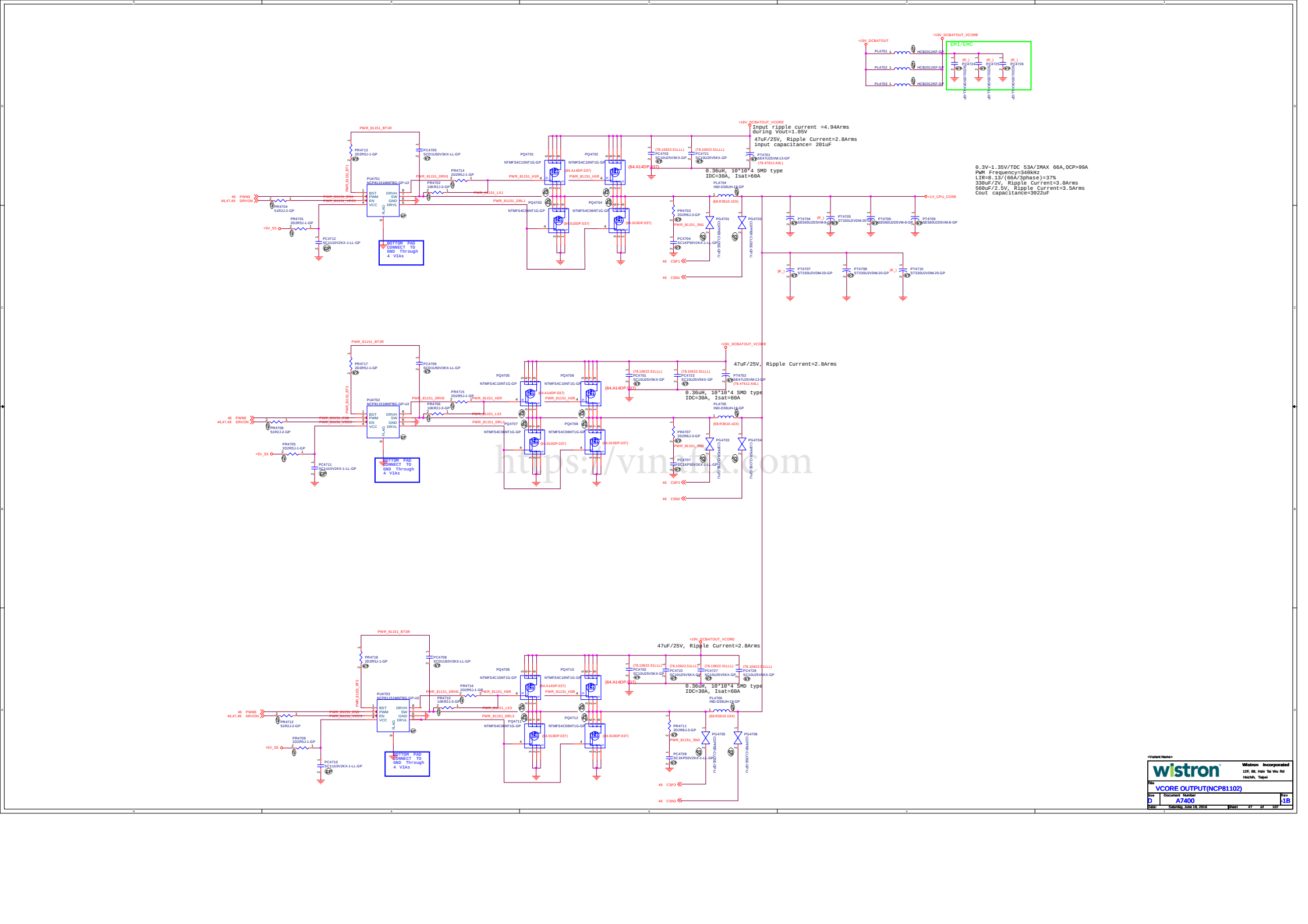
Date: Saturday, June 18, 2016 Sheet 46 of 107


EMI/EMC
Input ripple current =4.94Arms during Vout=1.05V
47uF/25V, Ripple Current=2.8Arms
input capacitance= 201uF
0.36uH, 10*10*4 SMD type
IDC=30A, Isat=60A
0.3V~1.35V/TDC 53A/IMAX 66A,OCP>99A
PWM Frequency=340kHz
LIR=8.13/(66A/3phase)=37%
330uF/2V, Ripple Current=3.0Arms
560uF/2.5V, Ripple Current=3.5Arms
Cout capacitance=3022uF
47uF/25V, Ripple Current=2.8Arms
0.36uH, 10*10*4 SMD type
IDC=30A, Isat=60A
47uF/25V, Ripple Current=2.8Arms
0.36uH, 10*10*4 SMD type
IDC=30A, Isat=60A
BOTTOM PAD CONNECT TO GND Through 4 VIAs
BOTTOM PAD CONNECT TO GND Through 4 VIAs
BOTTOM PAD CONNECT TO GND Through 4 VIAs
+19V_DCBATOUT
+19V_DCBATOUT_VCORE
+1V_CPU_CORE
+5V_S5
PWM1
DRVON
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
NCP81151MNTBG-GP-U2
NTMFS4C10NT1G-GP
NTMFS4C06NT1G-GP
IND-D36UH-10-GP
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
VCORE OUTPUT(NCP81102)
Size D
Document Number A7400
Rev 1B
Date: Saturday, June 16, 2018
Sheet 47 of 107

Reserved

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU Core_		
Size: A	Document Number: A7400	Rev: -1B
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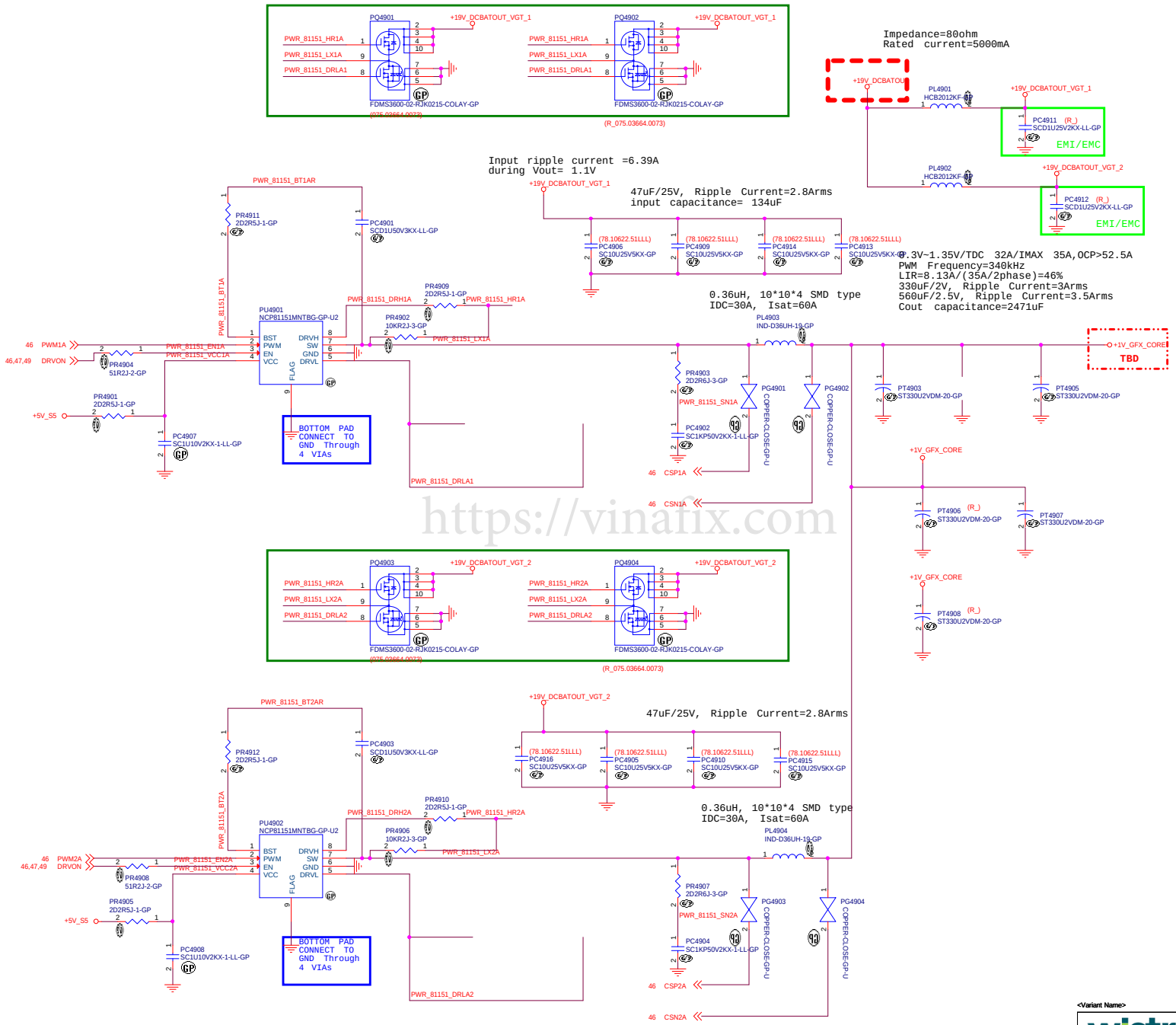

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: V_GT OUTPUT(NCP81151)

Size	Document Number	Rev
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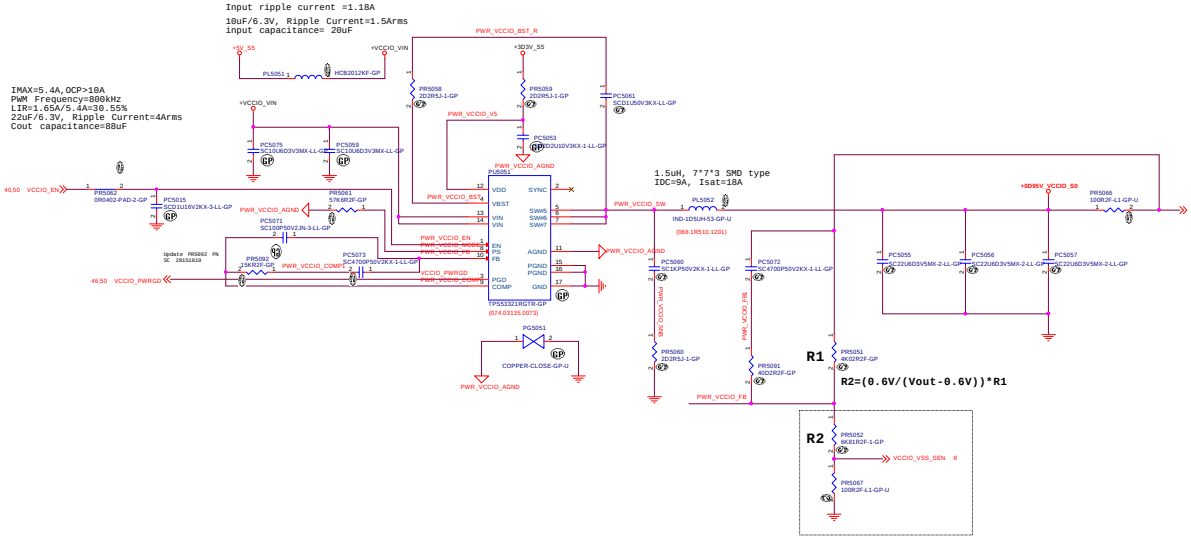
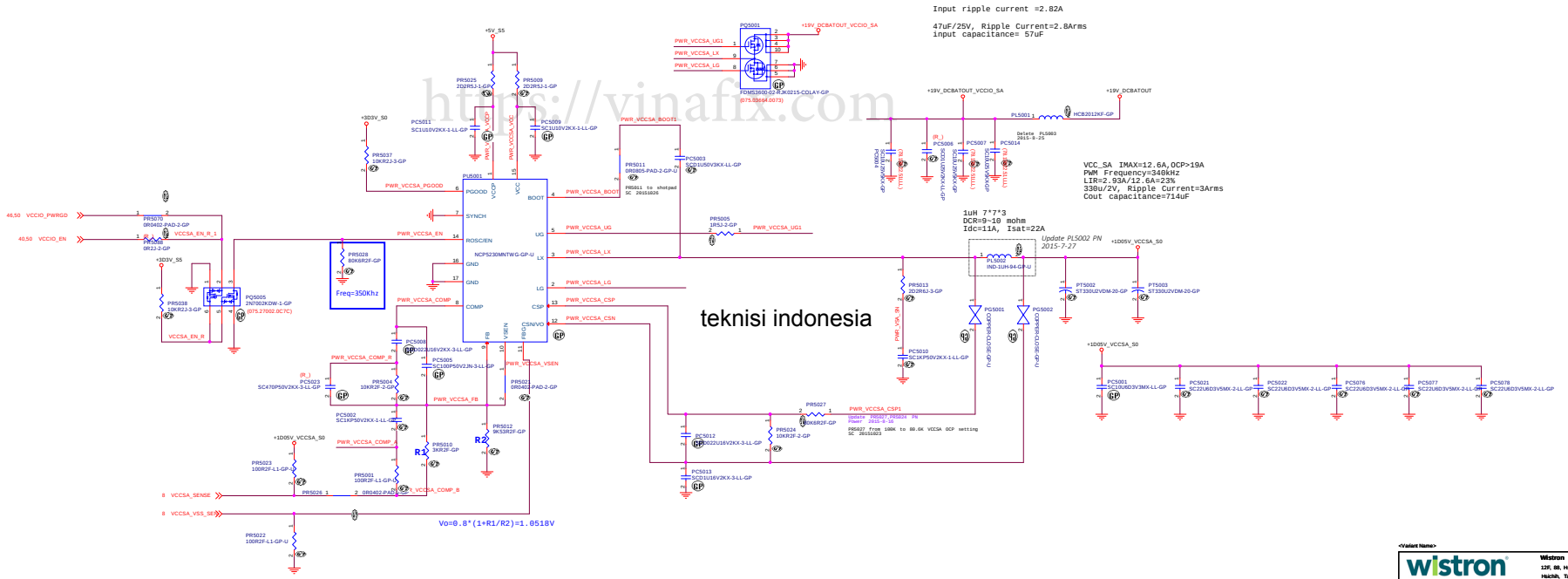
VCCIO



VCCSA



Wistron Incorporated
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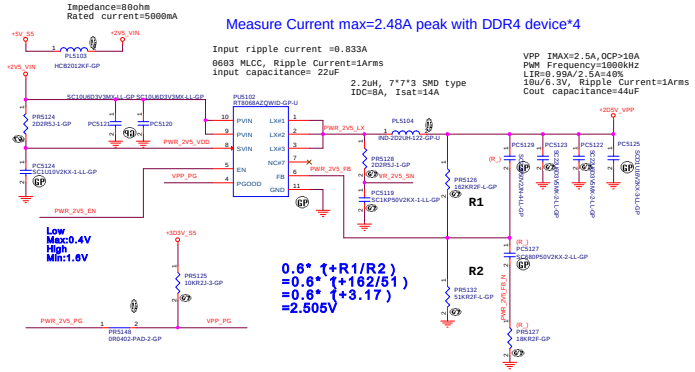
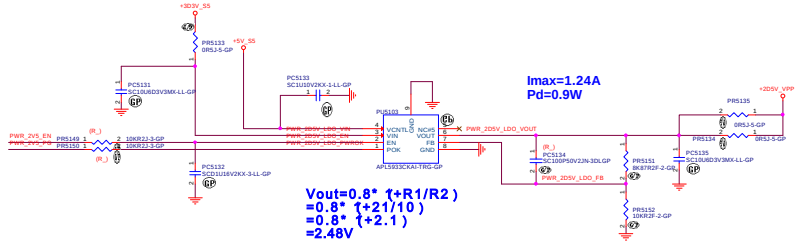
Hsichih, Taipei

Title	V_3P3_A	
Size: D	Document Number: A7400	Rev: 1B
Date: Saturday, June 18, 2016	Sheet 50 of 107	

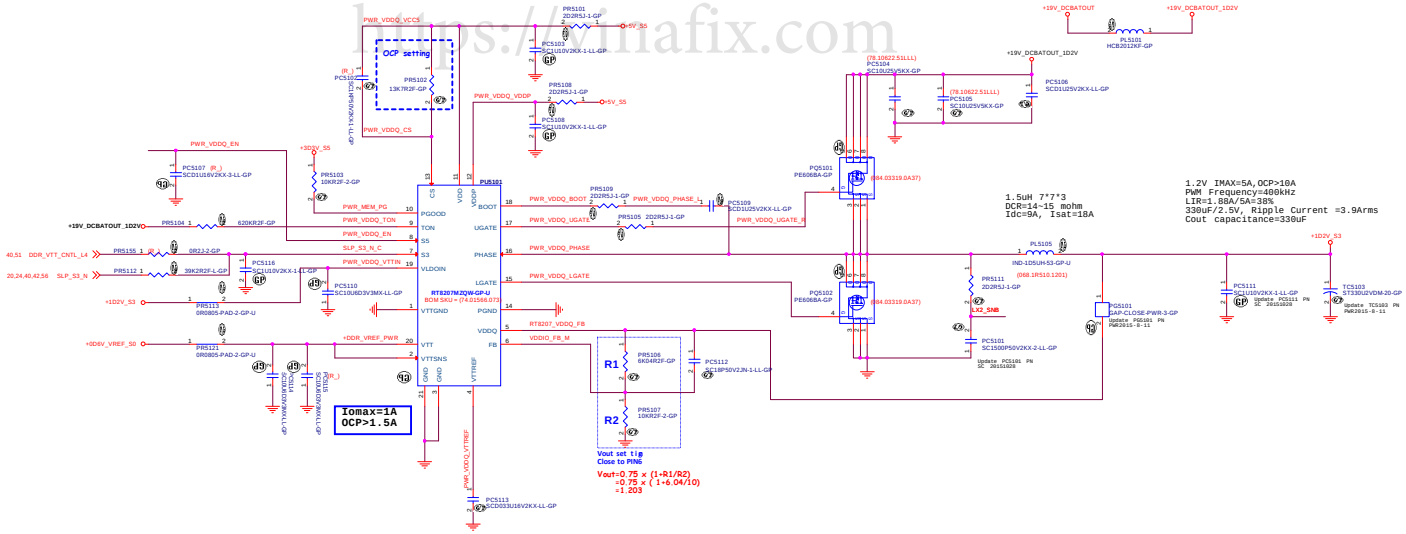
+2D5V_VPP





40 PWR_2V5_EN
40 PWR_VDDQ_EN
40,51 DDR_VTT_CNTL_L4
40 PWR_2V5_PG

+1D2V_S3
+0D6V_VREF_S0



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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: 051_MEM/MEMVTT (1589)

Size: D | Document Number: A7400 | Rev: -1B

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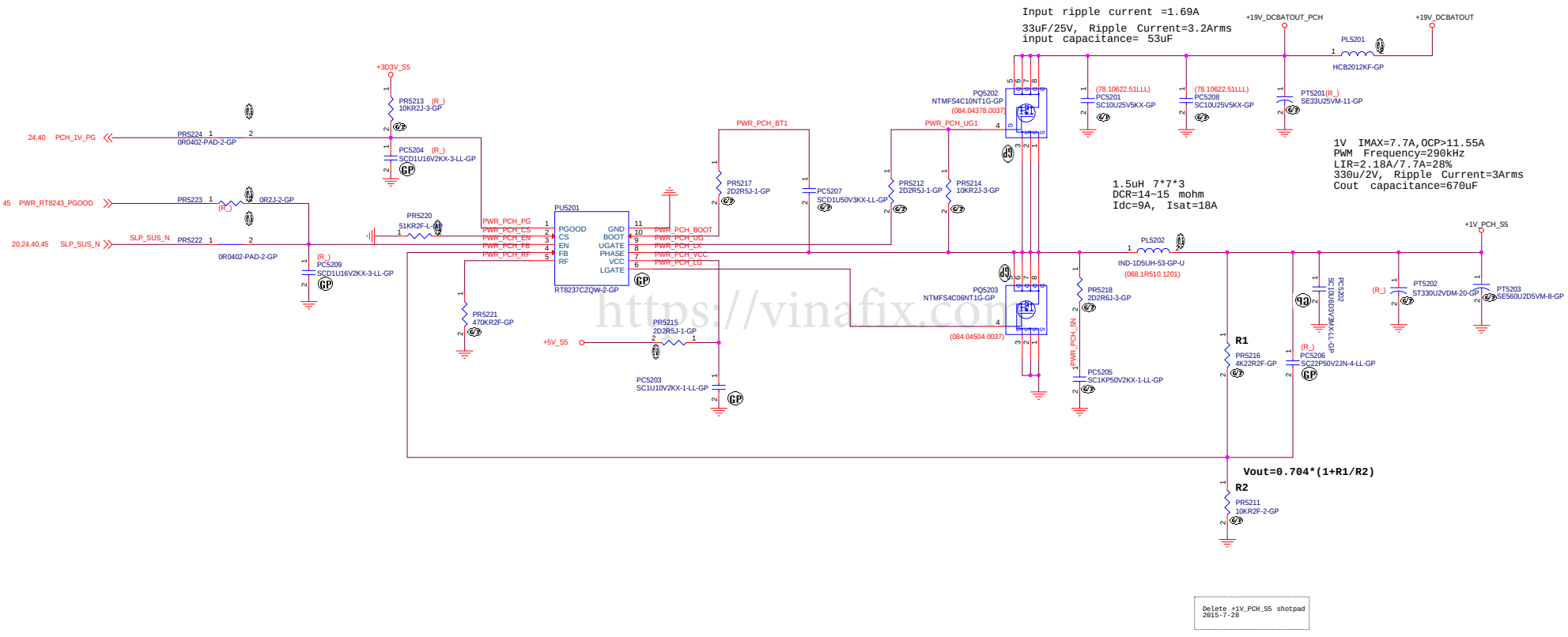
+1V_PCH_S5



<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DCDC-1D05V(NCP1589A)

Size	Document Number	Rev
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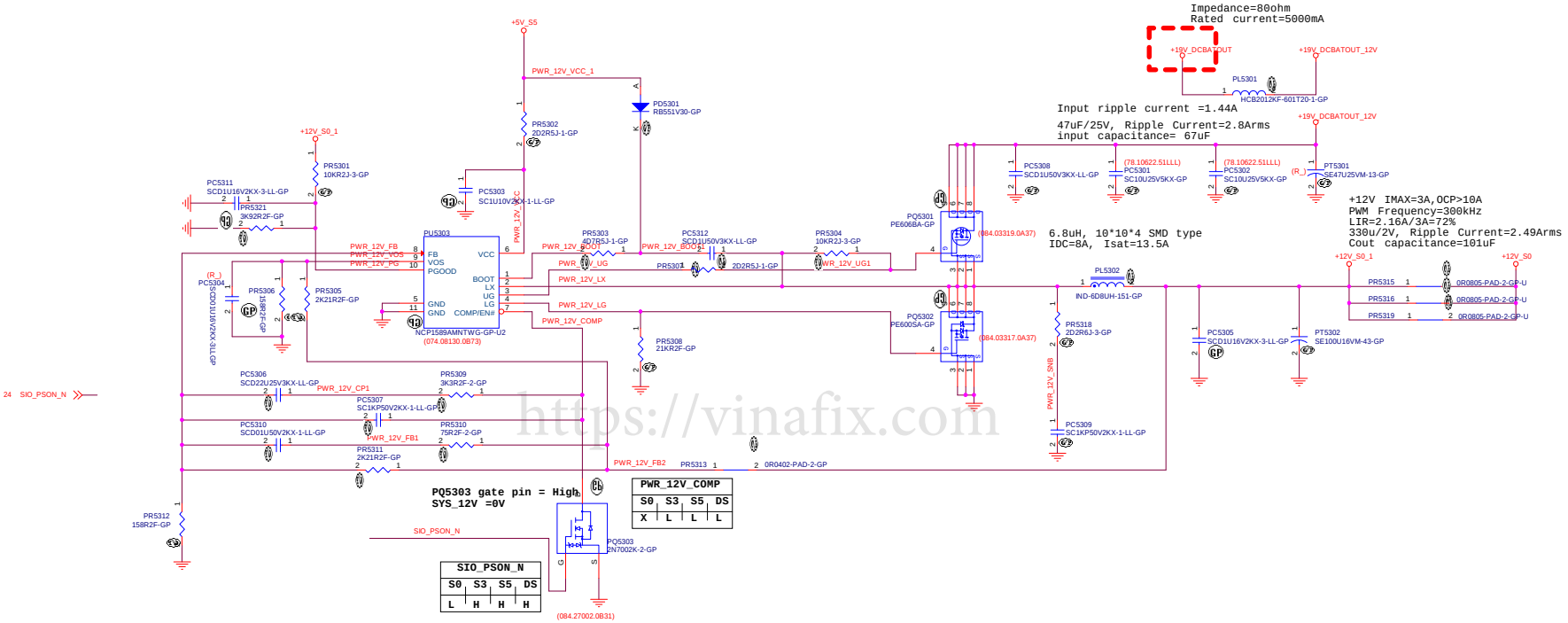

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PWR_12V(NCP1589A)

Size: A2 | Document Number: A7400 | Rev: -1B

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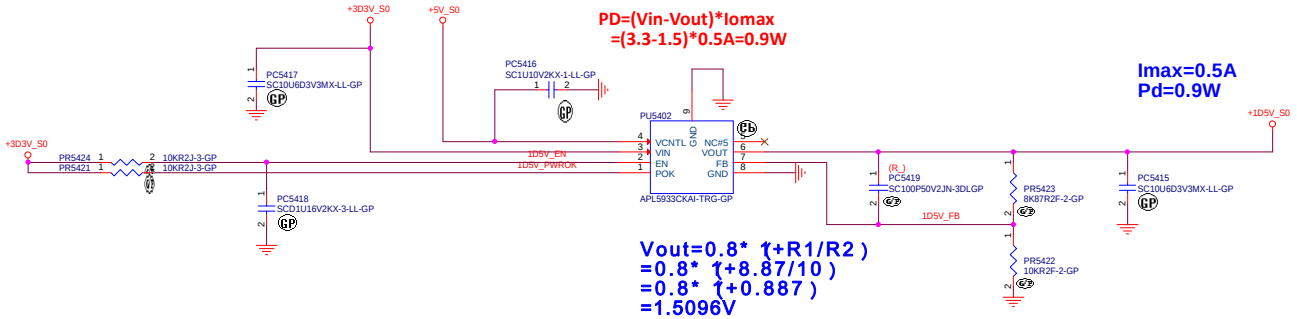

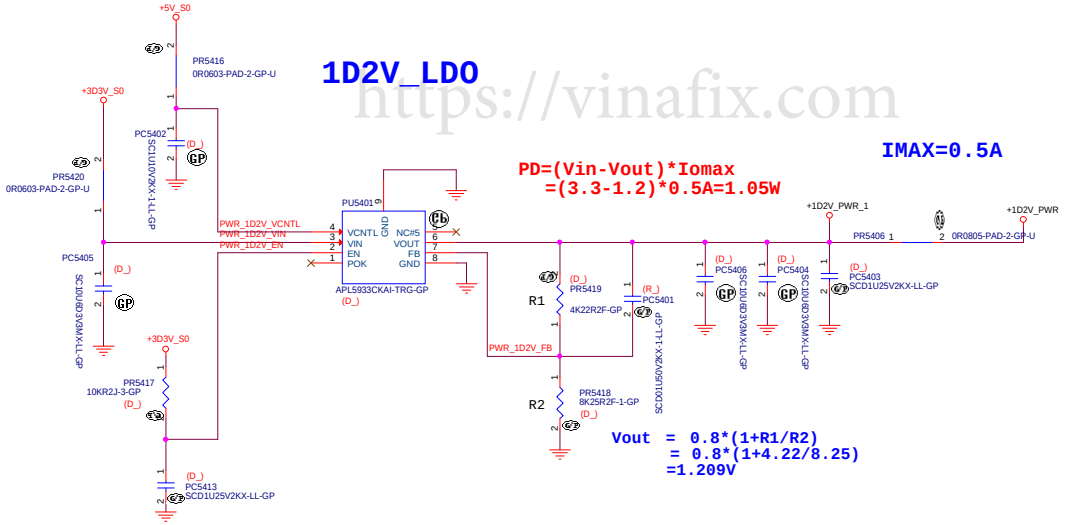

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LDO-1.5V & 1.2V

Size	Document Number	Rev
C	A7400	-1B

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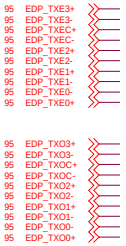
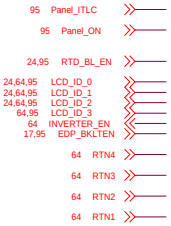
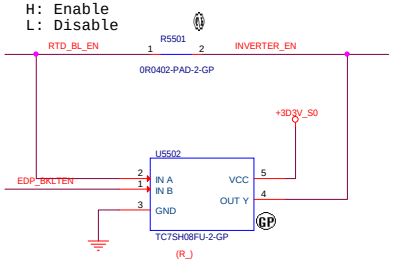
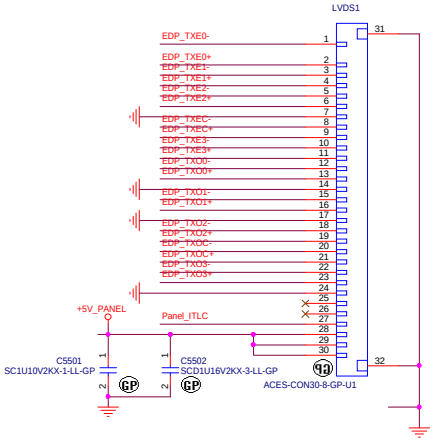
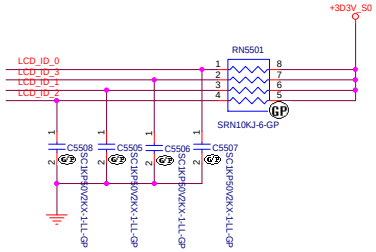


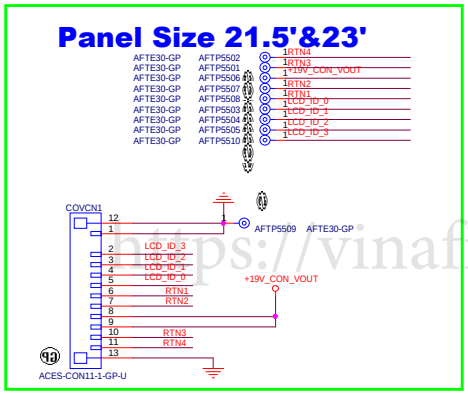


H: Enable
L: Disable









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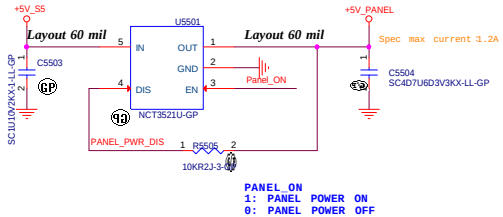

PANEL_ON
1: PANEL POWER ON
0: PANEL POWER OFF

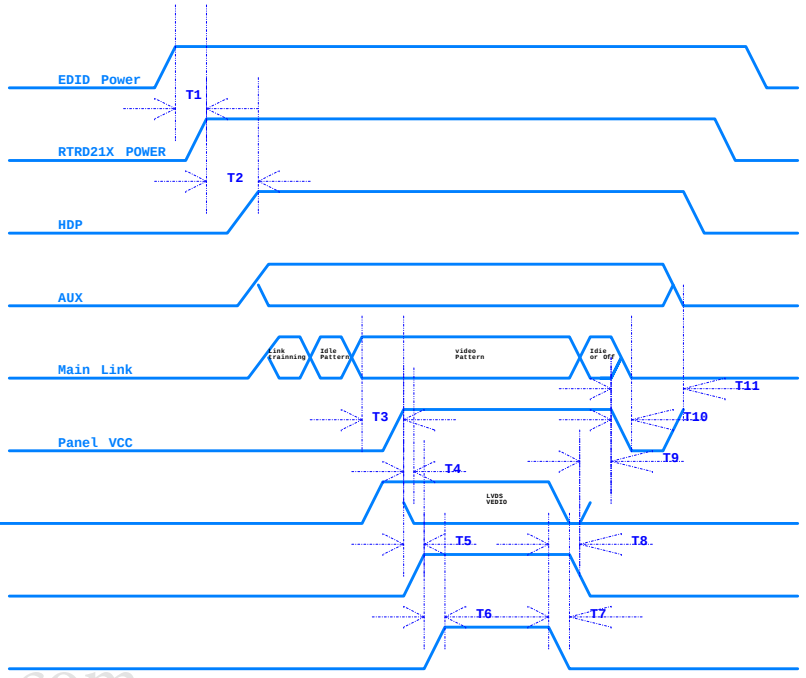

Table 7 Timing Parameters of Power on/off Sequence

Time Para.	Description	Min.(ms)	Max.(ms)
T_1	Delay from EDID power active to DP2LVDS power active	0	--
T_2	Delay from DP2LVDS power active to HPD asserted	0	70
T_3	Rising time of Panel Vcc	0.5	10
T_4	Delay from Panel Vcc output enable to LVDS output enable	0	50
T_5	Delay from LVDS output enable to backlight output enable	200	--
T_6	Delay from PWM output enable to backlight output enable	0	--
T_7	Delay from backlight output disable to PWM out disable	0	--
T_8	Delay from backlight output disable to LVDS output disable	200	--
T_9	Delay from LVDS output disable to Panel Vcc out disable	0	50
T_{10}	Falling time of Panel Vcc	0.5	10
T_{11}	Delay between two panel power on/off sequence	500	--

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	4.5	5	5.5	V	-
Ripple Voltage		V_{RP}	-	-	300	mV	-
Rush Current		I_{RUSH}	-	2.5	3	A	(2)
Power Supply Current	White	-		0.5	0.9	A	(3)a
	Black	-		0.8	1.2	A	(3)b
	Vertical Stripe	-		0.5	0.9	A	(3)c
Power Consumption		PLCD			6	Watt	(4)
LVDS differential input voltage		Vid	100	-	600	mV	
LVDS common input voltage		Vic	1.0	1.2	1.4	V	
Logic High Input Voltage		VIH	-	-	0.1	V	
Logic Low Input Voltage		VIL	-0.1	-	-	V	

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LCD/Converter Connector

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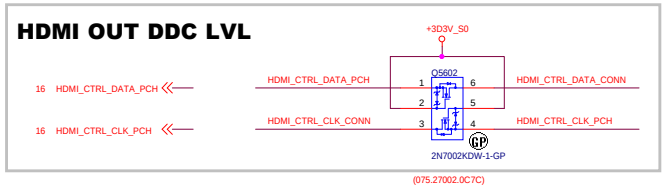
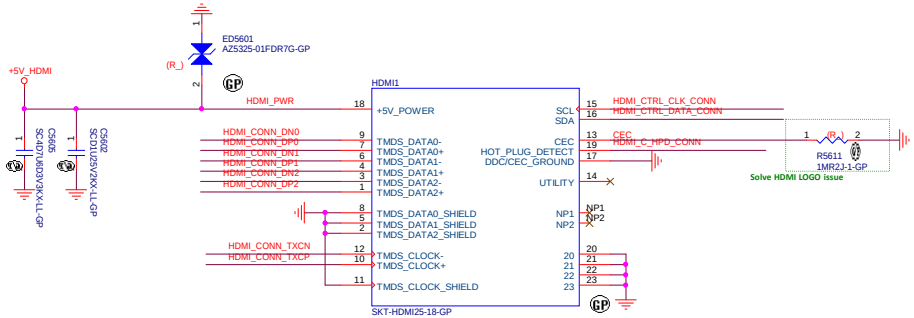
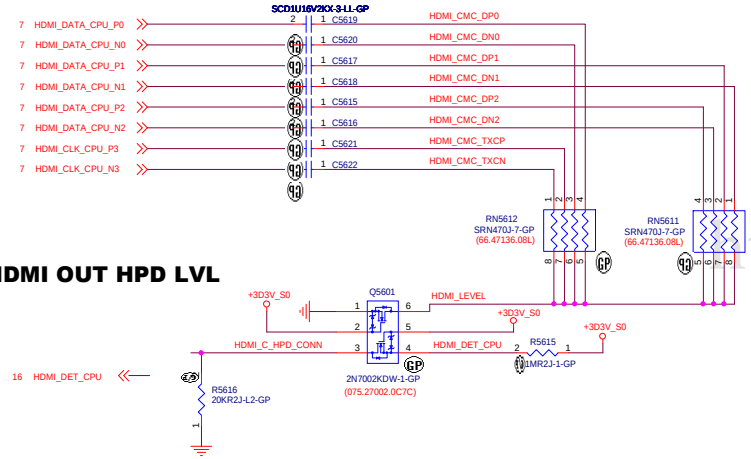
Date: Saturday, June 18, 2016 | Sheet 55 of 107

HDMI OUT DDC LVL

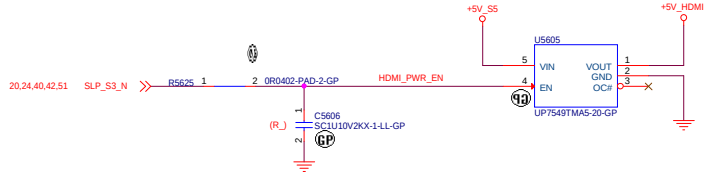




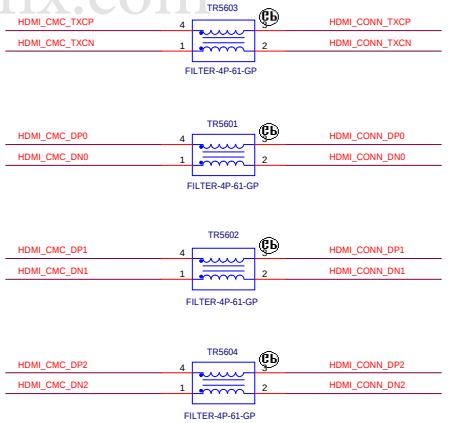
HDMI out Reduced Level Shift

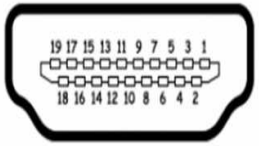


HDMI OUT HPD LVL



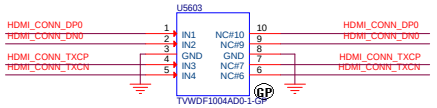
CMC

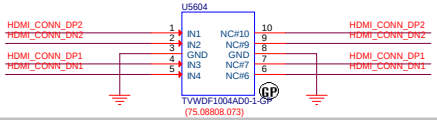


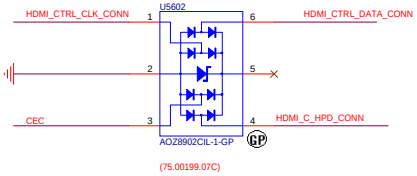


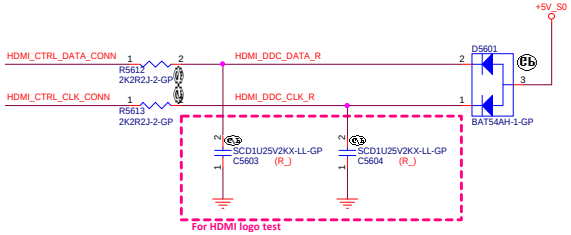
Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		

ESD









<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	HDMI	
Size: C	Document Number: A7400	Rev: -1B
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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DP_out

Size	Document Number	Rev
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Reserved

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DVI_

Size	Document Number	Rev
A	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 58 of 107

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Display switch_#

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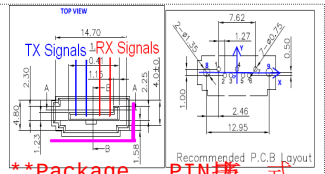
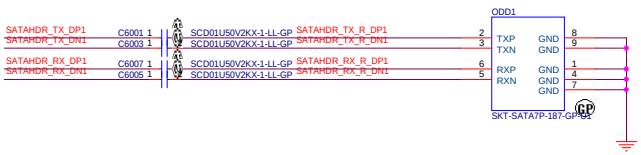
PCH SATA

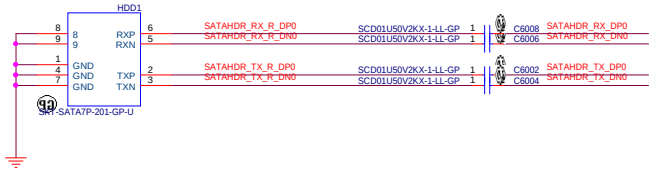
17 SATAHDR_TX_DN1
17 SATAHDR_TX_DP1
17 SATAHDR_RX_DN1
17 SATAHDR_RX_DP1

17 SATAHDR_TX_DN0
17 SATAHDR_TX_DP0
17 SATAHDR_RX_DN0
17 SATAHDR_RX_DP0



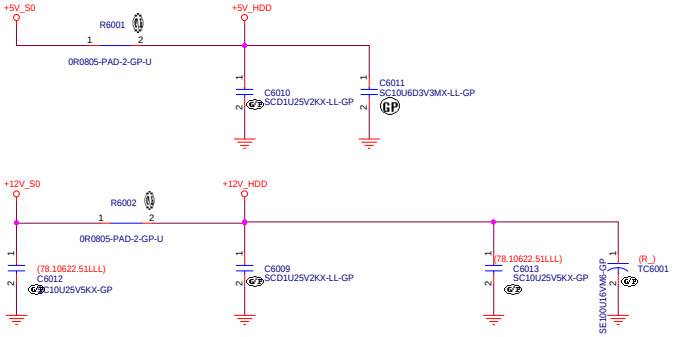
**Package PIN插 式有顛 倒 180度現象，差 分信號需要反 接 ！！
20121207 Phoran

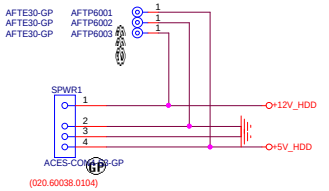




HD/OD Power CONN

Layout: Please put them together





<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDD&ODD
Size: C | Document Number: A7400 | Rev: -1B
Date: Saturday, June 18, 2016 | Sheet 60 of 107

CLINE I2C

17 CLINK_CLK_LAN
17 CLINK_DATA_LAN
17 CLINK_RST_LAN_N

PCIE WLAN

16 PCIE_TX_WLAN_N7
16 PCIE_TX_WLAN_P7
16 PCIE_RX_PCH_N7
16 PCIE_RX_PCH_P7

24,31,62 WAKE_N
24 MINI2_PCIE_RST_N

USB

16 USB_PCH_PN7
16 USB_PCH_PP7

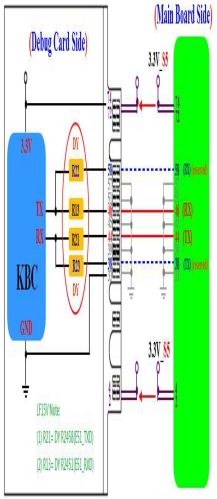
CLOCK

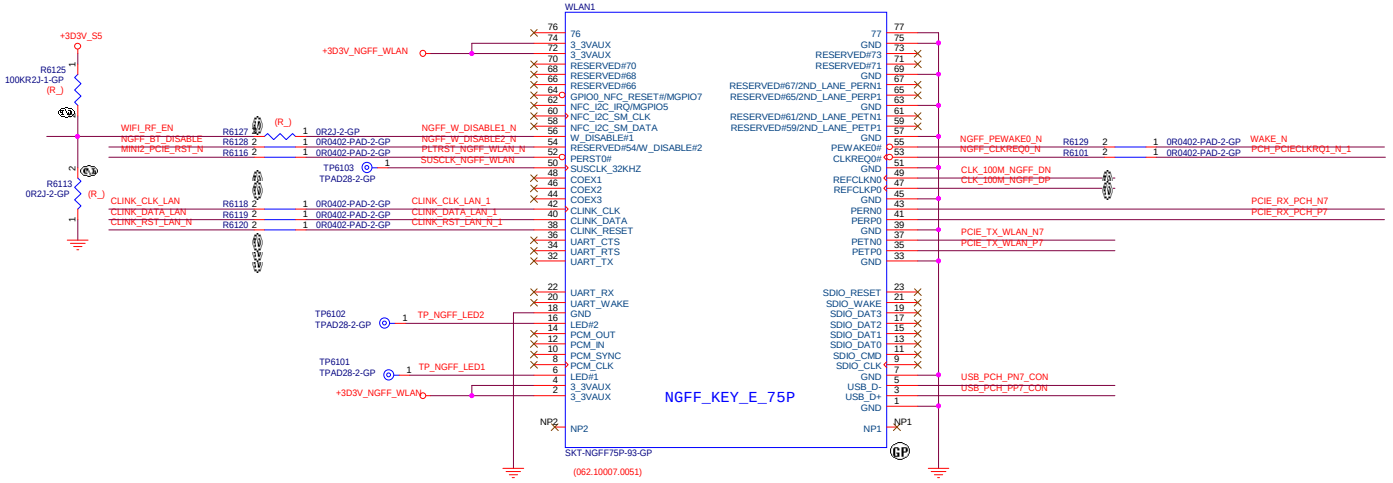
18 CLK_100M_NGFF_DN
18 CLK_100M_NGFF_DP

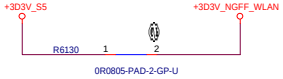
OTHER

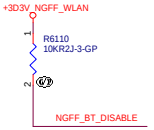
18 MINI_CLKREQ#_WLAN

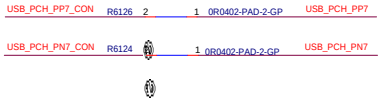
17 WIFI_RF_EN

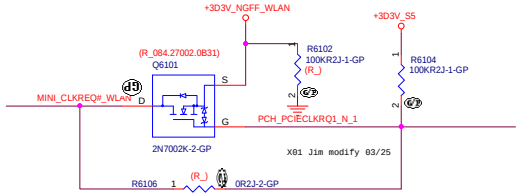


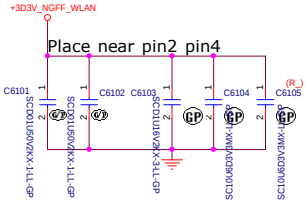


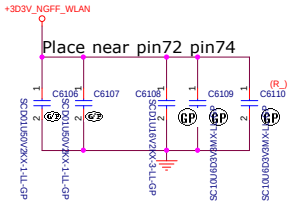












<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Mini card-WLAN

Size	Document Number	Rev
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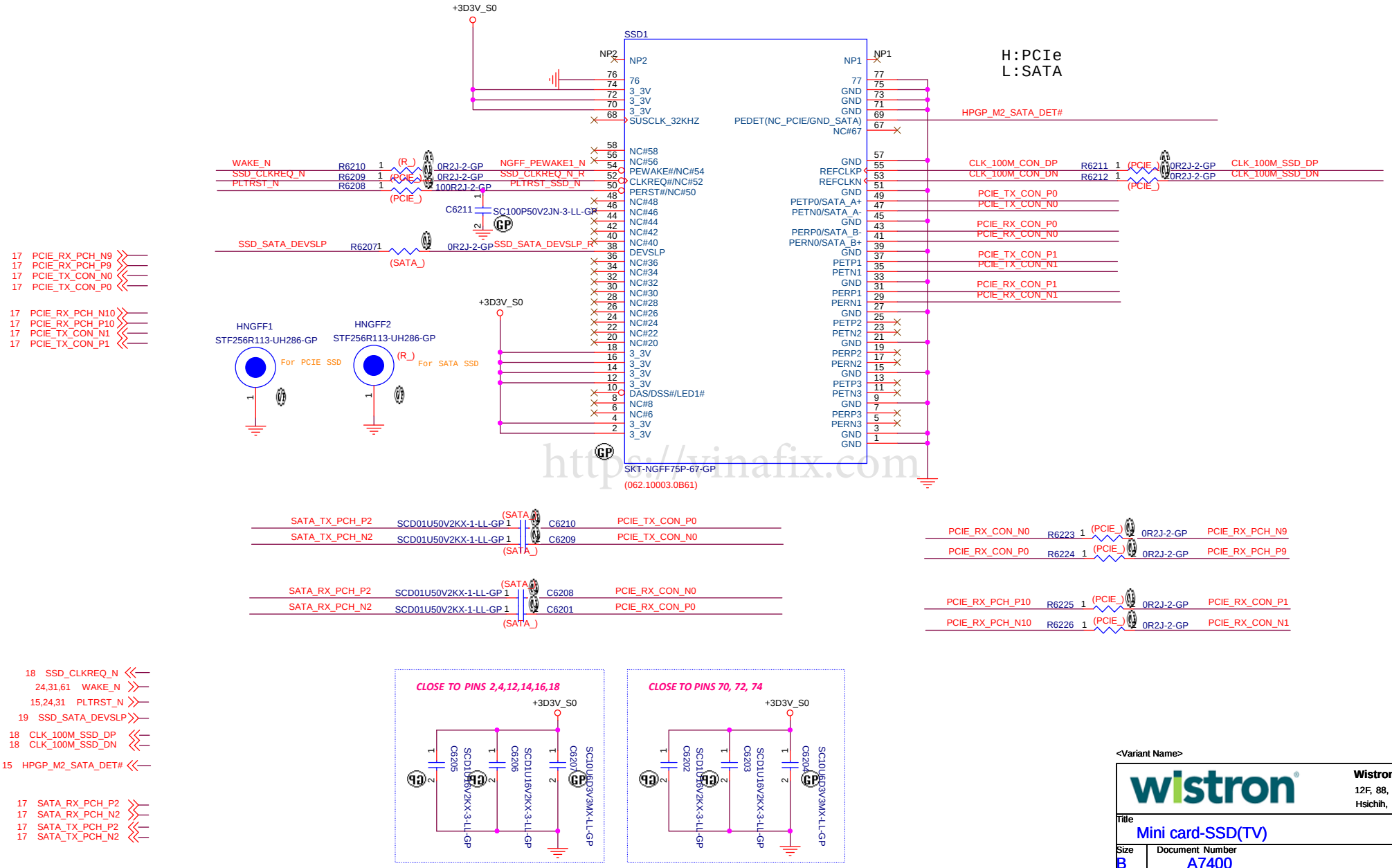
NGFF(M Key)



17 PCIE_RX_PCH_N9
17 PCIE_RX_PCH_P9
17 PCIE_TX_CON_N0
17 PCIE_TX_CON_P0

17 PCIE_RX_PCH_N10
17 PCIE_RX_PCH_P10
17 PCIE_TX_CON_N1
17 PCIE_TX_CON_P1

18 SSD_CLKREQ_N
24,31,61 WAKE_N
15,24,31 PLTRST_N
19 SSD_SATA_DEVSLP
18 CLK_100M_SSD_DP
18 CLK_100M_SSD_DN
15 HPGP_M2_SATA_DET#

17 SATA_RX_PCH_P2
17 SATA_RX_PCH_N2
17 SATA_TX_PCH_P2
17 SATA_TX_PCH_N2

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Mini card-SSD(TV)

Size: B | Document Number: A7400 | Rev: -1B

Date: Saturday, June 18, 2016 | Sheet 62 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Mini card-NGFF

Size	Document Number	Rev
C	A7400	-1B

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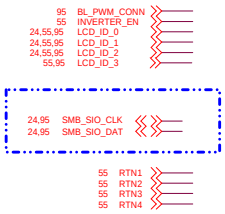

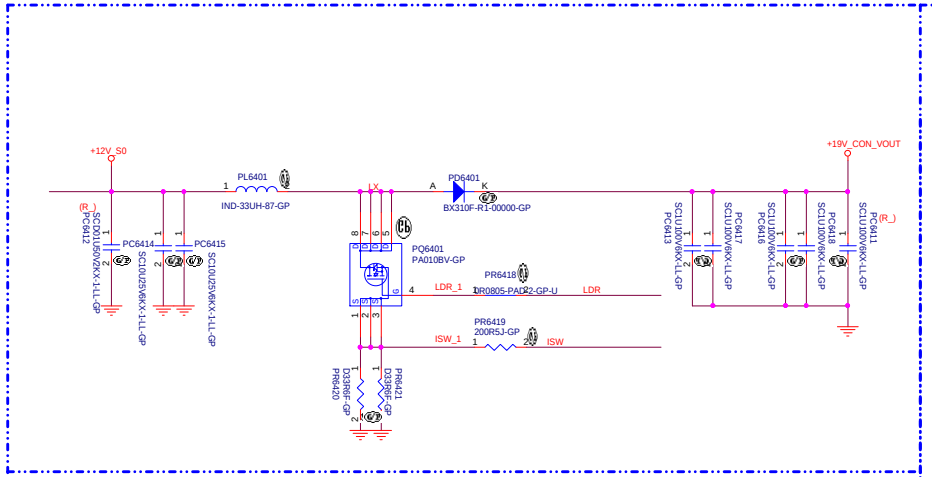

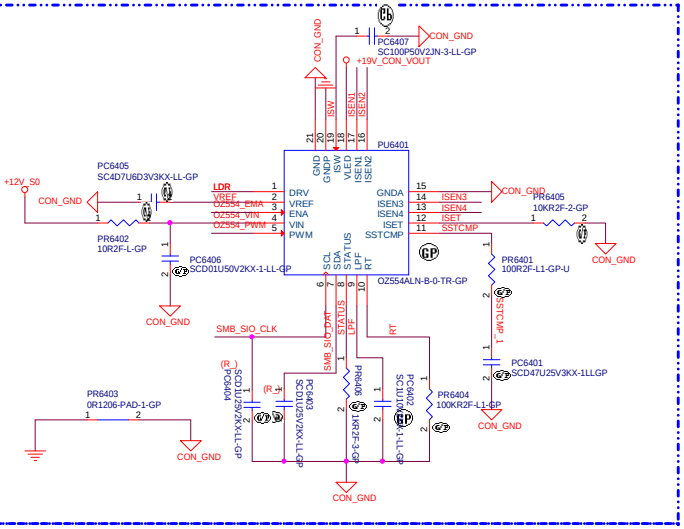

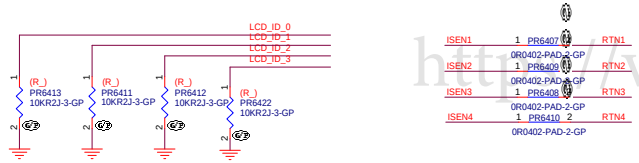

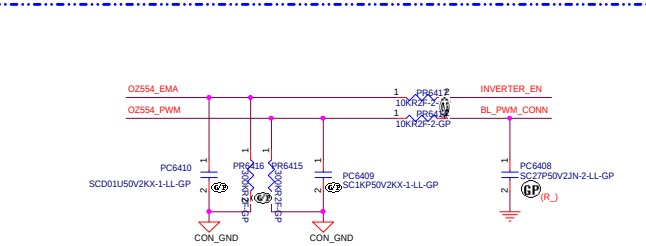

Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
	0	0	0	
	0	0	1	
	0	1	0	
	1	0	0	
	1	1	0	
	1	1	1	

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Converter board

Size	Document Number	Rev
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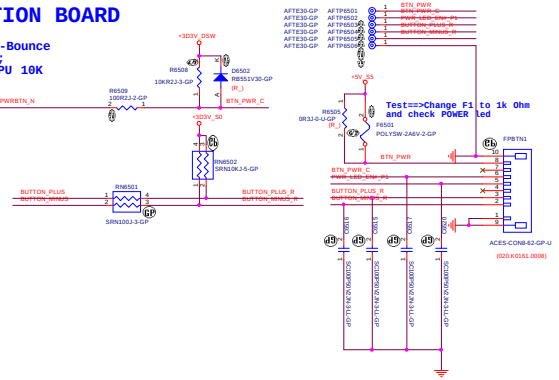
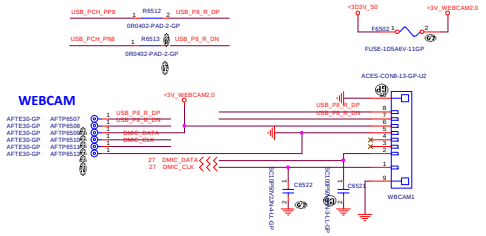
FUNCTION BOARD

ECIO: DE-Bounce function;
NO need PU 10K

Test==>Change F1 to 1k Ohm and check POWER Led



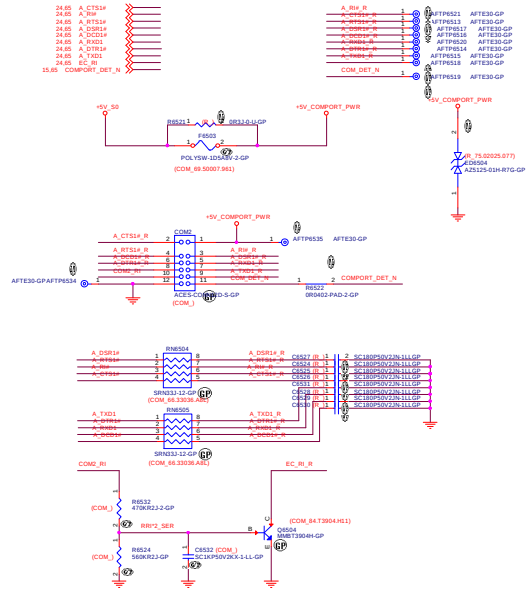
WEBCAM



5.3 LED State Control

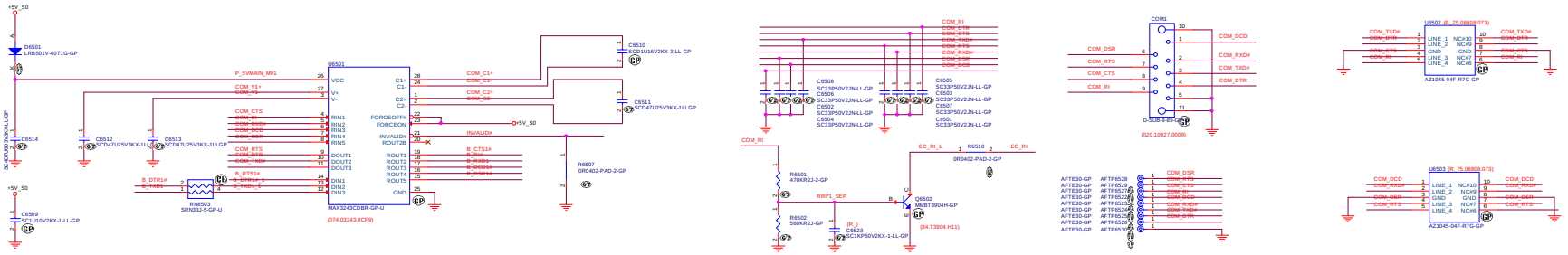
	Single Color Power LED
ACPI Status	Power LED
S0	On
S3	Blink（1HZ）
S4/S5	Off

External COM PORT



Vinafix.com

ON BOARD COM PORT



Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DP IN/OUT_(Repeater/SW)

Size	Document Number	Rev
C	A7400	-1B

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Delete Thermal header
--Young 20140920

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: THERMAL SENSOR HEAD

Size	Document Number	Rev
B	A7400	-1B

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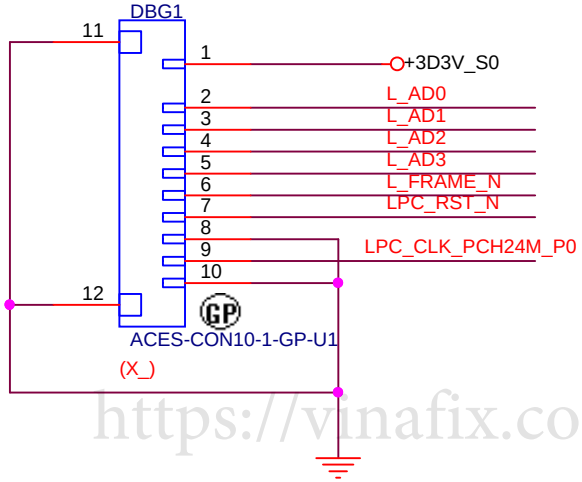
19,24 L_AD0
19,24 L_AD1
19,24 L_AD2
19,24 L_AD3
19,24 L_FRAME_N
24,91 LPC_RST_N
19 LPC_CLK_PCH24M_P0

LPC DEBUG PORT



<Variant Name>

wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: Debug_LPC		
Size: A	Document Number: A7400	Rev: -1B
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Delete circuits for 4K panel
--Young 20140920

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
4K Panel

Size	Document Number	Rev
C	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
G Sensor

Size	Document Number	Rev
B	A7400	-1B

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Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Thunderbolt_(1/5)

Size: D | Document Number: A7400 | Rev: 1B

Date: Saturday, June 16, 2018 | Sheet 71 of 107

Reserved

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Thunderbolt_(4/5)

Size	Document Number	Rev
D	A7400	1B

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Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_function (1/5)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_function (2/5)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_function (3/5)

Size	Document Number	Rev
A	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 78 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_function (4/5)

Size	Document Number	Rev
A	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 79 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_function (5/5)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU VRAM_1,2 (1/4)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU VRAM_3,4 (2/4)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU VRAM_5,6 (3/4)

Size	Document Number	Rev
A	A7400	-1B

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU VRAM_7,8 (4/4)

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU CORE_(solution)

Size	Document Number	Rev
A	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 85 of 107

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU discrete power_

Size	Document Number	Rev
A	A7400	-1B

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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU Switch_(1/2)

Size	Document Number	Rev
A	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 87 of 107

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU Switch_(2/2)

Size	Document Number	Rev
C	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 88 of 107

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU others_

Size	Document Number	Rev
C	A7400	-1B

Date: Saturday, June 18, 2016 Sheet 89 of 107

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
NFC

Size	Document Number	Rev
C	A7400	-1B

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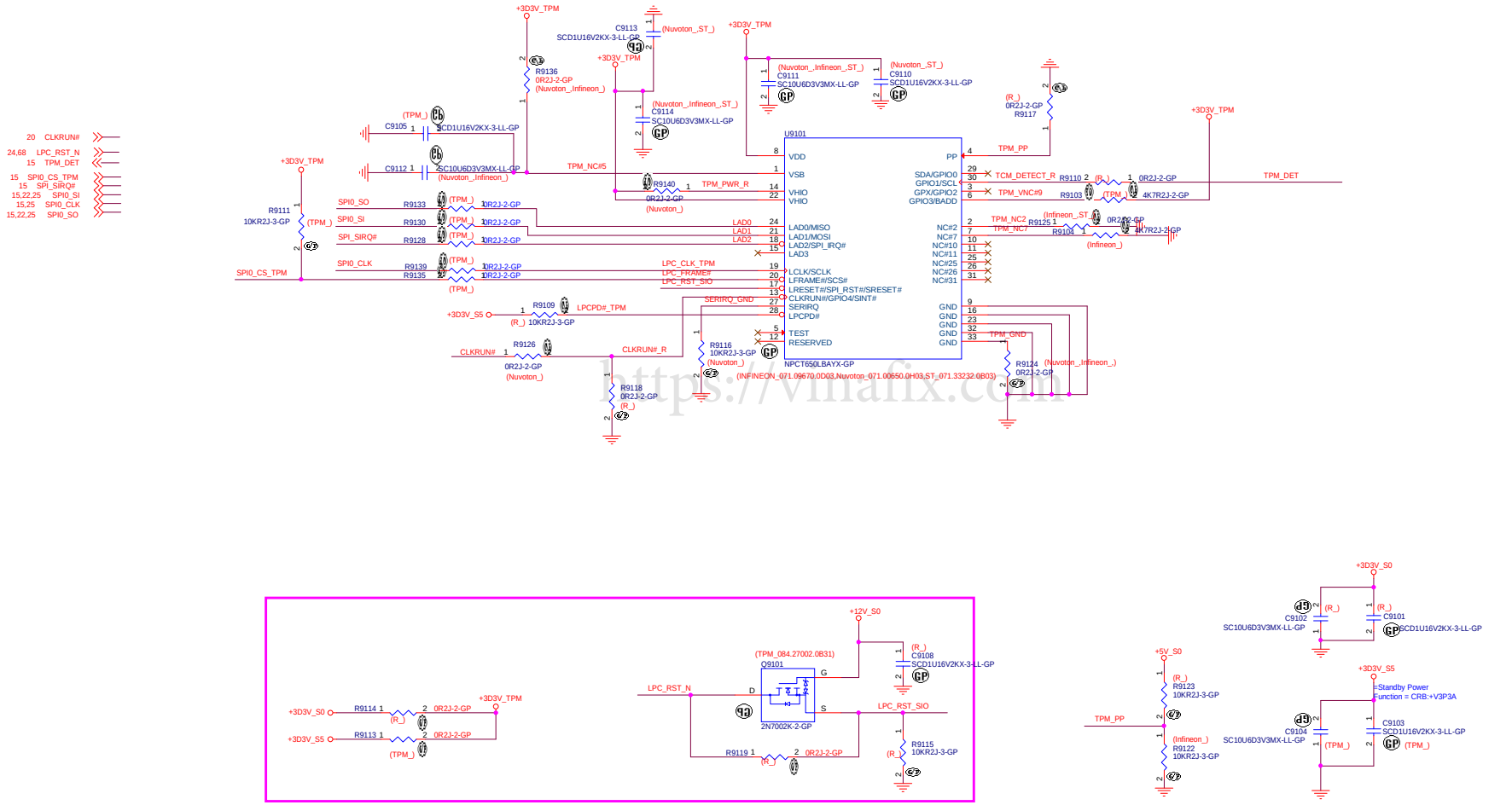
TPM PIN DEFINE



<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: TPM/Asset ID

Size	Document Number	Rev
C	A7400	-1B

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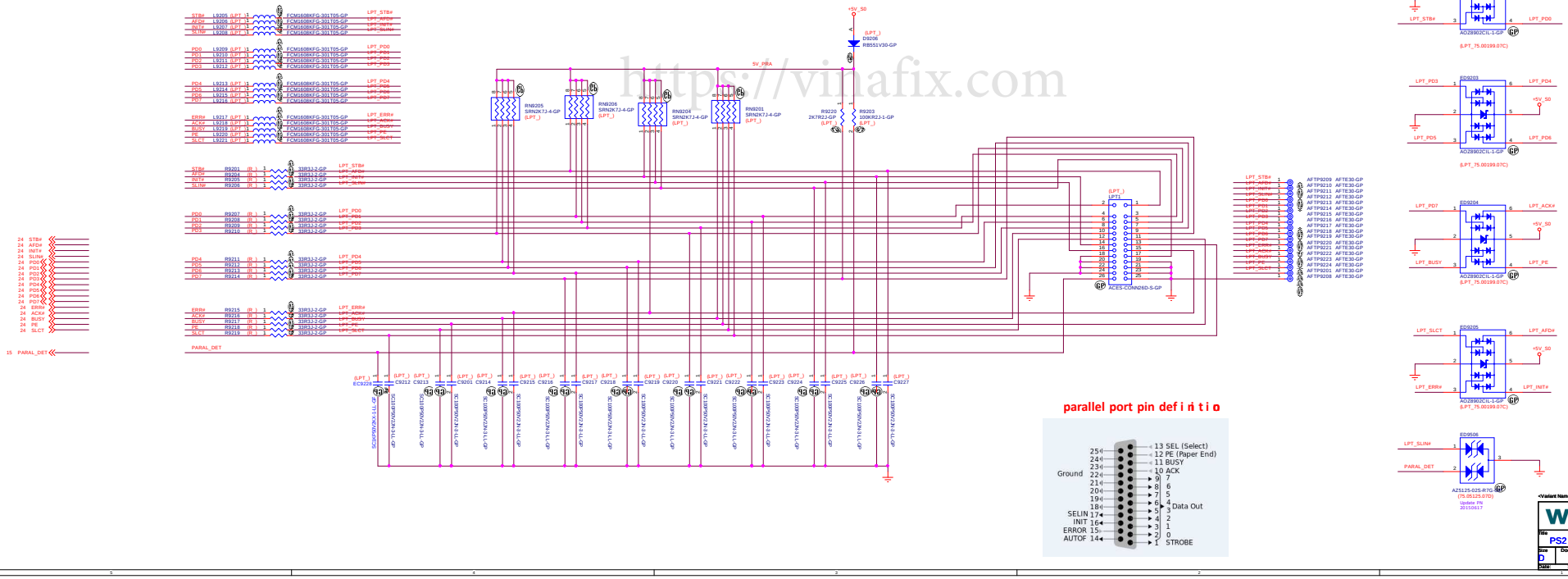
PS2 KEYBOARD& PS2 MOUSE

Parallel Port



wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PS2
Size: D | Document Number: A7400 | Rev: 1B
Date: Saturday, June 18, 2016 | Sheet 92 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Express Card		
Size: A	Document Number: A7400	Rev: -1B
Date: Saturday, June 18, 2016	Sheet 93 of 107	

Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Smart Card		
Size: A	Document Number: A7400	Rev: -1B
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SCALAR DP703(D)
PN:071.00703.000G

TRANSLATER PS8625
PN:071.08625.003

TO LVDS CONN

FROM CPU eDP

FW UPDATE BY SMBUS

SCALAR and ECIO

Panel ID

CRYSTAL

FROM PCH PORT D AUX CH- Link/Device/HPD

FROM CPU PORT D Main Link

AC Cap place near SCALAR

PCH control

SMBUS_ISP H :Simutaneous Mode
SMBUS_ISP L :Isolate Mode

Damping Register close to scaler

FLASH_CLK shielding

RTD2136 HOT PLUG
H:RTD2136 ready to take input
L: RTD2136 not ready

Mode Configure Table(Power On Latch)

PS8625_RLV_LNK
(internal PD 80K ohm)
L:Single link LVDS
H:Dual link LVDS

PS8625_RLV_CFG
L: 8-bit LVDS, VESA mapping
M: 8-bit LVDS, JEIDA mapping
H: 6-bit LVDS, both VESA and JEIDA mapping

PS8625_RLV_AMP
LVDS output swing control
Connect to a 4.99kΩ resistor to groundfor default output swing. The output swing can be adjusted by changing the resistor value.

EP Mode

ECIO

EEPROM Mode
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.
I2C address=0xA8

PS8625(T) F/W

DP703(D) OSD

wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Display Port
Size: D
Document Number: A7400
Rev: 1B
Date: Saturday, June 18, 2016
Sheet 95 of 107

Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
MCU

Size	Document Number	Rev
B	A7400	-1B

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Reserved

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Intel LAN_(solution)		
Size: A	Document Number: A7400	Rev: -1B
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Reserved

<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
LAN Switch_

Size	Document Number	Rev
B	A7400	-1B

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<Variant Name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
XDP&ITP

Size	Document Number	Rev
B	A7400	-1B

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Material part

LGA115x CPU SOCKET Symbol

Vendor:LOTES
P/N:22.78003.011

Vendor:FOXCONN
P/N:22.78006.001

Vendor: LOTES
P/N:22.78002.011
Thickness: max 2.2mm (含mylar膠厚)

Vendor: FOXCONN
P/N:22.78006.011
Thickness:2.0mm(含mylar)

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

2013/03/19 David
Removed CPU socket & back plate & cover

LABEL

MB serial NO# and MAC address
40.3KP03.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for adatlas

H2/2 Derek change to 70x8mm between CPU and DIMM

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

Stand-off

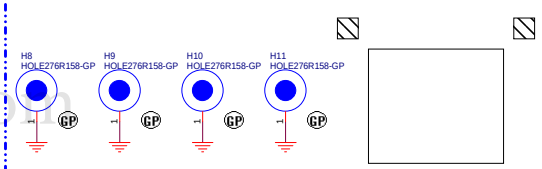
teknisi indonesia

HeatSink Symbol

2013/03/19 David
Removed HeatSink

Vendor
P/N:
60.3ET05.001
60.3ET05.011
60.3ET05.021

HOLE276R158 CPU MOUNTING HOLE-PTH



==>ZZ.00PAD.U61

Battery Symbol

BTT2
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

Combination:
U1 + SKT1 + SKT2 + SKT3

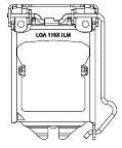
62.10055.761 (LOTES) + 22.78005.181 (LOTES)
+ 22.78002.011 (LOTES) + 22.78005.171 (LOTES)

62.10040.911 (FOXCONN) + 22.78006.001
FOXCONN) + 22.78006.011 (FOXCONN) + 22.78005.161 (FOXCONN)

Combination:
U1 + SKT1 + SKT2 + SKT3

062.10015.0081 (FOXCONN) + 22.78006.001(LOTES) + 22.78006.011 (LOTES) + 22.78005.281 (FOXCONN)

SKTF1



Load Plate
(022.70001.0101)

SKTB1

Back Plate
(22.78006.011)

SKT3

ILMCOVER
(22.78005.171)

Second source:
22.78005.281

Second source:
022.70001.0341

Foxconn : 22.78006.001
Lotes : 22.78005.181

Foxconn : 22.78006.011
Lotes : 22.78002.011
Thickness:2.6mm

Foxconn : 22.78005.161
Lotes : 22.78005.171

CPU Load Plate:
Part Number: 022.70001.0101
Vendor Part Number: PT44L51-6401

CPU Socket:
Part Number: 062.10015.0051
Vendor Part Number: 3H993827-4M41-01H

<Variant Name>

wistron

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Title: Label_RTC BATT

Size	Document Number	Rev
C	A7400	-1B

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Project Definition

Pin Name	Net Name	External Pull Up/Down	BIOS Setting: Internal Pull Up/Down	Type	SubType	if Output: S3	if Output: S5	Reset Config	Note
GPP_A0	KBRST_N KBRST_N	+3D3V_S0 <R2468(4K7R2J)> U2402@KBRST#/SPI_HOLD#/GPIO12	None	Native	Native1				
GPP_A1	LPC_AD_PCH_P0 L_AD0 L_AD0 LAD0 SPI0_SO_ROM1_R SPI0_SO_ROM1_R SPI0_SO_PCH	+3D3V_S0 <R1911(0R2J)/RN2403(SRN4K7J)> DBG1@2 <R1911(0R2J)> U2402@LAD0 <R1911(0R2J)> U9101@LAD0/MISO <R1911(0R2J)/R9133(0R2J)> SKT1@2 <R1911(0R2J)/R9133(0R2J)/R9132(0R2J)/R2508(33R2J)> U2501@DO/IO1 <R1911(0R2J)/R9133(0R2J)/R9132(0R2J)/R2508(33R2J)> PCH1@SPI0_MISO <R1911(0R2J)/R9133(0R2J)/R9132(0R2J)/R1505(0R2J)>	None	Native	Native1				
GPP_A2	LPC_AD_PCH_P1 LPC_AD_PCH_P1 L_AD1 L_AD1 LAD1 SPI0_SI_ROM1_R SPI0_SI_ROM1_R SPI0_SI_PCH	+3D3V_S0 <R1912(0R2J)/RN2403(SRN4K7J)> +3D3V_S5 <R1912(0R2J)/R9130(0R2J)/R9129(0R2J)/R2512(1KR2J)> DBG1@3 <R1912(0R2J)> U2402@LAD1 <R1912(0R2J)> U9101@LAD1/MOSI <R1912(0R2J)/R9130(0R2J)> SKT1@5 <R1912(0R2J)/R9130(0R2J)/R9129(0R2J)/R2504(33R2J)> U2501@DI/IO0 <R1912(0R2J)/R9130(0R2J)/R9129(0R2J)/R2504(33R2J)> PCH1@SPI0_MOSI <R1912(0R2J)/R9130(0R2J)/R9129(0R2J)/R1504(0R2J)>	None	Native	Native1				
GPP_A3	LPC_AD_PCH_P2 LPC_AD_PCH_P2 L_AD2 L_AD2 LAD2 SPI_SIRQ#	+3D3V_S0 <R1913(0R2J)/RN2404(SRN4K7J)> +3D3V_S5 <R1913(0R2J)/R9128(0R2J)/R9127(0R2J)/R1513(10KR2J)> DBG1@4 <R1913(0R2J)> U2402@LAD2 <R1913(0R2J)> U9101@LAD2/SPI_IRQ# <R1913(0R2J)/R9128(0R2J)> PCH1@GPP_A20/ISH_GP2 <R1913(0R2J)/R9128(0R2J)/R9127(0R2J)>	None	Native	Native1				
GPP_A4	LPC_AD_PCH_P3 L_AD3 L_AD3 LAD3	+3D3V_S0 <R1914(0R2J)/RN2404(SRN4K7J)> DBG1@5 <R1914(0R2J)> U2402@LAD3 <R1914(0R2J)> U9101@LAD3 <R1914(0R2J)/R9126(0R2J)>	None	Native	Native1				
GPP_A5	LPC_FRAME#_PCH L_FRAME_N L_FRAME_N LPC_FRAME# SPI0_CS_PCH_N1	No Power Rail DBG1@6 <R1915(0R2J)> U2402@LFRAME# <R1915(0R2J)> U9101@LFRAME#/SCS# <R1915(0R2J)/R9135(0R2J)> PCH1@SPI0_CS2# <R1915(0R2J)/R9135(0R2J)/R9134(0R2J)/R1508(0R2J)>	None	Native	Native1				
GPP_A6	SER_IRQ SER_IRQ SER_IRQ	+3D3V_S0 <R1920(10KR2J)> U9101@SERIRQ U2402@SERIRQ	None	Native	Native1				
GPP_A7	LPC_PIRQ_R L_DRQ_N	No Power Rail U2402@GPIO10/LDRQ# <R1916(0R2J)>	None	Native	Native1				
GPP_A8	CLKRUN# CLKRUN# [illegible]	+3D3V_S0 <R2039(8K2R2F)> GND <R9125(0R2J)/R9112(0R2J)> [illegible]	None	Native	Native1				
GPP_A9	CLK_PCI33M_SIO_R CK_PCH_33M_SIO	No Power Rail U2402@PCICLK <R1918(22R2F)>	None	Native	Native1				
GPP_A10	LPC_CLK_PCH24M_TPM LPC_CLK_PCH24M_P0 LPC_CLK_TPM SPI0_CLK_ROM1_R SPI0_CLK_ROM1_R SPI0_CLK_PCH	+3D3V_S5 <R9136(22R2J)/R9137(0R2J)/R2511(1KR2J)> DBG1@9 <R1919(22R2F)> U9101@LCLK/SCLK <R9136(22R2J)> SKT1@6 <R9136(22R2J)/R9137(0R2J)/R2510(33R2J)> U2501@CLK <R9136(22R2J)/R9137(0R2J)/R2510(33R2J)> PCH1@SPI0_CLK <R9136(22R2J)/R9137(0R2J)/R1507(0R2J)>	None	Native	Native1				
GPP_A11	VCCPGPPA_R	+3D3V_VCCPGPPA <R1502(10KR2F)>	None	Native	Native1				
GPP_A12	ME_CNTL	+3D3V_S5 <RN2002(SRN10KJ)>	None	Output	High				Defult Setting: High H: ME Disable L: ME Enable
GPP_A13	SUSWAR_N SUSWAR_SIO_N	No Power Rail U2402@SUSWARN#/GPIO90 <R2045(0R0402)>	None	Native	Native1				
GPP_A14	LPCPD_N LPCPD#_TPM LPCPD#_EC	+3D3V_TPM <R1917(0R2J)/R9124(0R2J)/R9106(10KR2J)> U9101@LPCPD# <R1917(0R2J)/R9124(0R2J)> U2402@TACHIN/PWMOUT/CIRWB/GPIO71 <R1917(0R2J)/R2472(0R0402)>	None	Input					
GPP_A15	SUSACK_N SUSACK_SIO_N	+3D3V_DSW <R2047(0R0402)/R2471(4K7R2J)> U2402@SUSACK#/GPIO92 <R2047(0R0402)>	None	Native	Native1				
GPP_A16	CLKOUT_48M_R CLKOUT_48M_R	No Power Rail TP_PCH_AR17@1	None	Native	Native1				
GPP_A17	CMOS_IN CMOS_IN	+3D3V_S5 <R2513(10KR2J)> CMOS1@2	None	Input					
GPP_A18	NC		None	Output	High				
GPP_A19	NC		None	Output	High				
GPP_A20	SPI_SIRQ# SPI_SIRQ# LAD2 L_AD2 L_AD2 LPC_AD_PCH_P2	+3D3V_S5 <R1513(10KR2J)> +3D3V_S0 <R9127(0R2J)/R9128(0R2J)/RN2404(SRN4K7J)> U9101@LAD2/SPI_IRQ# <R9127(0R2J)> DBG1@4 <R9127(0R2J)/R9128(0R2J)> U2402@LAD2 <R9127(0R2J)/R9128(0R2J)> PCH1@GPP_A3/LAD2/ESPI_IO2 <R9127(0R2J)/R9128(0R2J)/R1913(0R2J)>	None	Input					
GPP_A21	DOS_OS_STATUS DOS_OS_STATUS	+3D3V_S5 <R1534(10KR2J)> U2402@GPIO62/MSDA0	None	Output	Low				L: windows OS H: DOS OS
GPP_A22	NC		None	Output	High				
GPP_A23	NC		None	Output	High				
GPP_B0	GPP_B0 GPP_B0	No Power Rail TP2010@1	None	Output	High				NC
GPP_B1	GPP_B1 GPP_B1	No Power Rail TP2009@1	None	Output	High				NC
GPP_B2	VRALERTB_PU	+3D3V_S5 <RN2002(SRN10KJ)>	None	Native	Native1				
GPP_B3	BT_RF_KILL_R_N	+3D3V_S5 <R1514(10KR2J)>	None	Output	High				NC
GPP_B4	EXTTS_SNI_DRV1_PCH	+3D3V_S0 <R1522(8K2R2F)>	None	Output	High				
GPP_B5	NC		None	Output	High				
GPP_B6	GPP_B6 GPP_B6	No Power Rail TP_PCH_AW24@1	None	Output	High				NC
GPP_B7	GPP_B7 GPP_B7	No Power Rail TP_PCH_AT24@1	None	Output	High				NC
GPP_B8	NC		None	Output	High				
GPP_B9	NC		None	Output	High				
GPP_B10	NC		None	Output	High				
GPP_B11	SMBUS_ISP SMBUS_ISP SMBUS_ISP SMBUS_ISP SMBUS_ISP	+3D3V_S0 <R2026(10KR2J)> Q9502@2 Q9502@5 Q9503@2 Q9503@5	None	Output	Low				H:Not Isolate SNBUS for scalar FW update L:Isolation SMBUS for scalar FW update
GPP_B12	NC		None	Output	High				
GPP_B13	PCH_PLTRST_N LAN_RST_N PLTRST_N_EC	No Power Rail U3101@PERST# <R1512(33R2F)/R3104(0R0402)> U2402@LRESET# <R1512(33R2F)/R2439(0R0402)>	None	Native	Native1				
GPP_B14	SPKR	GND <R2711(4K7R2F)/R2712(1KR2J)>	20k pd	Native	Native1				
GPP_B15	TPM_DET TPM_DET	+3D3V_S0 <R1529(10KR2J)> GND <R1531(10KR2J)>	None	Input					H:TPM mount L:No TPM mount
GPP_B16	TCM_DET TCM_DET	+3D3V_S0 <R1530(10KR2J)> GND <R1532(10KR2J)>	None	Input					H : TCM mount L:No TCM mount
GPP_B17	NC		None	Output	High				
GPP_B18	LPSS_GSPI0_MOSI	GND <R2213(1KR2J)>	None	Output	High				
GPP_B19	RTC_DET_R_N RTC_DET_N	GND <R1524(0R0402)/R2502(6D2MR2J)> Q2501@S <R1524(0R0402)>	None	Input					High: battery installed Low: no battery
GPP_B20	NC		None	Output	High				
GPP_B21	NC		None	Output	High				
GPP_B22	LPSS_GSPI1_MOSI	GND <R2218(20KR2J)>	None	Output	High				
GPP_B23	PCH_HOT_R_N	+3D3V_S5 <R2221(150KR2F)>	None	Output	High				
GPP_C0	SMB_CLK_RESUME_R SMB_CLK_RESUME	+3D3V_S5 <R2037(0R0402)/RN2004(SRN1KJ)> Q2001@3 <R2037(0R0402)>	None	Native	Native1				
GPP_C1	SMB_DATA_RESUME_R SMB_DATA_RESUME	+3D3V_S5 <R2042(0R0402)/RN2004(SRN1KJ)> Q2001@6 <R2042(0R0402)>	None	Native	Native1				
GPP_C2	PCH_PORT80_LED	+3D3V_S5 <R2214(4K7R2J)>	None	Output	High				
GPP_C3	LAN_SMB_CLK	+3D3V_S5 <R2016(499R2F)>	None	Native	Native1				
GPP_C4	LAN_SMB_DATA	+3D3V_S5 <R2018(499R2F)>	None	Native	Native1				
GPP_C5	GPP_C_5	GND <R2220(20KR2J)>	None	Output	High				NC
GPP_C6	SML1CLK_PCH_R	+3D3V_S5 <RN2001(SRN1KJ)>	None	ME					
GPP_C7	SML1DATA_PCH_R	+3D3V_S5 <RN2001(SRN1KJ)>	None	ME					
GPP_C8	GPP_C8 GPP_C8	No Power Rail TP1505@1	None	Output	High				NC
GPP_C9	GPP_C9 GPP_C9	No Power Rail TP1504@1	None	Output	High				NC
GPP_C10	LANCLK_REQ_N	+3D3V_S5 <R1511(10KR2J)>	None	Input					
GPP_C11	NC		None	Output	High				
GPP_C12	NC		None	Output	High				
GPP_C13	NC		None	Output	High				
GPP_C14	NC		None	Output	High				
GPP_C15	CHARGER_DET CHARGER_DET	+3D3V_S0 <R1533(10KR2J)> GND <R1535(10KR2J)>	None	Input					H:Have Charger function L : No charger function
GPP_C16	GPP_C16 GPP_C16	No Power Rail TP1507@1	None	Output	High				NC
GPP_C17	GPP_C17 GPP_C17	No Power Rail TP1508@1	None	Output	High				NC
GPP_C18	GPP_C18 GPP_C18	No Power Rail TP1506@1	None	Output	High				NC
GPP_C19	GPP_C19 GPP_C19	No Power Rail TP1509@1	None	Output	High				NC
GPP_C20	NC		None	Output	High				
GPP_C21	NC		None	Input					For SCI
GPP_C22	BUTTON_MINUS BUTTON_MINUS_R BUTTON_MINUS_R	+3D3V_S0 <RN6501(SRN100J)/RN6502(SRN10KJ)> FPBTN1@2 <RN6501(SRN100J)> AFTP6505@1 <RN6501(SRN100J)>	None	Input					
GPP_C23	BUTTON_PLUS BUTTON_PLUS_R BUTTON_PLUS_R	+3D3V_S0 <RN6501(SRN100J)/RN6502(SRN10KJ)> FPBTN1@3 <RN6501(SRN100J)> AFTP6504@1 <RN6501(SRN100J)>	None	Input					
GPP_D0	NC		None	Output	High				
GPP_D1	NC		None	Output	High				
GPP_D2	NC		None	Output	High				
GPP_D3	NC		None	Output	High				
GPP_D4	NC		None	Output	High				
GPP_D5	NC		None	Output	High				
GPP_D6	NC		None	Output	High				
GPP_D7	NC		None	Output	High				
GPP_D8	NC		None	Output	High				
GPP_D9	BOARD_ID_1	GND <R1635(10KR2J)>	None	Input					
GPP_D10	BOARD_ID_2	GND <R1634(10KR2J)>	None	Input					
GPP_D11	NC		None	Output	High				
GPP_D12	NC		None	Output	High				
GPP_D13	PARAL_DET PARAL_DET PARAL_DET PARAL_DET	+3D3V_S0 <RN1501(SRN10KJ)> 5V_PRA <R9203(100KR2J)> ED9506@2 PRT1@25	None	Input					
GPP_D14	COMPORT_DET_N COM_DET_N COM_DET_N	+3D3V_S0 <RN1501(SRN10KJ)> COM2@11 <R6522(0R0402)> AFTP6519@1 <R6522(0R0402)>	None	Input					
GPP_D15	NC		None	Output	High				
GPP_D16	NC		None	Output	High				
GPP_D17	NC		None	Output	High				
GPP_D18	NC		None	Output	High				
GPP_D19	NC		None	Output	High				
GPP_D20	NC		None	Output	High				
GPP_D21	NC		None	Output	High				
GPP_D22	NC		None	Output	High				
GPP_D23	NC		None	Output	High				
GPP_E0	PCH_GPP_E0 PCH_GPP_E0	No Power Rail TP1703@1	None	Output	High				NC
GPP_E1	NC		None	Output	High				
GPP_E2	PCH_GPP_E2 PCH_GPP_E2	No Power Rail TP1705@1	None	Output	High				NC
GPP_E3	EXTTS_SNI_DRV0_PCH	+3D3V_S0 <R1525(8K2R2F)>	None	Output	High				
GPP_E4	NC		None	Output	High				
GPP_E5	NC		None	Output	High				
GPP_E6	NC		None	Native	Native1				SSD_SATA_DEVSLP
GPP_E7	NC		None	Output	High				
GPP_E8	NC		None	Output	High				
GPP_E9	USB_OC0_R_N USB_OC0_R_N	+3D3V_S5 <RN1602(SRN10KJ)> U3801@OC#	None	Native	Native1				For side USB3.0
GPP_E10	USB_OC1_R_N USB_OC1_R_N	+3D3V_S5 <RN1602(SRN10KJ)> U3601@OC#	None	Native	Native1				For Rear USB3.0
GPP_E11	USB_OC2_R_N USB_OC2_R_N	+3D3V_S5 <R1643(10KR2F)> U3901@OC#	None	Native	Native1				For rear USB2.0
GPP_E12	NC		None	Output	High				VISACH2_D3
GPP_F0	NC		None	Output	High				
GPP_F1	NC		None	Output	High				
GPP_F2	NC		None	Output	High				
GPP_F3	PCH_GPP_F3 PCH_GPP_F3	No Power Rail TP1709@1	None	Output	High				NC
GPP_F4	PCH_GPP_F4 PCH_GPP_F4	No Power Rail TP1710@1	None	Output	High				NC
GPP_F5	NC		None	Output	High				
GPP_F6	NC		None	Output	High				
GPP_F7	NC		None	Output	High				
GPP_F8	NC		None	Output	High				
GPP_F9	NC		None	Output	High				
GPP_F10	NC		None	Output	High				
GPP_F11	NC		None	Output	High				
GPP_F12	NC		None	Output	High				
GPP_F13	NC		None	Output	High				
GPP_F14	H_SKTOCC_N H_SKTOCC_N H_SKTOCC_N	No Power Rail CPU1@SKTOCC# TP414@1	None	Input					H: CPU not installed L: CPU installed
GPP_F15	USB2_OC4_R_N USB_CHARGE_OC_N	+3D3V_S5 <RN1603(SRN10KJ)> U2402@GPIO95/BKFD_CUT <R1646(0R2J)>	None	Native	Native1				For chager OC
GPP_F16	USB2_OC5_R_N	+3D3V_S5 <RN1603(SRN10KJ)>	None	Output	High				Not used
GPP_F17	NC		None	Output	High				
GPP_F17	NC		None	Output	High				
GPP_F18	NC		None	Output	High				
GPP_F19	EDP_VDDEN EDP_VDDEN	No Power Rail TP1702@1	None	Output	High				NC
GPP_F20	EDP_BKLTEN_PCH		None	Native	Native1				
GPP_F21	EDP_BKLTCTL EDP_BKLTCTL EDP_BKLTCTL	No Power Rail U9602@PWMI U9601@GPIO22/PWMI	None	Native	Native1				
GPP_F22	NC		None	Output	High				
GPP_F23	MISC_ID_2	GND <R1633(10KR2J)>	None	Input					
GPP_G0	NC		None	Output	High				
GPP_G1	NC		None	Output	High				
GPP_G2	NC		None	Output	High				
GPP_G3	NC	GND <R2442(0R0402)/R2427(1KR2J)> U2402@GPIO05/CIRTX1/AMDPWR_EN <R2442(0R0402)>	None	Output	High				NC
GPP_G4	NC		None	Output	High				
GPP_G5	NC		None	Output	High				
GPP_G6	NC		None	Output	High				
GPP_G7	NC		None	Output	High				
GPP_G8	NC		None	Output	High				
GPP_G9	NC		None	Output	High				
GPP_G10	NC		None	Output	High				
GPP_G11	NC		None	Output	High				
GPP_G12	NC		None	Output	High				
GPP_G13	NC		None	Output	High				
GPP_G14	NC		None	Output	High				
GPP_G15	NC		None	Output	High				
GPP_G16	NC		None	Output	High				
GPP_G17	NC		None	Output	High				
GPP_G18	NC		None	Output	High				
GPP_G19	IO_SMI_N IO_SMI_N	+3D3V_S0 <R2412(4K7R2J)> U2402@SMI#/OVT#/GPIO85	None	Output	High				NC
GPP_G20	MISC_ID_0	GND <R1639(10KR2J)>	None	Input					
GPP_G21	BOARD_ID_0	GND <R1626(10KR2J)>	None	Input					
GPP_G22	NC		None	Output	High				
GPP_G23	NC		None	Output	High				
GPP_H0	NC		None	Output	High				
GPP_H1	NC		None	Native	Native1				SSD_CLKREQ_N
GPP_H2	NC		None	Output	High				
GPP_H3	NC		None	Output	High				
GPP_H4	NC		None	Output	High				
GPP_H5	NC		None	Output	High				
GPP_H6	NC		None	Output	High				
GPP_H7	NC		None	Output	High				
GPP_H8	NC		None	Output	High				
GPP_H9	NC		None	Output	High				
GPP_H10	NC		None	Output	High				
GPP_H11	NC		None	Output	High				
GPP_H12	NC		None	Output	High				
GPP_H13	NC		None	Output	High				
GPP_H14	NC		None	Output	High				
GPP_H15	NC		None	Output	High				
GPP_H17	NC		None	Output	High				
GPP_H18	NC		None	Output	High				
GPP_H19	NC		None	Input					
GPP_H20	NC		None	Output	High				
GPP_H21	NC		None	Output	High				
GPP_H22	NC		None	Output	High				
GPP_H23	MISC_ID_1	GND <R1627(10KR2J)>	None	Input					
GPP_I0	HDMI_DET_CPU HDMI_DET_CPU	+3D3V_S0 <R5615(1MR2J)> Q5601@S	None	Native	Native1				
GPP_I1	NC		None	Output	High				
GPP_I2	NC		None	Output	High				
GPP_I3	NC		None	Output	High				
GPP_I4	EDP_HPD_CPU EDP_HPD_CPU	No Power Rail Q9601@S	None	Native	Native1				
GPP_I5	HDMI_CTRL_CLK_PCH HDMI_CTRL_CLK_PCH	+3D3V_S0 <RN1601(SRN2K2J)> Q5602@4	None	Native	Native1				
GPP_I6	HDMI_CTRL_DATA_PCH HDMI_CTRL_DATA_PCH	+3D3V_S0 <RN1601(SRN2K2J)> Q5602@1	None	Native	Native1				
GPP_I7	NC		None	Output	High				
GPP_I8	DDPC_CTRLDATA_PCH	GND <R1641(2K2R2J)>	None	Output	High				
GPP_I9	NC		None	Output	High				
GPP_I10	DDPD_CTRLDATA_PCH	GND <R1640(2K2R2J)>	None	Output	High				
GPD0	BATLOW_N	+3D3V_DSW <R2032(10KR2J)>	None	Native	Native1				
GPD1	WP_PRO	+3D3V_DSW <R2065(10KR2J)>	None	Output	High				
GPD2	LANWAKE_SMC_WAKE_SCI_N	+3D3V_DSW <R2034(4K7R2J)>	None	Output	High				
GPD3	SW_ON_N SW_ON_N	+3D3V_DSW <R2410(1KR2J)> U2402@PSOUT#/GPEN03	None	Native	Native1				
GPD4	SLP_S3_N SLP_S3_N SLP_S3_N PWRGD_3V_Q119_2 SLP_S3_N_XSTR_G1 PWR_S0_EN PWR_S0_EN	No Power Rail Q4011@5 U2402@SLP_S3#/GPEN01 Q4004@2 <R4058(4K7R2J)> Q4007@2 <R4020(10KR2J)> PU4201@EN1 <PR4201(0R2J)> PU4201@EN2 <PR4201(0R2J)>	None	Native	Native1				
GPD5	SLP_S4_N SLP_S4_N SLP_S4_N SLP_S4_N SLP_S4_N SLP_S4_N SLP_S4_N SLP_S4_N SE_BJT_B1 1V_VCCST_EN	No Power Rail Q4014@5 U4007@A U3801@EN U2001@B U2402@SLP_S5#/GPEN05 U3601@EN U3901@EN Q4016@2 <R4079(10KR2J)> U801@EN <R802(0R0402)>	None	Native	Native1				
GPD6	PCH_LAN_PWR_EN PCH_LAN_PWR_EN	No Power Rail TP2005@1	None	Native	Native1				
GPD7	TP_PCH_BD14 TP_PCH_BD14	No Power Rail TP_PCH_BD14@1	None	Output	High				
GPD8	NC		None	Output	High				
GPD9	NC		None	Output	High				
GPD10	SLP_S5_N SLP_S5_N	No Power Rail TP2006@1	None	Native	Native1				
GPD11	LAN_DISABLE_N LAN_DISABLE_N	No Power Rail TP2007@1	None	Output	High				

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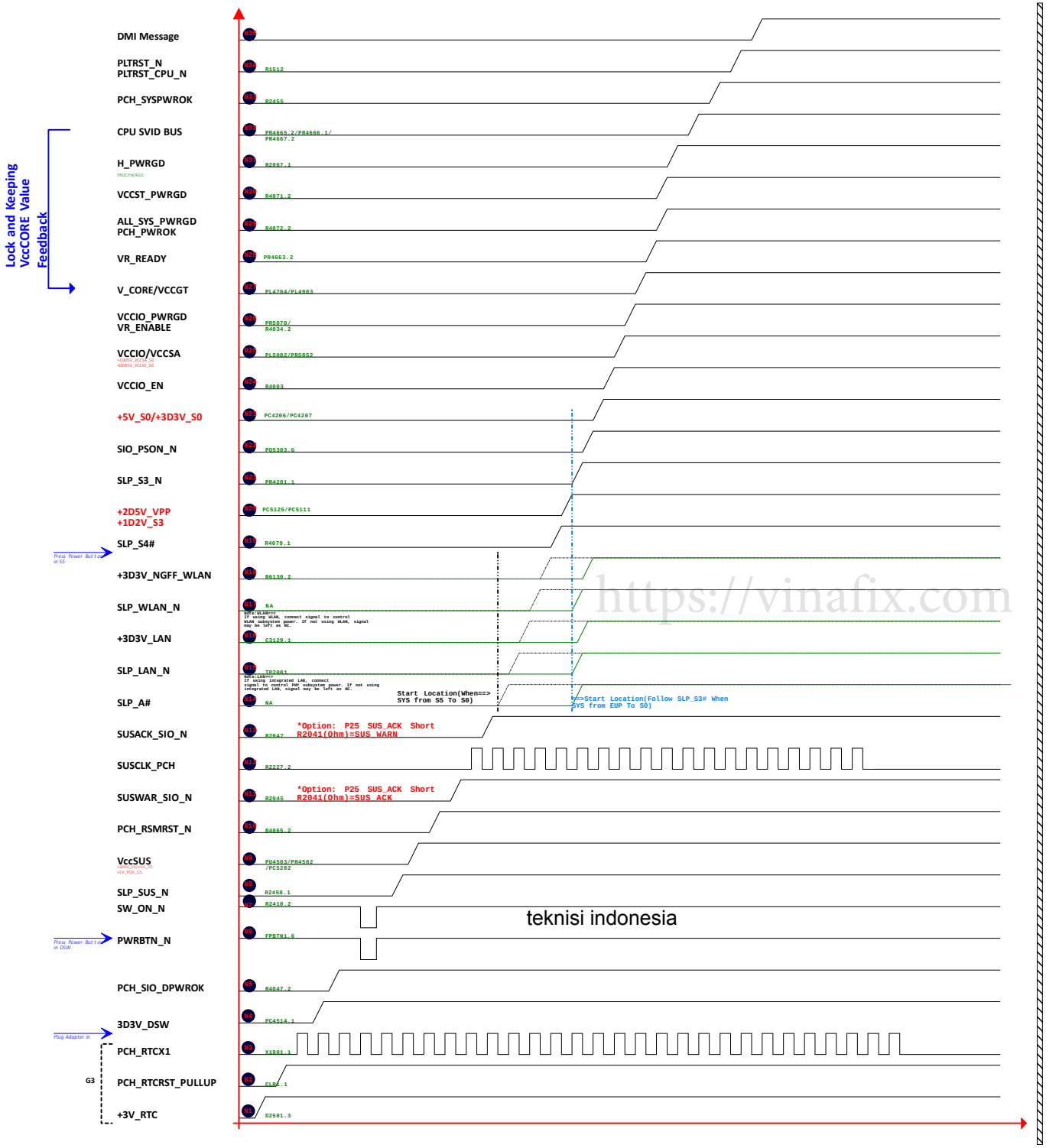

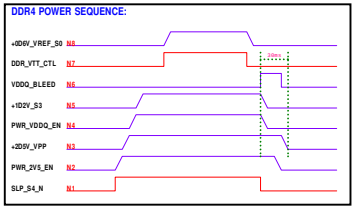

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Custom A7400 1B
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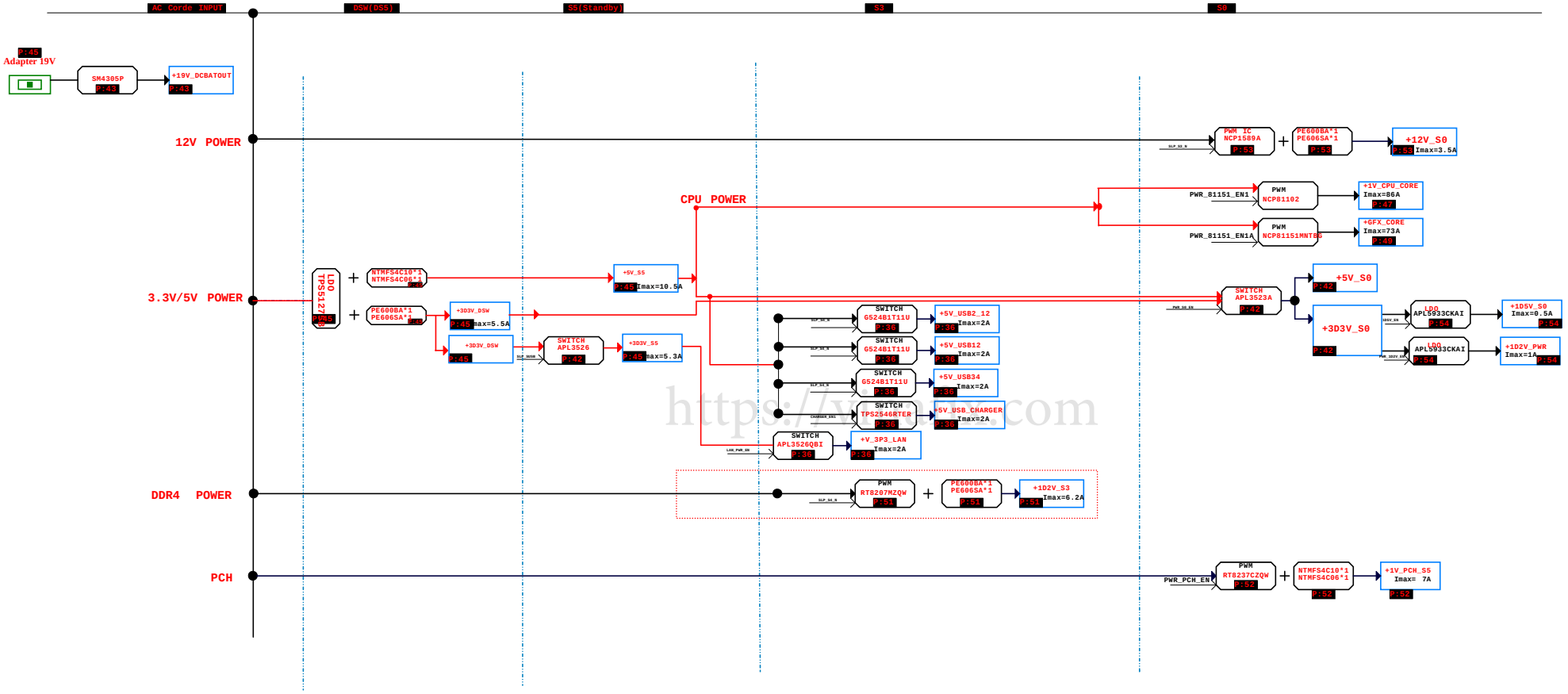

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A7400
Rev
1B
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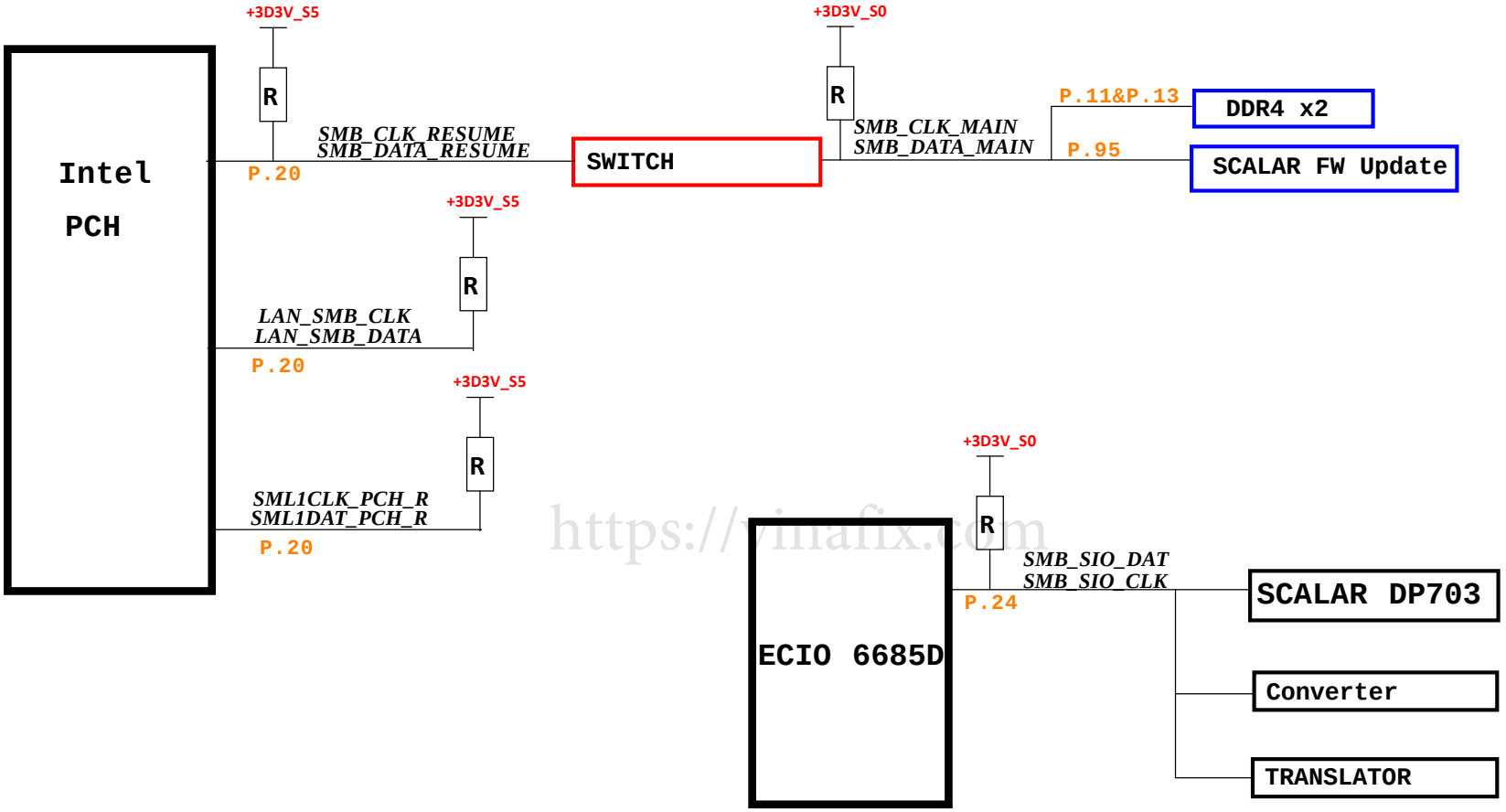

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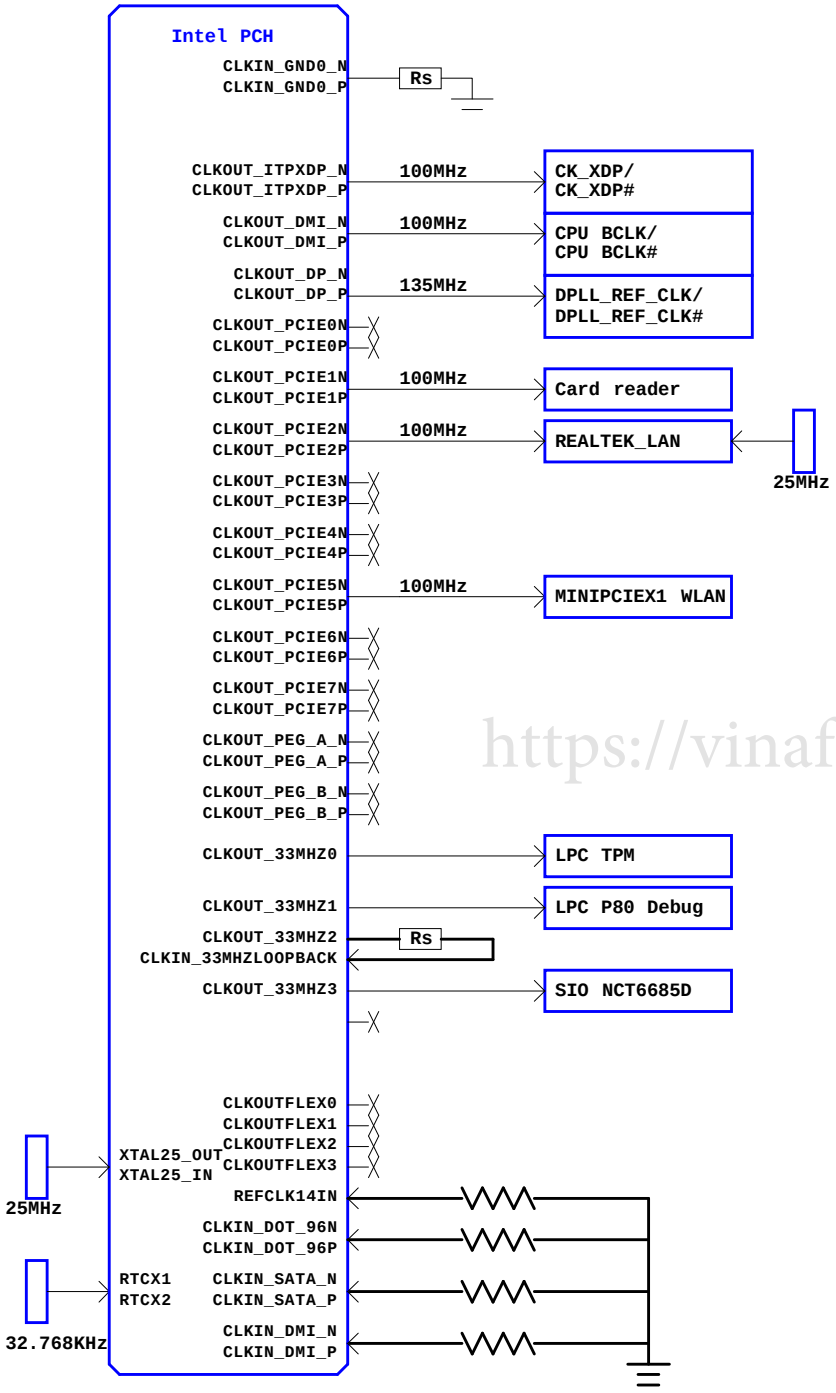

Note: .... is Reserve

Note: Rs is series resister

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Title: Clock MAP

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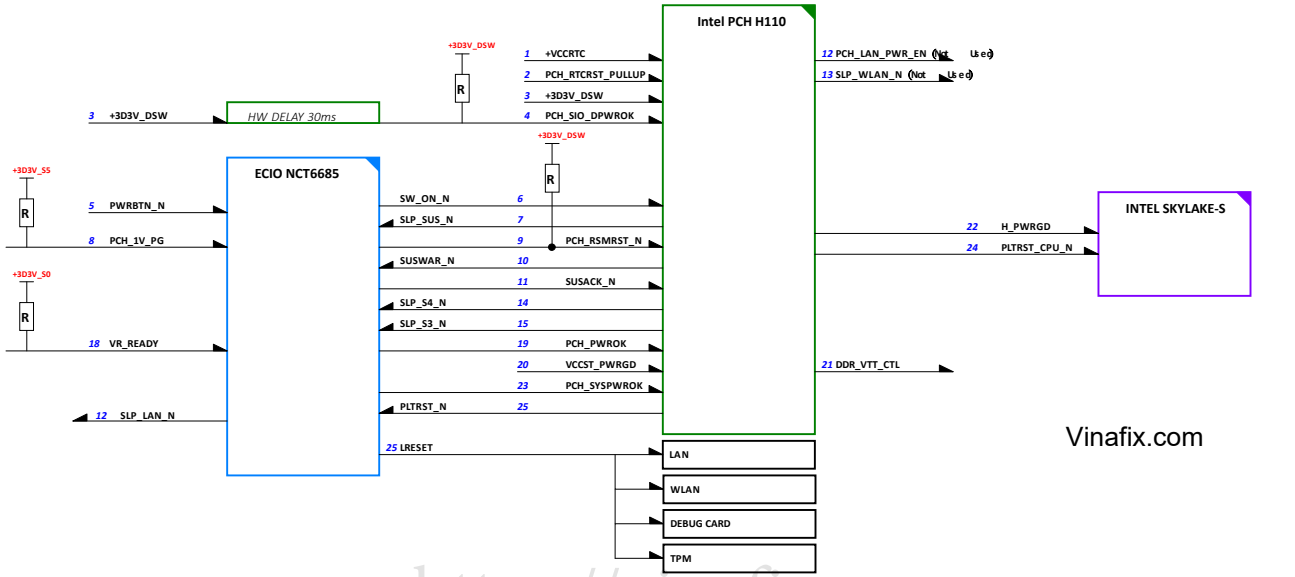

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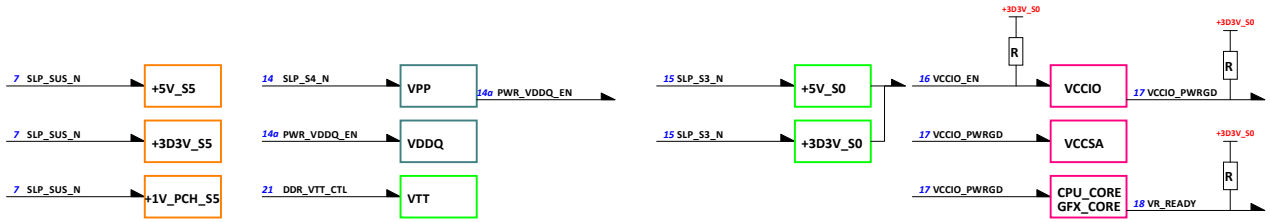

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Title: RESET Flow Chart

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