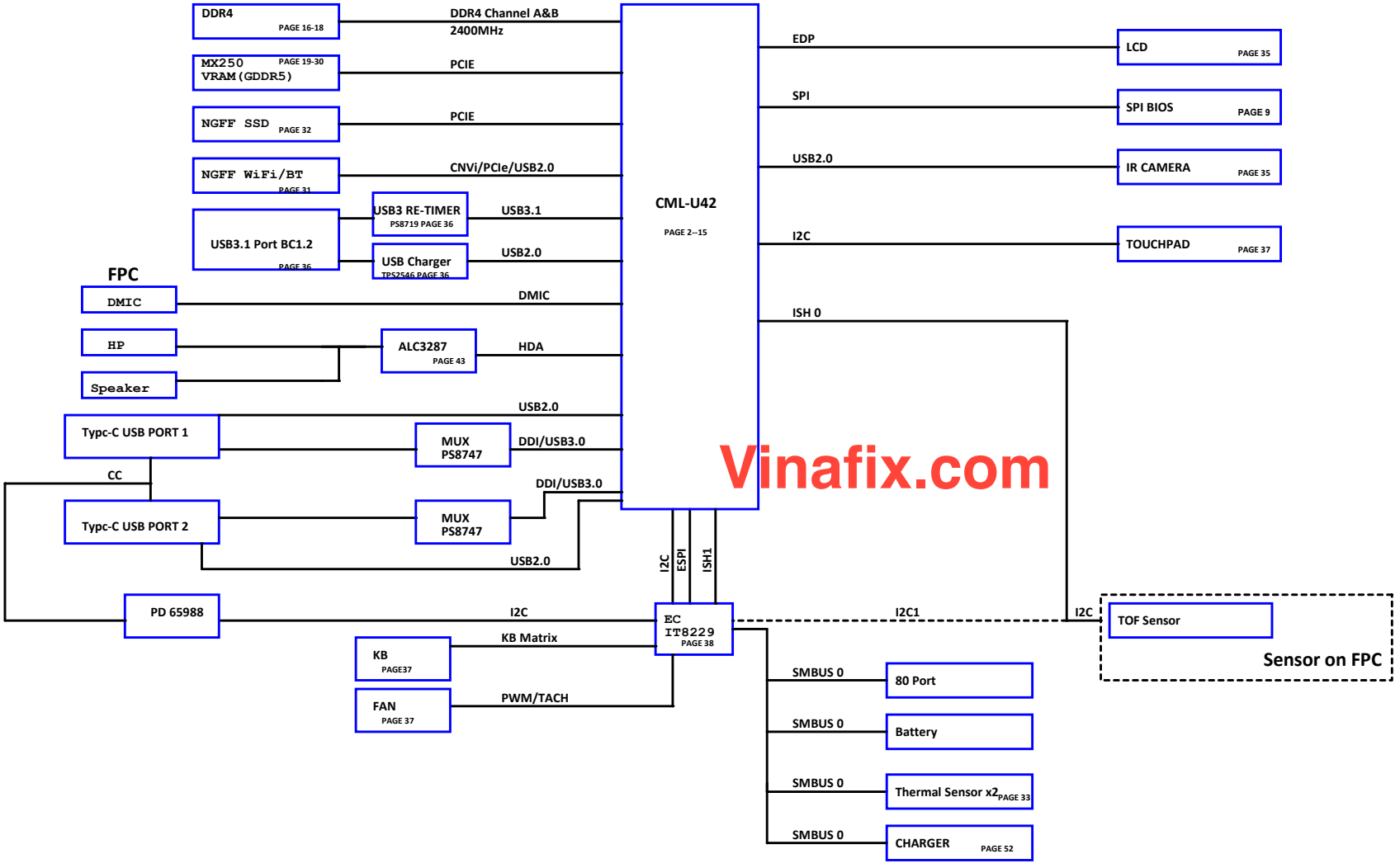
S540-13 CML-U42/v1 Schematic Block Diagram

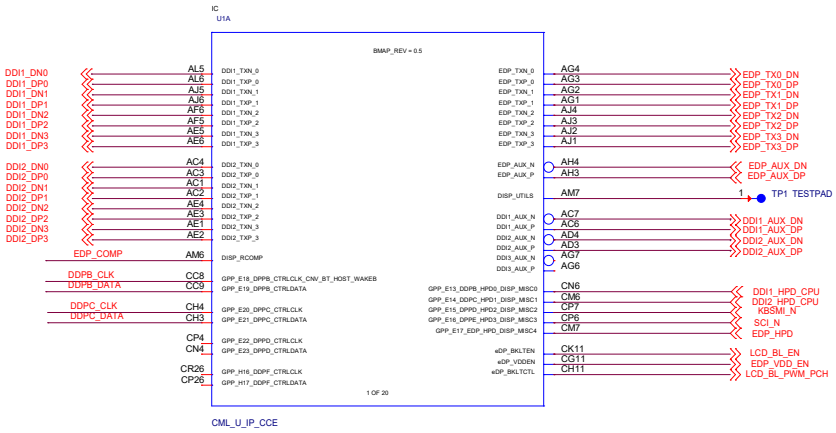


lenovo 联想 LENOVO.CRDN

Title: CML Block Diagram

Size: C | Document Number: S540-13 | Rev: V0.5

Date: Monday, June 17, 2019 | Sheet 1 of 63



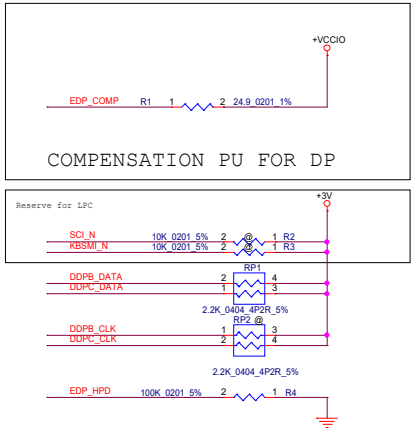


Table 53. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

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Title: CML MCP (DDI,EDP)

Size: C | Document Number: S540-13 | Rev V0.5

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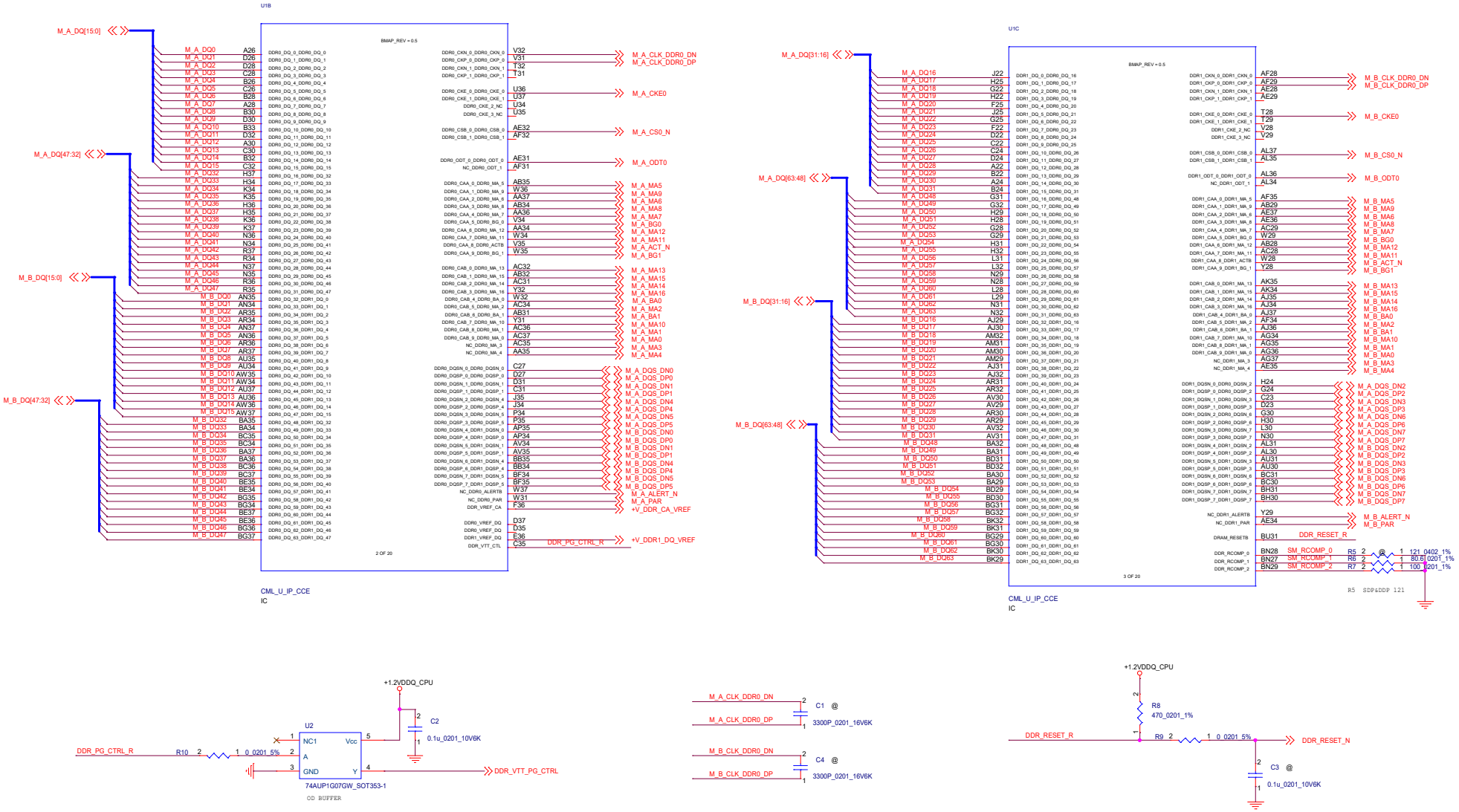

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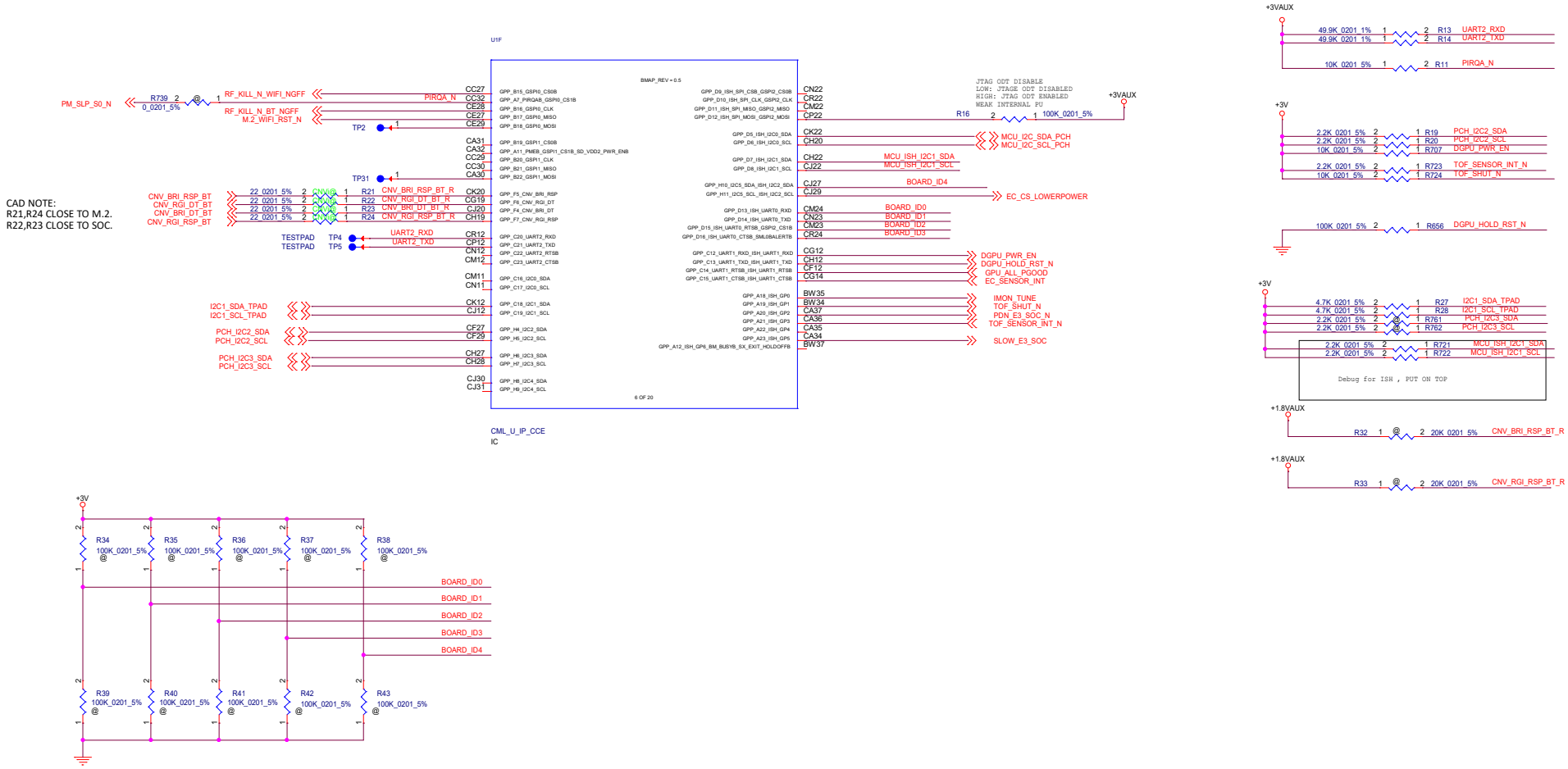
lenovo联想	LENOVO.CRDN		
Title: CML MCP (PROCESSOR DDR4)			
Size: C	Document Number: S540-13	Rev: V0.5	
Date: Monday, June 17, 2019	Sheet 3 of 63		



lenovo联想 LENOVO.CRDN

Title: CML MCP (PCH GPIO)

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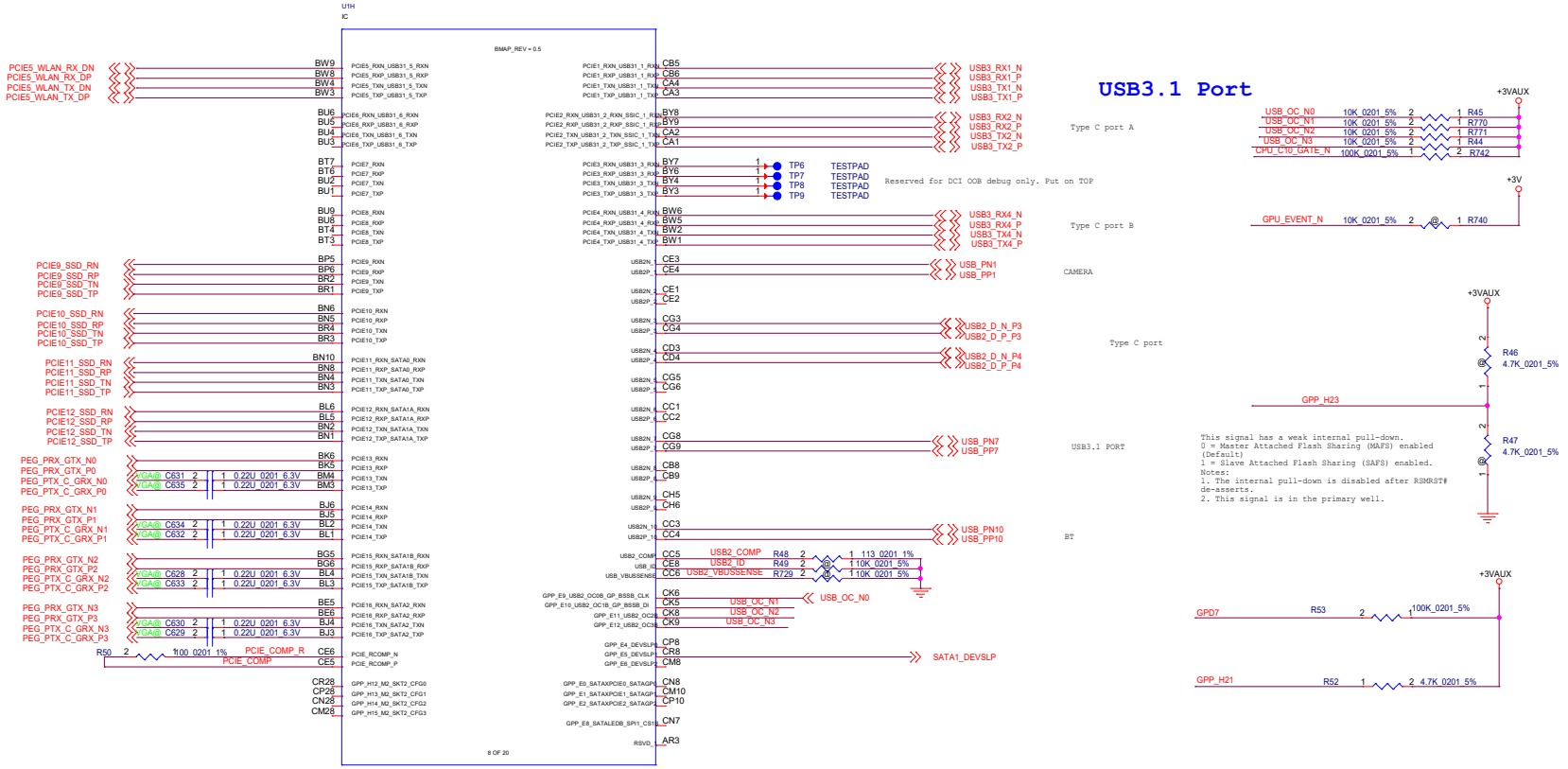
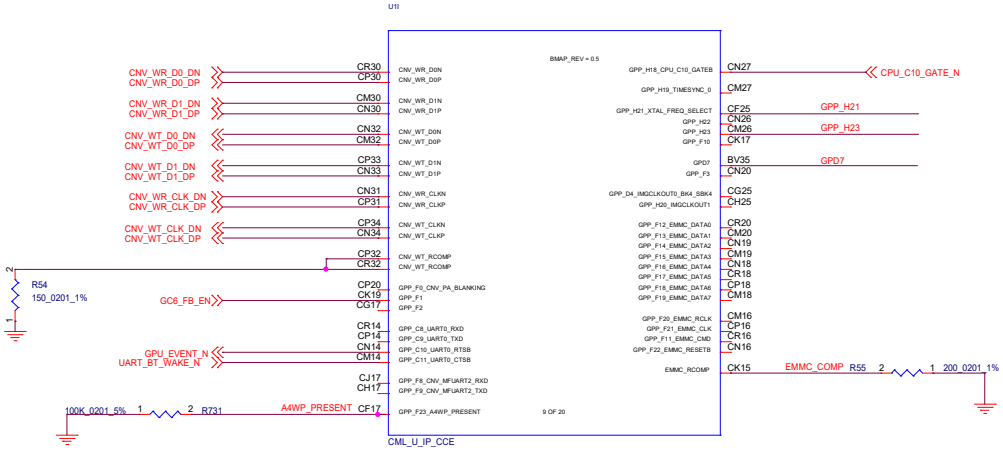
Wlan

PCIE Port 9-Port 11 SSD

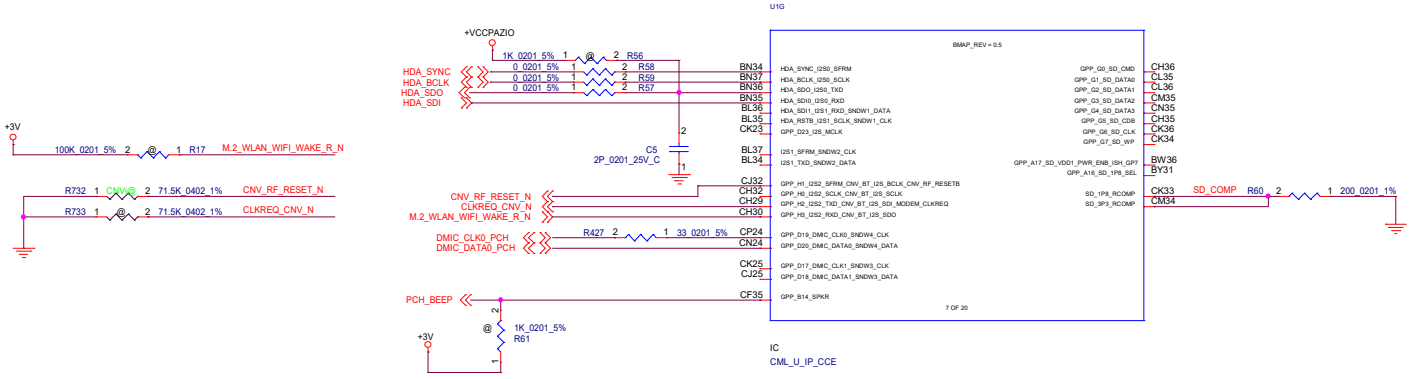
PCIE Port 13-Port 16 GPU

USB3.1 Port





lenovo联想	LENOVO.CRDN		
Title: CML MCP (PCIE USB CNVI EMMC)			
Size: C	Document Number: S540-13		Rev: V0.5
Date: Monday, June 17, 2019	Sheet 5 of 63		



lenovo联想	LENOVO.CRDN	
Title: CML MCP (HDA/I2S/SDIO/DMIC)		
Size: C	Document Number: S540-13	Rev: V0.5
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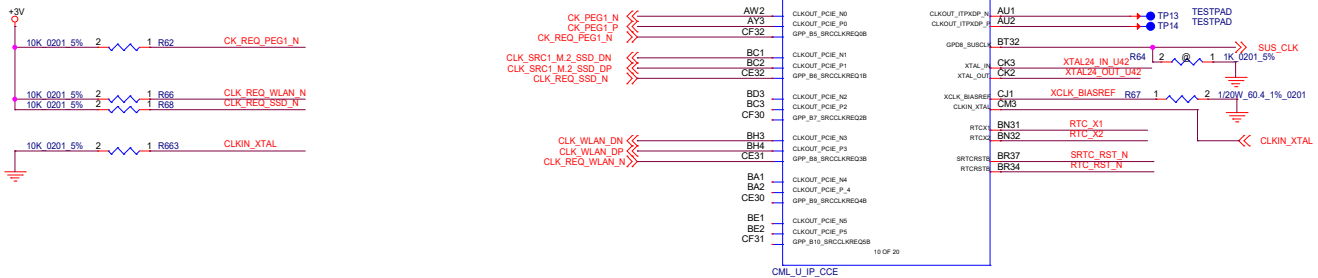
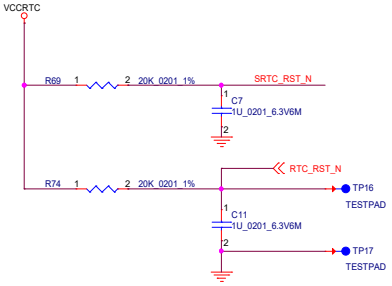
Any un-used SRCCLKRQ# signal not mapped to a Down Device or Connector/ADD-in Card must be disabled using the Kaby Lake Platform FITC tool and they must be left as no connects at the CPU side on the platform

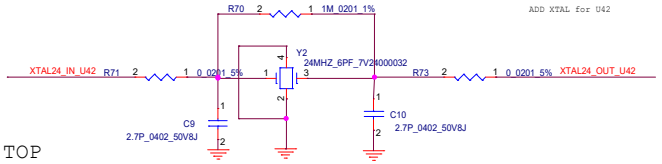


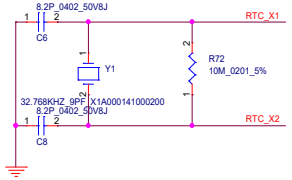


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP16 TP17 Need to put on the TOP





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Title: CML MCP (CLK)

Size: C | Document Number: S540-13 | Rev: V0.5

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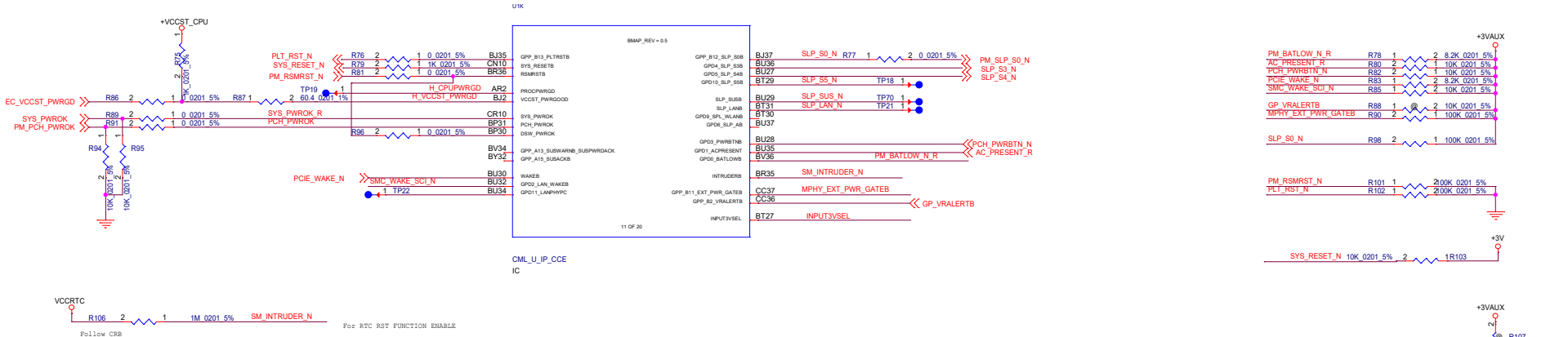
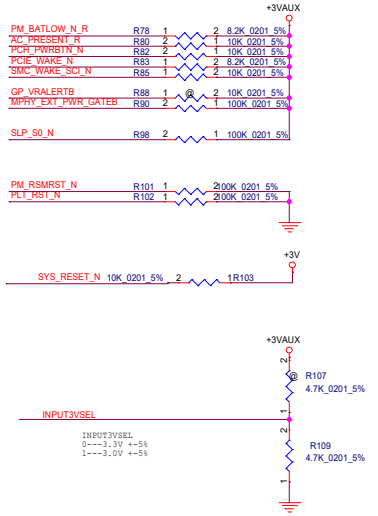


CML_U_IP_CCE

IC



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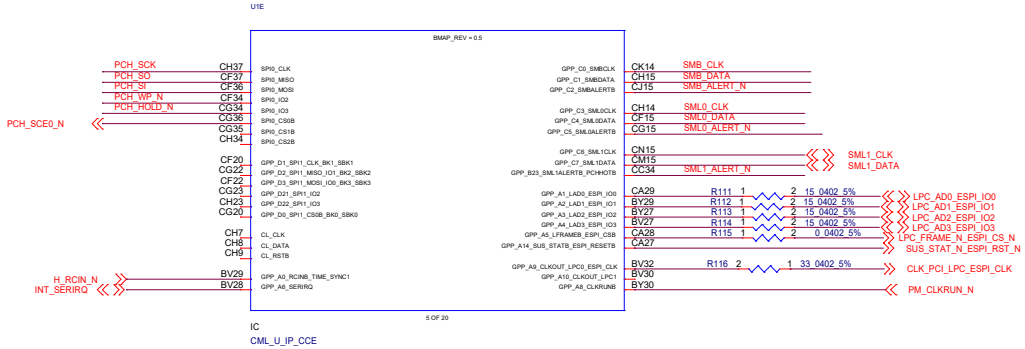
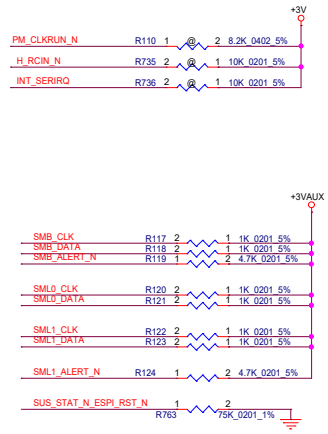
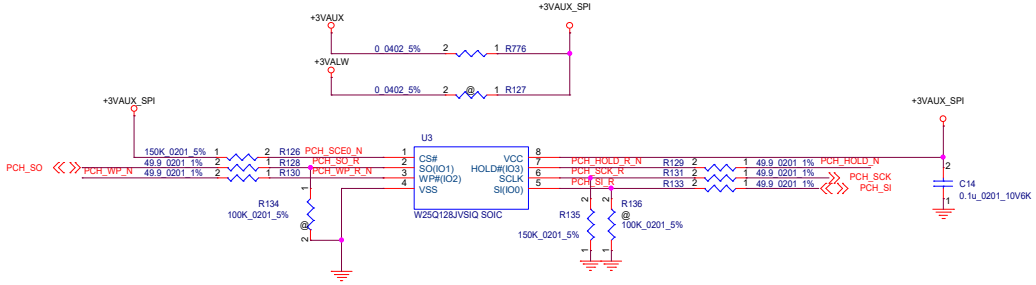
Title: CML MCP (PM)

Size: C | Document Number: S540-13 | Rev: V0.5

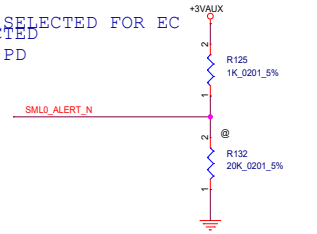
Date: Monday, June 17, 2019 | Sheet 8 of 63

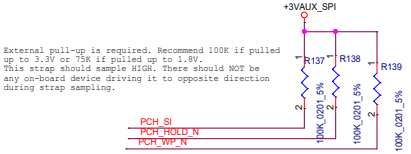






SML0_ALERT_N
HIGH: ESPI IS SELECTED FOR EC
LOW: LPC SELECTED
WEAK INTERNAL PD





External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

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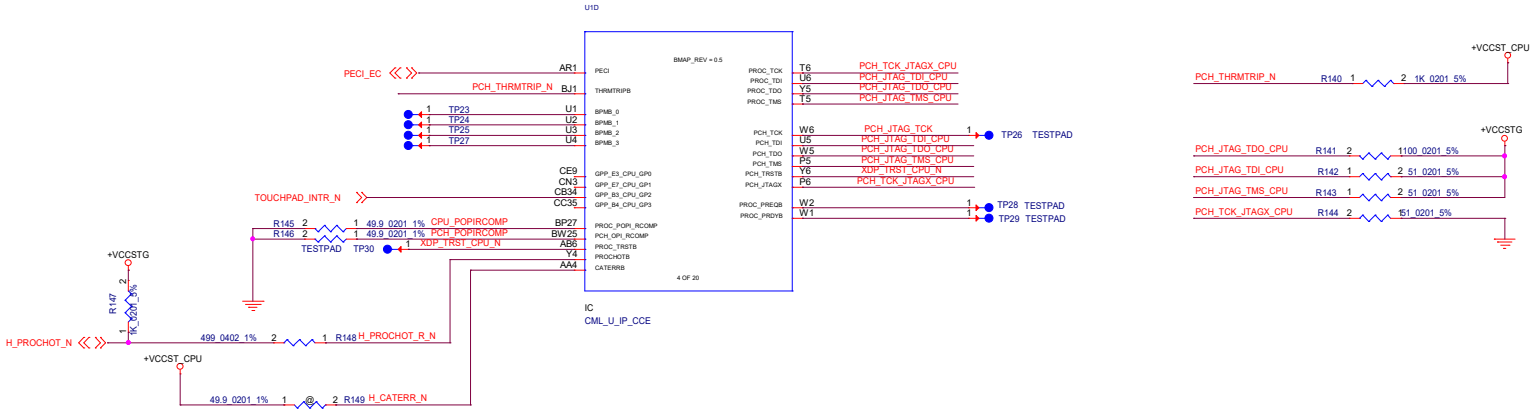
Title: CML MCP (eSPI SPI SMB CLINK)

Size: C | Document Number: S540-13 | Rev: V0.5

Date: Monday, June 17, 2019 | Sheet 9 of 63



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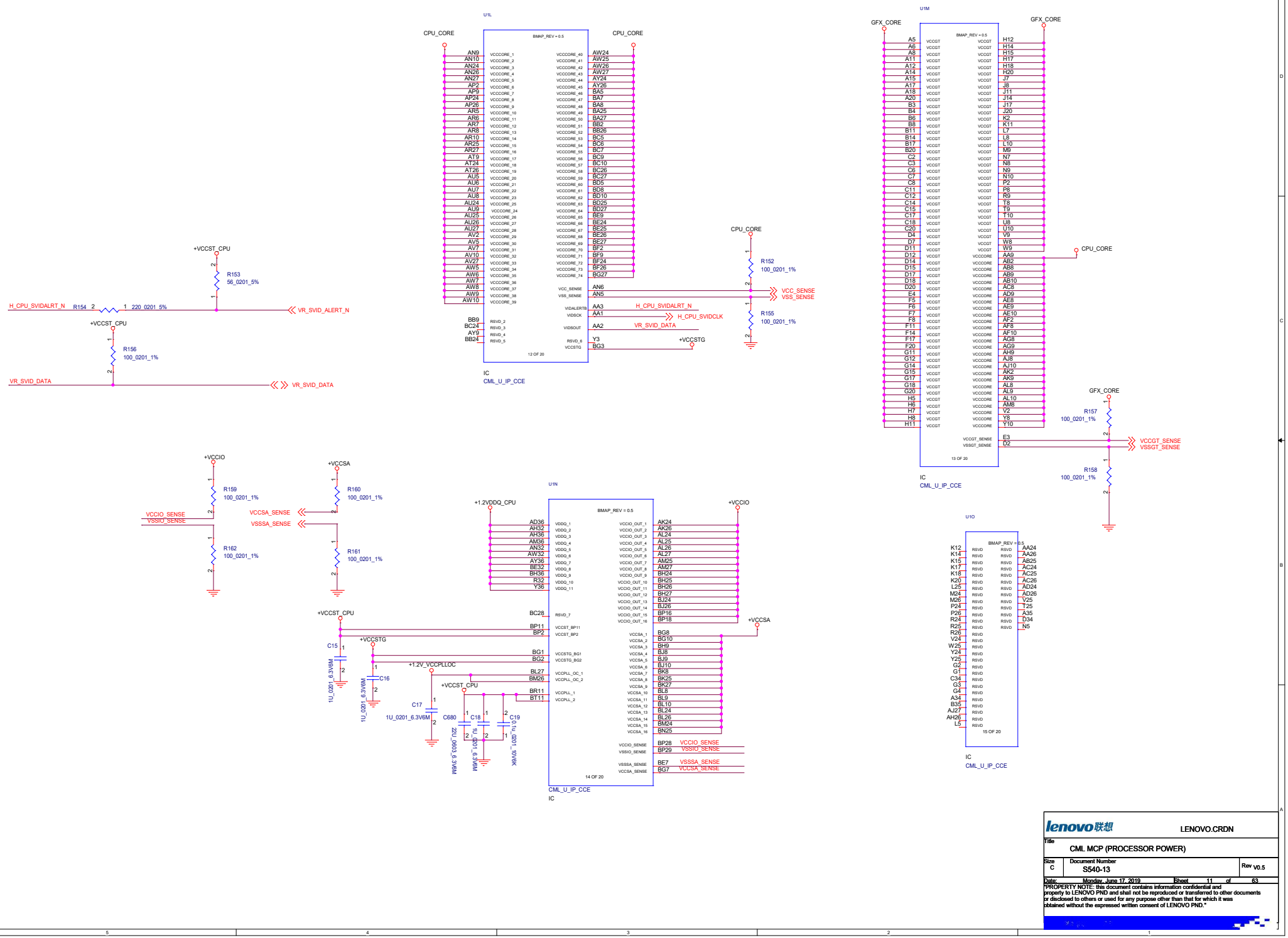
Title: CML MCP (MISC JTAG)

Size	Document Number	Rev
C	S540-13	V0.5

Date: Monday, June 17, 2019 Sheet 10 of 63



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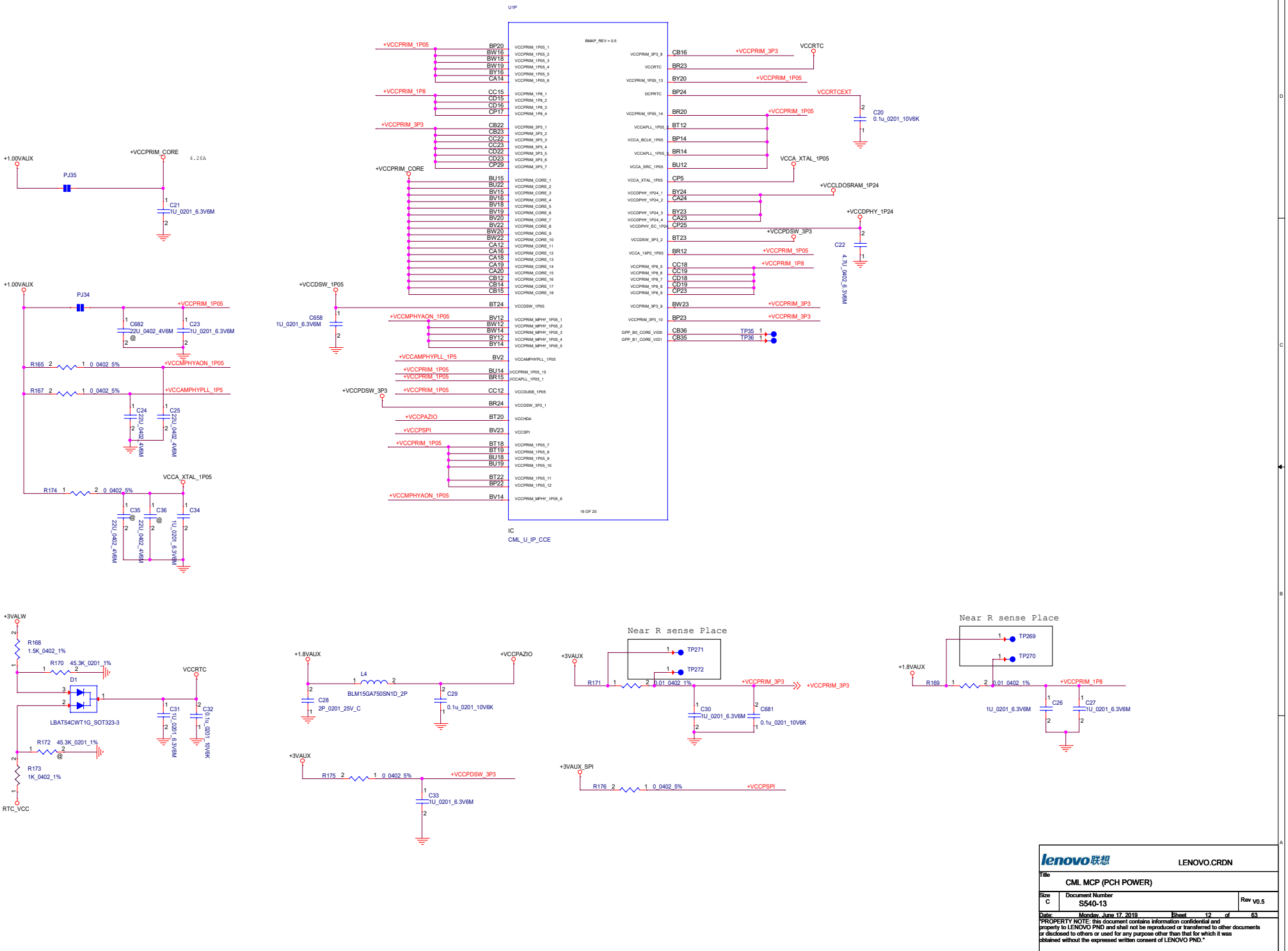
Title: CML MCP (PROCESSOR POWER)

Size	Document Number	Rev
C	S540-13	V0.5

Date: Monday, June 17, 2019 Sheet 11 of 63



Title	CML MCP (PCH POWER)
Size	C
Document Number	S540-13
Rev	V0.5
Date:	Monday, June 17, 2019
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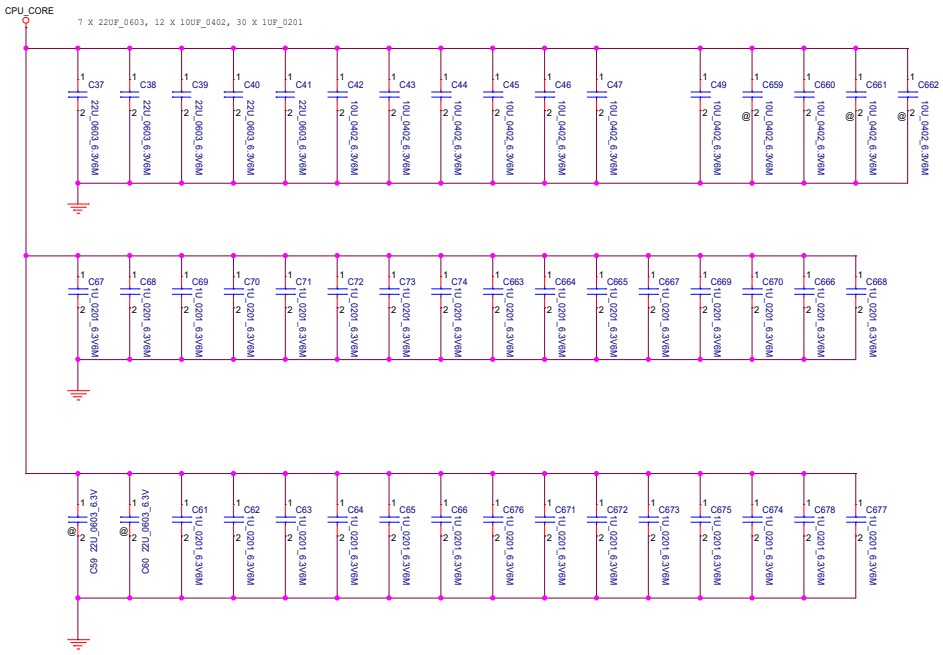

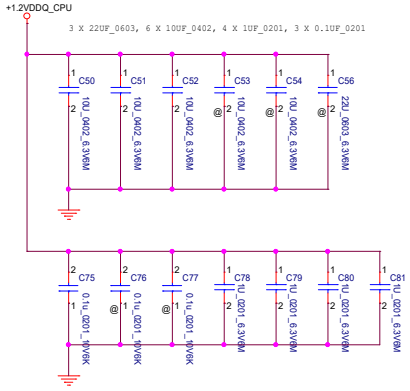

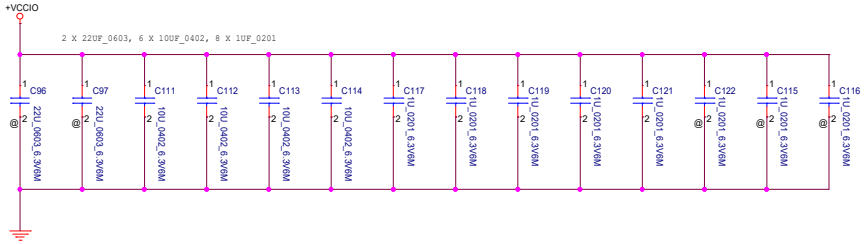

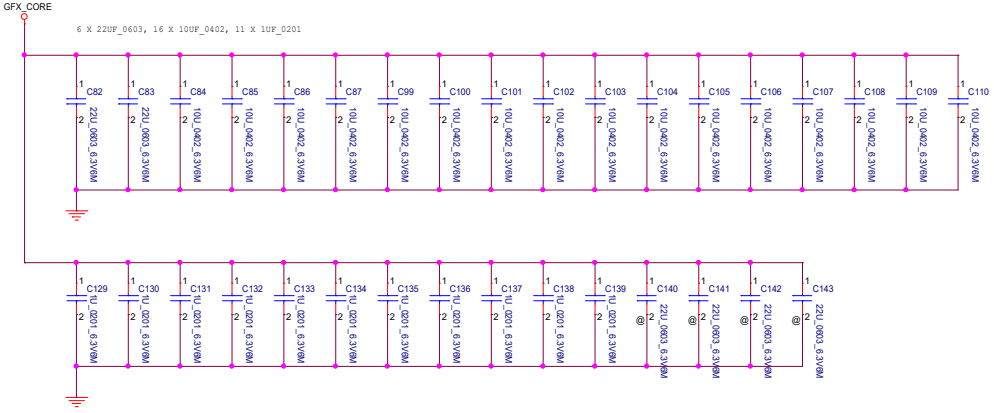

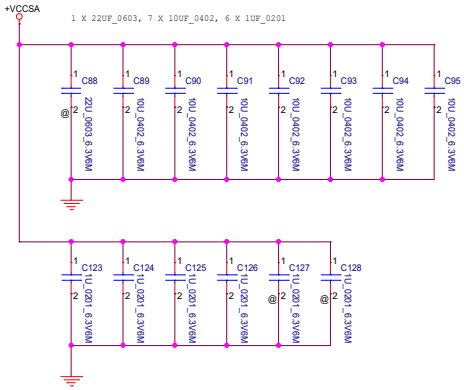

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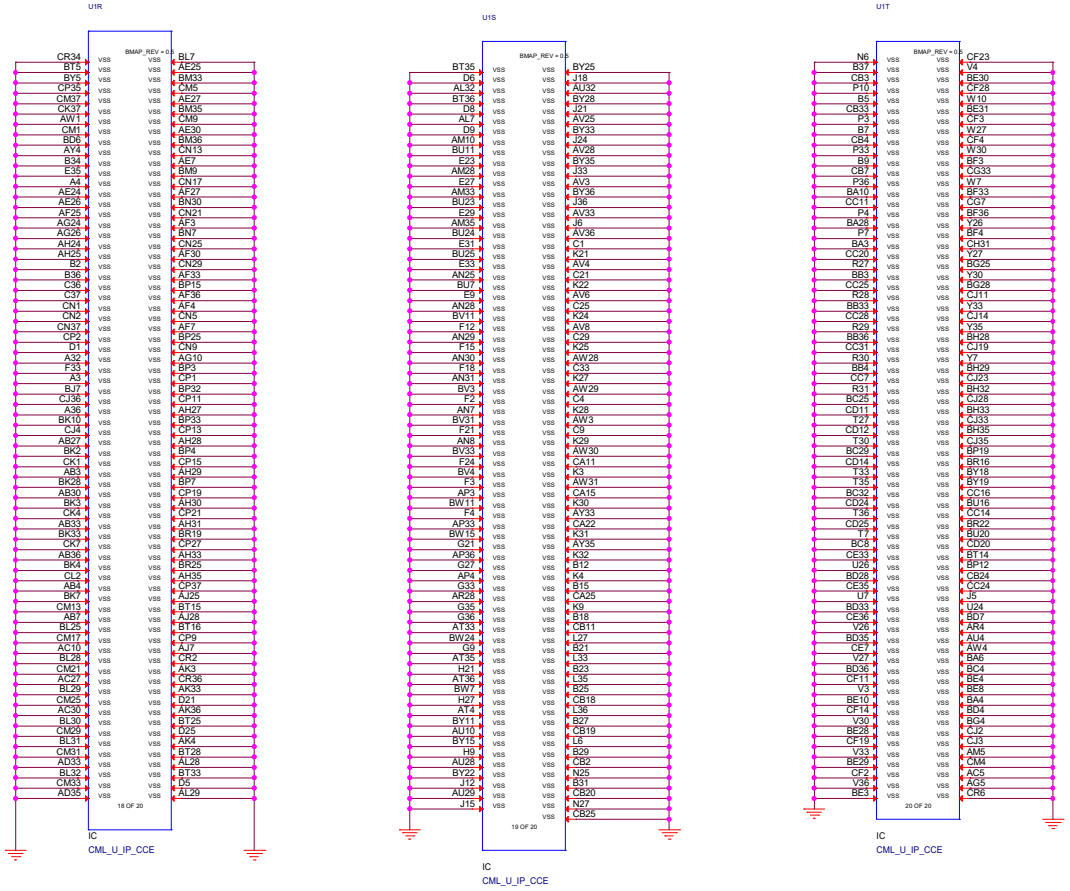
Title: CML MCP (Power CAP)

Size	Document Number	Rev
C	S540-13	V0.5

Date: Monday, June 17, 2019 Sheet 13 of 63



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Title: CML MCP (GND)

Size	Document Number	Rev
C	S540-13	V0.5

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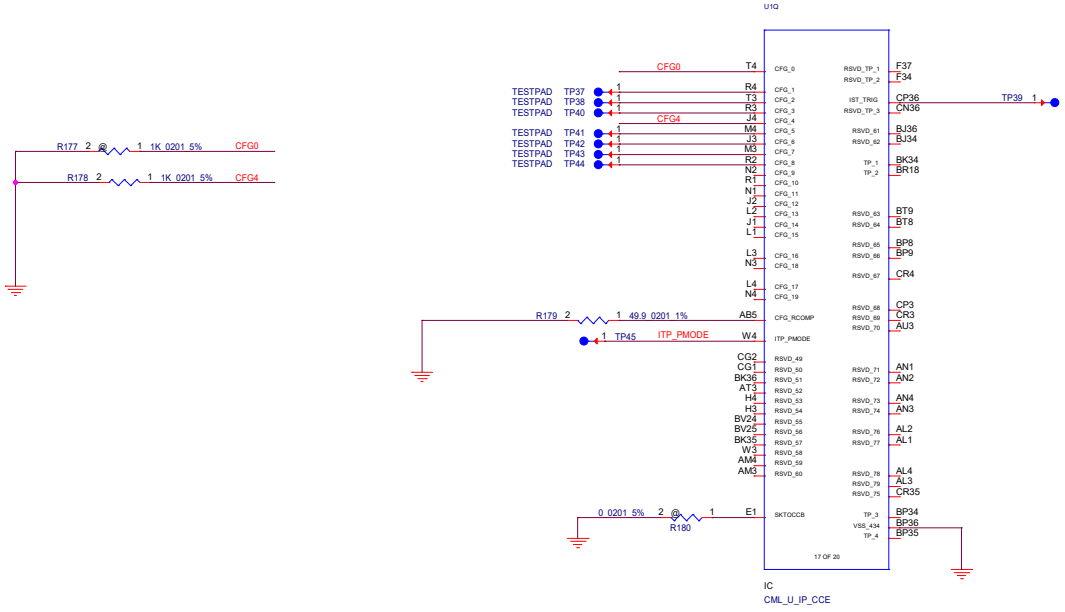
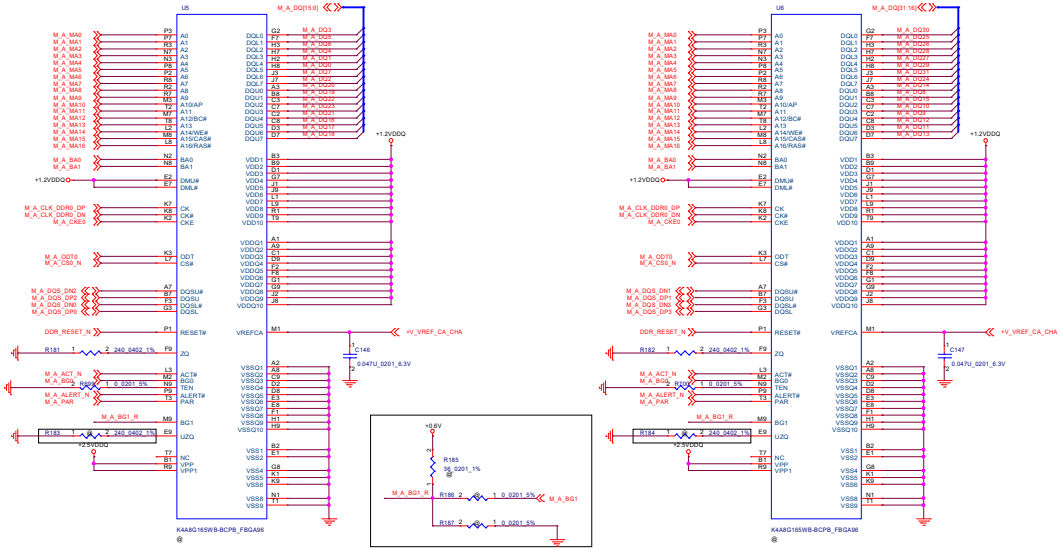
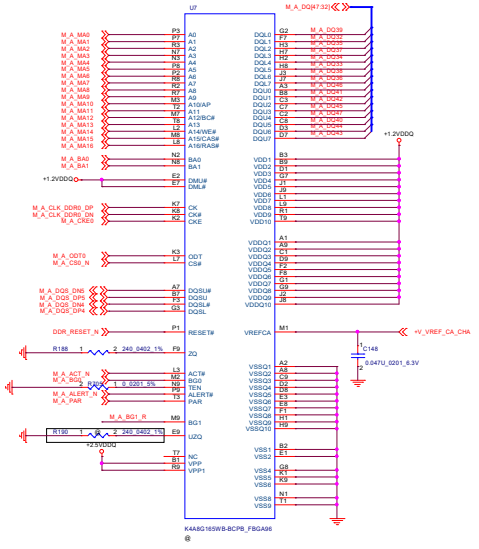
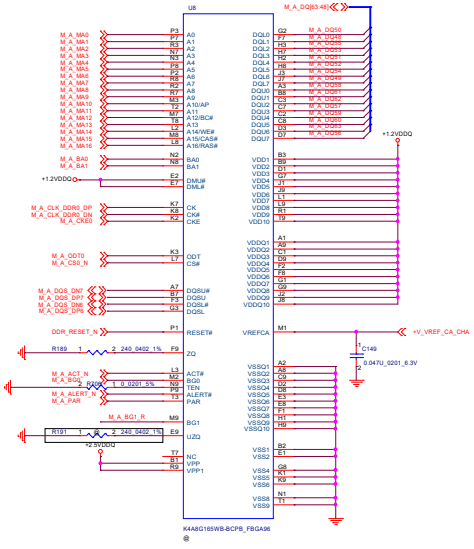


lenovo联想	LENOVO.CRDN	
Title: CML MCP (RSVD)		
Size: C	Document Number: S540-13	Rev: V0.5
Date: Monday, June 17, 2019	Sheet 15 of 63	

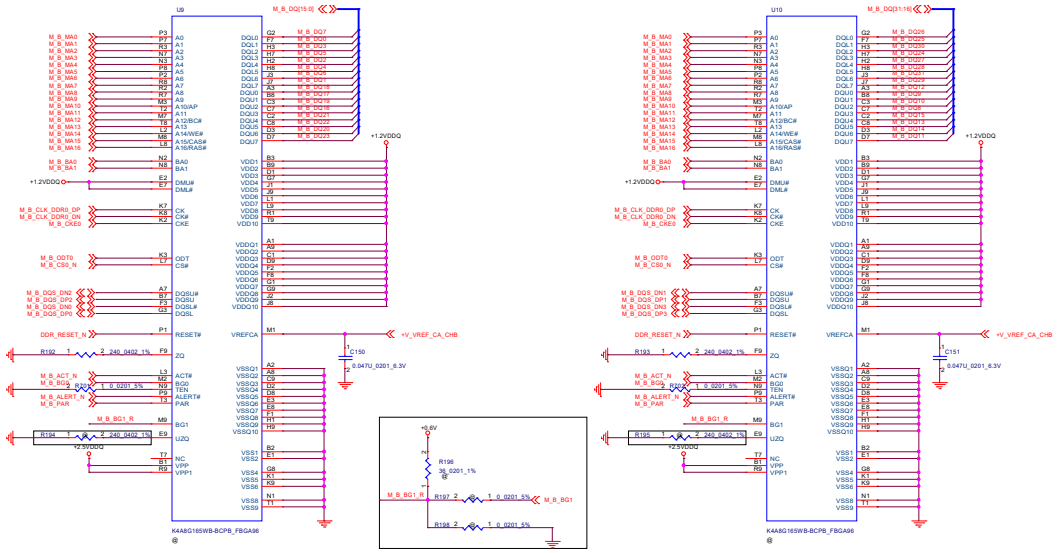


DDP: Stuff R186 and R185, Dummy R187; R183 184 190 191 @ 240ohm
SDP: Dummy R186 and R185, Stuff R187; R183 184 190 191 @ 0ohm



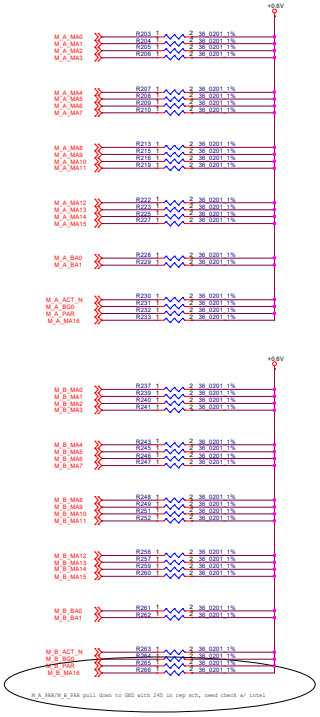


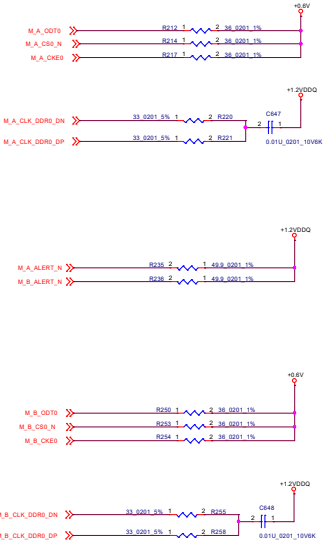
lenovo联想	LENOVO.CRDN	
Title: DDR4-CHA ONBD		
Size: D	Document Number: S540-13	Rev V0.5
Date: Monday, June 17, 2019	Sheet 15 of 63	

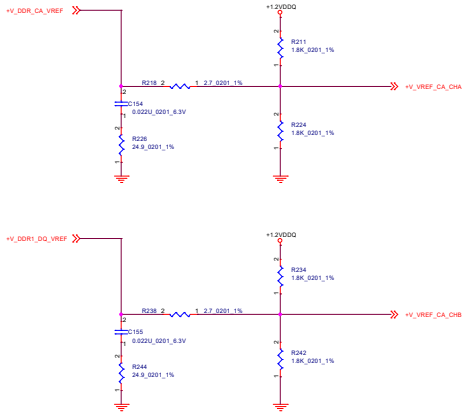


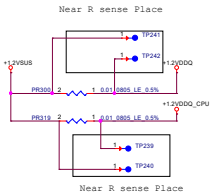
DDP: Stuff R197 and R196, Dummy R198; R194 195 201 202 @ 240ohm
SDP: Dummy R197 and R196, Stuff R198; R194 195 201 202@ 0ohm

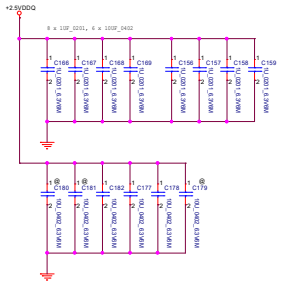
lenovo 联想	LENOVO.CRDN	
Title: DDR4-CHB ONBD		
Size: D	Document Number: S540-13	Rev V0.5
Date: Monday, June 17, 2019	Sheet 17 of 63	

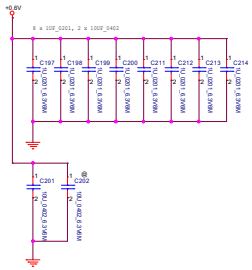












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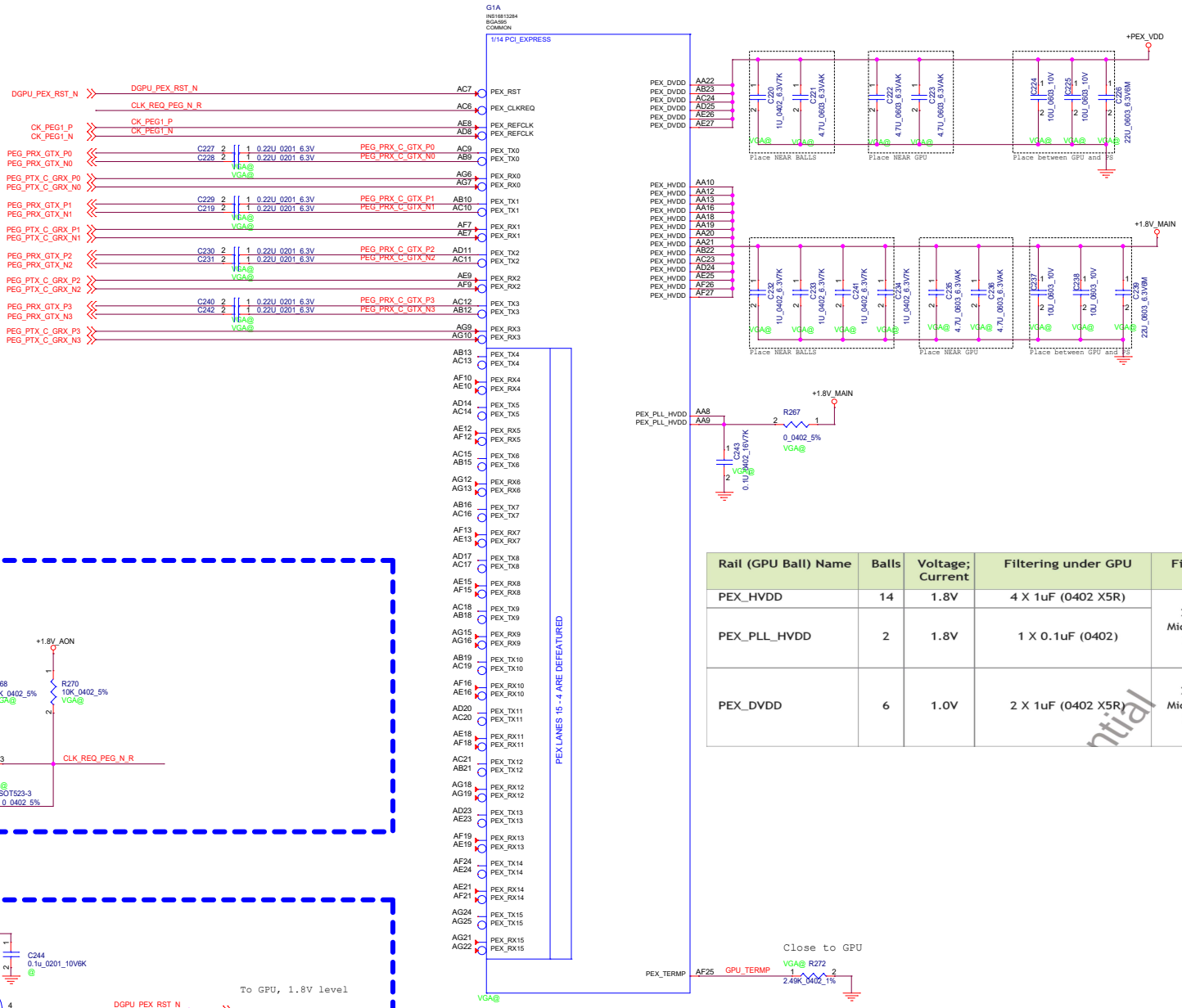
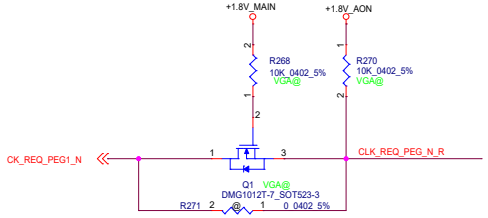
Title	DDR4- TERMINATION&DECOUPLING		
Size D	Document Number S540-13		Rev V0.4
Date: Monday, June 17, 2019	Sheet 18 of 63		

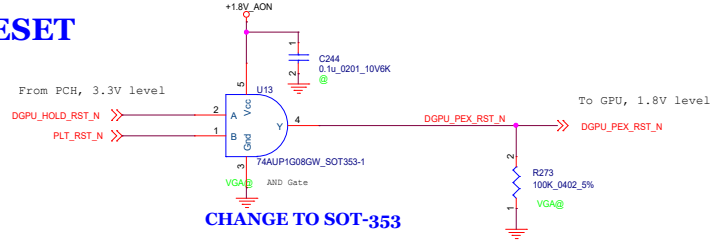


Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

CLK_REQ_N



GPU RESET



CHANGE TO SOT-353

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Title: GPU PCIE

Size: C | Document Number: S540-13 | Rev V1.0

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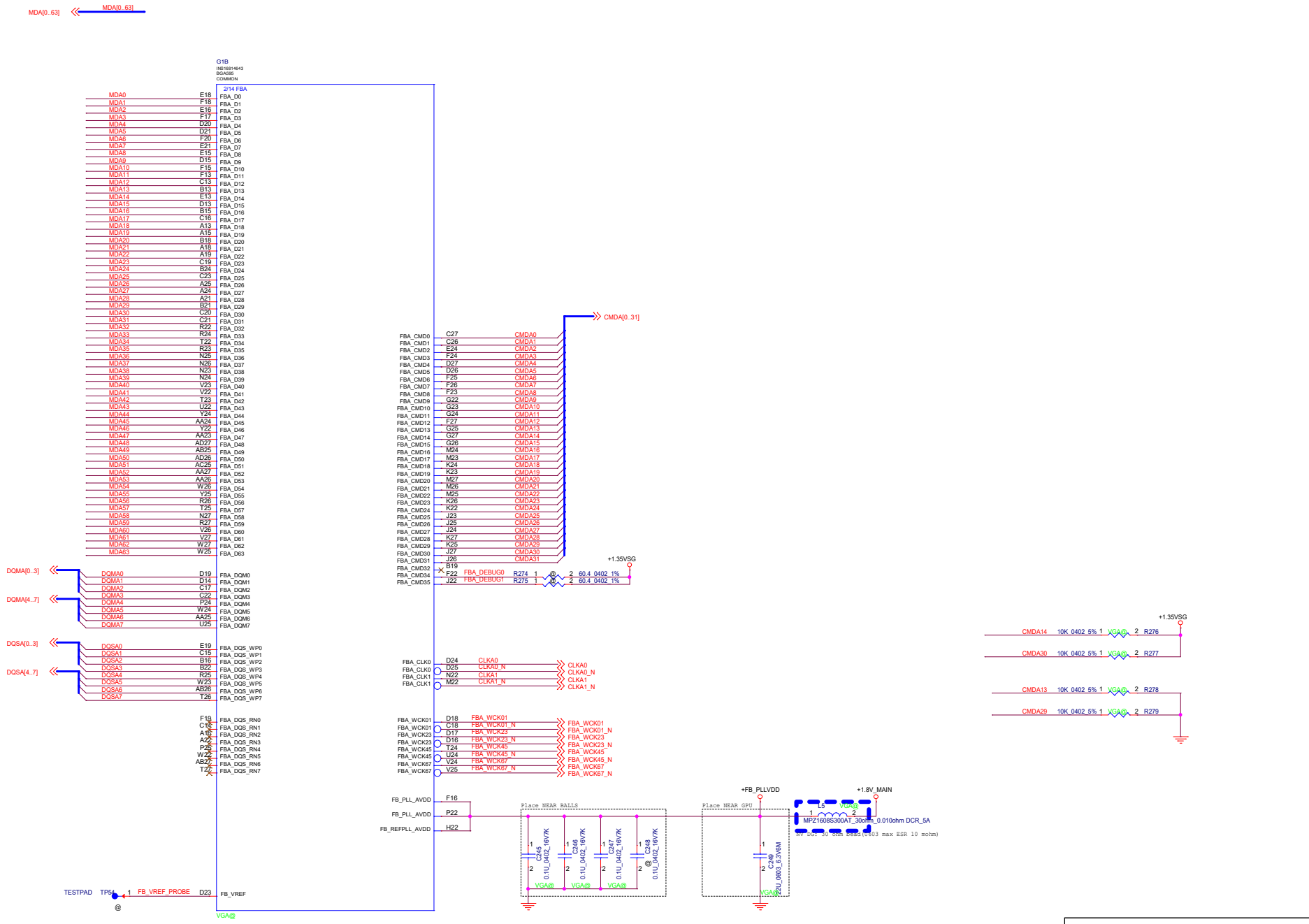

FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)
FBB_PLL_AVDD	1		1 X 30Ω bead (0603 max ESR 10 mΩ)
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)
			1 X 22uF (0805)

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Title: GPU FB_A

Size: C | Document Number: S540-13 | Rev V0.1

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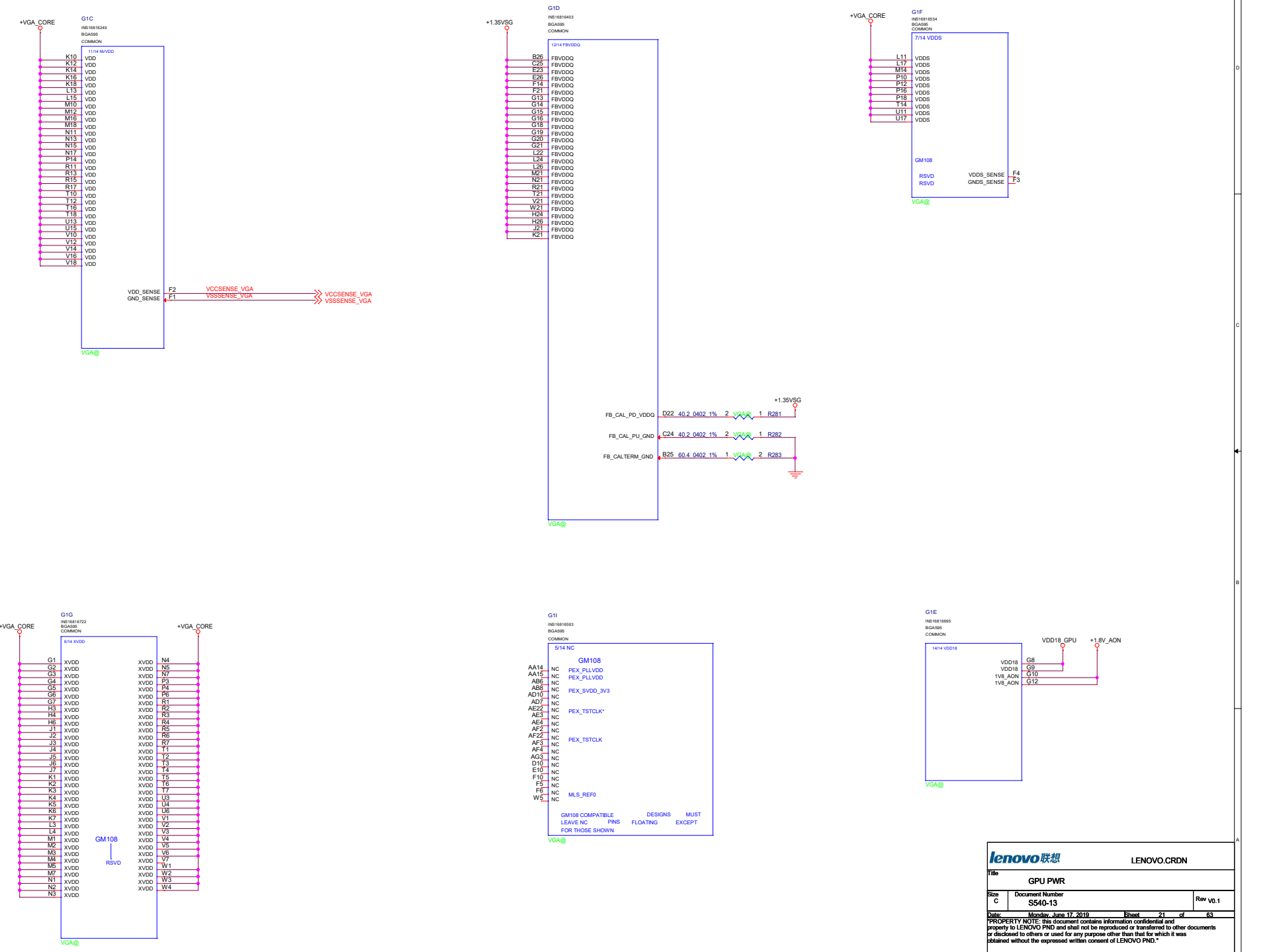

lenovo联想	LENOVO.CRDN	
Title: GPU PWR		
Size: C	Document Number: S540-13	Rev: V0.1
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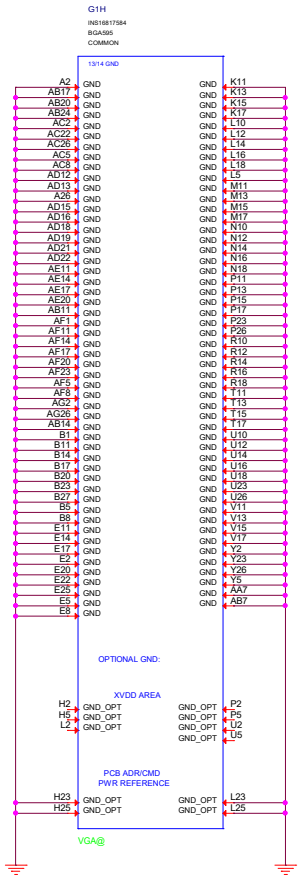

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Title

GPU GND

Size	Document Number	Rev
C	S540-13	V0.1

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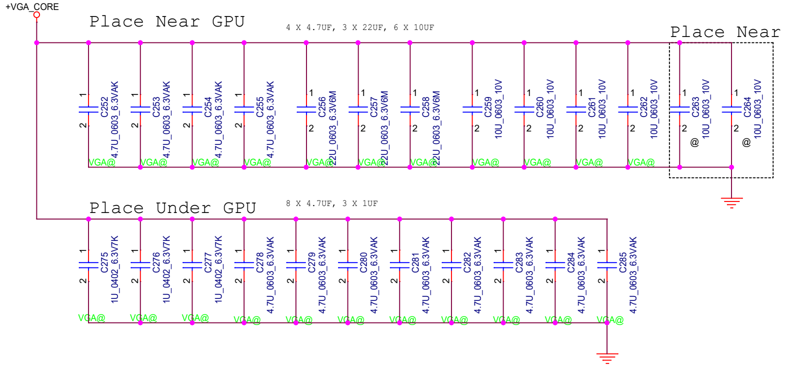
Follow NV ref-design



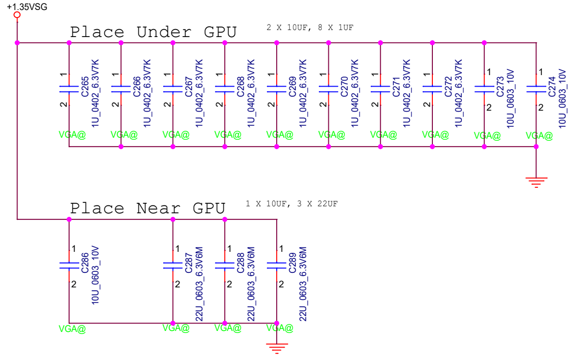
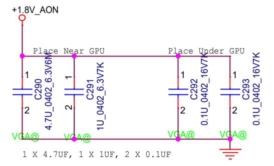
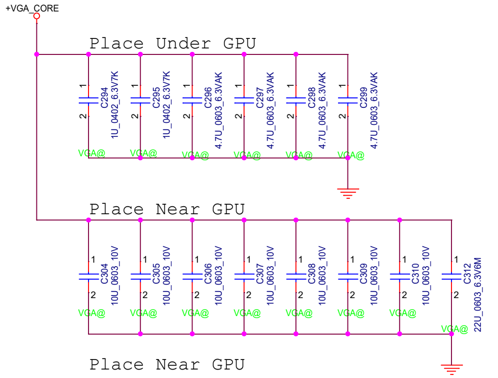


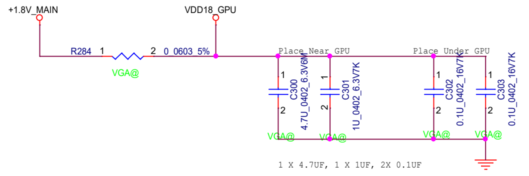
Table 7.18 GB2C-64 Package: Power Rail Filtering

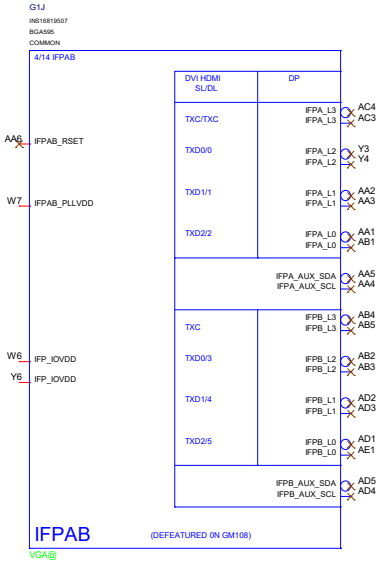
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	4 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Poscap) Near VR: 2 X 10uF (0805)
NVVDDS	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)





1 x 22uF
7x 10uF
4 x 4.7uF
2 x 1uF





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Title: GPU IFP AB		
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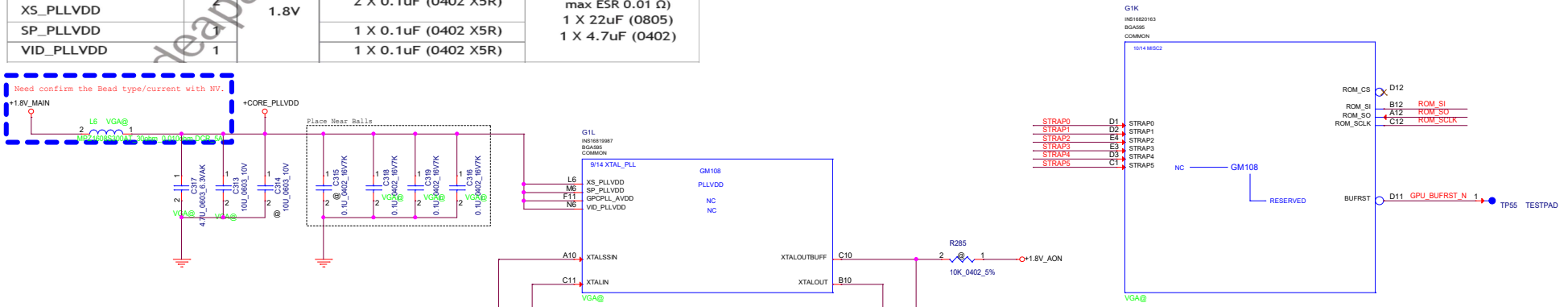
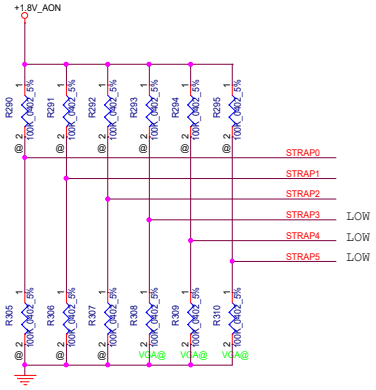
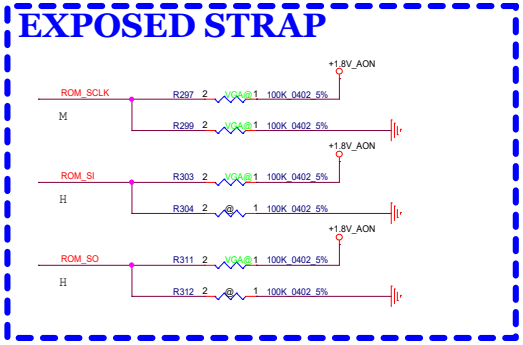
GPCPLL_AVDDx	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
XS_PLLVDD				
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	



STRAP



EXPOSED STRAP



STRAP0~2 , Please ref RVL for BOM stuffing
Micron: L M L
Hynix : H M L

GDDR5 RAM_CFG															
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Nurnber	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17S-G1	GDDR5	1.35V	8Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	7 Gbps	N/A	0x0	L	L	L	Prodution ready
							K4G80325FB-HC25		8 Gbps	N/A					Substitution allowed with waiver
						Micron	MT51J256M32HF-70:A	A-die	7 Gbps	N/A	0x1	L	L	H	Prodution ready
							MT51J256M32HF-80:A		8 Gbps	N/A					Substitution allowed with waiver
						Hynix	H5GC8H24MJR-R0C	M-die	7 Gbps	N/A	0x2	L	H	L	Post-Prodution Candidate
							H5GC8H24MJR-R4C		8 Gbps	N/A					Substitution allowed with waiver
						Micron	MT51J256M32HF-70:B	B-die	7 Gbps	N/A	0x4	H	L	L	Post-Prodution ready
							MT51J256M32HF-80:B		8 Gbps	N/A					Substitution allowed with waiver
						Hynix	H5GC8H24AJR-R0C	A-die	7 Gbps	N/A	0x5	H	L	H	Post-Prodution ready
							H5GC8H24AJR-R2C		8 Gbps	N/A					Substitution allowed with waiver

GDDR5 RAM_CFG															
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Nurnber	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17S-G0/G2	GDDR5	1.35V	8Gb	256Mx32	Micron	MT51J256M32HF-80:B	B-die	8 Gbps	N/A	0x9	L	M	L	Prodution ready
					512Mx16	Hynix	H5GC8H24AJR-R2C	A-die	8 Gbps	N/A	0xA	L	M	H	Prodution ready

ROM_SCLK(LSB)/ROM_SI/ROM_SO(MSB) : H H M

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins (see Note)			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
9	H	H	L	ENABLED	disabled	disabled	disabled
0	H	H	H	disabled	disabled	disabled	disabled
	All other Strap Configurations			(Reserved, do not configure)			
				(Reserved)			

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Title	GPU PLL/XTAL	
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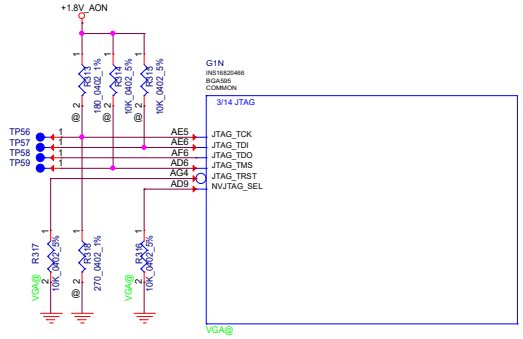

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Size: C	Document Number: S540-13	Rev: V0.1
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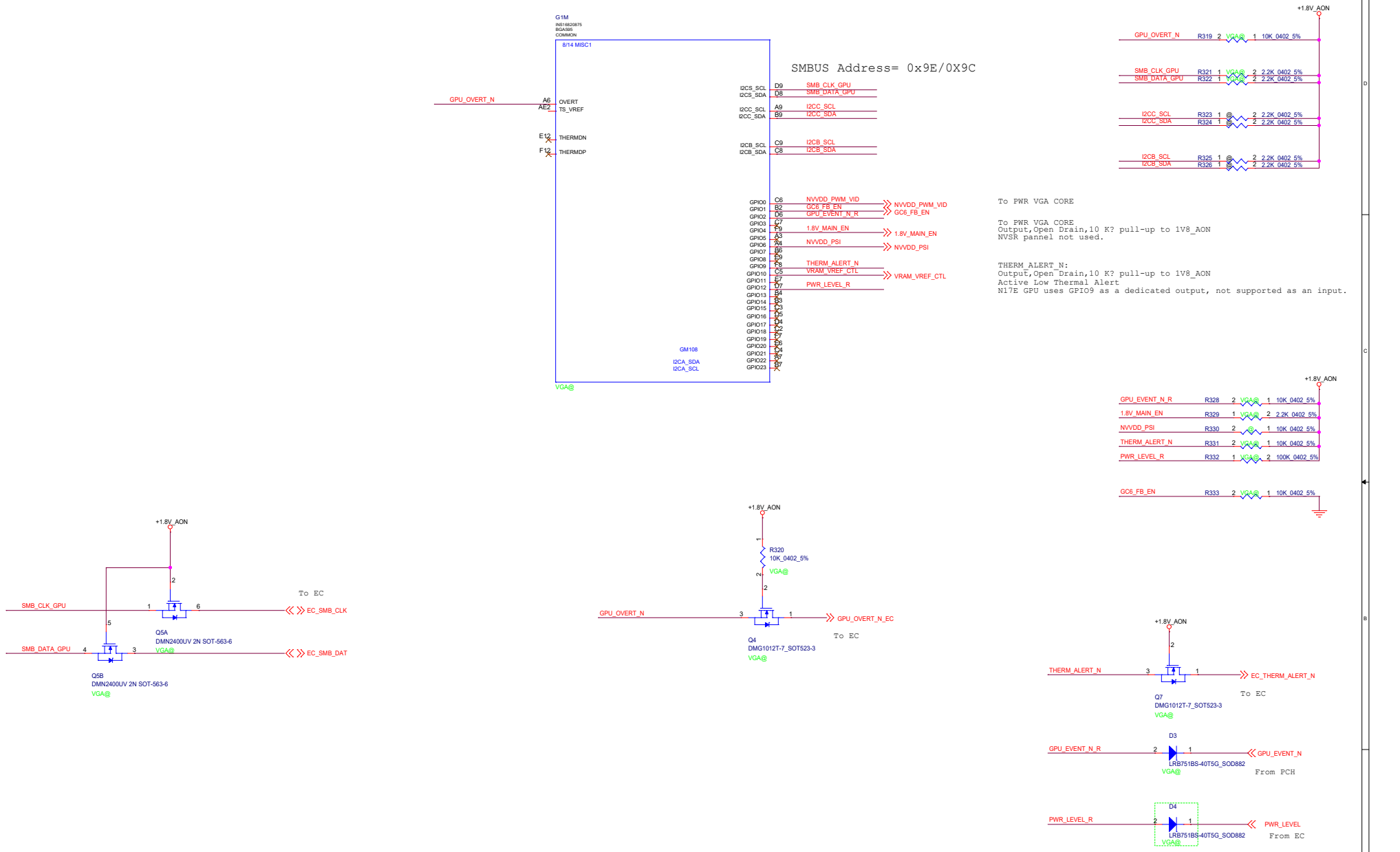

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Size: C	Document Number: S540-13	Rev V0.1
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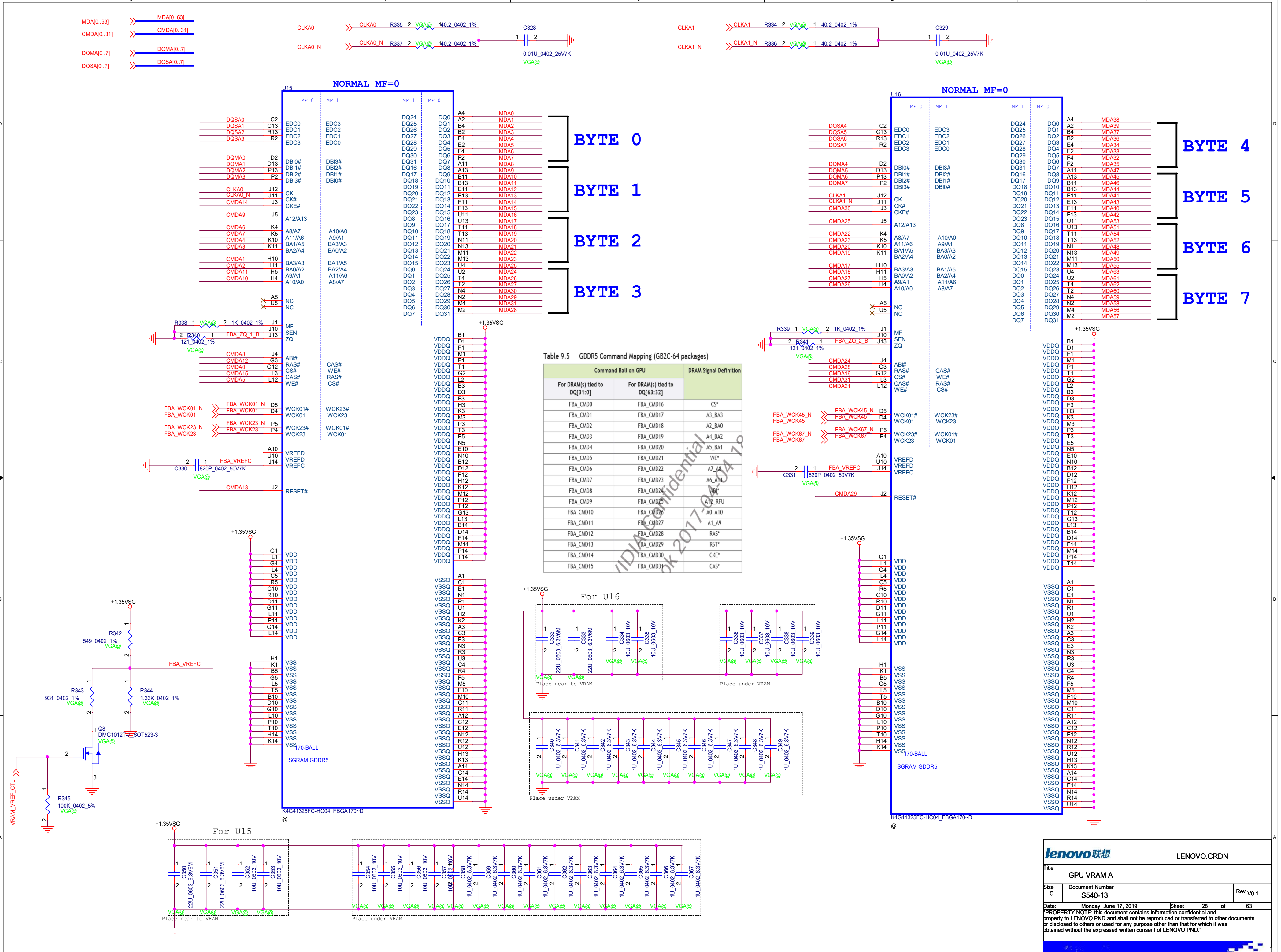

Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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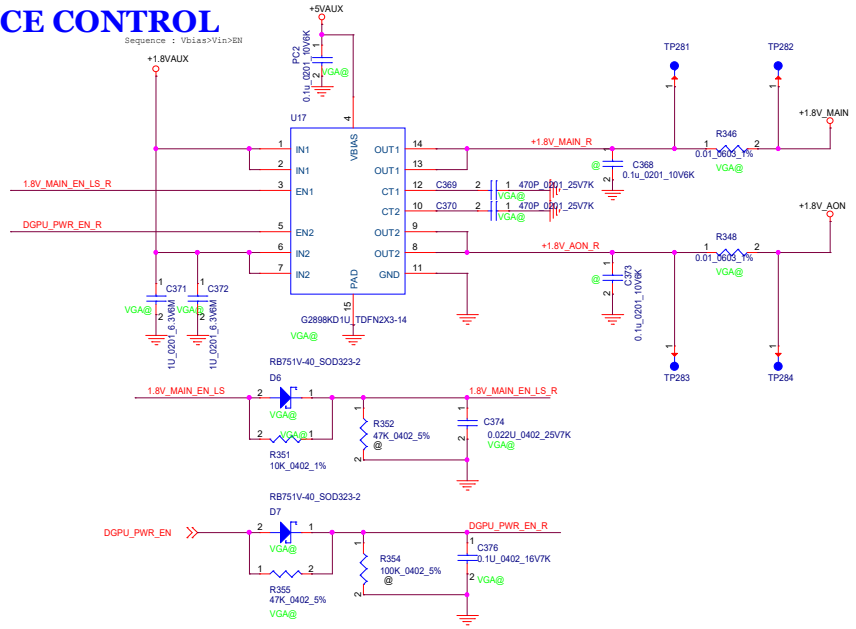
POWER SEQUENCE CONTROL



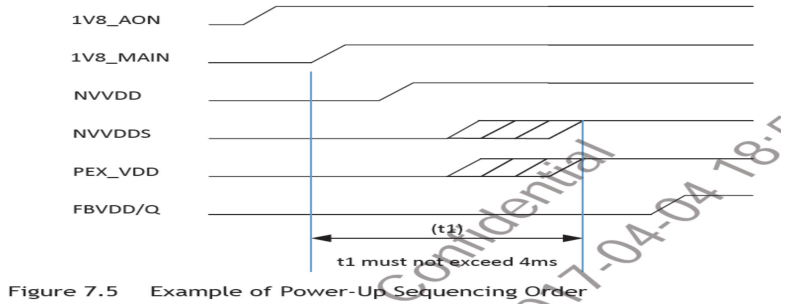


Figure 7.5 Example of Power-Up Sequencing Order

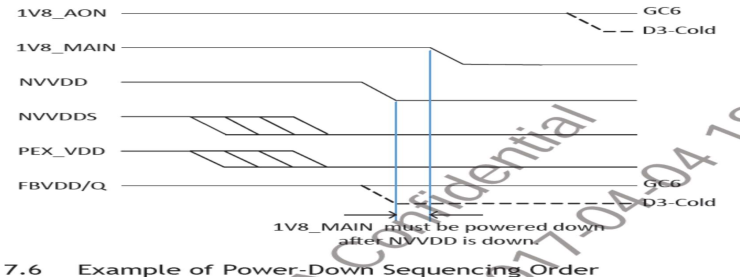
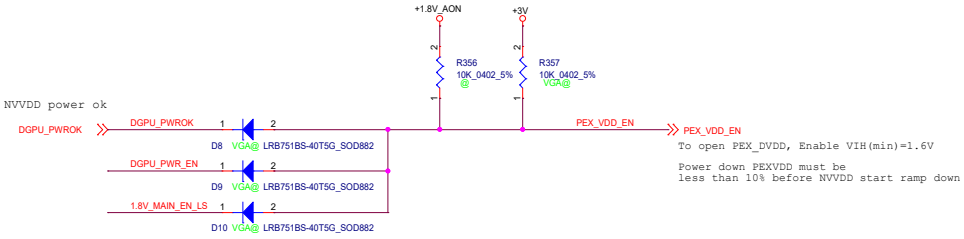
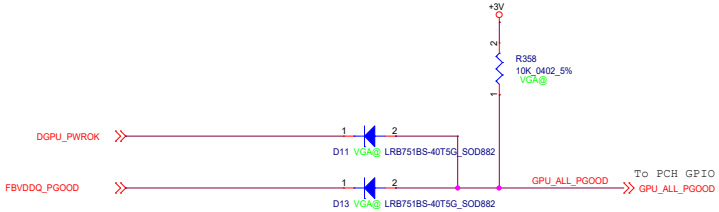
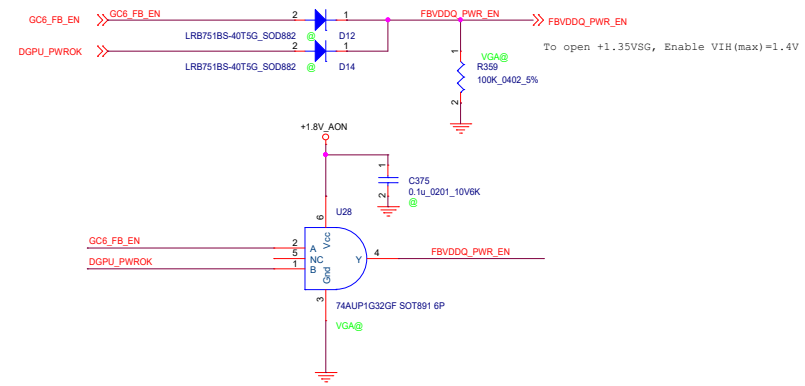
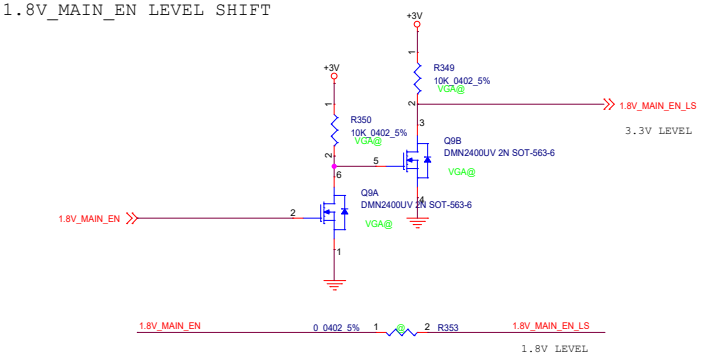


Figure 7.6 Example of Power-Down Sequencing Order









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Title: GPU Switch/Thermal

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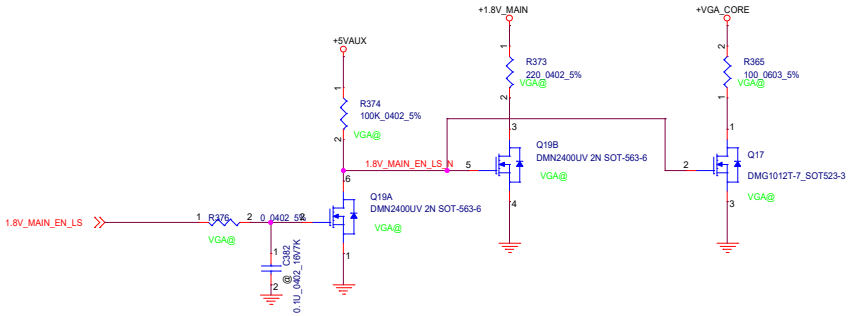

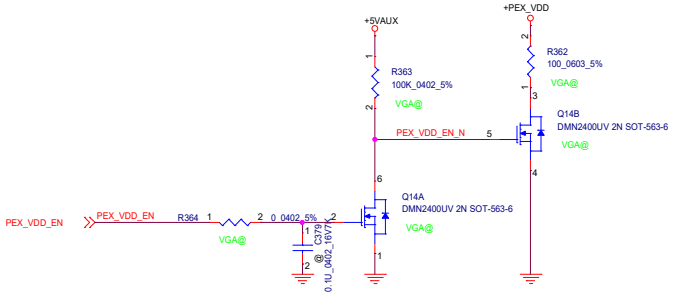

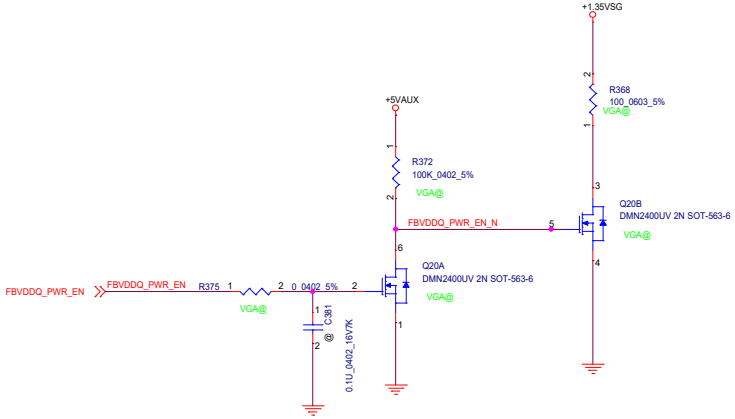

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Title: GPU POWER DISCHARGE

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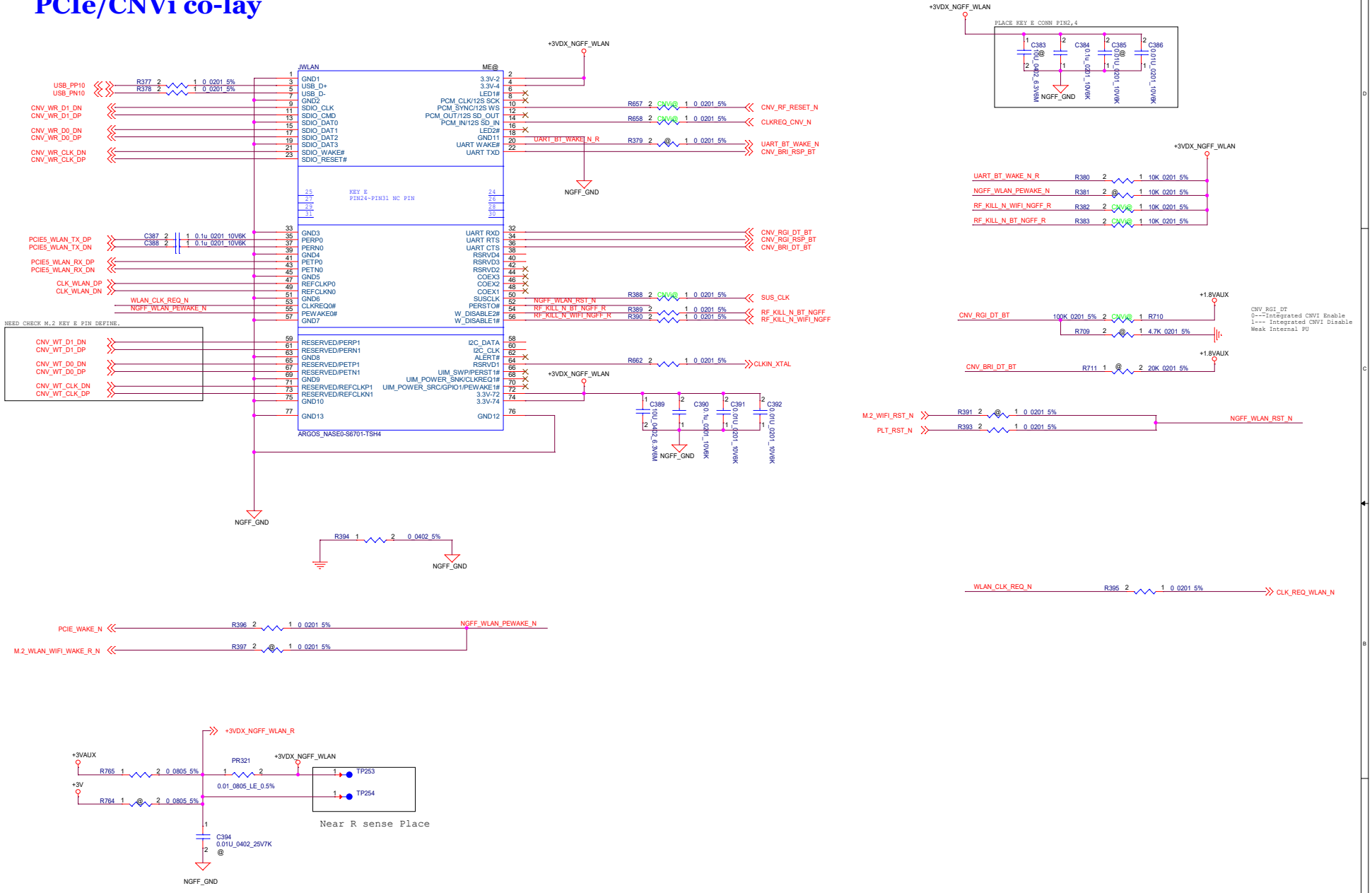
PCIe/CNVi co-lay



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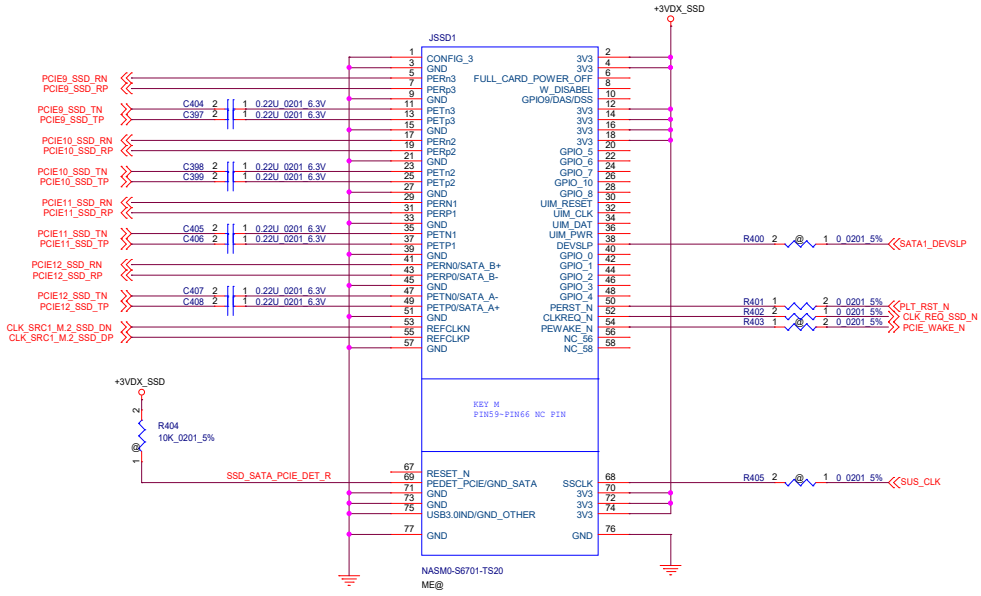

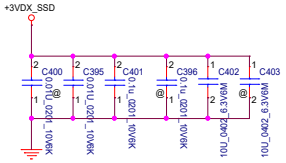

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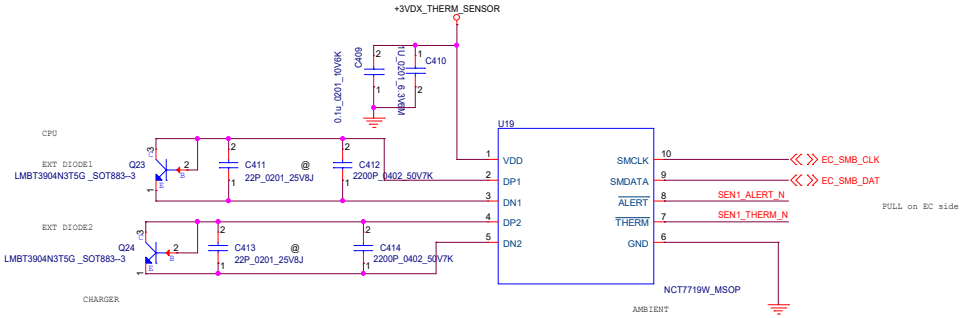

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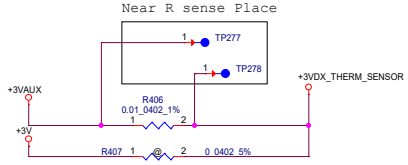

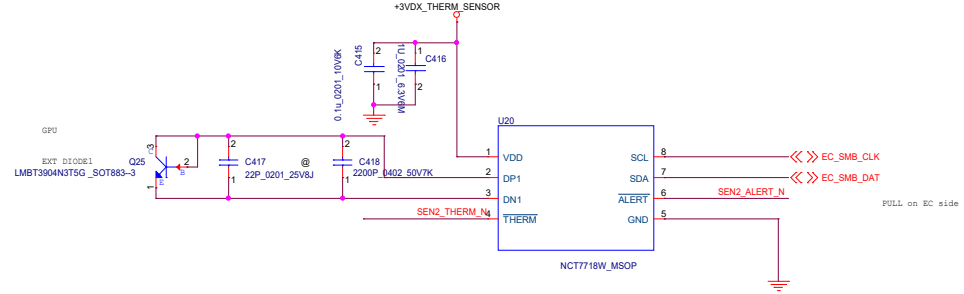

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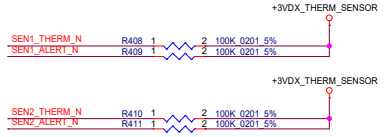

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Title: ThermalSensor

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Title

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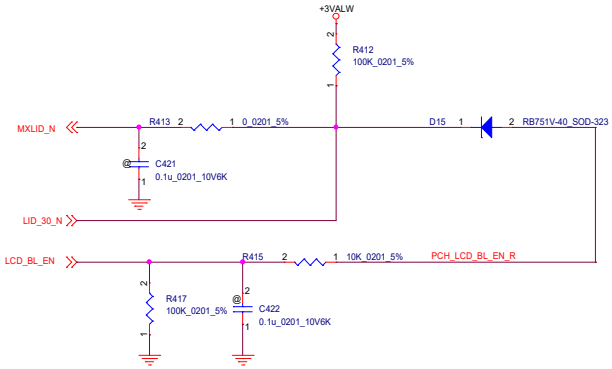

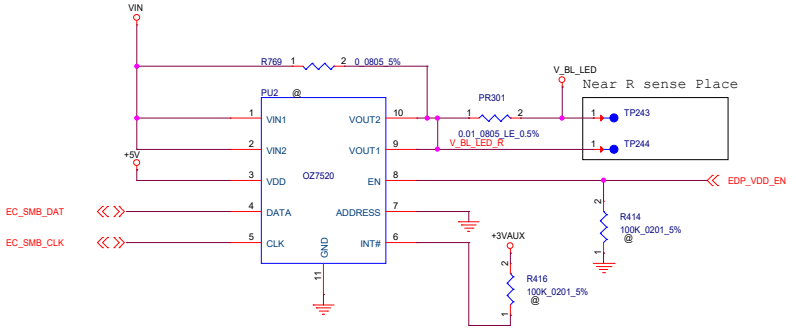

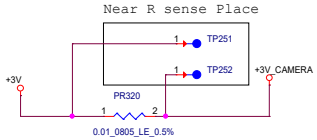

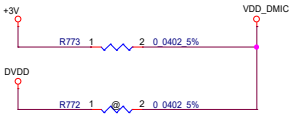

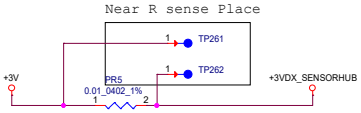

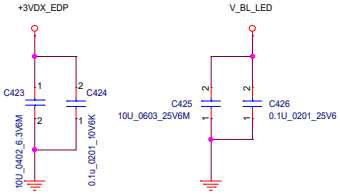

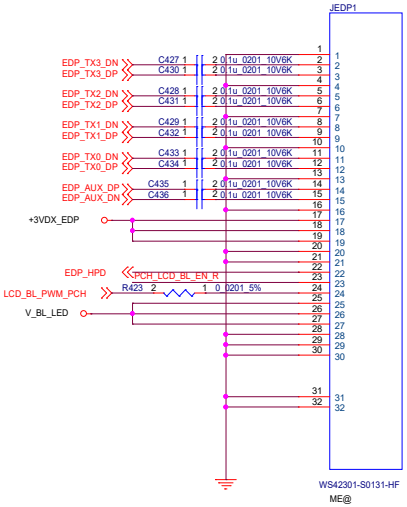

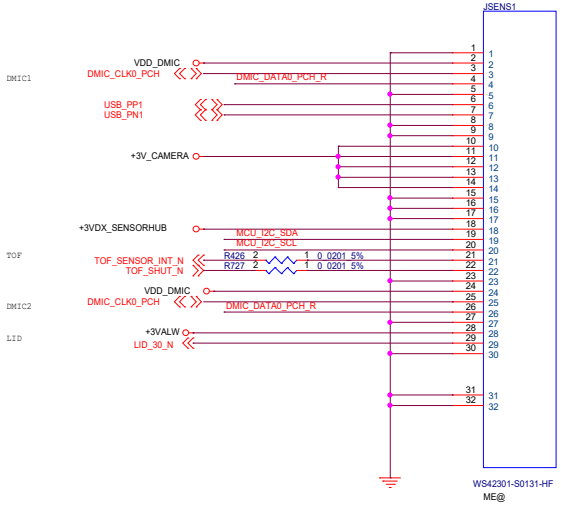

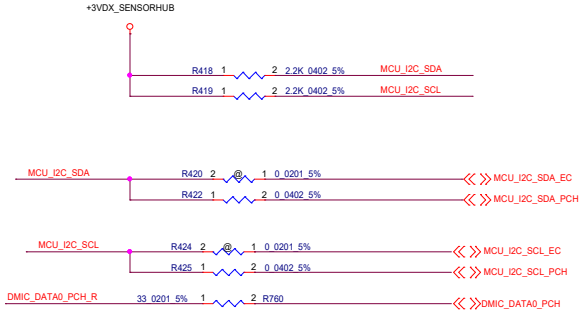

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Title: EDP/CAMERA

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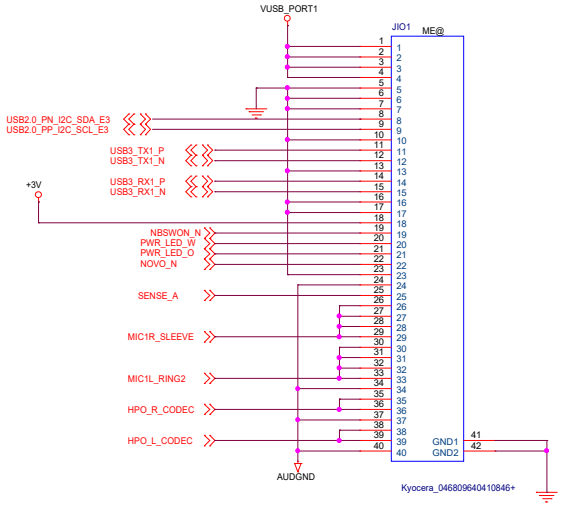

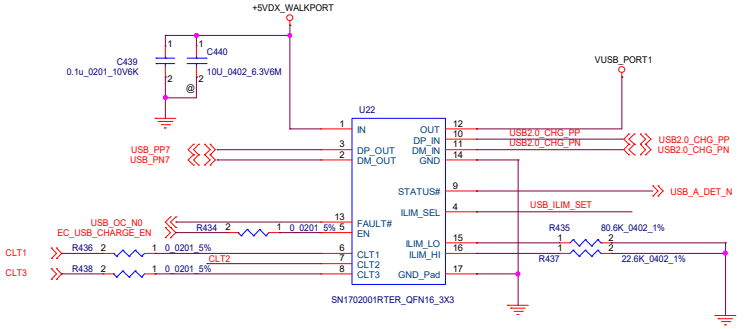

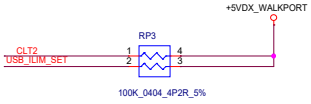


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Install ILIM_SEL shunt for ILIM = ILIM_LO = 0.63A
Remove ILIM_SEL shunt for ILIM =ILIM_HI = 2.3A
Support Mouse/Keyboard wake up.
Support Power Wake
CLT1      CLT3
 1         0   --    SDP
 0         1   --    DCP/Auto
```

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Title: USB 3.1 GEN2

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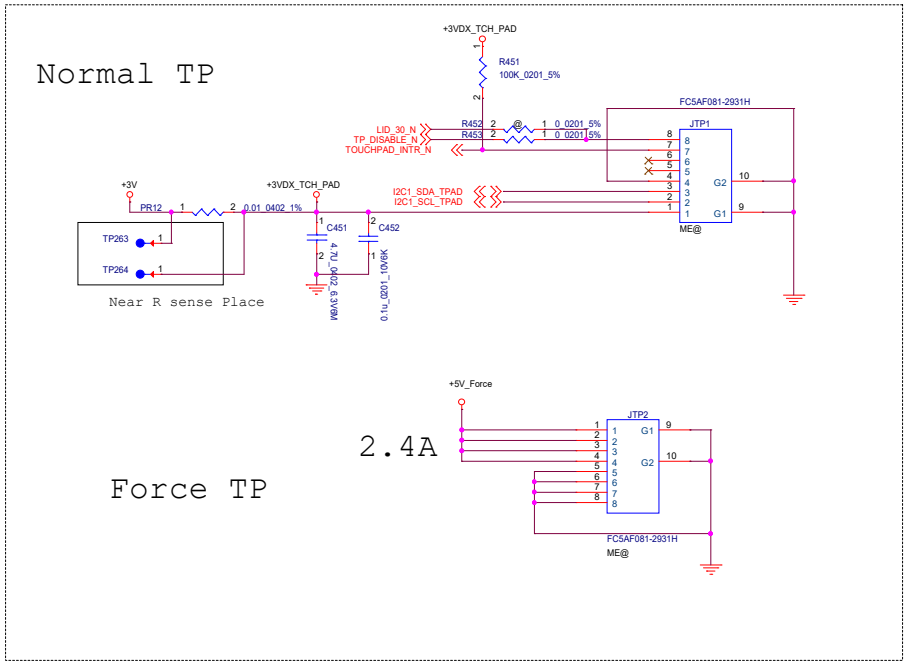

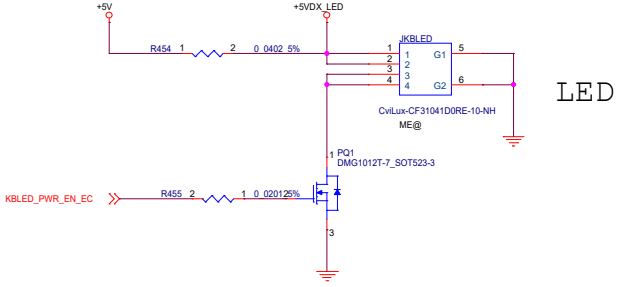

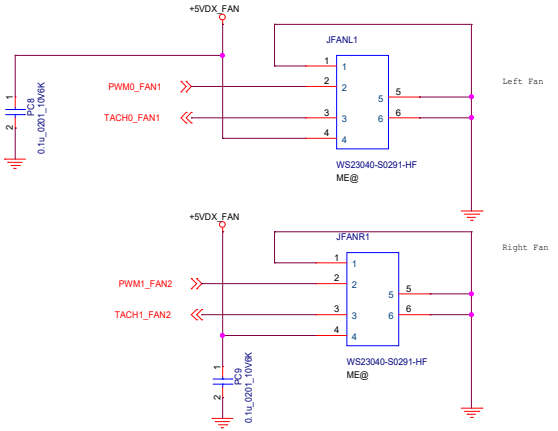

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Title: TP/KB LED

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Near R sense Place

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

* Recommended net "+3VAUX" and "RTCVCC" minimum trace width 12mils.

CAD NOTE: VDDQ_EN_EC
Go high after VPP_EN_EC hign when power on.
Go low before VPP_EN_EC low when power off.

CAD NOTE: EC_VCCST_PWRGD
VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST.
Go high/low with ALL_SYS_PWRGD_PMIC

IT8229 VFBGA

U25 IT8229VG-192

U24 SLG4T42224

Q27 DMG1012T-7_SOT523-3

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Title: BLANK

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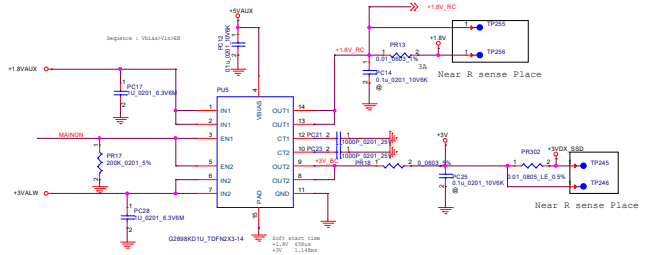

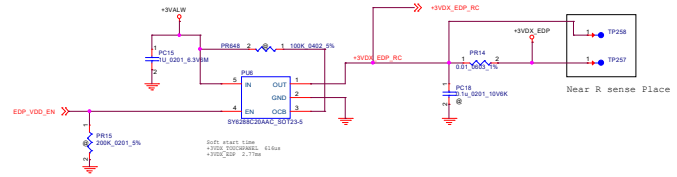

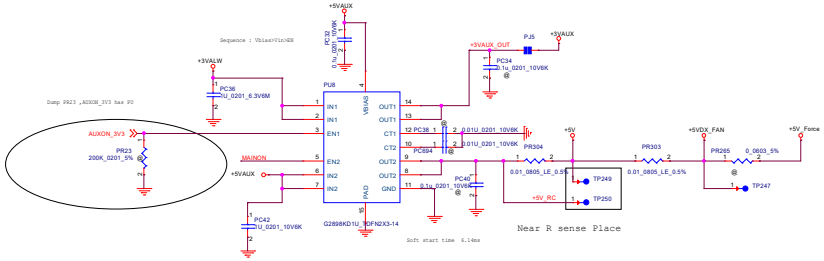

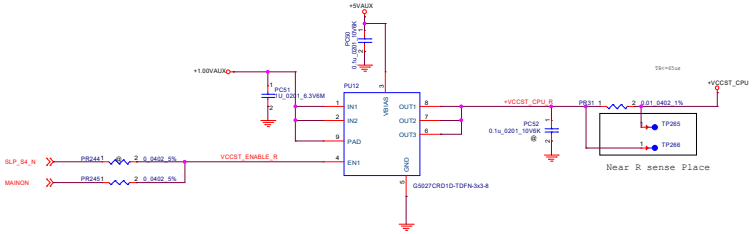

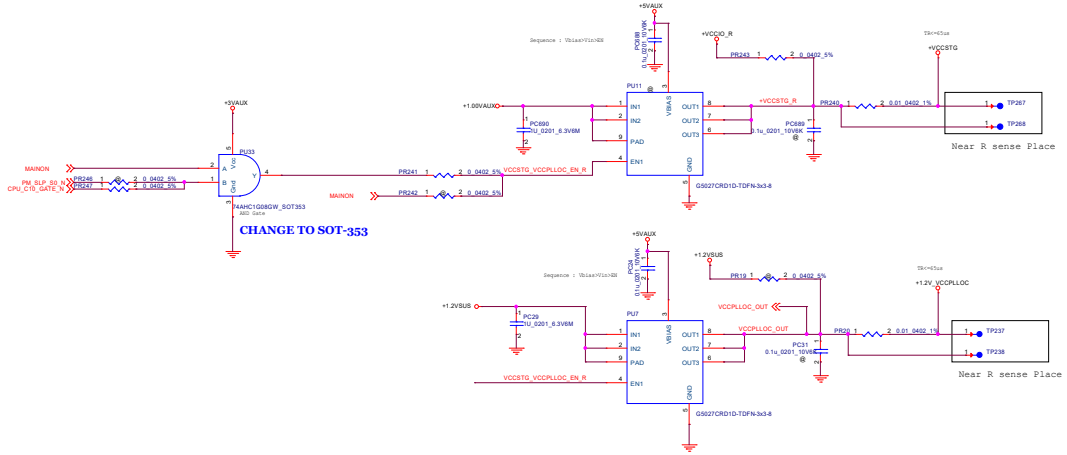

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Title: SWITCH POWER

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Title

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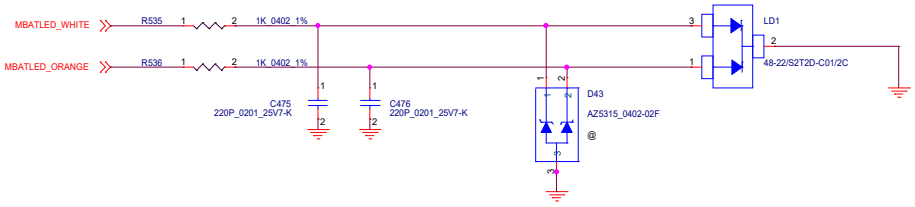

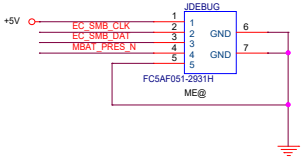

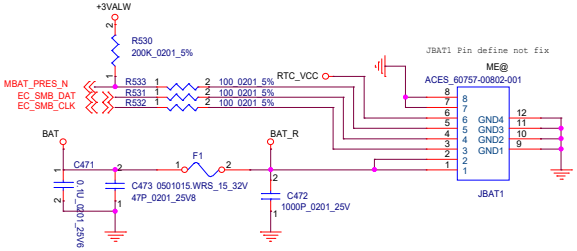

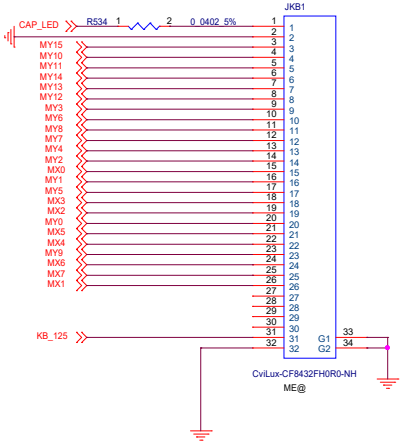

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Title: CONNECTOR

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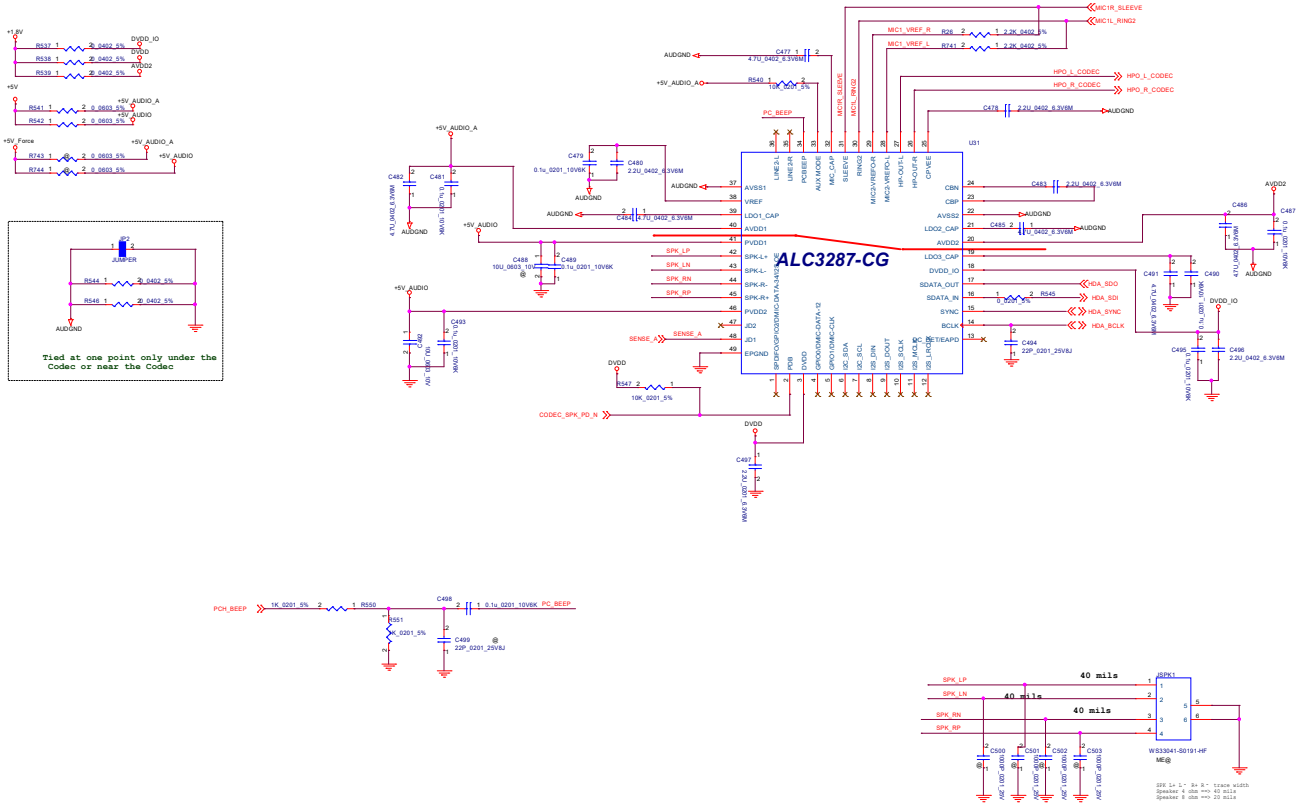

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Title: Audio		
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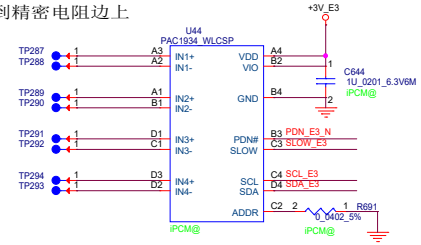
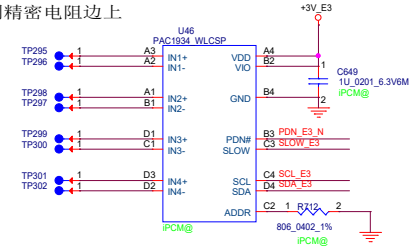
测点画到精密电阻边上



测点画到精密电阻边上



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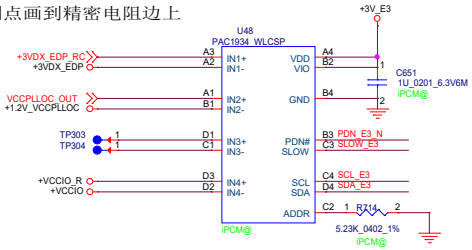
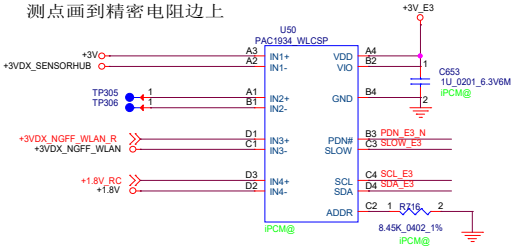
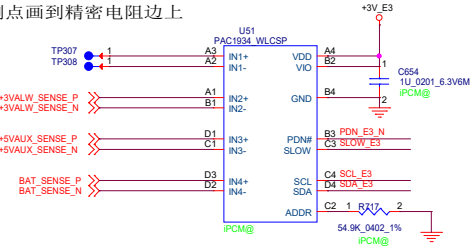


测点画到精密电阻边上

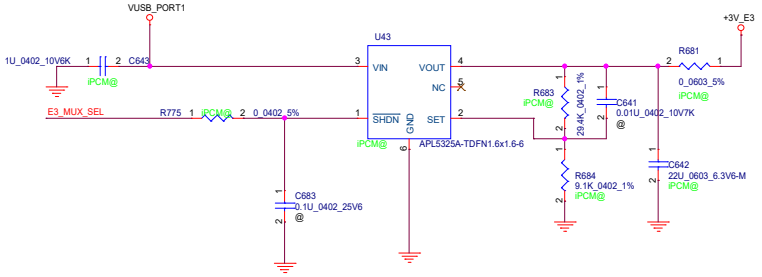


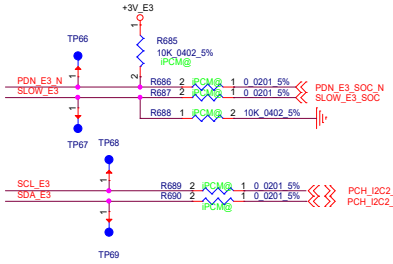
测点画到精密电阻边上

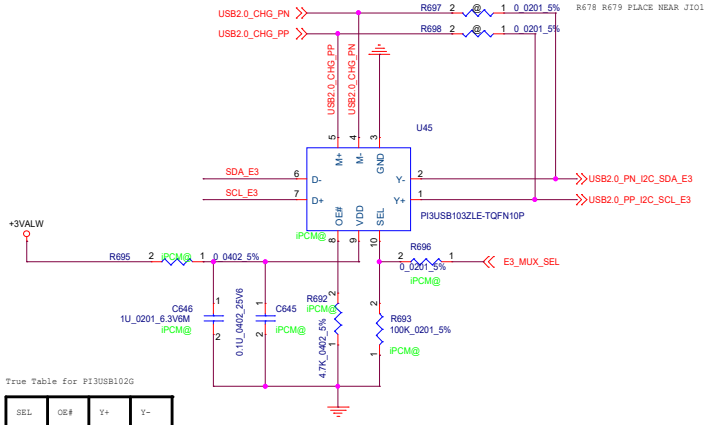


ADDR电阻：

0 ohm	0010_000
499 ohm	0010_001
806 ohm	0010_010
1.27K ohm	0010_011
2.05k ohm	0010_100
3.24k ohm	0010_101
5.23k ohm	0010_110
8.45k ohm	0010_111
21.5k ohm	0011_001
54.9k ohm	0011_011







True Table for PI3USB102G

SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

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Title: iPCM

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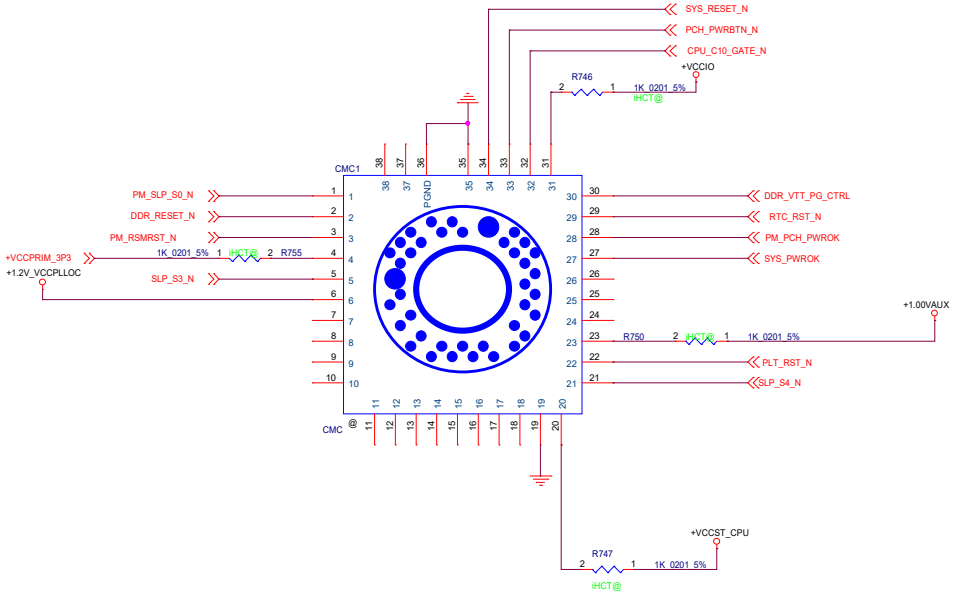

CAD NOTE:
R746,R747,R748,R749,R750,R751,R752,R753,R754,R755 CLOSE TO POWER SOURCE

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Title: BLANK

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Title

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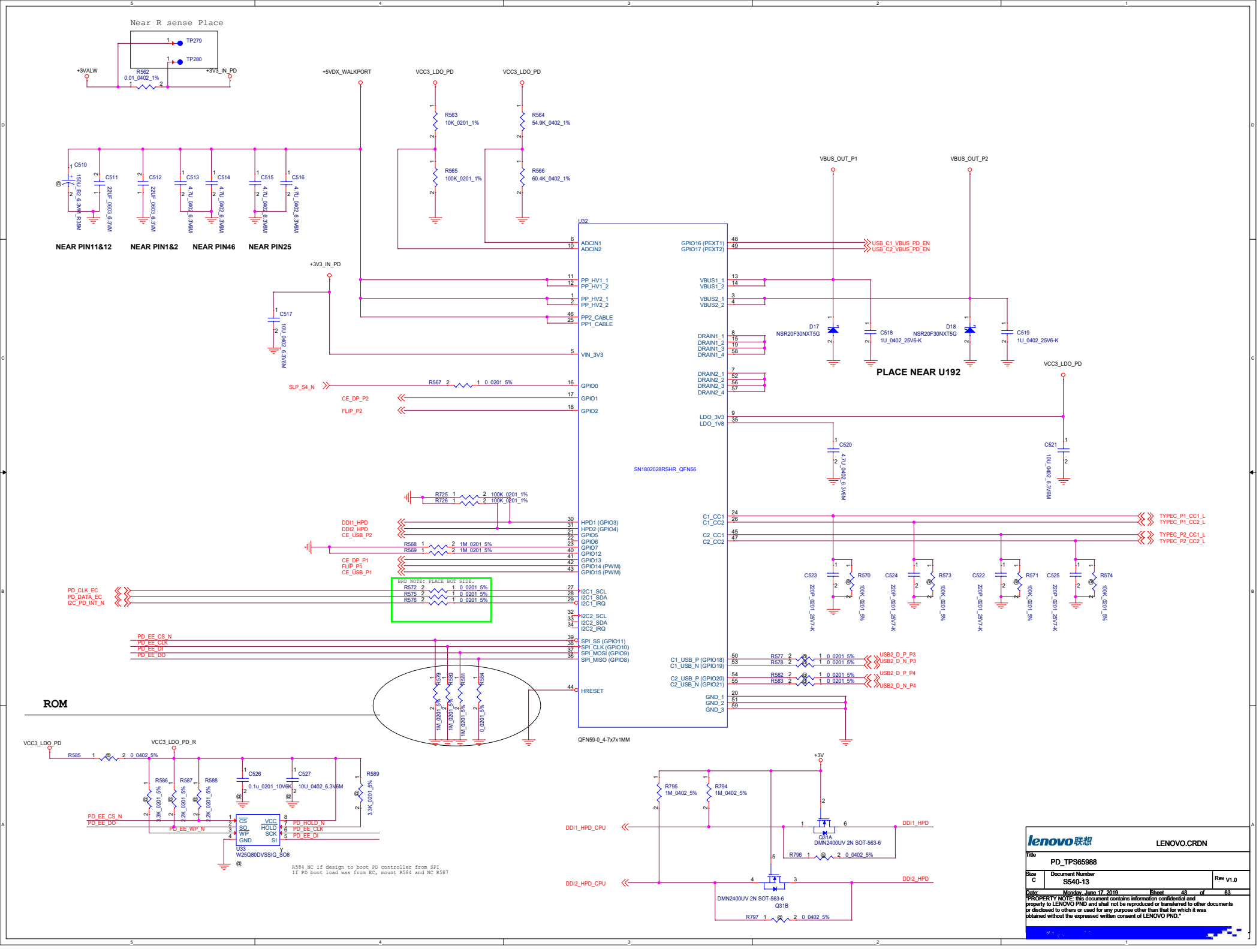
Near R sense Place
TP279
TP280
+3VALW
R562
0.01_0402_1%
+3V3_IN_PD
+5VDX_WALKPORT
VCC3_LDO_PD
VCC3_LDO_PD
R563
10K_0201_1%
R564
54.9K_0402_1%
R565
100K_0201_1%
R566
60.4K_0402_1%
C510
150U_B2_6.3VM_R39M
C511
22UF_0603_6.3VM
C512
22UF_0603_6.3VM
C513
4.7U_0402_6.3V6M
C514
4.7U_0402_6.3V6M
C515
4.7U_0402_6.3V6M
C516
4.7U_0402_6.3V6M
NEAR PIN11&12
NEAR PIN1&2
NEAR PIN46
NEAR PIN25
U32
ADCIN1
ADCIN2
PP_HV1_1
PP_HV1_2
PP_HV2_1
PP_HV2_2
PP2_CABLE
PP1_CABLE
VIN_3V3
GPIO0
GPIO1
GPIO2
HPD1 (GPIO3)
HPD2 (GPIO4)
GPIO5
GPIO6
GPIO7
GPIO12
GPIO13
GPIO14 (PWM)
GPIO15 (PWM)
I2C1_SCL
I2C1_SDA
I2C1_IRQ
I2C2_SCL
I2C2_SDA
I2C2_IRQ
SPI_SS (GPIO11)
SPI_CLK (GPIO10)
SPI_MOSI (GPIO9)
SPI_MISO (GPIO8)
HRESET
GPIO16 (PEXT1)
GPIO17 (PEXT2)
VBUS1_1
VBUS1_2
VBUS2_1
VBUS2_2
DRAIN1_1
DRAIN1_2
DRAIN1_3
DRAIN1_4
DRAIN2_1
DRAIN2_2
DRAIN2_3
DRAIN2_4
LDO_3V3
LDO_1V8
C1_CC1
C1_CC2
C2_CC1
C2_CC2
C1_USB_P (GPIO18)
C1_USB_N (GPIO19)
C2_USB_P (GPIO20)
C2_USB_N (GPIO21)
GND_1
GND_2
GND_3
SN1802028RSHR_QFN56
QFN59-0_4-7x7x1MM
USB_C1_VBUS_PD_EN
USB_C2_VBUS_PD_EN
VBUS_OUT_P1
VBUS_OUT_P2
D17
NSR20F30NXT5G
D18
NSR20F30NXT5G
C518
1U_0402_25V6-K
C519
1U_0402_25V6-K
PLACE NEAR U192
C520
4.7U_0402_6.3V6M
C521
10U_0402_6.3V6M
TYPEC_P1_CC1_L
TYPEC_P1_CC2_L
TYPEC_P2_CC1_L
TYPEC_P2_CC2_L
C523
220P_0201_25V7-K
R570
100K_0201_5%
C524
220P_0201_25V7-K
R573
100K_0201_5%
C522
220P_0201_25V7-K
R571
100K_0201_5%
C525
220P_0201_25V7-K
R574
100K_0201_5%
USB2_D_P_P3
USB2_D_N_P3
USB2_D_P_P4
USB2_D_N_P4
SLP_S4_N
CE_DP_P2
FLIP_P2
DDI1_HPD
DDI2_HPD
CE_USB_P2
CE_DP_P1
FLIP_P1
CE_USB_P1
PD_CLK_EC
PD_DATA_EC
I2C_PD_INT_N
PD_EE_CS_N
PD_EE_CLK
PD_EE_DI
PD_EE_DO
BRD NOTE: PLACE BOT SIDE.
ROM
VCC3_LDO_PD
VCC3_LDO_PD_R
R585
0_0402_5%
R586
3.3K_0201_5%
R587
2.2K_0201_5%
R588
2.2K_0201_5%
C526
0.1u_0201_10V6K
C527
10U_0402_6.3V6M
R589
3.3K_0201_5%
U33
W25Q80DVSSIG_SO8
PD_HOLD_N
PD_EE_CLK
PD_EE_DI
PD_EE_WP_N
R584 NC if design to boot PD controller from SPI
If PD boot load was from EC, mount R584 and NC R587
+3V
R795
1M_0402_5%
R794
1M_0402_5%
DDI1_HPD_CPU
DDI2_HPD_CPU
Q31A
DMN2400UV 2N SOT-563-6
Q31B
DMN2400UV 2N SOT-563-6
R796
0_0402_5%
R797
0_0402_5%
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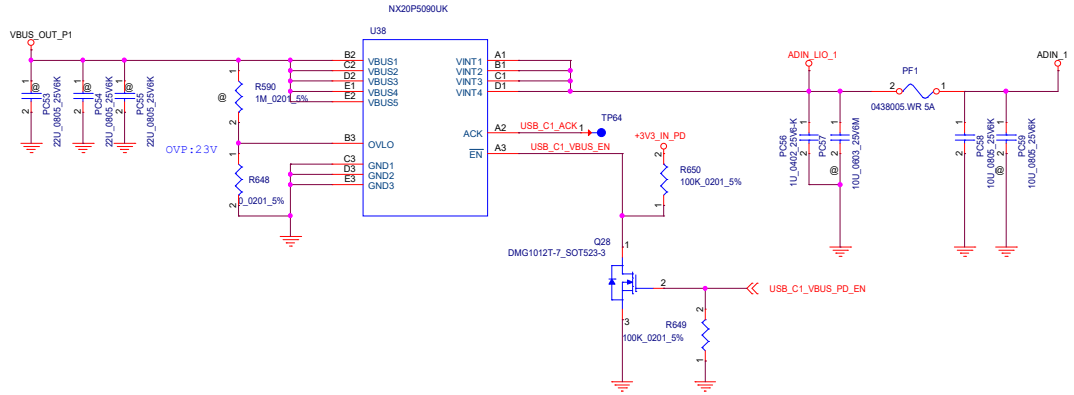
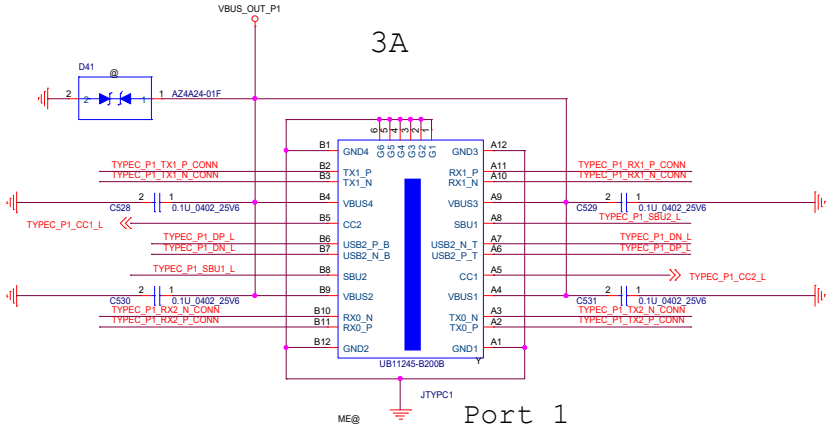
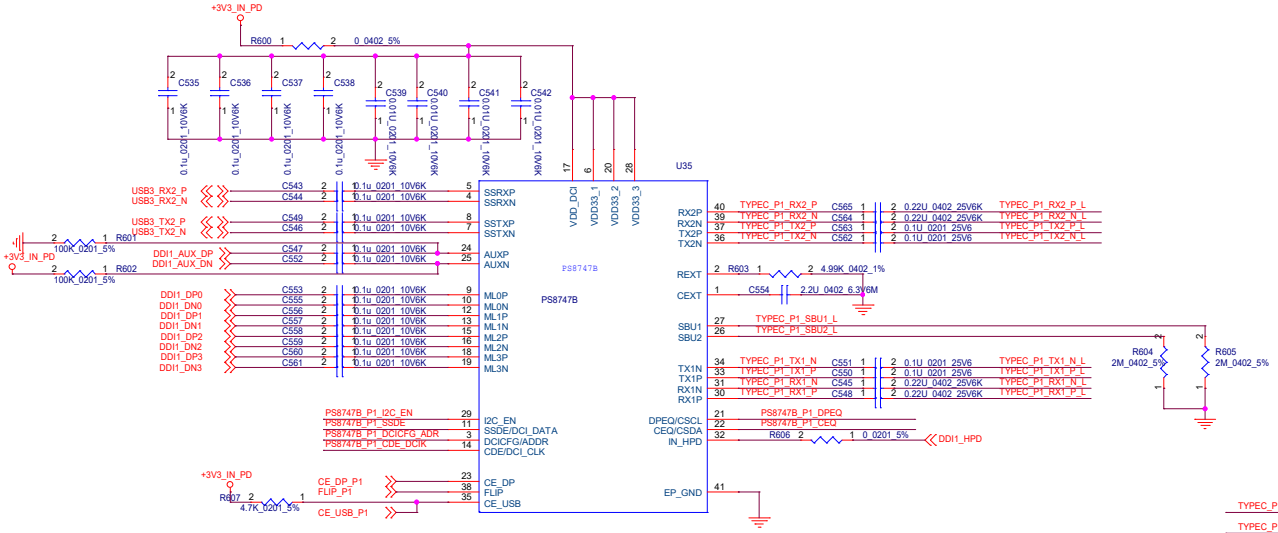
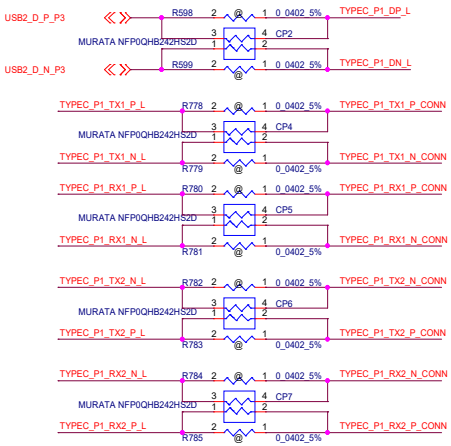
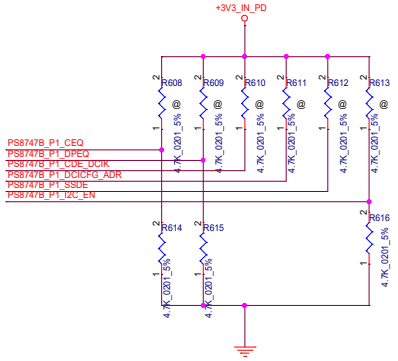
Type C PORT A VBUS SWITCH

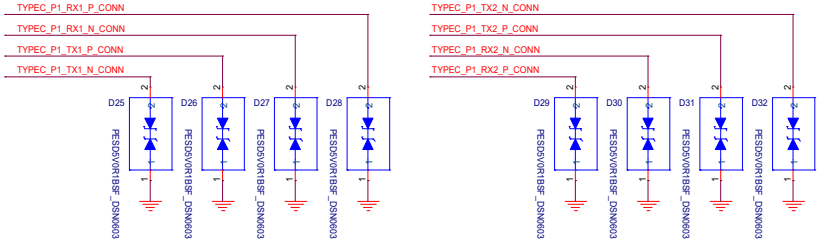


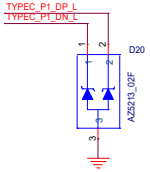


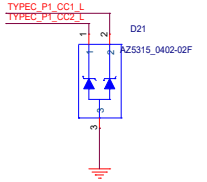


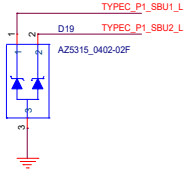












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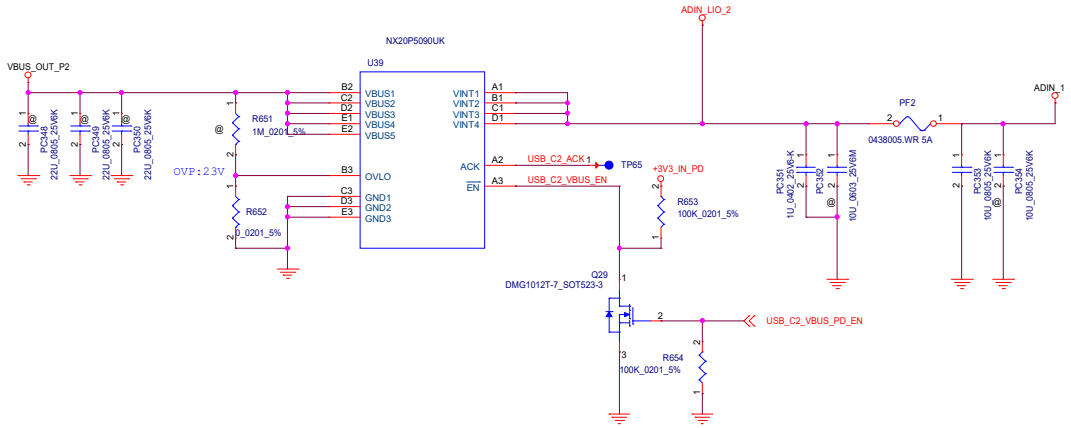
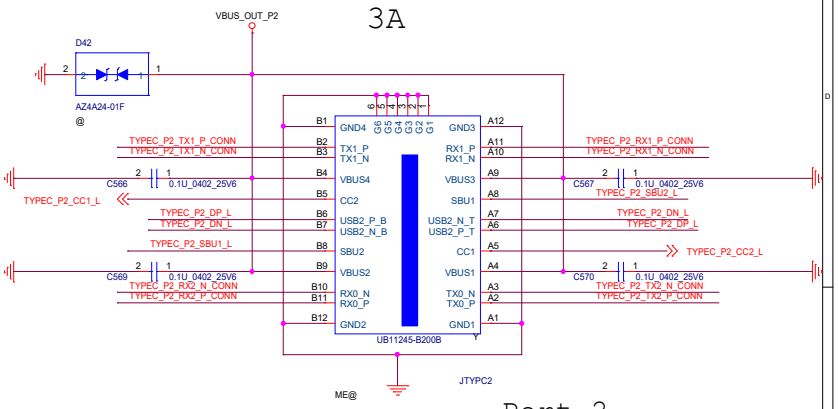
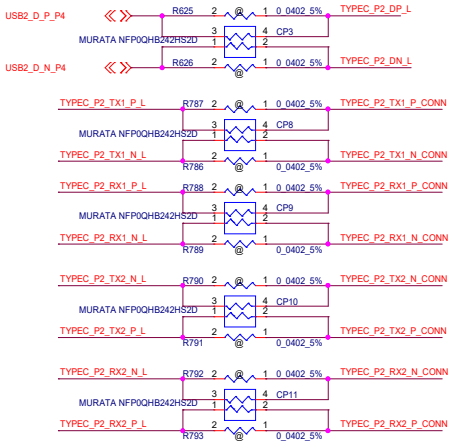
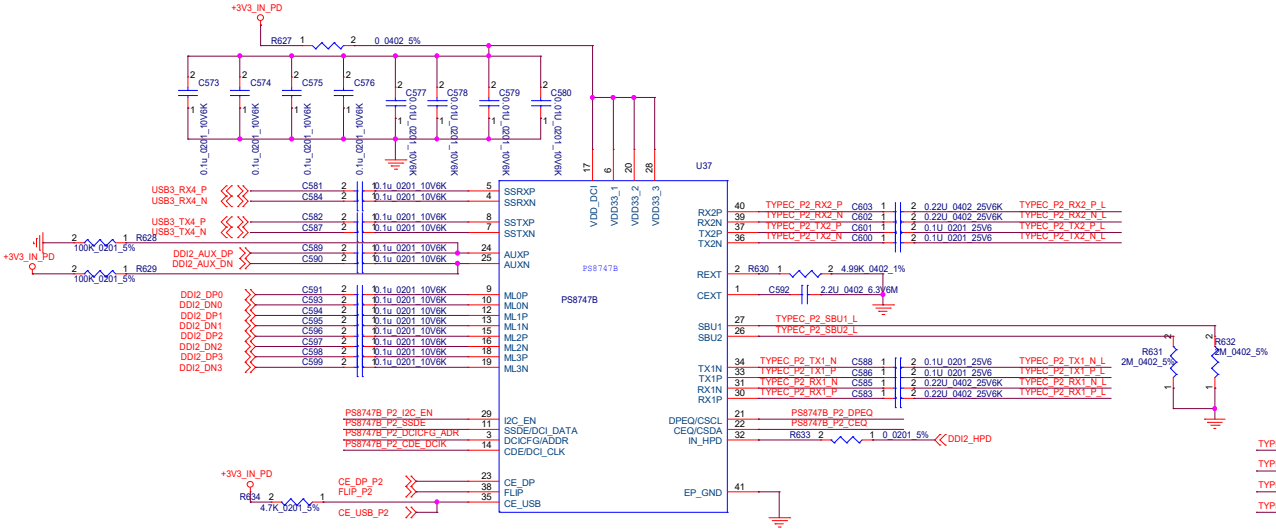
Type C PORT B VBUS SWITCH

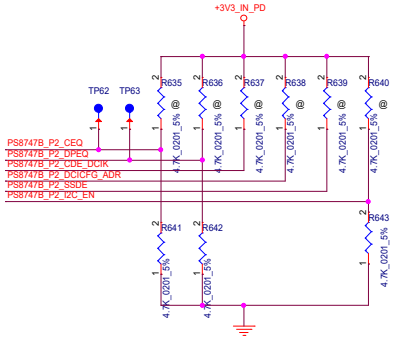


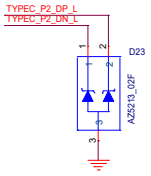


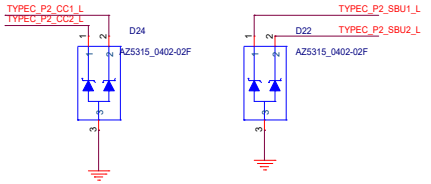
Port 2

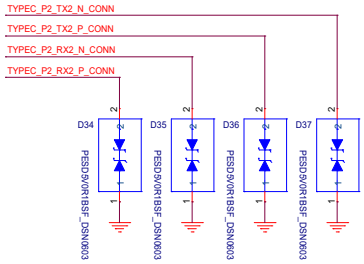


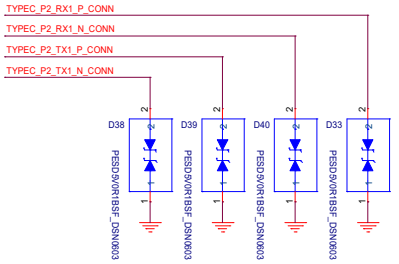












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Title: TYPEC_PORTB		
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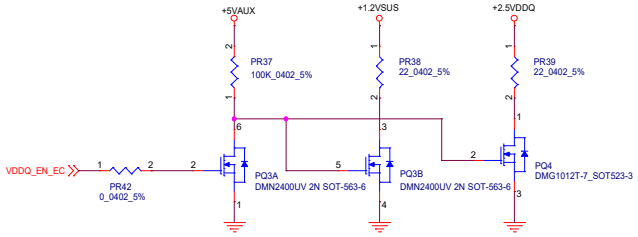

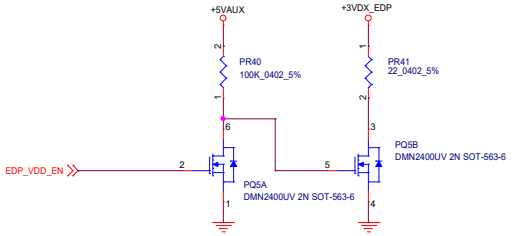

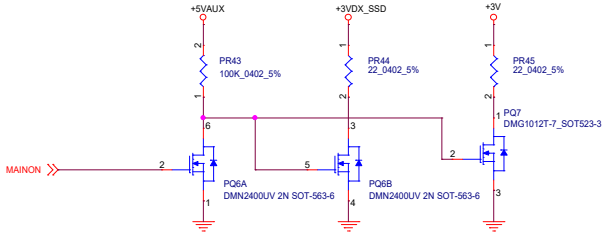

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Title: DISCHARGE

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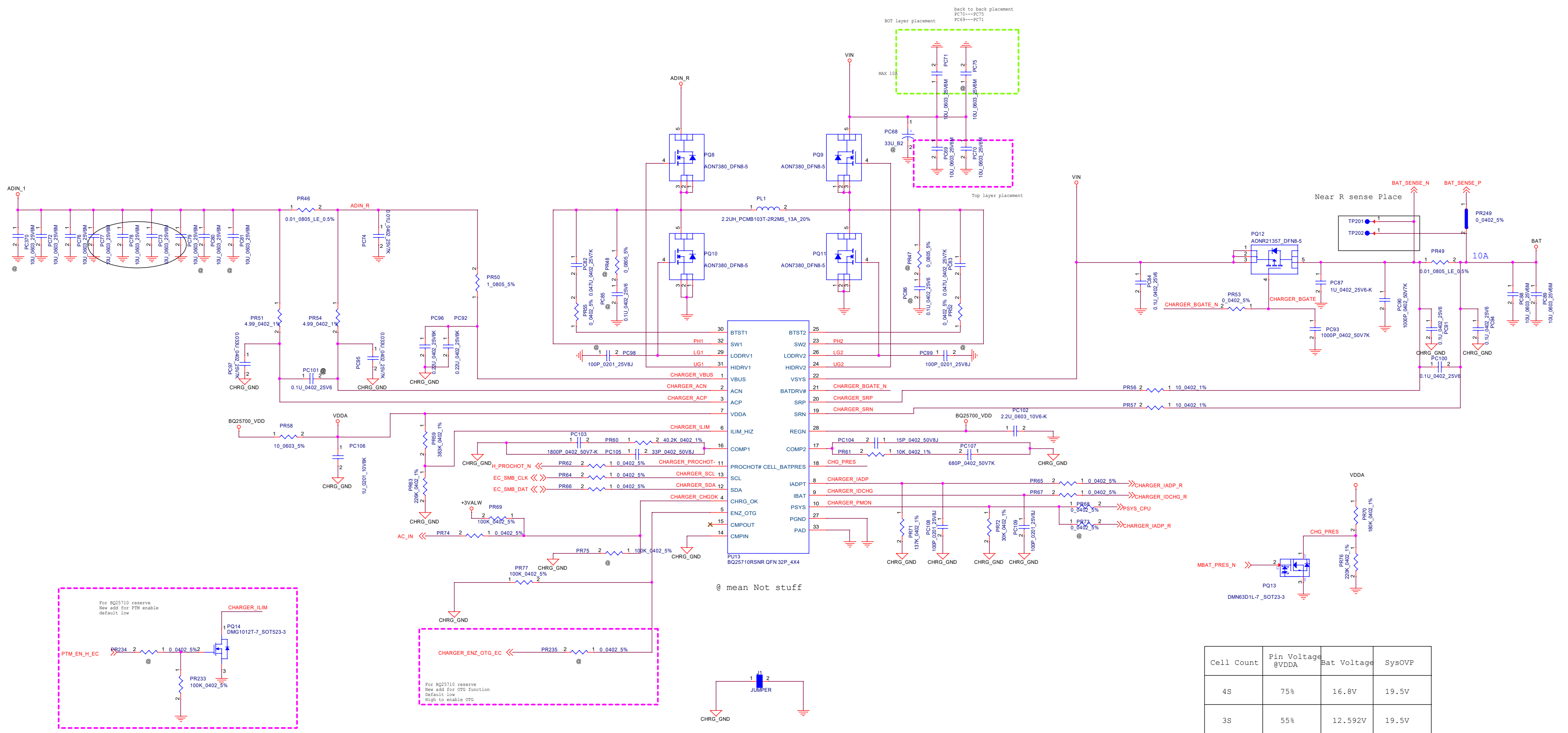

Cell Count	Pin Voltage @VDDA	Bat Voltage	SysOVP
4S	75%	16.8V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.4V	12V
1S	25%	4.192V	5V

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Title: NVDC CHARGER

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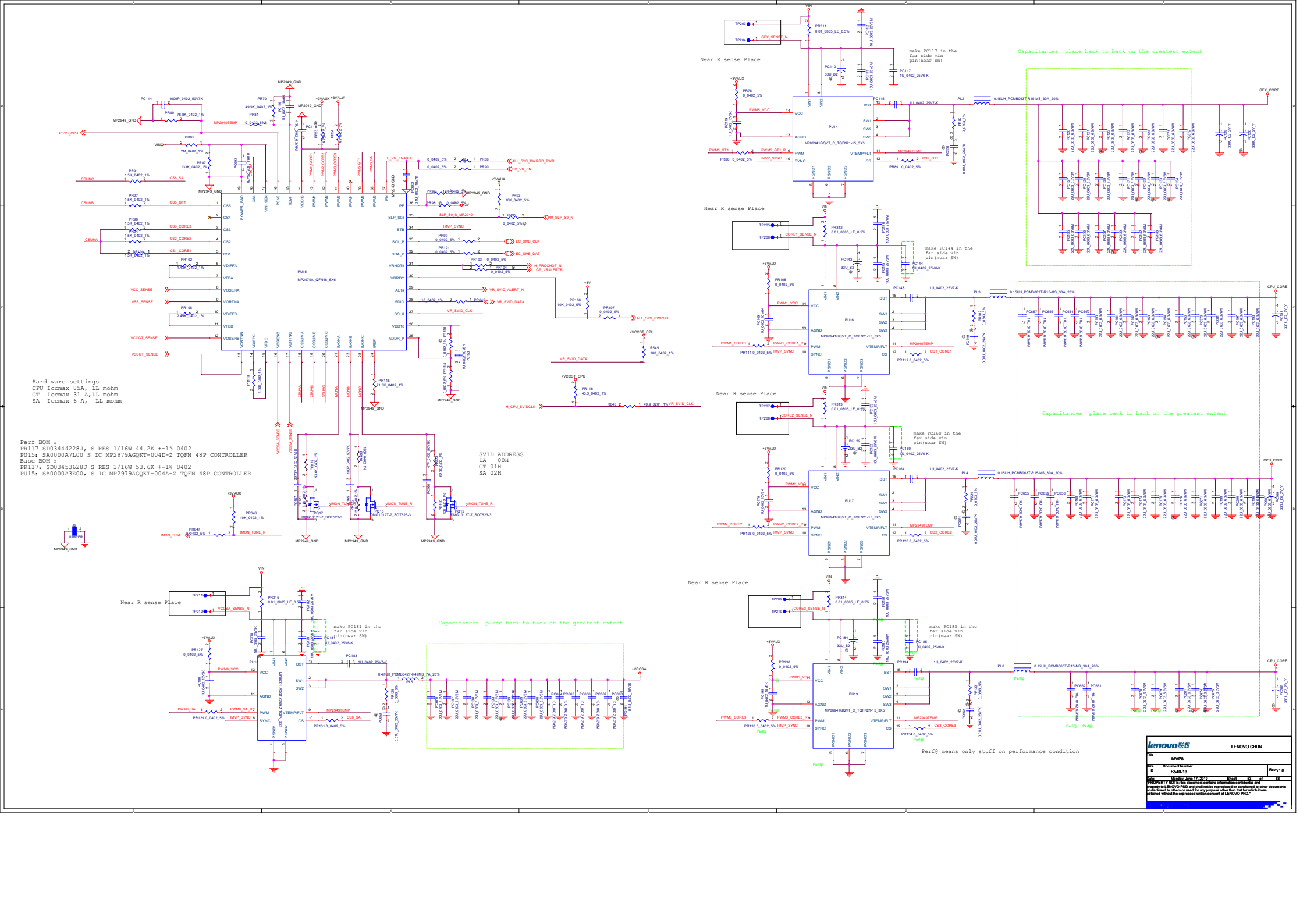
Hard ware settings
CPU Iccmax 85A, LL mohm
GT Iccmax 31 A,LL mohm
SA Iccmax 6 A, LL mohm
Perf BOM :
PR117 SD03444228J, S RES 1/16W 44.2K +-1% 0402
PU15: SA0000A7L00 S IC MP2979AGQKT-004D-Z TQFN 48P CONTROLLER
Base BOM :
PR117: SD03453628J S RES 1/16W 53.6K +-1% 0402
PU15: SA0000A3E00, S IC MP2979AGQKT-004A-Z TQFN 48P CONTROLLER
SVID ADDRESS
IA 00H
GT 01H
SA 02H
Near R sense Place
make PC117 in the far side vin pin(near SW)
make PC144 in the far side vin pin(near SW)
make PC160 in the far side vin pin(near SW)
make PC181 in the far side vin pin(near SW)
make PC185 in the far side vin pin(near SW)
Capacitances place back to back on the greatest extent
Perf@ means only stuff on performance condition
MP2949_GND
+3VAUX
+3VALW
VIN
GFX_CORE
CPU_CORE
LENOVO.CRDN
IMVP8
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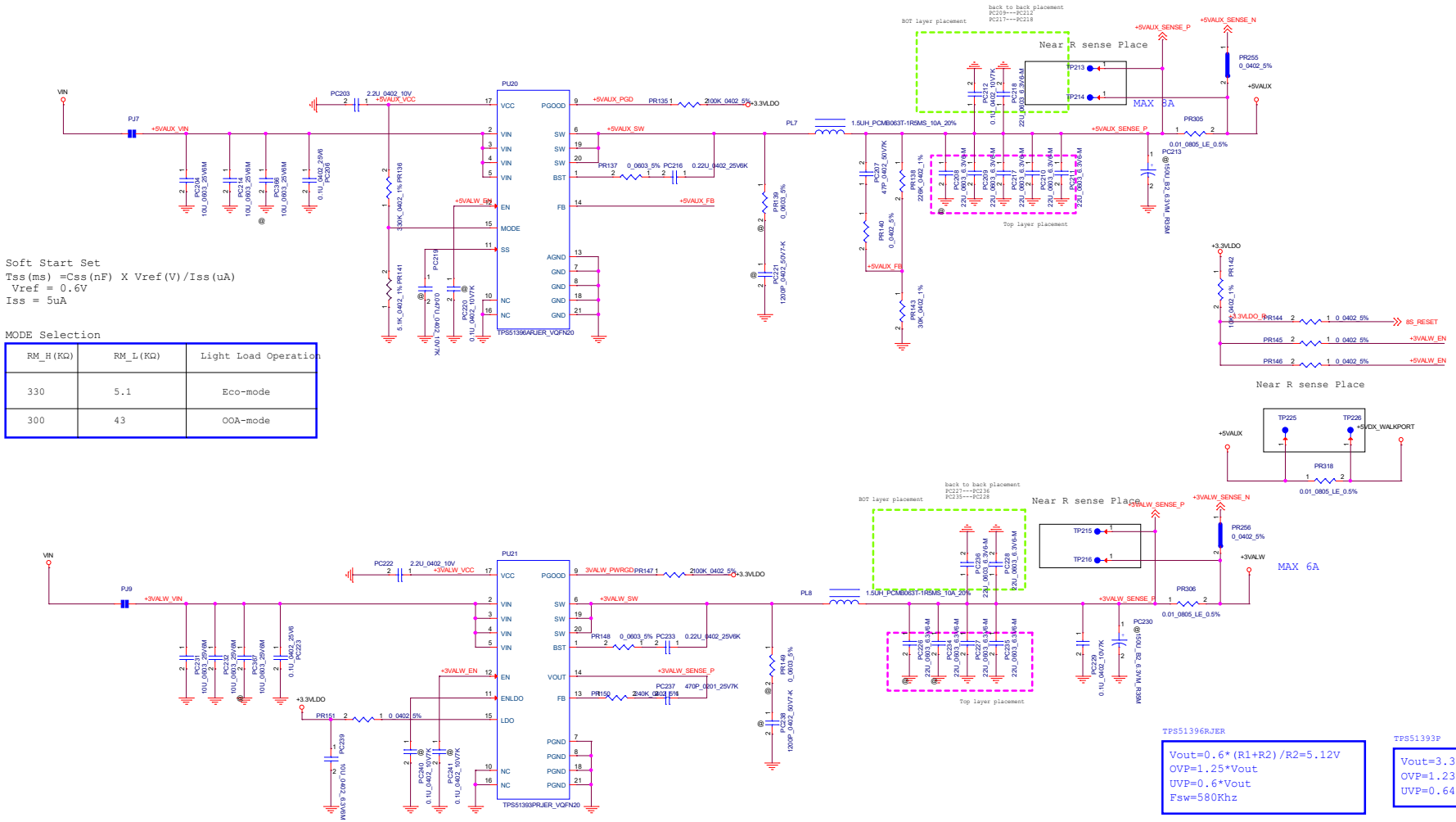

lenovo联想	LENOVO.CRDN	
Title	+3VALW/+5VAUX	
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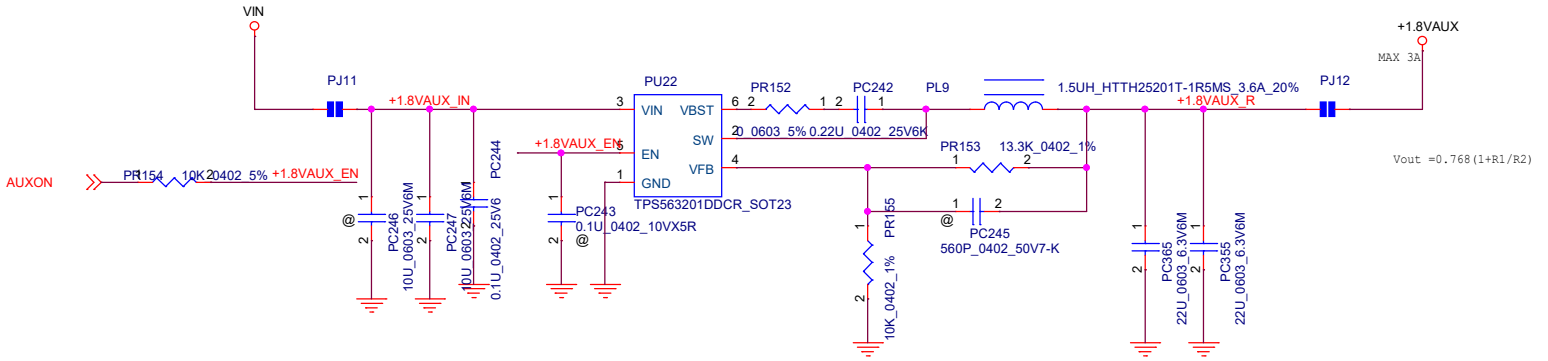
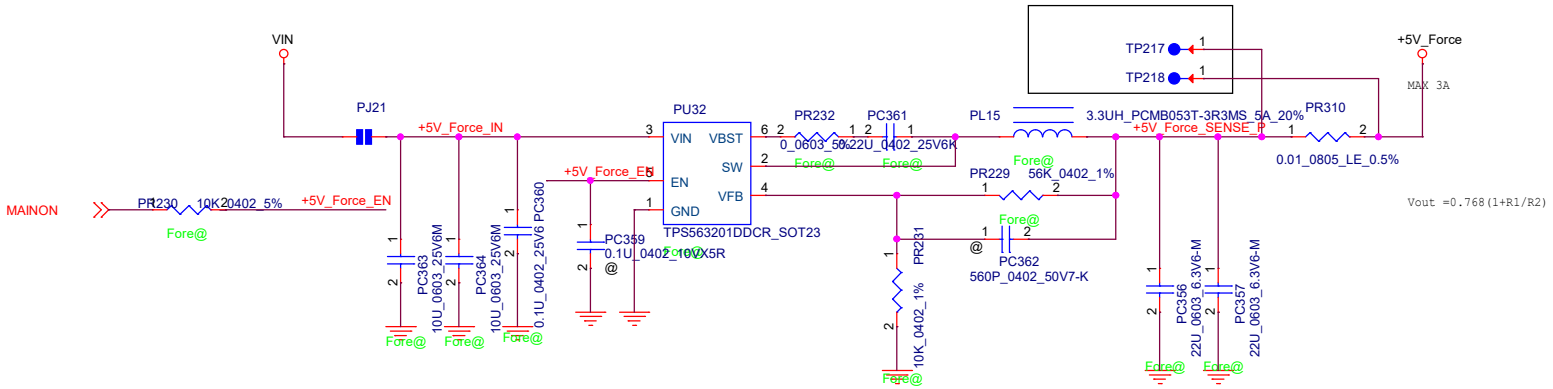


Near R sense Place



Option For Foretouch function
Force@ Only Stuff On forcetouch Existence

lenovo联想	LENOVO.CRDN	
Title: P55--PWR_+1.8VAUX/+5V_Force		
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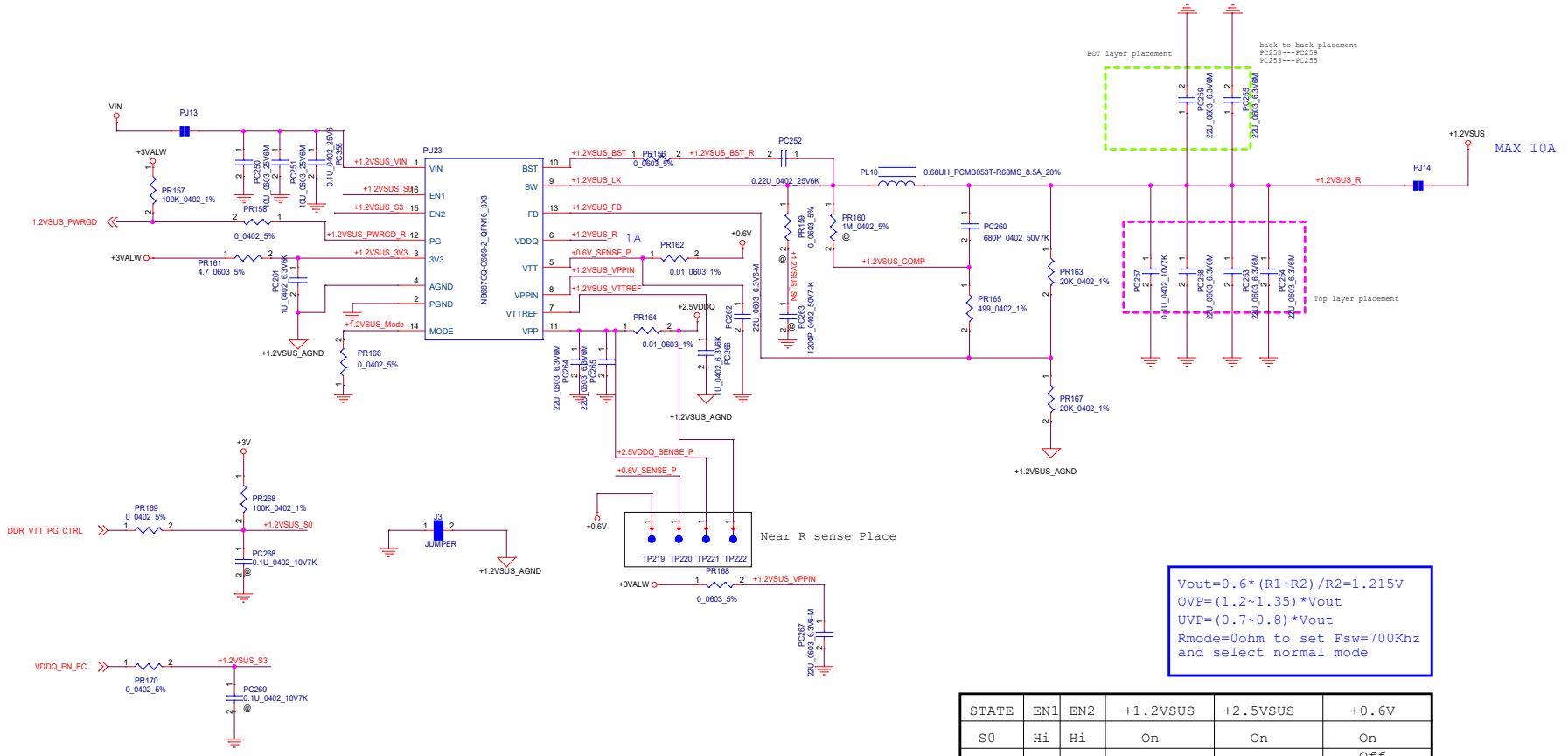

Vout=0.6*(R1+R2)/R2=1.215V
OVP=(1.2~1.35)*Vout
UVP=(0.7~0.8)*Vout
Rmode=0ohm to set Fsw=700Khz and select normal mode

STATE	EN1	EN2	+1.2VSUS	+2.5VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					

lenovo联想 LENOVO.CRDN

Title: +1.2VSUS/+0.6V

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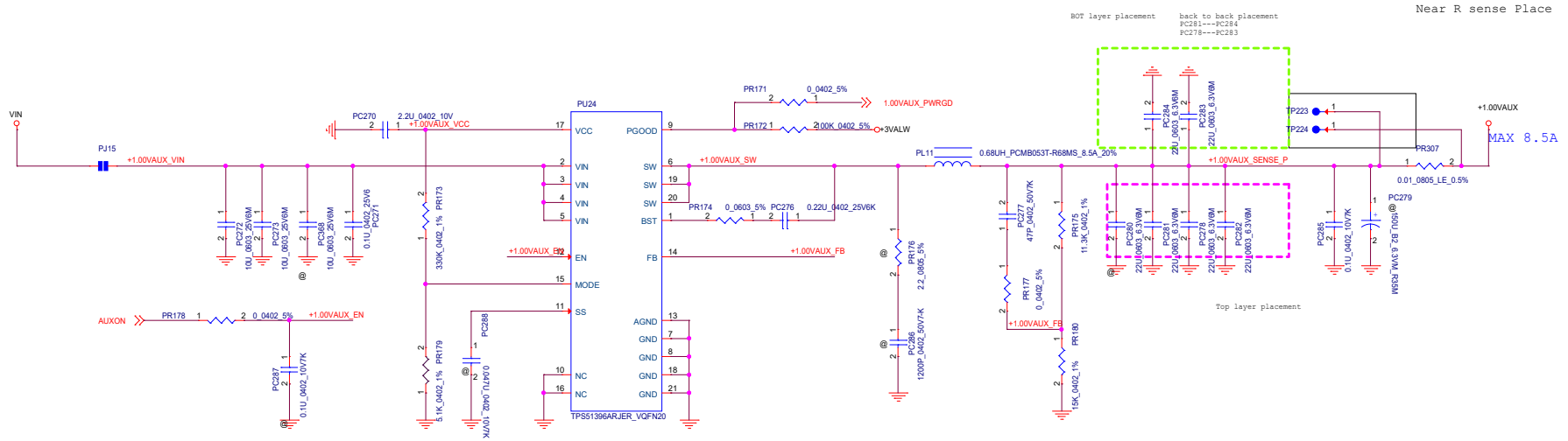

Soft Start Set

Tss(ms) =Css(nF) X Vref(V)/Iss(uA)

Vref = 0.6V

Iss = 5uA

MODE Selection

RM_H(KΩ)	RM_L(KΩ)	Light Load Operation
330	5.1	Eco-mode
300	43	OOA-mode

Vout=0.6*(R1+R2)/R2=1.052V

OVP=1.25*Vout

UVP=0.6*Vout

Fsw=580Khz

lenovo联想 LENOVO.CRDN

Title: PWR_+1.00VAUX

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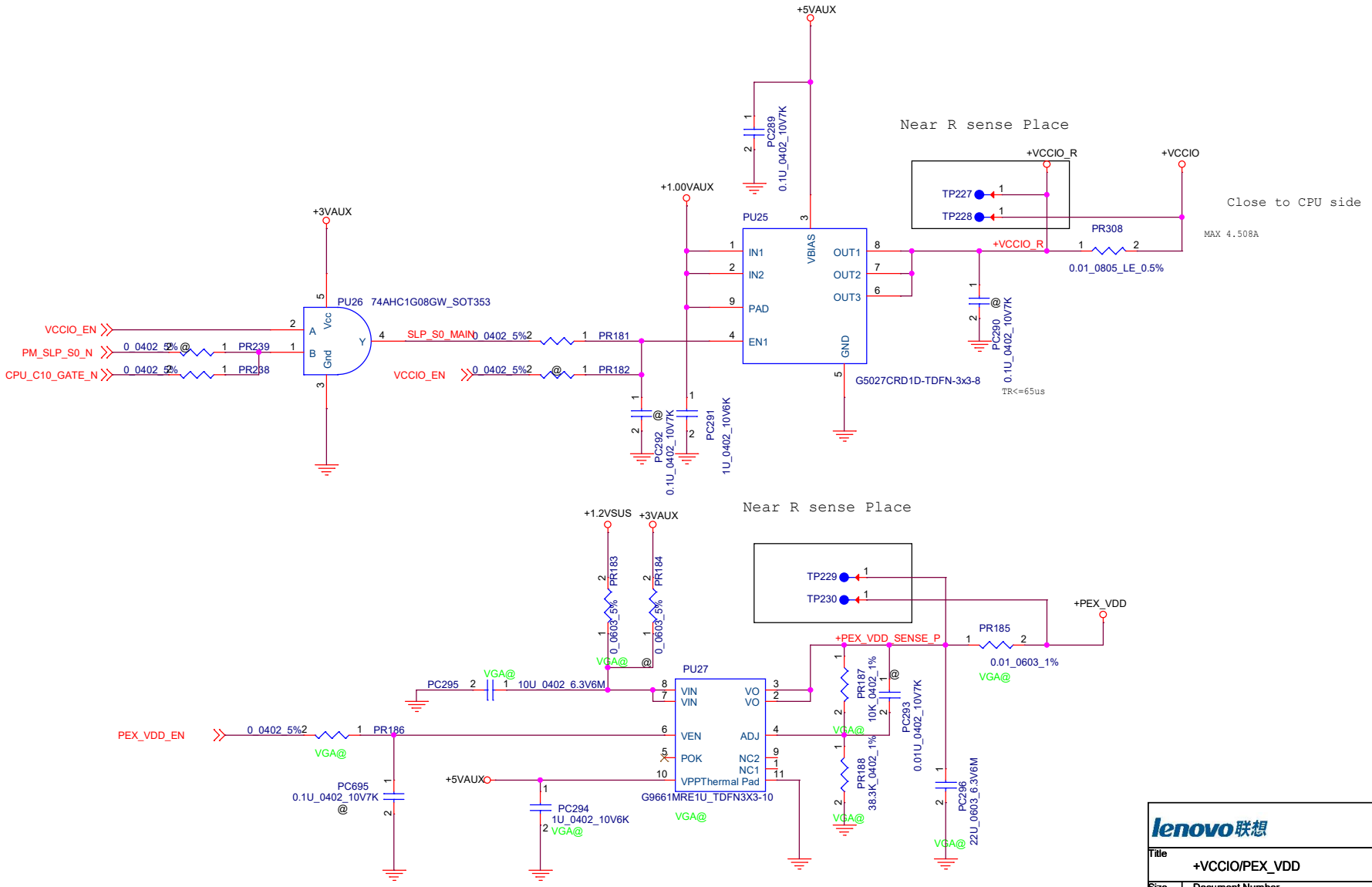

lenovo联想	LENOVO.CRDN	
Title: +VCCIO/PEX_VDD		
Size: B	Document Number: S540-13	Rev: V1.0
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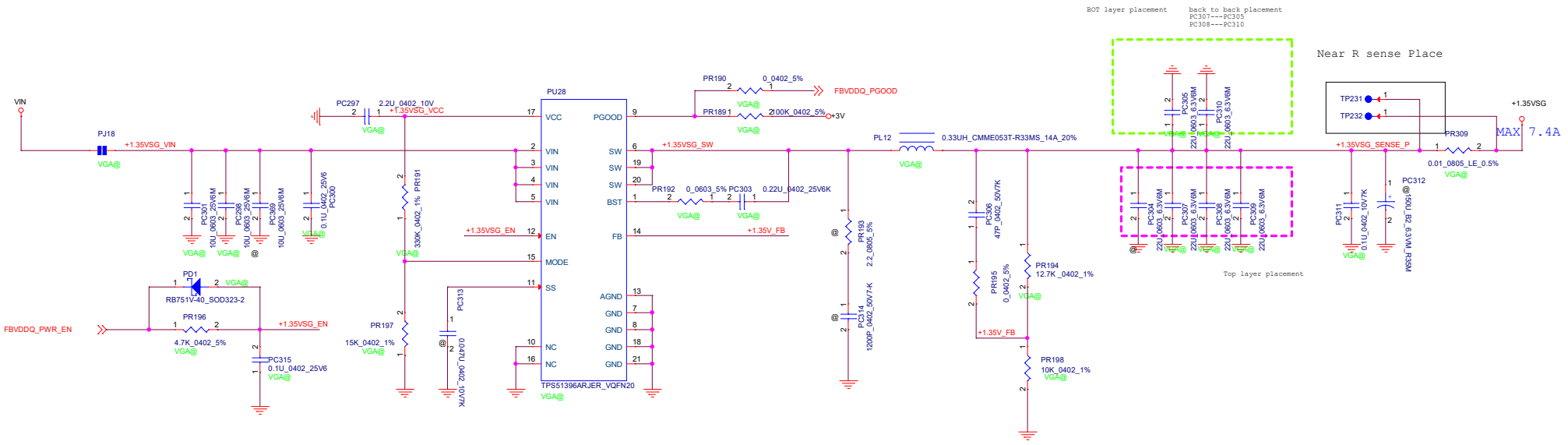

Soft Start Set

Tss(ms) =Css(nF) X Vref(V)/Iss(uA)
Vref = 0.6V
Iss = 5uA

MODE Selection

RM_H(KΩ)	RM_L(KΩ)	Light Load Operation
330	5.1	Eco-mode
300	43	OOA-mode

VGA@ Only Stuff On DGPU Existence

Vout=0.6*(R1+R2)/R2=1.38V
OVP=1.25*Vout
UVP=0.6*Vout
Fsw=580Khz

lenovo联想 LENOVO.CRDN

Title: +1.35VGS

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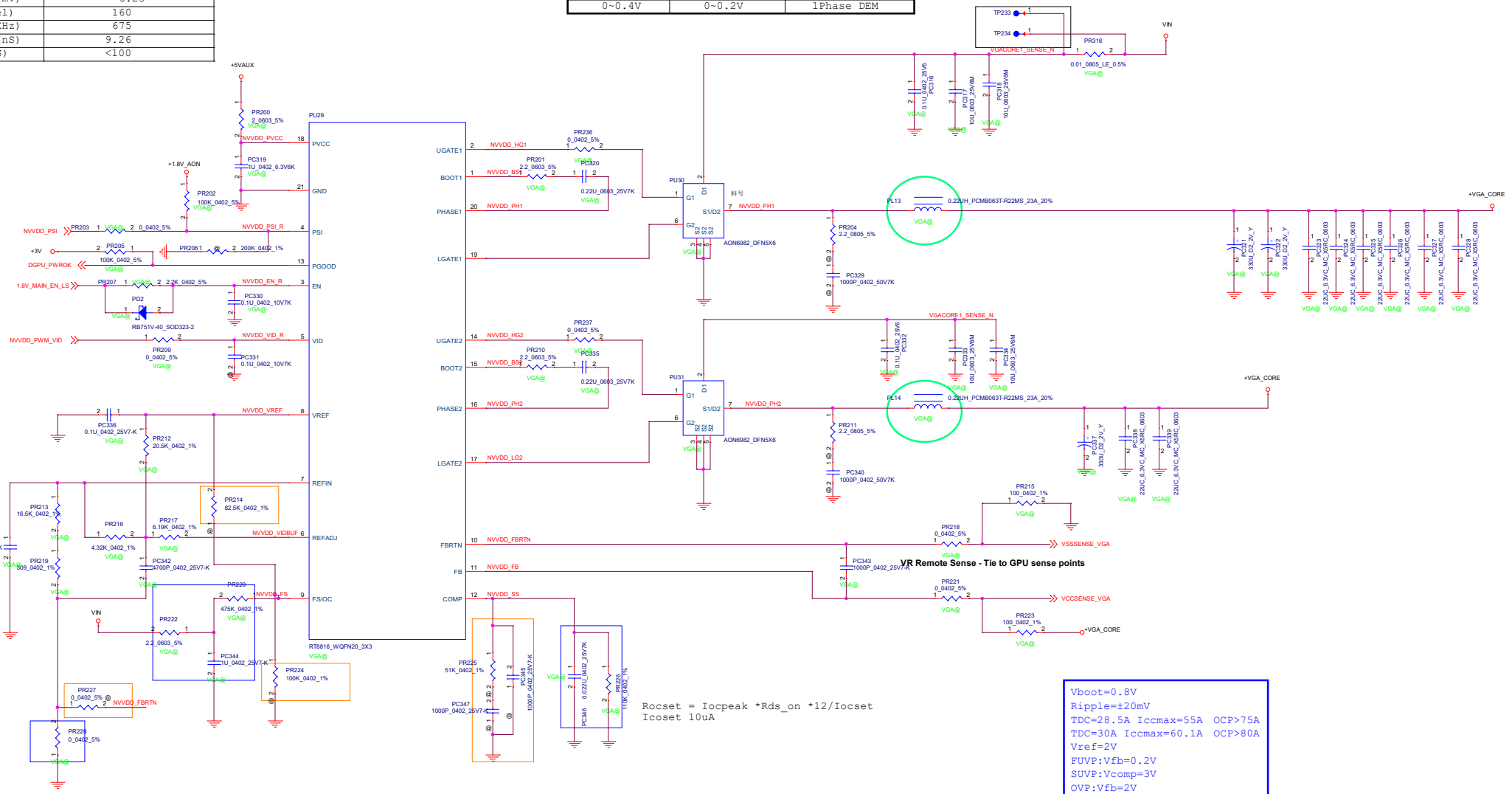
PWM-VID Specification	
	N17 Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

Near R sense Place



lenovo联想	LENOVO.CRDN
Title	+VGA_CORE
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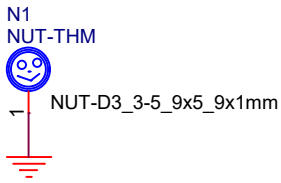

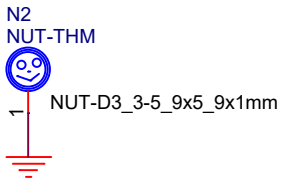

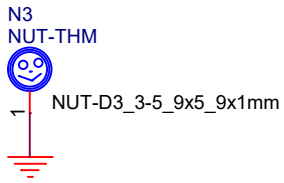

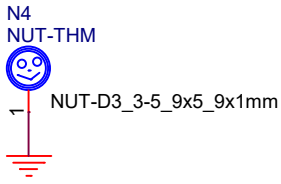

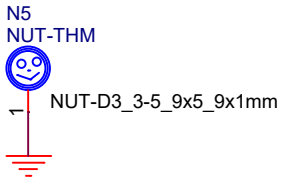

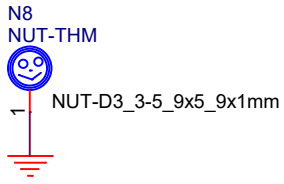

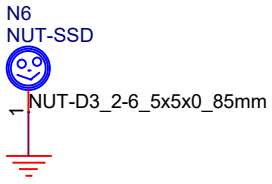

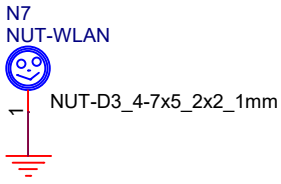

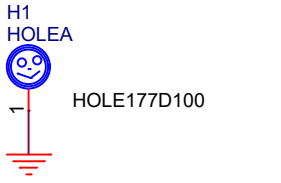

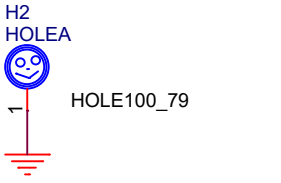

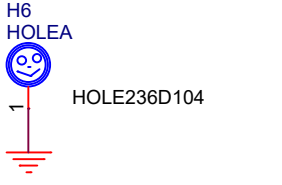

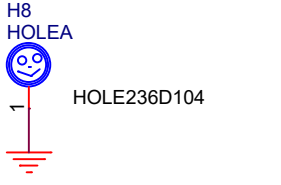

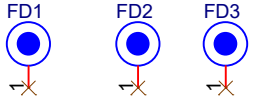

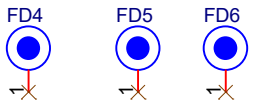

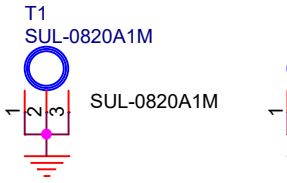

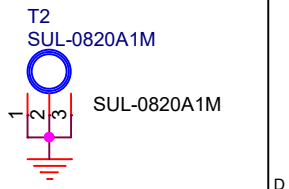

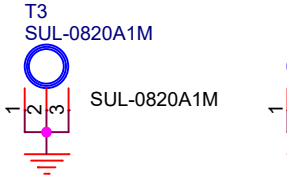

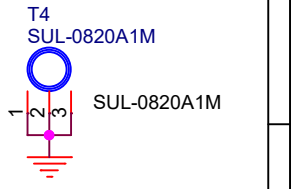

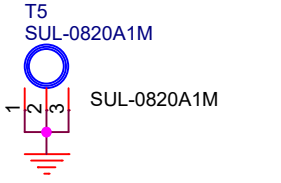

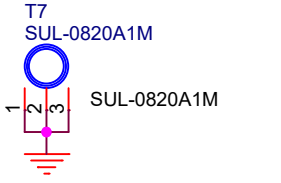

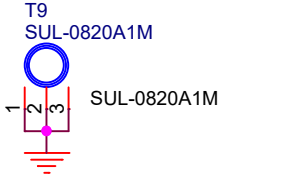

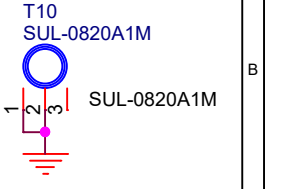

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Title

MOUNTING HOLE/EMI

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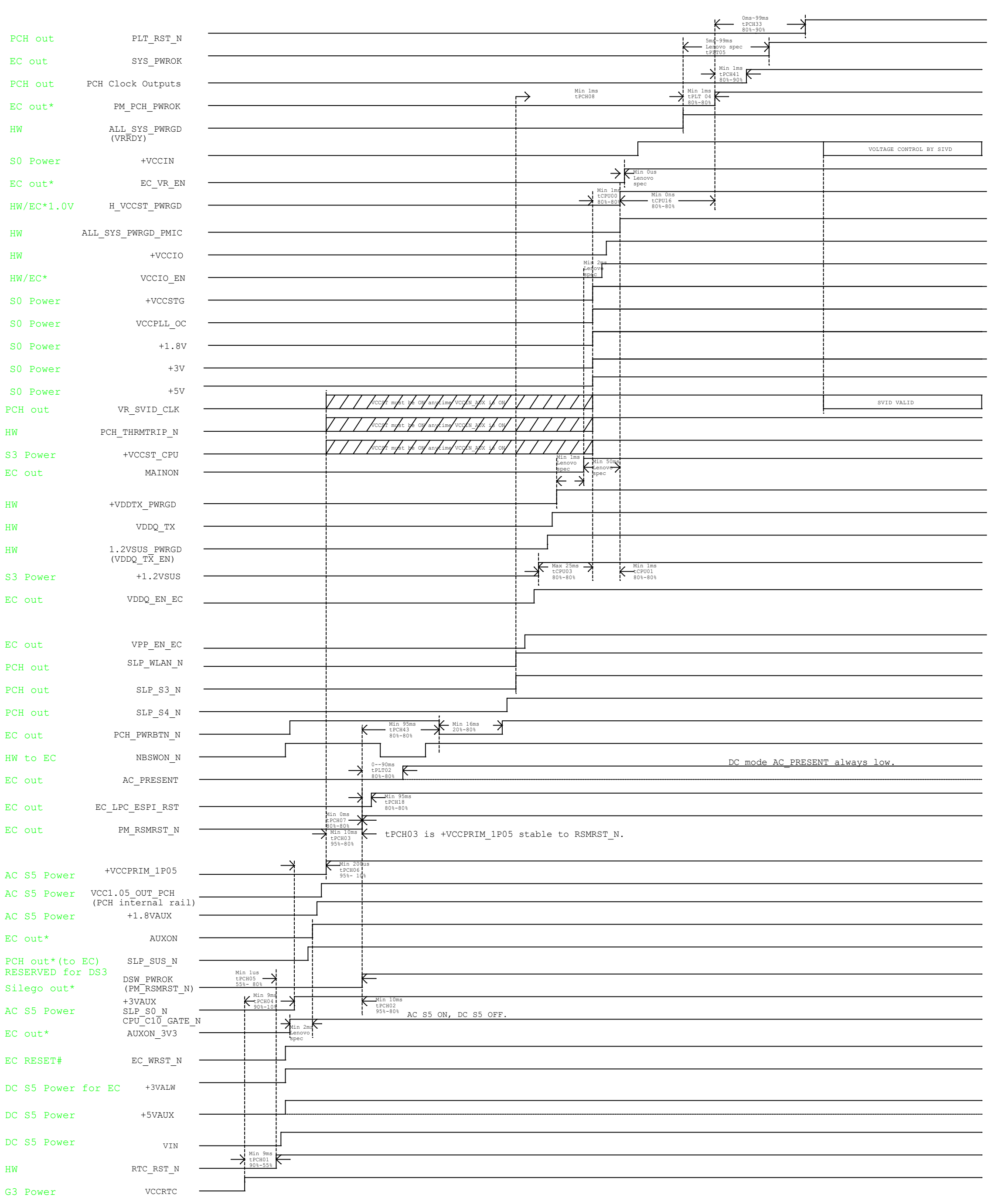
G3 AC/DC mode S5/S4 to S0 (Non Deep Sx)



G3 AC/DC mode S5/S4 to S0 (Non Deep Sx platform)

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CML Power Sequence

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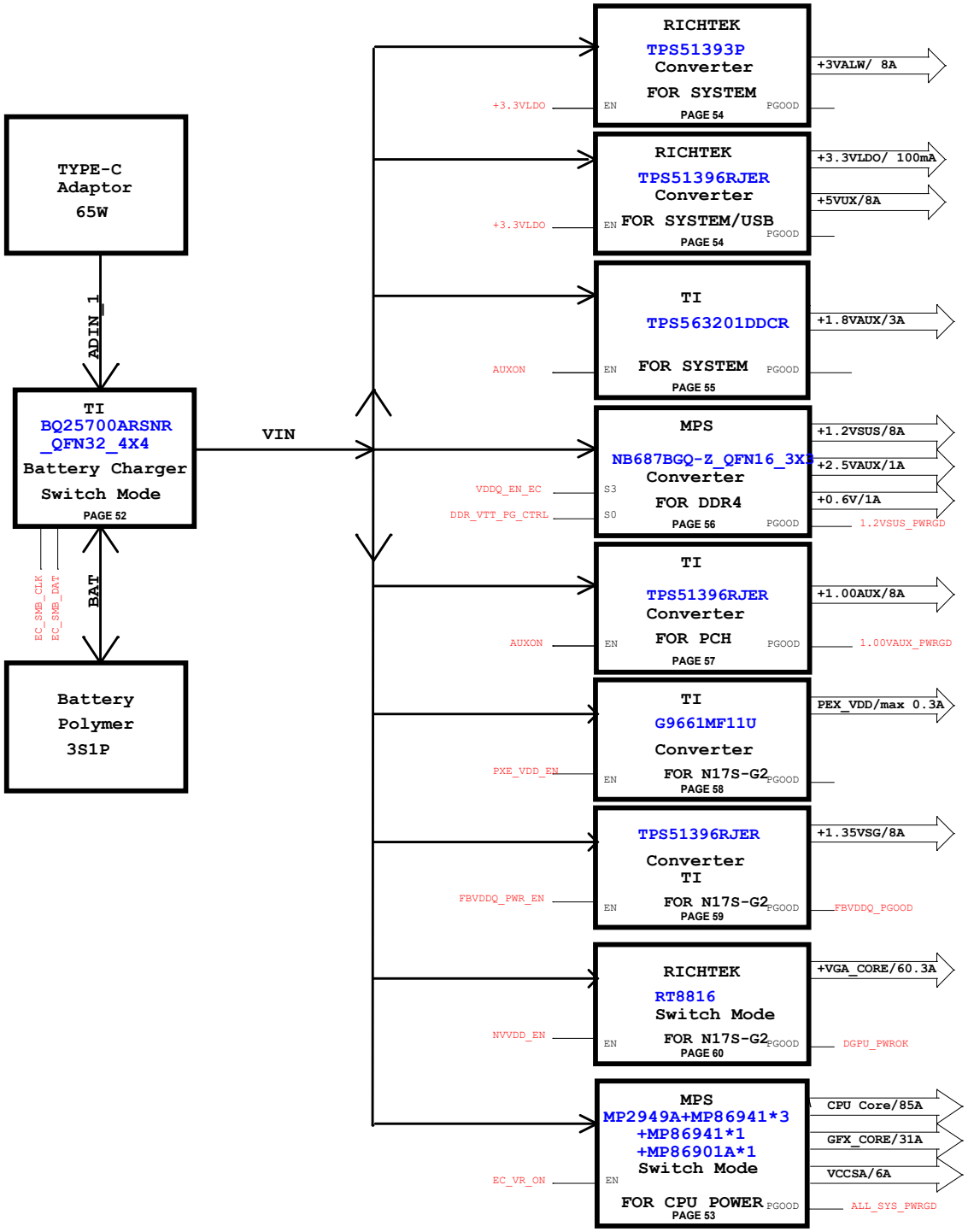

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Title: PWR-Power Diagram

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