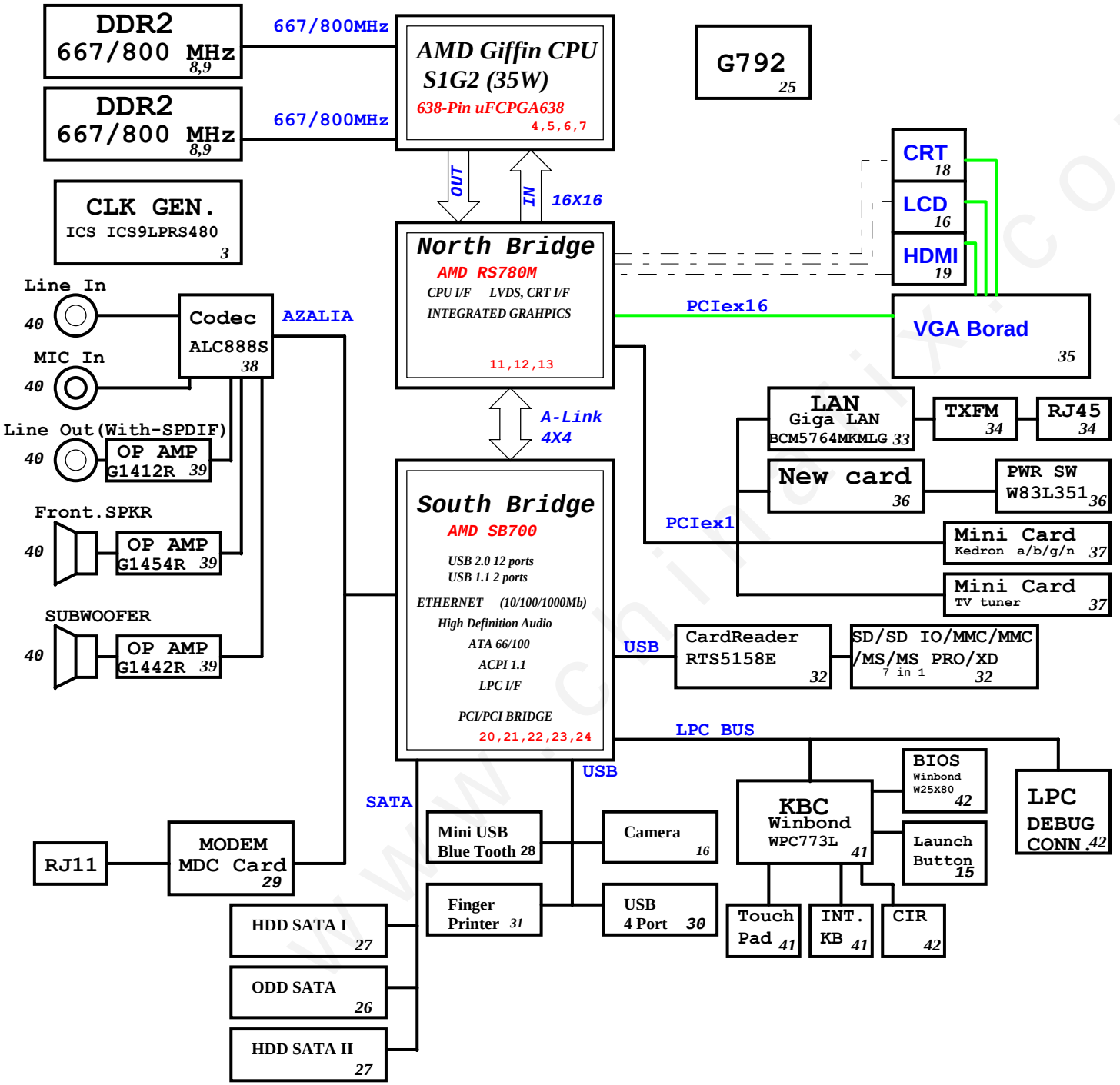
Big Bear 2A (AS 18") Block Diagram

Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 48	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 50	
1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)

RT9166 50	
3D3V_S0	2D5V_S0 (300mA)

G957 50	
3D3V_S0	1D5V_S0(1A)

G9161 50	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731A 51	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Big Bear 2A | Rev: SC
Date: Monday, October 27, 2008 | Sheet 1 of 55

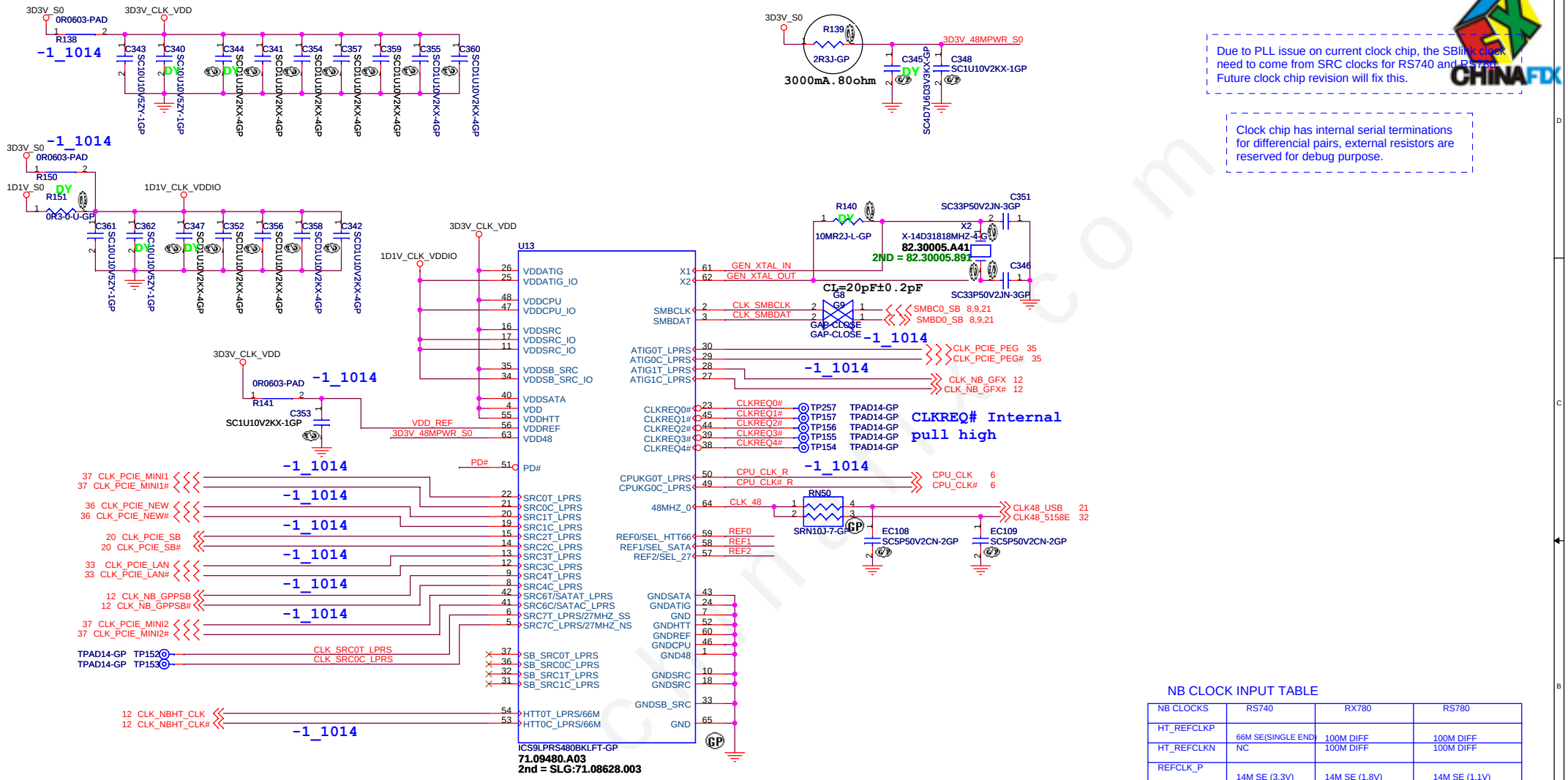
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 2 of 55



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

* default

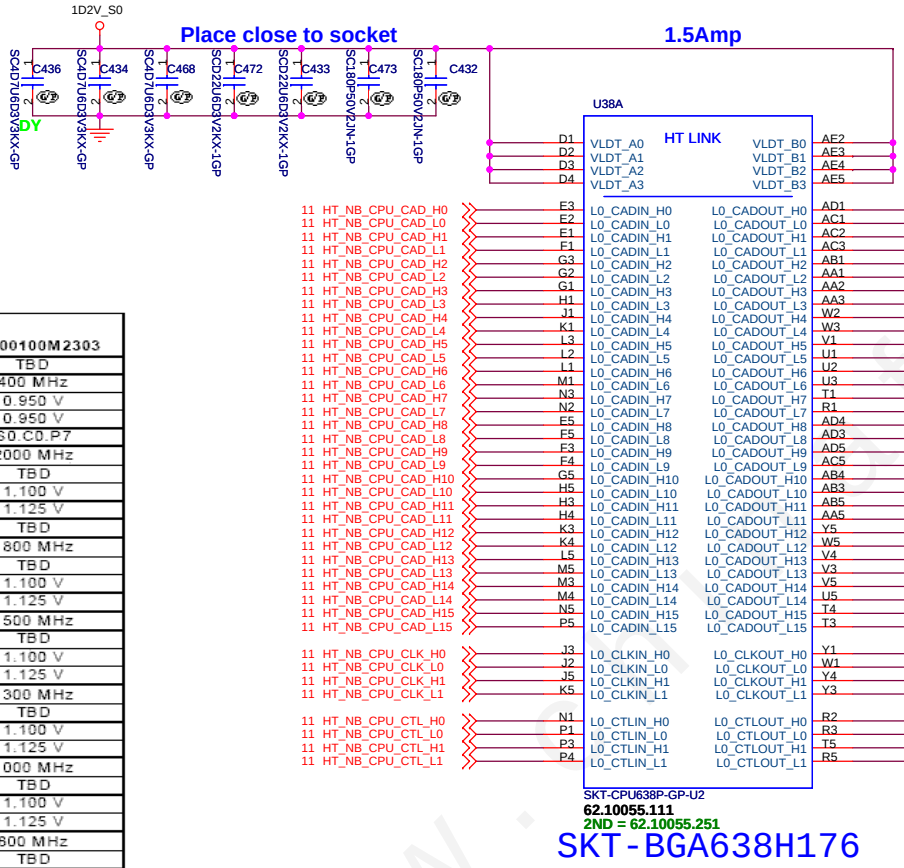
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 3 of 55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

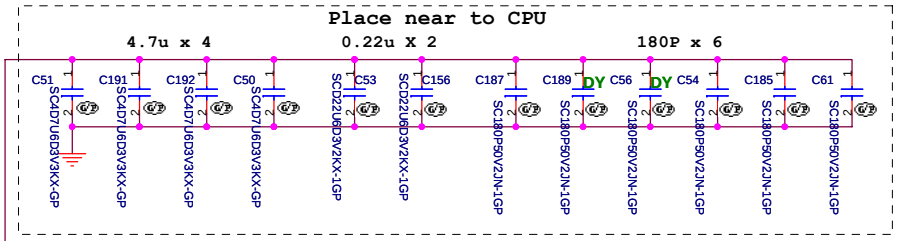
<Core Design>

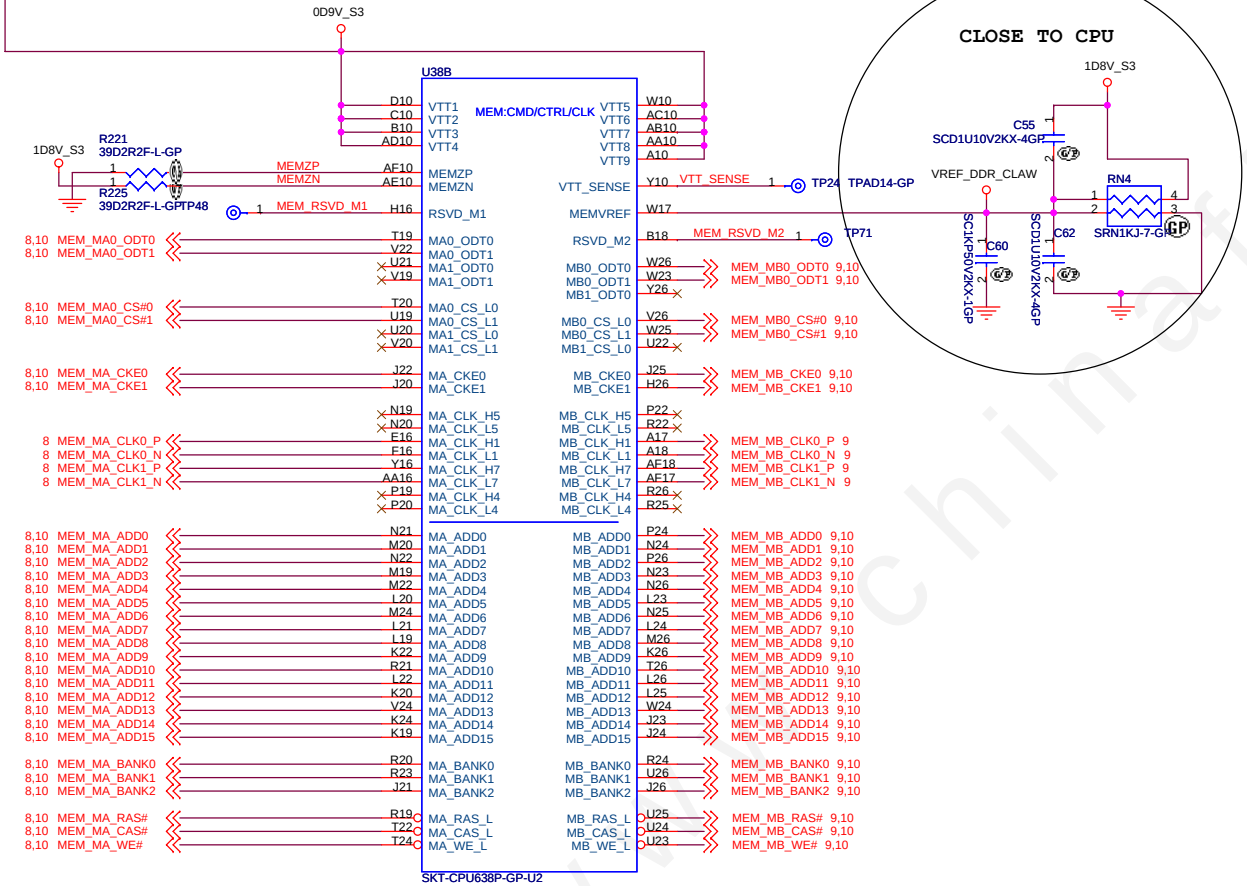
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

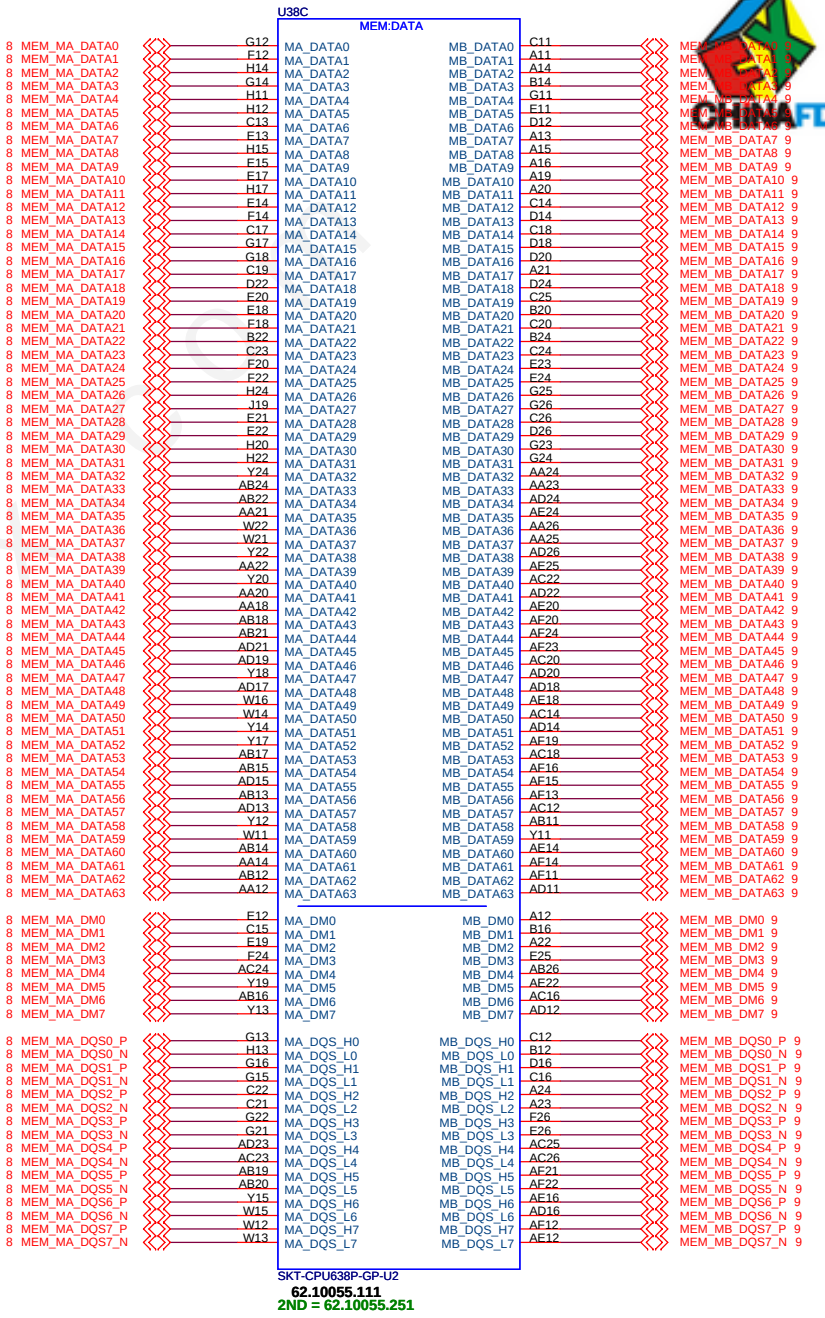
Title: CPU_HT_LINK I/F_(1/4)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 4 of 55







<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CPU_DDR_(2/4)*	
Size A3	Document Number **Big Bear 2A**	Rev SA
Date: Monday, October 27, 2008	Sheet 5 of 55	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active FAN
O=FAN

1D8V_S0
RN31
SRN300J-1-GP
-1_1014
20,53 CPU_LDT_RST# → R257 0R0402-PAD → LDT_RST#_CPU
20,53 CPU_PWRGD → R258 0R0402-PAD → LDT_PWROK
20 CPU_LDT_STOP# → R62 0R0402-PAD → LDT_STP#_CPU 12
12,20 ALLOW_LDTSTOP → R255 0R0402-PAD → CPU_LDT_REQ#_CPU
SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
2D5V_S0 → R55 0R3-0-U-GP → 2D5V_VDDA_S0
C162 DY, C163 SC4D7U6D3V3KX-GP, C153 SC3300P50V2KX-1GP, C164 SC3300P50V2KX-1GP, C161 SCD22U10V3KX-2GP
Cloce To CPU
CPU_CLK / CPU_CLK# → C481, C488 SC3900P50V2KX-2GP → R263 169R2F-GP → CLKCPU_IN / CLKCPU# IN
LDT_RST# CPU
HDT_RST# → R256 0R0402-PAD
For HDT DBG
1D2V_S0 → R48, R49 44D2R2F-GP
46 CPU_VDD0_RUN_FB_H / 46 CPU_VDD0_RUN_FB_L
46 CPU_VDD1_RUN_FB_H / 46 CPU_VDD1_RUN_FB_L
TPAD14-GP TP180 CPU_SIC, TP175 CPU_SID, TP174 CPU_ALERT#
CPU_HTREF0, CPU_HTREF1

U38D
VDDA1, VDDA2
CLKIN_H, CLKIN_L
RESET_L, PWROK, LDTSTOP_L, LDTREQ_L
SIC, SID, ALERT_L
HT_REF0, HT_REF1
VDD0_FB_H, VDD0_FB_L
VDD1_FB_H, VDD1_FB_L
DBRDY, TMS, TCK, TRST_L, TDI
TEST23, TEST18, TEST19, TEST25_H, TEST25_L, TEST21, TEST20, TEST24, TEST22, TEST12, TEST27, TEST9, TEST6
RSVD1, RSVD2, RSVD3, RSVD4, RSVD5
KEY1, KEY2
SVC, SVD
THERMTRIP_L, PROCHOT_L, MEMHOT_L
THERMDC, THERMDA
VDDIO_FB_H, VDDIO_FB_L
VDDNB_FB_H, VDDNB_FB_L
DBREQ_L, TDO
TEST28_H, TEST28_L, TEST17, TEST16, TEST15, TEST14, TEST7, TEST10, TEST8, TEST29_H, TEST29_L
RSVD10, RSVD9, RSVD8, RSVD7, RSVD6
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251

CPU_DBRDY, CPU_TMS, CPU_TCK, CPU_TRST#, CPU_TDI
TP69 CPU_TEST23
CPU_TEST18, CPU_TEST19
TP65 CPU_TEST25_H, TP64 CPU_TEST25_L
CPU_TEST21, TP176 CPU_TEST20, CPU_TEST24, CPU_TEST22, CPU_TEST12, CPU_TEST27
CPU_TEST9 → R254 0R0402-PAD
RN84 SRN300J-1-GP

1D8V_S3
RN30 SRN1KJ-7-GP
A6 CPU_SVC 46, A4 CPU_SVD 46
AF6 THERMTRIP#, AC7 PROCHOT#, AA8 CPU_MEMHOT#
internal pull high 300 ohm
W7 H_THERMDC 25, W8 H_THERMDA 25
DY C58 SC100P50V2JN-3GP
W9 CPU_VDDIO_SUS_FB_H → TP28, Y9 CPU_VDDIO_SUS_FB_L → TP27
H6 CPU_VDDNB_RUN_FB_H 46, G6 CPU_VDDNB_RUN_FB_L 46
E10 CPU_DBREQ#, AE9 CPU_TDO
J7 CPU_TEST28_H → TP52, H8 CPU_TEST28_L → TP54
D7 CPU_TEST17 → TP68, E7 CPU_TEST16 → TP63, F7 CPU_TEST15, C7 CPU_TEST14
C3, K8, C4, C9 CPU_TEST29H → TP184, C8 CPU_TEST29L → TP185
H18, H19, AA7, D5, C5

1D8V_S3
RN65 SRN300J-1-GP
R433 300R2J-4-GP DY
CPU_TEST27, CPU_DBREQ#
-1_1014
R227 0R0402-PAD → PROCHOT#_SB 20

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

-1_1014
46 CPU_PWRGD_SVID_REG → R259 0R0402-PAD → LDT_PWROK
C483 SCD1U16V2ZY-2GP DY
Near CPU PIN

LDT_PWROK → R261 2K2R2J-2-GP → C482 SCD1U16V2ZY-2GP → 1D8V_3DS_Q2
Q21 MMBT3904-4-GP
THERMTRIP# → KBC_THERMTRIP# 25,41
84.T3904.C11
2ND = 84.03904.T11
CPU exceeds to 125℃

CPU_TEST19 → R226 300R2J-4-GP DY
CPU_TEST18 → R45 300R2J-4-GP DY
CPU_TEST14 → R431 300R2J-4-GP DY
CPU_TEST15 → R432 300R2J-4-GP DY

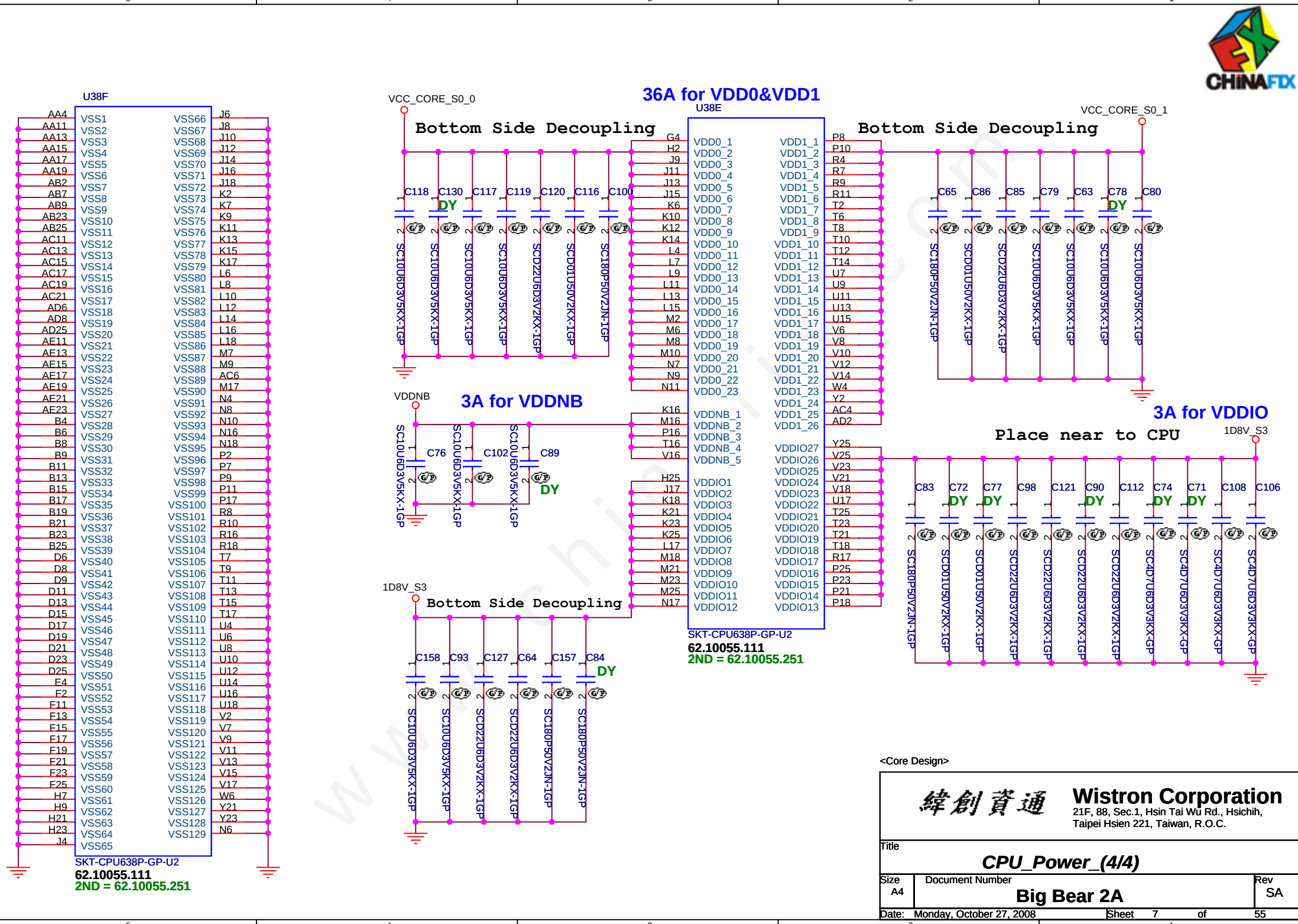
HDT Connectors

CPU_DBREQ#	TP17	TPAD14-GP
CPU_DBRDY	TP50	TPAD14-GP
CPU_TCK	TP21	TPAD14-GP
CPU_TMS	TP23	TPAD14-GP
CPU_TDI	TP20	TPAD14-GP
CPU_TRST#	TP19	TPAD14-GP
CPU_TDO	TP18	TPAD14-GP
1D8V_S3	TP29	TPAD14-GP
HDT_RST#	TP183	TPAD14-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)
Size: A3 | Document Number: Big Bear 2A | Rev: SC
Date: Monday, October 27, 2008 | Sheet 6 of 55

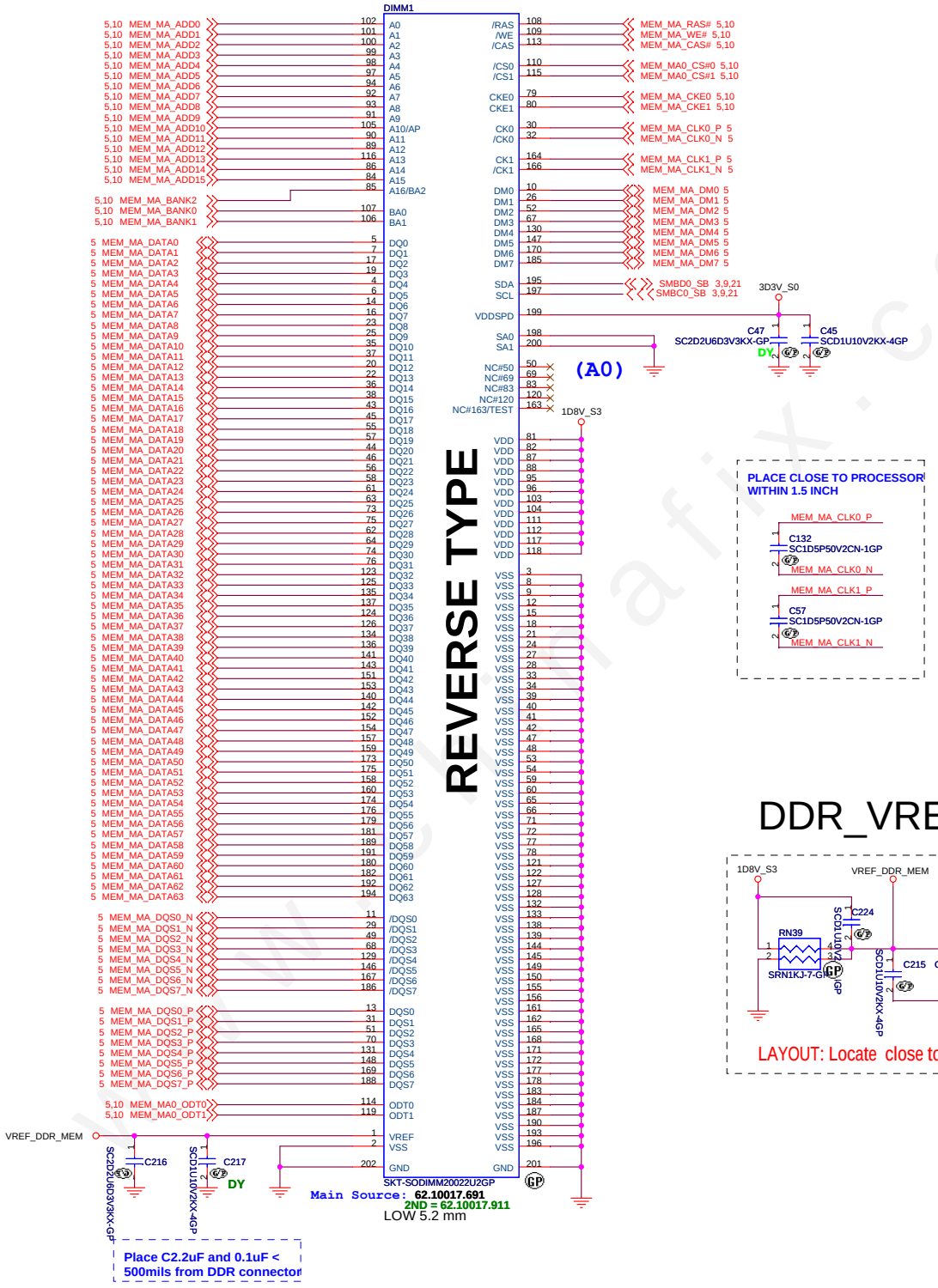


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
A4	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 7 of 55



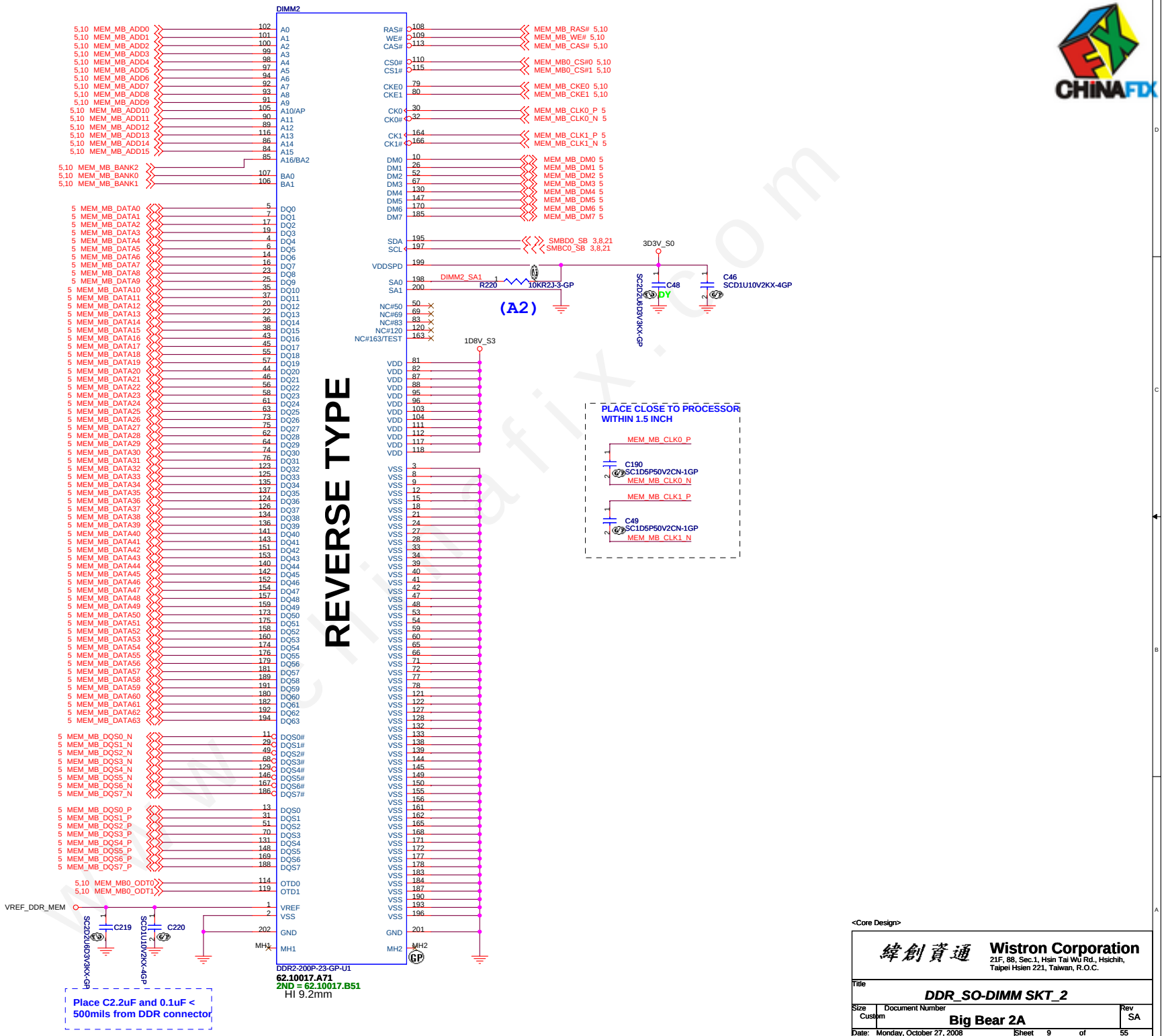
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 8 of 55



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

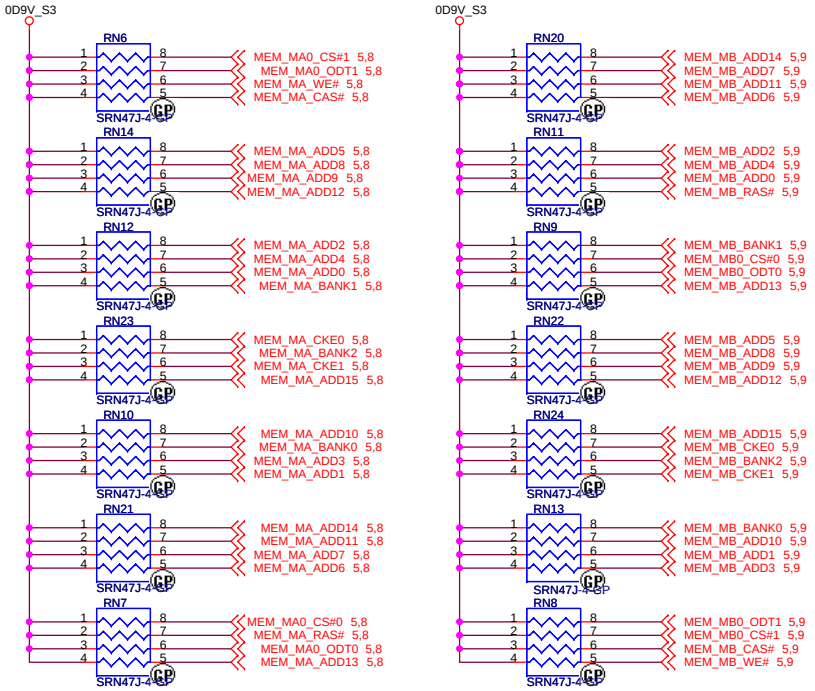
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 9 of 55

PARALLEL TERMINATION

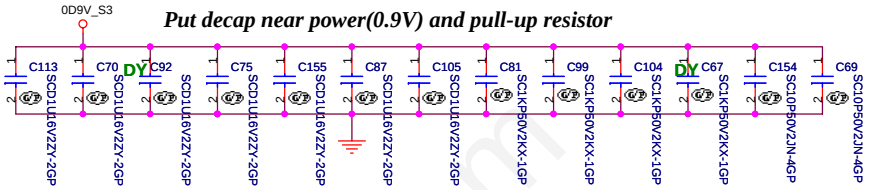
Put decap near power(0.9V) and pull-up resistor



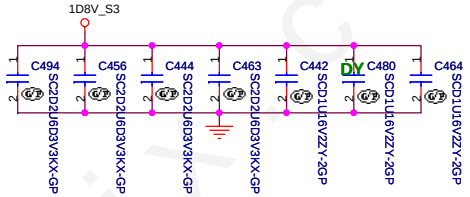
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

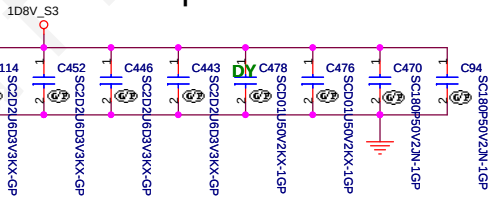


Place these Caps near DM1



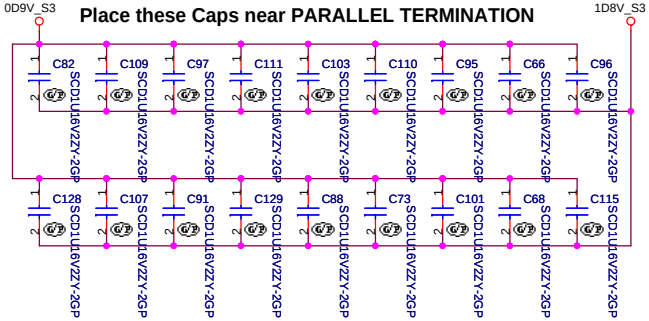
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



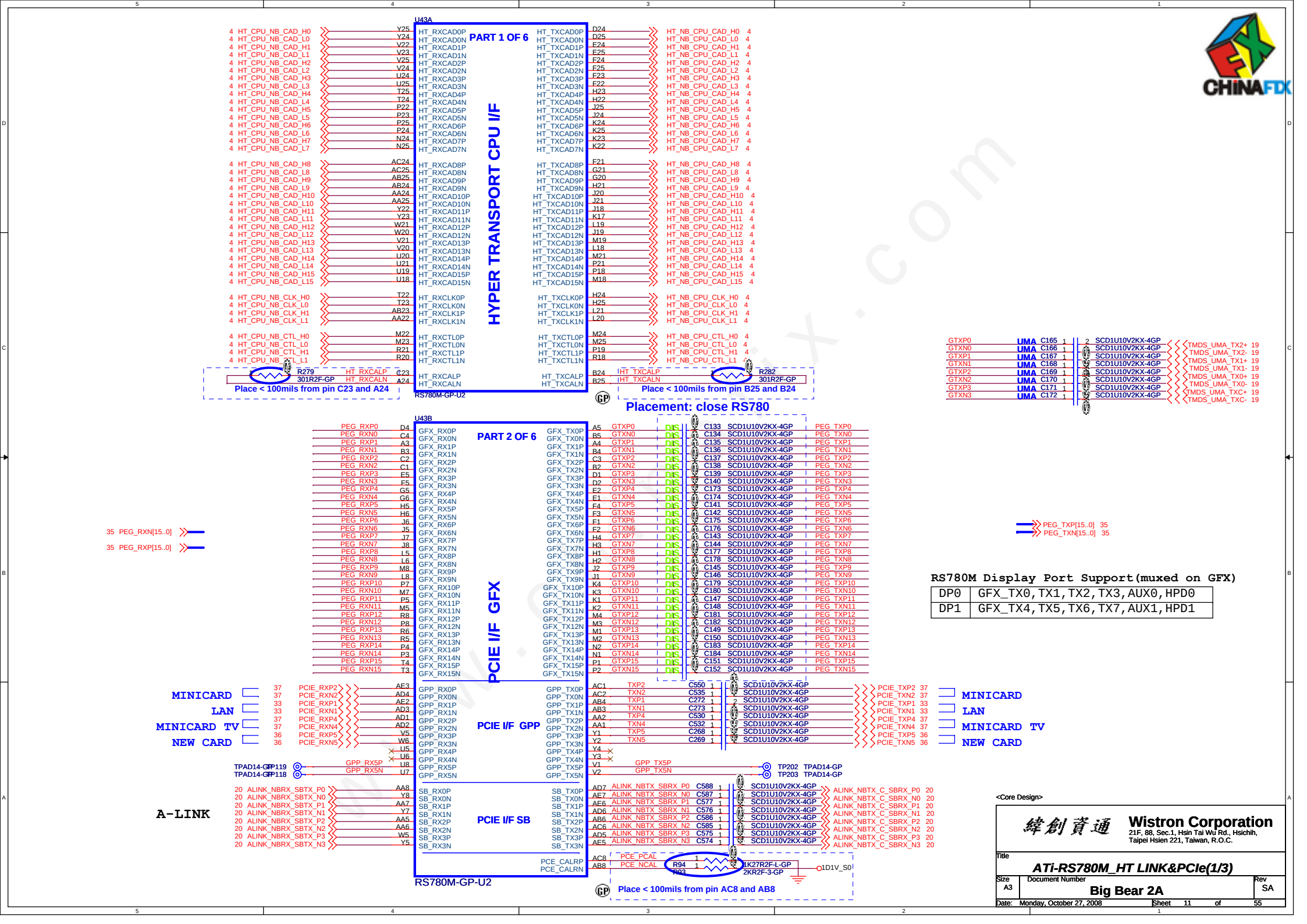
<Core Design>

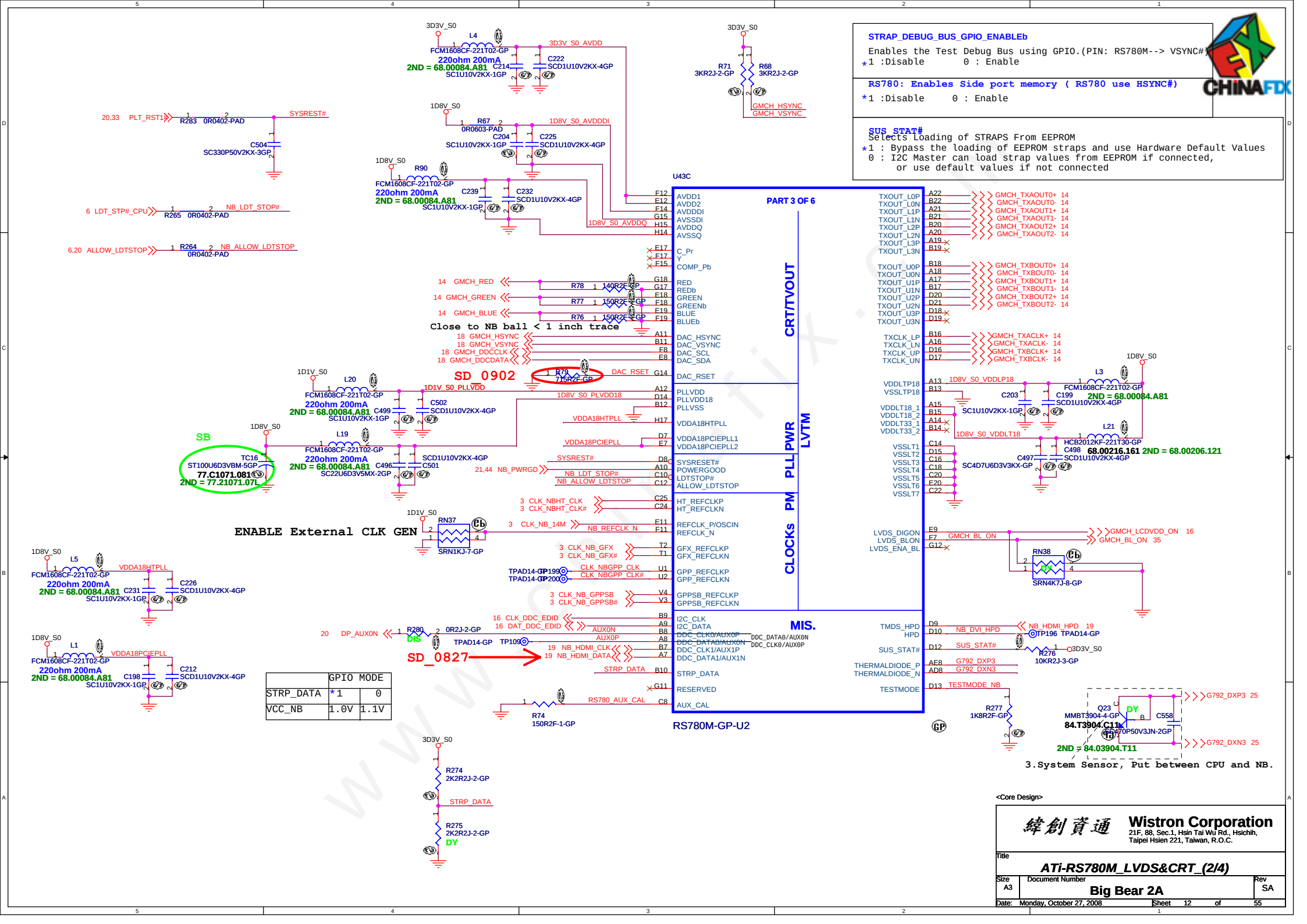
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

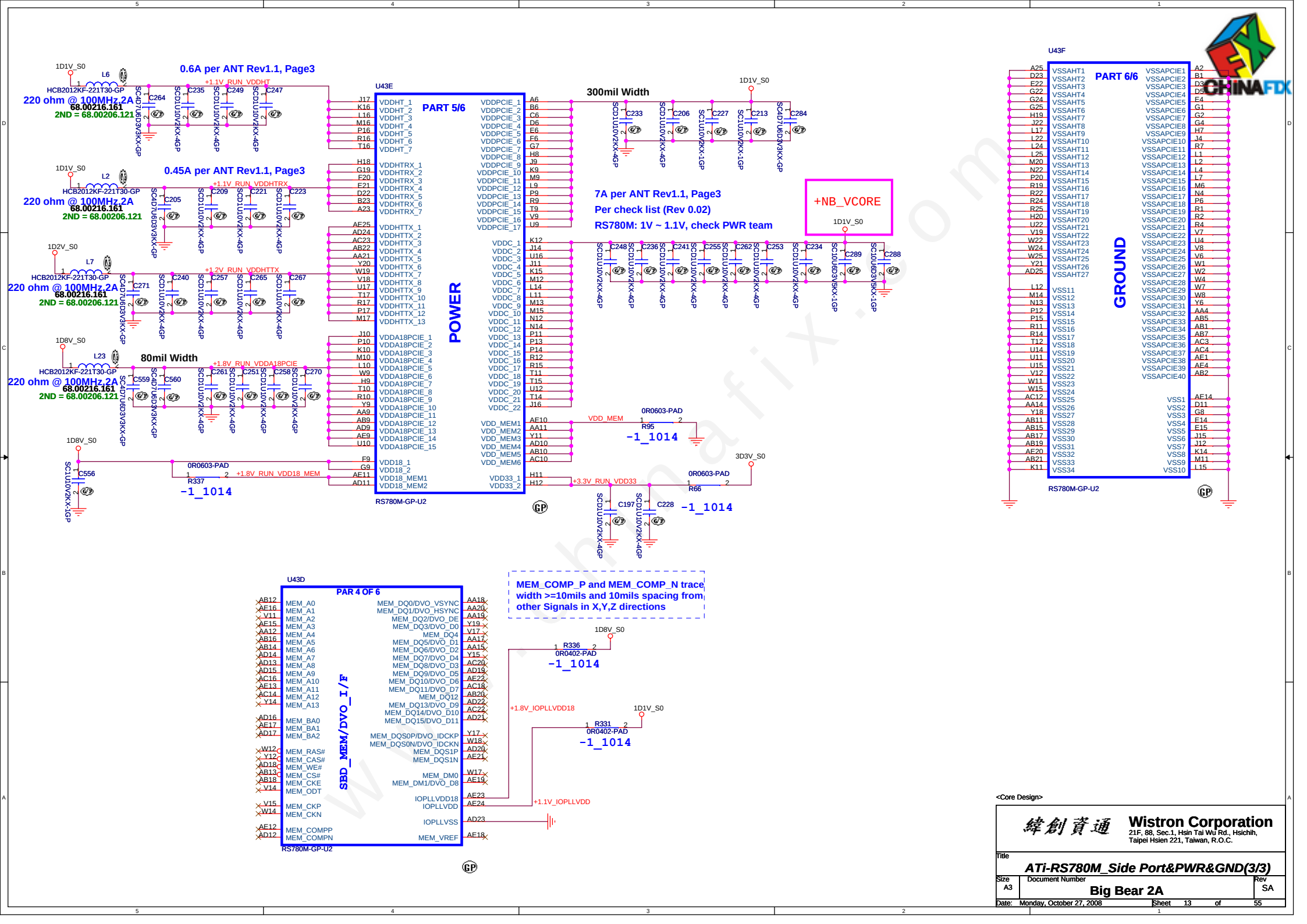
Title: ***DDR_DAMPING & TERMINATION***

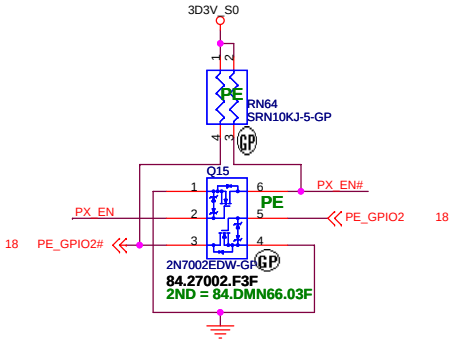
Size	Document Number	Rev
A3	Big Bear 2A	SA

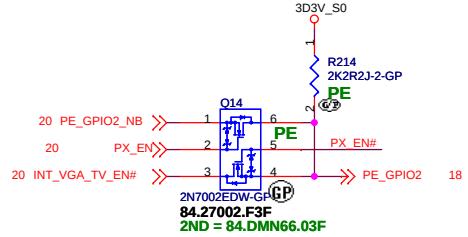
Date: Monday, October 27, 2008 Sheet 10 of 55


U43A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U43B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
MINICARD
LAN
MINICARD TV
NEW CARD
A-LINK
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 11 of 55


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL/PWR
CLOCKs
PM
MIS.
Close to NB ball < 1 inch trace
SD_0902
SD_0827
ENABLE External CLK GEN
SB
DIS
3.System Sensor, Put between CPU and NB.
GPIO MODE
STRP_DATA *1 0
VCC_NB 1.0V 1.1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
Big Bear 2A
Monday, October 27, 2008

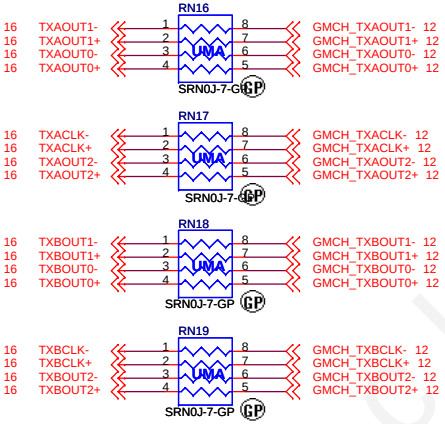

0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
PART 5/6
POWER
PART 6/6
GROUND
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
RS780M-GP-U2
Wistron Corporation
ATi-RS780M_Side Port&PWR&GND(3/3)
Big Bear 2A
Monday, October 27, 2008

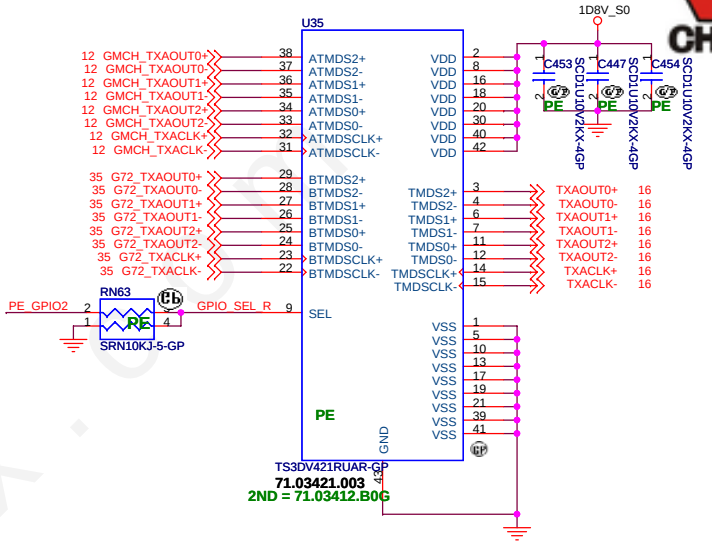


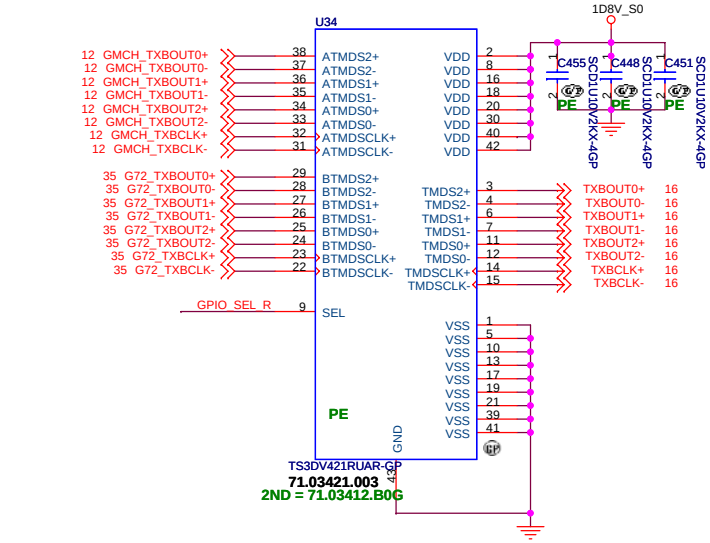


FUNCTION TABLE

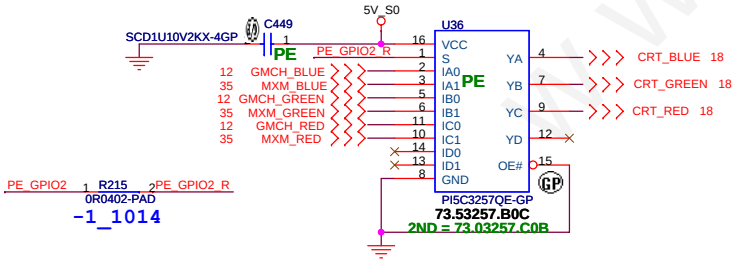
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

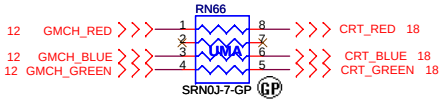






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





<Core Design>

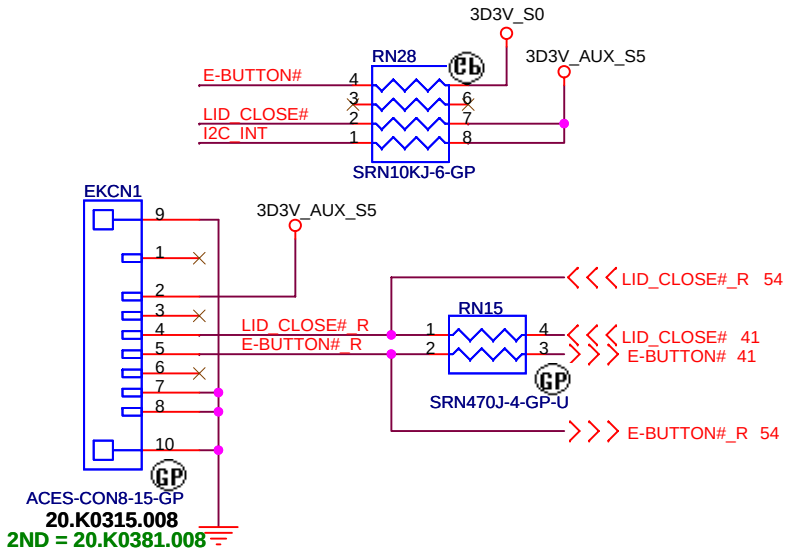
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

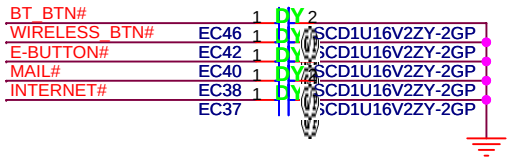
Title: SWITCH

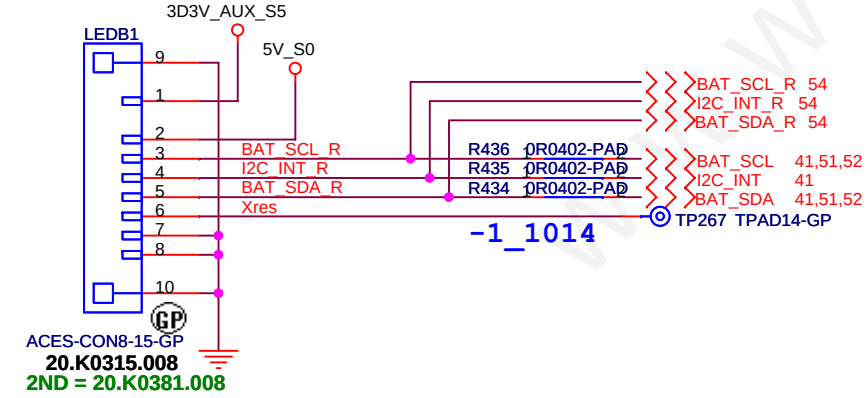
Size: A3 | Document Number: Big Bear 2A | Rev: SB

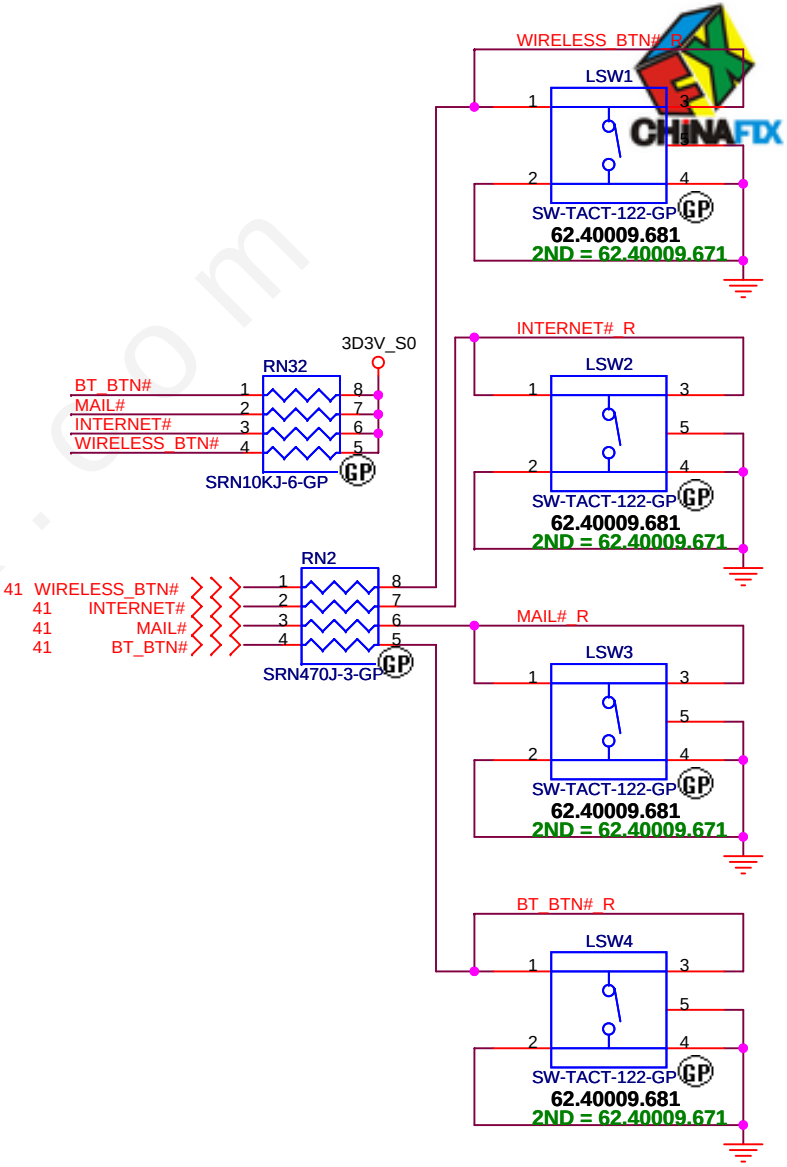
Date: Monday, October 27, 2008 | Sheet 14 of 55

LAUNCH









<Core Design>

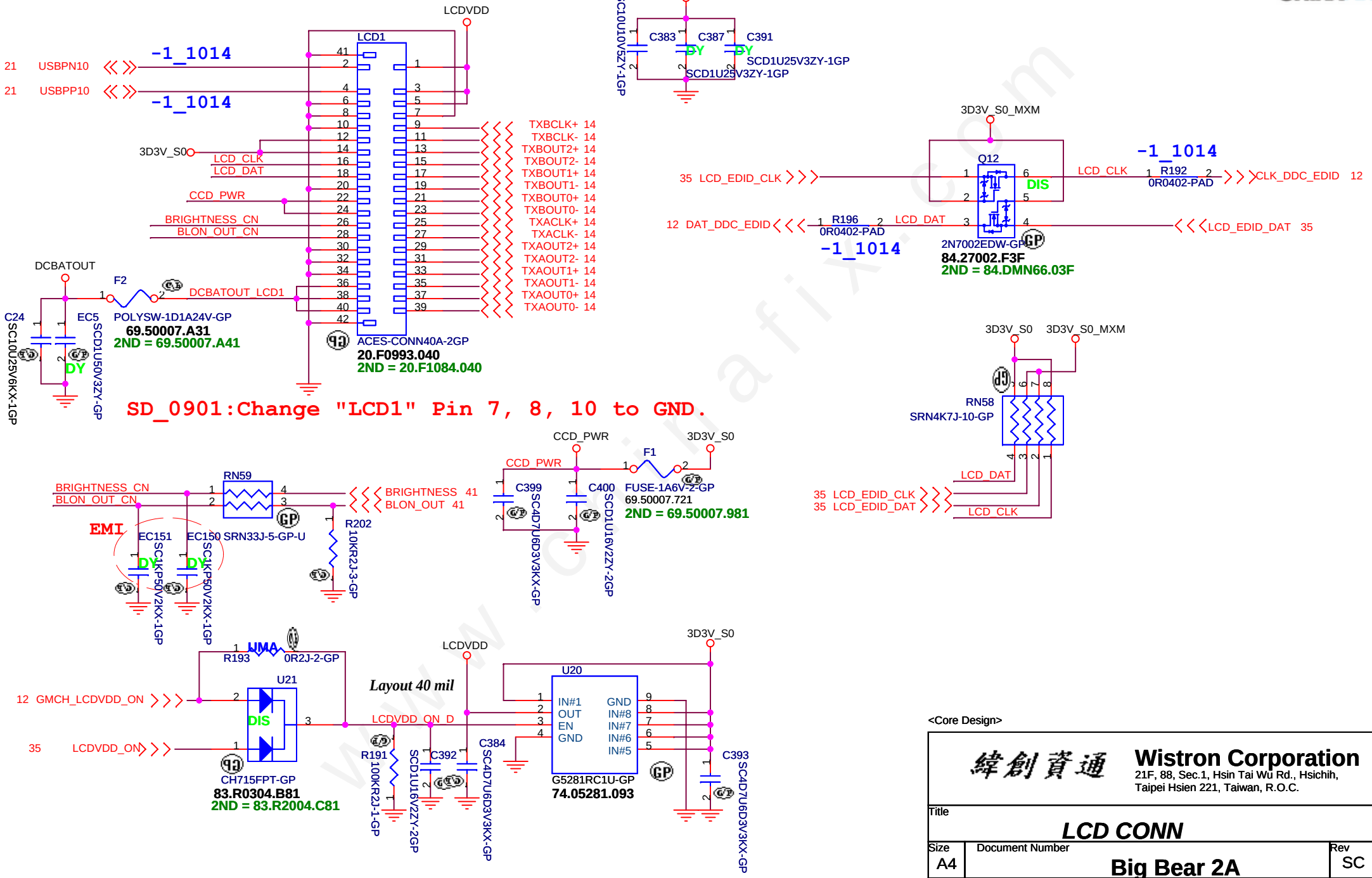
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH & LID**

Size	Document Number	Rev
A4	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 15 of 55

LCD/INVERTER/CCD CONN



<Core Design>

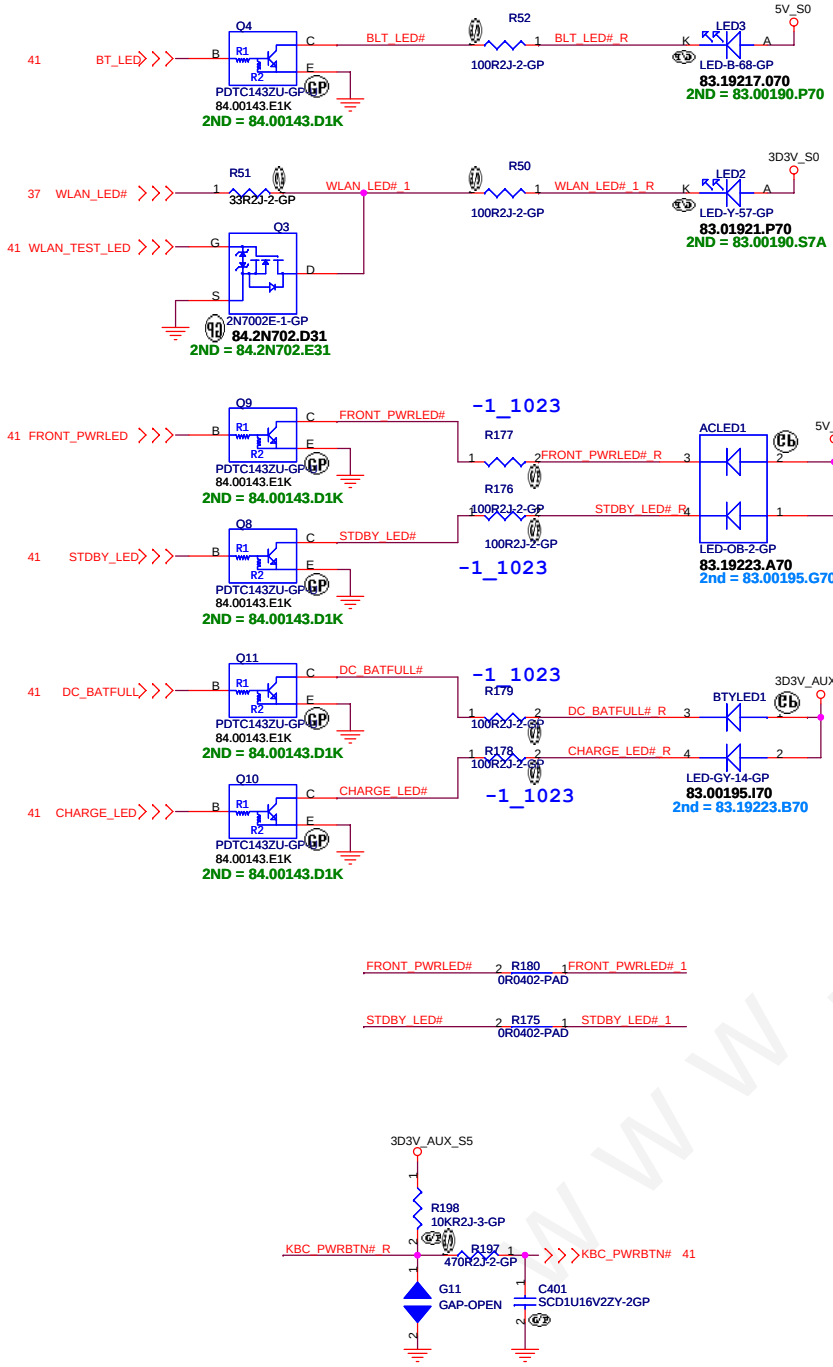
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

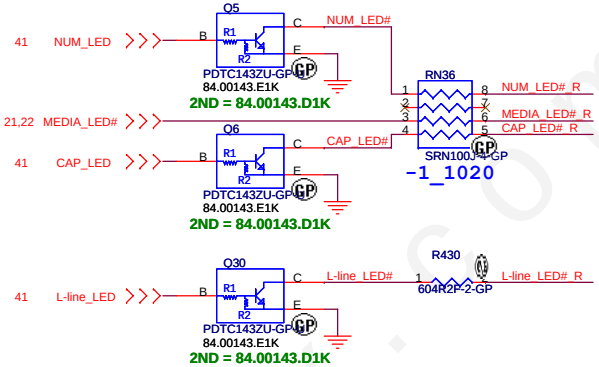
Title: LCD CONN

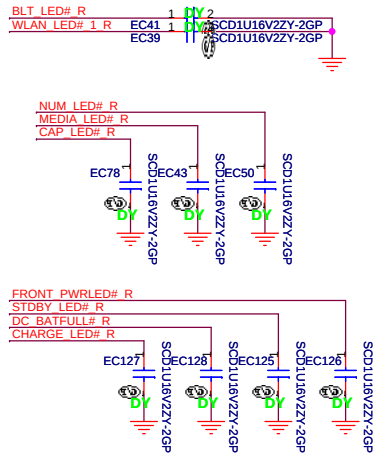
Size	Document Number	Rev
A4	Big Bear 2A	SC

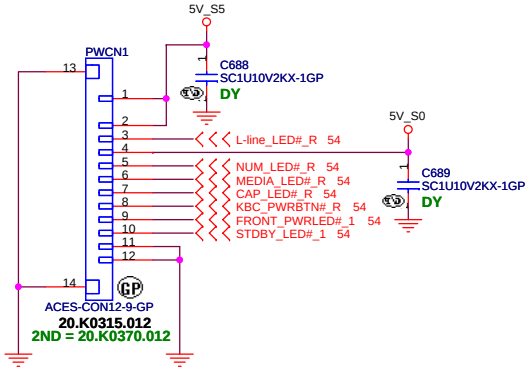
Date: Monday, October 27, 2008 Sheet 16 of 55

LED

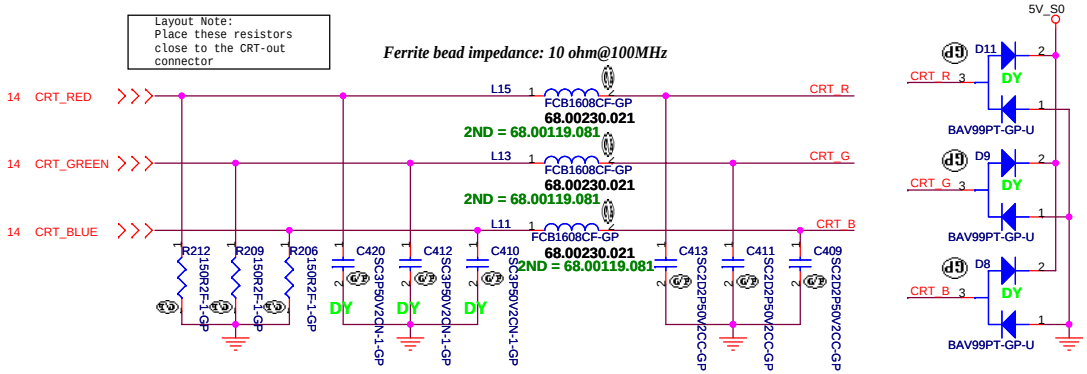






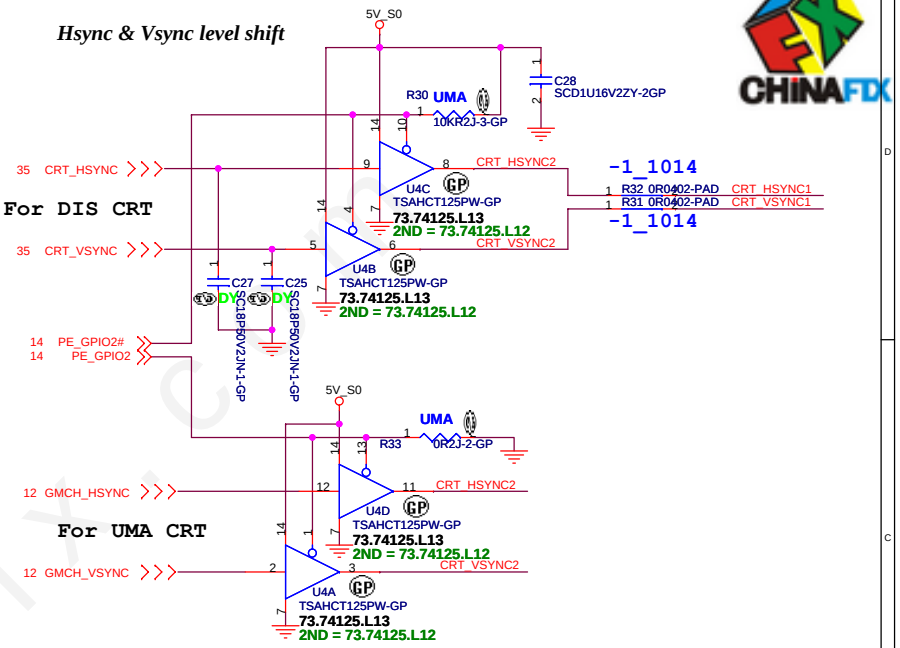


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED & LAUNCH	
Size: A3	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 17 of 55	

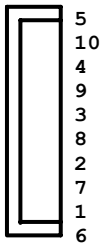


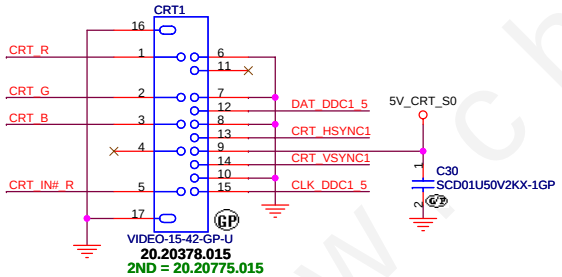
Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

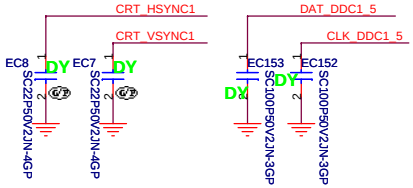
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

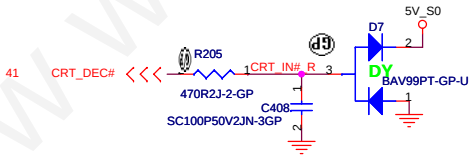


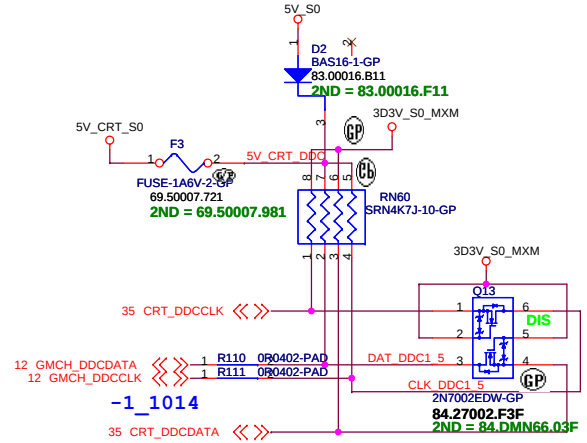
CRT I/F & CONNECTOR











<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

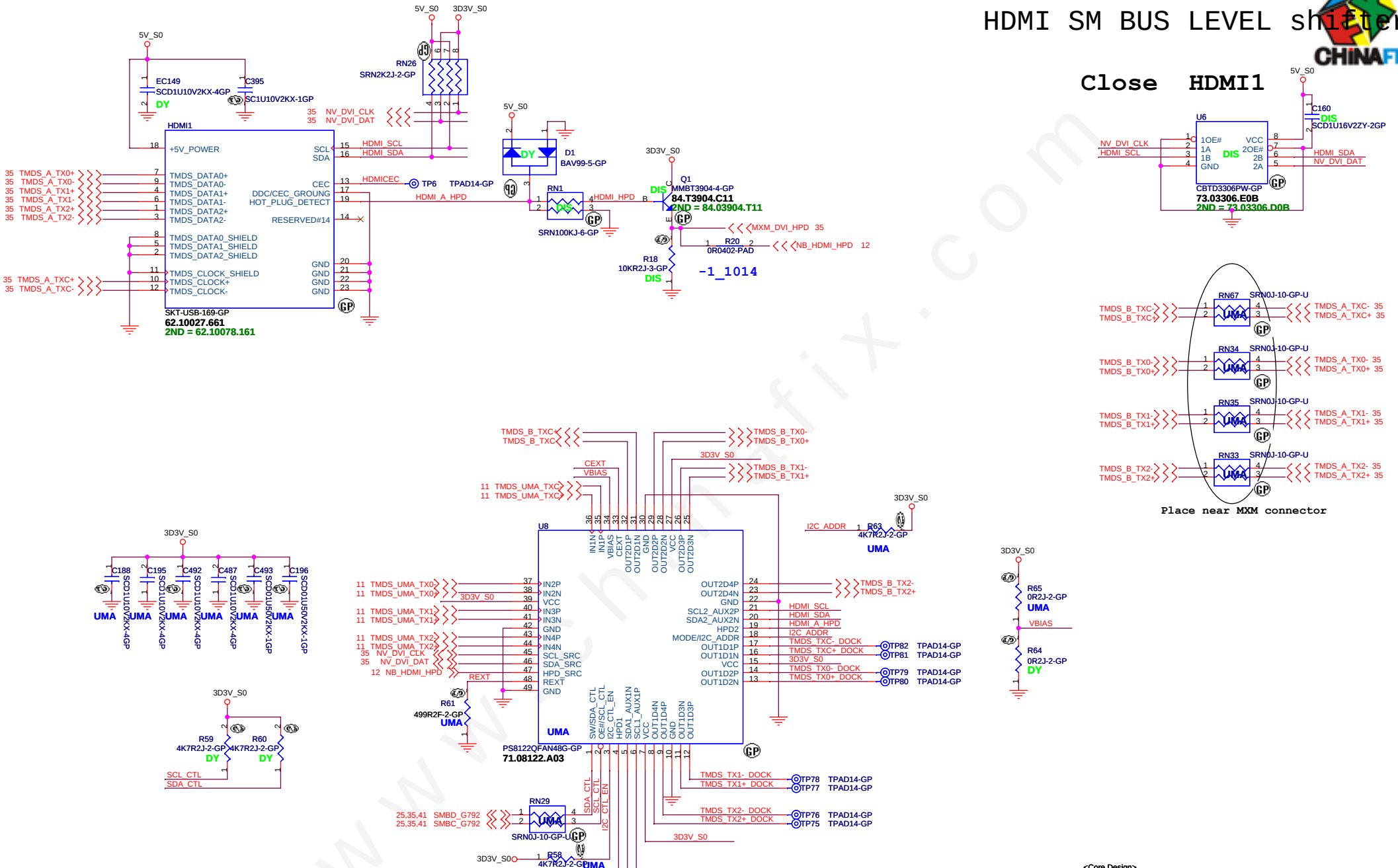
Title: **CRT Connector**

Size	Document Number	Rev
	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 18 of 55

HDMI SM BUS LEVEL shifter

Close HDMI1



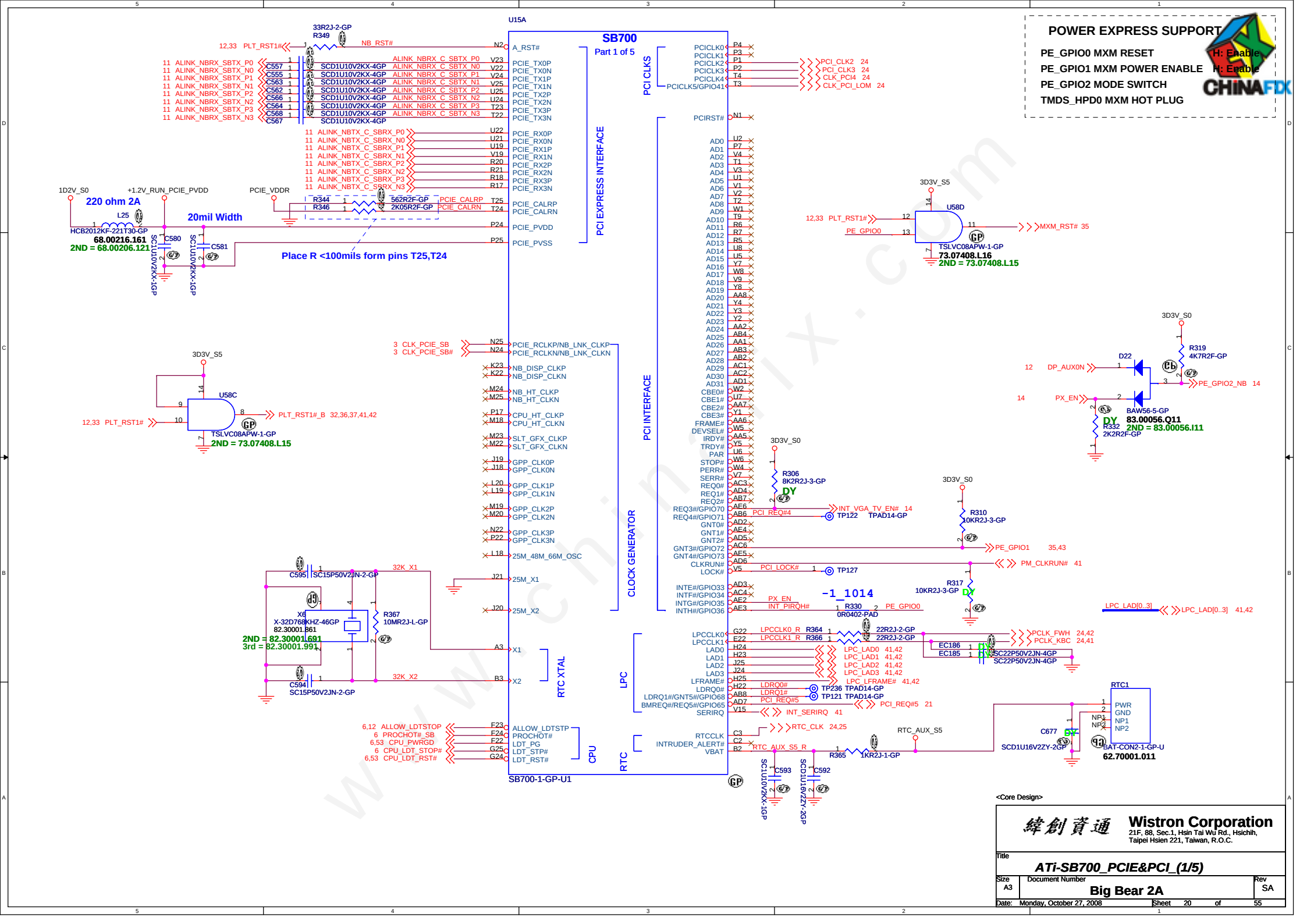
<Core Design>

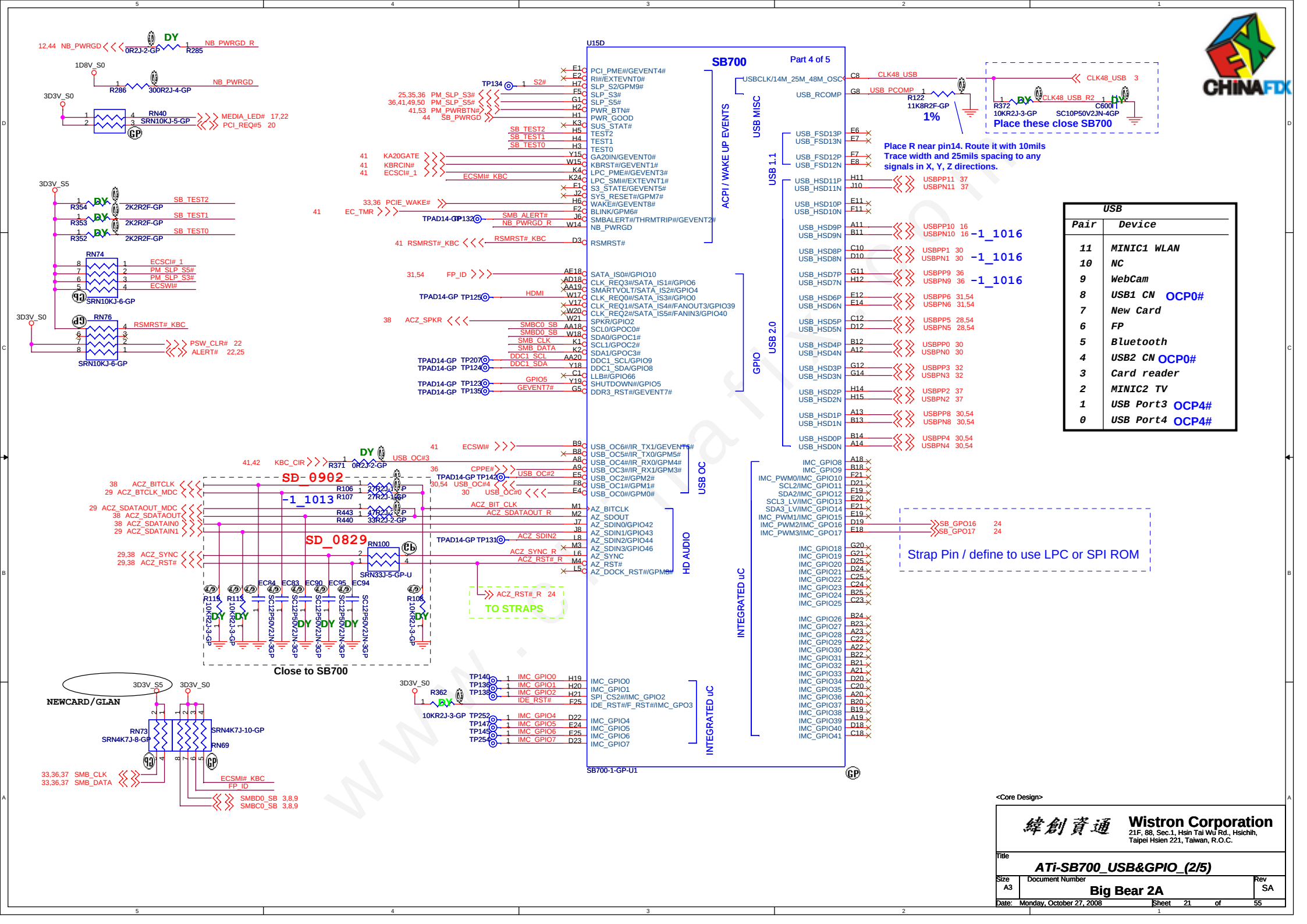
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

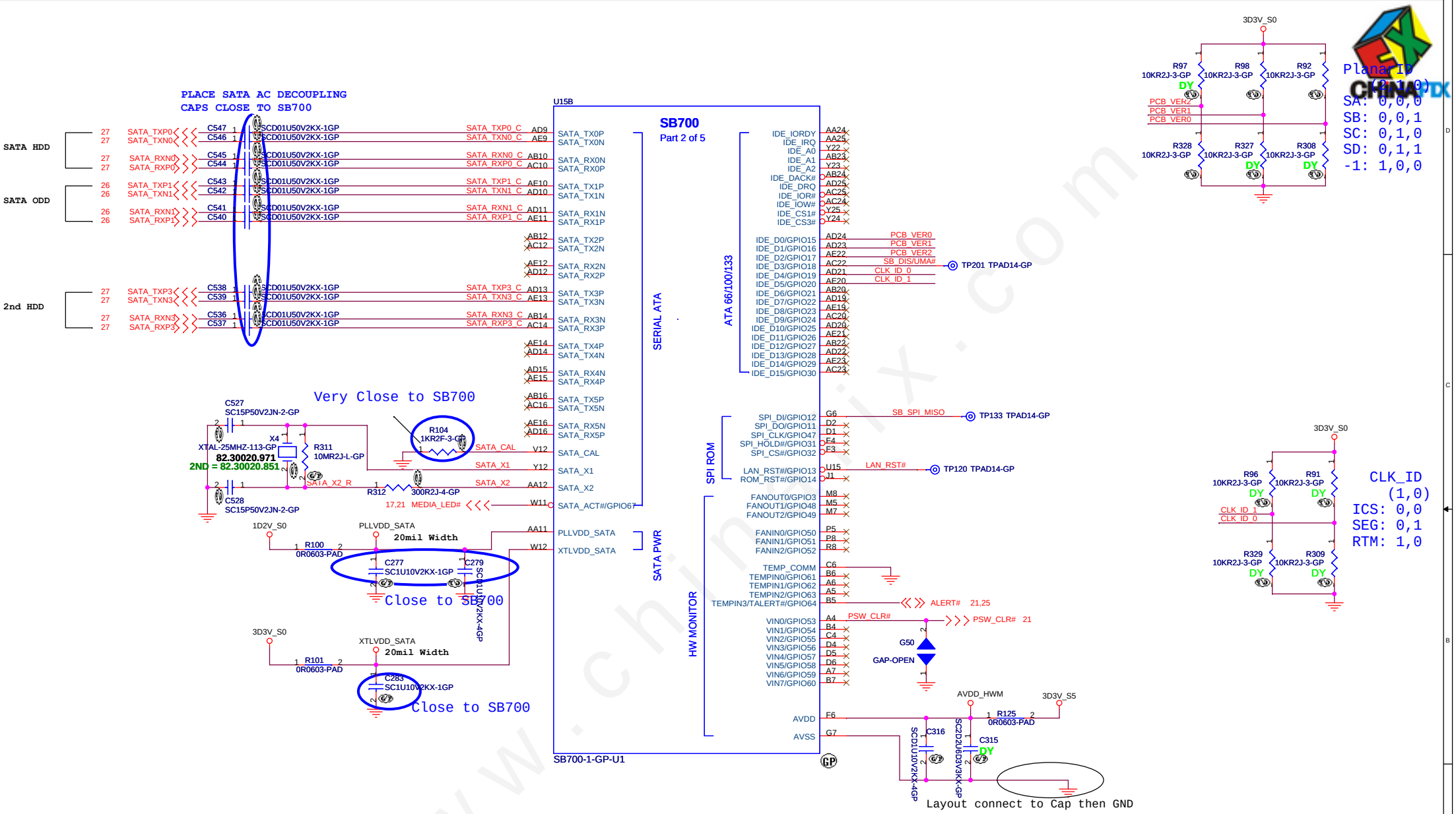
Title: HDMI CONNECTOR

Size	Document Number	Rev
A3	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 19 of 55


POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
CHINAFIX
U15A
SB700
Part 1 of 5
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
33R2J-2-GP
R349
NB_RST#
12,33 PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
1D2V_S0
220 ohm 2A
+1.2V_RUN_PCIE_PVDD
20mil Width
L25
HCB2012KF-221T30-GP
68.00216.161
2ND = 68.00206.121
C580
C581
SC1U10V2KX-1GP
PCIE_VDDR
R344 562R2F-GP PCIE_CALRP
R346 2K05R2F-GP PCIE_CALRN
Place R <100mils form pins T25,T24
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK2 24
PCI_CLK3 24
CLK_PCI4 24
CLK_PCI_LOM 24
PCIRST#
3D3V_S5
U58D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
MXM_RST# 35
3D3V_S0
R319
4K7R2F-GP
D22
DP_AUX0N
PE_GPIO2_NB 14
PX_EN
BAW56-5-GP
DY
83.00056.Q11
R332
2K2R2F-GP
2ND = 83.00056.I11
U58C
PLT_RST1#_B 32,36,37,41,42
2ND = 73.07408.L15
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
32K_X1
32K_X2
X6
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
3rd = 82.30001.991
R367
10MR2J-L-GP
C595 SC15P50V2JN-2-GP
C594 SC15P50V2JN-2-GP
X1
X2
REQ3#/GPIO70
REQ4#/GPIO71
PCI_REQ#4
INT_VGA_TV_EN# 14
TP122 TPAD14-GP
R306
8K2R2J-3-GP
DY
PCI_LOCK#
TP127
R310
10KR2J-3-GP
PE_GPIO1 35,43
PM_CLKRUN# 41
R317
10KR2J-3-GP
-1_1014
PX_EN
INT_PIRQH#
R330
0R0402-PAD
PE_GPIO0
LPC_LAD[0..3]
LPC_LAD[0..3] 41,42
LPCCLK0_R R364 22R2J-2-GP
LPCCLK1_R R366 22R2J-2-GP
PCLK_FWH 24,42
PCLK_KBC 24,41
EC186
EC185
SC22P50V2JN-4GP
LPC_LAD0 41,42
LPC_LAD1 41,42
LPC_LAD2 41,42
LPC_LAD3 41,42
LPC_LFRAME# 41,42
LDRQ0#
LDRQ1#
TP236 TPAD14-GP
TP121 TPAD14-GP
PCI_REQ#5
PCI_REQ#5 21
INT_SERIRQ 41
RTC_CLK 24,25
RTC_AUX_S5
RTC_AUX_S5_R
R365
1KR2J-1-GP
C593
C592
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
C677
SCD1U16V2ZY-2GP
RTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
62.70001.011
ALLOW_LDTSTOP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 20 of 55


SB700
Part 4 of 5
U15D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Place these close SB700
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
Close to SB700
SD_0902
-1_1013
SD_0829
NEWCARD/GLAN
USB
Pair | Device
11 | MINIC1 WLAN
10 | NC
9 | WebCam
8 | USB1 CN OCP0#
7 | New Card
6 | FP
5 | Bluetooth
4 | USB2 CN OCP0#
3 | Card reader
2 | MINIC2 TV
1 | USB Port3 OCP4#
0 | USB Port4 OCP4#
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 21 of 55



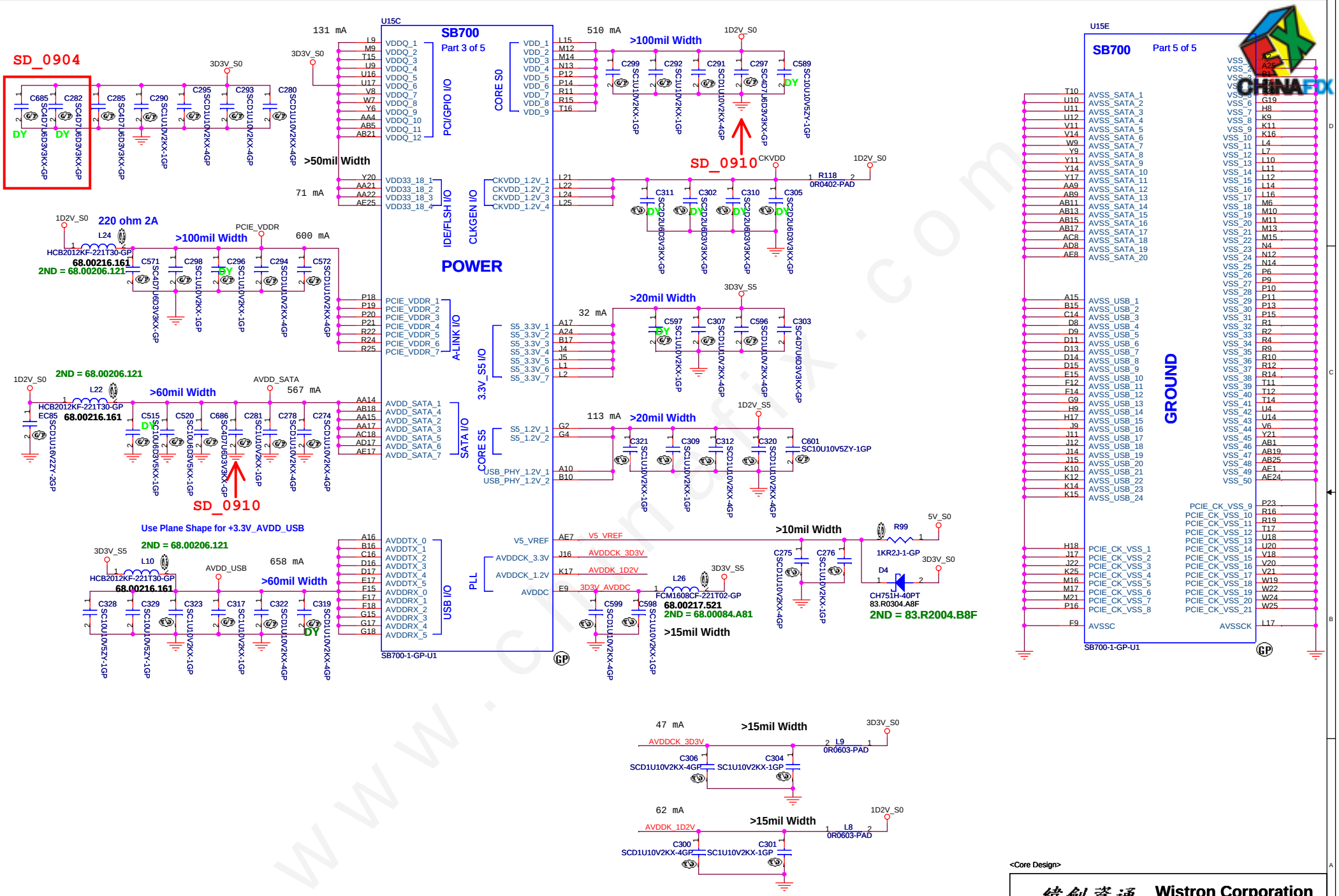
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)

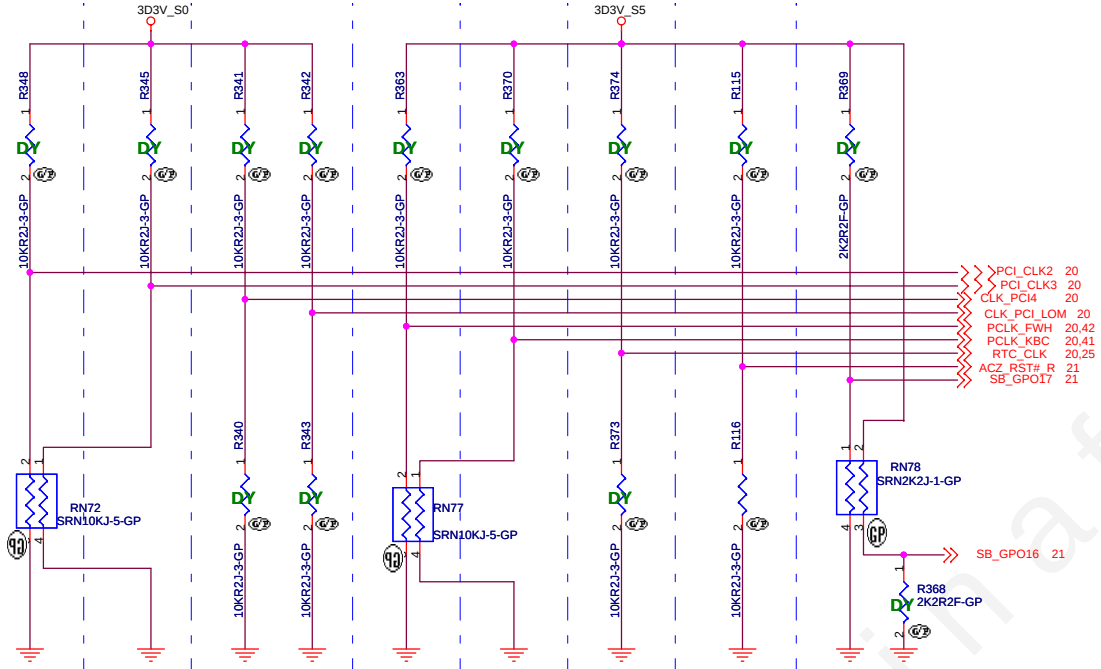
Size	Document Number	Rev
A3	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 22 of 55


SD_0904
SD_0910
SD_0910
U15C
SB700
Part 3 of 5
POWER
131 mA
510 mA
71 mA
600 mA
32 mA
113 mA
567 mA
658 mA
47 mA
62 mA
>100mil Width
>50mil Width
>20mil Width
>60mil Width
>10mil Width
>15mil Width
220 ohm 2A
2ND = 68.00206.121
2ND = 68.00084.A81
2ND = 68.00217.521
2ND = 83.R2004.B8F
Use Plane Shape for +3.3V_AVDD_USB
SB700-1-GP-U1
U15E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_POWER&GND_(4/5)
Size
A3
Document Number
Big Bear 2A
Rev
SA
Date: Monday, October 27, 2008
Sheet 23 of 55

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

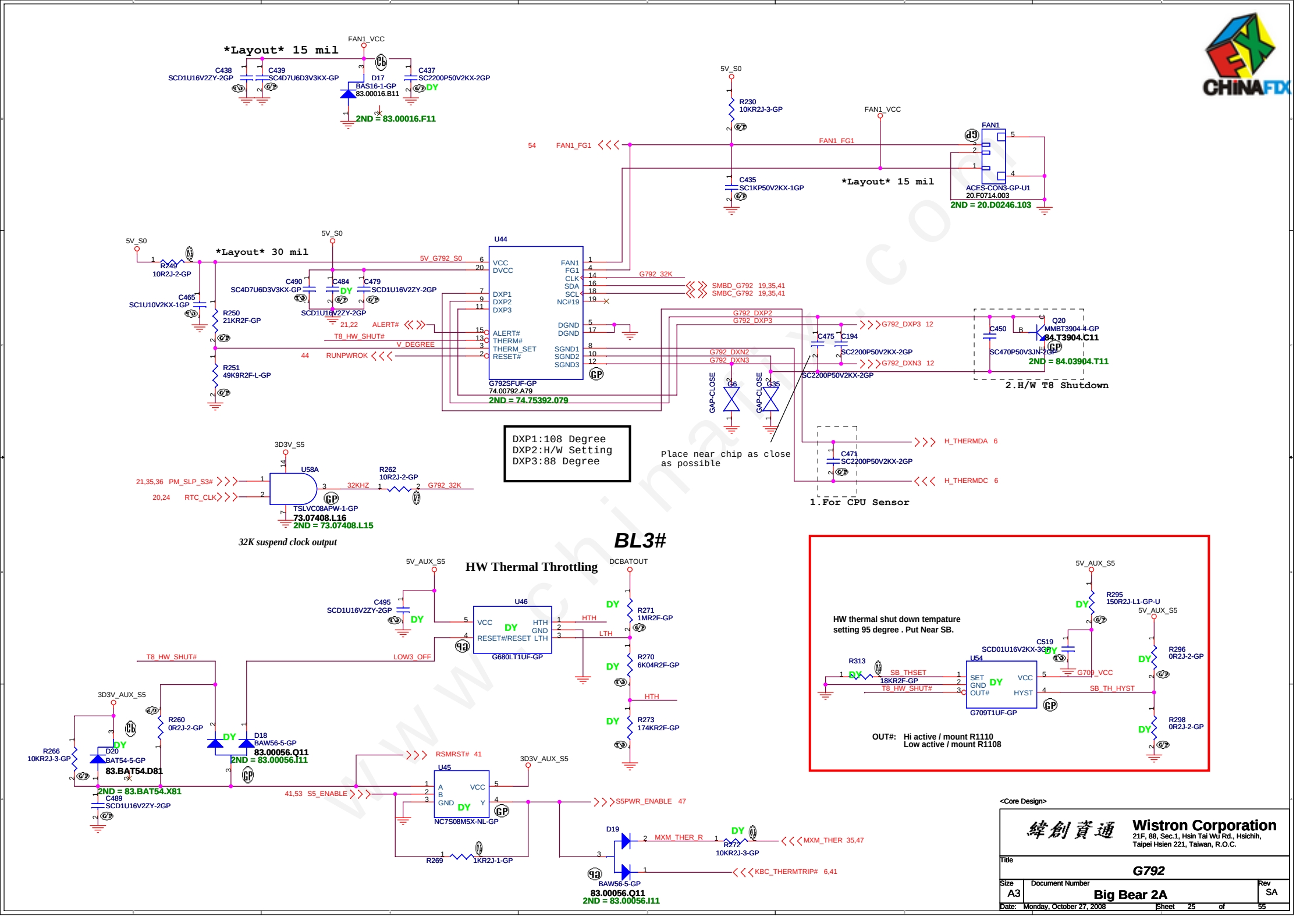
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

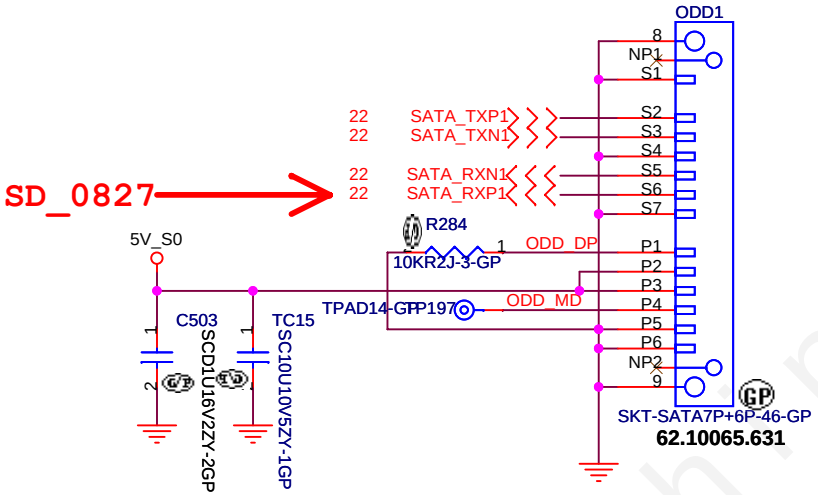
Title: ATi-SB700_STRAPPING_(5/5)

Size	Document Number	Rev
A3	Big Bear 2A	SA

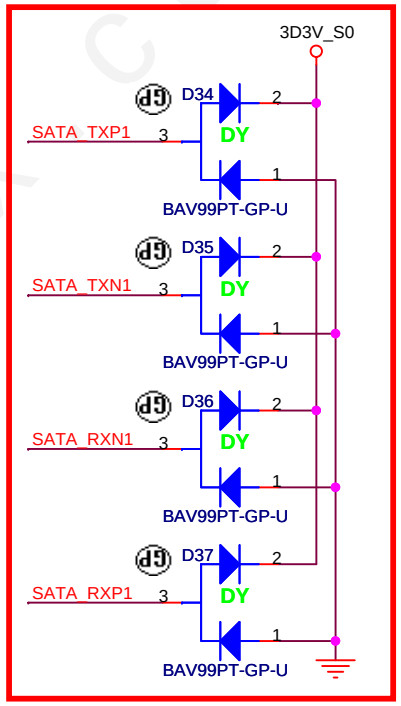
Date: Monday, October 27, 2008 Sheet 24 of 55


Layout 15 mil
FAN1_VCC
C438 SCD1U16V2ZY-2GP
C439 SC4D7U6D3V3KX-GP
D17 BAS16-1-GP 83.00016.B11
C437 SC2200P50V2KX-2GP
DY
2ND = 83.00016.F11
5V_S0
R230 10KR2J-3-GP
FAN1_VCC
54 FAN1_FG1
FAN1_FG1
FAN1
C435 SC1KP50V2KX-1GP
Layout 15 mil
ACES-CON3-GP-U1 20.F0714.003
2ND = 20.D0246.103
5V_S0
Layout 30 mil
R249 10R2J-2-GP
C465 SC1U10V2KX-1GP
R250 21KR2F-GP
R251 49K9R2F-L-GP
5V_S0
C490 SC4D7U6D3V3KX-GP
C484 DY
C479 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
5V_G792_S0
21,22 ALERT#
T8_HW_SHUT#
V_DEGREE
44 RUNPWROK
U44
VCC DVCC
DXP1 DXP2 DXP3
ALERT# THERM# THERM_SET RESET#
FAN1 FG1 CLK SDA SCL NC#19
DGND DGND
SGND1 SGND2 SGND3
G792SFUF-GP 74.00792.A79
2ND = 74.75392.079
G792_32K
SMBD_G792 19,35,41
SMBC_G792 19,35,41
G792_DXP2
G792_DXP3
G792_DXP3 12
C475 C194
SC2200P50V2KX-2GP
G792_DXN2
G792_DXN3
G792_DXN3 12
SC2200P50V2KX-2GP
GAP-CLOSE G6
GAP-CLOSE G35
C450
Q20 MMBT3904-4-GP 84.T3904.C11
SC470P50V3JN-2GP
2ND = 84.03904.T11
2.H/W T8 Shutdown
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C471 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
U58A
21,35,36 PM_SLP_S3#
20,24 RTC_CLK
32KHZ
R262 10R2J-2-GP
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
32K suspend clock output
BL3#
HW Thermal Throttling
5V_AUX_S5
C495 SCD1U16V2ZY-2GP
DY
U46
VCC DY RESET#/RESET
HTH GND LTH
G680LT1UF-GP
DCBATOUT
R271 1MR2F-GP
R270 6K04R2F-GP
R273 174KR2F-GP
HTH
LTH
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R260 0R2J-2-GP
R266 10KR2J-3-GP
D20 BAT54-5-GP 83.BAT54.D81
2ND = 83.BAT54.X81
C489 SCD1U16V2ZY-2GP
D18 BAW56-5-GP 83.00056.Q11
2ND = 83.00056.I11
RSMRST# 41
41,53 S5_ENABLE
U45
A B GND DY VCC Y
NC7S08M5X-NL-GP
3D3V_AUX_S5
S5PWR_ENABLE 47
R269 1KR2J-1-GP
D19 BAW56-5-GP
MXM_THER_R
R272 10KR2J-3-GP
MXM_THER 35,47
KBC_THERMTRIP# 6,41
83.00056.Q11
2ND = 83.00056.I11
HW thermal shut down tempature setting 95 degree . Put Near SB.
5V_AUX_S5
R295 150R2J-L1-GP-U
C519 SCD01U16V2KX-3GP
R313 18KR2F-GP
SB_THSET
T8_HW_SHUT#
U54
SET GND OUT# VCC HYST
G709T1UF-GP
G709_VCC
SB_TH_HYST
R296 0R2J-2-GP
R298 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 25 of 55

ODD Connector



SD_0828



<Core Design>

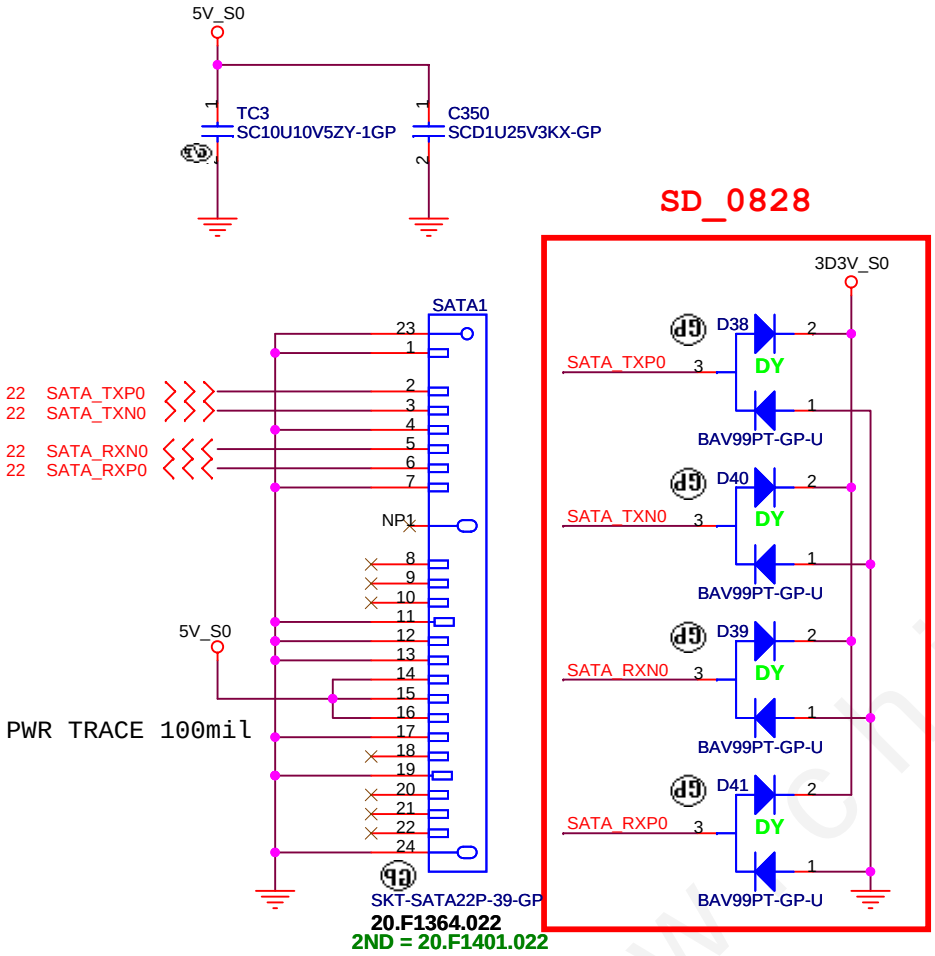
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

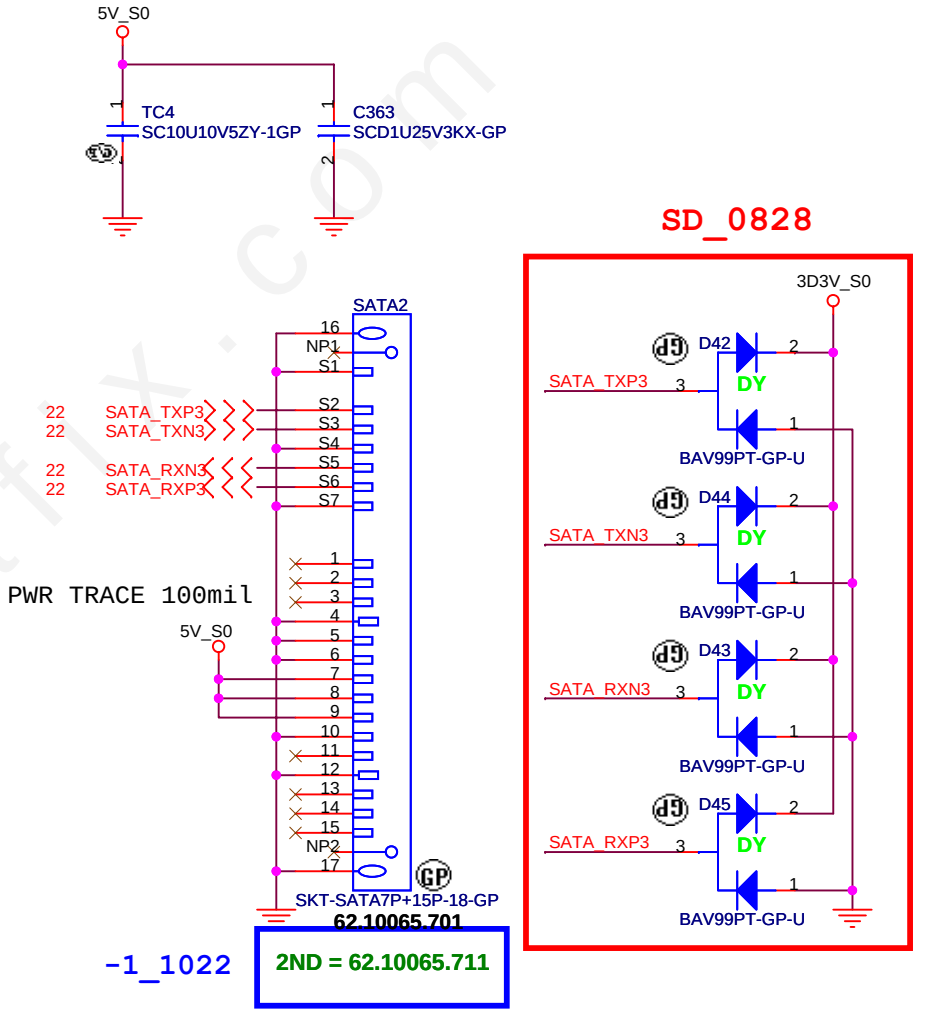
Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 26 of 55

SATA HDD Connector



2ND SATA HDD Connector

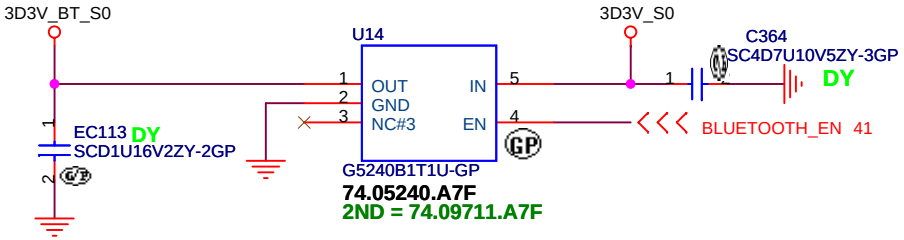


<Core Design>

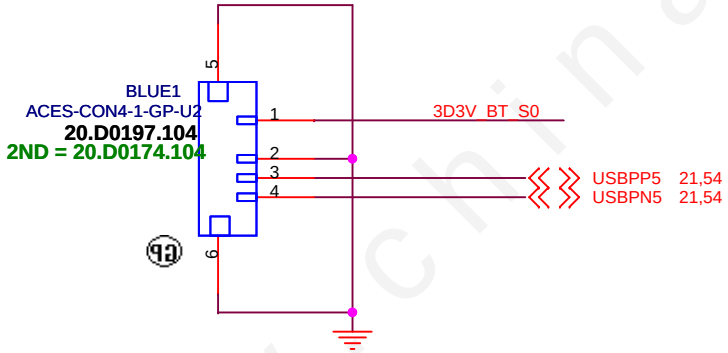
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HDD*		
Size: A4	Document Number: **Big Bear 2A**	Rev: SD
Date: Monday, October 27, 2008	Sheet 27 of 55	

BLUETOOTH MODULE



EC40 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

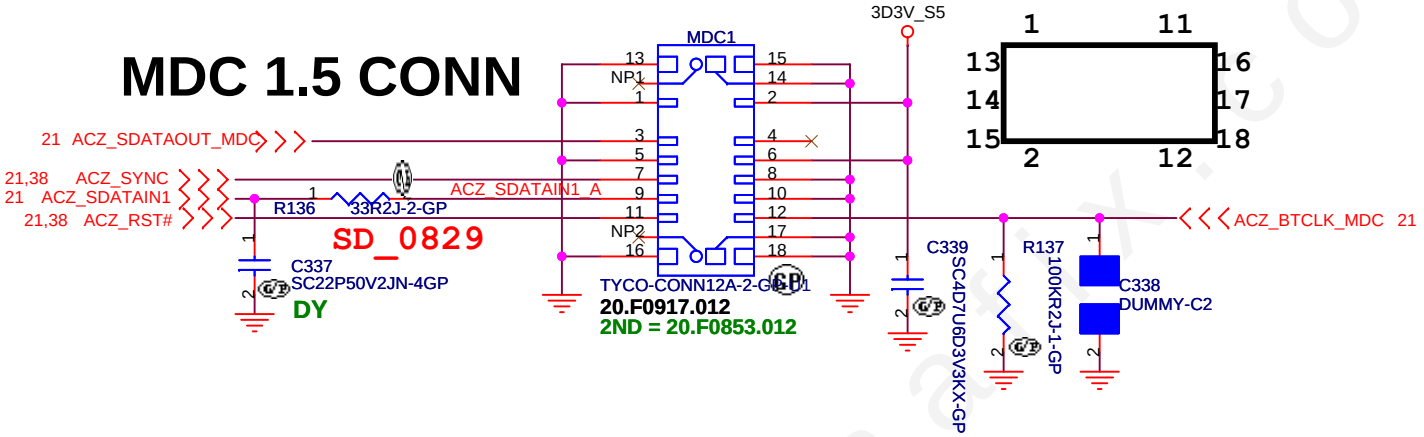


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

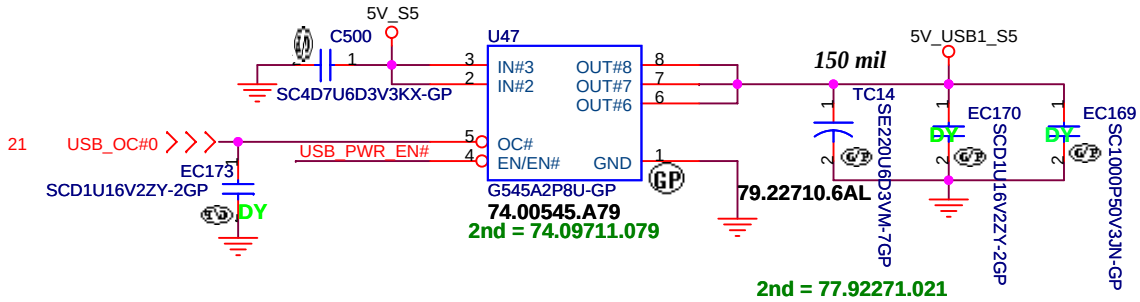
Title: BLUETOOTH		
Size: A4	Document Number: Big Bear 2A	Rev: SA
Date: Monday, October 27, 2008	Sheet 28 of 55	

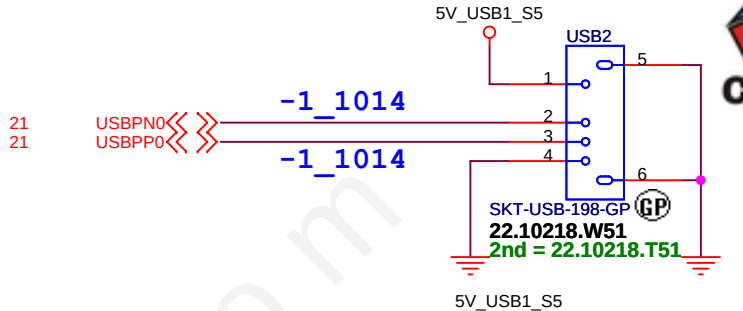
MDC 1.5 CONN

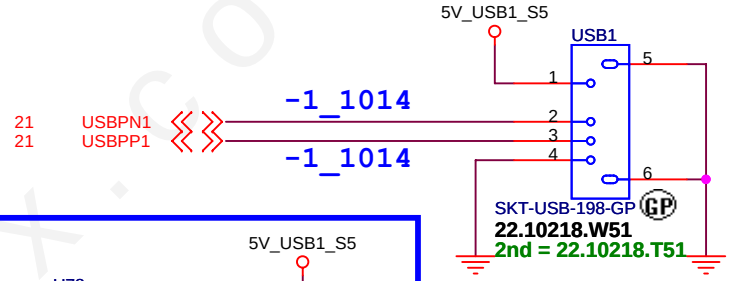


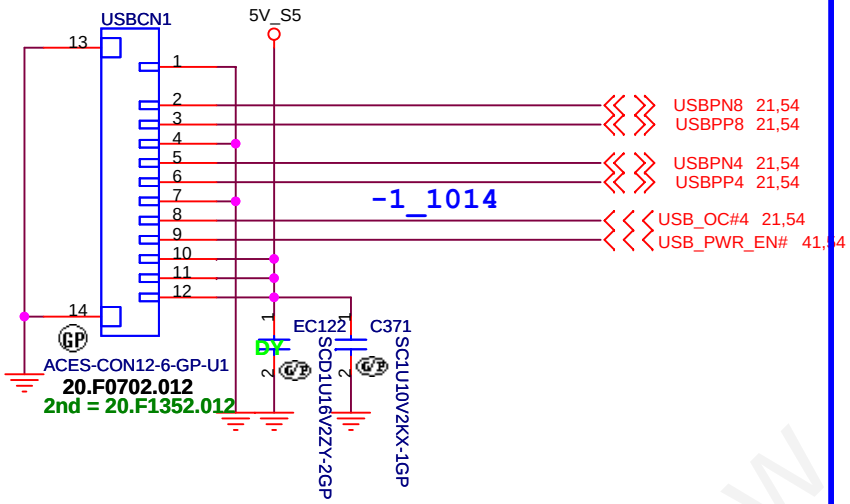
<Core Design>

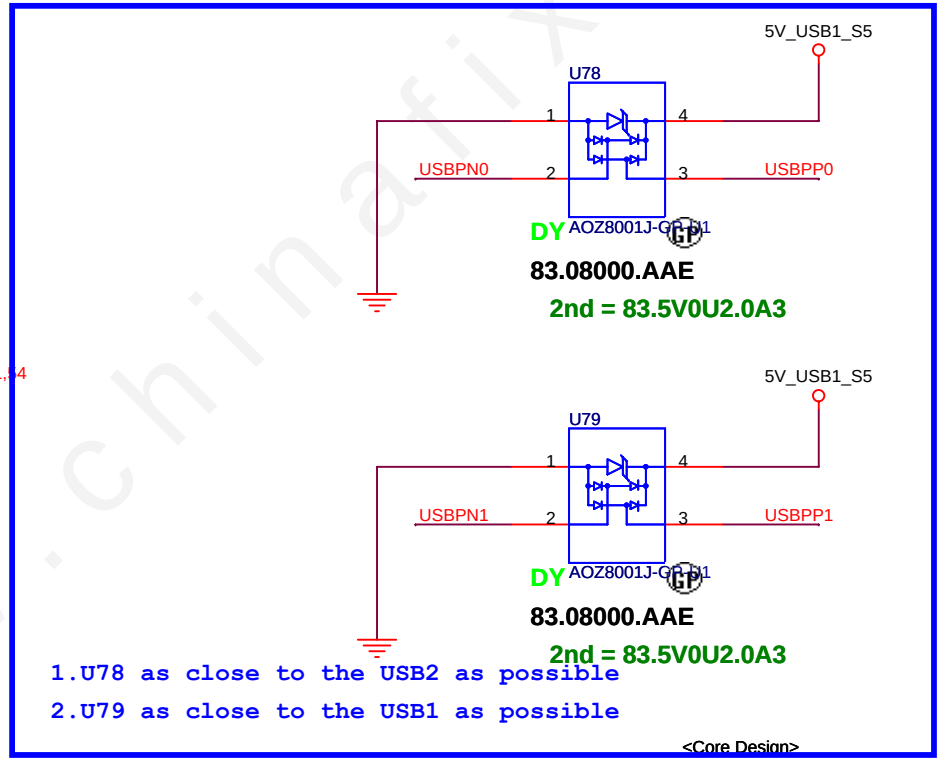
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC***
Size: A4	Document Number: **Big Bear 2A**
Rev: SA	
Date: Monday, October 27, 2008	Sheet 29 of 55









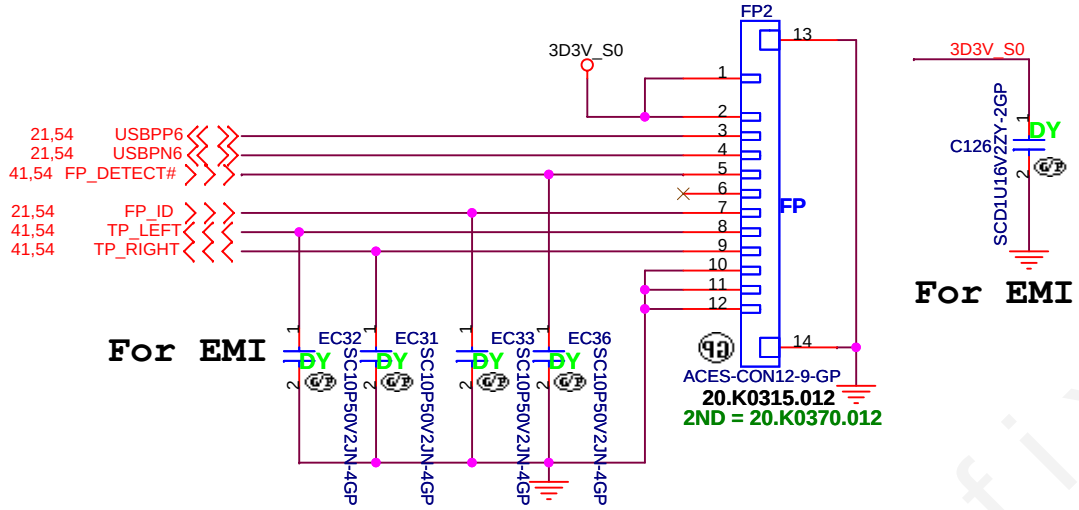


ESD Protection

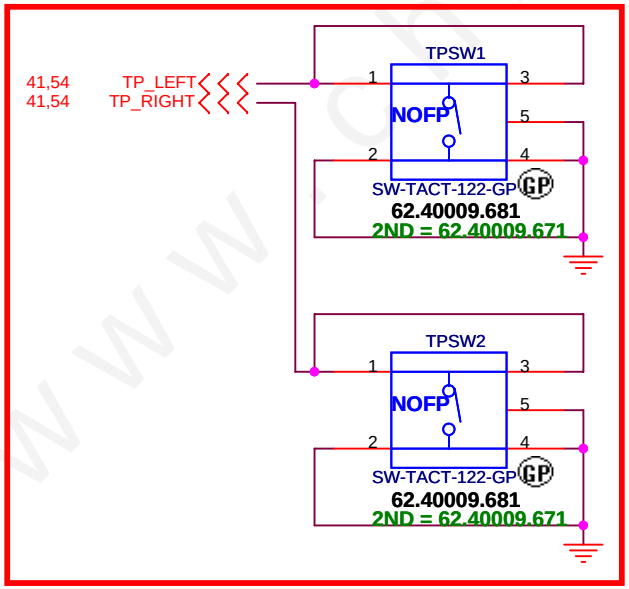
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size: A4	Document Number: Big Bear 2A	Rev: SB
Date: Monday, October 27, 2008	Sheet 30 of 55	

Finger printer



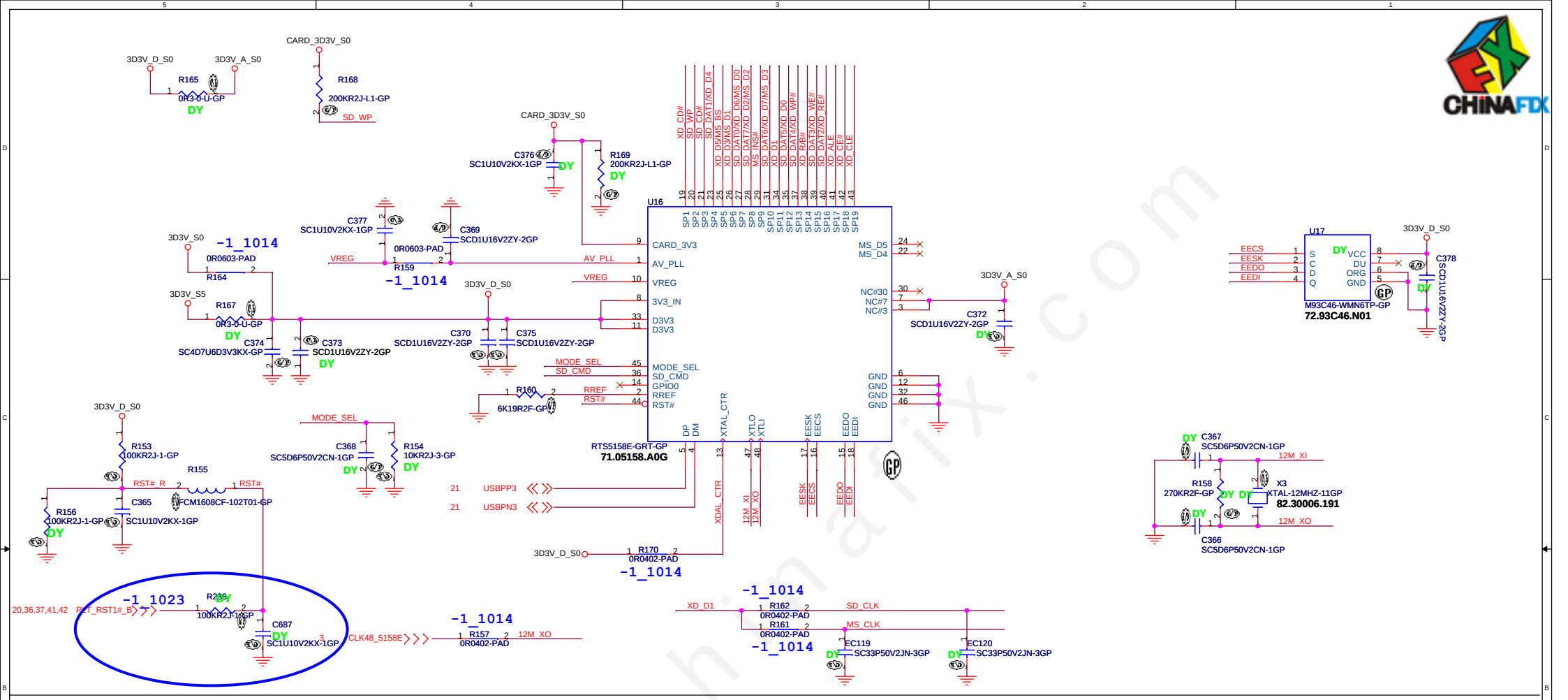
SD_0903



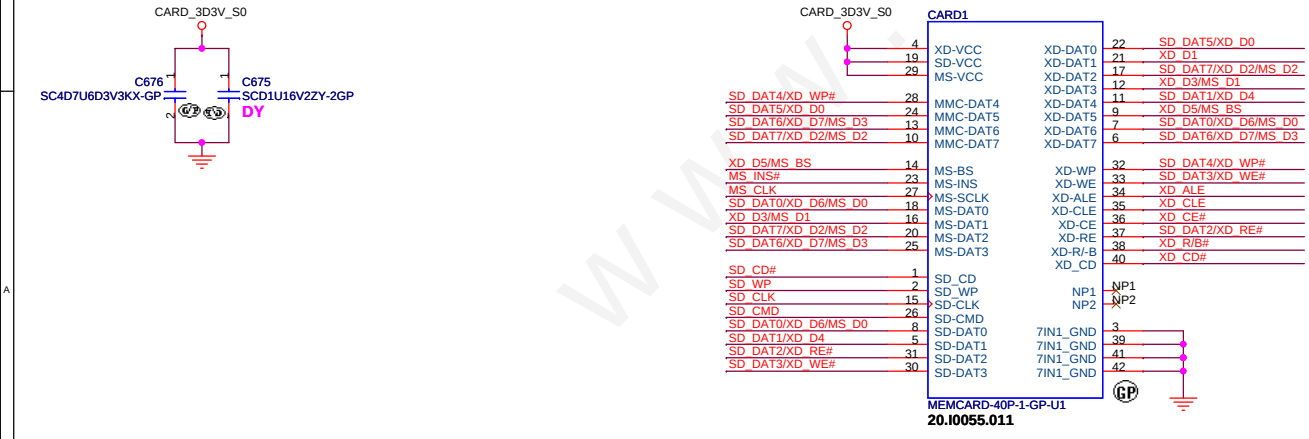
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Finger Printer***	
Size: A4	Document Number: **Big Bear 2A**	Rev: SD
Date: Monday, October 27, 2008	Sheet 31 of 55	

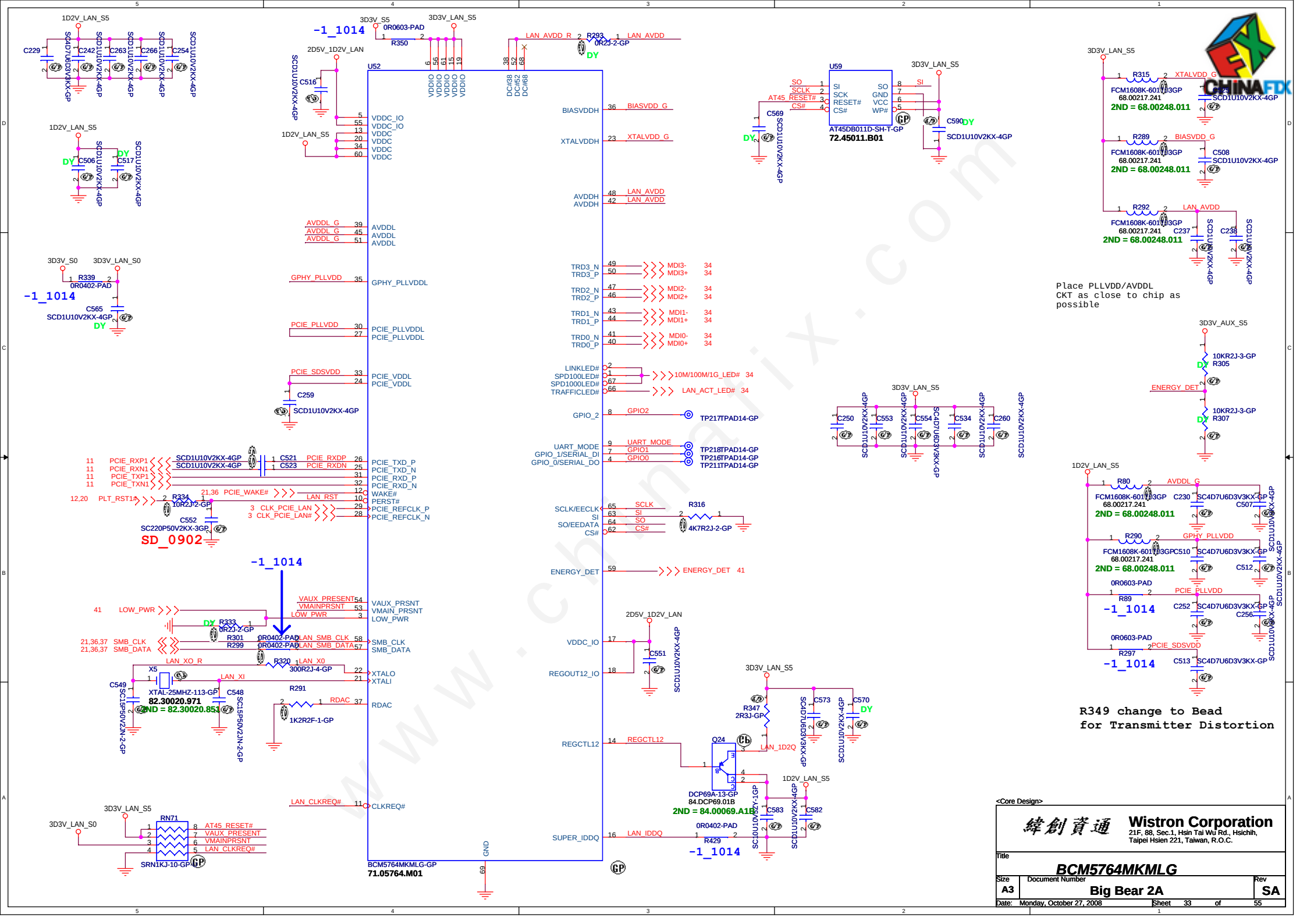


7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

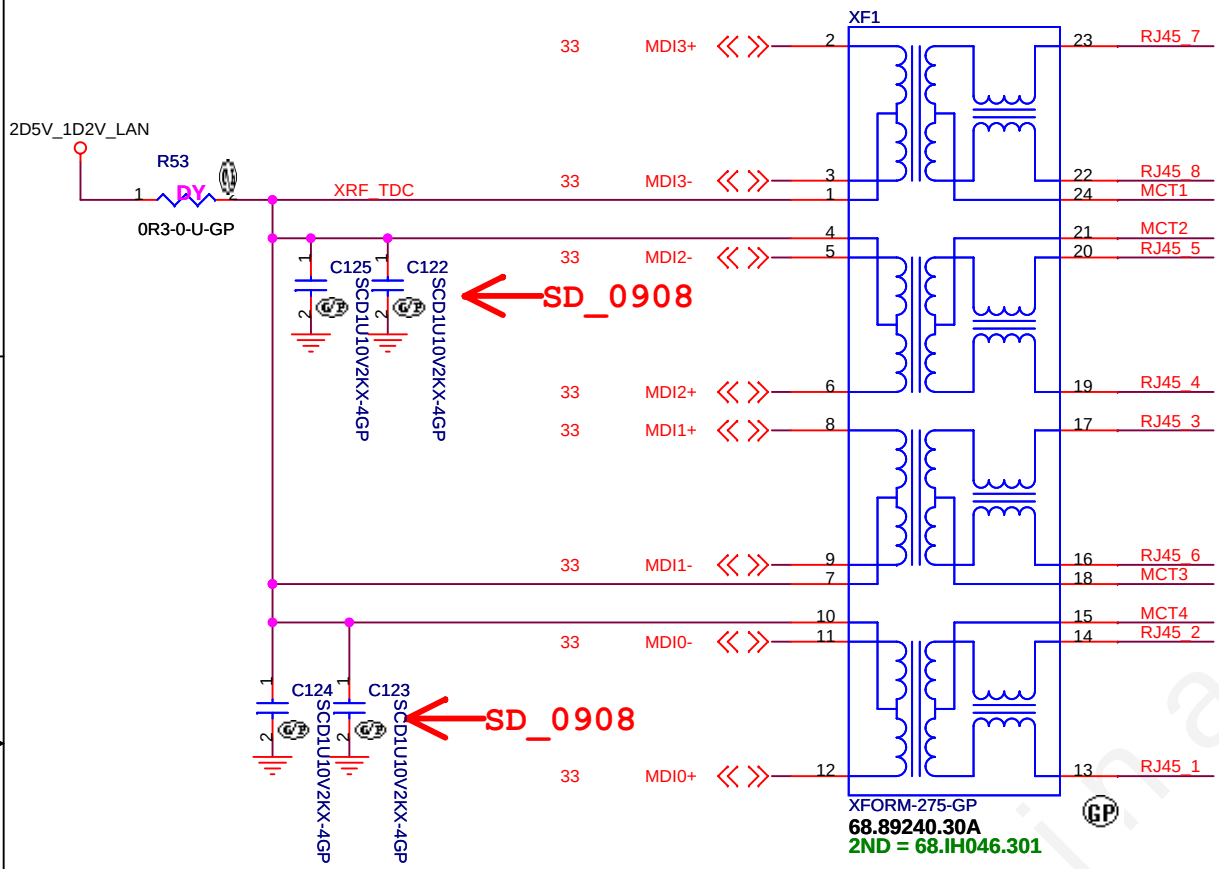


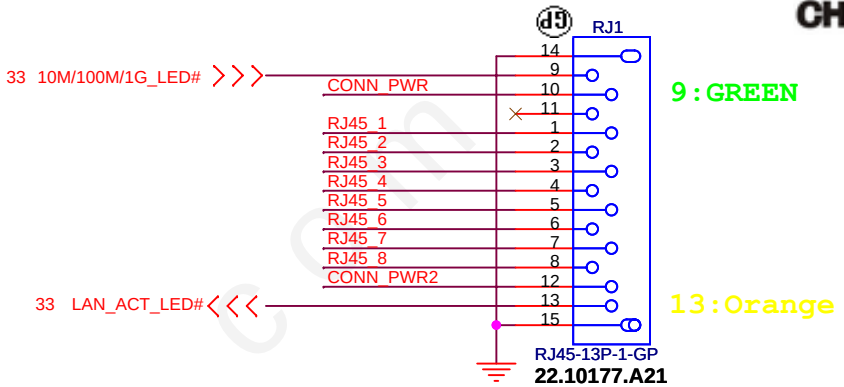
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Card Reader Connector		
Size: A3	Document Number: Big Bear 2A	Rev: SD
Date: Monday, October 27, 2008	Sheet 32 of 55	


U52
BCM5764MKMLG-GP
71.05764.M01
-1_1014
SD_0902
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R349 change to Bead
for Transmitter Distortion
U59
AT45DB011D-SH-T-GP
72.45011.B01
Q24
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
X5
XTAL-25MHZ-113-GP
82.30020.971
2ND = 82.30020.851
RN71
SRN1KJ-10-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5764MKMLG
Big Bear 2A
Monday, October 27, 2008
Sheet 33 of 55

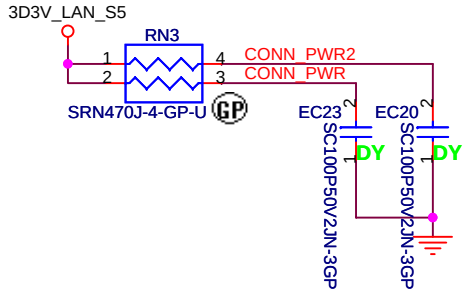
LAN Connector

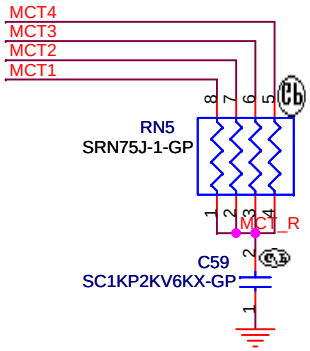




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

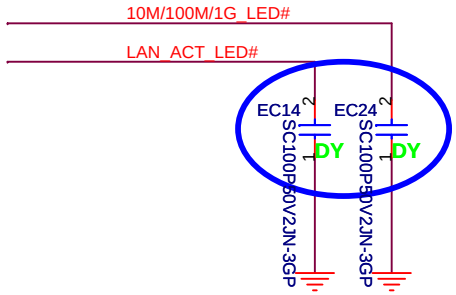
LAN Data: Yellow(B2), when LAN is transfering data.





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

Size	Document Number	Rev
A4	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 34 of 55

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

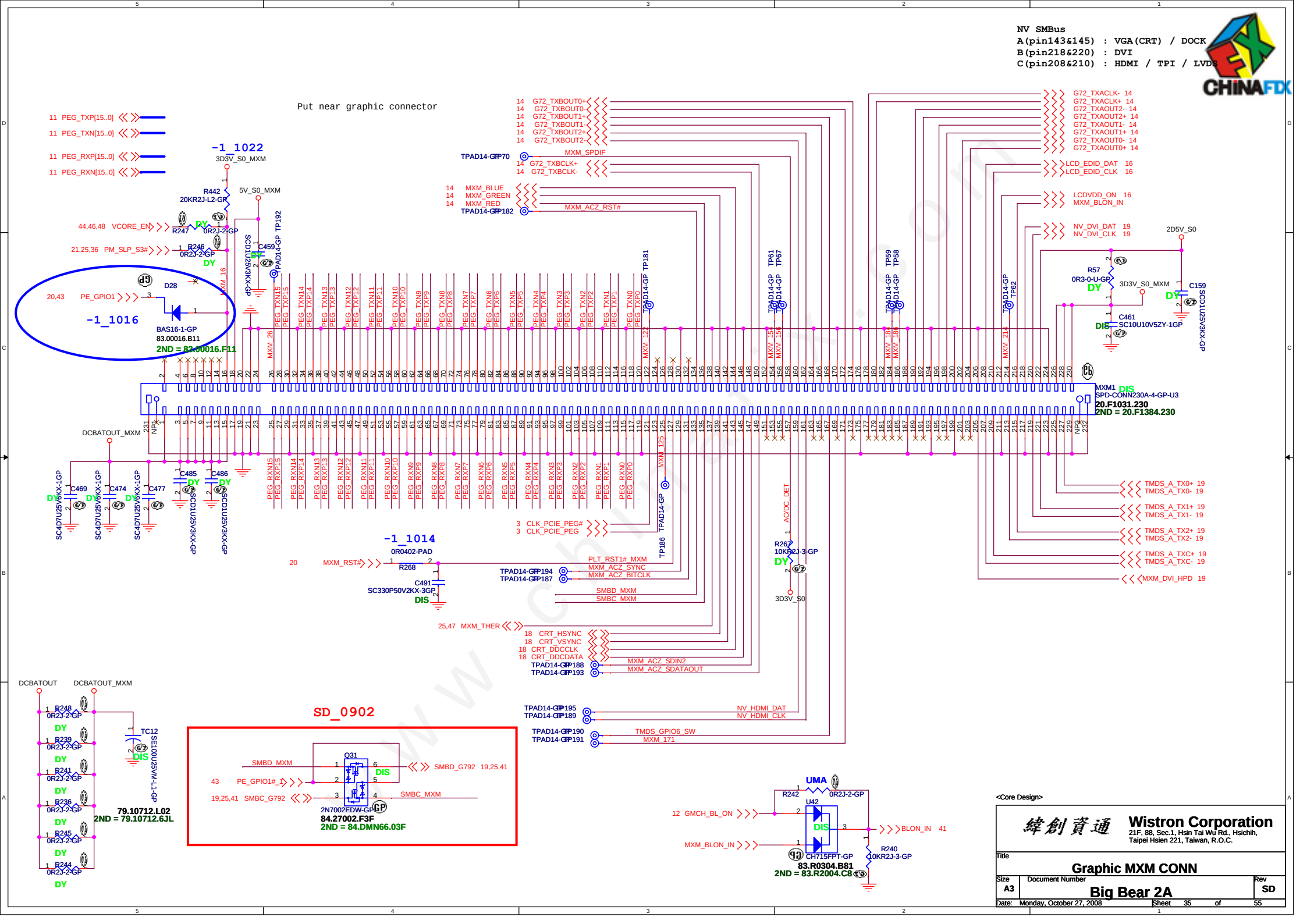
Put near graphic connector

-1_1022

-1_1016

-1_1014

SD_0902



<Core Design>

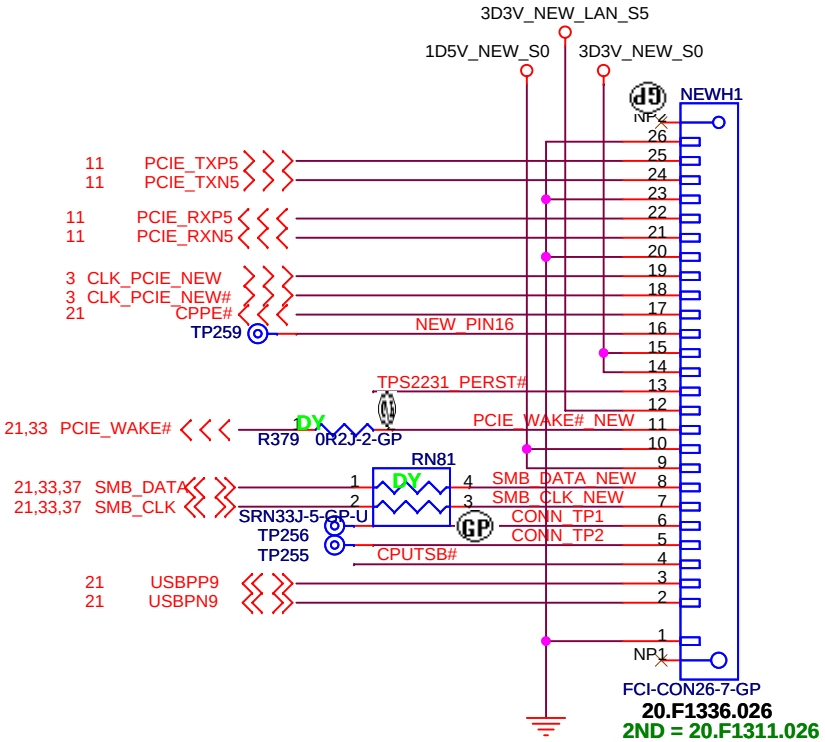
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

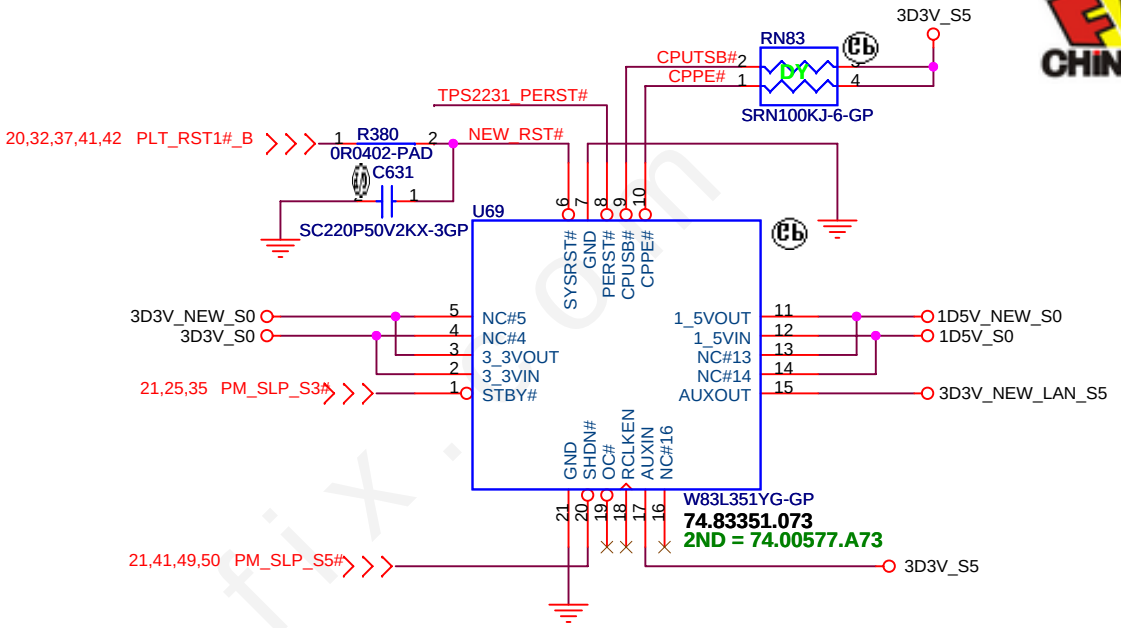
Title: Graphic MXM CONN

Size: A3 | Document Number: Big Bear 2A | Rev: SD

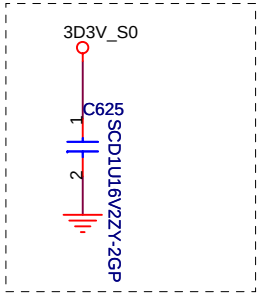
Date: Monday, October 27, 2008 | Sheet 35 of 55

NEWCARD Connector

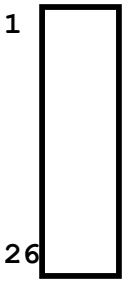


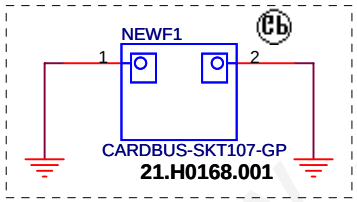


Place them Near to Chip

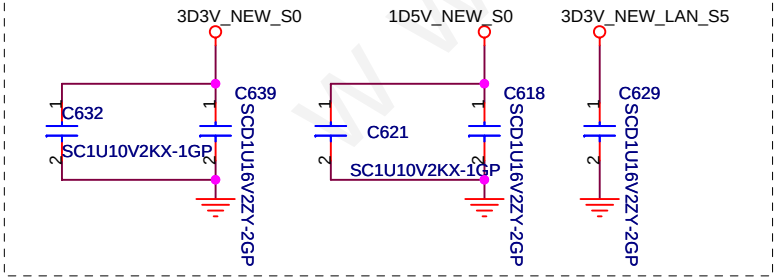


TOP VIEW





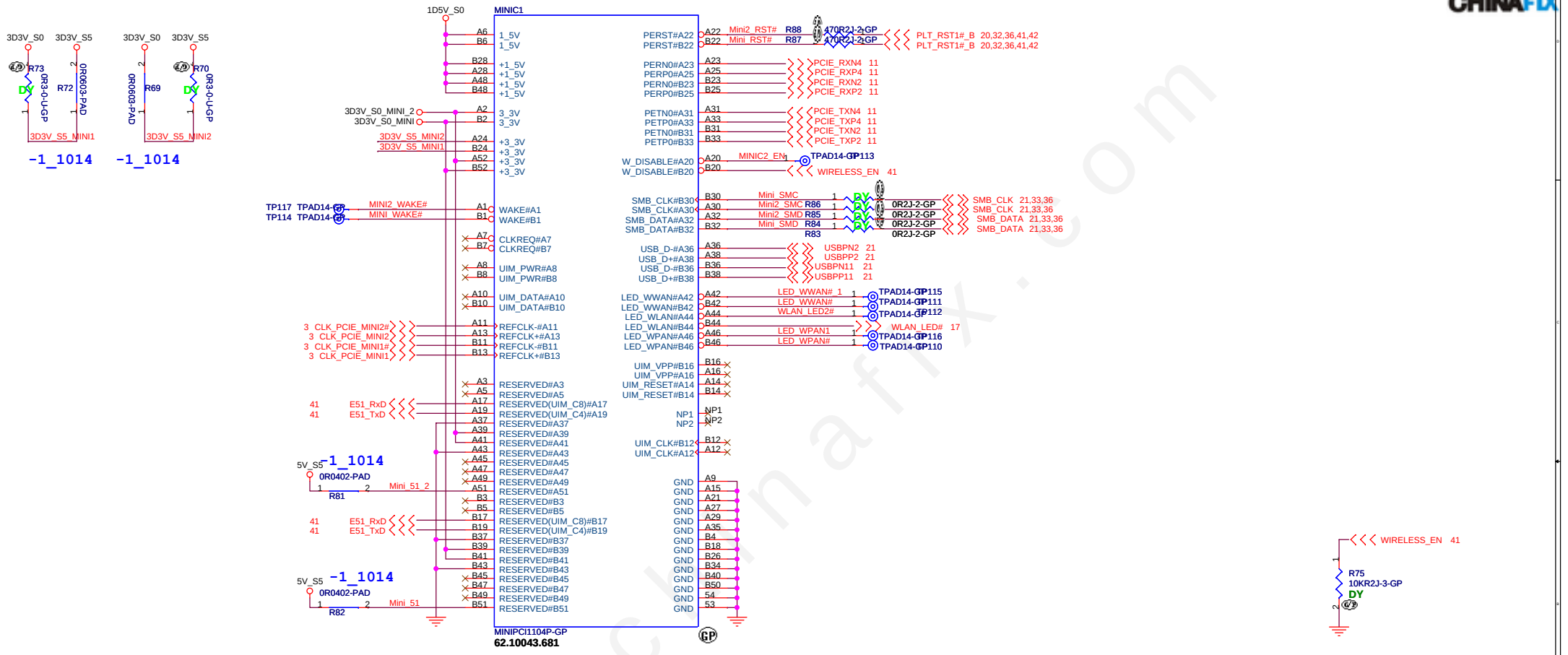
Place them Near to Connector



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	NEW CARD	
Size: A4	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 36 of 55	

Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT



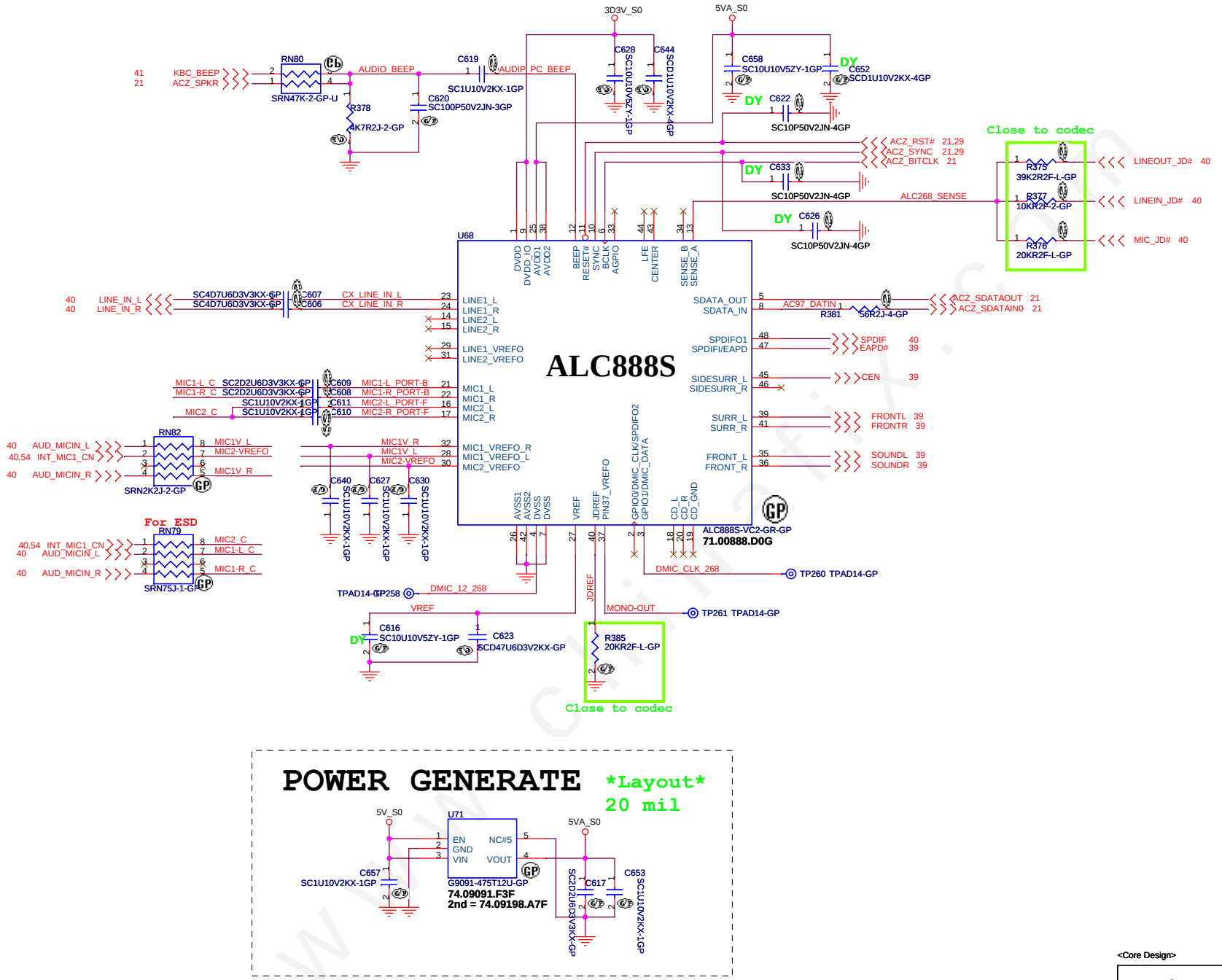
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 37 of 55



<Core Design>

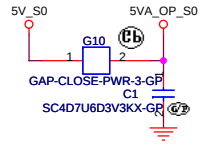
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

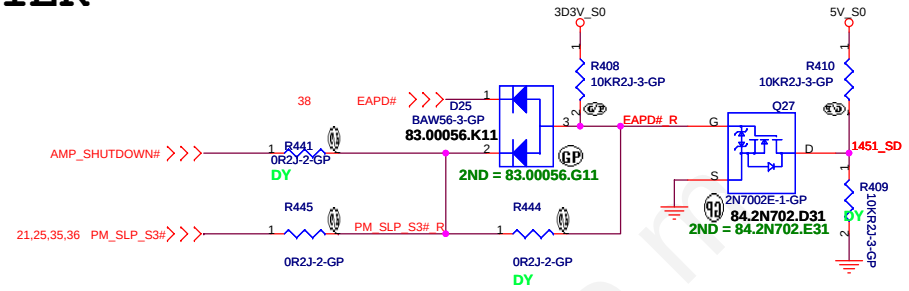
Title: ***Azalia codec ALC268***

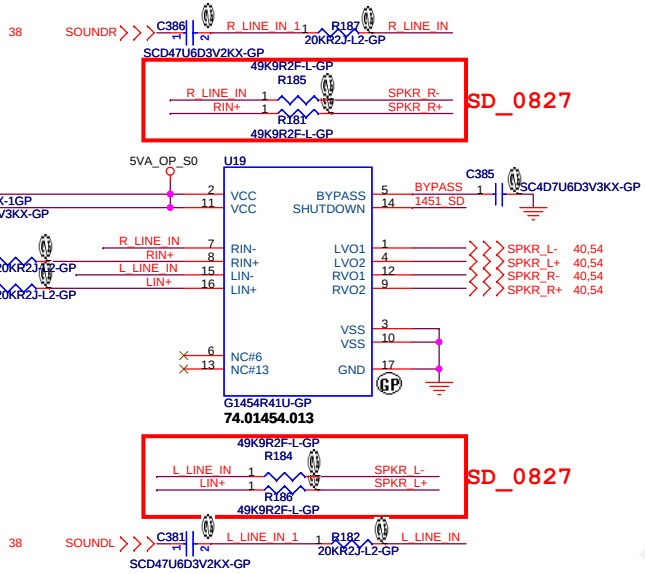
Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 38 of 55

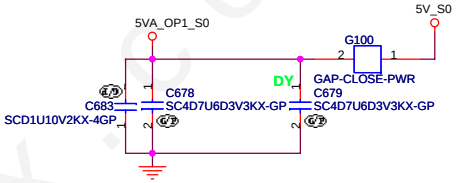
AUDIO OP AMPLIFIER

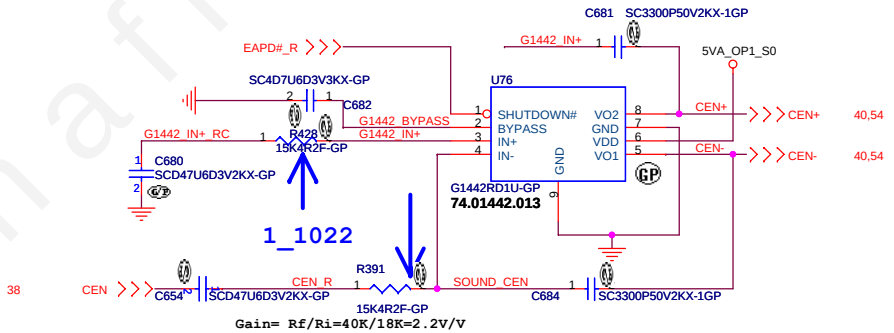






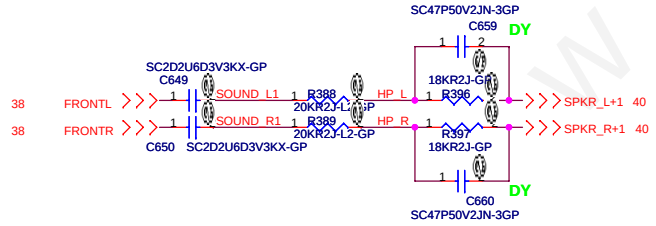
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W



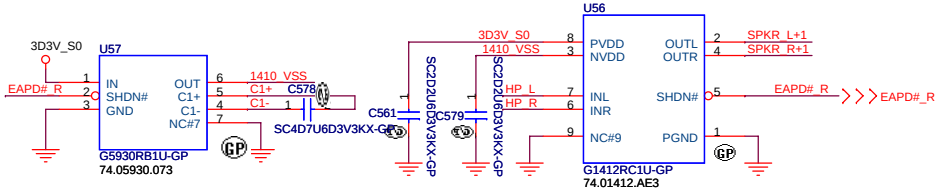


Gain= Rf/Ri=40K/18K=2.2V/V
f(HP)=1/(2 Pi*18K*0.47uf)=18Hz
If VIN= 1.54V Gain=2.2V/V RL=4Ω VO(peak) =3.38V V(rms)=2.390V
Power= 2.390^2/4=1.428W

KBC_MUTE_GPIO8



Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?



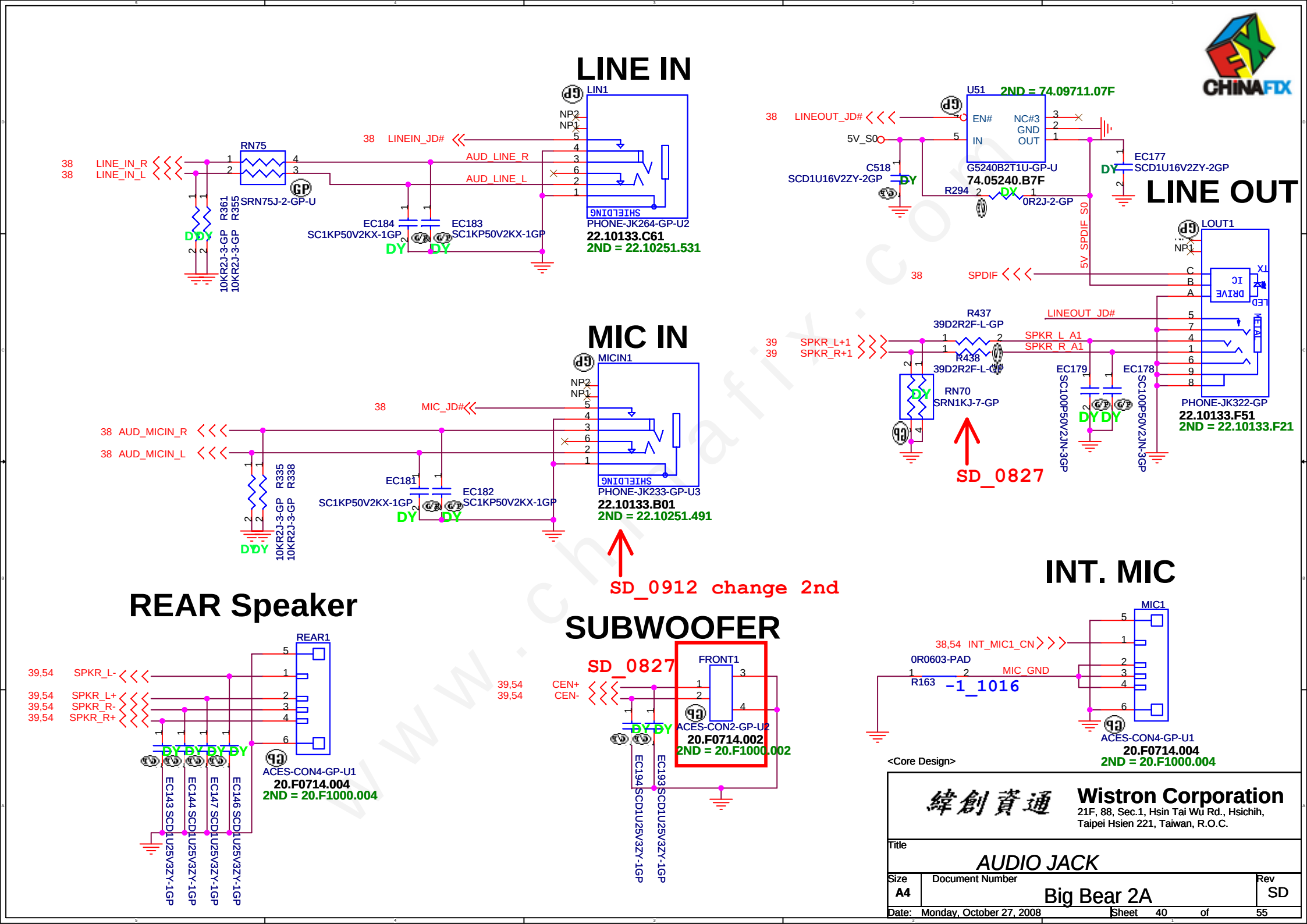
<Core Design>

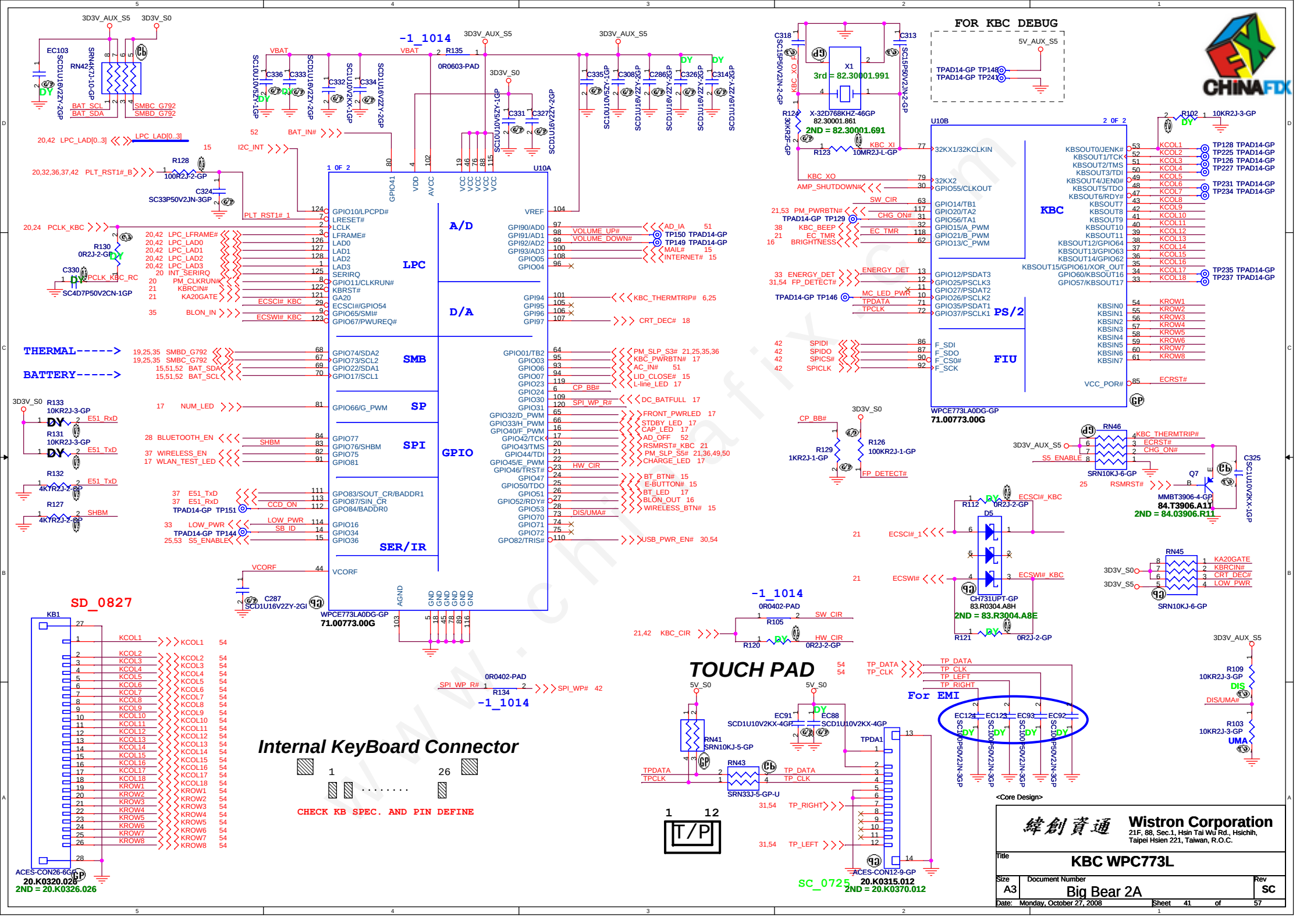
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

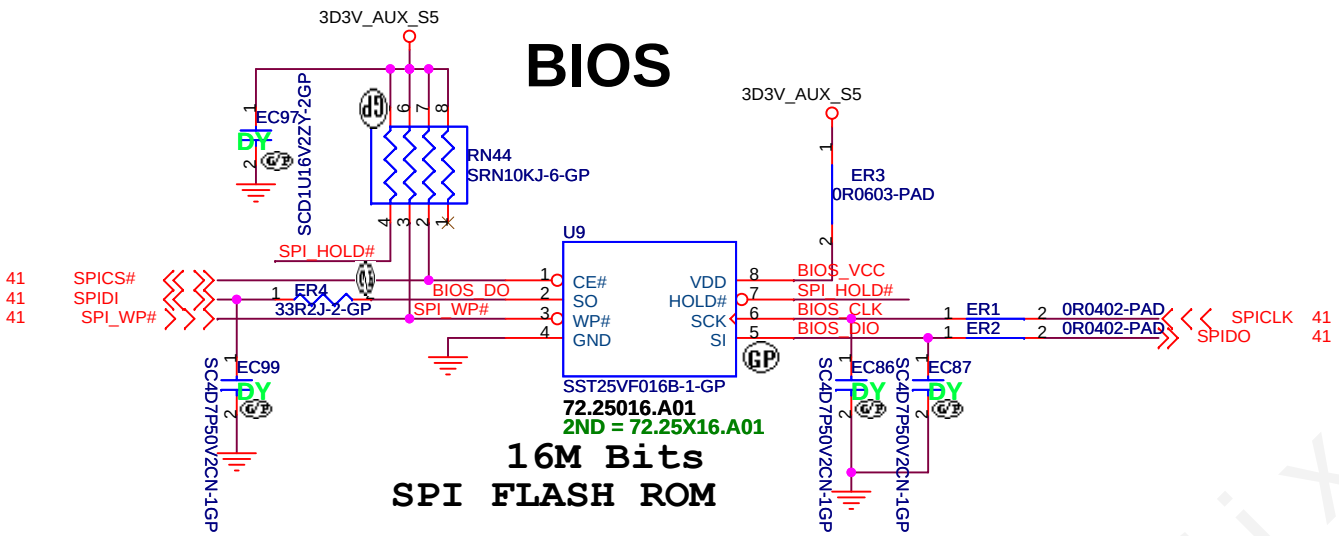
Title: AUDIO AMP

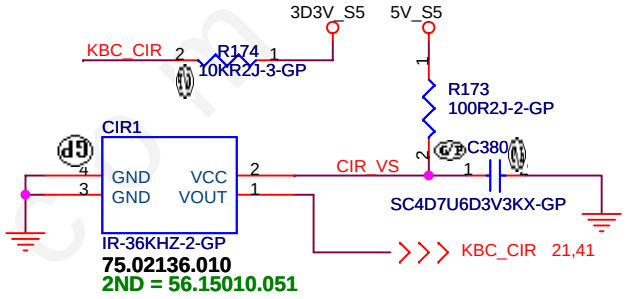
Size: A3 | Document Number: Big Bear 2A | Rev: SB

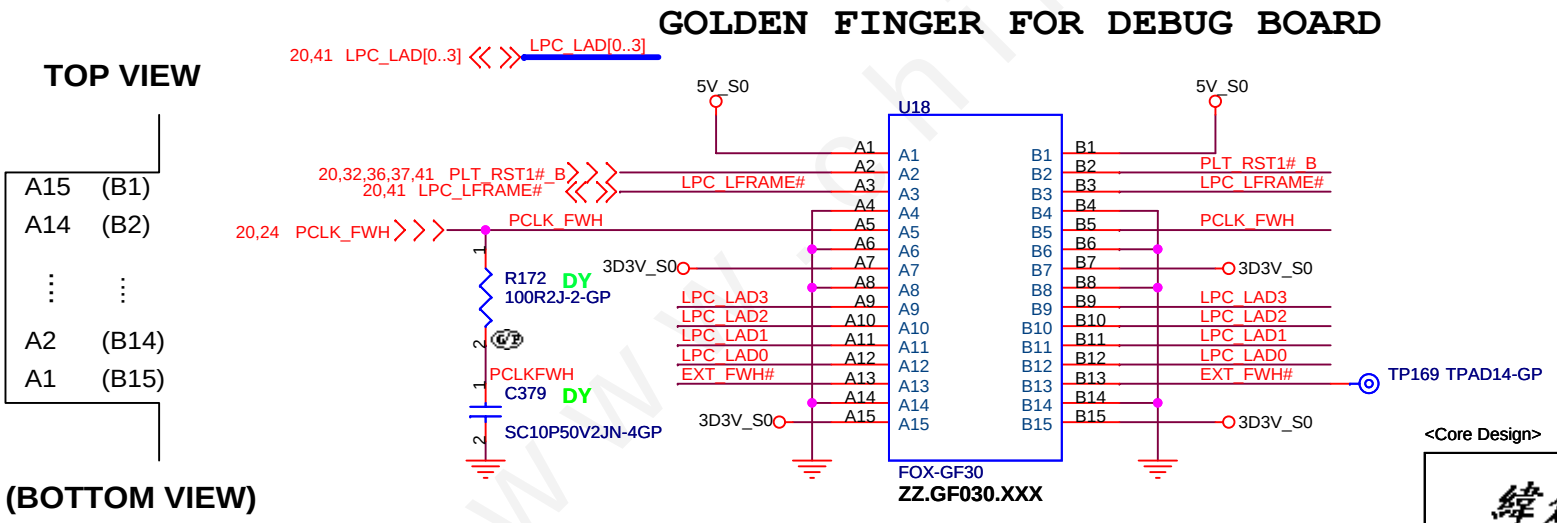
Date: Monday, October 27, 2008 | Sheet 39 of 55


LINE IN
LIN1
NP2
NP1
38 LINEIN_JD#
AUD_LINE_R
AUD_LINE_L
38 LINE_IN_R
38 LINE_IN_L
RN75
SRN75J-2-GP-U
R361
R355
10KR2J-3-GP
10KR2J-3-GP
EC184
SC1KP50V2KX-1GP
EC183
SC1KP50V2KX-1GP
SHIELDING
PHONE-JK264-GP-U2
22.10133.C61
2ND = 22.10251.531
U51
2ND = 74.09711.07F
38 LINEOUT_JD#
5V_S0
EN#
NC#3
GND
OUT
IN
G5240B2T1U-GP-U
74.05240.B7F
C518
SCD1U16V2ZY-2GP
R294
0R2J-2-GP
EC177
SCD1U16V2ZY-2GP
LINE OUT
5V SPDIF S0
LOUT1
38 SPDIF
MIC IN
MICIN1
38 MIC_JD#
38 AUD_MICIN_R
38 AUD_MICIN_L
R335
R338
10KR2J-3-GP
10KR2J-3-GP
EC181
SC1KP50V2KX-1GP
EC182
SC1KP50V2KX-1GP
PHONE-JK233-GP-U3
22.10133.B01
2ND = 22.10251.491
R437
39D2R2F-L-GP
R438
39D2R2F-L-GP
39 SPKR_L+1
39 SPKR_R+1
SPKR_L_A1
SPKR_R_A1
LINEOUT_JD#
RN70
SRN1KJ-7-GP
EC179
SC100P50V2JN-3GP
EC178
SC100P50V2JN-3GP
PHONE-JK322-GP
22.10133.F51
2ND = 22.10133.F21
SD_0827
SD_0912 change 2nd
REAR Speaker
REAR1
39,54 SPKR_L-
39,54 SPKR_L+
39,54 SPKR_R-
39,54 SPKR_R+
EC143 SCD1U25V3ZY-1GP
EC144 SCD1U25V3ZY-1GP
EC147 SCD1U25V3ZY-1GP
EC146 SCD1U25V3ZY-1GP
ACES-CON4-GP-U1
20.F0714.004
2ND = 20.F1000.004
SUBWOOFER
SD_0827
FRONT1
39,54 CEN+
39,54 CEN-
EC194 SCD1U25V3ZY-1GP
EC193 SCD1U25V3ZY-1GP
ACES-CON2-GP-U2
20.F0714.002
2ND = 20.F1000.002
INT. MIC
MIC1
38,54 INT_MIC1_CN
0R0603-PAD
R163
-1_1016
MIC_GND
ACES-CON4-GP-U1
20.F0714.004
2ND = 20.F1000.004
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO JACK
Size
A4
Document Number
Big Bear 2A
Rev
SD
Date: Monday, October 27, 2008
Sheet 40 of 55


FOR KBC DEBUG
KBC WPC773L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Big Bear 2A
Monday, October 27, 2008
Internal KeyBoard Connector
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
For EMI
SD_0827
THERMAL----->
BATTERY----->
KBC
PS/2
FIU
GPIO
A/D
D/A
LPC
SMB
SP
SPI
SER/IR
WPCE773LA0DG-GP
71.00773.00G
CHINAFDX



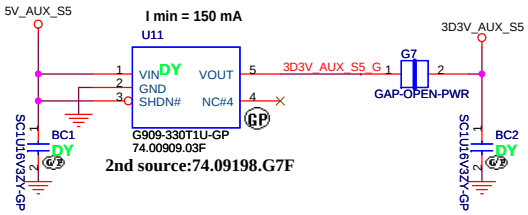




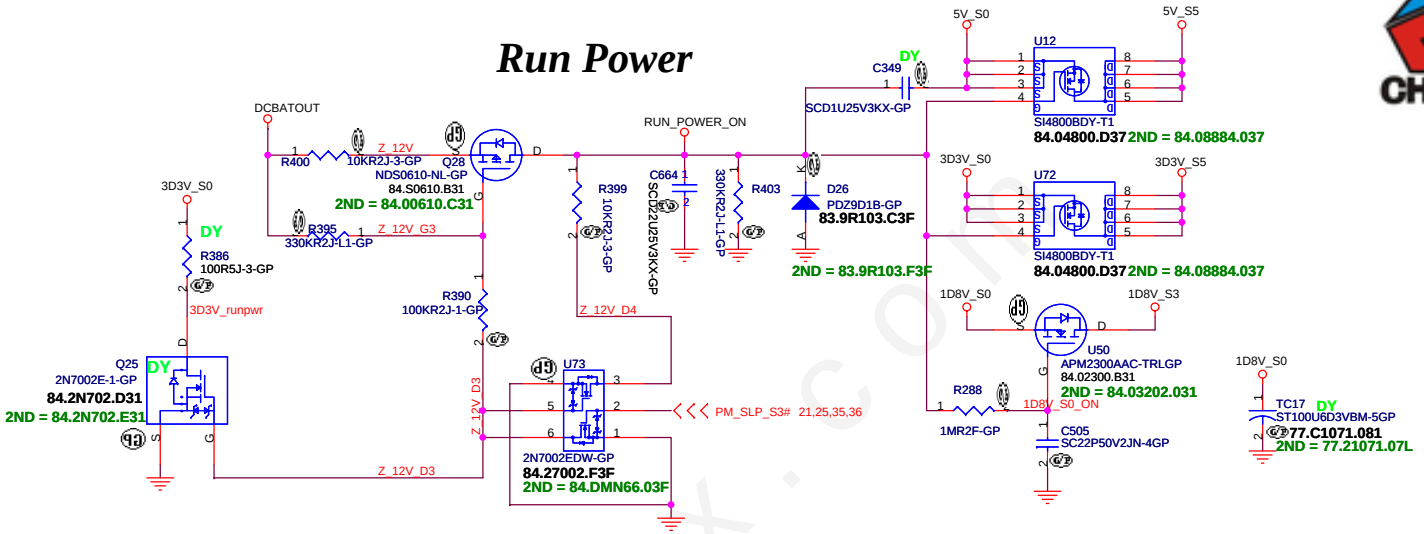
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS & CIR***	
Size: A4	Document Number: **Big Bear 2A**	Rev: SB
Date: Monday, October 27, 2008	Sheet 42 of 57	

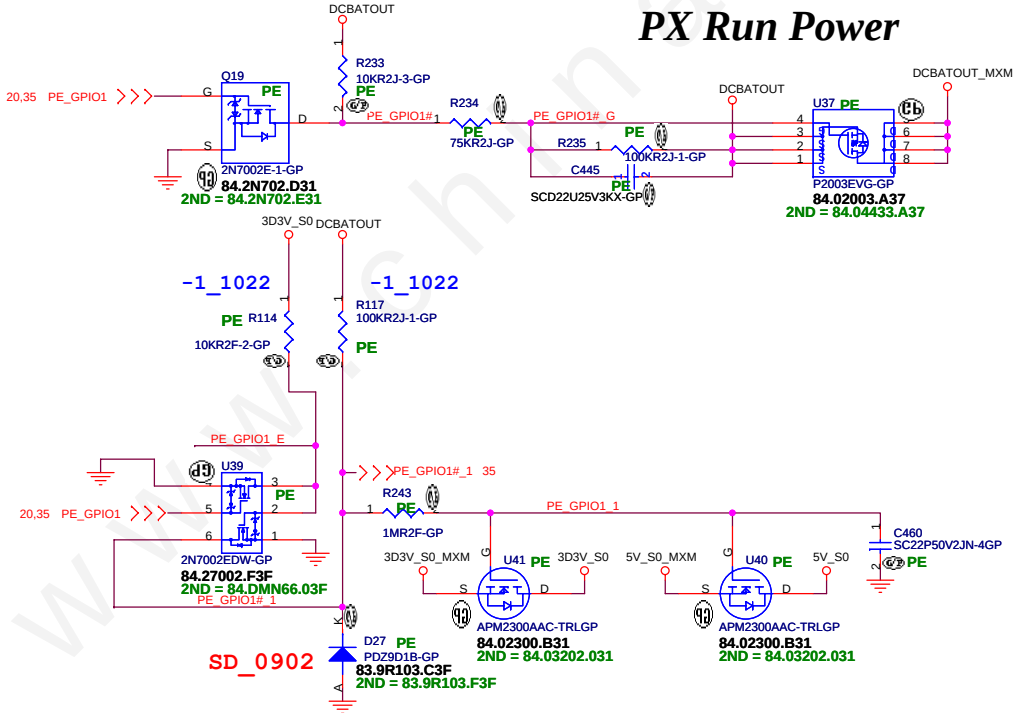
Aux Power 3D3V_AUX_S5



Run Power

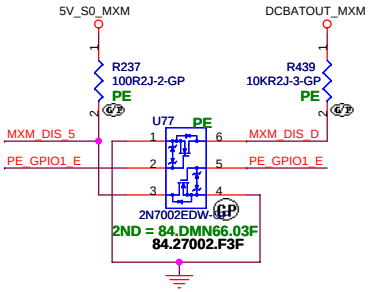


PX Run Power



SD_0902

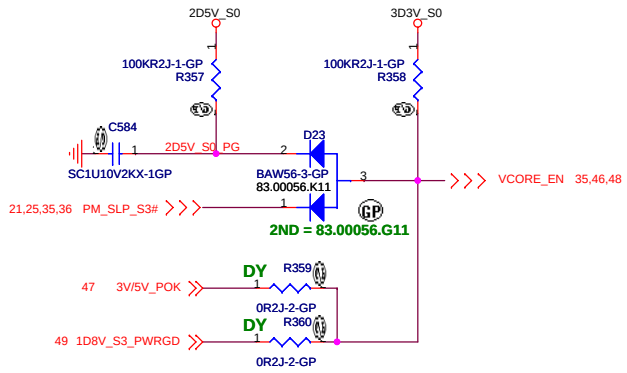
PX Run Power Discharge circuit



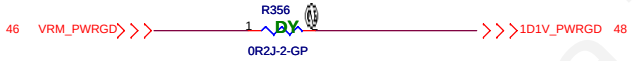
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

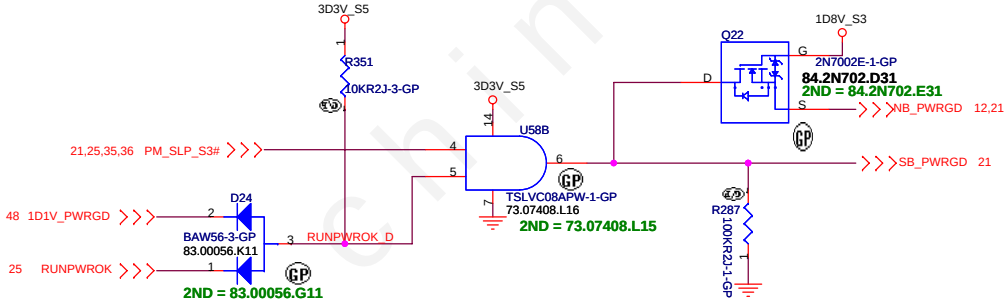
Title	RUN POWER and 3D3V_AUX_S5	
Size A3	Document Number Big Bear 2A	Rev SD
Date: Monday, October 27, 2008	Sheet 43 of 57	



P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

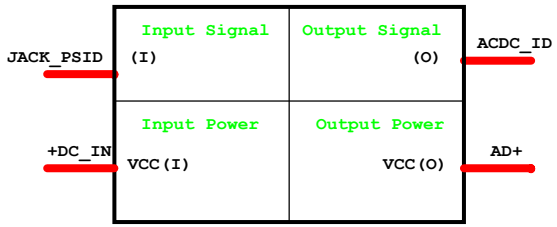
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

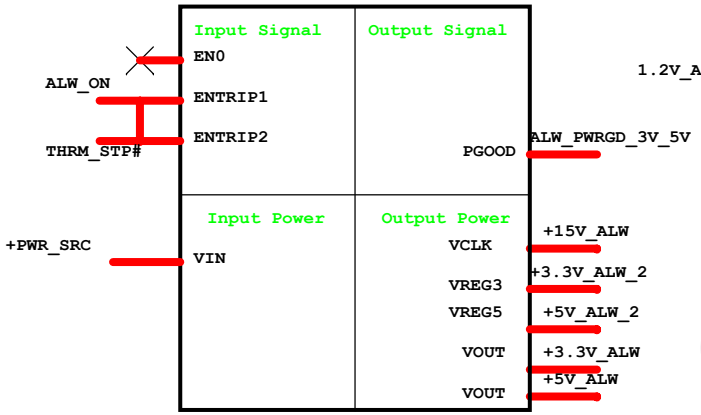
Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 44 of 57

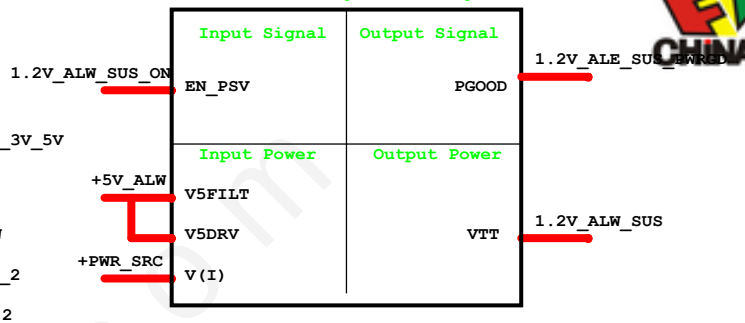
Adapter



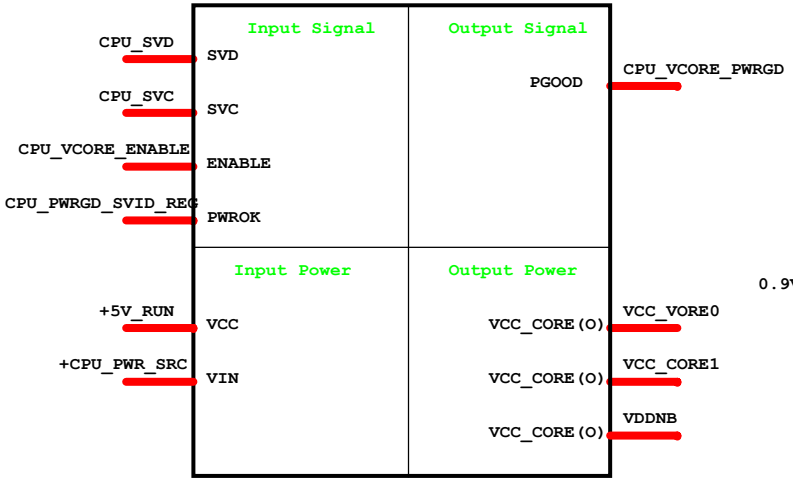
SN0608098



DCDC 1D2V(TPS5117)

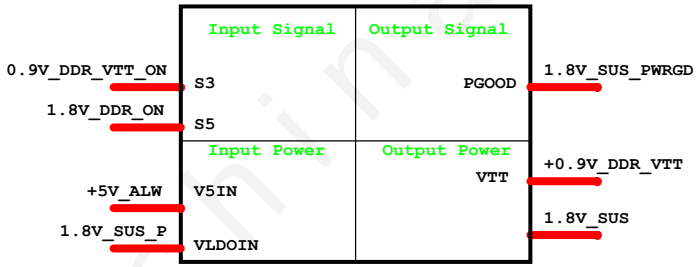


CPU_CORE
ISL6265HRTZ

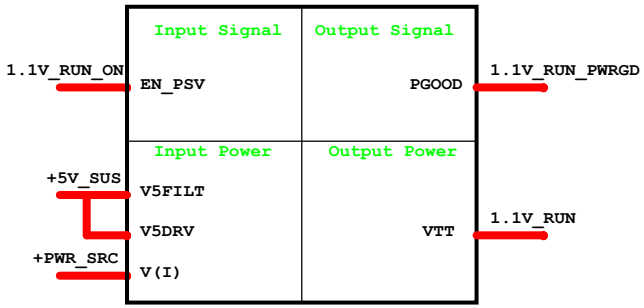


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

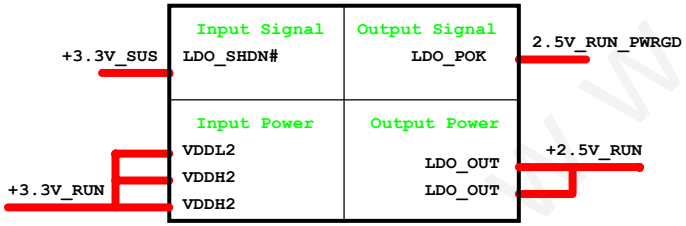
1D8V/0D9V(TPS5116)



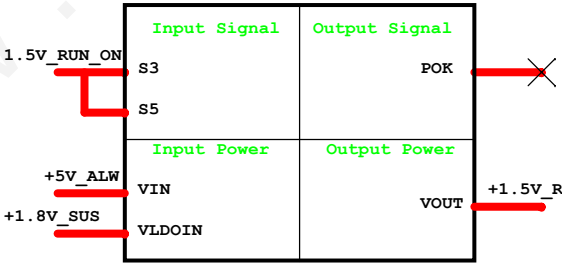
1D1V(TPS5117)



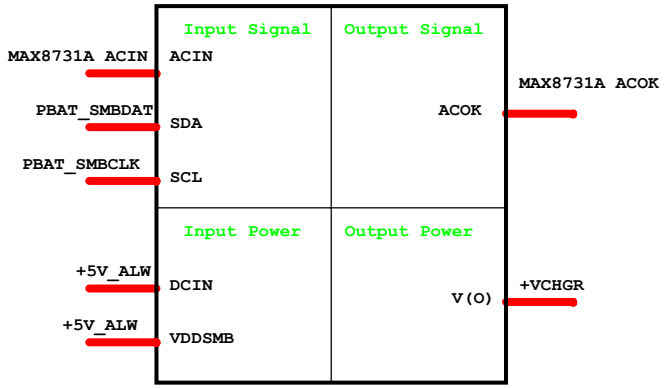
2.5V LDO
EMC4002



1.5V_LDO



CHARGER BQ24745



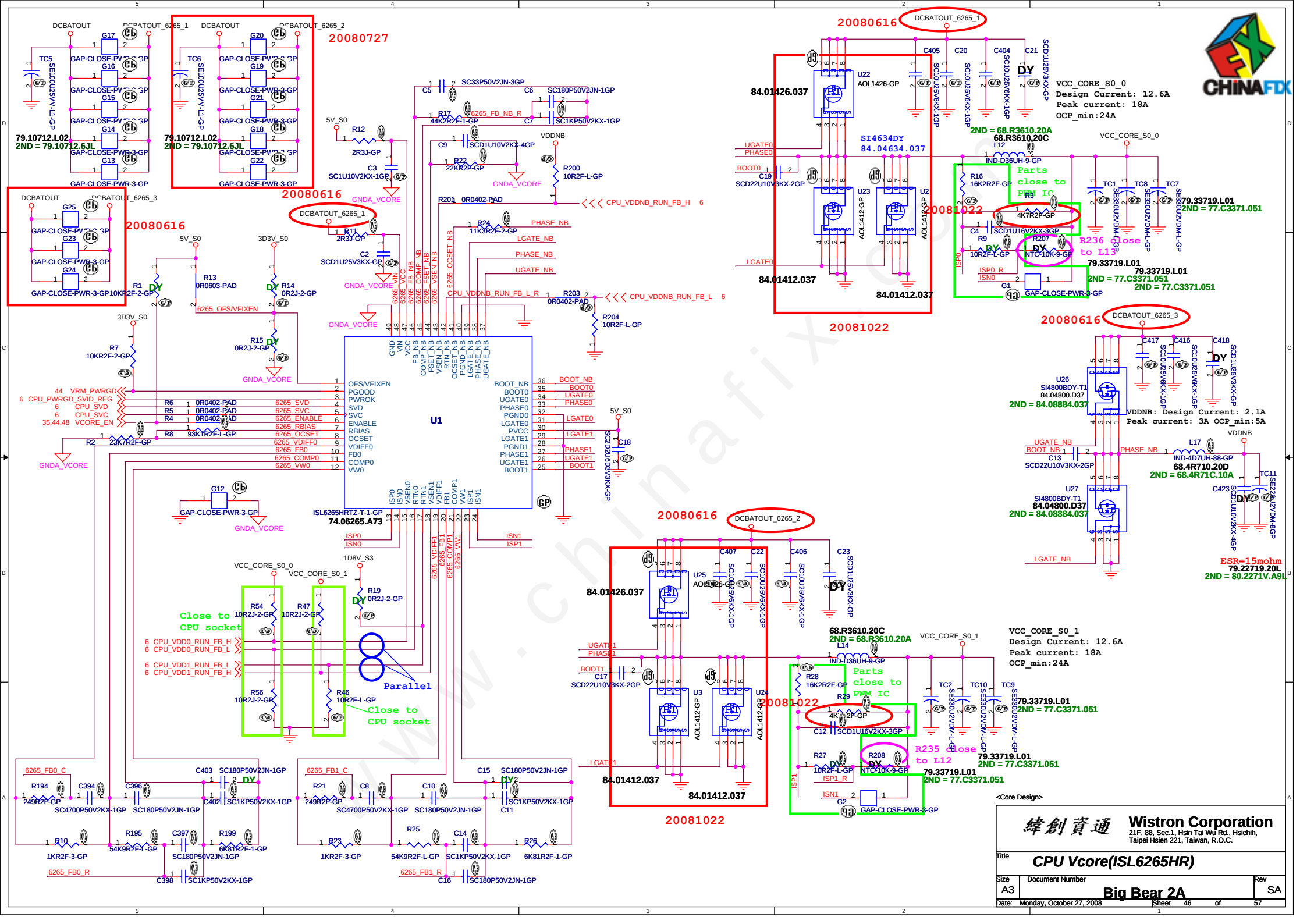
<Core Design>

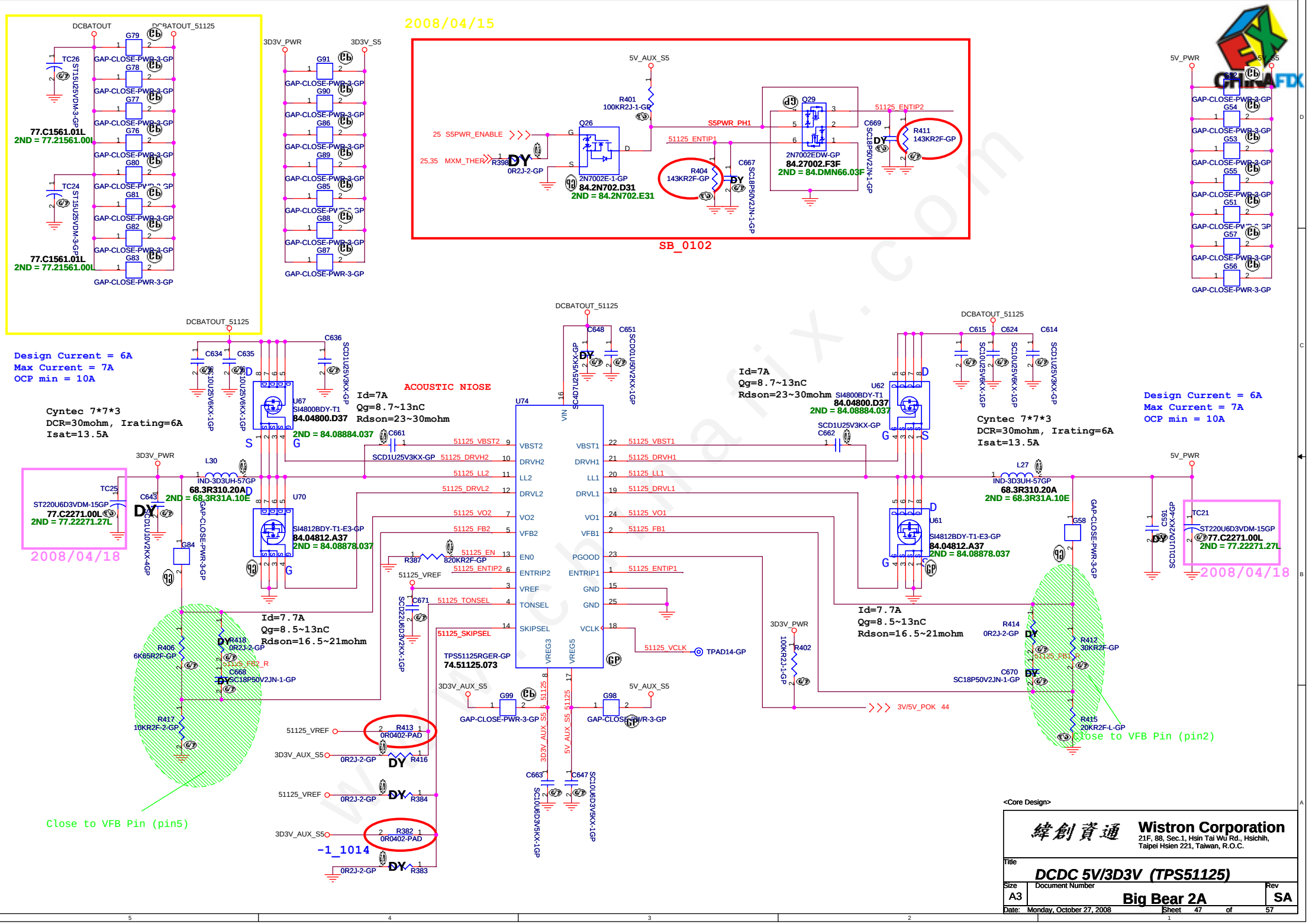
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

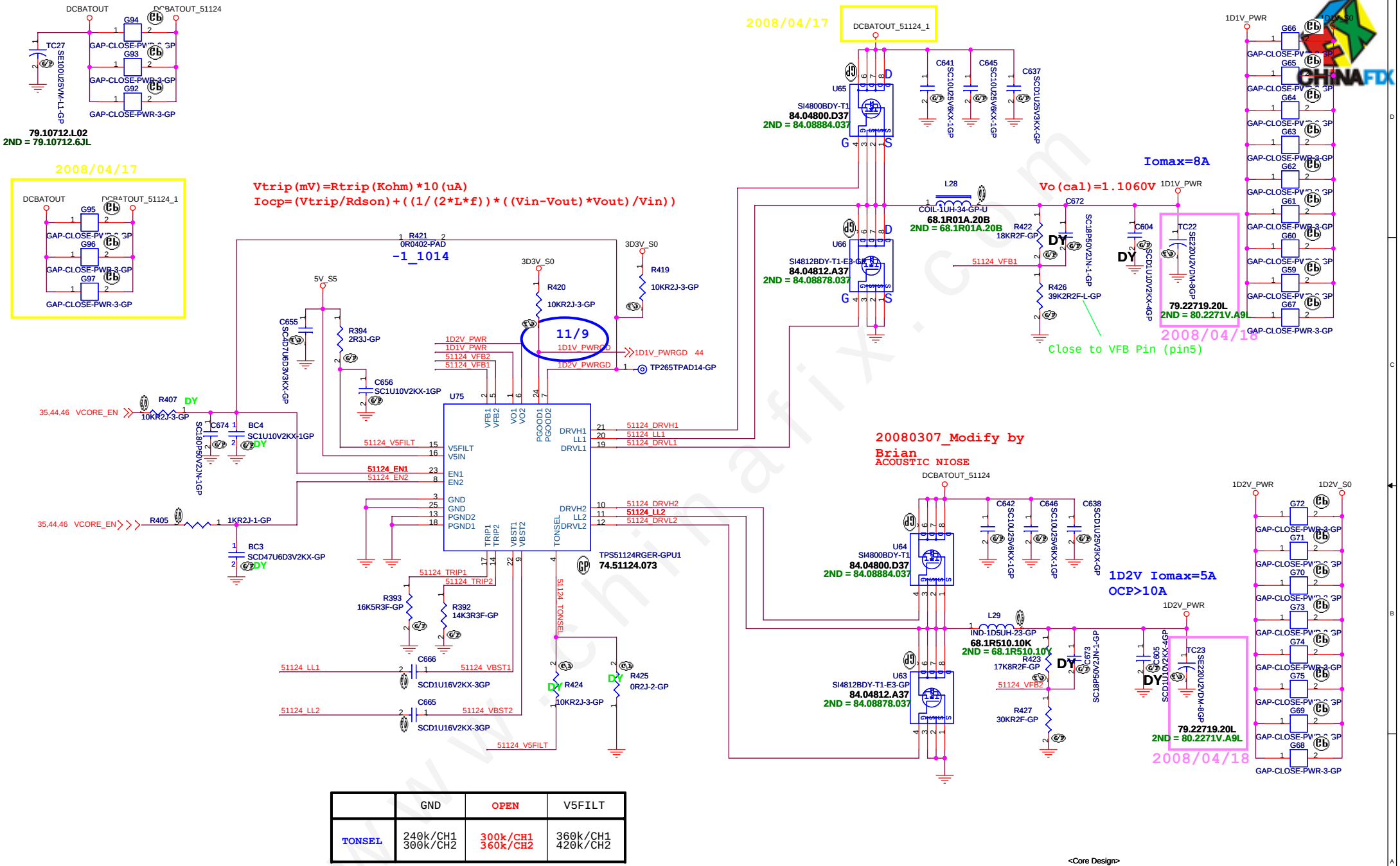
Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 45 of 57


20080727
20080616
20081022
U1
ISL6265HRTZ-T-1-GP
74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Close to CPU socket
Parallel
Parts close to PWM IC
R235 close to L12
R236 close to L13
ESR=15mohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Big Bear 2A
Monday, October 27, 2008
Sheet 46 of 57


2008/04/15
SB_0102
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
ACOUSTIC NIOSE
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
TPS51125RGER-GP
74.51125.073
-1_1014
2008/04/18
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2A
Monday, October 27, 2008
Sheet 47 of 57



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

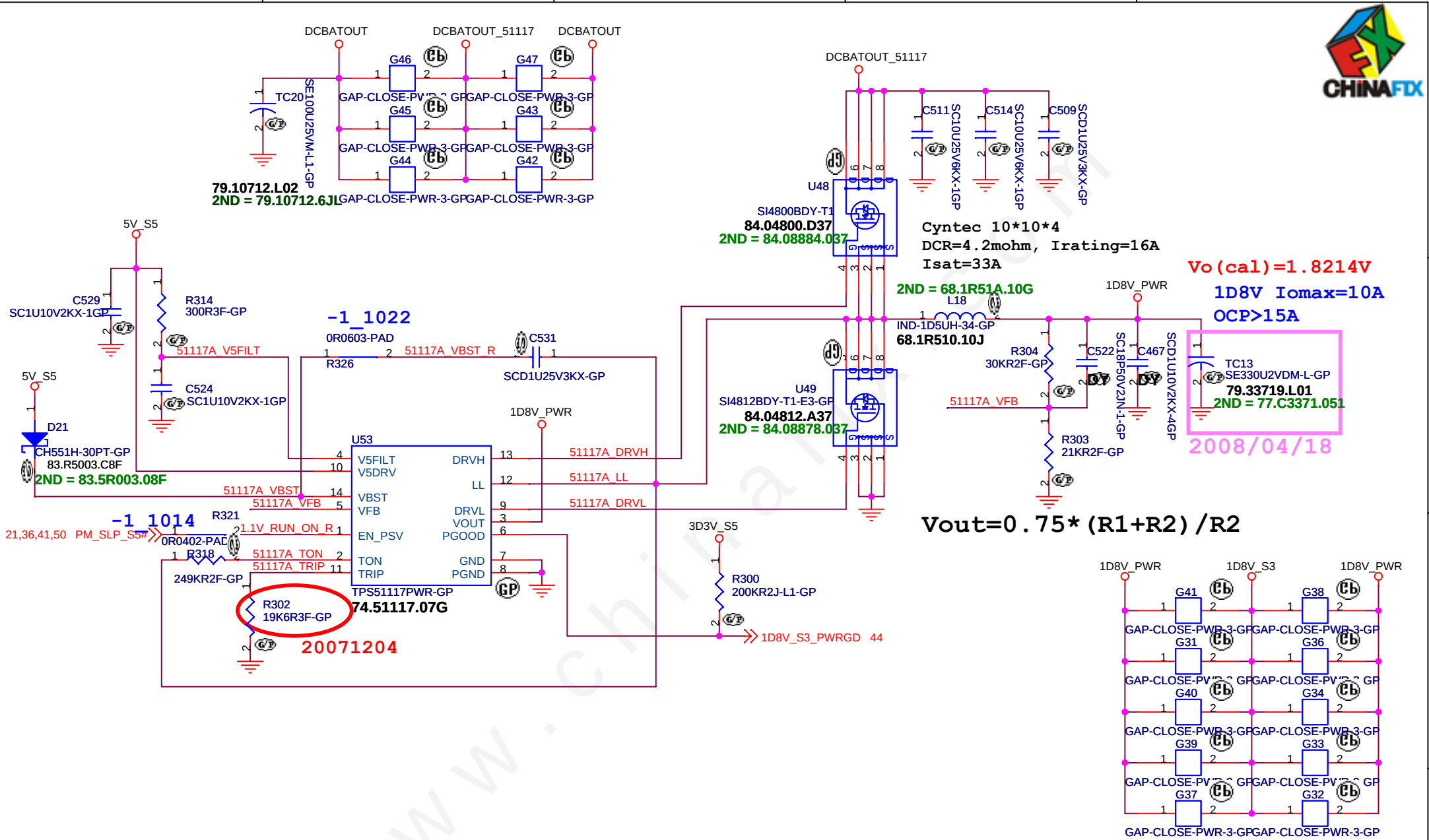
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 48 of 57



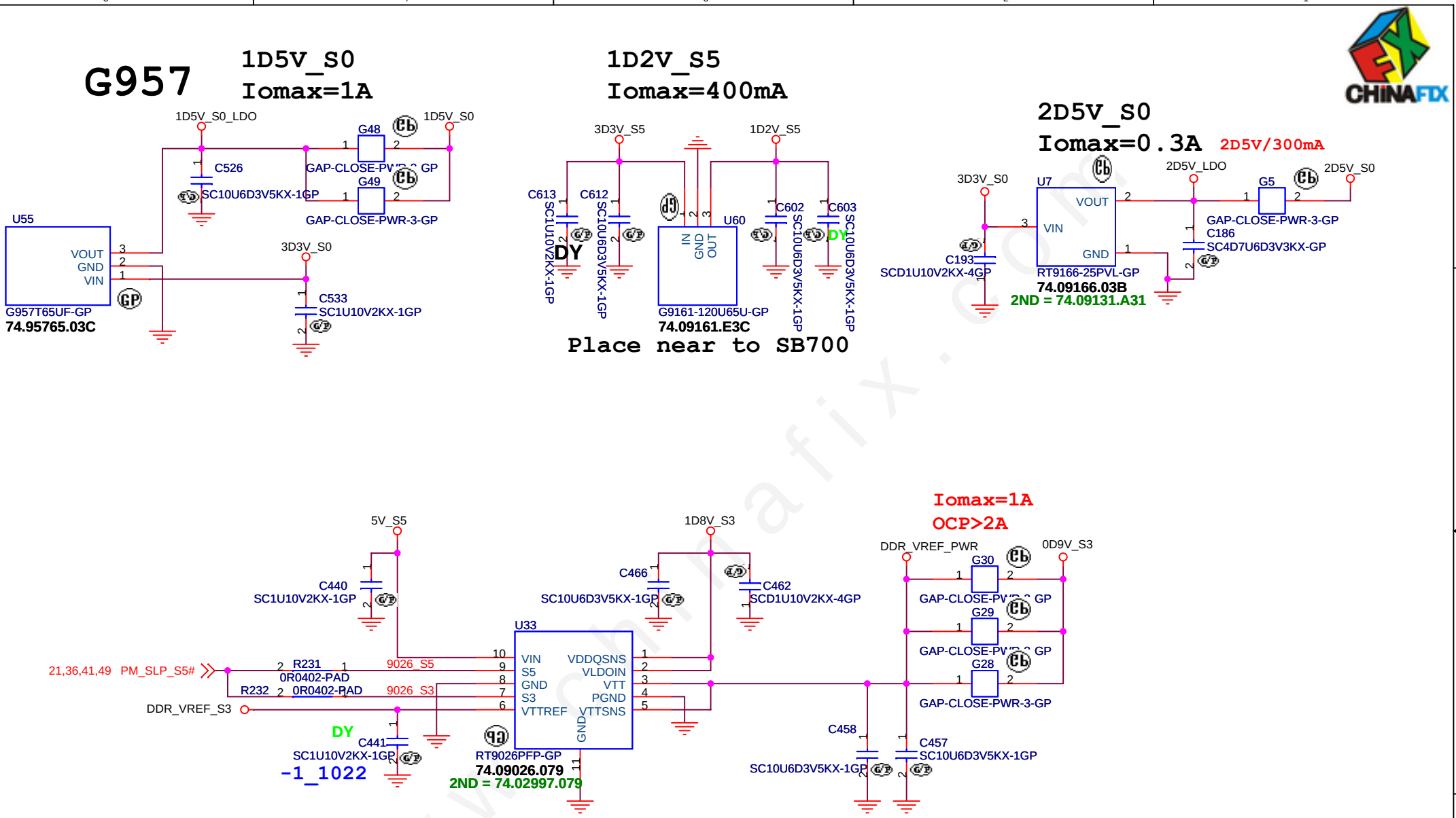
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V(TPS5117)*

Size	Document Number	Rev
A4	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 49 of 57



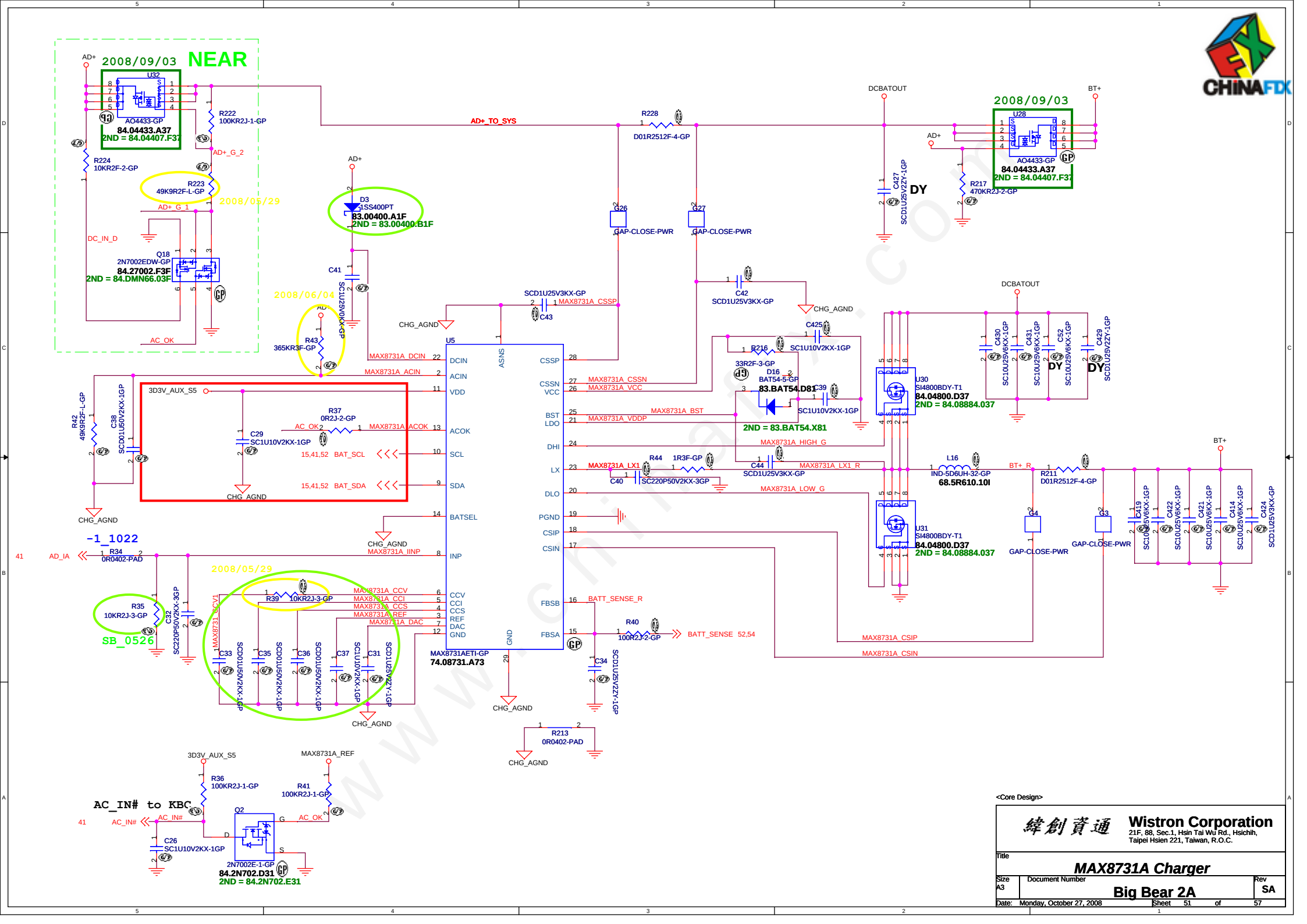
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

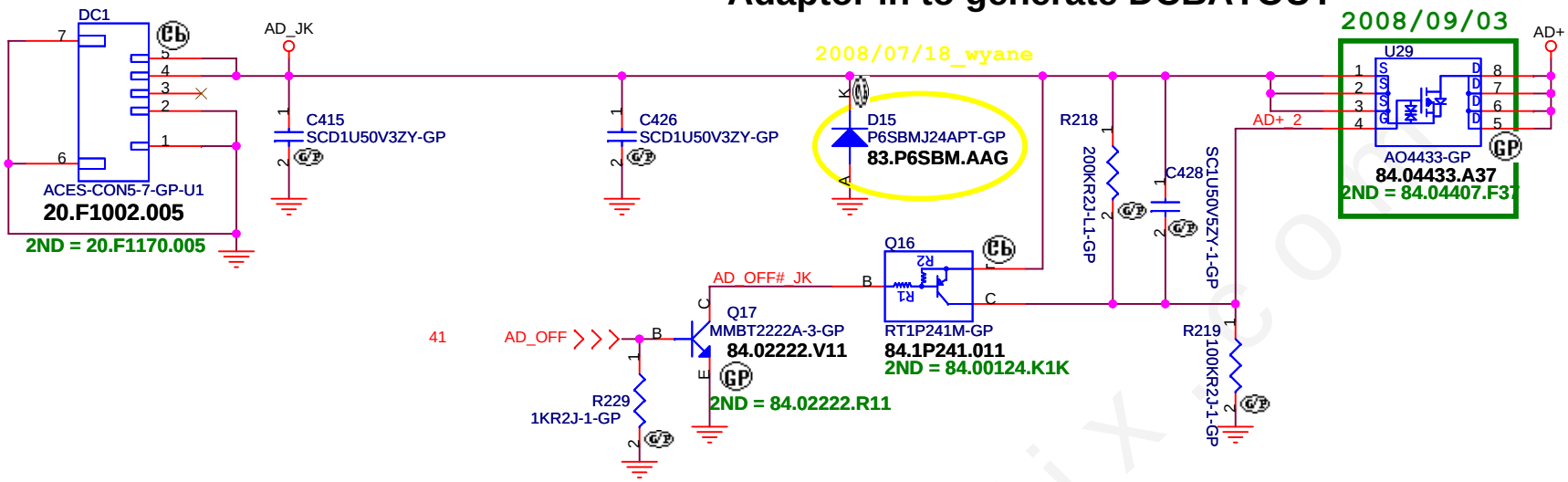
Title: ***0D9V&2D5V&1D25V&1D5V***

Size	Document Number	Rev
A4	Big Bear 2A	SB

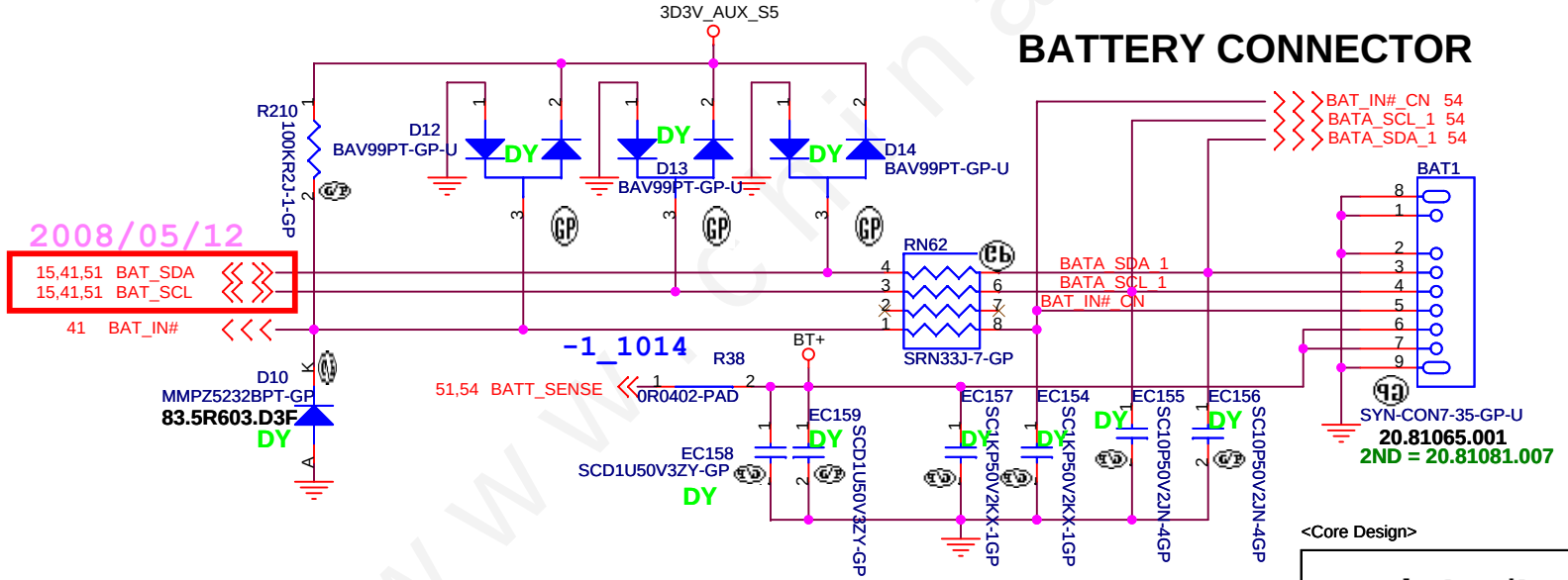
Date: Monday, October 27, 2008 Sheet 50 of 57


2008/09/03 NEAR
U32
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R222 100KR2J-1-GP
AD+_G_2
R224 10KR2F-2-GP
R223 49K9R2F-L-GP
2008/05/29
AD+_G_1
DC_IN_D
Q18
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
AC_OK
AD+
AD+_TO_SYS
R228 D01R2512F-4-GP
DCBATOUT
BT+
2008/09/03
U28
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R217 470KR2J-2-GP
C427 SCD1U25V2ZY-1GP
DY
D3
1SS400PT
83.00400.A1F
2ND = 83.00400.B1F
2008/06/04
R43 365KR3F-GP
C41 SCD1U25V3KX-GP
G26 GAP-CLOSE-PWR
G27 GAP-CLOSE-PWR
C42 SCD1U25V3KX-GP
C43 SCD1U25V3KX-GP
MAX8731A_CSSP
CHG_AGND
U5
MAX8731AETI-GP
74.08731.A73
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
ASNS
MAX8731A_DCIN
MAX8731A_ACIN
MAX8731A_ACOK
MAX8731A_IINP
MAX8731A_CCV
MAX8731A_CCI
MAX8731A_CCS
MAX8731A_REF
MAX8731A_DAC
MAX8731A_CSSN
MAX8731A_VCC
MAX8731A_VDDP
MAX8731A_BST
MAX8731A_HIGH_G
MAX8731A_LX1
MAX8731A_LX1_R
MAX8731A_LOW_G
MAX8731A_CSIP
MAX8731A_CSIN
BATT_SENSE_R
BATT_SENSE 52,54
3D3V_AUX_S5
R42 49K9R2F-L-GP
C38 SCD01U50V2KX-1GP
R37 0R2J-2-GP
C29 SC1U10V2KX-1GP
AC_OK
15,41,52 BAT_SCL
15,41,52 BAT_SDA
R216 33R2F-3-GP
C425 SC1U10V2KX-1GP
D16 BAT54-5-GP
83.BAT54.D81
2ND = 83.BAT54.X81
C39 SC1U10V2KX-1GP
U30 SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U31 SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
C430 SC10U25V6KX-1GP
C431 SC10U25V6KX-1GP
C52 SC10U25V6KX-1GP
C429 SCD1U25V2ZY-1GP
DY
L16 IND-5D6UH-32-GP
68.5R610.10I
R44 1R3F-GP
C44 SCD1U25V3KX-GP
C40 SC220P50V2KX-3GP
R211 D01R2512F-4-GP
G4 GAP-CLOSE-PWR
G3 GAP-CLOSE-PWR
C419 SC10U25V6KX-1GP
C422 SC10U25V6KX-1GP
C421 SC10U25V6KX-1GP
C414 SC10U25V6KX-1GP
C424 SCD1U25V3KX-GP
-1_1022
AD_IA
R34 0R0402-PAD
2008/05/29
R35 10KR2J-3-GP
SB_0526
C32 SC220P50V2KX-3GP
R39 10KR2J-3-GP
C33 SCD01U50V2KX-1GP
C35 SCD01U50V2KX-1GP
C36 SCD01U50V2KX-1GP
C37 SC1U10V2KX-1GP
C31 SCD1U25V2ZY-1GP
C34 SCD1U25V2ZY-1GP
R40 100R2J-2-GP
R213 0R0402-PAD
AC_IN# to KBC
R36 100KR2J-1-GP
R41 100KR2J-1-GP
Q2
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
C26 SC1U10V2KX-1GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAX8731A Charger
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 51 of 57

Adaptor in to generate DCBATOUT

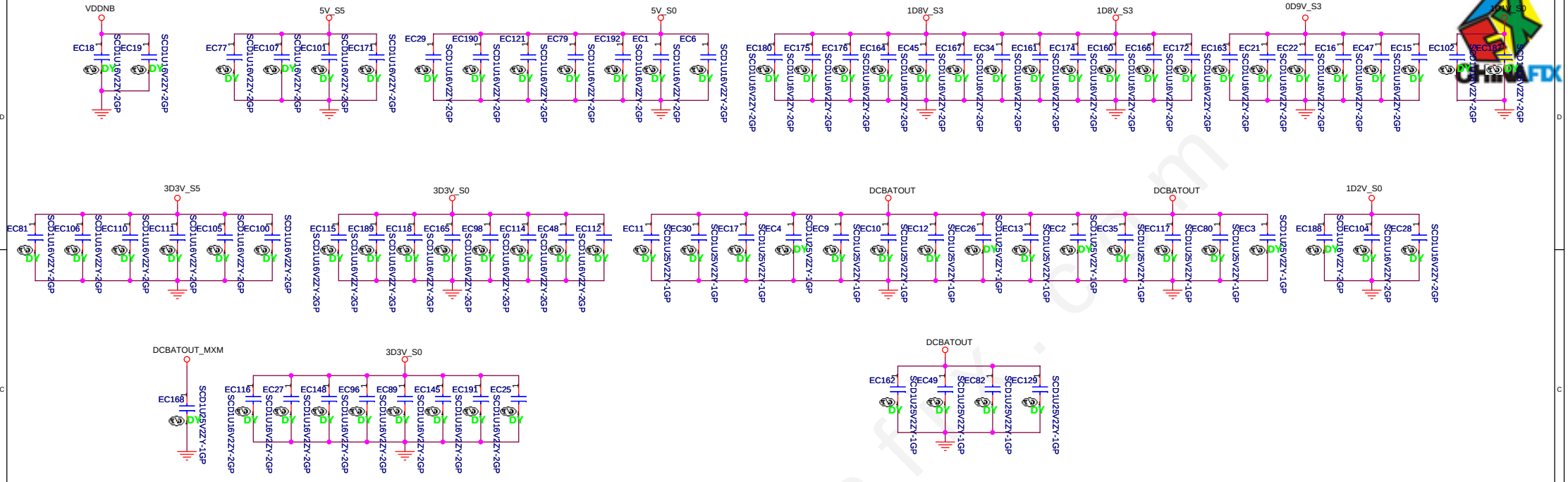


BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size **A4**	Document Number **Big Bear 2A**	Rev SA
Date: Monday, October 27, 2008	Sheet 52 of 57	



SPRING ON BOTTOM

DIMM

GND3 SPRING-62-GP 34.39S07.003 DY
GND1 SPRING-62-GP 34.39S07.003 DY

MXM

S1 SPRING-37-GP-U 34.15F09.001 DY
S2 SPRING-37-GP-U 34.15F09.001 DY
S3 SPRING-37-GP-U 34.15F09.001 DY

SPRING ON TOP

SD_0903

Touch Pad

H30 SPRING-57-GP 34.42T14.002

HDMI

SW2 SPRING-15-GP DY

SB-U15

SW3 SPRING-7 DY
SW4 SPRING-7 DY
SW5 SPRING-7 DY

USB

SW6 SPRING-6 DY
SW7 SPRING-6 DY

Jack

SW8 SPRING-15-GP DY

RN24

SW9 SPRING-7 DY

STAND OFF ON BOTTOM

CPU & NB

H31 HOLE 34.42Y01.011
H32 HOLE 34.42Y01.011
H33 HOLE 34.42Y01.011
H34 HOLE 34.42Y01.011

Mini Card

H19 HOLE 34.4Z402.001
H20 HOLE 34.4Z402.001

MXM

H14 HOLE DIS 34.4Z401.001
H17 HOLE DIS 34.4Z401.001

STAND OFF ON TOP

MDC

H21 HOLE 34.42Y01.011
H22 HOLE 34.42Y01.011

H1 PAD-1P-3-GP
H2 PAD-1P-3-GP
H3 PAD-1P-3-GP
H4 PAD-1P-3-GP
H5 PAD-1P-3-GP
H6 PAD-1P-3-GP
H7 PAD-1P-3-GP
H8 PAD-1P-3-GP
H9 PAD-1P-3-GP
H10 PAD-1P-3-GP
H13 PAD-1P-3-GP
H18 PAD-1P-3-GP
PAD1 PAD-1P-4-GP
H39 PAD-1P-3-GP
H40 PAD-1P-3-GP

Check test point

3D3V_S0	TP263 TPAD14-GP
3D3V_AUX_S5	TP226 TPAD14-GP
3D3V_S5	TP262 TPAD14-GP
5V_S5	TP246 TPAD14-GP
21,41 PM_PWRBTN#	TP253 TPAD14-GP
6,20 CPU_PWRGD	TP141 TPAD14-GP
25,41 S5_ENABLE	TP143 TPAD14-GP
6,20 CPU_LDT_RST#	TP238 TPAD14-GP

Test Point放在Dimm Door打開可量測處

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size: A3 | Document Number: Big Bear 2A | Rev: SD

Date: Monday, October 27, 2008 | Sheet 53 of 57

REAR1

39,40	SPKR_L-	1	TP1	AFTE14P-GP
39,40	SPKR_L+	1	TP2	AFTE14P-GP
39,40	SPKR_R-	1	TP3	AFTE14P-GP
39,40	SPKR_R+	1	TP4	AFTE14P-GP

FRONT1

39,40	CEN+	1	TP162	AFTE14P-GP
39,40	CEN-	1	TP163	AFTE14P-GP

INT. MIC

38,40	INT_MIC1_CN	1	TP5	AFTE14P-GP

EKCN1

	3D3V_AUX_S5	1	TP57	AFTE14P-GP
15	LID_CLOSE#_R	1	TP60	AFTE14P-GP
15	E-BUTTON#_R	1	TP47	AFTE14P-GP

LEDB1

	3D3V_AUX_S5	1	TP55	AFTE14P-GP
	5V_S0	1	TP56	AFTE14P-GP
15	BAT_SCL_R	1	TP179	AFTE14P-GP
15	I2C_INT_R	1	TP173	AFTE14P-GP
15	BAT_SDA_R	1	TP177	AFTE14P-GP

KB1

41	KROW8	1	TP96	AFTE14P-GP
41	KROW6	1	TP103	AFTE14P-GP
41	KROW7	1	TP83	AFTE14P-GP
41	KROW5	1	TP84	AFTE14P-GP
41	KROW4	1	TP104	AFTE14P-GP
41	KROW3	1	TP85	AFTE14P-GP
41	KROW2	1	TP97	AFTE14P-GP
41	KROW1	1	TP86	AFTE14P-GP
41	KCOL18	1	TP98	AFTE14P-GP
41	KCOL17	1	TP87	AFTE14P-GP
41	KCOL16	1	TP105	AFTE14P-GP
41	KCOL15	1	TP93	AFTE14P-GP
41	KCOL14	1	TP106	AFTE14P-GP
41	KCOL13	1	TP94	AFTE14P-GP
41	KCOL12	1	TP107	AFTE14P-GP
41	KCOL11	1	TP95	AFTE14P-GP
41	KCOL10	1	TP108	AFTE14P-GP
41	KCOL9	1	TP88	AFTE14P-GP
41	KCOL8	1	TP99	AFTE14P-GP
41	KCOL7	1	TP89	AFTE14P-GP
41	KCOL6	1	TP100	AFTE14P-GP
41	KCOL5	1	TP90	AFTE14P-GP
41	KCOL4	1	TP101	AFTE14P-GP
41	KCOL3	1	TP91	AFTE14P-GP
41	KCOL2	1	TP102	AFTE14P-GP
41	KCOL1	1	TP92	AFTE14P-GP

PWCN1

	5V_S0	1	TP31	AFTE14P-GP
	5V_S5	1	TP49	AFTE14P-GP
17	L-line_LED#_R	1	TP66	AFTE14P-GP
17	NUM_LED#_R	1	TP53	AFTE14P-GP
17	MEDIA_LED#_R	1	TP30	AFTE14P-GP
17	CAP_LED#_R	1	TP35	AFTE14P-GP
17	KBC_PWRBTN#_R	1	TP38	AFTE14P-GP
17	FRONT_PWRLED#_1	1	TP39	AFTE14P-GP
17	STDBY_LED#_1	1	TP266	AFTE14P-GP

FP2

	3D3V_S0	1	TP46	AFTE14P-GP
21,31	USBPP6	1	TP34	AFTE14P-GP
21,31	USBPN6	1	TP41	AFTE14P-GP
31,41	FP_DETECT#	1	TP32	AFTE14P-GP
21,31	FP_ID	1	TP42	AFTE14P-GP
31,41	TP_LEFT	1	TP33	AFTE14P-GP
31,41	TP_RIGHT	1	TP40	AFTE14P-GP

TPDA1

	5V_S0	1	TP44	AFTE14P-GP
41	TP_DATA	1	TP37	AFTE14P-GP
41	TP_CLK	1	TP43	AFTE14P-GP
31,41	TP_RIGHT	1	TP36	AFTE14P-GP
31,41	TP_LEFT	1	TP45	AFTE14P-GP

BLUE1

21,28	USBPP5	1	TP159	AFTE14P-GP
21,28	USBPN5	1	TP160	AFTE14P-GP
	3D3V_BT_S0	1	TP158	AFTE14P-GP

USBCN1

	5V_S5	1	TP161	AFTE14P-GP
	5V_S5	1	TP164	AFTE14P-GP
21,30	USB_OC#4	1	TP166	AFTE14P-GP
30,41	USB_PWR_EN#	1	TP165	AFTE14P-GP
21,30	USBPN4	1	TP168	AFTE14P-GP
21,30	USBPP4	1	TP167	AFTE14P-GP
21,30	USBPN8	1	TP171	AFTE14P-GP
21,30	USBPP8	1	TP170	AFTE14P-GP

FAN1

25	FAN1_FG1	1	TP25	AFTE14P-GP
	FAN1_VCC	1	TP26	AFTE14P-GP

BAT1

52	BATA_SDA_1	1	TP9	AFTE14P-GP
52	BATA_SCL_1	1	TP8	AFTE14P-GP
	BT+	1	TP11	AFTE14P-GP
	BT+	1	TP10	AFTE14P-GP
	BT+	1	TP14	AFTE14P-GP
51,52	BATT_SENSE	1	TP13	AFTE14P-GP
52	BAT_IN#_CN	1	TP7	AFTE14P-GP

DC1

	AD_JK	1	TP12	AFTE14P-GP
	AD_JK	1	TP16	AFTE14P-GP
	AD_JK	1	TP15	AFTE14P-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size	Document Number	Rev
A3	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 54 of 57