LCFC NM-E021

HY520 15P M/B Schematics Document

Tiger Lake H-Processor with DDR4 + NV GN20-P GPU

REV:0.1

2020-12-23

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Title	Cover Page		
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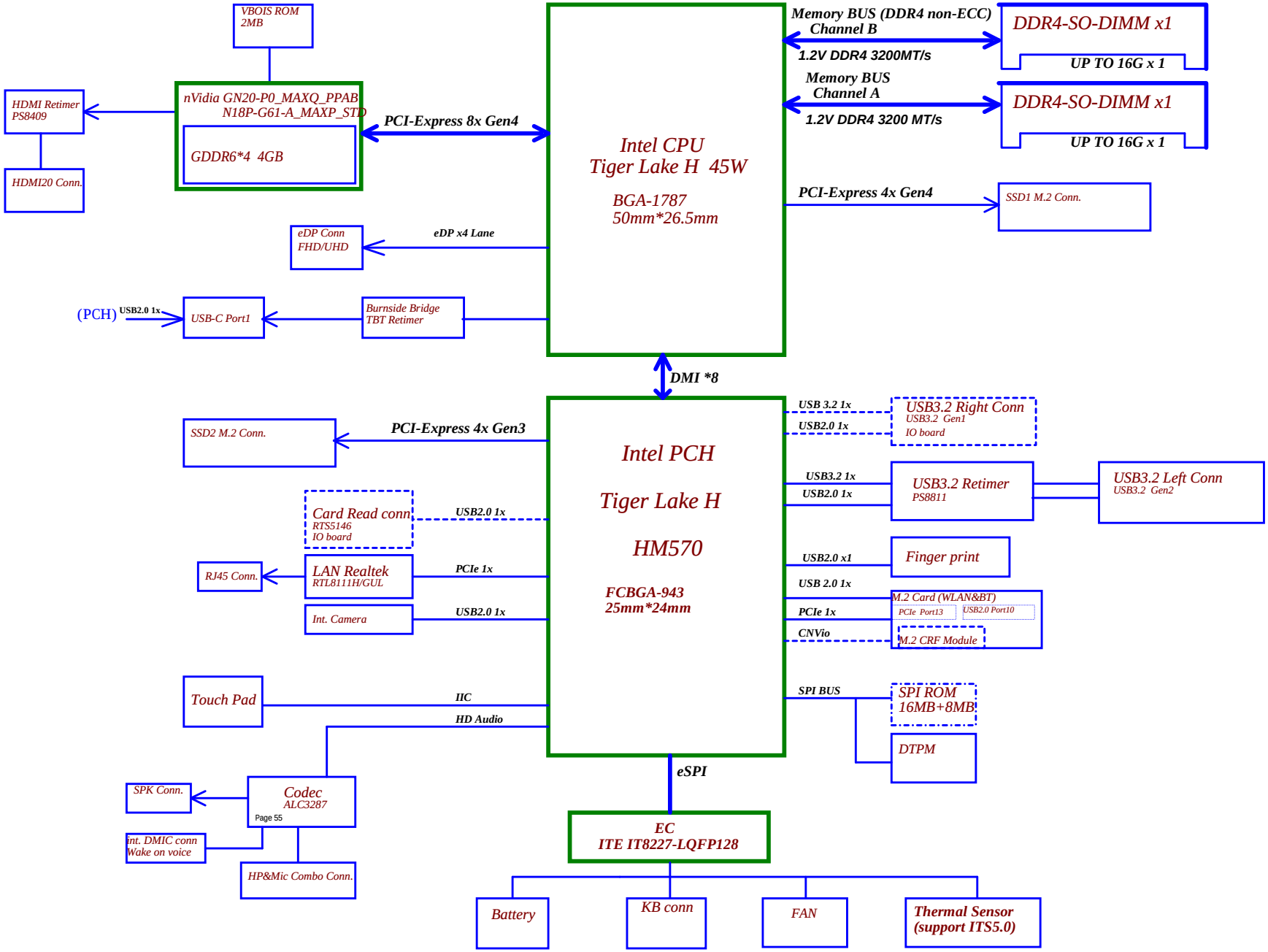

Title: **Block Diagram**

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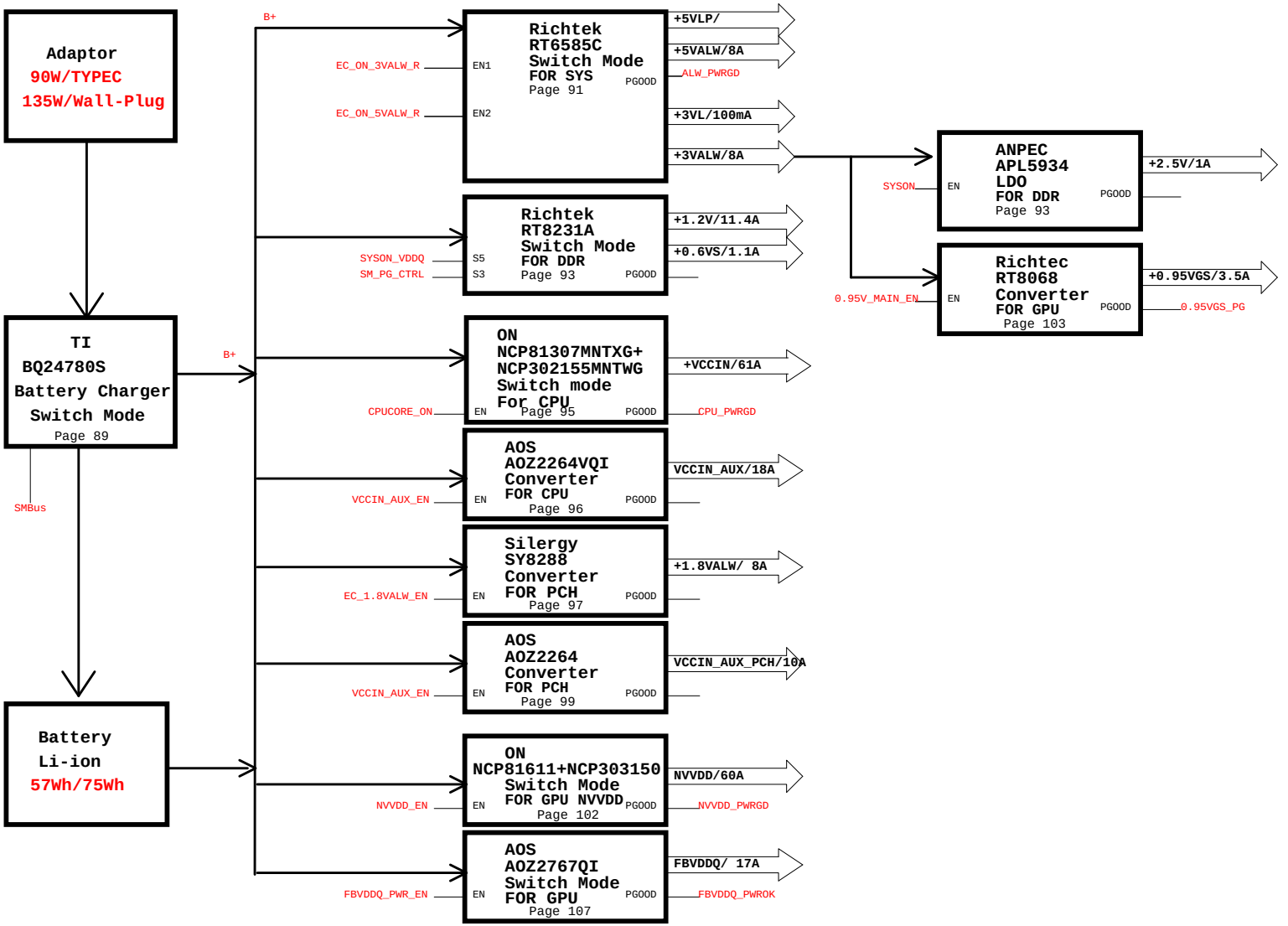

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Title: **Power Diagram**

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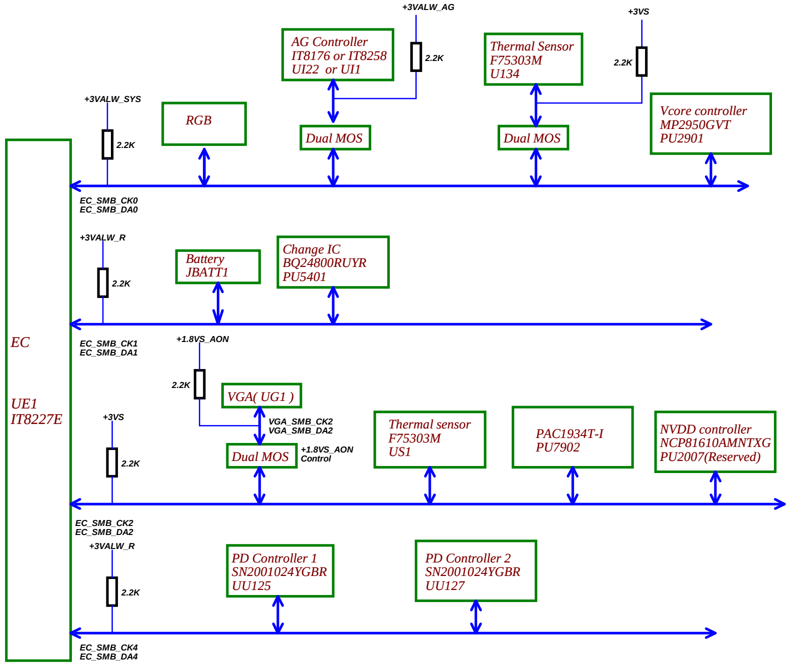
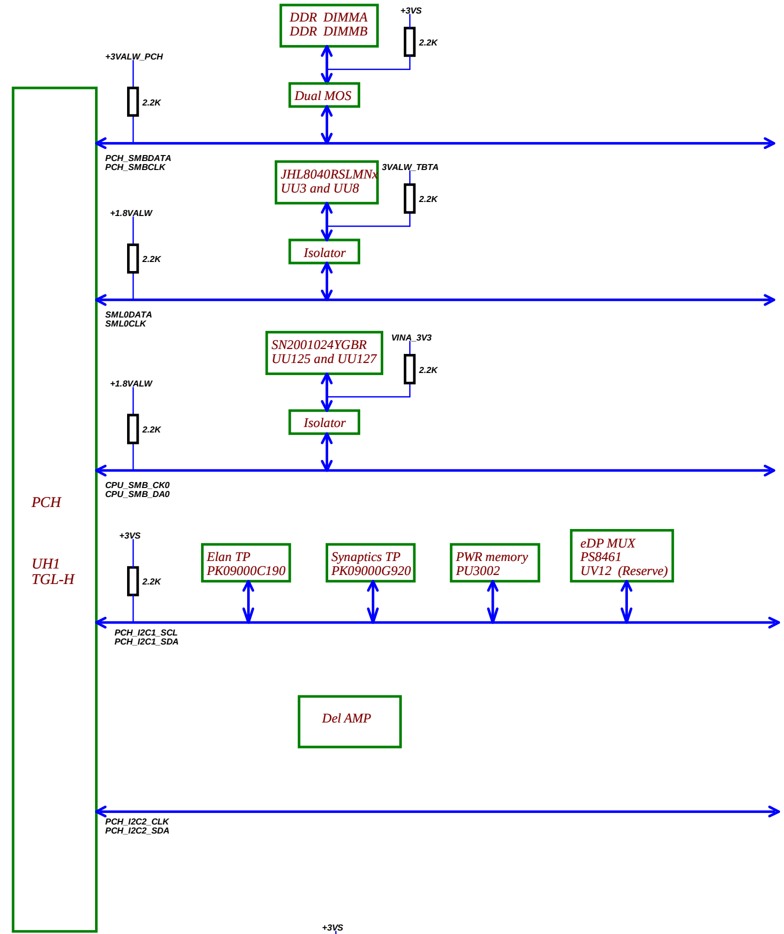




SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_VGA	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

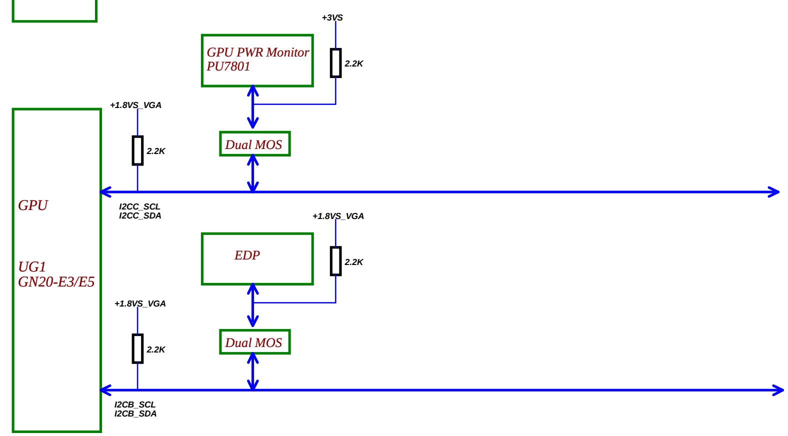
Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update
Thermal Sensor NCT7718W	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update



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Title: Notes

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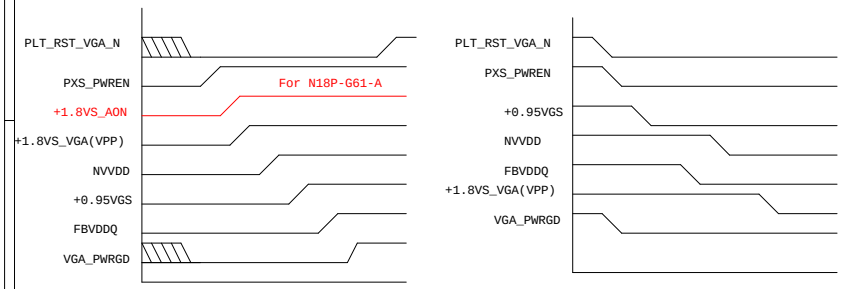
GN20x-P/N18P-G61-A GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN 1V8_MAIN_EN	GN20x-P GPU power sequencing for GC6 ---MSVDD_EN N18P-G61-A 1V8_MAIN_EN	GPIO4_GC6_MSVDD_EN 1V8_MAIN_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	iGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED	UNUSED		test point
GPIO24	IN	HPD_IFPF*	Hot Plug Detect for IFPF	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	test point
GPIO26	OUT	ROM_WP* FP_FUSE	GN20x-P Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)

GN20x-P/N18P-G61-A Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from 1V8 on to PEXVDD/GPU_PGOOD assertion not exceed 20ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90% before PEXVDD can ramp-up.
5. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6

1. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
2. All 3.3V devices that connect to the GPU must be ramp down before 1V8; GPU can NOT have any 3.3V leakage path after 1V8 power down.
3. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down.

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-P/N18P-G61-A VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	Hynix Only For GN20x-P H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION ENABLE

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	N18P-G61-A ENABLE OVERT*
L	L	H	GN20x-P ENABLE OVERT*

BOM NOTE:
1.BOM Structure:
GN20x-P1/P0-->GN20@
N18P-G61-A-->N18P@

2.1.0V_GS voltage different: need Power setting
GN20x-P1/P0-->0.95V
N18P-G61-A-->1.0V

3.VBIOS ROM partnumber need BOM control
GN20x-P1/P0-->2MB PN:SA0000AU500
N18P-G61-A-->1MB PN:SA000080E00

4.ROM_SO,ROM_SI,ROM_CLK setting
GN20x-P1/P0-->LLH
N18P-G61-A-->LLL

5.VRAM_FB(RG702 STUFF package 0402)
GN20x-P1/P0 :2.49K ohm（PN:SD03424918J）
N18P-G61-A: 49.9 ohm（PN:SD034499A8J）

6.+FUSE_1V8
GN20x-P1/P0 :RG1200:10K CG1104:1U
N18P-G61-A: RG1200:2.21K CG1104:2.2U

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
OPT@	GN20-P1/P0 N18P-G61 Stuff
GN20@	GN20P1/P0 Stuff
N18P@	N18P-G61 Stuff

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_VGA +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	Y540 15'' stuff
17@	17'' stuff
7000P@	7690P stuff
7502M@	7502 stuff
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
AG@	Anti-ghost
AOAC@	AOAC support part
BL@	BL
CD@	Cost down part
CNVI@	CNVi support part
DCI@	DCI
Debug@	USB2.0 port 1for Debug
EMC@	EMC part
EMC_8111H@	LAN 8111H EMC Part
EMC_NS@	EMC not stuff
GC6@	GC6
GYSNC@	GSYNC support part
HDMI@	HDMI
i5@i7@i9@	CPU Part
ME@	ME part(connector, hole)
M6GX6@S6GX6@	VRAM part

BOM Structure	BTO Item
MIRROR@	MIRROR
N18EG0@N18EG1@	GPU part
NOMIRROR@	17'' stuff
NPI@	DP1 VCC diode stuff
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
UP9632_@	UP9632 part stuff
USB@	USB2.0 port1 for USB Port
X76@	VRAM
GS@	Reserved for G-sensor
15_P@	

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7	RGBKB
9	AG
10	Back USB3.0
11:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Right USB3.0
3	Left USB3.0
4	Type-C Port
5	Back USB3.0
6	NA

SATA Port table	
Port	Function
0A	NA
0B	HDD Gen3
1A	M.2 SSD Gen3
1B	NA
2	NA
3	NA
4	M.2 SSD Gen3
5	NA
7	NA

PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
14	WLAN Gen1
15	LAN Gen1
16	for Card Reader 17"
17:20	M.2 SSD

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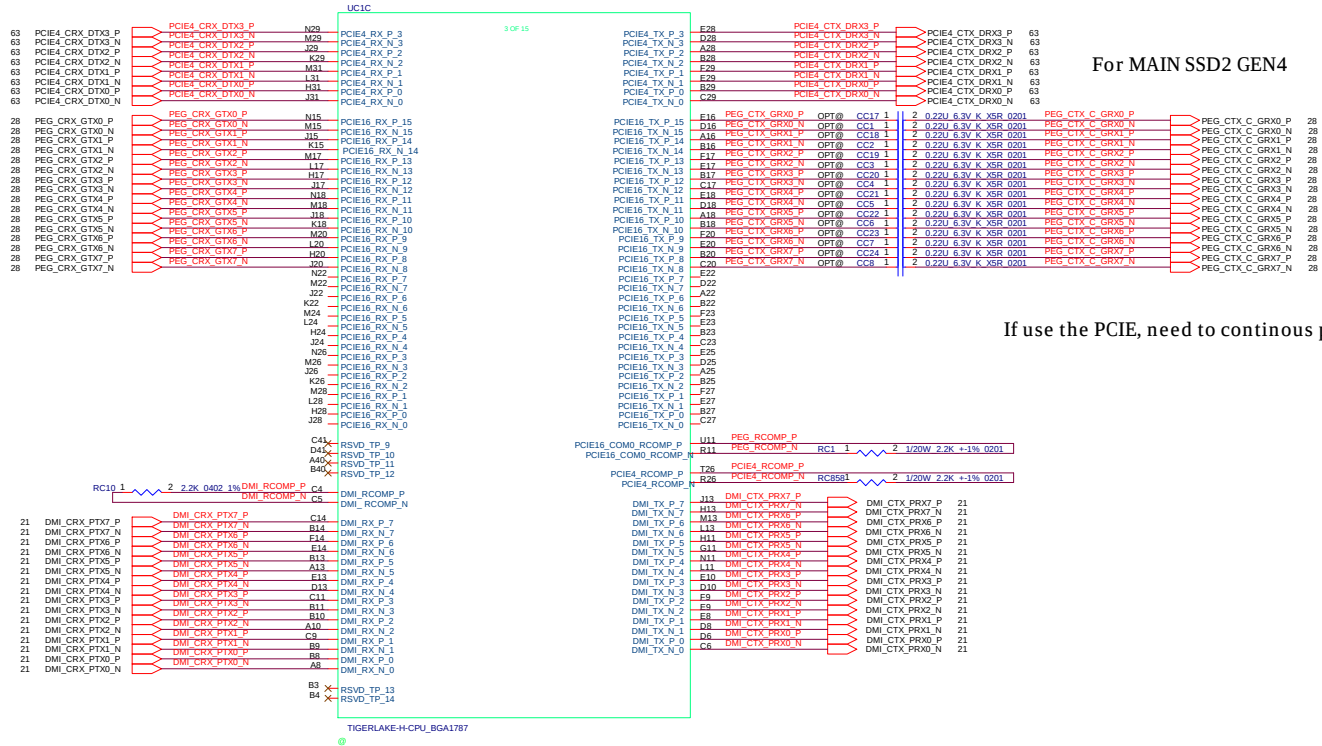
For MAIN SSD2 GEN4



For MAIN SSD2 GEN4

If use the PCIE, need to continous port

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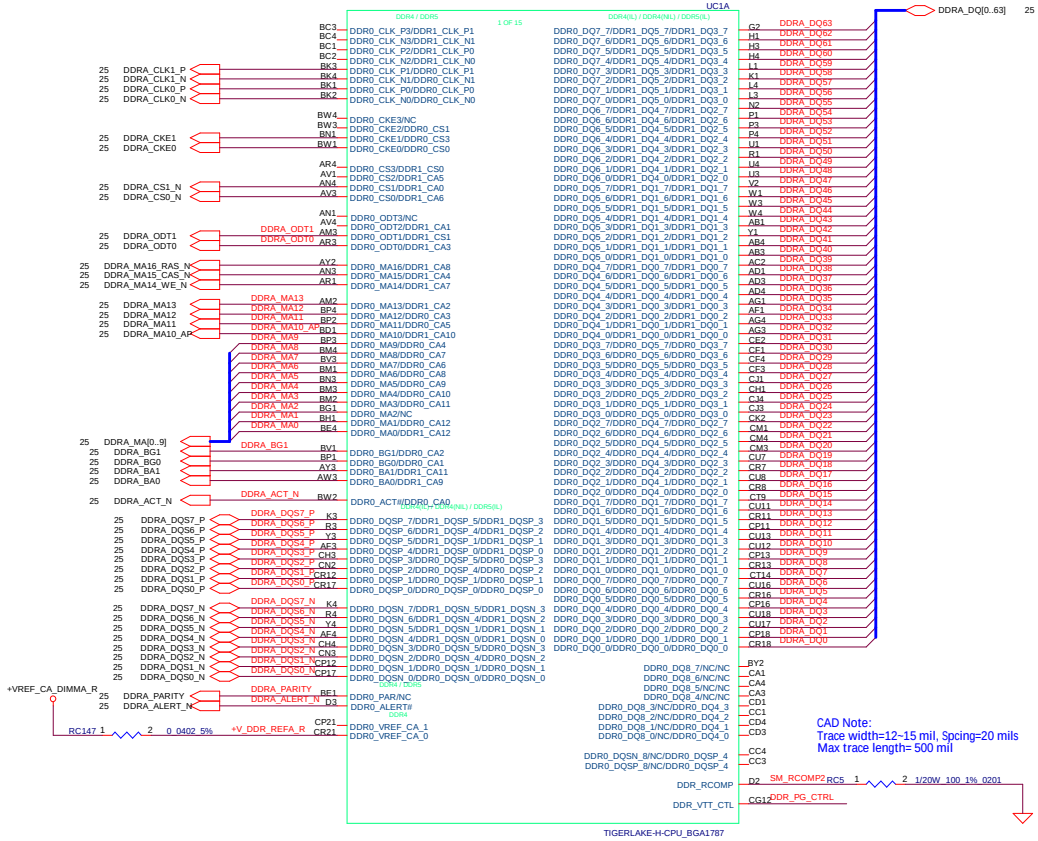

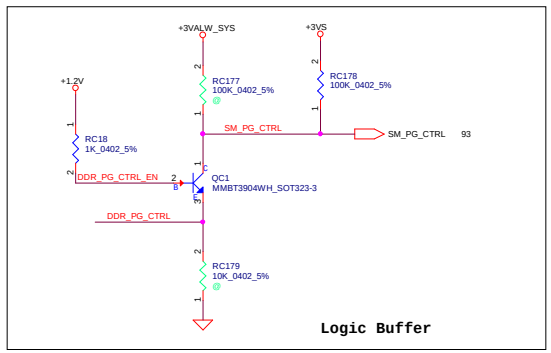

CAD Note:
Trace width= 20 mil, Spcing=20 mils

DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_CA : Connected to VREF_CA on DIMM CH-B

DDR4 COMPENSATION SIGNALS

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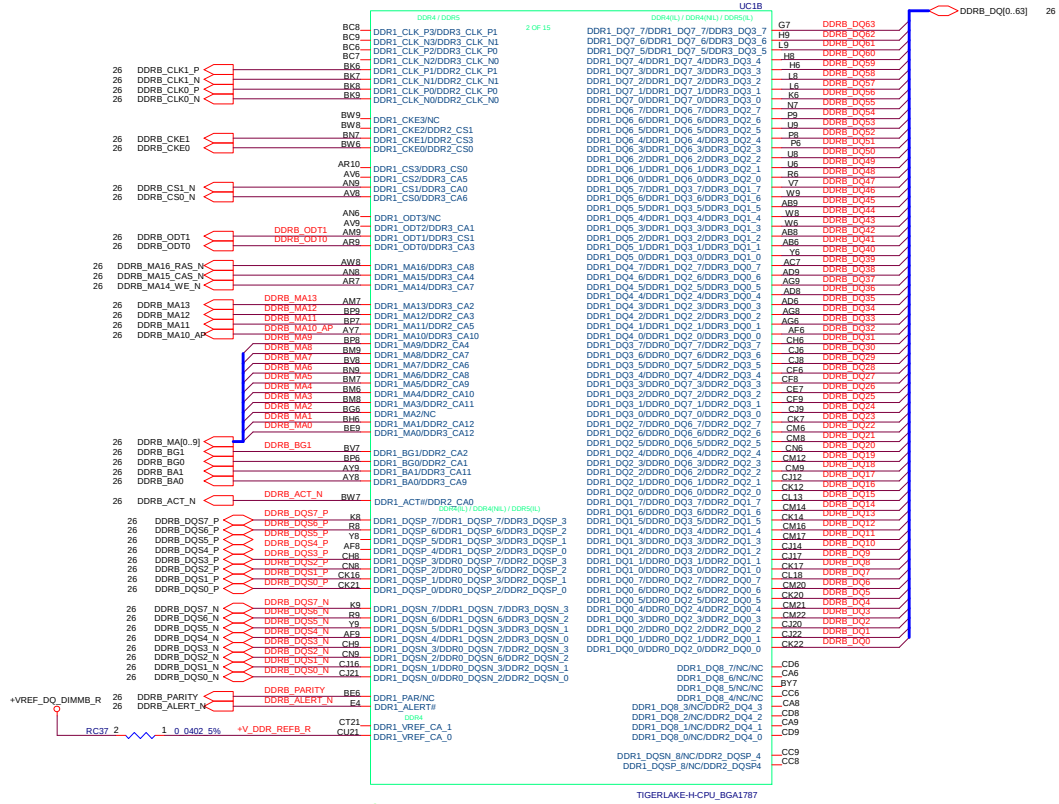

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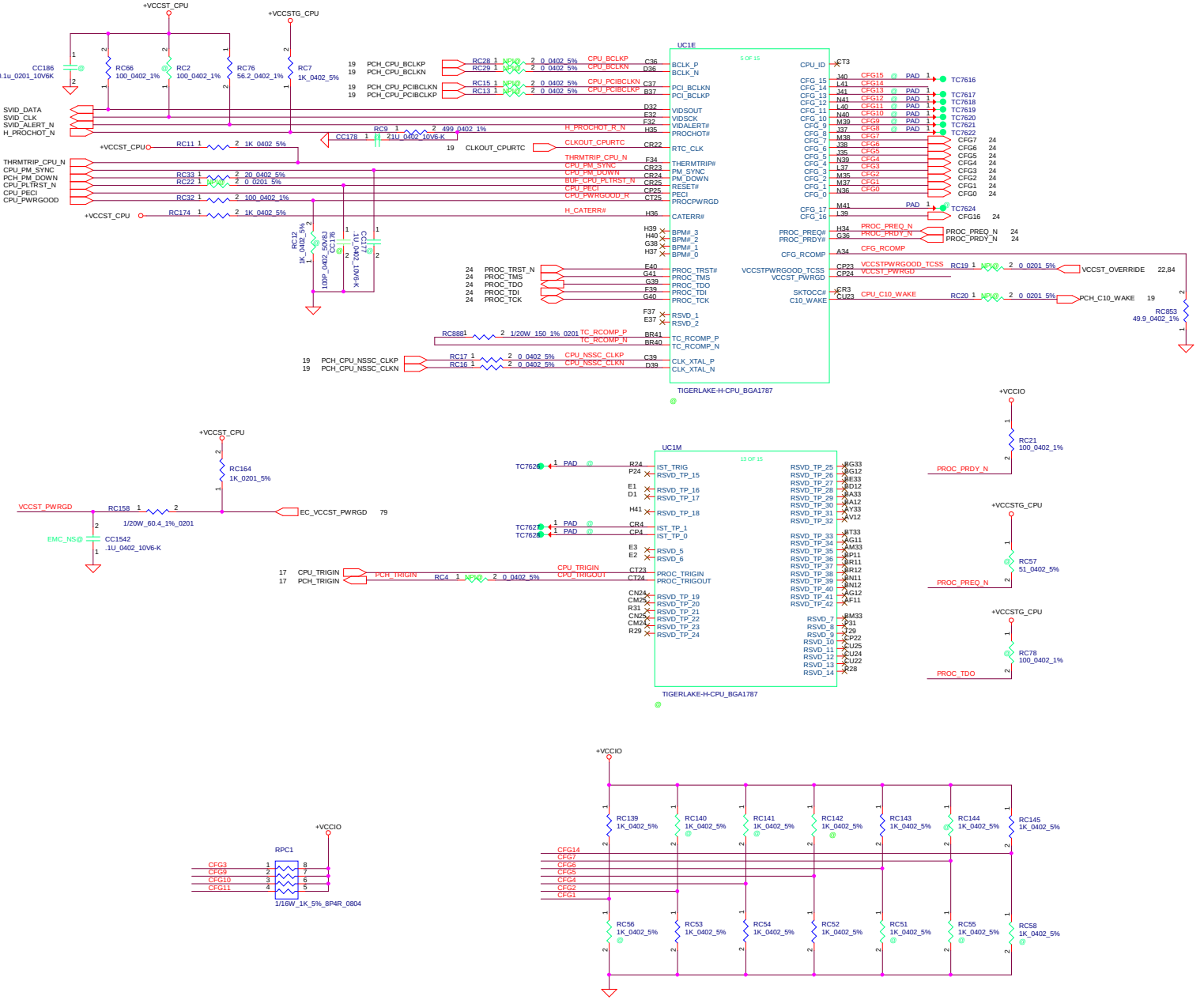

CFG Straps for CPU

Reserved configuration lane	
CFG0	N/A

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.

Reserved configuration lane	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*

Reserved configuration lane	
CFG[13:7]	N/A

PCIE4 LANE reversal	
CFG14	* 1 = (default) normal 0 = Reversed

Reserved configuration lane.	
CFG[17:15]	N/A

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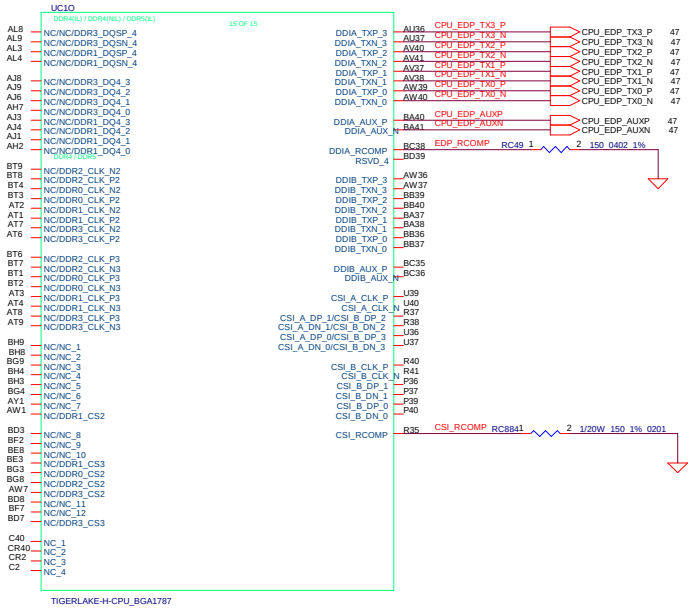

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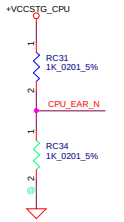

Stall CPU reset sequence until de-asserted	
CPU_EAR_N	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

Disabling and Termination Guidelines	
DPIPx_HPD	* Pull down to ground via 100k resistor

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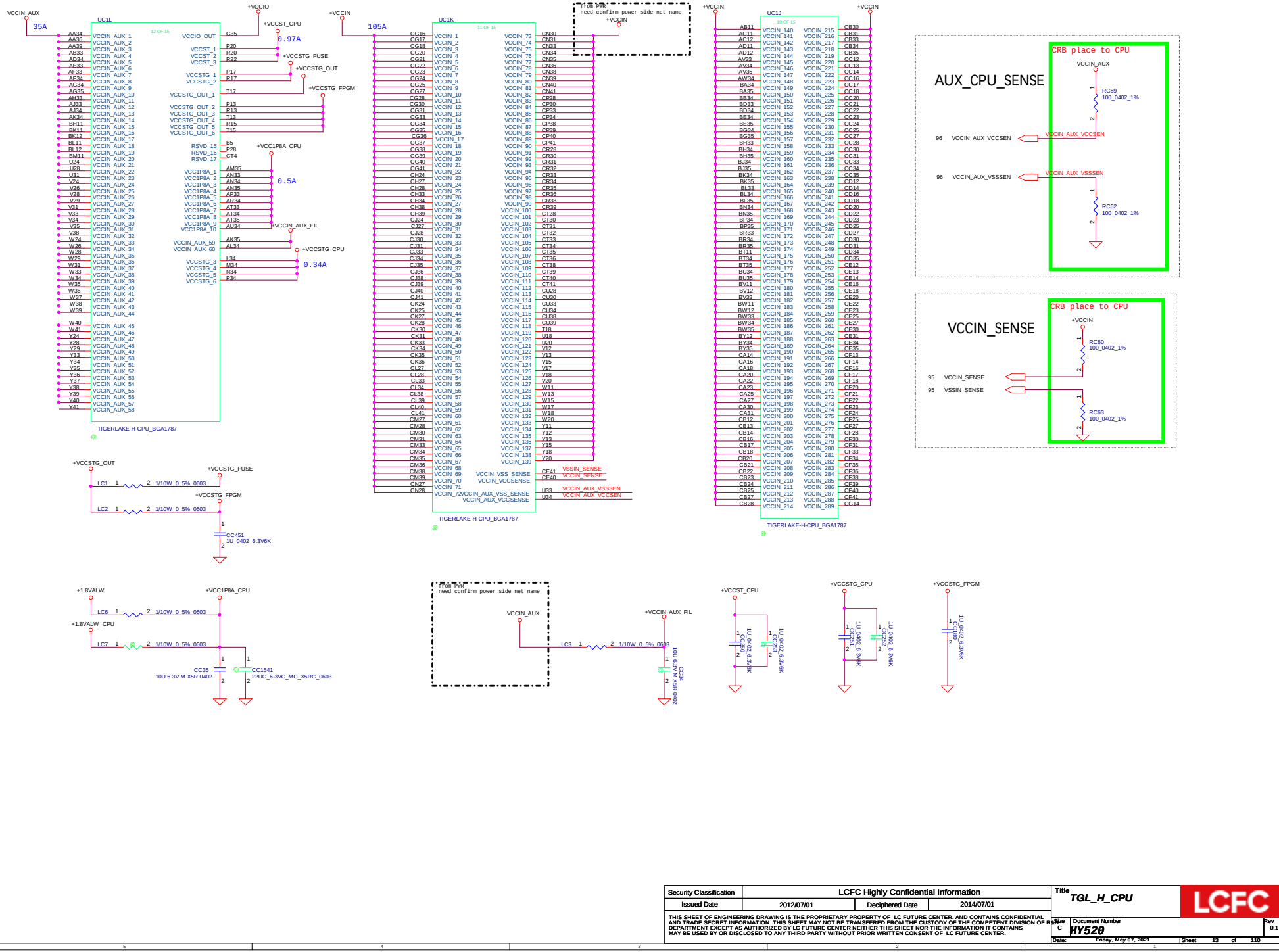

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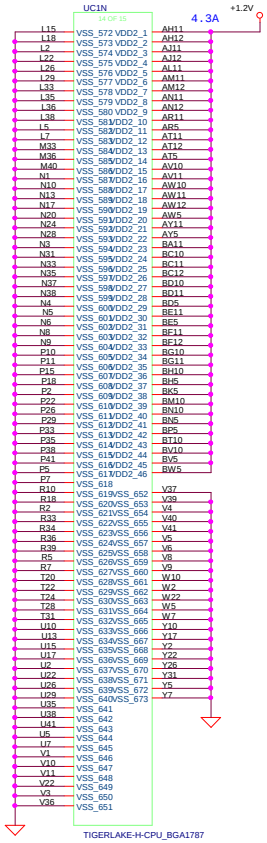

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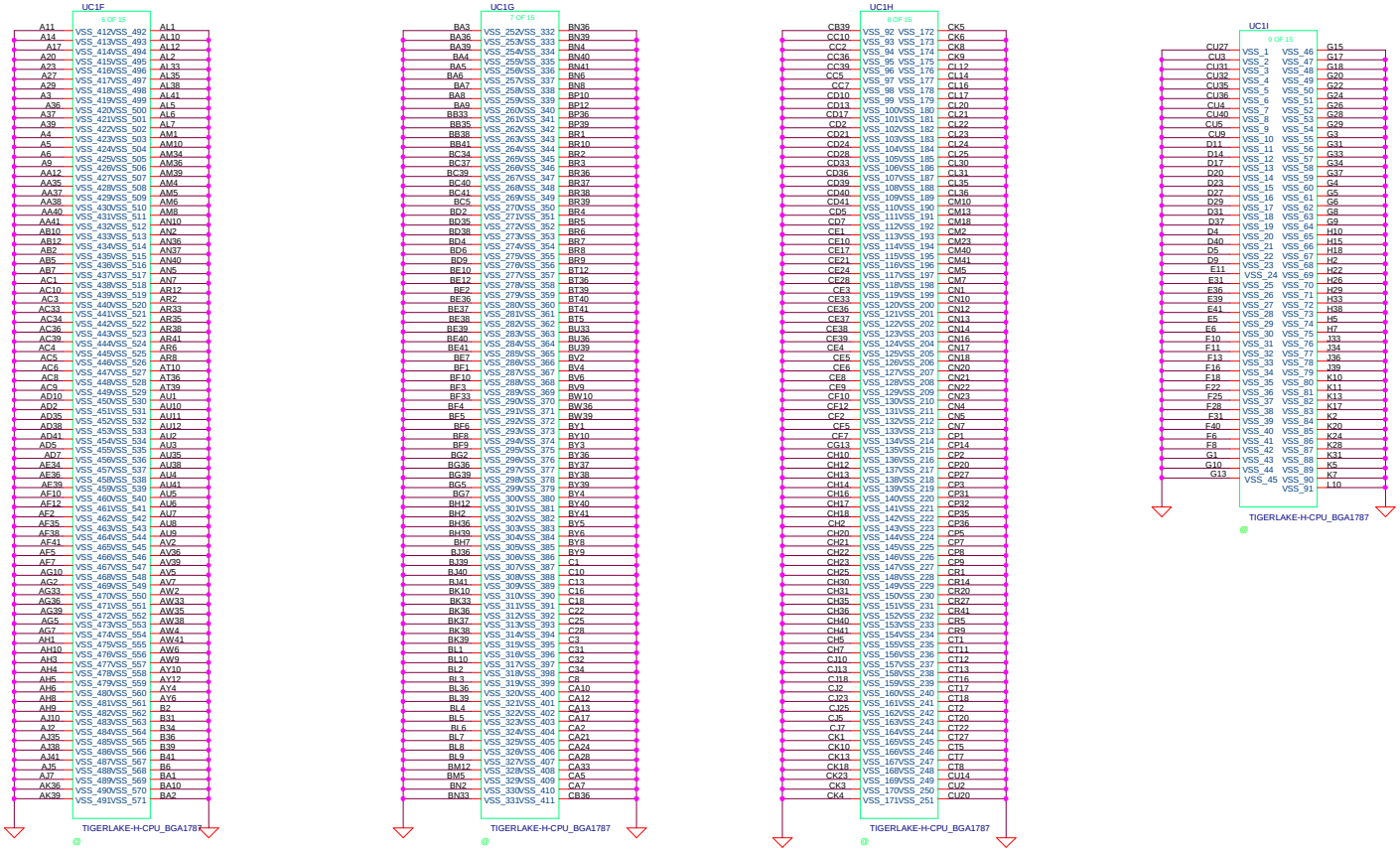

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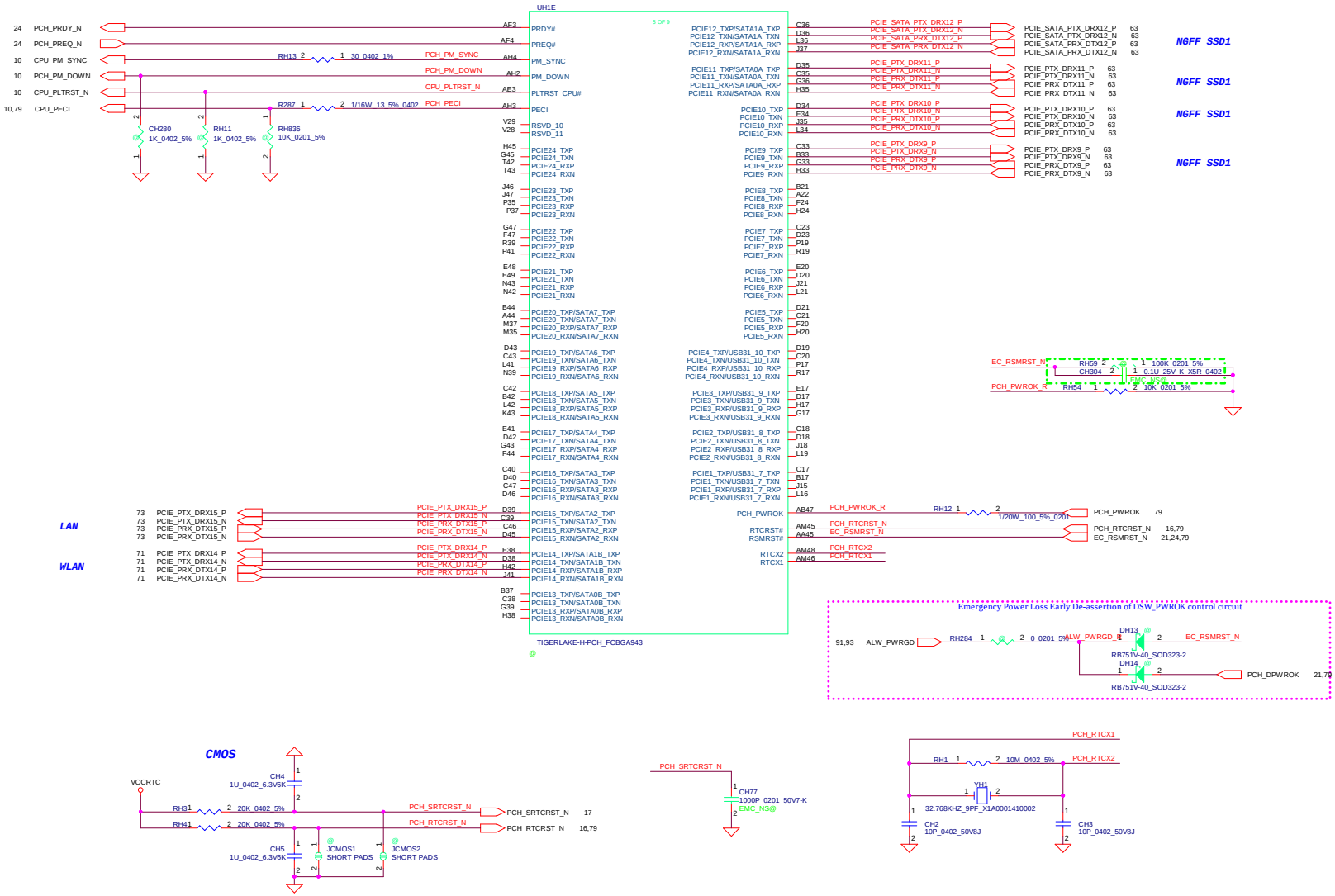

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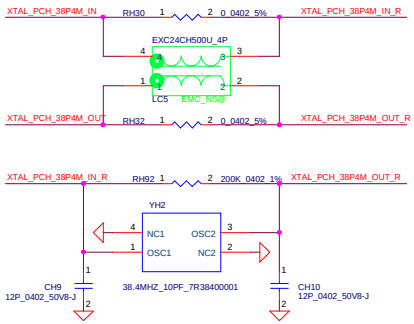
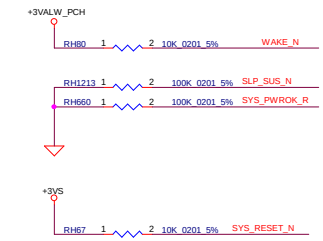
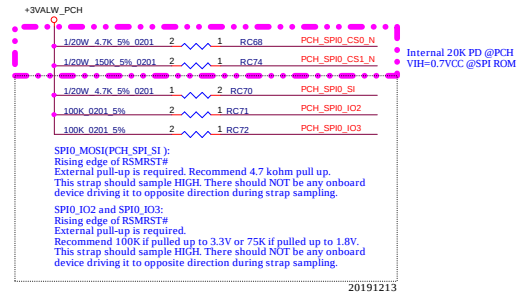
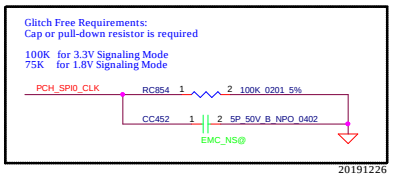
All processor based platforms are required to provide a 38.4MHz input to the PCH to enable the PCH to generate all of its internal reference clocks and all of the single-ended and differential platform clock outputs

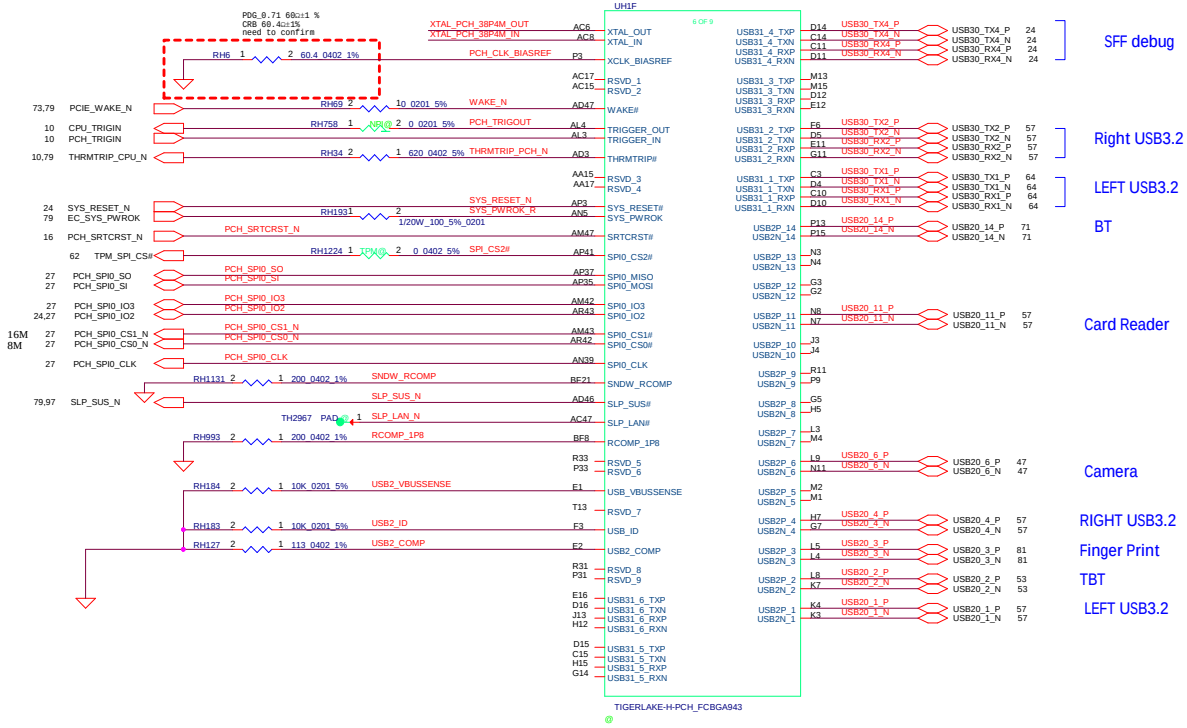






Internal 20K PD @PCH
VIH=0.7VCC @SPI ROM





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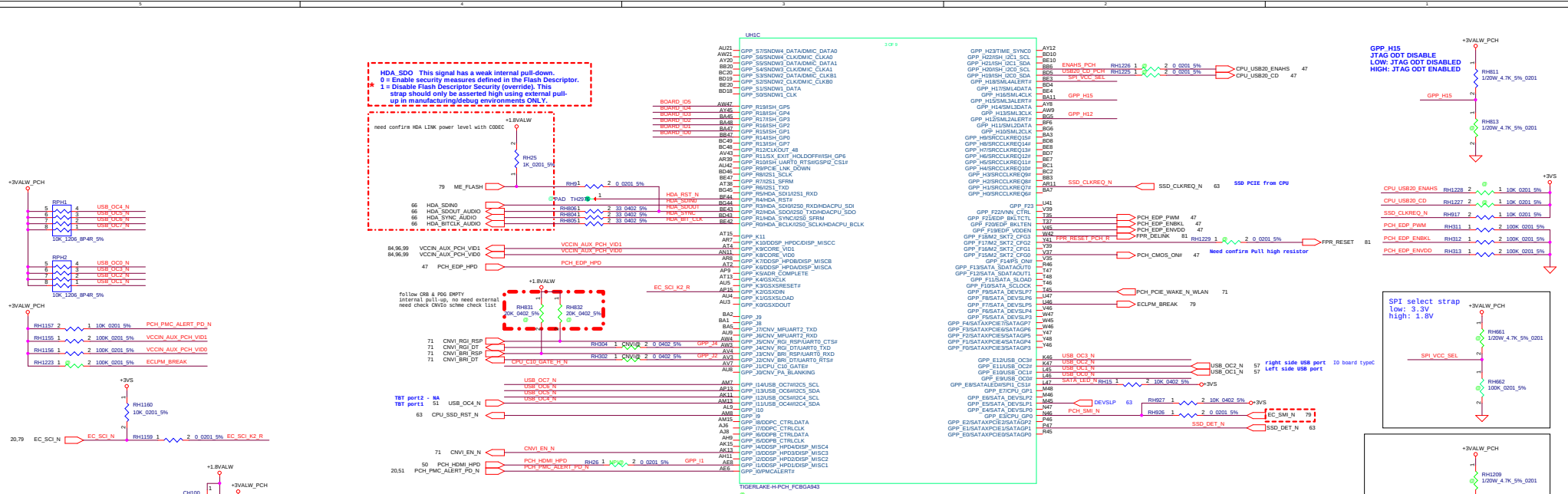

Function	BOARD_ID0 GPP_R14	BOARD_ID1 GPP_R15	BOARD_ID2 GPP_R16	BOARD_ID3 GPP_R17	BOARD_ID4 GPP_R18	BOARD_ID5 GPP_R19
	SKU Size			GPU Type		
TBD	0	0	1	0	0	1
TBD	0	1	0	0	0	1
TBD	0	0	1	0	1	0
TBD	0	1	1	0	0	1
TBD	0	1	1	0	1	0
TBD	1	0	0	0	0	1
TBD	1	0	0	0	1	0
TBD	1	0	0	0	1	1
TBD	0	0	1	1	0	0
TBD	0	1	0	1	0	0
TBD	0	0	1	1	0	1
TBD	0	1	0	1	0	1
15P-GN20P-P0	0	1	1	1	0	0
15P-GN20P-P1	0	1	1	1	0	1
15P-15-N18P-G61	0	0	1	1	1	0
TBD	0	1	0	1	1	0

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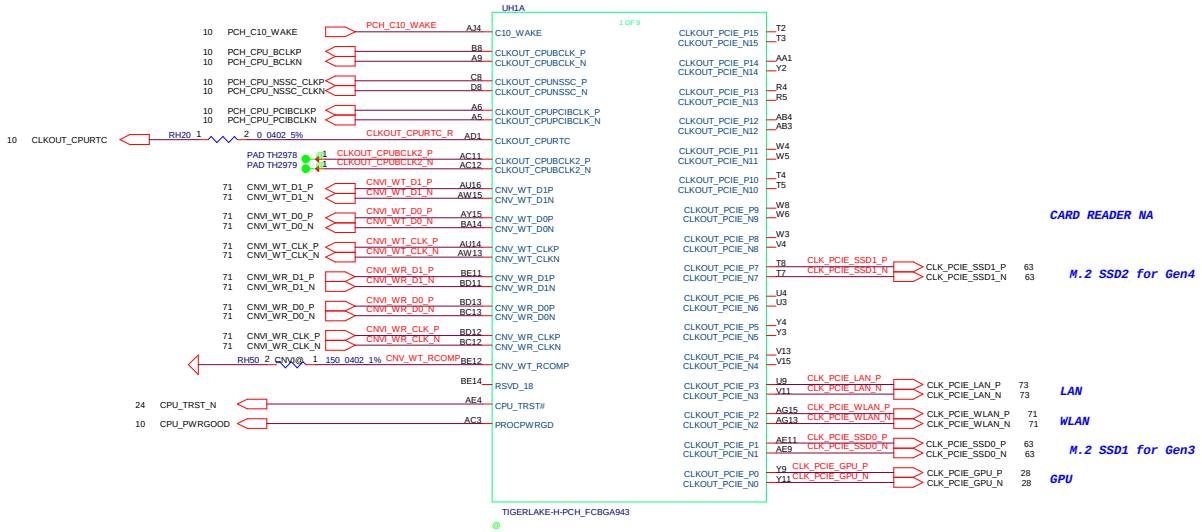

Title			
TGL_H_PCH			
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GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
0 = eSPI Enable (for EC). (Default)
1 = eSPI Disable (for EC).

GPP_B23 /SML1ALERT# /PCHHOT#
This strap has a 20 kOhm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable "Top Swap " mode. (Default)
1 = Enable "Top Swap " mode. This inverts an address on access to SPI and firmware hub. so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).

GPP_B22
HIGH: LPC SELECTED FOR SYSTEM FLASH
LOW: SPI SELECTED. (DEFAULT)
BOOT BIOS STRAP (BBS)
WEAK INTERNAL PD

SMBUS/SMLINK需要重新分配
GPPD电位1.8V
SMLINK0是给Burinside bridge re-timer
SMLINK1是给PD
GPU EC thermal等DEVICE换其他SMBUS

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Title: TGL_H_PCH
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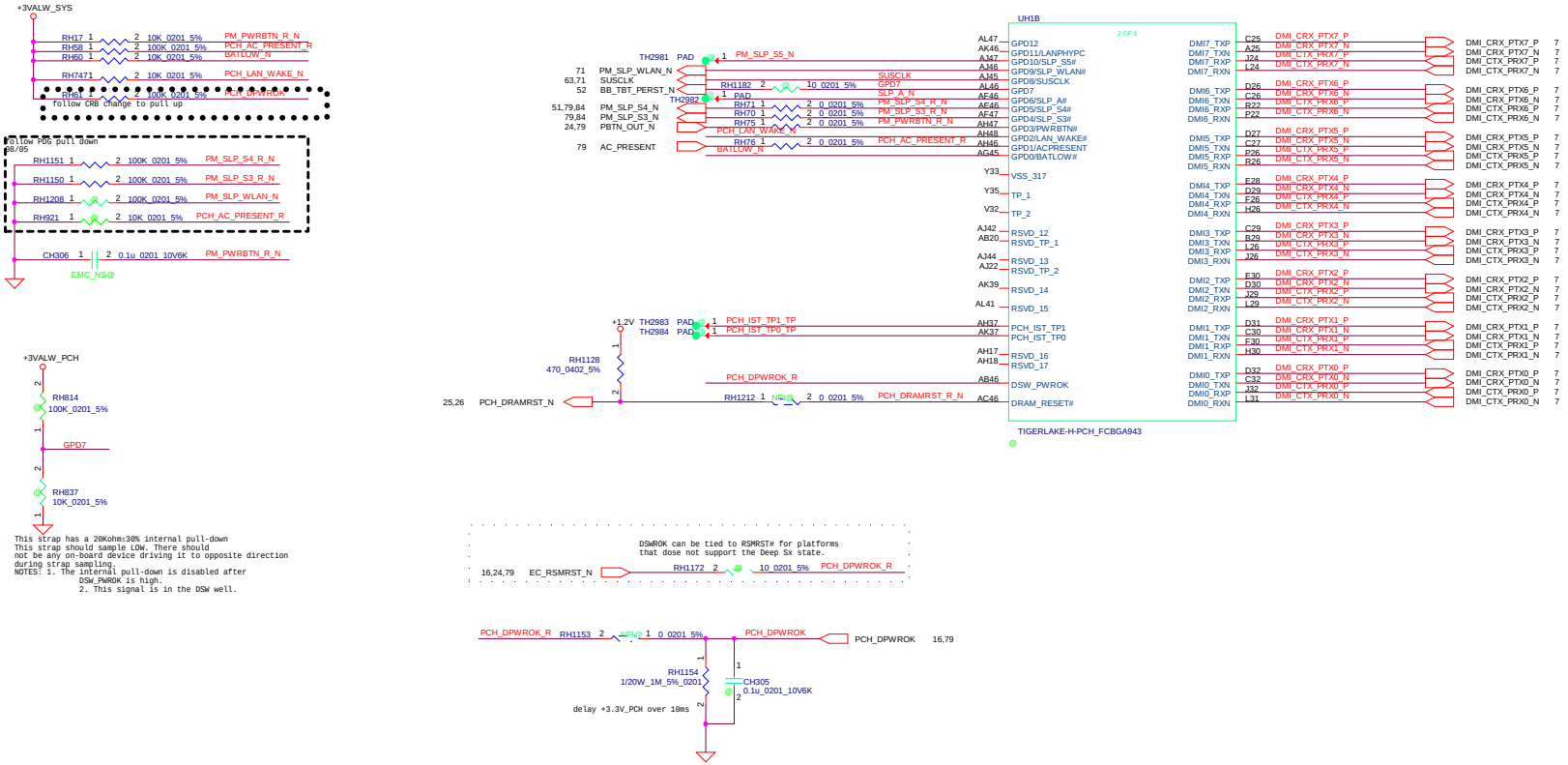

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	TGL_H_PCH		
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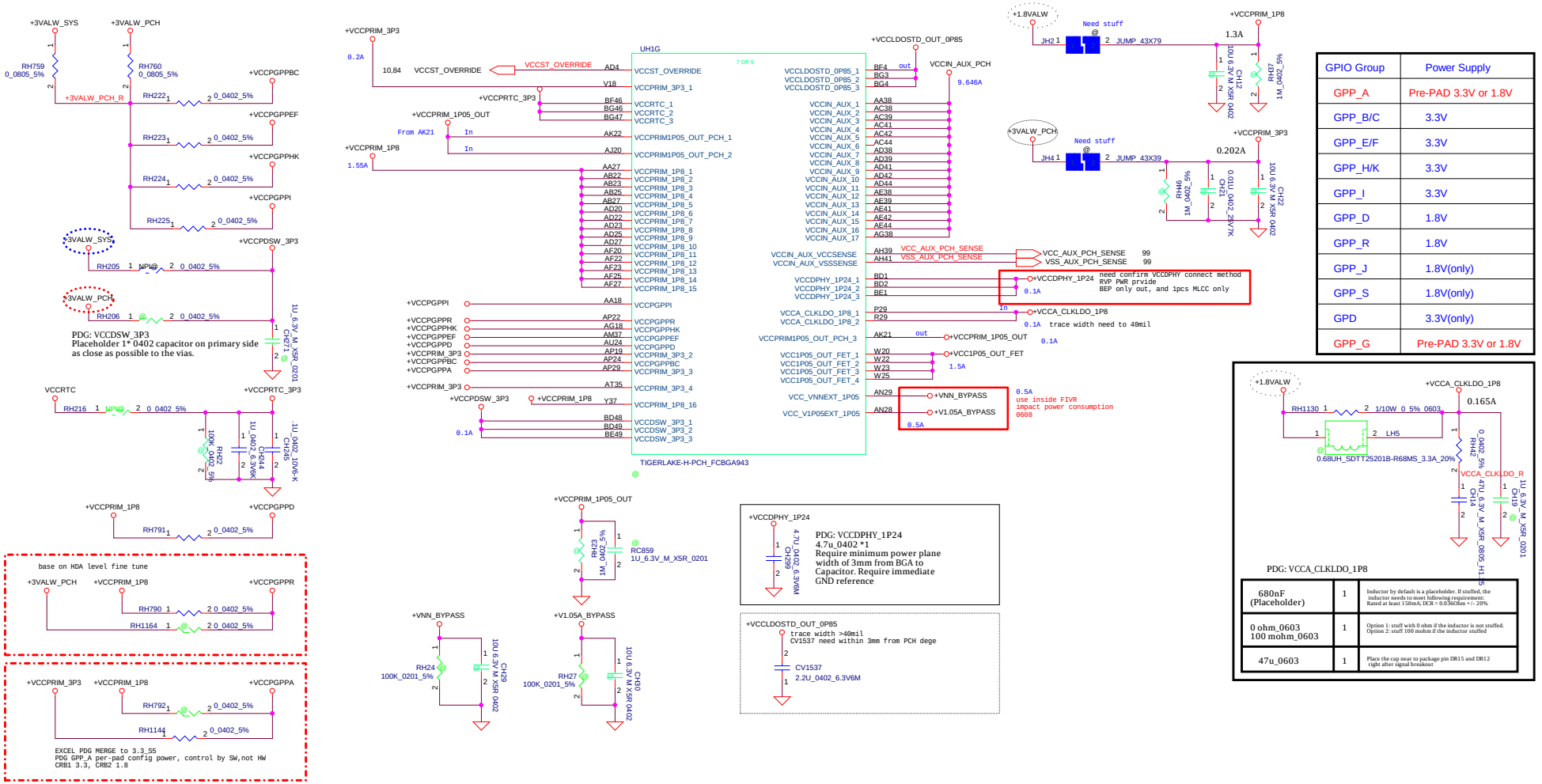

GPIO Group	Power Supply
GPP_A	Pre-PAD 3.3V or 1.8V
GPP_B/C	3.3V
GPP_E/F	3.3V
GPP_H/K	3.3V
GPP_I	3.3V
GPP_D	1.8V
GPP_R	1.8V
GPP_J	1.8V(only)
GPP_S	1.8V(only)
GPD	3.3V(only)
GPP_G	Pre-PAD 3.3V or 1.8V

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Title: TGL_H_PCH

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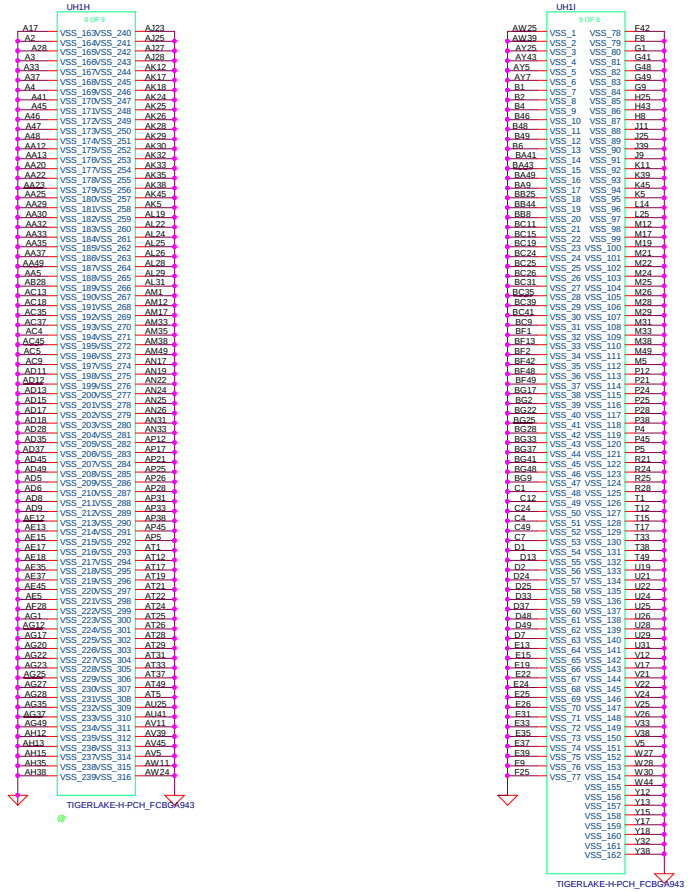

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: TGL_H_PCH

LCFC

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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: XDP

LCFC

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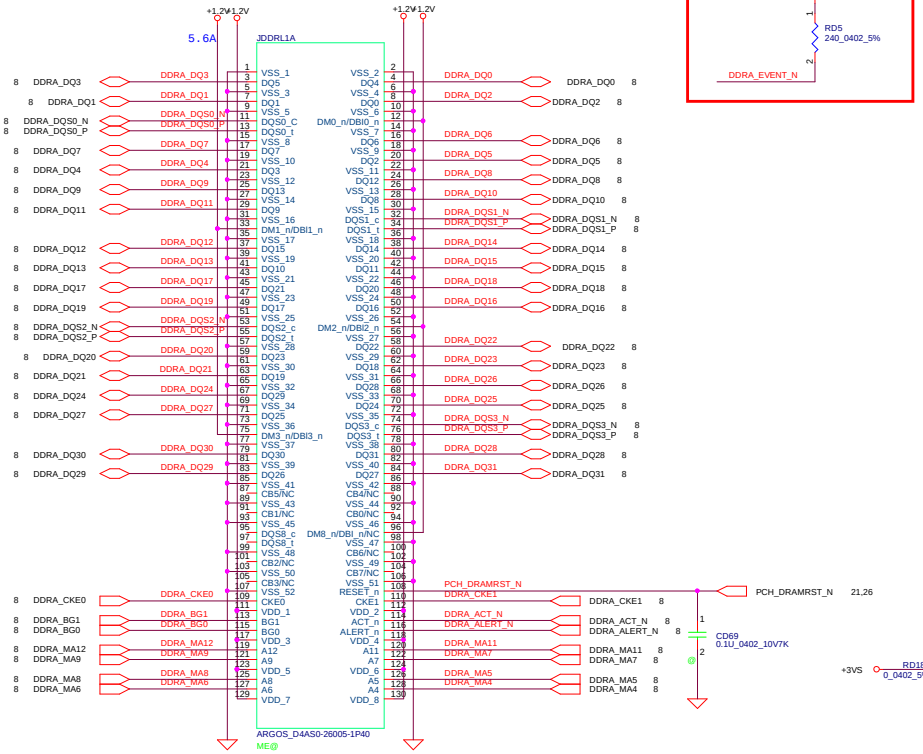
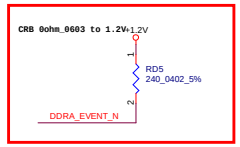
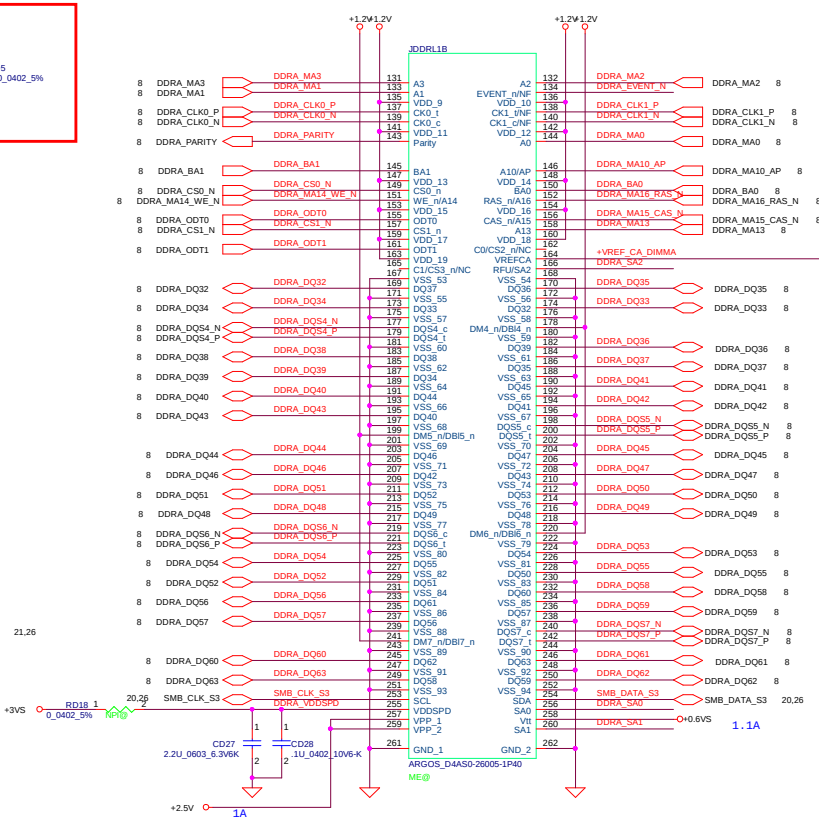
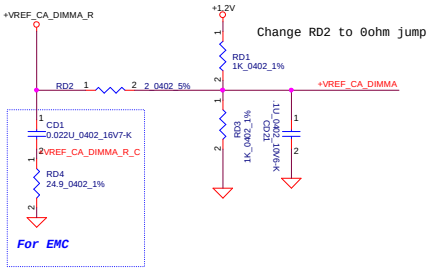
DDR4 SO-DIMM A
Follow CRB ball map TOP 9.2 Height

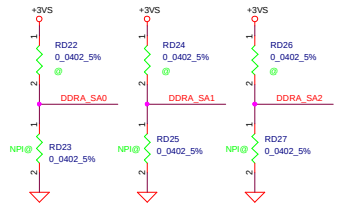






Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket





SPD Address = 0H

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: DDRVI SO-DIMM A

LCFC

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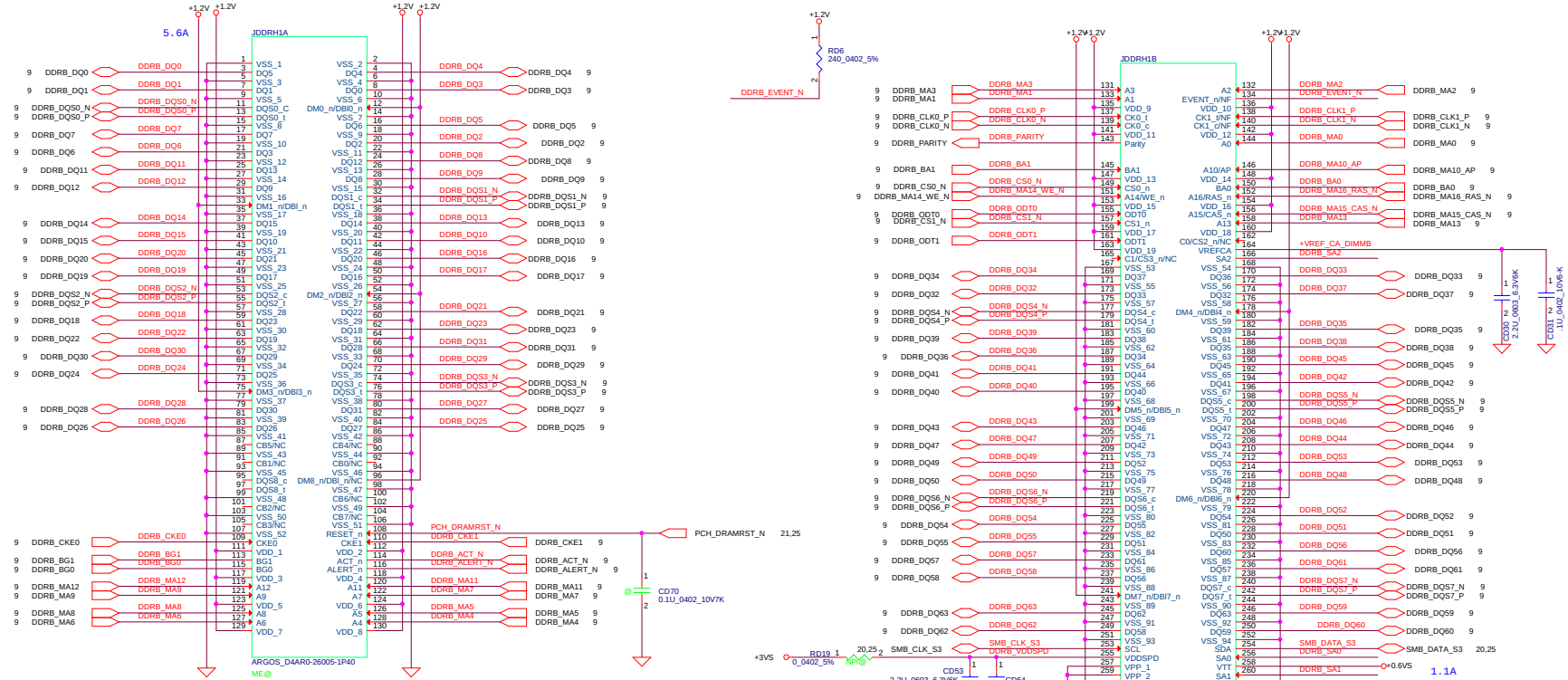
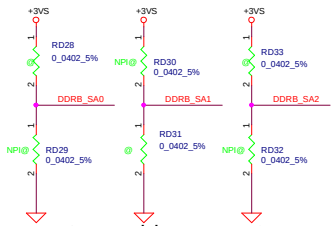
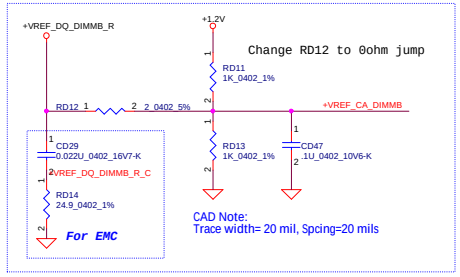
DDR4 SO-DIMM B
Follow CRB ball map TOP 5.2 Height







Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **DDRVI SO-DIMM B**

LCFC

Size	Document Number	Rev
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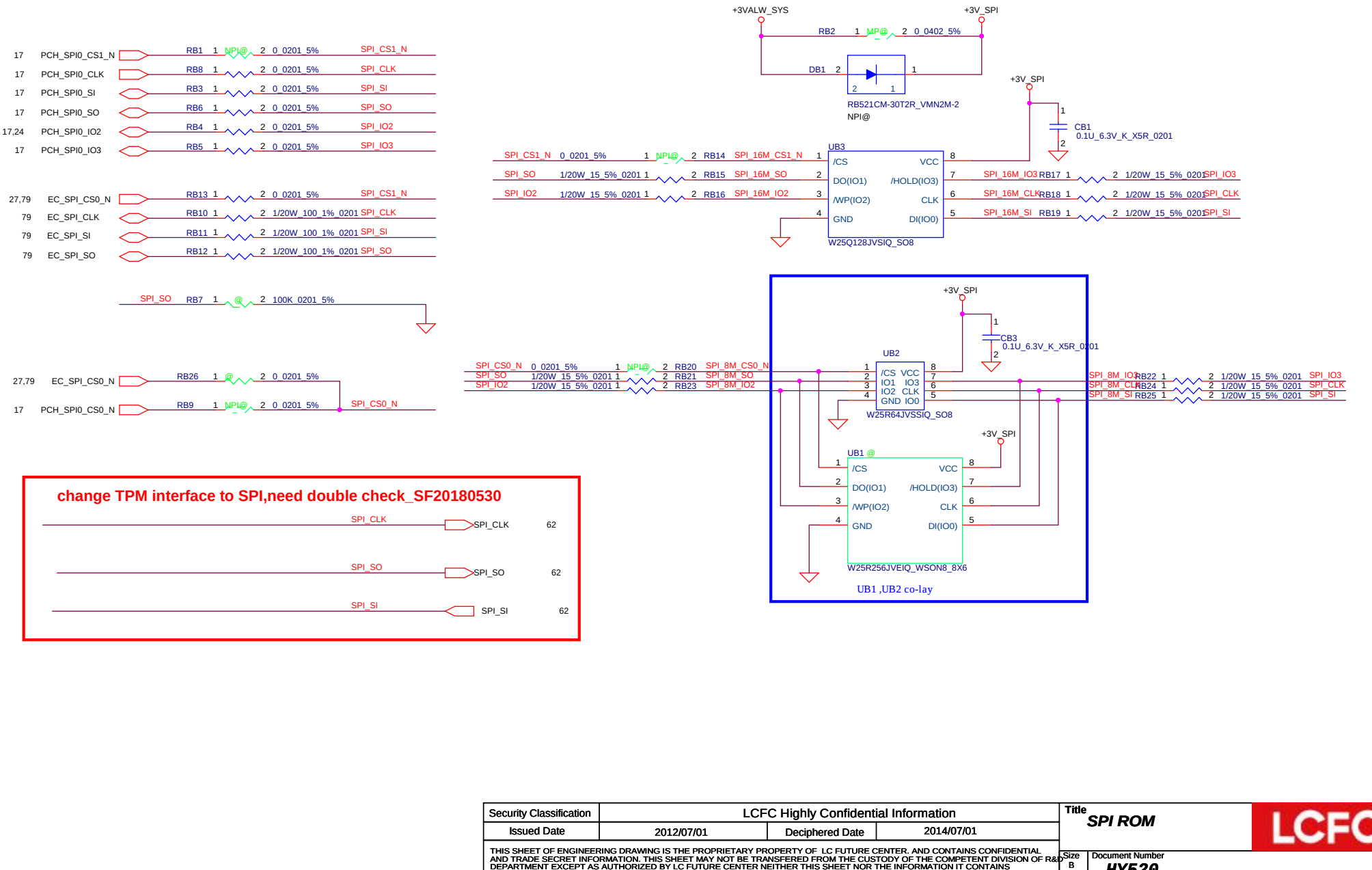

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: SPI ROM

LCFC

Size	Document Number	Rev
B	HY520	0.1

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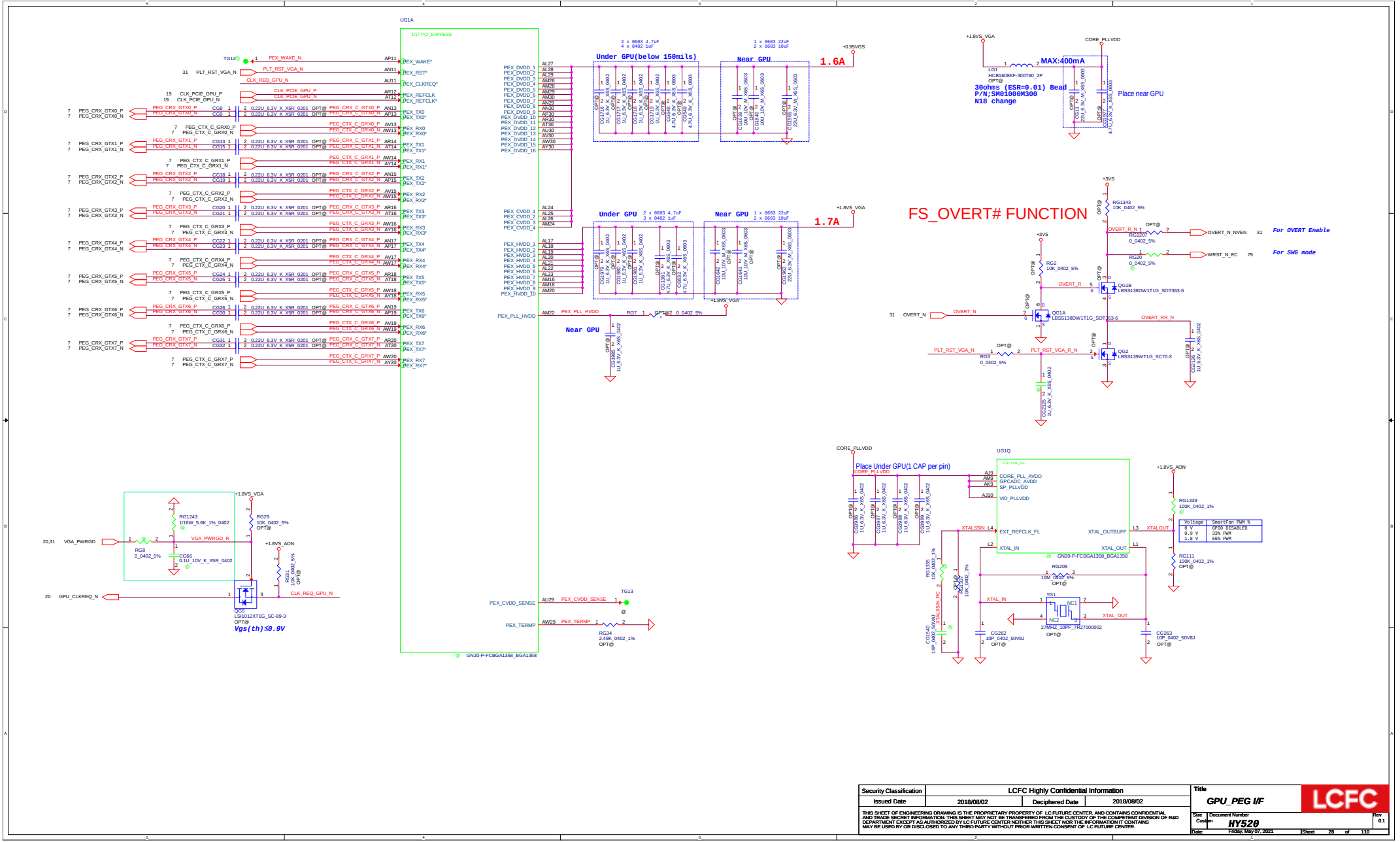

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	GPU_PEG I/F		
Size	Document Number		Rev
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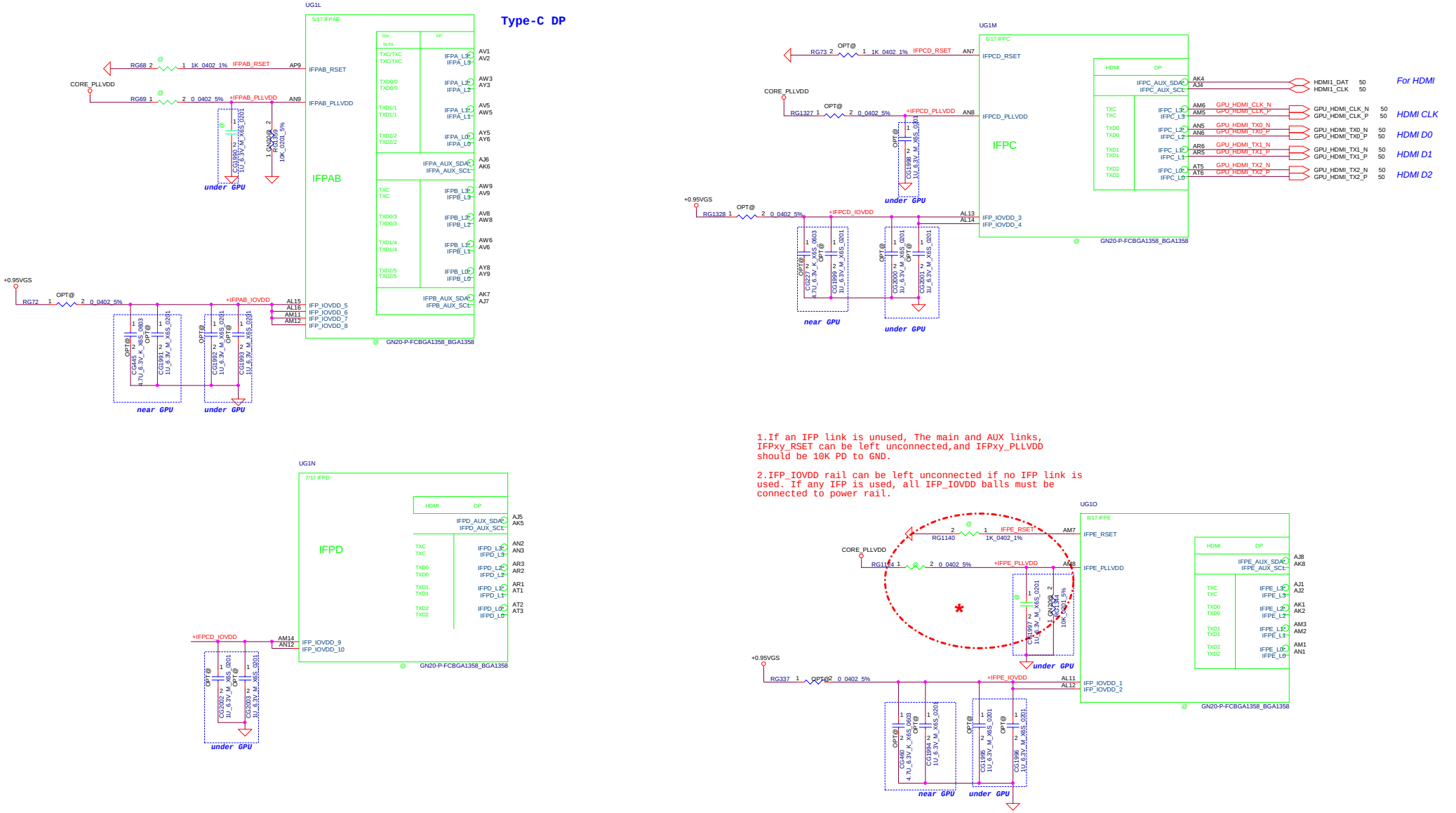
Type-C DP



1.If an IFP link is unused, The main and AUX links, IFPxy_RSET can be left unconnected,and IFPxy_PLLVDD should be 10K PD to GND.

2.IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

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Title: GPU_DIS I/F

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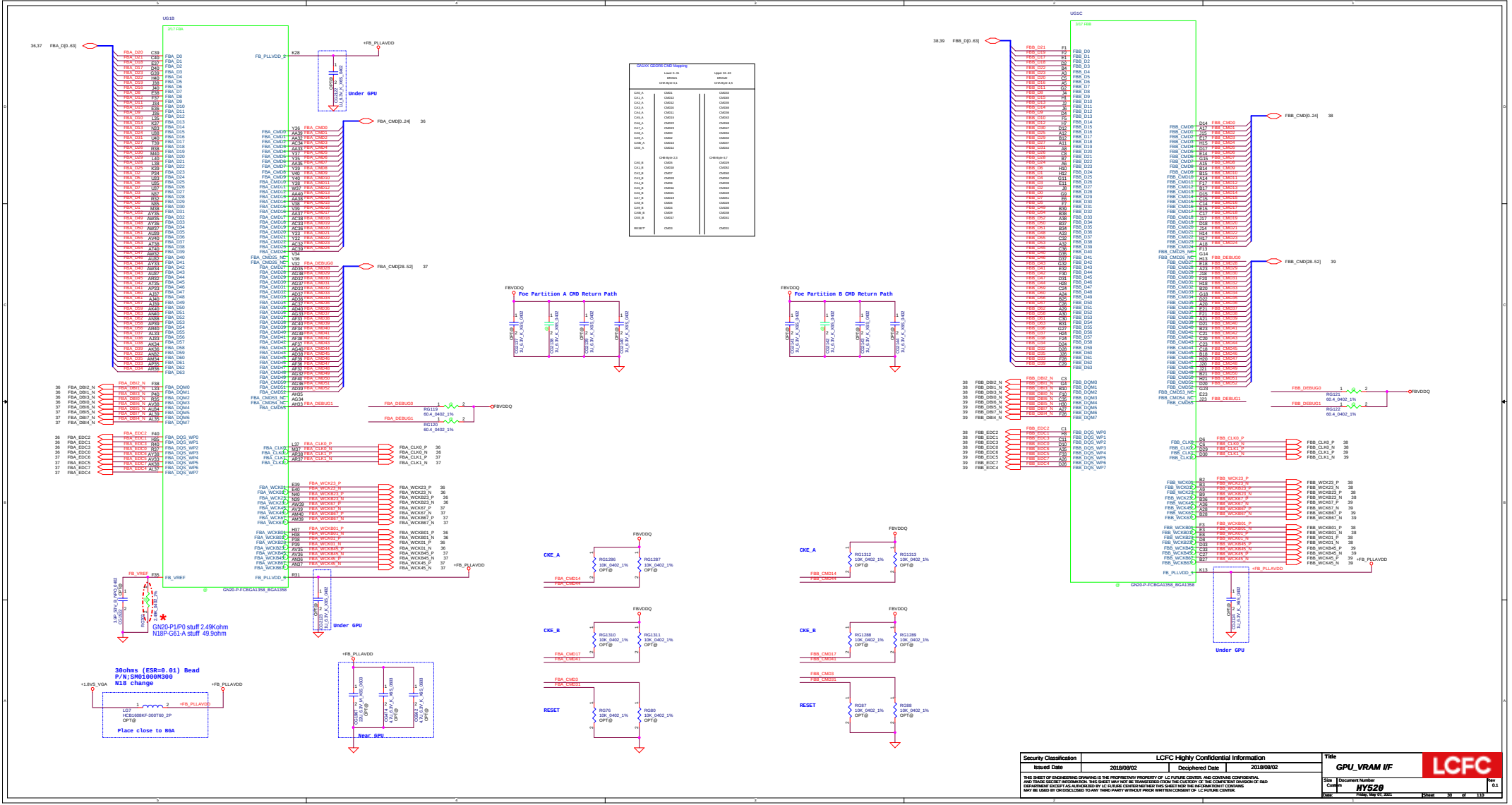
UG1B
2/17 FBA
36,37 FBA_D[0..63]
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
FBA_D16
FBA_D17
FBA_D18
FBA_D19
FBA_D20
FBA_D21
FBA_D22
FBA_D23
FBA_D24
FBA_D25
FBA_D26
FBA_D27
FBA_D28
FBA_D29
FBA_D30
FBA_D31
FBA_D32
FBA_D33
FBA_D34
FBA_D35
FBA_D36
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FBA_D39
FBA_D40
FBA_D41
FBA_D42
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FBA_D52
FBA_D53
FBA_D54
FBA_D55
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
FB_PLLVDD_P
+FB_PLLAVDD
Under GPU
FBA_CMD[0..24] 36
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25_NC
FBA_CMD26_NC
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CMD31
FBA_CMD32
FBA_CMD33
FBA_CMD34
FBA_CMD35
FBA_CMD36
FBA_CMD37
FBA_CMD38
FBA_CMD39
FBA_CMD40
FBA_CMD41
FBA_CMD42
FBA_CMD43
FBA_CMD44
FBA_CMD45
FBA_CMD46
FBA_CMD47
FBA_DEBUG0
FBA_DEBUG1
FBA_CMD[28..52] 37
FBA_CMD50_NC
FBA_CMD53_NC
FBA_CMD54_NC
FBA_CMD55
FBA_DBI2_N
FBA_DBI3_N
FBA_DBI0_N
FBA_DBI1_N
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBA_EDC2
FBA_EDC3
FBA_EDC0
FBA_EDC1
FBA_EDC4
FBA_EDC5
FBA_EDC6
FBA_EDC7
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBA_CLK0_P
FBA_CLK0_N
FBA_CLK1_P
FBA_CLK1_N
FBA_WCK23_P
FBA_WCK23_N
FBA_WCK01_P
FBA_WCK01_N
FBA_WCKB23_P
FBA_WCKB23_N
FBA_WCKB01_P
FBA_WCKB01_N
FBA_WCK67_P
FBA_WCK67_N
FBA_WCK45_P
FBA_WCK45_N
FBA_WCKB67_P
FBA_WCKB67_N
FBA_WCKB45_P
FBA_WCKB45_N
FB_VREF
FB_PLLVDD_S
GN20-P-FCBGA1358_BGA1358
GN20-P1/P0 stuff 2.49kohm
N18P-G61-A stuff 49.9ohm
30ohms (ESR=0.01) Bead
P/N;SM01000M300
N18 change
+1.8VS_VGA
LG7
HCB1608KF-300T60_2P
Place close to BGA
Near GPU
GA10X GDDR6 CMD Mapping
Fbe Partition A CMD Return Path
Fbe Partition B CMD Return Path
FBVDDQ
FBVDDQ
CKE_A
CKE_B
RESET
FBA_CMD14
FBA_CMD15
FBA_CMD17
FBA_CMD16
FBA_CMD3
FBA_CMD31
RG1286
RG1287
RG1310
RG1311
RG76
RG80
RG1312
RG1313
RG1288
RG1289
RG87
RG88
UG1C
2/17 FBB
38,39 FBB_D[0..63]
FBB_D0
FBB_D1
FBB_D2
FBB_D3
FBB_D4
FBB_D5
FBB_D6
FBB_D7
FBB_D8
FBB_D9
FBB_D10
FBB_D11
FBB_D12
FBB_D13
FBB_D14
FBB_D15
FBB_D16
FBB_D17
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FBB_D62
FBB_D63
FBB_CMD[0..24] 38
FBB_CMD0
FBB_CMD1
FBB_CMD2
FBB_CMD3
FBB_CMD4
FBB_CMD5
FBB_CMD6
FBB_CMD7
FBB_CMD8
FBB_CMD9
FBB_CMD10
FBB_CMD11
FBB_CMD12
FBB_CMD13
FBB_CMD14
FBB_CMD15
FBB_CMD16
FBB_CMD17
FBB_CMD18
FBB_CMD19
FBB_CMD20
FBB_CMD21
FBB_CMD22
FBB_CMD23
FBB_CMD24
FBB_CMD25_NC
FBB_CMD26_NC
FBB_CMD27
FBB_CMD28
FBB_CMD29
FBB_CMD30
FBB_CMD31
FBB_CMD32
FBB_CMD33
FBB_CMD34
FBB_CMD35
FBB_CMD36
FBB_CMD37
FBB_CMD38
FBB_CMD39
FBB_CMD40
FBB_CMD41
FBB_CMD42
FBB_CMD43
FBB_CMD44
FBB_CMD45
FBB_CMD46
FBB_CMD47
FBB_DEBUG0
FBB_DEBUG1
FBB_CMD[28..52] 39
FBB_CMD50_NC
FBB_CMD53_NC
FBB_CMD54_NC
FBB_CMD55
FBB_DBI2_N
FBB_DBI3_N
FBB_DBI0_N
FBB_DBI1_N
FBB_DQM0
FBB_DQM1
FBB_DQM2
FBB_DQM3
FBB_DQM4
FBB_DQM5
FBB_DQM6
FBB_DQM7
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FBB_EDC6
FBB_EDC7
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FBB_DQS_WP1
FBB_DQS_WP2
FBB_DQS_WP3
FBB_DQS_WP4
FBB_DQS_WP5
FBB_DQS_WP6
FBB_DQS_WP7
FBB_CLK0_P
FBB_CLK0_N
FBB_CLK1_P
FBB_CLK1_N
FBB_WCK23_P
FBB_WCK23_N
FBB_WCK01_P
FBB_WCK01_N
FBB_WCKB23_P
FBB_WCKB23_N
FBB_WCKB01_P
FBB_WCKB01_N
FBB_WCK67_P
FBB_WCK67_N
FBB_WCK45_P
FBB_WCK45_N
FBB_WCKB67_P
FBB_WCKB67_N
FBB_WCKB45_P
FBB_WCKB45_N
FB_PLLVDD_+
+FB_PLLAVDD
Under GPU
GN20-P-FCBGA1358_BGA1358
Security Classification
LCFC Highly Confidential Information
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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Title
GPU_VRAM I/F
LCFC
Size
Custom
Document Number
HY520
Rev
0.1
Date:
Friday, May 07, 2021
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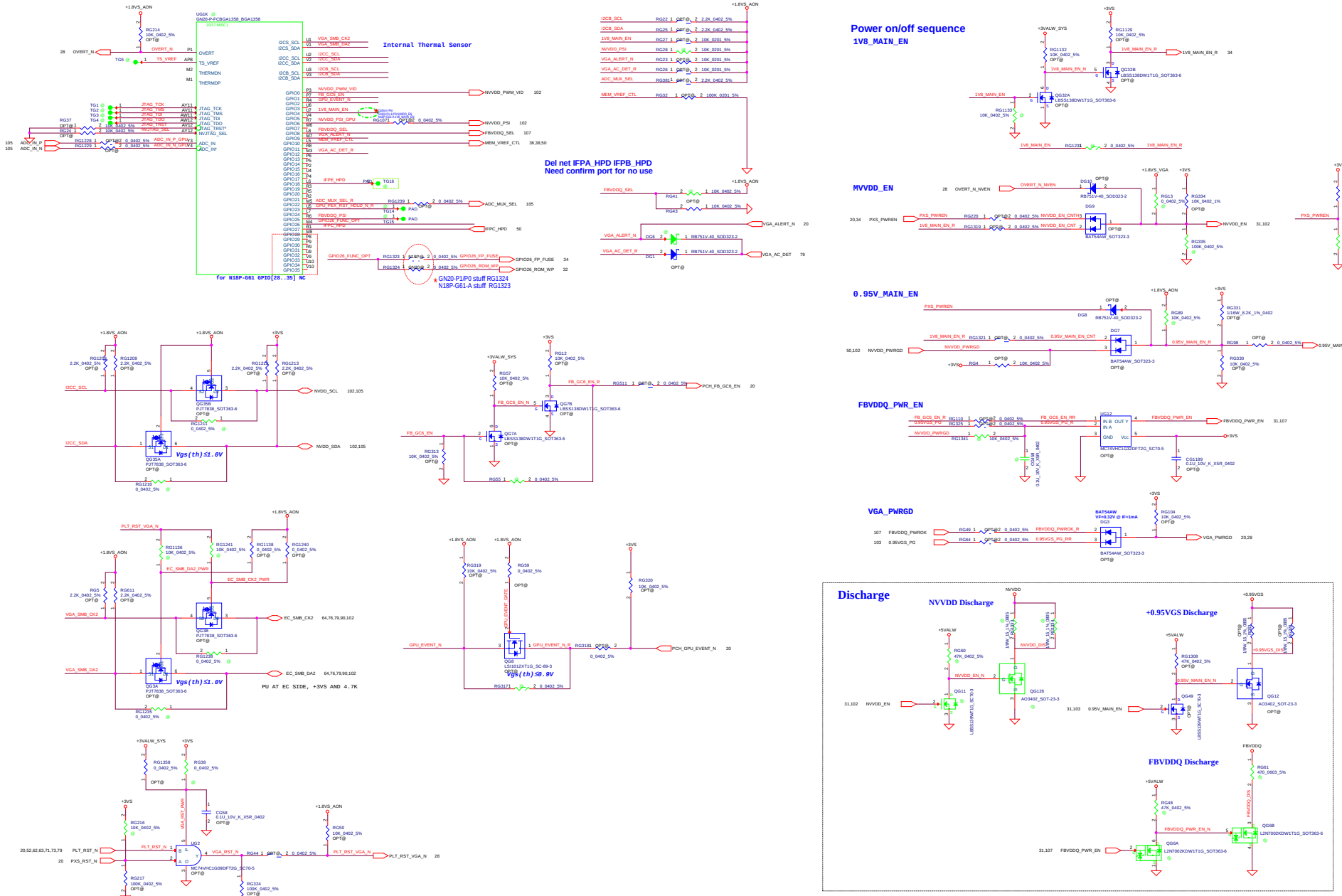
of
110



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Title: GPU_GPIO

LCFC

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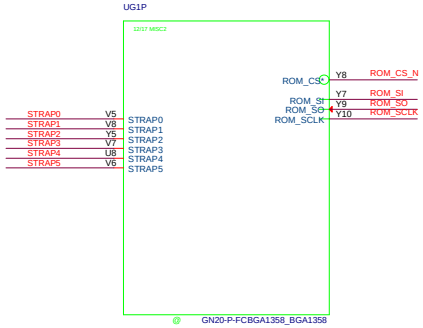
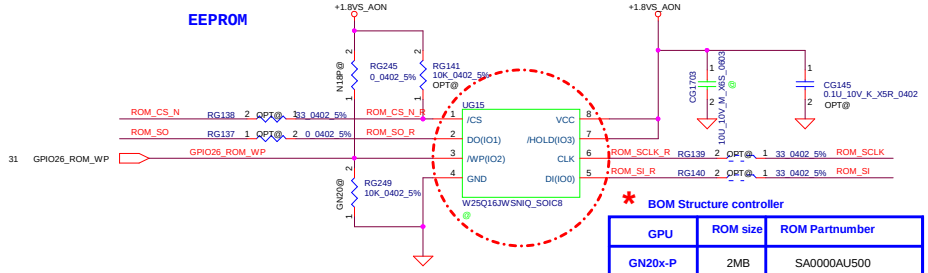
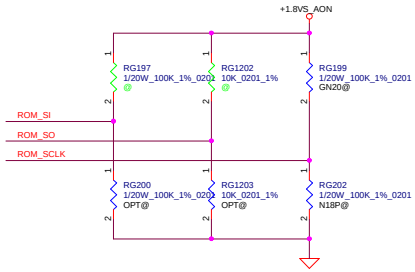




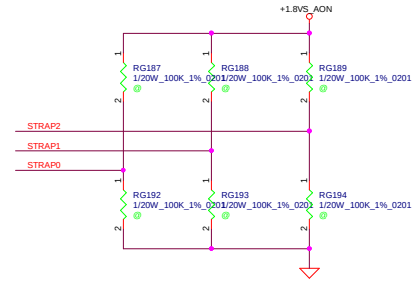
* BOM Structure controller

GPU	ROM size	ROM Partnumber
GN20x-P	2MB	SA0000AU500
N18P-G61-A	1MB	SA000080E00



1:ENABLE 0:DISABLE
SOR0 DISABLE
SOR1/2/3 ENABLE

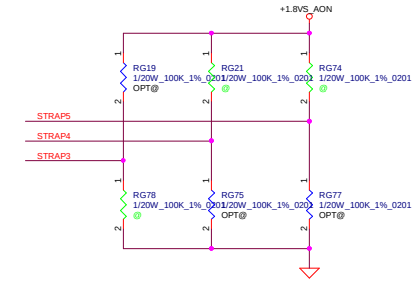
GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N18P-G61-A	L	L	L	ENABLE OVERT*
GN20x-P	L	L	H	ENABLE OVERT*



VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
GN20x-P0 N18P-G61-A 4GB	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H
	Hynix 8Gb	H56C8H24AIR-S2C	2(0x0002)	L	H	L

* Hynix VRAM only for GN20x-P1/P0



VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0 *	0	1

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1:DEVID_SEL for G-SYNC SKU

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

Title			
GPU_Strap			
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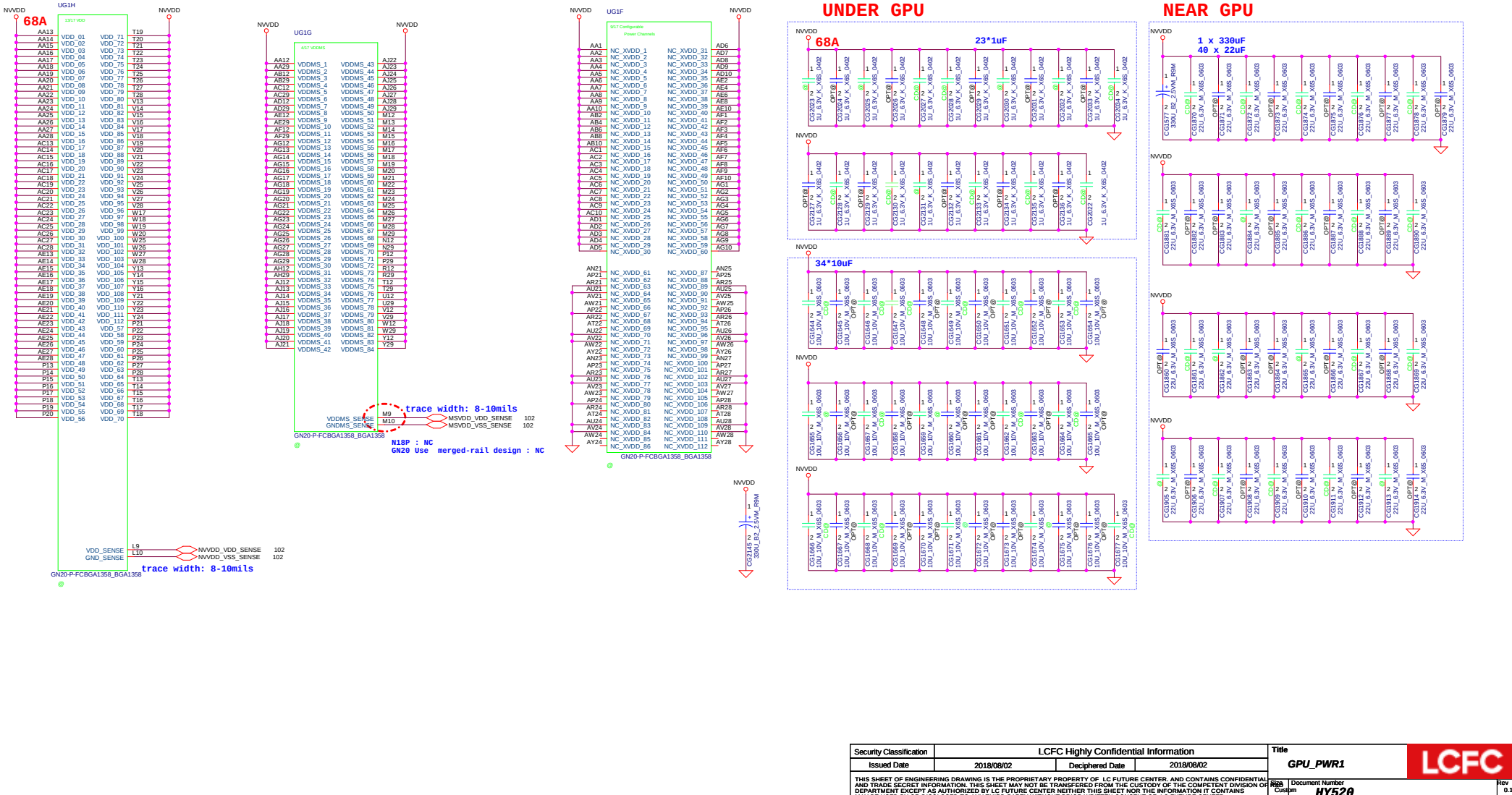

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Title: GPU_PWR1

LCFC

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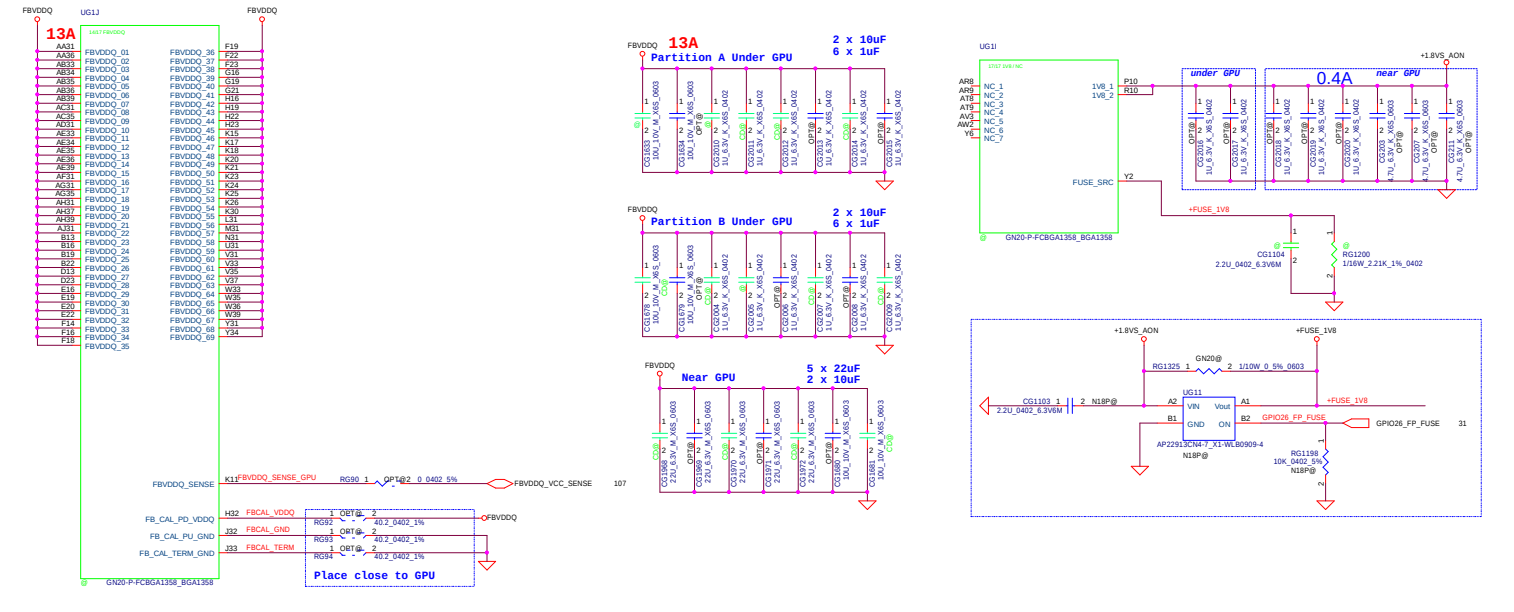

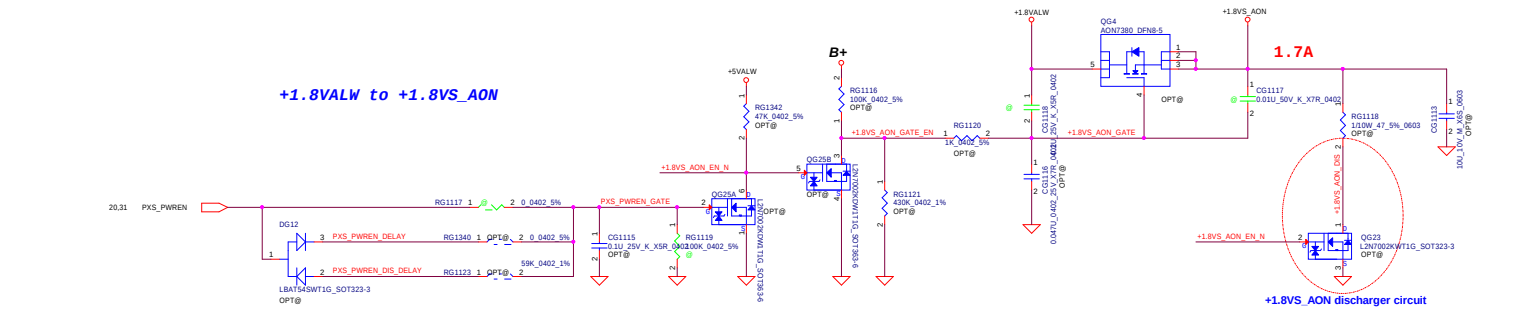

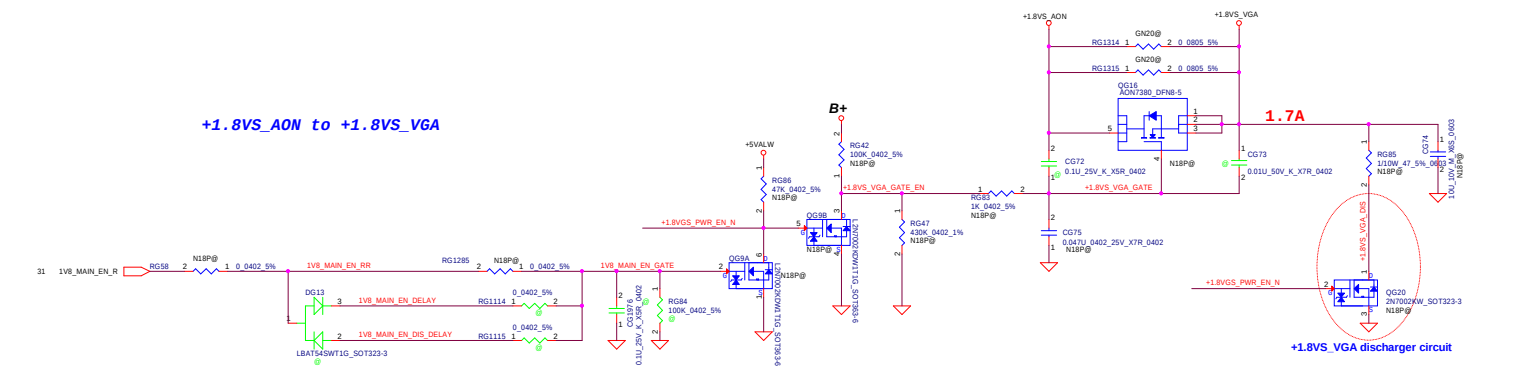

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Title	GPU_PWR2		
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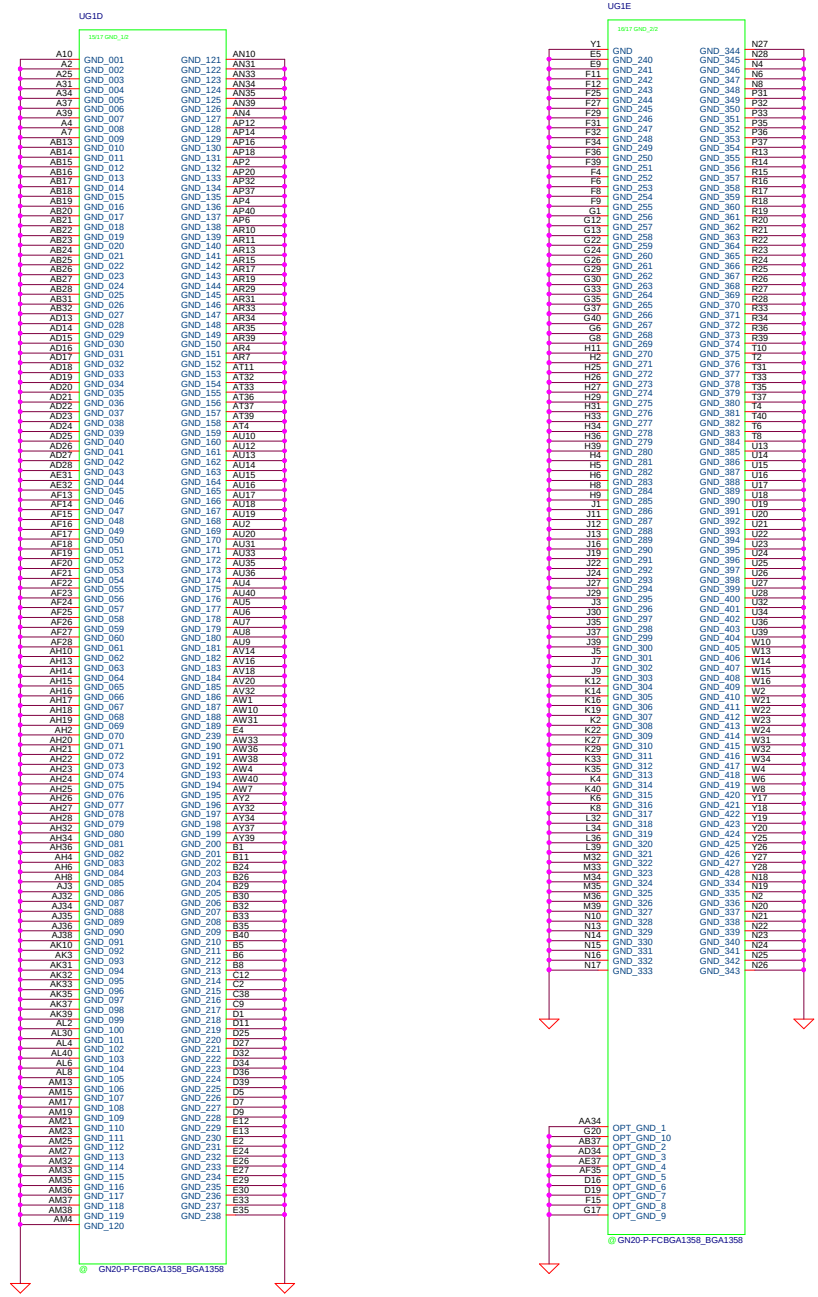
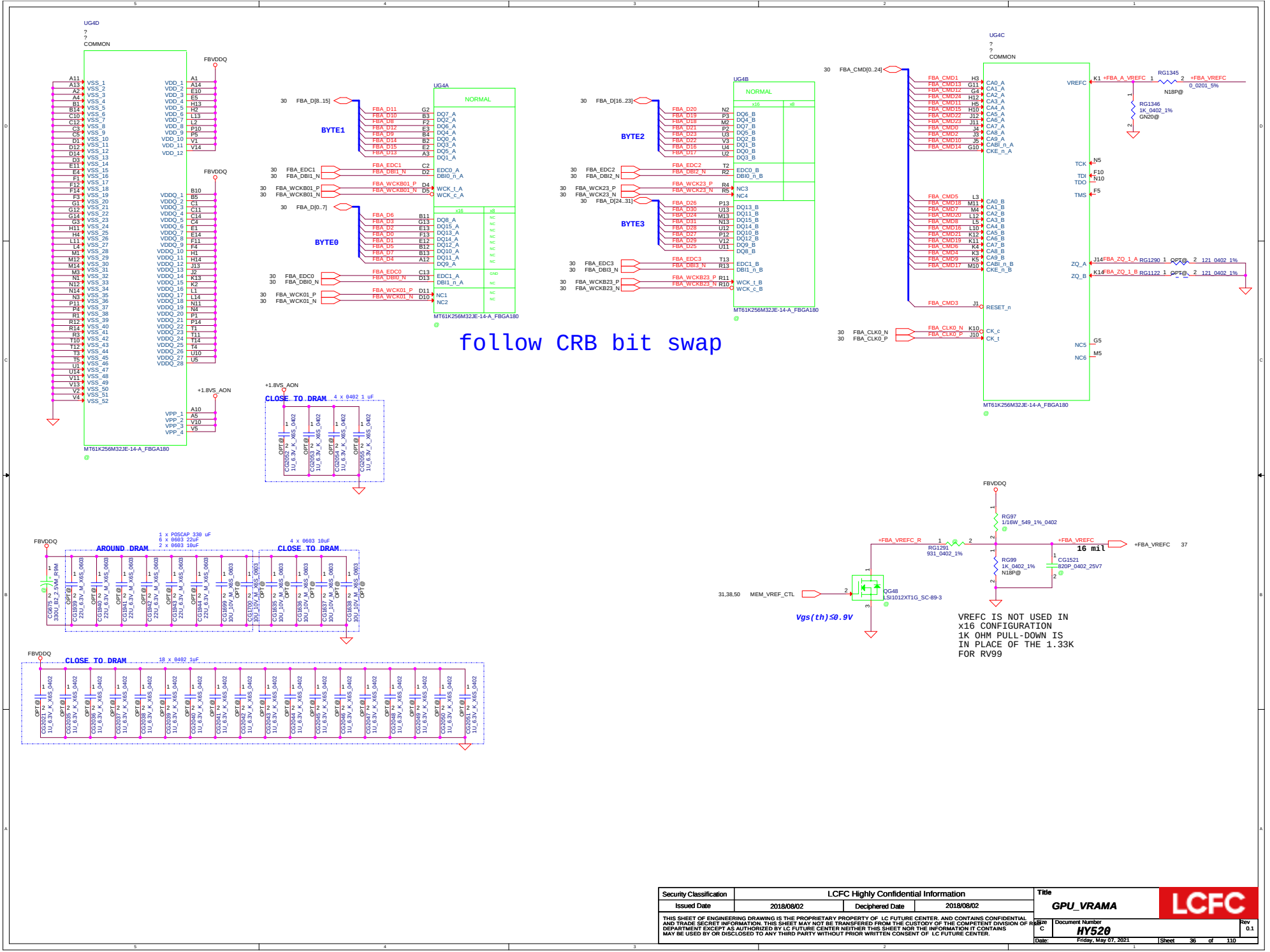


Title	GPU_GND		
Size C	Document Number HY520		Rev 0.1
Date: Friday, May 07, 2021	Sheet 35 of 110		



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GPU_VRAMA

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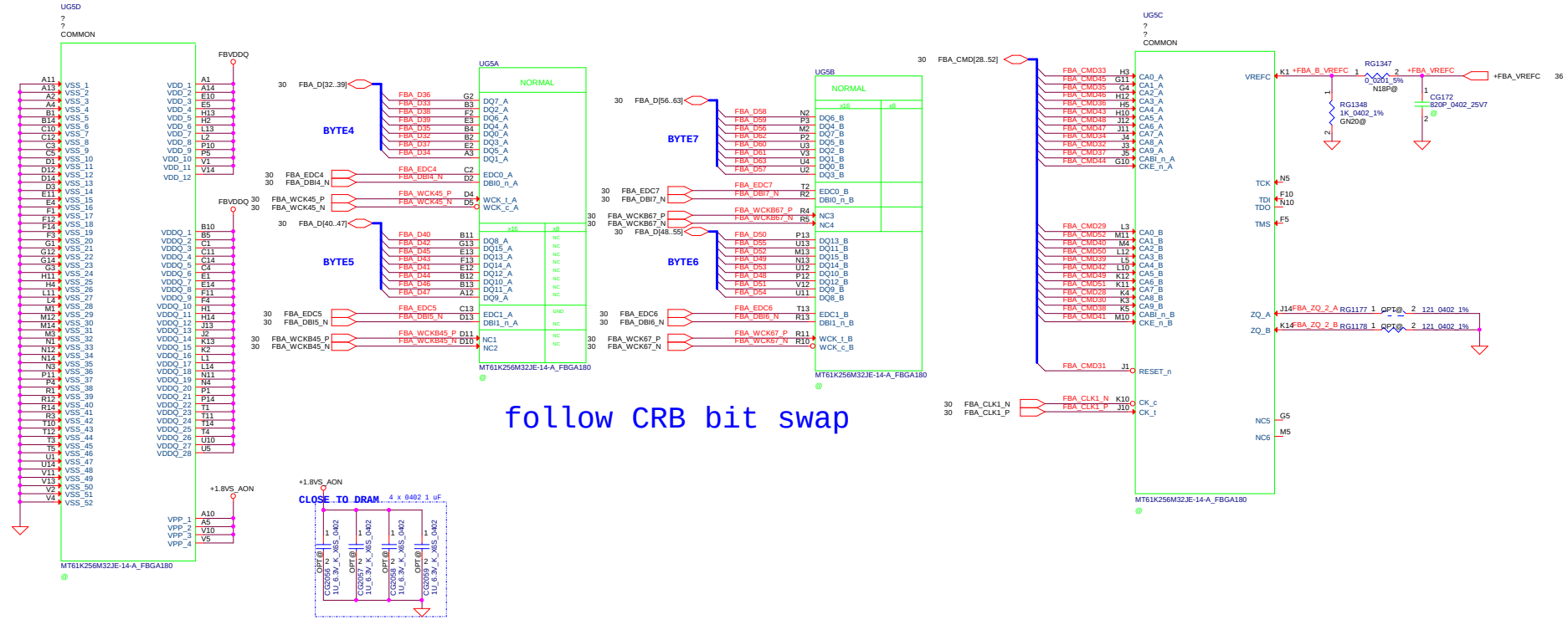

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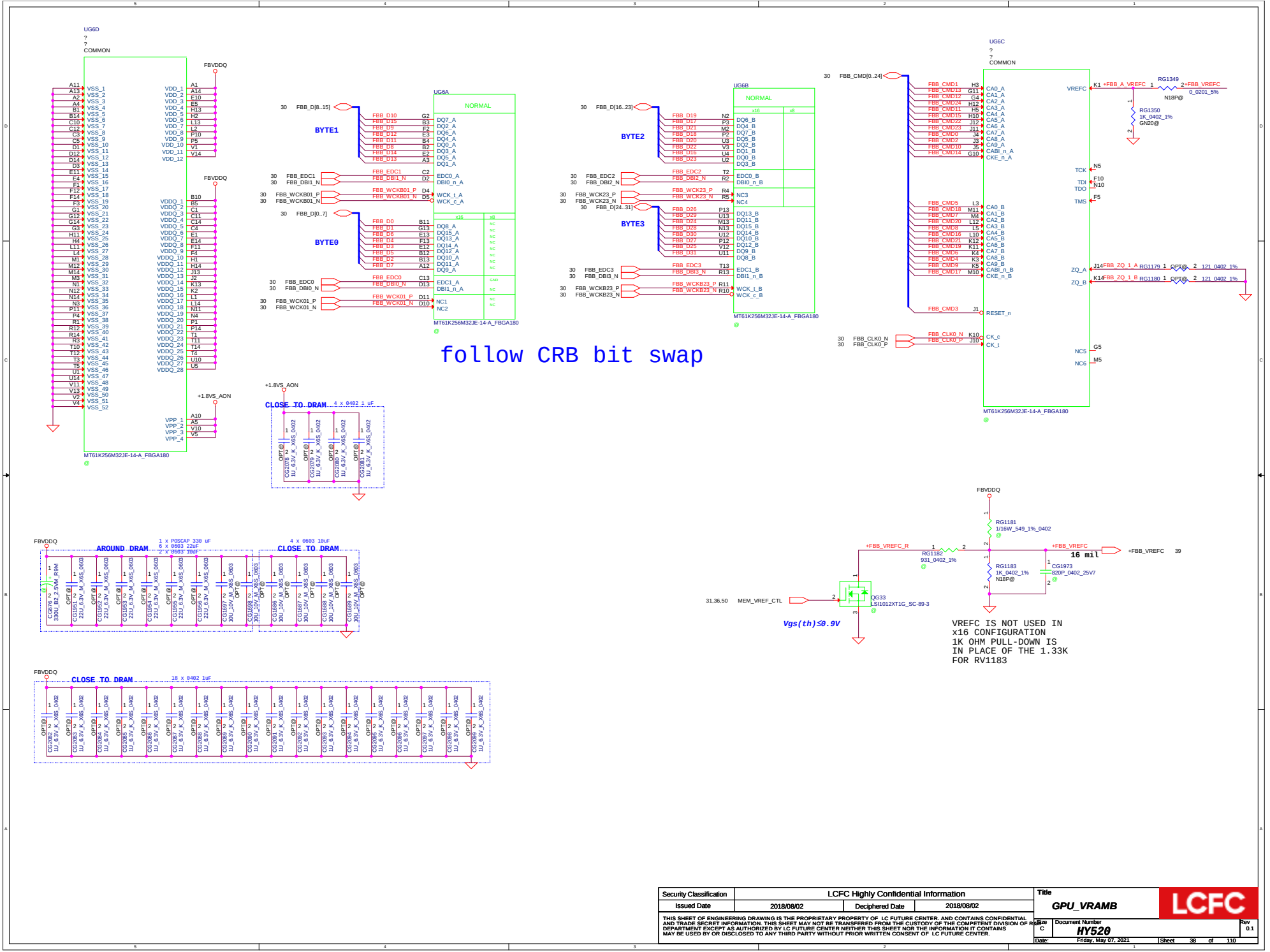
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	GPU_VRAMA		
Size C	Document Number HY520		Rev 0.1
Date: Friday, May 07, 2021	Sheet 37 of 110		



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	GPU_VRAMB		
Size	C	Document Number	HY520
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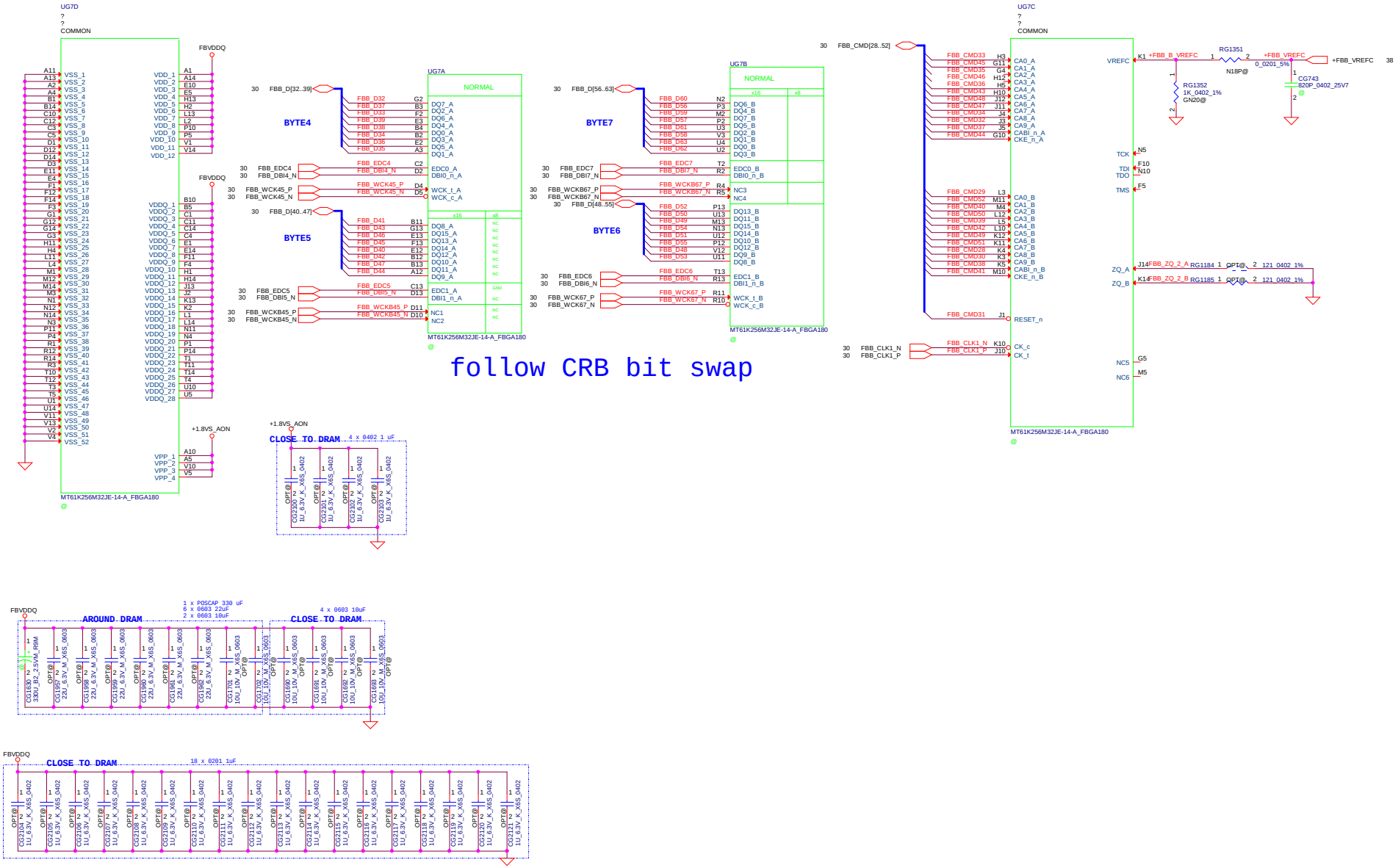

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GPU_VRAMB

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C	***HY520***	0.1

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Security Classification	LCFC Highly Confidential Information		
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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

Blank

LCFC

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C	***HY520***	0.1

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EDP_SW :Port switching control configuration; Internal pull down
at ~150Kꭥ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected

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Title

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Custom	*HY520*	0.1

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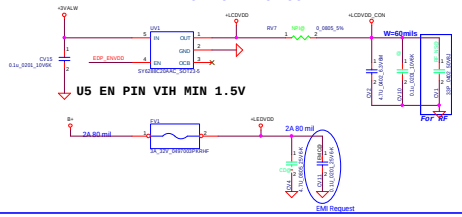
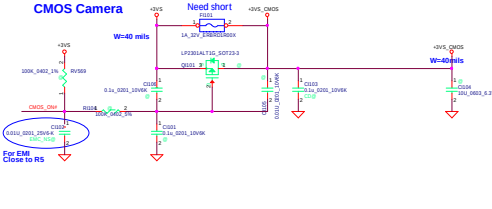
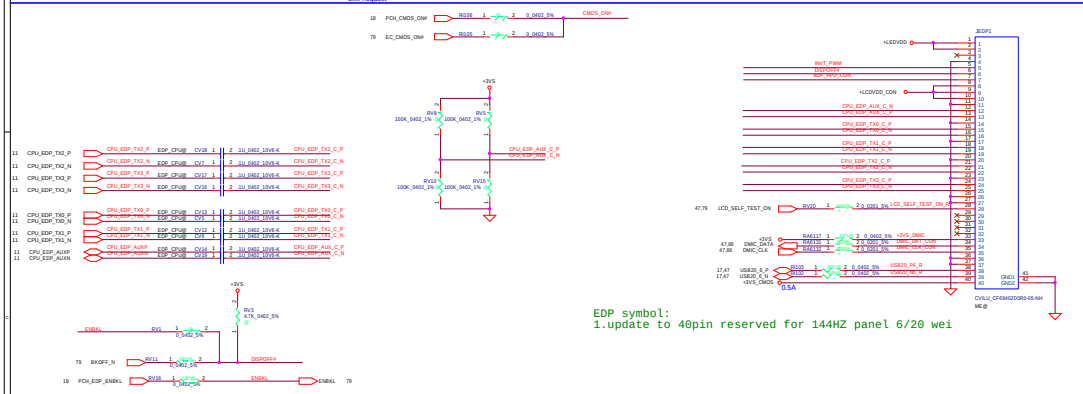
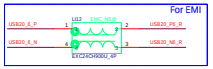
LCD POWER CIRCUIT

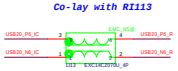


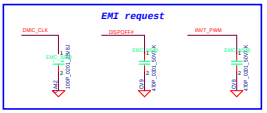
CMOS Camera

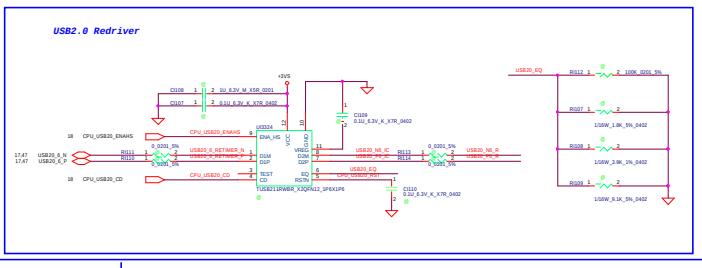


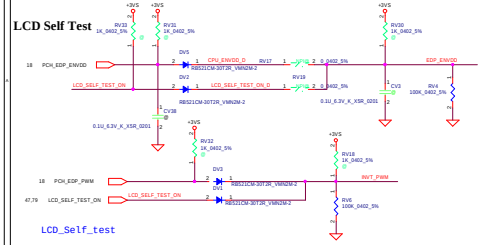


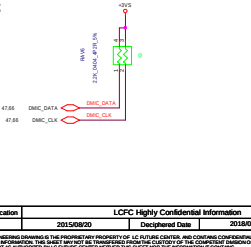












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Issued Date: 2015/08/20	Deciphered Date: 2018/09/20		
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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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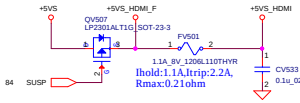
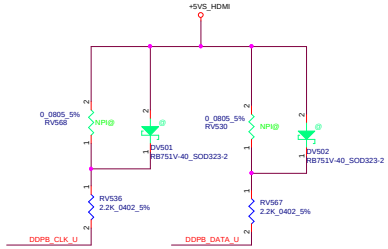
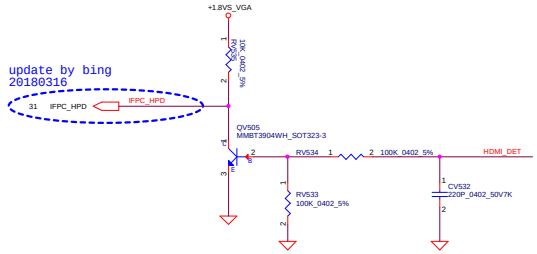
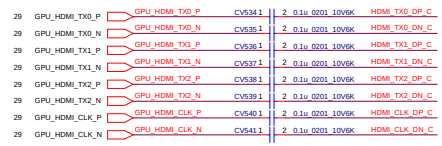
HDMI Power

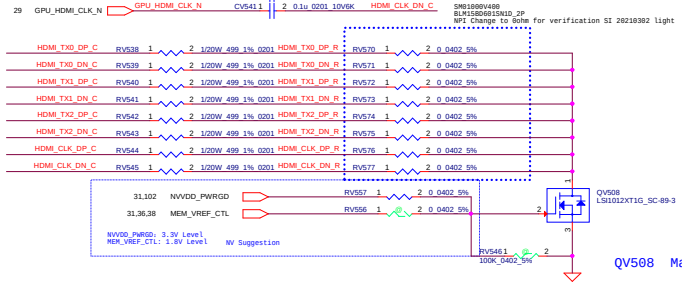




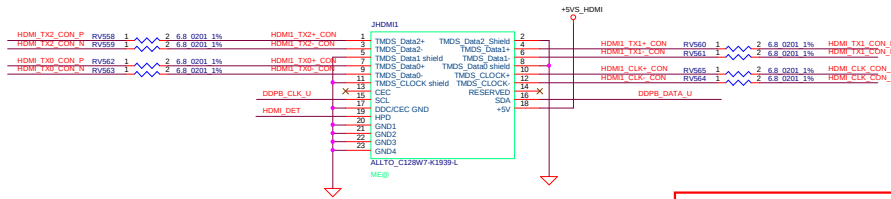
update by bing
20180316



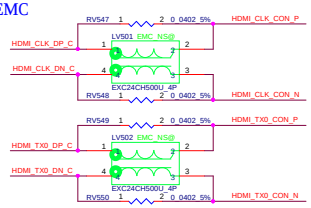


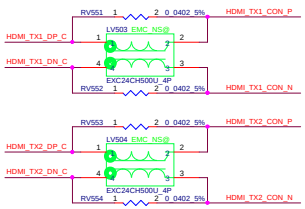


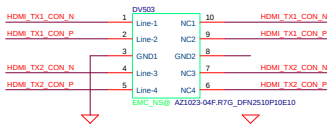
QV508 Max Vgs 0.9V



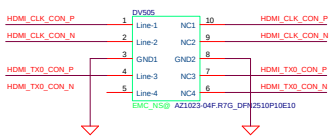
EMC

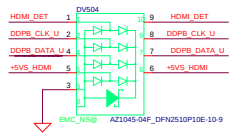


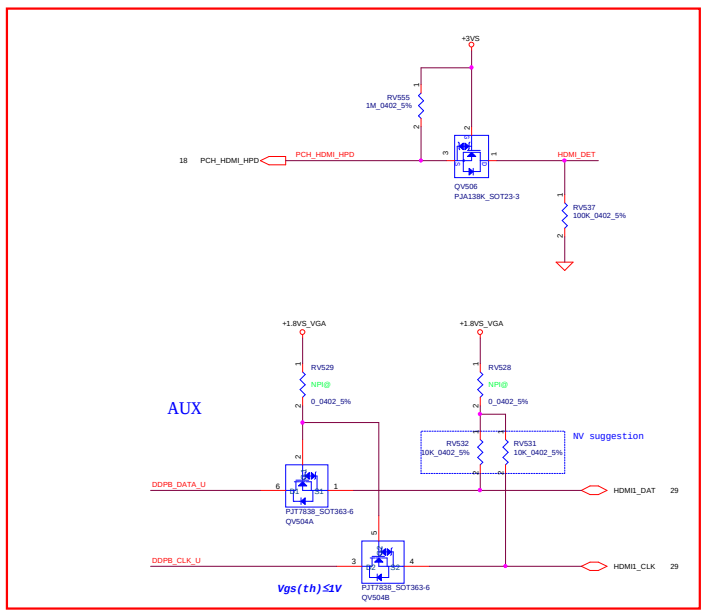




DV501 & DV503 Change to SC300005R00







If mounted re-driver, need to remove this parts

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: HDMI_CONN

LCFC

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TBT portA/rear side

+3VALW

VINA_3V3

RU2011 10K/0 2 1/10W 0 5% 0603

VBUS_TBTA

VINA_3V3

VCC3_LDO_PDA

CU201 4.7U_25V_M_X5R_0402

DU201 MSR20F30NX7SG_DSN2-2

DU202 SP1224-01UTG_UDFN-6

+5VALW

CU205 CU206 CU207 CU208 CU209 CU210 Z2UC_6.3VC_MC_X5RC_0603

UU201 SN2001024YGBR_DSBGA50

VSYS VIN_3V3 LDO_1V5_1 LDO_1V5_2 LDO_3V3 PA_VBUS_1 PA_VBUS_2 PA_VBUS_3 PB_VBUS_1 PB_VBUS_2 PB_VBUS_3 GND

PP5V_1 PP5V_2 PP5V_3 PP5V_4 PP5V_5 PP5V_6 PP5V_7 PP5V_8

PA_GATE_VSYS PA_GATE_VBUS PB_GATE_VSYS PB_GATE_VBUS

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9

88 TBTA_GATE_VSYS — RU205 1 2 0 0201 5% — TBTA_GATE_VSYS_R

52 TBTA_RESET_N — TBTA_RESET_N — RU208 1 NDW@ 2 0 0201 5% — PD_TBTA_RESET_N

21,79,84 PM_SLP_S4_N — RU210 1 NDW@ 2 0 0201 5% — PDA_PM_SLP_S4_N

52 TBTA_PWR_EN — TBTA_PWR_EN — RU214 1 NDW@ 2 0 0201 5% — PD_TBTA_PWR_EN

88 PD_ACK_SNK1 — RU216 1 NDW@ 2 0 0201 5% — PD_ACK_SNK1_R

18 USB_OC4_N — USB_OC4_N — RU218 1 NDW@ 2 0 0201 5% — USB_OC4_R_N

20 GPPC_B2_VRALERT_N — RU221 1 NDW@ 2 0 0201 5% — GPPC_B2_VRALERT_A_N

20,52 TBTA_FORCE_PWR — RU225 1 NDW@ 2 0 0201 5% — TBTA_FORCE_PWR_R

ADCIN1 PDA_ADCIN1

ADCIN2 VCC3_LDO_PDA

PA_CC1 TBTA_CC1 53

PA_CC2 TBTA_CC2 53

PB_CC1 PD1_B_CC1

PB_CC2 PD1_B_CC2

CU211 220P_25V_X7R_0201 CU212 220P_25V_X7R_0201

I2C_EC_IRQ# — EC_I2C_INT4_PDA_R — RU209 1 2 0 0201 5% — EC_I2C_INT4_PDA_N — EC_I2C_INT4_PDA_N 79

I2C_EC_SCL — EC_SMB_CK4_PDA_R — RU211 1 2 0 0402 5% — EC_SMB_CK4_PD — EC_SMB_CK4_PD 79 Slave EC

I2C_EC_SDA — EC_SMB_DA4_PDA_R — RU212 1 2 0 0402 5% — EC_SMB_DA4_PD — EC_SMB_DA4_PD 79

I2C2S_IRQ# — PMC_ALERT_PDA_N — RU217 1 2 0 0201 5% — PCH_PMC_ALERT_PD_N — PCH_PMC_ALERT_PD_N 18,20

I2C2S_SCL — SML1_CLK_R_PDA — RU219 1 2 0 0201 5% — PD_I2C2_SCL — PD_I2C2_SCL 20 Slave PCH SML1

I2C2S_SDA — SML1_DATA_R_PDA — RU220 1 2 0 0201 5% — PD_I2C2_SDA — PD_I2C2_SDA 20

I2C3M_IRQ# — TBTA_I2C_INT_R_N — RU222 1 2 0 0201 5% — TBTA_I2C_INT_N — TBTA_I2C_INT_N 52

I2C3M_SCL — TBTA_I2C_SCL_R — RU223 1 2 0 0402 5% — TBTA_I2C_SCL — TBTA_I2C_SCL 52 Master BB retimer

I2C3M_SDA_1 I2C3M_SDA_2 — TBTA_I2C_SDA_R — RU224 1 2 0 0402 5% — TBTA_I2C_SDA — TBTA_I2C_SDA 52

VCC3_LDO_PDA

PDA_ADCIN1 — RU202 1 2 10K_1% 1/20W 0201 — RU203 2 1 12.1K_1% 1/20W 0201

TABLE I2C Addressing

I2C1	Master: EC Slave: PD	TBTA PORT	0x23
		TBTC PORT	0x27
I2C2	Master: PMC Slave: PD	TBTB PORT	0x23
		TBTC PORT	0x27
I2C3	Master: PD Slave: RT	TBTB PORT	T.B.D.
		TBTC PORT	T.B.D.

need verify address

VCC3_LDO_PDA

EC — EC_I2C_INT4_PDA_N — RU204 1 2 10K 0201 5%

PCH — PD_I2C2_SCL / PD_I2C2_SDA — RPU201 1 4 2.2K_0404_4P2R_5% 2 3 — PCH_PMC_ALERT_PD_N — RU206 1 2 10K 0201 5%

BB Retimer — TBTA_I2C_SCL / TBTA_I2C_SDA — RPU202 1 4 2.2K_0404_4P2R_5% 2 3 — TBTA_I2C_INT_N — RU207 1 2 10K 0201 5%

PD1_B_CC1 — RU213 1 2 0 0201 5%

PD1_B_CC2 — RU215 1 2 0 0201 5%

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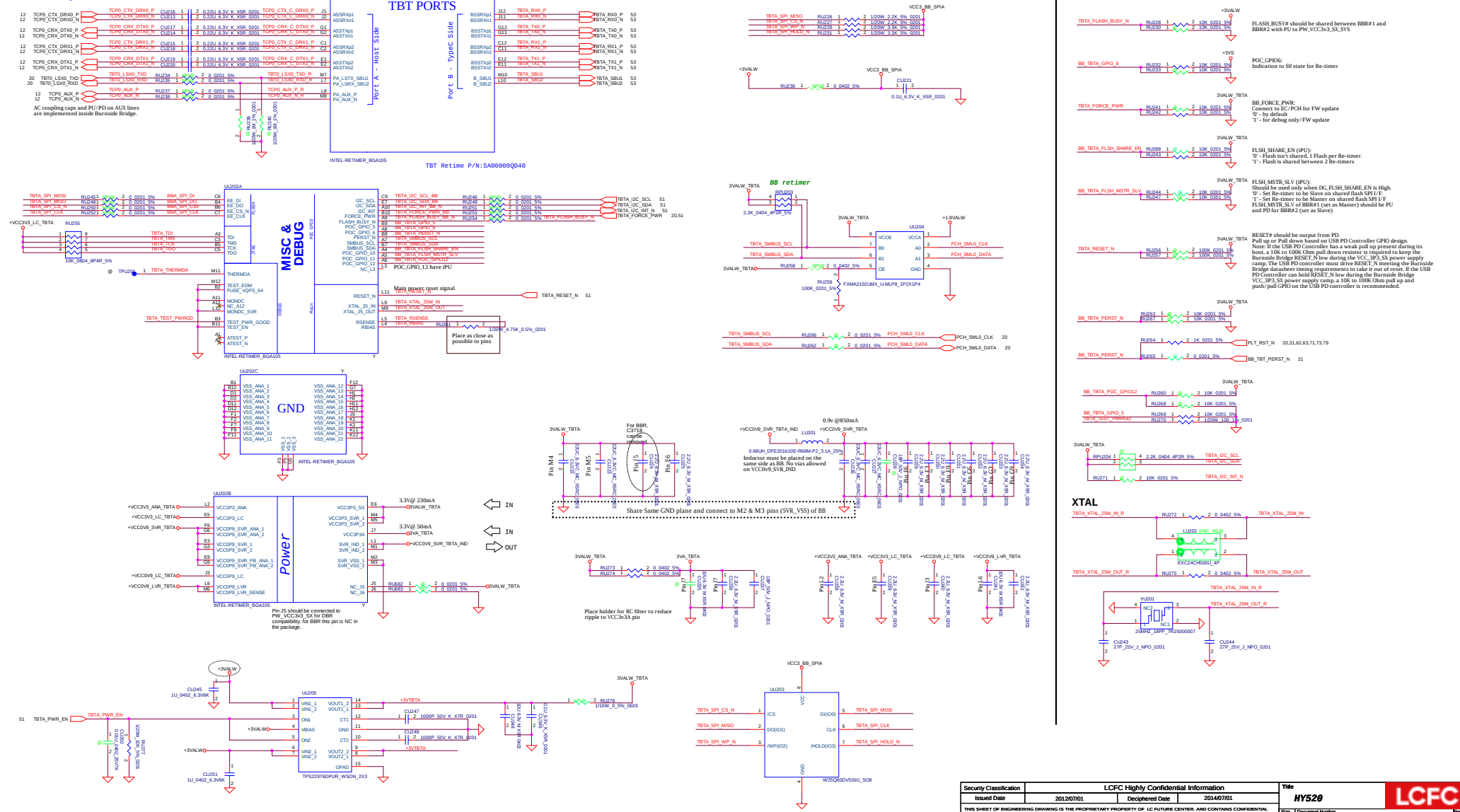
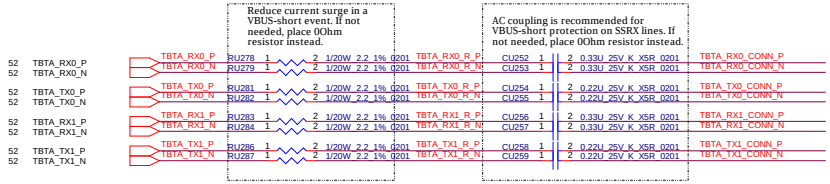
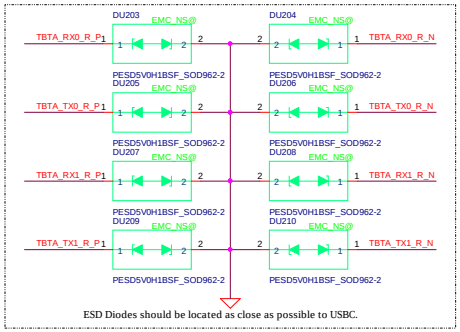
Burnside Bridge Re-Timer

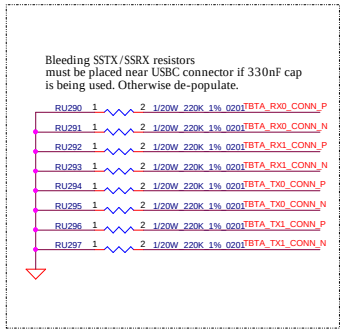


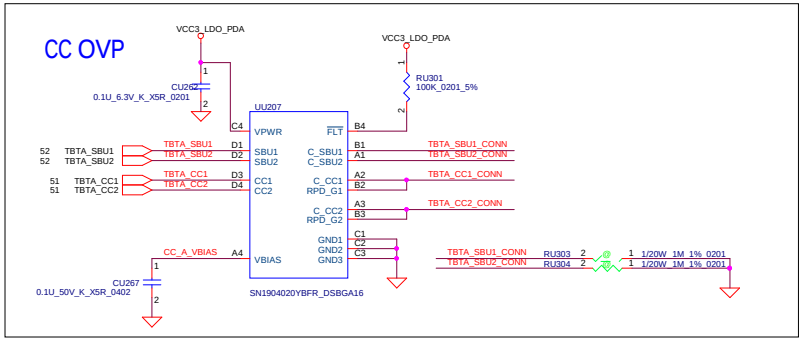
Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

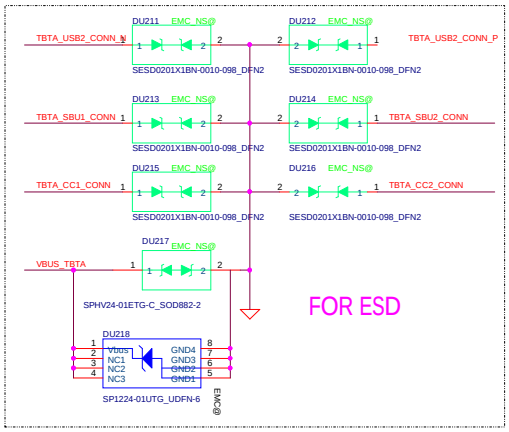
Title			
HY520			
Size	Document Number		Rev
Custom	TBT_RETIMER		0.1
Date:	Friday, May 07, 2021	Sheet 52 of 110	

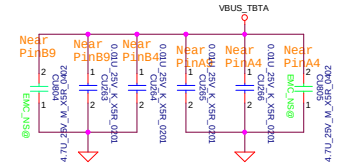




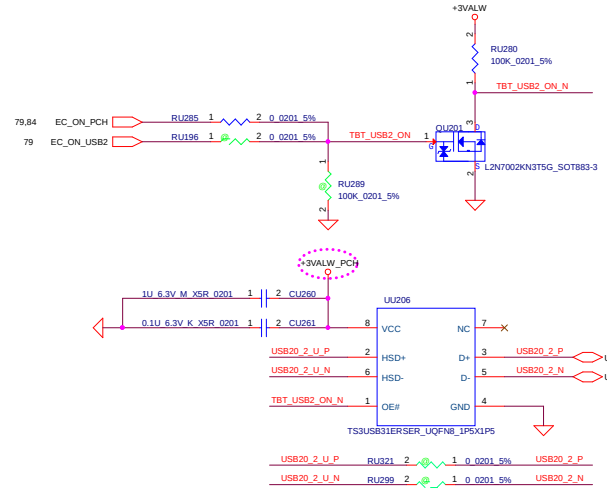


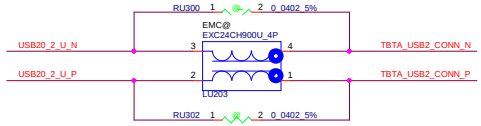


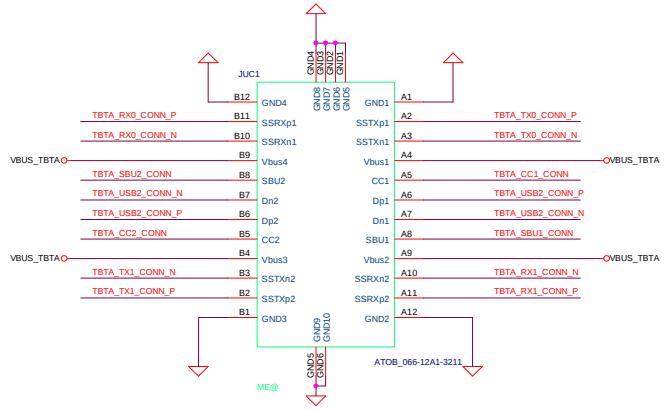




Vinafix







Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	TBT_CONN		
Size	Document Number		Rev
C	HY520		0.1
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: ***Blank***

LCFC

Size	Document Number	Rev
Custom	***HY520***	0.1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Blank

LCFC

Size	Document Number	Rev
Custom	HY520	0.1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: ***Blank***

LCFC

Size	Document Number	Rev
Custom	***HY520***	0.1

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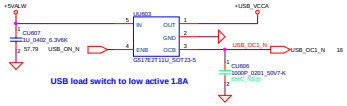
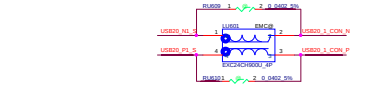
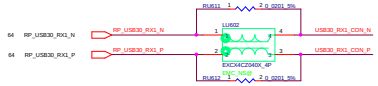
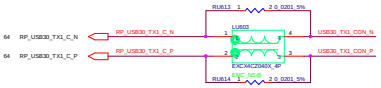
LEFT SIDE USB3.2 Gen2 PORT x1

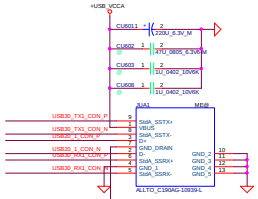


USB load switch to low active 1.8A

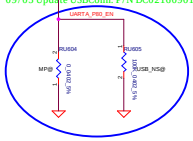








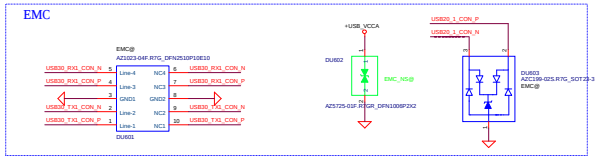
09/05 Update USBConn P/N DC021609011 wei



09/20SF Update USB debug CONN GND pin follow TINY5

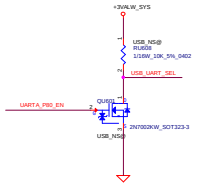
USB Conn

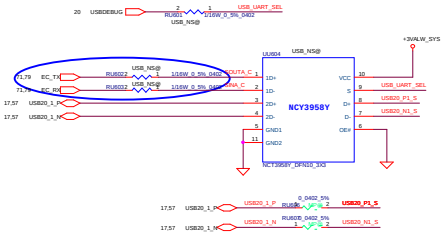
2021/03/11 Change DU601 for Gen2



For USB Debug Function

09/20SF add USB debug follow TINY5
change from SA00007WL0D to SA00007WL00 SF1001
SVT non-staff0322SF



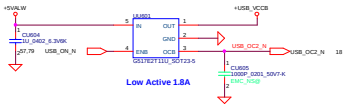


USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

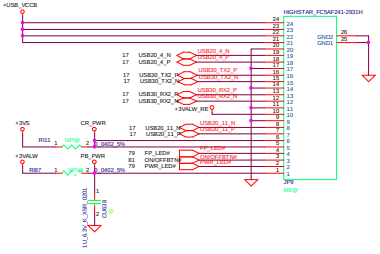
UART/A_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

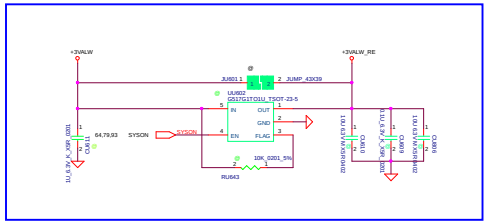
OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

RIGHT SIDE USB3.0 PORT x2



Low Active 1.8A





Security Classification	LCFC Highly Confidential Information		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: USB3.0 PORT (LEFT)

LCFC

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

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LCFC

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C	***HY520***	0.1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

Blank

LCFC

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C	***HY520***	0.1

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Delete USB3.0 Reapter Remove to DB board

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Blank		LCFC
Size	Document Number		Rev
D	HY520		0.1
Date:	Friday, May 07, 2021	Sheet	60 of 110

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

Blank

LCFC

Size	Document Number	Rev
B	***HY520***	0.1

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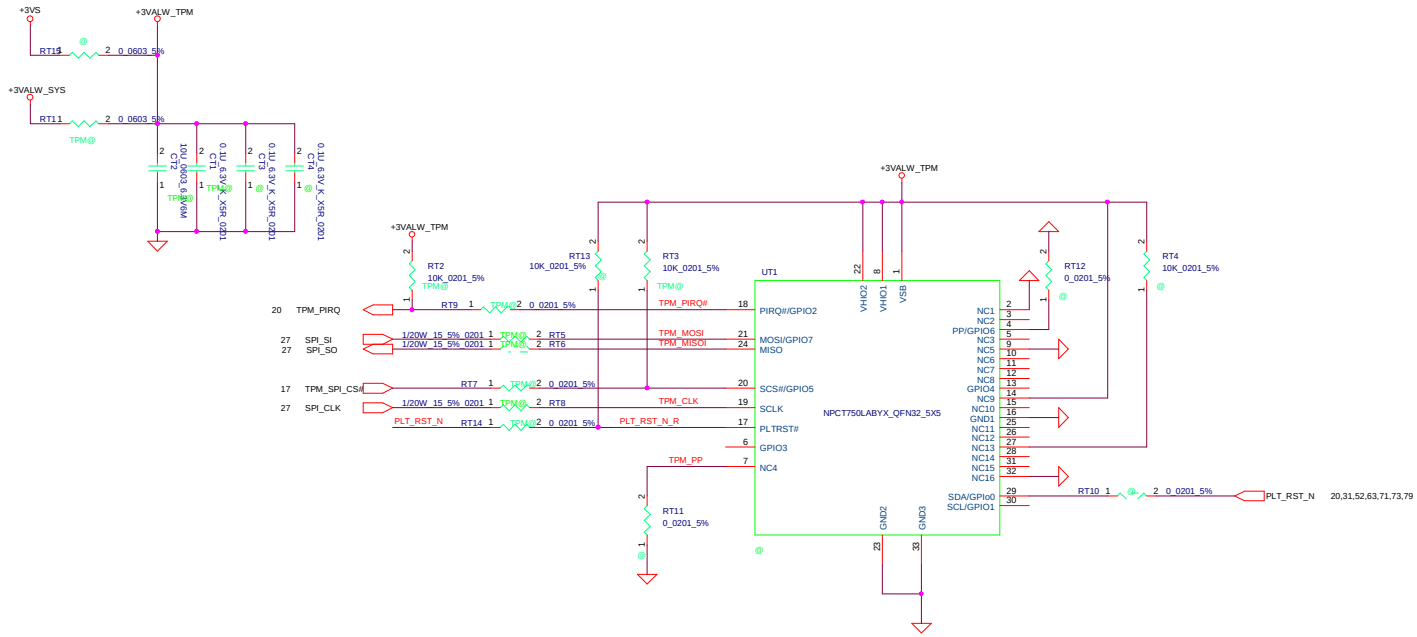
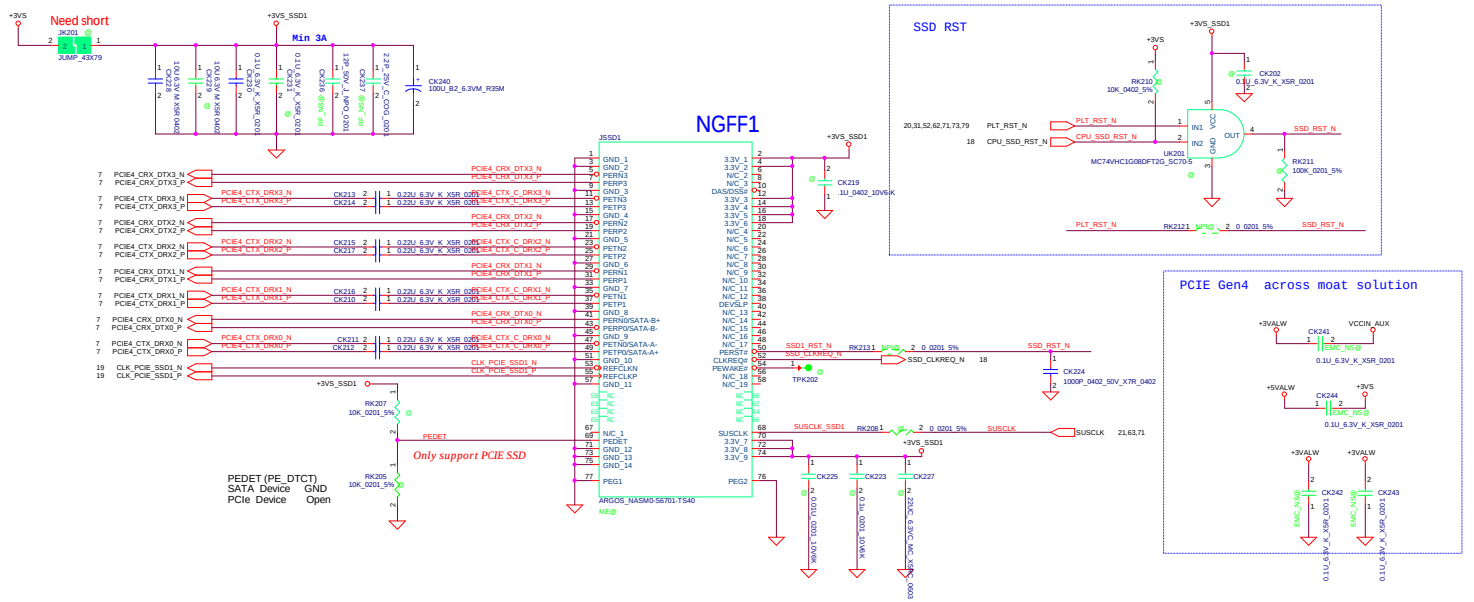


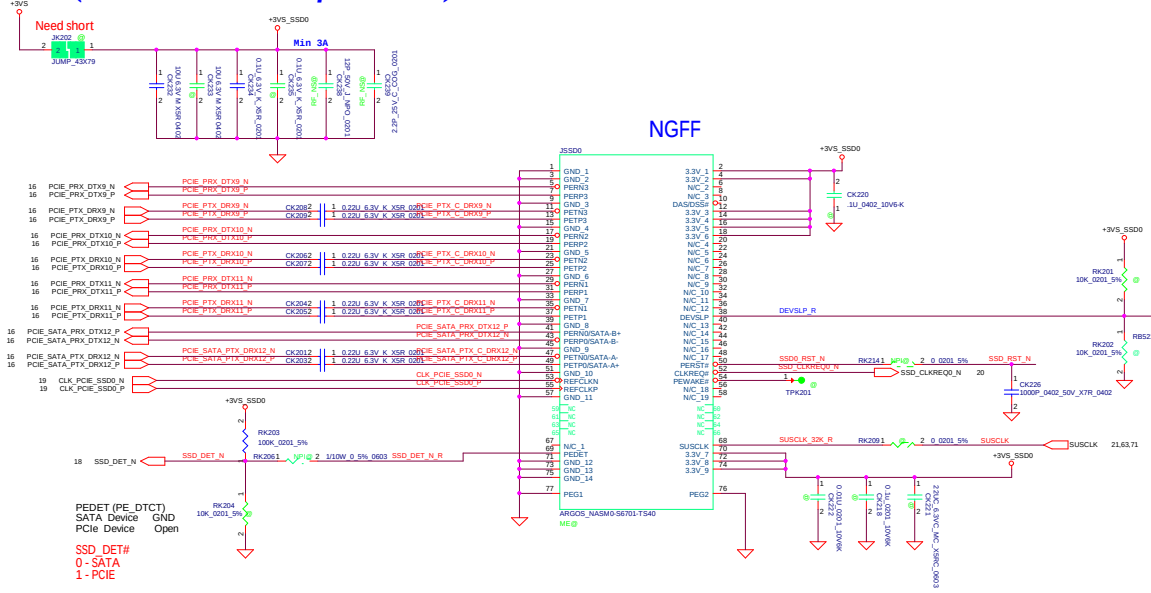
Security Classification	LCFC Highly Confidential Information		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	TPM		
Size C	Document Number HY520		Rev 0.1
Date: Friday, May 07, 2021	Sheet 62 of 110		

M.2 SSD(PCIE GEN4 from CPU)

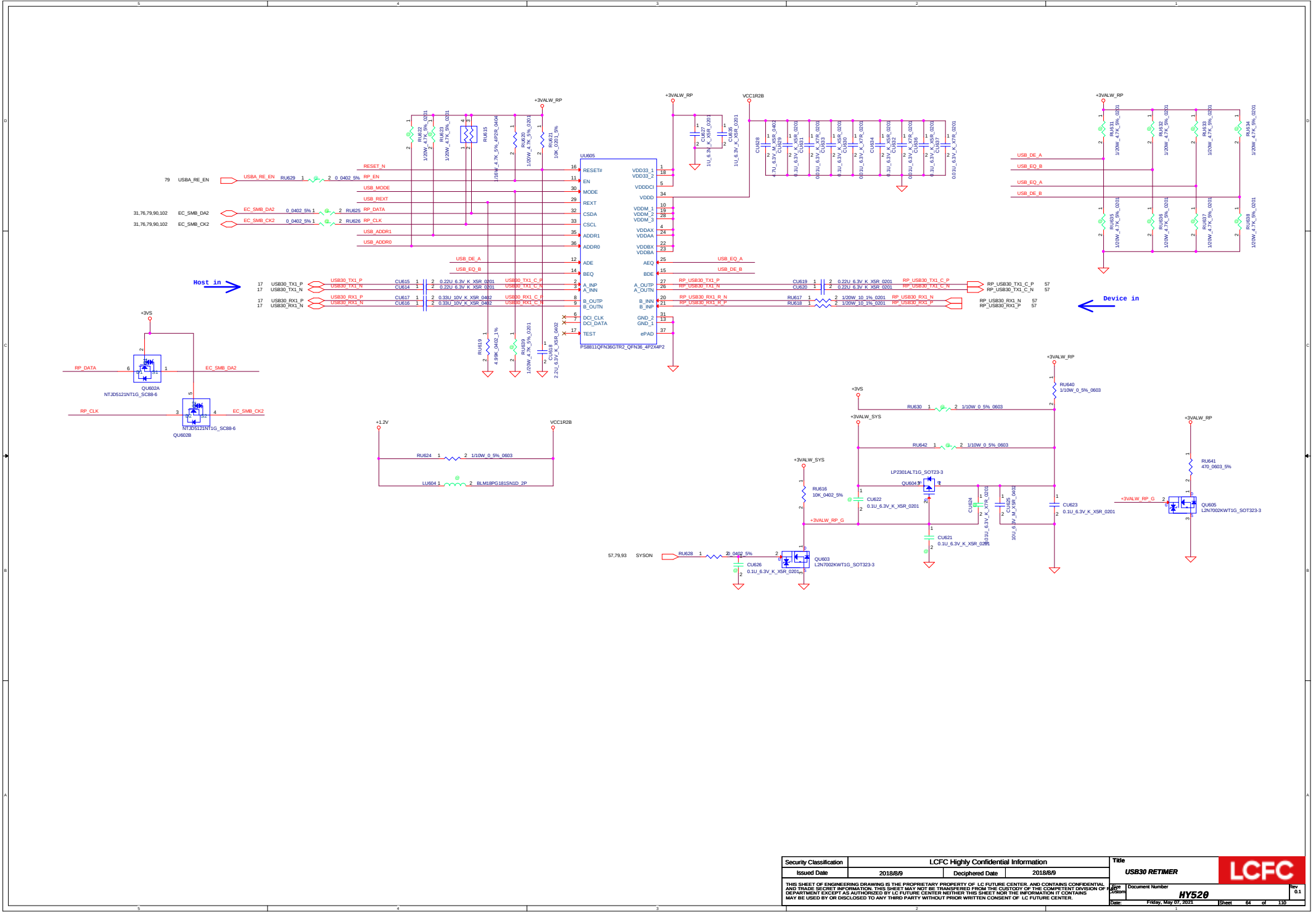


M.2 SSD(SATA/PCIE Gen3 from PCH)



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	SSD		
Size	Document Number		Rev
Custom	HY520		0.1
Date:	Friday, May 07, 2021	Sheet	63 of 110



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/8/9	Deciphered Date	2018/8/9

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Title: *USB30 RETIMER*

LCFC

Size: Custom | Document Number: *HY520* | Rev: 0.1

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Security Classification	LCFC Highly Confidential Information		
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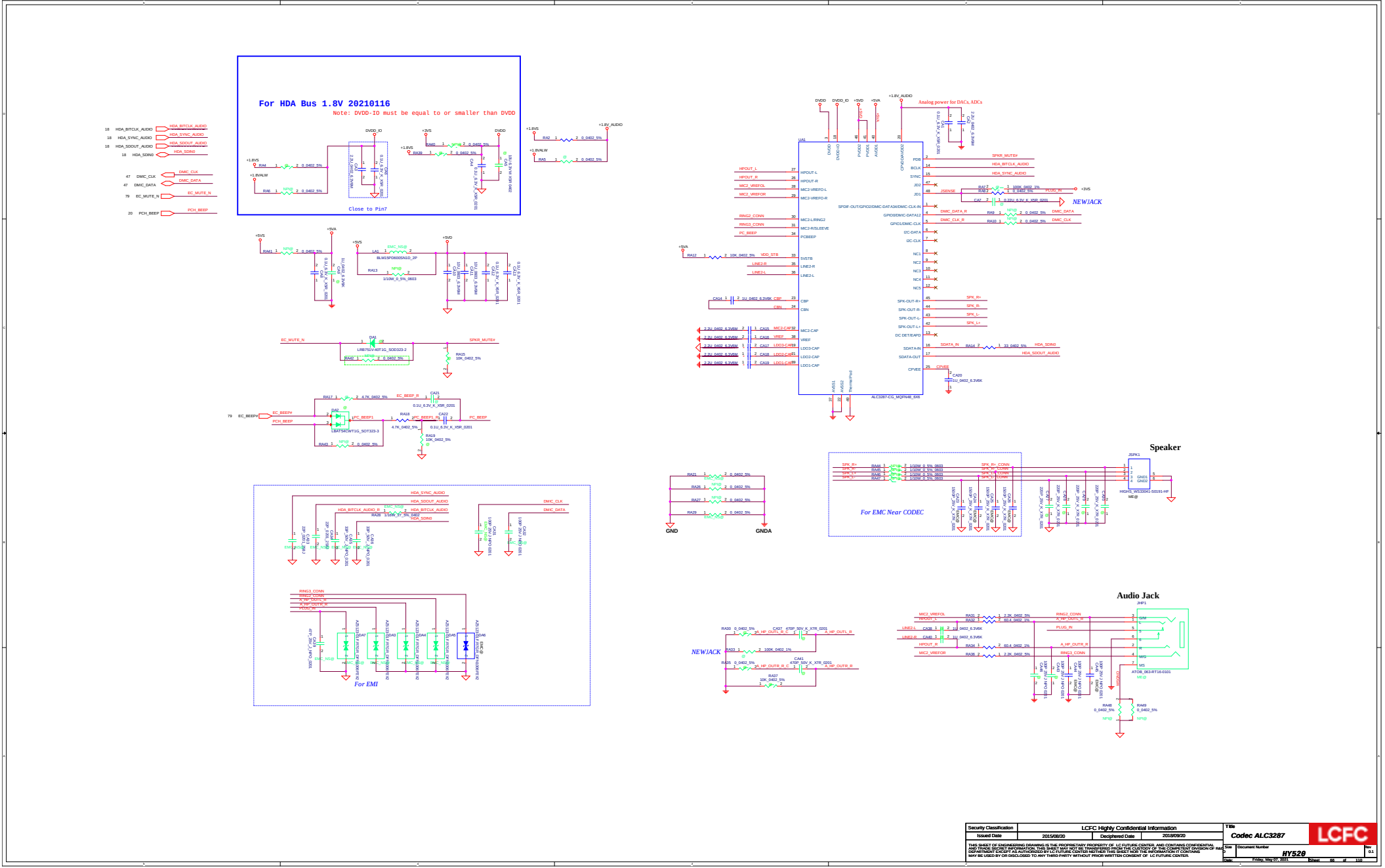
Title	LCFC
Size	Document Number / Rev
Date:	Sheet of


For HDA Bus 1.8V 20210116
Note: DVDD-IO must be equal to or smaller than DVDD
Close to Pin7
Analog power for DACs, ADCs
Speaker
Audio Jack
NEWJACK
For EMC Near CODEC
For EMI
ALC3287-CG_MQFN48_6X6
Codec ALC3287
HY520
LCFC Highly Confidential Information
Issued Date 2015/08/20
Deciphered Date 2018/09/20
Friday, May 07, 2021

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

Title

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LCFC

Size	Document Number	Rev
C	***HY520***	0.1

Date: Friday, May 07, 2021 Sheet 67 of 110

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

Title

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LCFC

Size	Document Number	Rev
C	***HY520***	0.1

Date: Friday, May 07, 2021 Sheet 68 of 110

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

Title

Blank

LCFC

Size	Document Number	Rev
C	***HY520***	0.1

Date: Friday, May 07, 2021 Sheet 69 of 110

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: ***Blank***

LCFC

Size	Document Number	Rev
C	***HY520***	0.1

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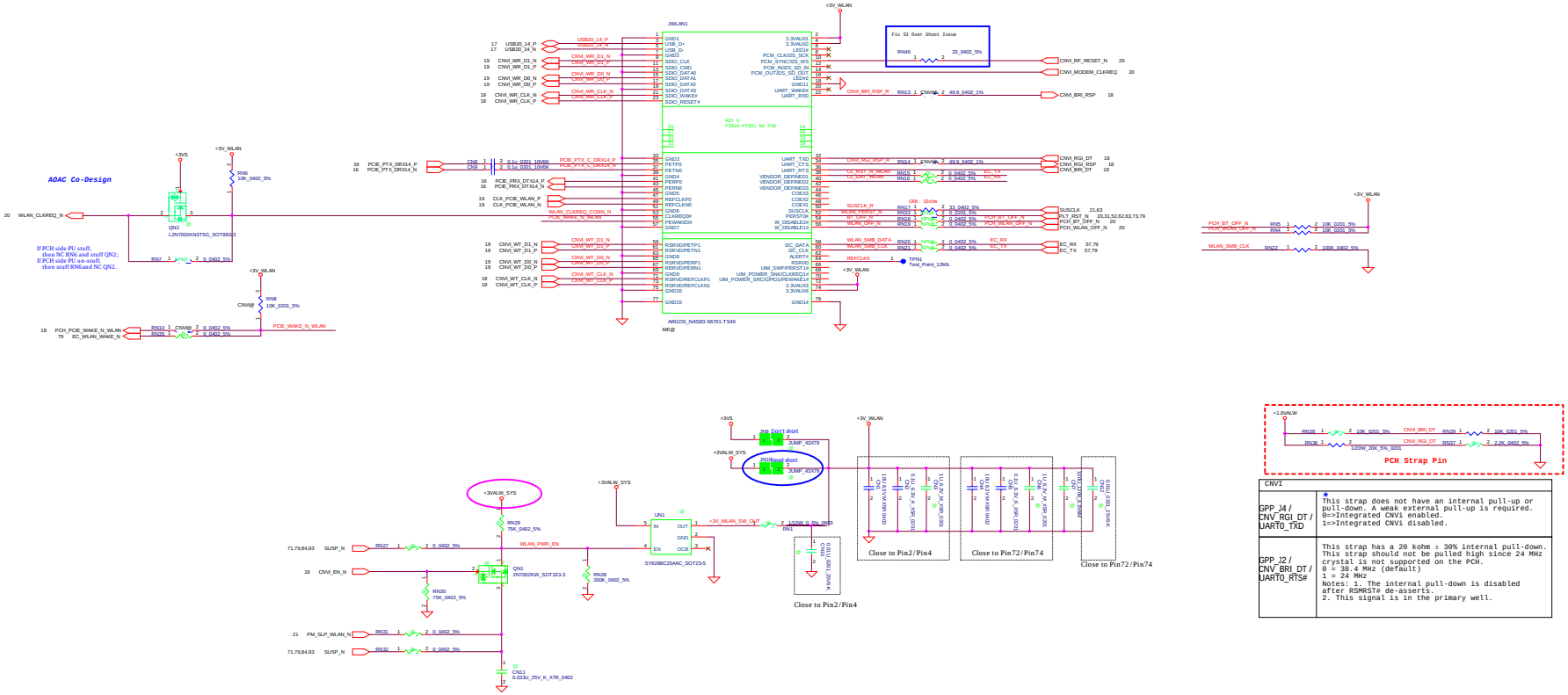
Mini-Express Card(WLAN/WiMAX)



CNVI	
GPP_J4 / CNV_RGI_DT / UART0_TXD	★ This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled.
GPP_J2 / CNV_BRI_DT / UART0_RTS#	This strap has a 20 kohm ± 30% internal pull-down. This strap should not be pulled high since 24 MHz crystal is not supported on the PCH. 0 = 38.4 MHz (default) 1 = 24 MHz Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	CNVi WLAN	LCFC
Size: D	Document Number: HY520	Rev: 0.1
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

Title

Blank

LCFC

Size	Document Number	Rev
B	***HY520***	0.1

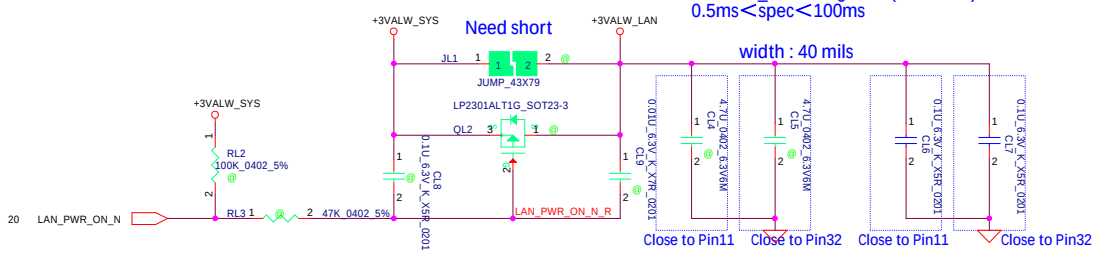
Date: Friday, May 07, 2021 Sheet 72 of 110

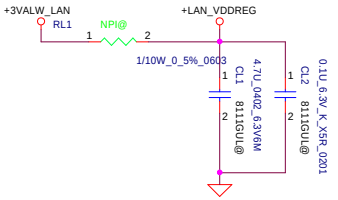
+3VALW_SYS TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

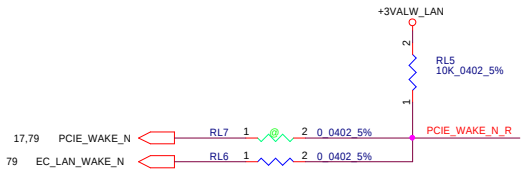
Need short

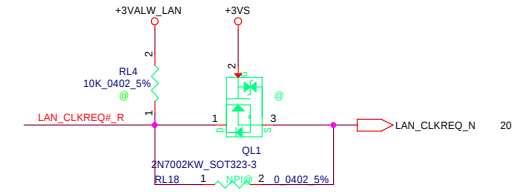
width : 40 mils

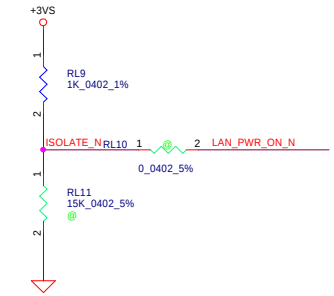


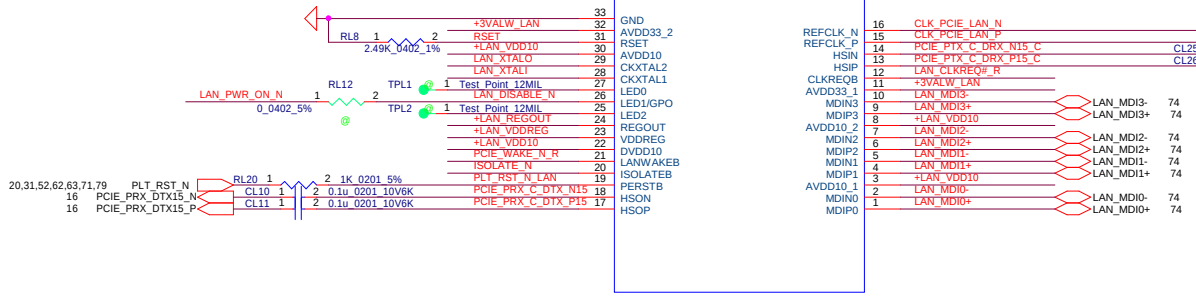


manual change the PN to RTL8111GUL-CG

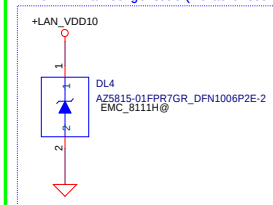


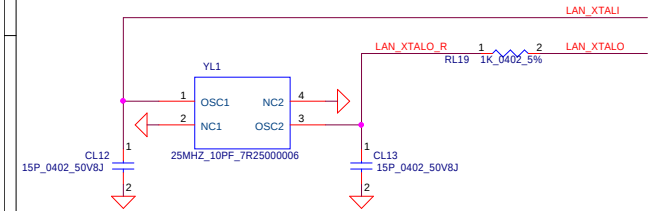


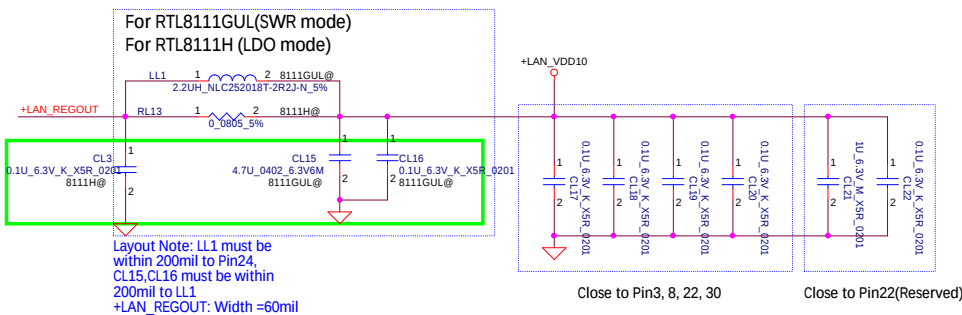




2018/01/24: add AZ5815-01F.R7GR for RTL8111H Lan Surge issue (Default reserve)







Security Classification	LCFC Highly Confidential Information		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title	LAN_RTL8111H_CG		
Size	Document Number		Rev
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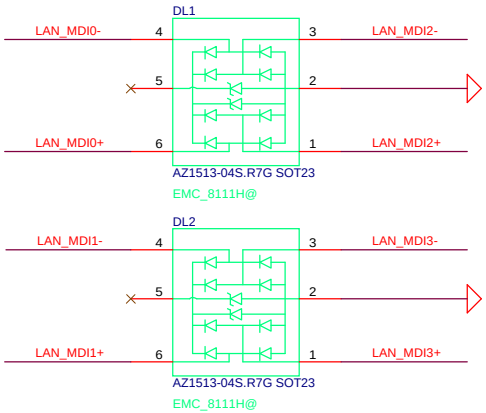
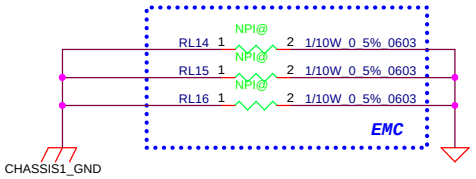
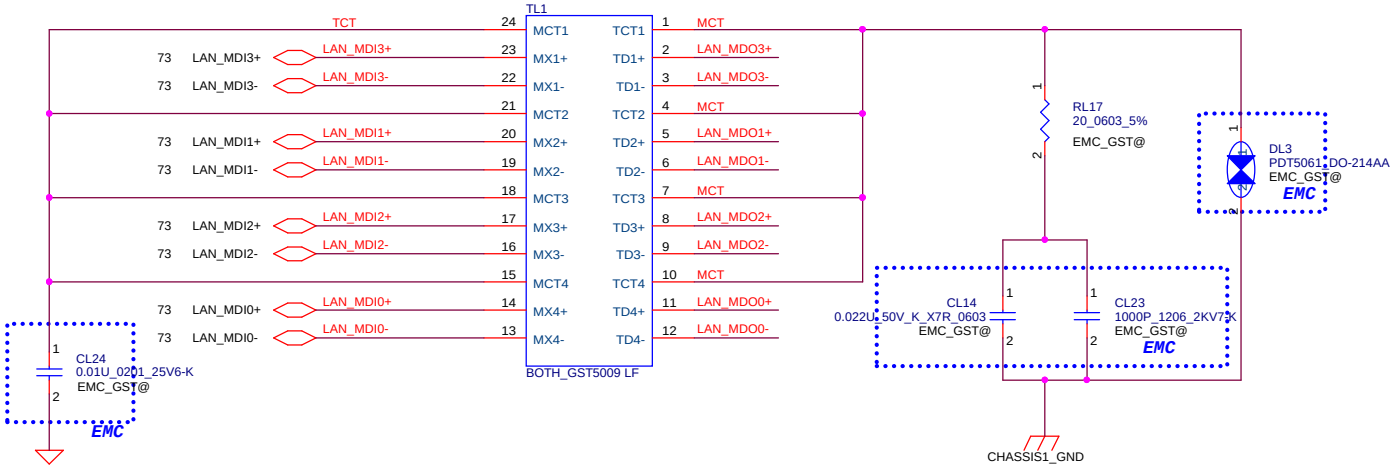
Default DL1/DL2 use
S DIO(BR) AZ1513-04S.R7G SOT23-6L
for 8111H, L340 project

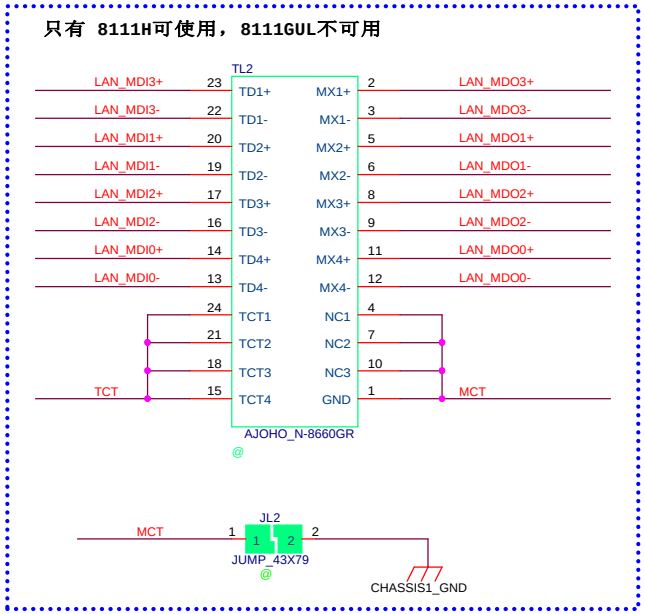


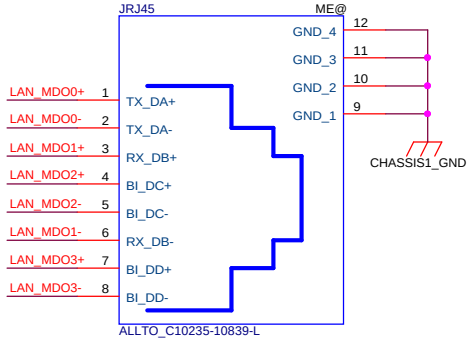
Place Close to TL2 *EMC*

Place Close to TL1 *EMC*









8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LCFC Highly Confidential Information		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: *LAN_Transformer*

LCFC

Size	Document Number	Rev
B	*HY520*	0.1

Date: Friday, May 07, 2021 Sheet 74 of 110

Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: ***Blank***

LCFC

Size	Document Number	Rev
C	***HY520***	0.1

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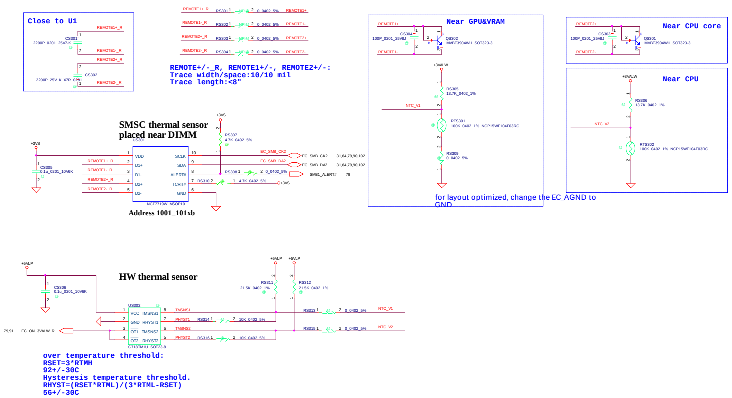
GEN1



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Thermal sensor*

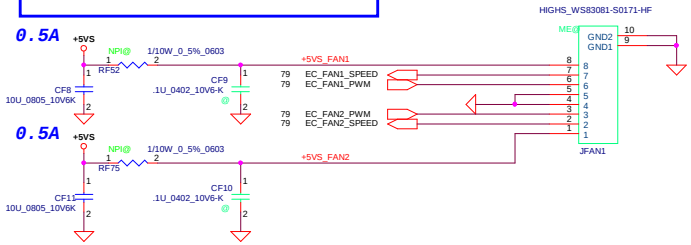
Size: E | Document Number: HY520 | Rev: 0.1

Date: Friday, May 07, 2021

FAN Conn GEN1

need check ME SDV CONN list

Change to SP011411114 ref ME conn list,20181017SF update



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **FAN CONN**

LCFC

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Security Classification	LCFC Highly Confidential Information		
Issued Date		Deciphered Date	

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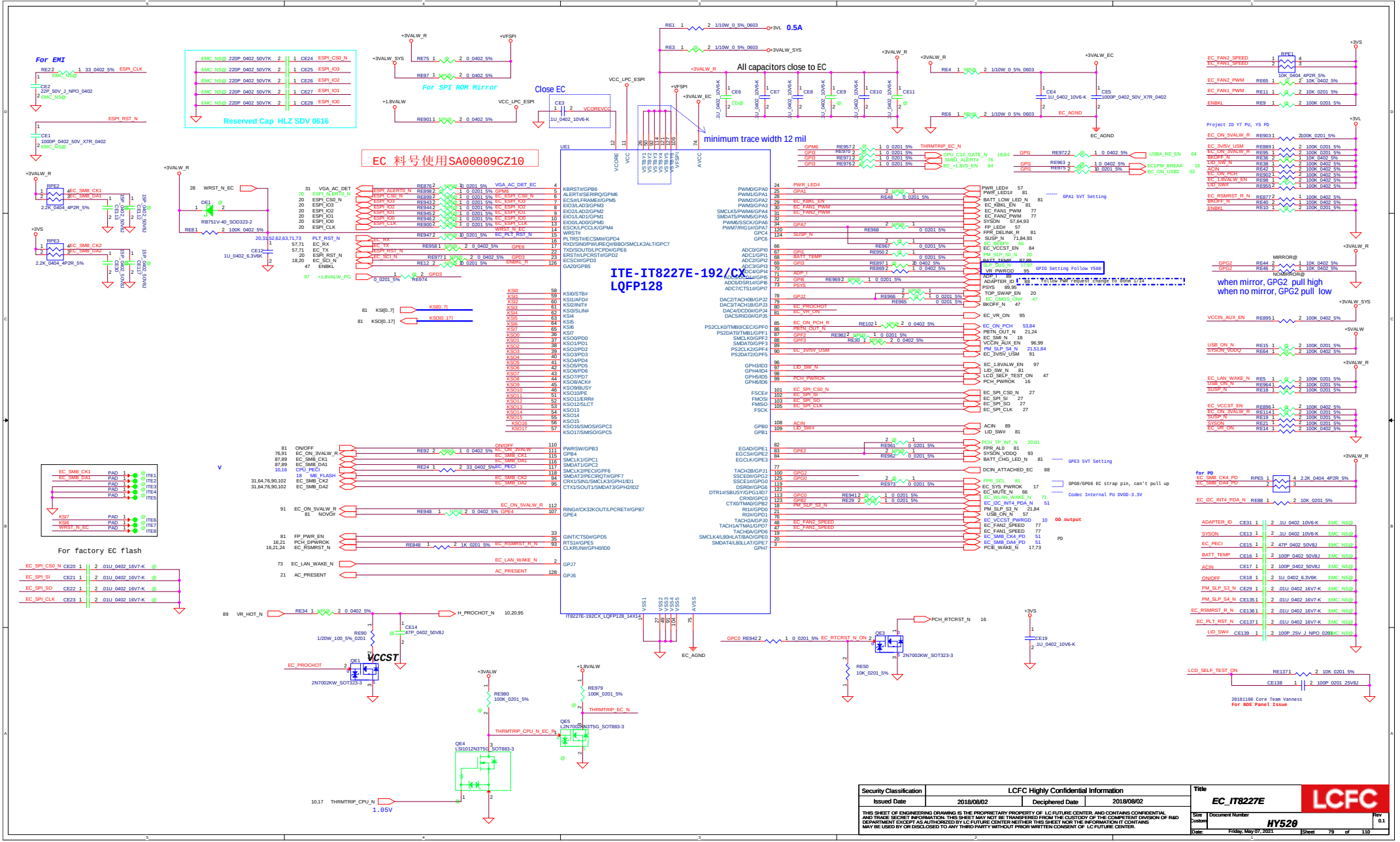
Title		LCFC
Size	Document Number	Rev
Date:	Sheet of	


For EMI
Reserved Cap HLZ SDV 0616
For SPI ROM Mirror
Close EC
All capacitors close to EC
minimum trace width 12 mil
EC 料号使用SA00009CZ10
ITE-IT8227E-192/CX
LQFP128
For factory EC flash
1.05V
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Project ID Y7 PU, Y5 PD
GPA1 SVT Setting
GPE3 SVT Setting
GPG8/GPG6 EC strap pin, can't pull up
Codec Internal PU DVDD-3.3V
OD output
for PD
For BOE Panel Issue
Security Classification
LCFC Highly Confidential Information
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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LCFC
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Custom
Document Number
HY520
Rev
0.1
Date:
Friday, May 07, 2021
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/07/02	Deciphered Date	2020/05/16

Title: *Blank*

LCFC

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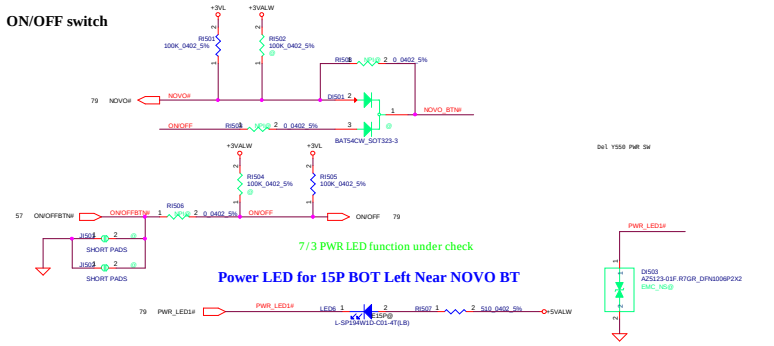
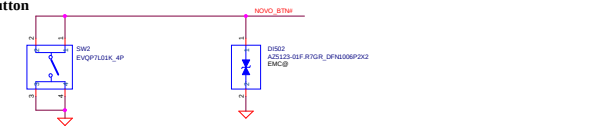
ON/OFF switch

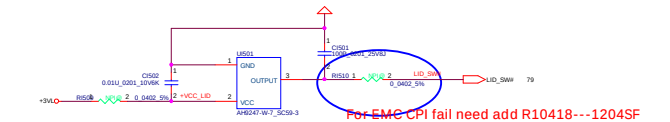


Novo button

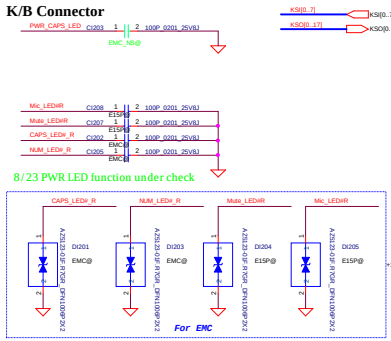


8/31 Update the P/N SN100008W00 wei

LID switch

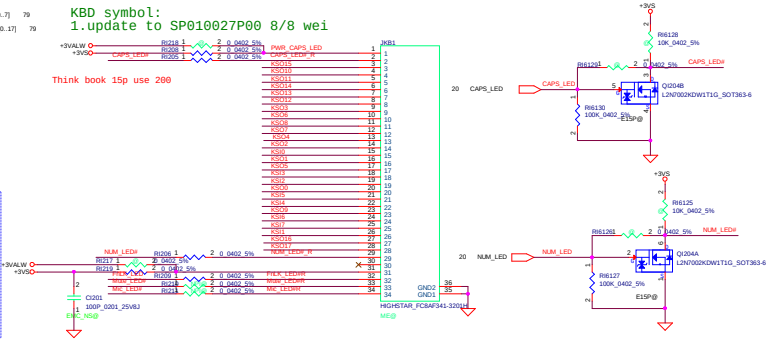


K/B Connector



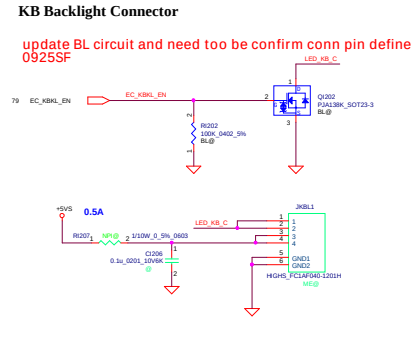
KBD symbol:
1.update to SP010027P00 8/8 wei

Think book 15p use 200

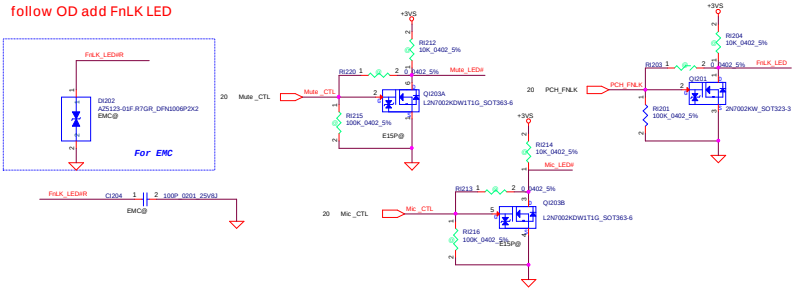


KB Backlight Connector

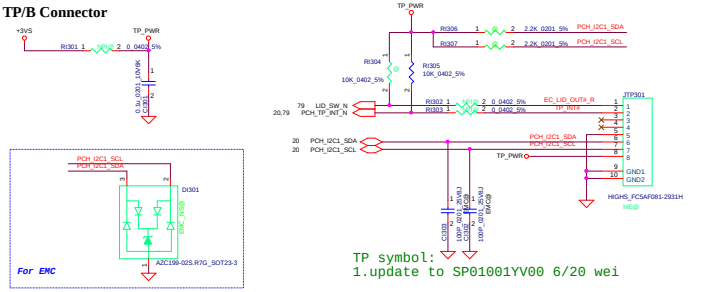
update BL circuit and need too be confirm conn pin define 0925SF



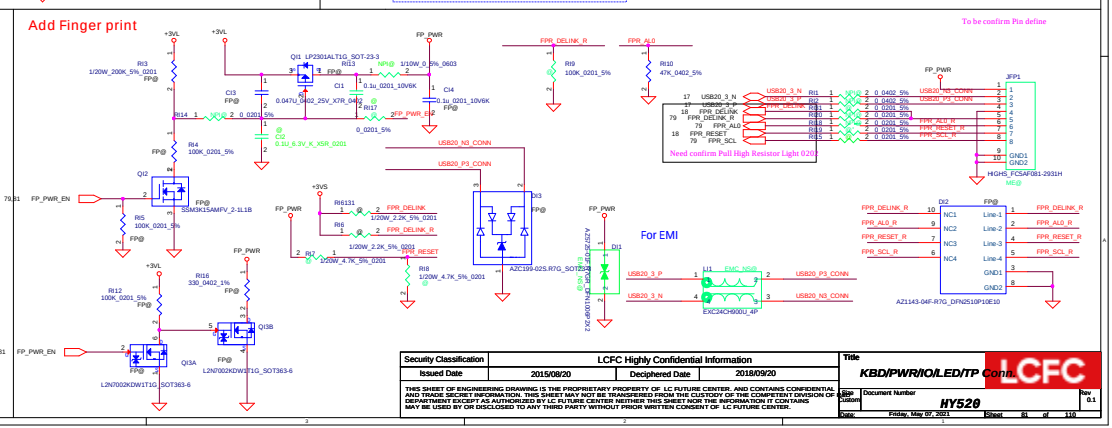
follow OD add FnLK LED

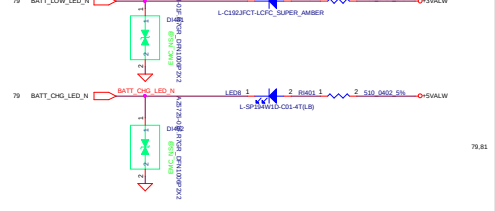


TP/B Connector



Add Finger print





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Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title: KBD/PWR/IO/LED/TP Conn

LCFC

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IT8258 delete for P

IT8176

Security Classification	LCFC Highly Confidential Information			Title: Blank
Issued Date	2019/07/02	Deciphered Date	2020/02/24	Size: E — Document Number: HY520 — Rev: 0.1
				Date: Friday, May 07, 2021 — Sheet 82 of 110

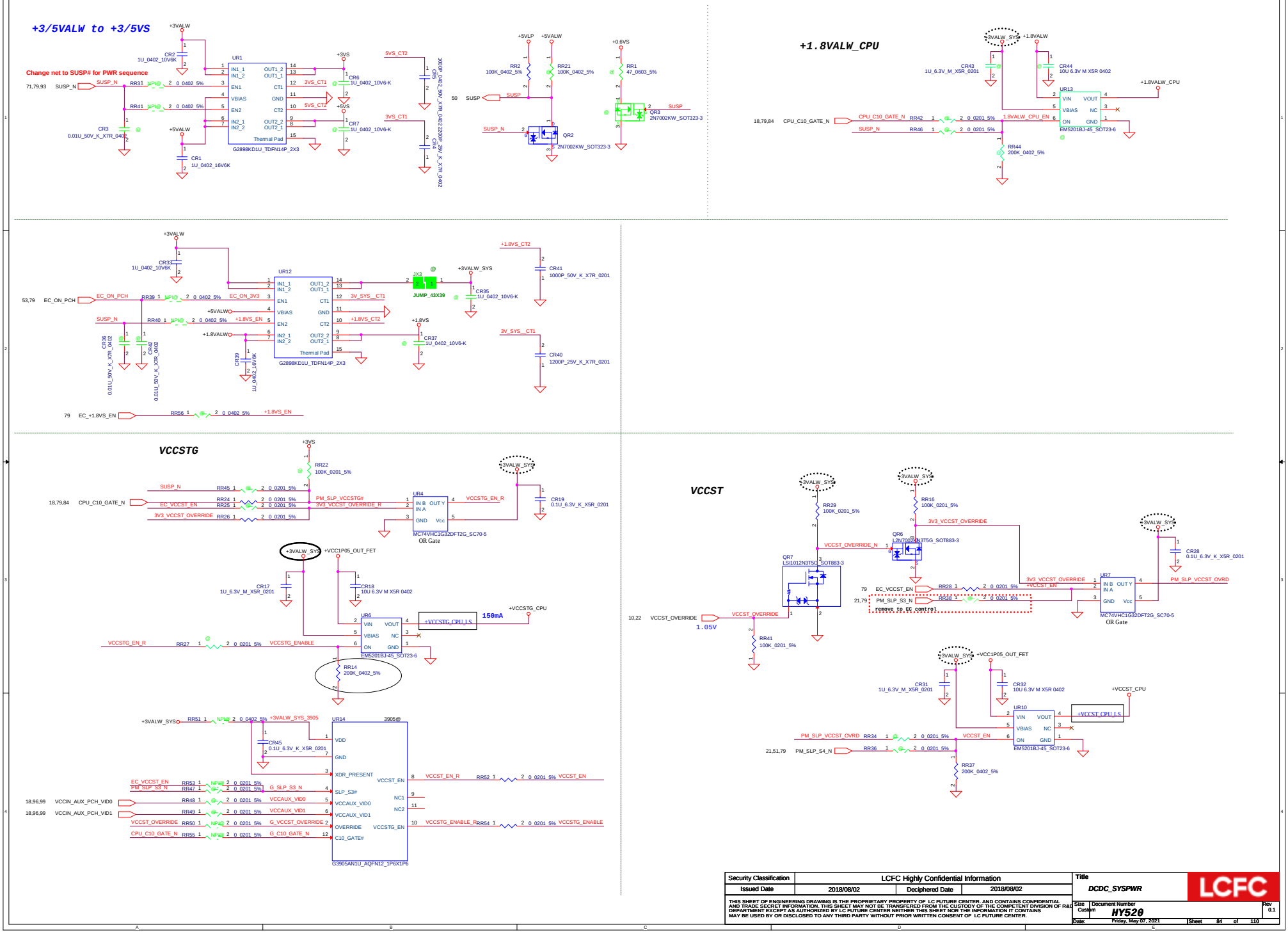
Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Blank*

LCFC

Size	Document Number	Rev
D	*HY520*	0.1

Date: Friday, May 07, 2021 Sheet 83 of 110


+3/5VALW to +3/5VS
Change net to SUSP# for PWR sequence
+1.8VALW_CPU
VCCSTG
VCCST
Security Classification
LCFC Highly Confidential Information
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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Title
DCDC_SYSPWR
LCFC
Size
Custom
Document Number
HY520
Rev
0.1
Date:
Friday, May 07, 2021
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

Title

Blank

LCFC

Size	Document Number	Rev
B	***HY520***	0.1

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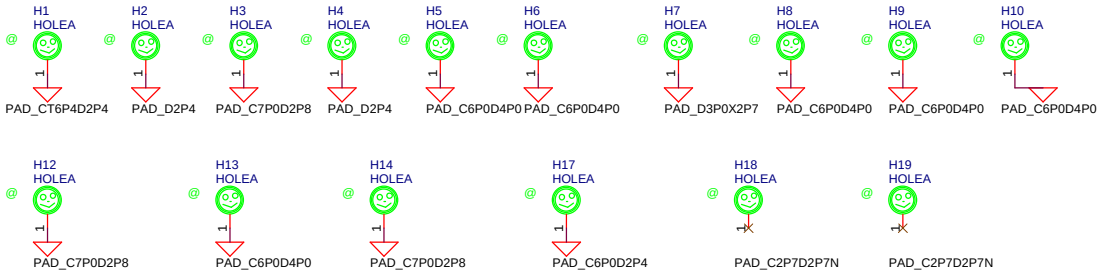
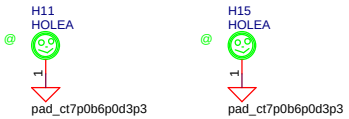
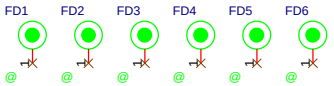
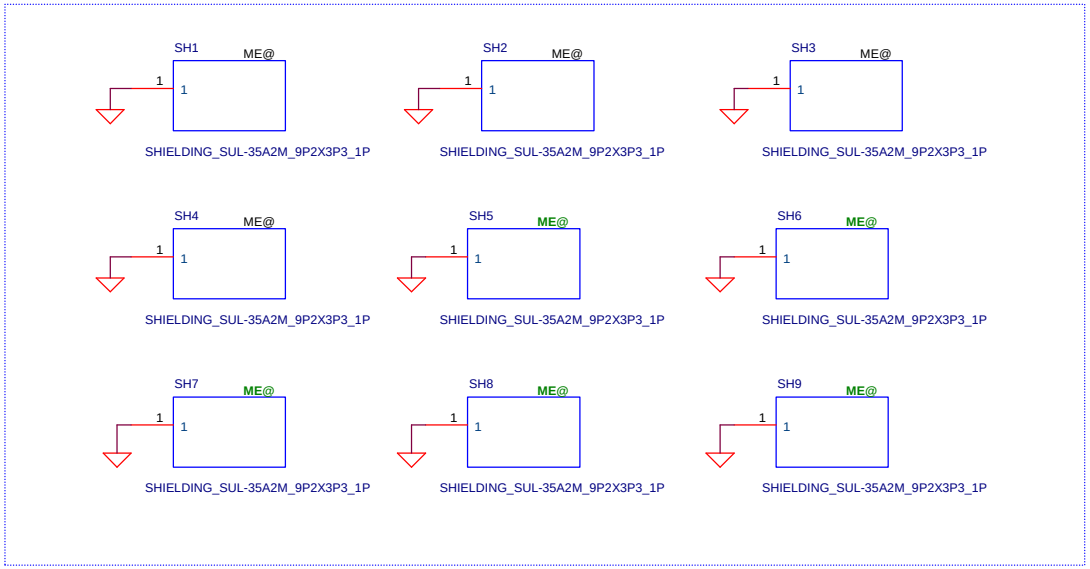




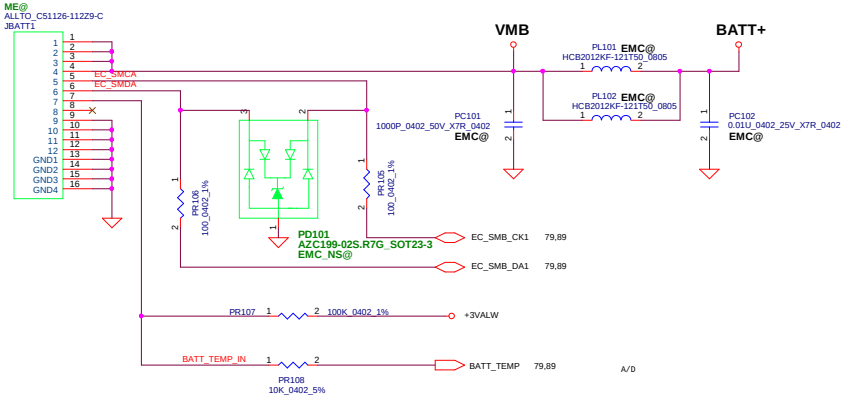


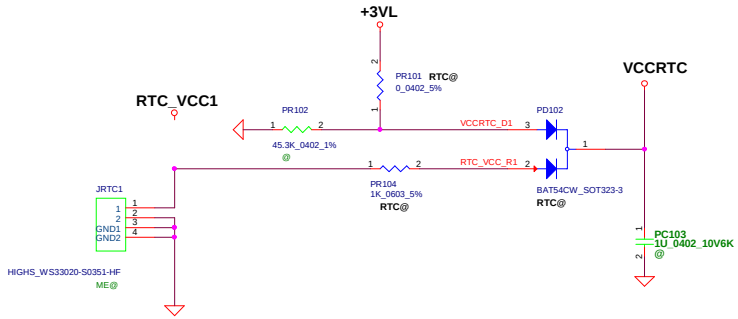


DDR4 Shielding

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Hole/Shielding		
Size B	Document Number HY520		Rev 0.1
Date: Friday, May 07, 2021	Sheet 86 of 110		





Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR_DCIN/RTC

LCFC

Size	Document Number	Rev
C	HY520	0.1

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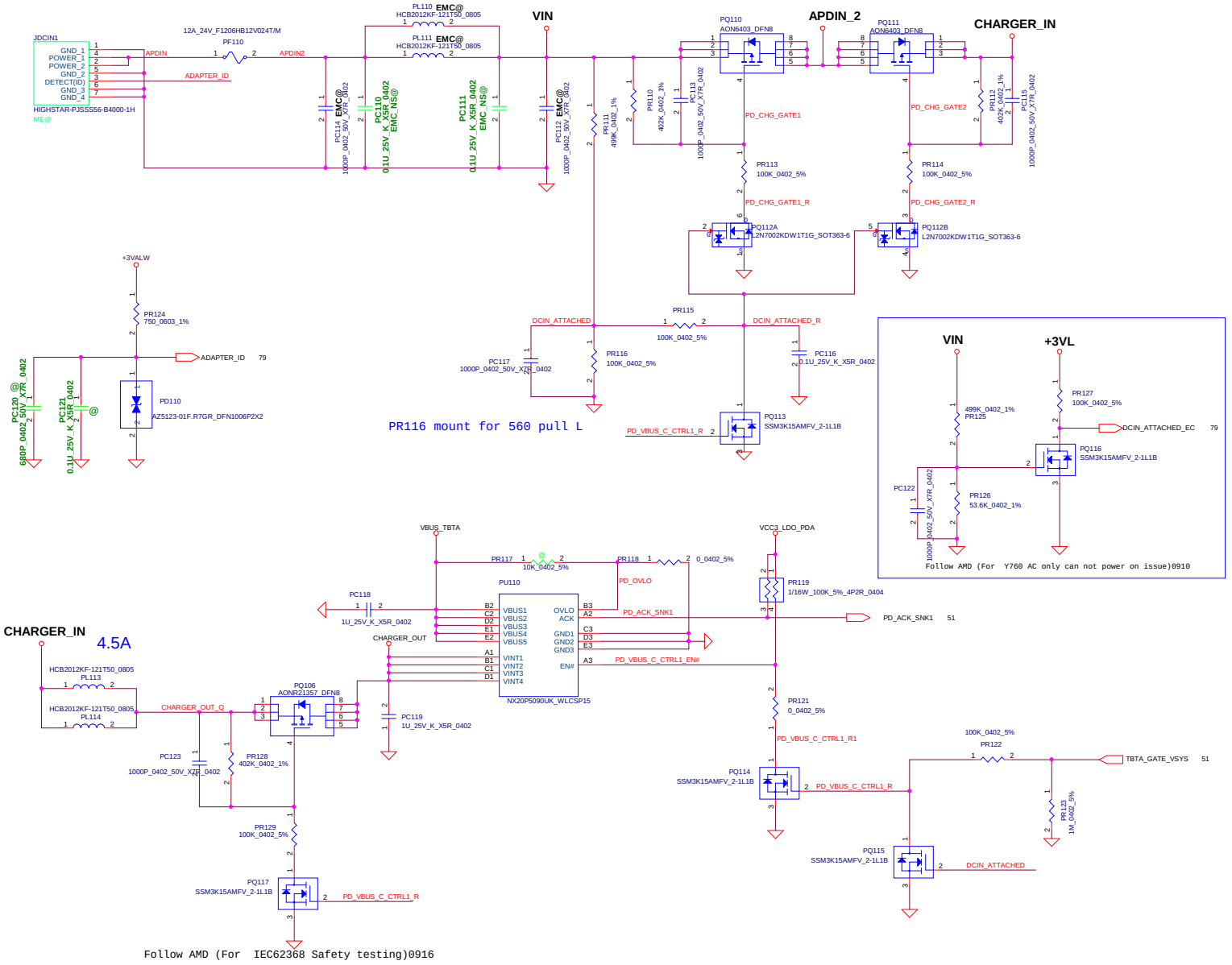
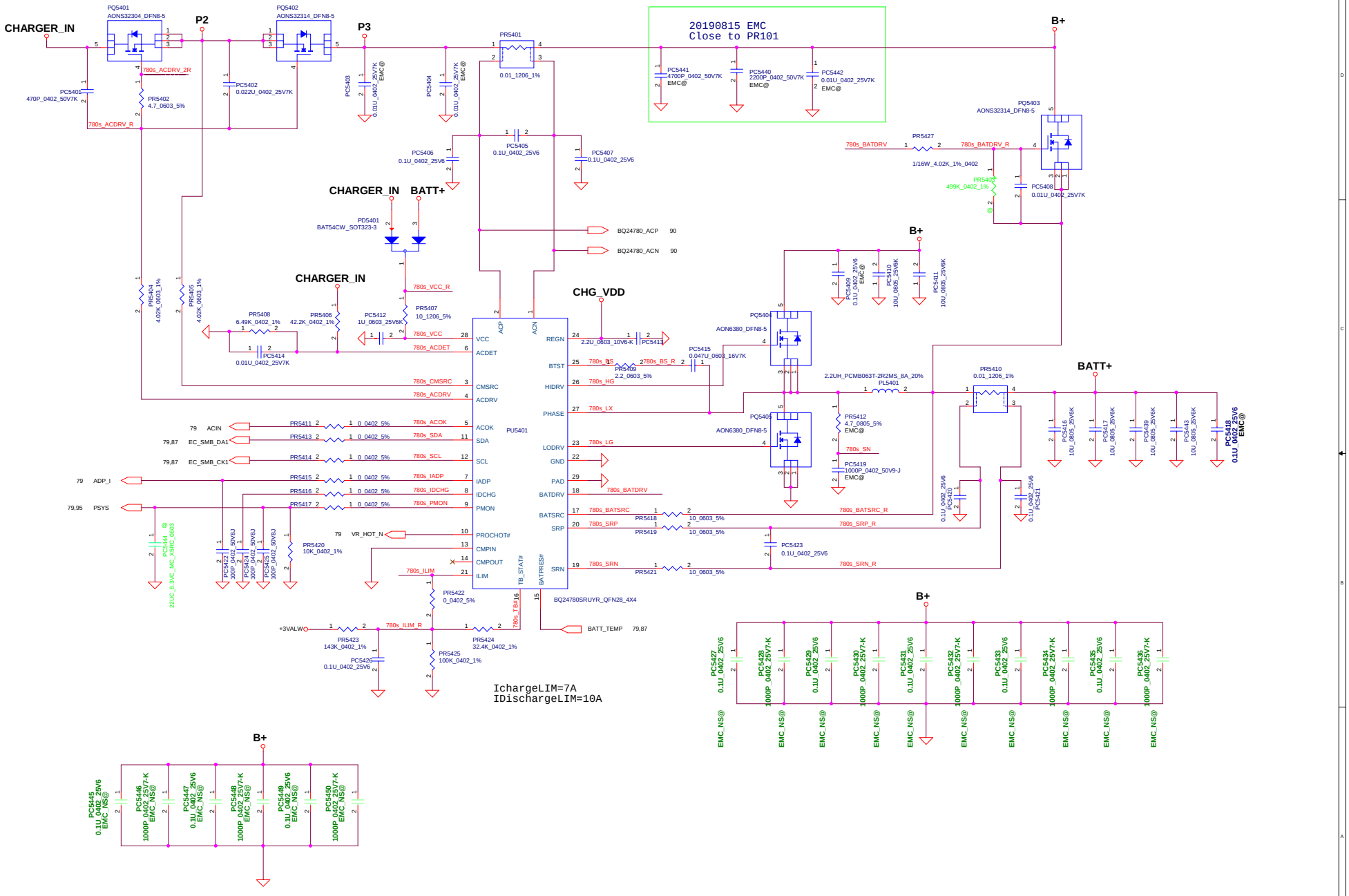


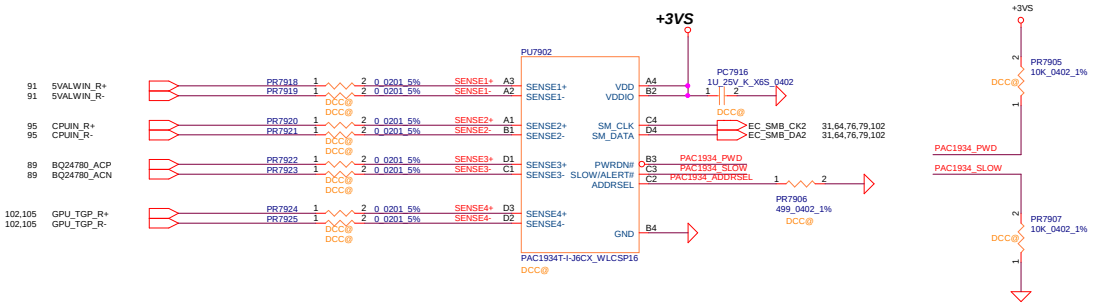
Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR_ACIN		
Size C	Document Number	HY520	Rev 0.1
Date:	Friday, May 07, 2021	Sheet 88 of 110	



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Charger-BQ24780SRUYR		
Size	Document Number	HY520	Rev 0.1
Custom			
Date:	Friday, May 07, 2021	Sheet 89 of 110	



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *PWR_Memory PWR Decoupling*

LCFC

Size	Document Number	Rev
Custom	*HY520*	0.1

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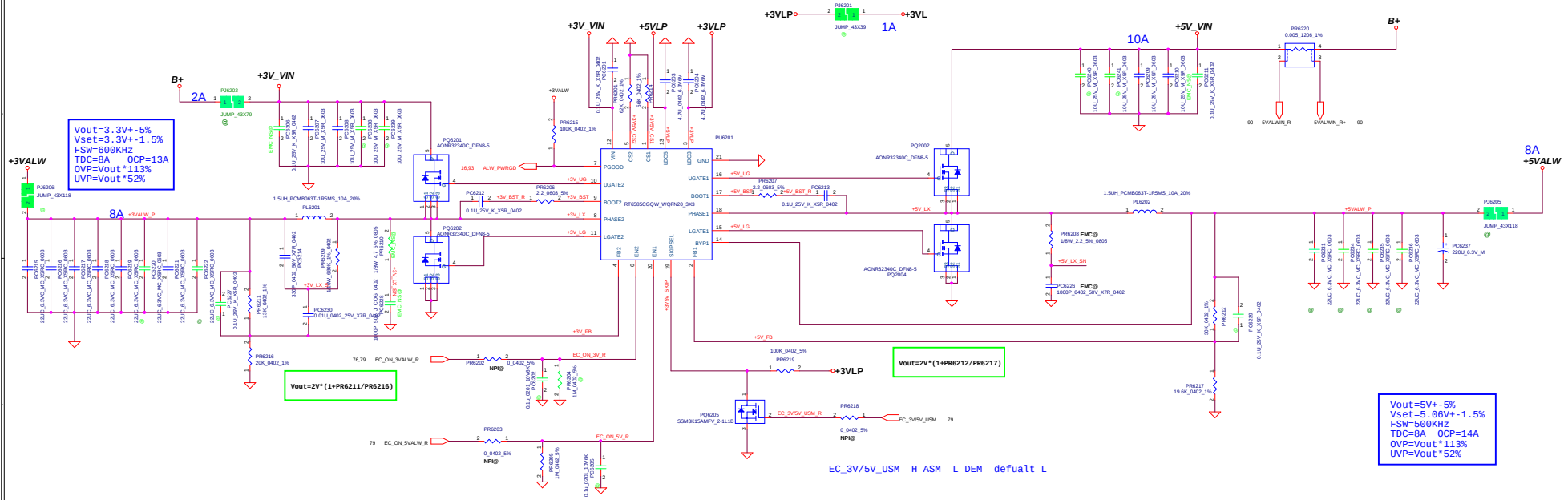

	RT6585C	RT6575D&TPS51275B
Mode	DEM/USM	USM/CCM
3V FSW	600K	355K
5V FSW	500K	300K
CSx	Rlimit=(Ilimit*Rdson)*8/50uA	Rlimit=(Ilimit*Rdson)*8/10uA

RT6585B&TPS51285B BOM to BOM
RT6575D&TPS51275B BOM to BOM
RT6585B&RT6575D PIN to PIN, with different work mode, FSW, and CS setting

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	PWR_3VALW/5VALW		LCFC
Size	Document Number		Rev
Custom	HY520		0.1
Date	Friday, May 07, 2021	Sheet 91 of 110	

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *PWR_NA*

LCFC

Size	Document Number	Rev
C	*HY520*	0.1

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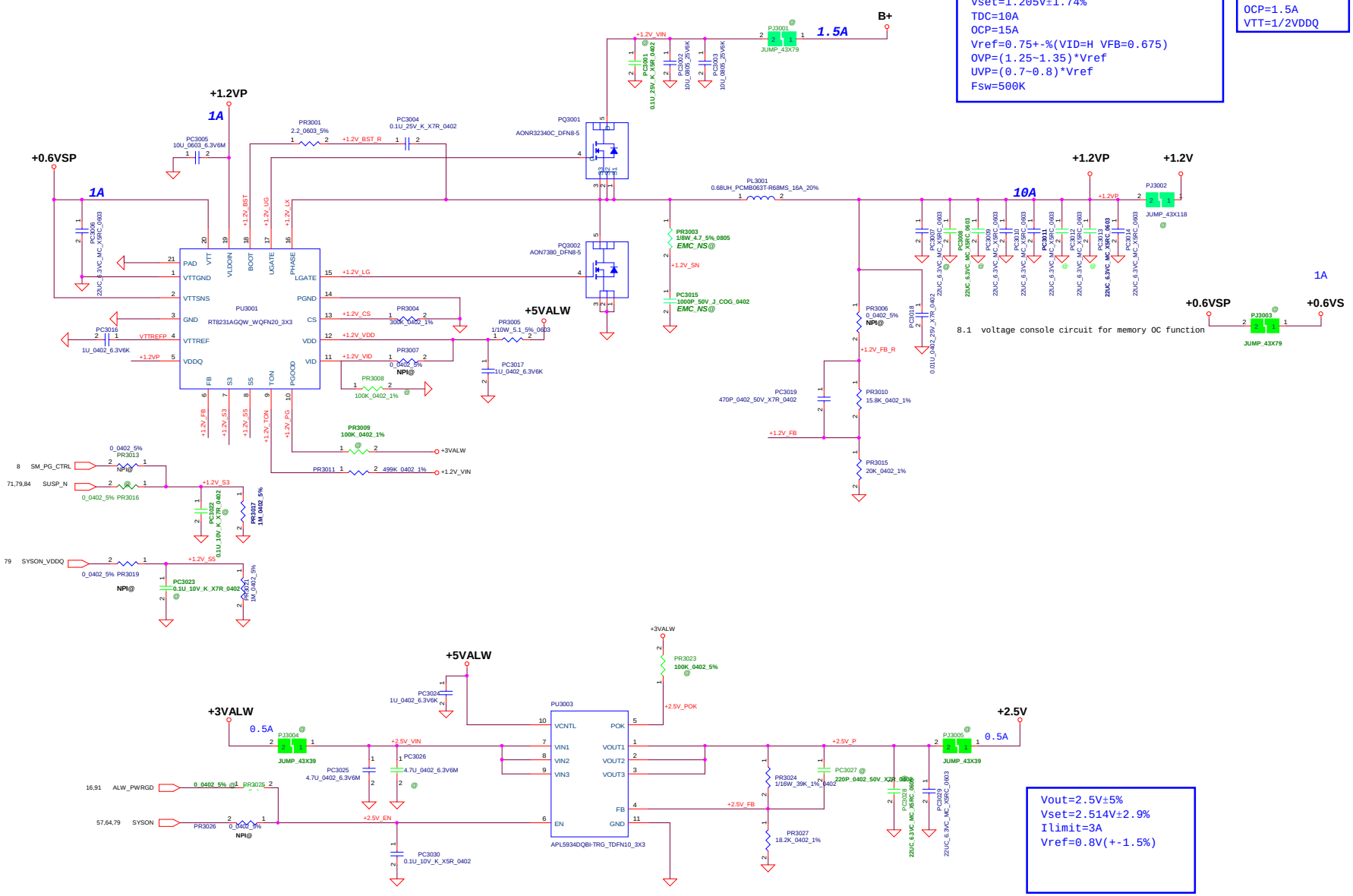

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

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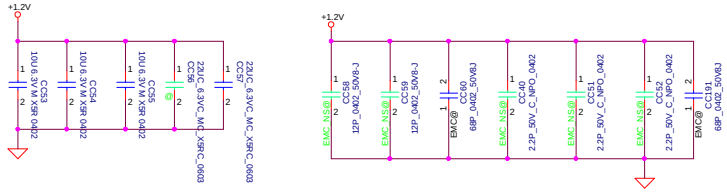
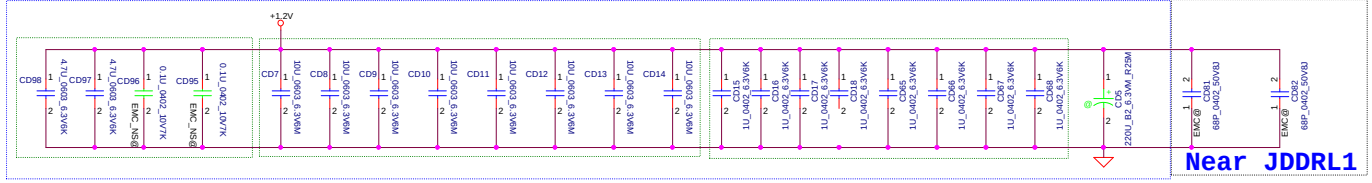
CPU

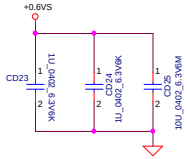


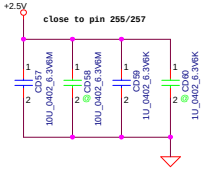
JDDRL1

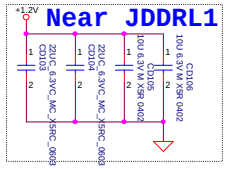
Layout Note:
Place near DIMM



Layout Note:
Place near DIMM

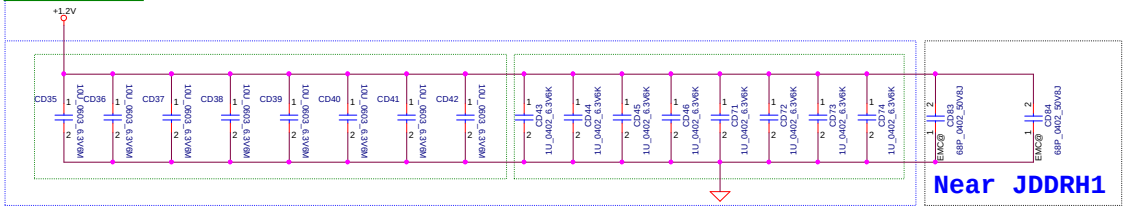




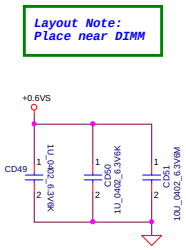


JDDRH1

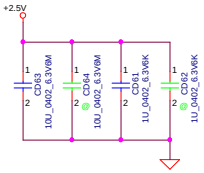
Layout Note:
Place near DIMM

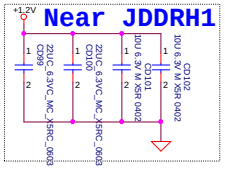


Layout Note:
Place near DIMM



close to pin 257,259





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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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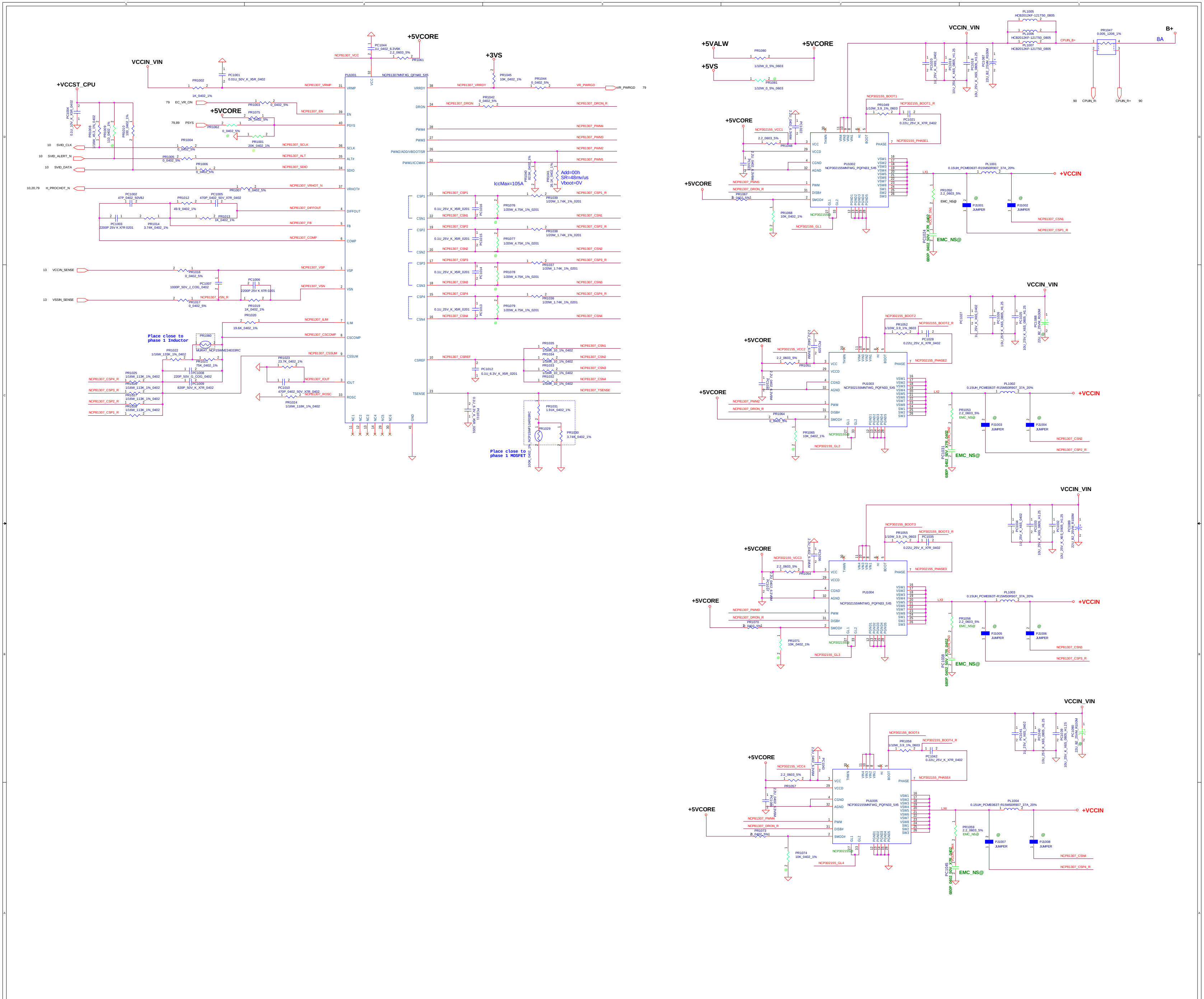

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR_CPU PWR_Onsemi

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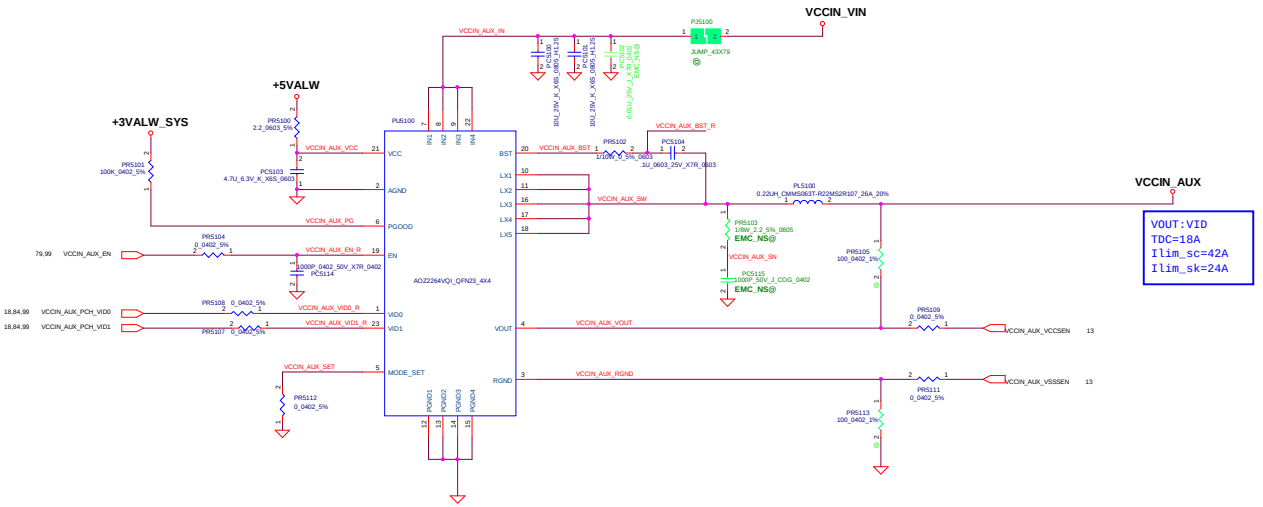
VOUT Setting	VID0	VID1
1.8V	H	H
1.65V	L	H
1.1V	H	L
0V	L	L



Security Classification	LCFC Highly Confidential Information		
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PWR_CPU PWR1			LCFC
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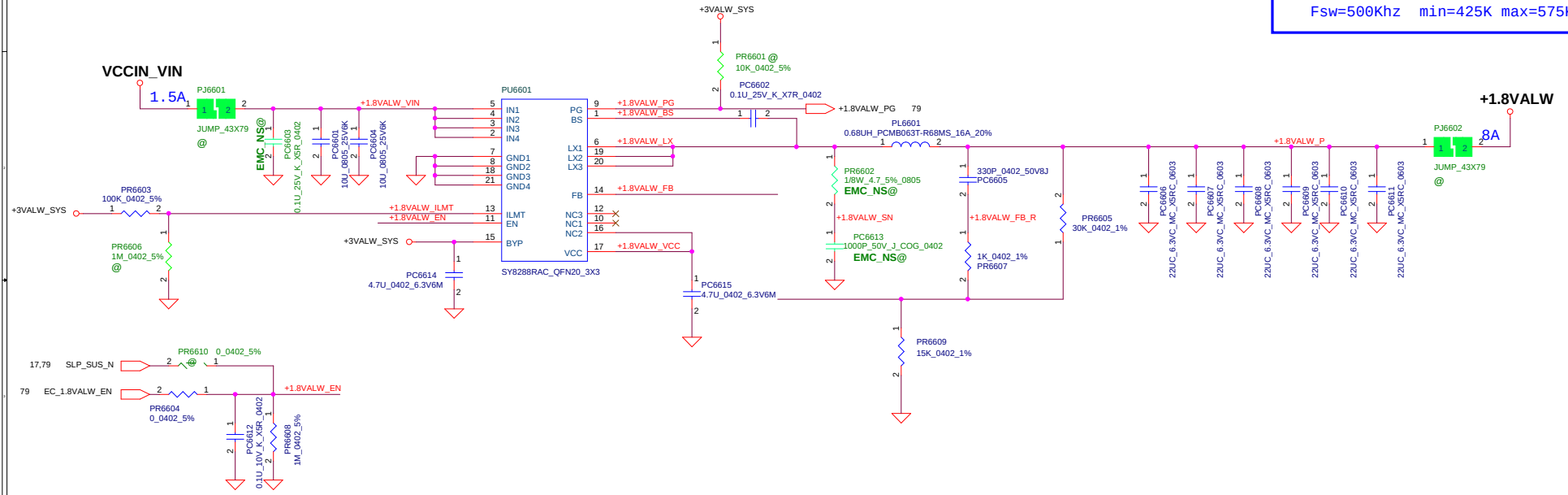
Vout=1.8V±5%
Vset=1.8V±2.3%
Vref=0.6V(+-1%)
TDC=8A
OCP=16A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR_CPU PWR2

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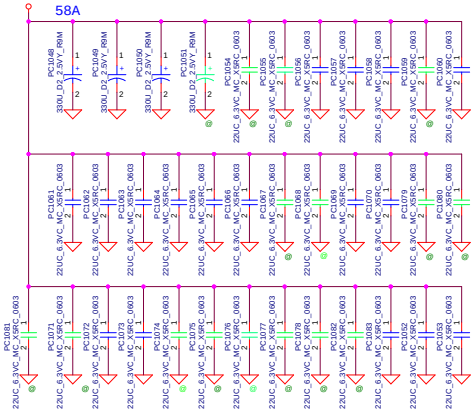
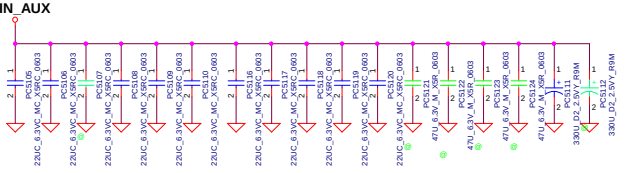
Y540:330u*2PCS+22u*19PCS
Y550:follow Y540 Vendor
PDG:470uF*4pcs+47uF*33pcs
Actual:330u*3PCS+22u*19PCS

+VCCIN

58A

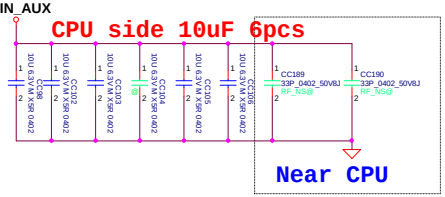


VCCIN_AUX



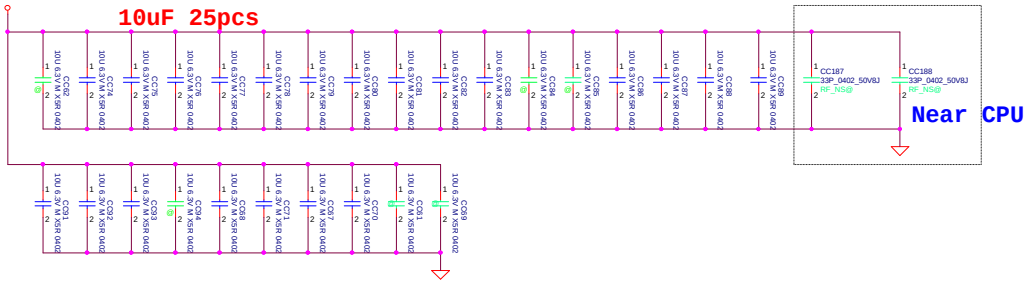
VCCIN_AUX

CPU side 10uF 6pcs

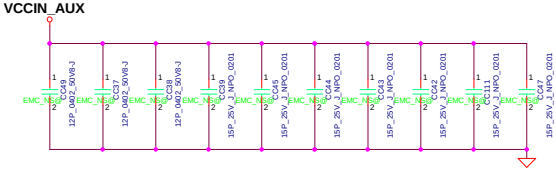


+VCCIN

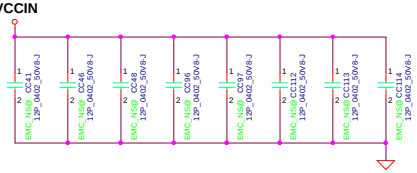
10uF 25pcs



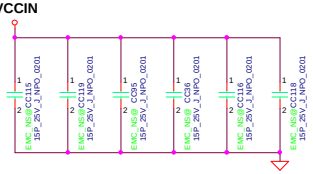
VCCIN_AUX



+VCCIN



+VCCIN



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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: PWR_CPU PWR Decoupling

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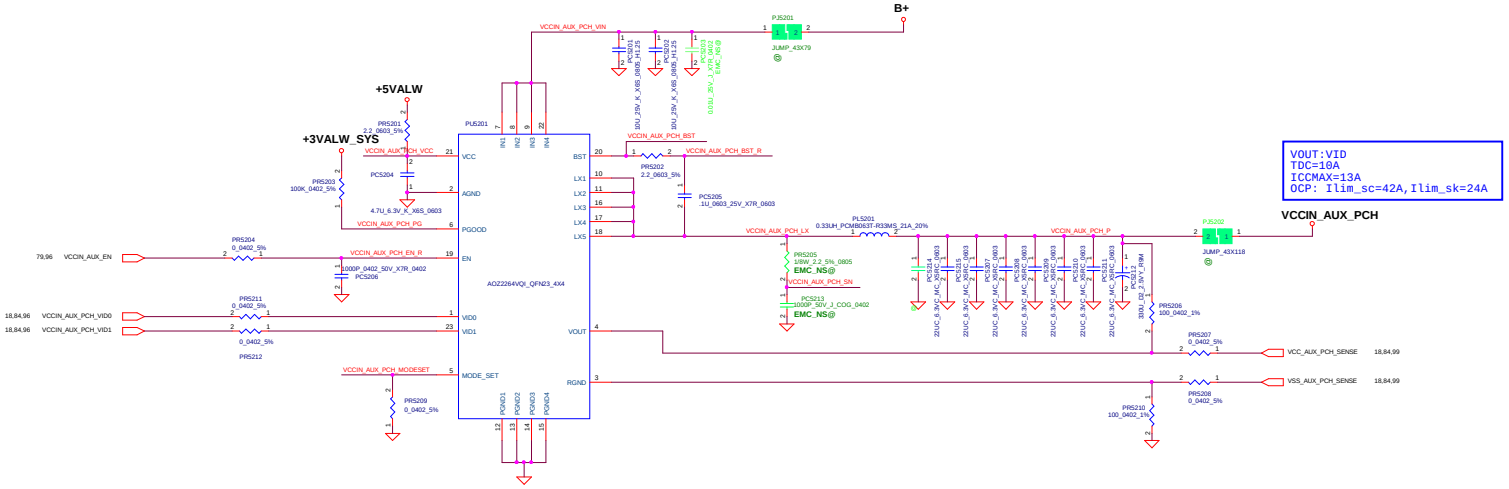

VOUT Setting	VID0	VID1
1.8V	H	H
1.65V	L	H
1.1V	H	L
0V	L	L

Title			
PWR-FBVDDQ-AOZ2767QI			
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Title

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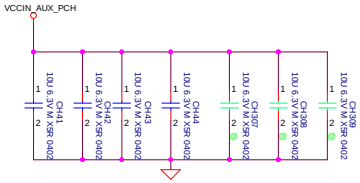

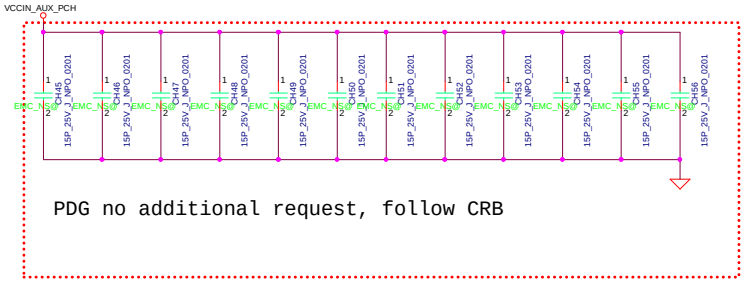

PDG no additional request, follow CRB

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *PWR_PCH PWR Decoupling*

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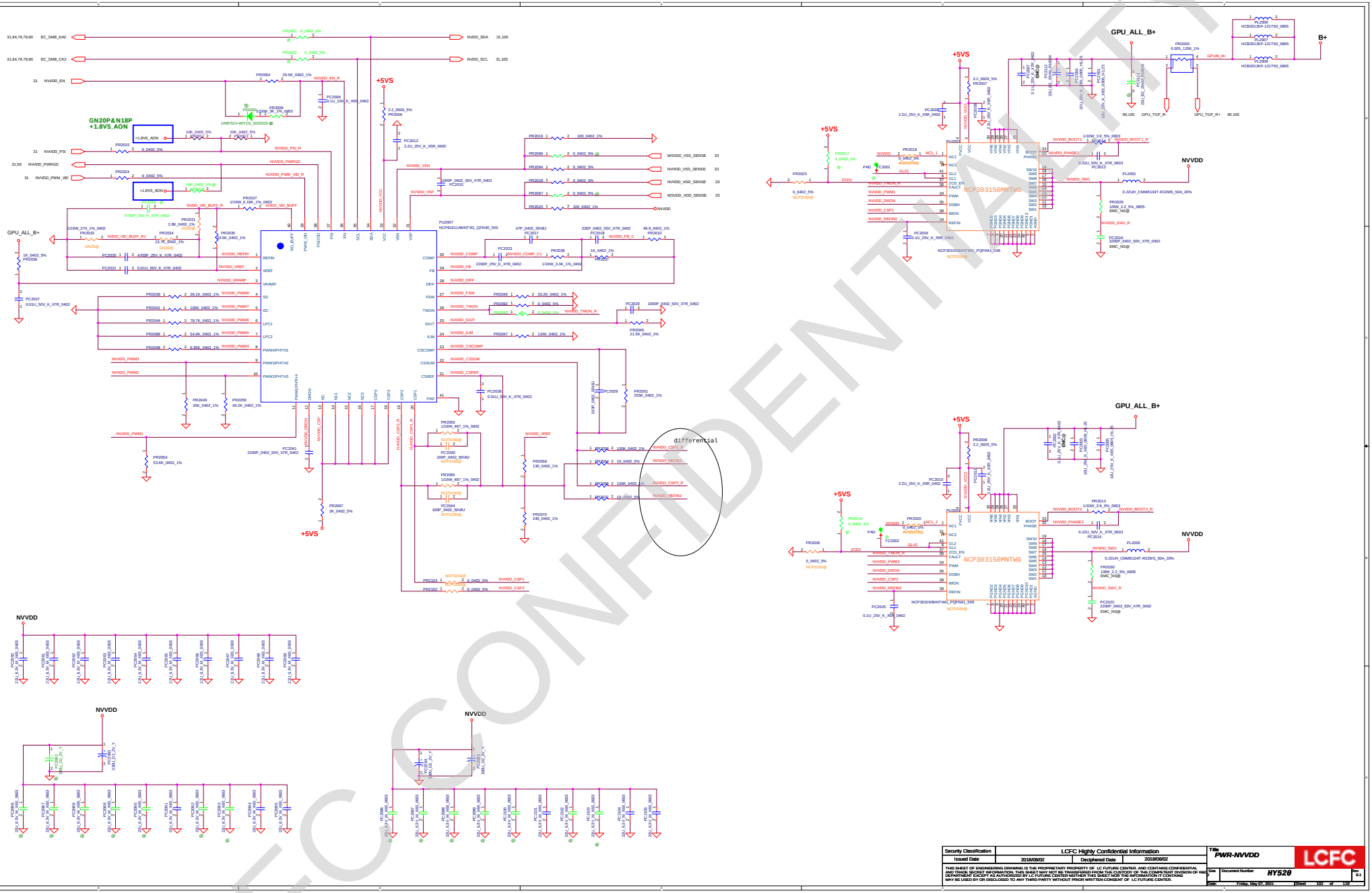

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Title	PWR-NVVDD	LCFC	
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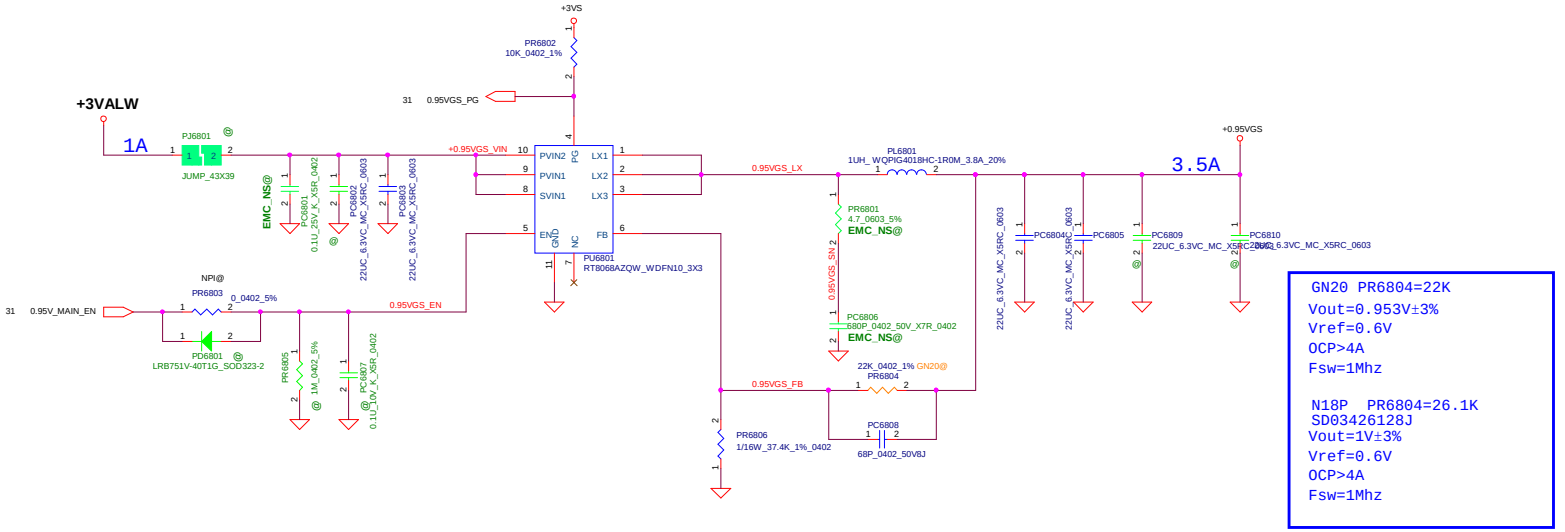

GN20 PR6804=22K
Vout=0.953V±3%
Vref=0.6V
OCP>4A
Fsw=1Mhz

N18P PR6804=26.1K
SD03426128J
Vout=1V±3%
Vref=0.6V
OCP>4A
Fsw=1Mhz

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Title: PWR_GPU PWR

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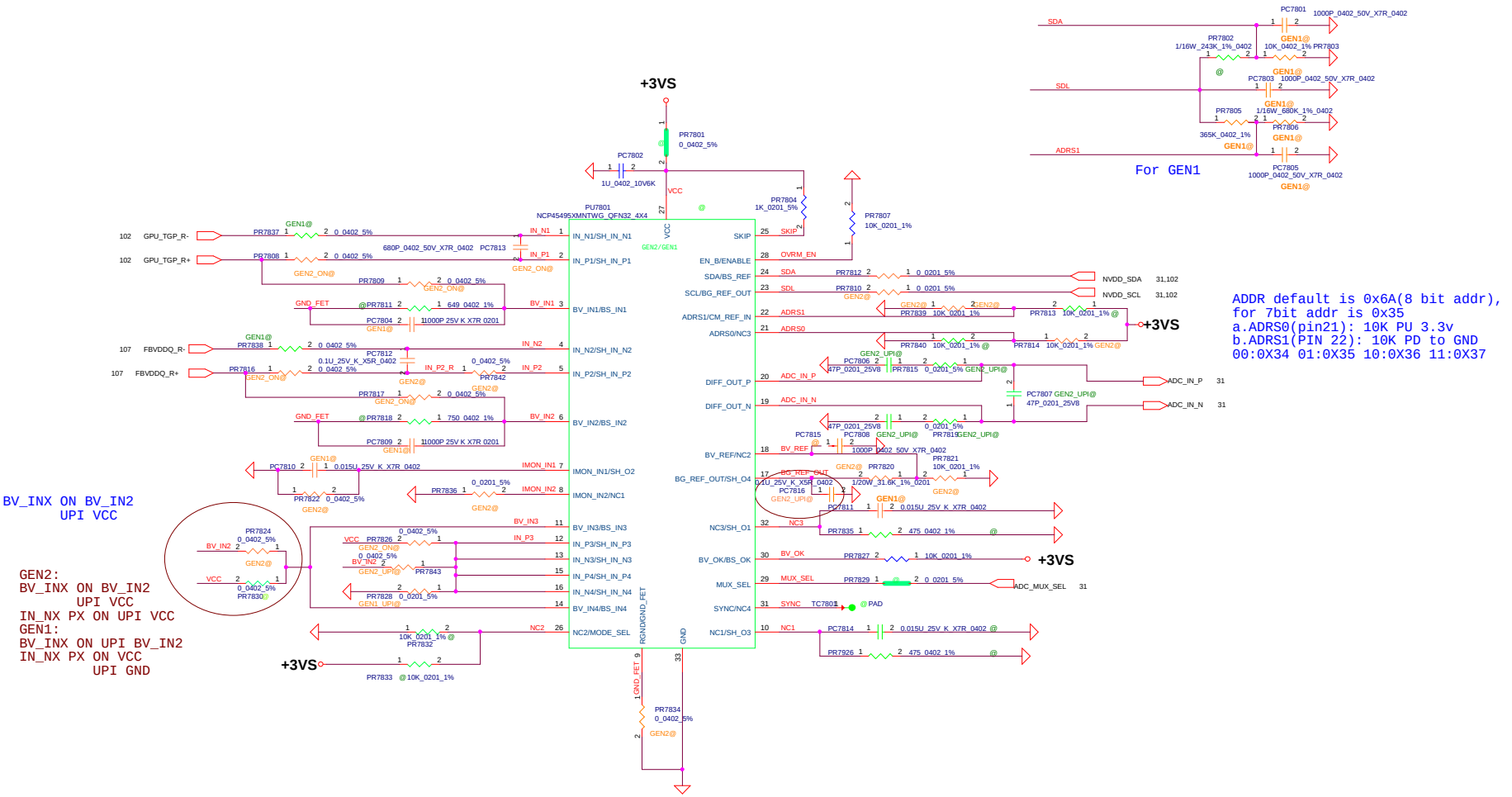

Security Classification	LCFC Highly Confidential Information		
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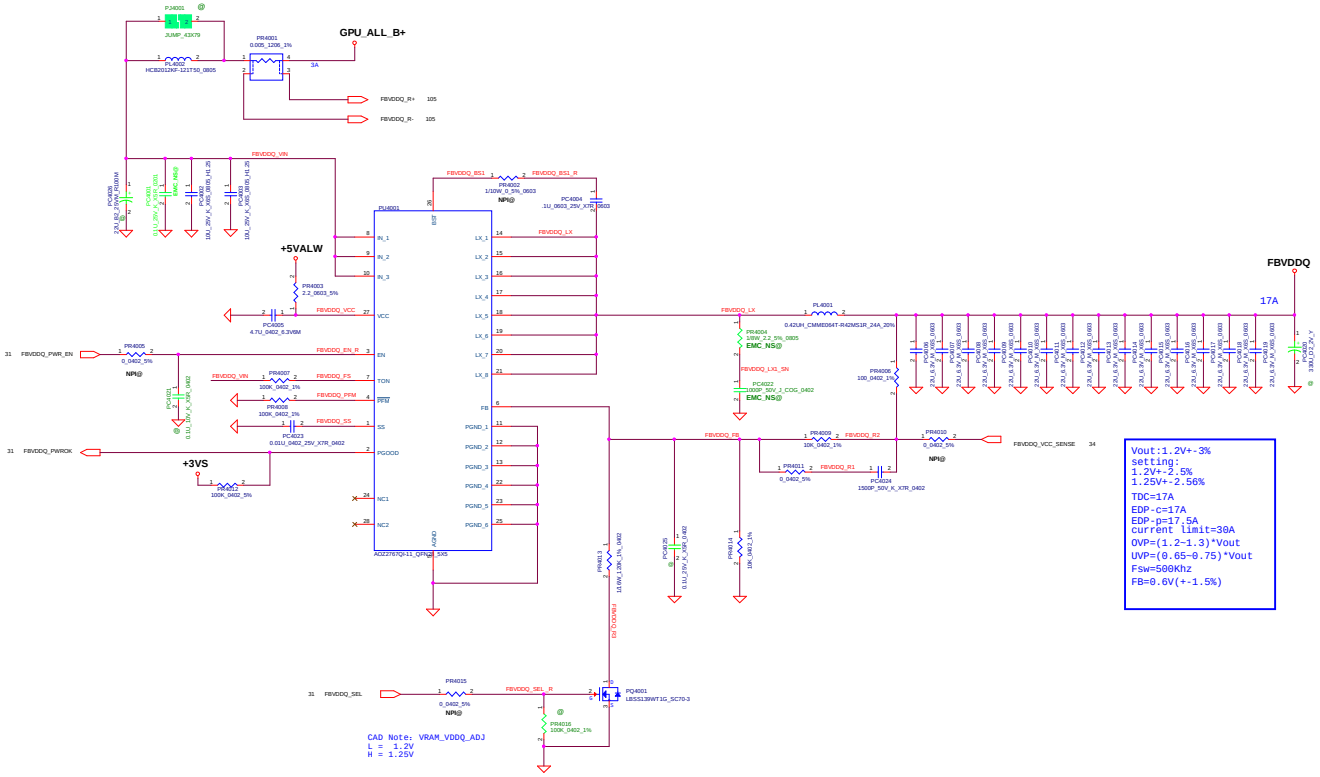

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Change List_EE

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Title: *Change Lise_PWR*

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