HP Typhon Z170 u-ATX Ver: 1.1

CPU:

INTEL-SkyLake LGA1151

System Chipset:

INTEL Z170

OnBoard Chipset:

HD Audio Codec:ALC1150
LAN-RTL8161GSH-CG
SIO:NCT 6683 D-T
Flash ROM: 8 MB SPI Quad read
HDMI level shift ASM1442K

Main Memory:

DDR4 (2133MHz) * 4 (2 DIMM per channel)

Expansion Slots:

PCI Express (X16) Slot * 2
M2 SSD key-M 4 lanes
M2 WLAN key A 1 lane

PWM:

IMVP8 - Onsemi 81203 6Phase(VCCP)+2Phase(VCCGT)

USB pin header:

USB2.0 X1(2 port) for card reader and NCT 9612D(MCU)
USB3.0 X1(2 port) for Type A (1 port support BC 1.2 charge)
USB3.0 X1(2 port) for Type C 2 port without PD

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Title: Cover Sheet

Size: Custom | Document Number: HP SCH P/N:MSI MS-7A09 | Rev: 10

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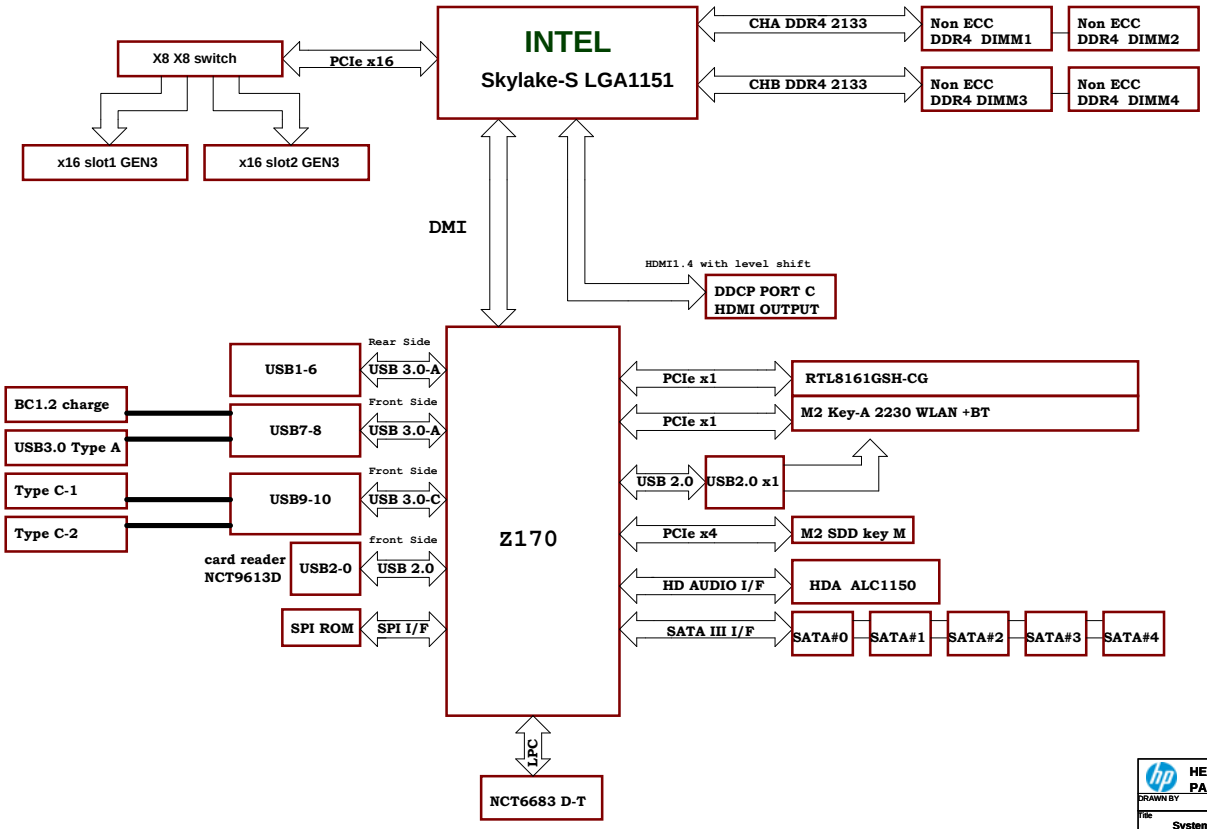
Block Diagram



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Title: System black Diagram

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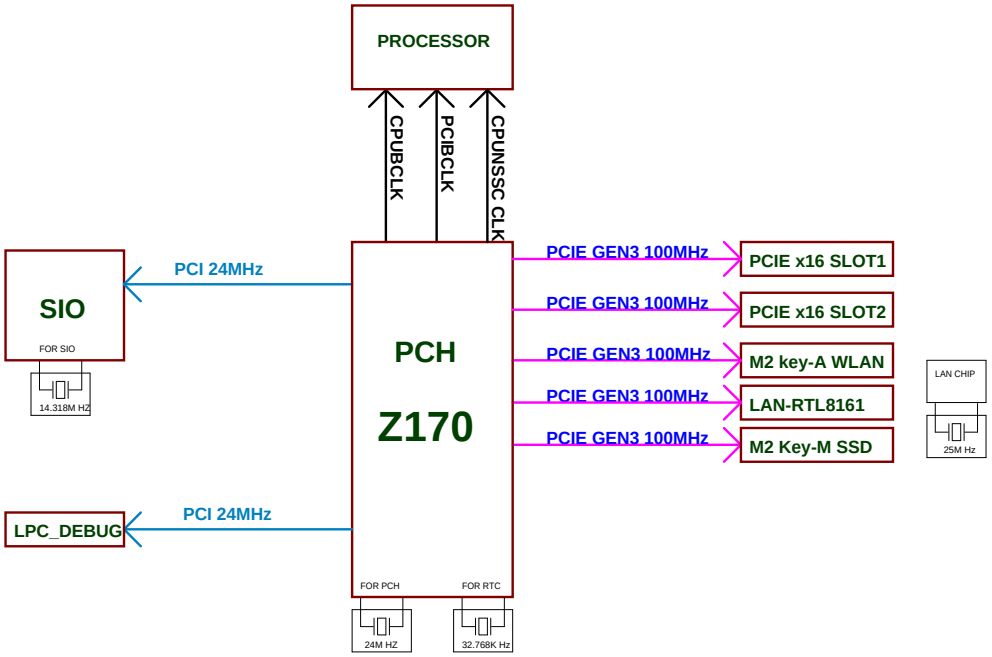
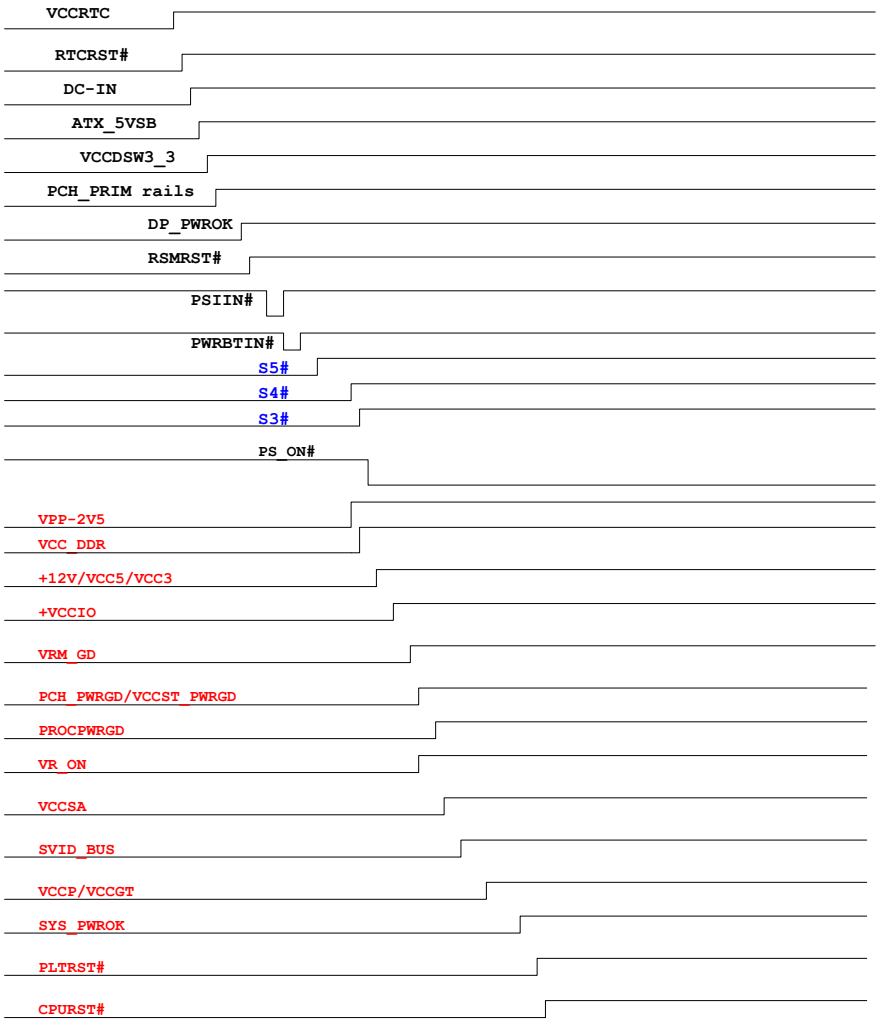
CLK MAP



Power ON Sequence

G3-->S5-->S0



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File	Power sequence & CLK Map
Size / Custom	Document Number: HP SCH P/N:MSI MS-7A09
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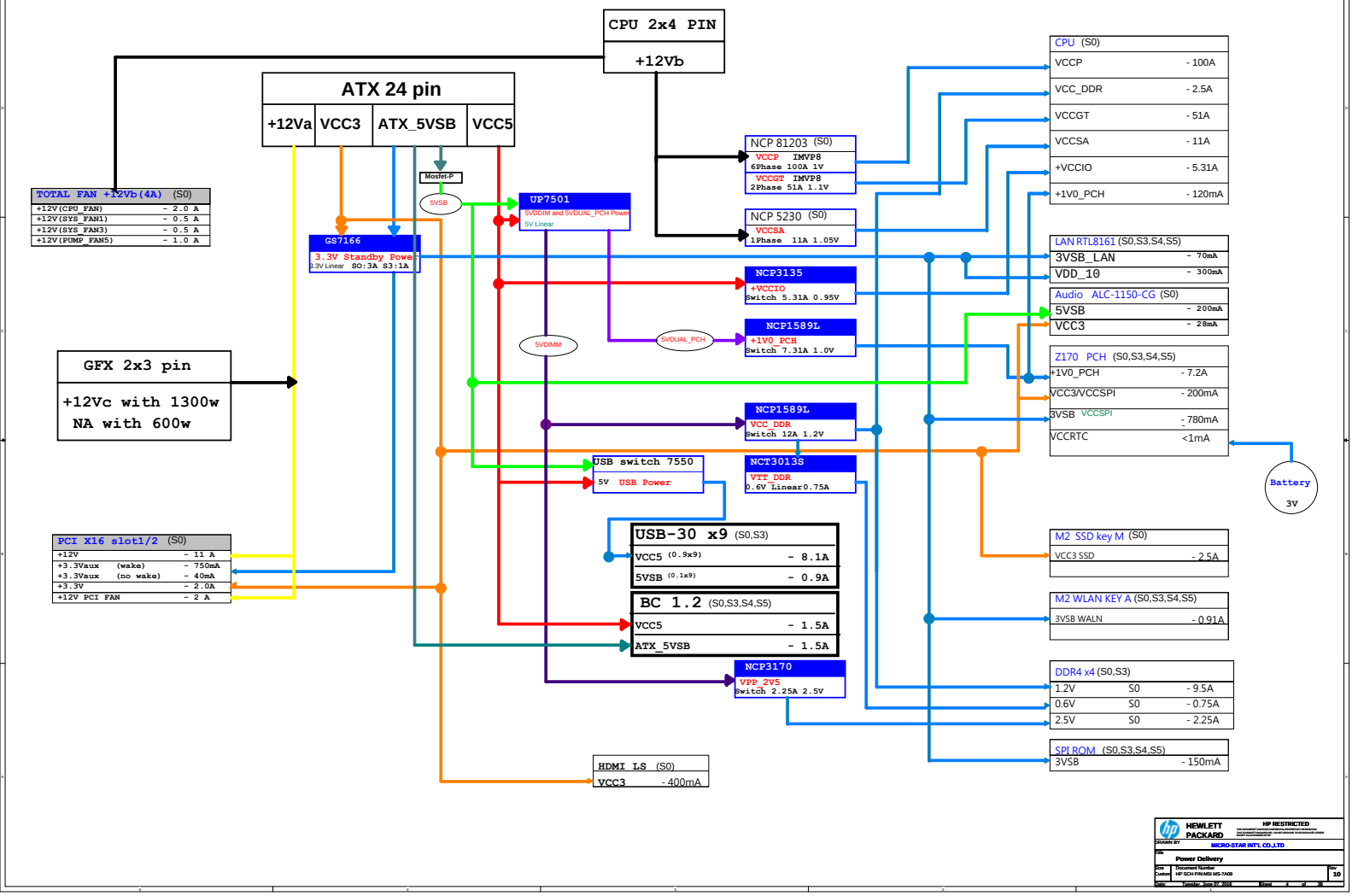
CPU 2x4 PIN
+12Vb
ATX 24 pin
+12Va
VCC3
ATX_5VSB
VCC5
TOTAL FAN +12Vb(4A) (S0)
+12V(CPU_FAN) - 2.0 A
+12V(SYS_FAN1) - 0.5 A
+12V(SYS_FAN3) - 0.5 A
+12V(PUMP_FAN5) - 1.0 A
Mosfet-P
5VSB
UP7501
5VDDIM and 5VDUAL_PCH Power
5V Linear
GS7166
3.3V Standby Power
3.3V Linear SO:3A S3:1A
NCP 81203 (S0)
VCCP IMVP8
6Phase 100A 1V
VCCGT IMVP8
2Phase 51A 1.1V
NCP 5230 (S0)
VCCSA
1Phase 11A 1.05V
NCP3135
+VCCIO
Switch 5.31A 0.95V
NCP1589L
+1V0_PCH
Switch 7.31A 1.0V
5VDIMM
5VDUAL_PCH
NCP1589L
VCC_DDR
Switch 12A 1.2V
NCT3013S
VTT_DDR
0.6V Linear0.75A
USB switch 7550
5V USB Power
GFX 2x3 pin
+12Vc with 1300w
NA with 600w
PCI X16 slot1/2 (S0)
+12V - 11 A
+3.3Vaux (wake) - 750mA
+3.3Vaux (no wake) - 40mA
+3.3V - 2.0A
+12V PCI FAN - 2 A
USB-30 x9 (S0,S3)
VCC5 (0.9x9) - 8.1A
5VSB (0.1x9) - 0.9A
BC 1.2 (S0,S3,S4,S5)
VCC5 - 1.5A
ATX_5VSB - 1.5A
NCP3170
VPP_2V5
Switch 2.25A 2.5V
HDMI LS (S0)
VCC3 - 400mA
CPU (S0)
VCCP - 100A
VCC_DDR - 2.5A
VCCGT - 51A
VCCSA - 11A
+VCCIO - 5.31A
+1V0_PCH - 120mA
LAN RTL8161 (S0,S3,S4,S5)
3VSB_LAN - 70mA
VDD_10 - 300mA
Audio ALC-1150-CG (S0)
5VSB - 200mA
VCC3 - 28mA
Z170 PCH (S0,S3,S4,S5)
+1V0_PCH - 7.2A
VCC3/VCCSPI - 200mA
3VSB VCCSPI - 780mA
VCCRTC <1mA
Battery
3V
M2 SSD key M (S0)
VCC3 SSD - 2.5A
M2 WLAN KEY A (S0,S3,S4,S5)
3VSB WALN - 0.91A
DDR4 x4 (S0,S3)
1.2V S0 - 9.5A
0.6V S0 - 0.75A
2.5V S0 - 2.25A
SPI ROM (S0,S3,S4,S5)
3VSB - 150mA
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Sunrise Point Z170

O	I		GPP_E0	I/O	primary 3.3V	SATAGP0	SATAGP0	strapping by M2 devices interface		Pull-up 10Kohm to VCC3	high: PCIE low:SATA
O	I		GPP_E1	I/O	primary 3.3V	SATAGP1	SATAGP1	strapping by resistor or BTC table		Pull-up 10Kohm to VCC3	high: PCIE low:SATA
O	I		GPP_E2	I/O	primary 3.3V	SATAGP2	SATAGP2	strapping by resistor or BTC table		Pull-down 10Kohm to VCC3	low:SATA
X	I		GPP_E3	I/O	primary 3.3V	GPI		NA		Pull-up 10Kohm to VCC3	
X	I		GPP_E4	I/O	primary 3.3V	GPI		NA		Pull-up 10Kohm to VCC3	
X	I		GPP_E5	I/O	primary 3.3V	GPI		NA		Pull-up 10Kohm to VCC3	
X	I		GPP_E6	I/O	primary 3.3V	GPI		NA		Pull-up 10Kohm to VCC3	
X	I		GPP_E7	I/O	primary 3.3V	GPI		NA		Pull-up 10Kohm to VCC3	
X	I		GPP_E8	I/O	primary 3.3V	GPI	SATA_LED#	active low by PCH		Pull-up 10Kohm to VCC3	
X	I		GPP_E9	I/O	primary 3.3V	GPI	OC#0	active low by USB OC event		Pull-up 10Kohm to USB power	
X	I		GPP_E10	I/O	primary 3.3V	GPI	OC#1	active low by USB OC event		Pull-up 10Kohm to USB power	
X	I		GPP_E11	I/O	primary 3.3V	GPI	OC#2	active low by USB OC event		Pull-up 10Kohm to USB power	
X	I		GPP_E12	I/O	primary 3.3V	GPI	OC#3	always high level		Pull-up 10Kohm to 3VSB	
O	I		GPP_F0	I/O	primary 3.3V	GPI	SATAGP3	strapping by resistor or BTC table		Pull-down 10Kohm to VCC3	low:SATA
O	I		GPP_F1	I/O	primary 3.3V	GPI	SATAGP4	strapping by resistor or BTC table		Pull-down 10Kohm to VCC3	low:SATA
X	I		GPP_F2	I/O	primary 3.3V	GPI	SATAGP5	NA, don't care		Pull-down 10Kohm to VCC3	
O	I		GPP_F3	I/O	primary 3.3V	GPI	SATAGP6	strapping by resistor or BTC table		Pull-up 10Kohm to VCC3	high: PCIE
O	I		GPP_F4	I/O	primary 3.3V	GPI	SATAGP7	strapping by resistor or BTC table		Pull-up 10Kohm to VCC3	high: PCIE

O	I		GPP_G0	I/O	primary 3.3V	GPI	ODD_SW+	ODD eject event by low trigger.		Pull-up 10Kohm to VCC3
X	I		GPP_G1	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G2	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G3	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G4	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G5	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G6	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G7	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G8	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G9	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G10	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G11	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G12	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G13	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G14	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G15	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G16	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G17	I/O	primary 3.3V	GPI		NA		
X	I		GPP_G18	I/O	primary 3.3V	GPI	NMI#			Pull-up 10Kohm to 3VSB
O	I		GPP_G19	I/O	primary 3.3V	GPI	ASM31_SMI#	USB31 SMI# low trigger to PCH		Pull-up 10Kohm to 3VSB

X	I		GPP_H21	I/O	primary 3.3V	GPI		NA		
X	I		GPP_H22	I/O	primary 3.3V	GPI		NA		
X	I		GPP_H23	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I0	I/O	primary 3.3V	GPI		NA		
O	I		GPP_I1	I/O	primary 3.3V	GPI	HDMI_PORTC_HPD	active high when connect to HDMI monitor.	PD 20K	
X	I		GPP_I2	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I3	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I4	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I5	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I6	I/O	primary 3.3V	GPO		NA	PD 20K	
O	I		GPP_I7	I/O	primary 3.3V	GPI	DDPC_CTRLCLK	HDMI I2C		
O	I		GPP_I8	I/O	primary 3.3V	GPO	DDPC_CTRLDATA	HDMI I2C, active high by PU VCC3.	PD 20K	Pull-up 2.2Kohm to VCC3
X	I		GPP_I9	I/O	primary 3.3V	GPI		NA		
X	I		GPP_I10	I/O	primary 3.3V	GPO		NA	PD 20K	
X	I		GPD0	I/O	primary 3.3V	GPI	BATLOW#			Pull-up 10Kohm to 3VSB
X	I		GPD1	I/O	primary 3.3V	GPI	ACPRESENT			Pull-up 10Kohm to 3VSB
X	I		GPD2	I/O	primary 3.3V	LAN_WAKE#	LAN_WAKE#			Pull-up 100Kohm to +FATX_3VSB
X	I		GPD3	I/O	primary 3.3V	PWRBTN#	PWRBTN#			Pull-up 4.7Kohm to 3VSB
X	I		GPD4	I/O	primary 3.3V	SLP_S3#	SLP_S3#			

NCT 6683 D-T

37	YLW_LED	GPIO30	SLCT			NC	CDR_BTN#	I	external PD to GND	low	TBD,GPI for EC.
38	GPIO31	PE	P2_DGL#			NC	CDR_PRSNT#	I	external PU 3VSB	high	PRSNT# low level if DGFX plug-in GPI for EC
39	GPIO32	BUSY	P2_DGL#			NC	CDR_PWRGD	I		low	Caldera resume power well and input pin. GPI for EC.
40	GPIO33	ACK#	P2_DGH#			GPIO	LED_VSB	O/OD	external PU 3VSB	high	active by high level at APCI S0 state and low level at APCI S3 state. GPO for EC.
41	GPIO34	PD7	P2_DGH#			GPIO	FUSB_ON	O/OD	external PU +FATX_3VSB	high	support USB wake up from non deep S5 for steambos application.GPO for EC.
42	GPIO35	PD6	LED_A			GPIO	FUSB_ON	O/OD	external PU +FATX_3VSB	high	support USB wake up from non deep S5 for steambos application.GPO for EC.
43	GPIO36	PD5	LED_B			GPIO	CDR_RED#	O/OD	external PU 3VSB	high	TBD,GPO for EC.
44	GPIO37	PD4	LED_C			GPIO	CDR_WHITE#	O/OD	external PU 3VSB	high	TBD,GPO for EC.
45	GPIO40	PD3	LED_D			GPIO	LAN_ON	O/OD	external PU 3VSB	high	onboard LAN power controll.GPO for EC.
46	GPIO41	PD2	LED_E			GPIO	ME_DISABLE	O/OD	external PU 3VSB	high	ME disable by low level.GPO for EC.
47	GPIO42	PD1	LED_F			GPIO	USB3.0_cable_detect#	I/OD	external PU 3VSB	high	detect USB3.0 cable plug-in if trigger by low level.GPI for EC.
48	GPIO43	PD0	LED_G			GPIO	M2_WALN_DET#	I/OD	external PU 3VSB	high	detect M2 WLAN device plug-in if trigger by low level.GPI for EC.
49	GPIO44	SLIN#	P1_DGL#			GPIO	M2_SSD_detect#	I/OD	external PU 3VSB	high	detect M2 SSD device plug-in if trigger by low level.GPI for EC.
50	GPIO45	INIT#	P1_DGL#			GPIO	HDMI_DDPC_HPD	I/OD	HDMI cable and monitor power driver	low	detect HDMI cable and monitor plug-in if trigger by high level.GPI for EC.
51	GPIO46	ERR#	P1_DGH#			GPIO	FP_AUD_DET#	I/OD	external PU VCC3	high	detect FP AUDIO cable plug-in if trigger by low level. GPI for EC.
52	GPIO47	AFD#	P1_DGH#			GPIO	PAS_DET#	I/OD	external PU 3VSB	high	CLEAR PASSWORD if trigger by low level.GPI for EC.

DDR-4 DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	000	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	001	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 3	010	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1
DIMM 4	011	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3

Power On Strapping Table form NCT6683 D-T

Symbol	Value	Description
2E_4E_SEL	0	SIO I/O address is 2EH/2FH
	1	SIO I/O address is 4EH/4FH
BKFD_EN	0	Pin67 3VSBSWI, Pin69 RSTOUT#x
	1	Pin67 BKFD_CUT, Pin69 LATCHED_BKFD_CUT
TESTMODE1	0	Please always pull down this pin with 1Kohm resistor.
DIS_HWACPI	0	Hardware ACPI could take over related signals
	1	Hardware ACPI never take over related signals
TESTMODE3 (SPI_CS#_SIO)	0	Output "0" : Pin93, 108, 123, 138 Output "z" : Pin69, 61, 62, 67, 70, 71, 121, 122 Configuration Register I/O port is 4E/4F.
SBI_CFG_EN (SPI_CLK_SIO)	0	Switches open or close are determined by AT/PDD
	1	Switches open or close are determined by configuration register

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Title PCH & SIO GPIO setting

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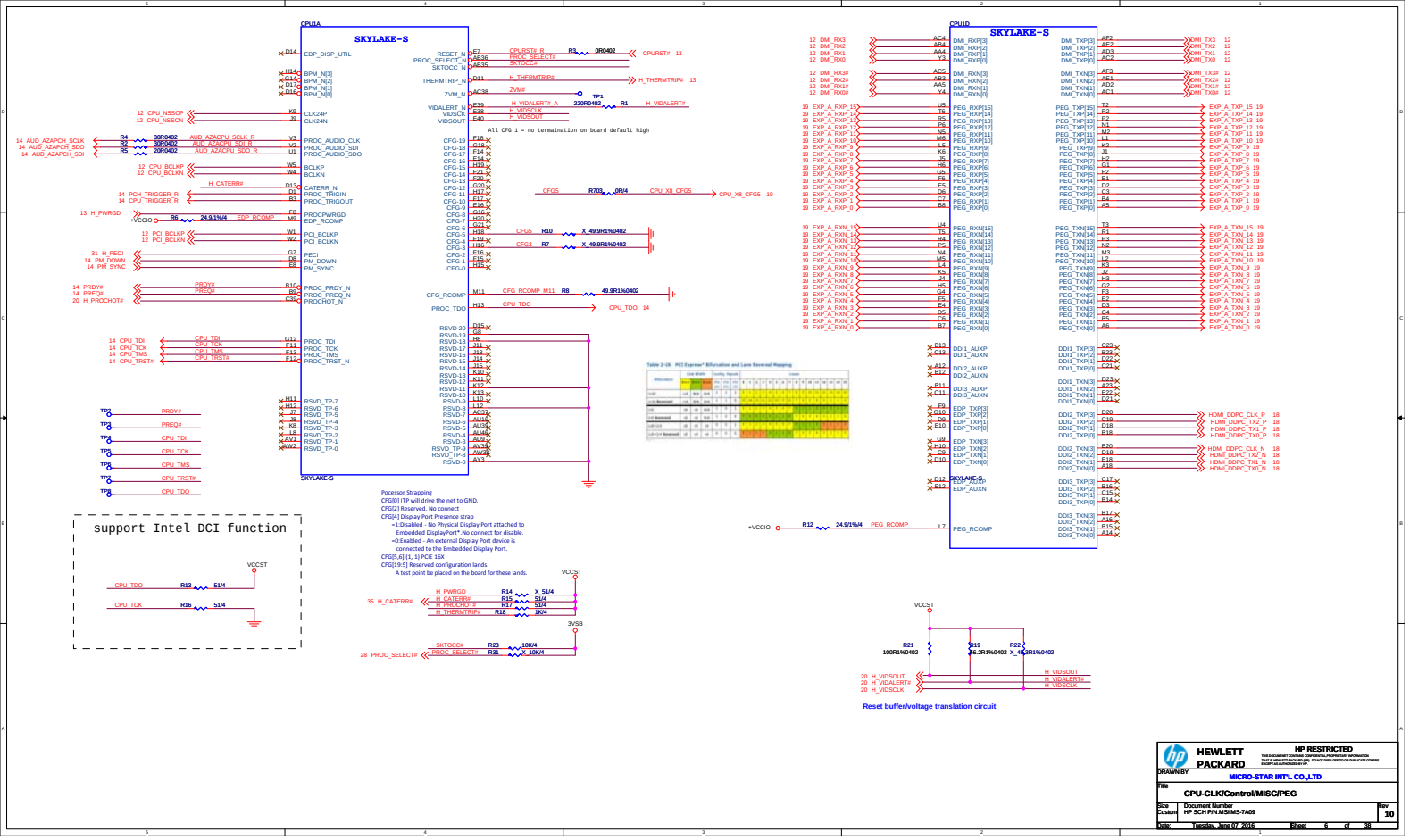
CPU1A
SKYLAKE-S
EDP_DISP_UTIL
BPM_N[3]
BPM_N[2]
BPM_N[1]
BPM_N[0]
CLK24P
CLK24N
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
BCLKP
BCLKN
CATERR_N
PROC_TRIGIN
PROC_TRIGOUT
PROCPWRGD
EDP_RCOMP
PCI_BCLKP
PCI_BCLKN
PECI
PM_DOWN
PM_SYNC
PROC_PRDY_N
PROC_PREQ_N
PROCHOT_N
PROC_TDI
PROC_TCK
PROC_TMS
PROC_TRST_N
RSVD_TP-7
RSVD_TP-6
RSVD_TP-5
RSVD_TP-4
RSVD_TP-3
RSVD_TP-2
RSVD_TP-1
RSVD_TP-0
RESET_N
PROC_SELECT_N
SKTOCC_N
THERMTRIP_N
ZVM_N
VIDALERT_N
VIDSCLK
VIDSOUT
CFG-19
CFG-18
CFG-17
CFG-16
CFG-15
CFG-14
CFG-13
CFG-12
CFG-11
CFG-10
CFG-9
CFG-8
CFG-7
CFG-6
CFG-5
CFG-4
CFG-3
CFG-2
CFG-1
CFG-0
CFG_RCOMP
PROC_TDO
RSVD-20
RSVD-19
RSVD-18
RSVD-17
RSVD-16
RSVD-15
RSVD-14
RSVD-13
RSVD-12
RSVD-11
RSVD-10
RSVD-9
RSVD-8
RSVD-7
RSVD-6
RSVD-5
RSVD-4
RSVD-3
RSVD_TP-8
RSVD_TP-9
RSVD-0
SKYLAKE-S
All CFG 1 = no termination on board default high
CPURST# 13
H_THERMTRIP# 13
H_VIDALERT#
CPU_X8_CFG5 19
CPU_TDO 14
Processor Strapping
CFG[0] ITP will drive the net to GND.
CFG[2] Reserved. No connect
CFG[4] Display Port Presence strap
=1:Disabled - No Physical Display Port attached to Embedded DisplayPort*.No connect for disable.
=0:Enabled - An external Display Port device is connected to the Embedded Display Port.
CFG[5,6] (1, 1) PCIE 16X
CFG[19:5] Reserved configuration lands.
A test point be placed on the board for these lands.
support Intel DCI function
VCCST
CPU_TDO
CPU_TCK
CPU_TMS
CPU_TRST#
CPU_TDI
PREQ#
PRDY#
3VSB
CPU1D
SKYLAKE-S
DMI_RXP[3]
DMI_RXP[2]
DMI_RXP[1]
DMI_RXP[0]
DMI_RXN[3]
DMI_RXN[2]
DMI_RXN[1]
DMI_RXN[0]
DMI_TXP[3]
DMI_TXP[2]
DMI_TXP[1]
DMI_TXP[0]
DMI_TXN[3]
DMI_TXN[2]
DMI_TXN[1]
DMI_TXN[0]
PEG_RXP[15]
PEG_RXP[14]
PEG_RXP[13]
PEG_RXP[12]
PEG_RXP[11]
PEG_RXP[10]
PEG_RXP[9]
PEG_RXP[8]
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PEG_RXP[6]
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PEG_RXN[11]
PEG_RXN[10]
PEG_RXN[9]
PEG_RXN[8]
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PEG_TXP[13]
PEG_TXP[12]
PEG_TXP[11]
PEG_TXP[10]
PEG_TXP[9]
PEG_TXP[8]
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PEG_TXN[9]
PEG_TXN[8]
PEG_TXN[7]
PEG_TXN[6]
PEG_TXN[5]
PEG_TXN[4]
PEG_TXN[3]
PEG_TXN[2]
PEG_TXN[1]
PEG_TXN[0]
DDI1_AUXP
DDI1_AUXN
DDI2_AUXP
DDI2_AUXN
DDI3_AUXP
DDI3_AUXN
EDP_TXP[3]
EDP_TXP[2]
EDP_TXP[1]
EDP_TXP[0]
EDP_TXN[3]
EDP_TXN[2]
EDP_TXN[1]
EDP_TXN[0]
SKYLAKE-S
EDP_AUXP
EDP_AUXN
DDI1_TXP[3]
DDI1_TXP[2]
DDI1_TXP[1]
DDI1_TXP[0]
DDI1_TXN[3]
DDI1_TXN[2]
DDI1_TXN[1]
DDI1_TXN[0]
DDI2_TXP[3]
DDI2_TXP[2]
DDI2_TXP[1]
DDI2_TXP[0]
DDI2_TXN[3]
DDI2_TXN[2]
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DDI2_TXN[0]
DDI3_TXP[3]
DDI3_TXP[2]
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DDI3_TXP[0]
DDI3_TXN[3]
DDI3_TXN[2]
DDI3_TXN[1]
DDI3_TXN[0]
PEG_RCOMP
HDMI_DDPC_CLK_P
HDMI_DDPC_TX2_P
HDMI_DDPC_TX1_P
HDMI_DDPC_TX0_P
HDMI_DDPC_CLK_N
HDMI_DDPC_TX2_N
HDMI_DDPC_TX1_N
HDMI_DDPC_TX0_N
Reset buffer/voltage translation circuit
HEWLETT PACKARD
HP RESTRICTED
DRAWN BY
MICRO-STAR INT'L CO.,LTD
File
CPU-CLK/Control/MISC/PEG
Size
Custom
Document Number
HP SCH P/N:MSI MS-7A09
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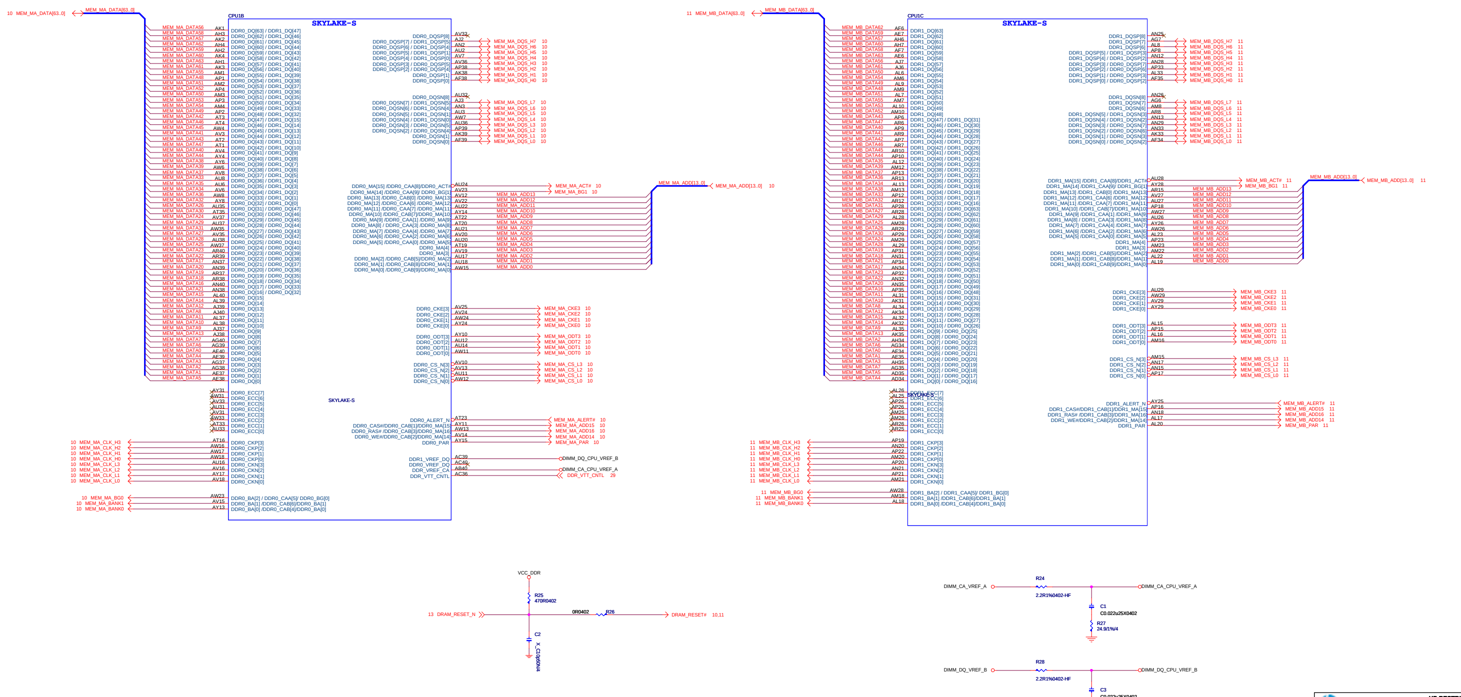

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Title	CPU-Memory	
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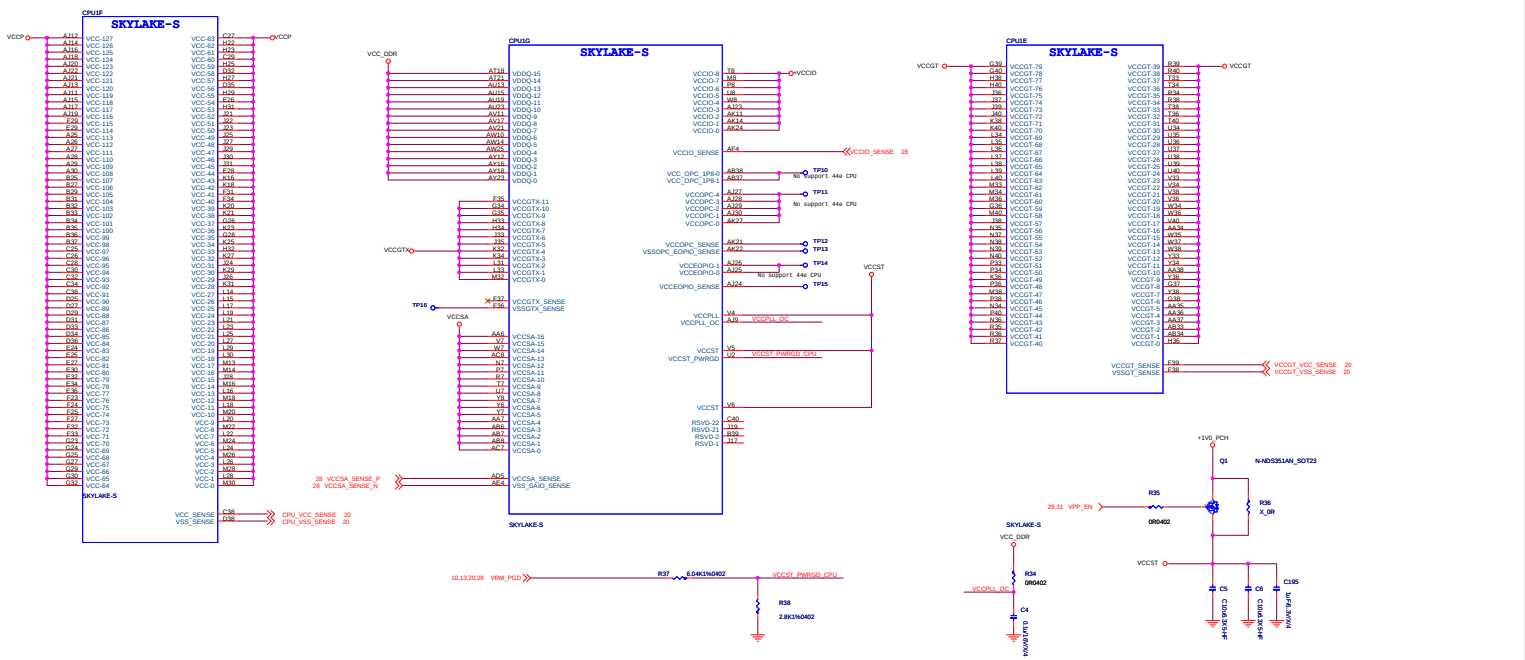

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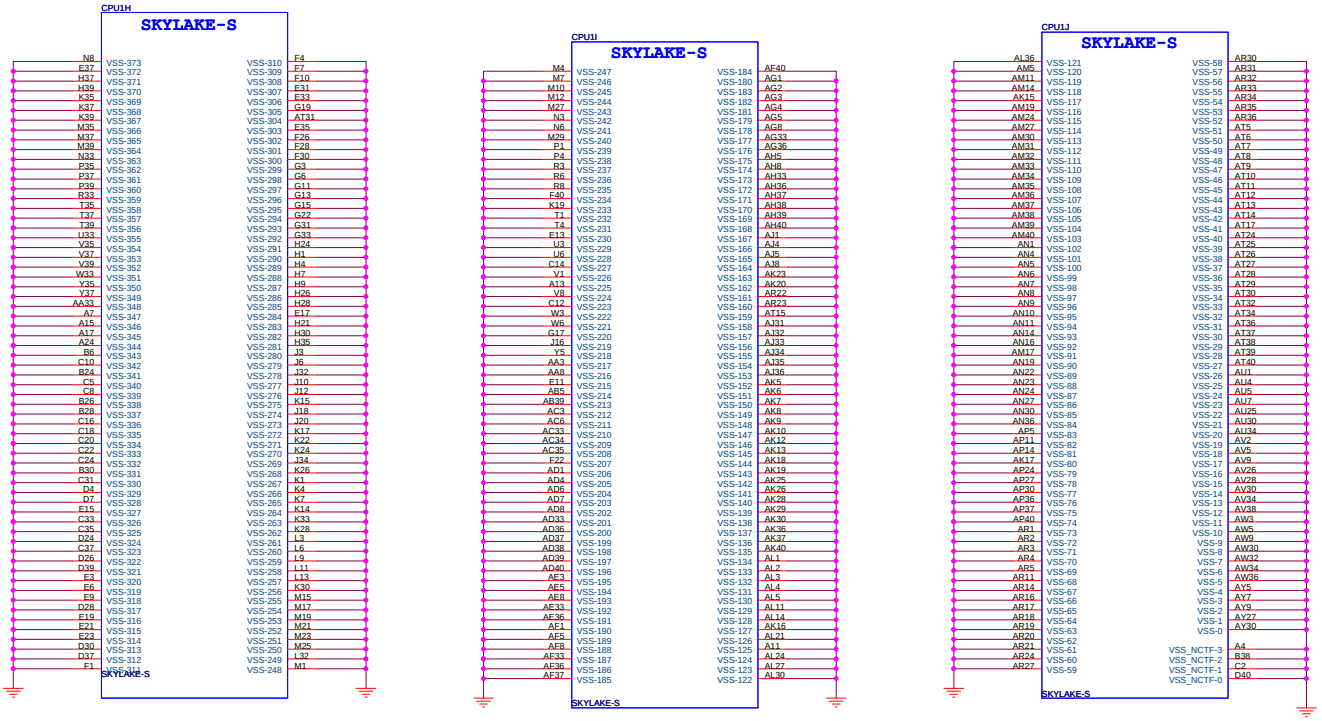

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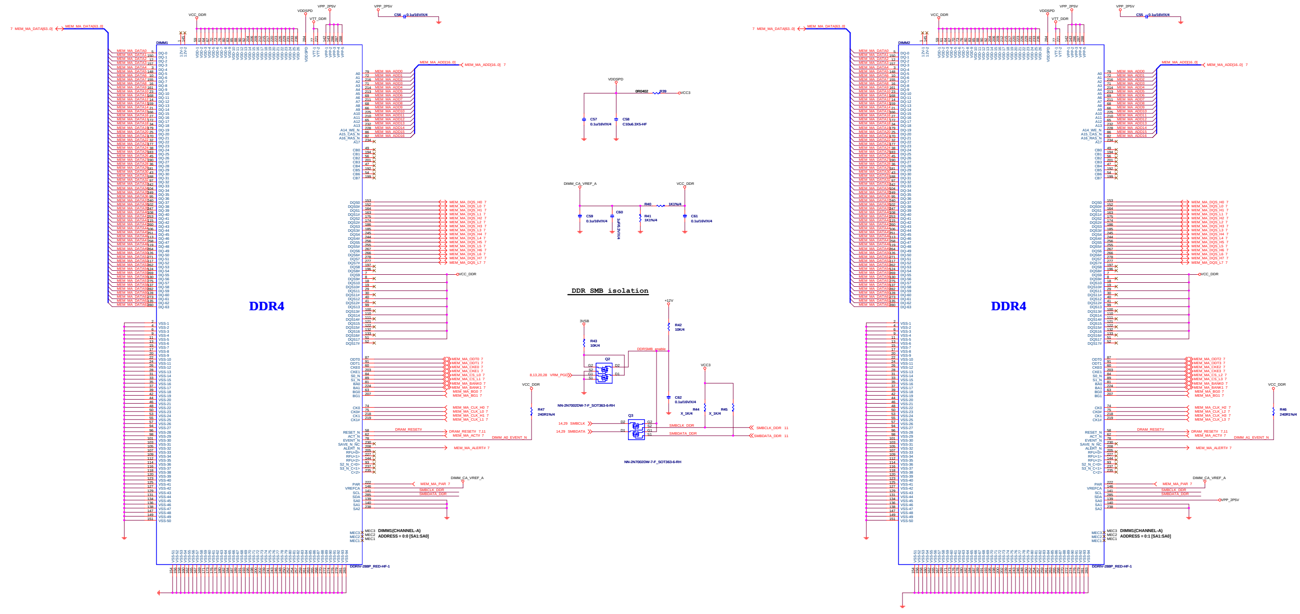
DDR4 DIMM_A0

DDR4 DIMM_A1



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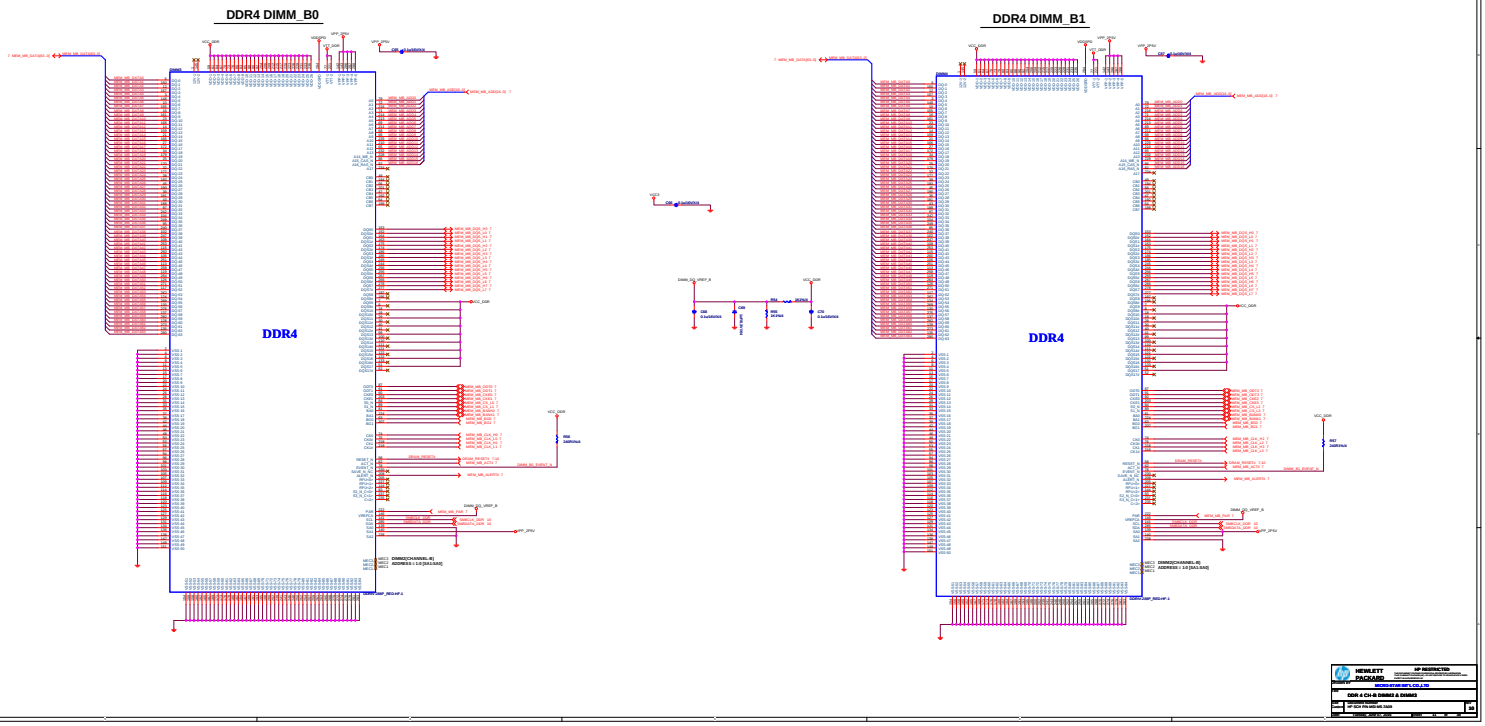
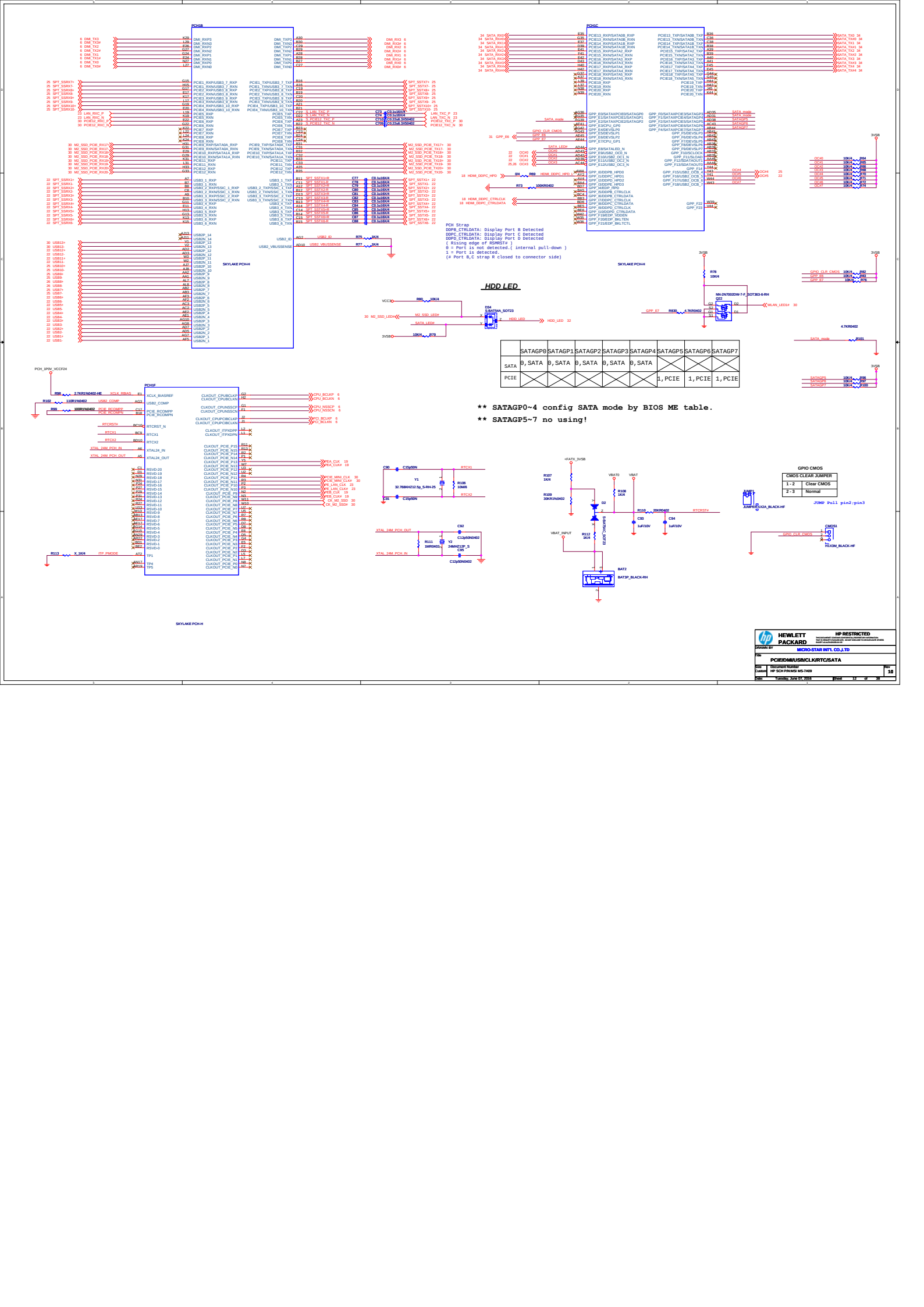
Title	DDR 4 CH-A DIMM1 & DIMM2		
Size: Custom	Document Number: HP SCH P/N:MSI MS-7A09		Rev: 10
Date:	Tuesday, June 07, 2016	Sheet 10 of 38	


DDR4 DIMM_B0
DDR4 DIMM_B1
DDR4
DDR4
HEWLETT PACKARD
HP RESTRICTED
DDR 4 CH-B DIMM2 & DIMM3


PCH Strap
DDPB_CTRLDATA: Display Port B Detected
DDPC_CTRLDATA: Display Port C Detected
DDPD_CTRLDATA: Display Port D Detected
(Rising edge of RSMRST#)
0 = Port is not detected.(internal pull-down)
1 = Port is detected.
(# Port B,C strap R closed to connector side)
HDD LED
SATAGP0 SATAGP1 SATAGP2 SATAGP3 SATAGP4 SATAGP5 SATAGP6 SATAGP7
SATA 0,SATA 0,SATA 0,SATA 0,SATA
PCIE 1,PCIE 1,PCIE 1,PCIE
** SATAGP0~4 config SATA mode by BIOS ME table.
** SATAGP5~7 no using!
GPIO CMOS
CMOS CLEAR JUMPER
1 - 2 Clear CMOS
2 - 3 Normal
JUMP Full pin2:pin3
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PCIE/DMI/USB/CLK/RTC/SATA
HP SCH PIN/MSI MS-7A09
10
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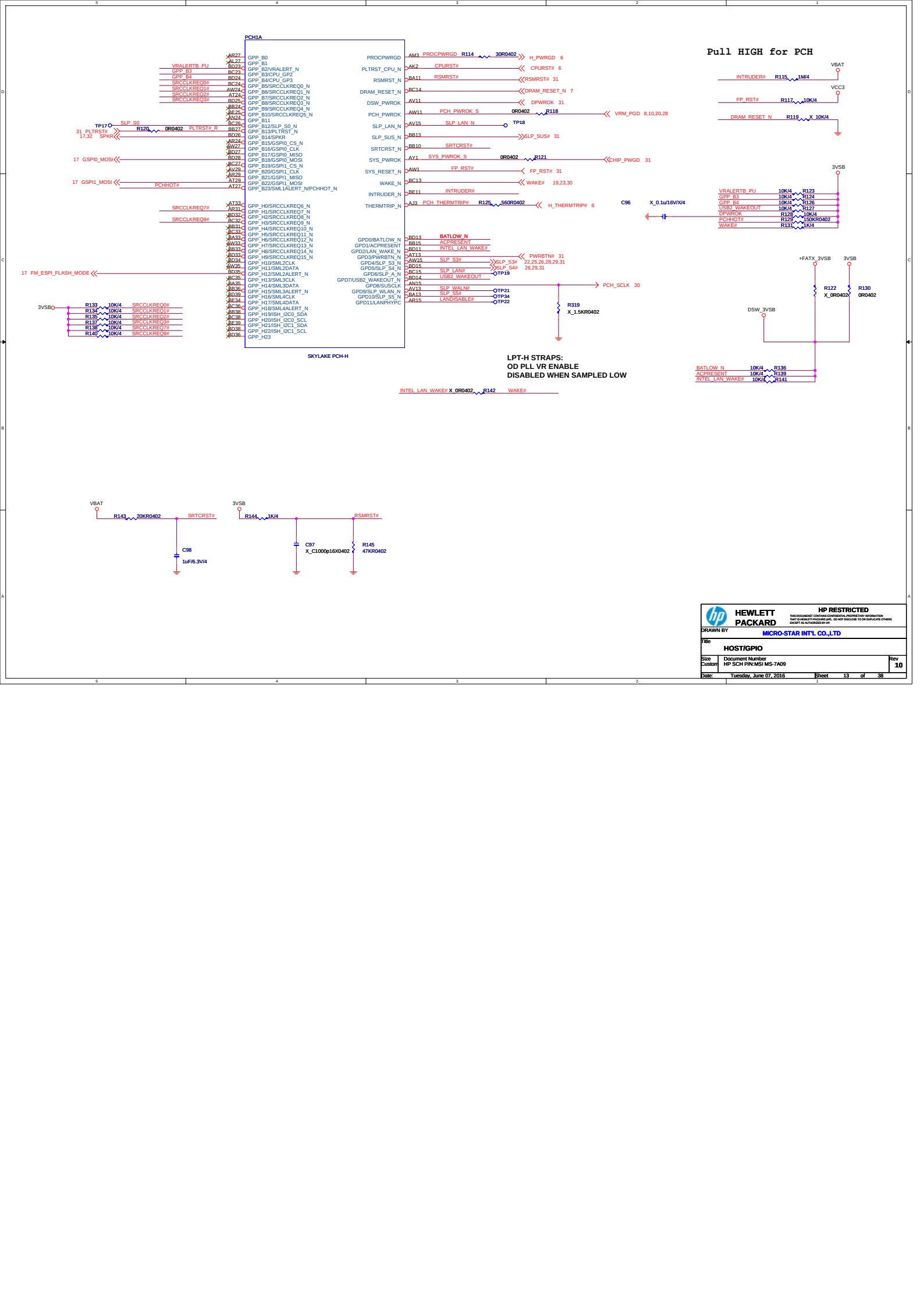
PCH1A
SKYLAKE PCH-H
Pull HIGH for PCH
LPT-H STRAPS:
OD PLL VR ENABLE
DISABLED WHEN SAMPLED LOW
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HOST/GPIO
Size
Custom
Document Number
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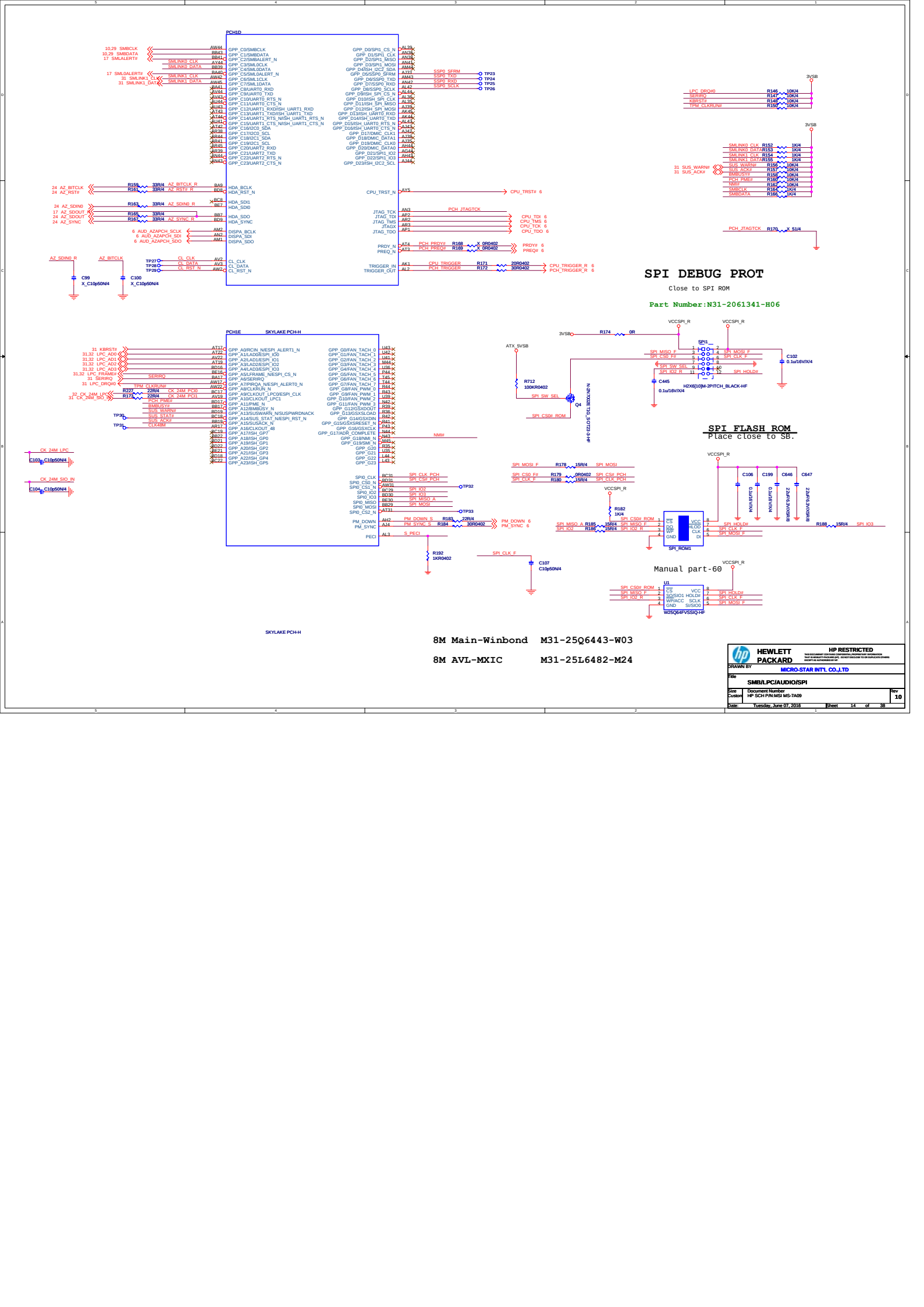
PCH1D
SKYLAKE PCH-H
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2061341-H06
SPI FLASH ROM
Place close to SB.
Manual part-60
SPI_ROM1
W25Q64FVSSIQ-HF
8M Main-Winbond M31-25Q6443-W03
8M AVL-MXIC M31-25L6482-M24
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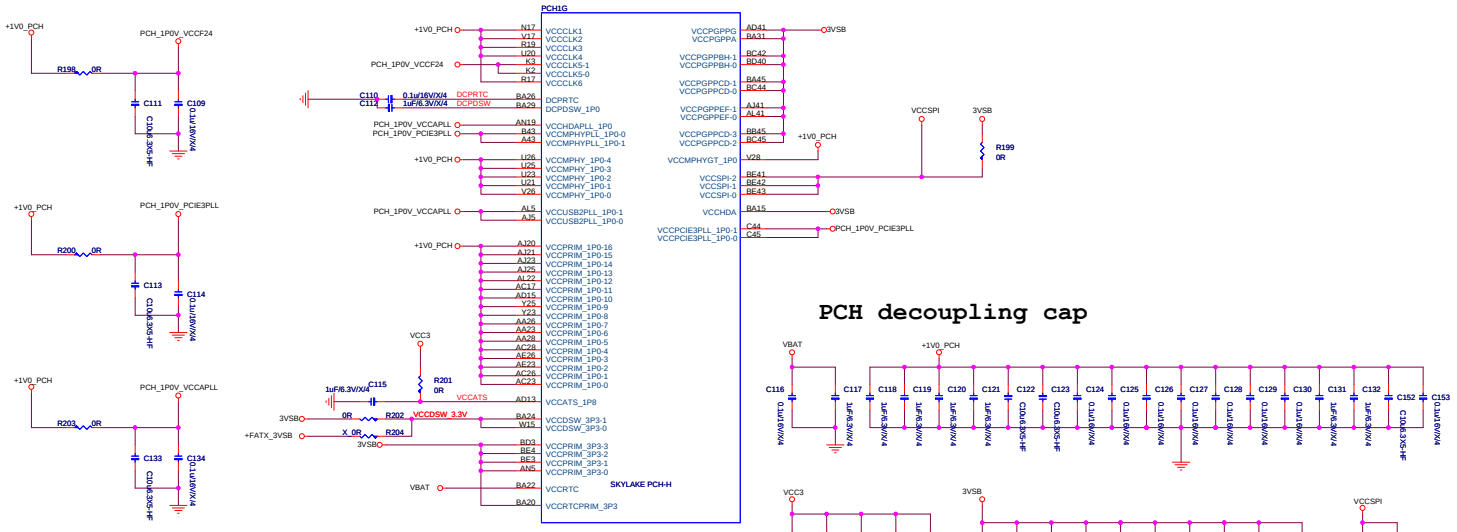

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Title

PCH-GND

Size	Document Number	Rev
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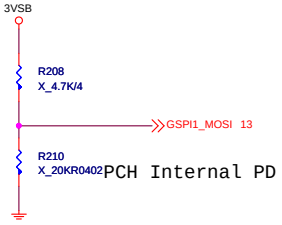
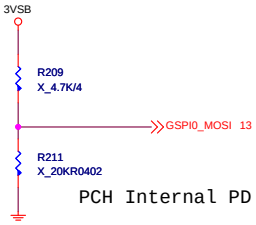
GPP-B strapping

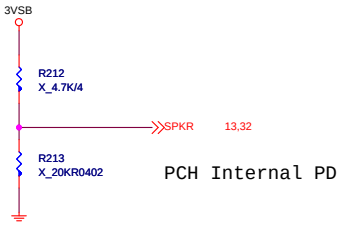
GSPI1_MOSI	GPP_B22
LPC	1
SPI	0 **



GSPI0_MOSI	GPP_B18
Enable no boot	1
disable No boot	0 **

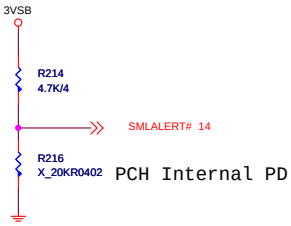


SWAP OVERRIDE STRAP	GPP_B14
ENABLE	1
DISABLE	0 **(default)



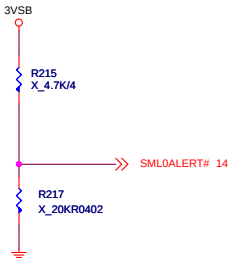
GPP-C strapping

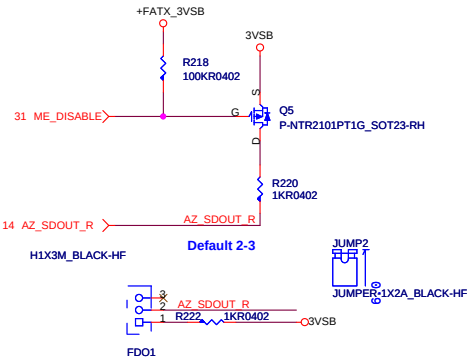
TLS	SMLALERT#
ENABLE	1 **
DISABLE	0



HW strapping

boot type	SML0ALERT#
ESPI	1
LPC	0 **(default)





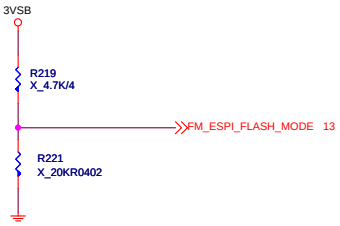
HDA_SDO need to be pulled high to disable flash securtity and ME

HW strapping

ESPI flash sharing mode

	GPP_H12
Slave	1
Master	0 **(default)

PCH Internal PD



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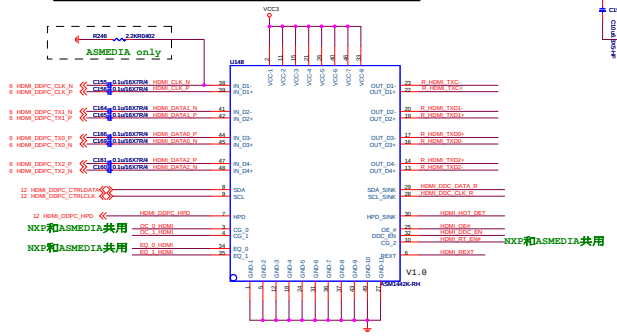
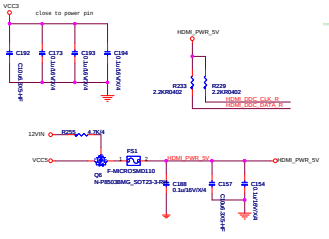
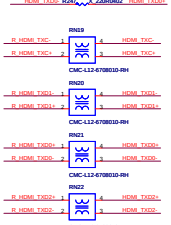
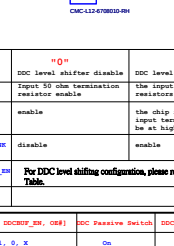
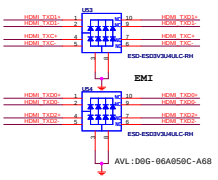
HDMI1.4 with level shifter (4K x 2K supporting)

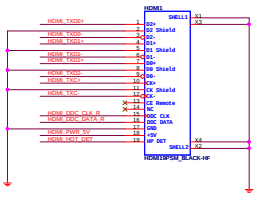


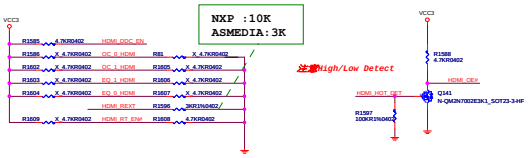












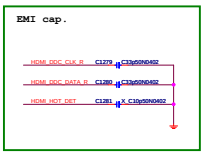


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

DDC_EN	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedance	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off

PCI, PCO		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	

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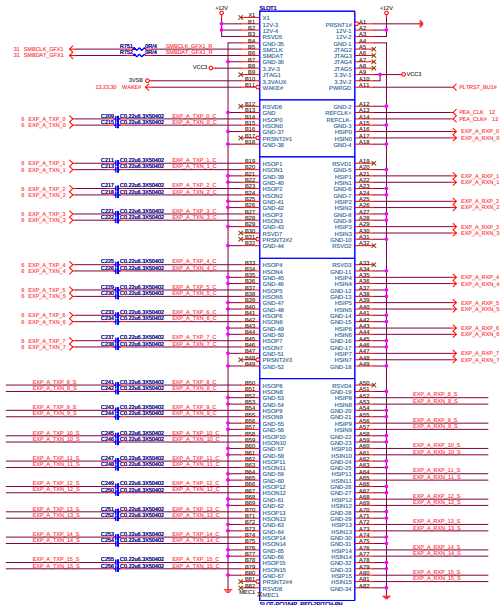
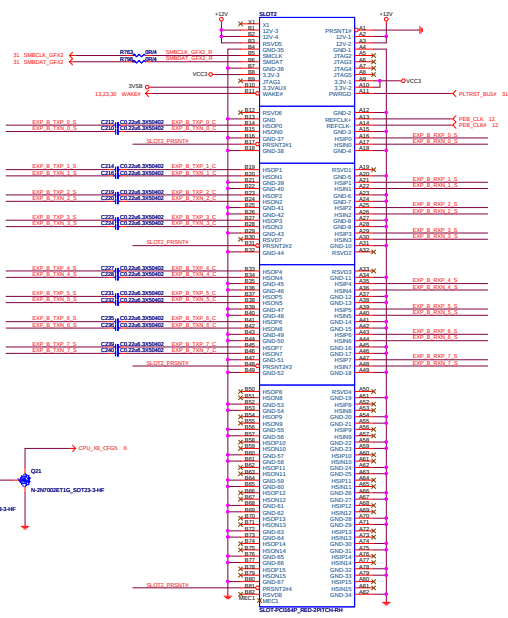
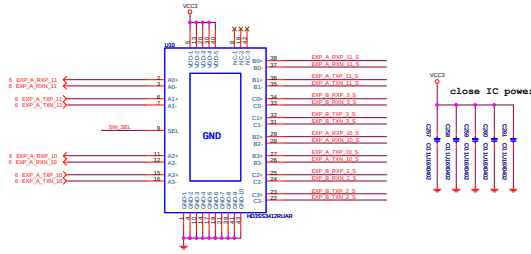
PCI EXPRESS X16 SLOT

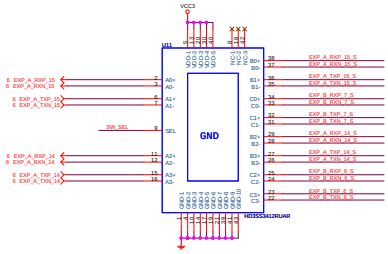


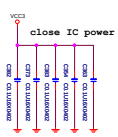
SLOT2_PRSNT#	1	0(active)
SW_SEL	0	1
	A=B	A=C
CFG	Normal	SLI
SLOT1	16	8
SLOT2	0	X1~X8

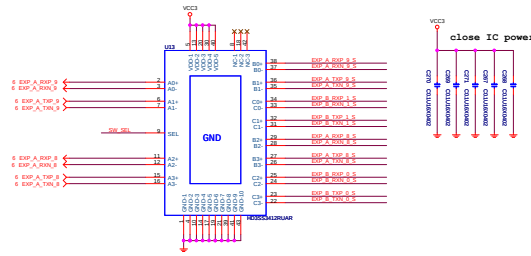
PCI EXPRESS X16 SLOT

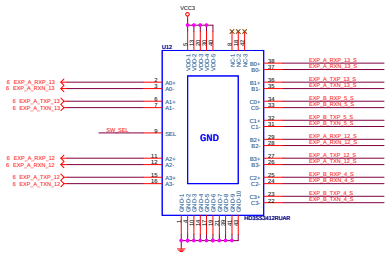


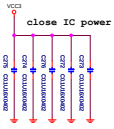












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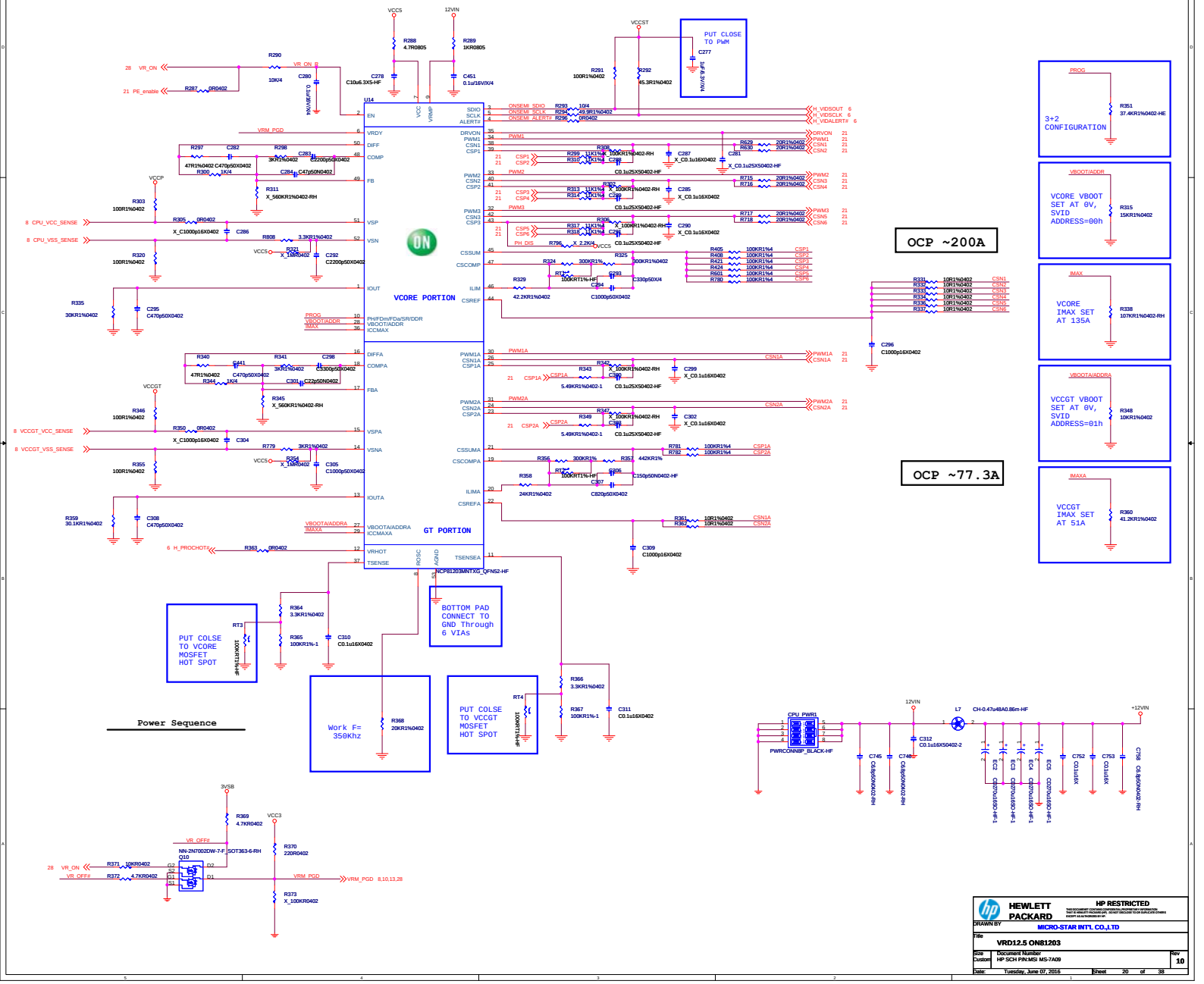
VOLTAGE REGULATOR MODULE (VRD12.5)



Power Sequence

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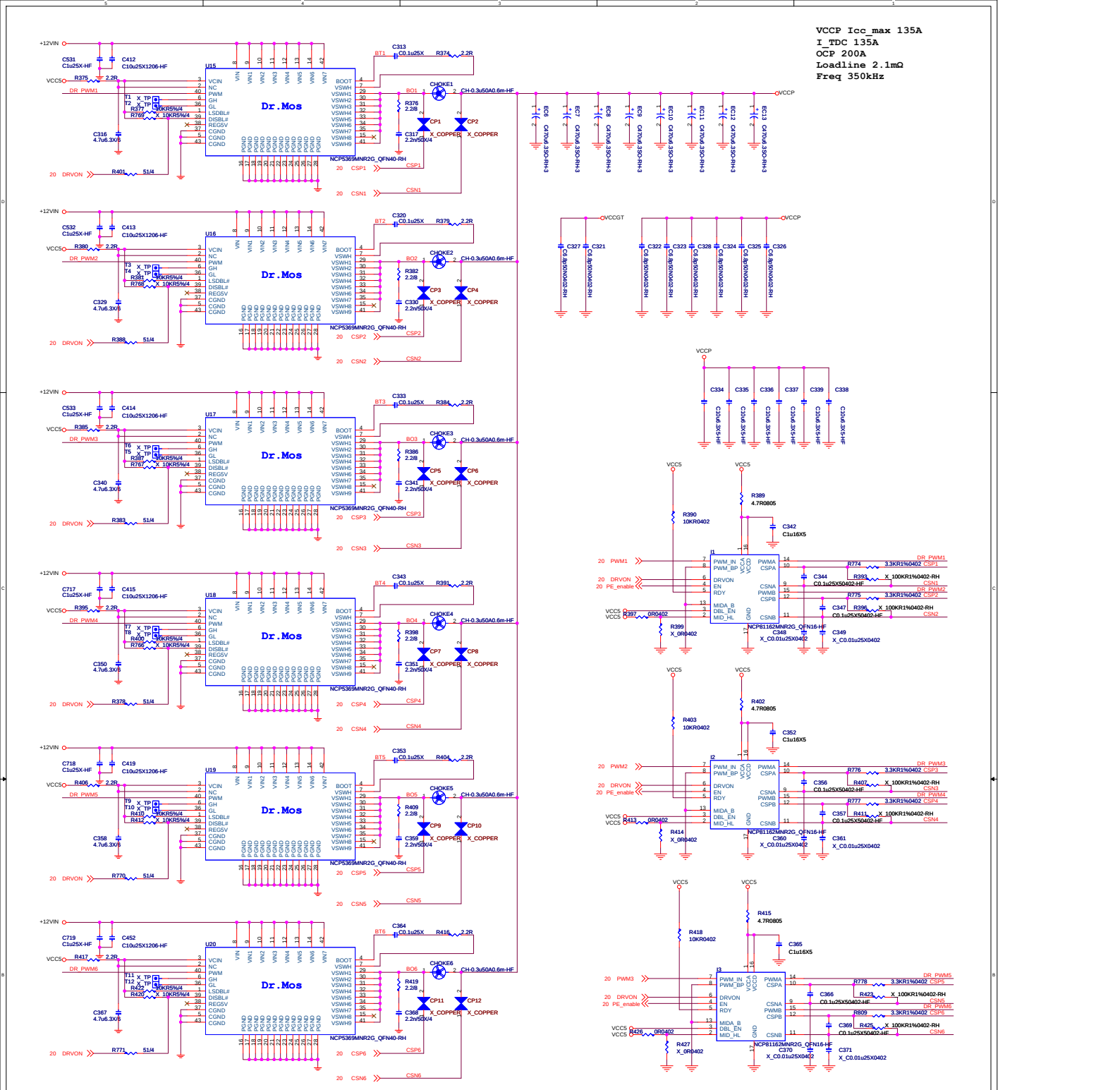

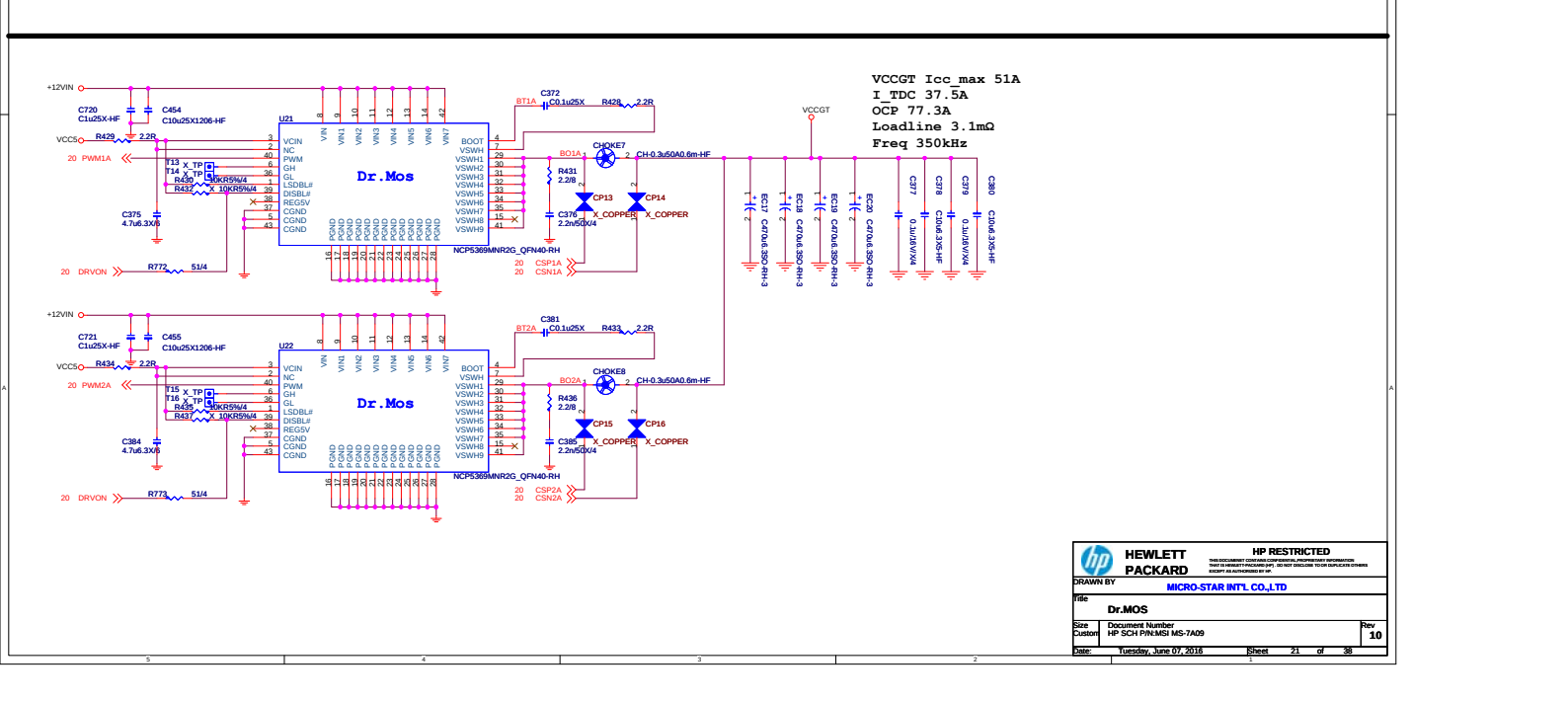

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Title	Dr.MOS		
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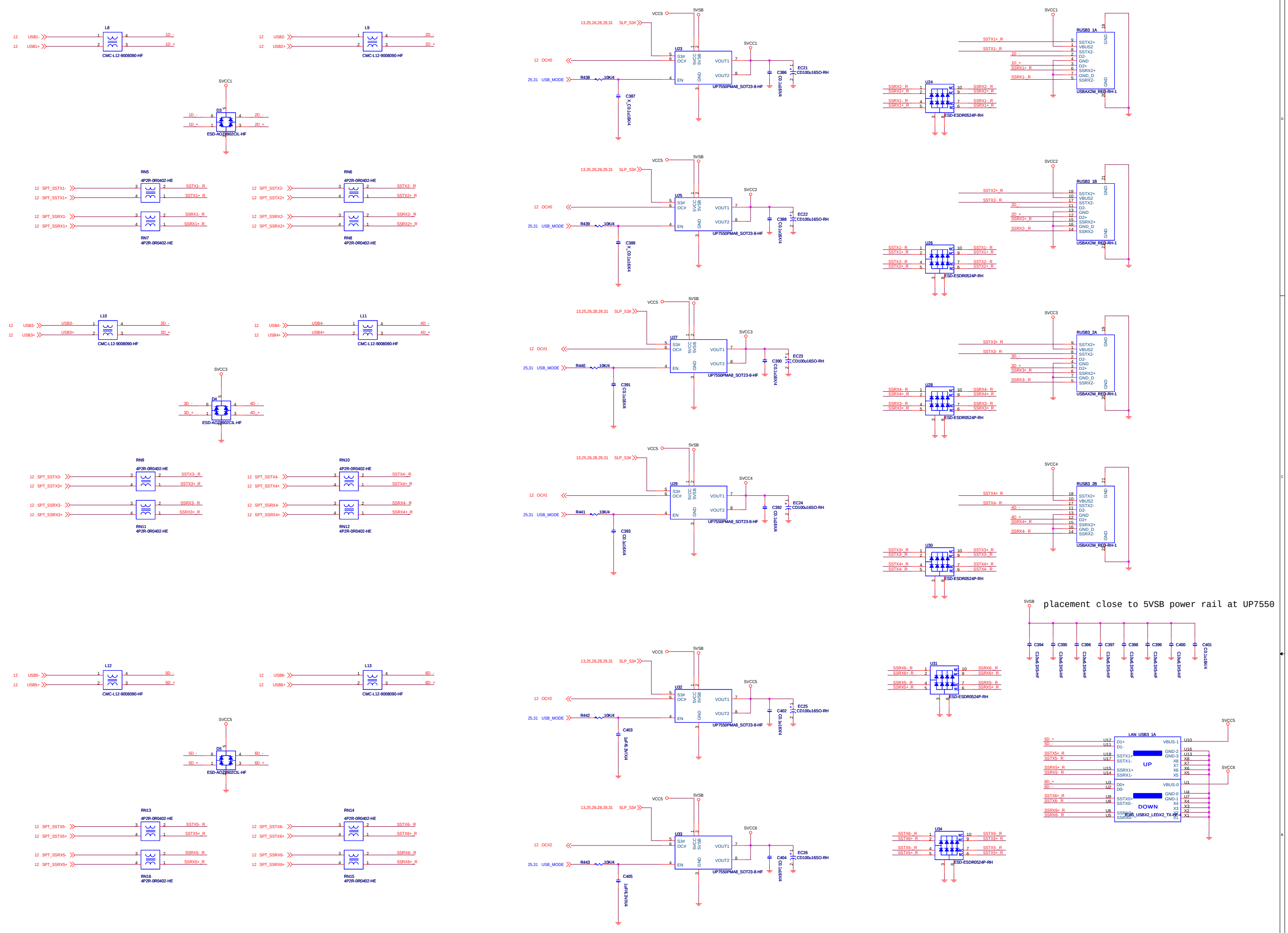
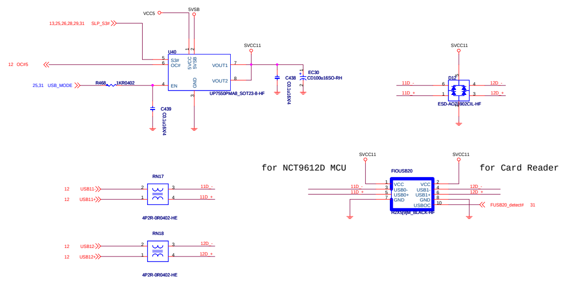
REAR USB3.0



FRONT USB2.0 PIN HEADER



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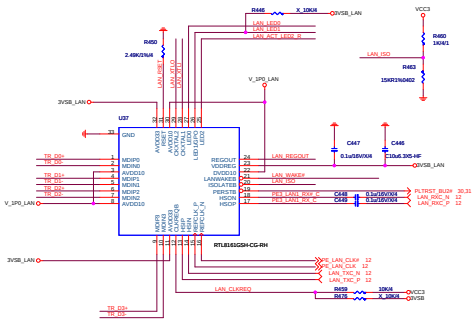
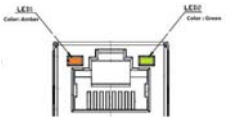
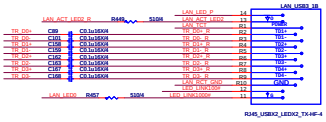
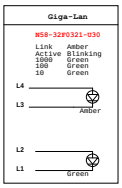
Gigabit LAN RTL8161GSH-CG

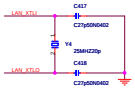


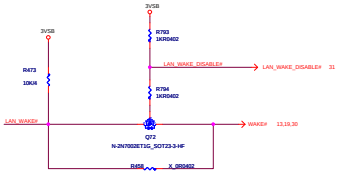


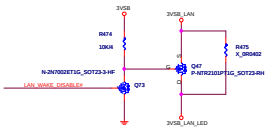
LAN Connector







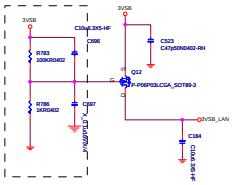




WOL ON	Speed	Active/Idle Mode		
		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	Blink Amber	Blink Amber
	100M Bit	Blink Amber	Blink Amber	Blink Amber
	10M Bit	Blink Amber	Blink Amber	Blink Amber
Link Speed LED	1G Bit	Green	Green	Green
	100M Bit	Green	Green	Green
	10M Bit	Green	Green	Green
WOL OFF		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	OFF	OFF
	100M Bit	Blink Amber	OFF	OFF
	10M Bit	Blink Amber	OFF	OFF
Link Speed LED	1G Bit	Green	OFF	OFF
	100M Bit	Green	OFF	OFF
	10M Bit	Green	OFF	OFF
Link OFF		S0	S3/S4	S5
Active LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF
Link Speed LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF

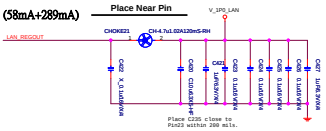
LAN Power

rise time >0.5mS

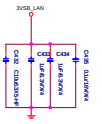


(58mA+289mA)

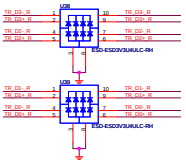
Place Near Pin

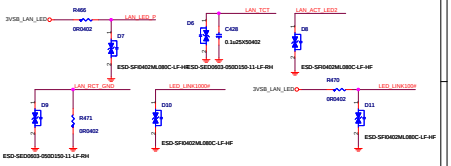


Place Near Pin



ESD





D12,D14,
DOG-1500500-SI0
AVL:DOG-3500510-N47

D11,D13,D15,D16
DOG-2950500-SI0
AVL:DOG-3010510-I05

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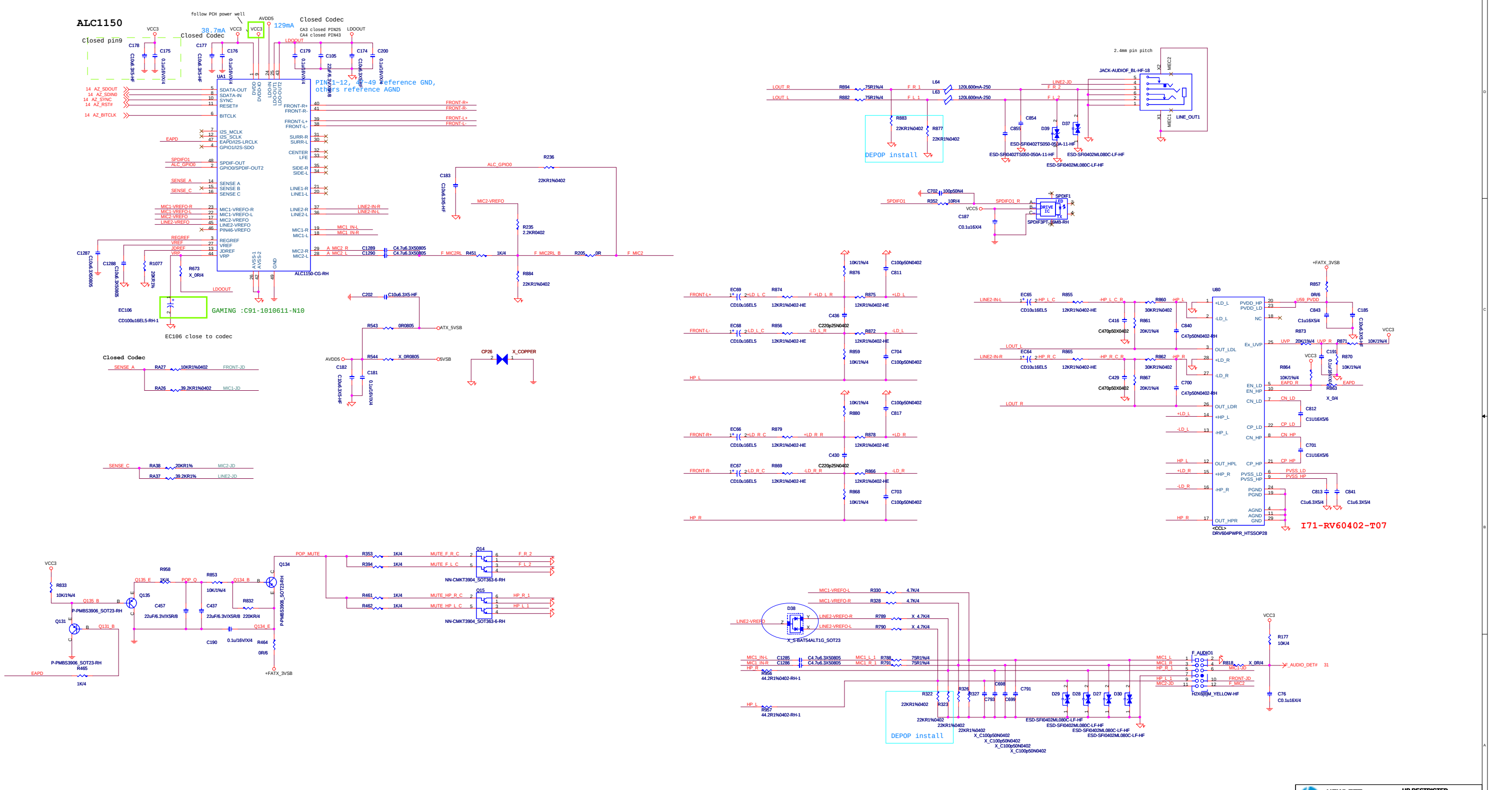

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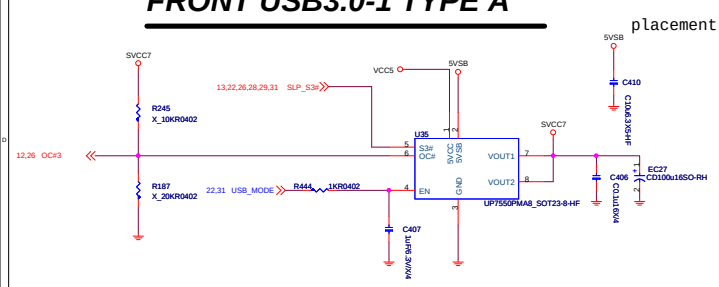
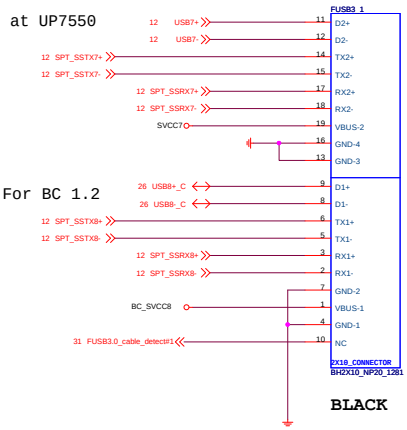
FRONT USB3.0-1 TYPE A

placement close to 5VSB power rail at UP7550



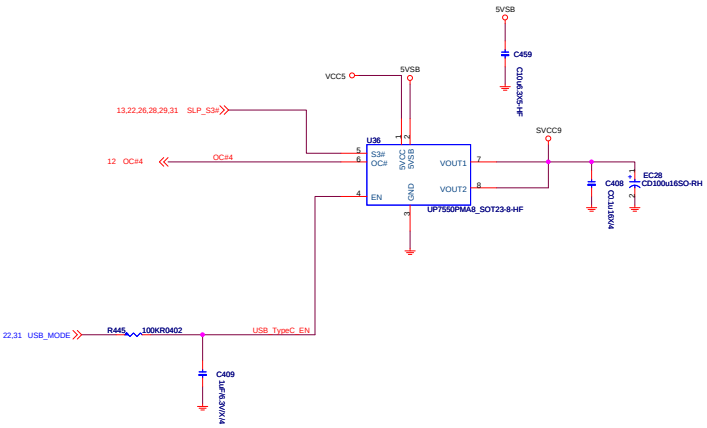
For BC 1.2

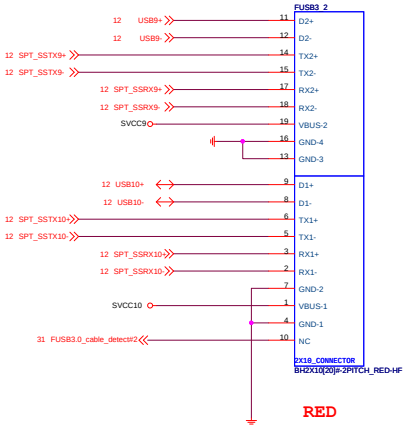


BLACK

FRONT USB3.0-1 TYPE C

placement close to 5VSB power rail at UP7550

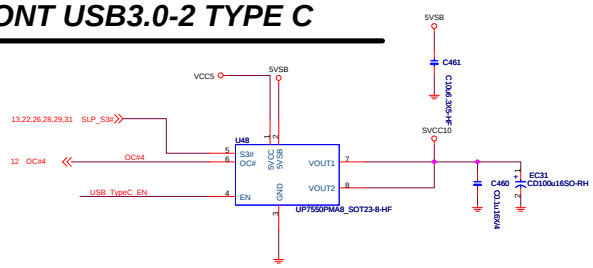




RED

placement close to 5VSB power rail at UP7550

FRONT USB3.0-2 TYPE C



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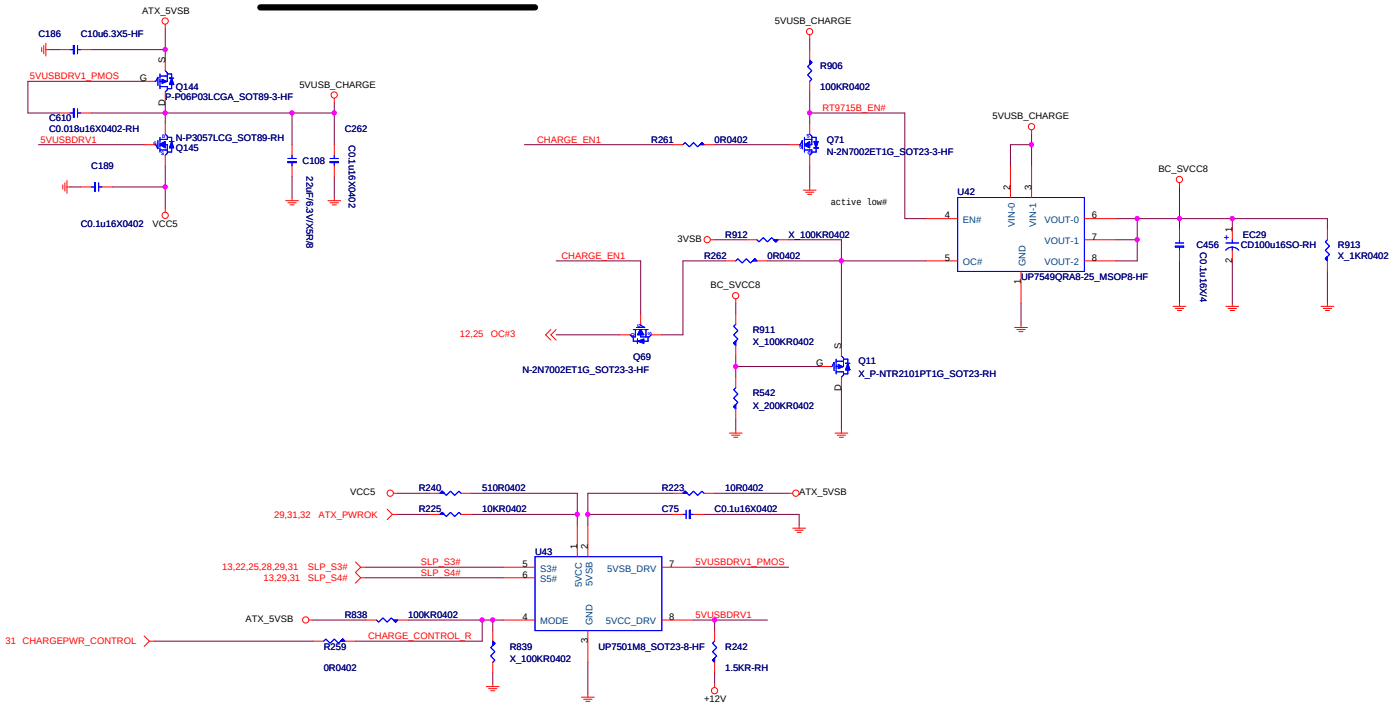
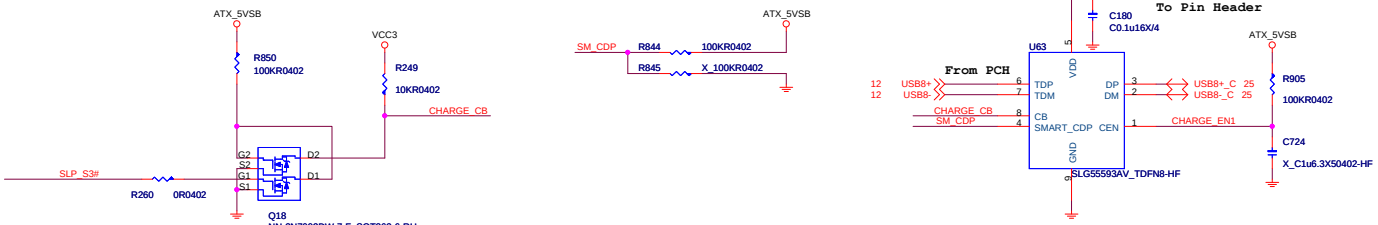
USB CHARGE for BC 1.2



CB MODE: Low support S0/S3 for offical USB function without charge.
CB MODE: Hi support S0/S3/S4/S5 for full charge function without KB/MOUSE wake.



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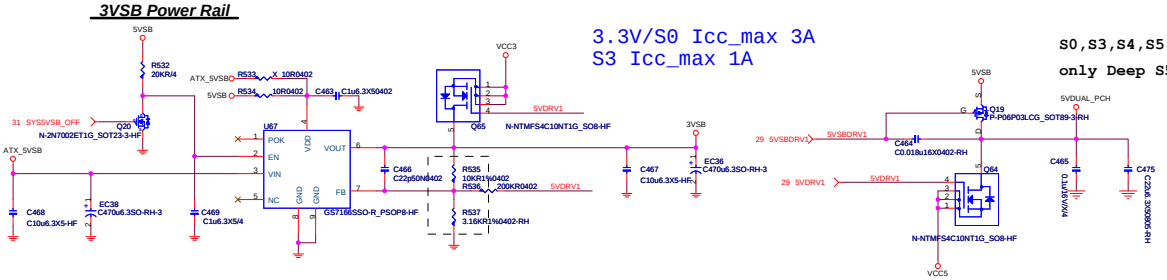
3VSB Power Rail

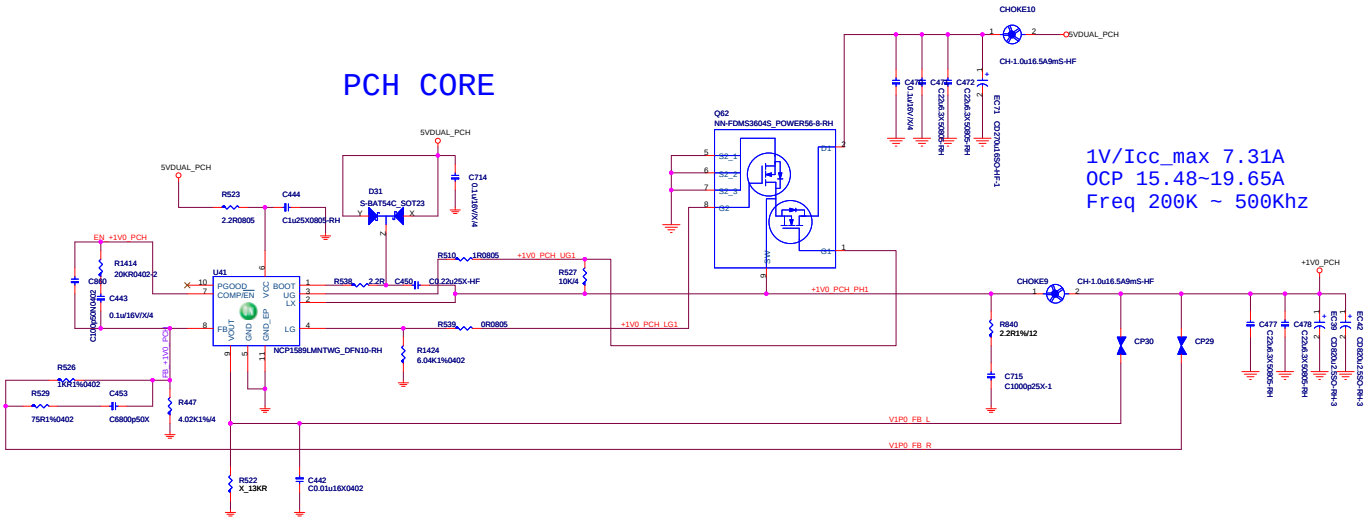
3.3V/S0 Icc_max 3A
S3 Icc_max 1A

S0,S3,S4,S5 5VDUAL_PCH power rail exist.
only Deep S5 no power.



PCH CORE

1V/Icc_max 7.31A
OCP 15.48~19.65A
Freq 200K ~ 500Khz



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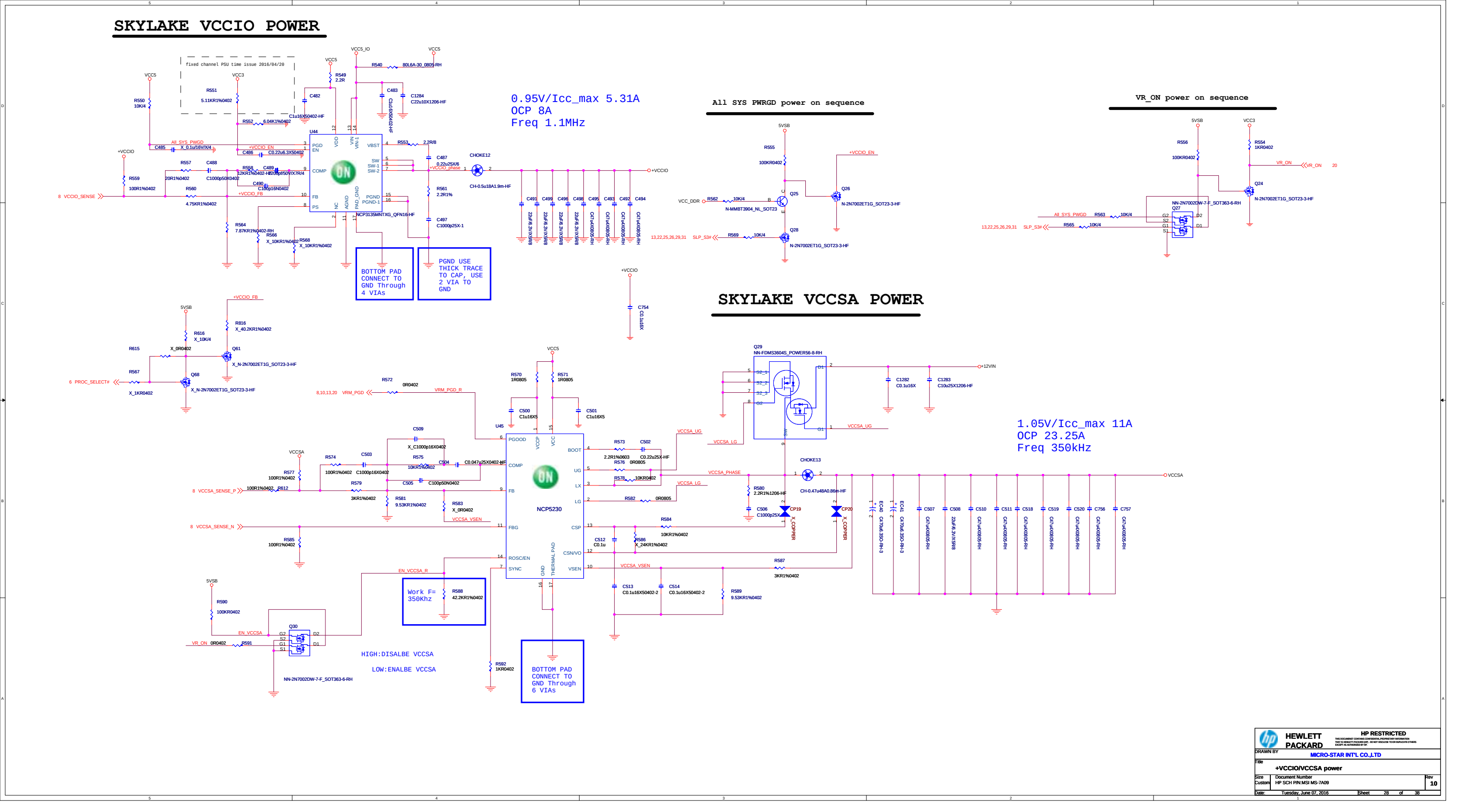
SKYLAKE VCCIO POWER
Fixed channel PSU time issue 2016/04/20
0.95V/Icc_max 5.31A
OCP 8A
Freq 1.1MHz
All SYS PWRGD power on sequence
VR_ON power on sequence
NCP3135MNTXG_QFN16-HF
CHOKE12
BOTTOM PAD CONNECT TO GND Through 4 VIAs
PGND USE THICK TRACE TO CAP, USE 2 VIA TO GND
SKYLAKE VCCSA POWER
1.05V/Icc_max 11A
OCP 23.25A
Freq 350kHz
NCP5230
CHOKE13
NN-FDMS3604S_POWER56-8-RH
Work F= 350Khz
HIGH:DISALBE VCCSA
LOW:ENALBE VCCSA
BOTTOM PAD CONNECT TO GND Through 6 VIAs
+VCCIO
VCCSA
+12VIN
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+VCCIO/VCCSA power
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EN_VCCSA

S0,S3,S4,S5 5VDIMM power rail working.
only Deep S5 no power.

DDR4 1.2V POWER

1.2V/Icc_max 12A
OCP 21~26.3A
Freq 200K ~ 500Khz

DDR4 2.5V POWER

2.5V/Icc_max 2.25A
OCP 4~6A
Freq 500Khz

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

Bit7=0
OUT1=10uA
0x6A:RH=22K,RL=30K

VPP ramp down almost 30 ms after VCC_DDR ramp down
follow JEDEC requirement

VTT DDR 0.6V Power

0.6V/Icc_max 0.75A

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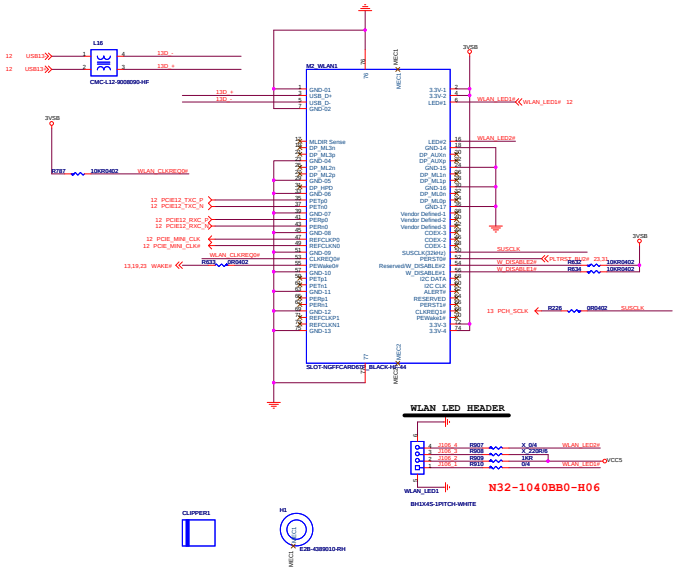
WLAN Key A
plating GF & Height 8.5mm

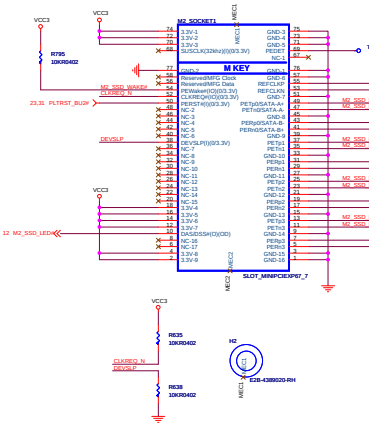


WLAN LED HEADER

CLIPPER1

H2 E16-4389010-RH

M2 SSD-KEY-M



32.768KHz Clock buffer

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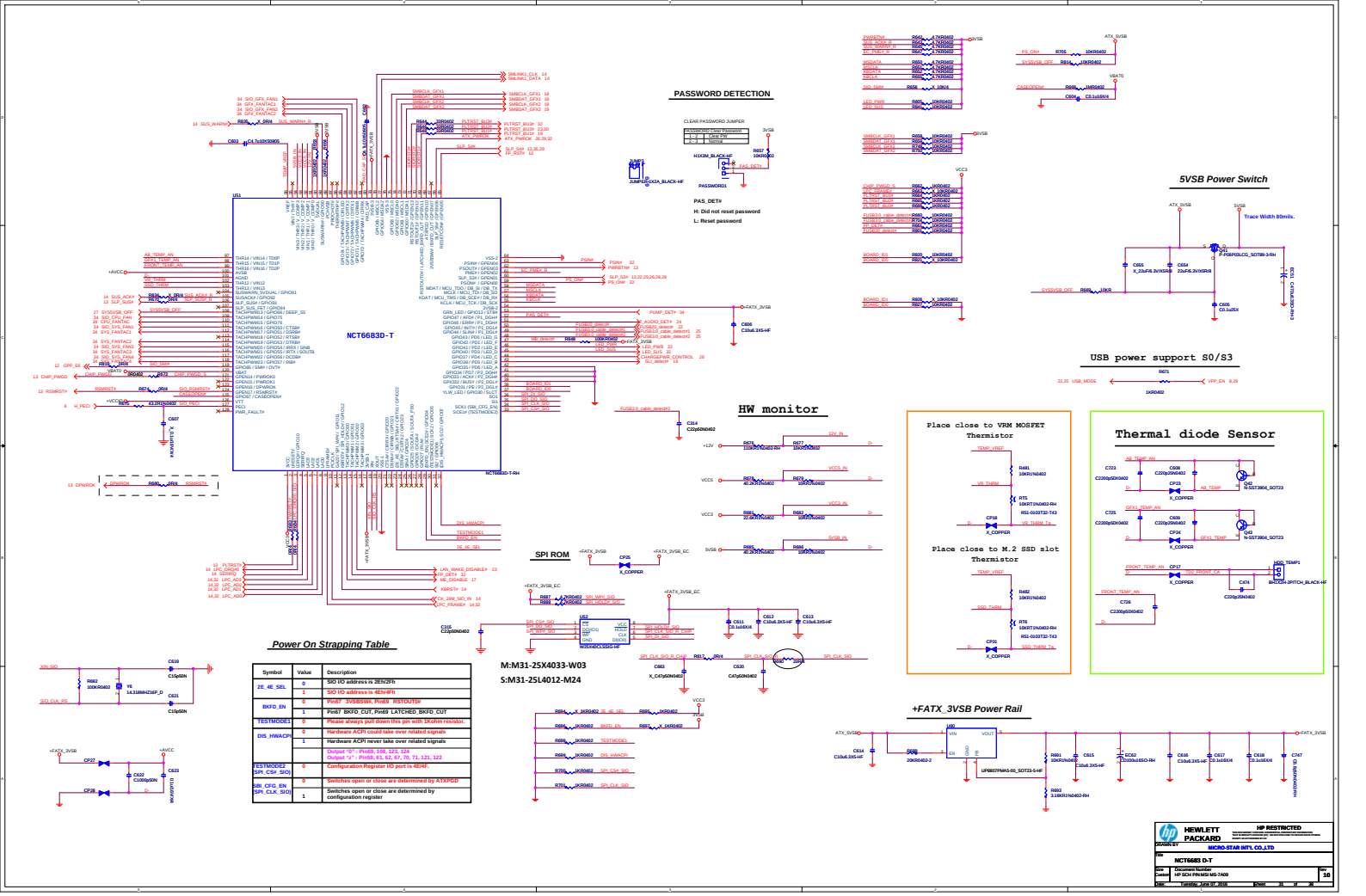
Rev	1.0
Date:	Tuesday, June 17, 2014
Sheet	30 of 38



Symbol	Value	Description
2E_4E_SEL	0	SIO I/O address is 2Eh/2Fh
	1	SIO I/O address is 4Eh/4Fh
BKFD_EN	0	Pin67 BKFD_CUT, Pin69 LATCHED_BKFD_CUT
	1	Pin67 3VSBSWH, Pin69 RSTOUT0#
TESTMODE1	0	Please always pull down this pin with 1K±5% resistor.
DIS_HWACPI	0	Hardware ACPI could take over related signals
	1	Hardware ACPI never take over related signals
		Output "0" - Pin69, 108, 123, 124 Output "Hi" - Pin69, 61, 63, 67, 70, 71, 121, 122
TESTMODE2 SPI_CS#_SIO1	0	Configuration Register I/O port is 4Eh/F.
SBI_CFG_EN SPI_CLK_SIO1	0	Switches open or close are determined by ATXPGD
	1	Switches open or close are determined by configuration register

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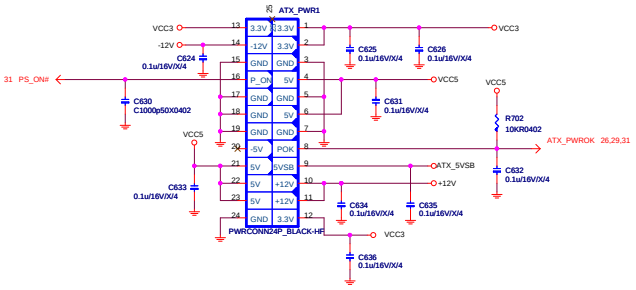
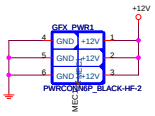
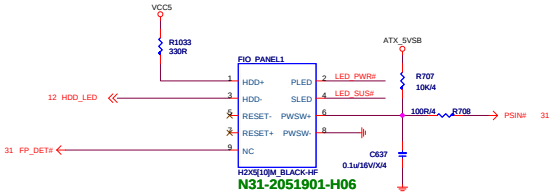


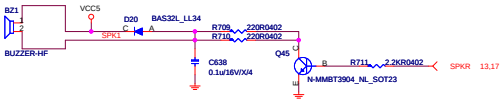


Front Panel

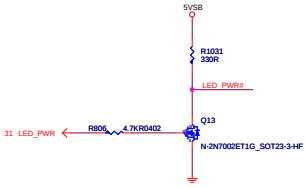


N31-2051901-H06

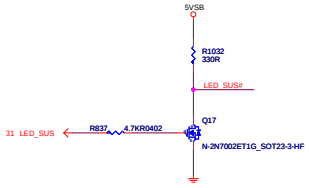
Internal Buzzer



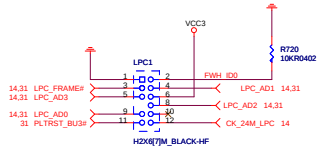
Power LED



SUS LED



LPC Debug Port



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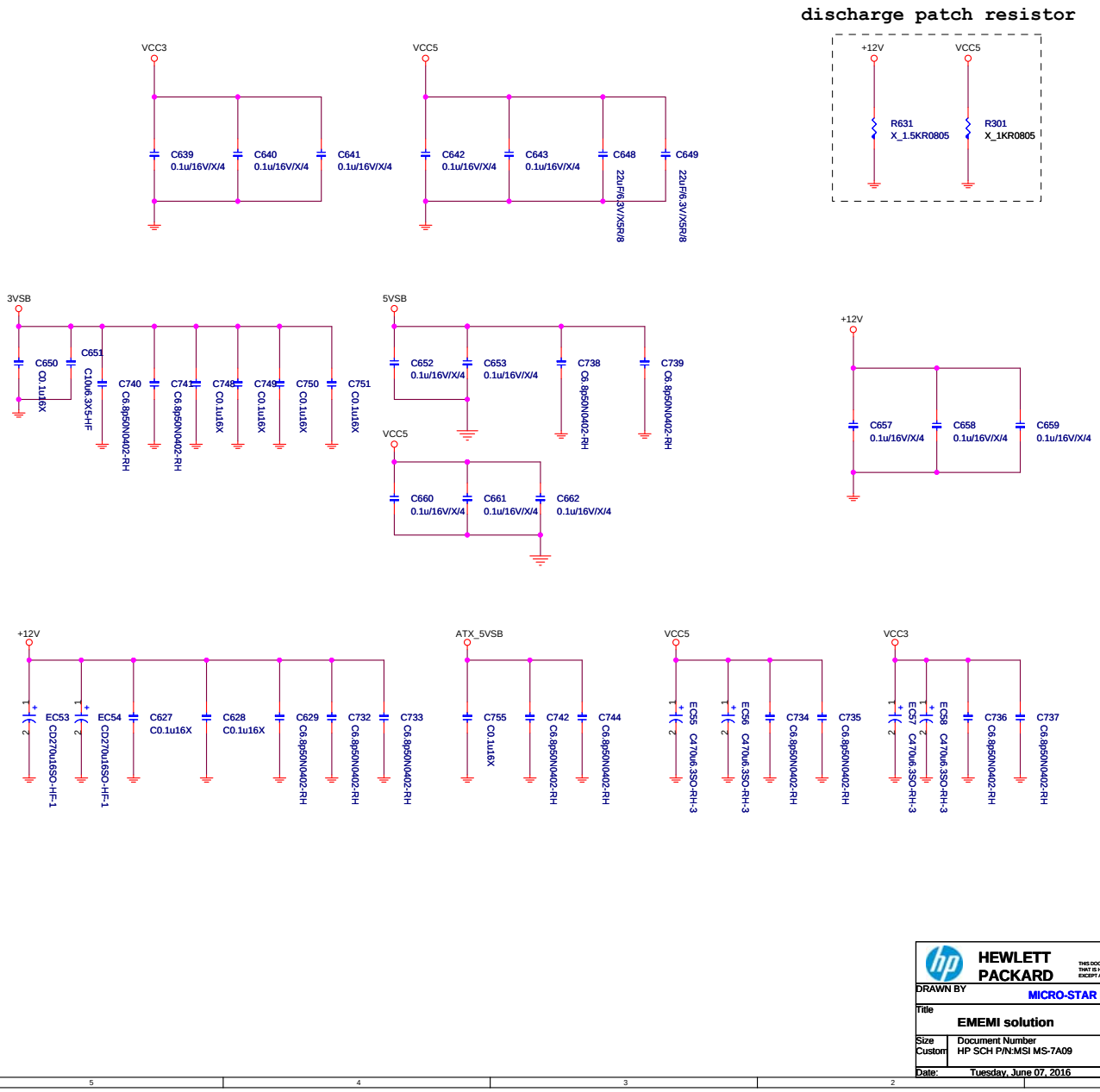
EMI Decoupling Cap



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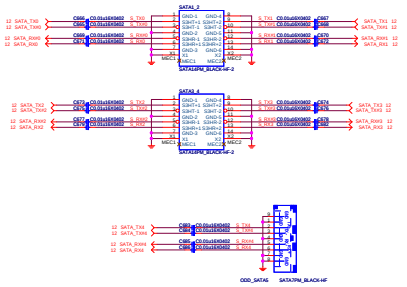
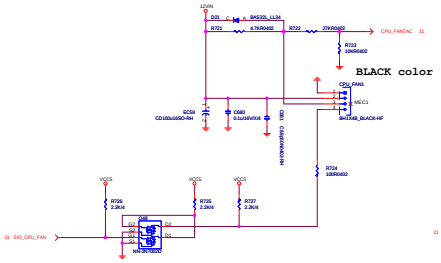
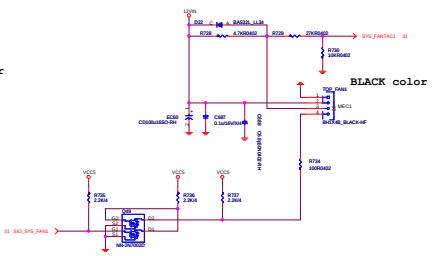
SATA port



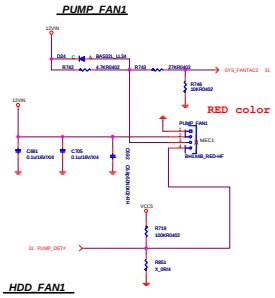
CPU FAN1



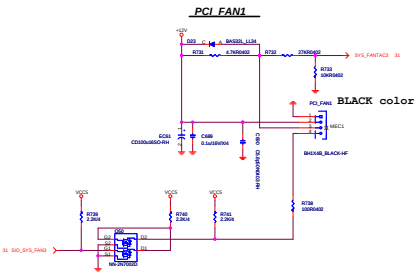
TOP FAN1



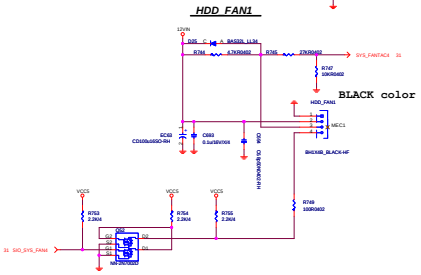
PUMP FAN1



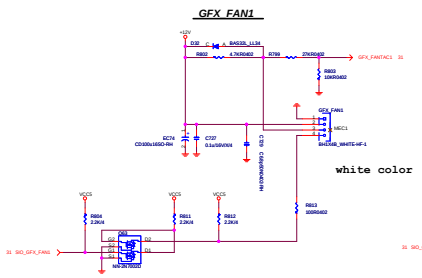
PCI FAN1



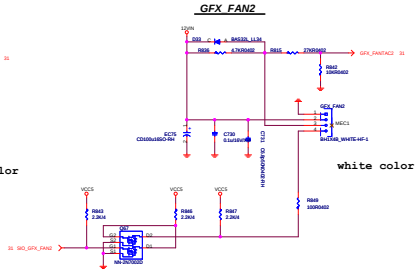
HDD FAN1



GFX FAN1



GFX FAN2



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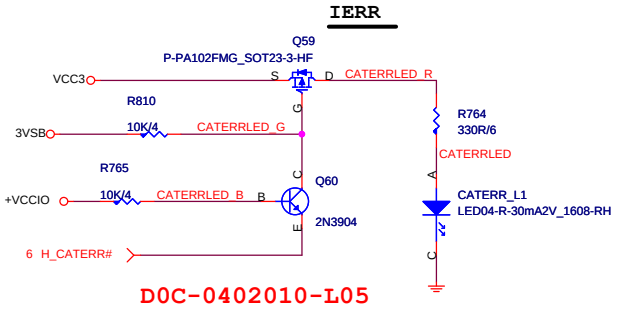

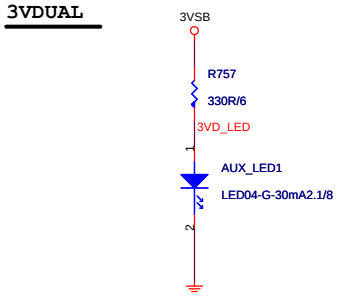

D0C-0402010-L05

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Title: SYSTEM signal LED display

Size	Document Number	Rev
Custom	HP SCH P/N:MSI MS-7A09	10

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Mounting Holes

PCB1

7A09-1.1

HDMI_LOGO1

HDMI Logo

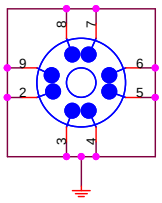
Y01-RHDMI03-000

LA1

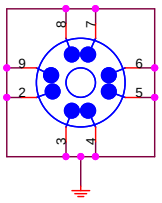
AMI_BIOS LABLE

BIOS_LABLE

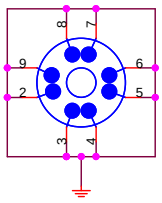
MTG1



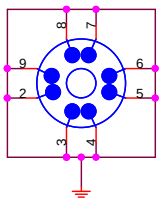
MTG2



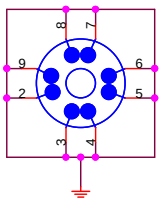
MTG3



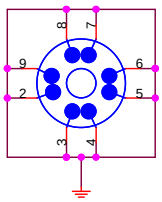
MTG4



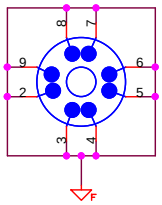
MTG5



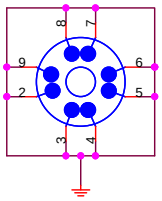
MTG6



MTG7



MTG8



CPU_BP1

E22-B009010-C22

E22-B009010-C22
AVL:E93-0000099-A21

VBAT-S1

BAT-BCR2032P-HF

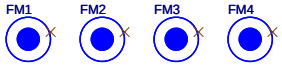
CPU_H1

E21-AC71010-L06

E21-AC71010-L06
AVL:E21-7826010-F02

Optical Fiducial Marks-X

FM1 FM2 FM3 FM4



X_FM X_FM X_FM X_FM

FM5 FM6 FM7 FM8

X_FM X_FM X_FM X_FM

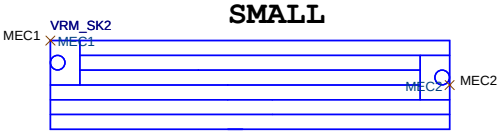
BIG

VRM_SK1

HS-0001110-HF

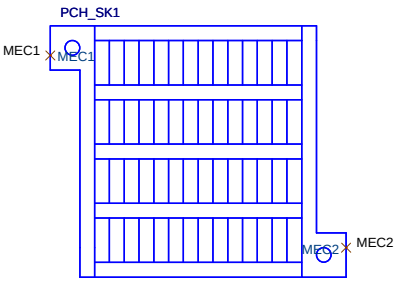
SMALL

VRM_SK2



HS-0503870-HF

PCH_SK1



HS-0407850-RH

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HP RESTRICTED

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Title: **Manual Parts**

Size	Document Number	Rev
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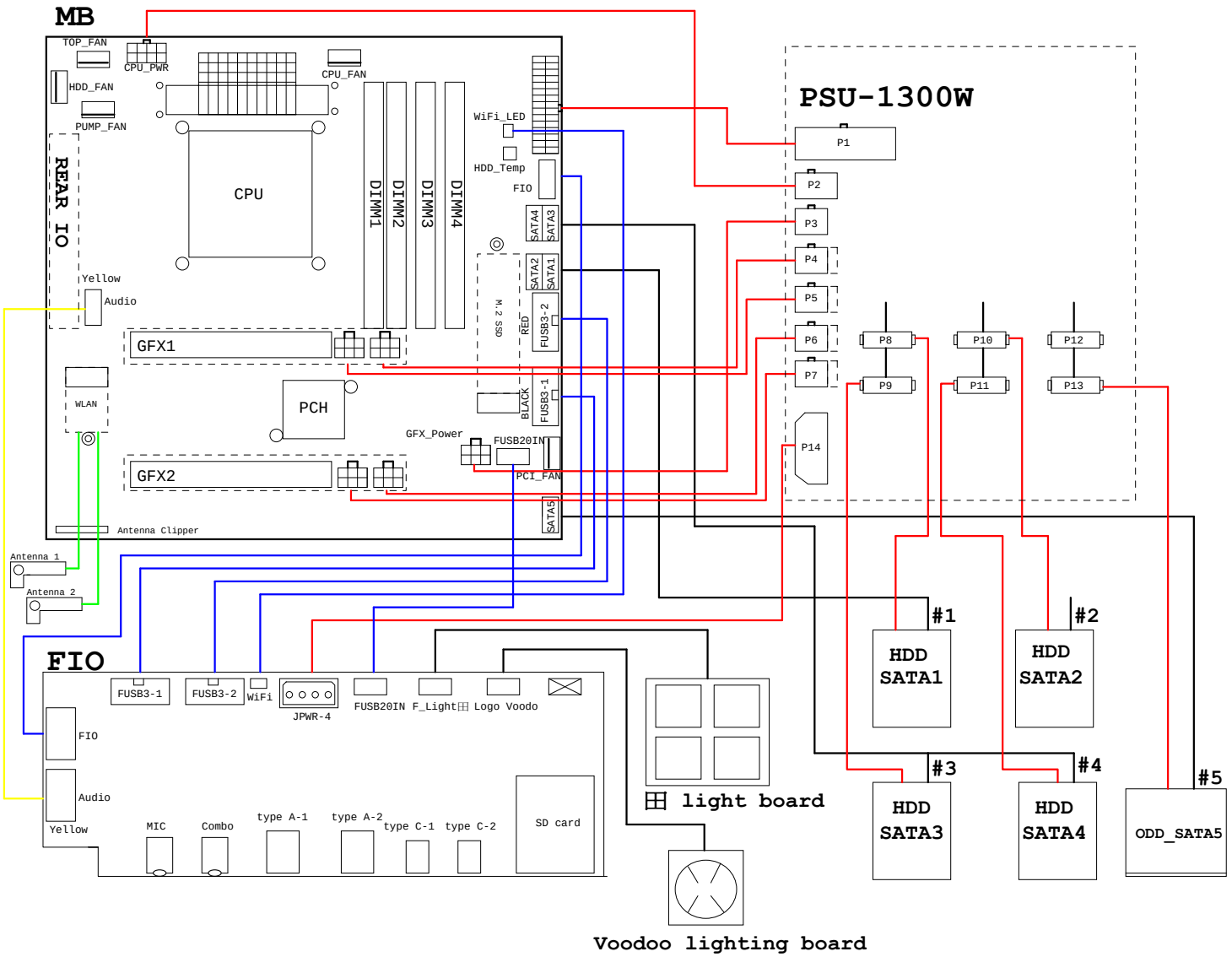
SYSTEM cable routing for 1300w PSU



SYSTEM cable routing for 600w PSU